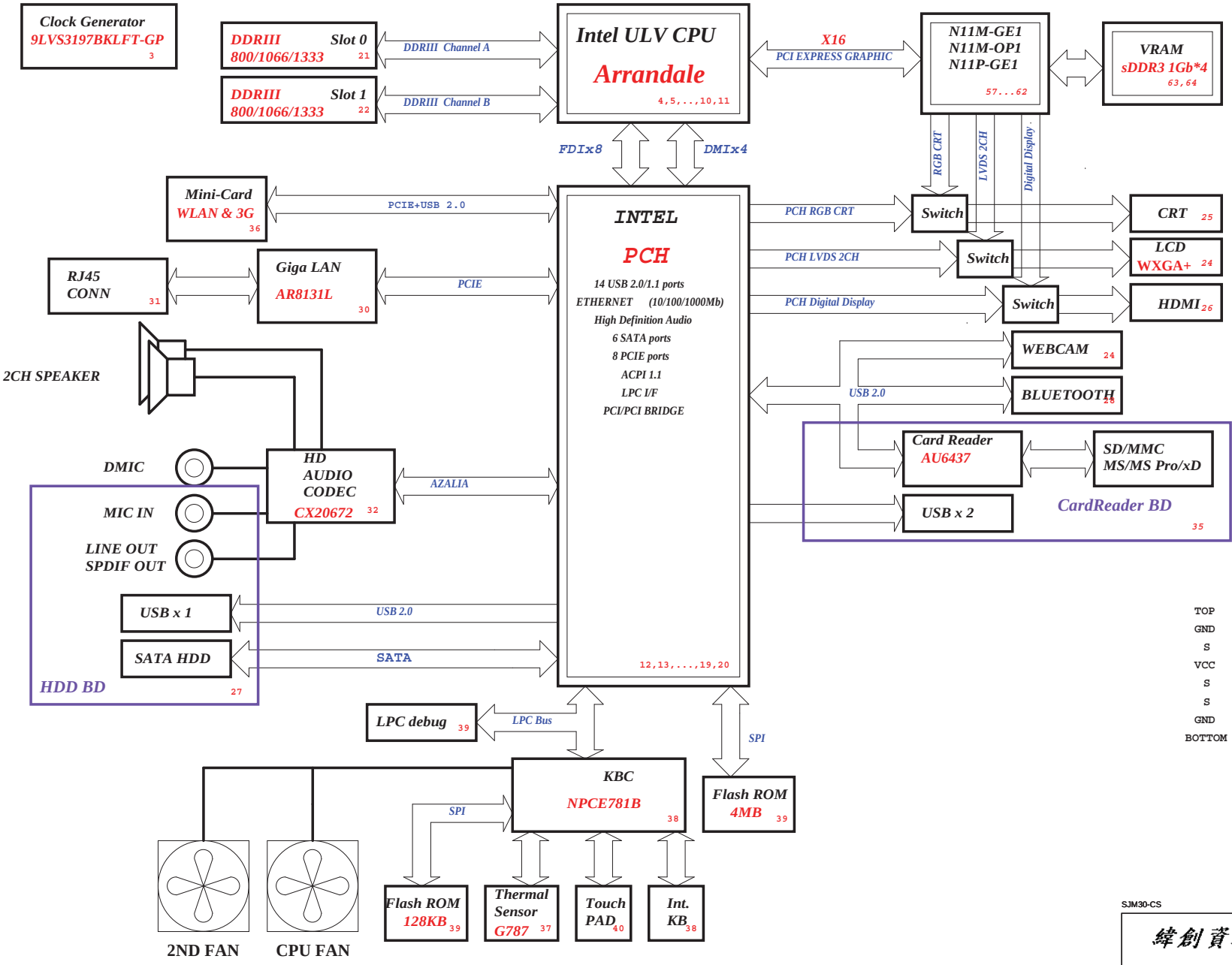
SJM30-CS Block Diagram

Project code:91.4HR01.001
PCBA :55.4HR01.M06G
PCB P/N :48.4HR01.021
REVISION :-2



SYSTEM DC/DC RT8223B	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5 46

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D5V_S3 47

SYSTEM DC/DC RT8209E	
INPUTS	OUTPUTS
DCBATOUT	1D05V_S0 48

SYSTEM DC/DC ISL62881	
INPUTS	OUTPUTS
DCBATOUT	VCC_GFXCORE 51

CPU DC/DC RT8152D	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE 44

INTERSIL CHARGER ISL88731A	
INPUTS	OUTPUTS
DCBATOUT	BT+ 50

PCB STACKUP

TOP	
GND	
S	
VCC	
S	
S	
GND	
BOTTOM	

SJM30-CS

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Title: Block Diagram

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PCH Strapping

Name	Schematics Notes
SPKR	**Reboot option at power-up** **Default Mode:** Internal weak Pull-down. **No Reboot Mode with TCO Disabled:** Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	**Default Mode:** Internal pull-up. **Low (0) = Top Block Swap Mode** (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	**High (1) = Integrated VRM is enabled** **Low (0) = Integrated VRM is disabled**
GNT0#, GNT1#	**Default (SPI):** Left both GNT0# and GNT1# floating. No pull up required. **Boot from PCI:** Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. **Boot from LPC:** Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	**Default - Internal pull-up.** **Low (0)**= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	**Default:** Do not pull low. **Disable ME in Manufacturing Mode:** Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	**Enable iTPM:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor **Disable iTPM:** Left floating, no pull-down required.
NV_ALE	**Enable Danbury:** Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. **Disable Danbury:** Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	**Low (0):** Flash Descriptor Security will be overridden. **High (1) :** Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	**Default = Do not connect (floating)** High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

Processor Strapping

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	**Embedded DisplayPort Presence**	**1:** Disabled - No Physical Display Port attached to Embedded DisplayPort. **0:** Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	**PCI-Express Static Lane Reversal**	**1:** Normal Operation. **0:** Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	**PCI-Express Configuration Select**	**1:** Single PCI-Express Graphics **0:** Bifurcation enabled	1
CFG[7]	**Reserved - Temporarily used for early Clarksfield samples.**	**Clarksfield (only for early samples pre-ES1)** - Connect to GND with 3.01K Ohm/5% resistor **Note:** Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

PCIE Routing

LANE1	LAN
LANE2	MiniCard1
LANE4	MiniCard2

USB Table

Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WECAM
5	SIM CARD
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

SJM30-CS

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Title: **Table of Content**

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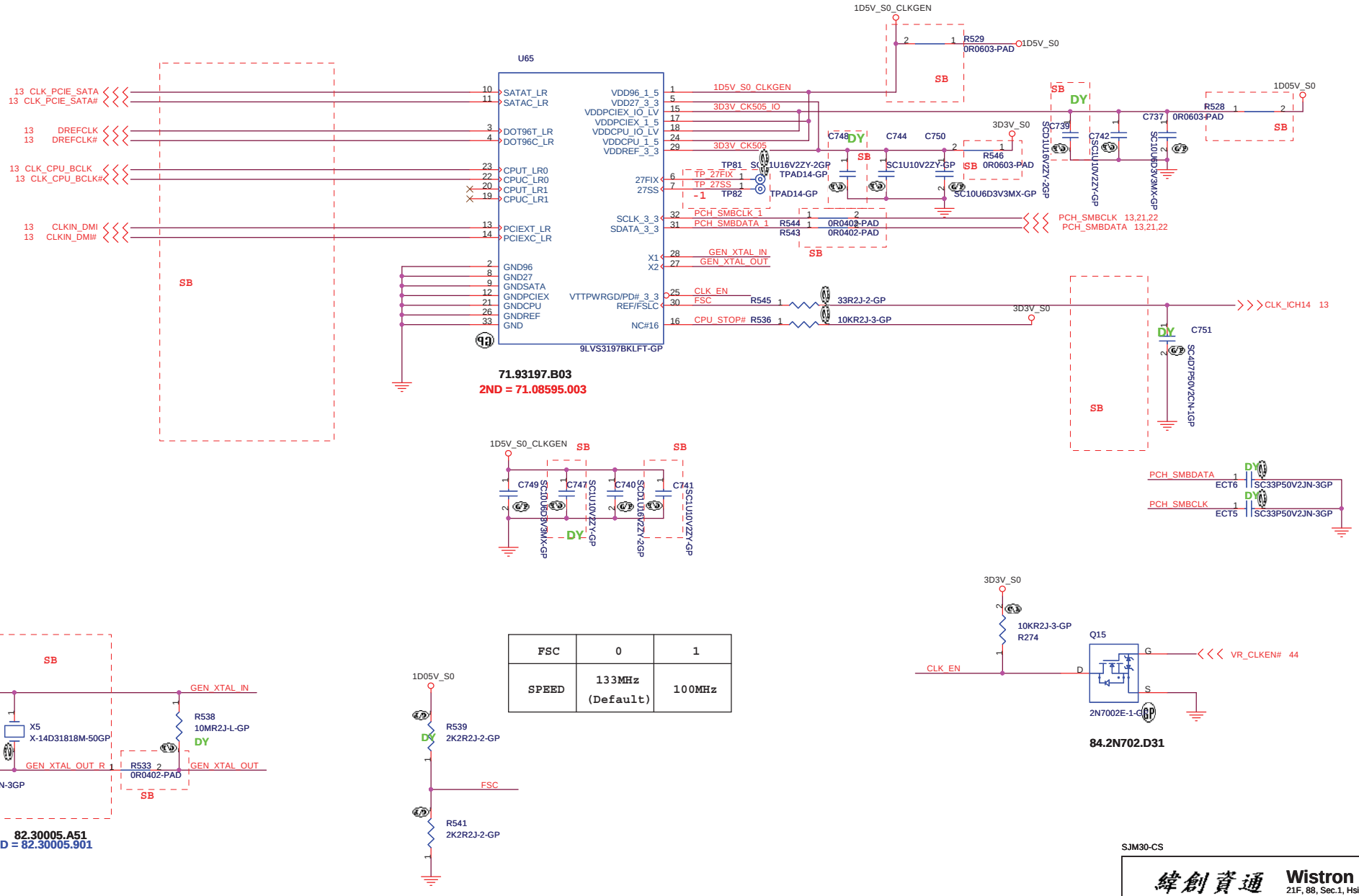

FSC	0	1
SPEED	133MHz (Default)	100MHz

SJM30-CS

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Title: **Clock Generator**

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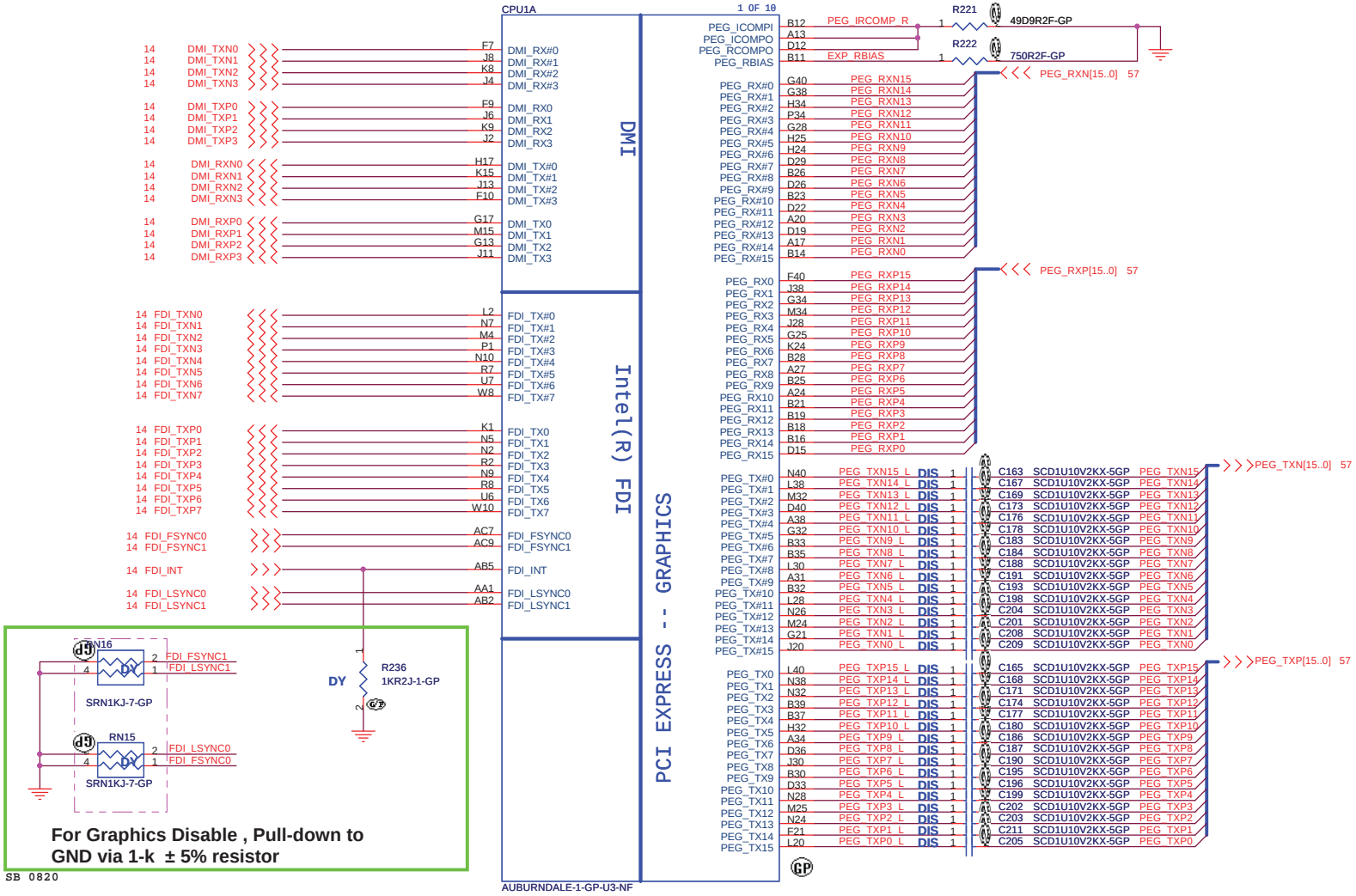

SB 0820

SJM30-CS

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Title: CPU 1 of 8

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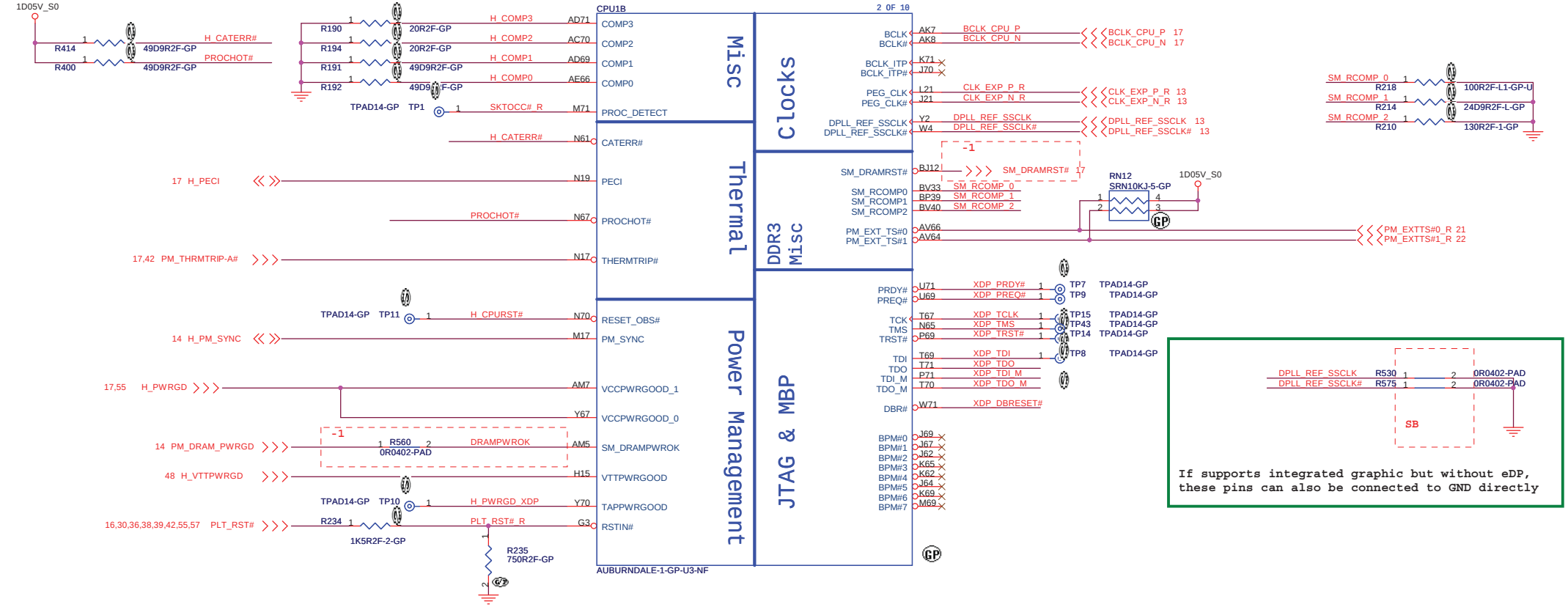

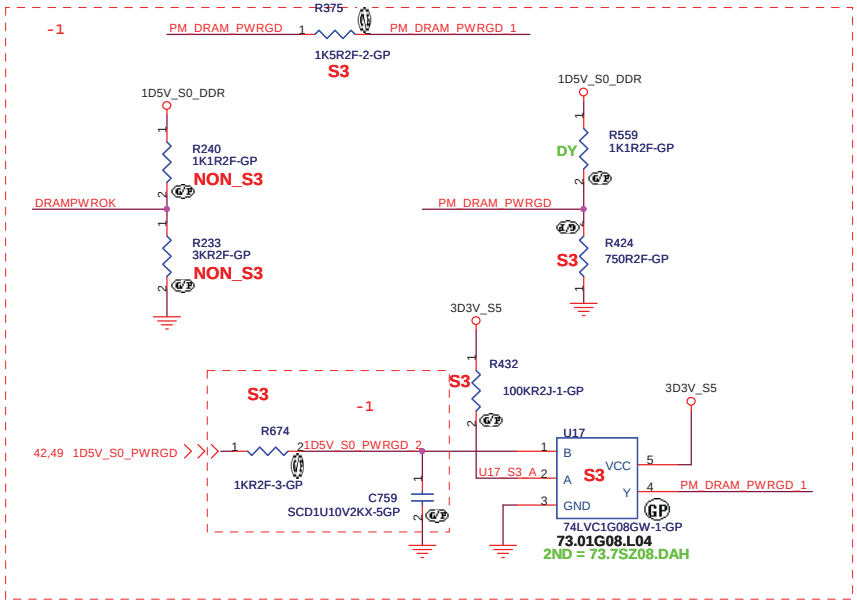

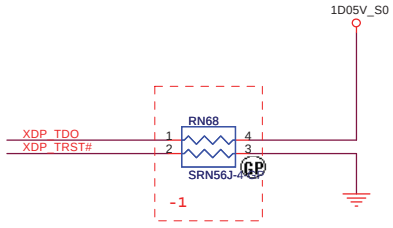

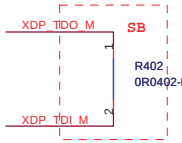

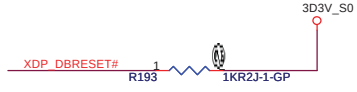

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Title: **CPU 2 of 8**

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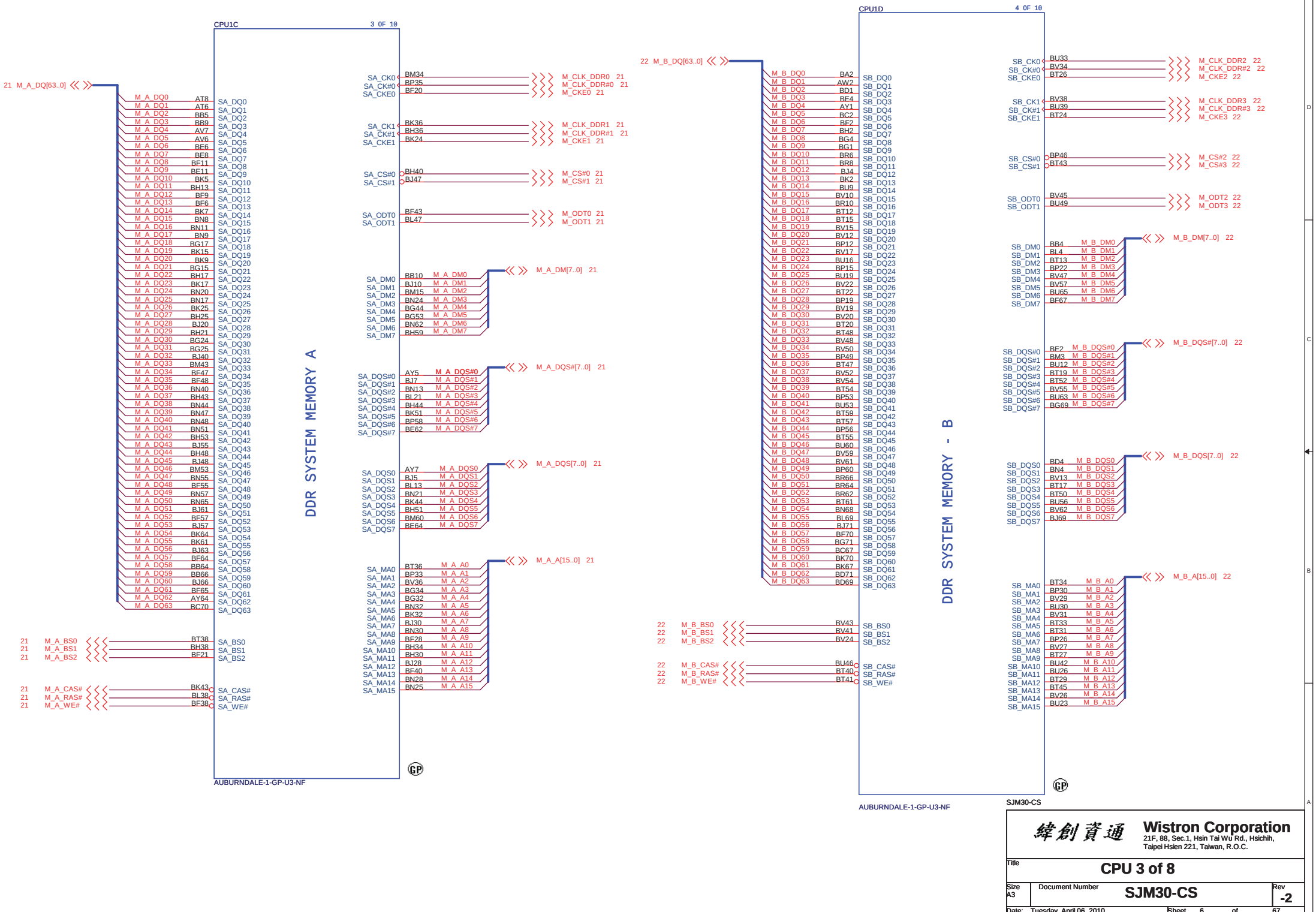

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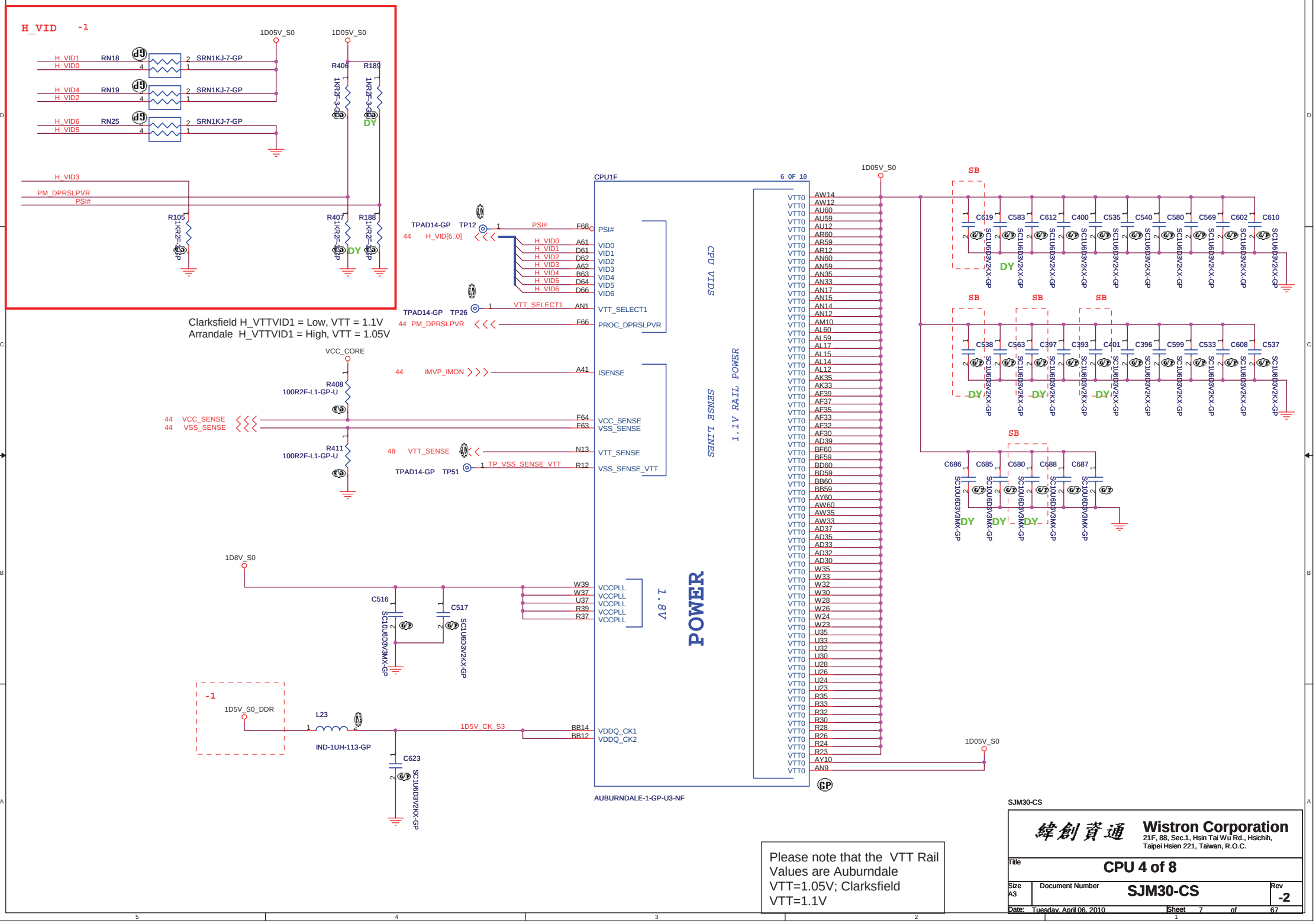
H_VID -1
H_VID1
H_VID0
H_VID4
H_VID2
H_VID6
H_VID5
RN18
RN19
RN25
SRN1KJ-7-GP
1D05V_S0
R406
R189
1KR2F-3-GP
DY
H_VID3
PM_DPRSLPVR
PSI#
R105
R407
R188
Clarksfield H_VTTVID1 = Low, VTT = 1.1V
Arrandale H_VTTVID1 = High, VTT = 1.05V
CPU1F
6 OF 10
TPAD14-GP TP12
44 H_VID[6..0]
PSI#
F68
H_VID0 A61
H_VID1 D61
H_VID2 D62
H_VID3 A62
H_VID4 B63
H_VID5 D64
H_VID6 D66
VID0
VID1
VID2
VID3
VID4
VID5
VID6
CPU VIDS
TPAD14-GP TP26
VTT_SELECT1
AN1
VTT_SELECT1
44 PM_DPRSLPVR
F66
PROC_DPRSLPVR
VCC_CORE
R408
100R2F-L1-GP-U
44 IMVP_IMON
A41
ISENSE
44 VCC_SENSE
44 VSS_SENSE
F64
F63
VCC_SENSE
VSS_SENSE
R411
100R2F-L1-GP-U
48 VTT_SENSE
N13
VTT_SENSE
TPAD14-GP TP51
TP_VSS_SENSE_VTT
R12
VSS_SENSE_VTT
SENSE LINES
1.1V RAIL POWER
1D8V_S0
C516
SC10U6D3V3MX-GP
C517
SC1U6D3V2KX-GP
W39 VCCPLL
W37 VCCPLL
U37 VCCPLL
R39 VCCPLL
R37 VCCPLL
1.8V
POWER
-1
1D5V_S0_DDR
L23
IND-1UH-113-GP
1D5V_CK_S3
BB14 VDDQ_CK1
BB12 VDDQ_CK2
C623
SC1U6D3V2KX-GP
AUBURNDALE-1-GP-U3-NF
VTT0
AW14
AW12
AU60
AU59
AU12
AR60
AR59
AR12
AN60
AN59
AN35
AN33
AN17
AN15
AN14
AN12
AM10
AL60
AL59
AL17
AL15
AL14
AL12
AK35
AK33
AF39
AF37
AF35
AF33
AF32
AF30
AD39
BF60
BF59
BD60
BD59
BB60
BB59
AY60
AW60
AW35
AW33
AD37
AD35
AD33
AD32
AD30
W35
W33
W32
W30
W28
W26
W24
W23
U35
U33
U32
U30
U28
U26
U24
U23
R35
R33
R32
R30
R28
R26
R24
R23
AY10
AN9
1D05V_S0
SB
C619
C583
C612
C400
C535
C540
C580
C569
C602
C610
SCU6D3V2KX-GP
DY
C538
C563
C397
C393
C401
C396
C599
C533
C608
C537
C686
C685
C680
C688
C687
SC10U6D3V3MX-GP
Please note that the VTT Rail Values are Auburndale VTT=1.05V; Clarksfield VTT=1.1V
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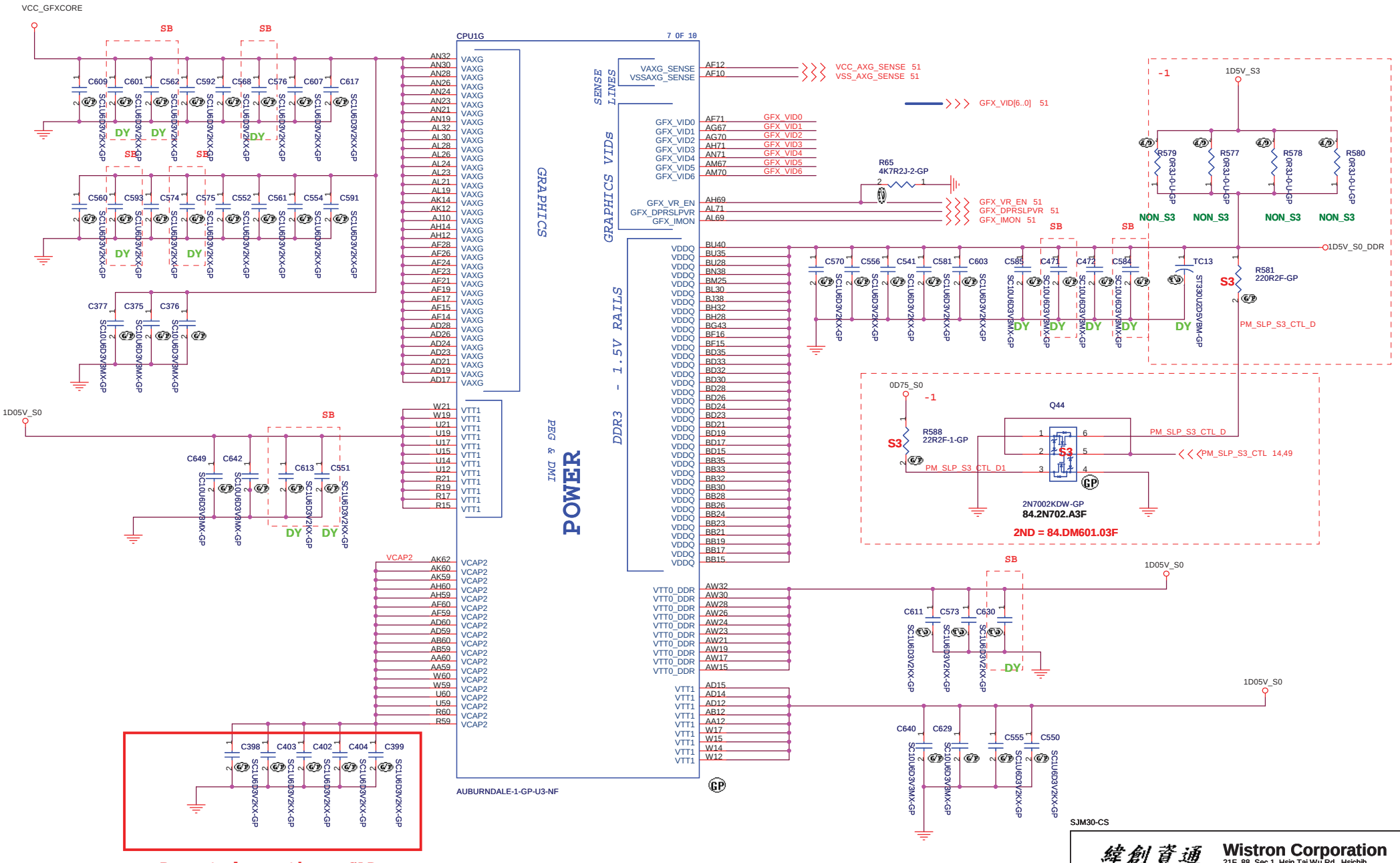
VCC_GFXCORE
CPU1G
7 OF 10
GRAPHICS
PEG & DMI
POWER
SENSE LINES
GRAPHICS VIDS
DDR3 - 1.5V RAILS
AUBURNDALE-1-GP-U3-NF
VAXG_SENSE
VSSAXG_SENSE
VCC_AXG_SENSE 51
VSS_AXG_SENSE 51
GFX_VID[6..0] 51
GFX_VID0
GFX_VID1
GFX_VID2
GFX_VID3
GFX_VID4
GFX_VID5
GFX_VID6
R65
4K7R2J-2-GP
GFX_VR_EN
GFX_DPRSLPVR
GFX_IMON
GFX_VR_EN 51
GFX_DPRSLPVR 51
GFX_IMON 51
1D05V_S0
1D05V_S0_DDR
1D05V_S3
0D75_S0
R579
R577
R578
R580
R581
220R2F-GP
R588
22R2F-1-GP
Q44
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
PM_SLP_S3_CTL_D
PM_SLP_S3_CTL_D1
PM_SLP_S3_CTL 14,49
NON_S3
S3
SB
DY
VCAP2
Do not dummy these CAPs
SJM30-CS
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Title
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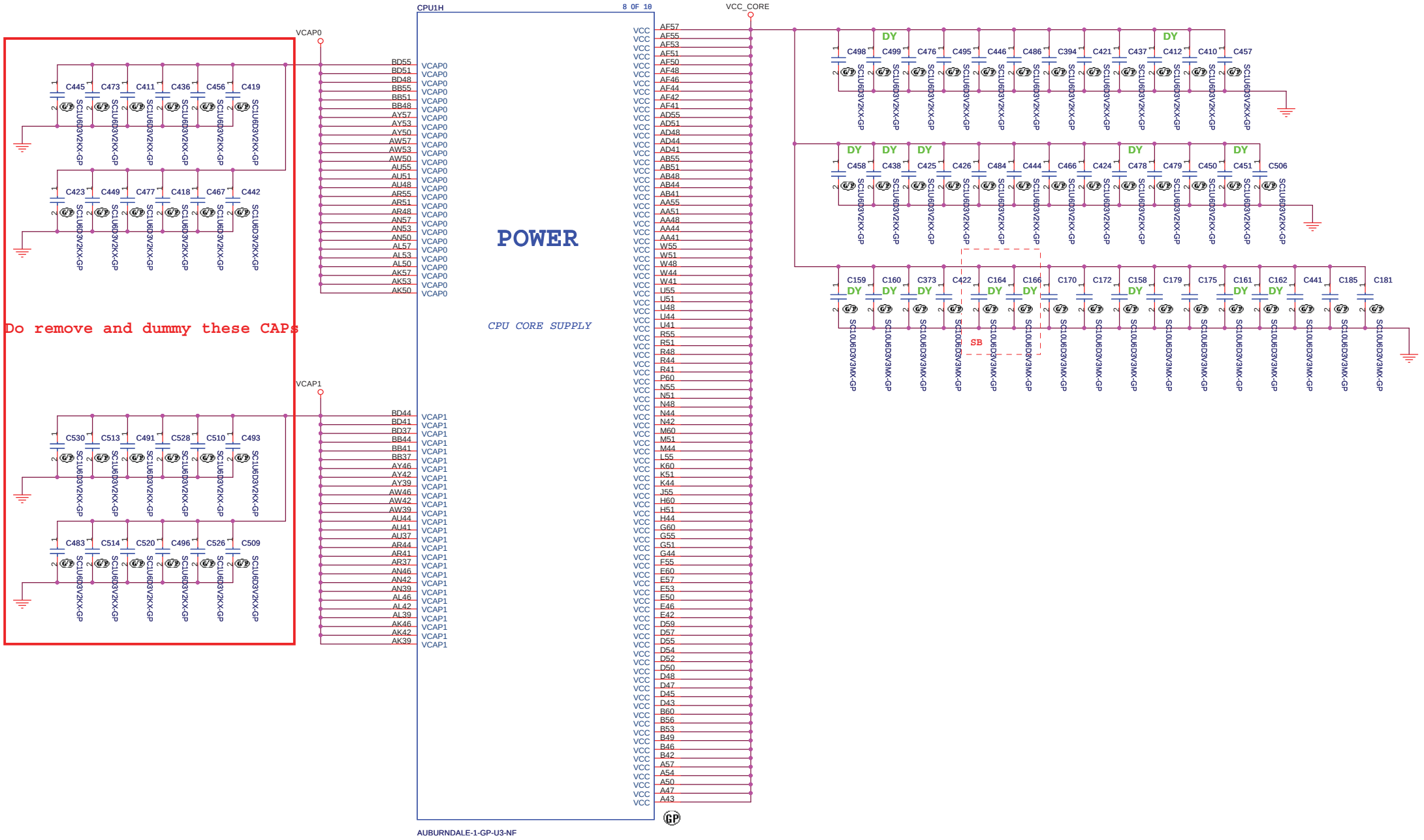

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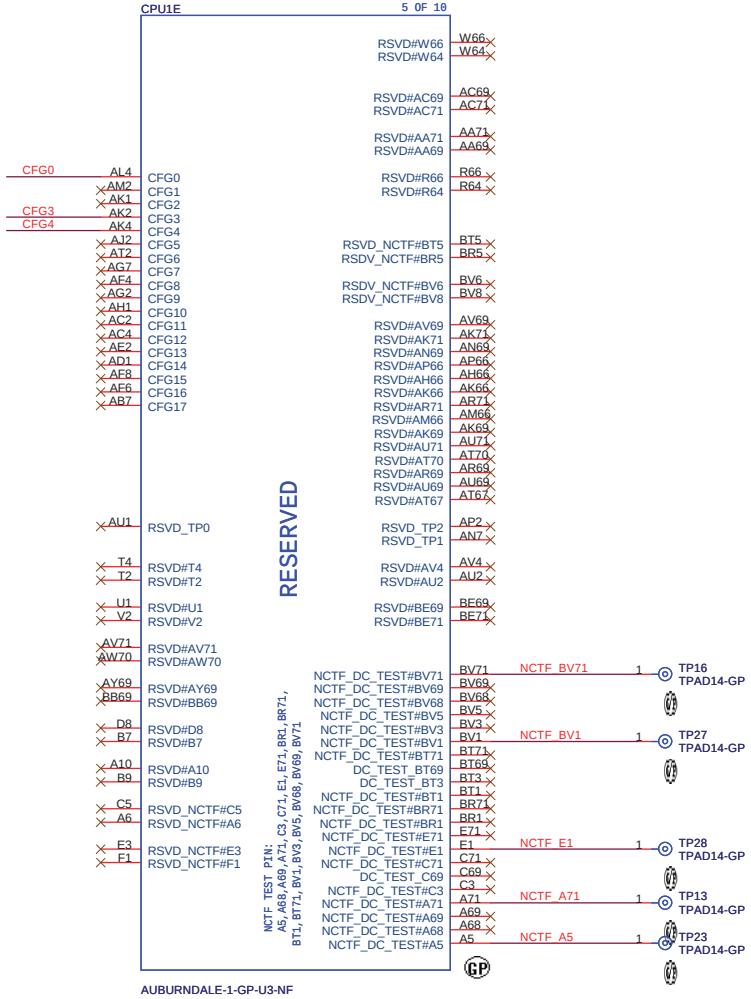

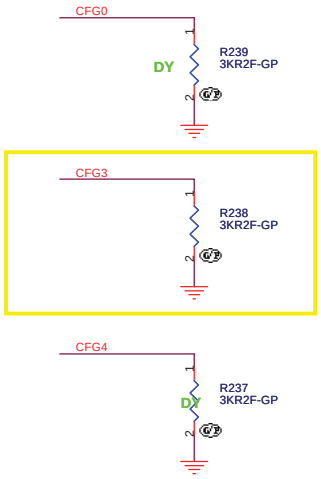

PCI-Express Configuration Select	
CFG0	1:Single PEG 0:Bifurcation enabled

CFG3 - PCI-Express Static Lane Reversal	
CFG3	1 :Normal Operation 0 :Lane Numbers Reversed 15 -> 0, 14 -> 1, ...

CFG4 - Display Port Presence	
CFG4	1:Disabled; No Physical Display Port attached to Embedded Display Port 0:Enabled; An external Display Port device is connected to the Embedded Display Port

CFG7(Reserved) - Temporarily used for early Clarksfield samples.	
CFG7	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor. Note: Only temporary for early CFD sample (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common M/B design (for AUB and CFD), the pull-down resistor shouble be used. Does not impact AUB functionality.

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Title: **CPU 7 of 8**

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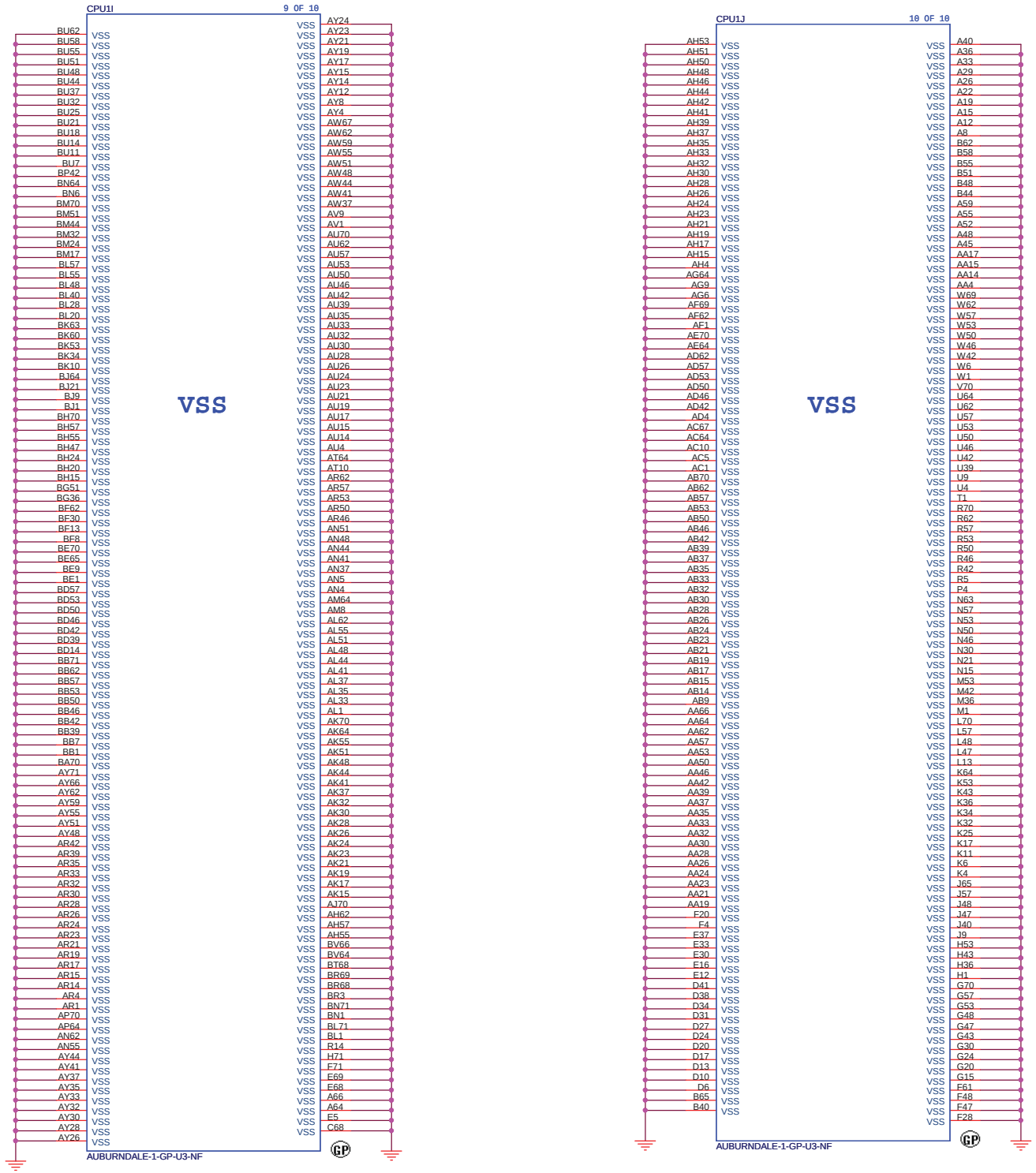

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integrated VccSus1_05,VccSus1_5,VccCL1_5		
INTVRMEN	High=Enable	Low=Disable
integrated VccLan1_05VccCL1_05		
LAN100_SLP	High=Enable	Low=Disable

INTVRMEN- Integrated SUS 1.1V VRM Enable
High - Enable internal VRs

PCH1A 1 OF 10

RTC: RTCX1, RTCX2, RTCRST#, SRTCRST#, INTRUDER#, INTVRMEN
LPC: FWH0/LAD0, FWH1/LAD1, FWH2/LAD2, FWH3/LAD3, FWH4/LFRAME#, LDRQ0#, LDRQ1#/GPIO23, SERIRQ
IHDA: HDA_BCLK, HDA_SYNC, SPKR, HDA_RST#, HDA_SDIN0, HDA_SDIN1, HDA_SDIN2, HDA_SDIN3, HDA_SDO, HDA_DOCK_EN#/GPIO33, HDA_DOCK_RST#/GPIO13
SATA: SATA0RXN/RXP/TXN/TXP, SATA1RXN/RXP/TXN/TXP, SATA2RXN/RXP/TXN/TXP, SATA3RXN/RXP/TXN/TXP, SATA4RXN/RXP/TXN/TXP, SATA5RXN/RXP/TXN/TXP, SATAICOMPO, SATAICOMPI, SATALED#, SATA0GP/GPIO21, SATA1GP/GPIO19
JTAG: JTAG_TCK, JTAG_TMS, JTAG_TDI, JTAG_TDO, TRST#
SPI: SPI_CLK, SPI_CS0#, SPI_CS1#, SPI_MOSI, SPI_MISO

IBEXPEAK-M-GP-NF

HDD

NO REBOOT STRAP

No Reboot Strap R23	
HDA_SPKR	Low = Default High = No Reboot

SA 0709

When unused all JTAG pins may be NC

SPI_MOSI Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor.
Disable iTPM: Left floating, no pull-down required

SPI_CS0#, SPI_MISO, SPI_MOSI, SPI_CLK:
No series resistor required if routing length is 1.5"-6.5"

LAYOUT SWAP

SJM30-CS

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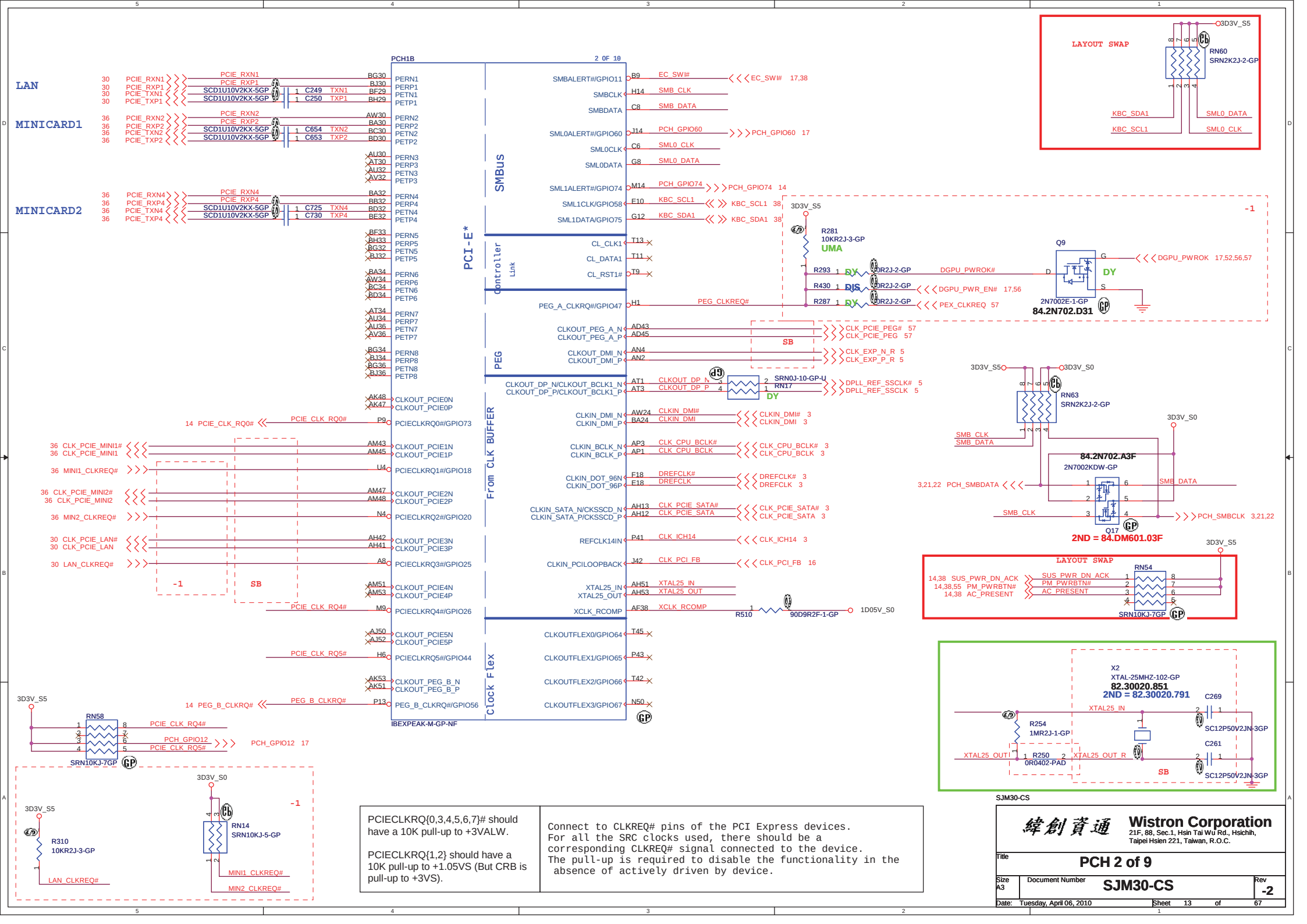

PCIECLKRQ{0,3,4,5,6,7}# should have a 10K pull-up to +3VALW.

PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).

Connect to CLKREQ# pins of the PCI Express devices. For all the SRC clocks used, there should be a corresponding CLKREQ# signal connected to the device. The pull-up is required to disable the functionality in the absence of actively driven by device.

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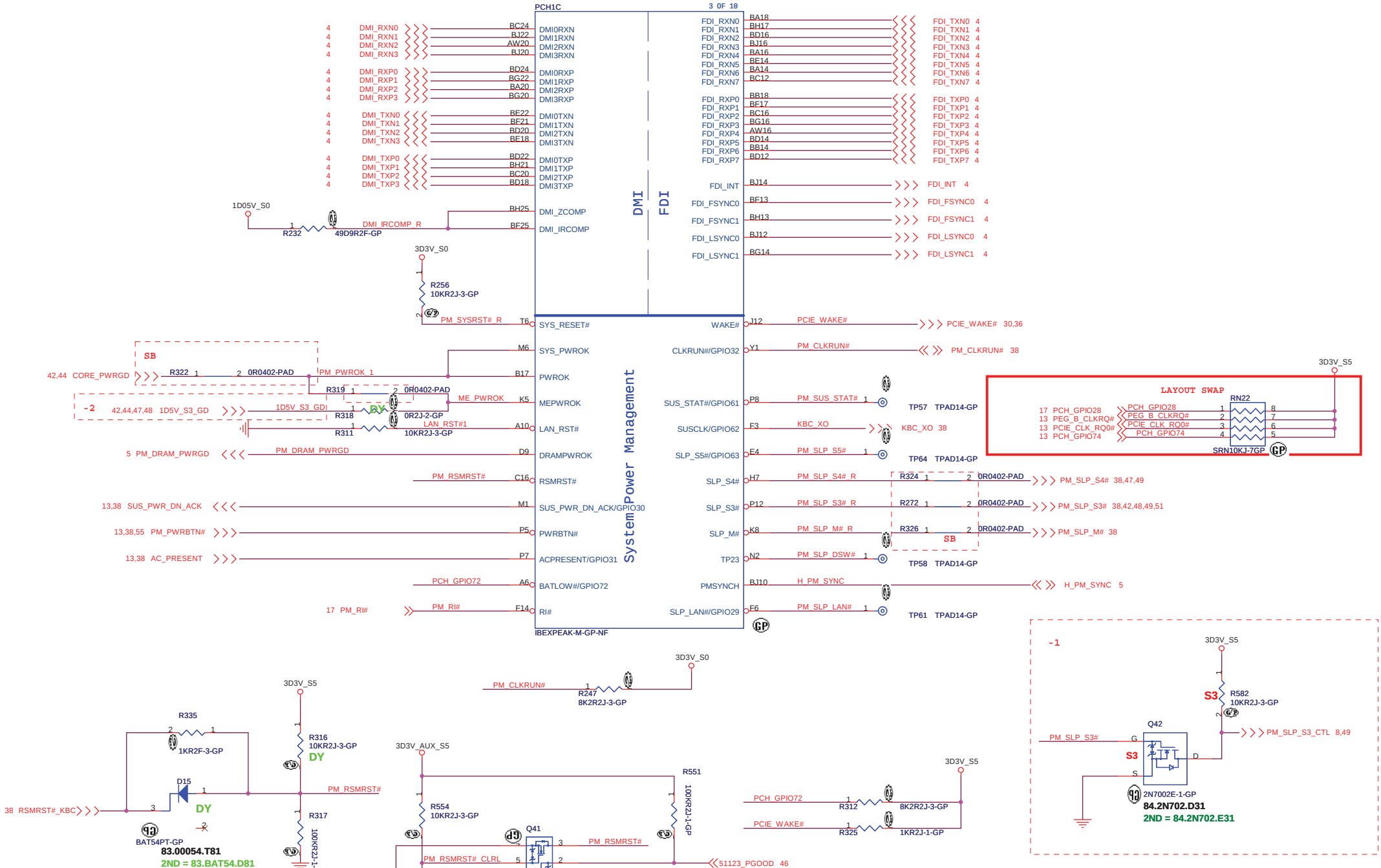

SJM30-CS

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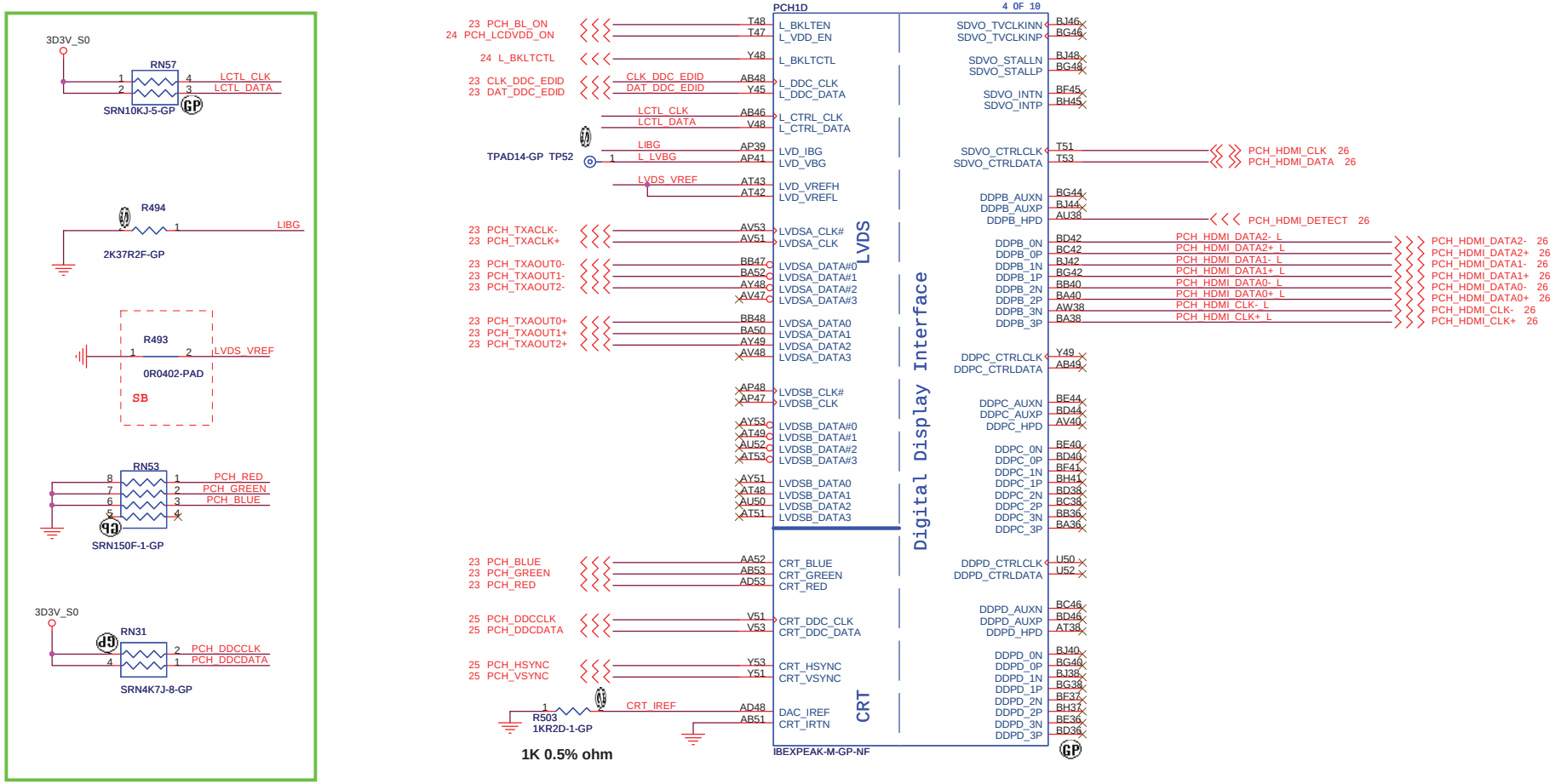

SB 0811

SJM30-CS

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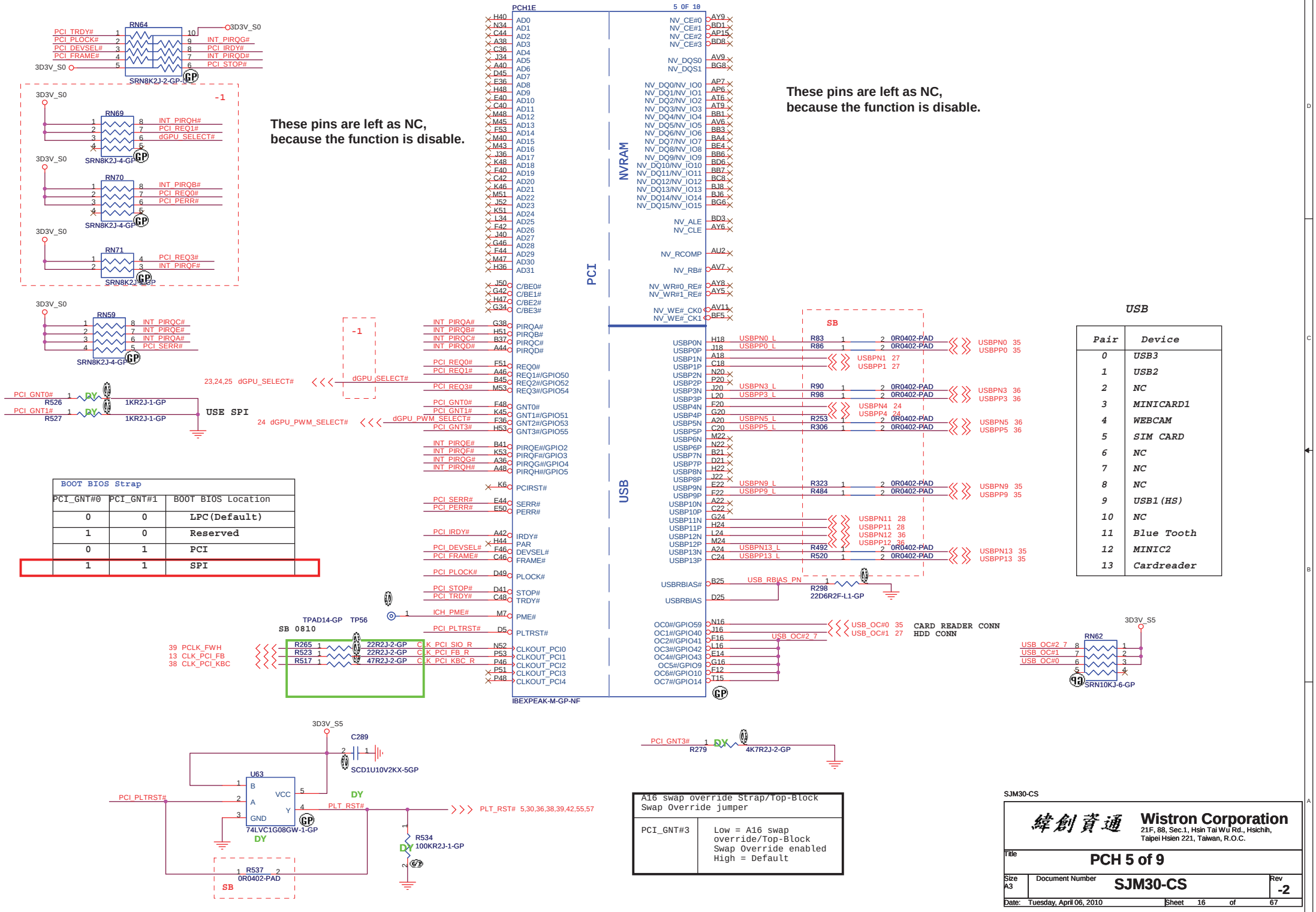

USB	
Pair	Device
0	USB3
1	USB2
2	NC
3	MINICARD1
4	WEBCAM
5	SIM CARD
6	NC
7	NC
8	NC
9	USB1(HS)
10	NC
11	Blue Tooth
12	MINIC2
13	Cardreader

BOOT BIOS Strap		
PCI_GNT#0	PCI_GNT#1	BOOT BIOS Location
0	0	LPC(Default)
1	0	Reserved
0	1	PCI
1	1	SPI

A16 swap override Strap/Top-Block Swap Override jumper	
PCI_GNT#3	Low = A16 swap override/Top-Block Swap Override enabled High = Default

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Title: PCH 5 of 9

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GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.
Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regurator,
should not place external pull down.

PCH1F 6 OF 10

MISC: PCH_GPIO0 Y3 BMBUSY#/GPIO0; 38 EC_SMI# EC_SMI# C38 TACH1/GPIO1; PX_HDMI# D37 TACH2/GPIO6; 38 EC_SCI# EC_SCI# J32 TACH3/GPIO7; FCIM_EN F10 GPIO8; 13 PCH_GPIO12 PCH_GPIO12 K9 LAN_PHY_PWR_CTRL/GPIO12; PCH_GPIO15 T7 GPIO15

GPIO: 57 DGPU_HOLD_RST# DGPU_HOLD_RST# AA2 SATA4GP/GPIO16; 13,52,56,57 DGPU_PWROK DGPU_PWROK F38 TACH0/GPIO17; PCH_GPIO22 Y7 SCLOCK/GPIO22; TPAD14-GP TP60 PCH_GPIO24 H10 GPIO24; TPAD14-GP TP55 PCH_GPIO27 AB12 GPIO27; 14 PCH_GPIO28 PCH_GPIO28 V13 GPIO28; STP_PCI# M11 STP_PCI#/GPIO34; dVRAM_2G_512M_1G# V6 SATACLKREQ#/GPIO35; 13,56 DGPU_PWR_EN# DGPU_PWR_EN# AB7 SATA2GP/GPIO36; dGPU_PRSNT# AB13 SATA3GP/GPIO37; 23,25 dGPU_EDID dGPU_EDID V3 SLOAD/GPIO38; OPTIMUS_SG# P3 SDATAOUT0/GPIO39; PCH_GPIO45 H3 PCIECLKRQ6#/GPIO45; RST_GATE F1 PCIECLKRQ7#/GPIO46; dVRAM_512M_1G# AB6 SDATAOUT1/GPIO48; PSW_CLR# AA4 SATA5GP/GPIO49; UMA_DISCRETE# F8 GPIO57

CPU: CLKOUT_PCIE6N AH45, CLKOUT_PCIE6P AH46; CLKOUT_PCIE7N AF48, CLKOUT_PCIE7P AF47; A20GATE U2 → KA20GATE 38; SB: CLKOUT_BCLK0_N/CLKOUT_PCIE8N AM3 → BCLK_CPU_N 5; CLKOUT_BCLK0_P/CLKOUT_PCIE8P AM1 → BCLK_CPU_P 5; PECI BG10 ↔ H_PECI 5; RCIN# T1 → KBRCIN# 38; PROCPWRGD BE10 → H_PWRGD 5,55; THRMTRIP# BD10 → PCH_THERMTRIP_R → R489 56R2J-4-GP (1D05V_S0) → R491 54D9R2F-L1-GP (DY) → PM_THRMTRIP-A# 5,42

NCTF: VSS_NCTF_8 B4, VSS_NCTF_9 B52, VSS_NCTF_16 BH2, VSS_NCTF_17 BH52, VSS_NCTF_28 D2; VSS_NCTF#A4 A4, VSS_NCTF#A49 A49, VSS_NCTF#A5 A5, VSS_NCTF#A50 A50, VSS_NCTF#A52 A52, VSS_NCTF#A53 A53, VSS_NCTF#B2 B2, VSS_NCTF#B53 B53, VSS_NCTF#BE1 BE1, VSS_NCTF#BE53 BE53, VSS_NCTF#BF1 BF1, VSS_NCTF#BF53 BF53, VSS_NCTF#BH1 BH1, VSS_NCTF#BH53 BH53, VSS_NCTF#BJ1 BJ1, VSS_NCTF#BJ2 BJ2, VSS_NCTF#BJ4 BJ4, VSS_NCTF#BJ49 BJ49, VSS_NCTF#BJ5 BJ5, VSS_NCTF#BJ50 BJ50, VSS_NCTF#BJ52 BJ52, VSS_NCTF#BJ53 BJ53, VSS_NCTF#D1 D1, VSS_NCTF#D53 D53, VSS_NCTF#E1 E1, VSS_NCTF#E53 E53

NCTF TEST PIN: A4,A49,A5,A50,A52,A53,B2,B53,BE1, BE53,BF1,BF53,BH1,BH53,BJ1,BJ2,BJ4, BJ49,BJ5,BJ50,BJ52,BJ53,D1,D53,E1,E53

RSVD: TP1 BA22, TP2 AW22, TP3 BB22, TP4 AY45, TP5 AY46, TP6 AV43, TP7 AV45, TP8 AF13, TP9 M18, TP10 N18, TP11 AJ24, TP12 AK41, TP13 AK42, TP14 M32, TP15 N32, TP16 M30, TP17 N30, TP18 H12, TP19 AA23, NC_1 AB45, NC_2 AB38, NC_3 AB42, NC_4 AB41, NC_5 T39, INIT3_3V# P6, TP24 C10

IBEXPEAK-M-GP-NF

Placed Within 2" from PCH

SB
3D3V_S0 — 512MB_UMA — R566 10KR2J-3-GP — GPIO48 — dVRAM_512M_1G# — R565 10KR2J-3-GP — 1GB
VGA RAM
H: 512M Byte
L: 1G Byte

3D3V_S0 — 2Gb — R571 10KR2J-3-GP — GPIO35 — dVRAM_2G_512M_1G# — R570 10KR2J-3-GP — Non_2Gb_UMA
VGA RAM
H: 2G Byte
L: 512M/1G Byte

-1
1D5V_S3 — R586 1KR2F-3-GP (S3) → DDR3_DRAMRST# 21,22
0121 -1
NON_S3 — R587 0R2J-2-GP
2ND = 84.2N702.E31
84.2N702.D31
2N7002E-1-GP
Q43
3D3V_S5 — R584 10KR2F-2-GP (S3) → RST_GATE
S3: C448 SCD047U25V2KX-GP
S3: R585 100KR2F-L1-GP → SM_DRAMRST# 5

SB
-1
3D3V_S5 — UMA_Optimas — R320 10KR2J-3-GP — GPIO57 — UMA_DISCRETE# — R535 10KR2J-3-GP — DY_SG_DIS
3D3V_S0 — 1GPU_UMA — R507 10KR2J-3-GP — GPIO37 — dGPU_PRSNT# — R505 10KR2J-3-GP — 2GPU_DIS
3D3V_S0 — Non_Ventura — R516 10KR2J-3-GP — GPIO39 — OPTIMUS_SG# — R519 10KR2J-3-GP — Ventura_support

UMA(H)_DISCRETE(L)# if GPI 37 H
Optimus(H)_SG(L)# if GPI37 L
POST with two GPUs#
H: one GPU
L: two GPUs
Ventura_Support#
H: non-support
L: support

SB
DGPU_HOLD_RST# — R245 10KR2J-3-GP
DGPU_PWR_EN# — 10KR2J-3-GP — R504

3D3V_S5
LAYOUT SWAP: RN61 SRN10KJ-7GP — 14 PM_RI# PM_RI#; 13,38 EC_SW# EC_SW#; 13 PCH_GPIO60 PCH_GPIO60
SB 0819: PCH_GPIO45 — R285 8K2R2J-3-GP
PCH_GPIO15 — R251 1KR2J-1-GP
R531 FCIM_EN 1KR2J-1-GP (DY)

PSW_CLR# — GAP-OPEN — G127

3D3V_S0
LAYOUT SWAP: RN51 SRN10KJ-7GP — 12,38 INT_SERIRQ INT_SERIRQ; PSW_CLR#

RP1 SRN10KJ-L3-GP: PCH_GPIO0, EC_SMI#, dGPU_EDID, EC_SCI# → 3D3V_S0; PCH_GPIO22, STP_PCI#, PX_HDMI#

SB 0722
AFTE14P-GP TP40 PCH_TP95; AFTE14P-GP TP41 PCH_TP96; AFTE14P-GP TP30 PCH_TP97; AFTE14P-GP TP29 PCH_TP98

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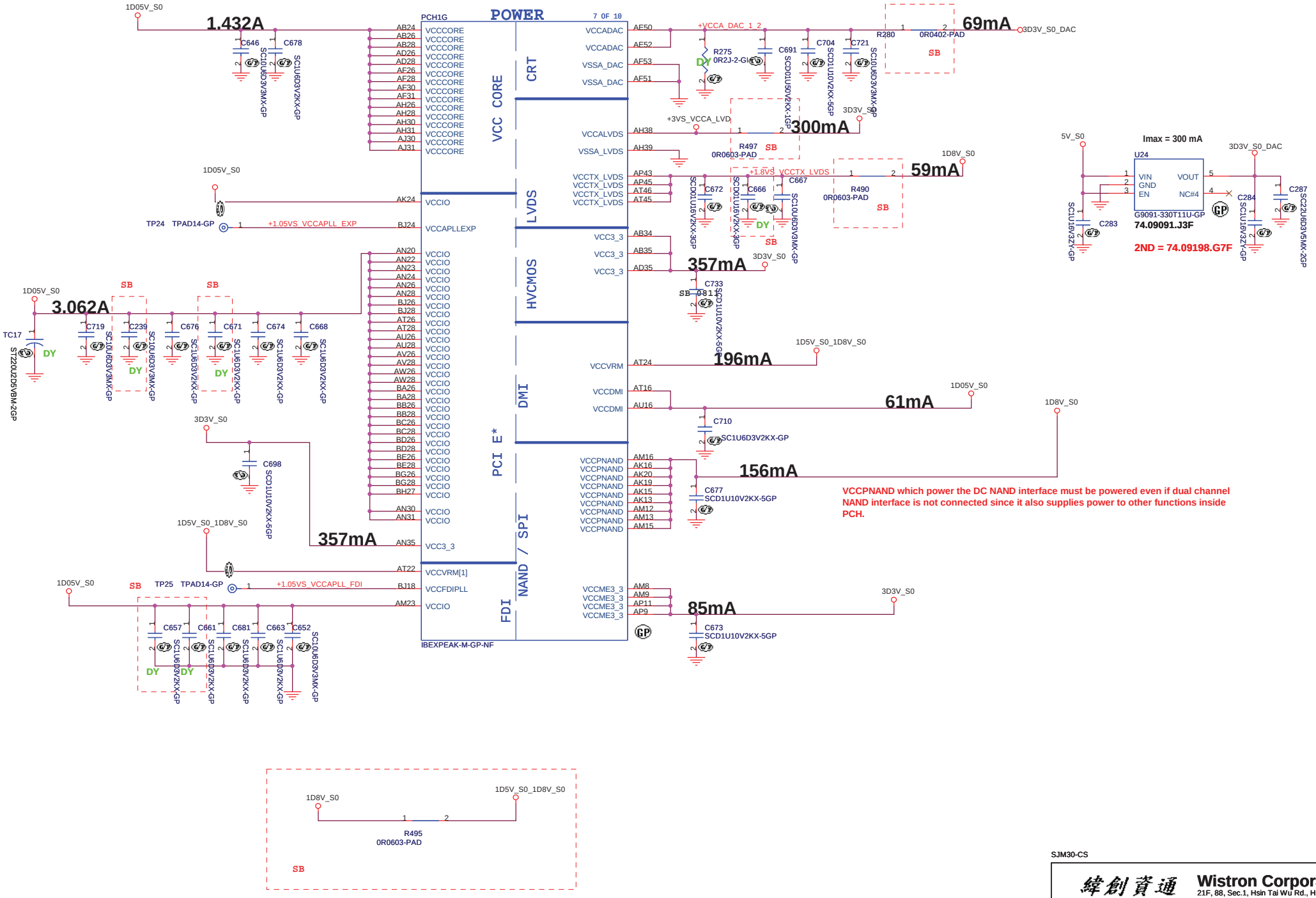
Title: PCH 6 of 9
Size: Custom | Document Number: SJM30-CS | Rev: -2
Date: Tuesday, April 06, 2010 | Sheet 17 of 67



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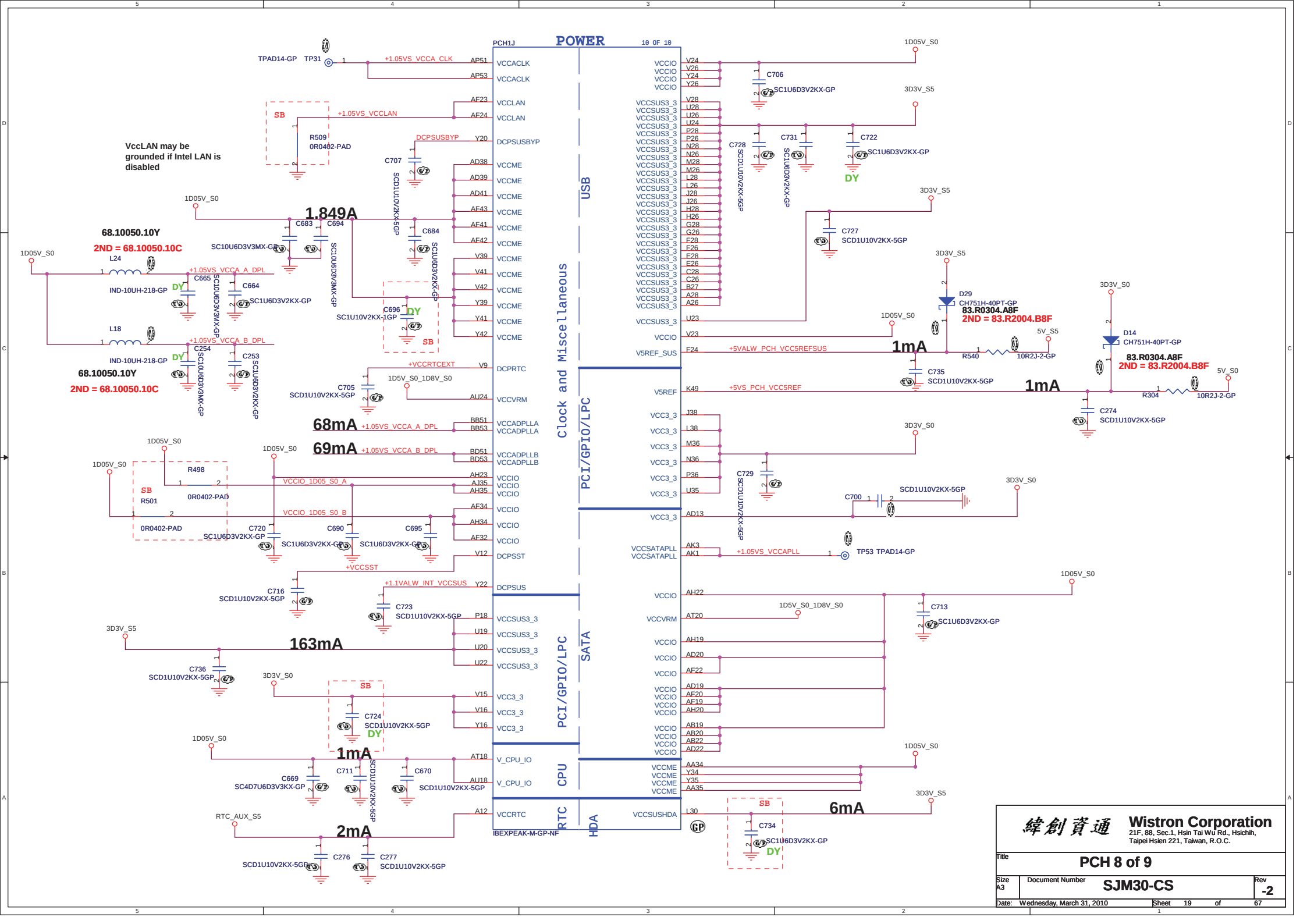
Title	PCH 7 of 9	
Size A3	Document Number SJM30-CS	Rev -2
Date: Wednesday, March 31, 2010	Sheet 18 of 67	


POWER
PCH1J
10 OF 10
Clock and Miscellaneous
USB
PCI/GPIO/LPC
SATA
CPU
RTC
HDA
IBEXPEAK-M-GP-NF
VccLAN may be grounded if Intel LAN is disabled
1.849A
68.10050.10Y
2ND = 68.10050.10C
68mA
69mA
163mA
1mA
2mA
6mA
83.R0304.A8F
2ND = 83.R2004.B8F
TPAD14-GP TP31
+1.05VS_VCCA_CLK
+1.05VS_VCCLAN
DCPSUSBYP
+1.05VS_VCCA_A_DPL
+1.05VS_VCCA_B_DPL
+VCCRTCEXT
1D05V_S0_1D8V_S0
VCCIO_1D05_S0_A
VCCIO_1D05_S0_B
+VCCSST
+1.1VALW_INT_VCCSUS
+5VALW_PCH_VCC5REFSUS
+5VS_PCH_VCC5REF
+1.05VS_VCCAPLL
RTC_AUX_S5
R509 0R0402-PAD
R498 0R0402-PAD
R501 0R0402-PAD
R540 10R2J-2-GP
R304 10R2J-2-GP
D29 CH751H-40PT-GP
D14 CH751H-40PT-GP
TP53 TPAD14-GP
SC10U6D3V3MX-GP
SC1U10V2KX-1GP
SC1U6D3V2KX-GP
SCD1U10V2KX-5GP
SC4D7U6D3V3KX-GP
IND-10UH-218-GP
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Title
PCH 8 of 9
Size A3
Document Number SJM30-CS
Rev -2
Date: Wednesday, March 31, 2010
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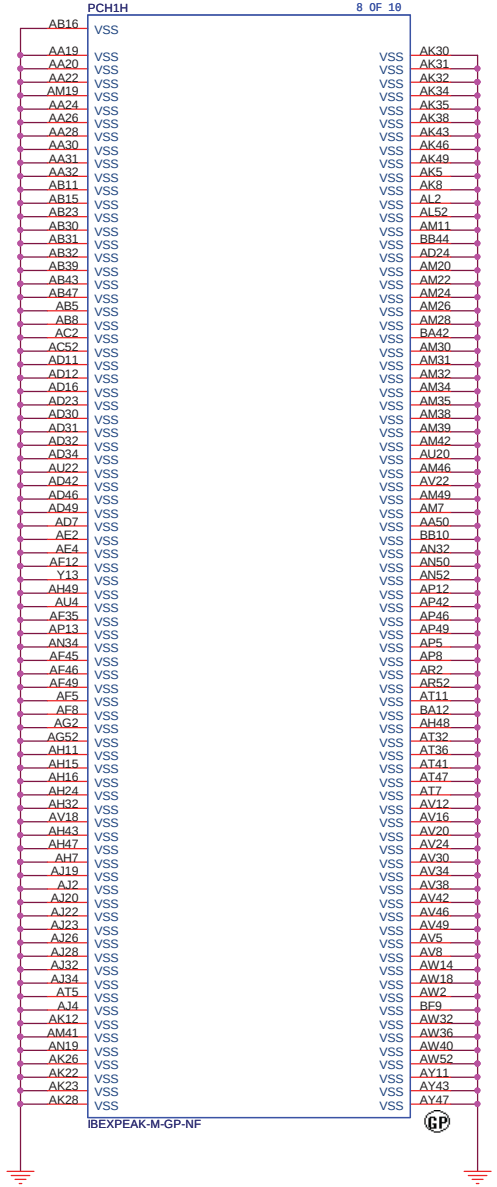

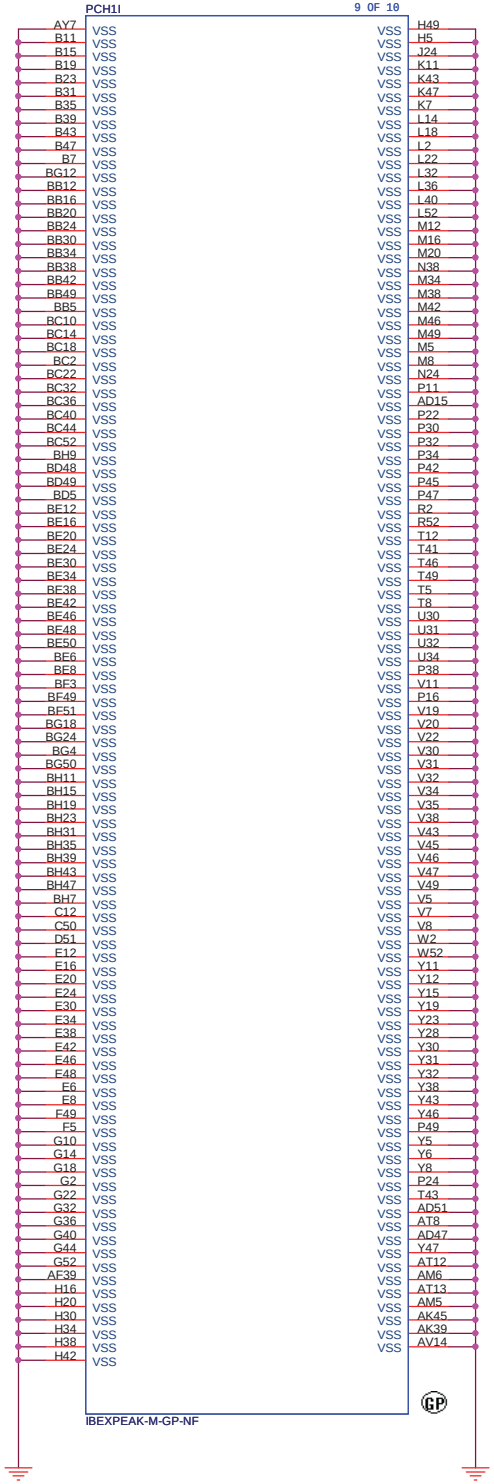

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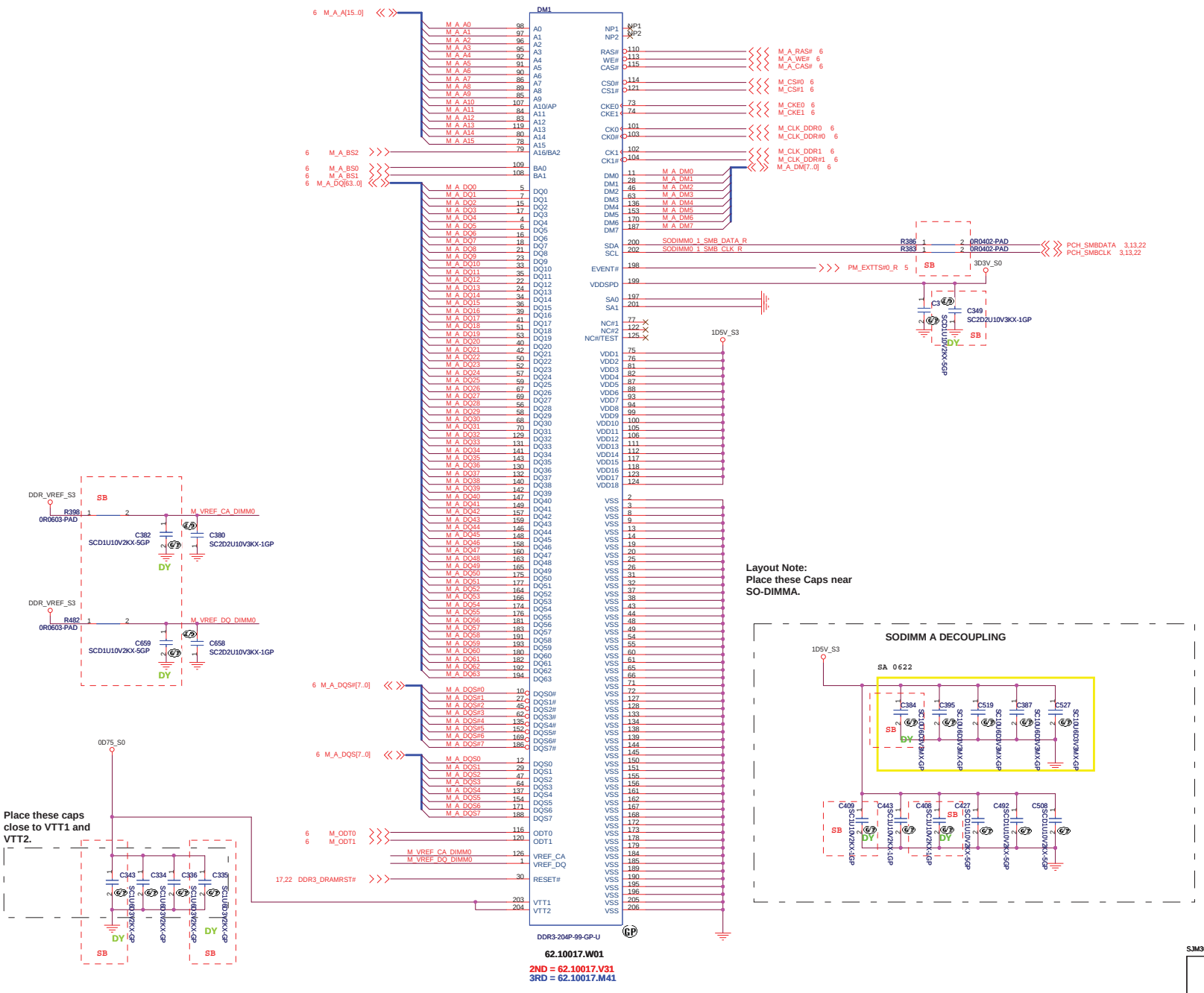
Title: **PCH 9 of 9**

Size	Document Number	Rev
A3	SJM30-CS	-2

Date: Wednesday, March 31, 2010 Sheet 20 of 67



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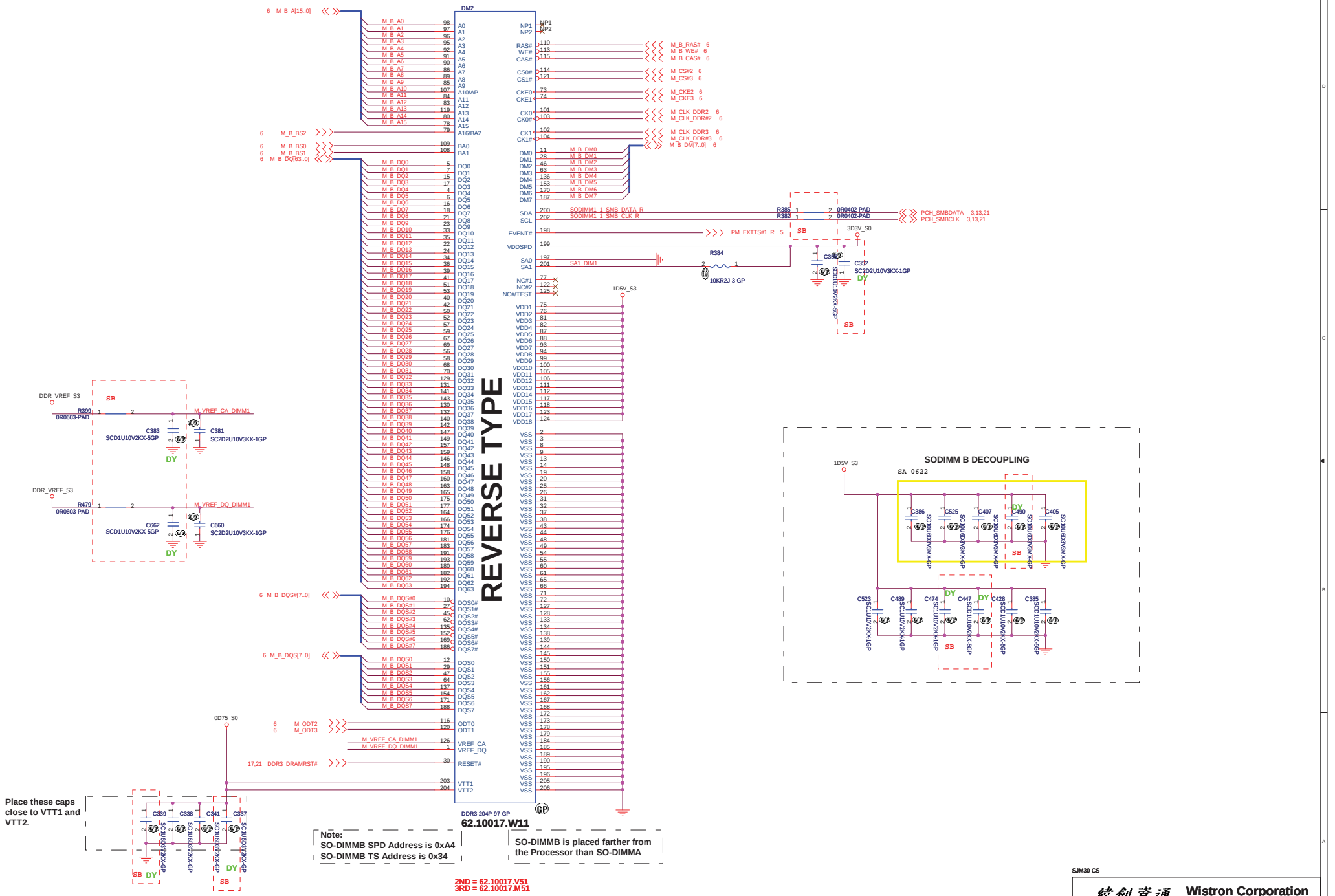
Title	DDR3 SODIMM1	
Size: C	Document Number: SJM30-CS	Rev: -2
Date: Tuesday, April 06, 2010	Sheet 21 of 67	



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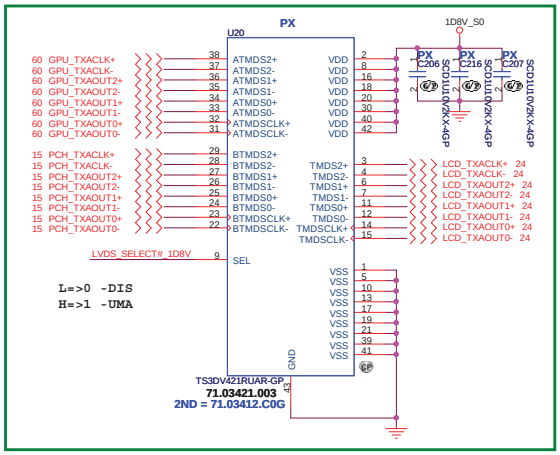
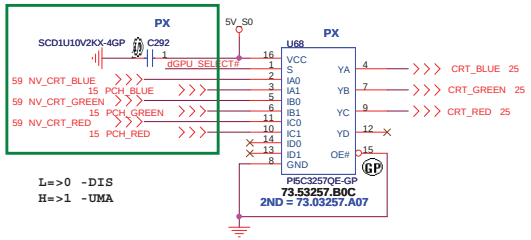
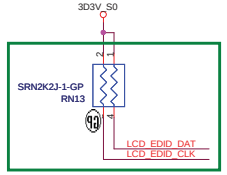
Title: DDR3 SODIMM2

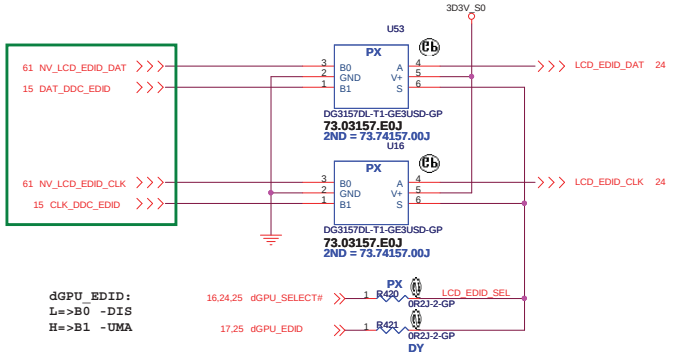
Size	Document Number	Rev
C	SJM30-CS	-2

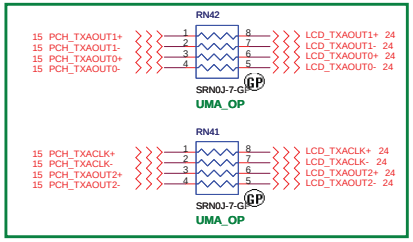
Date: Tuesday, April 06, 2010 Sheet 22 of 67

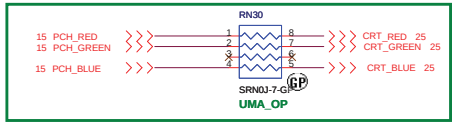


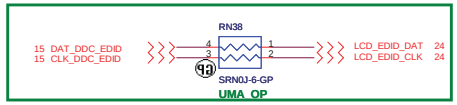


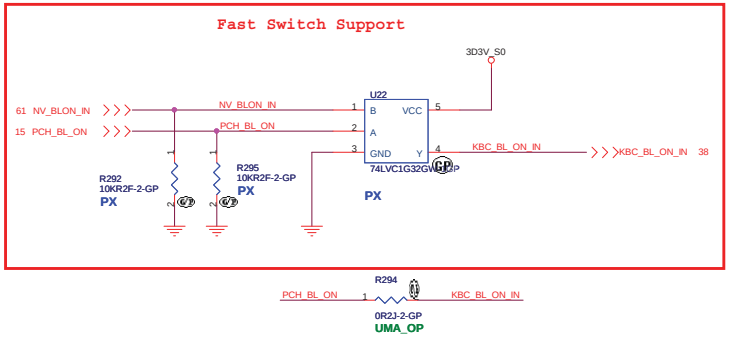


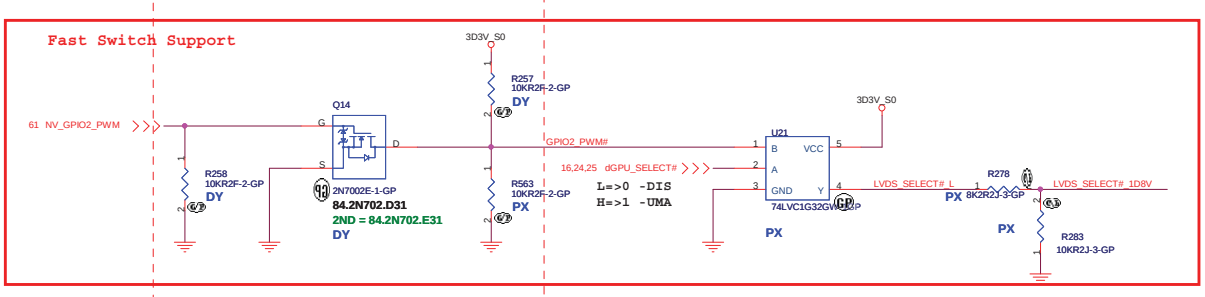












LVDS

FUNCTION TABLE

SEL	FUNCTION	OUTPUT
L	TMDSn+ = ATMDSn+ TMDSn- = ATMDSn- TMDSCLK+ = ATMDSCLK+ TMDSCLK- = ATMDSCLK- BTMDSn+ = High Impedance BTMDSn- = High Impedance BTMDSCLK+ = High Impedance BTMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-
H	TMDSn+ = BTMDSn+ TMDSn- = BTMDSn- TMDSCLK+ = BTMDSCLK+ TMDSCLK- = BTMDSCLK- ATMDSn+ = High Impedance ATMDSn- = High Impedance ATMDSCLK+ = High Impedance ATMDSCLK- = High Impedance	TMDSn+ TMDSn- TMDSCLK+ TMDSCLK-

CRT

$\overline{E}$	S	YA	YB	YC	YD	Function
H	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
L	L	IA0	IB0	IC0	ID0	S = 0
L	H	IA1	IB1	IC1	ID1	S = 1

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Title: PX SWITCH

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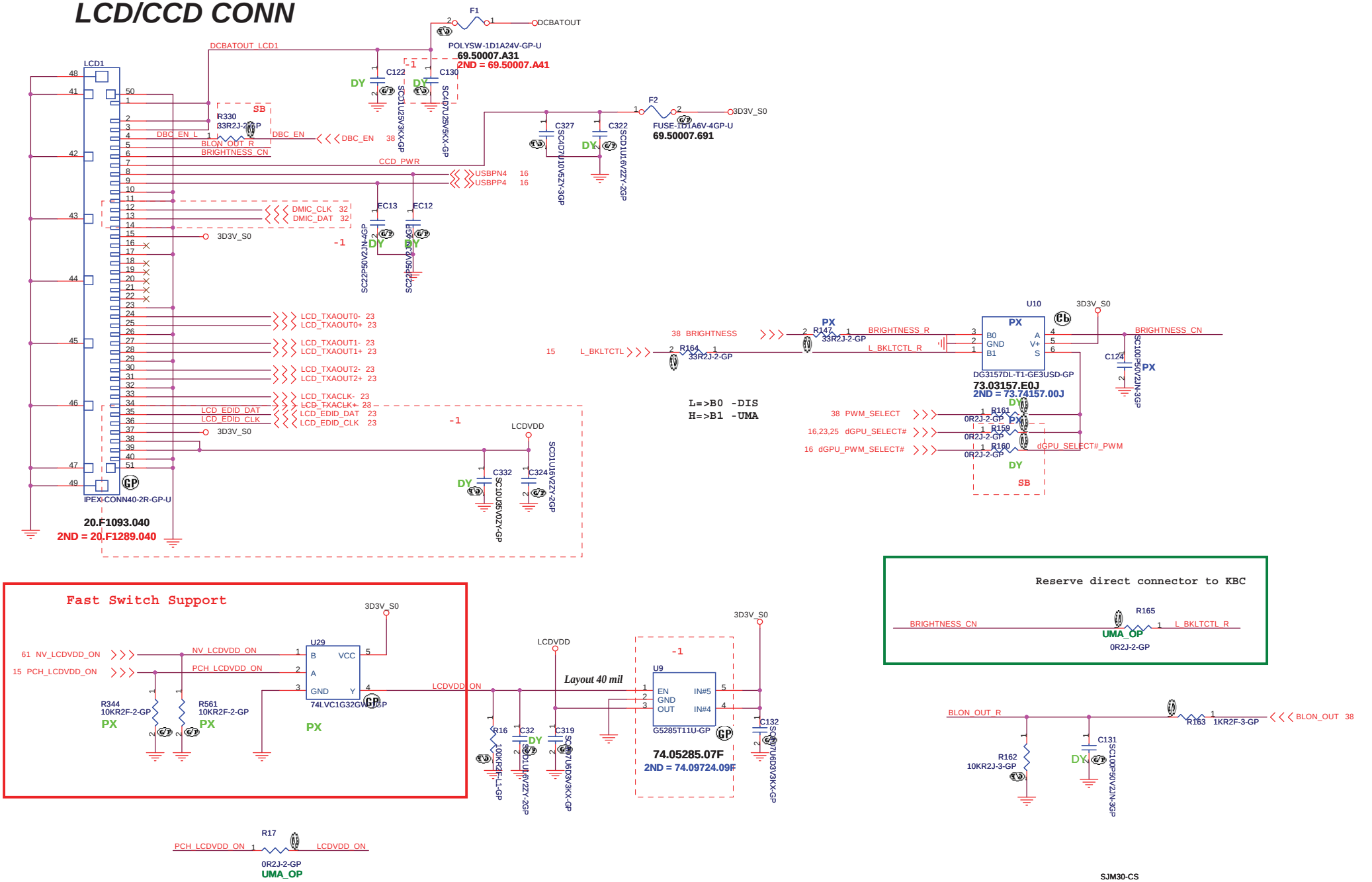
LCD/CCD CONN



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Title	LCD Conn	
Size A3	Document Number SJM30-CS	Rev -2
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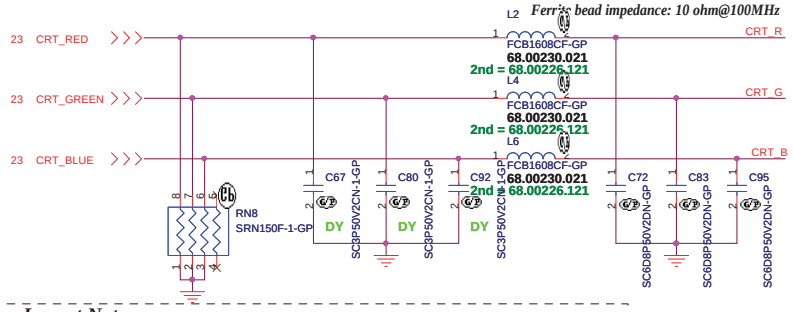
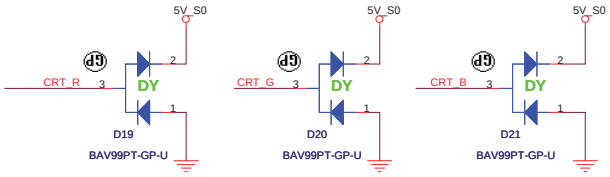
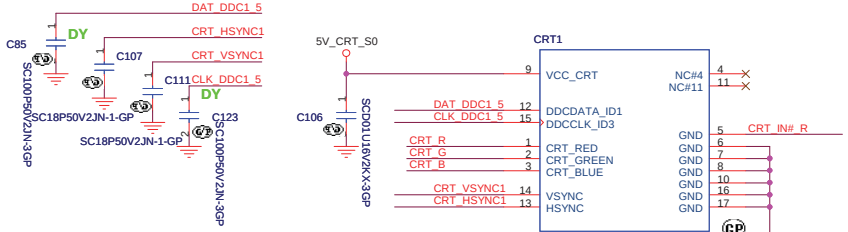
Layout Note:
Place these resistors close to the CRT-out connector

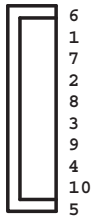


Layout Note:
**** Must be a ground return path between this ground and the ground on the VGA connector.***
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

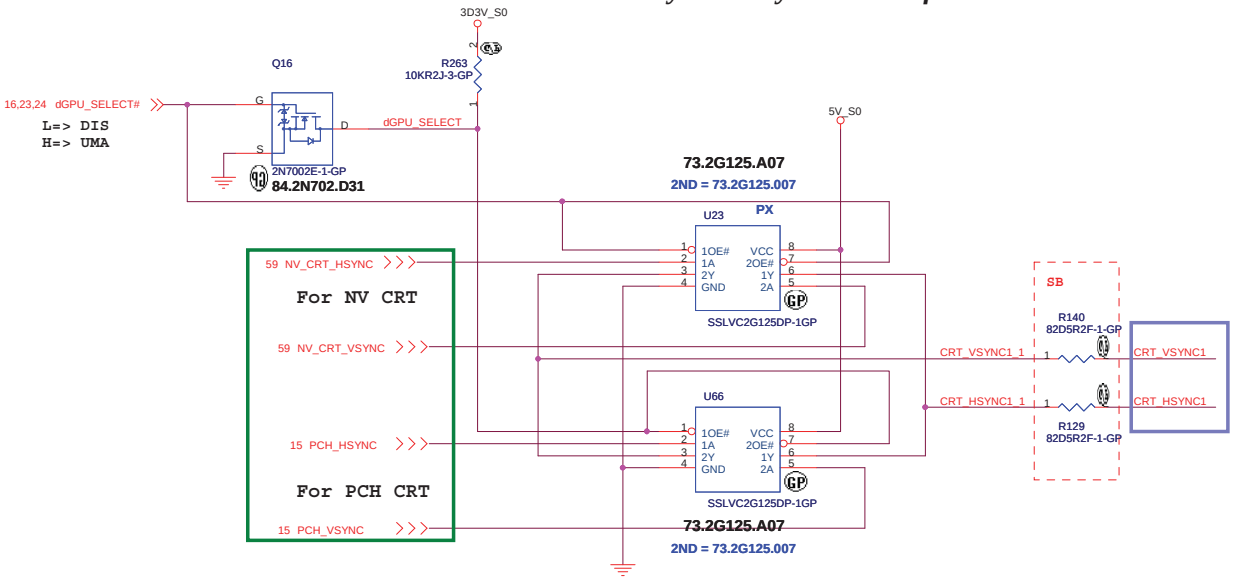


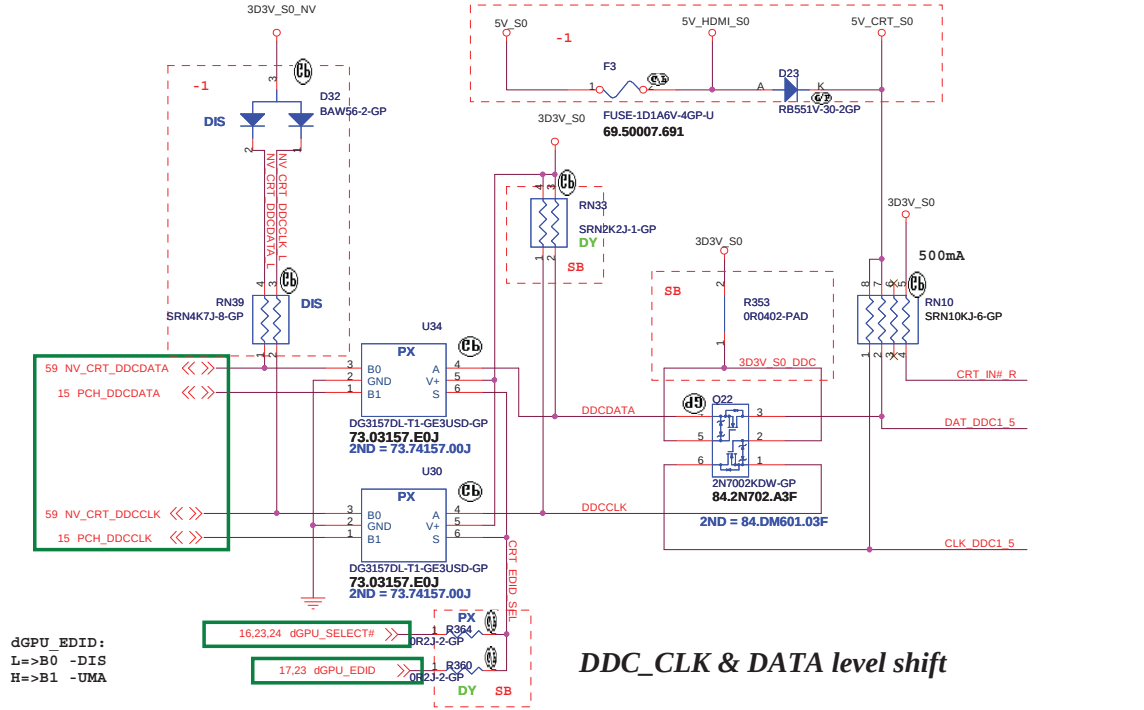
CRT I/F & CONNECTOR





Hsync & Vsync level shift





DDC_CLK & DATA level shift

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Title	CRT conn	
Size: Custom	Document Number: SJM30-CS	Rev: -2
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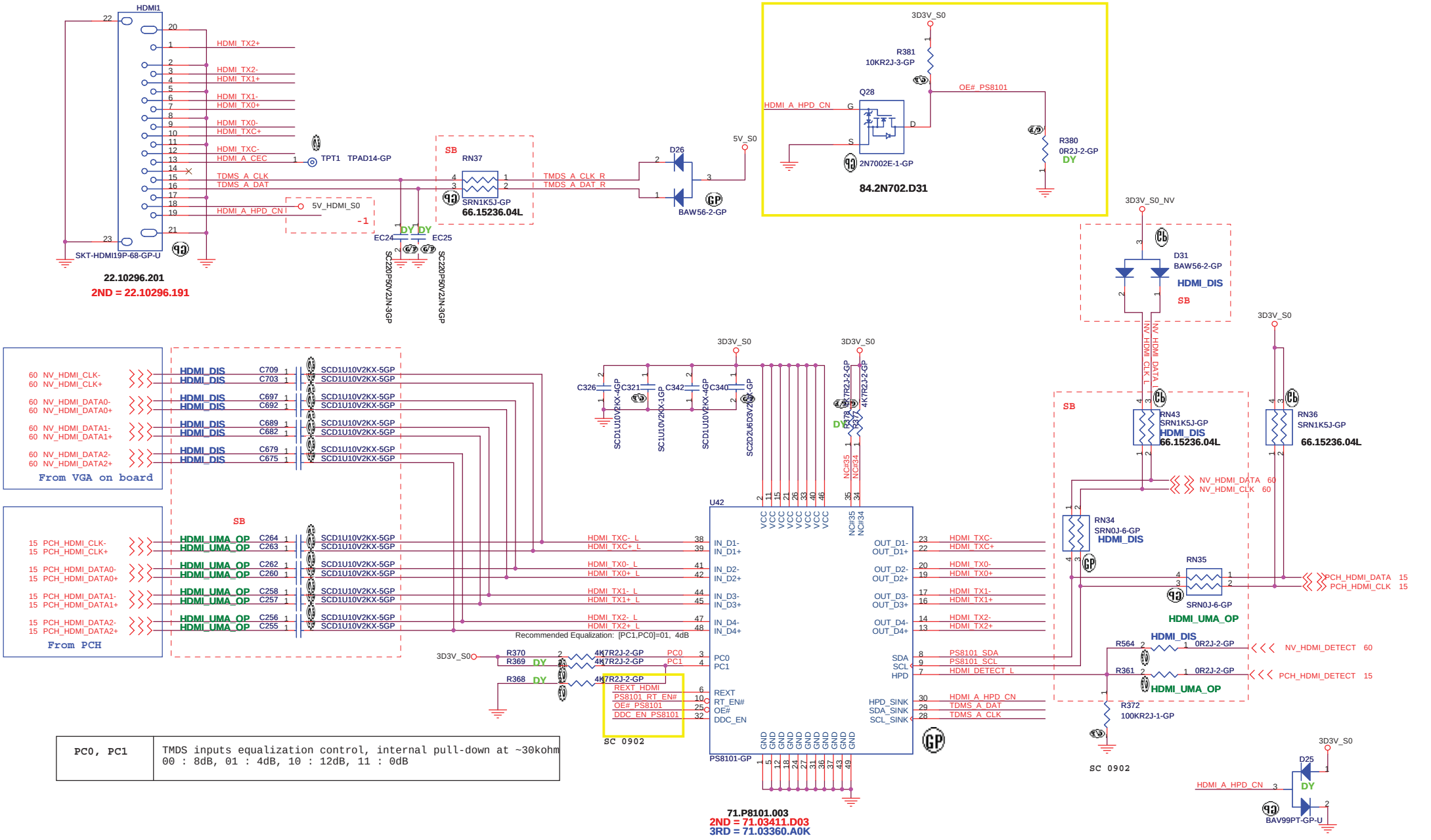

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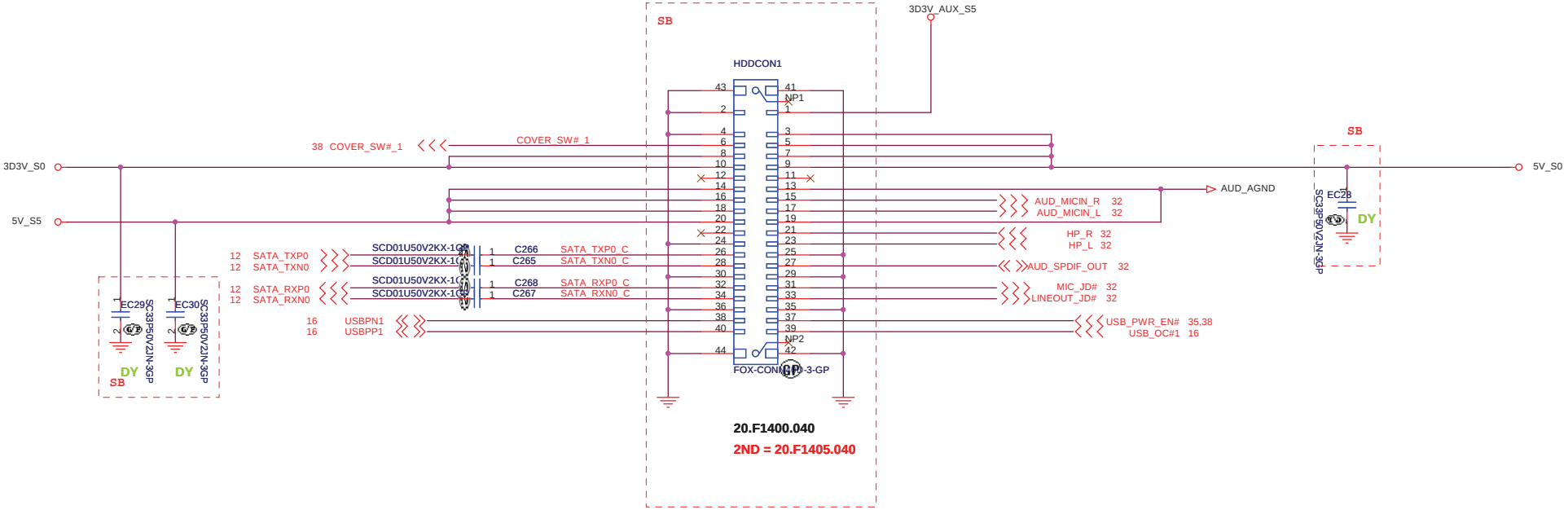
Title	PS8271 / HDMI conn	
Size A3	Document Number SJM30-CS	Rev -2
Date: Tuesday, April 06, 2010	Sheet 26 of 67	



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Title: HDDBD CONN		
Size: A3	Document Number: SJM30-CS	Rev: -2
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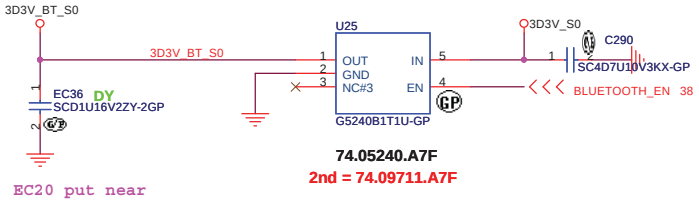
BLUETOOTH MODULE

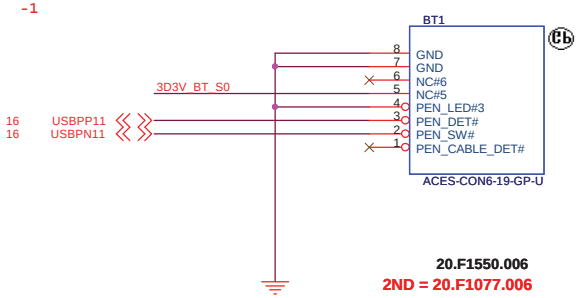


74.05240.A7F

2nd = 74.09711.A7F

EC20 put near
BLUE1 / all
USB put one
choke near
connector by
EMI request

-1



20.F1550.006

2ND = 20.F1077.006

Edit Part for PIN 6 to NC

SJM30-CS

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Taipei Hsien 221, Taiwan, R.O.C.

Title: BlueTooth		
Size: A3	Document Number: SJM30-CS	Rev: -2
Date: Tuesday, April 06, 2010	Sheet 28 of 67	

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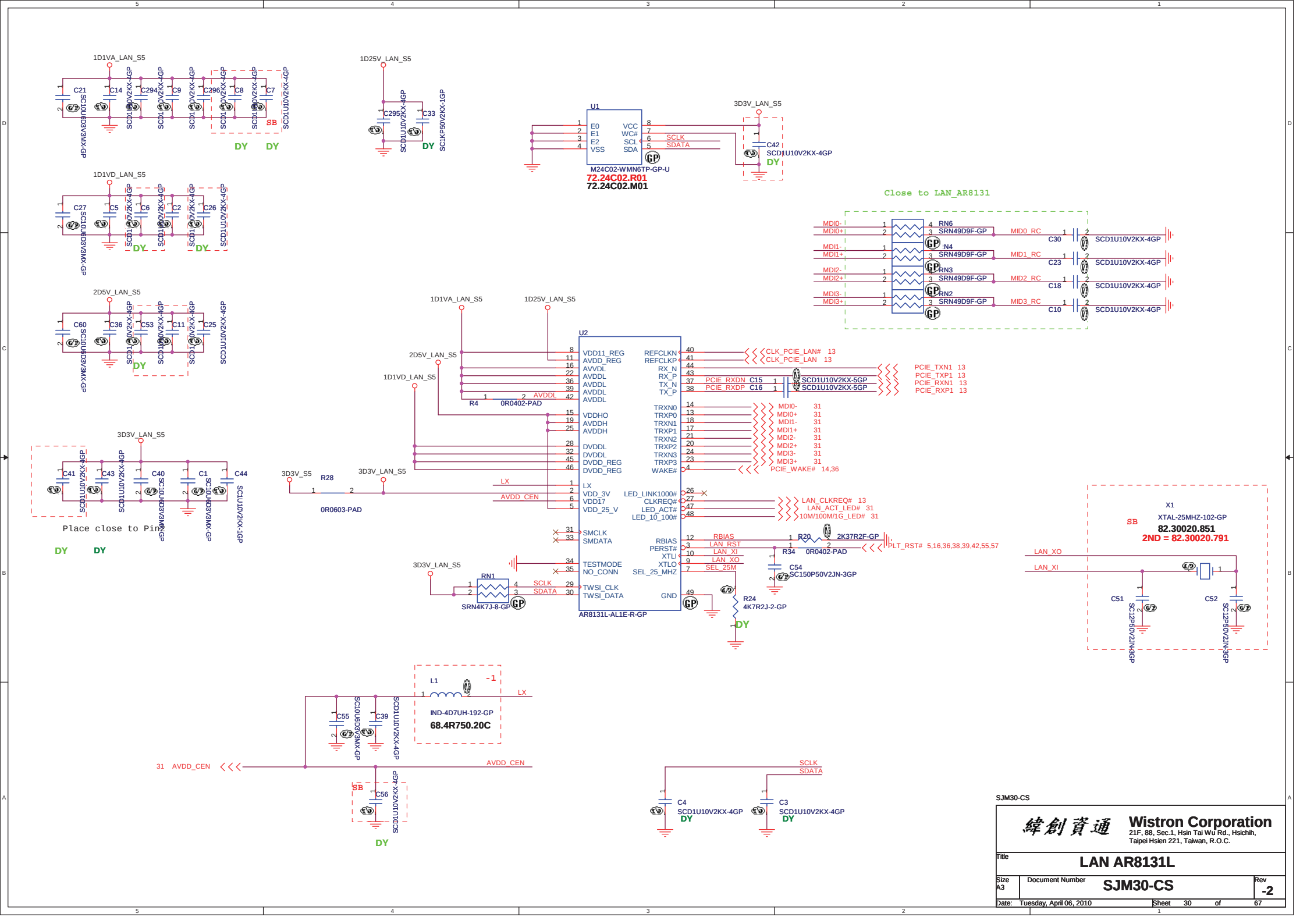
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	**Reserver**	
Size A3	Document Number **SJM30-CS**	Rev **-2**
Date: Wednesday, March 31, 2010	Sheet 29 of 67	


1D1VA_LAN_S5
1D25V_LAN_S5
3D3V_LAN_S5
1D1VD_LAN_S5
2D5V_LAN_S5
Close to LAN_AR8131
Place close to Pin
U1
M24C02-WMN6TP-GP-U
72.24C02.R01
72.24C02.M01
U2
AR8131L-AL1E-R-GP
X1
XTAL-25MHZ-102-GP
82.30020.851
2ND = 82.30020.791
IND-4D7UH-192-GP
68.4R750.20C
SRN4K7J-8-GP
0R0603-PAD
0R0402-PAD
SRN49D9F-GP
SCD1U10V2KX-4GP
SCD1U10V2KX-5GP
SC150P50V2JN-3GP
SC12P50V2JN-3GP
2K37R2F-GP
4K7R2J-2-GP
SJM30-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LAN AR8131L
Size A3
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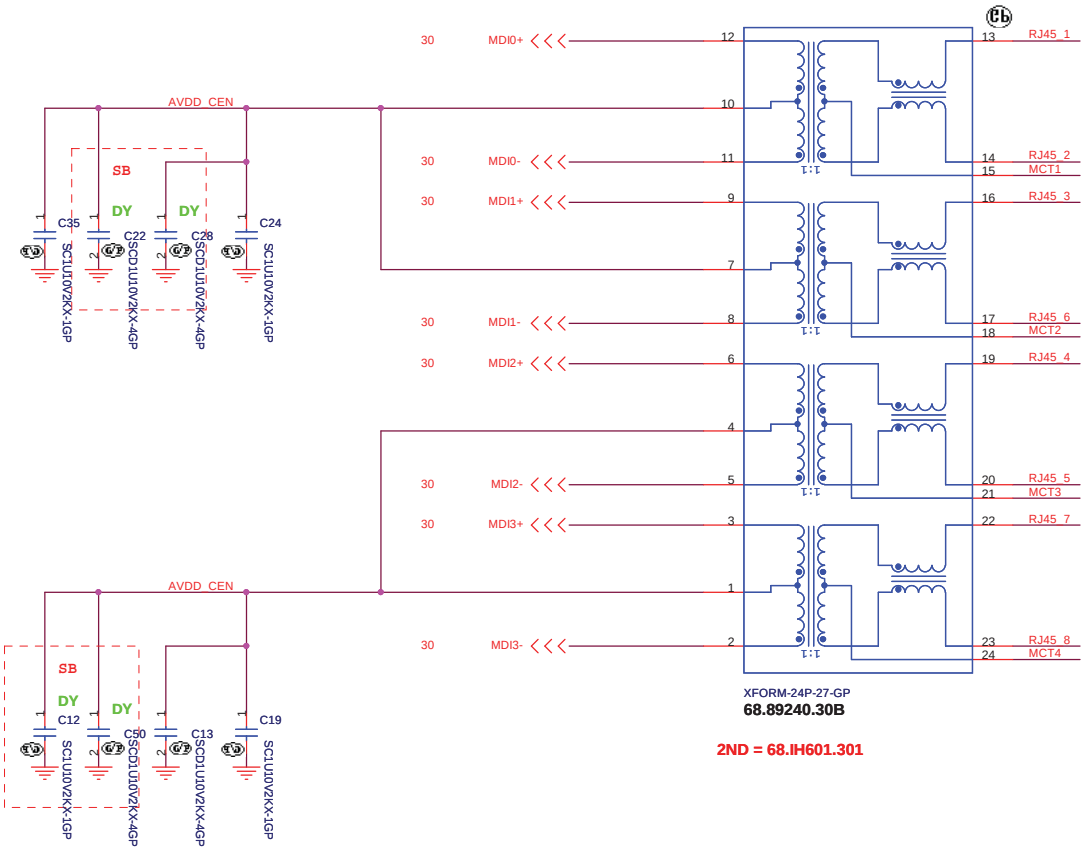
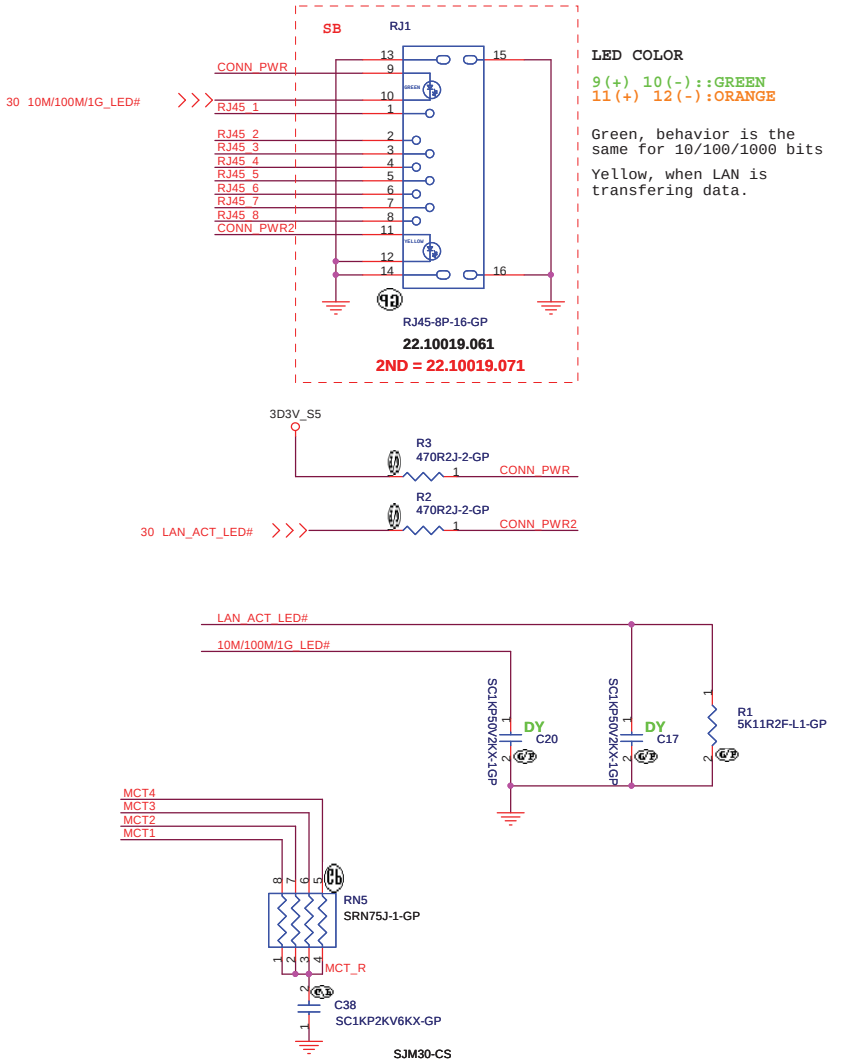
Date: Tuesday, April 06, 2010
Sheet 30 of 67

1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except
RJ-45 moat.

GIGA Lan Transformer



LAN Connector



30 AVDD_CEN >>> AVDD_CEN

SJM30-CS

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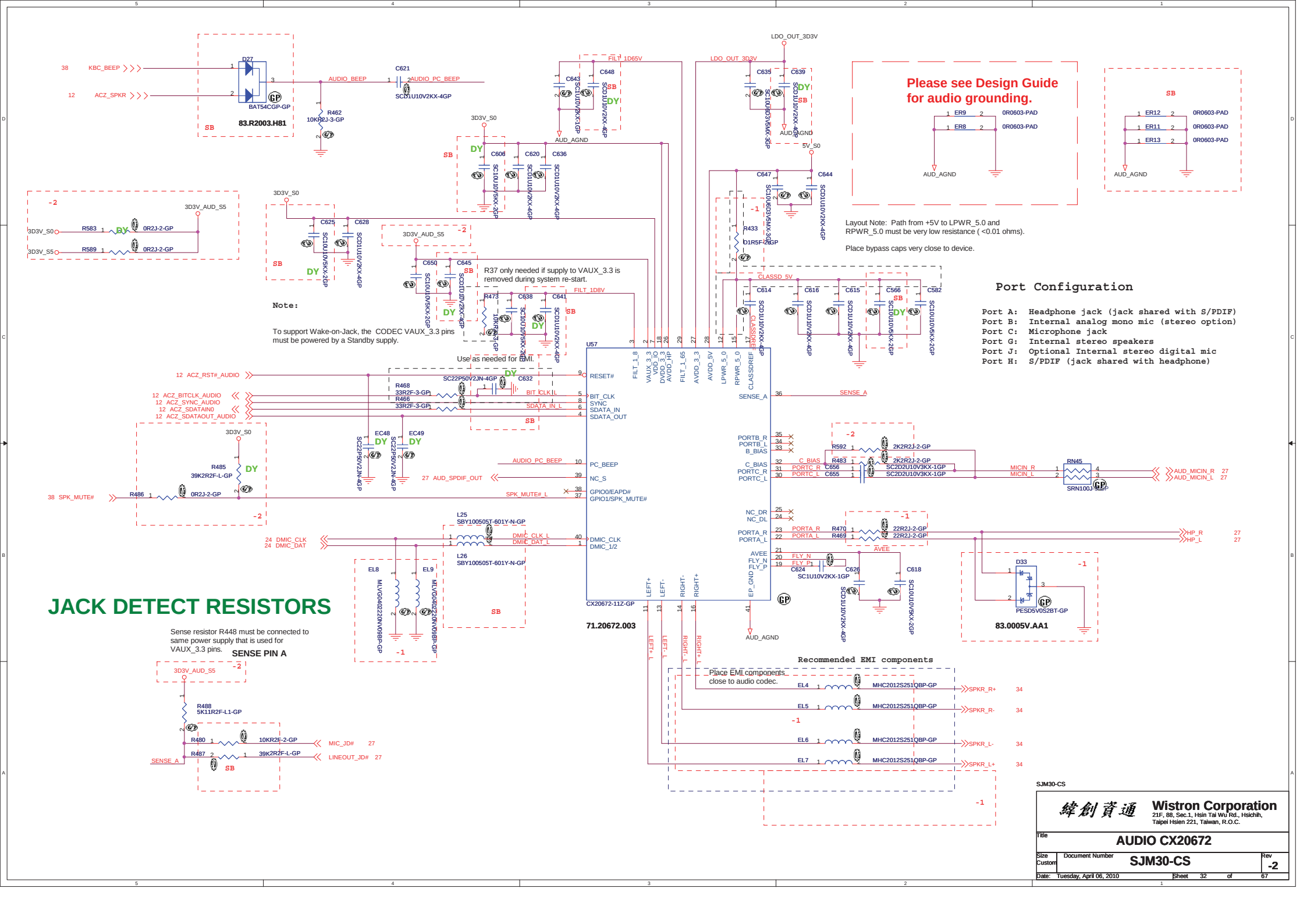
Title: LAN Conn		
Size: A3	Document Number: SJM30-CS	Rev: -2
Date: Tuesday, April 06, 2010	Sheet 31 of 67	


Please see Design Guide for audio grounding.
Layout Note: Path from +5V to LPWR_5.0 and RPWR_5.0 must be very low resistance (<0.01 ohms).
Place bypass caps very close to device.
Port Configuration
Port A: Headphone jack (jack shared with S/PDIF)
Port B: Internal analog mono mic (stereo option)
Port C: Microphone jack
Port G: Internal stereo speakers
Port J: Optional Internal stereo digital mic
Port H: S/PDIF (jack shared with headphone)
Note:
To support Wake-on-Jack, the CODEC VAUX_3.3 pins must be powered by a Standby supply.
R37 only needed if supply to VAUX_3.3 is removed during system re-start.
Use as needed for EMI.
JACK DETECT RESISTORS
Sense resistor R448 must be connected to same power supply that is used for VAUX_3.3 pins.
SENSE PIN A
Recommended EMI components
Place EMI components close to audio codec.
CX20672-11Z-GP
71.20672.003
83.R2003.H81
83.0005V.AA1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
AUDIO CX20672
SJM30-CS
Rev -2
Date: Tuesday, April 06, 2010
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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: **RESERVER**

Size	Document Number	Rev
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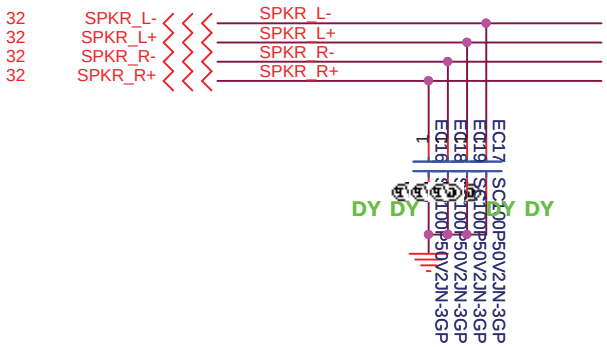
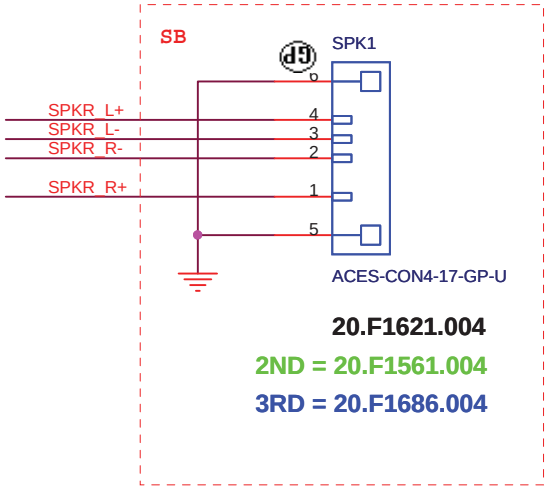
Internal Speaker





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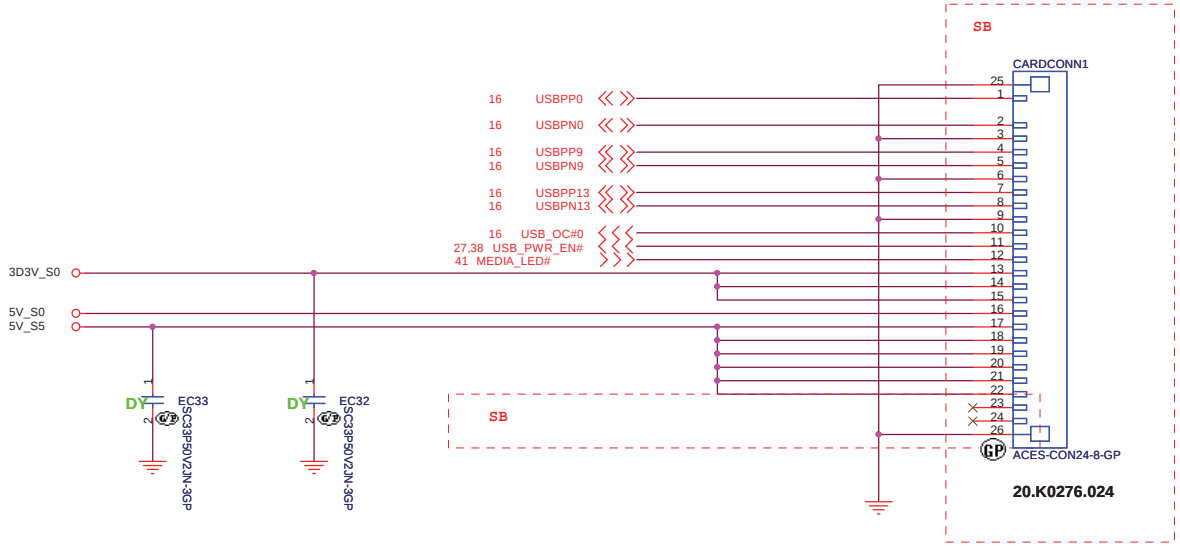
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AUDIO SPKR CONN	
Size A4	Document Number SJM30-CS	Rev -2
Date: Tuesday, April 06, 2010	Sheet 34 of 67	



SJM30-CS

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: CARDREADER BD CONN		
Size: A3	Document Number: SJM30-CS	Rev: -2
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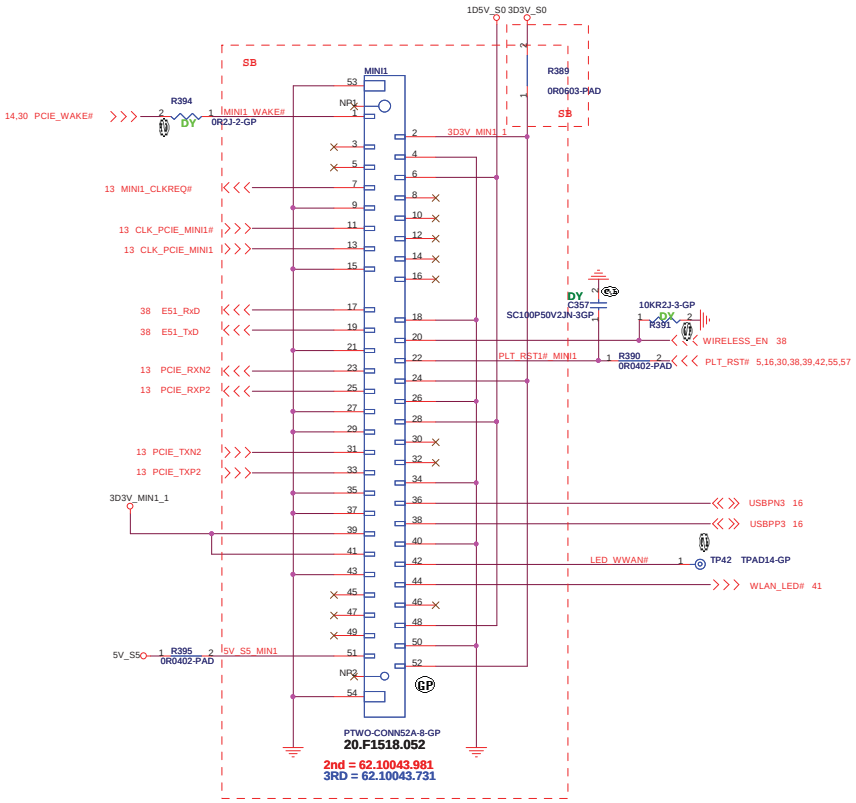
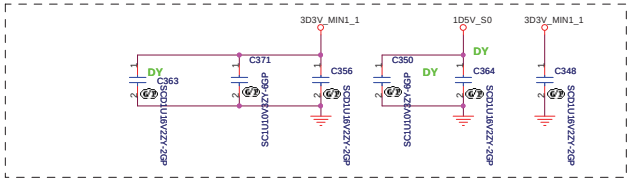
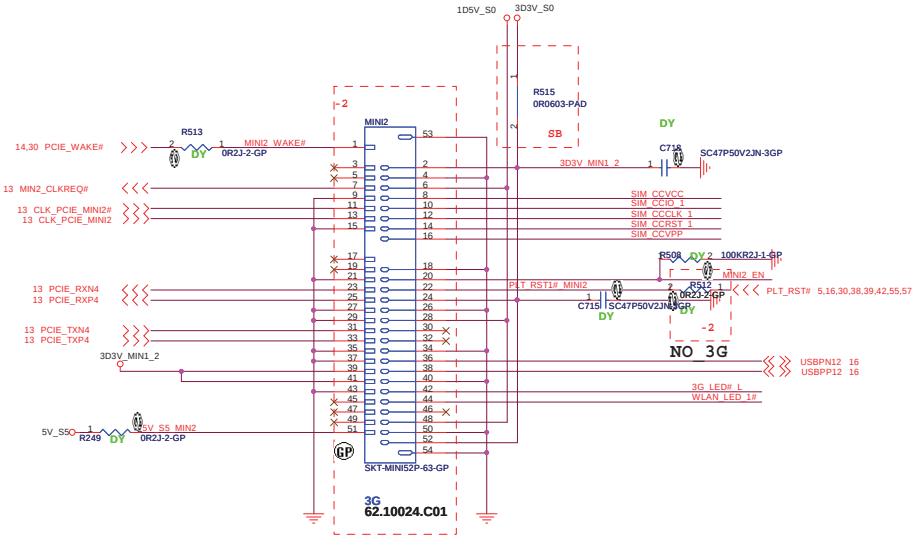
Mini Card Connector(WLAN)
Support debug-card



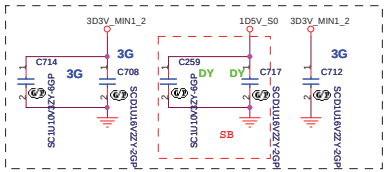
Place near MINI1

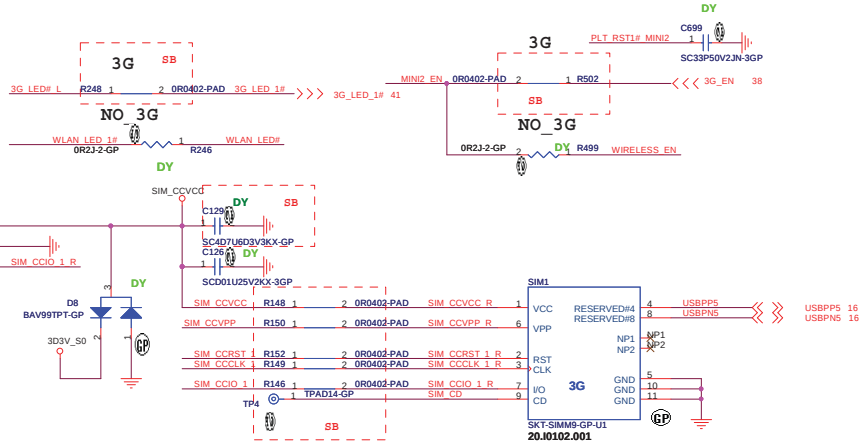


Mini Card Connector(Robson2 and 3G)



Place near MINIC2





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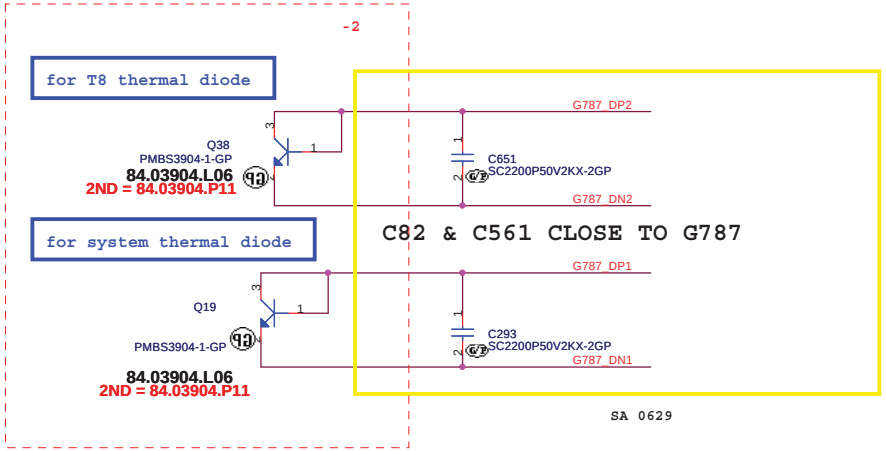
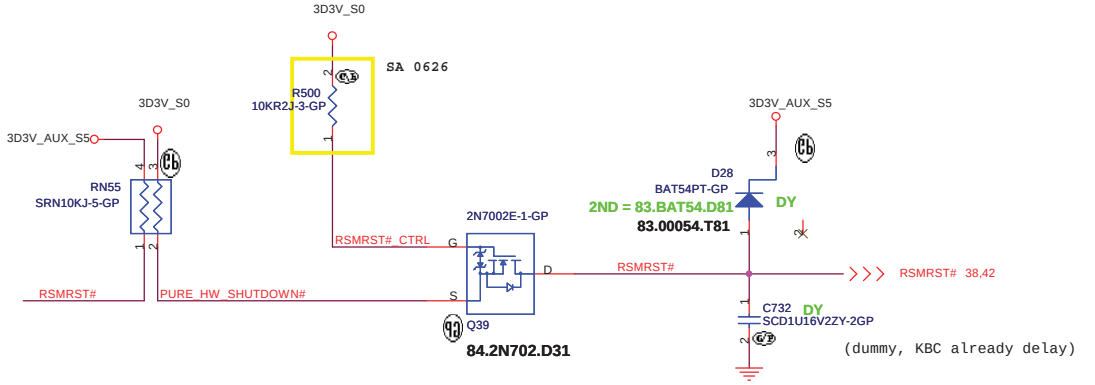
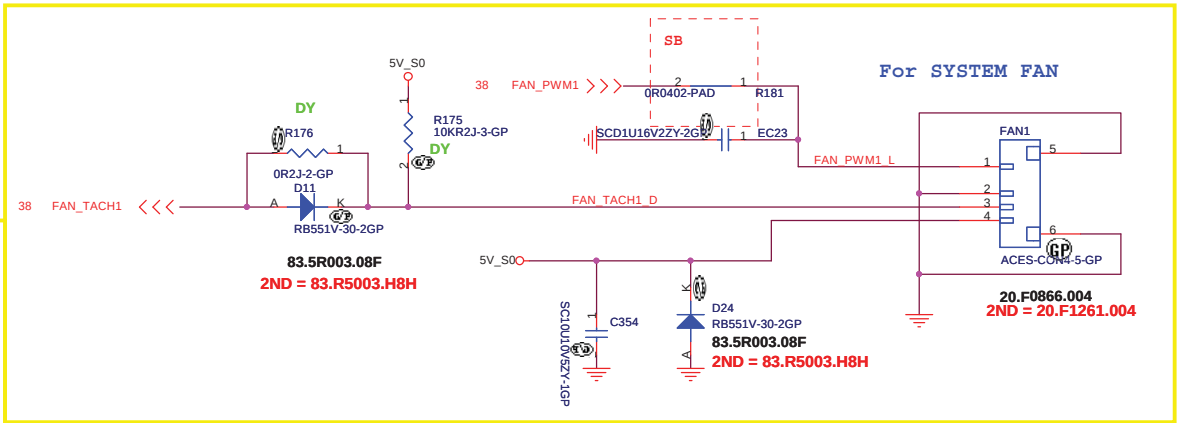
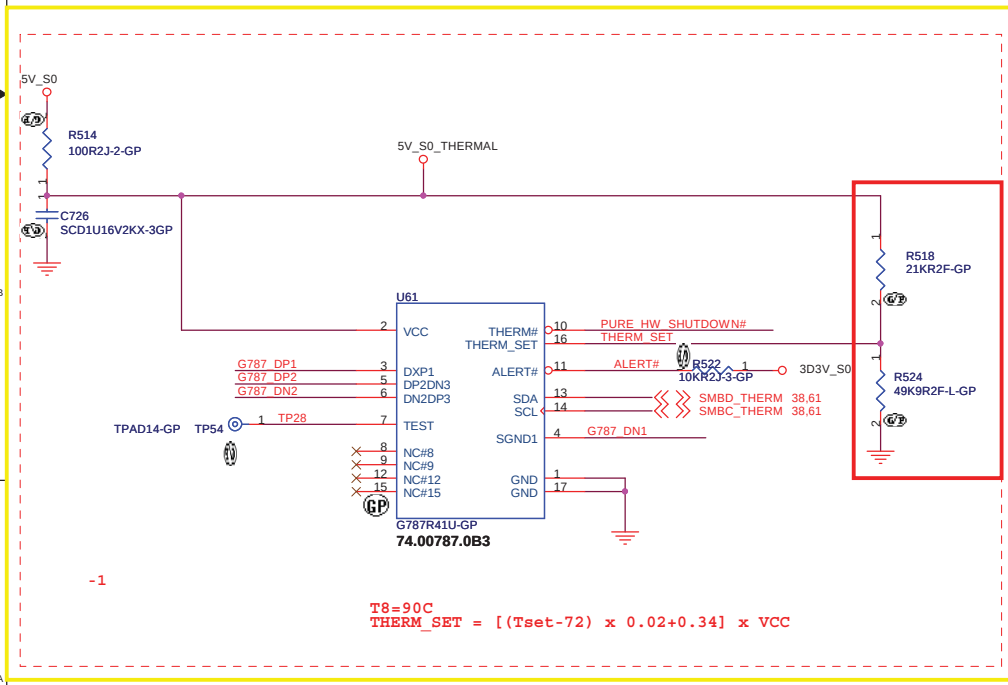
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

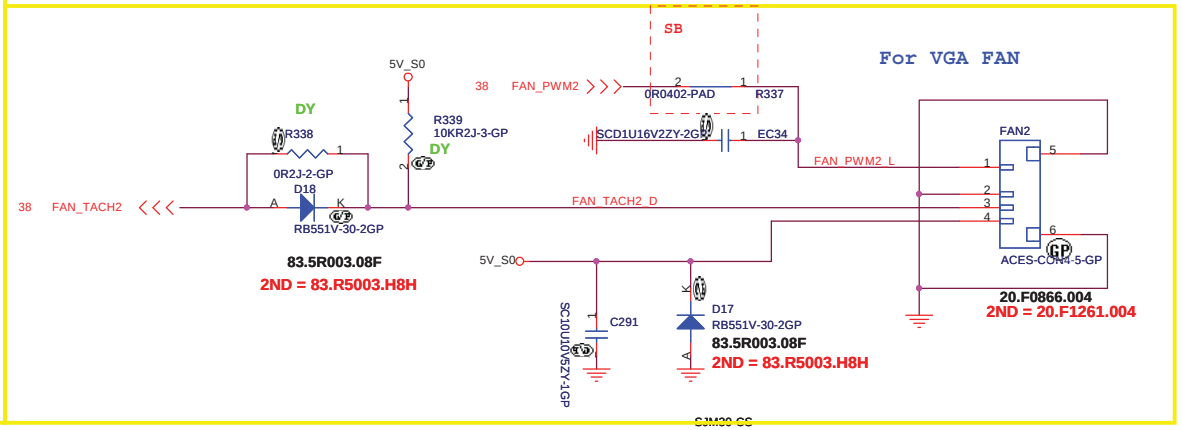
Title	MINI Conn	
Size: Custom	Document Number: SJM30-CS	Rev: -2
Date: Friday, April 09, 2010	Sheet 36 of 67	











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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**Thermal/Fan Conn**	
Size A3	Document Number **SJM30-CS**	Rev -2
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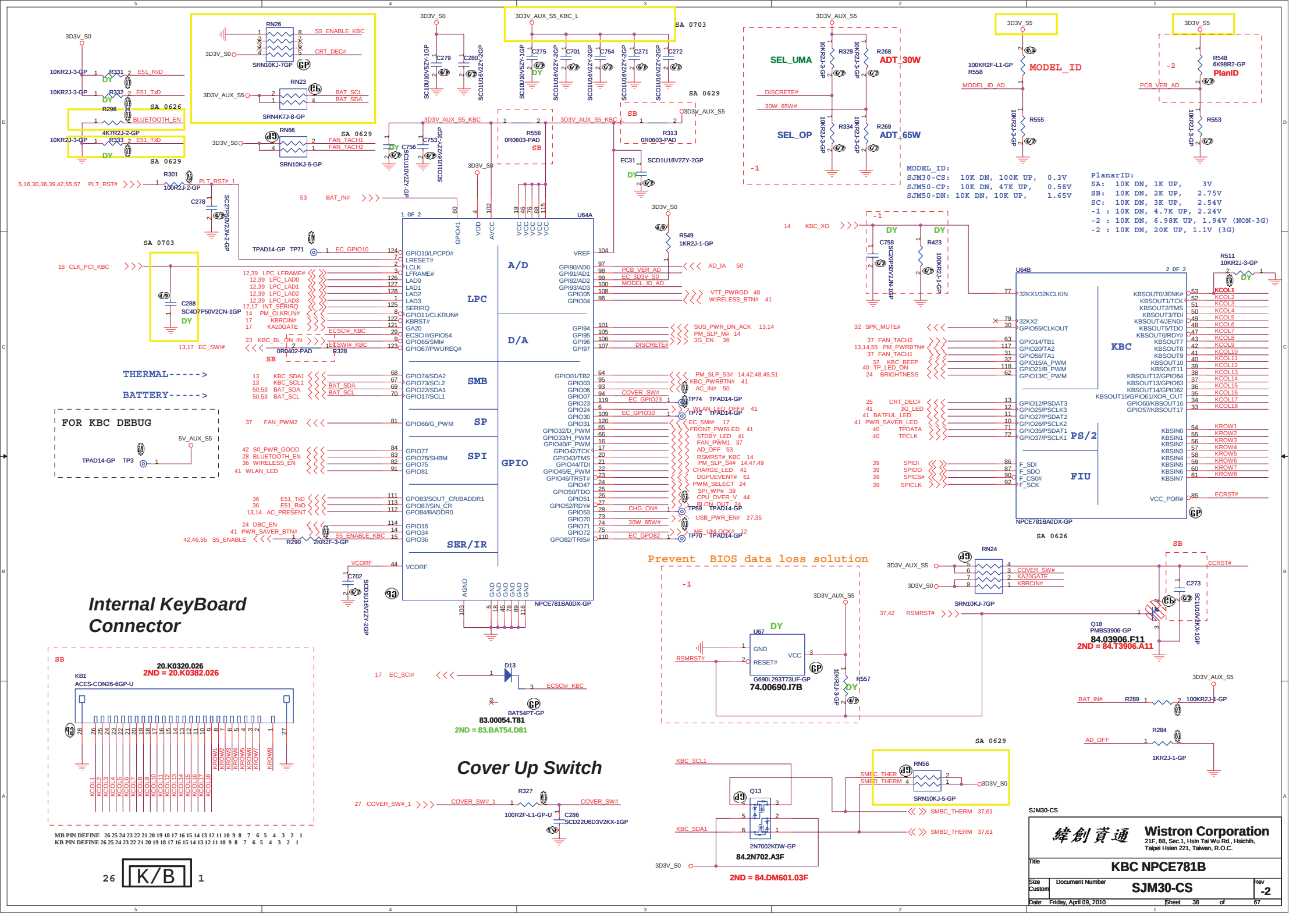
Internal KeyBoard Connector
Cover Up Switch
Prevent BIOS data loss solution
FOR KBC DEBUG
THERMAL------>
BATTERY------>
MODEL_ID:
SJM30-CS: 10K DN, 100K UP, 0.3V
SJM50-CP: 10K DN, 47K UP, 0.58V
SJM50-DN: 10K DN, 10K UP, 1.65V
PlanarID:
SA: 10K DN, 1K UP, 3V
SB: 10K DN, 2K UP, 2.75V
SC: 10K DN, 3K UP, 2.54V
-1 : 10K DN, 4.7K UP, 2.24V
-2 : 10K DN, 6.98K UP, 1.94V (NON-3G)
-2 : 10K DN, 20K UP, 1.1V (3G)
U64A
U64B
KBC
PS/2
FIU
LPC
SMB
SPI
GPIO
SER/IR
A/D
D/A
SP
MB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
KB PIN DEFINE 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC NPCE781B
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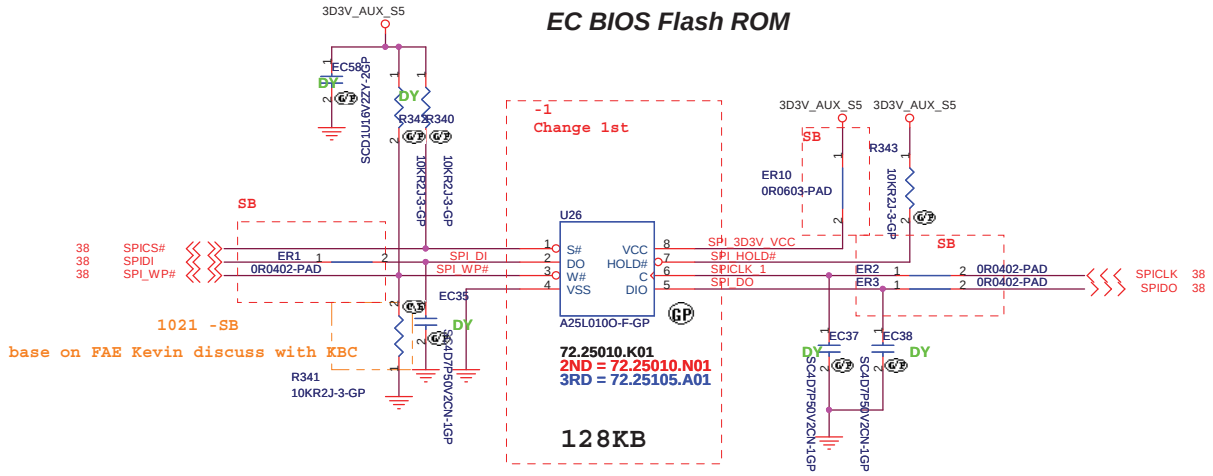
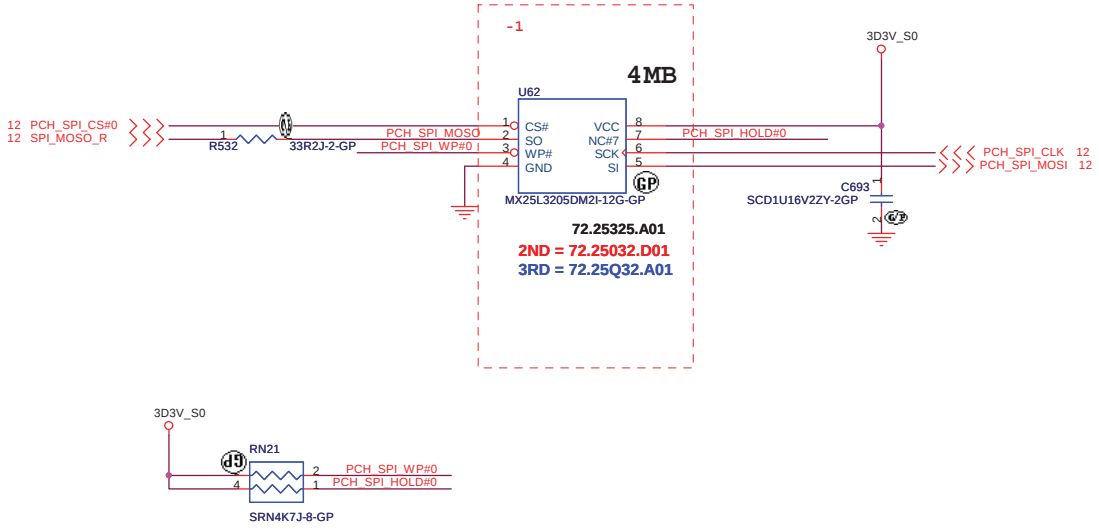
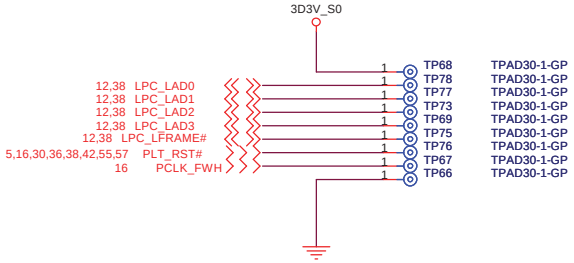
EC BIOS Flash ROM



System BIOS Flash ROM



GOLDEN FINGER FOR DEBUG BOARD



SJM30-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: BIOS		
Size: A3	Document Number: SJM30-CS	Rev: -2
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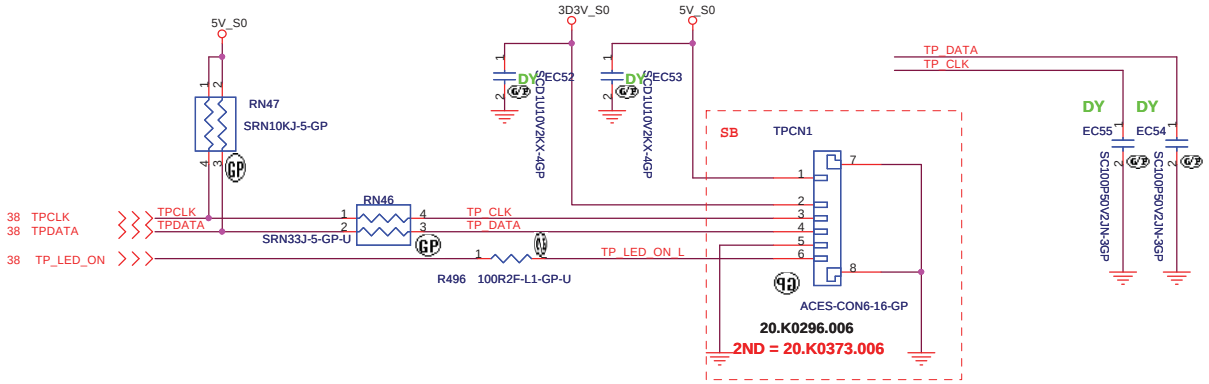
PIN	SIGNAL
1	VDD (5V FOR PS2 AND LED)
2	VDD (3.3V FOR CAPACITOR SENSOR)
3	CLK
4	DATA
5	GND
6	LED ON/OFF Control

TOUCH PAD



1 6

T/P

Need confirm

SJM30-CS

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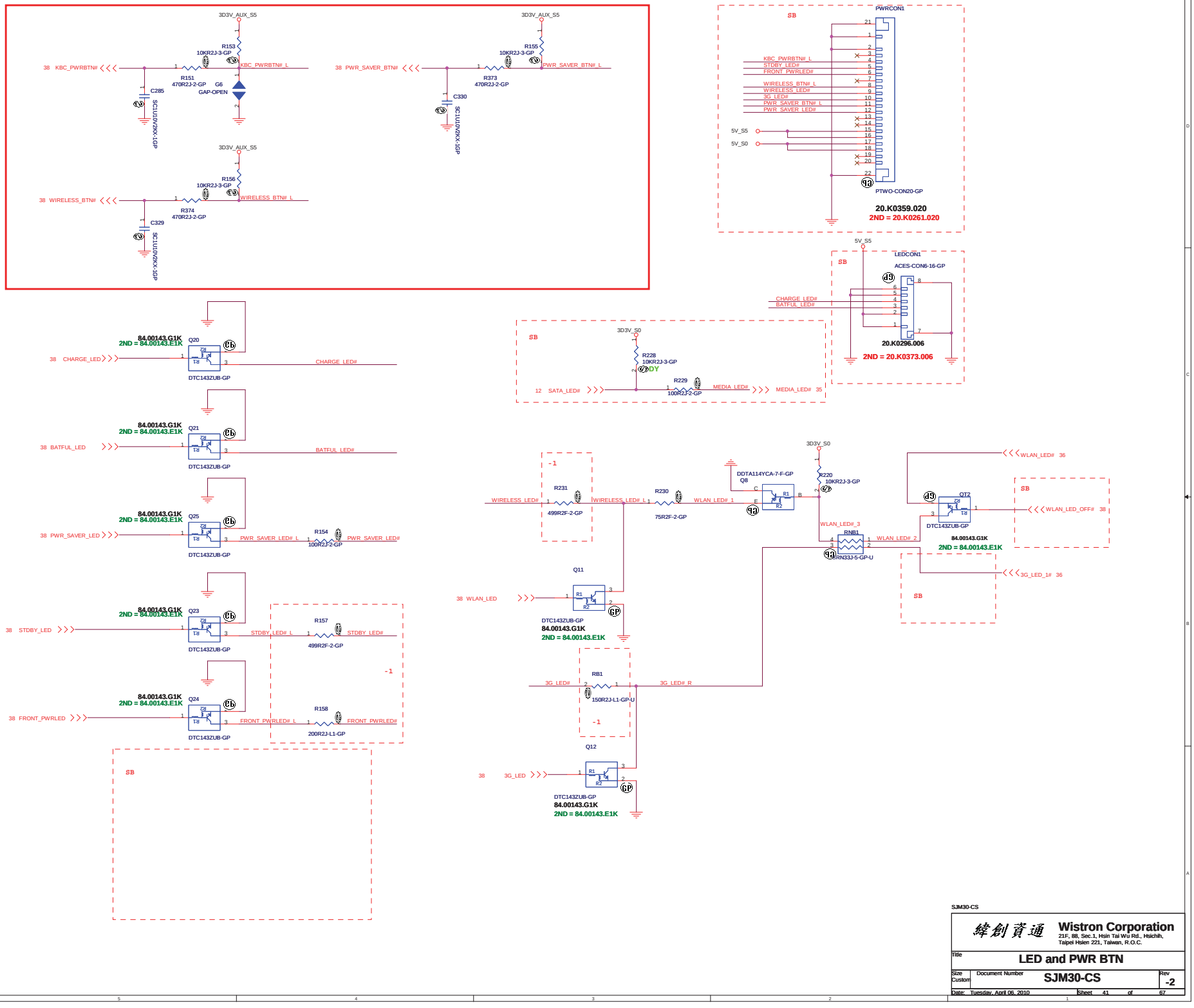
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Touch Pad		
Size: A3	Document Number: SJM30-CS	Rev: -2
Date: Tuesday, April 06, 2010	Sheet 40 of 67	


3D3V_AUX_S5
R153
10KR2J-3-GP
38 KBC_PWRBTN#
KBC_PWRBTN# L
R151
470R2J-2-GP
G6
GAP-OPEN
C285
SC1U10V2KX-1GP
3D3V_AUX_S5
R155
10KR2J-3-GP
38 PWR_SAVER_BTN#
PWR_SAVER_BTN# L
R373
470R2J-2-GP
C330
SC1U10V2KX-1GP
3D3V_AUX_S5
R156
10KR2J-3-GP
38 WIRELESS_BTN#
WIRELESS_BTN# L
R374
470R2J-2-GP
C329
SC1U10V2KX-1GP
SB
PWRCON1
KBC_PWRBTN# L
STDBY_LED#
FRONT_PWRLED#
WIRELESS_BTN# L
WIRELESS_LED#
3G_LED#
PWR_SAVER_BTN# L
PWR_SAVER_LED#
5V_S5
5V_S0
PTWO-CON20-GP
20.K0359.020
2ND = 20.K0261.020
5V_S5
SB
LEDCON1
ACES-CON6-16-GP
CHARGE_LED#
BATFUL_LED#
20.K0296.006
2ND = 20.K0373.006
SB
3D3V_S0
R228
10KR2J-3-GP
DY
12 SATA_LED#
R229
100R2J-2-GP
MEDIA_LED#
MEDIA_LED# 35
84.00143.G1K
2ND = 84.00143.E1K
Q20
38 CHARGE_LED
CHARGE_LED#
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
Q21
38 BATFUL_LED
BATFUL_LED#
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
Q25
38 PWR_SAVER_LED
PWR_SAVER_LED# L
R154
100R2J-2-GP
PWR_SAVER_LED#
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
Q23
38 STDBY_LED
STDBY_LED# L
R157
499R2F-2-GP
STDBY_LED#
DTC143ZUB-GP
-1
84.00143.G1K
2ND = 84.00143.E1K
Q24
38 FRONT_PWRLED
FRONT_PWRLED# L
R158
200R2J-L1-GP
FRONT_PWRLED#
DTC143ZUB-GP
SB
-1
WIRELESS_LED#
R231
499R2F-2-GP
WIRELESS_LED# L
R230
75R2F-2-GP
WLAN_LED# 1
DDTA114YCA-7-F-GP
Q8
3D3V_S0
R220
10KR2J-3-GP
WLAN_LED#_3
RNB1
8P4R33J-5-GP-U
WLAN_LED# 2
WLAN_LED# 36
QT2
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
SB
WLAN_LED_OFF# 38
3G_LED_1# 36
SB
Q11
38 WLAN_LED
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
3G_LED#
RB1
150R2J-L1-GP-U
3G_LED# R
-1
Q12
38 3G_LED
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.E1K
SB
SJM30-CS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
LED and PWR BTN
Size
Custom
Document Number
SJM30-CS
Rev
-2
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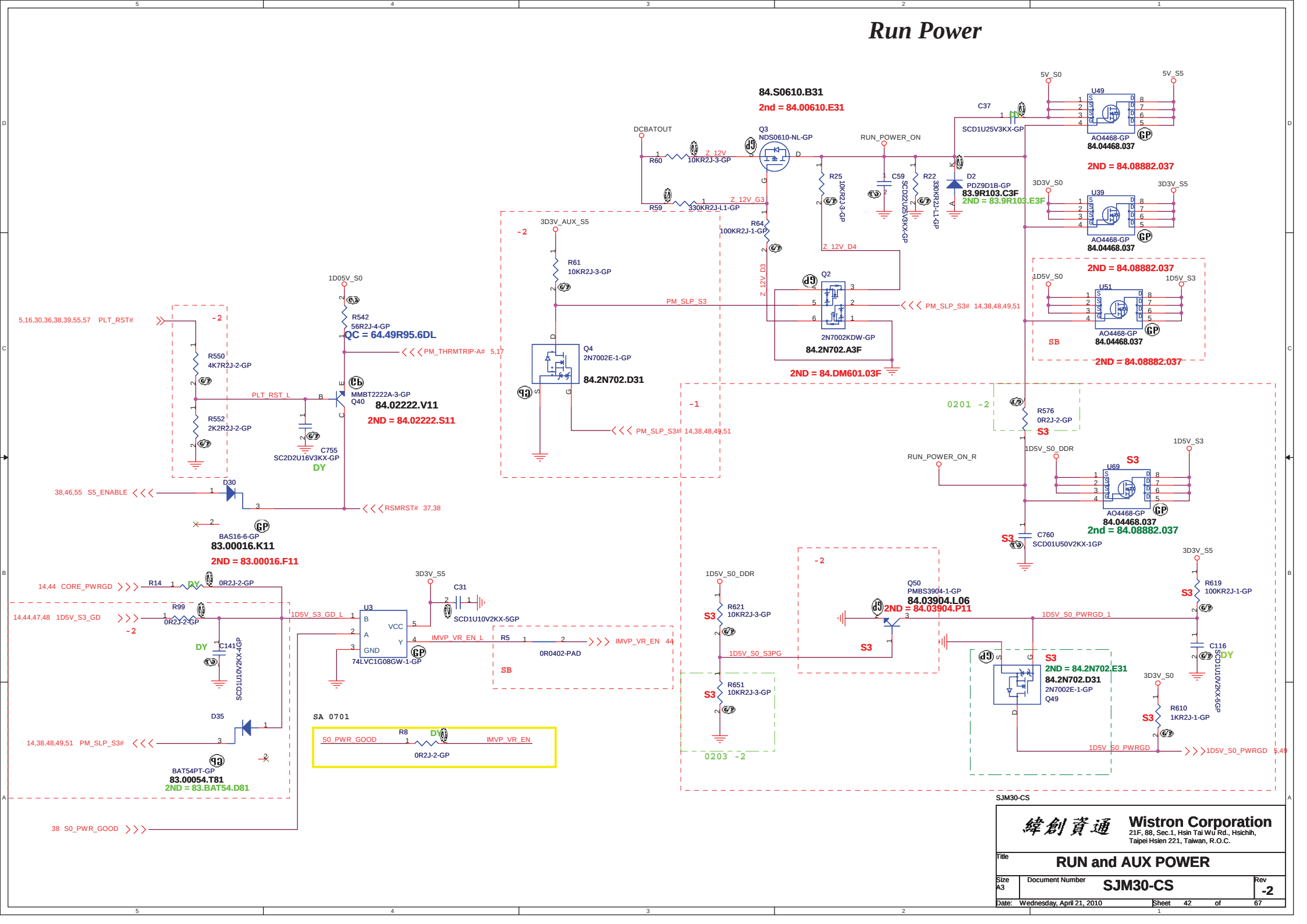
Sheet 41 of 67

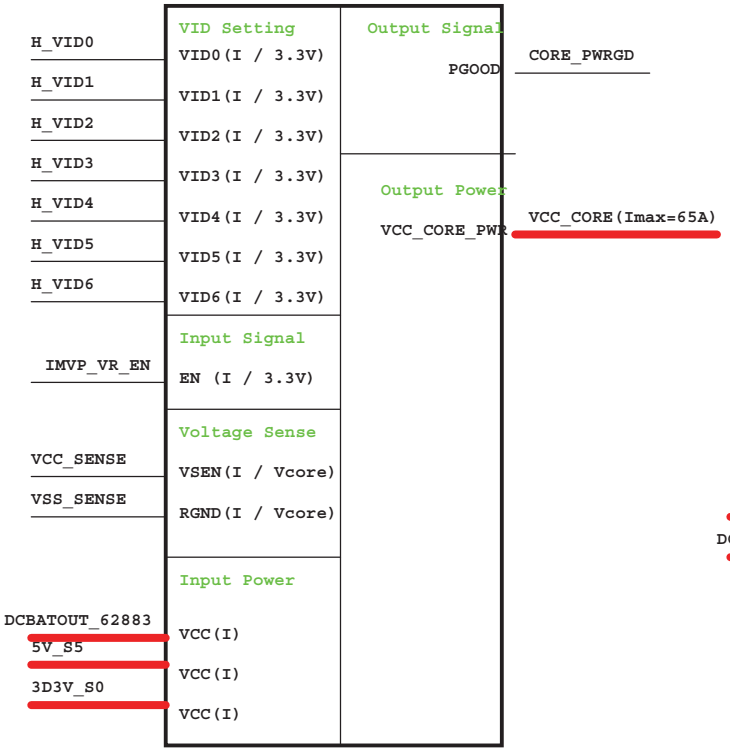
Run Power



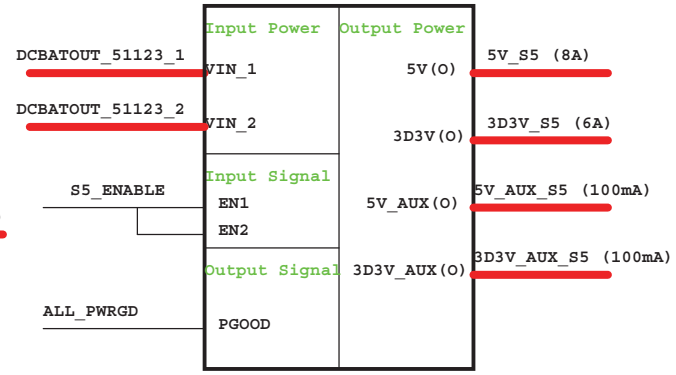
SJM30-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	**RUN and AUX POWER**
Size A3	Document Number **SJM30-CS** Rev **-2**
Date: Wednesday, April 21, 2010	Sheet 42 of 67

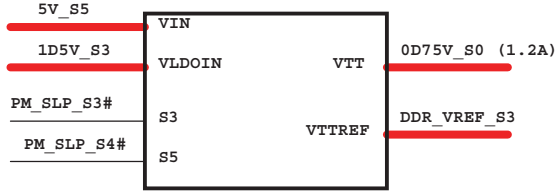
ISL62883 VCC_CORE



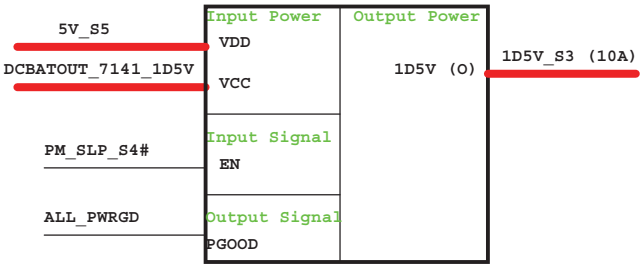
TPS51123 5V/3D3V



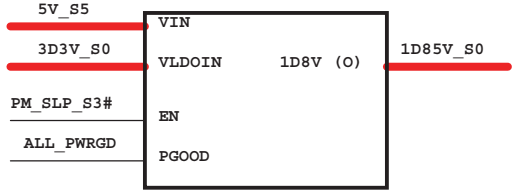
RT9026 0D75V_S0



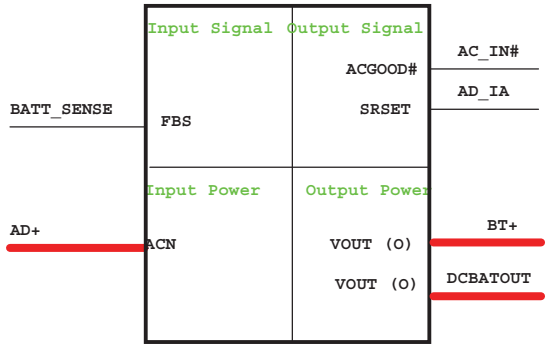
RT9025 1D5V



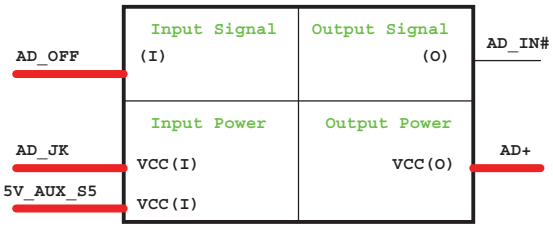
RT9025 1D8V



Charger BQ24745



Adapter



SJM30-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Power Block Diagram**

Size	Document Number	Rev
	SJM30-CS	-2

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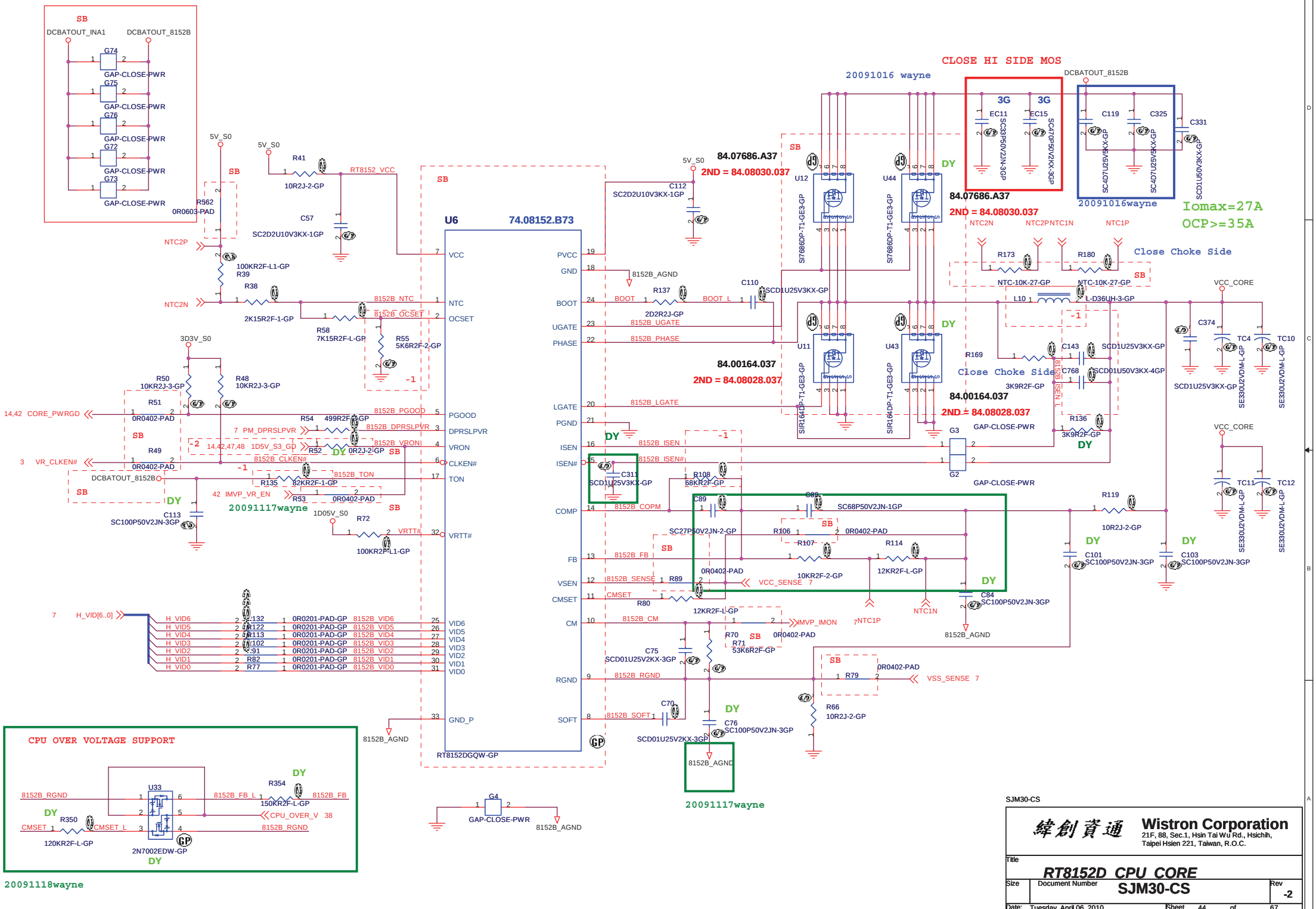

SJM30-CS

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8152D CPU CORE

Size	Document Number	Rev
	SJM30-CS	-2

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SJM30-CS

緯創資通

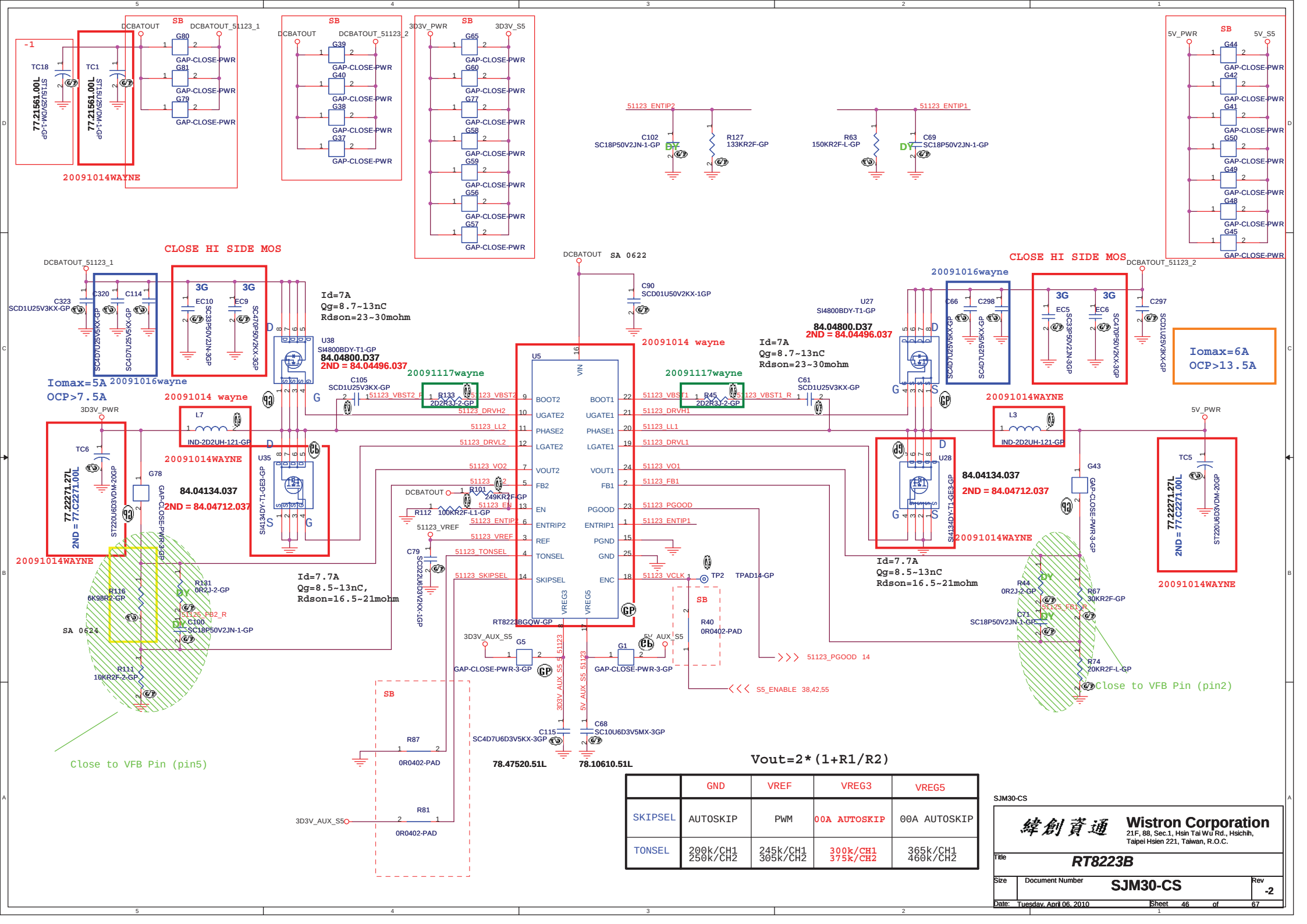
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

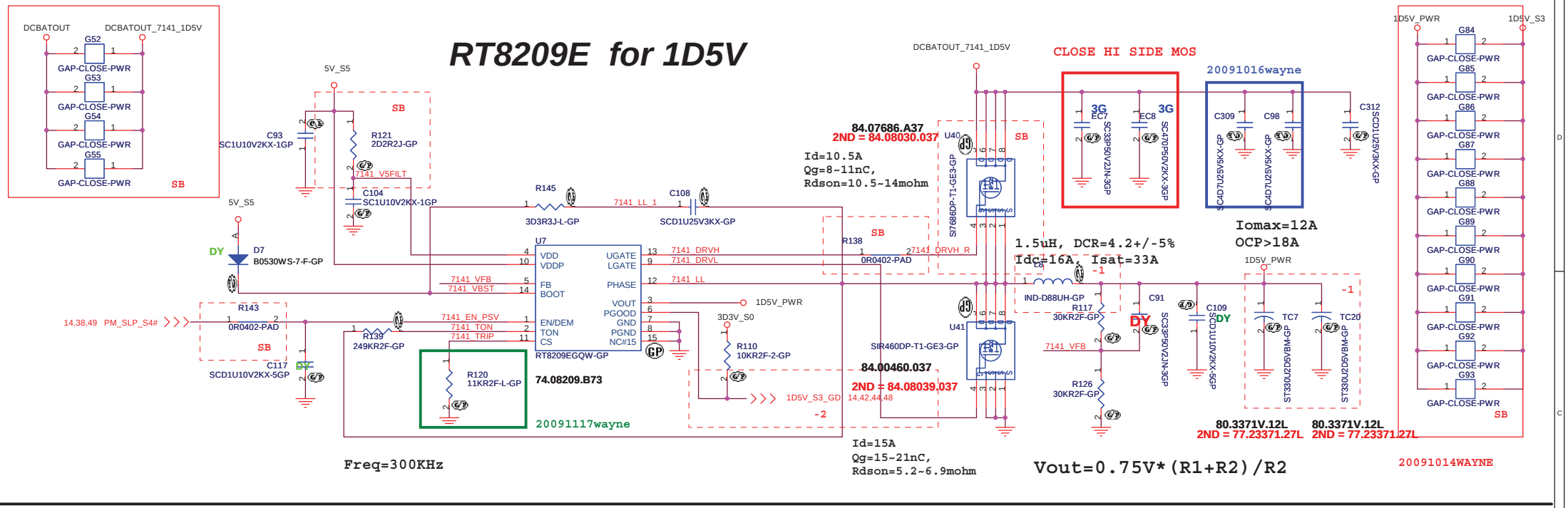
RESERVER

Size	Document Number	Rev
	SJM30-CS	**-2**

Date: Wednesday, March 31, 2010 Sheet 45 of 67

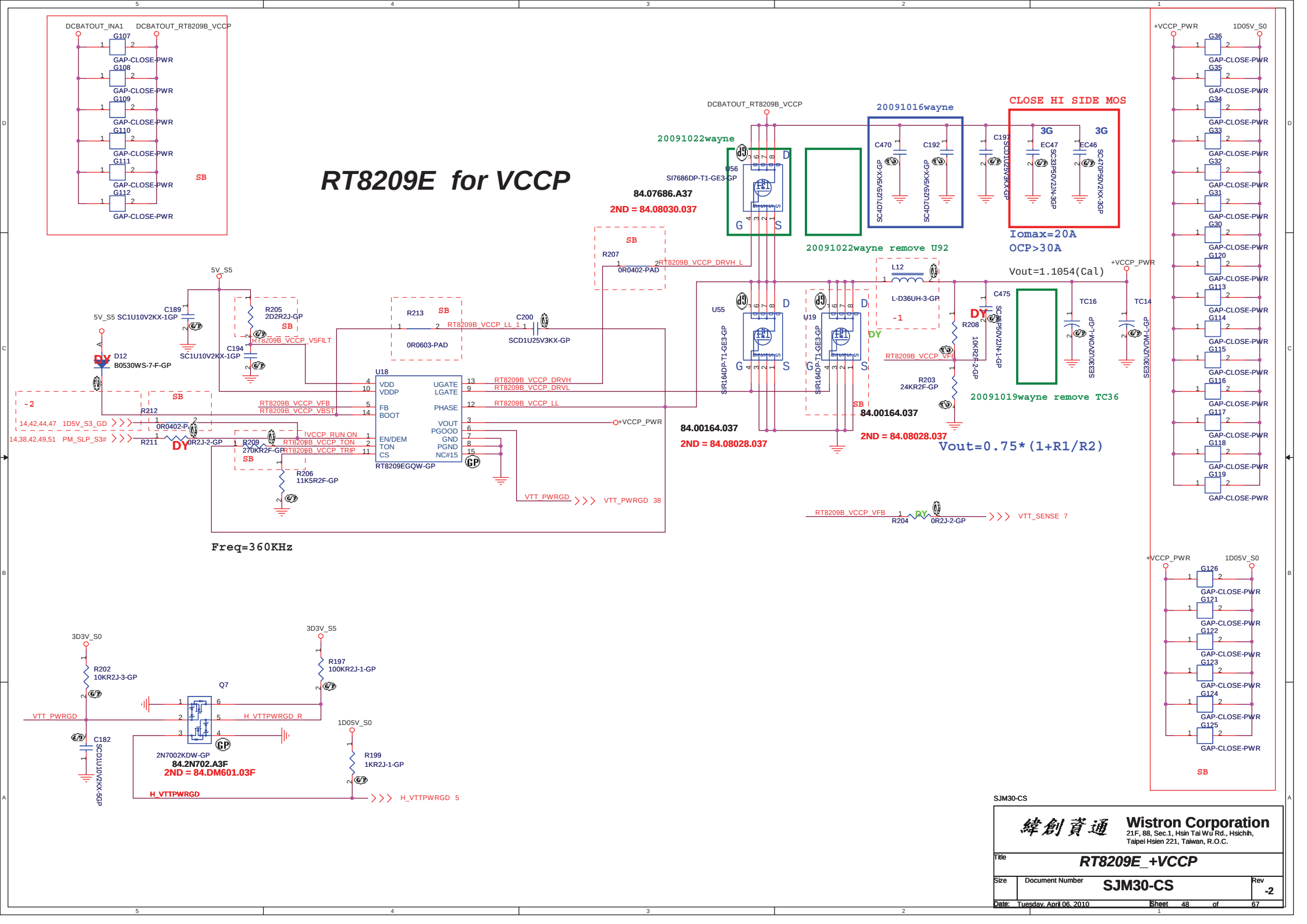


	GND	VREF	VREG3	VREG5
SKIPSEL	AUTOSKIP	PWM	00A AUTOSKIP	00A AUTOSKIP
TONSEL	200k/CH1 250k/CH2	245k/CH1 305k/CH2	300k/CH1 375k/CH2	365k/CH1 460k/CH2



SJM30-CS

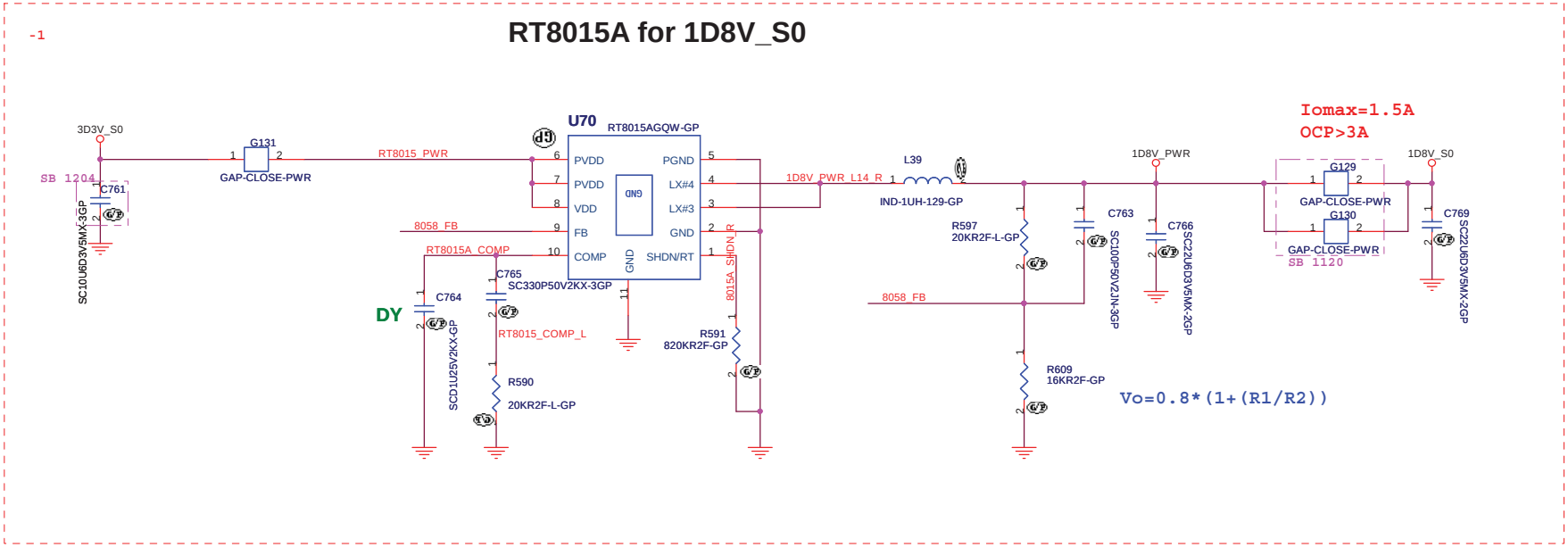
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT8209E_1D5V***	
Size	Document Number **SJM30-CS**	Rev **-2**
Date: Tuesday, April 06, 2010	Sheet 47 of 67	



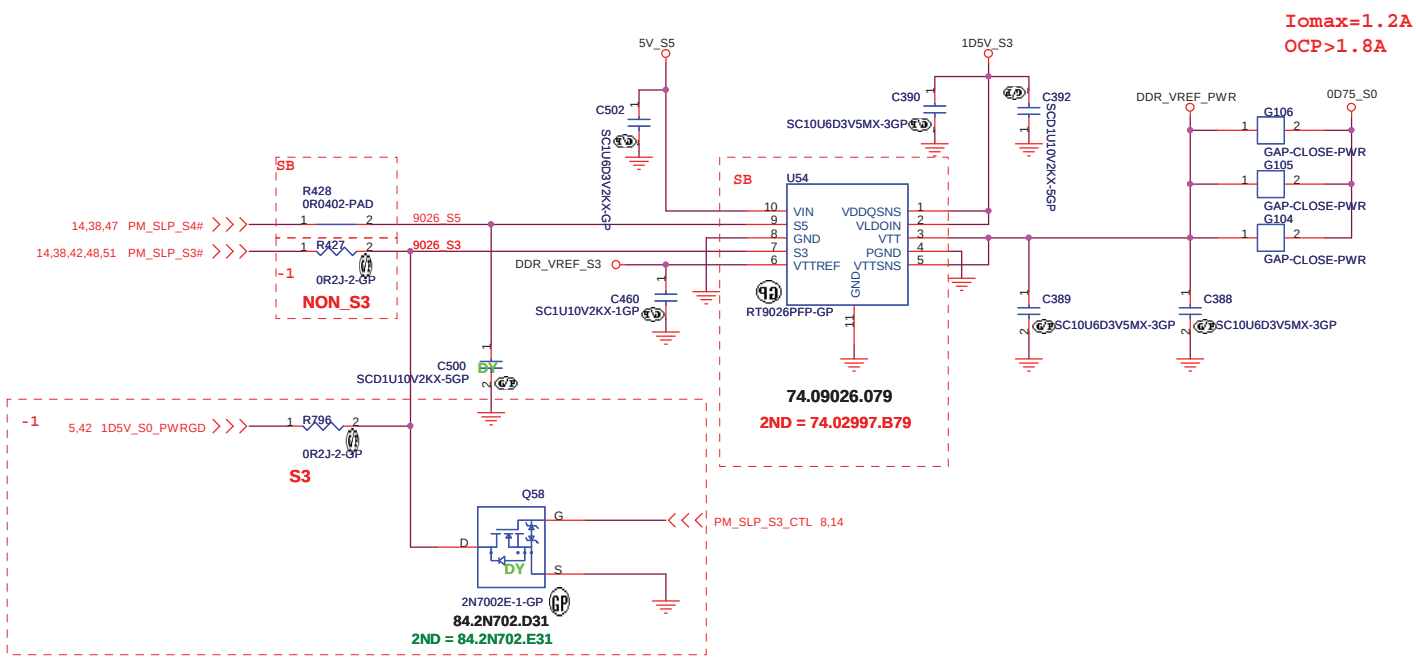
SJM30-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RT8209E_+VCCP***	
Size	Document Number **SJM30-CS**	Rev **-2**
Date: Tuesday, April 06, 2010	Sheet 48 of 67	

RT8015A for 1D8V_S0



RT9026 for 0D75V_S3



SJM30-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RT8015A 1D8V/RT9026 0D75*

Size	Document Number	Rev
	SJM30-CS	-2

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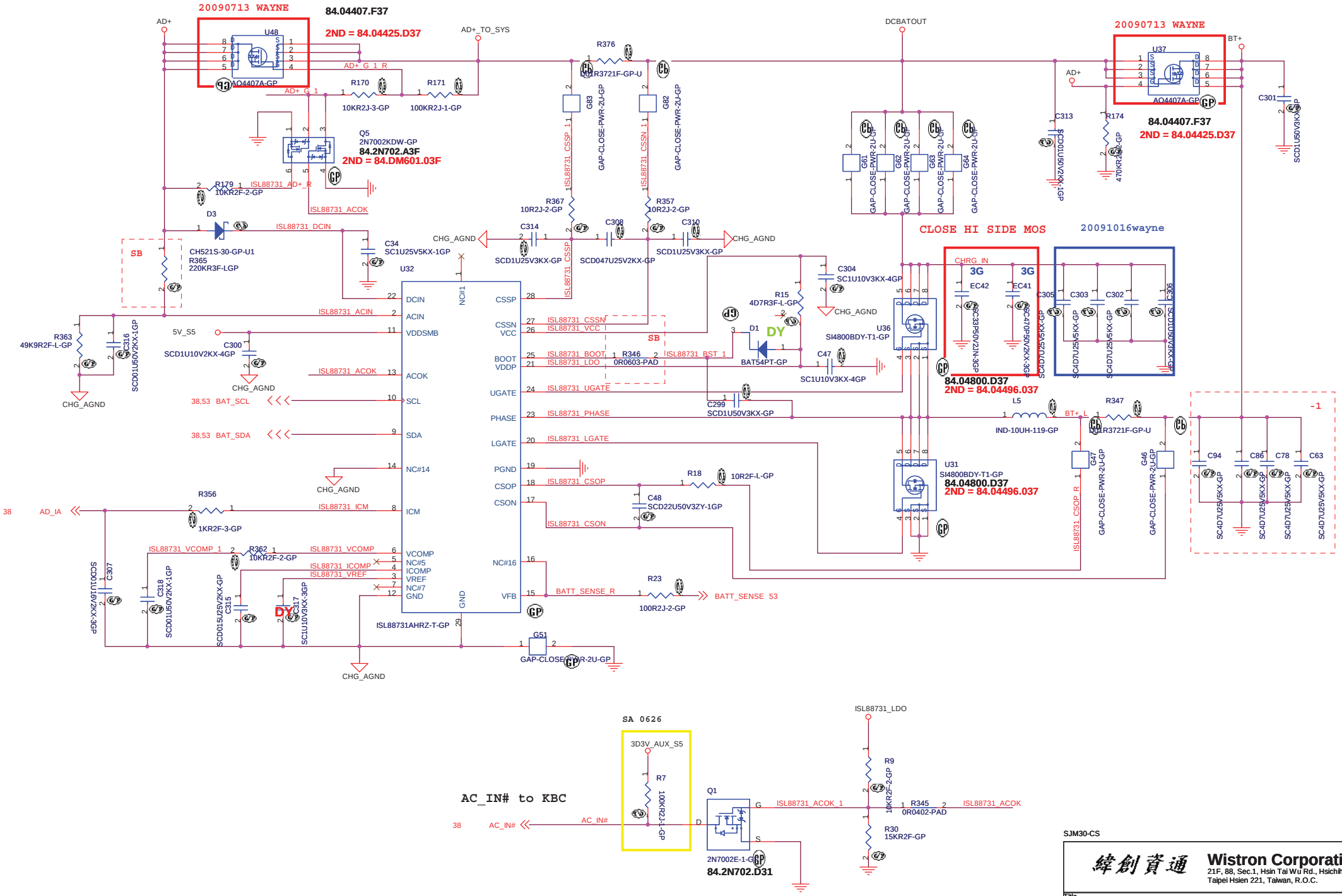
20090713 WAYNE
84.04407.F37
2ND = 84.04425.D37
U48
AO4407A-GP
AD+
AD+_TO_SYS
AD+_G_1
AD+_G_1_R
R170
10KR2J-3-GP
R171
100KR2J-1-GP
Q5
2N7002KDW-GP
84.2N702.A3F
2ND = 84.DM601.03F
R179
10KR2F-2-GP
ISL88731_AD+_R
ISL88731_ACOK
D3
CH521S-30-GP-U1
R365
220KR3F-LGP
ISL88731_DCIN
SB
C34
SC1U25V5KX-1GP
CHG_AGND
U32
ISL88731AHRZ-T-GP
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
NC#1
R363
49K9R2F-L-GP
C316
SCD01U50V2KX-1GP
5V_S5
C300
SCD1U10V2KX-4GP
38,53 BAT_SCL
38,53 BAT_SDA
R356
1KR2F-3-GP
38 AD_IA
ISL88731_ICM
ISL88731_VCOMP_1
R362
10KR2F-2-GP
ISL88731_VCOMP
ISL88731_ICOMP
ISL88731_VREF
C307
SCD01U50V2KX-3GP
C318
SCD01U50V2KX-1GP
C315
SCD015U25V2KX-GP
C317
SC1U10V3KX-3GP
DY
R376
0UR3721F-GP-U
G83
G82
GAP-CLOSE-PWR-2U-GP
ISL88731_CSSP_1
ISL88731_CSSN_1
R367
10R2J-2-GP
R357
10R2J-2-GP
C314
SCD1U25V3KX-GP
C308
SCD047U25V2KX-GP
C310
SCD1U25V3KX-GP
CHG_AGND
ISL88731_CSSP
ISL88731_CSSN
ISL88731_VCC
ISL88731_BOOT
ISL88731_LDO
ISL88731_UGATE
ISL88731_PHASE
ISL88731_LGATE
ISL88731_CSOP
ISL88731_CSON
R346
0R0603-PAD
ISL88731_BST_1
SB
R15
4D7R3F-L-GP
D1
BAT54PT-GP
DY
C304
SC1U10V3KX-4GP
C47
SC1U10V3KX-4GP
C299
SCD1U50V3KX-GP
R18
10R2F-L-GP
C48
SCD22U50V3ZY-1GP
R23
100R2J-2-GP
BATT_SENSE_R
BATT_SENSE 53
G51
GAP-CLOSE-PWR-2U-GP
DCBATOUT
G61
G62
G63
G64
C313
SCD01U50V2KX-1GP
20090713 WAYNE
U37
AO4407A-GP
84.04407.F37
2ND = 84.04425.D37
R174
470KR2F-GP
C301
SCD1U50V3KX-GP
BT+
CLOSE HI SIDE MOS
20091016wayne
CHRG_IN
3G
EC42
EC41
C305
C303
C302
C306
SC4D7U25V5KX-GP
SC4D7U25V5KX-3GP
SCD1U50V3KX-GP
84.04800.D37
2ND = 84.04496.037
U36
SI4800BDY-T1-GP
U31
SI4800BDY-T1-GP
84.04800.D37
2ND = 84.04496.037
L5
IND-10UH-119-GP
BT+_L
R347
0UR3721F-GP-U
G47
G46
GAP-CLOSE-PWR-2U-GP
ISL88731_CSOP_R
-1
C94
C86
C78
C63
SC4D7U25V5KX-GP
SA 0626
3D3V_AUX_S5
R7
100KR2J-1-GP
AC_IN# to KBC
38 AC_IN#
Q1
2N7002E-1-GP
84.2N702.D31
ISL88731_ACOK_1
R9
10KR2F-2-GP
R345
0R0402-PAD
R30
15KR2F-GP
ISL88731_ACOK
SJM30-CS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A CHARGER
Size
Document Number
SJM30-CS
Rev
-2
Date: Tuesday, April 06, 2010
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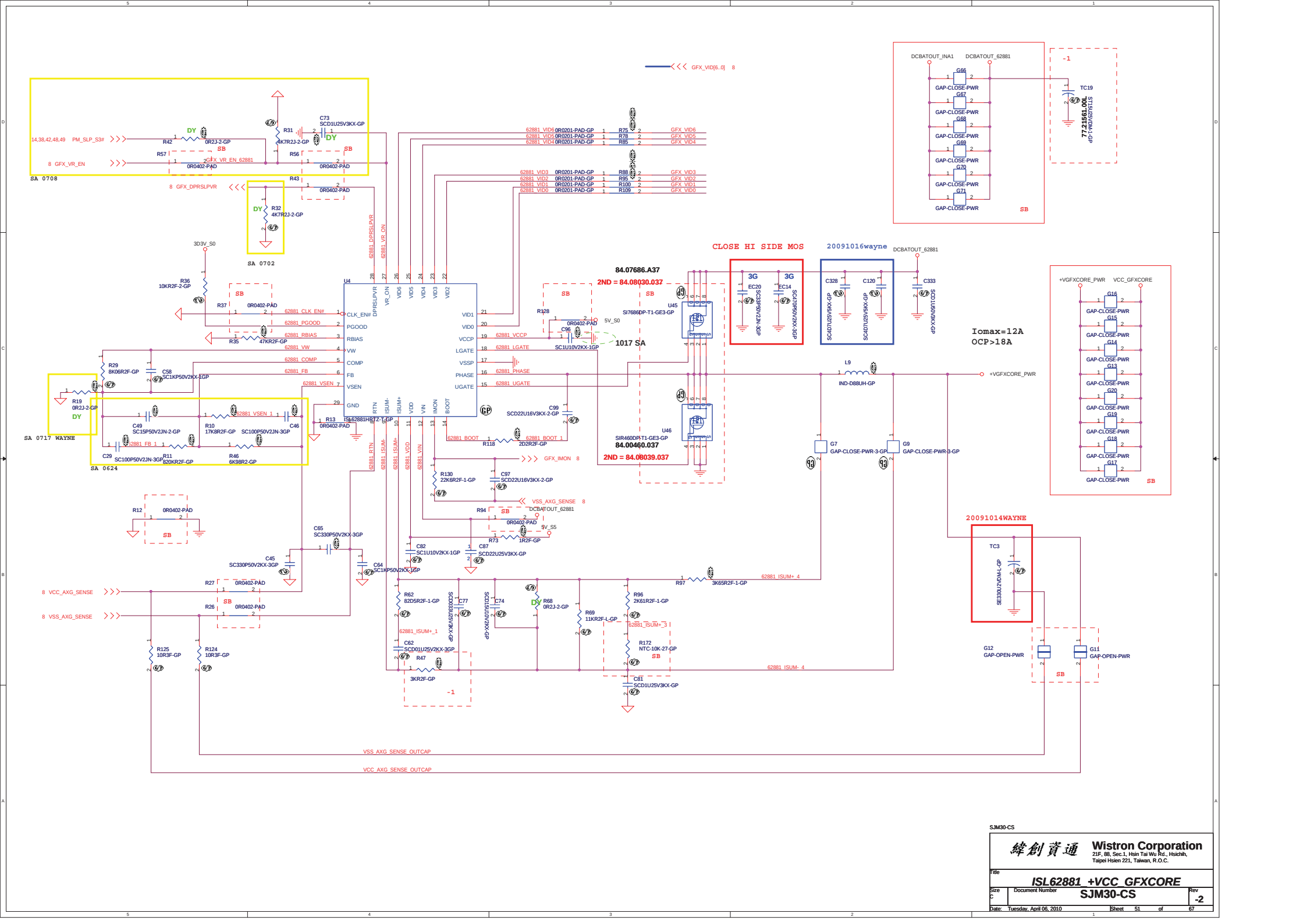
GFX_VID[6..0] 8
DCBATOUT_INA1
DCBATOUT_62881
TC19
7721551.001
GAP-CLOSE-PWR
SB
14,38,42,48,49 PM_SLP_S3#
8 GFX_VR_EN
8 GFX_DPRSLPVR
SA 0708
SA 0702
3D3V_S0
GFX_VR_EN_62881
62881_DPRSLPVR
62881_VR_ON
62881_VID6
62881_VID5
62881_VID4
62881_VID3
62881_VID2
62881_VID1
62881_VID0
GFX_VID6
GFX_VID5
GFX_VID4
GFX_VID3
GFX_VID2
GFX_VID1
GFX_VID0
CLOSE HI SIDE MOS
20091016wayne
84.07686.A37
2ND = 84.08030.037
SI7686DP-T1-GE3-GP
SIR460DP-T1-GE3-GP
84.00460.037
2ND = 84.08039.037
1017 SA
Iomax=12A
OCP>18A
+VGFXCORE_PWR
VCC_GFXCORE
IND-D88UH-GP
5V_S0
5V_S5
62881_VCCP
62881_LGATE
62881_PHASE
62881_UGATE
62881_BOOT
62881_BOOT_1
GFX_IMON 8
VSS_AXG_SENSE 8
VCC_AXG_SENSE 8
VSS_AXG_SENSE_OUTCAP
VCC_AXG_SENSE_OUTCAP
62881_ISUM+_1
62881_ISUM+_3
62881_ISUM+ 4
62881_ISUM- 4
20091014WAYNE
SA 0717 WAYNE
SA 0624
SJM30-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL62881_+VCC_GFXCORE
SJM30-CS
-2
Tuesday, April 06, 2010
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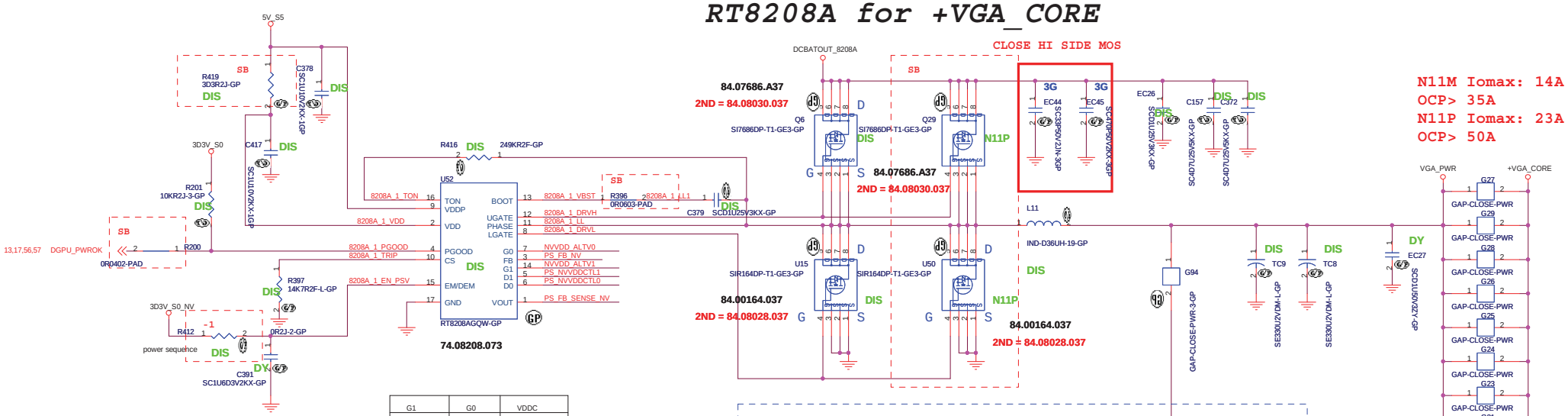
RT8208A for +VGA_CORE



G1	G0	VDDC
0	0	0.85V
0	1	0.85V
1	0	1.03V

NVDD = (1 + Rt / Rb) X 0.75

SJM30-CS SUPPORT

P-STATE	NVVDD_ALTV1	NVVDD_ALTV0	N11M-GE1	N11M-GE2	N11M-OP1	N11P-GE1
BOOT => P12	0	0	0.85V	0.85V	0.85V	0.80V
P8	0	1	0.85V	0.85V	0.85V	0.85V
P0	1	0	1.03V	1.03V	1.03V	0.95V

	R417 (TOP)	R418 (GND)	R415 (VID_0)	R413 (VID_1)
N11M-GE1	10K(64.10025.6DL)	75K(64.75025.6DL)	909K(64.90935.6DL)	40.2K(64.40225.6DL)
N11M-GE2	10K(64.10025.6DL)	75K(64.75025.6DL)	909K(64.90935.6DL)	40.2K(64.40225.6DL)
N11M-OP1	10K(64.10025.6DL)	75K(64.75025.6DL)	909K(64.90935.6DL)	40.2K(64.40225.6DL)
N11P-GE1	5.11K(64.51115.6DL)	75K(64.75025.6DL)	75K(64.75025.6DL)	25.5K(64.25525.6DL)

SJM30-CS

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: RT8208A VGA_CORE

Size: Custom | Document Number: SJM30-CS | Rev: -2

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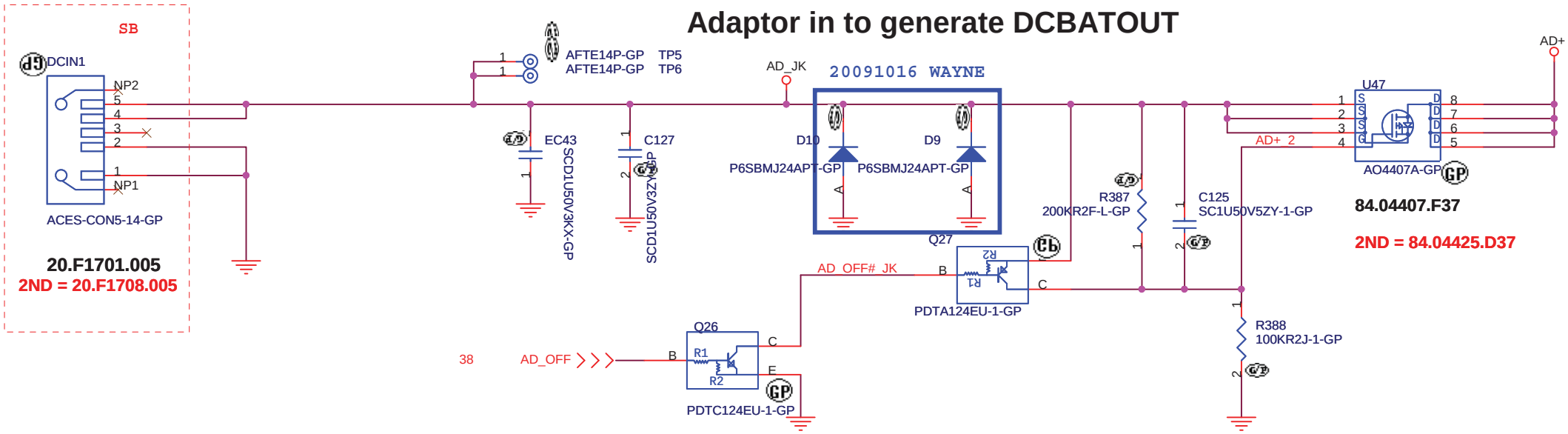
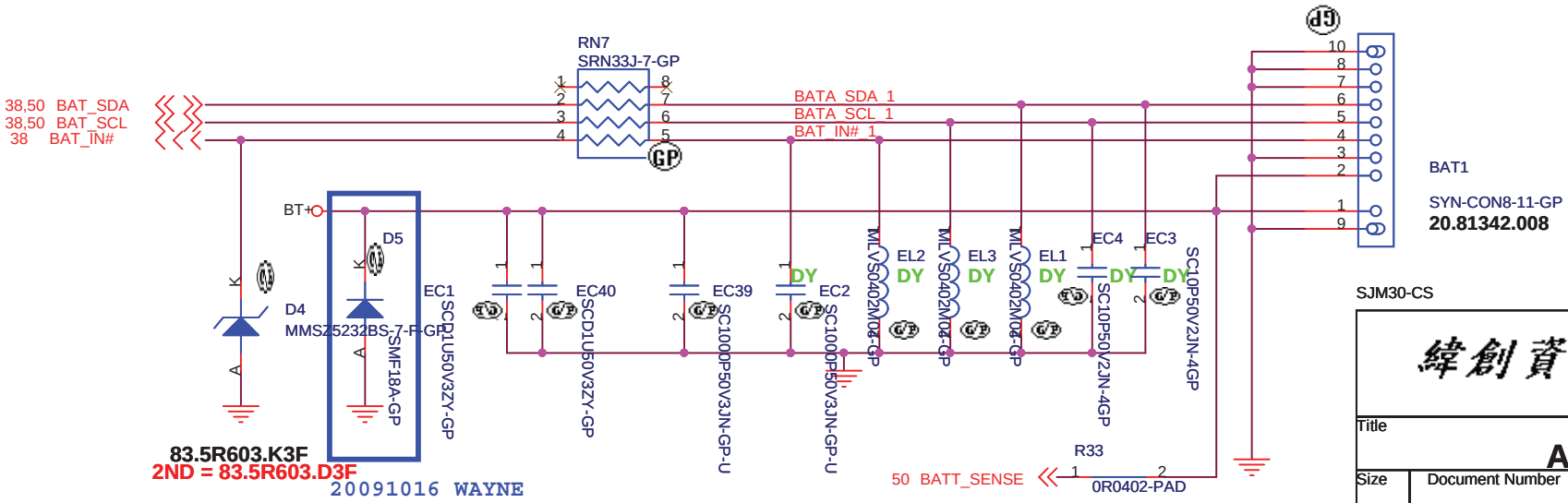
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



SJM30-CS

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**AD/BATT CONN**	
Size	Document Number **SJM30-CS**	Rev -2
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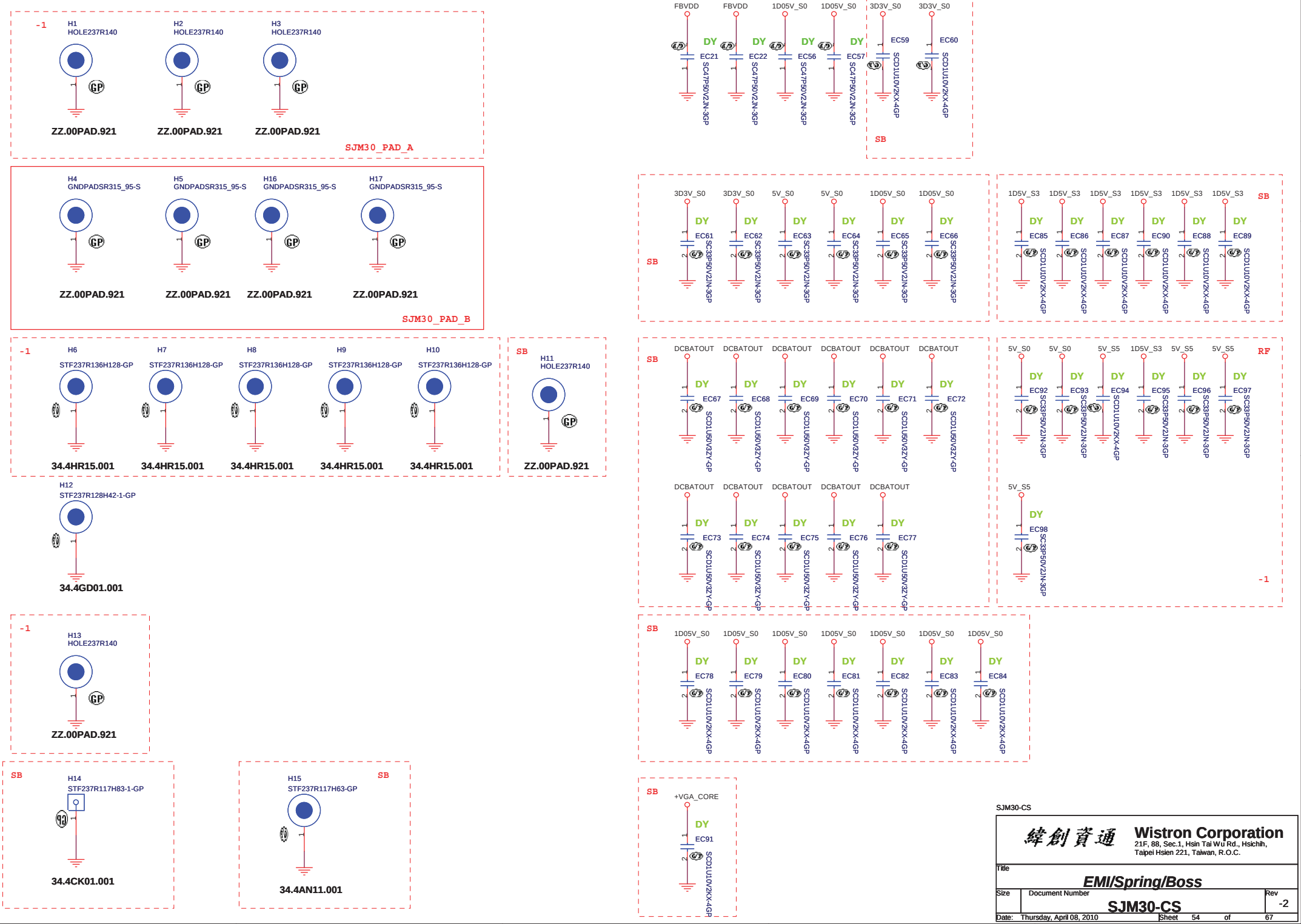
-1
H1
HOLE237R140
H2
HOLE237R140
H3
HOLE237R140
ZZ.00PAD.921
ZZ.00PAD.921
ZZ.00PAD.921
SJM30_PAD_A
H4
GNDPADSR315_95-S
H5
GNDPADSR315_95-S
H16
GNDPADSR315_95-S
H17
GNDPADSR315_95-S
ZZ.00PAD.921
ZZ.00PAD.921
ZZ.00PAD.921
ZZ.00PAD.921
SJM30_PAD_B
-1
H6
STF237R136H128-GP
H7
STF237R136H128-GP
H8
STF237R136H128-GP
H9
STF237R136H128-GP
H10
STF237R136H128-GP
34.4HR15.001
34.4HR15.001
34.4HR15.001
34.4HR15.001
34.4HR15.001
SB
H11
HOLE237R140
ZZ.00PAD.921
H12
STF237R128H42-1-GP
34.4GD01.001
-1
H13
HOLE237R140
ZZ.00PAD.921
SB
H14
STF237R117H83-1-GP
34.4CK01.001
SB
H15
STF237R117H63-GP
34.4AN11.001
FBVDD
FBVDD
1D05V_S0
1D05V_S0
3D3V_S0
3D3V_S0
DY
EC21
SC47P50V2JN-3GP
EC22
SC47P50V2JN-3GP
EC56
SC47P50V2JN-3GP
EC57
SC47P50V2JN-3GP
EC59
SCD1U10V2KX-4GP
EC60
SCD1U10V2KX-4GP
SB
SB
3D3V_S0
3D3V_S0
5V_S0
5V_S0
1D05V_S0
1D05V_S0
EC61
SC33P50V2JN-3GP
EC62
SC33P50V2JN-3GP
EC63
SC33P50V2JN-3GP
EC64
SC33P50V2JN-3GP
EC65
SC33P50V2JN-3GP
EC66
SC33P50V2JN-3GP
1D5V_S3
1D5V_S3
1D5V_S3
1D5V_S3
1D5V_S3
1D5V_S3
EC85
SCD1U10V2KX-4GP
EC86
SCD1U10V2KX-4GP
EC87
SCD1U10V2KX-4GP
EC90
SCD1U10V2KX-4GP
EC88
SCD1U10V2KX-4GP
EC89
SCD1U10V2KX-4GP
SB
SB
DCBATOUT
DCBATOUT
DCBATOUT
DCBATOUT
DCBATOUT
DCBATOUT
EC67
SCD1U50V3ZY-GP
EC68
SCD1U50V3ZY-GP
EC69
SCD1U50V3ZY-GP
EC70
SCD1U50V3ZY-GP
EC71
SCD1U50V3ZY-GP
EC72
SCD1U50V3ZY-GP
DCBATOUT
DCBATOUT
DCBATOUT
DCBATOUT
DCBATOUT
EC73
SCD1U50V3ZY-GP
EC74
SCD1U50V3ZY-GP
EC75
SCD1U50V3ZY-GP
EC76
SCD1U50V3ZY-GP
EC77
SCD1U50V3ZY-GP
5V_S0
5V_S0
5V_S5
1D5V_S3
5V_S5
5V_S5
RF
EC92
SC33P50V2JN-3GP
EC93
SC33P50V2JN-3GP
EC94
SCD1U10V2KX-4GP
EC95
SC33P50V2JN-3GP
EC96
SC33P50V2JN-3GP
EC97
SC33P50V2JN-3GP
5V_S5
EC98
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SB
1D05V_S0
1D05V_S0
1D05V_S0
1D05V_S0
1D05V_S0
1D05V_S0
1D05V_S0
EC78
SCD1U10V2KX-4GP
EC79
SCD1U10V2KX-4GP
EC80
SCD1U10V2KX-4GP
EC81
SCD1U10V2KX-4GP
EC82
SCD1U10V2KX-4GP
EC83
SCD1U10V2KX-4GP
EC84
SCD1U10V2KX-4GP
SB
+VGA_CORE
EC91
SCD1U10V2KX-4GP
SJM30-CS
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
EMI/Spring/Boss
Size
Document Number
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-2
Date: Thursday, April 08, 2010
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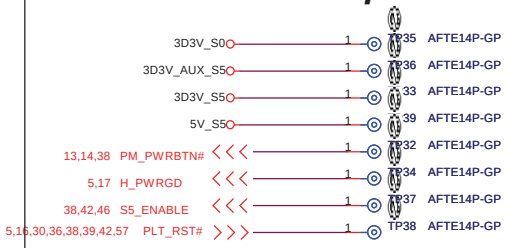
Check test point

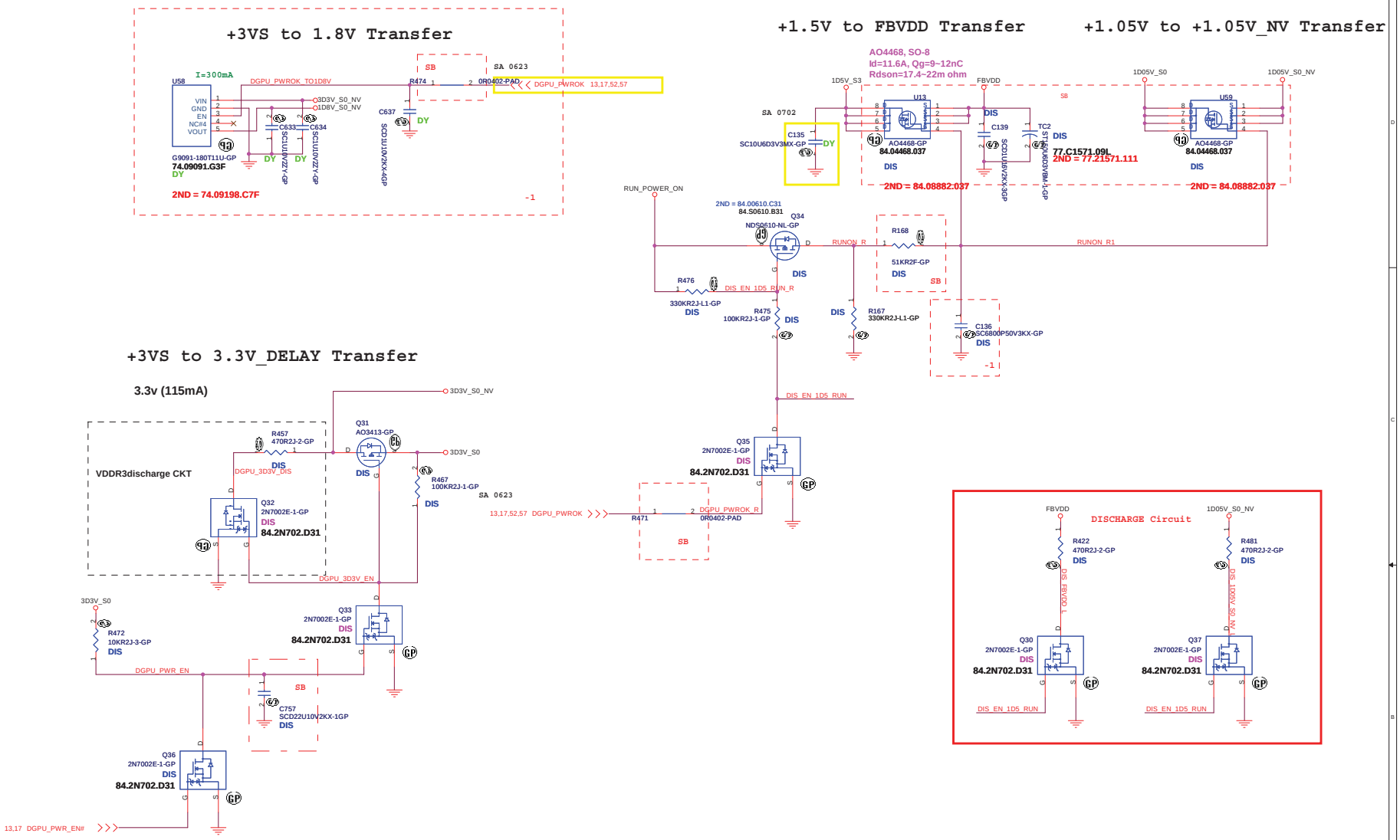


Test Point放在Dimm Door打開可量測處

SJM30-CS

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	AFTE_TP	
Size	Document Number: SJM30-CS	Rev: -2
Date: Tuesday, April 06, 2010	Sheet 55 of 67	


+3VS to 1.8V Transfer
+1.5V to FBVDD Transfer
+1.05V to +1.05V_NV Transfer
+3VS to 3.3V_DELAY Transfer
AO4468, SO-8
Id=11.6A, Qg=9~12nC
Rdson=17.4~22m ohm
I=300mA
U58
G9091-180T11U-GP
74.09091.G3F
2ND = 74.09198.C7F
SA 0623
SA 0702
0R0402-PAD
DGPU_PWROK_TO1D8V
DGPU_PWROK 13,17,52,57
3D3V_S0_NV
1D8V_S0_NV
1D05V_S3
1D05V_S0
1D05V_S0_NV
FBVDD
U13
U59
AO4468-GP
84.04468.037
77.C1571.09L
2ND = 77.21571.111
2ND = 84.08882.037
2ND = 84.08882.037
RUN_POWER_ON
2ND = 84.00610.C31
84.S0610.B31
Q34
NDS0610-NL-GP
RUNON_R
RUNON_R1
R168
51KR2F-GP
R476
330KR2J-L1-GP
DIS_EN_1D5_RUN_R
R475
100KR2J-1-GP
R167
330KR2J-L1-GP
C136
SC6800P50V3KX-GP
DIS_EN_1D5_RUN
Q35
2N7002E-1-GP
84.2N702.D31
VDDR3discharge CKT
3.3v (115mA)
3D3V_S0_NV
3D3V_S0
Q31
AO3413-GP
R457
470R2J-2-GP
R467
100KR2J-1-GP
Q32
2N7002E-1-GP
84.2N702.D31
DGPU_3D3V_DIS
DGPU_3D3V_EN
13,17,52,57 DGPU_PWROK
R471
DGPU_PWROK_R
0R0402-PAD
Q33
2N7002E-1-GP
84.2N702.D31
R472
10KR2J-3-GP
DGPU_PWR_EN
C757
SCD22U10V2KX-1GP
Q36
2N7002E-1-GP
84.2N702.D31
13,17 DGPU_PWR_EN#
DISCHARGE Circuit
R422
470R2J-2-GP
R481
470R2J-2-GP
DIS_FBVDD_L
DIS_1D05V_S0_NV
Q30
2N7002E-1-GP
84.2N702.D31
Q37
2N7002E-1-GP
84.2N702.D31
DIS_EN_1D5_RUN
DIS_EN_1D5_RUN
SJM30-CS
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
NV POWER
SJM30-CS
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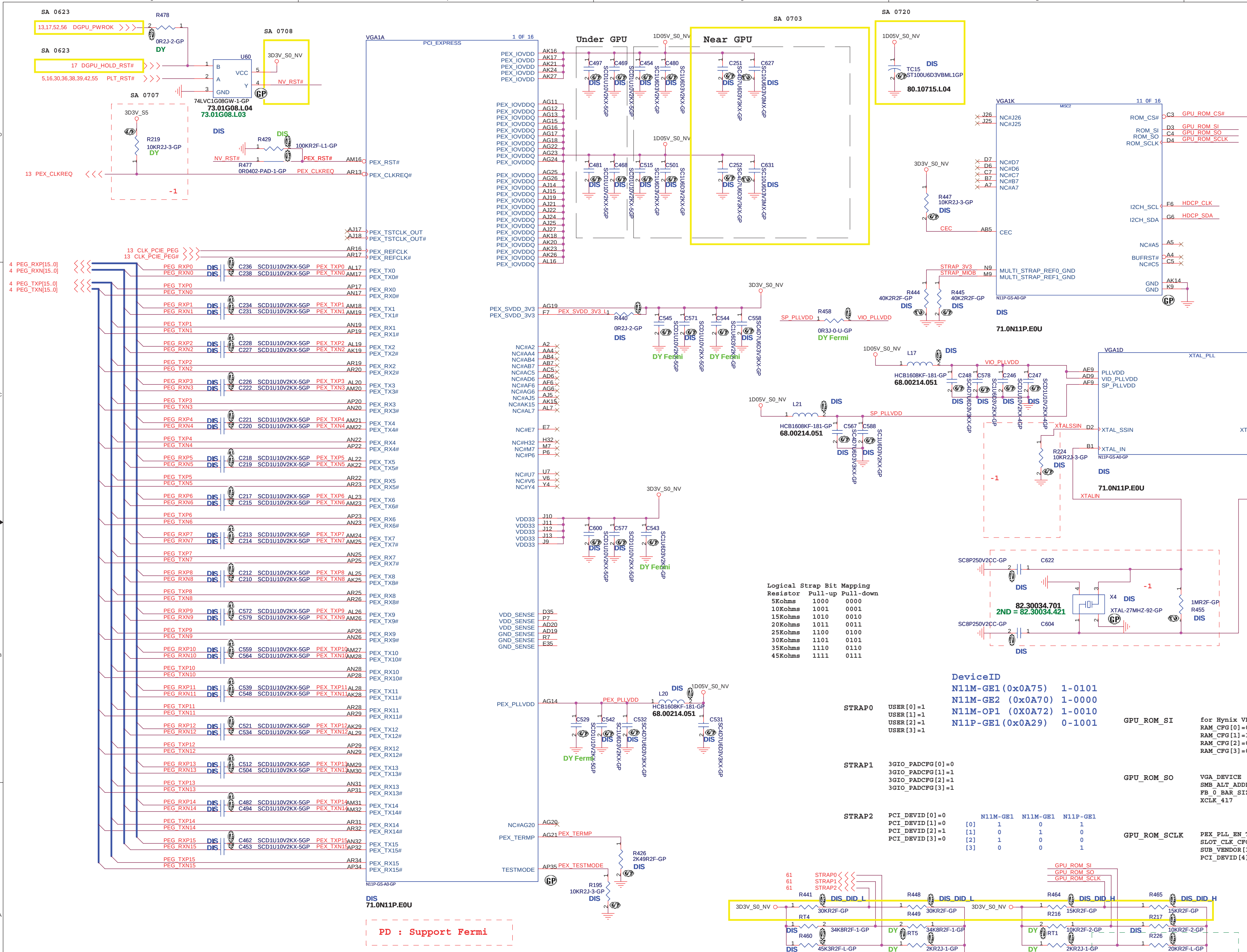

Logical Strap Bit Mapping

Resistor	Pull-up	Pull-down
5Kohms	1000	0000
10Kohms	1001	0001
15Kohms	1010	0010
20Kohms	1011	0011
25Kohms	1100	0100
30Kohms	1101	0101
35Kohms	1110	0110
45Kohms	1111	0111

DeviceID
N11M-GE1(0x0A75) 1-0101
N11M-GE2 (0x0A70) 1-0000
N11M-OP1 (0X0A72) 1-0010
N11P-GE1(0x0A29) 0-1001

STRAP0
USER[0]=1
USER[1]=1
USER[2]=1
USER[3]=1

STRAP1
3GIO_PADCFG[0]=0
3GIO_PADCFG[1]=1
3GIO_PADCFG[2]=1
3GIO_PADCFG[3]=1

STRAP2
PCI_DEVID[0]=0
PCI_DEVID[1]=0
PCI_DEVID[2]=1
PCI_DEVID[3]=0

	N11M-GE1	N11M-GE1	N11P-GE1
[0]	1	0	1
[1]	0	1	0
[2]	1	0	0
[3]	0	0	1

GPU_ROM_SI

for Hynix VRAM	for Samsung VRAM
RAM_CFG[0]=0	RAM_CFG[0]=1
RAM_CFG[1]=1	RAM_CFG[1]=1
RAM_CFG[2]=0	RAM_CFG[2]=0
RAM_CFG[3]=0	RAM_CFG[3]=0

GPU_ROM_SO
VGA_DEVICE =1
SMB_ALT_ADDR =0
PB_0_BAR_SIZE =0
XCLK_417 =0

GPU_ROM_SCLK
PEX_PLL_EN_TERM[1] =0
SLOT_CLK_CFG[2] =1
SUB_VENDOR[3] =0
PCI_DEVID[4] =1

	N11P-GE1	N11M-GE1	N11M-OP1
[4]	0	1	1

N11M-GE1	71.0N11M.E0U
N11M-OP1	71.0N11M.F0U
N11P-GE1	71.0N11P.G0U

STRAP 2: DIS_DID_L
N11M-GE1 R441 = NC, R448 = 30K(64.30025.6DL)
N11M-GE2 R441 = NC, R448 = 4.99K(64.49915.6DL)
N11M-OP1 R441 = NC, R448 = 15K(64.15025.6DL)
N11P-GE1 R441 = 10K(64.10025.6DL), R448 = NC

GPU_ROM_SCLK: DIS_DID_H
N11M-GE1 R464 = 15K(64.15025.6DL), R465 = NC
N11M-GE2 R464 = 15K(64.15025.6DL), R465 = NC
N11M-OP1 R464 = 15K(64.15025.6DL), R465 = NC
N11P-GE1 R464 = NC, R465 = 15K(64.15025.6DL)

R226
HYNIX-->15K(64.15025.6DL)
SAMSUNG-->20K(64.20025.6DL)

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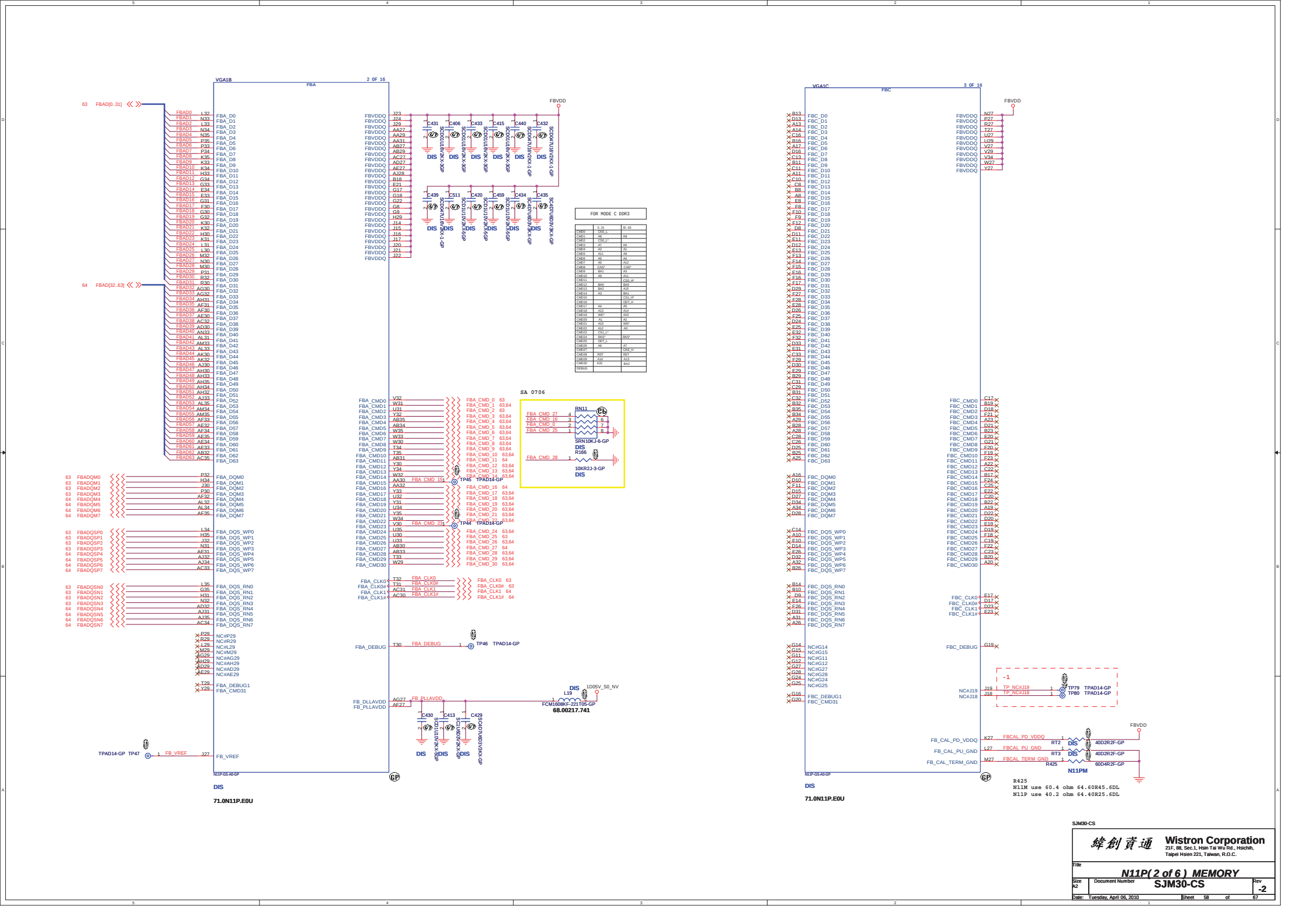
VGA1B
FBA
2 OF 16
FBVDD
FOR MODE C DDR3
SA 0706
RN11
SRN10KJ-6-GP
R166
10KR2J-3-GP
DIS
VGA1C
FBC
3 OF 16
71.0N11P.E0U
N11P-GS-A0-GP
N11PM
R425
N11M use 60.4 ohm 64.60R45.6DL
N11P use 40.2 ohm 64.40R25.6DL
SJM30-CS
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Taipei Hsien 221, Taiwan, R.O.C.
N11P(2 of 6) MEMORY
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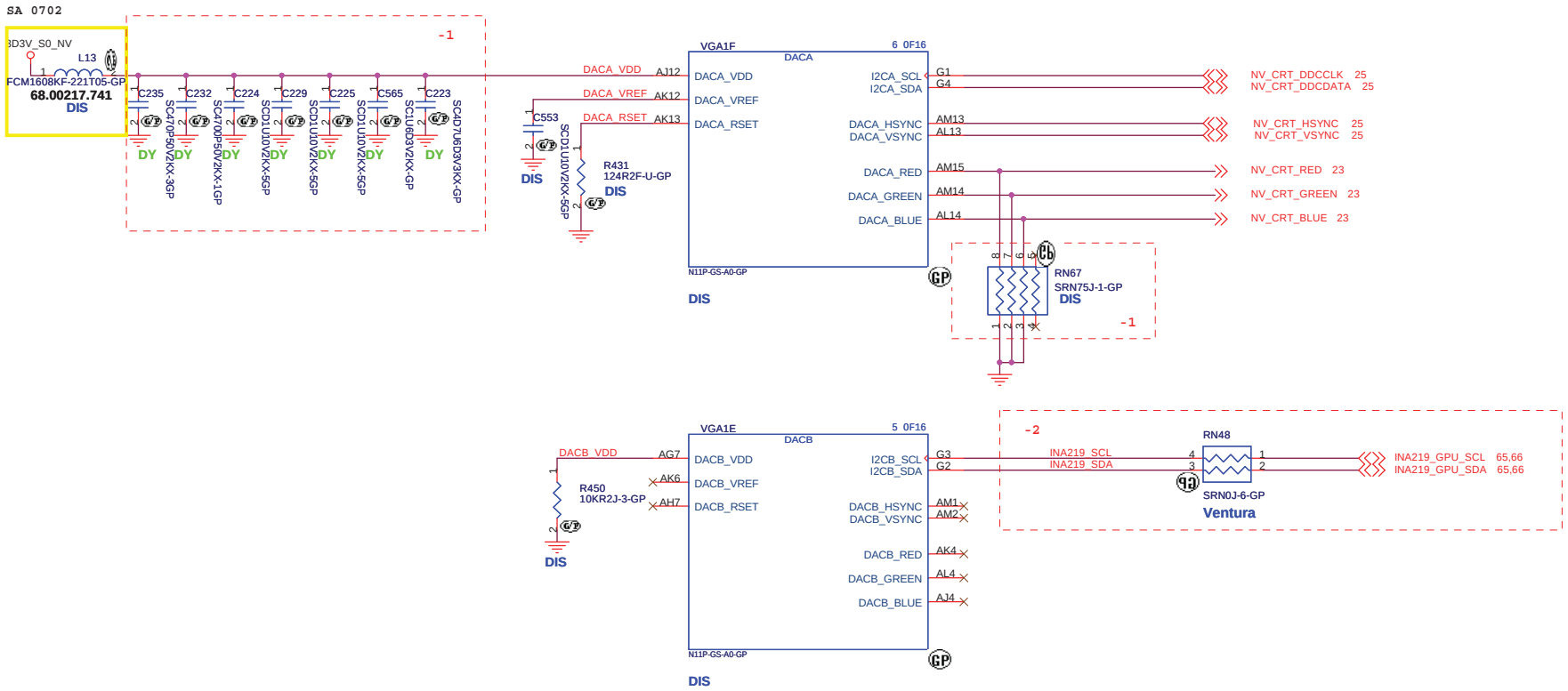

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Title: ***N11P(3 of 6)_DAC***

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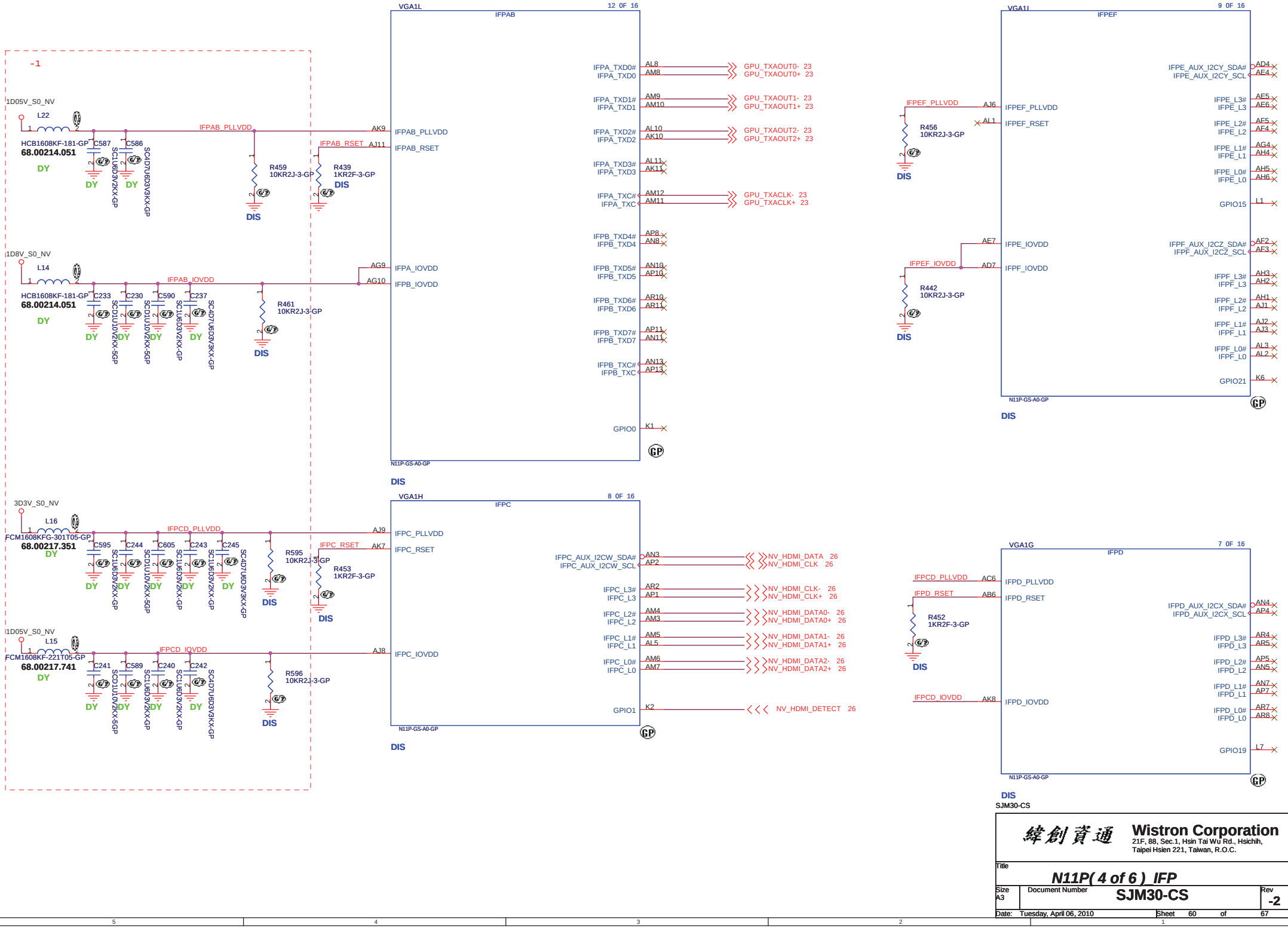
-1
1D05V_S0_NV
L22
HCB1608KF-181-GP
68.00214.051
DY
C587
C586
SC1U6D3V2KX-GP
SC47U6D3V3KX-GP
IFPAB_PLLVDD
AK9
R459
10KR2J-3-GP
DIS
IFPAB_RSET
AJ11
R439
1KR2F-3-GP
1D8V_S0_NV
L14
IFPAB_IOVDD
AG9
AG10
C233
C230
C590
C237
SC1U10V2KX-5GP
R461
10KR2J-3-GP
3D3V_S0_NV
L16
FCM1608KFG-301T05-GP
68.00217.351
IFPCD_PLLVDD
AJ9
C595
C244
C605
C243
C245
SC47U6D3V3KX-GP
R595
10KR2J-3-GP
IFPC_RSET
AK7
R453
1KR2F-3-GP
1D05V_S0_NV
L15
FCM1608KF-221T05-GP
68.00217.741
IFPCD_IOVDD
AJ8
C241
C589
C240
C242
R596
10KR2J-3-GP
VGA1L
12 OF 16
IFPAB
IFPAB_PLLVDD
IFPAB_RSET
IFPA_IOVDD
IFPB_IOVDD
IFPA_TXD0#
IFPA_TXD0
IFPA_TXD1#
IFPA_TXD1
IFPA_TXD2#
IFPA_TXD2
IFPA_TXD3#
IFPA_TXD3
IFPA_TXC#
IFPA_TXC
IFPB_TXD4#
IFPB_TXD4
IFPB_TXD5#
IFPB_TXD5
IFPB_TXD6#
IFPB_TXD6
IFPB_TXD7#
IFPB_TXD7
IFPB_TXC#
IFPB_TXC
GPIO0
K1
AL8
AM8
AM9
AM10
AL10
AK10
AL11
AK11
AM12
AM11
AP8
AN8
AN10
AP10
AR10
AR11
AP11
AN11
AN13
AP13
GPU_TXAOUT0- 23
GPU_TXAOUT0+ 23
GPU_TXAOUT1- 23
GPU_TXAOUT1+ 23
GPU_TXAOUT2- 23
GPU_TXAOUT2+ 23
GPU_TXACLK- 23
GPU_TXACLK+ 23
N11P-GS-A0-GP
DIS
VGA1H
8 OF 16
IFPC
IFPC_PLLVDD
IFPC_RSET
IFPC_IOVDD
IFPC_AUX_I2CW_SDA#
IFPC_AUX_I2CW_SCL
IFPC_L3#
IFPC_L3
IFPC_L2#
IFPC_L2
IFPC_L1#
IFPC_L1
IFPC_L0#
IFPC_L0
GPIO1
K2
AN3
AP2
AR2
AP1
AM4
AM3
AM5
AL5
AM6
AM7
NV_HDMI_DATA 26
NV_HDMI_CLK 26
NV_HDMI_CLK- 26
NV_HDMI_CLK+ 26
NV_HDMI_DATA0- 26
NV_HDMI_DATA0+ 26
NV_HDMI_DATA1- 26
NV_HDMI_DATA1+ 26
NV_HDMI_DATA2- 26
NV_HDMI_DATA2+ 26
NV_HDMI_DETECT 26
N11P-GS-A0-GP
DIS
VGA1I
9 OF 16
IFPEF
IFPEF_PLLVDD
IFPEF_RSET
IFPE_IOVDD
IFPF_IOVDD
IFPE_AUX_I2CY_SDA#
IFPE_AUX_I2CY_SCL
IFPE_L3#
IFPE_L3
IFPE_L2#
IFPE_L2
IFPE_L1#
IFPE_L1
IFPE_L0#
IFPE_L0
GPIO15
L1
IFPF_AUX_I2CZ_SDA#
IFPF_AUX_I2CZ_SCL
IFPF_L3#
IFPF_L3
IFPF_L2#
IFPF_L2
IFPF_L1#
IFPF_L1
IFPF_L0#
IFPF_L0
GPIO21
K6
AJ6
AL1
AE7
AD7
AD4
AE4
AE5
AE6
AE5
AF4
AG4
AH4
AH5
AH6
AF2
AF3
AH3
AH2
AH1
AJ1
AJ2
AJ3
AL3
AL2
R456
10KR2J-3-GP
R442
10KR2J-3-GP
N11P-GS-A0-GP
DIS
VGA1G
7 OF 16
IFPD
IFPD_PLLVDD
IFPD_RSET
IFPD_IOVDD
IFPD_AUX_I2CX_SDA#
IFPD_AUX_I2CX_SCL
IFPD_L3#
IFPD_L3
IFPD_L2#
IFPD_L2
IFPD_L1#
IFPD_L1
IFPD_L0#
IFPD_L0
GPIO19
L7
AC6
AB6
AK8
AN4
AP4
AR4
AR5
AP5
AN5
AN7
AP7
AR7
AR8
R452
1KR2F-3-GP
N11P-GS-A0-GP
DIS
SJM30-CS
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Title
N11P(4 of 6)_IFP
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A3
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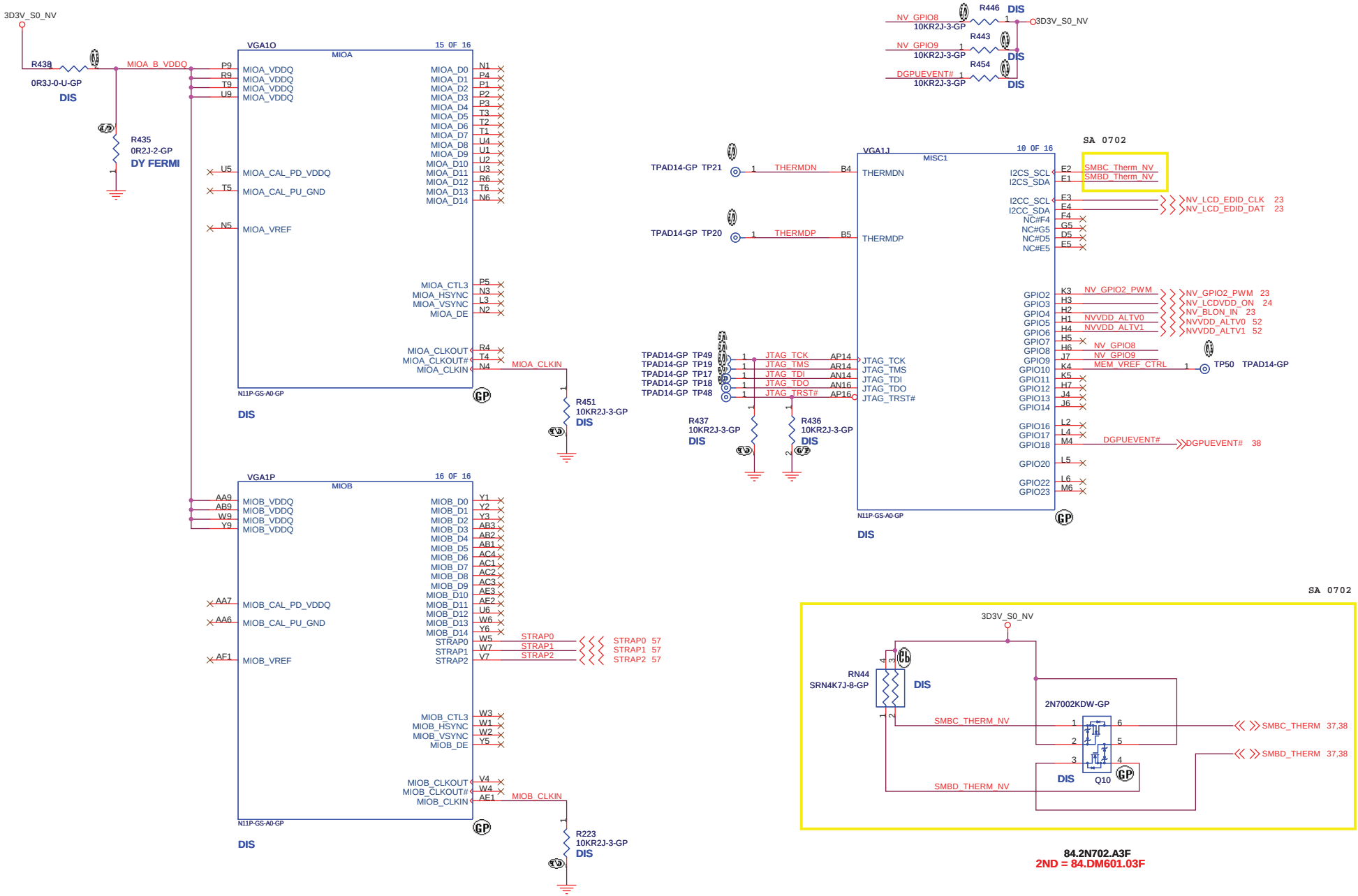

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Title: ***N11P(5 of 6)_MIO/ GPIO***

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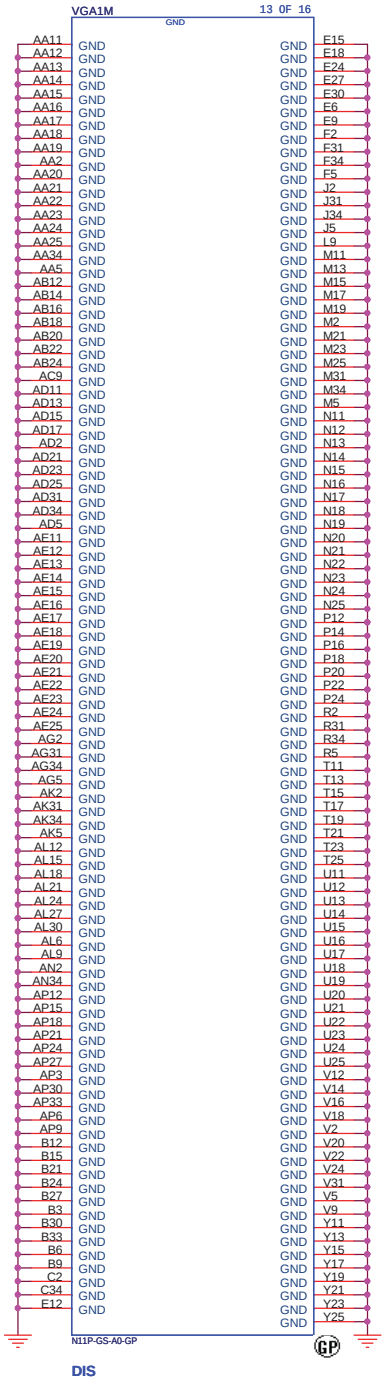

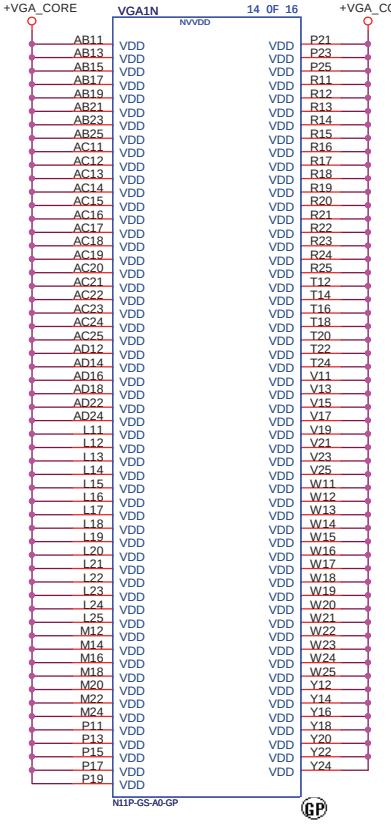

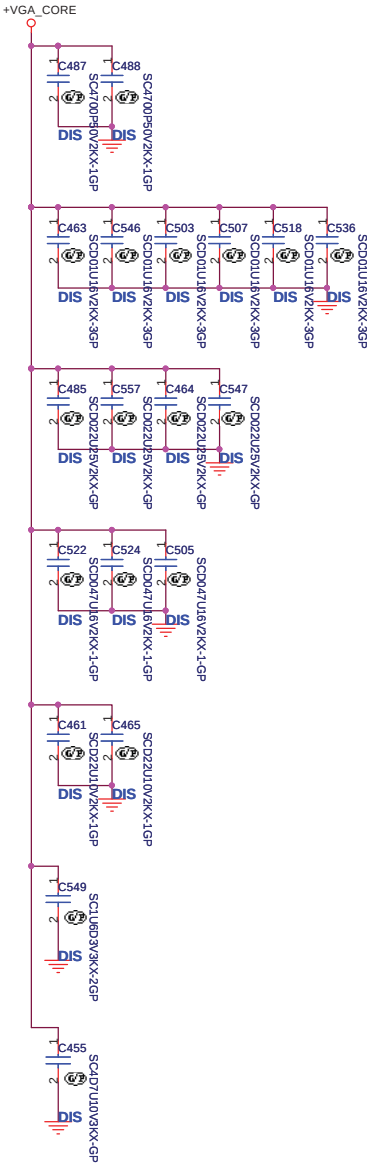

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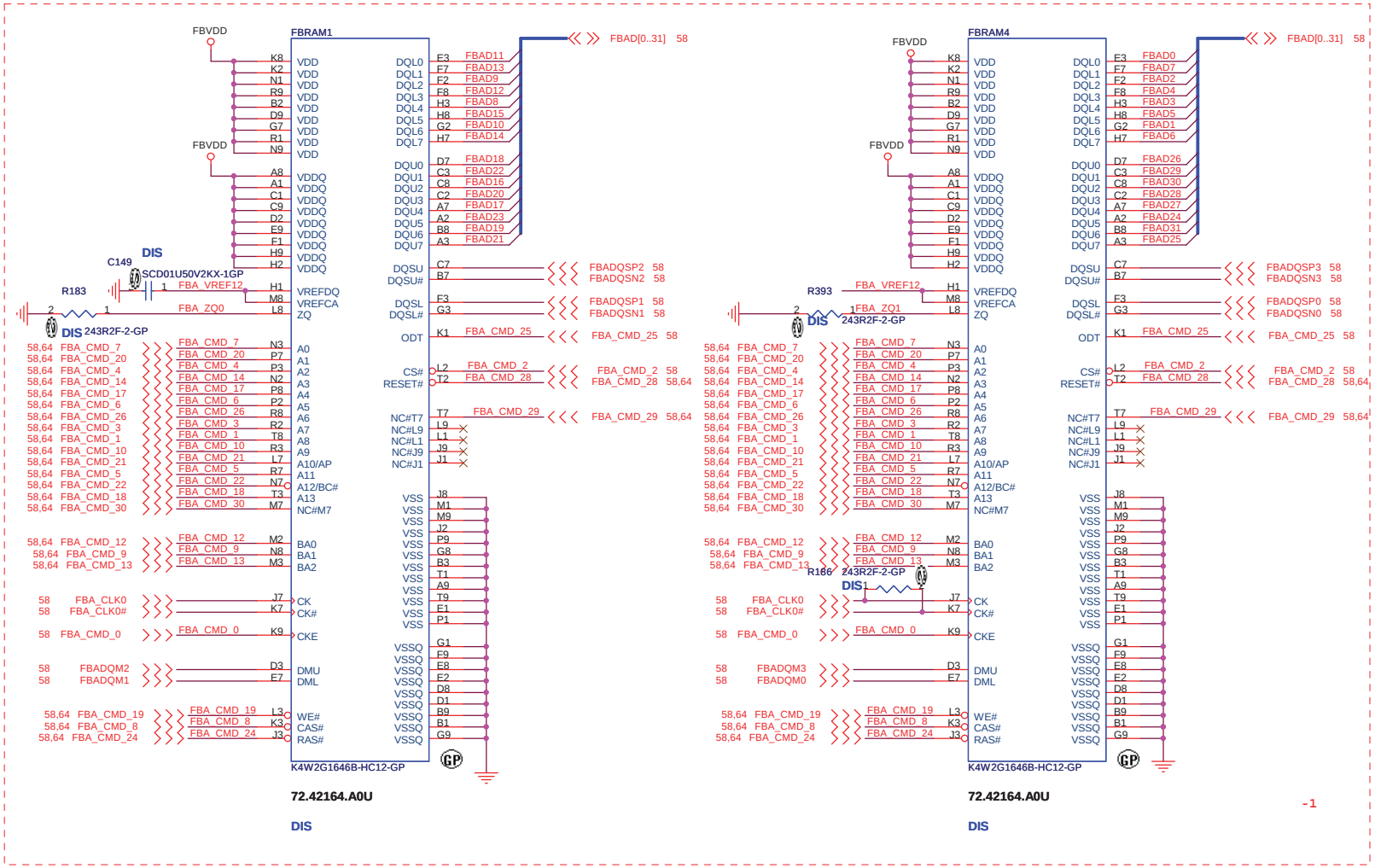

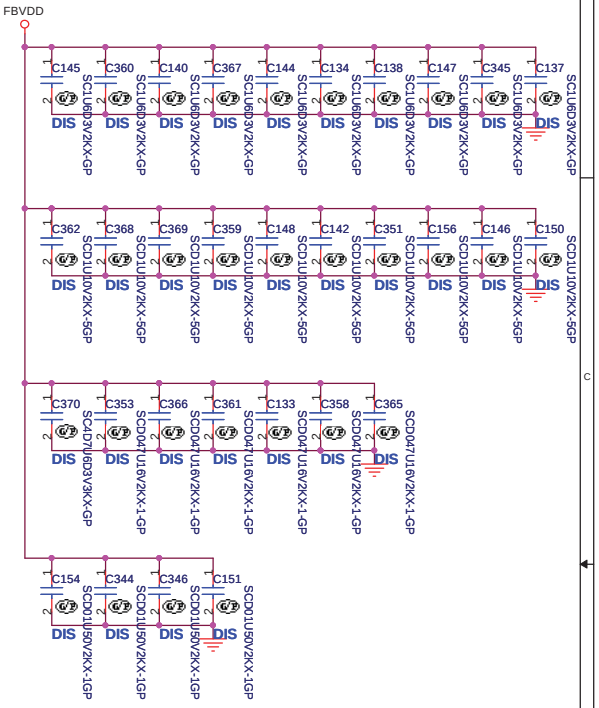

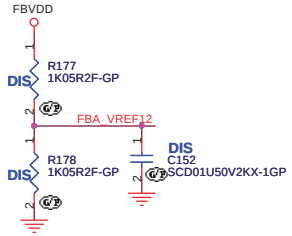

GDDR3 VRAM :
64Mx16
Samsung 72.41164.H0U K4W1G1646E-HC12 13.3 x 7.5 mm
Hynix 72.51G63.C0U H5TQ1G63BFR-12C 13.0 x 7.5 mm
128Mx16
Samsung 72.42164.A0U K4W2G1646B-HC12 13.3 x 9 mm

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Title: VRAM (1 of 4)

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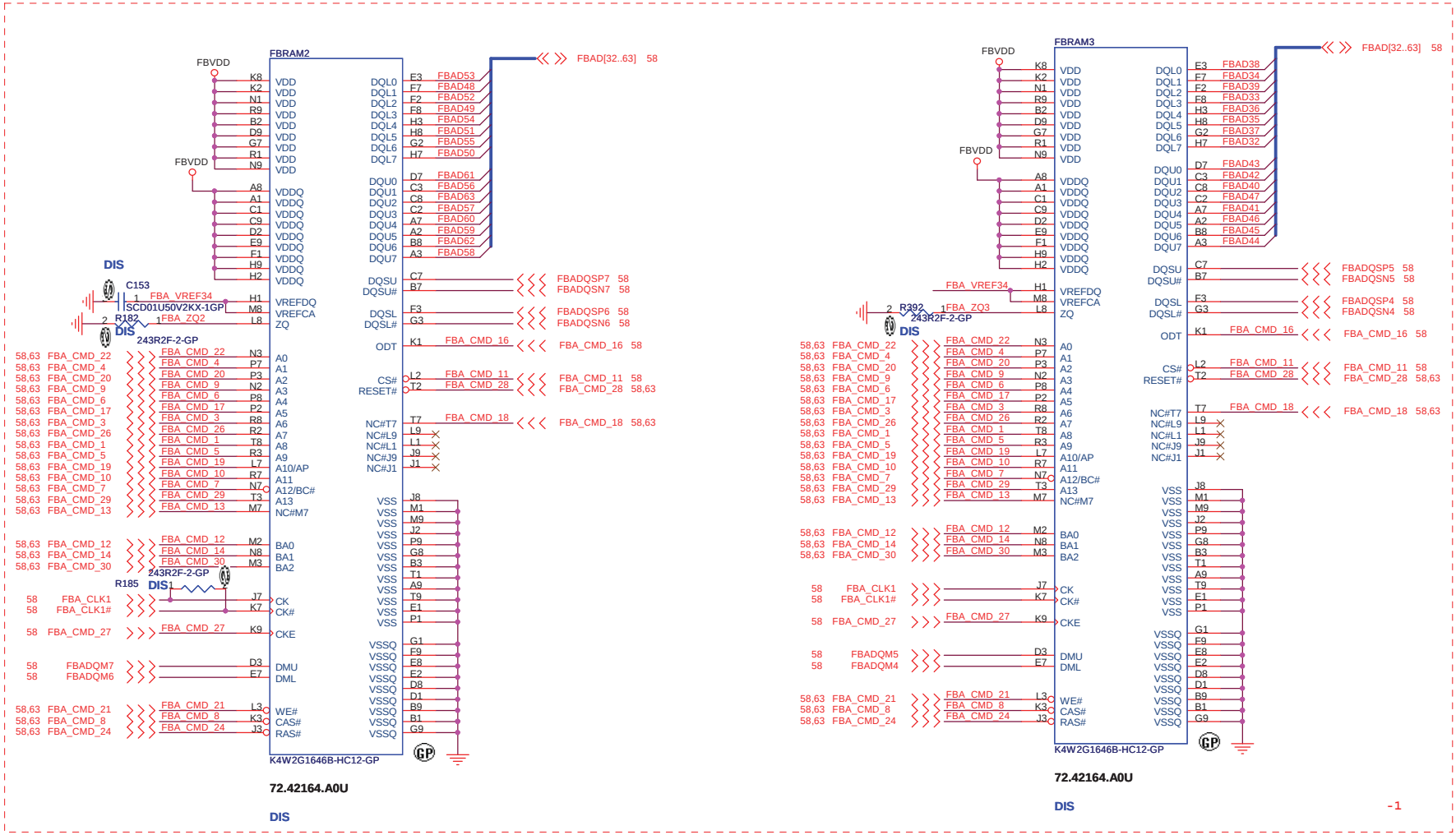

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Title	**VRAM (2 of 4)**	
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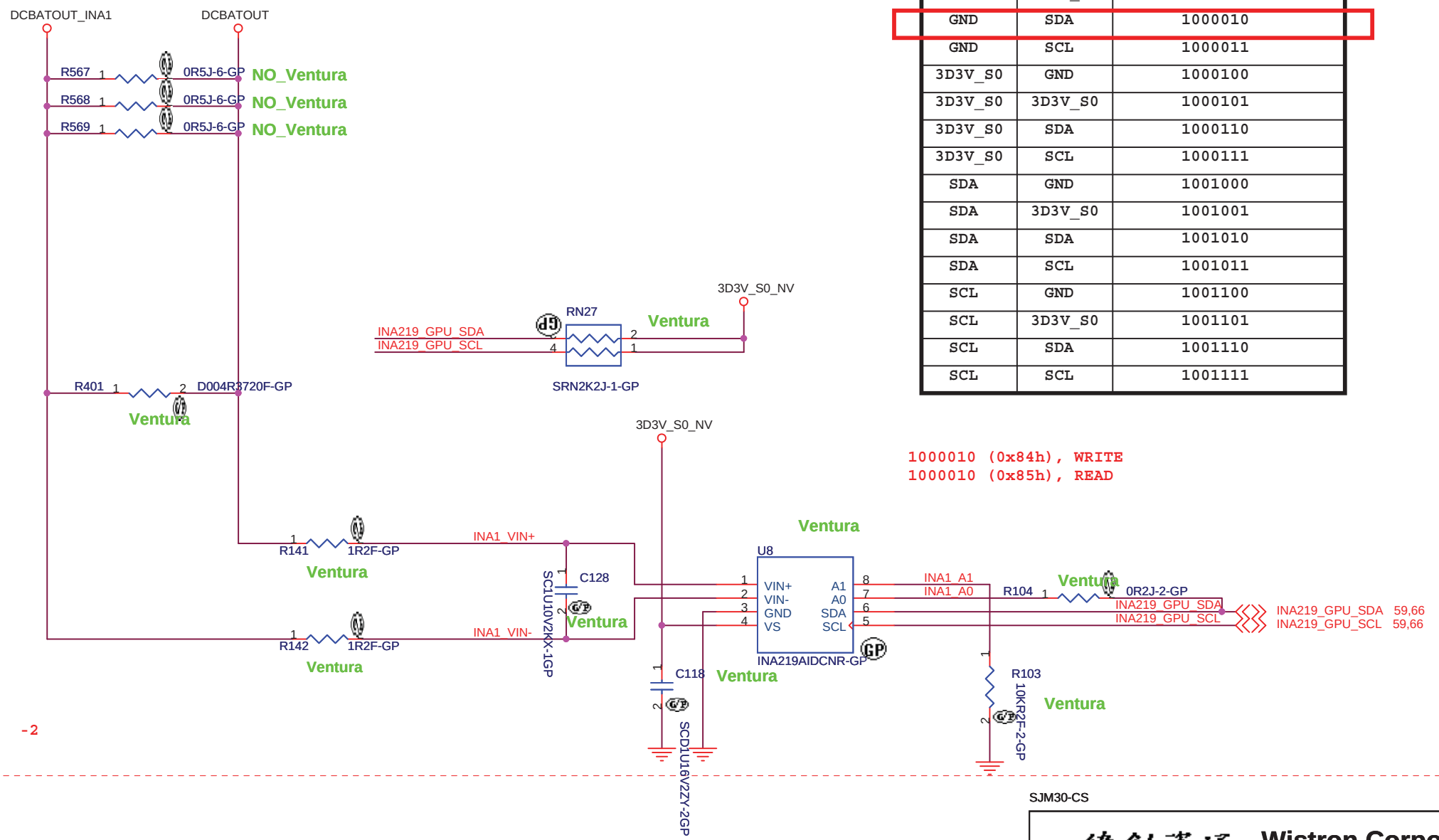
A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	3D3V_S0	1000001
GND	SDA	1000010
GND	SCL	1000011
3D3V_S0	GND	1000100
3D3V_S0	3D3V_S0	1000101
3D3V_S0	SDA	1000110
3D3V_S0	SCL	1000111
SDA	GND	1001000
SDA	3D3V_S0	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	3D3V_S0	1001101
SCL	SDA	1001110
SCL	SCL	1001111



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Title	INA219_CPU	
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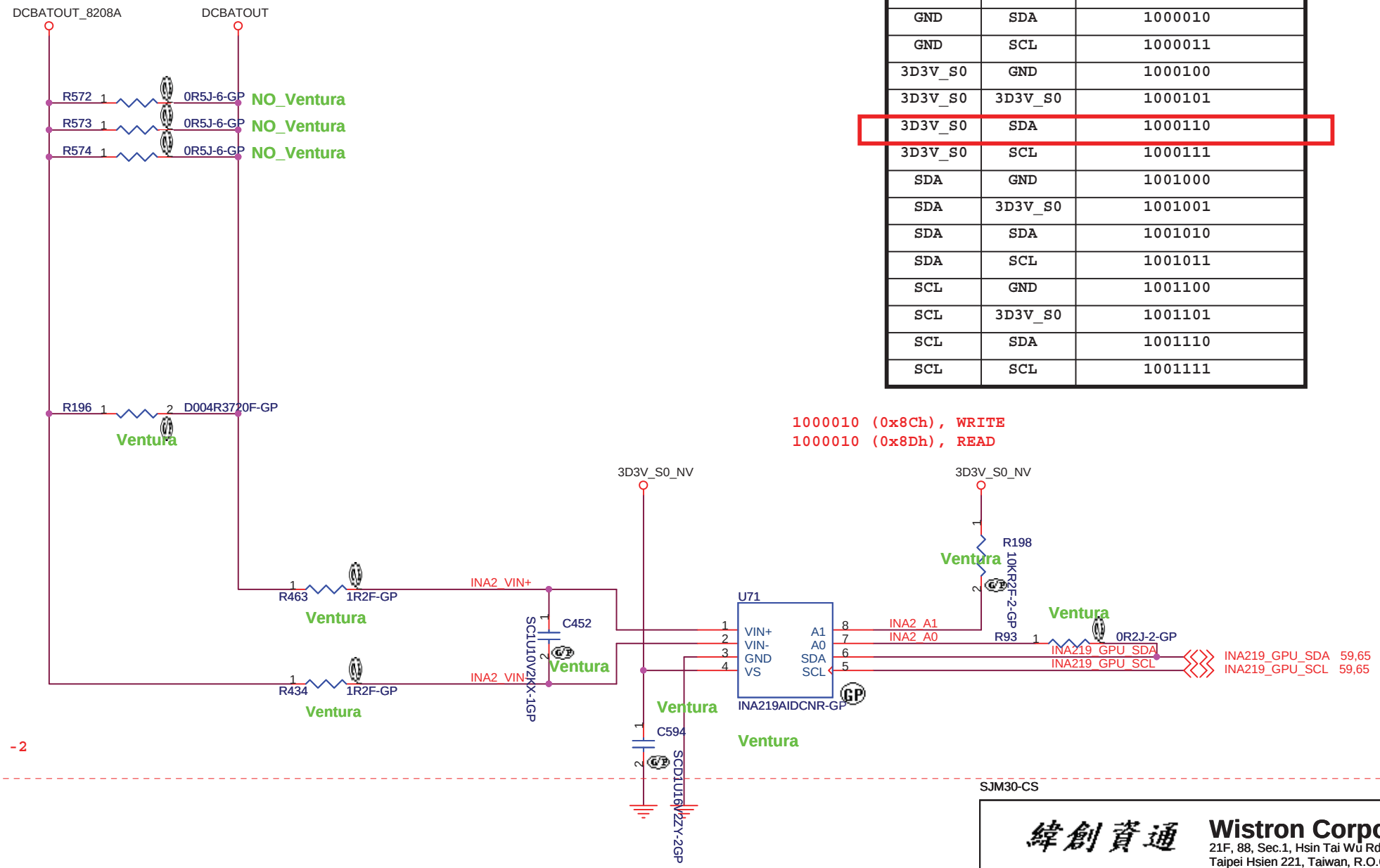
A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	3D3V_S0	1000001
GND	SDA	1000010
GND	SCL	1000011
3D3V_S0	GND	1000100
3D3V_S0	3D3V_S0	1000101
3D3V_S0	SDA	1000110
3D3V_S0	SCL	1000111
SDA	GND	1001000
SDA	3D3V_S0	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	3D3V_S0	1001101
SCL	SDA	1001110
SCL	SCL	1001111



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Title: INA219_GPU

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Title: **Modify History**

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