

MODEL NAME : *RANGER 17*
PCB NO : *LA-9331P*
BOM P/N : *4619KL31L01*

Compal Confidential

RANGER 17

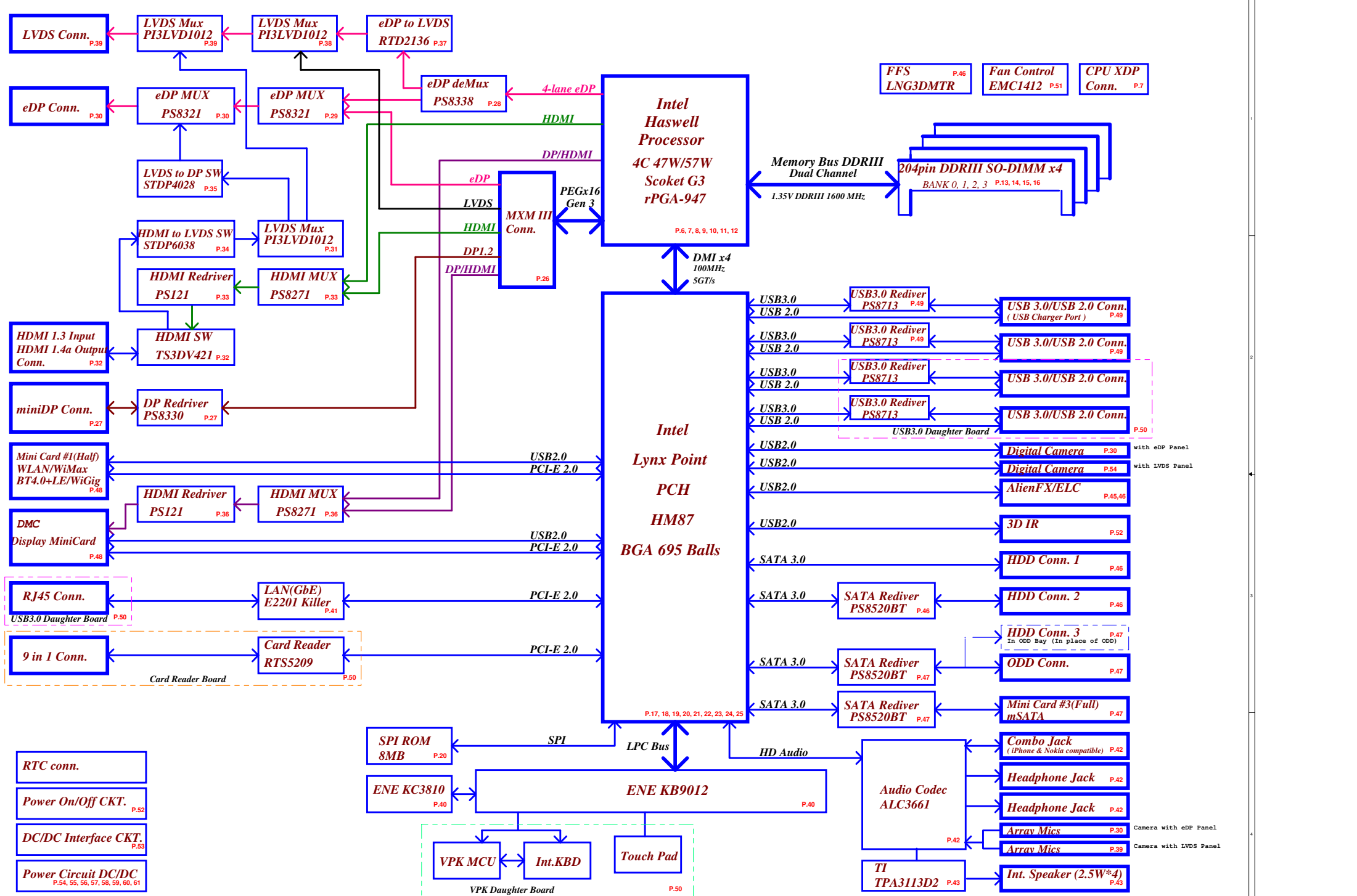
Schematic Document

Rev: X00

2012-06-22

@ : Nopop Component

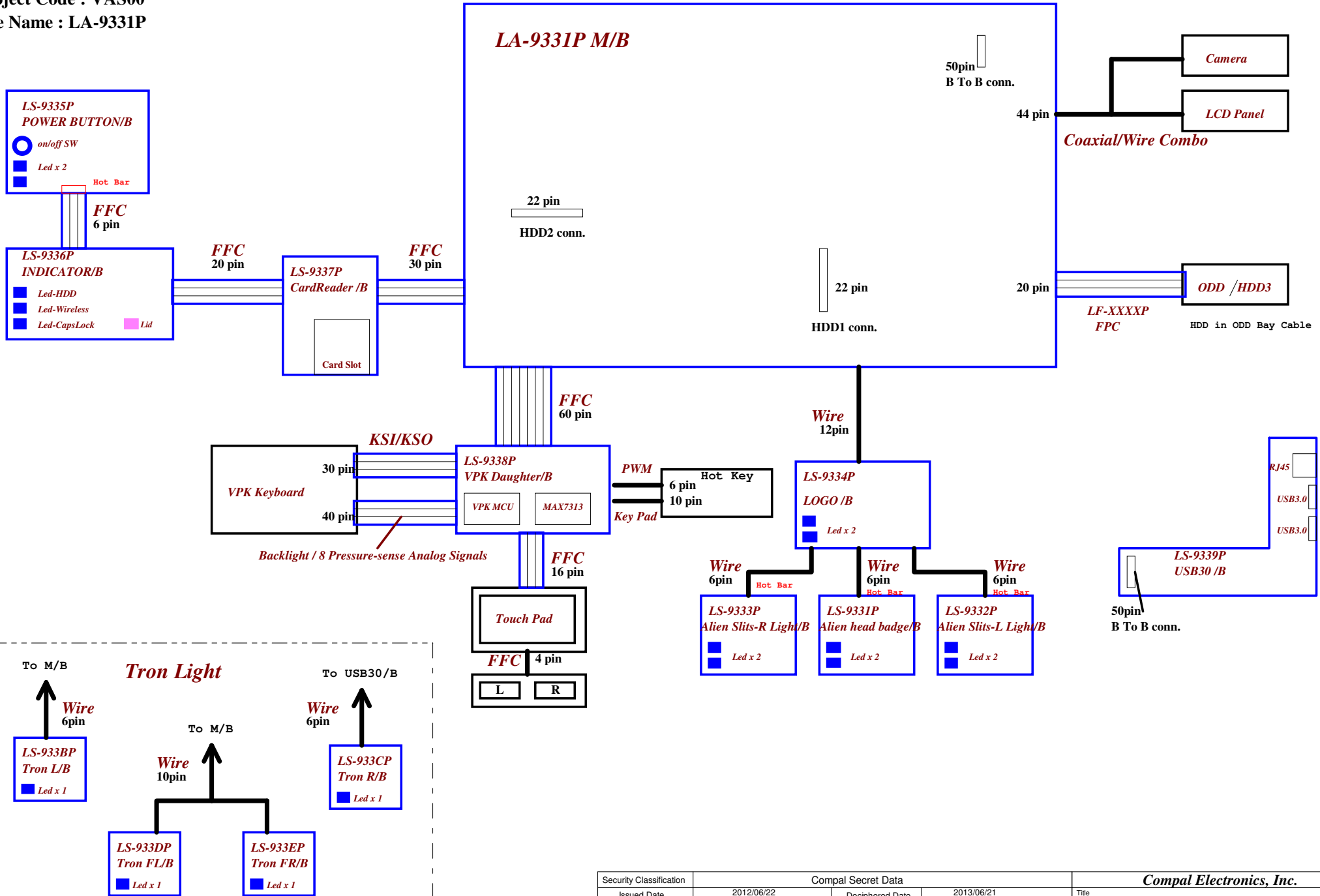
Security Classification	Compal Secret Data			Title <i>Compal Electronics, Inc.</i>	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title <i>Cover Sheet</i>	
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Project Code : VAS00

File Name : LA-9331P



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Board ID Table for AD channel

Vcc	3.3V +/- 5%				
Ra	100K +/- 5%				
Board ID	Rb	VAD_BID min	VAD_BID typ	VAD_BID max	EC AD3
0	0	0 V	0 V	0.155 V	0x00-0x0C
1	8.2K +/- 5%	0.168 V	0.250 V	0.362 V	0x0D-0x1C
2	18K +/- 5%	0.375 V	0.503 V	0.621 V	0x1D-0x30
3	33K +/- 5%	0.634 V	0.819 V	0.945 V	0x31-0x49
4	56K +/- 5%	0.958 V	1.185 V	1.359 V	0x4A-0x69
5	100K +/- 5%	1.372 V	1.650 V	1.838 V	0x6A-0x8E
6	200K +/- 5%	1.851 V	2.200 V	2.420 V	0x8F-0xBB
7	NC	2.433 V	3.300 V	3.300 V	0xBC-0xFF

BOARD ID Table

Board ID	PCB Revision
0	0.1 (SSI)
1	0.2 (PT)
2	0.3 (ST)
3	0.4 (OT)
4	1.0 (MP)
5	
6	
7	

USB 3.0 PORT	Connction
1	JUSB1 (Left side)
2	JUSB2 (Left side)
3	NA
4	NA
5	JUSB3 (Right side)
6	JUSB4 (Right side)

USB PORT#	DESTINATION
0	JUSB1(USB3.0 P1)
1	JUSB2(USB3.0 P2)
2	JUSB3(USB3.0 P5)
3	JUSB4(USB3.0 P6)
4	JMINI1 (WLAN)
5	JMINI2 (DMC)
6	AlienFX/ELC
7	IR SENSOR
8	None
9	None
10	None
11	eDP CAMERA
12	LVDS CAMERA
13	VPK K/B

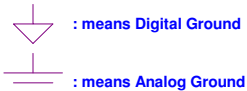
POWER STATES

State	Signal	SLP S3#	SLP S4#	SLP S5#	S4 STATE#	SLP M#	ALWAYS PLANE	SUS PLANE	RUN PLANE	CLOCKS
S0 (Full ON) / M0		HIGH	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S3 (Suspend to RAM) / M-OFF		LOW	HIGH		HIGH	LOW	ON	ON	OFF	OFF
S4 (Suspend to DISK) / M-OFF		LOW	LOW	HIGH	LOW	LOW	ON	OFF	OFF	OFF
S5 (SOFT OFF) / M-OFF		LOW	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

PM TABLE

State	power plane	+5VALW +3VALW +3VLP +3V_PCH	+1.35V +1.05V	+5VS +3VS +1.5VS +1.05VS +0.675VS +3VMXM +5VMXM +VCC_CORE +1.35V_CPU_VDDQ
S0		ON	ON	ON
S3		ON	ON	OFF
S5 S4/AC		ON	OFF	OFF
S5 S4/AC don't exist		OFF	OFF	OFF

Symbol Note :



CLK	DIFFERENTIAL	DESTINATION	FLEX CLOCKS	DESTINATION
	CLKOUT_PCIE0	MINI CARD-1 WLAN	CLKOUTFLEX0	None
	CLKOUT_PCIE1	MINI CARD-2 DMC	CLKOUTFLEX1	None
	CLKOUT_PCIE2	10/100/1G LAN	CLKOUTFLEX2	None
	CLKOUT_PCIE3	CARD READER	CLKOUTFLEX3	None
	CLKOUT_PCIE4	None		
	CLKOUT_PCIE5	None		
	CLKOUT_PCIE6	None		
	CLKOUT_PCIE7	None		
CLKOUT_PEG_A	MXM			

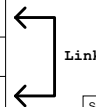
CLKOUT	DESTINATION
PCI0	PCH_LOOPBACK
PCI1	EC
PCI2	80port debug card
PCI3	None
PCI4	None

SATAIII	DESTINATION
SATA0	HDD1
SATA1	HDD2
SATA2	ODD
SATA3	mSATA
SATA4/PCIE LANE1	MINI CARD-1 WLAN
SATA5/PCIE LANE2	MINI CARD-2 DMC

PCI EXPRESS	DESTINATION
Lane 1/USB3.0 Port 3	None
Lane 2/USB3.0 Port 4	None
Lane 3	10/100/1G LAN
Lane 4	CARD READER
Lane 5	None
Lane 6	None
Lane 7	None
Lane 8	None

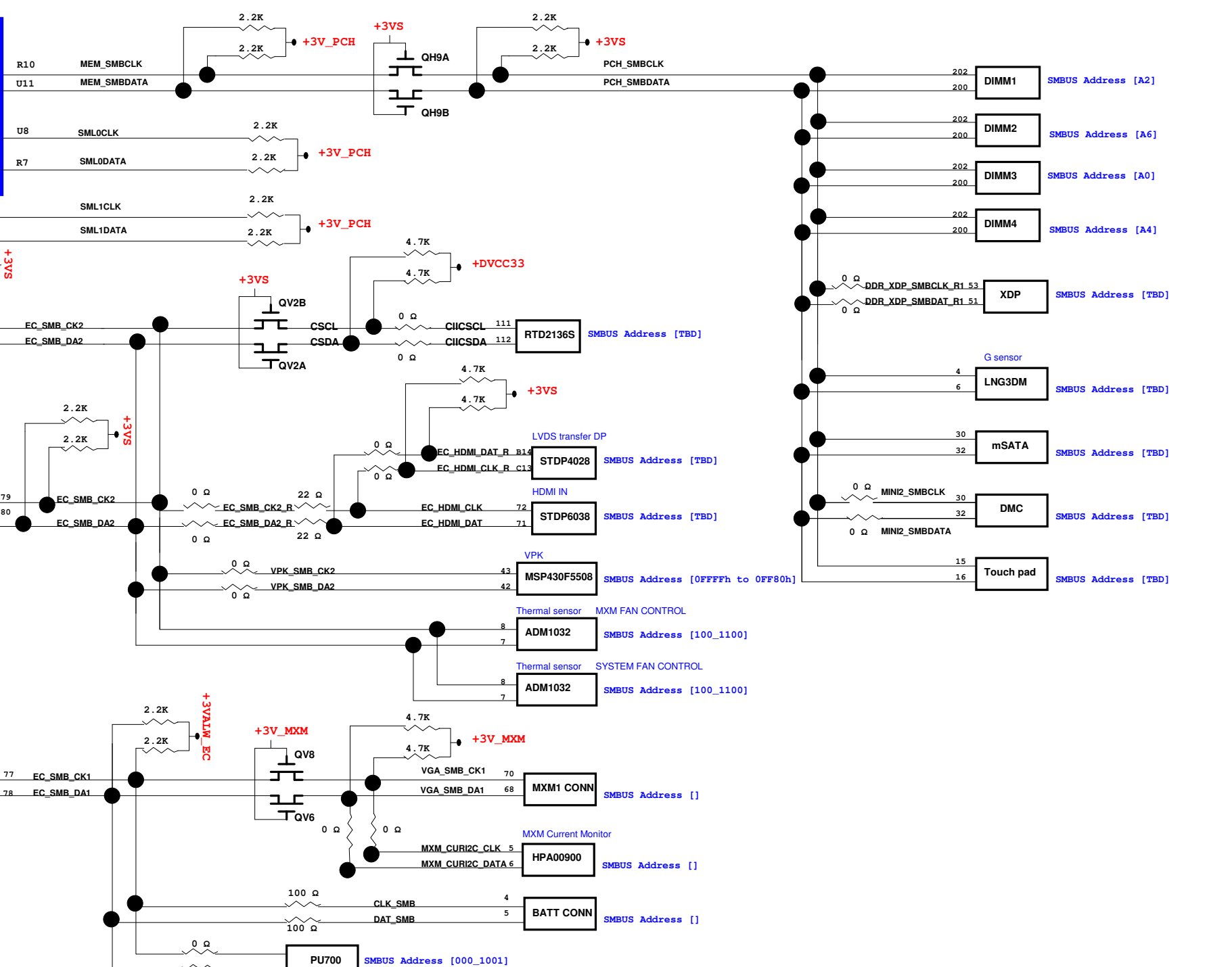
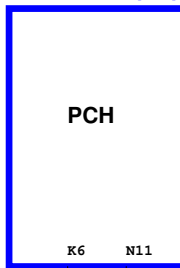
SMBUS Control Table

	SOURCE	WLAN	DMC	BATT	DIMM	6038	4028	Thermal Sensor	FFS	2136	VPK MCU	MXM	XDP	Charger	TP	mSATA
EC_SMB_CK1 EC_SMB_DA1	KB9012			✓								✓		✓		
EC_SMB_CK2 EC_SMB_DA2	KB9012				✓	✓	✓			✓	✓					
PCH_SML0CLK PCH_SML0DATA	PCH															
PCH_SML1CLK PCH_SML1DATA	PCH															
MEM_SMBCLK MEM_SMBDATA	PCH		✓		✓				✓			✓		✓	✓	



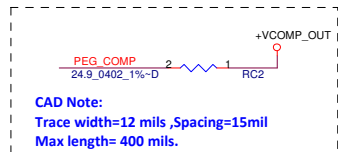
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SMBUS Address [TBD]



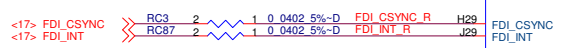
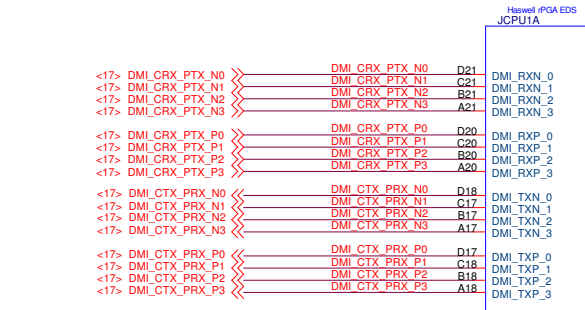
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SMBus block diagram



CAD Note:
Trace width=12 mils ,Spacing=15mil
Max length= 400 mils.

PEG_GTX_HRX_P10..15] <-29>
PEG_GTX_HRX_N10..15] <-29>
PEG_HTX_C_GRX_P10..15] <-29>
PEG_HTX_C_GRX_N10..15] <-29>



Component	Value	Part Number	Quantity	Notes	Location
E23	PEG_COMP				
M29	PEG GTX C HRX N0	CC1	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N0
K28	PEG GTX C HRX N1	CC2	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N1
M31	PEG GTX C HRX N2	CC3	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N2
L30	PEG GTX C HRX N3	CC4	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N3
M33	PEG GTX C HRX N4	CC5	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N4
L32	PEG GTX C HRX N5	CC13	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N5
M35	PEG GTX C HRX N6	CC6	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N6
L34	PEG GTX C HRX N7	CC7	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N7
E29	PEG GTX C HRX N8	CC8	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N8
D28	PEG GTX C HRX N9	CC9	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N9
E31	PEG GTX C HRX N10	CC10	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N10
D31	PEG GTX C HRX N11	CC11	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N11
E35	PEG GTX C HRX N12	CC12	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N12
D34	PEG GTX C HRX N13	CC14	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N13
E33	PEG GTX C HRX N14	CC15	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N14
E32	PEG GTX C HRX N15	CC16	1	2 0.22U 0402 16V7K-D	PEG GTX HRX N15
L29	PEG GTX C HRX P0	CC17	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P0
L28	PEG GTX C HRX P1	CC18	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P1
L31	PEG GTX C HRX P2	CC19	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P2
K30	PEG GTX C HRX P3	CC20	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P3
L33	PEG GTX C HRX P4	CC21	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P4
K32	PEG GTX C HRX P5	CC22	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P5
L35	PEG GTX C HRX P6	CC23	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P6
K34	PEG GTX C HRX P7	CC24	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P7
F29	PEG GTX C HRX P8	CC25	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P8
E28	PEG GTX C HRX P9	CC26	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P9
F31	PEG GTX C HRX P10	CC27	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P10
E30	PEG GTX C HRX P11	CC28	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P11
F35	PEG GTX C HRX P12	CC29	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P12
E34	PEG GTX C HRX P13	CC30	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P13
F33	PEG GTX C HRX P14	CC31	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P14
D32	PEG GTX C HRX P15	CC32	1	2 0.22U 0402 16V7K-D	PEG GTX HRX P15
H35	PEG HTX GRX N0	CC33	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N0
H34	PEG HTX GRX N1	CC34	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N1
I33	PEG HTX GRX N2	CC35	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N2
H32	PEG HTX GRX N3	CC36	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N3
J31	PEG HTX GRX N4	CC37	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N4
C30	PEG HTX GRX N5	CC38	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N5
C33	PEG HTX GRX N6	CC39	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N6
B32	PEG HTX GRX N7	CC40	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N7
B31	PEG HTX GRX N8	CC41	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N8
A30	PEG HTX GRX N9	CC42	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N9
B29	PEG HTX GRX N10	CC43	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N10
A28	PEG HTX GRX N11	CC44	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N11
B27	PEG HTX GRX N12	CC45	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N12
A26	PEG HTX GRX N13	CC46	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N13
B25	PEG HTX GRX N14	CC47	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N14
A24	PEG HTX GRX N15	CC48	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX N15
J35	PEG HTX GRX P0	CC49	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P0
G34	PEG HTX GRX P1	CC50	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P1
H33	PEG HTX GRX P2	CC51	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P2
G32	PEG HTX GRX P3	CC52	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P3
H31	PEG HTX GRX P4	CC53	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P4
H30	PEG HTX GRX P5	CC54	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P5
B33	PEG HTX GRX P6	CC55	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P6
A32	PEG HTX GRX P7	CC56	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P7
C31	PEG HTX GRX P8	CC57	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P8
B30	PEG HTX GRX P9	CC58	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P9
C29	PEG HTX GRX P10	CC59	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P10
B28	PEG HTX GRX P11	CC60	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P11
C27	PEG HTX GRX P12	CC61	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P12
B26	PEG HTX GRX P13	CC62	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P13
C25	PEG HTX GRX P14	CC63	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P14
B24	PEG HTX GRX P15	CC64	1	2 0.22U 0402 16V7K-D	PEG HTX C GRX P15

Near MXM Connector

INTEL_HASWELL_HASWELL

CONN@

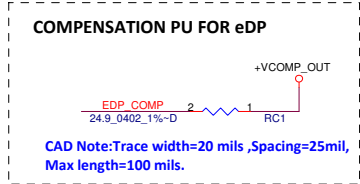
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CPU (I7) DMI,PEG

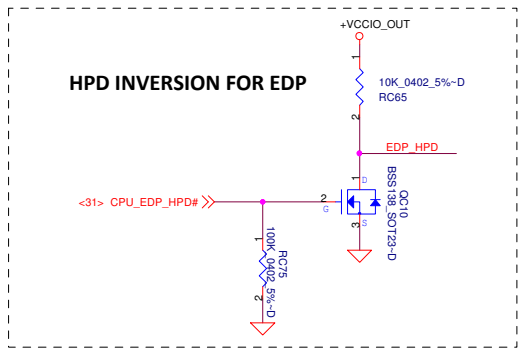
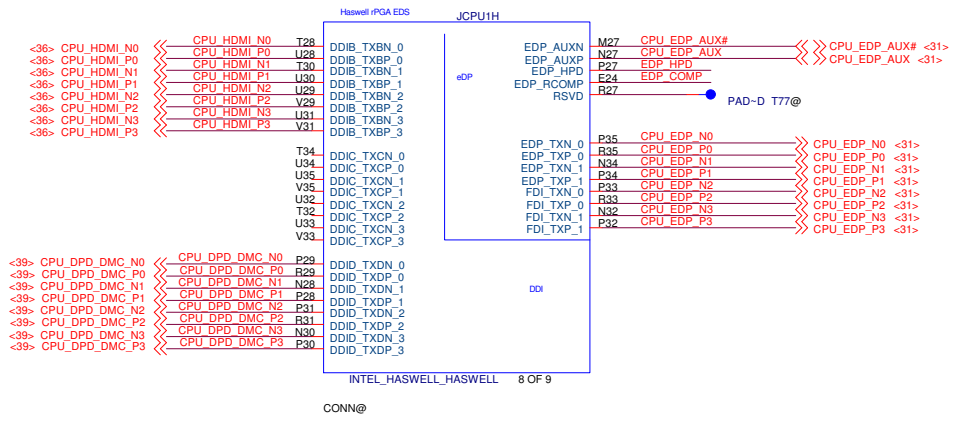
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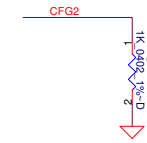
HDMI

DMC

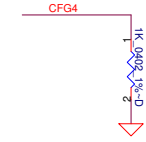


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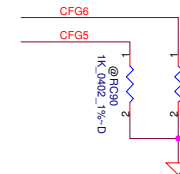
CFG STRAPS for CPU



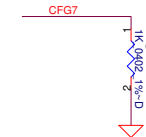
PEG Static Lane Reversal - CFG2 is for the 16x	
CFG2	1:(Default) Normal Operation; Lane # definition matches socket pin map definition 0:Lane Reversed



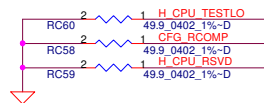
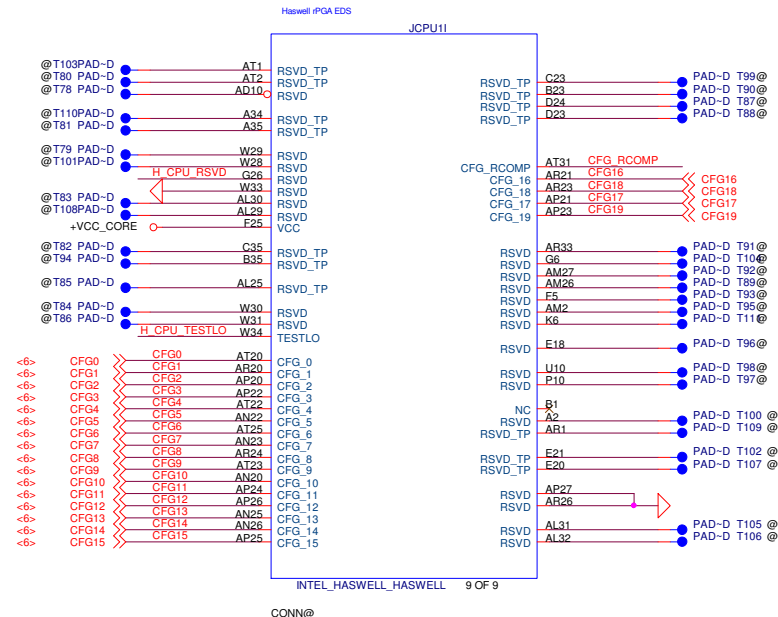
Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

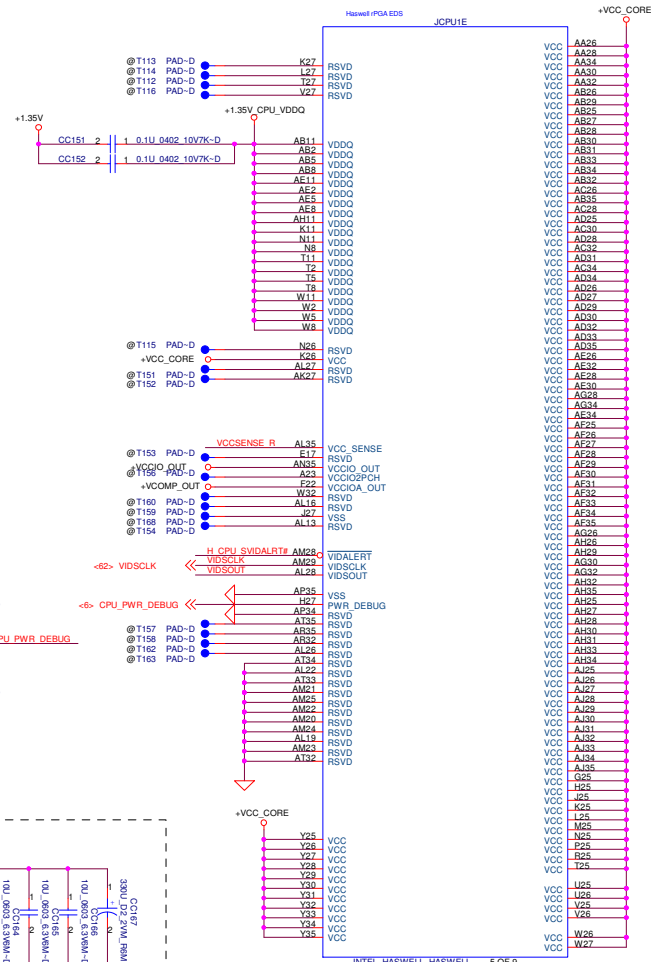
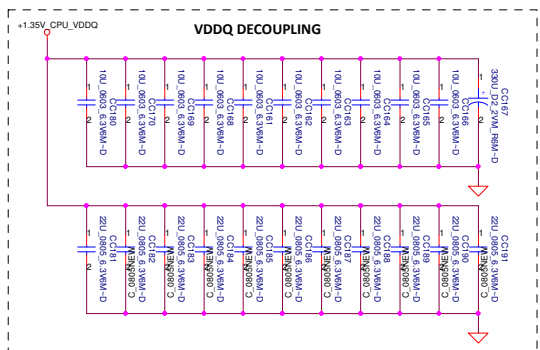
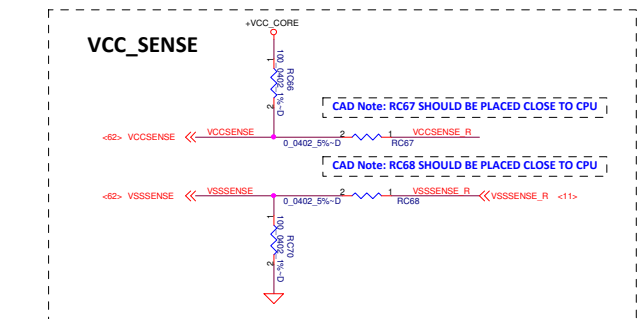
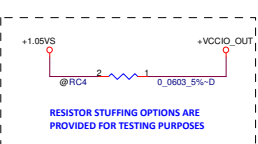
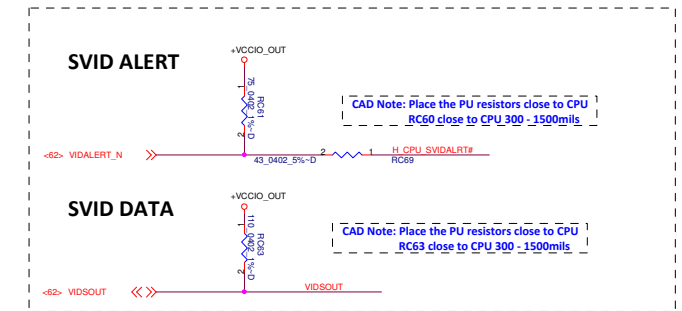
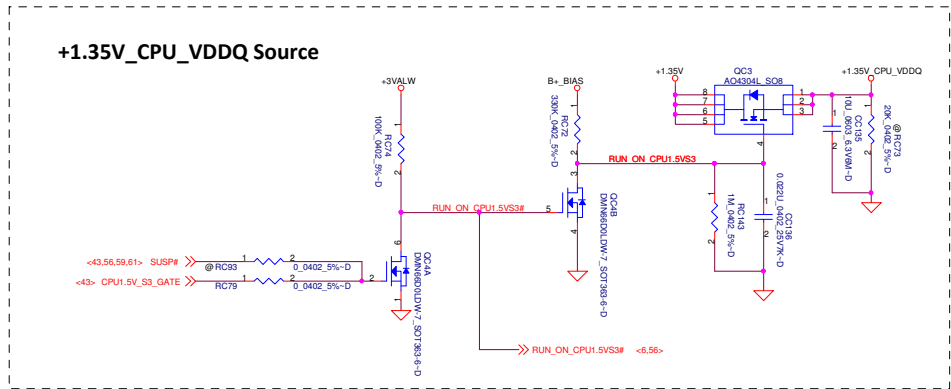


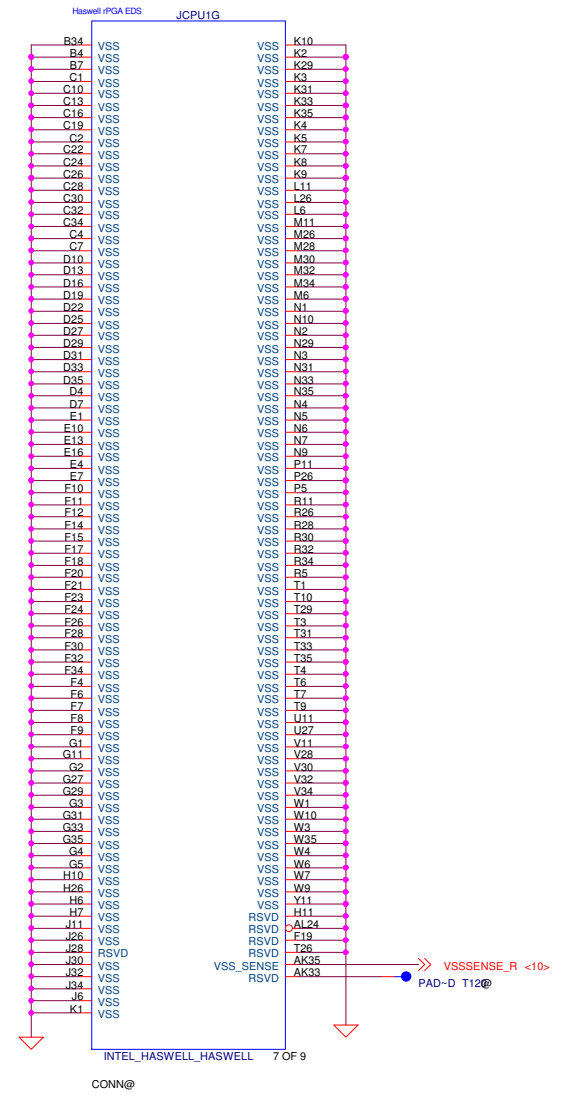
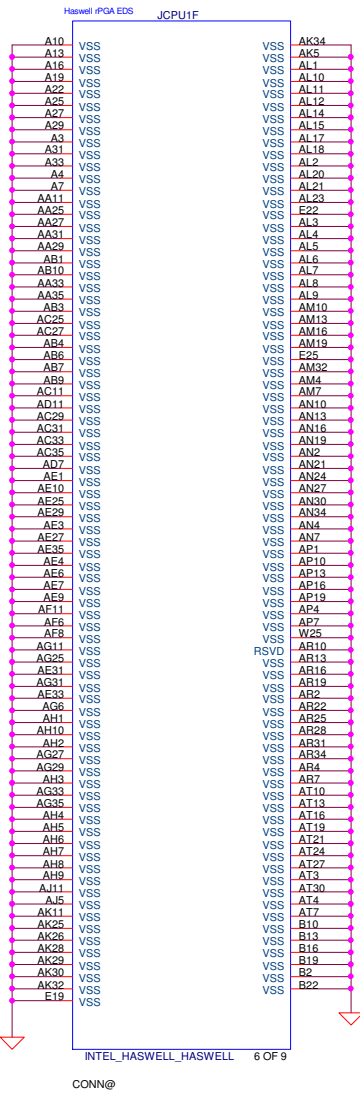
PCIe Port Bifurcation Straps	
CFG[6:5]	11: (Default) x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled



PEG DEFER TRAINING	
CFG7	1: (Default) PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training







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				Rev 0.1
				Sheet 12 of 61

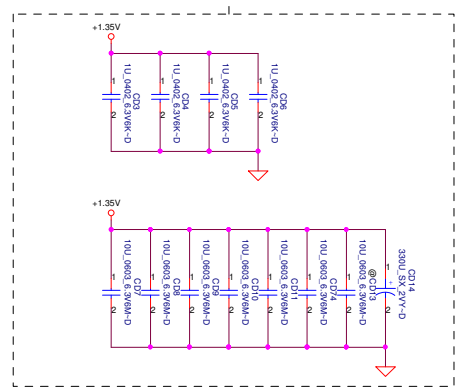
JDIMMA H=4mm



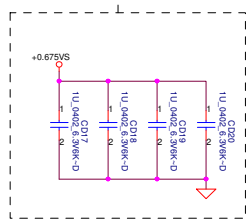
All VREF traces should have 20 mil trace width

- <7.14> DDR_A_DQS[0..7]
- <7.14> DDR_A_D[0..63]
- <7.14> DDR_A_DQS[0..7]
- <7.14> DDR_A_MA[0..15]

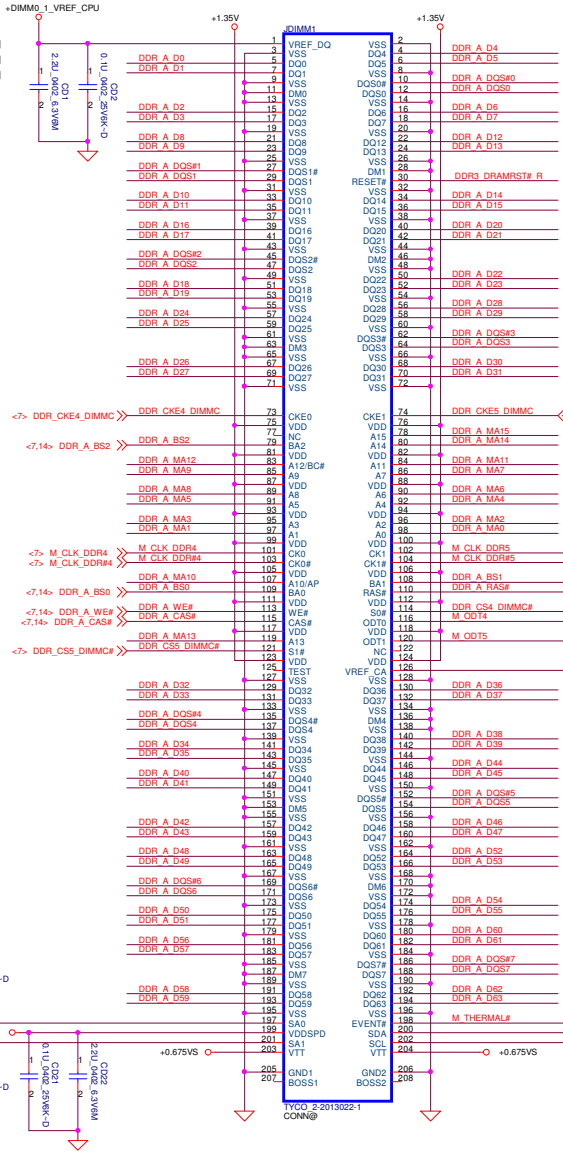
Layout Note:
Place near JDIMMA



Layout Note:
Place near JDIMMA.203,204

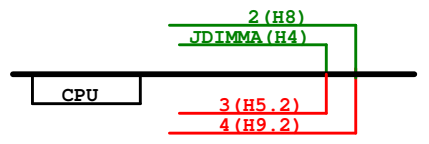


SA0	SA1	
1	0	DIMMIA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

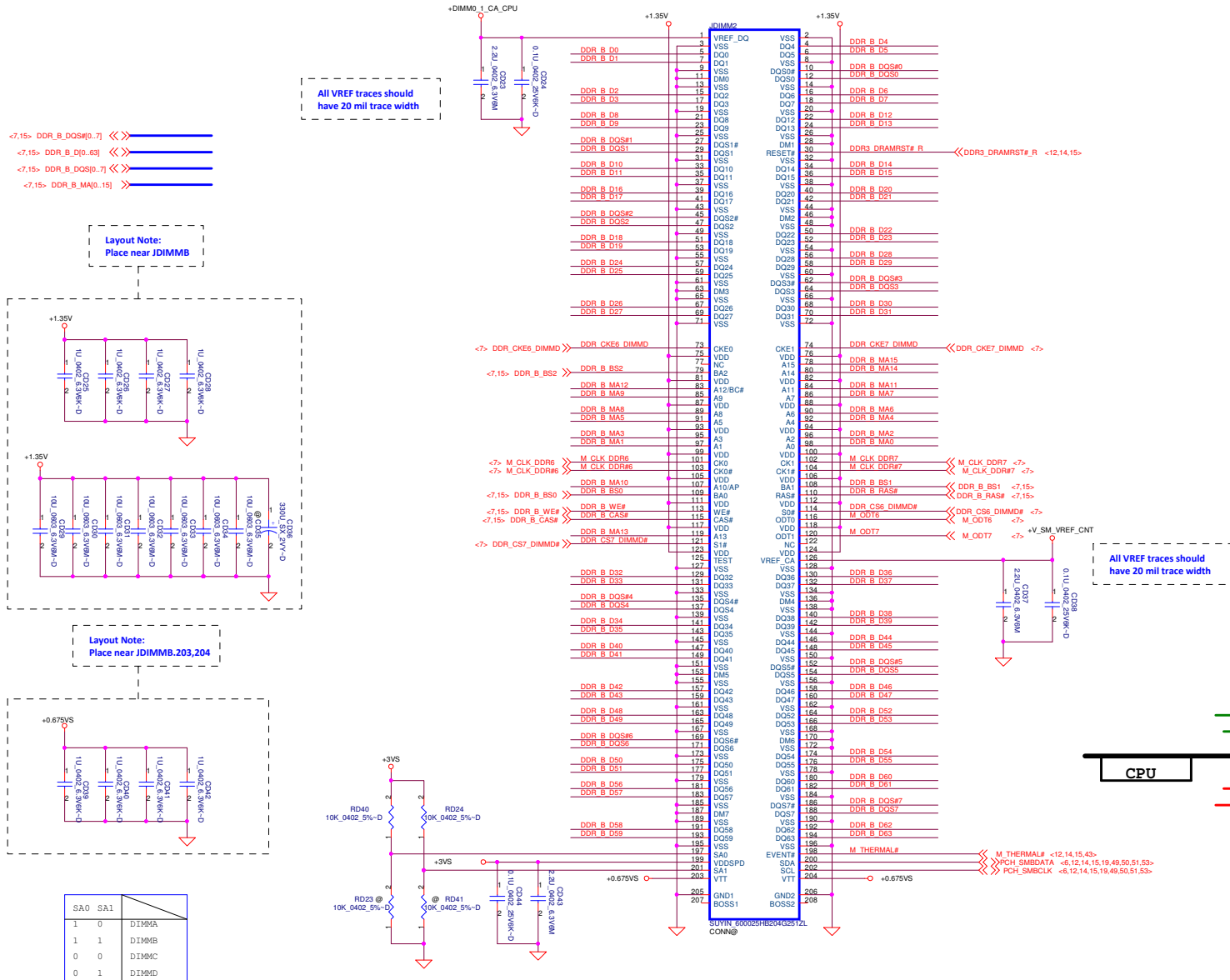


<13.14.15> DDR3_DRAMRST#_R << DDR3_DRAMRST#_R RD29 1K_0402.5%-D >>> DDR3_DRAMRST#_CPU <>

All VREF traces should have 20 mil trace width



JDIMMB H=4mm

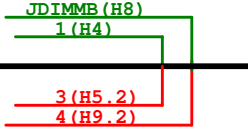


All VREF traces should have 20 mil trace width

Layout Note: Place near JDIMMB

All VREF traces should have 20 mil trace width

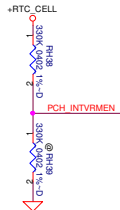
Layout Note: Place near JDIMMB.203,204



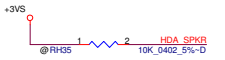
SA0	SA1	
1	0	DIMMA
1	1	DIMMB
0	0	DIMMC
0	1	DIMMD

JDIMMC H=5.2mm



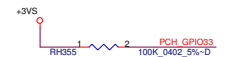


INTVRMEN - INTEGRATED SUS 1.05V VRM
ENABLE
 High - Enable Internal VRs
 Low - Enable External VRs



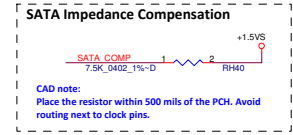
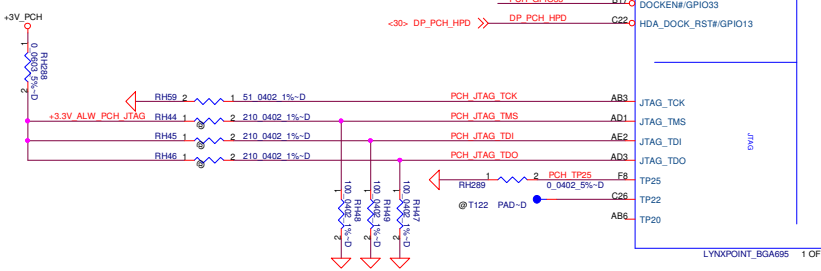
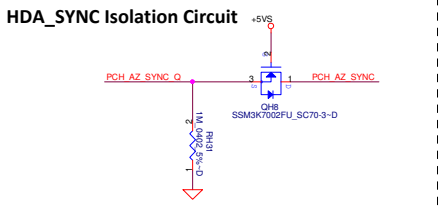
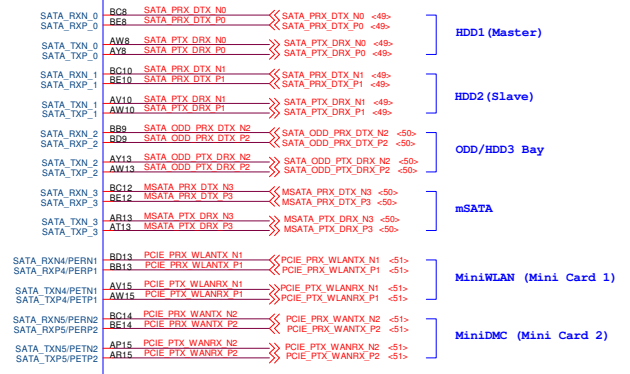
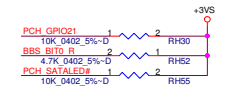
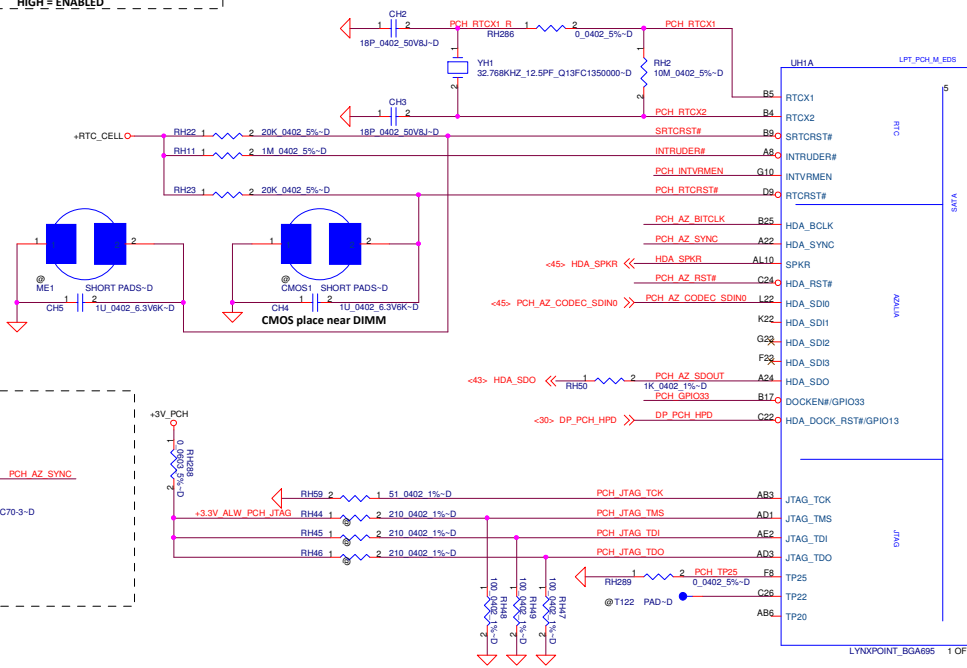
NO REBOOT STRAP
 DISABLED WHEN LOW (DEFAULT)
 ENABLED WHEN HIGH

FLASH DESCRIPTOR SECURITY OVERRIDE
 LOW = DESABLED (DEFAULT)
 HIGH = ENABLED

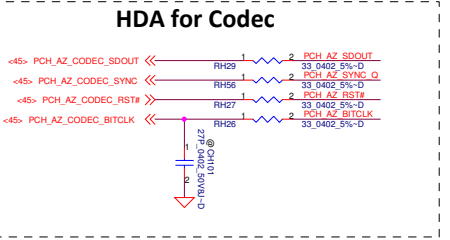
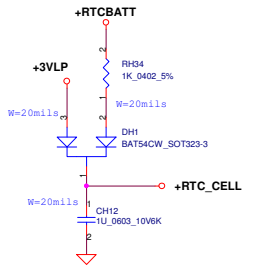


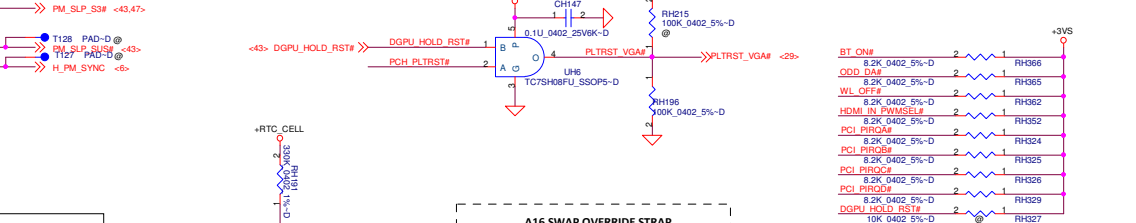
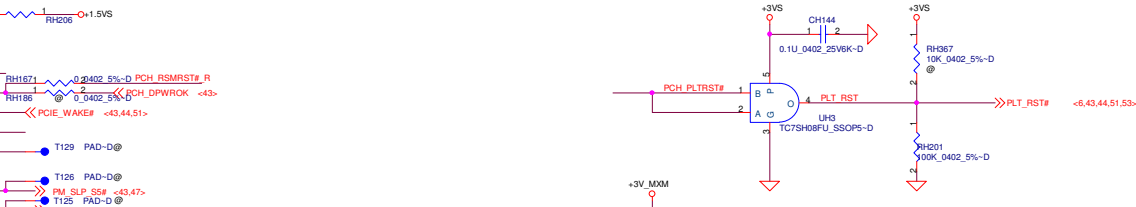
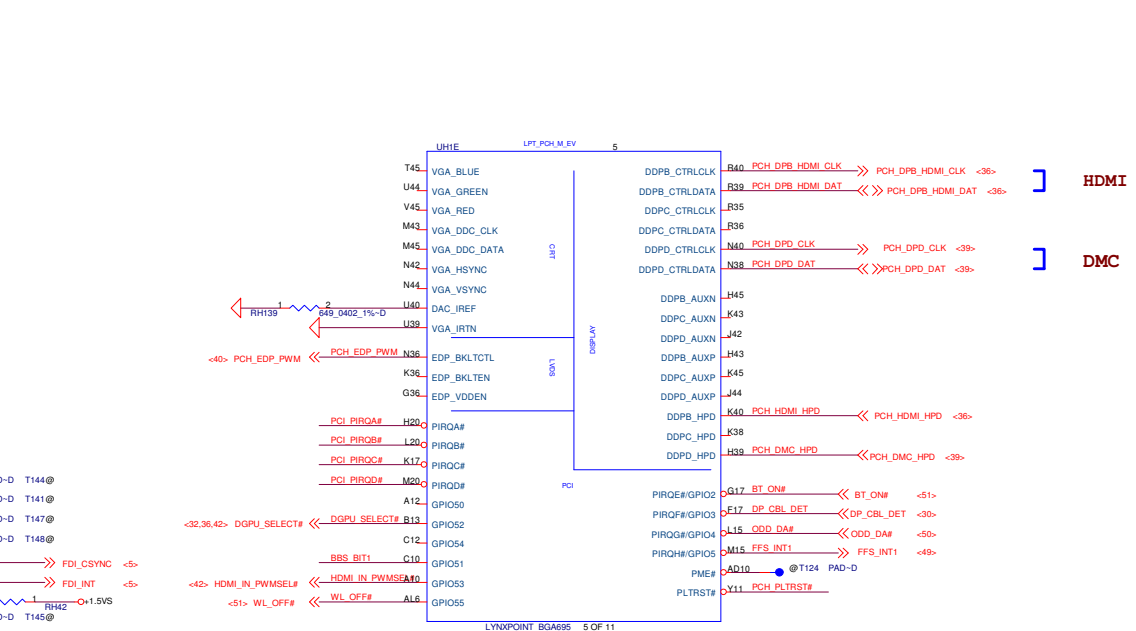
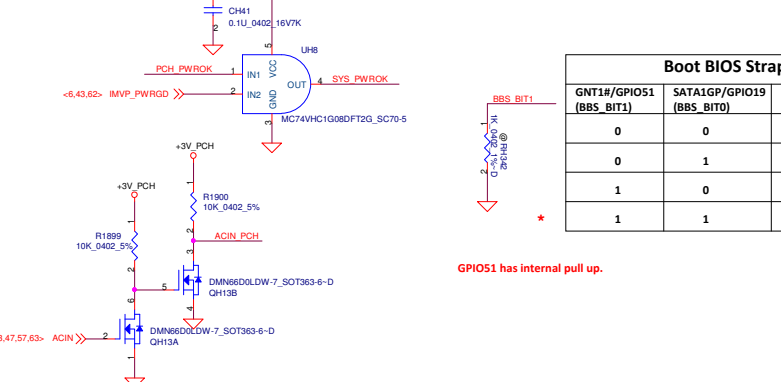
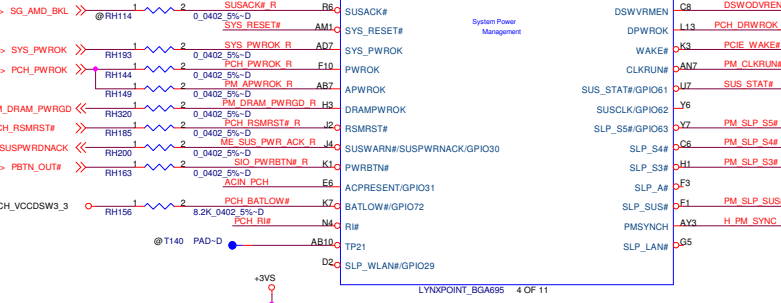
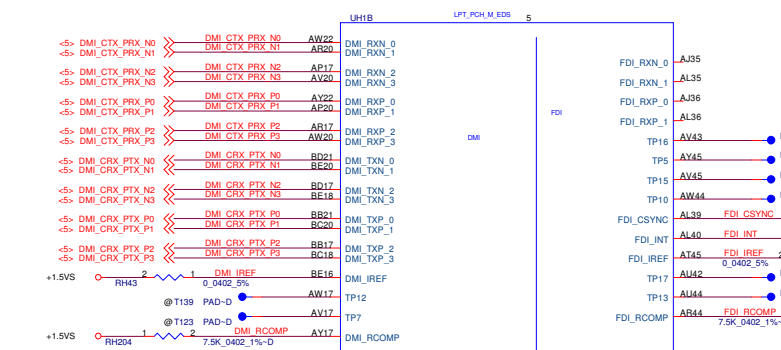
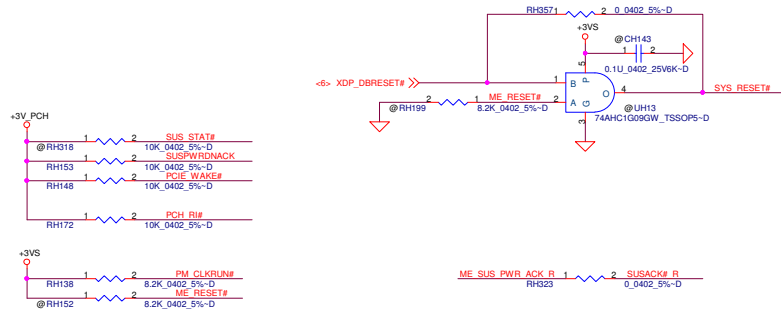
CMOS_CLR1	CMOS setting
Shunt	Clear CMOS
Open	Keep CMOS

ME_CLR1	TPM setting
Shunt	Clear ME RTC Registers
Open	Keep ME RTC Registers



RTC Battery





Boot BIOS Strap		
GNT1#/GPIO1 (BBS_BIT1)	SATA1GP/GPIO19 (BBS_BIT0)	Boot BIOS Location
0	0	LPC
0	1	Reserved (NAND)
1	0	PCI
1	1	SPI

DSWDVREN - ON DIE DSW VR ENABLE
 HIGH = ENABLED (DEFAULT)
 LOW = DISABLED

A16 SWAP OVERRIDE STRAP
 STP_A16OVR LOW = A16 SWAP OVERRIDE
 HIGH = DEFAULT

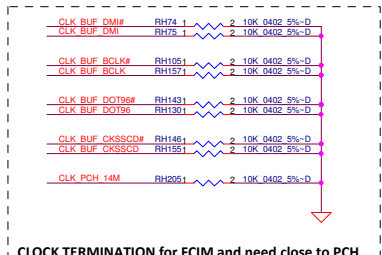
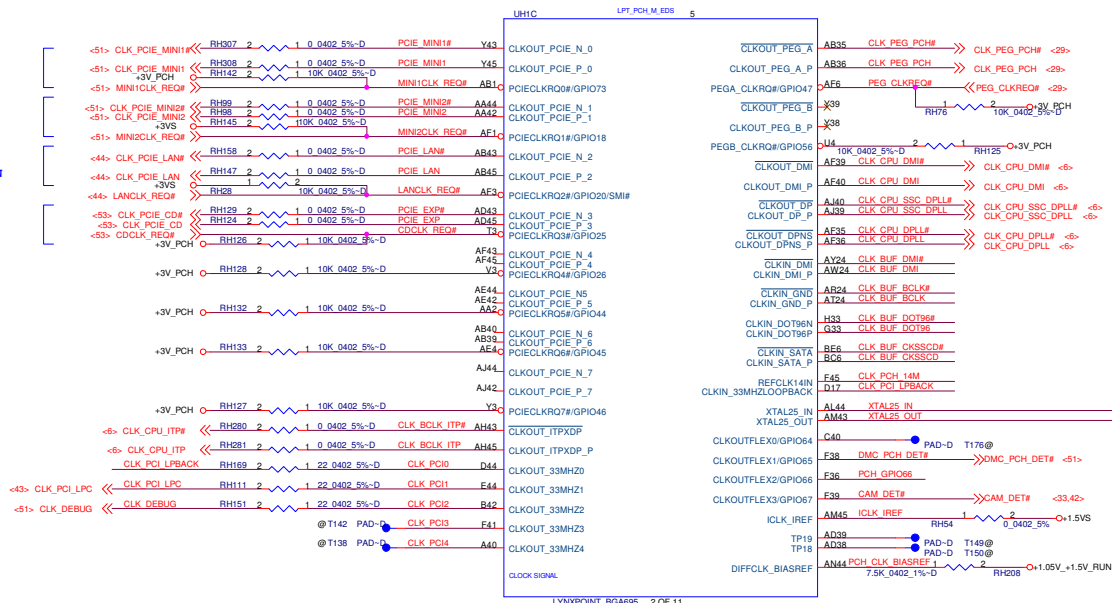
GPIO15 has internal pull up.

MiniWLAN (Mini Card 1)

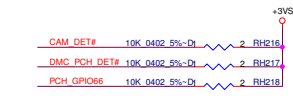
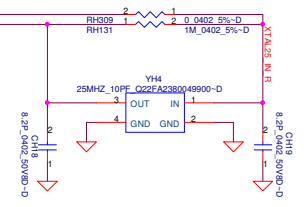
DMC (Mini Card 2)

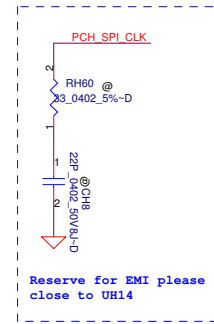
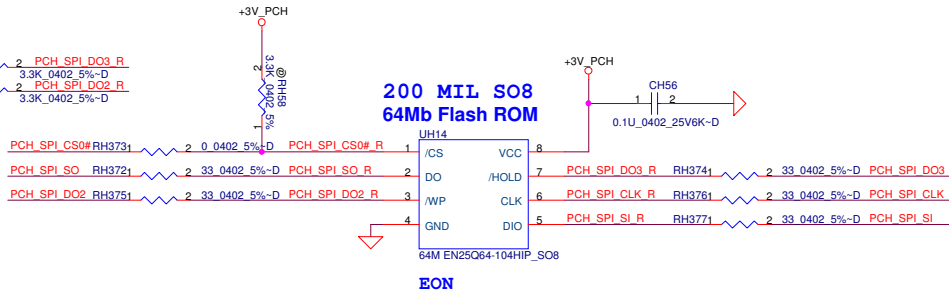
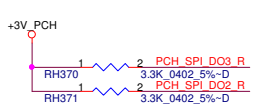
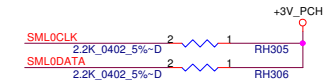
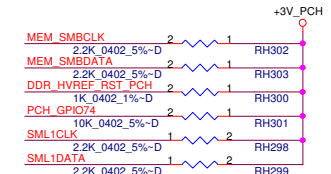
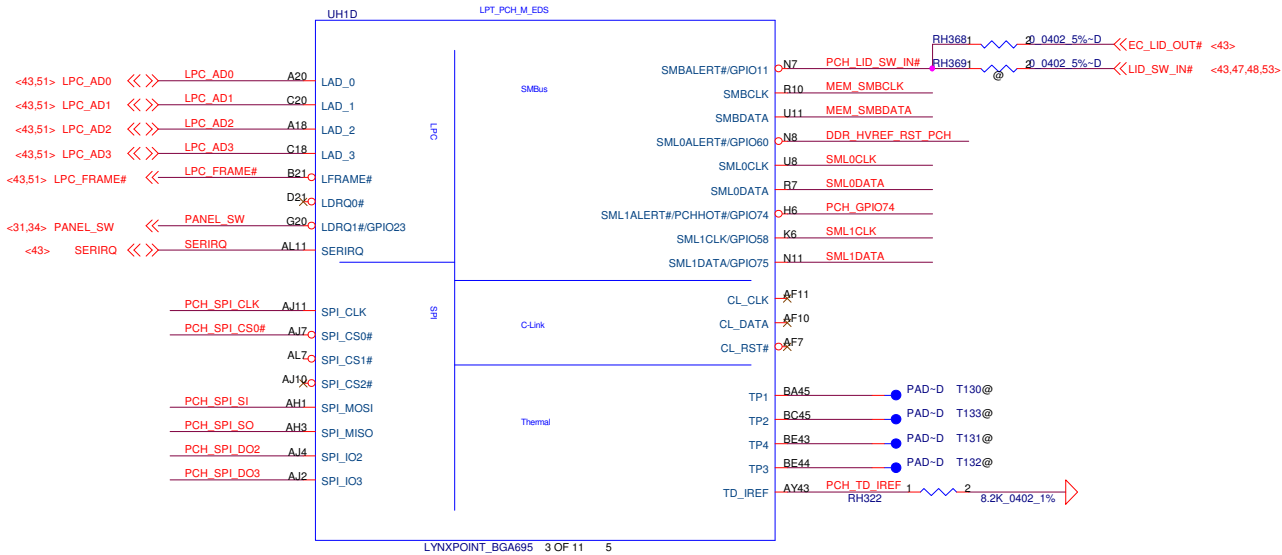
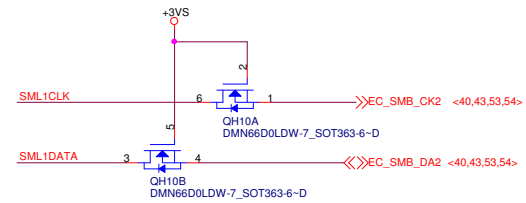
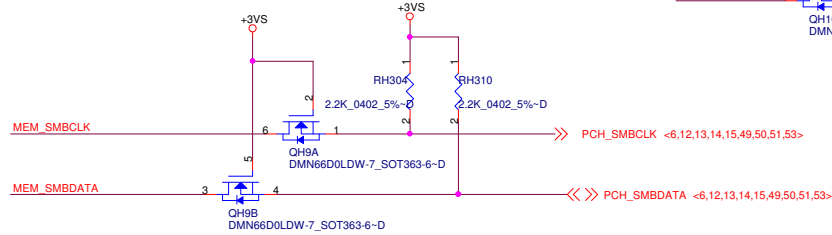
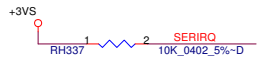
10/100/1G LAN

Card Reader

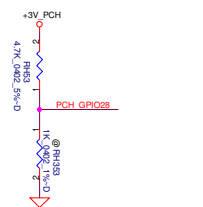
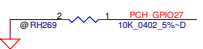
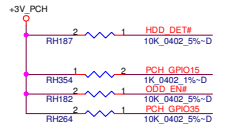
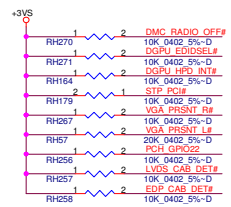


CLOCK TERMINATION for FCIM and need close to PCH

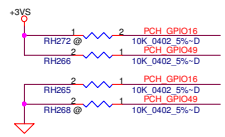




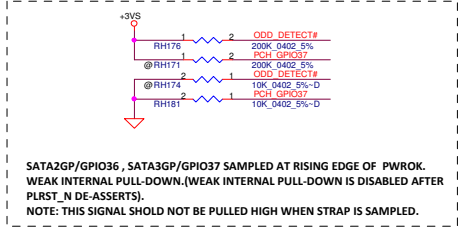
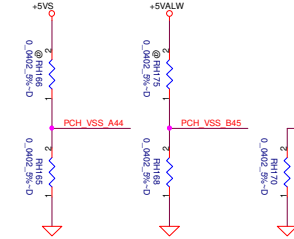
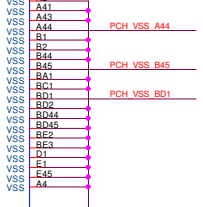
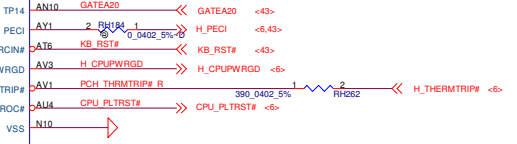
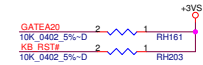
Security Classification	Compal Secret Data			Title PCH (4/9) SPI, SMBUS, LPC
Issued Date	2012/06/22	Deciphered Date	2013/06/21	
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Date:	Friday, June 22, 2012	Sheet	20 of 61	



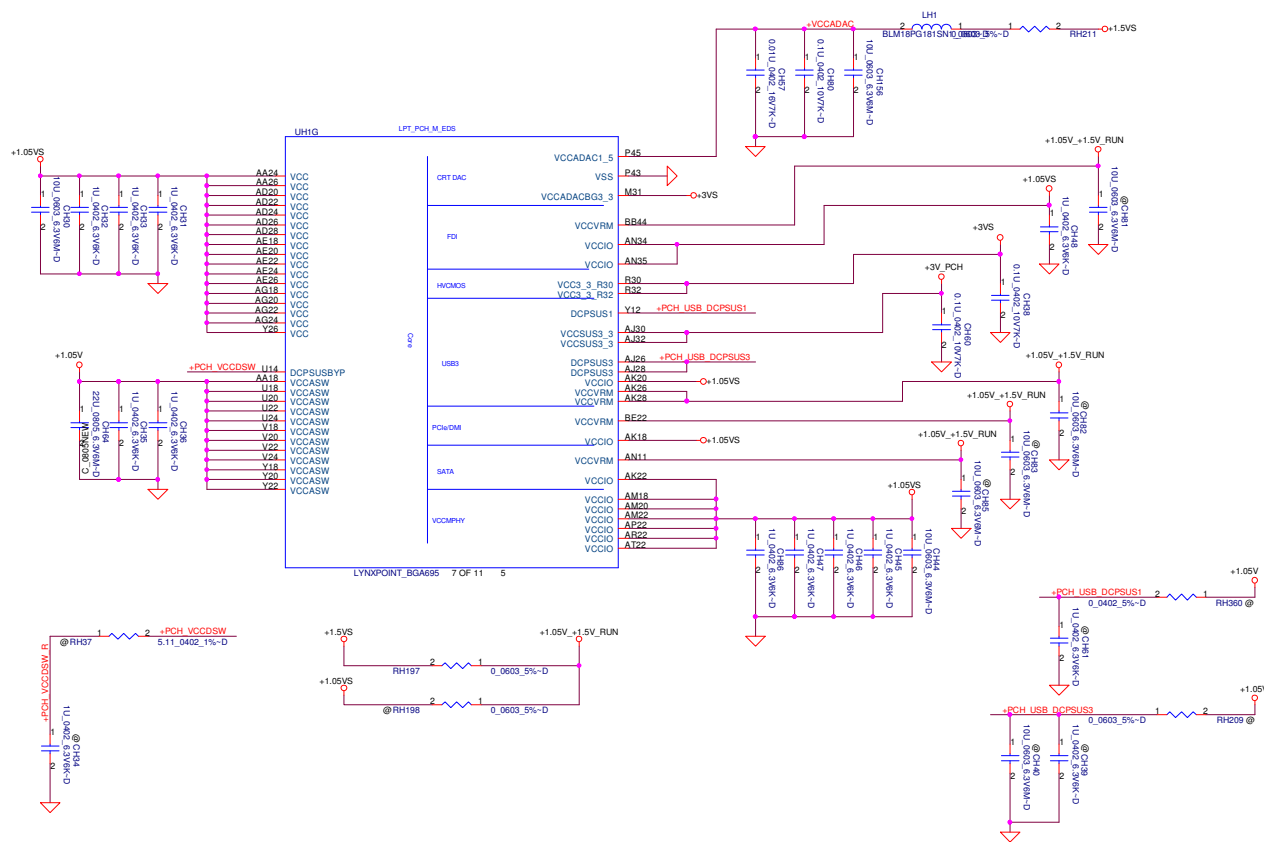
PLL ON DIE VR ENABLE
 ENABLED - HIGH(DEFAULT)
 DISABLED - LOW



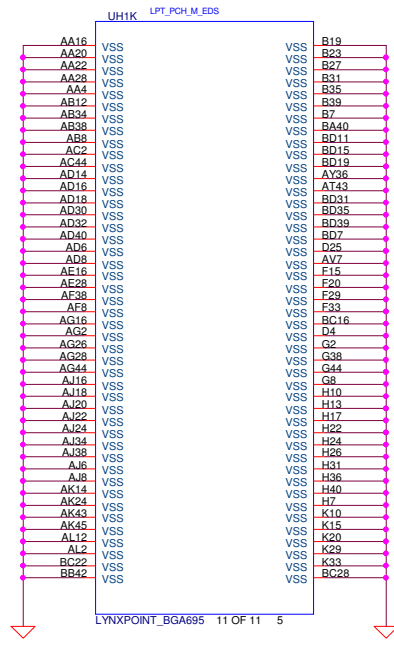
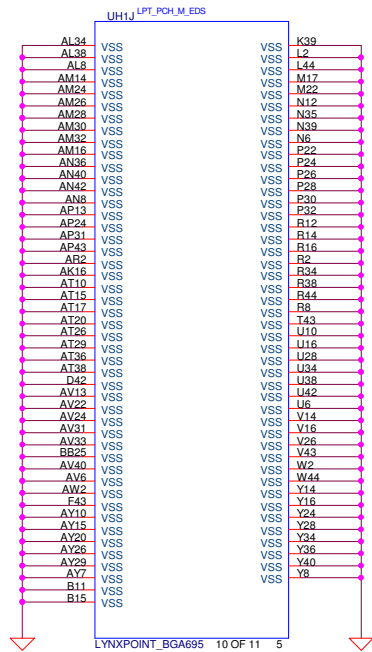
Config	GPIO16,49
USB X4,PCIEX8,SATAX6	11
* USB X6,PCIEX8,SATAX4	01



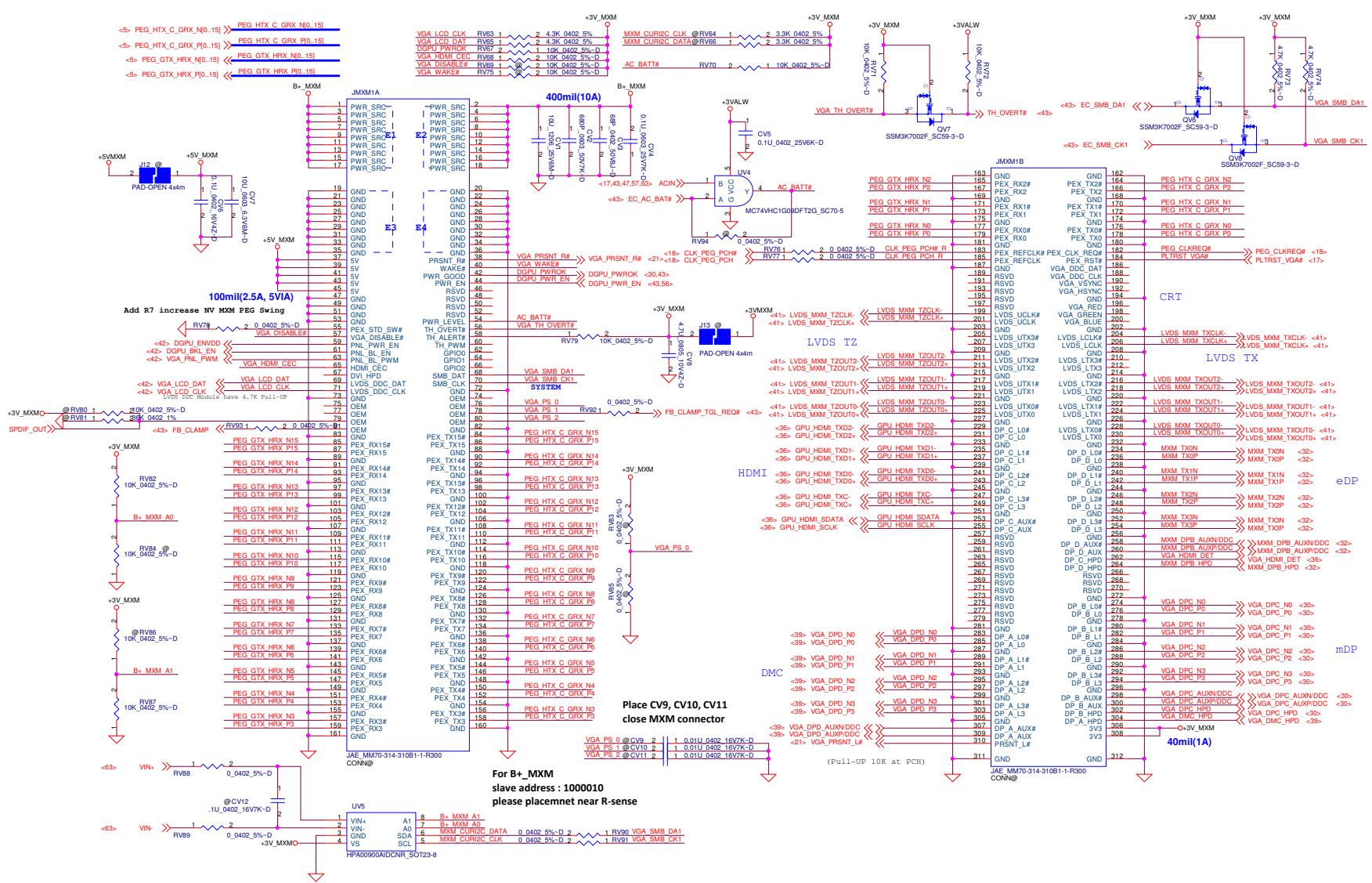
Fixed Signals				Muxed Signals		Fixed Signals								Muxed Signals		Fixed Signals				
USB3_1	USB3_2	USB3_5	USB3_6	PCIE_1	PCIE_2	PCIE_3	PCIE_4	PCIE_5	PCIE_6	PCIE_7	PCIE_8	SATA_4	SATA_5	SATA_0	SATA_1	SATA_2	SATA_3			
				(00)	(00)							(10)	(10)							
				USB3_3	USB3_4							PCIE_1	PCIE_2							
				(01)	(01)							(01)	(01)							



PCH Power Rail Table		
Voltage Rail	Voltage	50 Iccmax Current (A)
VCC	1.05V	1.29 A
VCCIO	1.05V	3.629 A
VCCDAC1_5	1.5V	0.070 A
VCCDAC3_3	3.3V	0.0133 A
VCCCLK	1.05V	0.306 A
VCCCLK3_3	3.3V	0.055 A
VCCVRM	1.5V	0.179 A
VCC3_3	3.3V	0.133 A
VCCASW	1.05V	0.67 A
VCCSUSHDA	3.3V	0.01 A
VCCSPI	3.3V	0.022 A
VCCSUS3_3	3.3V	0.261 A
VCCSW3_3	3.3V	0.015 A
V_PROC_IO	1.05V	0.004 A



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				LA-9331P	0.1
				Date: Friday, June 22, 2012	Sheet 25 of 61



For B+ M_XM
slave address : 1000010
please placemnet near R-sense

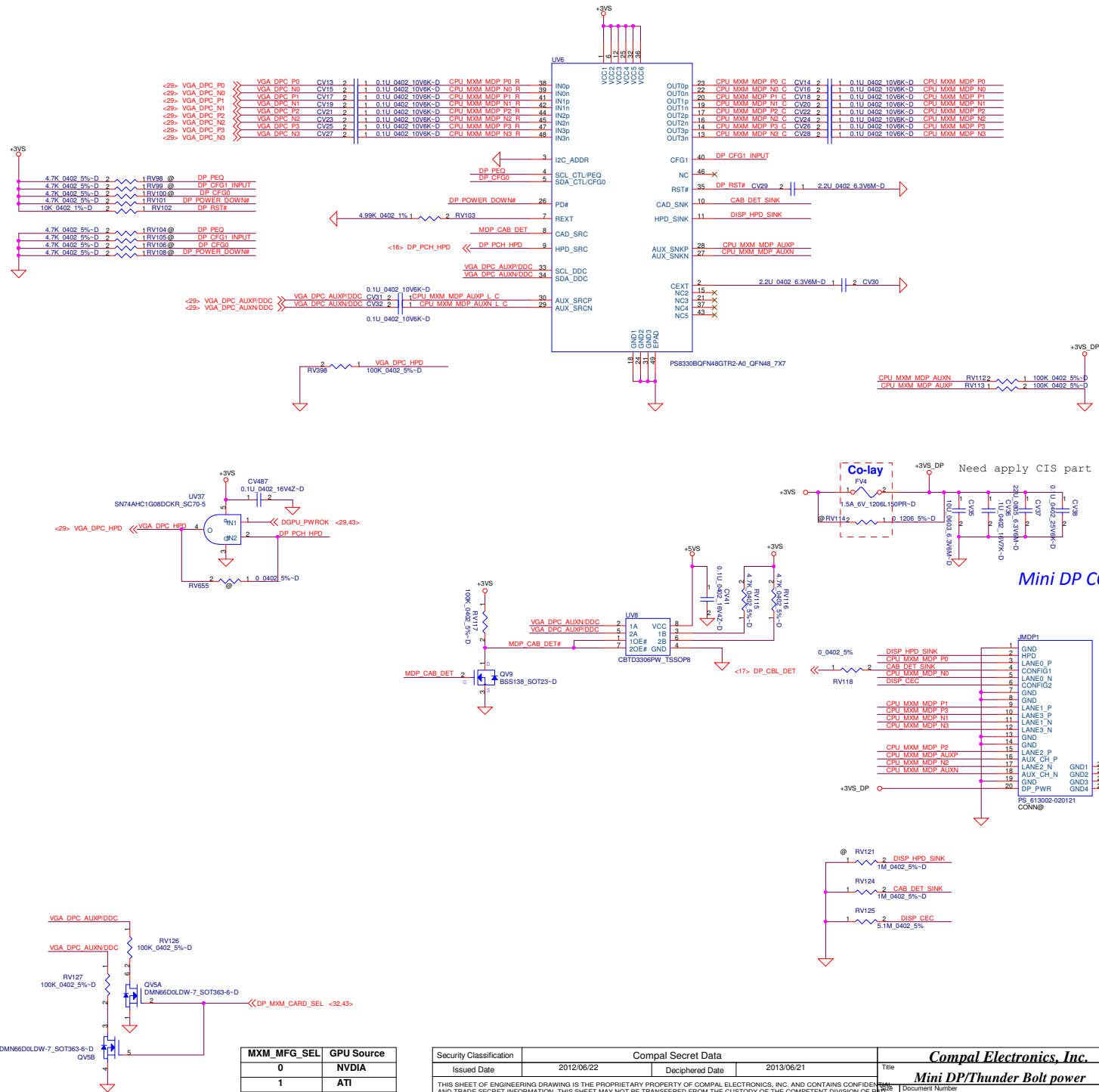
Place CV9, CV10, CV11
close MXM connector

(Pull-UP 10K at PCB)

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		2013/06/21
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Compal Electronics, Inc.	
Title	MXMIII Connector
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DP Redriver



MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

Security Classification	Compal Secret Data
Issued Date	2012/06/22
Deciphered Date	2013/06/21

Compal Electronics, Inc.	
Title: Mini DP/Thunder Bolt power	
Document Number:	LA-931P
Date:	Friday, June 22, 2012
Sheet:	27 of 61

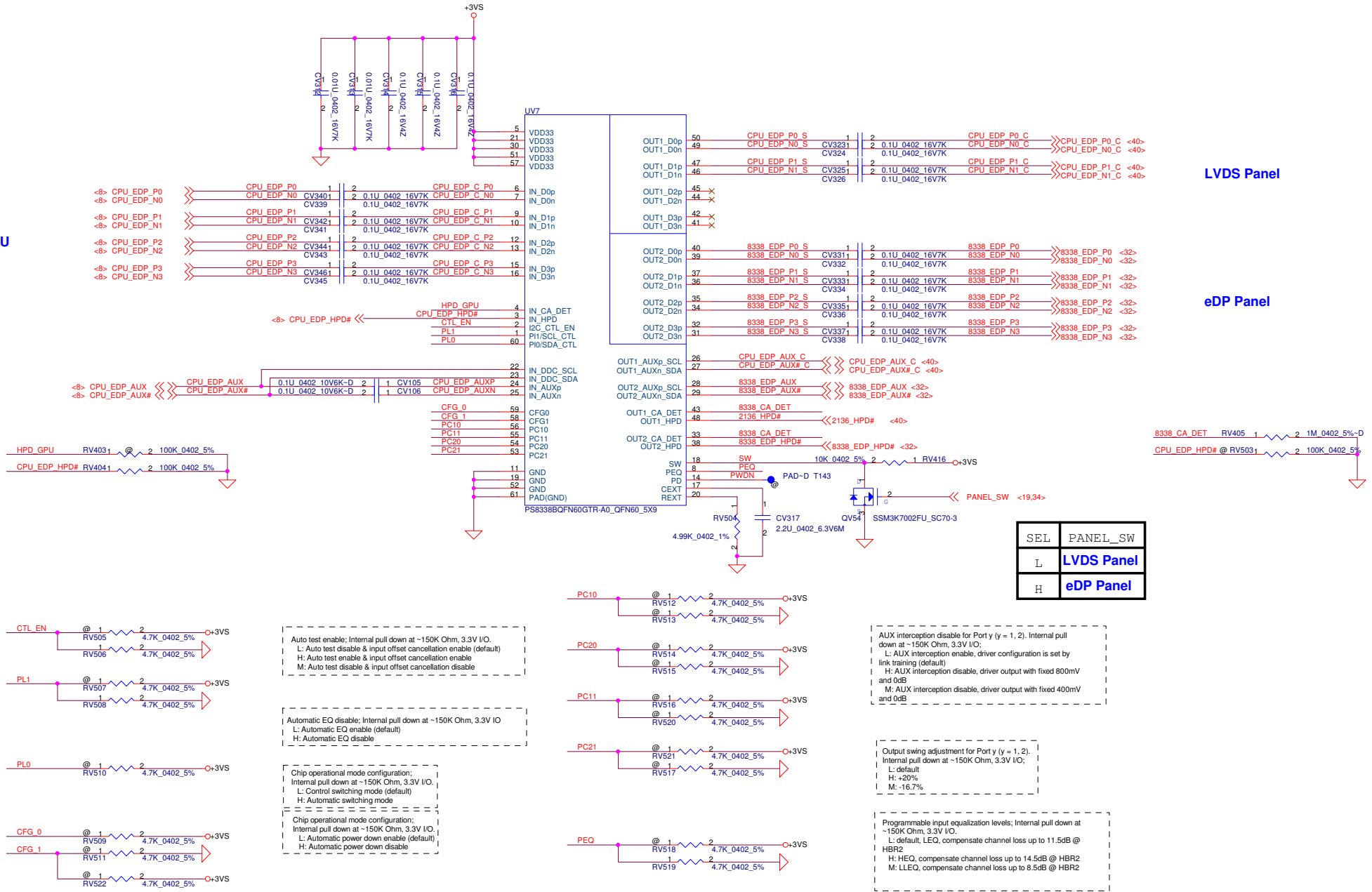
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CPU to EDP & LVDS MUX

CPU

LVDS Panel

eDP Panel



Auto test enable; Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Auto test disable & input offset cancellation enable (default)
 H: Auto test enable & input offset cancellation enable
 M: Auto test disable & input offset cancellation disable

Automatic EQ disable; Internal pull down at ~150K Ohm, 3.3V IO
 L: Automatic EQ enable (default)
 H: Automatic EQ disable

Chip operational mode configuration;
 Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Control switching mode (default)
 H: Automatic switching mode

Chip operational mode configuration;
 Internal pull down at ~150K Ohm, 3.3V I/O.
 L: Automatic power down enable (default)
 H: Automatic power down disable

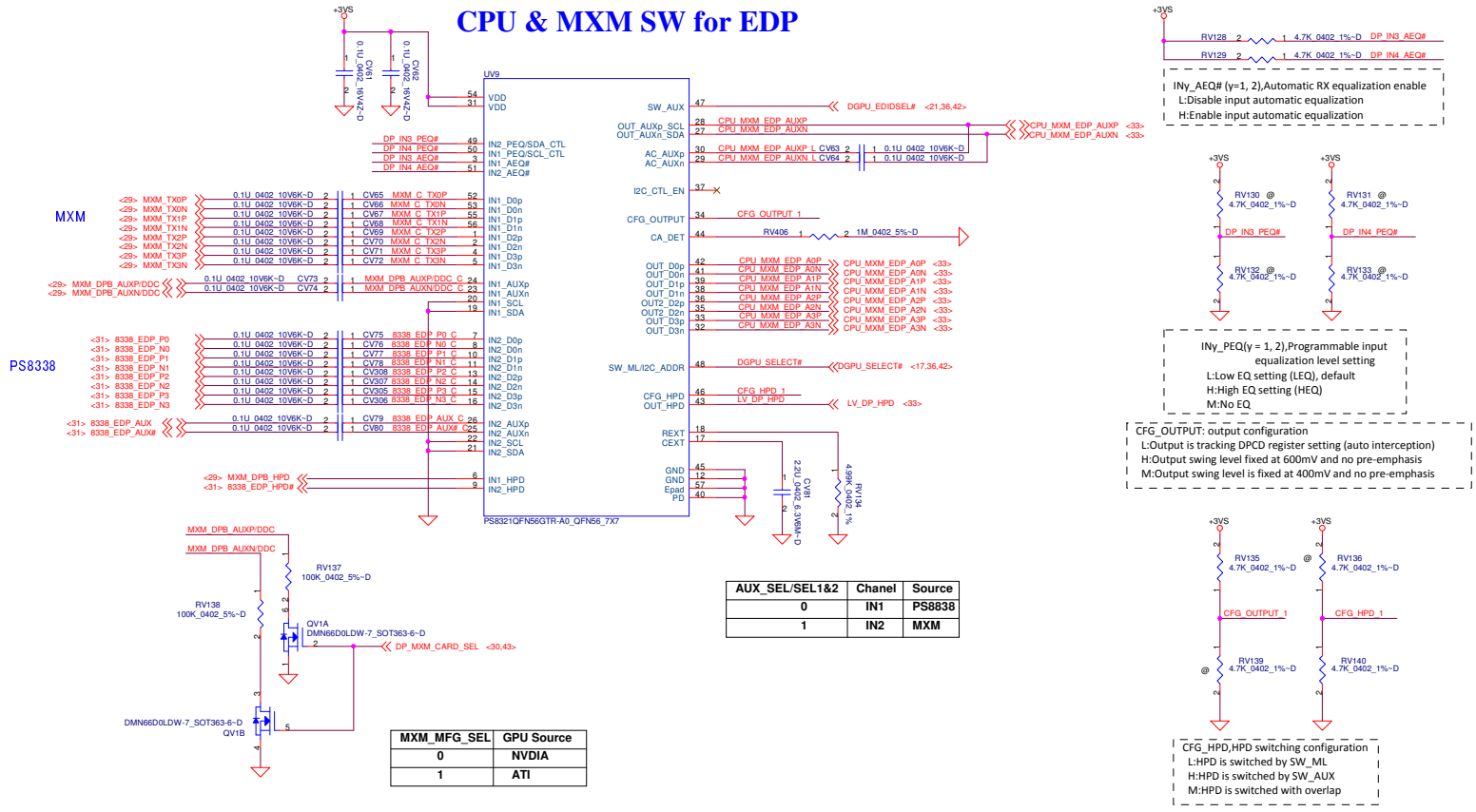
AUX interception disable for Port y (y = 1, 2). Internal pull down at ~150K Ohm, 3.3V I/O;
 L: AUX interception enable, driver configuration is set by link training (default)
 H: AUX interception disable, driver output with fixed 800mV and 0dB
 M: AUX interception disable, driver output with fixed 400mV and 0dB

Output swing adjustment for Port y (y = 1, 2).
 Internal pull down at ~150K Ohm, 3.3V I/O;
 L: default
 H: +20%
 M: -16.7%

Programmable input equalization levels; Internal pull down at ~150K Ohm, 3.3V I/O.
 L: default, LEQ, compensate channel loss up to 11.5dB @ HBR2
 H: HEQ, compensate channel loss up to 14.5dB @ HBR2
 M: LLEQ, compensate channel loss up to 8.5dB @ HBR2

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CPU & MXM SW for EDP



MXM

PS8338

AUX_SEL/SEL1&2	Chanel	Source
0	IN1	PS8838
1	IN2	MXM

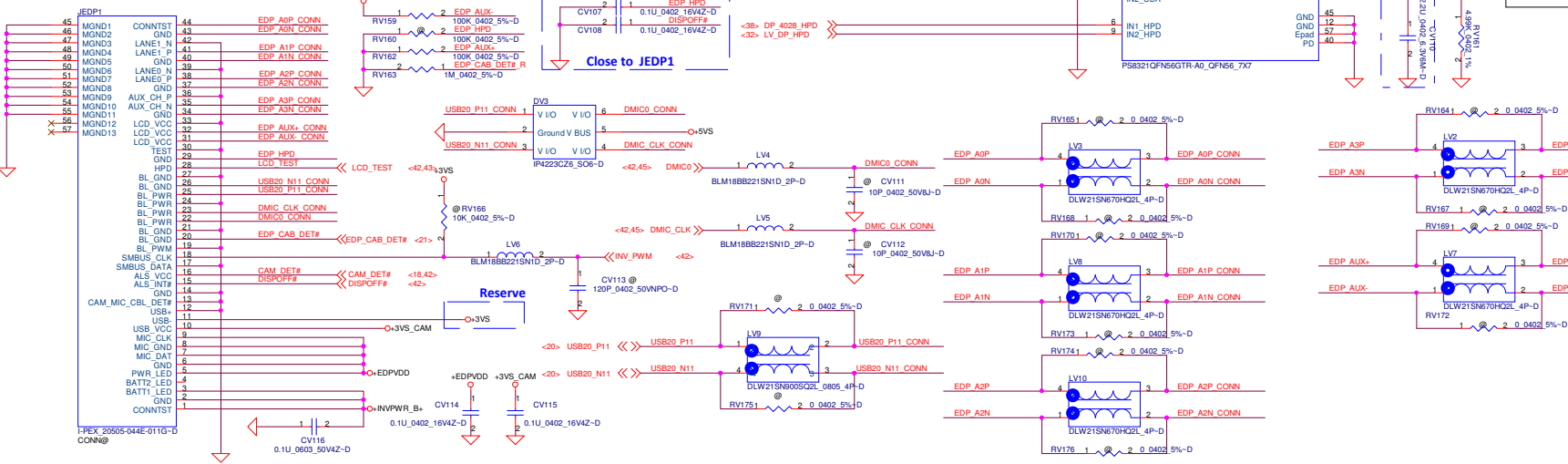
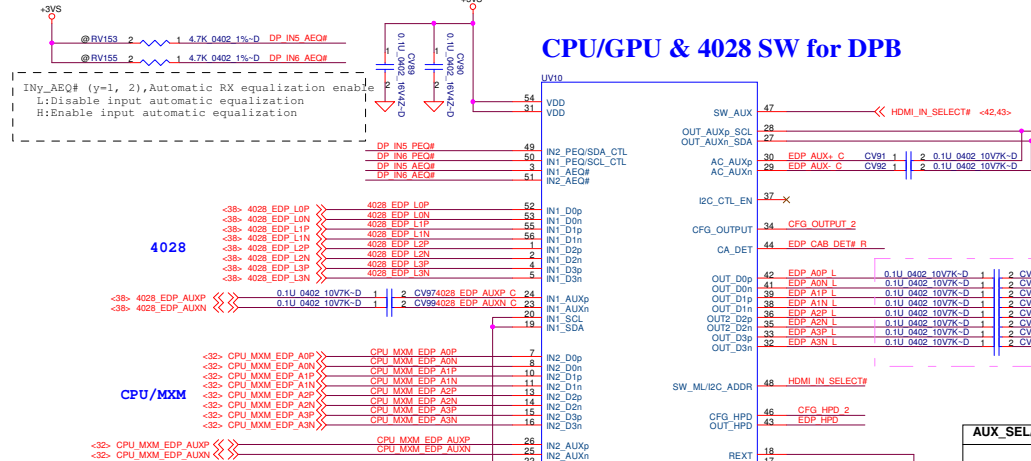
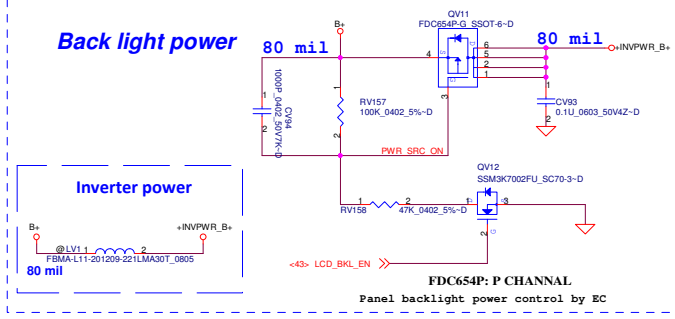
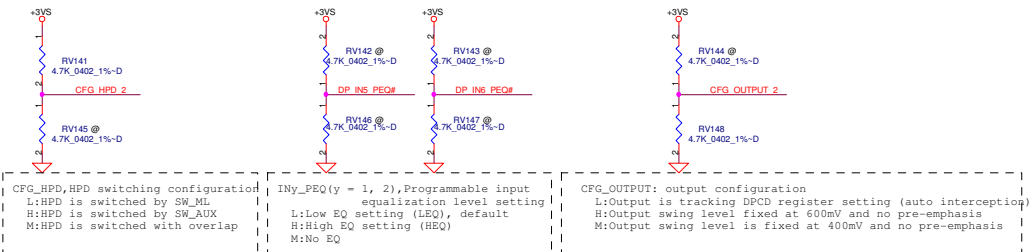
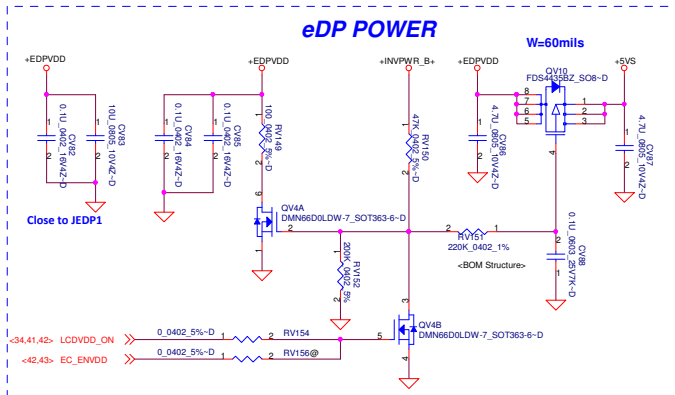
MXM_MFG_SEL	GPU Source
0	NVIDIA
1	ATI

INy_AEQ#(y=1, 2), Automatic RX equalization enable
 L: Disable input automatic equalization
 H: Enable input automatic equalization

INy_PEQ#(y = 1, 2), Programmable input equalization level setting
 L: Low EQ setting (LEQ), default
 H: High EQ setting (HEQ)
 M: No EQ

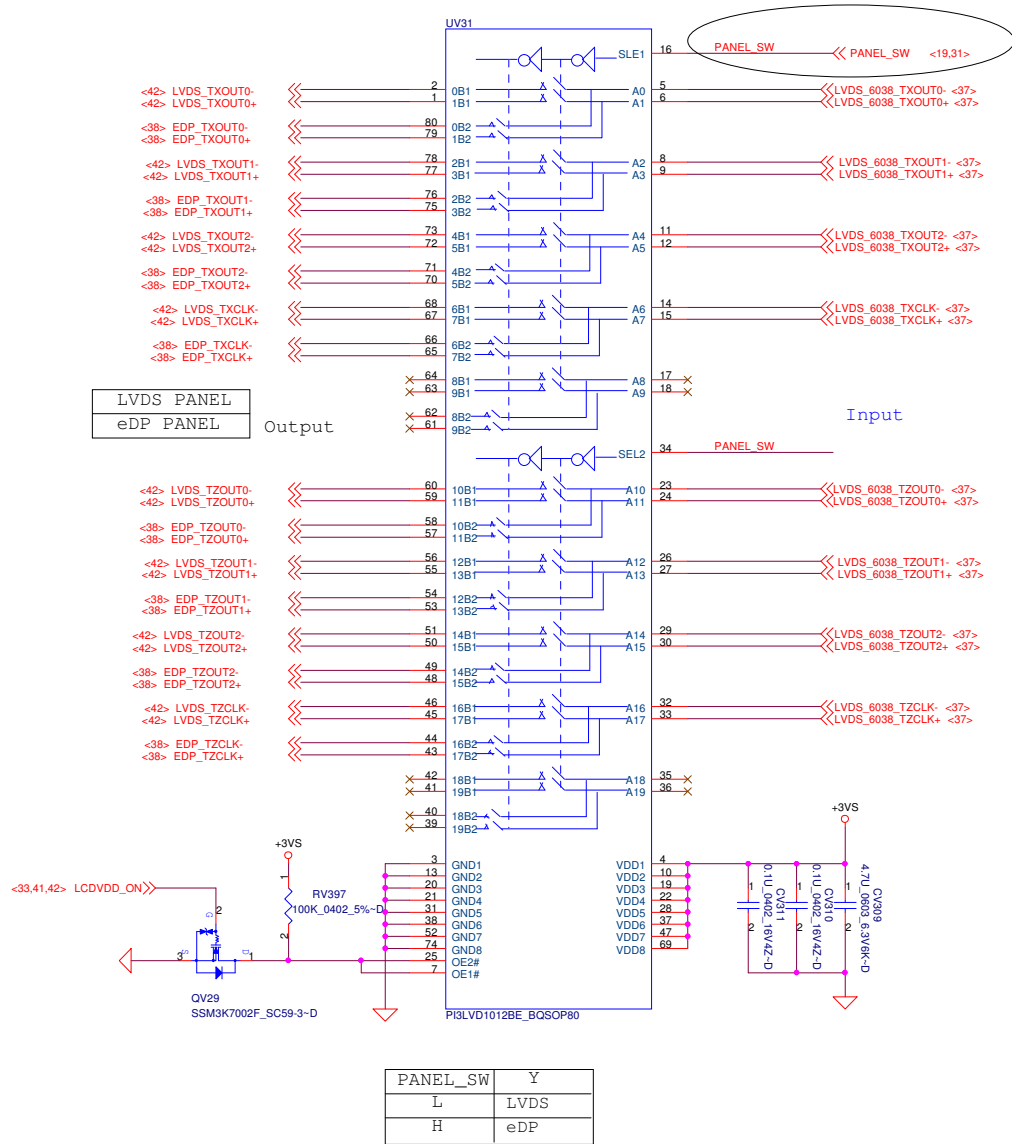
CFG_OUTPUT: output configuration
 L: Output is tracking DPCD register setting (auto interception)
 H: Output swing level fixed at 600mV and no pre-emphasis
 M: Output swing level is fixed at 400mV and no pre-emphasis

CFG_HPD, HPD switching configuration
 L: HPD is switched by SW_ML
 H: HPD is switched by SW_AUX
 M: HPD is switched with overlap



AUX_SEL/SEL1&2	Chanel	Source
0	A	4028
1	B	CPU/MXM

STDP6038 to EDP & LVDS MUX



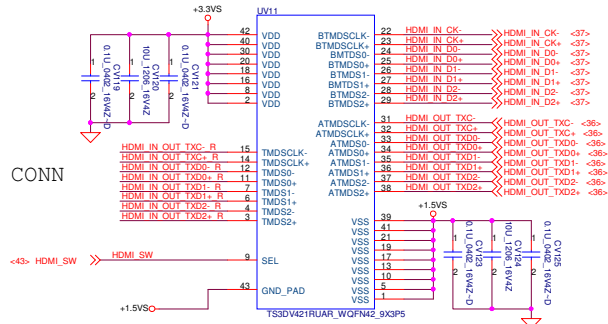
LVDS PANEL
eDP PANEL

Output

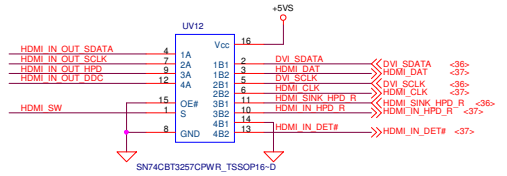
Input

PANEL_SW	Y
L	LVDS
H	eDP

HDMI CONN



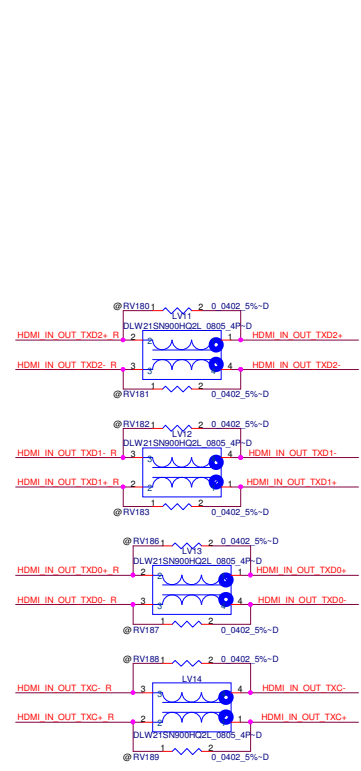
SEL	OUTPUT
L	A
H	B



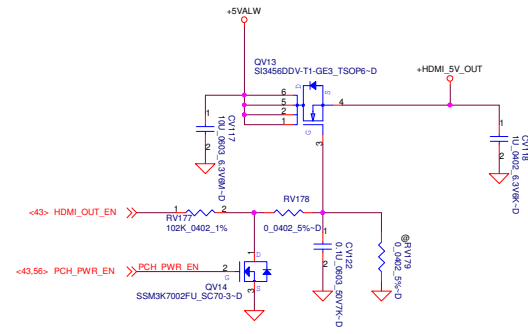
SEL	OUTPUT
L	B1
H	B2

STDP6038

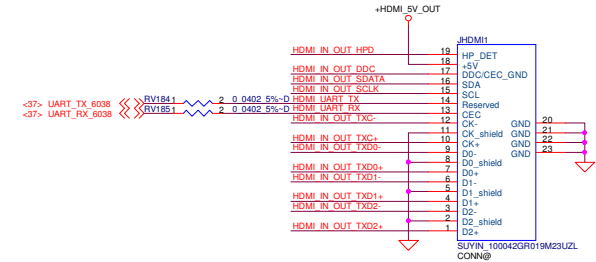
CPU/MXM



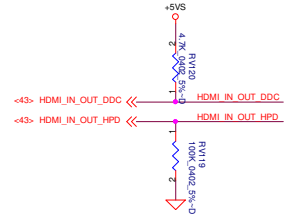
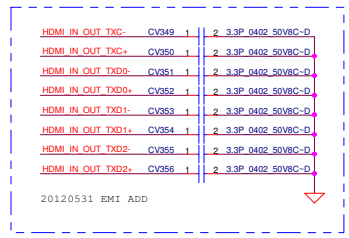
Reserve for EMI please close to JHDMI2

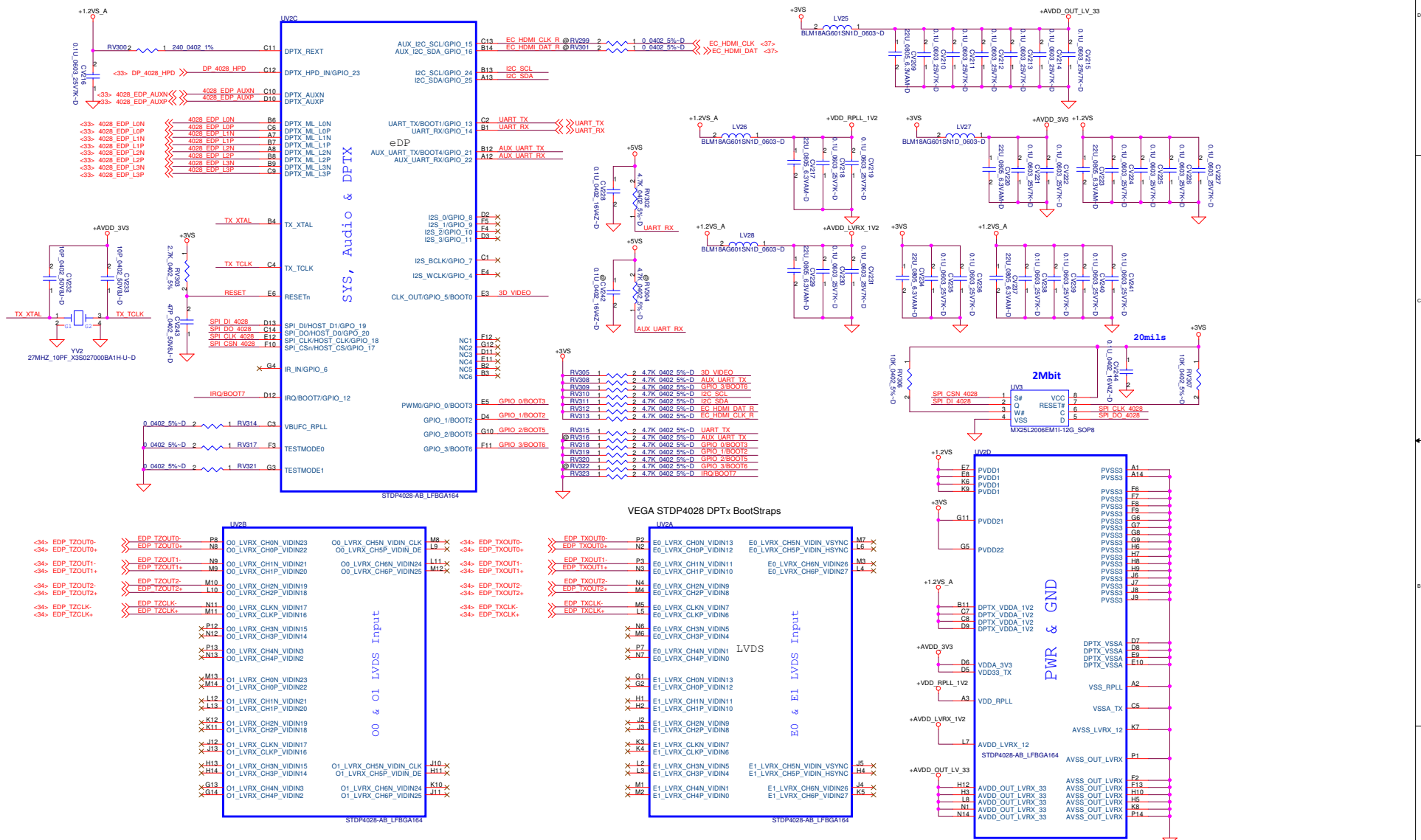


HDMI Input/Output Connector



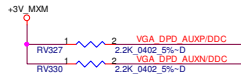
Part Number	Description
800000028R	HDMI W/Logo:800000028R



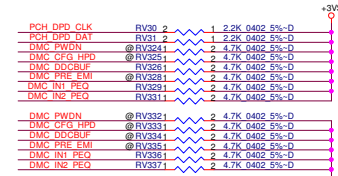
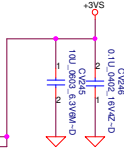


Security Classification	Compal Secret Data	
Issued Date	2012/06/22	Deciphered Date
		2013/06/21

Compal Electronics, Inc. LVDS to eDP-STDP4028		Title
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Date:	Friday, June 22, 2012	0.1
Sheet	35	of 61

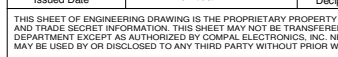
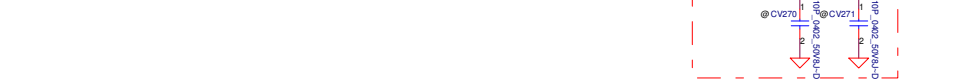
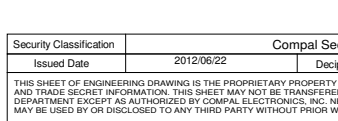
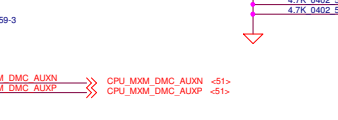
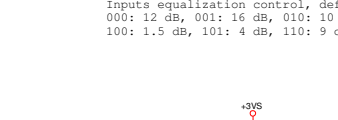
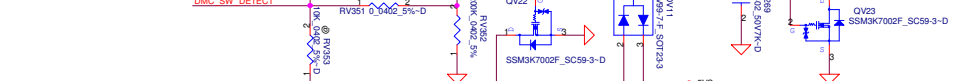
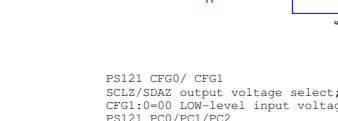
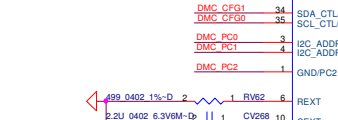
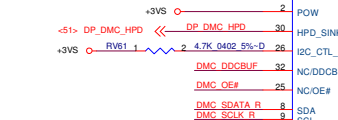
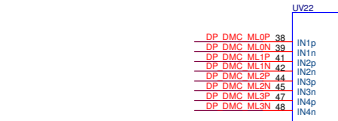
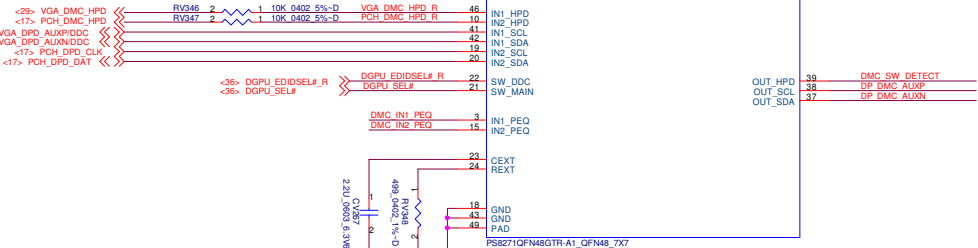
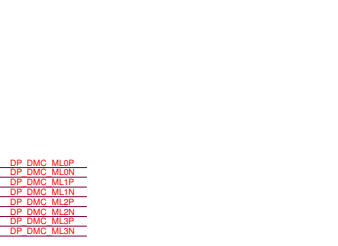
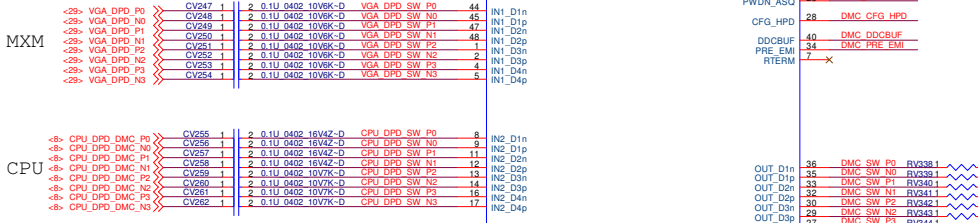


PCH/GPU AUX&LANE SW for DPB



MXM

CPU



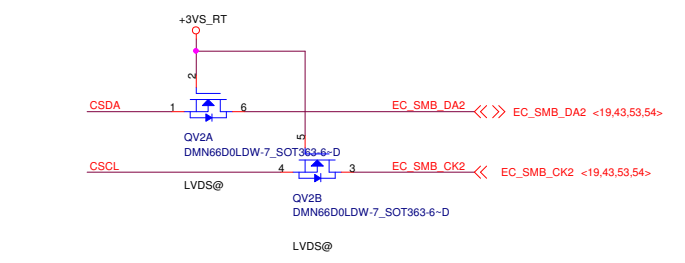
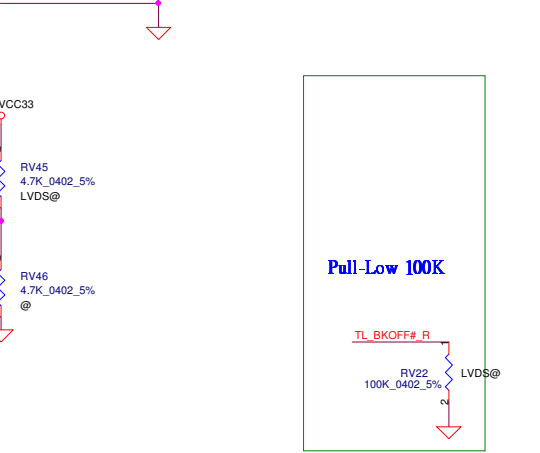
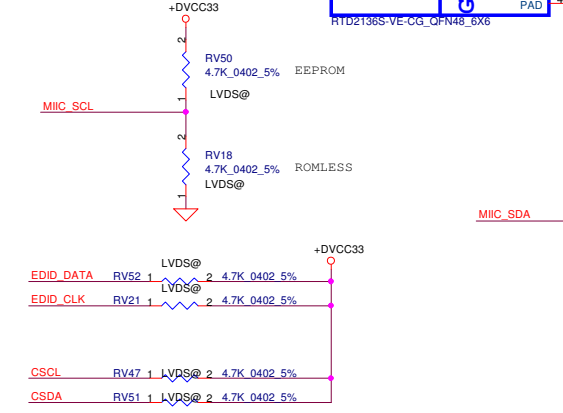
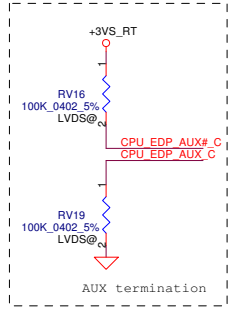
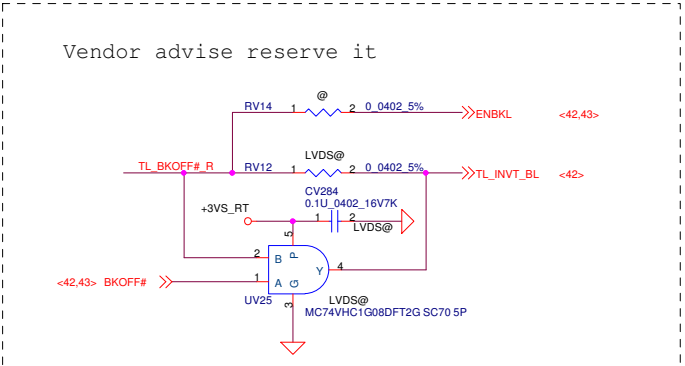
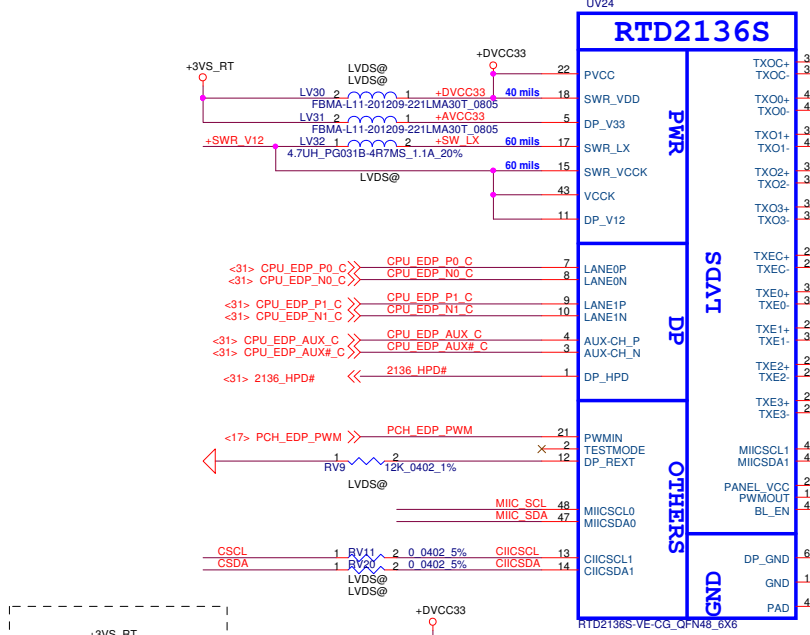
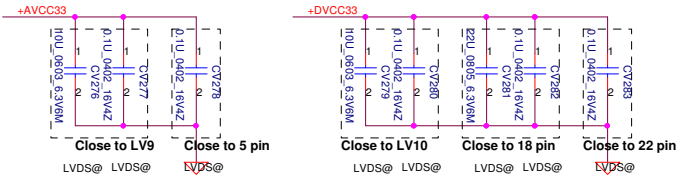
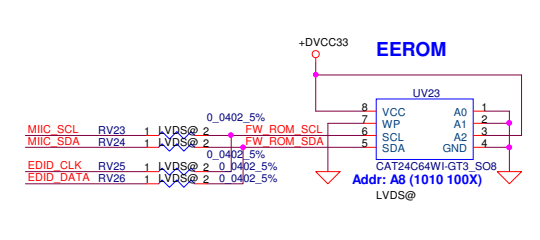
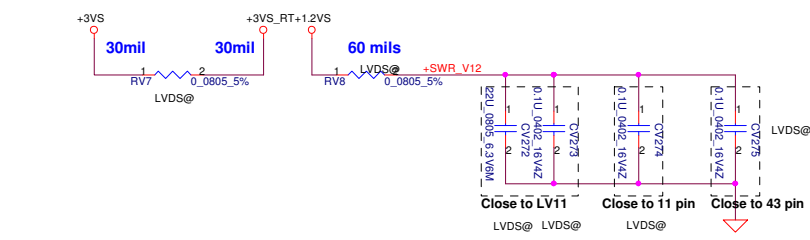
SEL	Y
0	IN1
1	IN2

PS121 CFG0/CFG1
SCLZ/SDAZ output voltage select;
CFG1:0=00 LOW-level input voltage: <0.40V LOW-level output voltage: 0.60V
PS121 PC0/PC1/PC2
Inputs equalization control, default inputs equalization setting at 12 dB
000: 12 dB, 001: 16 dB, 010: 10 dB, 011: 7 dB
100: 1.5 dB, 101: 4 dB, 110: 9 dB, 111: 7 dB

Place LC Filter closed to JHDMI

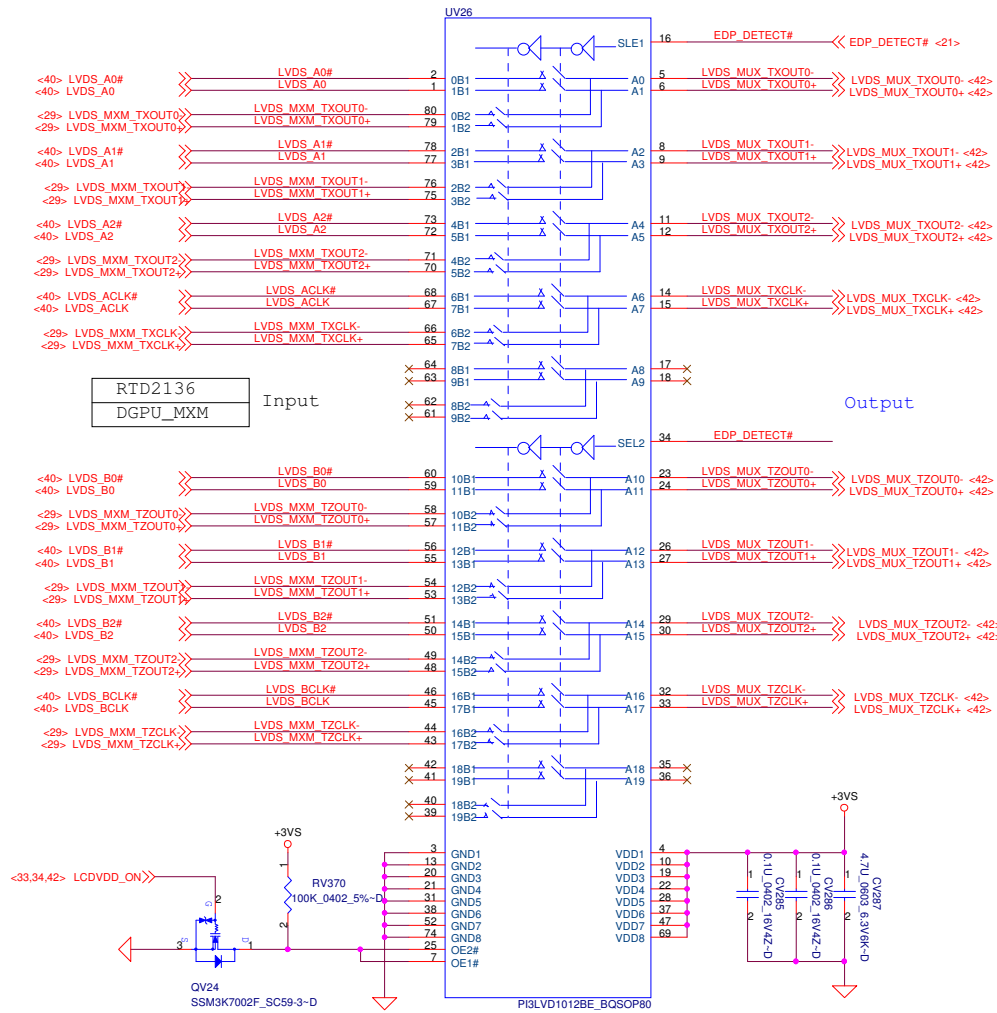
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Issued Date	2012/06/22	Deciphered Date
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		DP SW for DMC
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Compal Electronics, Inc.	
DP SW for DMC	
Document Number	
LA-931P	
Date	
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Date:	Friday, June 22, 2012	Sheet	37 of 61		

STDP6038 SW STDP4028 PCH/GPU AUX for LVDS

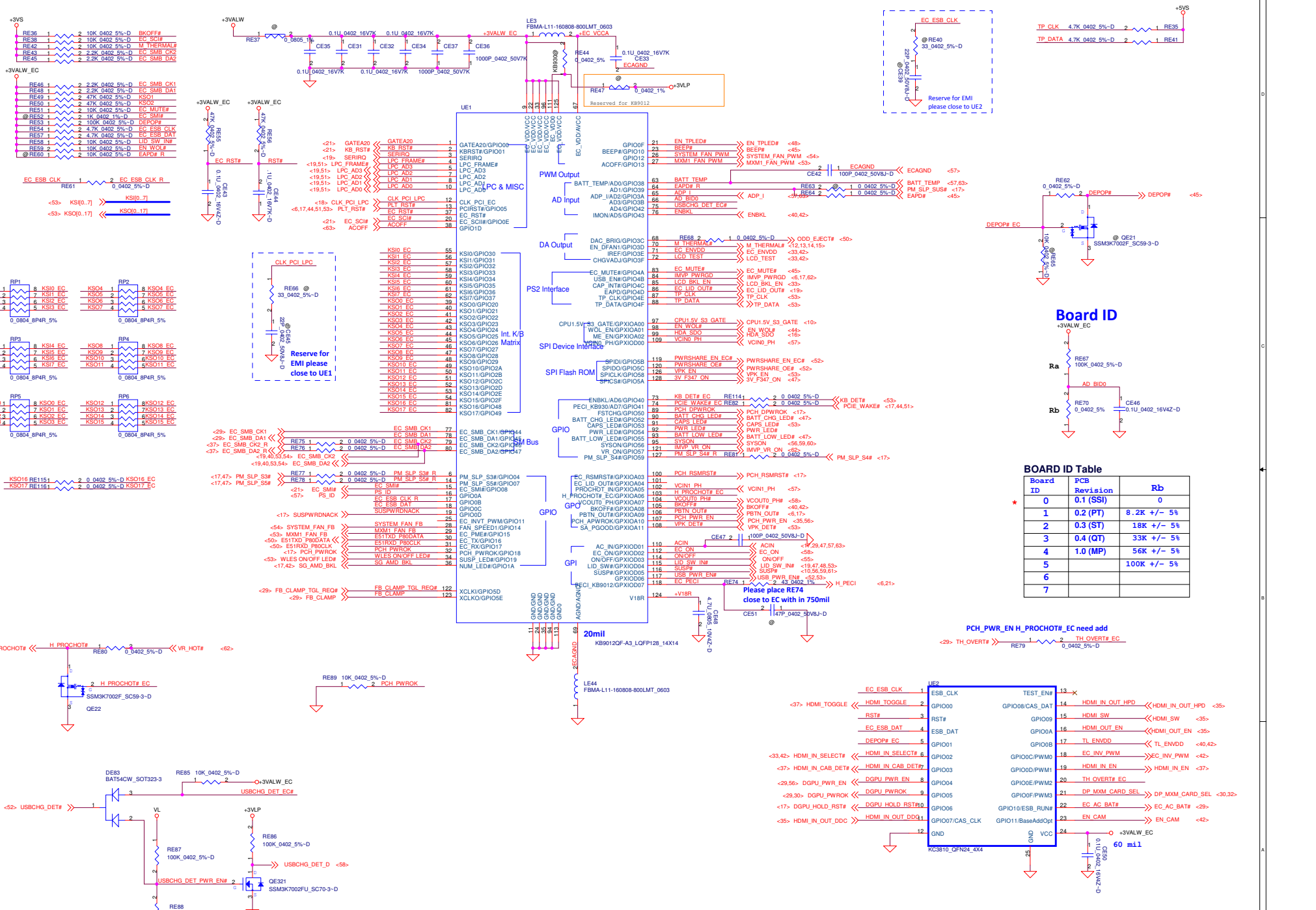


RTD2136
DGPU_MXM

Input

Output

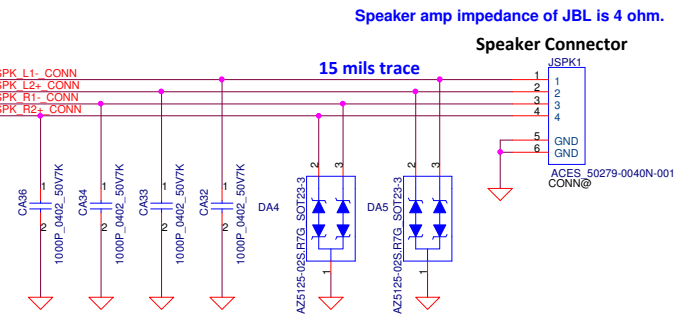
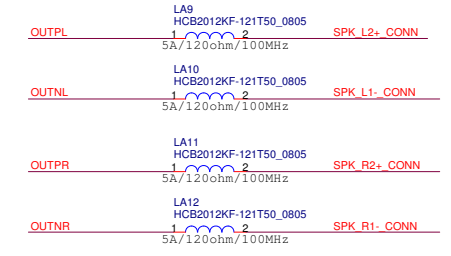
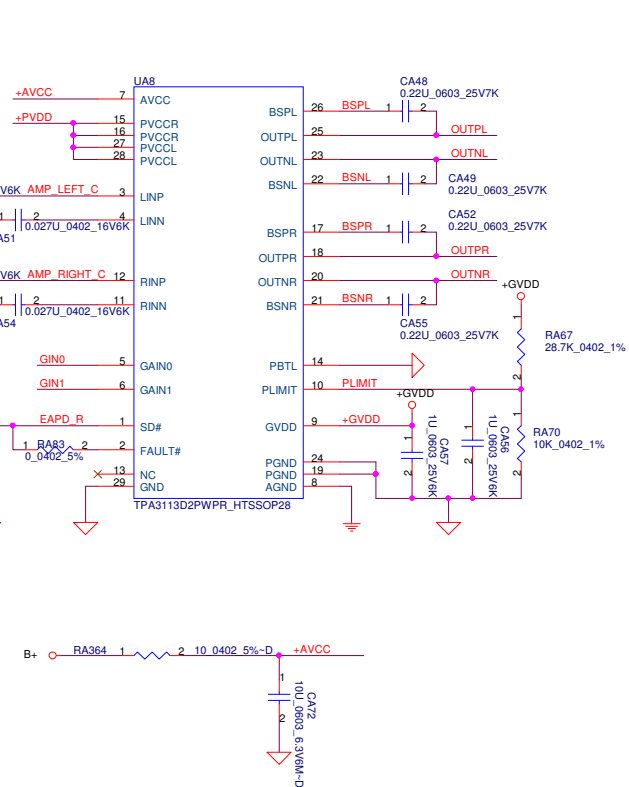
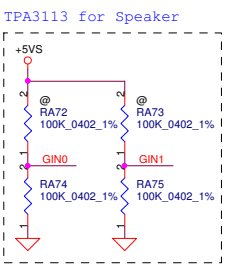
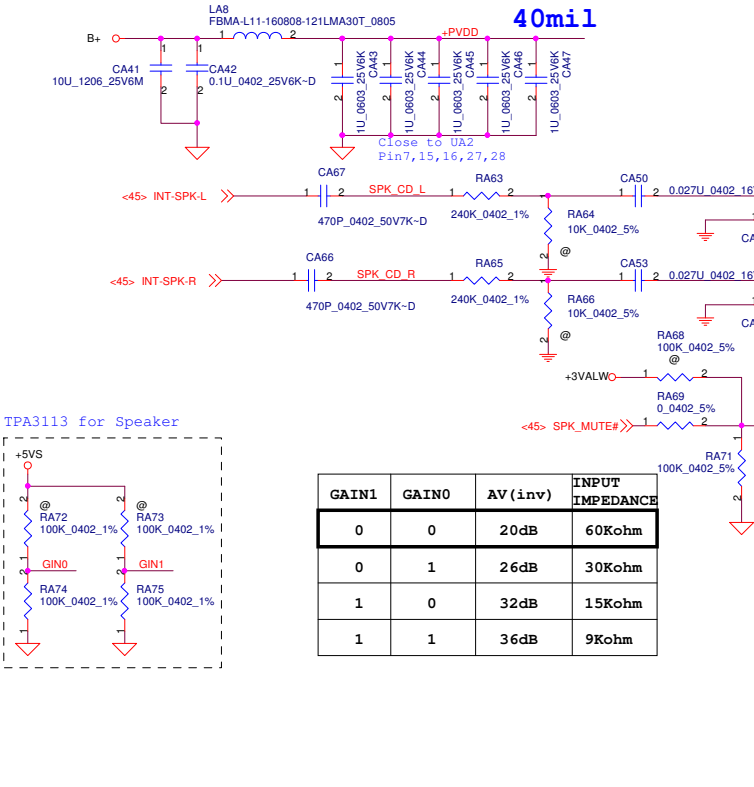
SEL	Y
L	RTD2136
H	DGPU_MXM

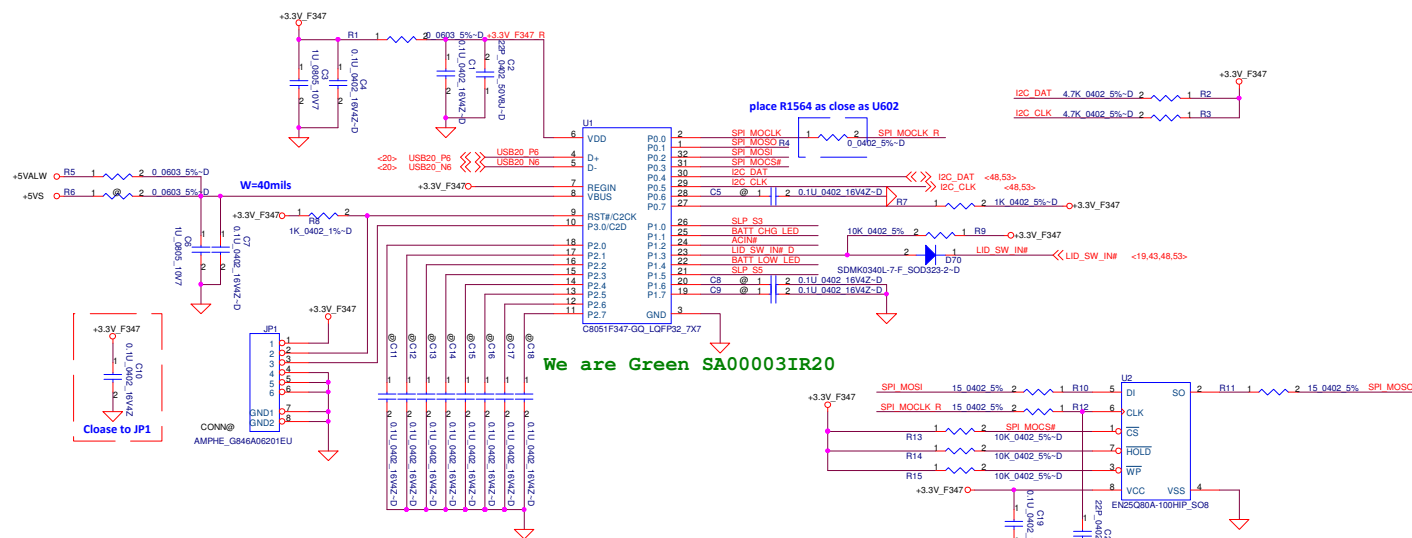


BOARD ID Table

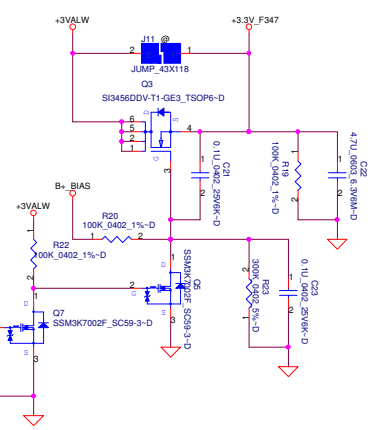
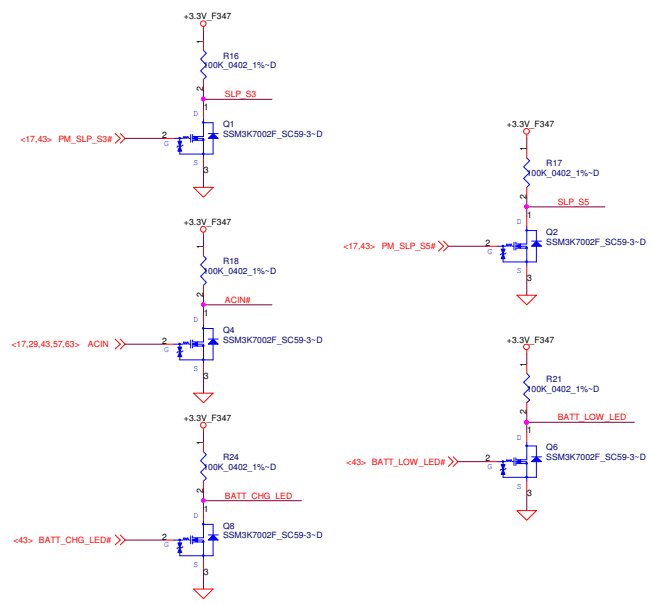
Board ID	PCB Revision	Rb
0	0.1 (SSI)	0
1	0.2 (PT)	8.2K +/- 5%
2	0.3 (ST)	18K +/- 5%
3	0.4 (QT)	33K +/- 5%
4	1.0 (MP)	56K +/- 5%
5		100K +/- 5%
6		
7		

* H_PROCHOT# EC need add
 -> TH_OVERT# EC





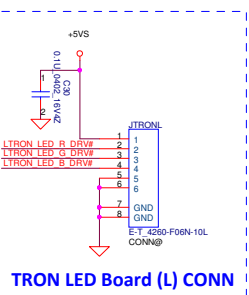
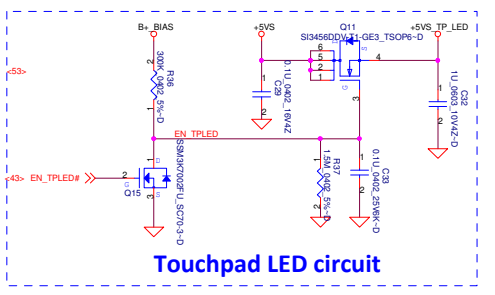
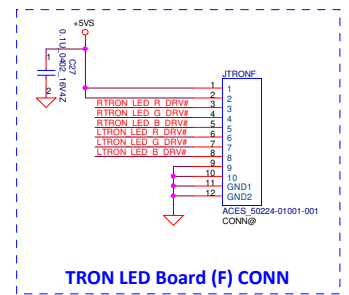
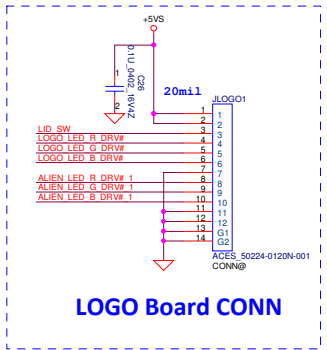
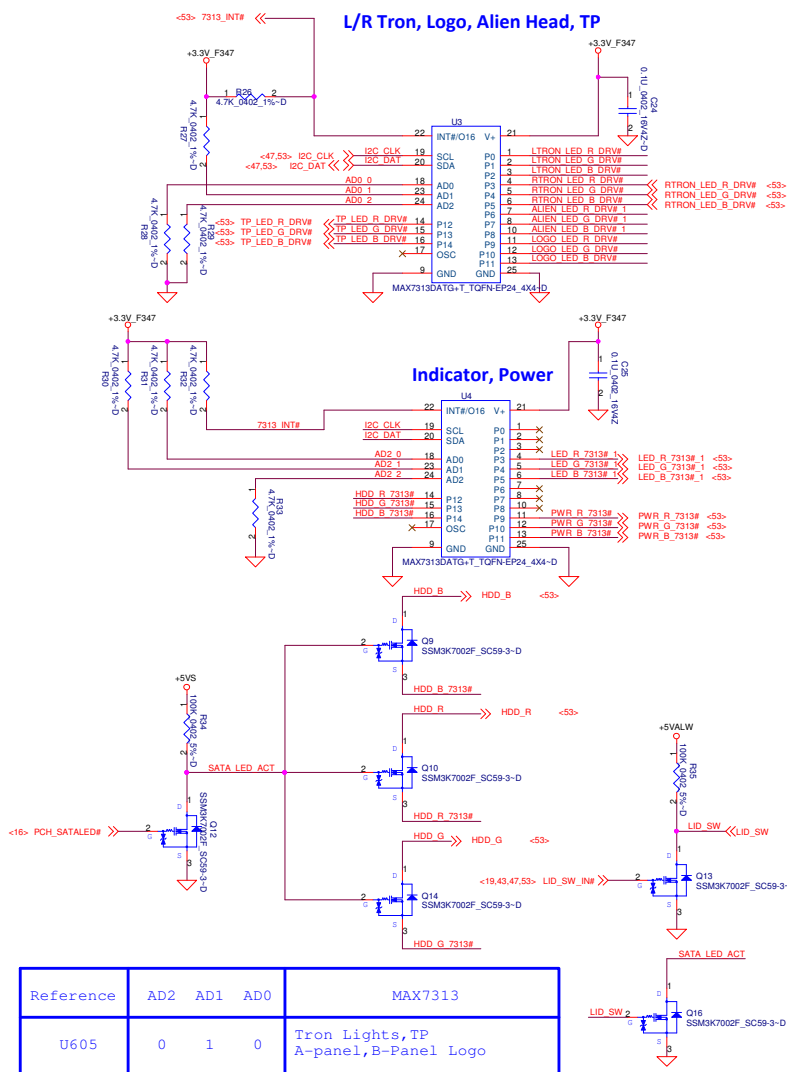
DEVICE	SMBUS ADDRESS
MAXIM - LED	0100 000b
MAXIM - GPIO	0100 001b
I2C EEPROM	1010 000b



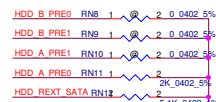
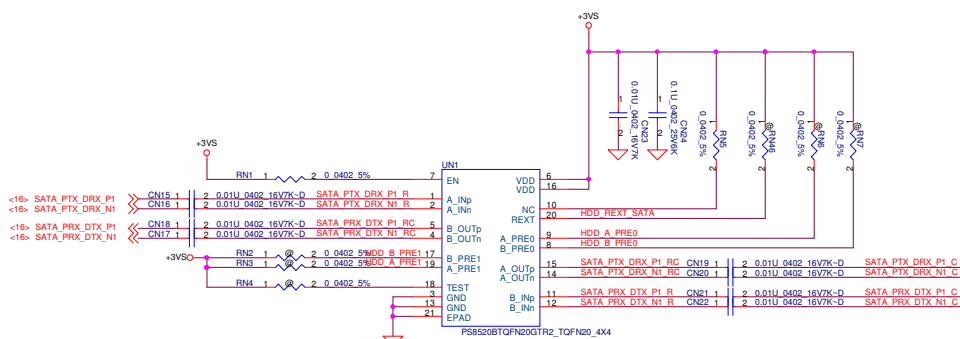
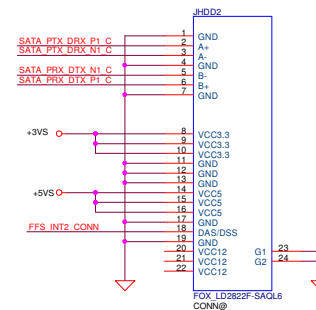
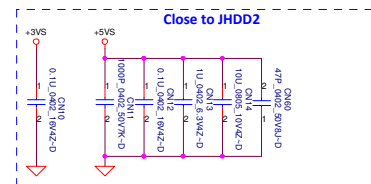
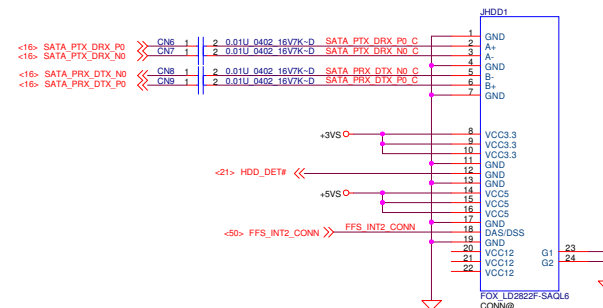
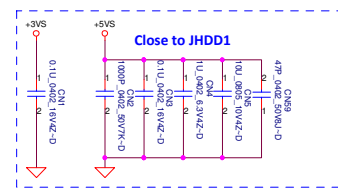
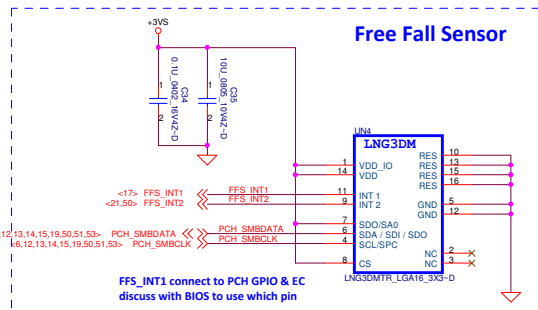
+3.3V F347 behavior

	STATE			
	S0	S3	S4	S5
AC IN	ON	ON	ON	ON
BAT only	ON	ON	OFF	OFF

AC mode battery full in S5=turn off ELC controller



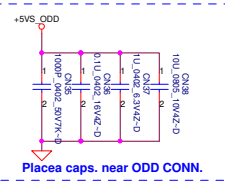
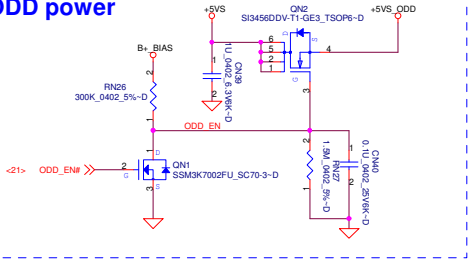
Reference	AD2	AD1	AD0	MAX7313
U605	0	1	0	Tron Lights, TP A-panel, B-Panel Logo
U608	0	1	1	Power Button, Media and Status LED Color
U?	1	0	0	Button, Indicator Brightness



Pin 20:
PARADE PS8250B:
Reserve RN46, Mount RN12
PERICOM PI3EQX6741ST:
Mount RN46, Reserve RN12
ASMEDIA ASM1466:
Mount RN46, Reserve RN12

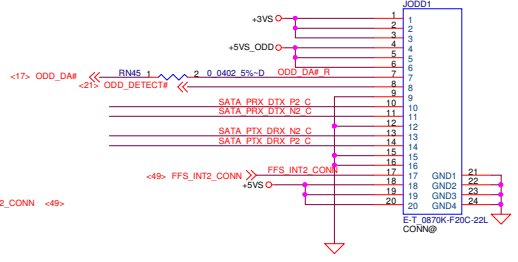
Pin 9:
PARADE PS8250B:
Reserve RN11.
PERICOM PI3EQX6741ST:
Reserve RN11
ASMEDIA ASM1466:
Mount RN11 to pull down

ODD power

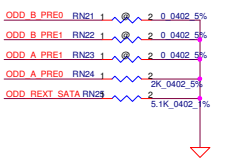
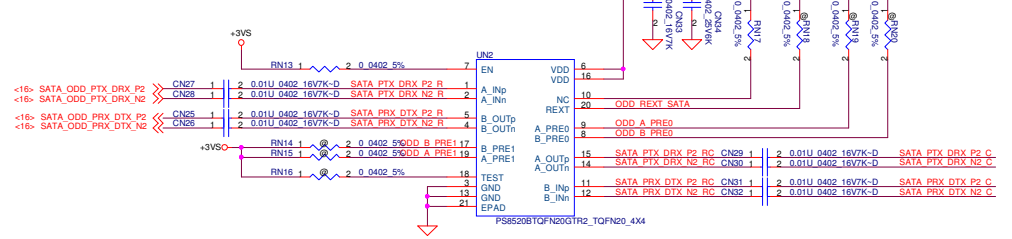


1. Host generate Low pulse 40ms to eject ODD
2. After this pulse, signal remain high and no pulse is allowed within 7s

SATA ODD Conn.

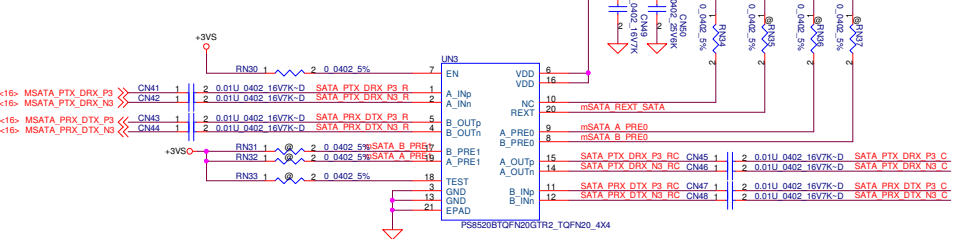


ODD Redriver

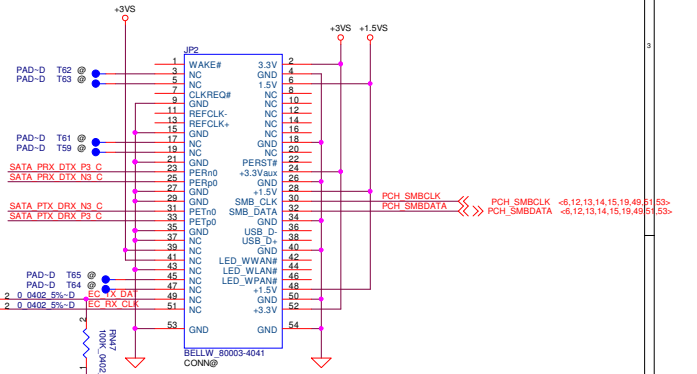
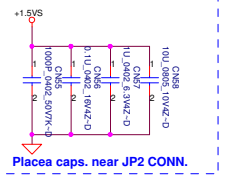
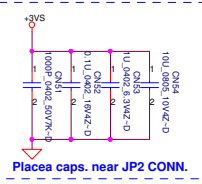


- Pin 20: PARADE PS8250B: Reserve RN18, Mount RN25
- Pin 9: PARADE PS8250B: Reserve RN24
- PERICOM P13EQX6741ST: Mount RN18, Reserve RN25
- PERICOM P13EQX6741ST: Reserve RN24
- ASMEEDIA ASM1466: Mount RN18, Reserve RN25
- ASMEEDIA ASM1466: Mount RN24 to pull down

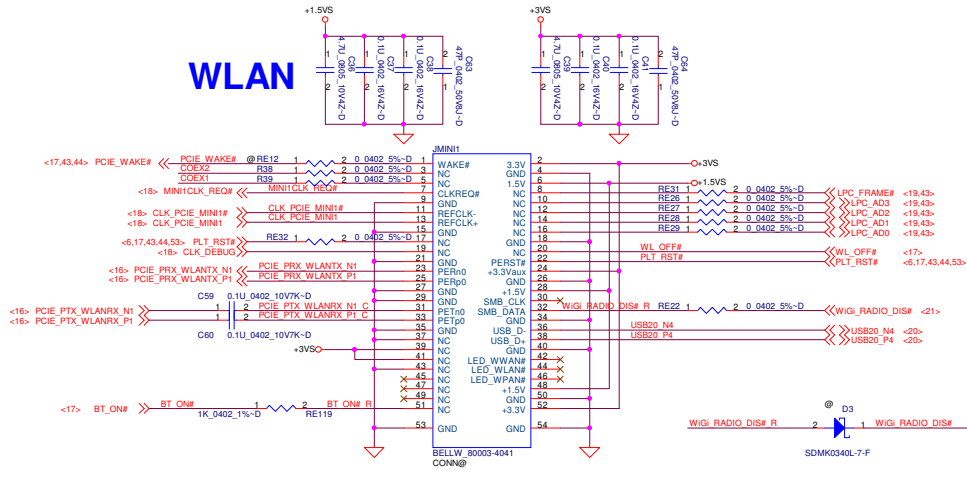
m-SATA Re-Driver



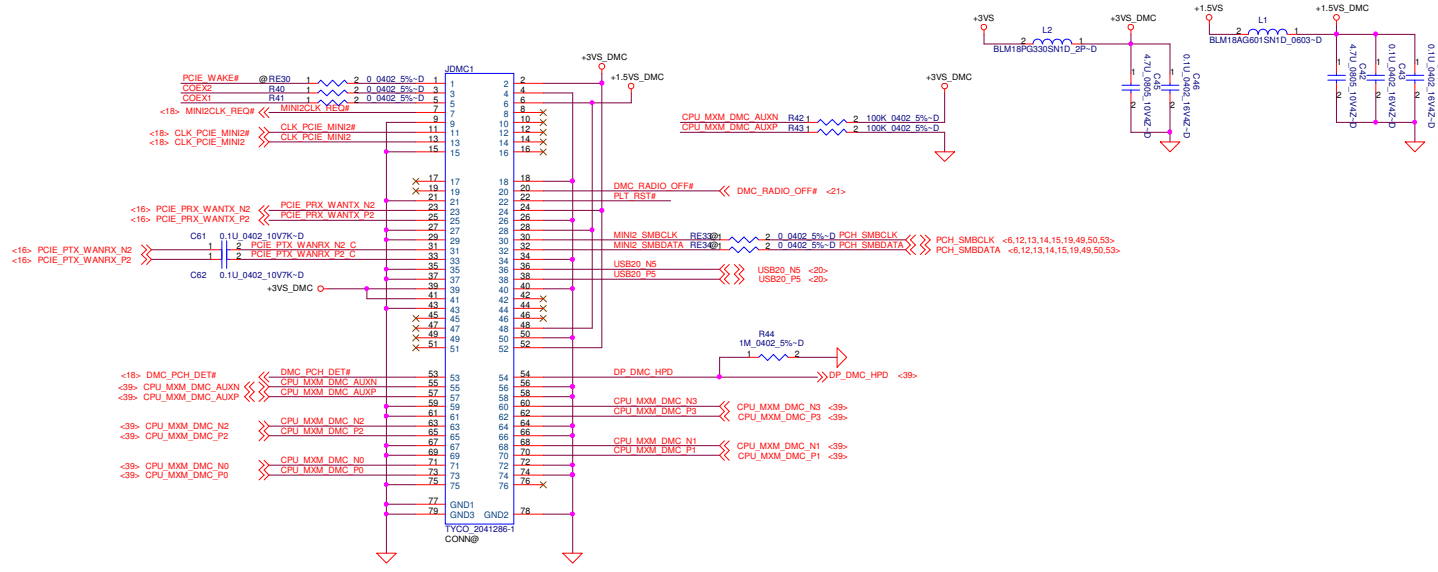
- Pin 20: PARADE PS8250B: Reserve RN35, Mount RN42
- Pin 9: PARADE PS8250B: Reserve RN41
- PERICOM P13EQX6741ST: Mount RN35, Reserve RN42
- PERICOM P13EQX6741ST: Reserve RN41
- ASMEEDIA ASM1466: Mount RN35, Reserve RN42
- ASMEEDIA ASM1466: Mount RN41 to pull down



WLAN

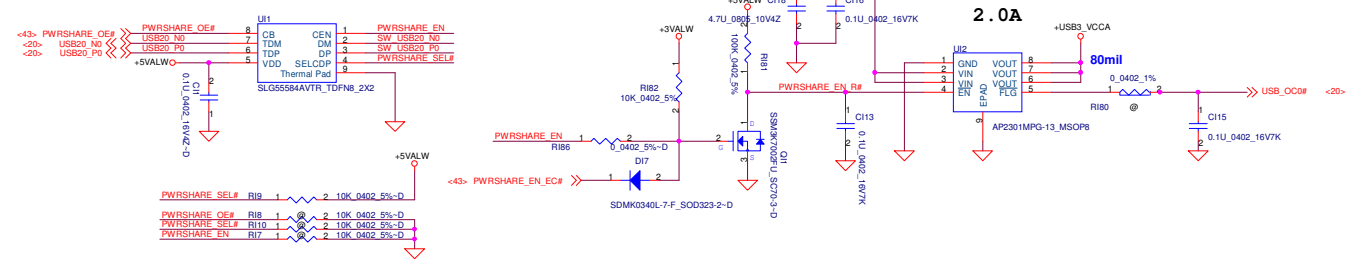


Display Mini Card (DMC)

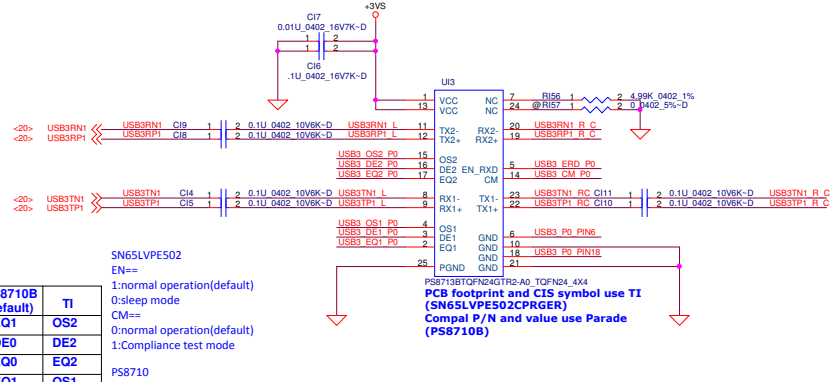
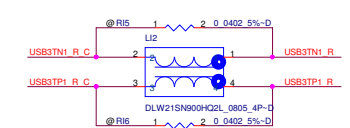
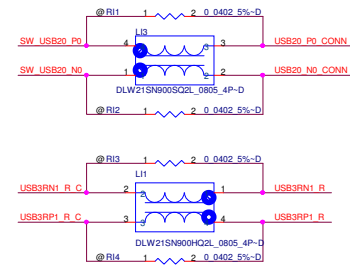
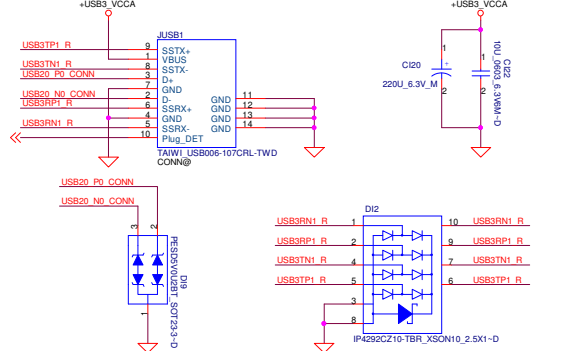


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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Mini Card -WLAN/DMC/BT
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Power share

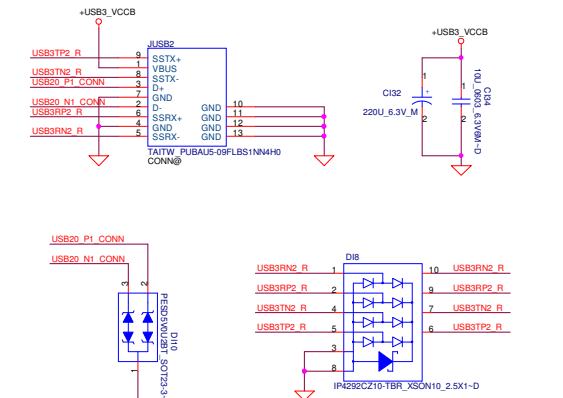
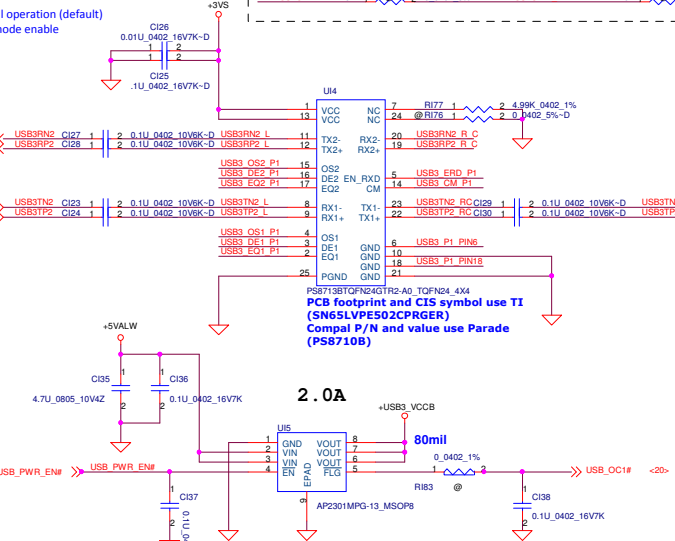
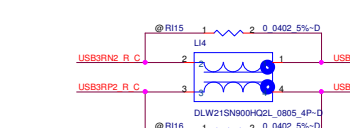
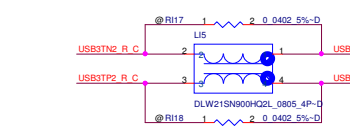
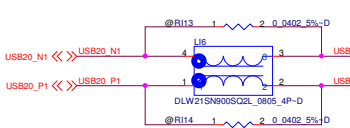
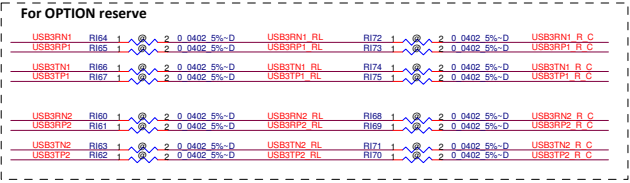


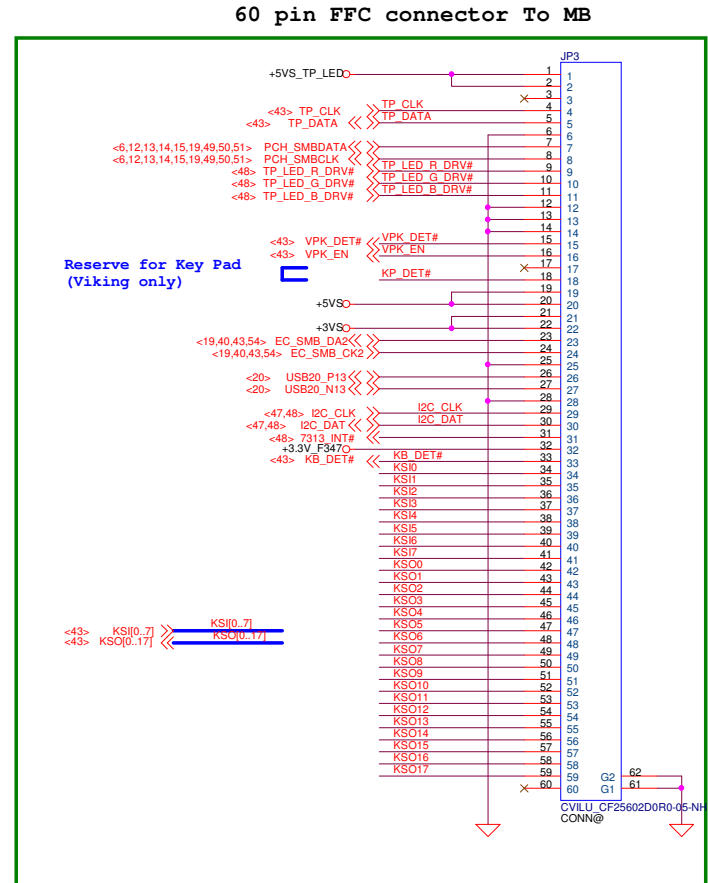
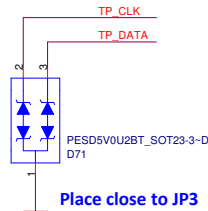
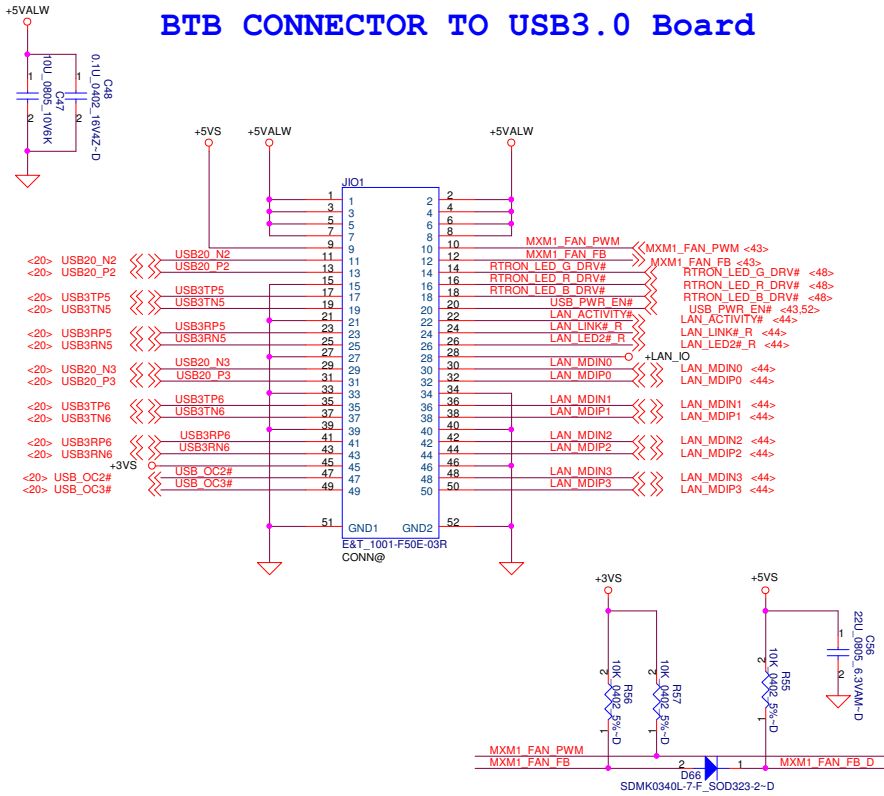
USB CONN



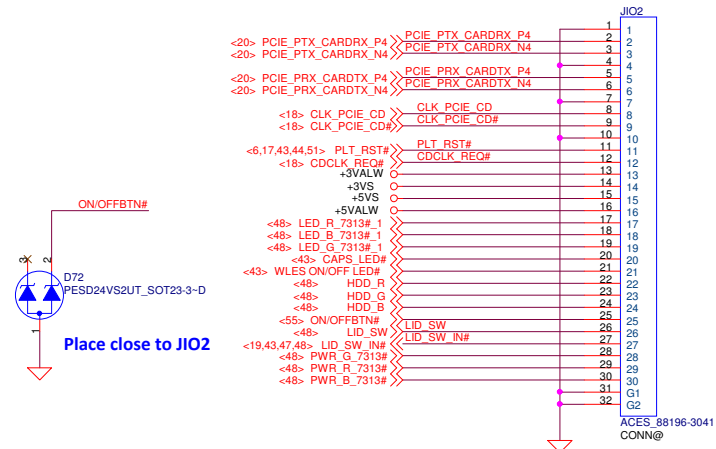
Vendor pin	PS8710B (default)	TI
pin15	AEQ1	OS2
pin16	ADE0	DE2
pin17	AEQ0	EQ2
pin4	BEQ1	OS1
pin3	BDE0	DE1
pin2	BEQ0	EQ1
pin5	PD	EN_RXD
pin14	TEST	CM
pin18	ADE1	
pin6	BDE1	

SN65LVPE502
 EN==
 1: normal operation (default)
 0: sleep mode
 CM==
 0: normal operation (default)
 1: compliance test mode
 PS8710
 [A(B)_DE1, A(B)_DE0] ==
 LL: 3.5dB de-emphasis
 LH: No de-emphasis
 HL: 7dB de-emphasis
 HH: 5dB with boost output swing
 [A(B)_EQ1, A(B)_EQ0] ==
 LL: reserved
 LH: program EQ for channel loss up to 7dB
 HL: program EQ for channel loss up to 14.5dB
 HH: program EQ for channel loss up to 11.5dB
 TEST ==
 L: Normal operation (default)
 H: Test mode enable



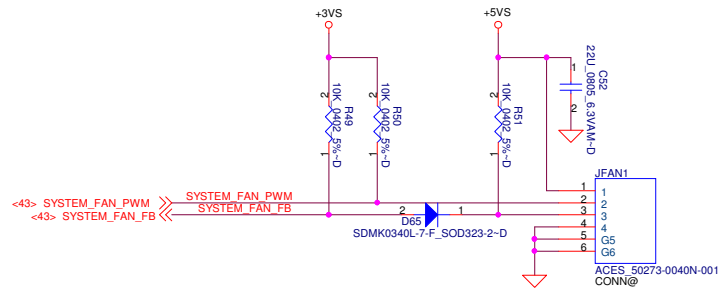
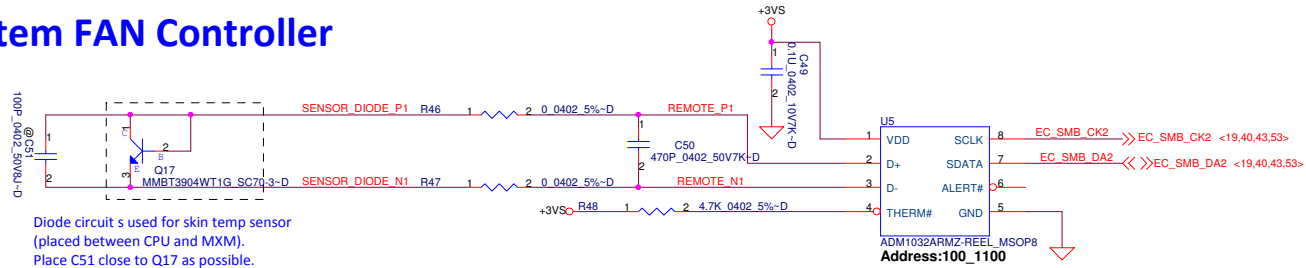


30pin Connector to CardReader

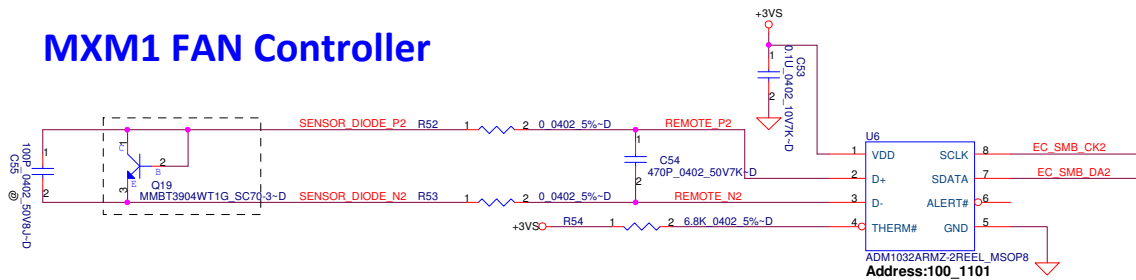


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	Issued Date	2012/06/22	Deciphered Date	2013/06/21		IO BTB CONN
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System FAN Controller

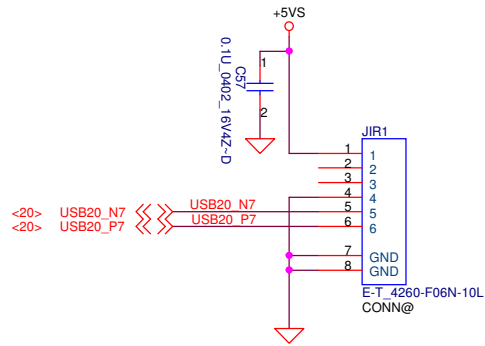


MXM1 FAN Controller

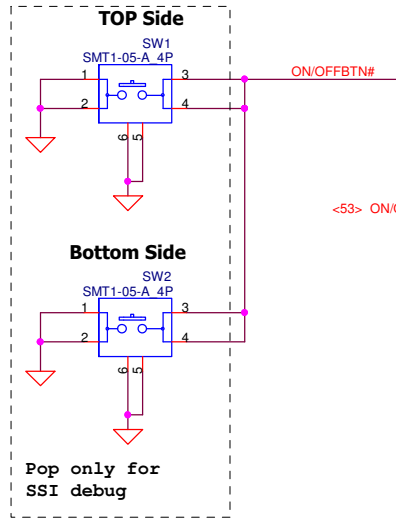


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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Compal Electronics, Inc.	
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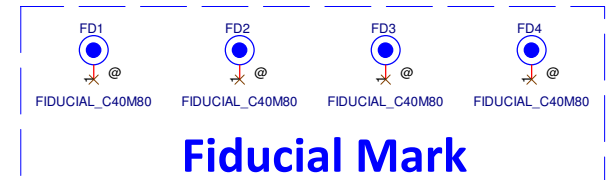
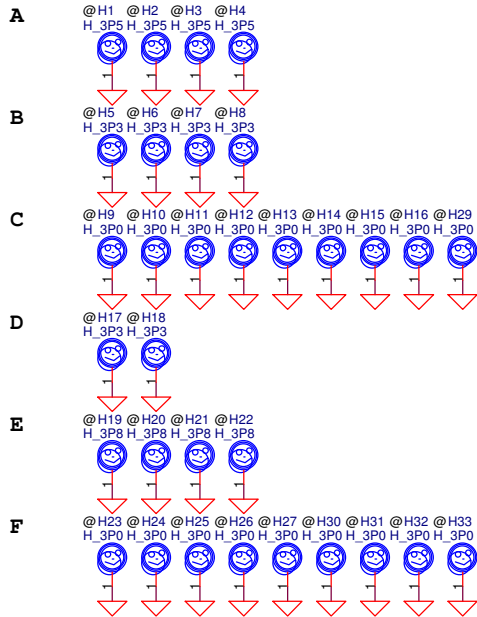
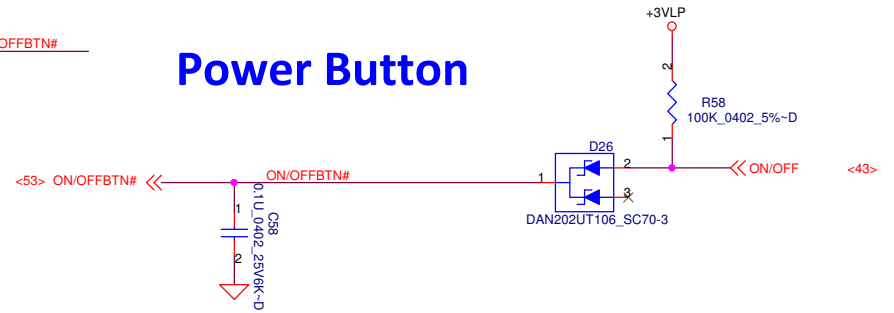
IR SENSOR connector



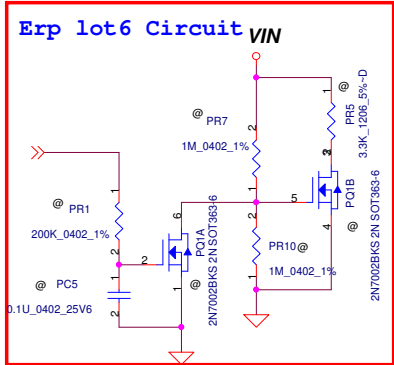
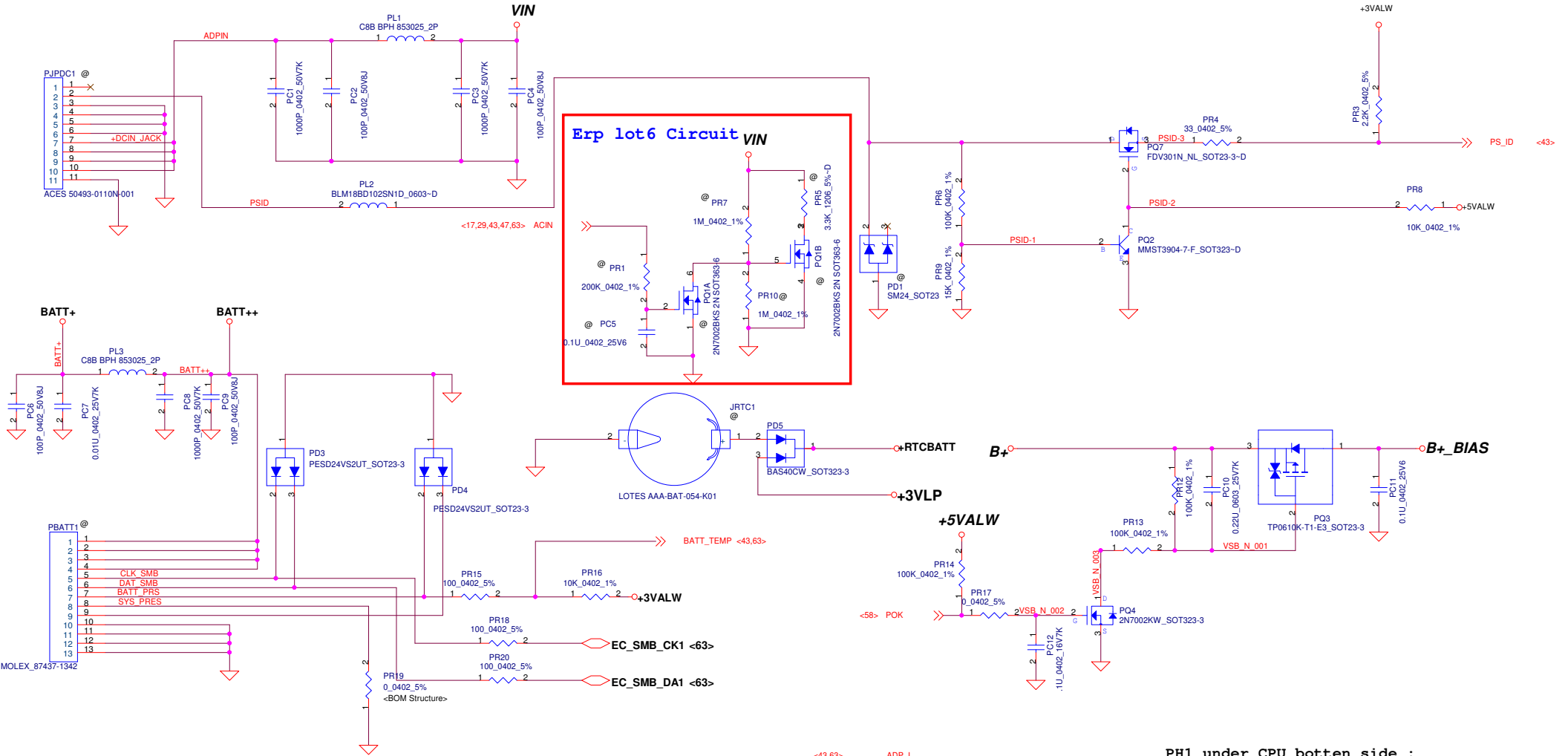
ON/OFF switch



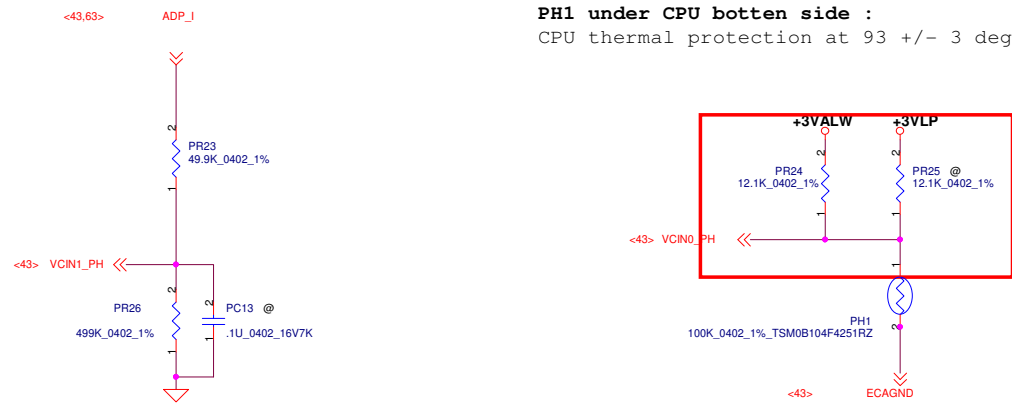
Power Button



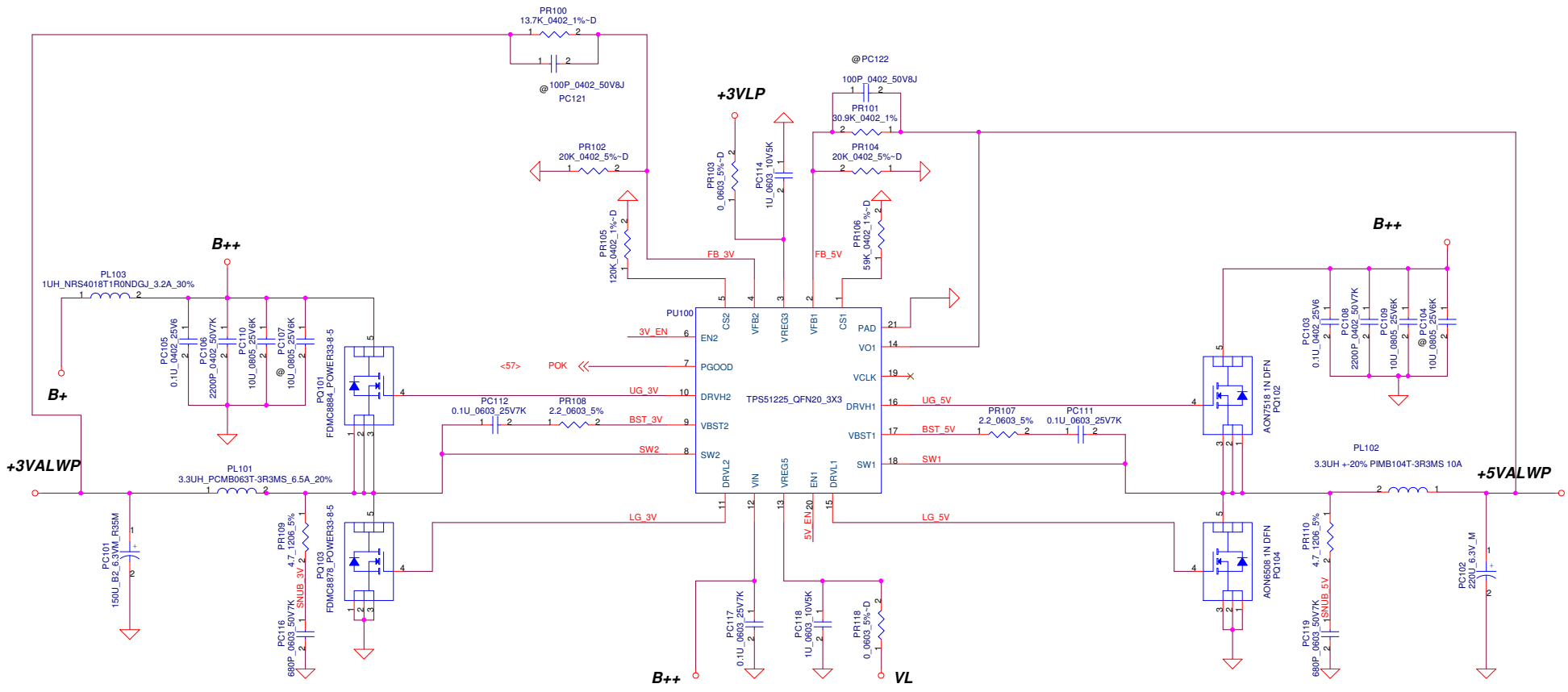
Security Classification	Compal Secret Data			Title	KB & Power Button & IR	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	Size	Document Number	Rev
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PH1 under CPU bottom side :
CPU thermal protection at 93 +/- 3 degree C

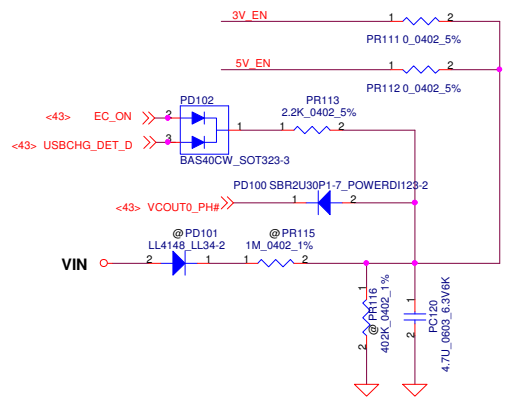


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Issued Date	2012/06/22	Deciphered Date	2013/06/21	Title	
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3VALWP
 TDC 6.08A
 Peak Current 8.11A
 OCP current 9.73A

	TYP	MAX
H/S Rds (on)	:22mohm	30mohm
L/S Rds (on)	:12.1mohm	17mohm



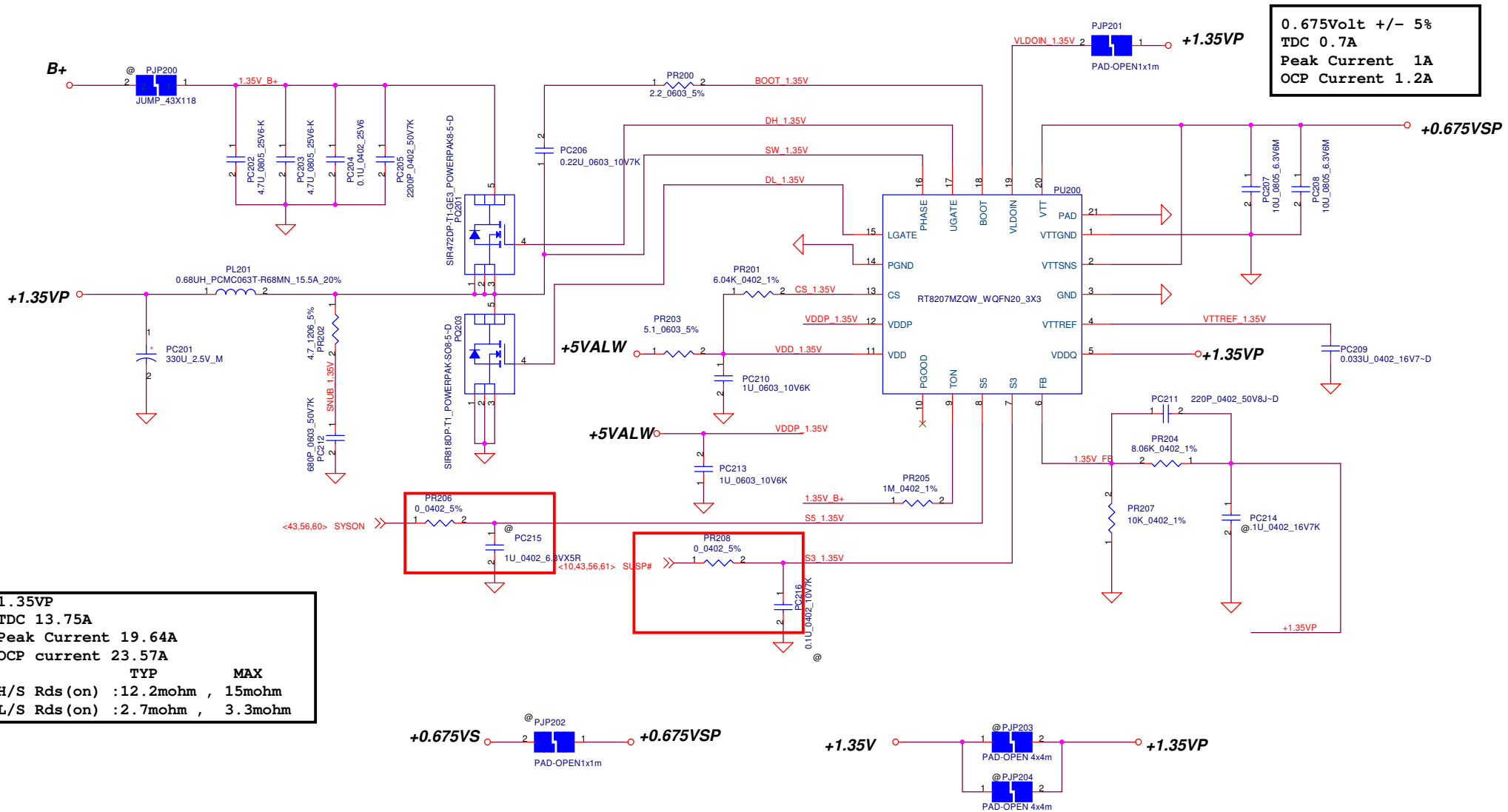
5VALWP
 TDC 10.64A
 Peak Current 14.19A
 OCP current 17.03A

	TYP	MAX
H/S Rds (on)	11.2mohm	14mohm
L/S Rds (on)	:3.7mohm	5mohm

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Issued Date	2012/06/22	Deciphered Date
		2013/06/21

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Title	PWR-3VALWP/SVALWP
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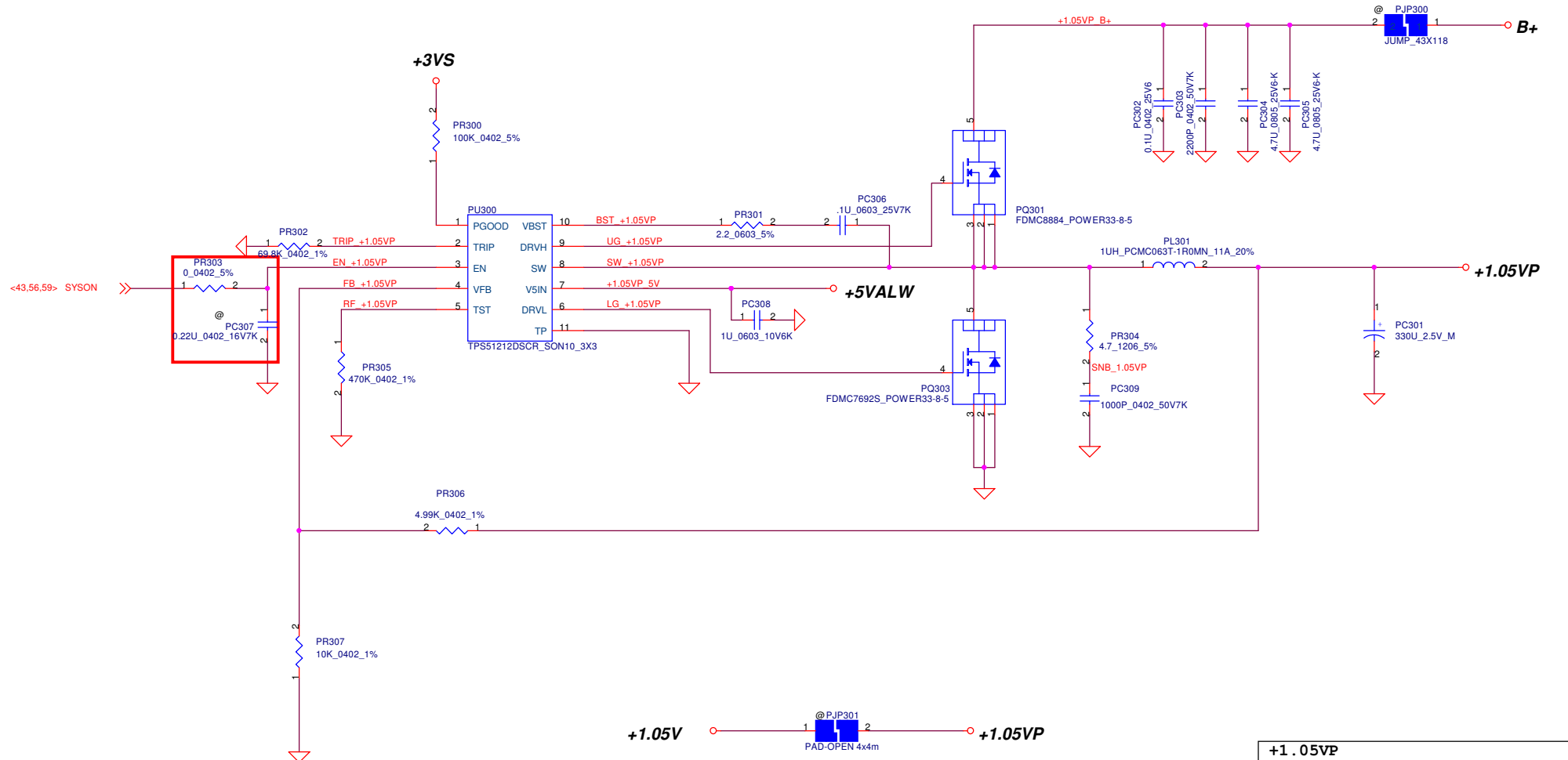


0.675V_{olt} +/- 5%
 TDC 0.7A
 Peak Current 1A
 OCP Current 1.2A

1.35VP
 TDC 13.75A
 Peak Current 19.64A
 OCP current 23.57A

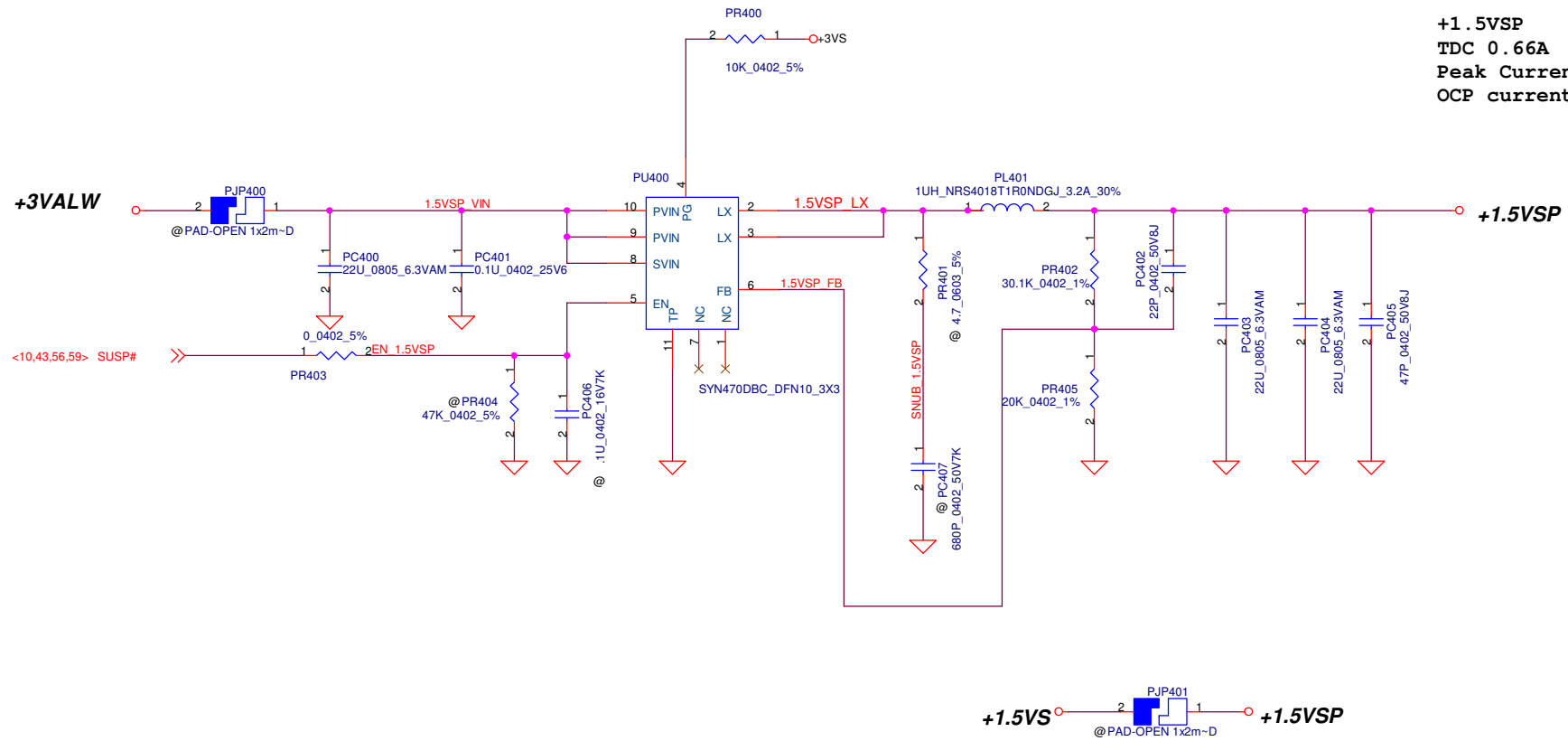
TYP		MAX	
H/S Rds (on)	: 12.2mohm	,	15mohm
L/S Rds (on)	: 2.7mohm	,	3.3mohm

Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	PWR-1.35VP/0.675VSP	
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+1.05VP	
TDC 4.56A	
Peak Current 6.51A	
OCP current 7.81A	
	TYP MAX
H/S Rds (on)	: 22mohm , 30mohm
L/S Rds (on)	: 10.8mohm , 13.6mohm

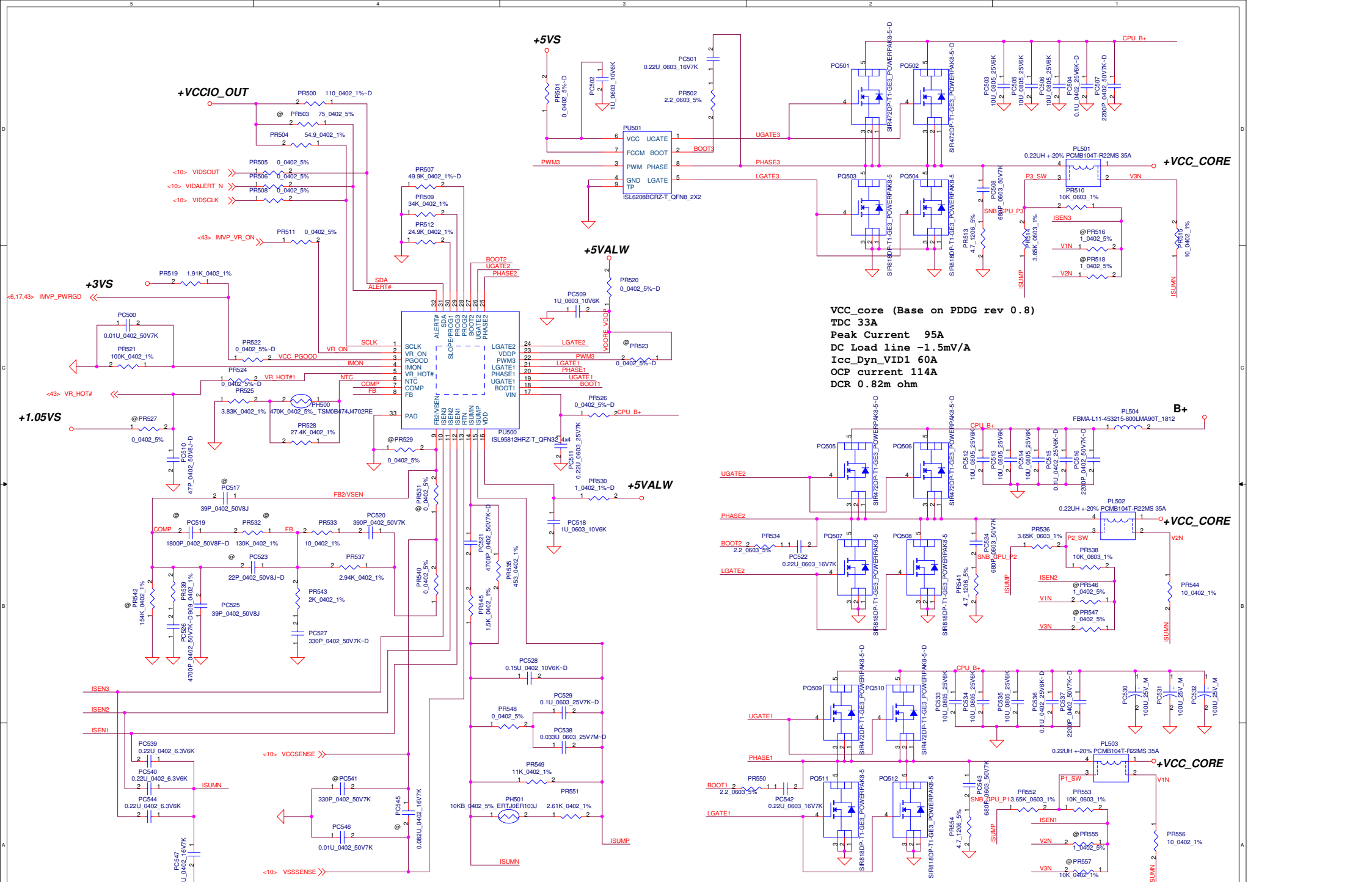
Security Classification		Compal Secret Data		Title	
Issued Date	2012/06/22	Deciphered Date	2013/06/21	PWR+1.05VP	
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Compal Electronics, Inc.		
Title		
PWR-1.5VSP		
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VCC_core (Base on PDDG rev 0.8)
TDC 33A
Peak Current 95A
DC Load line -1.5mV/A
Icc_Dyn_VID1 60A
OCp current 114A
DCR 0.82m ohm

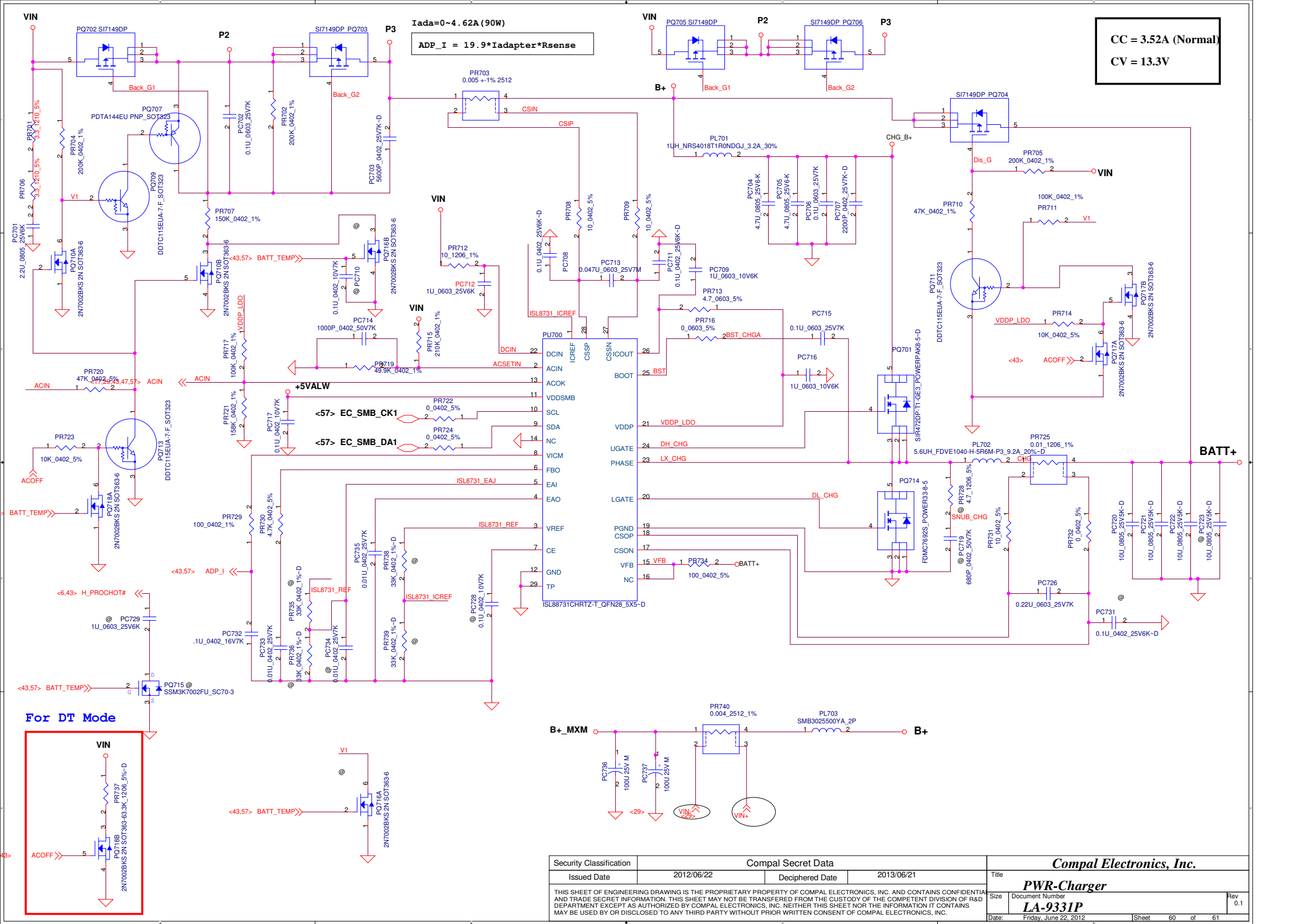
Local sense put on HW site

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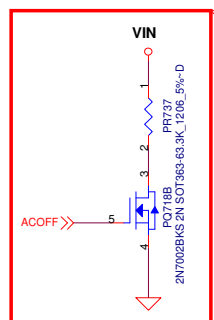
File		+VCC_CORE	
Size	Document Number	LA-9331P	
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Tada=0~4.62A (90W)
 $ADP_I = 19.9 * I_{adapter} * R_{sense}$

CC = 3.52A (Normal)
 CV = 13.3V

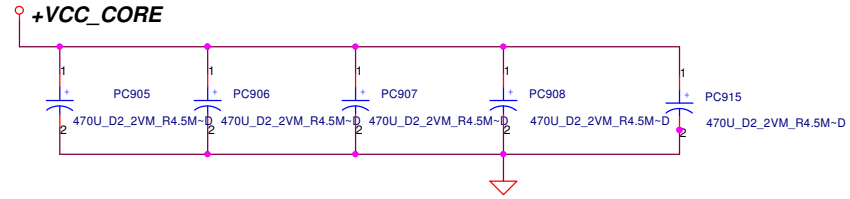
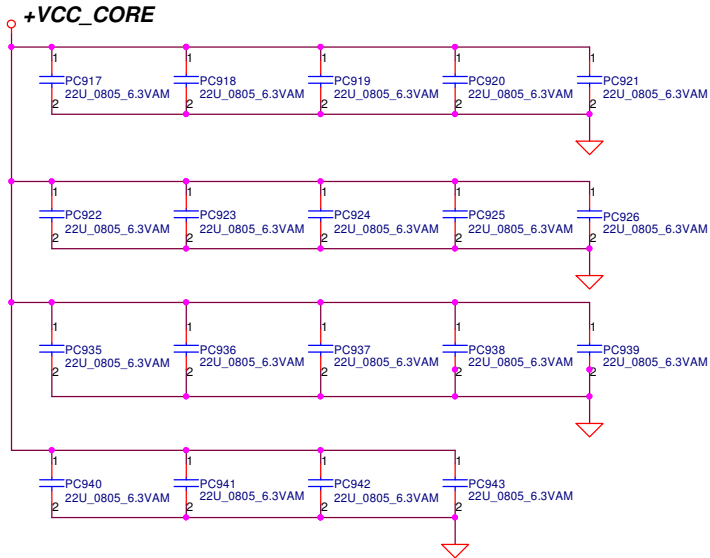
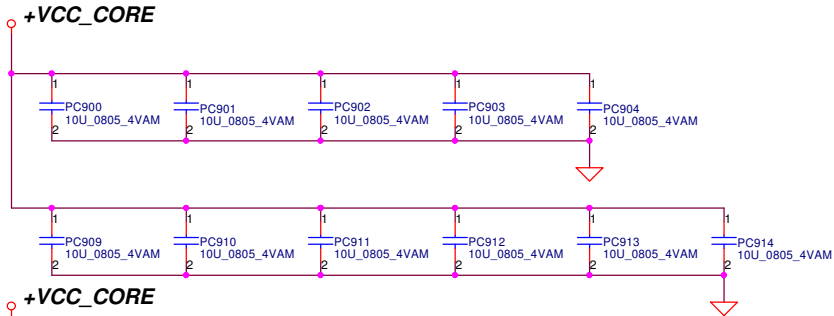
For DT Mode



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PWR-Charger	
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Based on PDDG rev 0.8 Table 5-1.



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			Compal Electronics, Inc.	
Title			PROCESSOR DECOUPLING	
Size	Document Number			Rev
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