

First International Computer, Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : AMD S1 + Nvidia C51D + MCP51

Version : 0.1

Initial Date : 05/13/2006

Confidential

Manager Sign by : Avery Lee

Drawing by : Jason Lee

Total confirm by : Adam Cho

		First International Computer, Inc. 3FL, NO.300, Yang Guang St., Nei-Hu 114 TAIPEI, TAIWAN, ROC (886)-2-6751-8751	
		Confidential	
Title: PA1538/XA1526(FSC) PTB50/XTB70(FIC)			
Size C	Document Number TITLE		Rev 0.1
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1. Schematic Page Description :

FIC Schematic Ver : 0.1

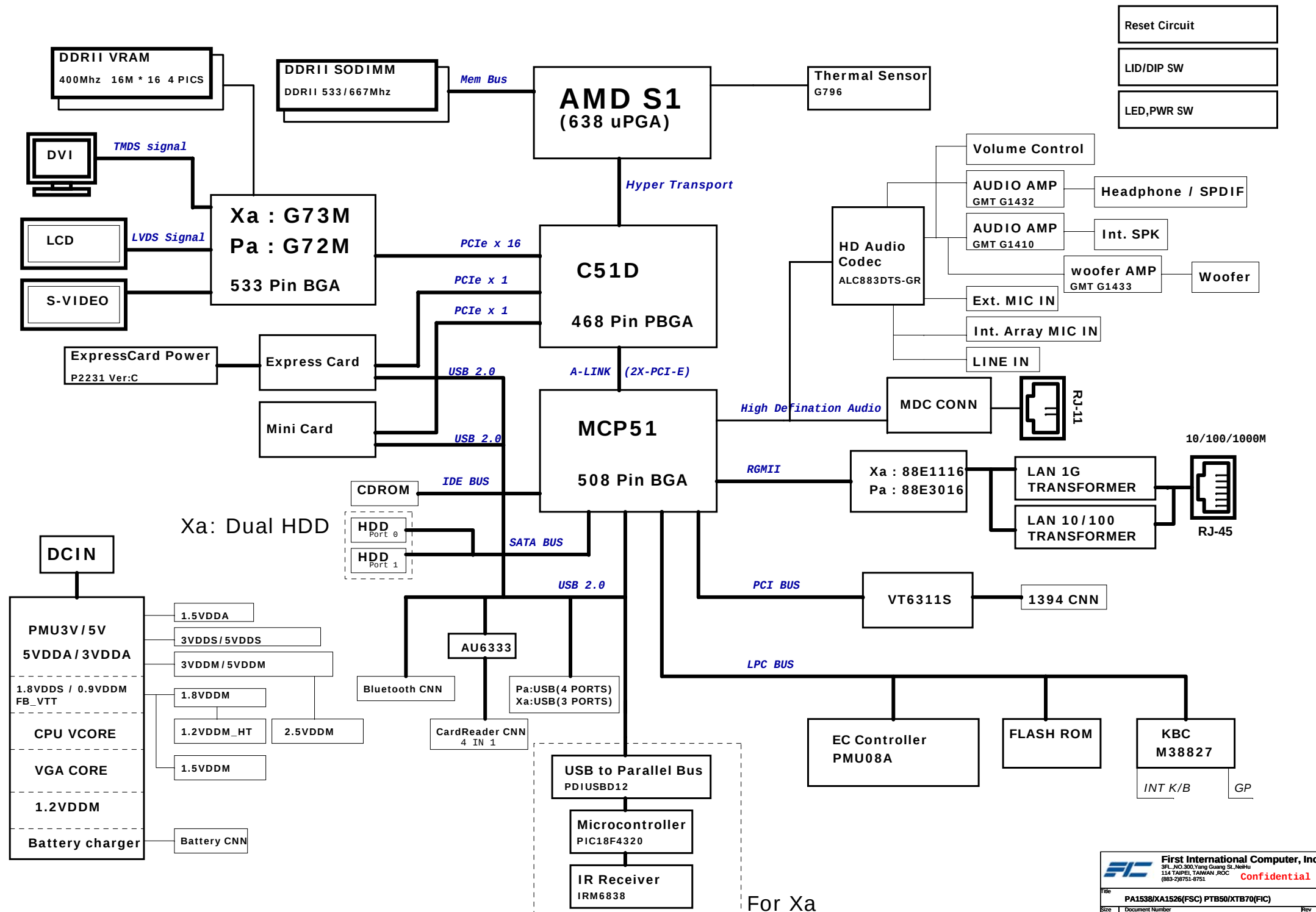
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6. AMD S1 HT(1/3)	26. VGA DDR2_C CHANNEL	46. KBC / GP CNN
7. AMD S1 DDR(2/3)	27. DVI Port	47. DIP/LID SW; SCREW
8. AMD S1 POWER(3/3)	28. LCD CNN	48. PMU08A
9. CPU Thermal/Fan CNN	29. TV Port	49. Power Block Diagram
10. C51D_HT (1/3)	30. 1394 VIA VT6311S	50. CPU CORE (MAX8774)
11. C51D_PCIE (2/3)	31. Cardreader AU6333	51. ACIN / DCIN
12. C51D_POWER(3/3)	32. New Card(express card)	52. Battery CNN
13. DDRII SO-DIMM 0 RSV	33. PCIE Mini Card	53. Charger MB3887
14. DDRII SO-DIMM 1 STD	34. GIGA PHY 88E1116	54. 5VDDA / 3VDDA
15. MCP51 HT(1/6)	35. GIGA TRANSFORMER	55. SYSTEM POWER
16. MCP51 PCI(E)/LPC (2/6)	36. FirmWare Hub	56. DDRII Power
17. MCP51 SATA/PATA(3/6)	37. USB CNN	57. VGA_VDD / 1.2V / 1.5V
18. MCP51 AC97/USB(4/6)	38. LED / SW	
19. MCP51 RGMII(5/6)	39. RTC/ BLUETOOTH CNN	
20. MCP51 POWER(6/6)	40. SATA HD / CD-ROM CNN	

2. PCI BUS Description :

IDSEL	CHIP
AD27	1394 VIA VT6311S

PCIINT	CHIP
IRQA	1394 VIA VT6311S
IRQB	---
IRQC	---
IRQD	---

BUSMASTER	
REQ	CHIP
REQ0 / GNT0	---
REQ1 / GNT1	1394 VIA VT6311S
REQ2 / GNT2	---
REQ3 / GNT3	---
REQ4 / GNT4	---



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
1.5VDDA	1.5V always on power rail by DCON or PSUSC0
5VDDS	5.0V power rail
3VDDS	3.3V power rail
1.8VDDS	1.8V power rail
FB_VTT	0.9V power rail for VGA
0.9VDDM	0.9V DDR Termination Voltage
5VDDM	5.0V suspend power rail
3VDDM	3.3V suspend power rail
2.5VDDM	2.5V suspend power rail
1.5VDDM	1.5V suspend power rail
VDD_CORE	Core Voltage for VGA
VCPU_CORE	Core Voltage for CPU
1.2VDDM	VCC For CPU & NB
+1.2VHT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal
---	---	-------------------

Signal Conditioning

D	=	Damped (by a resistor)
Q	=	Isolated (by a Q-switch)
L	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

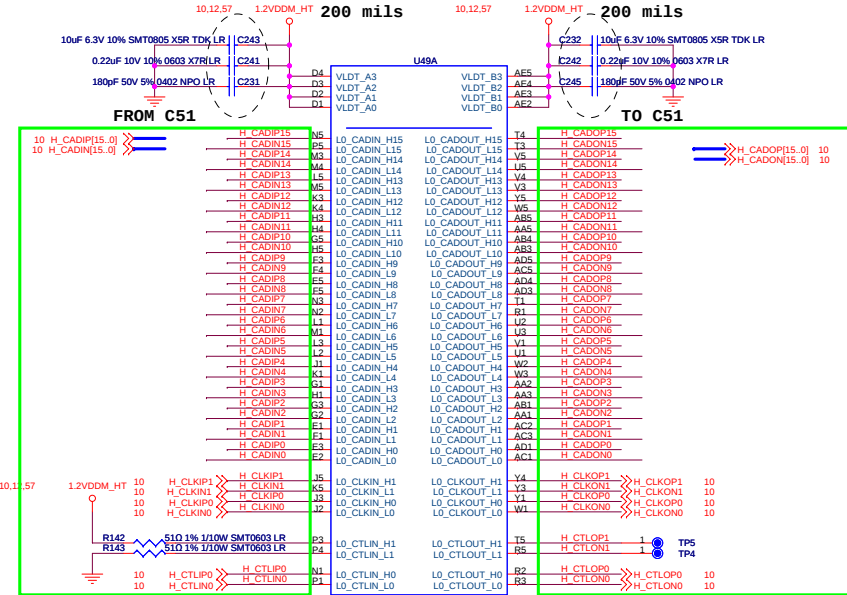
Layer 1		TOP
Layer 2		GND
Layer 3		IN1/Mixer
Layer 4		GND
Layer 5		VCC
Layer 6		IN2/Mixer
Layer 7		GND
Layer 8		BOTTOM

6.Schematic modify Item and History :

ClawHammer HT Interface

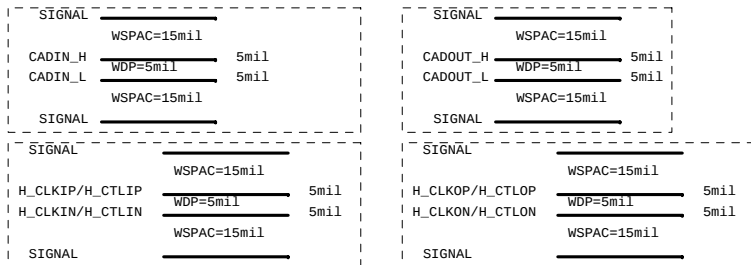
LAYOUT: Route 2.5VCCA approx. 50mil wide and 500mils long.(Reference to ground)

Close to SOCKET754



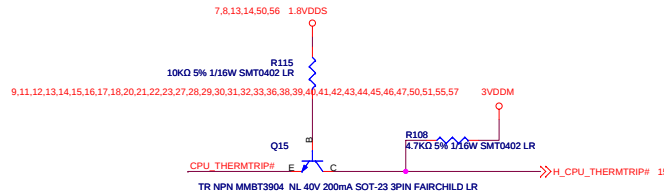
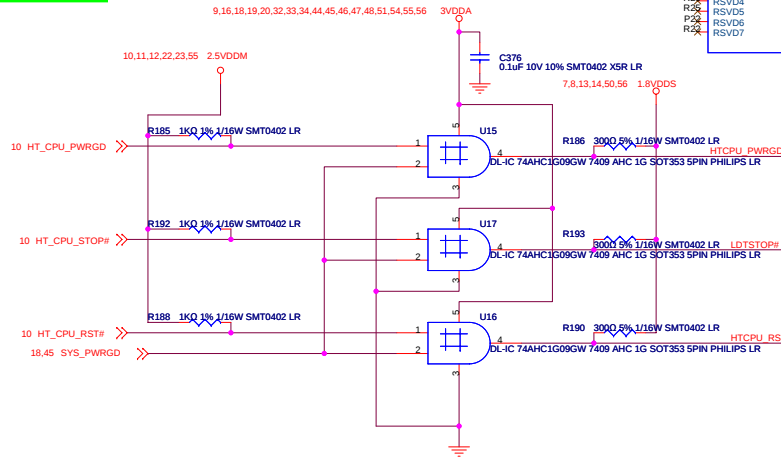
HT BUS General Routing Rules:

1. HT BUS is easy to route, and uses minimal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.



Route as Diff 5/5/5/20

Route as Diff 5/5/5/20



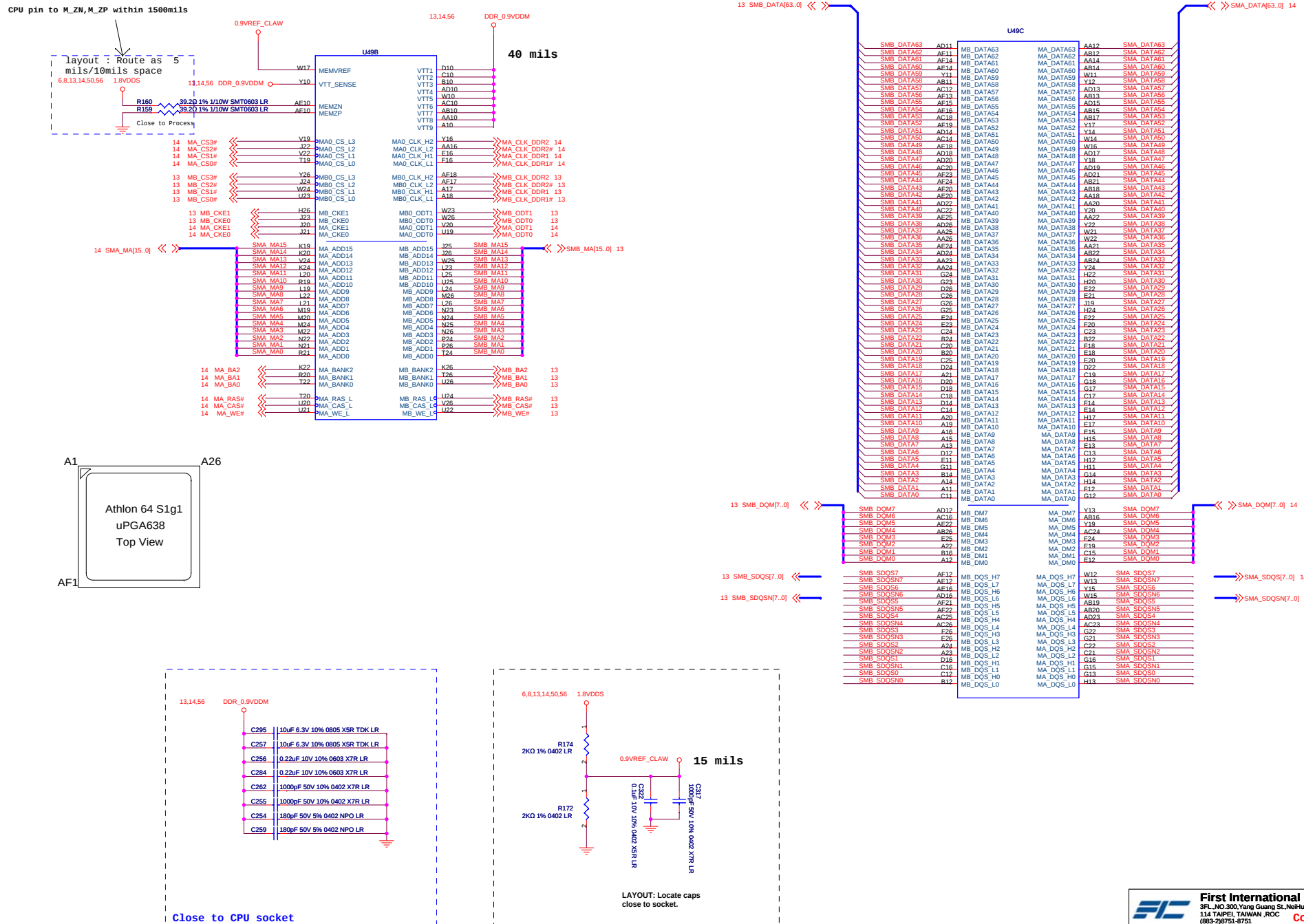
Routing 80 ohm differential impedance

Trace less than 0.5" from process

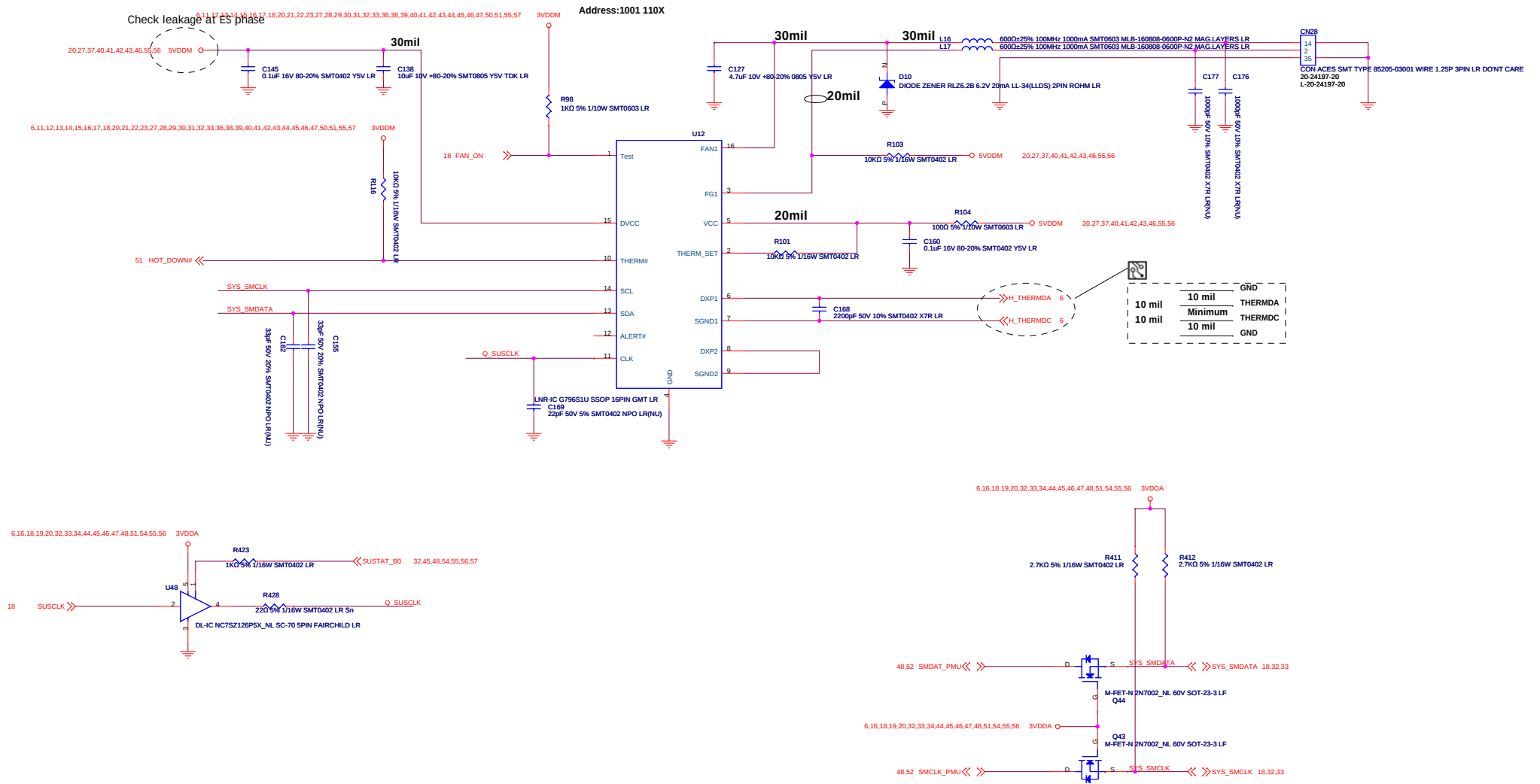
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(886-2)8751-8751

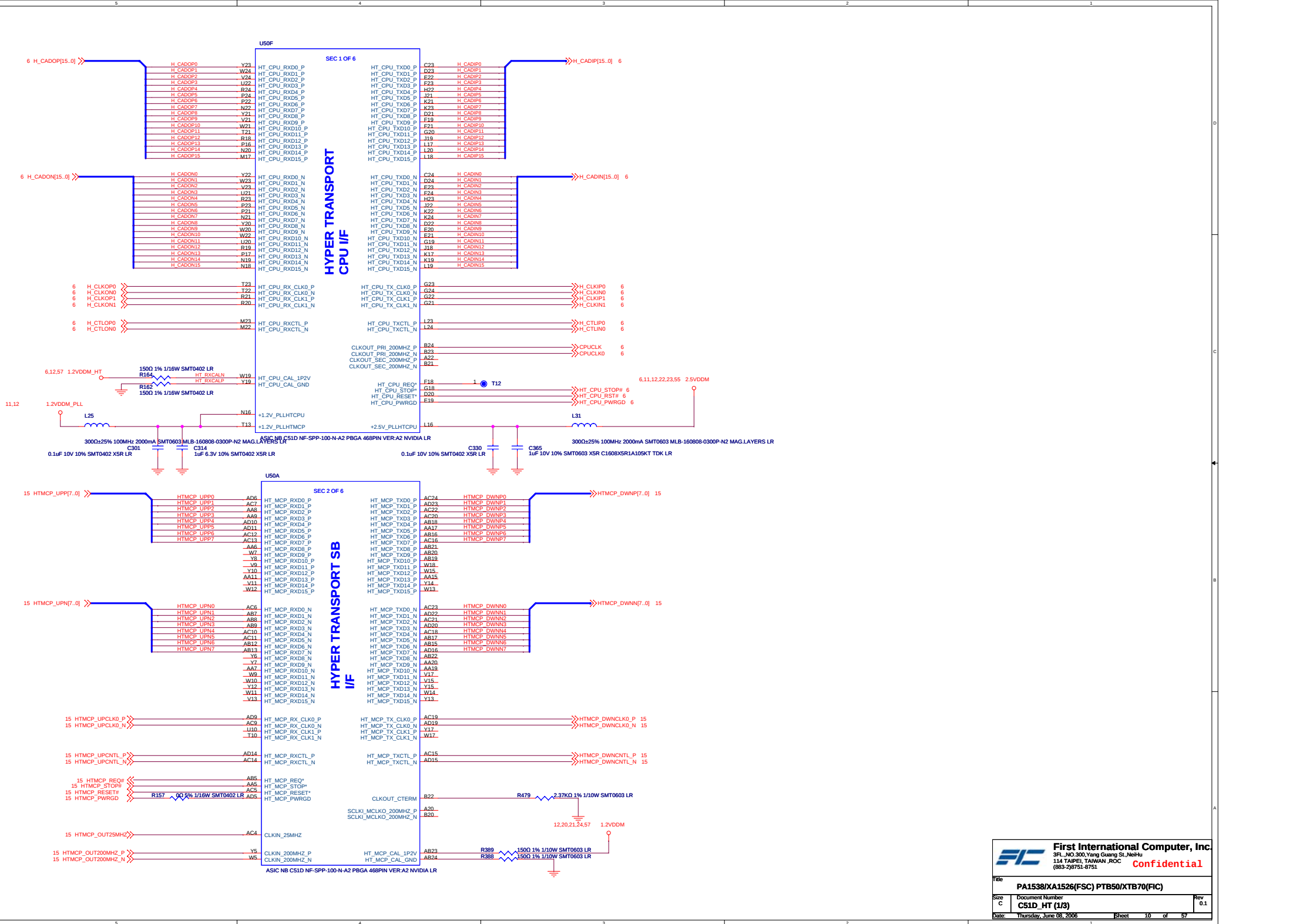
File: PA1538/XA1526(FSC) PTB50/XTB70(FIC)
Size: C Document Number: AMD S1 HT(1/3)
Date: Thursday, June 08, 2006 Sheet: 6 of 57

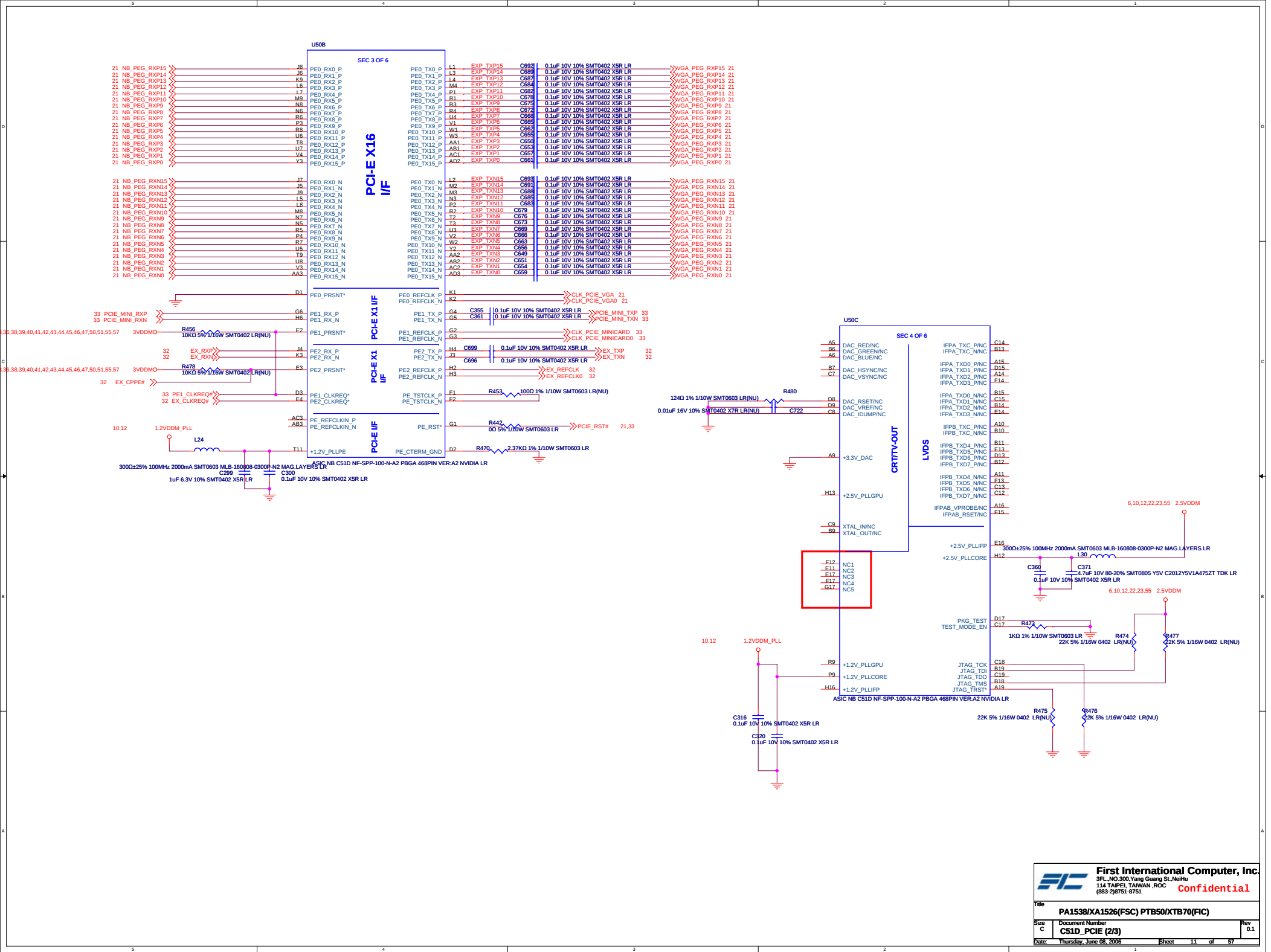
Clawhammer DDR Interface

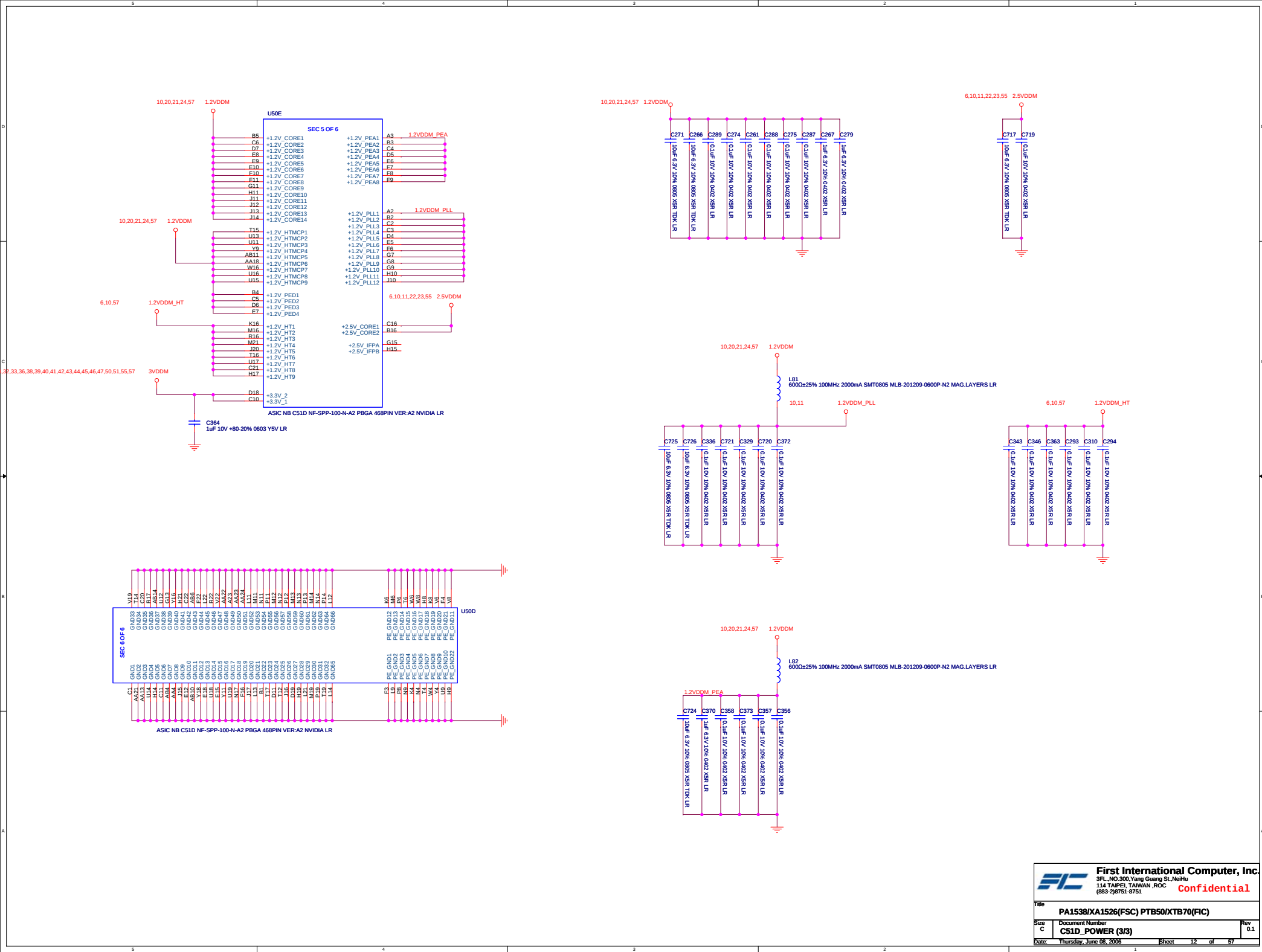


THERMAL SENSOR

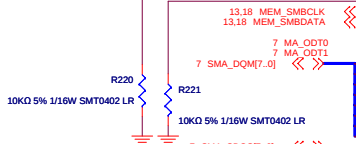
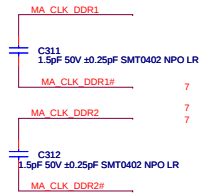








PLACE CLOSE TO CPU
WITHIN 1.5 INCH



6.7,8,13,50,56 1.8VDD5



6.9,11,12,13,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,46,47,50,51,55,57

13 DDR_D_VREF



0.1uF 10V 10% SMT0402 X5R LR

2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

3VDDM

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

7 MA_CS2#

7 MA_CS3#

LAYOUT GUIDE

Other signal	20mil	20mil
DDR_VREF	20mil	20mil
Other signal	20mil	20mil

SO DIMM 1

REV TYPE

SCKT FOXCONN SMT DDR2 SO-DIMM H=5.2 REV AS0A421-N28N-4F LR

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

7 SMA_DATA[63:0]

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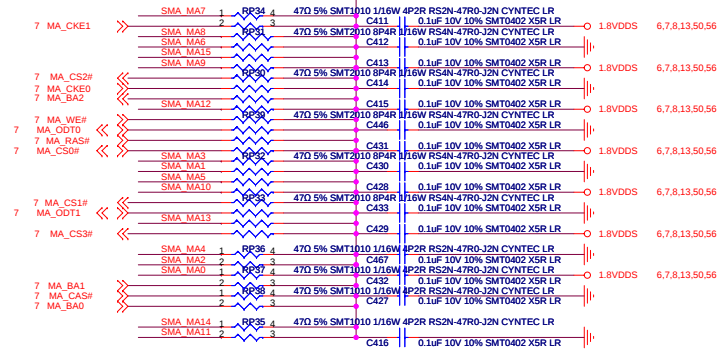
7 SMA_DATA[63:0]

LAYOUT GUIDE

Place one cap close to every 2 pullup resistors terminated to 0.9vddm

400 mils

DDR_0.9VDDM 7.13,56



Place these resistors near So-Dimm1

6.7,8,13,50,56 1.8VDD5

120mil

2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

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2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

2.2uF 10V ±10% SMT0805 X5R C2012X5R1A225KT TDK LR

Place these Hi-Freq decoupling caps near GMCH

Place these 0.1uF caps near So-Dimm1

Place these 2.2uF caps near So-Dimm1

SO-DIMM 1 is placed farther from the GMCH than SO-DIMM 0

6.7,8,13,50,56 1.8VDD5

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

0.01uF 10V 10% SMT0402 X5R LR

Place these 0.01uF caps around VDDIO plane

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File: PA1538/XA1526(FSC) PTB50/XTB70(FIC)

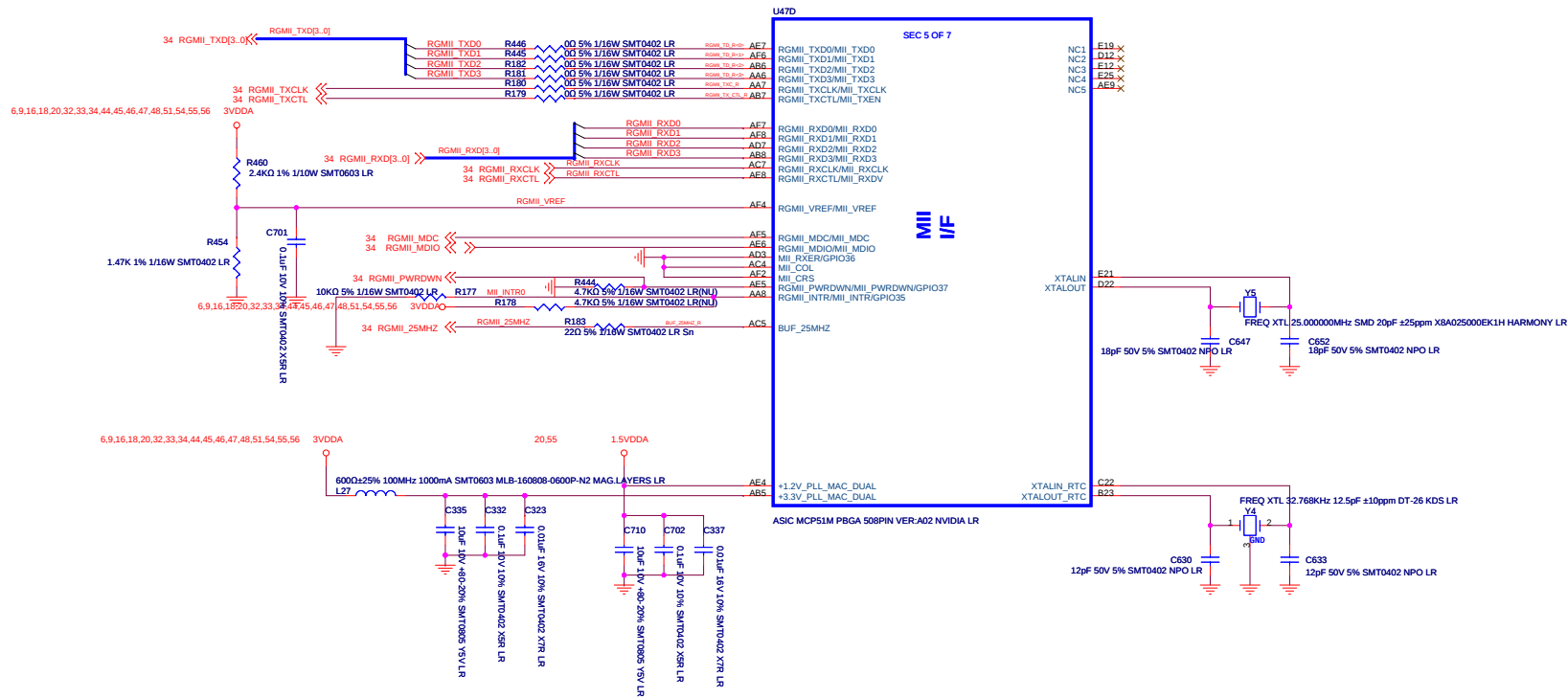
Doc: Document Number

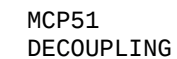
Rev: 0.1

Date: Thursday, June 08, 2006

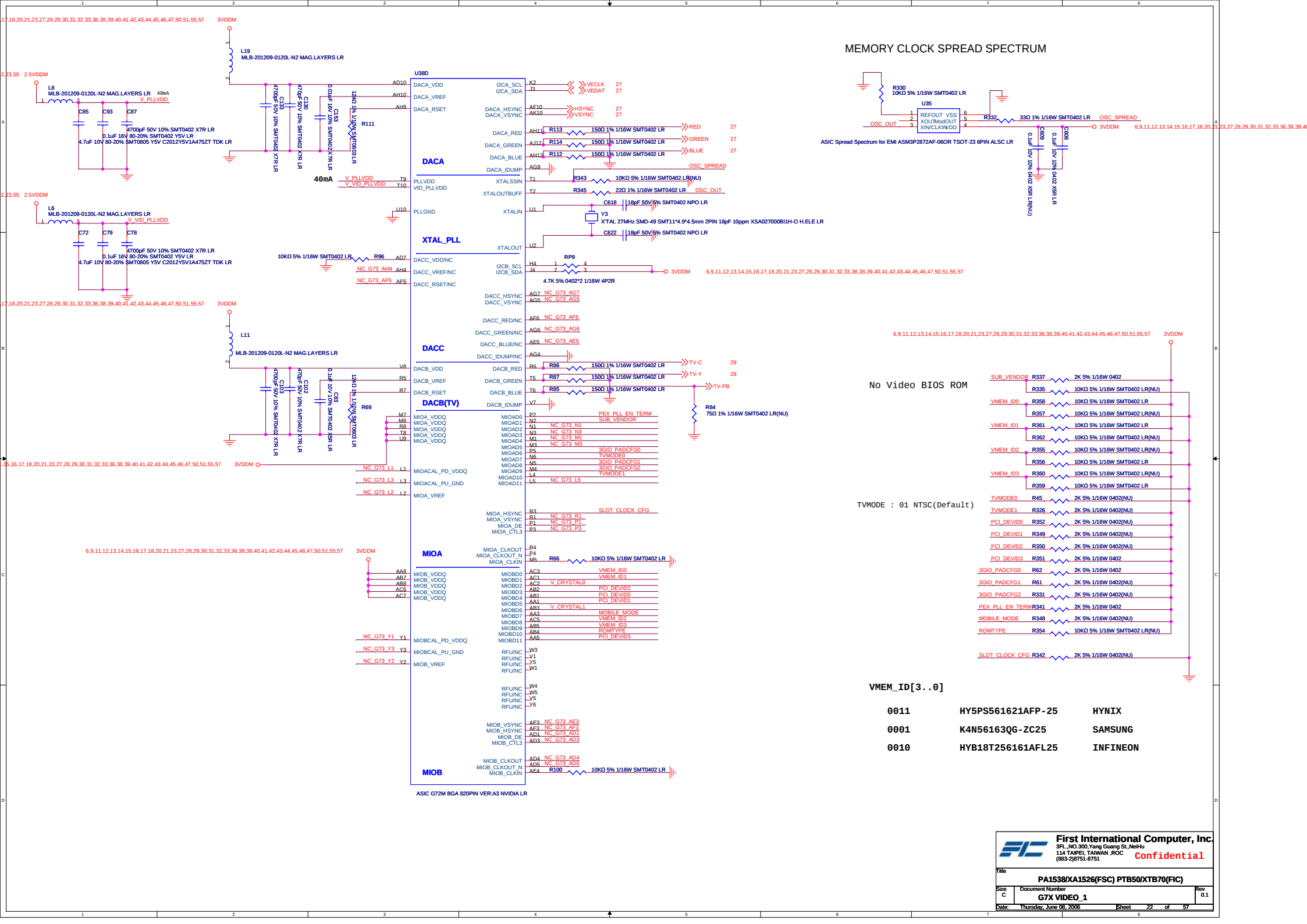
Sheet: 14 of 57



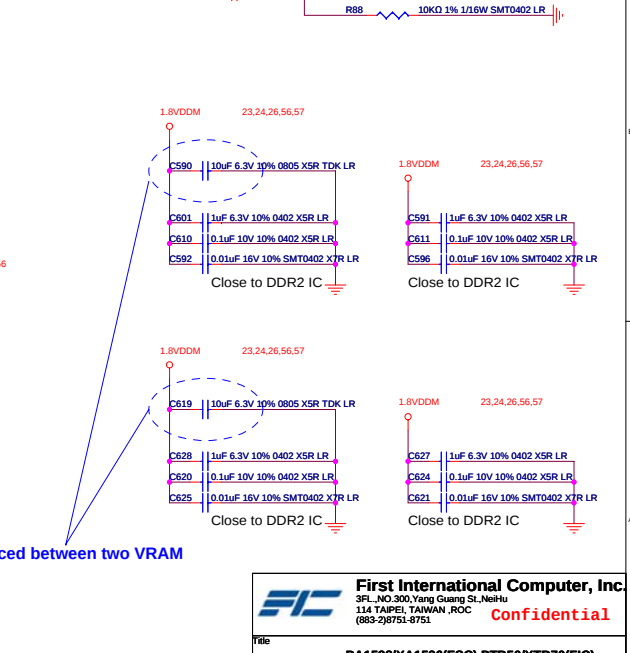
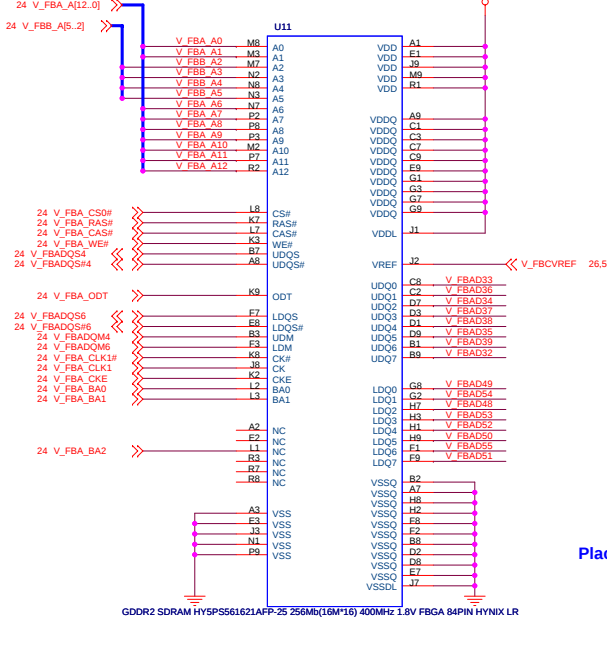
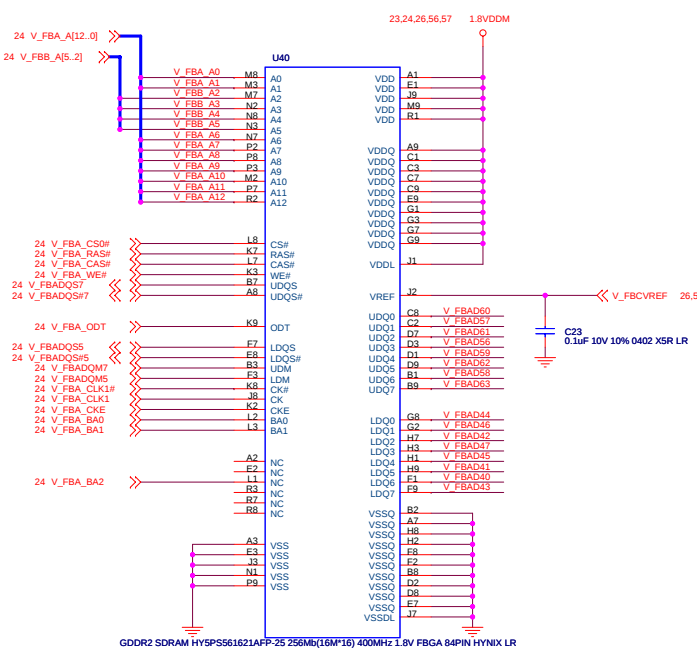
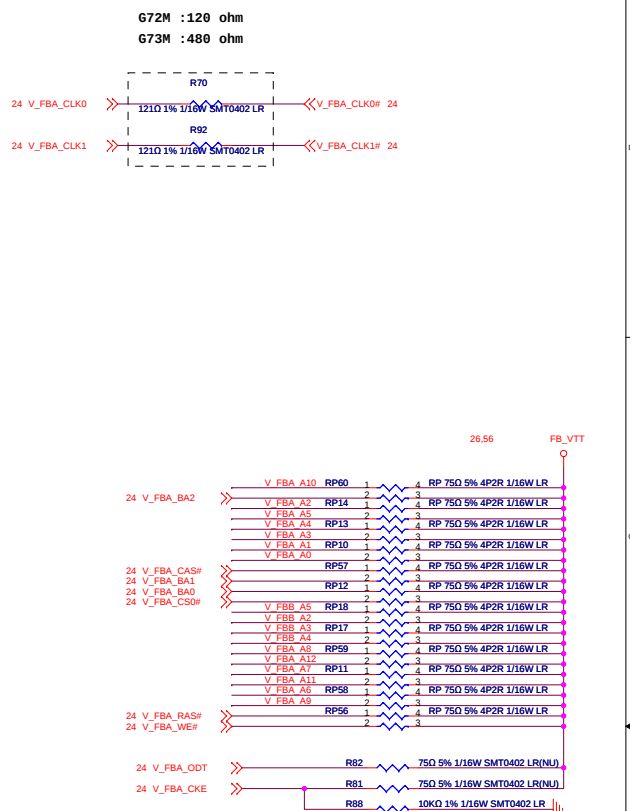
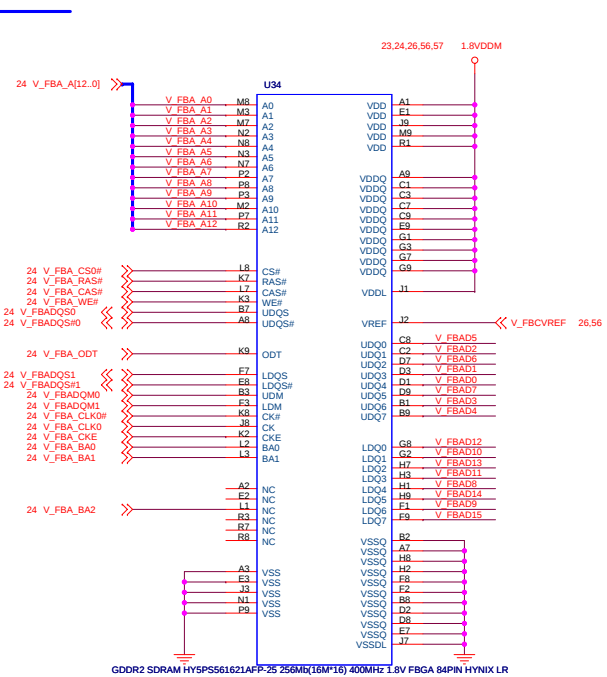
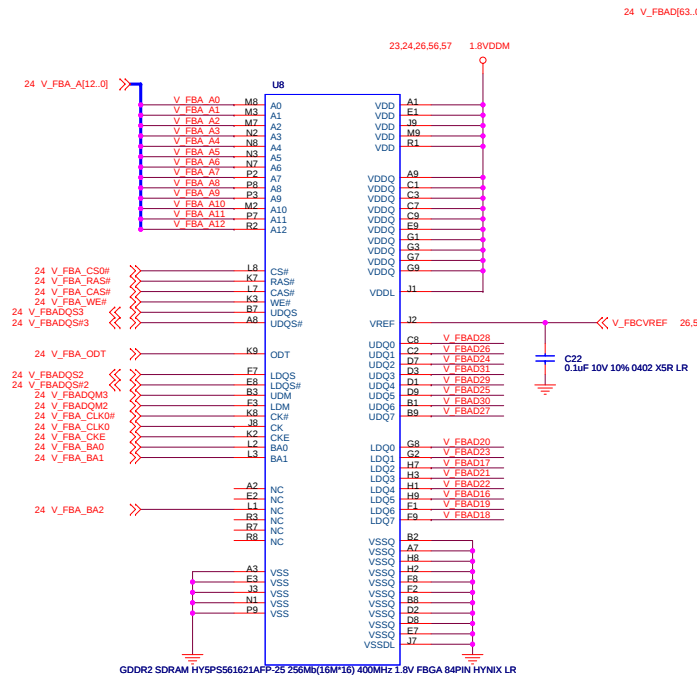










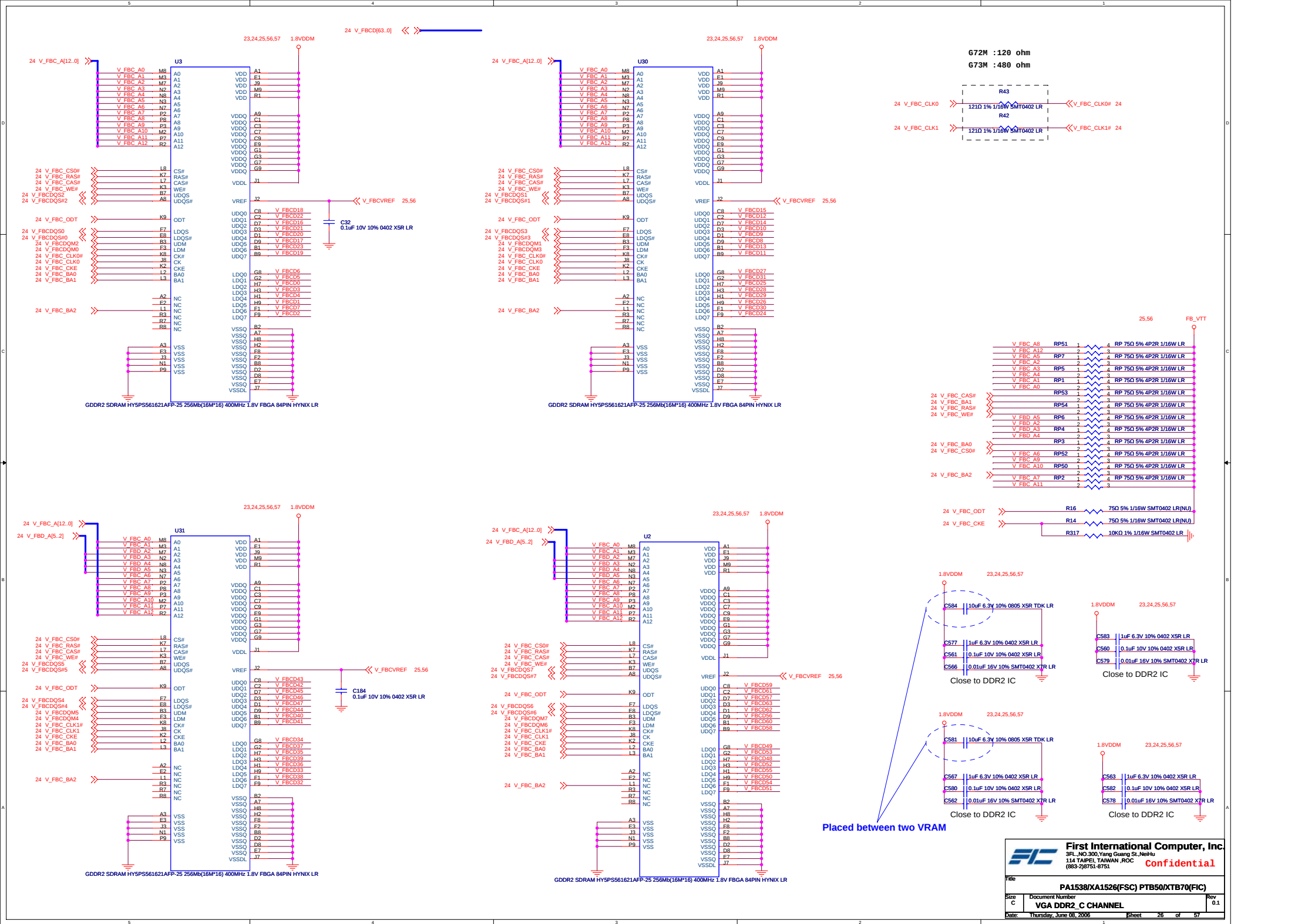


Placed between two VRAM

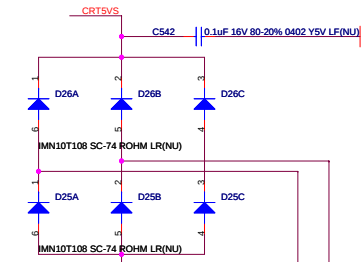
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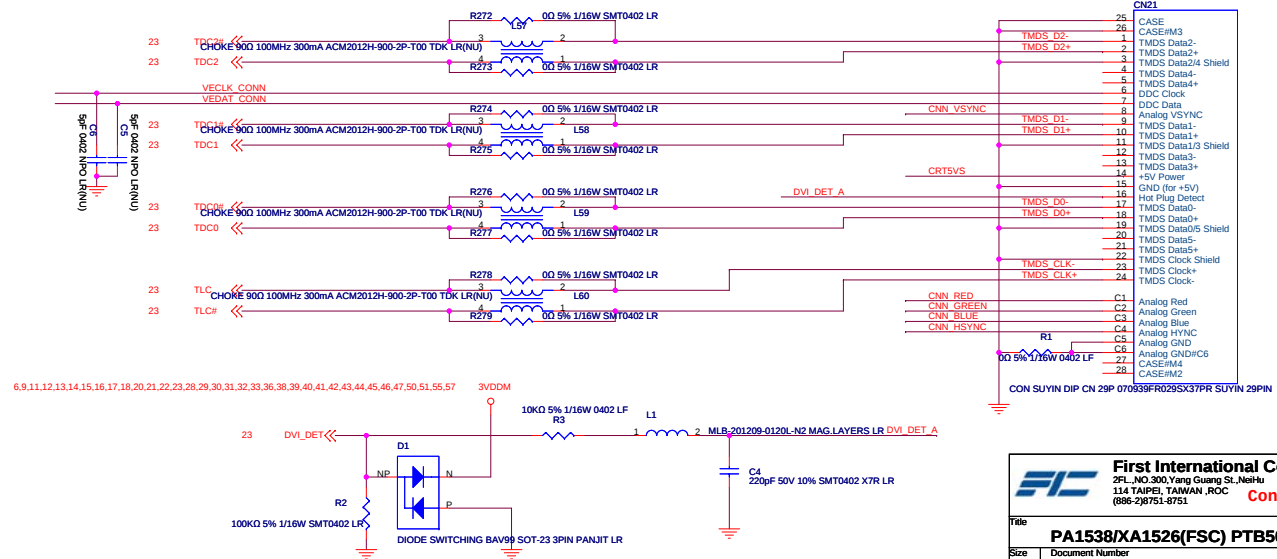
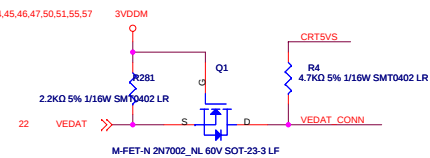
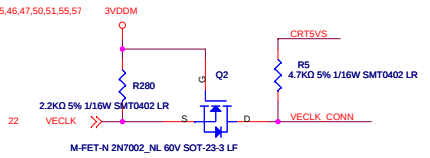
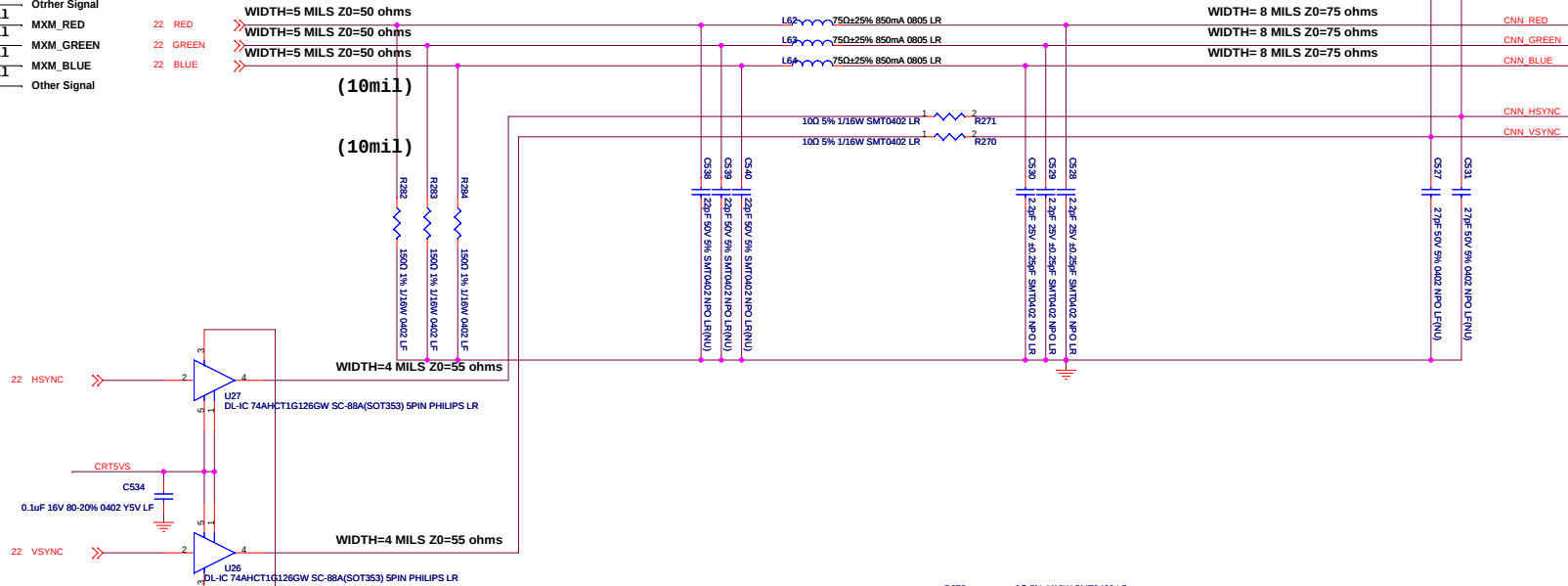
File: PA1538/XA1528(FSC) PTB50/XTB70(FIC)
 Size C Document Number
 VGA DDR2_A CHANNEL
 Date: Thursday, June 08, 2006 Sheet 25 of 57



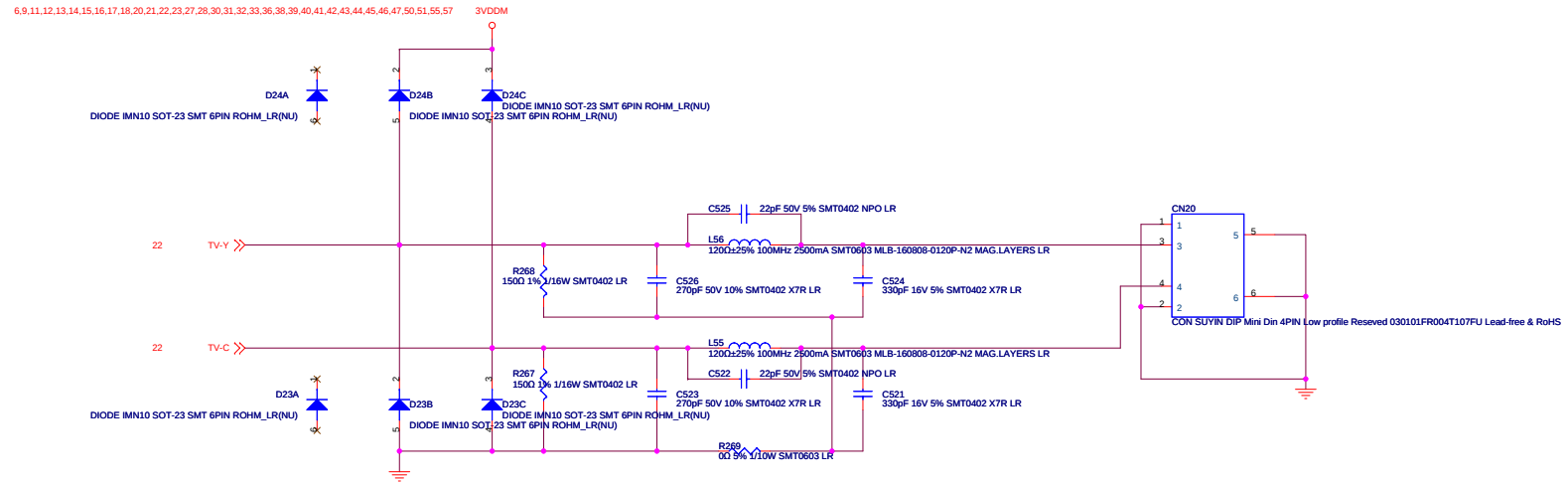
USE 47 ohms@100MHZ
BLM18BB470SN1 (MURATA)



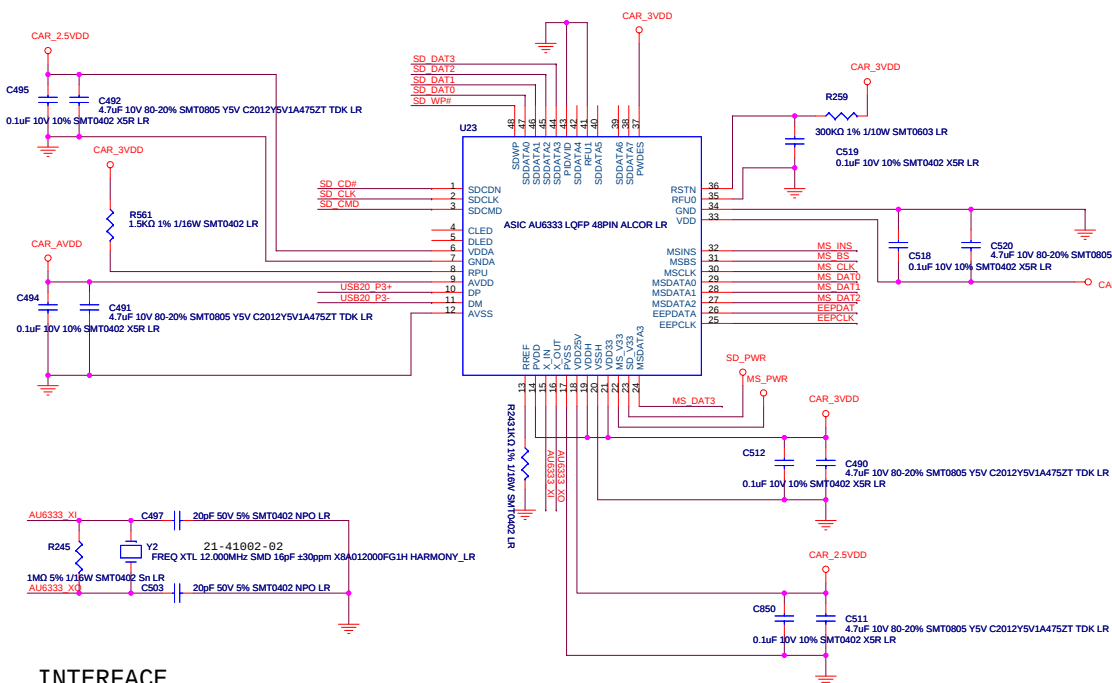
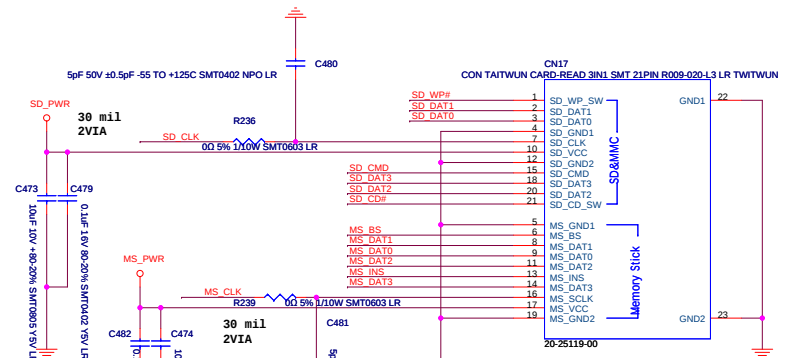
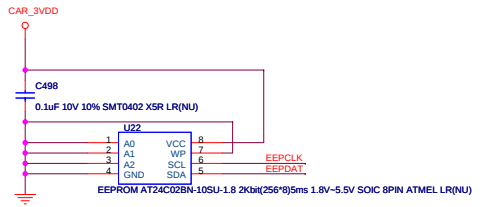
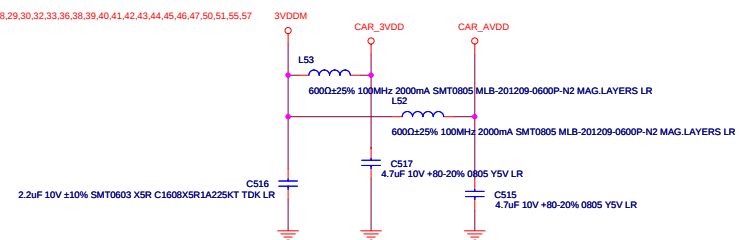
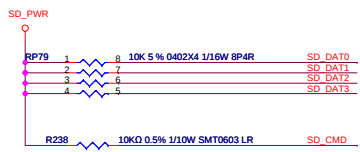
20 mil	Other Signal
20 mil	MXM_RED
20 mil	MXM_GREEN
20 mil	MXM_BLUE
20 mil	Other Signal



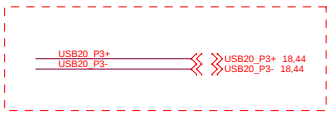
TV OUT CIRCUIT







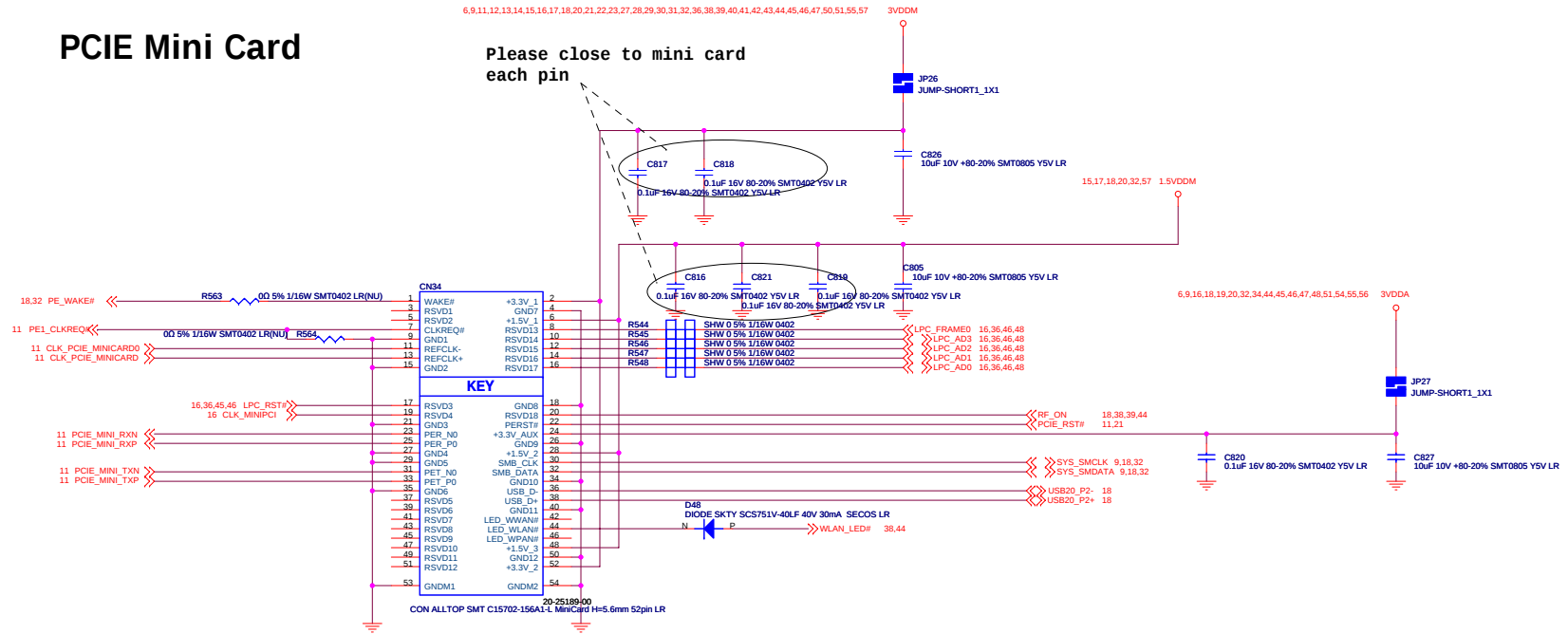
INTERFACE

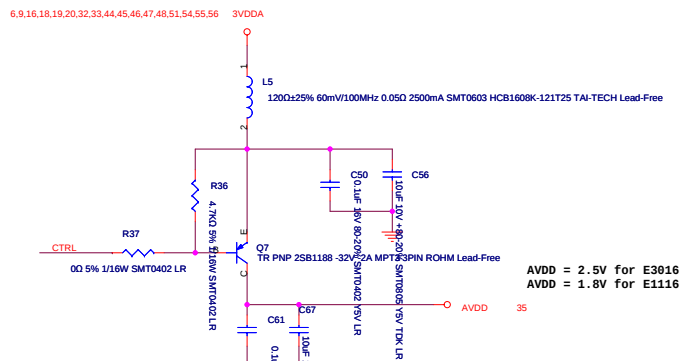
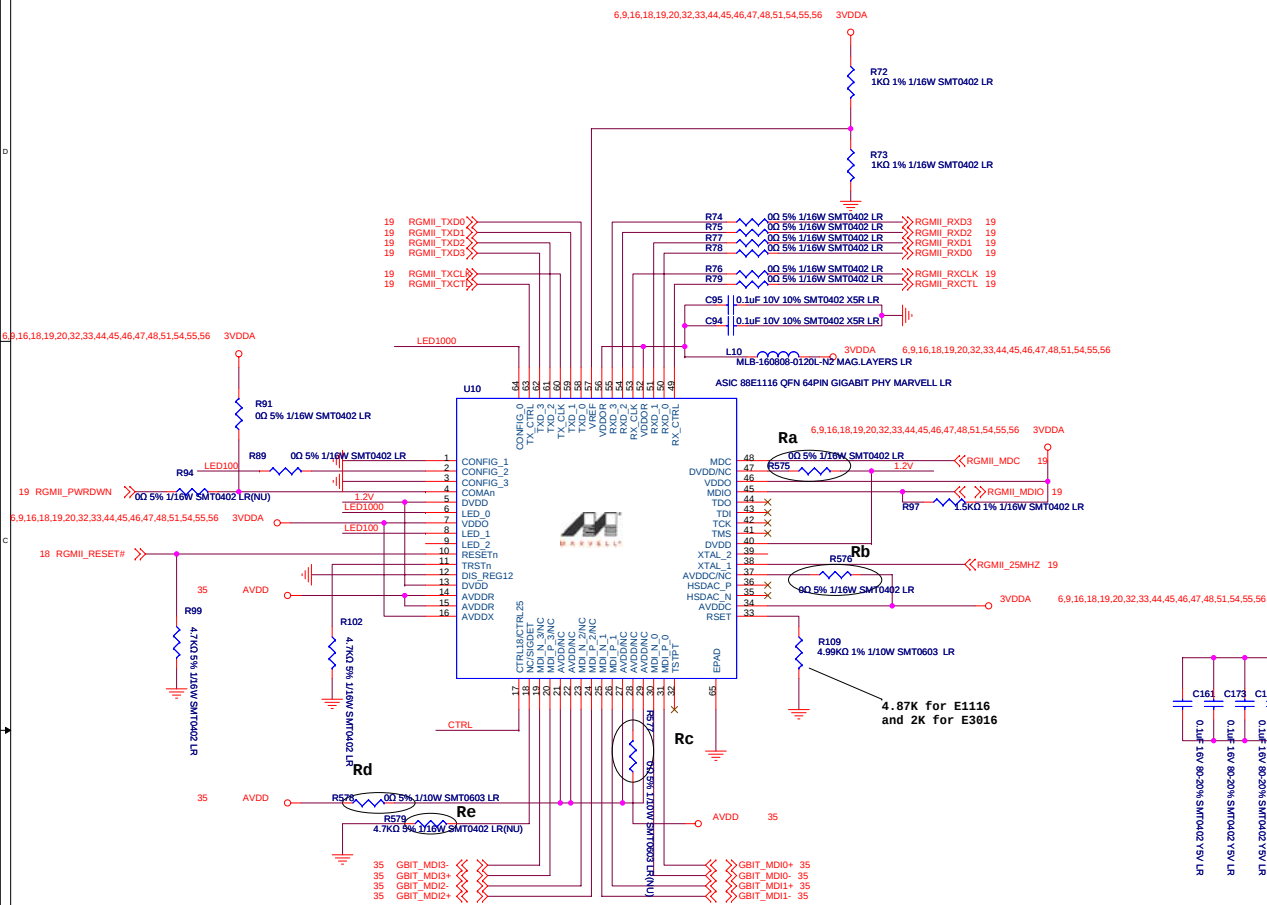




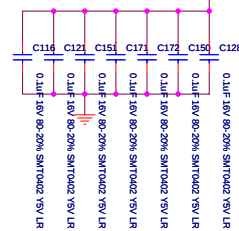
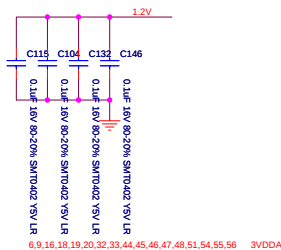
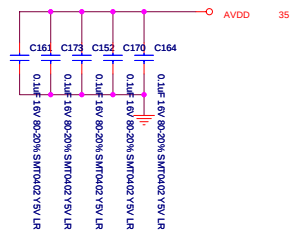
PCIE Mini Card

Please close to mini card
each pin





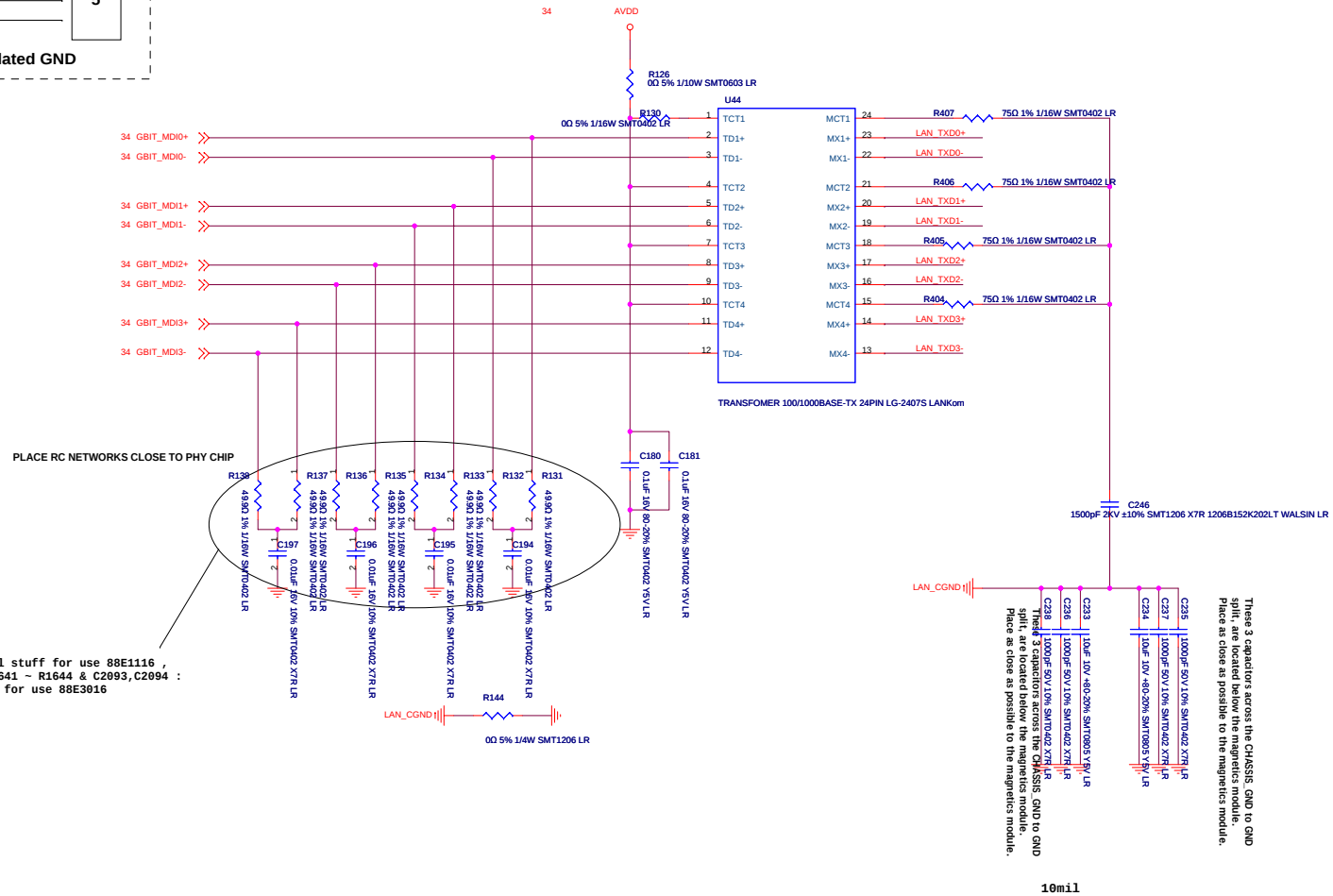
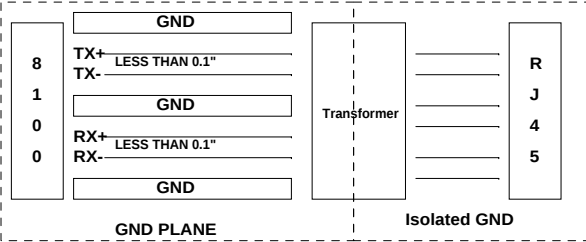
AVDD = 2.5V for E3016
AVDD = 1.8V for E1116



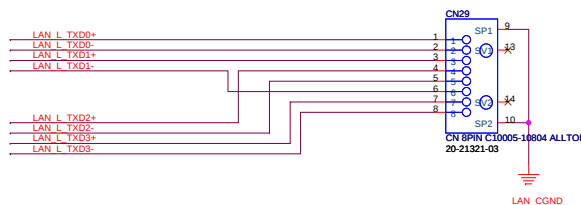
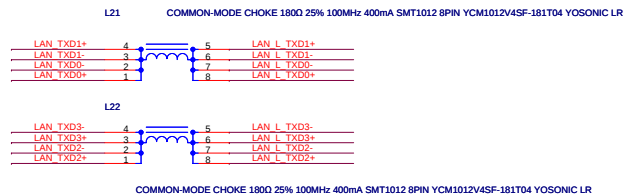
Layout Guide

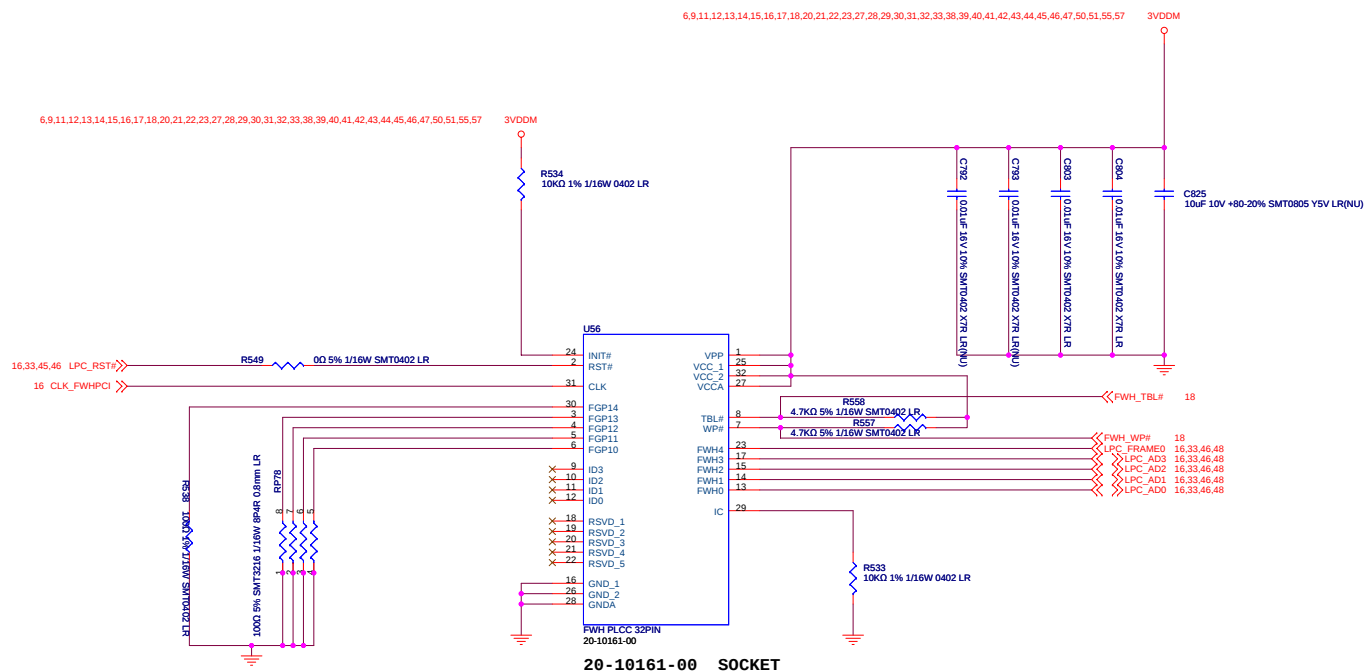
- The Lan Chip should be placed as close as possible to the transfer.
- The resistor connected to RSET pin should be placed near to the Lan Chip, and away from signal traces(ex:MDIO+/-) and clock signals as far as possible.
- The transfer should be placed as close as possible to the RJ45 connector.
- The crystal should be placed far away from I/O ports and high frequency signal.
- The termination resistors and capacitors should be placed closely to the Lan Chip.
- The decoupling capacitors should be placed as close as possible to the power pins, such that the distance from IC power pin to the capacitor is within 200mils.
- Traces routed from the Lan Chip to the transfer, and to the RJ45 connector should be as short as possible.
- The 10-12cm maximum length between Lan Chip and transfer is achievable only when there's no interferences around.
- All 4 pairs of the differential resistor(49.9K) must close to Lan Chip, and make them(4pairs) as same as distant.
- PLACE GND PLANE AS LARGE AS POSSIBLE
- If power pins are next to each other and there is not much room to accommodate multiple capacitors, then the power pins can share the same capacitors.
- It's important to separate digital signals from analog signals. If it is unavoidable to cross digital signals with analog power do it at 90 degree angle.
- The digital power plane should be separated from analog areas.
- All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
- The Lan Chip pin 1 facing the transformer, then you can make the signal shorter.

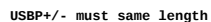
TX 100 ohm ---> trace 4 mil , space 10 mil
RX 50 mil space from other signals
Total Trace Length no more thans 4.8"
2 Differential pairs must have the same length



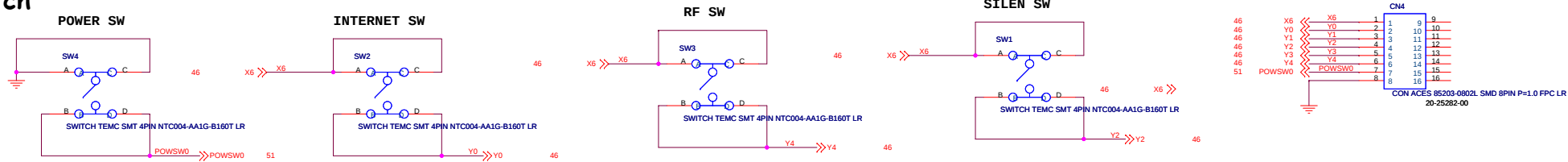
All stuff for use 88E1116 ,
R1641 ~ R1644 & C2093, C2094 :
NU for use 88E3016



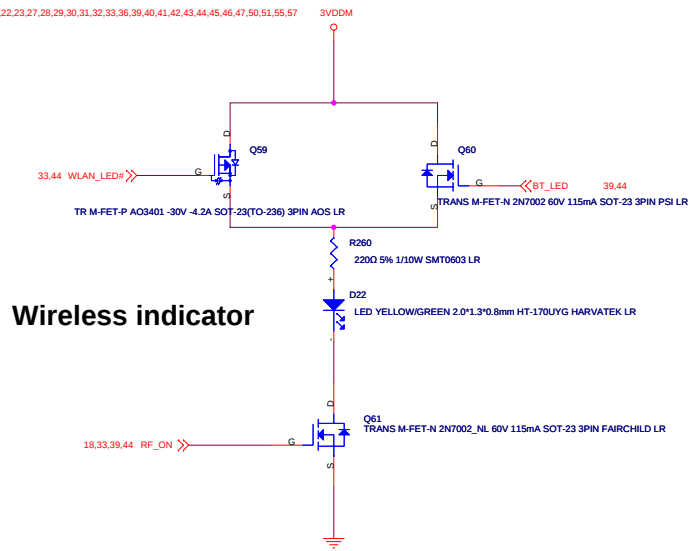




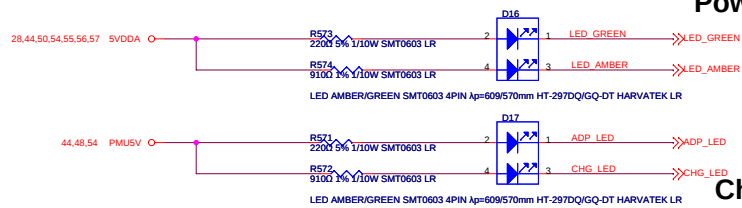
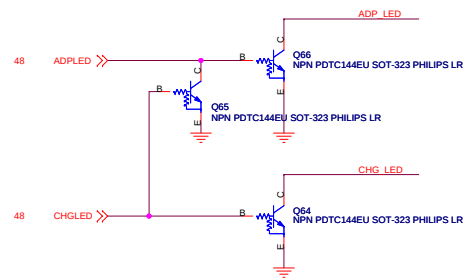
Switch



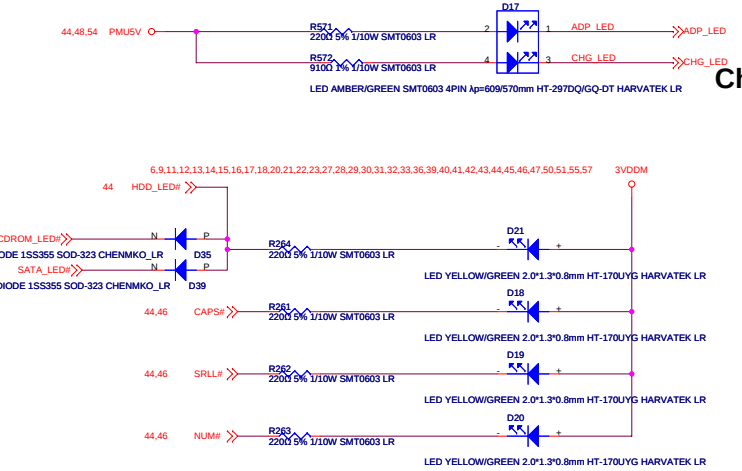
LED indicator control logic



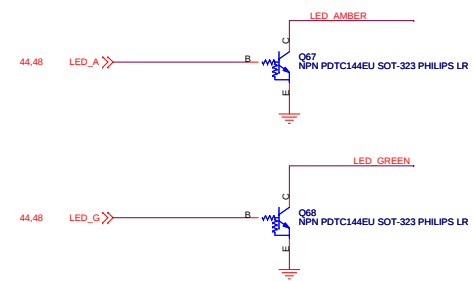
Wireless indicator



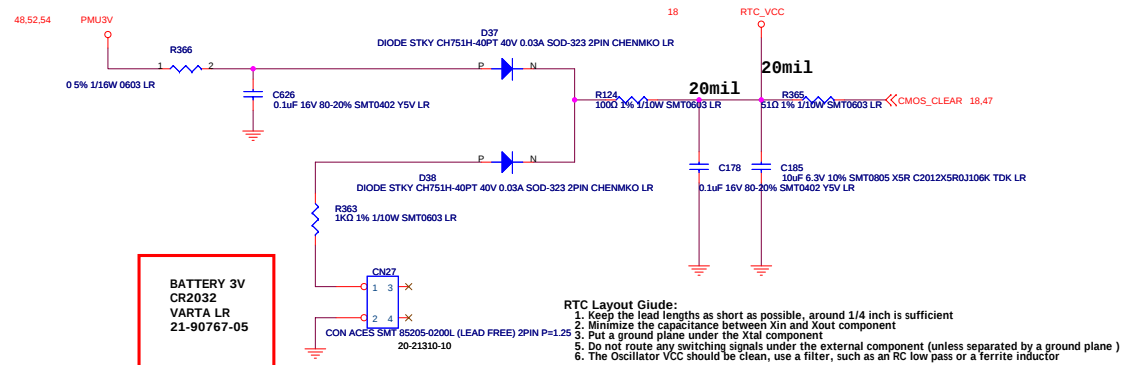
Power indicator



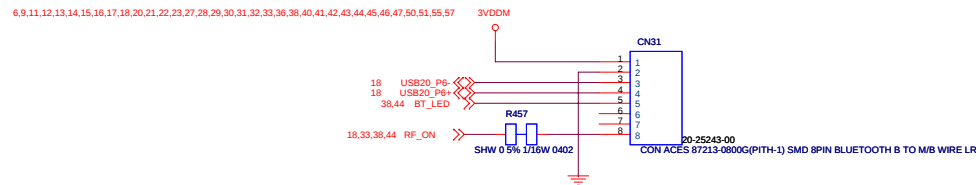
Charge indicator



RTC Discharge Circuit

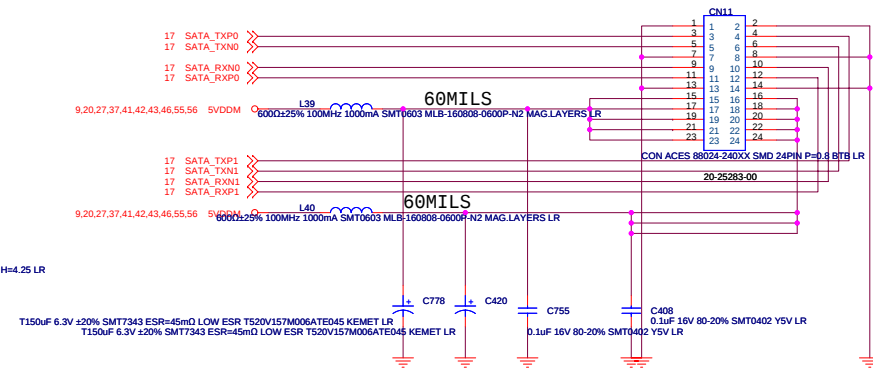
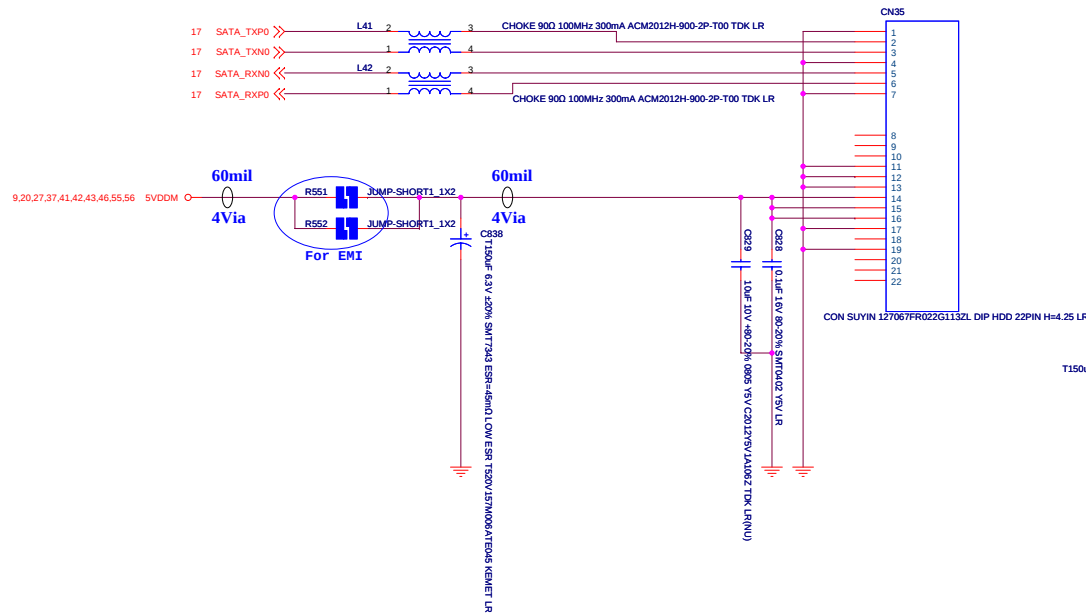


BLUETOOTH



HDD I/F

FOR XTB70



LAYOUT GUIDE **SATA Layout Note:**

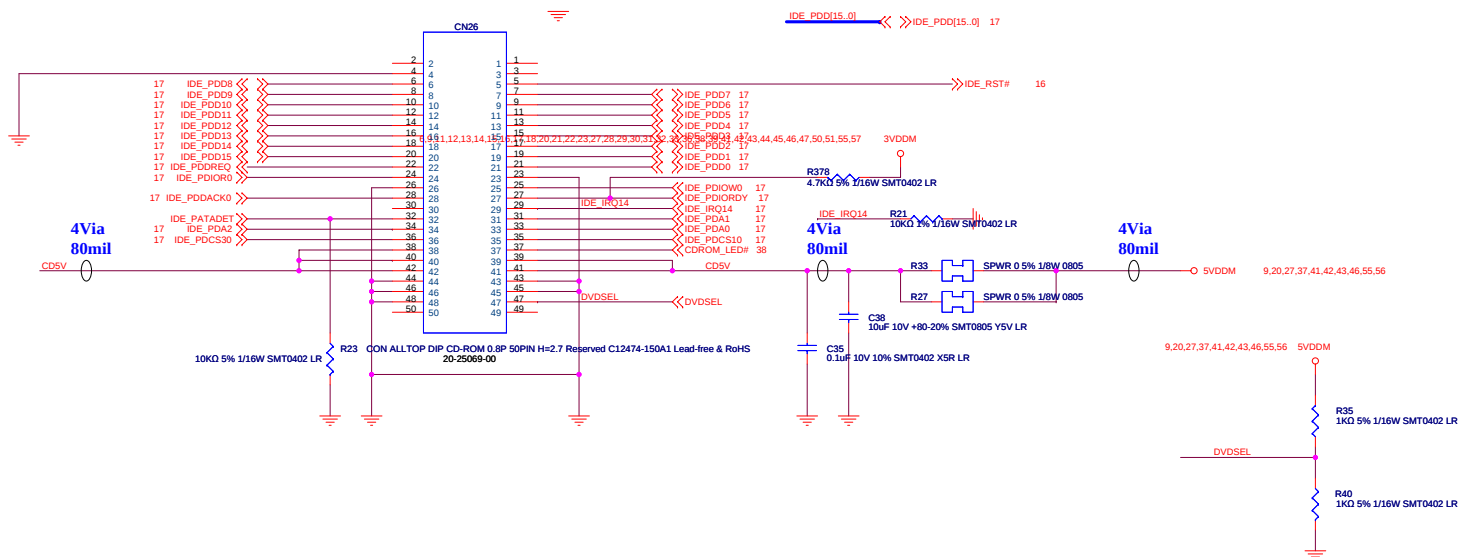
MS or SL: 20mils 5mils 8mils 5mils 20mils

TX RX

5mils 8mils 5mils 20mils

- * Zdif = 100 Ohm +/- 10%. TX & RX should refer GND.No via & stubs.The Best layer is Top.
- * TX/RX trace length < 2 inches.
- * TX+/- need matching trace ± 10 mils length.
- * RX+/- need matching trace ± 10 mils length.
- * SATA Pair to Pair Trace matching trace ± 10 mils length.

CD-ROM CNN

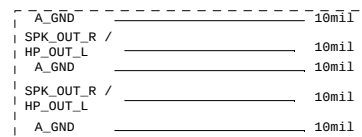
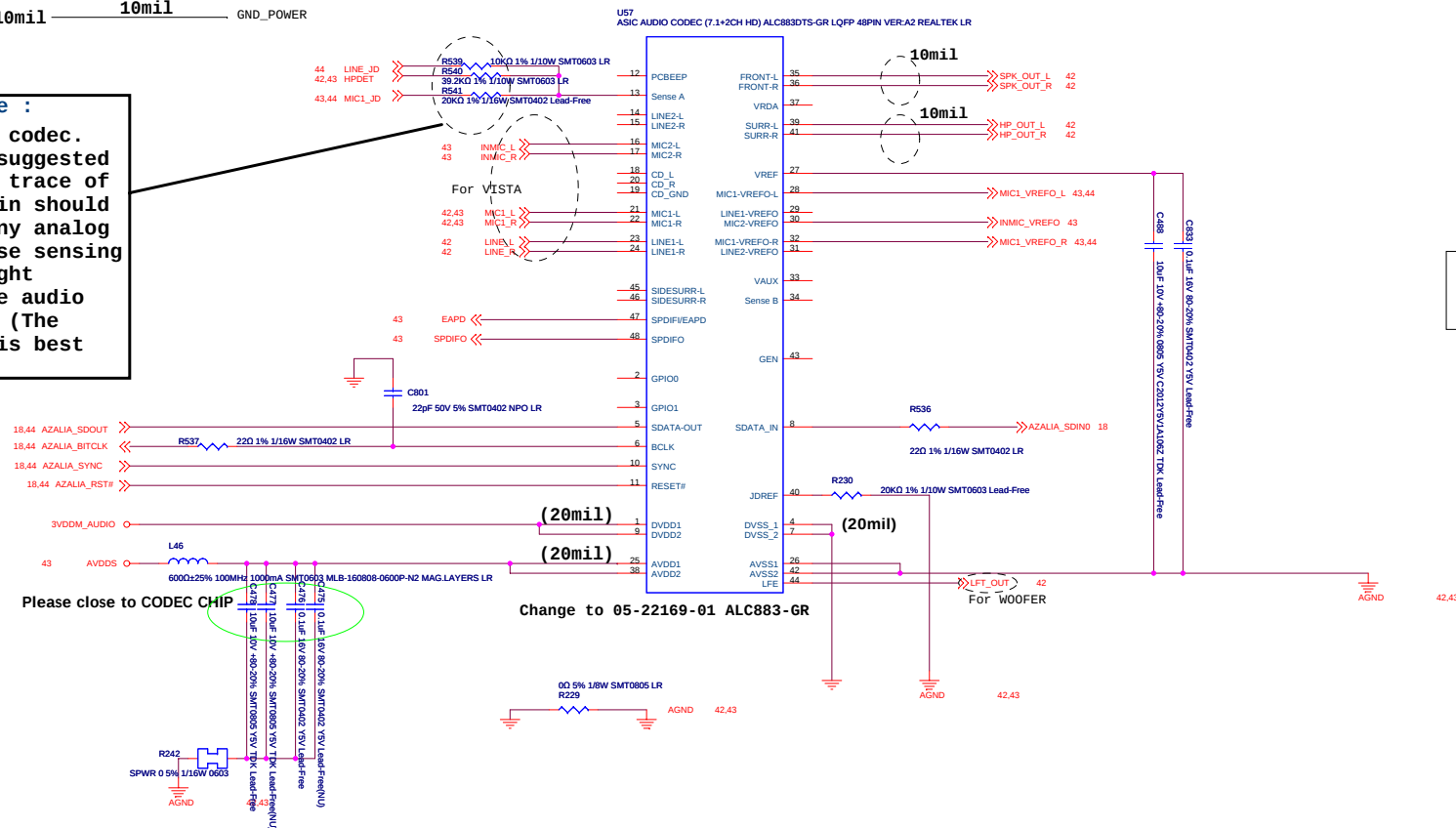


10mil GND_POWER
 10mil 10mil AZALIA_PCBEEP
 10mil 10mil GND_POWER
 10mil 10mil GND_POWER
 10mil 10mil AZALIA_BITCLK
 10mil 10mil GND_POWER

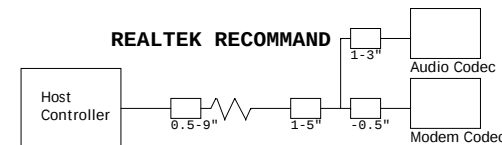
AC97/AZALIA CODEC DUAL LAYOUT AC97 USE AL883 DTS / AZALIA(RESERVE)

Layout guide :

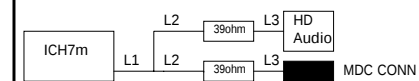
1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away from any analog trace because sensing current might distort the audio performance (The bottom lay is best choice).



REALTEK RECOMMEND



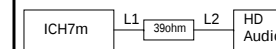
HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#



Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"-2.5" L2 <= 0.1" L3 = 1"-8"

*** L3 can be extended up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN



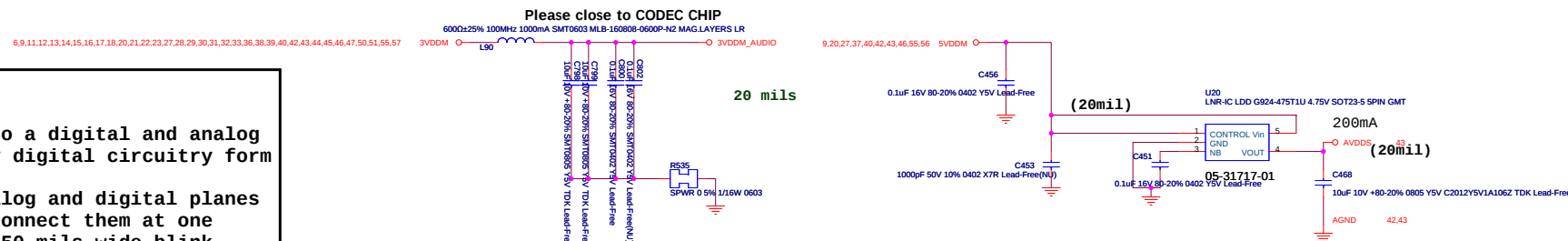
Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"-15" L2 <= 0.5"

*** Breakout can be routed 4 on 4 up to 500 mils

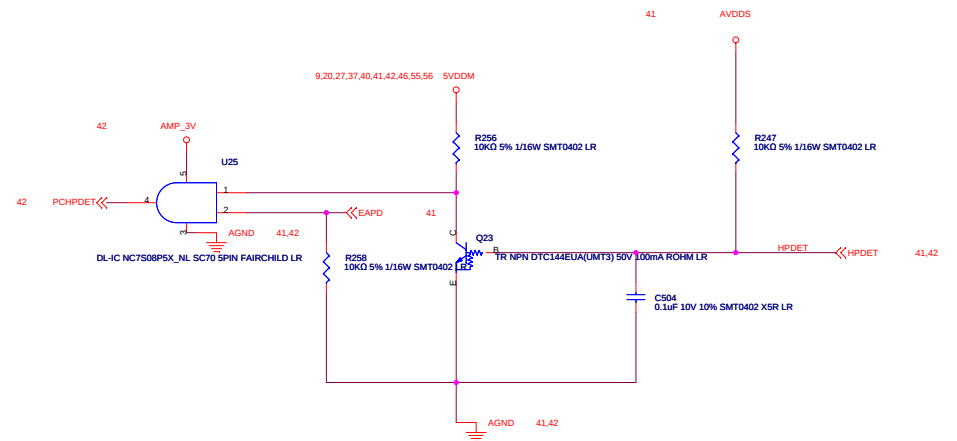
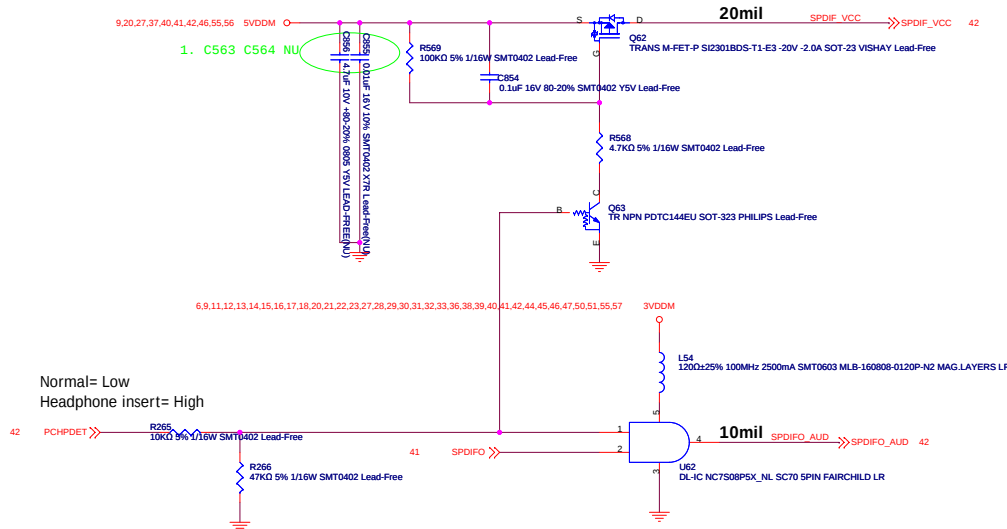
AC'97 CODEC & CD POWER

Layout guide :

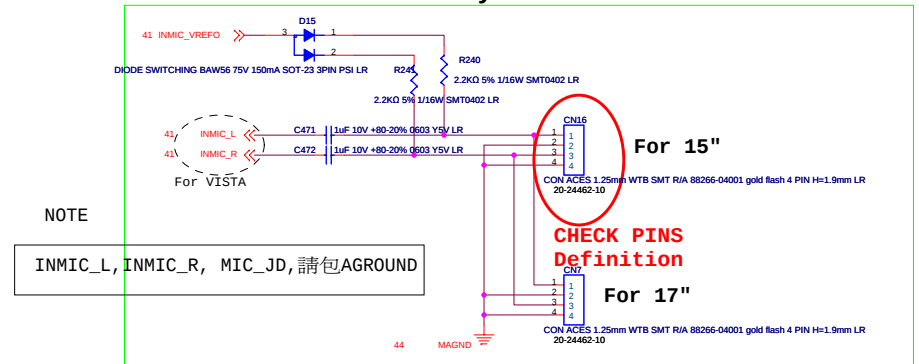
1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry from quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.



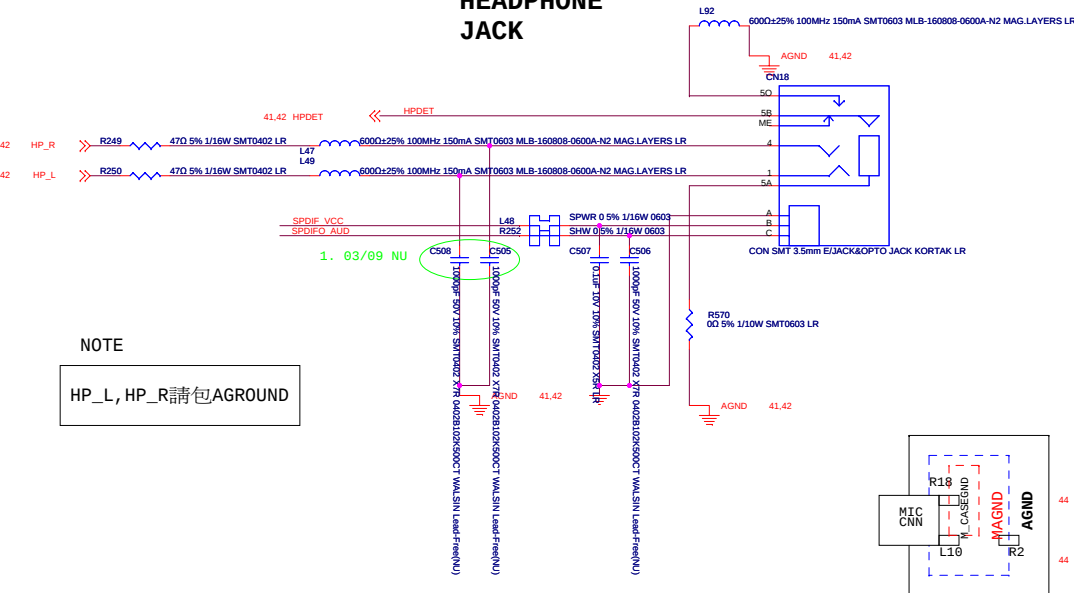
S/PDIF Power



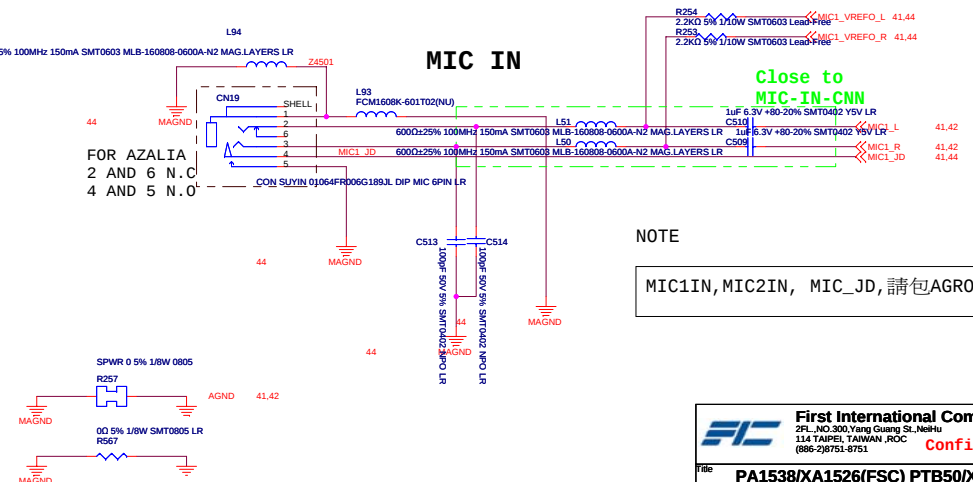
Internal array MIC



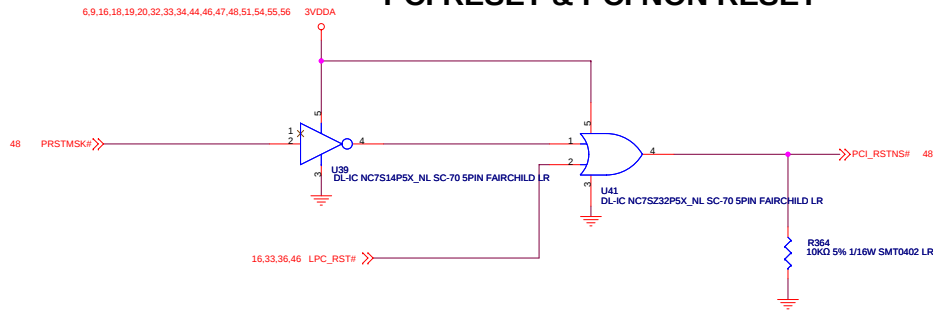
SPDIF & HEADPHONE JACK



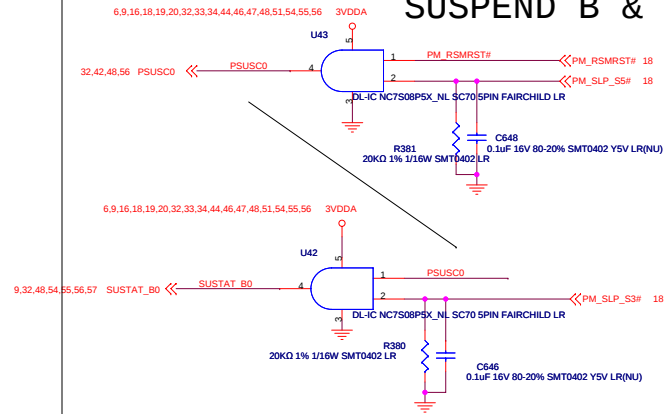
MIC IN



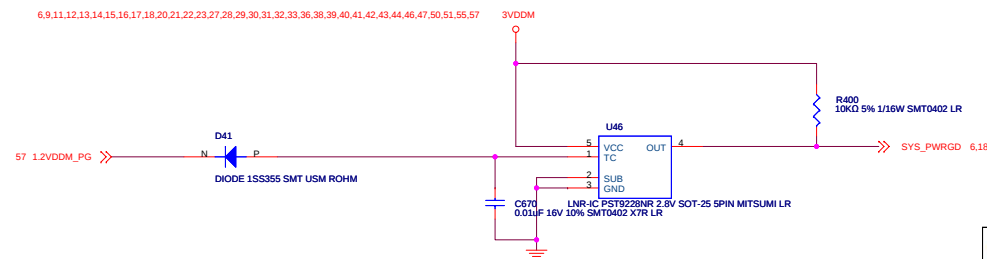
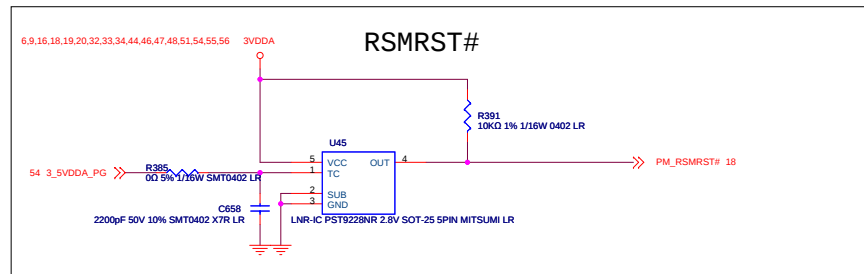
PCI RESET & PCI NON RESET



SUSPEND B & C



RESUME RESET



Trace:5mil, Spacing:5mil

600G±25% 100MHz 1000mA SMT0603 MLB-160808-0600P-N2 MAG.LAYERS LR

6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57

3VDDM

L78

C590

470pF 50V 10% 0402 XTR Lead-Free

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Y[7..0]

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6.9,16,18,19,20,32,33,34,44,45,47,48,51,54,55,56

3VDDA

R206

4.7KΩ 5% 1/16W SMT0402 LR

Q16

TRANS M-FET-N 2N7002_NL 60V 115mA SOT-23 3PIN FAIRCHILD LR

KBC_SMI#

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Q_SMI#

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6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57

3VDDM

RP74

10K 5% 0402X2 1/16W 4P2R

R504

00 5% 1/16W SMT0402 LR(NU)

R494

10K 5% 1/16W 0603(NU)

R493

10K 5% 1/16W 0603(NU)

10K 5% 1/16W 0603(NU)

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10K 5% 1/16W 0603(NU)

6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57

3VDDM

L32

600G±25% 100MHz 2000mA SMT0805 MLB-201209-0600P-N2 MAG.LAYERS LR

10K 5% 1/16W 0603(NU)

10K 5% 1/16W 0603(NU)

10K 5% 1/16W 0603(NU)

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10K 5% 1/16W 0603(NU)

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6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57

3VDDM

D13

N

P

D SC355V-LF 100V 500mA SOD-323 SECOS LEAD-FREE

R201

10K 5% 1/16W 0603 Lead-Free

C379

10uF 10V +80-20% SMT0805 Y5V LR

C378

470pF 50V 10% 0402 XTR(NU)

C377

0.1uF 10V +80-20% 0402 Y5V LR

C376

10uF 10V +80-20% SMT0805 Y5V LR

10K 5% 1/16W 0603 Lead-Free

R505

10K 5% 1/16W 0603 Lead-Free

10K 5% 1/16W 0603 Lead-Free

10K 5% 1/16W 0603 Lead-Free

10K 5% 1/16W 0603 Lead-Free

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10K 5% 1/16W 0603 Lead-Free

6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,55,57

3VDDM

RP29

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10K 5% 0402X2 1/16W 4P2R

KBC_CNTR1

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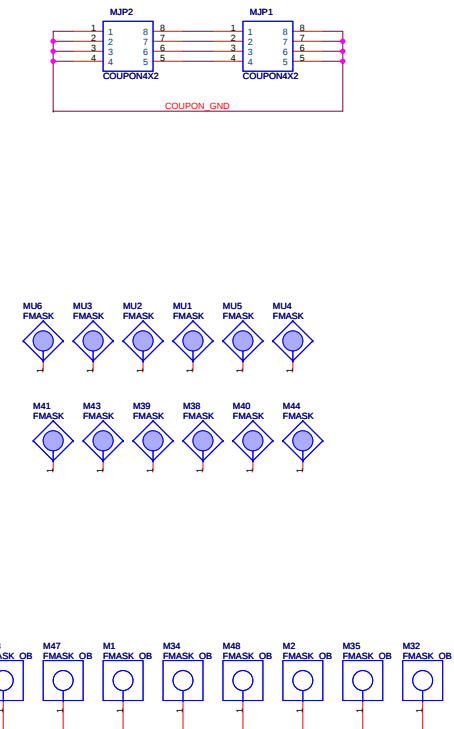
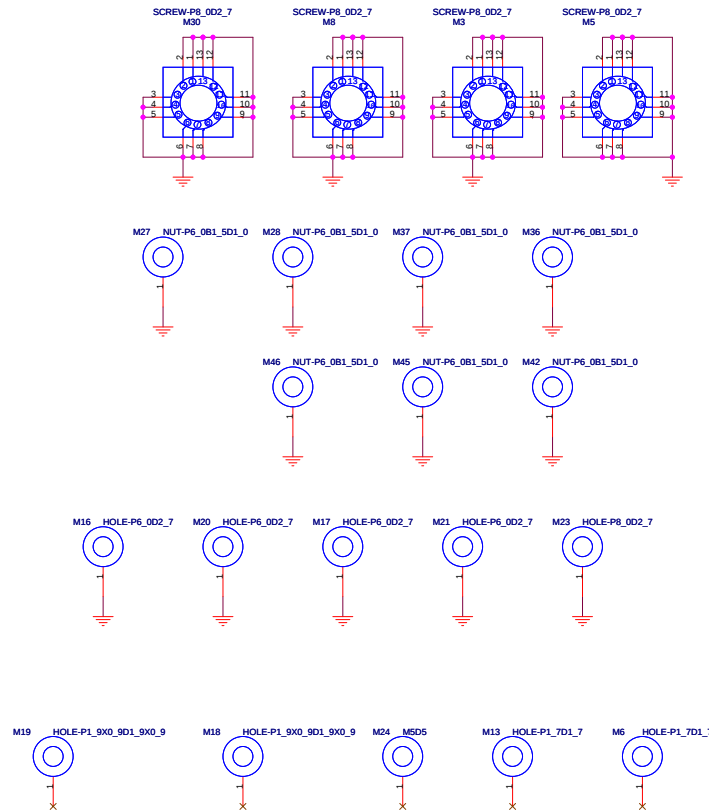
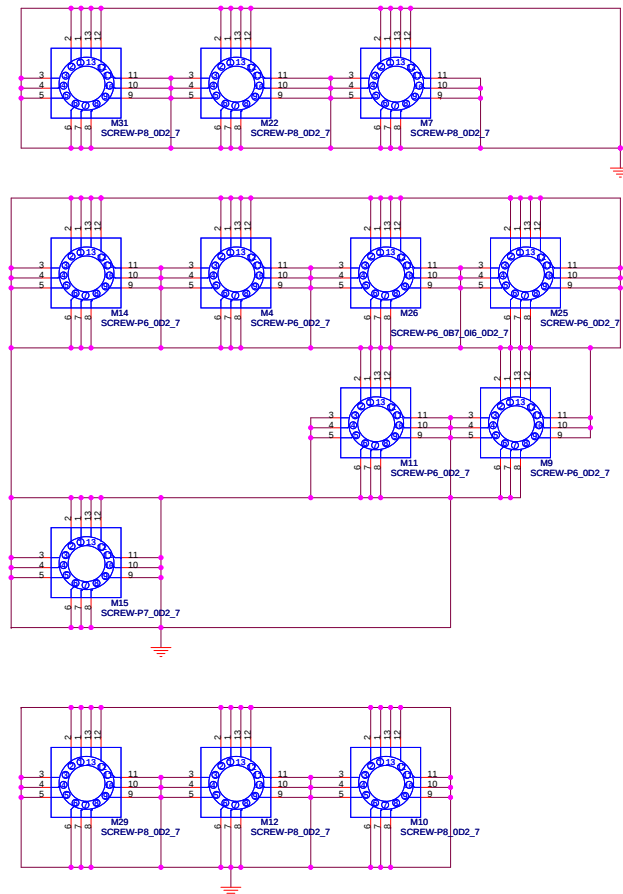
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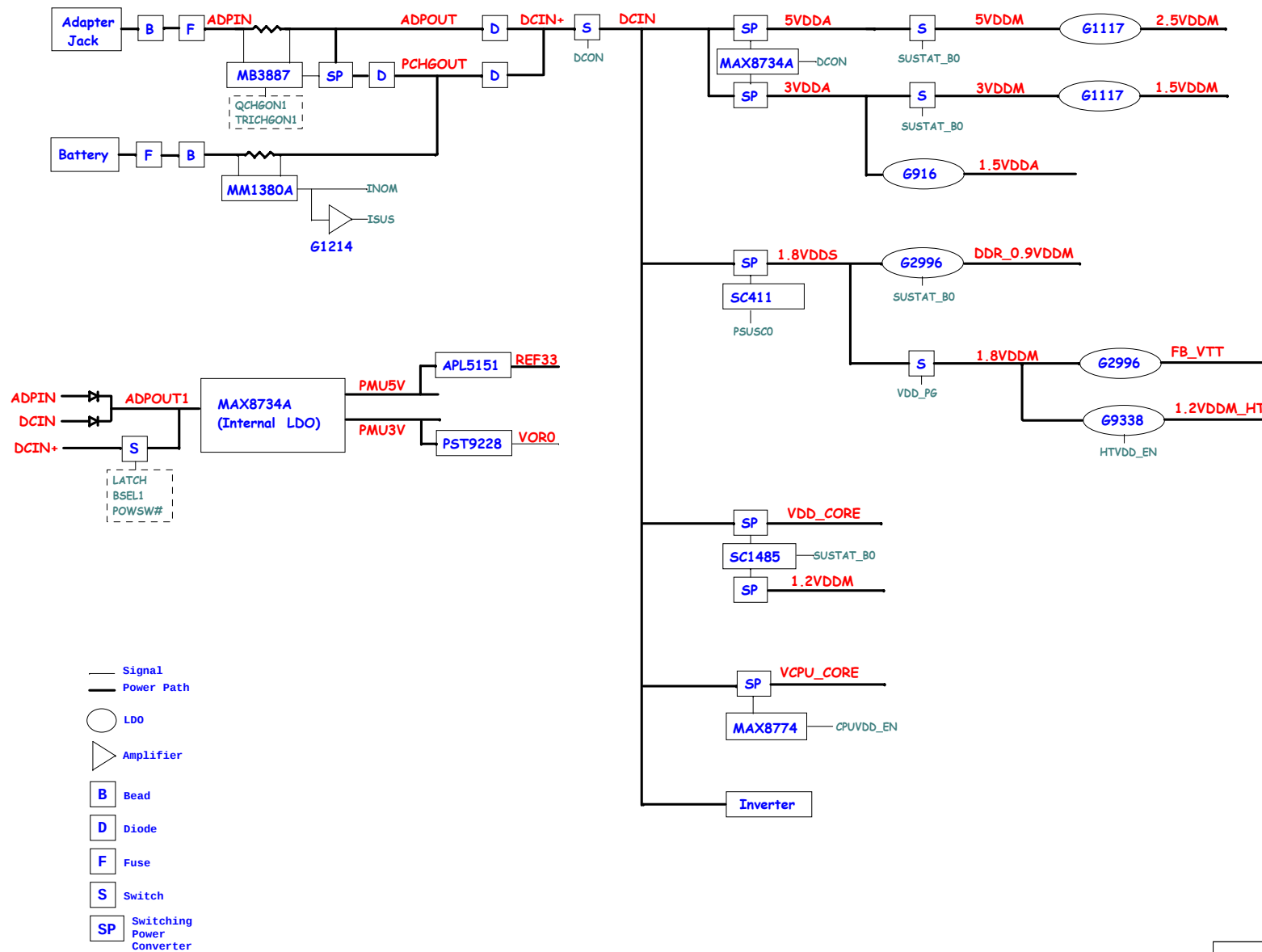
18

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6.9,11,12,13,14,15,16,17,18,20,21,22,23,27,28,29,30,31,32,33,36,38,39,40,41,42,43,44,45,47,50,51,5

[illegible]

PTB50 Power Block Diagram



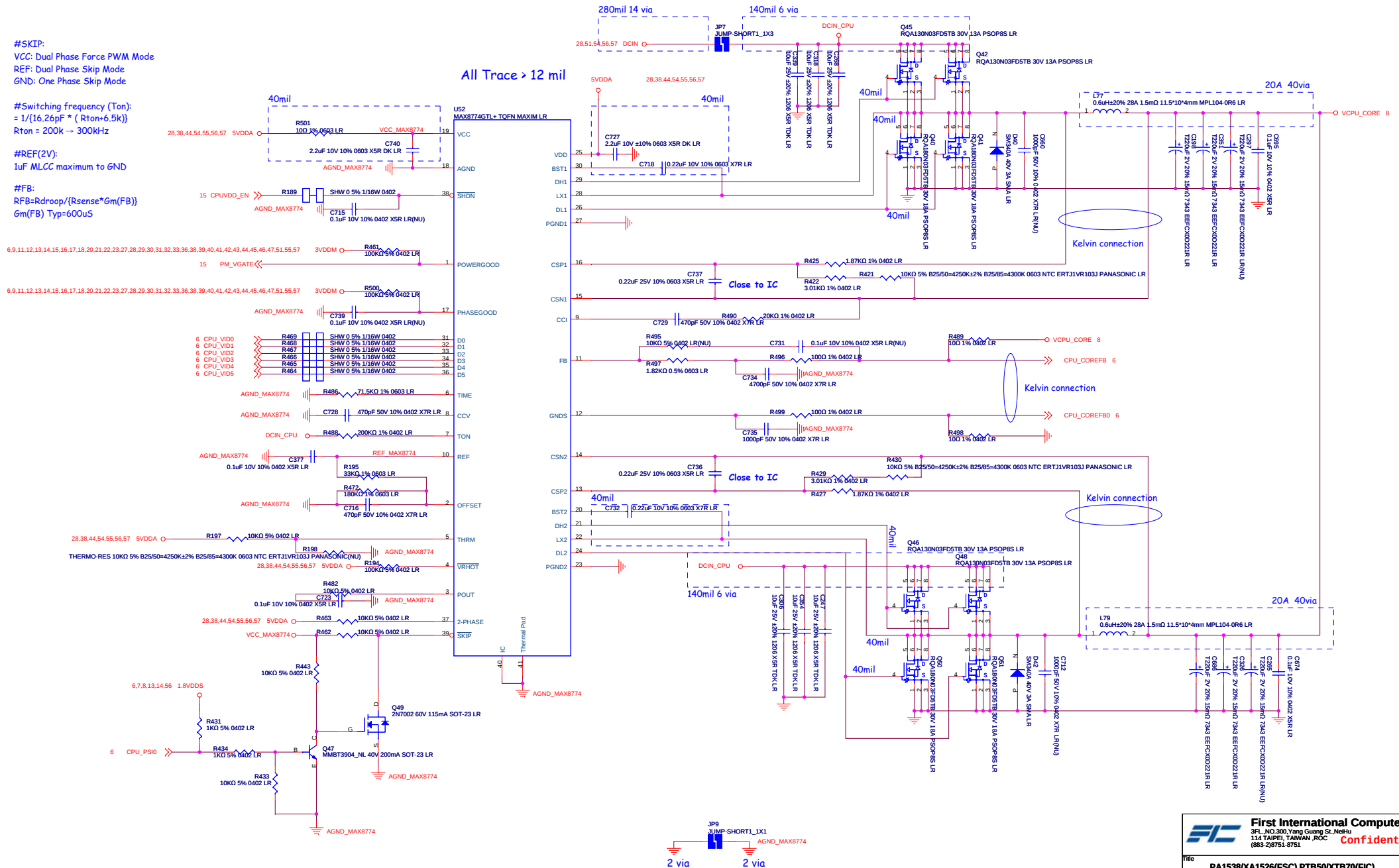
AMD K8 CPU Core Power (MAX8774)

#SKIP:
VCC: Dual Phase Force PWM Mode
REF: Dual Phase Skip Mode
GND: One Phase Skip Mode

#Switching frequency (Ton):
= $1/(16.26\mu F * (R_{ton} + 6.5k))$
Rton = 200k → 300kHz

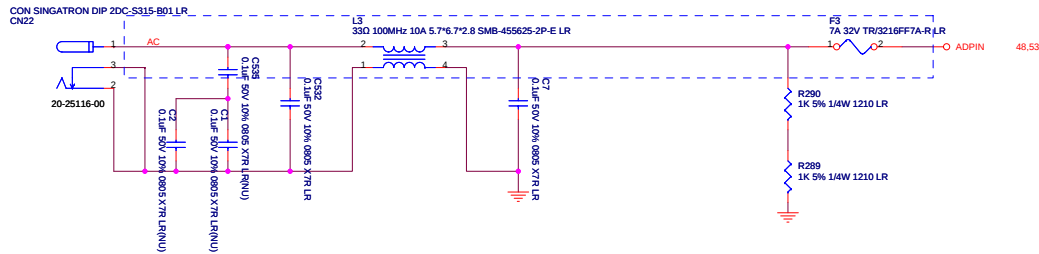
#REF(2V):
1uF MLCC maximum to GND

#FB:
RFB=Rdroop/(Rsense*Gm(FB))
Gm(FB) Typ=600uS

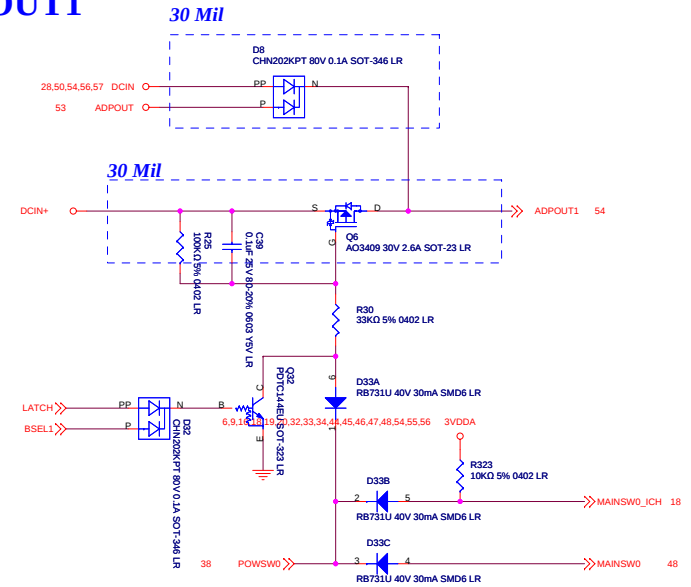


ACIN

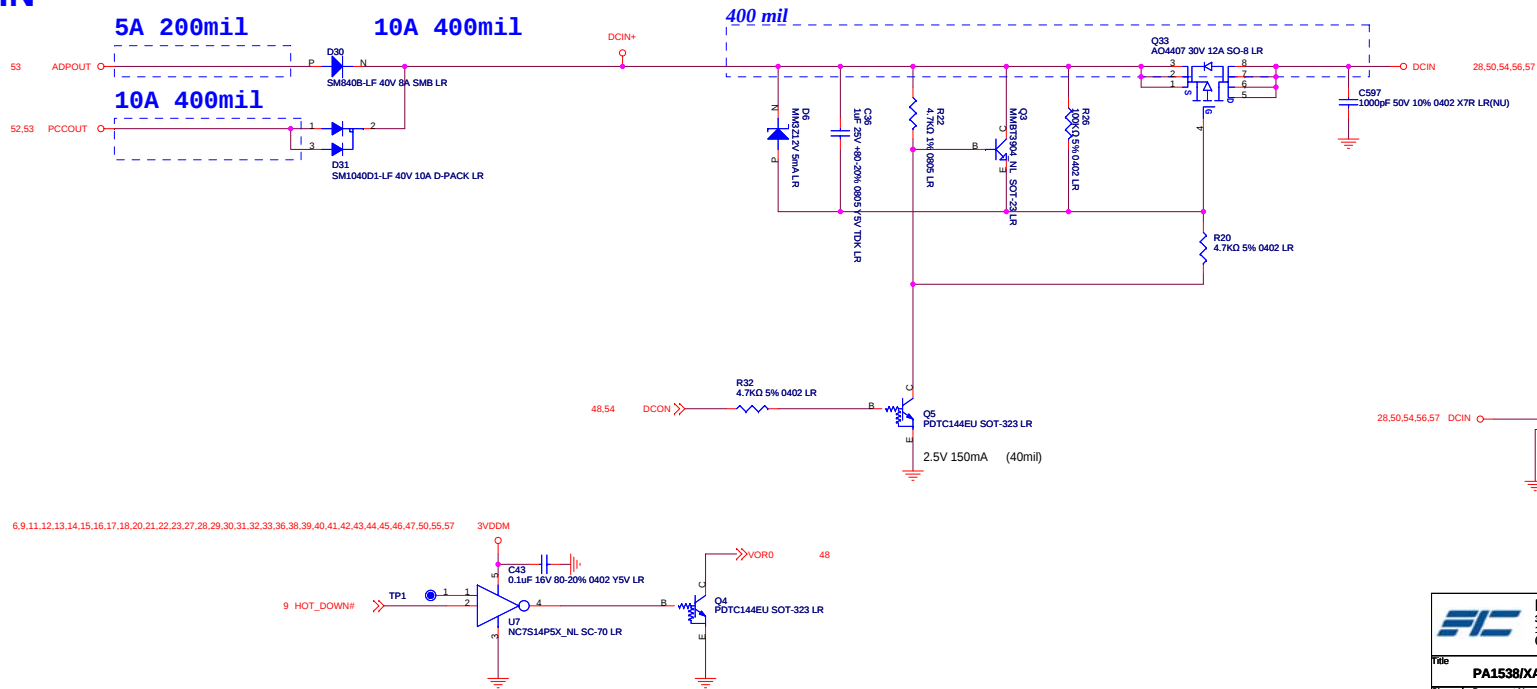
5A 200mil



ADPOUT1



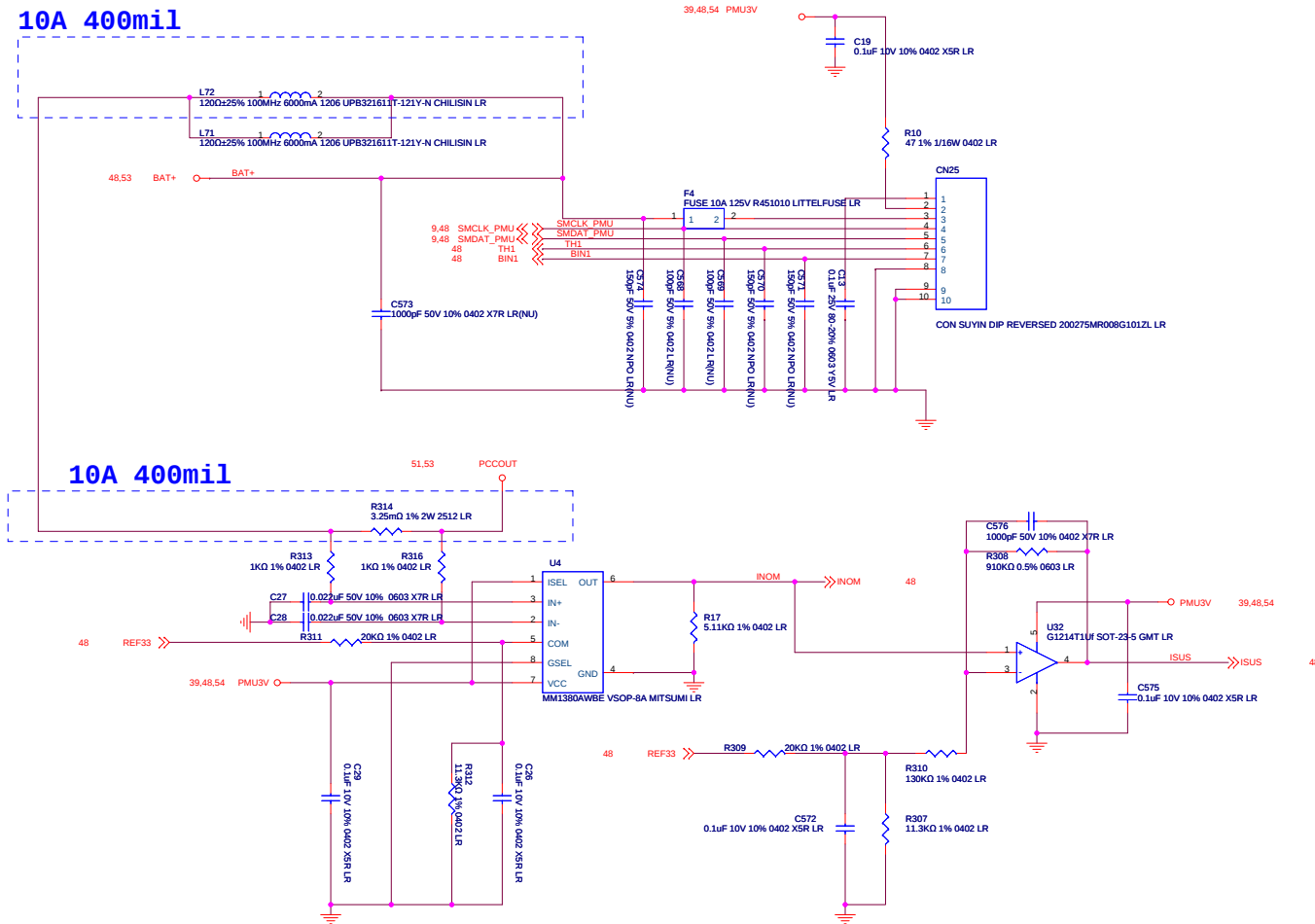
DCIN+ / DCIN



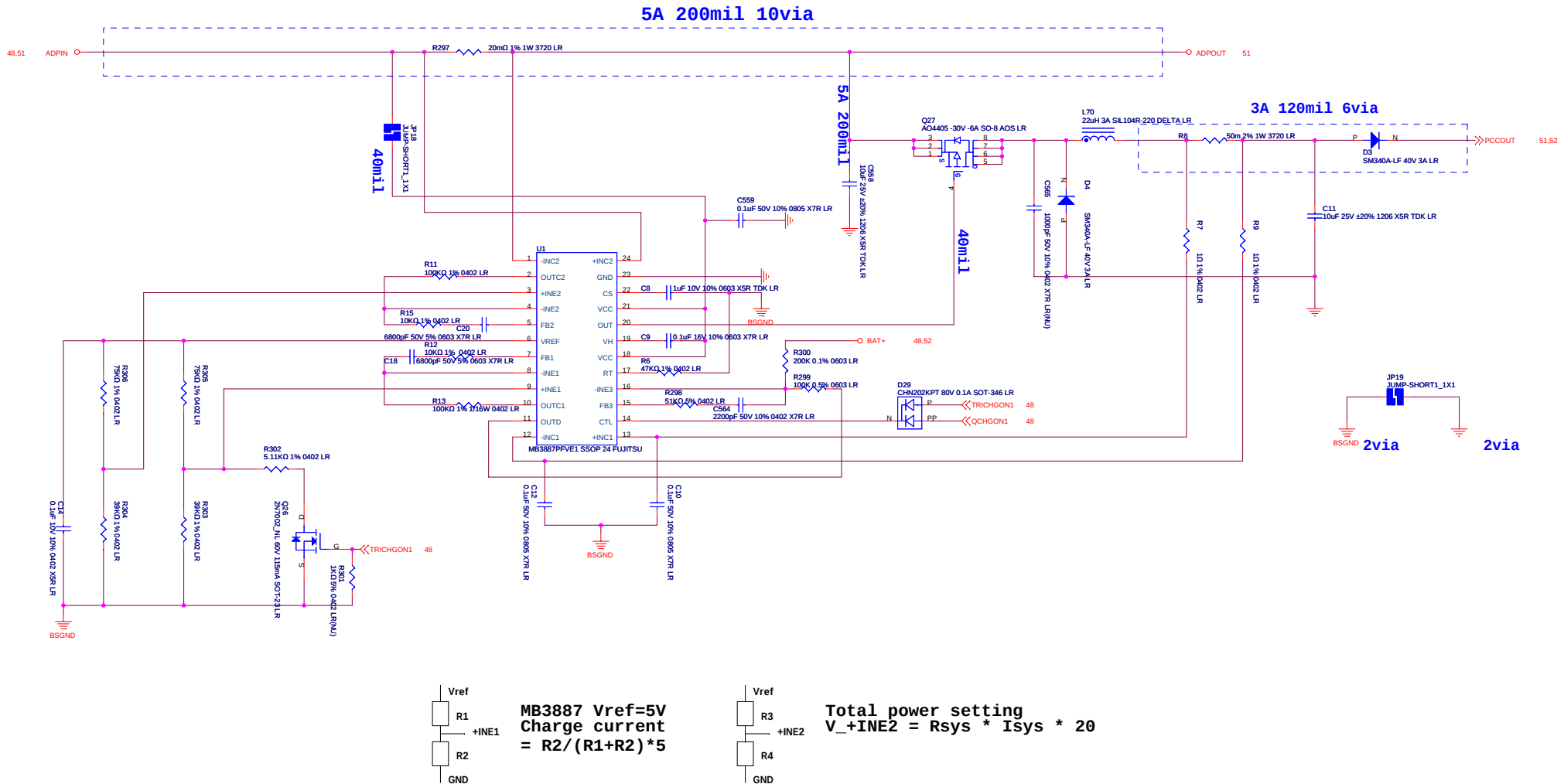
BATT CNN

Layout guideline : Close Battery CNN

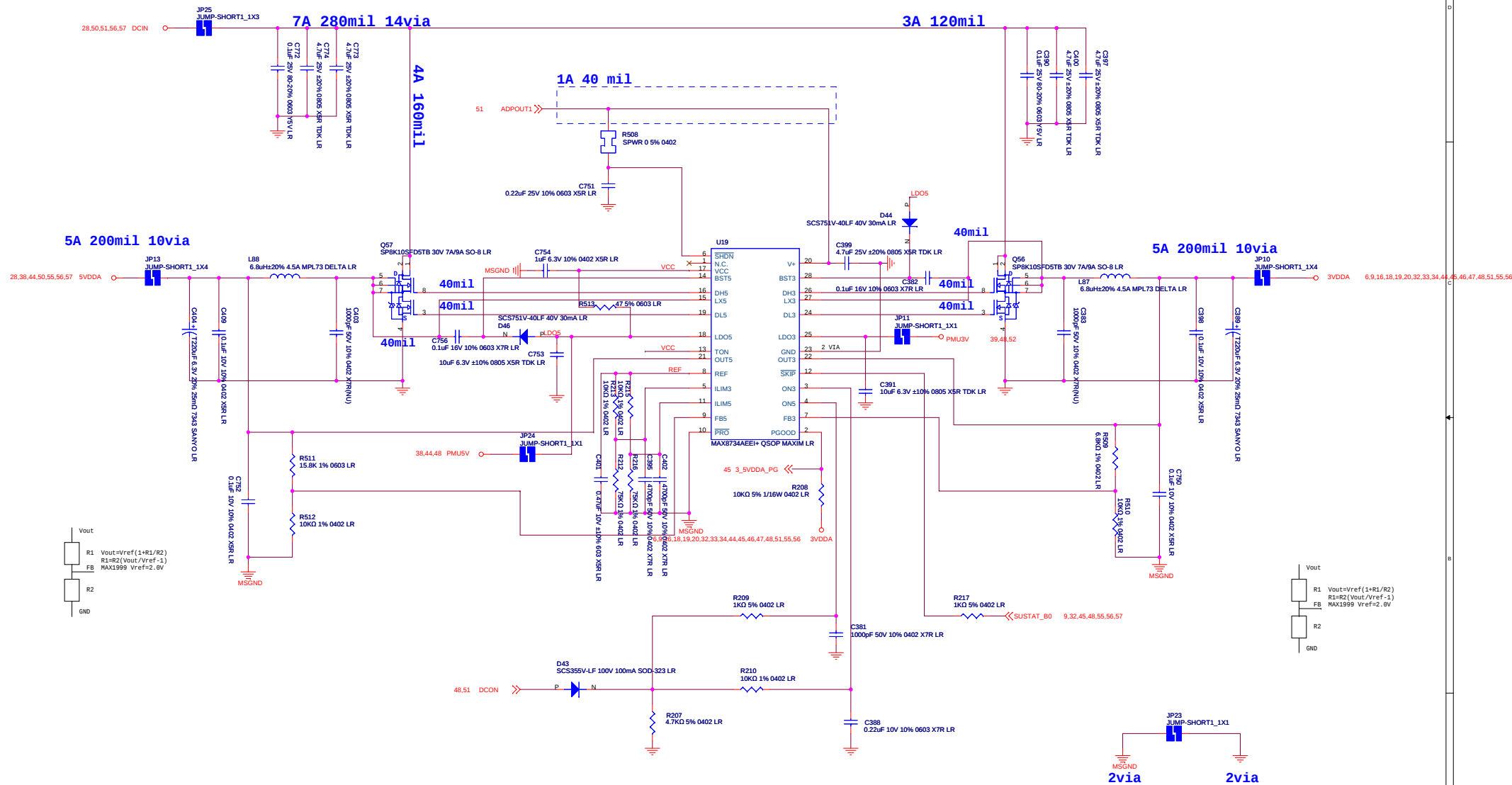
10A 400mil



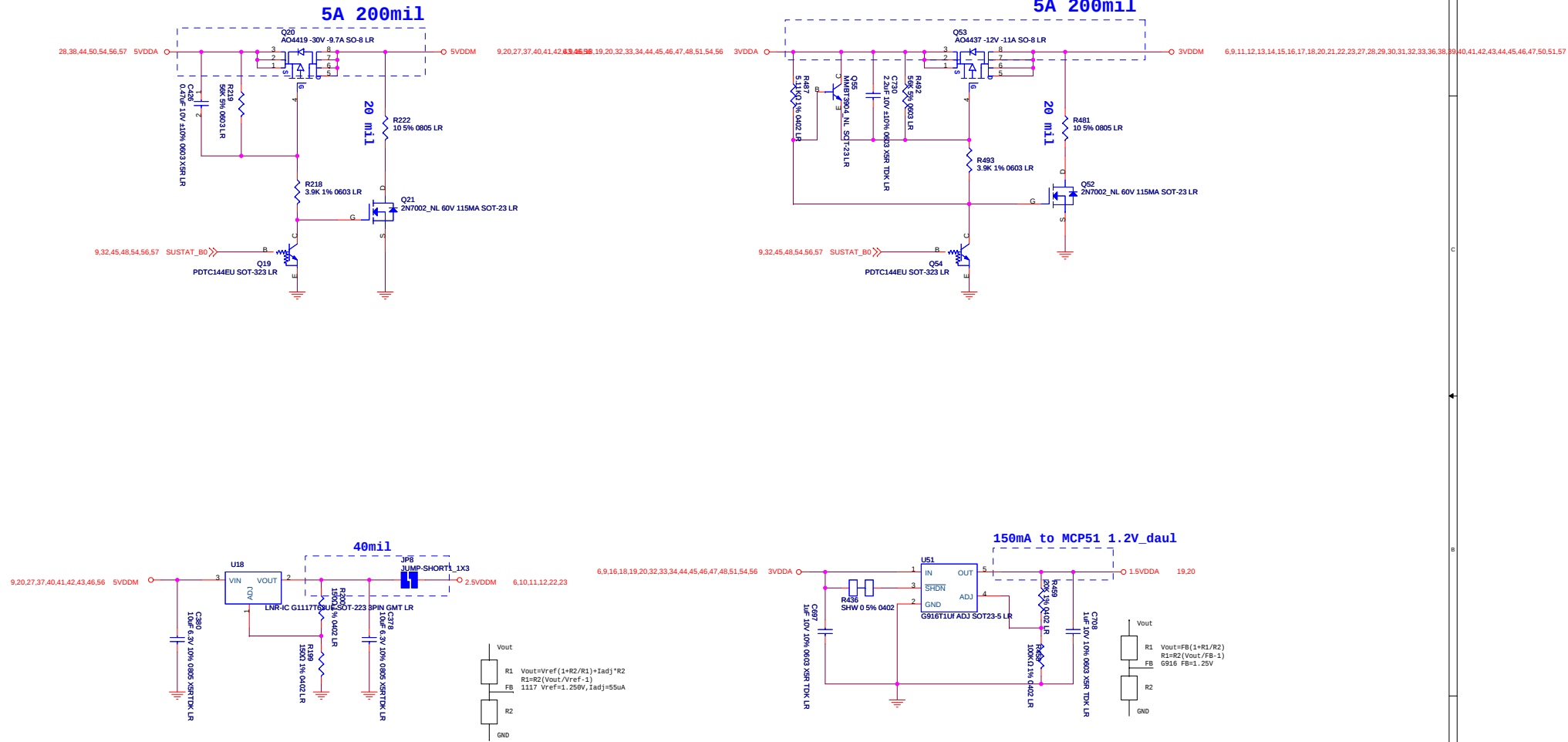
Charger



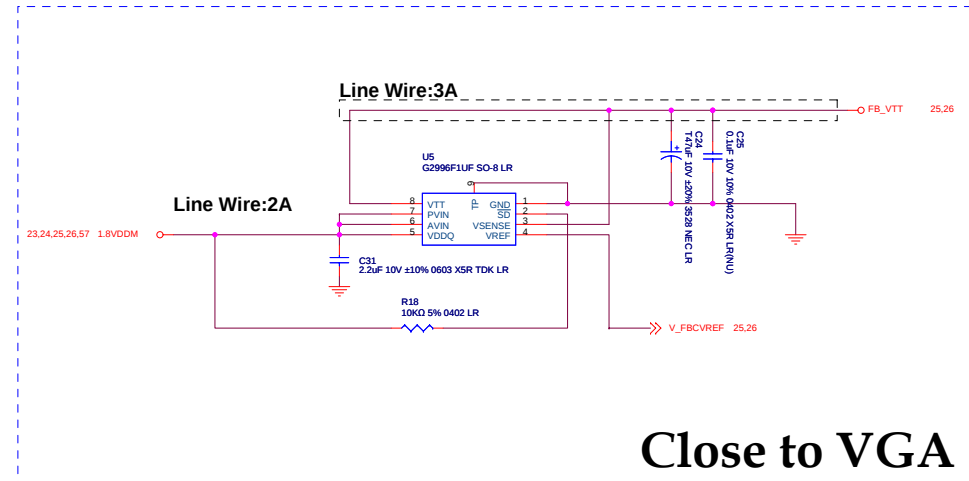
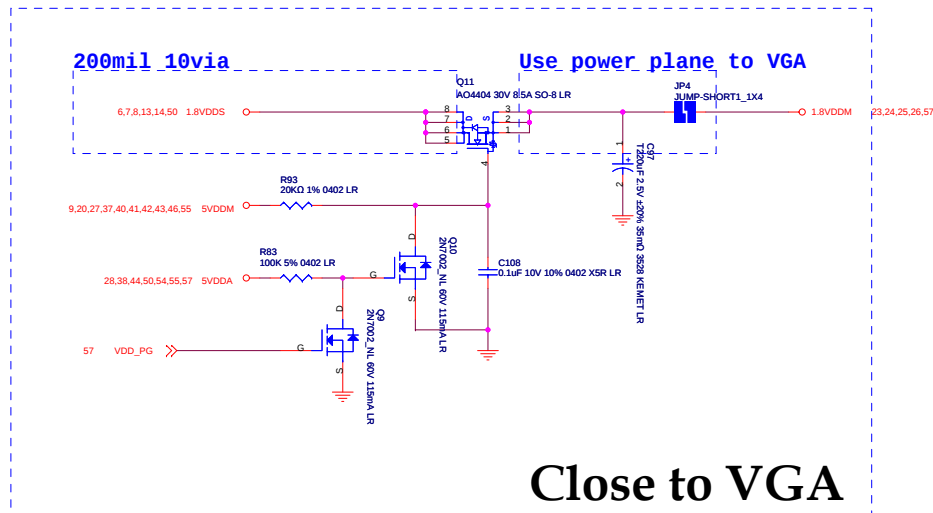
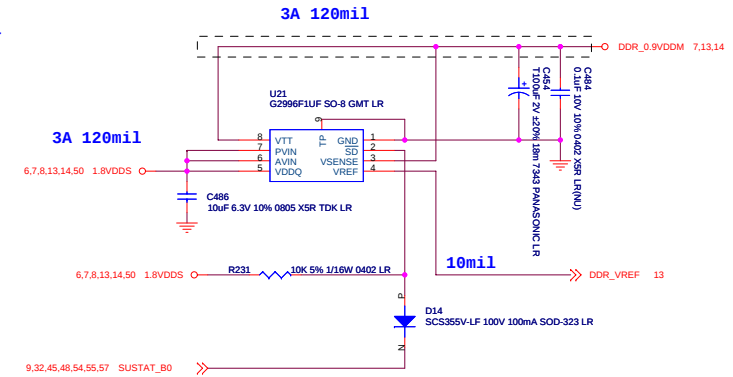
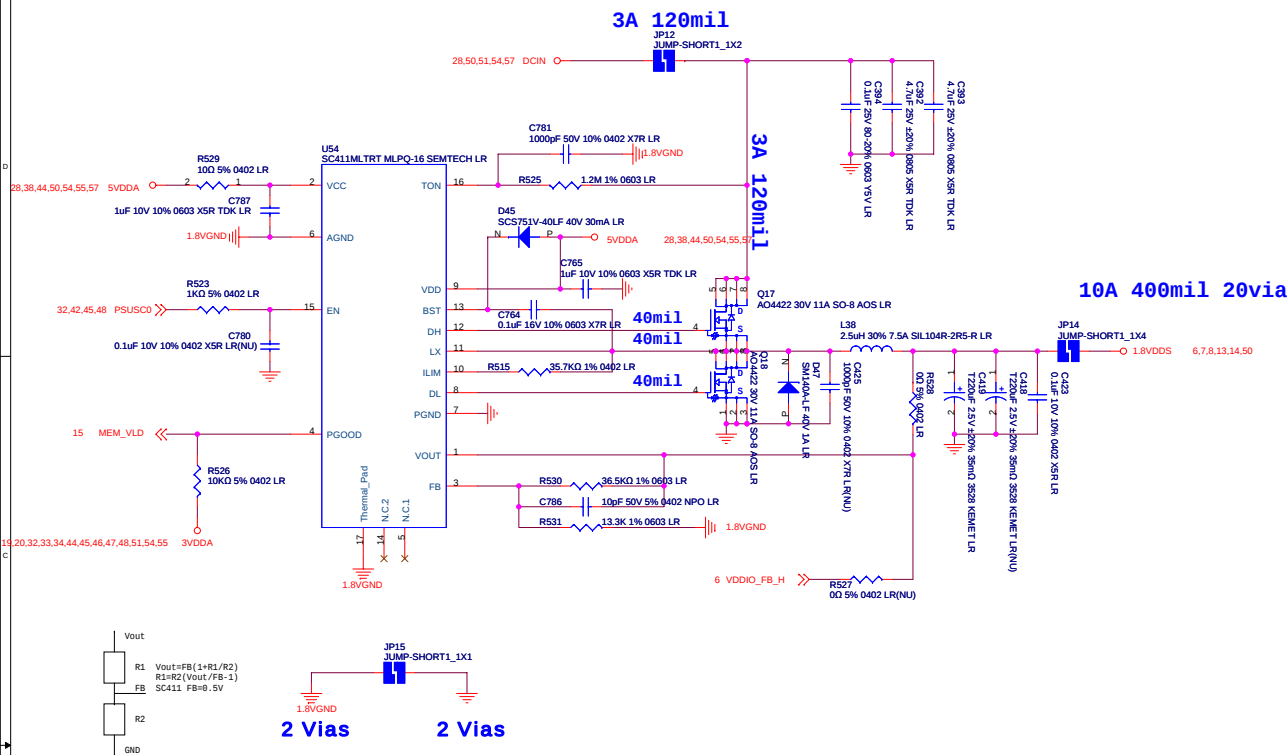
3VDDA / 5VDDA / PMU3/5V



3VDDM/5VDDM



DDRII Power



VGA POWER / 1.2VDDM / 1.5VDDM

