

First International Computer, Inc

Portable Computer Group HW Department

Board name : MotherBoard Schematic

Project : AMD S1 + MCP67MD + NB8M-SE

Version : 0.1

Initial Date : 10/25/2006

Confidential

Manager Sign by : Avery Lee

Drawing by : Ahsing Huang

Total confirm by : Adam Cho

		First International Computer, Inc. 3FL, NO. 300, Yang Guang St., Neihu 114 TAIPEI, TAIWAN, R.O.C. (886-2)8751-8751	
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1. Schematic Page Description :

FIC Schematic Ver : 0.1

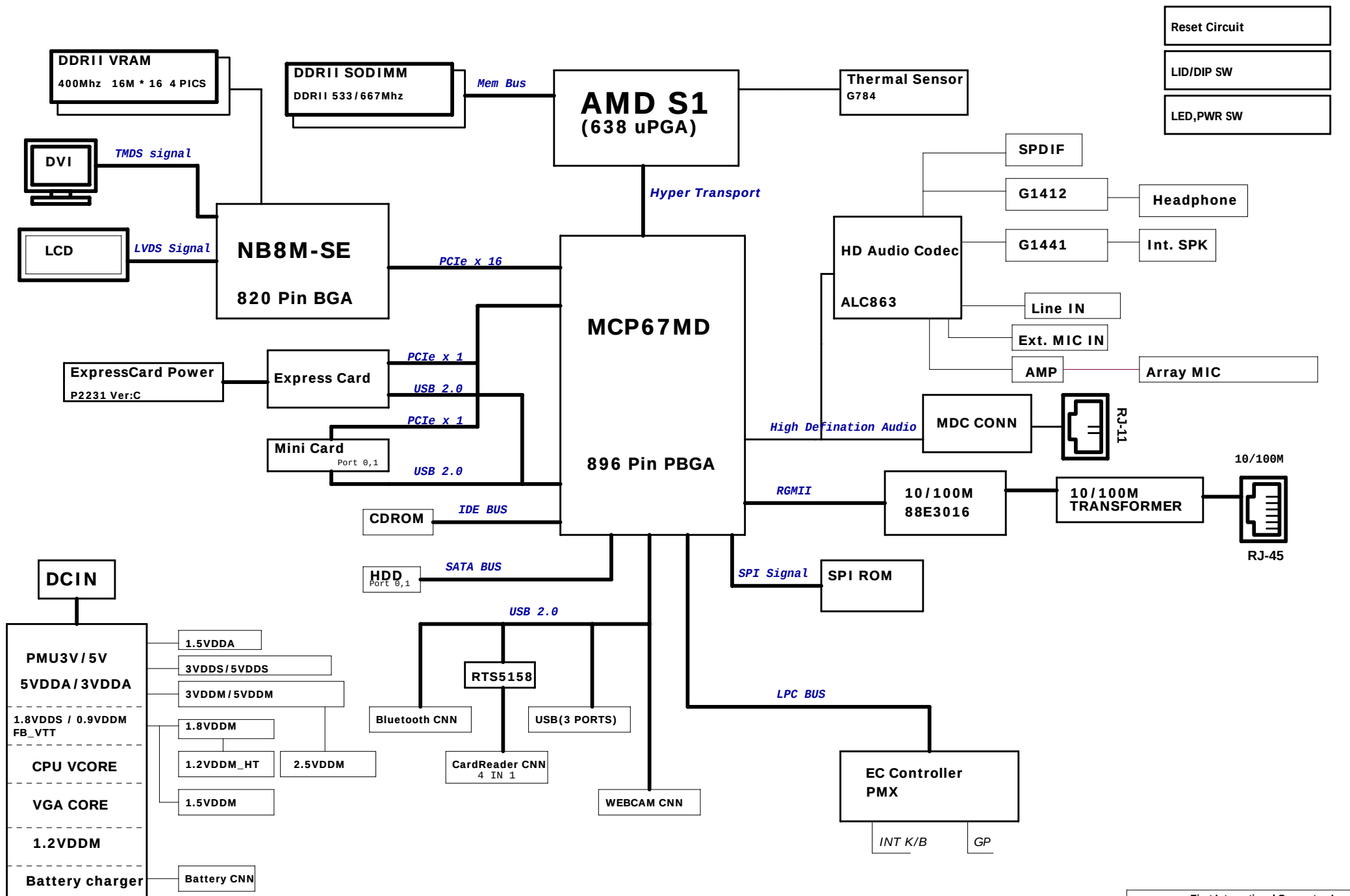
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19. DDRII SO-DIMM 0 RSV	39. RTC/ BLUETOOTH CNN		
20. DDRII SO-DIMM 1 STD	40. SATA HD / CD-ROM CNN		

2. PCI BUS Description :

IDSEL	CHIP
AD22	1394 VIA VT6311S

PCIINT	CHIP
IRQA	—
IRQB	—
IRQC	1394 VIA VT6311S
IRQD	—

BUSMASTER	REQ	CHIP
REQ0 / GNT0	—	—
REQ1 / GNT1	—	1394 VIA VT6311S
REQ2 / GNT2	—	—
REQ3 / GNT3	—	—
REQ4 / GNT4	—	—



4. Net name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON or PSUSC0
3VDDA	3.3V always on power rail by DCON or PSUSC0
1.5VDDA	1.5V always on power rail by DCON or PSUSC0
1.8VDDS	1.8V power rail
1.2VDDA	1.2V always on power rail by 3VDDA
0.9VDDM	0.9V DDR Termination Voltage
5VDDM	5.0V suspend power rail
3VDDM	3.3V suspend power rail
2.5VDDM	2.5V suspend power rail
1.5VDDM	1.5V suspend power rail
VDD_CORE	Core Voltage for VGA
VCPU_CORE	Core Voltage for CPU
1.2VDDM	VCC For CPU & NB
+1.2VHT	VCC For CPU & NB Hyper Transport

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

0	=	Active Low signal
---	---	-------------------

Signal Conditioning

D	=	Damped (by a resistor)
Q	=	Isolated (by a Q-switch)
L	=	Filtered (by an inductor or bead)

5.Board Stack up Description

PCB Layers

Layer 1		TOP
Layer 2		POWER
Layer 3		IN1(HT/CLOCK/DDR)
Layer 4		IN2(DVI/LVDS/HDMI/other)
Layer 5		GND
Layer 6		BOTTOM

Impedance Based On a Six-Layer Stack-Up

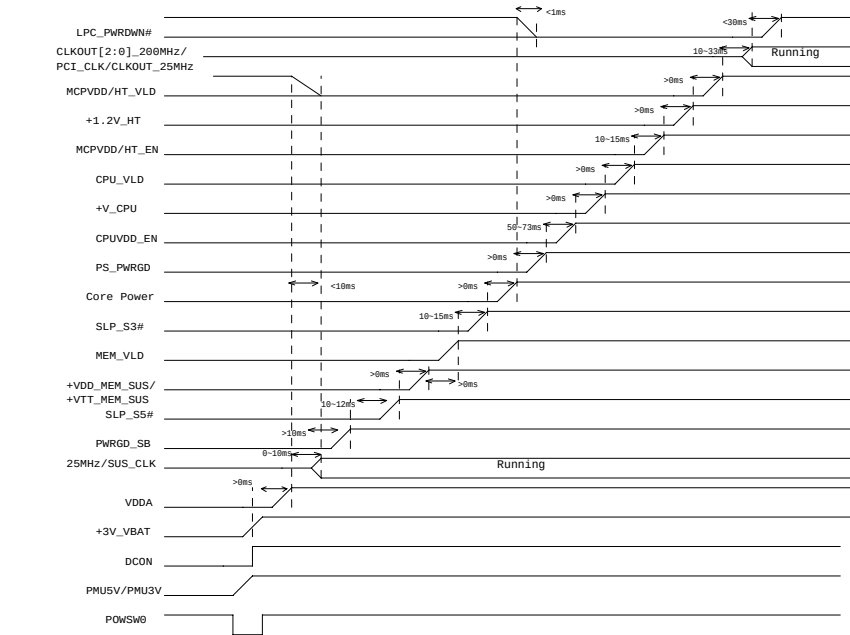
Interface	Impedance
PCI-Express	60 Ohm +/- 10% SE
HT signals	93 Ohm +/- 10% differential
RGMII, SATA, IFP/TMDS, HDMI	55 Ohm +/- 10% SE 100 Ohm +/- 10% differential
USB	50 Ohm +/- 10% SE 90 Ohm +/- 10% differential
All other interfaces	60 Ohm +/- 10% SE

6.Schematic modify Item and History :

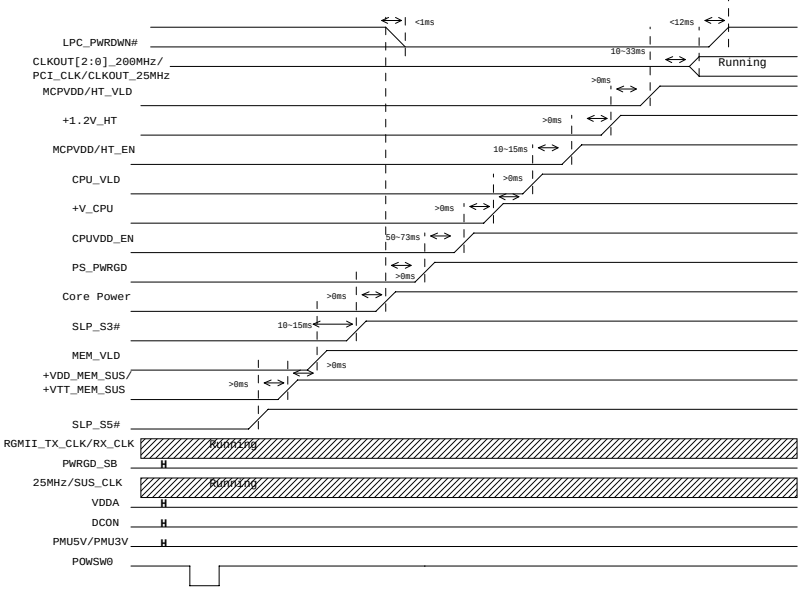
V0.1 --> V0.2

7. power on & off & S3 Sequence :

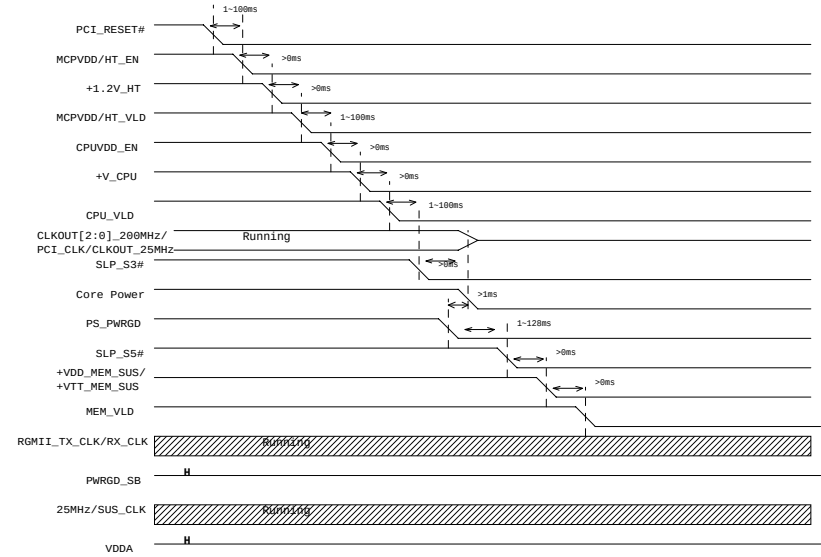
G3-to-S0 Power-Up Sequence



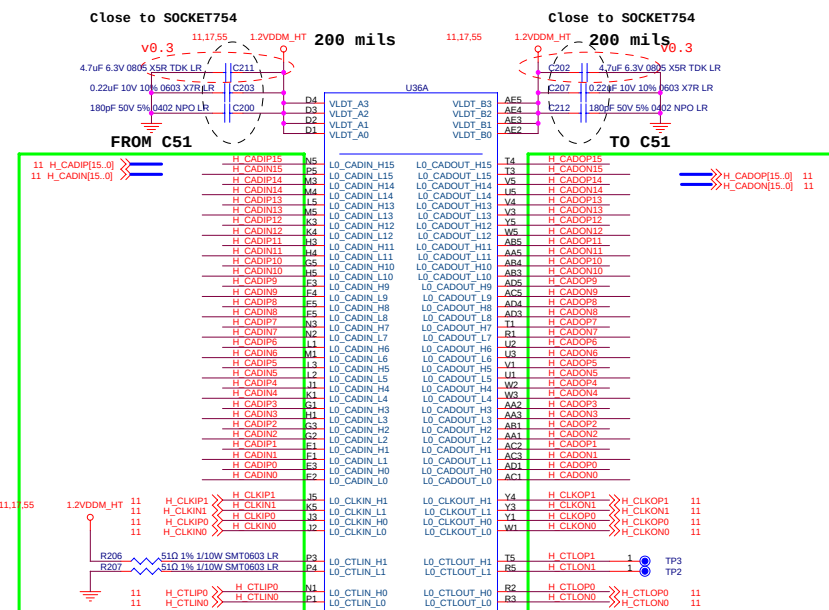
S3/S4/S5 to S0 Resume Sequence



S3/S4/S5 Power-Down Sequence



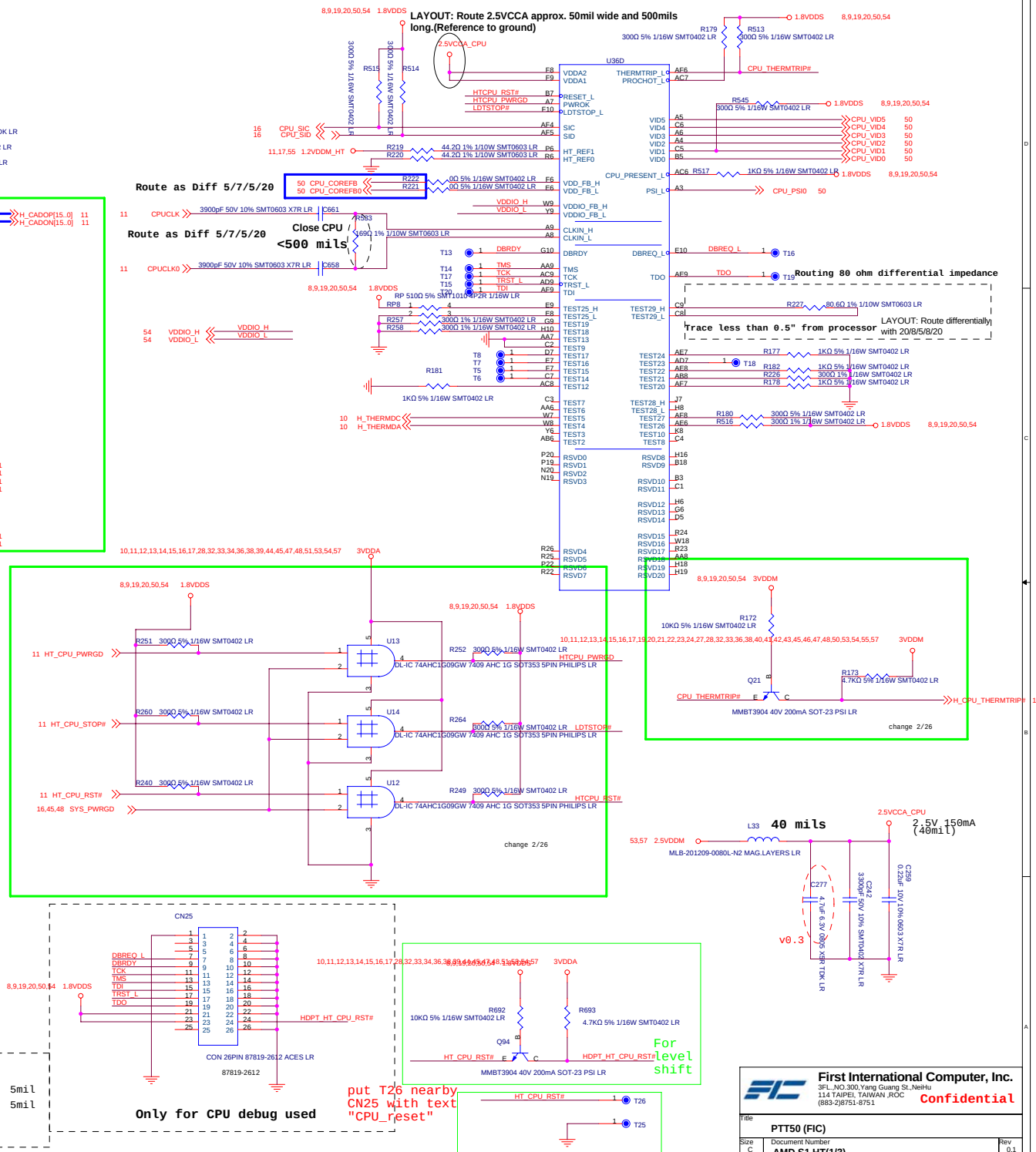
ClawHammer HT Interface



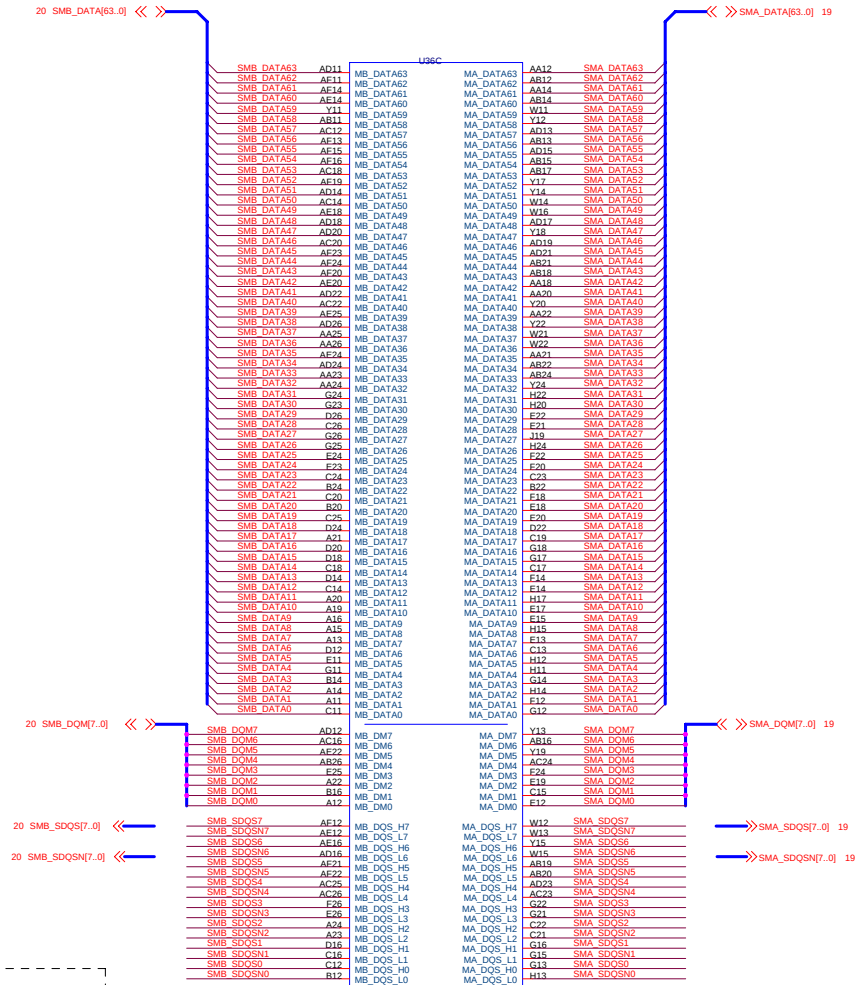
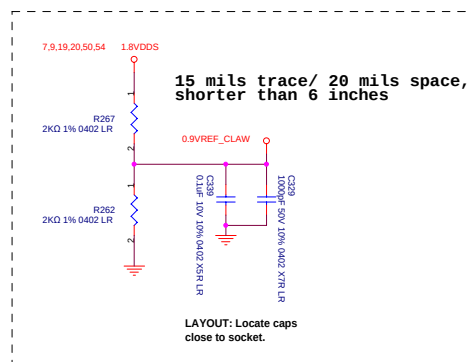
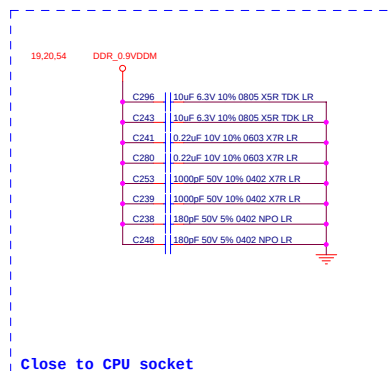
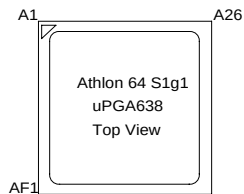
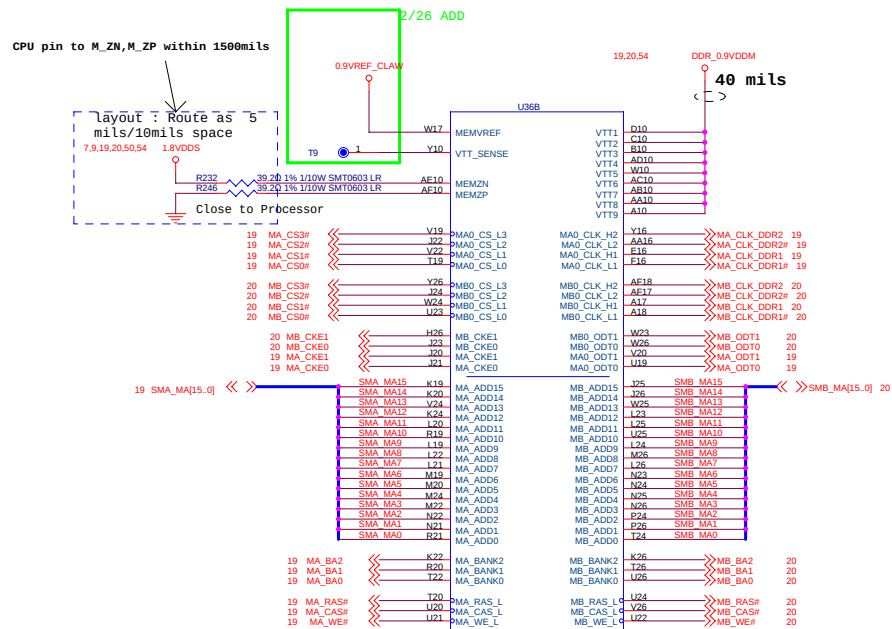
HT BUS General Routing Rules:

1. HT BUS is easy to route, and uses minimal board space.
2. HT BUS length must be greater than 1" and less than 12.0".
3. All CAD/CTL/CLK within a clock group must route at same layer.
4. HT BUS is Ground-referenced differential link.
5. Differential pair length matching within 30 mils.
6. CAD_H to CAD_L length matching within 30 mils.
7. CAD to CAD length matching within 120 mils.
8. CAD to CLK length matching within 60 mils.
9. CLK to CLK length matching within 600 mils(max).
10. CAD/CAD# and CTL/CTL# shall be treated identically within a clock group.

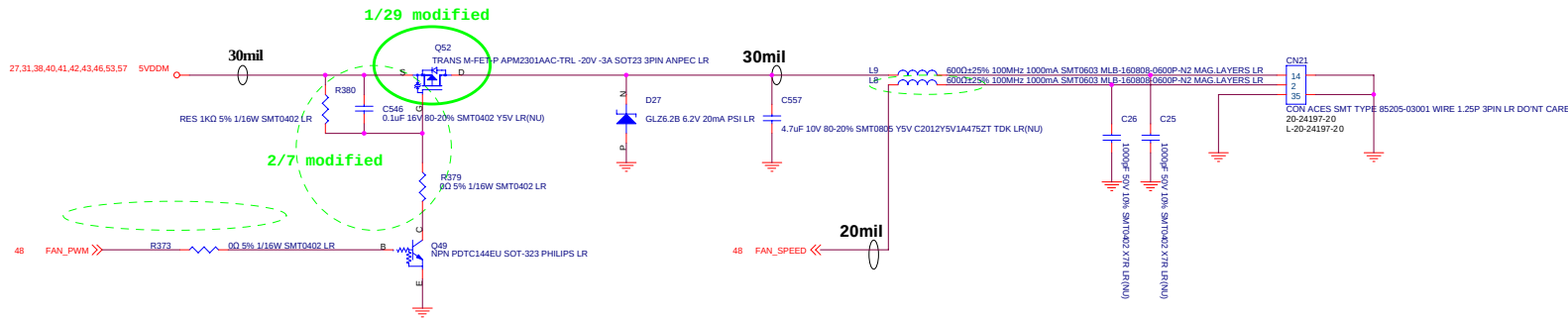
Left			Right		
SIGNAL WSPAC=15mil CADIN_H WDP=5mil CADIN_L WSPAC=15mil SIGNAL			SIGNAL WSPAC=15mil CADOUT_H WDP=5mil CADOUT_L WSPAC=15mil SIGNAL		
SIGNAL WSPAC=15mil H_CLKIP/H_CTLIP WDP=5mil H_CLKIN/H_CTLIN WSPAC=15mil SIGNAL			SIGNAL WSPAC=15mil H_CLKOP/H_CTLOP WDP=5mil H_CLKON/H_CTLON WSPAC=15mil SIGNAL		



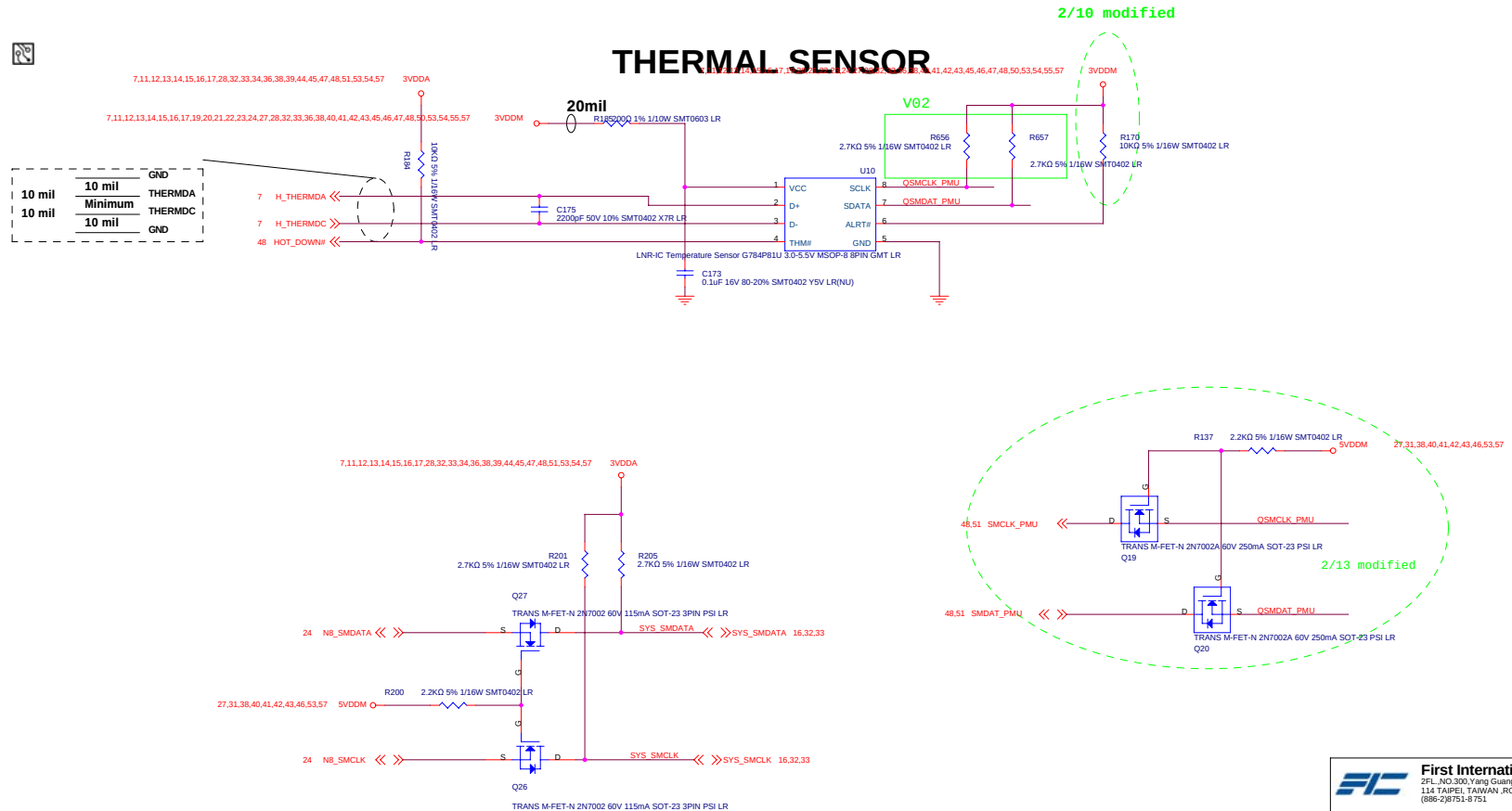
Clawhammer DDR Interface

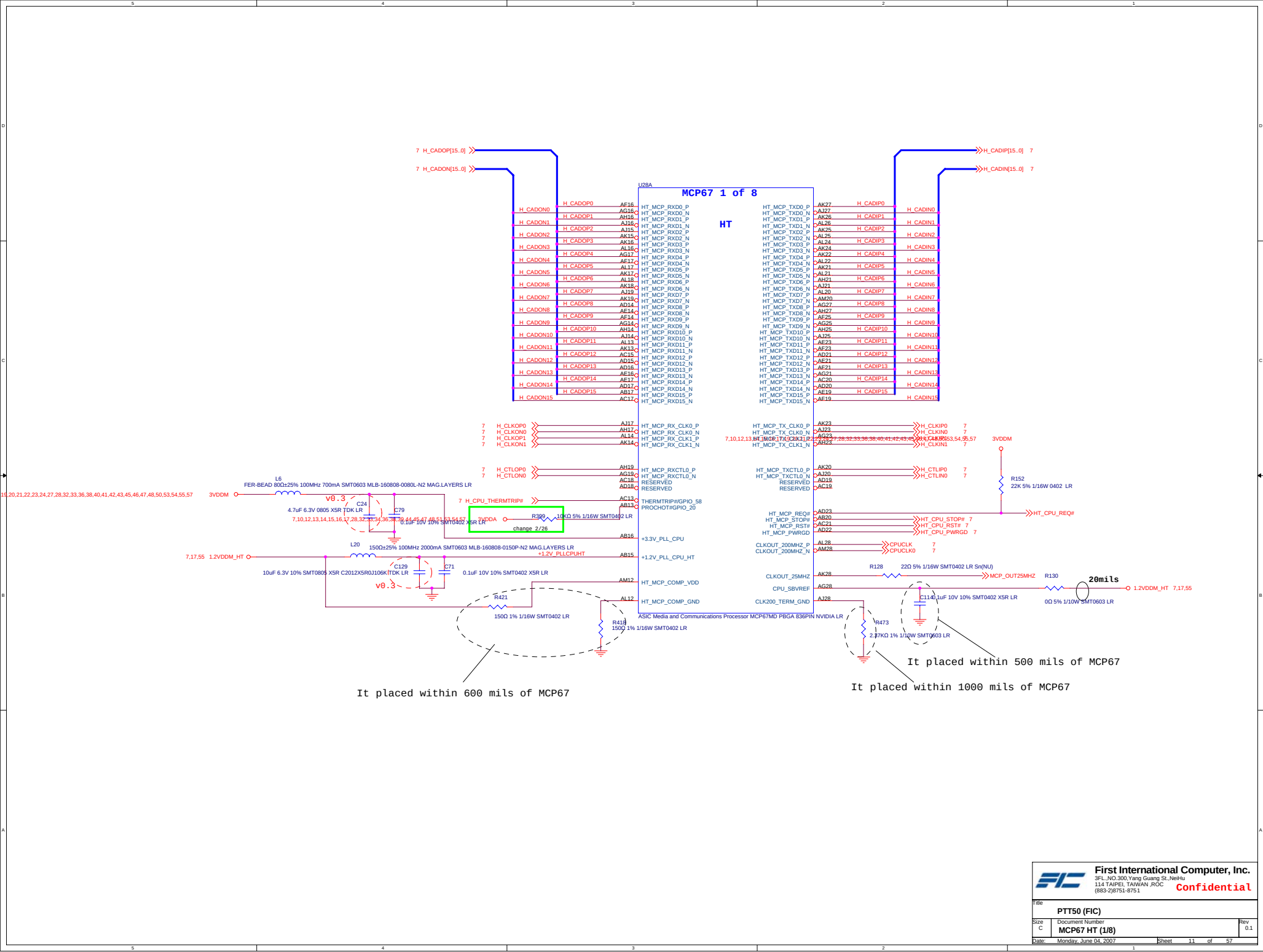


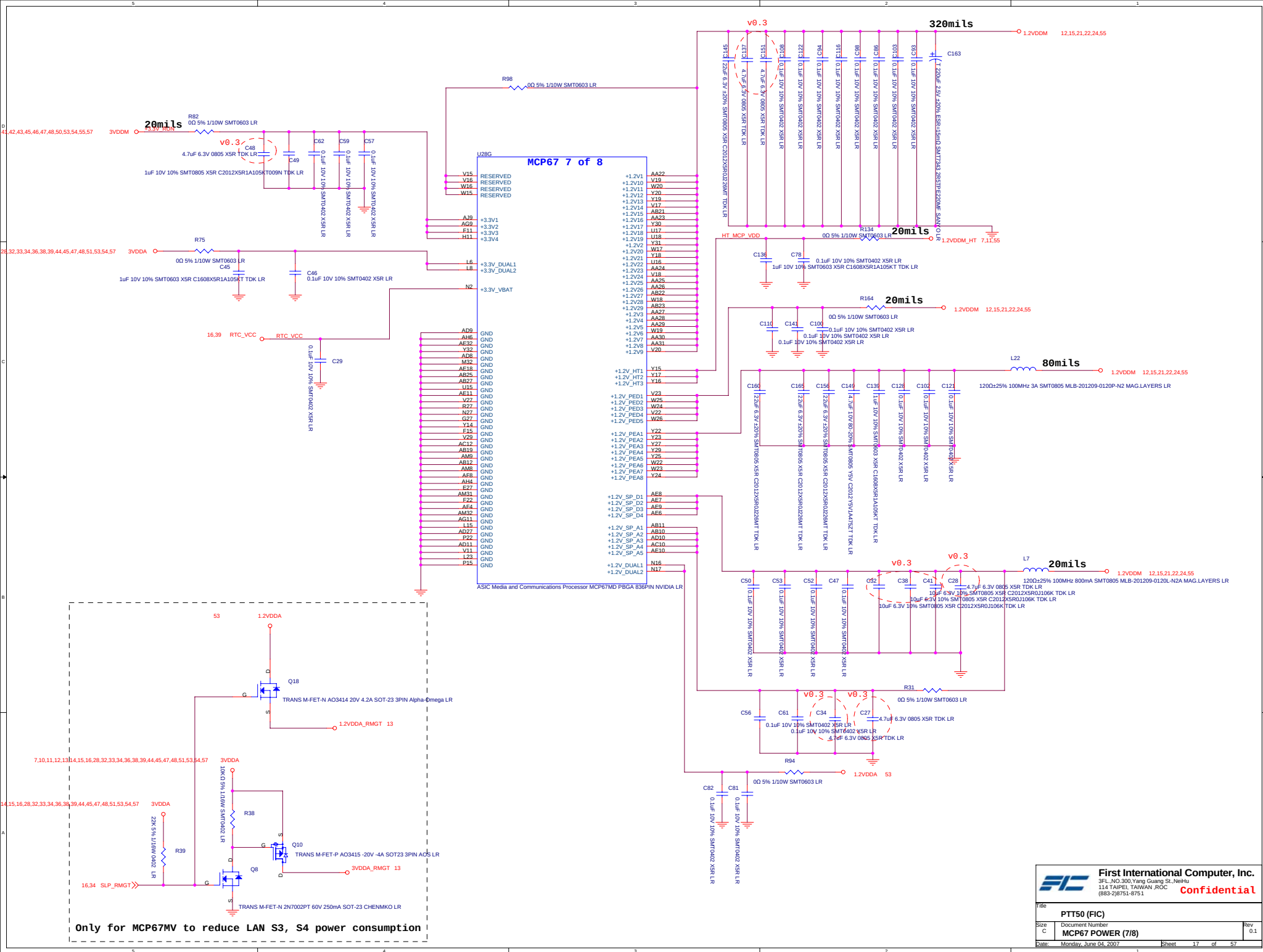
FAN Control

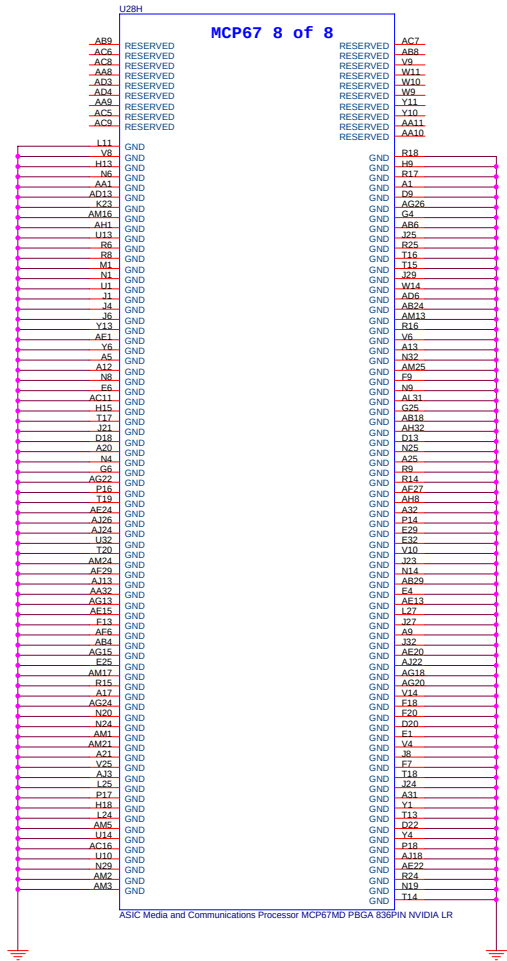


THERMAL SENSOR

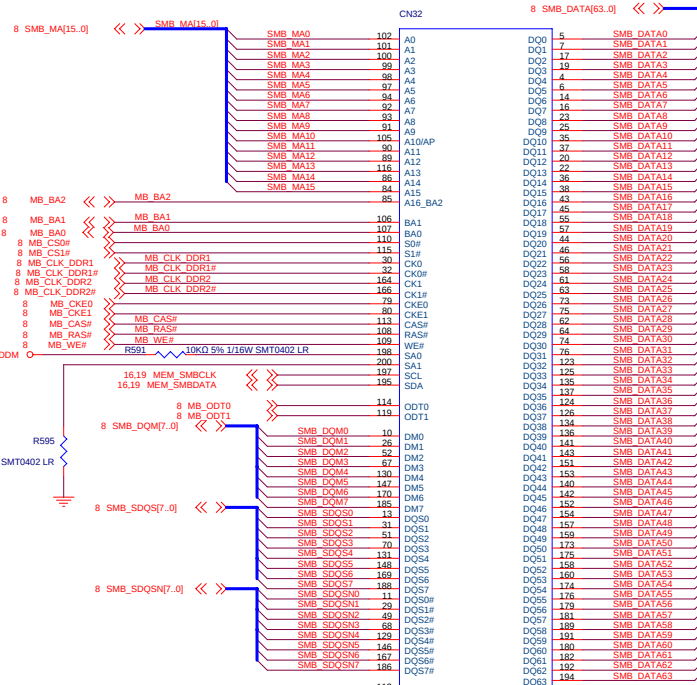
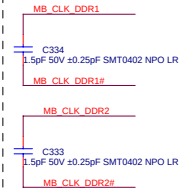








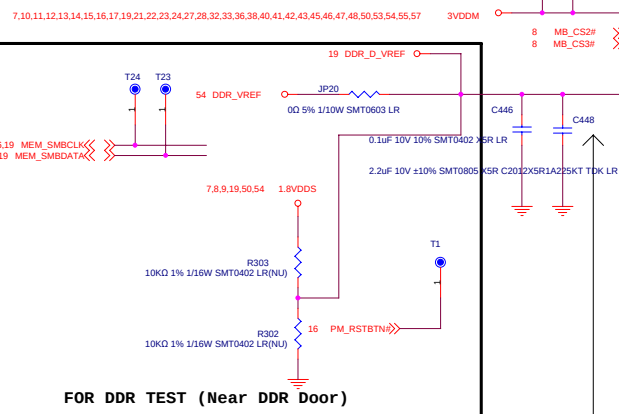
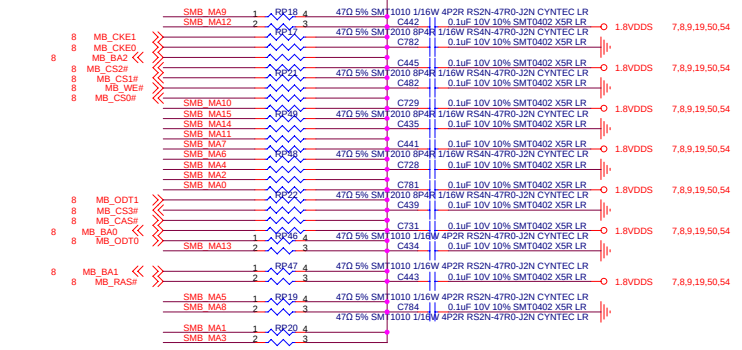
PLACE CLOSE TO CPU
WITHIN 1.2 Inch



LAYOUT
GUIDE

Place one cap close to every 2 pullup
resistors terminated to 0.9vddm

400 mils



FOR DDR TEST (Near DDR Door)

LAYOUT
GUIDE

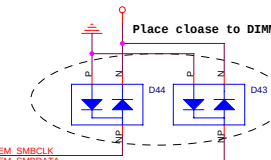
Other signal	20mil	20mil
DDR_VREF	20mil	
Other signal	20mil	

SO DIMM 1

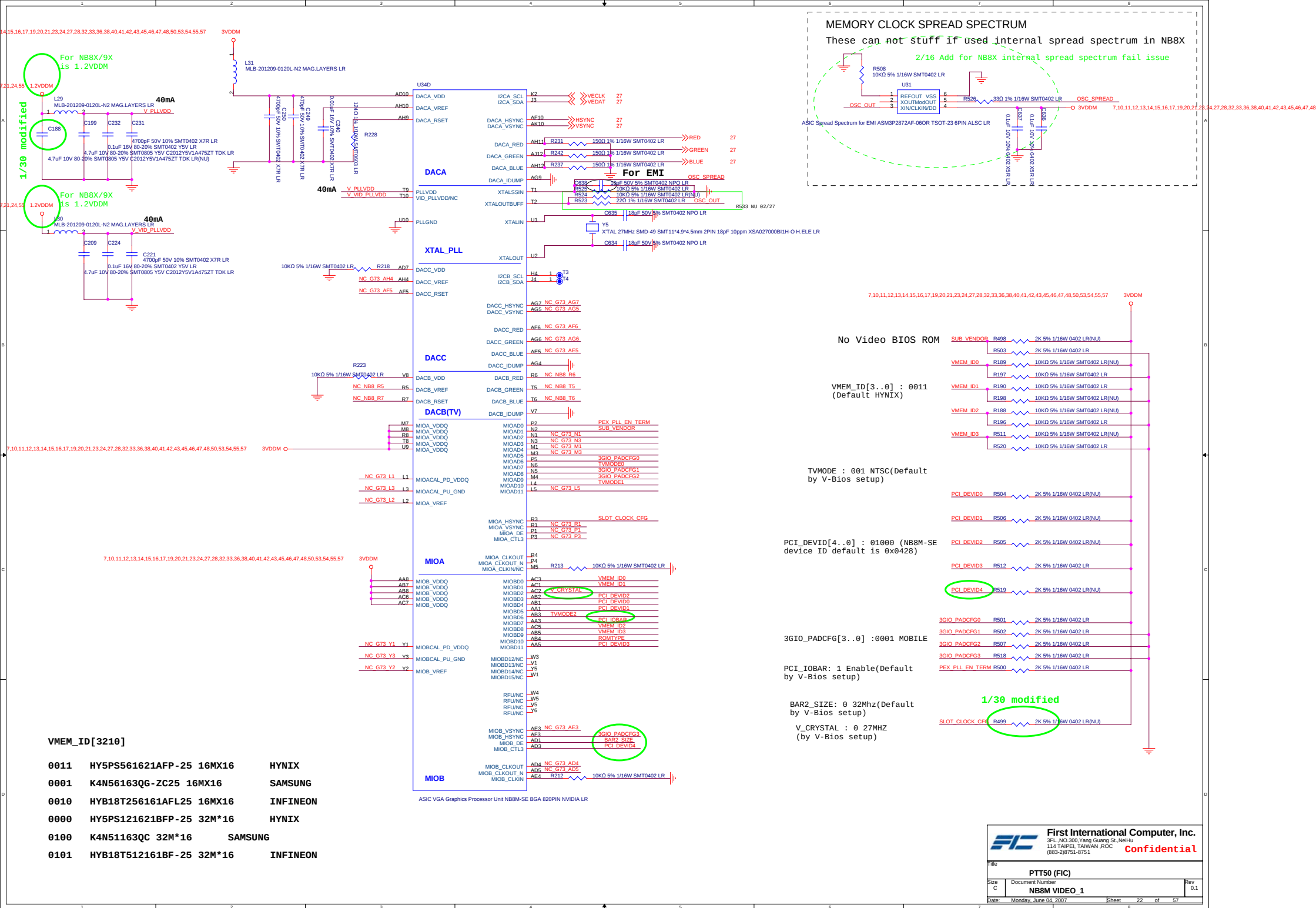
120mil

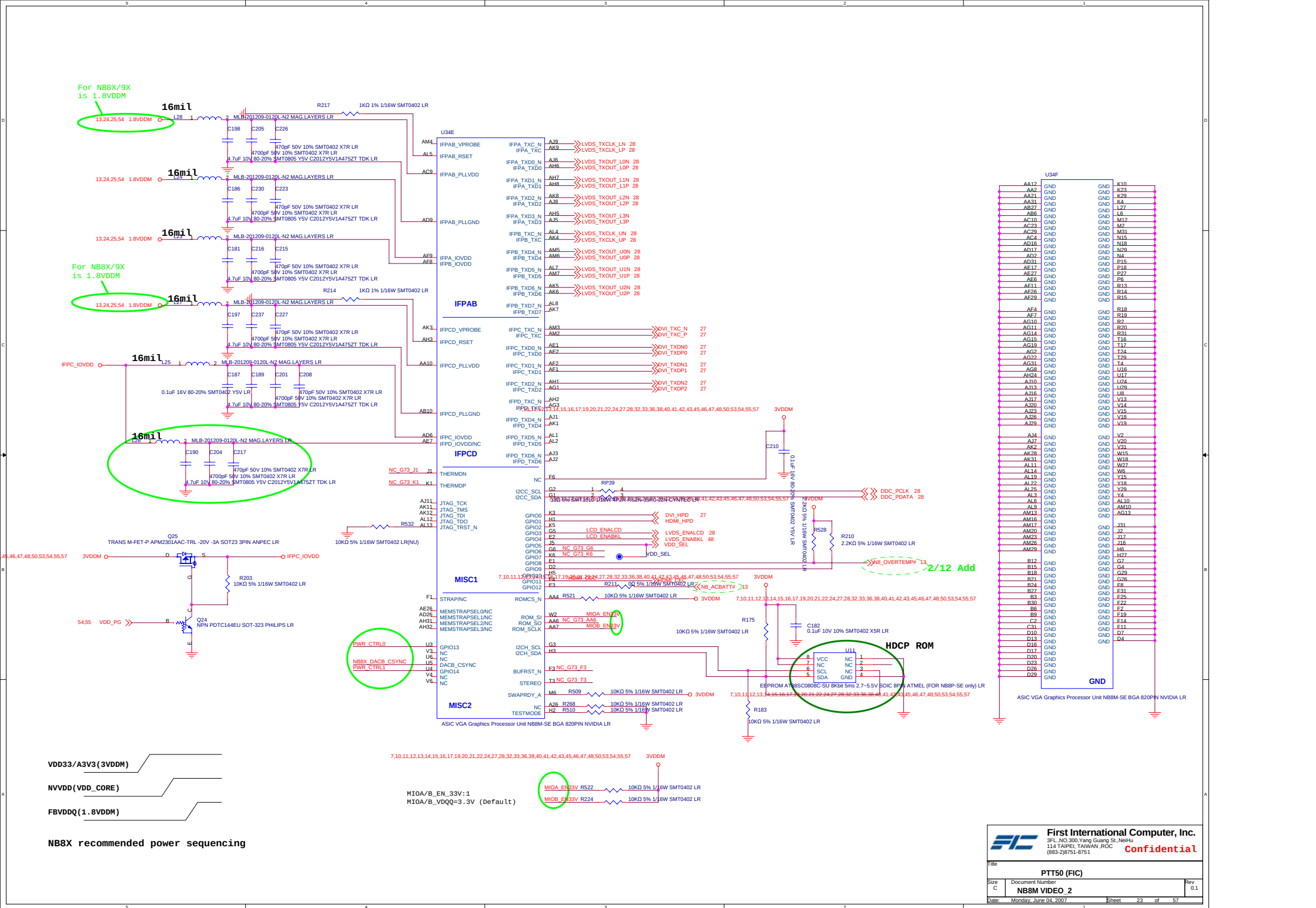
Place these 2.2uF caps
near So-Dimm0

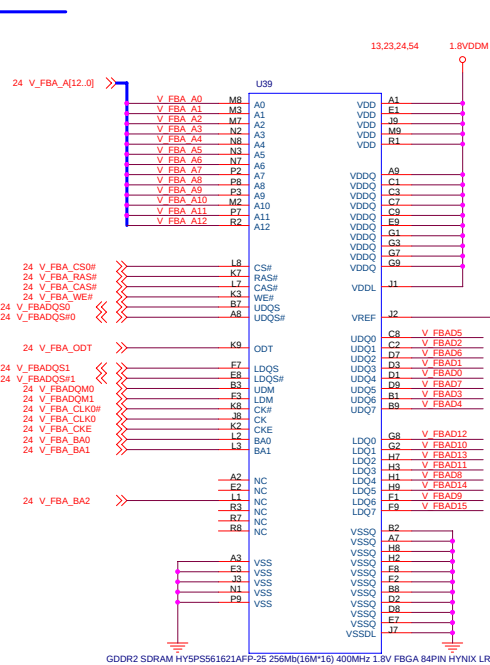
Place these 0.1uF caps
near So-Dimm0



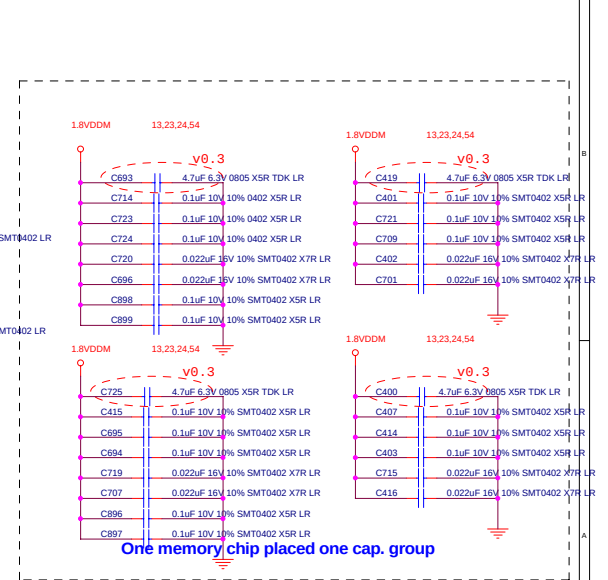
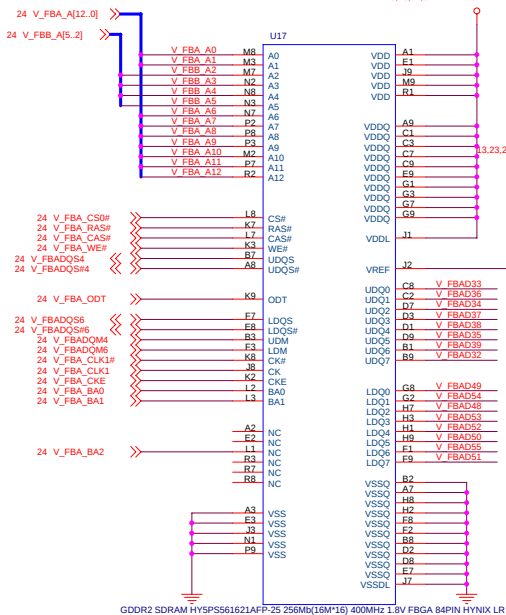
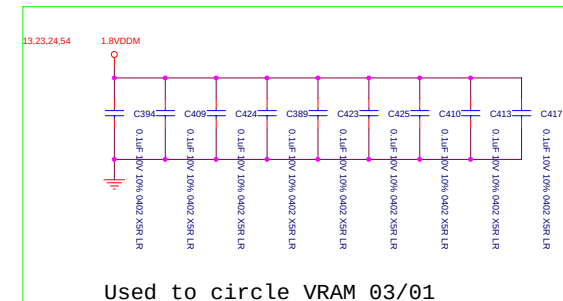
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Matched within +/- 0.15 tck





LAYOUT GUIDE

20 mil	Other Signal
20 mil	MXM_RED
20 mil	MXM_GREEN
20 mil	MXM_BLUE
20 mil	Other Signal

WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms
WIDTH=5 MILS Z0=50 ohms

22 RED
22 GREEN
22 BLUE

(10mil)

(10mil)

Place near to connector

WIDTH=4 MILS Z0=55 ohms

WIDTH=4 MILS Z0=55 ohms

For EMI

For EMI

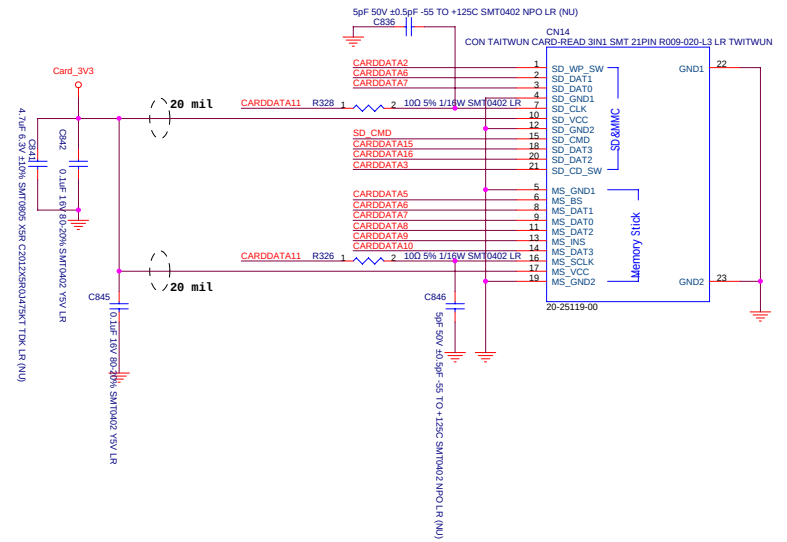
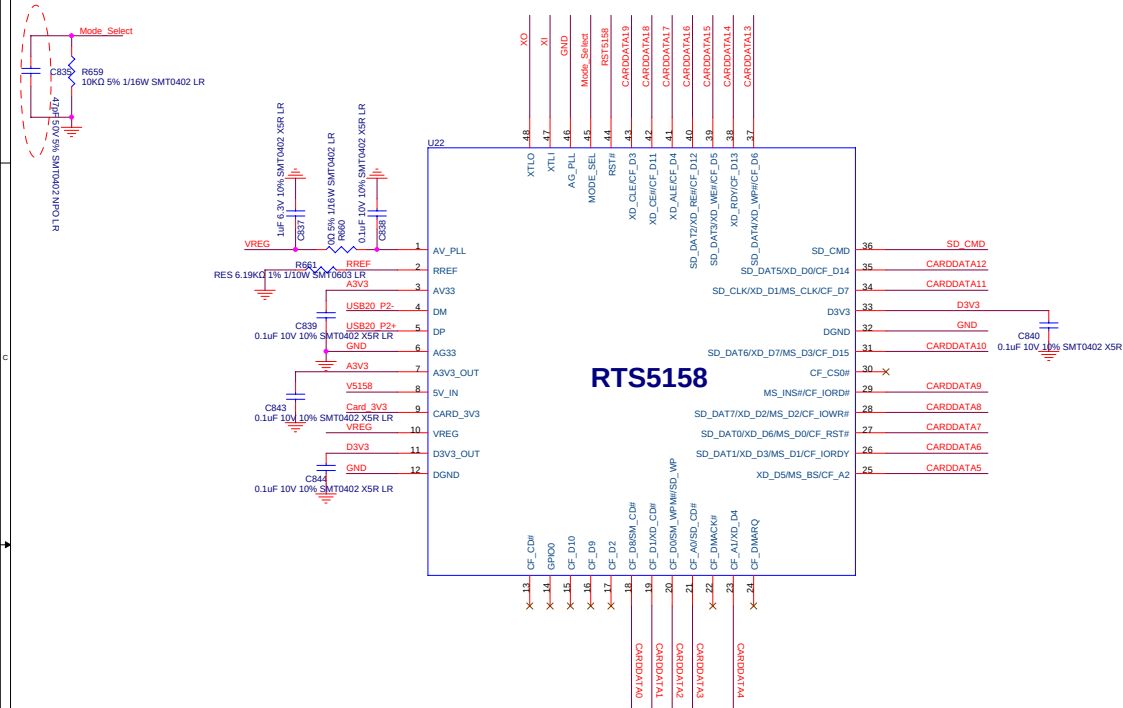
DVI CIRCUIT

06/25
MODIFY

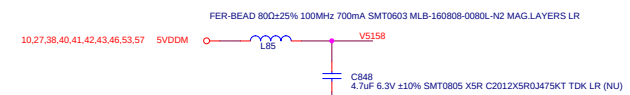
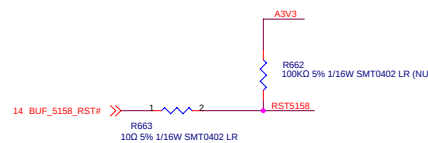
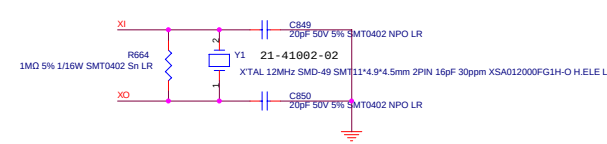
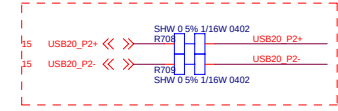
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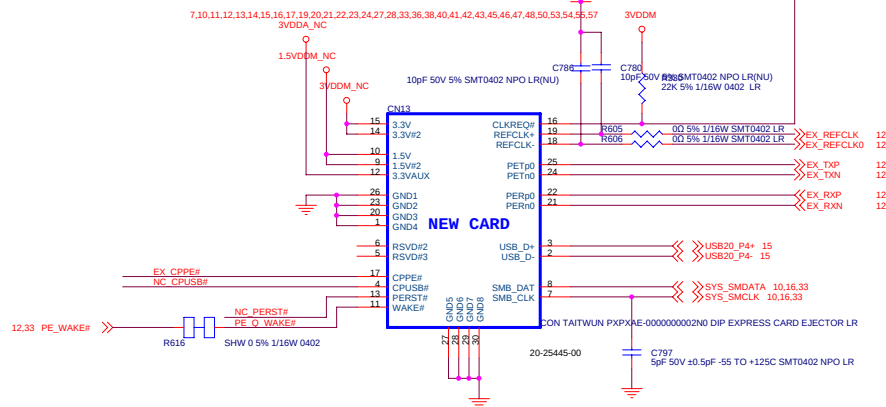
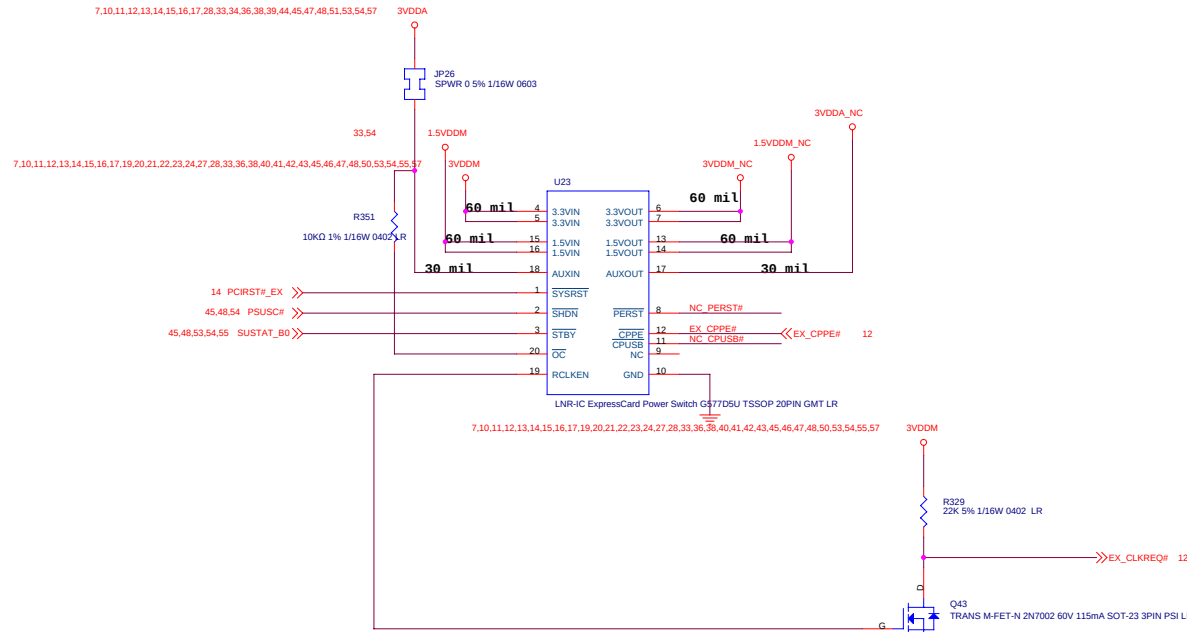
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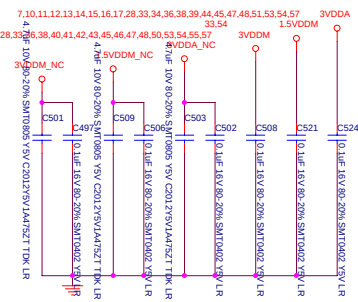
INTERFACE





Express Card Ejector : 20-25445-00

Express Card Header : 20-25446-00



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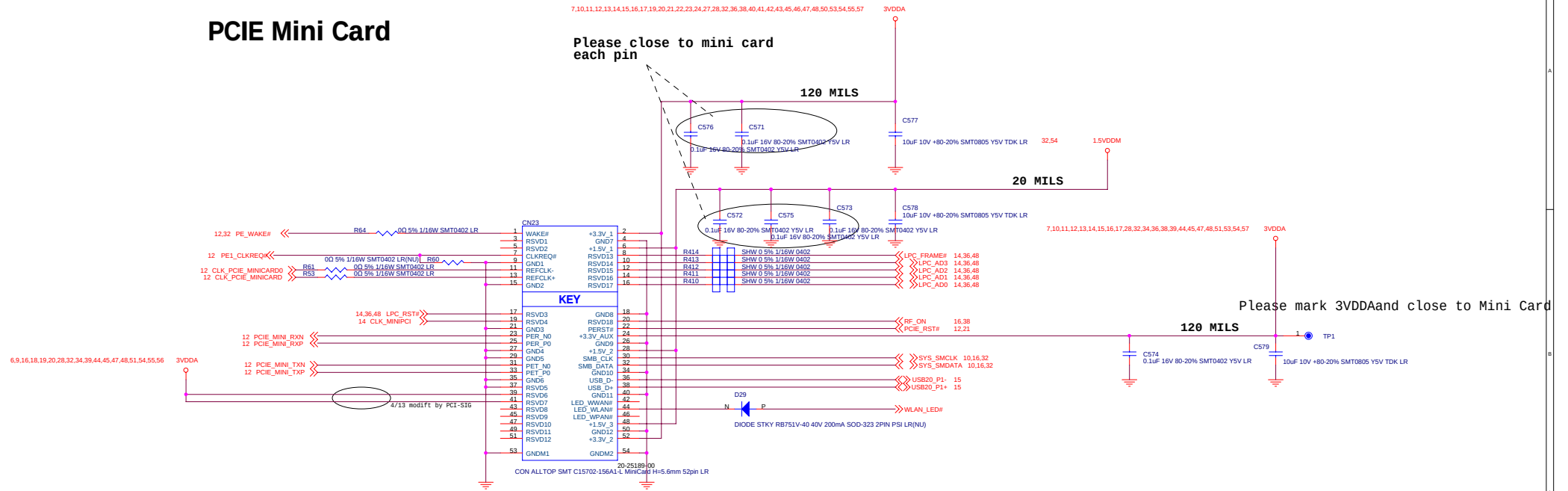
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PCIE Mini Card

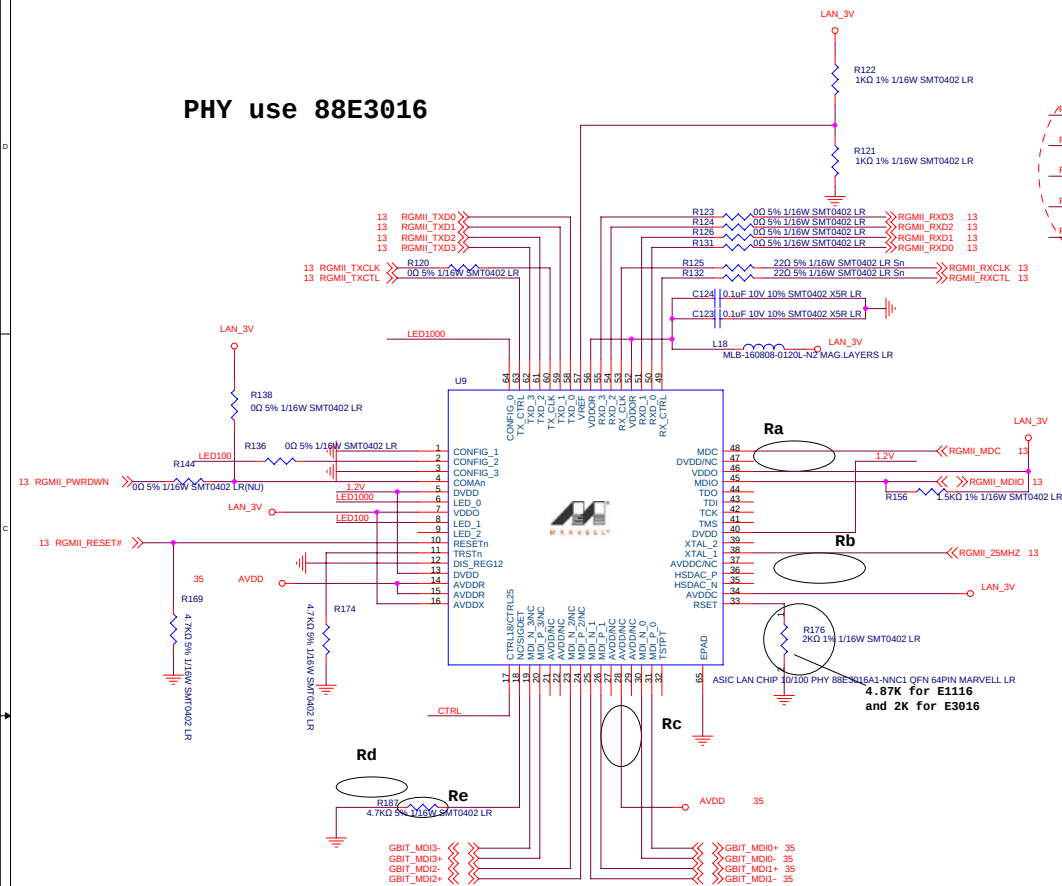
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,36,38,40,41,42,43,45,46,47,48,50,53,54,55,57

Please close to mini card
each pin



Please mark 3VDDA and close to Mini Card

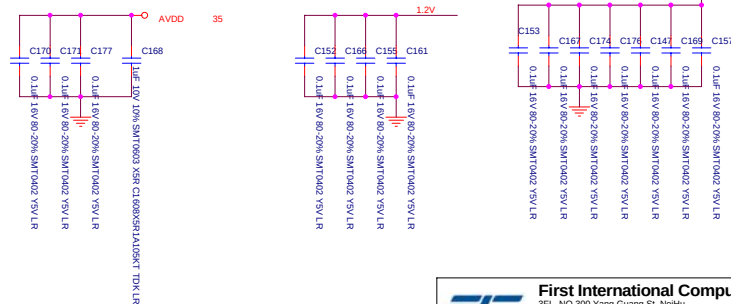
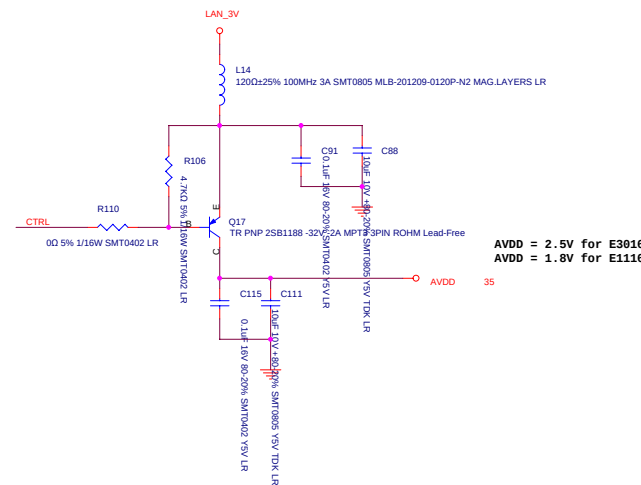
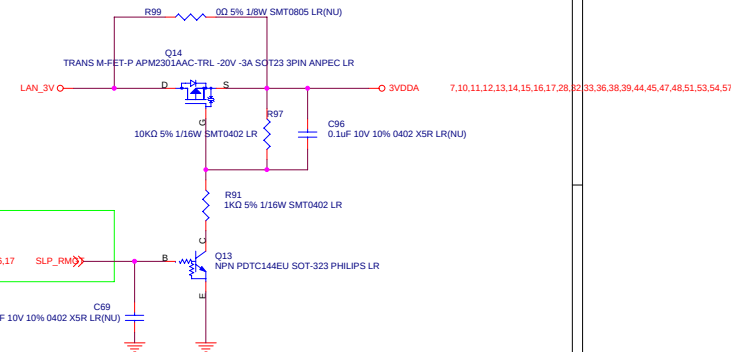
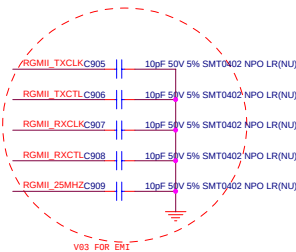
PHY use 88E3016



	for 88E3016	for 88E1116
Ra	NU	STUFF
Rb	NU	STUFF
Rc	STUFF	NU
Rd	NU	STUFF
Re	STUFF	NU

Layout Guide

- The Lan Chip should be placed as close as possible to the transfer.
- The resistor connected to RSET pin should be placed near to the Lan Chip, and away from signal traces(ex:MDIO+/-) and clock signals as far as possible.
- The transfer should be placed as close as possible to the RJ45 connector.
- The crystal should be placed far away from I/O ports and high frequency signal.
- The termination resistors and capacitors should be placed closely to the Lan Chip.
- The decoupling capacitors should be placed as close as possible to the power pins, such that the distance from IC power pin to the capacitor is within 200mils.
- Traces routed from the Lan Chip to the transfer, and to the RJ45 connector should be as short as possible.
- The 10-12cm maximum length between Lan chip and transfer is achievable only when there's no interferences around.
- All 4 pairs of the differential resistor(49.9k) must close to Lan Chip, and make them(4pairs) as same as distant.
- PLACE GND PLANE AS LARGE AS POSSIBLE
- If power pins are next to each other and there is not much room to accommodate multiple capacitors, then the power pins can share the same capacitors.
- It's important to separate digital signals from analog signals. If it is unavoidable to cross digital signals with analog power do it at 90 degree angle.
- The digital power plane should be separated from analog areas.
- All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.
- The Lan Chip pin 1 facing the transformer, then you can make the signal shorter.



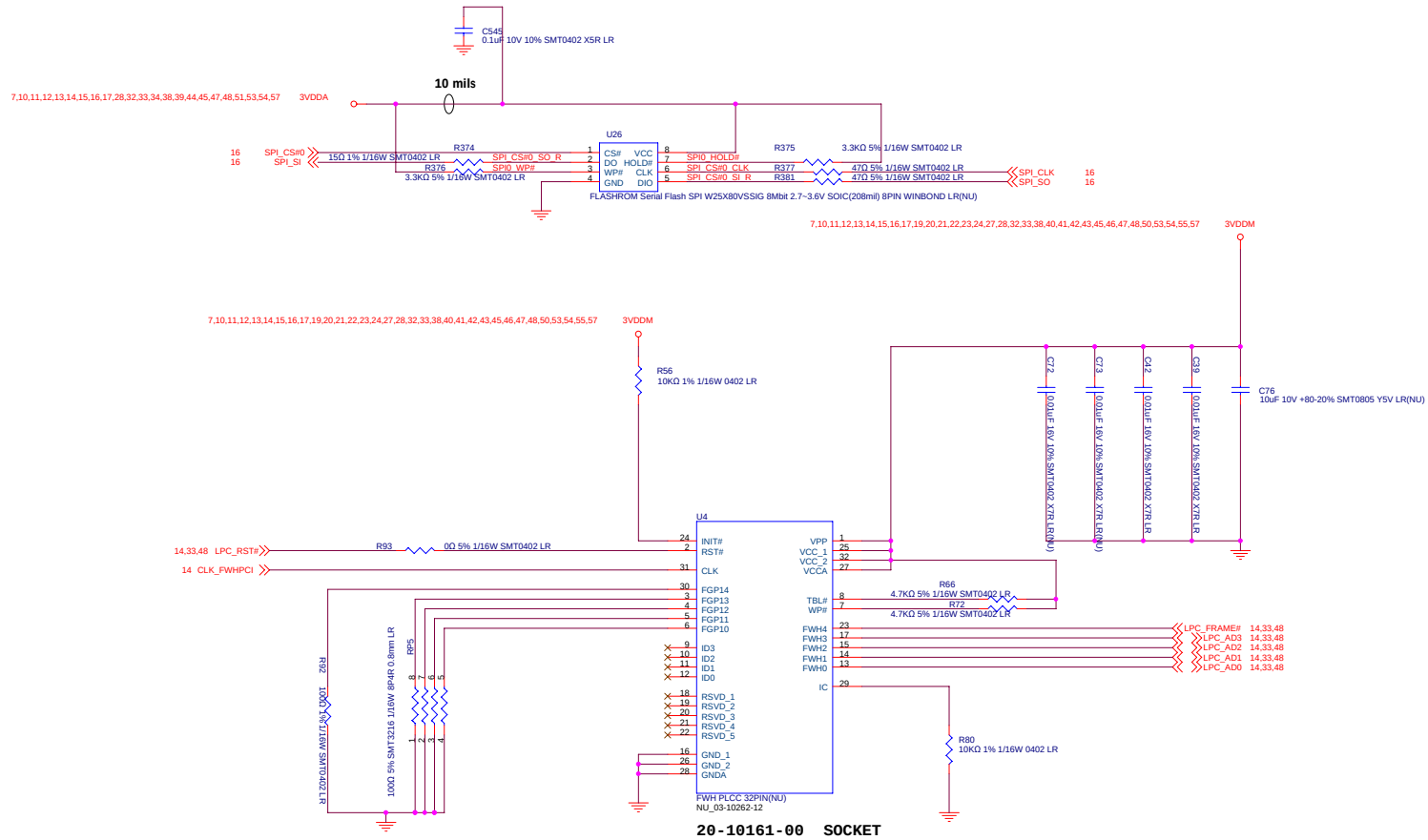
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C	10/100M PHY 88E3016		
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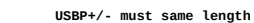
The diagram illustrates a transformer setup with two distinct ground planes. On the left, a vertical stack of components is shown: a top GND plane, followed by TX+ and TX- lines with a spacing of 'LESS THAN 0.1"', then a middle GND plane, followed by RX+ and RX- lines with a spacing of 'LESS THAN 0.1"', and finally a bottom GND plane. This stack is labeled 'GND PLANE' at the bottom. In the center is a vertical rectangle labeled 'Transformer'. To the right of the transformer is another vertical stack of components: an R component, followed by J, 4, and 5. This stack is labeled 'Isolated GND' at the bottom. The entire diagram is enclosed in a dashed rectangular border.



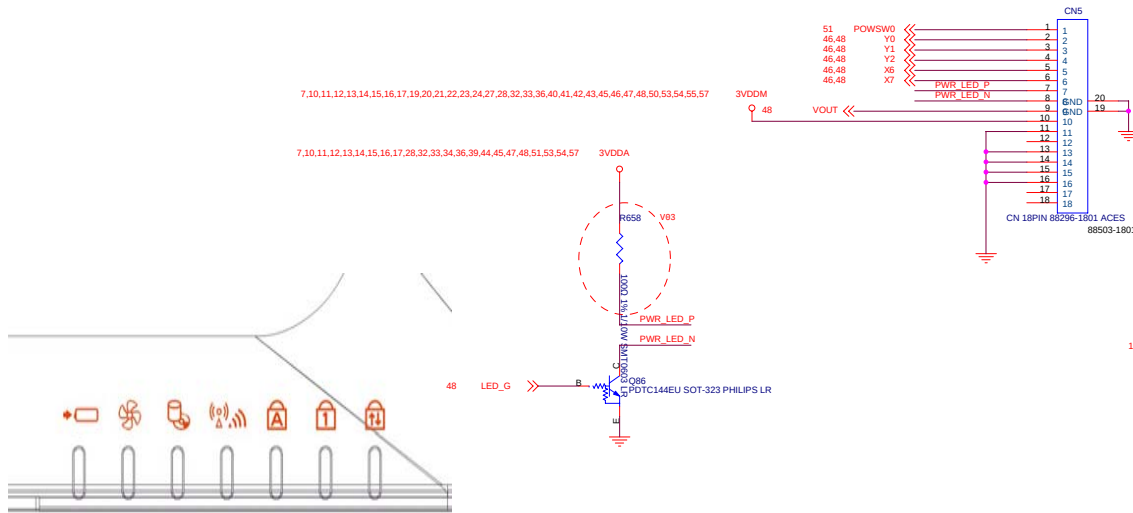
SPI Interface



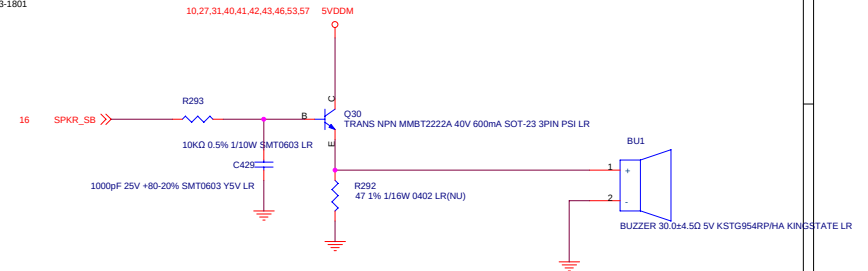
03-10262-12 Flash ROM PM49FL004TL-33JCE
4Mbit(512K*8) PMC LR



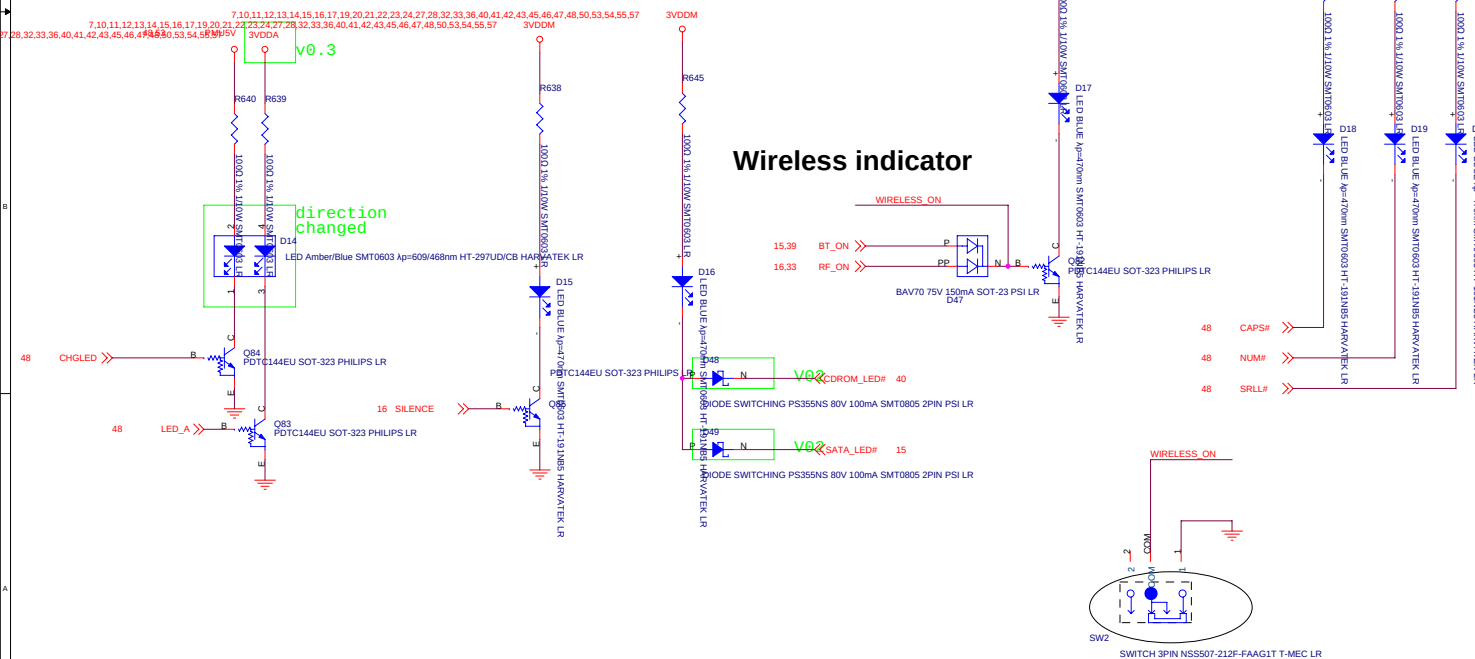
LED indicator control logic



BUZZR



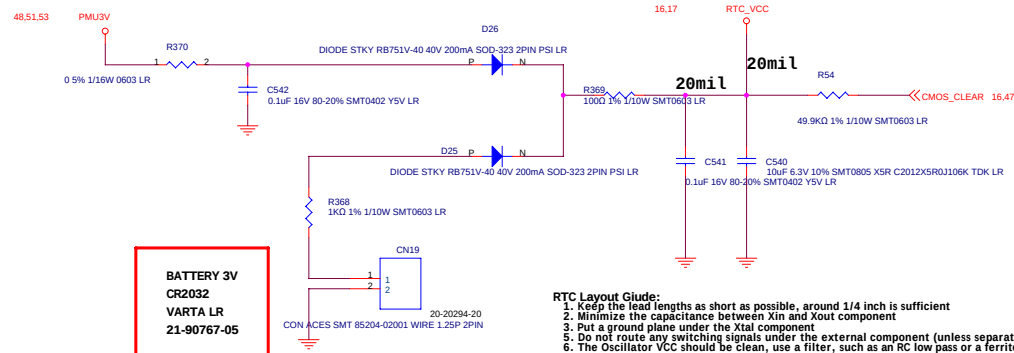
Wireless indicator



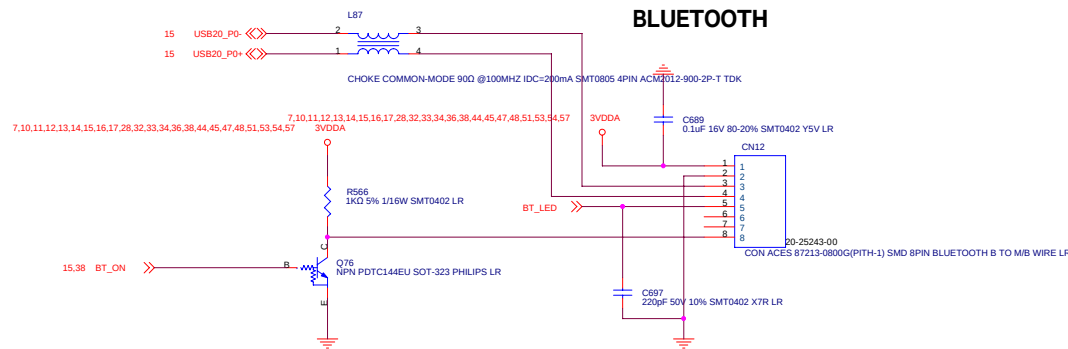
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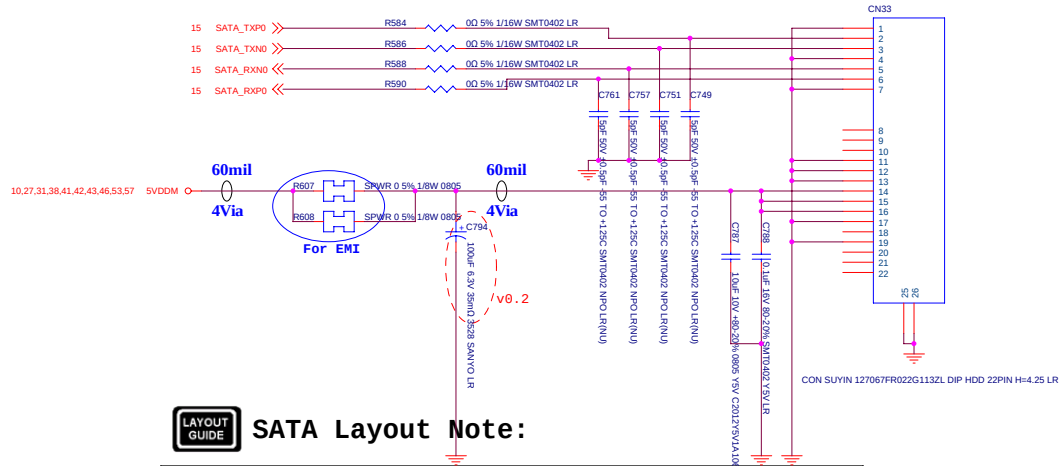
RTC Discharge Circuit



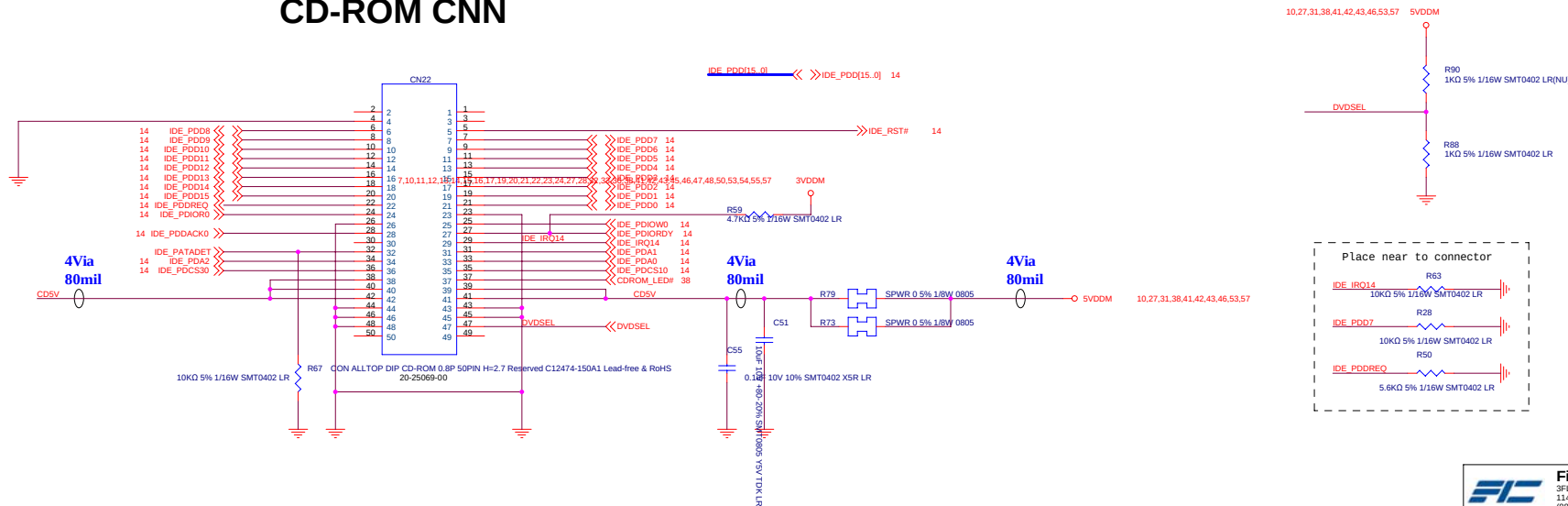
BLUETOOTH



HDD I/F



CD-ROM CNN



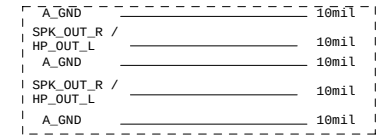
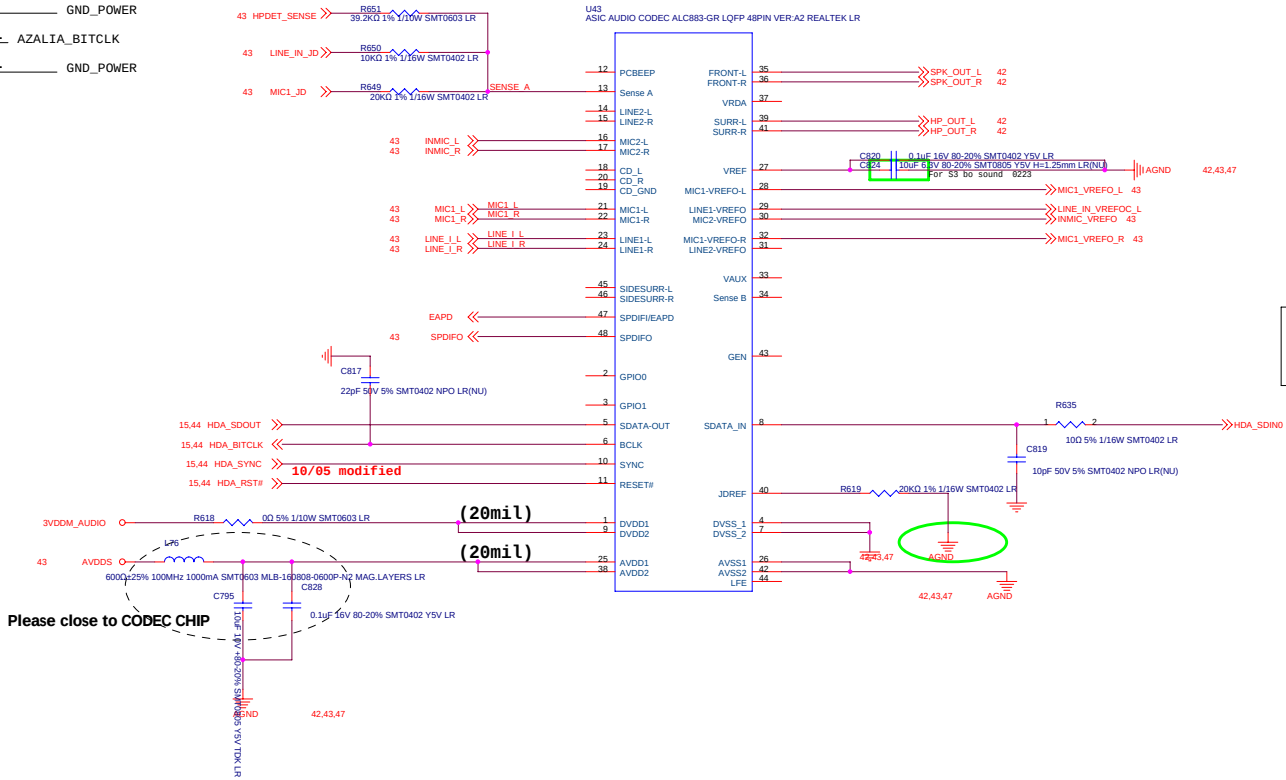
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(886-2)8751-8751

File	PTT50 (FIC)	Rev	0.1
Size	Document Number		
C	SATA HD / CD-ROM CNN		
Date	Monday, June 04, 2007	Sheet	40 of 57

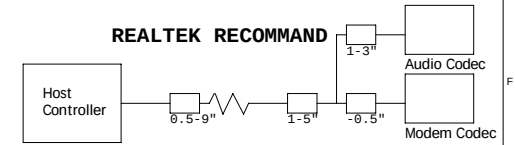
10mil _____ GND_POWER
 10mil _____ 10mil AZALIA_PCBEEP
 10mil _____ 10mil GND_POWER
 10mil _____ GND_POWER
 10mil _____ 10mil AZALIA_BITCLK
 10mil _____ 10mil GND_POWER

Layout guide :

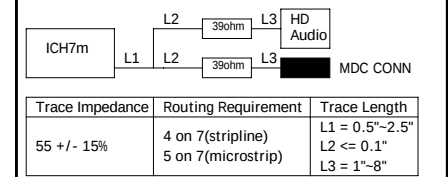
1. Close to codec.
2. Realtek suggested that layout trace of the sense pin should away form any analog trace because sensing current might distorts the audio performance (The bottom lay is best choice).



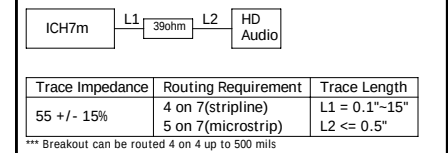
REALTEK RECOMMAND



HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#



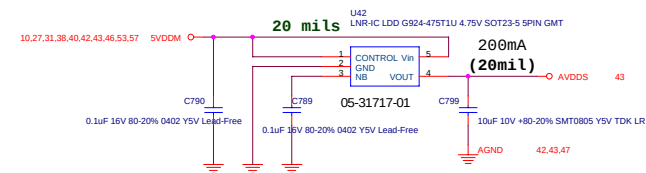
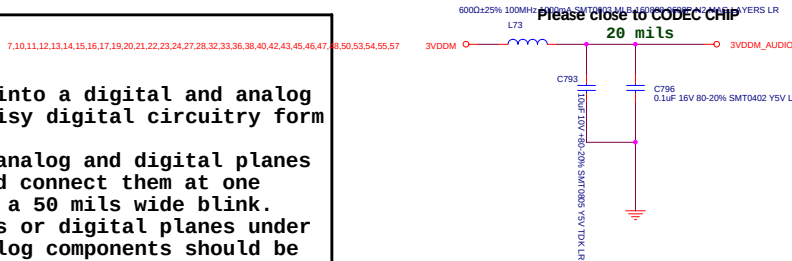
HD Audio-ACZ_SDIN

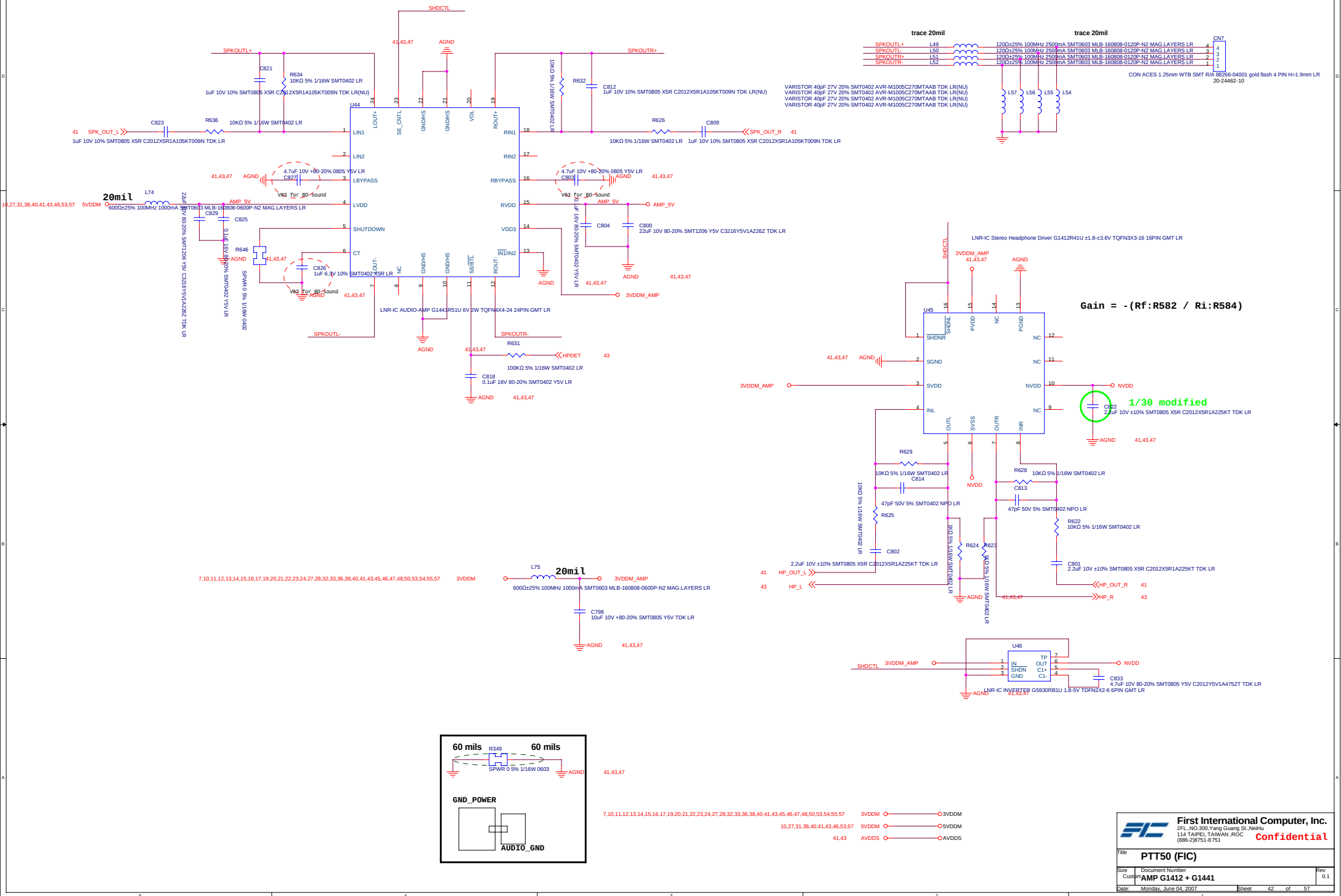


AZALIA CODEC POWER

Layout guide :

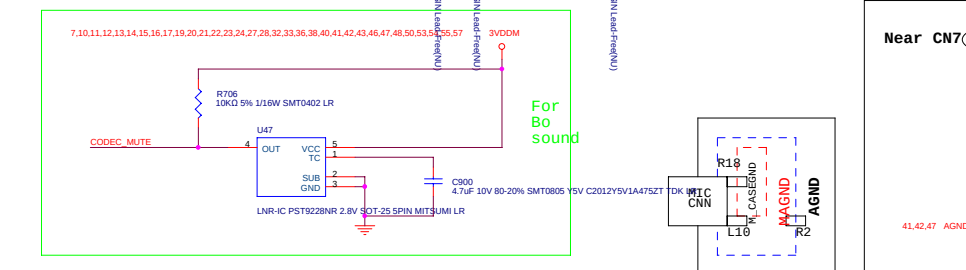
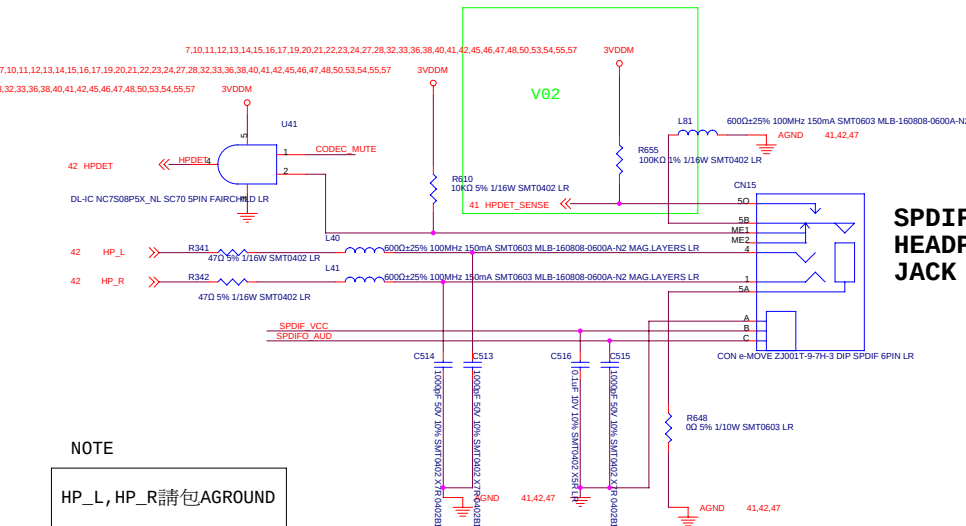
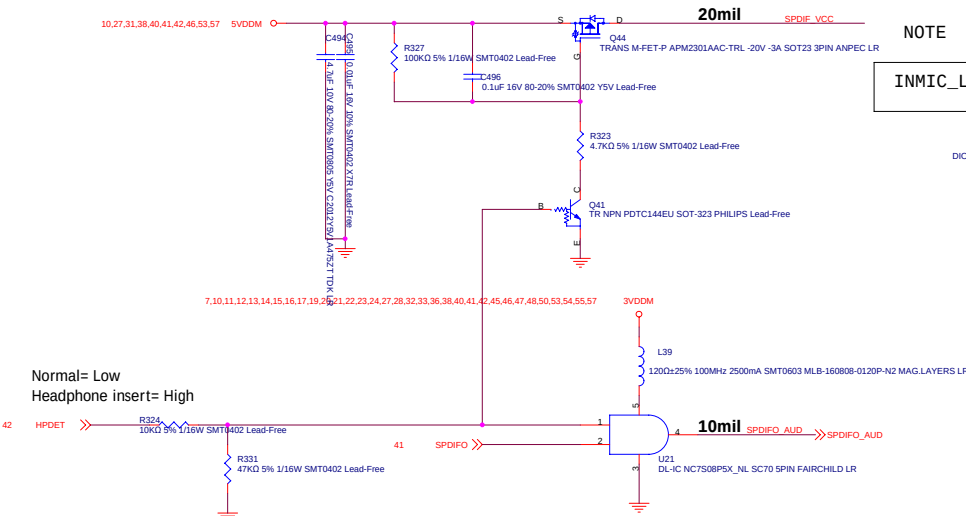
1. The codec is partitioned into a digital and analog sections to help isolated noisy digital circuitry form quiet analog circuitry.
2. The layout separates the analog and digital planes with a 60 to 100 mils gap and connect them at one point beneath the codec with a 50 mils wide blink.
3. Never route digital traces or digital planes under the analog ground areas. Analog components should be located over analog planes (ground and power planes) and digital components should be located over digital planes.





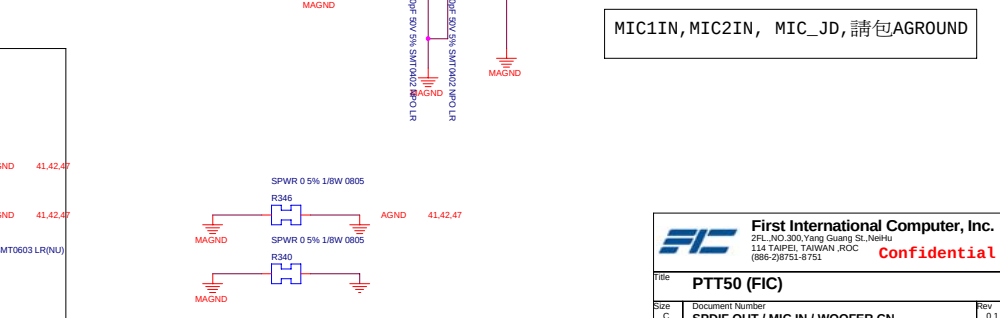
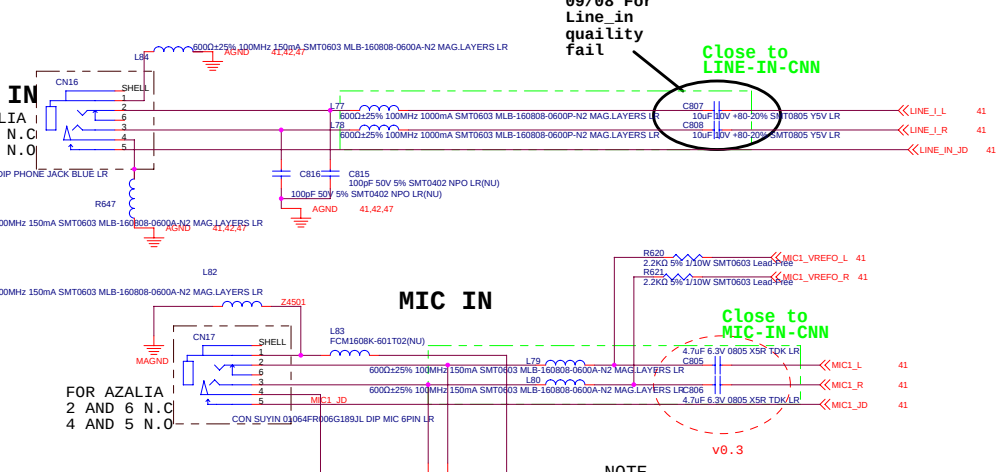
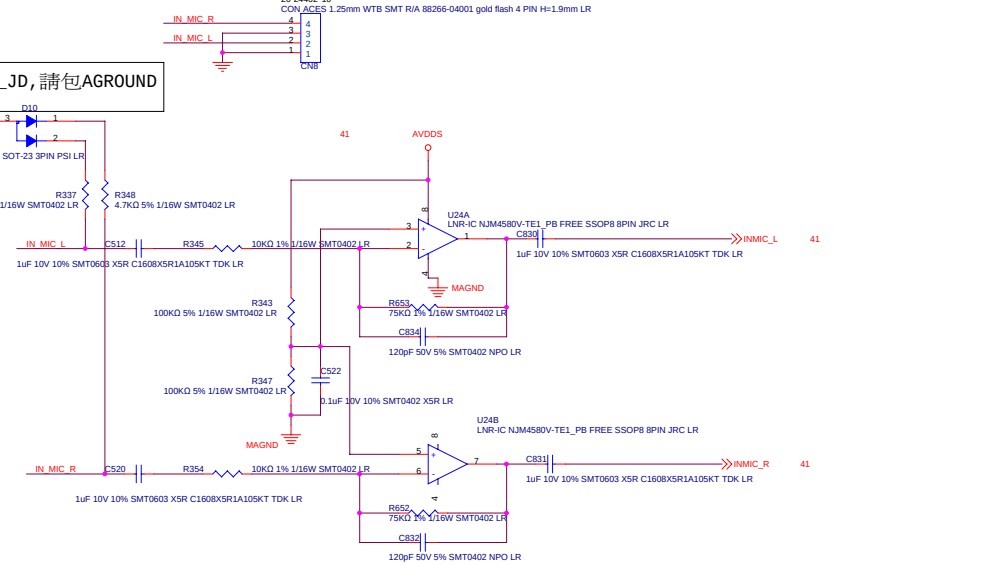
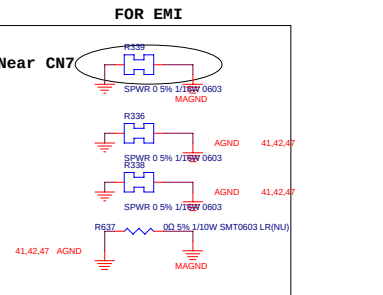
S/PDIF Power

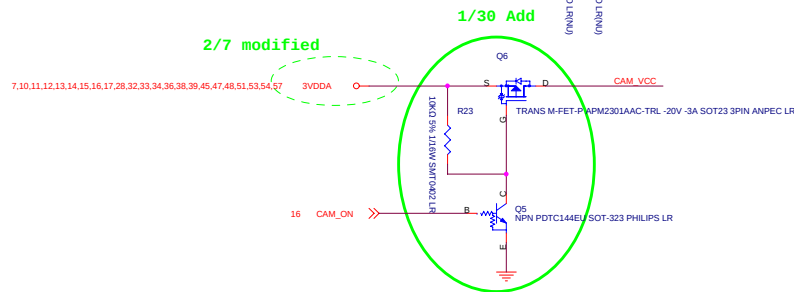
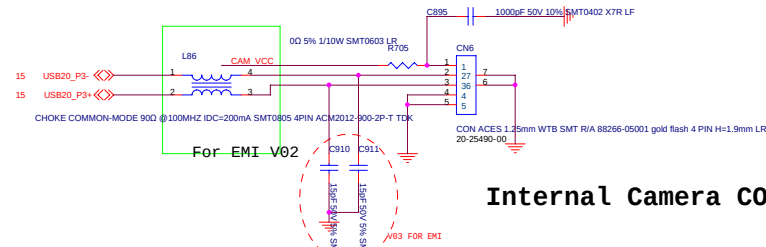
Internal array MIC



NOTE
INMIC_L, INMIC_R, MIC_JD, 請包AGROUND

SPDIF & HEADPHONE JACK





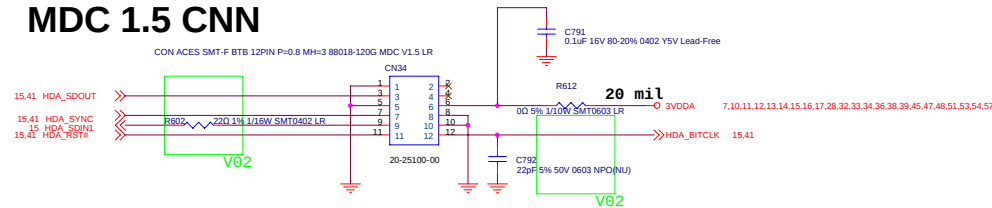
HD Audio-ACZ_SDIN (MDC Connector)



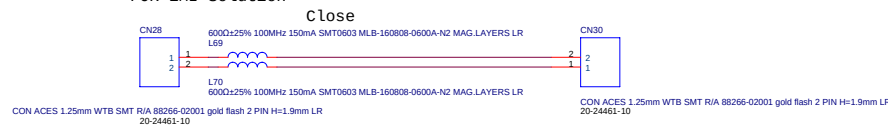
Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline)	L1 = 0.1"~15" L2 = 0.5"~1.5" L3 = 0.5"

*** Breakout can be routed 4 on 4 up to 400 mils

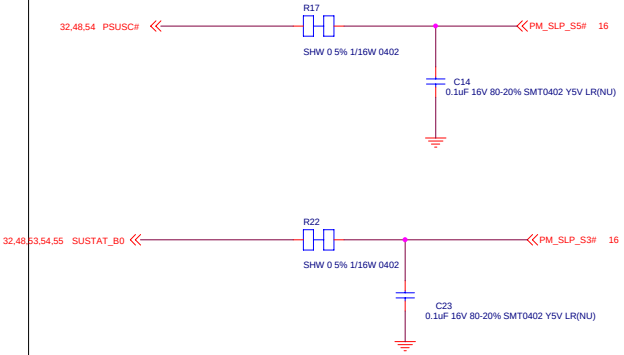
MDC 1.5 CNN



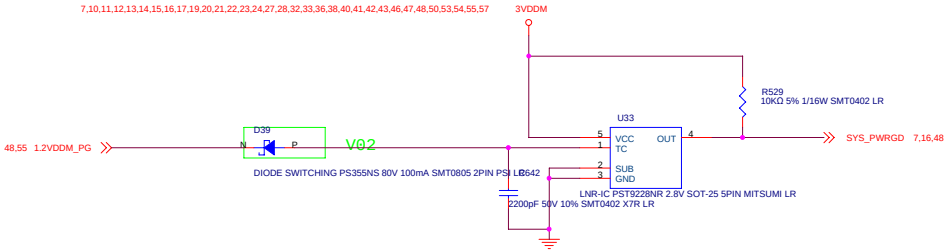
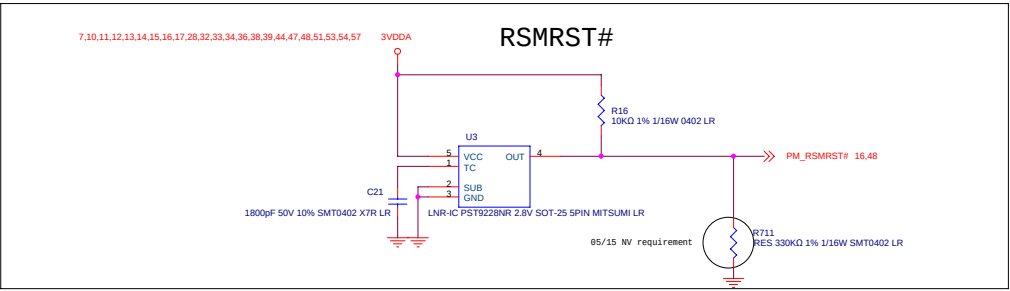
FOR EMI Solution



SUSPEND B & C

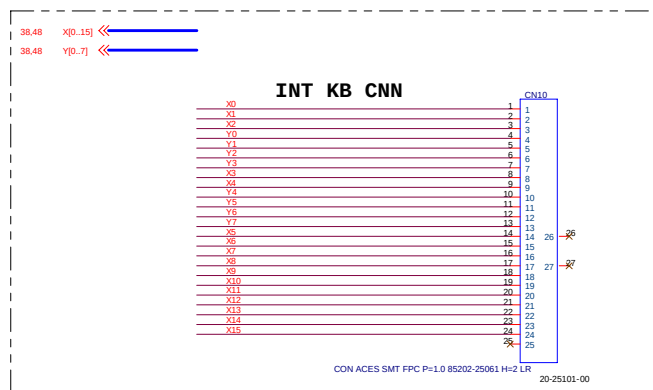
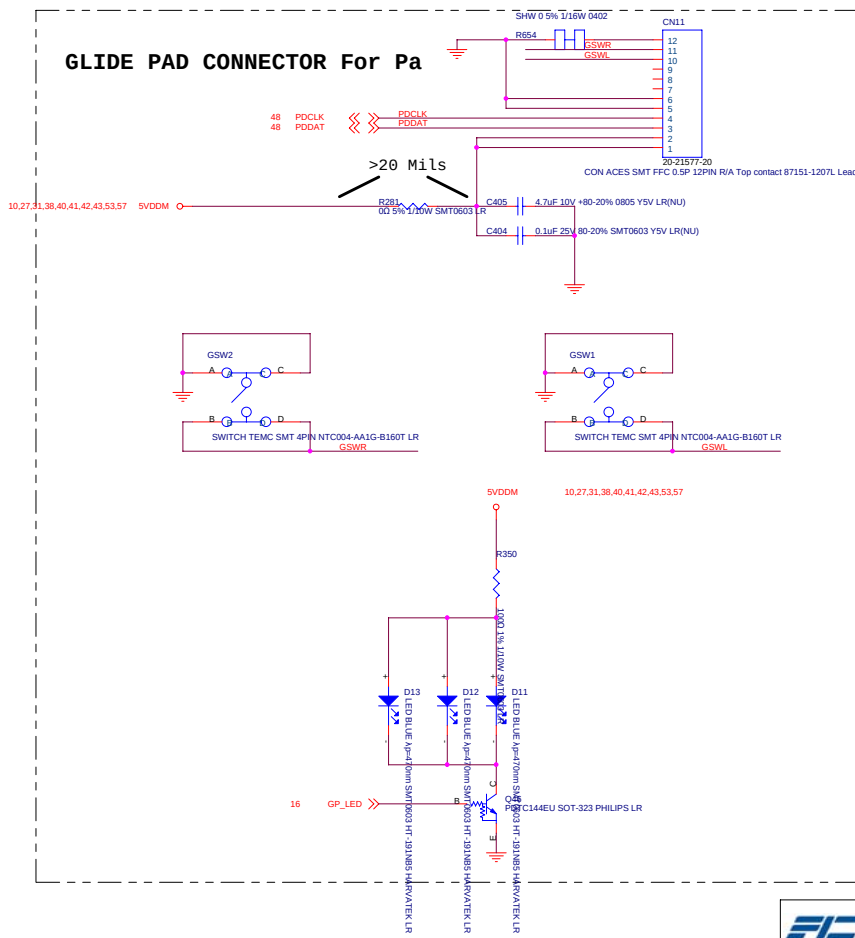
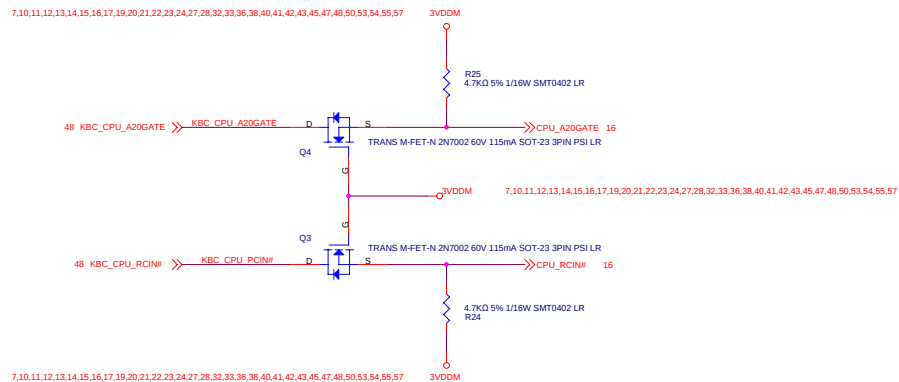


RESUME RESET

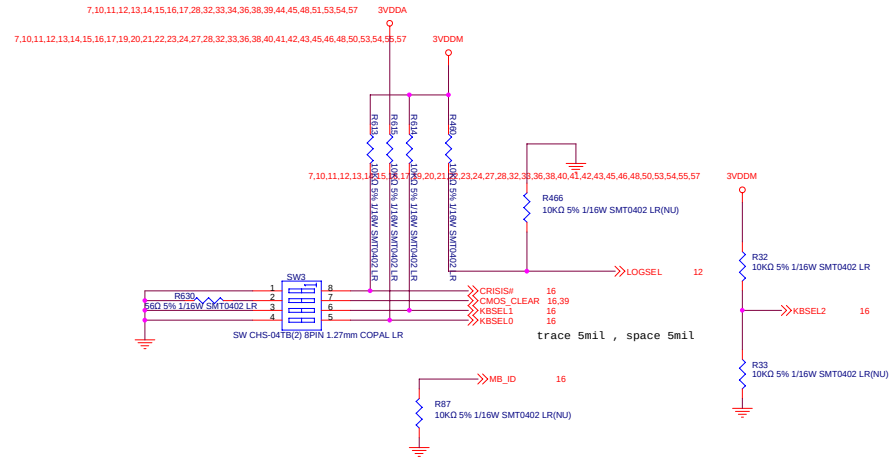


FIC First International Computer, Inc.
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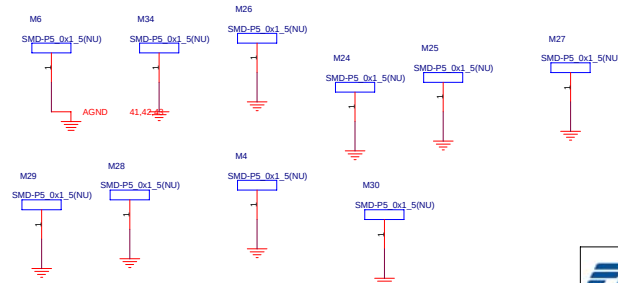
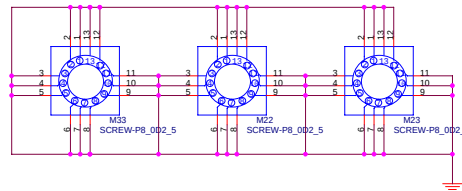
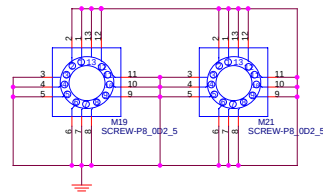
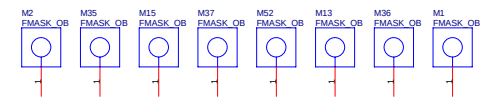
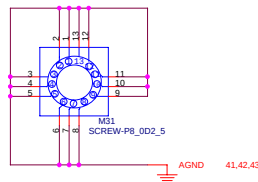
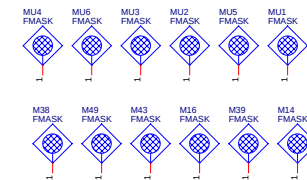
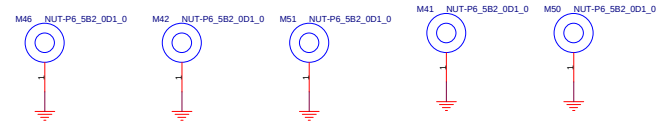
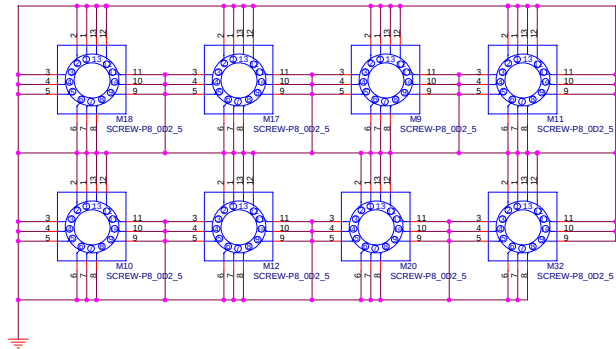
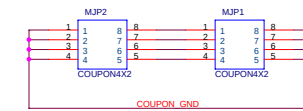
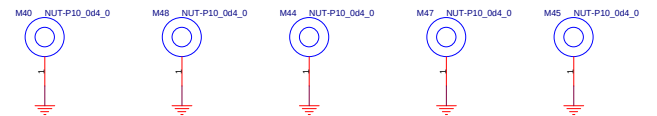
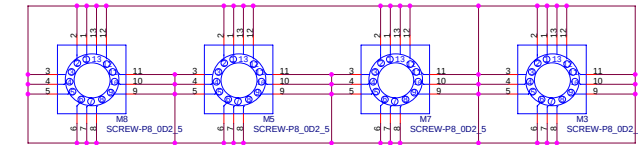
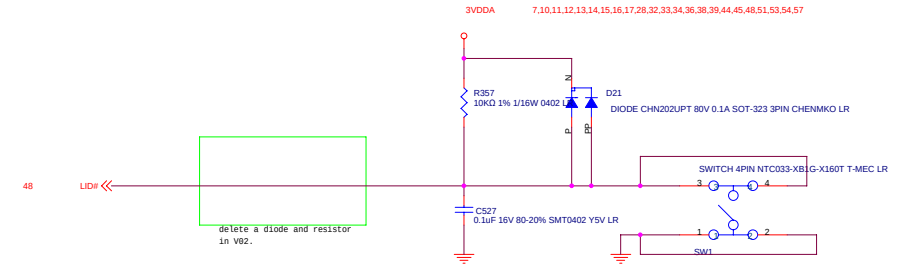
File	PTT50 (FIC)	
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C	Reset Circuit	0.1
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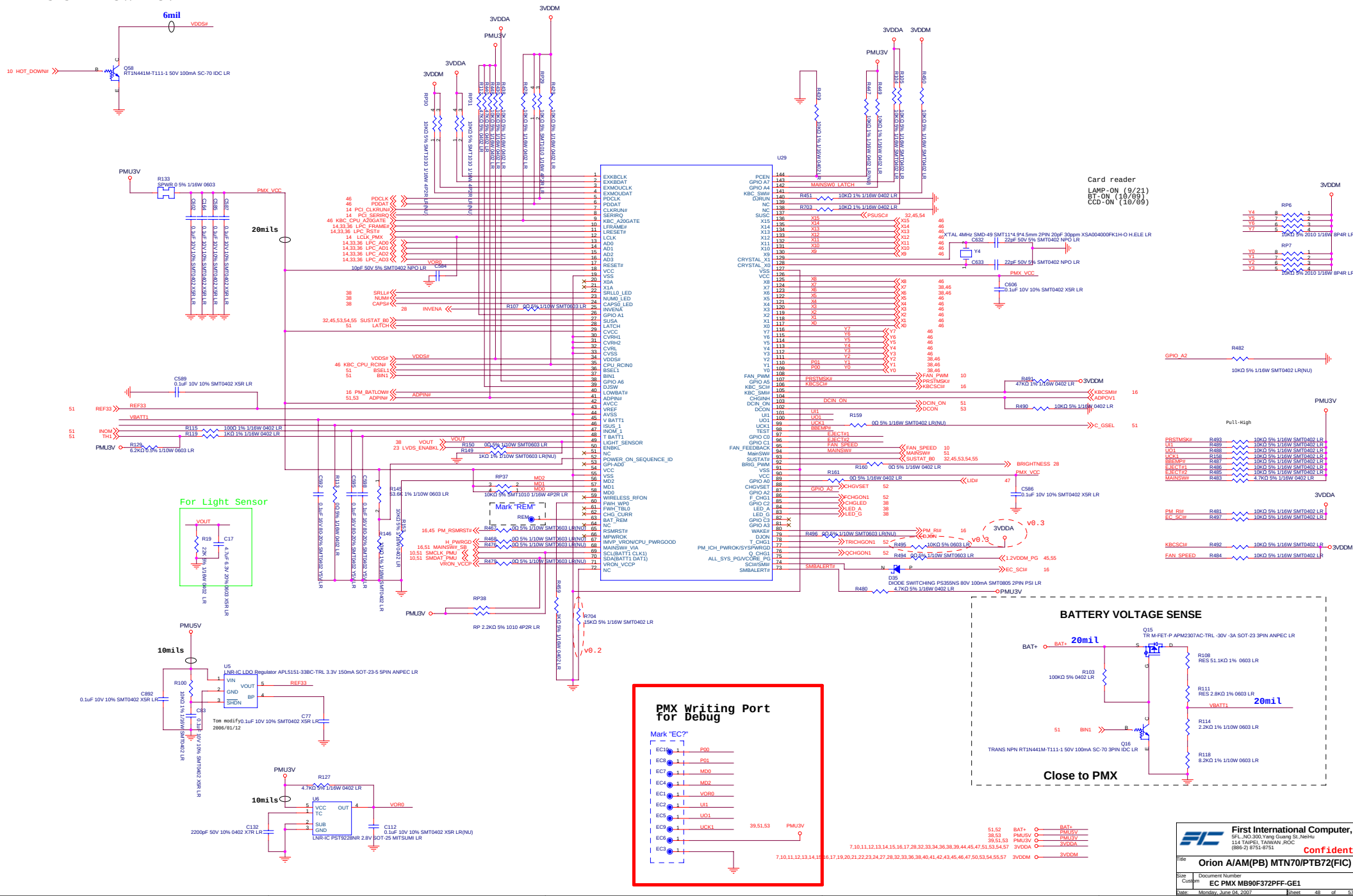
DIP SWITCH



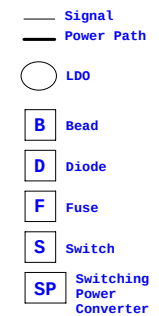
LID Switch



SYSTEM POWER OVP

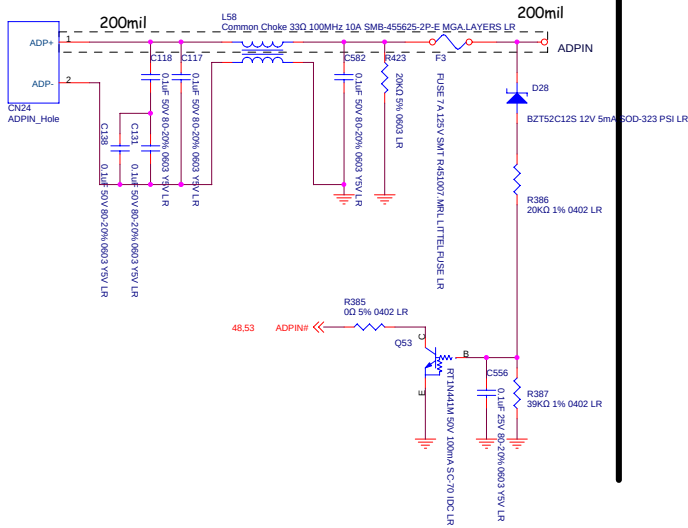


The schematic diagram illustrates the power management system for the APL5331. It shows the power flow from an Adapter Jack and Battery through various regulators and switches to the APL5331 and other components. Key components include the MAX8734A (Internal LDO), MB3887, MM1380A, MAX8774, and various capacitors and inductors. The APL5331 is configured to regulate the 5VDDM, 3VDDM, 1.2VDDA, 1.8VDDM, and 1.5VDDM rails. The diagram also shows the connection of the APL5331 to the APL5151, PST9228, and other components.

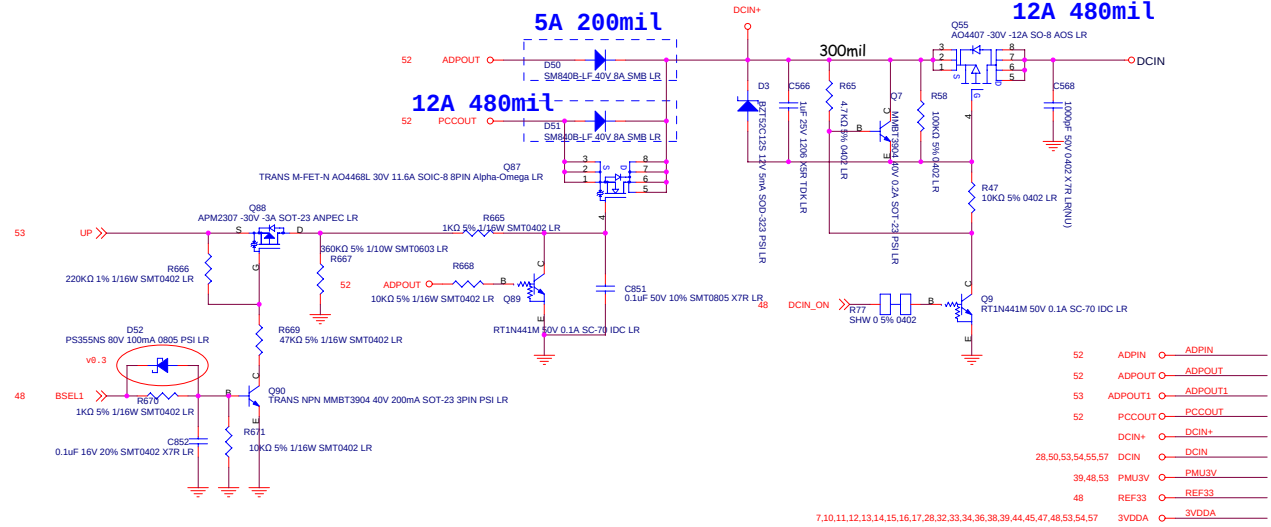


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Title					
PTT50					
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		CPU CORE (MAX8774)			0.1
Date:	Monday, June 04, 2007		Sheet	50	of 57

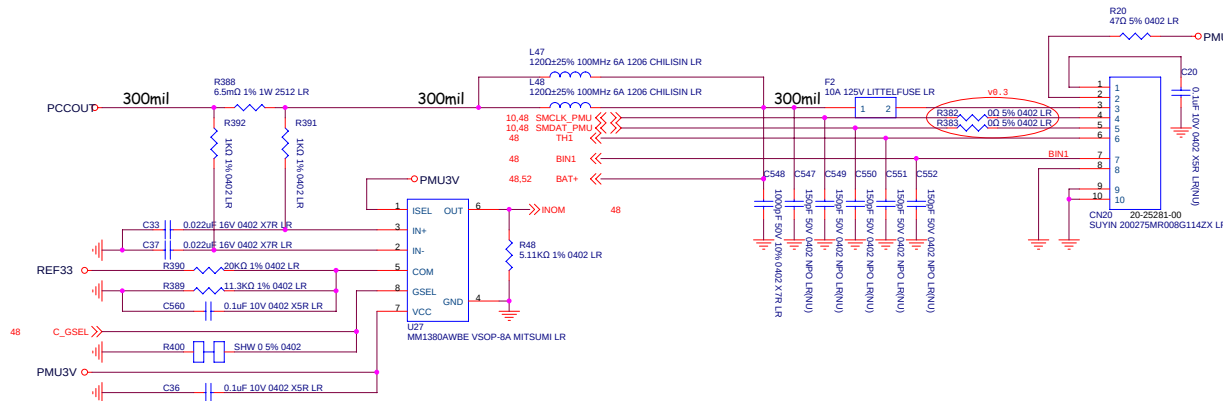
ADPIN



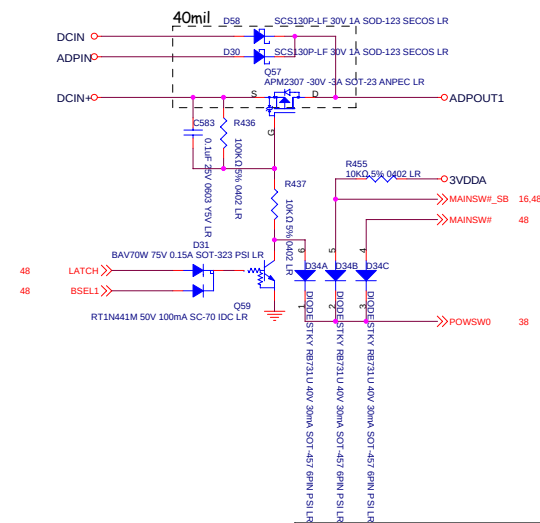
DCIN+ to DCIN



BATIN

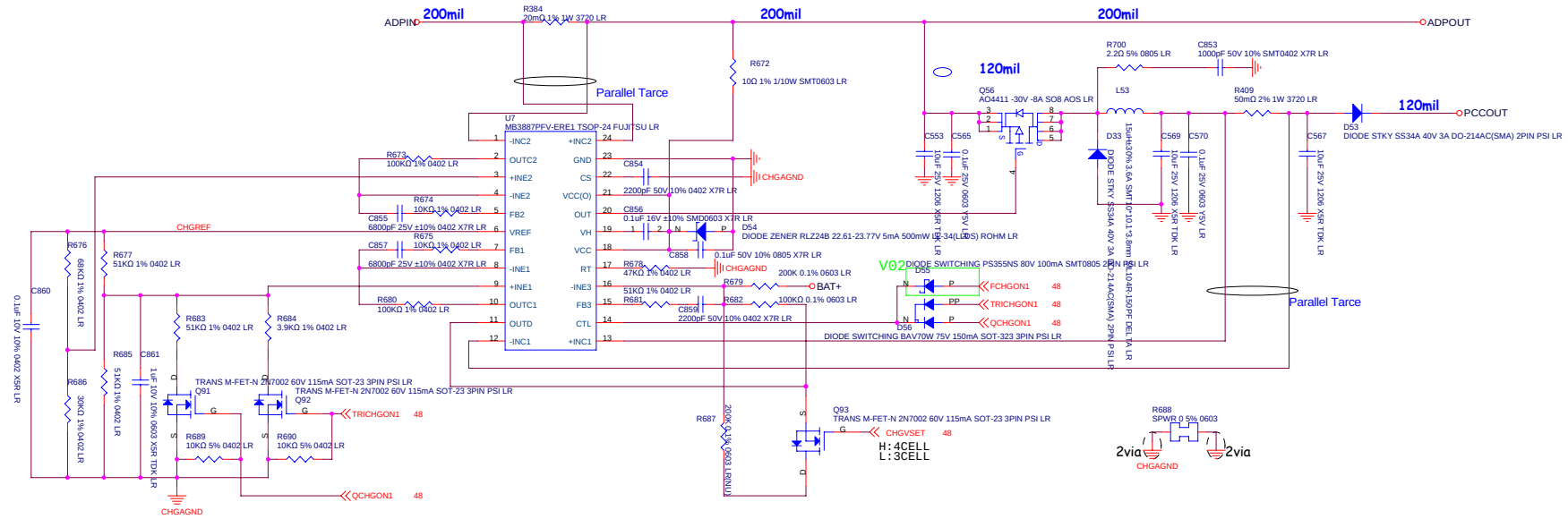


ADPOUT1



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Charger



Total PWR =
85.52W(20V)

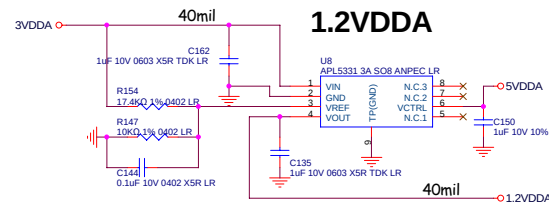
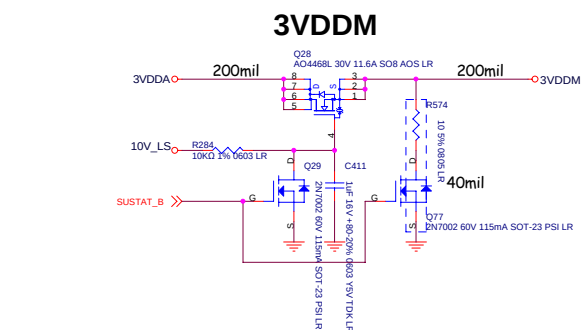
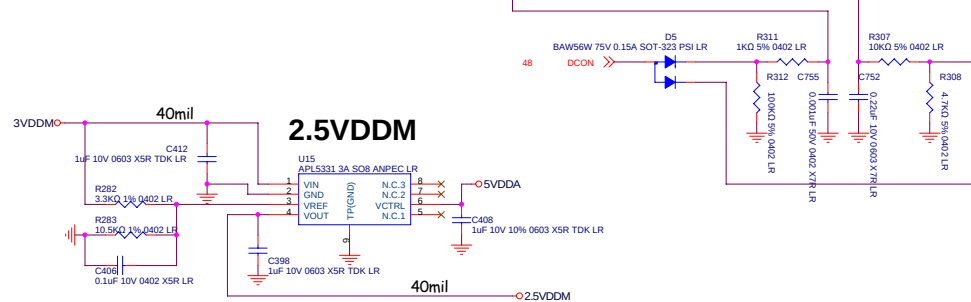
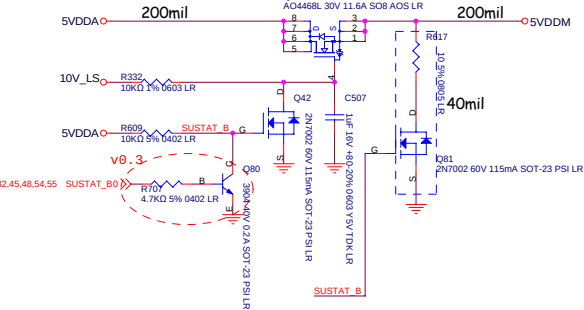
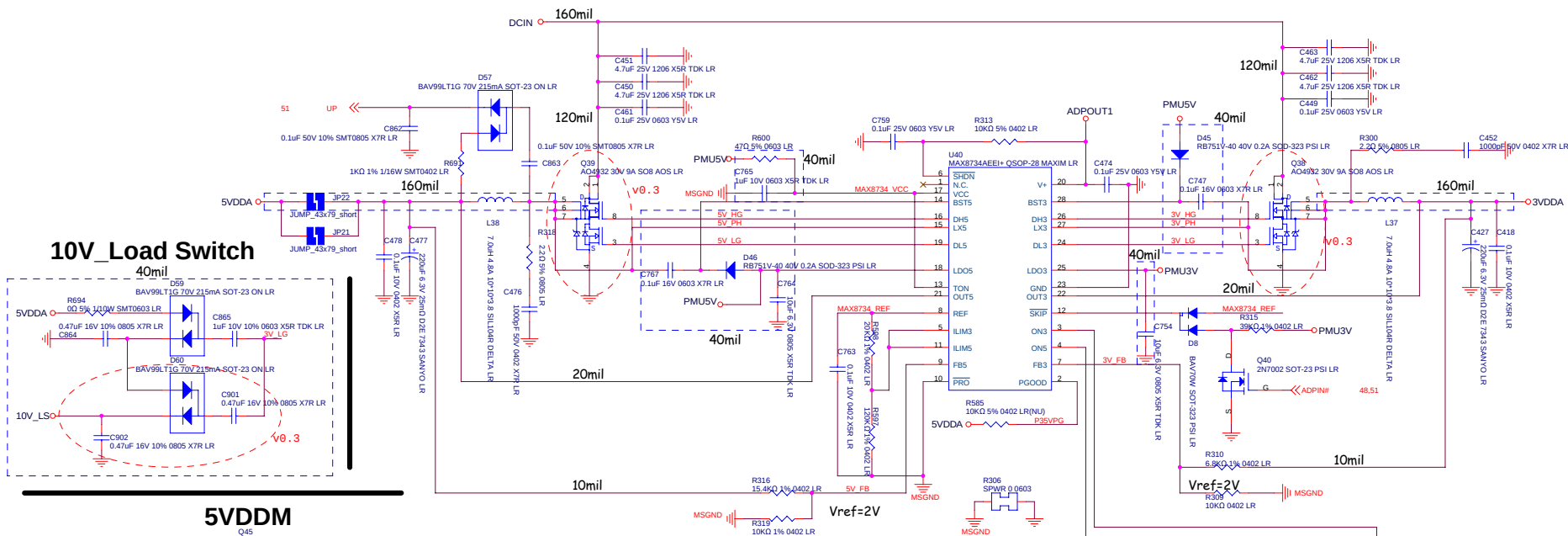
FCHG = 2.5A
QCHG = 1.67A
TCHG = 0.311A

51 ADPOUT ○ ADPOUT
51 ADPIN ○ ADPIN
51 PCCOUT ○ PCCOUT
48.51 BAT+ ○ BAT+

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Size C Document Number Rev
PCHG 0.2
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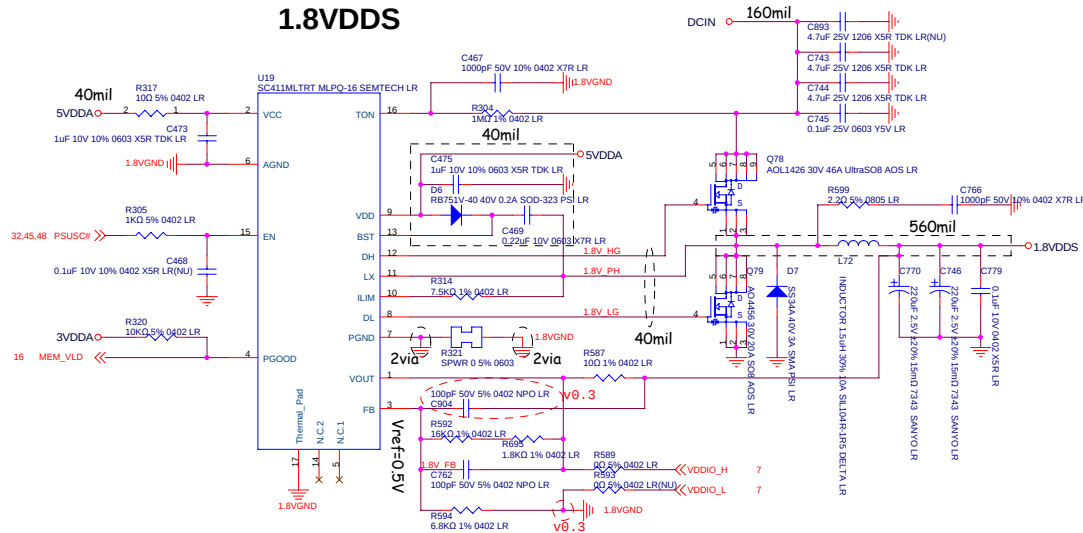
PMU5V/3V, 5VDDA/S/M, 3VDDA/S/M, 1.2VDDA, 2.5VDDM



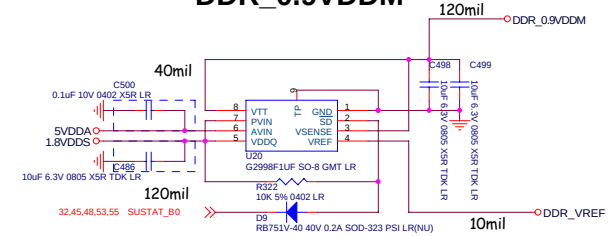
	51	ADPOUT1	ADPOUT1
	28,50,51,54,55,57	DCIN	DCIN
	54,55	10V_LS	10V_LS
	38,48	PMU5V	PMU5V
	39,49,51	PMU3V	PMU3V
	37,50,54,55,57	SVDDA	SVDDA
7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,54,57	37,50,54,55,57	3VDDA	3VDDA
	17	1,2VDDA	1,2VDDA
	10,27,31,38,40,41,42,43,46,57	5VDDM	5VDDM
9,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,54,55,57	37,50,54,55,57	3VDDM	3VDDM
	5,57	2,5VDDM	2,5VDDM

1.8VDDS/M, 0.9VDDM, 1.5VDDM

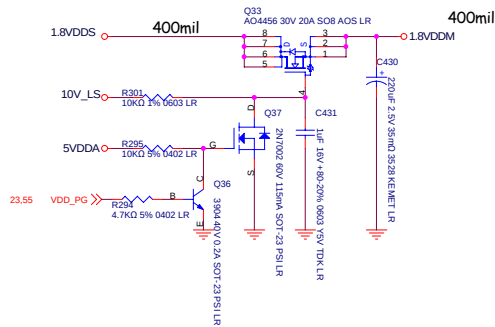
1.8VDDS



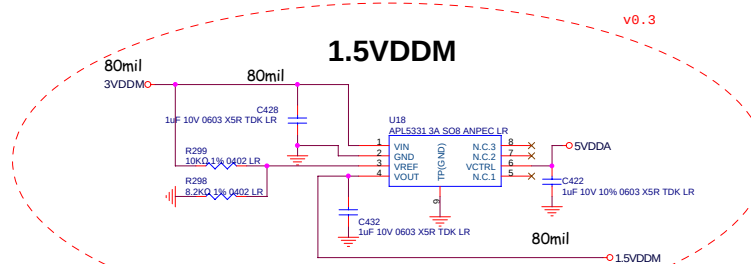
DDR_0.9VDDM



1.8VDDM



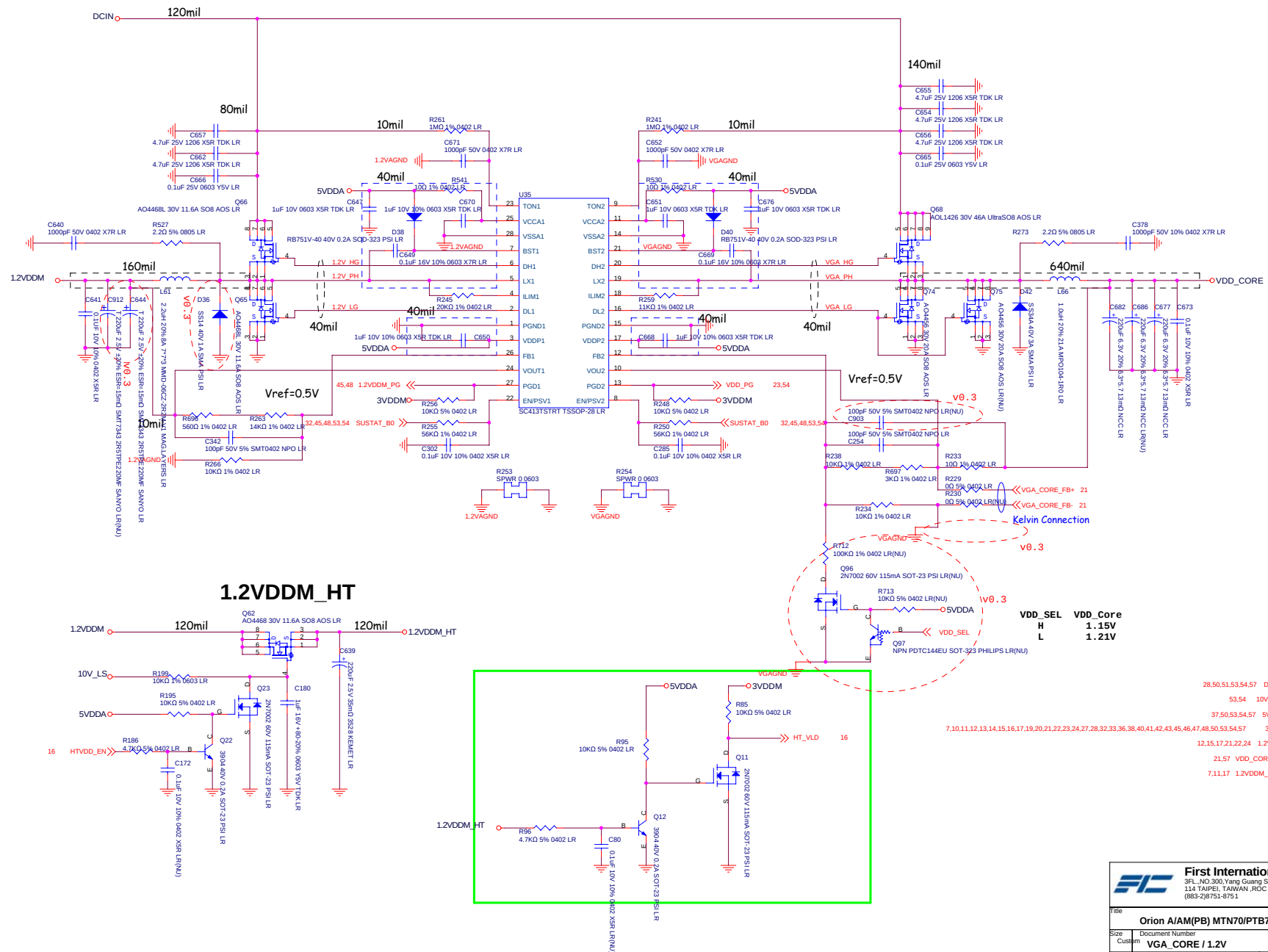
1.5VDDM



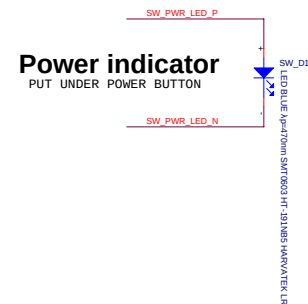
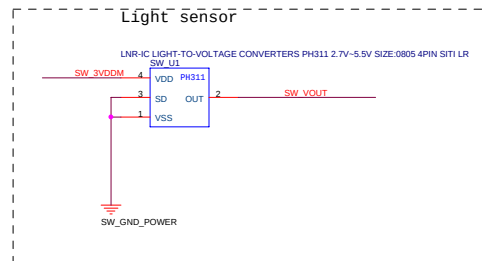
26,50,51,53,55,57	DCIN	DCIN
53,55	10V_LS	10V_LS
37,50,53,55,57	5VDDA	5VDDA
7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,53,57	3VDDA	3VDDA
7,8,9,19,20,50	1.8VDDS	1.8VDDS
8,19,20	DDR_0.9VDDM	DDR_0.9VDDM
20	DDR_VREF	DDR_VREF
13,23,24,25	1.8VDDM	1.8VDDM
VGADDR_0.9VDDM	VGADDR_0.9VDDM	VGADDR_0.9VDDM
VGADDR_VREF	VGADDR_VREF	VGADDR_VREF
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,55,57	3VDDM	3VDDM
32,33	1.5VDDM	1.5VDDM

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File	Orion A/JAM(PB) MTN70/PTB72(FIC)	Rev	0.1
Size	Document Number	Rev	0.1
C	DDR11 Power / 1.8VDDM	Rev	0.1
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Switch Board



WEBCAM SW

SW_X6

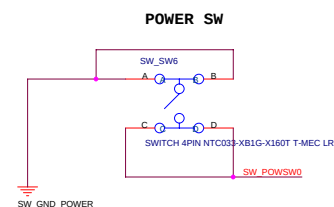
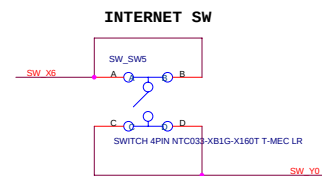
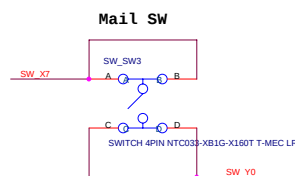
SW_SW1

A B

C D

SWITCH 4PIN NTC033-XB1G-X160T T-MEC LR

SW_Y2



POSITION	SEQUENCE
1	5'-GAG-3'
2	5'-GAG-3'
3	5'-GAG-3'
4	5'-GAG-3'
5	5'-GAG-3'
6	5'-GAG-3'
7	5'-GAG-3'
8	5'-GAG-3'
9	5'-GAG-3'
10	5'-GAG-3'
11	5'-GAG-3'
12	5'-GAG-3'
13	5'-GAG-3'
14	5'-GAG-3'
15	5'-GAG-3'
16	5'-GAG-3'
17	5'-GAG-3'
18	5'-GAG-3'
19	5'-GAG-3'
20	5'-GAG-3'
21	5'-GAG-3'
22	5'-GAG-3'
23	5'-GAG-3'
24	5'-GAG-3'
25	5'-GAG-3'
26	5'-GAG-3'
27	5'-GAG-3'
28	5'-GAG-3'
29	5'-GAG-3'
30	5'-GAG-3'
31	5'-GAG-3'
32	5'-GAG-3'
33	5'-GAG-3'
34	5'-GAG-3'
35	5'-GAG-3'
36	5'-GAG-3'
37	5'-GAG-3'
38	5'-GAG-3'
39	5'-GAG-3'
40	5'-GAG-3'
41	5'-GAG-3'
42	5'-GAG-3'
43	5'-GAG-3'
44	5'-GAG-3'
45	5'-GAG-3'
46	5'-GAG-3'
47	5'-GAG-3'
48	5'-GAG-3'
49	5'-GAG-3'
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89	5'-GAG-3'
90	5'-GAG-3'
91	5'-GAG-3'
92	5'-GAG-3'
93	5'-GAG-3'
94	5'-GAG-3'
95	5'-GAG-3'
96	5'-GAG-3'
97	5'-GAG-3'
98	5'-GAG-3'
99	5'-GAG-3'
100	5'-GAG-3'

SW6

SW5

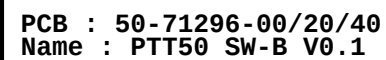
SW3

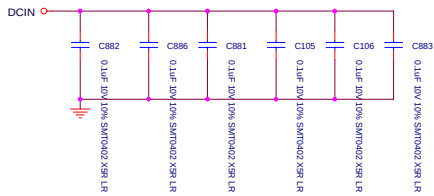
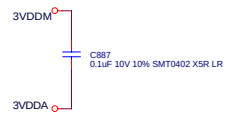
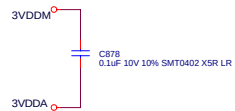
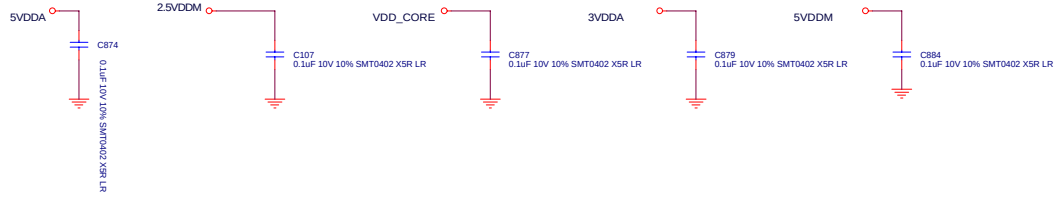
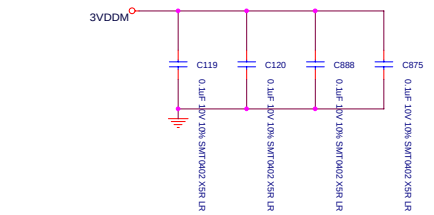
SW4

SW2

SW1

RIGHT





28,50,51,53,54,55	DCIN	DCIN
7,53	2.5VDDM	2.5VDDM
7,10,11,12,13,14,15,16,17,19,20,21,22,23,24,27,28,32,33,36,38,40,41,42,43,45,46,47,48,50,53,54,55	3VDDM	3VDDM
37,50,53,54,55	5VDDA	5VDDA
21,55	VDD_CORE	VDD_CORE
7,10,11,12,13,14,15,16,17,28,32,33,34,36,38,39,44,45,47,48,51,53,54	3VDDA	3VDDA
10,27,31,38,40,41,42,43,46,53	5VDDM	5VDDM