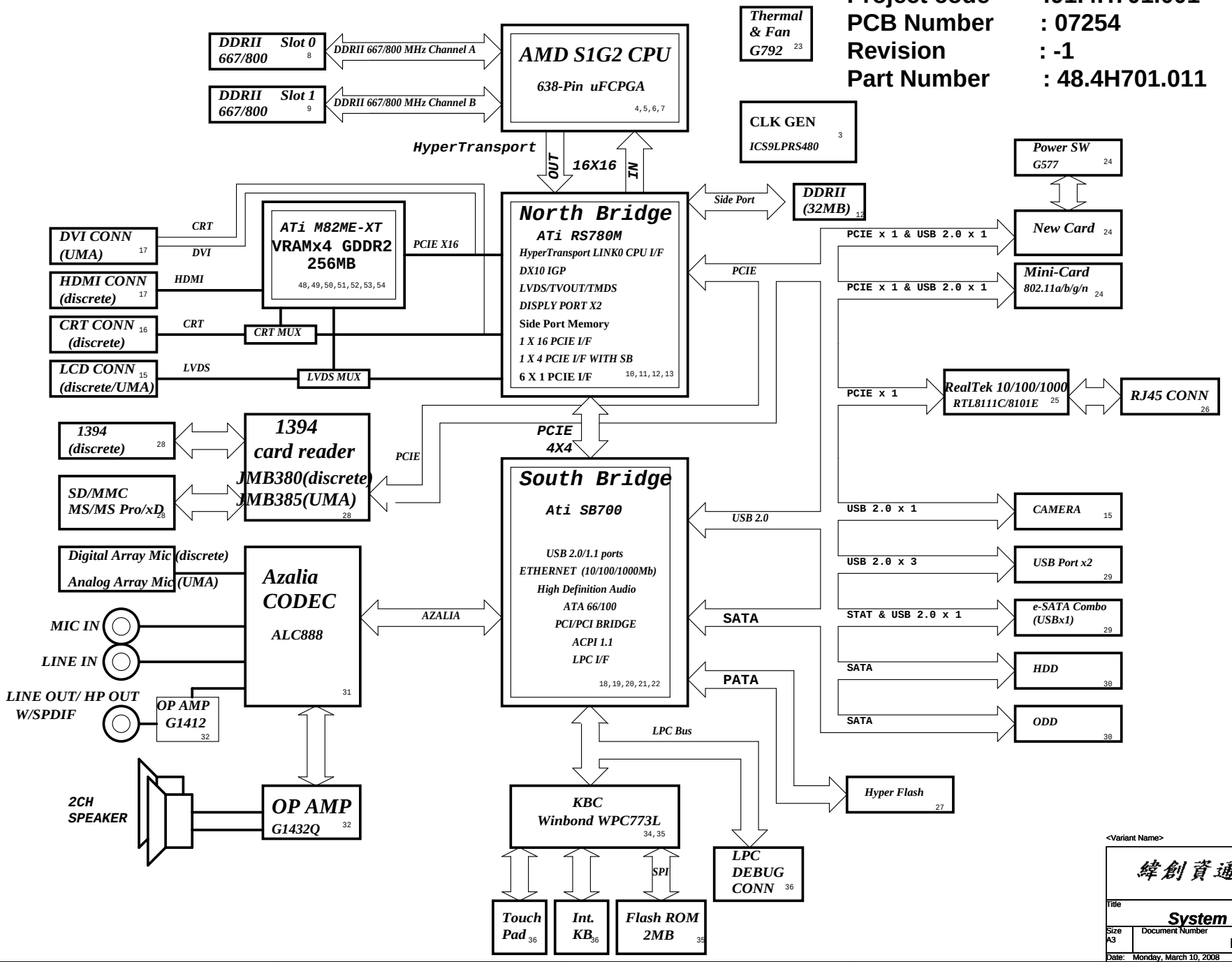
P1/P15 Block Diagram

Project code :91.4H701.001
PCB Number : 07254
Revision : -1
Part Number : 48.4H701.011



CPU V_CORE ISL6265 38,39	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51124 41	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC TPS51125 40	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC LDO 44	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC LDO 44	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC TPS51125 40	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER BQ24745 46	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***System Block Diagram***

Size	Document Number	Rev
A3	P1/P15	-1

Date: Monday, March 10, 2008 Sheet 1 of 56

SB700 Functional Strap Definitions

Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X

		USB PORT#	DESTINATION
SB700	2.0	0	Combo(ESATA/USB)
		1	USB1
		2	USB2
		3	CAMERA
		4	NC
		5	NEW CARD
		6	NC
		7	WLAN
		8	NC
		9	NC
		10	NC
		11	NC
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER &1394
Lane 4	NC
Lane 5	NC

CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED (DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX XX	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

	VGA	Display	Audio	LAN	1394a / Card Reader	BT	LED
P15	M82-ME XT	HDMI/CRT	Digital Array Mic	Giga LAN RTL 8111C	YES / JMB380	N/A	Power Button with white LED-Backlight
P1	RS780M	DVI-I	Analog Array Mic	LAN(10/100) RTL 8101E	N/A / JMB385	N/A	NO Backlight

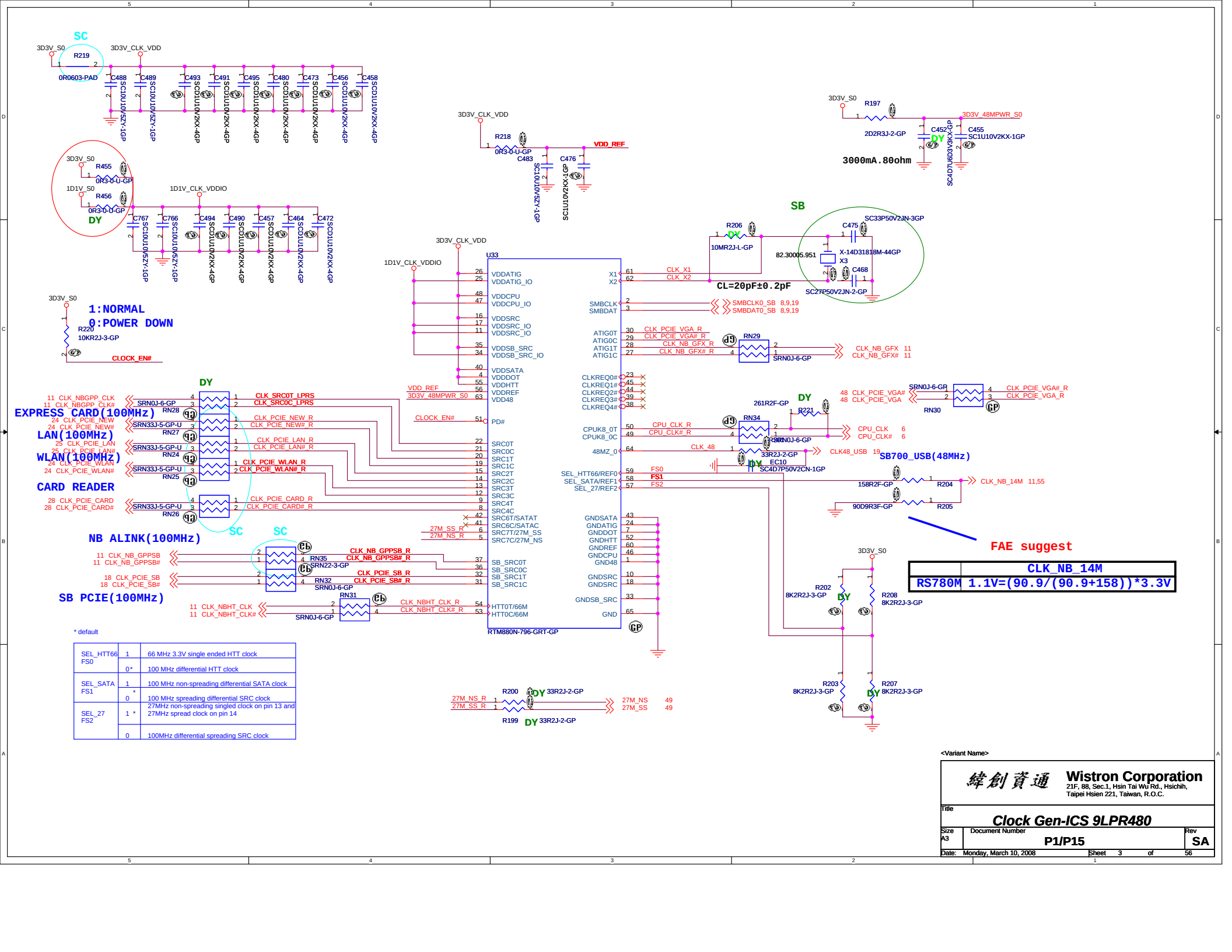
NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content
Size: A3 | Document Number: P1/P15 | Rev: SA
Date: Monday, March 10, 2008 | Sheet 2 of 56



* default

SEL_HTT66 FS0	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA FS1	1	100 MHz non-spreading differential SATA clock
	0 *	100 MHz spreading differential SRC clock
SEL_27 FS2	1 *	27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
	0	100MHz differential spreading SRC clock

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

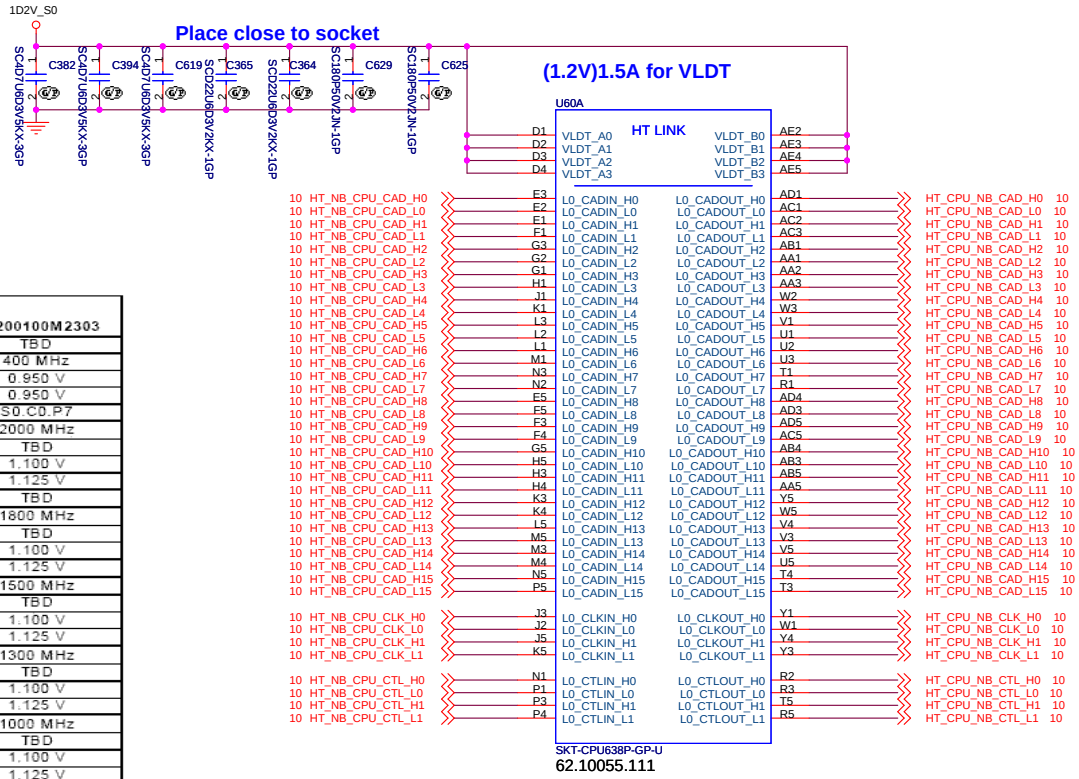
Title: Clock Gen-ICS 9LPR480

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 3 of 56

CPU / HT3.0

SSID = CPU



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Variant Name>

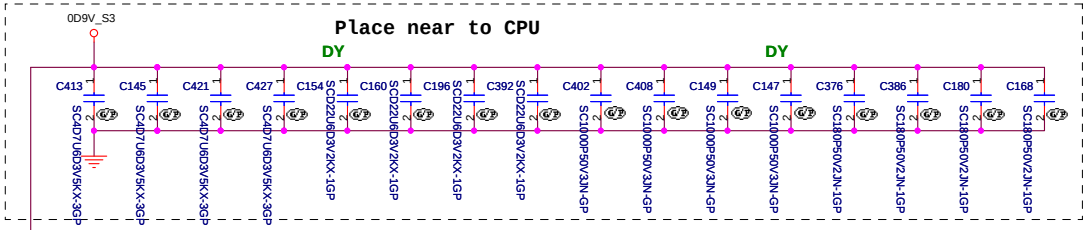
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

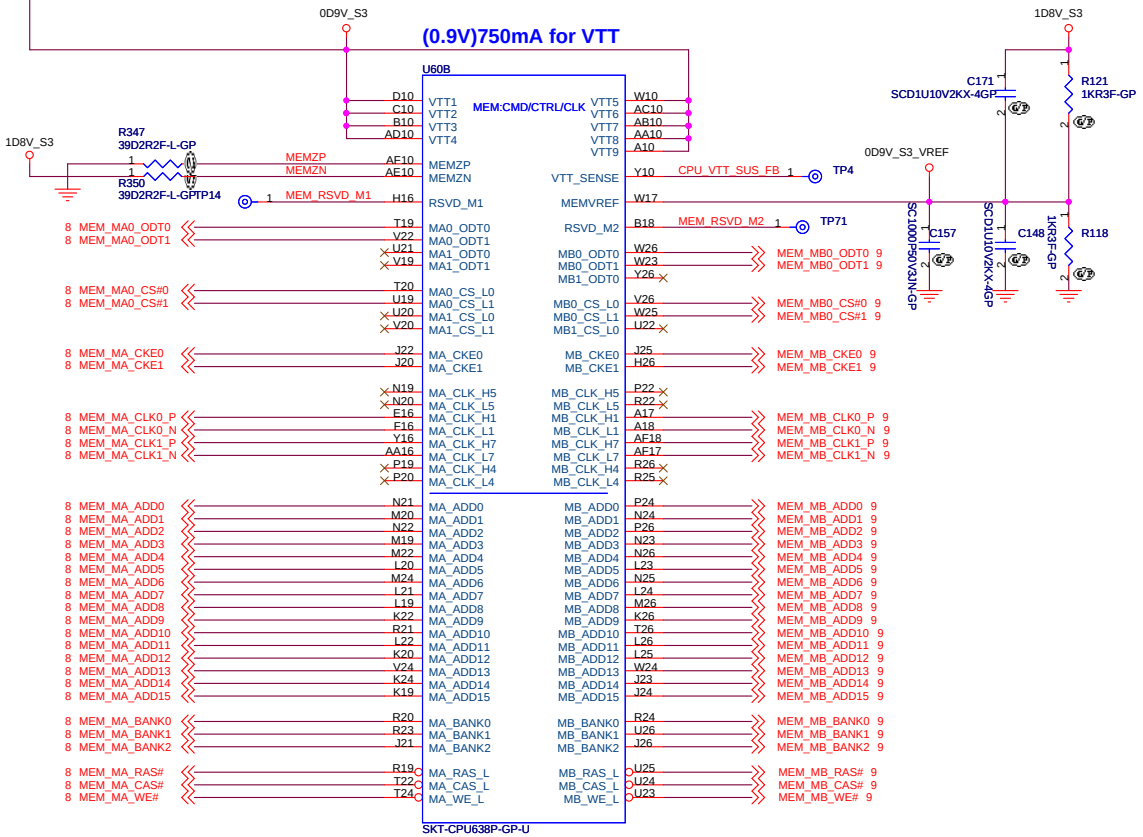
Title: CPU_HT_LINK I/F_(1/4)

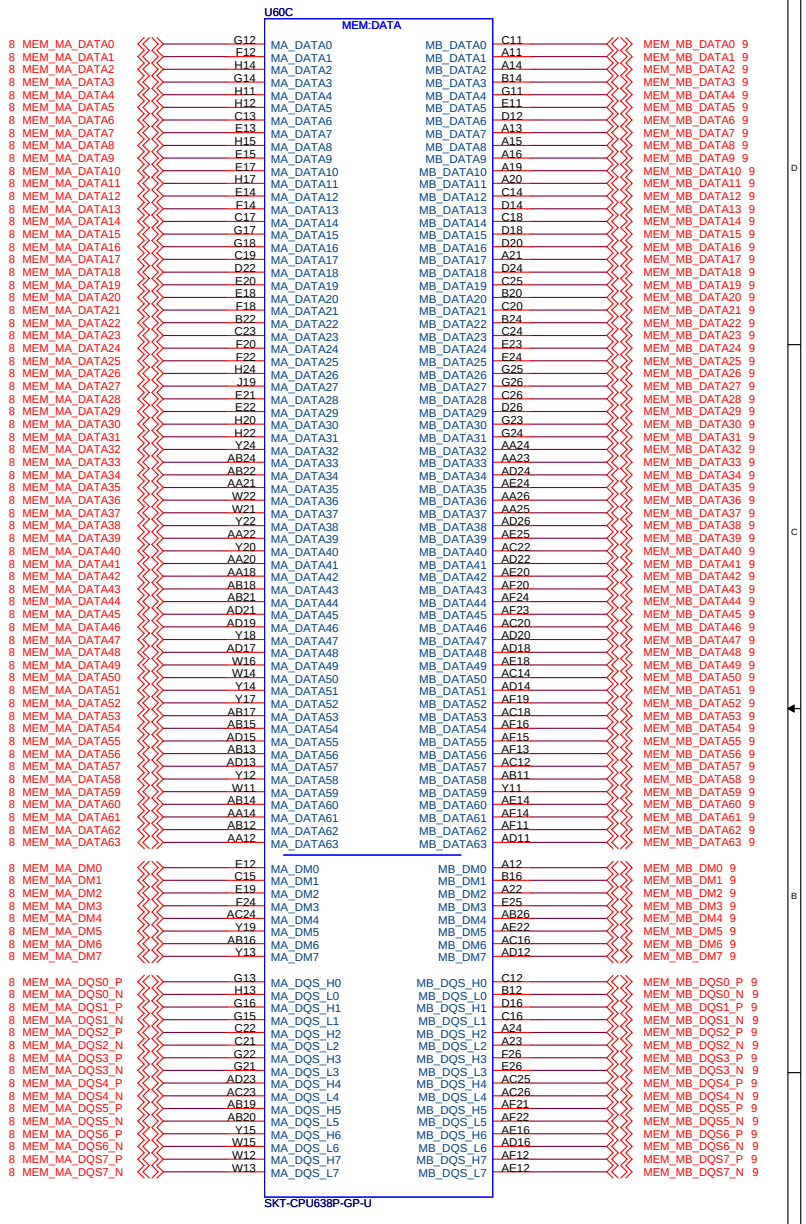
Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 4 of 56

CPU / DDR2







<variant_name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_DDR_(2/4)

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 5 of 56

1D8V_S0 1.8V_S3?

RN33 SRN300J-1-GP

18 CPU_LDT_RST# R439 0R2J-2-GP LDT_RST#_CPU 11
18 CPU_PWRGD R433 0R2J-2-GP LDT_PWROK
18 CPU_LDT_STOP# R437 0R2J-2-GP LDT_STP#_CPU 11
11 CPU_LDT_REQ# R178 CPU_LDT_REQ#_CPU 0R2J-2-GP

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

2D5V_S0 L25 BLM18PG330SN1D-GP +2.5V_RUN_VDDA (2.5V)250mA for VDDA

SC4D7U6D3V5KX-3GP C418 SC22U6D3V2KX-1GP C362 SC330P50V2KX-1GP C351

Cloce To CPU

CPU_CLK(200MHz)

3 CPU_CLK R432 169R2F-GP CLKCPU_IN
3 CPU_CLK# C738 SC3900P50V2KX-2GP C739 SC3900P50V2KX-2GP CLKCPU# IN

LDT_RST# CPU

HDT_RST# R440 0R2J-2-GP For HDT DBG

LDT_PWROK
LDT_STP# CPU
CPU_LDT_REQ# CPU

CPU_SIC
CPU_SID
CPU_ALERT#

1D2V_S0 R145 44D2R2F-GP R176 44D2R2F-GP CPU_HTREF0 CPU_HTREF1

38 CPU_VDD0_RUN_FB_H
38 CPU_VDD0_RUN_FB_L
38 CPU_VDD1_RUN_FB_H
38 CPU_VDD1_RUN_FB_L

CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI

TP53 CPU_TEST23
TP15 CPU_TEST18
TP18 CPU_TEST19
TP20 CPU_TEST25_H
TP16 CPU_TEST25_L
TP3 CPU_TEST21
TP57 CPU_TEST20
TP55 CPU_TEST24
TP52 CPU_TEST22
TP2 CPU_TEST12
TP56 CPU_TEST27

CPU_TEST9 R179 0R2J-2-GP

U60D

F8	VDDA1	KEY1	M11
F9	VDDA2	KEY2	W18
A9	CLKIN_H	SVC	A6
A8	CLKIN_L	SVD	A4
B7	RESET_L		
A7	PWROK		
F10	LDTSTOP_L	THERMTRIP_L	AF6
C6	LDTREQ_L	PROCHOT_L	AC7
		MEMHOT_L	AA8
AF4	SIC		
AF5	SID		
AF6	ALERT_L	THERMDC	W7
		THERMDA	W8
R6	HT_REF0		
P6	HT_REF1		
F6	VDD0_FB_H	VDDIO_FB_H	W9
F6	VDD0_FB_L	VDDIO_FB_L	Y9
Y6	VDD1_FB_H	VDDNB_FB_H	H6
AB6	VDD1_FB_L	VDDNB_FB_L	G6
G10	DBRDY		
AA9	TMS	DBREQ_L	E10
AC9	TCK		
AD9	TRST_L	TDO	AE9
AF9	TDI		
AD7	TEST23	TEST28_H	J7
		TEST28_L	H8
H10	TEST18		
G9	TEST19	TEST17	D7
		TEST16	E7
E9	TEST25_H	TEST15	F7
E8	TEST25_L	TEST14	C7
AB8	TEST21	TEST7	C3
AE7	TEST20	TEST10	K8
AE7	TEST24		
AE8	TEST22	TEST8	C4
AC8	TEST12		
AF8	TEST27		
C2	TEST9	TEST29_H	C9
AA6	TEST6	TEST29_L	C8
A3	RSVD1	RSVD10	H18
A5	RSVD2	RSVD9	H19
B3	RSVD3	RSVD8	AA7
B5	RSVD4	RSVD7	D5
C1	RSVD5	RSVD6	C5

SKT-CPU638P-GP-U

SC

1D8V_S3 R434 1KR2J-1-GP R435 1KR2J-1-GP

CPU_SVC 38
CPU_SVD 38

CPU exceeds to 125℃

CPU_PROCHOT# L
R340 300R2J-4-GP
1D8V_S3

H_THERMDC 23
H_THERMDA 23

DY C151 SC100P50V2JN-3GP

CPU_VDDIO_SUS_FB_H TP7
CPU_VDDIO_SUS_FB_L TP5

CPU_VDDNB_RUN_FB_H 38
CPU_VDDNB_RUN_FB_L 38

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

1D8V_S3 R349 300R2J-4-GP R338 300R2J-4-GP R342 10KR2J-3-GP

LDT_PWROK
C616 SCD1U10V2KX-4GP
MMBT3904-7-F-GP Q21
CPU_THERMTRIP#_L 19
CPU_PROCHOT# 18
R348 0R2J-2-GP

1D8V_S3 若不用要ph

R352 390R2J-1-GP R353 390R2J-1-GP
CPU_SIC
CPU_SID

Sideband temperature

near cpu

LDT_PWROK C615 SCD1U10V2KX-4GP

1D8V_S3 R653 300R2J-4-GP CPU_DBREQ#

CPU_TEST21 R652 300R2J-4-GP
CPU_TEST24 R654 300R2J-4-GP

1D8V_S3 DY R351 1KR2J-1-GP CPU_ALERT#

CPU temperature sensor driver INT event to EC

5V_S5 R447 10KR2J-3-GP LDT_PWROK#
3D3V_S0 R448 10KR2J-3-GP CPU_PWRGD_SVID_REG 38

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

LDT_PWROK H Q27 FDV301N-NL-GP
L Q28 FDV301N-NL-GP

HDT Connectors

HDT1 DY

CPU_DBREQ#
CPU_DBRDY
CPU_TCK
CPU_TMS
CPU_TDI
CPU_TRST#
CPU_TDO
1D8V_S3
HDT_RST#

SMC-CONN26A-FP 20.F0357.025

<Variant Name>

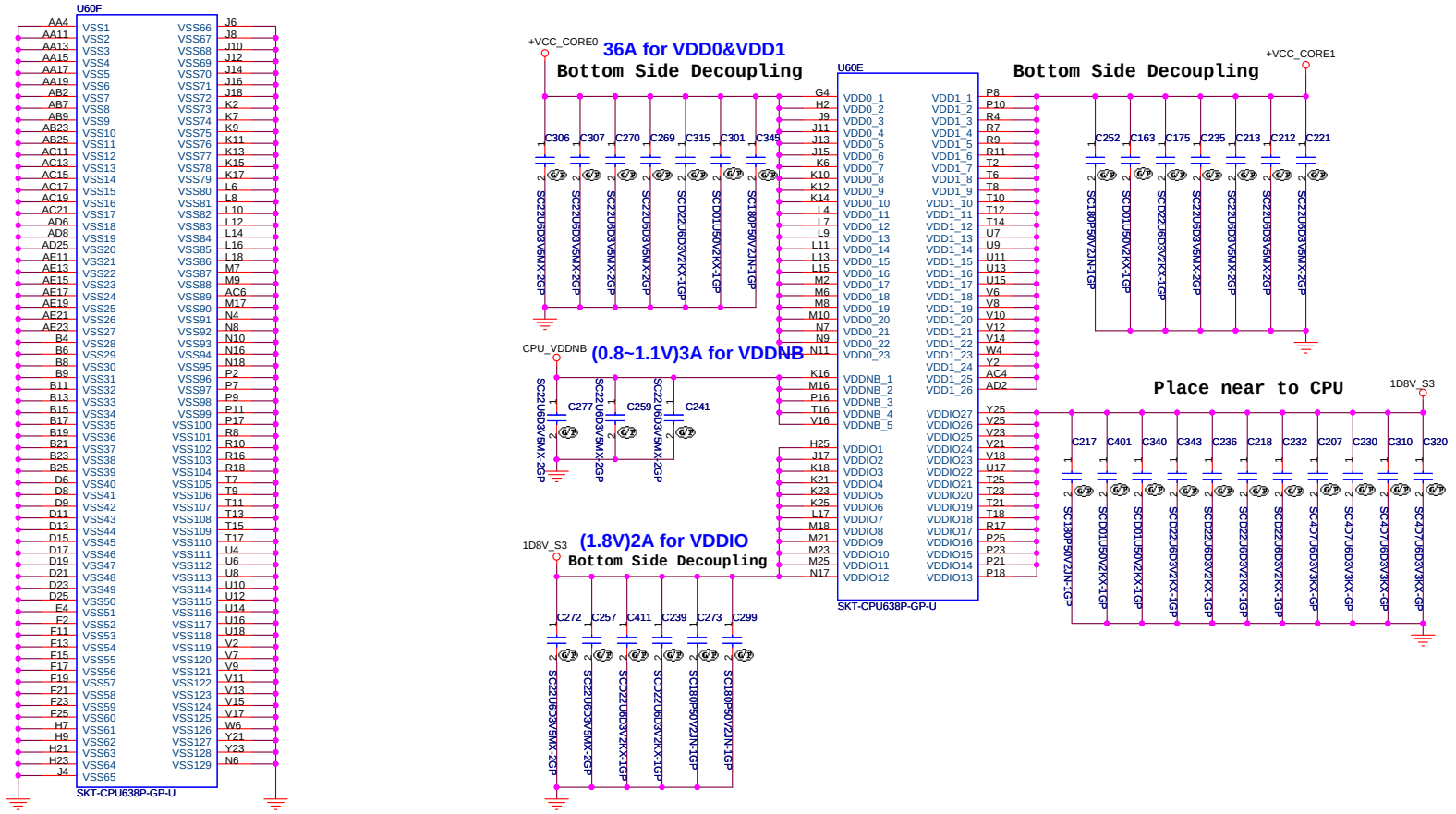
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Control&Debug_(3/4)

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 6 of 56

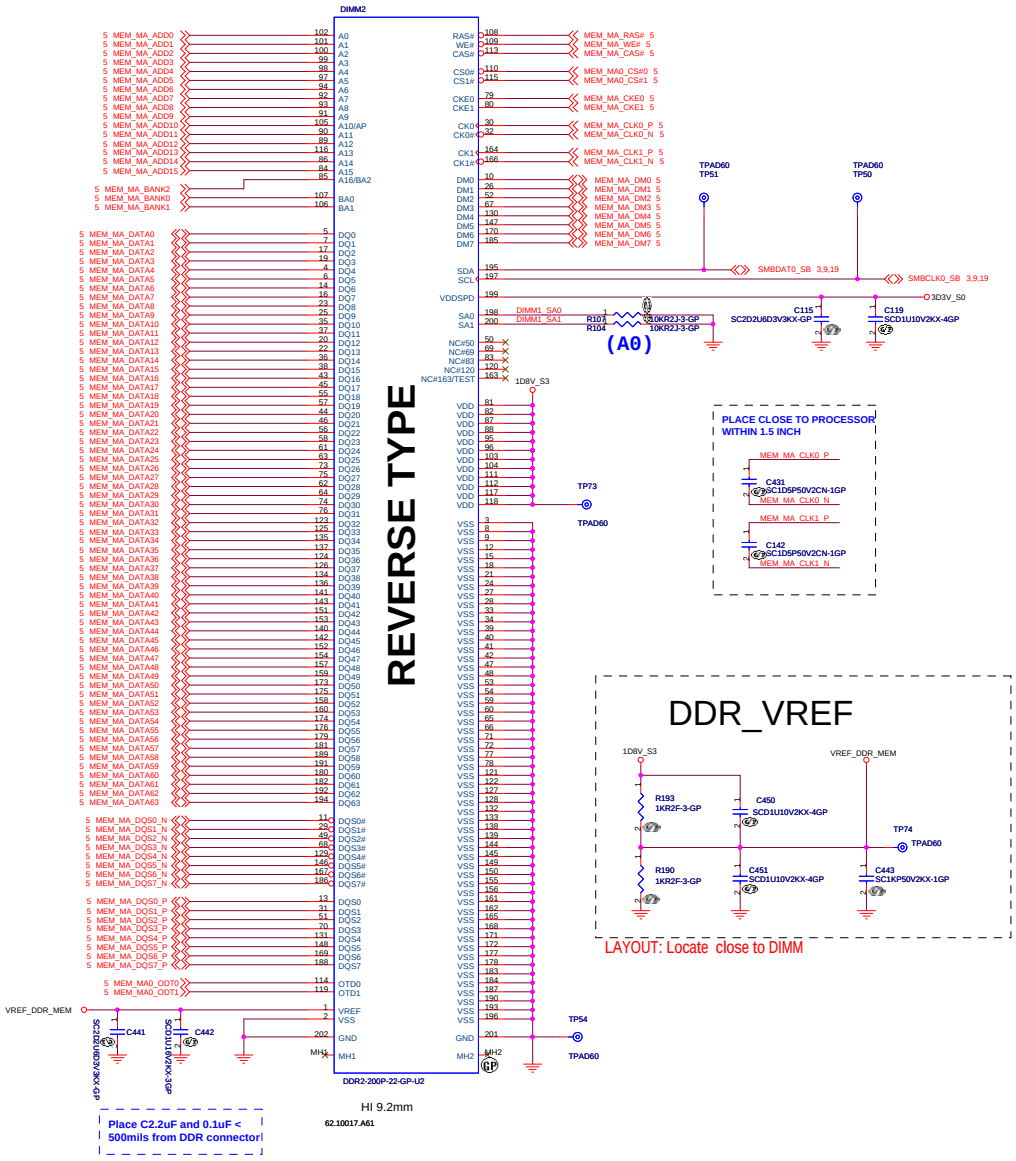
SSID = CPU

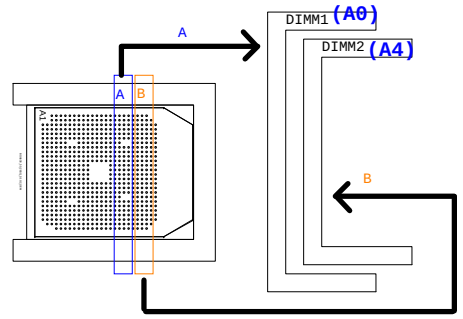


<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title	***CPU_Power_(4/4)***
Size: A3	Document Number: **P1/P15** Rev: **SA**
Date: Monday, March 10, 2008	Sheet 7 of 56

SSID = MEMORY

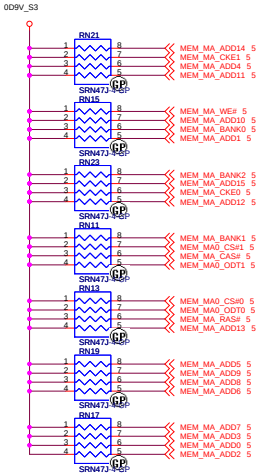




PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

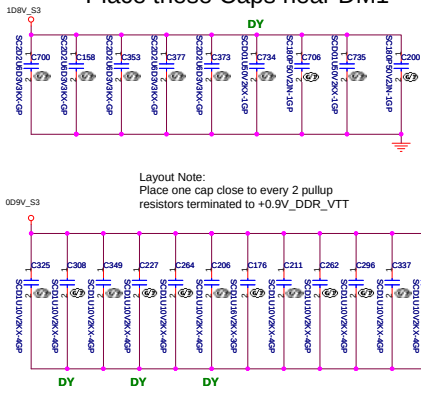
Do not share the Term resistor between the DDR addess and Control Signals.



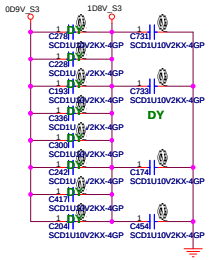
DDR_VREF

Decoupling Capacitor

Place these Caps near DM1



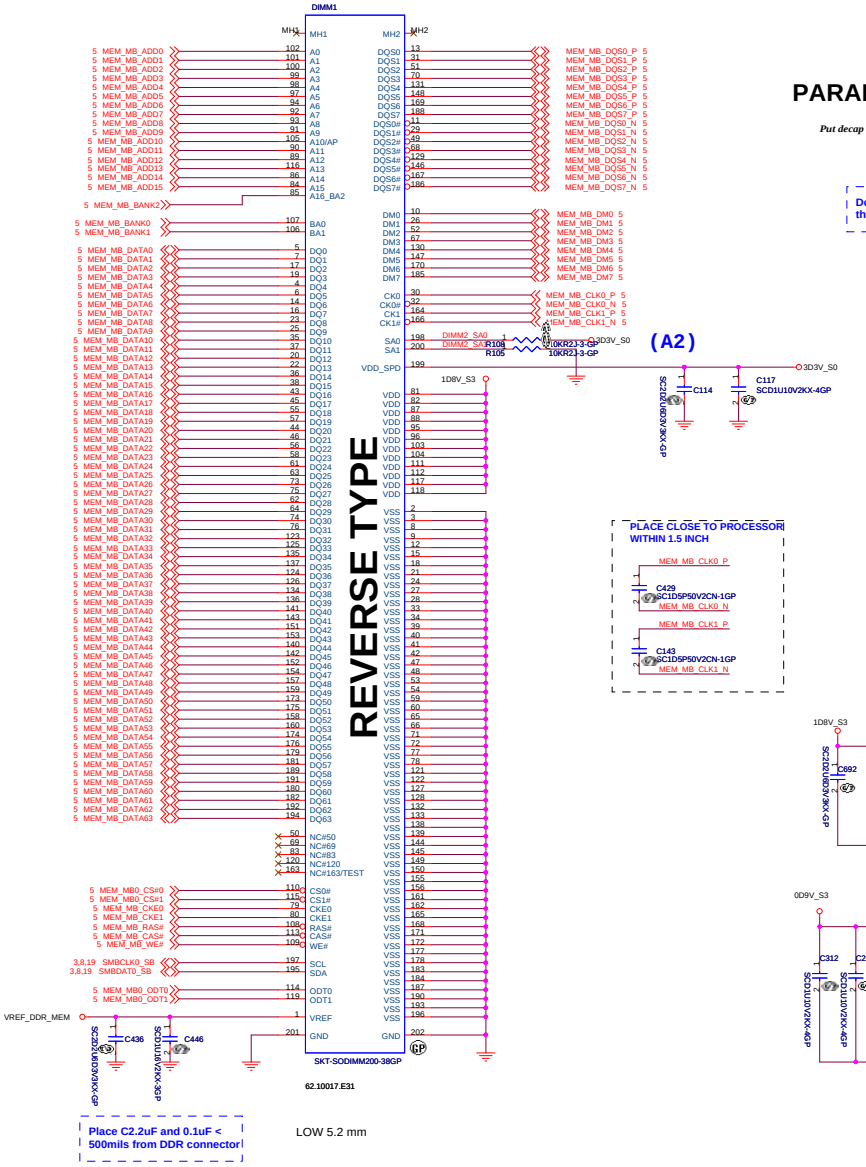
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



<Variant Name>
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_DIMM1
Size: A2 | Document Number: P1/P15 | Rev: SA
Date: Monday, March 10, 2008 | Sheet 8 of 56

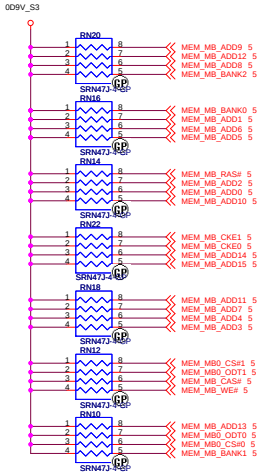
SSID = MEMORY



PARALLEL TERMINATION

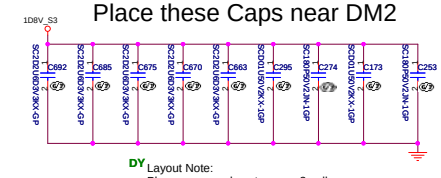
Put decap near power(0.9V) and pull-up resistor

Do not share the Term resistor between the DDR addess and Control Signals.

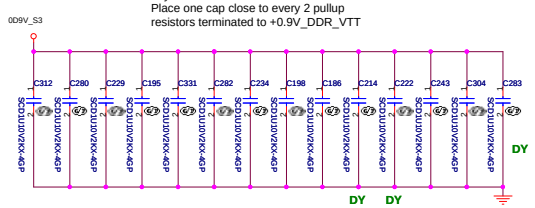


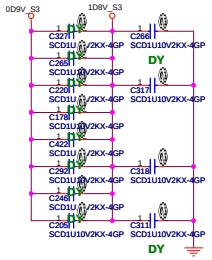
Decoupling Capacitor

Place these Caps near DM2



Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT





<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: DDR_DIMM2

Size	Document Number	Rev
A2	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 9 of 56

SSID = N.B

U61A

PART 1 OF 6

HYPER TRANSPORT CPU I/F

RS780M-GP-U1

Place < 100mils from pin C23 and A24

Place < 100mils from pin B25 and B24

Placement: close RS780

UMA DVI

U61B

PART 2 OF 6

PCIE I/F GFX

PCIE I/F GPP

PCIE I/F SB

RS780M-GP-U1

Rx PCIE reversed

Tx PCIE reversed

NEW

WLAN

LAN

CARD

A-LINK

Place < 100mils from pin AC8 and AB8

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_HT LINK&PCIE(1/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 10 of 56

SSID = N.B

STRAP_DEBUG_BUS_GPIO_ENABLE
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)
*0 : Enable 1 : Disable

SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

close NB within 1000 mil

Close to NB ball

ENABLE External CLK GEN

	GPIO	MODE
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V

15mil width

15mil width

pull up form SB

<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_LVDS&CRT_(2/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 11 of 56

SSID = N.B

MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

1D8V_S0 — L5 BLM21PG221SN-1GP — 220 ohm @ 100MHz,2A — +1.8V_MEM_VDDQ

C102 SC22U6D3V5MX-2GP; C140 SCD1U10V2KX-4GP; C141 SCD1U10V2KX-4GP; C105 SC1U6D3V2KX-GP; C106 SC1U6D3V2KX-GP

U61D — PAR 4 OF 6 — SBD_MEM/DVO_I/F — RS780M-GP-U1

MEM_A0 AB12; MEM_A1 AE16; MEM_A2 V11; MEM_A3 AE15; MEM_A4 AA12; MEM_A5 AB16; MEM_A6 AB14; MEM_A7 AD14; MEM_A8 AD13; MEM_A9 AD15; MEM_A10 AC16; MEM_A11 AE13; MEM_A12 AC14; MEM_A13 Y14

TP8

MEM_BA0 AD16; MEM_BA1 AE17; MEM_BA2 AD17

RAS# W12; CAS# Y12; WE# AD18; CS# AB13; CKE AB18; ODT V14

MEM_CLKP V15; MEM_CLKN W14

MEM_COMPP AE12; MEM_COMPN AD12

MEM_DQ0/DVO_VSYNC AA18 MEM_DQ0; MEM_DQ1/DVO_HSYNC AA20 MEM_DQ1; MEM_DQ2/DVO_DE AA19 MEM_DQ2; MEM_DQ3/DVO_D0 Y19 MEM_DQ3; MEM_DQ4 V17 MEM_DQ4; MEM_DQ5/DVO_D1 AA17 MEM_DQ5; MEM_DQ6/DVO_D2 AA15 MEM_DQ6; MEM_DQ7/DVO_D4 Y15 MEM_DQ7; MEM_DQ8/DVO_D3 AC20 MEM_DQ8; MEM_DQ9/DVO_D5 AD19 MEM_DQ9; MEM_DQ10/DVO_D6 AE22 MEM_DQ10; MEM_DQ11/DVO_D7 AC18 MEM_DQ11; MEM_DQ12 AB20 MEM_DQ12; MEM_DQ13/DVO_D9 AD22 MEM_DQ13; MEM_DQ14/DVO_D10 AC22 MEM_DQ14; MEM_DQ15/DVO_D11 AD21 MEM_DQ15

MEM_DQS0P/DVO_IDCKP Y17 MEM_DQS0P; MEM_DQS0N/DVO_IDCKN W18 MEM_DQS0N; MEM_DQS1P AD20 MEM_DQS1P; MEM_DQS1N AE21 MEM_DQS1N

MEM_DM0 W17 MEM_DM0; MEM_DM1/DVO_D8 AE19 MEM_DM1

IOPLLVDD18 AE23 +1.8V_IOPLLVDD18; IOPLLVDD AE24 +1.1V_IOPLLVDD

IOPLLVSS AD23

MEM_VREF AE18 MEM_VREF_NB

+1.8V_MEM_VDDQ — 40D2R2F-GP R120 — R360 40D2R2F-GP

15mil width — L8 BLM15AG221SN-GP — 1D8V_S0 — C153 SC2D2U6D3V3KX-GP

15mil width — L15 BLM15AG221SN-GP — 1D1V_S0 — C187 SC2D2U6D3V3KX-GP; C182 SCD1U10V2KX-4GP

+1.8V_MEM_VDDQ — R119 1KR2F-3-GP — C152 SCD1U10V2KX-4GP; R122 1KR2F-3-GP — C188 SCD1U10V2KX-4GP

SC

U21 — HYB18T512161B2F-25-GP

MEM_BA0 L2; MEM_BA1 L3

MEM_A12 R2; MEM_A11 P7; MEM_A10 M2; MEM_A9 P3; MEM_A8 P8; MEM_A7 P2; MEM_A6 N7; MEM_A5 N3; MEM_A4 N8; MEM_A3 N2; MEM_A2 M7; MEM_A1 M3; MEM_A0 M8

ATI DY — DY — R116 100R2F-L1-GP-U

MEM_CLKN K8; MEM_CLKP J8

CKE K2

CS# L8; WE# K3; RAS# K7; CAS# L7

MEM_DM0 F3; MEM_DM1 B3

ODT K9

MEM_DQS0P F7; MEM_DQS0N E8

MEM_DQS1P B7; MEM_DQS1N A8

MEM_VREF_CHIP J2

MEM_BA2 L1

BA0 BA1 A12 A11 A10/AP A9 A8 A7 A6 A5 A4 A3 A2 A1 A0

CK CK CKE CS WE RAS CAS LDM UDM ODT LDQS LDQS UDQS UDQS VREF NC#A2 NC#E2 NC#L1 NC#R3 NC#R7 NC#R8

DQ15 B9 MEM_DQ15; DQ14 B1 MEM_DQ14; DQ13 D9 MEM_DQ13; DQ12 D1 MEM_DQ12; DQ11 D3 MEM_DQ11; DQ10 D7 MEM_DQ10; DQ9 C2 MEM_DQ9; DQ8 C8 MEM_DQ8; DQ7 F9 MEM_DQ7; DQ6 F1 MEM_DQ6; DQ5 H9 MEM_DQ5; DQ4 H1 MEM_DQ4; DQ3 H3 MEM_DQ3; DQ2 H7 MEM_DQ2; DQ1 G2 MEM_DQ1; DQ0 G8 MEM_DQ0

+1.8V_MEM_VDDQ — VDDQ1 A9; VDDQ2 C1; VDDQ3 C3; VDDQ4 C7; VDDQ5 C9; VDDQ6 E9; VDDQ7 G1; VDDQ8 G3; VDDQ9 G7; VDDQ10 G9

VDD1 A1; VDD2 E1; VDD3 J9; VDD4 M9; VDD5 R1

L4 BLM18AG601SN-3GP — 600 ohm @ 100MHz,200mA

VDDL_VRAM — VDDL J1; VSSDL J7

Layout Note: 50 mil for VSSDL

C103 SC1U6D3V3KX-1GP

VSSQ1 A7; VSSQ2 B2; VSSQ3 B8; VSSQ4 D2; VSSQ5 D8; VSSQ6 E7; VSSQ7 F2; VSSQ8 F8; VSSQ9 H2; VSSQ10 H8

VSS1 A3; VSS2 E3; VSS3 J3; VSS4 N1; VSS5 P9

+1.8V_MEM_VDDQ — R93 1KR2F-3-GP — C100 SCD1U10V2KX-4GP — R100 1KR2F-3-GP — C104 SCD1U10V2KX-4GP

72.18512.M0U

<Variant Name>

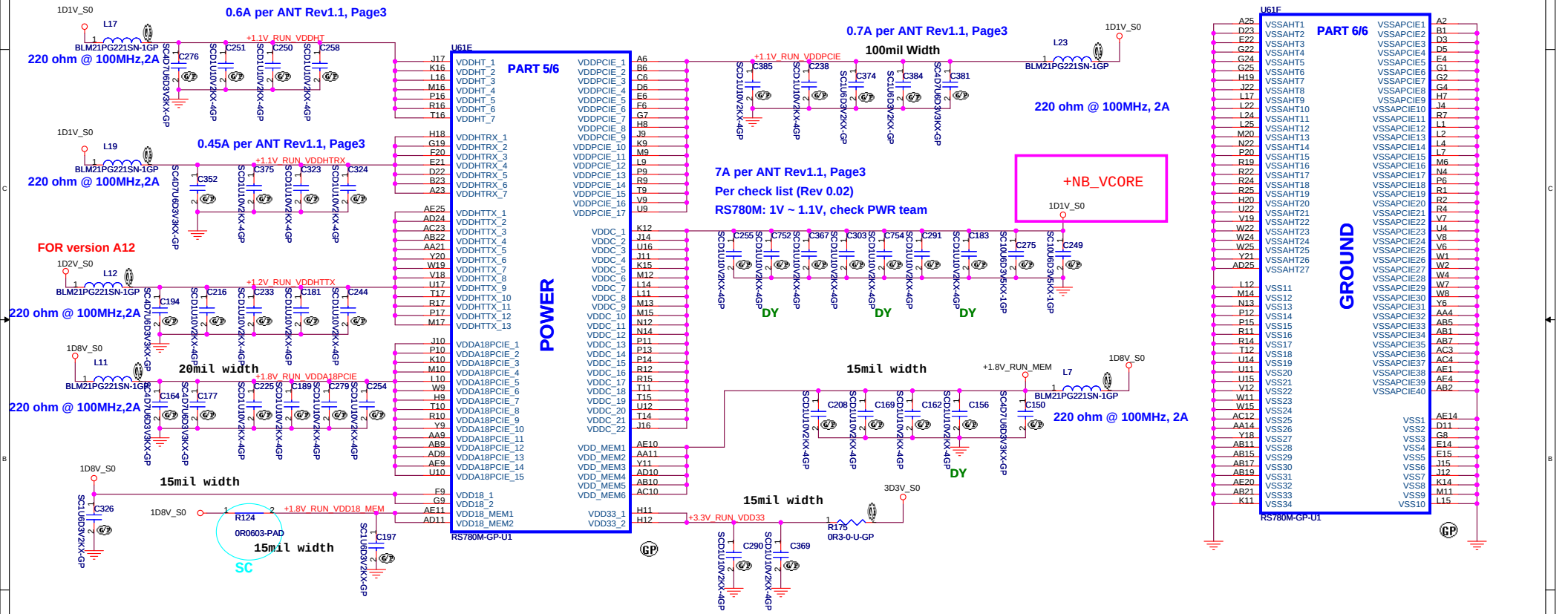
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_SidePort_(3/4)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 12 of 56

SSID = N.B



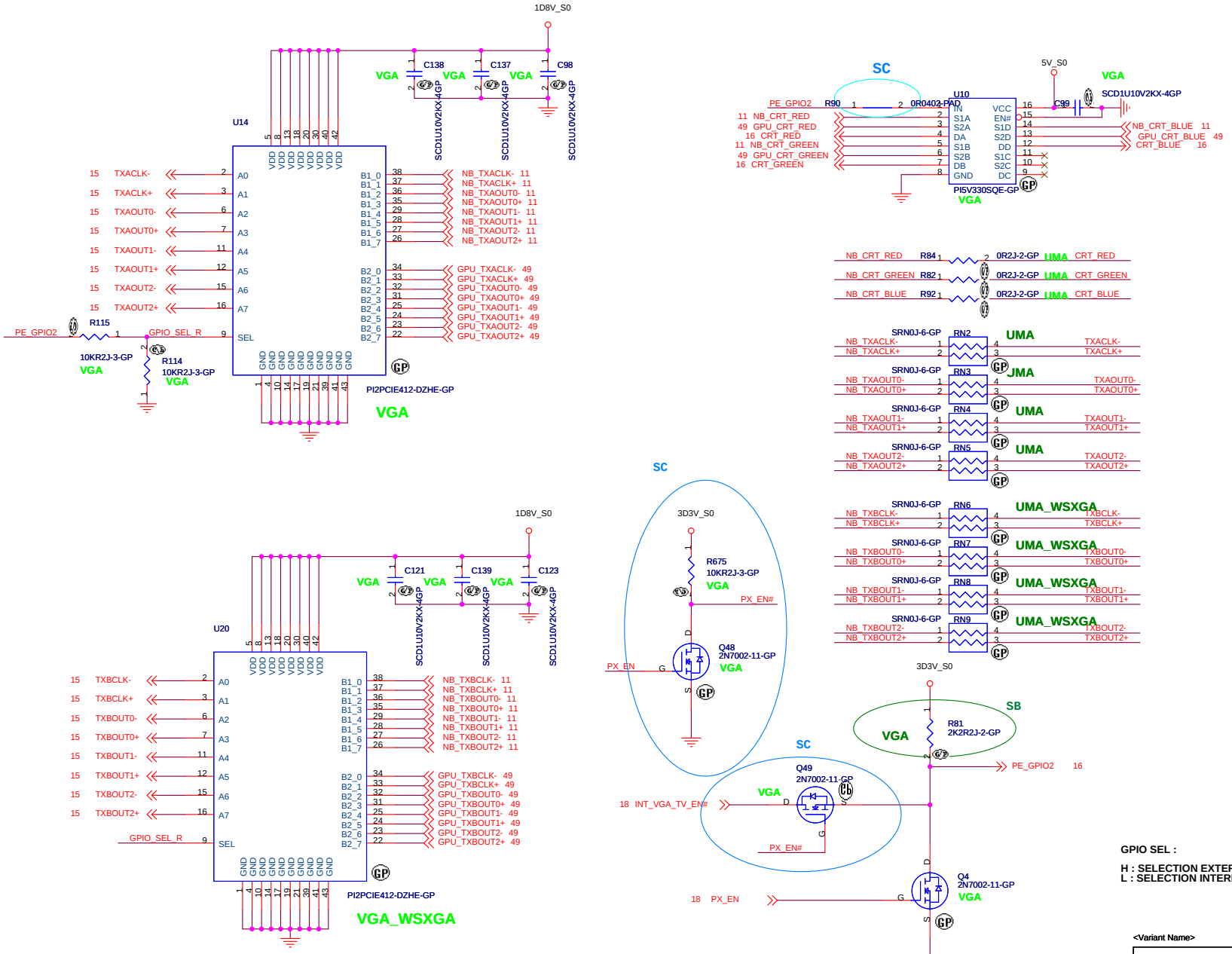
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

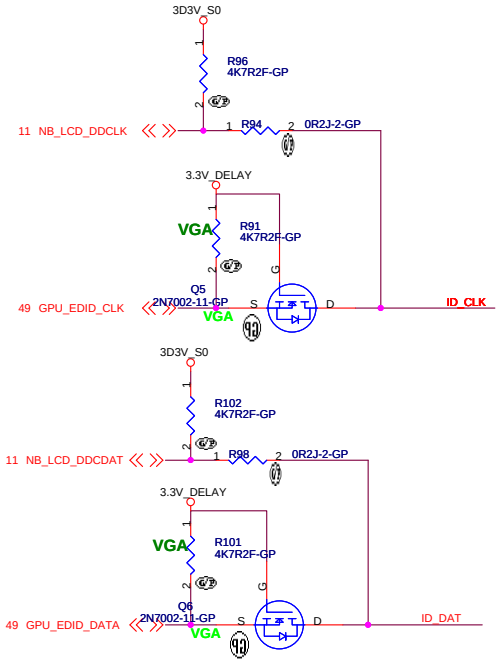
Title: ***ATi-RS780M_PWR&GD_(4/4)***

Size	Document Number	Rev
A3	P1/P15	SA

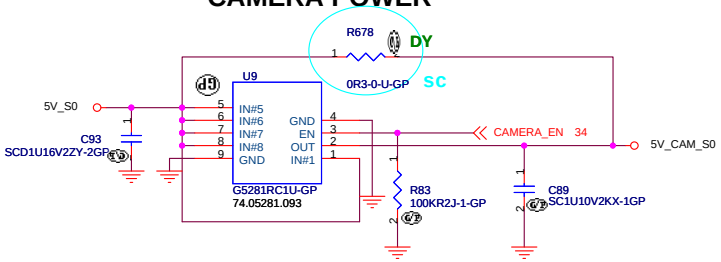
Date: Monday, March 10, 2008 Sheet 13 of 56

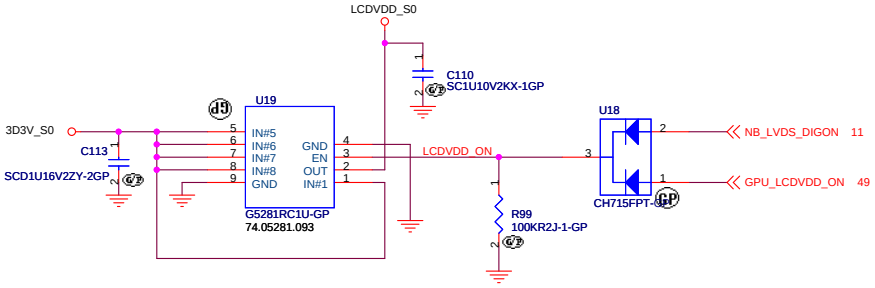

1D8V_S0
U14
PI2PCIE412-DZHE-GP
VGA
C138
C137
C98
SCD1U10V2KX-4GP
R115
10KR2J-3-GP
R114
10KR2J-3-GP
PE_GPIO2
GPIO_SEL_R
TXACLK-
TXACLK+
TXAOUT0-
TXAOUT0+
TXAOUT1-
TXAOUT1+
TXAOUT2-
TXAOUT2+
NB_TXACLK- 11
NB_TXACLK+ 11
NB_TXAOUT0- 11
NB_TXAOUT0+ 11
NB_TXAOUT1- 11
NB_TXAOUT1+ 11
NB_TXAOUT2- 11
NB_TXAOUT2+ 11
GPU_TXACLK- 49
GPU_TXACLK+ 49
GPU_TXAOUT0- 49
GPU_TXAOUT0+ 49
GPU_TXAOUT1- 49
GPU_TXAOUT1+ 49
GPU_TXAOUT2- 49
GPU_TXAOUT2+ 49
SC
5V_S0
U10
PI5V330SQE-GP
PE_GPIO2
R90
0R0402-PAD
C99
SCD1U10V2KX-4GP
NB_CRT_RED 11
GPU_CRT_RED 49
CRT_RED 16
NB_CRT_GREEN 11
GPU_CRT_GREEN 49
CRT_GREEN 16
NB_CRT_BLUE 11
GPU_CRT_BLUE 49
CRT_BLUE 16
R84
R82
R92
0R2J-2-GP
UMA
SRN0J-6-GP
RN2
RN3
RN4
RN5
RN6
RN7
RN8
RN9
UMA_WSXGA
U20
VGA_WSXGA
C121
C139
C123
TXBCLK-
TXBCLK+
TXBOUT0-
TXBOUT0+
TXBOUT1-
TXBOUT1+
TXBOUT2-
TXBOUT2+
NB_TXBCLK- 11
NB_TXBCLK+ 11
NB_TXBOUT0- 11
NB_TXBOUT0+ 11
NB_TXBOUT1- 11
NB_TXBOUT1+ 11
NB_TXBOUT2- 11
NB_TXBOUT2+ 11
GPU_TXBCLK- 49
GPU_TXBCLK+ 49
GPU_TXBOUT0- 49
GPU_TXBOUT0+ 49
GPU_TXBOUT1- 49
GPU_TXBOUT1+ 49
GPU_TXBOUT2- 49
GPU_TXBOUT2+ 49
3D3V_S0
R675
10KR2J-3-GP
PX_EN#
PX_EN
Q48
2N7002-11-GP
Q49
2N7002-11-GP
INT_VGA_TV_EN# 18
R81
2K2R2J-2-GP
SB
PE_GPIO2 16
Q4
2N7002-11-GP
PE_GPIO2_NB 18
GPIO SEL :
H : SELECTION EXTERNAL GRAPHIC
L : SELECTION INTERNAL GRAPHIC
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CRT / LVDS MUX
Size A3
Document Number
P1/P15
Rev SA
Date: Monday, March 10, 2008
Sheet 14 of 56

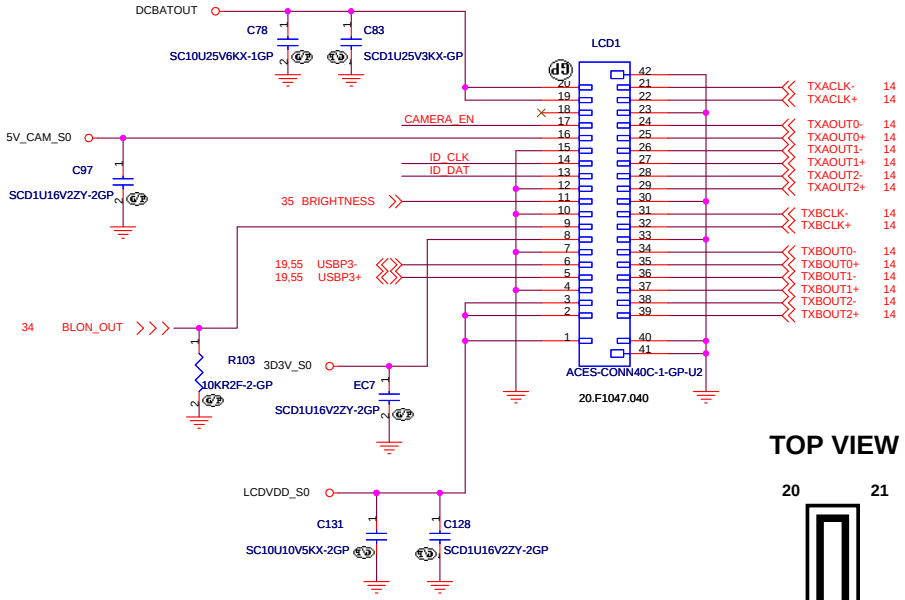
LCD CONNECTOR



CAMERA POWER







TOP VIEW

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

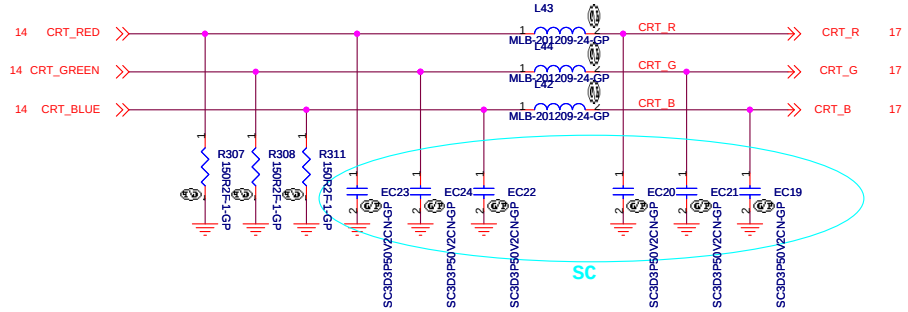
Title: **LCD CONN/CAMERA**

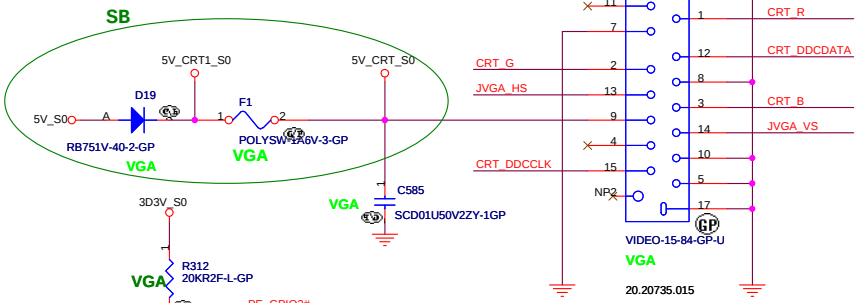
Size	Document Number	Rev
A3	P1/P15	SA

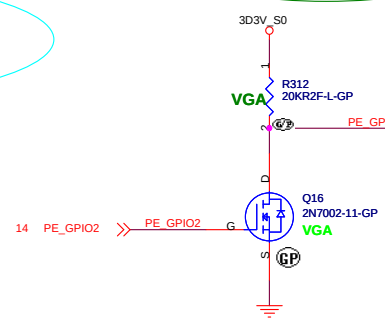
Date: Monday, March 10, 2008 Sheet 15 of 56

CRT I/F & CONNECTOR

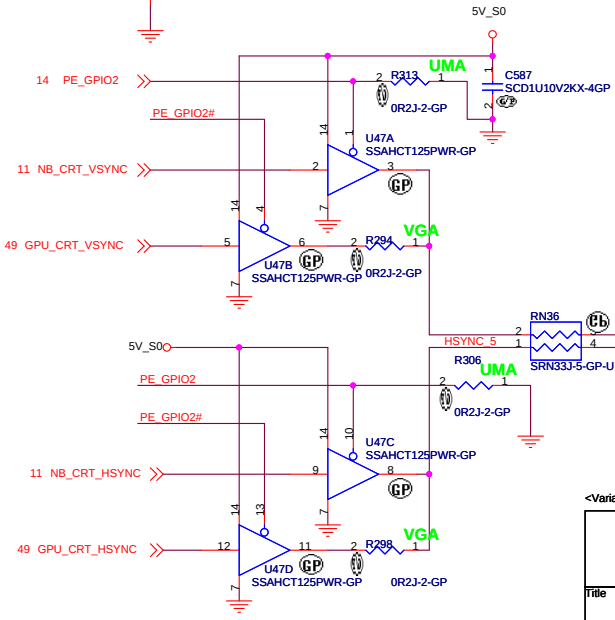
Layout Note:
Place these resistors close to the CRT-out connector

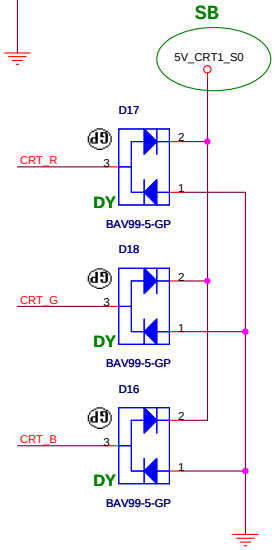


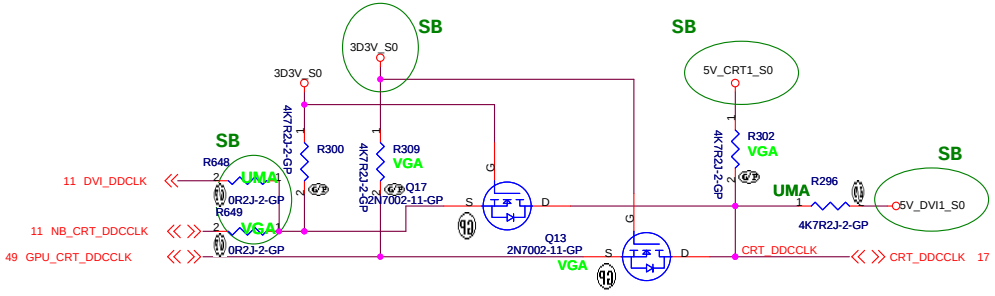


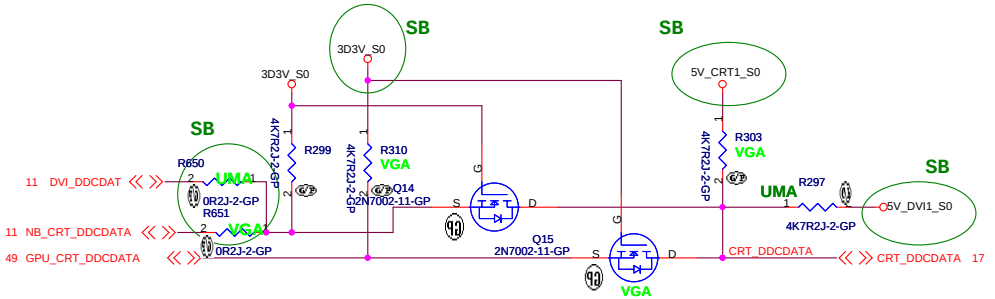


Hsync & Vsync level shift









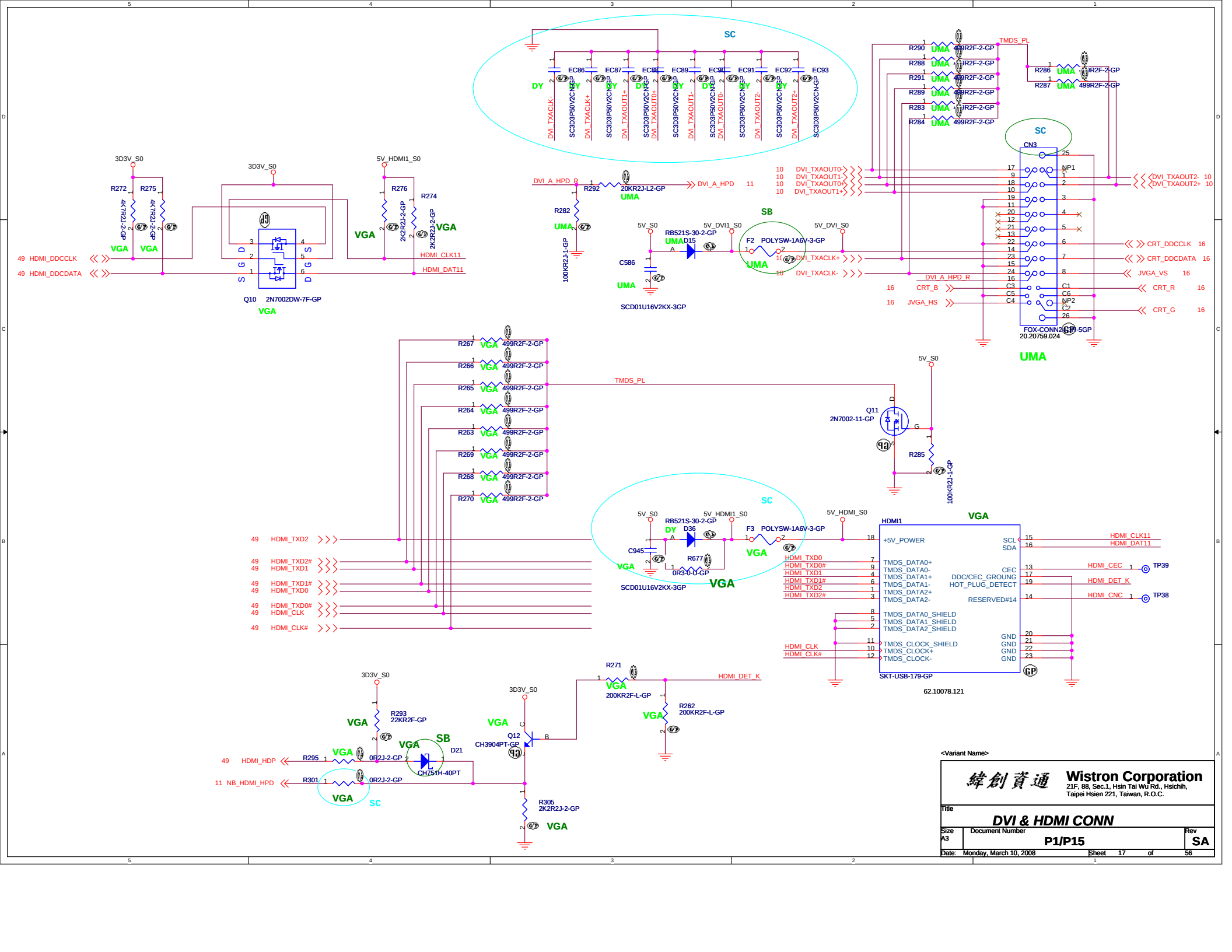
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

<Variant Name>

Title: **CRT CONN**

Size: A3 | Document Number: **P1/P15** | Rev: **SA**

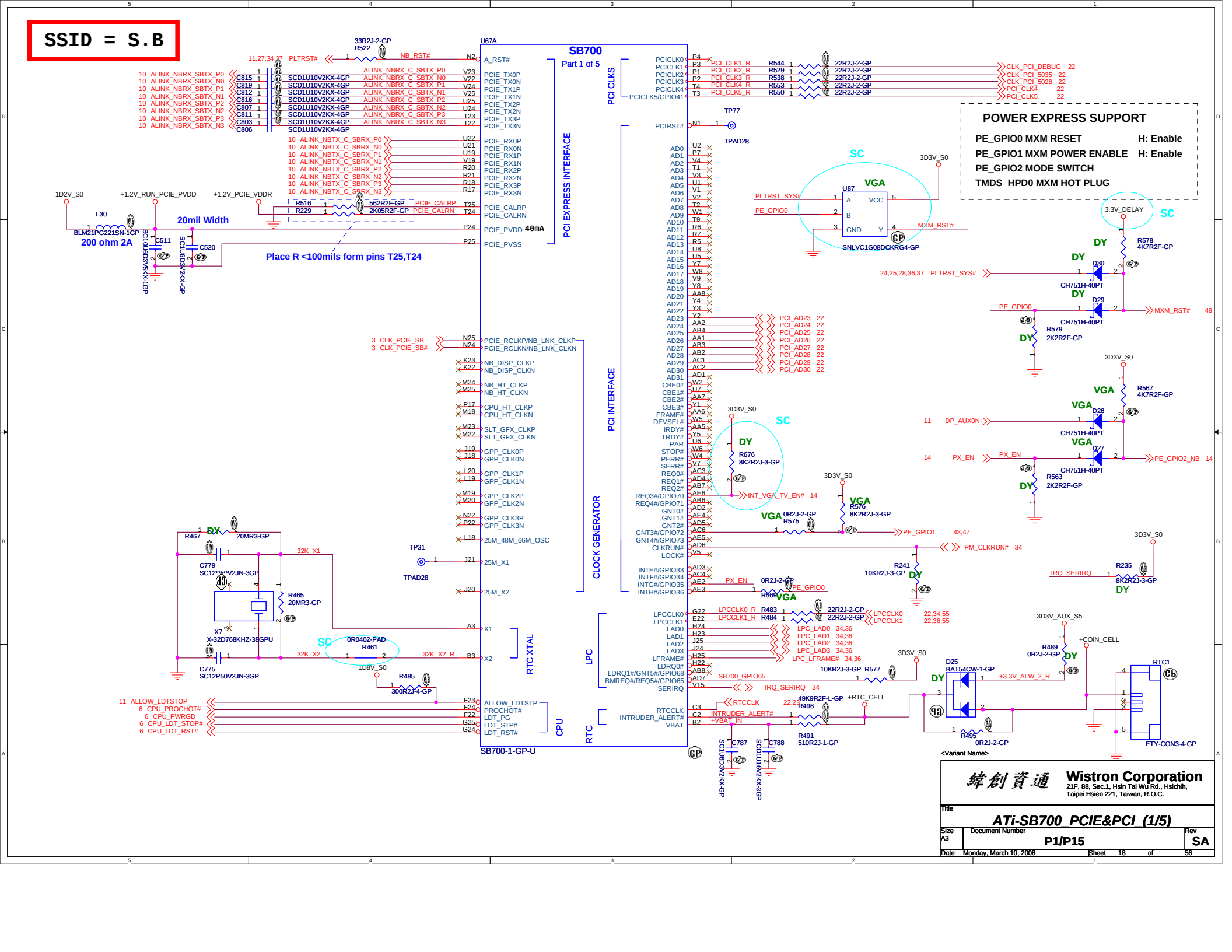
Date: Monday, March 10, 2008 | Sheet 16 of 56

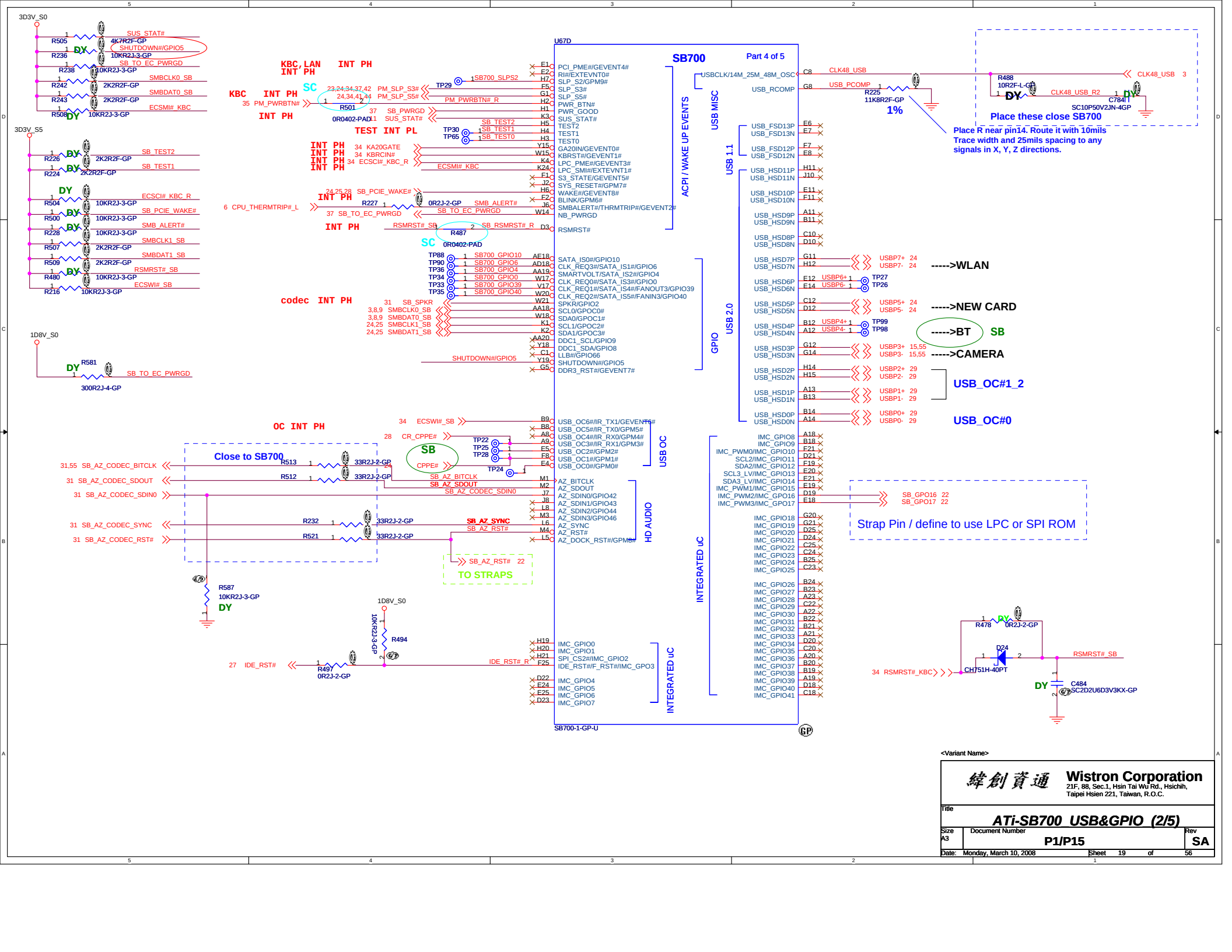


<variant_name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***DVI & HDMI CONN***	
Size A3	Document Number **P1/P15**	Rev **SA**
Date: Monday, March 10, 2008	Sheet 17 of 56	

SSID = S.B


SB700
Part 1 of 5
U67A
SB700-1-GP-U
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
POWER EXPRESS SUPPORT
PE_GPIO0 MXM RESET H: Enable
PE_GPIO1 MXM POWER ENABLE H: Enable
PE_GPIO2 MODE SWITCH
TMDS_HPD0 MXM HOT PLUG
SNLVC1G08DCKRG4-GP
CH751H-40PT
Place R <100mils form pins T25,T24
20mil Width
200 ohm 2A
BLM21PG221SN-1GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-SB700_PCIE&PCI_(1/5)
P1/P15
SA
Monday, March 10, 2008
Sheet 18 of 56



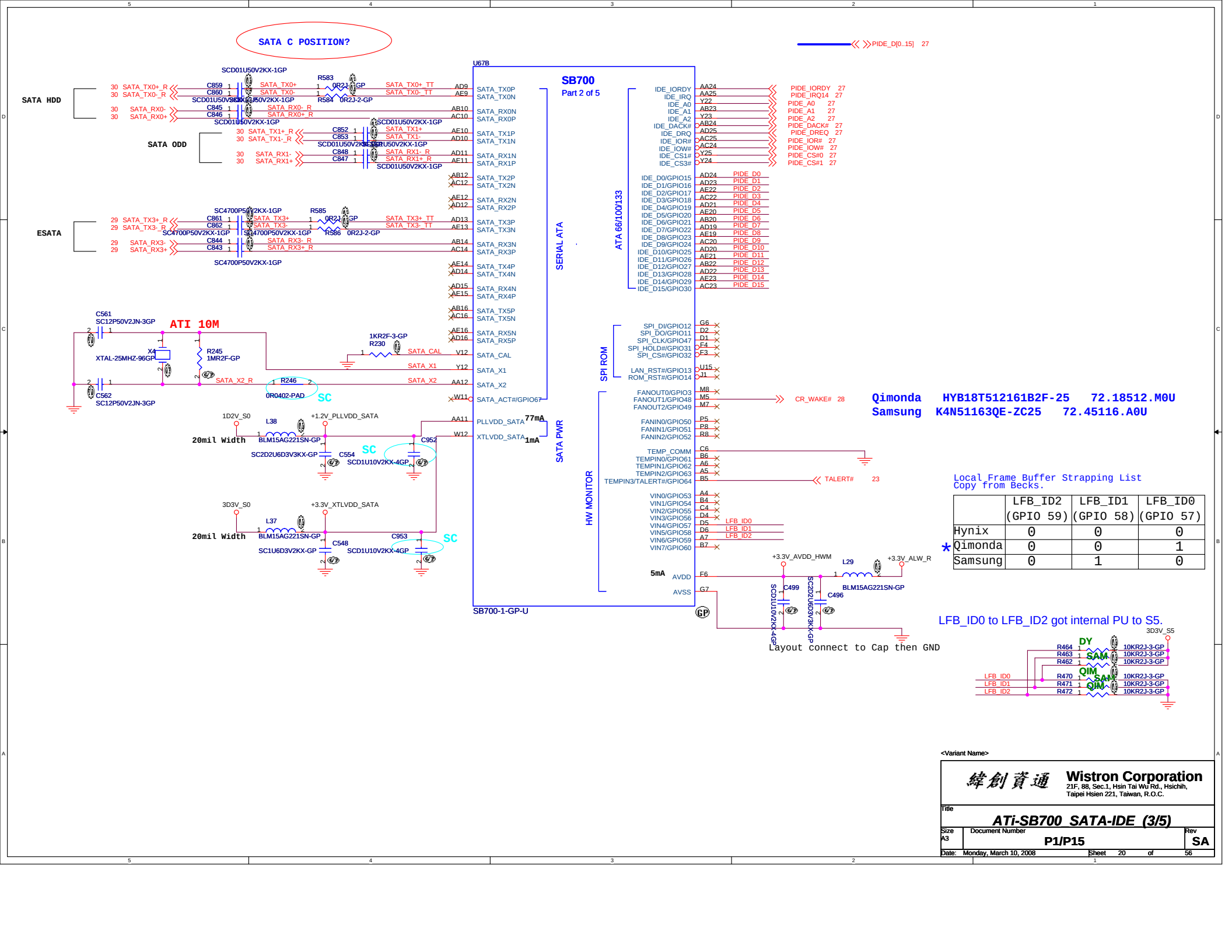
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_USB&GPIO_(2/5)

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 19 of 56



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***ATi-SB700_SATA-IDE_(3/5)***

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 20 of 56

SSID = S.B

U67C

SB700 Part 3 of 5

POWER

Use Flash I/O:+1.8V / IDE:+3.3V

Use Plane Shape for +3.3V_AVDD_USB

SB700-1-GP-U

U67E

SB700 Part 5 of 5

GROUND

SB700-1-GP-U

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

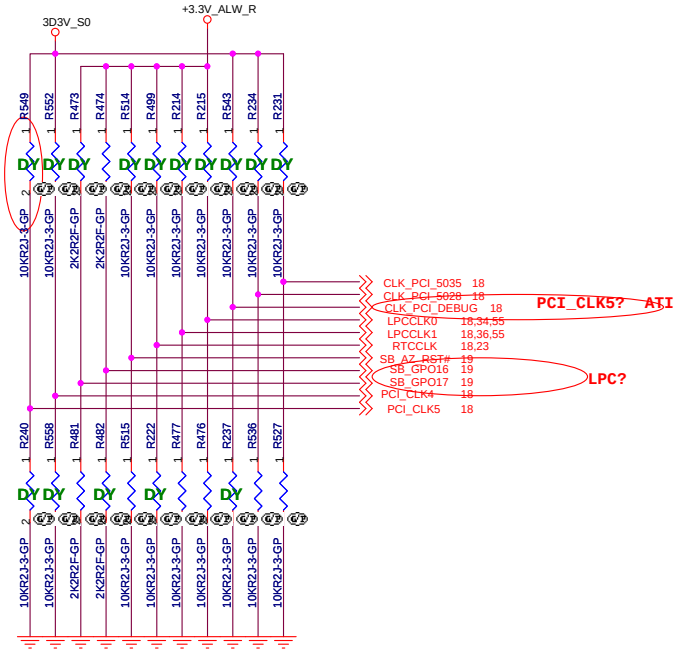
Title: **ATi-SB700_POWER&GND_(4/5)**

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 21 of 56

SSID = S.B

REQUIRED STRAPS



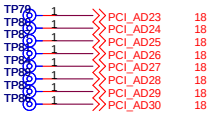
REQUIRED SYSTEM STRAPS

	CLK_PCI_5035	CLK_PCI_5028	CLK_PCI_DEBUG	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved; H, L = SPI ROM; L, H = LPC ROM DEFAULT; L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS

NEED?



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

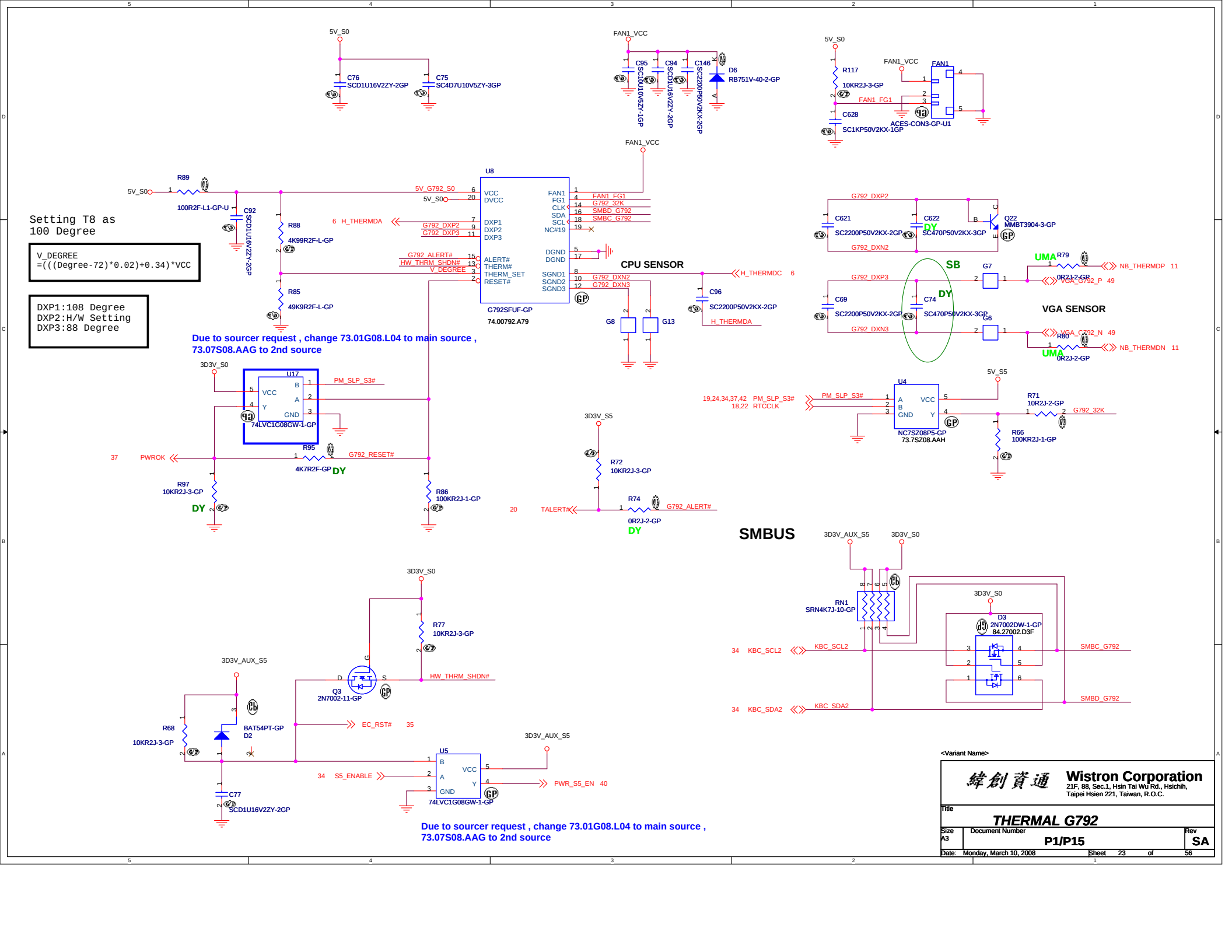
<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

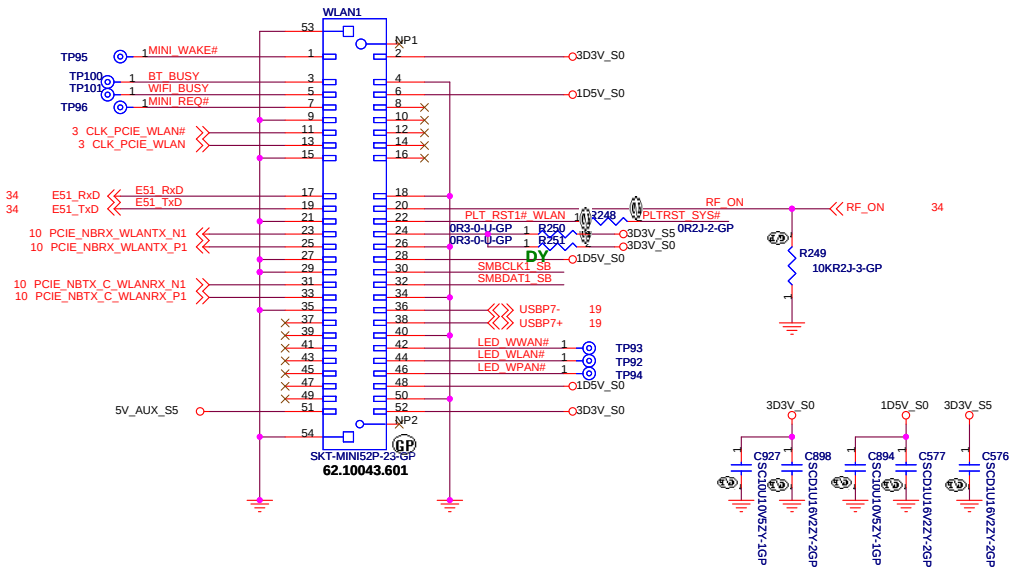
Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: P1/P15 | Rev: SA

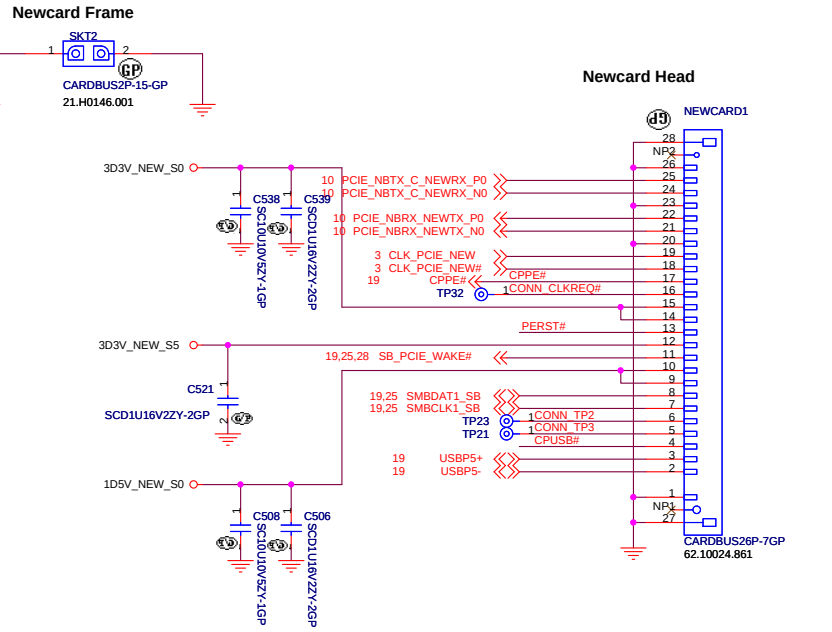
Date: Monday, March 10, 2008 | Sheet 22 of 56


Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
CPU SENSOR
VGA SENSOR
SMBUS
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
Due to sourcer request , change 73.01G08.L04 to main source ,
73.07S08.AAG to 2nd source
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
THERMAL G792
P1/P15
SA
Monday, March 10, 2008

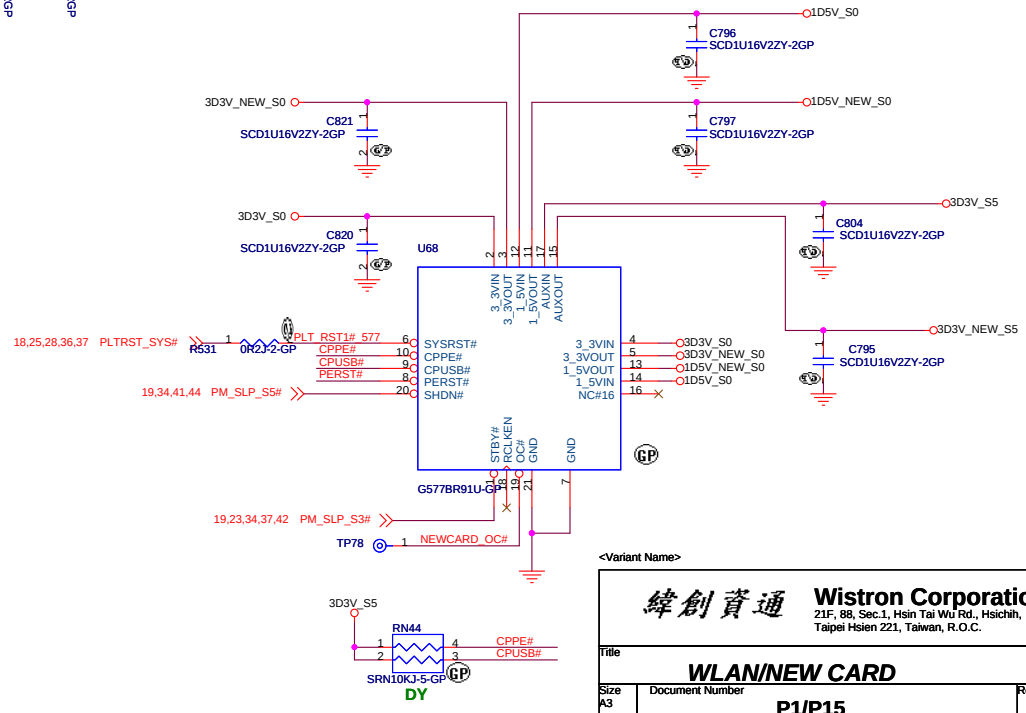
WLAN Connector



NEWCARD Connector



Place them Near to Chip



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***WLAN/NEW CARD***

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 24 of 56

UMA 8101E 71.08101.B0G
DIS 8111C 71.08111.E03
8102E 71.08102.003

3D3V_S5 — G3 GAP-CLOSE-PWR — 3D3V_LAN_S5
60 ~ 100 mils 60 ~ 100 mils

Power domain chart

	RTL8111B / RTL8101E	RTL8111C/ RTL8102E
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q3	Q5
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A
RTL8102E	N/A	N/A

EEPROM LED OPTION USE '01'
(DEFINED IN SPEC)
=> LED0 : ACT
=> LED1 : LINK
(BOTH 10/100 AND GIGA CHIP)

Pin 63 should be near 0.1u F(C494) then 22u F(C493).

The trace width from VDD33 to pin63 should>40mils

The trace length between L39 and 8111C pin1 must be within 200mil.

C471,C472,C473, and C474 as close as possible to RTL8111C

C469 close L39 200mil.

They are for U49 AVDD33 pin-2 and 59

They are for U49 VDD33 pin-16,37,46 and 53

They are for U49 AVDD18 pin-5,8,11 and 14

They are for U49 EVDD18 pin-22 and 28

They are for U49 DVDD15 pin-15,21,32,33,38,41,43,49,52 and 58

8101E REMOVE
8111B REMOVE
8111C STUFF

8111B STUFF CAP
8111C REMOVE CAP

Power plan for pin1

Pin1 should be near inductor(4.7u H,L39) then 22u F(C469) then 0.1u F(C470).

8111C/8102E 2.49K 64.24915.6DL
8101E 2K 64.20015.6DL

RTL8111C-VB-GR-GP
71.08111.C03

8101E/8111B STUFF
8111C REMOVE

8101E/8111B REMOVE
8111C STUFF

8111B STUFF
8111C REMOVE

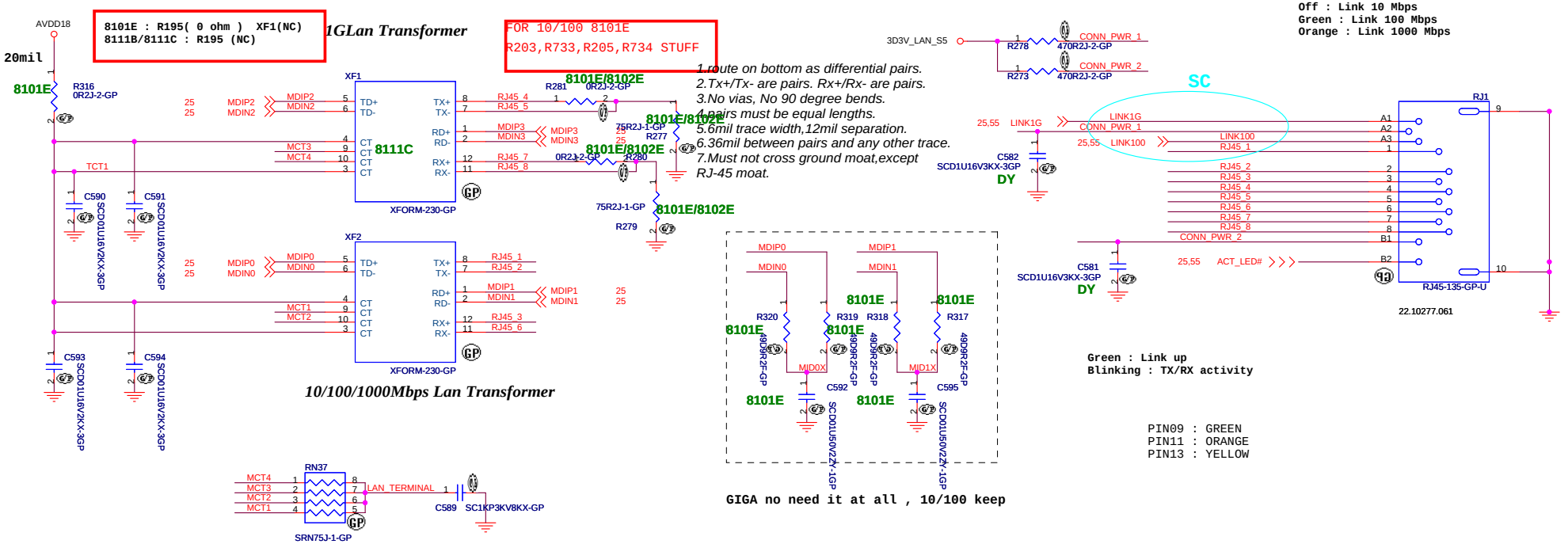
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: LAN 8111C/8101E

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 25 of 56



UMA 8101E 71.08101.B0G
DIS 8111C 71.08111.E03
8102E 71.08102.003

<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

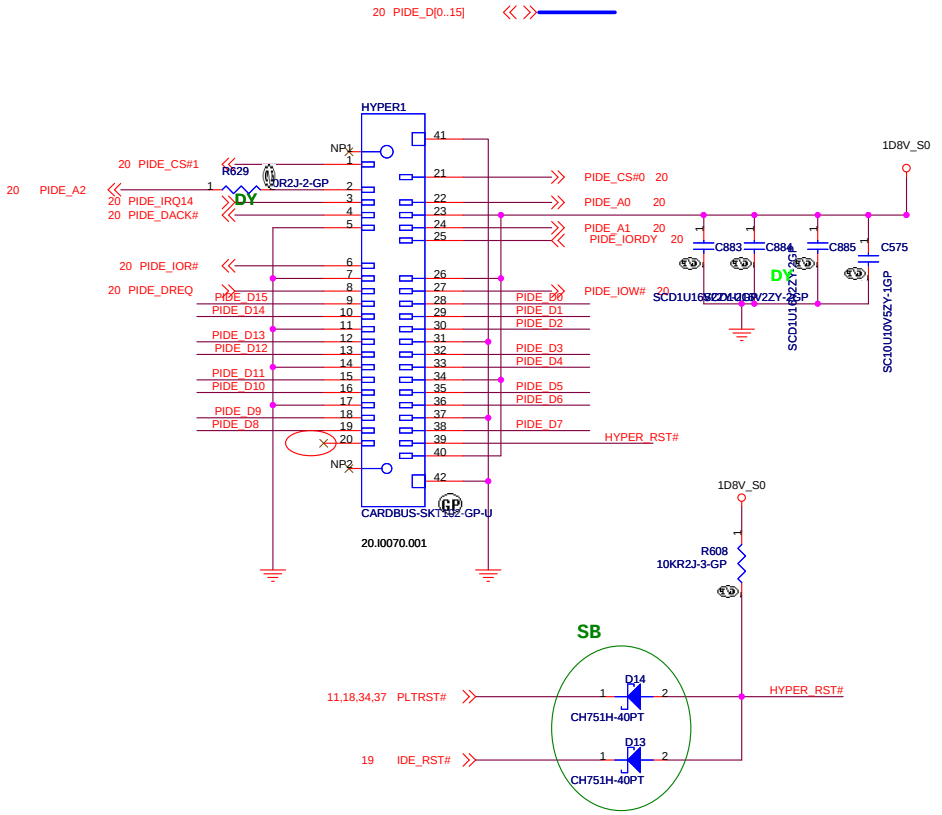
Title: ***LAN Connector***

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 26 of 56

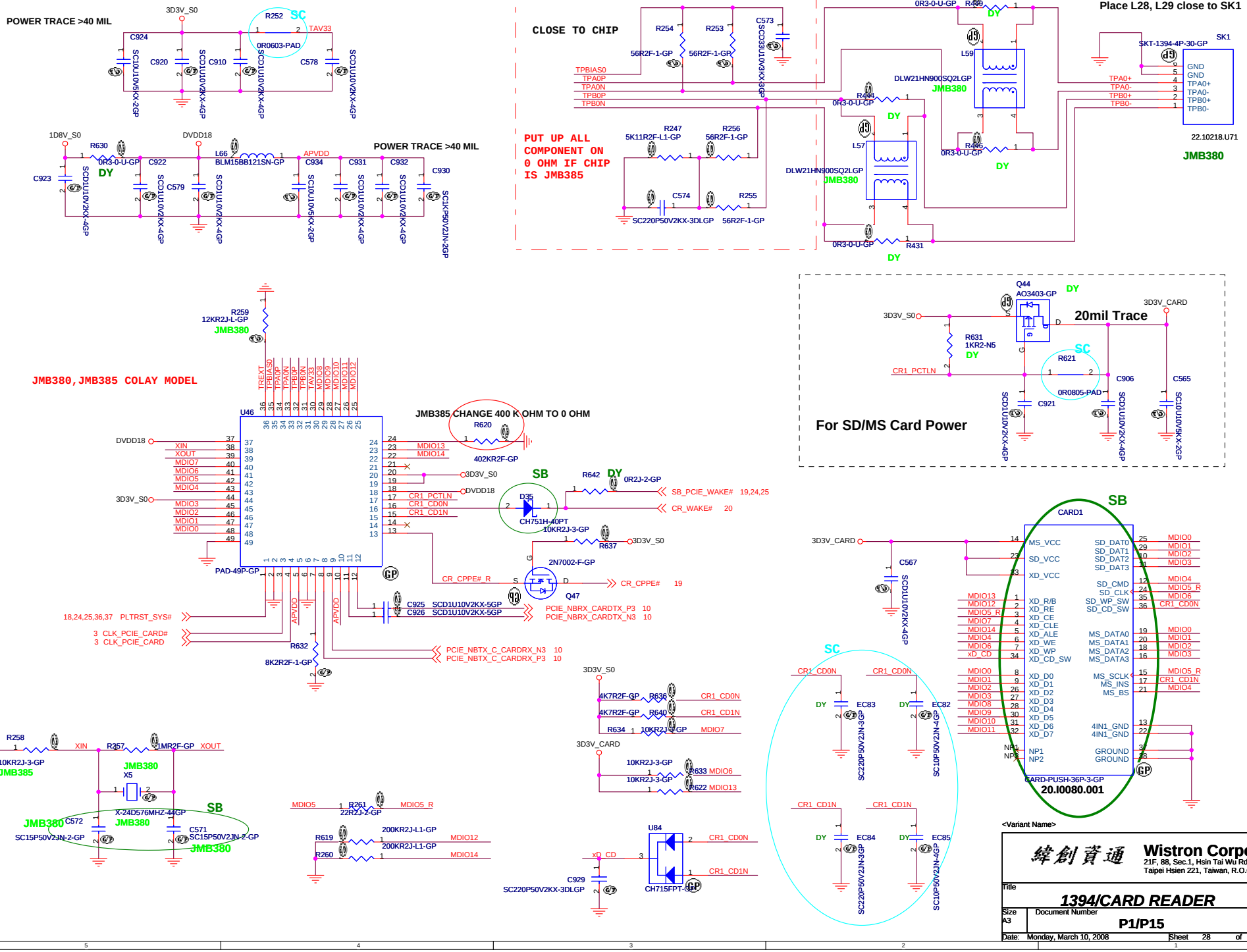
HYPER FLASH

SB DELETE Bluetooth



<Variant Name>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***HYPER FLASH/BT***	
Size A3	Document Number **P1/P15**	Rev **SA**
Date: Monday, March 10, 2008	Sheet 27 of 56	


POWER TRACE >40 MIL
3D3V_S0
R252
SC
TAV33
0R0603-PAD
C924
C920
C910
C578
SC10U10V5KX-2GP
SCD1U10V2KX-4GP
1D8V_S0
DVDD18
R630
0R3-0-U-GP
DY
L66
BLM15BB121SN-GP
APVDD
C922
C579
C934
C931
C932
C930
C923
SC1KP50V2JN-2GP
CLOSE TO CHIP
R254
R253
56R2F-1-GP
C573
SCD33U10V3KX-3GP
TPBIAS0
TPA0P
TPA0N
TPB0P
TPB0N
PUT UP ALL COMPONENT ON 0 OHM IF CHIP IS JMB385
R247
5K11R2F-L1-GP
R256
R255
C574
SC220P50V2KX-3DLGP
0R3-0-U-GP
R429
R430
R431
L59
L57
DLW21HN900SQ2LGP
JMB380
Place L28, L29 close to SK1
SK1
SKT-1394-4P-30-GP
GND
TPA0+
TPA0-
TPB0+
TPB0-
22.10218.U71
JMB380
JMB380,JMB385 COLAY MODEL
R259
12KR2J-L-GP
U46
PAD-49P-GP
XIN
XOUT
MDIO7
MDIO6
MDIO5
MDIO4
MDIO3
MDIO2
MDIO1
MDIO0
MDIO13
MDIO14
JMB385 CHANGE 400 K OHM TO 0 OHM
R620
402KR2F-GP
SB
R642
0R2J-2-GP
SB_PCIE_WAKE#
CR_WAKE#
D35
CH751H-40PT
10KR2J-3-GP
R637
2N7002-F-GP
Q47
CR_CPPE#_R
CR_CPPE#
PLTRST_SYS#
CLK_PCIE_CARD#
CLK_PCIE_CARD
C925
C926
SCD1U10V2KX-5GP
PCIE_NBRX_CARDTX_P3
PCIE_NBRX_CARDTX_N3
R632
8K2R2F-1-GP
PCIE_NBTX_C_CARDRX_N3
PCIE_NBTX_C_CARDRX_P3
For SD/MS Card Power
Q44
AO3403-GP
20mil Trace
3D3V_CARD
R631
1KR2-N5
CR1_PCTLN
R621
0R0805-PAD
C906
C565
C921
SCD1U10V2KX-4GP
SC10U10V5KX-2GP
CARD1
SD_DAT0
SD_DAT1
SD_DAT2
SD_DAT3
SD_CMD
SD_CLK
SD_WP_SW
SD_CD_SW
MS_DATA0
MS_DATA1
MS_DATA2
MS_DATA3
MS_SCLK
MS_INS
MS_BS
XD_R/B
XD_RE
XD_CE
XD_CLE
XD_ALE
XD_WE
XD_WP
XD_CD_SW
XD_D0
XD_D1
XD_D2
XD_D3
XD_D4
XD_D5
XD_D6
XD_D7
4IN1_GND
GROUND
NP1
NP2
CARD-PUSH-36P-3-GP
20.I0080.001
C567
EC83
EC82
EC84
EC85
SC220P50V2JN-3GP
SC10P50V2JN-4GP
SC10P50V2JN-2GP
R258
10KR2J-3-GP
JMB385
R257
1MR2F-GP
X5
X-24D576MHZ-44GP
C572
C571
SC15P50V2JN-2GP
R261
22R2J-2-GP
R619
R260
200KR2J-L1-GP
4K7R2F-GP
R636
R640
R634
R633
R622
U84
CH715FPT-GP
C929
SC220P50V2KX-3DLGP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1394/CARD READER
Size A3
Document Number
P1/P15
Rev SA
Date: Monday, March 10, 2008
Sheet 28 of 56

400uS rise time
Supply 2~1.5A

100 mil

5V_S5

U24

IN#3 IN#2 OUT#8 OUT#7 OUT#6 OC# EN/EN# GND

G545A2P8U-GP

34 USB_PWR_EN# → USB_PWR_EN#

C617 SC1U16V3ZY-GP

5V_S5 C641 SC10U25V6KX-1GP

5V_USB1_S3

100 mil

SCD1U16V2KX-3GP

C130 C134 C136 SC47U6D3V6MX-1GP

SC10U25V6KX-1GP

400uS rise time
Supply 1.5~1.1A

50 mil

5V_S5

U58

GND IN#2 IN#3 EN/EN# OUT#8 OUT#7 NC#6 OC#

G545B2P8U-GP

USB_PWR_EN#

C655 SC1U16V3ZY-GP

5V_S5 C144 SC10U25V6KX-1GP

5V_USB2_S3

50 mil

SC10U25V6KX-1GP C667

SC1KP50V2KX-1GP C676

5V_USB1_S3

100 mil

C626 SCD1U16V2ZY-2GP

USB1

19 USBP1+
19 USBP1-
19 USBP2+
19 USBP2-

ACES-CON15-GP

20.K0228.015

1D8V_S0

DY

C946 SC4D7U10V5ZY-3GP

C947 SCD1U10V2KX-4GP

C938 SCD1U10V2KX-4GP

C939 SCD1U10V2KX-4GP

U85

VDD VDD VDD VDD VDD

EQA EQB

BO- BO+

AO- AO+

AI- AI+

EN

GND GND GND GND

PI2EQX3211BHE-GP

C944 SC4700P50V2KX-1GP

SATA_TX3- RBB
SATA_TX3+ RBB
C942 SC4700P50V2KX-1GP

SATA_TX3- RB
SATA_TX3+ RB

20 SATA_TX3-_R
20 SATA_TX3+_R

R665 10KR2J-3GP → 1D8V_S0

SATA_TX3+_RB → R667 470R2J-2GP → SATA_TX3-_RB

put close to connector

1D8V_S0

R662 10KR2J-3-GP DY
R660 10KR2J-3-GP DY
R663 10KR2J-3-GP DY
R664 10KR2J-3-GP DY

EQA EQB

SATA_RX3- 20
SATA_RX3+ 20

SATA_RX3- RB → C943 SC4700P50V2KX-1GP → SATA_RX3- RBB
SATA_RX3+ RB → C941 SC4700P50V2KX-1GP → SATA_RX3+ RBB

R671 0R2J-2-GP: SATA_RX3+_RB → SATA_RX3+
R672 0R2J-2-GP: SATA_RX3-_RB → SATA_RX3-
R673 0R2J-2-GP: SATA_TX3+_RB → SATA_TX3+_R
R674 0R2J-2-GP: SATA_TX3-_RB → SATA_TX3-_R

put at the U85 bottom

R398 0R2J-2-GP

19 USBP0- → TR1 DLW21HN900SQ2LGP → USBP0-_RR
19 USBP0+ → TR1 DLW21HN900SQ2LGP → USBP0+_RR

R407 0R2J-2-GP

DY

U27

USBP0-_RR → I/O2
I/O1 → USBP0+_RR
5V_USB2_S3
VREF GND

PJSR05-GP

5V_USB2_S3

USB2

NP1 NP2

1A 2A 3A 4A

USBP0-_RR
USBP0+_RR

SATA_RX3+_RBB
SATA_RX3-_RBB
SATA_TX3-_RBB
SATA_TX3+_RBB

TC6 ST100U10VDM-5GP

SKT-SATA+USB11P-GP

22.10218.Z71

SC

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB/ESATA CONN

Size	Document Number	Rev
A3	P1/P15	SA

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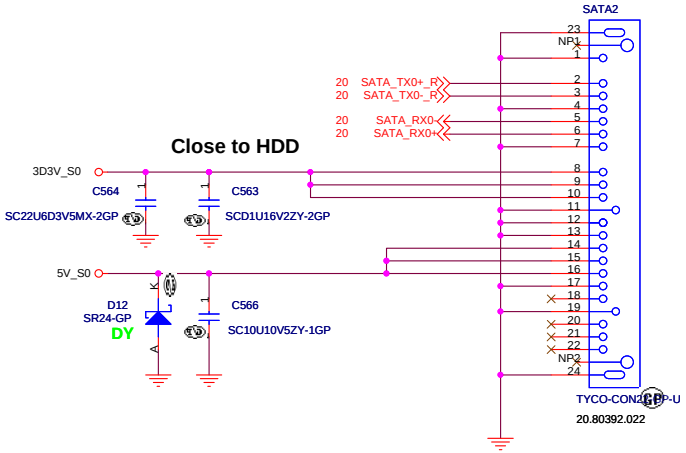
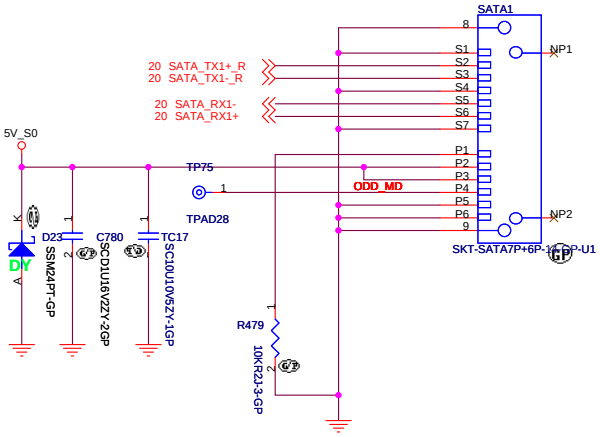
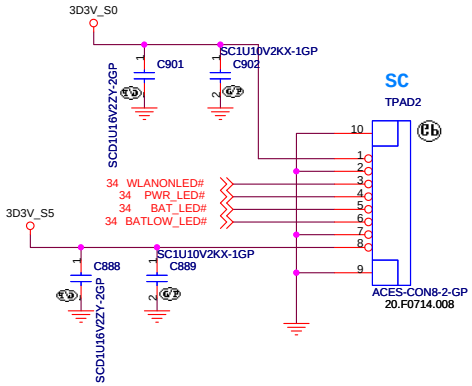
SATA HDD Connector



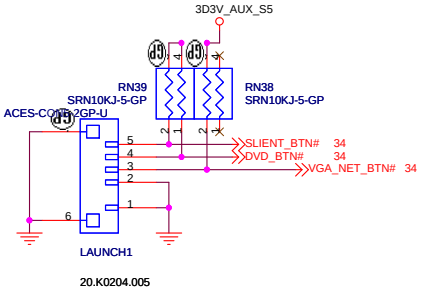
SATA ODD Connector



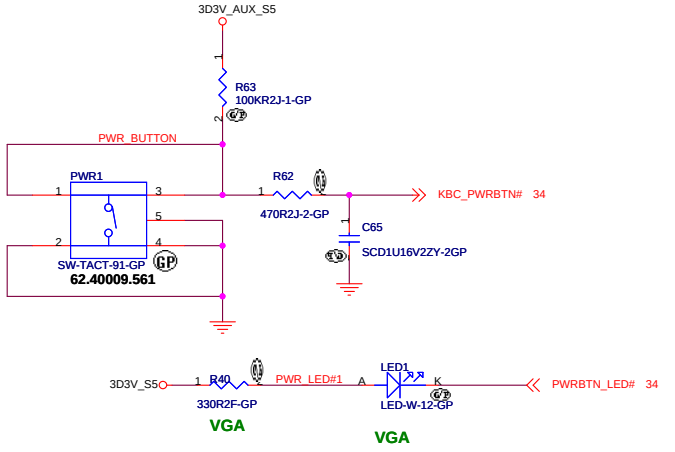
LED BD CONN

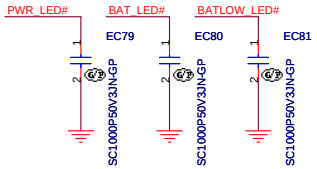


LAUNCH BD CONN



POWER BUTTON





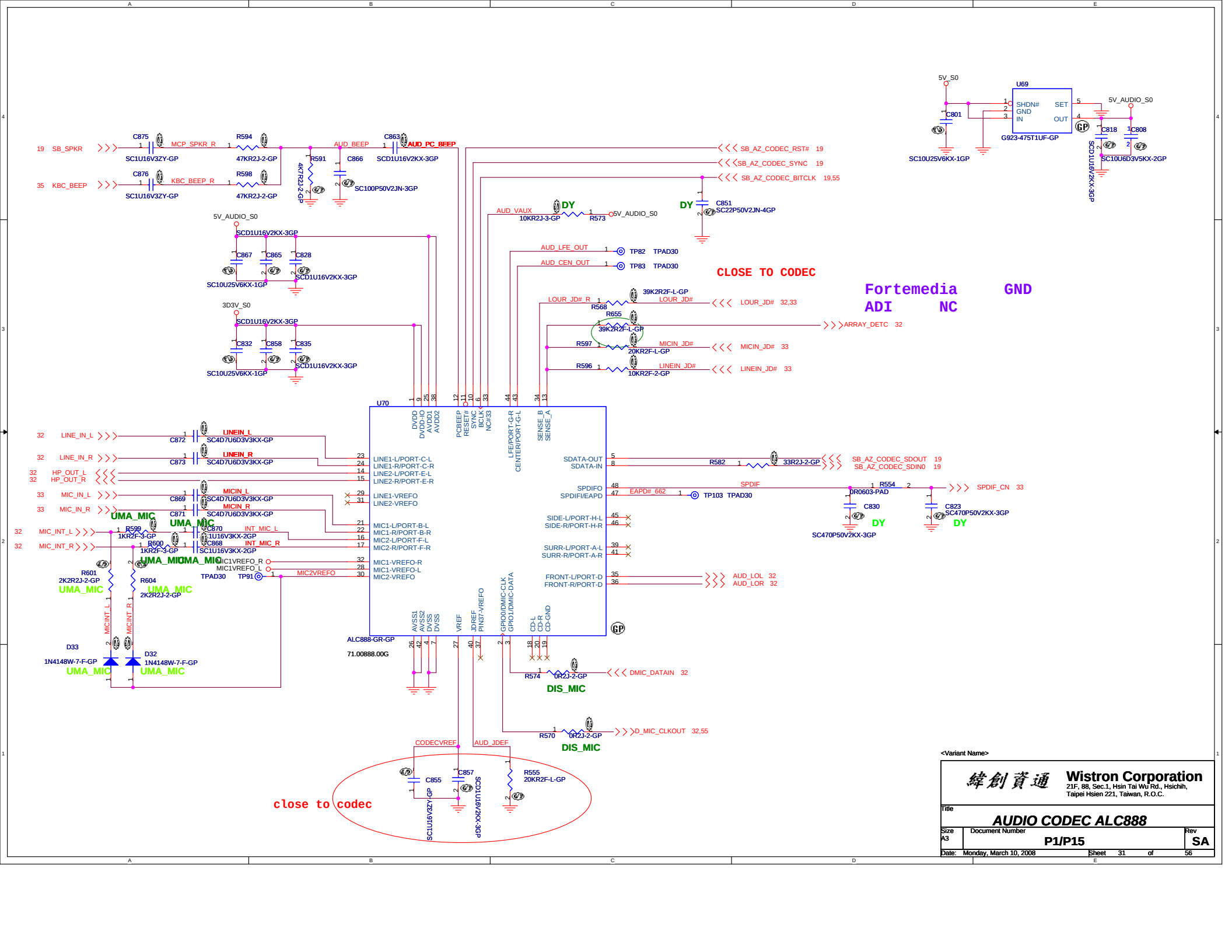
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

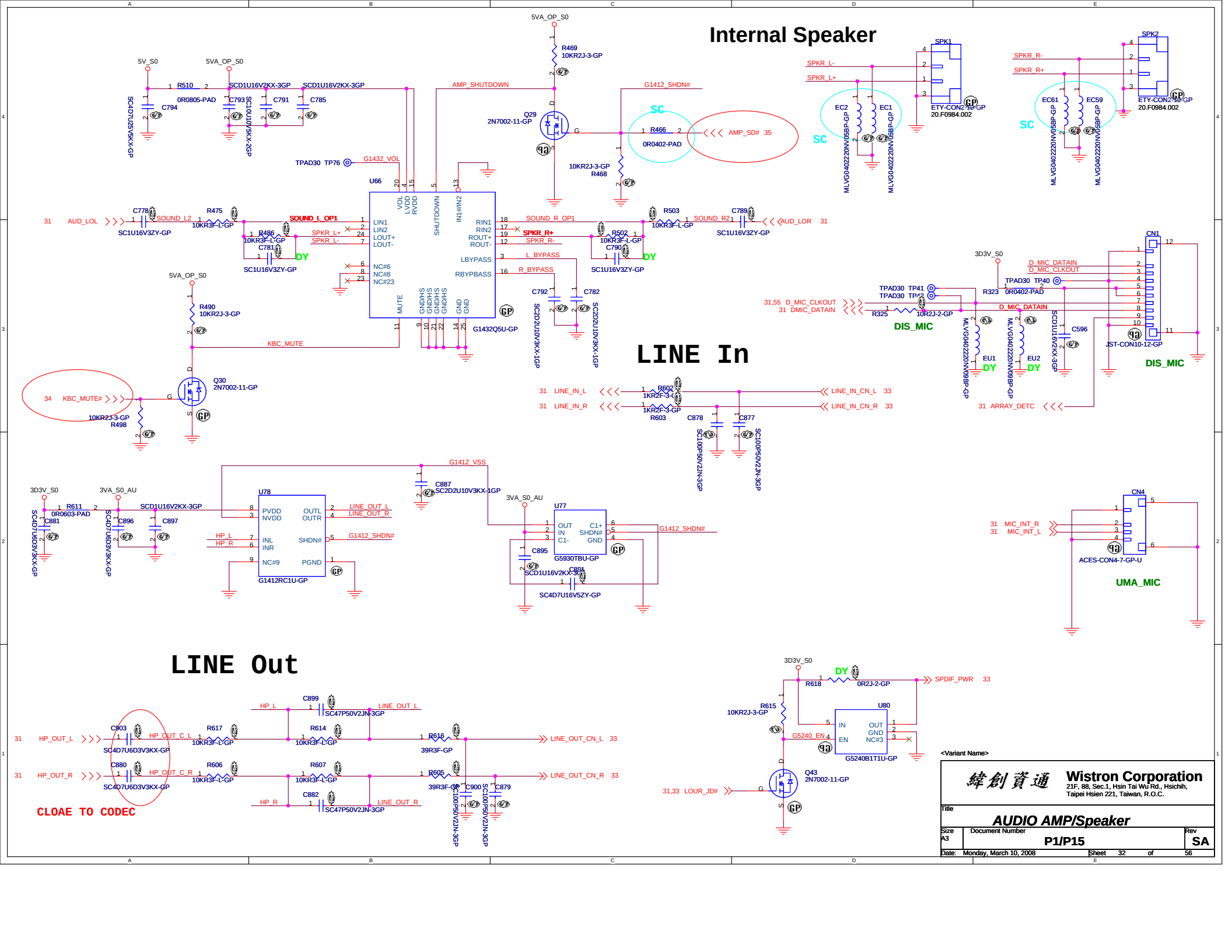
Title: ***HDD/CDROM/LED/LAUNCH***

Size	Document Number	Rev
A3	P1/P15	SA

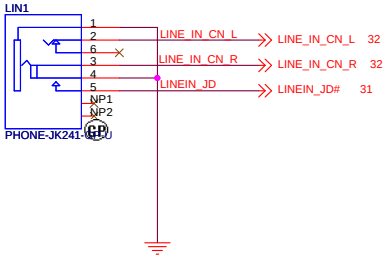
Date: Monday, March 10, 2008 Sheet 30 of 56


U70
ALC888-GR-GP
71.00888.00G
U69
G923-475T1UF-GP
SB_SPKR
KBC_BEEP
MCP_SPKR_R
KBC_BEEP_R
AUD_BEEP
AUD_PC_BEEP
SB_AZ_CODEC_RST# 19
SB_AZ_CODEC_SYNC 19
SB_AZ_CODEC_BITCLK 19,55
AUD_VAUX
AUD_LFE_OUT
AUD_CEN_OUT
LOUR_JD# R
LOUR_JD# 32,33
ARRAY_DETC 32
MICIN_JD# 33
LINEIN_JD# 33
LINE_IN_L
LINE_IN_R
HP_OUT_L
HP_OUT_R
MIC_IN_L
MIC_IN_R
MIC_INT_L
MIC_INT_R
LINEIN_L
LINEIN_R
MICIN_L
MICIN_R
INT_MIC_L
INT_MIC_R
MIC2VREFO
SDATA-OUT 5
SDATA-IN 8
SB_AZ_CODEC_SDOUT 19
SB_AZ_CODEC_SDIN0 19
SPDIFO 48
SPDIFI/EAPD 47
SPDIF
SPDIF_CN 33
EAPD#_662
TP103 TPAD30
SIDE-L/PORT-H-L 45
SIDE-R/PORT-H-R 46
SURR-L/PORT-A-L 39
SURR-R/PORT-A-R 41
FRONT-L/PORT-D 35
FRONT-R/PORT-D 36
AUD_LOL 32
AUD_LOR 32
DMIC_DATAIN 32
D_MIC_CLKOUT 32,55
DIS_MIC
UMA_MIC
CODECVREF
AUD_JDEF
close to codec
CLOSE TO CODEC
Fortemedia GND
ADI NC
5V_S0
5V_AUDIO_S0
3D3V_S0
DY
TP82 TPAD30
TP83 TPAD30
TP91
TPAD30

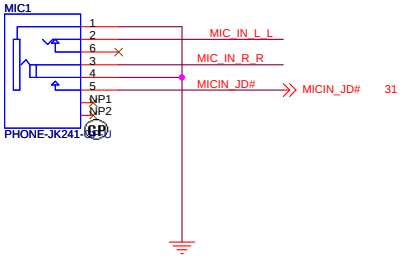
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC888
Size A3
Document Number
P1/P15
Rev SA
Date: Monday, March 10, 2008
Sheet 31 of 56

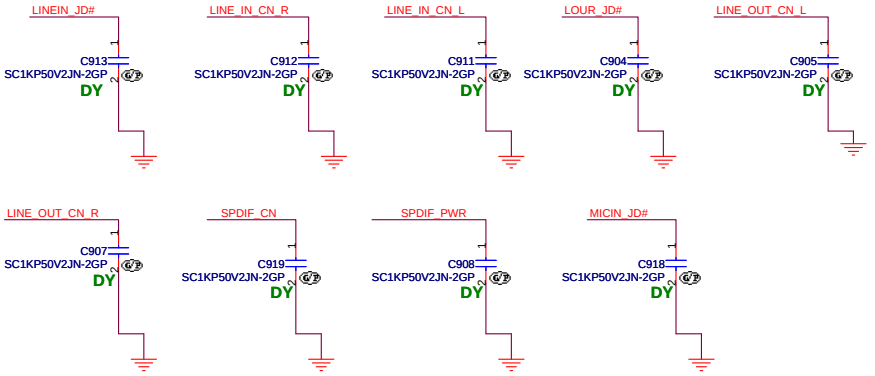

Internal Speaker
LINE In
LINE Out
5V_S0
5VA_OP_S0
3D3V_S0
3VA_S0_AU
R510
0R0805-PAD
SCD1U16V2KX-3GP
C794
C793
C791
C785
R469
10KR2J-3-GP
AMP_SHUTDOWN
G1412_SHDN#
Q29
2N7002-11-GP
R466
0R0402-PAD
AMP_SD# 35
10KR2J-3-GP
R468
TPAD30 TP76
G1432_VOL
U66
G1432Q5U-GP
C778
R475
SOUND_L2
SOUND_L_OP1
10KR3F-L-GP
R486
SPKR_L+
SPKR_L-
C781
SC1U16V3ZY-GP
DY
LIN1
LIN2
LOUT+
LOUT-
NC#6
NC#8
NC#23
VOL
LVDD
RVDD
SHUTDOWN
IN1#/IN2
RIN1
RIN2
ROUT+
ROUT-
LBYPASS
RBYPASS
MUTE
GND/HS
GND
SOUND_R_OP1
SPKR_R+
SPKR_R-
L_BYPASS
R_BYPASS
R503
SOUND_R2
C789
AUD_LOR 31
R502
C790
C792
C782
SC2D2U10V3KX-1GP
R490
10KR2J-3-GP
KBC_MUTE
Q30
2N7002-11-GP
34 KBC_MUTE#
R498
SPK1
SPKR_L-
SPKR_L+
EC2
EC1
MLVG0402220NV05BP-GP
ETY-CON2-10-GP
20.F0984.002
SPK2
SPKR_R-
SPKR_R+
EC61
EC59
R611
0R0603-PAD
C881
C896
C897
SC4D7U6D3V3KX-GP
U78
PVDD
NVDD
INL
INR
NC#9
PGND
OUTL
OUTR
SHDN#
LINE_OUT_L
LINE_OUT_R
HP_L
HP_R
G1412_SHDN#
G1412RC1U-GP
G1412_VSS
C887
SC2D2U10V3KX-1GP
U77
OUT
IN
C1-
C1+
SHDN#
GND
G5930TBU-GP
C895
C891
SC4D7U16V5ZY-GP
31 LINE_IN_L
31 LINE_IN_R
R602
R603
1KR2F-3-GP
LINE_IN_CN_L 33
LINE_IN_CN_R 33
C878
C877
SC100P50V2JN-3GP
TPAD30 TP41
TPAD30 TP42
31,55 D_MIC_CLKOUT
31 DMIC_DATAIN
R325
10R2J-2-GP
D_MIC_DATAIN
D_MIC_CLKOUT
TPAD30 TP40
R323
0R0402-PAD
EU1
EU2
MLVG0402220NV09BP-GP
C596
SCD1U16V2KX-3GP
CN1
JST-CON10-12-GP
DIS_MIC
31 ARRAY_DETC
CN4
ACES-CON4-7-GP-U
31 MIC_INT_R
31 MIC_INT_L
UMA_MIC
31 HP_OUT_L
31 HP_OUT_R
C903
C880
HP_OUT_C_L
HP_OUT_C_R
R617
R606
10KR3F-L-GP
SC4D7U6D3V3KX-GP
CLOAE TO CODEC
C899
C882
SC47P50V2JN-3GP
R614
R607
R616
R605
39R3F-GP
LINE_OUT_CN_L 33
LINE_OUT_CN_R 33
C900
C879
SC100P50V2JN-3GP
R618
0R2J-2-GP
SPDIF_PWR 33
R615
10KR2J-3-GP
U80
G5240_EN
G5240B1T1U-GP
Q43
2N7002-11-GP
31,33 LOUR_JD#
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO AMP/Speaker
Size A3
Document Number
P1/P15
Rev SA
Date: Monday, March 10, 2008
Sheet 32 of 56

LINE IN

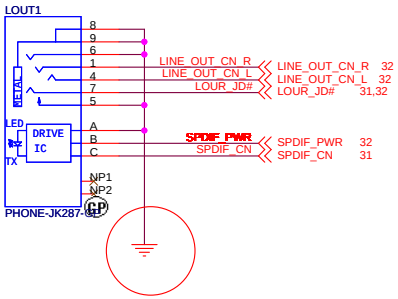


MIC IN



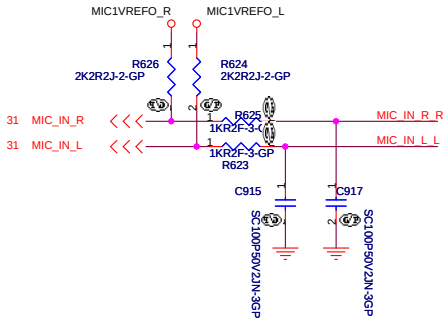


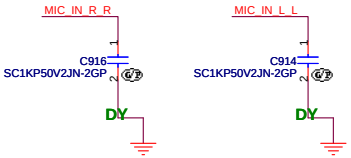
SPDIF / LINE OUT



ANALOG/GIGITAL GROUND SEPARATE

MIC In





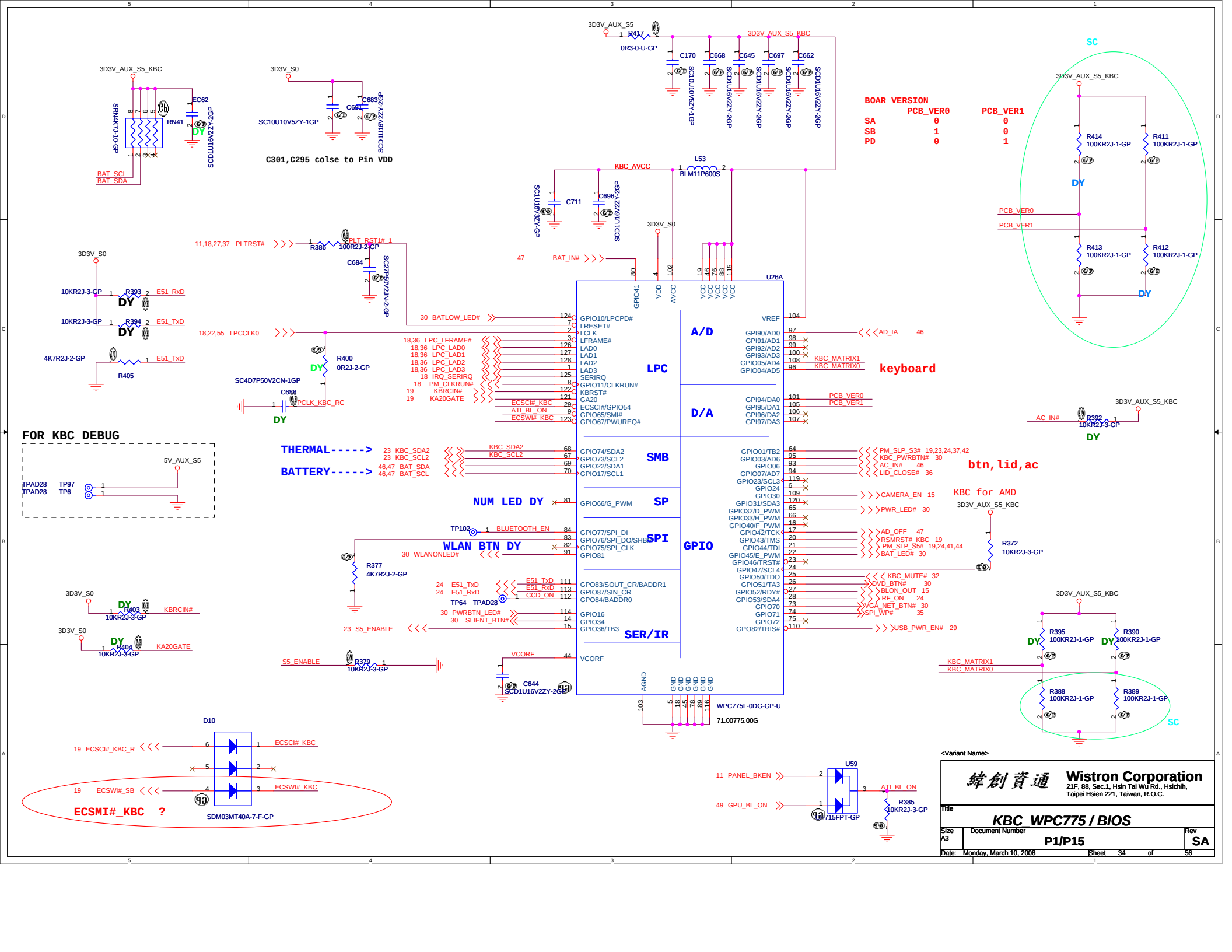
<Variant Name>

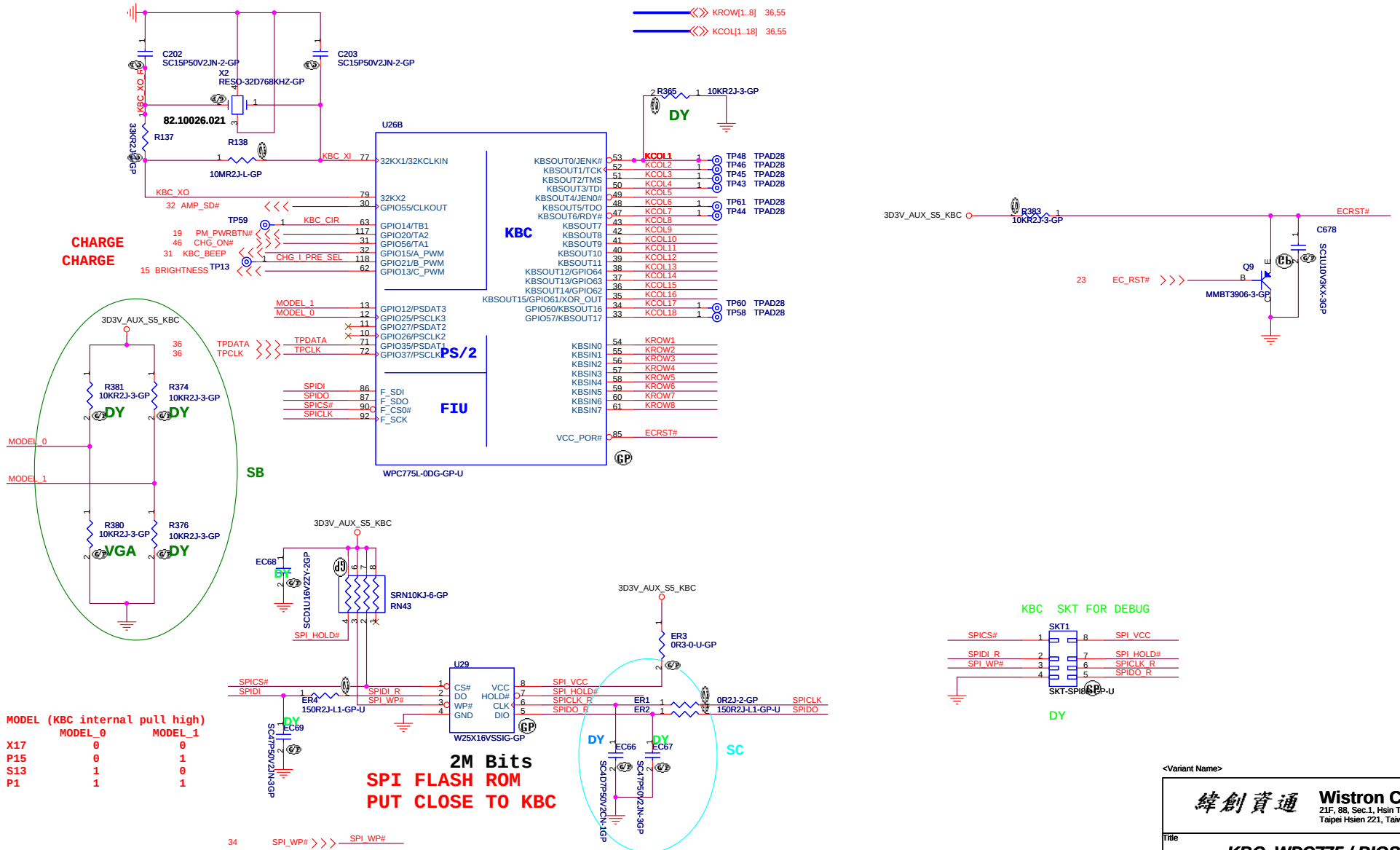
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: AUDIO CONN/SUBWOOFER

Size: A3 | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 33 of 56

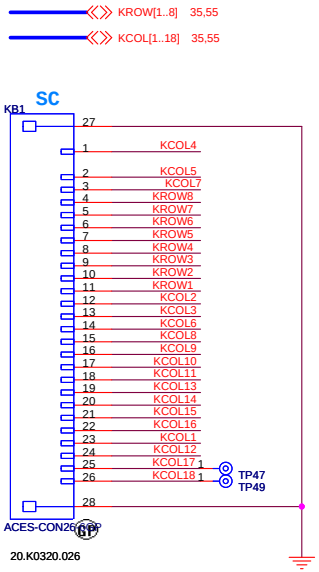

3D3V_AUX_S5
R417
0R3-0-U-GP
3D3V_AUX_S5_KBC
C170
C668
C645
C697
C662
SCD1U16V2ZY-2GP
3D3V_S0
C683
C691
SC10U10V5ZY-1GP
C301,C295 colse to Pin VDD
SRN4K7J-10-GP
RN41
EC62
DY
BAT_SCL
BAT_SDA
KBC_AVCC
L53
BLM11P600S
C711
C696
SC1U16V2ZY-1GP
BOAR VERSION
PCB_VER0
PCB_VER1
SA 0 0
SB 1 0
PD 0 1
SC
R414 100KR2J-1-GP
R411 100KR2J-1-GP
R413 100KR2J-1-GP
R412 100KR2J-1-GP
PCB_VER0
PCB_VER1
11,18,27,37 PLTRST#
R386
PLT_RST1#_1
100R2J-2-GP
C684
SC27P50V2JN-2GP
47 BAT_IN#
U26A
GPIO41
VDD
AVCC
VCC
10KR2J-3-GP
R393
R394
E51_RxD
E51_TxD
4K7R2J-2-GP
R405
18,22,55 LPCCLK0
R400
0R2J-2-GP
SC4D7P50V2CN-1GP
C688
LPCCLK_KBC_RC
30 BATLOW_LED#
18,36 LPC_LFRAME#
18,36 LPC_LAD0
18,36 LPC_LAD1
18,36 LPC_LAD2
18,36 LPC_LAD3
18 IRQ_SERIRQ
18 PM_CLKRUN#
19 KBRCIN#
19 KA20GATE
ECSCI# KBC
ATI_BL_ON
ECSWI# KBC
GPIO10/LPCPD#
LRESET#
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
GPIO11/CLKRUN#
KBRST#
GA20
ECSCI#/GPIO54
GPIO65/SMI#
GPIO67/PWUREQ#
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
VREF
GPI90/AD0
GPI91/AD1
GPI92/AD2
GPI93/AD3
GPIO05/AD4
GPIO04/AD5
AD_IA 46
KBC_MATRIX1
KBC_MATRIX0
keyboard
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
PCB_VER0
PCB_VER1
3D3V_AUX_S5_KBC
AC_IN#
R392
10KR2J-3-GP
DY
FOR KBC DEBUG
5V_AUX_S5
TPAD28
TP97
TP6
THERMAL-----> 23 KBC_SDA2 23 KBC_SCL2
BATTERY-----> 46,47 BAT_SDA 46,47 BAT_SCL
KBC_SDA2
KBC_SCL2
GPIO74/SDA2
GPIO73/SCL2
GPIO22/SDA1
GPIO17/SCL1
NUM LED DY
GPIO66/G_PWM
GPIO01/TB2
GPIO03/AD6
GPIO06
GPIO07/AD7
GPIO23/SCL3
GPIO24
GPIO30
GPIO31/SDA3
GPIO32/D_PWM
GPIO33/H_PWM
GPIO40/F_PWM
GPIO42/TCK
GPIO43/TMS
GPIO44/TDI
GPIO45/E_PWM
GPIO46/TRST#
GPIO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/RDY#
GPIO53/SDA4
GPIO70
GPIO71
GPIO72
GPIO82/TRIS#
PM_SLP_S3# 19,23,24,37,42
KBC_PWRBTN# 30
AC_IN# 46
LID_CLOSE# 36
btn,lid,ac
KBC for AMD
CAMERA_EN 15
PWR_LED# 30
AD_OFF 47
RSMRST#_KBC 19
PM_SLP_S5# 19,24,41,44
BAT_LED# 30
KBC_MUTE# 32
DVD_BTN# 30
BLON_OUT 15
RF_ON 24
WGA_NET_BTN# 30
SPI_WP# 35
USB_PWR_EN# 29
TP102
BLUETOOTH_EN
WLAN BTN DY
30 WLANONLED#
R377
4K7R2J-2-GP
24 E51_TxD
24 E51_RxD
TP64 TPAD28
CCD_ON
GPO83/SOUT_CR/BADDR1
GPIO87/SIN_CR
GPO84/BADDR0
30 PWRBTN_LED#
30 SLIENT_BTN#
GPIO16
GPIO34
GPIO36/TB3
23 S5_ENABLE
S5_ENABLE
R379
10KR2J-3-GP
VCORF
C644
SCD1U16V2ZY-2GP
AGND
GND
WPC775L-0DG-GP-U
71.00775.00G
R403
R404
KBRCIN#
KA20GATE
R372
10KR2J-3-GP
R395 100KR2J-1-GP
R390 100KR2J-1-GP
R388 100KR2J-1-GP
R389 100KR2J-1-GP
KBC_MATRIX1
KBC_MATRIX0
D10
19 ECSCI#_KBC_R
19 ECSWI#_SB
ECSCI#_KBC
ECSWI#_KBC
ECSMI#_KBC ?
SDM03MT40A-7-F-GP
U59
11 PANEL_BKEN
49 GPU_BL_ON
ATI_BL_ON
R385
10KR2J-3-GP
W715FPT-GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_WPC775 / BIOS
Size A3
Document Number
P1/P15
Rev SA
Date: Monday, March 10, 2008
Sheet 34 of 56

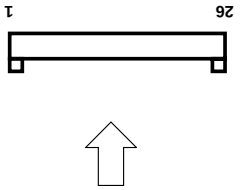


<variant_name>

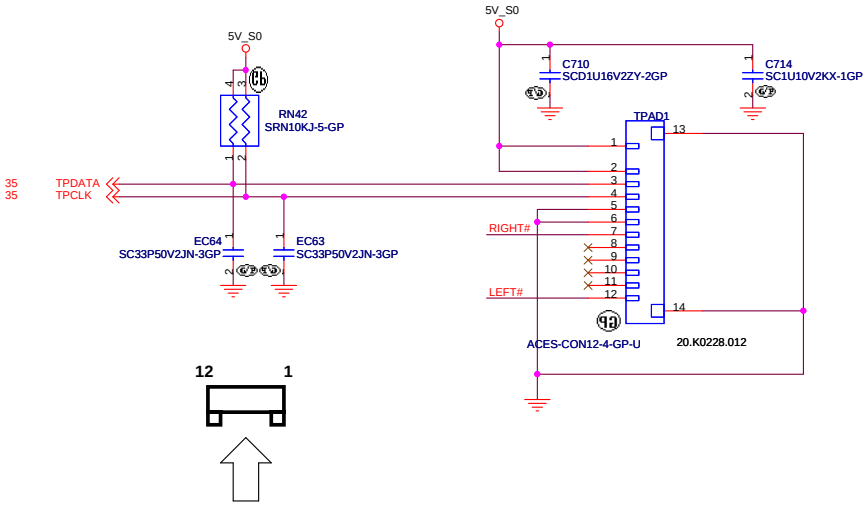
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: KBC_WPC775 / BIOS(2/2)		
Size: A3	Document Number: P1/P15	Rev: SA
Date: Monday, March 10, 2008	Sheet 35 of 56	

Internal KeyBoard Connector

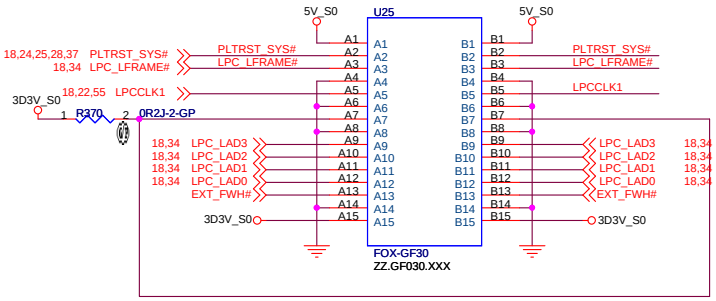




TouchPad Connector



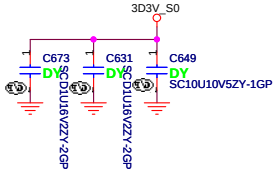
GOLDEN FINGER FOR DEBUG BOARD



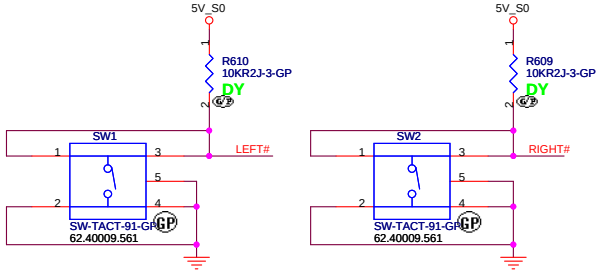
TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

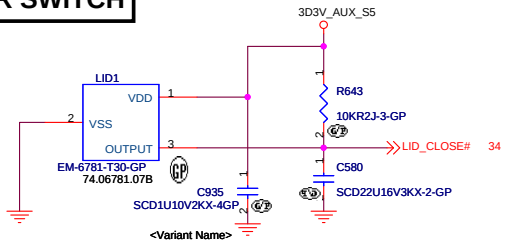
(BOTTOM VIEW)



15" TOUCHPAD BUTTON SWITCH



COVER SWITCH



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KEYBOARD/TPAD/DEBUG/LID**

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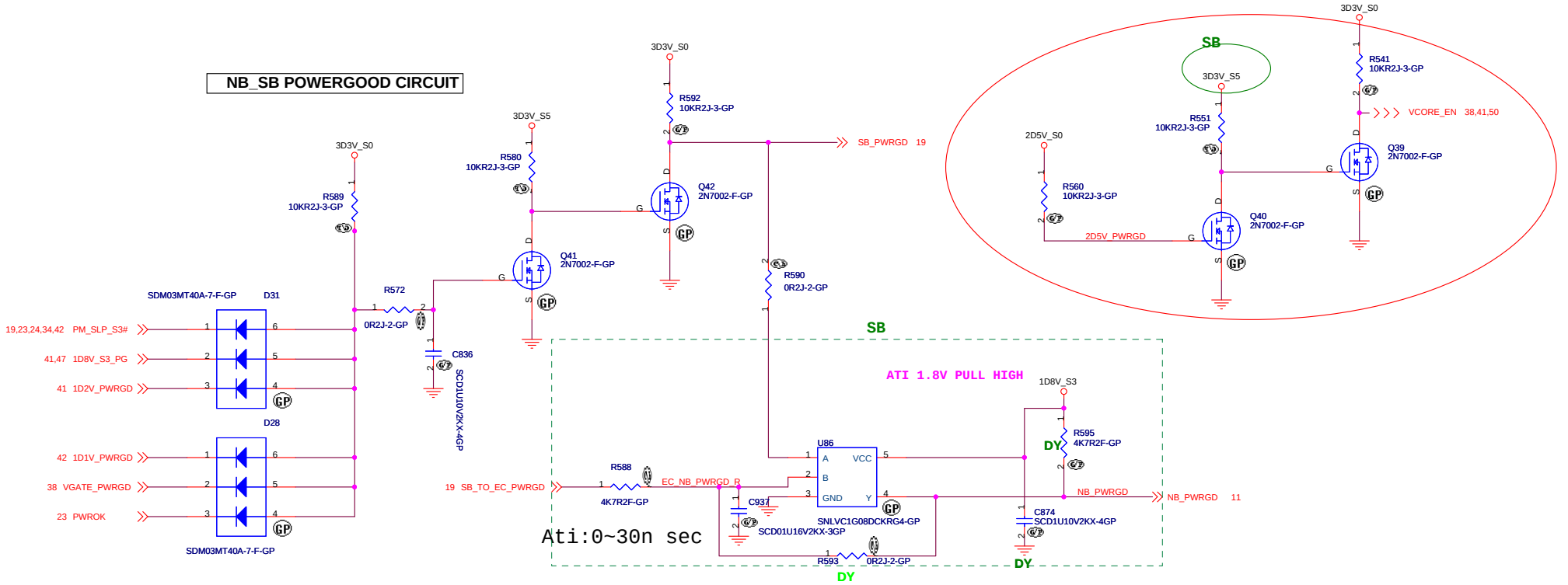
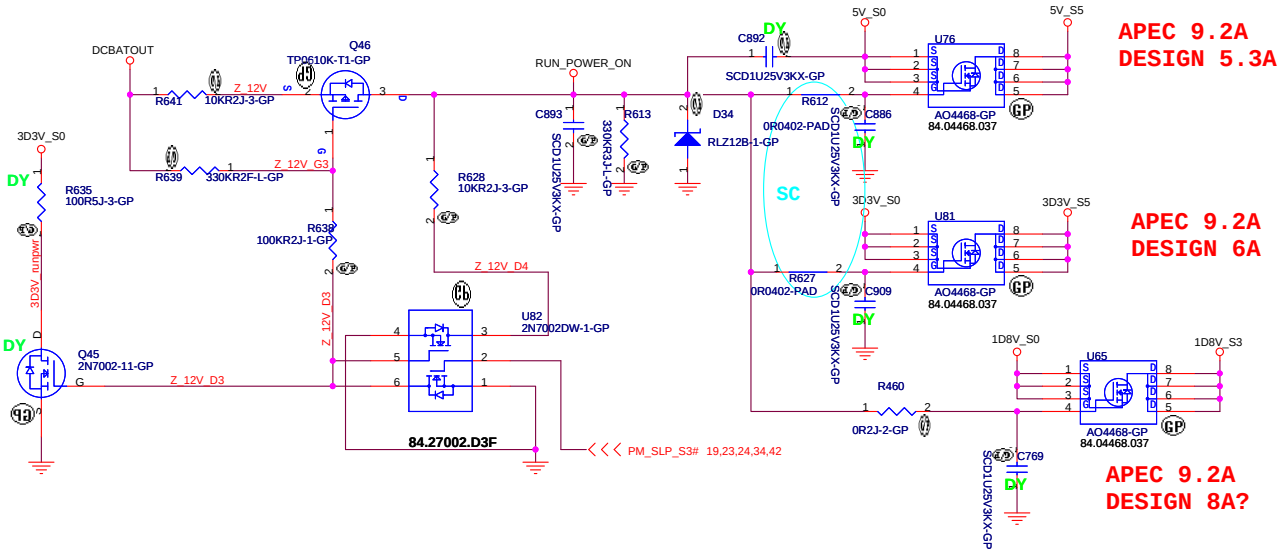
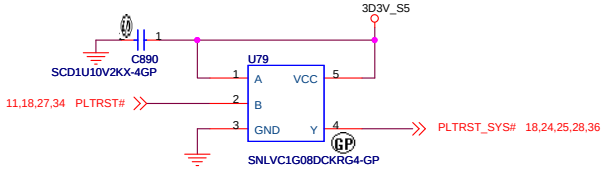
NB_SB POWERGOOD CIRCUIT



Run Power





<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***RUNPOWER***

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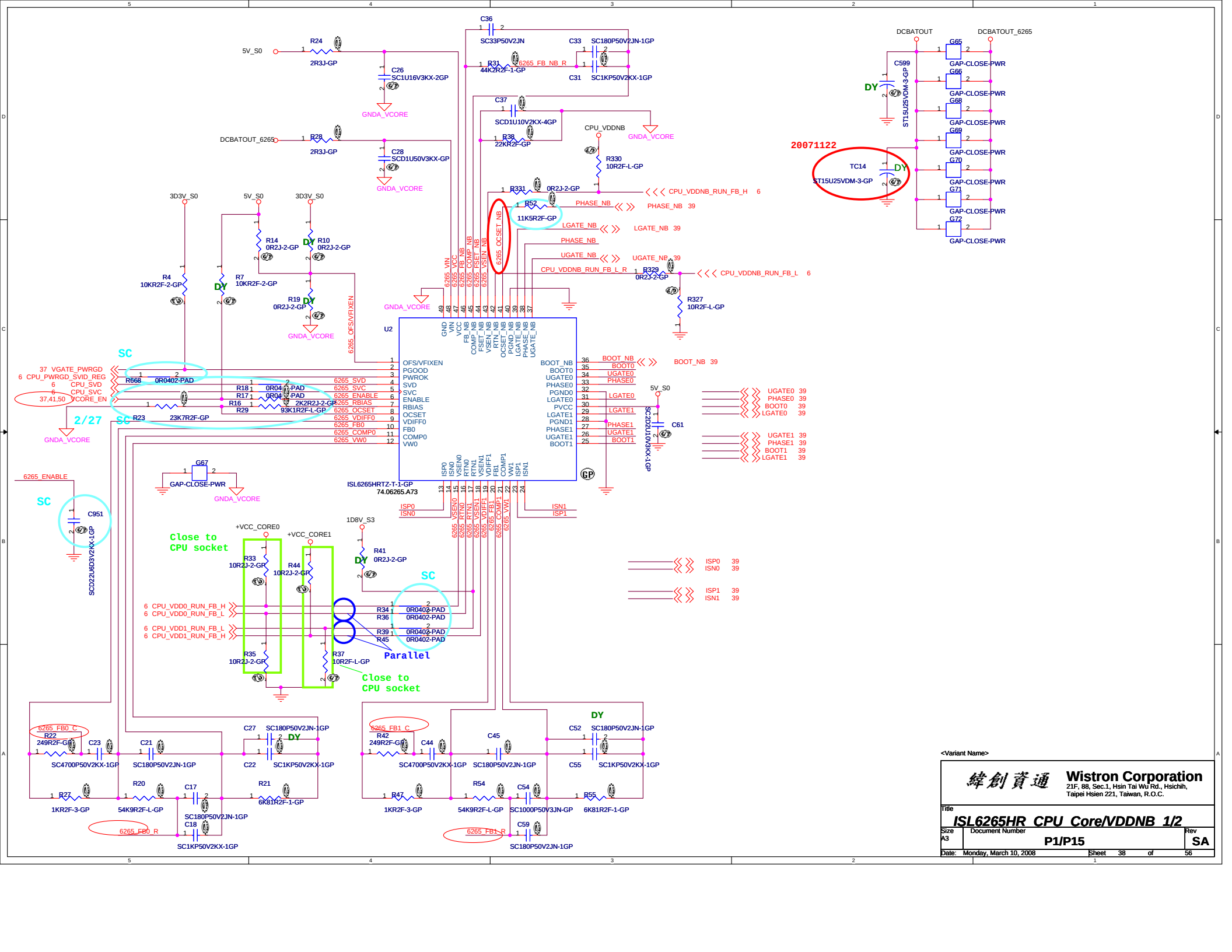
U2
ISL6265HRTZ-T-1-GP
74.06265.A73
OFS/VFIXEN
PGOOD
PWROK
SVD
SVC
ENABLE
RBIAS
OCSET
VDIFF0
FB0
COMP0
VW0
BOOT_NB
BOOT0
UGATE0
PHASE0
PGND0
LGATE0
PVCC
LGATE1
PGND1
PHASE1
UGATE1
BOOT1
ISP0
ISN0
VSEN0
RTN0
RTN1
VSEN1
VDIFF1
FB1
COMP1
VW1
ISP1
ISN1
GND
VIN
VCC
FB_NB
COMP_NB
FSET_NB
VSEN_NB
RTN_NB
OCSET_NB
PGND_NB
LGATE_NB
PHASE_NB
UGATE_NB
SC
DY
Close to CPU socket
Parallel
20071122
TC14
ST15U25VDM-3-GP
DCBATOUT
DCBATOUT_6265
GAP-CLOSE-PWR
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ISL6265HR CPU Core/VDDNB 1/2
P1/P15
SA
Monday, March 10, 2008
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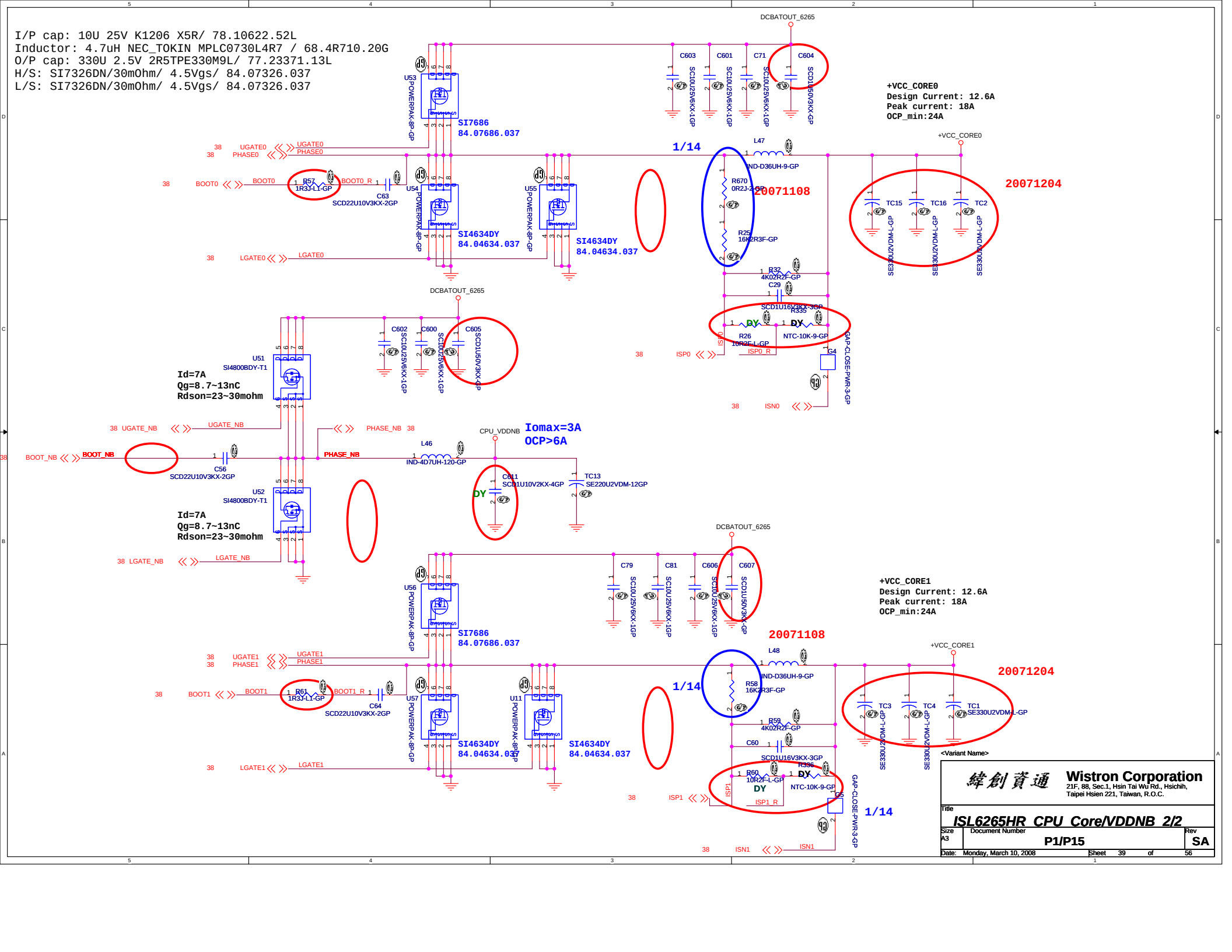
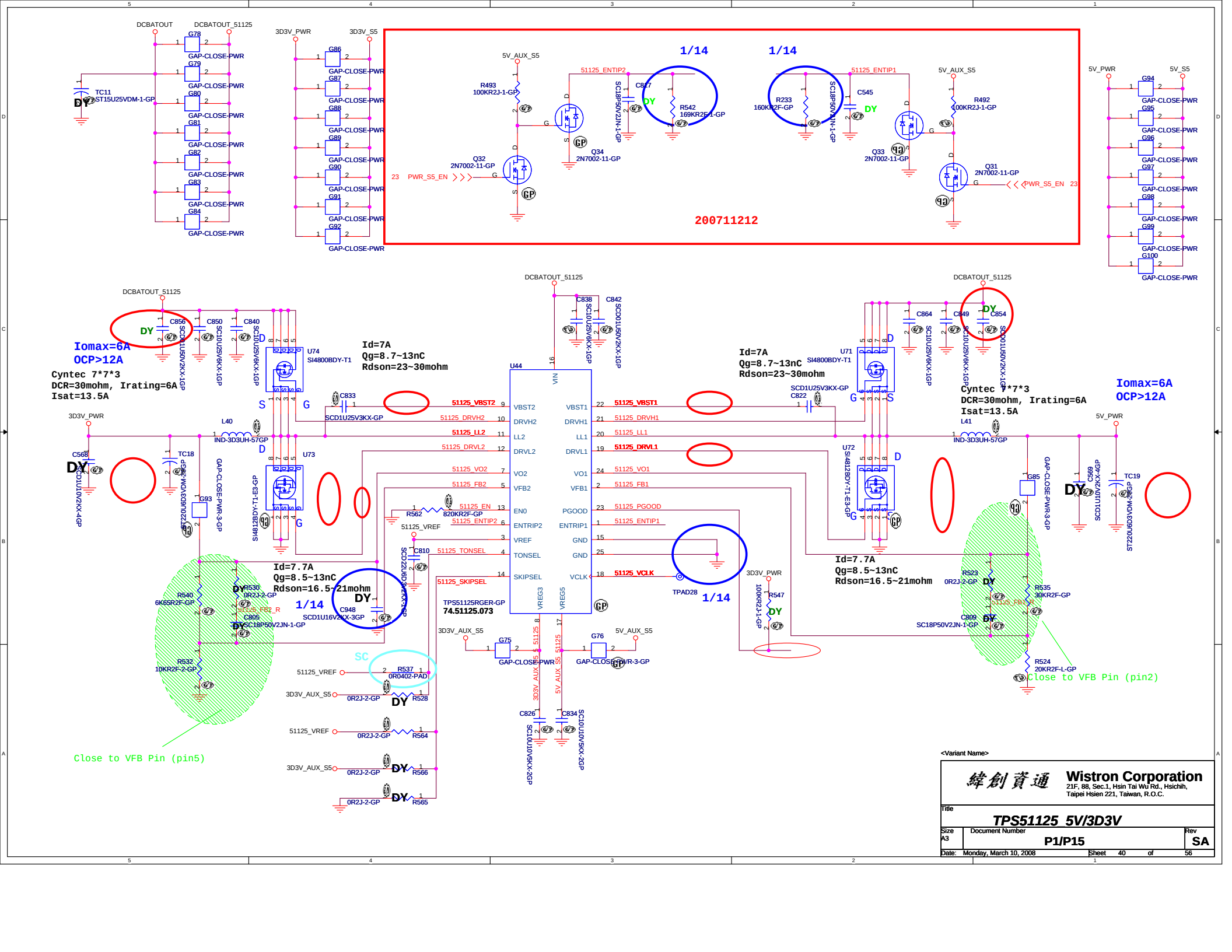
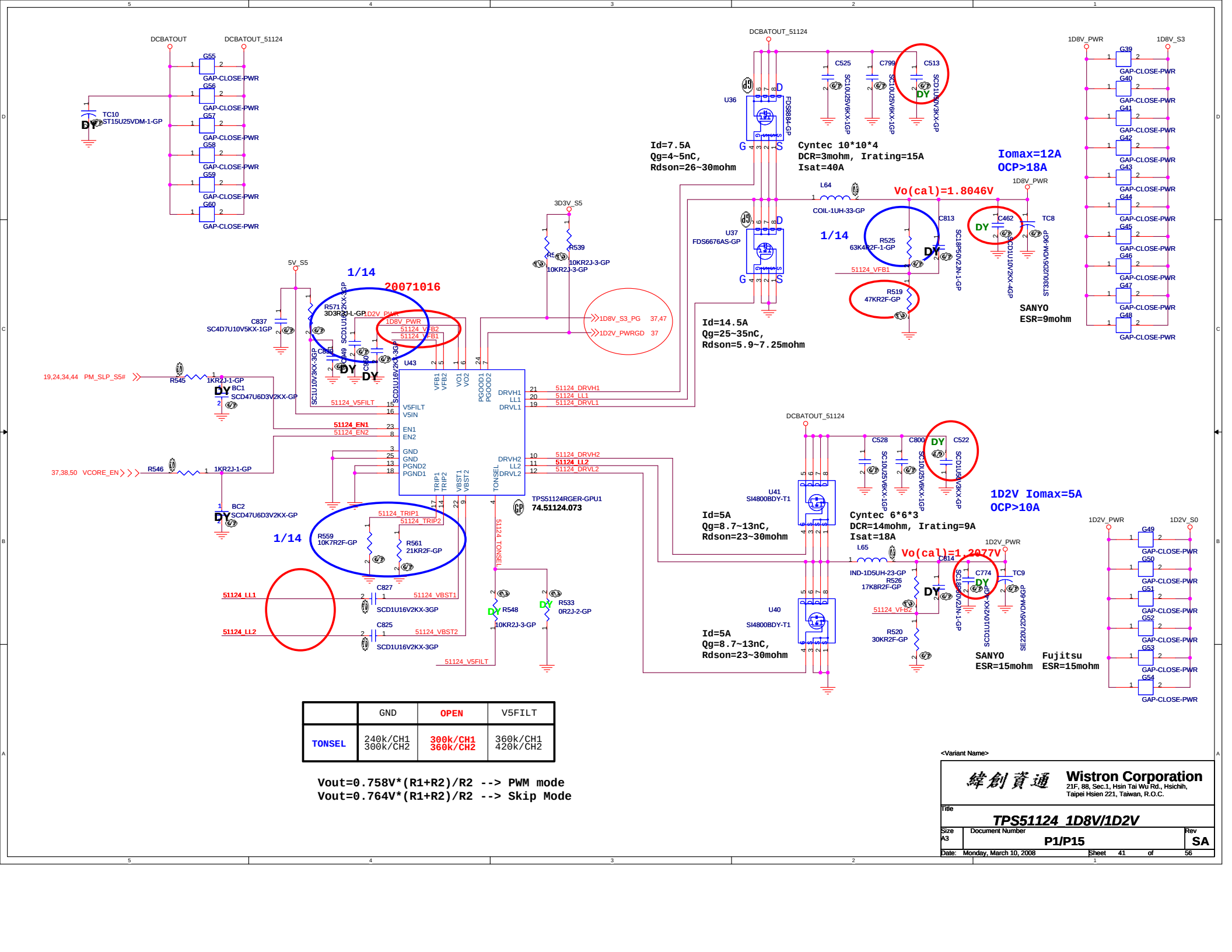
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037



緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title: ISL6265HR CPU Core/VDDNB 2/2			
Size: A3	Document Number: P1/P15		Rev: SA
Date: Monday, March 10, 2008		Sheet 39 of 56	


DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
5V_AUX_S5
5V_PWR
5V_S5
1/14
1/14
200711212
PWR_S5_EN
51125_ENTIP2
51125_ENTIP1
Iomax=6A
OCP>12A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
TPS51125RGER-GP
74.51125.073
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
TPS51125 5V/3D3V
P1/P15
Monday, March 10, 2008



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V/1D2V

Size	Document Number	Rev
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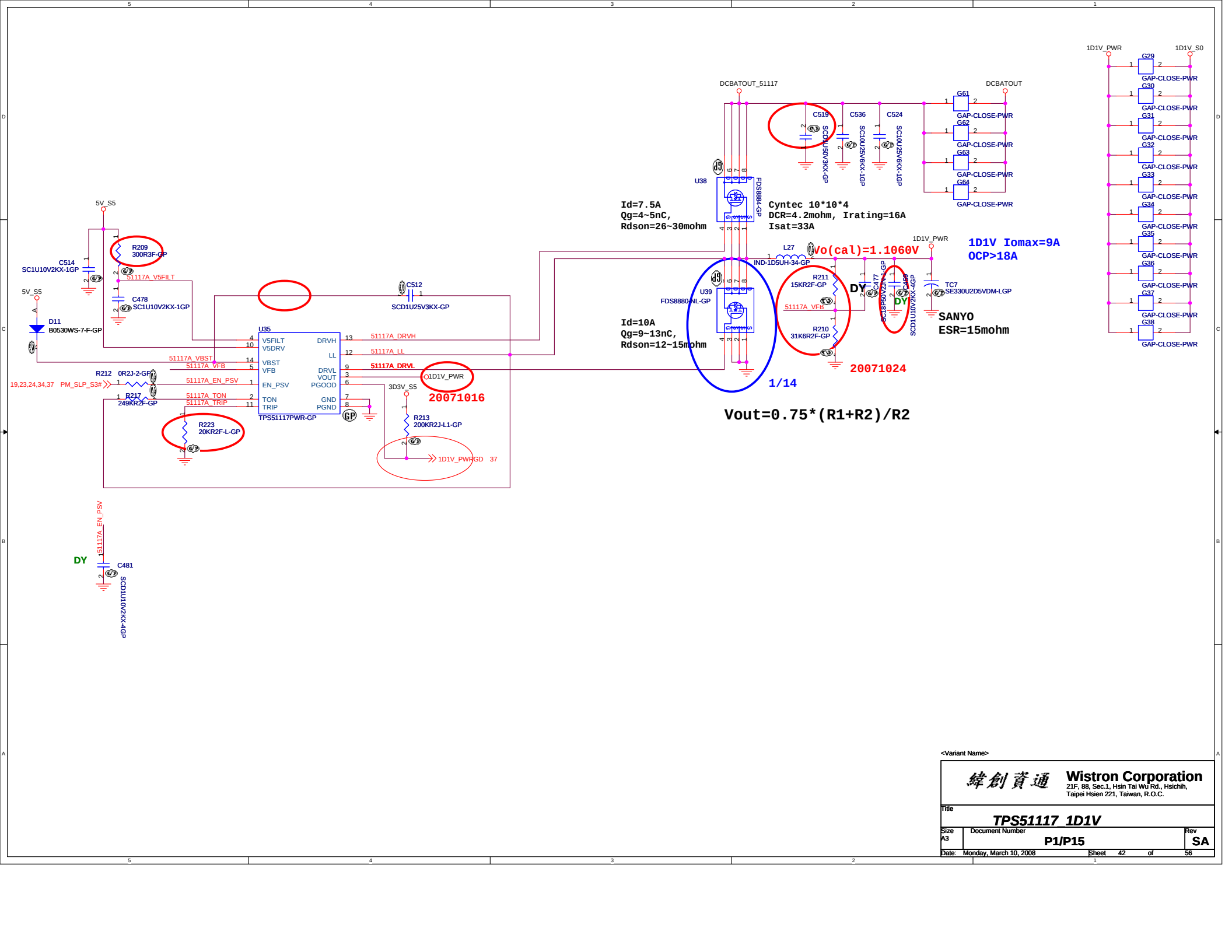
Date: Monday, March 10, 2008 Sheet 41 of 56



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117_1D1V***

Size	Document Number	Rev
A3	P1/P15	SA

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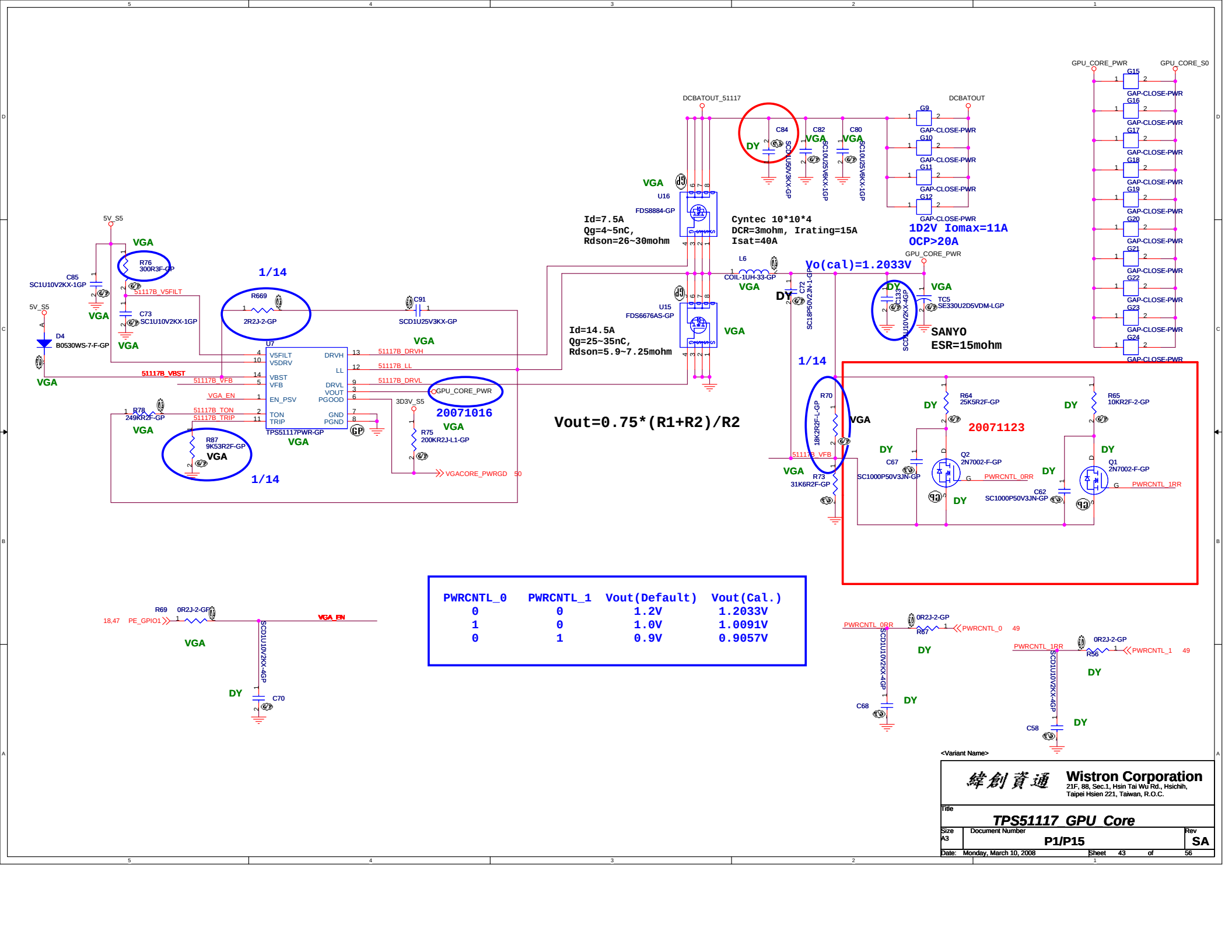


PWRCNTL_0	PWRCNTL_1	Vout(Default)	Vout(Cal.)
0	0	1.2V	1.2033V
1	0	1.0V	1.0091V
0	1	0.9V	0.9057V

<Variant Name>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

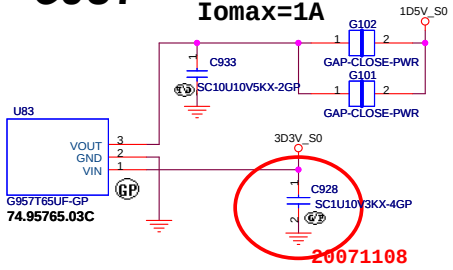
Title: TPS51117_GPU_Core

Size	Document Number	Rev
A3	P1/P15	SA

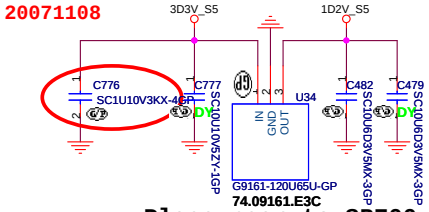
Date: Monday, March 10, 2008 Sheet 43 of 56

G957

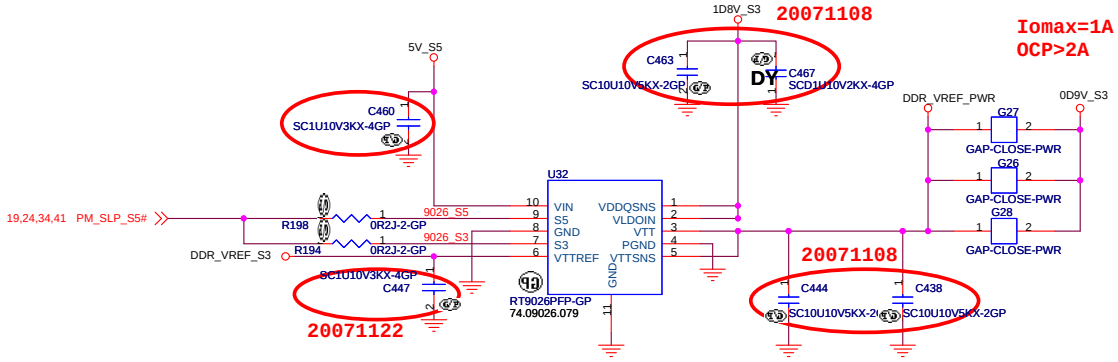
1D5V_S0
Iomax=1A



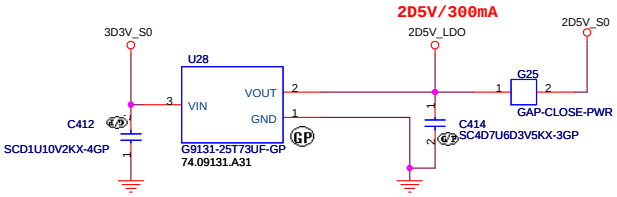
1D2V_S5
Iomax=400mA



Place near to SB700



2D5V_S0
Iomax=0.3A



<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***0D9V&2D5V&1D25V&1D5V***

Size	Document Number	Rev
A3	P1/P15	SA

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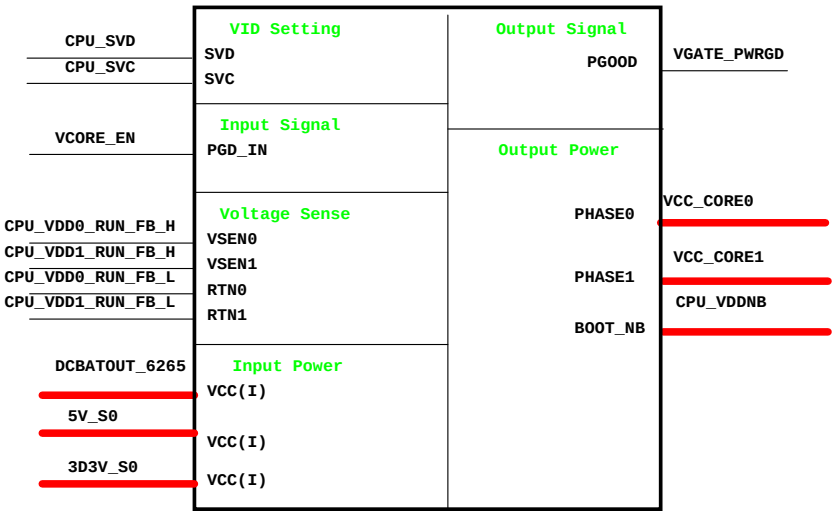
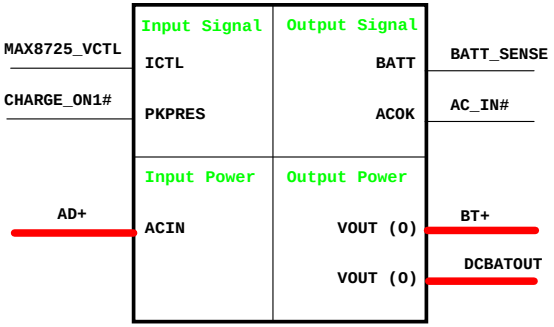
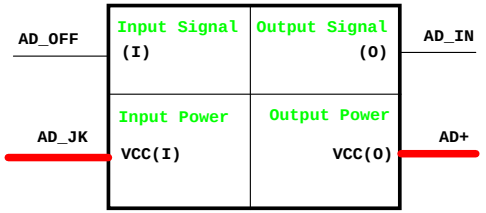
CPU_CORE
Intersil ISL6265



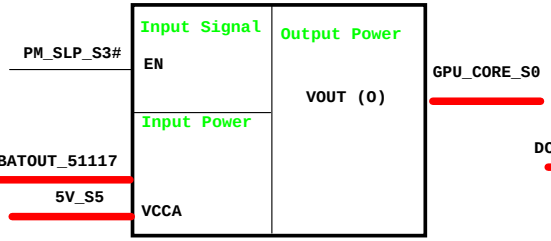
Charger Max8725



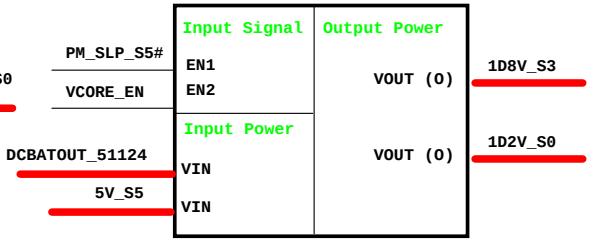
Adapter



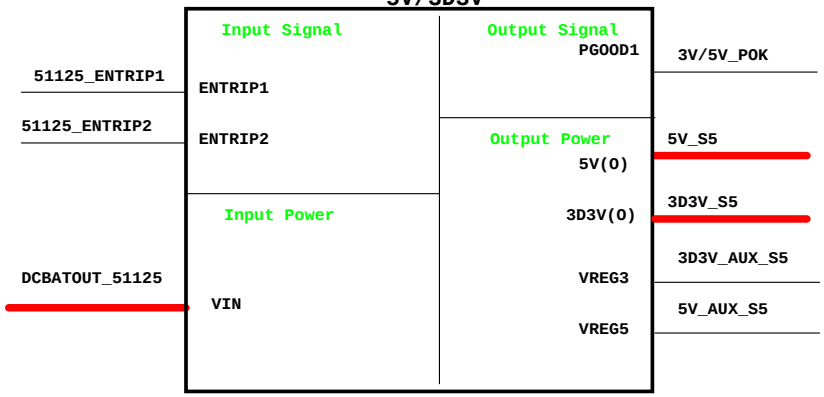
TPS51117
GPU_CORE



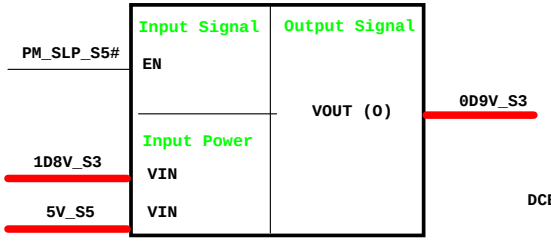
TPS51124
1D8V_S3
1D2V_S0



TPS51125
5V/3D3V



RT9026PFP
0D9V_S3



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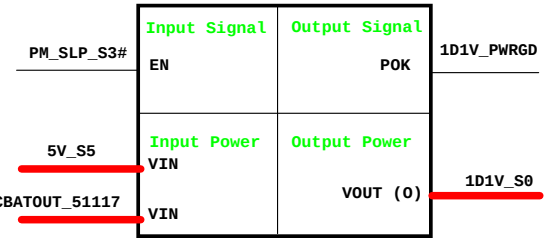

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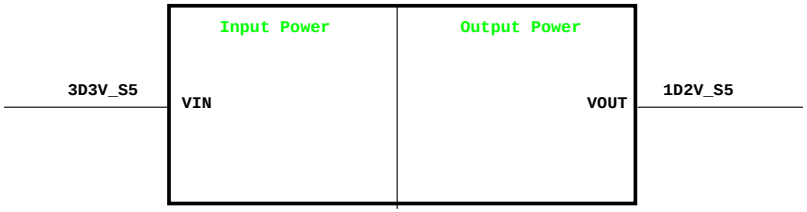

G957
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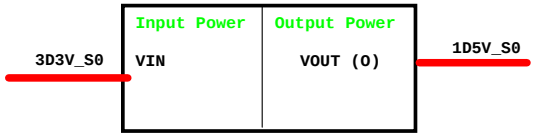


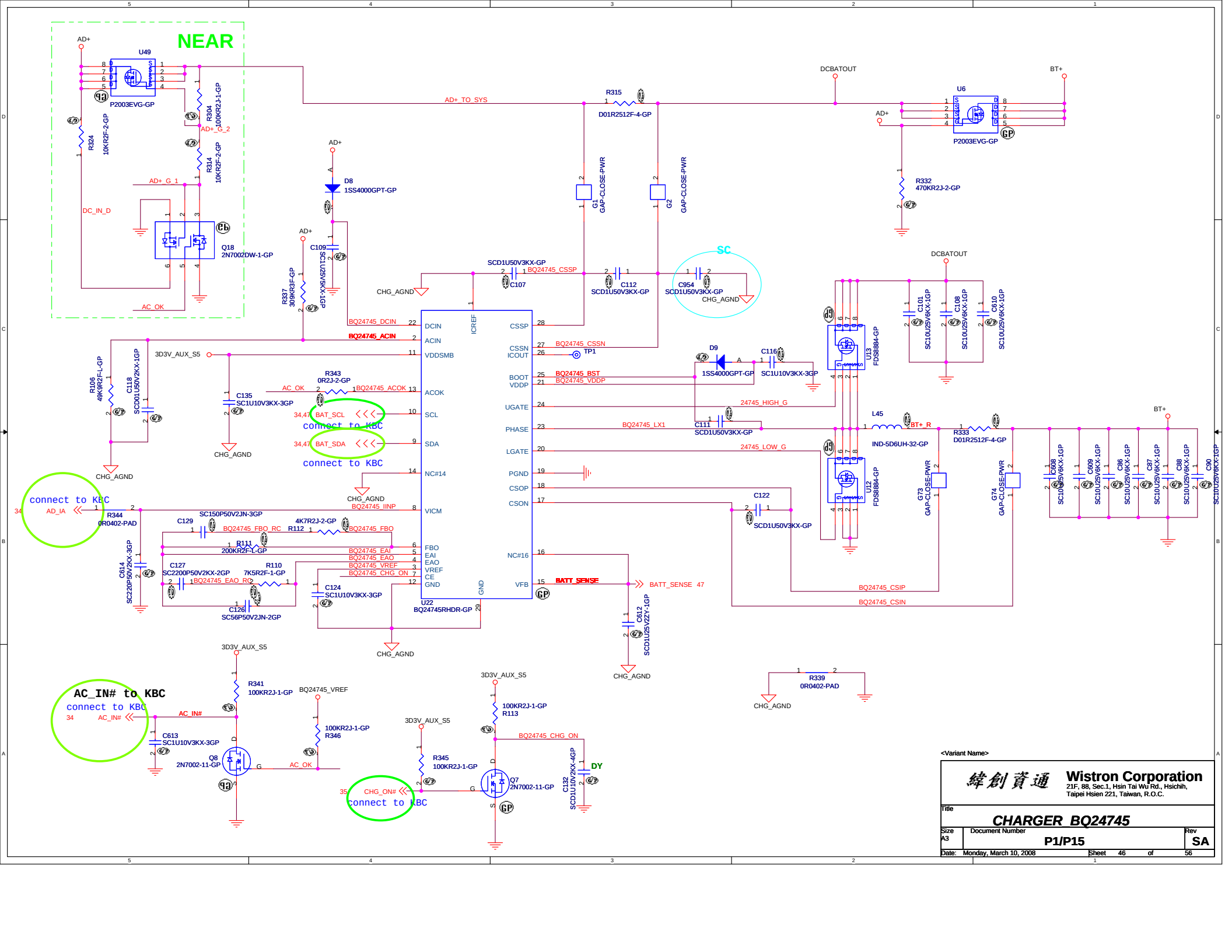
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Power Block Diagram***

Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 45 of 56



<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CHARGER_BQ24745

Size	Document Number	Rev
A3	P1/P15	SA

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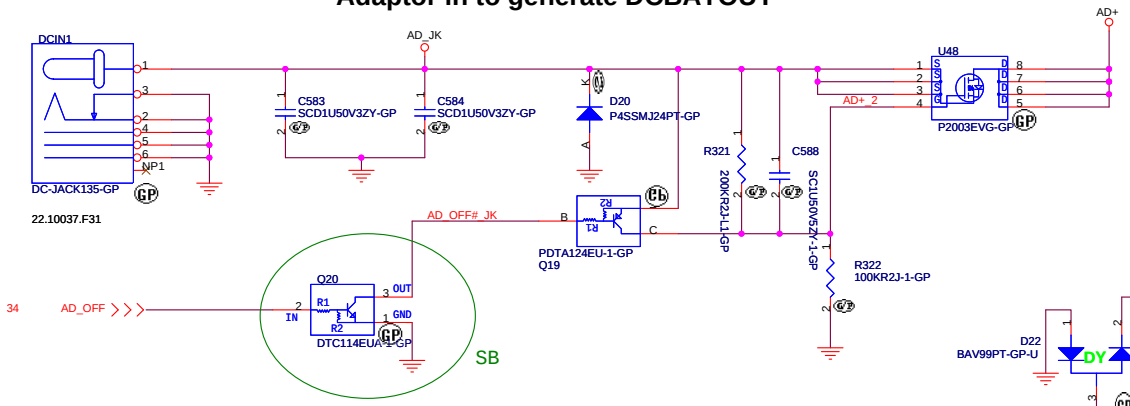
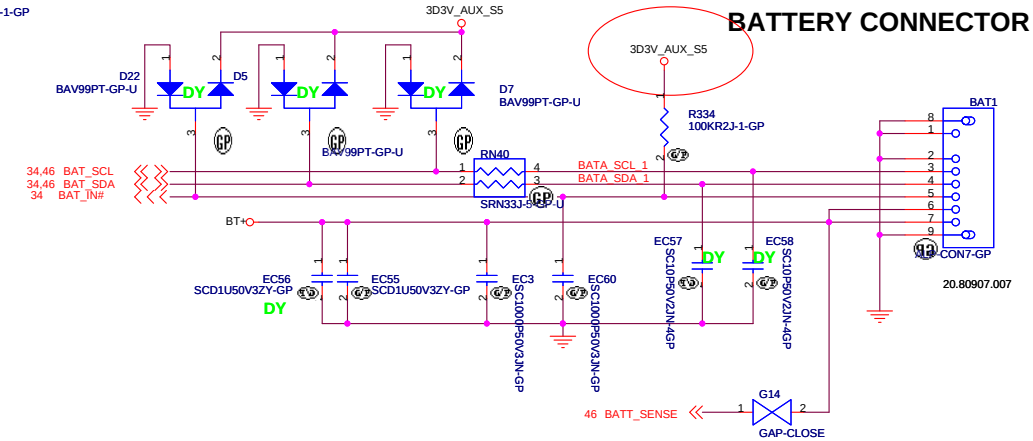
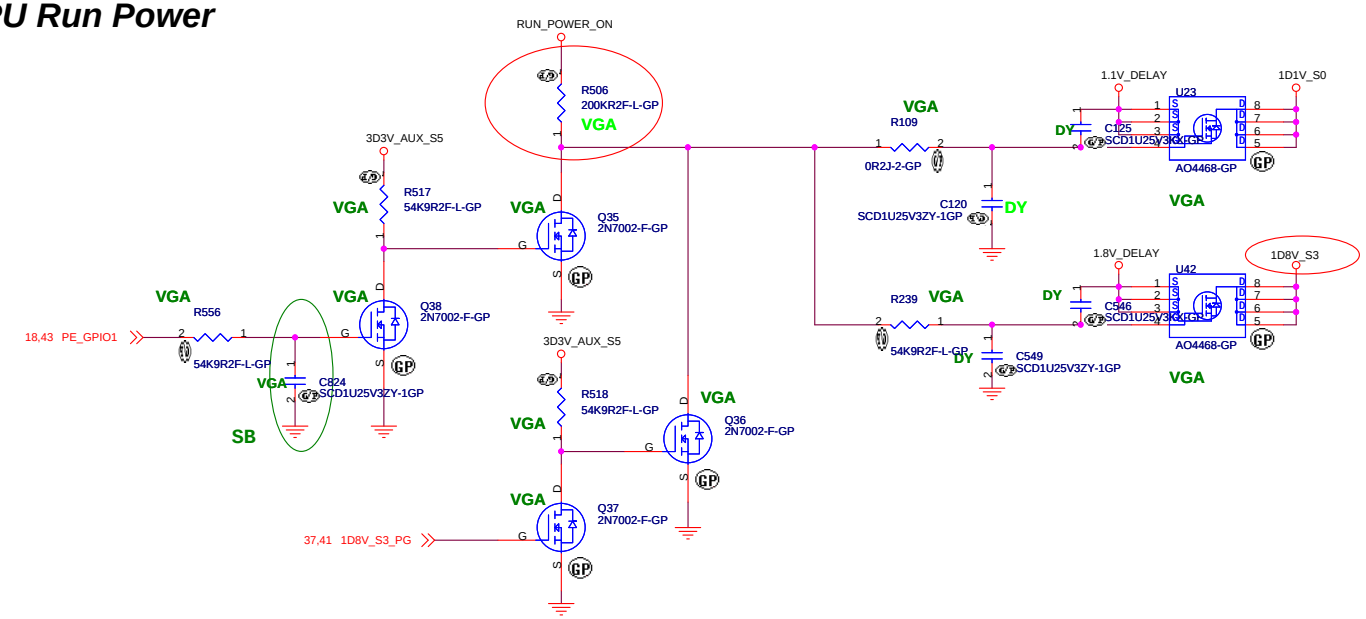
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



GPU Run Power



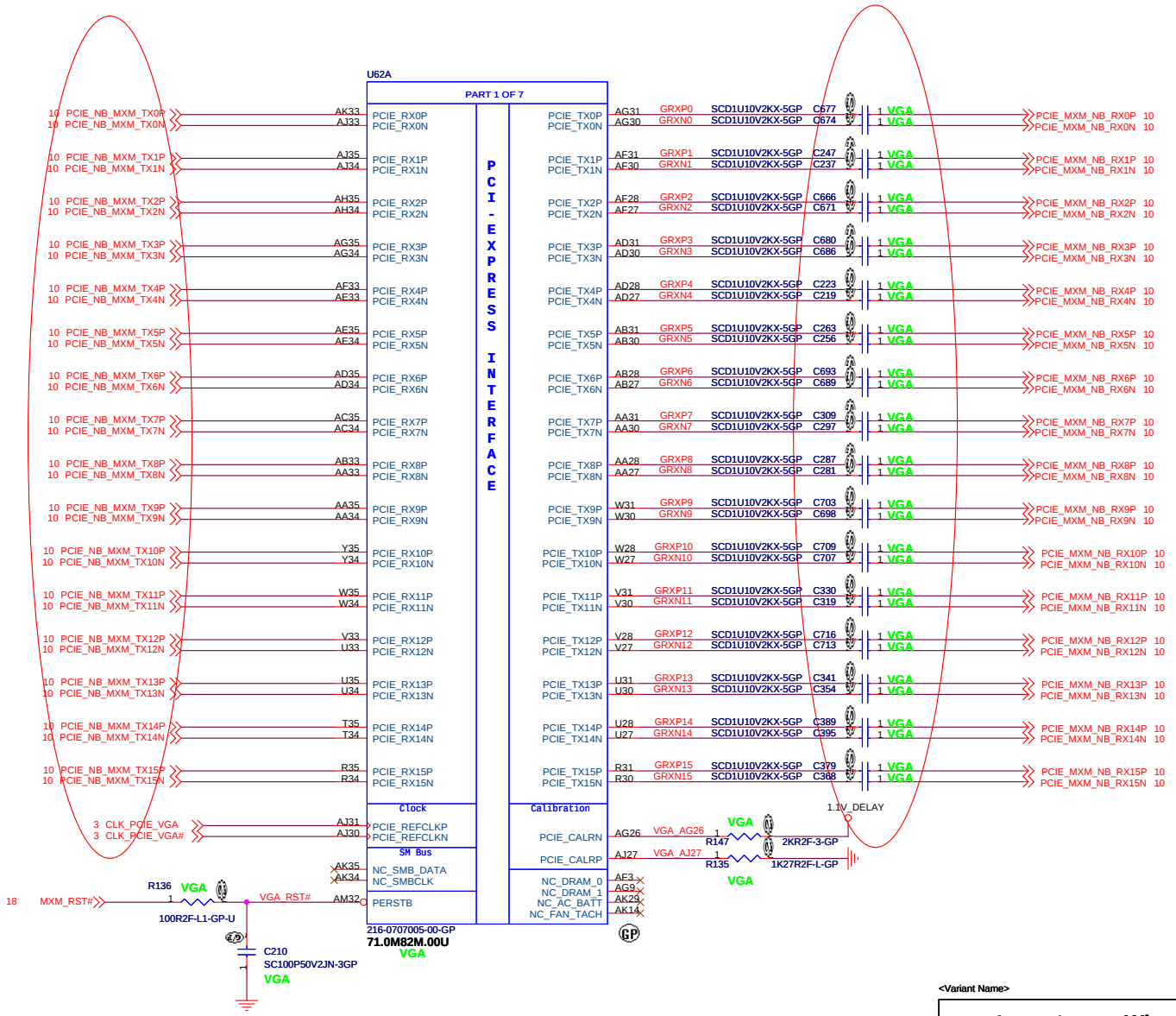
<Variant Name>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AD_IN/ BTY SWITCH/GPURUN***

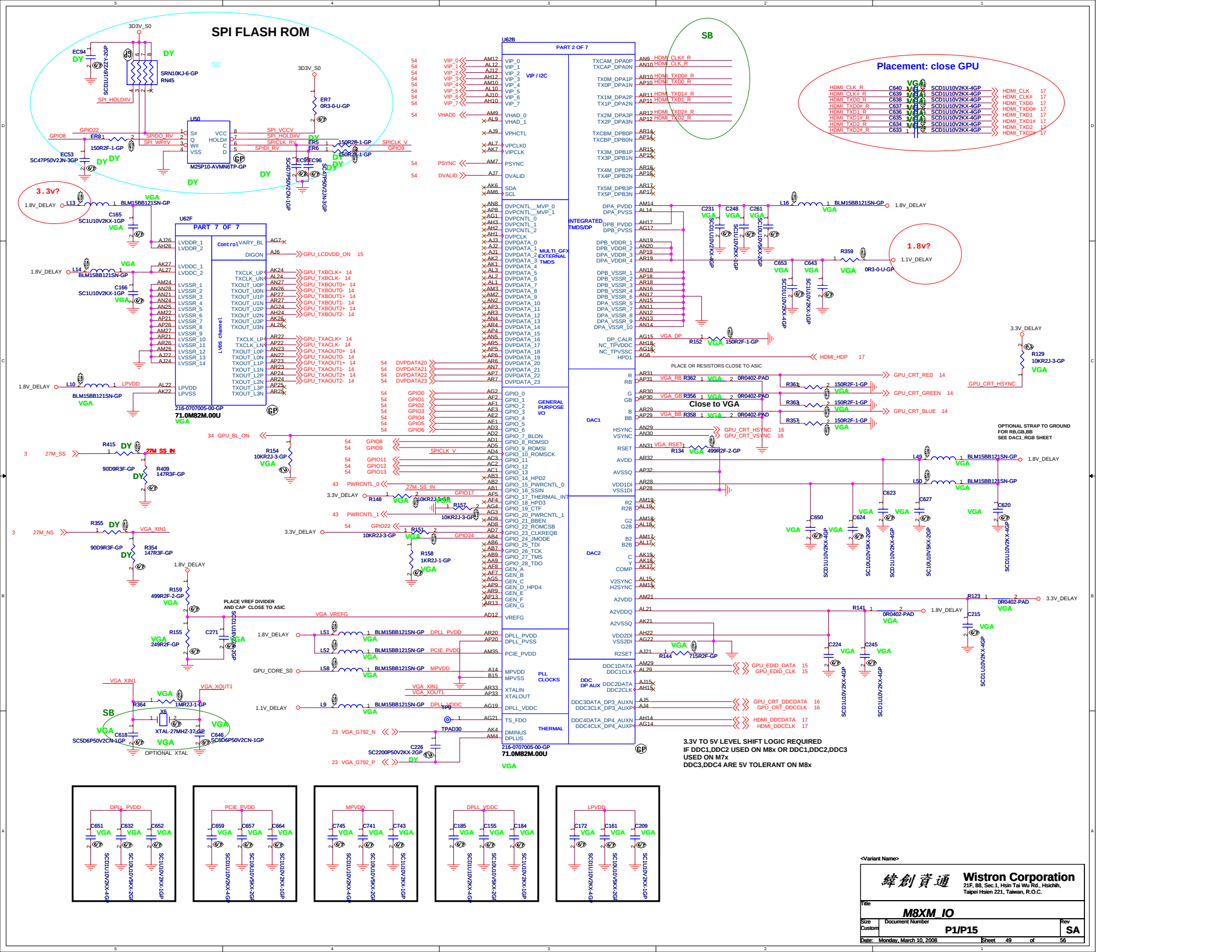
Size	Document Number	Rev
A3	P1/P15	SA

Date: Monday, March 10, 2008 Sheet 47 of 56



<Variant Name>

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M8XM_PCIE		
Size: A3	Document Number: P1/P15	Rev: SA
Date: Monday, March 10, 2008	Sheet 48 of 56	



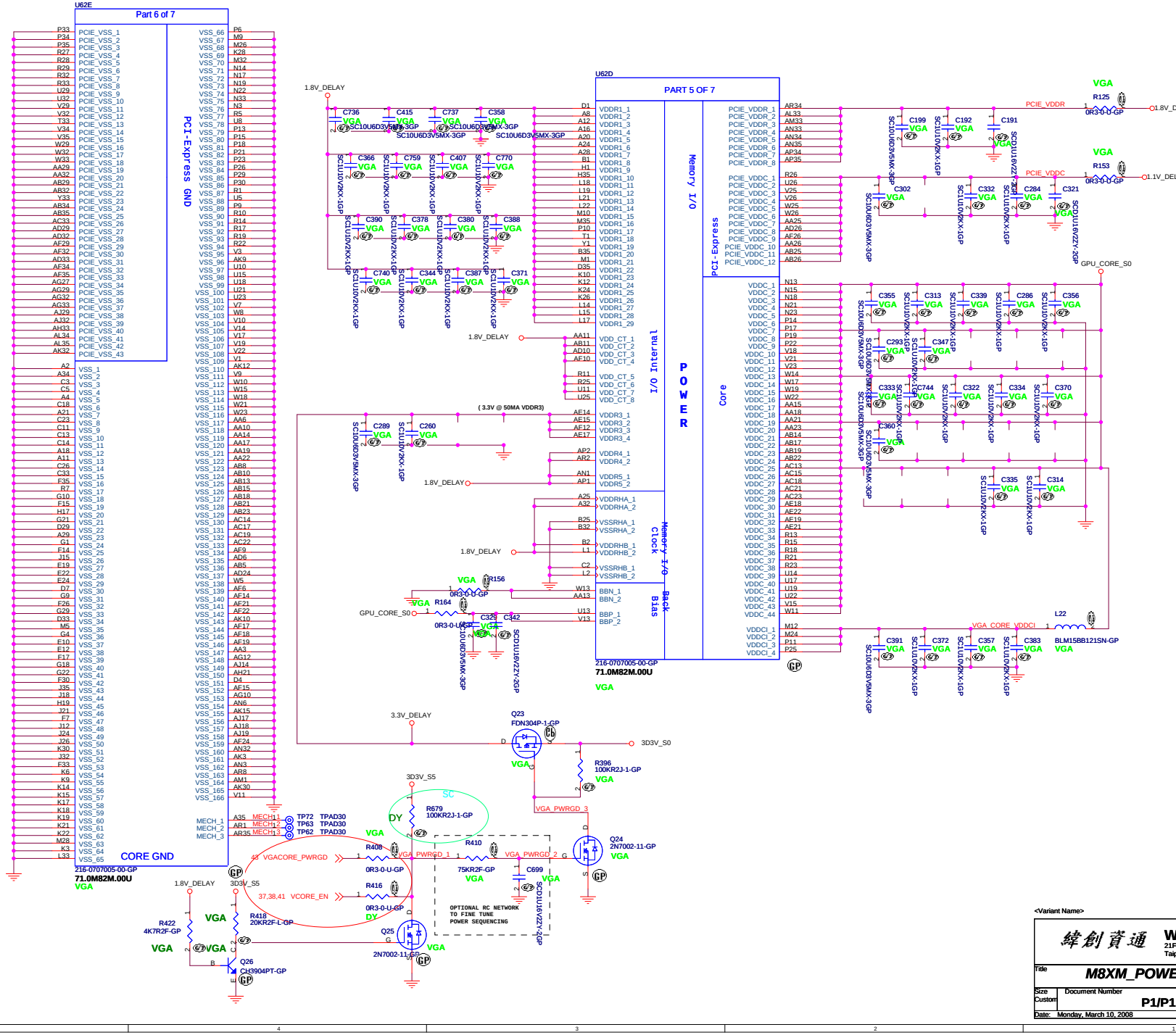
<Variant Name>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: M8XM_IO

Size: Custom | Document Number: P1/P15 | Rev: SA

Date: Monday, March 10, 2008 | Sheet 49 of 56


U62E
Part 6 of 7
PCIE_VSS_1
PCIE_VSS_2
PCIE_VSS_3
PCIE_VSS_4
PCIE_VSS_5
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PCIE_VSS_7
PCIE_VSS_8
PCIE_VSS_9
PCIE_VSS_10
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PCIE_VSS_43
PCI-Express GND
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VSS_166
CORE GND
216-0707005-00-GP
71.0M82M.00U
VGA
MECH_1
MECH_2
MECH_3
TP72 TPAD30
TP63 TPAD30
TP62 TPAD30
U62D
PART 5 OF 7
Memory I/O
I/O Internal
POWER
Core
PCI-Express
Memory I/O Clock
Bias
VDDR1_1
VDDR1_2
VDDR1_3
VDDR1_4
VDDR1_5
VDDR1_6
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VSSRHB_2
BBN_1
BBN_2
BBP_1
BBP_2
PCIE_VDDR_1
PCIE_VDDR_2
PCIE_VDDR_3
PCIE_VDDR_4
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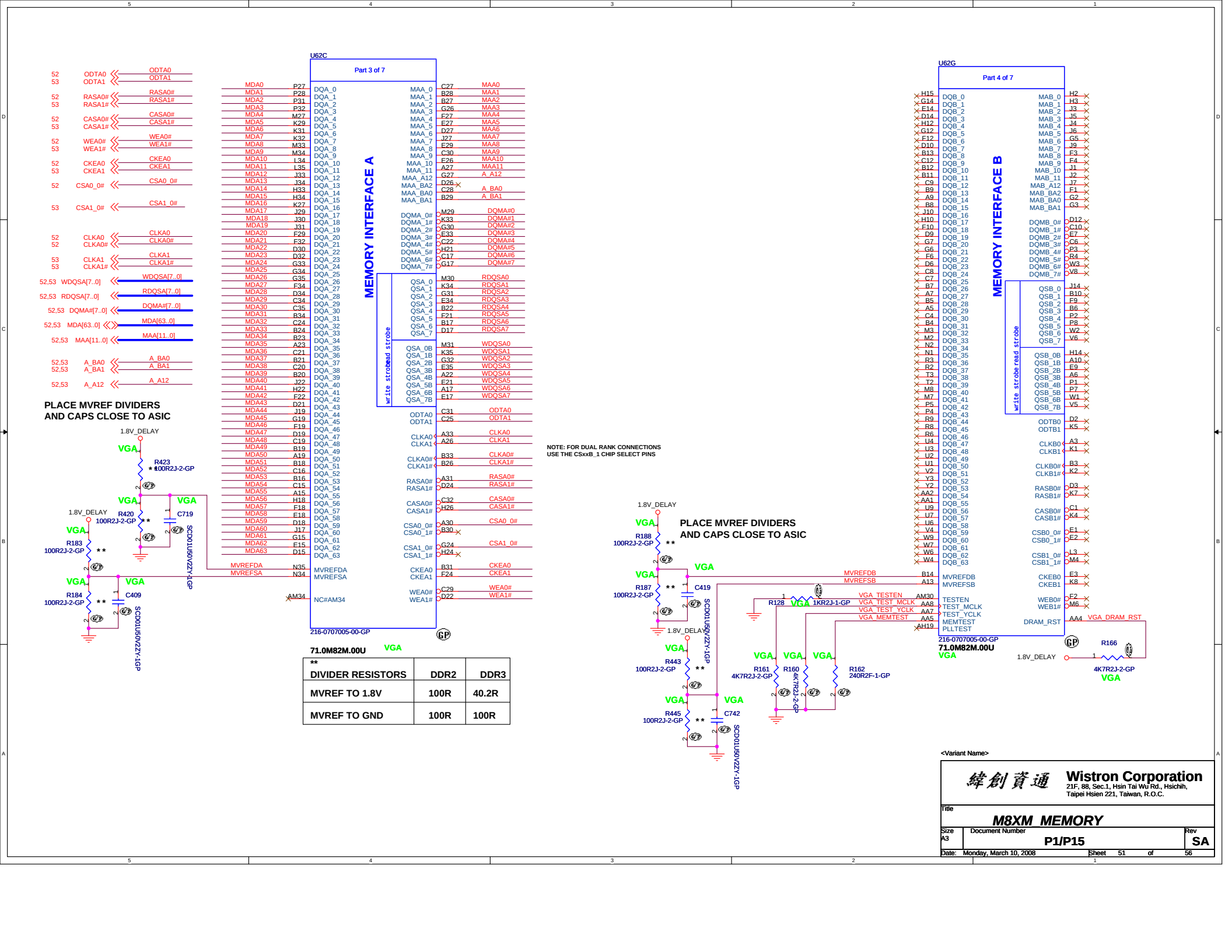
VGA
1.8V_DELAY
3.3V_DELAY
3D3V_S0
3D3V_S5
1.1V_DELAY
GPU_CORE_S0
VGA_CORE_VDDCI
PCIE_VDDR
PCIE_VDDC
(3.3V @ 50MA VDDR3)
Q23
FDN304P-1-GP
Q24
2N7002-11-GP
Q25
2N7002-11-GP
Q26
CH3904PT-GP
R679
100KR2J-1-GP
R396
100KR2J-1-GP
R408
0R3-0-U-GP
R410
75KR2F-GP
R416
0R3-0-U-GP
R418
20KR2F-1-GP
R422
4K7R2F-GP
R156
0R3-0-U-GP
R164
0R3-0-U-GP
R125
0R3-0-U-GP
R153
0R3-0-U-GP
L22
BLM15BB121SN-GP
42 VGACORE_PWRGD
37,38,41 VCORE_EN
VGA_PWRGD_1
VGA_PWRGD_2
VGA_PWRGD_3
OPTIONAL RC NETWORK
TO FINE TUNE
POWER SEQUENCING
SC
DY
GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M8XM_POWER
Size
Custom
Document Number
P1/P15
Rev
SA
Date: Monday, March 10, 2008
Sheet 50 of 56


U62C
Part 3 of 7
MEMORY INTERFACE A
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ODTA1
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CLKA0#
CLKA1
CLKA1#
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RASA1#
CASA0#
CASA1#
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WEA1#
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MVREFSA
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CKEA1
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read strobe
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GP
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DQMA#7
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RDQSA2
RDQSA3
RDQSA4
RDQSA5
RDQSA6
RDQSA7
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CLKA0#
CLKA1#
RASA0#
RASA1#
CASA0#
CASA1#
CSA0_0#
CSA1_0#
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WEA1#
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MVREFSA
CKEA0
CKEA1
WEA0#
WEA1#
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53 ODTA1
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53 CSA1_0#
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53 CLKA1
53 CLKA1#
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52,53 RDQSA[7..0]
52,53 DQMA#[7..0]
52,53 MDA[63..0]
52,53 MAA[11..0]
52,53 A_BA0
52,53 A_BA1
52,53 A_A12
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
1.8V_DELAY
VGA
R423
100R2J-2-GP
R420
R183
R184
C719
C409
SCD01U50V2ZY-1GP
MVREFDA
MVREFSA
**
DIVIDER RESISTORS
DDR2
DDR3
MVREF TO 1.8V
100R
40.2R
MVREF TO GND
100R
100R
NOTE: FOR DUAL RANK CONNECTIONS
USE THE CSxxB_1 CHIP SELECT PINS
U62G
Part 4 of 7
MEMORY INTERFACE B
DQB_0
DQB_1
DQB_2
DQB_3
DQB_4
DQB_5
DQB_6
DQB_7
DQB_8
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MAB_BA2
MAB_BA0
MAB_BA1
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DQMB_1#
DQMB_2#
DQMB_3#
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DQMB_5#
DQMB_6#
DQMB_7#
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QSB_2
QSB_3
QSB_4
QSB_5
QSB_6
QSB_7
QSB_0B
QSB_1B
QSB_2B
QSB_3B
QSB_4B
QSB_5B
QSB_6B
QSB_7B
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ODTB1
CLKB0
CLKB1
CLKB0#
CLKB1#
RASB0#
RASB1#
CASB0#
CASB1#
CSB0_0#
CSB0_1#
CSB1_0#
CSB1_1#
CKEB0
CKEB1
WEB0#
WEB1#
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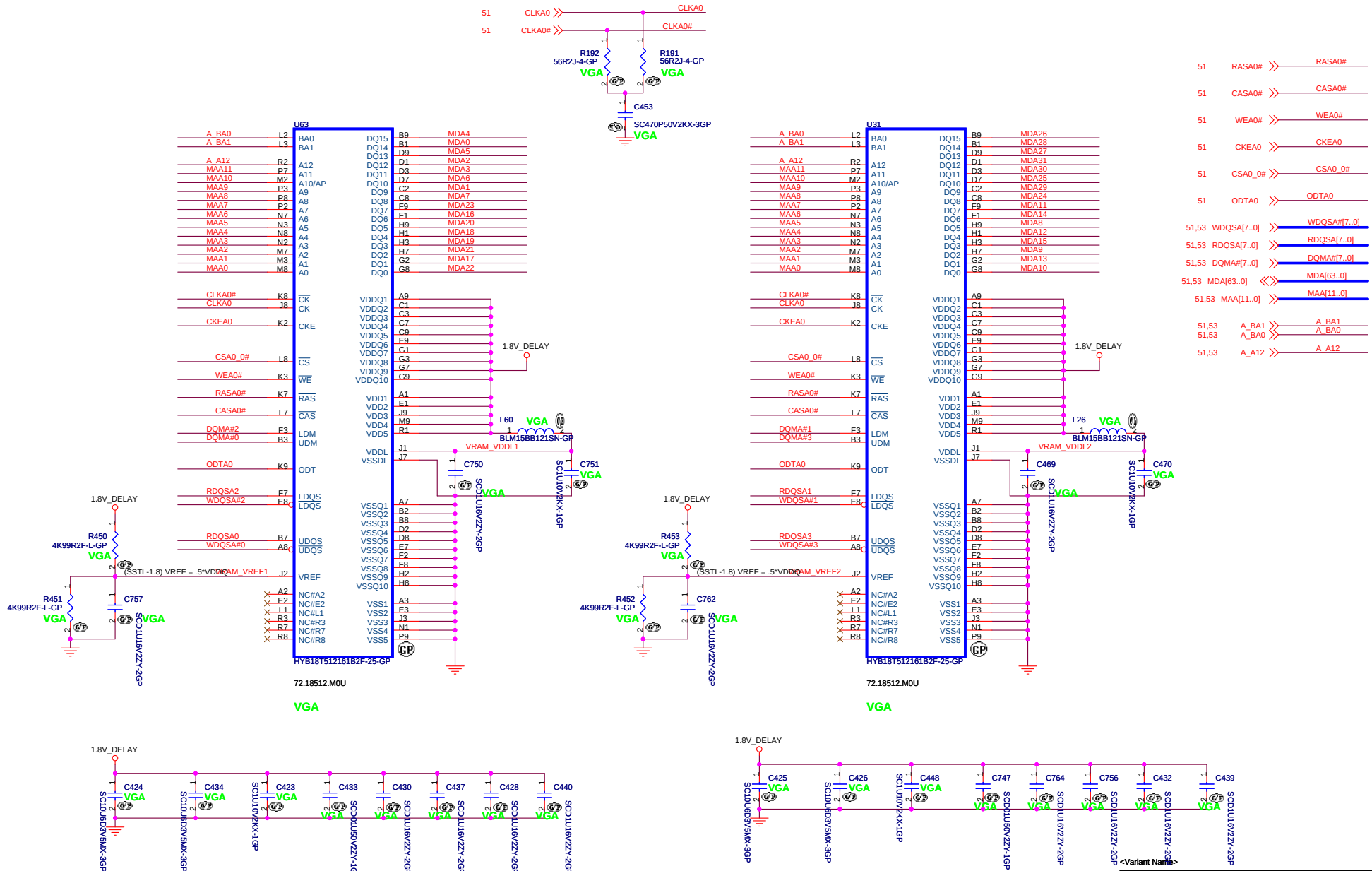
MVREFSB
TESTEN
TEST_MCLK
TEST_YCLK
MEMTEST
PLLTEST
DRAM_RST
VGA_DRAM_RST
VGA_TESTEN
VGA_TEST_MCLK
VGA_TEST_YCLK
VGA_MEMTEST
R128
1KR2J-1-GP
R161
4K7R2J-2-GP
R160
R162
240R2F-1-GP
R166
4K7R2J-2-GP
R188
R187
R443
R445
C419
C742
SCD01U50V2ZY-1GP
PLACE MVREF DIVIDERS
AND CAPS CLOSE TO ASIC
1.8V_DELAY
VGA
GP
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
M8XM_MEMORY
Size
A3
Document Number
P1/P15
Rev
SA
Date: Monday, March 10, 2008
Sheet 51 of 56



Wistron Corporation	緯創資通
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: VRAM DDR2 32MX16 A	
Size: A3	Document Number: P1/P15
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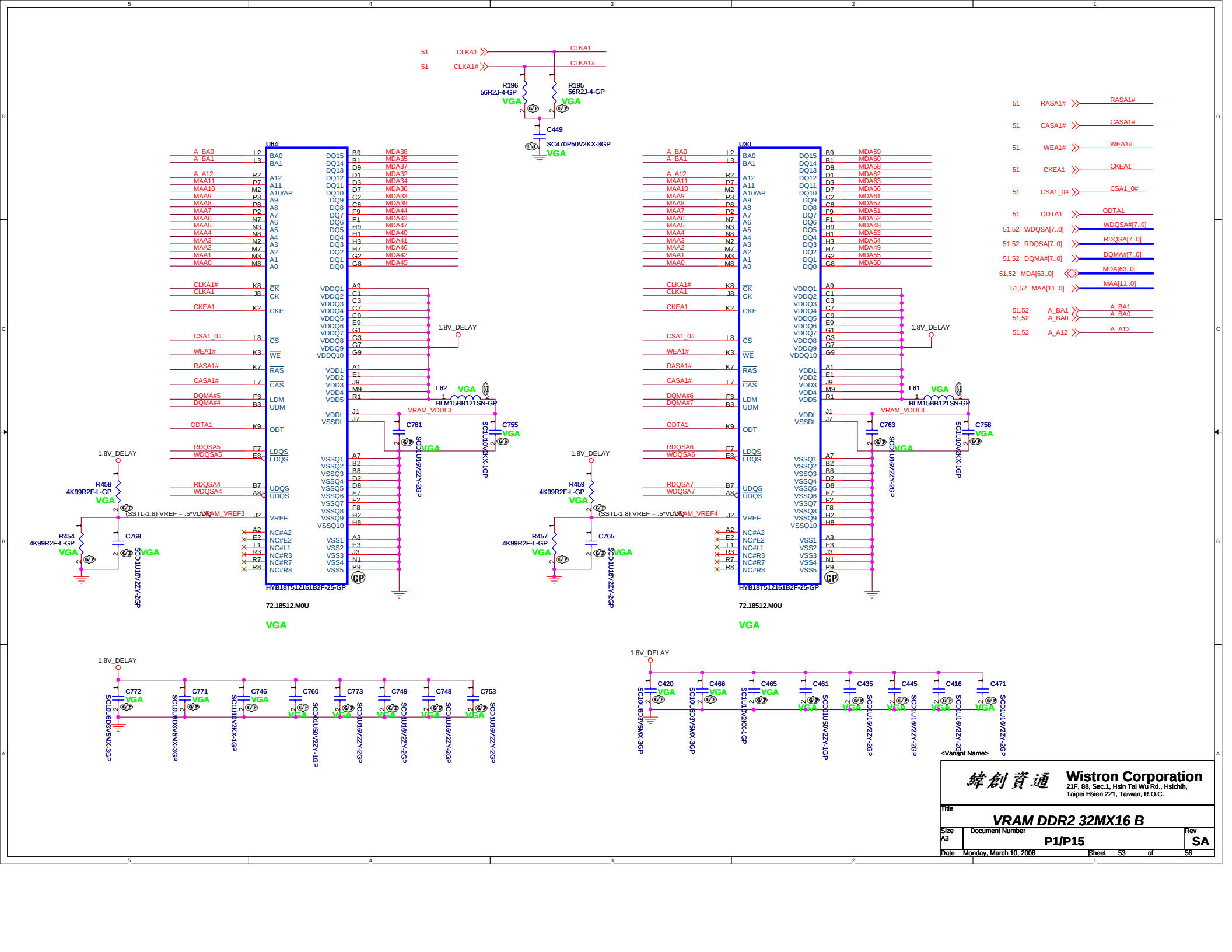
CLKA1
CLKA1#
R196 56R2J-4-GP
R195 56R2J-4-GP
C449 SC470P50V2KX-3GP
U64
U30
HYB18T512161B2F-25-GP
72.18512.M0U
1.8V_DELAY
L62 BLM15BB121SN-GP
L61 BLM15BB121SN-GP
VRAM_VDDL3
VRAM_VDDL4
VRAM_VREF3
VRAM_VREF4
(SSTL-1.8) VREF = .5*VDDQ
R458 4K99R2F-L-GP
R459 4K99R2F-L-GP
R454 4K99R2F-L-GP
R457 4K99R2F-L-GP
C761 SCD1U16V2ZY-2GP
C763 SCD1U16V2ZY-2GP
C755 SC1U10V2KX-1GP
C758 SC1U10V2KX-1GP
C768 SCD1U16V2ZY-2GP
C765 SCD1U16V2ZY-2GP
C772 SC10U6D3V5MX-3GP
C771 SC10U6D3V5MX-3GP
C746 SC1U10V2KX-1GP
C760 SCD1U50V2ZY-1GP
C773 SCD1U16V2ZY-2GP
C749 SCD1U16V2ZY-2GP
C748 SCD1U16V2ZY-2GP
C753 SCD1U16V2ZY-2GP
C420 SC10U6D3V5MX-3GP
C466 SC10U6D3V5MX-3GP
C465 SC1U10V2KX-1GP
C461 SCD1U50V2ZY-1GP
C435 SCD1U16V2ZY-2GP
C445 SCD1U16V2ZY-2GP
C416 SCD1U16V2ZY-2GP
C471 SCD1U16V2ZY-2GP
VGA
RASA1#
CASA1#
WEA1#
CKEA1
CSA1_0#
ODTA1
WDQSA#[7..0]
RDQSA[7..0]
DQMA#[7..0]
MDA[63..0]
MAA[11..0]
A_BA1
A_BA0
A_A12
<Variant Name>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
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VRAM DDR2 32MX16 B
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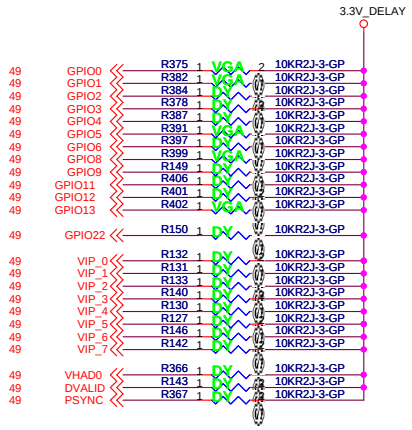
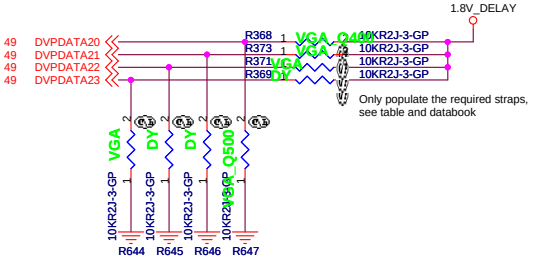
Note:1 VIP3 MUST NOT BE PULLED HIGH ON M82-M

Note:2 GPIO8 MUST NOT BE PULLED HIGH ON M86-M or M7X





CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 10K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE
RSVD = ATI RESERVED
(DO NOT INSTALL)

STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	M8x	M7x
BIF_MSI_DIS	VIP1	MESSAGE SIGNAL INTERRUPT ENABLED	NA	0
BIF_AUDIO_EN	VIP3	ENABLE HD AUDIO **(M7XM and M86M ONLY)** *Note:1*	X	X
BIF_64BAR_EN_A	VIP5	64 BIT BARS DISABLED	NA	0
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	X	X
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X	X
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO **(M82M ONLY)** *Note:2*	X	RSVD
BIF_GEN2_EN_A	GPIO5	Allows either PCIe 2.5GT/s or 5.0GT/s operation	X	0
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	NA	X
ROMIDCFG(3:0)	GPIO[13:11,9]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	XX X X	X X X X
VIP_DEVICE_STRAP_ENA	VSYNC	IGNORE VIP DEVICE STRAPS	O	O
BIF_VGA DIS	PSYNC	VGA ENABLED	0	O
BIF_HDMI_EN	HSYNC	HDMI ENABLE (SEE NOTE 2)	X	X
DEBUG_ I2C_ENABLE	GPIO6	Internal use only	0	0
MEM_TYPE	ANY UNUSED GPIO OR DVP THAT ARE NOT CONFIG STRAPS FOR EXAMPLE DVPDATA20:23 IN THIS DESIGN	MEMORY TYPE,MAKE AND SIZE INFO	X X X X	X X X X

NOTE 1: HD AUDIO MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

NOTE 2: HDMI MUST ONLY BE ENABLED ON SYSTEMS THAT ARE LEGALLY ENTITLED. IT IS THE RESPONSIBILITY OF THE SYSTEM DESIGNER TO ENSURE ENTITLEMENT

ATI RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

VHAD0 VIP0 VIP2 VIP4 VIP6 VIP7 GPIO2 GPIO3 H2SYNC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO GENERICC GPIO21_BB_EN

DVPDATA20 1
DVPDATA21 1
DVPDATA22 1
DVPDATA23 1

HY5PS121621CFP-25 Hynix
72.51216.F0U

DVPDATA20 1
DVPDATA21 1
DVPDATA22 1
DVPDATA23 0

HYB18T512161B2F-25 Qimonda 400MHz
72.18512.M0U

DVPDATA20 1
DVPDATA21 1
DVPDATA22 0
DVPDATA23 1

K4N51163QE-ZC25 Samsung
72.45116.A0U

DVPDATA20 0
DVPDATA21 1
DVPDATA22 1
DVPDATA23 0

HYB18T512161B2F-20 Qimonda 500MHz
72.18512.N0U

<Variant Name>

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Title: **STRAPS**

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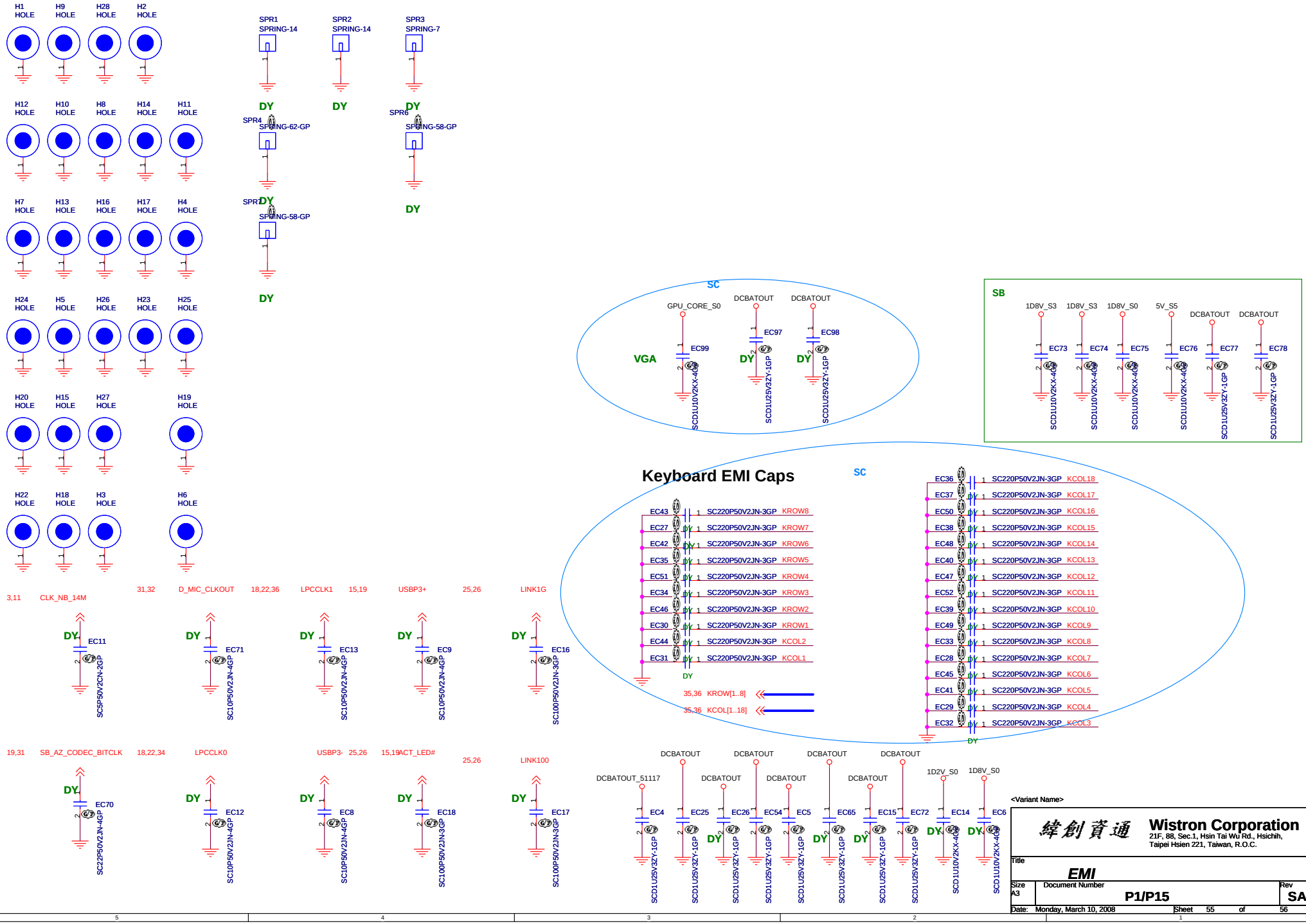
H1 HOLE
H9 HOLE
H28 HOLE
H2 HOLE
H12 HOLE
H10 HOLE
H8 HOLE
H14 HOLE
H11 HOLE
H7 HOLE
H13 HOLE
H16 HOLE
H17 HOLE
H4 HOLE
H24 HOLE
H5 HOLE
H26 HOLE
H23 HOLE
H25 HOLE
H20 HOLE
H15 HOLE
H27 HOLE
H19 HOLE
H22 HOLE
H18 HOLE
H3 HOLE
H6 HOLE
SPR1 SPRING-14
SPR2 SPRING-14
SPR3 SPRING-7
SPR4 SPRING-62-GP
SPR6 SPRING-58-GP
SPR7 SPRING-58-GP
DY
SC
VGA
GPU_CORE_S0
DCBATOUT
EC97
EC98
EC99
SCD1U10V2KX-4GP
SCD1U25V3ZY-1GP
SB
1D8V_S3
1D8V_S0
5V_S5
EC73
EC74
EC75
EC76
EC77
EC78
Keyboard EMI Caps
EC43 KROW8
EC27 KROW7
EC42 KROW6
EC35 KROW5
EC51 KROW4
EC34 KROW3
EC46 KROW2
EC30 KROW1
EC44 KCOL2
EC31 KCOL1
35,36 KROW[1..8]
35,36 KCOL[1..18]
EC36 KCOL18
EC37 KCOL17
EC50 KCOL16
EC38 KCOL15
EC48 KCOL14
EC40 KCOL13
EC47 KCOL12
EC52 KCOL11
EC39 KCOL10
EC49 KCOL9
EC33 KCOL8
EC28 KCOL7
EC45 KCOL6
EC41 KCOL5
EC29 KCOL4
EC32 KCOL3
SC220P50V2JN-3GP
3,11 CLK_NB_14M
EC11
SC5P50V2CN-2GP
31,32 D_MIC_CLKOUT
EC71
SC10P50V2JN-4GP
18,22,36 LPCCLK1
EC13
15,19 USBP3+
EC9
25,26 LINK1G
EC16
SC100P50V2JN-3GP
19,31 SB_AZ_CODEC_BITCLK
EC70
SC22P50V2JN-4GP
18,22,34 LPCCLK0
EC12
USBP3-
EC8
15,19 ACT_LED#
EC18
25,26 LINK100
EC17
DCBATOUT_51117
EC4
EC25
EC26
EC54
EC5
EC65
EC15
EC72
1D2V_S0
EC14
EC6
SCD1U10V2KX-4GP
<Variant Name>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
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NOTICE

1.VRAM and SIDE PORT GEOMETRY
2.digital array vendor

Change List

GEOMETRY

1.U60 62.10055.111 SKT-CPU638P-GP-U SKT-CPU638P-GP-U1 SKT-BGA638H176 SKT-BGA638H176

Common Part

1.RS780M_A13 U61 71.RS780.M12
2.SB700_A12 U67 71.SB700.M06
3.KBC U26 71.00773.00G
4.CLKGEN U33 71.09480.A03
5.SPDIF LOUT1 22.10270.031
6.MOSFET U53,U56 84.07686.037
7.MOSFET U11,U54,U55,U57 84.04634.037
8.H19,H20 34.4W601.001
9.U21 72.18512.M0U(QIMONDA)
10.card1 20.I0043.001
11.C861,C862,C941,C943 78.10324.2FL
12.C843,C844,C942,C944 63.R0034.1DL
13.USB2 22.10218.Z71
14.U70 71.00888.E0G
15.U32 74.51100.079

Common 2nd source

1.U21 72.45116.A0U

For P15

1.M82ME_A11 U62 71.M82ME.M01
2.8111C U1 71.08111.E03
3.JMB380 U46 71.00380.003
4.R12 64.24915.6DL
5.VRAM U30,U31,U63,U64 72.18512.M0U(QIMONDA400)

P15 2nd source

1.VRAM U30,U31,U63,U64 72.18512.N0U(QIMONDA500)

For P1

1.8101E U1 71.08101.B0G
2.JMB385 U46 71.JM385.A0G
3. R247,R253,R254,R255,R256,R620,C574 63.R0034.1DL
4. C573 63.00000.00L
5.R12 64.20015.6DL
6. R307,R163 64.14005.6DL

<Variant Name>

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Title: CHANGE LIST

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