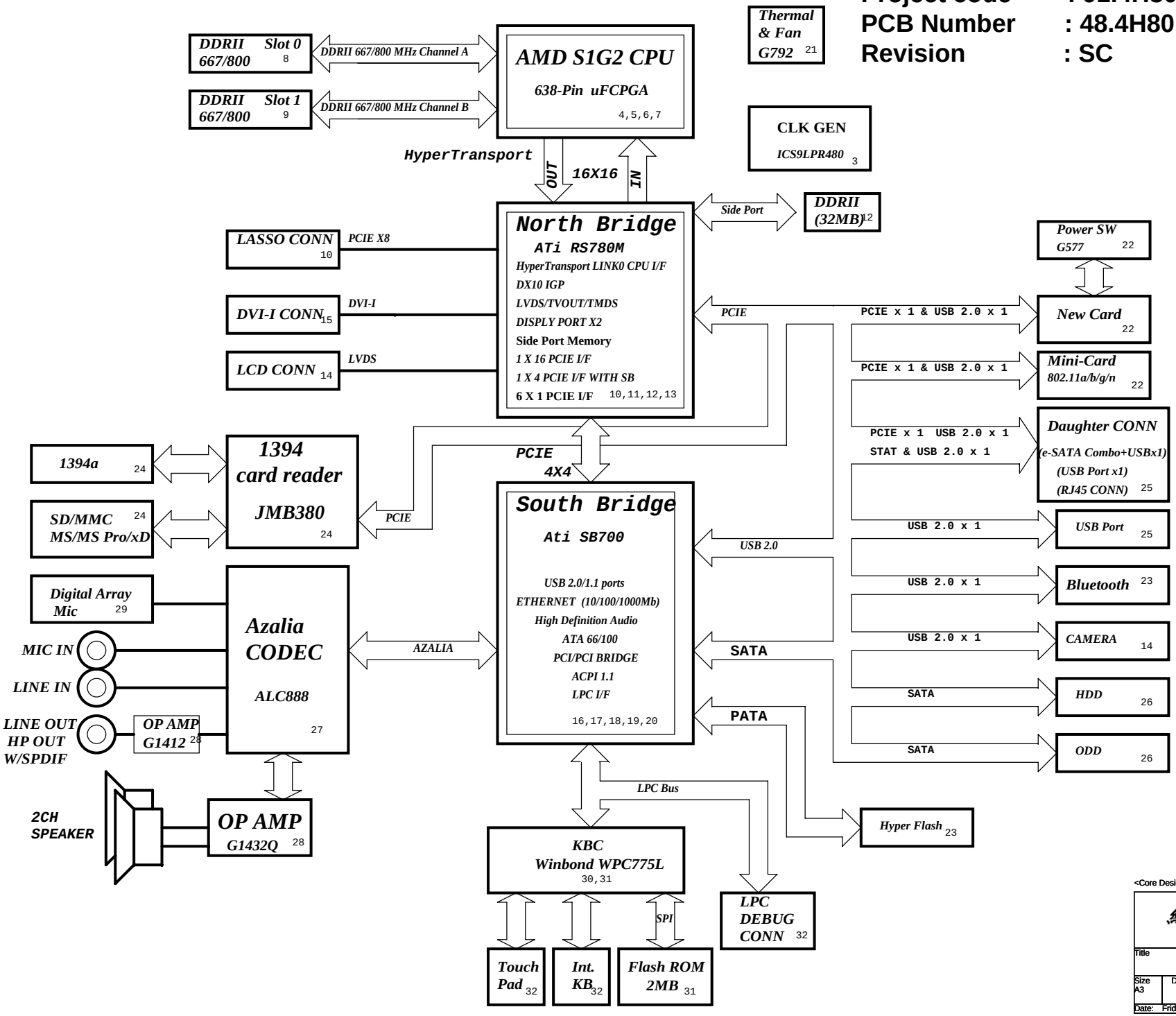
S13 Block Diagram

Project code : 91.4H801.001
PCB Number : 48.4H801.0SC
Revision : SC



CPU V_CORE ISL6265 34,35	
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51124 37	
INPUTS	OUTPUTS
DCBATOUT	1D8V_S3 1D2V_S0

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_S5 3D3V_S5

SYSTEM DC/DC LDO 39	
INPUTS	OUTPUTS
5V_S5 3D3V_S0	0D9V_S3 1D5V_S0

SYSTEM DC/DC LDO 39	
INPUTS	OUTPUTS
3D3V_S5 3D3V_S0	1D2V_S5 2D5V_S0

SYSTEM DC/DC TPS51125 36	
INPUTS	OUTPUTS
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

MAXIM CHARGER BQ24745 41	
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

<Core Design>

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Title: **System Block Diagram**

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 1 of 44

		USB PORT#	DESTINATION
SB700	2.0	0	USB1
		1	CAMERA
		2	Combo(ESATA/USB)
		3	NEW CARD
		4	USB2
		5	Bluetooth
		6	NC
		7	WLAN
		8	NC
		9	NC
		10	NC
		11	NC
	1.1	12	NC
		13	NC

PCI EXPRESS	DESTINATION
Lane 0	NEW CARD
Lane 1	WLAN
Lane 2	LAN
Lane 3	CARD READER&1394
Lane 4	NC
Lane 5	NC

RS780M Functional Strap Definitions

STRAP_DEBUG_BUS_GPIO_ENABLE

Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable

RS780: Enables Side port memory (RS780 use HSYNC)

* 0 : Enable 1 : Disable

SUS_STAT#

Selects Loading of STRAPS From EEPROM
* 1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected

SB700 Functional Strap Definitions

		PULL HIGH	PULL LOW
CLK_PCI_2	WatchDOG (NB_PWRGD)	ENABLED	DISABLED DEFAULT
CLK_PCI_3	DEBUG STRAPS	USB	IGNORE DEFAULT
CLK_PCI_1 CLK_PCI_4	RESERVED		
LPCCLK0	PCI MEM BOOT	ENABLED	DISABLED DEFAULT
LPCCLK1	INTERNAL CLK GEN	ENABLED	DISABLED DEFAULT
RTCCLK	INTERNAL RTC	ENABLED DEFAULT	DISABLED
AZ_RST#	IMC	ENABLED	DISABLED DEFAULT
SB_GPO17 SB_GPO16	ROM TYPE	H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM	

<Core Design>

緯創資通 Wistron Corporation
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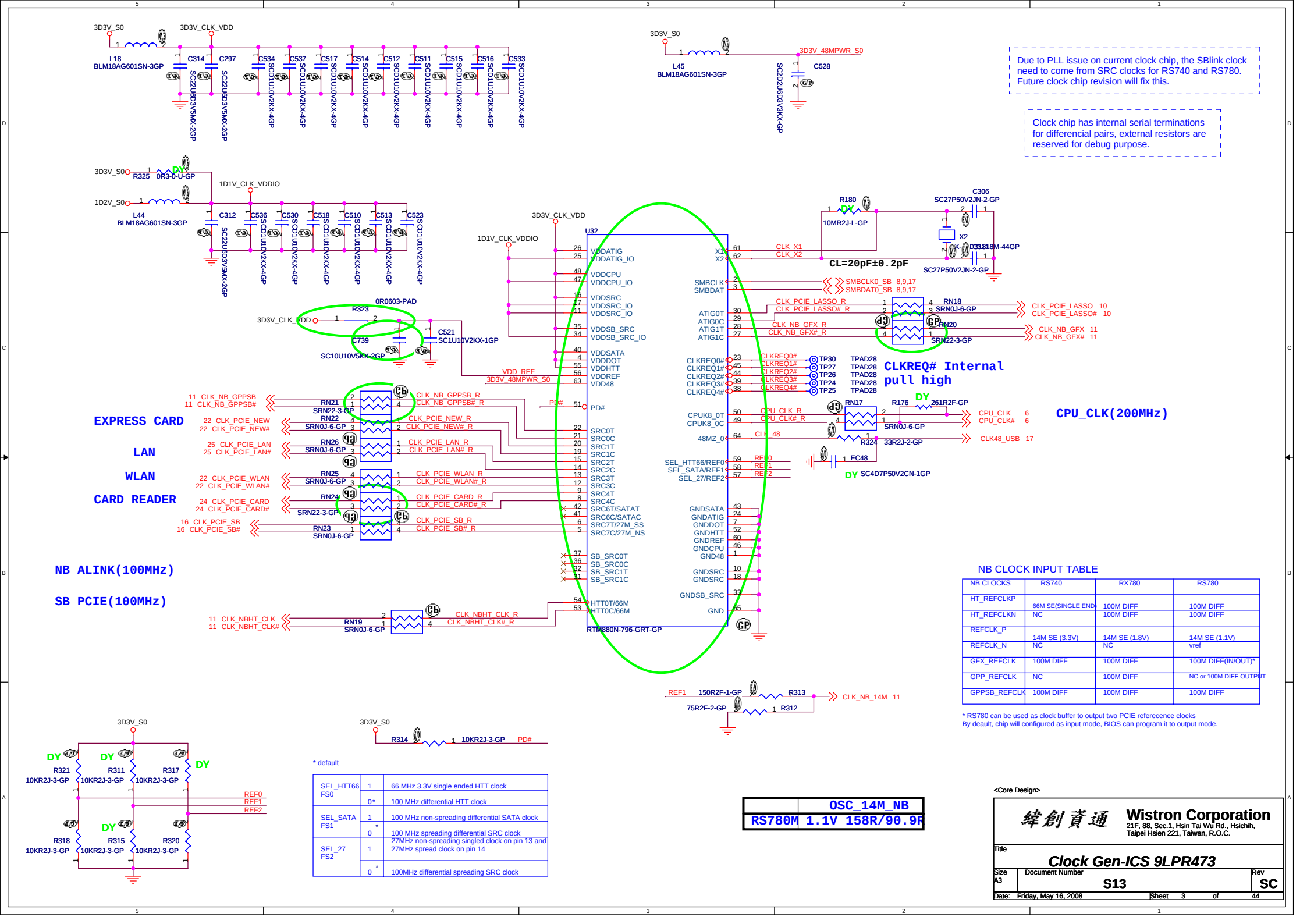
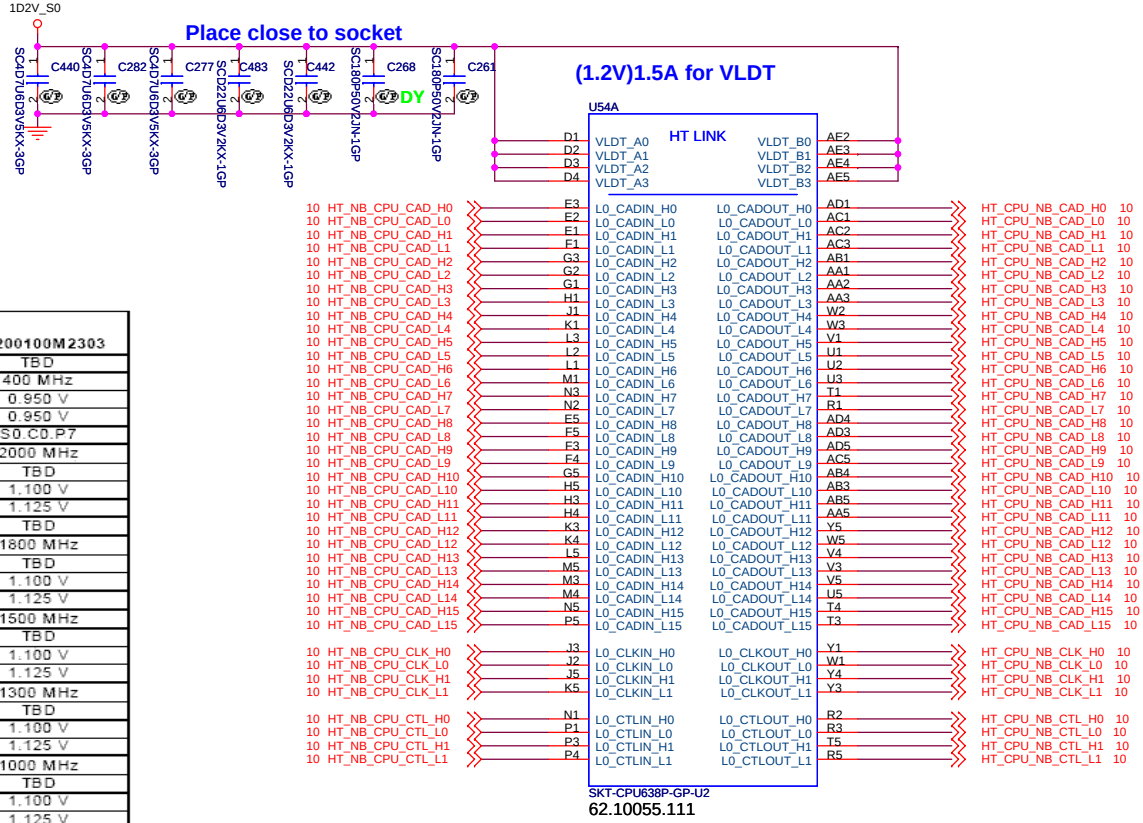
Taipei Hsien 221, Taiwan, R.O.C.

Title: Table of Content

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 2 of 44


3D3V_S0
3D3V_CLK_VDD
L18
BLM18AG601SN-3GP
C314
C297
C534
C537
C517
C514
C512
C511
C515
C516
C533
SC22U6D3V5MX-2GP
SC1U10V2KX-4GP
3D3V_S0
L45
BLM18AG601SN-3GP
3D3V_48MPWR_S0
C528
SC2D2U6D3V3KX-GP
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
DY
R325
0R3-0-U-GP
1D2V_S0
L44
BLM18AG601SN-3GP
1D1V_CLK_VDDIO
C312
C536
C530
C518
C510
C513
C523
SC22UD3V5MX-2GP
SC1U10V2KX-4GP
0R0603-PAD
R323
3D3V_CLK_VDD
C739
SC10U10V5KX-2GP
C521
SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
U32
3D3V_CLK_VDD
1D1V_CLK_VDDIO
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDDDOT
VDDHTT
VDDREF
VDD48
PD#
SRC0T
SRC0C
SRC1T
SRC1C
SRC2T
SRC2C
SRC3T
SRC3C
SRC4T
SRC4C
SRC6T/SATAT
SRC6C/SATAC
SRC7T/27M_SS
SRC7C/27M_NS
SB_SRC0T
SB_SRC0C
SB_SRC1T
SB_SRC1C
HTT0T/66M
HTT0C/66M
RTM880N-796-GRT-GP
X1
X2
CLK_X1
CLK_X2
SMBCLK
SMBDAT
SMBCLK0_SB 8,9,17
SMBDAT0_SB 8,9,17
ATIG0T
ATIG0C
ATIG1T
ATIG1C
CLK_PCIE_LASSO_R
CLK_PCIE_LASSO#_R
CLK_NB_GFX_R
CLK_NB_GFX#_R
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP30
TP27
TP26
TP24
TP25
TPAD28
CLKREQ# Internal pull high
CPUK8_0T
CPUK8_0C
CPU_CLK_R
CPU_CLK#_R
48MZ_0
CLK_48
SEL_HTT66/REF0
SEL_SATA/REF1
SEL_27/REF2
REF0
REF1
REF2
GNDSATA
GNDATIG
GNDDOT
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSB_SRC
GND
R180
DY
10MR2J-L-GP
C306
SC27P50V2JN-2-GP
X2
D33818M-44GP
SC27P50V2JN-2-GP
CL=20pF±0.2pF
RN18
SRN0J-6-GP
CLK_PCIE_LASSO 10
CLK_PCIE_LASSO# 10
RN20
SRN22-3-GP
CLK_NB_GFX 11
CLK_NB_GFX# 11
RN17
R176
DY
261R2F-GP
SRN0J-6-GP
CPU_CLK 6
CPU_CLK# 6
CPU_CLK(200MHz)
R324
33R2J-2-GP
CLK48_USB 17
EC48
DY SC4D7P50V2CN-1GP
EXPRESS CARD
LAN
WLAN
CARD READER
RN21
SRN22-3-GP
11 CLK_NB_GPPSB
11 CLK_NB_GPPSB#
CLK_NB_GPPSB_R
CLK_NB_GPPSB#_R
RN22
SRN0J-6-GP
22 CLK_PCIE_NEW
22 CLK_PCIE_NEW#
CLK_PCIE_NEW_R
CLK_PCIE_NEW#_R
RN26
SRN0J-6-GP
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
CLK_PCIE_LAN_R
CLK_PCIE_LAN#_R
RN25
SRN0J-6-GP
22 CLK_PCIE_WLAN
22 CLK_PCIE_WLAN#
CLK_PCIE_WLAN_R
CLK_PCIE_WLAN#_R
RN24
SRN22-3-GP
24 CLK_PCIE_CARD
24 CLK_PCIE_CARD#
CLK_PCIE_CARD_R
CLK_PCIE_CARD#_R
RN23
SRN0J-6-GP
16 CLK_PCIE_SB
16 CLK_PCIE_SB#
CLK_PCIE_SB_R
CLK_PCIE_SB#_R
NB ALINK(100MHz)
SB PCIE(100MHz)
RN19
SRN0J-6-GP
11 CLK_NBHT_CLK
11 CLK_NBHT_CLK#
CLK_NBHT_CLK_R
CLK_NBHT_CLK#_R
REF1
150R2F-1-GP
75R2F-2-GP
R313
R312
CLK_NB_14M 11
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
DY
R321
10KR2J-3-GP
R311
10KR2J-3-GP
R317
10KR2J-3-GP
R318
10KR2J-3-GP
R315
10KR2J-3-GP
R320
10KR2J-3-GP
REF0
REF1
REF2
3D3V_S0
R314
10KR2J-3-GP
PD#
* default
SEL_HTT66/FS0 | 1 | 66 MHz 3.3V single ended HTT clock
0* | 100 MHz differential HTT clock
SEL_SATA/FS1 | 1 | 100 MHz non-spreading differential SATA clock
0* | 100 MHz spreading differential SRC clock
SEL_27/FS2 | 1 | 27MHz non-spreading singled clock on pin 13 and 27MHz spread clock on pin 14
0* | 100MHz differential spreading SRC clock
OSC_14M_NB
RS780M 1.1V 158R/90.9F
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Gen-ICS 9LPR473
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
Sheet 3 of 44



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

<Core Design>

緯創資通 Wistron Corporation
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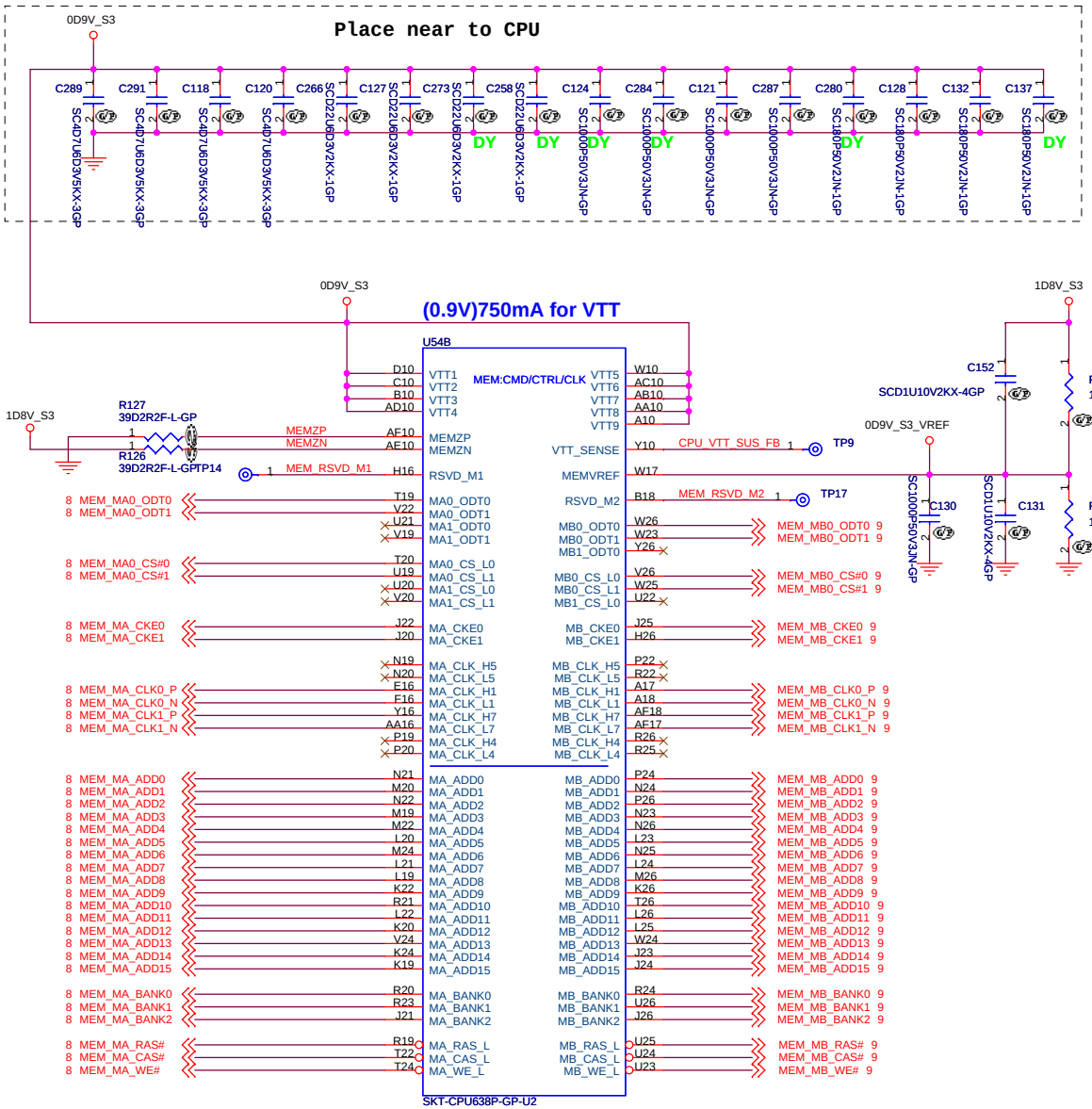
Title: CPU_HT_LINK I/F_(1/4)

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 4 of 44



<Core Design>

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Title: **CPU_DDR_(2/4)**

Size	Document Number	Rev
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LYAOUT:ROUTE VDDA TRACE APPROX.
50mils WIDE(USE 2X25 mil TRACES TO
EXIT BALL FIELD) AND 500 mils LONG.

(2.5V)250mA for VDDA

CPU exceeds to 125℃

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

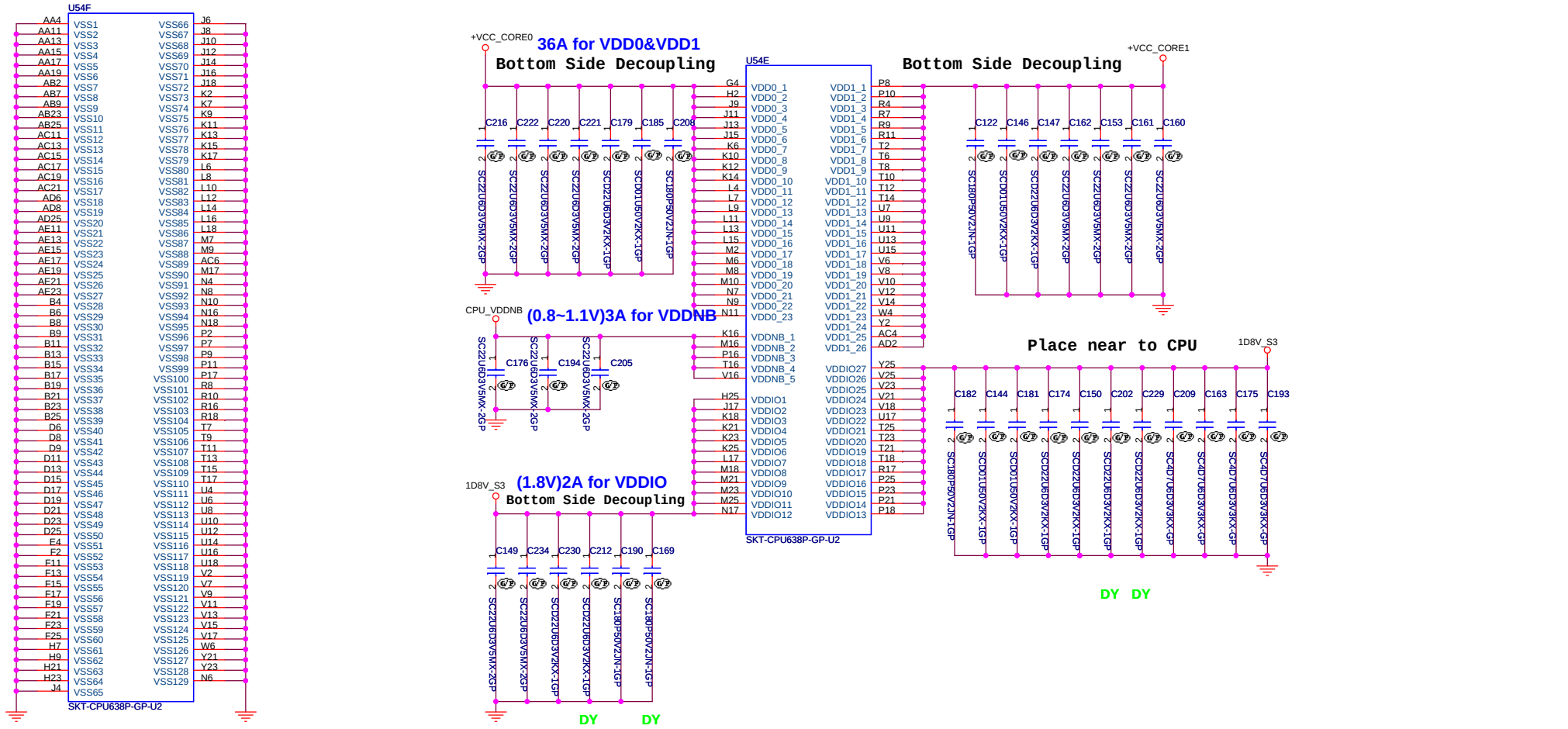
For HDT DBG

FDV301N, the Vgs is:
min = 0.65V
Typ = 0.85V
Max = 1.5V

HDT Connectors

<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***CPU_Control&Debug_(3/4)***		
Size: A3	Document Number: **S13**	Rev: **SC**
Date: Friday, May 16, 2008	Sheet 6 of 44	



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU_Power_(4/4)

Size	Document Number	Rev
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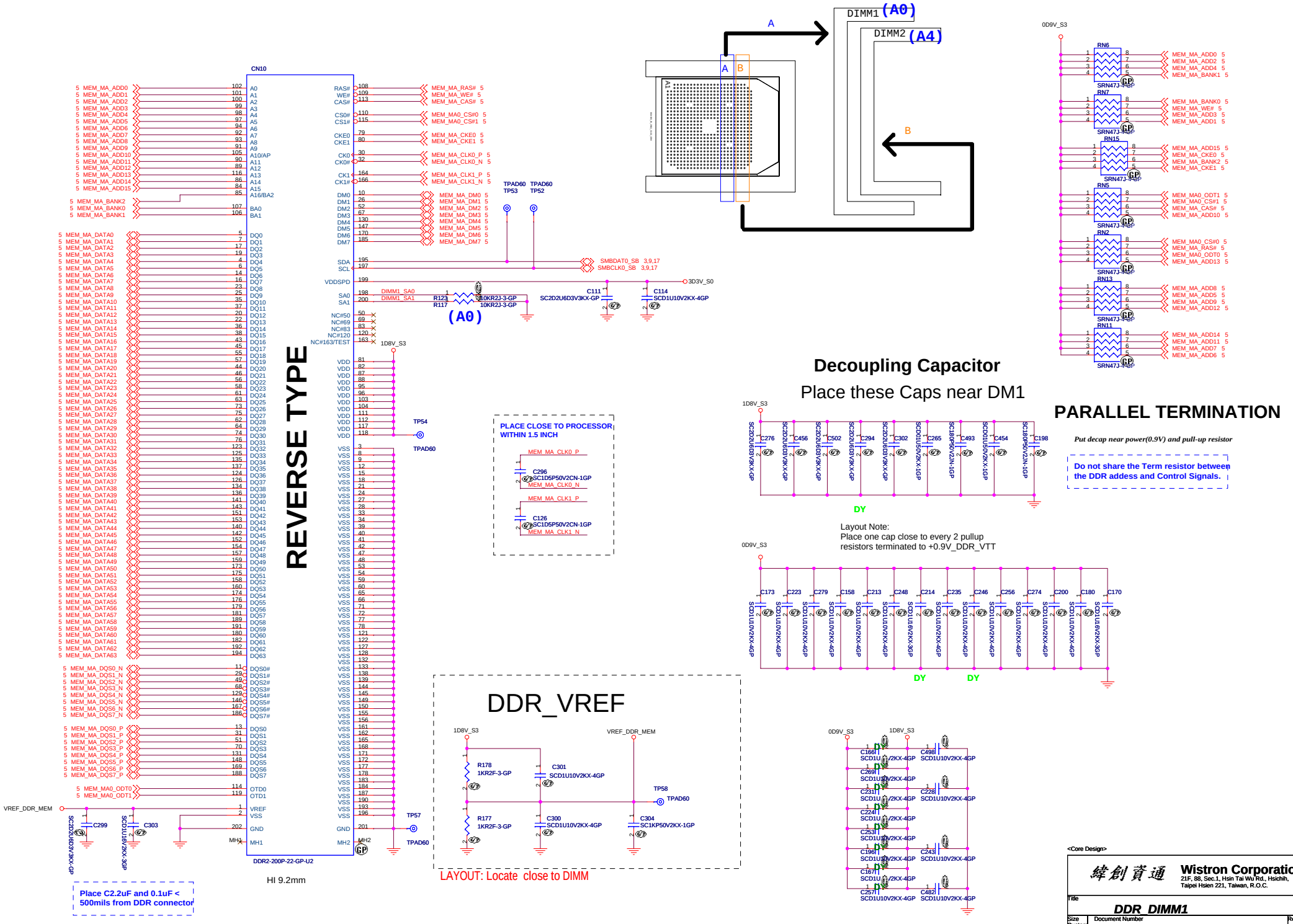
Date: Friday, May 16, 2008 Sheet 7 of 44


DIMM1 (A0)
DIMM2 (A4)
A
B
CN10
REVERSE TYPE
DDR2-200P-22-GP-U2
HI 9.2mm
(A0)
PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH
DDR_VREF
LAYOUT: Locate close to DIMM
Place C2.2uF and 0.1uF < 500mils from DDR connector
Decoupling Capacitor
Place these Caps near DM1
PARALLEL TERMINATION
Put decap near power(0.9V) and pull-up resistor
Do not share the Term resistor between the DDR addess and Control Signals.
Layout Note:
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT
DY
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
DDR_DIMM1
S13
SC
Friday, May 16, 2008
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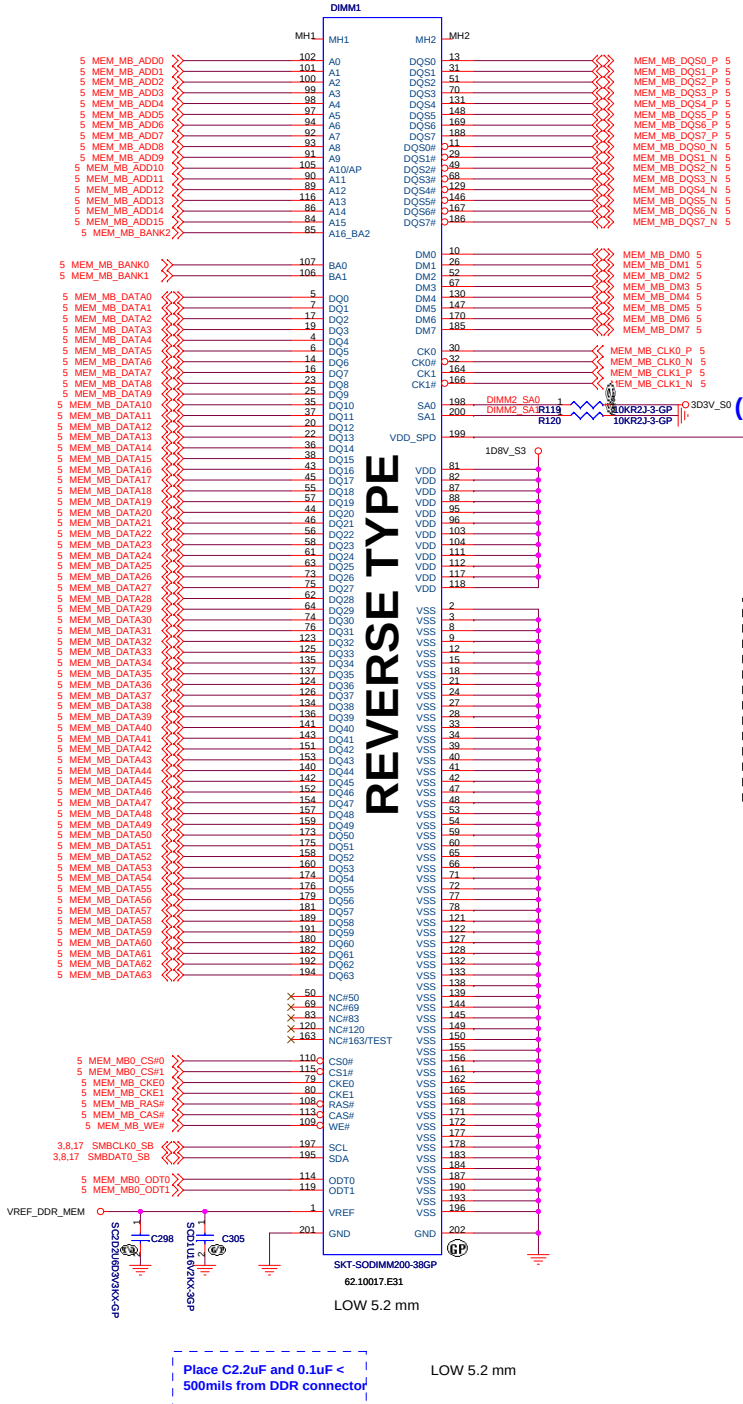
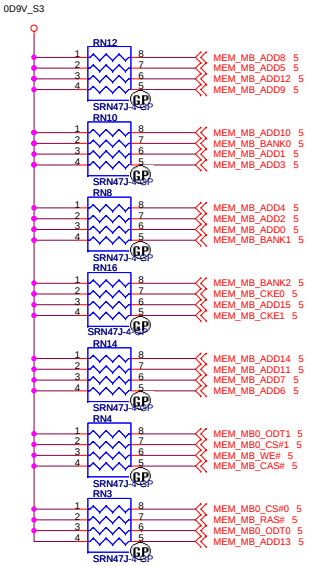
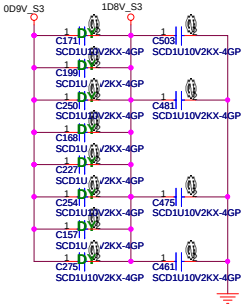


PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

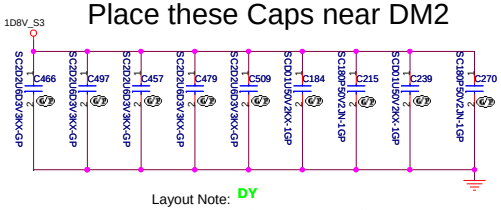
Do not share the Term resistor between the DDR addess and Control Signals.



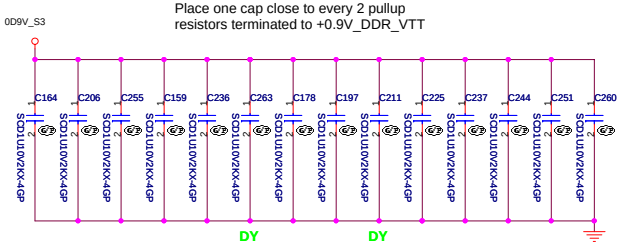


Decoupling Capacitor

Place these Caps near DM2



Layout Note: DY
Place one cap close to every 2 pullup resistors terminated to +0.9V_DDR_VTT



<Core Design>

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Title: DDR_DIMM2

Size	Document Number	Rev
Custom	S13	SC

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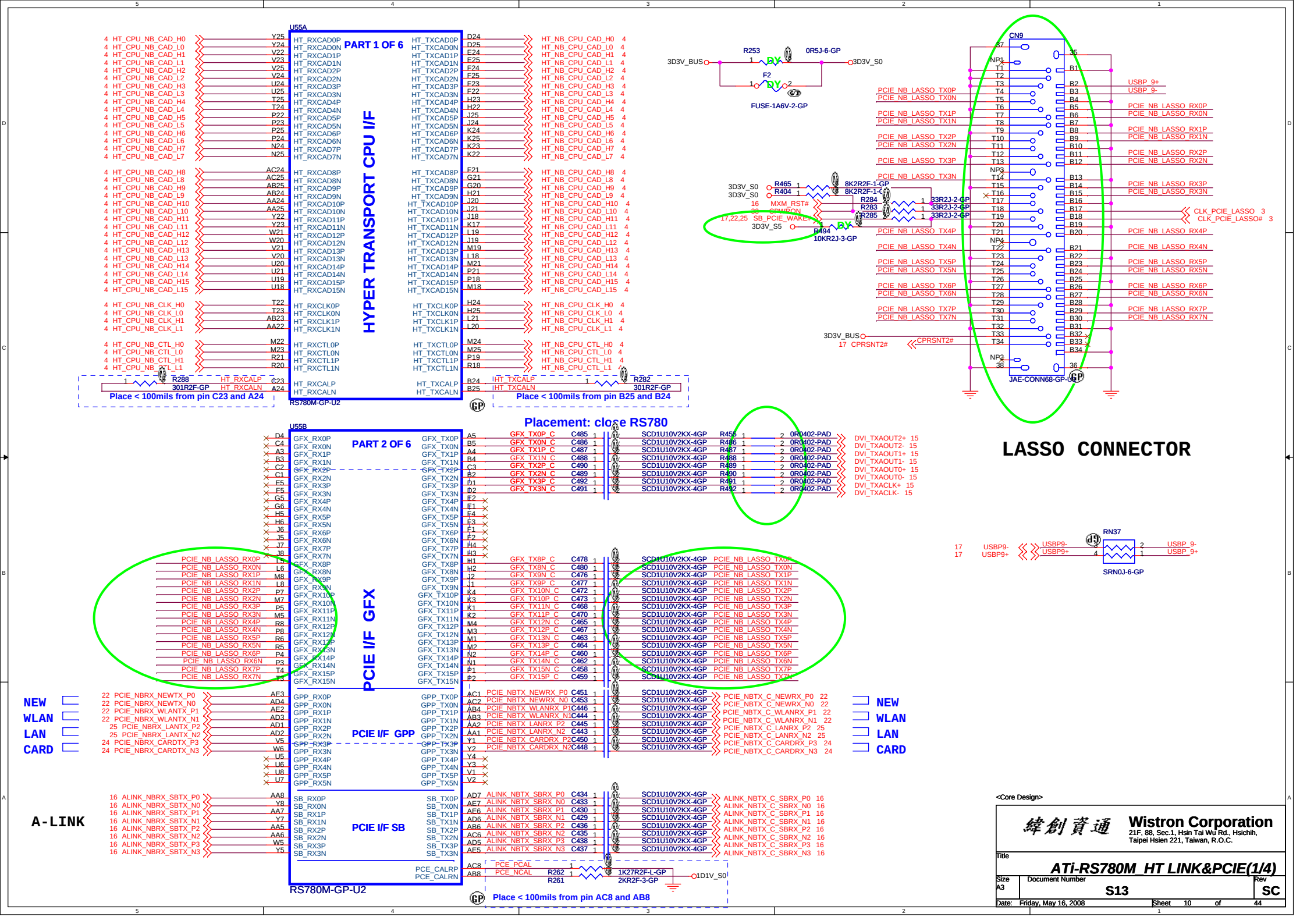
U55A
PART 1 OF 6
HYPER TRANSPORT CPU I/F
RS780M-GP-U2
Place < 100mils from pin C23 and A24
Place < 100mils from pin B25 and B24
Placement: close RS780
U55B
PART 2 OF 6
PCIE I/F GFX
PCIE I/F GPP
PCIE I/F SB
RS780M-GP-U2
Place < 100mils from pin AC8 and AB8
FUSE-1A6V-2-GP
CN9
JAE-CONN68-GP-U
LASSO CONNECTOR
SRN0J-6-GP
NEW
WLAN
LAN
CARD
A-LINK
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_HT LINK&PCIE(1/4)
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
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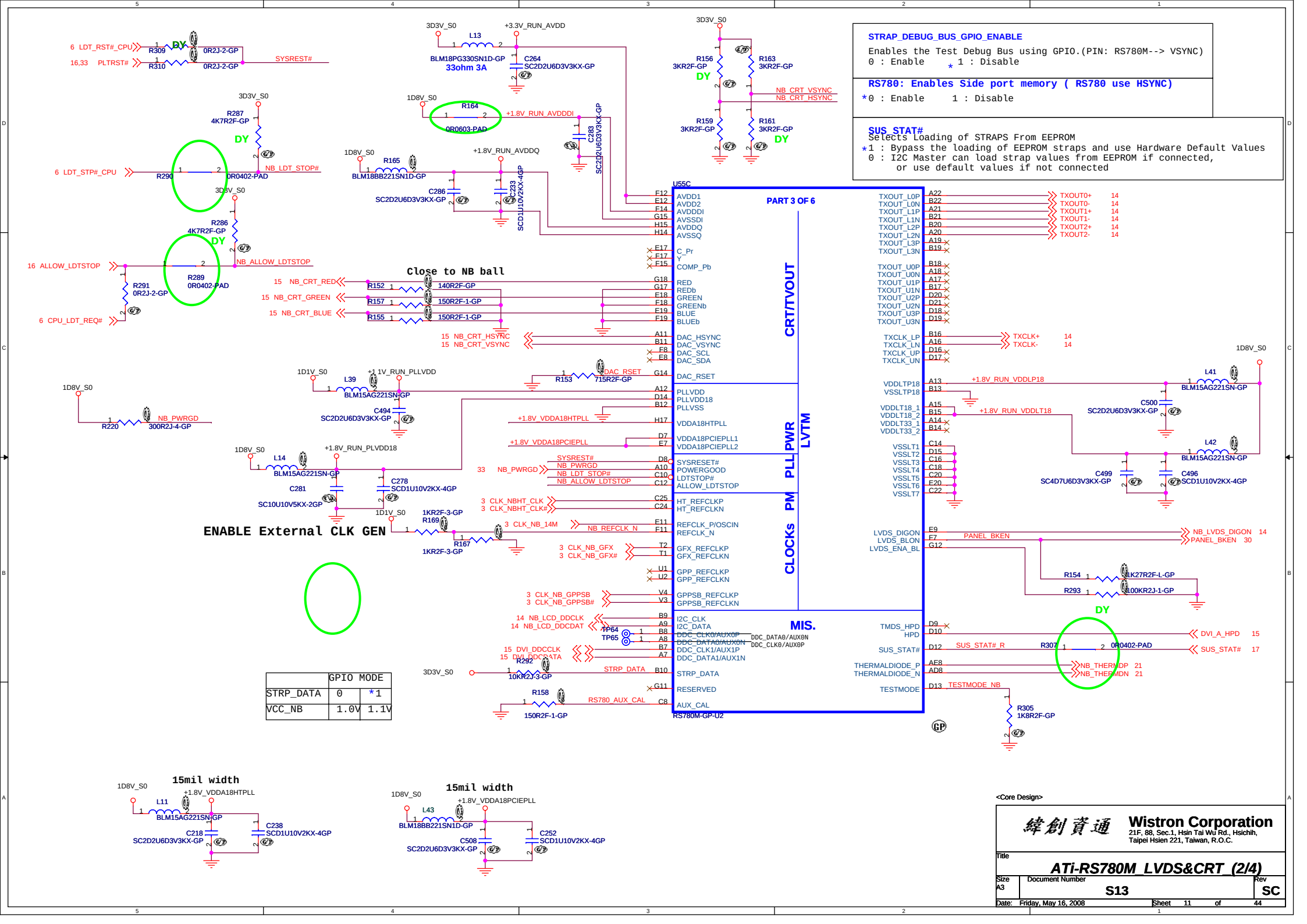
STRAP_DEBUG_BUS_GPIO_ENABLE
Enables the Test Debug Bus using GPIO.(PIN: RS780M--> VSYNC)
0 : Enable * 1 : Disable
RS780: Enables Side port memory (RS780 use HSYNC)
*0 : Enable 1 : Disable
SUS_STAT#
Selects Loading of STRAPS From EEPROM
*1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected,
or use default values if not connected
Close to NB ball
ENABLE External CLK GEN
15mil width
15mil width
PART 3 OF 6
CRT/TVOUT
PWR
LVTM
PLL
PM
CLOCKs
MIS.
RS780M-GP-U2
GPIO MODE
STRP_DATA 0 *1
VCC_NB 1.0V 1.1V
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
ATi-RS780M_LVDS&CRT_(2/4)
S13
SC
Friday, May 16, 2008
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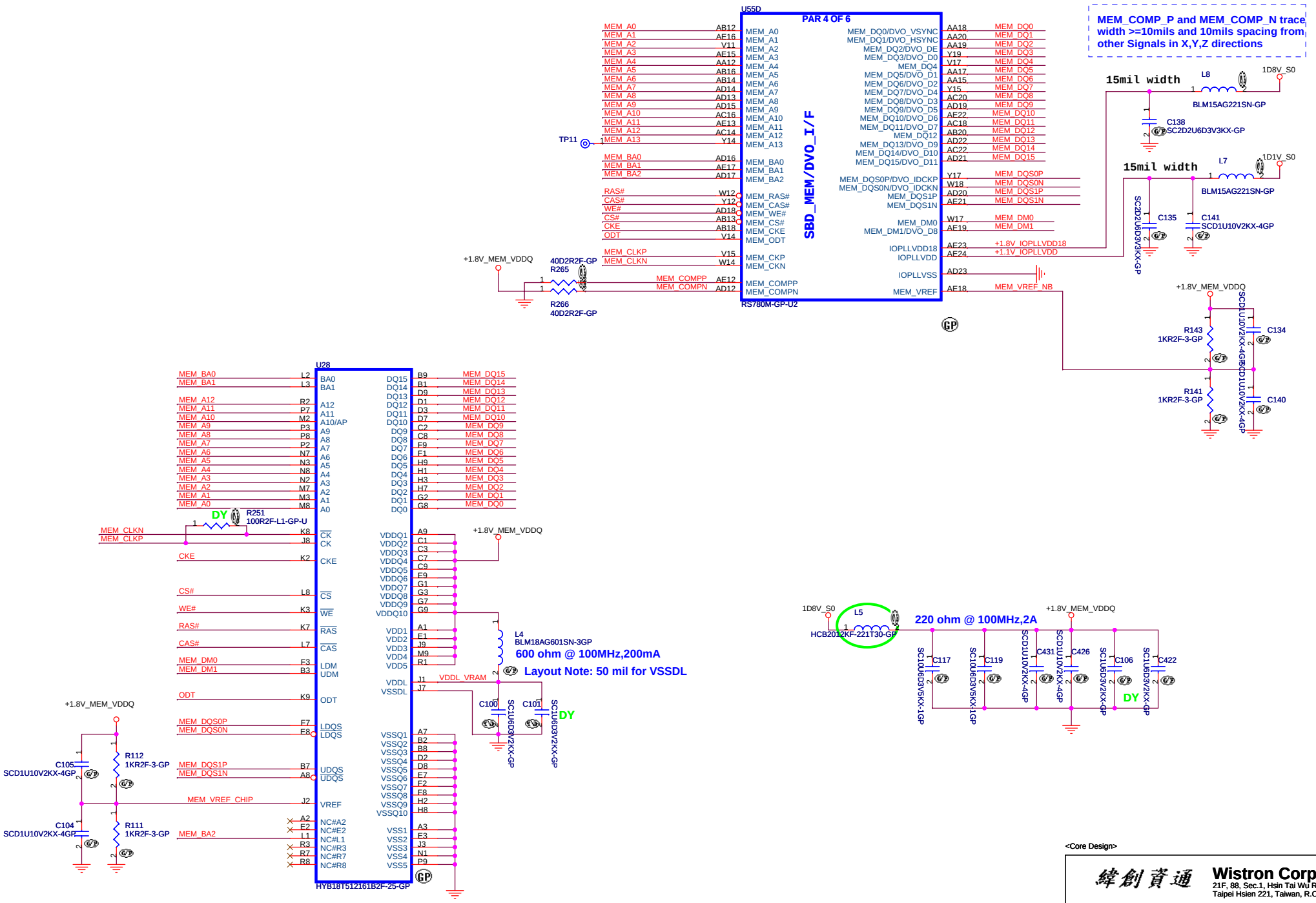


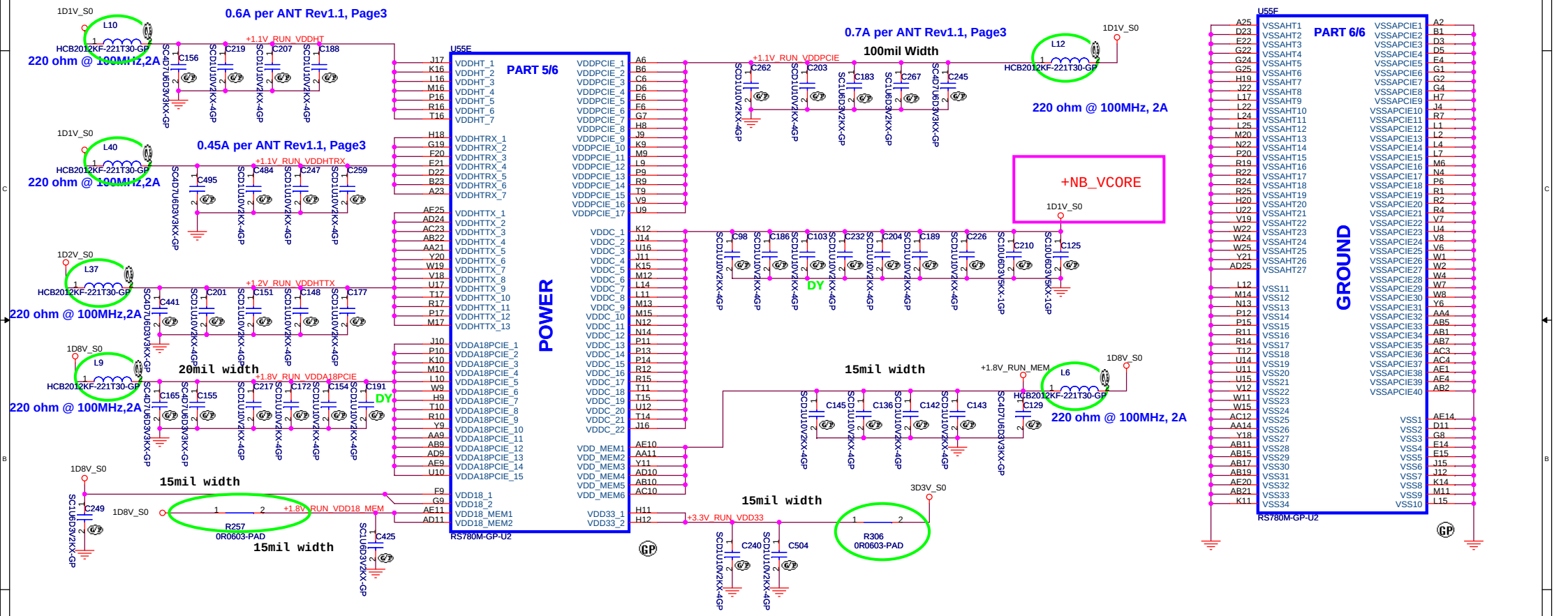
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-RS780M_SidePort_(3/4)

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 12 of 44



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

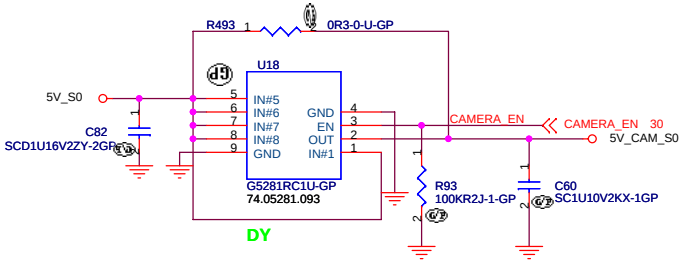
Title: ATi-RS780M_PWR&GD_(4/4)

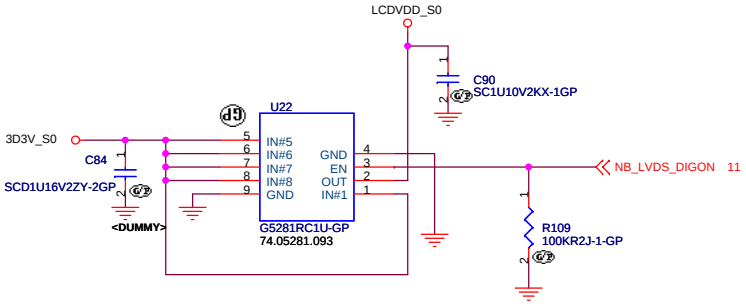
Size: A3 | Document Number: S13 | Rev: SC

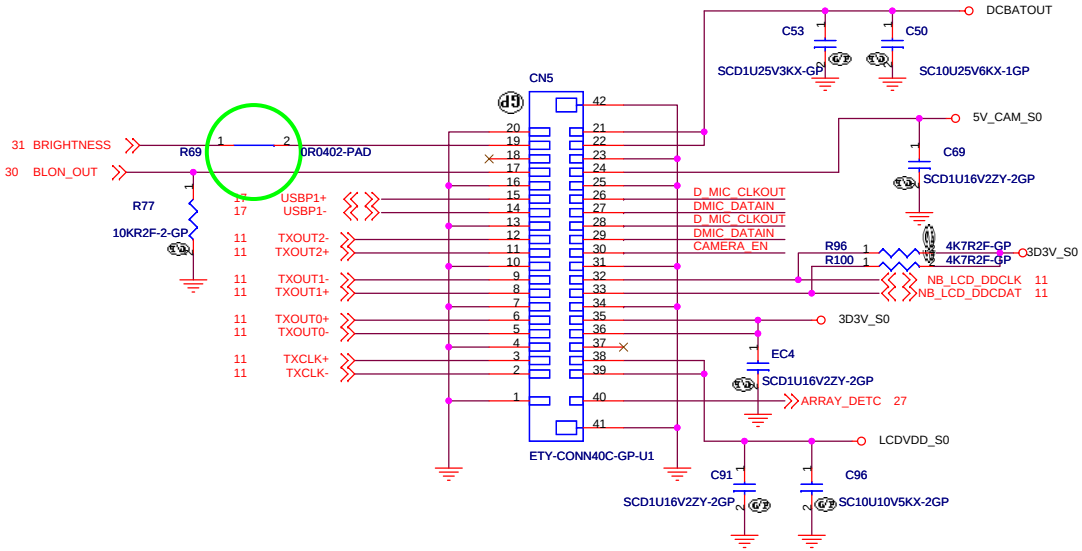
Date: Friday, May 16, 2008 | Sheet 13 of 44

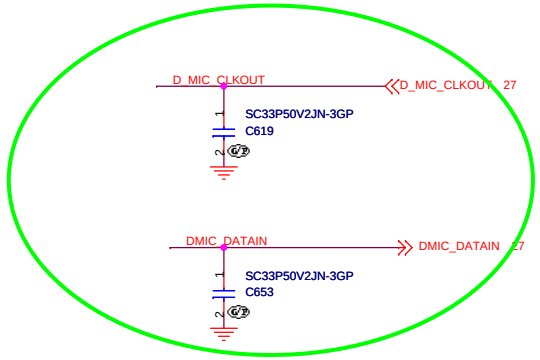
LCD CONNECTOR

CAMERA POWER

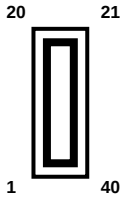








TOP VIEW



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LCD CONN/CAMERA**

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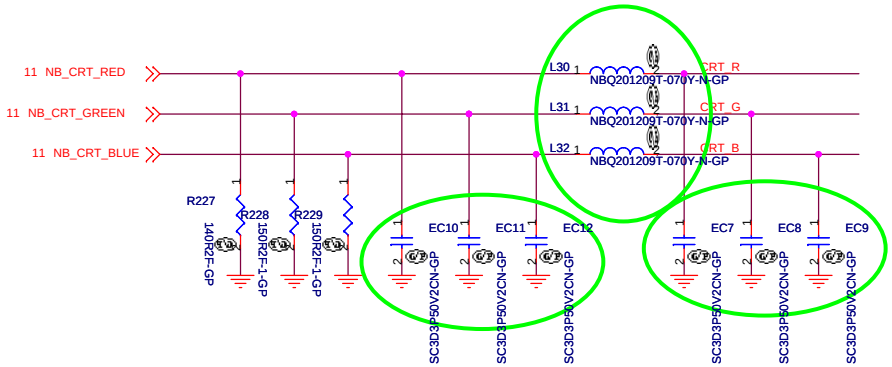
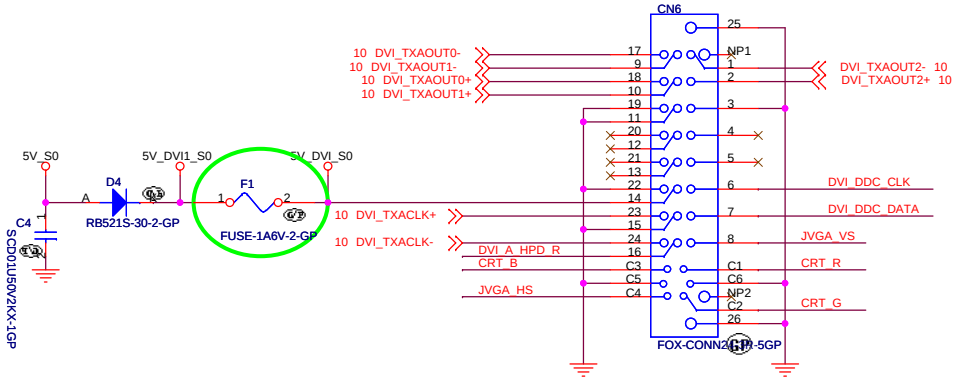
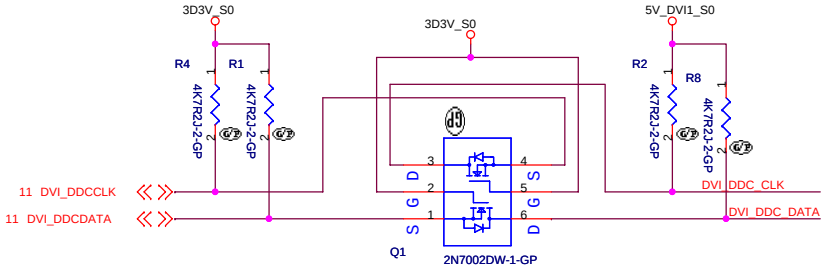
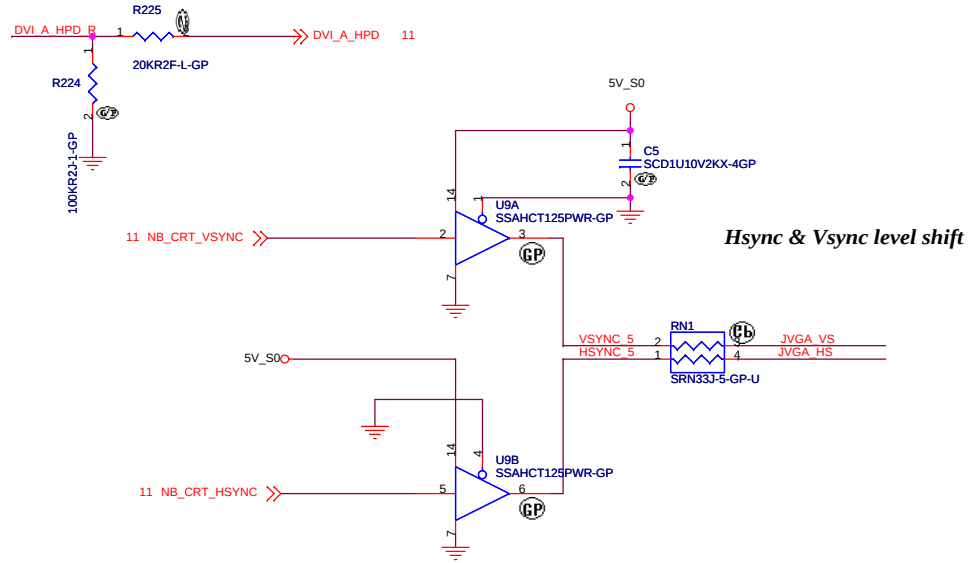
Date: Friday, May 16, 2008 Sheet 14 of 44

Layout Note:
Place these resistors close to the connector

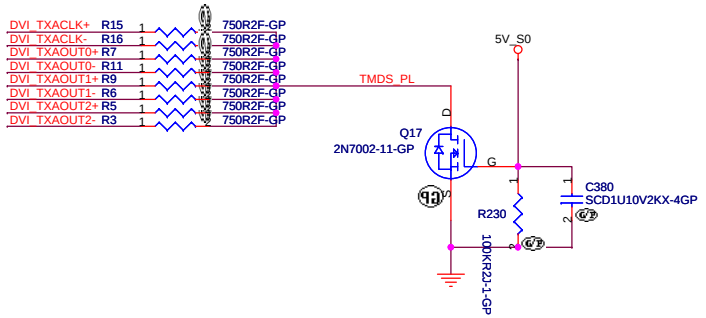








Hsync & Vsync level shift



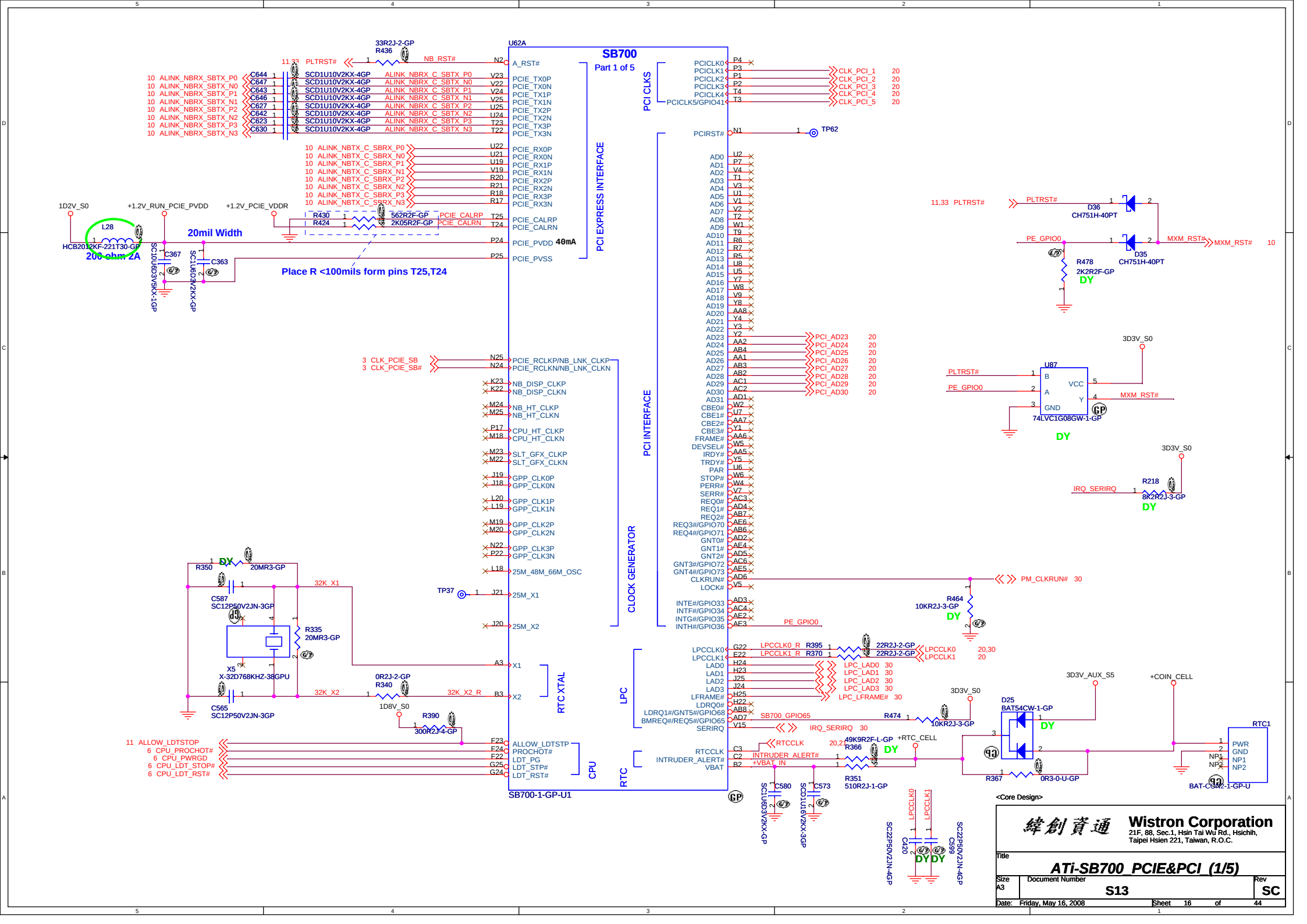
<Core Design>

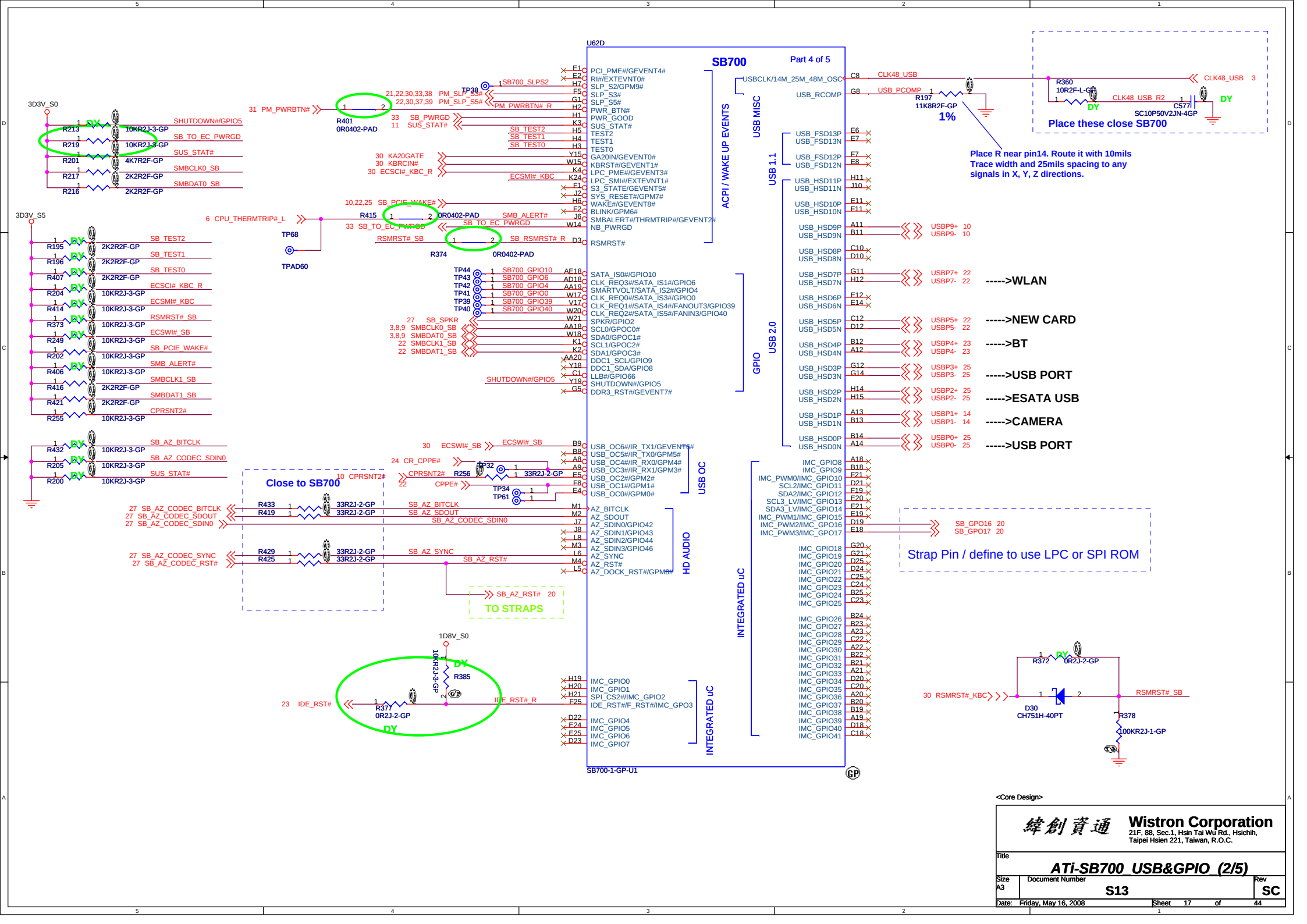
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **DVI CONN**

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 15 of 44


SB700
Part 1 of 5
U62A
SB700-1-GP-U1
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
33R2J-2-GP
R436
NB_RST#
A_RST#
PCIE_TX0P
PCIE_TX0N
PCIE_TX1P
PCIE_TX1N
PCIE_TX2P
PCIE_TX2N
PCIE_TX3P
PCIE_TX3N
PCIE_RX0P
PCIE_RX0N
PCIE_RX1P
PCIE_RX1N
PCIE_RX2P
PCIE_RX2N
PCIE_RX3P
PCIE_RX3N
PCIE_CALRP
PCIE_CALRN
PCIE_PVDD 40mA
PCIE_PVSS
PCICLK0
PCICLK1
PCICLK2
PCICLK3
PCICLK4
PCICLK5/GPIO41
PCIRST#
TP62
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
CBE0#
CBE1#
CBE2#
CBE3#
FRAME#
DEVSEL#
IRDY#
TRDY#
PAR
STOP#
PERR#
SERR#
REQ0#
REQ1#
REQ2#
REQ3#/GPIO70
REQ4#/GPIO71
GNT0#
GNT1#
GNT2#
GNT3#/GPIO72
GNT4#/GPIO73
CLKRUN#
LOCK#
INTE#/GPIO33
INTF#/GPIO34
INTG#/GPIO35
INTH#/GPIO36
PE_GPIO0
PM_CLKRUN# 30
R464
10KR2J-3-GP
DY
NB_DISP_CLKP
NB_DISP_CLKN
NB_HT_CLKP
NB_HT_CLKN
CPU_HT_CLKP
CPU_HT_CLKN
SLT_GFX_CLKP
SLT_GFX_CLKN
GPP_CLK0P
GPP_CLK0N
GPP_CLK1P
GPP_CLK1N
GPP_CLK2P
GPP_CLK2N
GPP_CLK3P
GPP_CLK3N
25M_48M_66M_OSC
25M_X1
25M_X2
X1
X2
32K_X1
32K_X2
32K_X2_R
TP37
R350
20MR3-GP
R335
20MR3-GP
C587
SC12P50V2JN-3GP
C565
SC12P50V2JN-3GP
X5
X-32D768KHZ-38GPU
0R2J-2-GP
R340
1D8V_S0
R390
300R2J-4-GP
LPCCLK0_R
LPCCLK1_R
R395
R370
22R2J-2-GP
LPCCLK0
LPCCLK1
20,30
20
LAD0
LAD1
LAD2
LAD3
LFRAME#
LDRQ0#
LDRQ1#/GNT5#/GPIO68
BMREQ#/REQ5#/GPIO65
SERIRQ
LPC_LAD0 30
LPC_LAD1 30
LPC_LAD2 30
LPC_LAD3 30
LPC_LFRAME# 30
SB700_GPIO65
IRQ_SERIRQ 30
R474
10KR2J-3-GP
3D3V_S0
RTCCLK
INTRUDER_ALERT#
VBAT
+VBAT_IN
20,21
49K9R2F-L-GP
R366
DY
+RTC_CELL
R351
510R2J-1-GP
C580
SCD1U16V2KX-3GP
C573
SCD1U16V2KX-3GP
D25
BAT54CW-1-GP
3D3V_AUX_S5
+COIN_CELL
RTC1
BAT-CON2-1-GP-U
R367
0R3-0-U-GP
ALLOW_LDTSTP
PROCHOT#
LDT_PG
LDT_STP#
LDT_RST#
11 ALLOW_LDTSTOP
6 CPU_PROCHOT#
6 CPU_PWRGD
6 CPU_LDT_STOP#
6 CPU_LDT_RST#
3 CLK_PCIE_SB
3 CLK_PCIE_SB#
PCIE_RCLKP/NB_LNK_CLKP
PCIE_RCLKN/NB_LNK_CLKN
CLK_PCI_1 20
CLK_PCI_2 20
CLK_PCI_3 20
CLK_PCI_4 20
CLK_PCI_5 20
PCI_AD23 20
PCI_AD24 20
PCI_AD25 20
PCI_AD26 20
PCI_AD27 20
PCI_AD28 20
PCI_AD29 20
PCI_AD30 20
ALINK_NBRX_SBTX_P0
ALINK_NBRX_SBTX_N0
ALINK_NBRX_SBTX_P1
ALINK_NBRX_SBTX_N1
ALINK_NBRX_SBTX_P2
ALINK_NBRX_SBTX_N2
ALINK_NBRX_SBTX_P3
ALINK_NBRX_SBTX_N3
ALINK_NBRX_C_SBTX_P0
ALINK_NBRX_C_SBTX_N0
ALINK_NBRX_C_SBTX_P1
ALINK_NBRX_C_SBTX_N1
ALINK_NBRX_C_SBTX_P2
ALINK_NBRX_C_SBTX_N2
ALINK_NBRX_C_SBTX_P3
ALINK_NBRX_C_SBTX_N3
SCD1U10V2KX-4GP
ALINK_NBTX_C_SBRX_P0
ALINK_NBTX_C_SBRX_N0
ALINK_NBTX_C_SBRX_P1
ALINK_NBTX_C_SBRX_N1
ALINK_NBTX_C_SBRX_P2
ALINK_NBTX_C_SBRX_N2
ALINK_NBTX_C_SBRX_P3
ALINK_NBTX_C_SBRX_N3
R430
R424
562R2F-GP
2K05R2F-GP
1D2V_S0
+1.2V_RUN_PCIE_PVDD
+1.2V_PCIE_VDDR
L28
HCB2012KF-221T30-GP
200 ohm 2A
20mil Width
C367
C363
SC10U6D3V5KX-1GP
SC1U6D3V2KX-GP
Place R <100mils form pins T25,T24
11,33 PLTRST#
PLTRST#
D36
CH751H-40PT
PE_GPIO0
D35
CH751H-40PT
MXM_RST#
MXM_RST# 10
R478
2K2R2F-GP
DY
U87
74LVC1G08GW-1-GP
IRQ_SERIRQ
R218
8K2R2J-3-GP
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_PCIE&PCI_(1/5)
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
Sheet 16 of 44



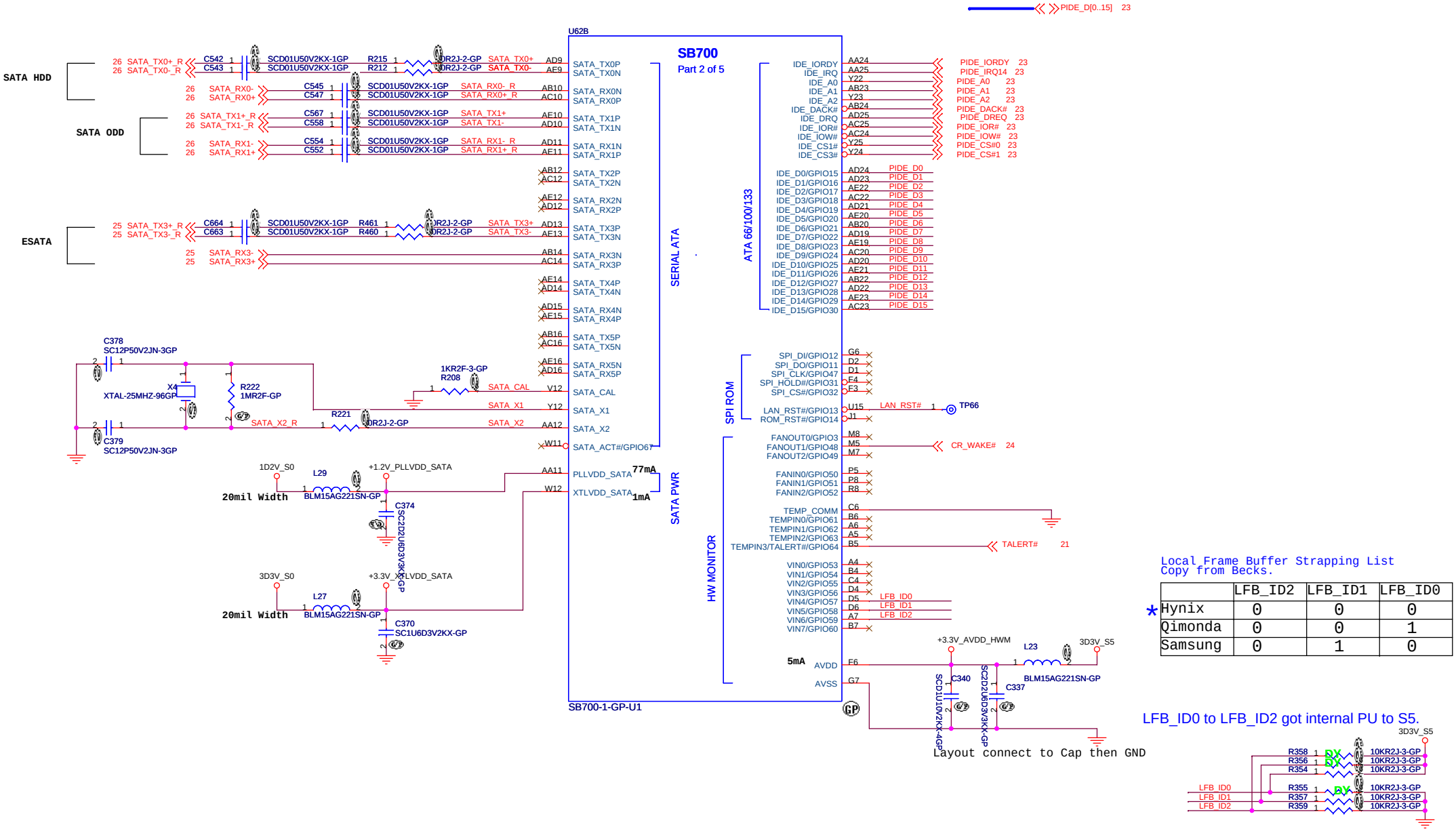
<Core Design>

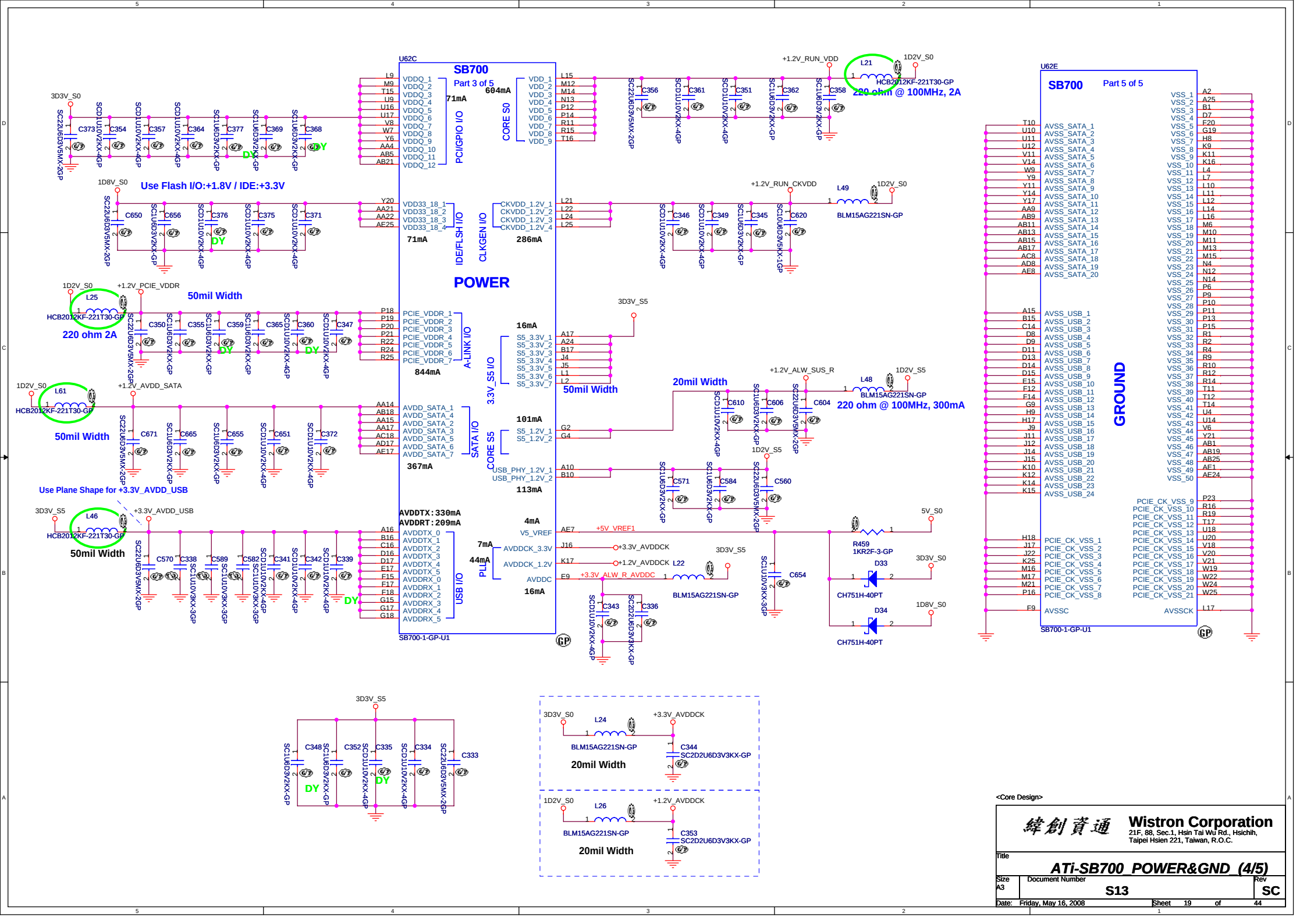
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_USB&GPIO_(2/5)

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 17 of 44


SATA HDD
SATA ODD
ESATA
U62B
SB700
Part 2 of 5
SERIAL ATA
ATA 66/100/133
SPI ROM
HW MONITOR
SATA PWR
SB700-1-GP-U1
PIDE_D[0..15] 23
SATA_TX0P
SATA_TX0N
SATA_RX0N
SATA_RX0P
SATA_TX1P
SATA_TX1N
SATA_RX1N
SATA_RX1P
SATA_TX2P
SATA_TX2N
SATA_RX2N
SATA_RX2P
SATA_TX3P
SATA_TX3N
SATA_RX3N
SATA_RX3P
SATA_TX4P
SATA_TX4N
SATA_RX4N
SATA_RX4P
SATA_TX5P
SATA_TX5N
SATA_RX5N
SATA_RX5P
SATA_CAL
SATA_X1
SATA_X2
SATA_ACT#/GPIO67
PLLVDD_SATA
XTLVDD_SATA
77mA
1mA
5mA
AVDD
AVSS
IDE_IORDY
IDE_IRQ
IDE_A0
IDE_A1
IDE_A2
IDE_DACK#
IDE_DRQ
IDE_IOR#
IDE_IOW#
IDE_CS1#
IDE_CS3#
IDE_D0/GPIO15
IDE_D1/GPIO16
IDE_D2/GPIO17
IDE_D3/GPIO18
IDE_D4/GPIO19
IDE_D5/GPIO20
IDE_D6/GPIO21
IDE_D7/GPIO22
IDE_D8/GPIO23
IDE_D9/GPIO24
IDE_D10/GPIO25
IDE_D11/GPIO26
IDE_D12/GPIO27
IDE_D13/GPIO28
IDE_D14/GPIO29
IDE_D15/GPIO30
SPI_DI/GPIO12
SPI_DO/GPIO11
SPI_CLK/GPIO47
SPI_HOLD#/GPIO31
SPI_CS#/GPIO32
LAN_RST#/GPIO13
ROM_RST#/GPIO14
FANOUT0/GPIO3
FANOUT1/GPIO48
FANOUT2/GPIO49
FANIN0/GPIO50
FANIN1/GPIO51
FANIN2/GPIO52
TEMP_COMM
TEMPIN0/GPIO61
TEMPIN1/GPIO62
TEMPIN2/GPIO63
TEMPIN3/TALERT#/GPIO64
VIN0/GPIO53
VIN1/GPIO54
VIN2/GPIO55
VIN3/GPIO56
VIN4/GPIO57
VIN5/GPIO58
VIN6/GPIO59
VIN7/GPIO60
LAN_RST#
TP66
CR_WAKE# 24
TALERT# 21
LFB_ID0
LFB_ID1
LFB_ID2
+3.3V_AVDD_HWM
3D3V_S5
L23
BLM15AG221SN-GP
C340
C337
SCD1U10V2KX-4GP
SC2D2U6D3V3KX-GP
XTAL-25MHZ-96GP
R222 1MR2F-GP
R208 1KR2F-3-GP
R221 0R2J-2-GP
C378 SC12P50V2JN-3GP
C379 SC12P50V2JN-3GP
1D2V_S0
+1.2V_PLLVDD_SATA
L29
20mil Width
C374
SC2D2U6D3V3KX-GP
3D3V_S0
+3.3V_XTLVDD_SATA
L27
C370 SC1U6D3V2KX-GP
Local Frame Buffer Strapping List
Copy from Becks.
Hynix 0 0 0
Qimonda 0 0 1
Samsung 0 1 0
LFB_ID0 to LFB_ID2 got internal PU to S5.
R358 R356 R354 R355 R357 R359
10KR2J-3-GP
Layout connect to Cap then GND
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ATi-SB700_SATA-IDE_(3/5)
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
Sheet 18 of 44



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_POWER&GND_(4/5)

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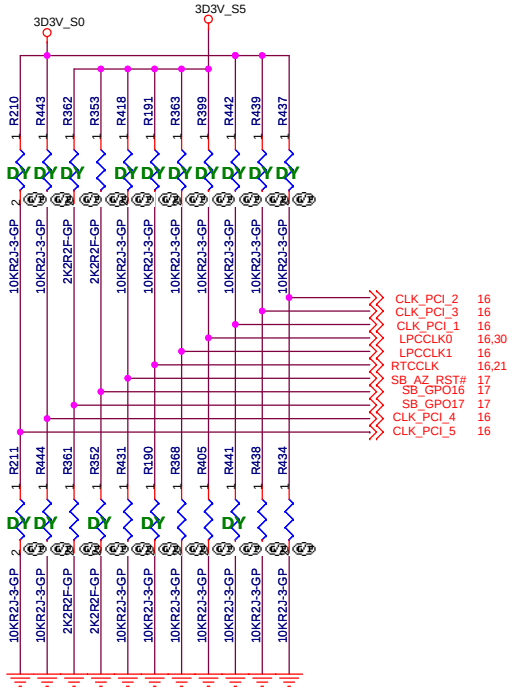
REQUIRED STRAPS

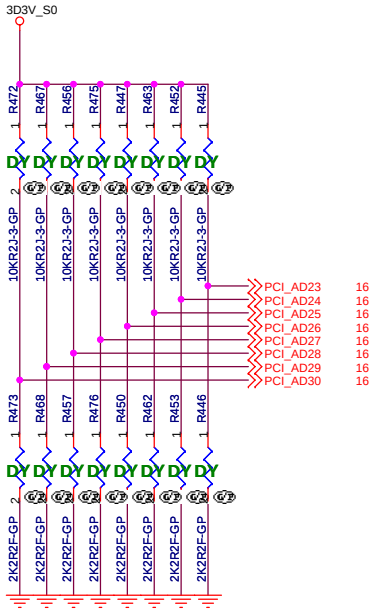


REQUIRED SYSTEM STRAPS

	CLK_PCI_2	CLK_PCI_3	CLK_PCI_4 CLK_PCI_5	LPCCLK0	LPCCLK1	RTCCLK	AZ_RST#	SB_GPO17 , SBGPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	IMC ENABLED	ROM TYPE: H, H = Reserved H, L = SPI ROM L, H = LPC ROM DEFAULT L, L = FWH ROM
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	IMC DISABLED DEFAULT	

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

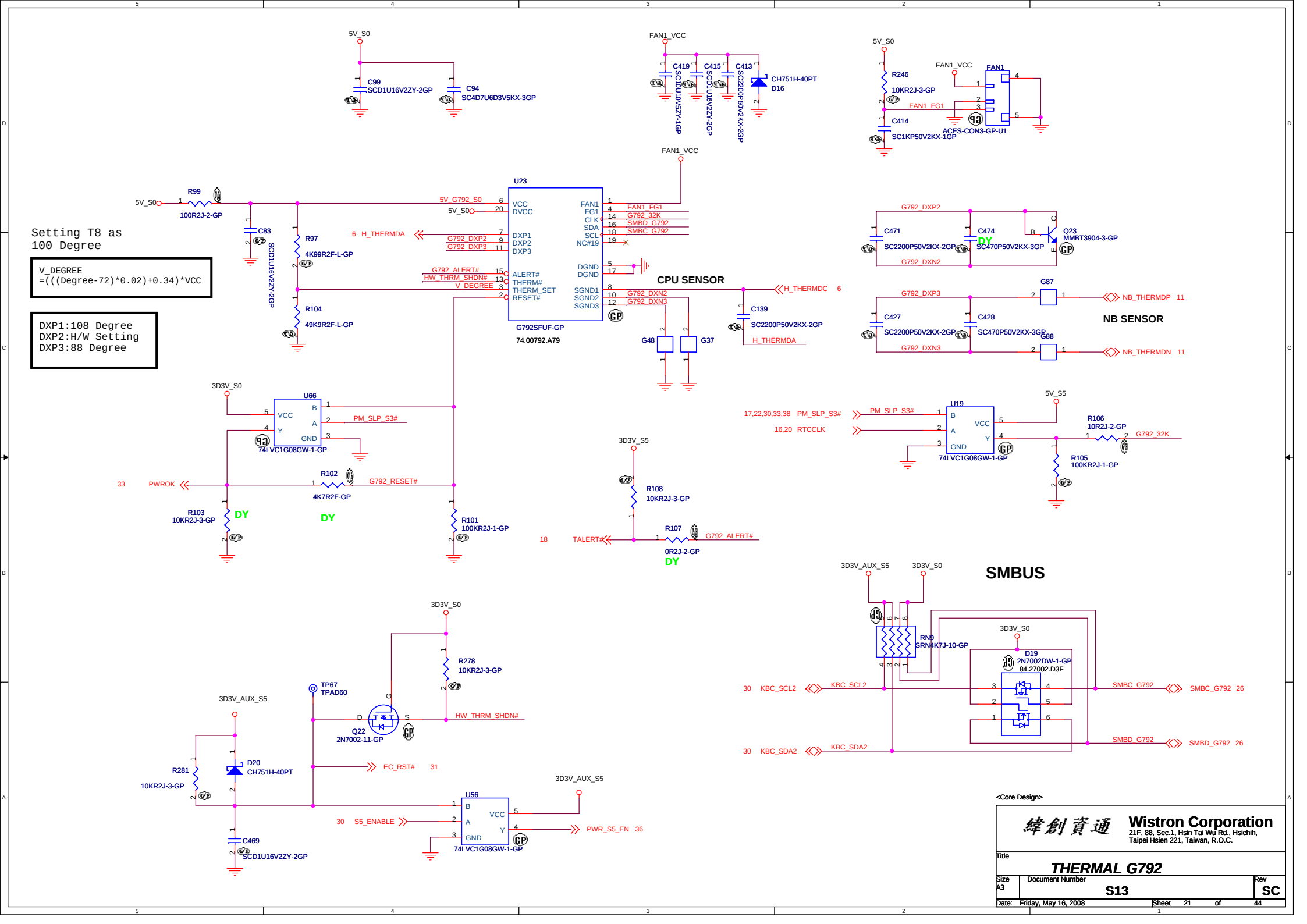
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ATi-SB700_STRAPPING_(5/5)

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 20 of 44


Setting T8 as
100 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
CPU SENSOR
NB SENSOR
SMBUS
U23
G792SFUF-GP
74.00792.A79
U66
74LVC1G08GW-1-GP
U19
74LVC1G08GW-1-GP
U56
74LVC1G08GW-1-GP
Q22
2N7002-11-GP
Q23
MMBT3904-3-GP
D16
CH751H-40PT
D20
CH751H-40PT
D19
2N7002DW-1-GP
84.27002.D3F
RN9
SRN4K7J-10-GP
FAN1
ACES-CON3-GP-U1
G87
G88
TP67
TPAD60
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
THERMAL G792
Size
A3
Document Number
S13
Rev
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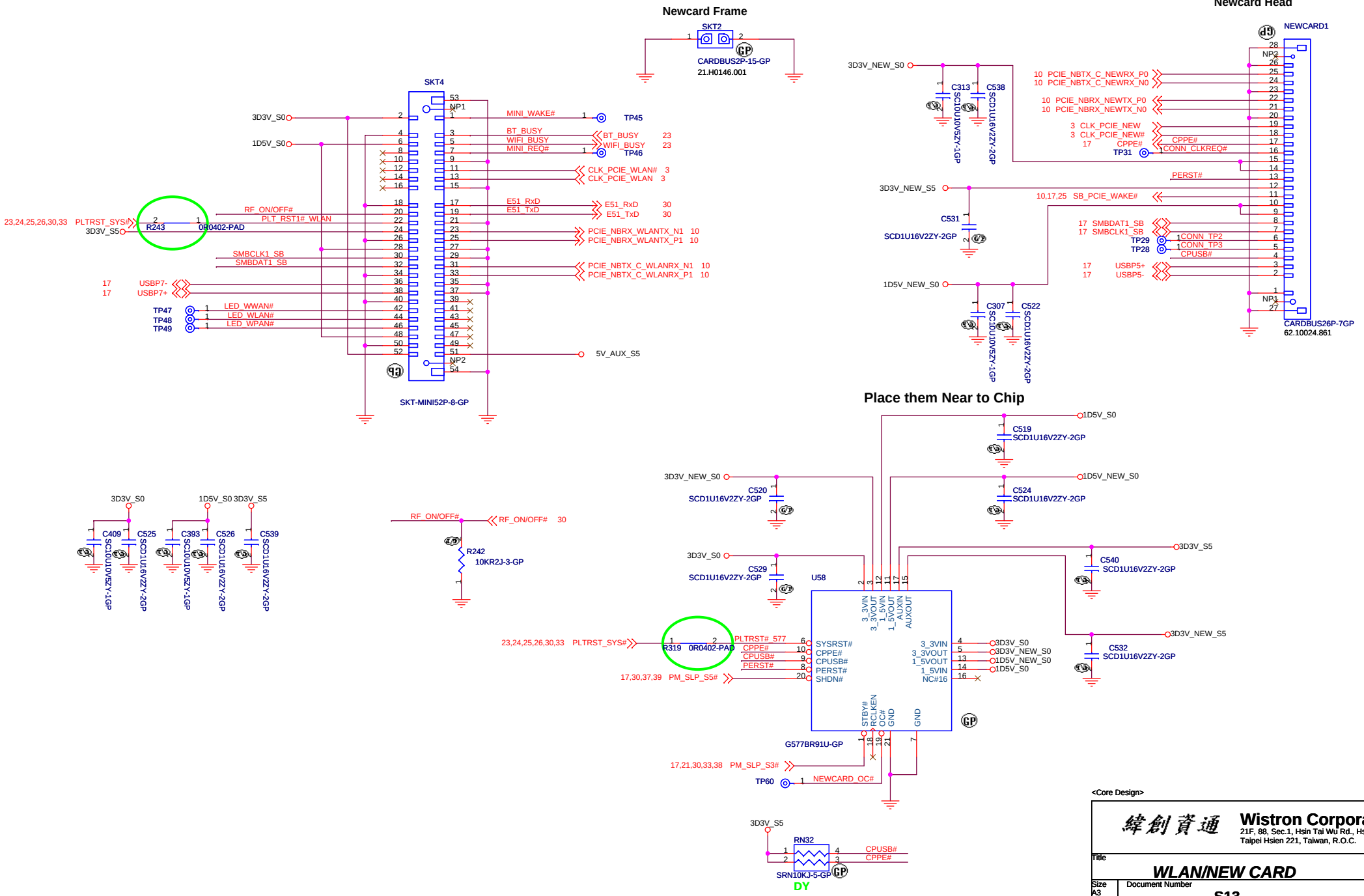
NEWCARD Connector

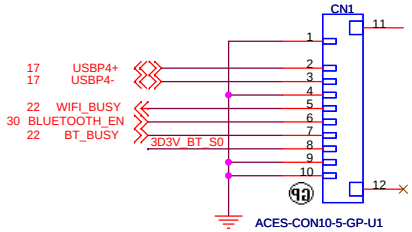
WLAN Connector

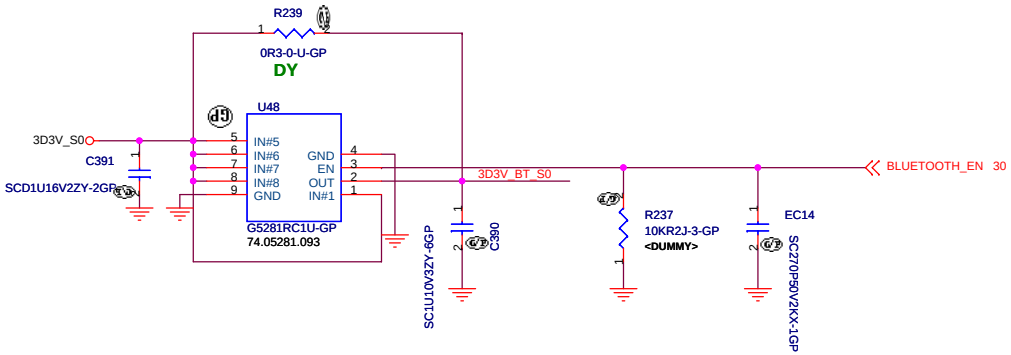


<Core Design>

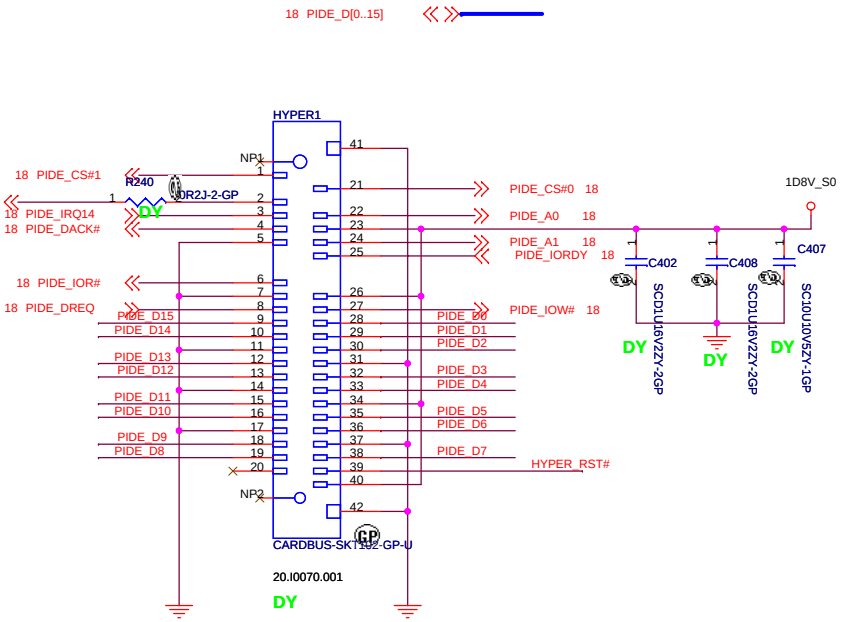
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***WLAN/NEW CARD***	
Size A3	Document Number **S13**	Rev **SC**
Date: Friday, May 16, 2008	Sheet 22 of 44	

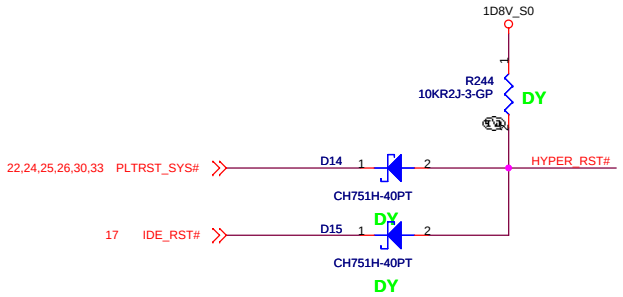
Bluetooth





HYPER FLASH





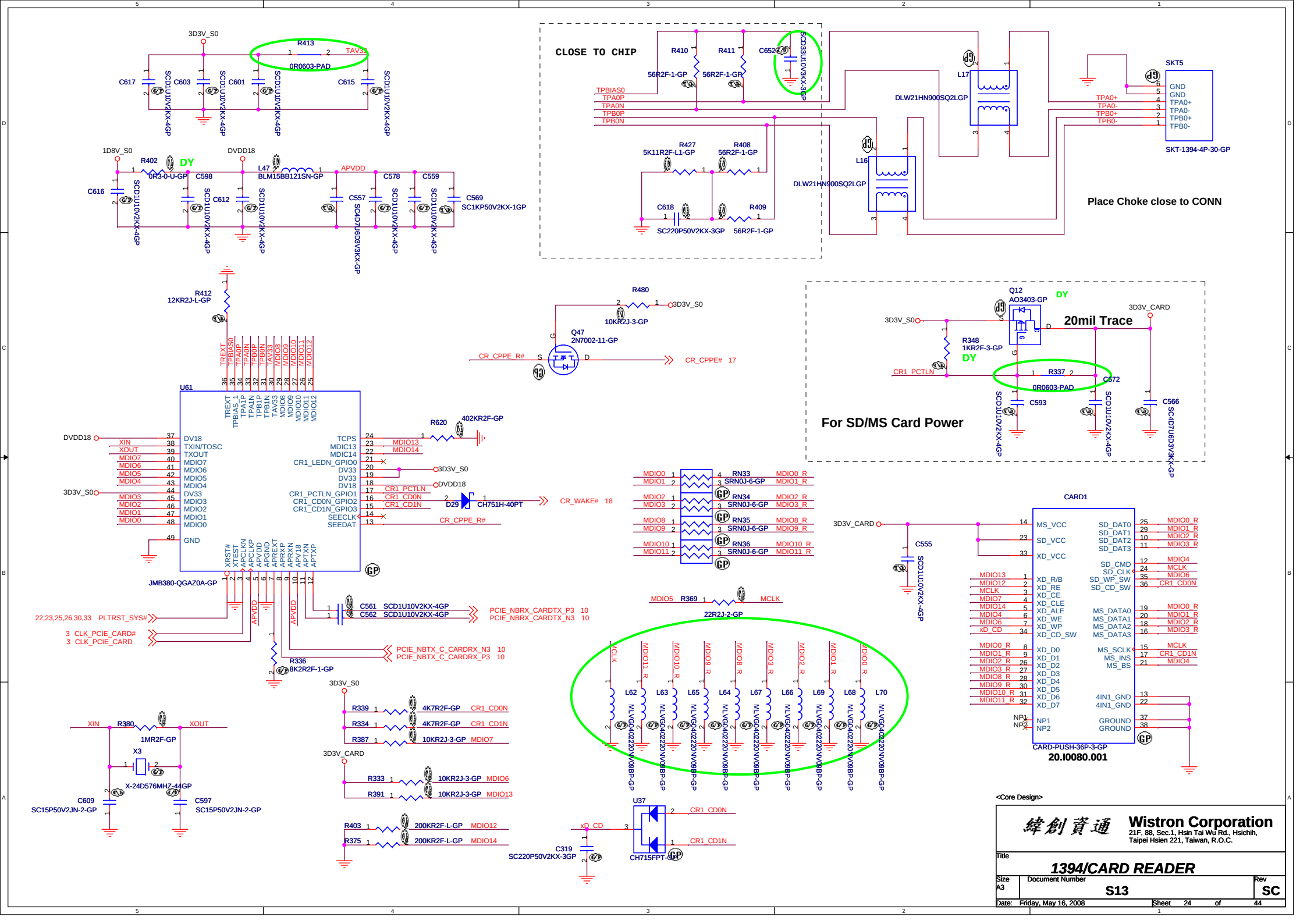
<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HYPER FLASH/BT***

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 23 of 44


CLOSE TO CHIP
Place Choke close to CONN
For SD/MS Card Power
20mil Trace
U61
JMB380-QGAZ0A-GP
CARD1
CARD-PUSH-36P-3-GP
20.I0080.001
U37
CH715FPT-GP
X3
X-24D576MHZ-44GP
SKT5
SKT-1394-4P-30-GP
DLW21HN900SQ2LGP
CH751H-40PT
SC1KP50V2KX-1GP
SC4D7U6D3V3KX-GP
SCD1U10V2KX-4GP
SCD33U10V3KX-3GP
SC220P50V2KX-3GP
SC15P50V2JN-2-GP
MLVG0402220NV08BP-GP
AO3403-GP
2N7002-11-GP
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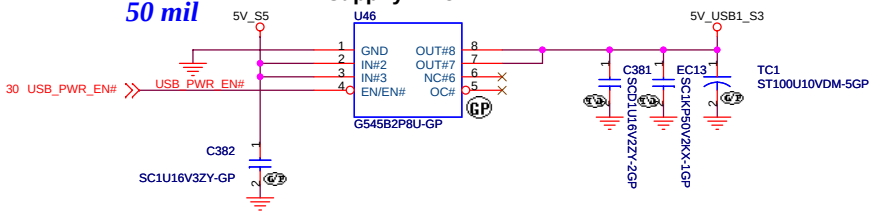
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
1394/CARD READER
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
Sheet 24 of 44

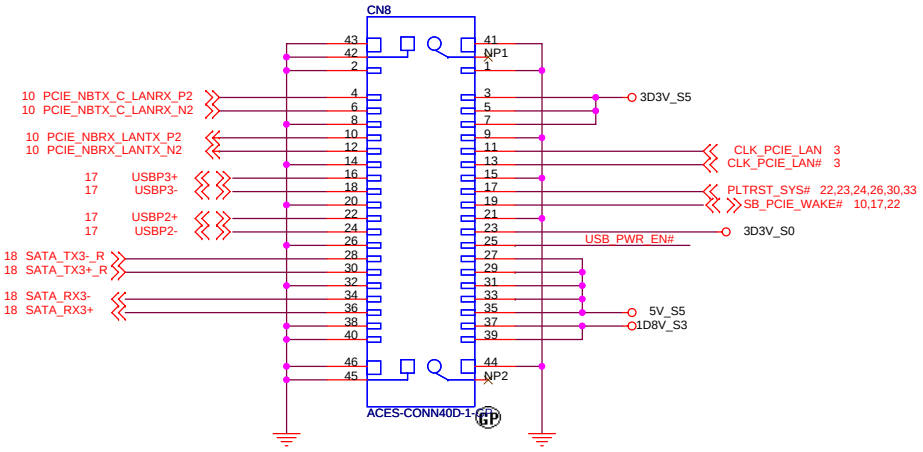
USB PORT

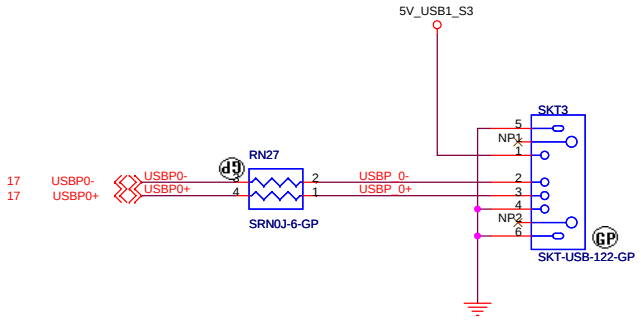
400uS rise time
Supply 1.5~1.1A

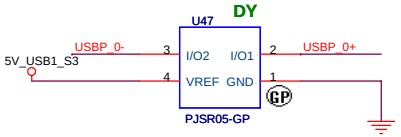
50 mil

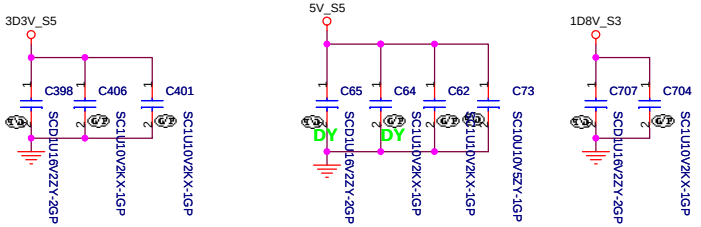
50 mil











<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB & DAUGHTER CONN

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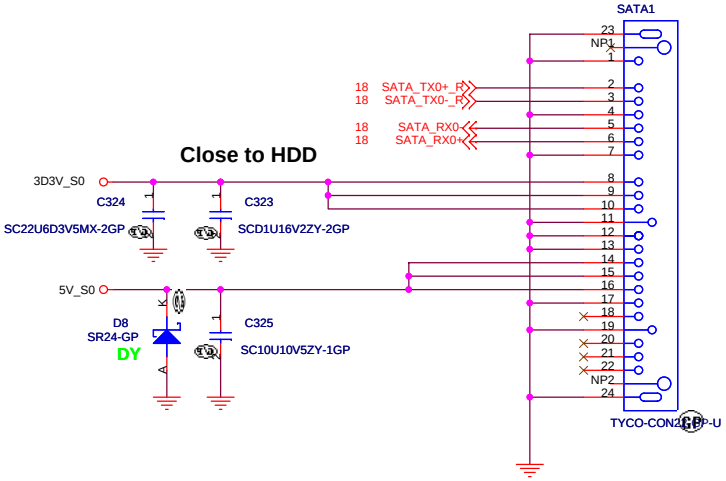
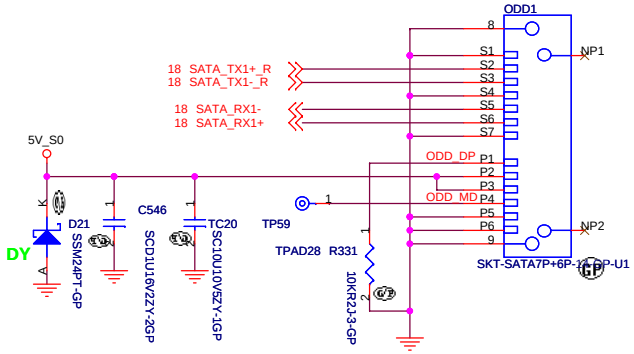
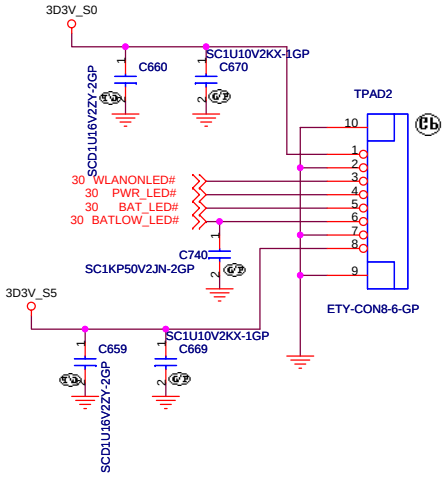
SATA HDD Connector



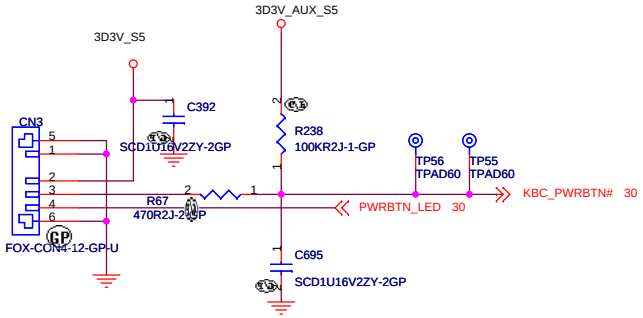
SATA ODD Connector



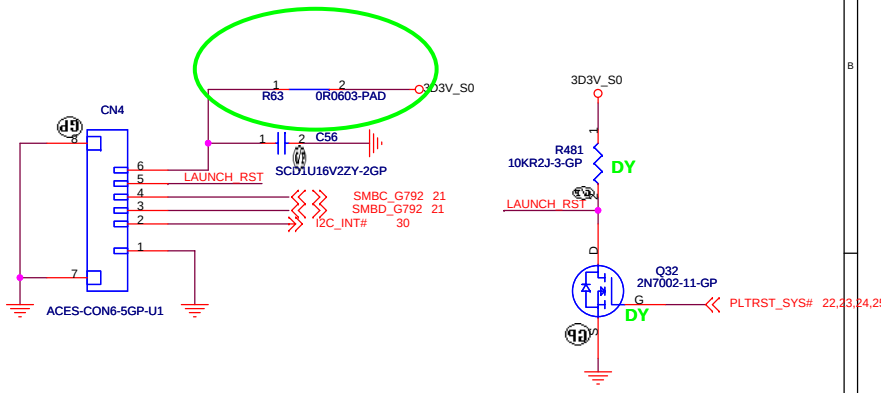
LED BD CONN



PWRBTN BD CONN



LAUNCH BD CONN



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***HDD/CDROM/LED/LAUNCH***

Size	Document Number	Rev
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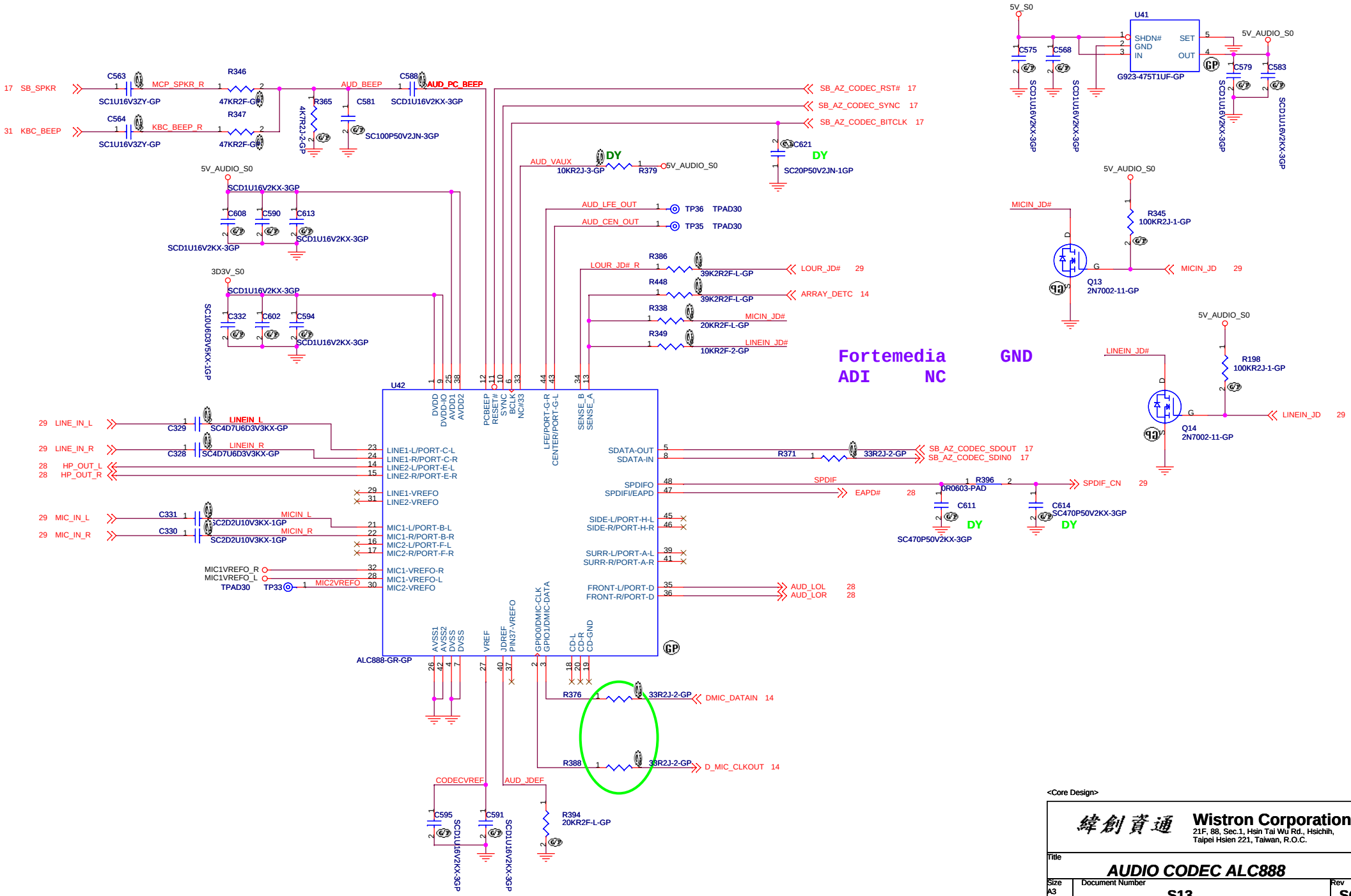
Fortemedia
ADI
GND
NC
U42
ALC888-GR-GP
U41
G923-475T1UF-GP
Q13
2N7002-11-GP
Q14
2N7002-11-GP
5V_S0
5V_AUDIO_S0
3D3V_S0
SB_SPKR
KBC_BEEP
MCP_SPKR_R
KBC_BEEP_R
AUD_BEEP
AUD_PC_BEEP
SB_AZ_CODEC_RST# 17
SB_AZ_CODEC_SYNC 17
SB_AZ_CODEC_BITCLK 17
AUD_VAUX
AUD_LFE_OUT
AUD_CEN_OUT
LOUR_JD# R
MICIN_JD#
LINEIN_JD#
LINE_IN_L
LINE_IN_R
HP_OUT_L
HP_OUT_R
MIC_IN_L
MIC_IN_R
MIC1VREFO_R
MIC1VREFO_L
MIC2VREFO
SDATA-OUT
SDATA-IN
SPDIFO
SPDIFI/EAPD
SPDIF
EAPD# 28
SPDIF_CN 29
SB_AZ_CODEC_SDOUT 17
SB_AZ_CODEC_SDIN0 17
AUD_LOL 28
AUD_LOR 28
DMIC_DATAIN 14
D_MIC_CLKOUT 14
CODECVREF
AUD_JDEF
LOUR_JD# 29
ARRAY_DETC 14
MICIN_JD 29
LINEIN_JD 29
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
AUDIO CODEC ALC888
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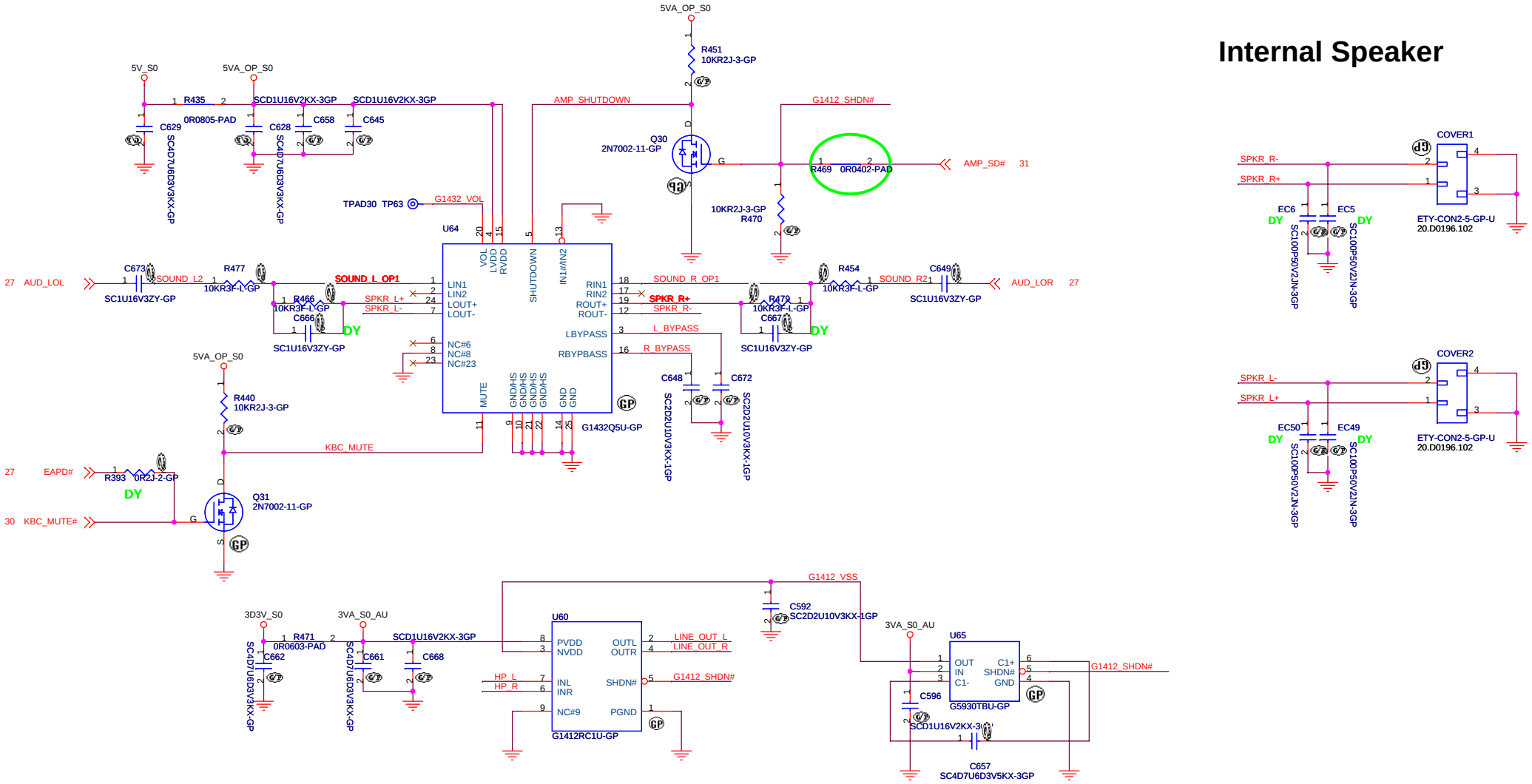
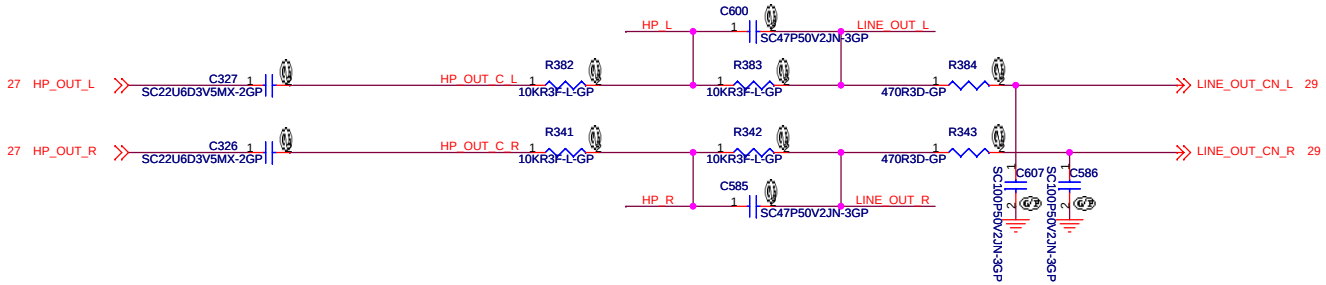
Internal Speaker



LINE Out



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***AUDIO AMP/Speaker***

Size	Document Number	Rev
A3	S13	SC

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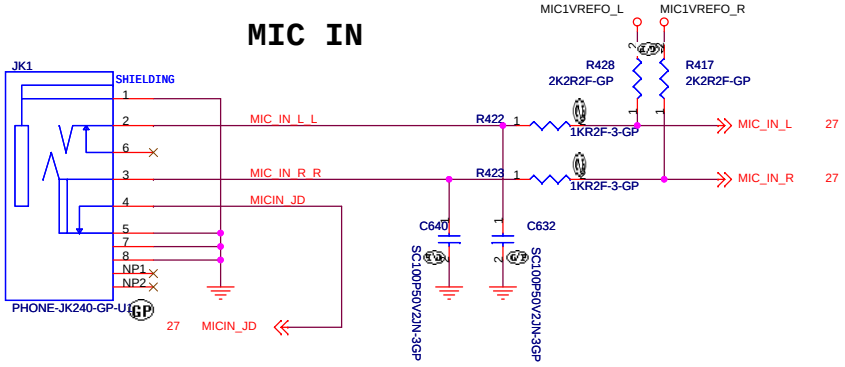
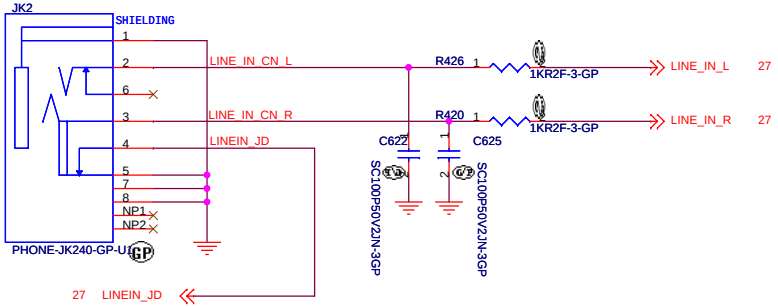
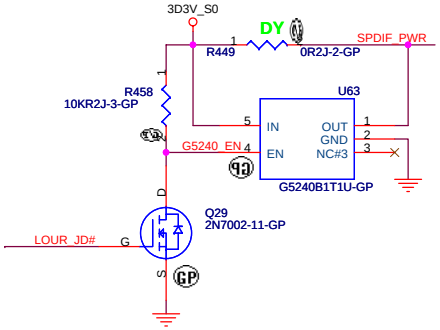
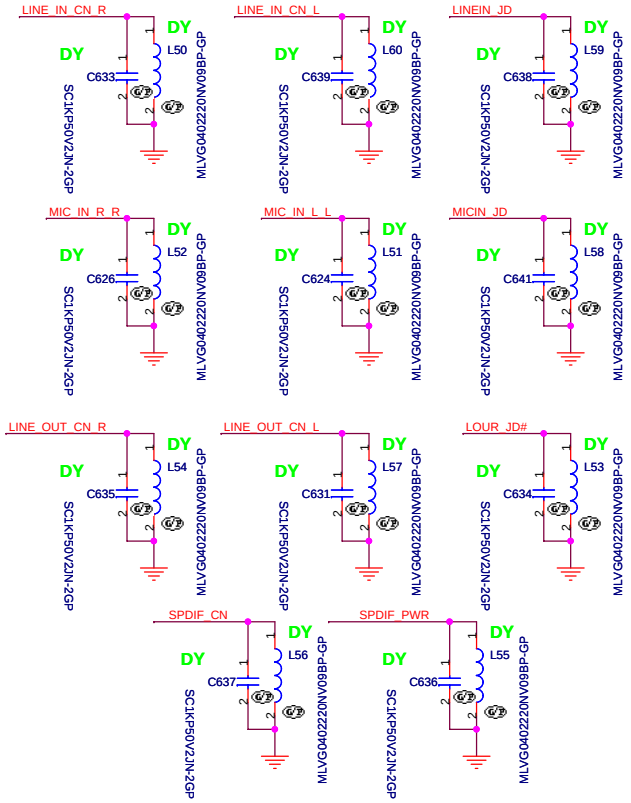
MIC IN



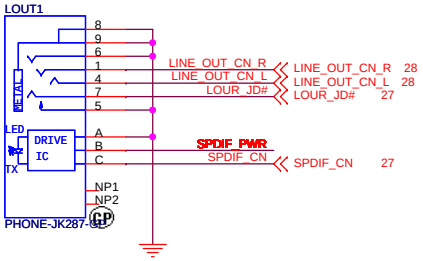
LINE IN







SPDIF / LINE OUT



<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CONN/SUBWOOFER**

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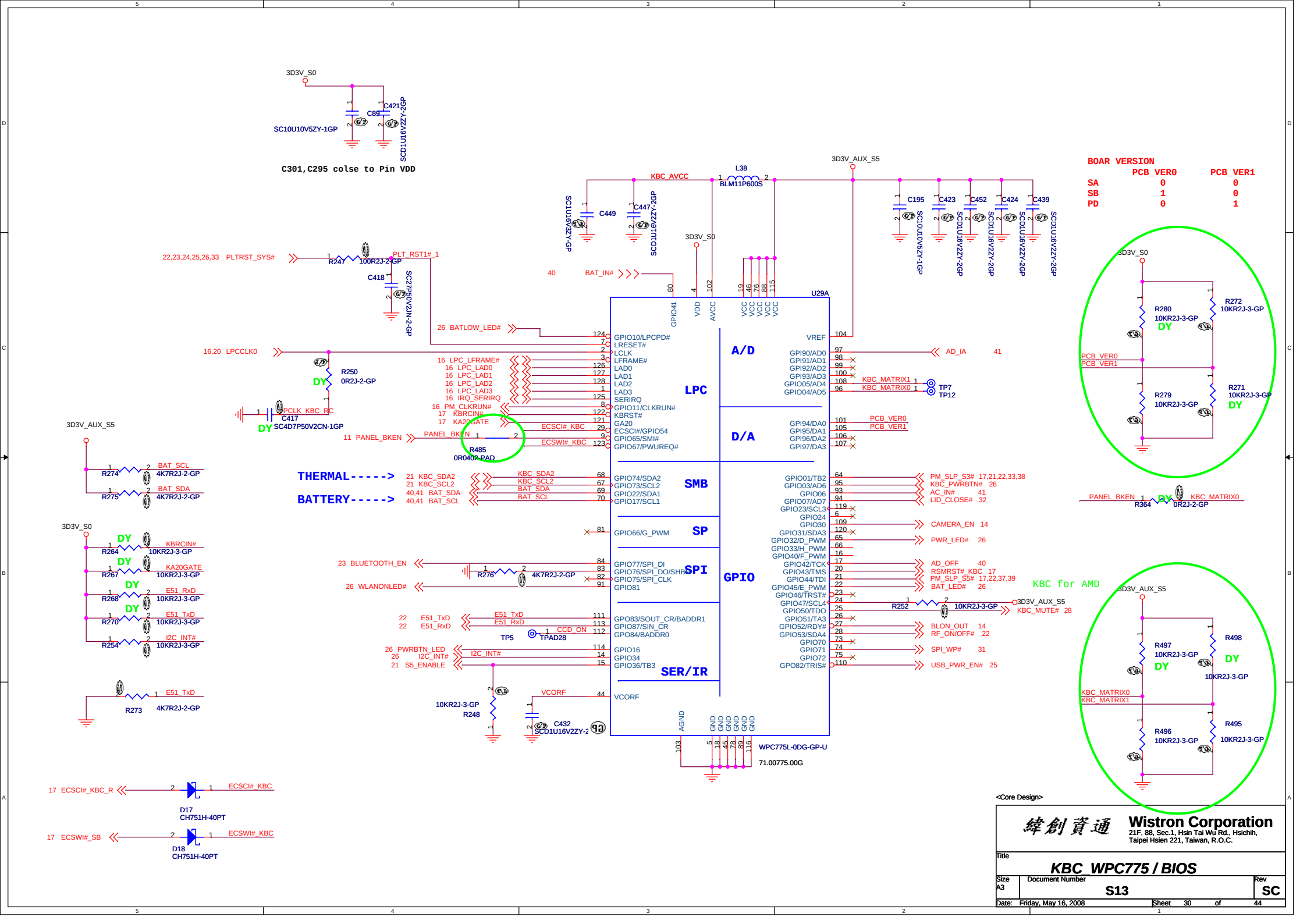
3D3V_S0
C421
C89
SC10U10V5ZY-1GP
SCD1U16V2ZY-2GP
C301,C295 colse to Pin VDD
3D3V_AUX_S5
KBC_AVCC
L38
BLM11P600S
C449
C447
C195
C423
C452
C424
C439
SCD1U16V2ZY-2GP
SCD1U10V5ZY-1GP
BOAR VERSION
PCB_VER0
PCB_VER1
SA 0 0
SB 1 0
PD 0 1
22,23,24,25,26,33 PLTRST_SYS#
R247 100R2J-2-GP
PLT_RST1#_1
C418
SC27P50V2JN-2-GP
40 BAT_IN#
U29A
GPIO41
VDD
AVCC
VCC
26 BATLOW_LED#
16,20 LPCCLK0
R250 0R2J-2-GP
DY
C417 SC4D7P50V2CN-1GP
PCLK_KBC_RC
11 PANEL_BKEN
PANEL_BKEN
R485 0R0402-PAD
ECSCI# KBC
ECSWI# KBC
16 LPC_LFRAME#
16 LPC_LAD0
16 LPC_LAD1
16 LPC_LAD2
16 LPC_LAD3
16 IRQ_SERIRQ
16 PM_CLKRUN#
17 KBRCIN#
17 KA20GATE
GPIO10/LPCPD#
LRESET#
LCLK
LFRAME#
LAD0
LAD1
LAD2
LAD3
SERIRQ
GPIO11/CLKRUN#
KBRST#
GA20
ECSCI#/GPIO54
GPIO65/SMI#
GPIO67/PWUREQ#
LPC
A/D
D/A
SMB
SP
SPI
GPIO
SER/IR
VREF
GPI90/AD0
GPI91/AD1
GPI92/AD2
GPI93/AD3
GPIO05/AD4
GPIO04/AD5
AD_IA 41
KBC_MATRIX1
KBC_MATRIX0
TP7
TP12
GPI94/DA0
GPI95/DA1
GPI96/DA2
GPI97/DA3
PCB_VER0
PCB_VER1
THERMAL-----> 21 KBC_SDA2 21 KBC_SCL2
BATTERY-----> 40,41 BAT_SDA 40,41 BAT_SCL
KBC_SDA2
KBC_SCL2
BAT_SDA
BAT_SCL
GPIO74/SDA2
GPIO73/SCL2
GPIO22/SDA1
GPIO17/SCL1
GPIO01/TB2 PM_SLP_S3# 17,21,22,33,38
GPIO03/AD6 KBC_PWRBTN# 26
GPIO06 AC_IN# 41
GPIO07/AD7 LID_CLOSE# 32
GPIO23/SCL3
GPIO24
GPIO30 CAMERA_EN 14
GPIO31/SDA3
GPIO32/D_PWM PWR_LED# 26
GPIO33/H_PWM
GPIO40/F_PWM
GPIO66/G_PWM
23 BLUETOOTH_EN
R276 4K7R2J-2-GP
26 WLANONLED#
GPIO77/SPI_DI
GPIO76/SPI_DO/SHBM
GPIO75/SPI_CLK
GPIO81
GPIO42/TCK AD_OFF 40
GPIO43/TMS RSMRST# KBC 17
GPIO44/TDI PM_SLP_S5# 17,22,37,39
GPIO45/E_PWM BAT_LED# 26
GPIO46/TRST#
GPIO47/SCL4
GPIO50/TDO
GPIO51/TA3
GPIO52/RDY# BLON_OUT 14
GPIO53/SDA4 RF_ON/OFF# 22
GPIO70
GPIO71 SPI_WP# 31
GPIO72
GPO82/TRIS# USB_PWR_EN# 25
KBC for AMD
R252 10KR2J-3-GP
3D3V_AUX_S5
KBC_MUTE# 28
22 E51_TxD
22 E51_RxD
E51_TxD
E51_RxD
TP5 CCD_ON
TPAD28
GPO83/SOUT_CR/BADDR1
GPO87/SIN_CR
GPO84/BADDR0
26 PWRBTN_LED
26 I2C_INT#
21 S5_ENABLE
I2C_INT#
GPIO16
GPIO34
GPIO36/TB3
R248 10KR2J-3-GP
VCORF
C432 SCD1U16V2ZY-2
VCORF
AGND
GND
WPC775L-0DG-GP-U
71.00775.00G
3D3V_AUX_S5
BAT_SCL R274 4K7R2J-2-GP
BAT_SDA R275 4K7R2J-2-GP
3D3V_S0
KBRCIN# R264 10KR2J-3-GP
KA20GATE R267 10KR2J-3-GP
E51_RxD R268 10KR2J-3-GP
E51_TxD R270 10KR2J-3-GP
I2C_INT# R254 10KR2J-3-GP
E51_TxD R273 4K7R2J-2-GP
17 ECSCI#_KBC_R
ECSCI# KBC
D17 CH751H-40PT
17 ECSWI#_SB
ECSWI# KBC
D18 CH751H-40PT
R280 10KR2J-3-GP
R272 10KR2J-3-GP
R279 10KR2J-3-GP
R271 10KR2J-3-GP
PANEL_BKEN
R364 0R2J-2-GP
KBC_MATRIX0
R497 10KR2J-3-GP
R498 10KR2J-3-GP
R496 10KR2J-3-GP
R495 10KR2J-3-GP
KBC_MATRIX1
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緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
KBC_WPC775 / BIOS
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
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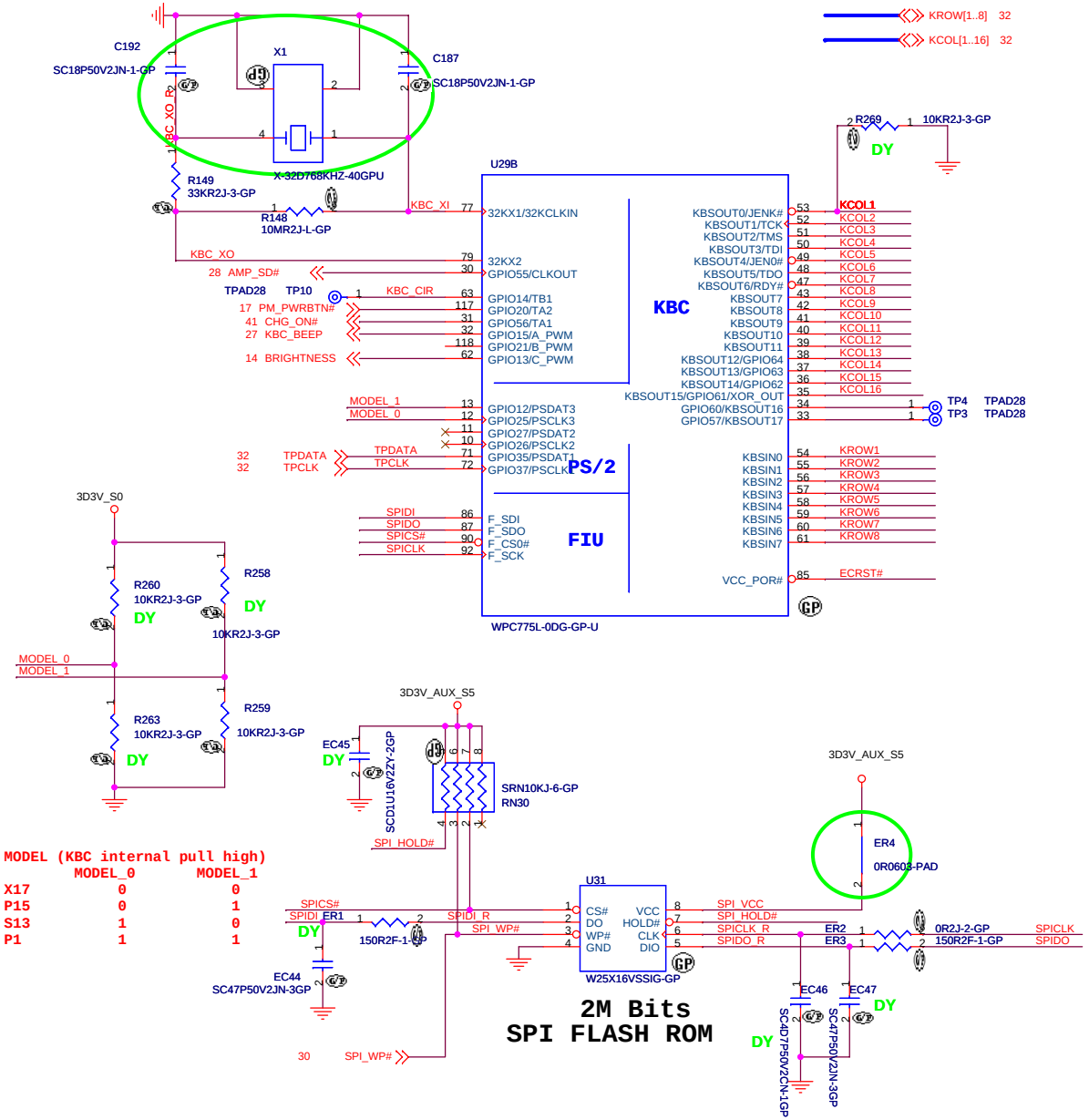


MODEL (KBC internal pull high)

	MODEL_0	MODEL_1
X17	0	0
P15	0	1
S13	1	0
P1	1	1

2M Bits SPI FLASH ROM

<Core Design>

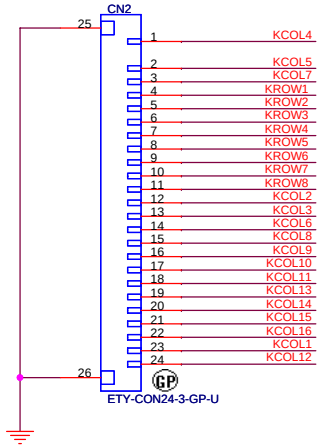
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

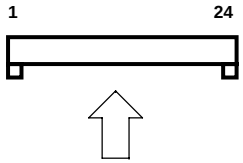
Title: KBC_WPC775 / BIOS(2/2)

Size	Document Number	Rev
A3	S13	SC

Date: Friday, May 16, 2008 Sheet 31 of 44

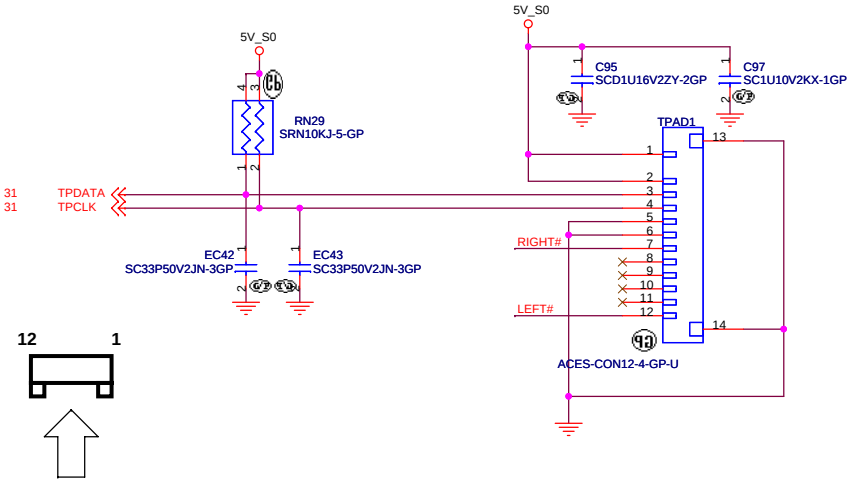
Internal KeyBoard Connector



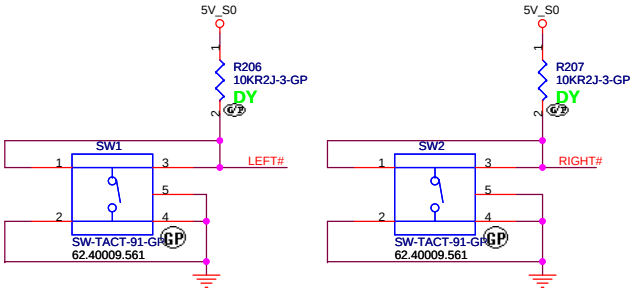


GOLDEN FINGER FOR DEBUG BOARD

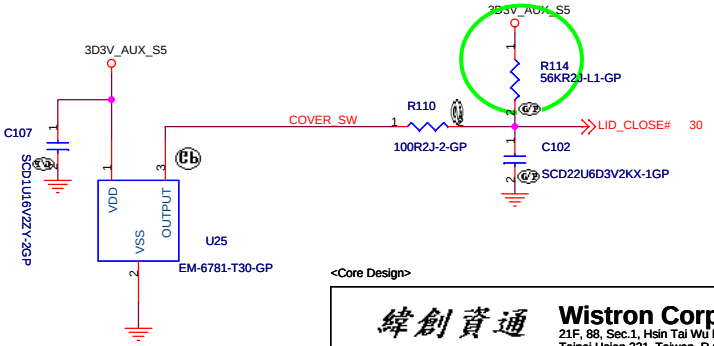
TouchPad Connector



TOUCHPAD BUTTON SWITCH



COVER SWITCH



<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: KEYBOARD/TPAD/DEBUG/LID

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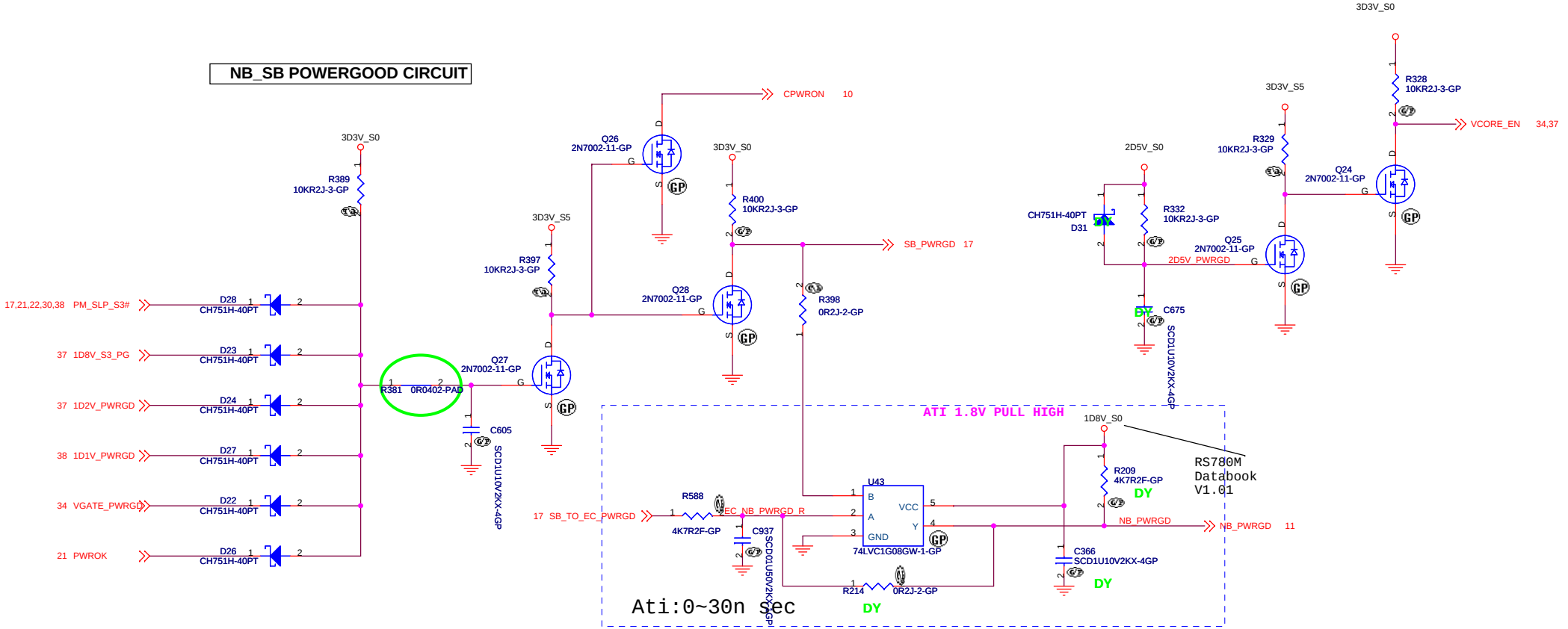
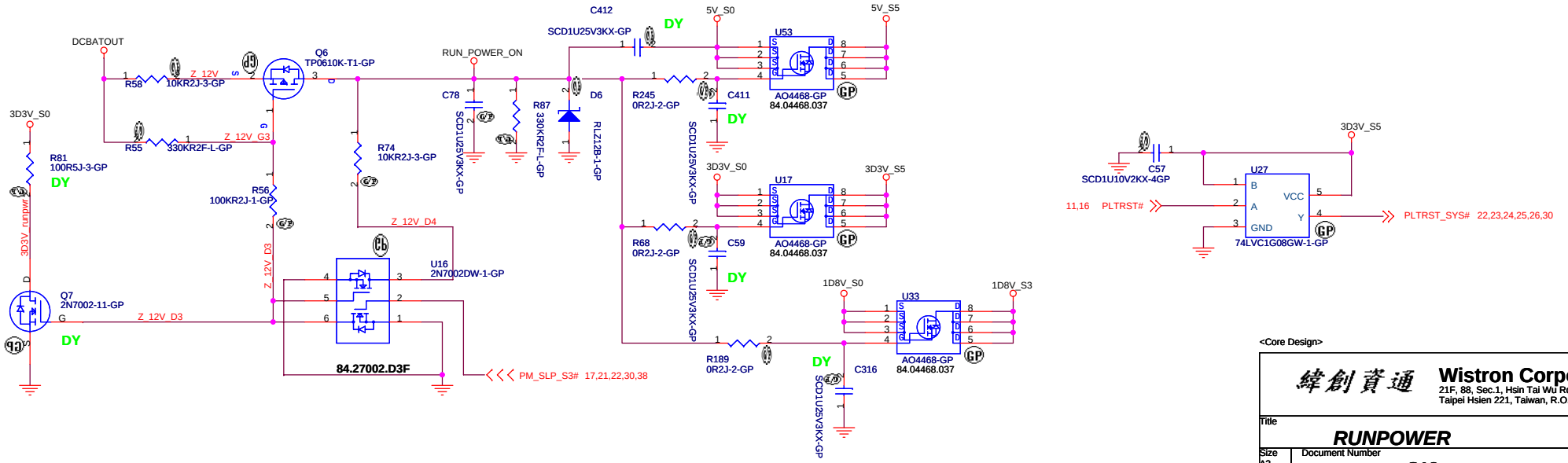
NB_SB POWERGOOD CIRCUIT



Run Power



<Core Design>

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: ***RUNPOWER***		
Size: A3	Document Number: **S13**	Rev: **SC**
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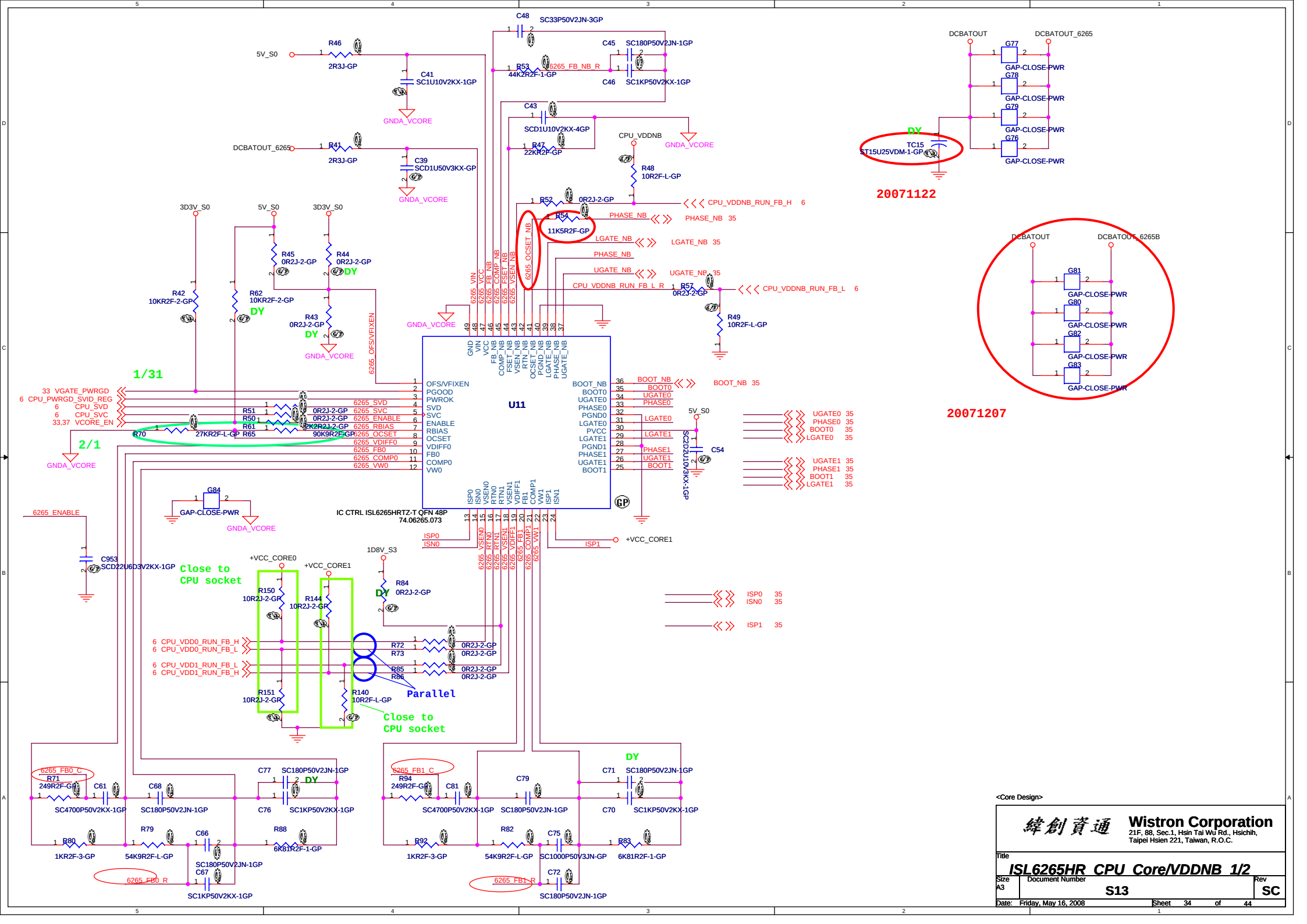
U11
IC CTRL ISL6265HRTZ-T QFN 48P
74.06265.073
1/31
2/1
Close to CPU socket
Parallel
20071122
20071207
DY
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL6265HR CPU Core/VDDNB 1/2
Size A3
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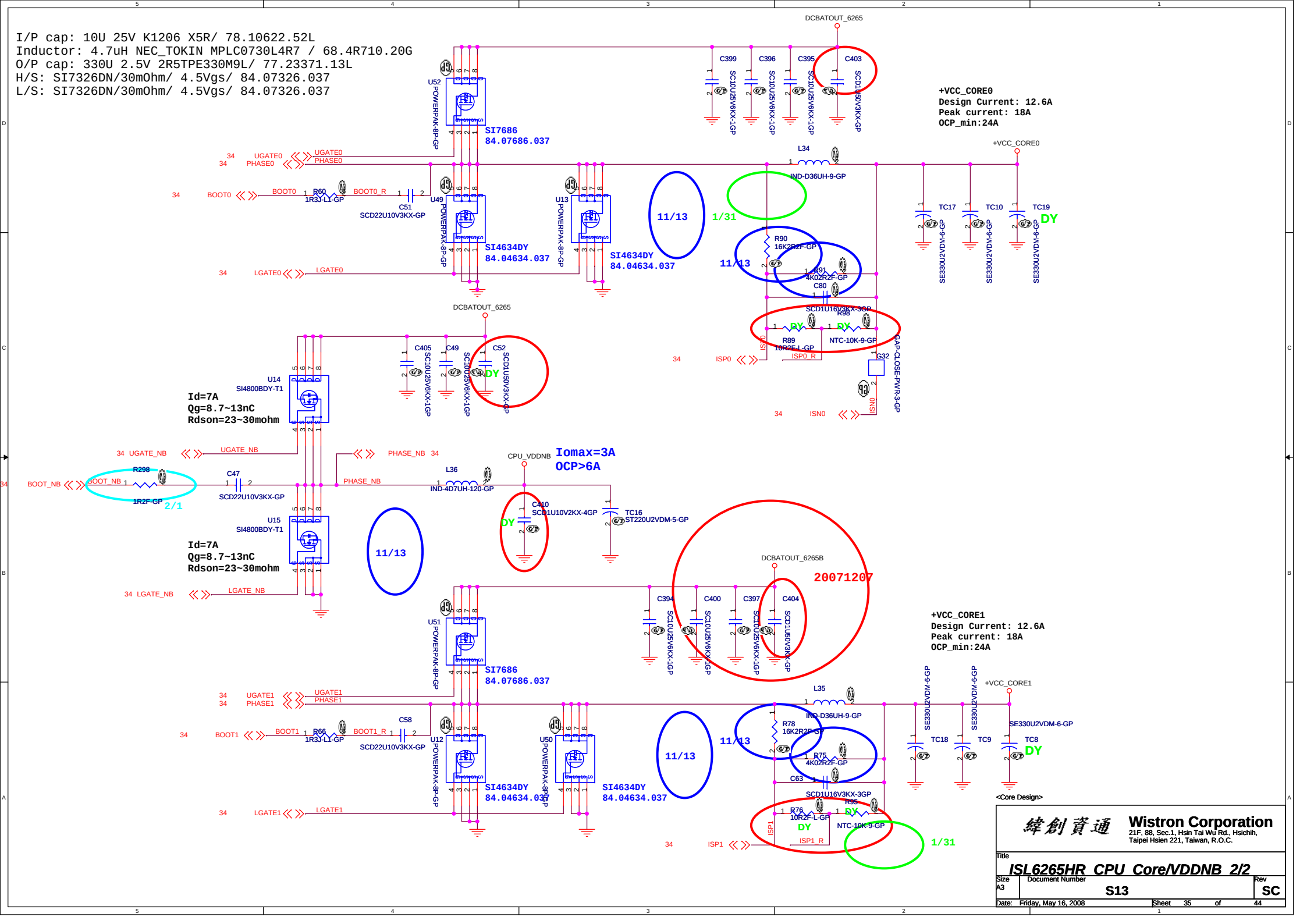
I/P cap: 10U 25V K1206 X5R/ 78.10622.52L
Inductor: 4.7uH NEC_TOKIN MPLC0730L4R7 / 68.4R710.20G
O/P cap: 330U 2.5V 2R5TPE330M9L/ 77.23371.13L
H/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037
L/S: SI7326DN/30mOhm/ 4.5Vgs/ 84.07326.037



緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ISL6265HR CPU Core/VDDNB 2/2
Size: A3 | Document Number: S13 | Rev: SC
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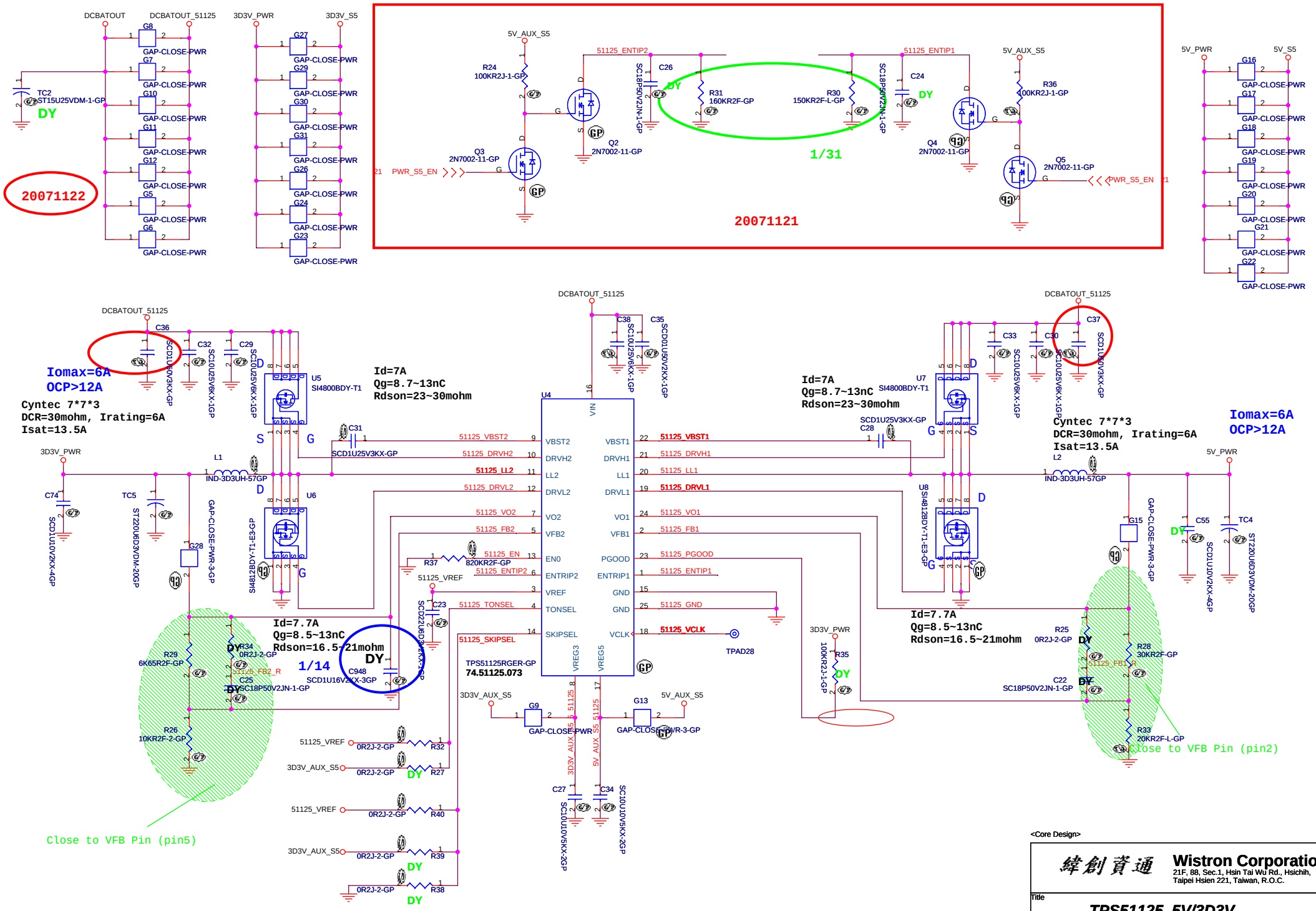
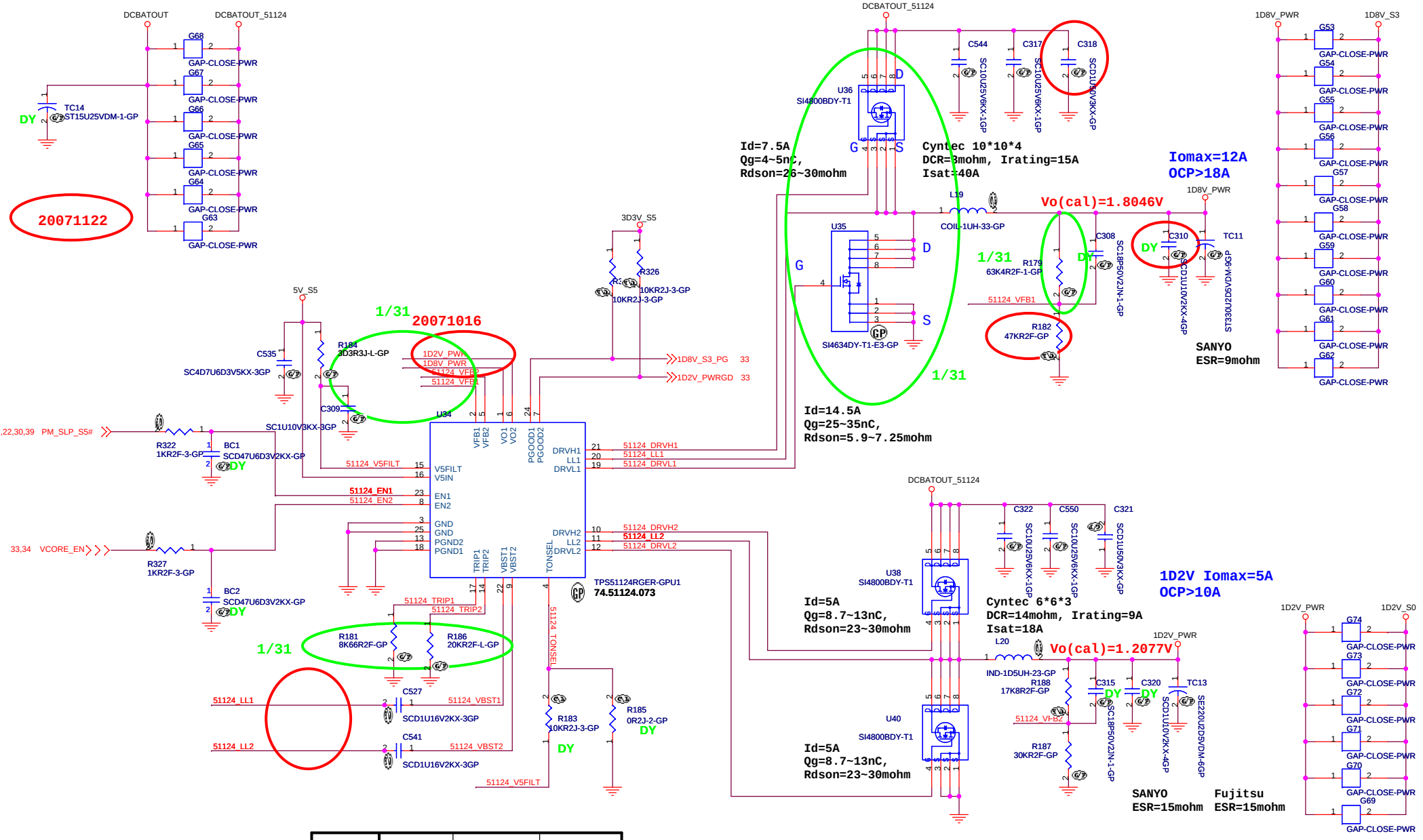

DCBATOUT
DCBATOUT_51125
3D3V_PWR
3D3V_S5
GAP-CLOSE-PWR
TC2
ST15U25VDM-1-GP
DY
20071122
5V_AUX_S5
R24
100KR2J-1-GP
Q3
2N7002-11-GP
PWR_S5_EN
51125_ENTIP2
C26
SC18P50V2JN-1-GP
R31
160KR2F-GP
Q2
2N7002-11-GP
1/31
R30
150KR2F-L-GP
51125_ENTIP1
C24
Q4
2N7002-11-GP
R36
100KR2J-1-GP
Q5
2N7002-11-GP
20071121
5V_PWR
5V_S5
Iomax=6A
OCP>12A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
U5
SI4800BDY-T1
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
U4
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
VCLK
VREG3
VREG5
TPS51125RGER-GP
74.51125.073
TPAD28
U7
SI4800BDY-T1
U8
SI4812BDY-T1-E3-GP
L1
L2
IND-3D3UH-57GP
U6
SI4812BDY-T1-E3-GP
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
1/14
Close to VFB Pin (pin5)
Close to VFB Pin (pin2)
<Core Design>
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51125_5V/3D3V
Size
A3
Document Number
S13
Rev
SC
Date: Friday, May 16, 2008
Sheet 36 of 44



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51124_1D8V/1D2V

Size	Document Number	Rev
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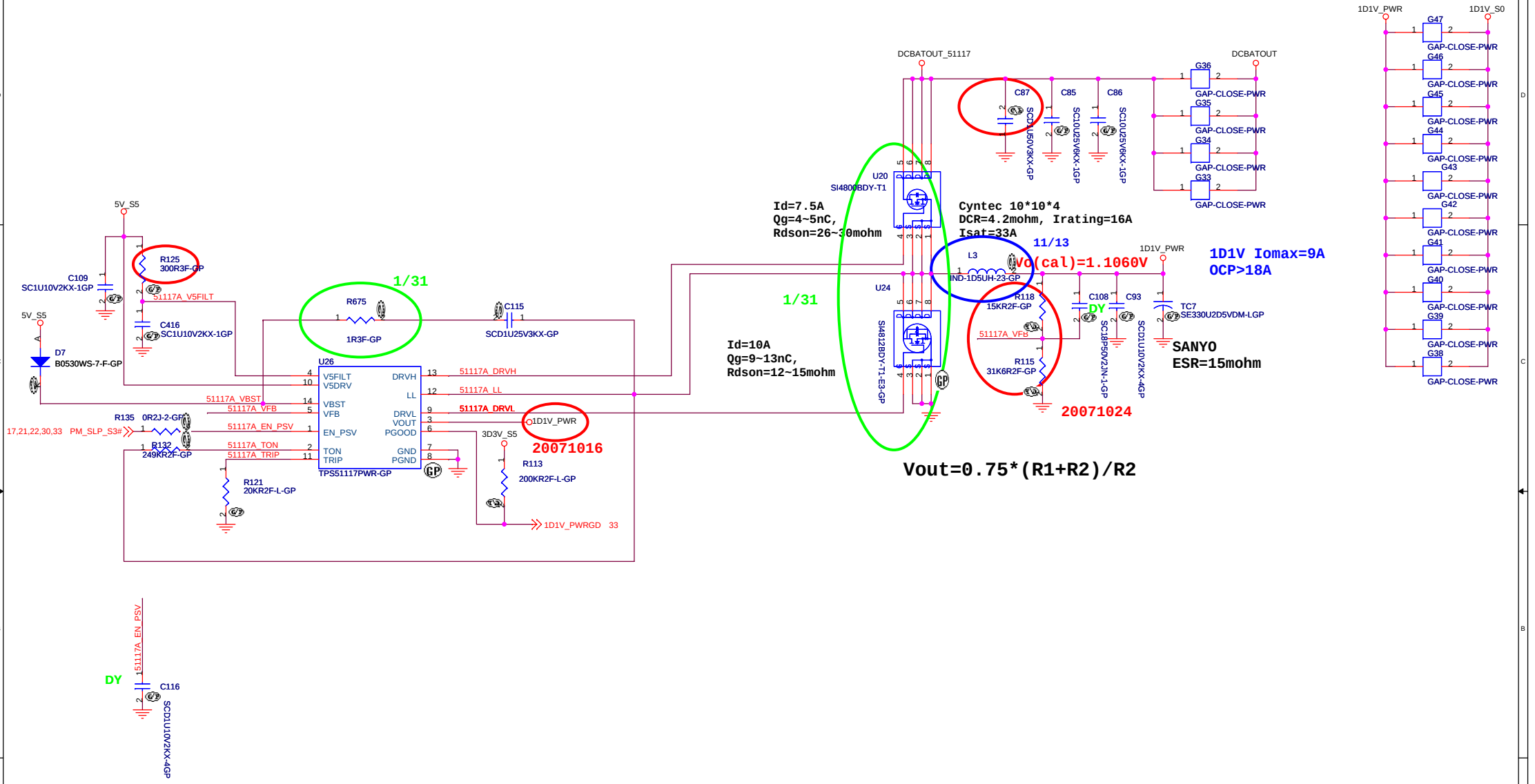
Date: Friday, May 16, 2008 Sheet 37 of 44



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緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPS51117_1D1V***

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Date: Friday, May 16, 2008 Sheet 38 of 44

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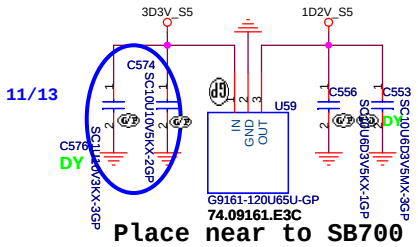

Place near to SB700

G957
1D5V_S0
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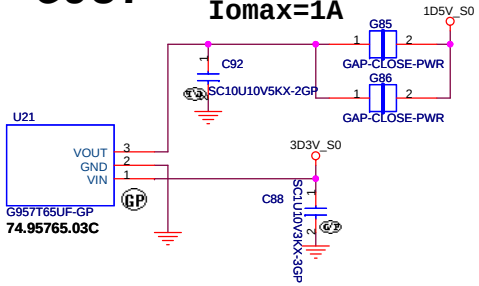

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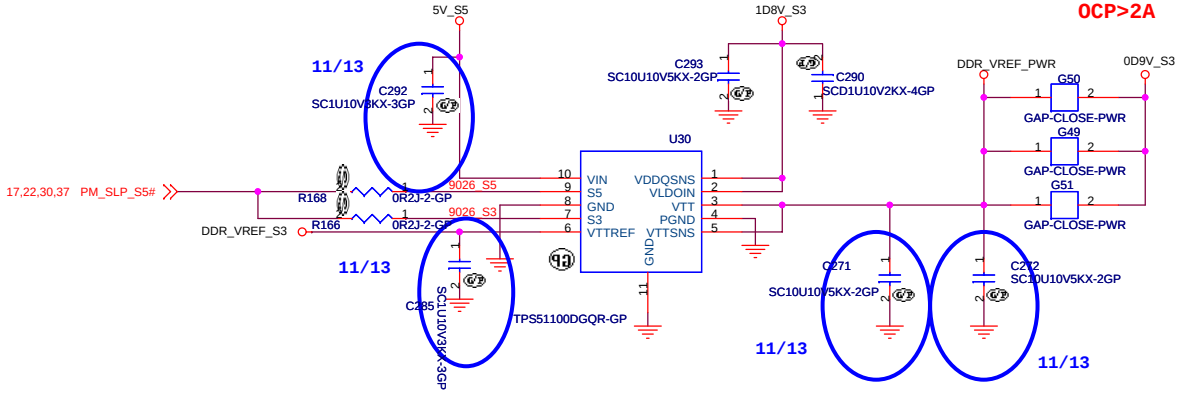
OCP>2A



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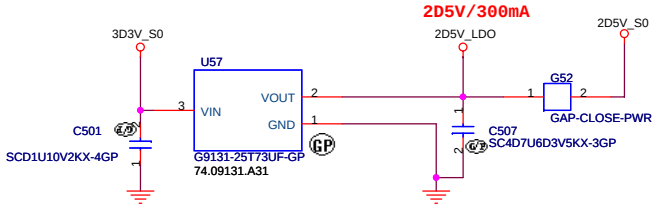

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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: 0D9V&2D5V&1D25V&1D5V		
Size: A3	Document Number: S13	Rev: SC
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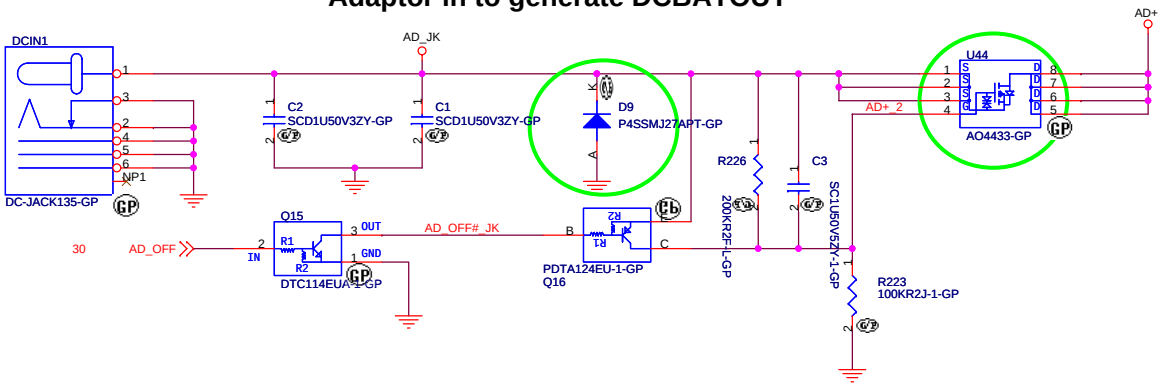
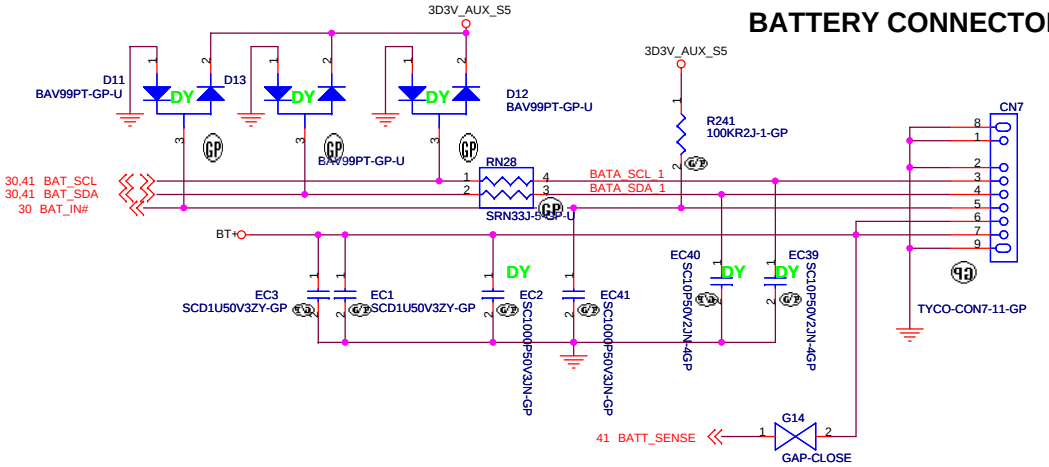
Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



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Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AD_IN/ BTY SWITCH/GPURUN**

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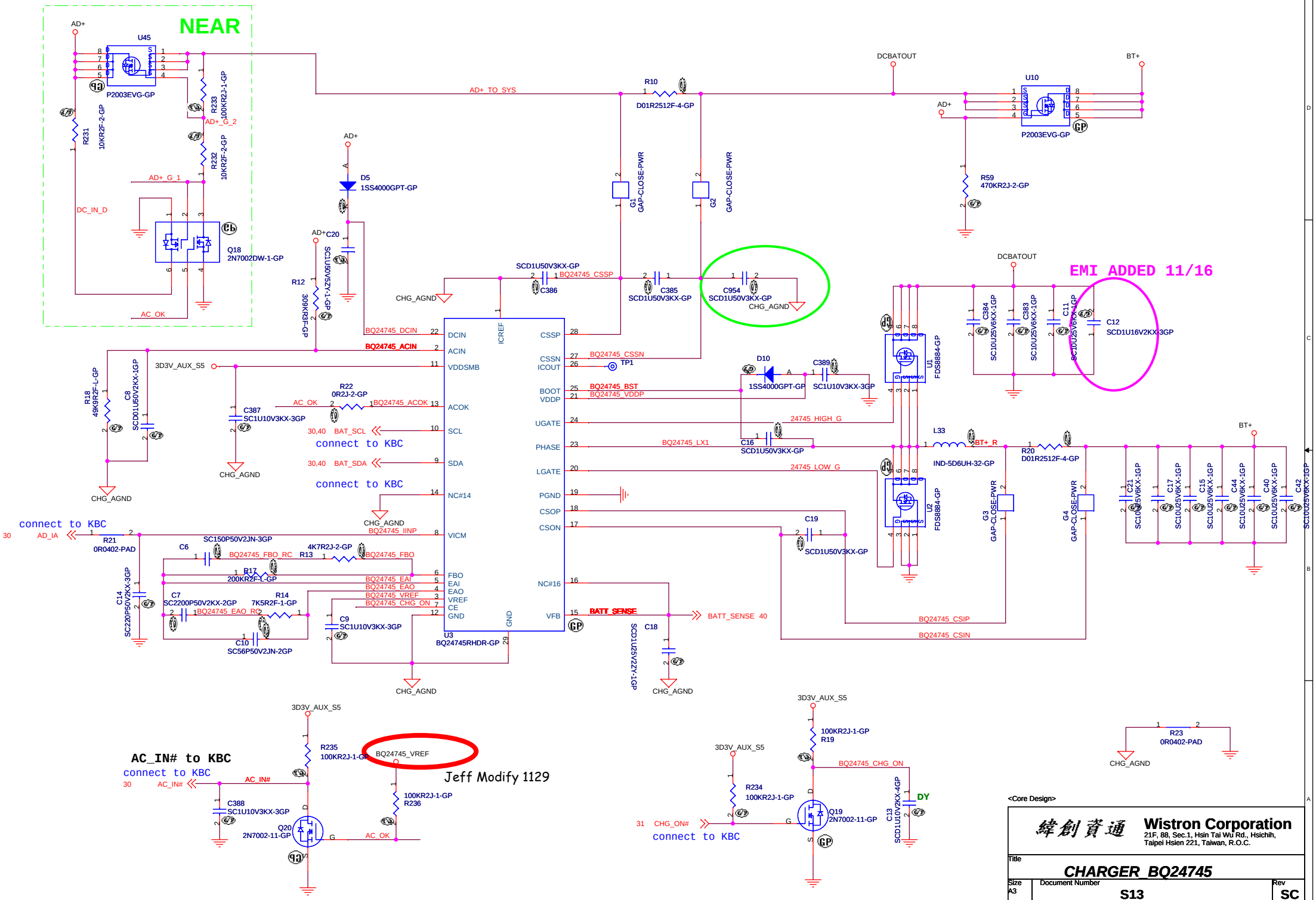
Date: Friday, May 16, 2008 Sheet 40 of 44


NEAR
U45
P2003EVG-GP
R231 10KR2F-2-GP
R233 100KR2J-1-GP
R232 10KR2F-2-GP
AD+_G_2
AD+_G_1
DC_IN_D
Q18 2N7002DW-1-GP
AC_OK
AD+
D5 1SS4000GPT-GP
C20 SCD1U50V5ZY-1-GP
R12 309KR2F-GP
CHG_AGND
AD+ TO_SYS
R10 D01R2512F-4-GP
G1 GAP-CLOSE-PWR
G2 GAP-CLOSE-PWR
DCBATOUT
BT+
U10
P2003EVG-GP
R59 470KR2J-2-GP
SCD1U50V3KX-GP
C386
BQ24745_CSSP
C385 SCD1U50V3KX-GP
C954 SCD1U50V3KX-GP
EMI ADDED 11/16
C384 SC10U25V6KX-1GP
C383 SC10U25V6KX-1GP
C11 SC10U25V6KX-1GP
C12 SCD1U16V2KX-3GP
U1 FDS8884-GP
U2 FDS8884-GP
BQ24745_DCIN
BQ24745_ACIN
3D3V_AUX_S5
R18 49K9R2F-L-GP
C8 SCD01U50V2KX-1GP
R22 0R2J-2-GP
AC_OK
BQ24745_ACOK
C387 SC1U10V3KX-3GP
30,40 BAT_SCL
connect to KBC
30,40 BAT_SDA
connect to KBC
CHG_AGND
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
VICM
FBO
EAI
EAO
VREF
CE
GND
ICREF
CSSP
CSSN
ICOUT
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
U3 BQ24745RHDR-GP
BQ24745_CSSN
TP1
BQ24745_BST
BQ24745_VDDP
D10 1SS4000GPT-GP
C389 SC1U10V3KX-3GP
24745_HIGH_G
BQ24745_LX1
C16 SCD1U50V3KX-GP
L33 IND-5D6UH-32-GP
BT+_R
R20 D01R2512F-4-GP
24745_LOW_G
C19 SCD1U50V3KX-GP
G3 GAP-CLOSE-PWR
G4 GAP-CLOSE-PWR
C21 SC10U25V6KX-1GP
C17 SC10U25V6KX-1GP
C15 SC10U25V6KX-1GP
C44 SC10U25V6KX-1GP
C40 SC10U25V6KX-1GP
C42 SC10U25V6KX-1GP
connect to KBC
30 AD_IA
R21 0R0402-PAD
SC150P50V2JN-3GP
C6
BQ24745_FBO_RC
R13 4K7R2J-2-GP
BQ24745_FBO
R17 200KR2F-1-GP
C14 SC220P50V2KX-3GP
C7 SC2200P50V2KX-2GP
BQ24745_EAO_RC
R14 7K5R2F-1-GP
C10 SC56P50V2JN-2GP
C9 SC1U10V3KX-3GP
BQ24745_EAI
BQ24745_EAO
BQ24745_VREF
BQ24745_CHG_ON
BQ24745_IINP
BATT_SENSE
SCD1U25V2ZY-1GP
C18
BATT_SENSE 40
BQ24745_CSIP
BQ24745_CSIN
AC_IN# to KBC
connect to KBC
30 AC_IN#
R235 100KR2J-1-GP
BQ24745_VREF
Jeff Modify 1129
C388 SC1U10V3KX-3GP
Q20 2N7002-11-GP
100KR2J-1-GP R236
AC_OK
3D3V_AUX_S5
100KR2J-1-GP R19
BQ24745_CHG_ON
R234 100KR2J-1-GP
31 CHG_ON#
connect to KBC
Q19 2N7002-11-GP
C13 SCD1U10V2KX-4GP
DY
R23 0R0402-PAD
<Core Design>
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER_BQ24745
Size A3
Document Number S13
Rev SC
Date: Friday, May 16, 2008
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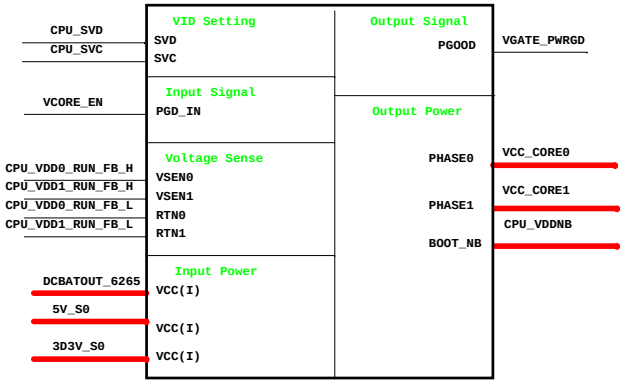
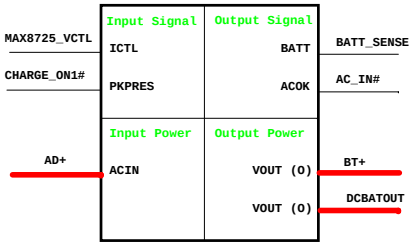
CPU_CORE
Intersil ISL6265



Charger Max8725



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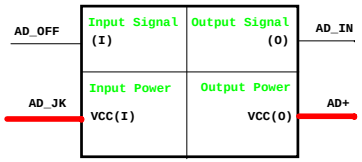

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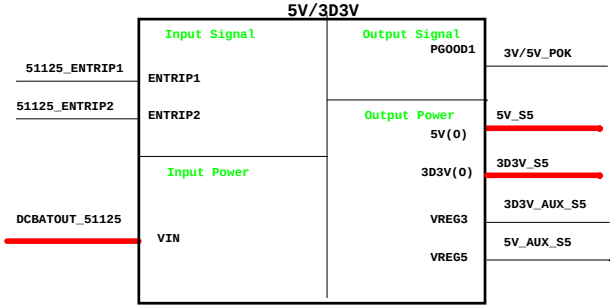

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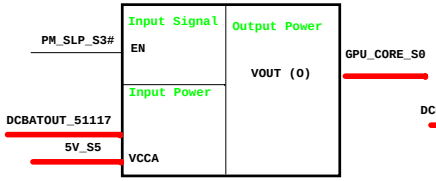
GPU_CORE



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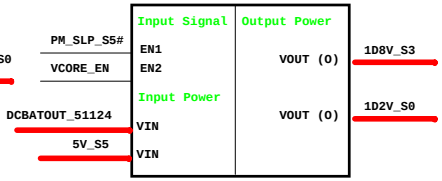

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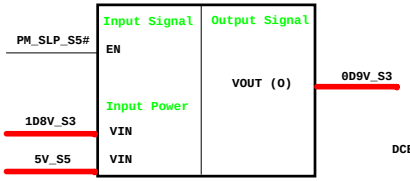

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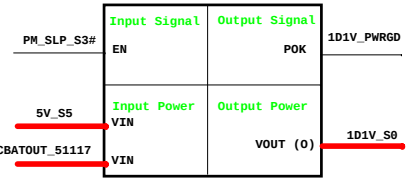

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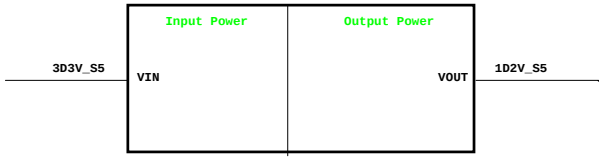

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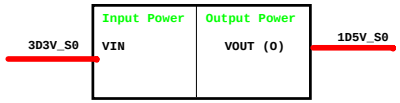

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Power Block Diagram*

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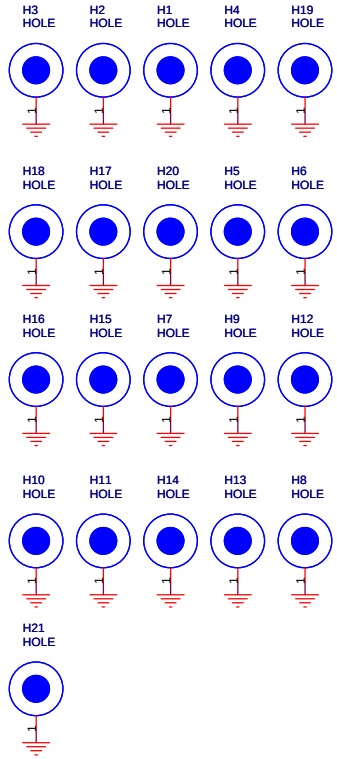

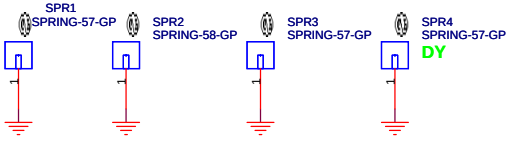

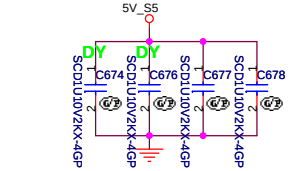

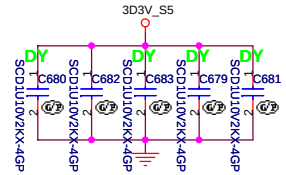

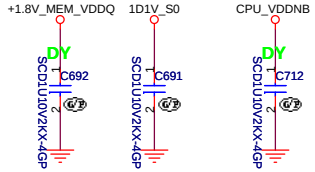

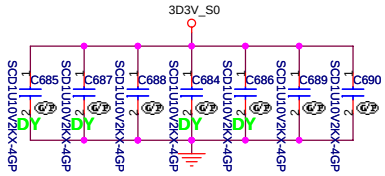

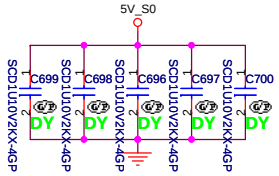

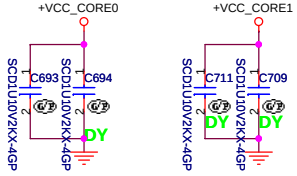

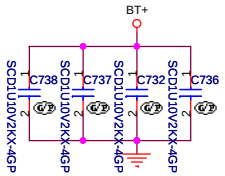

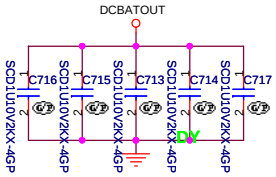

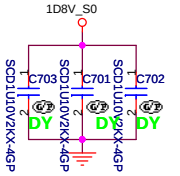

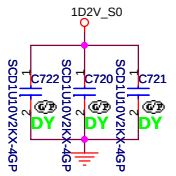

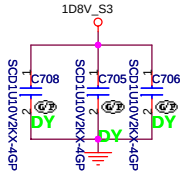

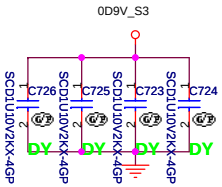

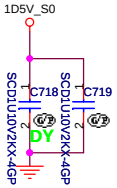

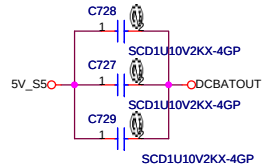

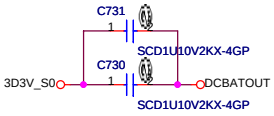

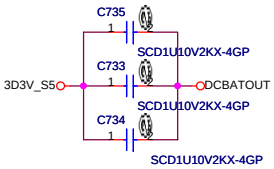

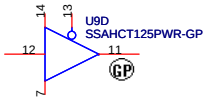

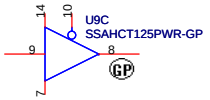

<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: MISC

Size: A3 | Document Number: S13 | Rev: SC

Date: Friday, May 16, 2008 | Sheet 43 of 44

NOTICE

Change List

Common Part

1.RS780M_A12 U55 71.RS780.M12
2.SB700_A12 U62 71.SB700.M06
3.KBC U29 71.00773.00G
4.CLKGEN U32 71.09480.A03
5.SIDE PORT U28 72.18512.M0U
6.MOSFET U52,U51 84.07686.037
7.MOSFET U13,U12,U49,U50 84.04634.037
8.H18,H19 34.4H802.001
9.CARD1 20.I0043.001
10.U61 71.00380.003
11. U11 74.06265.A73
12. U42 71.00888.E0G
13. U31 72.25X16.A01

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