First International Computer,Inc

Portable Computer Group HW Department

Board name : Mother Board Schematic

Project : CW0A0 (Diamondville+945GMS+ICH7M)

Version : 0.1

Initial Date : March 04, 2008

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Manager Sign by:Avery Lee

Drawing by : Beckham Chen/Leon Lee

Total confirm by:Jason Lee

LAN Circuit check by:

Audio Circuit check by:

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)875 1-8751

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1. Schematic Page Description :

CW0A0 Schematic Ver : 0.1

POWER CIRCUIT

DAUGHT BOARD

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD19	
AD23	

PCIINT	CHIP
IRQA	
IRQB	
IRQC	
IRQD	

BUSMASTER

REQ	CHIP
REQ0 / GNT0	
REQ1 / GNT1	
REQ2 / GNT2	
REQ3 / GNT3	
REQ4 / GNT4	

IRQ Channel	Desciption	
IRQ0	System timer	
IRQ1	Keyboard	
IRQ2	(Cascade)	
IRQ3	LAN / MODEM	
IRQ4	~~Serial Port~~	
IRQ5	AUDIO / VGA / USB	
IRQ6	~~FLOPPY DISK~~	
IRQ7	~~LPT~~	
IRQ8	RTC	
IRQ9	ACPI	
IRQ10	FIR (Disable by default)	(MODEM/LAN)
IRQ11	Cardbus	
IRQ12	~~PS/2 mouse~~	
IRQ13	FPU	
IRQ14	HDD	
IRQ15	CDROM	

DMA Channel	Device	
DMA0	FIR (disable by default)	(MODEM / LAN)
DMA1	~~ECP~~	
DMA2	~~FLOPPY DISK~~	
DMA3	AUDIO	
DMA4	(Cascade)	
DMA5	Unused	
DMA6	Unused	
DMA7	Unused	

First International Computer, Inc.
5FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2) 8751-8751

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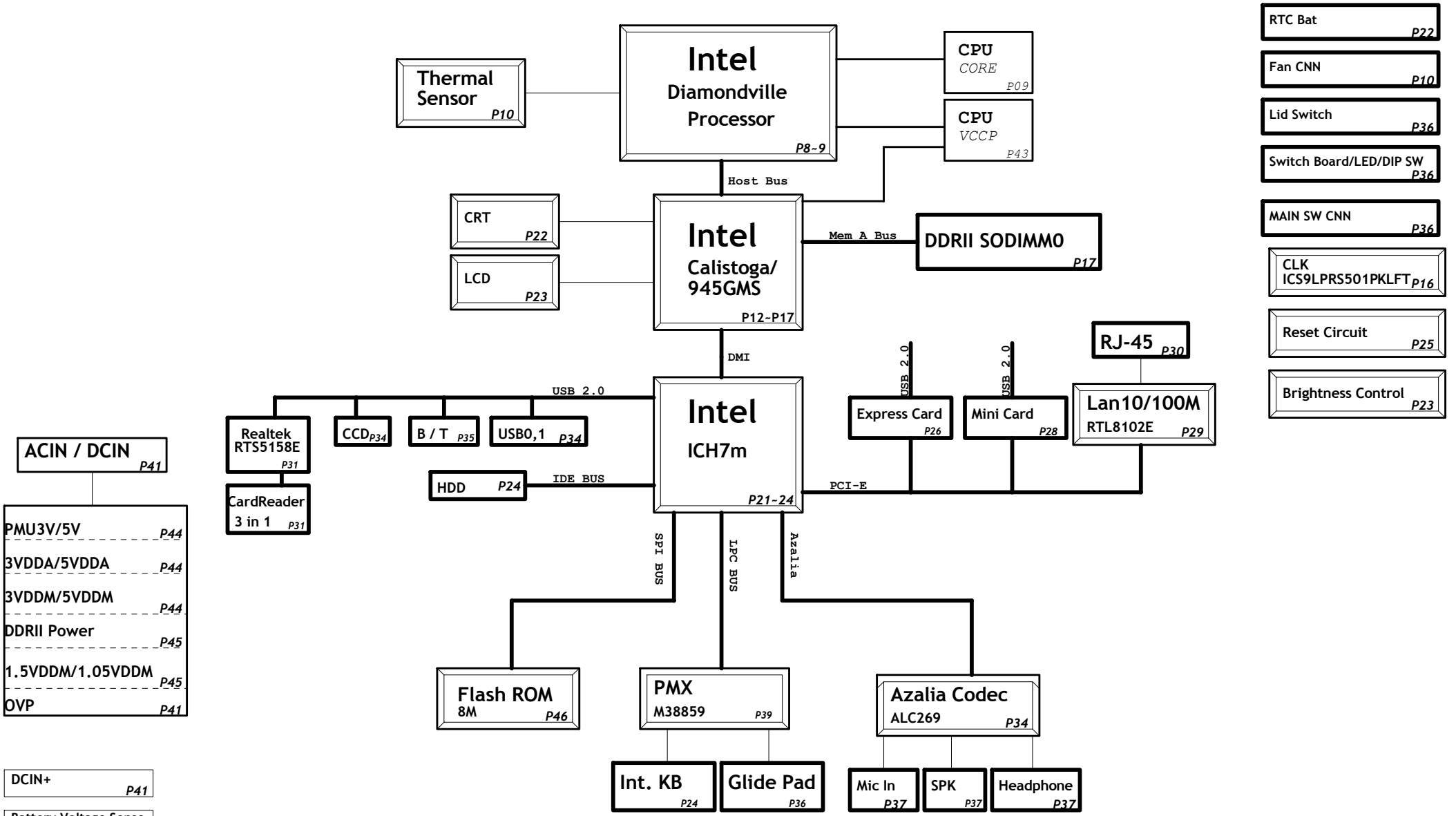
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

DCIN	Primary DC system power supply
PMU5V	5.0V always on power rail by LATCH or ACIN
PMU3V	3.3V always on power rail by LATCH or ACIN
5VDDA	5.0V always on power rail by DCON
3VDDA	3.3V always on power rail by DCON
3VDDS	3.3V power rail by PSUSC#
5VDDS	5.0V power rail by PSUSC#
3VDDM	3.3V switched power rail by SUSTAT_B#
5VDDM	5.0V switched power rail by SUSTAT_B#
VCC_CORE	Core Voltage for CPU
1.05VDDM	1.05V power rail for AGTL+ termination/Core for GMCH by SUSTAT_B#
1.5VDDM	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SUSTAT_B#
1.8VDDS	1.8V power rail for DDRII by PSUSC#
0.9VDDT_DDRII	0.9V DDRII Termination Voltage by SUSTAT_B#

Part Naming Conventions

C	=	Capacitor
CN	=	Connector
D	=	Diode
F	=	Fuse
L	=	Inductor
Q	=	Transistor
R	=	Resistor
RP	=	Resistor Pack
U	=	Arbitrary Logic Device
Y	=	Crystal and Osc

Net Name Suffix

#	=	Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Power Plane
Layer 3	Stripline Layer(AGTL,CLOCK,DDR)
Layer 4	Stripline Layer(Analog,LVDS,other)
Layer 5	Ground Plane
Layer 6	Solder Side,Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

Power Rail	Destination	Voltage	S0 Current
VCC_CORE	Diamondville HFM:	0.9V~1.1V	2.2A %Recommend Design Target 4A
	LFM:	0.75V~1.00V	1.5A
1.05VDDM	Diamondville: AGTL+ termination	1.0V~1.05V~1.1V	2.5A
	945GMs: Core	1.0V~1.05V~1.1V	2.94A
	945GMs: AGTL+ termination	0.9975V~1.05V~1.1025V	1.4A
	ICH7m:		
1.5VDDM	Diamondville PLL	1.425V~1.5V~1.575V	120mA
	945GMs: PCIE	1.425V~1.5V~1.575V	400mA
	945GMs: LVDS	1.425V~1.5V~1.575V	20mA
	945GMs: TVDAC	1.425V~1.5V~1.575V	24mA
	945GMs: Various PLLS analog supply	1.425V~1.5V~1.575V	320mA
	945GMs: DDR DLLS,DDRII,FSB HSIO	1.425V~1.5V~1.575V	1.25A
	ICH7m:		
	ICH7m:		
	ICH7m:		
	ICH7m:		
	Mini Card:		
	Express Card:		
1.8VDDS:	945GMs: DDRII System Memory	1.7V~1.8V~1.9V	1.72A
	SO-DIMM:		
0.9VDDT_DDRII:	DDRII Terminator:	0.855V~0.9V~0.945V	10uA
2.5VDDM	945GMs: PCIE analog	2.32V~2.5V~2.625V	2mA
	945GMs: LVDS analog	2.375V~2.5V~2.625V	10mA
	945GMs: LVDS I/O	2.375V~2.5V~2.625V	60mA
	945GMs: CRT DAC	2.32V~2.5V~2.625V	70mA
	CH7307:		
3VDDM	945GMs: HV CMOS	3.135V~3.3V~3.465V	40mA
	945GMs: TVDAC analog	3.135V~3.3V~3.465V	120mA
	ICH7m:		
	ICH7m:		
	ICH7m:		
	ICH7m:		
	ICH7m:		
	Mini Card:		
	Express Card:		
	CLK Generator: ICS9LPRS501PKLFT	3.135V~3.3V~3.465V	400mA
	Mini PCI: WirelessLan		
	KBC:		
	Flash ROM: BIOS		
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	Azalia MDC:		
	HDD: SATA		
3VDDS	CardBus:		
	CardBus:		
	Lan: Realtek RTL8102E		
	Card Reader: RTS5158E		
	Azalia MDC:		
	Mini PCI: For wake up		
3VDDA	ICH7m:		
	ICH7m:		
	ICH7m:		
	LCD:	3.0V~3.3V~3.6V	1.0A
5VDDM	Mini PCI:		
	Azalia Codec: ALC269	3.0V~3.3V~3.6V	
	Azalia MDC:		
	HDD: PATA	4.75V~5.0V~5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA
	ODD:		
	Audio AMP:		
	Woofer AMP:		
	Inverter:		
5VDDS	CardBus: Slot voltage		
	USB: x 4 ports	5V	2.0A
PMU3V	EC: PMX		
	ICH7m: RTC		

First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
114 TAIPEI, TAIWAN ,ROC
(886-2)875 1-8751

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6.Schematic modify Item and History :

1025
R479 change from 150ohm(NU) to 75ohm(NU)

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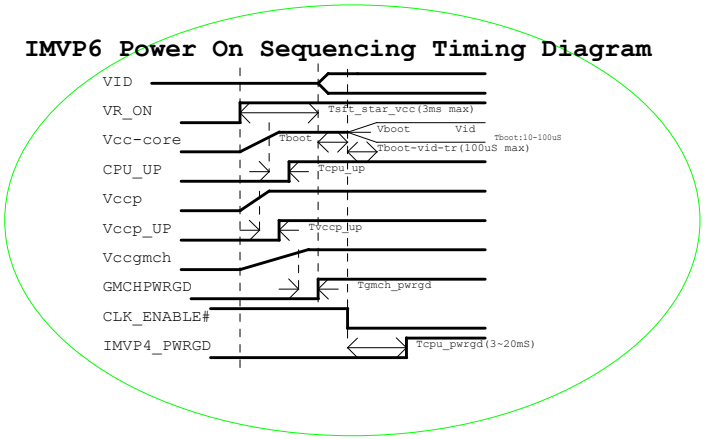
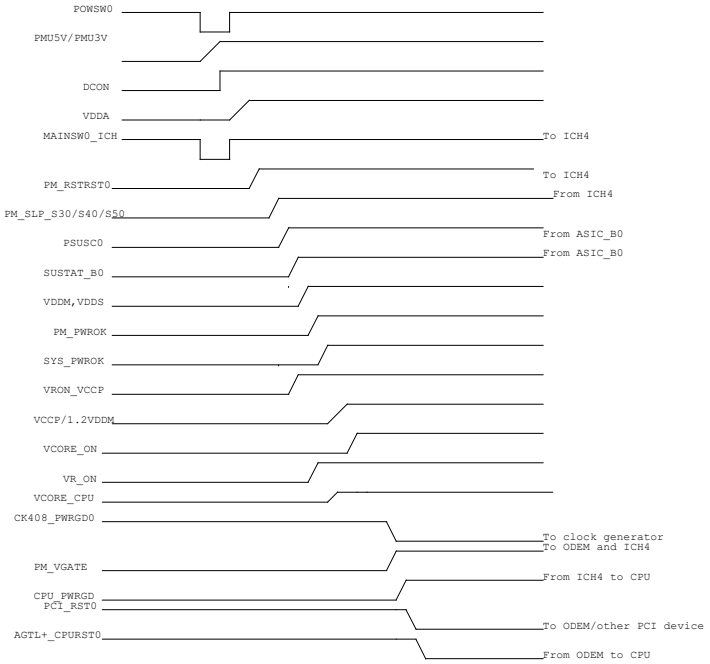
7. power on & off & S3 Sequence :

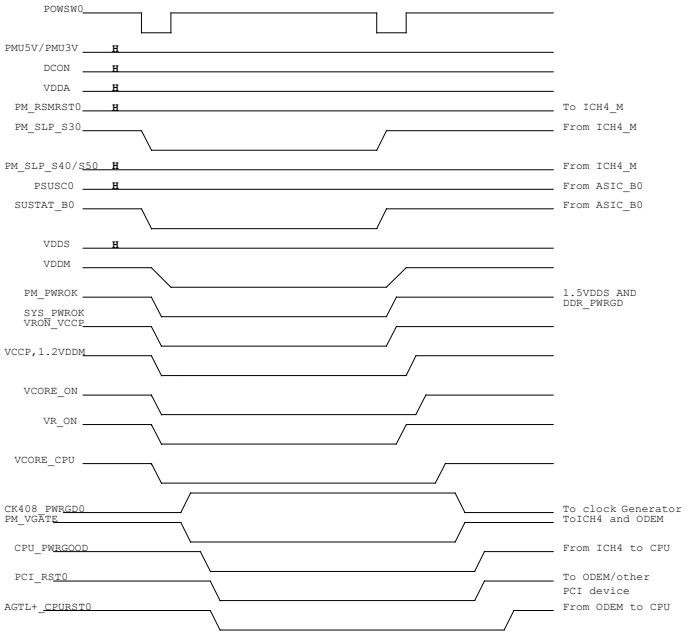
IMVP6 Power On Sequencing Timing Diagram



BATTERY ONLY POWER ON TIMING



S3 SUSPEND AND RESUME TIMING



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8. Layout Guideline :

Calistoga (945GM) DDRII Layout Guidelines

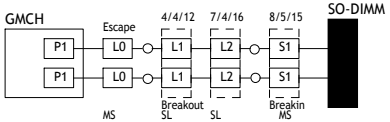
DDRII Signal Groups

Group	Signal Name
Data	SA_DQ[63..0]/SB_DQ[63..0] SA_DM[7..0]/SB_DM[7..0] SA_DQS[7..0]/SA_DQS#[7..0] SB_DQS[7..0]/SB_DQS#[7..0]
Address	SA_MA[13..0]/SB_MA[13..0] SA_BS[2..0]/SB_BS[2..0] SA_RAS#/SB_RAS# SA_CAS#/SB_CAS# SA_WE#/SB_WE#
Control	SM_CS#[3..0] SM_CKE[3..0] SM_ODT[3..0]
Clock	SM_CK[3..0] SM_CK#[3..0]
FeedBack	SA_RCVENOUT#/SB_RCVENOUT# SA_RCVENIN#/SB_RCVENIN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : SM_CK[3..0],SM_CK#[3..0]

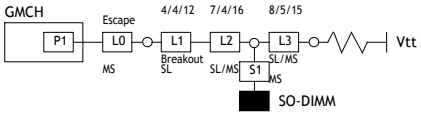


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Nominal Trace Width	Inner Layer : 7 mils Outer Layer : 8 mils
Nominal CK to CK# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum Serpentine Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Spacing to Other DDR2	Inner Layer : 16 mils Outer Layer : 20 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	1000 mils +/- 250 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group : SA_RCVENIN#],SA_RCVENOUT#,SB_RCVENIN#],SB_RCVENOUT#

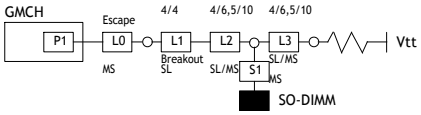
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : SM_CKE[3..0],SM_CS#[3..0],SM_ODT[3..0]



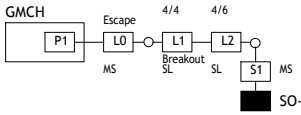
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 200 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group : SA_MA[13..0],SB_MA[13..0],SA_BS[2..0],SB_BS[2..0],SA_RAS#, SB_RAS#,SA_CAS#,SB_CAS#,SA_WE#,SB_WE#



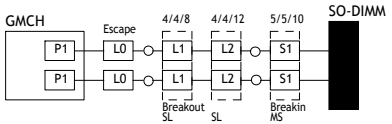
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : SA_DQ[63..0],SB_DQ[63..0],SA_DM[7..0],SB_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : SA_DQS[7..0],SA_DQS[7..0]#,SB_DQS[7..0],SB_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 50 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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2FL.,NO.300,Yang Guang St.,NeiHu
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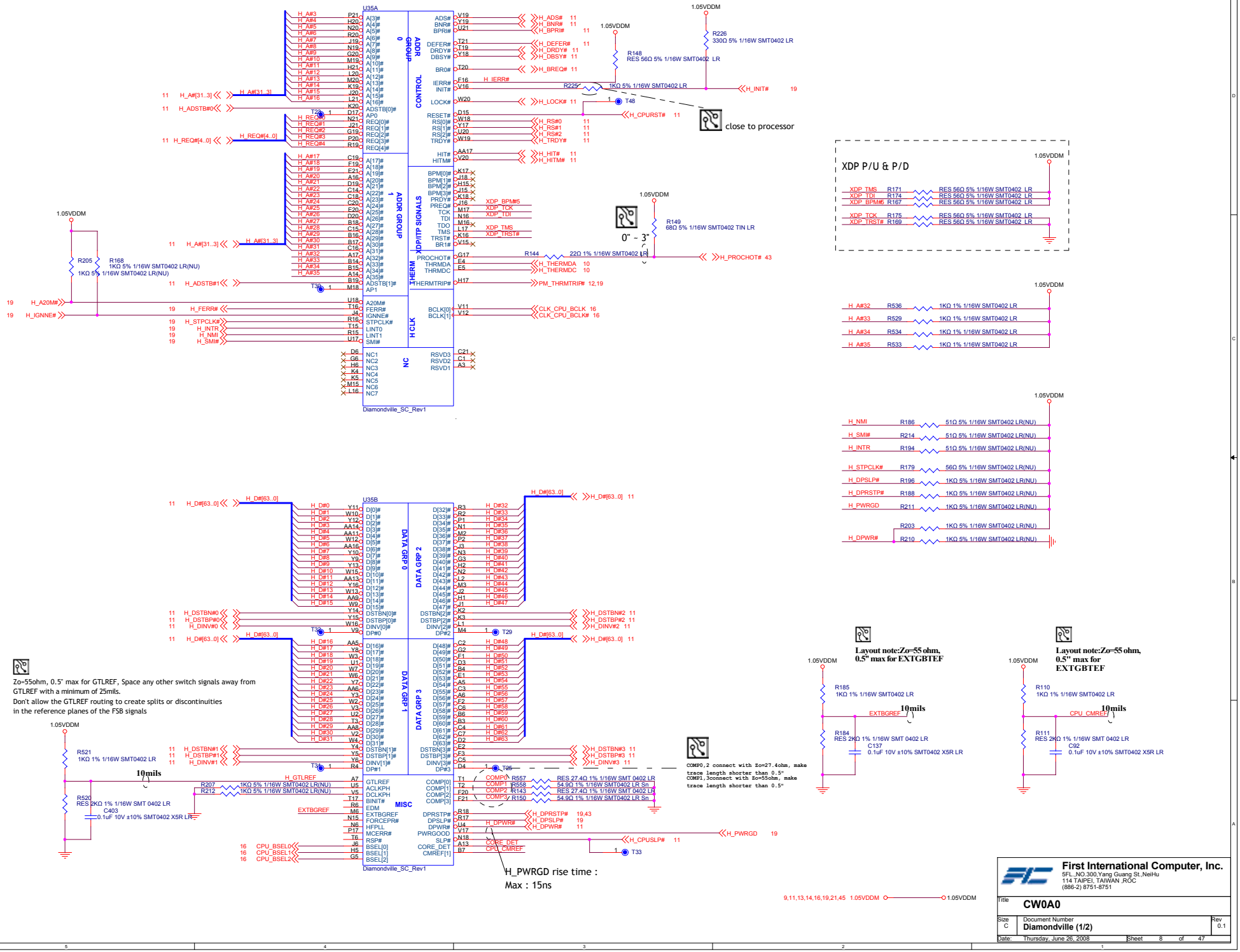

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Address	5FL.,NO.300,Yang Guang St.,NeiHu 114 TAIPEI, TAIWAN ,ROC
Phone	(886-2) 8751-8751
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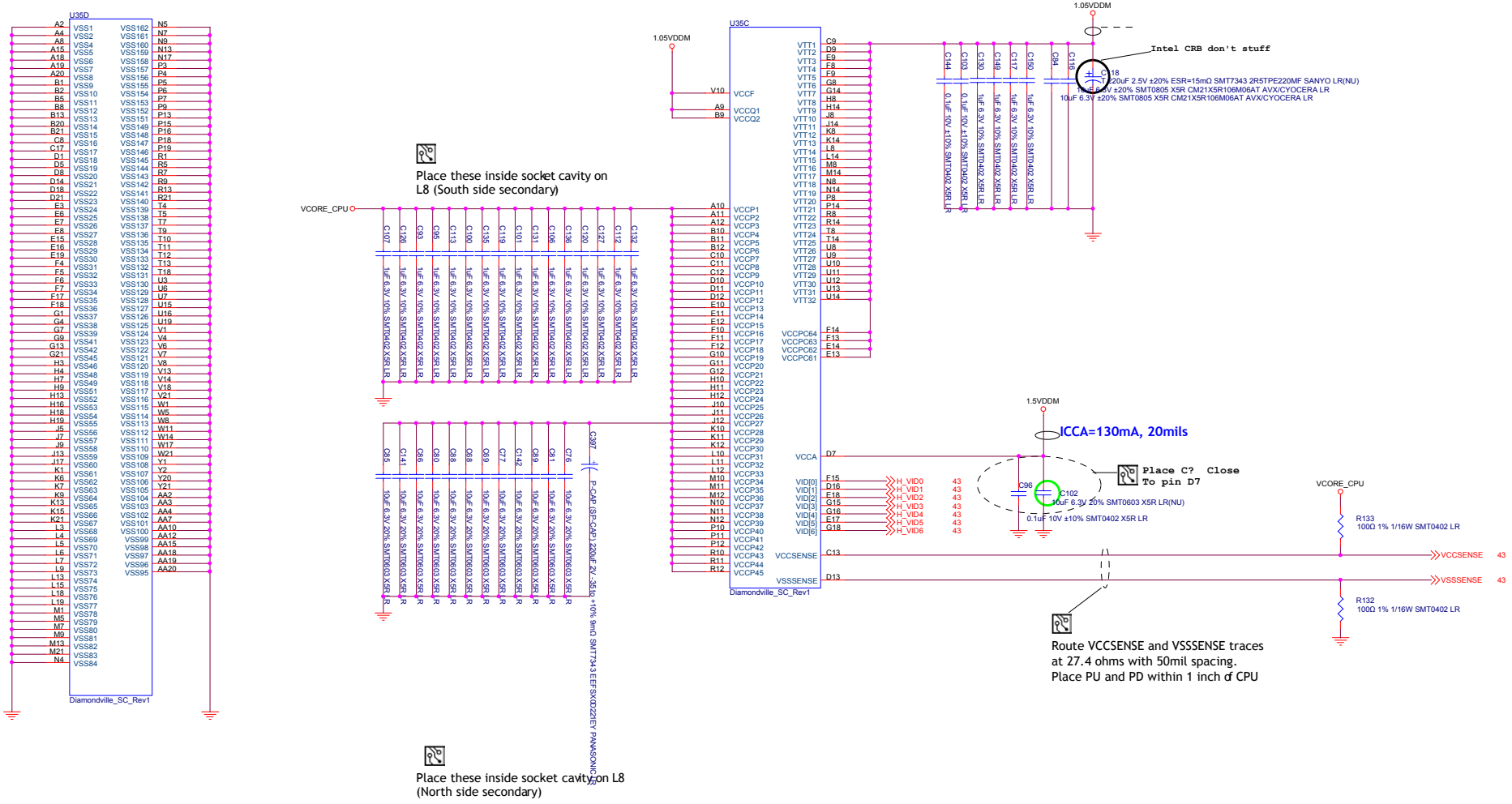

43 VCORE_CPU — VCORE_CPU

8,11,13,14,16,19,21,45 1.05VDDM — 1.05VDDM

12,13,14,18,21,27,28,45 1.5VDDM — 1.5VDDM

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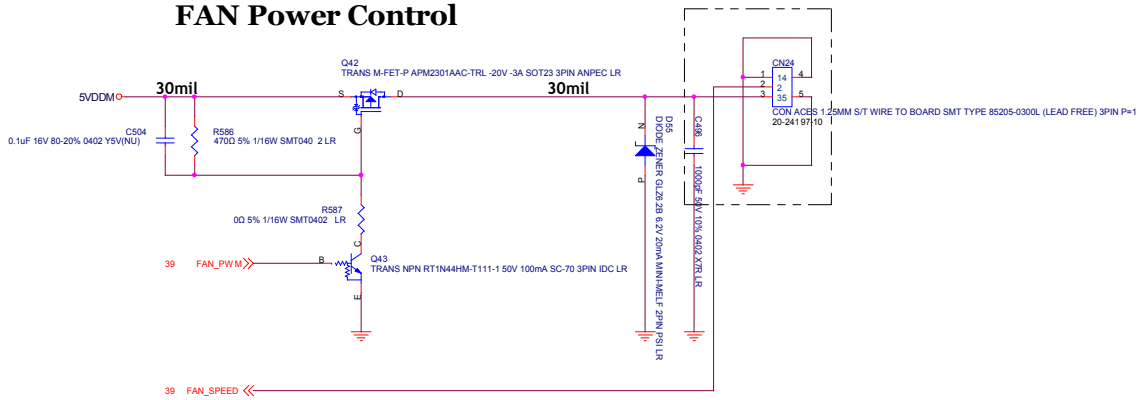
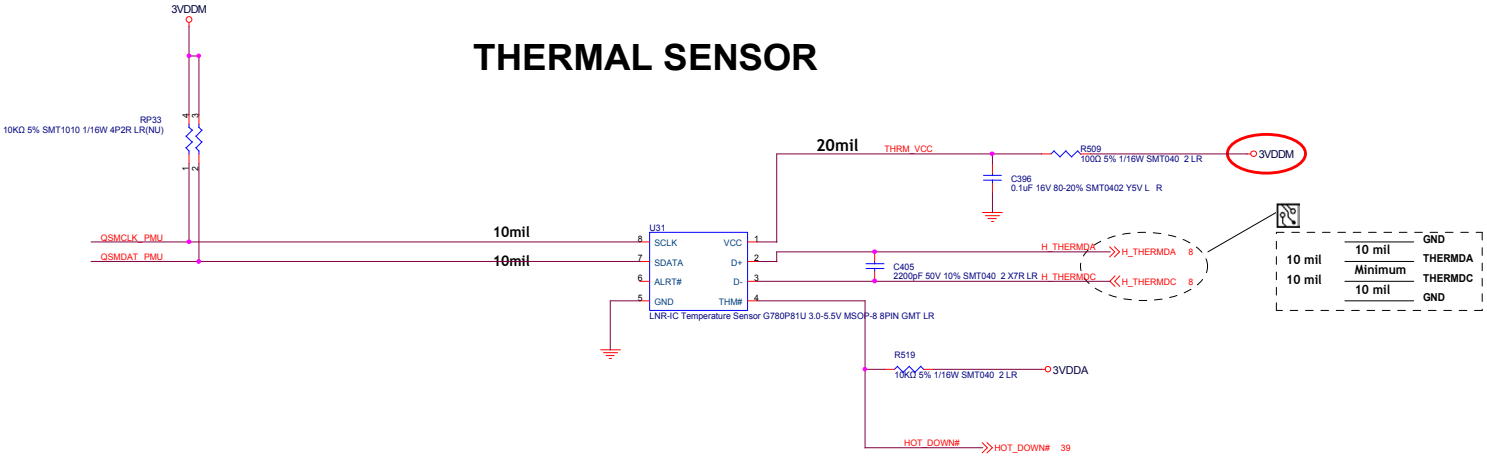
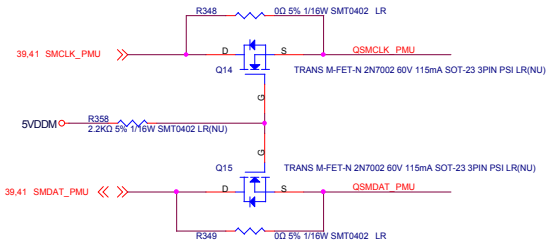
FAN Power Control



THERMAL SENSOR





18,20,21,23,25,26,27,28,29,35,36,38,39,41,4 4,45 3VDDA 3VDDA
12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39, 43,44 3VDDM 3VDDM
21,22,23,24,32,36,37,43,44, 45 5VDDM 5VDDM

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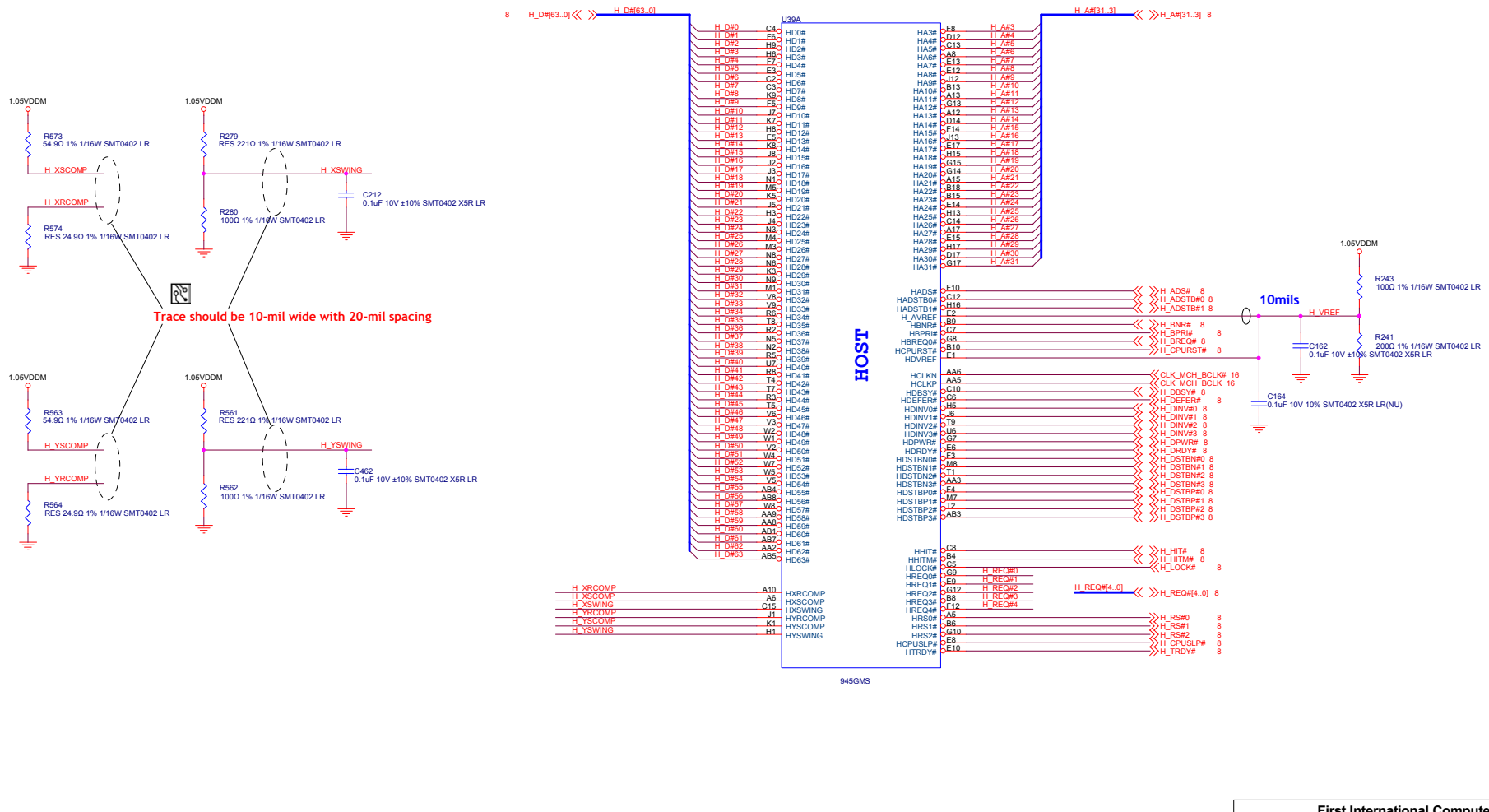
Title	CW0A0	
Size C	Document Number CPU Thermal	Rev 0.1
Date: Thursday, June 26, 2008	Sheet 10 of 47	



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Title	CW0A0	
Size C	Document Number 945GMS Host (1/5)	Rev 0.1
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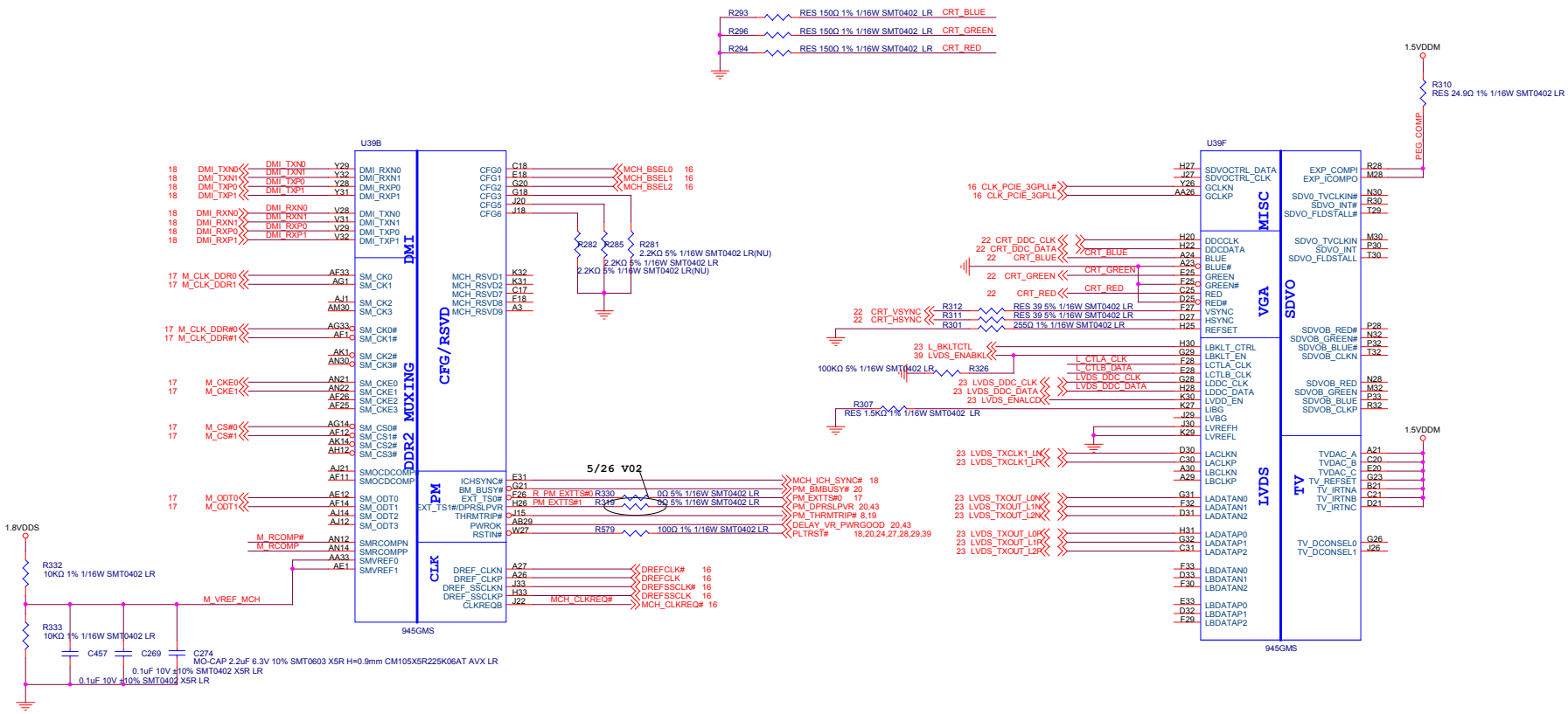

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Title	CW0A0
Size	C
Document Number	945GMS DMI/Graph (2/5)
Rev	0.1
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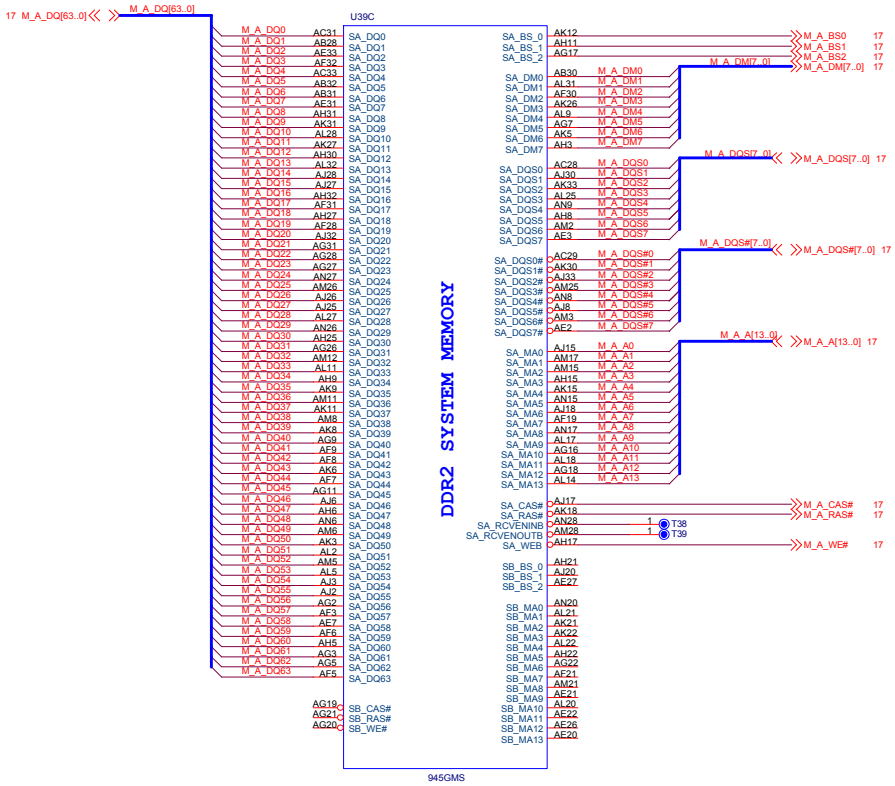

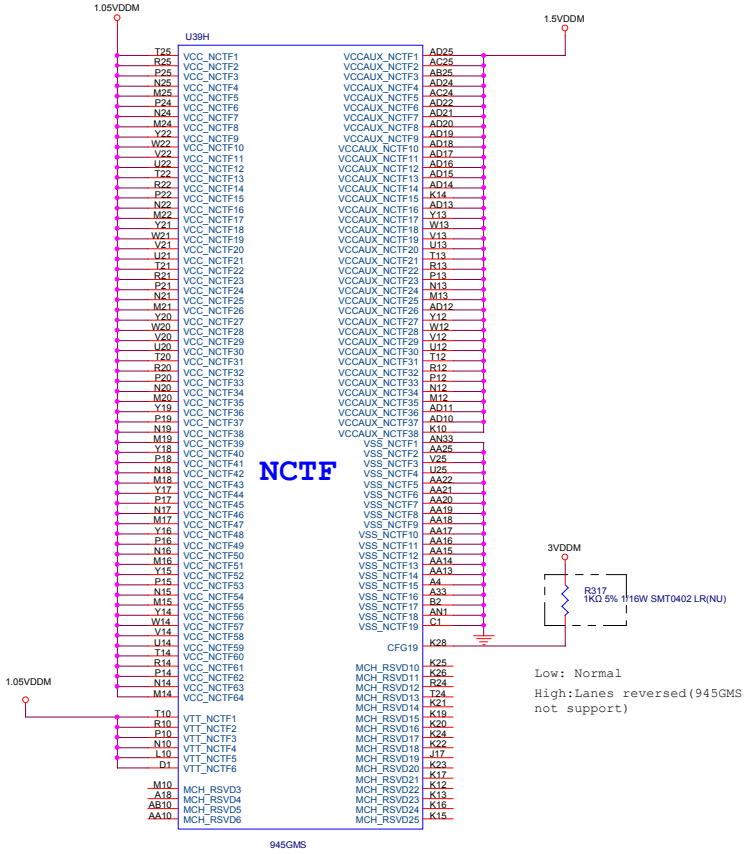

8,9,11,14,16,19,21,45 1.05VDDM → 1.05VDDM

9,12,14,18,21,27,28,45 1.5VDDM → 1.5VDDM

10,12,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39,43,44 3VDDM → 3VDDM

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Title: CW0A0

Size	Document Number	Rev
C	945GMS DDR2 (3/5)	0.1

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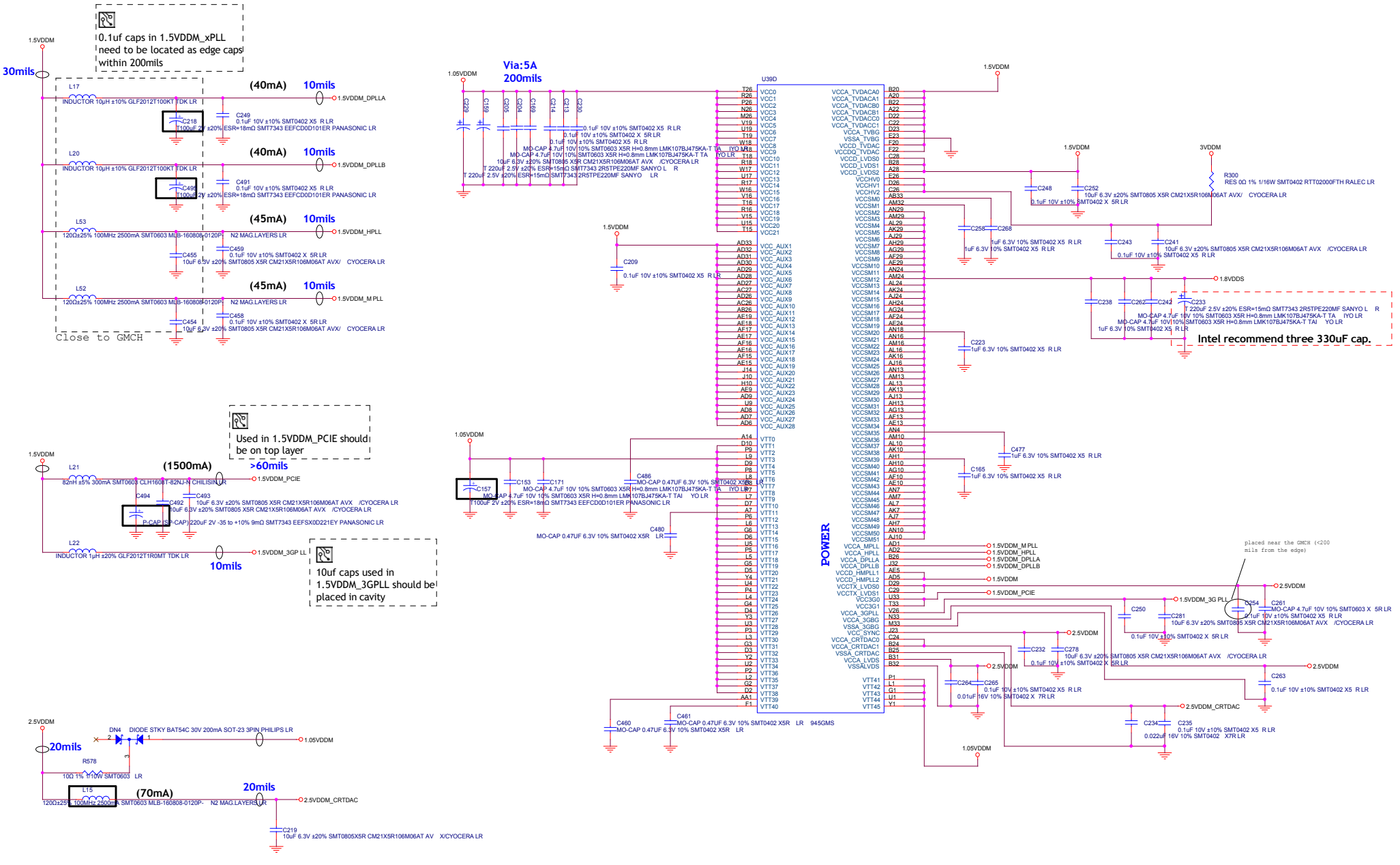
0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
1.5VDDM
30mils
L17
INDUCTOR 10µH ±10% GLF2012T100KT TDK LR
(40mA)
10mils
1.5VDDM_DPLLA
C218
C249
0.1uF 10V ±10% SMT0402 X5 R LR
L20
INDUCTOR 10µH ±10% GLF2012T100KT TDK LR
(40mA)
10mils
1.5VDDM_DPLLB
C491
L53
120Ω±25% 100MHz 2500mA SMT0603 MLB-160808-0120P- N2 MAG.LAYERS LR
(45mA)
10mils
1.5VDDM_HPLL
C455
C459
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/ CYOCERA LR
L52
120Ω±25% 100MHz 2500mA SMT0603 MLB-160808-0120P- N2 MAG.LAYERS LR
(45mA)
10mils
1.5VDDM_M PLL
C454
C458
Close to GMCH
Via:5A
200mils
1.05VDDM
U39D
C229
C159
C205
C204
C189
C214
C213
C230
0.1uF 10V ±10% SMT0402 X5 R LR
0.1uF 10V ±10% SMT0402 X 5R LR
0.1uF 10V ±10% SMT0402 X5 R LR
MO-CAP 4.7uF 10V 10% SMT0603 X5R H=0.8mm LMK107BJ475KA-T TA IYO LR
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
T 220uF 2.5V ±20% ESR=15mΩ SMT7343 2R5TPE220MF SANYO L R
T 220uF 2.5V ±20% ESR=15mΩ SMT7343 2R5TPE220MF SANYO LR
VCC0 VCC1 VCC2 VCC3 VCC4 VCC5 VCC6 VCC7 VCC8 VCC9 VCC10 VCC11 VCC12 VCC13 VCC14 VCC15 VCC16 VCC17 VCC18 VCC19 VCC20 VCC21
1.5VDDM
C209
0.1uF 10V ±10% SMT0402 X5 R LR
VCC_AUX1 VCC_AUX2 VCC_AUX3 VCC_AUX4 VCC_AUX5 VCC_AUX6 VCC_AUX7 VCC_AUX8 VCC_AUX9 VCC_AUX10 VCC_AUX11 VCC_AUX12 VCC_AUX13 VCC_AUX14 VCC_AUX15 VCC_AUX16 VCC_AUX17 VCC_AUX18 VCC_AUX19 VCC_AUX20 VCC_AUX21 VCC_AUX22 VCC_AUX23 VCC_AUX24 VCC_AUX25 VCC_AUX26 VCC_AUX27 VCC_AUX28
POWER
VCCA_TVDACA0 VCCA_TVDACA1 VCCA_TVDACB0 VCCA_TVDACB1 VCCA_TVDACC0 VCCA_TVDACC1 VCCA_TVBG VSSA_TVBG VCCD_TVDAC VCCDQ_TVDAC VCCD_LVDS0 VCCD_LVDS1 VCCD_LVDS2 VCCHV0 VCCHV1 VCCHV2 VCCSM0 VCCSM1 VCCSM2 VCCSM3 VCCSM4 VCCSM5 VCCSM6 VCCSM7 VCCSM8 VCCSM9 VCCSM10 VCCSM11 VCCSM12 VCCSM13 VCCSM14 VCCSM15 VCCSM16 VCCSM17 VCCSM18 VCCSM19 VCCSM20 VCCSM21 VCCSM22 VCCSM23 VCCSM24 VCCSM25 VCCSM26 VCCSM27 VCCSM28 VCCSM29 VCCSM30 VCCSM31 VCCSM32 VCCSM33 VCCSM34 VCCSM35 VCCSM36 VCCSM37 VCCSM38 VCCSM39 VCCSM40 VCCSM41 VCCSM42 VCCSM43 VCCSM44 VCCSM45 VCCSM46 VCCSM47 VCCSM48 VCCSM49 VCCSM50 VCCSM51 VCCA_MPLL VCCA_HPLL VCCA_DPLLA VCCA_DPLLB VCCD_HMPLL1 VCCD_HMPLL2 VCCTX_LVDS0 VCCTX_LVDS1 VCC3G0 VCC3G1 VCCA_3GPLL VCCA_3GBG VSSA_3GBG VCC_SYNC VCCA_CRTDAC0 VCCA_CRTDAC1 VSSA_CRTDAC VCCA_LVDS VSSALVDS VTT41 VTT42 VTT43 VTT44 VTT45
1.5VDDM
3VDDM
R300
RES 0Ω 1% 1/16W SMT0402 RTT02000FTH RALEC LR
C248
C252
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX/ CYOCERA LR
0.1uF 10V ±10% SMT0402 X 5R LR
C258
C268
1uF 6.3V 10% SMT0402 X5 R LR
C243
C241
0.1uF 10V ±10% SMT0402 X5 R LR
1.8VDDS
C238
C262
C242
C233
T 220uF 2.5V ±20% ESR=15mΩ SMT7343 2R5TPE220MF SANYO L R
MO-CAP 4.7uF 10V 10% SMT0603 X5R H=0.8mm LMK107BJ475KA-T TA IYO LR
1uF 6.3V 10% SMT0402 X5 R LR
Intel recommend three 330uF cap.
C223
1uF 6.3V 10% SMT0402 X5 R LR
C477
1uF 6.3V 10% SMT0402 X5 R LR
C165
1uF 6.3V 10% SMT0402 X5 R LR
1.05VDDM
C157
C153
C171
C486
MO-CAP 4.7uF 10V 10% SMT0603 X5R H=0.8mm LMK107BJ475KA-T TAI YO LR
T100uF 2V ±20% ESR=18mΩ SMT7343 EEFCD0D101ER PANASONIC LR
MO-CAP 0.47UF 6.3V 10% SMT0402 X5R LR
C480
MO-CAP 0.47UF 6.3V 10% SMT0402 X5R LR
C460
C461
MO-CAP 0.47UF 6.3V 10% SMT0402 X5R LR 945GMS
1.5VDDM
L21
82nH ±5% 300mA SMT0603 CLH1608T-82NJ-N CHILISIN LR
(1500mA)
>60mils
1.5VDDM_PCIE
C494
C493
C492
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
P-CAP (SP-CAP) 220uF 2V -35 to +10% 9mΩ SMT7343 EEFSX0D221EY PANASONIC LR
L22
INDUCTOR 1µH ±20% GLF2012T1R0MT TDK LR
1.5VDDM_3GP LL
10mils
Used in 1.5VDDM_PCIE should be on top layer
10uf caps used in 1.5VDDM_3GPLL should be placed in cavity
1.5VDDM_M PLL
1.5VDDM_HPLL
1.5VDDM_DPLLA
1.5VDDM_DPLLB
1.5VDDM
1.5VDDM_PCIE
1.5VDDM_3G PLL
placed near the GMCH (<200 mils from the edge)
2.5VDDM
C250
C281
C254
C261
MO-CAP 4.7uF 10V 10% SMT0603 X 5R LR
0.1uF 10V ±10% SMT0402 X5 R LR
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
0.1uF 10V ±10% SMT0402 X 5R LR
C232
C278
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
0.1uF 10V ±10% SMT0402 X 5R LR
C263
0.1uF 10V ±10% SMT0402 X5 R LR
C264
C265
0.1uF 10V ±10% SMT0402 X5 R LR
0.01uF 16V 10% SMT0402 X 7R LR
2.5VDDM_CRTDAC
C234
C235
0.1uF 10V ±10% SMT0402 X5 R LR
0.022uF 16V 10% SMT0402 X7R LR
1.05VDDM
2.5VDDM
DN4 DIODE STKY BAT54C 30V 200mA SOT-23 3PIN PHILIPS LR
20mils
1.05VDDM
R578
10Ω 1% 1/10W SMT0603 LR
L15
1200±25% 100MHz 2500mA SMT0603 MLB-160808-0120P- N2 MAG.LAYERS LR
(70mA)
20mils
2.5VDDM_CRTDAC
C219
10uF 6.3V ±20% SMT0805X5R CM21X5R106M06AT AV X/CYOCERA LR
8,9,11,13,16,19,21,45 1.05VDDM
9,12,13,18,21,27,28,4 5 1.5VDDM
10,12,13,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39, 43,44 3VDDM
45 2.5VDDM
12,17,4 5 1.8VDDS
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Title
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Document Number
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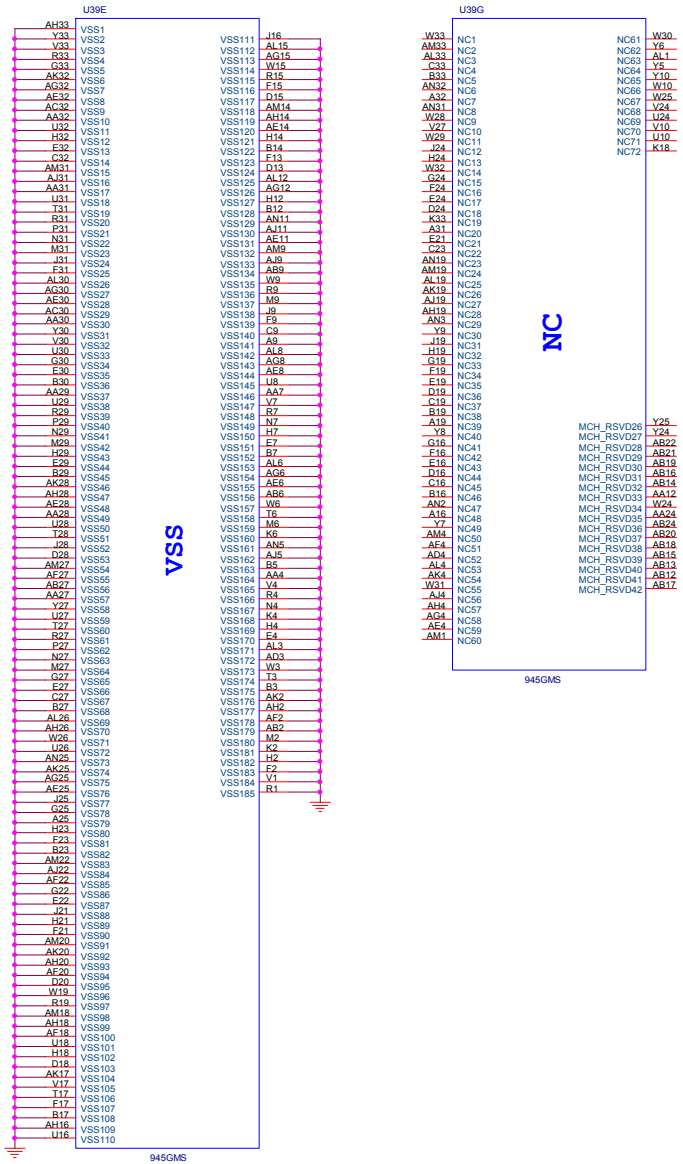
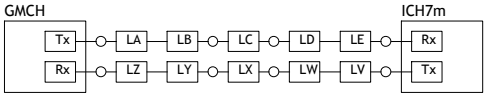


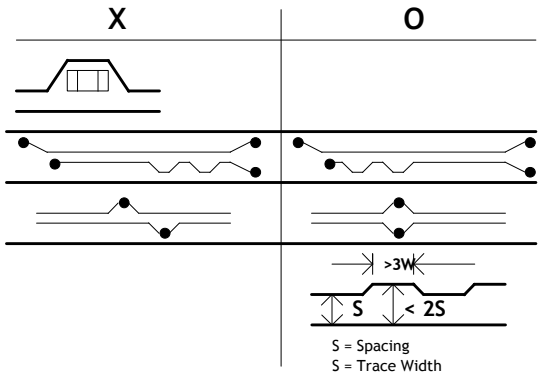
DMI Routing Guideline



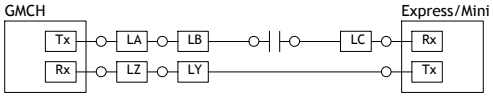
Breakout/in LA/LZ	Main Route LB/LY	Main Route LD/LW	Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 400 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



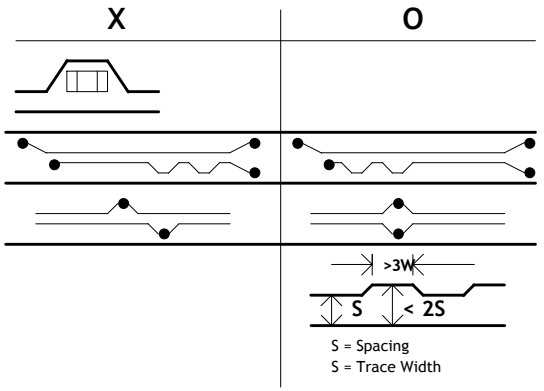
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



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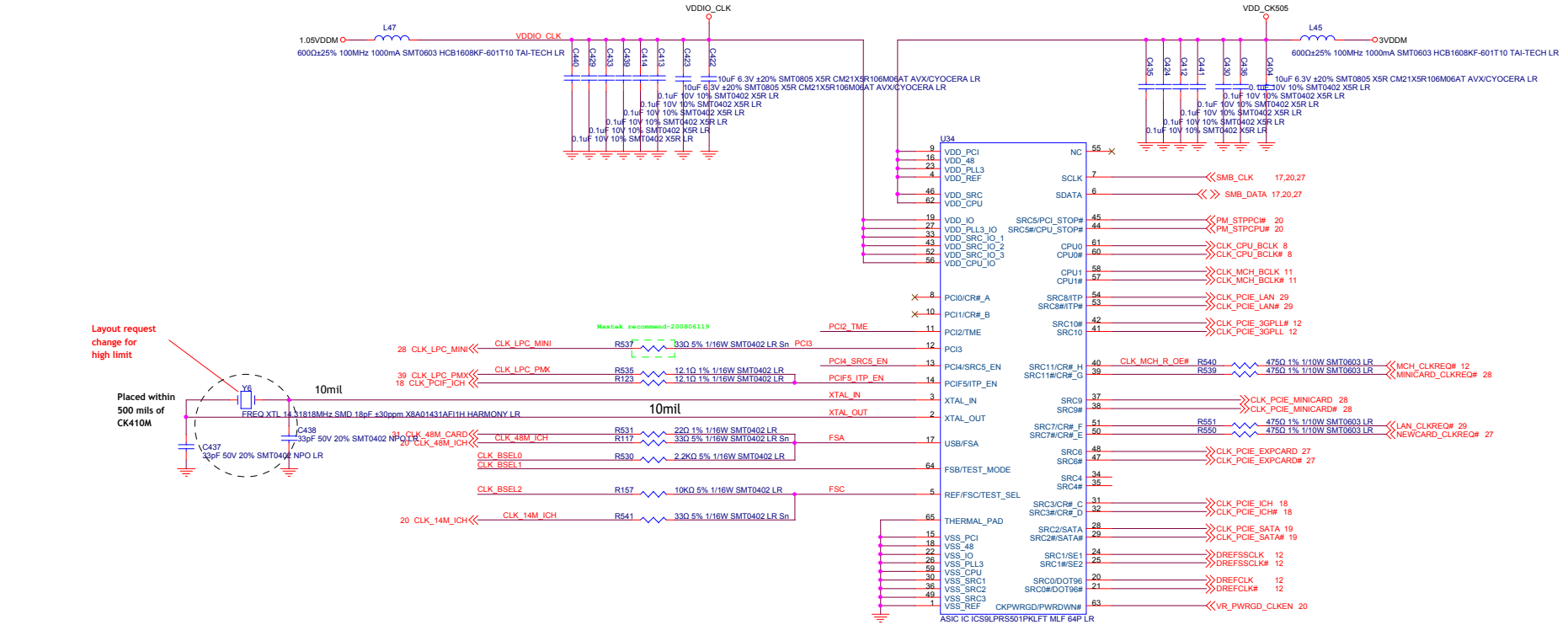

FSC	FSB	FSA	Host Clock
CPU_BSEL2	CPU_BSEL1	CPU_BSEL0	Frequency MHz
0	1	1	166
0	1	0	200

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Title	CW0A0
Size C	Document Number: Clock Generator IC ICS9LP505-1
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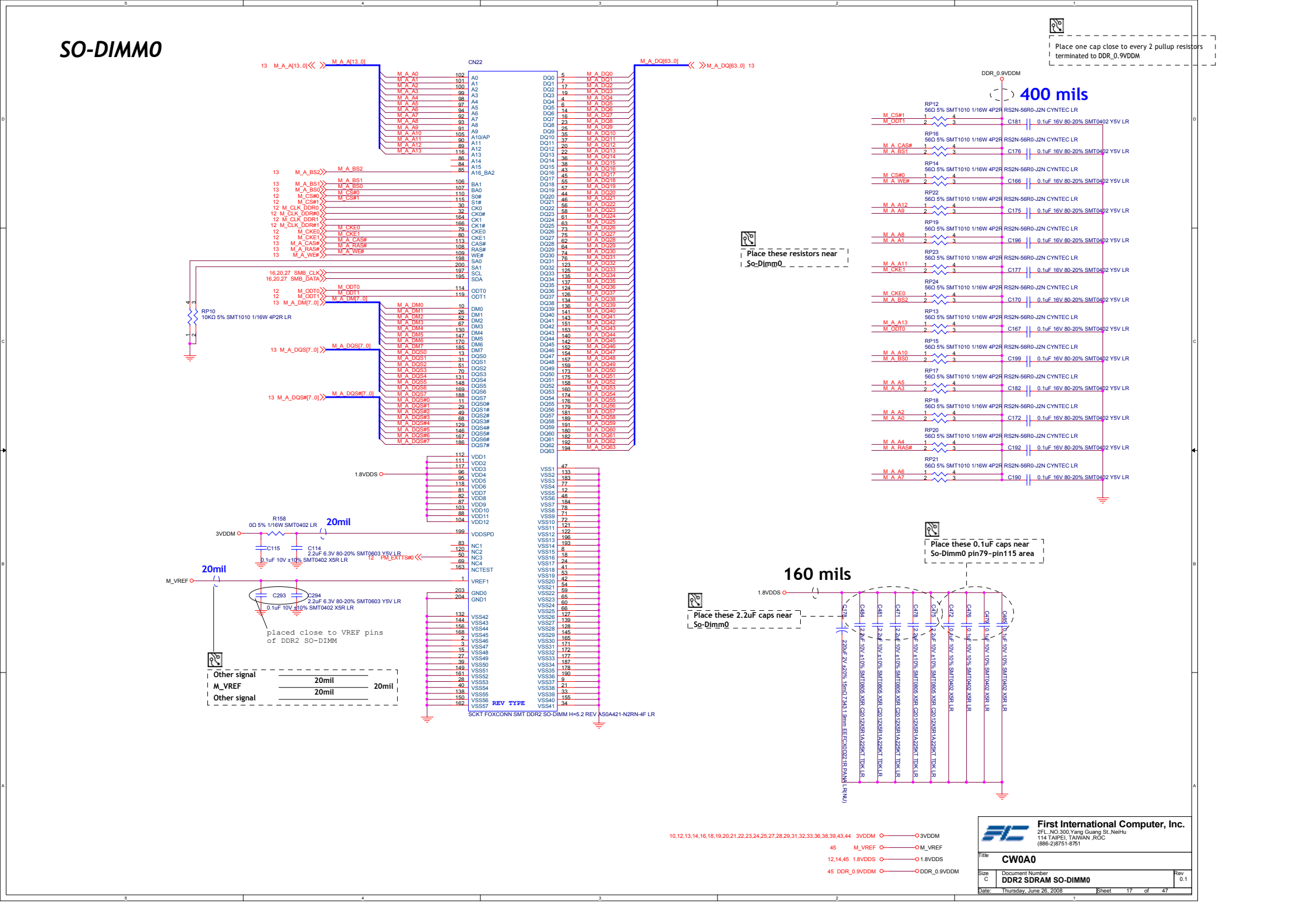
SO-DIMM0



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Title	CW0A0	
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PCIE AC coupling caps need to be within 250mils of the driver

Place close to ICH7m

Placed less than 100 mils from ICH7m

Place within 500mils of ICH

5/5 mils spacing on microstrip

Web-Cam
Module USB
Touch Panel
USB Port
Card Reader
New Card
USB Port
Bluetooth

PCI Pull up

PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#5	PCI_GNT#4	
1	1	LPC
1	0	PCI
0	1	SPI

Check BIOS type

Title	CW0A0
Size	C
Document Number	ICH7m PCI/PCIE/DMI (1/4)
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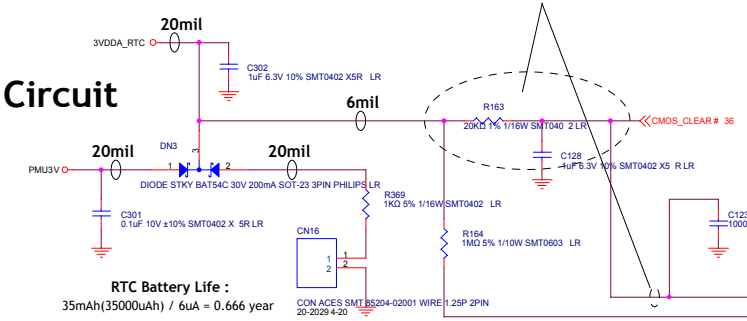
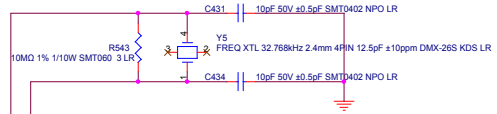
RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

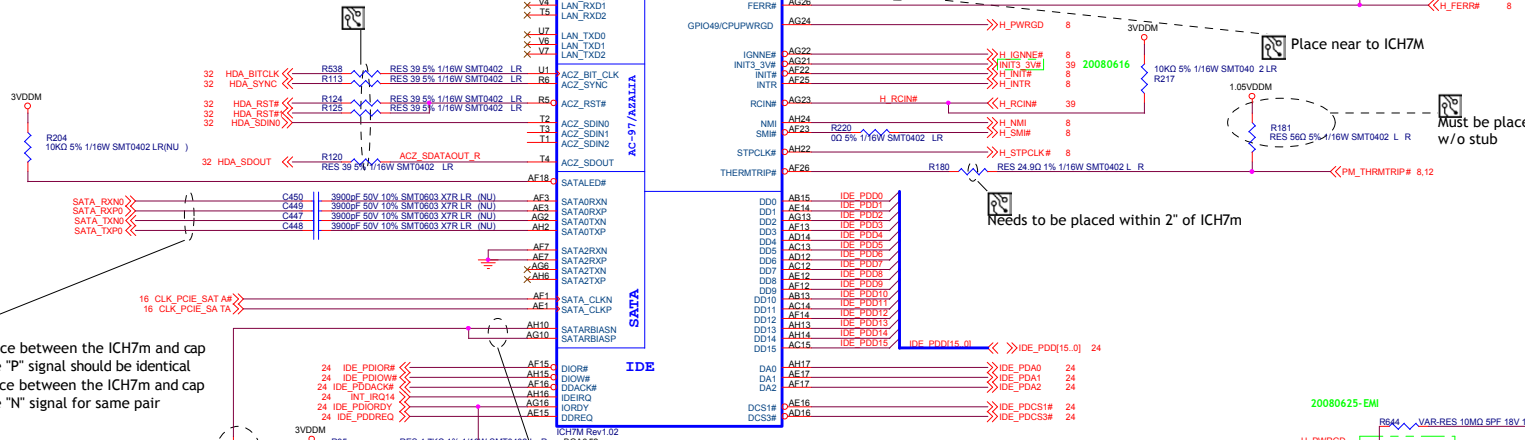
1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



RTC Battery Life :
35mAh(35000uAh) / 6uA = 0.666 year



Place all series resistors 0.6 to 2.6 inches from the ICH7



Place near to ICH7M

Must be placed within 2" of 24.9 ohm w/o stub

Needs to be placed within 2" of ICH7m

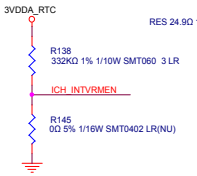
Distance between the ICH7m and cap on the "P" signal should be identical distance between the ICH7m and cap on the "N" signal for same pair

Placed within 500mils of ICH7m ball

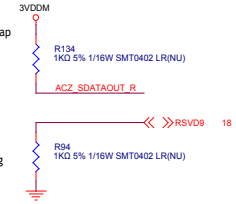
Short pins AH10 and AG10 at the package

ICH7m internal VR enable strap

	Enable	Disable
INTVRMEN	1(Default)	0

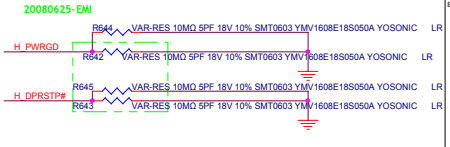


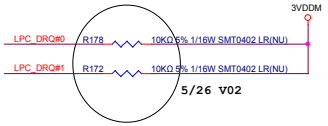
ACZ_SDATAOUT strap functionality base on RSVD9 strap
XOR chain entrance (RSVD9 pulled low)
PCIE port config bit 1(RSVD9 not pulled low)



Stuff for XOR chain testing

20080625-EMI





8,9,11,13,14,16,21,4 5 1.05VDDM → 1.05VDDM
9,12,13,14,18,21,27,28,4 5 1.5VDDM → 1.5VDDM
10,12,13,14,16,17,18,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39 ,43,44 3VDDM → 3VDDM
10,18,20,21,23,25,26,27,28,29,35,36,38,39,41,4 4,45 3VDDA → 3VDDA
24,39,41,4 4 PMU3V → PMU3V

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Title	CW0A0	
Size C	ICH7m CPU/IDE/SATA (2/4)	Rev 0.1
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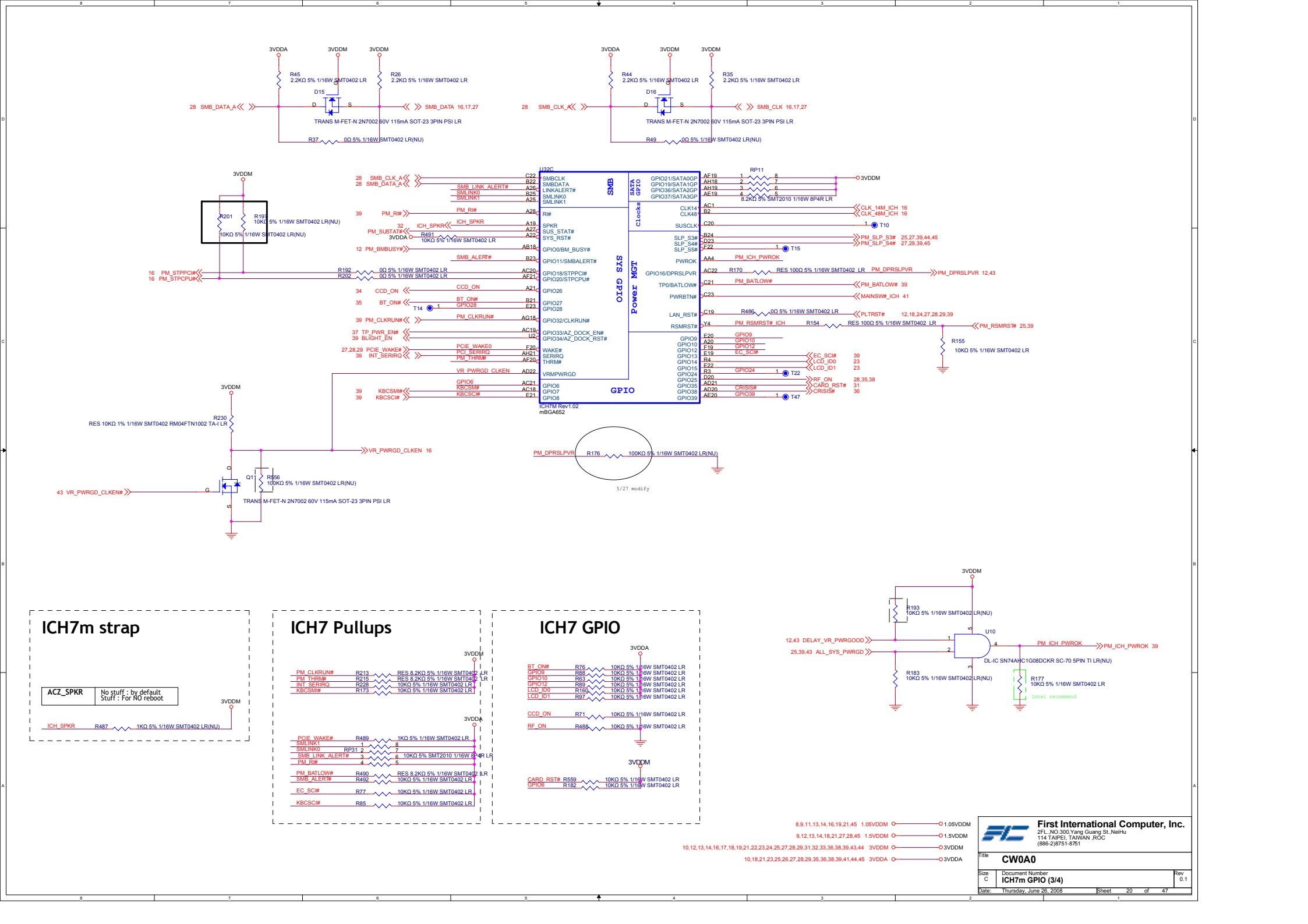
3VDDA
3VDDM
R45 2.2KΩ 5% 1/16W SMT0402 LR
R26 2.2KΩ 5% 1/16W SMT0402 LR
D15
28 SMB_DATA_A
SMB_DATA 16,17,27
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
R37 0Ω 5% 1/16W SMT0402 LR(NU)
R44 2.2KΩ 5% 1/16W SMT0402 LR
R35 2.2KΩ 5% 1/16W SMT0402 LR
D16
28 SMB_CLK_A
SMB_CLK 16,17,27
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
R49 0Ω 5% 1/16W SMT0402 LR(NU)
U32C
SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
ICH7M Rev1.02
mBGA652
RP11
8.2KΩ 5% SMT2010 1/16W 8P4R LR
3VDDM
CLK_14M_ICH 16
CLK_48M_ICH 16
T10
PM_SLP_S3# 25,27,39,44,45
PM_SLP_S4# 27,29,39,45
T15
PM_ICH_PWROK
R170 RES 100Ω 5% 1/16W SMT0402_LR
PM_DPRSLPVR
PM_DPRSLPVR 12,43
PM_BATLOW# 39
MAINSW#_ICH 41
R486 0Ω 5% 1/16W SMT0402 LR
PLTRST# 12,18,24,27,28,29,39
PM_RSMRST# ICH
R154 RES 100Ω 5% 1/16W SMT0402_LR
PM_RSMRST# 25,39
R155 10KΩ 5% 1/16W SMT0402 LR
GPIO9
GPIO10
GPIO12
EC_SCI#
GPIO24
RF_ON
CARD_RST#
CRISIS#
GPIO39
T22
T47
R201 10KΩ 5% 1/16W SMT0402 LR(NU)
R193 10KΩ 5% 1/16W SMT0402 LR(NU)
R491 10KΩ 5% 1/16W SMT0402 LR
R192 0Ω 5% 1/16W SMT0402 LR
R202 0Ω 5% 1/16W SMT0402 LR
T14
R230 RES 10KΩ 1% 1/16W SMT0402 RM04FTN1002 TA-I LR
VR_PWRGD_CLKEN 16
43 VR_PWRGD_CLKEN#
Q1
R556 100KΩ 5% 1/16W SMT0402 LR(NU)
TRANS M-FET-N 2N7002 60V 115mA SOT-23 3PIN PSI LR
PM_DPRSLPVR
R176 100KΩ 5% 1/16W SMT0402 LR(NU)
5/27 modify
ICH7m strap
ACZ_SPKR
No stuff : by default
Stuff : For NO reboot
ICH_SPKR
R487 1KΩ 5% 1/16W SMT0402 LR(NU)
ICH7 Pullups
PM_CLKRUN# R213 RES 8.2KΩ 5% 1/16W SMT0402 LR
PM_THRM# R215 RES 8.2KΩ 5% 1/16W SMT0402 LR
INT_SERIRQ R228 10KΩ 5% 1/16W SMT0402 LR
KBCSMI# R173 10KΩ 5% 1/16W SMT0402 LR
PCIE_WAKE# R489 1KΩ 5% 1/16W SMT0402 LR
SMLINK1
SMLINK0 RP31
SMB_LINK_ALERT#
PM_RI#
10KΩ 5% SMT2010 1/16W 8P4R LR
PM_BATLOW# R490 RES 8.2KΩ 5% 1/16W SMT0402 LR
SMB_ALERT# R492 10KΩ 5% 1/16W SMT0402 LR
EC_SCI# R77 10KΩ 5% 1/16W SMT0402 LR
KBCSCI# R85 10KΩ 5% 1/16W SMT0402 LR
ICH7 GPIO
BT_ON# R76 10KΩ 5% 1/16W SMT0402 LR
GPIO9 R88 10KΩ 5% 1/16W SMT0402 LR
GPIO10 R63 10KΩ 5% 1/16W SMT0402 LR
GPIO12 R89 10KΩ 5% 1/16W SMT0402 LR
LCD_ID0 R160 10KΩ 5% 1/16W SMT0402 LR
LCD_ID1 R97 10KΩ 5% 1/16W SMT0402 LR
CCD_ON R71 10KΩ 5% 1/16W SMT0402 LR
RF_ON R488 10KΩ 5% 1/16W SMT0402 LR
CARD_RST# R559 10KΩ 5% 1/16W SMT0402 LR
GPIO6 R182 10KΩ 5% 1/16W SMT0402 LR
R193 10KΩ 5% 1/16W SMT0402 LR(NU)
12,43 DELAY_VR_PWRGOOD
25,39,43 ALL_SYS_PWRGD
U10
DL-IC SN74AHC1G08DCKR SC-70 5PIN TI LR(NU)
PM_ICH_PWROK
PM_ICH_PWROK 39
R183 10KΩ 5% 1/16W SMT0402 LR(NU)
R177 10KΩ 5% 1/16W SMT0402 LR
Intel recommend
8,9,11,13,14,16,19,21,45 1.05VDDM
9,12,13,14,18,21,27,28,45 1.5VDDM
10,12,13,14,16,17,18,19,21,22,23,24,25,27,28,29,31,32,33,36,38,39,43,44 3VDDM
10,18,21,23,25,26,27,28,29,35,36,38,39,41,44,45 3VDDA
First International Computer, Inc.
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114 TAIPEI, TAIWAN ,ROC
(886-2)8751-8751
Title
CW0A0
Size C
Document Number
ICH7m GPIO (3/4)
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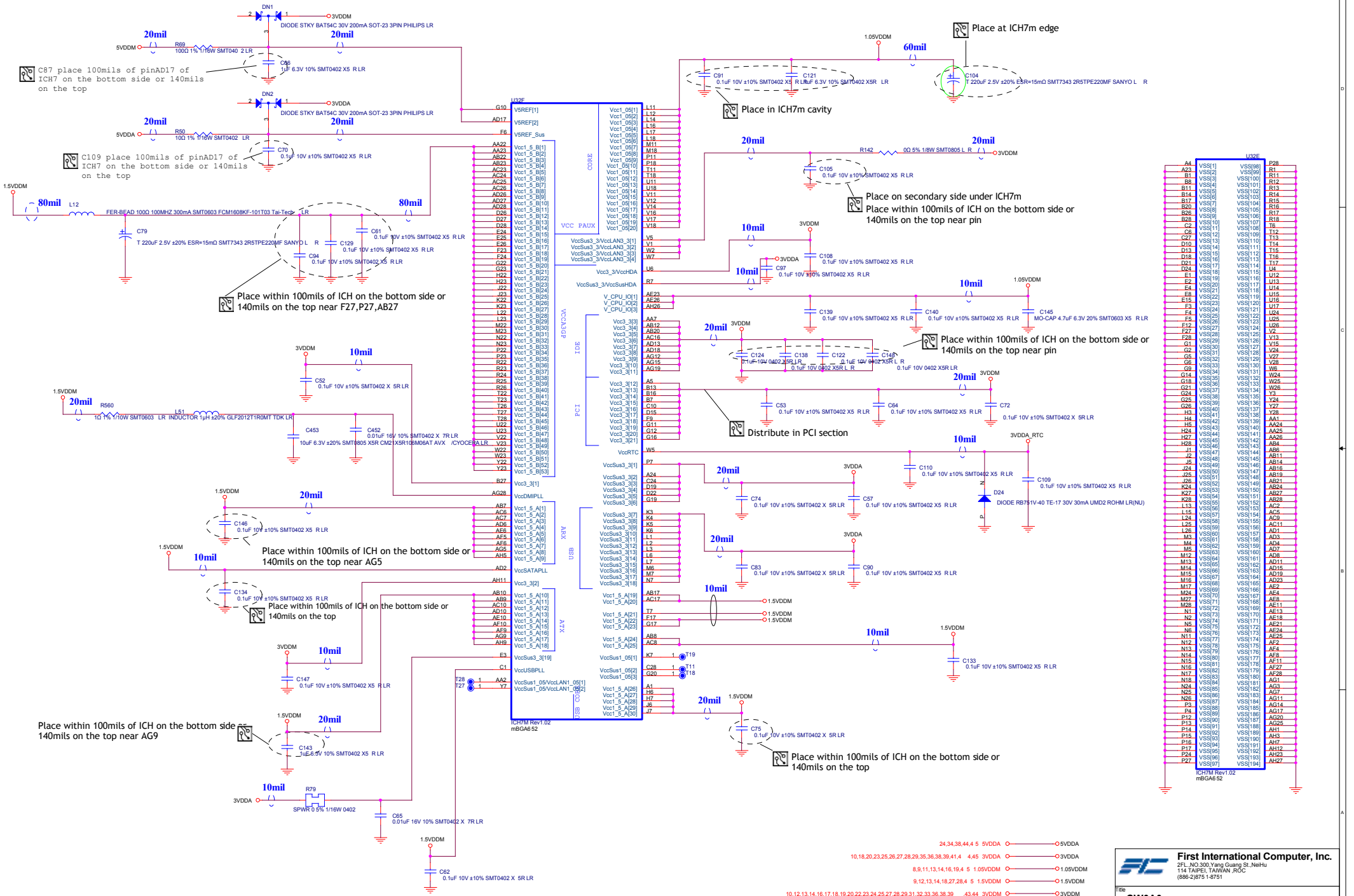
DN1
DIODE STKY BAT54C 30V 200mA SOT-23 3PIN PHILIPS LR
3VDDM
5VDDM
R69
100Ω 1% 1/16W SMT040 2 LR
C87 place 100mils of pinAD17 of ICH7 on the bottom side or 140mils on the top
C86
1uF 6.3V 10% SMT0402 X5 R LR
DN2
DIODE STKY BAT54C 30V 200mA SOT-23 3PIN PHILIPS LR
3VDDA
5VDDA
R50
10Ω 1% 1/16W SMT0402 LR
C109 place 100mils of pinAD17 of ICH7 on the bottom side or 140mils on the top
C70
0.1uF 10V ±10% SMT0402 X5 R LR
1.5VDDM
L12
FER-BEAD 100Ω 100MHZ 300mA SMT0603 FCM1608KF-101T03 Tai-Tech LR
C79
T 220uF 2.5V ±20% ESR=15mΩ SMT7343 2R5TPE220MF SANYO L R
C129
0.1uF 10V ±10% SMT0402 X5 R LR
C61
0.1uF 10V ±10% SMT0402 X5 R LR
C94
0.1uF 10V ±10% SMT0402 X5 R LR
Place within 100mils of ICH on the bottom side or 140mils on the top near F27,P27,AB27
C52
0.1uF 10V ±10% SMT0402 X 5R LR
R560
1Ω 1% 1/10W SMT0603 LR
L51
INDUCTOR 1μH ±20% GLF2012T1R0MT TDK LR
C453
10uF 6.3V ±20% SMT0805 X5R CM21X5R106M06AT AVX /CYOCERA LR
C452
0.01uF 16V 10% SMT0402 X 7R LR
C146
0.1uF 10V ±10% SMT0402 X5 R LR
Place within 100mils of ICH on the bottom side or 140mils on the top near AG5
C134
0.1uF 10V ±10% SMT0402 X5 R LR
Place within 100mils of ICH on the bottom side or 140mils on the top
C147
0.1uF 10V ±10% SMT0402 X5 R LR
Place within 100mils of ICH on the bottom side or 140mils on the top near AG9
C143
1uF 6.3V 10% SMT0402 X5 R LR
R79
SPWR 0 5% 1/16W 0402
C65
0.01uF 16V 10% SMT0402 X 7R LR
C62
0.1uF 10V ±10% SMT0402 X 5R LR
U32F
V5REF[1]
V5REF[2]
V5REF_Sus
CORE
VCC_PAUX
VCCA3GP
IDE
PCI
AGX
USB
ATX
CSI
USB
ICH7M Rev1.02
mBGA652
Place at ICH7m edge
C91
0.1uF 10V ±10% SMT0402 X5 R LR
C121
1uF 6.3V 10% SMT0402 X5R LR
C104
T 220uF 2.5V ±20% ESR=15mΩ SMT7343 2R5TPE220MF SANYO L R
Place in ICH7m cavity
R142
0Ω 5% 1/8W SMT0805 L R
C105
0.1uF 10V ±10% SMT0402 X5 R LR
Place on secondary side under ICH7m
Place within 100mils of ICH on the bottom side or 140mils on the top near pin
C108
0.1uF 10V ±10% SMT0402 X5 R LR
C97
0.1uF 10V ±10% SMT0402 X5 R LR
C139
0.1uF 10V ±10% SMT0402 X5 R LR
C140
0.1uF 10V ±10% SMT0402 X5 R LR
C145
MO-CAP 4.7uF 6.3V 20% SMT0603 X5 R LR
C124
0.1uF 10V 0402 X5R LR
C138
0.1uF 10V 0402 X5R LR
C122
0.1uF 10V 0402 X5R LR
C148
0.1uF 10V 0402 X5R LR
Place within 100mils of ICH on the bottom side or 140mils on the top near pin
C53
0.1uF 10V ±10% SMT0402 X5 R LR
C64
0.1uF 10V ±10% SMT0402 X5 R LR
C72
0.1uF 10V ±10% SMT0402 X 5R LR
Distribute in PCI section
3VDDA_RTC
C110
0.1uF 10V ±10% SMT0402 X5 R LR
C109
0.1uF 10V ±10% SMT0402 X5 R LR
D24
DIODE RB751V-40 TE-17 30V 30mA UMD2 ROHM LR(NU)
C74
0.1uF 10V ±10% SMT0402 X 5R LR
C57
0.1uF 10V ±10% SMT0402 X5 R LR
C83
0.1uF 10V ±10% SMT0402 X 5R LR
C90
0.1uF 10V ±10% SMT0402 X5 R LR
1.5VDDM
C133
0.1uF 10V ±10% SMT0402 X5 R LR
C75
0.1uF 10V ±10% SMT0402 X 5R LR
Place within 100mils of ICH on the bottom side or 140mils on the top
24,34,38,44,4 5 5VDDA
10,18,20,23,25,26,27,28,29,35,36,38,39,41,4 4,45 3VDDA
8,9,11,13,14,16,19,4 5 1.05VDDM
9,12,13,14,18,27,28,4 5 1.5VDDM
10,12,13,14,16,17,18,19,20,22,23,24,25,27,28,29,31,32,33,36,38,39 ,43,44 3VDDM
10,22,23,24,32,36,37,43,44 ,45 5VDDM
First International Computer, Inc.
2FL.,NO.300,Yang Guang St.,NeiHu
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Title
CW0A0
Size Custom
Document Number
ICH7m Power/GND (4/4)
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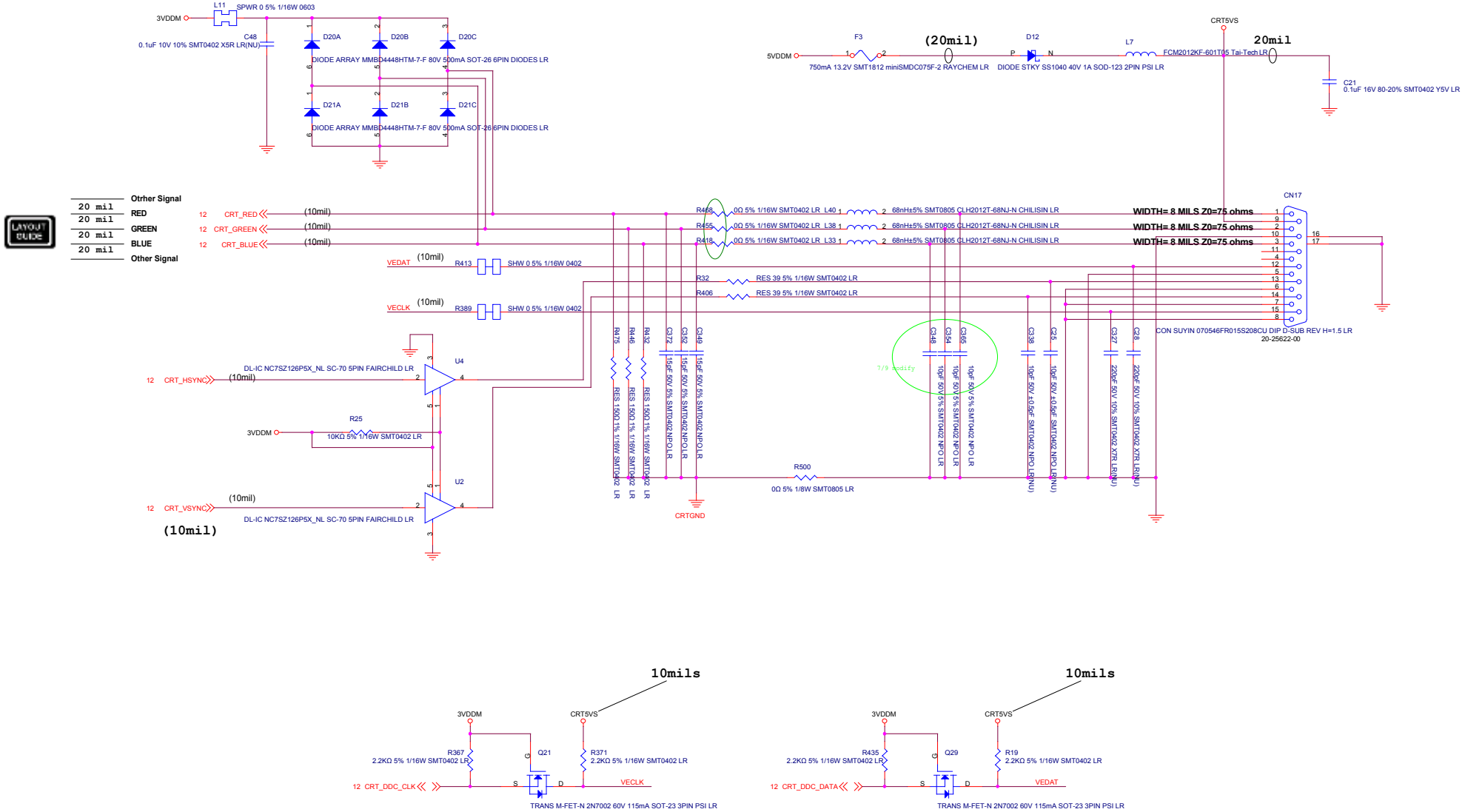

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Title: CW0A0

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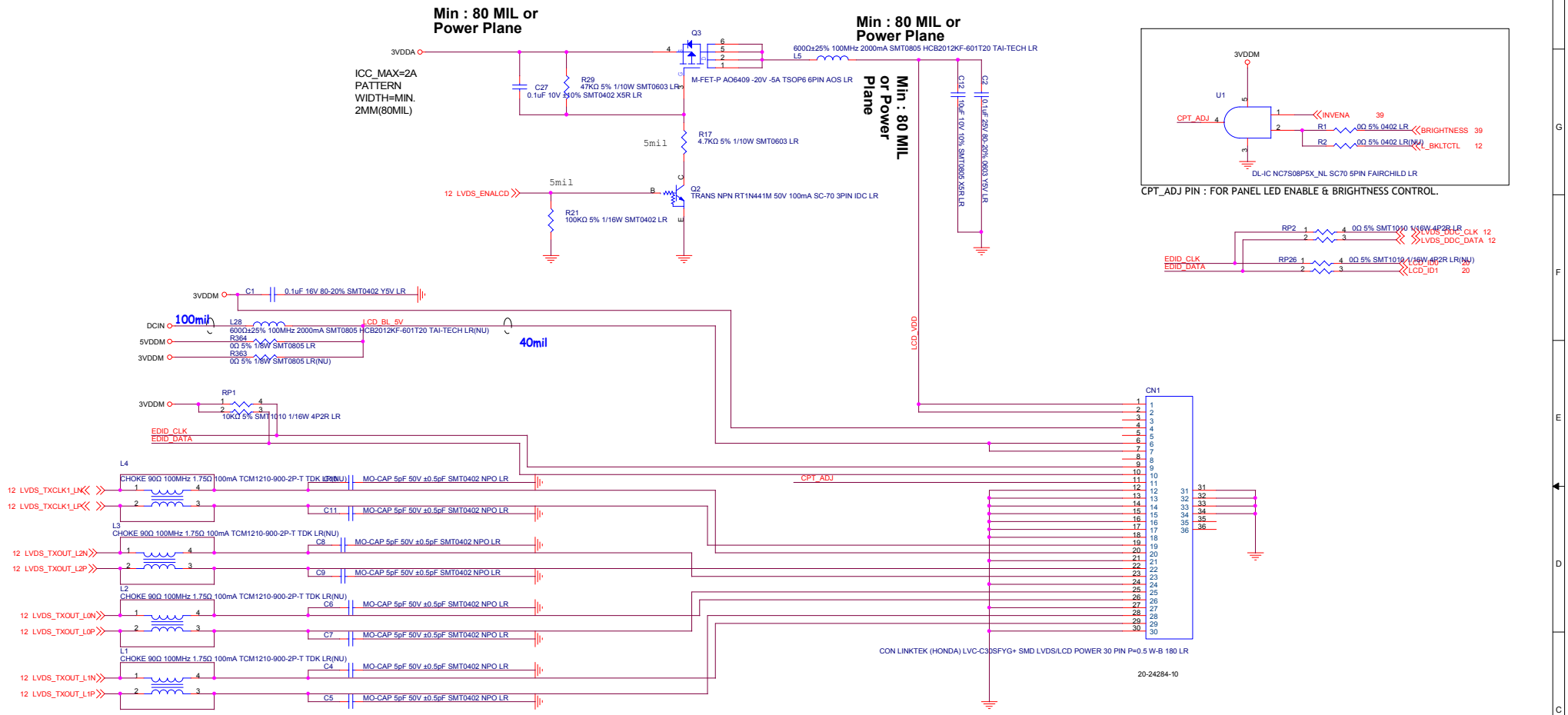
Only for CE260 & CE261 Panel circuit.



HannStar 8.9"W WSVGA 1024*600

(HSD089IFW1-A IF: LVDS Digital)

(PANEL SIDE / MB SIDE) 20080401A-BUILD FOR 8.9"

20080401A-CE262 V0.3 (CE2A1 V0.1) USE.

* EN PIN : PWM frquency min: 120Hz, max: 25KHz
("HIGH" = 1.7V~5.5V, "LOW" = 0V~0.4V)

* [ ]: LCD cable need to twist by pair.

01	18	GND	11	29	RxIN1-	21		NC	31	12	VLED_GND
02	01	VDD (+3.3V)	12	28	RxIN1+	22	15	GND	32	13	VLED_GND
03	02	VDD (+3.3V)	13	30	GND	23		NC	33	14	VLED_GND
04	04	VEDID (+3.3V)	14	23	RxIN2-	24		NC	34		NC
05		NC	15	22	RxIN2+	25	16	GND	35		NC
06	09	CLKEDID	16	24	GND	26		NC	36		NC
07	10	DATAEDID	17	20	RxCLKIN-	27		NC	37		NC
08	26	RxIN0-	18	19	RxCLKIN+	28	17	GND	38	11	ADJ
09	25	RxIN0+	19	21	GND	29	06	VLED (+5V)	39		NC
10	27	GND	20		NC	30	07	VLED (+5V)	40		NC

CPT 7" TFT LCD (CLAA070LC0ECT)

(CPT DOC. NO. SPEC-CLAA070LC0ECT-FIC-070314)

20080401A-CE262 V0.2 USE / CE2A1 CANCEL THE SPEC.

(PANEL SIDE / MB SIDE) (LVDS CLK Frequency 25MHz ~ 32MHz)

01		AVSS	11		RxIN1-	21		NC
02		VCC (LCD/3.3V)	12		RxIN1+	22		AVSS
03		VCC (LCD/3.3V)	13		AVSS	23		NC
04		NC	14		RxIN2-	24		VDD (LED / 5V)
05		ADJ	15		RxIN2+	25		VDD (LED / 5V)
06		NC	16		AVSS	26		VDD (LED / 5V)
07		NC	17		RXCLK-	27		NC
08		RxIN0-	18		RXCLK+	28		AVSS
09		RxIN0+	19		AVSS	29		NC
10		AVSS	20		NC	30		NC

10,18,20,21,25,26,27,28,29,35,36,38,39,41,44,45 3VDDA

10,13,14,16,17,18,19,20,21,22,24,25,27,28,29,31,32,33,36,38,39,43,44 3VDDM

10,21,22,24,32,36,37,43,44,45 5VDDM

41,42,43,45 DCIN

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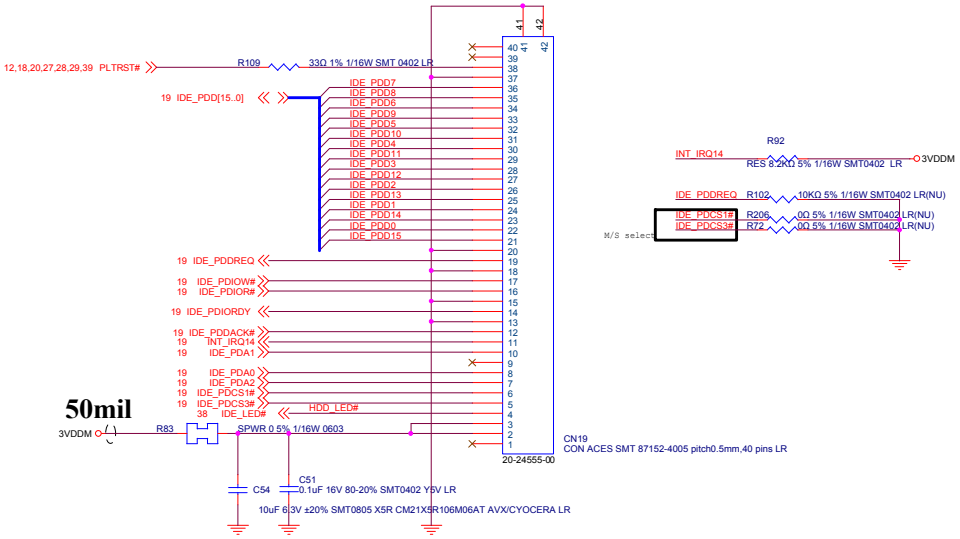
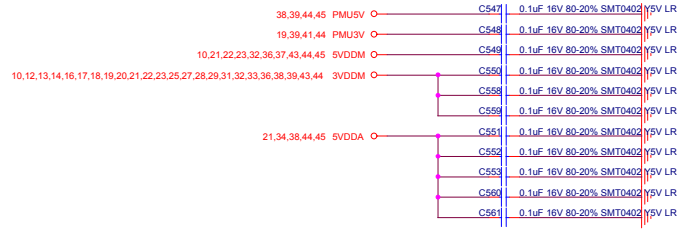
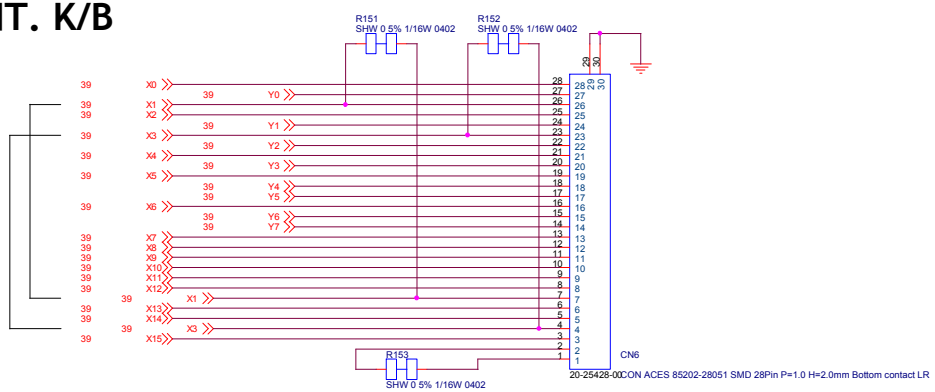
20080625-EMI SOLUTION

HDD I/F





INT. K/B



20061116A-InnovACE K/B SPEC.

PIN 3 & PIN 22 SHORT
PIN 6 & PIN 25 SHORT
PIN 27, 28 SHORT --- US & UK
PIN 27, 28 OPEN --- JP

20061124A-Follow ME PIN-1

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Title: CW0A0

Size: C | Document Number: HDD / DOM | Rev: 0.1

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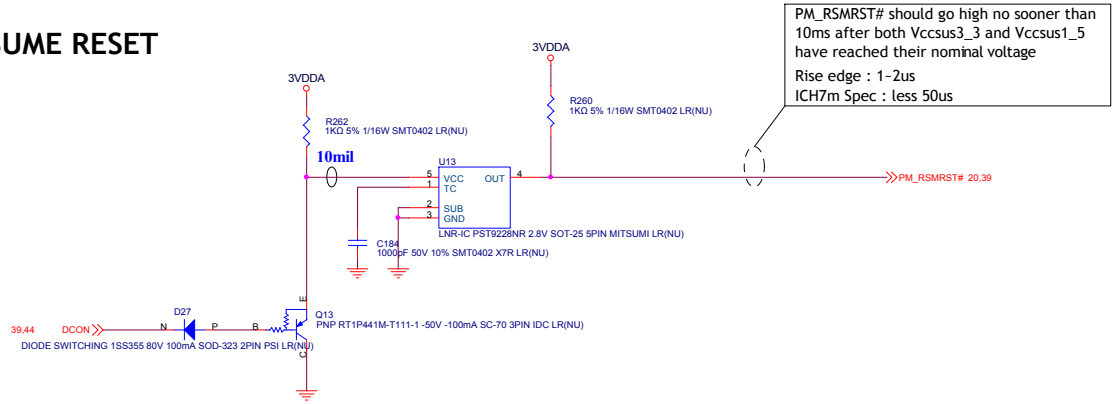
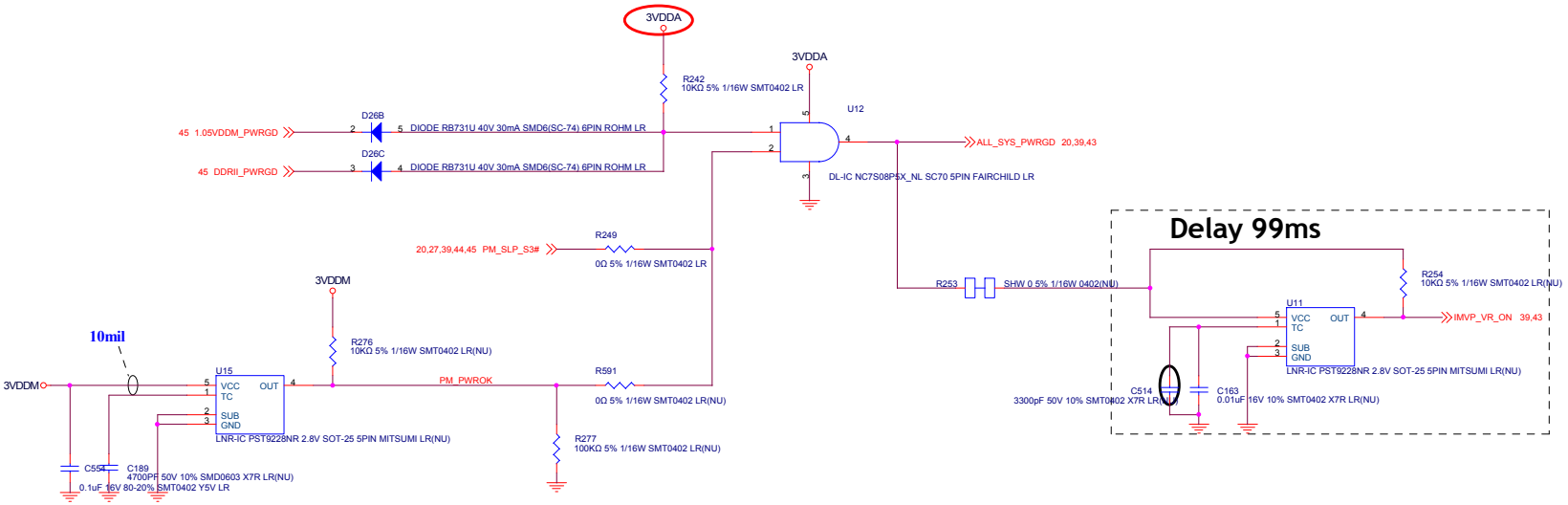
RESUME RESET



NAPA Platfoem Power Good Circuit



Confidential

10,18,20,21,23,26,27,28,29,35,36,38,39,41,44,45 3VDDA — 3VDDA

10,12,13,14,16,17,18,19,20,21,22,23,24,27,28,29,31,32,33,36,38,39,43,44 3VDDM — 3VDDM

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Title: CW0A0

Size	Document Number	Rev
C	Reset Circuit	0.1

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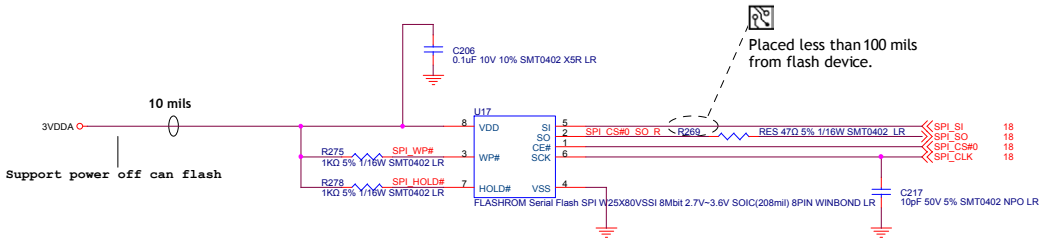
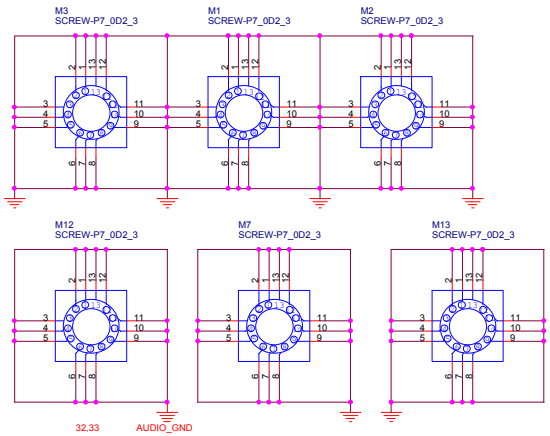
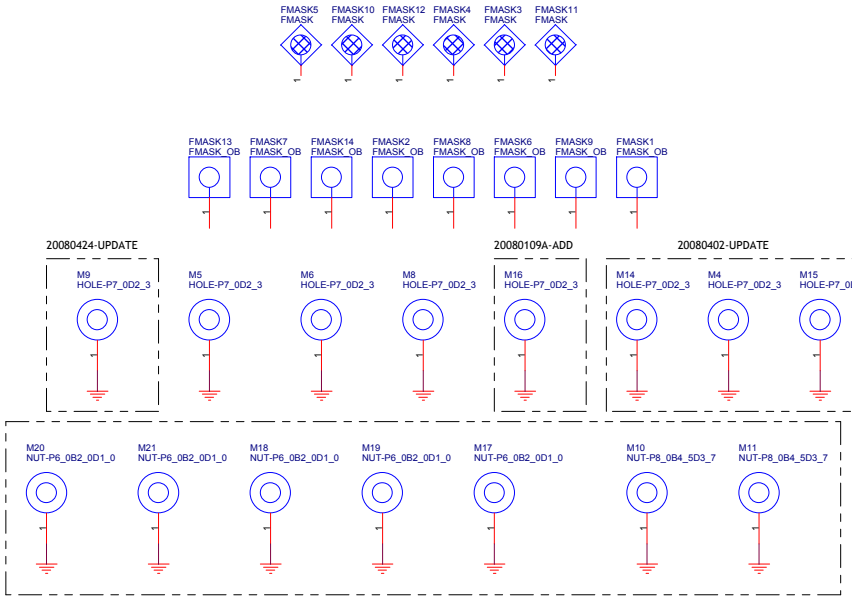
SPI Interface



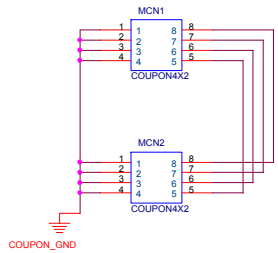


20061125A-CHANGE SCREW TYPE.

20061110A-DON'T ADD SCREW FOR HDD.



COUPON 4X2



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Title: CW0A0

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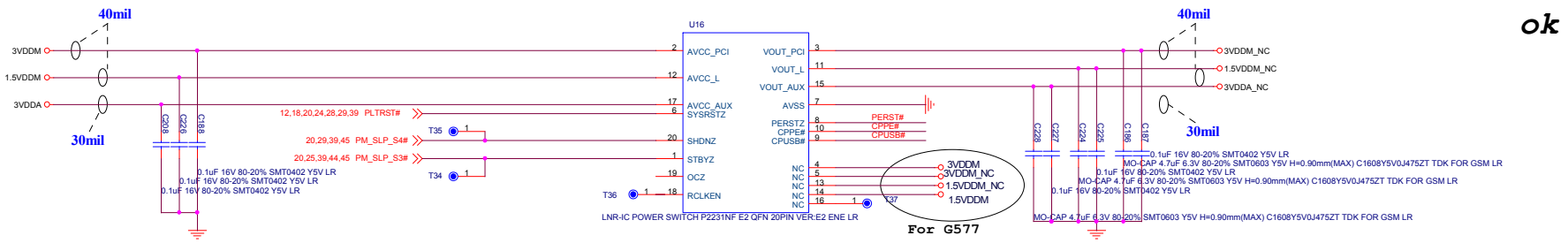
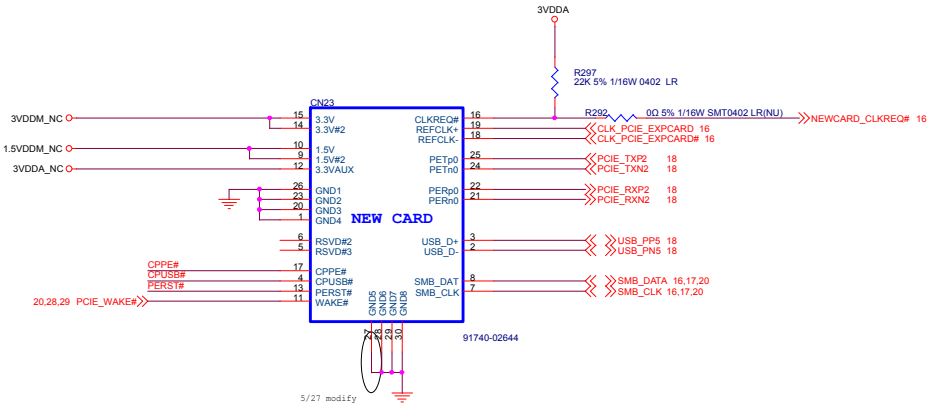
New Card(express card)



ok



9,12,13,14,18,21,28,45 1.5VDDM — 1.5VDDM

10,12,13,14,16,17,18,19,20,21,22,23,24,25,28,29,31,32,33,36,38,39,43,44 3VDDM — 3VDDM

10,18,20,21,23,25,26,28,29,35,36,38,39,41,44,45 3VDDA — 3VDDA

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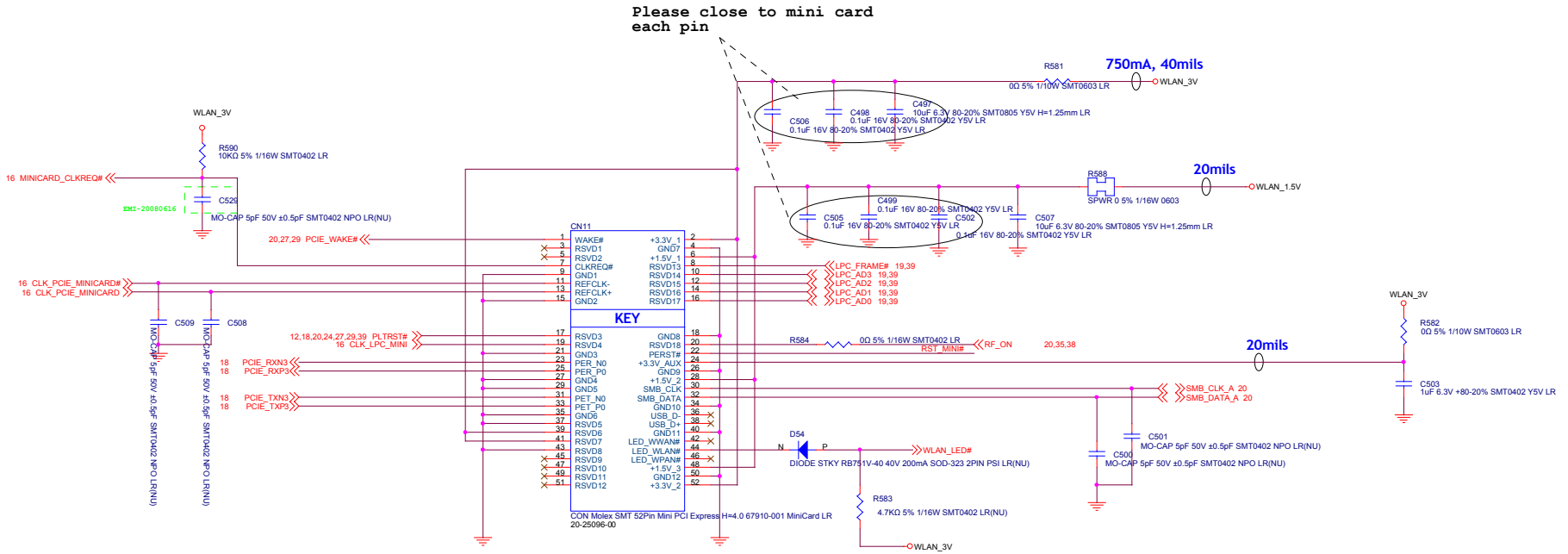
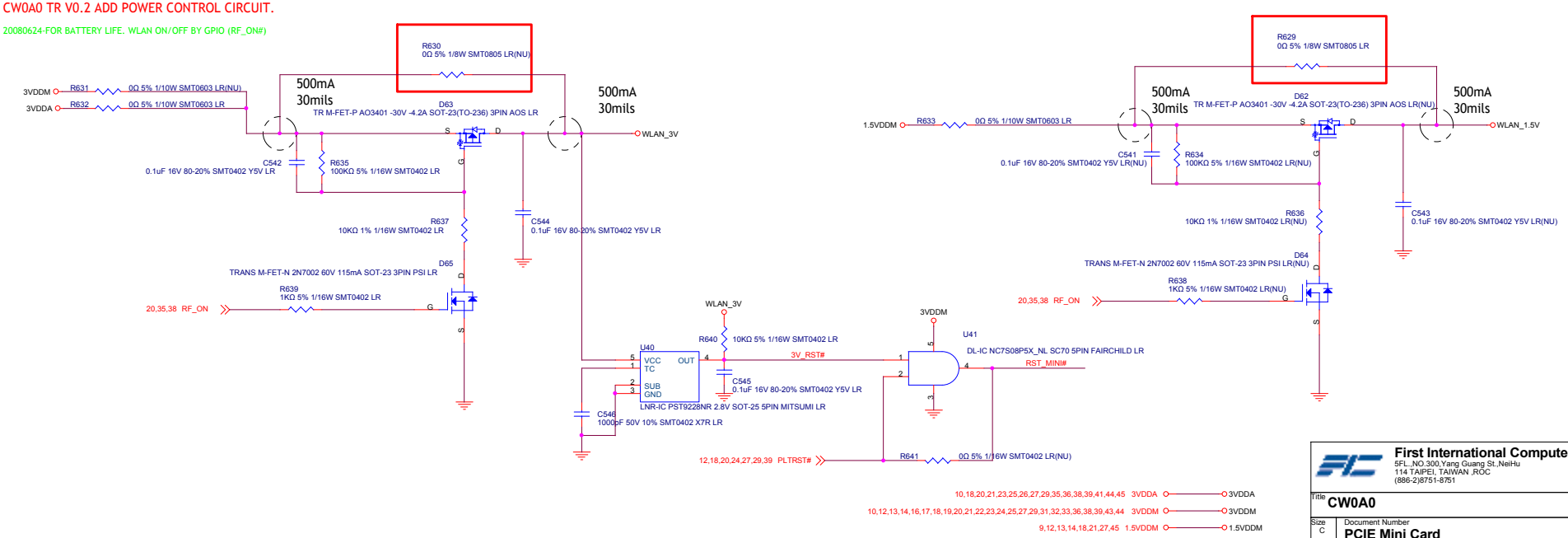
Title	CW0A0	
Size C	Document Number New Card	Rev 0.1
Date: Thursday, June 26, 2008	Sheet 27 of 47	

PCIE Mini Card for Wireless Lan



CW0A0 TR V0.2 ADD POWER CONTROL CIRCUIT.

20080624-FOR BATTERY LIFE, WLAN ON/OFF BY GPIO (RF_ON#)



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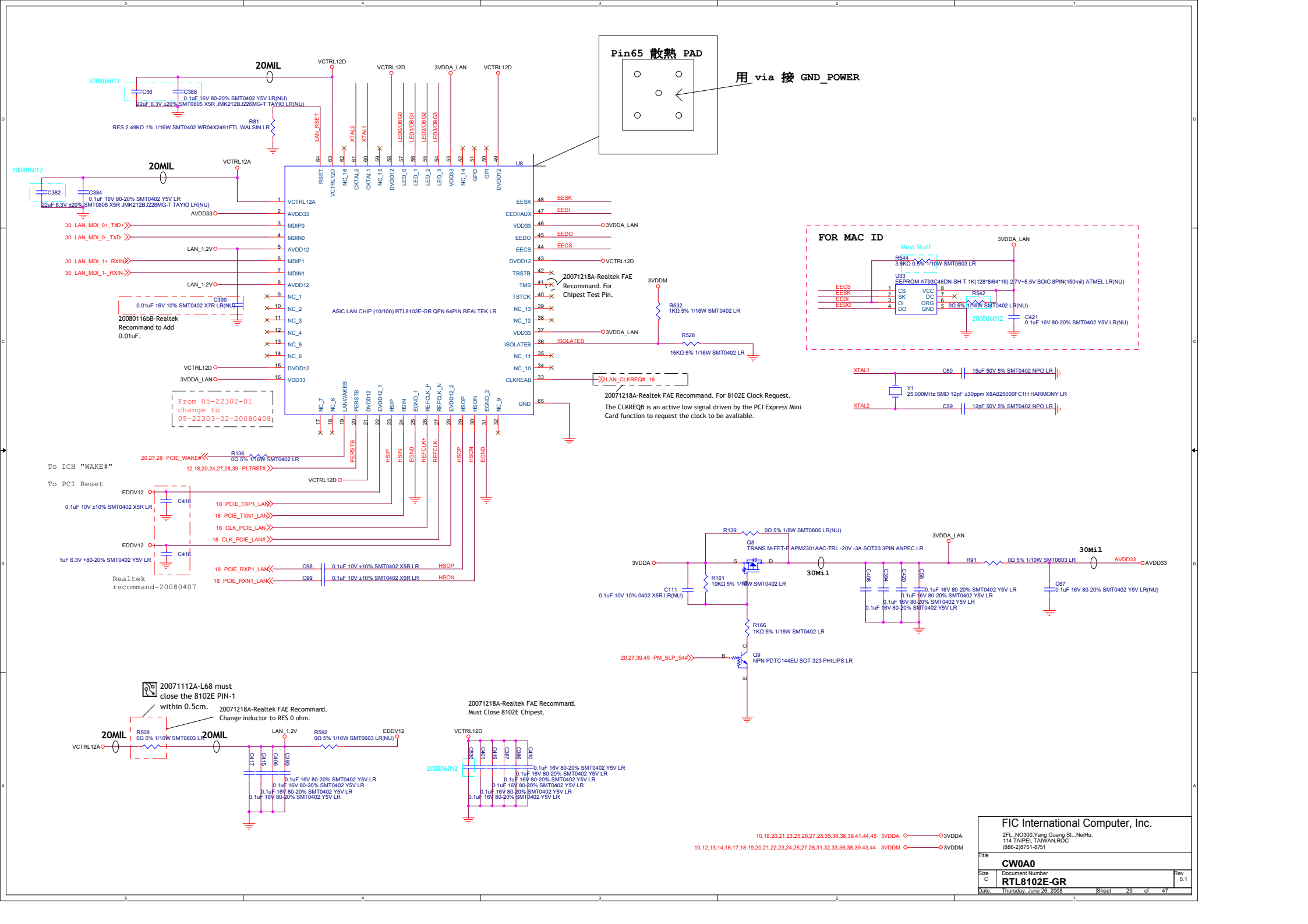
Title: CW0A0

Size	Document Number	Rev
C	PCIE Mini Card	0.2

Date: Thursday, June 26, 2008 Sheet 28 of 47


Pin65 散熱 PAD
用 via 接 GND_POWER
ASIC LAN CHIP (10/100) RTL8102E-GR QFN 64PIN REALTEK LR
20071218A-Realtek FAE Recommand. For Chipest Test Pin.
20080116bB-Realtek Recommand to Add 0.01uF.
From 05-22302-01 change to 05-22303-02-20080408
20071218A-Realtek FAE Recommand. For 8102E Clock Request.
The CLKREQB is an active low signal driven by the PCI Express Mini Card function to request the clock to be avaliable.
FOR MAC ID
Must Stuff
To ICH "WAKE#"
To PCI Reset
Realtek recommand-20080407
20071112A-L68 must close the 8102E PIN-1 within 0.5cm.
20071218A-Realtek FAE Recommand. Change inductor to RES 0 ohm.
20071218A-Realtek FAE Recommand. Must Close 8102E Chipest.
FIC International Computer, Inc.
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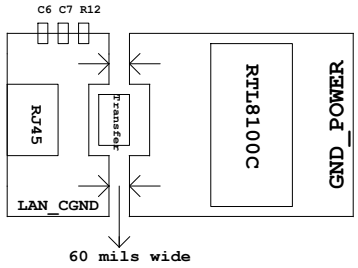
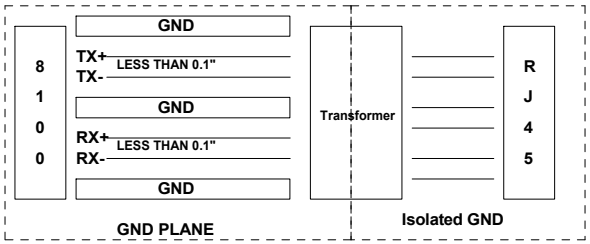
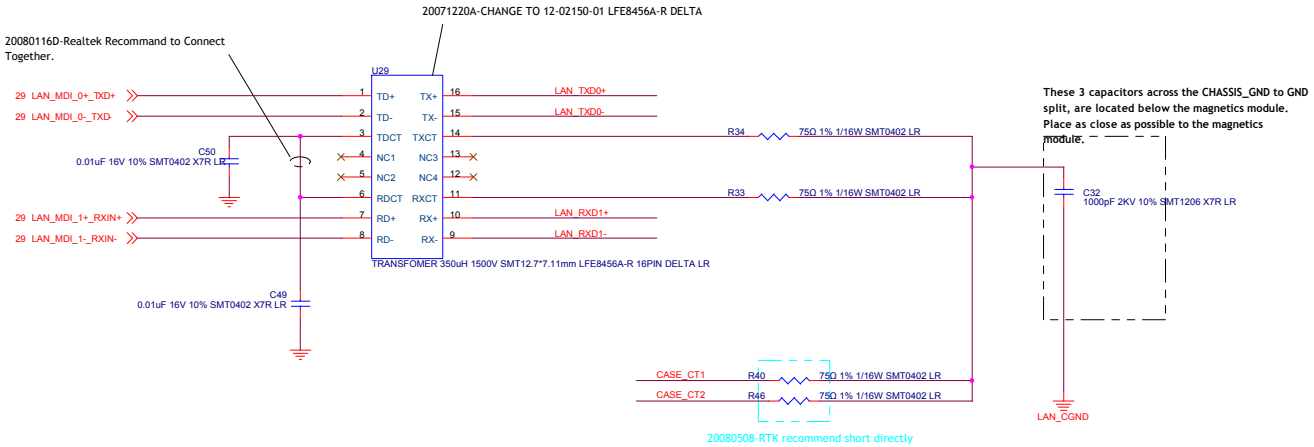
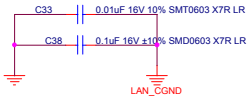
CW0A0
RTL8102E-GR
Thursday, June 26, 2008









Layout Guide

1.The Lan Chip should be placed as close as possible to the transfer.

2. The resistor connected to RSET pin should be placed near to the Lan Chip,and away from signal traces(ex:MDI0+/-) and clock signals as far as possible.

3. The transfer should be placed as close as possible to the RJ45 connector.

4. The crystal should be placed far away from I/O ports and high frequency signal.

5. The termination resistors and capacitors should be placed closely to the Lan Chip.

6. The decoupling capacitors should be placed as close as posslble to the power pins,such that the distance from IC power pin to the capacitor is within 200mils.

7. Traces routed from the Lan Chip to the transfer,and to the RJ45 connector should be as short as possible.

8. The 10-12cm maximum lenghth between Lan Chip and transfer is achievable only when there's no interferences around.

9. All 4 pairs of the differential resister(49.9k) must close to Lan Chip,and make them(4pairs) as same as distant.

10.PLACE GND PLANE AS LARGE AS POSSIBLE

11.If power pins are next to each other and there is not much room to accommodate multipe capacitors,then the power pins can share the same capacitors.

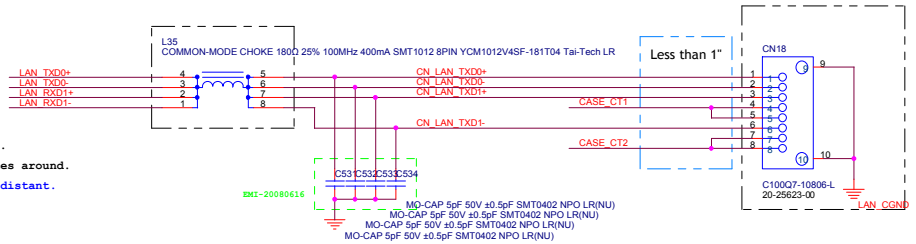
12.It's important to separate digital signals from analog signals.If it is unavoidable to cross digtal signals with analong power do it at 90 degree angle.

13. The digital power plane should be separated from analog areas.

14. All analog decoupling capacitors should be placed as close to the IC as possible and the traces should be short.

15.The Lan Chip pin 1 facing the transformer,then you can make the signal shorter.

LAN RJ45 JACK



Layout Guide

1. In addition,it is also important to keep the gap between Chassis GND and System GND to be wider than 60mils for better Isolation requirement.

2.The analog GND pins must maintain agood ground return path.

3. All 4 pairs trace width of 4pair is 4mil.It's 10mil between 2 trace(+/-),It's morethan 50mil spacing different differential pairs.

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Title	CW0A0	
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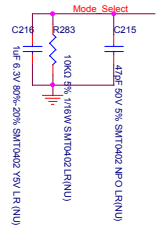
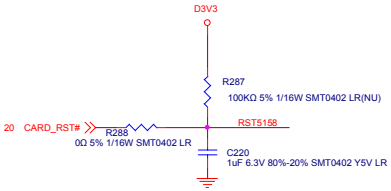
Mode Select



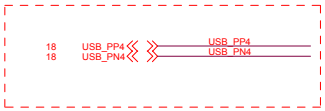
R614/C655 == 10 K/ 47p F ==>> R599 ON

R614/C655 == NC/NC ==>> R607 ON

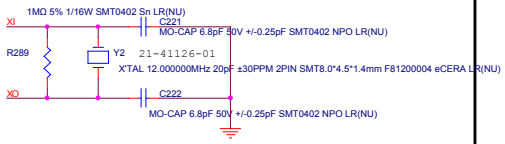
RESET



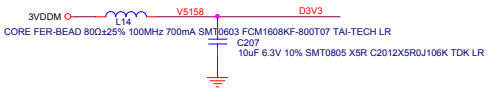
INTERFACE

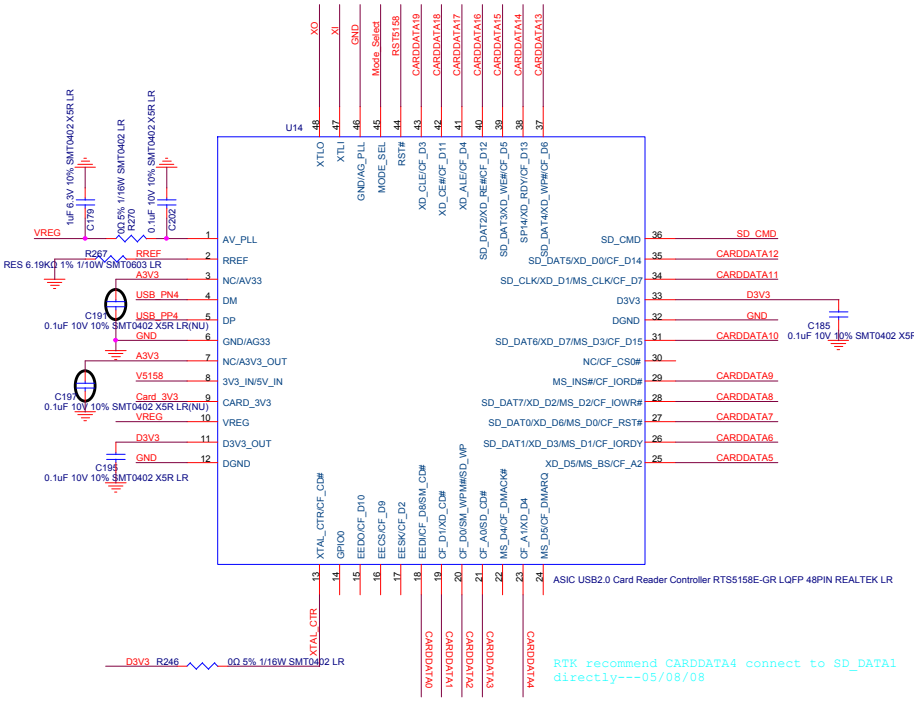


X'TAL

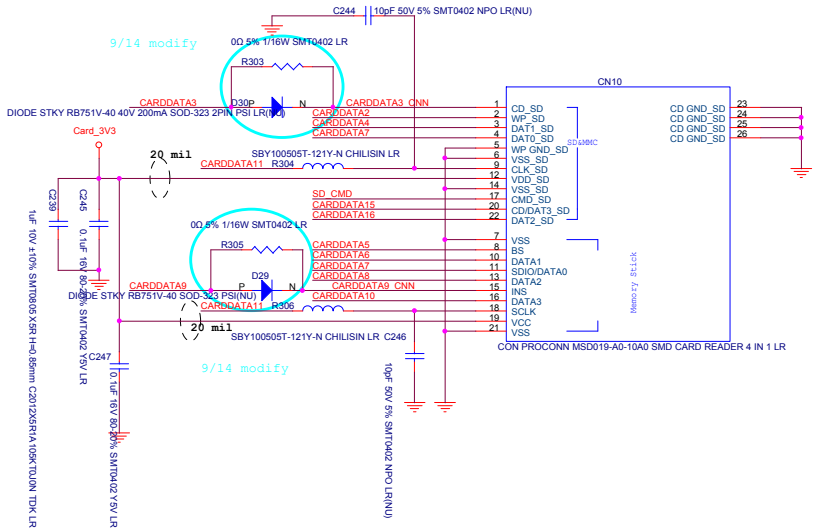


POWER





RTK recommend CARDDATA4 connect to SD_DATA1 directly---05/08/08



10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,32,33,36,38,39,43,44 3VDDM — 3VDDM

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Title: CW0A0

Size: C | Document Number: Cardreader AU6371 | Rev: 0.1

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10mil GND_POWER
10mil 10mil 14MCLK_AC97
10mil 10mil

AC97/HDA CODEC DUALLAYOUT

AC97 USE VIA VT1708

A_GND 10mil
LINE_OUT_L 10mil
A_GND 10mil
LINE_OUT_R 10mil
A_GND 10mil

HD Audio-ACZ_SDOUT/ACZ_SYNC/ACZ_BITCLK/ACZ_RESET#

ICH7m — L1 — L2 — 39ohm — L3 — HD Audio
ICH7m — L1 — L2 — 39ohm — L3 — MDC CONN

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.5"-2.5" L2 <= 0.1" L3 = 1"-8"

*** L3 can be extened up to 15" if HD Audio docking is not used

HD Audio-ACZ_SDIN

ICH7m — L1 — 39ohm — L2 — HD Audio

Trace Impedance	Routing Requirement	Trace Length
55 +/- 15%	4 on 7(stripline) 5 on 7(microstrip)	L1 = 0.1"-15" L2 <= 0.5"

*** Breakout can be routed 4 on 4 up to 500 mils

60 mils R340 60 mils
SPWR 0 5% 1/16W 0603
26,33 AUDIO_GND
GND_POWER
AUDIO_GND

Place next to pin27
Please close to CODEC CHIP
Close to Chip
For CW0A1
Realtek recommand
Analog
Digital
ASIC AUDIO CODEC ALC269Q-GR QFN 48PIN REALTEK LR
L Mute Enable
DIODE SWITCHING 1SS355 80V 100mA SOD-323 2PIN PSI LR(NU)
DL-IC NC7SZ32P5X_NL SC-70 5PIN FAIRCHILD LR

CODEC POWER:

AVDD1	5V or 3.3V	Analog power for mixer and amplifer
AVDD2	5V or 3.3V	Analog power for DACs and ADCs
DVDD	3.3V	Digital core power for core logic
DVDD I/O	3.3V or 1.5V	Digital I/O power for HDA link.
PVDD1	5V	Power supply for full-bridge left channel
PVDD2	5V	Power supply for full-bridge right channel

3VDDM_AUDIO 3VDDM_AUDIO
33 AVDDS AVDDS
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,33,36,38,39, 43,44 3VDDM 3VDDM

CODEC POWER

Please close to CODEC CHIP
3VDDM L16 20 mils 3VDDM_AUDIO 3VDDM_AUDIO
600Ω±25% 100MHz 1000mA SMT0603 HCB1608KF-601T10 TA I-TECH LR
C236 C240 0.1uF 16V 80-20% SMT0402 Y5V L R
10uF 10V +80-20% SMT0805 Y5V LR

Please close to CODEC CHIP
10,21,22,23,24,36,37,43,44 ,45 5VDDM L18 600Ω±25% 100MHz 2000mA SMT0805 HCB2012KF-601T20 T AI-TECH LR
5VDDM_AUDIO 5VDDM_AUDIO
C253 10uF 10V ±10% SMT0805 X5R TDK LR
C267 0.1uF 10V 10% SMT0402 X5R LR
R316 SPWR 0 5% 1/16W 060 3

10,21,22,23,24,36,37,43,44 ,45 5VDDM (20mil)
U23 LNR-IC LDD G924-475T1U 4.75V SOT23-5 5PIN GMT
CONTROL Vin GND NB VOUT
200mA
AVDDS 33
(40mil)
C276 0.1uF 16V 80-20% SMT0402 Y5V LR
C266 1000pF 50V 10% SMT040 2 X7R LR
C257 0.1uF 16V 80-20% 0402 Y5V Lead-Free
05-31717-01
C271 10uF 10V ±10% SMT0805 X5R A VXTV21X5R106K10AT AVX LR
AUDIO_GND 26,33

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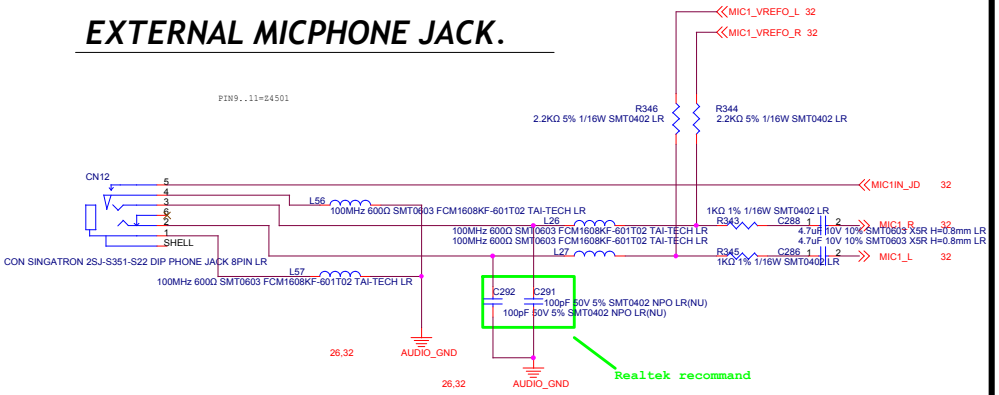
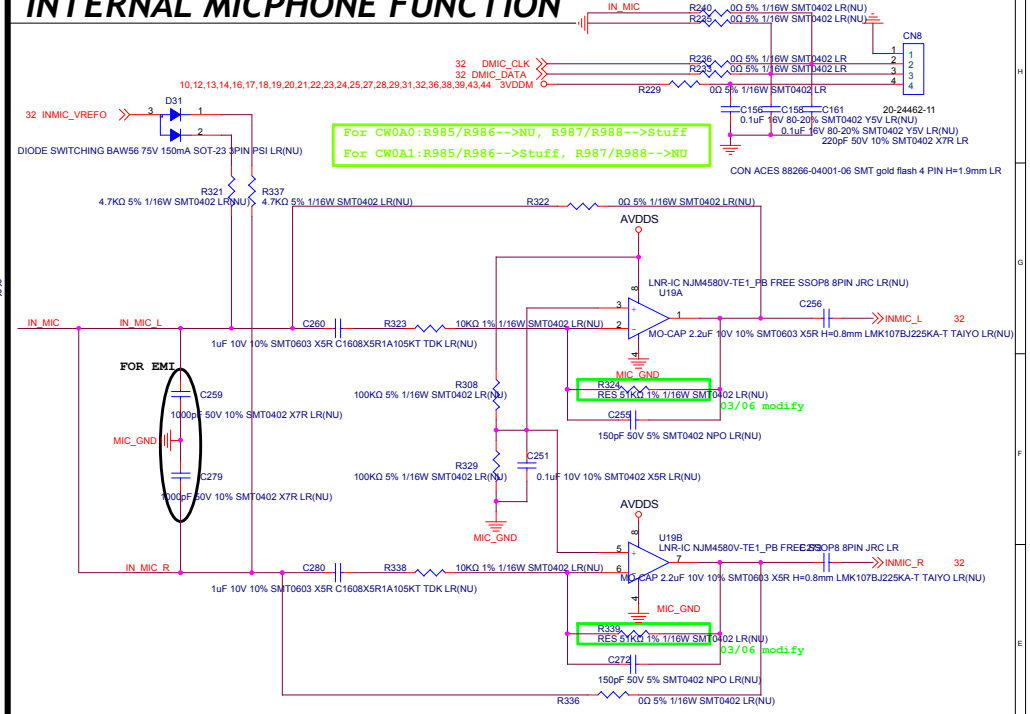
EXTERNAL MICPHONE JACK.



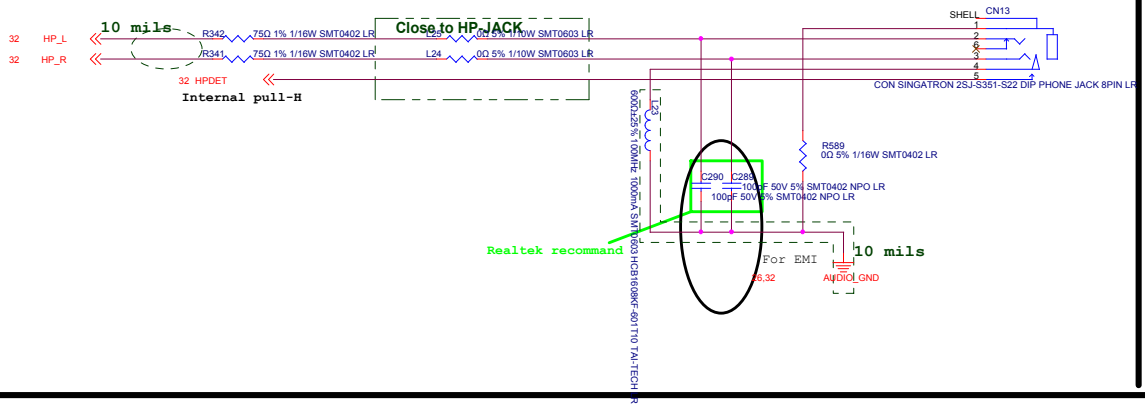
NOTE

MIC1IN,MIC2IN,INTERNAL_MIC
請包AGROUND

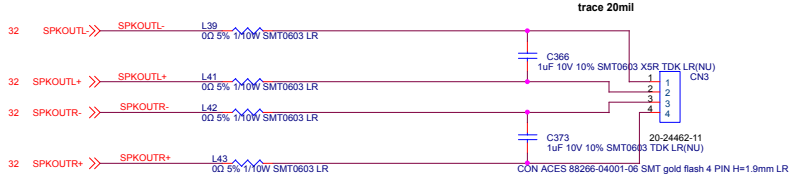
INTERNAL MICPHONE FUNCTION

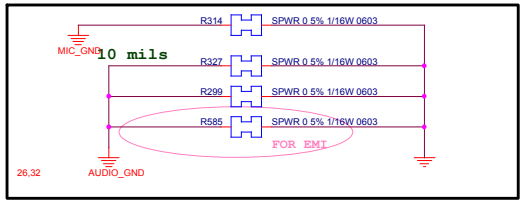


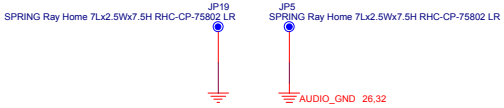
EXTERNAL HEADPHONE JACK.



INTERNAL SPEAKER JACK.







32 3VDDM_AUDIO — 3VDDM_AUDIO
32 AVDDS — AVDDS
10,21,22,23,24,32,36,37,43,44,45 5VDDM — 5VDDM

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C	HP OUT & MIC IN	0.1

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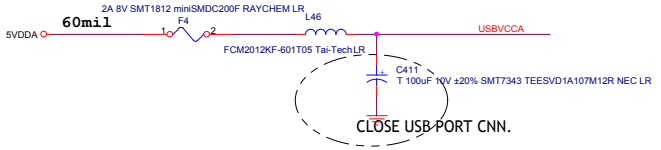
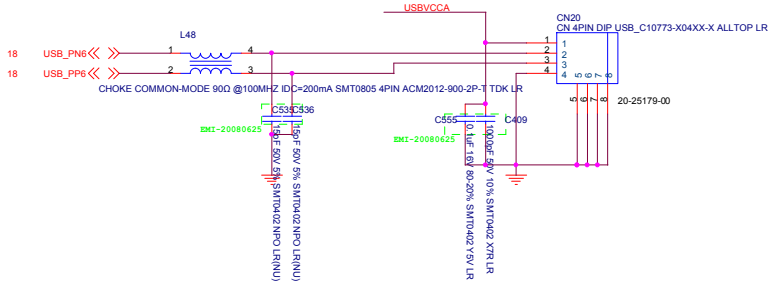
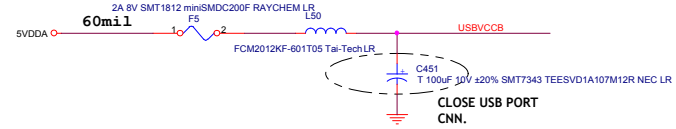
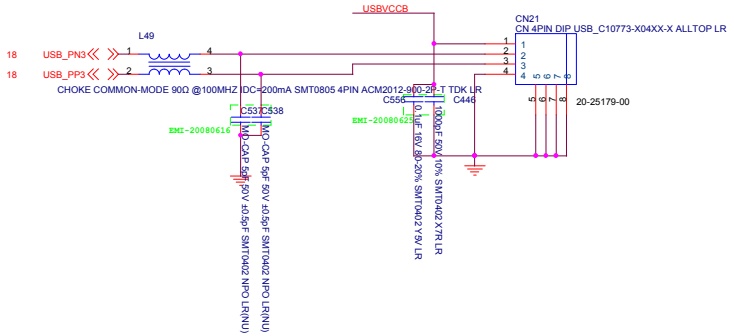
NC FOR 8.9" PANEL

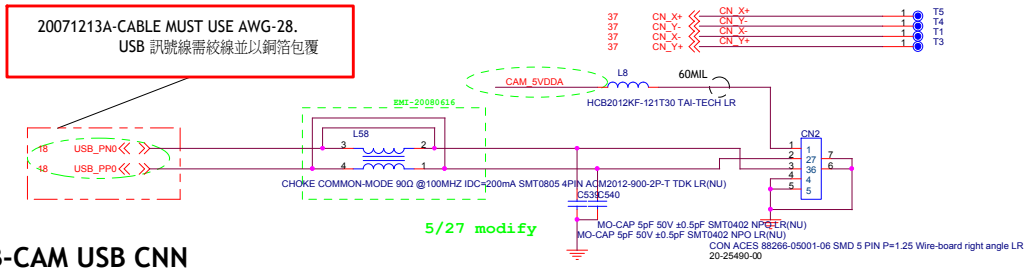






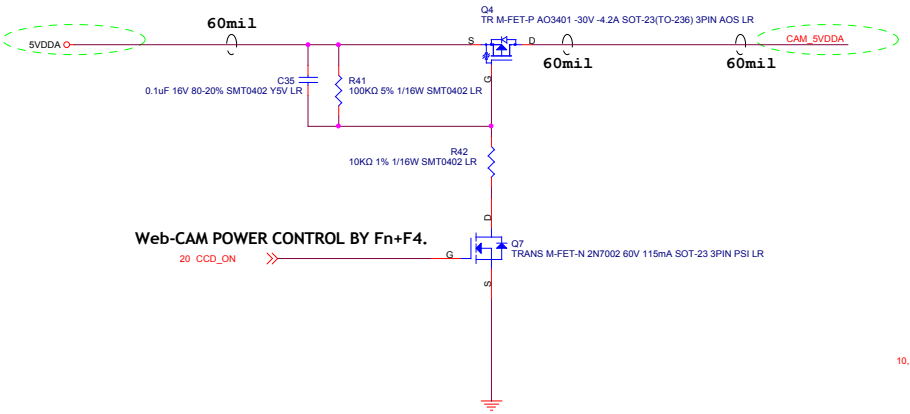


20071213A-CABLE MUST USE AWG-28.
USB 訊號線需絞線並以銅箔包覆



5/27 modify

WEB-CAM USB CNN



10,18,20,21,23,25,26,27,28,29,35,36,38,39,41,44,45 3VDDA → 3VDDA
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39,43,44 3VDDM → 3VDDM
21,24,38,44,45 5VDDA → 5VDDA

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Title: CW0A0
Size: C
Document Number: EXT USB / GPS / WEB-CAM
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NC FOR 8.9" PANEL

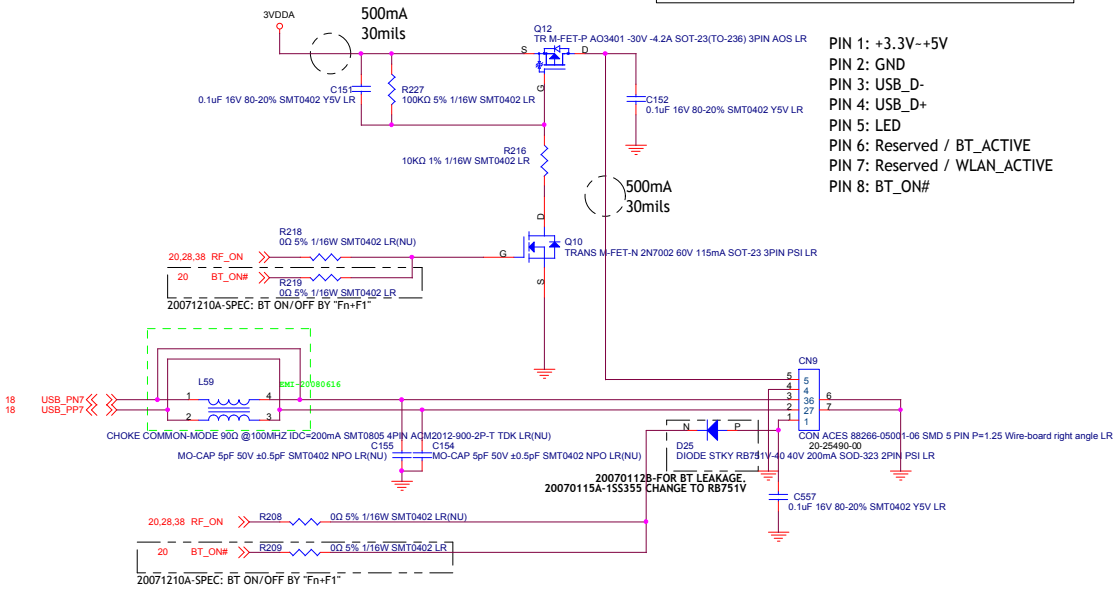
TOUCH SCREEN & MODULE USB/POWER CNN

BLUETOOTH CNN

20070129A-ADD, SPEC CHANGE. NEED TO TURN OFF PWR WHEN S3.

Billionton Bluetooth Module / GUBTCR42M

Power Consumption
Idle Mode: 40mA
TX Continuous: 63mA
3.3V +/- 5%



PIN 1: +3.3V~+5V
PIN 2: GND
PIN 3: USB_D-
PIN 4: USB_D+
PIN 5: LED
PIN 6: Reserved / BT_ACTIVE
PIN 7: Reserved / WLAN_ACTIVE
PIN 8: BT_ON#

21,24,34,38,44,45 5VDDA — 5VDDA
10,18,20,21,23,25,26,27,28,29,36,38,39,41,44,45 3VDDA — 3VDDA
10,21,22,23,24,32,36,37,43,44,45 5VDDM — 5VDDM
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39,43,44 3VDDM — 3VDDM

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Title: CW0A0

Size	Document Number	Rev
C	BT / Touch Screen Cnn	0.1

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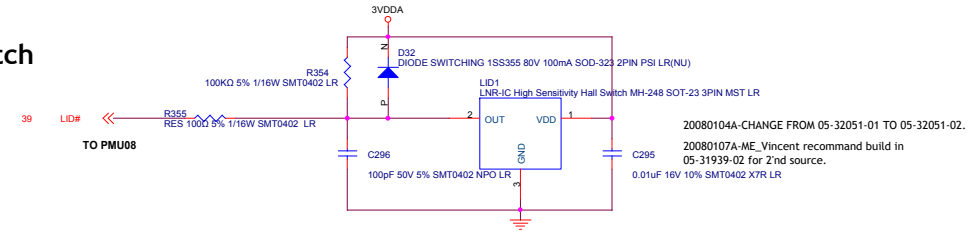
LID Switch

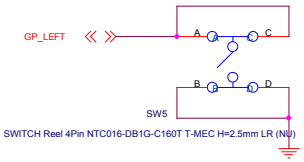


20080104A-CHANGE FROM 05-32051-01 TO 05-32051-02.

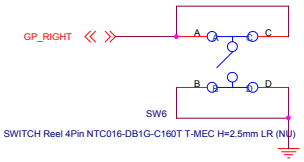
20080107A-ME_Vincent recommand build in 05-31939-02 for 2'nd source.

CW0A1 Micro pad CNN

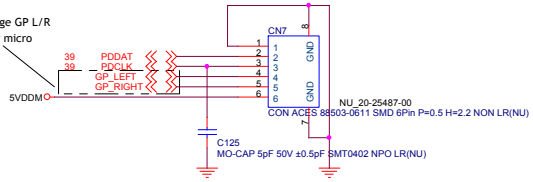
LEFT BUTTON



RIGHT BUTTON

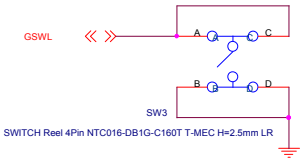


2007_05_08 Change GP L/R button control by micro pad

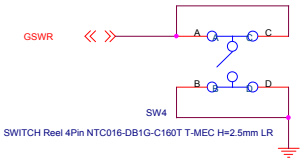


CW0A0 Micro pad CNN

LEFT BUTTON



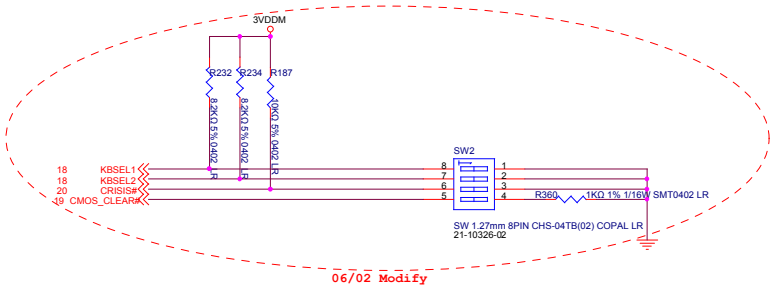
RIGHT BUTTON



Keyboard language DIP SWITCH

KBSEL2	KBSEL1	
ON	ON	UK Keyboard
	OFF	Reserved
OFF		JP Keyboard
OFF	OFF	US Keyboard

CMOS_CLEAR#	ON	Reset RTC
	OFF	NONE
CRISIS#	ON	CRISIS mode
	OFF	Normal



06/02 Modify

24,38,39,44,45 PMU5V — PMU5V
21,24,34,38,44,45 5VDDA — 5VDDA
10,18,20,21,23,25,26,27,28,29,35,38,39,41,44,45 3VDDA — 3VDDA
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,38,39,43,44 3VDDM — 3VDDM
10,21,22,23,24,32,37,43,44,45 5VDDM — 5VDDM

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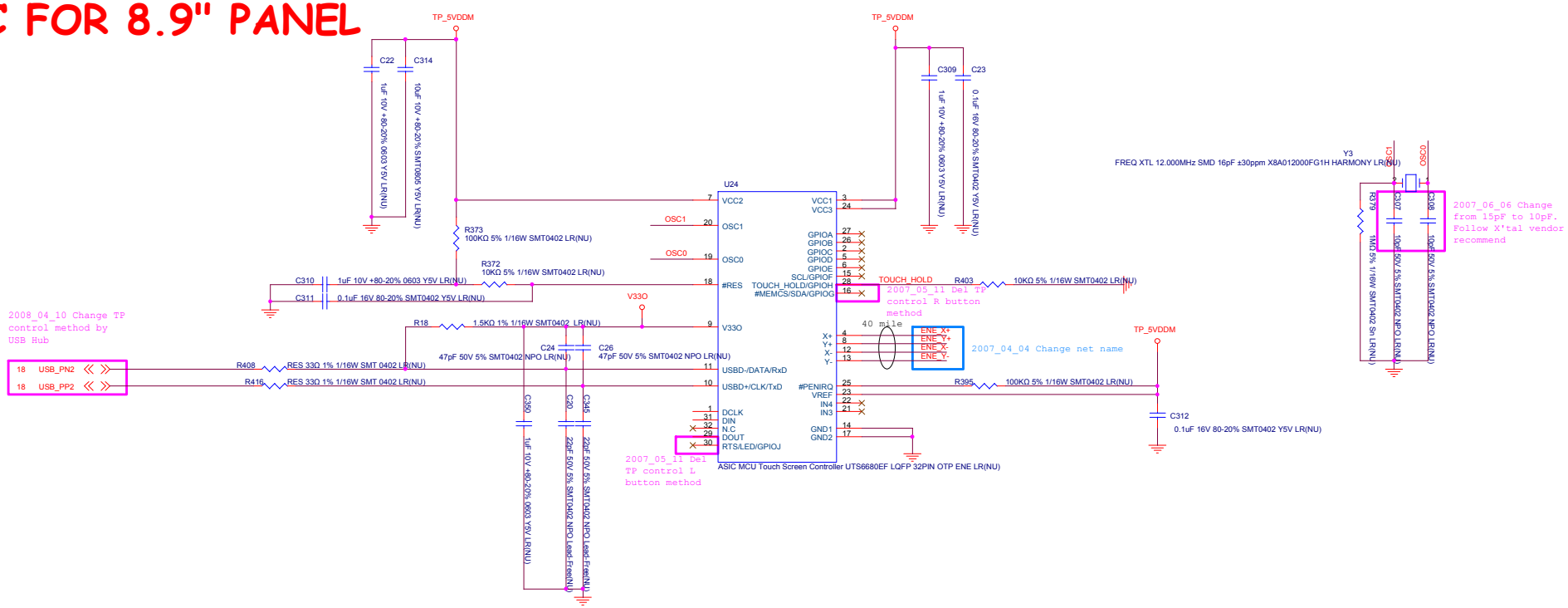
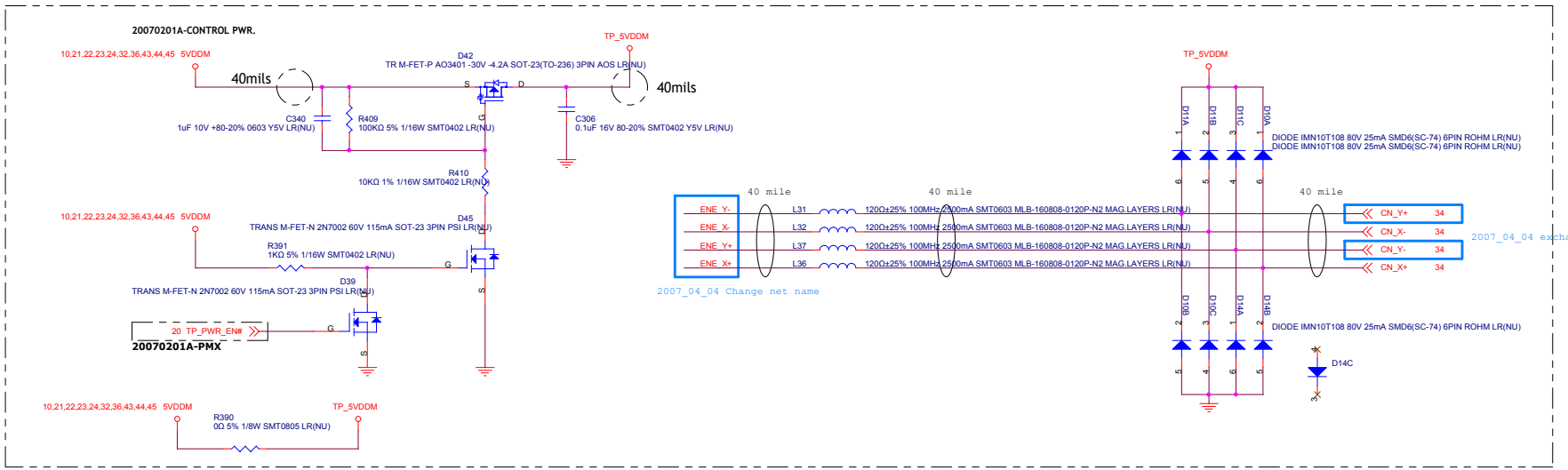
NC FOR 8.9" PANEL



20070328A-RESERVE CE261 V0.1 LOCATION.



10,21,22,23,24,32,36,43,44,45 5VDDM — 5VDDM

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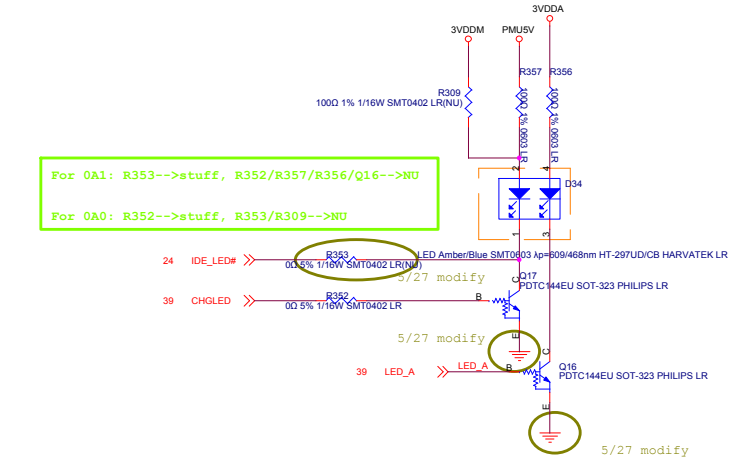
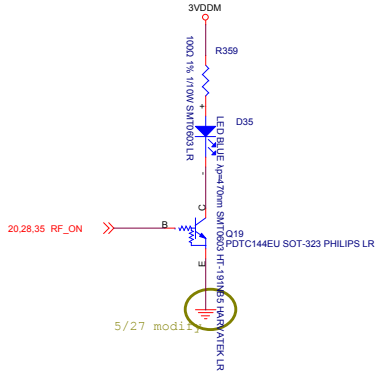
For CW0A0

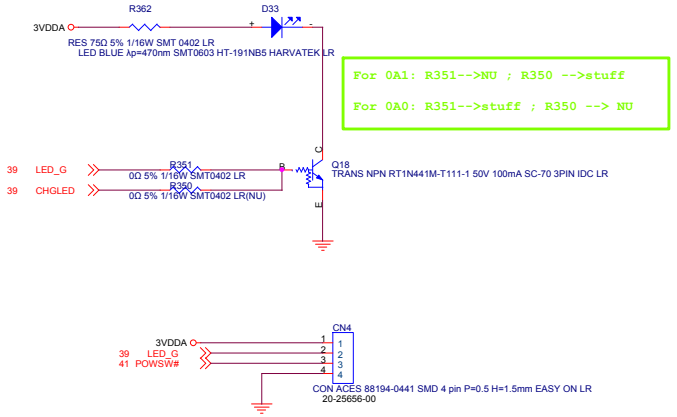
Wireless indicator

0A0:Charger LED 0A1:HDD LED



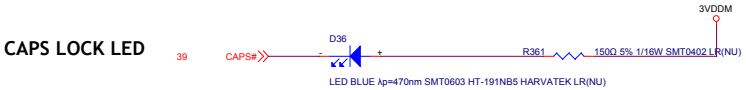


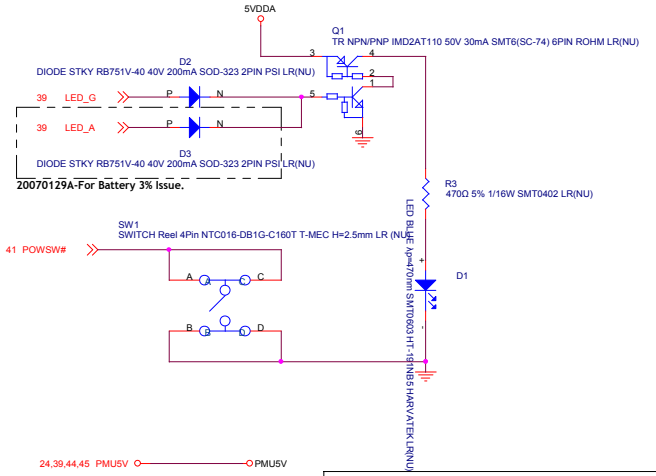
0A0:Power LED 0A1:Charger LED



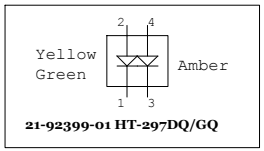
For CW0A1

Power button and LED

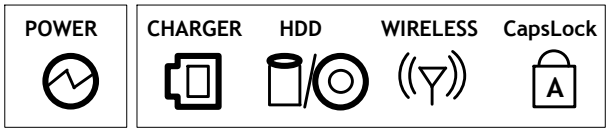




Status Indicator SPEC:
Power On Status.
Battery Status.
RF Status.
HDD / NAND Flash Status.
CAPS Lock.



Battery status indicator by 2 colors LED
-->Charge state: green ;
--> Battery Low State: Amber (8% -> shut down)



24,39,44,45 PMU5V → PMU5V
21,24,34,44,45 5VDDA → 5VDDA
10,18,20,21,23,25,26,27,28,29,35,36,39,41,44,45 3VDDA → 3VDDA
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,39,43,44 3VDDM → 3VDDM

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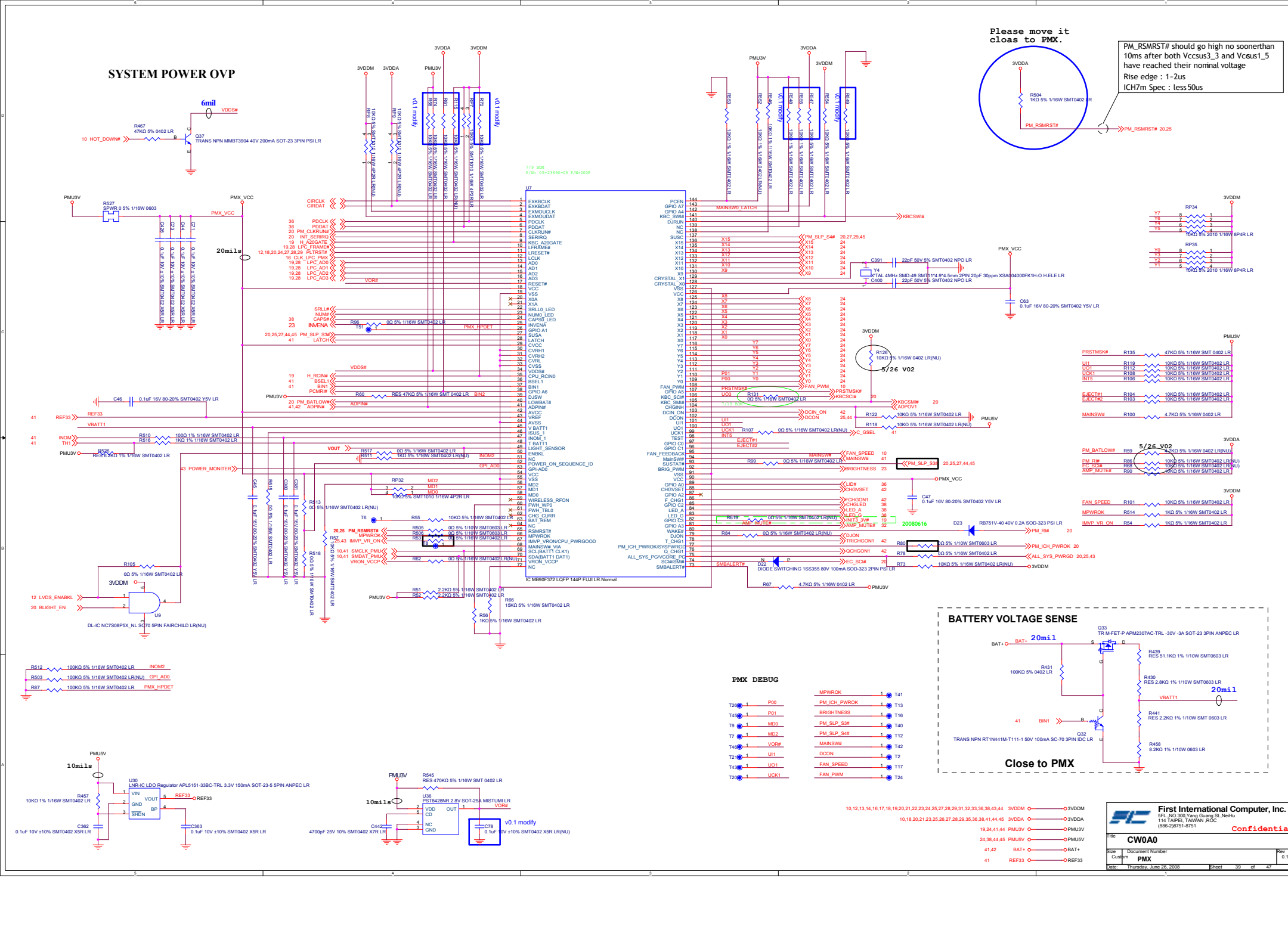
SYSTEM POWER OVP



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Size: Custom	Document Number: PMX	Rev: 0.1
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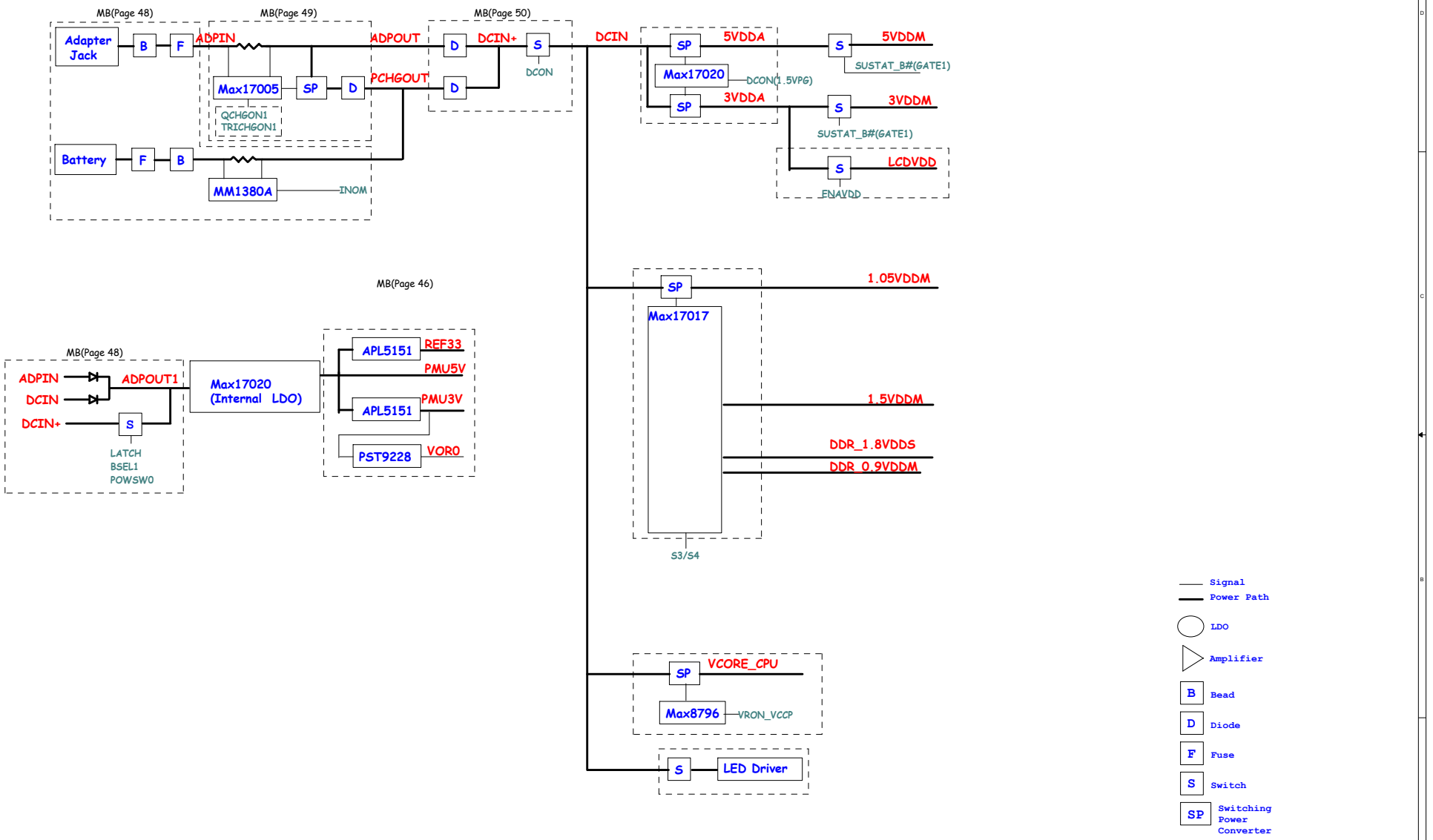
Diamondville Power Block(Maxim solution)



Signal
Power Path
LDO
Amplifier
B Bead
D Diode
F Fuse
S Switch
SP Switching Power Converter

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CW0A0

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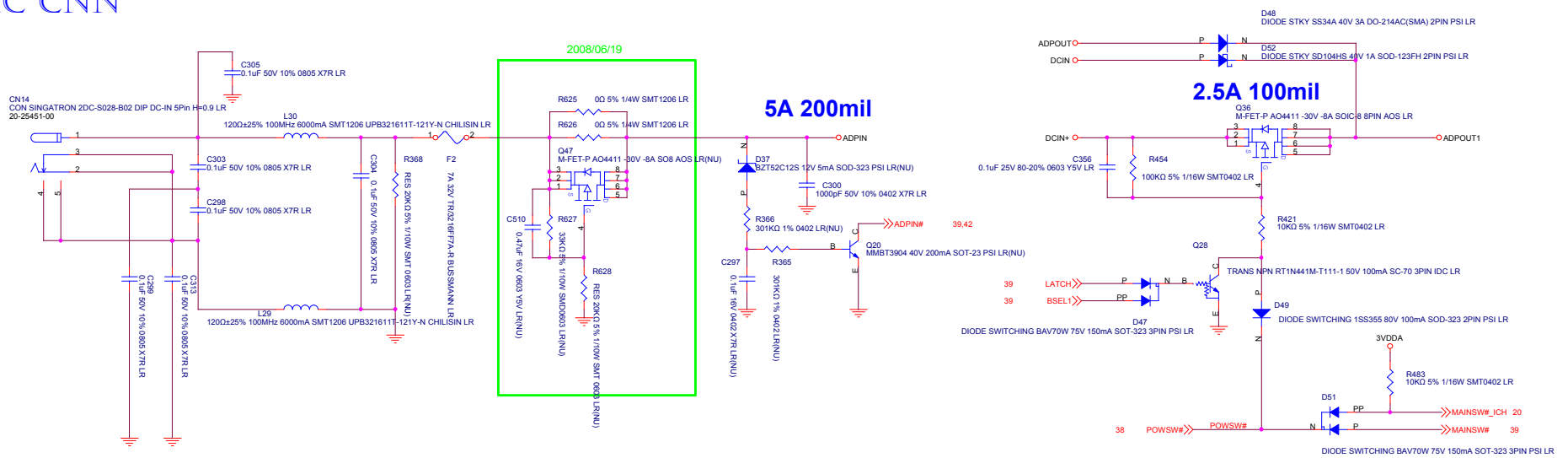
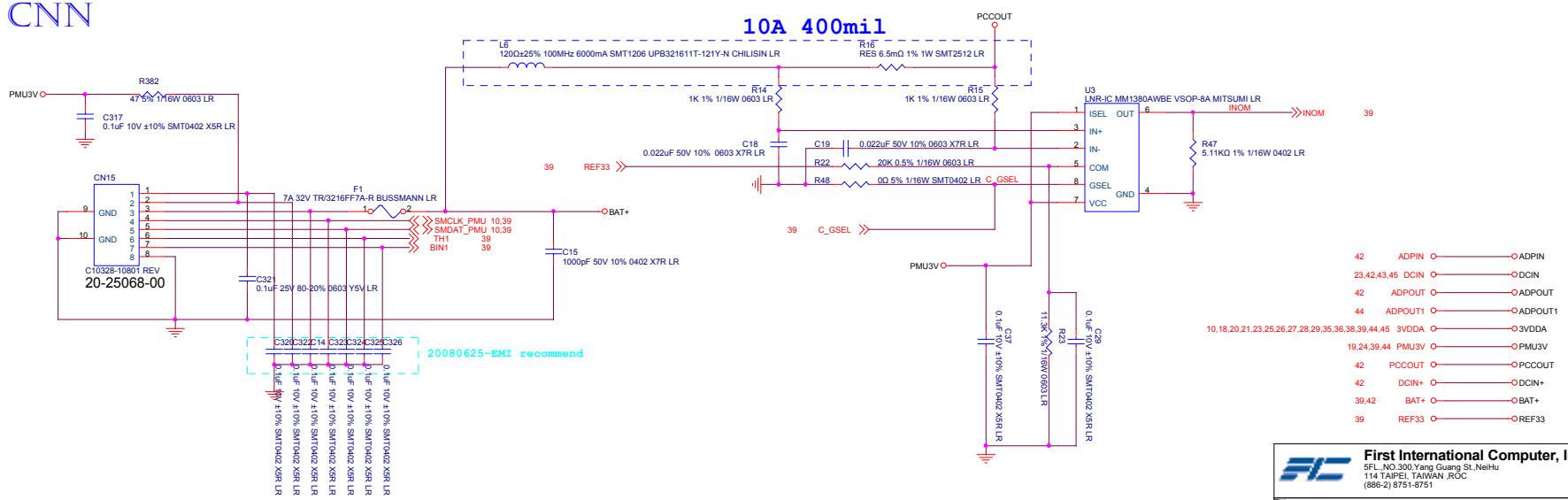
AC CNN



BATT CNN



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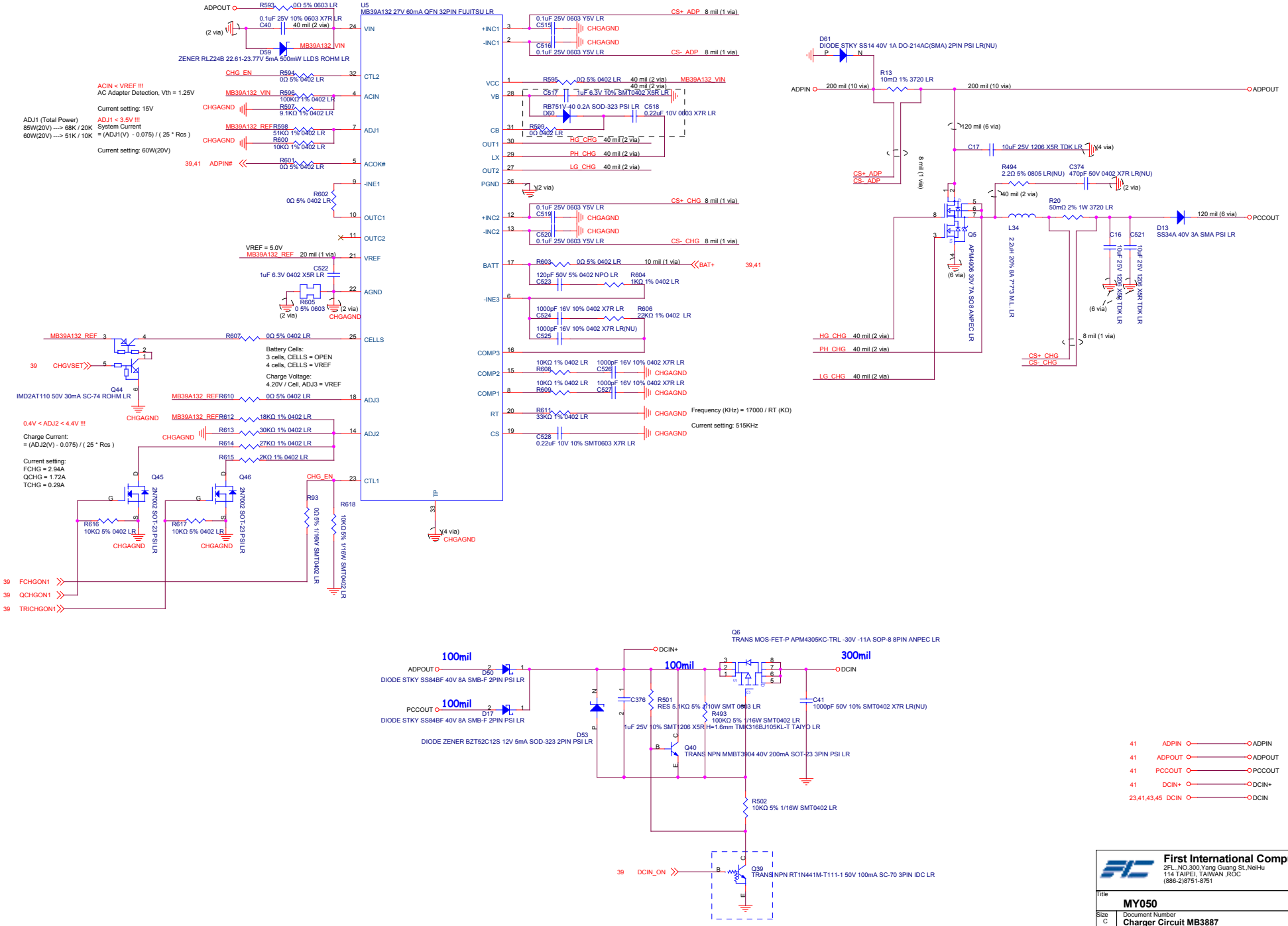
Charger



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Title
MY050

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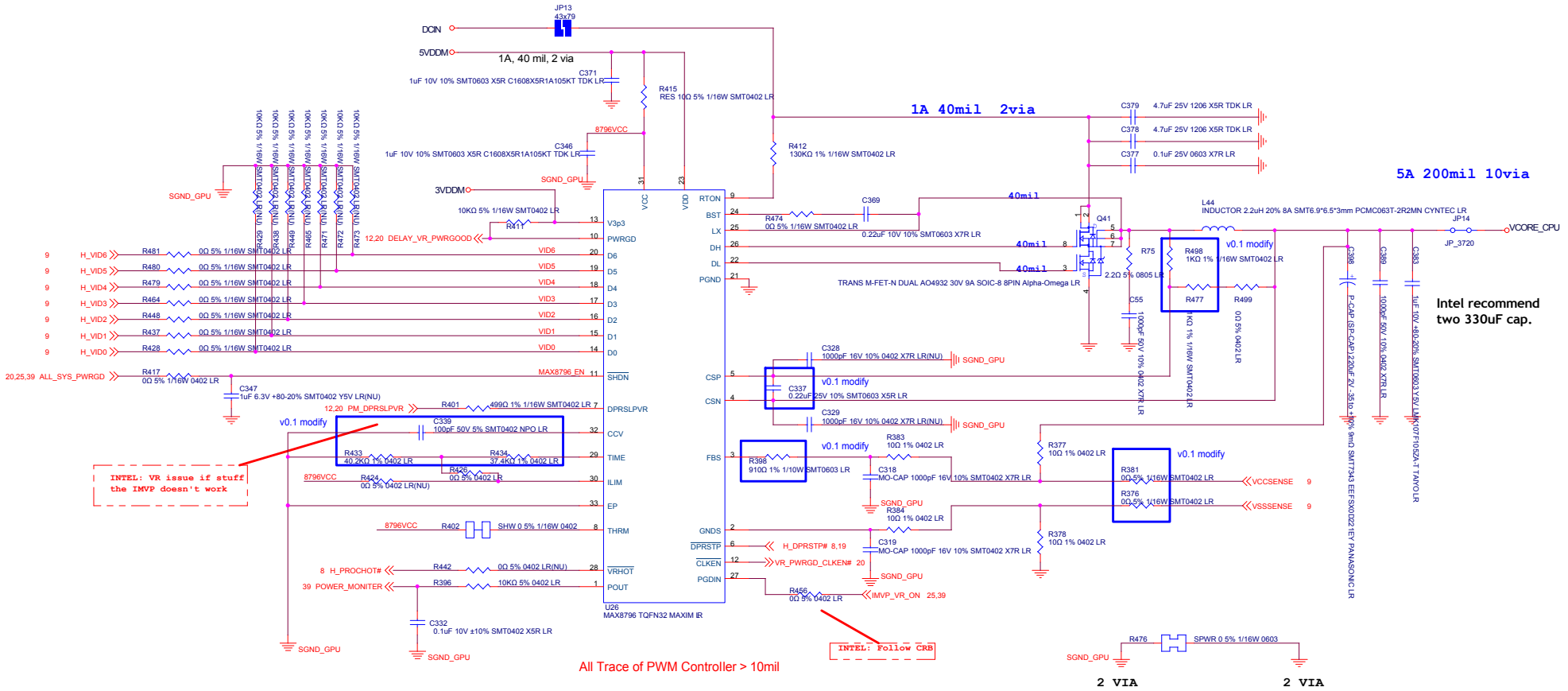

23,41,42,45 DCIN → DCIN
21,24,34,38,44,45 5VDDA → 5VDDA
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39,44 3VDDM → 3VDDM
9 VCORE_CPU → VCORE_CPU
10,21,22,23,24,32,36,37,44,45 5VDDM → 5VDDM

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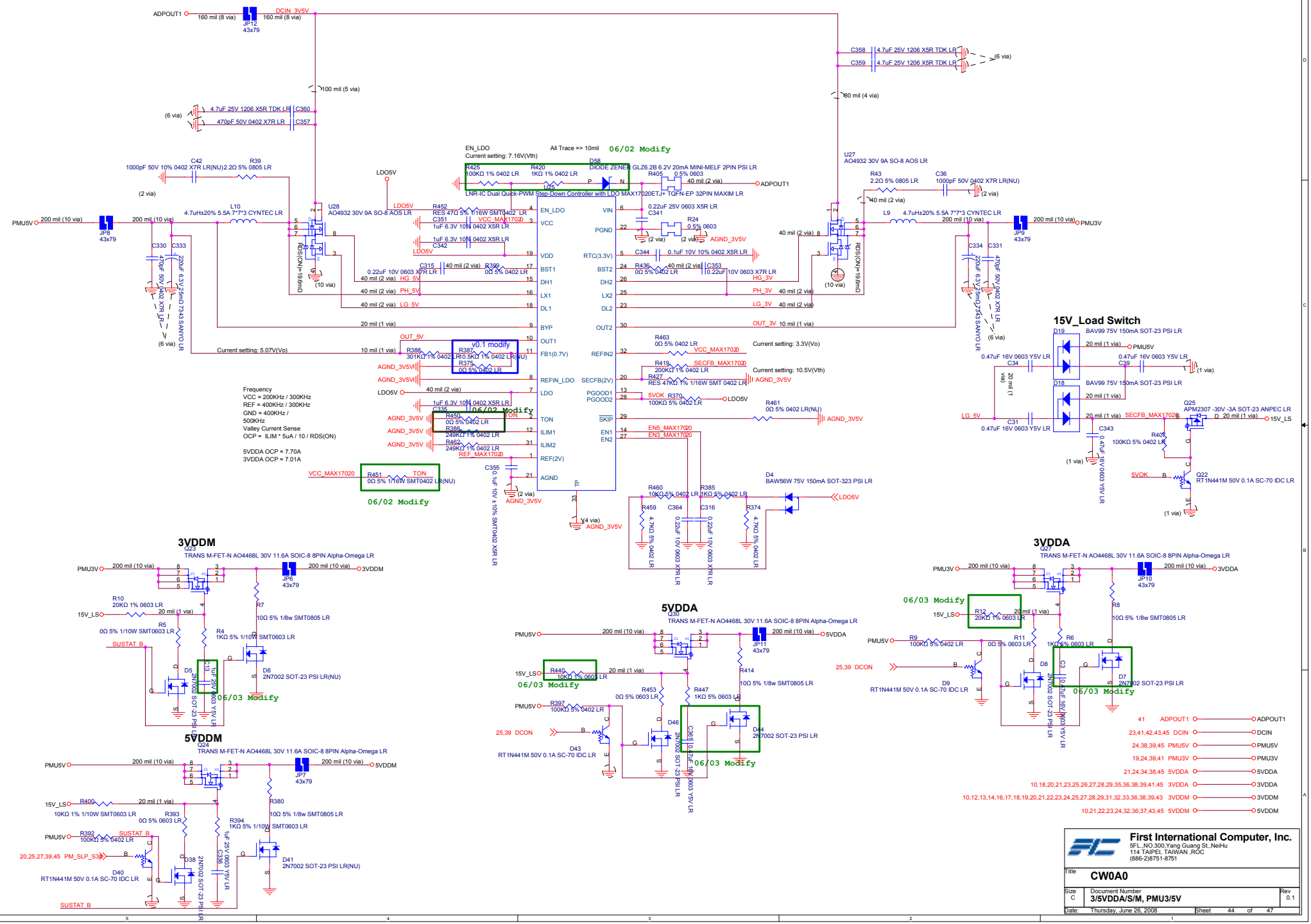
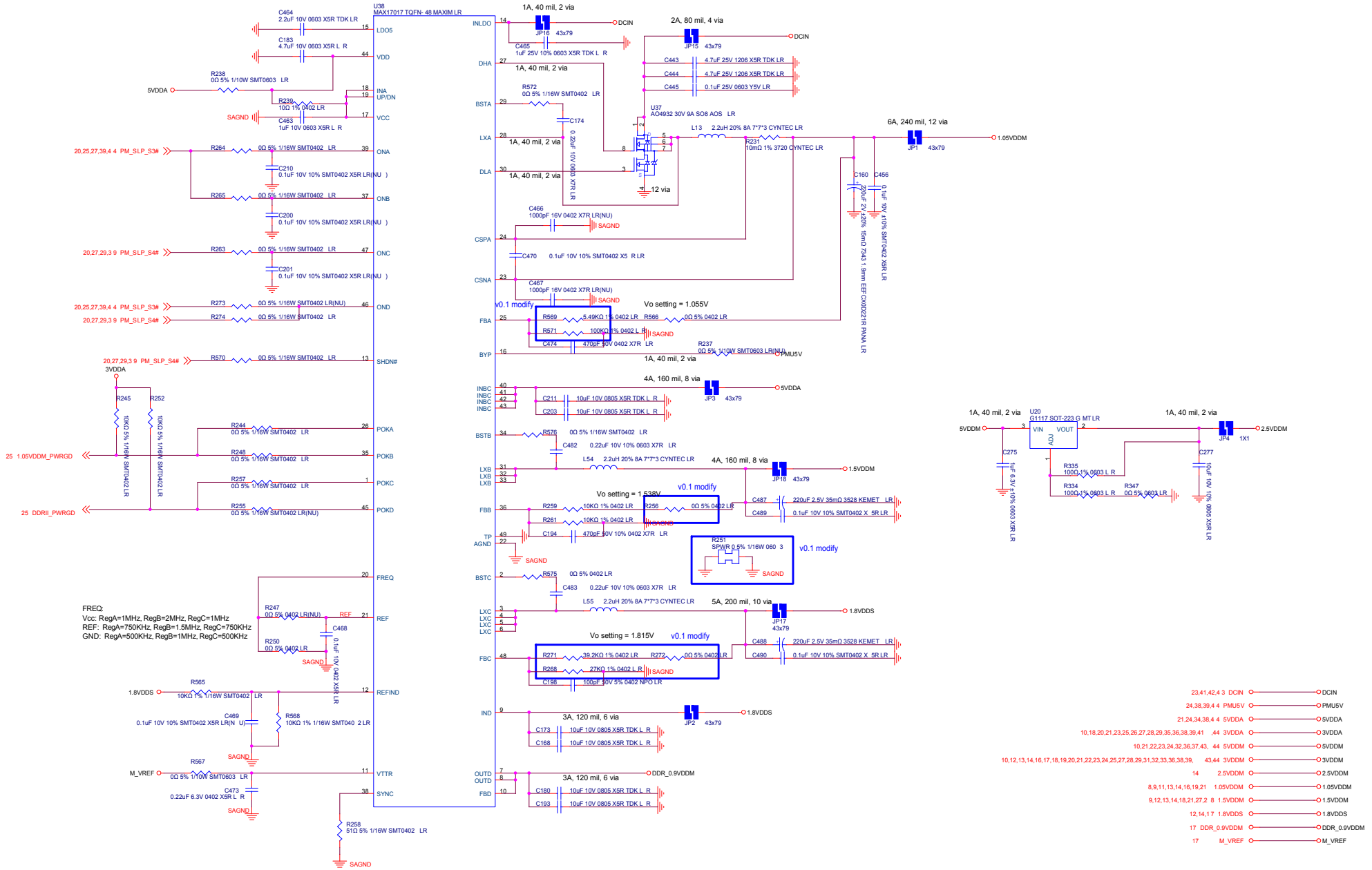
PMU5V, PMU3V, 5VDDA/S/M, 3VDDA/S/M, 1.5VDDA




U38
MAX17017 TQFN- 48 MAXIM LR
INLDO
DHA
BSTA
LXA
DLA
CSPA
CSNA
FBA
BYP
INBC
BSTB
LXB
FBB
TP
AGND
BSTC
LXC
FBC
IND
OUTD
FBD
LDO5
VDD
INA
UP/DN
VCC
ONA
ONB
ONC
OND
SHDN#
POKA
POKB
POKC
POKD
FREQ
REF
REFIND
VTTR
SYNC
1A, 40 mil, 2 via
JP16 43x79
DCIN
C465
1uF 25V 10% 0603 X5R TDK L R
2A, 80 mil, 4 via
JP15 43x79
C443 4.7uF 25V 1206 X5R TDK LR
C444 4.7uF 25V 1206 X5R TDK LR
C445 0.1uF 25V 0603 Y5V LR
R572
0Ω 5% 1/16W SMT0402 LR
C174
0.22uF 10V 0603 X7R LR
U37
AO4932 30V 9A SO8 AOS LR
12 via
L13 2.2uH 20% 8A 7*7*3 CYNTEC LR
R231
10mΩ 1% 3720 CYNTEC LR
6A, 240 mil, 12 via
JP1 43x79
1.05VDDM
C160
220uF 2V ±20% 15mΩ 7343 1.9mm EEF CX0D221R PANA LR
C456
0.1uF 10V ±10% SMT0402 X5R LR
C466
1000pF 16V 0402 X7R LR(NU)
SAGND
C470 0.1uF 10V 10% SMT0402 X5 R LR
C467
1000pF 16V 0402 X7R LR(NU)
v0.1 modify
Vo setting = 1.055V
R569 5.49KΩ 1% 0402 LR
R566 0Ω 5% 0402 LR
R571 100KΩ 1% 0402 L R
C474 470pF 50V 0402 X7R LR
R237
0Ω 5% 1/10W SMT0603 LR(NU)
PMU5V
4A, 160 mil, 8 via
JP3 43x79
5VDDA
C211 10uF 10V 0805 X5R TDK L R
C203 10uF 10V 0805 X5R TDK L R
R576 0Ω 5% 1/16W SMT0402 LR
C482 0.22uF 10V 10% 0603 X7R LR
L54 2.2uH 20% 8A 7*7*3 CYNTEC LR
4A, 160 mil, 8 via
JP18 43x79
1.5VDDM
Vo setting = 1.538V
v0.1 modify
R259 10KΩ 1% 0402 LR
R256 0Ω 5% 0402 LR
R261 10KΩ 1% 0402 LR
C194 470pF 50V 10% 0402 X7R LR
C487 220uF 2.5V 35mΩ 3528 KEMET LR
C489 0.1uF 10V 10% SMT0402 X 5R LR
R251
SPWR 0.5% 1/16W 060 3
v0.1 modify
R575 0Ω 5% 0402 LR
C483 0.22uF 10V 10% 0603 X7R LR
L55 2.2uH 20% 8A 7*7*3 CYNTEC LR
5A, 200 mil, 10 via
JP17 43x79
1.8VDDS
Vo setting = 1.815V
v0.1 modify
R271 39.2KΩ 1% 0402 LR
R272 0Ω 5% 0402 LR
R268 27KΩ 1% 0402 L R
C198 100pF 50V 5% 0402 NPO LR
C488 220uF 2.5V 35mΩ 3528 KEMET LR
C490 0.1uF 10V 10% SMT0402 X 5R LR
3A, 120 mil, 6 via
JP2 43x79
C173 10uF 10V 0805 X5R TDK L R
C168 10uF 10V 0805 X5R TDK L R
3A, 120 mil, 6 via
DDR_0.9VDDM
C180 10uF 10V 0805 X5R TDK L R
C193 10uF 10V 0805 X5R TDK L R
1A, 40 mil, 2 via
U20
G1117 SOT-223 G MT LR
VIN
VOUT
ADJ
5VDDM
2.5VDDM
JP4 1X1
C275 1uF 6.3V ±10% 0603 X5R LR
R335 100Ω 1% 0603 L R
R334 100Ω 1% 0603 L R
R347 0Ω 5% 0603 LR
C277 10uF 10V 10% 0805 X5R LR
FREQ:
Vcc: RegA=1MHz, RegB=2MHz, RegC=1MHz
REF: RegA=750KHz, RegB=1.5MHz, RegC=750KHz
GND: RegA=500KHz, RegB=1MHz, RegC=500KHz
R247 0Ω 5% 0402 LR(NU)
R250 0Ω 5% 0402 LR
C468 0.1uF 10V 0402 X5R LR
R565 10KΩ 1% 1/16W SMT0402 LR
C469 0.1uF 10V 10% SMT0402 X5R LR(N U)
R568 10KΩ 1% 1/16W SMT040 2 LR
R567 0Ω 5% 1/10W SMT0603 LR
C473 0.22uF 6.3V 0402 X5R L R
R258 51Ω 5% 1/16W SMT0402 LR
R245 10KΩ 5% 1/16W SMT0402 LR
R252 10KΩ 5% 1/16W SMT0402 LR
R238 0Ω 5% 1/10W SMT0603 LR
R239 10Ω 1% 0402 LR
C464 2.2uF 10V 0603 X5R TDK LR
C183 4.7uF 10V 0603 X5R L R
C463 1uF 10V 0603 X5R L R
C210 0.1uF 10V 10% SMT0402 X5R LR(NU)
C200 0.1uF 10V 10% SMT0402 X5R LR(NU)
C201 0.1uF 10V 10% SMT0402 X5R LR(NU)
R244 0Ω 5% 1/16W SMT0402 LR
R248 0Ω 5% 1/16W SMT0402 LR
R257 0Ω 5% 1/16W SMT0402 LR
R255 0Ω 5% 1/16W SMT0402 LR(NU)
R264 0Ω 5% 1/16W SMT0402 LR
R265 0Ω 5% 1/16W SMT0402 LR
R263 0Ω 5% 1/16W SMT0402 LR
R273 0Ω 5% 1/16W SMT0402 LR(NU)
R274 0Ω 5% 1/16W SMT0402 LR
R570 0Ω 5% 1/16W SMT0402 LR
3VDDA
25 1.05VDDM_PWRGD
25 DDRII_PWRGD
20,25,27,39,4 4 PM_SLP_S3#
20,27,29,3 9 PM_SLP_S4#
20,27,29,3 9 PM_SLP_S4#
23,41,42,4 3 DCIN
24,38,39,4 4 PMU5V
21,24,34,38,4 4 5VDDA
10,18,20,21,23,25,26,27,28,29,35,36,38,39,41 ,44 3VDDA
10,21,22,23,24,32,36,37,43, 44 5VDDM
10,12,13,14,16,17,18,19,20,21,22,23,24,25,27,28,29,31,32,33,36,38,39, 43,44 3VDDM
14 2.5VDDM
8,9,11,13,14,16,19,21 1.05VDDM
9,12,13,14,18,21,27,2 8 1.5VDDM
12,14,1 7 1.8VDDS
17 DDR_0.9VDDM
17 M_VREF
DCIN
PMU5V
5VDDA
3VDDA
5VDDM
3VDDM
2.5VDDM
1.05VDDM
1.5VDDM
1.8VDDS
DDR_0.9VDDM
M_VREF
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MODULE TRANSFER BOARD (MODULEXF)

ok

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Title
CW0A0

Size	Document Number	Rev
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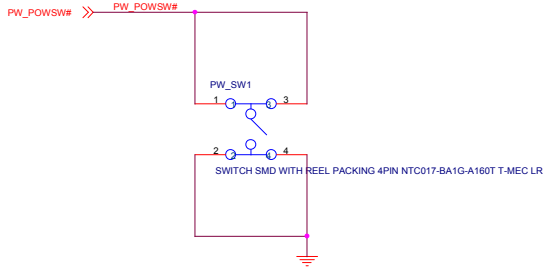

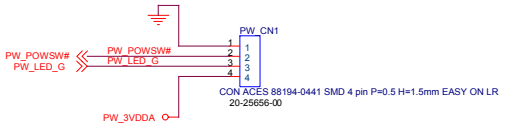

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Title	**CW0A0**	
Size: C	Document Number: **POWER SWITCH**	Rev: 0.1
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