



L50II0 Schematics Rev:B

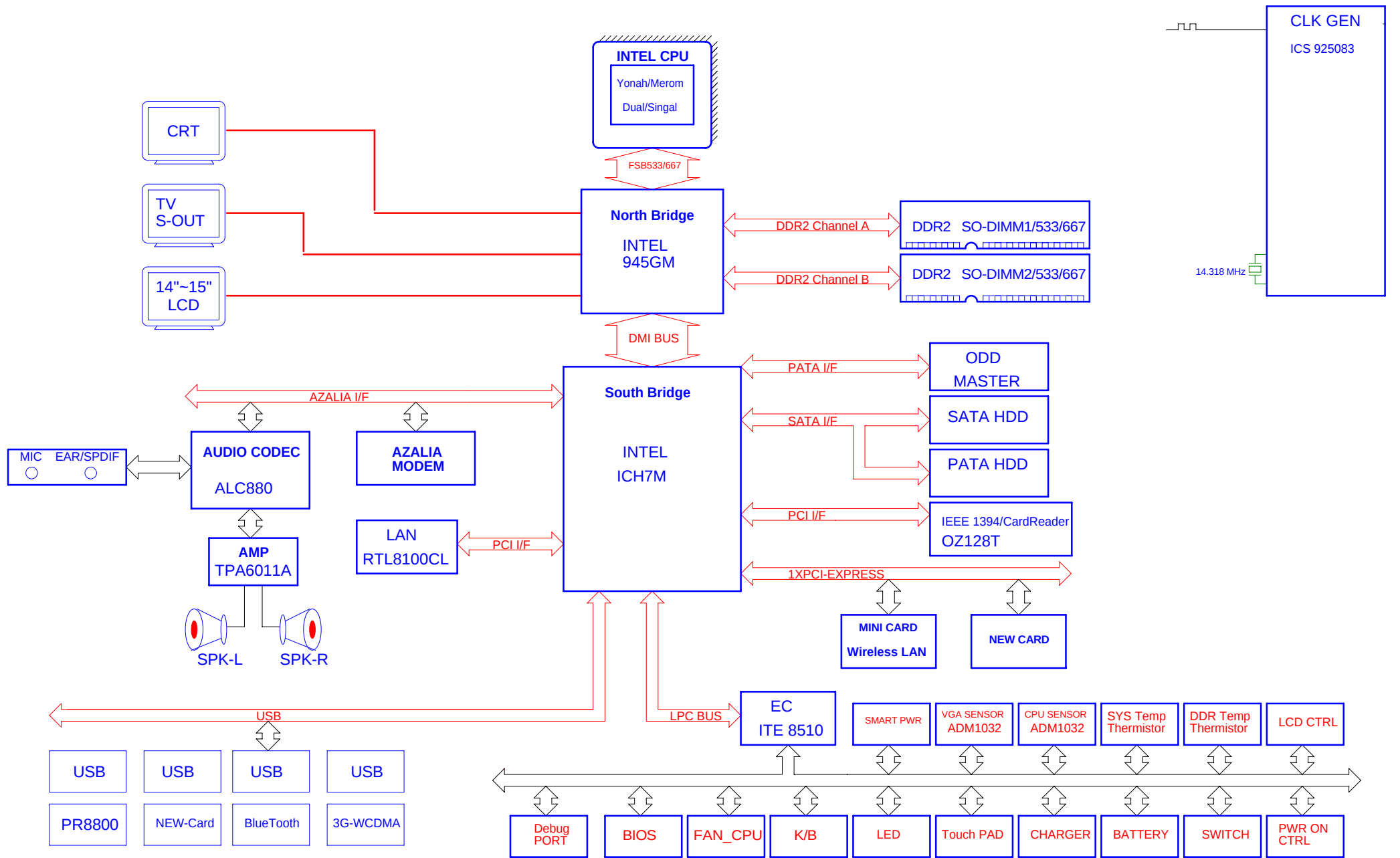
PAGE	CONTENT
1.	Cover Page
2.	System Block Diagram
3.	POWER BLOCK DIAGRAM
4.	GPIO & POWER CONSU
5.	YONAH CPU HOST & CPU Thermal Sensor
6.	CPU_POWER
7.	CLK GEN ICS9LPR310-CLK
8.	NB(1)_Host
9.	NB(2)_DMI/Configuration/PM
10.	NB(3)_VGA_TV_LVDS_PCIEx16* I/F
11.	NB(4)_DDR2 I/F
12.	NB(5)_POWER
13.	NB(6)_POWER
14.	DDR2 _SO-DIMM
15.	SB(1)_CPU/SATA/IDE/RTC/LPC/AZALIA
16.	SB(2)_PCI/GPIO/SMBUS/PM/DMI/USB/PCIEx1
17.	SB(3)_Power
18.	IEEE1394A & CARD READER
19.	LAN 10/100
20.	HDD/ODD/FAN/SMART PWR
21.	EC IT8510E
22.	LCD PWR / INVERT CONN / LVDS CONN/ROM
23.	MINI CARD & NEW CARD
24.	Daughter BD CONN
25.	CRT CONN WITH PR8800
26.	+5V&+3V(MAX8734A)
27.	+CPU CORE(MAX8771)
28.	+1.5V&+1.8V(OZ813) & +2.5V(RT9173B)
29.	+1.05V(OZ818) & +1.2V(RT9173B) & +0.9V(RT9173B)
30.	+1.0V_VGA & +1.8V_VGA(OZ813)
31.	POWER ON SWITCH FUNC.
32.	Charger func.(TL594) & DC IN CON & BATTERY CONN
33.	Every Ver. Histor

37GL50200-B0 PCB MAIN BD FOR L50II0 REV:B
82GL50200-B0 M/B ASSY FOR L50II0

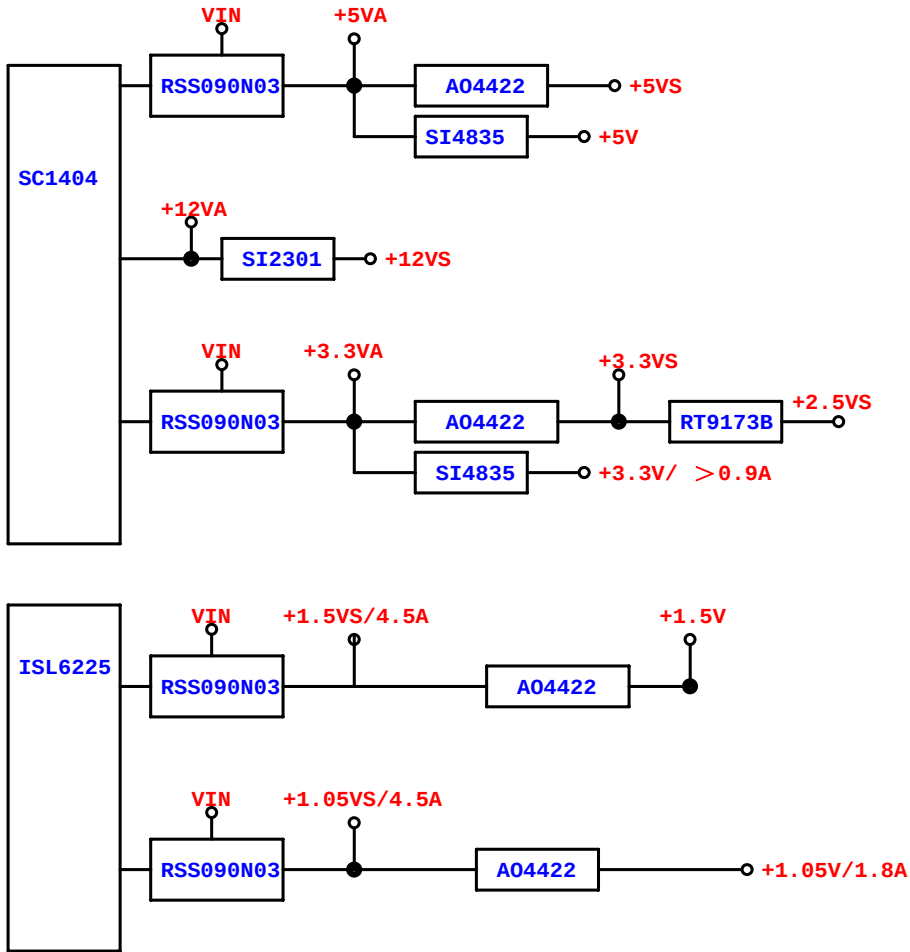
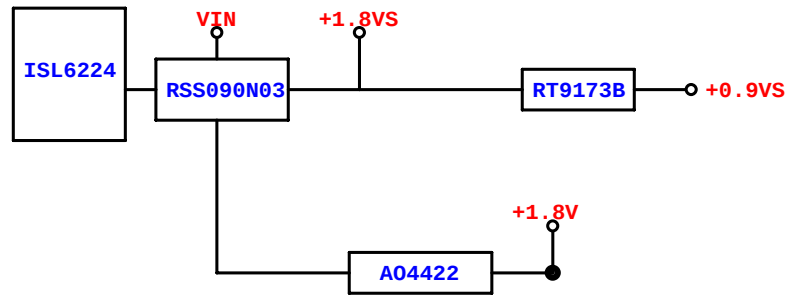
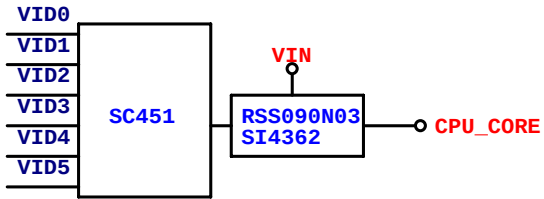
L50II0 REV:A P/N LIST

	PCB P/N	PCB ASSY P/N

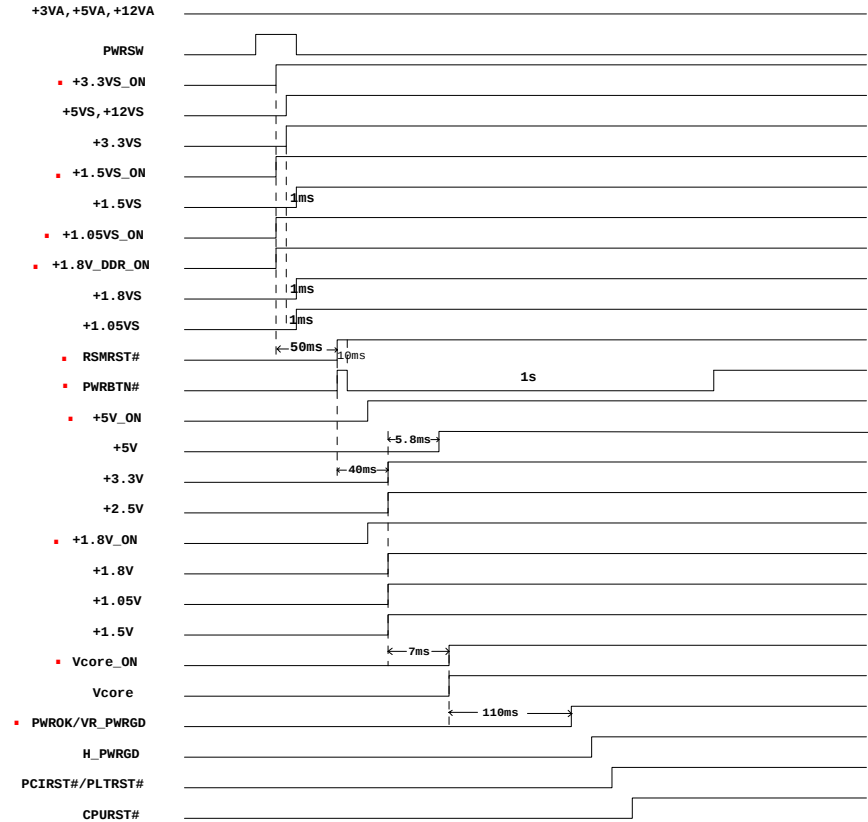
Name of Part		Cover Page	
Project	L50II0	Rev	B
Date:	Saturday, April 01, 2006	Sheet	1 / 33
3255		UNIWill COMPUTER CORP.	



POWER BLOCK DIAGRAM



POWER Sequence



ICH6-M GPIO	
GPI0	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GP018	PM_STPPCI_ICH#
GP019	
GP020	PM_STPCPU_ICH#
GP021	TPM_EN
GP023	
GPI024	
GPI025	
GPI026	SATA0_GP
GPI027	
GPI028	
GPI029	PNLSW1
GPI030	PNLSW2
GPI031	PNLSW0
GPI032	PM_CLKRUN#
GPI033	
GPI034	

ITE8510E GPIO	
GPCF0	RF_SW#
GPCF1	SILENT#
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#
GPCF7	BROWSER#
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	VOLMAX
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GP64	TP_DISABLE
GP65	LCDSW
GP66	MUTE#
GP67	EXTTS#0
GP80	CELERON_VO_DET
GPB1	CPPE#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	NA
GPE1	CPU_BSEL0
GPE2	NA
GPE3	NA
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	EC_PREST#
GPA0	BT1_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO	
GPC0	PWR0K
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1
GPC4	SB_ALERT#2
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	NA

CPU				
CPU	CORE(V)	ICC(mA)	W	TEMP(°C)
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_CORE	266	0.452	

ICH6-M			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

SMART POWER TABLE

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

ITE8510E			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V	300	1	70

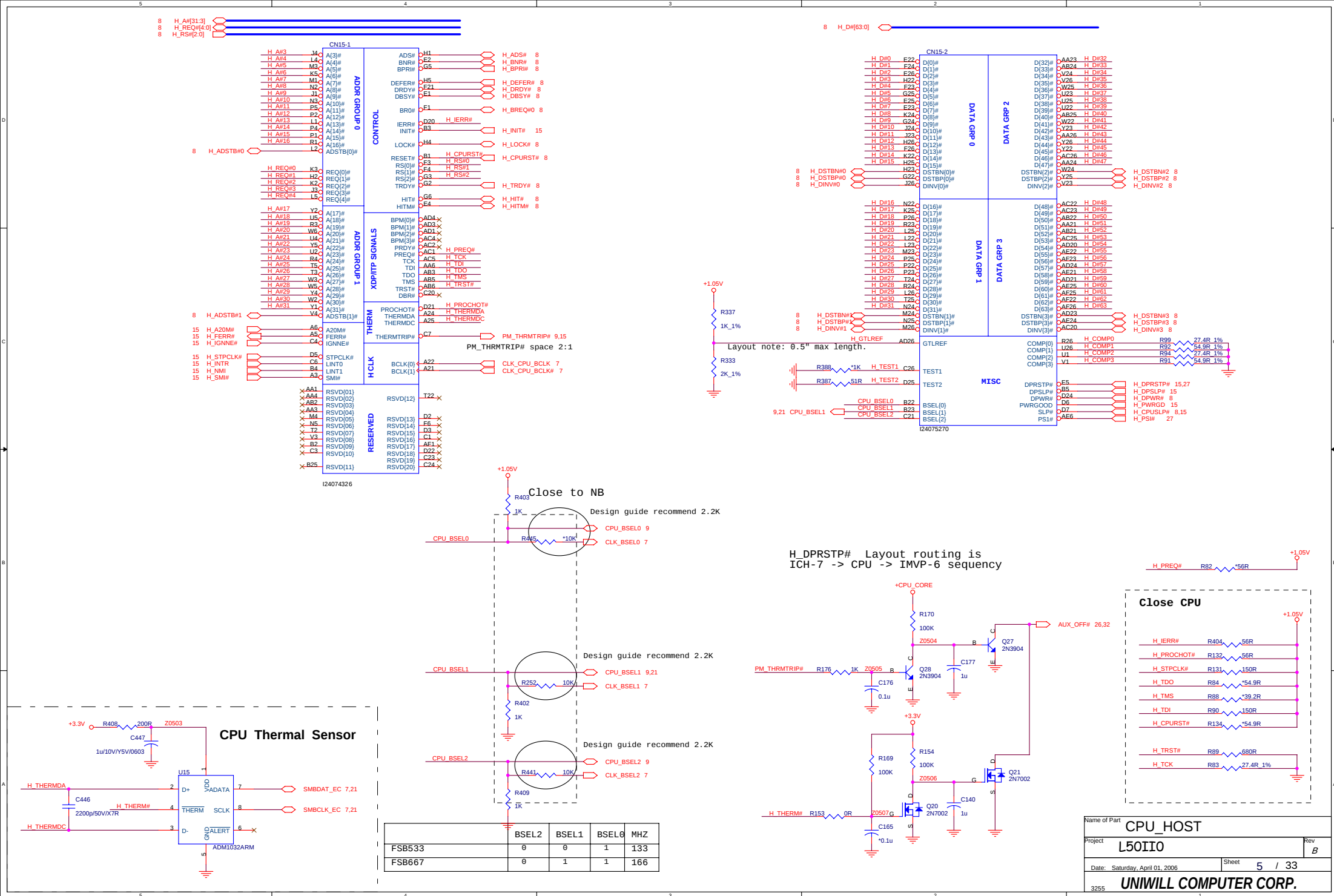
CLOCK GENERATOR			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V	180	0.594	70

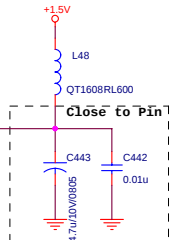
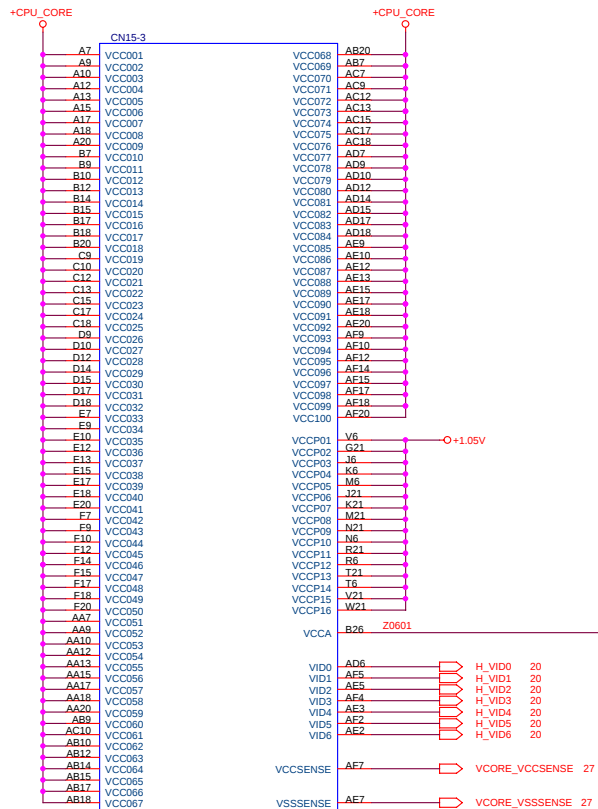
ALC880			
VCC	ICC(mA)	W	TEMP(°C)
+3.3V(DVDD)	71	0.234	70

TPA6011A4			
VCC	ICC(mA)	W	TEMP(°C)
3.3V	30	0.099W	85

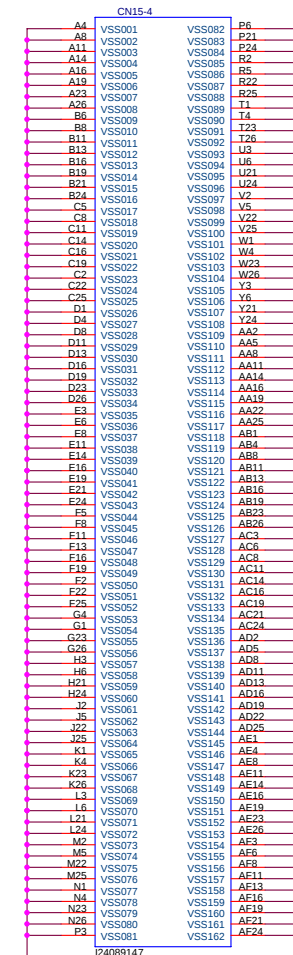
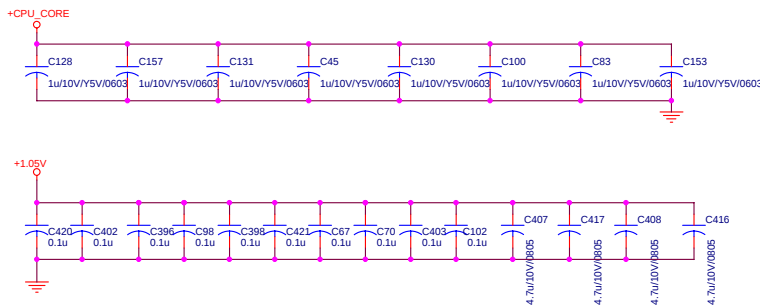
ADM1032			
VCC	ICC	W	TEMP(°C)
+3.3V	170uA	0.56mW	150

Name of Part		GPIO & POWER CONSU	
Project	L50IIO	Rev	B
Date:	Saturday, April 01, 2006	Sheet	4 / 33
3255	UNIWILL COMPUTER CORP.		



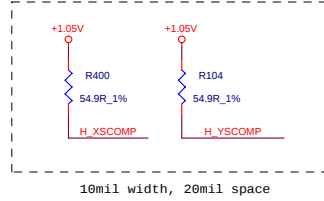


QT1608GRL600 = 200mA
 QT1608RL120 = 200mA
 QT1608RL600 = 200 mA
 QT1608RL030 = 500mA
 QT1608RL060 = 500mA

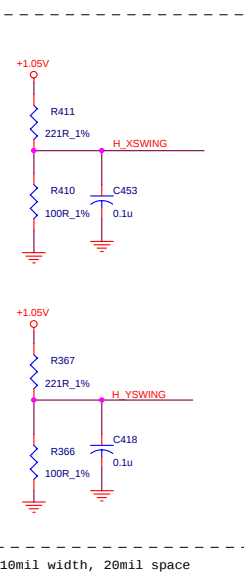


AT23	VSS_180	J11	VSS_273
AN23	VSS_181	D11	VSS_274
AM23	VSS_182	B11	VSS_275
AC23	VSS_183	AV10	VSS_276
W23	VSS_185	AP10	VSS_277
K23	VSS_186	AL10	VSS_278
J23	VSS_187	AG10	VSS_279
F23	VSS_188	AC10	VSS_280
C23	VSS_189	W10	VSS_281
AA22	VSS_190	LI10	VSS_282
K22	VSS_191	BA9	VSS_283
G22	VSS_192	AW9	VSS_284
F22	VSS_193	AB9	VSS_285
E22	VSS_194	AG9	VSS_286
D22	VSS_195	AB9	VSS_287
A22	VSS_196	AG9	VSS_288
BA21	VSS_197	E9	VSS_289
AV21	VSS_198	AG9	VSS_290
AR21	VSS_199	AG8	VSS_291
AN21	VSS_200	AG8	VSS_292
AL21	VSS_201	AG8	VSS_293
AB21	VSS_202	AD8	VSS_294
Y21	VSS_203	AA8	VSS_295
Z21	VSS_204	K8	VSS_296
K21	VSS_205	VSS_297	VSS_297
J21	VSS_206	VSS_298	VSS_298
H21	VSS_207	VSS_299	VSS_299
C21	VSS_208	VSS_300	VSS_300
AW20	VSS_209	AV7	VSS_301
AR20	VSS_210	AP7	VSS_302
AA20	VSS_211	AL7	VSS_303
K20	VSS_212	AG7	VSS_304
B20	VSS_213	AG7	VSS_305
A20	VSS_214	AG7	VSS_306
AN19	VSS_215	AG7	VSS_307
AC19	VSS_216	G7	VSS_308
W19	VSS_217	D7	VSS_309
K19	VSS_218	AD6	VSS_310
G19	VSS_219	AB6	VSS_311
C19	VSS_220	Y6	VSS_312
AN18	VSS_221	U6	VSS_313
P18	VSS_222	N6	VSS_314
H18	VSS_223	N6	VSS_315
D18	VSS_224	K6	VSS_316
A18	VSS_225	H6	VSS_317
AY17	VSS_226	B6	VSS_318
AV17	VSS_227	AV5	VSS_319
AM17	VSS_228	AF5	VSS_320
AC17	VSS_229	AD5	VSS_321
AV16	VSS_230	AY4	VSS_322
AN16	VSS_231	AR4	VSS_323
AL16	VSS_232	AD4	VSS_324
J16	VSS_233	AL4	VSS_325
F16	VSS_234	Y4	VSS_326
C16	VSS_235	U4	VSS_327
AN15	VSS_236	R4	VSS_328
AM15	VSS_237	J4	VSS_329
AK15	VSS_238	F4	VSS_330
N15	VSS_239	C4	VSS_331
L15	VSS_240	AY3	VSS_332
B15	VSS_241	AW3	VSS_333
A15	VSS_242	U3	VSS_334
BA14	VSS_243	R3	VSS_335
AT14	VSS_244	AL3	VSS_336
AK14	VSS_245	AG3	VSS_337
AD14	VSS_246	AT2	VSS_338
AA14	VSS_247	AG2	VSS_339
U14	VSS_248	AG2	VSS_340
K14	VSS_249	AG2	VSS_341
H14	VSS_250	AG2	VSS_342
E14	VSS_251	AG2	VSS_343
AV13	VSS_252	AG2	VSS_344
AR13	VSS_253	AG2	VSS_345
AN13	VSS_254	AG2	VSS_346
AM13	VSS_255	AG2	VSS_347
AC13	VSS_256	AG2	VSS_348
W13	VSS_257	AG2	VSS_349
K13	VSS_258	AG2	VSS_350
J13	VSS_259	AG2	VSS_351
F13	VSS_260	AG2	VSS_352
C13	VSS_261	AG2	VSS_353
AN12	VSS_262	AG2	VSS_354
AM12	VSS_263	AG2	VSS_355
AC12	VSS_264	AG2	VSS_356
W12	VSS_265	AG2	VSS_357
K12	VSS_266	AG2	VSS_358
J12	VSS_267	AG2	VSS_359
F12	VSS_268	AG2	VSS_360
C12	VSS_269	AG2	VSS_361
AN11	VSS_270	AG2	VSS_362
AM11	VSS_271	AG2	VSS_363
AC11	VSS_272	AG2	VSS_364

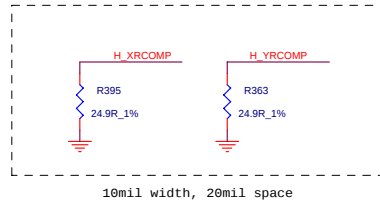
FSB I/O slew rate compensation



Reference Voltage for RCOMP



Calibration FSB I/O Buffer



5 H_DM[63:0]
5 H_AW[31:3]

H_DM0	F1	H_DM#_0	H_DM#_0
H_DM1	J1	H_DM#_1	H_DM#_1
H_DM2	H1	H_DM#_2	H_DM#_2
H_DM3	H3	H_DM#_3	H_DM#_3
H_DM4	J6	H_DM#_4	H_DM#_4
H_DM5	K2	H_DM#_5	H_DM#_5
H_DM6	G1	H_DM#_6	H_DM#_6
H_DM7	C2	H_DM#_7	H_DM#_7
H_DM8	K9	H_DM#_8	H_DM#_8
H_DM9	K1	H_DM#_9	H_DM#_9
H_DM10	J2	H_DM#_10	H_DM#_10
H_DM11	K7	H_DM#_11	H_DM#_11
H_DM12	J8	H_DM#_12	H_DM#_12
H_DM13	H4	H_DM#_13	H_DM#_13
H_DM14	J3	H_DM#_14	H_DM#_14
H_DM15	G4	H_DM#_15	H_DM#_15
H_DM16	T10	H_DM#_16	H_DM#_16
H_DM17	T3	H_DM#_17	H_DM#_17
H_DM18	W11	H_DM#_18	H_DM#_18
H_DM19	U7	H_DM#_19	H_DM#_19
H_DM20	U9	H_DM#_20	H_DM#_20
H_DM21	U11	H_DM#_21	H_DM#_21
H_DM22	T11	H_DM#_22	H_DM#_22
H_DM23	W9	H_DM#_23	H_DM#_23
H_DM24	T8	H_DM#_24	H_DM#_24
H_DM25	T4	H_DM#_25	H_DM#_25
H_DM26	T4	H_DM#_26	H_DM#_26
H_DM27	W7	H_DM#_27	H_DM#_27
H_DM28	U6	H_DM#_28	H_DM#_28
H_DM29	T9	H_DM#_29	H_DM#_29
H_DM30	W6	H_DM#_30	H_DM#_30
H_DM31	T5	H_DM#_31	H_DM#_31
H_DM32	AB7	H_DM#_32	H_DM#_32
H_DM33	AA9	H_DM#_33	H_DM#_33
H_DM34	WA	H_DM#_34	H_DM#_34
H_DM35	W3	H_DM#_35	H_DM#_35
H_DM36	Y3	H_DM#_36	H_DM#_36
H_DM37	Y7	H_DM#_37	H_DM#_37
H_DM38	W5	H_DM#_38	H_DM#_38
H_DM39	Y10	H_DM#_39	H_DM#_39
H_DM40	AB8	H_DM#_40	H_DM#_40
H_DM41	W2	H_DM#_41	H_DM#_41
H_DM42	AA4	H_DM#_42	H_DM#_42
H_DM43	AA7	H_DM#_43	H_DM#_43
H_DM44	AA2	H_DM#_44	H_DM#_44
H_DM45	AA6	H_DM#_45	H_DM#_45
H_DM46	AA10	H_DM#_46	H_DM#_46
H_DM47	Y8	H_DM#_47	H_DM#_47
H_DM48	AA1	H_DM#_48	H_DM#_48
H_DM49	AB4	H_DM#_49	H_DM#_49
H_DM50	AC9	H_DM#_50	H_DM#_50
H_DM51	AB11	H_DM#_51	H_DM#_51
H_DM52	AC11	H_DM#_52	H_DM#_52
H_DM53	AB3	H_DM#_53	H_DM#_53
H_DM54	AC2	H_DM#_54	H_DM#_54
H_DM55	AD1	H_DM#_55	H_DM#_55
H_DM56	AD9	H_DM#_56	H_DM#_56
H_DM57	AC1	H_DM#_57	H_DM#_57
H_DM58	AD7	H_DM#_58	H_DM#_58
H_DM59	AC8	H_DM#_59	H_DM#_59
H_DM60	AB5	H_DM#_60	H_DM#_60
H_DM61	AD10	H_DM#_61	H_DM#_61
H_DM62	AD4	H_DM#_62	H_DM#_62
H_DM63	AC8	H_DM#_63	H_DM#_63

H_XRCOMP	E1	H_XRCOMP	H_XRCOMP
H_XSCOMP	E2	H_XSCOMP	H_XSCOMP
H_XSWING	E4	H_XSWING	H_XSWING

H_YRCOMP	Y1	H_YRCOMP	H_YRCOMP
H_YSCOMP	U1	H_YSCOMP	H_YSCOMP
H_YSWING	W1	H_YSWING	H_YSWING

7 CLK_MCH_BCLK
7 CLK_MCH_BCLK#

AG2	AG2	H_CLKIN	H_CLKIN
AG1	AG1	H_CLKIN#	H_CLKIN#

HOST

H_A#_3	H_A#3	H_A#3	H_A#3
H_A#_4	H_A#4	H_A#4	H_A#4
H_A#_5	H_A#5	H_A#5	H_A#5
H_A#_6	H_A#6	H_A#6	H_A#6
H_A#_7	H_A#7	H_A#7	H_A#7
H_A#_8	H_A#8	H_A#8	H_A#8
H_A#_9	H_A#9	H_A#9	H_A#9
H_A#_10	H_A#10	H_A#10	H_A#10
H_A#_11	H_A#11	H_A#11	H_A#11
H_A#_12	H_A#12	H_A#12	H_A#12
H_A#_13	H_A#13	H_A#13	H_A#13
H_A#_14	H_A#14	H_A#14	H_A#14
H_A#_15	H_A#15	H_A#15	H_A#15
H_A#_16	H_A#16	H_A#16	H_A#16
H_A#_17	H_A#17	H_A#17	H_A#17
H_A#_18	H_A#18	H_A#18	H_A#18
H_A#_19	H_A#19	H_A#19	H_A#19
H_A#_20	H_A#20	H_A#20	H_A#20
H_A#_21	H_A#21	H_A#21	H_A#21
H_A#_22	H_A#22	H_A#22	H_A#22
H_A#_23	H_A#23	H_A#23	H_A#23
H_A#_24	H_A#24	H_A#24	H_A#24
H_A#_25	H_A#25	H_A#25	H_A#25
H_A#_26	H_A#26	H_A#26	H_A#26
H_A#_27	H_A#27	H_A#27	H_A#27
H_A#_28	H_A#28	H_A#28	H_A#28
H_A#_29	H_A#29	H_A#29	H_A#29
H_A#_30	H_A#30	H_A#30	H_A#30
H_A#_31	H_A#31	H_A#31	H_A#31

H_ADS#	E8	H_ADS#	H_ADS#
H_ADSTB#_0	B9	H_ADSTB#_0	H_ADSTB#_0
H_ADSTB#_1	C13	H_ADSTB#_1	H_ADSTB#_1
H_VREF	I13	H_VREF	H_VREF
H_BNR#	C6	H_BNR#	H_BNR#
H_BREQ#0	C7	H_BREQ#0	H_BREQ#0
H_CPURST#	B7	H_CPURST#	H_CPURST#
H_DEBSY#	A7	H_DEBSY#	H_DEBSY#
H_DEFER#	C3	H_DEFER#	H_DEFER#
H_DPWR#	J9	H_DPWR#	H_DPWR#
H_DRDY#	H8	H_DRDY#	H_DRDY#
H_VREF	K13	H_VREF	H_VREF

H_DINV#_0	J7	H_DINV#_0	H_DINV#_0
H_DINV#_1	W8	H_DINV#_1	H_DINV#_1
H_DINV#_2	U3	H_DINV#_2	H_DINV#_2
H_DINV#_3	AB10	H_DINV#_3	H_DINV#_3

H_DSTBN#0	K4	H_DSTBN#0	H_DSTBN#0
H_DSTBN#1	T7	H_DSTBN#1	H_DSTBN#1
H_DSTBN#2	Y5	H_DSTBN#2	H_DSTBN#2
H_DSTBN#3	AC4	H_DSTBN#3	H_DSTBN#3

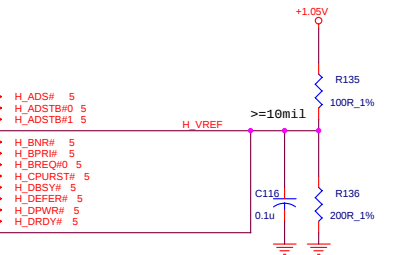
H_DSTBP#0	K3	H_DSTBP#0	H_DSTBP#0
H_DSTBP#1	T6	H_DSTBP#1	H_DSTBP#1
H_DSTBP#2	AA5	H_DSTBP#2	H_DSTBP#2
H_DSTBP#3	AC5	H_DSTBP#3	H_DSTBP#3

H_HIT#	D3	H_HIT#	H_HIT#
H_HITM#	D4	H_HITM#	H_HITM#
H_LOCK#	B3	H_LOCK#	H_LOCK#

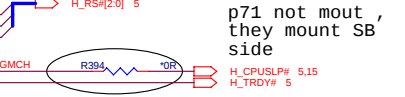
H_REQ#_0	D8	H_REQ#_0	H_REQ#_0
H_REQ#_1	C8	H_REQ#_1	H_REQ#_1
H_REQ#_2	B8	H_REQ#_2	H_REQ#_2
H_REQ#_3	F8	H_REQ#_3	H_REQ#_3
H_REQ#_4	A8	H_REQ#_4	H_REQ#_4

H_RS#_0	B4	H_RS#_0	H_RS#_0
H_RS#_1	E6	H_RS#_1	H_RS#_1
H_RS#_2	D6	H_RS#_2	H_RS#_2

H_SLPUP#	E3	H_SLPUP#	H_SLPUP#
H_TRDY#	E7	H_TRDY#	H_TRDY#

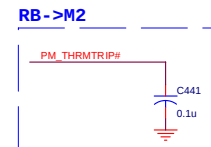


Close to MGCH <100mil

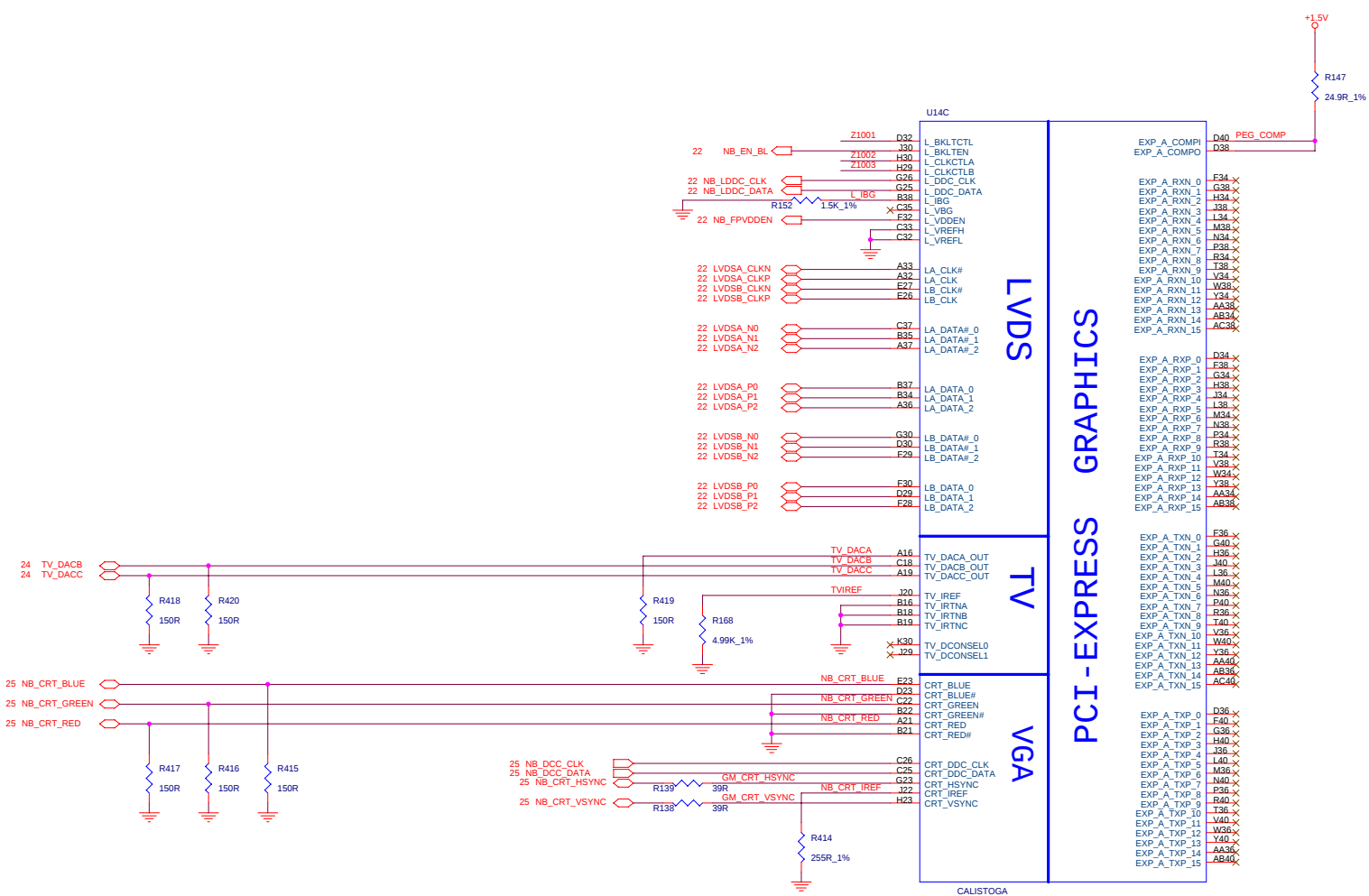


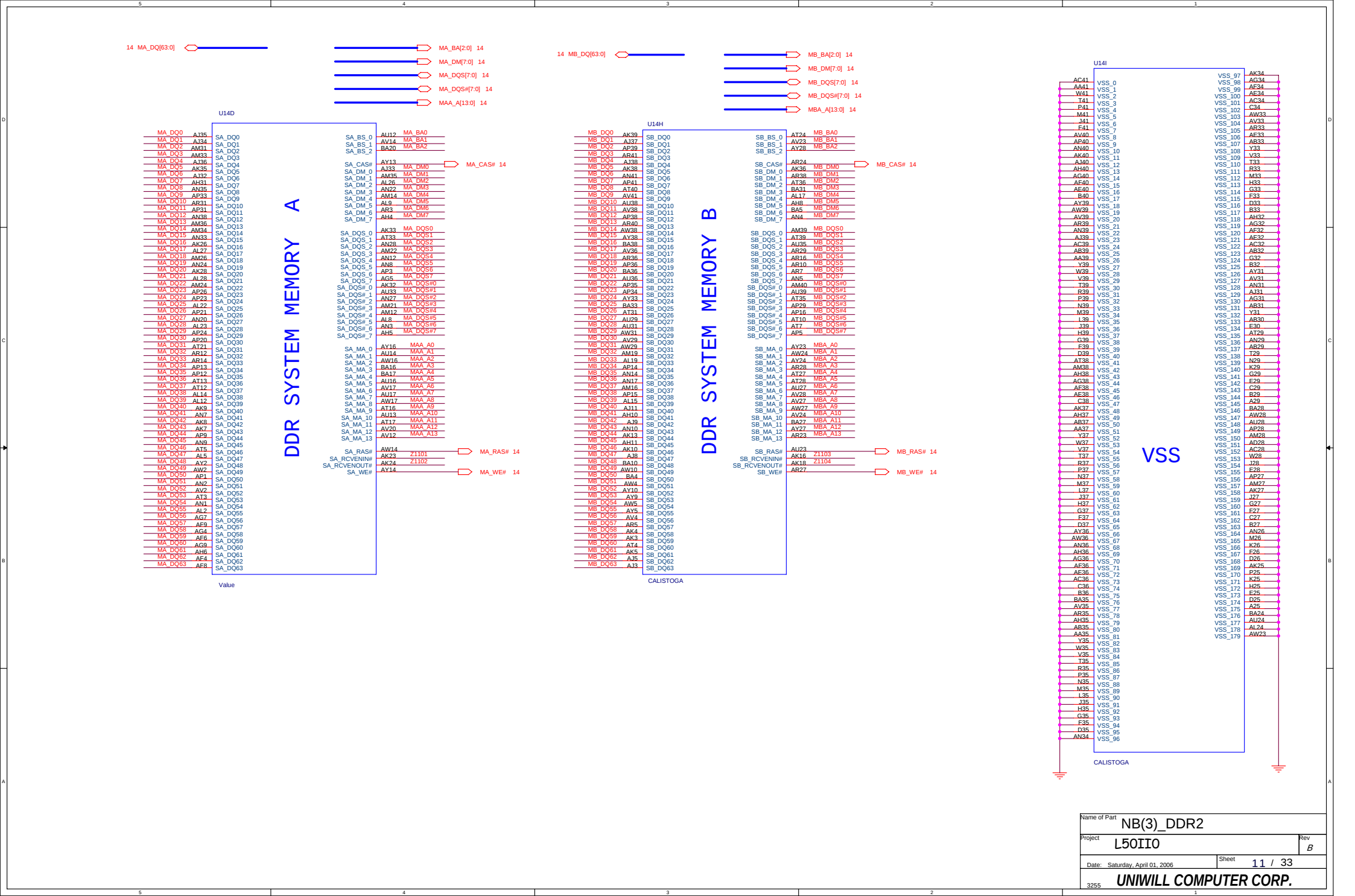
p71 not mout , they mount SB side

Name of Part	NB(1)_Host
Project	L50II0
Date:	Saturday, April 01, 2006
Sheet	8 / 33
3255	UNIWILL COMPUTER CORP.



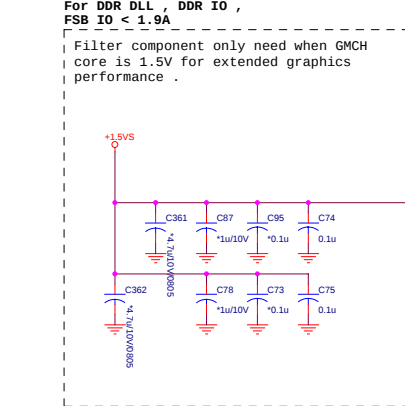
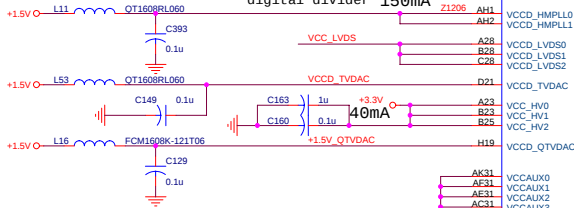
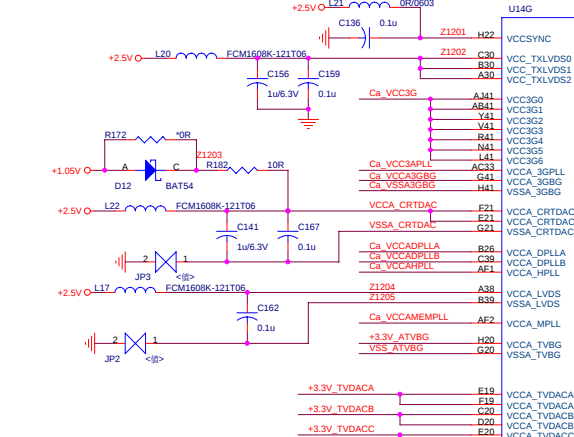
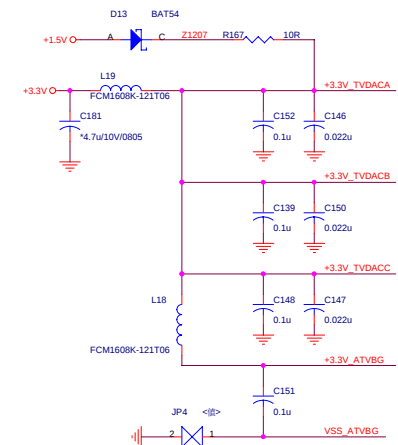
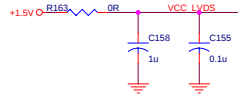
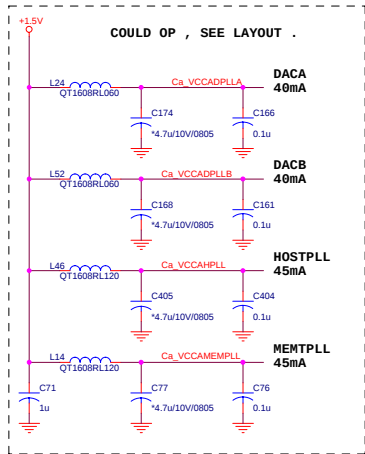
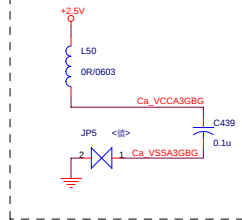
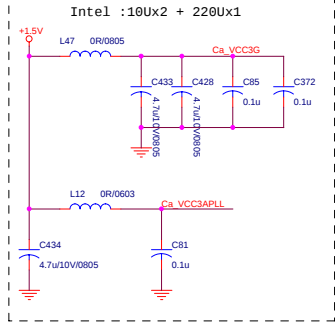
Name of Part		NB(2)_DMI/VGA/MICS	
Project	L50II0	Rev	B
Date:	Saturday, April 01, 2006	Sheet	9 / 33
3255 UNIWILL COMPUTER CORP.			





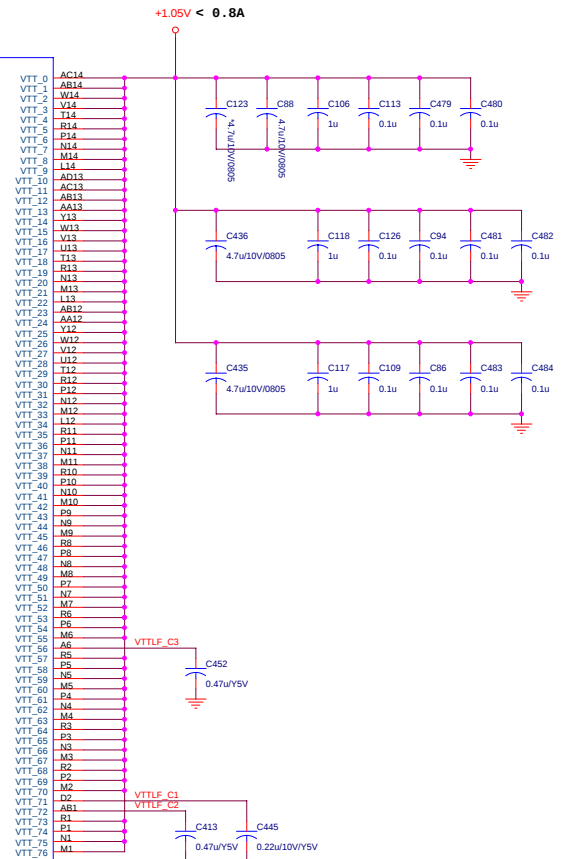
PCIE & DMI ANA
POWER <1.5 A

2.5V PCIE ANA
Power < 2 mA

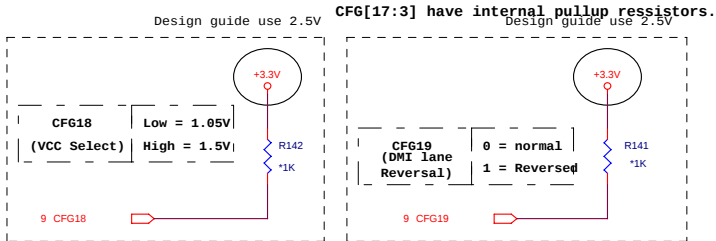
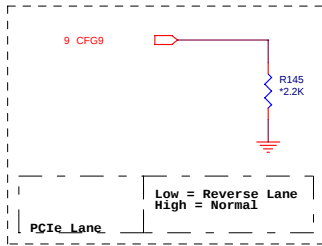
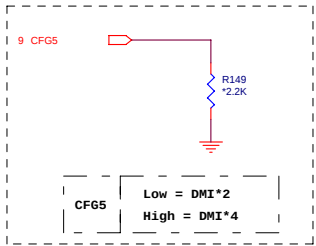
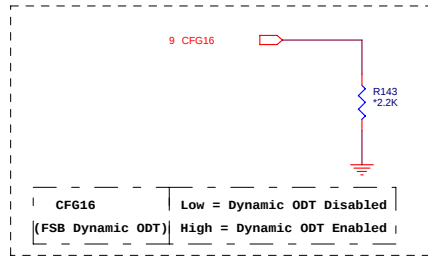


POWER

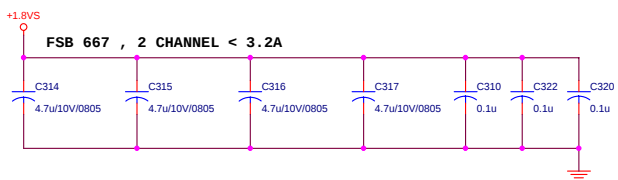
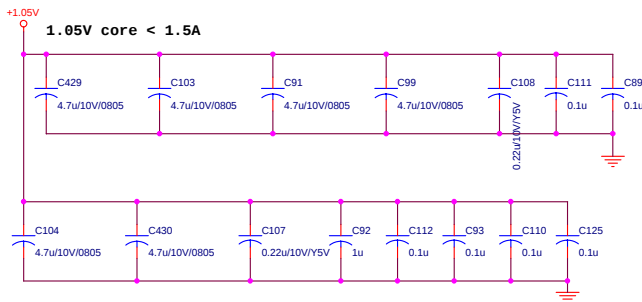
POWER



NB 1.05V layout < 2.5A
NB 1.5VS layout < 1.9A
NB 1.5V layout < 1.8A
NB 2.5V layout < 0.1A
NB 3.3V layout < 0.1A
NB 1.8VS layout < 3.2A

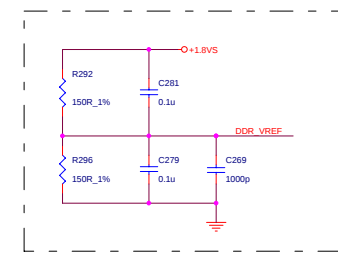
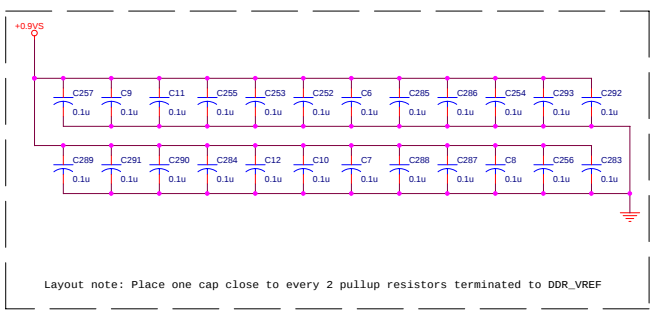
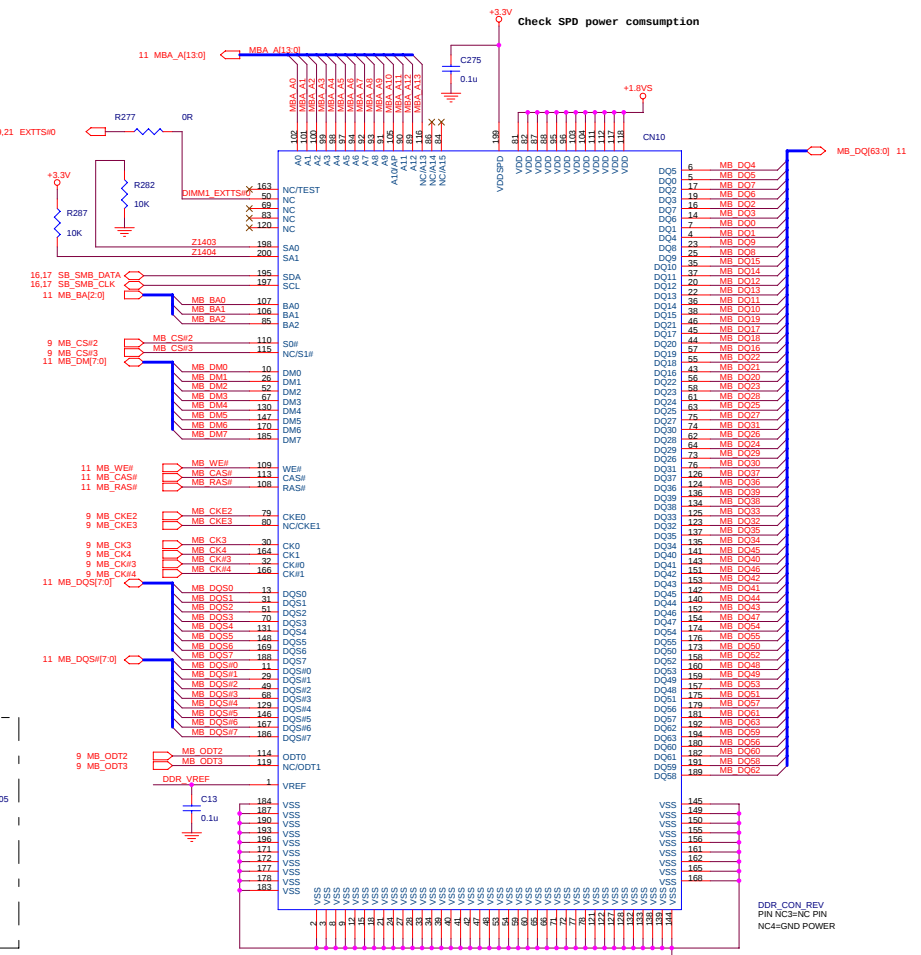
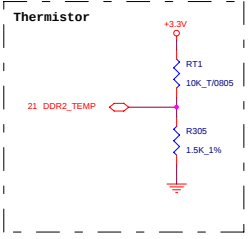
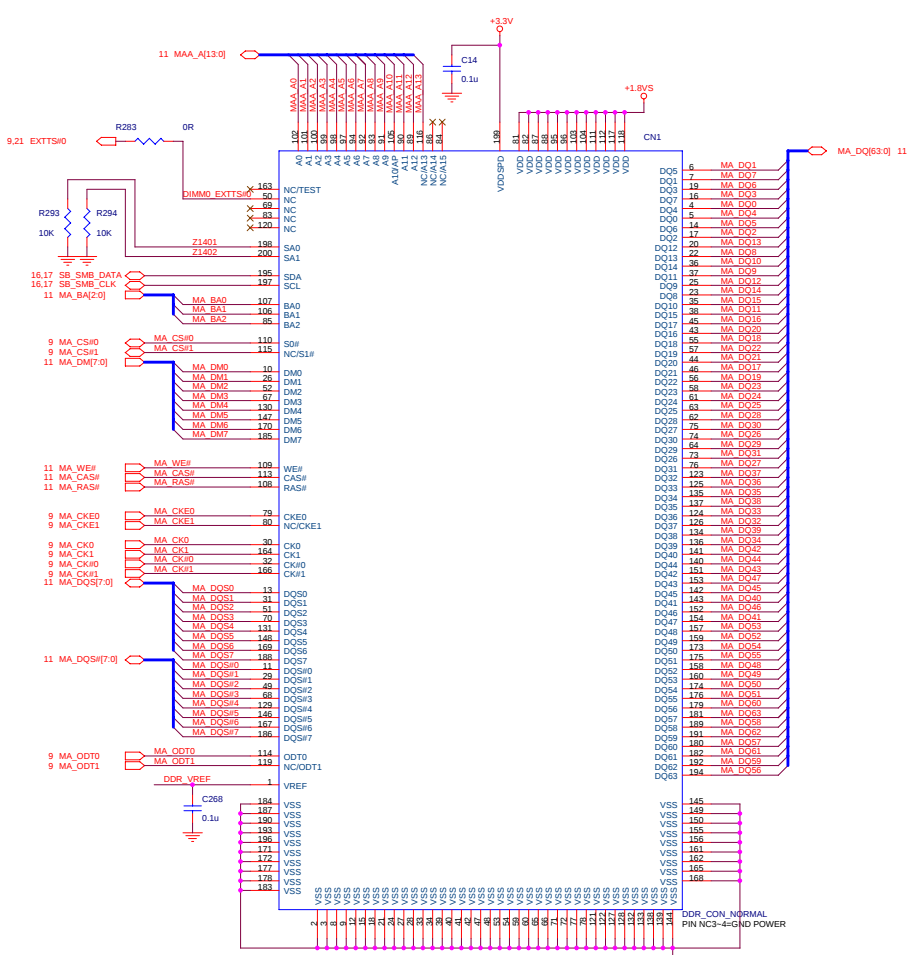


CFG[20:18] have internal pulldown resistors.

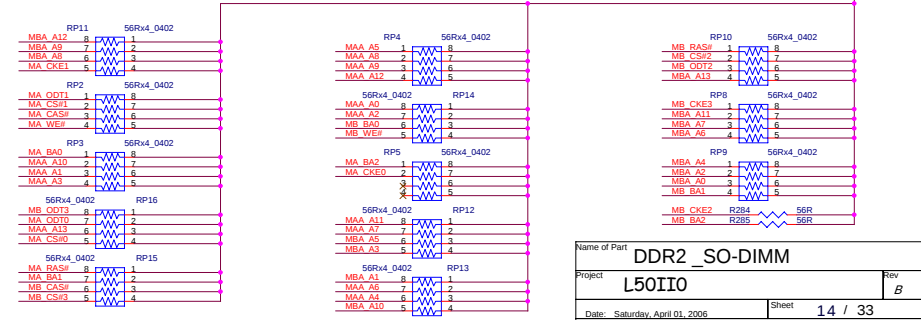


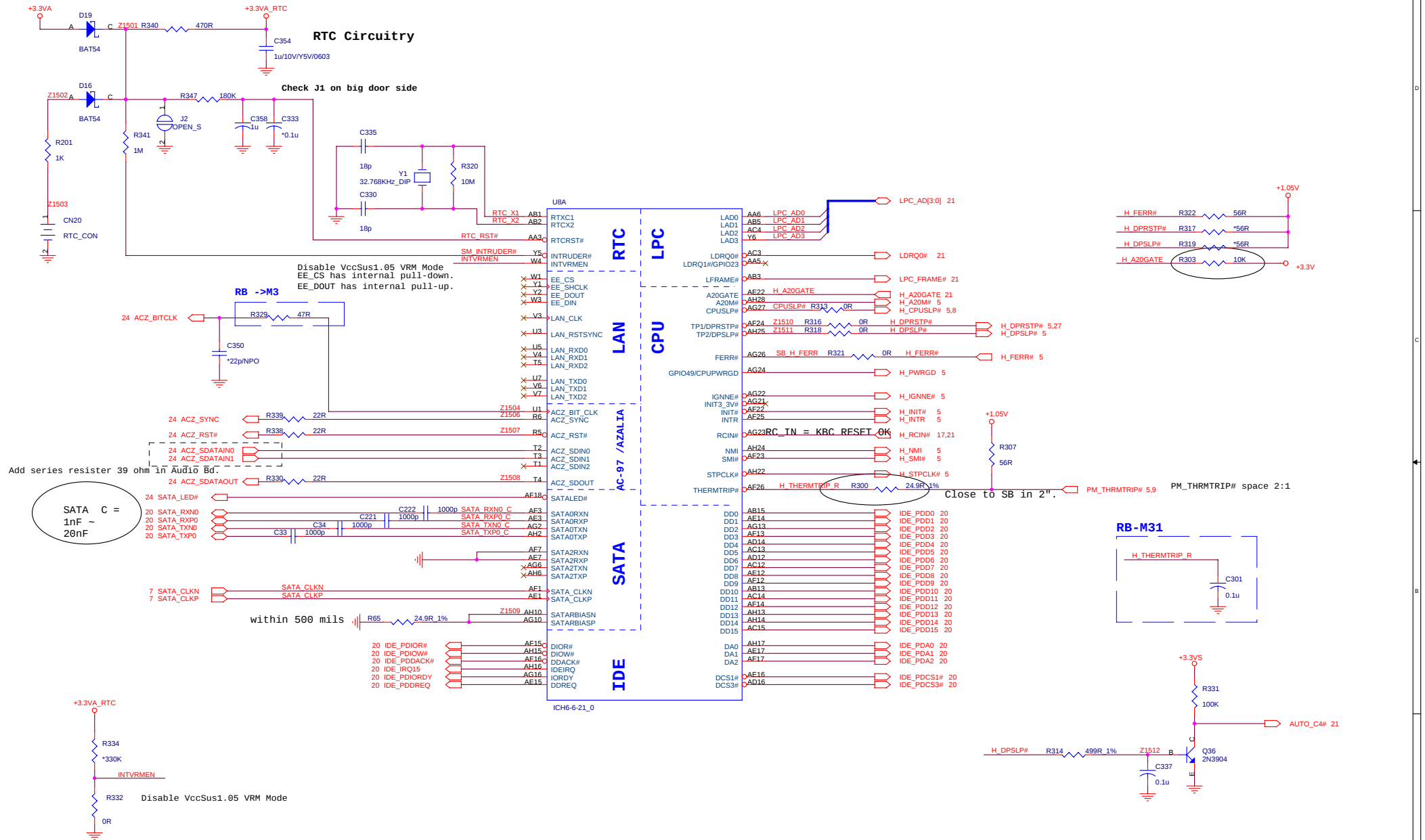
U14E

AA33 VCC_0
W33 VCC_1
P33 VCC_2
N33 VCC_3
L33 VCC_4
J33 VCC_5
AA32 VCC_6
L32 VCC_7
W32 VCC_8
V32 VCC_9
P32 VCC_10
N32 VCC_11
L32 VCC_12
M32 VCC_13
J32 VCC_14
AA31 VCC_15
W31 VCC_16
V31 VCC_17
P31 VCC_18
N31 VCC_19
L31 VCC_20
M31 VCC_21
J31 VCC_22
AA30 VCC_23
W30 VCC_24
V30 VCC_25
P30 VCC_26
N30 VCC_27
L30 VCC_28
M30 VCC_29
J30 VCC_30
P30 VCC_31
N30 VCC_32
L30 VCC_33
AA29 VCC_34
W29 VCC_35
V29 VCC_36
P29 VCC_37
N29 VCC_38
L29 VCC_39
M29 VCC_40
J29 VCC_41
AA28 VCC_42
W28 VCC_43
V28 VCC_44
P28 VCC_45
N28 VCC_46
L28 VCC_47
M28 VCC_48
J28 VCC_49
AA27 VCC_50
W27 VCC_51
V27 VCC_52
P27 VCC_53
N27 VCC_54
L27 VCC_55
M27 VCC_56
J27 VCC_57
AA26 VCC_58
W26 VCC_59
V26 VCC_60
P26 VCC_61
N26 VCC_62
L26 VCC_63
M26 VCC_64
J26 VCC_65
AA25 VCC_66
W25 VCC_67
V25 VCC_68
P25 VCC_69
N25 VCC_70
L25 VCC_71
M25 VCC_72
J25 VCC_73
AA24 VCC_74
W24 VCC_75
V24 VCC_76
P24 VCC_77
N24 VCC_78
L24 VCC_79
M24 VCC_80
J24 VCC_81
AA23 VCC_82
W23 VCC_83
V23 VCC_84
P23 VCC_85
N23 VCC_86
L23 VCC_87
M23 VCC_88
J23 VCC_89
AA22 VCC_90
W22 VCC_91
V22 VCC_92
P22 VCC_93
N22 VCC_94
L22 VCC_95
M22 VCC_96
J22 VCC_97
AA21 VCC_98
W21 VCC_99
V21 VCC_100
P21 VCC_101
N21 VCC_102
L21 VCC_103
M21 VCC_104
J21 VCC_105
AA20 VCC_106
W20 VCC_107
V20 VCC_108
P20 VCC_109
N20 VCC_110
L20 VCC_111
M20 VCC_112
J20 VCC_113
AA19 VCC_114
W19 VCC_115
V19 VCC_116
P19 VCC_117
N19 VCC_118
L19 VCC_119
M19 VCC_120
J19 VCC_121
AA18 VCC_122
W18 VCC_123
V18 VCC_124
P18 VCC_125
N18 VCC_126
L18 VCC_127
M18 VCC_128
J18 VCC_129
AA17 VCC_130
W17 VCC_131
V17 VCC_132
P17 VCC_133
N17 VCC_134
L17 VCC_135
M17 VCC_136
J17 VCC_137
AA16 VCC_138
W16 VCC_139
V16 VCC_140
P16 VCC_141
N16 VCC_142
L16 VCC_143
M16 VCC_144
J16 VCC_145
AA15 VCC_146
W15 VCC_147
V15 VCC_148
P15 VCC_149
N15 VCC_150
L15 VCC_151
M15 VCC_152
J15 VCC_153
AA14 VCC_154
W14 VCC_155
V14 VCC_156
P14 VCC_157
N14 VCC_158
L14 VCC_159
M14 VCC_160
J14 VCC_161
AA13 VCC_162
W13 VCC_163
V13 VCC_164
P13 VCC_165
N13 VCC_166
L13 VCC_167
M13 VCC_168
J13 VCC_169
AA12 VCC_170
W12 VCC_171
V12 VCC_172
P12 VCC_173
N12 VCC_174
L12 VCC_175
M12 VCC_176
J12 VCC_177
AA11 VCC_178
W11 VCC_179
V11 VCC_180
P11 VCC_181
N11 VCC_182
L11 VCC_183
M11 VCC_184
J11 VCC_185
AA10 VCC_186
W10 VCC_187
V10 VCC_188
P10 VCC_189
N10 VCC_190
L10 VCC_191
M10 VCC_192
J10 VCC_193
AA9 VCC_194
W9 VCC_195
V9 VCC_196
P9 VCC_197
N9 VCC_198
L9 VCC_199
M9 VCC_200
J9 VCC_201
AA8 VCC_202
W8 VCC_203
V8 VCC_204
P8 VCC_205
N8 VCC_206
L8 VCC_207
M8 VCC_208
J8 VCC_209
AA7 VCC_210
W7 VCC_211
V7 VCC_212
P7 VCC_213
N7 VCC_214
L7 VCC_215
M7 VCC_216
J7 VCC_217
AA6 VCC_218
W6 VCC_219
V6 VCC_220
P6 VCC_221
N6 VCC_222
L6 VCC_223
M6 VCC_224
J6 VCC_225
AA5 VCC_226
W5 VCC_227
V5 VCC_228
P5 VCC_229
N5 VCC_230
L5 VCC_231
M5 VCC_232
J5 VCC_233
AA4 VCC_234
W4 VCC_235
V4 VCC_236
P4 VCC_237
N4 VCC_238
L4 VCC_239
M4 VCC_240
J4 VCC_241
AA3 VCC_242
W3 VCC_243
V3 VCC_244
P3 VCC_245
N3 VCC_246
L3 VCC_247
M3 VCC_248
J3 VCC_249
AA2 VCC_250
W2 VCC_251
V2 VCC_252
P2 VCC_253
N2 VCC_254
L2 VCC_255
M2 VCC_256
J2 VCC_257
AA1 VCC_258
W1 VCC_259
V1 VCC_260
P1 VCC_261
N1 VCC_262
L1 VCC_263
M1 VCC_264
J1 VCC_265
AA0 VCC_266
W0 VCC_267
V0 VCC_268
P0 VCC_269
N0 VCC_270
L0 VCC_271
M0 VCC_272
J0 VCC_273
AA33 VCC_274
W33 VCC_275
P33 VCC_276
N33 VCC_277
L33 VCC_278
J33 VCC_279
AA32 VCC_280
W32 VCC_281
V32 VCC_282
P32 VCC_283
N32 VCC_284
L32 VCC_285
M32 VCC_286
J32 VCC_287
AA31 VCC_288
W31 VCC_289
V31 VCC_290
P31 VCC_291
N31 VCC_292
L31 VCC_293
M31 VCC_294
J31 VCC_295
AA30 VCC_296
W30 VCC_297
V30 VCC_298
P30 VCC_299
N30 VCC_300
L30 VCC_301
M30 VCC_302
J30 VCC_303
AA29 VCC_304
W29 VCC_305
V29 VCC_306
P29 VCC_307
N29 VCC_308
L29 VCC_309
M29 VCC_310
J29 VCC_311
AA28 VCC_312
W28 VCC_313
V28 VCC_314
P28 VCC_315
N28 VCC_316
L28 VCC_317
M28 VCC_318
J28 VCC_319
AA27 VCC_320
W27 VCC_321
V27 VCC_322
P27 VCC_323
N27 VCC_324
L27 VCC_325
M27 VCC_326
J27 VCC_327
AA26 VCC_328
W26 VCC_329
V26 VCC_330
P26 VCC_331
N26 VCC_332
L26 VCC_333
M26 VCC_334
J26 VCC_335
AA25 VCC_336
W25 VCC_337
V25 VCC_338
P25 VCC_339
N25 VCC_340
L25 VCC_341
M25 VCC_342
J25 VCC_343
AA24 VCC_344
W24 VCC_345
V24 VCC_346
P24 VCC_347
N24 VCC_348
L24 VCC_349
M24 VCC_350
J24 VCC_351
AA23 VCC_352
W23 VCC_353
V23 VCC_354
P23 VCC_355
N23 VCC_356
L23 VCC_357
M23 VCC_358
J23 VCC_359
AA22 VCC_360
W22 VCC_361
V22 VCC_362
P22 VCC_363
N22 VCC_364
L22 VCC_365
M22 VCC_366
J22 VCC_367
AA21 VCC_368
W21 VCC_369
V21 VCC_370
P21 VCC_371
N21 VCC_372
L21 VCC_373
M21 VCC_374
J21 VCC_375
AA20 VCC_376
W20 VCC_377
V20 VCC_378
P20 VCC_379
N20 VCC_380
L20 VCC_381
M20 VCC_382
J20 VCC_383
AA19 VCC_384
W19 VCC_385
V19 VCC_386
P19 VCC_387
N19 VCC_388
L19 VCC_389
M19 VCC_390
J19 VCC_391
AA18 VCC_392
W18 VCC_393
V18 VCC_394
P18 VCC_395
N18 VCC_396
L18 VCC_397
M18 VCC_398
J18 VCC_399
AA17 VCC_400
W17 VCC_401
V17 VCC_402
P17 VCC_403
N17 VCC_404
L17 VCC_405
M17 VCC_406
J17 VCC_407
AA16 VCC_408
W16 VCC_409
V16 VCC_410
P16 VCC_411
N16 VCC_412
L16 VCC_413
M16 VCC_414
J16 VCC_415
AA15 VCC_416
W15 VCC_417
V15 VCC_418
P15 VCC_419
N15 VCC_420
L15 VCC_421
M15 VCC_422
J15 VCC_423
AA14 VCC_424
W14 VCC_425
V14 VCC_426
P14 VCC_427
N14 VCC_428
L14 VCC_429
M14 VCC_430
J14 VCC_431
AA13 VCC_432
W13 VCC_433
V13 VCC_434
P13 VCC_435
N13 VCC_436
L13 VCC_437
M13 VCC_438
J13 VCC_439
AA12 VCC_440
W12 VCC_441
V12 VCC_442
P12 VCC_443
N12 VCC_444
L12 VCC_445
M12 VCC_446
J12 VCC_447
AA11 VCC_448
W11 VCC_449
V11 VCC_450
P11 VCC_451
N11 VCC_452
L11 VCC_453
M11 VCC_454
J11 VCC_455
AA10 VCC_456
W10 VCC_457
V10 VCC_458
P10 VCC_459
N10 VCC_460
L10 VCC_461
M10 VCC_462
J10 VCC_463
AA9 VCC_464
W9 VCC_465
V9 VCC_466
P9 VCC_467
N9 VCC_468
L9 VCC_469
M9 VCC_470
J9 VCC_471
AA8 VCC_472
W8 VCC_473
V8 VCC_474
P8 VCC_475
N8 VCC_476
L8 VCC_477
M8 VCC_478
J8 VCC_479
AA7 VCC_480
W7 VCC_481
V7 VCC_482
P7 VCC_483
N7 VCC_484
L7 VCC_485
M7 VCC_486
J7 VCC_487
AA6 VCC_488
W6 VCC_489
V6 VCC_490
P6 VCC_491
N6 VCC_492
L6 VCC_493
M6 VCC_494
J6 VCC_495
AA5 VCC_496
W5 VCC_497
V5 VCC_498
P5 VCC_499
N5 VCC_500
L5 VCC_501
M5 VCC_502
J5 VCC_503
AA4 VCC_504
W4 VCC_505
V4 VCC_506
P4 VCC_507
N4 VCC_508
L4 VCC_509
M4 VCC_510
J4 VCC_511
AA3 VCC_512
W3 VCC_513
V3 VCC_514
P3 VCC_515
N3 VCC_516
L3 VCC_517
M3 VCC_518
J3 VCC_519
AA2 VCC_520
W2 VCC_521
V2 VCC_522
P2 VCC_523
N2 VCC_524
L2 VCC_525
M2 VCC_526
J2 VCC_527
AA1 VCC_528
W1 VCC_529
V1 VCC_530
P1 VCC_531
N1 VCC_532
L1 VCC_533
M1 VCC_534
J1 VCC_535
AA0 VCC_536
W0 VCC_537
V0 VCC_538
P0 VCC_539
N0 VCC_540
L0 VCC_541
M0 VCC_542
J0 VCC_543
AA33 VCC_544
W33 VCC_545
P33 VCC_546
N33 VCC_547
L33 VCC_548
J33 VCC_549
AA32 VCC_550
W32 VCC_551
V32 VCC_552
P32 VCC_553
N32 VCC_554
L32 VCC_555
M32 VCC_556
J32 VCC_557
AA31 VCC_558
W31 VCC_559
V31 VCC_560
P31 VCC_561
N31 VCC_562
L31 VCC_563
M31 VCC_564
J31 VCC_565
AA30 VCC_566
W30 VCC_567
V30 VCC_568
P30 VCC_569
N30 VCC_570
L30 VCC_571
M30 VCC_572
J30 VCC_573
AA29 VCC_574
W29 VCC_575
V29 VCC_576
P29 VCC_577
N29 VCC_578
L29 VCC_579
M29 VCC_580
J29 VCC_581
AA28 VCC_582
W28 VCC_583
V28 VCC_584
P28 VCC_585
N28 VCC_586
L28 VCC_587
M28 VCC_588
J28 VCC_589
AA27 VCC_590
W27 VCC_591
V27 VCC_592
P27 VCC_593
N27 VCC_594
L27 VCC_595
M27 VCC_596
J27 VCC_597
AA26 VCC_598
W26 VCC_599
V26 VCC_600
P26 VCC_601
N26 VCC_602
L26 VCC_603
M26 VCC_604
J26 VCC_605
AA25 VCC_606
W25 VCC_607
V25 VCC_608
P25 VCC_609
N25 VCC_610
L25 VCC_611
M25 VCC_612
J25 VCC_613
AA24 VCC_614
W24 VCC_615
V24 VCC_616
P24 VCC_617
N24 VCC_618
L24 VCC_619
M24 VCC_620
J24 VCC_621
AA23 VCC_622
W23 VCC_623
V23 VCC_624
P23 VCC_625
N23 VCC_626
L23 VCC_627
M23 VCC_628
J23 VCC_629
AA22 VCC_630
W22 VCC_631
V22 VCC_632
P22 VCC_633
N22 VCC_634
L22 VCC_635
M22 VCC_636
J22 VCC_637
AA21 VCC_638
W21 VCC_639
V21 VCC_640
P21 VCC_641
N21 VCC_642
L21 VCC_643
M21 VCC_644
J21 VCC_645
AA20 VCC_646
W20 VCC_647
V20 VCC_648
P20 VCC_649
N20 VCC_650
L20 VCC_651
M20 VCC_652
J20 VCC_653
AA19 VCC_654
W19 VCC_655
V19 VCC_656
P19 VCC_657
N19 VCC_658
L19 VCC_659
M19 VCC_660
J19 VCC_661
AA18 VCC_662
W18 VCC_663
V18 VCC_664
P18 VCC_665
N18 VCC_666
L18 VCC_667
M18 VCC_668
J18 VCC_669
AA17 VCC_670
W17 VCC_671
V17 VCC_672
P17 VCC_673
N17 VCC_674
L17 VCC_675
M17 VCC_676
J17 VCC_677
AA16 VCC_678
W16 VCC_679
V16 VCC_680
P16 VCC_681
N16 VCC_682
L16 VCC_683
M16 VCC_684
J16 VCC_685
AA15 VCC_686
W15 VCC_687
V15 VCC_688
P15 VCC_689
N15 VCC_690
L15 VCC_691
M15 VCC_692
J15 VCC_693
AA14 VCC_694
W14 VCC_695
V14 VCC_696
P14 VCC_697
N14 VCC_698
L14 VCC_699
M14 VCC_700
J14 VCC_701
AA13 VCC_702
W13 VCC_703
V13 VCC_704
P13 VCC_705
N13 VCC_706
L13 VCC_707
M13 VCC_708
J13 VCC_709
AA12 VCC_710
W12 VCC_711
V12 VCC_712
P12 VCC_713
N12 VCC_714
L12 VCC_715
M12 VCC_716
J12 VCC_717
AA11 VCC_718
W11 VCC_719
V11 VCC_720
P11 VCC_721
N11 VCC_722
L11 VCC_723
M11 VCC_724
J11 VCC_725
AA10 VCC_726
W10 VCC_727
V10 VCC_728
P10 VCC_729
N10 VCC_730
L10 VCC_731
M10 VCC_732
J10 VCC_733
AA9 VCC_734
W9 VCC_735
V9 VCC_736
P9 VCC_737
N9 VCC_738
L9 VCC_739
M9 VCC_740
J9 VCC_741
AA8 VCC_742
W8 VCC_743
V8 VCC_744
P8 VCC_745
N8 VCC_746
L8 VCC_747
M8 VCC_748
J8 VCC_749
AA7 VCC_750
W7 VCC_751
V7 VCC_752
P7 VCC_753
N7 VCC_754
L7 VCC_755
M7 VCC_756
J7 VCC_757
AA6 VCC_758
W6 VCC_759
V6 VCC_760
P6 VCC_761
N6 VCC_762
L6 VCC_763
M6 VCC_764
J6 VCC_765
AA5 VCC_766
W5 VCC_767
V5 VCC_768
P5 VCC_769
N5 VCC_770
L5 VCC_771
M5 VCC_772
J5 VCC_773
AA4 VCC_774
W4 VCC_775
V4 VCC_776
P4 VCC_777
N4 VCC_778
L4 VCC_779
M4 VCC_780
J4 VCC_781
AA3 VCC_782
W3 VCC_783
V3 VCC_784
P3 VCC_785
N3 VCC_786
L3 VCC_787
M3 VCC_788
J3 VCC_789
AA2 VCC_790
W2 VCC_791
V2 VCC_792
P2 VCC_793
N2 VCC_794
L2 VCC_795
M2 VCC_796
J2 VCC_797
AA1 VCC_798
W1 VCC_799
V1 VCC_800
P1 VCC_801
N1 VCC_802
L1 VCC_803
M1 VCC_804
J1 VCC_805
AA0 VCC_806
W0 VCC_807
V0 VCC_808
P0 VCC_809
N0 VCC_810
L0 VCC_811
M0 VCC_812
J0 VCC_813
AA33 VCC_814
W33 VCC_815
P33 VCC_816
N33 VCC_817
L33 VCC_818
J33 VCC_819
AA32 VCC_820
W32 VCC_821
V32 VCC_822
P32 VCC_823
N32 VCC_824
L32 VCC_825
M32 VCC_826
J32 VCC_827
AA31 VCC_828
W31 VCC_829
V31 VCC_830
P31 VCC_831
N31 VCC_832
L31 VCC_833
M31 VCC_834
J31 VCC_835
AA30 VCC_836
W30 VCC_837
V30 VCC_838
P30 VCC_839
N30 VCC_840
L30 VCC_841
M30 VCC_842
J30 VCC_843
AA29 VCC_844
W29 VCC_845
V29 VCC_846
P29 VCC_847
N29 VCC_848
L29 VCC_849
M29 VCC_850
J29 VCC_851
AA28 VCC_852
W28 VCC_853
V28 VCC_854
P28 VCC_855
N28 VCC_856
L28 VCC_857
M28 VCC_858
J28 VCC_859
AA27 VCC_860
W27 VCC_861
V27 VCC_862
P27 VCC_863
N27 VCC_864
L27 VCC_865
M27 VCC_866
J27 VCC_867
AA26 VCC_868
W26 VCC_869
V26 VCC_870
P26 VCC_871
N26 VCC_872
L26 VCC_873
M26 VCC_874
J26 VCC_875
AA25 VCC_876
W25 VCC_877
V25 VCC_878
P25 VCC_879
N25 VCC_880
L25 VCC_881
M25 VCC_882
J25 VCC_883
AA24 VCC_884
W24 VCC_885
V24 VCC_886
P24 VCC_887
N24 VCC_888
L24 VCC_889
M24 VCC_890
J24 VCC_891
AA23 VCC_892
W23 VCC_893
V23 VCC_894
P23 VCC_895
N23 VCC_896
L23 VCC_897
M23 VCC_898
J23 VCC_899
AA22 VCC_900
W22 VCC_901
V22 VCC_902
P22 VCC_903
N22 VCC_904
L22 VCC_905
M22 VCC_906
J22 VCC_907
AA21 VCC_908
W21 VCC_909
V21 VCC_910
P21 VCC_911
N21 VCC_912
L21 VCC_913
M21 VCC_914
J21 VCC_915
AA20 VCC_916
W20 VCC_917
V20 VCC_918
P20 VCC_919
N20 VCC_920
L20 VCC_921
M20 VCC_922
J20 VCC_923
AA19 VCC_924
W19 VCC_925
V19 VCC_926
P19 VCC_927
N19 VCC_928
L19 VCC_929
M19 VCC_930
J19 VCC_931
AA18 VCC_932
W18 VCC_933
V18 VCC_934
P18 VCC_935
N18 VCC_936
L18 VCC_937
M18 VCC_938
J18 VCC_939
AA17 VCC_940
W17 VCC_941
V17 VCC_942
P17 VCC_943
N17 VCC_944
L17 VCC_945
M17 VCC_946
J17 VCC_947
AA16 VCC_948
W16 VCC_949
V16 VCC_950
P16 VCC_951
N16 VCC_952
L16 VCC_953
M16 VCC_954
J16 VCC_955
AA15 VCC_956
W15 VCC_957
V15 VCC_958
P15 VCC_959
N15 VCC_960
L15 VCC_961
M15 VCC_962
J15 VCC_963
AA14 VCC_964
W14 VCC_965
V14 VCC_966
P14 VCC_967
N14 VCC_968
L14 VCC_969
M14 VCC_970
J14 VCC_971
AA13 VCC_972
W13 VCC_973
V13 VCC_974
P13 VCC_975
N13 VCC_976
L13 VCC_977
M13 VCC_978
J13 VCC_979
AA12 VCC_980
W12 VCC_981
V12 VCC_982
P12 VCC_983
N12 VCC_984
L12 VCC_985
M12 VCC_986
J12 VCC_987
AA11 VCC_988
W11 VCC_989
V11 VCC_990
P11 VCC_991
N11 VCC_992
L11 VCC_993
M11 VCC_994
J11 VCC_995
AA10 VCC_996
W10 VCC_997
V10 VCC_998
P10 VCC_999
N10 VCC_1000
L10 VCC_1001
M10 VCC_1002
J10 VCC_1003
AA9 VCC_1004
W9 VCC_1005
V9 VCC_1006
P9 VCC_1007
N9 VCC_1008
L9 VCC_1009
M9 VCC_1010
J9 VCC_1011
AA8 VCC_1012
W8 VCC_1013
V8 VCC_1014
P8 VCC_1015
N8 VCC_1016
L8 VCC_1017
M8 VCC_1018
J8 VCC_1019
AA7 VCC_1020
W7 VCC_1021
V7 VCC_1022
P7 VCC_1023
N7 VCC_1024
L7 VCC_1025
M7 VCC_1026
J7 VCC_1027
AA6 VCC_1028
W6 VCC_1029
V6 VCC_1030
P6 VCC_1031
N6 VCC_1032
L6 VCC_1033
M6 VCC_1034
J6 VCC_1035
AA5 VCC_1036
W5 VCC_1037
V5 VCC_1038
P5 VCC_1039
N5 VCC_1040
L5 VCC_1041
M5 VCC_1042
J5 VCC_1043
AA4 VCC_1044
W4 VCC_1045
V4 VCC_1046
P4 VCC_1047
N4 VCC_1048
L4 VCC_1049
M4 VCC_1050
J4 VCC_1051
AA3 VCC_1052
W3 VCC_1053
V3 VCC_1054
P3 VCC_1055
N3 VCC_1056
L3 VCC_1057
M3 VCC_1058
J3 VCC_1059
AA2 VCC_1060
W2 VCC_1061
V2 VCC_1062
P2 VCC_1063
N2 VCC_1064
L2 VCC_1065
M2 VCC_1066
J2 VCC_1067

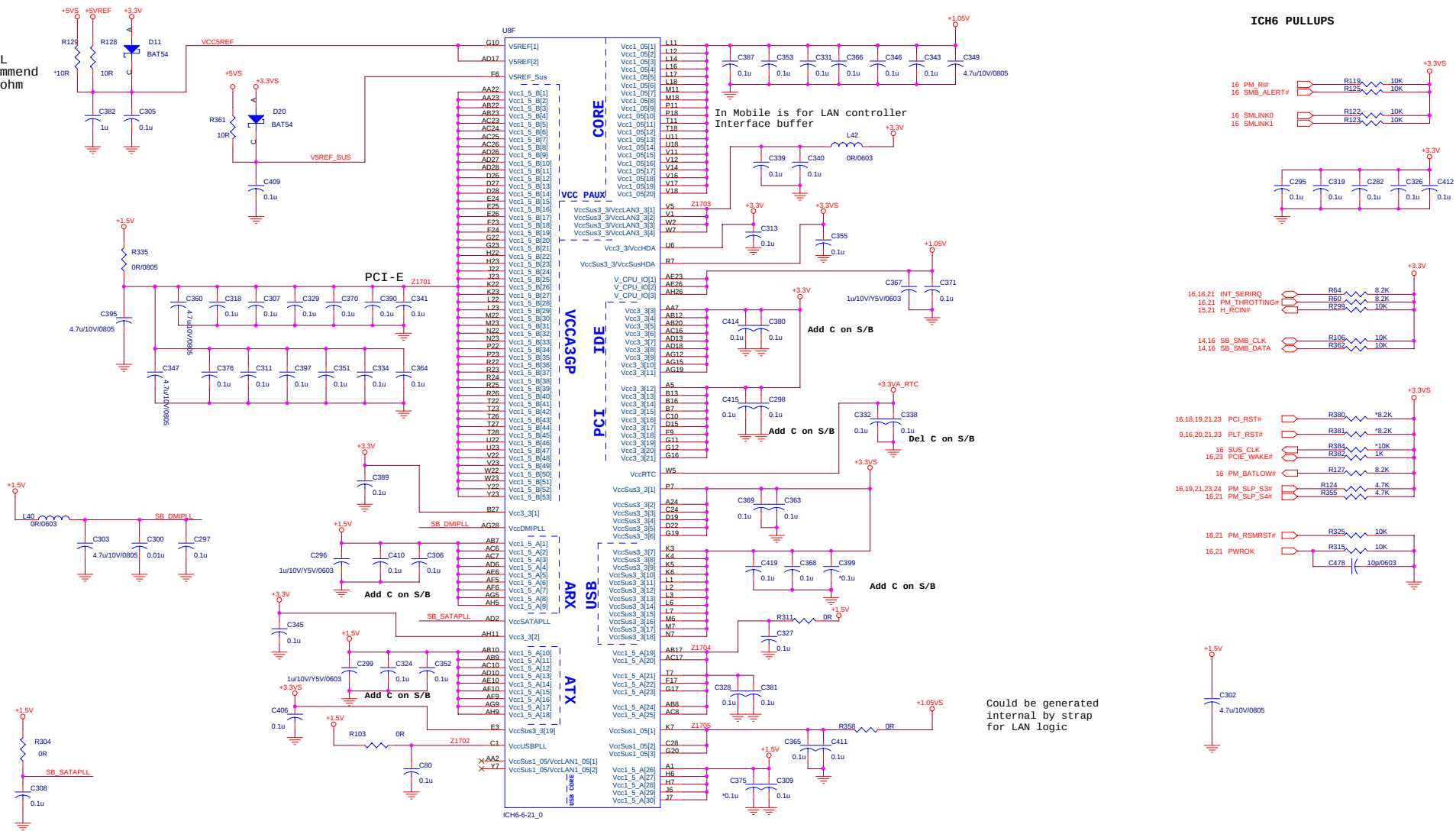


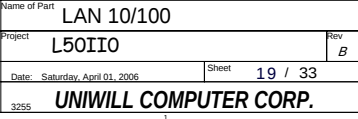
DDR2_Terminate (SWAP RP PIN when layout)



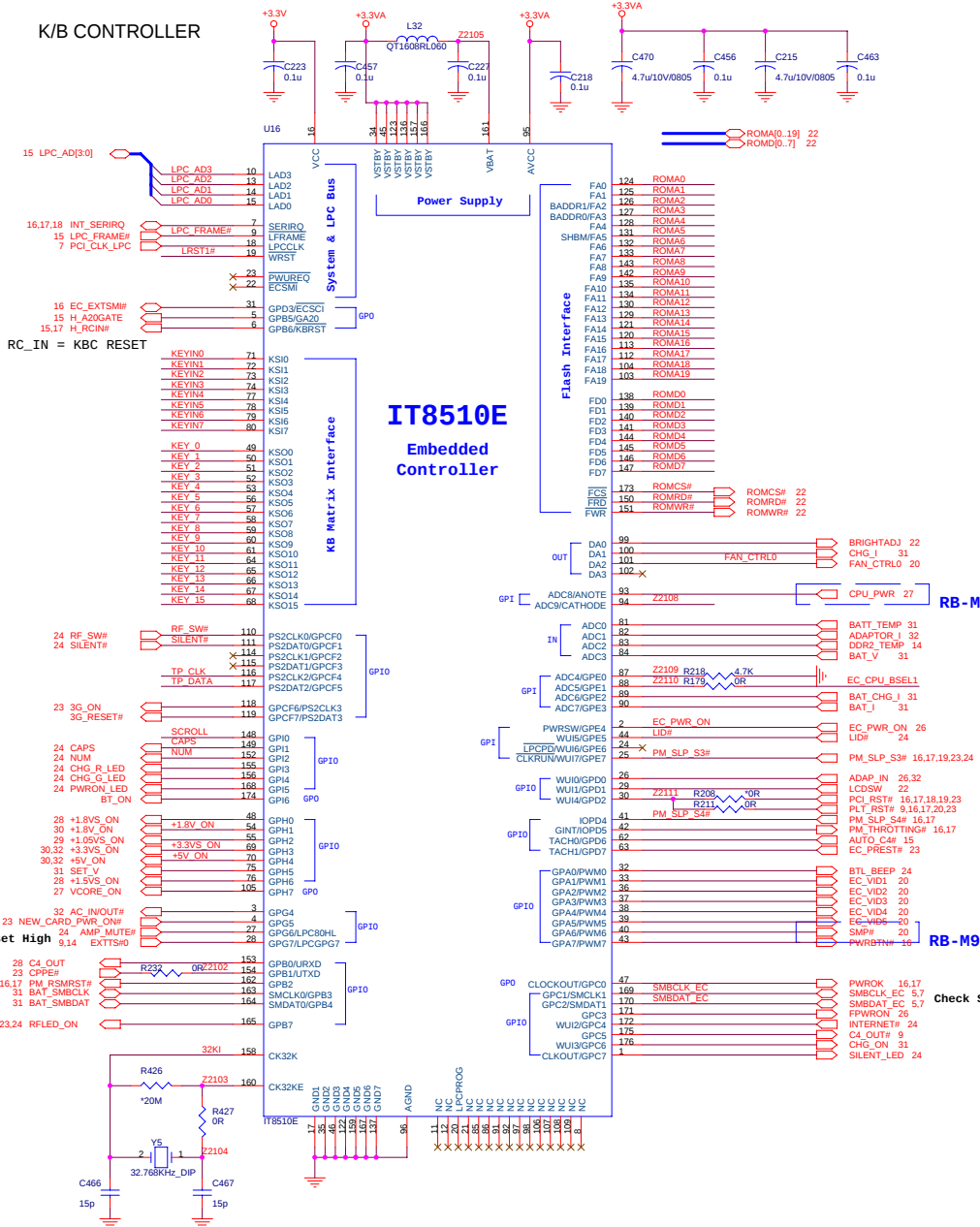


INTEL
recommend
100 ohm

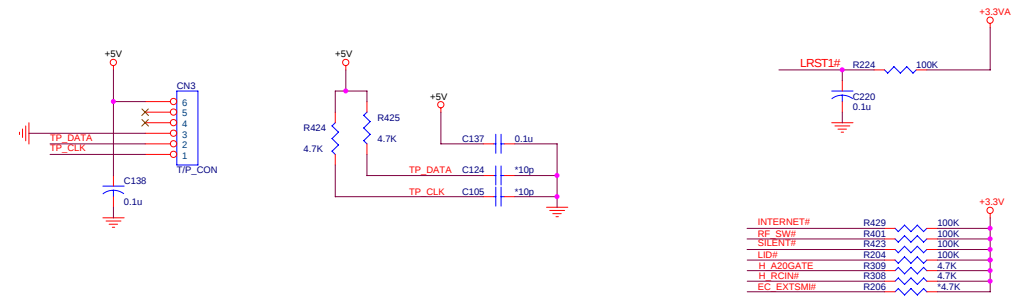




K/B CONTROLLER



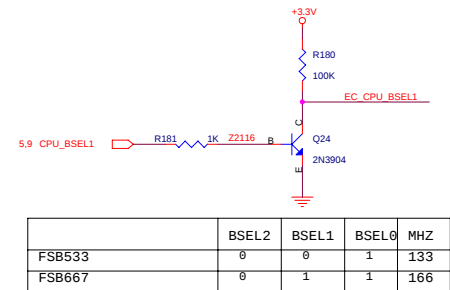
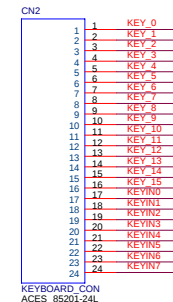
TOUCHPAD CONN



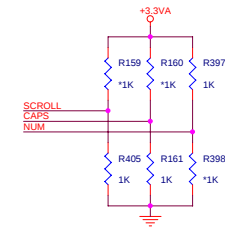
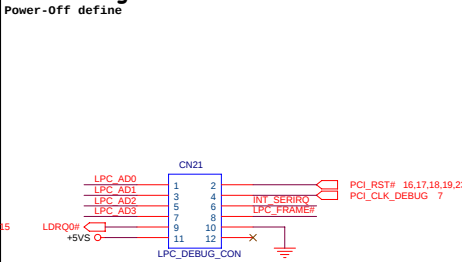
EC SMBUS



Keyboard CONN

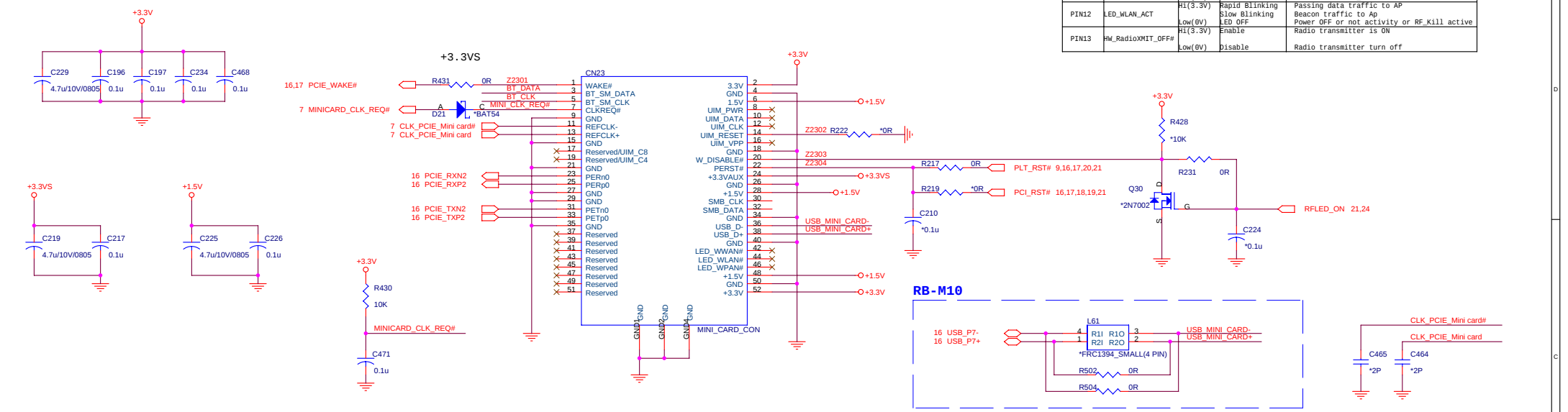


LPC Debug CONN



(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID MODEL
0	0	0	223
0	0	1	245
0	1	0	255
0	1	1	259
1	0	0	P71EN0
1	0	1	P50EN0
1	1	0	XXX
1	1	1	XXX

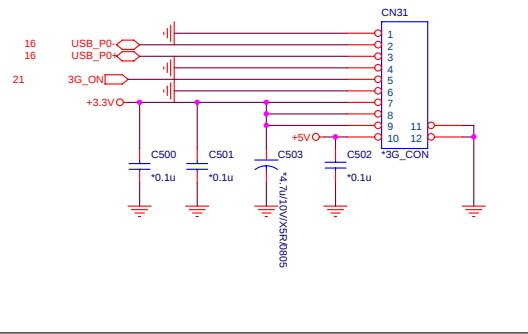
MINI CARD Socket



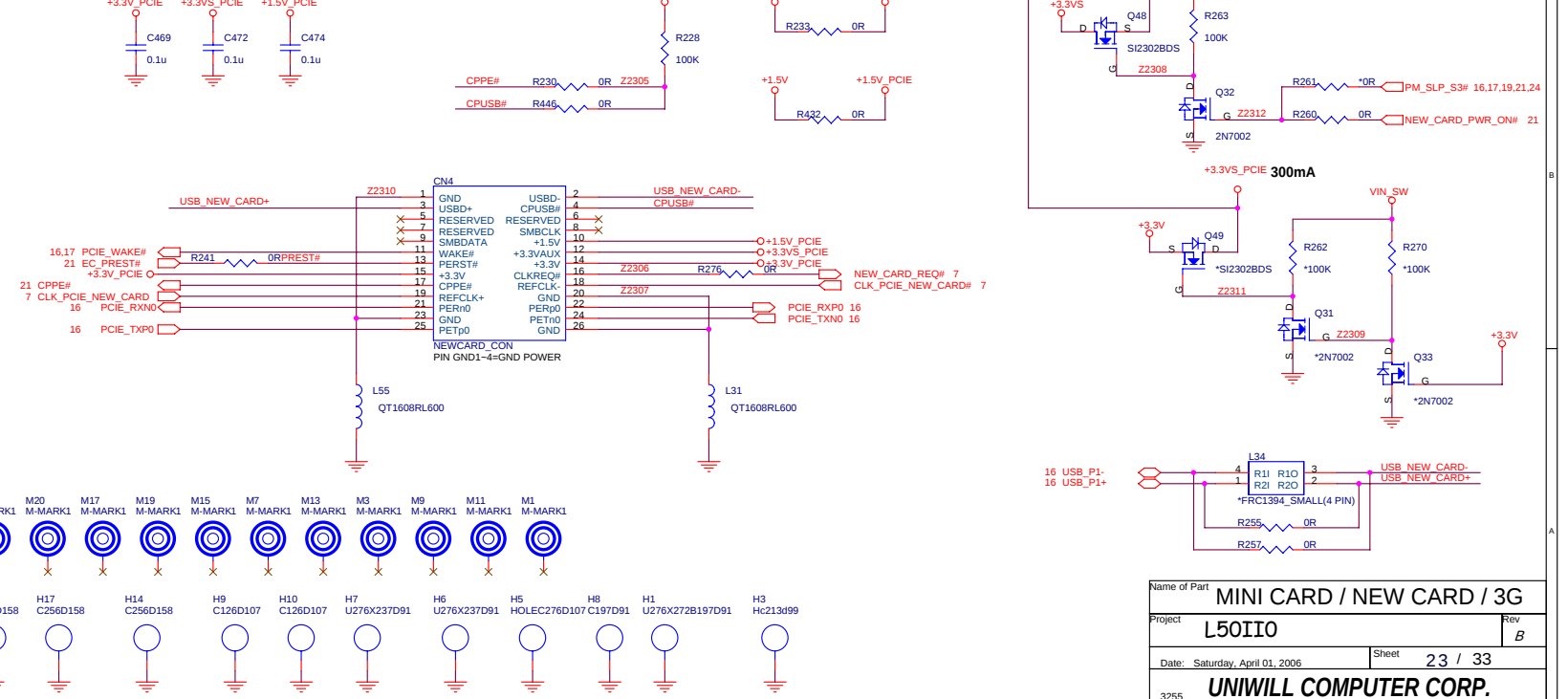
Intel PRO/Wireless 2100 LAN			
PIN11	LED_WLAN_LINK	Hi(3.3V) Low(0V)	Solid ON 8 Flash/3 sec LED OFF
PIN12	LED_WLAN_ACT	Hi(3.3V) Low(0V)	Rapid Blinking Slow Blinking LED OFF
PIN13	HW_RadioXMIT_OFF#	Hi(3.3V) Low(0V)	Enable Disable

Associated AP	Not Associated with an AP
Power OFF or RF_Kill active	Power OFF or RF_Kill active
Passing data traffic to AP	Passing data traffic to AP
Beacon traffic to AP	Beacon traffic to AP
Power OFF or not activity or RF_Kill active	Power OFF or not activity or RF_Kill active
Radio transmitter is ON	Radio transmitter is ON
Radio transmitter turn off	Radio transmitter turn off

3G Module

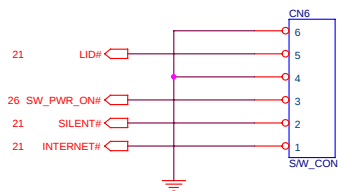


NEW CARD Socket

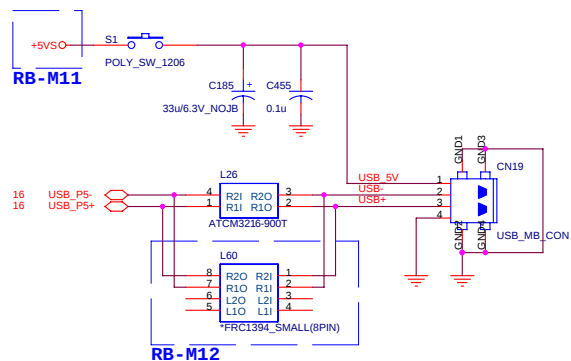


Name of Part	MINI CARD / NEW CARD / 3G	
Project	L50IIO	Rev B
Date:	Saturday, April 01, 2006	Sheet 23 / 33
3255 UNIWILL COMPUTER CORP.		

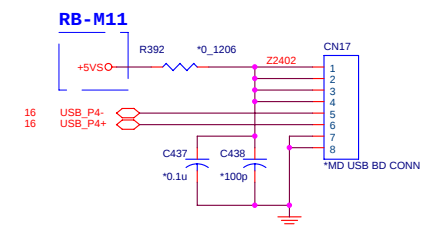
SWITCH BD CONN



ON BOARD USB

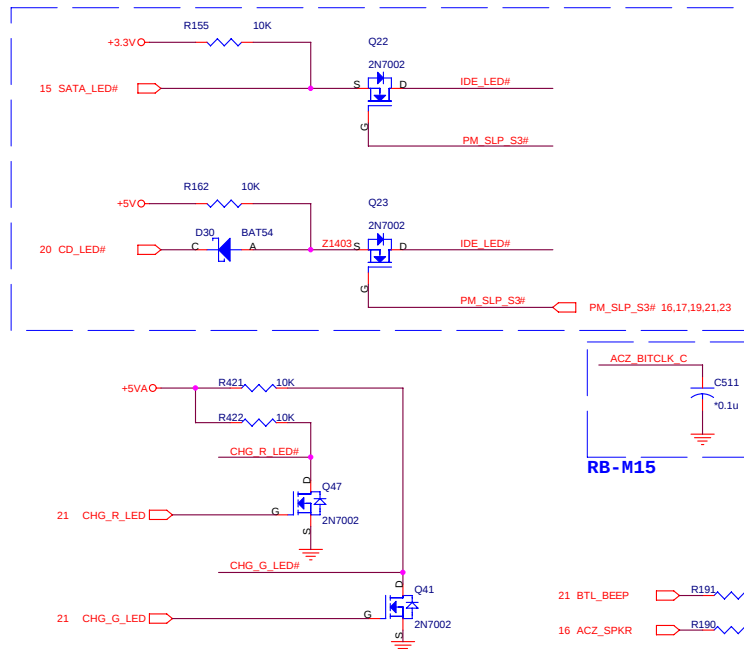


MDC BD's USB Conn

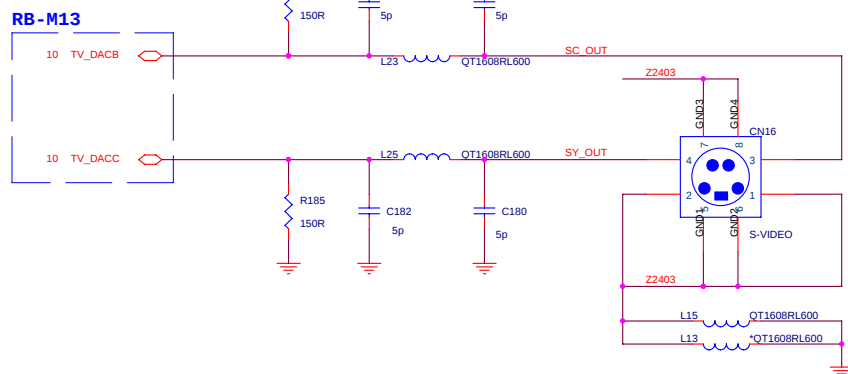


AUDIO & LED BD CONN

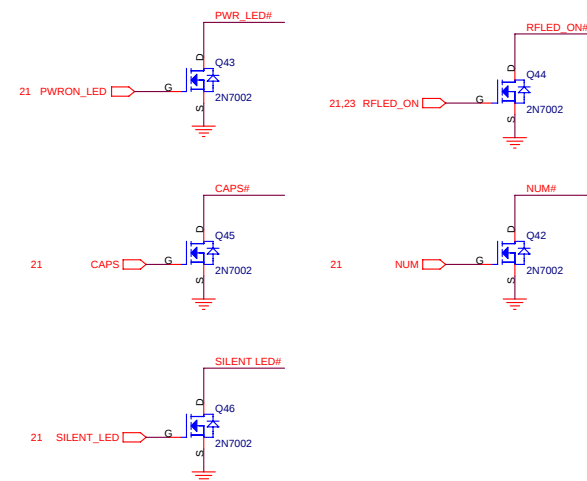
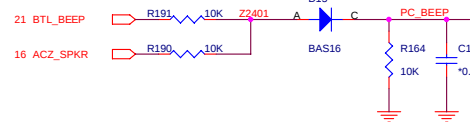
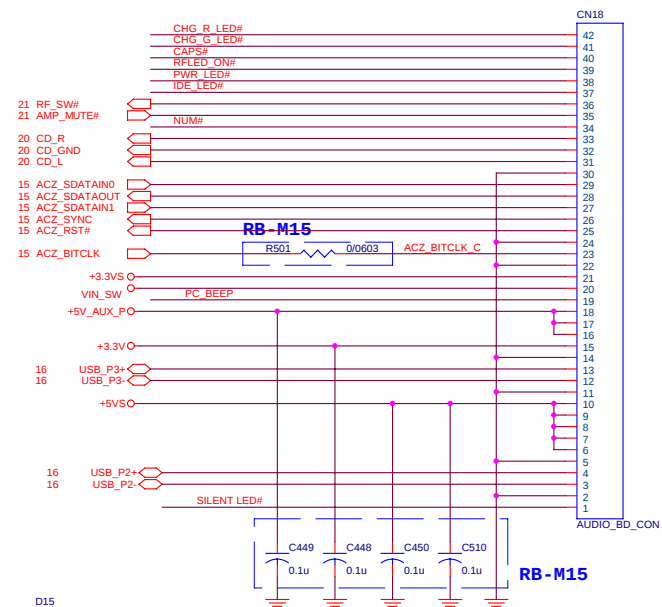
RB-M14

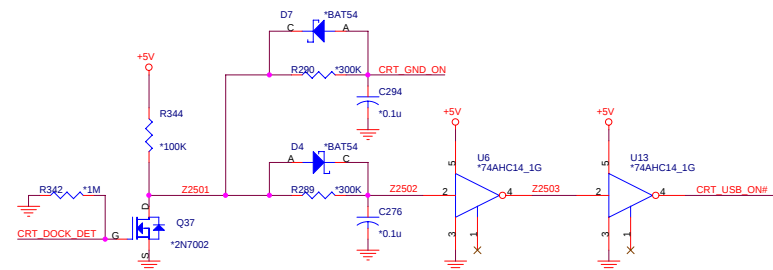
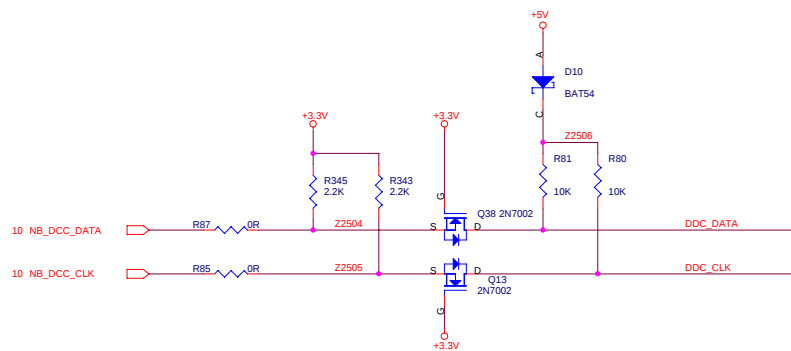
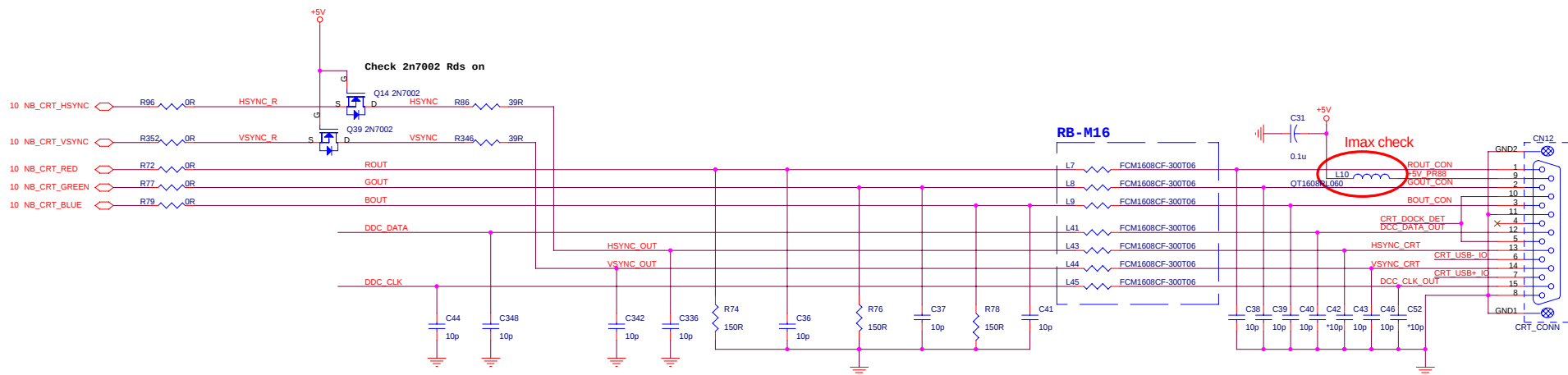


S-Vedio CONN

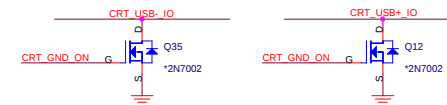


RB-M15

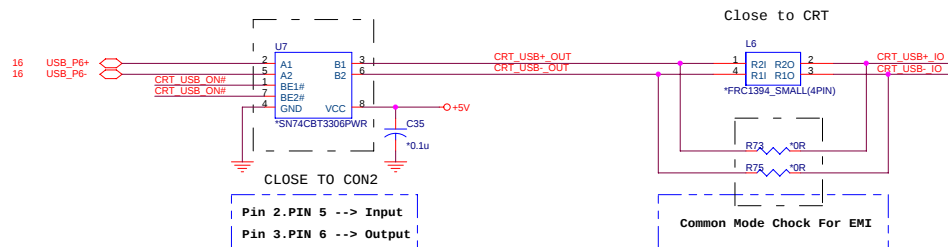




DOCK_DET is Pulled High at Docking Side

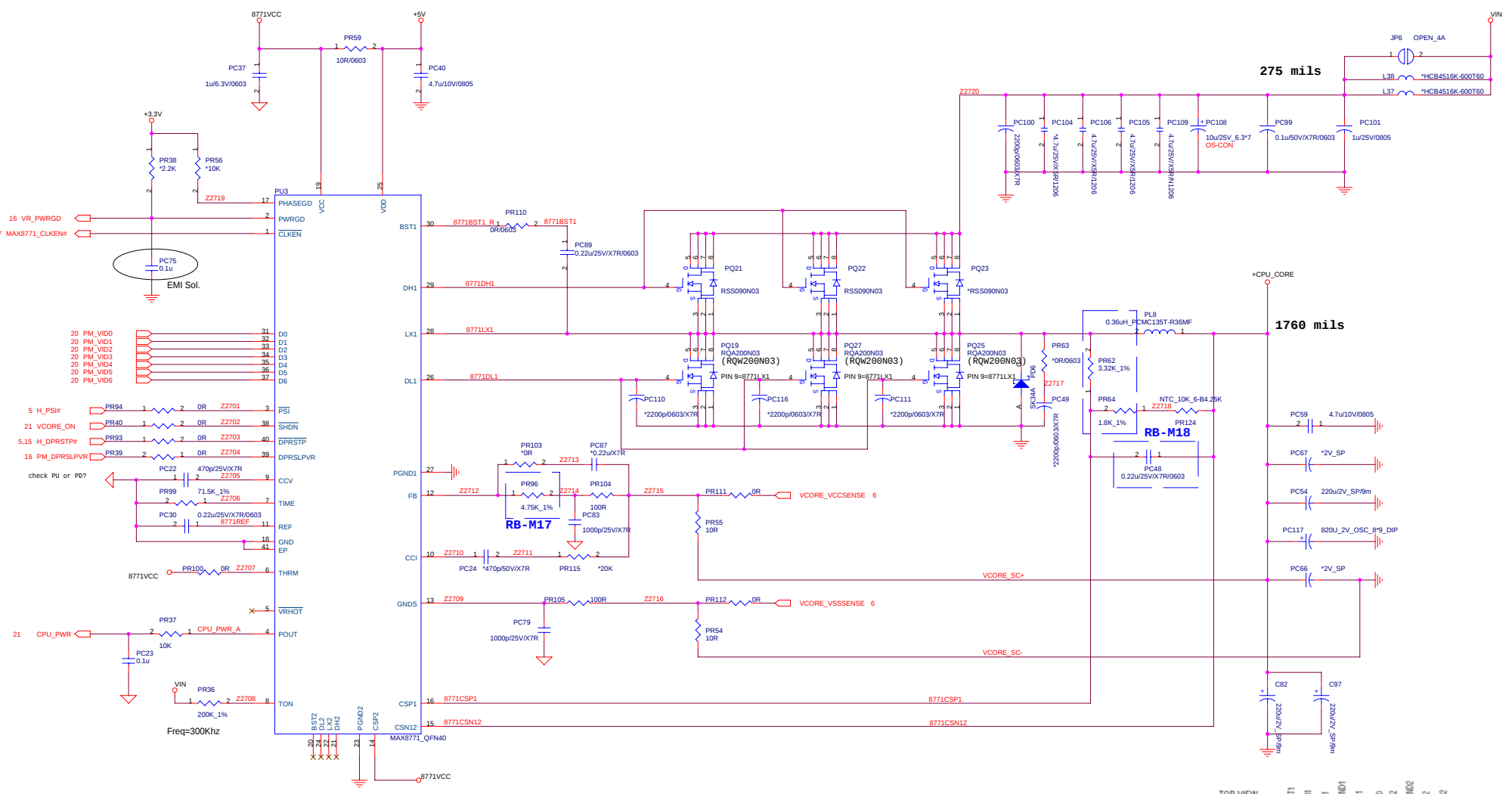


Keep the USB Stub to the MOSFET.Drain as Short as Possible



TC Modify 0914

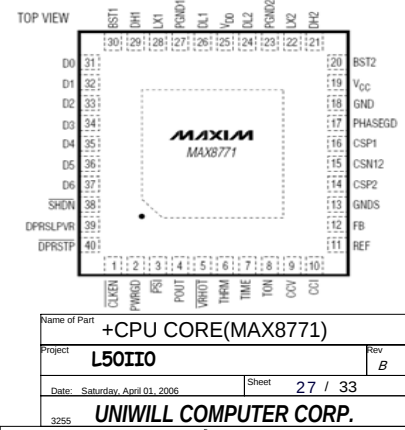
Name of Part	Card Reader	
Project	L50IIO	
Date: Saturday, April 01, 2006	Sheet	25 / 33
3255	UNIWILL COMPUTER CORP.	



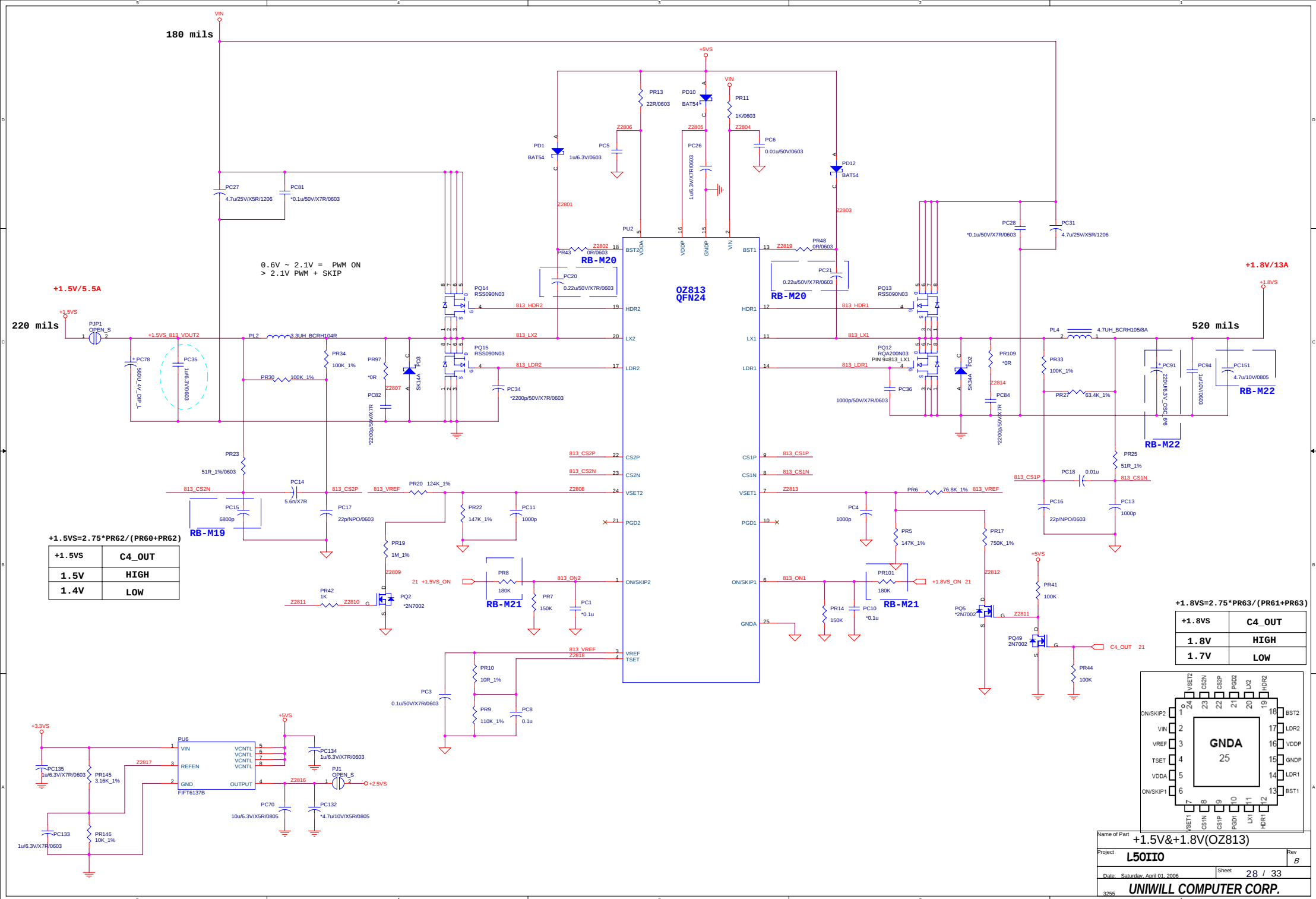
- 1. check PS#&DPRSTP#&DPRSLPVR PU or PD?
- 2. what CAP or R need use 0603?
- 3. CPU vcc-sense & vss-sense?
- 4. Input CAP enough?
- 5. thermal func. disable.NC?
- 6. DGND and AGND problem?
- 7. check CHOKE footprint and hight with ME?
- 8. BST func.?
- 9. TON pull high to Vin or 5V?

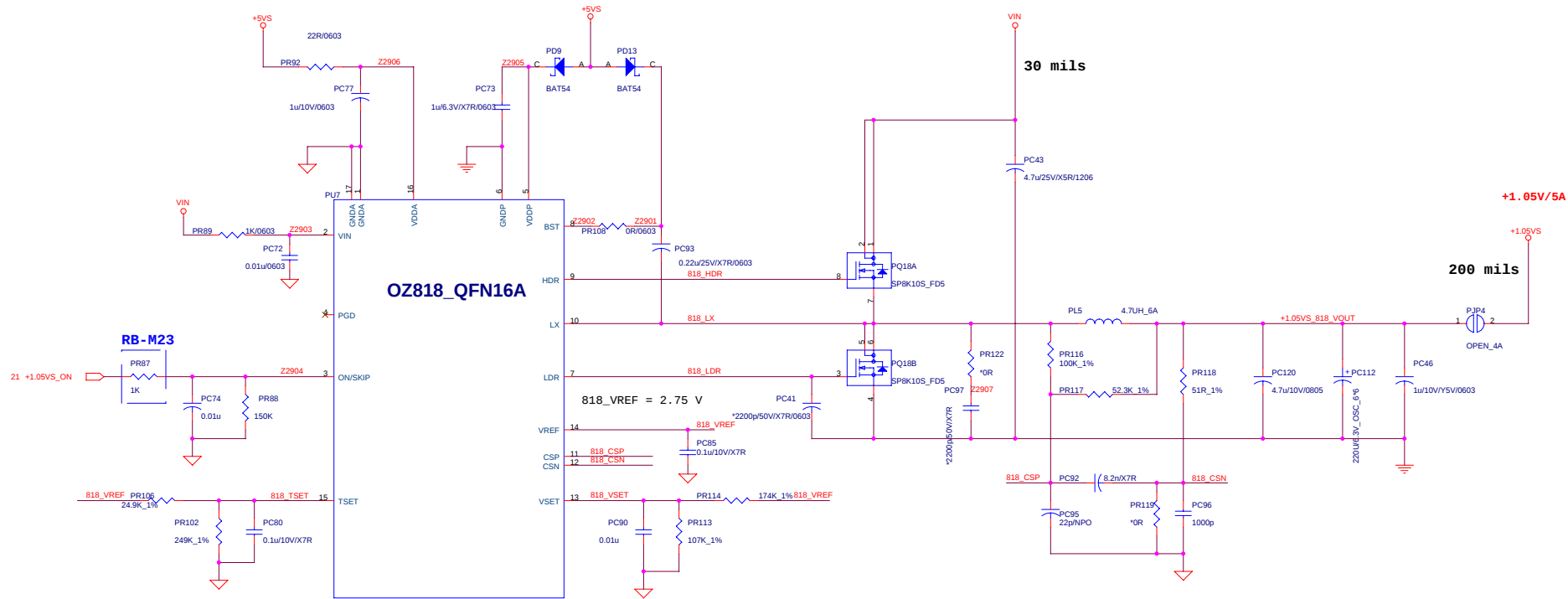
VID TABLE

6	5	4	3	2	1	0	Vcore	Status
0	0	1	0	0	0	1	1.2875	Yonah(HFM)
0	0	1	1	0	0	0	1.2000	Boot Vout
0	0	1	1	1	0	0	1.1500	Merom(HFM)
0	1	1	0	1	0	1	0.8375	Y&M(LFM)
0	1	1	1	0	1	1	0.7625	Y&M(Deeper Sleep)
1	1	1	1	1	1	1	0.0000	Shut down

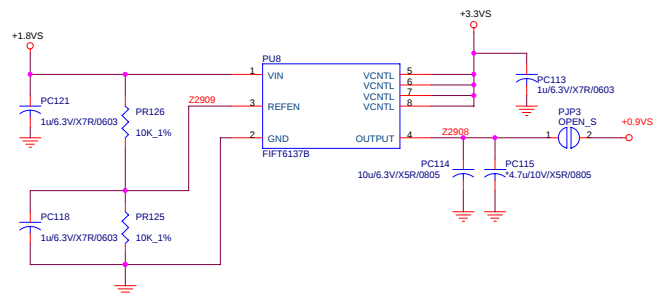


Name of Part		+CPU CORE(MAX8771)	
Project	L50110		Rev
Date:	Saturday, April 01, 2006	Sheet	27 / 33
UNIWILL COMPUTER CORP.			

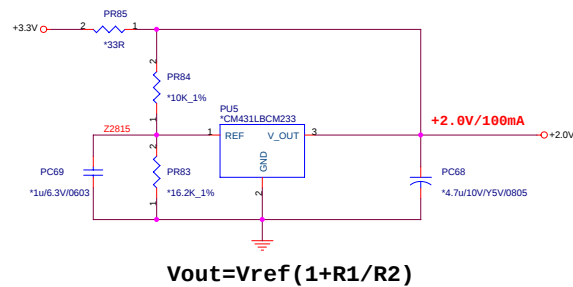




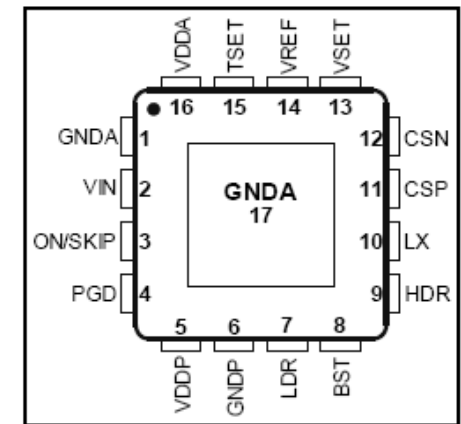
DDR2 Termination Power



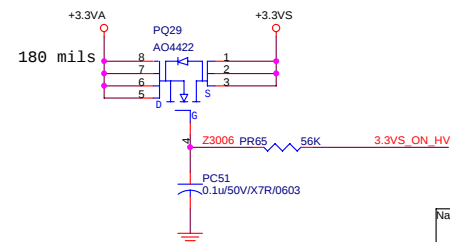
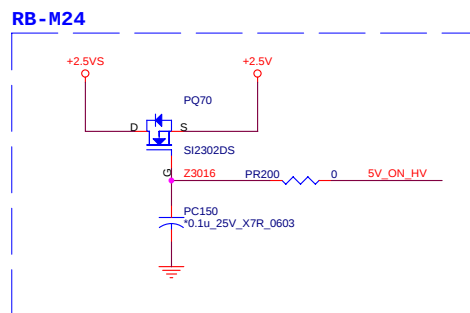
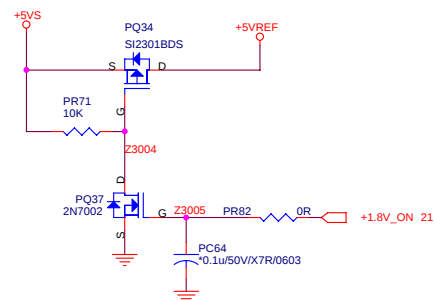
Reserve for 1394 core power

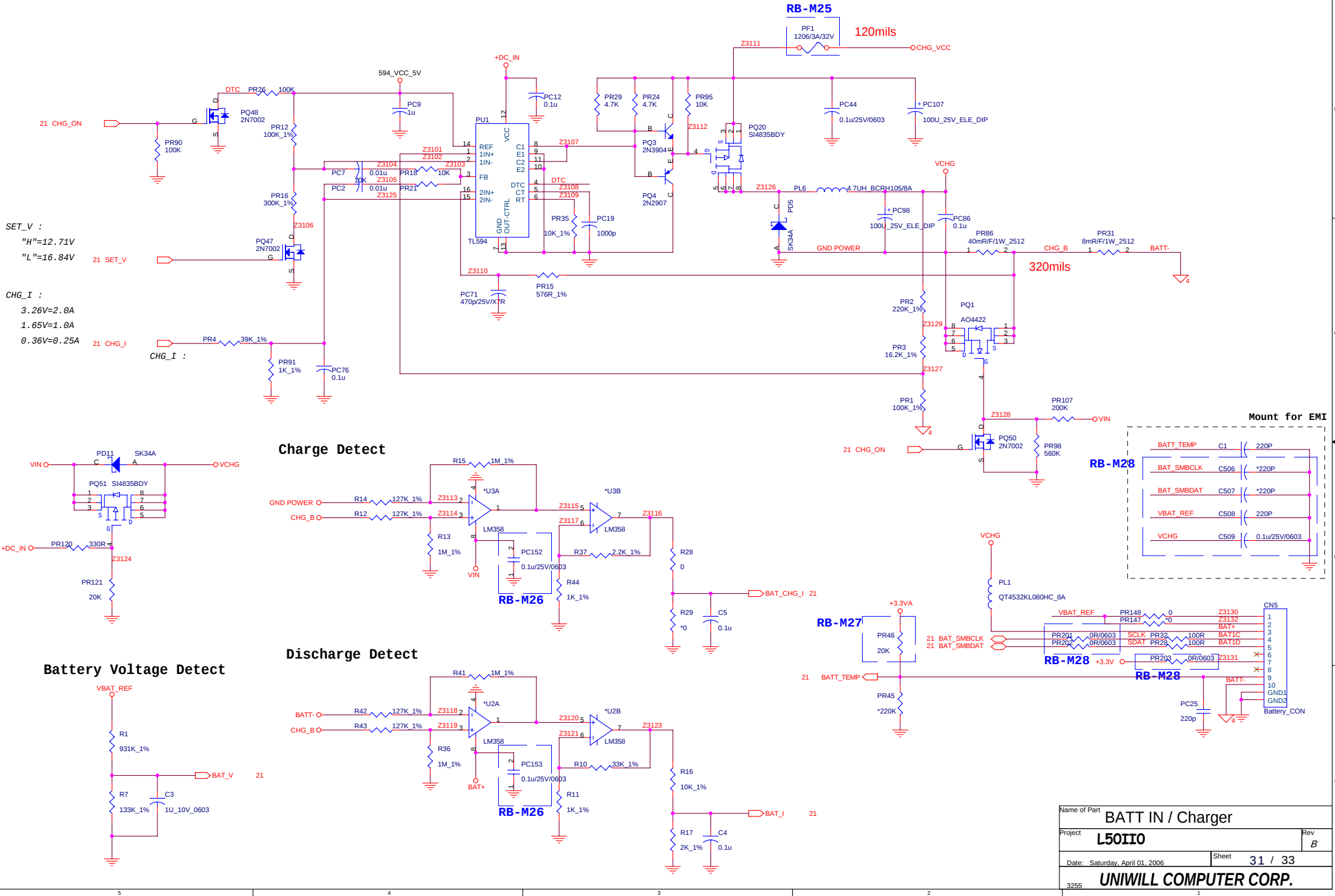


$$V_{out} = V_{ref} (1 + R1/R2)$$

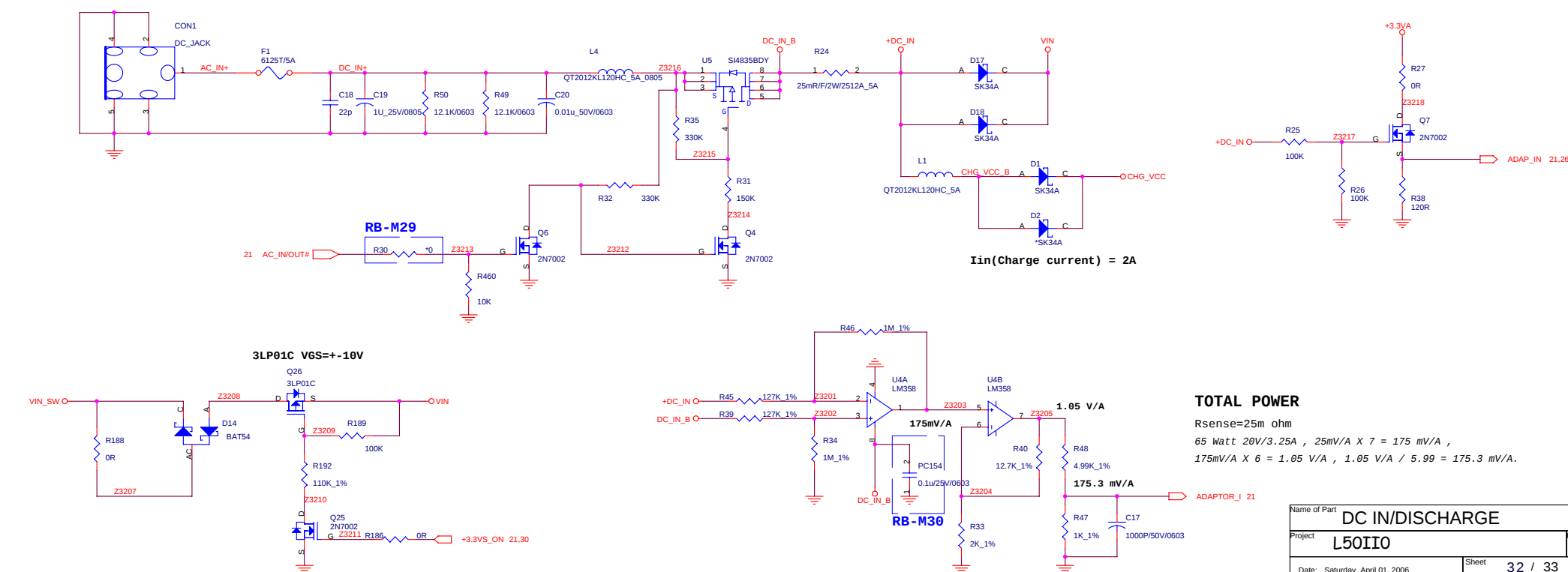
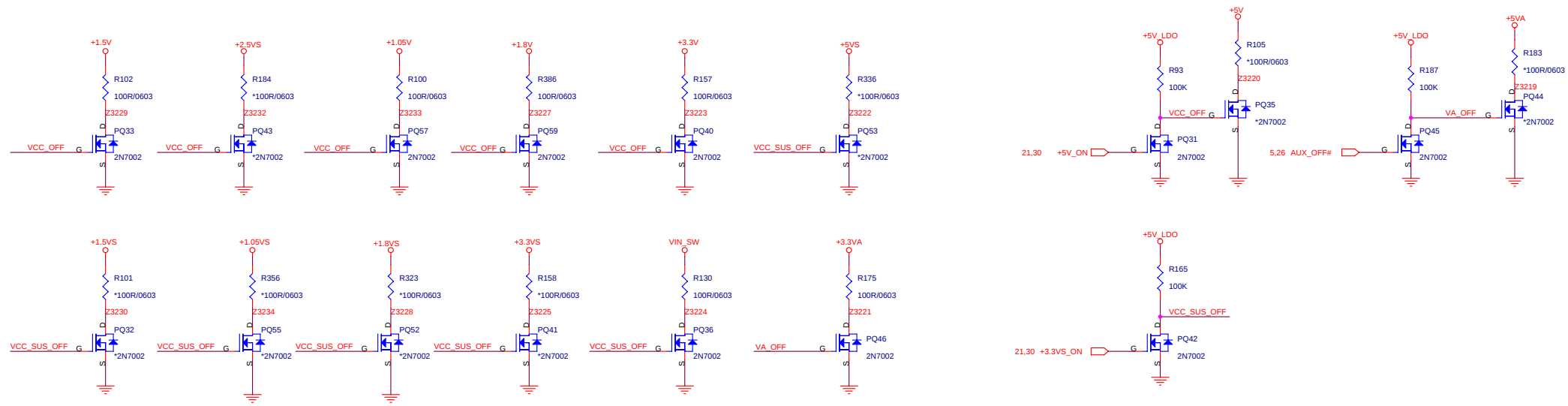


Name of Part	+0.9VS/+1.05V(OZ818)	
Project	L50IIIO	Rev B
Date:	Sunday, April 02, 2006	Sheet 29 / 33
3255 UNIWILL COMPUTER CORP.		





Name of Part	BATT IN / Charger	
Project	L50IIO	Rev B
Date: Saturday, April 01, 2006	Sheet	31 / 33
3255	UNIWILL COMPUTER CORP.	



Name of Part			DC IN/DISCHARGE
Project	L50IIO	Rev	B
Date:	Saturday, April 01, 2006	Sheet	32 / 33
3255 UNIWILL COMPUTER CORP.			

RA to RB change list:

- Page 7,M1->change net name for LAN clock.
Page 9,M2->Add cap. for EMI solution.
Page 15,M3->Change R329 to 47 ohm for EMI solution.
Page 18,M4->Del bead to GND for ESD solution.
Page 19,M5->Change transformer for LAN function.
Page 19,M6->Add R500 for IRQA or IRQB selection.
Page 20,M7->Add circuit for SMP.
Page 21,M8->Add CPU_PWR pin to EC for CPU vlotage detection function.
Page 21,M9->Change pin name for SMP.
Page 23,M10->Add USB signal for mini_card.
Page 24,M11->Change USB port power source.
Page 24,M12->Reserve common choke for EMI test.
Page 24,M13->Change TV signal for right design.
Page 24,M14->Change HDD LED circuit for flash function.
Page 24,M15->Add cap. and resister for EMI solution.
Page 25,M16->Change CRT signal bead for signal quality.
Page 27,M17->Addjust CPU PWR load line.
Page 27,M18->Addjust CPU PWR OCP point.
Page 28,M19->Change PC15 to 6800pf for vset2 ccuracy.
Page 28,M20->Change cap. from 0.1uf to 0.22uf for LX accuracy.
Page 28,M21->Disable skip mode.
Page 28,M22->Add PC151 and change PC91 to solve PWR ripple over spec. issue.
Page 29,M23->Change PR87 to 1K ohm for skip mode function.
Page 30,M24->Add PQ70 for +2.5VS and +2.5V switch.
Page 31,M25->Change PF1 type to 1A/32V.
Page 31,M26->Add cap. for OP input power.
Page 31,M27->Change PR46 to 20K ohm for bat temp.
Page 31,M28->Add Res. for EMI solution.
Page 32,M29->Disable AC IN / OUT function.
Page 32,M30->Add cap. for OP input power.
Page 15,M31->Add cap. for EMI solution.

Name of Part		Every Ver. Histor	
Project		L50II0	Rev B
Date: Saturday, April 01, 2006		Sheet 33 / 33	
3255		UNIWILL COMPUTER CORP.	