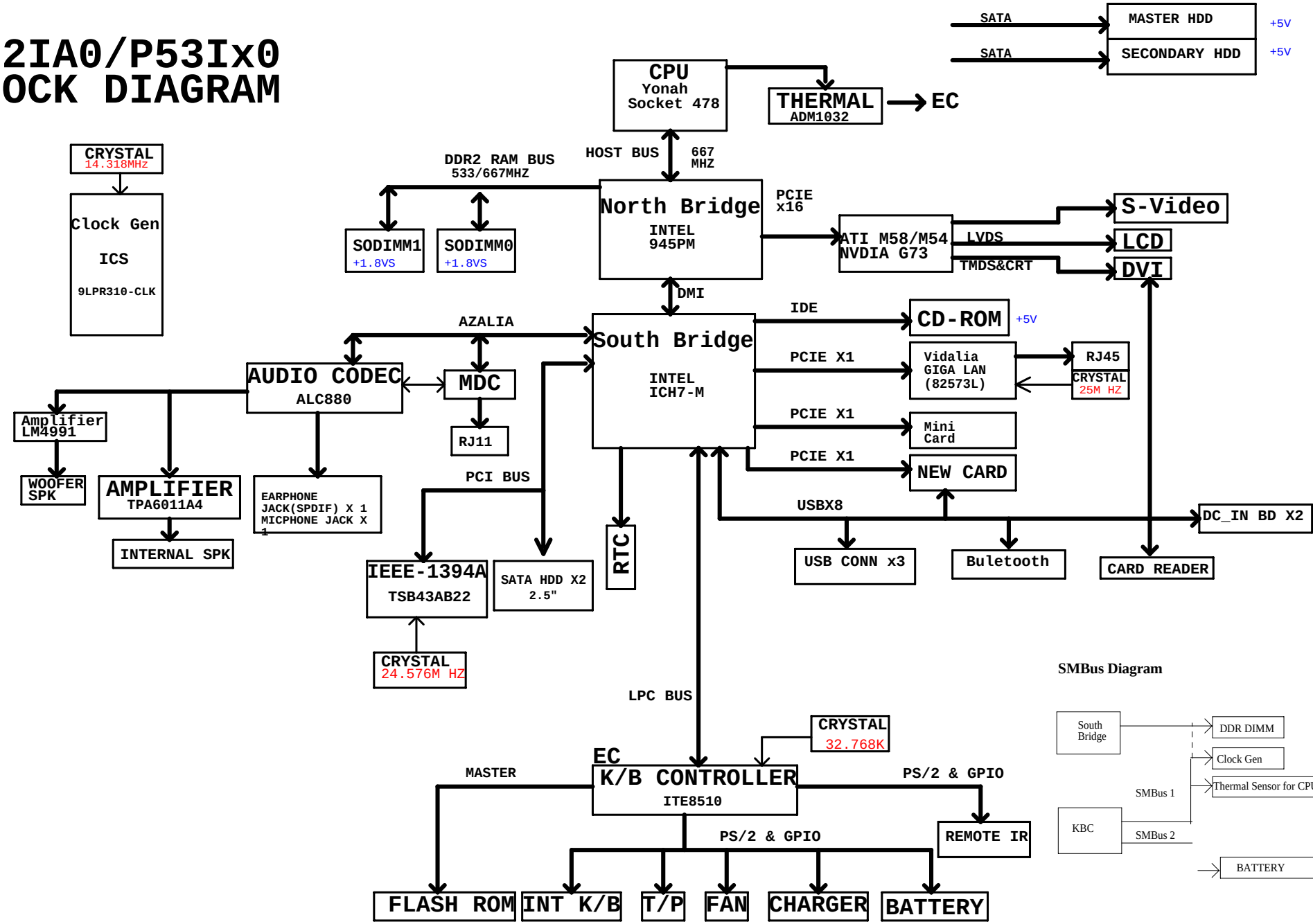
Model : P72IA0

Intel Yonah CPU + 945PM / ICH7-M Chipset

Revision History		
	09/2005	RA
	11/2005	RB
	12/2005	RC

UNIWILL COMPUTER CORP.		
Title: P53IA0		
Size	Document Number: 3220 INDEX	Rev: C
Date: Monday, February 06, 2006	Sheet 1 of 33	

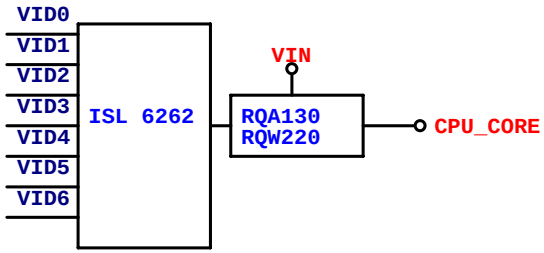
P72IA0/P53Ix0 BLOCK DIAGRAM

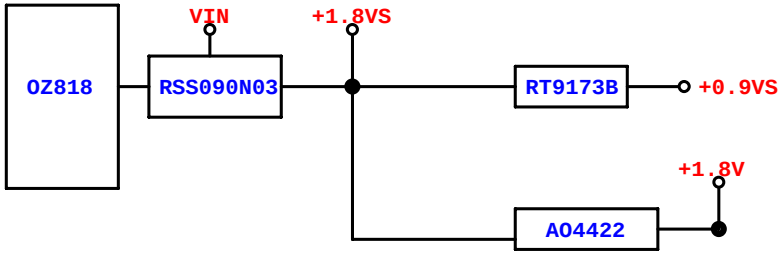


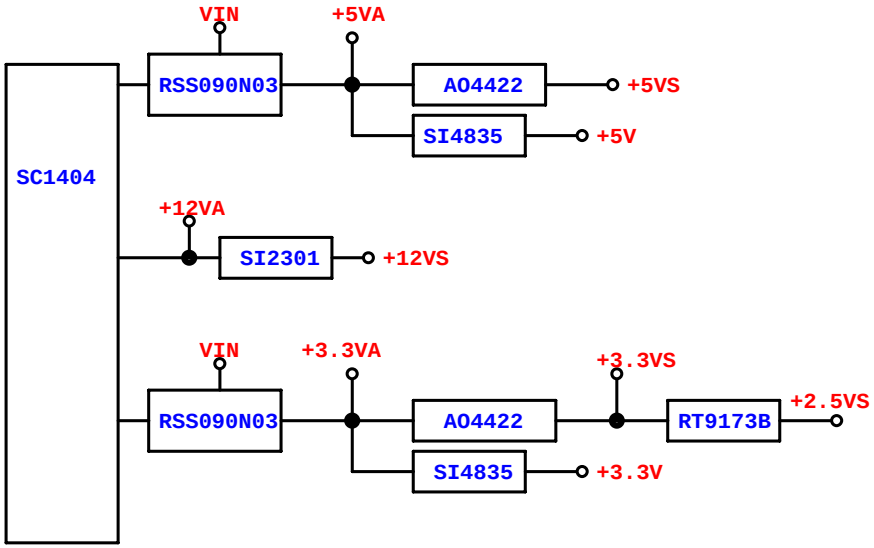
SMBus Diagram

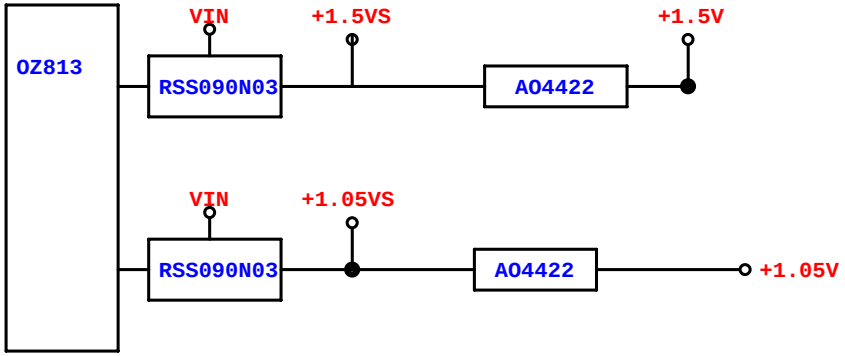
UNIWILL COMPUTER CORP.		
Title: P53IA0		
Size	Document Number: 3220 SYSTEM BLOCK DIAGRAM	Rev C
Date: Monday, February 06, 2006	Sheet 2 of 33	

POWER BLOCK DIAGRAM

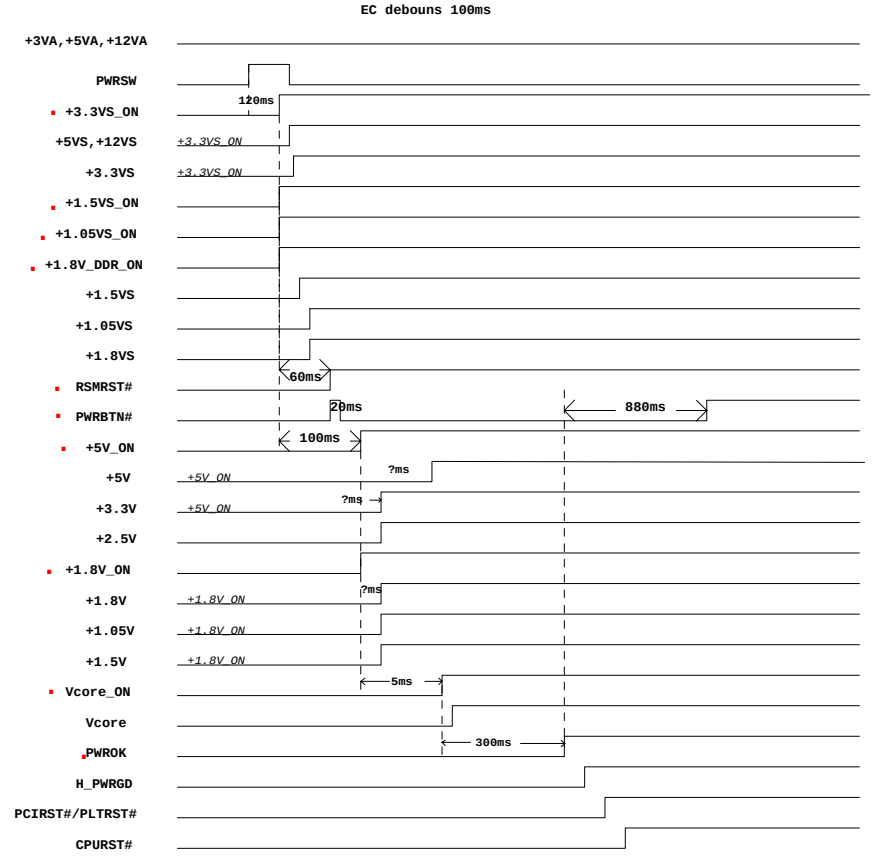








POWER Sequence



▪ EC Control Pin

UNIWILL COMPUTER CORP.		
Title: P53IA0		
Size: C	Document Number: 3220 POWER DIAGRAM	Rev: C
Date: Monday, February 06, 2006	Sheet 3 of 33	

ICH6-M GPIO

GPI0	BM_BUSY#
GP7	
GP8	EC_EXTSMI#
GPI11	SMB_ALERT#
GPI12	
GPI13	
GPO18	PM_STPPCI_ICH#
GPO19	
GPO20	PM_STPCPU_ICH#
GPO21	TPM_EN
GPO23	
GPIO24	
GPIO25	
GPIO26	SATA0_GP
GPIO27	
GPIO28	
GPIO29	PNLSW1
GPIO30	PNLSW2
GPIO31	PNLSW0
GPIO32	PM_CLKRUN#
GPIO33	
GPIO34	

ITE8510E GPIO

GPCF0	RF_SW#
GPCF1	SILENT#/
GPCF2	IR_PS2CLK1
GPCF3	IR_PS2DAT1
GPCF4	TP_CLK
GPCF5	TP_DATA
GPCF6	MAIL#
GPCF7	BROWSER#
GPI0	SCROLL#
GPI1	CAPS#
GPI2	NUM#
GPI3	CHG_R_LED#
GPI4	CHG_G_LED#
GPI5	SUSLED_LED#
GPI6	***VOLMAX***
GPH0	+1.8V_DDR_ON
GPH1	+1.8V_ON
GPH2	+1.05VS_ON
GPH3	+3.3VS_ON
GPH4	+5V_ON
GPH5	SET_V
GPH6	+1.5VS_ON
GPH7	VCORE_ON
GPG4	TP_DISABLE
GPG5	LCDSW
GPG6	MUTE#
GPG7	EXTTS#0
GPB0	CELERON_VO_DET
GPB1	CPPE#
GPB2	PM_RSMRST#
GPB3	BAT_SMBCLK
GPB4	BAT_SMBDAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	RFLED_ON#
GPE0	***NA***
GPE1	CPU_BSEL0
GPE2	***NA***
GPE3	***NA***
GPE4	PWRSW
GPE5	LID#
GPE6	PCM#
GPE7	PM_SLP_S3#
GPD0	ADAP_IN
GPD1	REMOTE_ON#
GPD2	PCI_RST#/PLT_RST#
GPD3	EC_EXTSMI#
GPD4	PM_SLP_S4#
GPD5	PM_THROTTLING#
GPD6	FAN_SPD#
GPD7	EC_PREST#
GPA0	BTL_BEEP
GPA1	EC_VID1
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	SMP1_EN#
GPA6	SMP2_EN#
GPA7	PWRBTN#

ITE8510E GPIO

GPC0	PWROK
GPC1	BAT2_SMBCLK
GPC2	BAT2_SMBDAT
GPC3	SB_ALERT#1
GPC4	SB_ALERT#2
GPC5	TP_LED#
GPC6	CHG_ON
GPC7	SILENT_LED#
ADC0	BAT_TEMP
ADC1	ADAPTOR_I
ADC2	DDR2_TEMP
ADC3	VGA_TEMP
DAC0	BRIGHTADJ
DAC1	CHG_I
DAC2	FAN_CTRL0
DAC3	***NA***

CPU

	CPU CORE(V)	ICC(mA)	W	TEMP(℃)
2.0G	1.525	35.7	54.3	69
2.2G	1.525	37.5	57.1	70
2.26G	1.525	38.1	58.0	70
2.4G	1.525	39.3	59.8	71
2.5G	1.525	40	61.0	72
2.53G	1.525	40.4	61.5	72
2.6G	1.525	41.05	62.6	72
2.66G	1.525	43.35	66.1	74
2.8G	1.525	44.86	68.4	75
3.06G	1.525	55.9	85.2	81

MCHE

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	108.19	0.357	70
+3.3VA	501.3	1.254	
+2.5V	1390	2.502	
+1.5V	33.4	0.084	
+VCCP	10	0.018	
+VCC_GMCH_CORE	266	0.452	

ICH6-M

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	96	0.315	70
+3.3VA	275	0.909	
+1.5V	487	0.876	
+1.5VA	27	0.049	
+3.3VA_RTC	0.003	0.00001	

ITE8510E

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	300	1	70

CLOCK GENERATOR

VCC	ICC(mA)	W	TEMP(℃)
+3.3V	180	0.594	70

ALC880

VCC	ICC(mA)	W	TEMP(℃)
+3.3V(DVDD)	71	0.234	70

TPA6011A4

VCC	ICC(mA)	W	TEMP(℃)
3.3V	30	0.099W	85

ADM1032

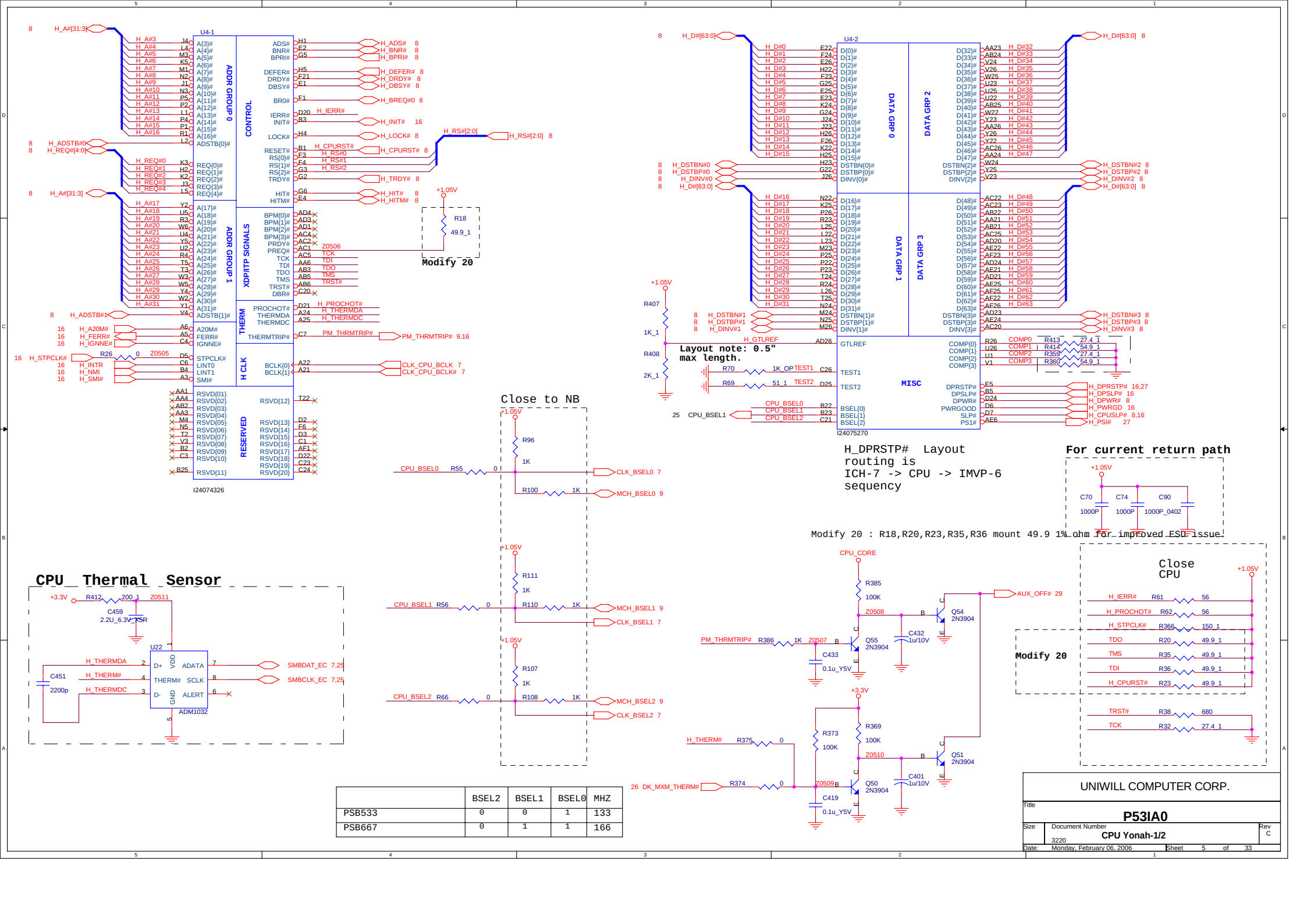
VCC	ICC	W	TEMP(℃)
+3.3V	170uA	0.56mW	150

UNIWILL COMPUTER CORP.

Title: P53IA0

Size: C | Document Number: 3220 GPIO & POWER CONSU | Rev: C

Date: Monday, February 06, 2006 | Sheet 4 of 33



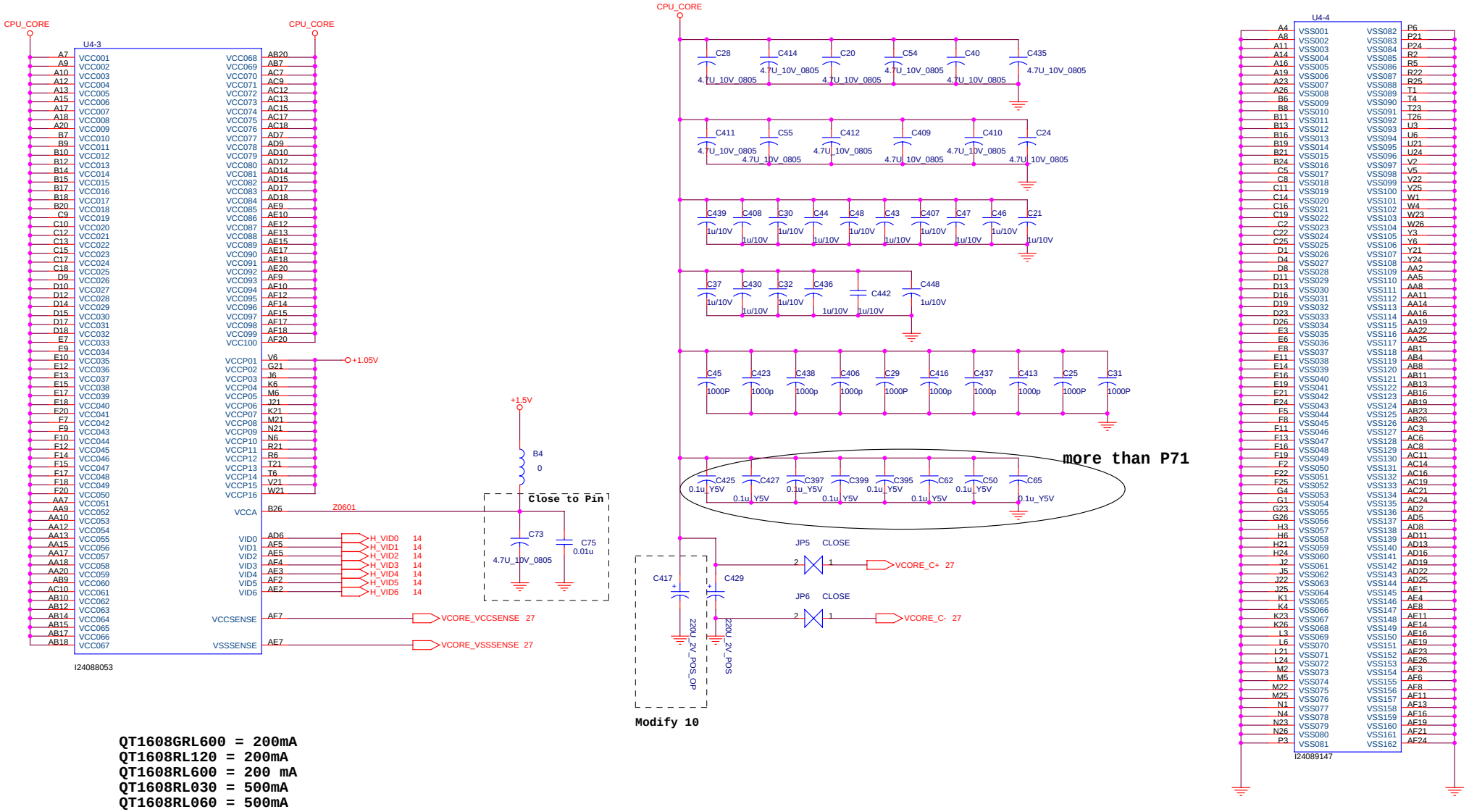
	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

UNIWILL COMPUTER CORP.

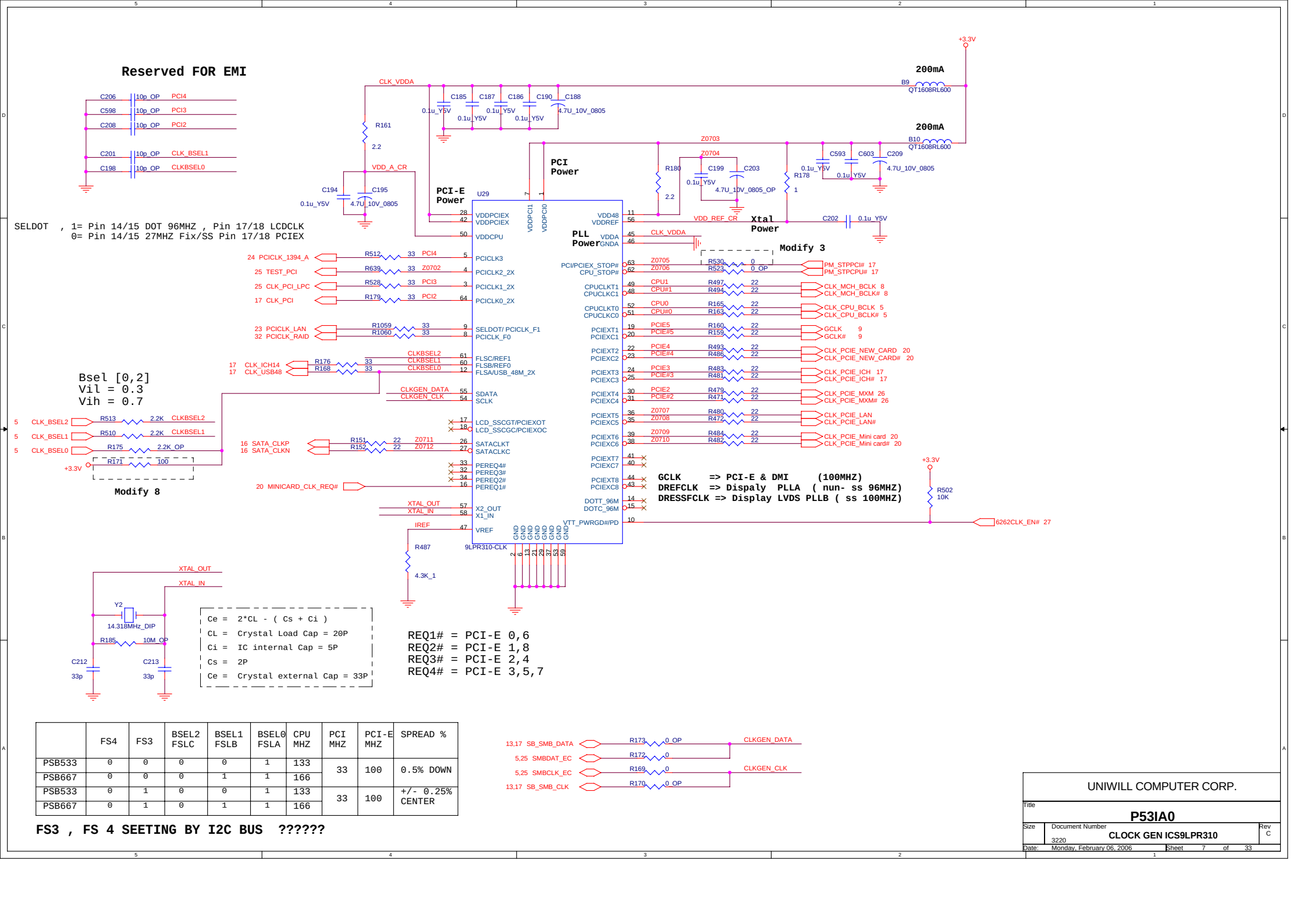
Title: **P53IA0**

Size: 3220 | Document Number: CPU Yonah-1/2 | Rev: C

Date: Monday, February 06, 2006 | Sheet 5 of 33



UNIWILL COMPUTER CORP.	
Title	P53IA0
Size	Document Number: CPU Yonah-2/2 (3220) — Rev C
Date: Monday, February 06, 2006	Sheet 6 of 33



	FS4	FS3	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ	SPREAD %
PSB533	0	0	0	0	1	133	33	100	0.5% DOWN
PSB667	0	0	0	1	1	166			
PSB533	0	1	0	0	1	133	33	100	+/- 0.25% CENTER
PSB667	0	1	0	1	1	166			

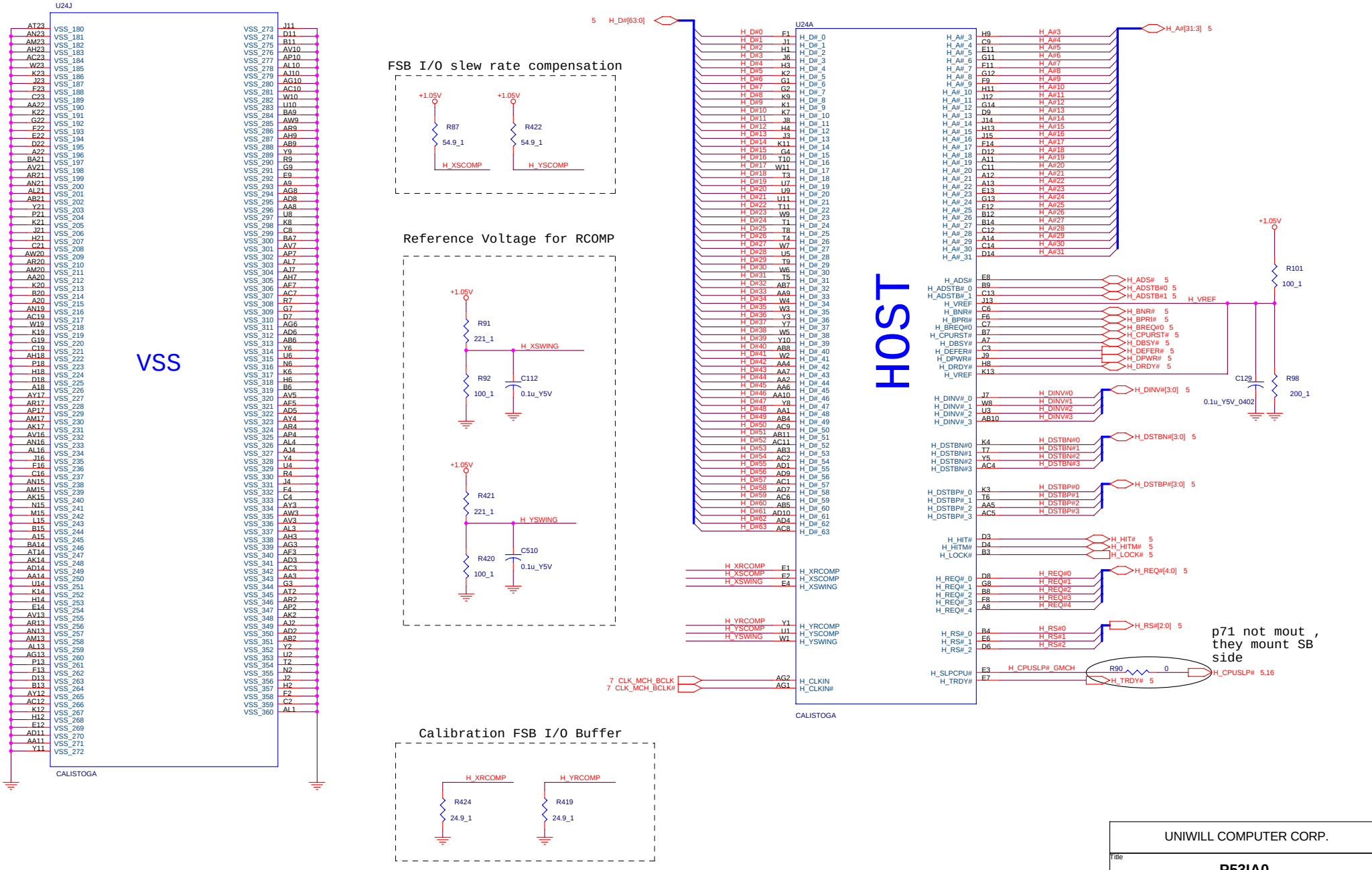
FS3 , FS 4 SEETING BY I2C BUS ??????

UNIWILL COMPUTER CORP.

Title: **P53IA0**

Size | Document Number: 3220 **CLOCK GEN ICS9LPR310** | Rev C

Date: Monday, February 06, 2006 | Sheet 7 of 33


U24J
VSS
CALISTOGA
FSB I/O slew rate compensation
+1.05V
R87
54.9_1
H_XSCOMP
R422
H_YSCOMP
Reference Voltage for RCOMP
R91
221_1
H_XSWING
R92
100_1
C112
0.1u_Y5V
R421
H_YSWING
R420
C510
Calibration FSB I/O Buffer
H_XRCOMP
R424
24.9_1
H_YRCOMP
R419
U24A
HOST
H_D#[63:0]
H_A#[31:3]
H_ADS#
H_ADSTB#0
H_ADSTB#1
H_VREF
H_BNR#
H_BPRI#
H_BREQ#0
H_CPURST#
H_DBSY#
H_DEFER#
H_DPWR#
H_DRDY#
H_DINV#[3:0]
H_DSTBN#[3:0]
H_DSTBP#[3:0]
H_HIT#
H_HITM#
H_LOCK#
H_REQ#[4:0]
H_RS#[2:0]
H_CPUSLP#
H_TRDY#
H_XRCOMP
H_XSCOMP
H_XSWING
H_YRCOMP
H_YSCOMP
H_YSWING
H_CLKIN
H_CLKIN#
7_CLK_MCH_BCLK
7_CLK_MCH_BCLK#
CALISTOGA
R101
100_1
C129
0.1u_Y5V_0402
R98
200_1
R90
0
H_CPUSLP# 5,16
p71 not mout , they mount SB side
UNIWILL COMPUTER CORP.
P53IA0
NB_945PM-1/5
Monday, February 06, 2006
Sheet 8 of 33

U24B

DMI
DMI_RXP[3:0] → DMI_RXP3 AG41, DMI_RXP2 AF37, DMI_RXP1 AE41, DMI_RXP0 AC37
DMI_RXN[3:0] → DMI_RXN3 AH41, DMI_RXN2 AG37, DMI_RXN1 AF41, DMI_RXN0 AE37
DMI_TXP[3:0] → DMI_TXP3 AG39, DMI_TXP2 AF35, DMI_TXP1 AE39, DMI_TXP0 AC35
DMI_TXN[3:0] → DMI_TXN3 AH39, DMI_TXN2 AG35, DMI_TXN1 AF39, DMI_TXN0 AE35
DMI_TXP_3 DMI_TXP_2 DMI_TXP_1 DMI_TXP_0
DMI_TXN_3 DMI_TXN_2 DMI_TXN_1 DMI_TXN_0
DMI_RXP_3 DMI_RXP_2 DMI_RXP_1 DMI_RXP_0
DMI_RXN_3 DMI_RXN_2 DMI_RXN_1 DMI_RXN_0

NC
NC18 A3, NC17 A39, NC16 A4, NC15 A40, NC14 AW1, NC13 AW41, NC12 AY1, NC11 AY41, NC10 B2, NC9 B41, NC8 BA1, NC7 BA2, NC6 BA3, NC5 BA39, NC4 BA40, NC3 BA41, NC2 C1, NC1 C41, NC0 D1

MISC
CLK_REQ# H32, LT_RESET# K28, SDVO_CTRLDATA H27, SDVO_CTRLCLK H28
Z0907 R117 0_OP → +1.5V; NB_SYNC# 17

PM
RSTIN# AH34, PWROK AH33, PM_THRMTRIP# G6, PM_EXTTS#_1 H26, PM_EXTTS#_0 F25, PM_BMBUSY# G28
Z0911 R157 100 → PLT_RST# 17,19,20,25,26; DELAY_VR_PWRGOOD 17
ICH7_THRMTRIP#
PM_EXTTS#1 R112 0 D6 BAT54 → PM_DPRSLPVR 17,27; EXTTS#0 14,25
PM_EXTTS#0
BM_BUSY# 17

CLK
D_REFSSCLKIN H33, D_REFSSCLKIN# G34, D_REFCLKIN A26, D_REFCLKIN# A27, G_CLKIN AG33, G_CLKIN# AF33
R468 0 Z0901 D41
R470 0 Z0902 C40
R438 0 Z0906 A26
R441 0 Z0912 A27
GCLK, GCLK#

CFG
CFG_20 J26, CFG_19 K27, CFG_18 J25, CFG_17 H15, CFG_16 G18, CFG_15 H16, CFG_14 C15, CFG_13 K15, CFG_12 G15, CFG_11 D15, CFG_10 E16, CFG_9 G16, CFG_8 D16, CFG_7 D19, CFG_6 E18, CFG_5 F15, CFG_4 E15, CFG_3 F18, CFG_2 J18, CFG_1 K18, CFG_0 K16
CFG19 12, CFG18 12, CFG16 12, CFG9 12, CFG5 12
Z0903 R104 1K_OP, Z0904 R105 1K_OP
MCH_BSEL2 5, MCH_BSEL1 5, MCH_BSEL0 5
Base on RSTIN#

RSVD
RSVD_13 D27, RSVD_12 D28, RSVD_11 A34, RSVD_10 A35, RSVD_9 A41, RSVD_8 J19, RSVD_7 H7, RSVD_6 AF11, RSVD_5 AG11, RSVD_4 F7, RSVD_3 F3, RSVD_2 R32, RSVD_1 T32

DDR MUXING
M_VREF_MCH → AK41; SM_VREF_1 AK1, SM_VREF_0
M_RCOMPP AT9, M_RCOMPN AV9; SM_RCOMP, SM_RCOMP#
SM_ODT_3 AU21, SM_ODT_2 AY20, SM_ODT_1 BA12, SM_ODT_0 BA13
13,14 MB_ODT3, 13,14 MB_ODT2, 13,14 MA_ODT1, 13,14 MA_ODT0
M_OCDCOMP1 AF10, M_OCDCOMP0 AL20; SM_OCDCOMP_1, SM_OCDCOMP_0
as short as possible
R97, R106, 40.2_1_OP, 40.2_1_OP
SM_CS#_3 AW21, SM_CS#_2 AY21, SM_CS#_1 AW12, SM_CS#_0 AW13
13,14 MB_CS#3, 13,14 MB_CS#2, 13,14 MA_CS#1, 13,14 MA_CS#0
SM_CKE_3 AY29, SM_CKE_2 BA29, SM_CKE_1 AT20, SM_CKE_0 AU20
13,14 MB_CKE3, 13,14 MB_CKE2, 13,14 MA_CKE1, 13,14 MA_CKE0
SM_CK#_3 AY40, SM_CK#_2 AY7, SM_CK#_1 AT1, SM_CK#_0 AW35
13 MB_CK#3, 13 MB_CK#4, 13 MA_CK#1, 13 MA_CK#0
SM_CK_3 AW40, SM_CK_2 AW7, SM_CK_1 AR1, SM_CK_0 AY35
13 MB_CK3, 13 MB_CK4, 13 MA_CK1, 13 MA_CK0

CALISTOGA

GCLK => PCI-E & DMI (100MHZ)
DREFCLK => Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

SDVODATA has internal pull down
0= no DVO device
1= DVO device present
SDVOCLK has internal pull down .

Asserted to control the raw PCI-E clock
Asserted to synchronize with ICH on fault
GHCH integrated graphics busy

U24C

LVDS
L_BKLTCTL D32, L_BKLTEN J30, L_CLKCTLA H30, L_CLKCTLB H29, L_DDC_CLK G26, L_DDC_DATA G25, L_IBG B38, L_VBG C35, L_VDDEN F32, L_VREFH C33, L_VREFL C32
LA_CLK# A33, LA_CLK A32, LB_CLK# E27, LB_CLK E26
LA_DATA#_0 C37, LA_DATA#_1 B35, LA_DATA#_2 A37
LA_DATA_0 B37, LA_DATA_1 B34, LA_DATA_2 A36
LB_DATA#_0 G30, LB_DATA#_1 D30, LB_DATA#_2 F29
LB_DATA_0 F30, LB_DATA_1 D29, LB_DATA_2 F28

TV
TV_DACA_OUT A16, TV_DACB_OUT C18, TV_DACC_OUT A19
TV_IREF J20, TV_IRTNA B16, TV_IRTNB B18, TV_IRTNC B19
TV_DCONSEL0 K30, TV_DCONSEL1 J29
+1.5V
O/A

VGA
CRT_BLUE E23, CRT_BLUE# D23, CRT_GREEN C22, CRT_GREEN# B22, CRT_RED A21, CRT_RED# B21
CRT_DDC_CLK C26, CRT_DDC_DATA C25, CRT_HSYNC G23, CRT_IREF J22, CRT_VSYNC H23
+1.05V

PCI-EXPRESS GRAPHICS
EXP_A_COMPI D40, EXP_A_COMPO D38
PEG_COMP R469 24.9_1 → +1.5V
EXP_A_RXN_0 F34, EXP_A_RXN_1 G38, EXP_A_RXN_2 H34, EXP_A_RXN_3 J38, EXP_A_RXN_4 L34, EXP_A_RXN_5 M38, EXP_A_RXN_6 N34, EXP_A_RXN_7 P38, EXP_A_RXN_8 R34, EXP_A_RXN_9 T38, EXP_A_RXN_10 V34, EXP_A_RXN_11 W38, EXP_A_RXN_12 Y34, EXP_A_RXN_13 AA38, EXP_A_RXN_14 AB34, EXP_A_RXN_15 AC38
PEG_RXN0 … PEG_RXN15 → PEG_RXN[15..0] 26
EXP_A_RXP_0 D34, EXP_A_RXP_1 E38, EXP_A_RXP_2 G34, EXP_A_RXP_3 H38, EXP_A_RXP_4 J34, EXP_A_RXP_5 L38, EXP_A_RXP_6 M34, EXP_A_RXP_7 N38, EXP_A_RXP_8 P34, EXP_A_RXP_9 R38, EXP_A_RXP_10 T34, EXP_A_RXP_11 V38, EXP_A_RXP_12 W34, EXP_A_RXP_13 Y38, EXP_A_RXP_14 AA34, EXP_A_RXP_15 AB38
PEG_RXP0 … PEG_RXP15 → PEG_RXP[15..0] 26
EXP_A_TXN_0 F36, EXP_A_TXN_1 G40, EXP_A_TXN_2 H36, EXP_A_TXN_3 J40, EXP_A_TXN_4 L36, EXP_A_TXN_5 M40, EXP_A_TXN_6 N36, EXP_A_TXN_7 P40, EXP_A_TXN_8 R36, EXP_A_TXN_9 T40, EXP_A_TXN_10 V36, EXP_A_TXN_11 W40, EXP_A_TXN_12 Y36, EXP_A_TXN_13 AA40, EXP_A_TXN_14 AB36, EXP_A_TXN_15 AC40
PEG_TXN0 … PEG_TXN15 → PEG_TXN[15..0] 26
EXP_A_TXP_0 D36, EXP_A_TXP_1 F40, EXP_A_TXP_2 G36, EXP_A_TXP_3 H40, EXP_A_TXP_4 J36, EXP_A_TXP_5 L40, EXP_A_TXP_6 M36, EXP_A_TXP_7 N40, EXP_A_TXP_8 P36, EXP_A_TXP_9 R40, EXP_A_TXP_10 T36, EXP_A_TXP_11 V40, EXP_A_TXP_12 W36, EXP_A_TXP_13 Y40, EXP_A_TXP_14 AA36, EXP_A_TXP_15 AB40
PEG_TXP0 … PEG_TXP15 → PEG_TXP[15..0] 26

CALISTOGA

+1.8VS
R89 150_1, R88 150_1
0.05A M_VREF_MCH
C169 0.1u_Y5V, C105 0.1u_Y5V

+1.8VS
R95 80.6_1 → M_RCOMPN
R94 80.6_1 → M_RCOMPP

+1.05V
C196 1000P

Only Base on Discreted VGA

VCCA_DPLLA , VCCA_DPLLB => NC
DREF_CLKP / DREF_SSCLKP = GND
DREF_CLKN / DREF_SSCLKN = GND

VCCA_DPLLA , VCCA_DPLLB =>1.5V
DREF_CLKP / DREF_SSCLKP = 1.5V
DREF_CLKN / DREF_SSCLKN = GND

CFG0	CFG1	CFG2	Host Clock frequency
1	0	0	533
1	1	0	667

CFG20 (IPD) => 1= Only SDVO or PCI-E
0 = SDVO and PCI-E

CFG7 (IPU) => 1= Mobility CPU
0 = Reverse

For MEN bus throttling
+3.3V
R114 10K → PM_EXTTS#1
R115 10K → PM_EXTTS#0
PM_EXTTS#0 13
Check with S/W

Reserve for NB THRMTRIP# (O/D Vccp)
IPU
ICH7_THRMTRIP# → D5 BAT54_OP → PM_THRMTRIP# 5,16

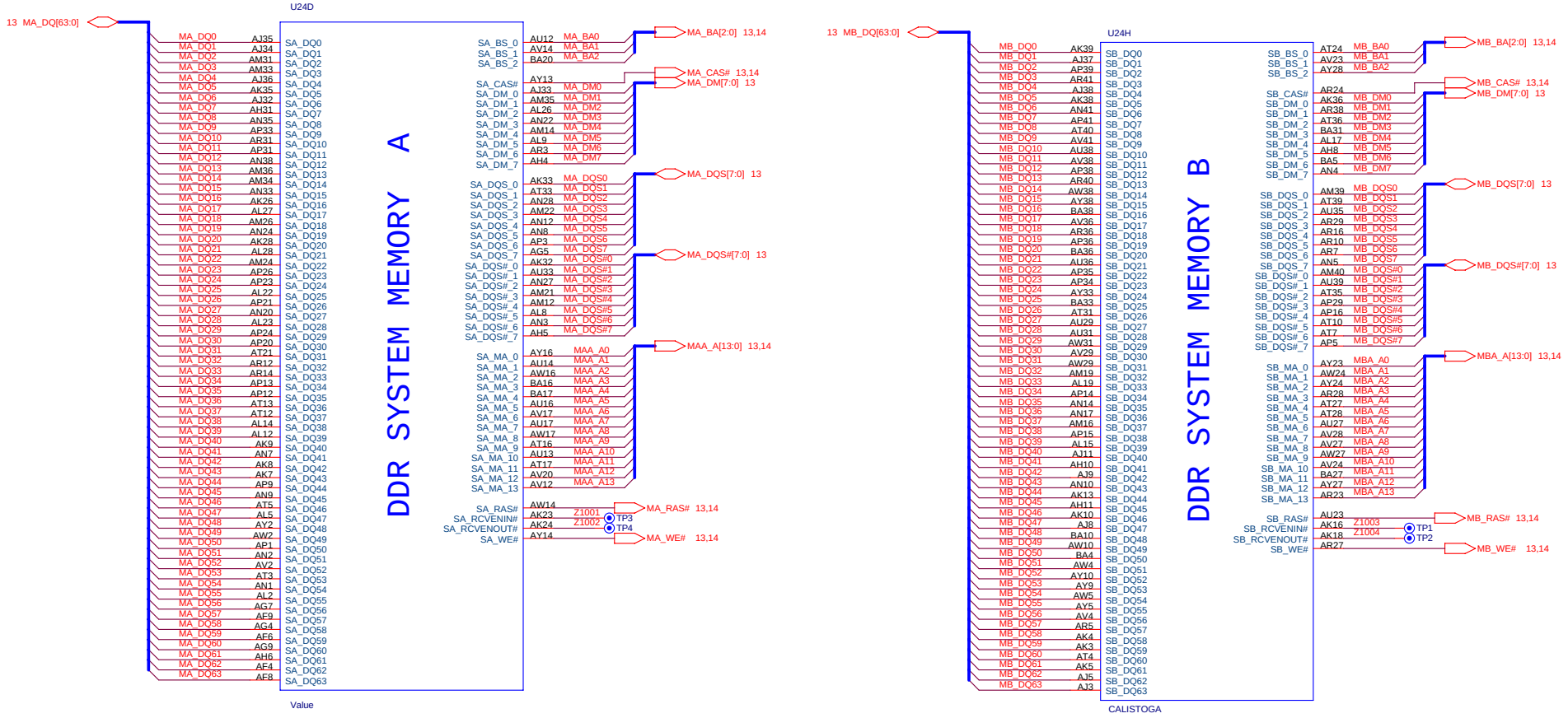
Colse to NB
DELAY_VR_PWRGOOD
C193 0.1u_Y5V

UNIWILL COMPUTER CORP.

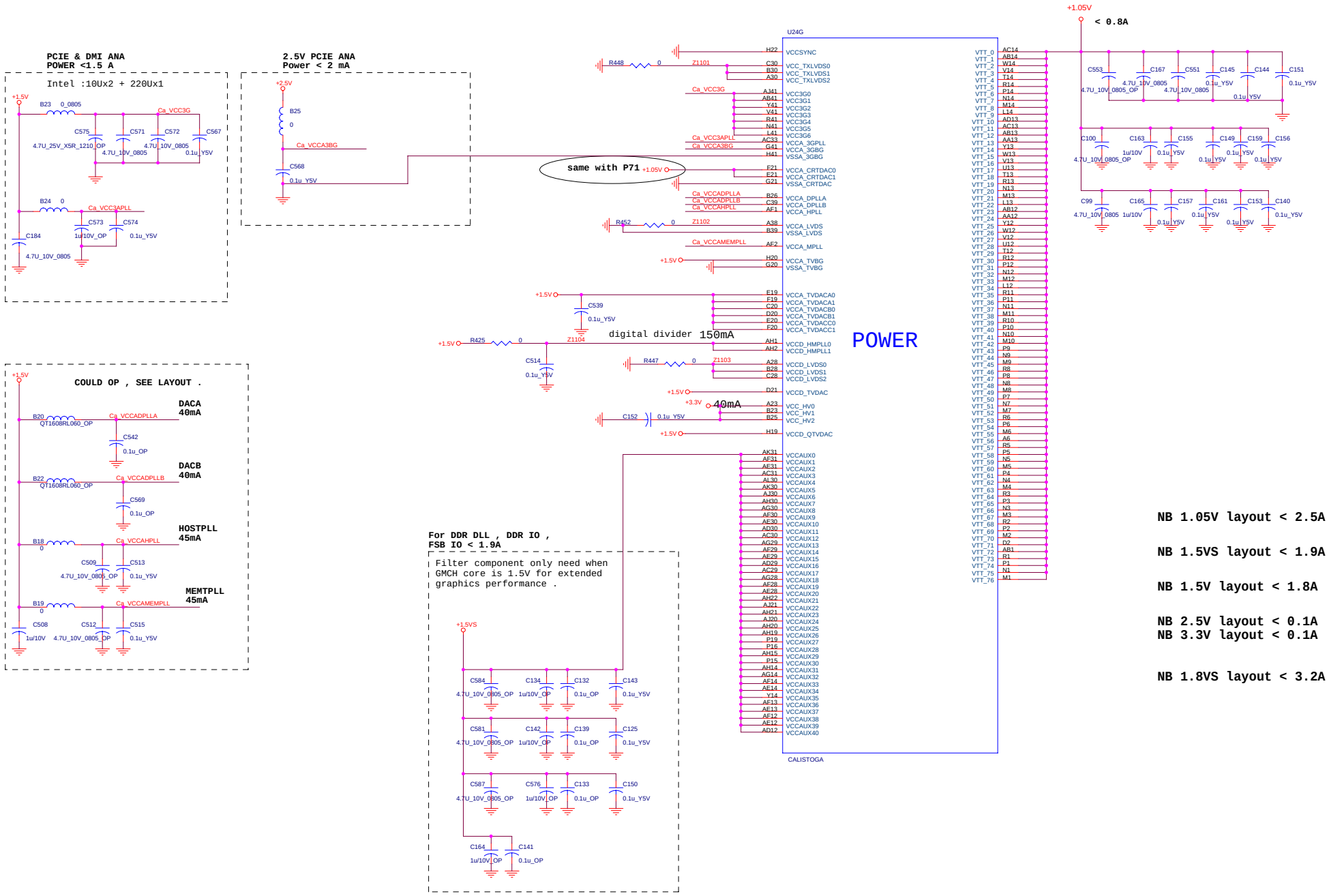
Title: P53IA0

Size: 3220 | Document Number: NB NB DDRCLK_VGA_PCIEXPR-2/5 | Rev: C

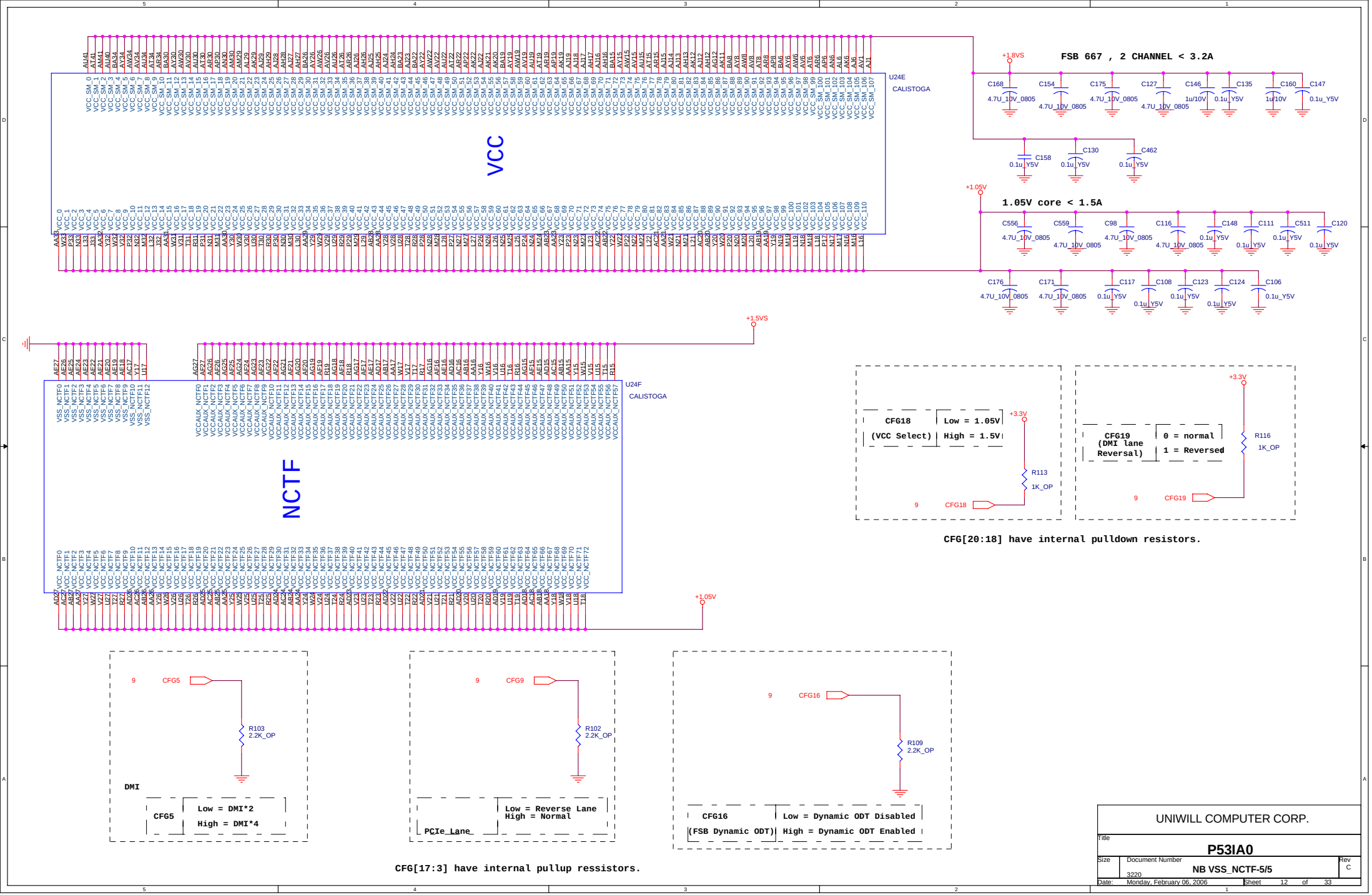
Date: Monday, February 06, 2006 | Sheet 9 of 33



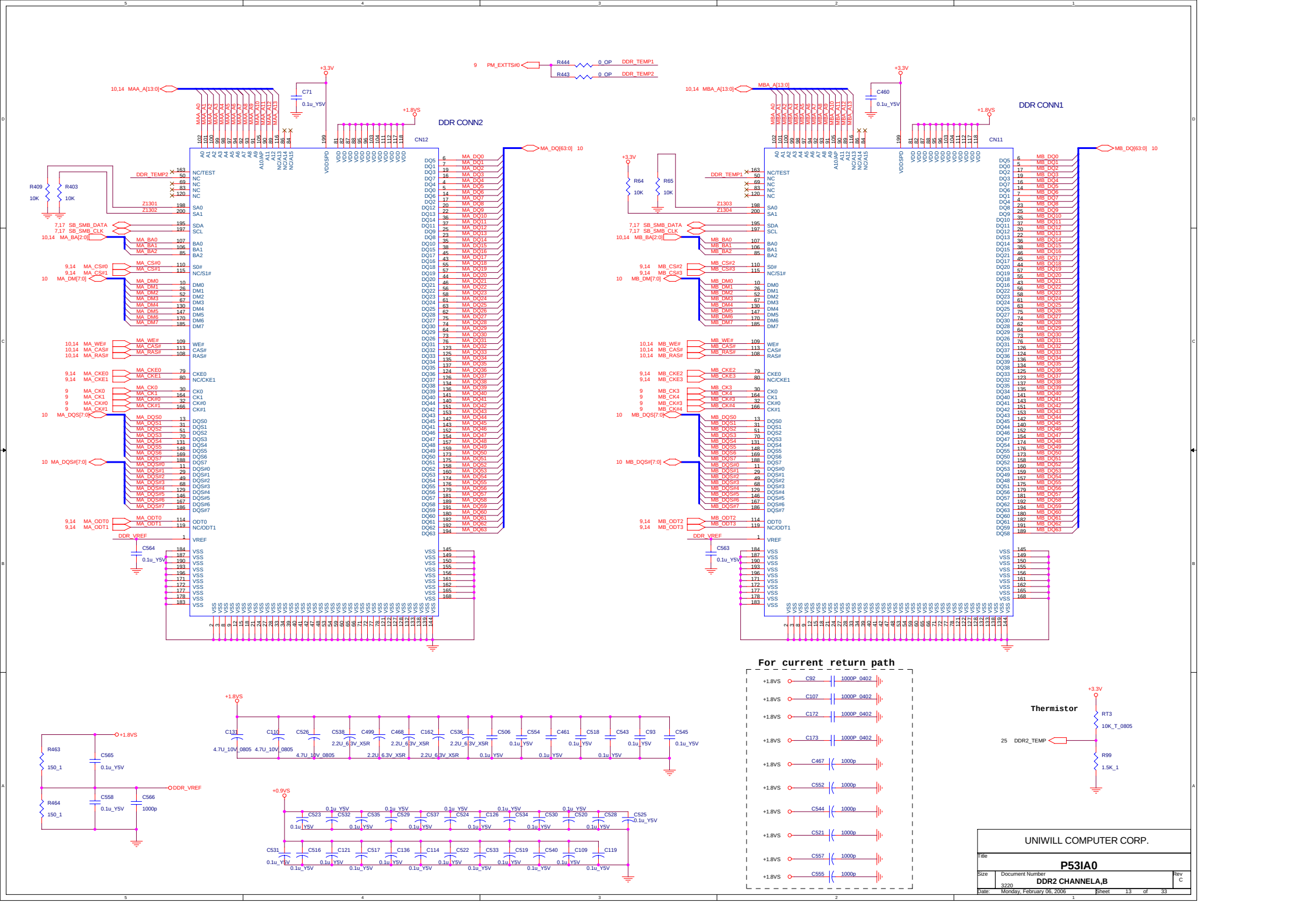
UNIWILL COMPUTER CORP.			
Title: P53IA0			
Size	Document Number: NB DDR_MEM SYSTEM-3/5		Rev: C
	3220		
Date: Monday, February 06, 2006	Sheet 10 of 33		



UNIWILL COMPUTER CORP.		
Title	P53IA0	
Size	Document Number 3220	Rev C
	NB POWER-4/5	
Date: Monday, February 06, 2006	Sheet 11 of 33	

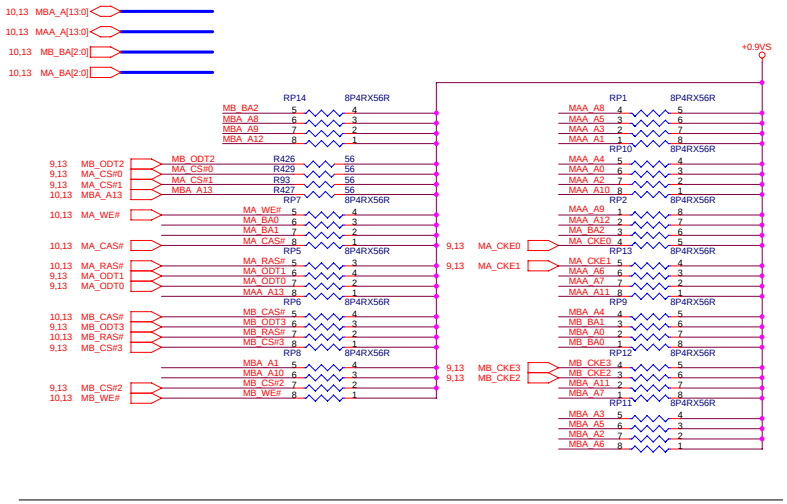


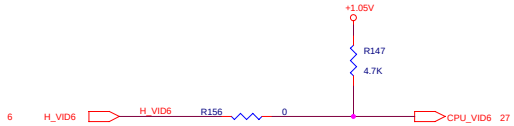
UNIWILL COMPUTER CORP.	
Title	P53IA0
Size	Document Number: 3220 NB VSS_NCTF-5/5 Rev: C
Date: Monday, February 06, 2006	Sheet 12 of 33

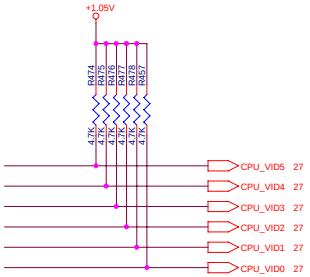

DDR CONN2
DDR CONN1
For current return path
Thermistor
UNIWILL COMPUTER CORP.
P53IA0
DDR2 CHANNELA,B
Monday, February 06, 2006

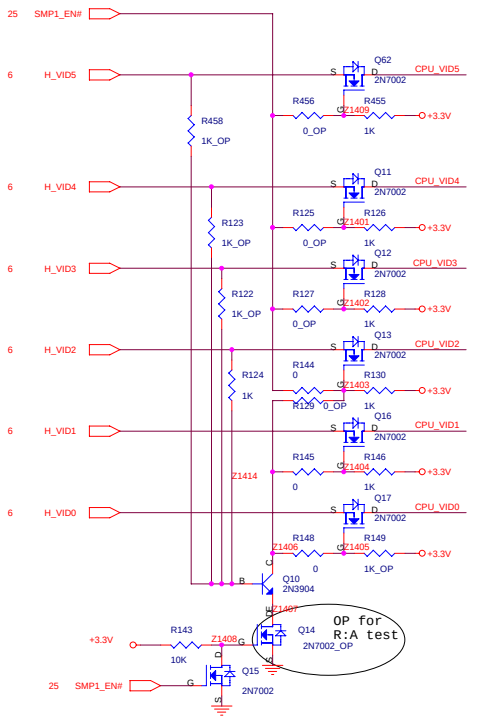
SMART POWER

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		

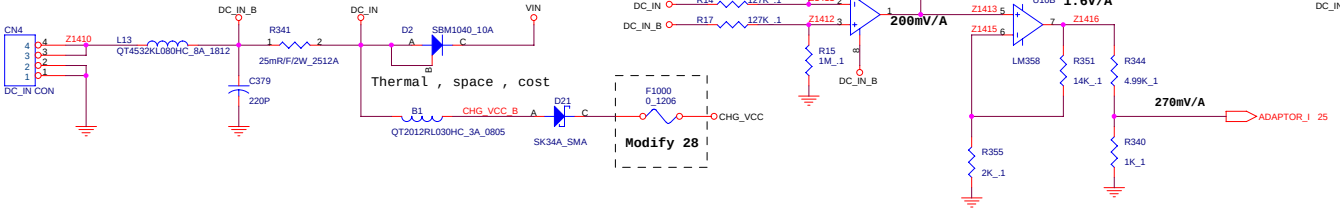


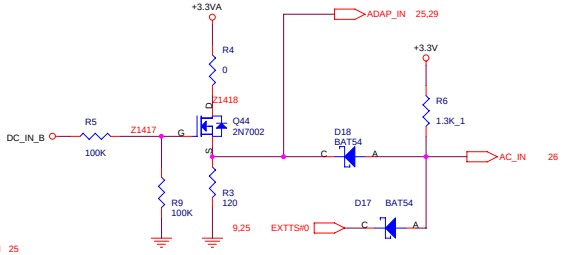






DC IN



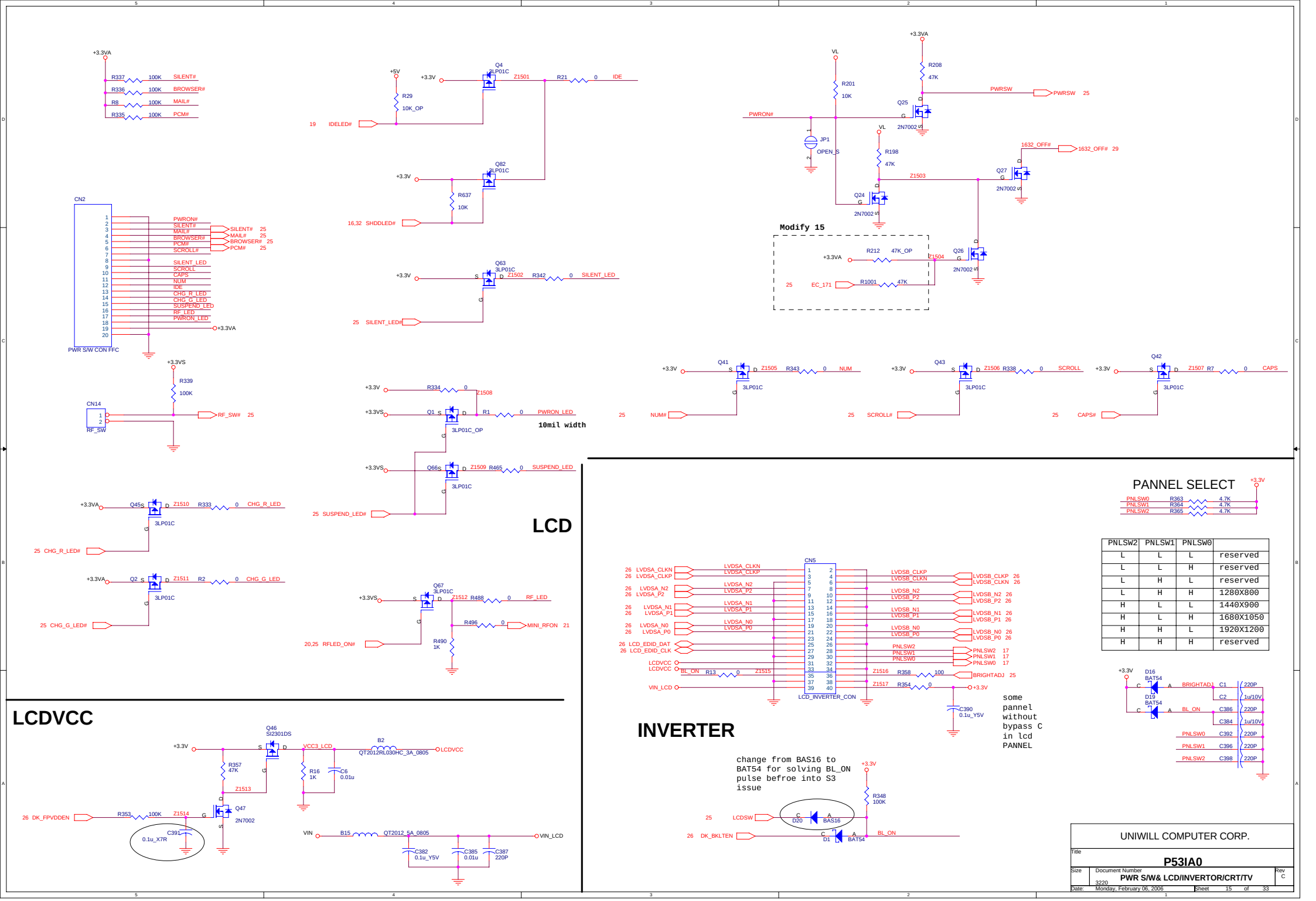


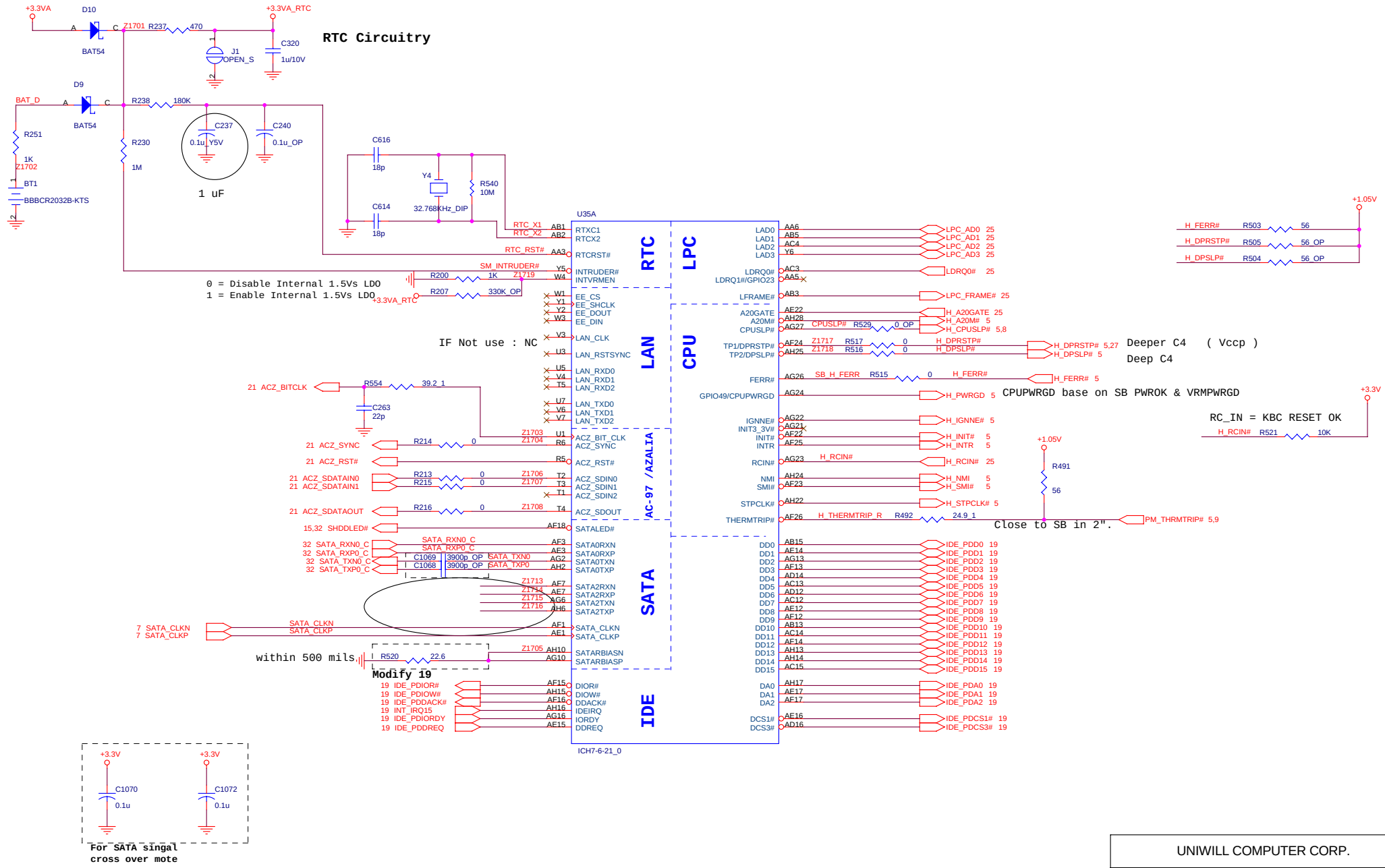
UNIWILL COMPUTER CORP.

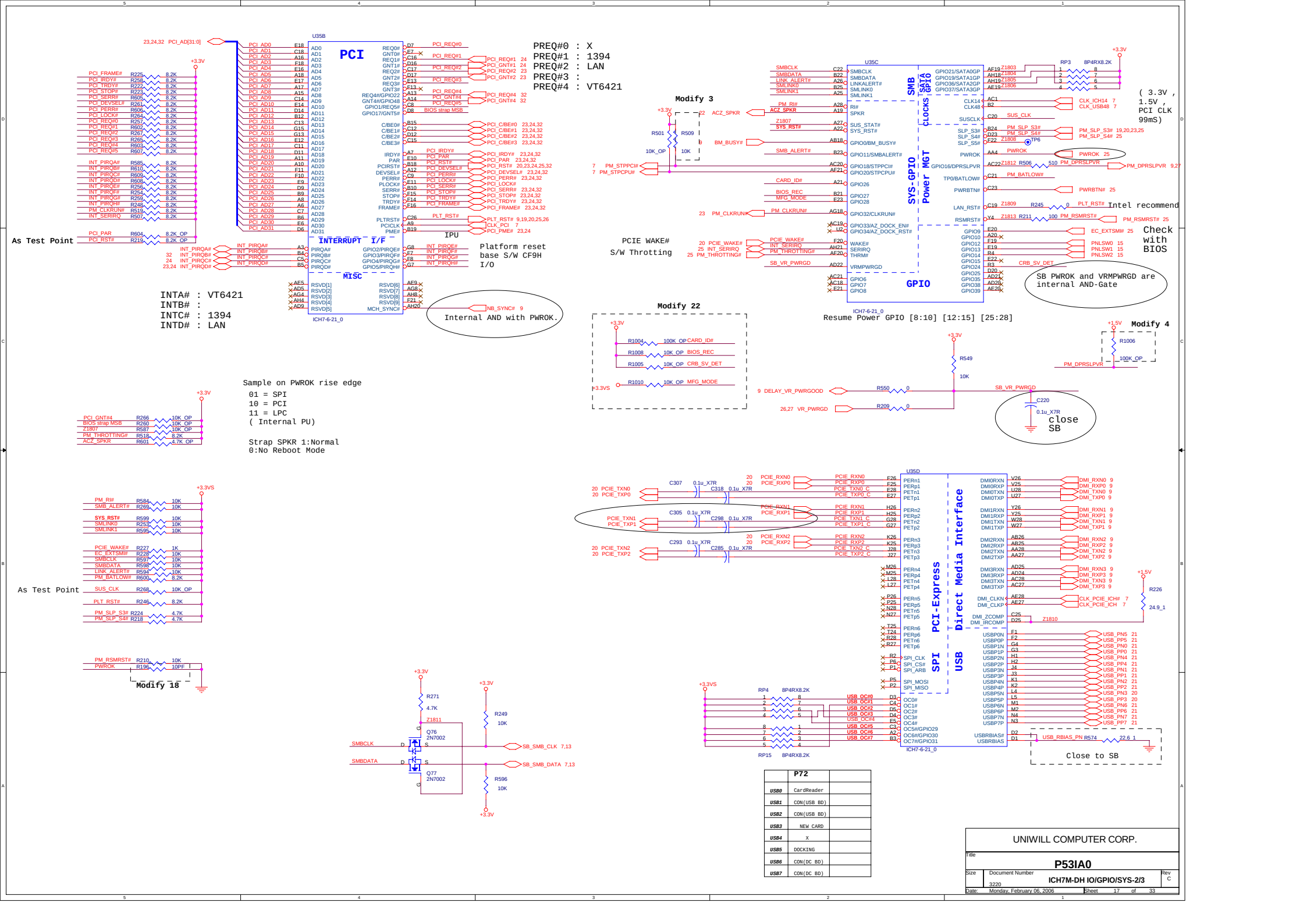
Title: **P53IA0**

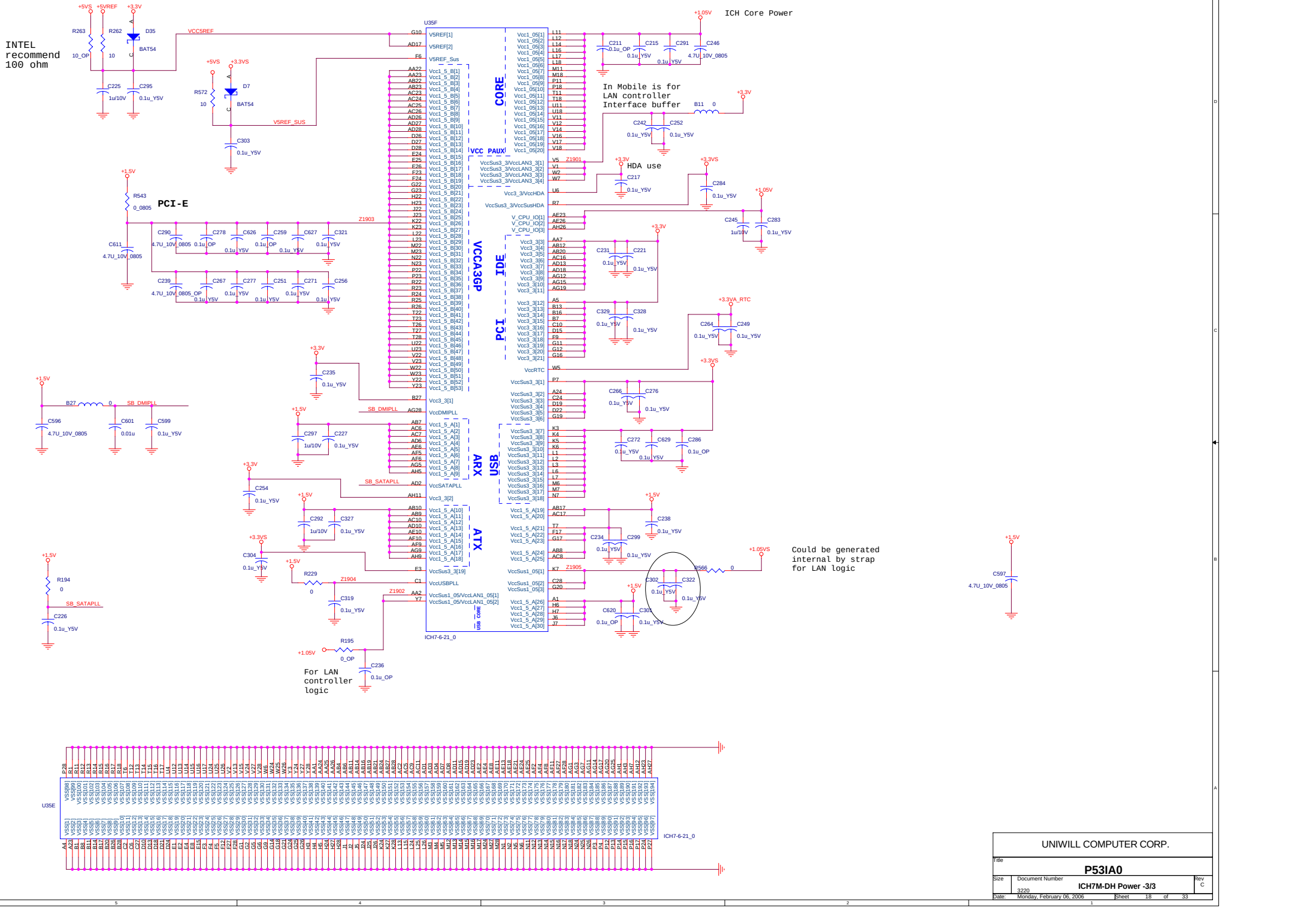
Size	Document Number	Rev
	3220 **Termination / Smart Power/DC IN**	C

Date: Monday, February 06, 2006 Sheet 14 of 33


+3.3VA
R337 100K SILENT#
R336 100K BROWSER#
R8 100K MAIL#
R335 100K PCM#
+5V
+3.3V
Q4 2LP01C Z1501 R21 0 IDE
R29 10K_OP
19 IDELED#
Q82 2LP01C
R637 10K
16,32 SHDDLED#
Q63 3LP01C Z1502 R342 0 SILENT_LED
25 SILENT_LED#
VL
R201 10K
R208 47K
PWRSW
PWRSW 25
Q25 2N7002
PWRON#
JP1 OPEN_S
R198 47K
1632_OFF#
1632_OFF# 29
Z1503
Q27 2N7002
Q24 2N7002
Modify 15
R212 47K_OP
Z1504
Q26 2N7002
R1001 47K
25 EC_171
CN2
PWRON#
SILENT#
MAIL#
BROWSER#
PCM#
SCROLL#
SILENT_LED
SCROLL
CAPS
NUM
IDE
CHG_R_LED
CHG_G_LED
SUSPEND_LED
RF_LED
PWRON_LED
+3.3VA
PWR S/W CON FFC
+3.3VS
R339 100K
CN14
RF_SW# 25
RF_SW
Q41 3LP01C Z1505 R343 0 NUM
25 NUM#
Q43 3LP01C Z1506 R338 0 SCROLL
25 SCROLL#
Q42 3LP01C Z1507 R7 0 CAPS
25 CAPS#
R334 0 Z1508
Q1 3LP01C_OP R1 0 PWRON_LED
10mil width
Q66 3LP01C Z1509 R465 0 SUSPEND_LED
25 SUSPEND_LED#
Q45 3LP01C Z1510 R333 0 CHG_R_LED
25 CHG_R_LED#
Q2 3LP01C Z1511 R2 0 CHG_G_LED
25 CHG_G_LED#
Q67 3LP01C Z1512 R488 0 RF_LED
R496 0 MINI_RFON 21
20,25 RFLED_ON#
R490 1K
LCD
PANNEL SELECT
PNLSW0 R363 4.7K
PNLSW1 R364 4.7K
PNLSW2 R365 4.7K
PNLSW2 PNLSW1 PNLSW0
L L L reserved
L L H reserved
L H L reserved
L H H 1280X800
H L L 1440X900
H L H 1680X1050
H H L 1920X1200
H H H reserved
CN5
LVDSA_CLKN
LVDSA_CLKP
LVDSA_N2
LVDSA_P2
LVDSA_N1
LVDSA_P1
LVDSA_N0
LVDSA_P0
LCD_EDID_DAT
LCD_EDID_CLK
LCDVCC
BL_ON R13 0 Z1515
VIN_LCD
LVDSB_CLKP
LVDSB_CLKN
LVDSB_N2
LVDSB_P2
LVDSB_N1
LVDSB_P1
LVDSB_N0
LVDSB_P0
PNLSW2
PNLSW1
PNLSW0
Z1516 R358 100 BRIGHTADJ 25
Z1517 R354 0 +3.3V
C390 0.1u_Y5V
LCD_INVERTER_CON
some pannel without bypass C in lcd PANNEL
INVERTER
change from BAS16 to BAT54 for solving BL_ON pulse befroe into S3 issue
25 LCDSW
26 DK_BKLTEN
D20 BAS16
D1 BAT54
R348 100K
BL_ON
D16 BAT54
D19 BAT54
BRIGHTADJ
BL_ON
C1 220P
C2 1u/10V
C386 220P
C384 1u/10V
PNLSW0 C392 220P
PNLSW1 C396 220P
PNLSW2 C398 220P
LCDVCC
Q46 SI2301DS
VCC3_LCD
B2 QT2012RL030HC_3A_0805 LCDVCC
R357 47K
Z1513
R16 1K
C6 0.01u
26 DK_FPVDDEN
R353 100K Z1514
Q47 2N7002
C391 0.1u_X7R
VIN
B15 QT2012_5A_0805 VIN_LCD
C382 0.1u_Y5V
C385 0.01u
C387 220P
UNIWILL COMPUTER CORP.
Title
P53IA0
Size
Document Number
PWR S/W& LCD/INVERTOR/CRT/TV
3220
Rev C
Date: Monday, February 06, 2006
Sheet 15 of 33

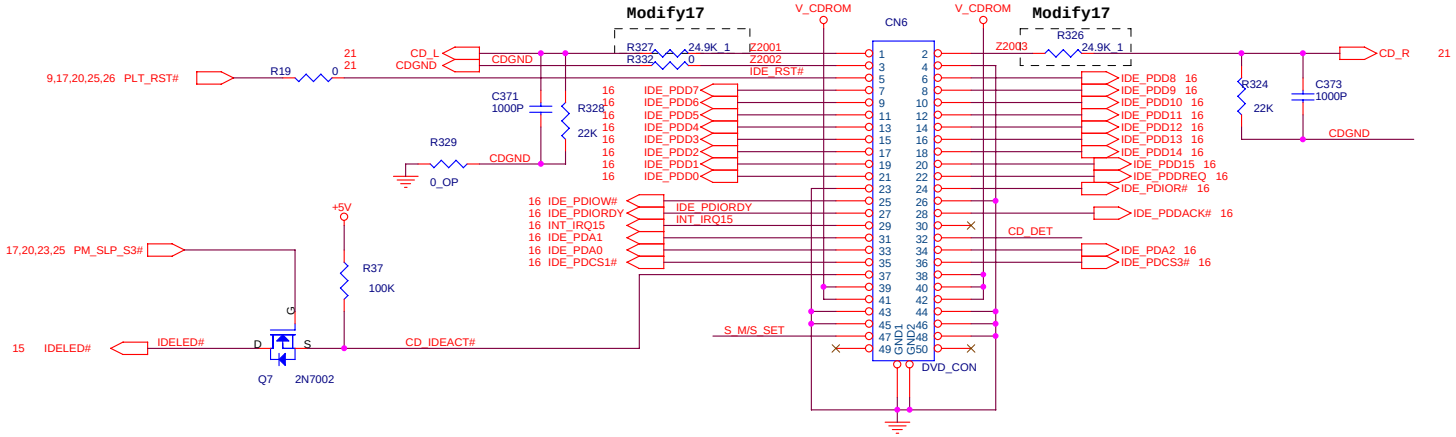

RTC Circuitry
+3.3VA
+3.3VA_RTC
D10
BAT54
Z1701
R237
470
C320
1u/10V
J1
OPEN_S
D9
BAT_D
R238
180K
R251
1K
Z1702
BT1
BBBCR2032B-KTS
R230
1M
C237
0.1u
Y5V
C240
0.1u_OP
1 uF
C616
18p
C614
18p
Y4
32.768KHz_DIP
R540
10M
U35A
RTC_X1
RTC_X2
RTC_RST#
SM_INTRUDER#
R200
1K
Z1719
R207
330K_OP
0 = Disable Internal 1.5Vs LDO
1 = Enable Internal 1.5Vs LDO
IF Not use : NC
RTC
LAN
AC-97 /AZALIA
SATA
IDE
LPC
CPU
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
ACZ_BIT_CLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH7-6-21_0
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
LPC_AD0 25
LPC_AD1 25
LPC_AD2 25
LPC_AD3 25
LDRQ0# 25
LPC_FRAME# 25
H_A20GATE 25
H_A20M# 5
H_CPUSLP# 5,8
H_DPRSTP# 5,27
H_DPSLP# 5
H_FERR# 5
H_PWRGD 5
H_IGNNE# 5
H_INIT# 5
H_INTR 5
H_RCIN# 25
H_NMI 5
H_SMI# 5
H_STPCLK# 5
PM_THRMTRIP# 5,9
IDE_PDD0 19
IDE_PDD1 19
IDE_PDD2 19
IDE_PDD3 19
IDE_PDD4 19
IDE_PDD5 19
IDE_PDD6 19
IDE_PDD7 19
IDE_PDD8 19
IDE_PDD9 19
IDE_PDD10 19
IDE_PDD11 19
IDE_PDD12 19
IDE_PDD13 19
IDE_PDD14 19
IDE_PDD15 19
IDE_PDA0 19
IDE_PDA1 19
IDE_PDA2 19
IDE_PDCS1# 19
IDE_PDCS3# 19
Deeper C4 (Vccp)
Deep C4
CPUPWRGD base on SB PWROK & VRMPWRGD
RC_IN = KBC RESET OK
H_RCIN# R521 10K
+3.3V
+1.05V
R491
56
Close to SB in 2".
H_FERR# R503 56
H_DPRSTP# R505 56_OP
H_DPSLP# R504 56_OP
21 ACZ_BITCLK
R554
39.2_1
C263
22p
21 ACZ_SYNC
R214
21 ACZ_RST#
21 ACZ_SDATAIN0
21 ACZ_SDATAIN1
R213
R215
21 ACZ_SDATAOUT
R216
15,32 SHDDLED#
32 SATA_RXN0_C
32 SATA_RXP0_C
32 SATA_TXN0_C
32 SATA_TXP0_C
C1069
C1068
3900p_OP
SATA_TXN0
SATA_TXP0
7 SATA_CLKN
7 SATA_CLKP
within 500 mils
R520
22.6
Modify 19
19 IDE_PDIOR#
19 IDE_PDIOW#
19 IDE_PDDACK#
19 INT_IRQ15
19 IDE_PDIORDY
19 IDE_PDDREQ
+3.3V
C1070
0.1u
C1072
0.1u
For SATA singal
cross over mote
UNIWILL COMPUTER CORP.
P53IA0
SB ICH7M-DH -1/3
3220
Monday, February 06, 2006
Sheet 16 of 33

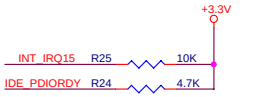

PREQ#0 : X
PREQ#1 : 1394
PREQ#2 : LAN
PREQ#3 :
PREQ#4 : VT6421
Modify 3
PCIE WAKE#
S/W Throtting
Resume Power GPIO [8:10] [12:15] [25:28]
Modify 22
Modify 4
Sample on PWROK rise edge
01 = SPI
10 = PCI
11 = LPC
(Internal PU)
Strap SPKR 1:Normal
0:No Reboot Mode
INTA# : VT6421
INTB# :
INTC# : 1394
INTD# : LAN
Platform reset
base S/W CF9H
I/O
IPU
Internal AND with PWROK.
SB PWROK and VRMPWRGD are
internal AND-Gate
Check
with
BIOS
(3.3V ,
1.5V ,
PCI CLK
99mS)
Intel recommend
close
SB
Close to SB
As Test Point
As Test Point
Modify 18
PCI
INTERRUPT I/F
MISC
SMB
CLOCKS
SATA
SYS-GPIO
Power MGT
GPIO
PCI-Express
SPI
USB
Direct Media Interface
P72
UNIWILL COMPUTER CORP.
P53IA0
ICH7M-DH IO/GPIO/SYS-2/3
3220
Monday, February 06, 2006



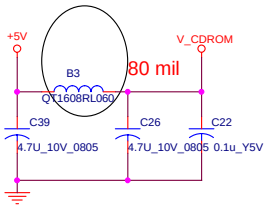
Title	UNIWILL COMPUTER CORP.
	P53IA0
Size	Document Number: 3220 — ICH7M-DH Power -3/3 — Rev C
Date: Monday, February 06, 2006	Sheet 18 of 33

CR-ROM



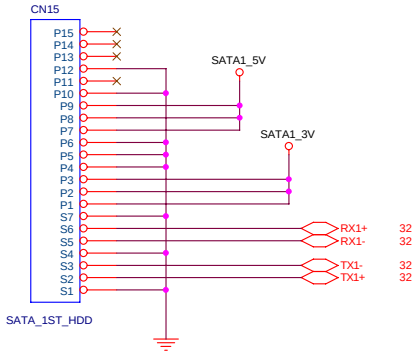


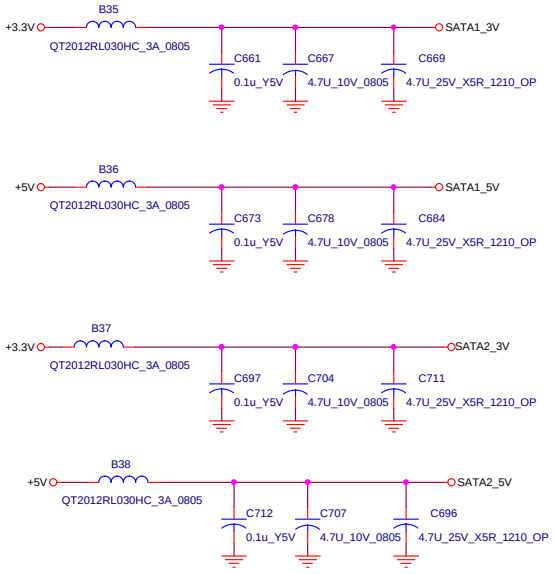
500mA Bead => 80 mils trace ?

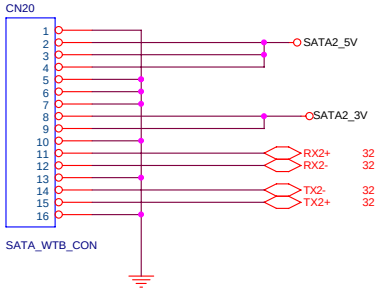


CSEL : Master = 0 / Slave = 1

HDD





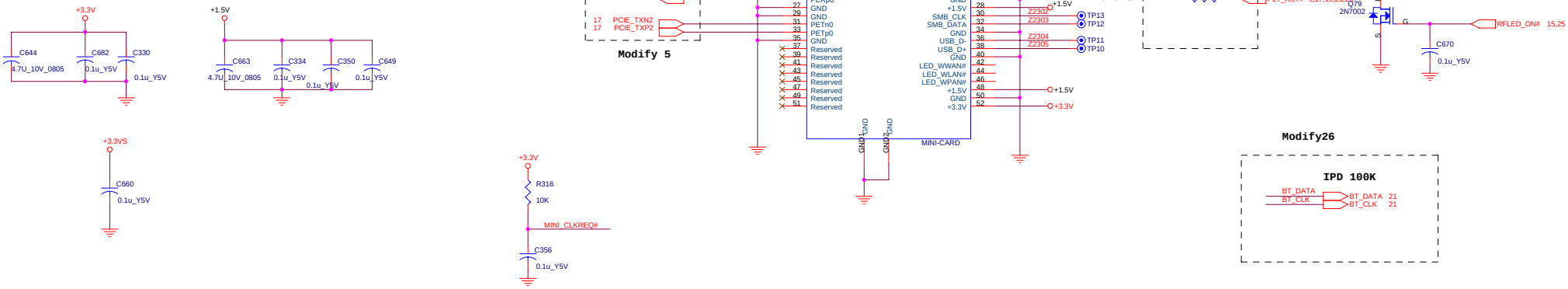


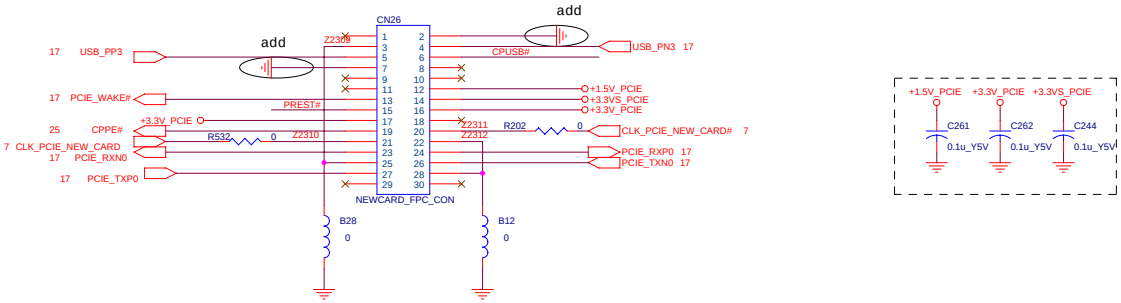
UNIWILL COMPUTER CORP.		
Title: **P53IA0**		
Size	Document Number: **HDD / CD-ROM CONN** 3220	Rev C
Date: Monday, February 06, 2006	Sheet 19 of 33	

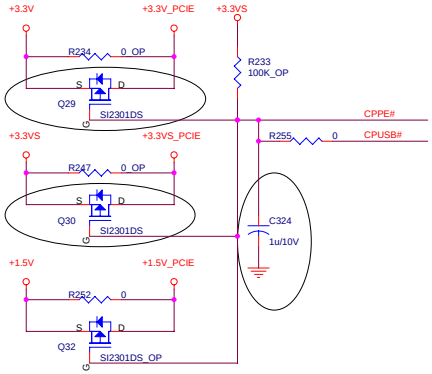
MINI CARD CONN

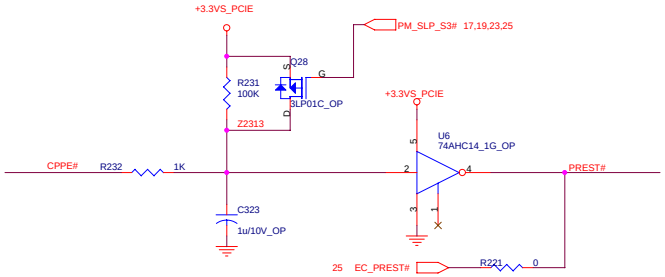
Intel PRO/Wireless 2100 LAN

PIN11	LED_WLAN_LINK	Hi(3.3V) Low(0V)	Solid ON 1 flash/3 sec LED OFF	Associated AP Not Associated with an AP Power OFF or RF_Kill active
PIN12	LED_WLAN_ACT	Hi(3.3V) Low(0V)	Rapid Blinking Slow Blinking LED OFF	Passing data traffic to AP Beacon traffic to Ap Power OFF or not activity or RF_Kill active
PIN13	HW_RadioXMIT_OFF#	Hi(3.3V) Low(0V)	Enable Disable	Radio transmitter is ON Radio transmitter turn off

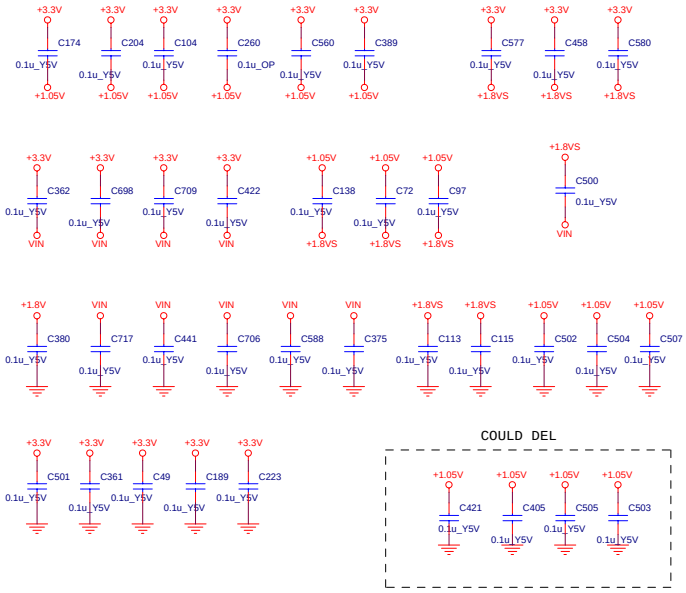




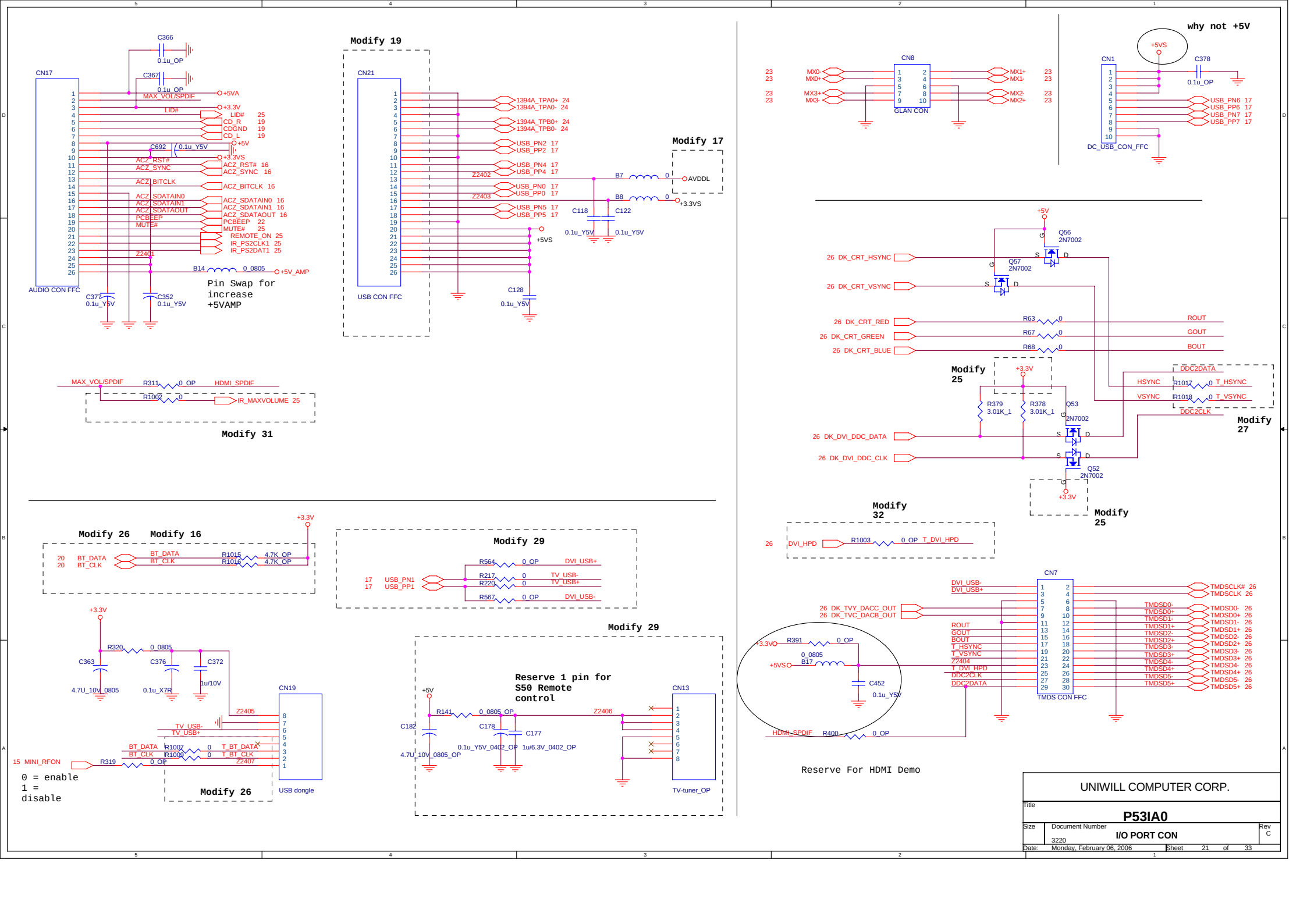




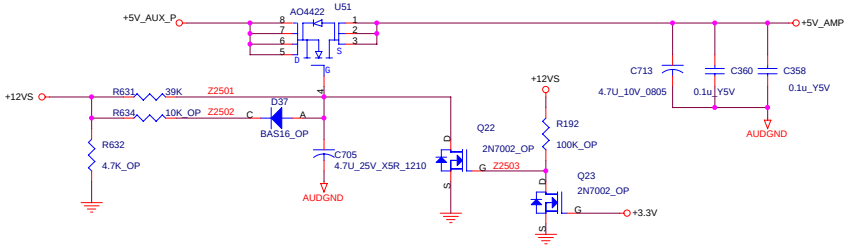
FOR EMI

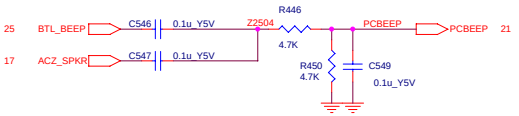


UNIWILL COMPUTER CORP.			
Title: P53IA0			
Size	Document Number: Wireless / New Card / EMI		Rev: C
	3220		
Date: Monday, February 06, 2006	Sheet 20 of 33		

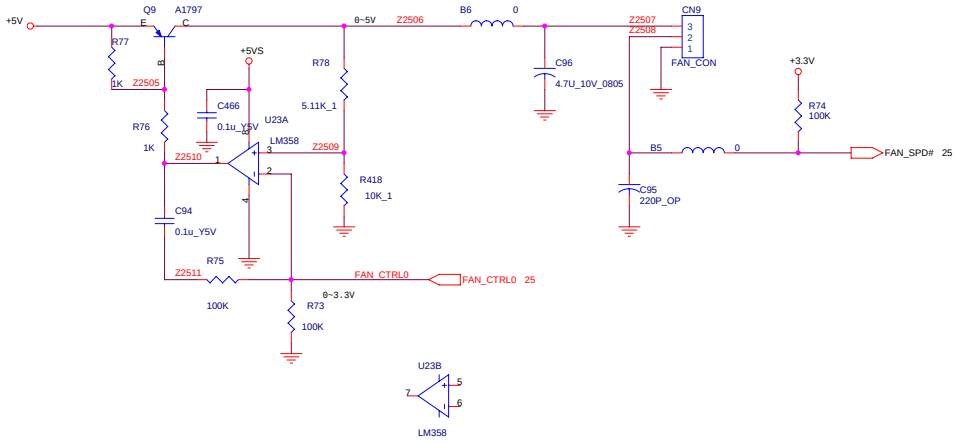

CN17
AUDIO CON FFC
C366
0.1u_OP
C367
0.1u_OP
MAX_VOL/SPDIF
LID#
C692
0.1u_Y5V
ACZ_RST#
ACZ_SYNC
ACZ_BITCLK
ACZ_SDATAIN0
ACZ_SDATAIN1
ACZ_SDATAOUT
PCBEEP
MUTE#
REMOTE_ON
IR_PS2CLK1
IR_PS2DAT1
Z2401
B14
0_0805
+5V_AMP
C377
0.1u_Y5V
C352
0.1u_Y5V
Pin Swap for increase +5VAMP
Modify 19
CN21
USB CON FFC
1394A_TPA0+
1394A_TPA0-
1394A_TPB0+
1394A_TPB0-
USB_PN2
USB_PP2
USB_PN4
USB_PP4
USB_PN0
USB_PP0
USB_PN5
USB_PP5
Z2402
Z2403
B7
B8
AVDDL
+3.3VS
C118
C122
C128
Modify 17
MAX_VOL/SPDIF
R311
0_OP
HDMI_SPDIF
R1002
IR_MAXVOLUME
Modify 31
Modify 26
Modify 16
BT_DATA
BT_CLK
R1015
R1016
4.7K_OP
+3.3V
R320
0_0805
C363
4.7U_10V_0805
C376
0.1u_X7R
C372
1u/10V
CN19
USB dongle
Z2405
TV_USB-
TV_USB+
R1007
R1009
T_BT_DATA
T_BT_CLK
Z2407
MINI_RFON
R319
0 = enable
1 = disable
Modify 26
Modify 29
R564
R217
R220
R567
DVI_USB+
TV_USB-
DVI_USB-
USB_PN1
USB_PP1
Modify 29
Reserve 1 pin for S50 Remote control
R141
0_0805_OP
Z2406
C182
4.7U_10V_0805_OP
C178
0.1u_Y5V_0402_OP
C177
1u/6.3V_0402_OP
CN13
TV-tuner_OP
CN8
GLAN CON
MX0-
MX0+
MX3+
MX3-
MX1+
MX1-
MX2-
MX2+
why not +5V
+5VS
CN1
DC_USB_CON_FFC
C378
0.1u_OP
USB_PN6
USB_PP6
USB_PN7
USB_PP7
Q56
2N7002
Q57
2N7002
DK_CRT_HSYNC
DK_CRT_VSYNC
DK_CRT_RED
DK_CRT_GREEN
DK_CRT_BLUE
R63
R67
R68
ROUT
GOUT
BOUT
Modify 25
R379
3.01K_1
R378
3.01K_1
Q53
2N7002
Q52
2N7002
DK_DVI_DDC_DATA
DK_DVI_DDC_CLK
DDC2DATA
DDC2CLK
HSYNC
VSYNC
R1017
R1018
T_HSYNC
T_VSYNC
Modify 27
Modify 32
DVI_HPD
R1003
T_DVI_HPD
Modify 25
CN7
TMDS CON FFC
DVI_USB-
DVI_USB+
DK_TVY_DACC_OUT
DK_TVC_DACB_OUT
TMDSCLK#
TMDSCLK
TMDSD0-
TMDSD0+
TMDSD1-
TMDSD1+
TMDSD2-
TMDSD2+
TMDSD3-
TMDSD3+
TMDSD4-
TMDSD4+
TMDSD5-
TMDSD5+
R391
0_OP
B17
0_0805
C452
0.1u_Y5V
HDMI_SPDIF
R400
0_OP
Reserve For HDMI Demo
UNIWILL COMPUTER CORP.
Title
P53IA0
Size
Document Number
3220
I/O PORT CON
Rev C
Date: Monday, February 06, 2006
Sheet 21 of 33

AMP VDD

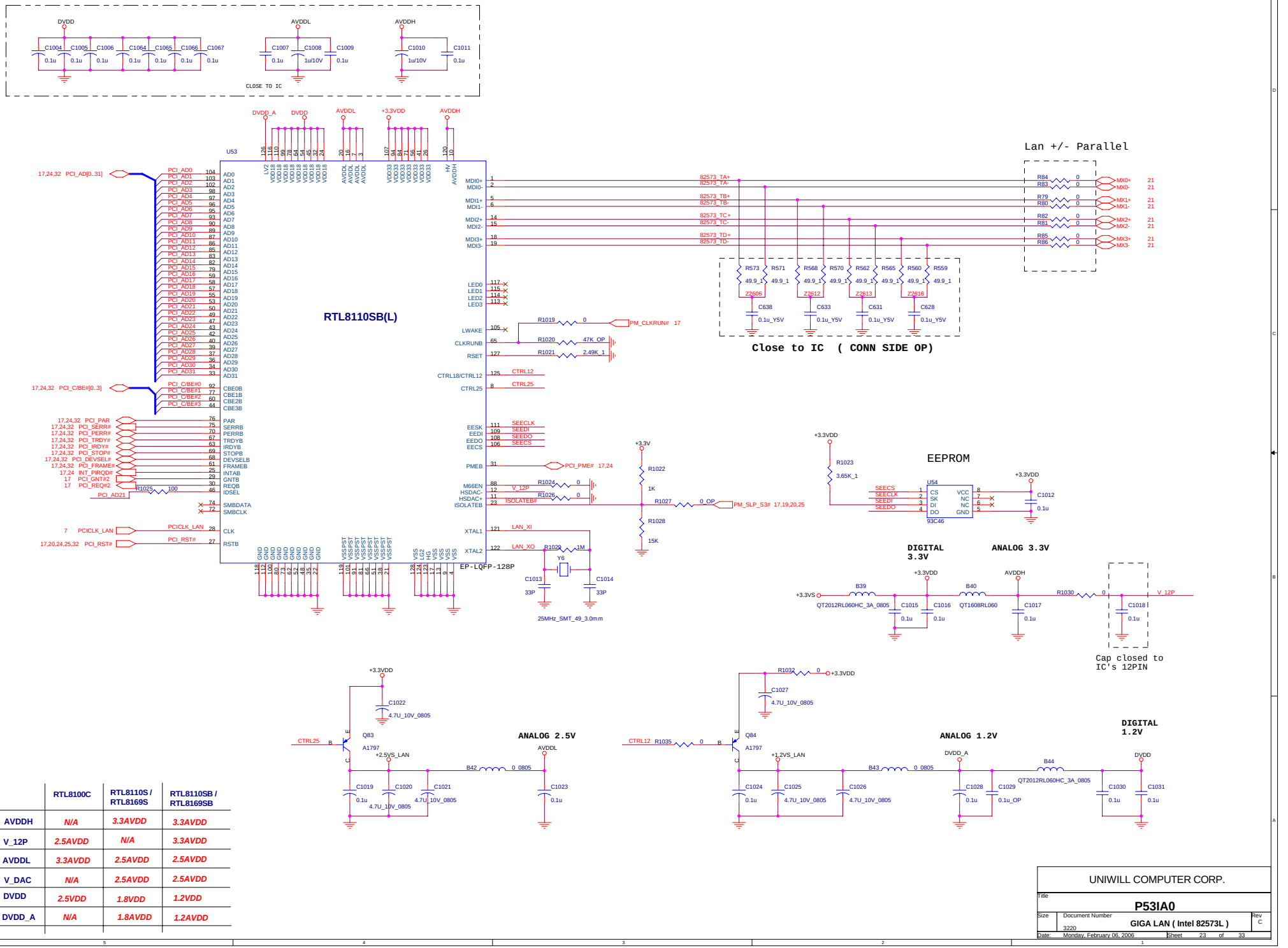




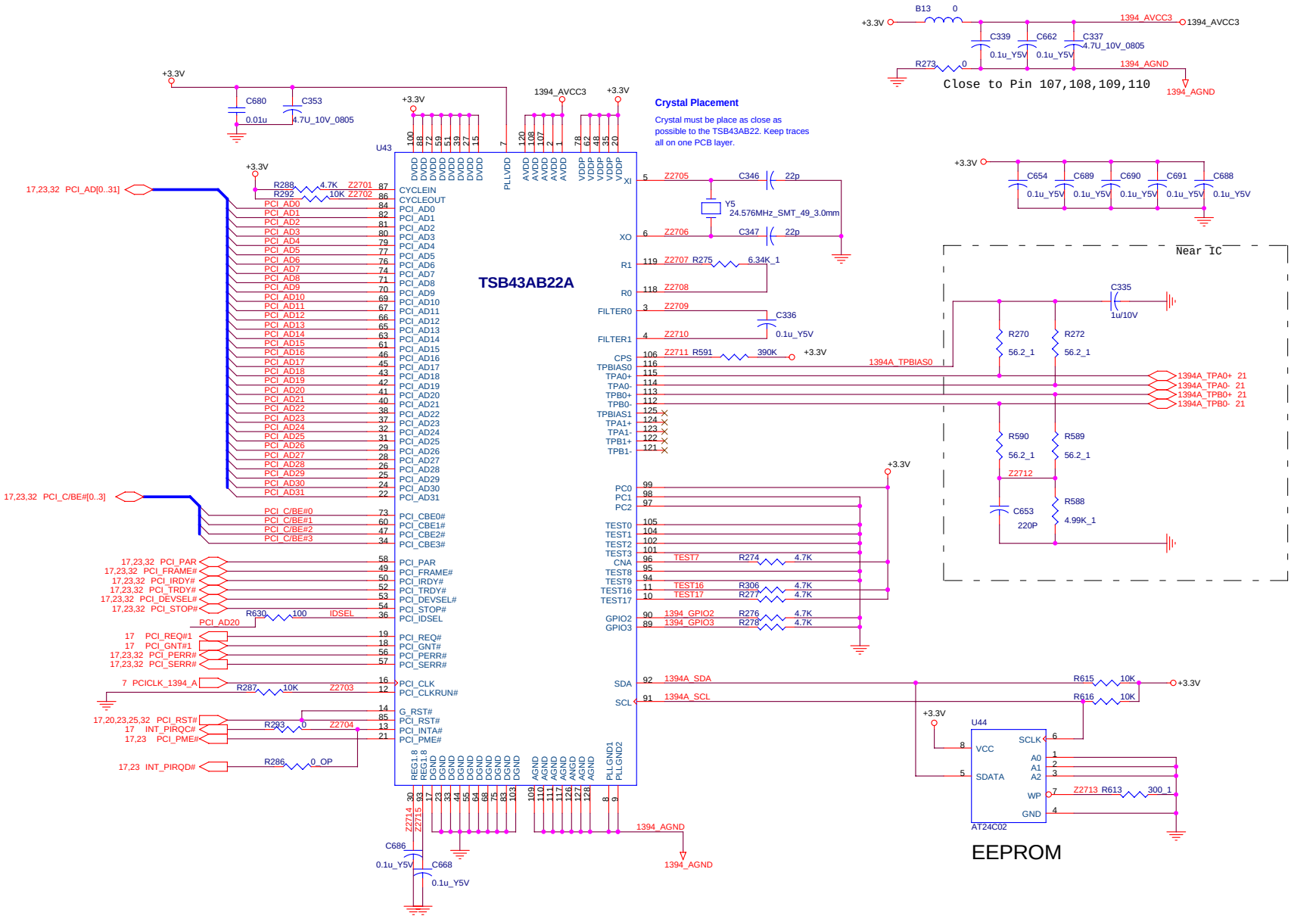
CPU FAN CONTROL



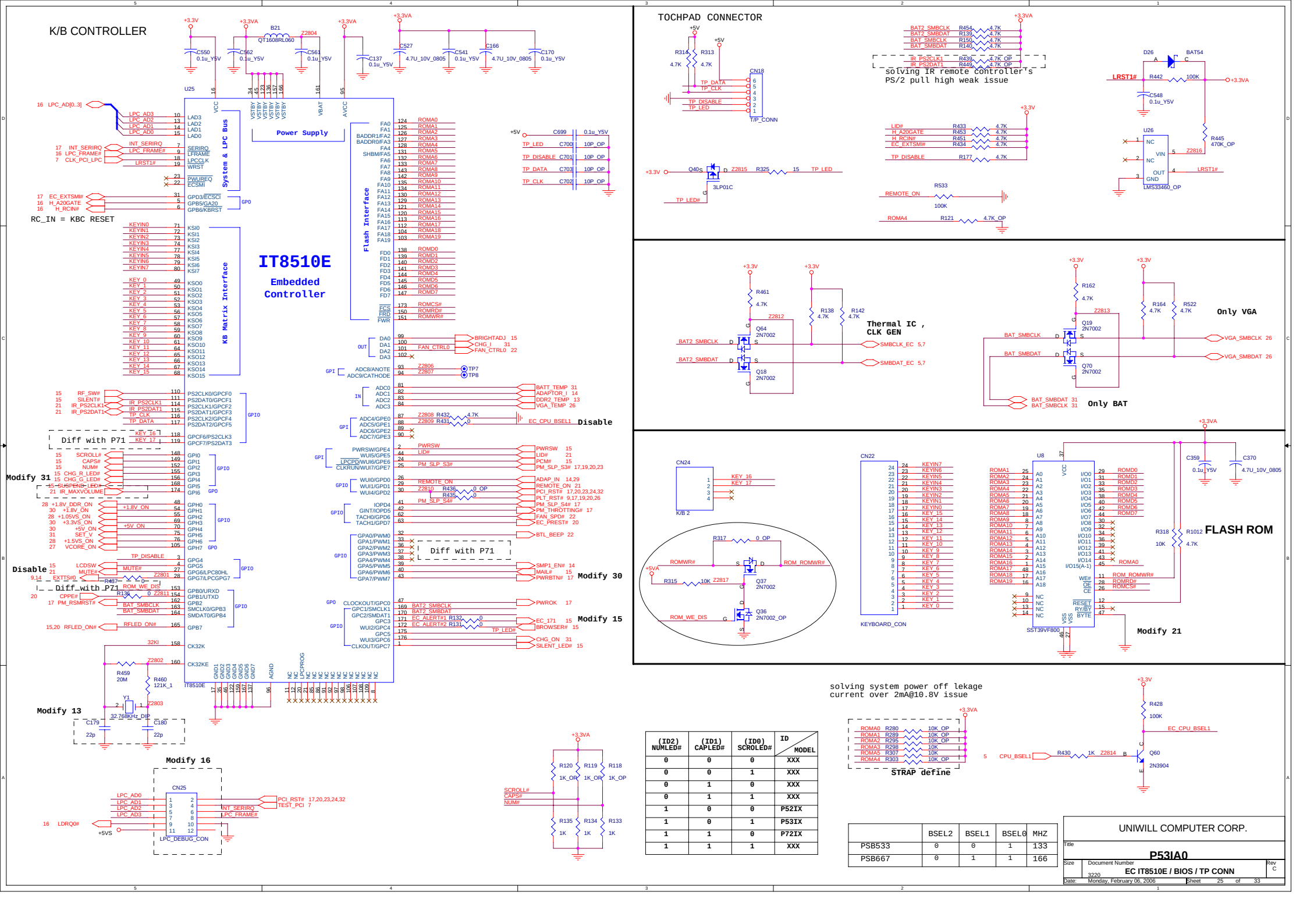
UNIWILL COMPUTER CORP.		
Title	**P53IA0**	
Size	Document Number 3220 **AUD PWR / FAN CTL**	Rev C
Date: Monday, February 06, 2006	Sheet 22 of 33	



	RTL8100C	RTL8110S / RTL8169S	RTL8110SB / RTL8169SB
AVDDH	N/A	3.3AVDD	3.3AVDD
V_12P	2.5AVDD	N/A	3.3AVDD
AVDDL	3.3AVDD	2.5AVDD	2.5AVDD
V_DAC	N/A	2.5AVDD	2.5AVDD
DVDD	2.5VDD	1.8VDD	1.2VDD
DVDD_A	N/A	1.8AVDD	1.2AVDD



Unwill International Corp.		
Title: IEEE1394A TSB43AB22		
Size	Document Number: P53IA0	Rev: C
	3220	
Date: Monday, February 06, 2006	Sheet 24 of 33	



(ID2) NUMLED#	(ID1) CAPLED#	(ID0) SCROLED#	ID / MODEL
0	0	0	XXX
0	0	1	XXX
0	1	0	XXX
0	1	1	XXX
1	0	0	P52IX
1	0	1	P53IX
1	1	0	P72IX
1	1	1	XXX

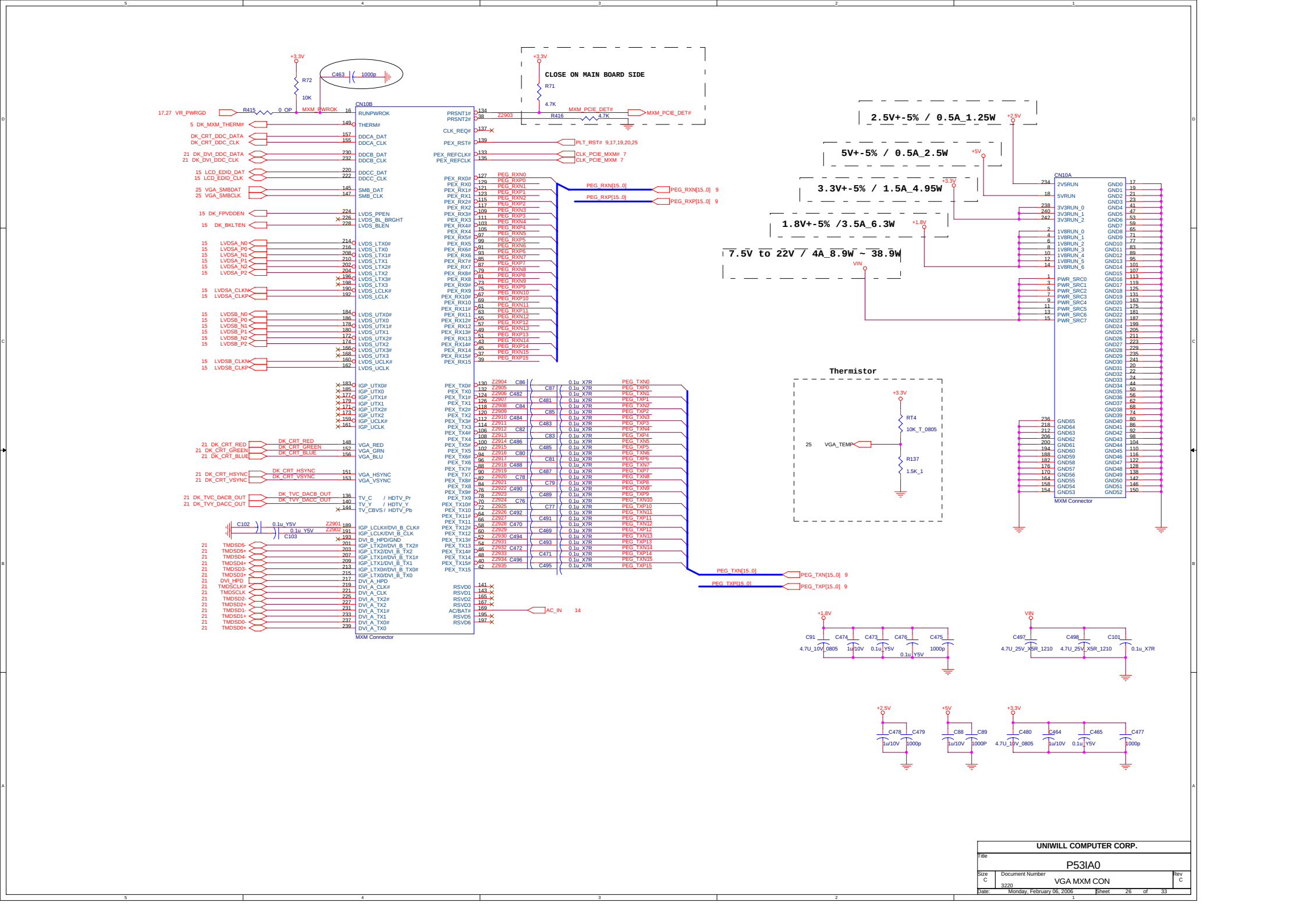
	BSEL2	BSEL1	BSEL0	MHZ
PSB533	0	0	1	133
PSB667	0	1	1	166

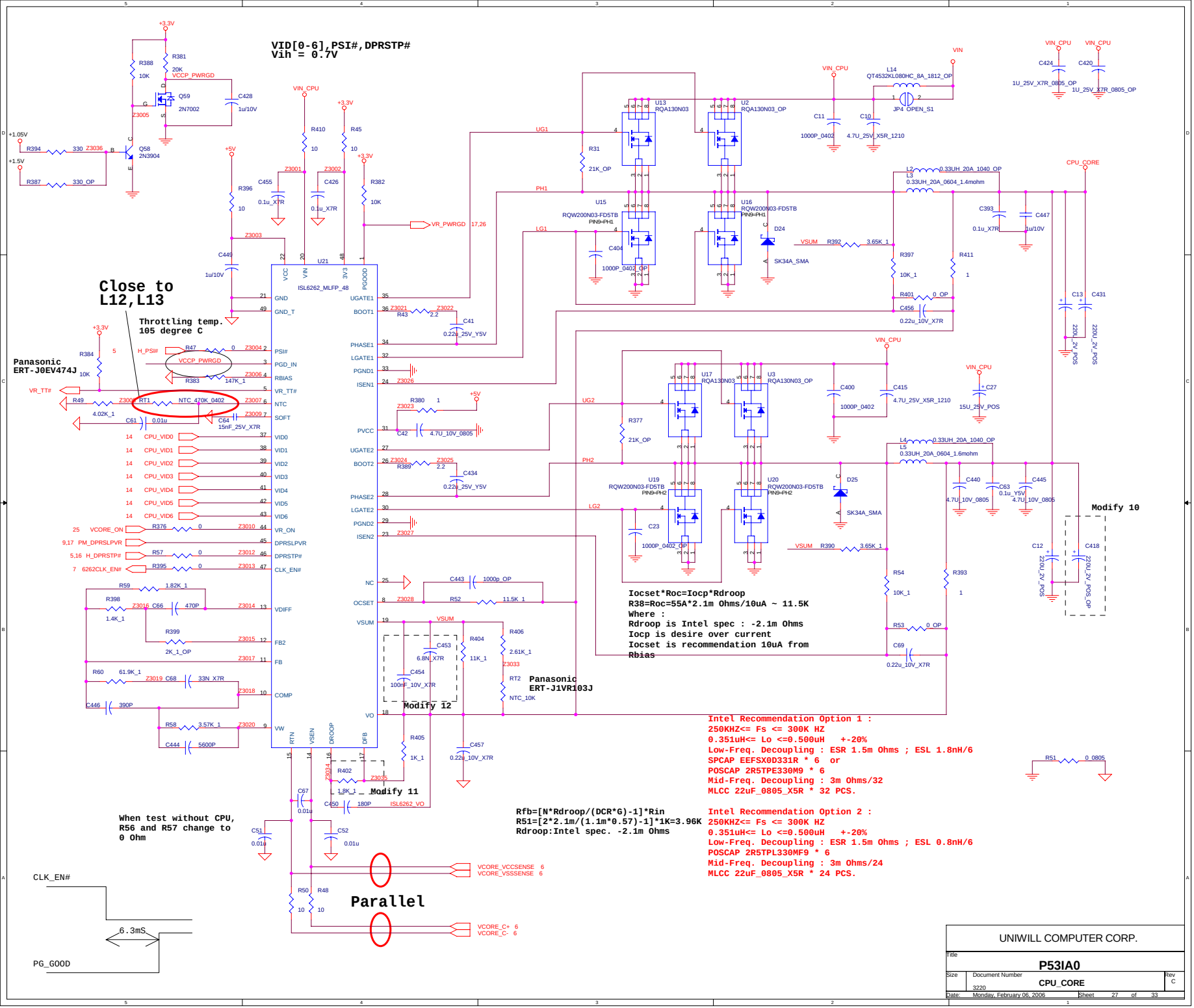
UNIWILL COMPUTER CORP.

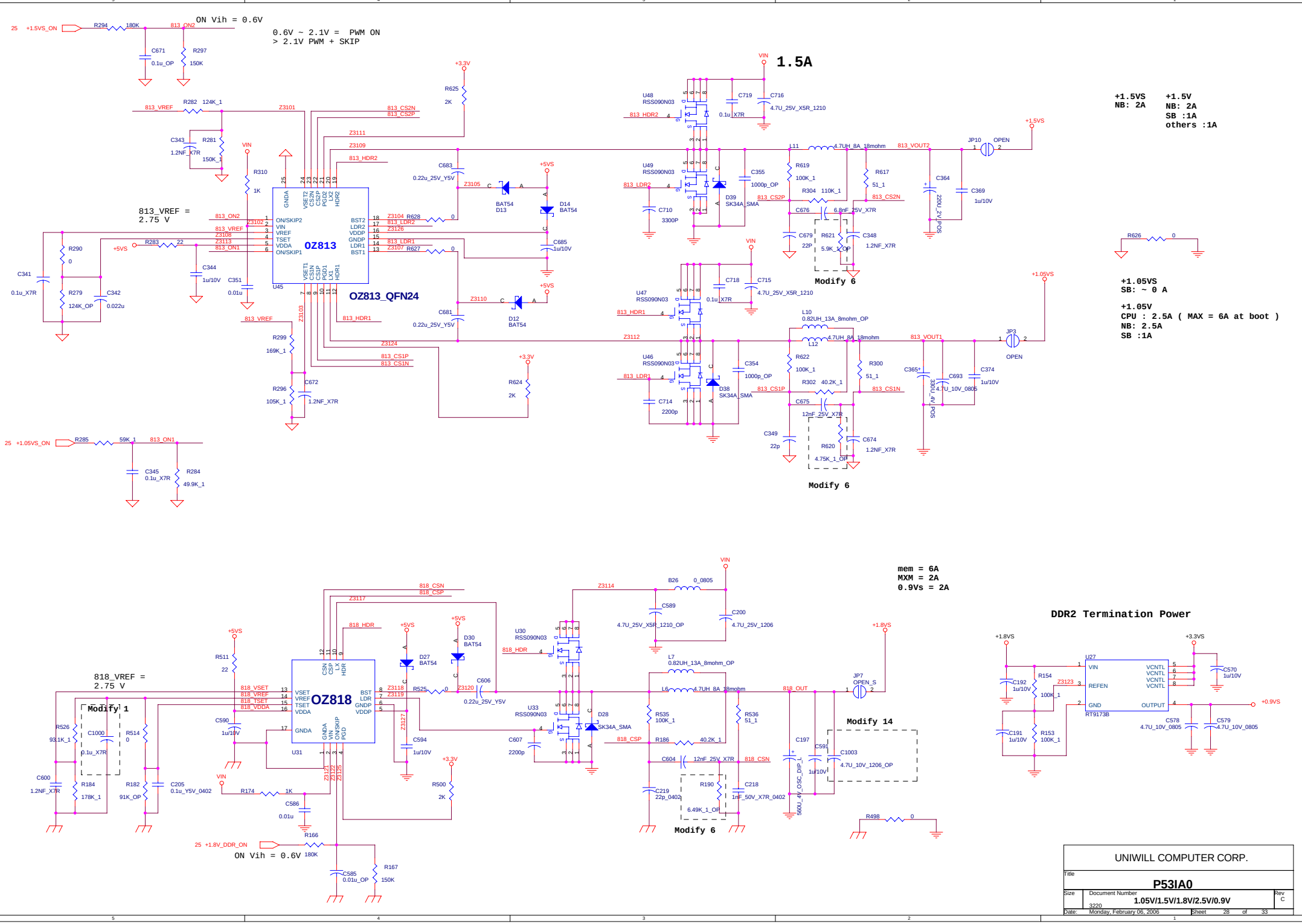
Title: P53IA0

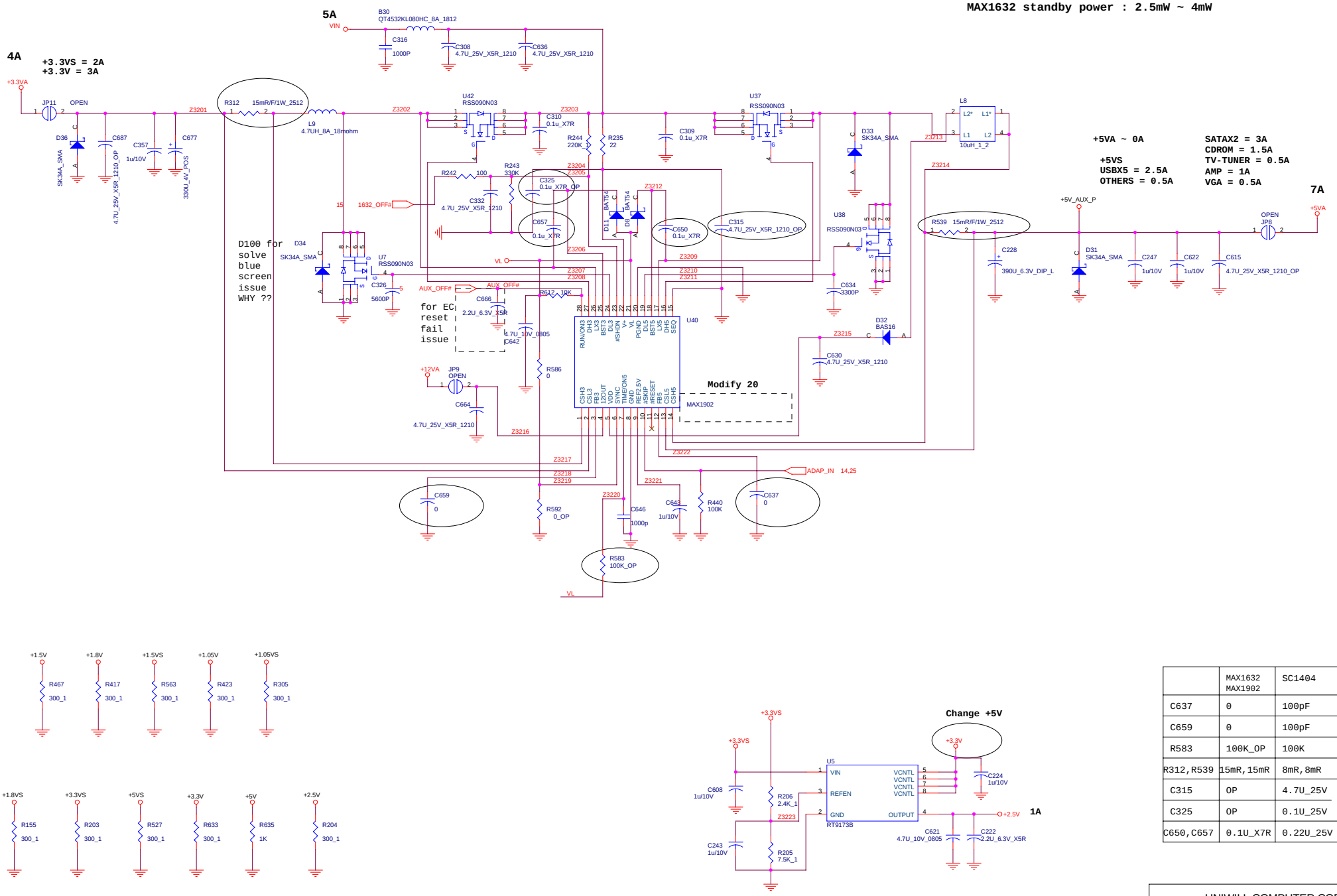
Size: Document Number: EC IT8510E / BIOS / TP CONN 3220 Rev C

Date: Monday, February 06, 2006 Sheet 25 of 33


CLOSE ON MAIN BOARD SIDE
2.5V+-5% / 0.5A_1.25W
5V+-5% / 0.5A_2.5W
3.3V+-5% / 1.5A_4.95W
1.8V+-5% /3.5A_6.3W
7.5V to 22V / 4A_8.9W ~ 38.9W
Thermistor
CN10B
MXM Connector
CN10A
MXM Connector
UNIWILL COMPUTER CORP.
P53IA0
VGA MXM CON
Monday, February 06, 2006


VID[0-6],PSI#,DPRSTP#
Vih = 0.7V
Close to
L12,L13
Throttling temp.
105 degree C
Panasonic
ERT-J0EV474J
ISL6262_MLFP_48
Iocset*Roc=Iocp*Rdroop
R38=Roc=55A*2.1m Ohms/10uA ~ 11.5K
Where :
Rdroop is Intel spec : -2.1m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from
Rbias
Panasonic
ERT-J1VR103J
Modify 10
Modify 12
Modify 11
When test without CPU,
R56 and R57 change to
0 Ohm
Rfb=[N*Rdroop/(DCR*G)-1]*Rin
R51=[2*2.1m/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms
Intel Recommendation Option 1 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
SPCAP EEFSX0D331R * 6 or
POSCAP 2R5TPE330M9 * 6
Mid-Freq. Decoupling : 3m Ohms/32
MLCC 22uF_0805_X5R * 32 PCS.
Intel Recommendation Option 2 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
POSCAP 2R5TPL330MF9 * 6
Mid-Freq. Decoupling : 3m Ohms/24
MLCC 22uF_0805_X5R * 24 PCS.
Parallel
CLK_EN#
6.3mS
PG_GOOD
UNIWILL COMPUTER CORP.
P53IA0
CPU_CORE
Monday, February 06, 2006
27 of 33


ON Vih = 0.6V
0.6V ~ 2.1V = PWM ON
> 2.1V PWM + SKIP
1.5A
OZ813
OZ813_QFN24
813_VREF = 2.75 V
Modify 6
+1.5VS NB: 2A
+1.5V NB: 2A SB :1A others :1A
+1.05VS SB: ~ 0 A
+1.05V CPU : 2.5A (MAX = 6A at boot) NB: 2.5A SB :1A
mem = 6A MXM = 2A 0.9Vs = 2A
DDR2 Termination Power
OZ818
818_VREF = 2.75 V
Modify 1
Modify 14
ON Vih = 0.6V
UNIWILL COMPUTER CORP.
P53IA0
1.05V/1.5V/1.8V/2.5V/0.9V
3220
Monday, February 06, 2006
Sheet 28 of 33



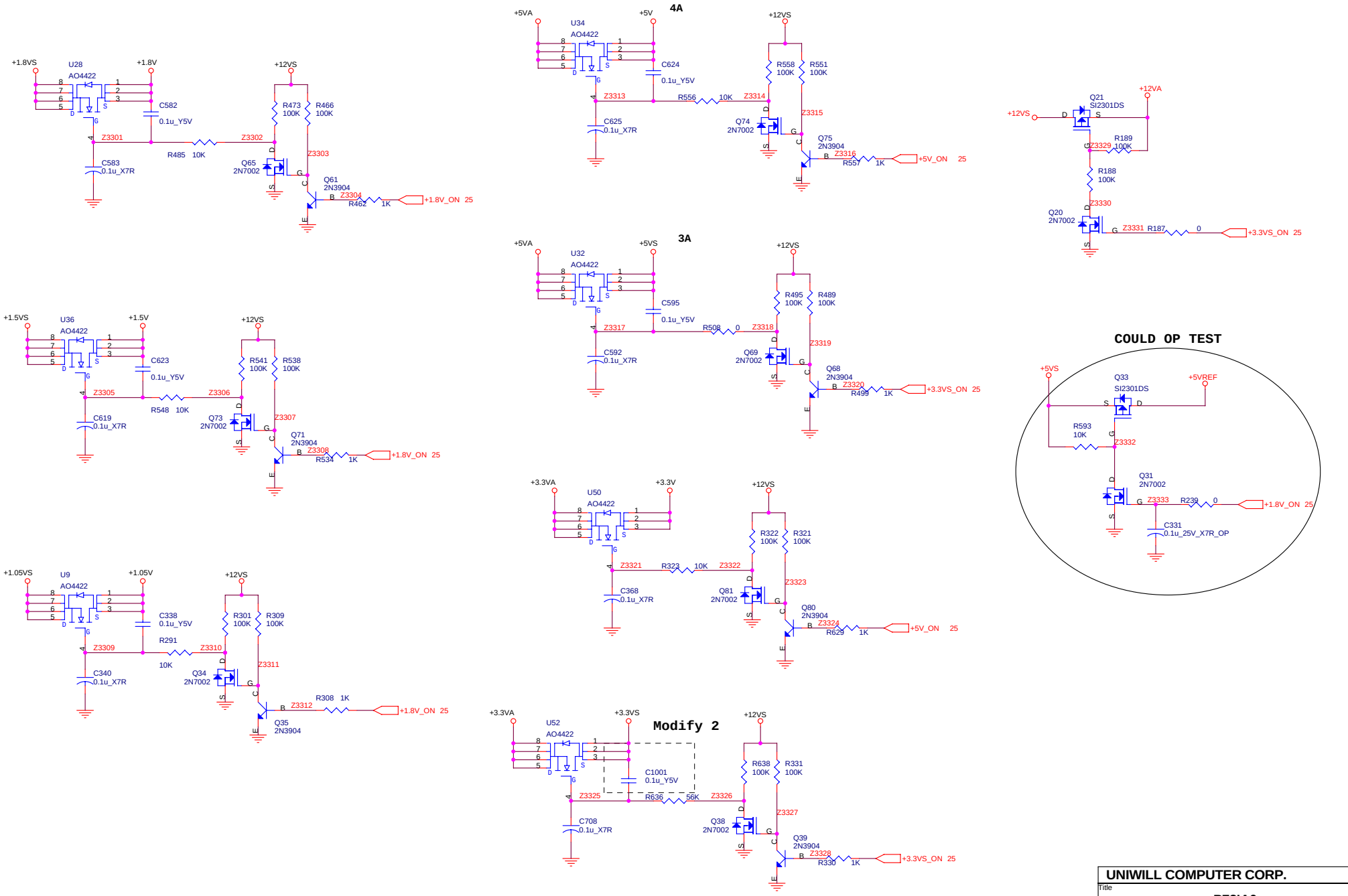
	MAX1632 MAX1902	SC1404
C637	0	100pF
C659	0	100pF
R583	100K_OP	100K
R312,R539	15mR,15mR	8mR,8mR
C315	OP	4.7U_25V
C325	OP	0.1U_25V
C650,C657	0.1U_X7R	0.22U_25V

UNIWILL COMPUTER CORP.

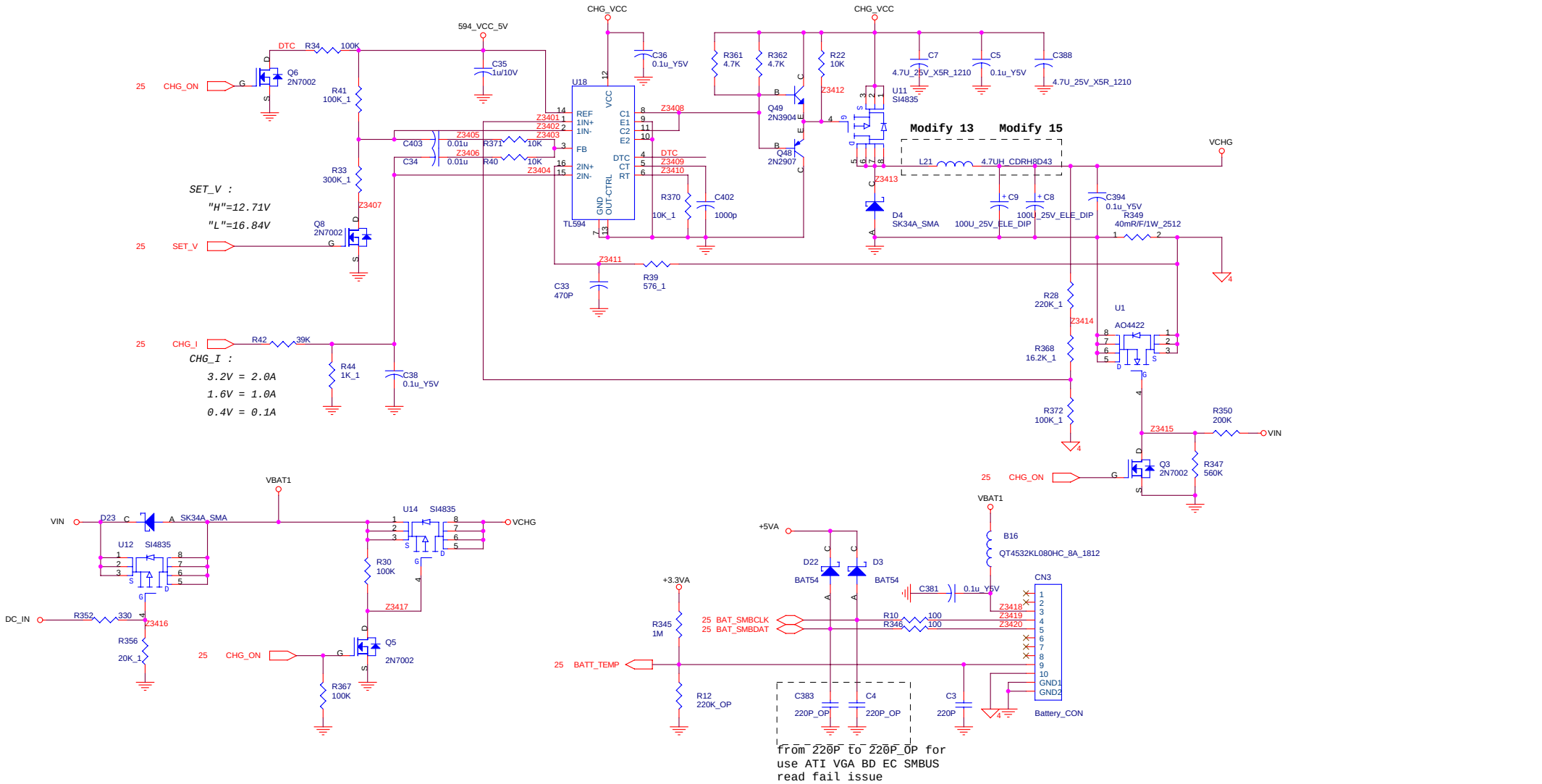
Title: P53IA0

Size: | Document Number: 3220 | +3.3VA/+5VA/+12VA | Rev: C

Date: Monday, February 06, 2006 | Sheet 29 of 33



UNIWILL COMPUTER CORP.		
Title: P72IA0		
Size: Custom	Document Number: P53IA0 3220 — VCC SW/+1.05VS/+1.5VS	Rev: C
Date: Monday, February 06, 2006	Sheet 30 of 33	



H8 C264D107 H5 C315D154 H10 C315D154 H6 C315D154 H4 C264D107 H9 C264D107 H14 C264D107 H20 C264D107 H19 C264D107 H13 C264D107 H12 C264D107 H3 C264D107

H11 C237D111 H22 C158D158 H2 C158D158 H21 C158D158 H1 C158D158 H7 C315B178D178 H23 C256B126D126 H18 C263D103 H17 C237D111

H1000 C197D91 H1001 C197D91

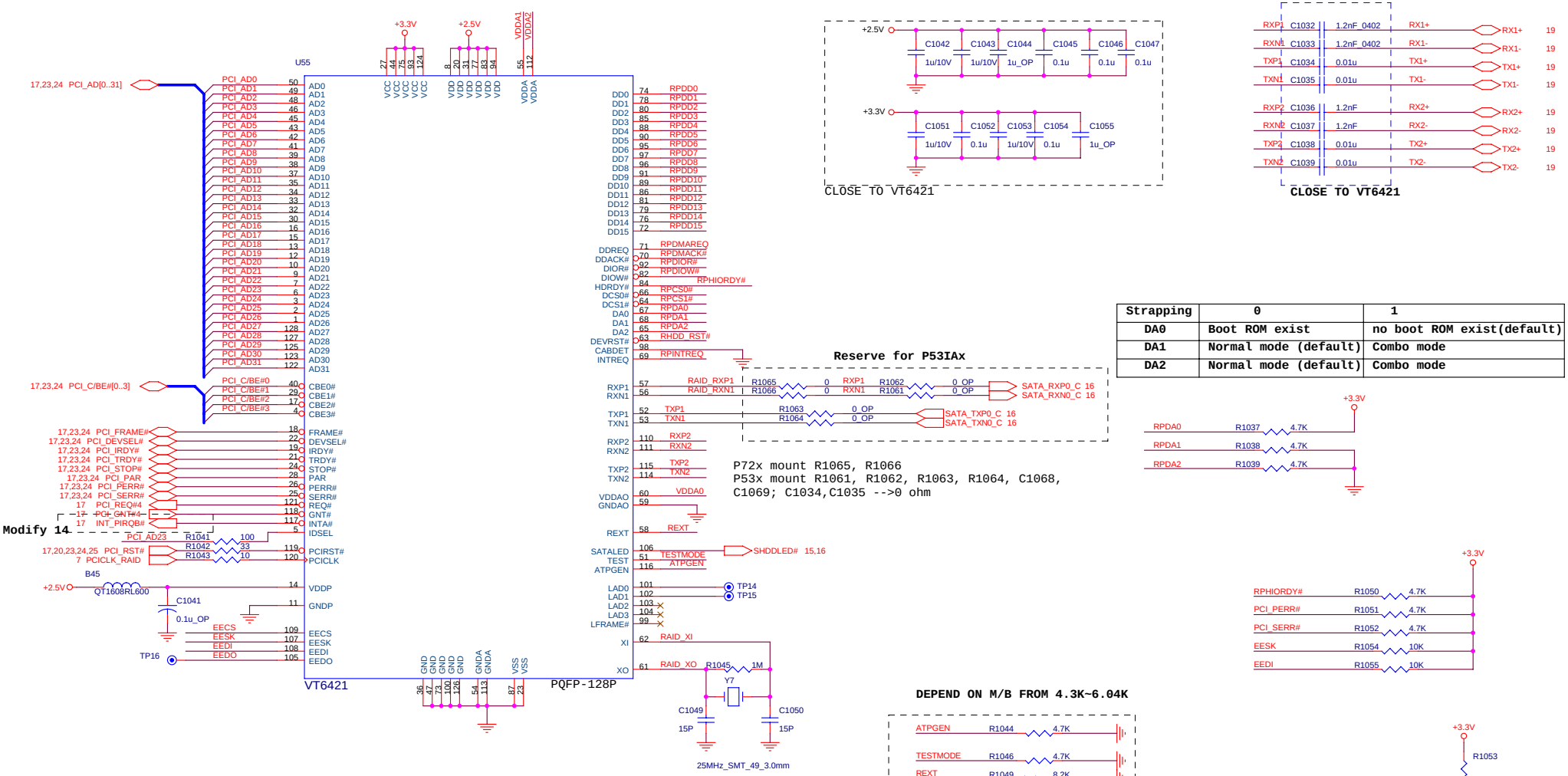
M12 M-MARK1 M15 M-MARK1 M14 M-MARK1 M16 M-MARK1 M13 M-MARK1 M19 M-MARK1 M17 M-MARK1 M20 M-MARK1 M21 M-MARK1 M18 M-MARK1 M5 M-MARK1 M4 M-MARK1 M23 M-MARK1 M6 M-MARK1 M22 M-MARK1 M7 M-MARK1 M3 M-MARK1 M24 M-MARK1 M9 M-MARK1 M25 M-MARK1 M2 M-MARK1 M10 M-MARK1 M8 M-MARK1 M11 M-MARK1 M1 M-MARK1

UNIWILL COMPUTER CORP.

Title: P53IA0

Size	Document Number	Rev
	3220 BATT IN / Charger	C

Date: Monday, February 06, 2006 Sheet 31 of 33



Strapping	0	1
DA0	Boot ROM exist	no boot ROM exist(default)
DA1	Normal mode (default)	Combo mode
DA2	Normal mode (default)	Combo mode

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Title: P53IA0

Size	Document Number	Rev
	RAID IC VT6421 3220	C

Date: Monday, February 06, 2006 Sheet 32 of 33

RA to RB change list

Modify 1 : Add one 0.1u_X7R C1000 to OZ818 Vref .

Modify 2 : Add one 0.1u_Y5V C1001 to U52 gate and source .

Modify 3 : Add R530 => 0 hom , R509 => 10K make sure PCI CLK will work fine.

Modify 4 : Reserve R1006 (10k_OP) for SB PM_DPRSLPVR sometimes will floating bug.

Modify 5 : Swap the mini-card TX , RX pairs .

Modify 6 : Change R190 , R620 , R621 OP .

Modify 7 : Change R611 OP , add R1000 , to make Mini-card RST from PCI_RST# to PLT_RST# .

Modify 8 : Change R171 to 100 Ohm , make sure USB 48M work fine with CLKGEN Ver.A .

Modify 9 : Swap HDD RXP and RXN signals.

Modify 10 : C417 and C418 OP .

Modify 11 : R402 change to 1.8K_1 for fine tune Vcore load-line.

Modify 12 : C454 change to 100NF , C453 change to 6.8N for improve Vcore dynamic ripple.

Modify 13 : Add L20&L21colay with L1 for SMT require.

RB to RC change list

Modify 14 : RAID change INT from INTA# to INTB# for IRQ routing
Modify 15 : DEL L1 and L20 for SMT required
Modify 16 : Remove R1015&R1016 for WLAN issue
Modify 17 : R326&R327 change from 20K to 24.9K ohm for solving CD gain issue.
Modify 18 : R196 change from 10K to 10pF for solving ESD issue.
Modify 19 : R520 change from 24.9 to 22.6 ohm for solving SATA Eye-patern fail issue.

Uniwill International Corp.		
Title: Appendix A. Ver. History		
Size	Document Number: P53IA0 3220	Rev: C
Date: Monday, February 06, 2006	Sheet 33 of 33	