Model : L53II0

PCB P/N:37GL53010-A1
PCBA
P/N:82GL53010-A1

Intel Merom CPU + 965GM + ICH8-M Chipset

L53II0 M/B and Daughter P/N LIST:

82GL53010-A1 37GL53010-A1	MAIN BOARD ASSY L53II0 REV.A1 PCB MAIN BD FOR L53II0 REV:A1
80G2L7020-C0 35G2L5020-C0	AUDIO BD ASSY FOR L50II REV:C PCB AUDIO BD FOR L50II0 REV:C
80G8L5000-C0 35G8L5000-C0	TOUCHPAD BD FOR L50RI0 REV:C PCB TOUCHPAD BD FOR L50RI0 REV:C
80G9L5000-C0 35G9L5000-C0	MODEM BD FOR L50RI0 REV:C PCB MODEM BD FOR L50RI0 REV:C
80G5L5000-C0 35G5L5000-C0	SWITCH BD FOR L50RI0 REV:C PCB SWITCH BD FOR L50RI0 REV:C
80GPL5000-C0 35GPL5000-C0	ODD BD FOR L50RI0 REV:C PCB ODD BD FOR L50RIO REV:C
80GJL5100-B0 35GJL5100-B0	3G BD FOR L50AI0 REV:B0 PCB 3G BD FOR L50AIO REV:B0
80GYL5310-A0 35GYL5310-A0	IR BD FOR L50IIX REV:A PCB IR BD FOR L53IIX VER:A

PCB STACK UP

LAYER1:TOP
LAYER2:GND
LAYER3:IN1
LAYER4:IN2
LAYER5:GND1
LAYER6:IN3
LAYER7:VCC
LAYER8:BOT

L53II0 M/B Affiliated FFC/Cable P/N LIST:

80G2L7020-C0	AUDIO BD ASSY FOR L50II REV:C		
1st	29GL50041-00	FFC AUDIO L50 HB	To Mother board
2nd	29GL50041-10	FFC AUDIO L50 JH	
3rd	29GL50041-20	FFC AUDIO L50 HF	
1st	29GL50080-00	CABLE SPK 4 OHM 28N04E2 L50 FG	To Audio board
2nd	29GL50085-00	CABLE SPK HB28C 4O1.5W M.S.	

80G8L5000-C0	TOUCHPAD BD FOR L50RI0 R:C		
1st	29GL50040-00	FFC BT MB L50 HB	To Mother board
2nd	29GL50040-10	FFC BT MB L50 JH	
3rd	29GL50040-20	FFC BT MB L50 HF	
1st	29GL50043-00	FFC TP BT L50 HB	To Mouse board
2nd	29GL50043-10	FFC TP BT L50 JH	
3rd	29GL50043-20	FFC TP BT L50 HF	

80G9L5000-C0	MODEM BD FOR L50RI0 R:C		
1st	29GL50082-00	CABLE MDC L50 HL	To Mother board
2nd	29GL50082-10	CABLE MDC L50 CMI	
3rd	29GL50082-20	CABLE MDC L50 FVC	

80GPL5000-C0	SWITCH BD ASSY L50RI0 VER.C		
1st	29GL50042-00	FFC SWITCH L50 HB	To Mother board
2nd	29GL50042-10	FFC SWITCH L50 JH	
3rd	29GL50042-20	FFC SWITCH L50 HF	

80GJL5100-B0	3G BD FOR L50AI0 REV:B0		
1st	29GL51083-10	CABLE FOR 3G BD HL L51AI/RI	To Mother board
2nd			
3rd			

80GYL5310-A0	IR BD ASSY L53II0 VER.A		
1st	29GL51083-10		To Mother board

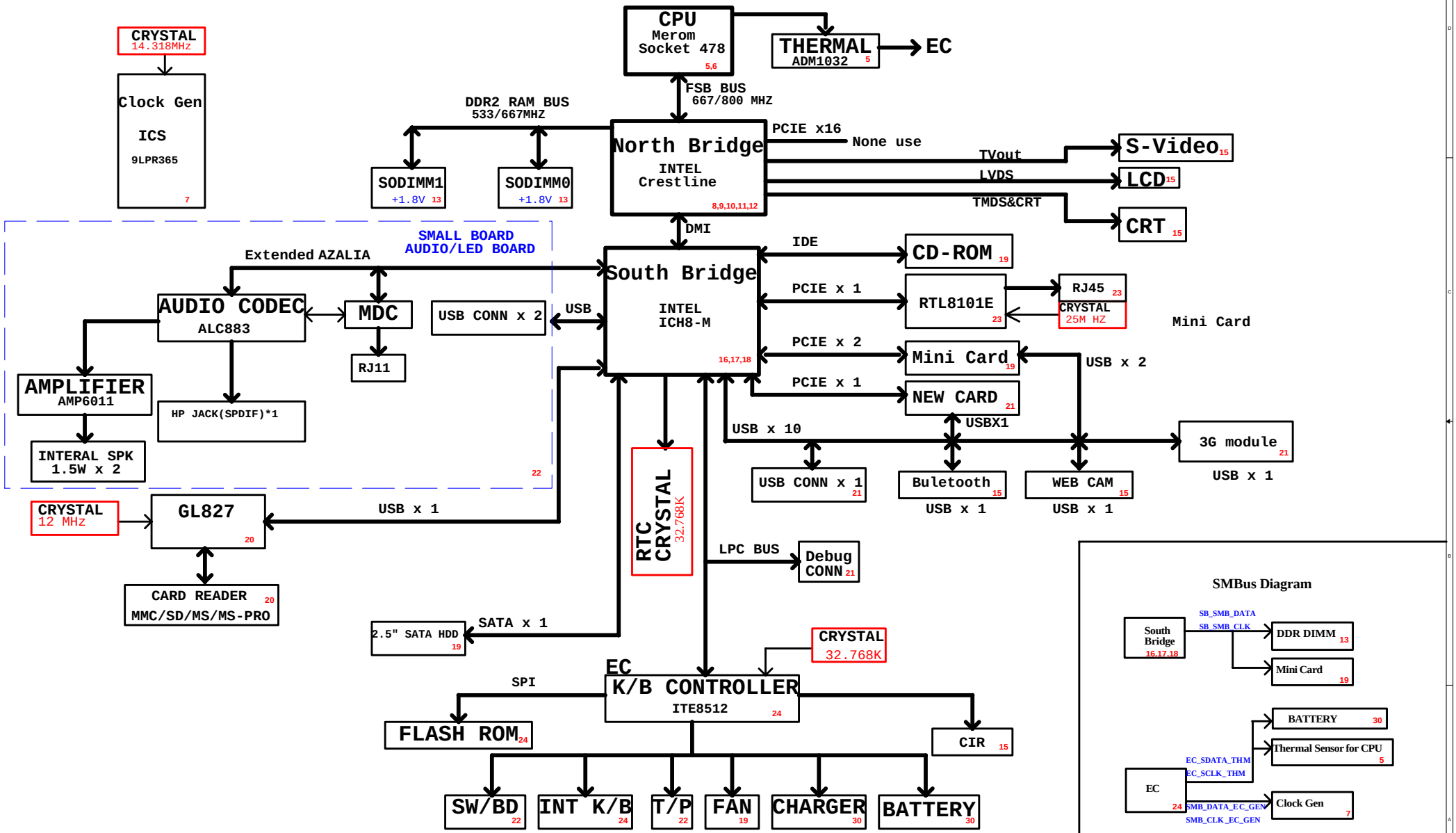
WEBCAM			
1st			To Mother board

BLUETOOTH			
1st			To Mother board

UNIWILL COMPUTER CORP.

Title	INDEX	
Size	Document Number: 3737 Custom — L53IIX	Rev A1
Date: Monday, December 18, 2006	Sheet 1 of 34	

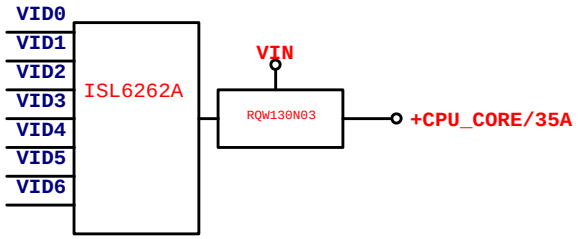
L53IIX
SYSTEM BLOCK DIAGRAM

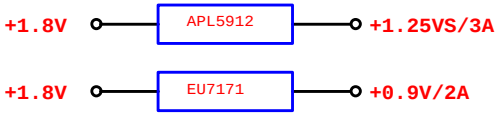


UNIWILL COMPUTER CORP.

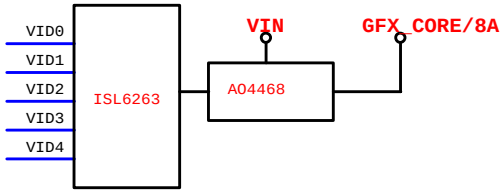
Title	SYSTEM BLOCK DIAGRAM	
Size	Document Number: L53IIX	Rev: A1
Date: Monday, December 18, 2006	Sheet 2 of 34	

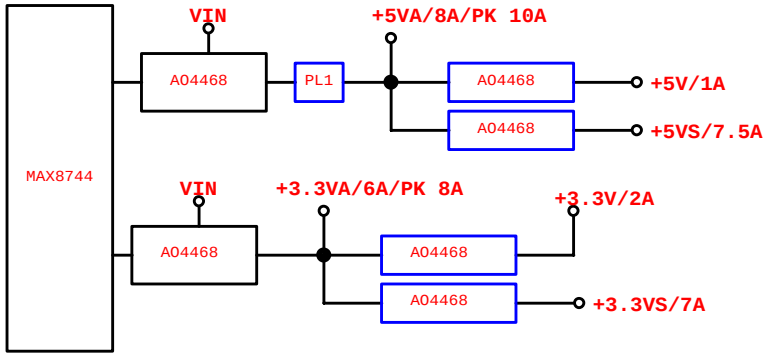
POWER BLOCK DIAGRAM

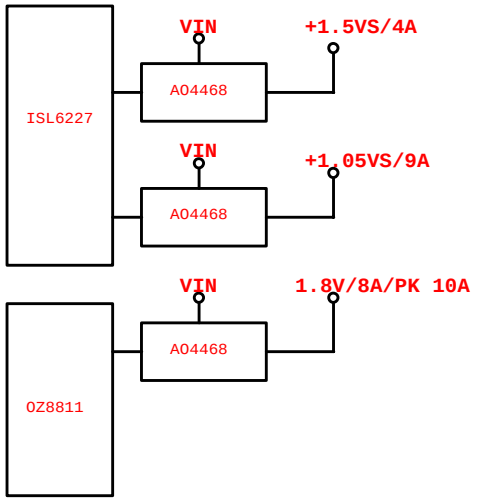


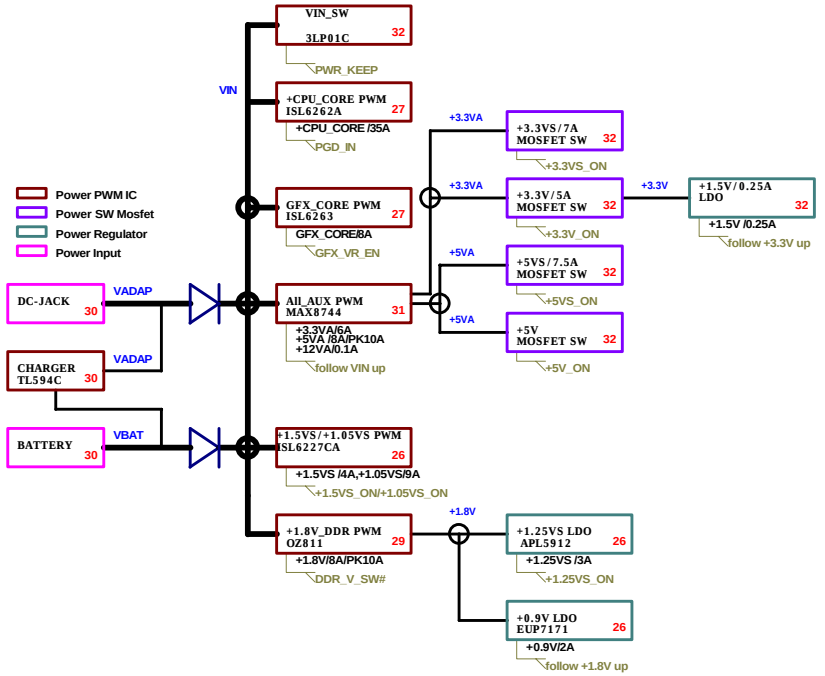


Signal / State	+*VA	+*V	+*VS	CLOCKs
S0(FULL ON)/M0	ON	ON	ON	ON
S3(Suspend to RAM)/M1	ON	ON	OFF	ON
S4(Suspend to DISK)/M1	ON	ON	OFF	ON
S5(Soft OFF)/M1	ON	ON	OFF	ON









UNIWILL COMPUTER CORP.

Title	POWER DIAGRAM	
Size	Document Number 3737 Custom L53IIX	Rev A1
Date: Monday, December 18, 2006	Sheet 3 of 34	

ICH8-M GPIO

GPIO0	PM_BM_BUSY#
GPIO1	EC_EXTSMI#
GPIO2	INT_PIRQE#
GPIO3	INT_PIRQF#
GPIO4	INT_PIRQG#
GPIO5	INT_PIRQH#
GPIO6	BIOS_REC
GPIO7	***RF_OFF#***
GPIO8	***BT_ON***
GPIO9	WOL_EN Pull low 100k
GPIO10	***GPIO10***
GPIO11	SMB_ALERT#
GPIO12	LAN_PHYPC
GPIO13	***RF_OFF#***
GPIO14	***GPIO14***
GPIO15	PM_STPPCI#
GPIO16	PM_DPRSLPVR
GPIO17	***3G_ON***
GPIO18	***GPIO18***
GPIO19	SATA1GP
GPIO20	***GPIO20***
GPIO21	SATA0GP
GPIO22	***LED_RF***
GPIO23	***N.C***
GPIO24	CRB_SV_DET
GPIO25	PM_STPCPU#
GPIO26	PM_SLP_S4_STATE#
GPIO27	***N.C***(QRT_STATE0)
GPIO28	***N.C***(QRT_STATE1)
GPIO29	USB_OC#5
GPIO30	USB_OC#6
GPIO31	USB_OC#7
GPIO32	PM_CLKRUN#
GPIO33	HDA_DOCK_EN#
GPIO34	***N.C***
GPIO35	CLK_SATA_OE#
GPIO36	SATA2GP
GPIO37	SATA3GP
GPIO38	ODD_DET
GPIO39	ICH_GPIO39
GPIO40	USB_OC#1
GPIO41	USB_OC#2
GPIO42	USB_OC#3
GPIO43	USB_OC#4
GPIO48	MFG_MODE
GPIO49	H_PWRGD
GPIO50	PCI_REQ#1
GPIO51	PCI_GNT#1
GPIO52	PCI_REQ#2
GPIO53	PCI_GNT#2
GPIO54	PCI_REQ#3
GPIO55	PCI_GNT#3
GPIO(44 ~ 47)	***NA***

ITE8512E GPIO Pin Definition list

GPA0	BTL_BEEP
GPA1	NC
GPA2	EC_VID2
GPA3	EC_VID3
GPA4	EC_VID4
GPA5	EC_VID5
GPA6	SMP_100MV_EN#
GPA7	SMP_50MV_EN#
GPB0	LED_PWR
GPB1	+3.3V_ON
GPB2	NC
GPB3	SMB_CLK_BAT
GPB4	SMB_DATA_BAT
GPB5	H_A20GATE
GPB6	H_RCIN#
GPB7	MUTE_AMP#
GPC0	IR_RX
GPC1	SMB_CLK_EC_GEN
GPC2	SMB_DATA_EC_GEN
GPC3	SMP2_EN#
GPC4	PWR_KEEP
GPC5	EC_SKIP
GPC6	SB-PWRBTN#
GPC7	DDR_V_SW#
GPD0	AC_IN
GPD1	H_PROCHOT_EC#
GPD2	PLT_RST#
GPD3	ECSCI#
GPD4	EC_EXTSMI#_A
GPD5	CHR_R
GPD6	FAN_SPEED#
GPD7	RF_SW_ON#
GPE0	PM_RSMRST#
GPE1	PM_PWROK_SB
GPE2	PGD_IN
GPE3	INTERNET#
GPE4	PWR_SW
GPE5	NEWCARD_PWRON
GPE6	NEWCARD_PERST#
GPE7	NEWCARD_CPPE#
GPF0	SILENT_ON#
GPF1	LED_CAP
GPF2	LED_NUM
GPF3	SILENT_LED
GPF4	PS2_CLK_TP
GPF5	PS2_DATA_TP
GPF6	CHR_G
GPF7	CHR_R
GPH0	+CPU_CORE_ON
GPH1	+1.05VS_ON
GPH2	+1.5VS_ON
GPH3	+3.3VS_ON
GPH4	+5VS_ON
GPH5	+1.8V_ON
GPH6	+1.25VS_ON
GPG1	+5V_ON
ADC0/GPI0	BATT_TEMP
ADC1/GPI1	ADAPTOR_I
ADC2/GPI2	BAT_I
ADC3/GPI3	BAT_V
ADC4/GPI4	PM_SLP_S4#
ADC5/GPI5	PM_SLP_S3#
ADC6/GPI6	EC_CPU_200MHz
ADC7/GPI7	WEBCAM_SW

ITE8512E GPIO Pin Definition list

DAC0/GPJ0	BRIGHTNESS
DAC0/GPJ1	CHG_I
DAC0/GPJ2	FAN_CTRL0
DAC0/GPJ3	CHG_ON
DAC0/GPJ4	SENBAT_V
DAC0/GPJ5	CHG_V

ITE8512E KB Matrlk interface

KSI0/STB#	KB_SIN0
KSI1/AFD#	KB_SIN1
KSI0/STB#	KB_SIN2
KSI3SLIN#	KB_SIN3
KSI4	KB_SIN4
KSI5	KB_SIN5
KSI6	KB_SIN6
KSI7	KB_SIN7
KSO0/PD0	KB_SOUT0
KSO1/PD1	KB_SOUT1
KSO2/PD2	KB_SOUT2
KSO2/PD3	KB_SOUT3
KSO2/PD4	KB_SOUT4
KSO2/PD5	KB_SOUT5
KSO2/PD6	KB_SOUT6
KSO2/PD7	KB_SOUT7
KSO8/ACK#	KB_SOUT8
KSO9/BUSY	KB_SOUT9
KSO10/PE	KB_SOUT10
KSO11/ERR#	KB_SOUT11
KSO12/SLCT	KB_SOUT12
KSO13	KB_SOUT13
KSO14	KB_SOUT14
KSO15	KB_SOUT15

ITE8512E SPI Flash ROM interface

FLFRAME#/GPG2	FLFRAME#
FLAD0/SCE#	SPI_CE#
FLAD1/S1	SPI_DIN
FLAD2/S2	SPI_DOUT
FLAD3/GPG6	***N.C***
FLCLK/SCK	SPI_CLK
FLRST#/WU17 /GPG0/IM	***N.C***

ITE8512E System & LPC Bus

LAD0	LPC_AD0
LAD1	LPC_AD1
LAD2	LPC_AD2
LAD3	LPC_AD3
SERIRQ	INT_SERIRQ
LFRAME#	LPC_FRAME#
LPCCLK	CLK_PCI_LPC
WRST#	LRST#

ITE8512E Clock

CK32K	EC32KI
CK32KE	EC32KO

ITE8512E Power

VSTBY0	+3.3VA
VSTBY1	+3.3VA
VSTBY2	+3.3VA
VSTBY3	+3.3VA
VSTBY4	+3.3VA
VSTBY5	+3.3VA
VBAT	+3.3VA
AVCC	+3.3VA
VCC	+3.3VS

ITE8512E GND

AVSS	EC-AVSS-75
VSS0	GND
VSS1	GND
VSS2	GND
VSS3	GND
VSS4	GND
VSS5	GND
VSS6	GND

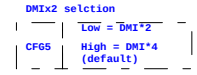
965-GM GPIO

GPIO0	MCH_BSEL0
GPIO1	MCH_BSEL1
GPIO2	MCH_BSEL2
GPIO3	***N.C***
GPIO4	***N.C***
GPIO5	CFG5(DMIx2 selction)
GPIO6	***N.C***
GPIO7	***N.C***
GPIO8	***N.C***
GPIO9	CFG9(PCIe Lane)
GPIO10	***N.C***
GPIO11	***N.C***
GPIO12	CFG12(XOR / ALLZ / Clock Un-gating)
GPIO13	CFG13(XOR / ALLZ / Clock Un-gating)
GPIO14	***N.C***
GPIO15	***N.C***
GPIO16	CFG16(FSB Dynamic ODT)
GPIO17	***N.C***
GPIO18	CFG18(NAPA design)
GPIO19	CFG19(DMI lane Reversal)
GPIO20	CFG20(SDVO/PCIE Concurrent Operation)

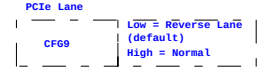
1. CFG_0 ~ CFG_2 Host clock frequency initial

CFG0	CFG1	CFG2	Host Clock Frequency
0	1	0	800
1	1	0	667

2. CFG5 DMIx2 selection



3. CFG_9 PCIe Lane



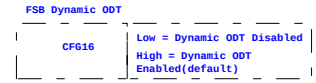
CFG[17:3] have internal pullup ressistors.

4. CFG_12 ~ CFG_13

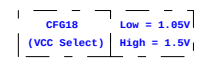
XOR / ALLZ / Clock Un-gating

CFG12	CFG13	Configuration
0	0	Clock Gating Disabled
0	1	XOR Mode Enabled
1	0	All-Z Mode Enabled
1	1	Normal Operation (Default)

5. CFG_16 FSB Dynamic ODT

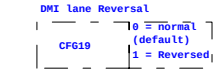


6. CFG_18 NAPA design

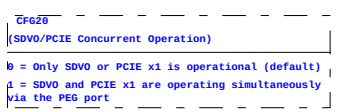


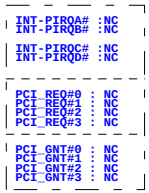
NAPA design

7. CFG_19 DMI lane Reversal



8. CFG_20 SDVO/PCIE Concurrent operation





Merom CPU

	CPU CORE(V)	ICC(A)	W	TEMP(℃)
IMVP-6+	1.25	44.0	46.2	

Crestline

VCC	ICC(mA)	W	TEMP(℃)
+3.3VS	340	1.122	105
+1.8V	3800	6.84	
+1.5VS	130	0.195	
+1.25VS	2440	3.05	
+1.05VS	4140	4.347	
+0.9V	30	0.27	
GFX_CORE	7700	8.085	

ICH8-M

VCC	ICC(mA)	mW	TEMP(℃)
+5V	2	10	70
+5VS	1	5	
+3.3VA	230	756	
+3.3VS	330	1089	
+1.5VS	2400	3600	
+1.25V	5	6.25	
+1.05V	1131	1187.55	

ITE8512E

VCC	ICC(mA)	W	TEMP(℃)
+3.3VA	300	1	70

CLOCK GENERATOR

VCC	ICC(mA)	mW	TEMP(℃)
+3.3VS	270	891	70

ADM1032

VCC	ICC	mW	TEMP(℃)
+3.3VS	170uA	0.56	150

GL827

VCC	ICC(mA)	mW	TEMP(℃)
+5VS	170	561	70

RTL8101E

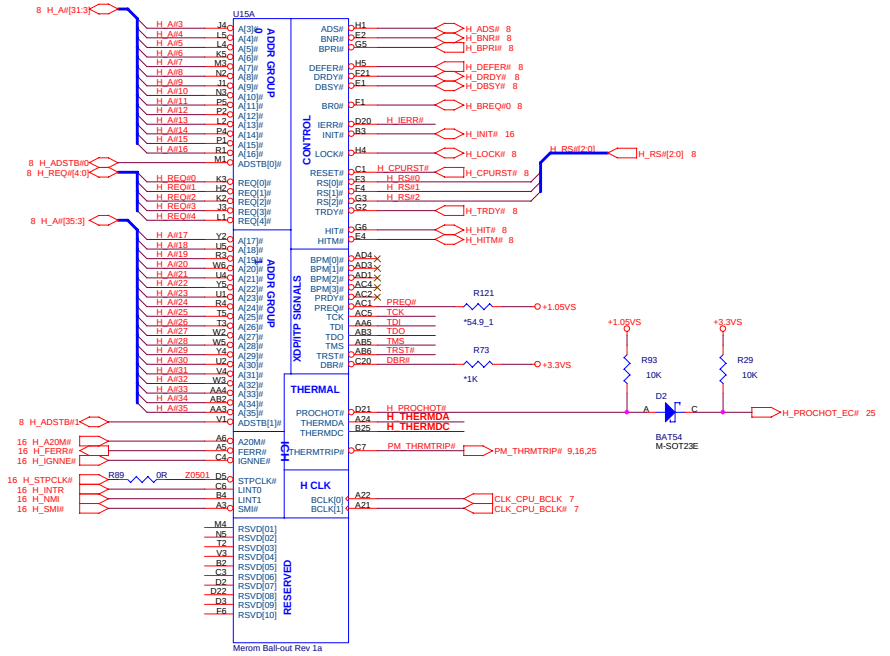
VCC	ICC(mA)	mW	TEMP(℃)
+3.3V	238	785.4	80
+1.8V	153	275.4	
+1.5V	77	115.5	

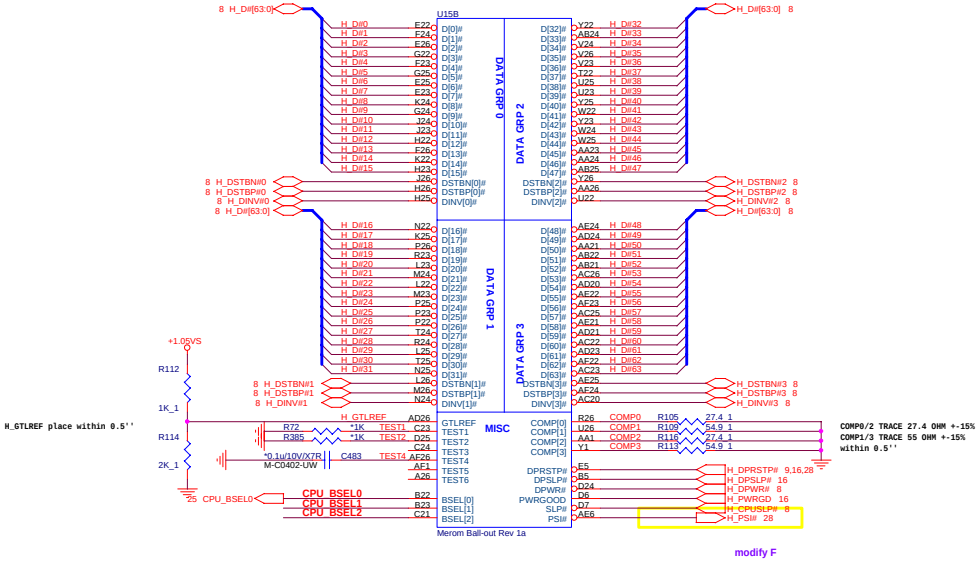
UNIWILL COMPUTER CORP.

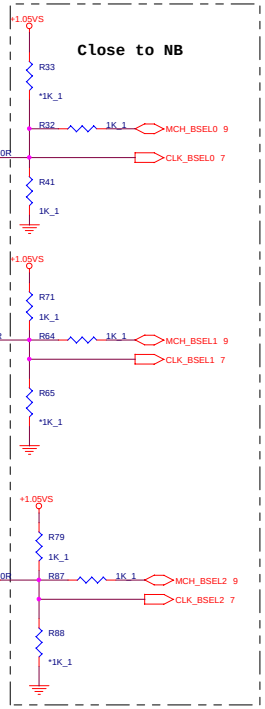
Title: GPIO & POWER CONSU

Size: 3737 Custom | Document Number: L53IIX | Rev: A1

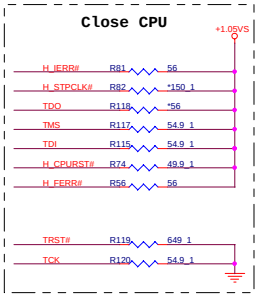
Date: Monday, December 18, 2006 | Sheet 4 of 34

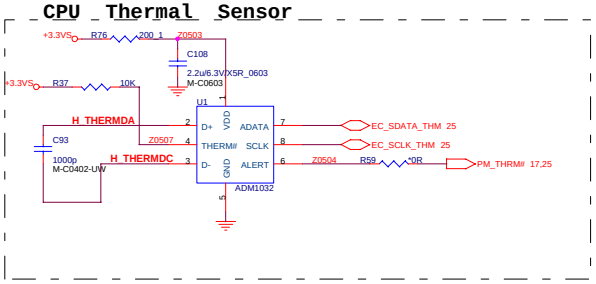


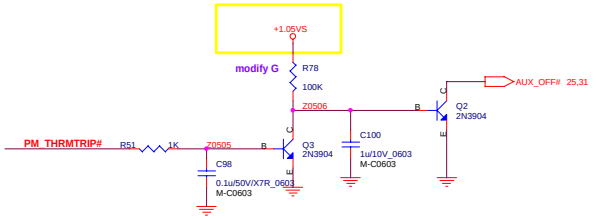




	BSEL2	BSEL1	BSEL0	MHZ
PSB800	0	1	0	200
PSB667	0	1	1	166
PSB533				133

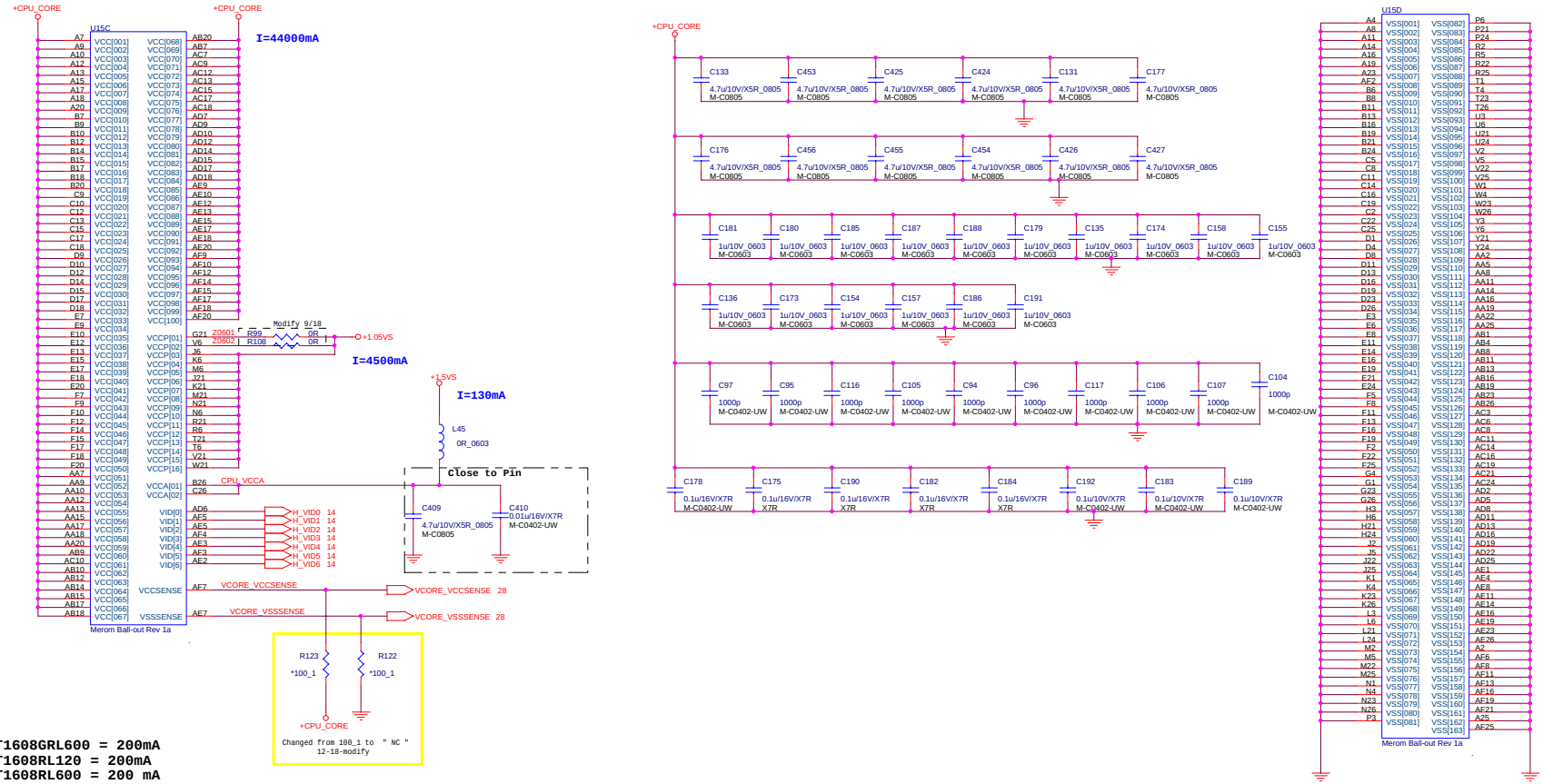






Title	CPU Merom-1/2
Size	Document Number 3737 Custom L53IIX Rev A1
Date: Monday, December 18, 2006	Sheet 5 of 34

UNIWILL COMPUTER CORP.



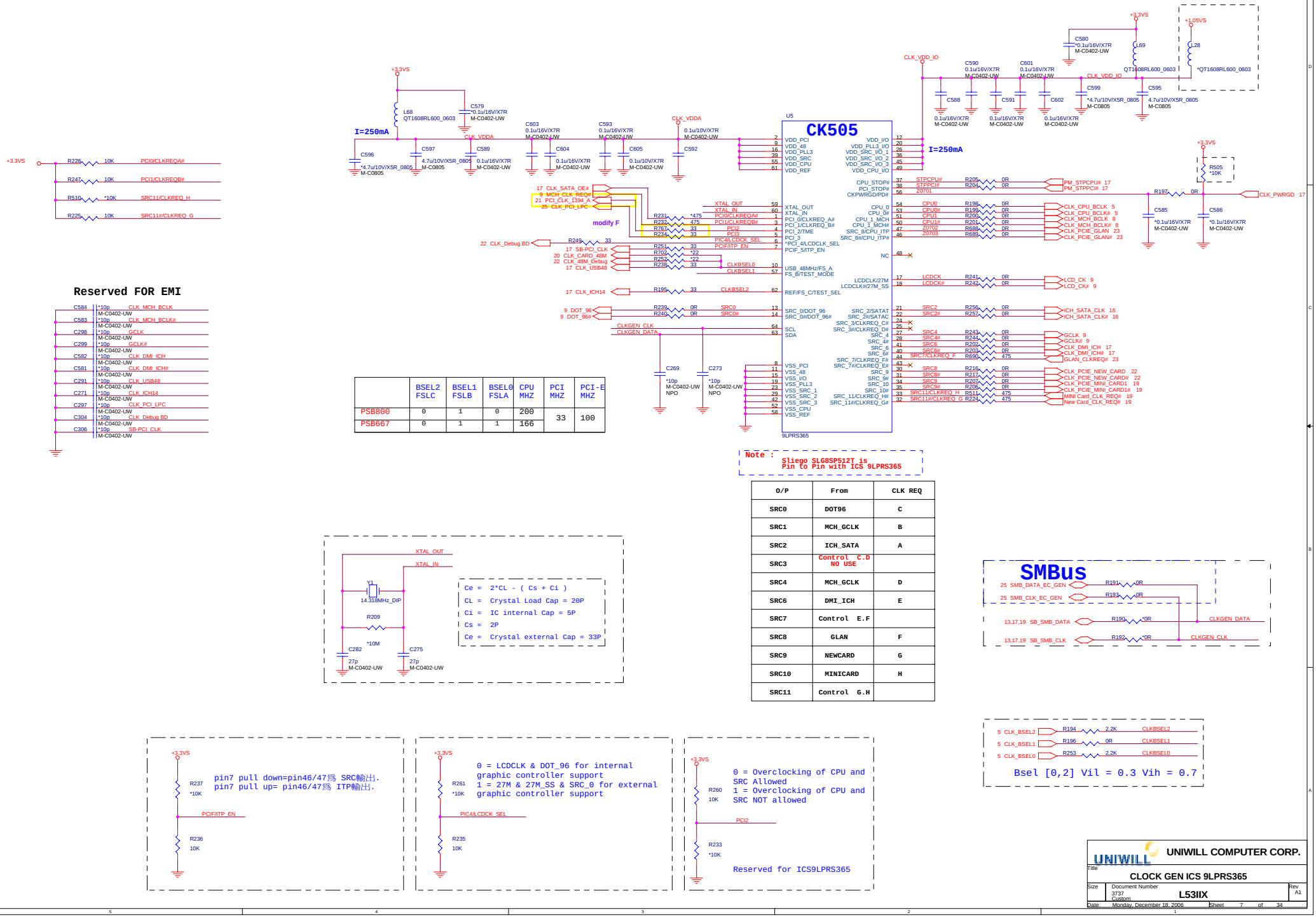
QT1608GRL600 = 200mA
QT1608RL120 = 200mA
QT1608RL600 = 200 mA
QT1608RL030 = 500mA
QT1608RL060 = 500mA

UNIWILL COMPUTER CORP.

Title: CPU Merom-1/2

Size	Document Number	Rev
3737 Custom	L53IIX	A1

Date: Monday, December 18, 2006 Sheet 6 of 34

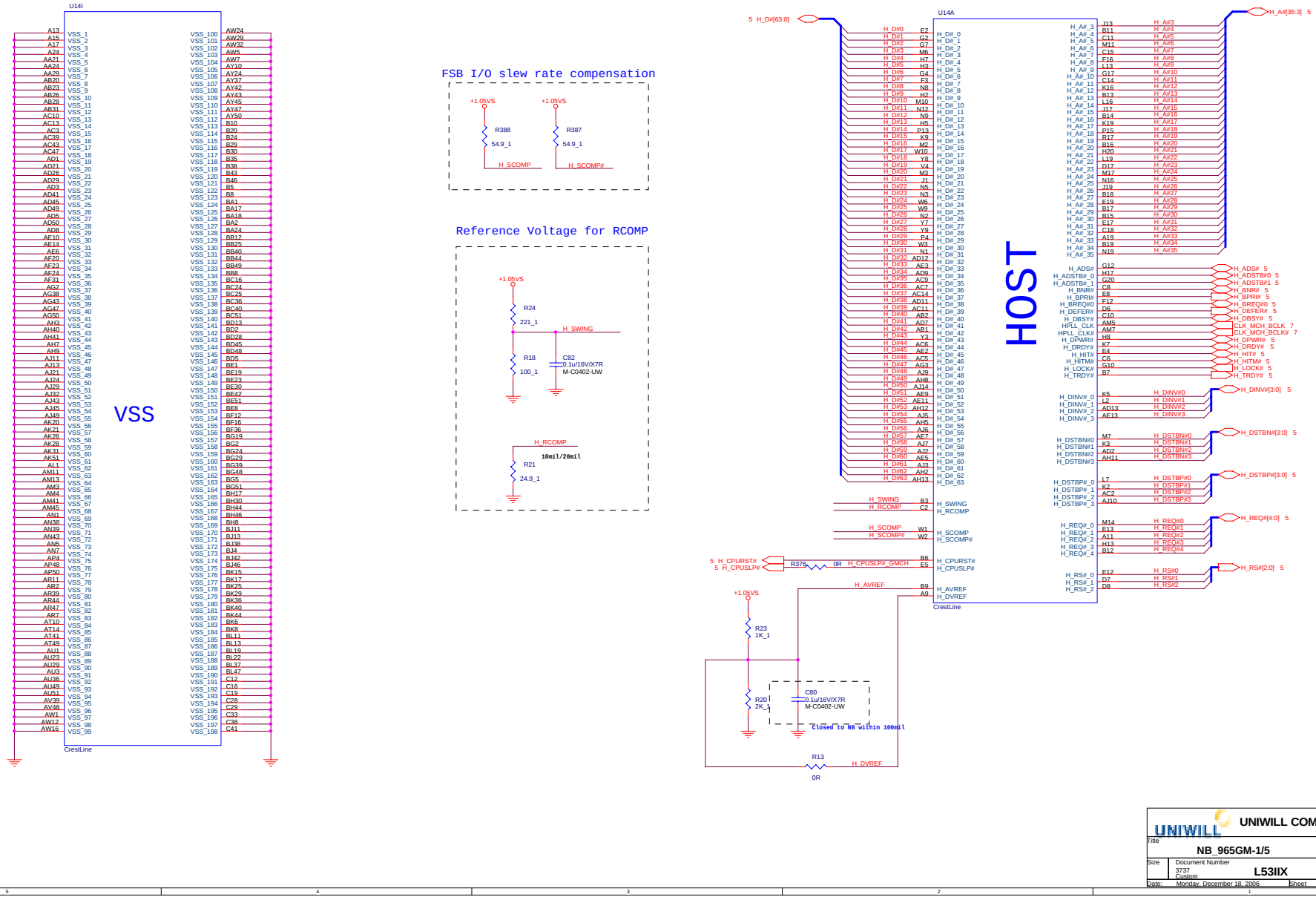


	BSEL2 FSLC	BSEL1 FSLB	BSEL0 FSLA	CPU MHZ	PCI MHZ	PCI-E MHZ
PSB800	0	1	0	200	33	100
PSB667	0	1	1	166		

O/P	From	CLK REQ
SRC0	DOT96	C
SRC1	MCH_GCLK	B
SRC2	ICH_SATA	A
SRC3	Control C.D NO USE	
SRC4	MCH_GCLK	D
SRC6	DMI_ICH	E
SRC7	Control E.F	
SRC8	GLAN	F
SRC9	NEWCARD	G
SRC10	MINICARD	H
SRC11	Control G.H	

Title	CLOCK GEN ICS 9LPRS365	
Size	Document Number 3737 Custom L53IIX	Rev A1
Date: Monday, December 18, 2006	Sheet 7 of 34	

UNIWILL COMPUTER CORP.



UNIWILL COMPUTER CORP.		
Title: NB_965GM-1/5		
Size	Document Number: 3737 Custom L53IIX	Rev: A1
Date: Monday, December 18, 2006	Sheet 8 of 34	

GCLK => PCI-E & DMI (100MHZ)
DREFCLK => Dispaly PLLA (nun- ss 96MHZ)
DRESSFCLK => Display LVDS PLLB (ss 100MHZ)

CFG0	CFG1	CFG2	Host Clock Frequency
0	1	0	800
1	1	0	667

GHCH integrated graphics busy

CFG20 (IPD) => 1= Only SDVO or PCI-E
0 = SDVO and PCI-E

CFG7 (IPU) => 1= Mobility CPU
0 = Reverse

SDVODATA has internal pull down
0= no DVO device
1= DVO device present

SDVOCLK has internal pull down .

CLK_REQ:Asserted to control the raw PCI-E clock

Reserve for NB THRMTRIP# (O/D Vccp)

Checking

For MEN bus throttling

Check with S/W

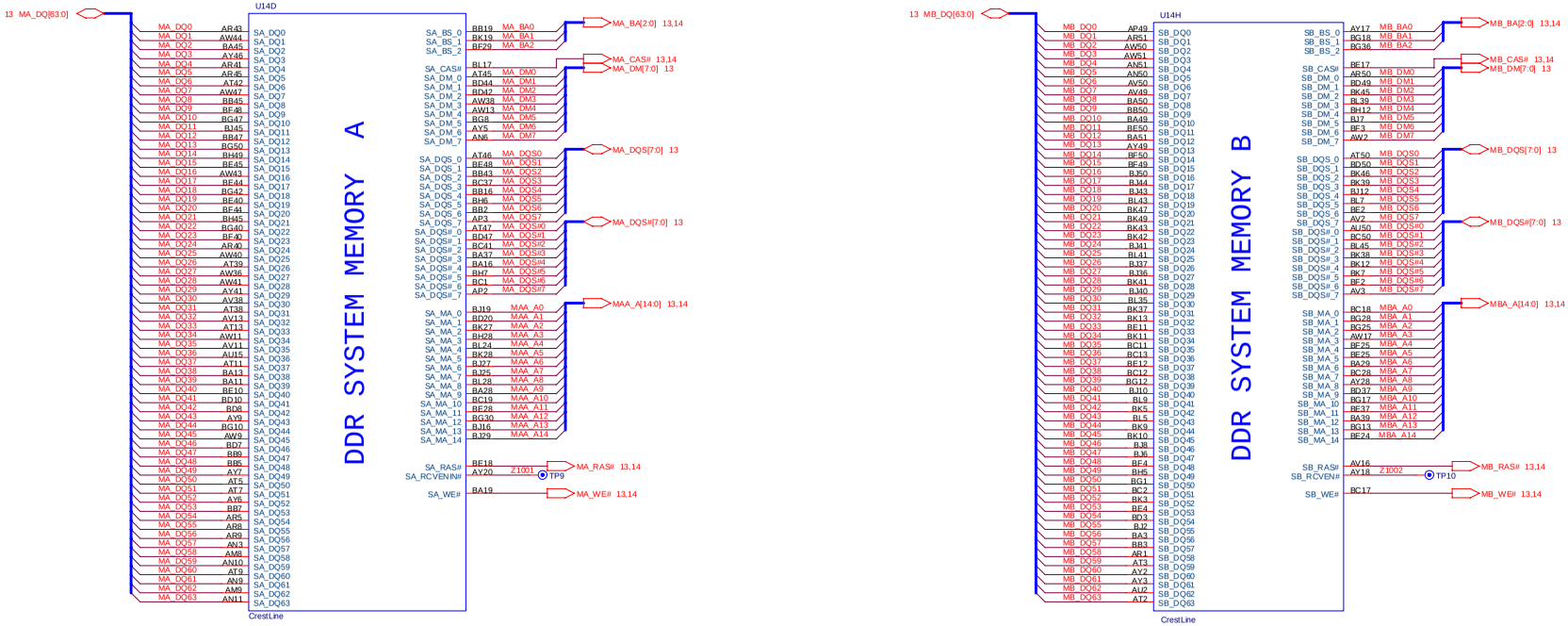
Colse to NB

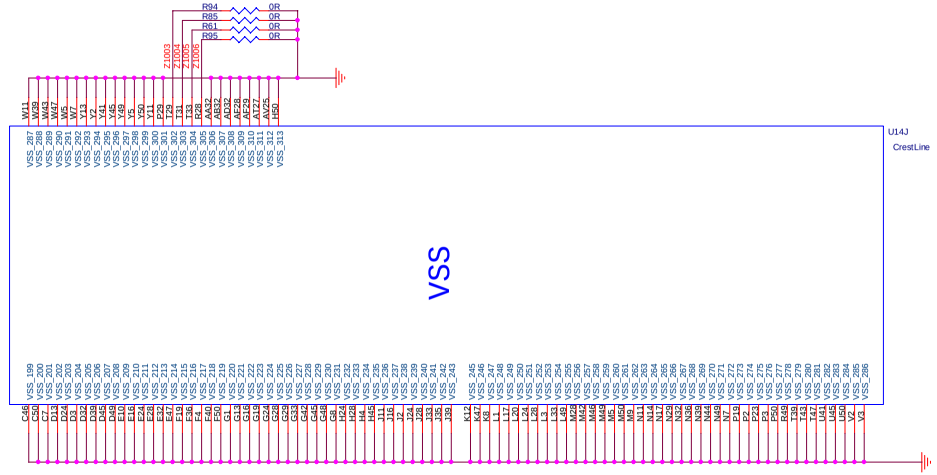
should be tied to GND

should be tied to GND

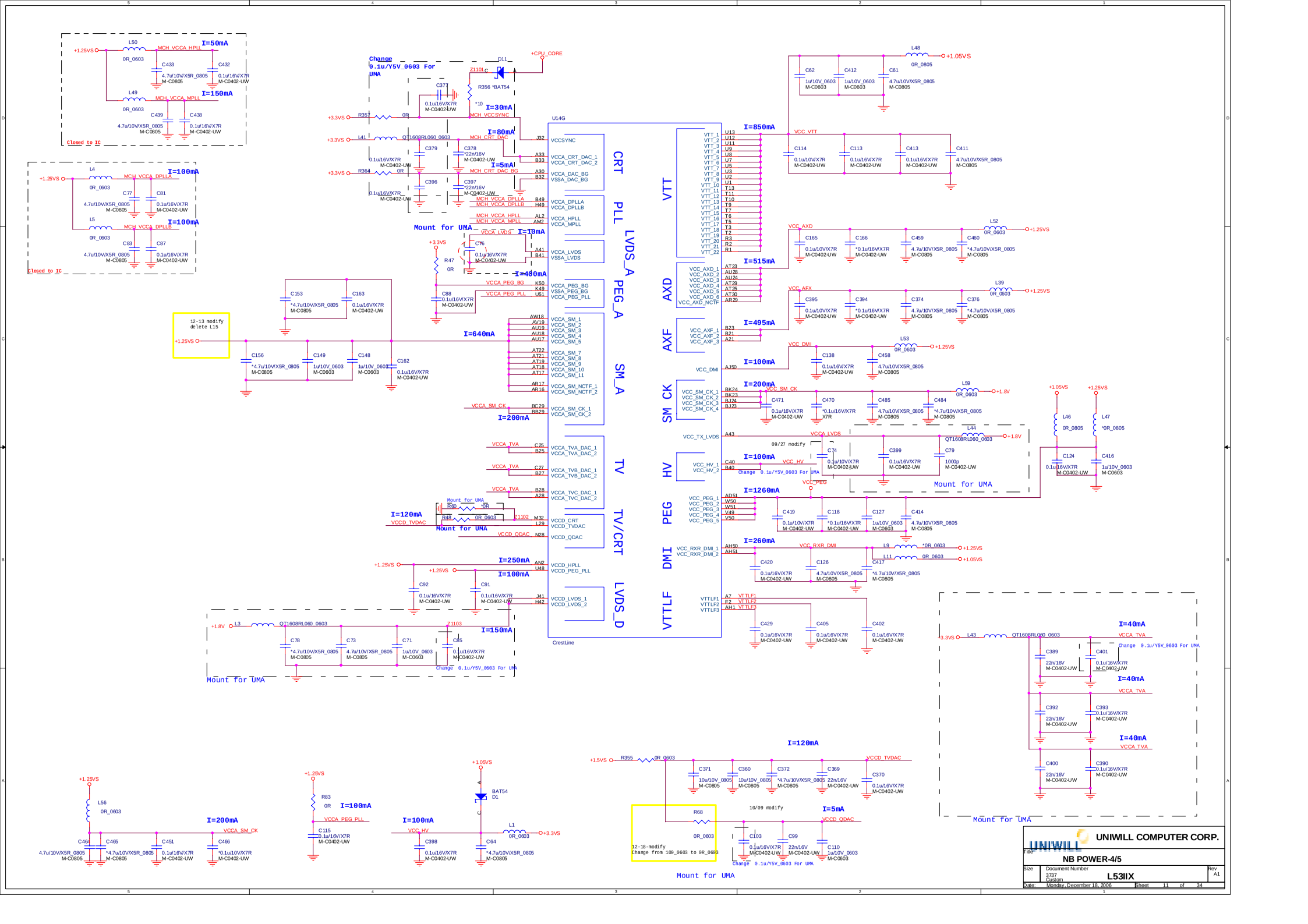
Title	NB NB DDRCLK_VGA_PCIEXPR-2/5
Size	Document Number: 3737 Custom
Rev	A1
Date:	Monday, December 18, 2006
Sheet	9 of 34

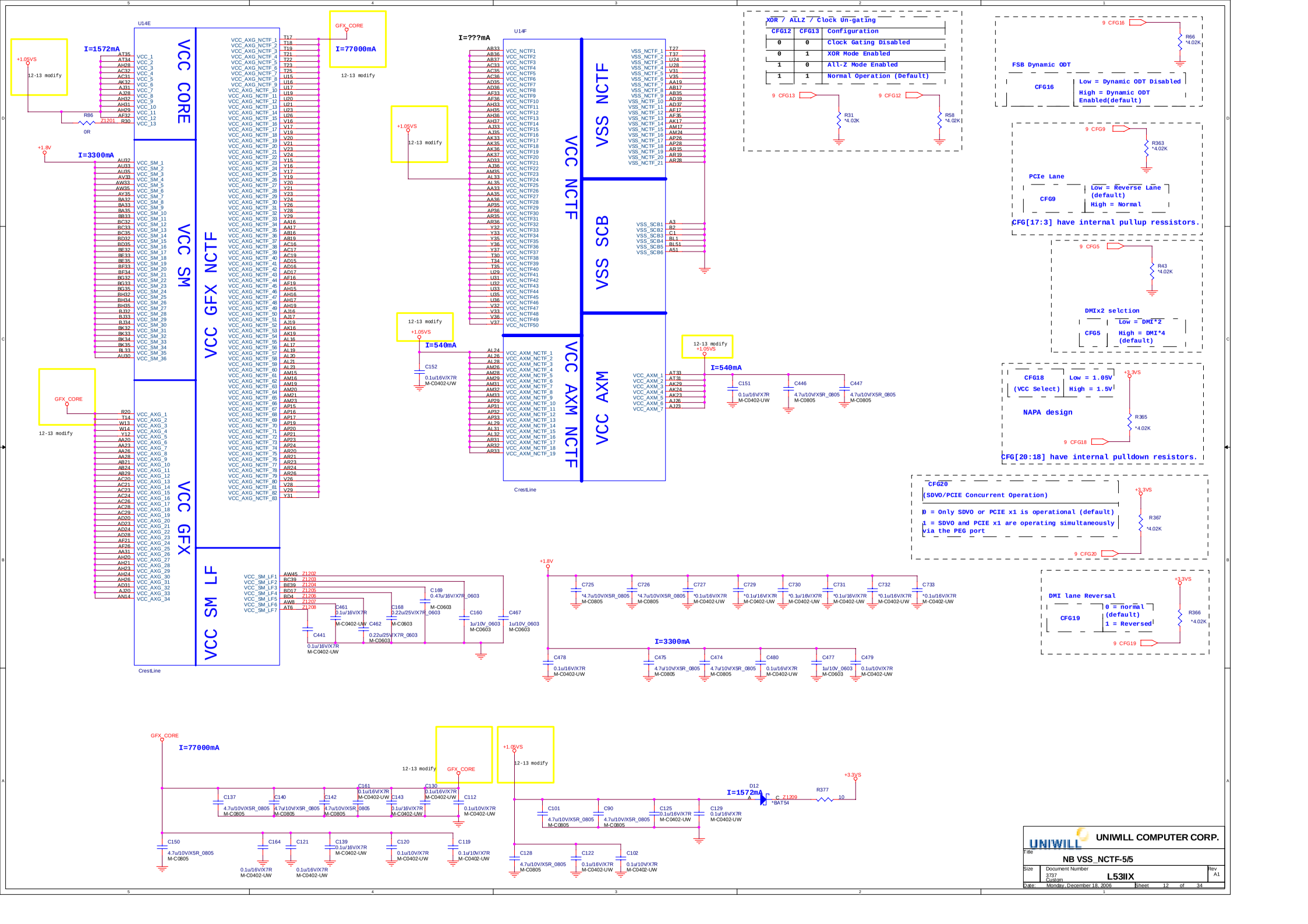
UNIWILL COMPUTER CORP.

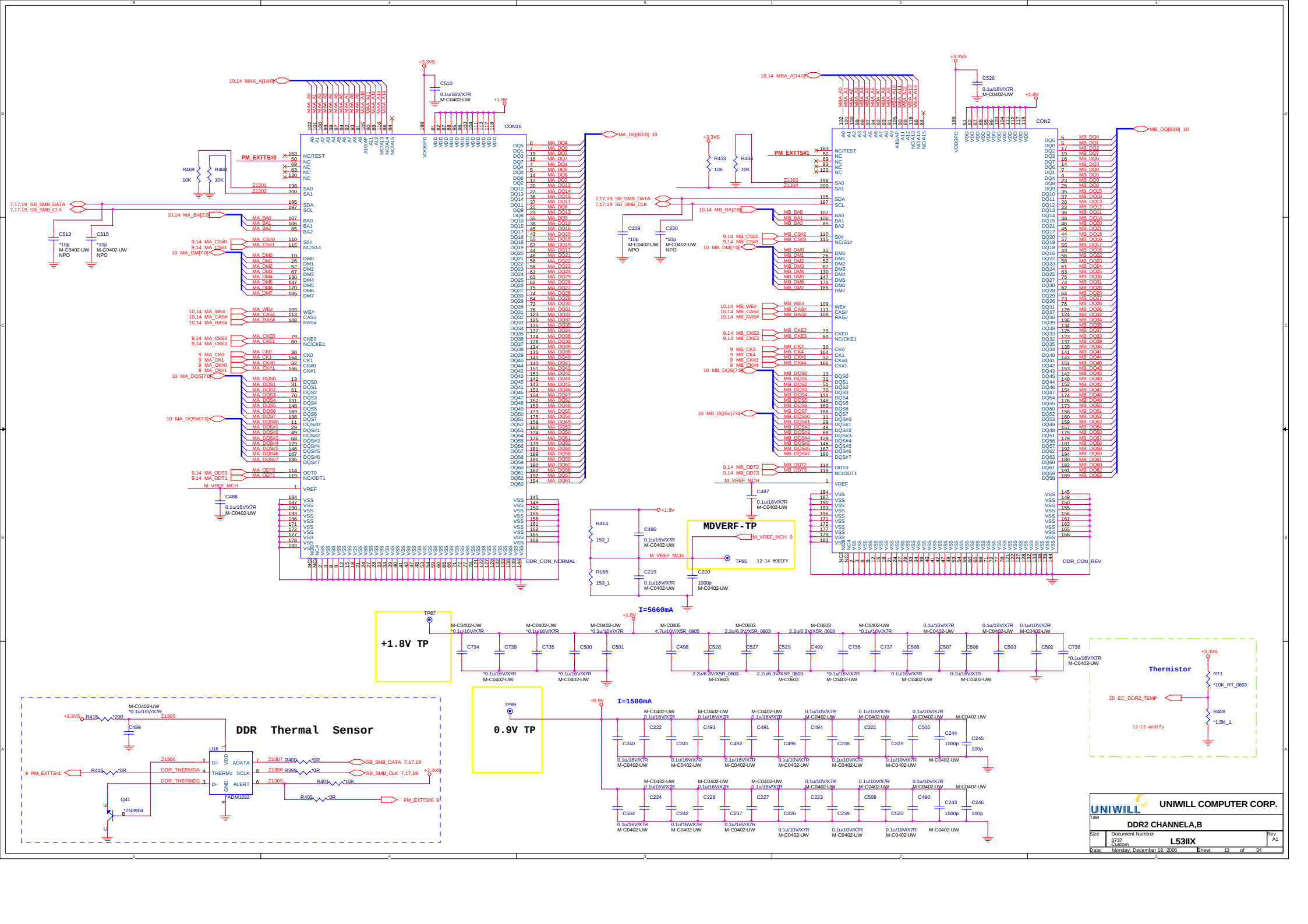




UNIWILL	UNIWILL COMPUTER CORP.		
Title	NB DDR_MEM SYSTEM-3/5		
Size	Document Number 3737 Custom	L53IIX	Rev A1
Date:	Monday, December 18, 2006	Sheet 10 of 34	

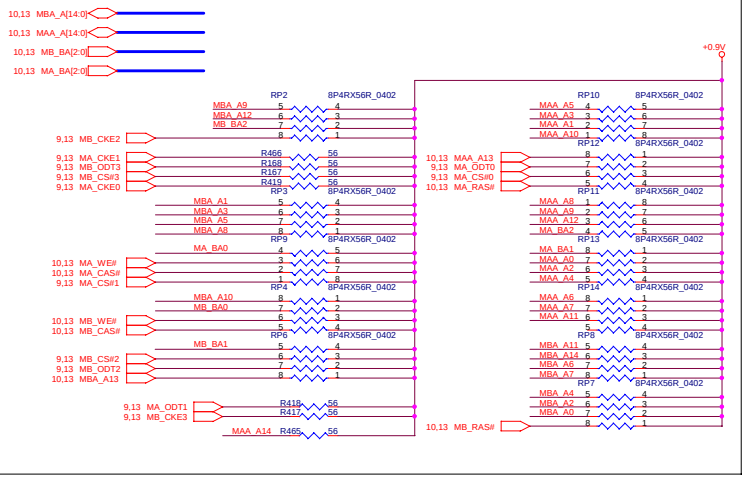

CRT
PLL
LVDS_A
PEG_A
SM_A
TV
TV/CRT
LVDS_D
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
U14G
CrestLine
Mount for UMA
Change 0.1u/Y5V_0603 For UMA
12-13 modify delete L15
12-18-modify Change from 100_0603 to 0R_0603
10/09 modify
09/27 modify
Closed to IC
UNIWILL COMPUTER CORP.
NB POWER-4/5
L53IIX
Monday, December 18, 2006

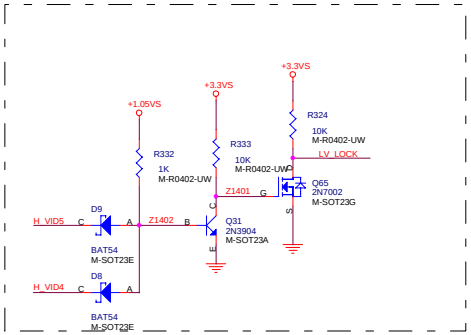

U14E
VCC CORE
VCC SM
VCC GFX NCTF
VCC GFX
VCC SM LF
I=1572mA
+1.05VS
12-13 modify
R86
0R
Z1201
R30
+1.8V
I=3300mA
GFX_CORE
I=77000mA
CrestLine
U14F
I=???mA
VCC NCTF
VSS NCTF
VSS SCB
VCC AXM NCTF
I=540mA
C152
0.1u/16V/X7R
M-C0402-UW
C151
4.7u/10V/X5R_0805
M-C0805
C446
C447
VCC_AXM_1
VCC_AXM_2
VCC_AXM_3
VCC_AXM_4
VCC_AXM_5
VCC_AXM_6
VCC_AXM_7
CFG[17:3] have internal pullup ressistors.
CFG[20:18] have internal pulldown resistors.
XOR / ALLZ / Clock Un-gating
CFG12 | CFG13 | Configuration
0 | 0 | Clock Gating Disabled
0 | 1 | XOR Mode Enabled
1 | 0 | All-Z Mode Enabled
1 | 1 | Normal Operation (Default)
CFG13
CFG12
R31
*1.02K
R58
*1.02K
FSB Dynamic ODT
CFG16
Low = Dynamic ODT Disabled
High = Dynamic ODT Enabled(default)
R66
*4.02K
PCIe Lane
CFG9
Low = Reverse Lane (default)
High = Normal
R363
*4.02K
DMIx2 selction
CFG5
Low = DMI*2
High = DMI*4 (default)
R43
*4.02K
CFG18
(VCC Select)
Low = 1.05V
High = 1.5V
NAPA design
R365
*4.02K
CFG20
(SDVO/PCIE Concurrent Operation)
0 = Only SDVO or PCIE x1 is operational (default)
1 = SDVO and PCIE x1 are operating simultaneously via the PEG port
R367
*4.02K
DMI lane Reversal
CFG19
0 = normal (default)
1 = Reversed
R366
*4.02K
+3.3VS
C725
C726
C727
C729
C730
C731
C732
C733
C478
C475
C474
C480
C477
C479
C137
C140
C142
C143
C112
C161
C130
C150
C164
C121
C139
C120
C119
C101
C90
C125
C129
C128
C122
C102
D12
I=1572mA
C_Z1209
*BAT54
R377
10
UNIWILL COMPUTER CORP.
NB VSS_NCTF-5/5
L53IIX
Monday, December 18, 2006
Sheet 12 of 34

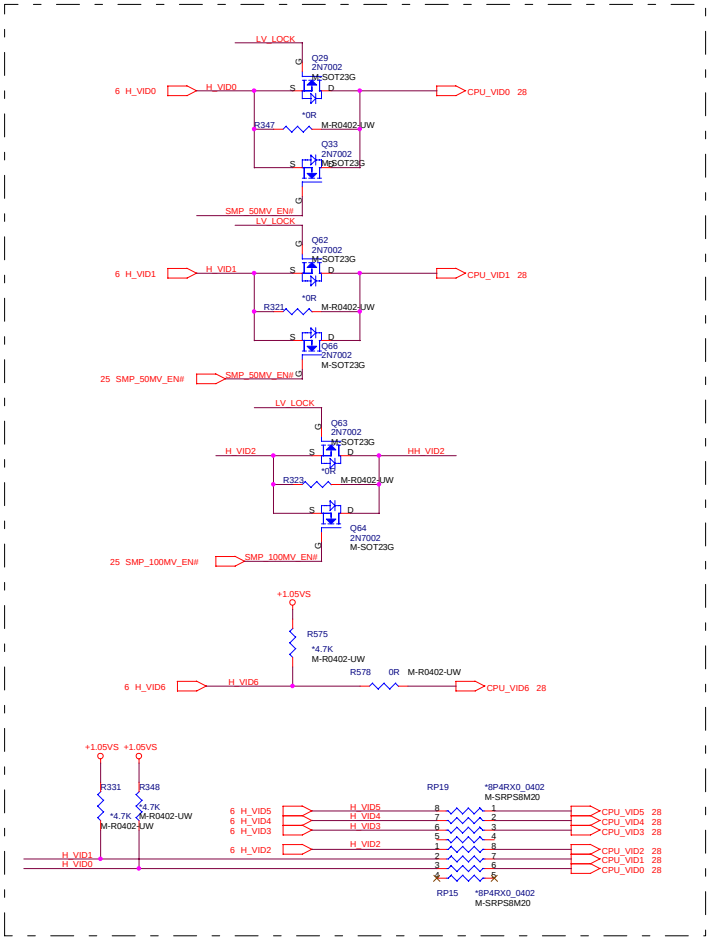

CON16
CON2
DDR_CON_NORMAL
DDR_CON_REV
PM_EXTTS#0
PM_EXTTS#1
MDVERF-TP
I=5660mA
I=1500mA
+1.8V TP
0.9V TP
DDR Thermal Sensor
ADM1032
Thermistor
UNIWILL COMPUTER CORP.
DDR2 CHANNELA,B
L53IIX

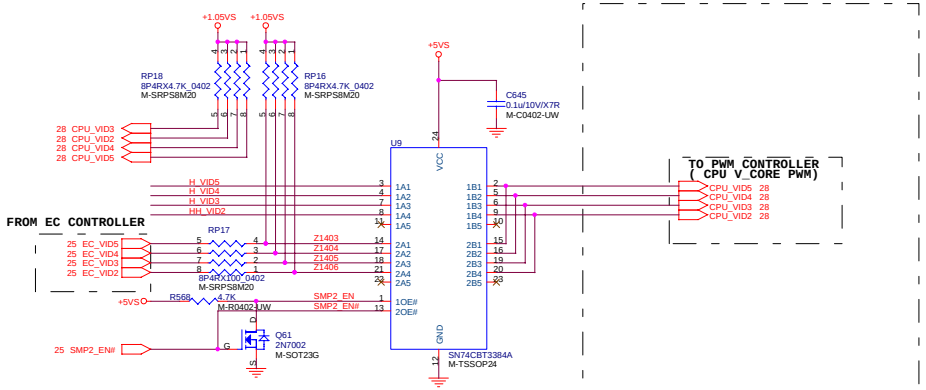
SMART POWER

VID6	VID5	VID4	VID3	VID2	VID1	VID0	VCORE	+_mV
0	0	0	0	0	0	0	1.5000	-0mV
0	0	0	0	0	0	1	1.4875	-2.5mV
0	0	0	0	0	1	0	1.4750	-5mV
0	0	0	0	1	0	0	1.4500	-50mV
0	0	0	1	0	0	0	1.4000	-100mV
0	0	1	0	0	0	0	1.3000	-200mV
0	1	0	0	0	0	0	1.1000	-400mV
1	0	0	0	0	0	0	0.7000	-800mV
0	0	1	1	0	1	1	1.1625	
0	0	1	0	0	0	1		
0	0	1	0	0	1	0		
0	0	1	0	1	0	0		
0	0	1	0	1	1	0		
0	0	1	1	0	0	1		
0	0	1	1	0	1	0		









UNIWILL COMPUTER CORP.

Title: Termination / Smart Power/DC IN

Size	Document Number	Rev
	3737 Custom L53IIX	A1

Date: Monday, December 18, 2006 Sheet 14 of 34

LCD Panel SELECT

LCD_SEL2#	LCD_SEL1#	LCD_SEL0#	
L	L	L	reserved
L	L	H	1024X768
L	H	L	1400X1050
L	H	H	1280X800
H	L	L	reserved
H	L	H	1680X1050
H	H	L	1920X1200
H	H	H	1440X900

LCD

CRT

LCD VCC

WEBCAM

+5VS/+5V/1.5A

	PM_DPRSLPVR
C3	LOW
C4/S1	HIGH
S3/S4/S5	LOW

BLUETOOTH

+5VS/+5V/1.5A

	PM_DPRSLPVR
C3	LOW
C4/S1	HIGH
S3/S4/S5	LOW

INVERTER

S-VIDEO

IR

LAYOUT: Place L31, L32,L33 90 degree from each other.

LAYOUT: Resistor / Caps / Bead close to CRT_CON.

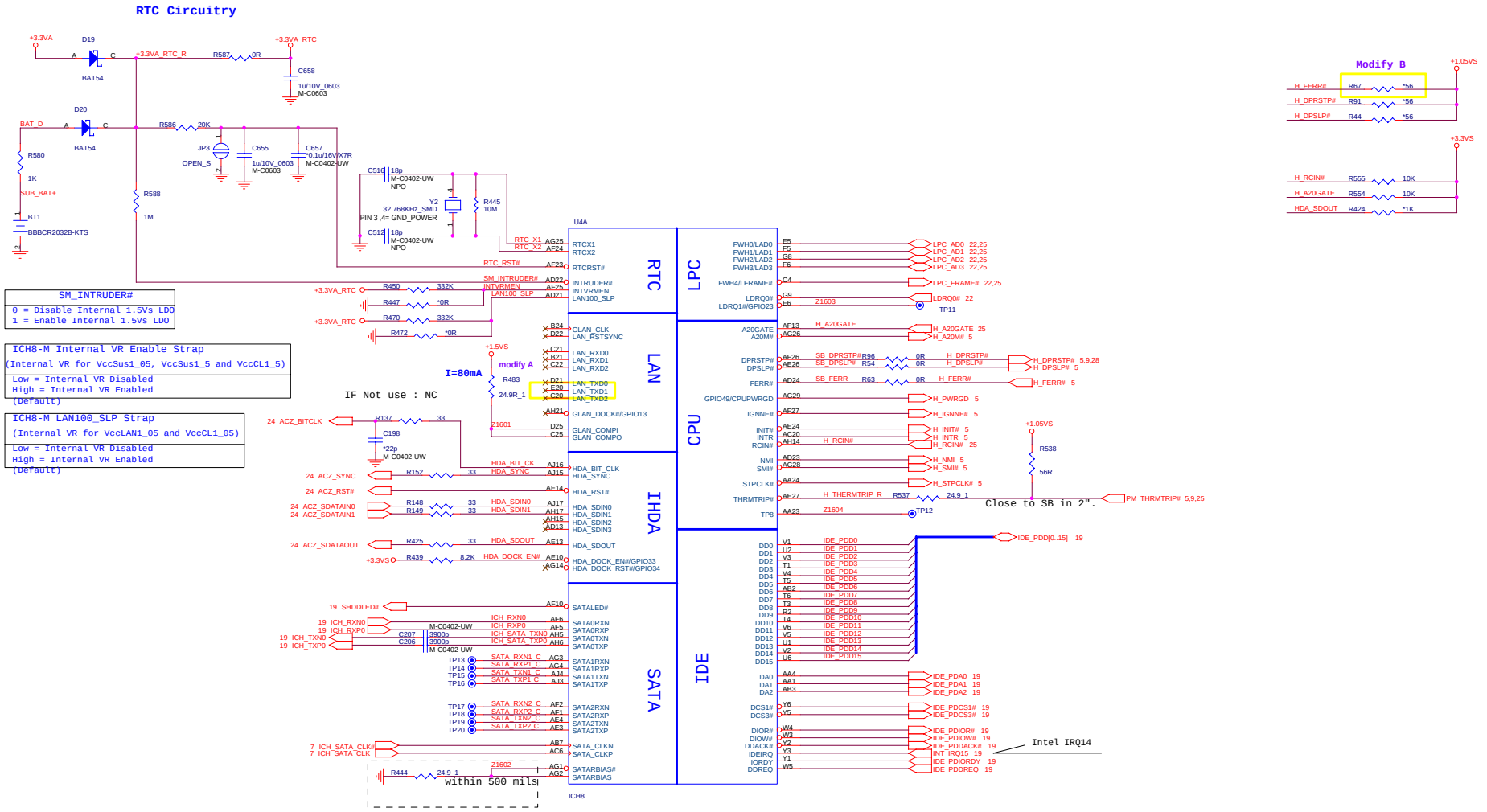
CRT resistor trace impedance between NB and 150 ohm resistor should be 37.5 ohm +/- 15%, Between two 150 ohm resistors should be 50 ohm, Between 150 ohm resistor and connector should be 75 ohm +/- 15%.

TV resistor trace impedance between NB and 75 ohm resistor should be 37.5 ohm +/- 15%, The trace impedance between 75 ohm resistor and connector should be 75 ohm +/- 15%.

0 = Enable
1 = Disable

Title	LCD&S-VDIO&CRT&WEBCAOM&BLUETOOTH
Size	3737 Custom
Document Number	L53IIX
Rev	A1
Date:	Monday, December 18, 2006
Sheet	15 of 34

UNIWILL COMPUTER CORP.



UNIWILL COMPUTER CORP.	
Title	ICH8M CPU/SATA/IDE 1/3
Size	Document Number: 3737 Custom — L53IIX — Rev: A1
Date: Monday, December 18, 2006	Sheet 16 of 34

(3.3V , 1.5V , PCI CLK 99mS)

PCI

ICH8M IO/GPIO/USB/SYS-2/3

Company	UNIWILL COMPUTER CORP.
Size	Document Number: 3737 Custom — L53IIX — Rev A1
Date	Monday, December 18, 2006
Sheet	17 of 34

Sample on PWROK rise edge

PCI_GNT#0	SPI_CS#1	BOOT BIOS LOCATION
0	1	SPI
1	0	PCI
1	1	LPC (DEFAULT)

Strap SPKR 1:Normal
0:No Reboot Mode

PCI_GNT#0 R504 *1K
SPI_CS#1 R489 *1K

PCI_GNT#3 R498 *1K

0 = A16 Swap override enabled
1 = default

As Test Point

Buffer to reduce loading on PLT_RST#

Modify 9/18

PCI-E WAKE UP

10/21 Modify

Resume Power GPIO [8:10] [12:15] [25:28]

For New Card

For Mini Card

For Lan8101E

Modify 9/19

Changed R134 from 100K to * NC * 12-18 modify

INT-PIRQA# : NC
INT-PIRQB# : NC
INT-PIRQC# : NC
INT-PIRQD# : NC

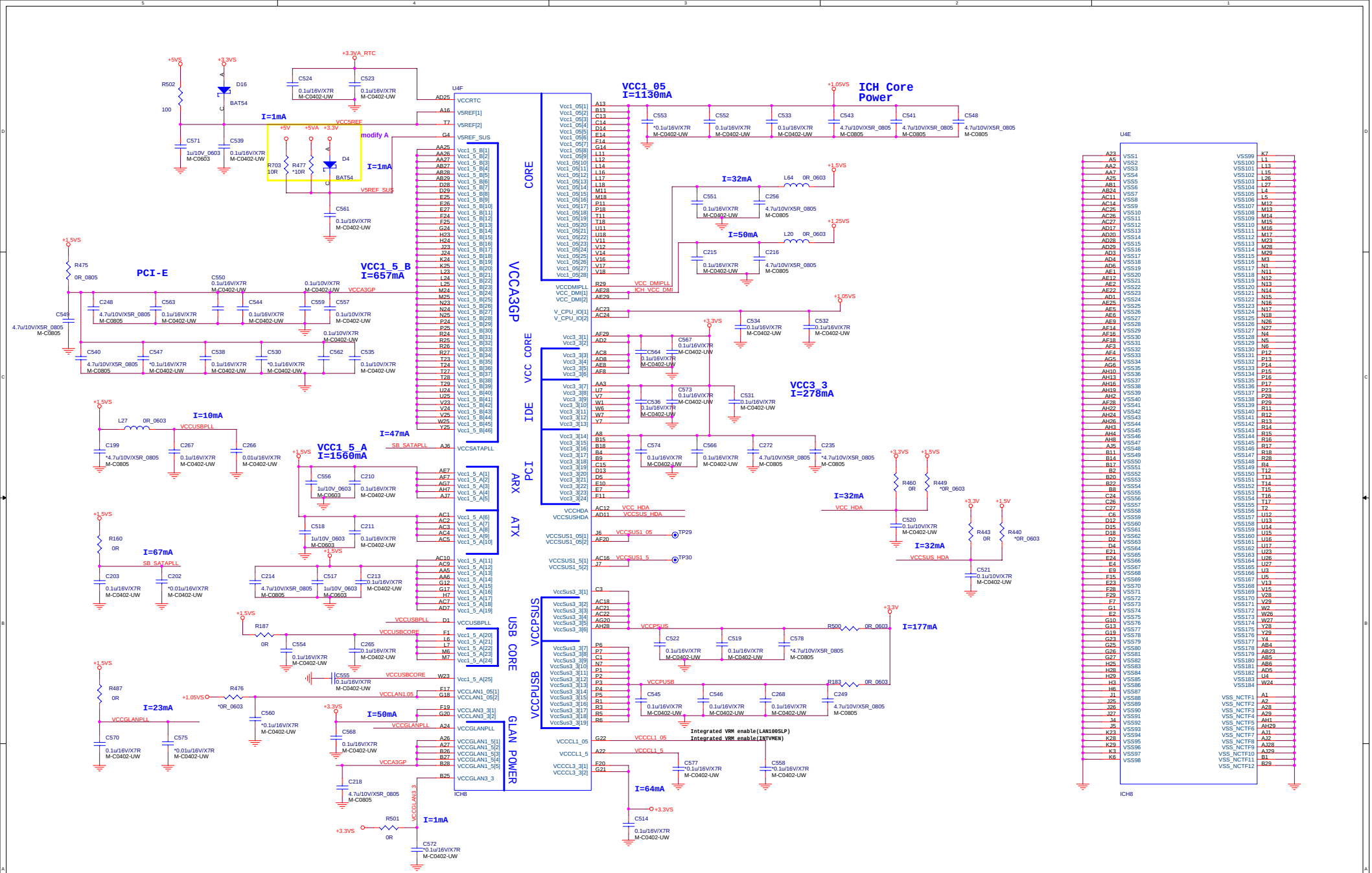
PCI_REQ#0 : NC
PCI_REQ#1 : NC
PCI_REQ#2 : NC
PCI_REQ#3 : NC

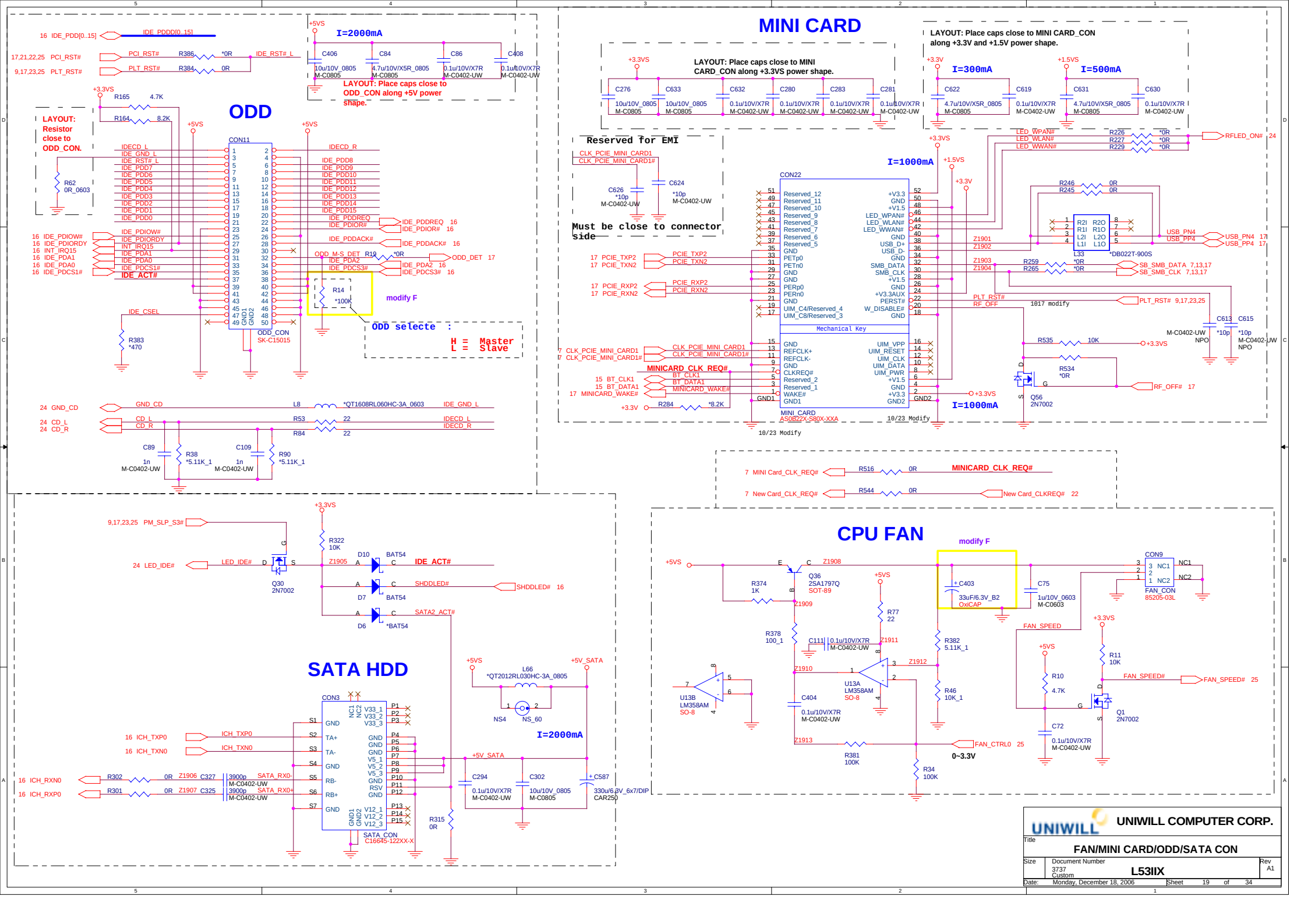
PCI_GNT#0 : NC
PCI_GNT#1 : NC
PCI_GNT#2 : NC
PCI_GNT#3 : NC

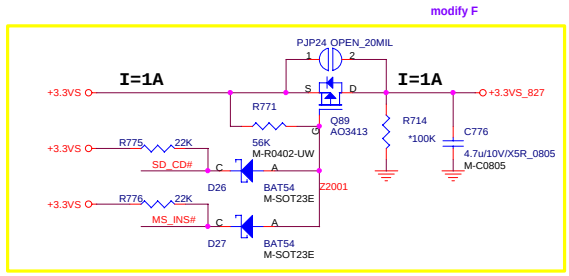
	L53II	L53RI
PCIE 0	NEW CARD	NEW CARD
PCIE 1	miniCARD1	miniCARD1
PCIE 2	No	No
PCIE 3	No	No
PCIE 4	No	No
PCIE 5	No	No
PCIE 6	No	No

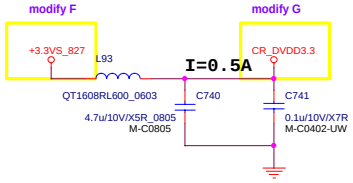
	L53II	L53RI
USB0	on board CON20	
USB1	NEW CARD	
USB2	MINI CARD1	
USB3	3G MODULE ext board CON19	
USB4		
USB5	BLUETOOTH ext board CON19	
USB6		
USB7	WEBCAM_CON	
USB8	GL827 Cardread	
USB9		

Close to SB (D<500mil)

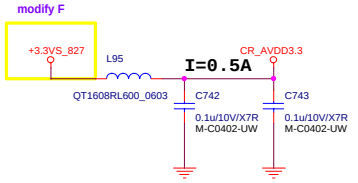

VCC1_05
I=1130mA
ICH Core Power
VCC3_3
I=278mA
VCC1_5_B
I=657mA
PCI-E
VCCA3GP
VCC1_5_A
I=1560mA
I=10mA
I=47mA
I=67mA
I=23mA
I=1mA
I=50mA
I=32mA
I=177mA
I=64mA
CORE
VCC CORE
IDE
ICH
ARX
ATX
USB CORE
VCCPSUS
VCCPUSB
GLAN POWER
Integrated VRM enable(LAN100SLP)
Integrated VRM enable(INTVMEN)
ICH8
UNIWILL COMPUTER CORP.
ICH8M Power -3/3
L53IIX
Monday, December 18, 2006


ODD
MINI CARD
SATA HDD
CPU FAN
I=2000mA
I=300mA
I=500mA
I=1000mA
LAYOUT: Place caps close to ODD_CON along +5V power shape.
LAYOUT: Place caps close to MINI CARD_CON along +3.3VS power shape.
LAYOUT: Place caps close to MINI CARD_CON along +3.3V and +1.5V power shape.
LAYOUT: Resistor close to ODD_CON.
Reserved for EMI
Must be close to connector side
ODD selecte : H = Master L = Slave
modify F
10/23 Modify
1017 modify
UNIWILL COMPUTER CORP.
FAN/MINI CARD/ODD/SATA CON
L53IIX
Monday, December 18, 2006
Sheet 19 of 34



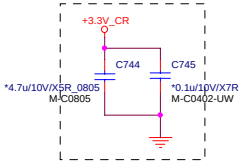


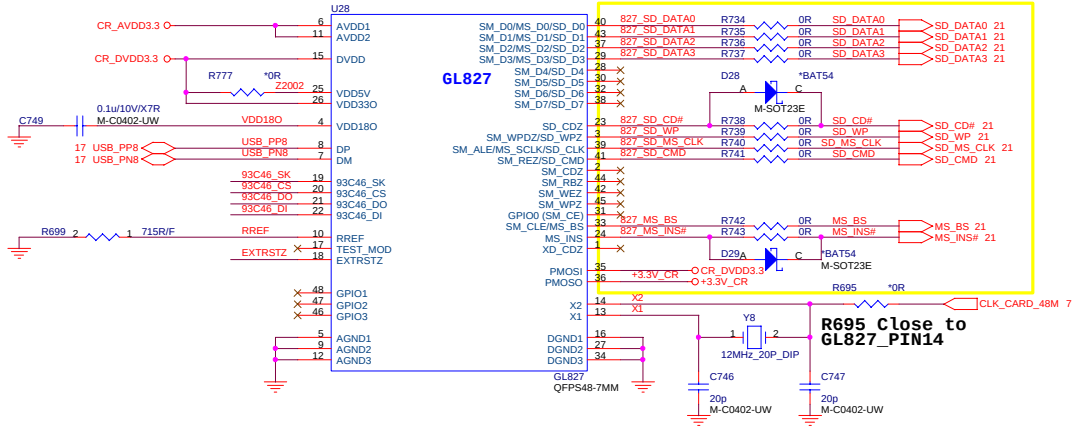
Close to GL827_PIN25
(Regulator 5V input)



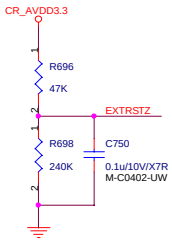
Close to GL827_PIN26
(Regulator 3.3V
output)

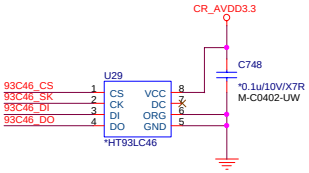
Close to card reader connector

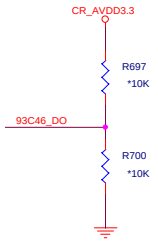




R695 Close to
GL827_PIN14







Source clock selection

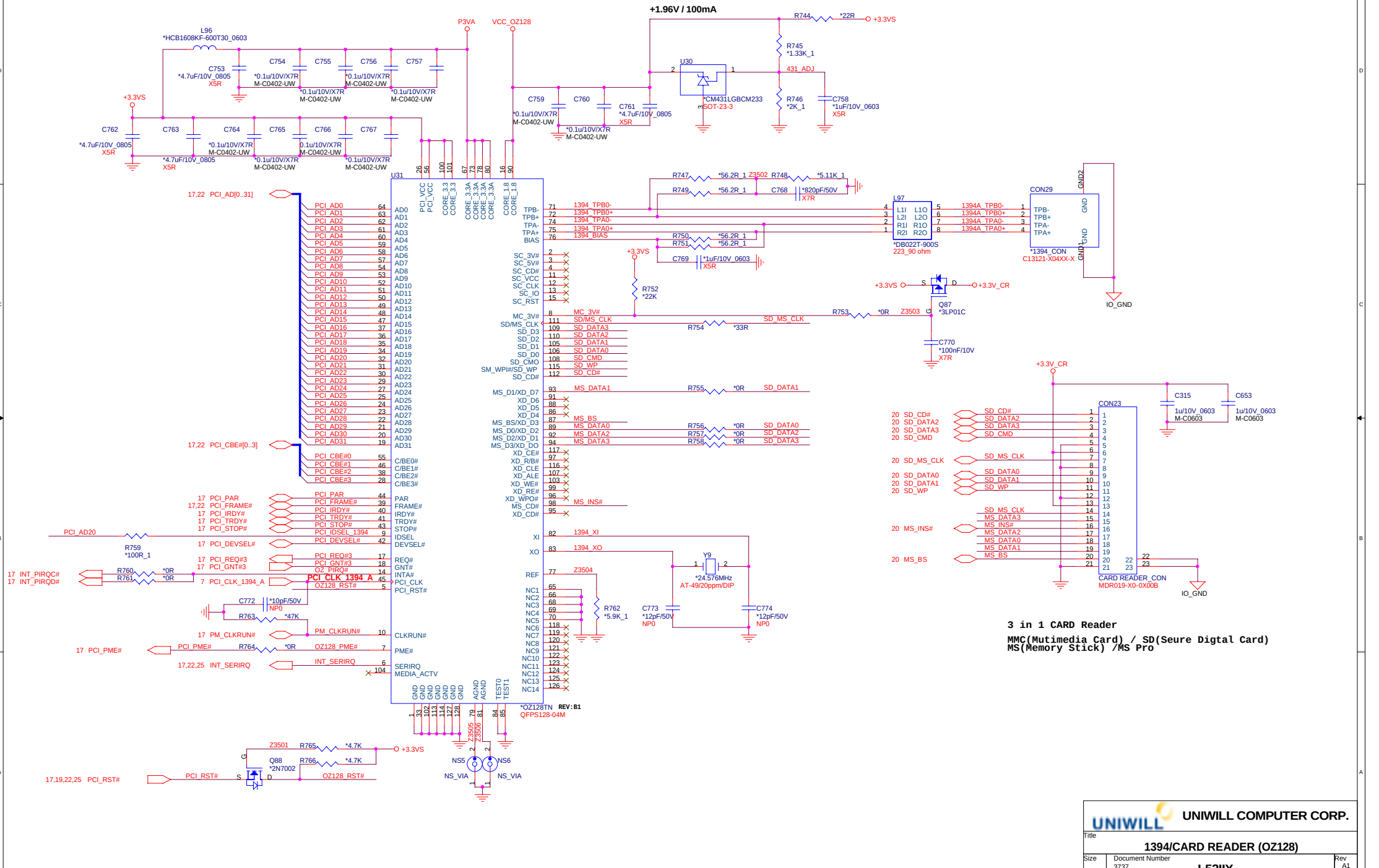
Freq.	R697	R700
12MHz	NC	NC
12MHz	NC	10K
48MHz	10K	NC

UNIWILL COMPUTER CORP.

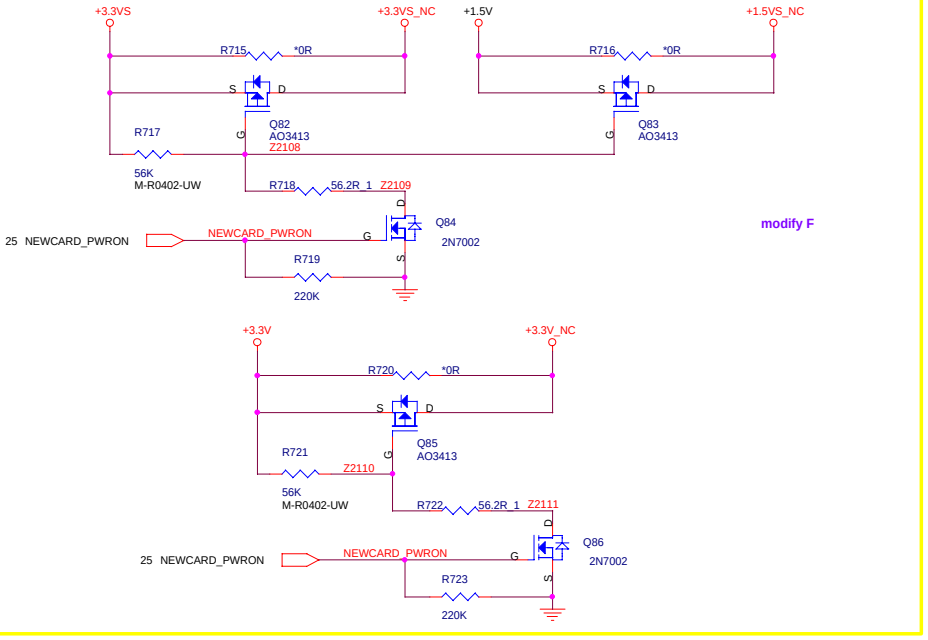
Title: GL827/CARD READER

Size: Custom | Document Number: 3737 L53IIX | Rev: A1

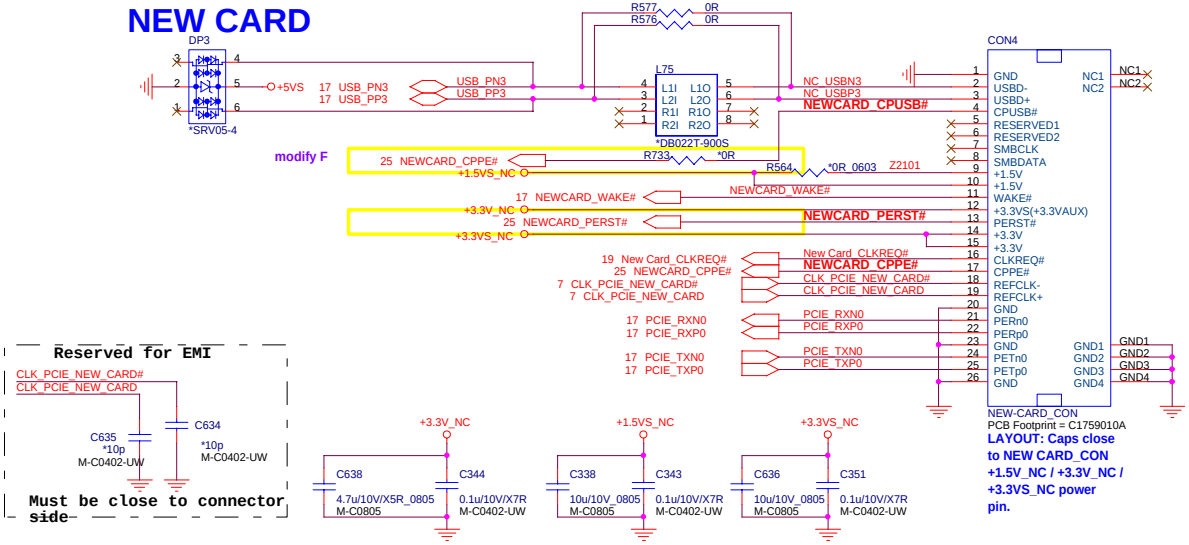
Date: Monday, December 18, 2006 | Sheet 20 of 34


+1.96V / 100mA
U31
*OZ128TN REV:B1
QFPS128-04M
3 in 1 CARD Reader
MMC(Mutimedia Card) / SD(Seure Digtal Card)
MS(Memory Stick) /MS Pro
UNIWILL COMPUTER CORP.
1394/CARD READER (OZ128)
L53IIX
Monday, December 18, 2006

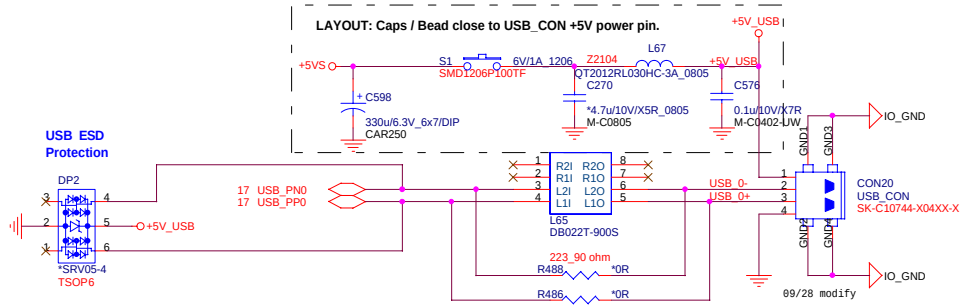
NEW CARD POWER



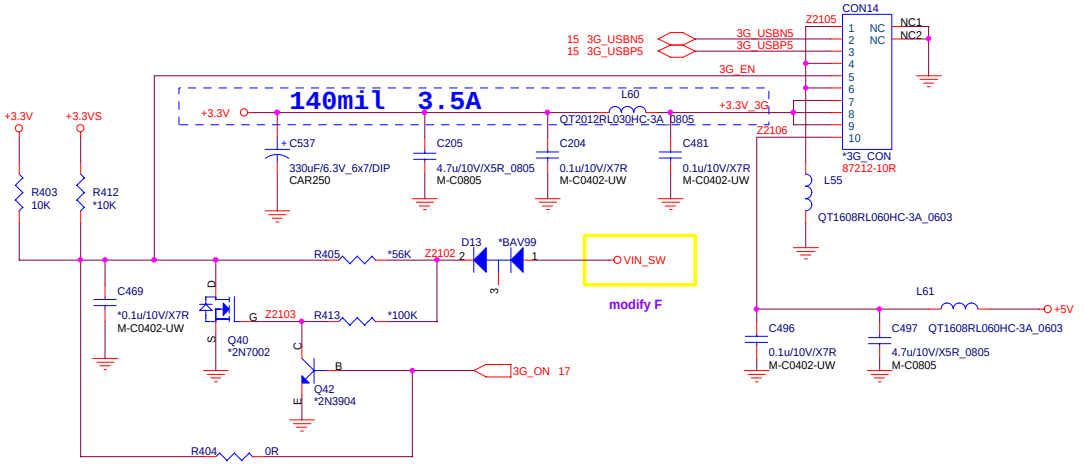
NEW CARD



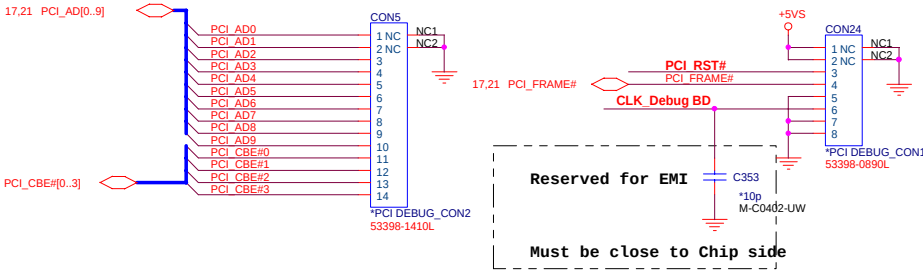
ON BOARD USB



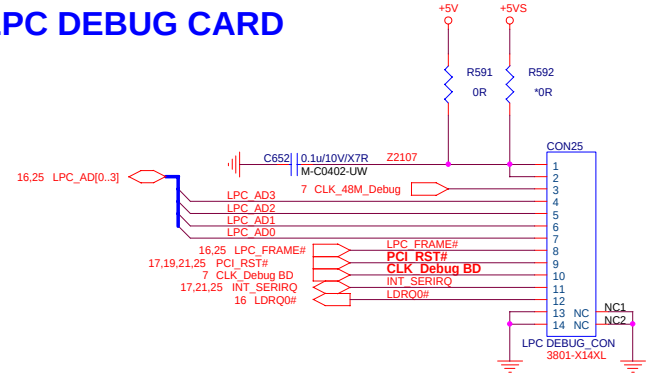
3G USB



PCI DEBUG CARD



LPC DEBUG CARD

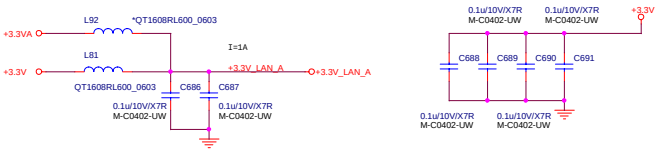


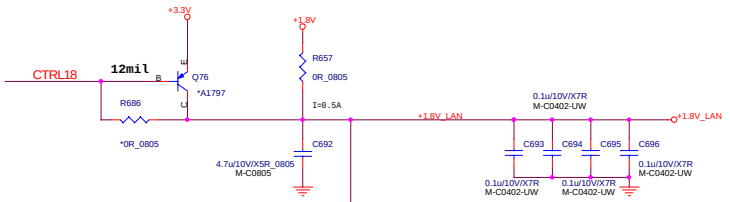
UNIWILL COMPUTER CORP.

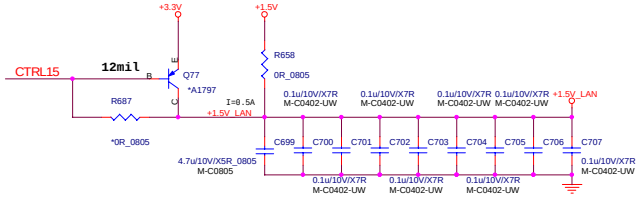
Title: 3G/DEBUG/NEW CARD/USB CON

Size	Document Number	Rev
	3737 Custom L53IIX	A1

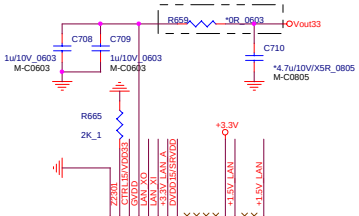
Date: Monday, December 18, 2006 Sheet 22 of 34





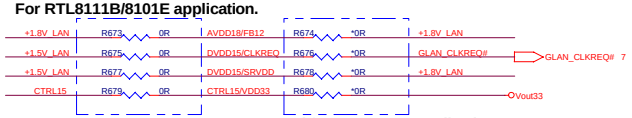


R659 is only used for RTL8111C application.
For RTL8111B/8101E remove R659.

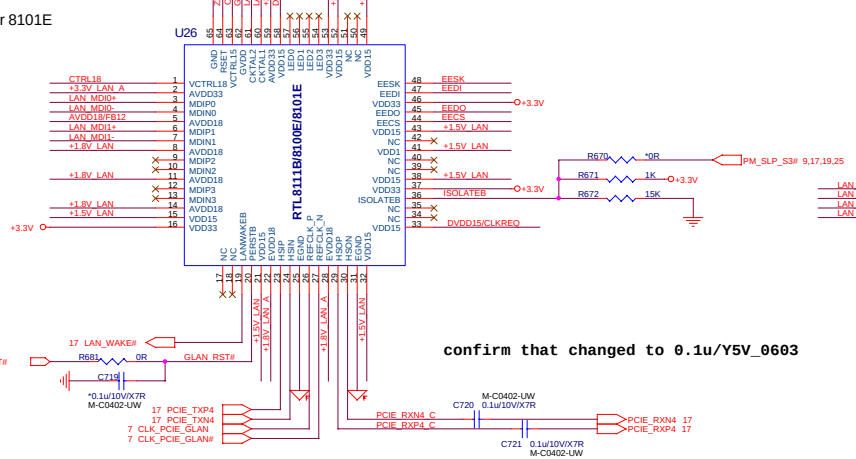


R665 value should be 2.49K (1%) for 8111B/8111C application
R665 should be 2.0K(1%) for 8101E application

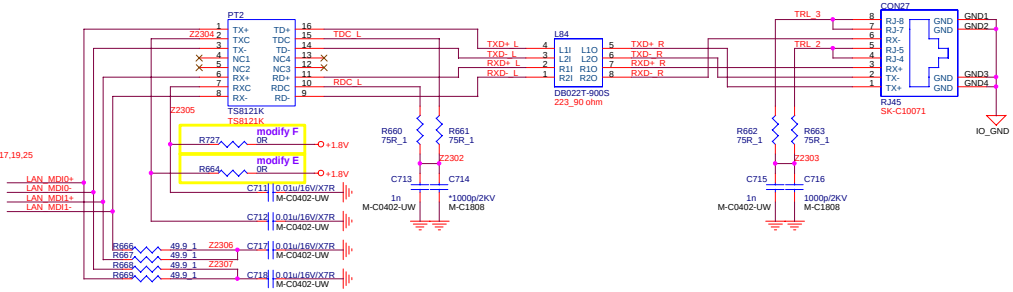
For RTL8111B/8101E application.

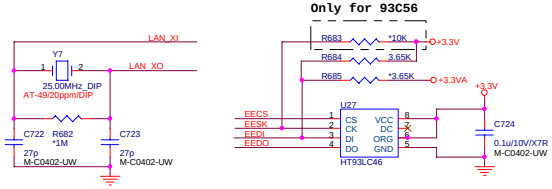


Reserved for RTL8111C application.



confirm that changed to 0.1u/Y5V_0603



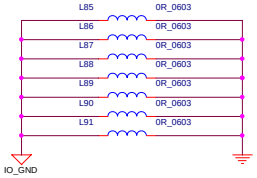


Only for 93C56

Power domain chart

	RTL8111B / RTL8101E	RTL8111C
AVDD33	3.3V	3.3V
AVDD18	1.8V	1.2V
EVDD18	1.8V	1.2V
DVDD15	1.5V	1.2V

	Q76	Q77
RTL8111B	Need	Need
RTL8111C	N/A	N/A
RTL8101E	N/A	N/A



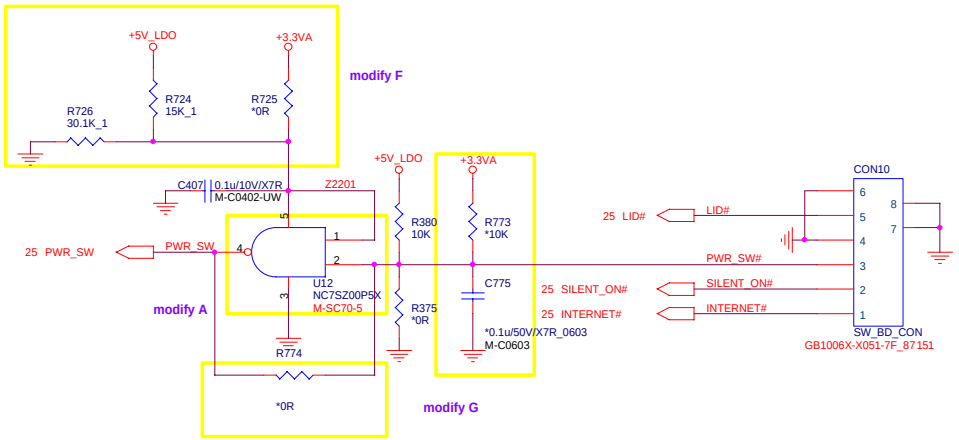
UNIWILL COMPUTER CORP.

Title: LAN-RTL8101

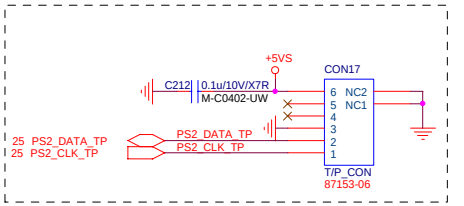
Size	Document Number	Rev
	3737 Custom L53IIX	A1

Date: Monday, December 18, 2006 Sheet 23 of 34

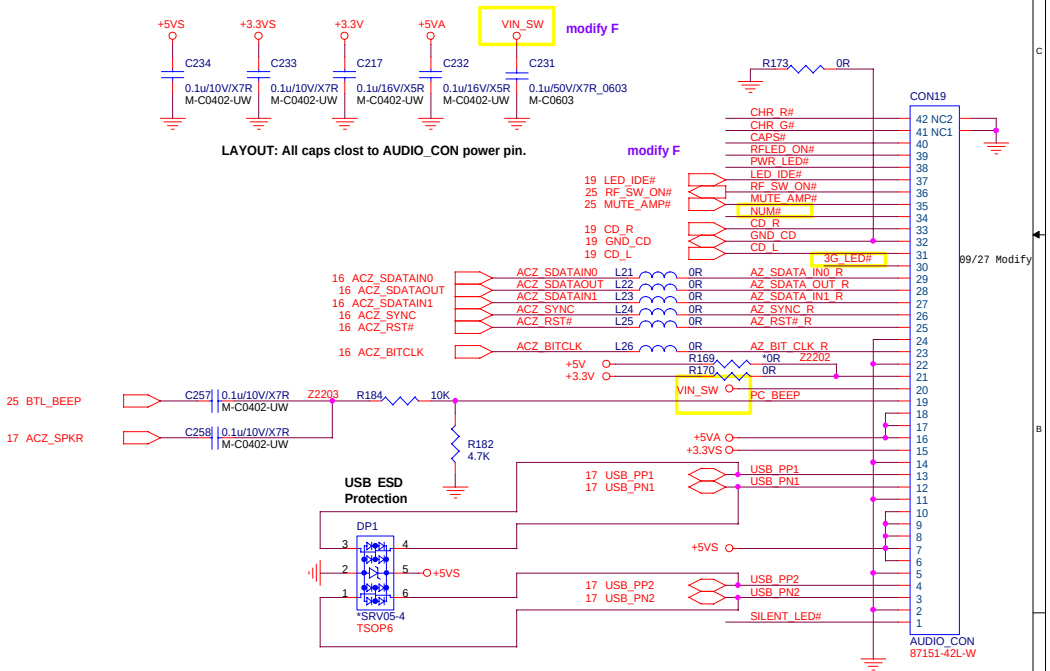
SWITCH BD CON



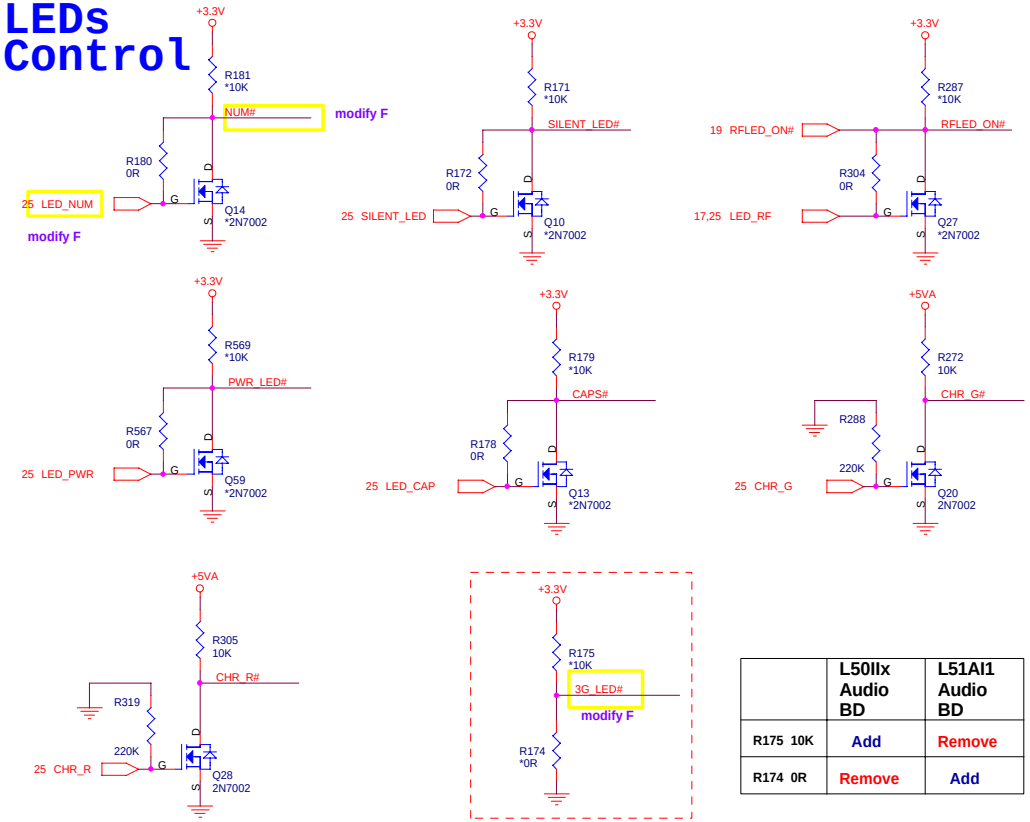
TOUCH PAD CON



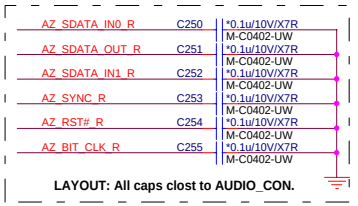
AUDIO / LED BD CON



LEDs Control



	L50IIx Audio BD	L51AI1 Audio BD
R175 10K	Add	Remove
R174 0R	Remove	Add

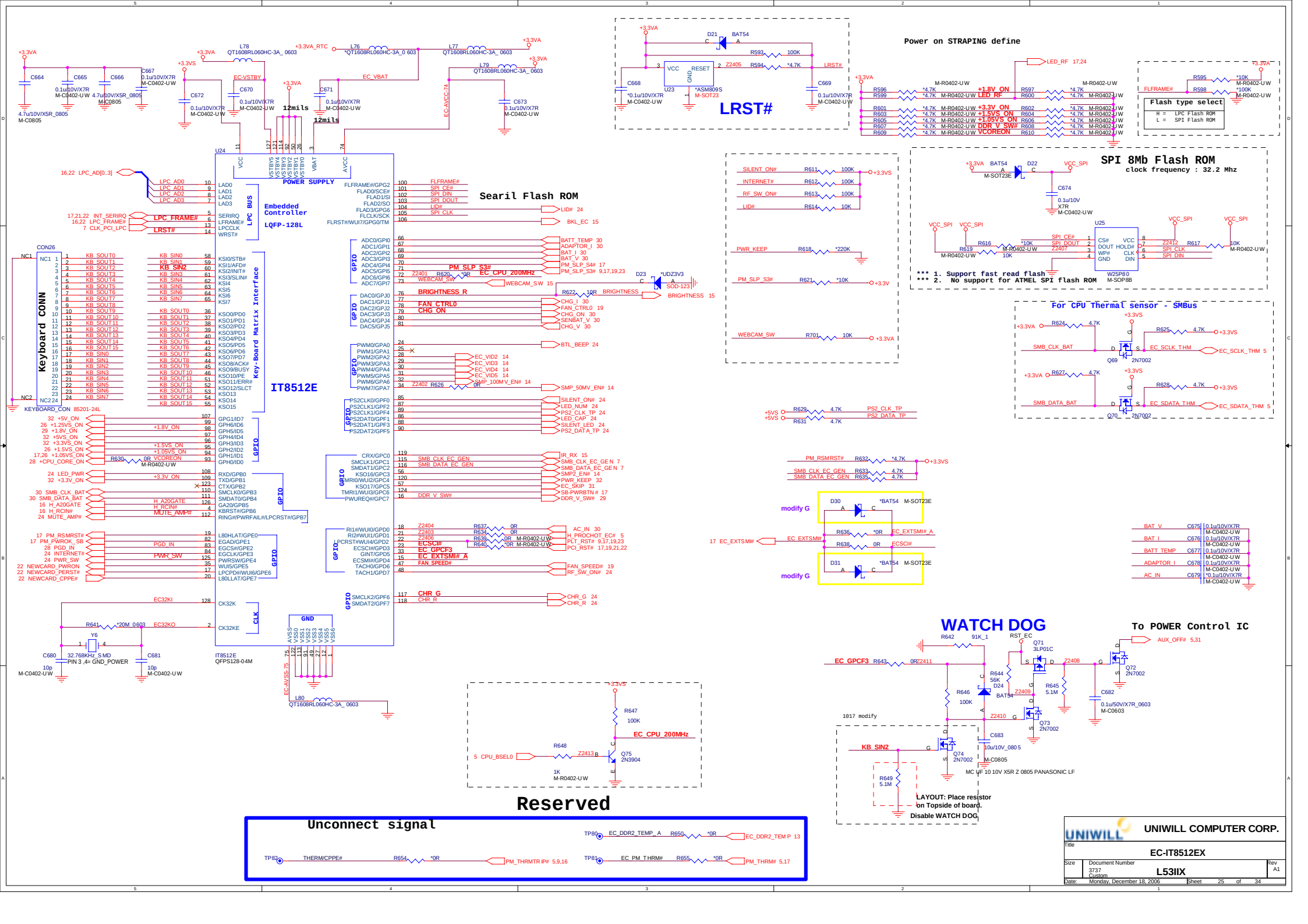


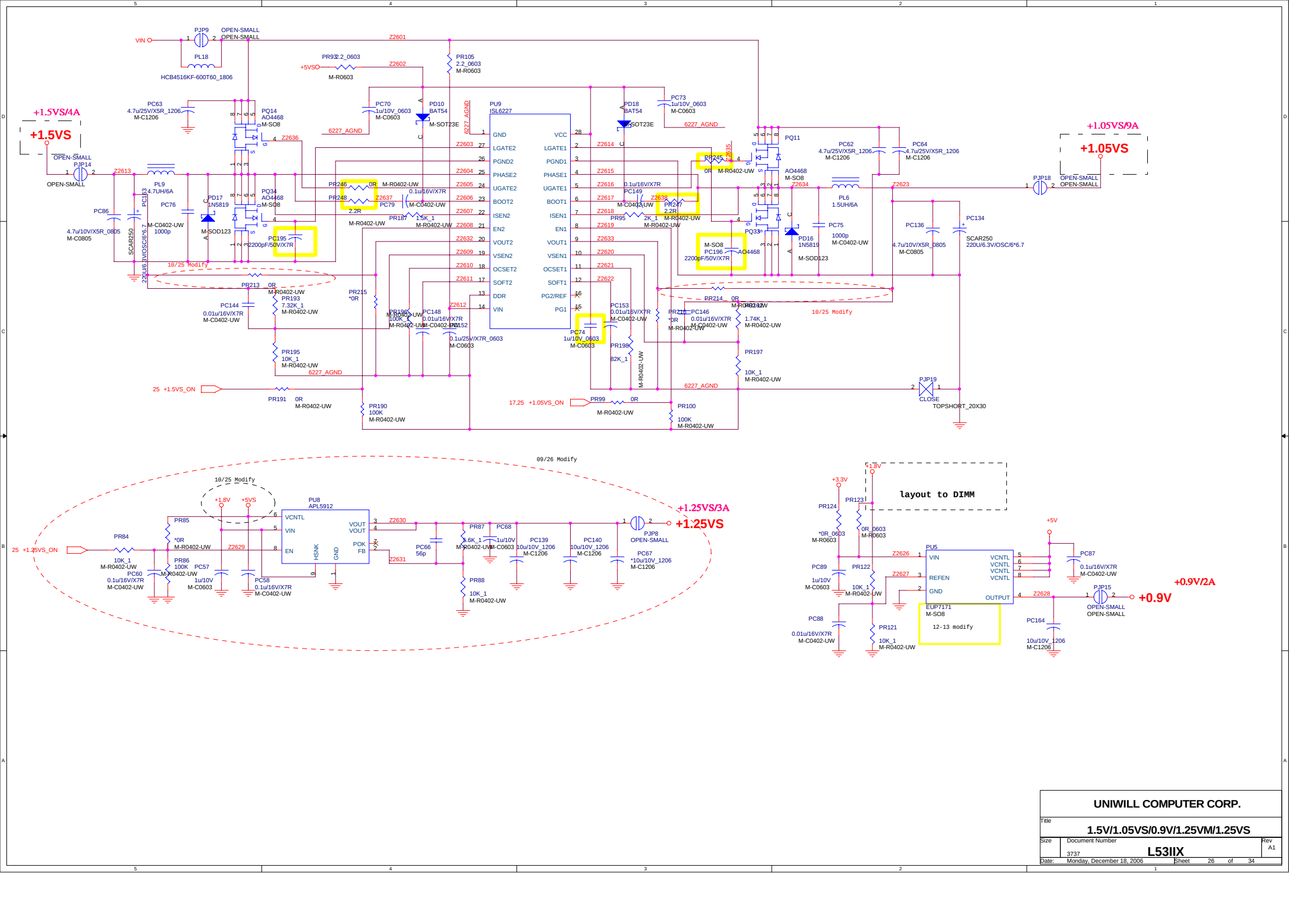
UNIWILL COMPUTER CORP.

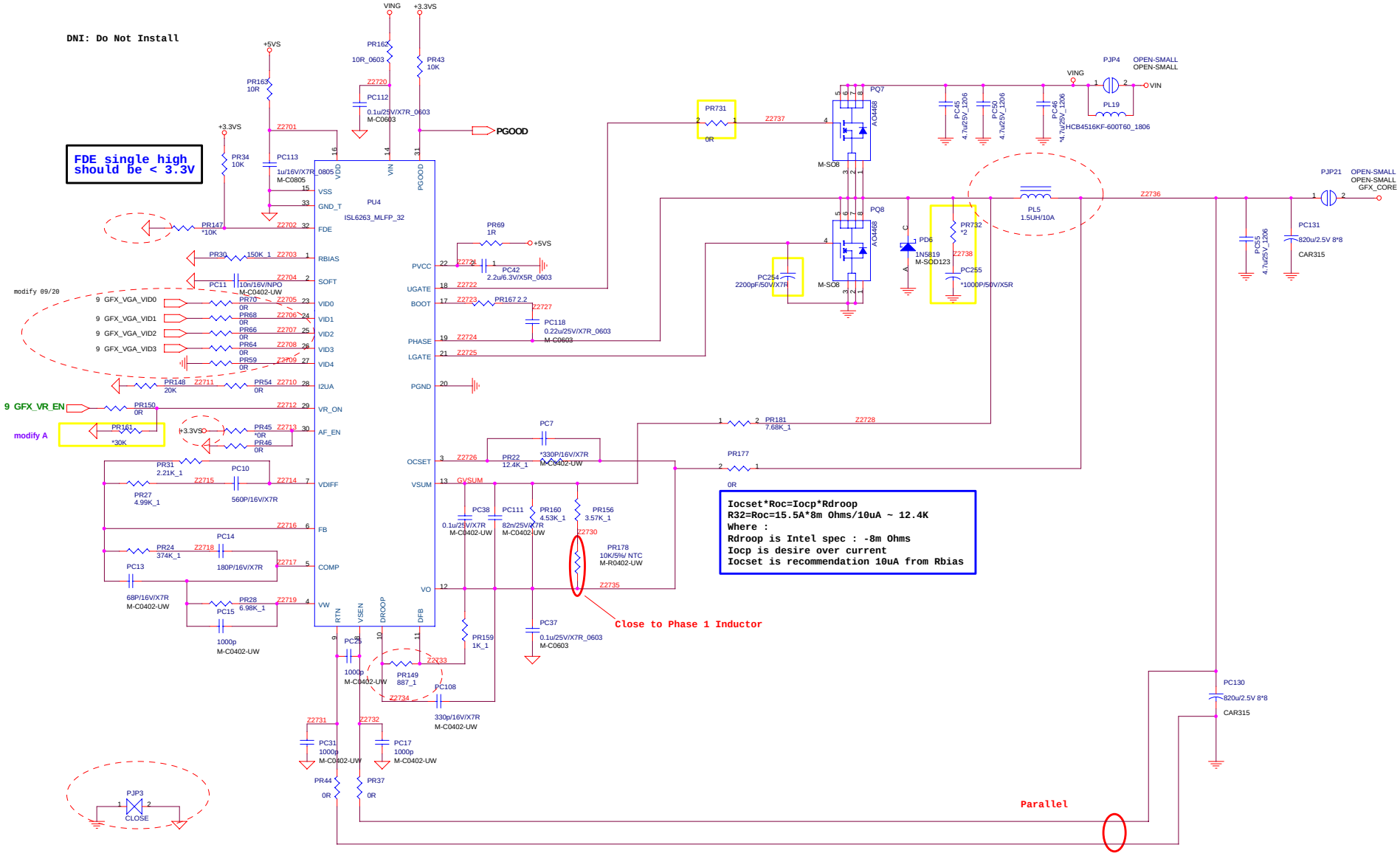
Title: AUDIO/LED/SW BD/TP CON/BIOS

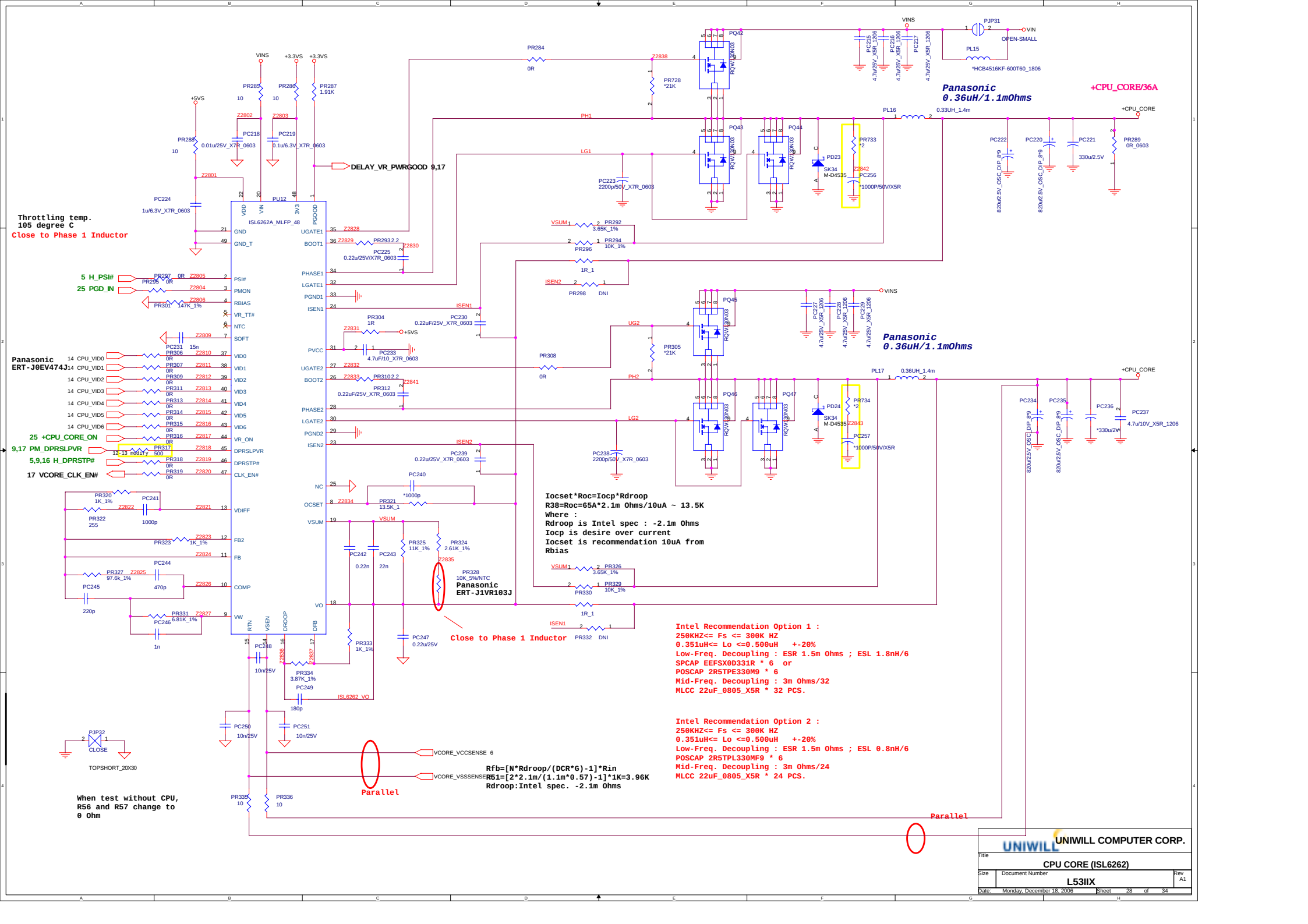
Size	Document Number	Rev
3737 Custom	L53IIX	A1

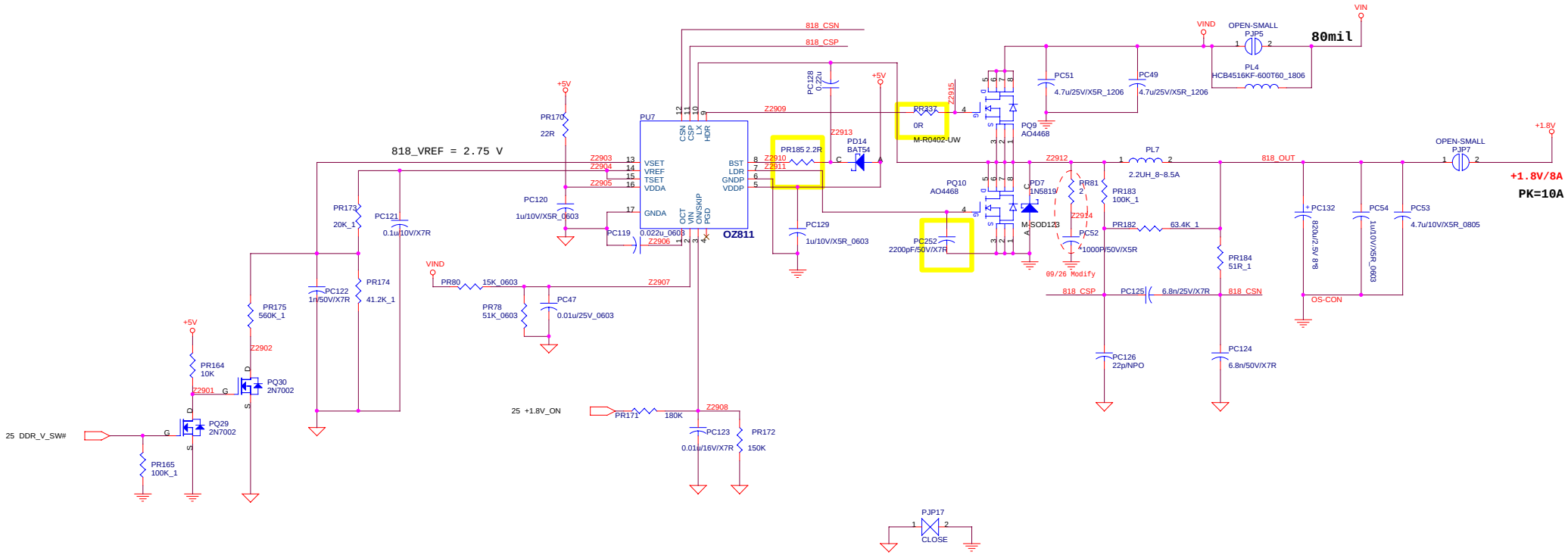
Date: Monday, December 18, 2006 Sheet 24 of 34


Power on STRAPING define
LRST#
Flash type select
H = LPC Flash ROM
L = SPI Flash ROM
SPI 8Mb Flash ROM
clock frequency : 32.2 Mhz
*** 1. Support fast read flash
*** 2. No support for ATMEL SPI flash ROM
For CPU Thermal sensor - SMBus
Searil Flash ROM
Embedded Controller
LQFP-128L
IT8512E
POWER SUPPLY
LPC BUS
Keyboard CONN
Key-Board Matrix Interface
GPIO
CLK
WATCH DOG
To POWER Control IC
1017 modify
LAYOUT: Place resistor on Topside of board.
Disable WATCH DOG
Reserved
Unconnect signal
UNIWILL COMPUTER CORP.
EC-IT8512EX
L53IIX

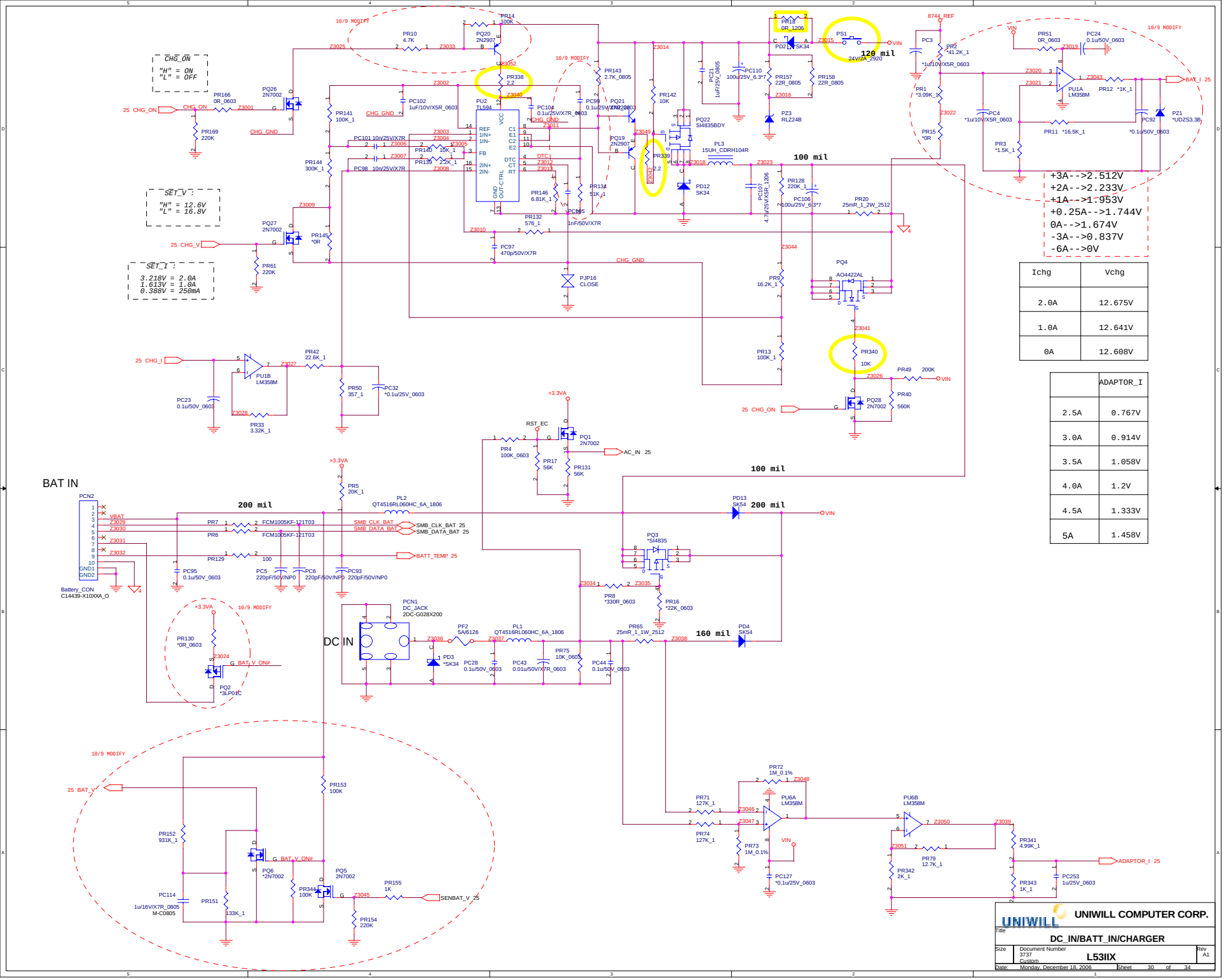

+1.5VS/4A
+1.5VS
+1.05VS/9A
+1.05VS
+1.25VS/3A
+1.25VS
+0.9V/2A
+0.9V
VIN
+5VS
PU9 ISL6227
PU8 APL5912
PU5 EUP7171
PQ11
PQ14 AO4468
PQ34 AO4468
PQ33 AO4468
PD10 BAT54
PD18 BAT54
PD17 1N5819
PD16 1N5819
PJP9
PJP14
PJP18
PJP19
PJP8
PJP15
PL18 HCB4516KF-600T60_1806
PL9 4.7UH/6A
PL6 1.5UH/6A
6227_AGND
09/26 Modify
10/25 Modify
12-13 modify
layout to DIMM
UNIWILL COMPUTER CORP.
1.5V/1.05VS/0.9V/1.25VM/1.25VS
L53IIX
3737
Monday, December 18, 2006
Sheet 26 of 34


DNI: Do Not Install
FDE single high should be < 3.3V
modify 09/20
modify A
9 GFX_VR_EN
Iocset*Roc=Iocp*Rdroop
R32=Roc=15.5A*8m Ohms/10uA ~ 12.4K
Where :
Rdroop is Intel spec : -8m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from Rbias
Close to Phase 1 Inductor
Parallel
PGOOD
ISL6263_MLFP_32
PU4
HCB4516KF-600T60_1806
AO4468
1N5819
M-SOD123
CAR315
UNIWILL COMPUTER CORP.
GFX CORE
L53IIX
Monday, December 18, 2006


Throttling temp.
105 degree C
Close to Phase 1 Inductor
ISL6262A_MLFP_48
Panasonic
0.36uH/1.1mOhms
+CPU_CORE/36A
Panasonic
ERT-J0EV474J
Panasonic
ERT-J1VR103J
Iocset*Roc=Iocp*Rdroop
R38=Roc=65A*2.1m Ohms/10uA ~ 13.5K
Where :
Rdroop is Intel spec : -2.1m Ohms
Iocp is desire over current
Iocset is recommendation 10uA from
Rbias
Intel Recommendation Option 1 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
SPCAP EEFSX0D331R * 6 or
POSCAP 2R5TPE330M9 * 6
Mid-Freq. Decoupling : 3m Ohms/32
MLCC 22uF_0805_X5R * 32 PCS.
Intel Recommendation Option 2 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
POSCAP 2R5TPL330MF9 * 6
Mid-Freq. Decoupling : 3m Ohms/24
MLCC 22uF_0805_X5R * 24 PCS.
Rfb=[N*Rdroop/(DCR*G)-1]*Rin
R51=[2*2.1m/(1.1m*0.57)-1]*1K=3.96K
Rdroop:Intel spec. -2.1m Ohms
When test without CPU,
R56 and R57 change to
0 Ohm
Close to Phase 1 Inductor
Parallel
Parallel
DELAY_VR_PWRGOOD 9,17
5 H_PSI#
25 PGD_IN
25 +CPU_CORE_ON
9,17 PM_DPRSLPVR
5,9,16 H_DPRSTP#
17 VCORE_CLK_EN#
VCORE_VCCSENSE 6
VCORE_VSSSENSE 6
UNIWILL COMPUTER CORP.
CPU CORE (ISL6262)
L53IIX
Monday, December 18, 2006



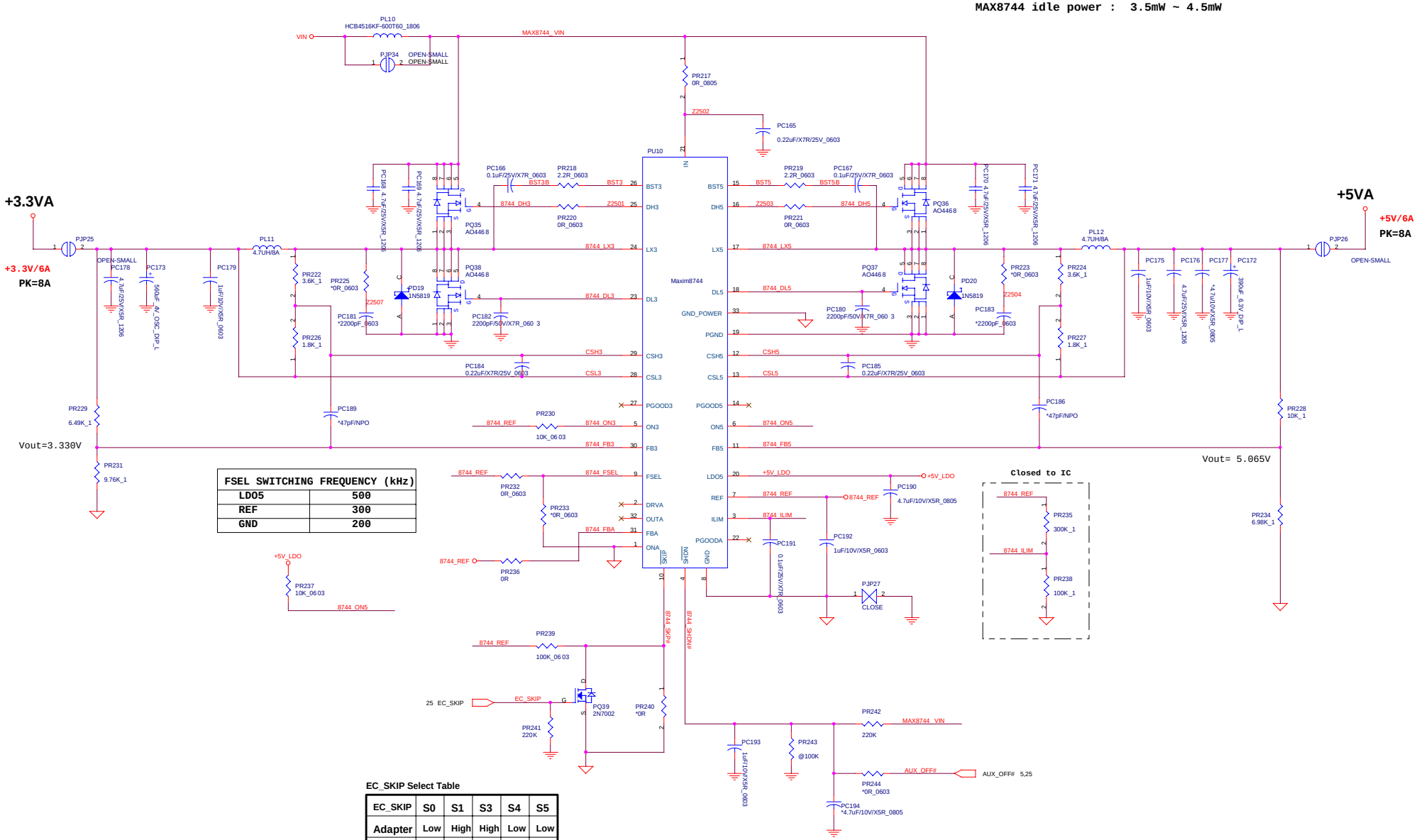
UNIWILL COMPUTER CORP.		
Title: +1.8V_DDR (OZ811)		
Size:	Document Number: 3737 Custom L53IIX	Rev: A1
Date: Monday, December 18, 2006	Sheet 29 of 34	



Ichg	Vchg
2.0A	12.675V
1.0A	12.641V
0A	12.608V

	ADAPTOR_I
2.5A	0.767V
3.0A	0.914V
3.5A	1.058V
4.0A	1.2V
4.5A	1.333V
5A	1.458V

MAX8744 standby current : 65 ~ 120 uA
MAX8744 idle power : 3.5mW ~ 4.5mW



FSEL SWITCHING FREQUENCY (kHz)	
LDO5	500
REF	300
GND	200

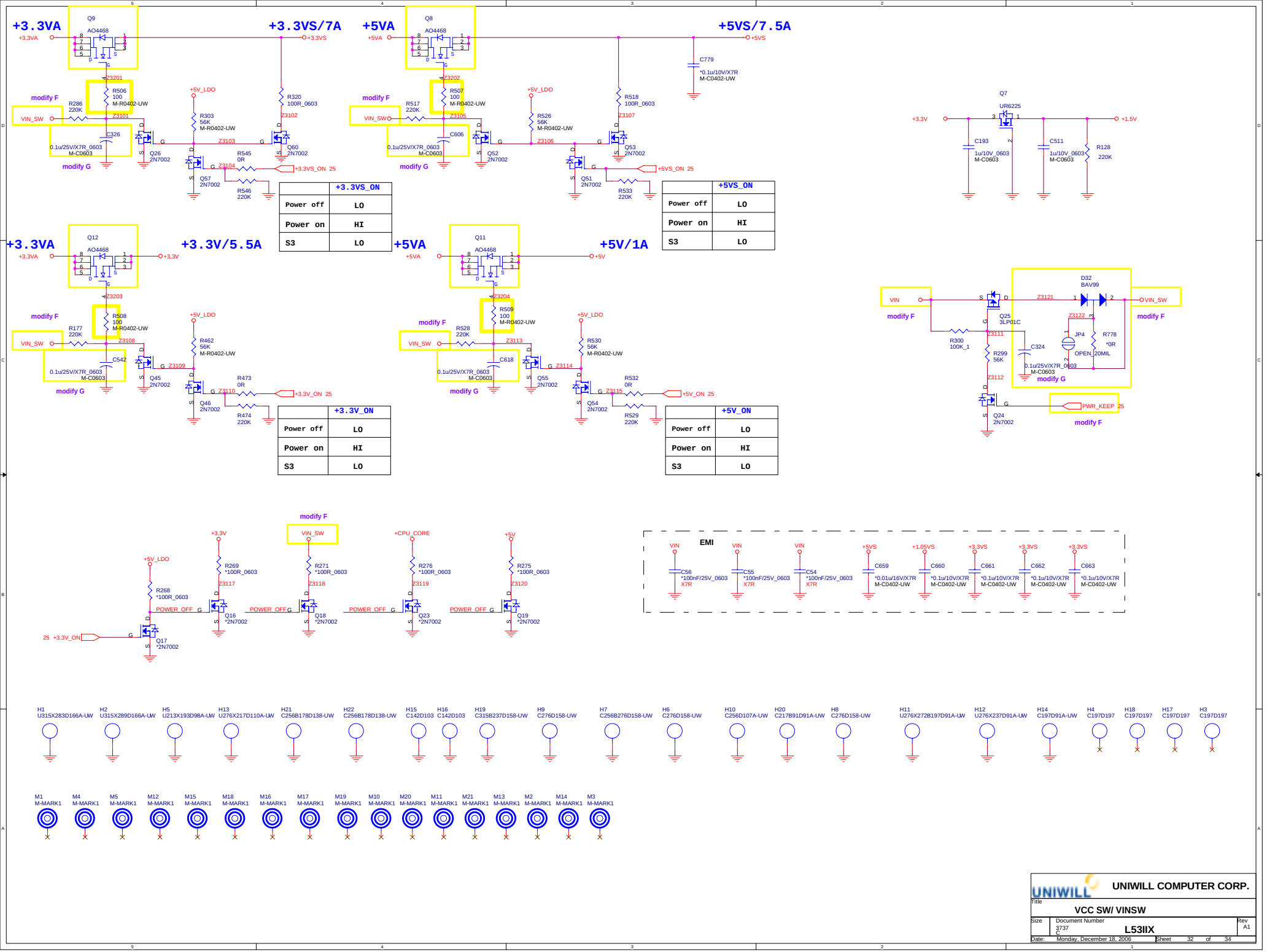
EC_SKIP Select Table

EC_SKIP	S0	S1	S3	S4	S5
Adapter	Low	High	High	Low	Low
Battery	Low	Low	Low	Low	Low

High = Enable MAX8744 normal idle-mode (pulse-skipping).
Low = Enable MAX8744 ultrasonic mode (pulse skipping, 25kHz min).

UNIWILL COMPUTER CORP.

Title	SYSTEM POWER (MA X8744)	
Size	Document Number: 3737 Custom L53IIX	Rev A1
Date: Monday, December 18, 2006	Sheet 31 of 34	



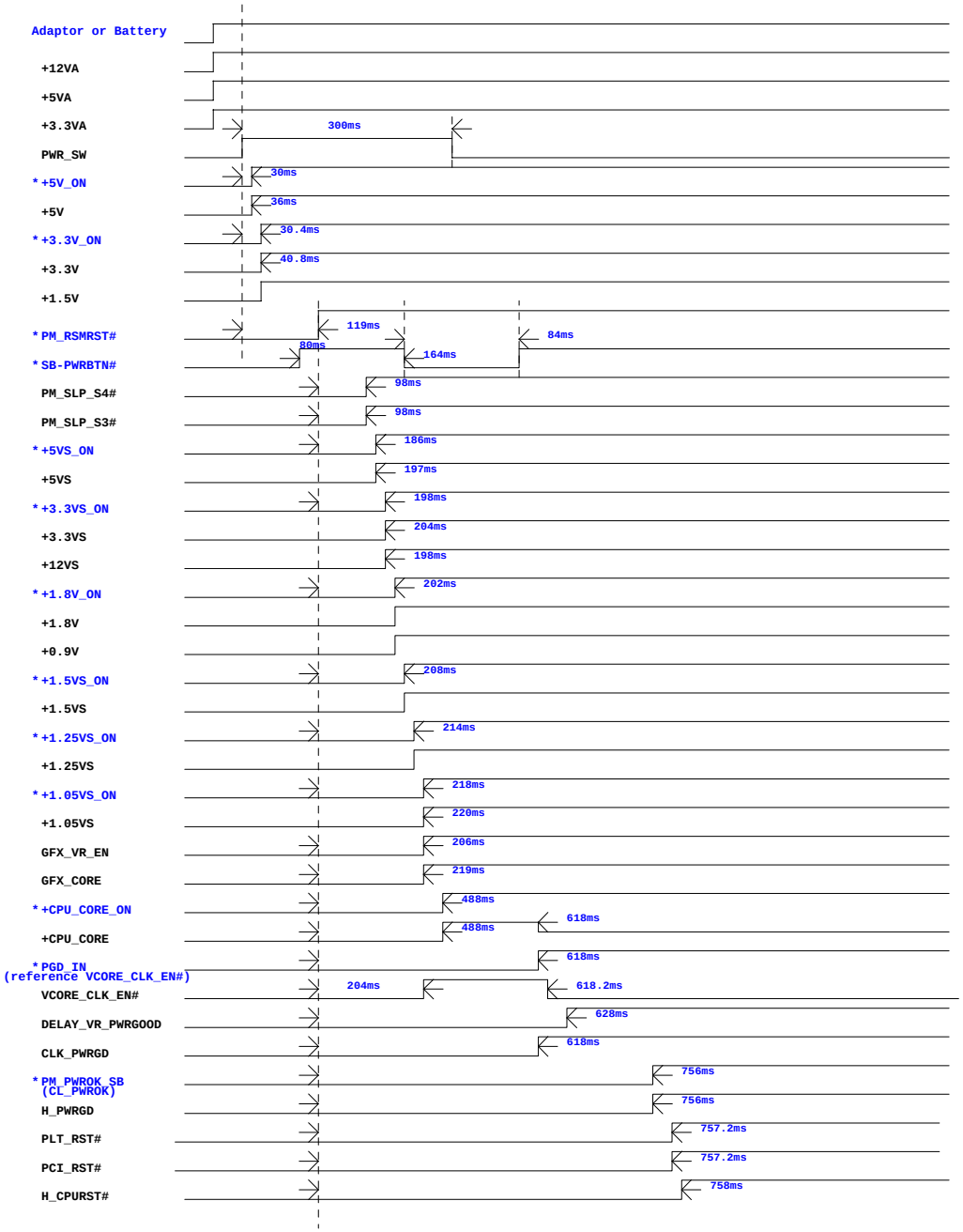
	+3.3VS_ON
Power off	LO
Power on	HI
S3	LO

	+5VS_ON
Power off	LO
Power on	HI
S3	LO

	+3.3V_ON
Power off	LO
Power on	HI
S3	LO

	+5V_ON
Power off	LO
Power on	HI
S3	LO

L53II POWER ON SEQUENCE



UNIWILL	UNIWILL COMPUTER CORP.	
Title	POWER ON SEQUENCE	
Size	Document Number 3737 C L53IIX	Rev A1
Date: Monday, December 18, 2006	Sheet 33 of 34	

L53II change list:

Sch Rev.	PCB Rev.	Data	Symbol	REVISION DESCRIPTION
	37GL53010-A0	2006/11/26	modify A	1. Change R453/R454/R455/R456/R457/R458/R448/R467/R461/R563/R131/R132/R130 Pull up power +3.3VA to +3.3V(Page 17) 2. Change D4 Pull up power +3.3VA to +3.3V (Page.18) 3. Change R446 Pull up power +3.3V to +3.3VS (Page.17) 4. Change R133 8.2K to NA.R318,R558 4.7K to NA(Page 17) 5. Change R477 10R to NA,R703 mount to 10R.(Page 18) 6. Change R16 mount to 30K.(Page9) 7. Change PR119,PR113 to NA.(Page25),for Watch DOG use. 8. Change U12 value 74HC1G00 to NC7SZ00P5X.(Page22)
		2006/11/26	modify B	1. Del R67 for net H_FERR#(Page 16)
		2006/11/28	modify C	1. Change R15 NA to 100K(Page 9) 2. Change PR161 30K to NA.(Page 27)
		2006/11/29	modify D	1. Change R45 0R to NA.(Page 9)
		2006/12/01	modify E	1. Change R664 mount to 0R.(Page23)
		2006/12/05	modify F	1. Change C403 4.7u/10V/X5R_0805 to 33uF/6.3V_B2.(Page 19) 2. Change R14 *10K to *100K.(Page19) 3. Change U2,U3 74AHC1G08DCKR to *100K.(Page15)

UNIWILL COMPUTER CORP.

Title: Appendix A. Ver. History

Size	Document Number	Rev
	3737 Custom L53IIX	A1

Date: Monday, December 18, 2006 Sheet 34 of 34