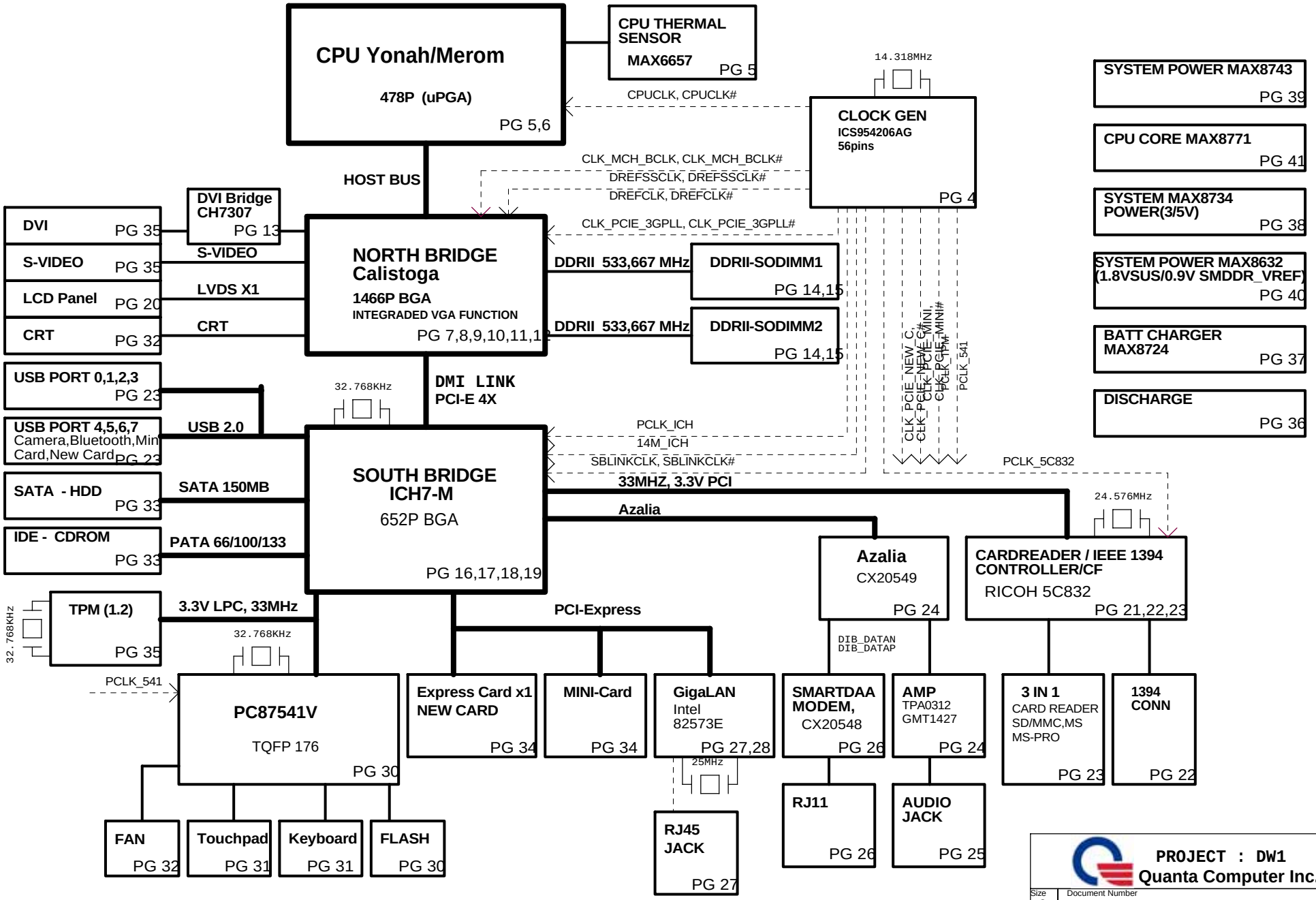
DW1 BLOCK DIAGRAM

Yonah / Calistoga / ICH7-M



PROJECT : DW1
Quanta Computer Inc.

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Power & Ground

Label	ACTIVE	Description	Control Signal
VIN	S0, S3, S4, S5	AC ADAPTER (19V)	
MBAT	S0, S3, S4, S5	MAIN BATTERY + (10~17V)	
VCCRTC	S0, S3, S4, S5	RTC & KBC POWER (3_3V)	
+15V	S0, S3, S4, S5	+15V	
CPU_CORE	S0	CPU CORE POWER (1.25/1.15V)	VRON
+1.05V	S0	FSB POWER (1.05V)	VRON
+3V	S0		MAIND
3VSUS	S0, S3		SUSON
3V_S5	S0, S3, S4, S5		S5_ON
3VPCU	S0, S3, S4, S5	ALWAYS POWER (3V)	
+5V	S0		MAIND
5VSUS	S0, S3		SUSON
5V_S5	S0, S3, S4, S5		S5_ON
5VPCU	S0, S3, S4, S5	ALWAYS POWER (5V)	
+1.5V	S0		MAIND
1.5V_S5	S0, S3, S4, S5		S5_ON
1.8VSUS	S0, S3	DDR CORE POWER	SUSON
+2.5V	S0		MAINON
SMDDR_VTERM	S0	DDR COMMAND & CONTROL PULL UP POWER	MAINON
SMDDR_VREF	S0, S3	DDR REF POWER	SUSON
VDDA	S0	AUDIO ANALOG POWER (5V)	MAINON
GND	ALL PAGES	DIGITAL GROUND	
AGND		AUDIO GND	
T-GND		AUDIO JACK GND	
6260AGND		CPU ANALOG GROUND	

PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
Ricoh 5C832	AD25	0	E,F

PCB STACK UP

LAYER 1 : TOP
LAYER 2 : GND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : GND
LAYER 6 : IN3
LAYER 7 : VCC
LAYER 8 : BOT

SM BUS

DEVICE	ADDRESS	BUS
CLOCK GENERATOR	D2H	(ICH6)PCLK_SMB, PCLK_SMB
DDR II	A0H	(ICH6)PCLK_SMB, PCLK_SMB
LCD EDID	TBD	GMCH
CHARGER	16H	(KBC) MBDATA,MBCLK
CPU THERMAL SENSOR	98H	(KBC) MBDATA,MBCLK

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	System Information	1A

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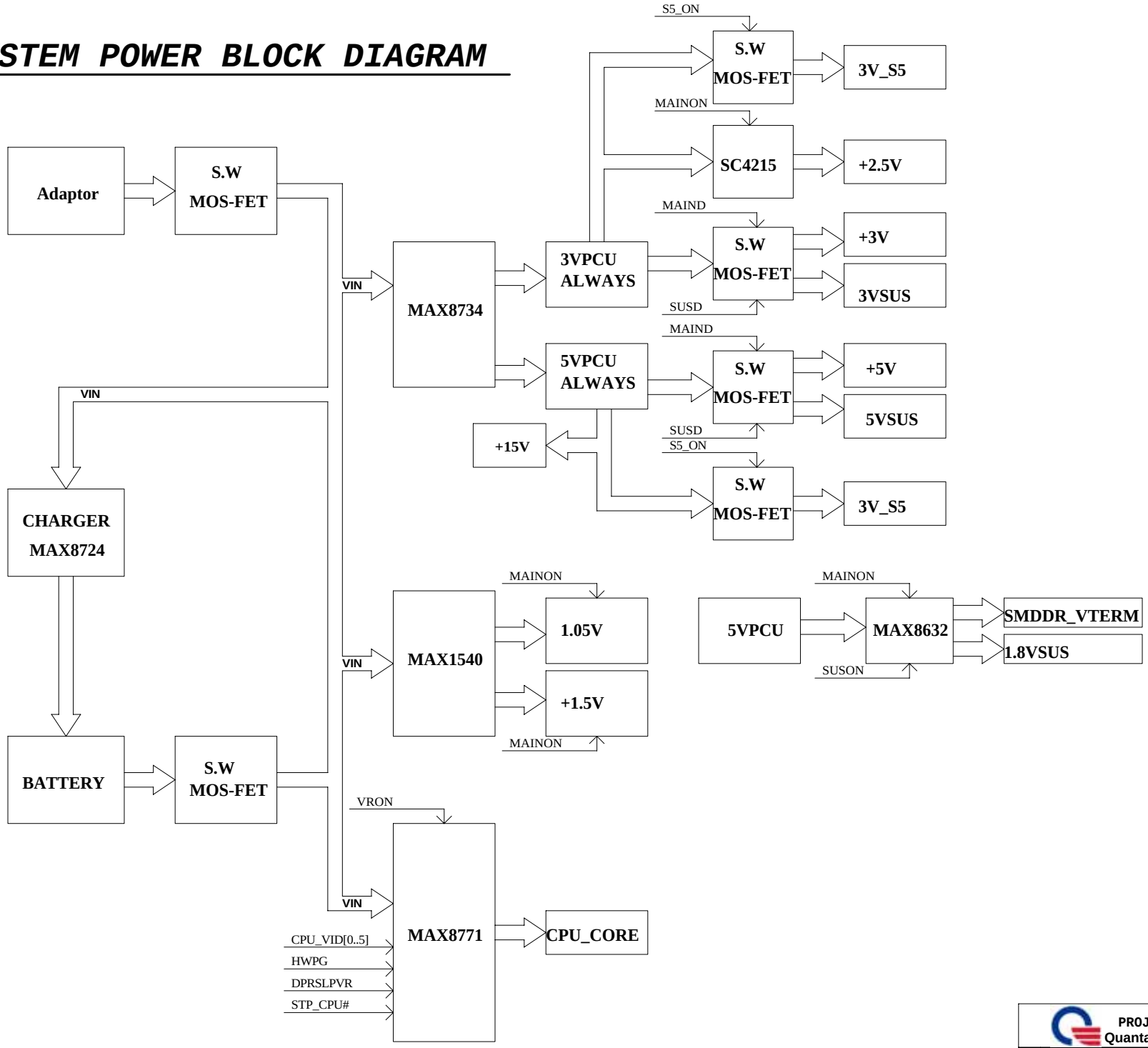
SYSTEM POWER BLOCK DIAGRAM



PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
C	System Power block diagram	1A

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

(5,9,11,13,14,15,16,17,18,19,20,24,29,30,31,32,33,34,35,36,38) +3V

(5,6,7,10,11,16,19,36,39) +1.05V

Close to IC <500mils

Place these termination to close CK410M.

CK-410M

ICS954206AG-T

SMbus address D2 /IDT

Iref=5mA,
Ioh=4*Iref

DREFSSCLK Frequency Select.
"0" : 96MHz
"1" : 100MHz

To check intel reference circuit default setting.
100MHZ? or 96MHZ?
EMI problem?

EMI

48MHZ

33MHZ

14.318MHZ

FSB frequency will be selected by CPU internal.

B Stage:
Change Q9,Q10 footprint.

Q9 2N7002E

Q10 2N7002E

Place these termination to close CK410M.

Project	PROJECT : DW1
Company	Quanta Computer Inc.
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Document Number	CLOCK GENERATOR
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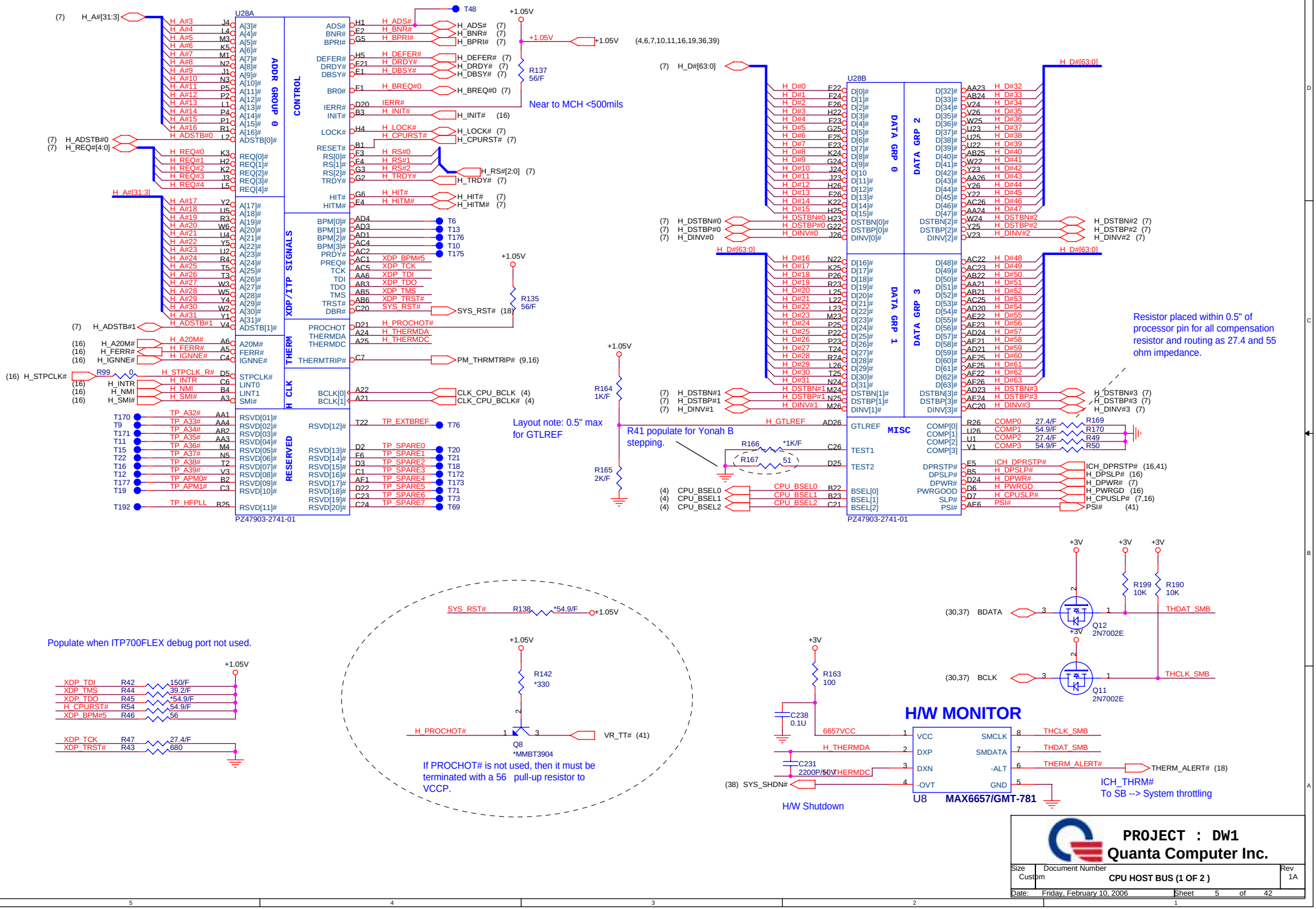
U28A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U28B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
H_A#[31:3]
H_ADSTB#0
H_REQ#[4:0]
H_ADSTB#1
H_A20M#
H_FERR#
H_IGNNE#
H_STPCLK#
H_INTR
H_NMI
H_SMI#
H_D#[63:0]
H_DSTBN#0
H_DSTBP#0
H_DINV#0
H_DSTBN#1
H_DSTBP#1
H_DINV#1
H_ADS#
H_BNR#
H_BPRI#
H_DEFER#
H_DRDY#
H_DBSY#
H_BREQ#0
H_INIT#
H_LOCK#
H_CPURST#
H_RS#[2:0]
H_TRDY#
H_HIT#
H_HITM#
H_PROCHOT#
H_THERMDA
H_THERMDC
PM_THRMTRIP# (9,16)
SYS_RST# (18)
CLK_CPU_BCLK (4)
CLK_CPU_BCLK# (4)
H_GTLREF
CPU_BSEL0
CPU_BSEL1
CPU_BSEL2
+1.05V
(4,6,7,10,11,16,19,36,39)
R137 56/F
Near to MCH <500mils
R135 56/F
R164 1K/F
R165 2K/F
Layout note: 0.5" max for GTLREF
R41 populate for Yonah B stepping.
R166 *1K/F
R167 51
Resistor placed within 0.5" of processor pin for all compensation resistor and routing as 27.4 and 55 ohm impedance.
R169
R170
R49
R50
COMP0 27.4/F
COMP1 54.9/F
COMP2 27.4/F
COMP3 54.9/F
ICH_DPRSTP# (16,41)
H_DPSLP# (16)
H_DPWR# (7)
H_PWRGD (16)
H_CPUSLP# (7,16)
PSI# (41)
Populate when ITP700FLEX debug port not used.
XDP_TDI R42 150/F
XDP_TMS R44 39.2/F
XDP_TDO R45 *54.9/F
H_CPURST# R54 54.9/F
XDP_BPM#5 R46 56
XDP_TCK R47 27.4/F
XDP_TRST# R43 680
SYS_RST# R138 *54.9/F
R142 *330
Q8 *MMBT3904
If PROCHOT# is not used, then it must be terminated with a 56 pull-up resistor to VCCP.
R199 10K
R190 10K
(30,37) BDATA
(30,37) BCLK
Q12 2N7002E
Q11 2N7002E
THDAT_SMB
THCLK_SMB
H/W MONITOR
R163 100
C238 0.1U
C231 2200P/50V
6657VCC
H_THERMDA
H_THERMDC
(38) SYS_SHDN#
H/W Shutdown
U8 MAX6657/GMT-781
THERM_ALERT# (18)
ICH_THRM#
To SB --> System throttling
PROJECT : DW1
Quanta Computer Inc.
CPU HOST BUS (1 OF 2)
Size Custom
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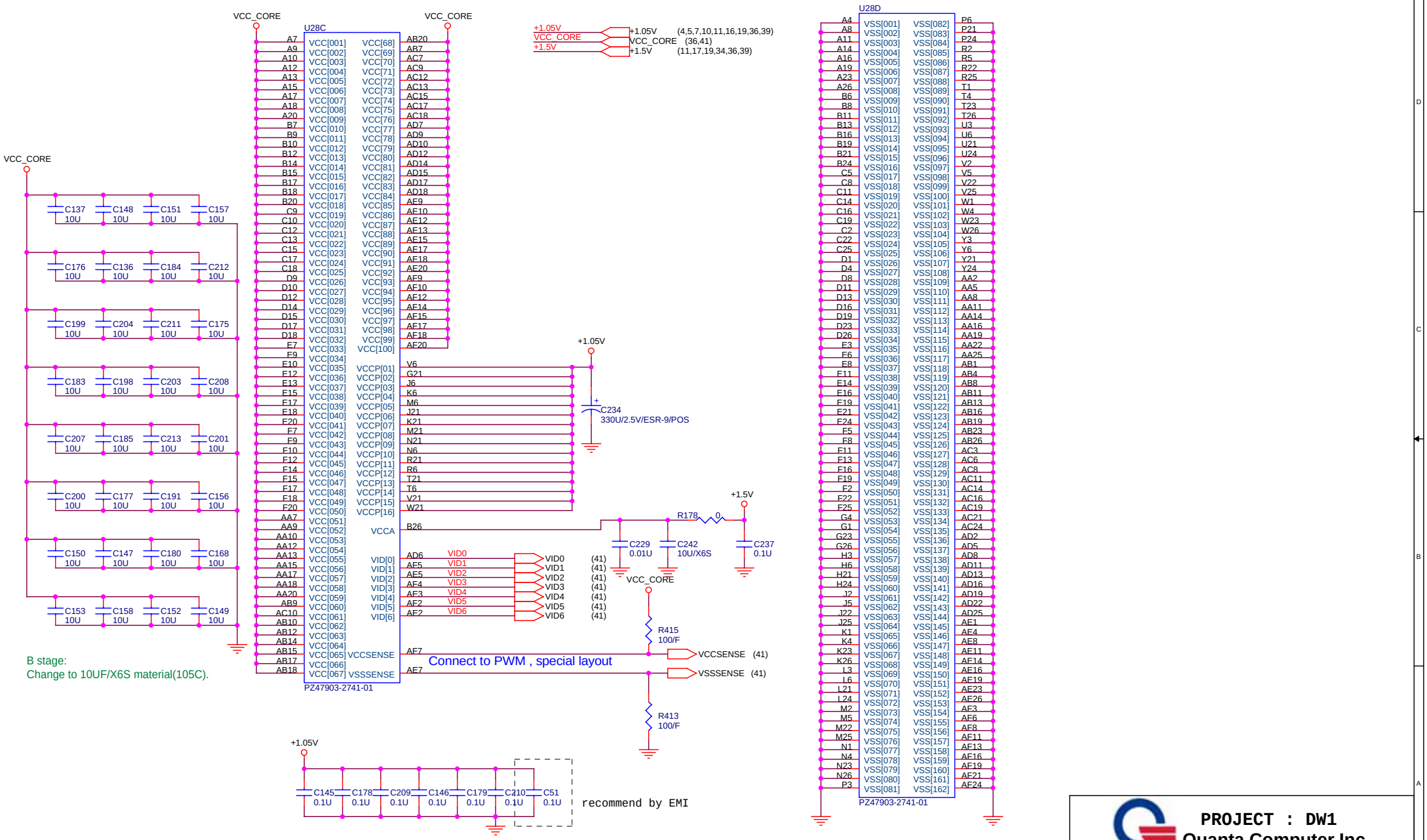

PROJECT : DW1		
Quanta Computer Inc.		
Size: B	Document Number: CPU POWER/GND (2 OF 2)	Rev: 1A
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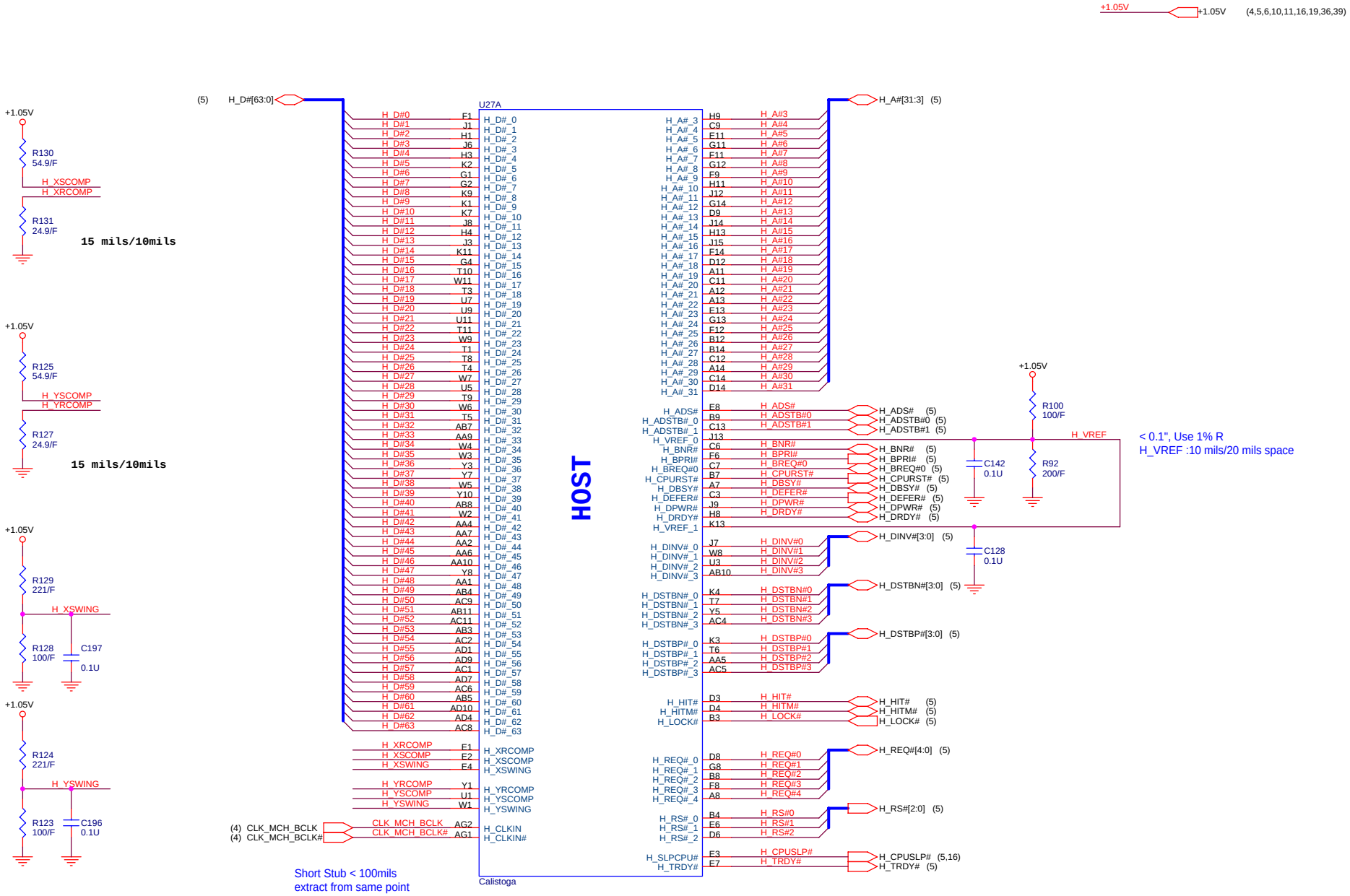
+1.05V
+1.05V (4,5,6,10,11,16,19,36,39)
(5) H_D#[63:0]
U27A
HOST
Calistoga
H_A#[31:3] (5)
R130 54.9/F
H_XSCOMP
H_XRCOMP
R131 24.9/F
15 mils/10mils
R125 54.9/F
H_YSCOMP
H_YRCOMP
R127 24.9/F
15 mils/10mils
R129 221/F
H_XSWING
R128 100/F
C197 0.1U
R124 221/F
H_YSWING
R123 100/F
C196 0.1U
R100 100/F
H_VREF
R92 200/F
C142 0.1U
C128 0.1U
< 0.1", Use 1% R
H_VREF :10 mils/20 mils space
(4) CLK_MCH_BCLK
(4) CLK_MCH_BCLK#
Short Stub < 100mils
extract from same point
H_ADS# (5)
H_ADSTB#0 (5)
H_ADSTB#1 (5)
H_BNR# (5)
H_BPRI# (5)
H_BREQ#0 (5)
H_CPURST# (5)
H_DBSY# (5)
H_DEFER# (5)
H_DPWR# (5)
H_DRDY# (5)
H_DINV#[3:0] (5)
H_DSTBN#[3:0] (5)
H_DSTBP#[3:0] (5)
H_HIT# (5)
H_HITM# (5)
H_LOCK# (5)
H_REQ#[4:0] (5)
H_RS#[2:0] (5)
H_CPUSLP# (5,16)
H_TRDY# (5)
PROJECT : DW1
Quanta Computer Inc.
Size Custom
Document Number GMCH HOST(1 OF 6)
Rev 1A
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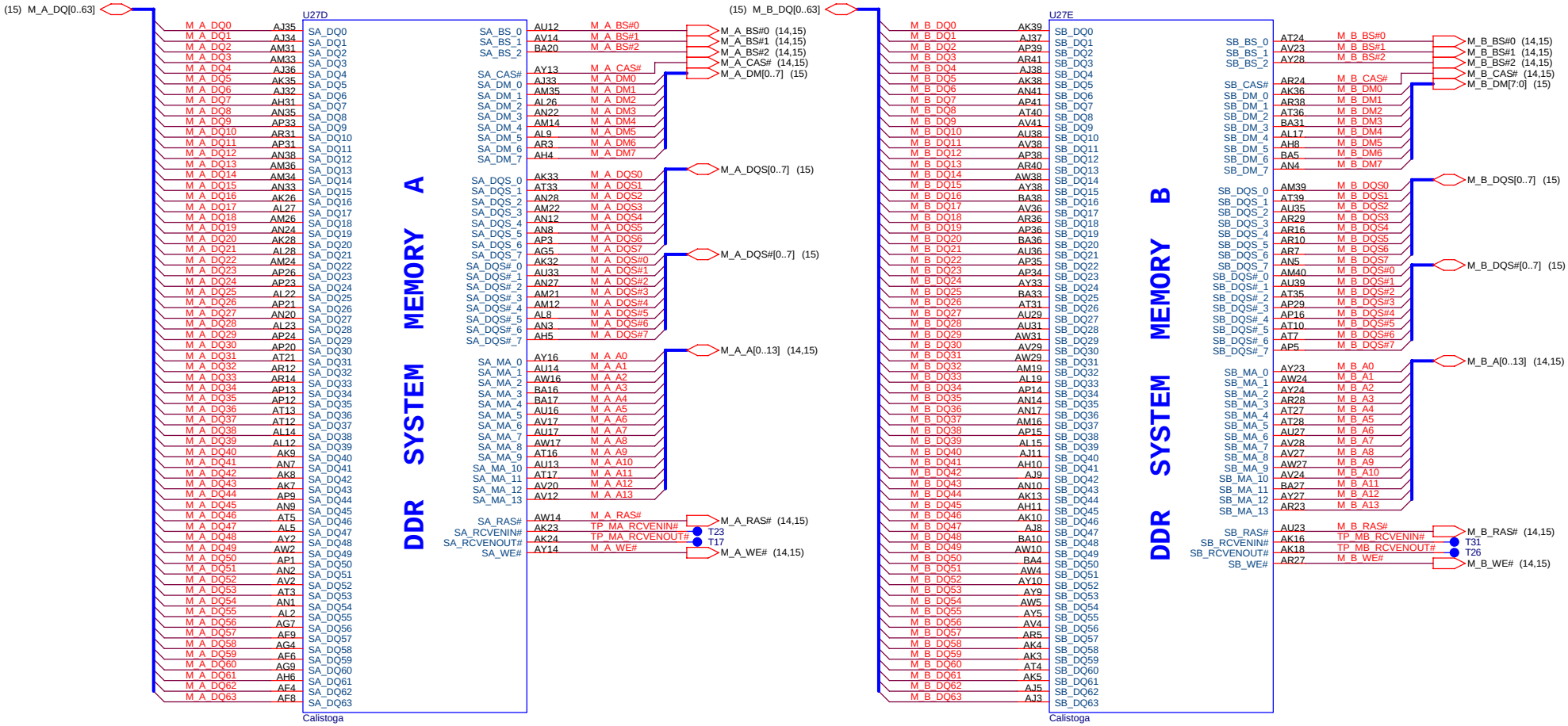

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
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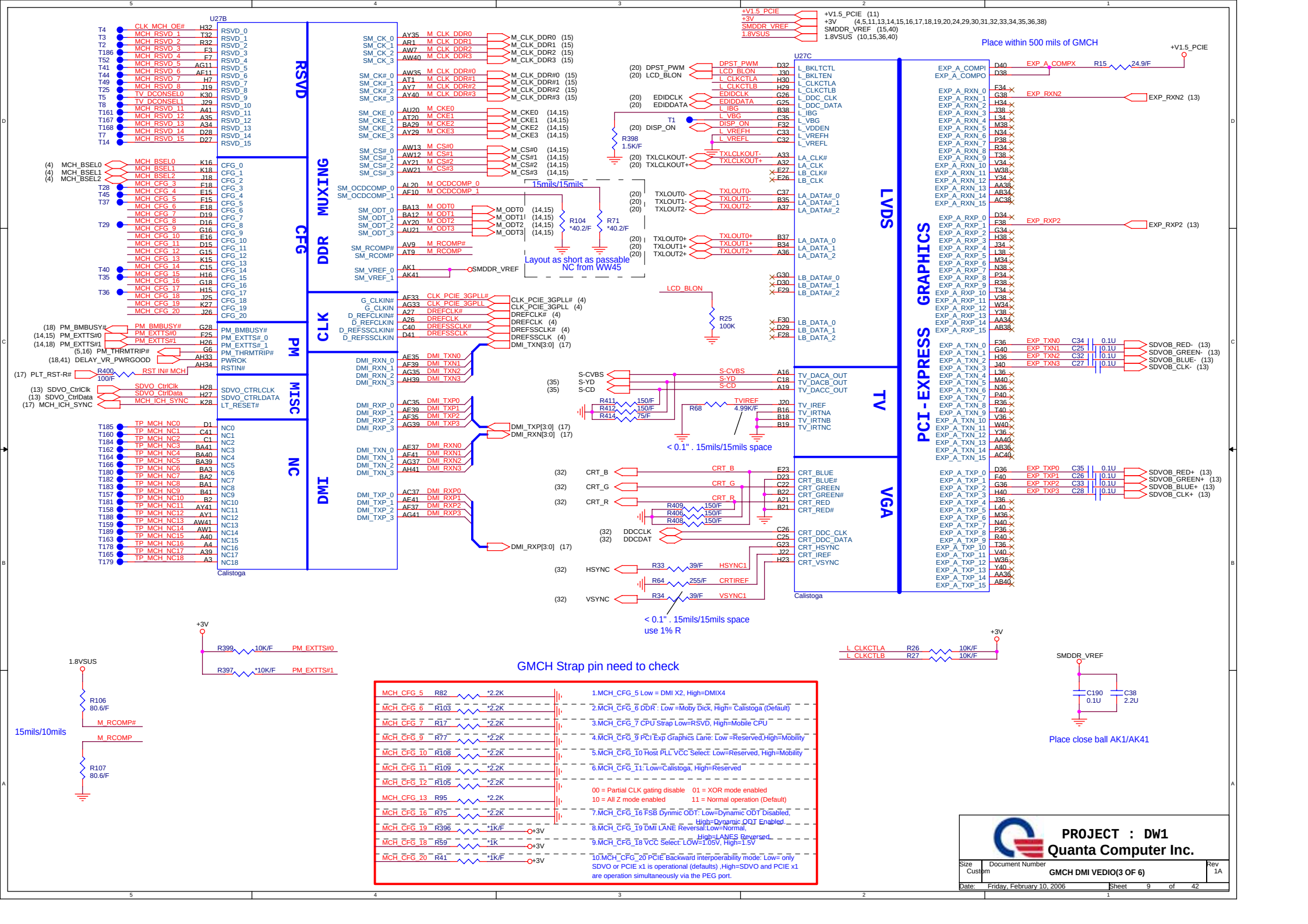
U27B
RSVD
CFG
DDR MUXING
CLK
PM
MISC
DMI
NC
Calistoga
U27C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
Calistoga
15mils/15mils
Layout as short as passable
NC from WW45
< 0.1" . 15mils/15mils space
< 0.1" . 15mils/15mils space
use 1% R
Place within 500 mils of GMCH
Place close ball AK1/AK41
15mils/10mils
GMCH Strap pin need to check
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: Low=Calistoga, High=Reserved
00 = Partial CLK gating disable 01 = XOR mode enabled
10 = All Z mode enabled 11 = Normal operation (Default)
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled
8.MCH_CFG_19 DMI LANE Reversal:Low=Normal, High=LANES Reversed
9.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.
PROJECT : DW1
Quanta Computer Inc.
GMCH DMI VEDIO(3 OF 6)
Size Custom
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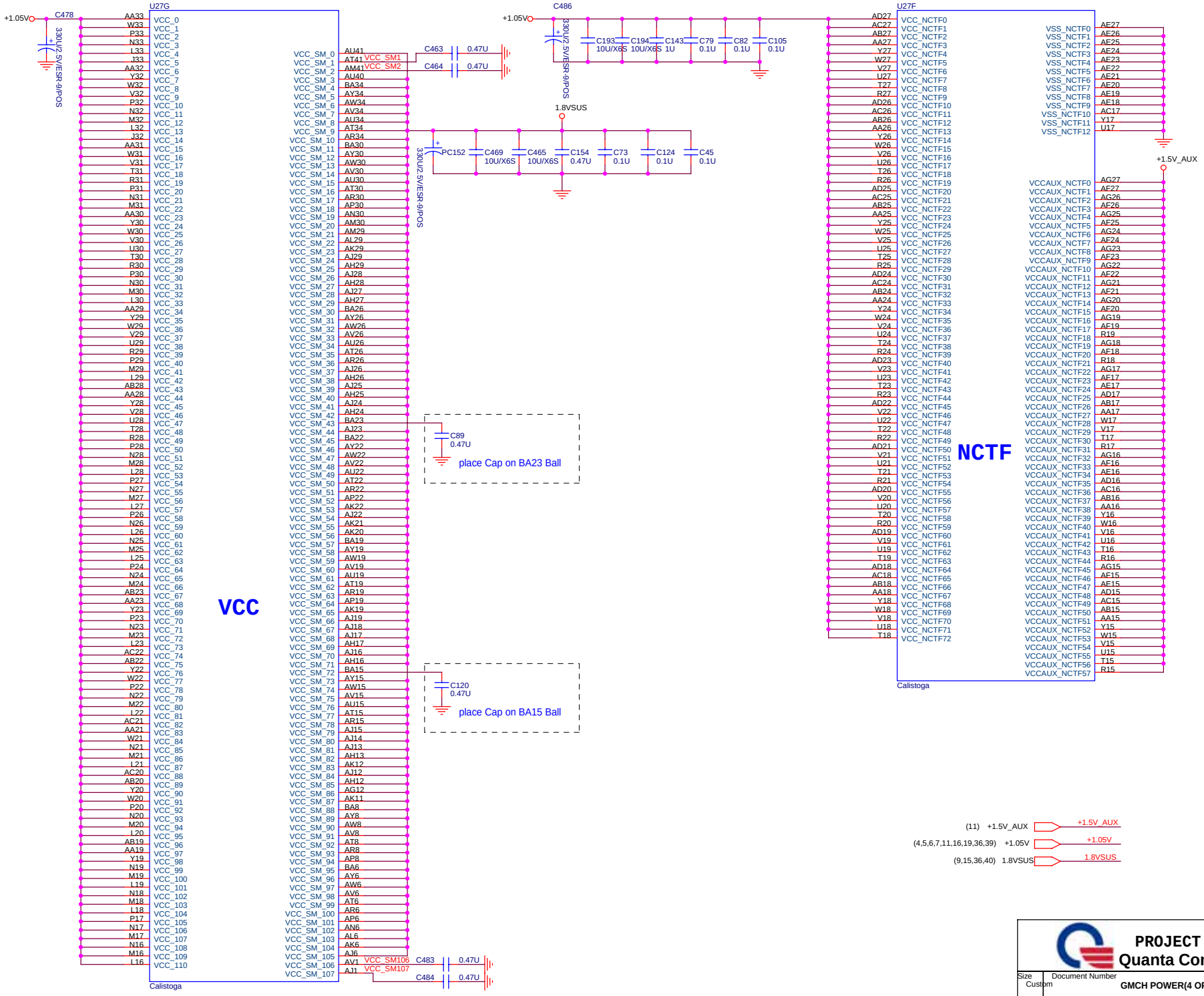
U27G
VCC
Calistoga
+1.05V
C478
330U/2.5VESR-9/POS
C486
C193 10U/X6S
C194 10U/X6S
C143 1U
C79 0.1U
C82 0.1U
C105 0.1U
C463 0.47U
C464 0.47U
1.8VSUS
PC152
C469 10U/X6S
C465 10U/X6S
C154 0.47U
C73 0.1U
C124 0.1U
C45 0.1U
C89 0.47U
place Cap on BA23 Ball
C120 0.47U
place Cap on BA15 Ball
C483 0.47U
C484 0.47U
U27F
NCTF
Calistoga
+1.5V_AUX
(11) +1.5V_AUX
(4,5,6,7,11,16,19,36,39) +1.05V
(9,15,36,40) 1.8VSUS
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Quanta Computer Inc.
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Document Number
GMCH POWER(4 OF 6)
Rev 1A
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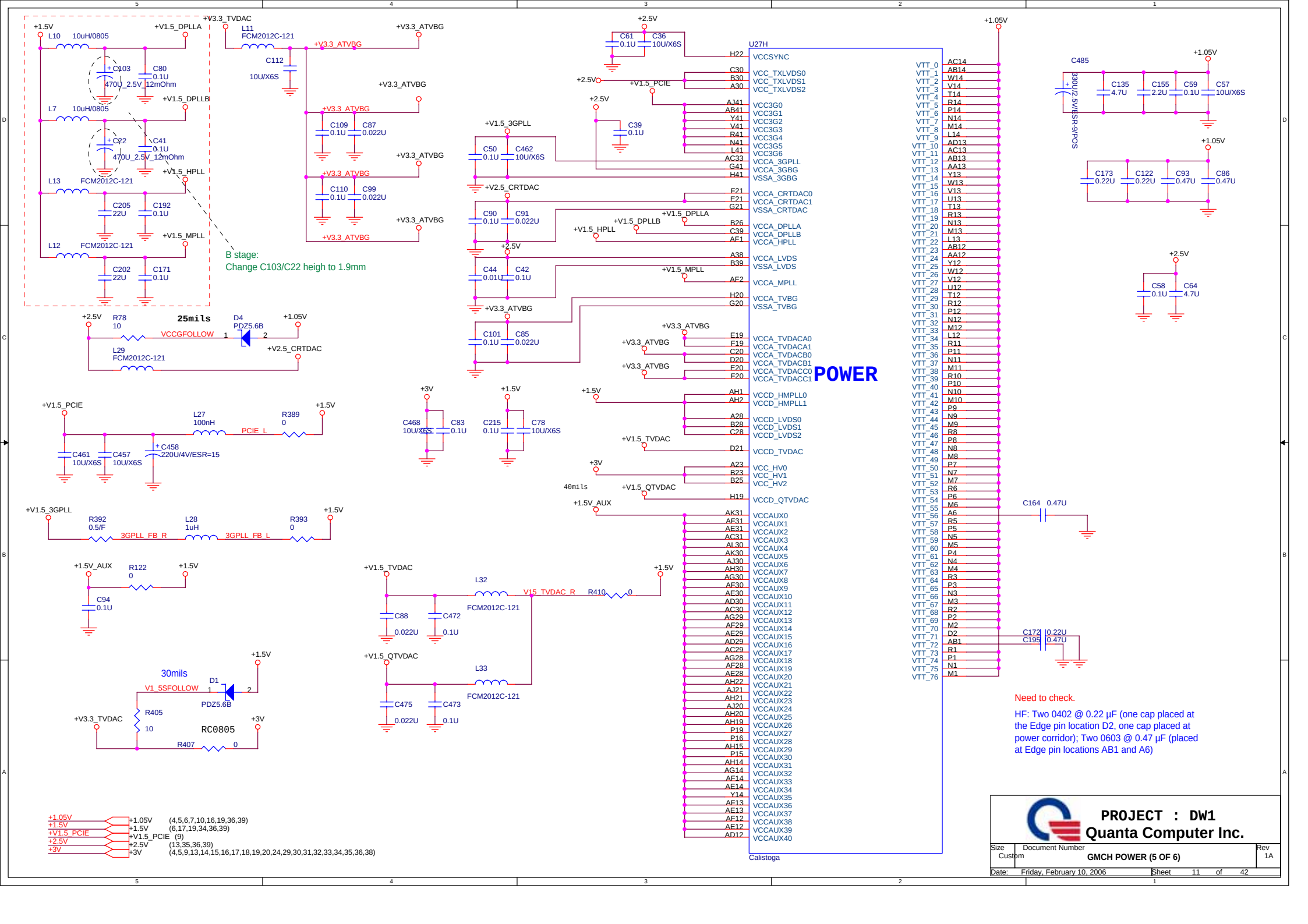
+1.5V
L10 10uH/0805
+V1.5_DPLLA
+V3.3_TVDAC
L11 FCM2012C-121
+V3.3_ATVBG
C103 470U_2.5V_12mOhm
C80 0.1U
C112 10U/X6S
+V1.5_DPLLB
L7 10uH/0805
C22 470U_2.5V_12mOhm
C41 0.1U
C109 0.1U
C87 0.022U
C110 0.1U
C99 0.022U
+V1.5_HPLL
L13 FCM2012C-121
C205 22U
C192 0.1U
+V1.5_MPLL
L12 FCM2012C-121
C202 22U
C171 0.1U
B stage:
Change C103/C22 heigh to 1.9mm
+2.5V
R78 10
25mils
VCCGFOLLOW
D4 PDZ5.6B
+1.05V
L29 FCM2012C-121
+V2.5_CRTDAC
+V1.5_PCIE
L27 100nH
PCIE_L
R389 0
C461 10U/X6S
C457 10U/X6S
C458 220U/4V/ESR=15
+V1.5_3GPLL
R392 0.5/F
3GPLL_FB_R
L28 1uH
3GPLL_FB_L
R393 0
+1.5V_AUX
R122 0
C94 0.1U
30mils
V1_5SFOLLOW
D1 PDZ5.6B
R405 10
RC0805
R407 0
+3V
C468 10U/X6S
C83 0.1U
C215 0.1U
C78 10U/X6S
+V1.5_TVDAC
L32 FCM2012C-121
V15_TVDAC_R
R410 0
C88 0.022U
C472 0.1U
+V1.5_QTVDAC
L33 FCM2012C-121
C475 0.022U
C473 0.1U
C61 0.1U
C36 10U/X6S
C39 0.1U
C50 0.1U
C462 10U/X6S
C90 0.1U
C91 0.022U
C44 0.01U
C42 0.1U
C101 0.1U
C85 0.022U
U27H
H22 VCCSYNC
C30 VCC_TXLVDS0
B30 VCC_TXLVDS1
A30 VCC_TXLVDS2
AJ41 VCC3G0
AB41 VCC3G1
Y41 VCC3G2
V41 VCC3G3
R41 VCC3G4
N41 VCC3G5
L41 VCC3G6
AC33 VCCA_3GPLL
G41 VCCA_3GBG
H41 VSSA_3GBG
F21 VCCA_CRTDAC0
E21 VCCA_CRTDAC1
G21 VSSA_CRTDAC
B26 VCCA_DPLLA
C39 VCCA_DPLLB
AF1 VCCA_HPLL
A38 VCCA_LVDS
B39 VSSA_LVDS
AF2 VCCA_MPLL
H20 VCCA_TVBG
G20 VSSA_TVBG
E19 VCCA_TVDACA0
F19 VCCA_TVDACA1
C20 VCCA_TVDACB0
D20 VCCA_TVDACB1
E20 VCCA_TVDACC0
F20 VCCA_TVDACC1
POWER
AH1 VCCD_HMPLL0
AH2 VCCD_HMPLL1
A28 VCCD_LVDS0
B28 VCCD_LVDS1
C28 VCCD_LVDS2
D21 VCCD_TVDAC
A23 VCC_HV0
B23 VCC_HV1
B25 VCC_HV2
H19 VCCD_QTVDAC
AK31 VCCAUX0
AF31 VCCAUX1
AE31 VCCAUX2
AC31 VCCAUX3
AL30 VCCAUX4
AK30 VCCAUX5
AJ30 VCCAUX6
AH30 VCCAUX7
AG30 VCCAUX8
AF30 VCCAUX9
AE30 VCCAUX10
AD30 VCCAUX11
AC30 VCCAUX12
AG29 VCCAUX13
AF29 VCCAUX14
AE29 VCCAUX15
AD29 VCCAUX16
AC29 VCCAUX17
AG28 VCCAUX18
AF28 VCCAUX19
AE28 VCCAUX20
AH22 VCCAUX21
AJ21 VCCAUX22
AH21 VCCAUX23
AJ20 VCCAUX24
AH20 VCCAUX25
AH19 VCCAUX26
P19 VCCAUX27
P16 VCCAUX28
AH15 VCCAUX29
P15 VCCAUX30
AH14 VCCAUX31
AG14 VCCAUX32
AF14 VCCAUX33
AE14 VCCAUX34
Y14 VCCAUX35
AF13 VCCAUX36
AE13 VCCAUX37
AF12 VCCAUX38
AE12 VCCAUX39
AD12 VCCAUX40
Calistoga
VTT_0 AC14
VTT_1 AB14
VTT_2 W14
VTT_3 V14
VTT_4 T14
VTT_5 R14
VTT_6 P14
VTT_7 N14
VTT_8 M14
VTT_9 L14
VTT_10 AD13
VTT_11 AC13
VTT_12 AB13
VTT_13 AA13
VTT_14 Y13
VTT_15 W13
VTT_16 V13
VTT_17 U13
VTT_18 T13
VTT_19 R13
VTT_20 N13
VTT_21 M13
VTT_22 L13
VTT_23 AB12
VTT_24 AA12
VTT_25 Y12
VTT_26 W12
VTT_27 V12
VTT_28 U12
VTT_29 T12
VTT_30 R12
VTT_31 P12
VTT_32 N12
VTT_33 M12
VTT_34 L12
VTT_35 R11
VTT_36 P11
VTT_37 N11
VTT_38 M11
VTT_39 R10
VTT_40 P10
VTT_41 N10
VTT_42 M10
VTT_43 P9
VTT_44 N9
VTT_45 M9
VTT_46 R8
VTT_47 P8
VTT_48 N8
VTT_49 M8
VTT_50 P7
VTT_51 N7
VTT_52 M7
VTT_53 R6
VTT_54 P6
VTT_55 M6
VTT_56 A6
VTT_57 R5
VTT_58 P5
VTT_59 N5
VTT_60 M5
VTT_61 P4
VTT_62 N4
VTT_63 M4
VTT_64 R3
VTT_65 P3
VTT_66 N3
VTT_67 M3
VTT_68 R2
VTT_69 P2
VTT_70 M2
VTT_71 D2
VTT_72 AB1
VTT_73 R1
VTT_74 P1
VTT_75 N1
VTT_76 M1
C485 330U/2.5V/ESR-9/POS
C135 4.7U
C155 2.2U
C59 0.1U
C57 10U/X6S
C173 0.22U
C122 0.22U
C93 0.47U
C86 0.47U
C58 0.1U
C64 4.7U
C164 0.47U
C172 0.22U
C195 0.47U
Need to check.
HF: Two 0402 @ 0.22 µF (one cap placed at the Edge pin location D2, one cap placed at power corridor); Two 0603 @ 0.47 µF (placed at Edge pin locations AB1 and A6)
+1.05V (4,5,6,7,10,16,19,36,39)
+1.5V (6,17,19,34,36,39)
+V1.5_PCIE (9)
+2.5V (13,35,36,39)
+3V (4,5,9,13,14,15,16,17,18,19,20,24,29,30,31,32,33,34,35,36,38)
PROJECT : DW1
Quanta Computer Inc.
Size Custom
Document Number
GMCH POWER (5 OF 6)
Rev 1A
Date: Friday, February 10, 2006
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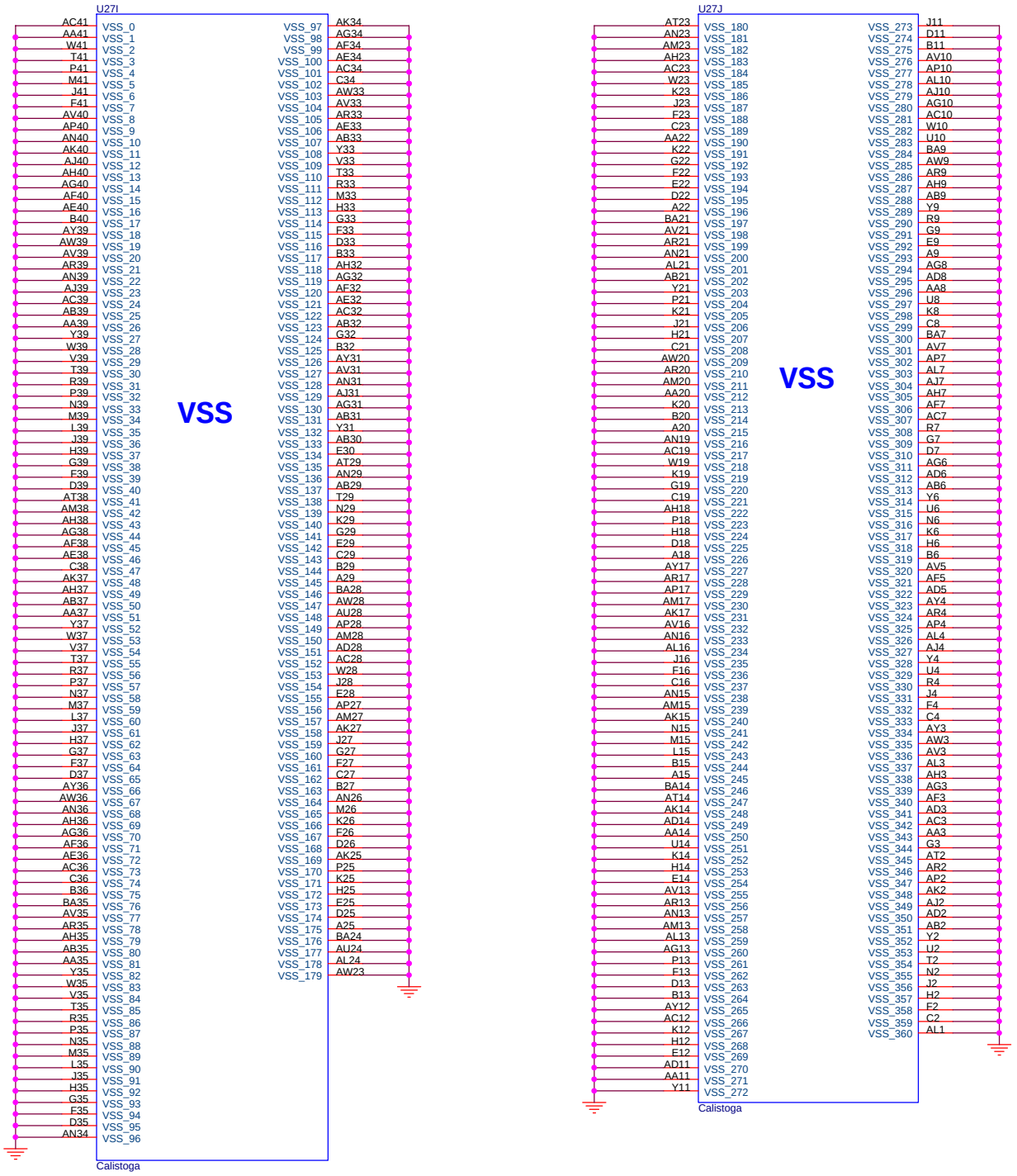
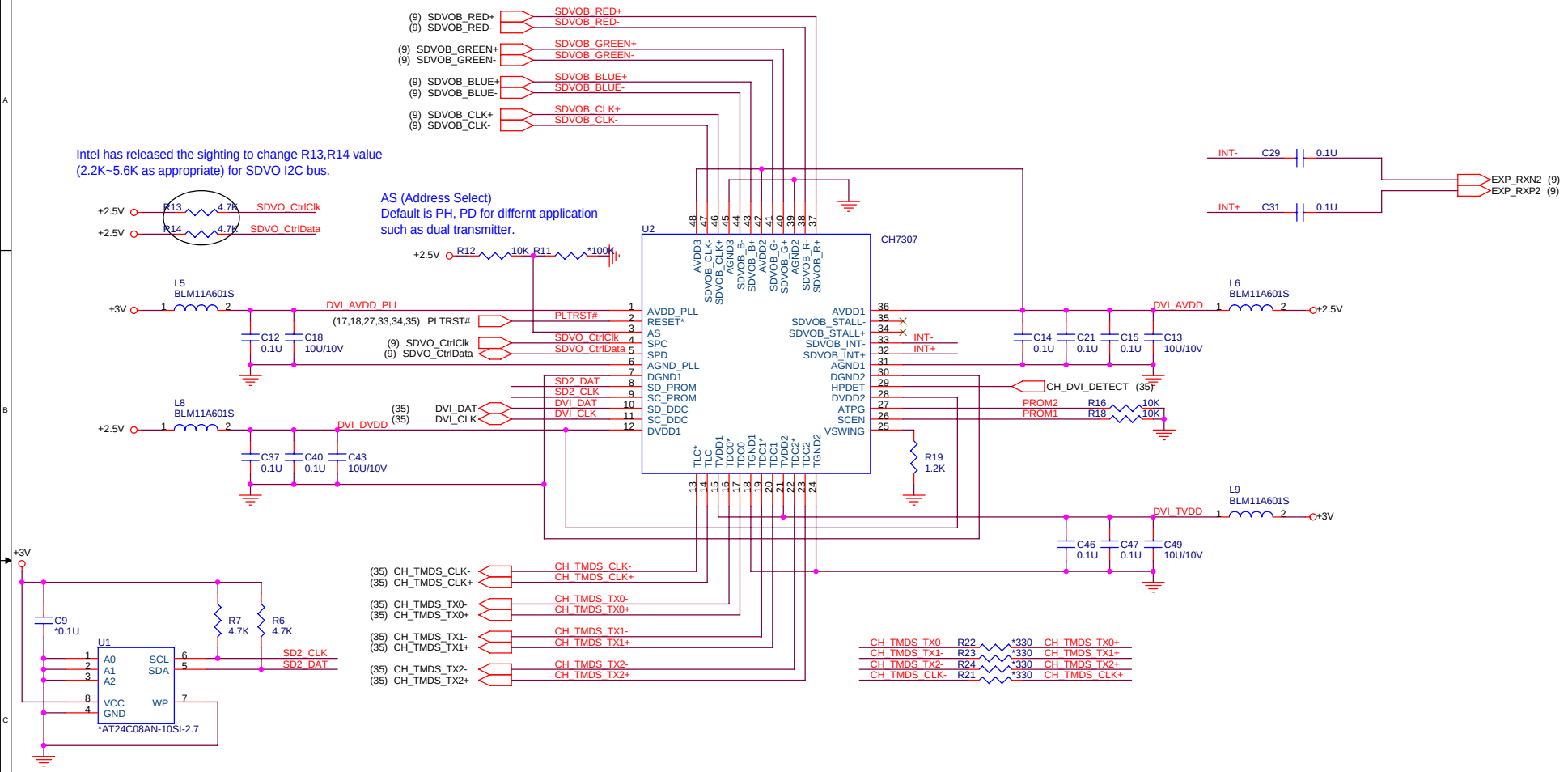


PROJECT : DW1	
Quanta Computer Inc.	
Size: Custom	Document Number: GMCH GND(6 OF 6)
Rev: 1A	
Date: Friday, February 10, 2006	Sheet 12 of 42

GMCH SDVO Signal to DVI Signal Bridge

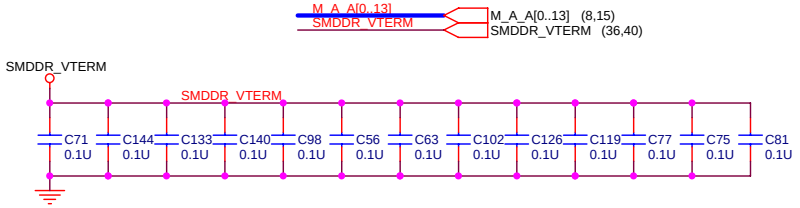


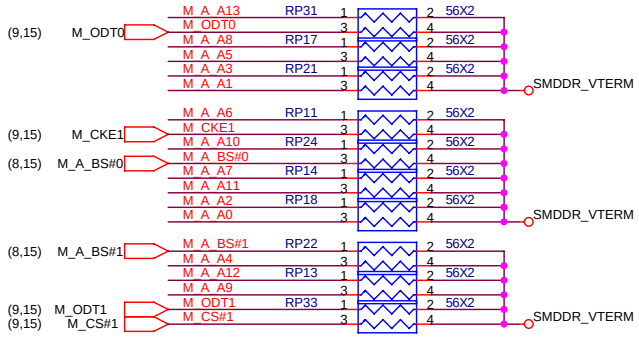
PROJECT : DW1
Quanta Computer Inc.

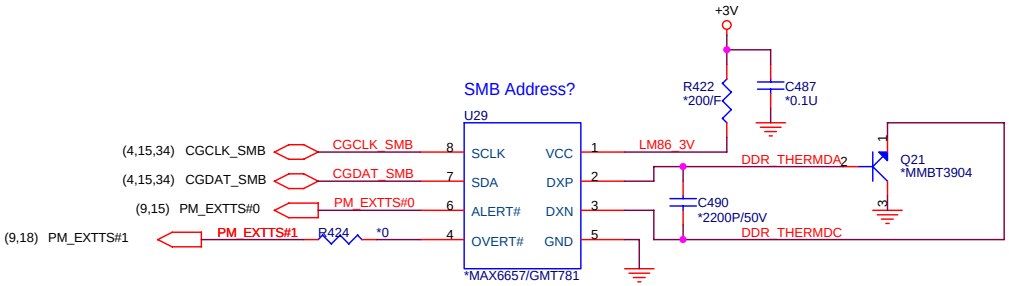
Size	Document Number	Rev
Custom	GMCH SDVO Signal to DVI Signal Bridge	1A
Date: Friday, February 10, 2006	Sheet 13 of 42	

DDRII DUAL CHANNEL A,B

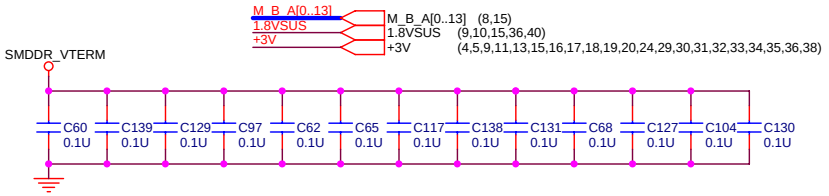
DDRII A CHANNEL



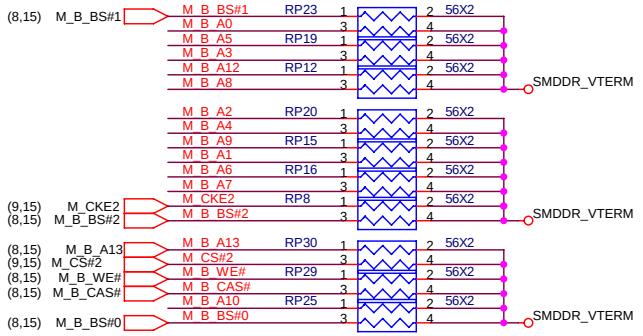


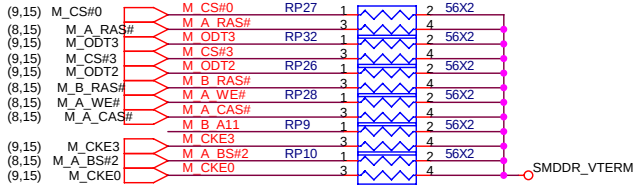


DDRII B CHANNEL



Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

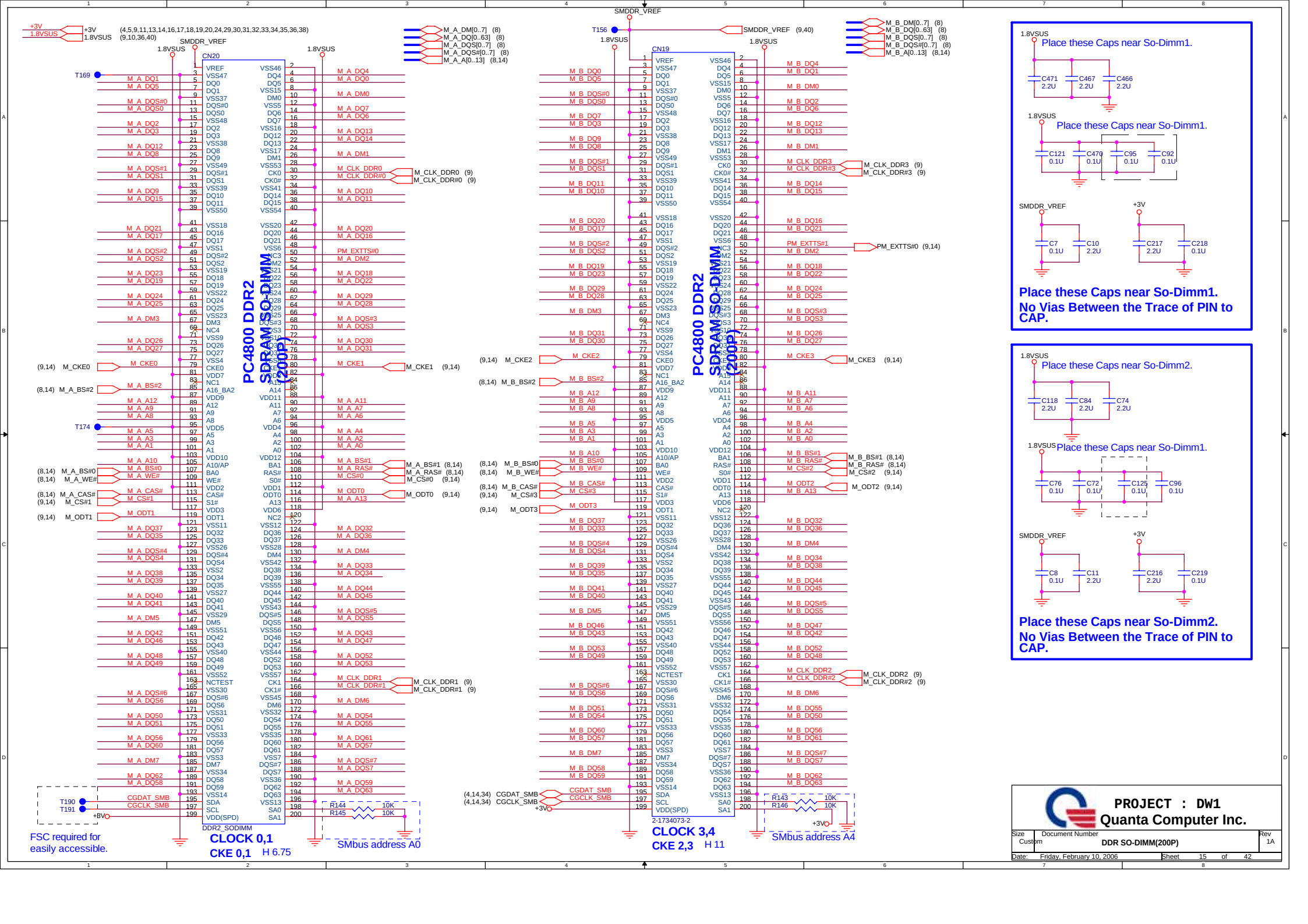




PROJECT : CT6
Quanta Computer Inc.

Size	Document Number	Rev
B	DDR RES. ARRAY	1A

Date: Friday, February 10, 2006 Sheet 14 of 42


CN20
PC4800 DDR2 SDRAM SO-DIMM (200P)
DDR2_SODIMM
CN19
PC4800 DDR2 SDRAM SO-DIMM (200P)
2-1734073-2
SMDDR_VREF
1.8VSUS
+3V
T156
T169
T174
T190
T191
CLOCK 0,1
CKE 0,1 H 6.75
CLOCK 3,4
CKE 2,3 H 11
SMbus address A0
SMbus address A4
FSC required for easily accessible.
Place these Caps near So-Dimm1.
No Vias Between the Trace of PIN to CAP.
Place these Caps near So-Dimm2.
No Vias Between the Trace of PIN to CAP.
PROJECT : DW1
Quanta Computer Inc.
DDR SO-DIMM(200P)
Friday, February 10, 2006
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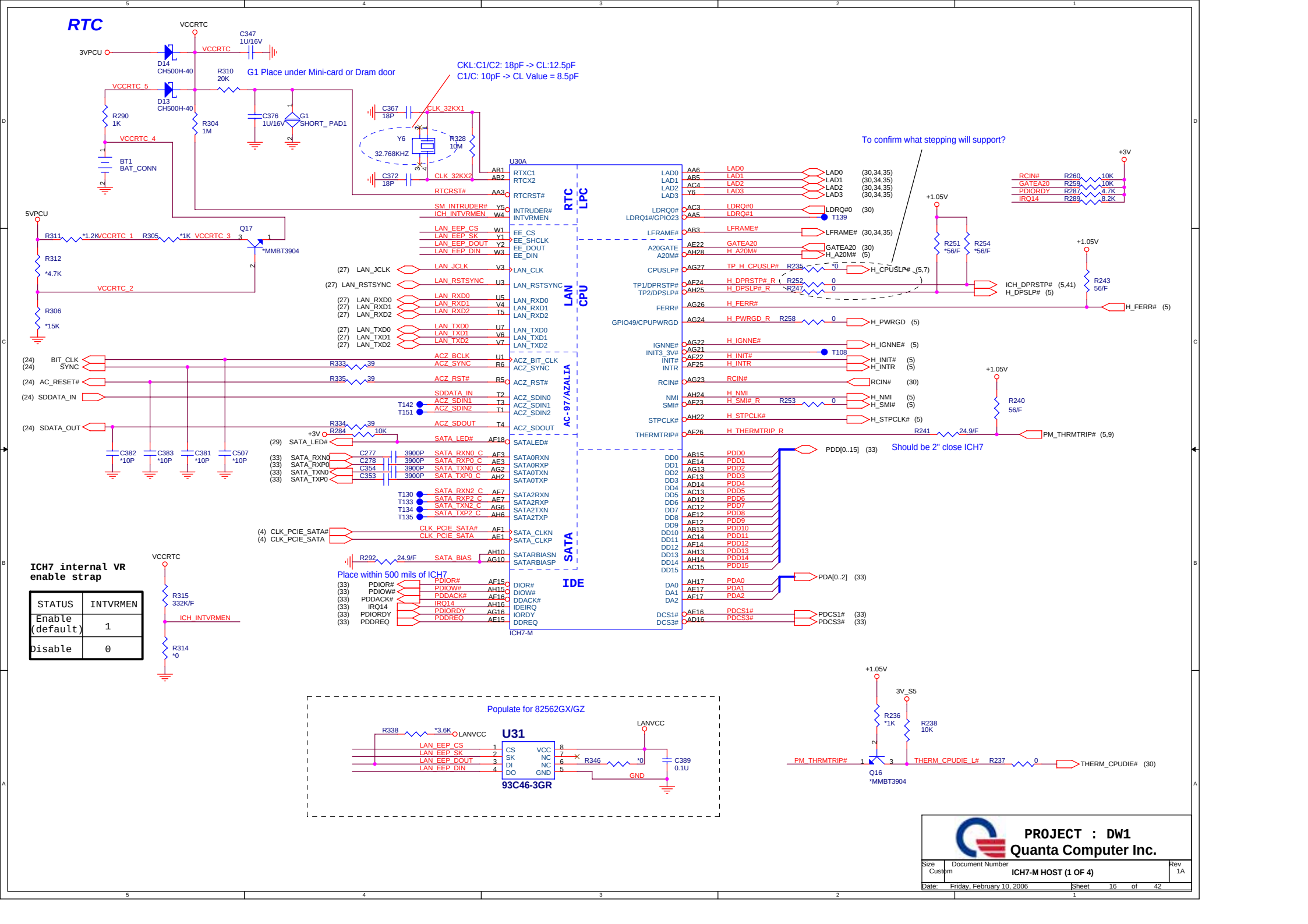
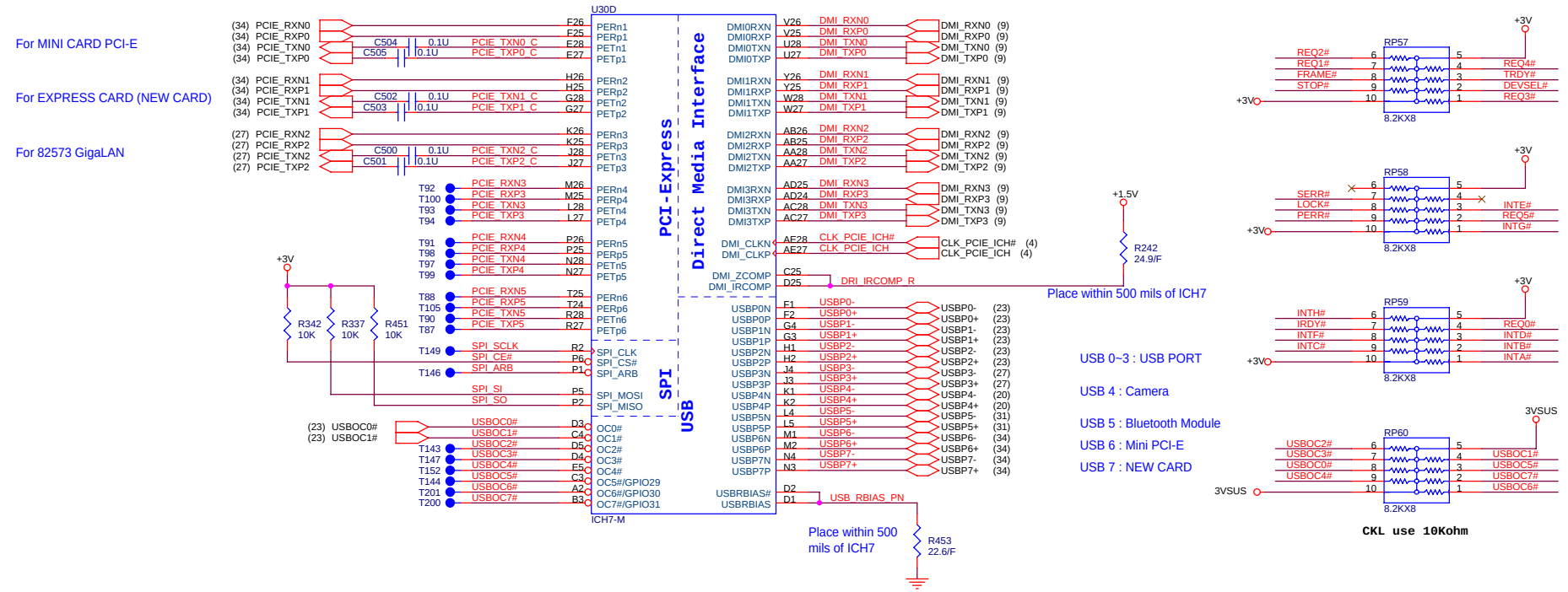
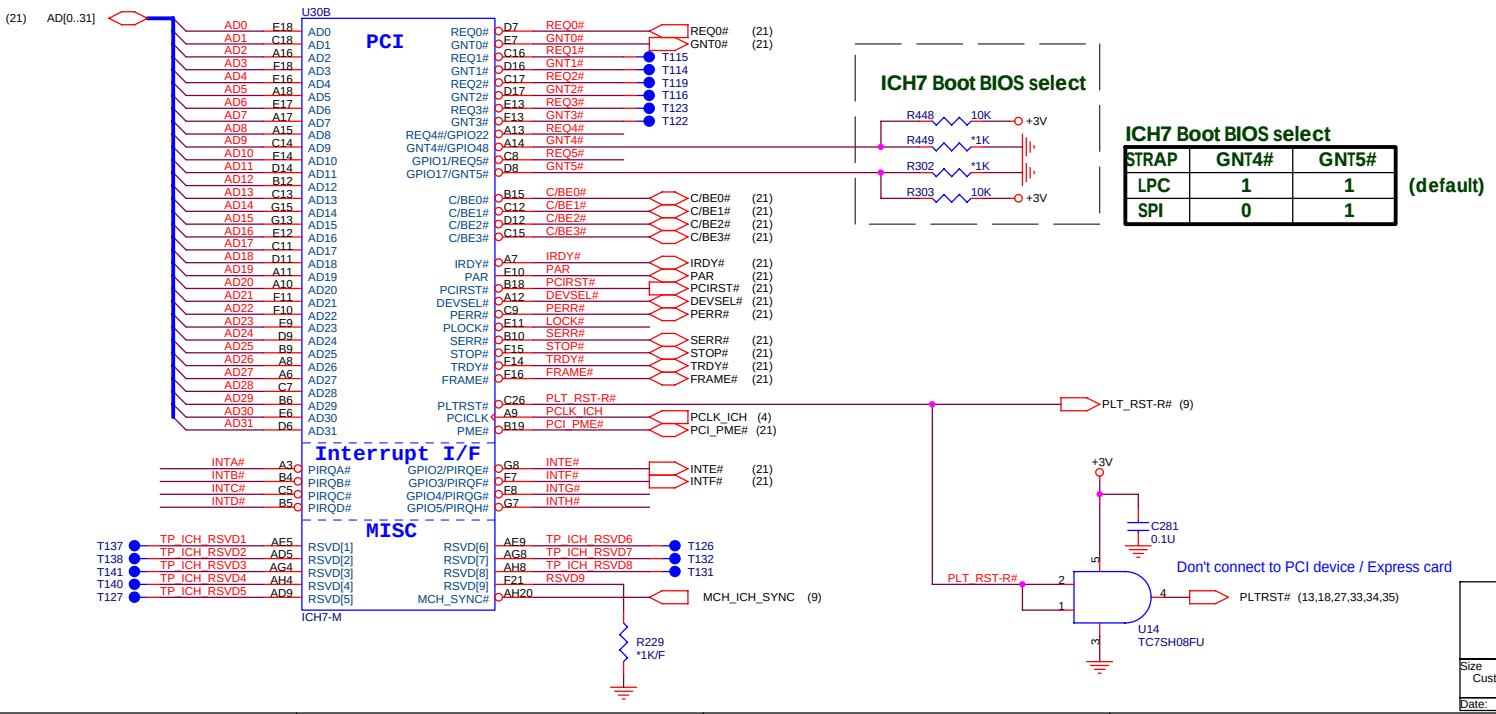
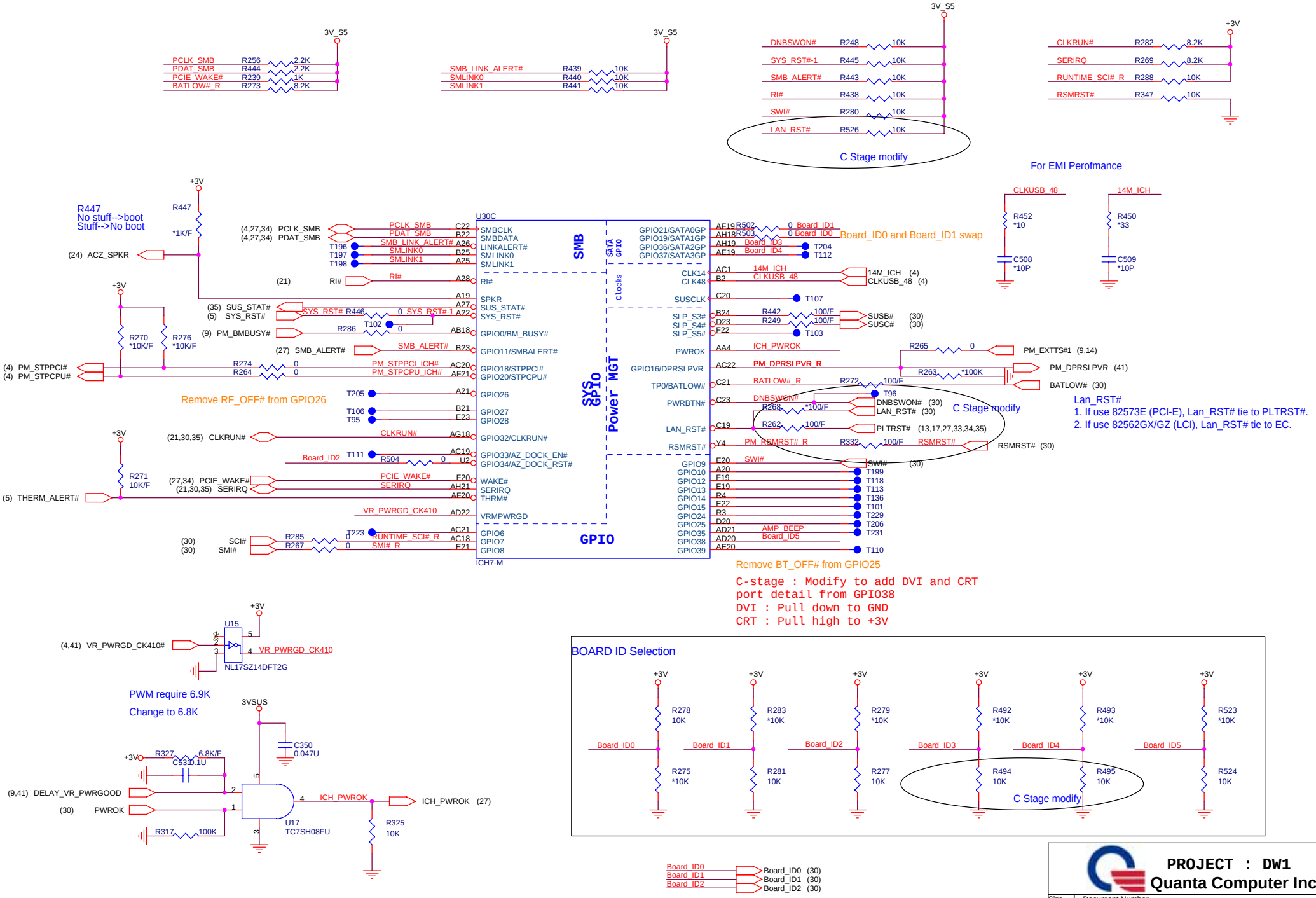
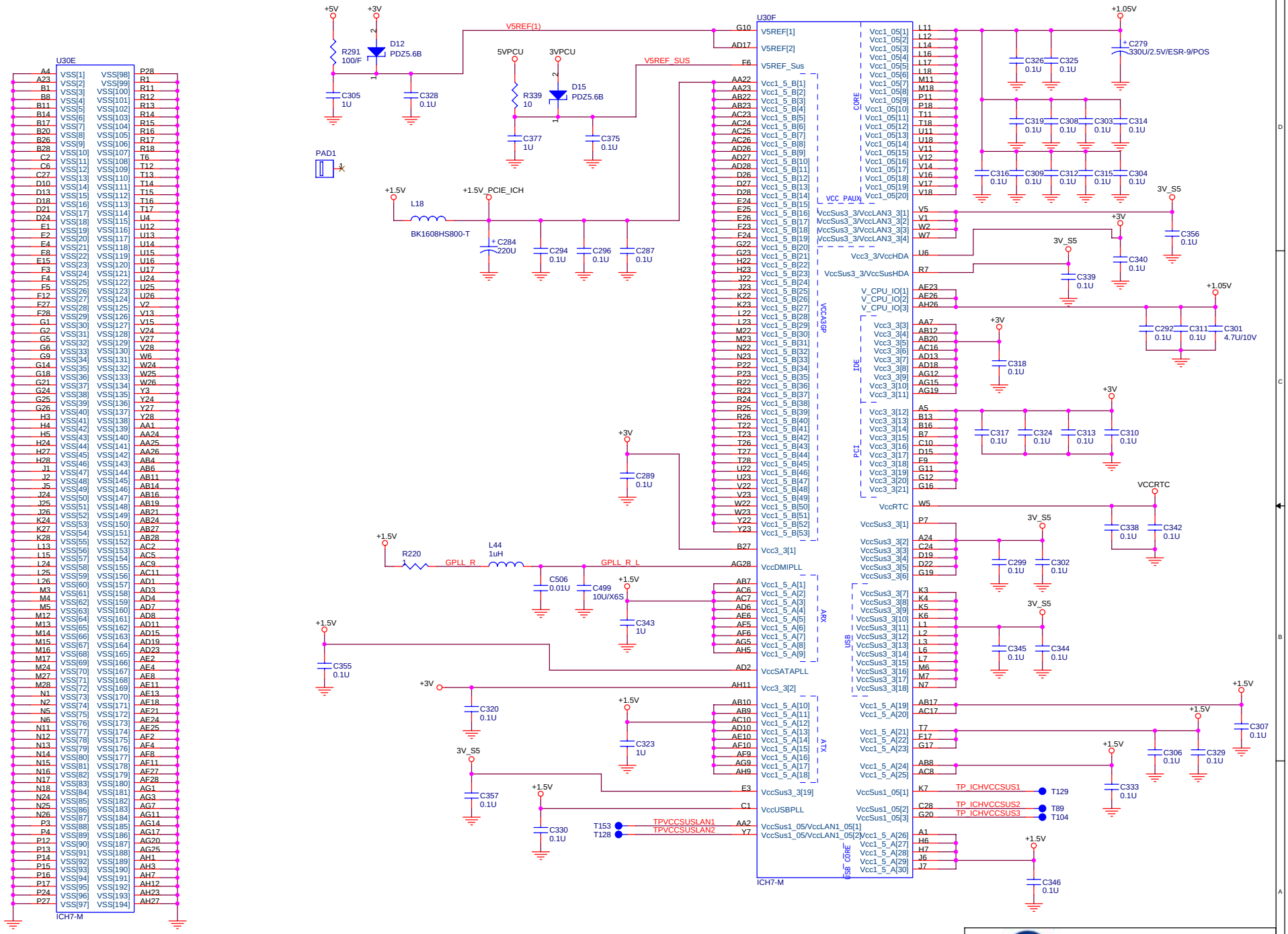

RTC
VCCRTC
3VPCU
C347 1U/16V
D14 CH500H-40
R310 20K
G1 Place under Mini-card or Dram door
CKL:C1/C2: 18pF -> CL:12.5pF
C1/C: 10pF -> CL Value = 8.5pF
VCCRTC_5
D13 CH500H-40
R290 1K
R304 1M
C376 1U/16V
G1 SHORT_ PAD1
C367 18P
CLK_32KX1
Y6 32.768KHZ
R328 10M
C372 18P
CLK_32KX2
VCCRTC_4
BT1 BAT_CONN
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
5VPCU
R311 *1.2K
VCCRTC_1
R305 *1K
VCCRTC_3
Q17 *MMBT3904
R312 *4.7K
VCCRTC_2
R306 *15K
U30A
RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
LAN_EEP_CS
LAN_EEP_SK
LAN_EEP_DOUT
LAN_EEP_DIN
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_JCLK
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
LAN
CPU
BIT_CLK
SYNC
AC_RESET#
SDDATA_IN
SDATA_OUT
ACZ_BCLK
ACZ_SYNC
ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
AC-97/AZALIA
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
SATA
IDE
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
ICH7-M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
To confirm what stepping will support?
+1.05V
+3V
R251 *56/F
R254 *56/F
R243 56/F
R240 56/F
R241 24.9/F
RCIN# R260 10K
GATEA20 R259 10K
PDIORDY R287 4.7K
IRQ14 R289 8.2K
H_CPUSLP#
H_DPRSTP# R
H_DPSLP# R
H_FERR#
H_PWRGD_R
H_IGNNE#
H_INIT#
H_INTR
H_NMI
H_SMI# R
H_STPCLK#
H_THERMTRIP_R
ICH_DPRSTP#
H_DPSLP#
PM_THRMTRIP#
Should be 2" close ICH7
PDD[0..15]
PDA[0..2]
PDCS1#
PDCS3#
C382 *10P
C383 *10P
C381 *10P
C507 *10P
R333 39
R335 39
R334 39
R284 10K
C277 3900P
C278 3900P
C354 3900P
C353 3900P
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
CLK_PCIE_SATA#
CLK_PCIE_SATA
R292 24.9/F
SATA_BIAS
Place within 500 mils of ICH7
ICH7 internal VR enable strap
STATUS | INTVRMEN
Enable (default) | 1
Disable | 0
R315 332K/F
R314 *0
Populate for 82562GX/GZ
U31
93C46-3GR
R338 *3.6K
LANVCC
R346 *0
C389 0.1U
GND
3V_S5
R236 *1K
R238 10K
Q16 *MMBT3904
THERM_CPUDIE_L#
R237 0
THERM_CPUDIE#
PROJECT : DW1
Quanta Computer Inc.
Size Custom
Document Number ICH7-M HOST (1 OF 4)
Rev 1A
Date: Friday, February 10, 2006
Sheet 16 of 42

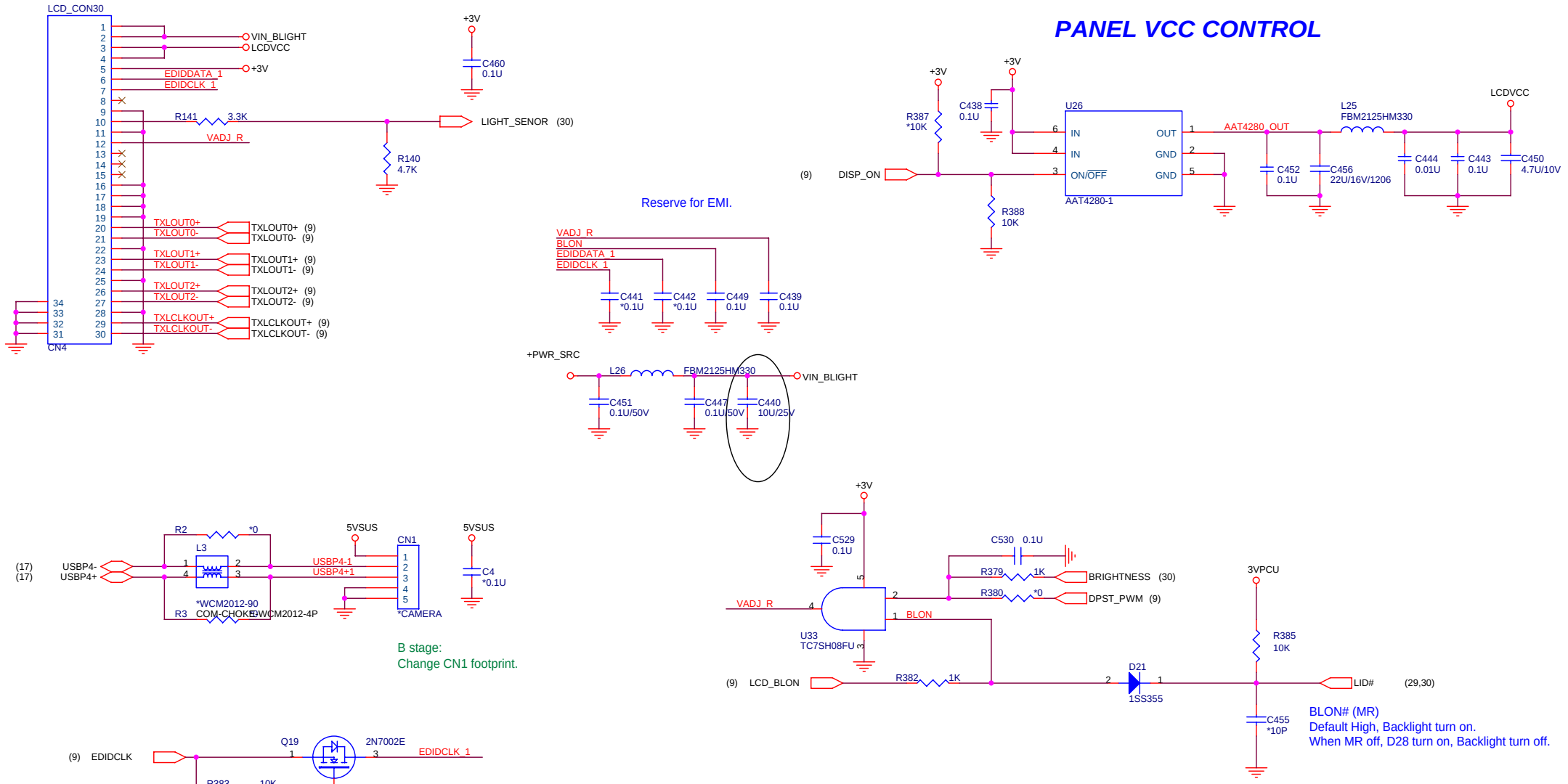




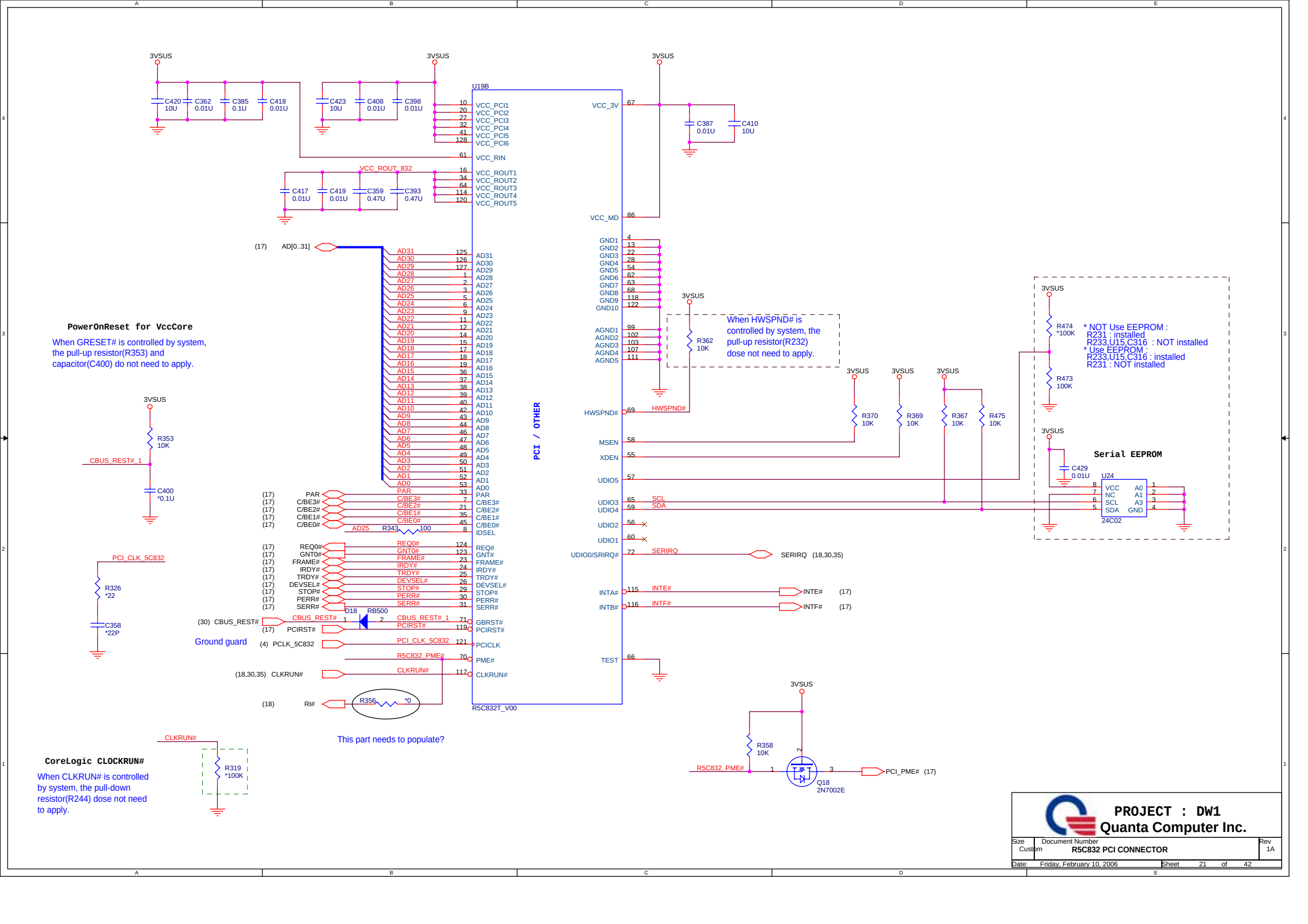
STRAP	GNT4#	GNT5#	
LPC	1	1	(default)
SPI	0	1	

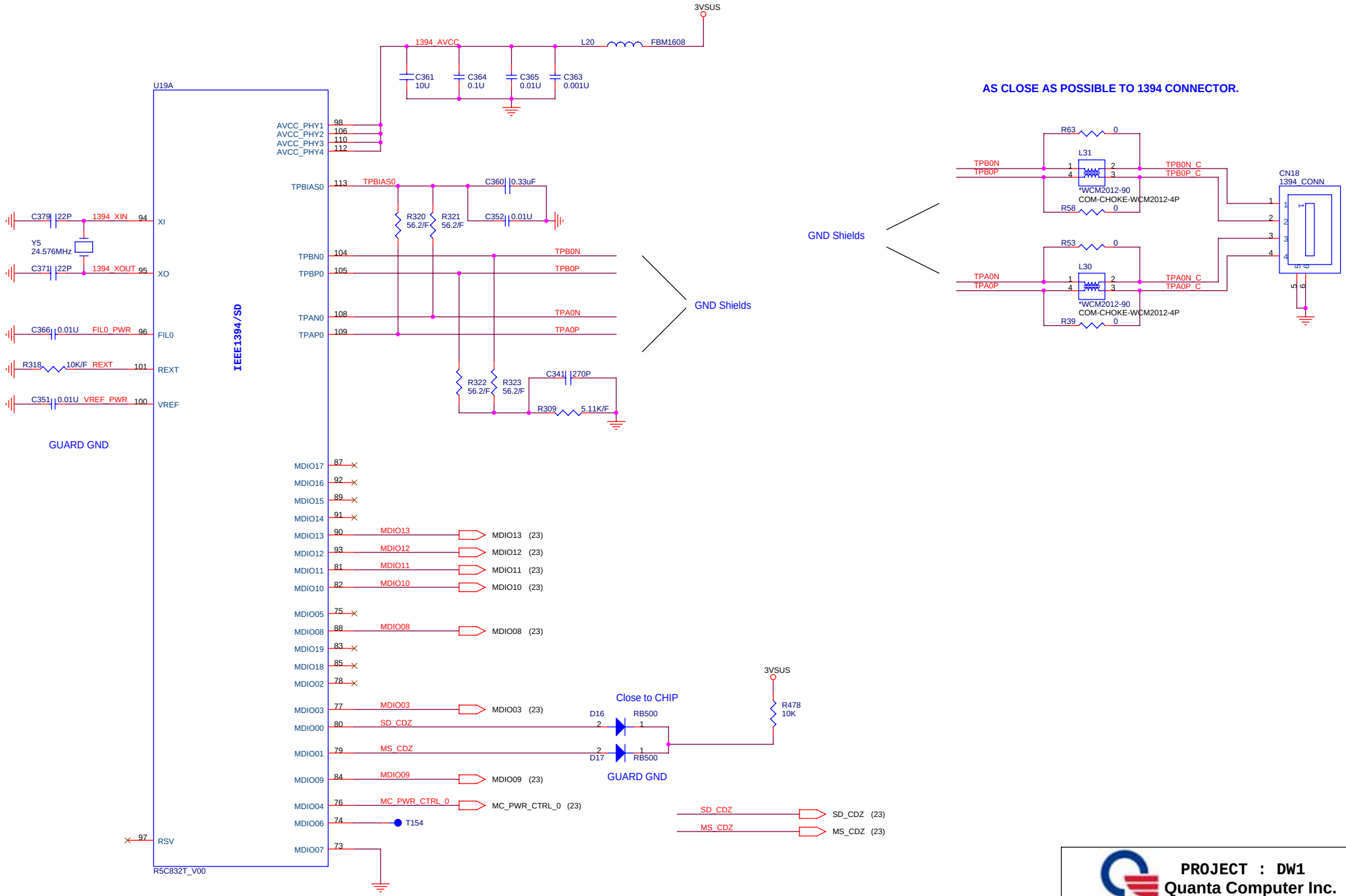

3V_S5
PCLK_SMB R256 2.2K
PDAT_SMB R444 2.2K
PCIE_WAKE# R239 1K
BATLOW#_R R273 8.2K
SMB_LINK_ALERT# R439 10K
SMLINK0 R440 10K
SMLINK1 R441 10K
DNBSWON# R248 10K
SYS_RST#-1 R445 10K
SMB_ALERT# R443 10K
RI# R438 10K
SWI# R280 10K
LAN_RST# R526 10K
C Stage modify
+3V
CLKRUN# R282 8.2K
SERIRQ R269 8.2K
RUNTIME_SCI#_R R288 10K
RSMRST# R347 10K
For EMI Perofmance
R447
No stuff-->boot
Stuff-->No boot
*1K/F
(24) ACZ_SPKR
U30C
SMB
SATA GPIO
Clocks
SYS PWR MGT
GPIO
ICH7-M
SMBCLK
SMBDATA
LINKALERT#
SMLINK0
SMLINK1
RI#
SPKR
SUS_STAT#
SYS_RST#
GPIO0/BM_BUSY#
GPIO11/SMBALERT#
GPIO18/STPPCI#
GPIO20/STPCPU#
GPIO26
GPIO27
GPIO28
GPIO32/CLKRUN#
GPIO33/AZ_DOCK_EN#
GPIO34/AZ_DOCK_RST#
WAKE#
SERIRQ
THRM#
VRMPWRGD
GPIO6
GPIO7
GPIO8
GPIO21/SATA0GP
GPIO19/SATA1GP
GPIO36/SATA2GP
GPIO37/SATA3GP
CLK14
CLK48
SUSCLK
SLP_S3#
SLP_S4#
SLP_S5#
PWROK
GPIO16/DPRSLPVR
TP0/BATLOW#
PWRBTN#
LAN_RST#
RSMRST#
GPIO9
GPIO10
GPIO12
GPIO13
GPIO14
GPIO15
GPIO24
GPIO25
GPIO35
GPIO38
GPIO39
Board_ID0 and Board_ID1 swap
14M_ICH
CLKUSB_48
Remove RF_OFF# from GPIO26
Remove BT_OFF# from GPIO25
C-stage : Modify to add DVI and CRT
port detail from GPIO38
DVI : Pull down to GND
CRT : Pull high to +3V
Lan_RST#
1. If use 82573E (PCI-E), Lan_RST# tie to PLTRST#.
2. If use 82562GX/GZ (LCI), Lan_RST# tie to EC.
BOARD ID Selection
Board_ID0
Board_ID1
Board_ID2
Board_ID3
Board_ID4
Board_ID5
C Stage modify
PWM require 6.9K
Change to 6.8K
U15
NL17SZ14DFT2G
U17
TC7SH08FU
3VSUS
PROJECT : DW1
Quanta Computer Inc.
ICH7-M GPIO (3 OF 4)
Size Custom
Rev 1A
Date: Friday, February 10, 2006
Sheet 18 of 42


U30E
ICH7-M
U30F
ICH7-M
PROJECT : DW1
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
Size Custom
Document Number
Rev 1A
Date: Friday, February 10, 2006
Sheet 19 of 42



PROJECT : DW1		
Quanta Computer Inc.		
Size B	Document Number LCD CONN	Rev 1A
Date: Friday, February 10, 2006	Sheet 20 of 42	

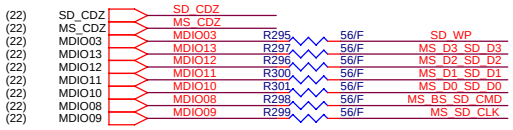

U19B
PCI / OTHER
R5C832T_V00
3VSUS
C420 10U
C362 0.01U
C385 0.1U
C418 0.01U
C423 10U
C408 0.01U
C398 0.01U
VCC_PCI1
VCC_PCI2
VCC_PCI3
VCC_PCI4
VCC_PCI5
VCC_PCI6
VCC_RIN
VCC_ROUT_832
C417 0.01U
C419 0.01U
C359 0.47U
C393 0.47U
VCC_ROUT1
VCC_ROUT2
VCC_ROUT3
VCC_ROUT4
VCC_ROUT5
VCC_3V
C387 0.01U
C410 10U
VCC_MD
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
AGND1
AGND2
AGND3
AGND4
AGND5
R362 10K
When HWSPND# is controlled by system, the pull-up resistor(R232) dose not need to apply.
HWSPND#
MSEN
XDEN
UDIO5
UDIO3
UDIO4
UDIO2
UDIO1
UDIO0/SRIRQ#
SERIRQ (18,30,35)
INTA#
INTB#
INTE# (17)
INTF# (17)
TEST
R370 10K
R369 10K
R367 10K
R475 10K
(17) AD[0..31]
AD31
AD30
AD29
AD28
AD27
AD26
AD25
AD24
AD23
AD22
AD21
AD20
AD19
AD18
AD17
AD16
AD15
AD14
AD13
AD12
AD11
AD10
AD9
AD8
AD7
AD6
AD5
AD4
AD3
AD2
AD1
AD0
PAR
C/BE3#
C/BE2#
C/BE1#
C/BE0#
IDSEL
REQ#
GNT#
FRAME#
IRDY#
TRDY#
DEVSEL#
STOP#
PERR#
SERR#
GBRST#
PCIRST#
PCICLK
PME#
CLKRUN#
PowerOnReset for VccCore
When GRESET# is controlled by system, the pull-up resistor(R353) and capacitor(C400) do not need to apply.
R353 10K
CBUS_REST# 1
C400 *0.1U
PCI_CLK_5C832
R326 *22
C358 *22P
Ground guard
(30) CBUS_REST#
(17) PCIRST#
(4) PCLK_5C832
(18,30,35) CLKRUN#
(18) RI#
D18 RB500
R343 100
R356 *0
This part needs to populate?
CoreLogic CLOCKRUN#
When CLKRUN# is controlled by system, the pull-down resistor(R244) dose not need to apply.
R319 *100K
R358 10K
R5C832_PME#
Q18 2N7002E
PCI_PME# (17)
R474 *100K
R473 100K
* NOT Use EEPROM :
R231 : installed
R233,U15,C316 : NOT installed
* Use EEPROM :
R233,U15,C316 : installed
R231 : NOT installed
Serial EEPROM
C429 0.01U
U24
VCC
NC
SCL
SDA
A0
A1
A3
GND
24C02
PROJECT : DW1
Quanta Computer Inc.
Size Custom
Document Number
R5C832 PCI CONNECTOR
Rev 1A
Date: Friday, February 10, 2006
Sheet 21 of 42

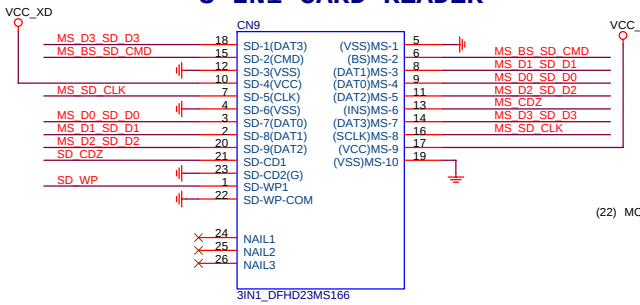


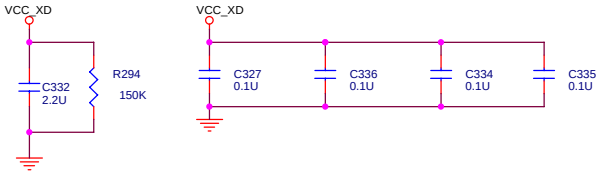
PROJECT : DW1
Quanta Computer Inc.

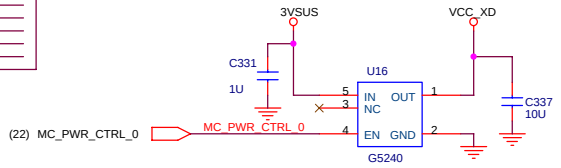
Size	Document Number	Rev
Custom	IEEE1394	1A
Date: Friday, February 10, 2006	Sheet 22 of 42	

3 IN1 CARD READER

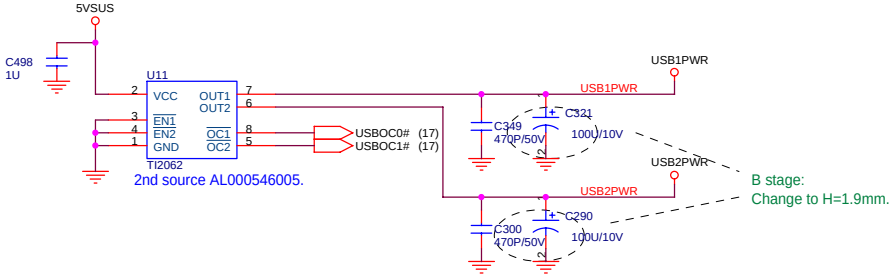






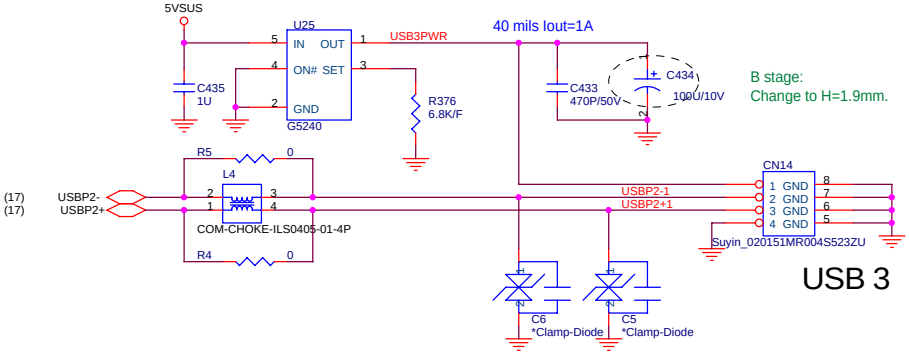


Memory Card Power Supply

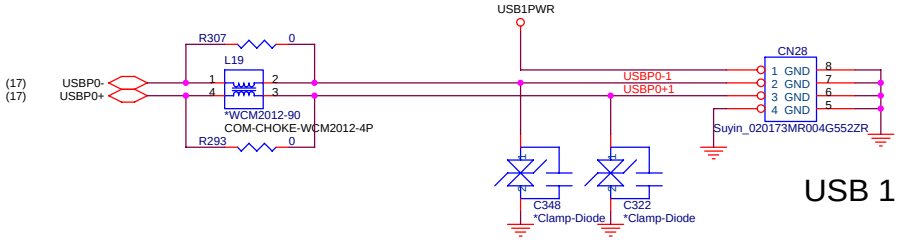


2nd source AL000546005.

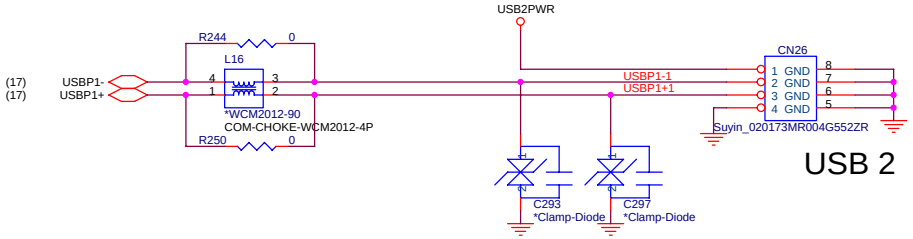
B stage:
Change to H=1.9mm.



USB 3



USB 1



USB 2

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CARD READER CONN,USB x 3	1A
Date: Friday, February 10, 2006	Sheet 23 of 42	

C-stage : Modify for WOR
change from +3V to 3VSUS

3VSUS
L23
BLM11A601S
C399 10U/10V
C391 0.1U
C388 0.1U
3V_DVDD
AVDD
C412 0.1U
C513 0.1U
C517 0.1U
C514 10U/10V
AGND
U20
GMT_G910T21U
Vout
Vin
GND
AGND
5V_AVDD
C396 0.1U
C397 0.047U
C394 1U
L22
BLM11A601S
+5V
C386 0.1U
C390 10U/10V

BIT_CLK
R455 *22
C510 *22P
Reserve for EMI

VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

U22
VDDIO 3
DVDD 8
DVDDM 45
AVDD_20 20
AVDD_31 31
AVDDHP 37

(16) AC_RESET# — AC_RESET# — 10 RESET#
(16) BIT_CLK — BIT_CLK R457 33 BITCLK — 5 BIT_CLK
(16) SYNC — SYNC — 9 SYNC
(16) SDDATA_IN — SDDATA_IN R348 33 SDI — 7 SDI
(16) SDATA_OUT — SDATA_OUT — 4 SDO

For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

(26) DIBP_HS — DIBP_HS R355 0 DIBP — 44 DIBP
(26) DIBN_HS — DIBN_HS R354 0 DIBN — 43 DIBN
(18) ACZ_SPKR — ACZ_SPKR C392 0.1U PCBEEP — 11 PCBEEP
(25) SPDIF — SPDIF — 48 SPDIF
T155 — EAPD — 47 EAPD
1 NC_1
2 NC_2
16 NC_16
3V_DVDD — R363 237K/F RCOSC — 41 RCOSC

VSSIO_42 42
VSSIO_46 46
DVSS 6
CX20549-12
AVSS_12 12
AVSS_25 25
AVSS_32 32
AVSSHP 40
AGND

MIC_BIAS_L 29 — INT_MICBIAS_L
MIC_BIAS_R 30 — INT_MICBIAS_R
MIC_L 21 — INT_MIC_L
MIC_R 22 — INT_MIC_R
Internal MIC

LINEOUT_L 35 — LINEOUT_L
LINEOUT_R 36 — LINEOUT_R
LINEOUT_L (25)
LINEOUT_R (25)
Speaker

PORT-A_BIAS_L 33
PORT-A_BIAS_R 34
PORT-A_L 38
PORT-A_R 39

PORT-B_BIAS_L 14 — MICBIAS_B
PORT-B_BIAS_R 15
PORT-B_L 23 — MIC
PORT-B_R 24
MICBIAS_B (25)
MIC (25)
MIC IN

CD_L 17
CD_GND 18
CD_R 19

SENSE 13 — SENSE
R464 5.11K/F
R467 5.11K/F
R461 10K/F
AVDD
SENSE_PORT_A (25)
SENSE_PORT_B (25)

VREF_HI 26
VREF_LO 27
VC_REFA 28 — C516 1U — AGND — C515 1U

R508 0
R465 0
R364 *0
R456 *0
R462 *0
R330 *0
R481 *0
AGND

PAD2
*EMI spring
+3V
C550 *0.1U
C543 *0.1U
C544 *1U
C545 *0.1U
AGND
AVDD

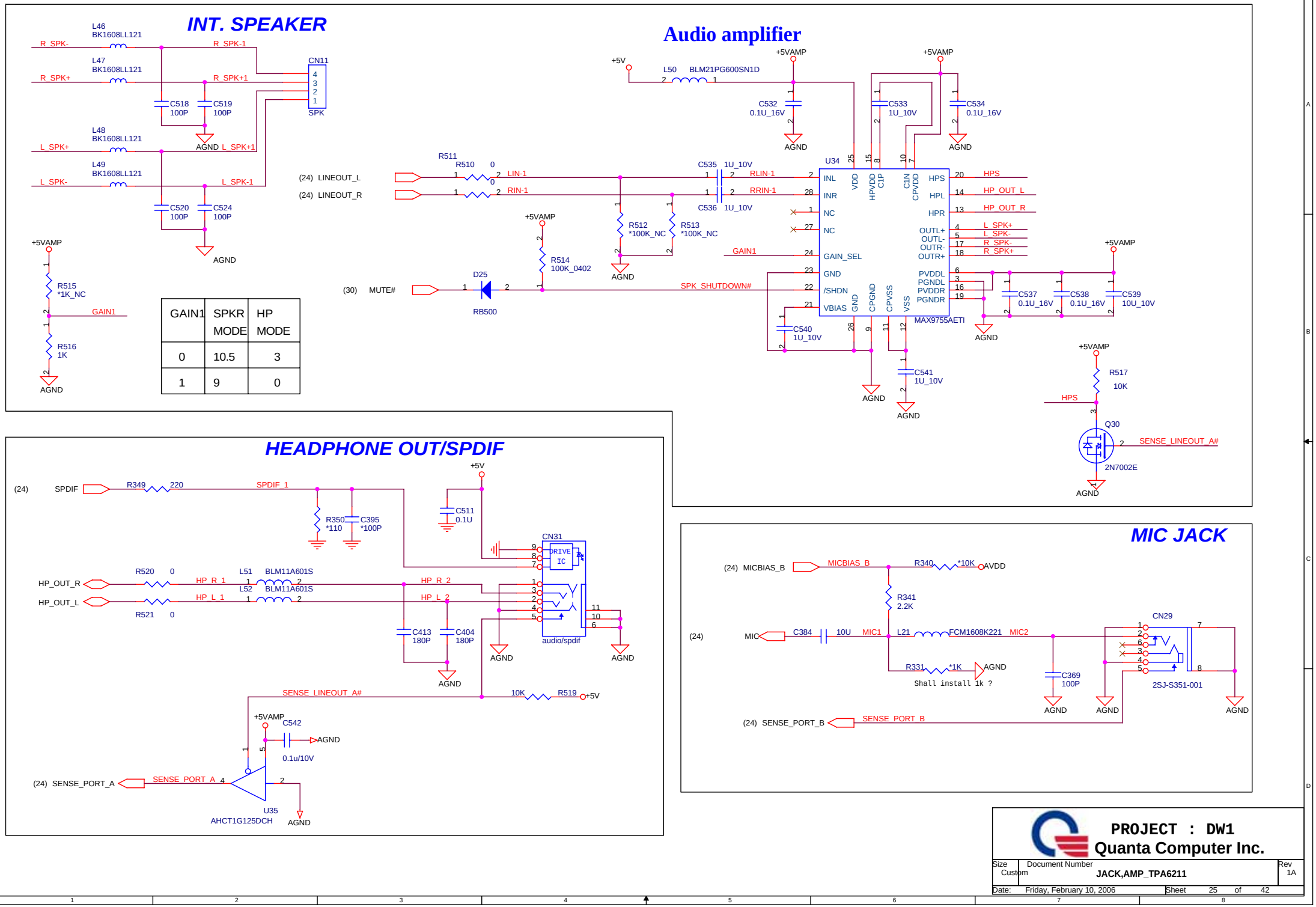
Modify for EMI
C stahge add
for EMI issue

Internal MIC

INT_MICBIAS_R
INT_MICBIAS_L
B stage:
Change CN2 footprint.
R377 2.2K
R378 2.2K
INT_MIC_R — C436 10U — INT_MIC_R_1
INT_MIC_L — C437 10U — INT_MIC_L_1
CN2
1
2
3
4
MIC
AGND

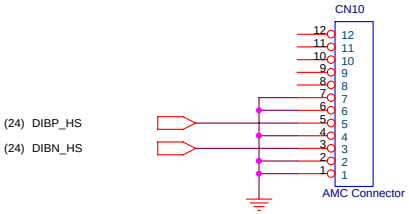
DIGITAL **ANALOG**

Quanta Computer Inc.	PROJECT : DW1	
Size B	Document Number: Azalia CTRL_CONEXANT20549	Rev 1A
Date: Friday, February 10, 2006	Sheet 24 of 42	



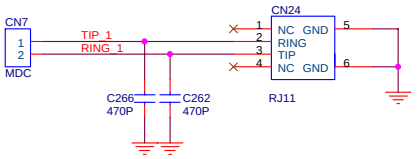
PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	JACK,AMP_TPA6211	1A
Date: Friday, February 10, 2006	Sheet 25 of 42	



RJ11 CONNECTOR

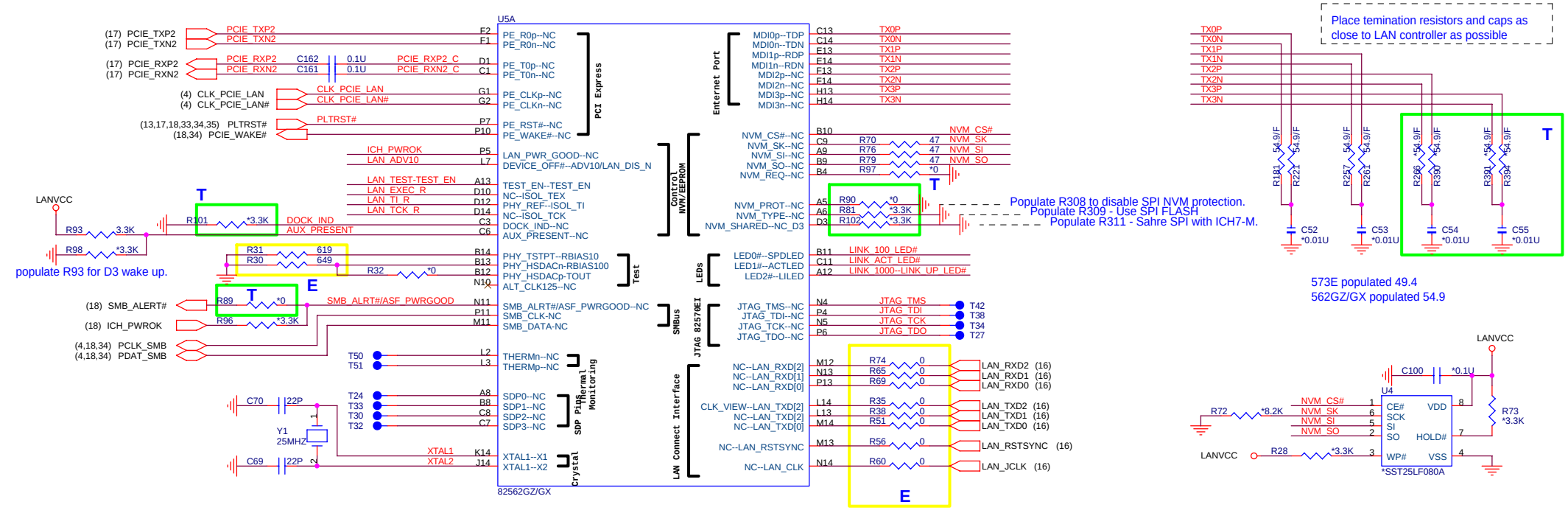
B stage:
Change CN7 footprint.



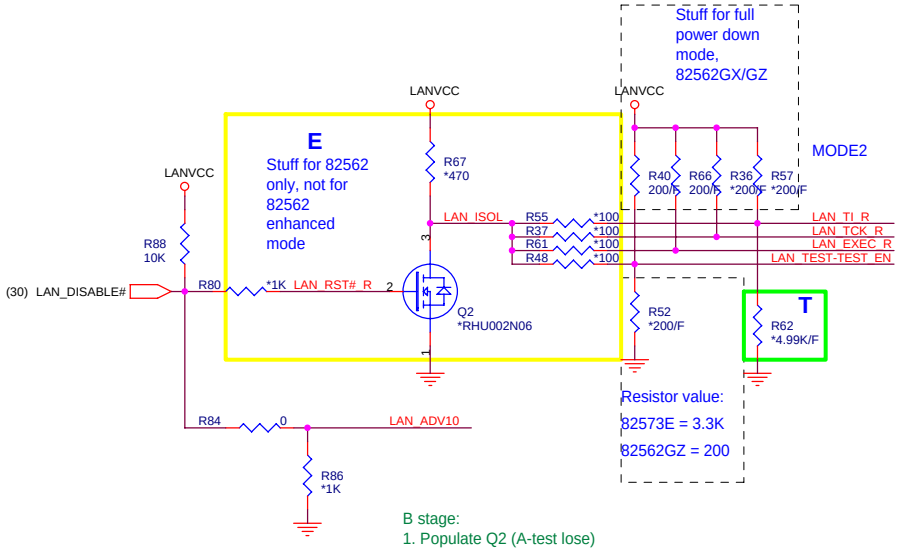
PROJECT : DW1
Quanta Computer Inc.

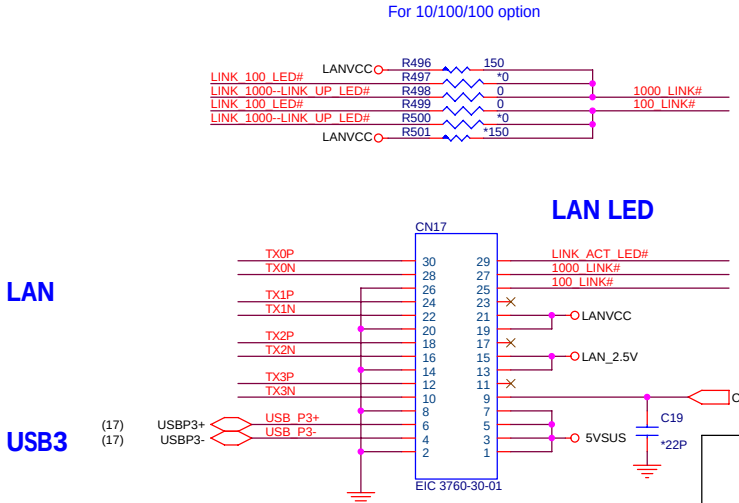
Size	Document Number	Rev
Custom	MODEM (DAA)	1A

Date: Friday, February 10, 2006 Sheet 26 of 42



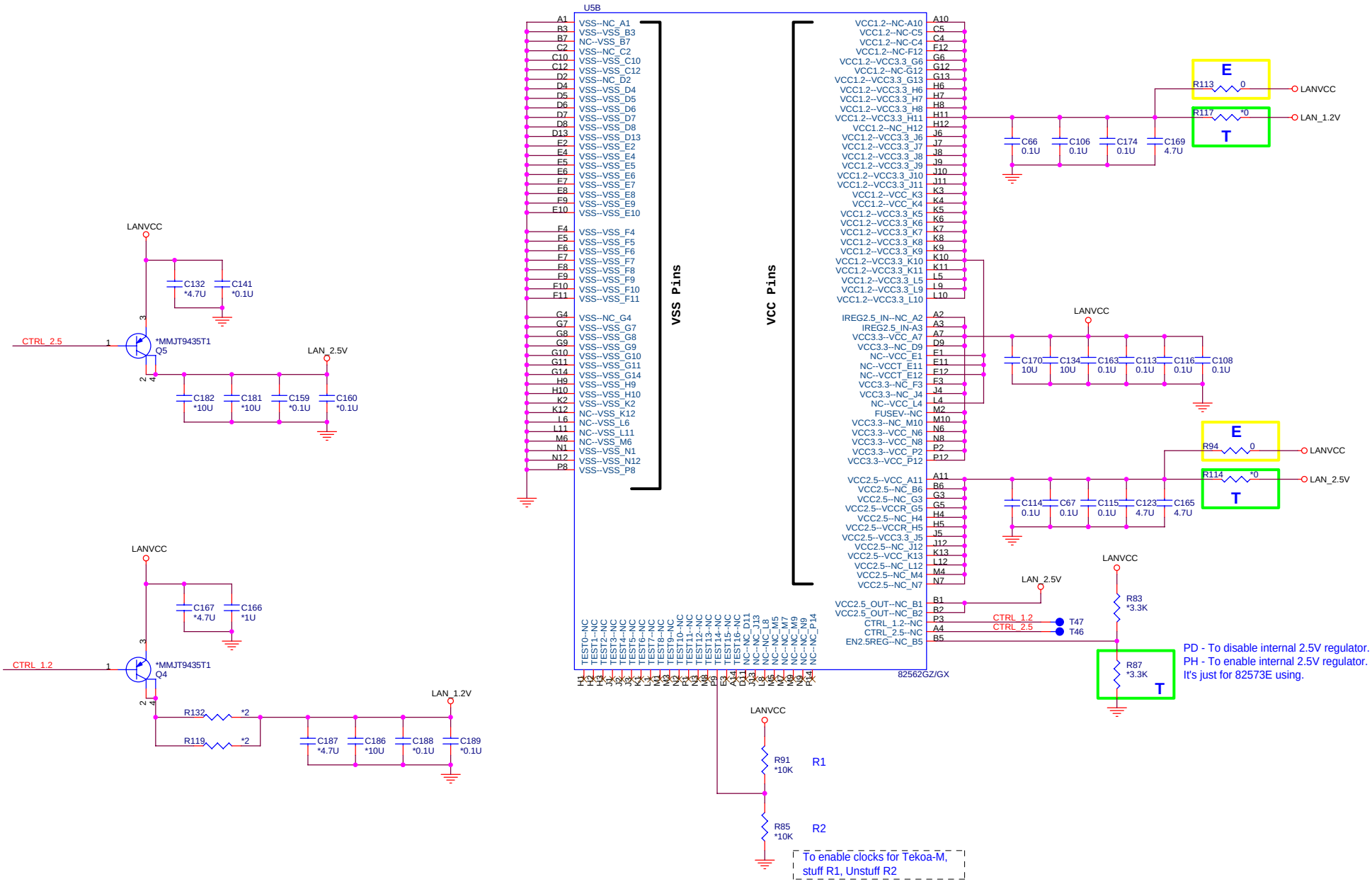
T : Stuffed for 82573E(10/100/1000)
E : Stuffed for 82856GZ/GX(10/100/1000)





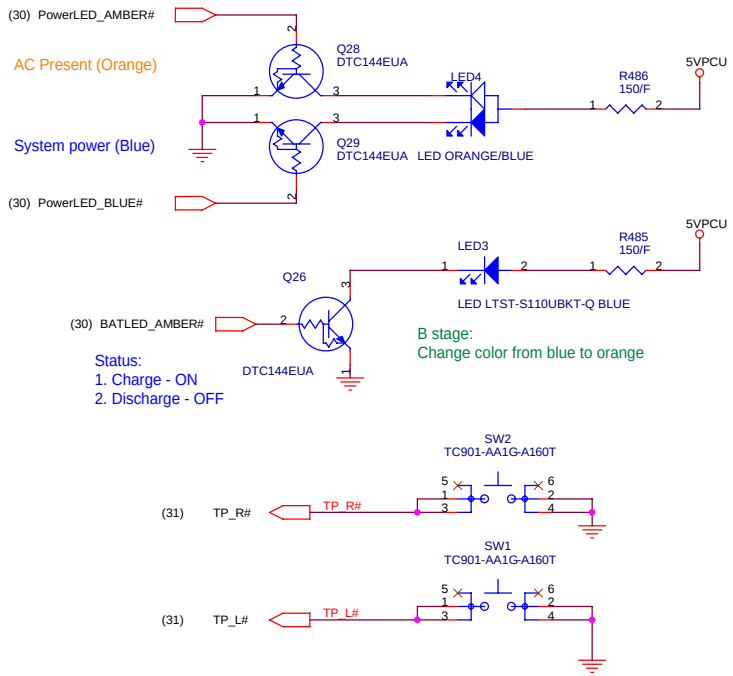
PROJECT : DW1
Quanta Computer Inc.

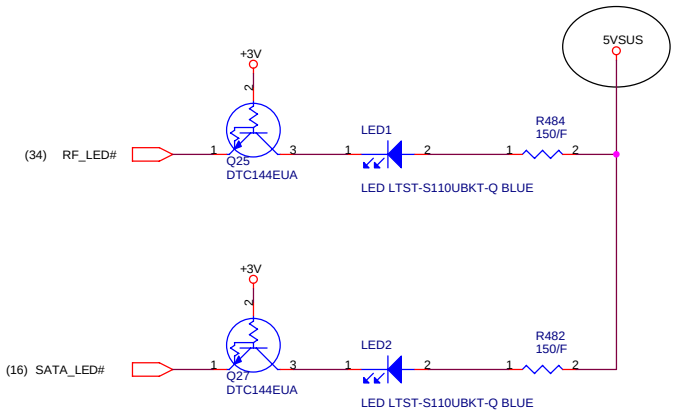
Size	Document Number	Rev
Custom	LAN 82573E/82562GZ	1A
Date: Friday, February 10, 2006	Sheet 27 of 42	

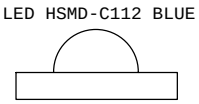


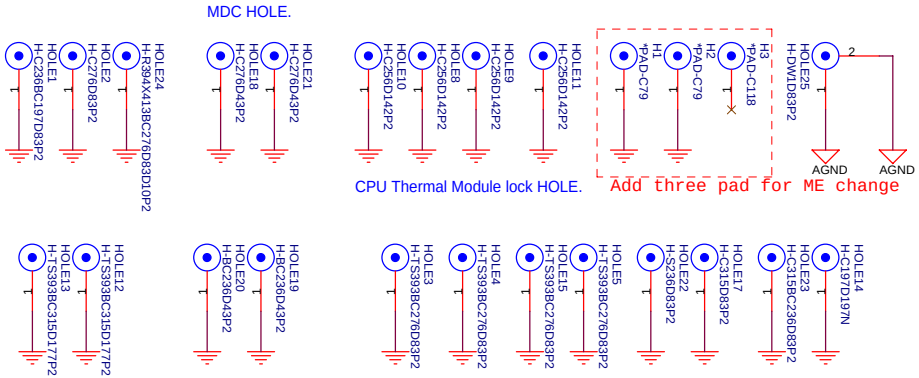
PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	1A
Date: Friday, February 10, 2006	Sheet 28 of 42	

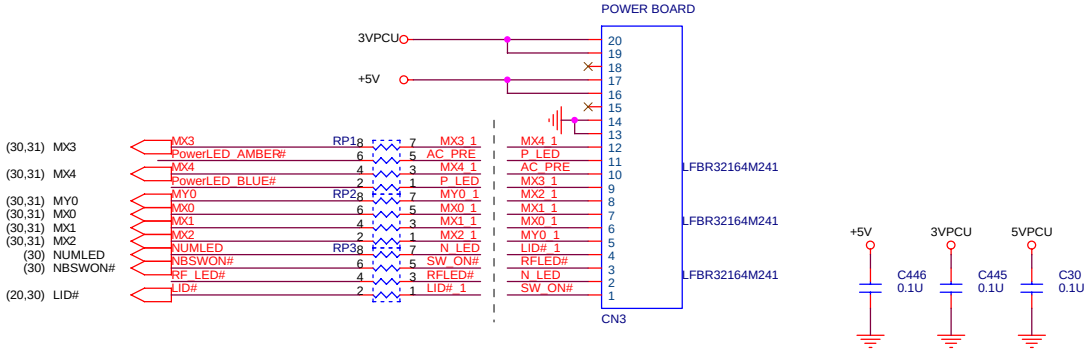








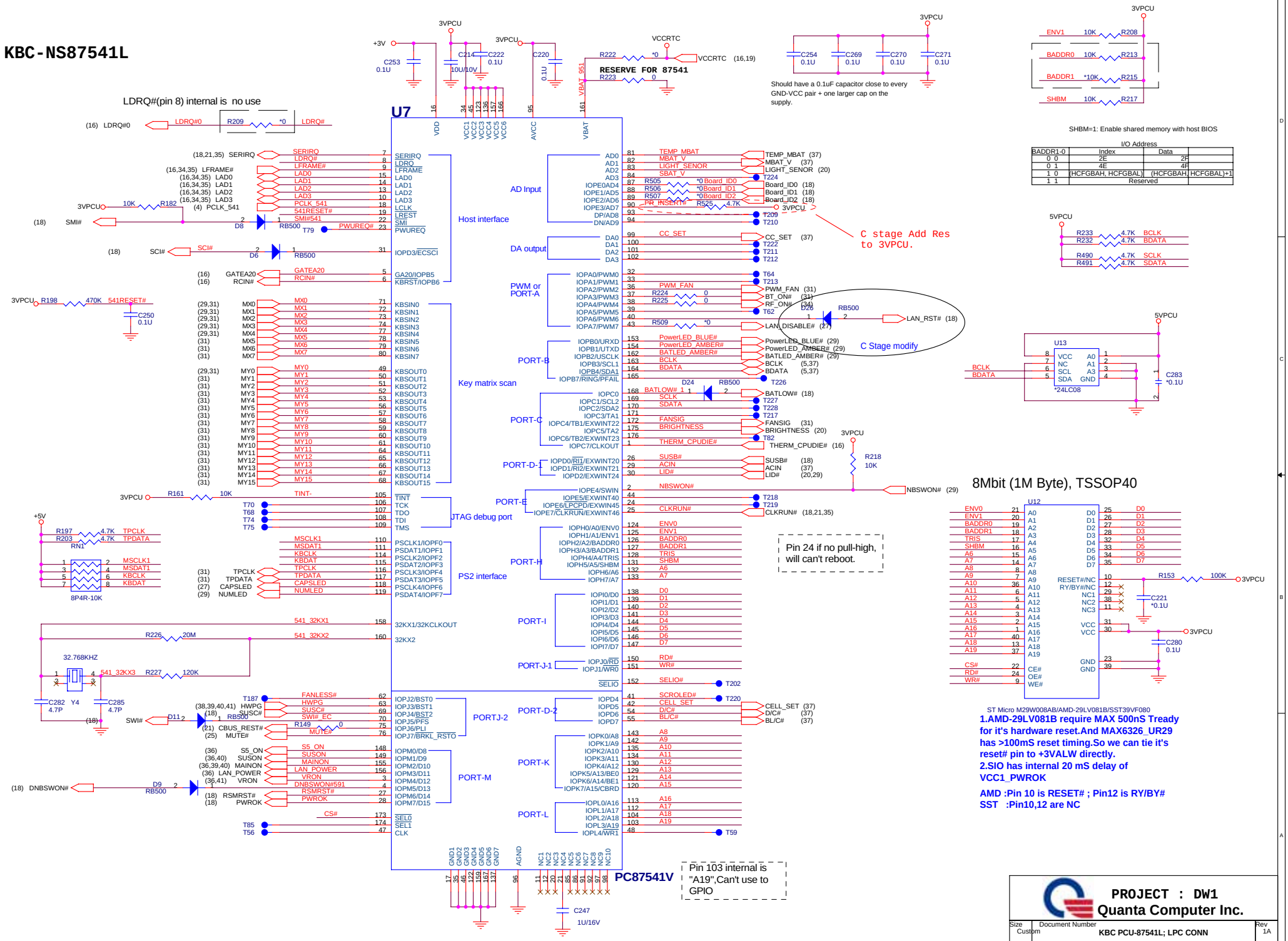
Need to apply Nut part number for Thermal,
MDC and Mini-card module.



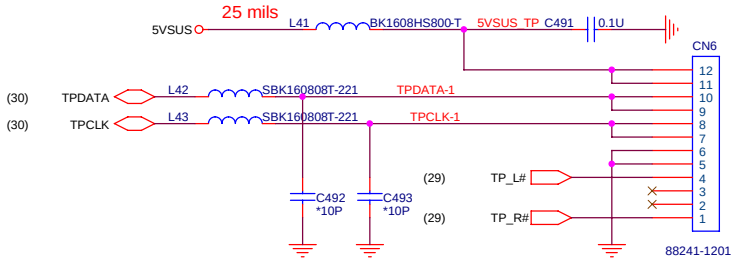
PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LED, Hole, TP SW, SW/B	1A
Date: Friday, February 10, 2006	Sheet 29 of 42	

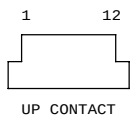
KBC - NS87541L



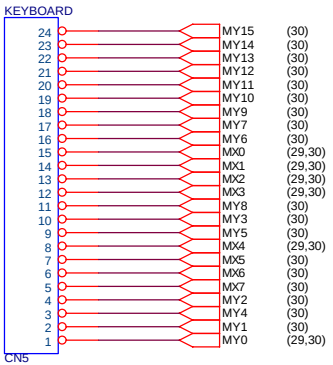
TOUCH PAD CONNECTOR



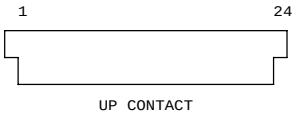
B Stage:
Change to P-TWO DFFC12FR234

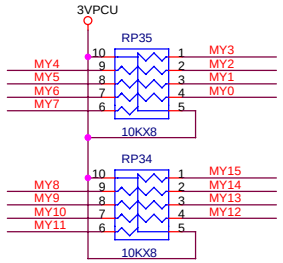


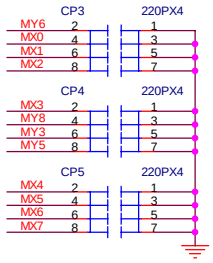
KEYBOARD CONNECTOR

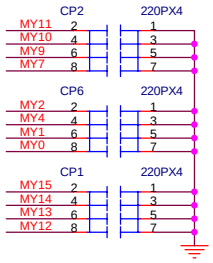


P-TWO
DFHS24FR358

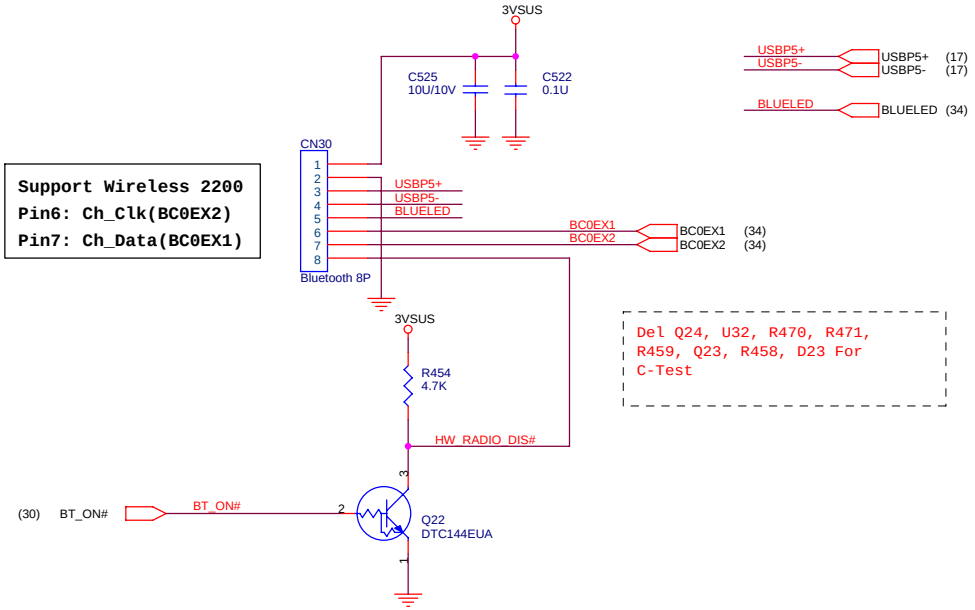








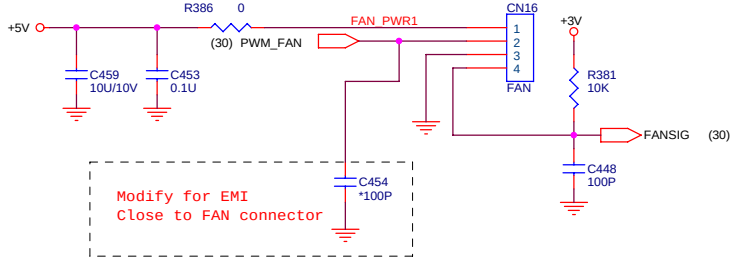
BLUETOOTH



Support Wireless 2200
Pin6: Ch_Clk(BC0EX2)
Pin7: Ch_Data(BC0EX1)

Del Q24, U32, R470, R471,
R459, Q23, R458, D23 For
C-Test

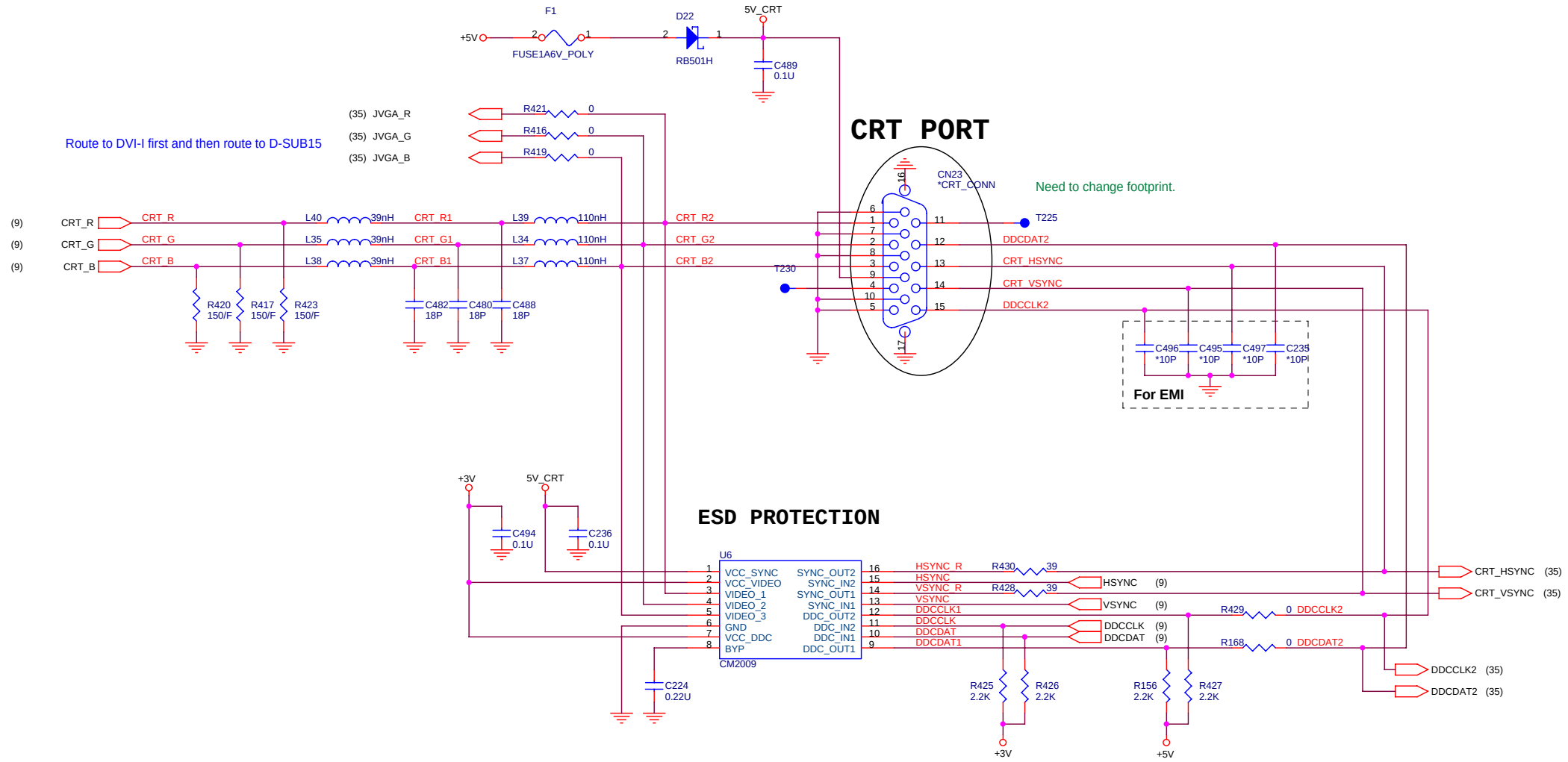
FAN CONTROL



Modify for EMI
Close to FAN connector

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLUETOOTH/TP/KEY/BTB	1A
Date: Friday, February 10, 2006	Sheet 31 of 42	



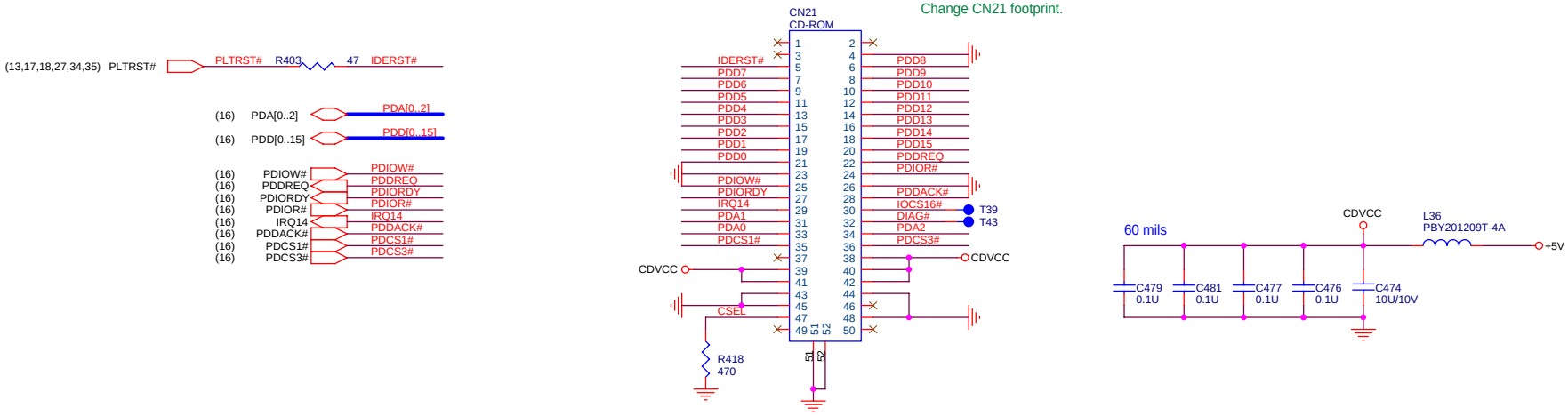
PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
B	CRT, DVI-I	1A

Date: Friday, February 10, 2006 Sheet 32 of 42

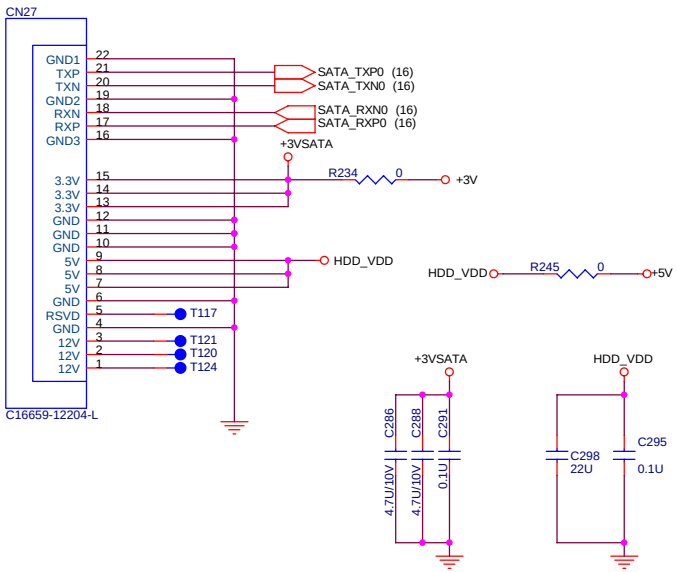
CD-ROM

B stage:
Change CN21 footprint.



SATA CONNECTOR

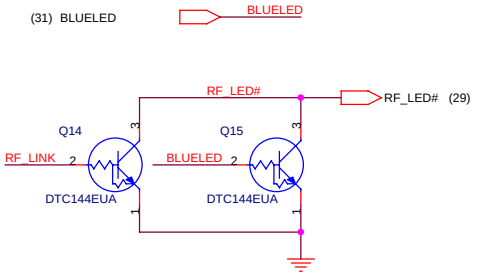
B stage:
Change CN27 net.



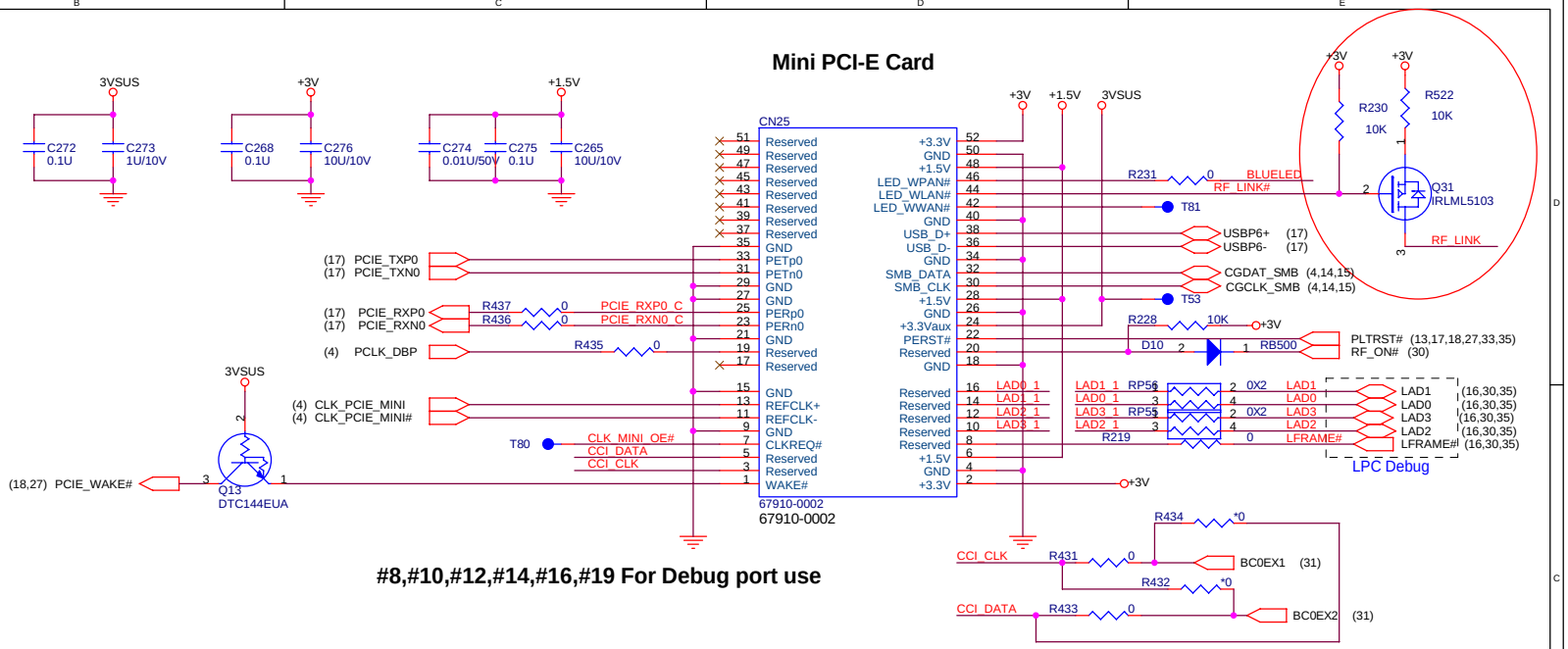
PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD, CD-ROM	1A
Date: Friday, February 10, 2006	Sheet 33 of 42	

RF LED control.

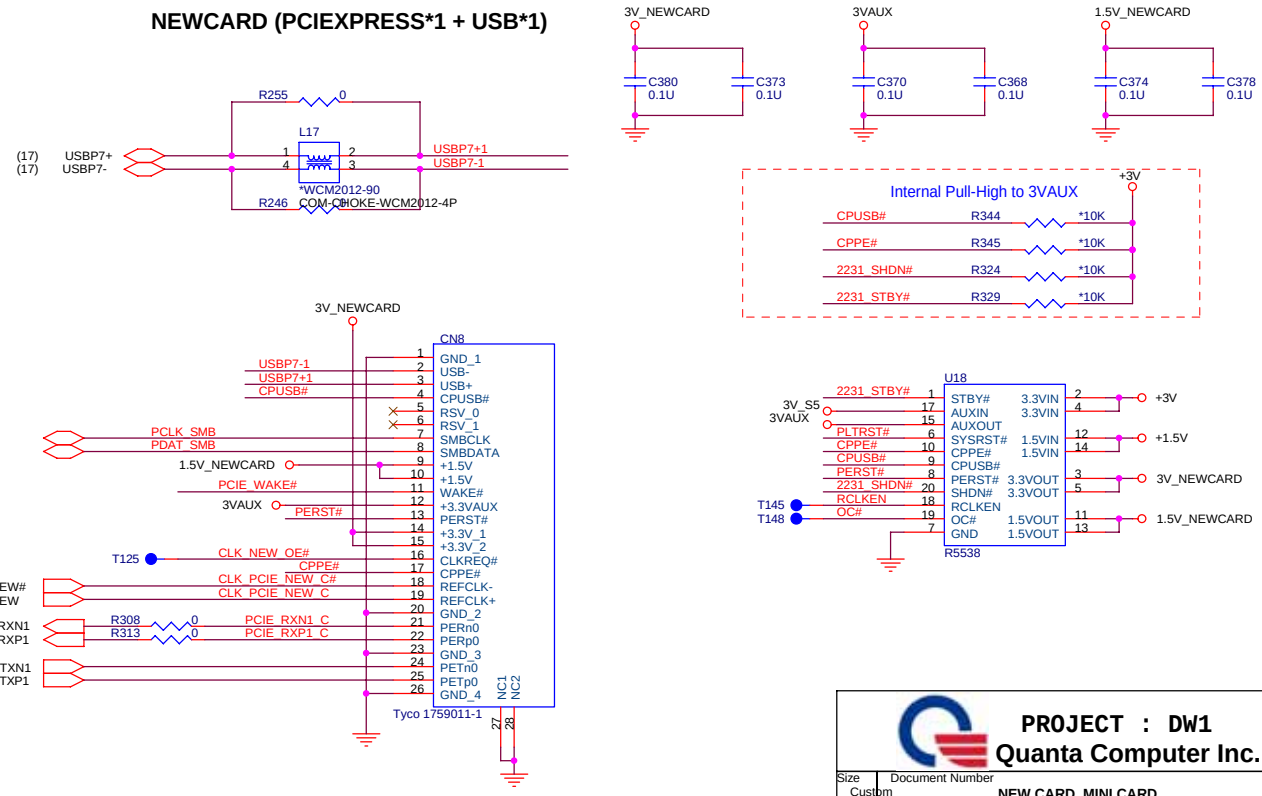


Mini PCI-E Card



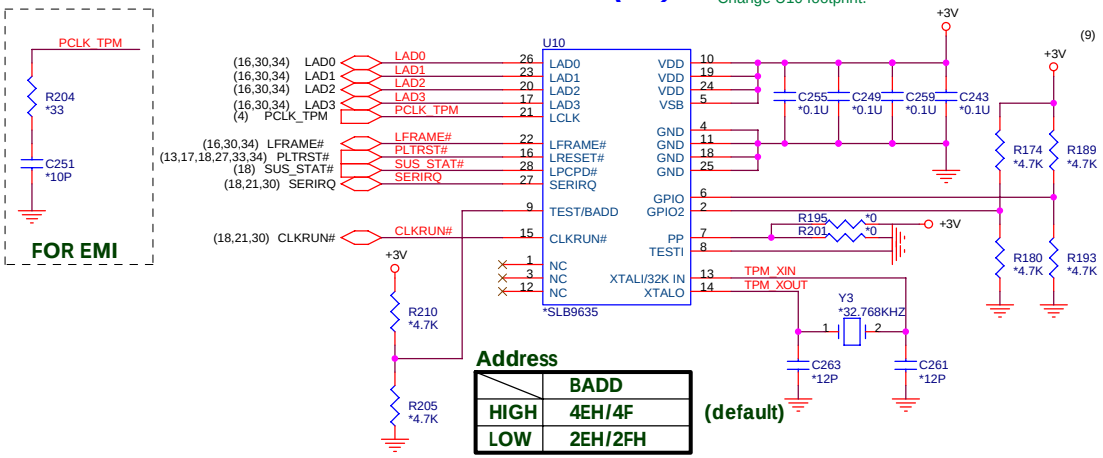
#8,#10,#12,#14,#16,#19 For Debug port use

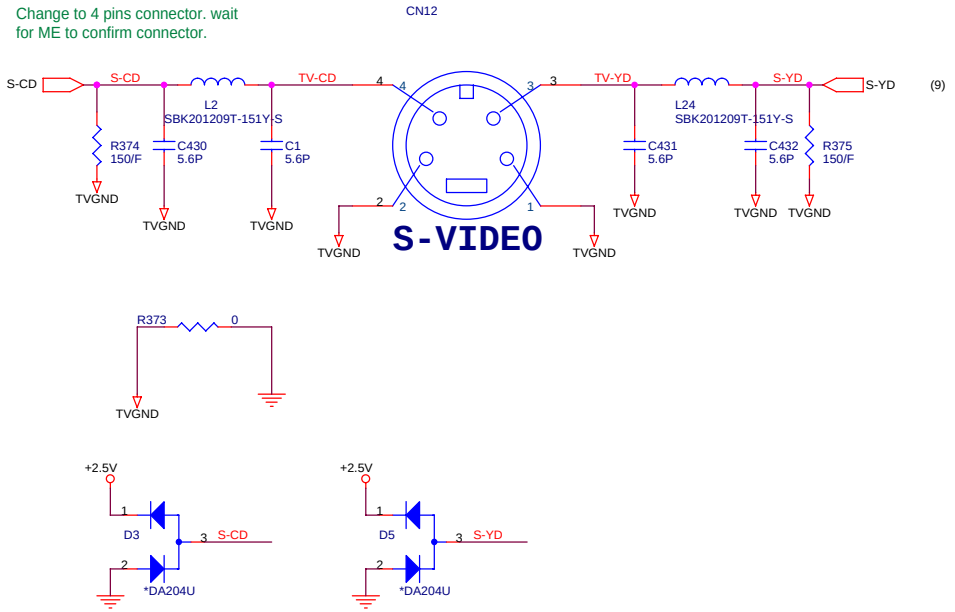
NEWCARD (PCIEXPRESS*1 + USB*1)

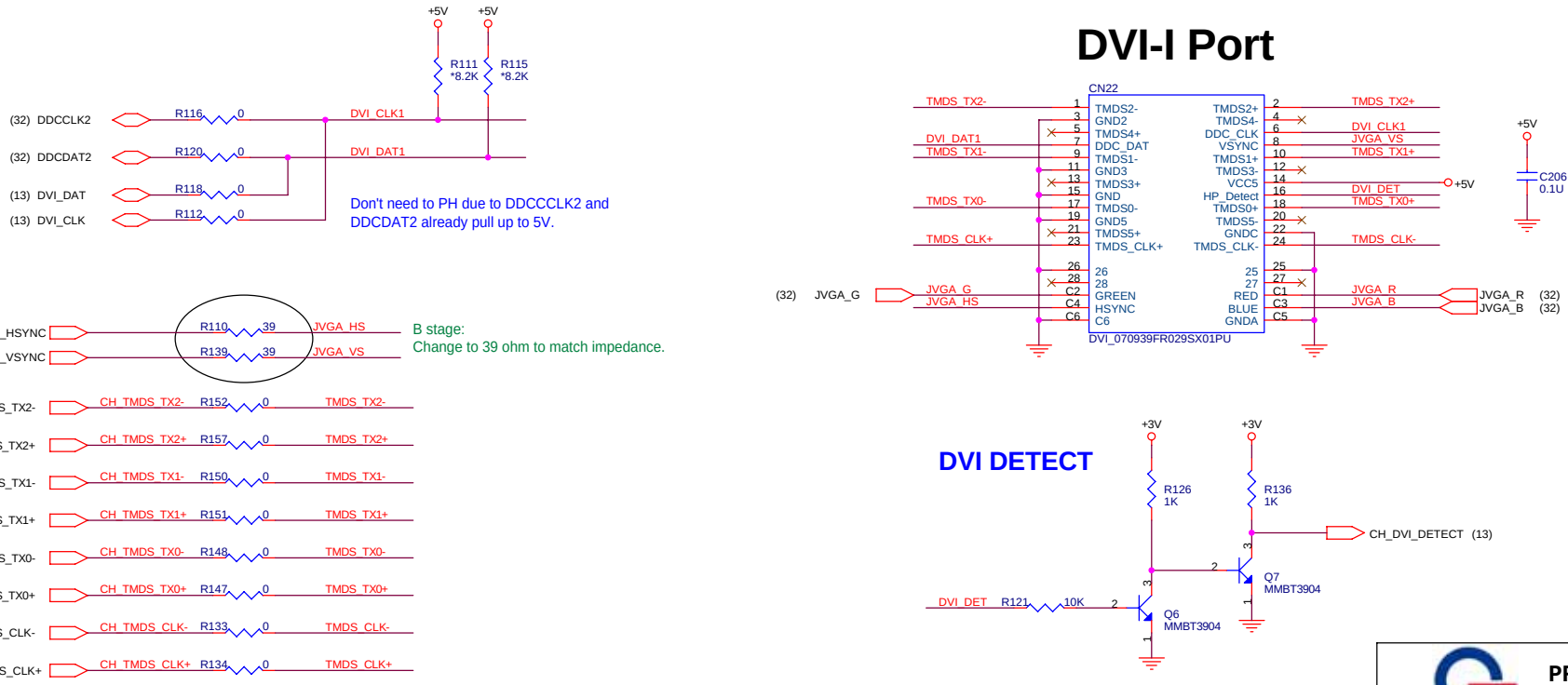


PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD, MINI CARD	1A
Date: Friday, February 10, 2006	Sheet 34 of 42	

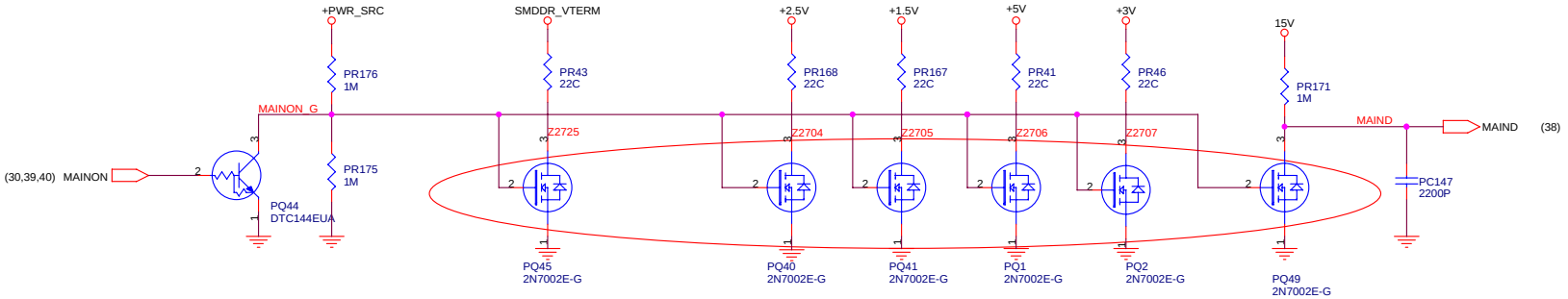






PROJECT : DW1
Quanta Computer Inc.

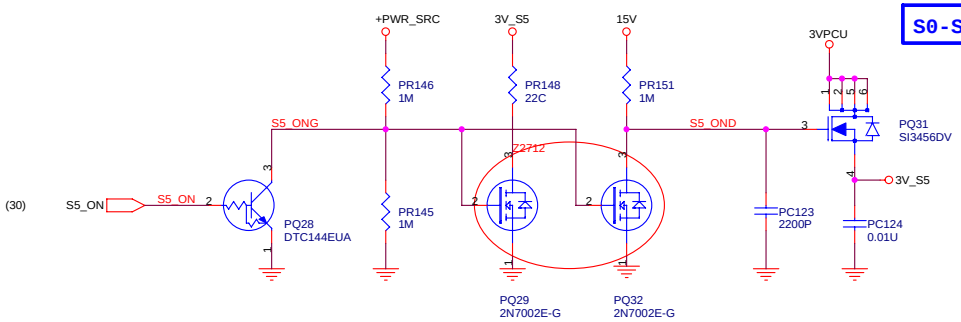
Size	Document Number	Rev
Custom	TPM	1A
Date: Friday, February 10, 2006	Sheet 35 of 42	



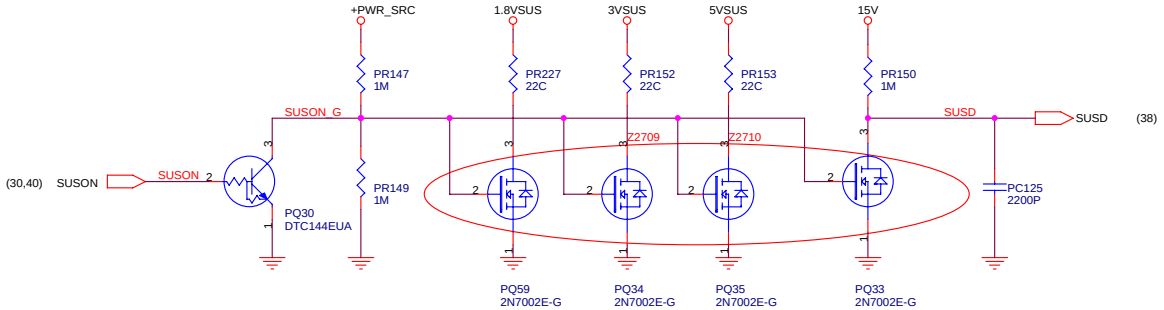
modify from 2N7002E TO 2M7002E-G

3V_S5
72mA

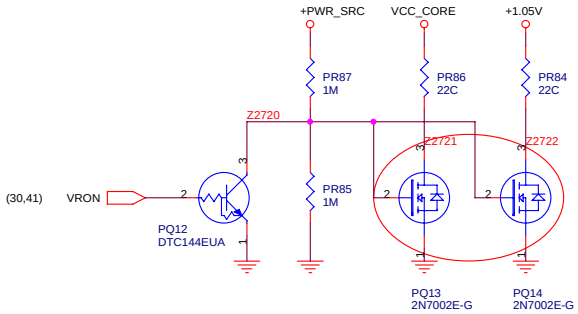
S0-S5



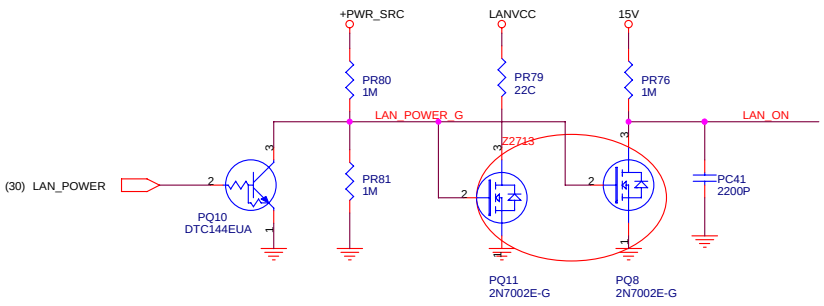
modify from 2N7002E TO 2M7002E-G



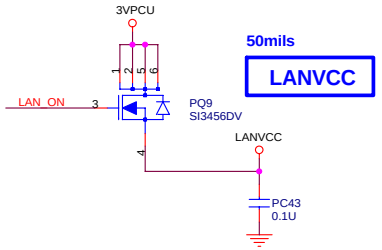
modify from 2N7002E TO 2M7002E-G



modify from 2N7002E TO 2M7002E-G



modify from 2N7002E TO 2M7002E-G



PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	1A
Date: Friday, February 10, 2006	Sheet 36 of 42	

A2 TEST TO B TEST PD14 AND PD15 MODIFY FROM SSM24PT TO SBM1040

Iinput =(V CLS / V REF)*(0.075/ RS1)

ICHG =(V ICTL / V REFIN)*(0.075/ RS2)

CELL-SET
0 = 4 CELL
1 = 3 CELL

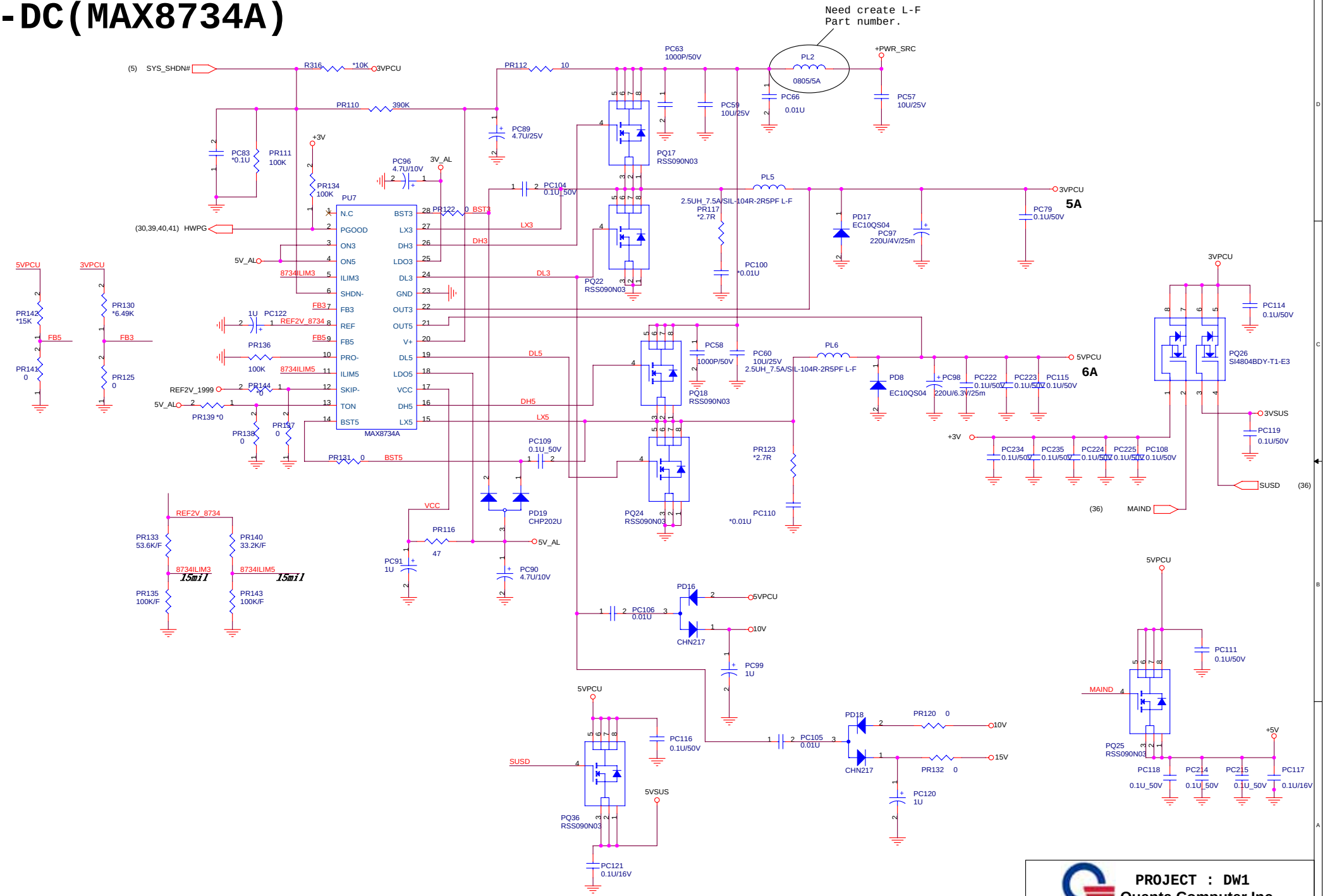
MODIFY FROM 2N7002E TO 2M7002E-G

MODIFY FROM 2N7002E TO 2M7002E-G

PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGE	1A
Date: Friday, February 10, 2006	Sheet 37 of 42	

DC-DC(MAX8734A)



PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3V/5V	1A

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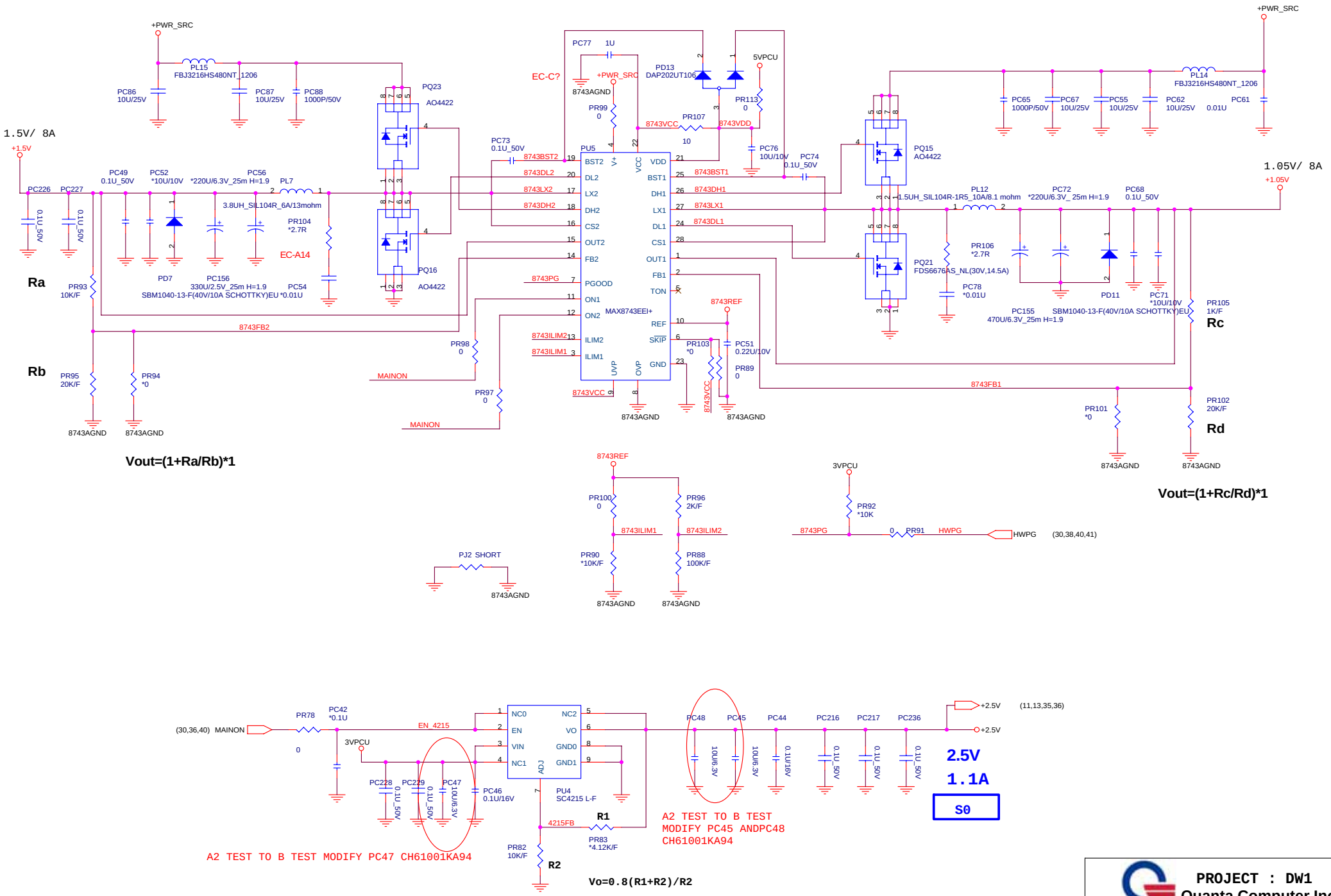
1.5V/ 8A
+PWR_SRC
PL15
FBJ3216HS480NT_1206
PC86
10U/25V
PC87
10U/25V
PC88
1000P/50V
PQ23
AO4422
PQ16
AO4422
+1.5V
PC226
PC227
0.1U_50V
PC49
0.1U_50V
PC52
*10U/10V
*220U/6.3V_25m H=1.9
PC56
PL7
3.8UH_SIL104R_6A/13mohm
PR104
*2.7R
EC-A14
PD7
PC156
330U/2.5V_25m H=1.9
SBM1040-13-F(40V/10A SCHOTTKY)EU
PC54
*0.01U
Ra
PR93
10K/F
Rb
PR95
20K/F
PR94
*0
8743AGND
8743FB2
PC73
0.1U_50V
PC77
1U
EC-C?
8743AGND
PR99
0
PD13
DAP202UT106
5VPCU
PR113
0
PR107
8743VCC
10
8743VDD
PC76
10U/10V
PC74
0.1U_50V
PU5
MAX8743EEI+
8743BST2
8743DL2
8743LX2
8743DH2
8743PG
8743ILIM2
8743ILIM1
PR98
0
MAINON
PR97
0
8743REF
PR103
*0
PC51
0.22U/10V
PR89
0
8743FB1
PR101
*0
PR102
20K/F
Rd
Vout=(1+Ra/Rb)*1
1.05V/ 8A
+1.05V
PL14
FBJ3216HS480NT_1206
PC65
1000P/50V
PC67
10U/25V
PC55
10U/25V
PC62
10U/25V
0.01U
PC61
PQ15
AO4422
PQ21
FDS6676AS_NL(30V,14.5A)
PL12
1.5UH_SIL104R-1R5_10A/8.1 mohm
PC72
*220U/6.3V_ 25m H=1.9
PC68
0.1U_50V
PR106
*2.7R
PC78
*0.01U
PC155
470U/6.3V_25m H=1.9
SBM1040-13-F(40V/10A SCHOTTKY)EU
PD11
PC71
*10U/10V
PR105
1K/F
Rc
Vout=(1+Rc/Rd)*1
PJ2 SHORT
8743AGND
PR100
0
PR96
2K/F
8743ILIM1
8743ILIM2
PR90
*10K/F
PR88
100K/F
3VPCU
PR92
*10K
8743PG
0
PR91
HWPG
(30,38,40,41)
(30,36,40) MAINON
PR78
0
PC42
*0.1U
EN_4215
3VPCU
PC228
PC229
PC47
10U/6.3V
PC46
0.1U/16V
PU4
SC4215 L-F
4215FB
R1
PR83
*4.12K/F
PR82
10K/F
R2
A2 TEST TO B TEST MODIFY PC47 CH61001KA94
Vo=0.8(R1+R2)/R2
PC48
PC45
PC44
PC216
PC217
PC236
10U/6.3V
0.1U/16V
0.1U_50V
+2.5V
(11,13,35,36)
2.5V
1.1A
S0
A2 TEST TO B TEST
MODIFY PC45 ANDPC48
CH61001KA94
PROJECT : DW1
Quanta Computer Inc.
Size
Custom
Document Number
MAX8743 1.5VS_5/+1.05V/2.5V
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1A
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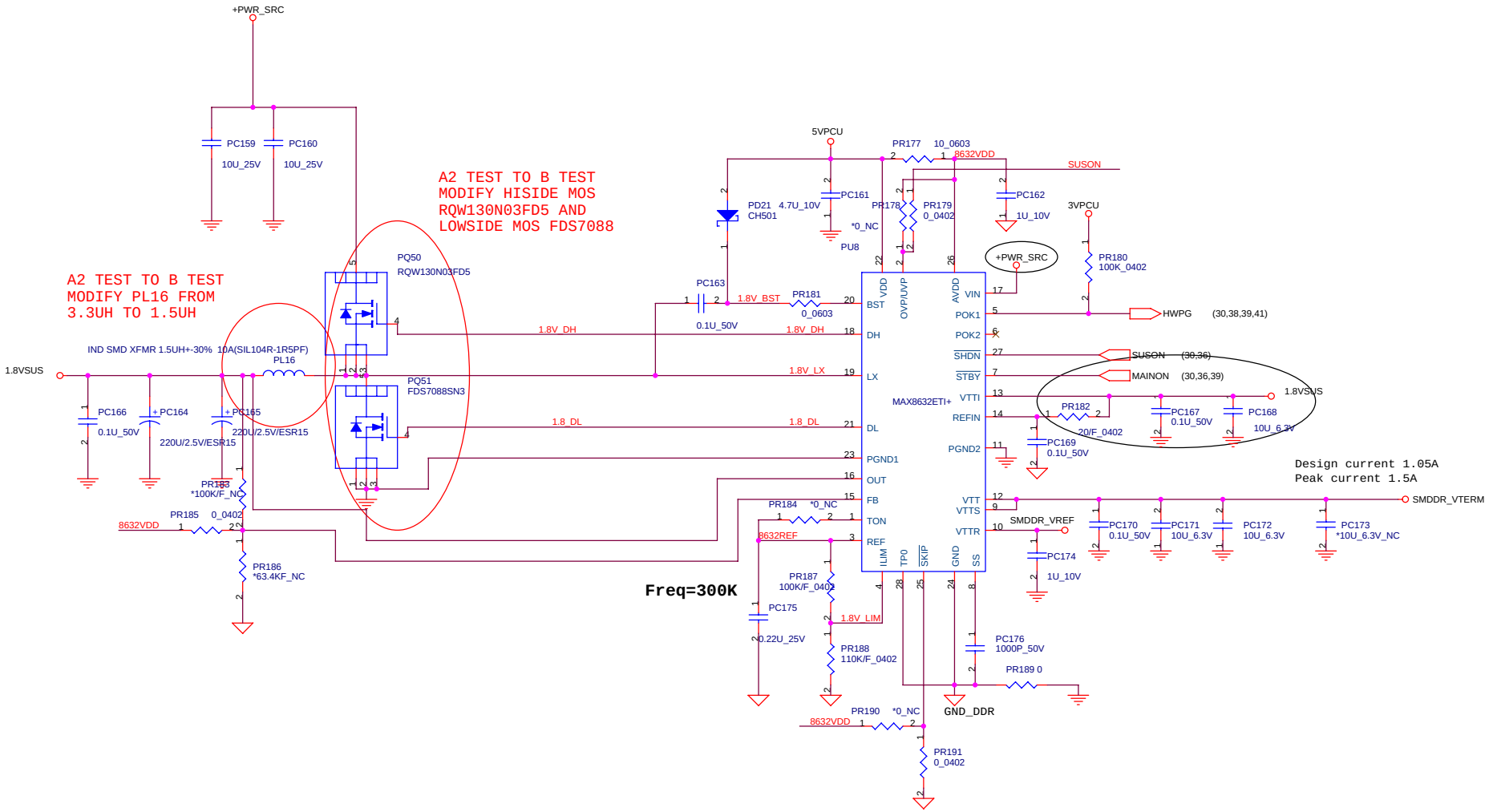

PROJECT : DW1		
Quanta Computer Inc.		
Size: Custom	Document Number: 1.8V/0.9V	Rev: 1A
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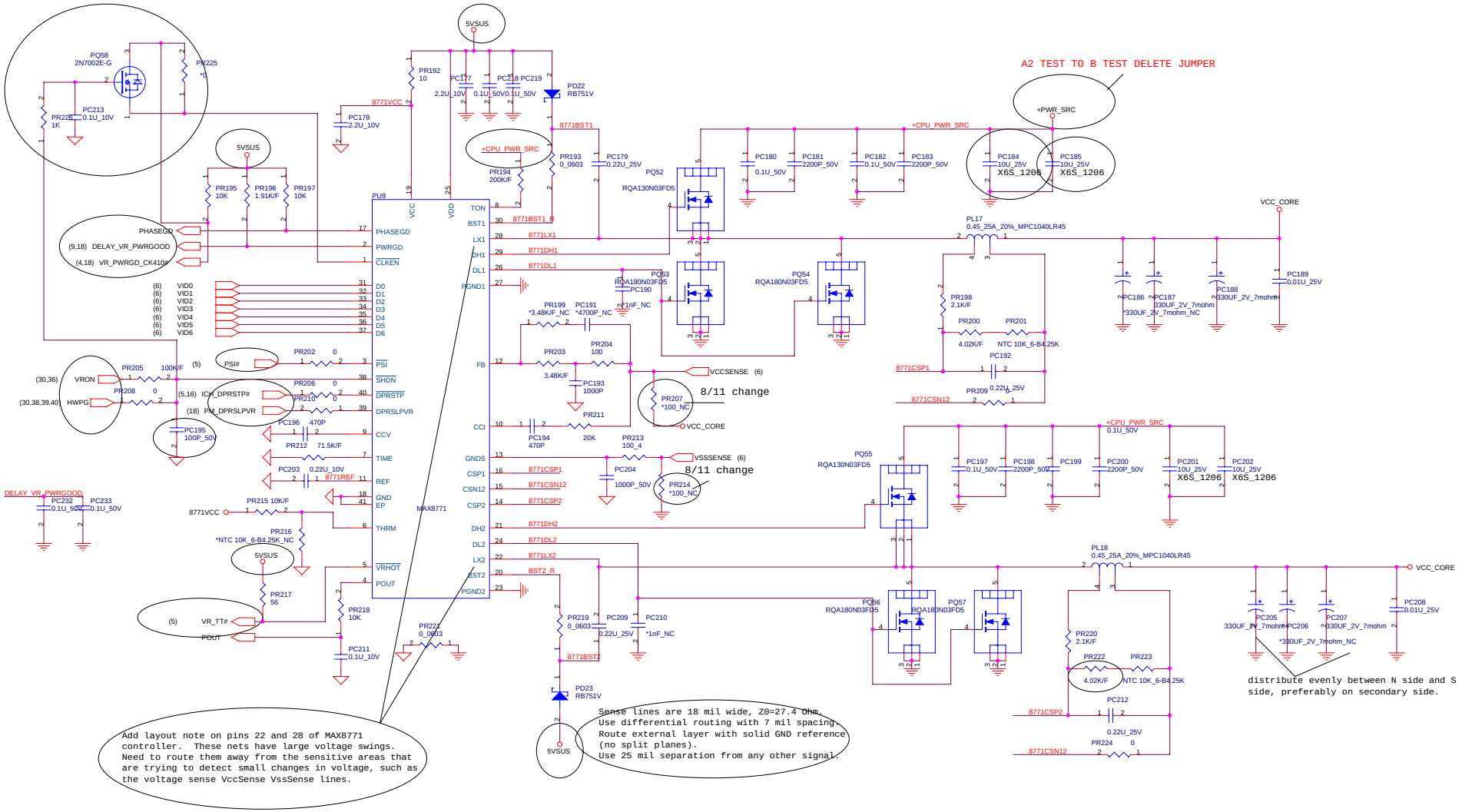

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C	max8771	1A

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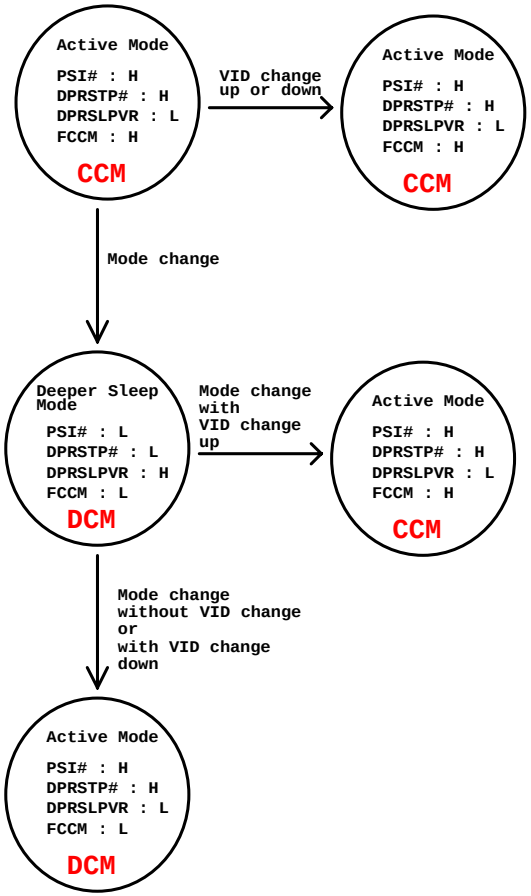
IMVP Spec. Rev. 0.8

(Nom.)	Yonah-2M	Meron
HFM	1.2875 V	1.1500 V
LFM	0.8375 V	0.8375 V
Deeper	0.7625 V	0.7625 V
VBOOT	1.2000 V	1.2000 V
SLOPE	-2.1 mV/A	-2.1 mV/A

(Max.)	Yonah-2M	Meron
HFM	36 A	44 A
LFM	9.5 A	12.5 A
Deeper	3.5 A	5.5 A
Dynamic	27 A	34.5 A
TDC	26 A	32 A

Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

CCM : Continuous Conduction Mode
DCM : Dis-Continuous Mode



PROJECT : DW1
Quanta Computer Inc.

Size	Document Number	Rev
C	CPU_Operation State	1A

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