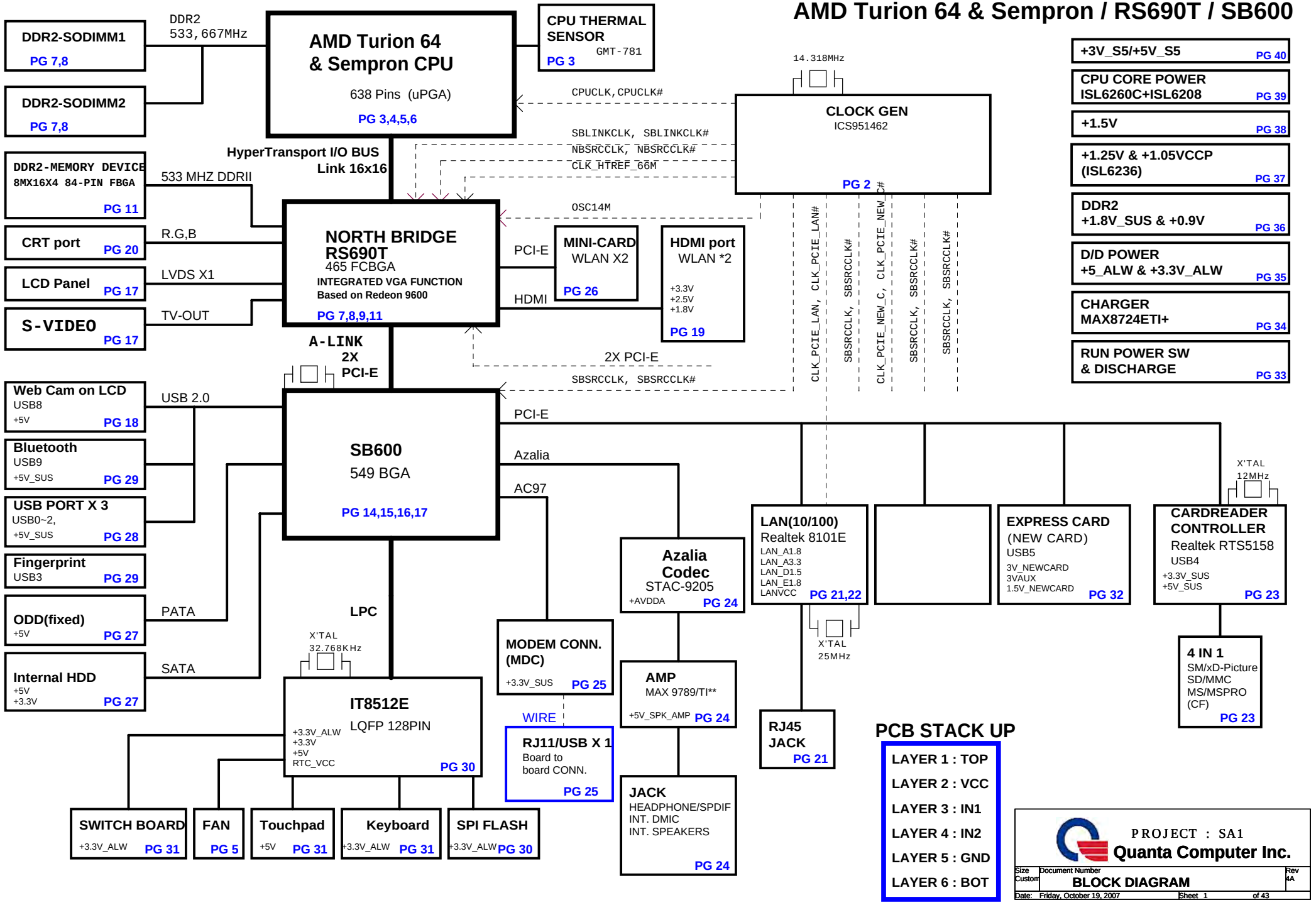
SA1A BLOCK DIAGRAM

AMD Turion 64 & Sempron / RS690T / SB600

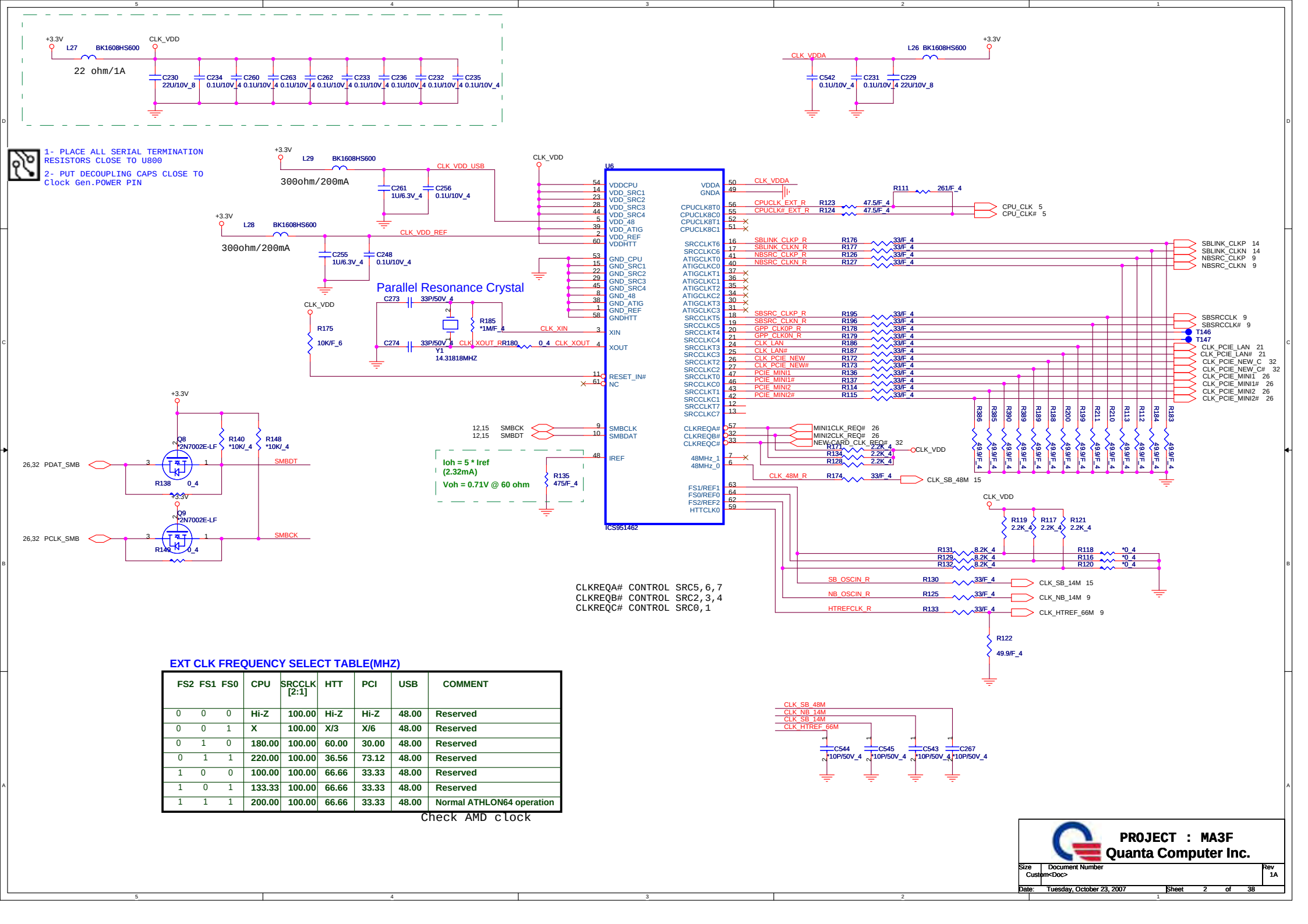


PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	4A

Date: Friday, October 19, 2007 Sheet 1 of 43



EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal ATHLON64 operation

Check AMD clock

PROJECT : MA3F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	<Doc>	1A

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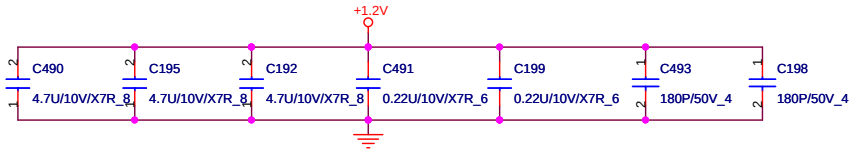
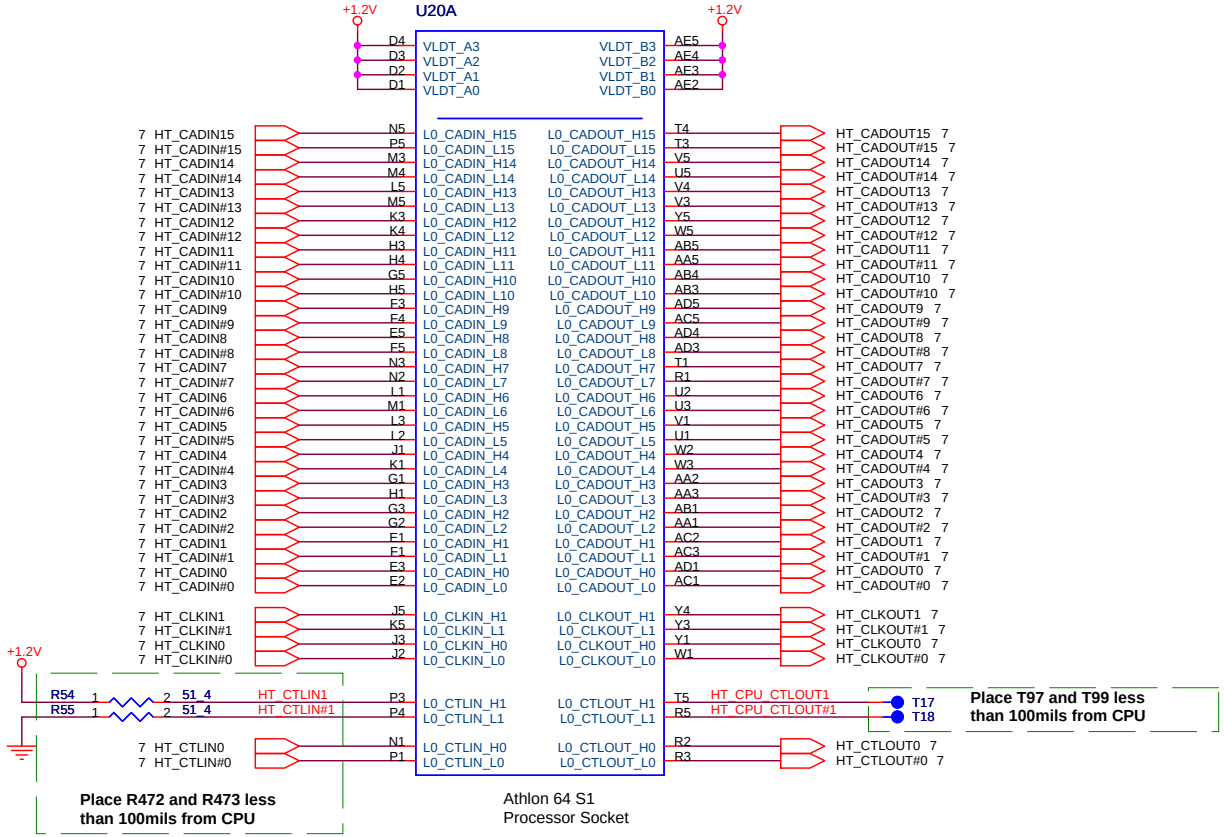


LAYOUT: Place bypass cap on topside of board

NEAR HT POWER PINS THAT ARE NOT CONNECTED DIRECTLY TO DOWNSTREAM HT DEVICE, BUT CONNECTED INTERNALLY TO OTHER HT POWER PINS
PLACE CLOSE TO VLDT0 POWER PINS

PROCESSOR HYPERTRANSPORT INTERFACE

VLDT_Ax AND VLDT_Bx ARE CONNECTED TO THE LDT_RUN POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE



NB2/RD1

PROJECT : SA8
Quanta Computer Inc.

Size	Document Number	Rev
B	<Doc>	1A

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VDD_VTT_SUS_CPU IS CONNECTED TO THE VDD_VTT_SUS POWER SUPPLY THROUGH THE PACKAGE OR ON THE DIE. IT IS ONLY CONNECTED ON THE BOARD TO DECOUPLING NEAR THE CPU PACKAGE

+1.8V_SUS

C67 0.1U/10V/X7R_4

R48 1K/F_6

CPU_VTT_SUS_SENSE should be routed as 10mils and 10mils spacing from any adjacent signals in X, Y, Z directions.

+0.9V_CPU_M_VREF_SUS

C76 0.1U/10V/X7R_4

C73 1000P/50V_4

R47 1K/F_6

for +0.9V_DDR_VTT feedback

Place Capacitors for +0.9V_CPU_M_VREF_SUS < 1" from the RS690. +0.9V_CPU_M_VREF_SUS trace length < 6", trace width > 15mils and 20mils spacing from any adjacent signals in X, Y, Z directions.

+1.8V_SUS

R351 39.2/F_4

R352 39.2/F_4

36 CPU_VTT_SENSE

M_ZN

M_ZP

KEEP TRACE TO RESISTORS LESS THAN 1.5" FROM CPU PIN

U20B

+0.9V_DDR_VTT

MEMVREF W17

VTT_SENSE Y10

MEMZN AE10

MEMZP AE10

VTT1 D10
VTT2 C10
VTT3 B10
VTT4 AD10
VTT5 W10
VTT6 AC10
VTT7 AB10
VTT8 AA10
VTT9 A10

T16 DDR_CS3_DIMMA#
T32 DDR_CS2_DIMMA#
12,13 DDR_CS1_DIMMA#
12,13 DDR_CS0_DIMMA#

MA0_CS_L3 V19
MA0_CS_L2 J22
MA0_CS_L1 V22
MA0_CS_L0 T19

MA0_CLK_H2 Y16
MA0_CLK_L2 AA16
MA0_CLK_H1 E16
MA0_CLK_L1 F16

M_CLK_DDR1 12,13
M_CLK_DDR#1 12,13
M_CLK_DDR0 12,13
M_CLK_DDR#0 12,13

T14 DDR_CS3_DIMMB#
T33 DDR_CS2_DIMMB#
12,13 DDR_CS1_DIMMB#
12,13 DDR_CS0_DIMMB#

MB0_CS_L3 Y26
MB0_CS_L2 J24
MB0_CS_L1 W24
MB0_CS_L0 U23

MB0_CLK_H2 AF18
MB0_CLK_L2 AF17
MB0_CLK_H1 A17
MB0_CLK_L1 A18

M_CLK_DDR3 12,13
M_CLK_DDR#3 12,13
M_CLK_DDR2 12,13
M_CLK_DDR#2 12,13

12,13 DDR_CKE1_DIMMB
12,13 DDR_CKE0_DIMMB
12,13 DDR_CKE1_DIMMA
12,13 DDR_CKE0_DIMMA

MB_CKE1 H26
MB_CKE0 J23
MA_CKE1 J20
MA_CKE0 J21

MB0_ODT1 W23
MB0_ODT0 W26
MA0_ODT1 V20
MA0_ODT0 U19

M_ODT3 12,13
M_ODT2 12,13
M_ODT1 12,13
M_ODT0 12,13

12,13 DDR_A_MA[0..15]

DDR_A_MA15 K19
DDR_A_MA14 K20
DDR_A_MA13 V24
DDR_A_MA12 K24
DDR_A_MA11 L20
DDR_A_MA10 R19
DDR_A_MA9 L19
DDR_A_MA8 L22
DDR_A_MA7 L21
DDR_A_MA6 M19
DDR_A_MA5 M20
DDR_A_MA4 M24
DDR_A_MA3 M22
DDR_A_MA2 N22
DDR_A_MA1 N21
DDR_A_MA0 R21

MA_ADD15
MA_ADD14
MA_ADD13
MA_ADD12
MA_ADD11
MA_ADD10
MA_ADD9
MA_ADD8
MA_ADD7
MA_ADD6
MA_ADD5
MA_ADD4
MA_ADD3
MA_ADD2
MA_ADD1
MA_ADD0

MB_ADD15 J25
MB_ADD14 J26
MB_ADD13 W25
MB_ADD12 L23
MB_ADD11 L25
MB_ADD10 U25
MB_ADD9 L24
MB_ADD8 M26
MB_ADD7 L26
MB_ADD6 N23
MB_ADD5 N24
MB_ADD4 N25
MB_ADD3 N26
MB_ADD2 P24
MB_ADD1 P26
MB_ADD0 T24

DDR_B_MA15
DDR_B_MA14
DDR_B_MA13
DDR_B_MA12
DDR_B_MA11
DDR_B_MA10
DDR_B_MA9
DDR_B_MA8
DDR_B_MA7
DDR_B_MA6
DDR_B_MA5
DDR_B_MA4
DDR_B_MA3
DDR_B_MA2
DDR_B_MA1
DDR_B_MA0

DDR_B_MA[0..15] 12,13

12,13 DDR_A_BS2
12,13 DDR_A_BS1
12,13 DDR_A_BS0

MA_BANK2 K22
MA_BANK1 R20
MA_BANK0 T22

MB_BANK2 K26
MB_BANK1 T26
MB_BANK0 U26

DDR_B_BS2 12,13
DDR_B_BS1 12,13
DDR_B_BS0 12,13

12,13 DDR_A_RAS#
12,13 DDR_A_CAS#
12,13 DDR_A_WE#

MA_RAS_L T20
MA_CAS_L U20
MA_WE_L U21

MB_RAS_L U24
MB_CAS_L V26
MB_WE_L U22

DDR_B_RAS# 12,13
DDR_B_CAS# 12,13
DDR_B_WE# 12,13

DDR II: CMD/CTRL/CLK

Athlon 64 S1
Processor Socket

Notes for the SODIMM locations:
DIMMA = Far = Bottom
DIMMB = Near = Top

Processor DDR2 Memory Interface

U20C

12 DDR_B_D[0..63]

DDR_B_D63 AD11
DDR_B_D62 AE11
DDR_B_D61 AE14
DDR_B_D60 AE14
DDR_B_D59 Y11
DDR_B_D58 AB11
DDR_B_D57 AC12
DDR_B_D56 AF13
DDR_B_D55 AF15
DDR_B_D54 AF16
DDR_B_D53 AC18
DDR_B_D52 AF19
DDR_B_D51 AD14
DDR_B_D50 AC14
DDR_B_D49 AF18
DDR_B_D48 AD18
DDR_B_D47 AD20
DDR_B_D46 AC20
DDR_B_D45 AF23
DDR_B_D44 AF24
DDR_B_D43 AF20
DDR_B_D42 AE20
DDR_B_D41 AD22
DDR_B_D40 AC22
DDR_B_D39 AE25
DDR_B_D38 AD26
DDR_B_D37 AA25
DDR_B_D36 AA26
DDR_B_D35 AE24
DDR_B_D34 AD24
DDR_B_D33 AA23
DDR_B_D32 AA24
DDR_B_D31 G24
DDR_B_D30 G23
DDR_B_D29 D26
DDR_B_D28 C26
DDR_B_D27 G26
DDR_B_D26 G25
DDR_B_D25 E24
DDR_B_D24 E23
DDR_B_D23 C24
DDR_B_D22 B24
DDR_B_D21 C20
DDR_B_D20 B20
DDR_B_D19 C25
DDR_B_D18 D24
DDR_B_D17 A21
DDR_B_D16 D20
DDR_B_D15 D18
DDR_B_D14 C18
DDR_B_D13 D14
DDR_B_D12 C14
DDR_B_D11 A20
DDR_B_D10 A19
DDR_B_D9 A16
DDR_B_D8 A15
DDR_B_D7 A13
DDR_B_D6 D12
DDR_B_D5 E11
DDR_B_D4 G11
DDR_B_D3 B14
DDR_B_D2 A14
DDR_B_D1 A11
DDR_B_D0 C11

MB_DATA63
MB_DATA62
MB_DATA61
MB_DATA60
MB_DATA59
MB_DATA58
MB_DATA57
MB_DATA56
MB_DATA55
MB_DATA54
MB_DATA53
MB_DATA52
MB_DATA51
MB_DATA50
MB_DATA49
MB_DATA48
MB_DATA47
MB_DATA46
MB_DATA45
MB_DATA44
MB_DATA43
MB_DATA42
MB_DATA41
MB_DATA40
MB_DATA39
MB_DATA38
MB_DATA37
MB_DATA36
MB_DATA35
MB_DATA34
MB_DATA33
MB_DATA32
MB_DATA31
MB_DATA30
MB_DATA29
MB_DATA28
MB_DATA27
MB_DATA26
MB_DATA25
MB_DATA24
MB_DATA23
MB_DATA22
MB_DATA21
MB_DATA20
MB_DATA19
MB_DATA18
MB_DATA17
MB_DATA16
MB_DATA15
MB_DATA14
MB_DATA13
MB_DATA12
MB_DATA11
MB_DATA10
MB_DATA9
MB_DATA8
MB_DATA7
MB_DATA6
MB_DATA5
MB_DATA4
MB_DATA3
MB_DATA2
MB_DATA1
MB_DATA0

MA_DATA63 AA12
MA_DATA62 AB12
MA_DATA61 AA14
MA_DATA60 AB14
MA_DATA59 W11
MA_DATA58 Y12
MA_DATA57 AD13
MA_DATA56 AB13
MA_DATA55 AD15
MA_DATA54 AB15
MA_DATA53 AB17
MA_DATA52 Y17
MA_DATA51 Y14
MA_DATA50 W14
MA_DATA49 W16
MA_DATA48 AD17
MA_DATA47 Y18
MA_DATA46 AD19
MA_DATA45 AD21
MA_DATA44 AB21
MA_DATA43 AB18
MA_DATA42 AA18
MA_DATA41 AA20
MA_DATA40 Y20
MA_DATA39 AA22
MA_DATA38 Y22
MA_DATA37 W21
MA_DATA36 W22
MA_DATA35 AA21
MA_DATA34 AB22
MA_DATA33 AB24
MA_DATA32 Y24
MA_DATA31 H22
MA_DATA30 H20
MA_DATA29 E22
MA_DATA28 E21
MA_DATA27 J19
MA_DATA26 H24
MA_DATA25 F22
MA_DATA24 F20
MA_DATA23 C23
MA_DATA22 B22
MA_DATA21 F18
MA_DATA20 E18
MA_DATA19 E20
MA_DATA18 D22
MA_DATA17 C19
MA_DATA16 G18
MA_DATA15 G17
MA_DATA14 C17
MA_DATA13 F14
MA_DATA12 E14
MA_DATA11 H17
MA_DATA10 E17
MA_DATA9 E15
MA_DATA8 H15
MA_DATA7 E13
MA_DATA6 C13
MA_DATA5 H12
MA_DATA4 H11
MA_DATA3 G14
MA_DATA2 H14
MA_DATA1 E12
MA_DATA0 G12

DDR_A_D63
DDR_A_D62
DDR_A_D61
DDR_A_D60
DDR_A_D59
DDR_A_D58
DDR_A_D57
DDR_A_D56
DDR_A_D55
DDR_A_D54
DDR_A_D53
DDR_A_D52
DDR_A_D51
DDR_A_D50
DDR_A_D49
DDR_A_D48
DDR_A_D47
DDR_A_D46
DDR_A_D45
DDR_A_D44
DDR_A_D43
DDR_A_D42
DDR_A_D41
DDR_A_D40
DDR_A_D39
DDR_A_D38
DDR_A_D37
DDR_A_D36
DDR_A_D35
DDR_A_D34
DDR_A_D33
DDR_A_D32
DDR_A_D31
DDR_A_D30
DDR_A_D29
DDR_A_D28
DDR_A_D27
DDR_A_D26
DDR_A_D25
DDR_A_D24
DDR_A_D23
DDR_A_D22
DDR_A_D21
DDR_A_D20
DDR_A_D19
DDR_A_D18
DDR_A_D17
DDR_A_D16
DDR_A_D15
DDR_A_D14
DDR_A_D13
DDR_A_D12
DDR_A_D11
DDR_A_D10
DDR_A_D9
DDR_A_D8
DDR_A_D7
DDR_A_D6
DDR_A_D5
DDR_A_D4
DDR_A_D3
DDR_A_D2
DDR_A_D1
DDR_A_D0

DDR_A_D[0..63] 12

To SODIMM socket B (Near/TOP)

To SODIMM socket A (Far/Bottom)

12 DDR_B_DM[0..7]

DDR_B_DM7 AD12
DDR_B_DM6 AC16
DDR_B_DM5 AE22
DDR_B_DM4 AB26
DDR_B_DM3 E25
DDR_B_DM2 A22
DDR_B_DM1 B16
DDR_B_DM0 A12

MB_DM7
MB_DM6
MB_DM5
MB_DM4
MB_DM3
MB_DM2
MB_DM1
MB_DM0

MA_DM7 Y13
MA_DM6 AB16
MA_DM5 Y19
MA_DM4 AC24
MA_DM3 F24
MA_DM2 E19
MA_DM1 C15
MA_DM0 E12

DDR_A_DM7
DDR_A_DM6
DDR_A_DM5
DDR_A_DM4
DDR_A_DM3
DDR_A_DM2
DDR_A_DM1
DDR_A_DM0

DDR_A_DM[0..7] 12

DDR_B_DQS7 AE12
DDR_B_DQS#7 AE12
DDR_B_DQS6 AE16
DDR_B_DQS#6 AD16
DDR_B_DQS5 AF21
DDR_B_DQS#5 AF22
DDR_B_DQS4 AC25
DDR_B_DQS#4 AC26
DDR_B_DQS3 F26
DDR_B_DQS#3 F26
DDR_B_DQS2 A24
DDR_B_DQS#2 A23
DDR_B_DQS1 D16
DDR_B_DQS#1 C16
DDR_B_DQS0 C12
DDR_B_DQS#0 B12

MB_DQS_H7
MB_DQS_L7
MB_DQS_H6
MB_DQS_L6
MB_DQS_H5
MB_DQS_L5
MB_DQS_H4
MB_DQS_L4
MB_DQS_H3
MB_DQS_L3
MB_DQS_H2
MB_DQS_L2
MB_DQS_H1
MB_DQS_L1
MB_DQS_H0
MB_DQS_L0

MA_DQS_H7 W12
MA_DQS_L7 W13
MA_DQS_H6 Y15
MA_DQS_L6 W15
MA_DQS_H5 AB19
MA_DQS_L5 AB20
MA_DQS_H4 AD23
MA_DQS_L4 AC23
MA_DQS_H3 G22
MA_DQS_L3 G21
MA_DQS_H2 C22
MA_DQS_L2 C21
MA_DQS_H1 G16
MA_DQS_L1 G15
MA_DQS_H0 G13
MA_DQS_L0 H13

DDR_A_DQS7
DDR_A_DQS#7
DDR_A_DQS6
DDR_A_DQS#6
DDR_A_DQS5
DDR_A_DQS#5
DDR_A_DQS4
DDR_A_DQS#4
DDR_A_DQS3
DDR_A_DQS#3
DDR_A_DQS2
DDR_A_DQS#2
DDR_A_DQS1
DDR_A_DQS#1
DDR_A_DQS0
DDR_A_DQS#0

DDR: DATA

Athlon 64 S1
Processor Socket

12 DDR_B_DQS[0..7]

DDR_B_DQS0
DDR_B_DQS1
DDR_B_DQS2
DDR_B_DQS3
DDR_B_DQS4
DDR_B_DQS5
DDR_B_DQS6
DDR_B_DQS7

12 DDR_B_DQS#[0..7]

DDR_B_DQS#0
DDR_B_DQS#1
DDR_B_DQS#2
DDR_B_DQS#3
DDR_B_DQS#4
DDR_B_DQS#5
DDR_B_DQS#6
DDR_B_DQS#7

12 DDR_A_DQS[0..7]

DDR_A_DQS0
DDR_A_DQS1
DDR_A_DQS2
DDR_A_DQS3
DDR_A_DQS4
DDR_A_DQS5
DDR_A_DQS6
DDR_A_DQS7

12 DDR_A_DQS#[0..7]

DDR_A_DQS#0
DDR_A_DQS#1
DDR_A_DQS#2
DDR_A_DQS#3
DDR_A_DQS#4
DDR_A_DQS#5
DDR_A_DQS#6
DDR_A_DQS#7

QUANTA COMPUTER

Title	ATHLON64 DDRII MEMORY	
Size	Document Number MGD	Rev 1A
Date: Tuesday, October 23, 2007	Sheet 4 of 38	

SB600 ONLY

14 CPU_PWRGD — R376 680_4 — C210 1000P/16V/X7R_4 — CPU_PWRGD — R91 *0_4 — LDT_STOP_R#

+1.8V — R99 *0_4 — +1.8V_SUS — R97 0_4

D4 SDMK0340L-7-F

9,14 LDT_STOP# — R100 680_4 — C221 0.1U/16V_4 — R98 20K/F_4 — C217 47P/50V_4 — U4 NL17SZ17DFT2G — R96 *680_4

NOTE: R7518 and C7598 close to JCPU pin F10

14 LDT_RST# — R377 680 — C540 1000P/16V/X7R_4 — LDT_RST#

NOTE: Place R7090 on the top of the board that is iaccessible, and that shorting across this resistor will toggle the hyper Transport reset signal.

2 CPU_CLK — C529 3900P/50V_4 — CPU_CLKIN_SC_P / CPU_CLKIN_SC_N

R373 169/F_4

2 CPU_CLK# — C528 3900P/50V_4

1.KEEP TRACE TO RESISTOR LESS THAN 600MILS FROM CPU PIN AND TRACE TO AC CAPS LESS THAN 1250MILS.

2. CPUCLK and CPUCLK# mismatch < 35 mils.

+1.8V_SUS — R40 *10K_4 — +3.3V — R42 *4.7K_4 — Q2 *MMBT3904 — CPU_PROCHOT# — SB_CPU_PROCHOT# 16

VR_TT# 37

+1.8V_SUS — R92 220_4 — R90 220_4 — R28 220_4 — R30 220_4 — R29 220_4

HDT CONNECTOR

JHDT1 *HDT conn

CPU_DBREQ# CPU_DBRDY CPU_TCK CPU_TMS CPU_TDI CPU_TRST# CPU_TDO

GND Resreved1 Resreved2 DBREQ_L DBRDY TCK TMS TDI TRST_L TDO VDDIO1 VDDIO2 RESET_L GND

+1.8V_SUS

+3.3V — R379 4.7K_4 — +1.8V — R381 4.7K_4 — CPU_RESET# — Q37 MMBT3904 — LDT_RST#

R380 *100K_4

NOTE:HDT TERMINATION IS REQUIRED FOR REV.Ax SILICON ONLY.

L65 ferrite bead with an approximate impedance of 33 , a maximum DC resistance of 0.025 ohm , and a current rating of at least 3000mA.

LAYOUT: ROUTE VDDA TRACE APPROX. 50 mils WIDE (USE 2x25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG. This trace should be kept at least 20 mils away from all other signals.

+2.5V_CPU_VDDA_RUN

+2.5V — L25 <Size> BLM18PG330SN1D — +2.5V_CPU_VDDA_RUN — +2.5V_CPU_VDDA_RUN

C532 100U/6.3V_3528 — C224 4.7U/10V_8 — C223 0.22U/10V_6 — C218 3300P/X7R/_4

If AMD SI is not used, the SID pin can be left unconnected and SIC should have a 300- (ƒ 5%) pulldown to VSS.

The AMD SI feature has errata, and will not be plemented.

Place R78 and R77 < 1.5". Route CPU_HTREF1/0 with 5mils trace width and 10mils spacing from other signals in X, Y, Z directions

+1.2V — R353 300_4 — CPU_SIC — R354 *0_4 — CPU_SID

R361 44.2/F_4 — CPU_HTREF1 — R358 44.2/F_4 — CPU_HTREF0

To Power 37 CPU_VDD_RUN_FB_H / CPU_VDD_RUN_FB_L — T42 — T49

36 VDDIO_FB_H / VDDIO_FB_L

T15 T13 T58 T59 T47 T46 — VDDIO_FB_H / VDDIO_FB_L / CPU_CLK / CPU_CLK# / CPU_TEST29_H_FBCLKOUT_P / CPU_TEST29_L_FBCLKOUT_N

U20D

VDDA2 VDDA1 — RESET_L PWROK LDTSTOP_L — SIC SID — HT_REF1 HT_REF0 — VDD_FB_H VDD_FB_L — VDDIO_FB_H VDDIO_FB_L — CLKIN_H CLKIN_L — DBRDY — TMS TCK TRST_L TDI — TDO

LDT_RST# CPU_PWRGD LDT_STOP_R# CPU_SIC CPU_SID CPU_HTREF1 CPU_HTREF0 CPU_CLKIN_SC_P CPU_CLKIN_SC_N CPU_DBRDY CPU_TMS CPU_TCK CPU_TRST# CPU_TDI CPU_DBREQ# CPU_TDO

THERMTRIP_L PROCHOT_L — THERMTRIP# CPU_PROCHOT# — H_THERMTRIP# 15

+1.8V_SUS — R41 300_4 — R22 300_4 — R104 300_4 — THERM EB — +3.3V_ALW — R38 10K_4 — R34 *4.7K

Q1 MMST3904 — C49 0.1U/16V_4

VID5 VID4 VID3 VID2 VID1 VID0 — 37

CPU_PRESENT_L — CPU_PRESENT# — PSI_L — CPU_PSI# 37 — T51

PSI_L is a Power Status Indicator signal. This signal is asserted when the processor is in a low powerstate. PSI_L should be connected to the power supply controller, if the controller supports ¨skipmode, or diode emulation mode〃. PSI_L is asserted by the processor during the C3 and S1 states.

TEST29_H TEST29_L — C9 CPU_TEST29_H_FBCLKOUT_P — R89 80.6/F_4 — C8 CPU_TEST29_L_FBCLKOUT_N

ROUTE AS 80 Ohm DIFFERENTIAL PAIR PLACE IT CLOSE TO CPU WITHIN 1"

T41 T44 T38 T35 — CPU_TEST25_H_BYPASSCLK_H / CPU_TEST25_L_BYPASSCLK_L / CPU_TEST19_PLLTEST0 / CPU_TEST18_PLLTEST1 — TEST25_H TEST25_L TEST19 TEST18 TEST13 TEST9

T45 T43 T139 T54 T9 — CPU_TEST17_BP3 / CPU_TEST16_BP2 / CPU_TEST15_BP1 / CPU_TEST14_BP0 / CPU_TEST12_SCANSHIFTENB — TEST17 TEST16 TEST15 TEST14 TEST12

TEST24 TEST23 TEST22 TEST21 TEST20 — CPU_TEST24_SCANCLK1 / CPU_TEST23_TSTUPD / CPU_TEST22_SCANSHIFTEN / CPU_TEST21_SCANEN / CPU_TEST20_SCANCLK2 — T4 T6 T8 T10 T3

TEST28_H TEST28_L TEST27 TEST26 TEST10 TEST8 — CPU_TEST27_SINGLECHAIN / CPU_TEST26_BURNIN# — T5 T7

H_THERMDC H_THERMDA — TEST7 TEST6 TEST5 TEST4 TEST3 TEST2

T26 T25 T29 T28 — CPU_RSVD_MA0_CLK3_P / CPU_RSVD_MA0_CLK3_N / CPU_RSVD_MA0_CLK0_P / CPU_RSVD_MA0_CLK0_N — RSVD0 RSVD1 RSVD2 RSVD3

RSVD8 RSVD9 — CPU_MA_RESET# / CPU_MB_RESET# — T39 T50

RSVD10 RSVD11 — CPU_RSVD_VIDSTRB1 / CPU_RSVD_VIDSTRB0 — T138 T137

RSVD12 RSVD13 RSVD14 — CPU_RSVD_VDDNB_FB_P / CPU_RSVD_VDDNB_FB_N / CPU_RSVD_CORE_TYPE — T34 T40 T48

RSVD15 RSVD16 RSVD17 RSVD18 RSVD19 RSVD20 — CPU_RSVD_15 / CPU_RSVD_16 / CPU_RSVD_17 / CPU_RSVD_18 / CPU_RSVD_19 / CPU_RSVD_20 — T21 T12 T20 T11 T36 T37

T23 T22 T27 T19 — CPU_RSVD_MB0_CLK3_P / CPU_RSVD_MB0_CLK3_N / CPU_RSVD_MB0_CLK0_P / CPU_RSVD_MB0_CLK0_N — RSVD4 RSVD5 RSVD6 RSVD7

MISC

AMD NPT S1 SOCKET Processor Socket

CPU_TEST27_SINGLECHAIN R347 *300_4 — CPU_TEST26_BURNIN# R346 300_4 — CPU_PRESENT# R44 1K/F_4 — CPU_TEST25_H_BYPASSCLK_H R90 510/F_4

+1.8V_SUS

CPU_TEST21_SCANEN R26 300_4 — CPU_TEST20_SCANCLK2 R45 *300_4 — CPU_TEST24_SCANCLK1 R349 *300_4 — CPU_TEST22_SCANSHIFTEN R350 *300_4 — CPU_TEST12_SCANSHIFTENB R27 *300_4 — CPU_TEST15_BP1 R94 *300_4 — CPU_TEST14_BP0 R93 *300_4

CPU_TEST25_L_BYPASSCLK_L R95 510/F_4

CPU_TEST19_PLLTEST0 R64 300_4 — CPU_TEST18_PLLTEST1 R65 300_4

If no use which Net need pull-up or down

CPU Thermal monitor

30 ABCLK — Q4 2N7002W-7-F — ABCLK — THCLK_SMB

30 ABDATA — Q6 2N7002W-7-F — ABDATA — THDAT_SMB

16 THERM_ALERT# — R85 *0_4

34 SYS_SHDN# — Q7 2N7002W-7-F — 6648OVERT#

+3.3V — R82 10K_4 — R83 10K_4 — R84 10K_4 — R87 *10K_4

R88 220_6 — 6648VCC — C207 0.1U/10V/X5R_4

U3 G781P8 ADDRESS: 98H

SCLK SDA ALERT# OVERT# — VCC DXP DXN GND

H_THERMDA — C208 2200P/50V_6 — H_THERMDC

Layout Note: Layout Note:Routing 10:10 mils and away from noise source with ground gard

30 PWM_FAN1 — R378 100K_4 — C534 0.1U/10V/X5R_4

+5V — 30 mil — U21 G993P1U — VEN VIN VO SET GND GND GND GND — +5V_FAN — 30 mil

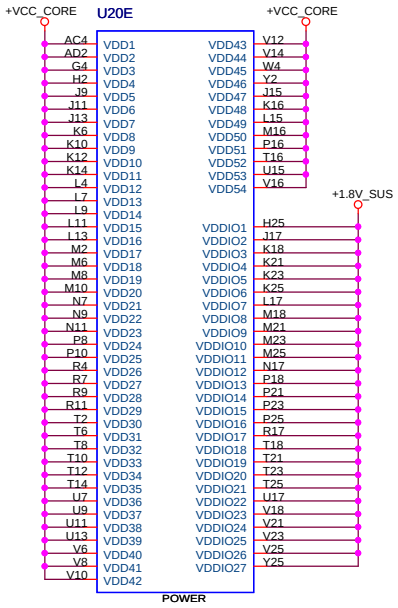
C539 1U/10V/X5R_6 — C536 0.1U/10V/X5R_4 — C537 10U/10V/X5R_8 — C548 1000P/16V/X7R_4

30 mil — +5V_FAN — CN21 FAN

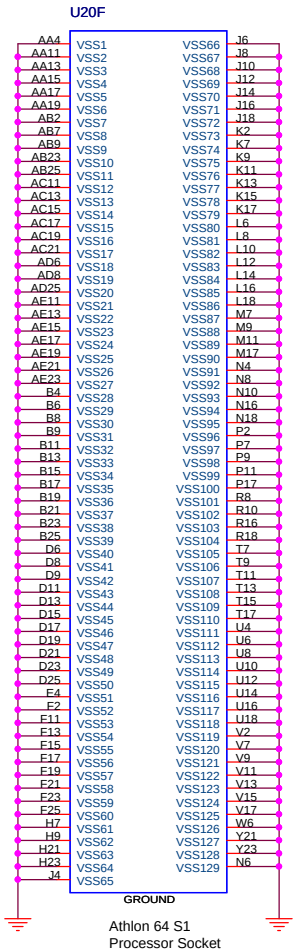
+3.3V — Q39 PDTA124EU — 30 FANSIG1 — R409 100K_4

QUANTA COMPUTER

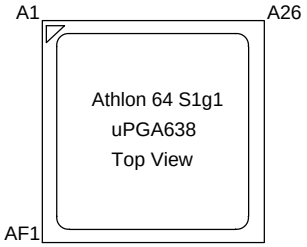
Title	ATHLON64 CTRL & DEBUG	
Size	Document Number MGD	Rev 1A
Date: Tuesday, October 23, 2007	Sheet 5 of 38	

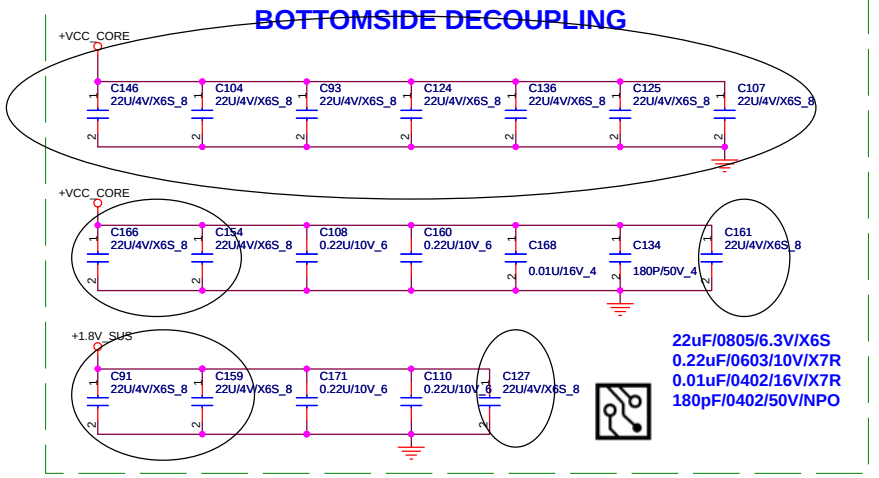


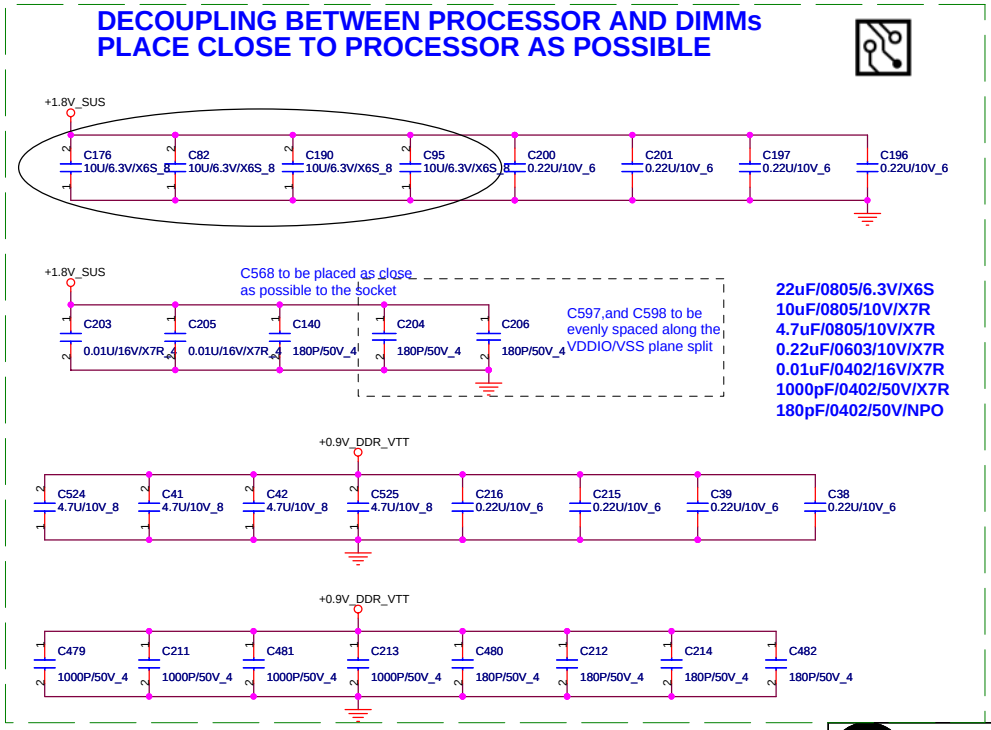
Athlon 64 S1
Processor Socket



Athlon 64 S1
Processor Socket







PROCESSOR POWER AND GROUND

QUANTA COMPUTER

Title	ATHLON64 PWR & GND	
Size	Document Number MGD	Rev 1A
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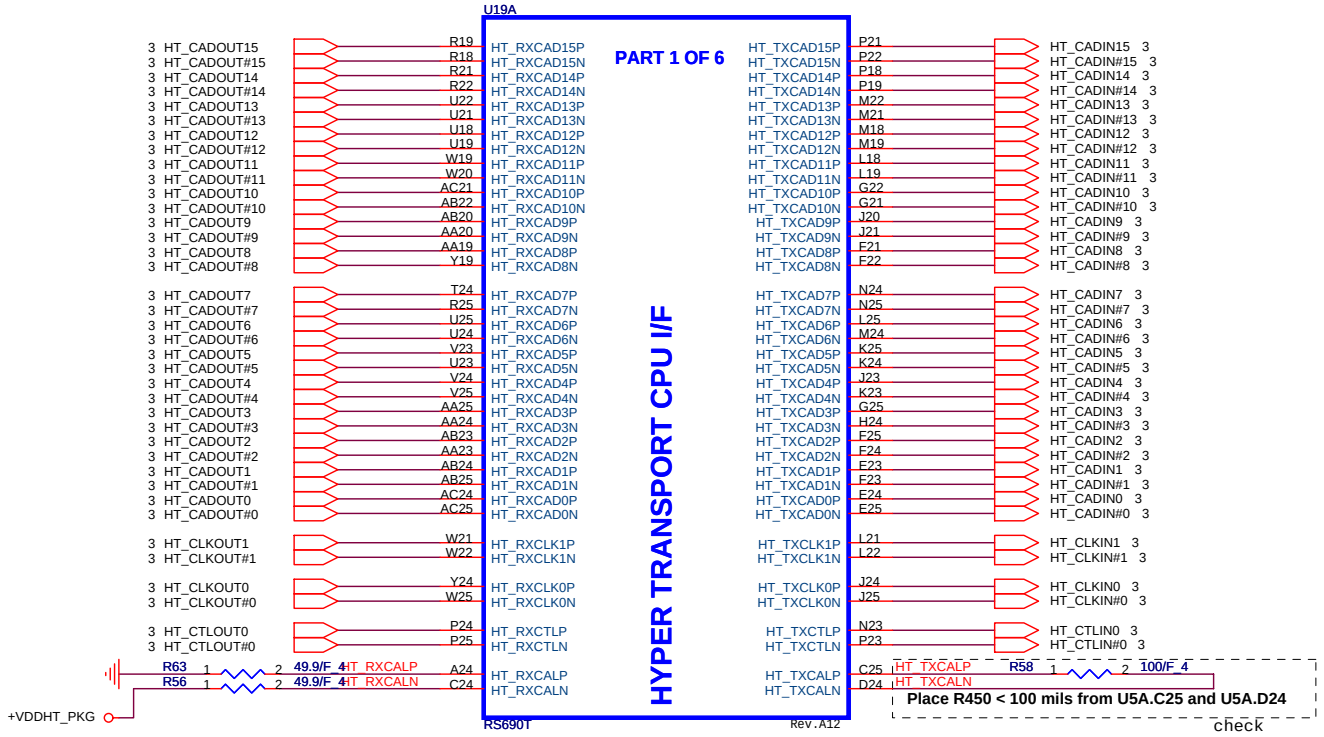
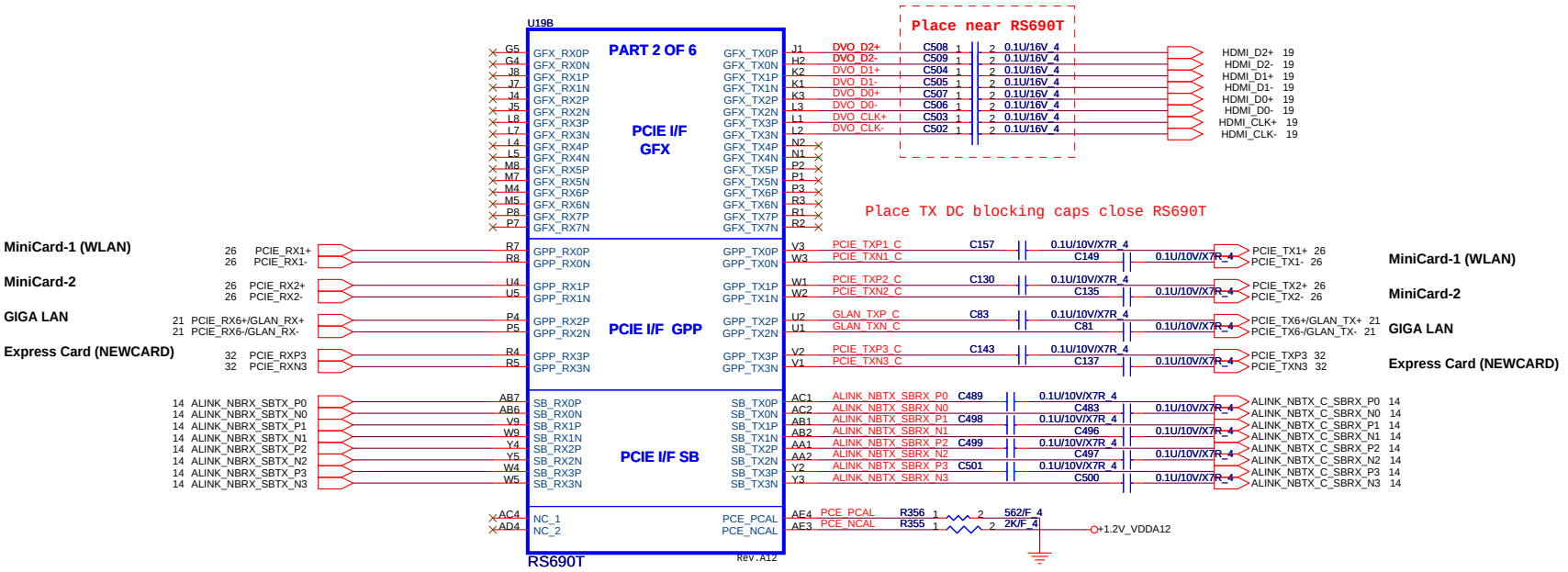
Change Part Number

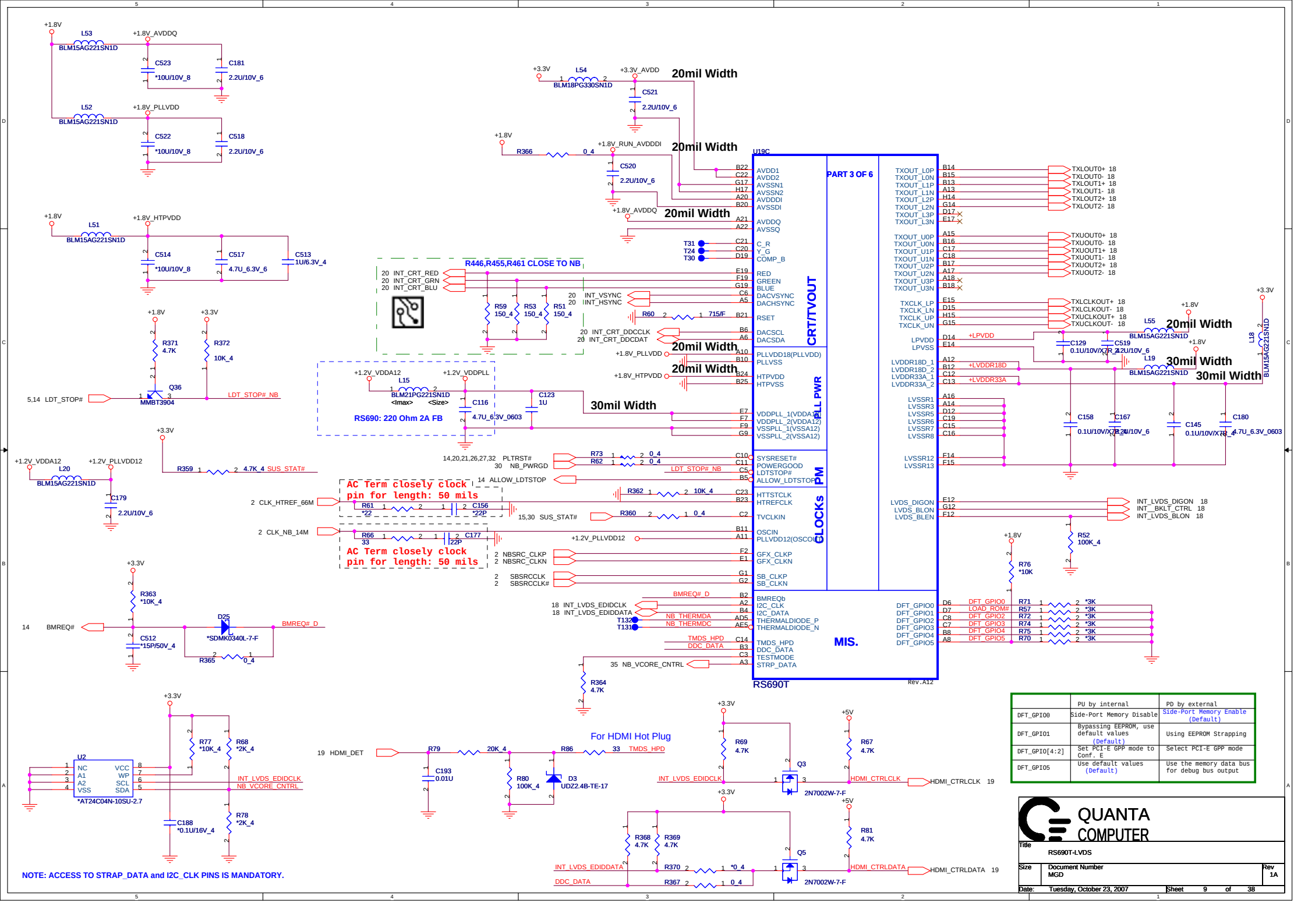


QUANTA COMPUTER

Title	RS690T-HT LINK0 I/F	
Size	Document Number MGD	Rev 1A
Date: Tuesday, October 23, 2007	Sheet 7 of 38	



Title	RS690T-PCIE LINK I/F
Size	Document Number: MGD
Rev	1A
Date:	Tuesday, October 23, 2007
Sheet	8 of 38


+1.8V
L53
BLM15AG221SN1D
+1.8V_AVDDQ
C523
*10U/10V_8
C181
2.2U/10V_6
L52
+1.8V_PLLVDD
C522
C518
+1.8V_HTPVDD
L51
C514
C517
4.7U_6.3V_6
C513
1U/6.3V_4
+3.3V
L54
BLM18PG330SN1D
+3.3V_AVDD
C521
20mil Width
+1.8V_RUN_AVDDDI
R366
0_4
C520
+1.8V_AVDDQ
U19C
PART 3 OF 6
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDDI
AVSSDI
AVDDQ
AVSSQ
C_R
Y_G
COMP_B
CRT/TVOUT
R446,R455,R461 CLOSE TO NB
20 INT_CRT_RED
20 INT_CRT_GRN
20 INT_CRT_BLU
RED
GREEN
BLUE
R59 150_4
R53 150_4
R51 150_4
20 INT_VSYNC
20 INT_HSYNC
DACVSYNC
DACHSYNC
R60 715/F
RSET
DACSCL
DACSDA
20 INT_CRT_DDCCLK
20 INT_CRT_DDCDAT
+1.8V_PLLVDD
+1.8V_HTPVDD
PLLVDD18(PLLVDD)
PLLVSS
HTPVDD
HTPVSS
PLL PWR
+1.2V_VDDA12
+1.2V_VDDPLL
L15
BLM21PG221SN1D
<Imax>
<Size>
C116
4.7U_6.3V_0603
C123
1U
30mil Width
RS690: 220 Ohm 2A FB
VDDPLL_1(VDDA12)
VDDPLL_2(VDDA12)
VSSPLL_1(VSSA12)
VSSPLL_2(VSSA12)
Q36
MMBT3904
R371
4.7K
R372
10K_4
5,14 LDT_STOP#
LDT_STOP# NB
+3.3V
R359
4.7K_4
SUS_STAT#
+1.2V_VDDA12
+1.2V_PLLVDD12
L20
BLM15AG221SN1D
C179
2.2U/10V_6
14,20,21,26,27,32 PLTRST#
30 NB_PWRGD
R73
R62
0_4
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
14 ALLOW_LDTSTOP
LDT_STOP# NB
PM
AC Term closely clock pin for length: 50 mils
2 CLK_HTREF_66M
R61
*22
C156
*22P
R362
10K_4
15,30 SUS_STAT#
R360
0_4
HTTSTCLK
HTREFCLK
TVCLKIN
2 CLK_NB_14M
R66
33
C177
22P
+1.2V_PLLVDD12
OSCIN
PLLVDD12(OSCOUT)
CLOCKs
2 NBSRC_CLKP
2 NBSRC_CLKN
GFX_CLKP
GFX_CLKN
2 SBSRCCLK
2 SBSRCCLK#
SB_CLKP
SB_CLKN
BMREQ# D
18 INT_LVDS_EDIDCLK
18 INT_LVDS_EDIDDATA
BMREQb
I2C_CLK
I2C_DATA
NB_THERMDA
NB_THERMDC
THERMALDIODE_P
THERMALDIODE_N
T132
T131
TMDS_HPD
DDC_DATA
TESTMODE
STRP_DATA
MIS.
35 NB_VCORE_CNTRL
R364
4.7K
RS690T
Rev.A12
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXCLK_LP
TXCLK_LN
TXCLK_UP
TXCLK_UN
LPVDD
LPVSS
LVDDR18D_1
LVDDR18D_2
LVDDR33A_1
LVDDR33A_2
LVSSR1
LVSSR3
LVSSR5
LVSSR6
LVSSR7
LVSSR8
LVSSR12
LVSSR13
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
DFT_GPIO0
DFT_GPIO1
DFT_GPIO2
DFT_GPIO3
DFT_GPIO4
DFT_GPIO5
TXCLKOUT+ 18
TXCLKOUT- 18
TXUCLKOUT+ 18
TXUCLKOUT- 18
+LPVDD
+LVDDR18D
+LVDDR33A
L55
BLM15AG221SN1D
C129
0.1U/10V/X7R
C519
2.2U/10V_6
L19
30mil Width
L18
C158
C167
C145
C180
4.7U_6.3V_0603
INT_LVDS_DIGON 18
INT__BKLT_CTRL 18
INT_LVDS_BLON 18
R52
100K_4
R76
*10K
R71
R57
R72
R74
R75
R70
*3K
LOAD_ROM#
R363
*10K_4
D25
*SDMK0340L-7-F
C512
*15P/50V_4
R365
0_4
BMREQ# D
U2
NC
A1
A2
VSS
VCC
WP
SCL
SDA
*AT24C04N-10SU-2.7
R77
*10K_4
R68
*2K_4
R78
*2K_4
C188
*0.1U/16V_4
INT_LVDS_EDIDCLK
NB_VCORE_CNTRL
For HDMI Hot Plug
19 HDMI_DET
R79
20K_4
C193
0.01U
R86
33
TMDS_HPD
R80
100K_4
D3
UDZ2.4B-TE-17
R69
4.7K
R67
4.7K
Q3
2N7002W-7-F
HDMI_CTRLCLK
HDMI_CTRLCLK 19
R368
4.7K
R369
4.7K
R370
*0_4
R367
0_4
INT_LVDS_EDIDDATA
DDC_DATA
Q5
R81
4.7K
HDMI_CTRLDATA
HDMI_CTRLDATA 19
NOTE: ACCESS TO STRAP_DATA and I2C_CLK PINS IS MANDATORY.
PU by internal
PD by external
Side-Port Memory Disable
Side-Port Memory Enable (Default)
Bypassing EEPROM, use default values (Default)
Using EEPROM Strapping
Set PCI-E GPP mode to Conf. E
Select PCI-E GPP mode
Use default values (Default)
Use the memory data bus for debug bus output
QUANTA COMPUTER
Title
RS690T-LVDS
Size
Document Number
MGD
Rev
1A
Date: Tuesday, October 23, 2007
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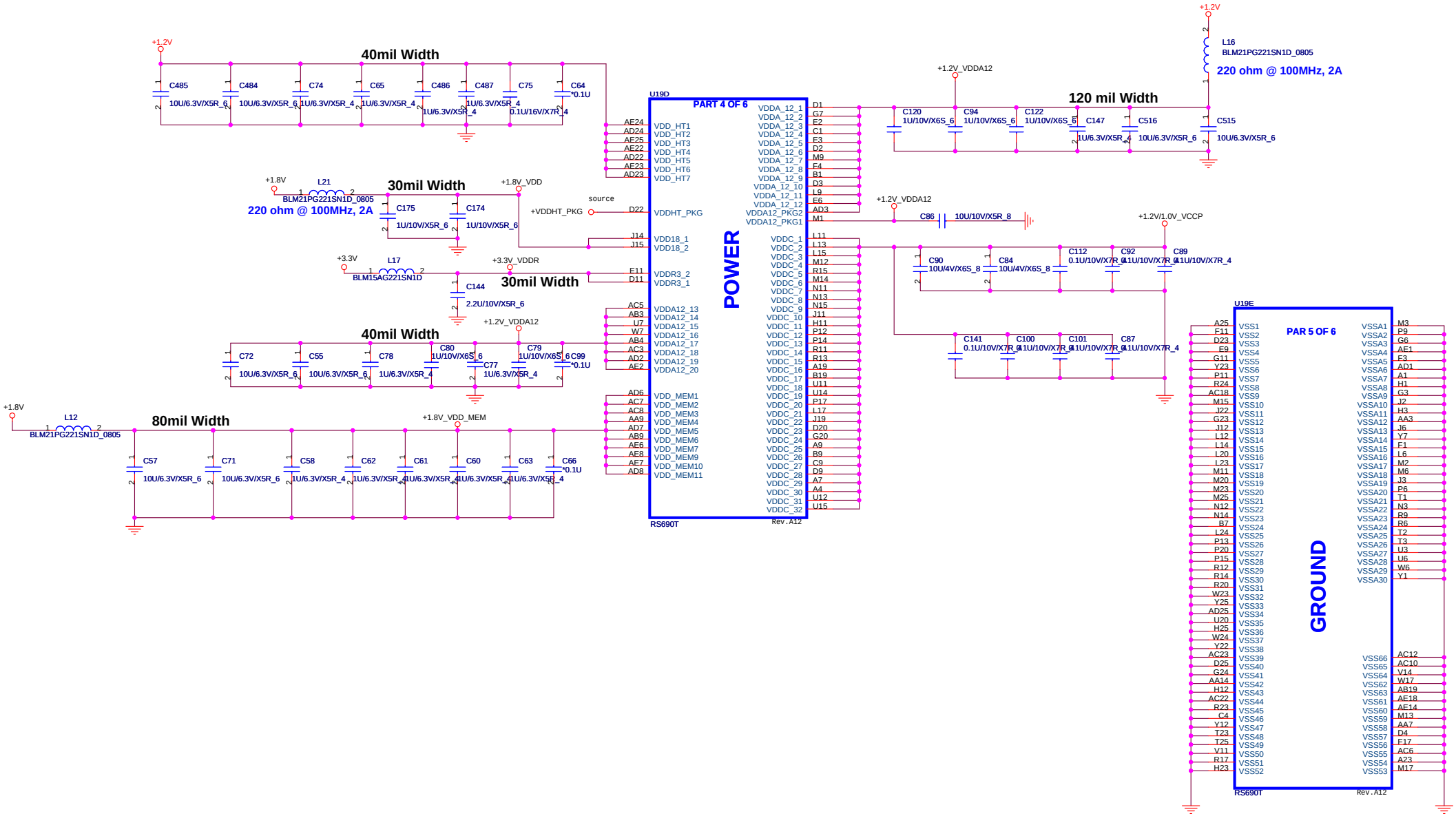

QUANTA COMPUTER

Title	RS690T-POWER	
Size	Document Number MGD	Rev 1A
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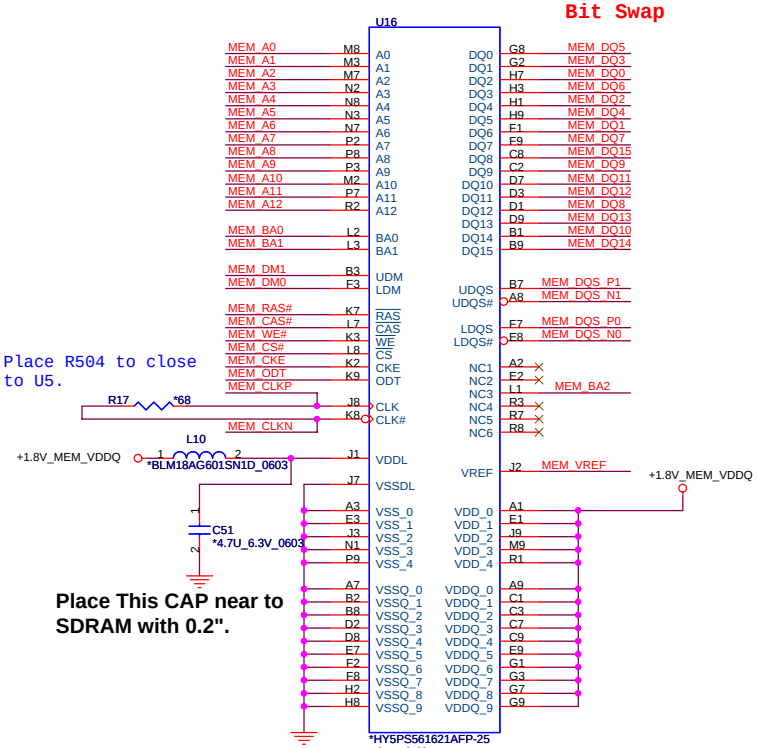
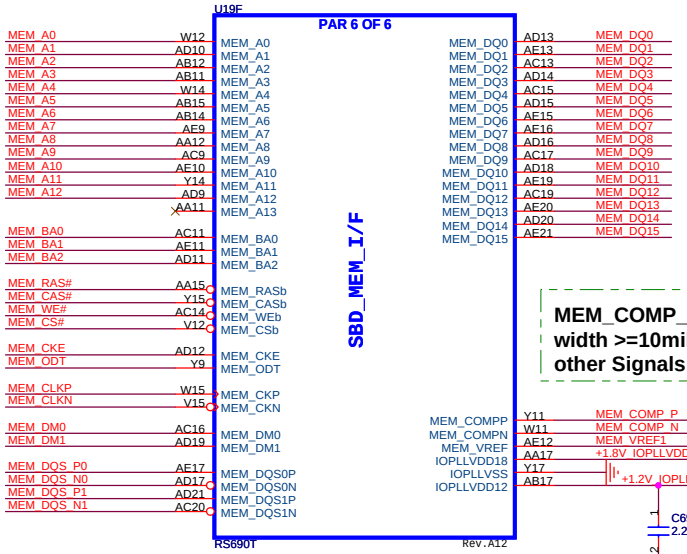
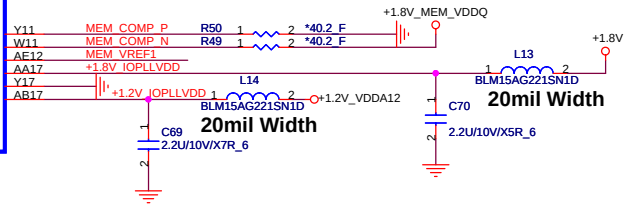
Bit Swap

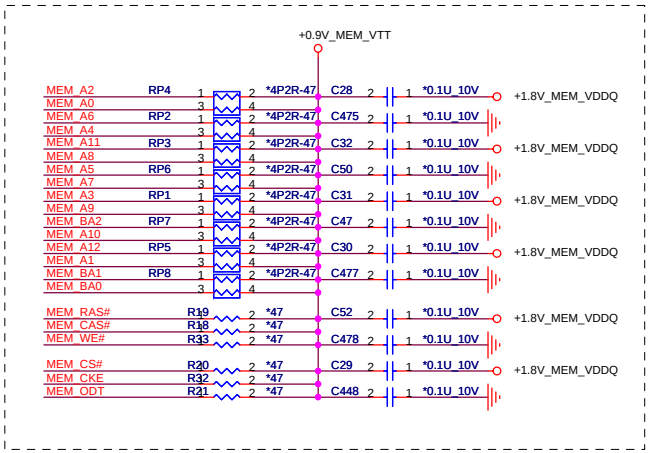


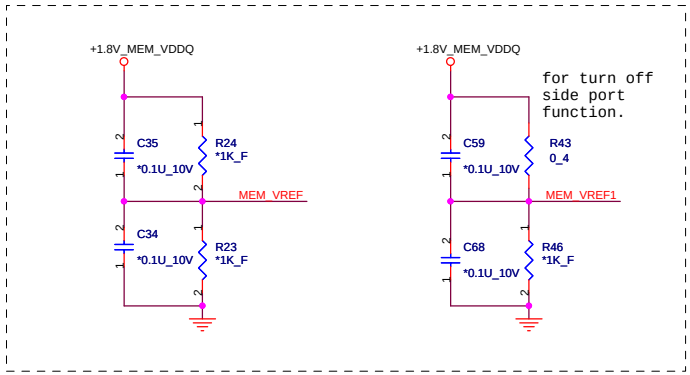
256-Mbit DDR2 16Mbit*16(4bank)

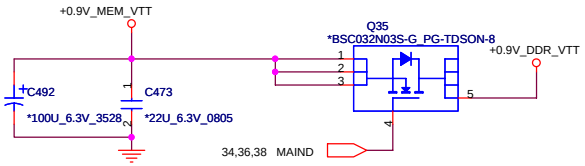


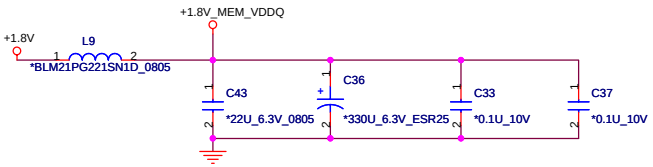
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions











Local Frame Buffer(64MB) DDRII Power

QUANTA COMPUTER

Title	RS690T-SIDE PORT I/O	
Size	Document Number MGD	Rev 1A
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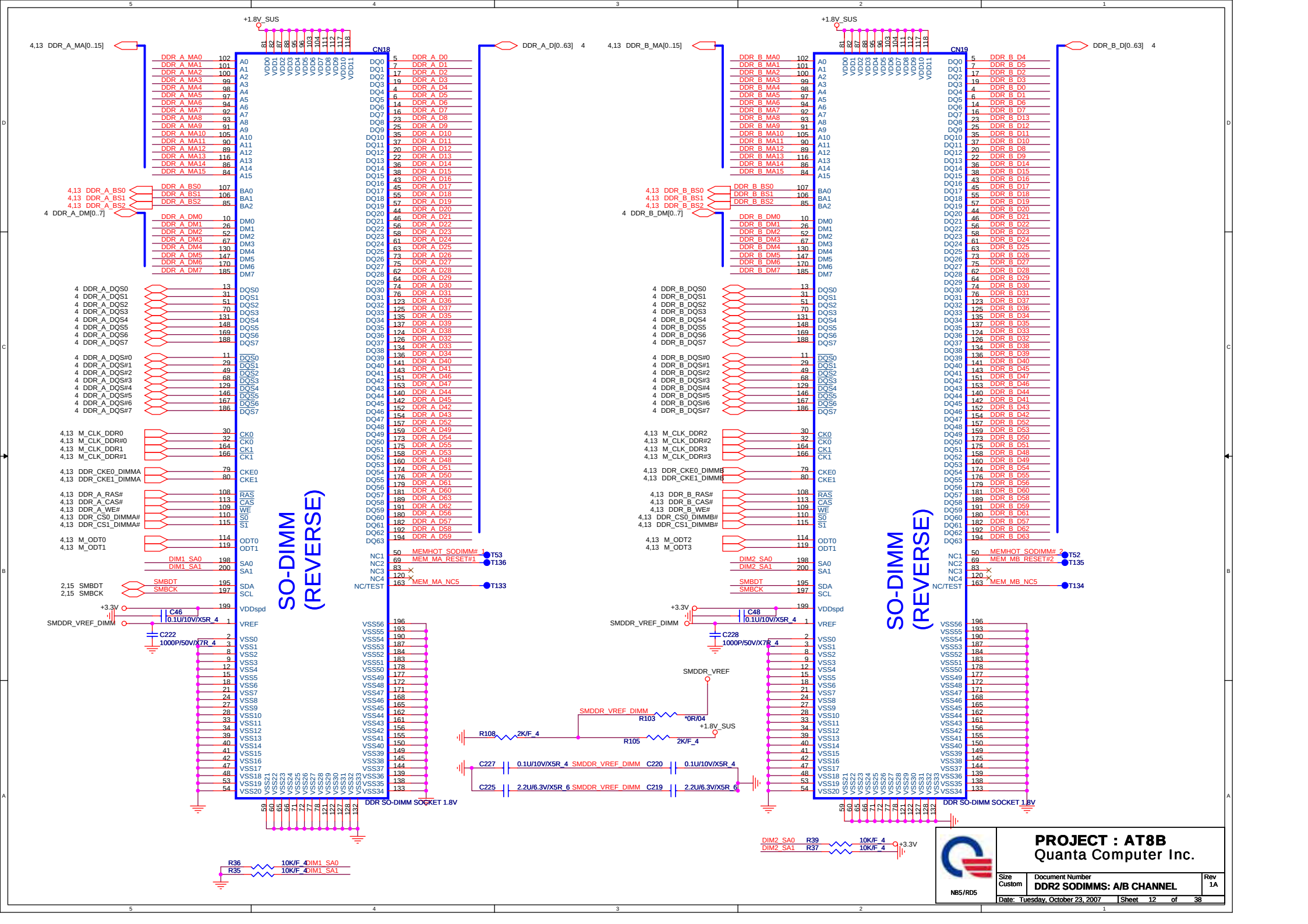
+1.8V_SUS
CN18
CN19
SO-DIMM (REVERSE)
DDR SO-DIMM SOCKET 1.8V
4,13 DDR_A_MA[0..15]
4,13 DDR_B_MA[0..15]
DDR_A_D[0..63] 4
DDR_B_D[0..63] 4
4,13 DDR_A_BS0
4,13 DDR_A_BS1
4,13 DDR_A_BS2
4 DDR_A_DM[0..7]
4,13 DDR_B_BS0
4,13 DDR_B_BS1
4,13 DDR_B_BS2
4 DDR_B_DM[0..7]
4 DDR_A_DQS0
4 DDR_A_DQS1
4 DDR_A_DQS2
4 DDR_A_DQS3
4 DDR_A_DQS4
4 DDR_A_DQS5
4 DDR_A_DQS6
4 DDR_A_DQS7
4 DDR_A_DQS#0
4 DDR_A_DQS#1
4 DDR_A_DQS#2
4 DDR_A_DQS#3
4 DDR_A_DQS#4
4 DDR_A_DQS#5
4 DDR_A_DQS#6
4 DDR_A_DQS#7
4 DDR_B_DQS0
4 DDR_B_DQS1
4 DDR_B_DQS2
4 DDR_B_DQS3
4 DDR_B_DQS4
4 DDR_B_DQS5
4 DDR_B_DQS6
4 DDR_B_DQS7
4 DDR_B_DQS#0
4 DDR_B_DQS#1
4 DDR_B_DQS#2
4 DDR_B_DQS#3
4 DDR_B_DQS#4
4 DDR_B_DQS#5
4 DDR_B_DQS#6
4 DDR_B_DQS#7
4,13 M_CLK_DDR0
4,13 M_CLK_DDR#0
4,13 M_CLK_DDR1
4,13 M_CLK_DDR#1
4,13 M_CLK_DDR2
4,13 M_CLK_DDR#2
4,13 M_CLK_DDR3
4,13 M_CLK_DDR#3
4,13 DDR_CKE0_DIMMA
4,13 DDR_CKE1_DIMMA
4,13 DDR_CKE0_DIMMB
4,13 DDR_CKE1_DIMMB
4,13 DDR_A_RAS#
4,13 DDR_A_CAS#
4,13 DDR_A_WE#
4,13 DDR_CS0_DIMMA#
4,13 DDR_CS1_DIMMA#
4,13 DDR_B_RAS#
4,13 DDR_B_CAS#
4,13 DDR_B_WE#
4,13 DDR_CS0_DIMMB#
4,13 DDR_CS1_DIMMB#
4,13 M_ODT0
4,13 M_ODT1
4,13 M_ODT2
4,13 M_ODT3
DIM1_SA0
DIM1_SA1
DIM2_SA0
DIM2_SA1
2,15 SMBDT
2,15 SMBCK
+3.3V
SMDDR_VREF_DIMM
C46 0.1U/10V/X5R_4
C222 1000P/50V/X7R_4
C48 0.1U/10V/X5R_4
C228 1000P/50V/X7R_4
SMDDR_VREF
R103 *0R/04
R105 2K/F_4
R108 2K/F_4
C227 0.1U/10V/X5R_4
C225 2.2U/6.3V/X5R_6
C220 0.1U/10V/X5R_4
C219 2.2U/6.3V/X5R_6
R36 10K/F_4
R35 10K/F_4
R39 10K/F_4
R37 10K/F_4
MEMHOT_SODIMM# 1
MEM_MA_RESET#1
MEM_MA_NC5
MEMHOT_SODIMM# 2
MEM_MB_RESET#2
MEM_MB_NC5
T53
T136
T133
T52
T135
T134
NB5/RD5
PROJECT : AT8B
Quanta Computer Inc.
Size Custom
Document Number
DDR2 SODIMMS: A/B CHANNEL
Rev 1A
Date: Tuesday, October 23, 2007
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4,12 DDR_A_MA[0..15] — DDR_A_MA[0..15]
4,12 DDR_A_BS[0..2] — DDR_A_BS[0..2]

4,12 DDR_B_MA[0..15] — MEM_MB_ADD[0..15]
4,12 DDR_B_BS[0..2] — DDR_B_BS[0..2]

+0.9V_DDR_VTT

4,12 DDR_CKE0_DIMMA	DDR_CKE0_DIMMA	RP33	47R_4P2R	C131	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_BS2				
	DDR_A_MA12	RP30	47R_4P2R	C165	0.1U/10V/X5R_4
	DDR_A_MA9				
	DDR_A_MA8	RP25	47R_4P2R	C85	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_MA5				
	DDR_A_MA3	RP22	47R_4P2R	C170	0.1U/10V/X5R_4
	DDR_A_MA1				
	DDR_A_MA10	RP17	47R_4P2R	C162	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_BS0				
4,12 DDR_A_WE#	DDR_A_WE#	RP13	47R_4P2R	C111	0.1U/10V/X5R_4
4,12 DDR_A_CAS#	DDR_A_CAS#				
4,12 M_ODT1	M_ODT1	RP9	47R_4P2R	C139	0.1U/10V/X5R_4 +1.8V_SUS
4,12 DDR_CS1_DIMMA#	DDR_CS1_DIMMA#				
	DDR_A_MA15	RP35	47R_4P2R	C119	0.1U/10V/X5R_4
4,12 DDR_CKE1_DIMMA	DDR_CKE1_DIMMA				
	DDR_A_MA7	RP31	47R_4P2R	C185	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_MA14				
	DDR_A_MA6	RP27	47R_4P2R	C96	0.1U/10V/X5R_4
	DDR_A_MA11				
				C164	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_MA2	RP21	47R_4P2R	C88	0.1U/10V/X5R_4
	DDR_A_MA4				
	DDR_A_BS1	RP19	47R_4P2R	C189	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_MA0				
4,12 DDR_CS0_DIMMA#	DDR_CS0_DIMMA#	RP15	47R_4P2R	C191	0.1U/10V/X5R_4
4,12 DDR_A_RAS#	DDR_A_RAS#				
				C163	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_A_MA13	RP12	47R_4P2R	C113	0.1U/10V/X5R_4
4,12 M_ODT0	M_ODT0				

+0.9V_DDR_VTT

4,12 DDR_CKE0_DIMMB	DDR_CKE0_DIMMB	RP34	47R_4P2R	C132	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_BS2				
	DDR_B_MA12	RP28	47R_4P2R	C118	0.1U/10V/X5R_4
	DDR_B_MA9				
	DDR_B_MA8	RP26	47R_4P2R	C178	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_MA5				
	DDR_B_MA3	RP23	47R_4P2R	C102	0.1U/10V/X5R_4
	DDR_B_MA1				
	DDR_B_MA10	RP18	47R_4P2R	C115	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_BS0				
4,12 DDR_B_WE#	DDR_B_WE#	RP14	47R_4P2R	C109	0.1U/10V/X5R_4
4,12 DDR_B_CAS#	DDR_B_CAS#				
4,12 M_ODT3	M_ODT3	RP11	47R_4P2R	C133	0.1U/10V/X5R_4 +1.8V_SUS
4,12 DDR_CS1_DIMMB#	DDR_CS1_DIMMB#				
4,12 DDR_CKE1_DIMMB	DDR_CKE1_DIMMB	RP36	47R_4P2R	C117	0.1U/10V/X5R_4
	DDR_B_MA15				
	DDR_B_MA7	RP32	47R_4P2R	C138	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_MA14				
	DDR_B_MA6	RP29	47R_4P2R	C106	0.1U/10V/X5R_4
	DDR_B_MA11				
				C98	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_MA2	RP24	47R_4P2R	C103	0.1U/10V/X5R_4
	DDR_B_MA4				
	DDR_B_BS1	RP20	47R_4P2R	C121	0.1U/10V/X5R_4 +1.8V_SUS
	DDR_B_MA0				
4,12 DDR_CS0_DIMMB#	DDR_CS0_DIMMB#	RP16	47R_4P2R	C184	0.1U/10V/X5R_4
4,12 DDR_B_RAS#	DDR_B_RAS#				
				C97	0.1U/10V/X5R_4
4,12 M_ODT2	M_ODT2	RP10	47R_4P2R		
	DDR_B_MA13				

4,12 M_CLK_DDR1 — C44 1.5P/50V/NPO_4
4,12 M_CLK_DDR#1
4,12 M_CLK_DDR0 — C527 1.5P/50V/NPO_4
4,12 M_CLK_DDR#0

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

4,12 M_CLK_DDR3 — C45 1.5P/50V/NPO_4
4,12 M_CLK_DDR#3
4,12 M_CLK_DDR2 — C526 1.5P/50V/NPO_4
4,12 M_CLK_DDR#2

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C105 C128 C155 C172 C186 C187 — 0.1U/10V/X5R_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

+1.8V_SUS

C511 C126 C183 C169 C510 C173 — 0.1U/10V/X5R_4

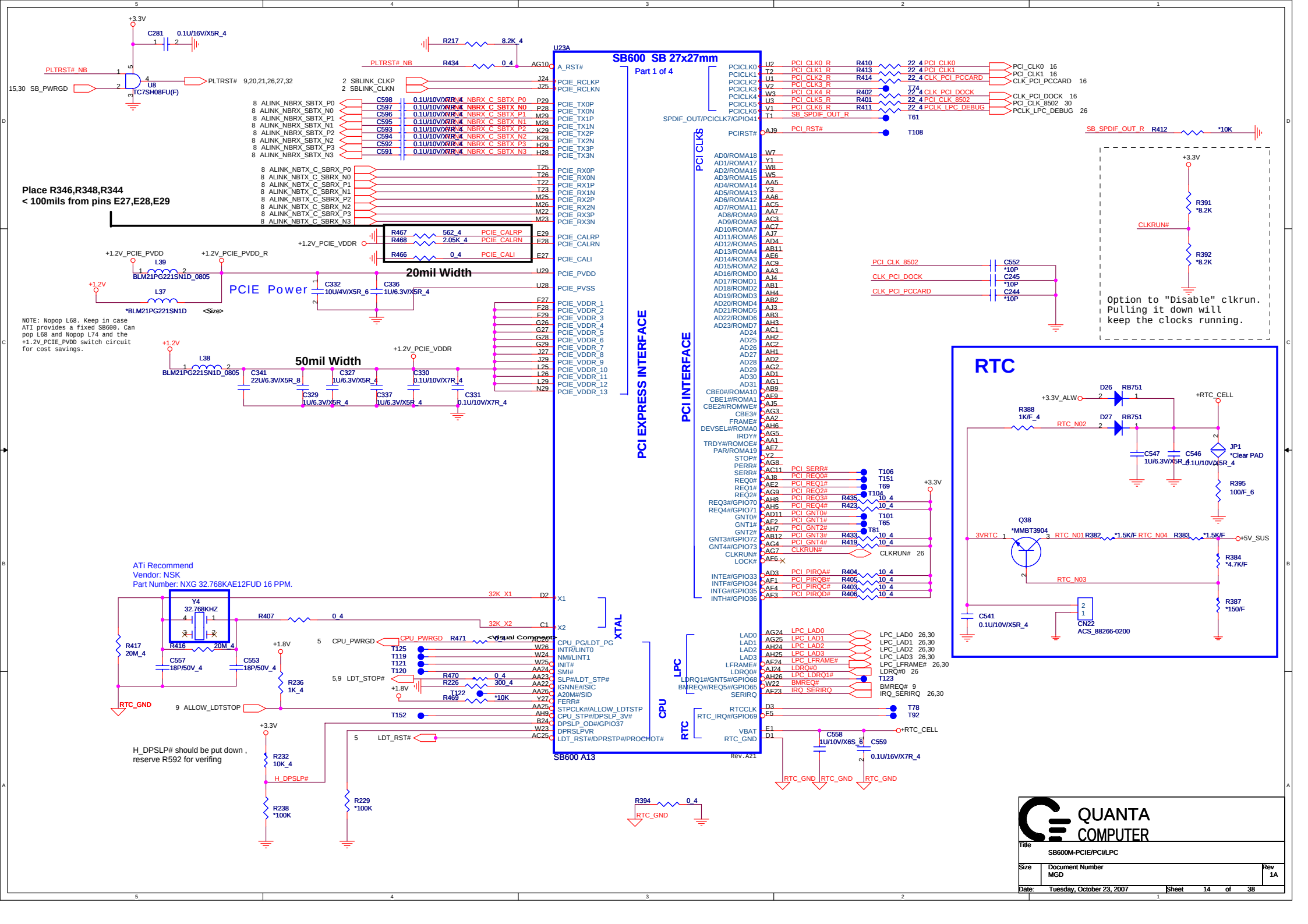
PLACE CLOSE TO SOCKET(PER EMI/EMC)

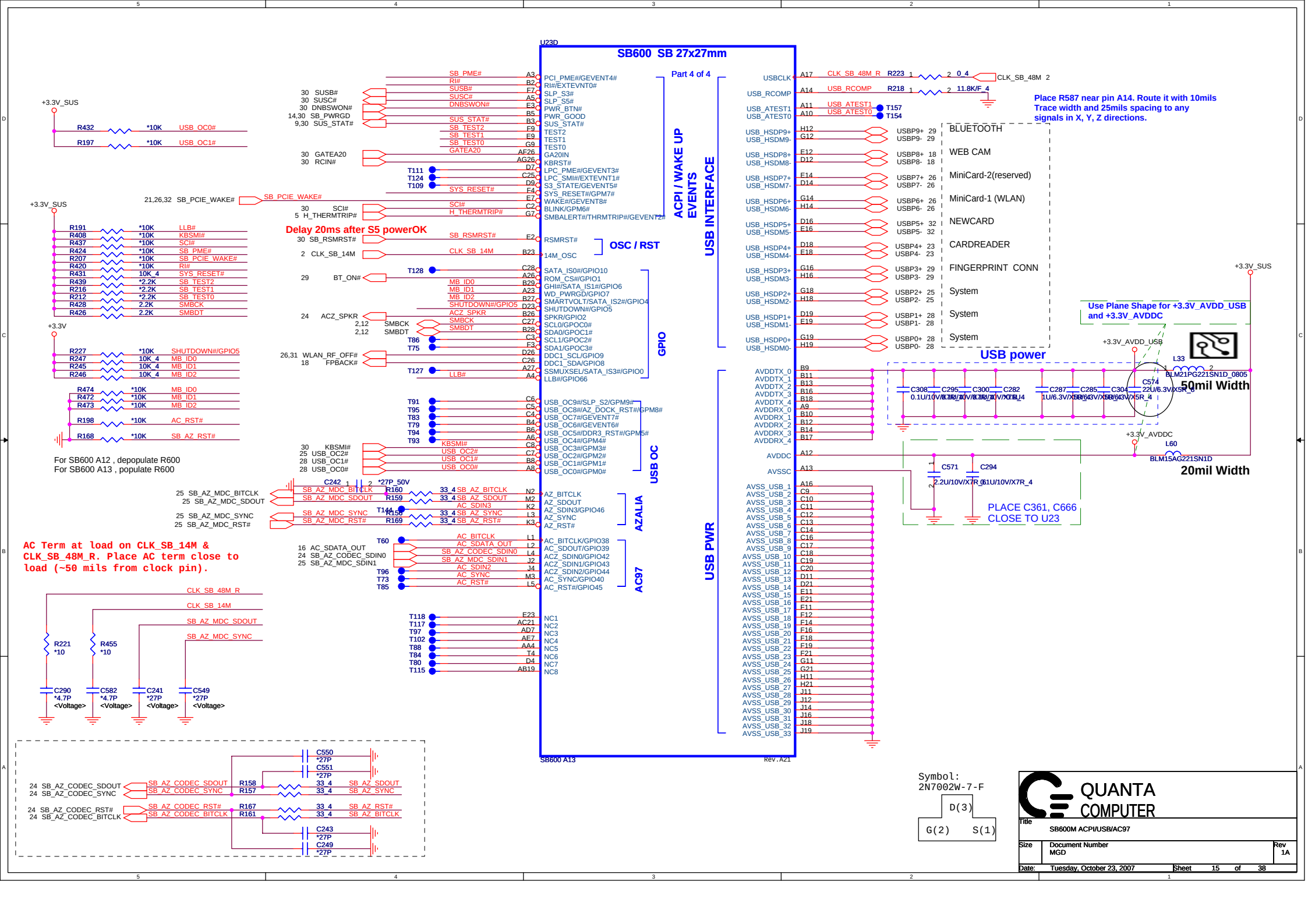
NB5/RD5

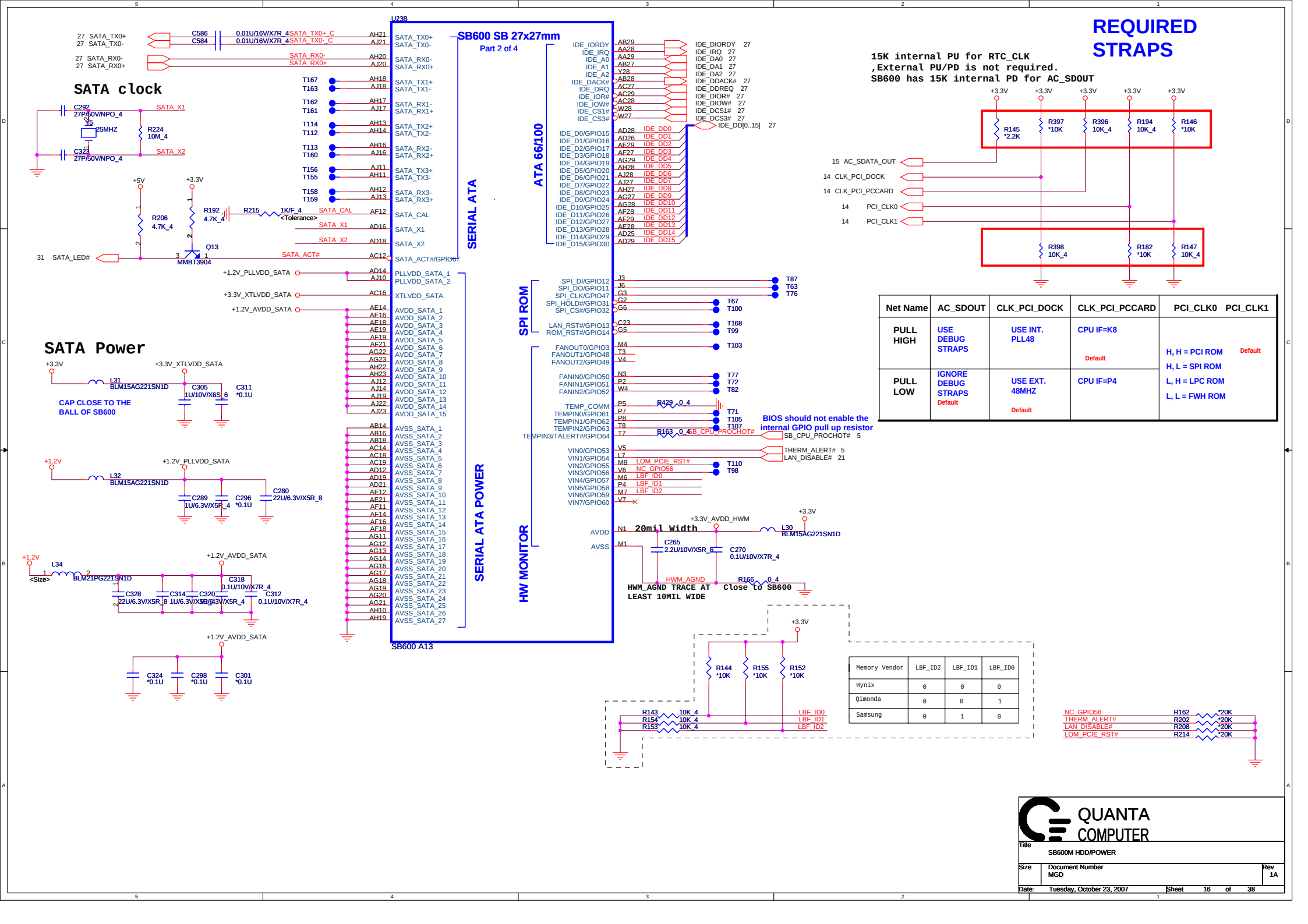
PROJECT : AT8B
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

Date: Tuesday, October 23, 2007 | Sheet 13 of 38


SB600 SB 27x27mm
Part 1 of 4
SB600 A13
PCI EXPRESS INTERFACE
PCI INTERFACE
PCI CLKs
XTAL
LPC
CPU
RTC
Place R346,R348,R344
< 100mils from pins E27,E28,E29
20mil Width
50mil Width
PCIE Power
NOTE: Nopop L68. Keep in case ATI provides a fixed SB600. Can pop L68 and Nopop L74 and the +1.2V_PCIE_PVDD switch circuit for cost savings.
ATi Recommend
Vendor: NSK
Part Number: NXG 32.768KAE12FUD 16 PPM.
H_DPSLP# should be put down , reserve R592 for verifing
RTC
Option to "Disable" clkrun. Pulling it down will keep the clocks running.
QUANTA COMPUTER
Title
SB600M-PCIE/PCI/LPC
Size
Document Number
MGD
Rev
1A
Date: Tuesday, October 23, 2007
Sheet 14 of 38


U23D
SB600 SB 27x27mm
Part 4 of 4
ACPI / WAKE UP EVENTS
USB INTERFACE
GPIO
USB OC
AZALIA
AC97
USB PWR
OSC / RST
SB600 A13
Rev.A21
Delay 20ms after S5 powerOK
AC Term at load on CLK_SB_14M & CLK_SB_48M_R. Place AC term close to load (~50 mils from clock pin).
For SB600 A12 , depopulate R600
For SB600 A13 , populate R600
Place R587 near pin A14. Route it with 10mils Trace width and 25mils spacing to any signals in X, Y, Z directions.
USB power
Use Plane Shape for +3.3V_AVDD_USB and +3.3V_AVDDC
50mil Width
20mil Width
PLACE C361, C666 CLOSE TO U23
BLUETOOTH
WEB CAM
MiniCard-2(reserved)
MiniCard-1 (WLAN)
NEWCARD
CARDREADER
FINGERPRINT CONN
System
System
System
Symbol: 2N7002W-7-F
QUANTA COMPUTER
Title SB600M ACPI/USB/AC97
Size Document Number MGD
Rev 1A
Date: Tuesday, October 23, 2007
Sheet 15 of 38

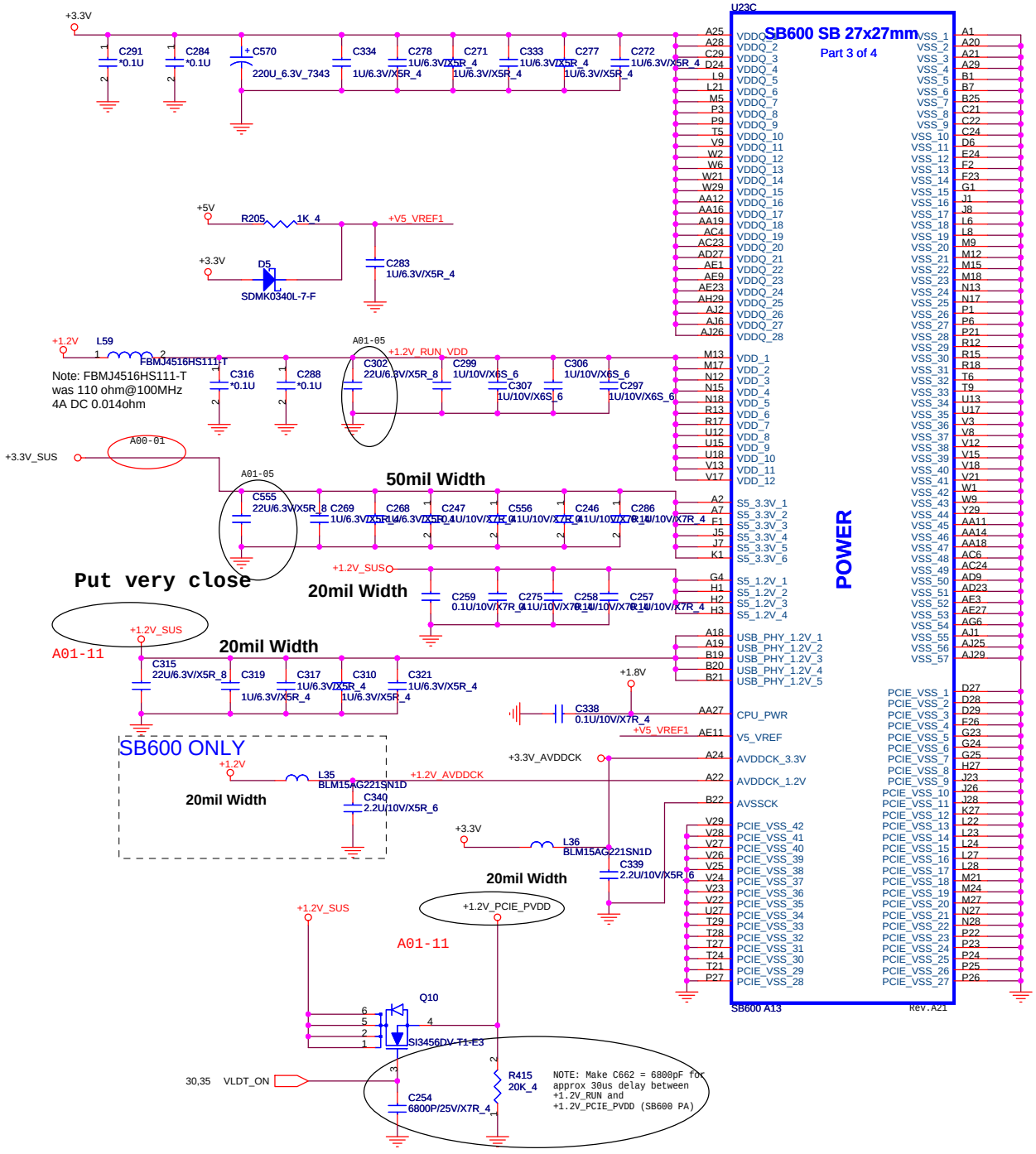


Net Name	AC_SDOUT	CLK_PCI_DOCK	CLK_PCI_PCCARD	PCI_CLK0 PCI_CLK1
PULL HIGH	USE DEBUG STRAPS	USE INT. PLL48	CPU IF=K8 Default	H, H = PCI ROM Default H, L = SPI ROM L, H = LPC ROM L, L = FWH ROM
PULL LOW	IGNORE DEBUG STRAPS Default	USE EXT. 48MHZ Default	CPU IF=P4	

Memory Vendor	LBF_ID2	LBF_ID1	LBF_ID0
Hynix	0	0	0
Qimonda	0	0	1
Samsung	0	1	0

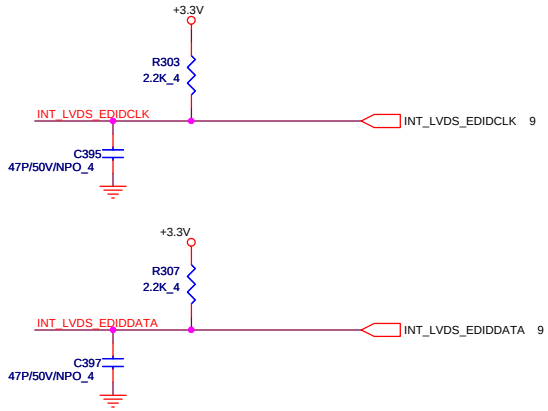
QUANTA COMPUTER

Title	SB600M HDD/POWER	
Size	Document Number MGD	Rev 1A
Date: Tuesday, October 23, 2007	Sheet 16 of 38	

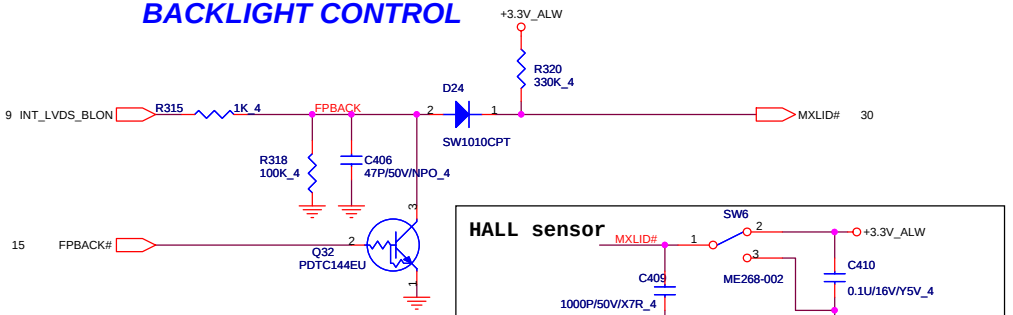


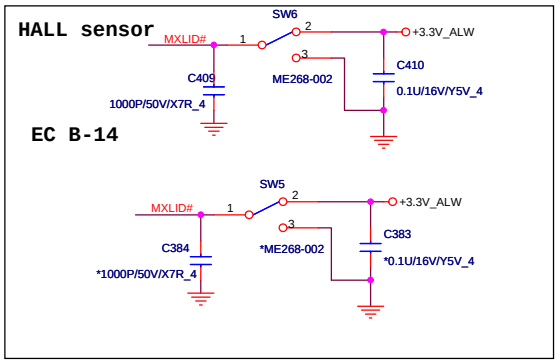
Title	SB600M Power & STRAPS		
Size	Document Number MGD		Rev 1A
Date:	Tuesday, October 23, 2007	Sheet 17 of 38	

QUANTA COMPUTER

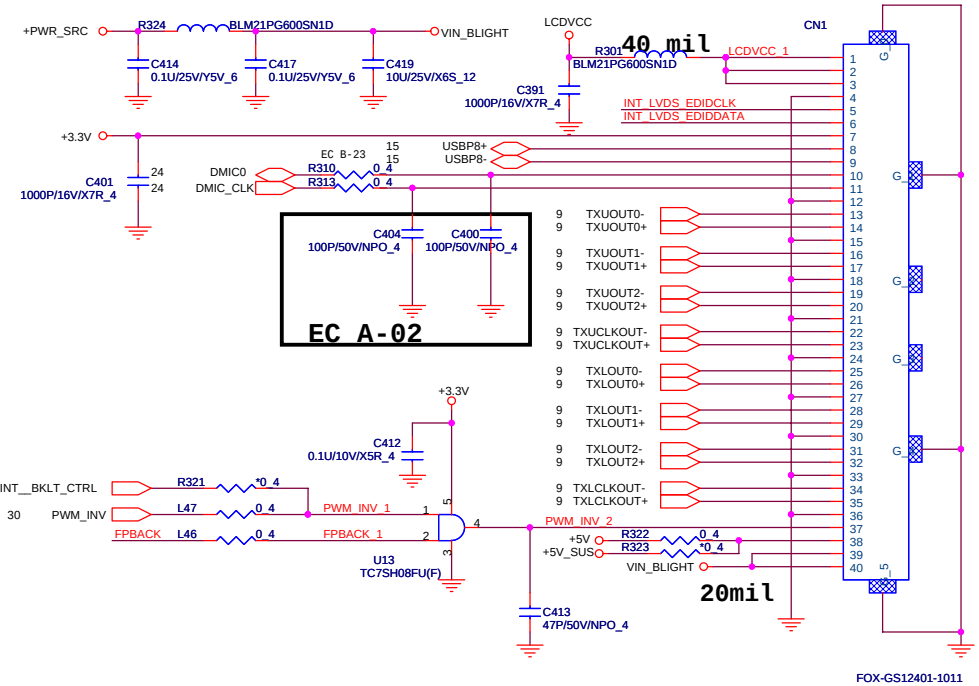


BACKLIGHT CONTROL



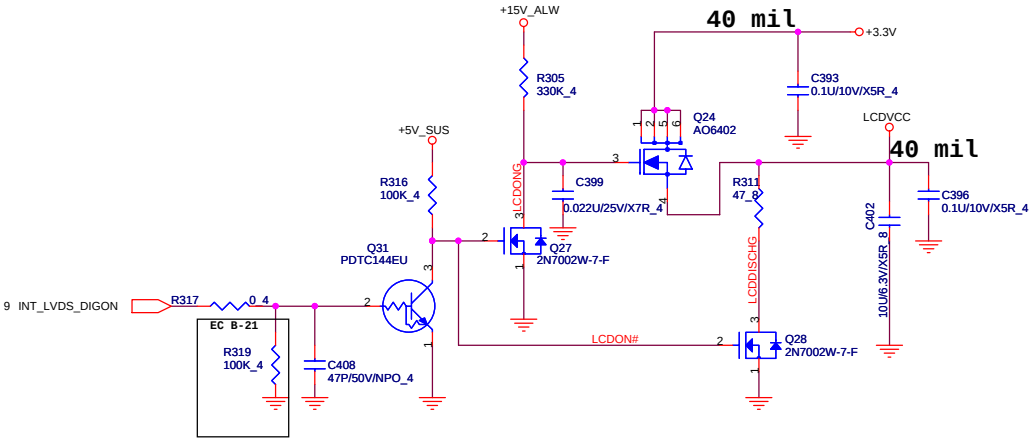


LCD CONNECTOR(Include WEB CAM function)



TO PANEAL

PANEL VCC CONTROL

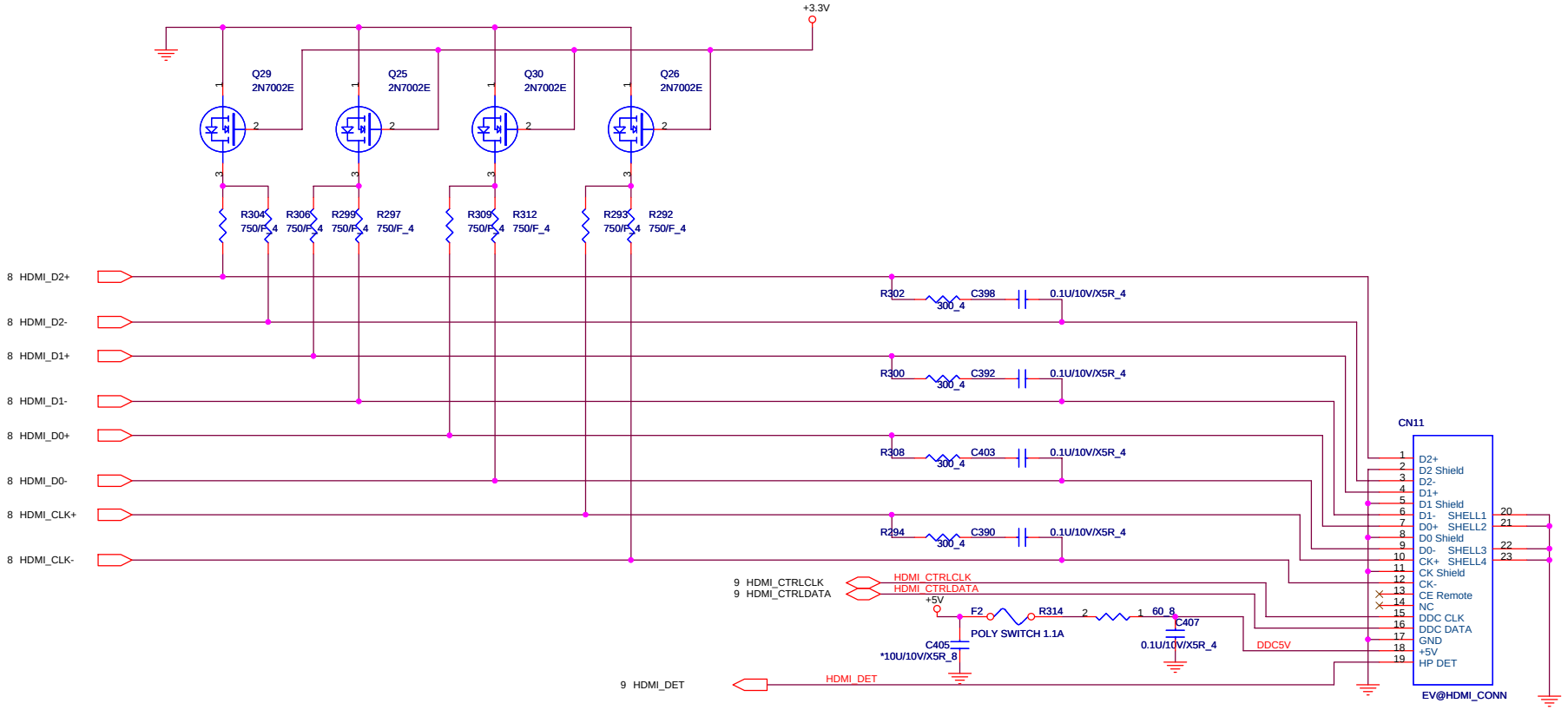


PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	1A

Date: Tuesday, October 23, 2007 Sheet 18 of 38



LAYOUT must support connectors from JAE, Molex, and Acon

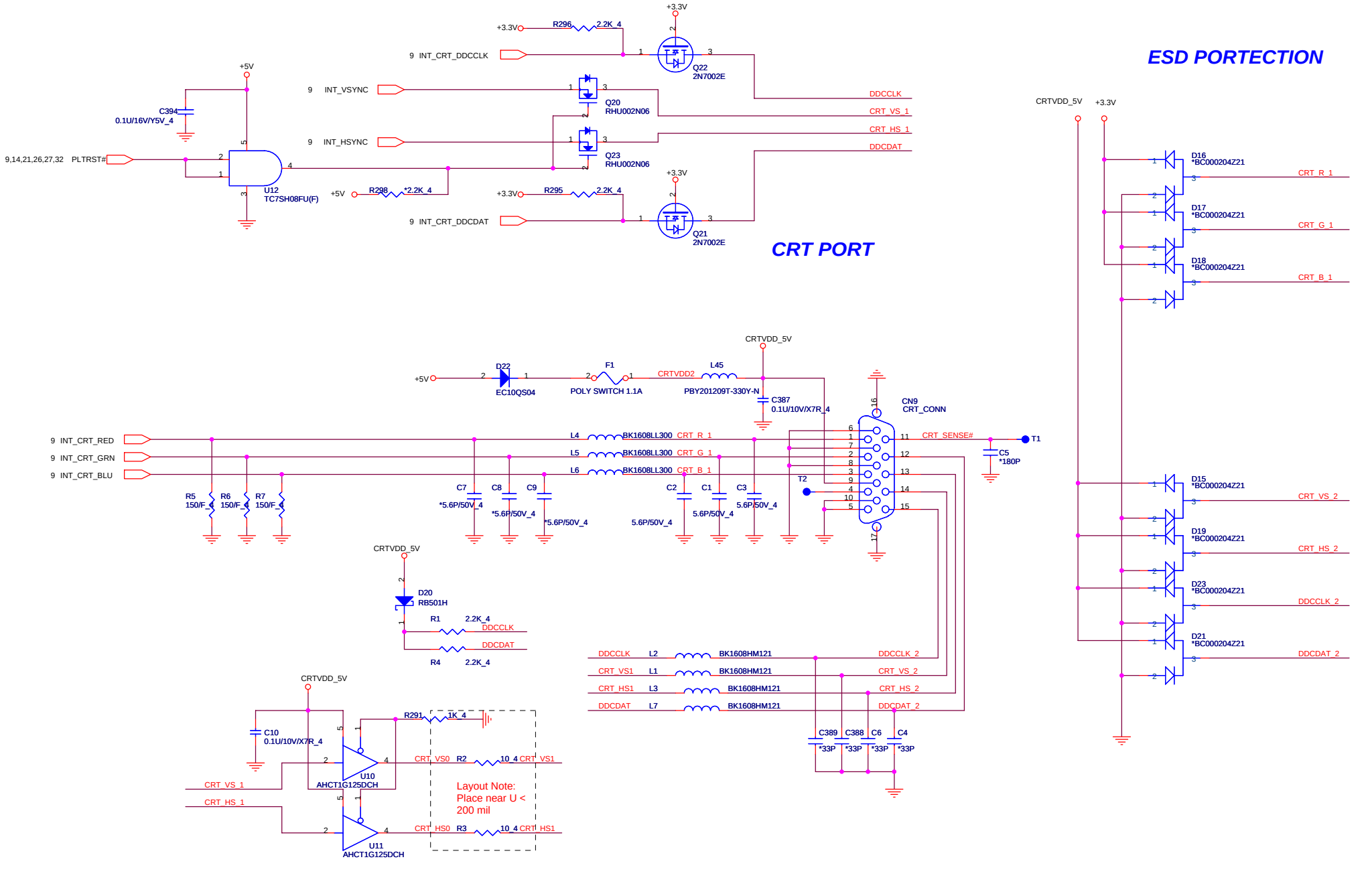
LANCELOT

PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	HDMI	1A

Date: Tuesday, October 23, 2007 Sheet 19 of 38



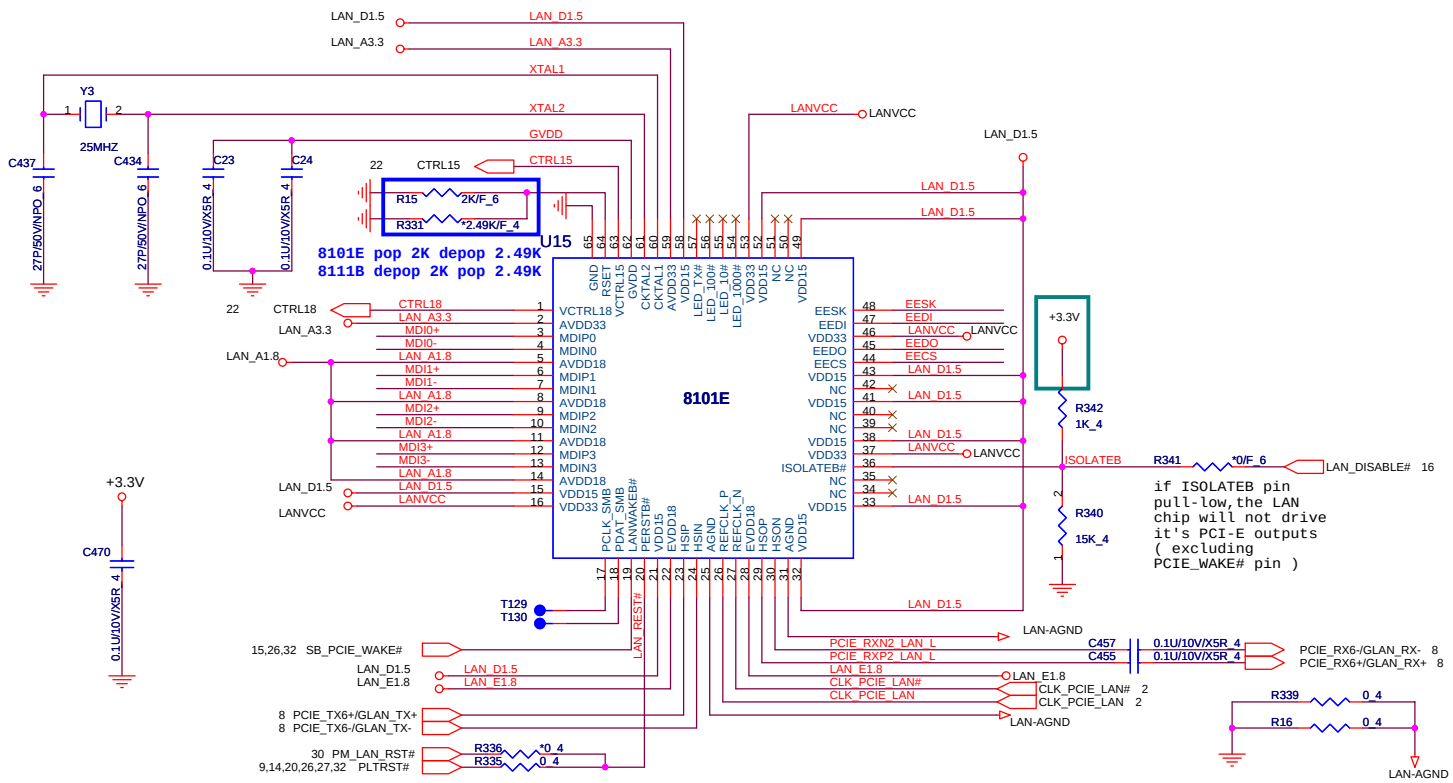
PROJECT : SA1

Quanta Computer Inc.

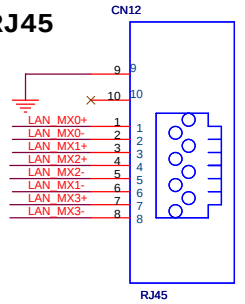
Size	Document Number	Rev
Custom	CRT PORT	1A

Date: Tuesday, October 23, 2007 Sheet 20 of 38

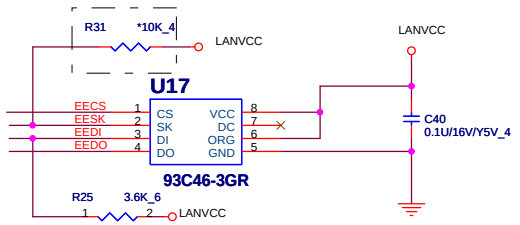
E : Stuffed for 8101E(10/100)

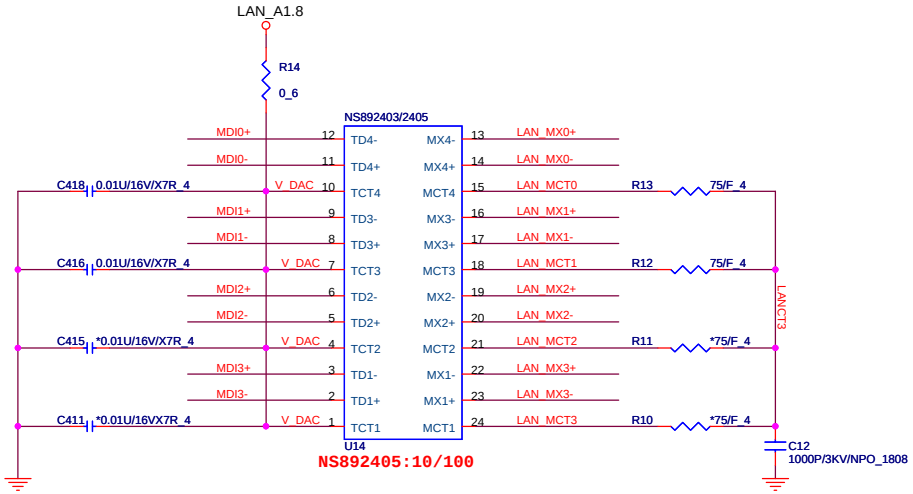


RJ45

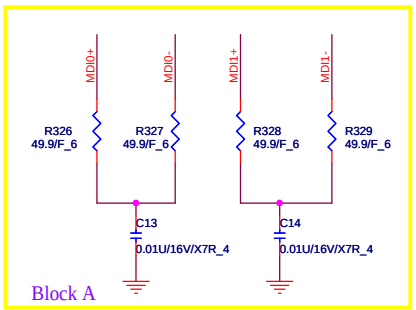


for 93C56 used. NC if 93C46 is used.





BLOCK A is only for RTL8101E application.



	10/100M	1G
R14 R15 R16 R17	ASM	NoASM

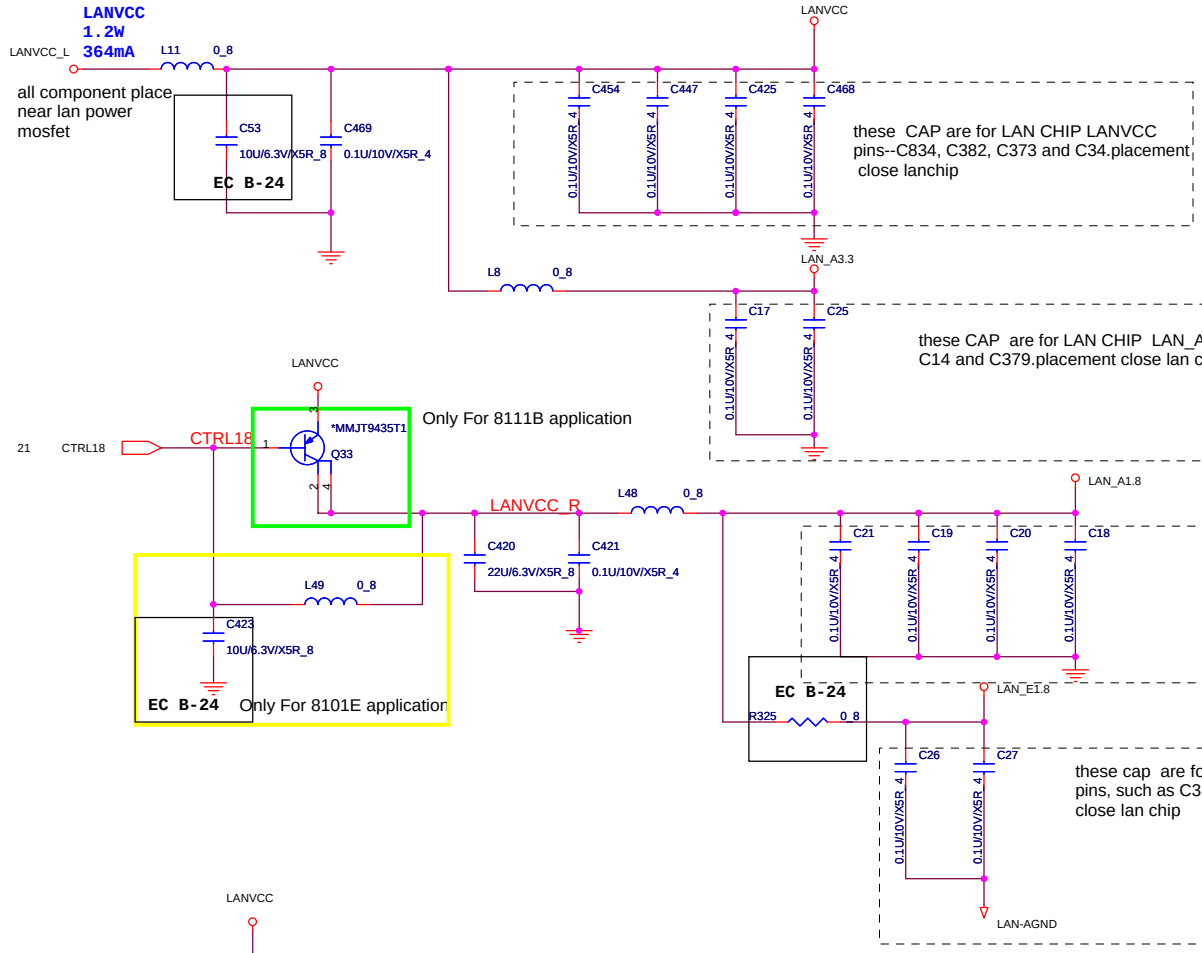
PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN-REALTEK 8101E	1A
Date: Tuesday, October 23, 2007	Sheet 21	of 38

T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



Power domain chart

	RTL8111B / RTL8101E
LANVCC	3.3V
LAN_D1.8	1.8V
LAN_A1.8	1.8V
LAN_D1.5	1.5V

	Q23	Q24
RTL8111B	Need	Need
RTL8101E	N/A	N/A

PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN POWER	1A

Date: Tuesday, October 23, 2007 Sheet 22 of 38

Note:

	SD/MMC	MS	XD
SP0			
SP1	SD_WP		XD_CD#
SP2			
SP3	SD_CD#		
SP4			XD_D4
SP5		MS_BS	XD_D5
SP6	SD_DAT1	MS_D1	XD_D3
SP7	SD_DAT0	MS_D0	XD_D6
SP8	SD_DAT7	MS_D2	XD_D2
SP9		MS_INS#	
SP10	SD_DAT6	MS_D3	XD_D7
SP11	SD_CLK	MS_SCLK	XD_D1
SP12	SD_DAT5		XD_D0
SP13	SD_DAT4		XD_WP#
SP14			XD_R/B#
SP15	SD_DAT3		XD_WE#
SP16	SD_DAT2		XD_RE#
SP17			XD_ALE
SP18			XD_CE#
SP19			XD_CLE

U9

Realtek RTS5158

CF_CD# GPIO0 CF_D10 CF_D9 CF_D2 CF_D8/SM_CD# CF_D1/XD_CD# CF_D0/SM_WPM#/SD_WP CF_A0/SD_CD# CF_DMACK# CF_A1/XD_D4 CF_DMARQ RREF DM DP XTLO XTLI MODE_SEL RST#

XD_CLE/CF_D3 XD_CE#/CF_D11 XD_ALE/CF_D4 SD_DAT2/XD_RE#/CF_D12 SD_DAT3/XD_WE#/CF_D5 XD_RDY/CF_D13 SD_DAT4/XD_WP#/CF_D6 SD_CMD SD_DAT5/XD_D0/CF_D14 SD_CLK/XD_D1/MS_CLK/CF_D7 SD_DAT6/XD_D7/MS_D3/CF_D15 CF_CS0# MS_INS#/CF_IORD# SD_DAT7/XD_D2/MS_D2/CF_IOWR# SD_DAT0/XD_D6/MS_D0/CF_RST# SD_DAT1/XD_D3/MS_D1/CF_IORDY XD_D5/MS_BS/CF_A2

AV_PLL_IN VREG_OUT 5V_IN A3V3_IN D3V3_IN D3V3_OUT A3V3_OUT CARD_3V3_OUT AG33 AG_PLL DGND2 DGND1

R249 6.25K/F_4 RREF
R250 0_4 DM
R251 0_4 DP
USBP4- USBP4+
C349 15P/50V/NPO_6
R244 270K_6
C348 15P/50V/NPO_6
Y2 12MHZ
R234 10K_4
C335 *0.1U/10V_4
R230 100K_4
C326 1U/6.3V/X5R_6
+3.3V_SUS
C352 0.1U/10V/X5R_4
R252 0_4
C343 1U/6.3V/X5R_6
AV_PLL
R253 0_6
+5V_SUS
C313 0.1U/10V/X5R_4
C344 0.1U/10V/X5R_4
C345 0.1U/10V/X5R_4
C351 4.7U/10V/X5R_8
D3V3
C342 0.1U/10V/X5R_4
C303 4.7U/10V/X5R_8
5V to 3V3 as digital power
A3V3
C346 0.1U/10V/X5R_4
C350 4.7U/6.3V/X5R_8
5V to 3V3 as analog power
CARD_3V3
C347 1U/6.3V/X5R_6
3.3V Power for all cards

SP0	R233	56_4	SM_CD#
SP1	R190	56_4	XD_CD#
SP2	R181	56_4	SD_WP
SP3	R170	56_4	SD_CD#
SP4	R213	56_4	XD_D4
SP5	R220	56_4	XD_D5/MS_BS
SP6	R222	56_4	SD_DAT1/XD_D3/MS_D1
SP7	R209	56_4	SD_DAT0/XD_D6/MS_D0
SP8	R225	56_4	SD_DAT7/XD_D2/MS_D2
SP9	R228	56_4	MS_INS#
SP10	R204	56_4	MS_D3/SD_DAT6/XD_D7
SP11	R219	56_4	XD_D1/SD_CLK/MS_SCLK
SP12	R237	56_4	SD_DAT5/XD_D0
SP13	R240	56_4	SD_DAT4/XD_WP#
SP14	R248	56_4	XD_R/B#
SP15	R231	56_4	SD_DAT3/XD_WE#
SP16	R235	56_4	SD_DAT2/XD_RE#
SP17	R241	56_4	XD_ALE
SP18	R243	56_4	XD_CE#
SP19	R242	56_4	XD_CLE

T126

CARD_3V3
C325 0.1U/10V/X5R_4
C309 0.1U/10V/X5R_4
C279 0.1U/10V/X5R_4

7 IN1 CARD-READER (PUSH-PUSH)

Support SD/MS/xD/SM/RS-MMC/MMC/miniSD Cards

CN8

XD_R/B# SD_DAT2/XD_RE# XD_CE# XD_CLE XD_ALE SD_DAT3/XD_WE# SD_DAT4/XD_WP# SD_DAT5/XD_D0 XD_D1/SD_CLK/MS_SCLK SD_DAT2/XD_RE# SD_DAT3/XD_WE# SD_CMD MS_INS# SD_DAT7/XD_D2/MS_D2 SD_DAT0/XD_D6/MS_D0

XD-R/B XD-RE XD-CE XD-CLE XD-ALE XD-WE XD-WP XD-D0 XD-D1 SD-DAT2 SD-DAT3 SD-CMD 4IN1-GND1 MS-VCC MS-SCLK MS-DATA3 MS-INS MS-DATA2 MS-DATA0

MS-DATA1 MS-BS 4IN1-GND2 SD-VCC SD-CLK SD-DAT0 XD-D2 XD-D3 XD-D4 SD-DAT1 XD-D5 XD-D6 XD-D7 XD-VCC XD-CD-SW SD-WP-SW SD-CD-SW

SHIELD1-GND SHIELD2-GND SHIELD3-GND SHIELD4-GND

SD_DAT1/XD_D3/MS_D1 XD_D5/MS_BS XD_D1/SD_CLK/MS_SCLK SD_DAT0/XD_D6/MS_D0 SD_DAT7/XD_D2/MS_D2 SD_DAT1/XD_D3/MS_D1 XD_D4 SD_DAT1/XD_D3/MS_D1 XD_D5/MS_BS SD_DAT0/XD_D6/MS_D0 MS_D3/SD_DAT6/XD_D7 XD_CD# SD_WP SD_CD#

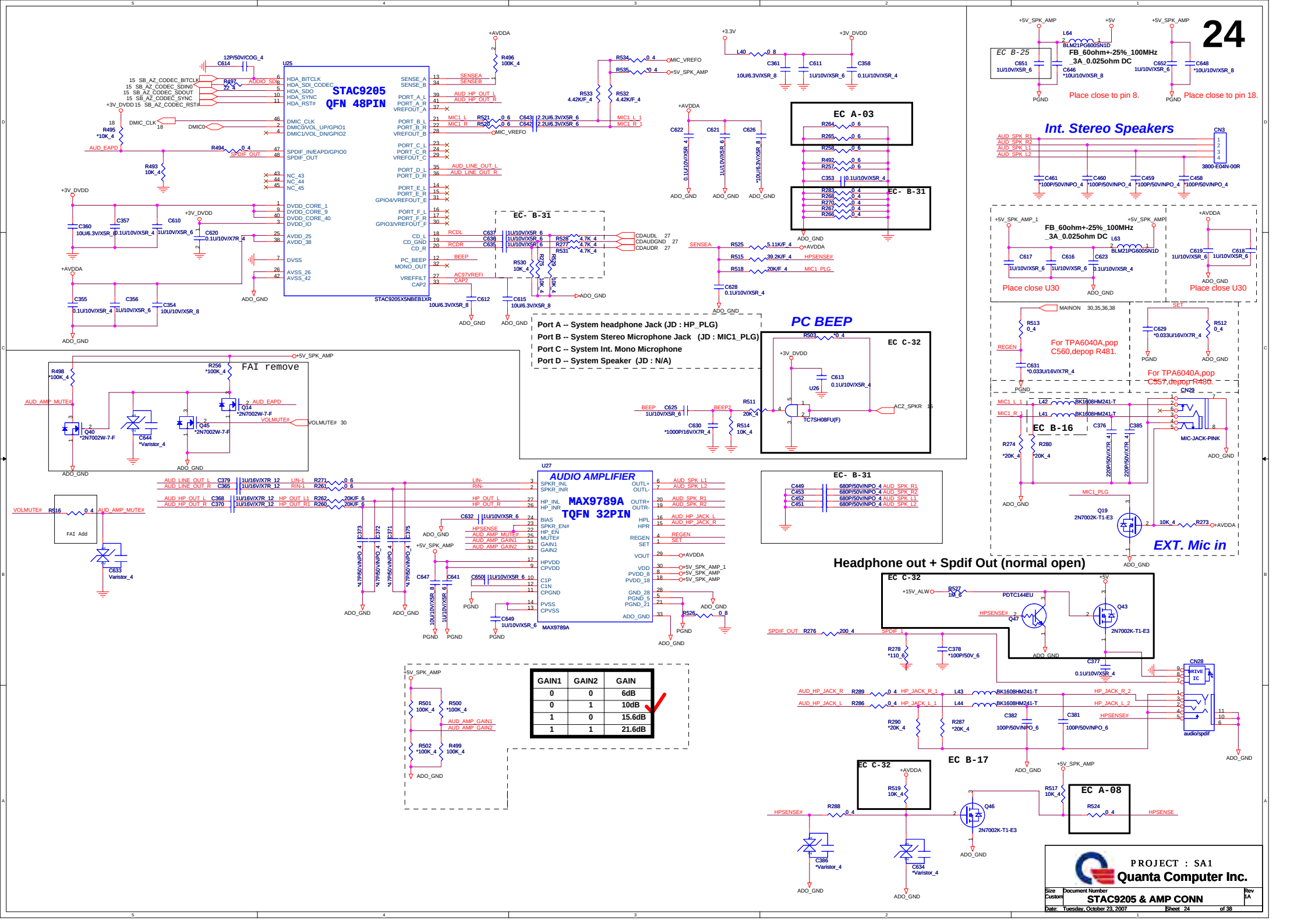
CARD_3V3 R193 *10K
C293 22P/50V/NPO_4
C322 *270P/50V/06
C264 *270P/50V/06

R015-212-LM

PROJECT : SA1

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTS5158 CONTROLLER	1A
Date: Tuesday, October 23, 2007	Sheet 23	of 38


STAC9205
QFN 48PIN
STAC9205X5NBEB1XR
EC- B-31
EC A-03
EC- B-31
Port A -- System headphone Jack (JD : HP_PLG)
Port B -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port C -- System Int. Mono Microphone
Port D -- System Speaker (JD : N/A)
PC BEEP
EC C-32
FAI remove
FAI Add
AUDIO AMPLIFIER
MAX9789A
TQFN 32PIN
MAX9789A
EC B-25
FB_60ohm+-25%_100MHz
_3A_0.025ohm DC
Place close to pin 8.
Place close to pin 18.
Int. Stereo Speakers
3800-E04N-00R
FB_60ohm+-25%_100MHz
_3A_0.025ohm DC
Place close U30
Place close U30
For TPA6040A,pop
C560,depop R481.
For TPA6040A,pop
C557,depop R480.
EC B-16
MIC-JACK-PINK
EXT. Mic in
EC- B-31
Headphone out + Spdif Out (normal open)
EC C-32
EC B-17
EC C-32
EC A-08
GAIN1 GAIN2 GAIN
0 0 6dB
0 1 10dB
1 0 15.6dB
1 1 21.6dB
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Quanta Computer Inc.
STAC9205 & AMP CONN
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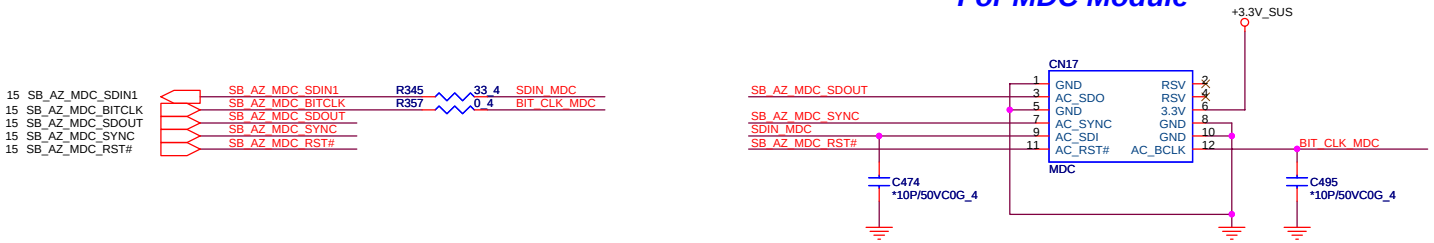
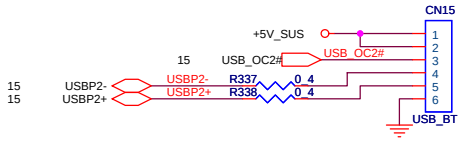
For MDC Module



TO RJ11/USB PORT



PROJECT : SA1		
Quanta Computer Inc.		
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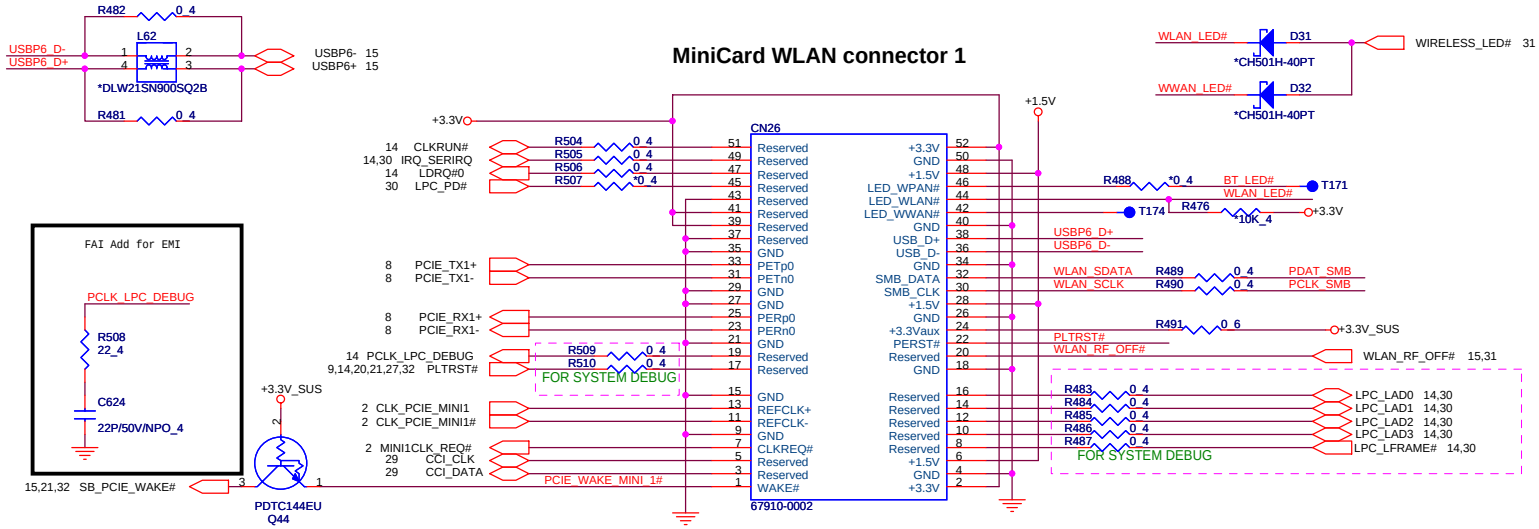
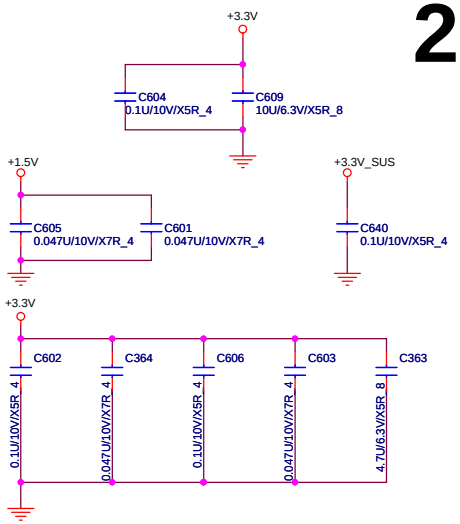
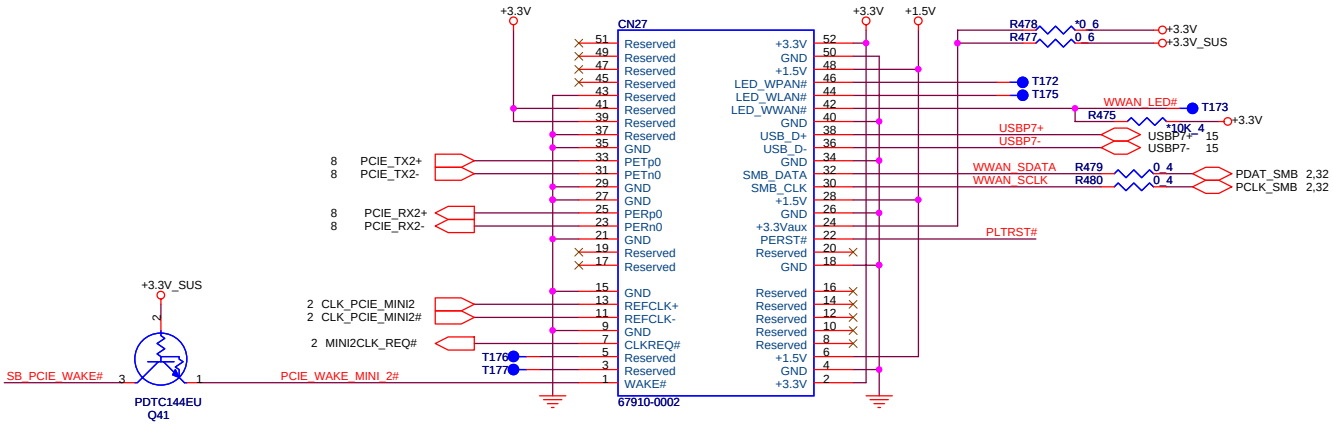
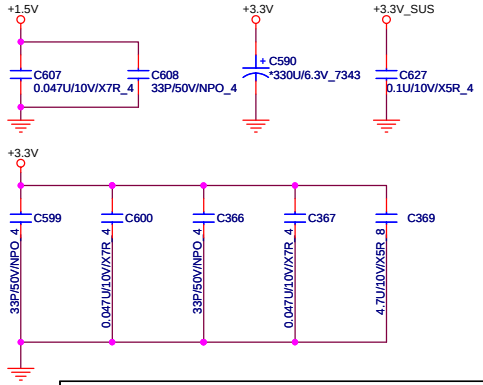
MiniCard WLAN connector 1





MiniCard connector 2





PROJECT : SA1

Quanta Computer Inc.

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Custom	MiniCard connector	1A
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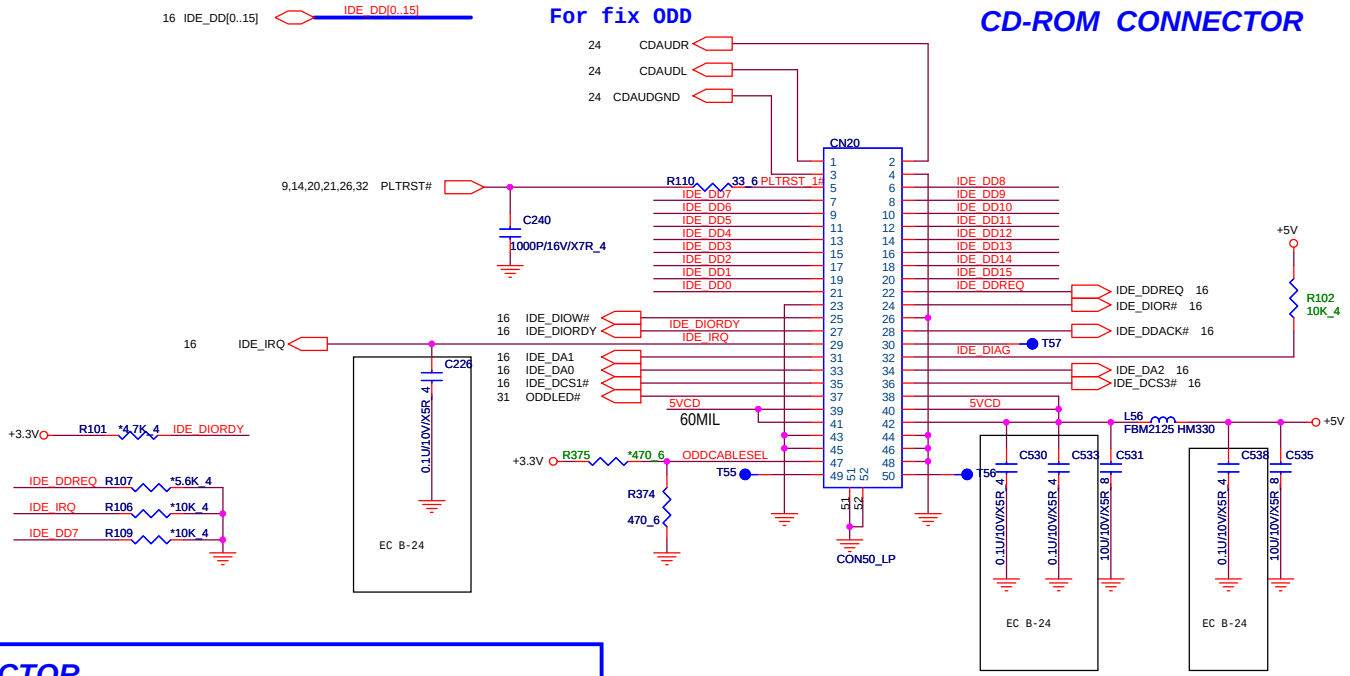
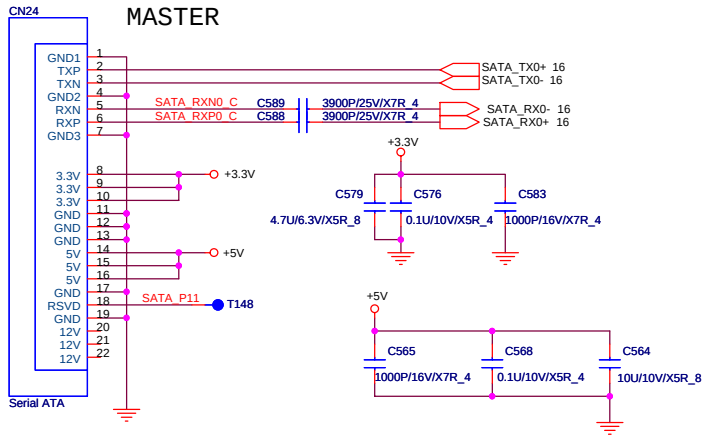
For fix ODD

CD-ROM CONNECTOR



SATA CONNECTOR



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Quanta Computer Inc.

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Custom	SATA HDD,ODD,USB	1A
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NB SCREW HOLE

HOLE12 H-C236D142P2
HOLE17 H-C236D142P2

MINI PCI-E SCREW HOLE 2

HOLE21 H-C236D142P2
HOLE24 H-C236D142P2

MINI PCI-E SCREW HOLE 1

HOLE23 H-C236D142P2
HOLE22 H-C236D142P2

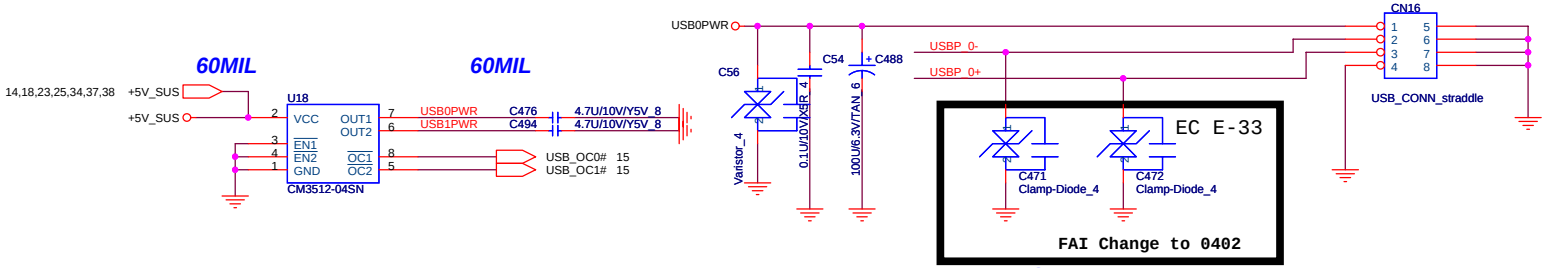
MDC SCREW HOLE

HOLE11 H-C236D142P2
HOLE7 H-TC236BS4D142P2

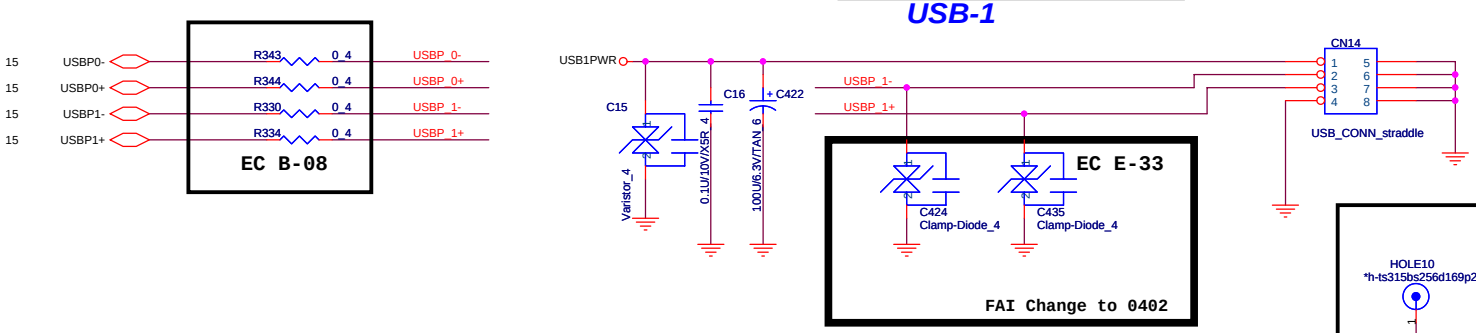
CPU SCREW HOLE

HOLE10 *h-ts315bs256d169p2
HOLE15 *h-ts315bs256d169p2
HOLE9 *h-ts315bs256d169p2
HOLE14 *h-ts315bs256d169p2

USB-0

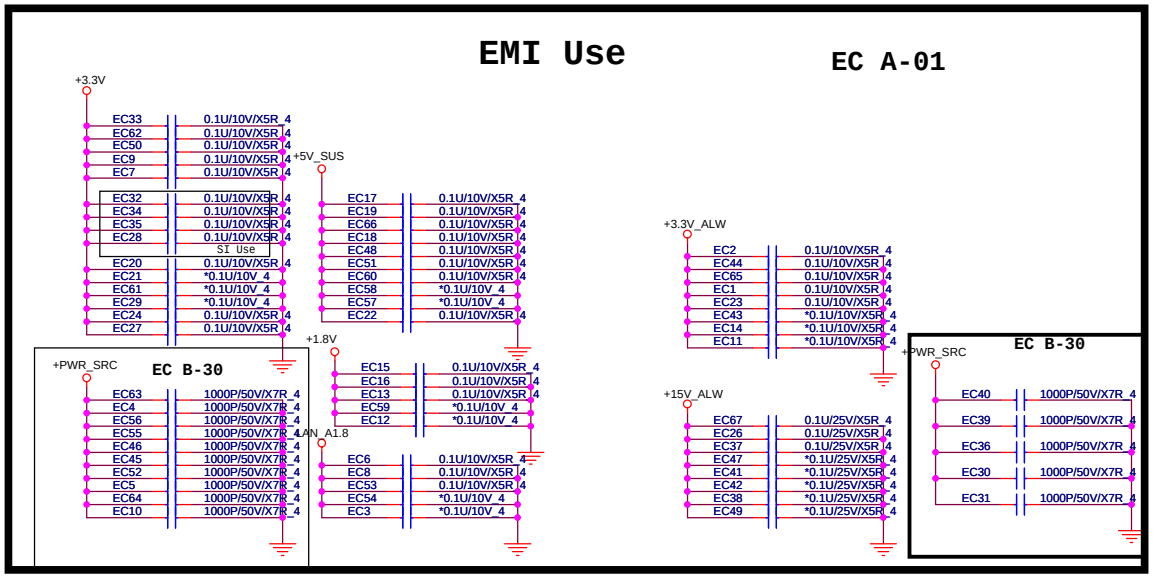


USB-1



EMI Use

EC A-01



HOLE1 *h-ts4bs8d110p2
HOLE2 *h-ts8bs8d110p2
HOLE8 *h-ts1-be354x354d110p2
HOLE6 *h-ts7bs8d110p2
HOLE16 *H-TS354BC280D110P2
HOLE3 *h-c118d118n
HOLE5 *H-C98D98N
HOLE26 *H-TS314BS1D110P2
HOLE27 *h-te433bs354d110p2
HOLE25 *H-TC276BC354D110P2
HOLE4 *h-ts5bs6d110p2
HOLE13 *h-ob355x453d197x295p2
HOLE18 *h-ts2bs2d110p2
HOLE28 *H-C236D110P2
ADO_GND
HOLE20 *h-ts314bs354d119p2
HOLE19 *H-TC276TD110RB

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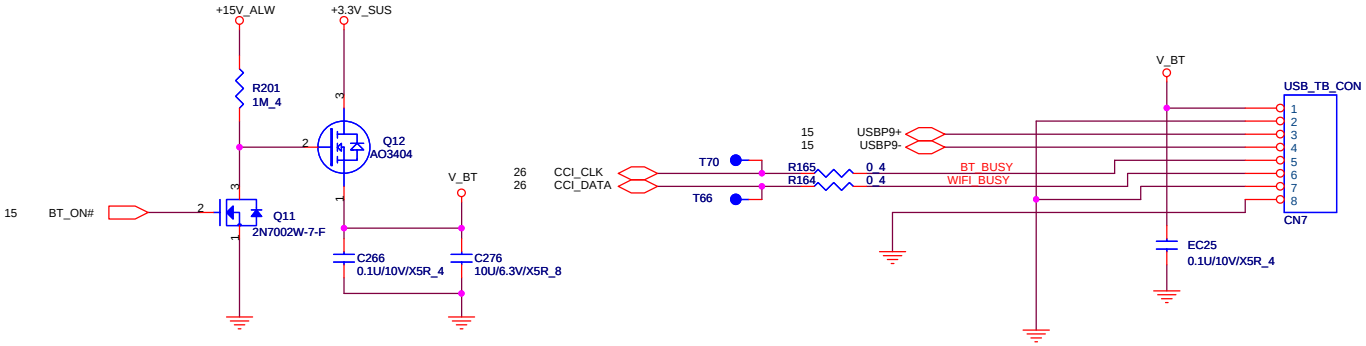
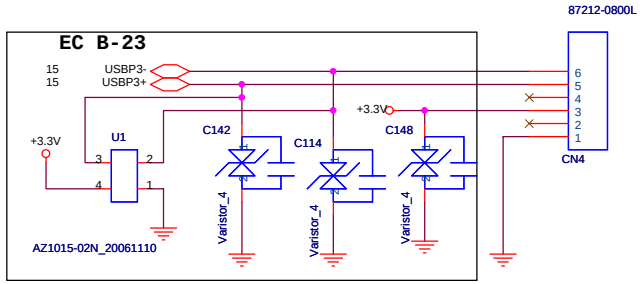
BLUETOOTH CONNECTOR



FINGERPRINT CONNECTOR



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IT8512

POWER SWITCH

RF ON/OFF SLIDE SWITCH

8Mbit (1M Byte), SPI

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
Place all capacitors close to IT8512.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Layout Note:
Place R428,R416,R420 within 500 mils from SPI Flash.

Please reserve this connector for serial debug port & KBS download usage.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

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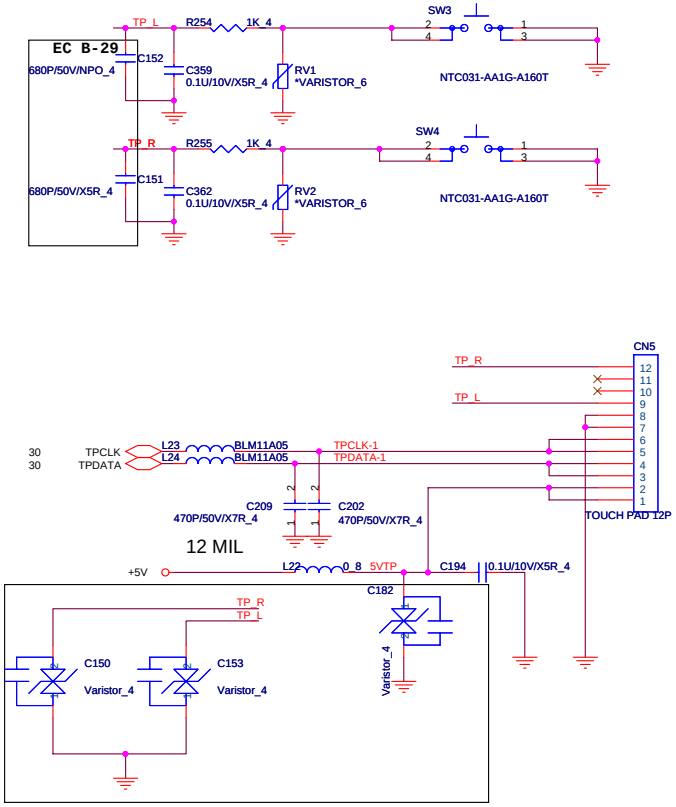
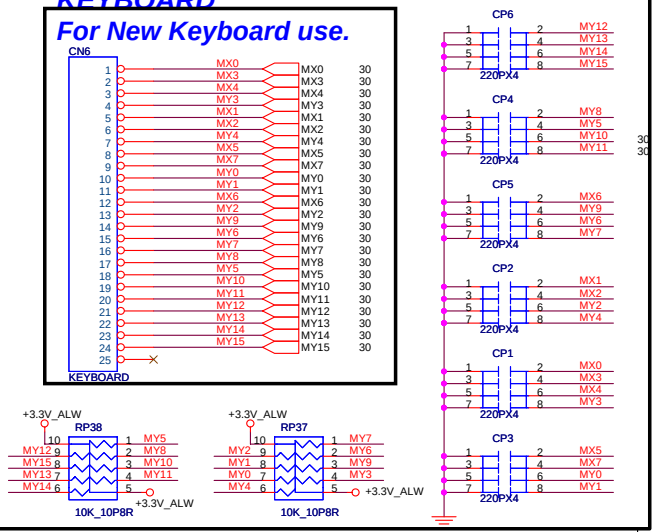
TOUCHPAD SWITCH CONN

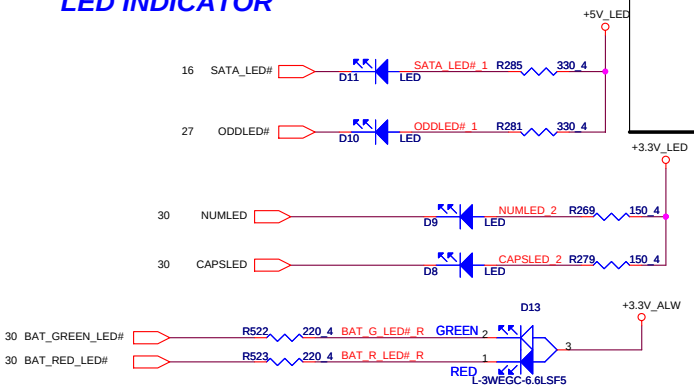


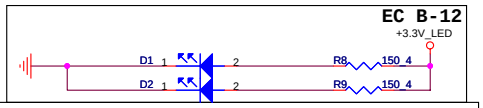
KEYBOARD

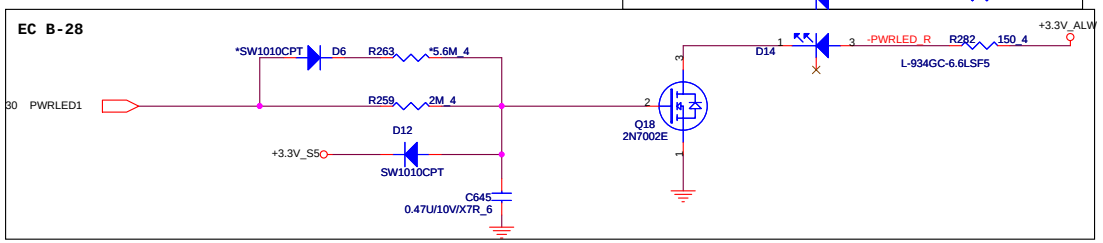
For New Keyboard use.

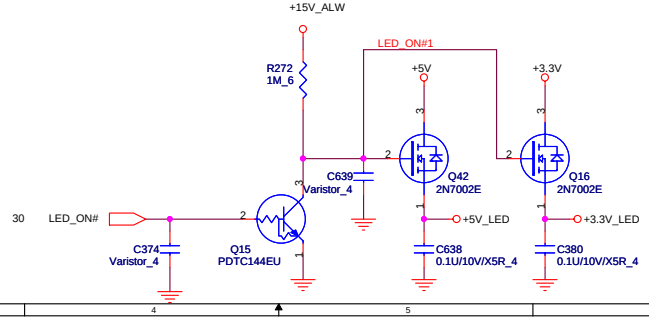


LED INDICATOR

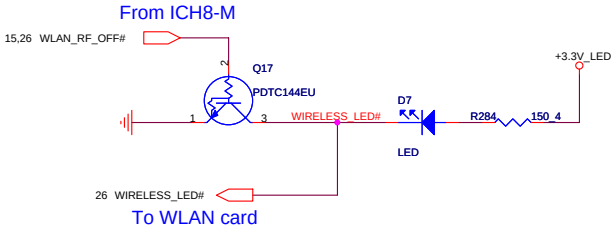


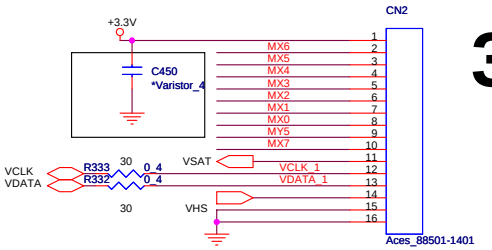


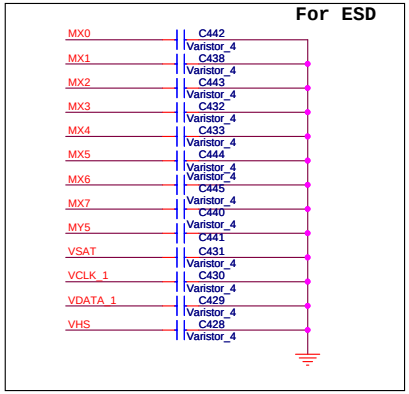




WIRELESS LED







SWITCH/Volume cintral BOARD

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Quanta Computer Inc.

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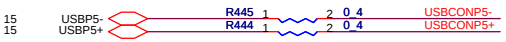
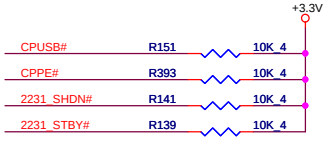
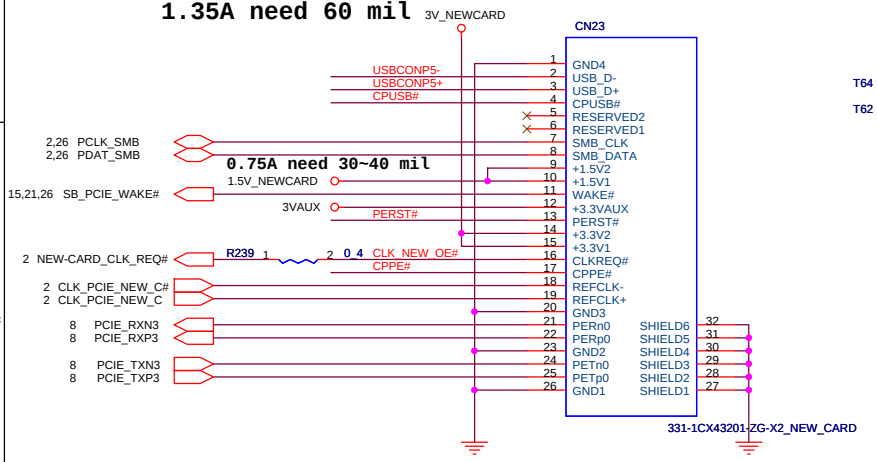
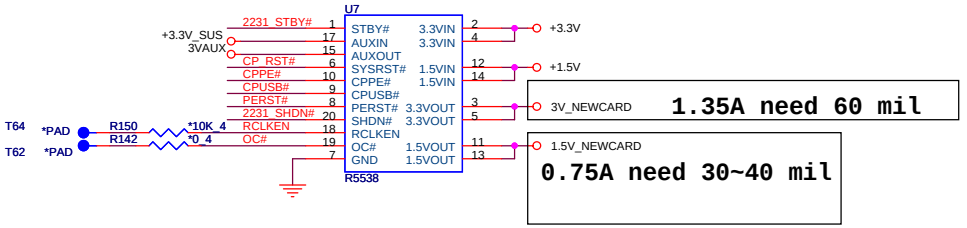
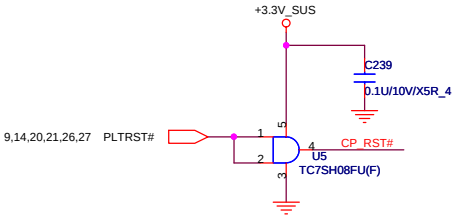
NEWCARD

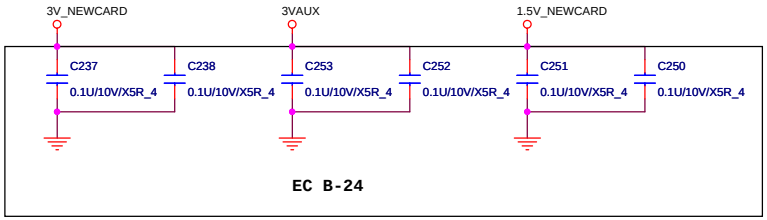












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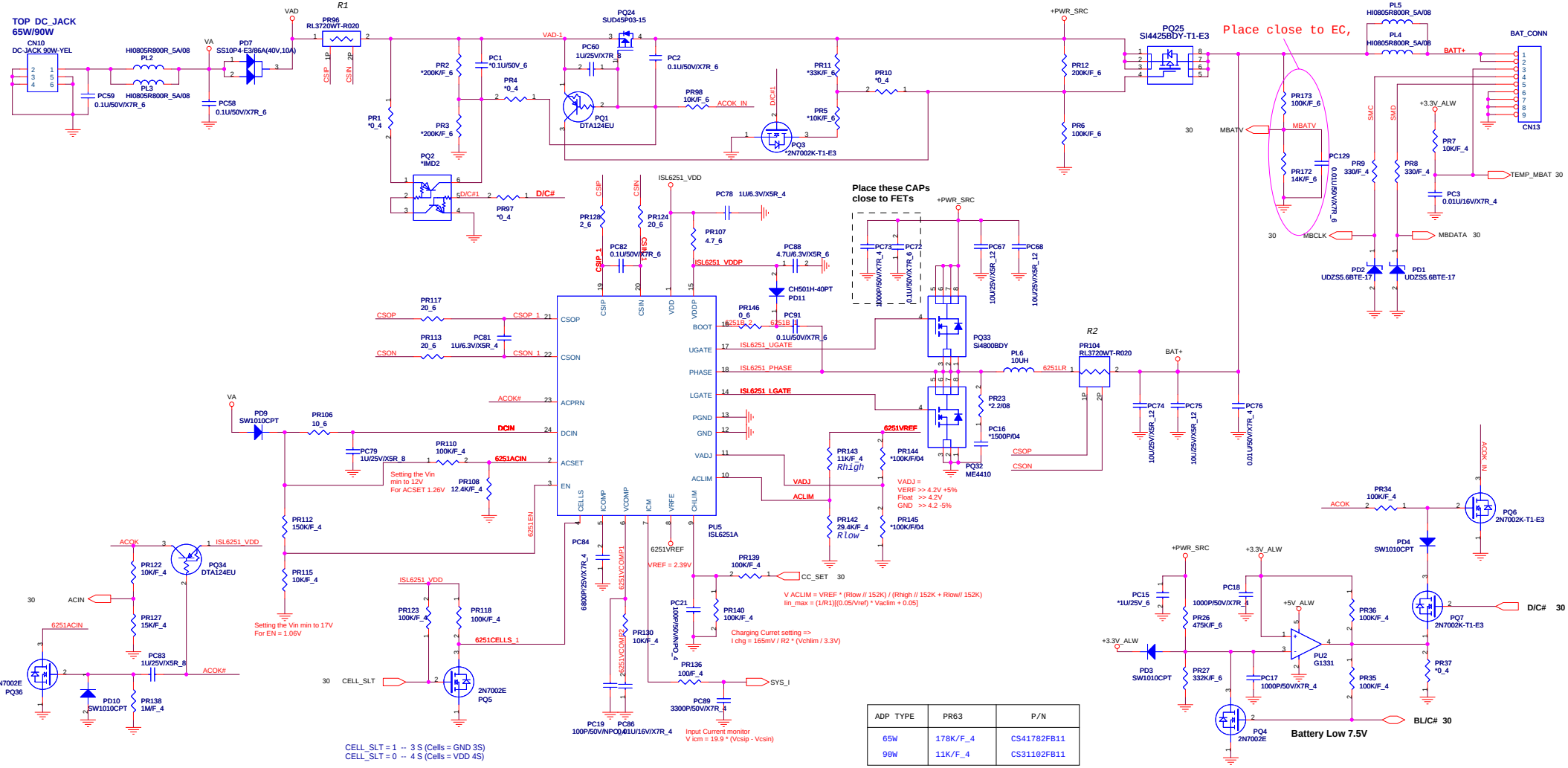
BATTERY CHARGER



ADP TYPE	PR63	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

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Quanta Computer Inc.

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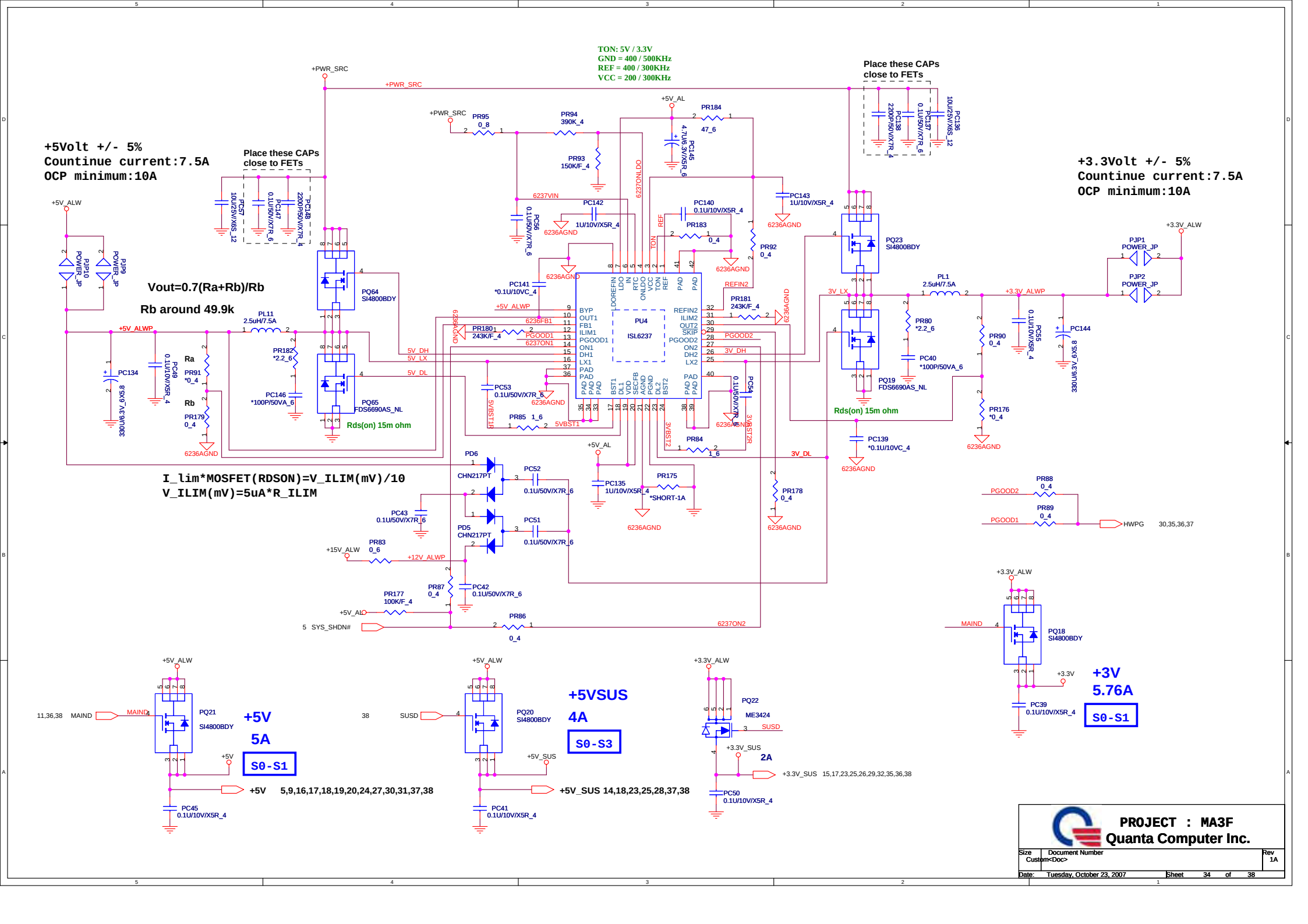
TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz
Place these CAPs close to FETs
+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k
I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM
Rds(on) 15m ohm
PU4
ISL6237
+5V
5A
S0-S1
+5VSUS
4A
S0-S3
+3V
5.76A
S0-S1
2A
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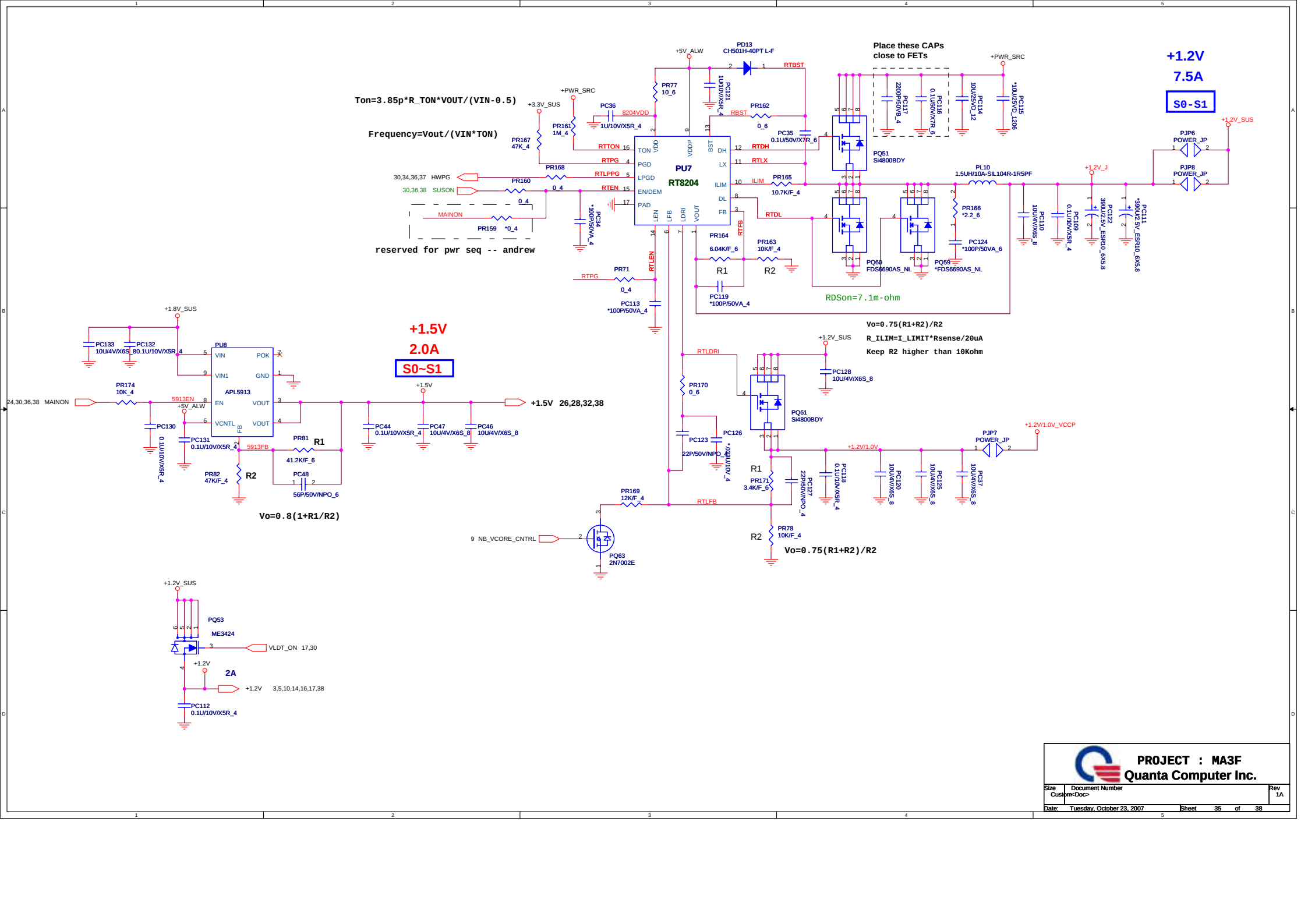
Quanta Computer Inc.


Ton=3.85p*R_TON*VOUT/(VIN-0.5)
Frequency=Vout/(VIN*TON)
reserved for pwr seq -- andrew
Place these CAPs close to FETs
+1.2V
7.5A
S0-S1
PU7
RT8204
PD13
CH501H-40PT L-F
PQ51
Si4800BDY
PL10
1.5UH/10A-SIL104R-1R5PF
PQ60
FDS6690AS_NL
PQ59
*FDS6690AS_NL
RDSon=7.1m-ohm
Vo=0.75(R1+R2)/R2
R_ILIM=I_LIMIT*Rsense/20uA
Keep R2 higher than 10Kohm
+1.5V
2.0A
S0~S1
PU8
APL5913
Vo=0.8(1+R1/R2)
PQ61
Si4800BDY
PQ63
2N7002E
Vo=0.75(R1+R2)/R2
PQ53
ME3424
2A
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1A
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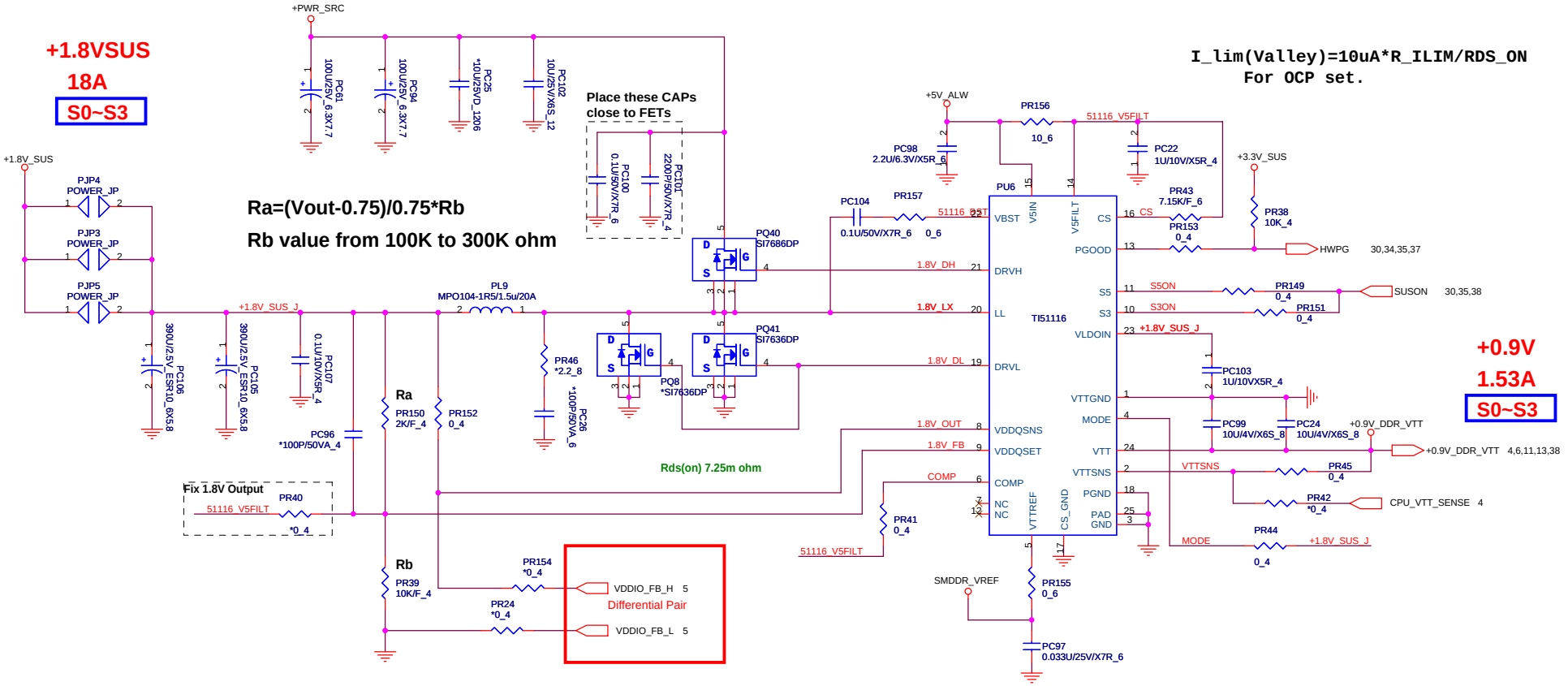

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Quanta Computer Inc.		
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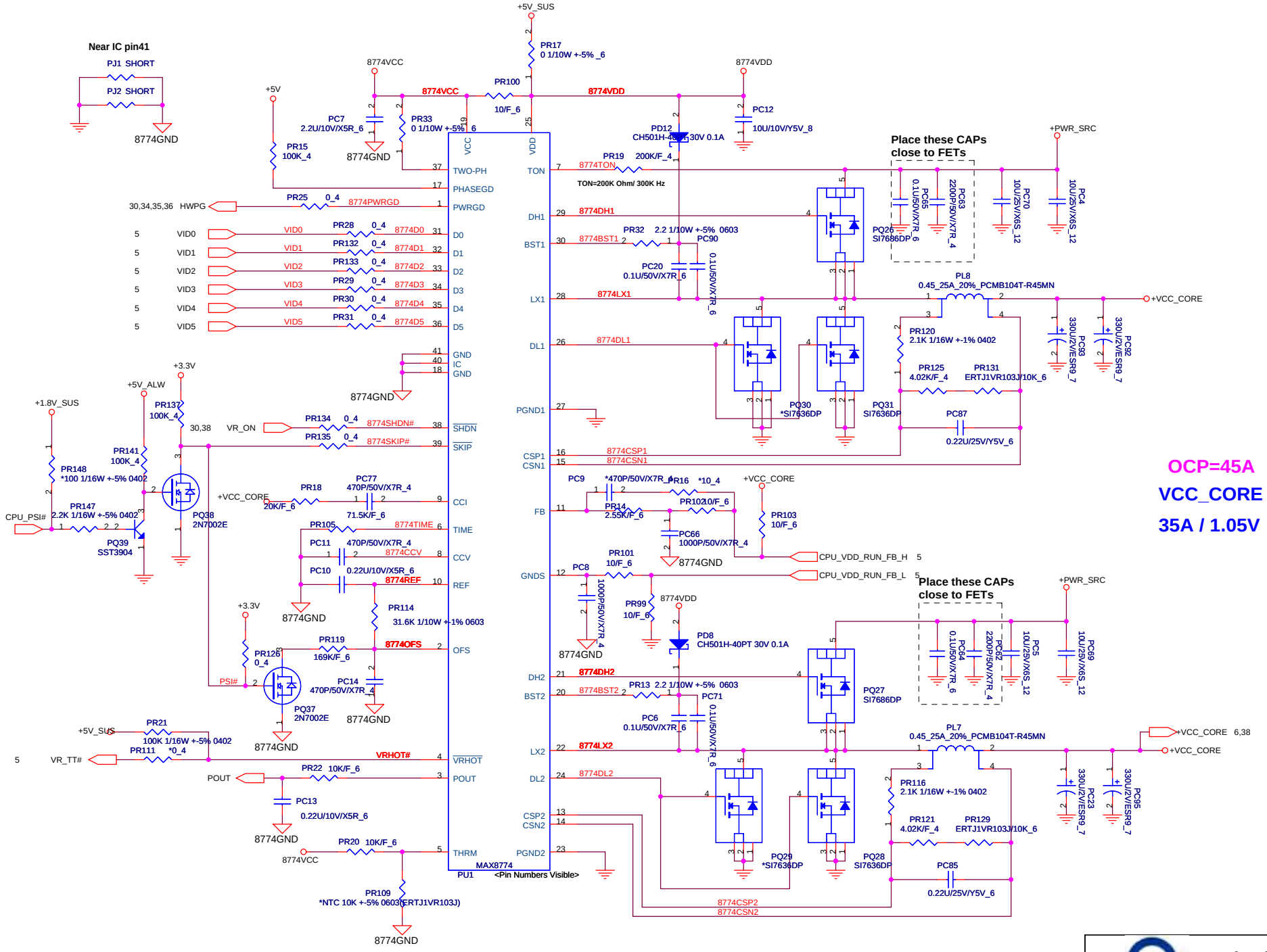

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Quanta Computer Inc.		
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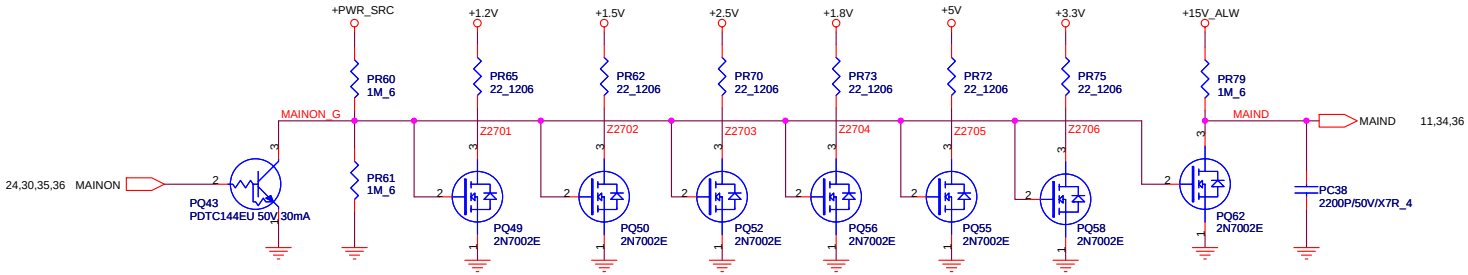

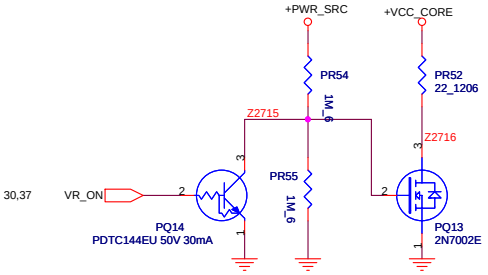

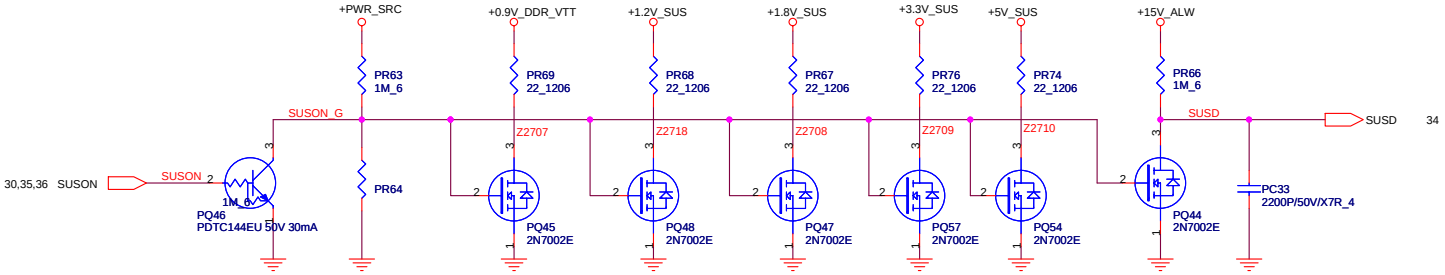

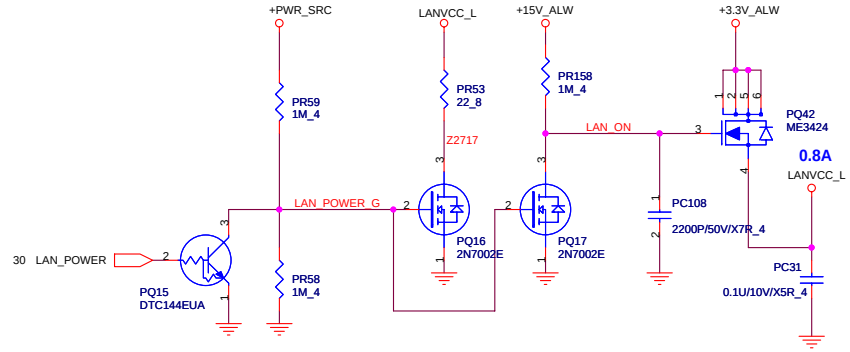

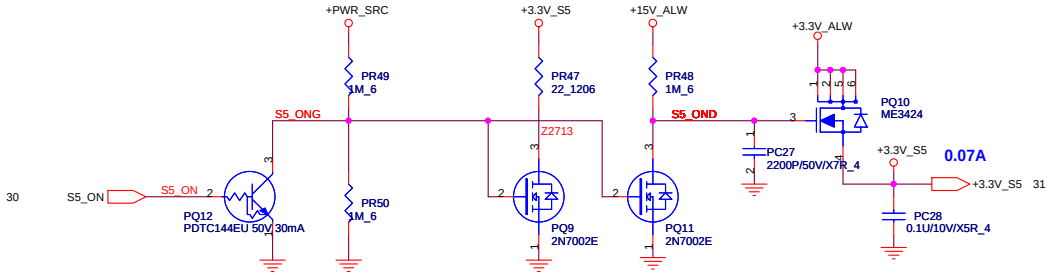

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Quanta Computer Inc.

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Custom	<Doc>	1A

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