SA6 BLOCK DIAGRAM

Penryn / Cantiga / ICH9-M

CPU THERMAL SENSOR
+3.3V
PG 3

CPU Penryn
(479 Micro-FCPGA)
+1.5V
+1.05V_VCCP
+VCC_CORE
PG 3,4

FSB
667/800 MHz

X'TAL
14.318MHz

CLOCK GEN
ICS9LPRS365/RTM875T-606
64pins
+3.3V
PG 2

CPU CLK_ 200MHz
GMCH CLK_ 200MHz
DREFCLK_96MHz
PCIE MCH CLK_100MHz

+3V_S5/+5V_S5 PG 40
CPU CORE POWER ISL6260C+ISL6208 PG 38
+1.5V & +1.05VCCP (RT8204) PG 37
DDR2 +1.8V_SUS & +0.9V PG 36
D/D POWER +5_ALW & +3.3V_ALW PG 35
CHARGER ISL6251A PG 34
RUN POWER SW & DISCHARGE PG 33

DDRII-SODIMM1
DDRII-SODIMM2
+0.9V_DDR_VTT
+1.8V_SUS
+3.3V
V_DDR_MCH_REF
PG 12,13

DDRII 667 MHz

NORTH BRIDGE
Cantiga
1299 uFCBGA
+1.05V_VCCP
+1.8V_SUS
+1.5V
+3.3V
V_DDR_MCH_REF
PG 5~11

FOR Crestline (LCD/CRT/S-VIDEO)
LCD Panel
VIN_BLIGHT
LCDVCC
+3.3V
PG 18

FOR Crestline (LCD/CRT)
CRT port
+5V
+3.3V
PG 20

SDVO
Parade
PS8101
PG 19

HDMI
HDMI port
+3.3V
+2.5V
PG 19

PCIE ICH CLK_100MHz
SATA ICH CLK_100MHz
PCIE LAN CLK_100MHz
PCIE MINICARD CLK_100MHz
PCIE NEW CARD CLK_100MHz
PCI OZ126T CLK_33MHz

Web Cam on LCD
USB8
+5V
PG 18

Bluetooth
USB9
+5V_SUS
PG 29

USB PORT X 3
USB0~2,
+5V_SUS
PG 28

USB 2.0

Fingerprint
USB6
PG 29

ODD(fixed)
+5V
PG 27

SATA

Internal HDD
+5V
+3.3V
PG 27

SATA

X'TAL
32.768KHz

DMI LINK
4X PCI-E

ICH9-M
652 BGA
+1.5V
+1.05V_VCCP
+1.25V
+3.3V
+3.3V_ALW
+3.3V_S5
+3.3V_SUS
+3V_VCCLAN
+5V
+5V_ALW
+5V_S5
VCCRTC_(1~4)
PG 14~17

PCI
PCI-E
Azalia
LPC

Azalia Codec
CX20561
+AVDDA
PG 23

LAN(10/100)
Marvell 88E8040
LAN_A1.8
LAN_A3.3
LAN_D1.5
LAN_E1.8
LANVCC
PG 20,21

MINI-PCI-E Card X2
USB4~5
+3.3V_SUS
+3.3V
+1.5V
PG 26

EXPRESS CARD
(NEW CARD)
USB3
3V_NEWCARD
3VAUX
1.5V_NEWCARD
PG 32

CARDREADER CONTROLLER
OZ126T
+3.3V
+1.8V
PG 22

X'TAL
25MHz

4 IN 1
SM/xD-Picture
SD/MMC
MS/MSPRO
(CF)
PG 22

MODEM CONN. (MDC)
+3.3V_SUS
PG 25

WIRE

RJ11/USB X 1
Board to board CONN.
PG 25

AMP
TPA6017A2
+5V_SPK_AMP PG 24

RJ45 JACK
PG 20

JACK
HEADPHONE/SPDIF
INT. DMIC
INT. SPEAKERS
PG 24

X'TAL
32.768KHz

HDCP SPI FLASH
PG 15

SPI

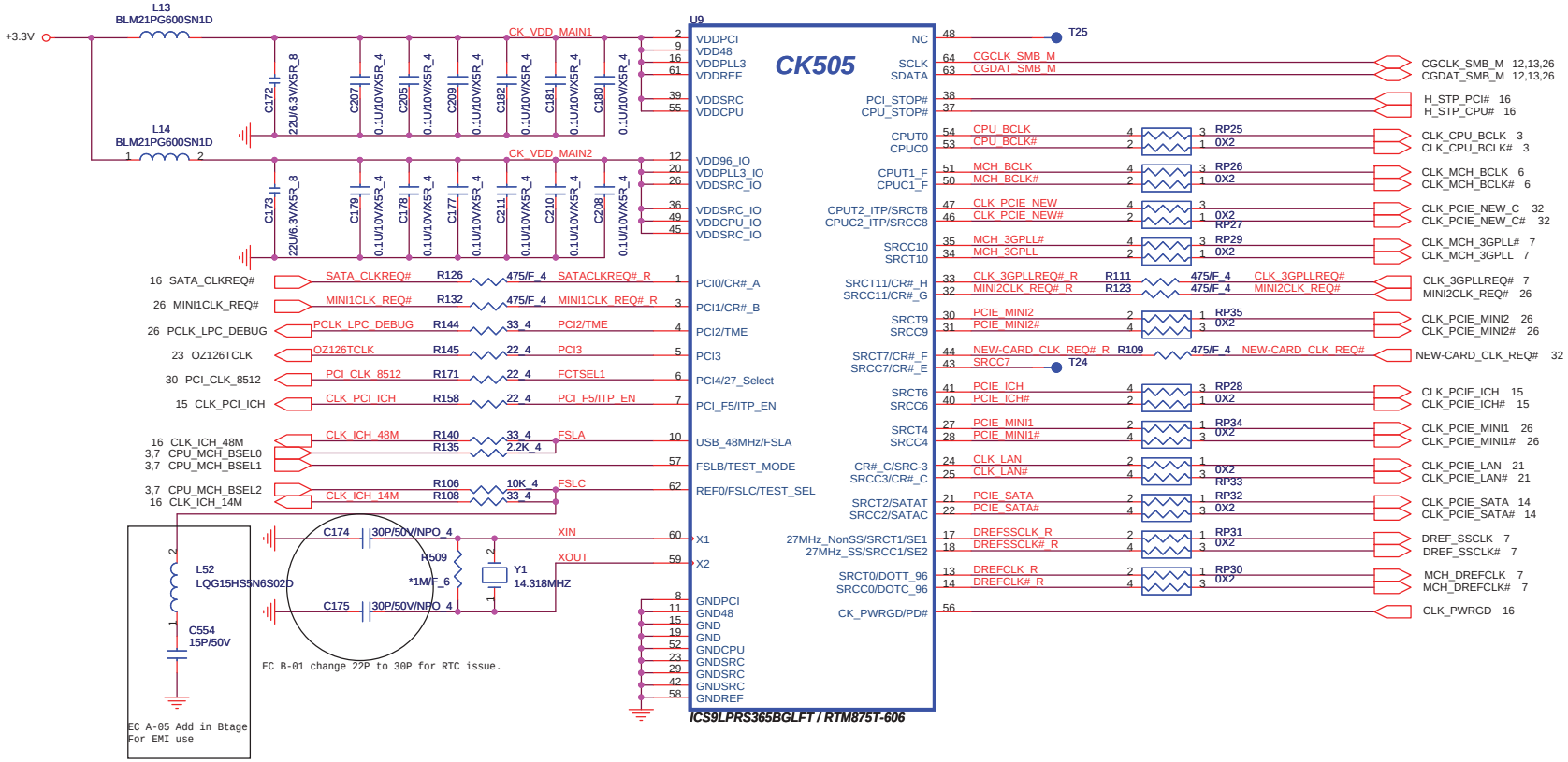
IT8502E
LQFP 128PIN
+3.3V_ALW
+3.3V
+5V
RTC_VCC
PG 29

SWITCH BOARD +3.3V_ALW PG 31
FAN PG 3
Touchpad +5V PG 31
Keyboard +3.3V_ALW PG 31
SPI FLASH +3.3V_ALW PG 29

PROJECT : SA6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3B

Date: Friday, April 25, 2008 Sheet 1 of 41



	PULL HIGH	PULL LOW
PCI_F5/ITP_EN	ITP/ITP#	SRC8/SRC8#
PCI2/TME	Overclocking of CPU and SRC not allowed	Overclocking of CPU and SRC allowed

GCLK_SEL = FCTSEL1

FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS

CPU Clock select

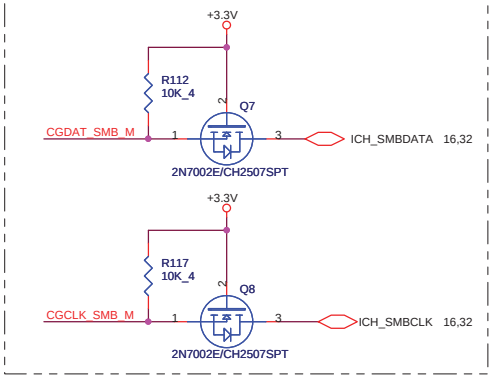
FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33

EMI CAP

C223	*15P/50V	OZ126TCLK
C216	15P/50V	CLK_ICH_48M
C176	15P/50V	CLK_ICH_14M
C229	10P/50V/C0G_4	PCI_CLK_8512
C222	15P/50V	PCLK_LPC_DEBUG
C224	15P/50V	CLK_PCI_ICH

EC C-10/03 Change C229 to 10P and R171 to 22 ohm for meet Clock test.

	PULL HIGH	PULL LOW
PCI3	PIN37/38 is CPU_STOP/PCI_STOP PIN37/38 IS SRC5.	**SRC5_EN/PCI-3 (Internal Pull Low)



PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3B
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U16A

ADDR GROUP 0 / ADDR GROUP 1 / CONTROL / XDP/ITP SIGNALS / THERMAL / ICH / H CLK / RESERVED

Layout Note: Place R347 close to CPU.

Layout Note: Place voltage divider within 0.5" of GTLREF pin

U16B

DATA GRP 0 / DATA GRP 2 / DATA GRP 1 / DATA GRP 3 / MISC

Penryn Ball-out Rev 1a

Note: H_DPRTSTP need to daisy chain from ICH9 to IMVP6 to CPU.

Voltage Level shift

Place C close to the CPU_TEST4 pin. Make sure CPU_TEST4 routing is reference to GND and away from other noisy signal.

PAD T6
PAD T84

For the purpose of testability, route these signals through a ground referenced Z0 = 55ohm trace that ends in a via that is near a GND via and is accessible through an oscilloscope connection.

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

Populate ITP700Flex for bringup

EC B-02 chamge from 150 to 10K for meet Intel spec.

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	54.9 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	54.9 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	54.9 ohm ± 5%	GND	Place the pull-down near CPU
TCK	54.9 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	54.9 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	54.9 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

Comp0,2 connect with Zo=27.4ohm,Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5".Trace should be at least 25 mils away from any other toggling signal.

PROJECT : SA6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn Processor (HOST BUS)	3B

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All use 22U 10V(+-20%,X5R,1210)Pb-Free.

+VCC_CORE

C338 10U/4V
C339 10U/4V
C38 10U/4V
C350 10U/4V
C349 10U/4V

+VCC_CORE

C334 10U/4V
C336 10U/4V
C348 10U/4V
C351 10U/4V
C39 10U/4V

8 inside cavity, north side, secondary layer.

+VCC_CORE

C335 10U/4V
C14 10U/4V
C17 10U/4V
C16 10U/4V
C353 10U/4V

+VCC_CORE

C15 10U/4V
C18 10U/4V
C19 10U/4V
C37 10U/4V
C337 10U/4V

8 inside cavity, south side, secondary layer.

+VCC_CORE

C20 10U/4V
C24 10U/4V
C25 10U/4V
C12 10U/4V
C21 10U/4V
C13 10U/4V

6 inside cavity, north side, primary layer.

+VCC_CORE

C32 10U/4V
C33 10U/4V
C34 10U/4V
C35 10U/4V
C352 10U/4V
C36 10U/4V

6 inside cavity, south side, primary layer.

+1.05V_VCCP

C345 0.1U/10V
C341 0.1U/10V
C340 0.1U/10V
C342 0.1U/10V
C347 0.1U/10V
C344 0.1U/10V

Layout out:
Place these inside socket cavity on North side secondary.

+PWR_SRC

C331 *100U/25V

C331 and C317 remove in B stage
C317 PAD remove in FAI stage

Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.

+VCC_CORE

U16C

VCC[001] A7
VCC[002] A9
VCC[003] A10
VCC[004] A12
VCC[005] A13
VCC[006] A15
VCC[007] A17
VCC[008] A18
VCC[009] A20
VCC[010] B7
VCC[011] B9
VCC[012] B10
VCC[013] B12
VCC[014] B14
VCC[015] B15
VCC[016] B17
VCC[017] B18
VCC[018] B20
VCC[019] C9
VCC[020] C10
VCC[021] C12
VCC[022] C13
VCC[023] C15
VCC[024] C17
VCC[025] C18
VCC[026] D9
VCC[027] D10
VCC[028] D12
VCC[029] D14
VCC[030] D15
VCC[031] D17
VCC[032] D18
VCC[033] E7
VCC[034] E9
VCC[035] E10
VCC[036] E12
VCC[037] E13
VCC[038] E15
VCC[039] E17
VCC[040] E18
VCC[041] E20
VCC[042] F7
VCC[043] F9
VCC[044] F10
VCC[045] F12
VCC[046] F14
VCC[047] F15
VCC[048] F17
VCC[049] F18
VCC[050] F20
VCC[051] AA7
VCC[052] AA9
VCC[053] AA10
VCC[054] AA12
VCC[055] AA13
VCC[056] AA15
VCC[057] AA17
VCC[058] AA18
VCC[059] AA20
VCC[060] AB9
VCC[061] AC10
VCC[062] AB10
VCC[063] AB12
VCC[064] AB14
VCC[065] AB15
VCC[066] AB17
VCC[067] AB18

VCC[068] AB20
VCC[069] AB7
VCC[070] AC7
VCC[071] AC9
VCC[072] AC12
VCC[073] AC13
VCC[074] AC15
VCC[075] AC17
VCC[076] AC18
VCC[077] AD7
VCC[078] AD9
VCC[079] AD10
VCC[080] AD12
VCC[081] AD14
VCC[082] AD15
VCC[083] AD17
VCC[084] AD18
VCC[085] AE9
VCC[086] AE10
VCC[087] AE12
VCC[088] AE13
VCC[089] AE15
VCC[090] AE17
VCC[091] AE18
VCC[092] AE20
VCC[093] AF9
VCC[094] AF10
VCC[095] AF12
VCC[096] AF14
VCC[097] AF15
VCC[098] AF17
VCC[099] AF18
VCC[100] AF20

VCCP[01] G21
VCCP[02] V6
VCCP[03] J6
VCCP[04] K6
VCCP[05] M6
VCCP[06] J21
VCCP[07] K21
VCCP[08] M21
VCCP[09] N21
VCCP[10] N6
VCCP[11] R21
VCCP[12] R6
VCCP[13] T21
VCCP[14] T6
VCCP[15] V21
VCCP[16] W21

VCCA[01] B26
VCCA[02] C26

VID[0] AD6
VID[1] AE5
VID[2] AE5
VID[3] AF4
VID[4] AE3
VID[5] AF3
VID[6] AE2

VCCSENSE AF7
VSSSENSE AF7

Penryn Ball-out Rev 1a

+1.05V_VCCP

C333 330U/2.5V_7343

+1.5V

C52 0.01U/25V
C49 10U/4V

Layout Note:
Place C105 near PIN B26.

VID0 38
VID1 38
VID2 38
VID3 38
VID4 38
VID5 38
VID6 38

VCCSENSE 38
VSSSENSE 38

+VCC_CORE

R311 100/F
R312 100/F

VCCSENSE
VSSSENSE

Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

U16D

VSS[001] A4
VSS[002] A8
VSS[003] A11
VSS[004] A14
VSS[005] A16
VSS[006] A19
VSS[007] A23
VSS[008] AE2
VSS[009] B6
VSS[010] B8
VSS[011] B11
VSS[012] B13
VSS[013] B16
VSS[014] B19
VSS[015] B21
VSS[016] B24
VSS[017] C5
VSS[018] C8
VSS[019] C11
VSS[020] C14
VSS[021] C16
VSS[022] C19
VSS[023] C2
VSS[024] C22
VSS[025] C25
VSS[026] D1
VSS[027] D4
VSS[028] D8
VSS[029] D11
VSS[030] D13
VSS[031] D16
VSS[032] D19
VSS[033] D23
VSS[034] D26
VSS[035] E3
VSS[036] E6
VSS[037] E8
VSS[038] E11
VSS[039] E14
VSS[040] E16
VSS[041] E19
VSS[042] F21
VSS[043] E24
VSS[044] F5
VSS[045] F8
VSS[046] F11
VSS[047] F13
VSS[048] F16
VSS[049] F19
VSS[050] F2
VSS[051] F22
VSS[052] F25
VSS[053] G4
VSS[054] G1
VSS[055] G23
VSS[056] G26
VSS[057] H3
VSS[058] H6
VSS[059] H21
VSS[060] H24
VSS[061] J2
VSS[062] J5
VSS[063] J22
VSS[064] J25
VSS[065] K1
VSS[066] K4
VSS[067] K23
VSS[068] K26
VSS[069] L3
VSS[070] L6
VSS[071] L21
VSS[072] L24
VSS[073] M2
VSS[074] M5
VSS[075] M22
VSS[076] M25
VSS[077] N1
VSS[078] N4
VSS[079] N23
VSS[080] N26
VSS[081] P3

VSS[082] P6
VSS[083] P21
VSS[084] P24
VSS[085] R2
VSS[086] R5
VSS[087] R22
VSS[088] R25
VSS[089] T1
VSS[090] T4
VSS[091] T23
VSS[092] T26
VSS[093] U3
VSS[094] U6
VSS[095] U21
VSS[096] U24
VSS[097] V2
VSS[098] V5
VSS[099] V22
VSS[100] V25
VSS[101] W1
VSS[102] W4
VSS[103] W23
VSS[104] W26
VSS[105] Y3
VSS[106] Y6
VSS[107] Y21
VSS[108] Y24
VSS[109] AA2
VSS[110] AA5
VSS[111] AA8
VSS[112] AA11
VSS[113] AA14
VSS[114] AA16
VSS[115] AA19
VSS[116] AA22
VSS[117] AA25
VSS[118] AB1
VSS[119] AB4
VSS[120] AB8
VSS[121] AB11
VSS[122] AB13
VSS[123] AB16
VSS[124] AB19
VSS[125] AB23
VSS[126] AB26
VSS[127] AC3
VSS[128] AC6
VSS[129] AC8
VSS[130] AC11
VSS[131] AC14
VSS[132] AC16
VSS[133] AC19
VSS[134] AC21
VSS[135] AC24
VSS[136] AD2
VSS[137] AD5
VSS[138] AD8
VSS[139] AD11
VSS[140] AD13
VSS[141] AD16
VSS[142] AD19
VSS[143] AD22
VSS[144] AD25
VSS[145] AE1
VSS[146] AE4
VSS[147] AE8
VSS[148] AE11
VSS[149] AE14
VSS[150] AE16
VSS[151] AE19
VSS[152] AE23
VSS[153] AE26
VSS[154] A2
VSS[155] AF6
VSS[156] AF8
VSS[157] AF11
VSS[158] AF13
VSS[159] AF16
VSS[160] AF19
VSS[161] AF21
VSS[162] A25
VSS[163] AF25

Penryn Ball-out Rev 1a

PROJECT : SA6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn Processor (POWER)	3B
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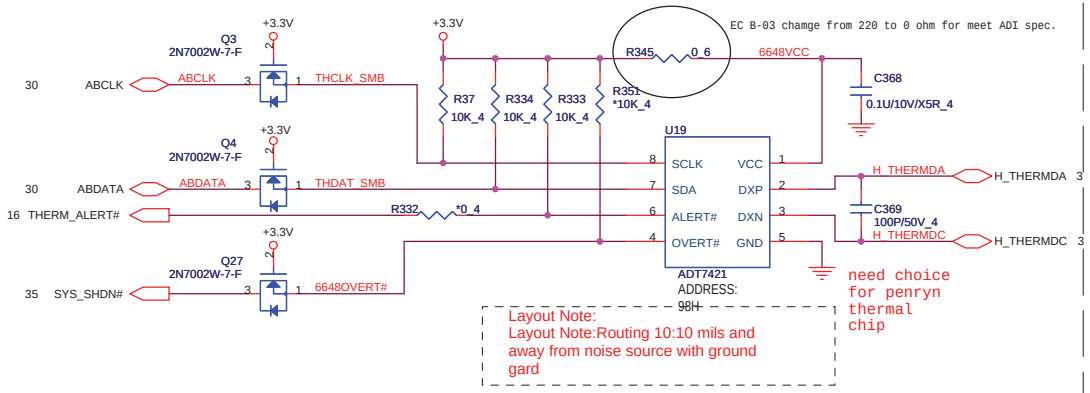
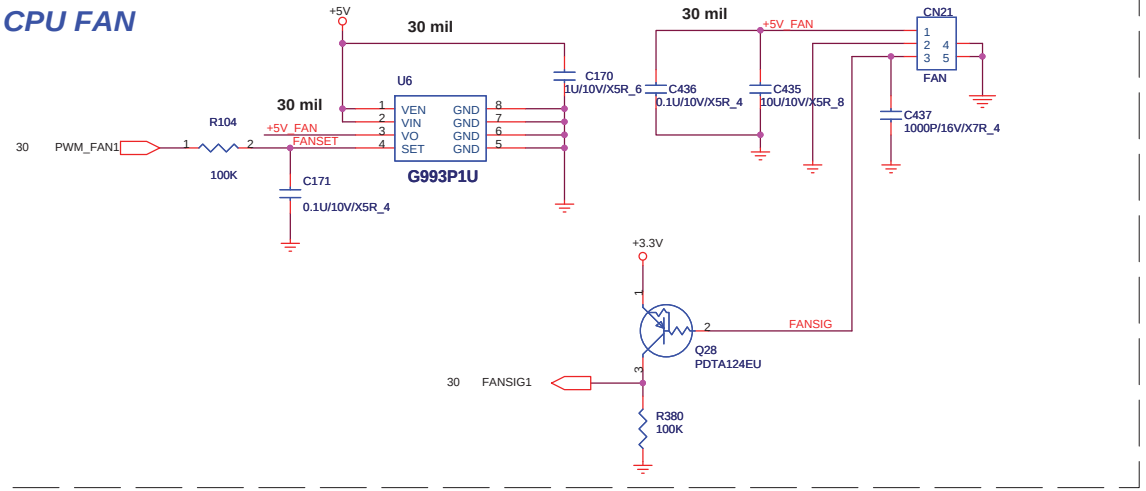
CPU Thermal monitor



CPU FAN



PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Thermal monitor	3B
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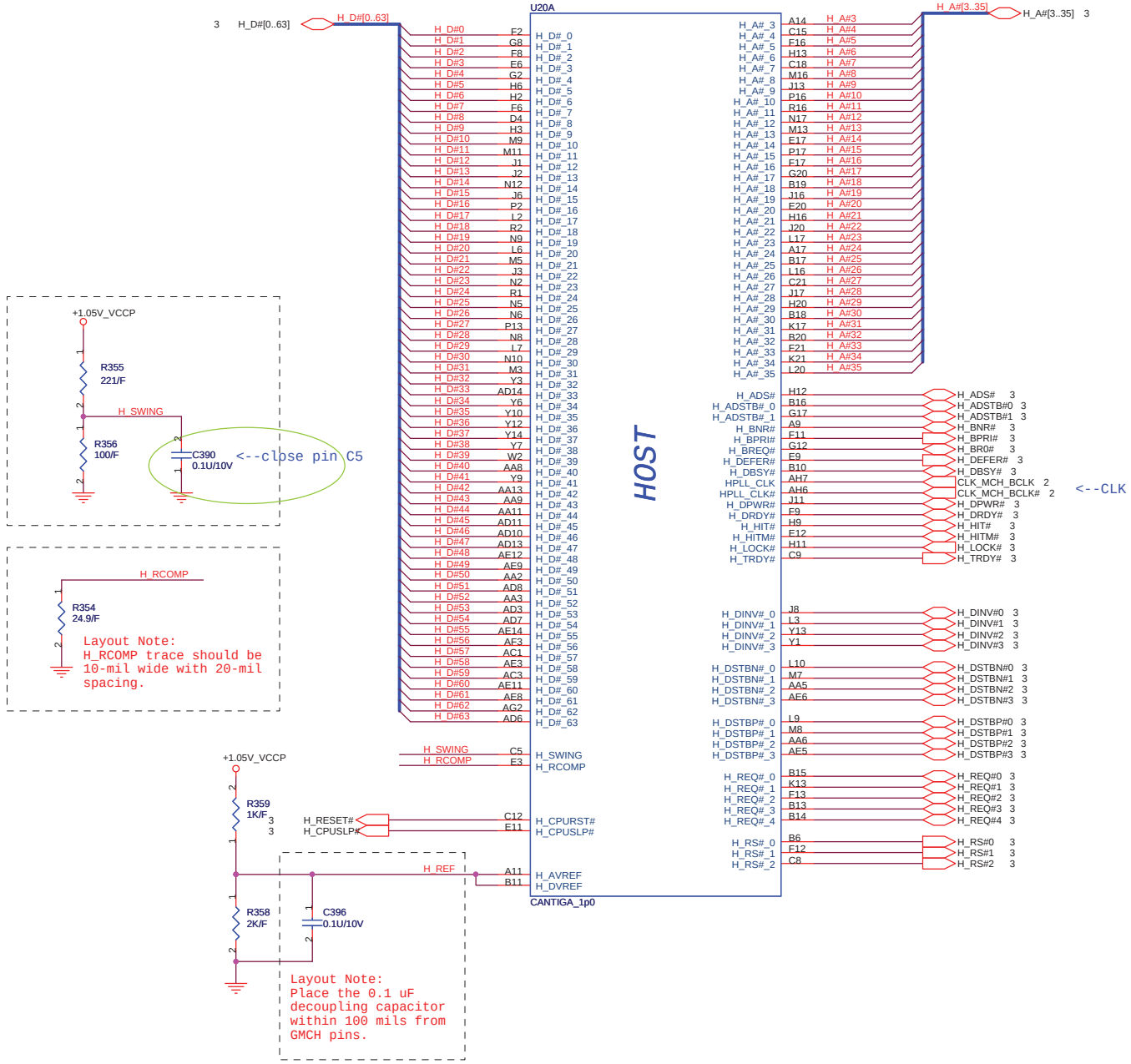

PROJECT :	SA6
Quanta Computer Inc.	
Size: Custom	Document Number: Cantiga (HOST)
Rev: 3B	
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U20B

RSVD

CONTROL/COMPENSATION

DDR

CLK

DMI

CFG

GRAPHICS VID

PM

ME

MISC

HDA

NC

U20C

LVDS

TV

VGA

PCI-EXPRESS GRAPHICS

CANTIGA_1p0

pull up/down impedance compensation For Memory

Layout Note: Location of all MCH_CFG strap resistors needs to be close to minmize stub.

Layout Note: Place 150 ohm termination resistors close to GMCH.

Layout Note: HSYNC/VSYNC serial R place close to NB

EC-19 change R88 from 1.02K to 1K meet Intel check list 1.1

49.9 ohm for cantiga

For UMA HDMI Function

FOR HDME HPD (NEED CHECK)

Non-iAMT

For ME Management Engine

For Memory

install 80.6 for Cantiga.
install 20 for Teenah.

PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (VGA,DMI)	3B
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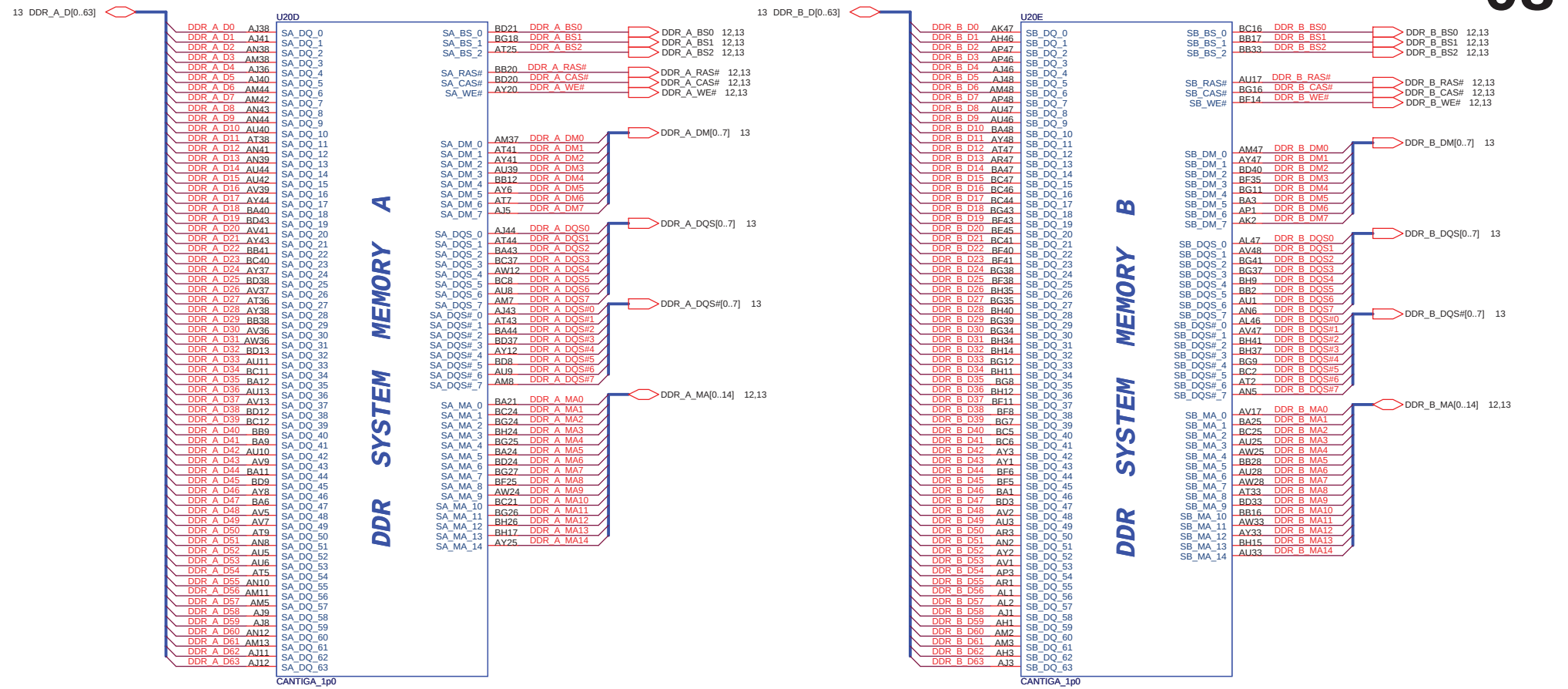
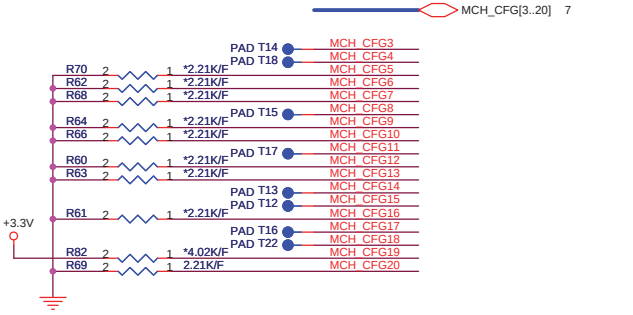
DDR2



STRAPPING

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG6	iTPM Host Interface	Low= Enable High=Disable(Default)
CFG7	Intel Management Engine Crypto Strap	Low= Intel Management Engine Crypto TLS cipher suite with no Confidentiality High=Intel Management Engine Crypto TLS cipher suite with Confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG10	PCIe Loopback Enable	Low= Enable High=Disable(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	Digital Display Port(SDVO/DP/iHDMI) and PCIe Concurrent Operation.	Low=Only DP or inly PCIe is operational (defaults) High=DP and PCIe x1 are operating simultaneously.
CFG13 / CFG12	XOR / ALLZ / Clock Un-gating	00=Reserved. 10=XOR Mode Enabled. 01=All-Z Mode Enabled. 11=Normal Operation (Default).



PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (DDR2,STRAPPING)	3B
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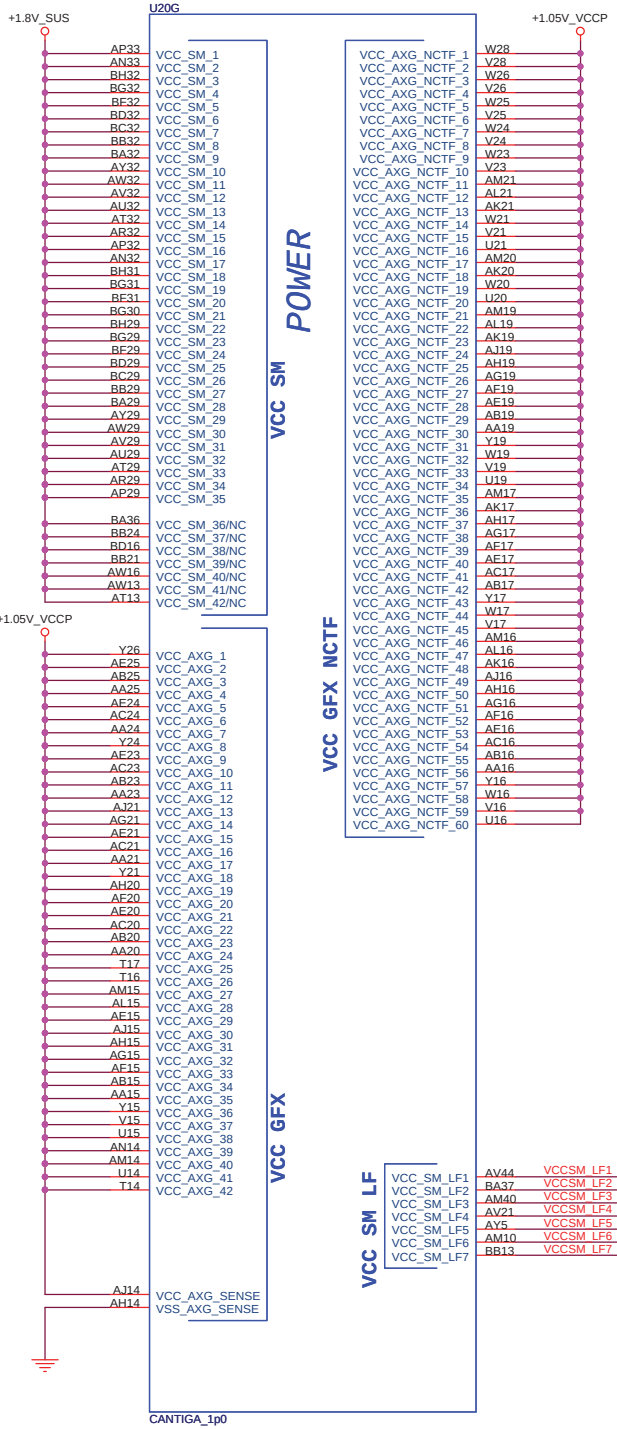
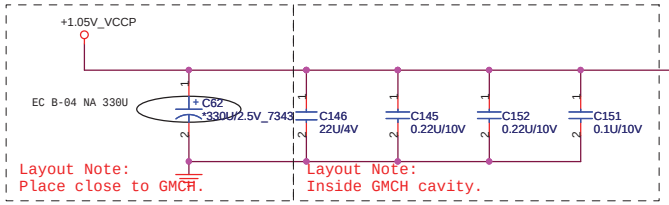


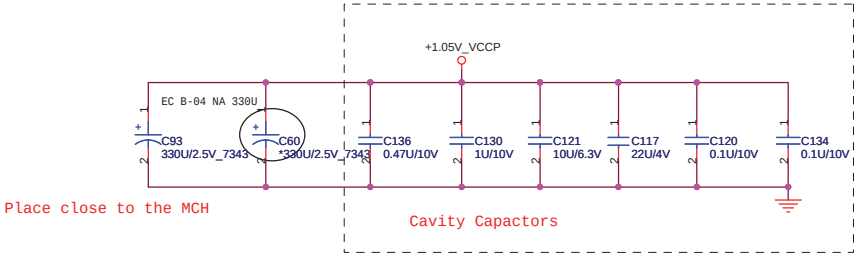


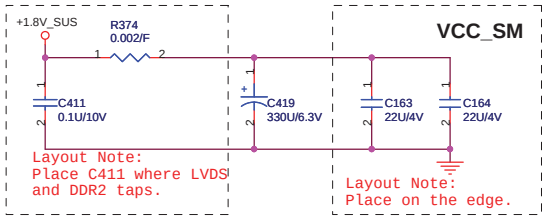
NB Power Status and max current table(1/3)

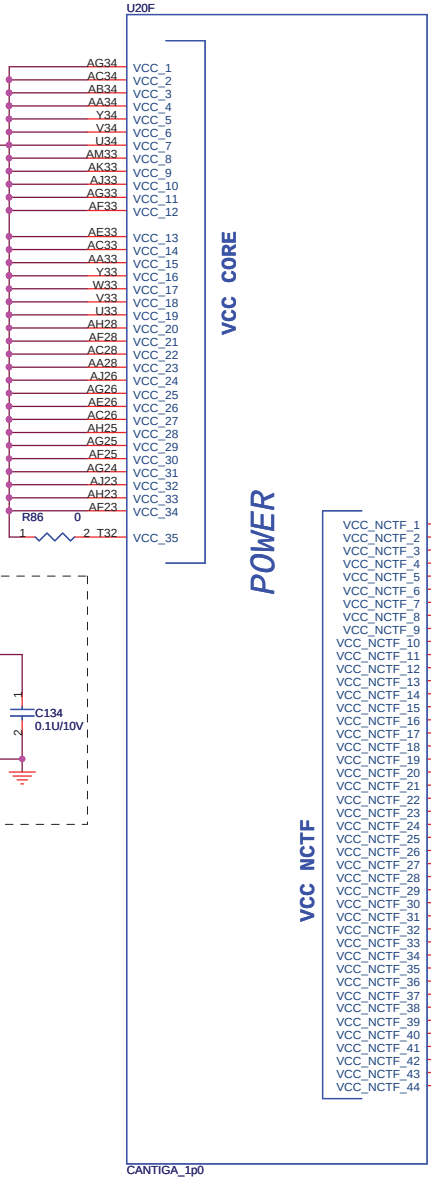
POWER PLANE	S0	S3	S4/S5	Voltage	I(max)	Note
VCC(EXT_VGA)	O	X	X	+1.05V	2178mA	
VCC(INT_VGA)	O	X	X	+1.05V	2899mA	
VCC_AXG	O	X	X	+1.05V	8700mA	Graphics Core
VCC_SM(800)	O	O	X	+1.8VSUS	3A	(DDRII-667) 2.6A
VCC_SM(Standby)	O	O	X	+1.8VSUS	1mA	Self Refresh during S3

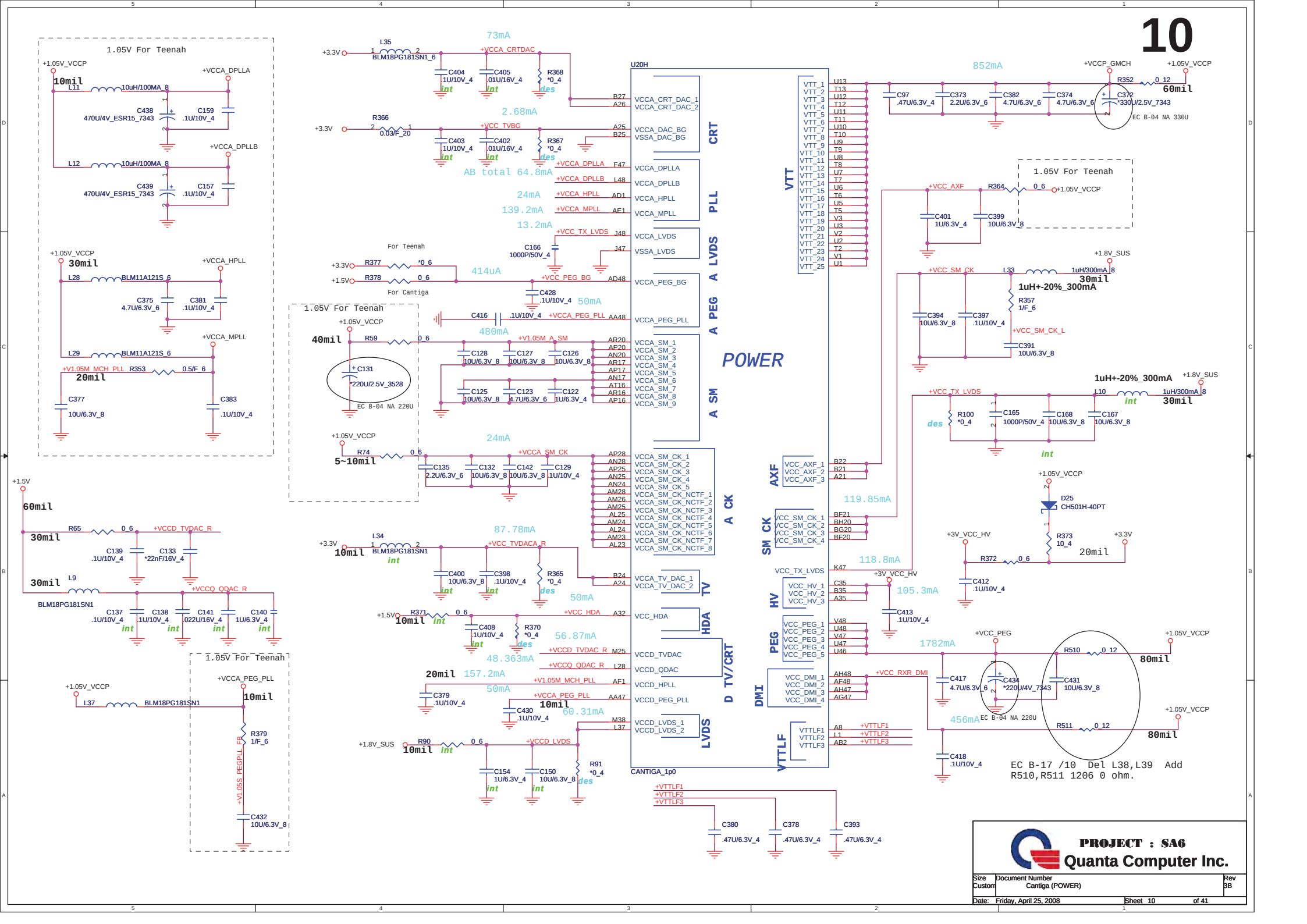
(See NB EDS Rev:1.0 Section 10.1 for max current)

(See NB EDS Rev:1.0 Section 12.2 for DC voltage)









PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (POWER)	3B

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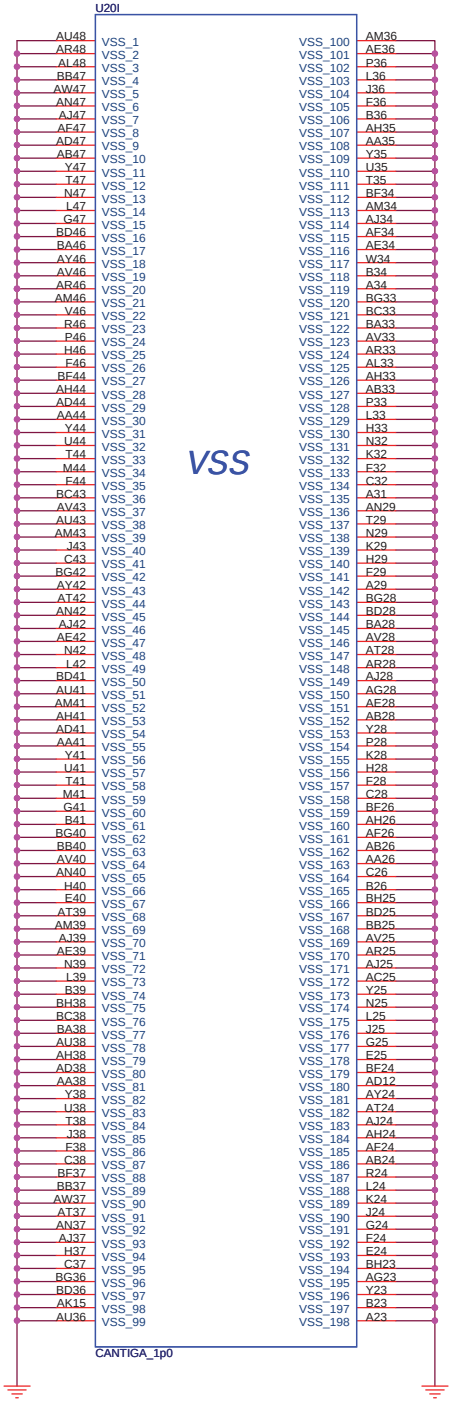

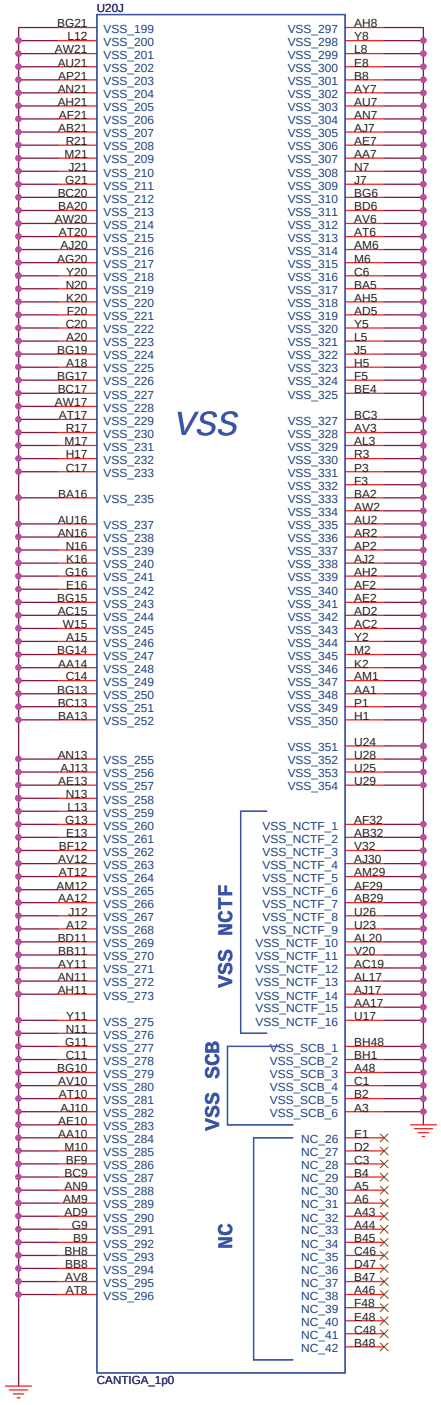

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Quanta Computer Inc.			
Size: Custom	Document Number: Cantiga (VSS)		Rev: 3B
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DDR2 Dual channel A/B PU

DDRII A CHANNEL

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

+0.9V_DDR_VTT

C108 C119 C63 C89 C104 C115 C111 C58 C68 C114 C66 C102 C110

0.1U/10V/X5R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C64 C77 C107 C112 C116 C94 C118 C61 C65 C57 C70 C86 C96

0.1U/10V/X5R_4

8,13 DDR_A_MA[0..13]

+0.9V_DDR_VTT

+0.9V_DDR_VTT 33,36

DDR_B_MA[0..13] 8,13

DDR_A_MA7 / DDR_A_MA11	RP21	56X2	RP20	56X2	DDR_B_MA11 / DDR_B_MA7
DDR_A_MA2 / DDR_A_MA6	RP19	56X2	RP17	56X2	DDR_B_MA6 / DDR_B_MA4
8,13 DDR_A_RAS# / 8,13 DDR_A_BS1	RP13	56X2	RP10	56X2	DDR_B_BS1 8,13 / DDR_B_RAS# 8,13
DDR_A_MA13 / 7,13 M_ODT0	RP7	56X2	RP4	56X2	DDR_B_MA13 / M_ODT2 7,13
DDR_A_MA12 / 8,13 DDR_A_BS2	RP24	56X2	RP14	56X2	DDR_B_MA1 / DDR_B_MA3
DDR_A_MA8 / DDR_A_MA9	RP22	56X2	RP23	56X2	DDR_B_MA9 / DDR_B_MA12
DDR_A_MA5 / DDR_A_MA3	RP16	56X2	RP18	56X2	DDR_B_MA5 / DDR_B_MA8
DDR_A_MA10 / DDR_A_BS0	RP11	56X2	RP9	56X2	DDR_B_MA10 / DDR_B_BS0 8,13
8,13 DDR_A_CAS# / 8,13 DDR_A_WE#	RP8	56X2	RP6	56X2	DDR_B_WE# 8,13 / DDR_B_CAS# 8,13
DDR_A_MA0 / DDR_A_MA4	RP15	56X2	RP12	56X2	DDR_B_MA2 / DDR_B_MA0

7,13 M_ODT1 / DDR_A_MA1	R39 / R46	56_4	R38 / R52	M_ODT3 7,13 / DDR_B_BS2 8,13
7,13 DDR_CS0_DIMMA#	R44	56_4	R42	DDR_CS2_DIMMB# 7,13
7,13 DDR_CS1_DIMMA#	R41	56_4	R40	DDR_CS3_DIMMB# 7,13
7,13 DDR_CKE0_DIMMA	R56	56_4	R55	DDR_CKE3_DIMMB 7,13
7,13 DDR_CKE1_DIMMA	R53	56_4	R54	DDR_CKE4_DIMMB 7,13
8,13 DDR_A_MA14	R50	56_4	R51	DDR_B_MA14 8,13

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V

+3.3V 2,5,7,8,10,13,14,15,16,17,18,19,20,21,23,24,26,27,29,30,31,32,33,40

R21 *220_6

C40 *0.1U/10V/X5R_4

LM86_3V

DDR_THERMDA

DDR_THERMDC

*MMBT3904_NL Q1

U3

2,13,26 CGCLK_SMB_M	8	SCLK	VCC 1
2,13,26 CGDAT_SMB_M	7	SDA	DXP 2
7,13 PM_EXTTS#0	6	ALERT#	DXN 3
7 PM_EXTTS#1	4	OVERT#	GND 5

R22 *0_4

*LM86CIMM

PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR RES. ARRAY	3B
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A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

PC4800 DDR2 SDRAM SO-DIMM (200P)

CN19 — DIMM1_9.2

CKE 0,1
CLOCK 0,1

SMbus address A0

CN18 — DIMM2_5.2

CKE 2,3
CLOCK 3,4

SMbus address A4

Place these Caps near So-Dimm1.

Place these Caps near So-Dimm2.

PROJECT : SA6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR SO-DIMM(200P)	3B

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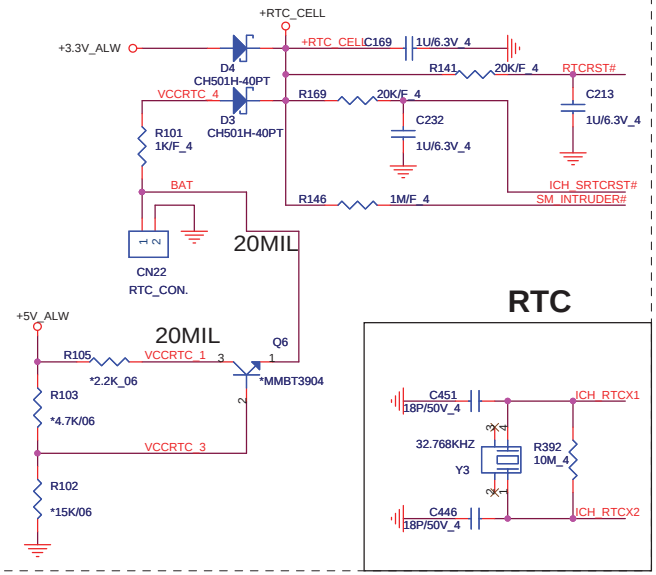
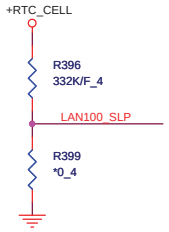
RTC

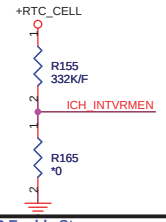


SB Strap

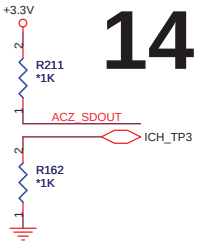


ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

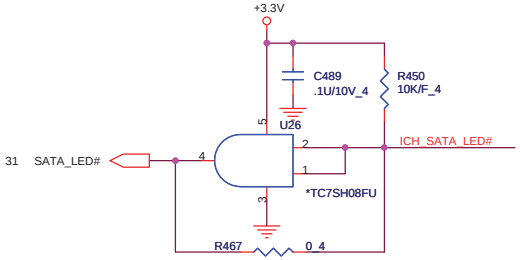
LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)



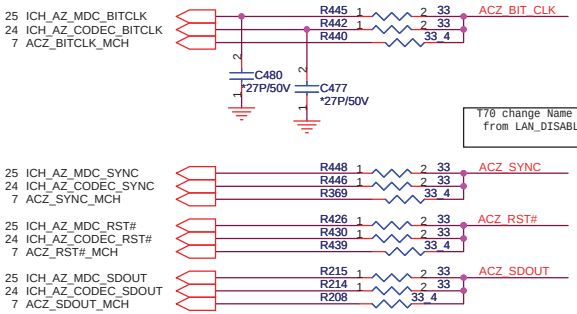
ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)



XOR Chain Entrance Strap		
ICH TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1



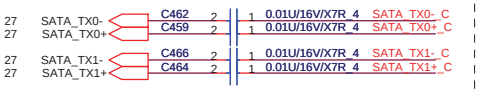
AZ Interface(MDC, CODEC, HDMI)



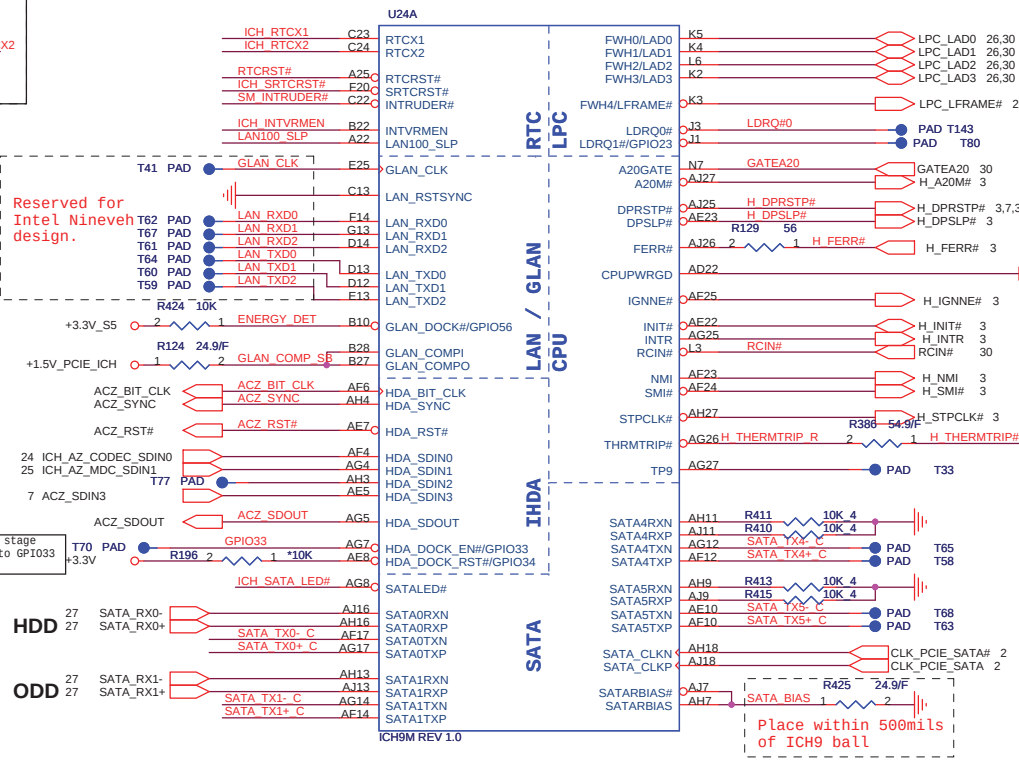
Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.

AC-TX for SATA

EC A-06 C462,C459,C466,C464 Change to 10nF in B Stage.



Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.



Quanta Computer Inc.
PROJECT : SA6

Size	Document Number	Rev
Custom	ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)	3B
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Place TX DC blocking caps close ICH8.

OC# pull up

RP40 10P8R-10K: +3.3V_SUS
USB_OC2# 6 — USB_OC3# 5
USB_OC5# 7 — OC8# 4
OC9# 8 — WLAN_RF_OFF# 3
USB_OC0# 9 — USB_OC4# 2
+3.3V_SUS 10 — 1

+3.3V_SUS	R210	10K	OC10#	
	R218	10K	OC11#	
	R225	10K	OC7#	
	R207	10K	USB_OC1#	
+3.3V_S5	R224	10K	PCI_PME#	

EC A-07 /15 Add R224 PCI_PME# Connect to +3.3V_S5

PCI Pullups

+3.3V — R204 8.2K_4 — PCI_FRAME#

RP42 10P8R-8.2K: +3.3V
PCI_PIRQB# 6 — PCI_TRDY# 5
GPIO3 7 — PCI_PLOCK# 4
PCI_IRDY# 8 — PCI_DEVSEL# 3
PCI_PIRQD# 9 — PCI_STOP# 2
+3.3V 10 — 1

RP41 10P8R-8.2K: +3.3V
PCI_PERR# 6 — ICH_GPIO4_PIRQG# 5
PCI_PIRQC# 7 — PCI_REQ0# 4
PCI_PIRQA# 8 — ICH_GPIO5_PIRQH# 3
PCI_SERR# 9 — GPIO2 2
+3.3V 10 — 1

MiniCard-1 (WLAN)

26	PCIE_RX1-			N29	PERN1
26	PCIE_RX1+			N28	PERP1
26	PCIE_TX1-	C187	0.1U/10V/X5R_4	P27	PETN1
26	PCIE_TX1+	C188	0.1U/10V/X5R_4	P26	PETP1

MiniCard-2

26	PCIE_RX2-			L29	PERN2
26	PCIE_RX2+			L28	PERP2
26	PCIE_TX2-	C189	0.1U/10V/X5R_4	M27	PETN2
26	PCIE_TX2+	C190	0.1U/10V/X5R_4	M26	PETP2

Express Card (NEWCARD)

32	PCIE_RXN3			J29	PERN3
32	PCIE_RXP3			J28	PERP3
32	PCIE_TXN3	C191	0.1U/10V/X5R_4	K27	PETN3
32	PCIE_TXP3	C192	0.1U/10V/X5R_4	K26	PETP3

T10				G29	PERN4
T31				G28	PERP4
T35				H27	PETN4
T36				H26	PETP4
T29				E29	PERN5
T32				E28	PERP5
T28				F27	PETN5
T39				F26	PETP5

21	PCIE_RX6-/GLAN_RX-			C29	PERN6/GLAN_RXN
21	PCIE_RX6+/GLAN_RX+			C28	PERP6/GLAN_RXP
21	PCIE_TX6-/GLAN_TX-	C194	0.1U/10V/X5R_4	D27	PETN6/GLAN_TXN
21	PCIE_TX6+/GLAN_TX+	C193	0.1U/10V/X5R_4	D26	PETP6/GLAN_TXP

U24D

PCI-Express / Direct Media Interface

				V27	DMI0RXN
				V26	DMI0RXP
				U29	DMI0TXN
				U28	DMI0TXP
				Y27	DMI1RXN
				Y26	DMI1RXP
				W29	DMI1TXN
				W28	DMI1TXP
				AB27	DMI2RXN
				AB26	DMI2RXP
				AA29	DMI2TXN
				AA28	DMI2TXP
				AD27	DMI3RXN
				AD26	DMI3RXP
				AC29	DMI3TXN
				AC28	DMI3TXP
				T26	DMI_CLKN
				T25	DMI_CLKP
				AF29	DMI_ZCOMP
				AF28	DMI_IRCOMP

DMI_IRCOMP R382 24.9/F +1.5V_PCIE_ICH

DMI_MTX_IRX_N0 7 / DMI_MTX_IRX_P0 7 / DMI_MRX_ITX_N0 7 / DMI_MRX_ITX_P0 7
DMI_MTX_IRX_N1 7 / DMI_MTX_IRX_P1 7 / DMI_MRX_ITX_N1 7 / DMI_MRX_ITX_P1 7
DMI_MTX_IRX_N2 7 / DMI_MTX_IRX_P2 7 / DMI_MRX_ITX_N2 7 / DMI_MRX_ITX_P2 7
DMI_MTX_IRX_N3 7 / DMI_MTX_IRX_P3 7 / DMI_MRX_ITX_N3 7 / DMI_MRX_ITX_P3 7

CLK_PCIE_ICH# 2 / CLK_PCIE_ICH 2

Place within 500mils of ICH9

SPI

SPI_CLK_R	D23	SPI_CLK	
SPI_CS0#_R	D24	SPI_CS0#	
SPI_CS1#_R	F23	SPI_CS1#/GPIO58/CLKGPIO6	
SPI_MOSI_R	D25	SPI_MOSI	
SPI_MISO_R	E23	SPI_MISO	

USB

28	USB_OC0#		N4	OC0#/GPIO59	
28	USB_OC1#		N5	OC1#/GPIO40	
25	USB_OC2#		N6	OC2#/GPIO41	
	USB_OC3#		P6	OC3#/GPIO42	
	USB_OC4#		M1	OC4#/GPIO43	
	USB_OC5#		N2	OC5#/GPIO29	
26,31	WLAN_RF_OFF#		M4	OC6#/GPIO30	
	OC7#		M3	OC7#/GPIO31	
	OC8#		N3	OC8#/GPIO44	
	OC9#		N1	OC9#/GPIIO45	
	OC10#		P5	OC10#/GPIO46	
	OC11#		P3	OC11#/GPIO47	

R452 22.6/F USB_RBIAS_PN — AG2 USBRBIAS, AG1 USBRBIAS#

placed within 500-mils of the ICH9M

ICH9M REV 1.0

				AC5	USBP0-
				AC4	USBP0+
				AD3	USBP1-
				AD2	USBP1+
				AC1	USBP2-
				AC2	USBP2+
				AA5	USBP3-
				AA4	USBP3+
				AB2	USBP4-
				AB3	USBP4+
				AA1	USBP5-
				AA2	USBP5+
				W5	USBP6-
				W4	USBP6+
				Y3	USBP7-
				Y2	USBP7+
				W1	USBP8-
				W2	USBP8+
				V2	USBP9-
				V3	USBP9+
				U5	ICH_USBP10-
				U4	ICH_USBP10+
				U1	ICH_USBP11-
				U2	ICH_USBP11+
					USBP10N
					USBP10P
					USBP11N
					USBP11P

USBP0- 28 / USBP0+ 28 / USBP1- 28 / USBP1+ 28 / USBP2- 25 / USBP2+ 25 / USBP3- 32 / USBP3+ 32 / USBP4- 26 / USBP4+ 26 / USBP5- 26 / USBP5+ 26 / USBP6- 29 / USBP6+ 29
USBP7- T76 / USBP7+ T75
USBP8- 18 / USBP8+ 18 / USBP9- 29 / USBP9+ 29
ICH_USBP10- T74 / ICH_USBP10+ T78 / ICH_USBP11- T79 / ICH_USBP11+ T81

System
System
System
NEWCARD
MiniCard-1 (WLAN)
MiniCard-2(reserved)
FINGERPRINT CONNECTOR
X
WEB CAM
BLUETOOTH

SPI_CS1# R / PCI_GNT0# — R222 *1K — R139 *1K

Boot BIOS Strap			
		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3# — R203 *1K

A16 away override strap.
Low = A16 swap override enabled.
High = Default.

U24B

PCI

AD0	D11	AD0	REQ0#	F1	PCI_REQ0#
AD1	C8	AD1	GNT0#	G4	PCI_GNT0#
AD2	D9	AD2	REQ1#/GPIO50	B6	BOARD_ID1
AD3	E12	AD3	GNT1#/GPIO51	A7	PCI_GNT1#
AD4	E9	AD4	REQ2#/GPIO52	E13	BOARD_ID2
AD5	C9	AD5	GNT2#/GPIO53	E12	PCI_GNT2#
AD6	E10	AD6	REQ3#/GPIO54	E6	BOARD_ID3
AD7	B7	AD7	GNT3#/GPIO55	F6	PCI_GNT3#
AD8	C7	AD8			
AD9	C5	AD9			
AD10	G11	AD10			
AD11	F8	AD11			
AD12	F11	AD12			
AD13	E7	AD13			
AD14	A3	AD14			
AD15	D2	AD15			
AD16	F10	AD16			
AD17	D5	AD17			
AD18	D10	AD18			
AD19	B3	AD19			
AD20	F7	AD20			
AD21	C3	AD21			
AD22	F3	AD22			
AD23	F4	AD23			
AD24	C1	AD24			
AD25	G7	AD25			
AD26	H7	AD26			
AD27	D1	AD27			
AD28	G5	AD28			
AD29	H6	AD29			
AD30	G1	AD30			
AD31	H3	AD31			

			C/BE0#	D8	CBE0#
			C/BE1#	B4	C/BE1#
			C/BE2#	D6	C/BE2#
			C/BE3#	A5	C/BE3#
			IRDY#	D3	PCI_IRDY#
			PAR	E3	PCI_PAR
			PCIRST#	R1	
			DEVSEL#	C6	PCI_DEVSEL#
			PERR#	E4	PCI_PERR#
			PLOCK#	C2	PCI_PLOCK#
			SERR#	J4	PCI_SERR#
			STOP#	A4	PCI_STOP#
			TRDY#	E5	PCI_TRDY#
			FRAME#	D7	PCI_FRAME#
			PLTRST#	C14	PLTRST#_NB
			PCICLK	D4	CLK_PCI_ICH
			PME#	R2	PCI_PME#

23 AD[0..31]

Interrupt I/F

23	PCI_PIRQA#	PIRQA#	PIRQE#/GPIO2	H4	GPIO2
	PCI_PIRQB#	PIRQB#	PIRQF#/GPIO3	K6	GPIO3
	PCI_PIRQC#	PIRQC#	PIRQG#/GPIO4	E2	ICH_GPIO4_PIRQG#
	PCI_PIRQD#	PIRQD#	PIRQH#/GPIO5	G2	ICH_GPIO5_PIRQH#

PCI_PIRQA# J5 — T130
PCI_PIRQB# E1 — T139
PCI_PIRQC# J6 — T132
PCI_PIRQD# C4

GPIO2 — T135
GPIO3 — T73
ICH_GPIO4_PIRQG# — T133
ICH_GPIO5_PIRQH# — T131

ICH9M REV 1.0

PCI_REQ0# 23 / PCI_GNT0# 23 / BOARD_ID1 16 — T127
BOARD_ID2 16 — T66
BOARD_ID3 16

C/BE0# 23 / C/BE1# 23 / C/BE2# 23 / C/BE3# 23

PCI_IRDY# 23 / PCI_PAR 23 / PCIRST# 20,23 / PCI_DEVSEL# 23 / PCI_PERR# / PCI_PLOCK# / PCI_SERR# / PCI_STOP# 23 / PCI_TRDY# 23 / PCI_FRAME# 23

CLK_PCI_ICH 2 / PCI_PME# 23

Reserved for EMI.
Place resister and cap close to ICH.

CLK_PCI_ICH — R447 33_4 — C482 22P/50V/NPO_4

EC B-8 /15 mount R447 and C482 for EMI request.

PLTRST#_NB 7

+3.3V_SUS — EC A-01 change to +3.3V_SUS for B test

C195 0.1U/10V/X5R_4

U10 TC7SH08FU(F)

PLTRST# 7,21,26,32

R118 100K_4

+3.3V — C559 0.1U/10V/X5R_4 — R506 10K/F_4

SPI_CLK_R — C558 *0.1U/10V/X5R_4 FAI Remove

U31

1	SPI_CS#0	R501	22_4	SPI_CS#0_R	
6	SPI_CLK	R503	22_4	SPI_CLK_R	
5	SPI_MOSI	R502	22_4	SPI_MOSI_R	
2	SPI_MISO	R504	22_4	SPI_MISO_R	
3	SPI_WP#				
7	SPI_HOLD#				

VDD 8 — VSS 4 — CE# — SCK — SI — SO — HOLD# — WP#

MX25L512MC-12G

R505 10K/F_4

EC B-12 /15 Add U31 for HDCP support.
512K byte SPI ROM
For HDCP only

PROJECT : SA6
Quanta Computer Inc.

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Custom	ICH9-M (USB,DMI,PCIE,PCI)	3B
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Non-iAMT ASF 2.0

Option to " Disable " clkrun. Pulling it down will keep the clks running.

LCD_ID

Place these close to ICH8.

U24C

ICH9M REV 1.0

Board ID	ID3	ID2	ID1	ID0
INTEL SENTAROSA	1	1	1	1
INTEL MENTAVIRA	1	1	0	1
AMD	1	0	1	1
NVIDIA	1	0	0	1

GPIO[20]--Integrated Pull-Down 20K.

EC A-03 Add R499 Pull high to +3.3V_S5

No Reboot strap.

ACZ_SPKR	Low = Default. High = No Reboot.

Non-iAMT For ME

PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (PM,GPIO,SMB,CL)	3B
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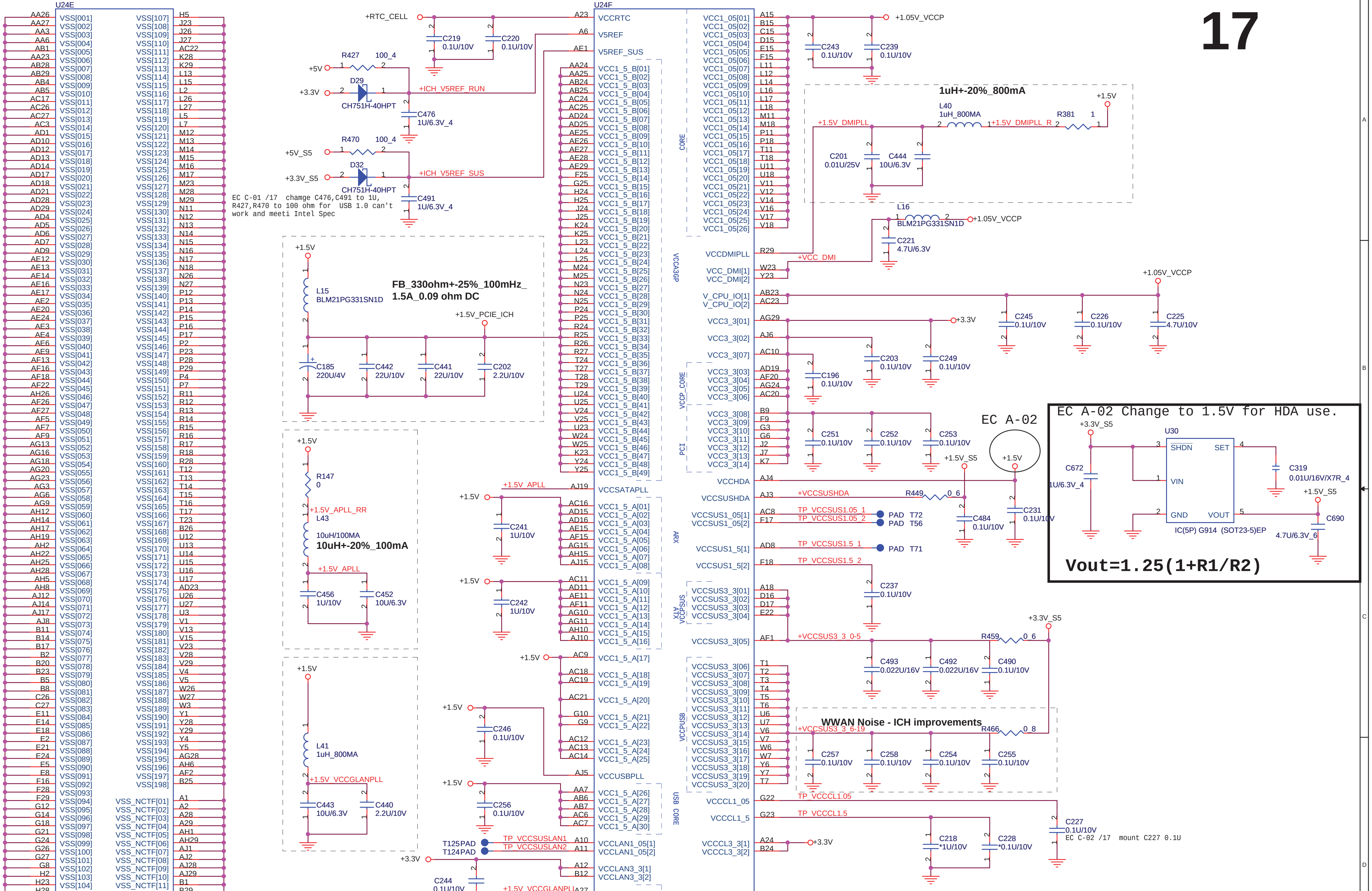

17
U24E
VSS[001] … VSS[106]
VSS[107] … VSS[198]
VSS_NCTF[01] … VSS_NCTF[12]
ICH9M REV 1.0
U24F
VCCRTC
V5REF
V5REF_SUS
VCC1_5_B[01] … VCC1_5_B[49]
VCC1_05[01] … VCC1_05[26]
CORE
VCCA3GP
VCCDMIPLL
VCC_DMI[1]
VCC_DMI[2]
V_CPU_IO[1]
V_CPU_IO[2]
VCC3_3[01] … VCC3_3[14]
VCCP_CORE
PCI
VCCHDA
VCCSUSHDA
VCCSUS1_05[1]
VCCSUS1_05[2]
VCCSUS1_5[1]
VCCSUS1_5[2]
VCCSATAPLL
VCC1_5_A[01] … VCC1_5_A[30]
ARX
VCCSUS3_3[01] … VCCSUS3_3[20]
VCCPSUS ATX
VCCPUSB
VCCUSBPLL
USB CORE
VCCCL1_05
VCCCL1_5
VCCCL3_3[1]
VCCCL3_3[2]
VCCLAN1_05[1]
VCCLAN1_05[2]
VCCLAN3_3[1]
VCCLAN3_3[2]
VCCGLANPLL
VCCGLAN1_5[1] … VCCGLAN1_5[4]
VCCGLAN3_3
GLAN POWER
ICH9M REV 1.0
+RTC_CELL
C219 0.1U/10V
C220 0.1U/10V
R427 100_4
+5V
D29 CH751H-40HPT
+3.3V
+ICH_V5REF_RUN
C476 1U/6.3V_4
R470 100_4
+5V_S5
D32 CH751H-40HPT
+3.3V_S5
+ICH_V5REF_SUS
C491 1U/6.3V_4
EC C-01 /17 chamge C476,C491 to 1U,
R427,R470 to 100 ohm for USB 1.0 can't
work and meeti Intel Spec
+1.5V
L15 BLM21PG331SN1D
FB_330ohm+-25%_100mHz_
1.5A_0.09 ohm DC
+1.5V_PCIE_ICH
C185 220U/4V
C442 22U/10V
C441 22U/10V
C202 2.2U/10V
R147 0
+1.5V_APLL_RR
L43 10uH/100MA
10uH+-20%_100mA
+1.5V_APLL
C456 1U/10V
C452 10U/6.3V
L41 1uH_800MA
+1.5V_VCCGLANPLL
C443 10U/6.3V
C440 2.2U/10V
C241 1U/10V
C242 1U/10V
C246 0.1U/10V
C256 0.1U/10V
TP_VCCSUSLAN1
TP_VCCSUSLAN2
T125 PAD
T124 PAD
C244 0.1U/10V
C204 4.7U/6.3V
+1.05V_VCCP
C243 0.1U/10V
C239 0.1U/10V
1uH+-20%_800mA
L40 1uH_800MA
+1.5V_DMIPLL
+1.5V_DMIPLL_R
R381 1
C201 0.01U/25V
C444 10U/6.3V
L16 BLM21PG331SN1D
C221 4.7U/6.3V
+VCC_DMI
C245 0.1U/10V
C226 0.1U/10V
C225 4.7U/10V
C203 0.1U/10V
C249 0.1U/10V
C196 0.1U/10V
C251 0.1U/10V
C252 0.1U/10V
C253 0.1U/10V
EC A-02
+1.5V_S5
+VCCSUSHDA
R449 0_6
C484 0.1U/10V
C231 0.1U/10V
TP_VCCSUS1.05_1
TP_VCCSUS1.05_2
PAD T72
PAD T56
TP_VCCSUS1.5_1
PAD T71
TP_VCCSUS1.5_2
C237 0.1U/10V
+VCCSUS3_3_0-5
R459 0_6
C493 0.022U/16V
C492 0.022U/16V
C490 0.1U/10V
WWAN Noise - ICH improvements
+VCCSUS3_3_6-19
R466 0_8
C257 0.1U/10V
C258 0.1U/10V
C254 0.1U/10V
C255 0.1U/10V
TP_VCCCL1.05
TP_VCCCL1.5
C218 *1U/10V
C228 *0.1U/10V
C227 0.1U/10V
EC C-02 /17 mount C227 0.1U
EC A-02 Change to 1.5V for HDA use.
U30
SHDN
SET
VIN
GND
VOUT
IC(5P) G914 (SOT23-5)EP
C672 1U/6.3V_4
C319 0.01U/16V/X7R_4
C690 4.7U/6.3V_6
Vout=1.25(1+R1/R2)

PROJECT : SA6

Quanta Computer Inc.

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Custom	ICH9-M (POWER,GND)	3B

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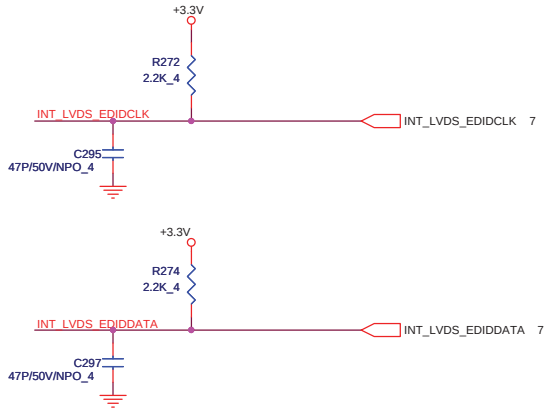
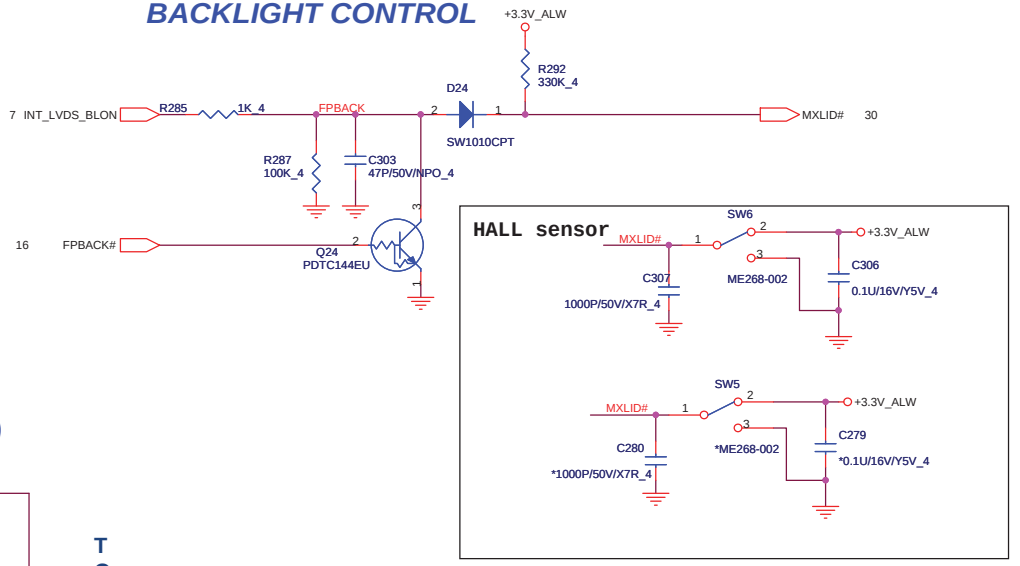
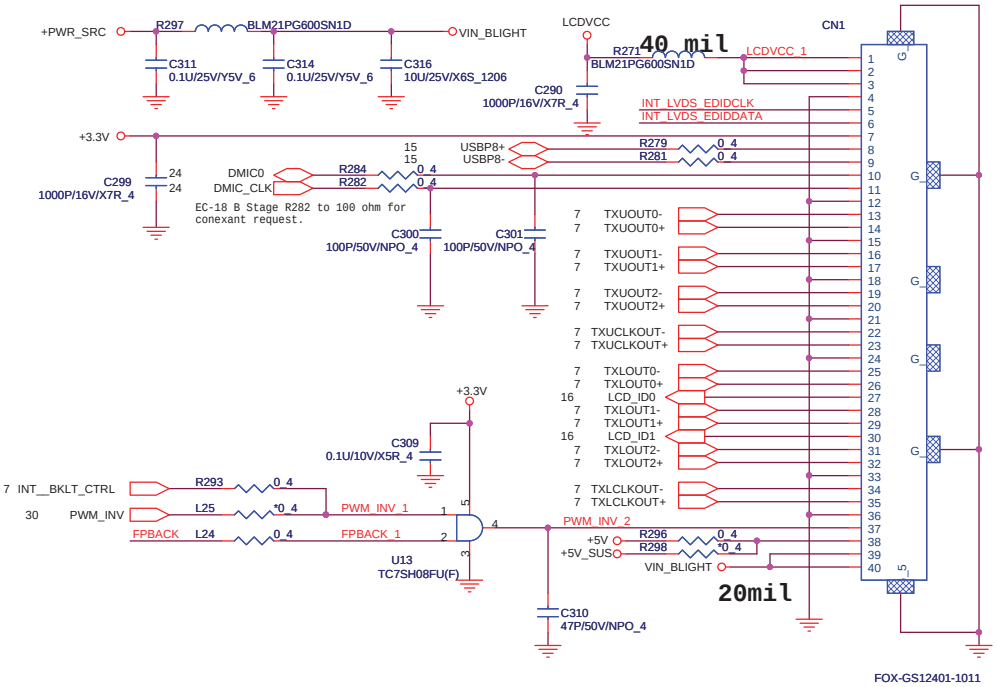


BACKLIGHT CONTROL

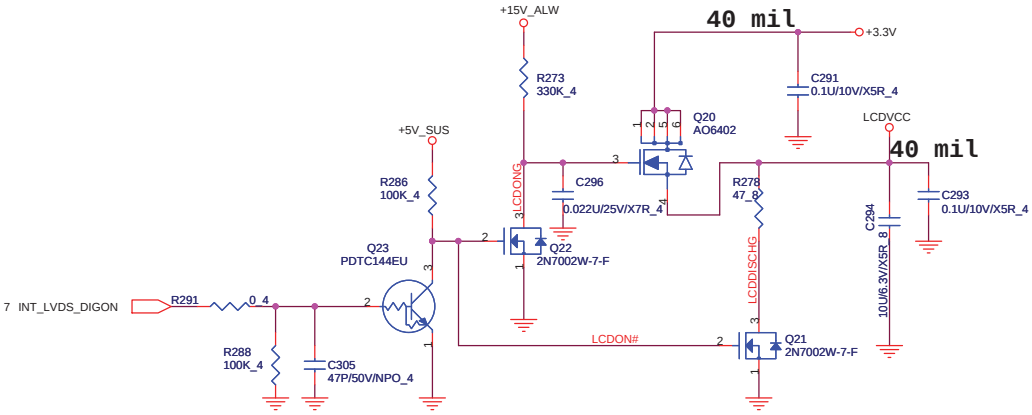


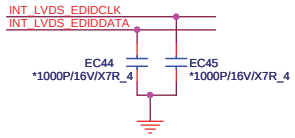
LCD CONNECTOR(Include WEB CAM function)



TO PANEAL

PANEL VCC CONTROL





PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	3B
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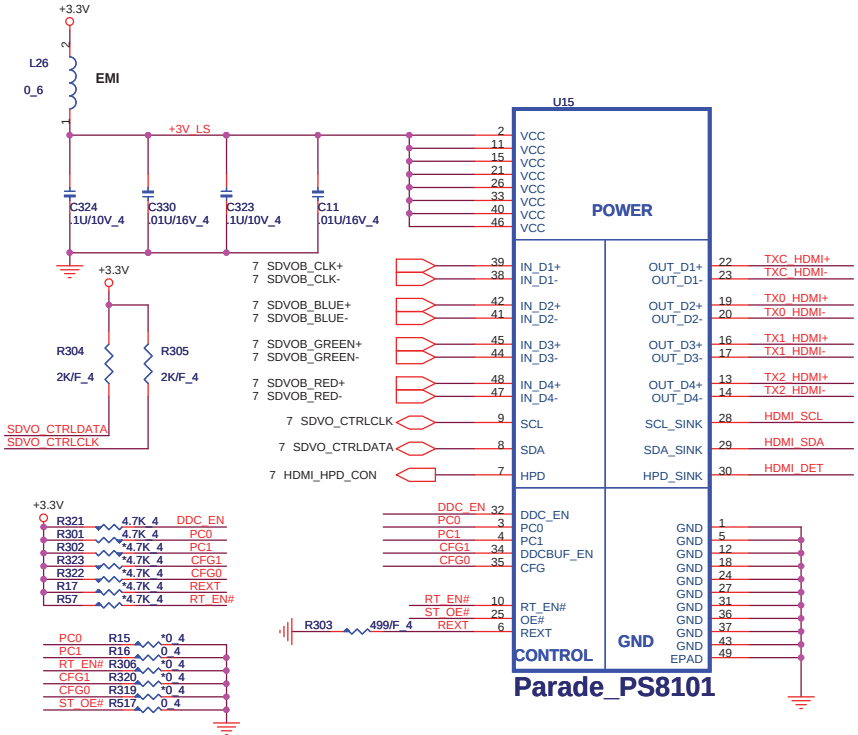
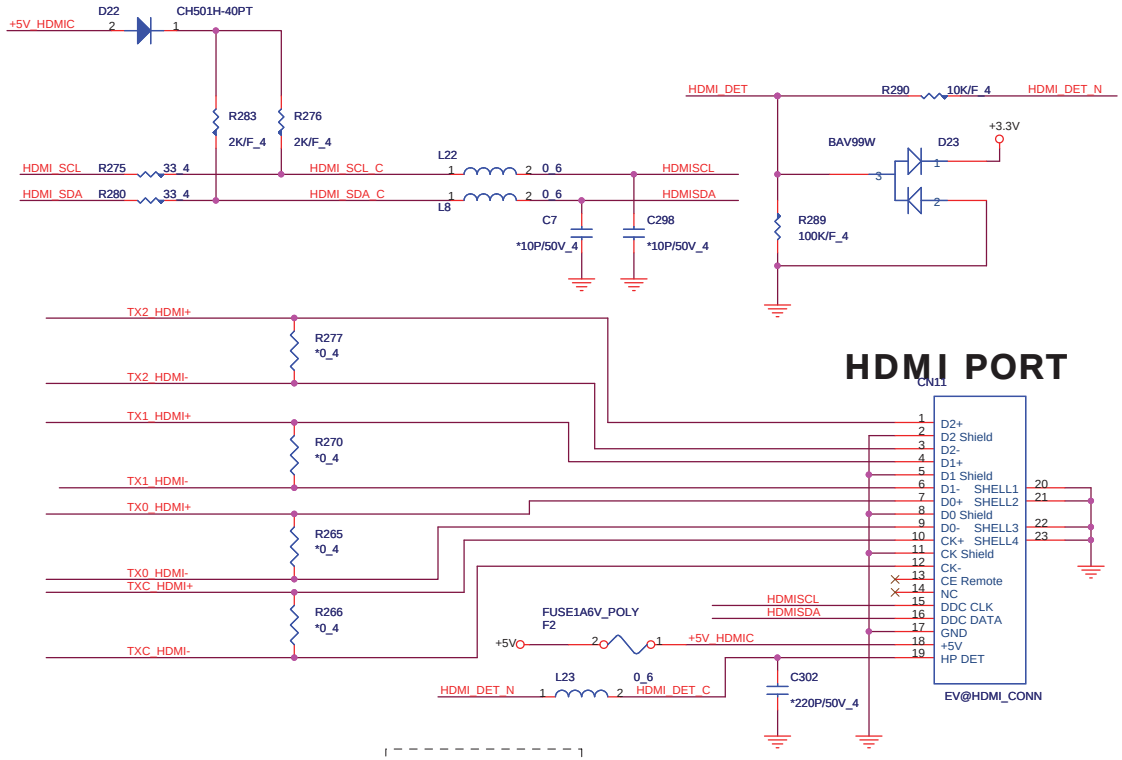
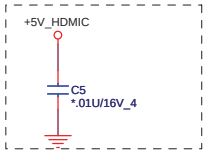
For UMA HDMI function







for EMI request

EC C-05 /19 change Pin 25 connect to GND.

EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

SCLZ/SDAZ Low-level input/output Voltage
CFG1:CFG0=0:0 VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1 VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0 VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1 VIL:<0.36V VOL:0.6V

Use Pericom ST
Add R15,R16,R306,R319,R320 0 ohm. R303 4.7K
R277,R270,R265,R266 mount 0.2P.

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Quanta Computer Inc.

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Custom	HDMI	3B
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CRT PORT

ESD PORTECTION

EC A-08 /20 change VGA Pin 9 Desgin in B Stage.

CRTVDD_5V
D20
EC10QS04
+5V
F1
POLY SWITCH 1.1A
CRTVDD2

+3.3V R268 2.2K_4
7 INT_CRT_DDCCLK
Q17 2N7002E
DDCCLK

7 INT_VSYNC
Q18 RHU002N06
CRT_VS_1

7 INT_HSYNC
Q19 RHU002N06
CRT_HS_1

DDCDAT
+3.3V R267 2.2K_4
7 INT_CRT_DDCDAT
Q16 2N7002E

+5V C292 0.1U/16V/Y5V_4
15,23 PCIRST#
U12 TC7SH08FU(F)
+5V R269 *2.2K_4

7 INT_CRT_RED INT_CRT_GRN INT_CRT_BLU
R5 150/F R8 150/F R6 150/F
RED_PI GEN_PI BLU_PI
L1 BK1608LL300 CRT_R_1
L6 BK1608LL300 CRT_G_1
L4 BK1608LL300 CRT_B_1
C1 *5.6P/50V_4 C3 *5.6P/50V_4 C4 *5.6P/50V_4
C289 5.6P/50V_4 C284 5.6P/50V_4 C283 5.6P/50V_4
C282 0.1U/10V/X7R_4
CN9 CRT_CONN
T83
CRT_SENSE# T1
C287 *180P

CRTVDD_5V
R2 2.2K DDCCLK
DDCDAT R4 2.2K

DDCCLK L2 BK1608HM121 DDCCLK_2
CRT_VS1 L5 BK1608HM121 CRT_VS_2
CRT_HS1 L7 BK1608HM121 CRT_HS_2
DDCDAT L3 BK1608HM121 DDCDAT_2
C286 *33P C285 *33P C2 *33P C288 *33P

CRTVDD_5V
C6 0.1U/10V/X7R_4
R9 1K_4
U1 AHCT1G125DCH
CRT_VS_1 CRT_VS0 R3 10_4 CRT_VS1
CRT_HS_1 CRT_HS0 R7 10_4 CRT_HS1
U2 AHCT1G125DCH
Layout Note: Place near U < 200 mil

CRTVDD_5V +3.3V
D15 *BC000204Z21 CRT_R_1
D16 *BC000204Z21 CRT_G_1
D19 *BC000204Z21 CRT_B_1
D14 *BC000204Z21 CRT_VS_2
D18 *BC000204Z21 CRT_HS_2
D21 *BC000204Z21 DDCCLK_2
D17 *BC000204Z21 DDCDAT_2

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Quanta Computer Inc.

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Custom	CRT PORT	3B
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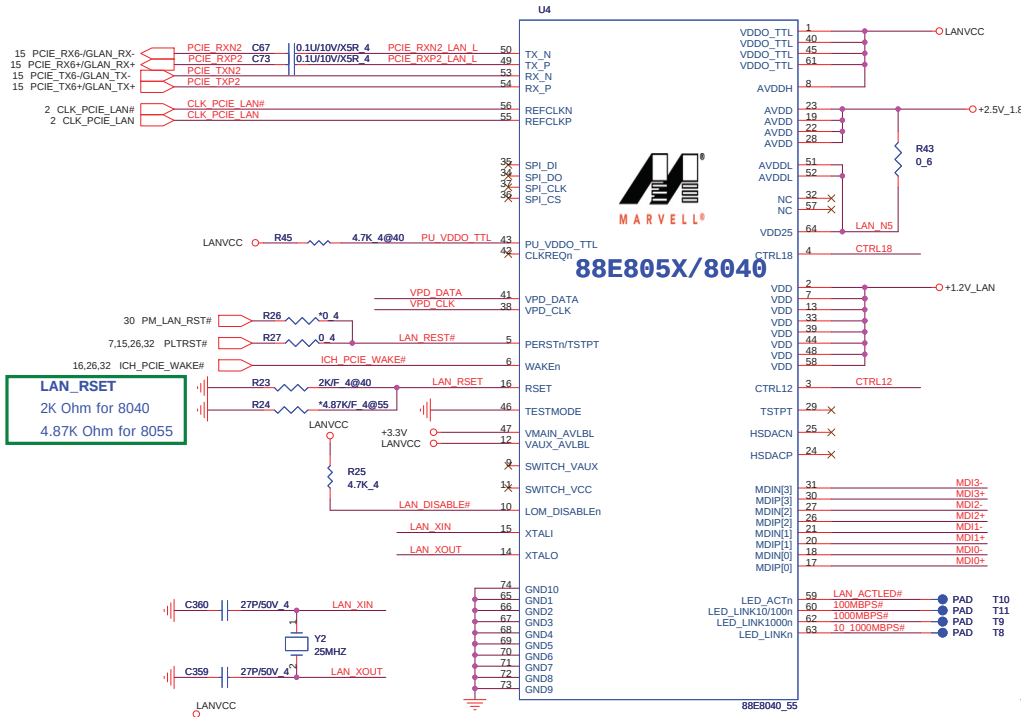
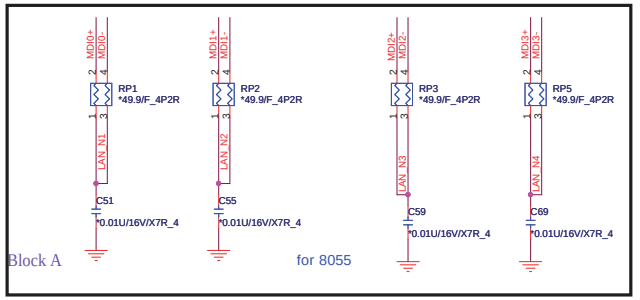
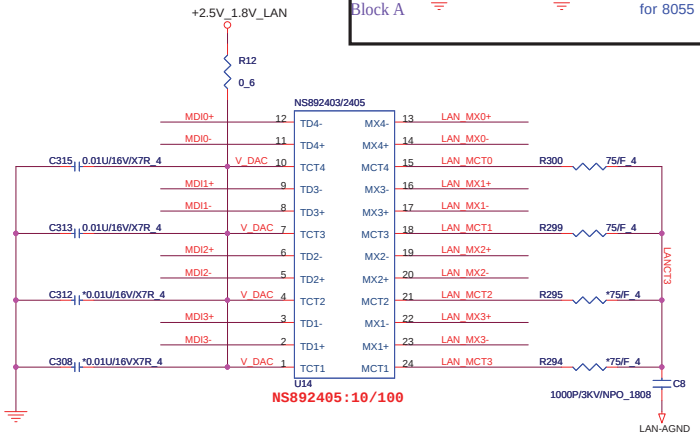
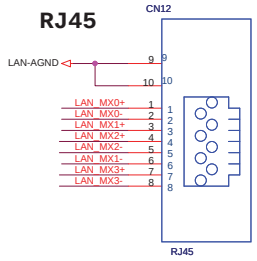
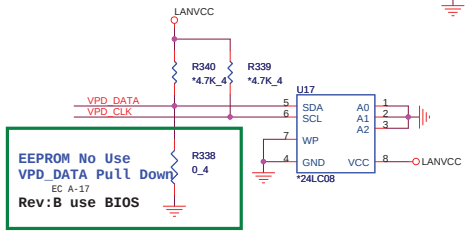


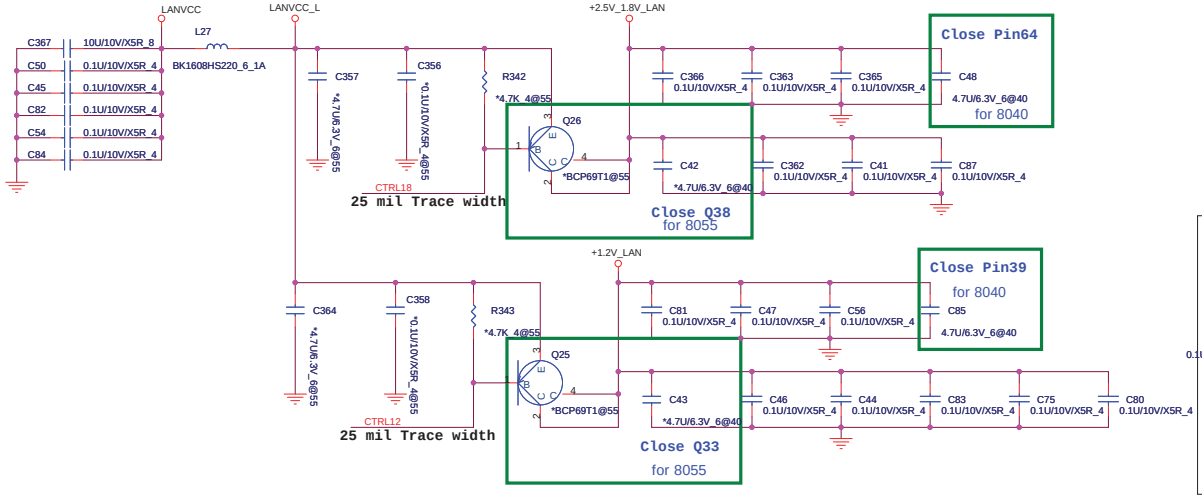


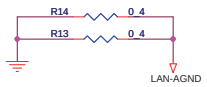




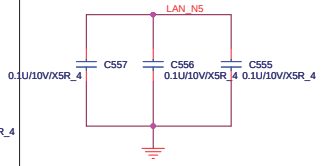


	ASM	No ASM
Use BIOS	R338	R340, R339,U17
EEPROM	R340, R339,U17	R338





EC A-09 /21 Add C557,C558,C555 for EMI Request.



	ASM	No ASM
88E8040	C48,C85,R23	RP1,RP2,RP3,RP5 C51,C55,C59,C69 ,C312,C308 Q25,Q26,C42,C43 R524,R294,R295 U4(8040),U14 10/100 C356,C357,C358,C364,R342,R343
88E8055	RP1,RP2,RP3,RP5 C51,C55,C59,C69 ,C312,C308 Q25,Q26,C42,C43 R524,R294,R295 U4(8040),U14 10/100 C356,C357,C358,C364,R342,R343	C48,C85,R23

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Quanta Computer Inc.

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Quanta Computer Inc.

Size	Document Number	Rev
C	LAN Power	3B

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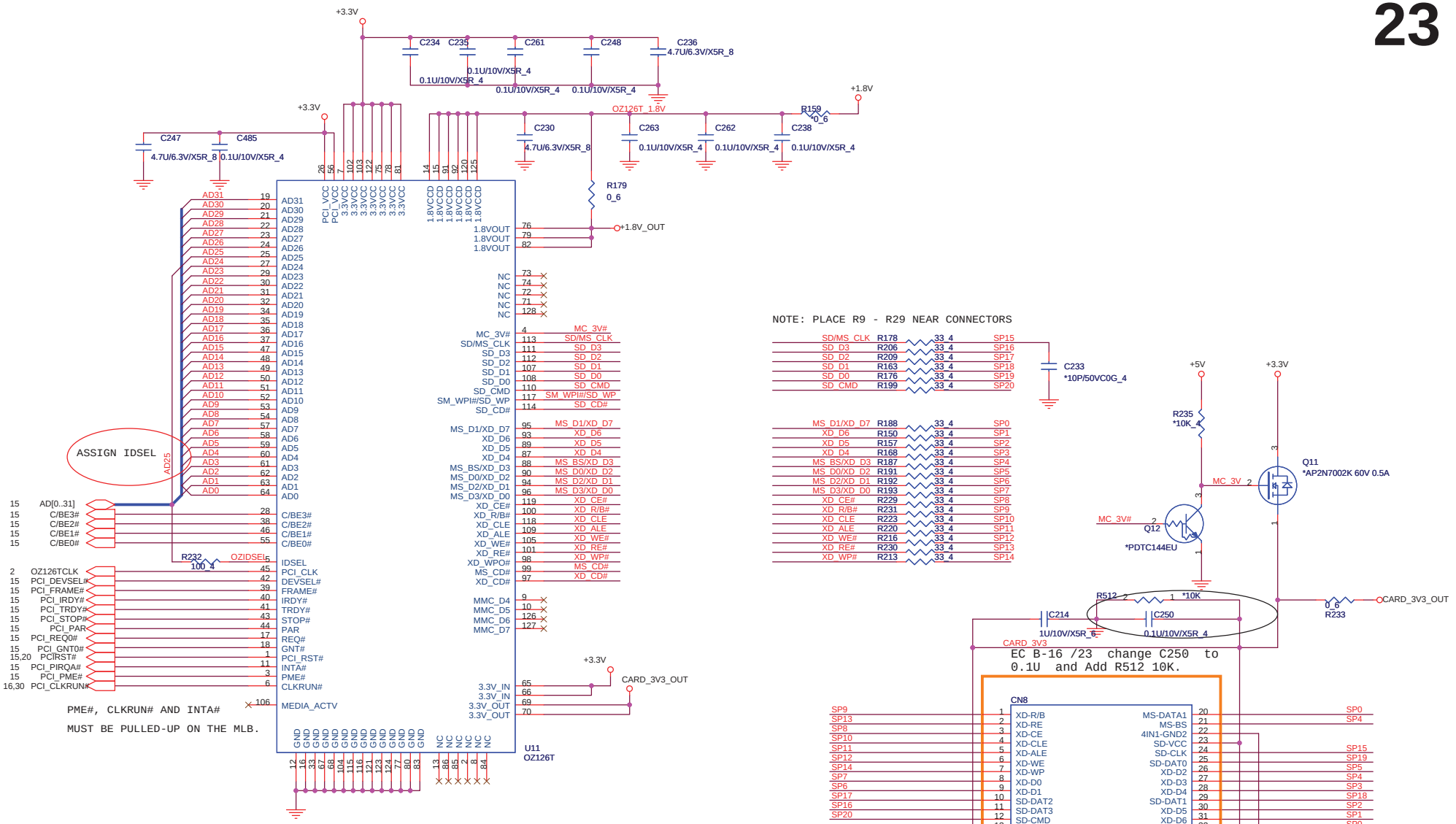

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Quanta Computer Inc.			
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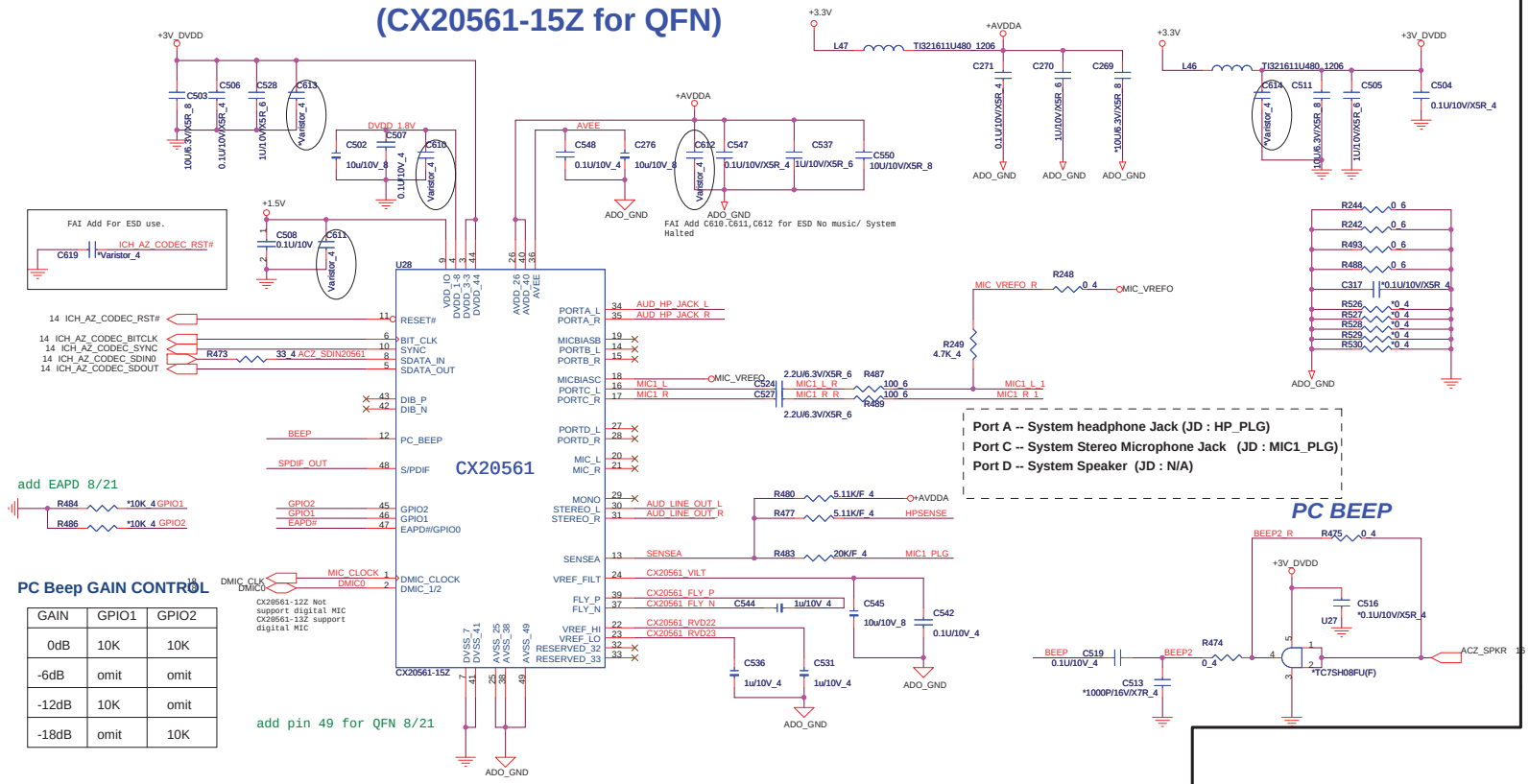
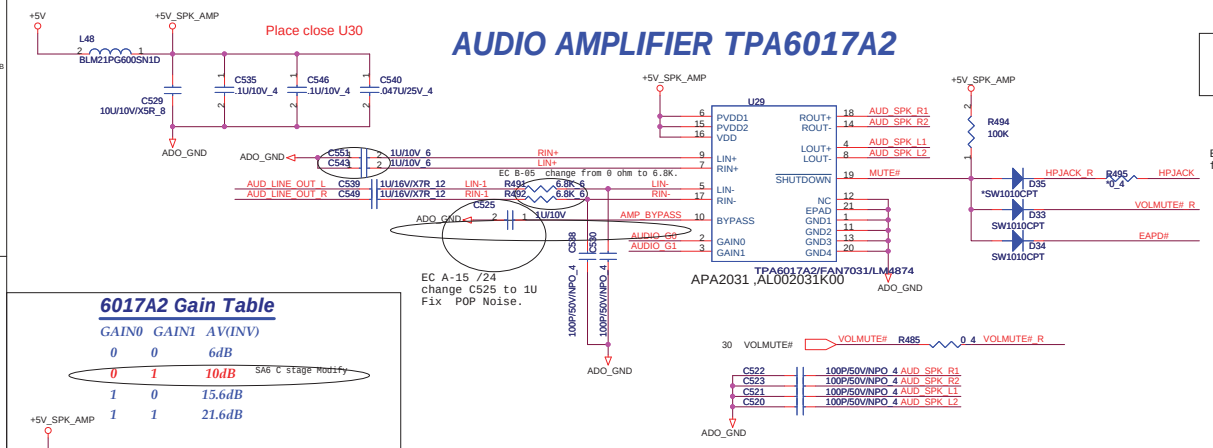
(CX20561-15Z for QFN)



PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	10K

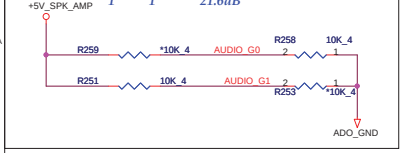
AUDIO AMPLIFIER TPA6017A2



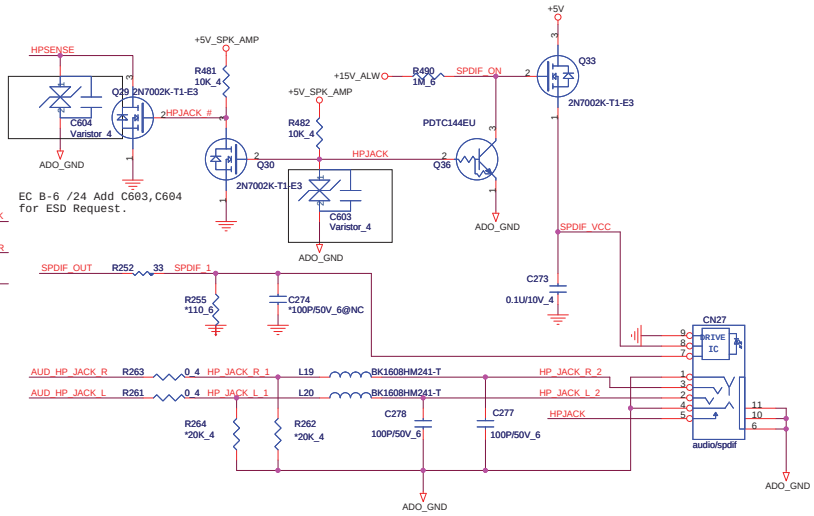
6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

SA6 C stage Modify



Headphone out + Spdif Out (normal open)



PROJECT : SA6
Quanta Computer Inc.
Size C | Document Number AUDIO(CX20561)&CONN | Rev 3B
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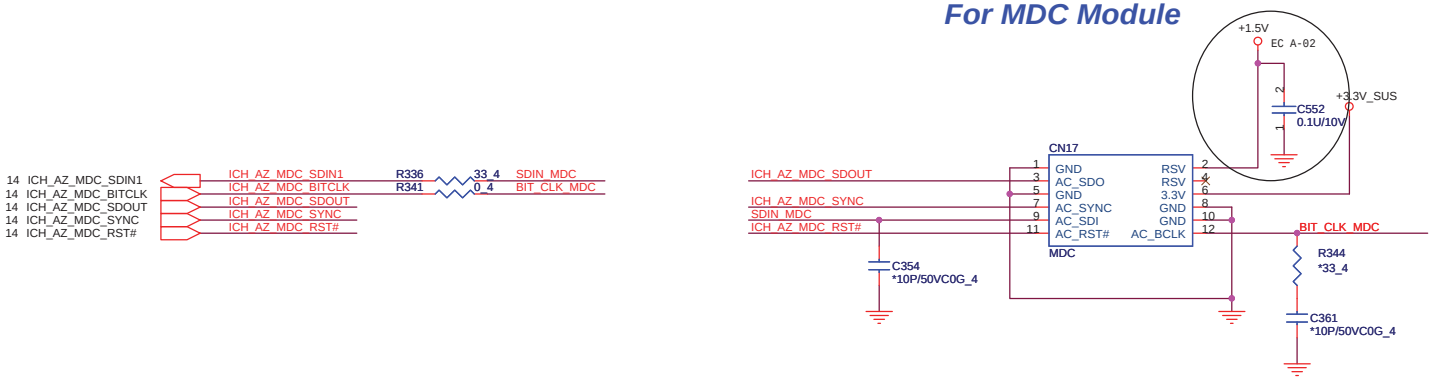
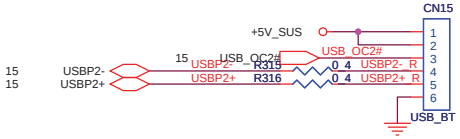
For MDC Module



TO RJ11/USB PORT



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(MDC)/RJ11 BOARD	3B

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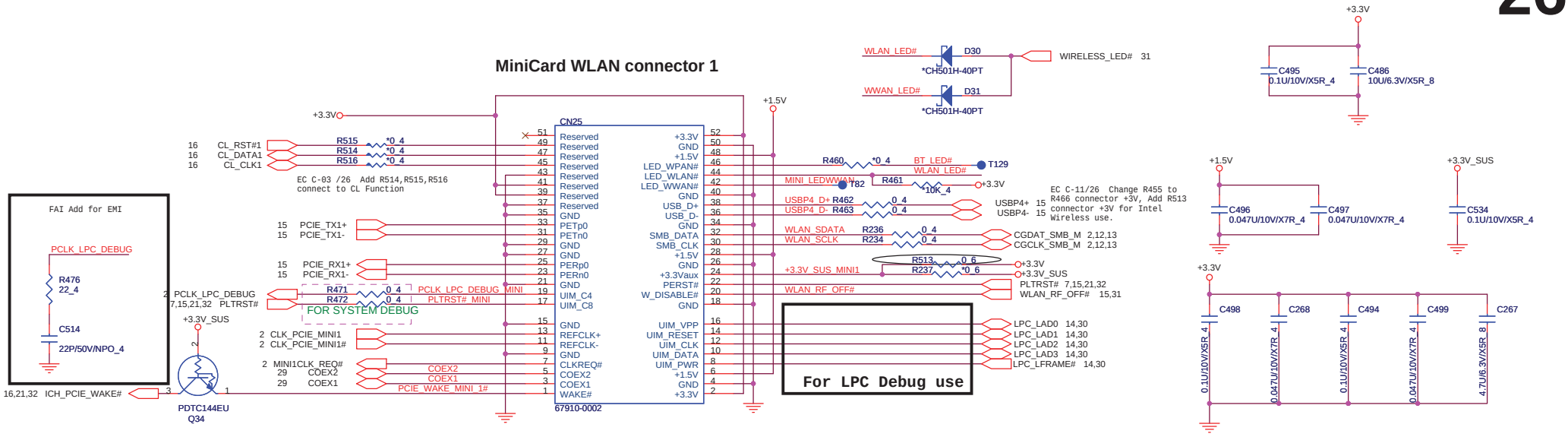
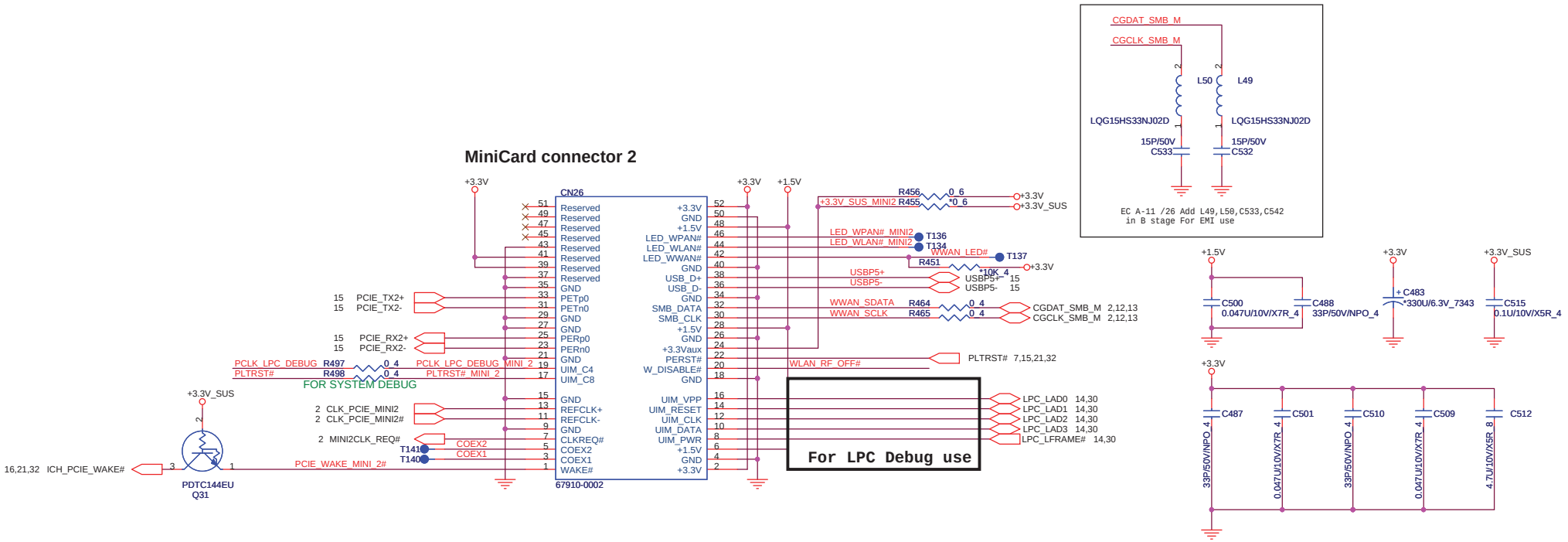
MiniCard WLAN connector 1



MiniCard connector 2



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Quanta Computer Inc.		
Size: Custom	Document Number: MINI PCI-E Card	Rev: 3B
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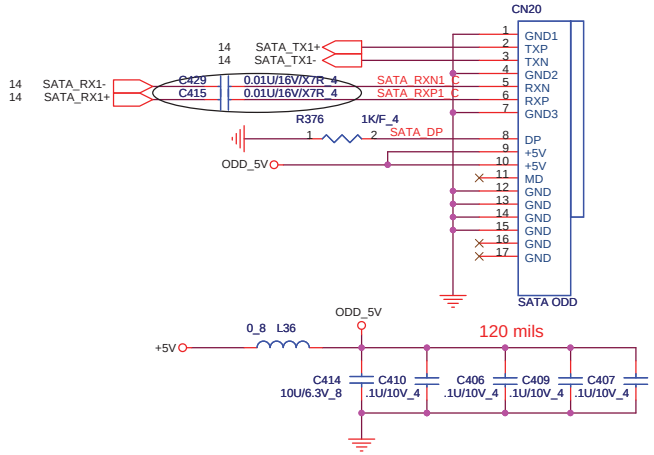
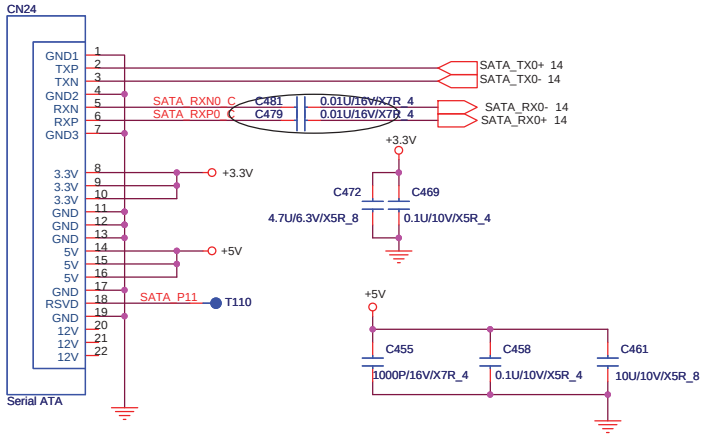
SATA CD-ROM



EC C-06 /27 change C479,C481,C415,C429 to 0.01U for meet Intel Spc.

SATA CONNECTOR



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD ODD	3B
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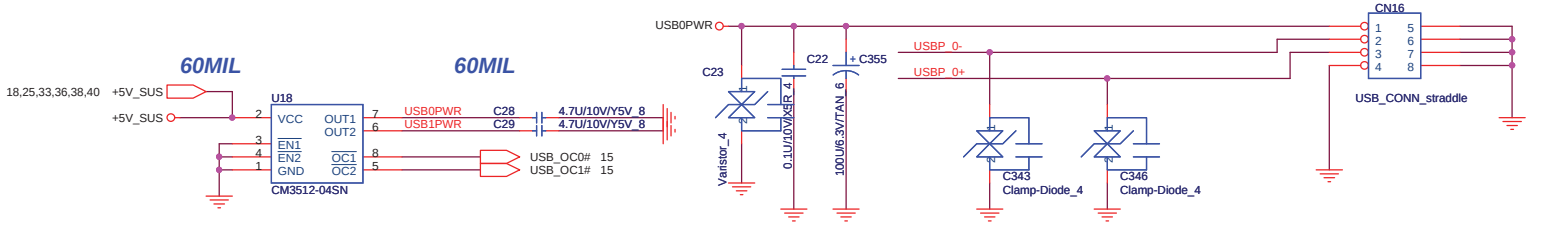
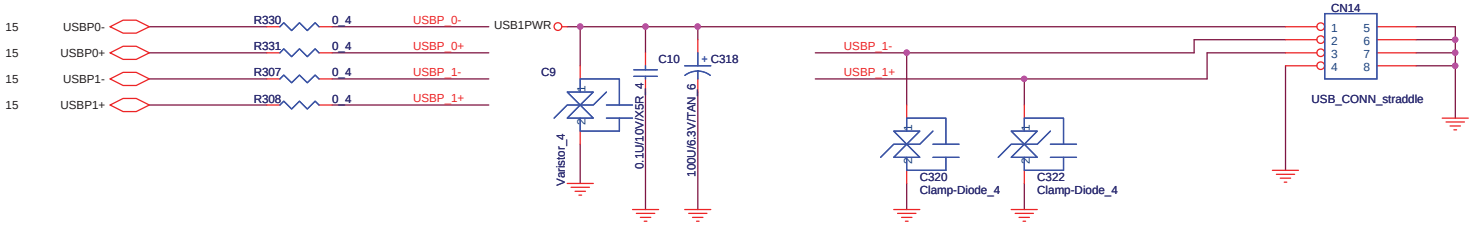
USB-0



USB-1



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Quanta Computer Inc.

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Custom	USB CONN	3B

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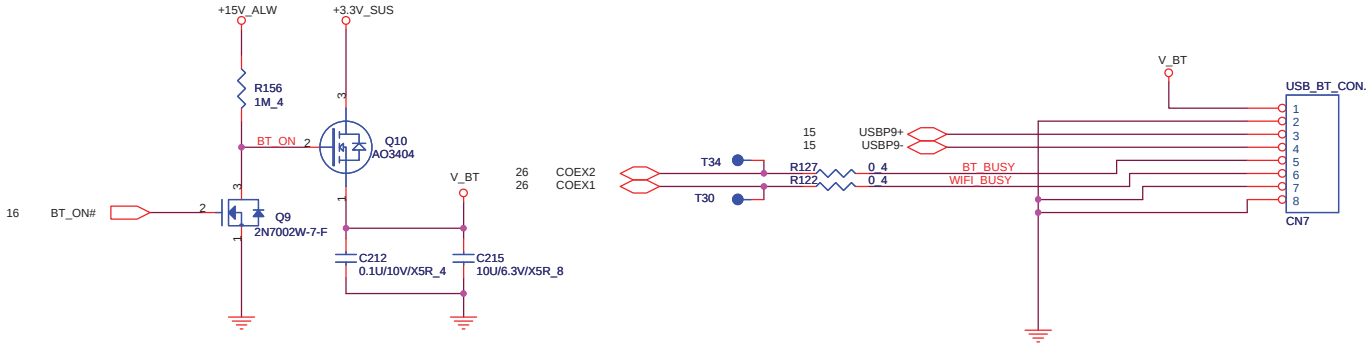
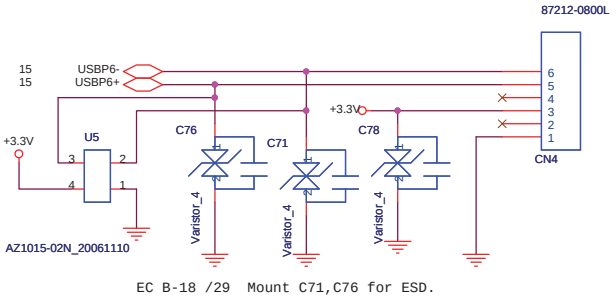
BLUETOOTH CONNECTOR



FINGERPRINT CONNECTOR



EC B-18 /29 Mount C71,C76 for ESD.

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Quanta Computer Inc.

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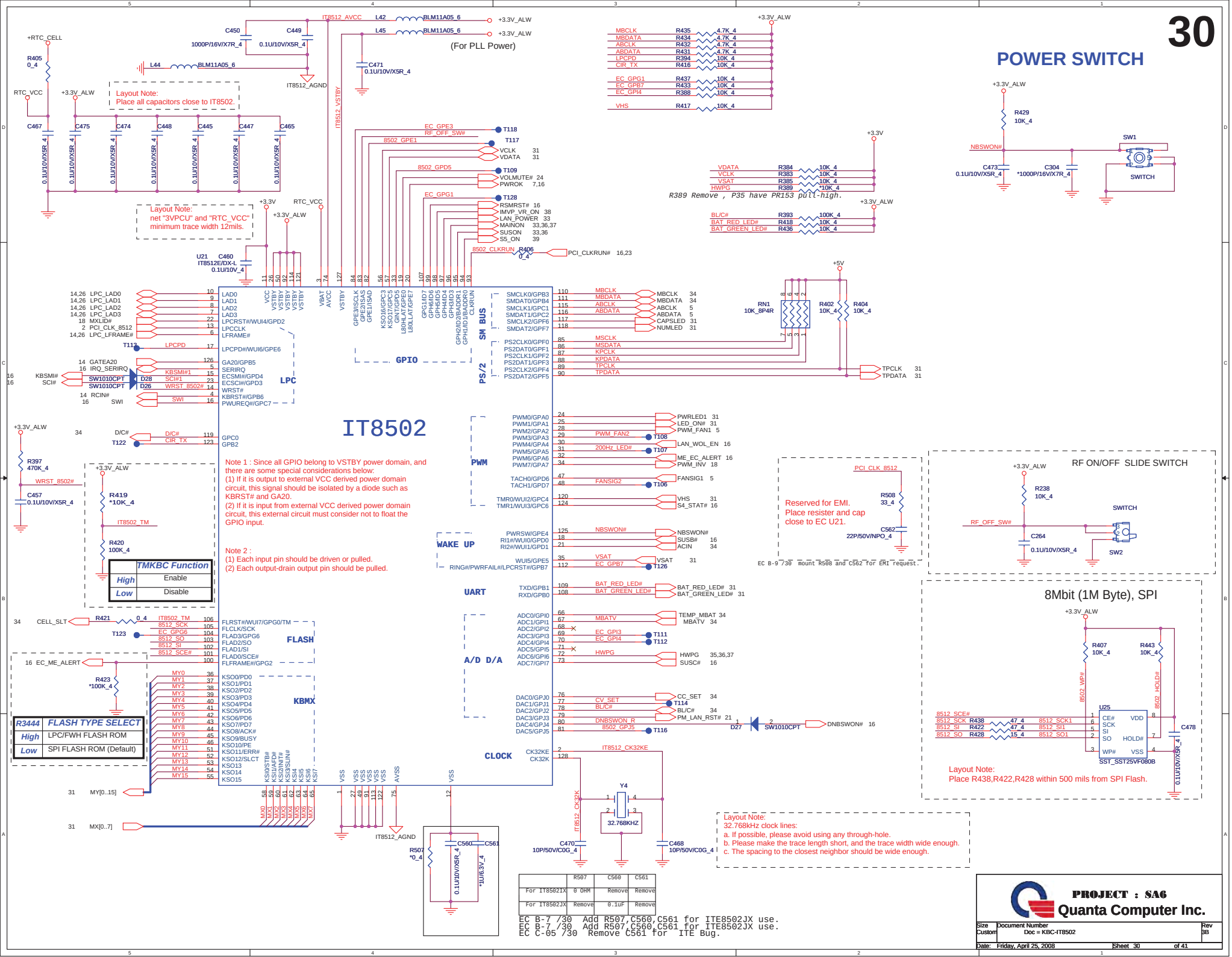
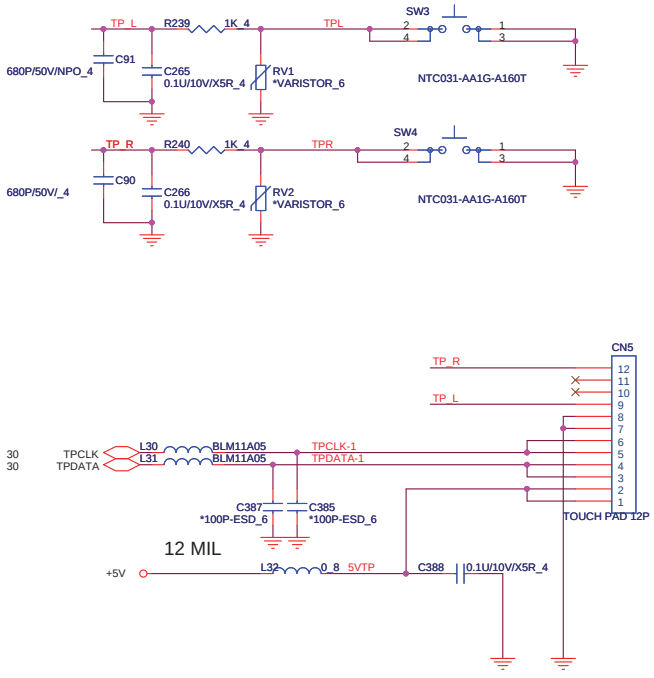
POWER SWITCH

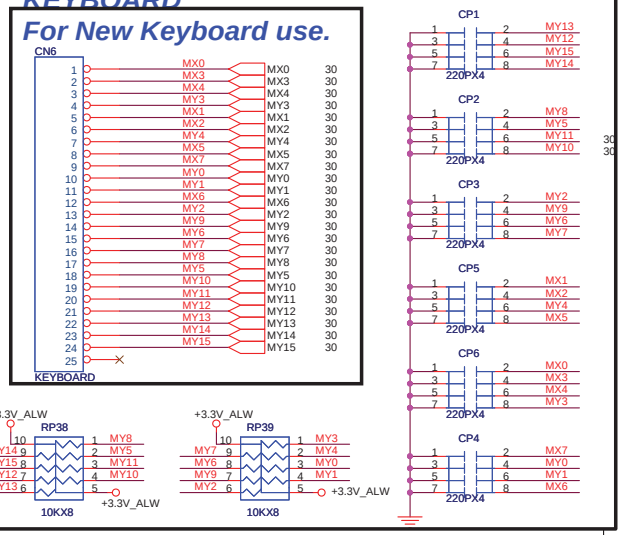


TOUCHPAD SWITCH CONN

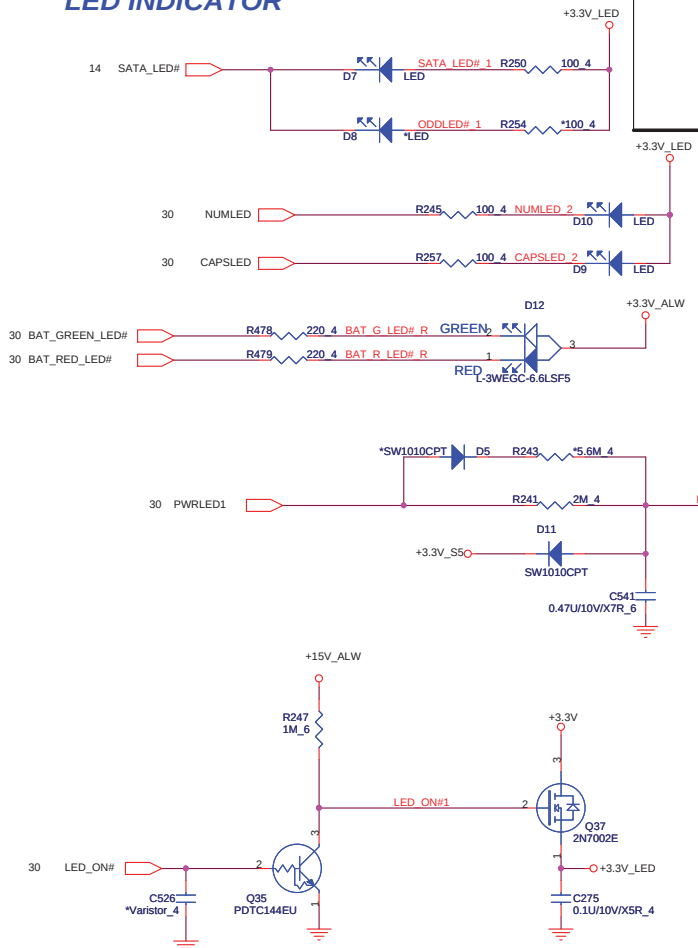


KEYBOARD

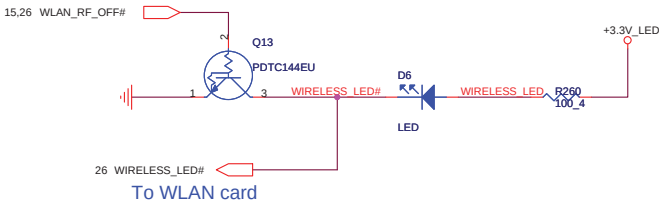
For New Keyboard use.

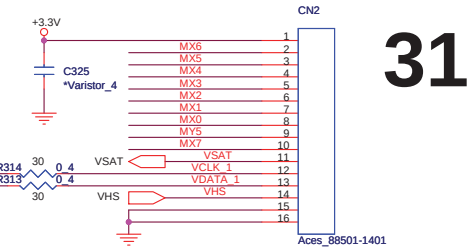


LED INDICATOR

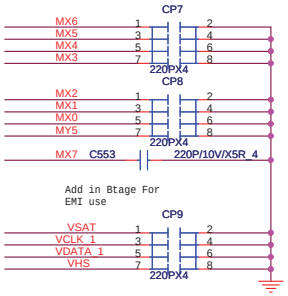


WIRELESS LED



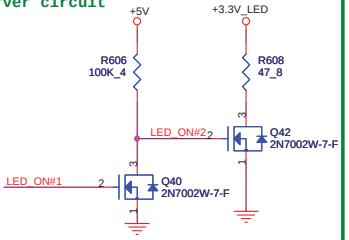


EC A-12 /31 Add CP7 CP8 C553 in B stage For EMI use



SWITCH/Volume cintral BOARD

EC A-13 /31 for LED +3.3V leak electricity. reserver circuit



EC B-15 /31 change R608 to 0805 and Q40 change to 2N7002.

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Quanta Computer Inc.

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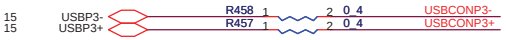
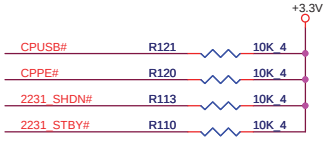
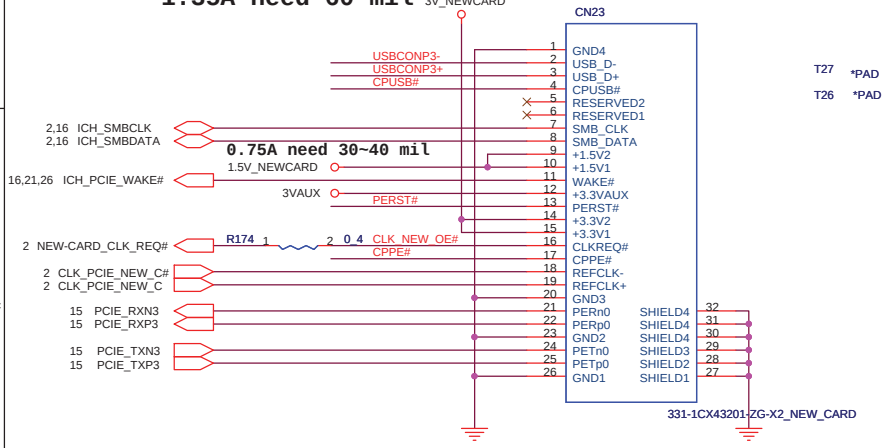
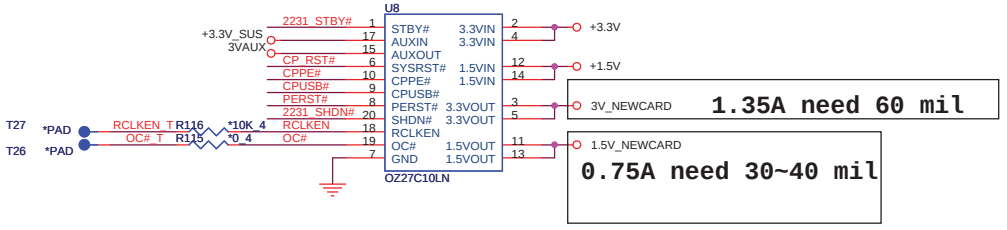
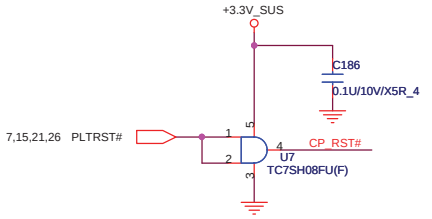
NEWCARD

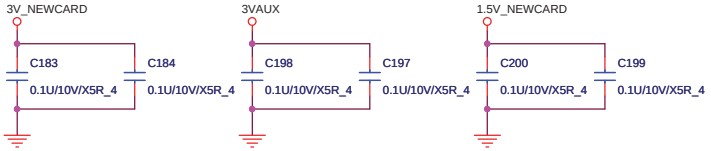












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Size	Document Number	Rev
Custom	NEW CARD	3B

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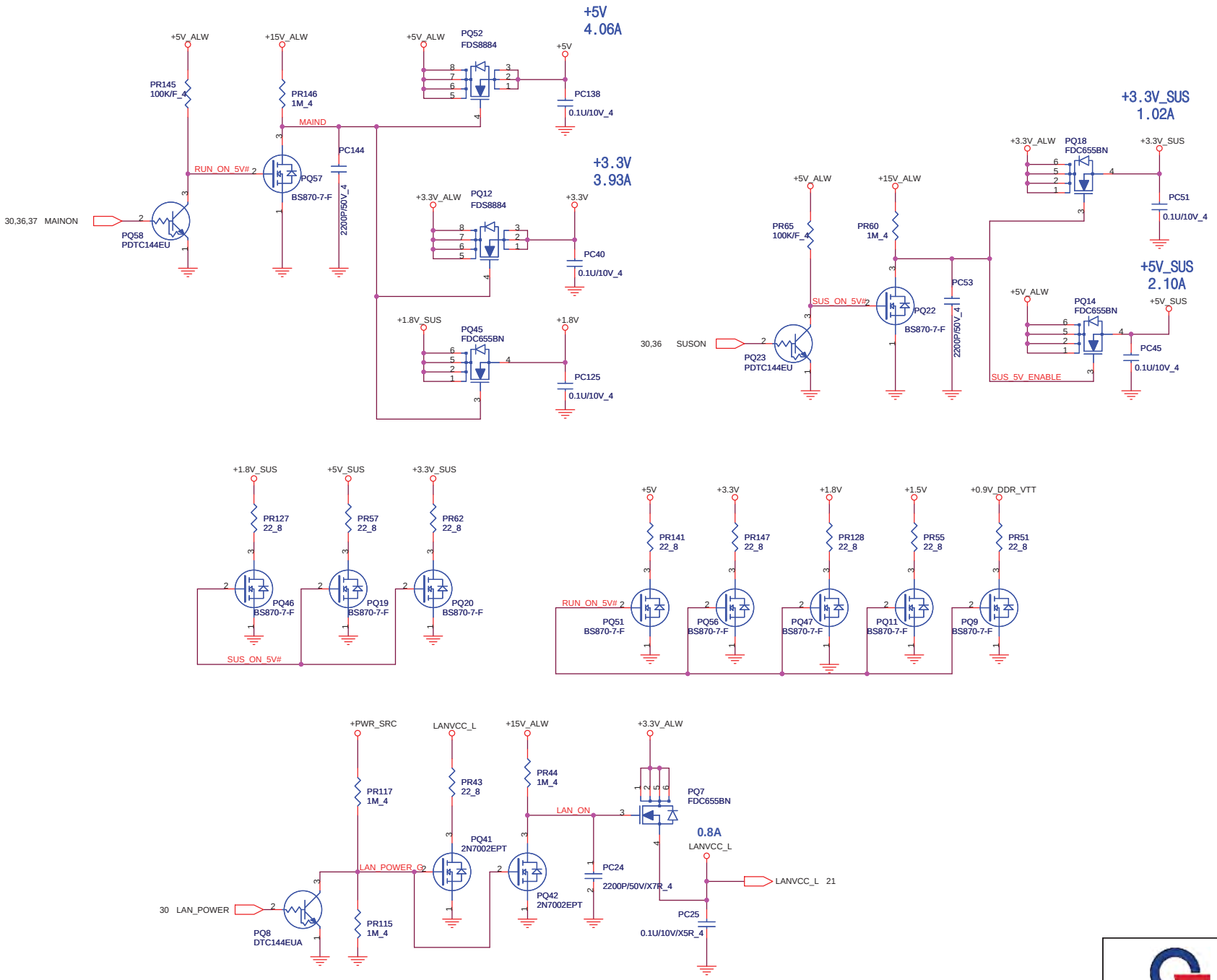

PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RUN POWER SW & DISCHARGER	3B

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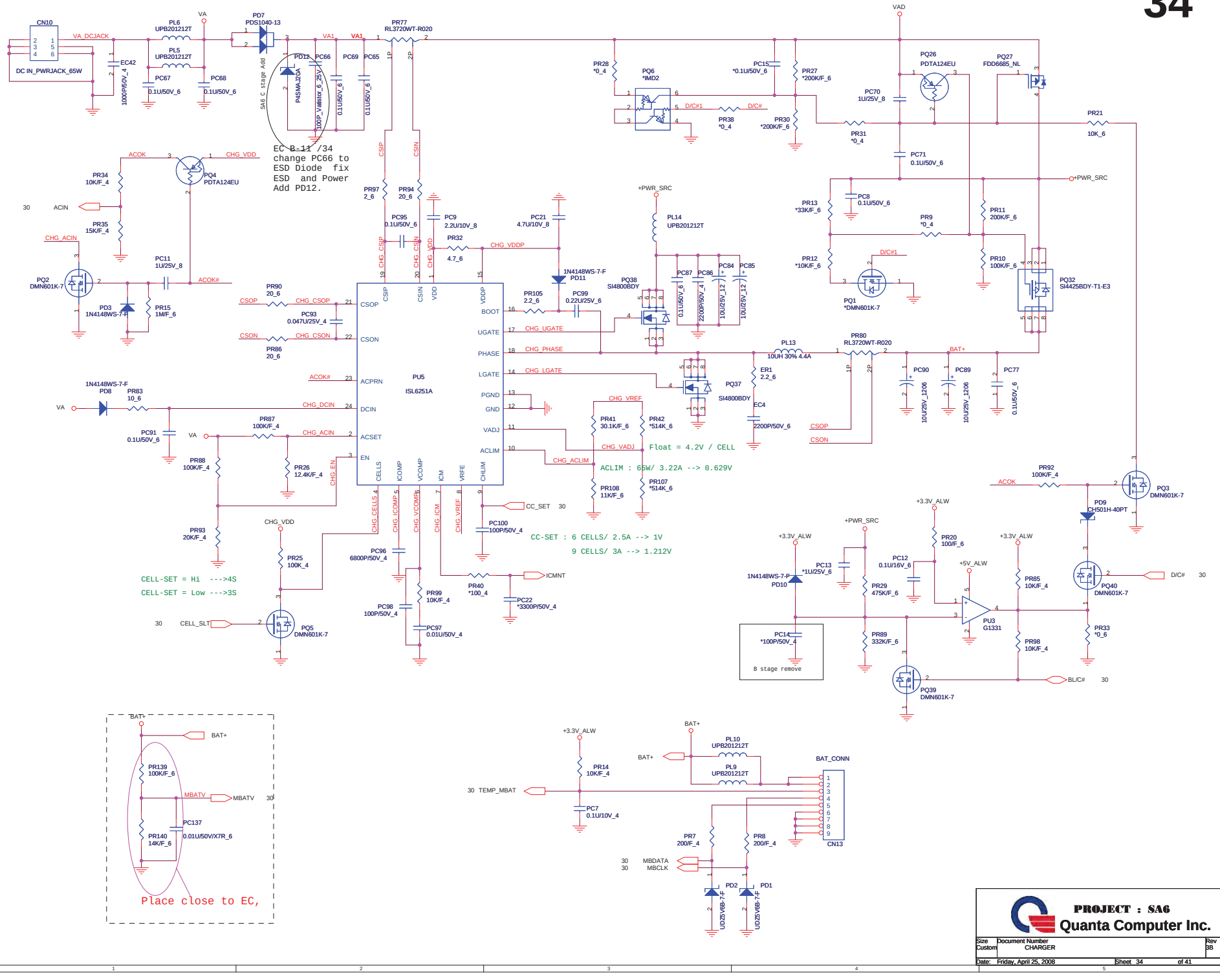

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	CHARGER	3B

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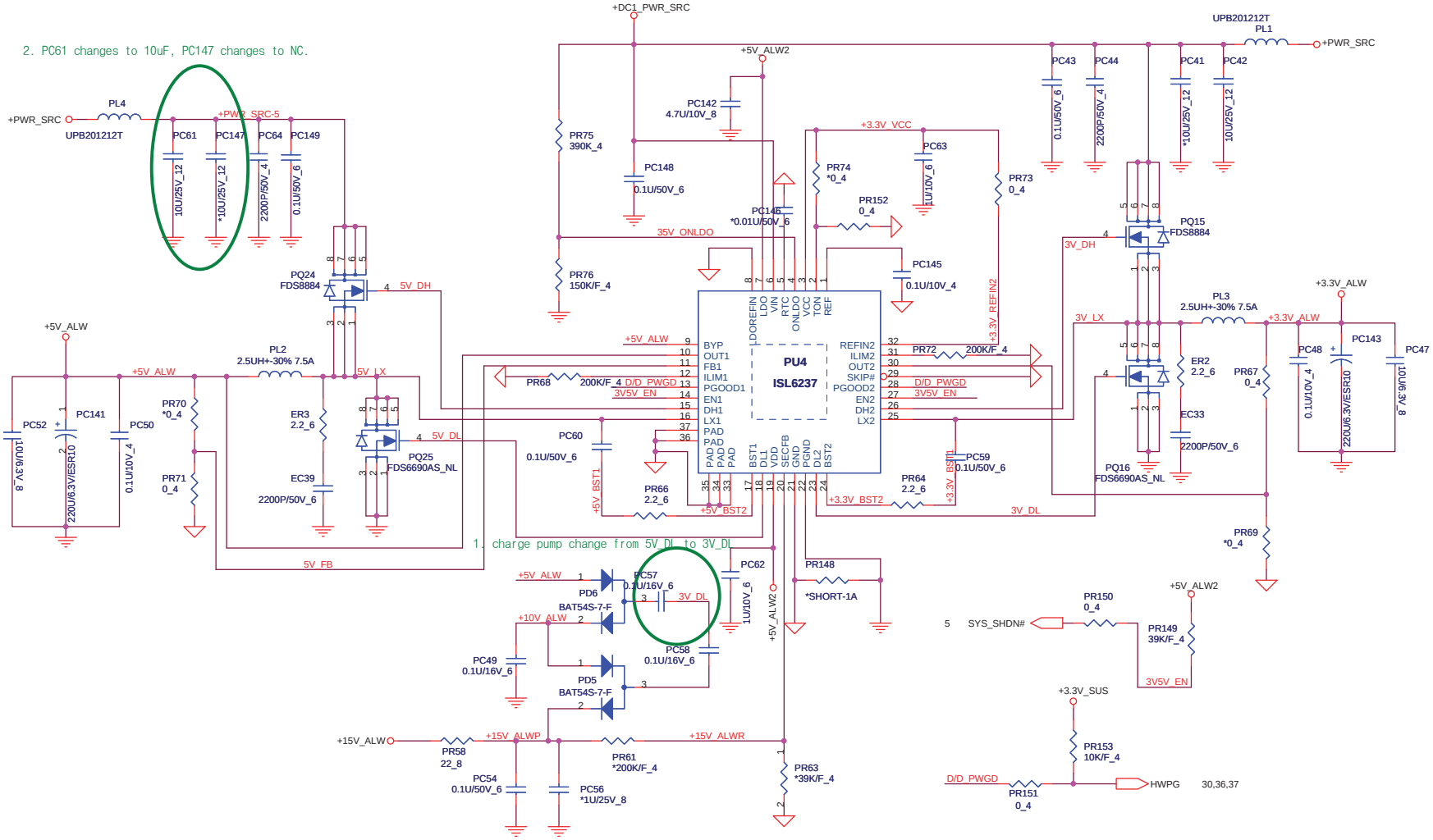

PROJECT : SA6			
Quanta Computer Inc.			
Size: Custom	Document Number: D/D POWER		Rev: 3B
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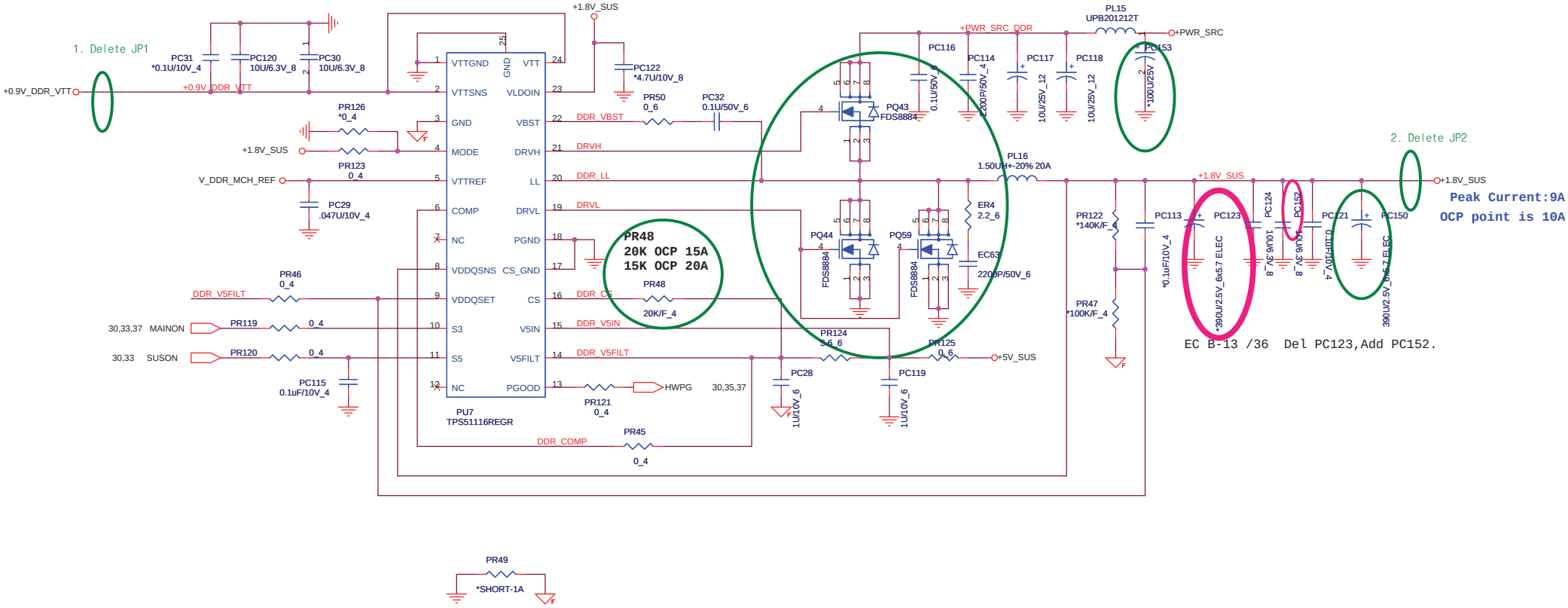

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Quanta Computer Inc.			
Size: Custom	Document Number: DDR2_1.8VSUS,0.9V		Rev: 3B
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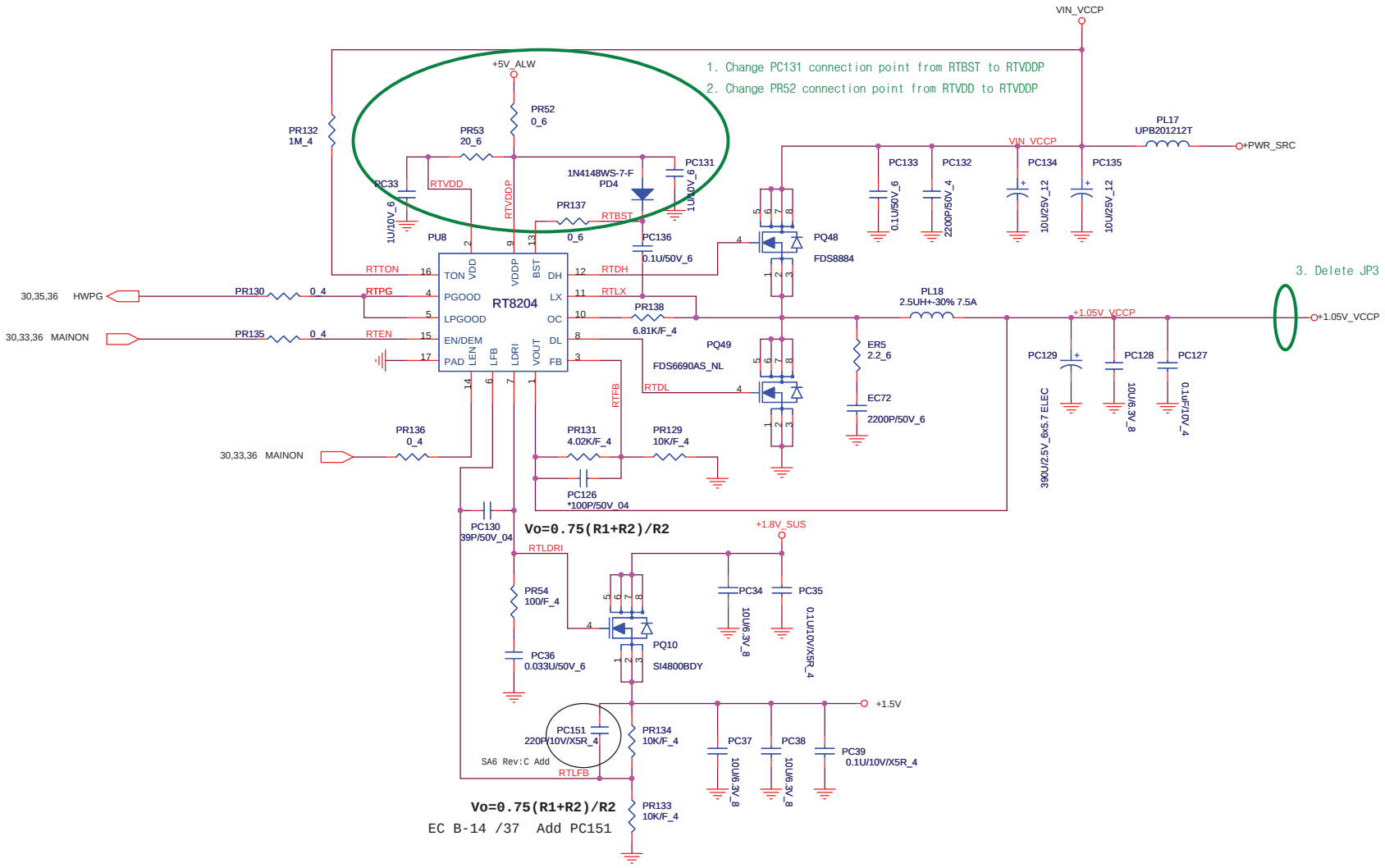

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.5v&1.05V	3B

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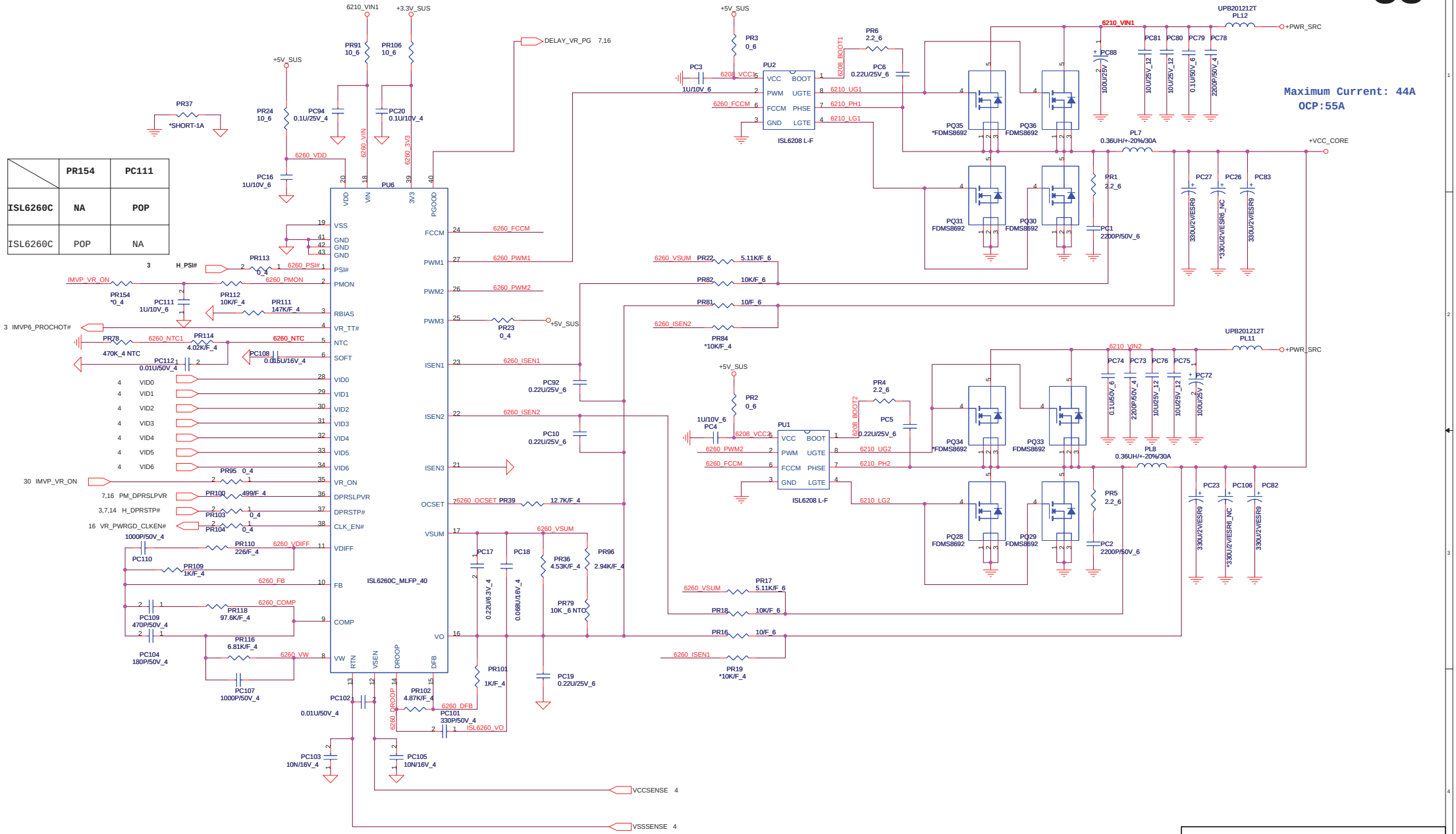
	PR154	PC111
ISL6260C	NA	POP
ISL6260C	POP	NA

Maximum Current: 44A
OCP:55A



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU_CORE POWER	3B

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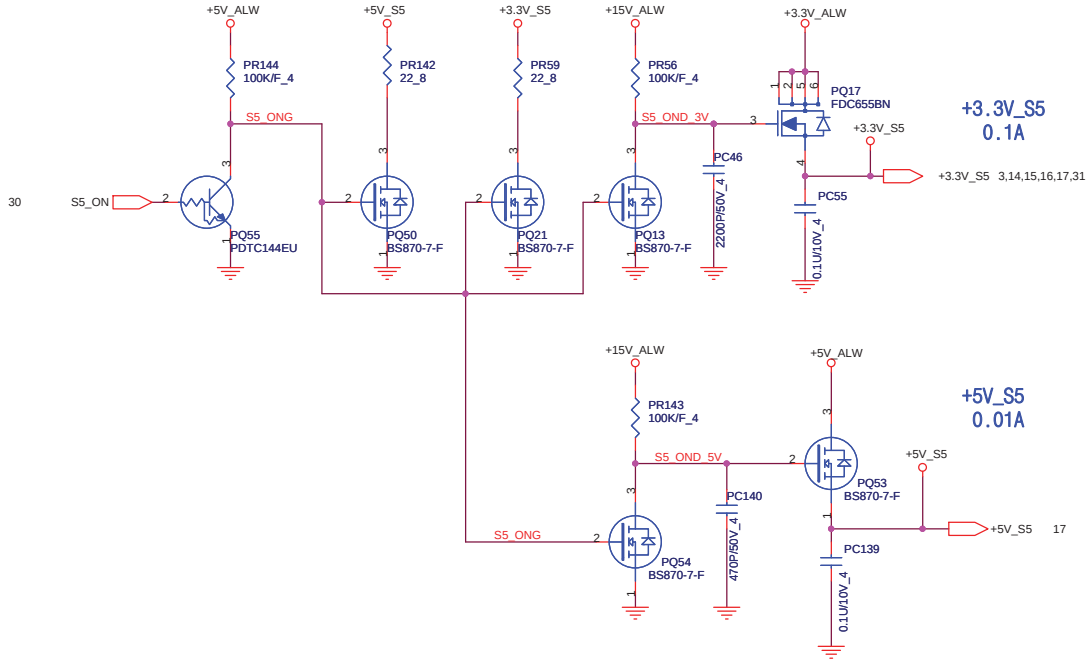

PROJECT : SA6

Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3v_5S5/+5V_S5	3B
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CPU SCREW HOLE

HOLE7 *h-ts315bs256d169p2
HOLE11 *h-ts315bs256d169p2
HOLE8 *h-ts315bs256d169p2
HOLE10 *h-ts315bs256d169p2

MINI PCI-E SCREW HOLE 2

HOLE26 H-C236D142P2
HOLE25 H-C236D142P2

MINI PCI-E SCREW HOLE 1

HOLE24 H-C236D142P2
HOLE27 H-C236D142P2

MDC SCREW HOLE

HOLE21 H-C236D142P2
HOLE20 H-TC236BS4D142P2

NB SCREW HOLE

HOLE22 H-C236D142P2
HOLE23 H-C236D142P2

HOLE1 *h-ts4bs8d110p2
HOLE2 *h-ts8bs8d110p2
HOLE9 *h-ts1-be354x354d110p2
HOLE5 *h-ts7bs8d110p2
HOLE13 *H-TS354BC280D110P2
HOLE3 *h-c118d118n
HOLE6 *H-C98D98N
HOLE18 *H-TS314BS1D110P2
HOLE19 *h-te433bs354d110p2
HOLE17 *H-TC276BC354D110P2
HOLE4 *h-ts5bs6d110p2
HOLE12 *h-tc276bs3d196p2
HOLE14 *h-ts2bs2d110p2
HOLE28 *H-C236D110P2
ADO_GND
HOLE16 *h-ts314bs354d119p2
HOLE15 *H-TC276TD110RB

EMI Use

+3.3V
EC62 EC6 EC49 EC2 EC3 0.1U/10V_4
EC68 EC74 EC64 EC60 0.1U/10V_4 SI Use
EC14 EC48 EC46 EC24 EC21 EC25 0.1U/10V_4
EC24 *0.1U/10V_4

+5V_SUS
EC50 EC16 EC12 EC10 EC58 EC52 EC30 EC61 EC47 EC51 EC1 EC56 EC57 EC29 0.1U/10V_4
EC61 *0.1U/10V_4
EC51 *0.1U/10V_4
EC57 *0.1U/10V_4

+1.05V_VCCP
EC18 EC19 0.1U/10V_4

+3.3V_ALW
EC13 EC38 EC77 EC9 EC17 EC41 EC7 EC5 *0.1U/10V_4

+1.05V_VCCP
EC71 EC73 EC75 EC76 EC82 EC80 EC83 EC81 EC84 EC85 EC87 0.1U/10V_4
EC80 100P/50V_6
EC81 EC85 EC87 100P/50V_6
Add EC80~83 for EMI in B-Stage

+1.5V

+15V_ALW
EC78 *0.1U/25V_4
EC23 *0.1U/25V_4
EC32 0.1U/25V_4
EC43 *0.1U/25V_4
EC31 *0.1U/25V_4
EC37 *0.1U/25V_4

+PWR_SRC
EC67 EC59 EC8 EC55 EC40 EC28 EC53 EC70 EC69 EC54 1000P/50V_4
EC79 EC11 EC20 EC65 EC22 EC15 EC66 0.1U/25V_4
Add in Btage For EMI use

+PWR_SRC
EC36 EC35 EC34 EC26 EC27 1000P/50V_4

PA1 *EMIPAD
PA2 *EMIPAD

ESD Use

+3.3V C563
+3.3V C564
+1.5V C565
+1.5V C566
+3.3V_SUS C615
+5V_SUS C616
Varistor_4

New Footprint.
C563 close to C489 C564 close to C495 C565 close to C241 C563 close to HOLE26
EC B-10 /40 Add C563,C563,C565,C566 fix ESD .
EC C-04 /40 Add C614~C617 for ESD Request.

+1.5V C618
+3.3V_ALW C617
Varistor_4

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Quanta Computer Inc.

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A-test to B-test EC list

EC A-01 /15 change to +3.3V_SUS for B test
EC A-02 /24 and 15 Change to 1.5V for HDA use.
EC A-03 /16 Add R499 Pull high to +3.3V_S5
EC A-04 /16 change R190 pull-high to +3.3V_S5
EC A-05 /02 Add EMI Request L52 C554.
EC A-06 /14 C462,C459,C466,C464 Change to 10nF in B Stage.
EC A-07 /15 Add R224 PCI_PME# Connect to +3.3V_S5
EC A-08 /20 change VGA Pin 9 Desgin in B Stage.
EC A-09 /21 Add C557,C558,C555 for EMI Request.
EC A-10 /24 Add C329,C328,C327,C326 for EMI Request.
EC A-11 /26 Add L49,L50,C533,C542 in B stage For EMI use
EC A-12 /31 Add CP7 CP8 C553 in B stage For EMI use
EC A-14 /31 for LED +3.3V leak electricity.
EC A-15 /24 change C525 to 1U Fix POP Noise.
EC A-16 /7 CLK_3GPLLREQ# pull-high Page2 have, So remove R80 CLK_3GPLLREQ# Pull High.
EC A-17 / 21 Use BIOS MAC address , remove R340,R339,U17 , Mount R338.
EC A-18 / 18 B Stage R282 to 100 ohm for conexant request.

B-test to C-test EC list

EC B-01 /02 chamge 22P to 30P for RTC issue.
EC B-02 /03 chamge to 10K for meet Intel spec.
EC B-03 /05 chamge to 0 ohm for meet ADI spec.
EC B-04 /09/10 NA 220U and 330U.
EC B-05 /24 change R491,R492 from 0 ohm to 6.8K C551,C543 to 1U and change AMP Gain to 10 db for meet SPK Spec 1.5W.

EC B-6 /24 Add C603,C604,C606,C607,C608,C609 for ESD Request.
EC B-7 /30 Add R507,C560,C561 for ITE8502JX use.
EC B-8 /15 mount R447 and C482 for EMI request.
EC B-9 /30 Add R508 and C562 for EMI request.
EC B-10 /40 Add C563,C564,C565,C566 fix ESD .
EC B-11 /34 change PC66 to ESD Diode fix ESD .
EC B-12 /15 Add U31 for HDCP support.
EC B-13 /36 Del PC123,Add PC152.
EC B-14 /37 Add PC151
EC B-15 /31 change R608 to 0805 and Q40 change to 2N7002.
EC B-16 /23 Remove Q11,Q12,R235,R159 change C250 to 0.1U for OZ126 Rev:B use.
EC B-17 /10 Del L38,L39 Add R510,R511 1206 0 ohm.
EC B-18 /29 Mount C71,C76 for ESD.
EC B-19 /07 change R88 from 1.02K to 1K meet Intel check list 1.1

C-test to FAI-test EC list

EC C-01 /17 chamge C476,C491 to 1U, R427,R470 to 100 ohm for USB 1.0 can't work and meeti Intel Spec.
EC C-02 /17 mount C227 0.1U
EC C-03 /26 Add R514,R515,R516 connect to CL Function
EC C-04 /40 Add C614~C617 for ESD Request.
EC C-05 /30 Remove C561 for ITE Bug.
EC C-06 /27 change C479,C481,C415,C429 to 0.01U for meet Intel Spc.
EC C-07 /19 Add R517 Pin 25 connect to GND, ST Add R320,R319.
EC C-08/14 Add for TMP in FAI
EC C-09/14 Add R424 10K to meet Intel Demo Board.
EC C-10/03 Change C229 to 10P and R171 to 22 ohm for meet Clock test.
EC C-11/26 Change R455 to R466 connector +3V, Add R513 connector +3V for Intel Wireless use.