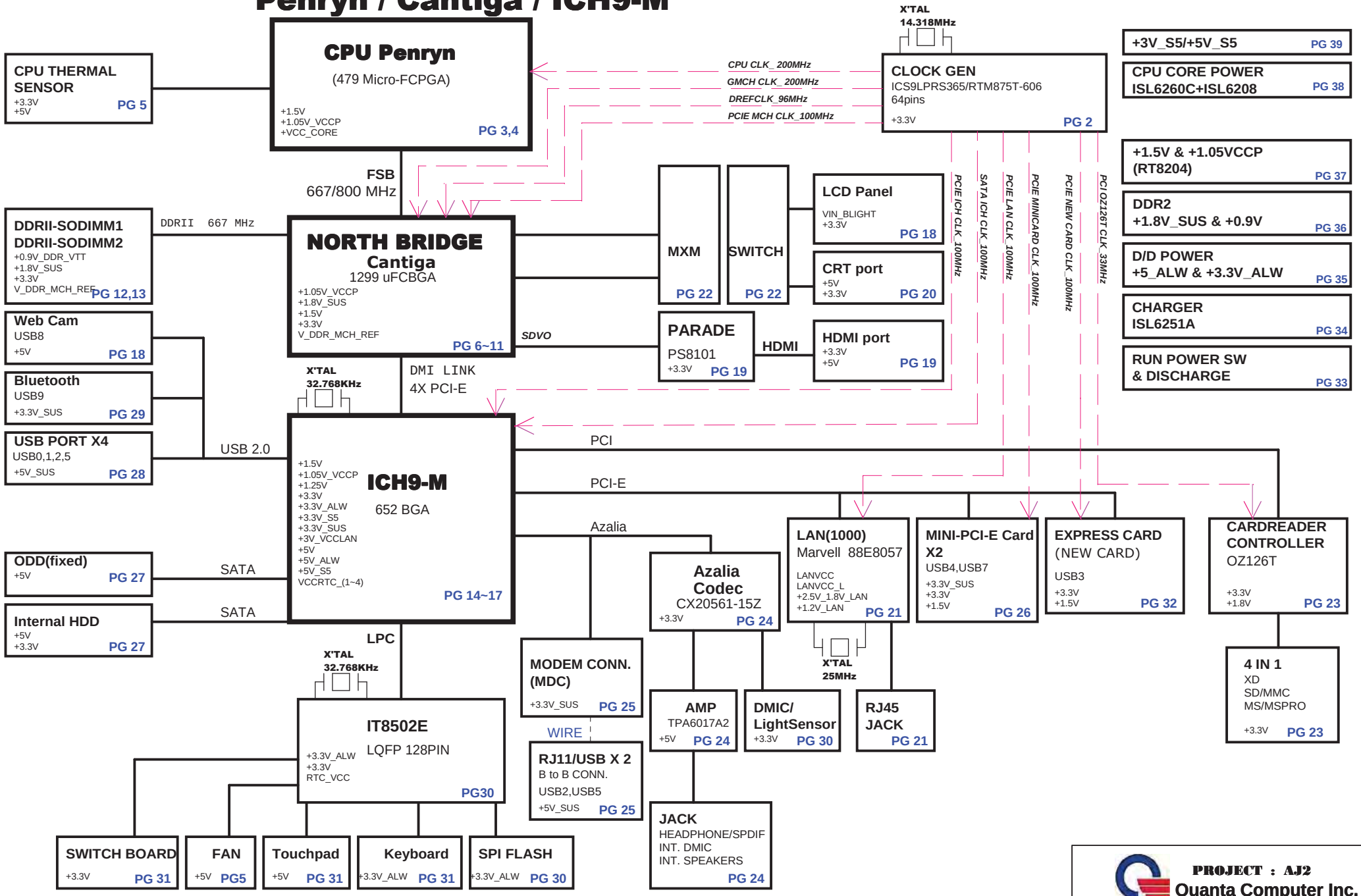
AJ2 BLOCK DIAGRAM

(Montevina Platform)

Penryn / Cantiga / ICH9-M



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	1A

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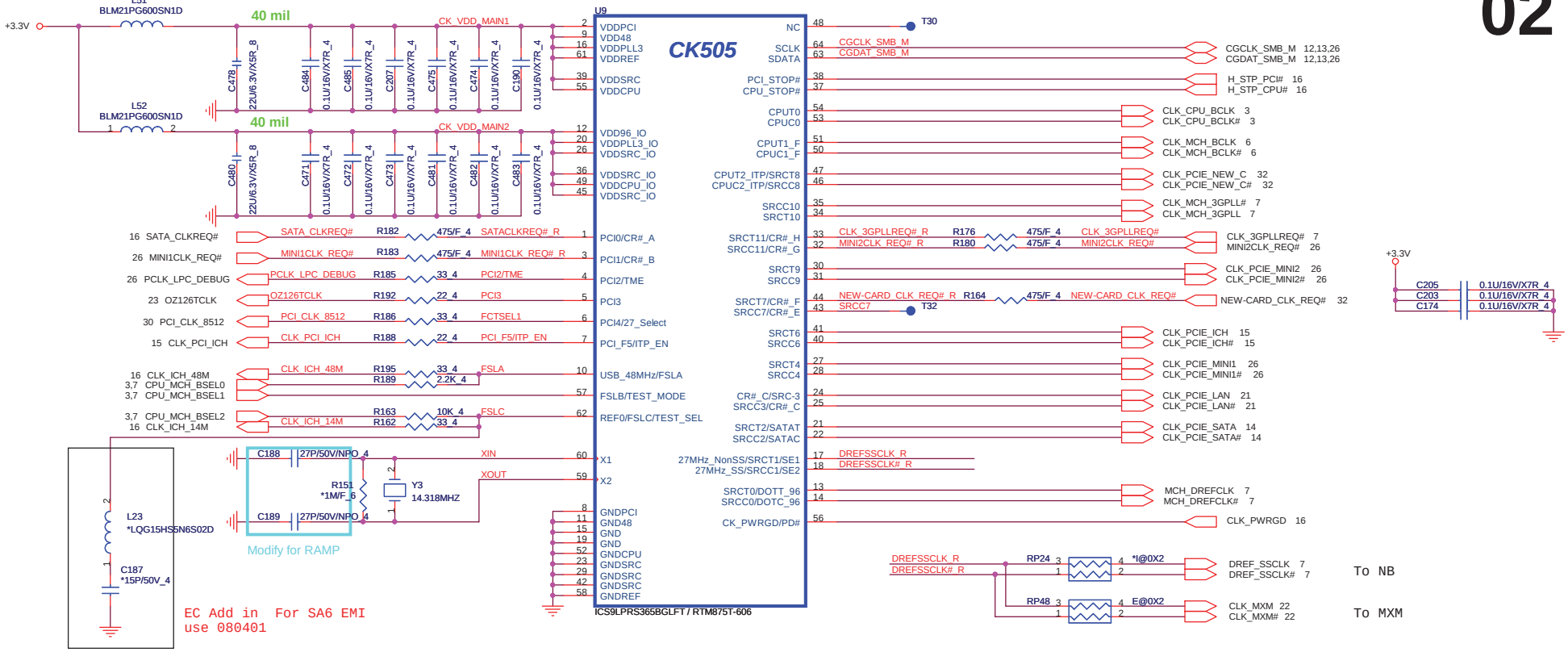
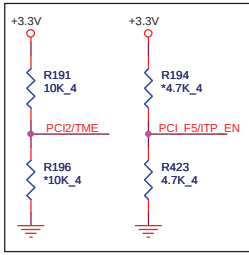
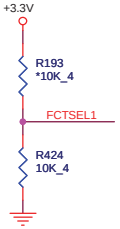


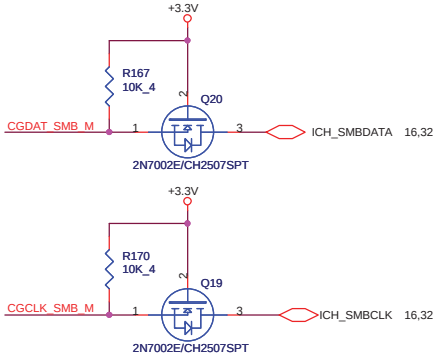


	PULL HIGH	PULL LOW
PCI_F5/ITP_EN	ITP/ITP#	SRC8/SRC8#
PCI2/TME	Overclocking of CPU and SRC not allowed	Overclocking of CPU and SRC allowed

GCLK_SEL = FCTSEL1

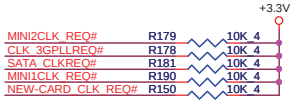
FCTSEL1 (PIN6)	PIN13	PIN14	PIN17	PIN18
0=UMA	DOT96	DOT96#	SRC-1/LCDT_100	SRC-1#/LCDT_100
1 = External VGA	SRC-0	SRC-0#	27Mout-NSS	27Mout-SS

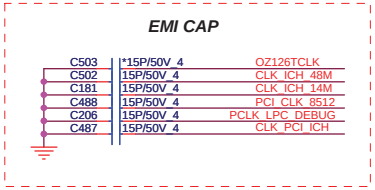


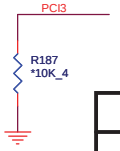


CPU Clock select

FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100.00	100	33
0	0	1	133.33	100	33
0	1	1	166.66	100	33
0	1	0	200.00	100	33
0	0	0	266.66	100	33
1	0	0	333.33	100	33
1	1	0	400.00	100	33
1	1	1	200.00	100	33







	PULL HIGH	PULL LOW
PCI3	PIN37/38 is CPU_STOP/PCI_STOP PIN37/38 IS SRC5.	**SRC5_EN/PCI-3 (Internal Pull Low)

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	1A
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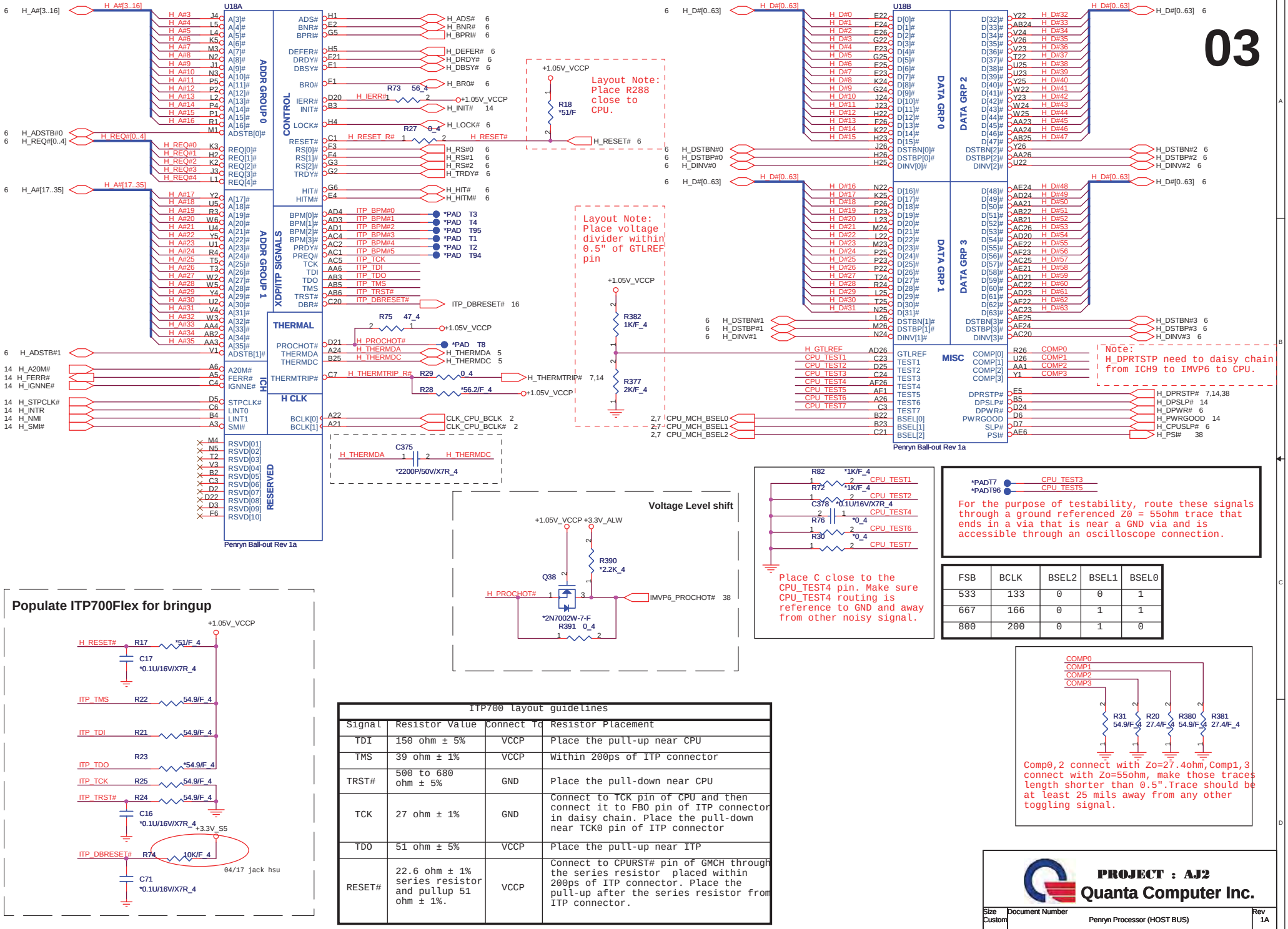

FSB	BCLK	BSEL2	BSEL1	BSEL0
533	133	0	0	1
667	166	0	1	1
800	200	0	1	0

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 680 ohm ± 5%	GND	Place the pull-down near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to FBO pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near ITP
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn Processor (HOST BUS)	1A
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All use 22U 10V(+-20%,X5R,1210)Pb-Free.

+VCC_CORE

C350 10U/4V/X6S_8 C353 10U/4V/X6S_8 C50 10U/4V/X6S_8 C345 10U/4V/X6S_8 C341 10U/4V/X6S_8

+VCC_CORE

C337 10U/4V/X6S_8 C344 10U/4V/X6S_8 C339 10U/4V/X6S_8 C349 10U/4V/X6S_8 C59 10U/4V/X6S_8

8 inside cavity, north side, secondary layer.

+VCC_CORE

C340 10U/4V/X6S_8 C33 10U/4V/X6S_8 C45 10U/4V/X6S_8 C38 10U/4V/X6S_8 C354 10U/4V/X6S_8

+VCC_CORE

C36 10U/4V/X6S_8 C51 10U/4V/X6S_8 C58 10U/4V/X6S_8 C44 10U/4V/X6S_8 C348 10U/4V/X6S_8

8 inside cavity, south side, secondary layer.

+VCC_CORE

C29 10U/4V/X6S_8 C57 10U/4V/X6S_8 C26 10U/4V/X6S_8 C27 10U/4V/X6S_8 C60 10U/4V/X6S_8 C31 10U/4V/X6S_8

6 inside cavity, north side, primary layer.

+VCC_CORE

C28 10U/4V/X6S_8 C30 10U/4V/X6S_8 C32 10U/4V/X6S_8 C35 10U/4V/X6S_8 C351 10U/4V/X6S_8 C37 10U/4V/X6S_8

6 inside cavity, south side, primary layer.

+1.05V_VCCP

C336 0.1U/16V/X7R_4 C338 0.1U/16V/X7R_4 C355 0.1U/16V/X7R_4 C335 0.1U/16V/X7R_4 C357 0.1U/16V/X7R_4 C356 0.1U/16V/X7R_4

Layout out:
Place these inside socket cavity on North side secondary.

+PWR_SRC

C314 *100U/25V

Layout Note:
Need to add 100uF cap on PWR_SRC for cap singing.
Place on PWR_SRC near +VCC_CORE.

+VCC_CORE +VCC_CORE

U18C

A7	VCC[001]	VCC[068]	AB20
A9	VCC[002]	VCC[069]	AB7
A10	VCC[003]	VCC[070]	AC7
A12	VCC[004]	VCC[071]	AC9
A13	VCC[005]	VCC[072]	AC12
A15	VCC[006]	VCC[073]	AC13
A17	VCC[007]	VCC[074]	AC15
A18	VCC[008]	VCC[075]	AC17
A20	VCC[009]	VCC[076]	AC18
B7	VCC[010]	VCC[077]	AD7
B9	VCC[011]	VCC[078]	AD9
B10	VCC[012]	VCC[079]	AD10
B12	VCC[013]	VCC[080]	AD12
B14	VCC[014]	VCC[081]	AD14
B15	VCC[015]	VCC[082]	AD15
B17	VCC[016]	VCC[083]	AD17
B18	VCC[017]	VCC[084]	AD18
B20	VCC[018]	VCC[085]	AE9
C9	VCC[019]	VCC[086]	AE10
C10	VCC[020]	VCC[087]	AE12
C12	VCC[021]	VCC[088]	AE13
C13	VCC[022]	VCC[089]	AE15
C15	VCC[023]	VCC[090]	AE17
C17	VCC[024]	VCC[091]	AE18
C18	VCC[025]	VCC[092]	AE20
D9	VCC[026]	VCC[093]	AF9
D10	VCC[027]	VCC[094]	AF10
D12	VCC[028]	VCC[095]	AF12
D14	VCC[029]	VCC[096]	AF14
D15	VCC[030]	VCC[097]	AF15
D17	VCC[031]	VCC[098]	AF17
D18	VCC[032]	VCC[099]	AF18
E7	VCC[033]	VCC[100]	AF20
E9	VCC[034]		
E10	VCC[035]	VCCP[01]	G21
E12	VCC[036]	VCCP[02]	V6
E13	VCC[037]	VCCP[03]	J6
E15	VCC[038]	VCCP[04]	K6
E17	VCC[039]	VCCP[05]	M6
E18	VCC[040]	VCCP[06]	J21
E20	VCC[041]	VCCP[07]	K21
F7	VCC[042]	VCCP[08]	M21
F9	VCC[043]	VCCP[09]	N21
F10	VCC[044]	VCCP[10]	N6
F12	VCC[045]	VCCP[11]	R21
F14	VCC[046]	VCCP[12]	R6
F15	VCC[047]	VCCP[13]	T21
F17	VCC[048]	VCCP[14]	T6
F18	VCC[049]	VCCP[15]	V21
F20	VCC[050]	VCCP[16]	W21
AA7	VCC[051]		
AA9	VCC[052]	VCCA[01]	B26
AA10	VCC[053]	VCCA[02]	C26
AA12	VCC[054]		
AA13	VCC[055]	VID[0]	AD6
AA15	VCC[056]	VID[1]	AE5
AA17	VCC[057]	VID[2]	AE5
AA18	VCC[058]	VID[3]	AF4
AA20	VCC[059]	VID[4]	AE3
AB9	VCC[060]	VID[5]	AF3
AC10	VCC[061]	VID[6]	AE2
AB10	VCC[062]		
AB12	VCC[063]		
AB14	VCC[064]	VCCSENSE	AF7
AB15	VCC[065]		
AB17	VCC[066]		
AB18	VCC[067]	VSSSENSE	AF7

Penryn Ball-out Rev 1a

+1.05V_VCCP

C346 330U/2.5V_7343

VID0 38
VID1 38
VID2 38
VID3 38
VID4 38
VID5 38
VID6 38

VCCSENSE VCCSENSE 38

VSSSENSE VSSSENSE 38

+1.5V

C72 0.01U/25V/X7R_4 C73 10U/4V/X6S_8

Layout Note:
Place C424 near PIN B26.

+VCC_CORE

R350 100/F_4

VCCSENSE
VSSSENSE

R347 100/F_4

Route VCCSENSE and VSSSENSE traces at 27.4ohms and length matched to within 25 mil. Place PU and PD within 2 inch of CPU.

U18D

A4	VSS[001]	VSS[082]	P6
A8	VSS[002]	VSS[083]	P21
A11	VSS[003]	VSS[084]	P24
A14	VSS[004]	VSS[085]	R2
A16	VSS[005]	VSS[086]	R5
A19	VSS[006]	VSS[087]	R22
A23	VSS[007]	VSS[088]	R25
AE2	VSS[008]	VSS[089]	T1
B6	VSS[009]	VSS[090]	T4
B8	VSS[010]	VSS[091]	T23
B11	VSS[011]	VSS[092]	T26
B13	VSS[012]	VSS[093]	U3
B16	VSS[013]	VSS[094]	U6
B19	VSS[014]	VSS[095]	U21
B21	VSS[015]	VSS[096]	U24
B24	VSS[016]	VSS[097]	V2
C5	VSS[017]	VSS[098]	V5
C8	VSS[018]	VSS[099]	V22
C11	VSS[019]	VSS[100]	V25
C14	VSS[020]	VSS[101]	W1
C16	VSS[021]	VSS[102]	W4
C19	VSS[022]	VSS[103]	W23
C2	VSS[023]	VSS[104]	W26
C22	VSS[024]	VSS[105]	Y3
C25	VSS[025]	VSS[106]	Y6
D1	VSS[026]	VSS[107]	Y21
D4	VSS[027]	VSS[108]	Y24
D8	VSS[028]	VSS[109]	AA2
D11	VSS[029]	VSS[110]	AA5
D13	VSS[030]	VSS[111]	AA8
D16	VSS[031]	VSS[112]	AA11
D19	VSS[032]	VSS[113]	AA14
D23	VSS[033]	VSS[114]	AA16
D26	VSS[034]	VSS[115]	AA19
E3	VSS[035]	VSS[116]	AA22
E6	VSS[036]	VSS[117]	AA25
E8	VSS[037]	VSS[118]	AB1
E11	VSS[038]	VSS[119]	AB4
E14	VSS[039]	VSS[120]	AB8
E16	VSS[040]	VSS[121]	AB11
E19	VSS[041]	VSS[122]	AB13
E21	VSS[042]	VSS[123]	AB16
E24	VSS[043]	VSS[124]	AB19
F5	VSS[044]	VSS[125]	AB23
F8	VSS[045]	VSS[126]	AB26
F11	VSS[046]	VSS[127]	AC3
F13	VSS[047]	VSS[128]	AC6
F16	VSS[048]	VSS[129]	AC8
F19	VSS[049]	VSS[130]	AC11
F2	VSS[050]	VSS[131]	AC14
F22	VSS[051]	VSS[132]	AC16
F25	VSS[052]	VSS[133]	AC19
G4	VSS[053]	VSS[134]	AC21
G1	VSS[054]	VSS[135]	AC24
G23	VSS[055]	VSS[136]	AD2
G26	VSS[056]	VSS[137]	AD5
H3	VSS[057]	VSS[138]	AD8
H6	VSS[058]	VSS[139]	AD11
H21	VSS[059]	VSS[140]	AD13
H24	VSS[060]	VSS[141]	AD16
J2	VSS[061]	VSS[142]	AD19
J5	VSS[062]	VSS[143]	AD22
J22	VSS[063]	VSS[144]	AD25
J25	VSS[064]	VSS[145]	AE1
K1	VSS[065]	VSS[146]	AE4
K4	VSS[066]	VSS[147]	AE8
K23	VSS[067]	VSS[148]	AE11
K26	VSS[068]	VSS[149]	AE14
L3	VSS[069]	VSS[150]	AE16
L6	VSS[070]	VSS[151]	AE19
L21	VSS[071]	VSS[152]	AE23
L24	VSS[072]	VSS[153]	AE26
M2	VSS[073]	VSS[154]	A2
M5	VSS[074]	VSS[155]	AF6
M22	VSS[075]	VSS[156]	AF8
M25	VSS[076]	VSS[157]	AF11
N1	VSS[077]	VSS[158]	AF13
N4	VSS[078]	VSS[159]	AF16
N23	VSS[079]	VSS[160]	AF19
N26	VSS[080]	VSS[161]	AF21
P3	VSS[081]	VSS[162]	A25
		VSS[163]	AF25

Penryn Ball-out Rev 1a

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Penryn Processor (POWER)	1A
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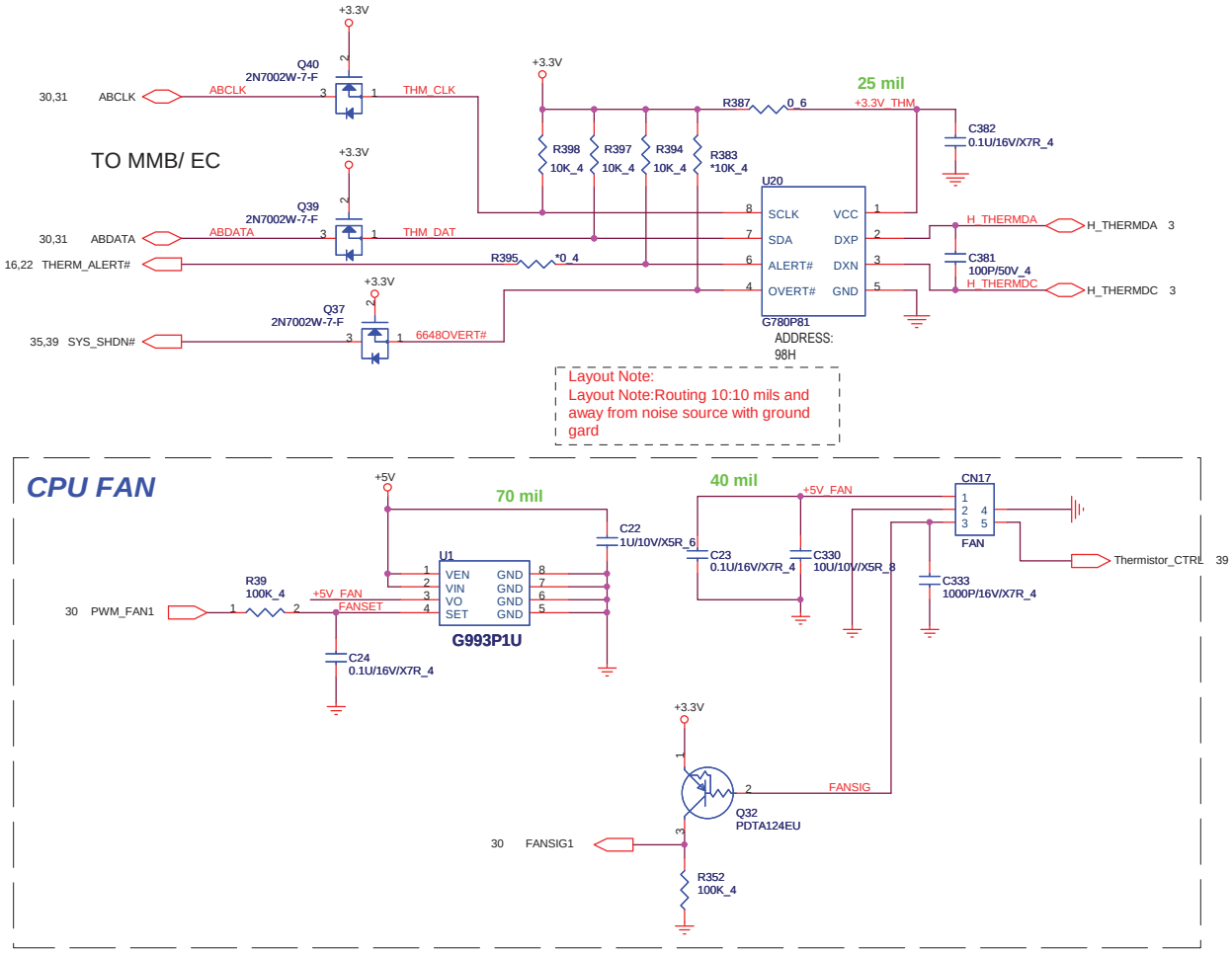
CPU Thermal monitor



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Thermal IC	1A
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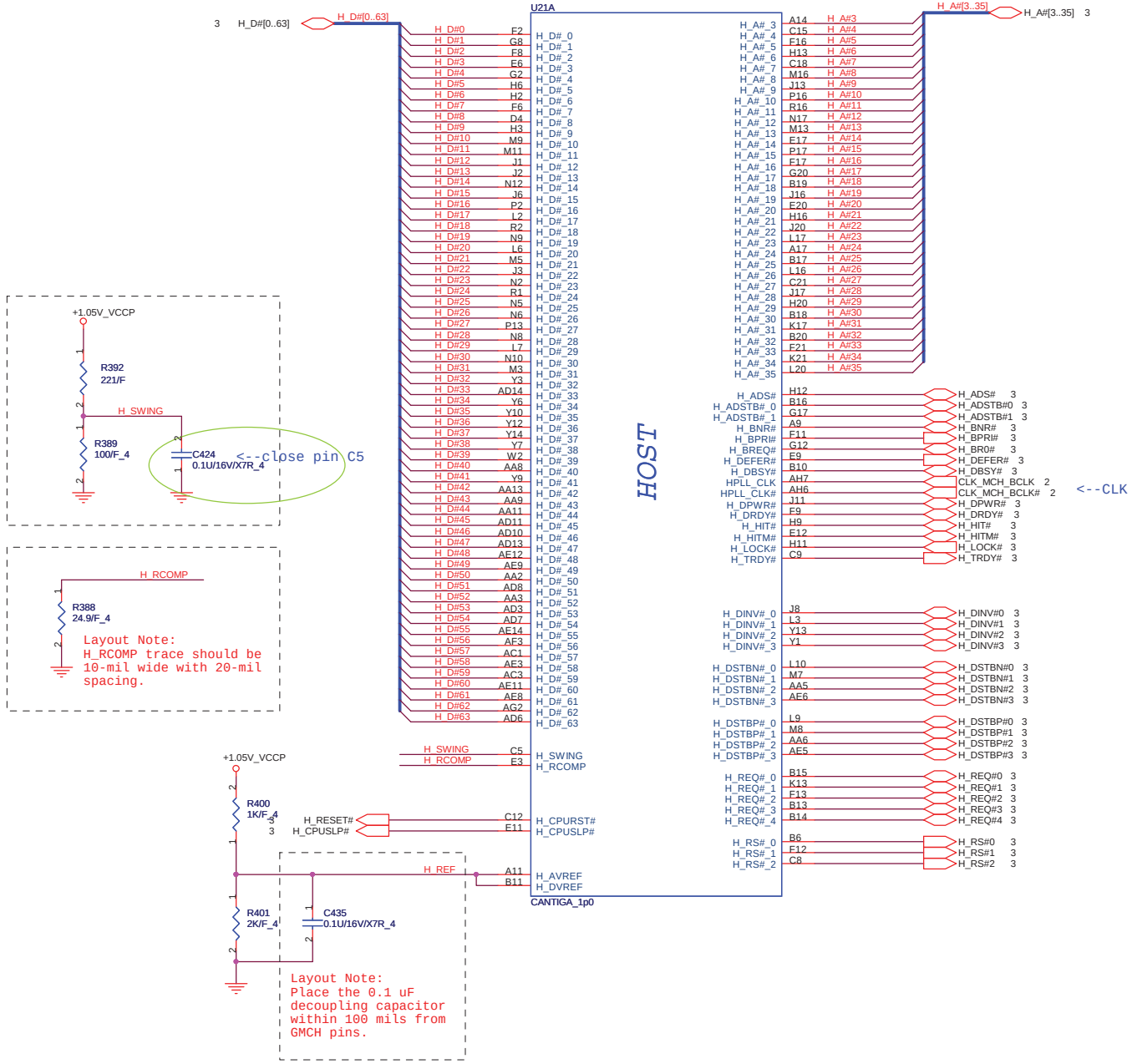

PROJECT : AJ2		
Quanta Computer Inc.		
Size: Custom	Document Number: Cantiga (HOST)	Rev: 1A
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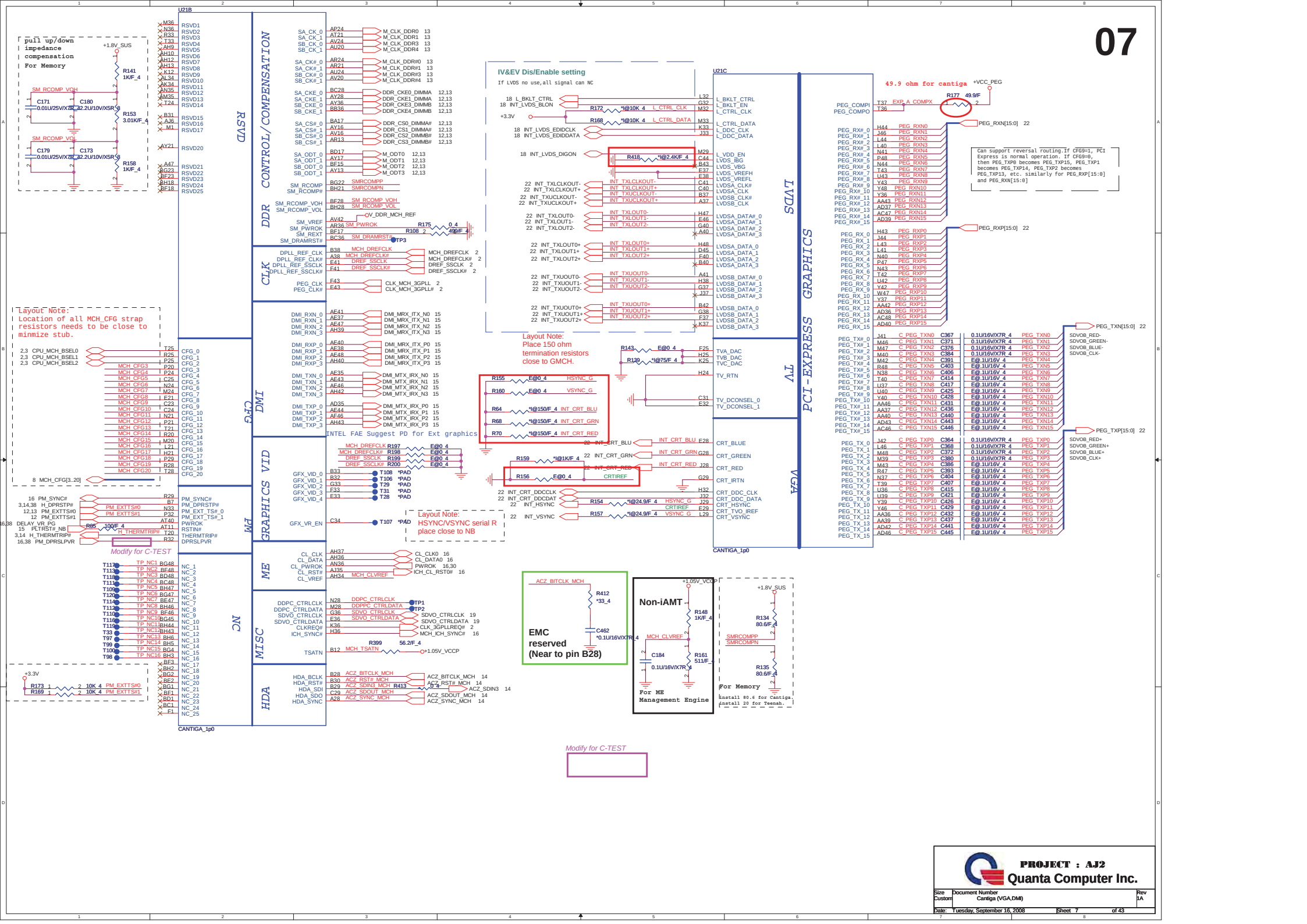

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (VGA,DMI)	1A

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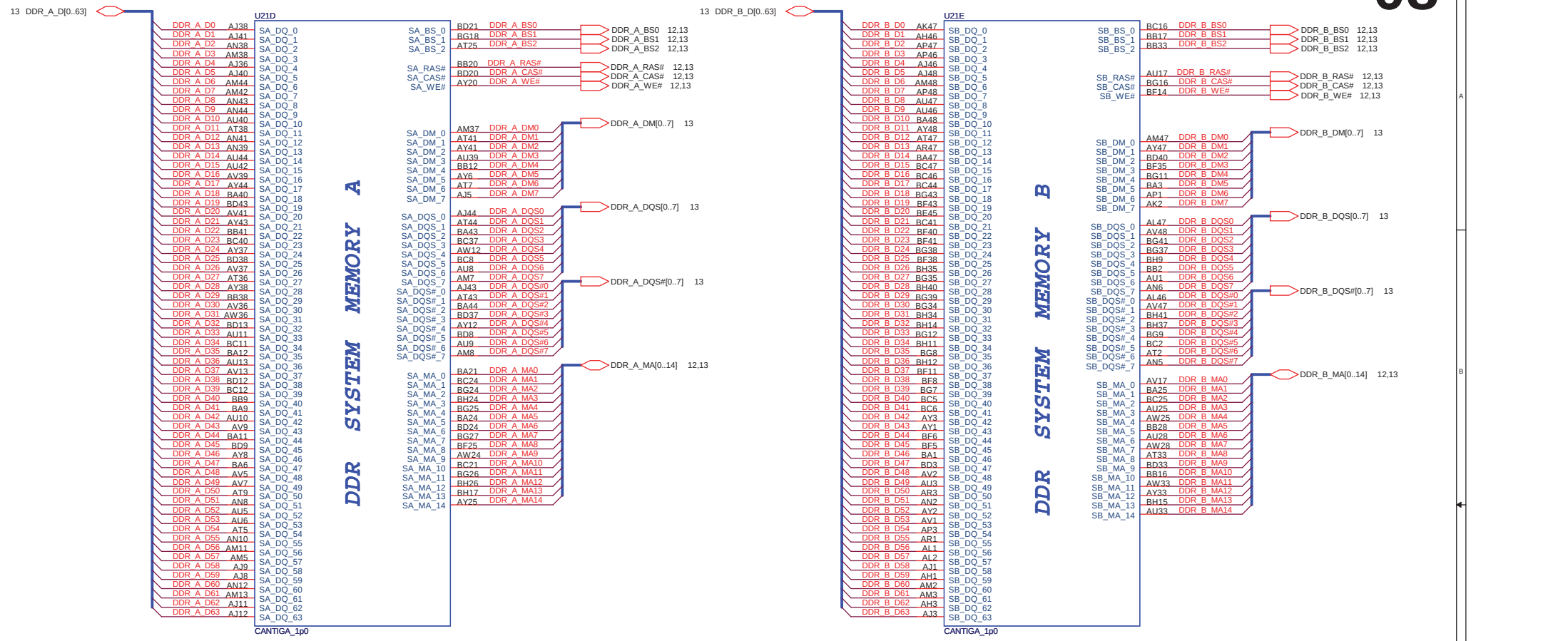
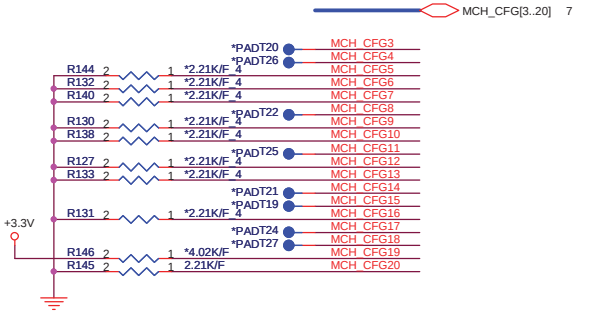
DDR2



STRAPPING

CFG5	DMI X2 Select	Low=DMIx2 High=DMIx4(Default)
CFG6	iTPM Host Interface	Low= Enable High=Disable(Default)
CFG7	Intel Management Engine Crypto Strap	Low= Intel Management Engine Crypto TLS cipher suite with no Confidentiality High=Intel Management Engine Crypto TLS cipher suite with Confidentiality(Default)
CFG9	PCI Express Graphic Lane	Low= Reveise Lane High=Normal operation
CFG10	PCIe Loopback Enable	Low= Enable High=Disable(Default)
CFG16	FSB Dynamic ODT	Low=Dynamic ODT Disable High=Dynamic ODT Enable(default).
CFG19	DMI Lane Reversal	Low=Normal(default). High=Lane Reversed
CFG20	Digital Display Port(SDVO/DP/iHDMI) and PCIe Concurrent Operation.	Low=Only DP or inly PCIe is operational (defaults) High=DP and PCIe x1 are operating simultaneously.
CFG13 / CFG12	XOR / ALLZ / Clock Un-gating	00=Reserved. 10=XOR Mode Enabled. 01=All-Z Mode Enabled. 11=Normal Operation (Default).



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (DDR2,STRAPPING)	1A
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U21G

+1.8V_SUS

AP33 VCC_SM_1
AN33 VCC_SM_2
BH32 VCC_SM_3
BG32 VCC_SM_4
BF32 VCC_SM_5
BD32 VCC_SM_6
BC32 VCC_SM_7
BB32 VCC_SM_8
BA32 VCC_SM_9
AY32 VCC_SM_10
AW32 VCC_SM_11
AV32 VCC_SM_12
AU32 VCC_SM_13
AT32 VCC_SM_14
AR32 VCC_SM_15
AP32 VCC_SM_16
AN32 VCC_SM_17
BH31 VCC_SM_18
BG31 VCC_SM_19
BF31 VCC_SM_20
BG30 VCC_SM_21
BH29 VCC_SM_22
BG29 VCC_SM_23
BF29 VCC_SM_24
BD29 VCC_SM_25
BC29 VCC_SM_26
BB29 VCC_SM_27
BA29 VCC_SM_28
AY29 VCC_SM_29
AW29 VCC_SM_30
AV29 VCC_SM_31
AU29 VCC_SM_32
AT29 VCC_SM_33
AR29 VCC_SM_34
AP29 VCC_SM_35

VCC SM

BA36 VCC_SM_36/NC
BB24 VCC_SM_37/NC
BD16 VCC_SM_38/NC
BB21 VCC_SM_39/NC
AW16 VCC_SM_40/NC
AW13 VCC_SM_41/NC
AT13 VCC_SM_42/NC

POWER

+1.05V_AXG

Y26 VCC_AXG_1
AE25 VCC_AXG_2
AB25 VCC_AXG_3
AA25 VCC_AXG_4
AE24 VCC_AXG_5
AC24 VCC_AXG_6
AA24 VCC_AXG_7
Y24 VCC_AXG_8
AE23 VCC_AXG_9
AC23 VCC_AXG_10
AB23 VCC_AXG_11
AA23 VCC_AXG_12
AJ21 VCC_AXG_13
AG21 VCC_AXG_14
AE21 VCC_AXG_15
AC21 VCC_AXG_16
AA21 VCC_AXG_17
Y21 VCC_AXG_18
AH20 VCC_AXG_19
AF20 VCC_AXG_20
AE20 VCC_AXG_21
AC20 VCC_AXG_22
AB20 VCC_AXG_23
AA20 VCC_AXG_24
T17 VCC_AXG_25
T16 VCC_AXG_26
AM15 VCC_AXG_27
AL15 VCC_AXG_28
AE15 VCC_AXG_29
AJ15 VCC_AXG_30
AH15 VCC_AXG_31
AG15 VCC_AXG_32
AF15 VCC_AXG_33
AB15 VCC_AXG_34
AA15 VCC_AXG_35
Y15 VCC_AXG_36
V15 VCC_AXG_37
U15 VCC_AXG_38
AN14 VCC_AXG_39
AM14 VCC_AXG_40
U14 VCC_AXG_41
T14 VCC_AXG_42

VCC GFX

AJ14 VCC_AXG_SENSE
AH14 VSS_AXG_SENSE

+1.05V_AXG

VCC_AXG_NCTF_1 W28
VCC_AXG_NCTF_2 V28
VCC_AXG_NCTF_3 W26
VCC_AXG_NCTF_4 V26
VCC_AXG_NCTF_5 W25
VCC_AXG_NCTF_6 V25
VCC_AXG_NCTF_7 W24
VCC_AXG_NCTF_8 V24
VCC_AXG_NCTF_9 W23
VCC_AXG_NCTF_10 V23
VCC_AXG_NCTF_11 AM21
VCC_AXG_NCTF_12 AL21
VCC_AXG_NCTF_13 AK21
VCC_AXG_NCTF_14 W21
VCC_AXG_NCTF_15 V21
VCC_AXG_NCTF_16 U21
VCC_AXG_NCTF_17 AM20
VCC_AXG_NCTF_18 AK20
VCC_AXG_NCTF_19 W20
VCC_AXG_NCTF_20 U20
VCC_AXG_NCTF_21 AM19
VCC_AXG_NCTF_22 AL19
VCC_AXG_NCTF_23 AK19
VCC_AXG_NCTF_24 AJ19
VCC_AXG_NCTF_25 AH19
VCC_AXG_NCTF_26 AG19
VCC_AXG_NCTF_27 AF19
VCC_AXG_NCTF_28 AE19
VCC_AXG_NCTF_29 AB19
VCC_AXG_NCTF_30 AA19
VCC_AXG_NCTF_31 Y19
VCC_AXG_NCTF_32 W19
VCC_AXG_NCTF_33 V19
VCC_AXG_NCTF_34 U19
VCC_AXG_NCTF_35 AM17
VCC_AXG_NCTF_36 AK17
VCC_AXG_NCTF_37 AH17
VCC_AXG_NCTF_38 AG17
VCC_AXG_NCTF_39 AF17
VCC_AXG_NCTF_40 AE17
VCC_AXG_NCTF_41 AC17
VCC_AXG_NCTF_42 AB17
VCC_AXG_NCTF_43 Y17
VCC_AXG_NCTF_44 W17
VCC_AXG_NCTF_45 V17
VCC_AXG_NCTF_46 AM16
VCC_AXG_NCTF_47 AL16
VCC_AXG_NCTF_48 AK16
VCC_AXG_NCTF_49 AJ16
VCC_AXG_NCTF_50 AH16
VCC_AXG_NCTF_51 AG16
VCC_AXG_NCTF_52 AF16
VCC_AXG_NCTF_53 AE16
VCC_AXG_NCTF_54 AC16
VCC_AXG_NCTF_55 AB16
VCC_AXG_NCTF_56 AA16
VCC_AXG_NCTF_57 Y16
VCC_AXG_NCTF_58 W16
VCC_AXG_NCTF_59 V16
VCC_AXG_NCTF_60 U16

VCC GFX NCTF

CANTIGA_1p0

VCC SM LF

VCC_SM_LF1 AV44 VCCSM_LF1
VCC_SM_LF2 BA37 VCCSM_LF2
VCC_SM_LF3 AM40 VCCSM_LF3
VCC_SM_LF4 AV21 VCCSM_LF4
VCC_SM_LF5 AY5 VCCSM_LF5
VCC_SM_LF6 AM10 VCCSM_LF6
VCC_SM_LF7 BB13 VCCSM_LF7

C130 0.1U/16V/X7R_4
C123 0.1U/16V/X7R_4
C104 0.22U/10V
C157 0.22U/10V
C201 0.47U/10V
C197 1U/10V/X5R_6
C202 1U/10V/X5R_6

+1.05V_VCCP

C77 330U/2.5V_7343
C192 22U/4V_8
C178 0.22U/10V
C191 0.22U/10V
C195 0.1U/16V/X7R_4

Layout Note:
Place close to GMCH.

Layout Note:
Inside GMCH cavity.

U21F

AG34 VCC_1
AC34 VCC_2
AB34 VCC_3
AA34 VCC_4
Y34 VCC_5
V34 VCC_6
U34 VCC_7
AM33 VCC_8
AK33 VCC_9
AJ33 VCC_10
AG33 VCC_11
AF33 VCC_12
AE33 VCC_13
AC33 VCC_14
AA33 VCC_15
Y33 VCC_16
W33 VCC_17
V33 VCC_18
U33 VCC_19
AH28 VCC_20
AF28 VCC_21
AC28 VCC_22
AA28 VCC_23
AJ26 VCC_24
AG26 VCC_25
AE26 VCC_26
AC26 VCC_27
AH25 VCC_28
AG25 VCC_29
AF25 VCC_30
AG24 VCC_31
AJ23 VCC_32
AH23 VCC_33
AF23 VCC_34
VCC_35

VCC CORE

R152 0_4 1 2 T32

+1.05V_VCCP

R87 *I@0_8
R88 *I@0_8
E@0_6 E@0_6
R91 R93

+1.05V_AXG

Cavity Capacitors

C75 *I@330U/2.5V_7343
C76 *I@330U/2.5V_7343
C152 *I@0.47U/10V
C139 *I@1U/10V/X5R_6
C156 *I@10U/6.3V/X5R_6
C165 *I@22U/4V_8
C145 *I@0.1U/16V/X7R_4
C167 *I@0.1U/16V/X7R_4

Place close to the MCH

+1.8V_SUS

R174 0.002/F

C196 0.1U/16V/X7R_4
C198 330U/6.3V

Layout Note:
Place C411 where LVDS
and DDR2 taps.

VCC_SM

C186 22U/4V_8
C185 22U/4V_8

Layout Note:
Place on the edge.

+1.05V_VCCP

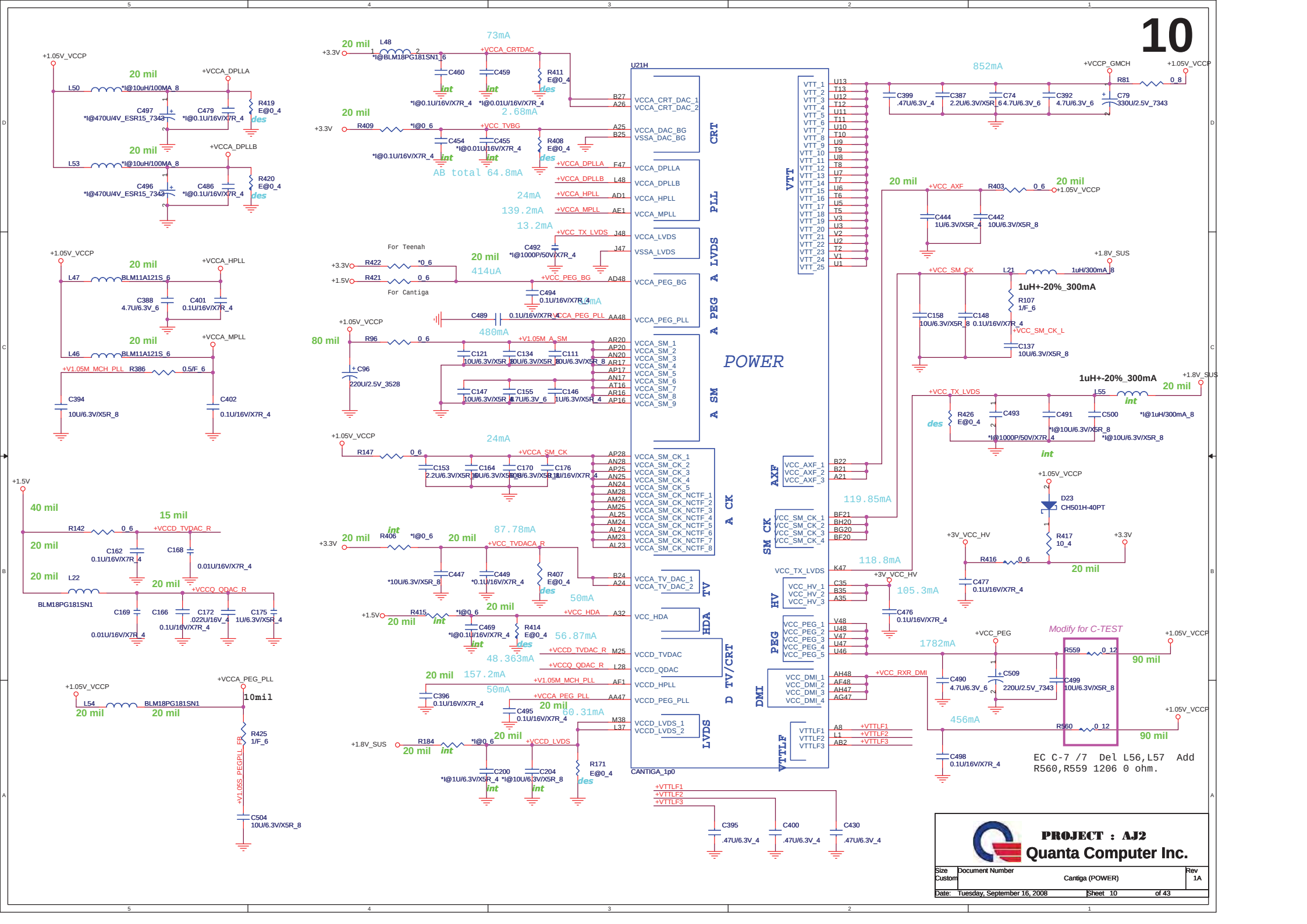
VCC_NCTF_1 AM32
VCC_NCTF_2 AL32
VCC_NCTF_3 AK32
VCC_NCTF_4 AJ32
VCC_NCTF_5 AH32
VCC_NCTF_6 AG32
VCC_NCTF_7 AE32
VCC_NCTF_8 AC32
VCC_NCTF_9 AA32
VCC_NCTF_10 Y32
VCC_NCTF_11 W32
VCC_NCTF_12 U32
VCC_NCTF_13 AM30
VCC_NCTF_14 AL30
VCC_NCTF_15 AK30
VCC_NCTF_16 AH30
VCC_NCTF_17 AG30
VCC_NCTF_18 AF30
VCC_NCTF_19 AE30
VCC_NCTF_20 AC30
VCC_NCTF_21 AB30
VCC_NCTF_22 AA30
VCC_NCTF_23 Y30
VCC_NCTF_24 W30
VCC_NCTF_25 V30
VCC_NCTF_26 U30
VCC_NCTF_27 AL29
VCC_NCTF_28 AK29
VCC_NCTF_29 AJ29
VCC_NCTF_30 AH29
VCC_NCTF_31 AG29
VCC_NCTF_32 AE29
VCC_NCTF_33 AC29
VCC_NCTF_34 AA29
VCC_NCTF_35 Y29
VCC_NCTF_36 W29
VCC_NCTF_37 V29
VCC_NCTF_38 AL28
VCC_NCTF_39 AK28
VCC_NCTF_40 AL26
VCC_NCTF_41 AK26
VCC_NCTF_42 AK25
VCC_NCTF_43 AK24
VCC_NCTF_44 AK23

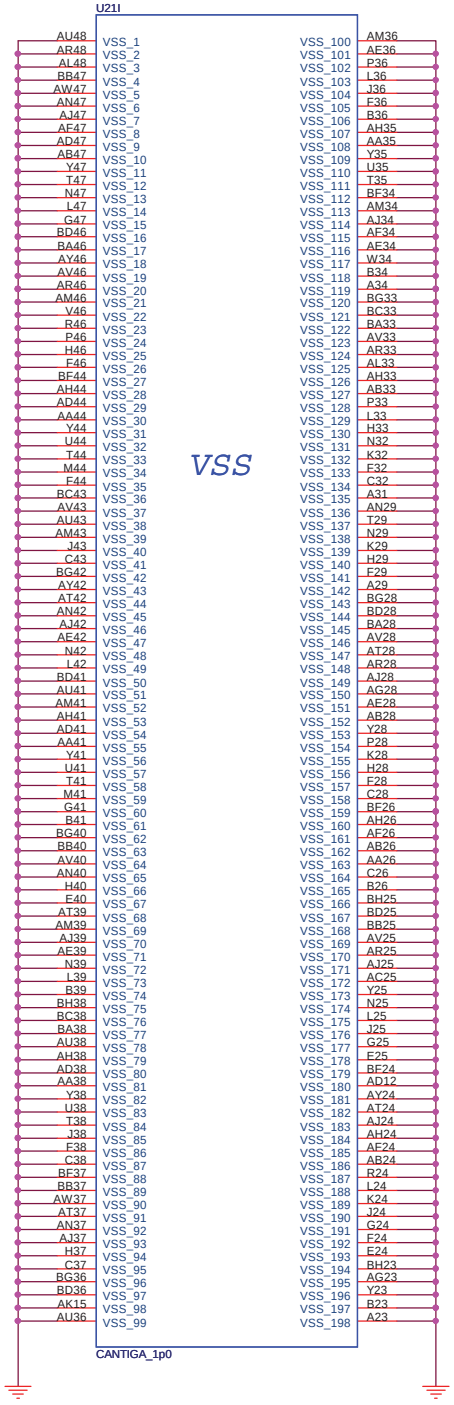
VCC NCTF

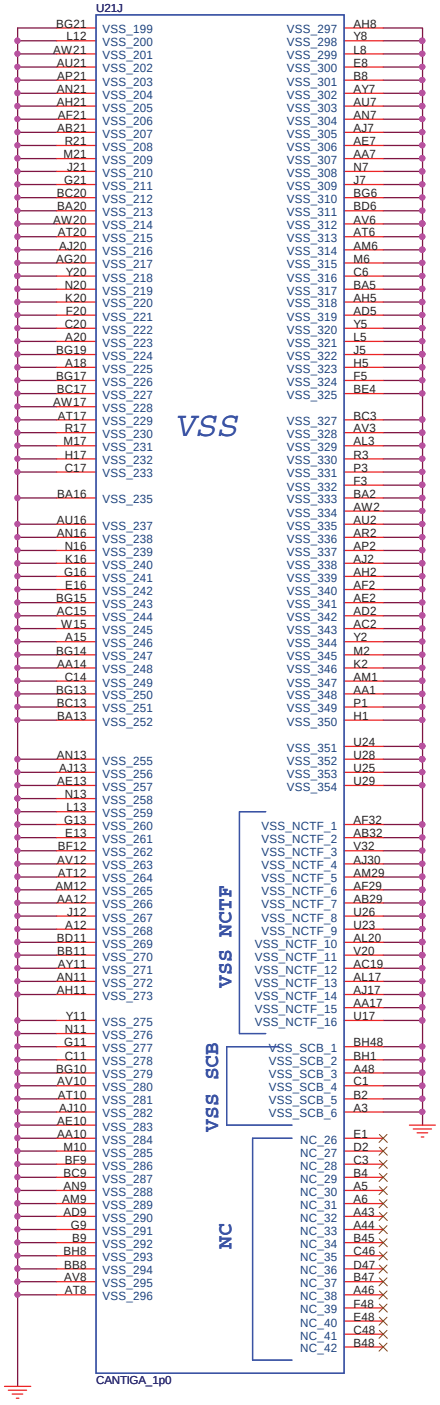
CANTIGA_1p0

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (VCC,NCTF)	1A
Date: Tuesday, September 16, 2008	Sheet 9	of 43


+1.05V_VCCP
+VCCA_DPLLA
+VCCA_DPLLB
+VCCA_HPLL
+VCCA_MPLL
+1.5V
+3.3V
+1.8V_SUS
+VCCA_PEG_PLL
+VCC_GMCH
U21H
CANTIGA_1p0
CRT
PLL
LVDS
A PEG
A SM
A CK
TV
HDA
TV/CRT
D
POWER
AXF
SM CK
HV
PEG
DMI
VTTLF
VTT
+VCC_CRTDAC
+VCC_TVBG
+VCC_TX_LVDS
+VCC_PEG_BG
+V1.05M_A_SM
+VCCA_SM_CK
+VCC_TVDACA_R
+VCC_HDA
+VCCD_TVDAC_R
+VCCQ_QDAC_R
+V1.05M_MCH_PLL
+VCCD_LVDS
+VCC_AXF
+VCC_SM_CK
+VCC_RXR_DMI
+VCC_PEG
+3V_VCC_HV
+VTTLF1
+VTTLF2
+VTTLF3
+V1.05S_PEGPLL_FB
For Teenah
For Cantiga
Modify for C-TEST
EC C-7 /7 Del L56,L57 Add R560,R559 1206 0 ohm.
PROJECT : AJ2
Quanta Computer Inc.
Cantiga (POWER)
Tuesday, September 16, 2008
Sheet 10 of 43





PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Cantiga (VSS)	1A
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DDR2 Dual channel A/B PU

DDRII A CHANNEL

+0.9V_DDR_VTT

Layout note: Place 1 cap close to every 1 R-pack terminated to SMDDR_VTERM.

C141 C136 C405 C408 C161 C448 C416 C87 C160 C109 C100 C112 C94

0.1U/16V/X7R_4

DDRII B CHANNEL

+0.9V_DDR_VTT

C90 C106 C131 C118 C154 C97 C83 C124 C89 C451 C86 C150 C133

0.1U/16V/X7R_4

+0.9V_DDR_VTT

+0.9V_DDR_VTT 33,36

8,13 DDR_A_MA[0..13]

DDR_B_MA[0..13] 8,13

DDR_A_MA11 DDR_A_MA7	RP47	56X2	RP16	56X2	DDR_B_MA11 DDR_B_MA7
DDR_A_MA6 DDR_A_MA4	RP46	56X2	RP11	56X2	DDR_B_MA6 DDR_B_MA2 SWAP
8,13 DDR_A_BS1 8,13 DDR_A_RAS#	RP44	56X2	RP5	56X2	DDR_B_BS1 8,13 DDR_B_RAS# 8,13
7,13 M_ODT0 DDR_A_MA13	RP43	56X2	RP2	56X2	DDR_B_MA13 M_ODT2 7,13
8,13 DDR_A_BS2 DDR_A_MA12	RP17	56X2	RP13	56X2	DDR_B_MA5 DDR_B_MA8
DDR_A_MA9 DDR_A_MA8	RP15	56X2	RP14	56X2	DDR_B_MA9 DDR_B_MA12
DDR_A_MA5 DDR_A_MA3	RP12	56X2	RP9	56X2	DDR_B_MA1 DDR_B_MA3
8,13 DDR_A_BS0 DDR_A_MA10	RP6	56X2	RP7	56X2	DDR_B_MA10 DDR_B_BS0 8,13
8,13 DDR_A_WE# 8,13 DDR_A_CAS#	RP4	56X2	RP3	56X2	DDR_B_WE# 8,13 DDR_B_CAS# 8,13
DDR_A_MA2 DDR_A_MA0	RP45	56X2	RP8	56X2	SWAP DDR_B_MA4 DDR_B_MA0

7,13 M_ODT1 DDR_A_MA1	R97 R102 R396 R100 R123 R405 R404	56_4	R95 R105 R101 R98 R109 R126 R125	M_ODT3 7,13 DDR_B_BS2 8,13
7,13 DDR_CS0_DIMMA#				DDR_CS2_DIMMB# 7,13
7,13 DDR_CS1_DIMMA#				DDR_CS3_DIMMB# 7,13
7,13 DDR_CKE0_DIMMA				DDR_CKE3_DIMMB 7,13
7,13 DDR_CKE1_DIMMA				DDR_CKE4_DIMMB 7,13
8,13 DDR_A_MA14				DDR_B_MA14 8,13

Please these resistor closely DIMMA,all trace length<750 mil.

Please these resistor closely DIMMB,all trace length<750 mil.

DDR2 Thermal Sensor SO-DIMM 0 & 1

Uninstall

+3.3V

30 mil

+3.3V 2,5,7,8,10,13,14,15,16,17,18,19,20,21,22,23,24,26,27,30,31,32,33

R48 *220_6

20 mil

C42 *0.1U/16V/X7R_4

U4

LM86_3V

2,13,26 CGCLK_SMB_M

2,13,26 CGDAT_SMB_M

7,13 PM_EXTTS#0

7 PM_EXTTS#1

R62 *0_4

8	SCLK	VCC	1
7	SDA	DXP	2
6	ALERT#	DXN	3
4	OVERT#	GND	5

DDR_THERMDA

DDR_THERMDC

*MMBT3904 Q14

*LM86CIMM

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR RES. ARRAY	1A

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A is required to route to Top SoDIMM for AMT to function.This will need to change for M08

DDR2 Dual channel A/B CONN

CN23 — PC4800 DDR2 SDRAM SO-DIMM (200P)

DIMM1_9.2

V_DDR_MCH_REF, +1.8V_SUS

DDR_A_DM[0..7] 8
DDR_A_D[0..63] 8
DDR_A_DQS[0..7] 8
DDR_A_DQS#[0..7] 8
DDR_A_MA[0..13] 8,12

1 VREF	2 VSS46	DDR_A_D0	DDR_A_D4
3 VSS47	4 DQ4	DDR_A_D1	DDR_A_D5
5 DQ0	6 DQ5		
7 DQ1	8 VSS15	DDR_A_DM0	
9 VSS37	10 DM0		
11 DQS#0	12 VSS5	DDR_A_DQS#0	DDR_A_D7
13 DQS0	14 DQ6	DDR_A_DQS0	DDR_A_D2
15 VSS48	16 DQ7		
17 DQ2	18 VSS16	DDR_A_D6	DDR_A_D8
19 DQ3	20 DQ12	DDR_A_D3	DDR_A_D9
21 VSS38	22 DQ13		
23 DQ8	24 VSS17	DDR_A_D12	DDR_A_DM1
25 DQ9	26 DM1	DDR_A_D13	
27 VSS49	28 VSS53		
29 DQS#1	30 CK0	DDR_A_DQS#1	M_CLK_DDR0 7
31 DQS1	32 CK0#	DDR_A_DQS1	M_CLK_DDR#0 7
33 VSS39	34 VSS41		
35 DQ10	36 DQ14	DDR_A_D14	DDR_A_D15
37 DQ11	38 DQ15	DDR_A_D11	DDR_A_D10
39 VSS50	40 VSS54		
41 VSS18	42 VSS20		
43 DQ16	44 DQ20	DDR_A_D21	DDR_A_D20
45 DQ17	46 DQ21	DDR_A_D17	DDR_A_D16
47 VSS1	48 VSS6		
49 DQS#2	50 NC3	DDR_A_DQS#2	PM_EXTTS#0
51 DQS2	52 DM2	DDR_A_DQS2	DDR_A_DM2
53 VSS19	54 VSS21		
55 DQ18	56 DQ22	DDR_A_D18	DDR_A_D22
57 DQ19	58 DQ23	DDR_A_D23	DDR_A_D19
59 VSS22	60 VSS24		
61 DQ24	62 DQ28	DDR_A_D28	DDR_A_D24
63 DQ25	64 DQ29	DDR_A_D29	DDR_A_D25
65 VSS23	66 VSS25		
67 DM3	68 DQS#3	DDR_A_DM3	DDR_A_DQS#3
69 NC4	70 DQS3		DDR_A_DQS3
71 VSS9	72 VSS10		
73 DQ26	74 DQ30	DDR_A_D30	DDR_A_D26
75 DQ27	76 DQ31	DDR_A_D31	DDR_A_D27
77 VSS4	78 VSS8		
79 CKE0	80 CKE1	7,12 DDR_CKE0_DIMMA	DDR_CKE1_DIMMA 7,12
81 VDD7	82 VDD8		
83 NC1	84 A15		
85 A16_BA2	86 A14	8,12 DDR_A_BS2	DDR_A_MA14 8,12
87 VDD9	88 VDD11		
89 A12	90 A11	DDR_A_MA12	DDR_A_MA11
91 A9	92 A7	DDR_A_MA9	DDR_A_MA7
93 A8	94 A6	DDR_A_MA8	DDR_A_MA6
95 VDD5	96 VDD4		
97 A5	98 A4	DDR_A_MA5	DDR_A_MA4
99 A3	100 A2	DDR_A_MA3	DDR_A_MA2
101 A1	102 A0	DDR_A_MA1	DDR_A_MA0
103 VDD10	104 VDD12		
105 A10/AP	106 BA1	DDR_A_MA10	DDR_A_BS1 8,12
107 BA0	108 RAS#	8,12 DDR_A_BS0	DDR_A_RAS# 8,12
109 WE#	110 S0#	8,12 DDR_A_WE#	DDR_CS0_DIMMA# 7,12
111 VDD2	112 VDD1		
113 CAS#	114 ODT0	8,12 DDR_A_CAS#	M_ODT0 7,12
115 S1#	116 A13	7,12 DDR_CS1_DIMMA#	DDR_A_MA13
117 VDD3	118 VDD6		
119 ODT1	120 NC2	7,12 M_ODT1	
121 VSS11	122 VSS12		
123 DQ32	124 DQ36	DDR_A_D36	DDR_A_D33
125 DQ33	126 DQ37	DDR_A_D37	DDR_A_D32
127 VSS26	128 VSS28		
129 DQS#4	130 DM4	DDR_A_DQS#4	DDR_A_DM4
131 DQS4	132 VSS42	DDR_A_DQS4	
133 VSS2	134 DQ38		DDR_A_D34
135 DQ34	136 DQ39	DDR_A_D39	DDR_A_D38
137 DQ35	138 VSS55	DDR_A_D35	
139 VSS27	140 DQ44		DDR_A_D44
141 DQ40	142 DQ45	DDR_A_D41	DDR_A_D45
143 DQ41	144 VSS43	DDR_A_D40	
145 VSS29	146 DQS#5		DDR_A_DQS#5
147 DM5	148 DQS5	DDR_A_DM5	DDR_A_DQS5
149 VSS51	150 VSS56		
151 DQ42	152 DQ46	DDR_A_D46	DDR_A_D43
153 DQ43	154 DQ47	DDR_A_D47	DDR_A_D42
155 VSS40	156 VSS44		
157 DQ48	158 DQ52	DDR_A_D48	DDR_A_D52
159 DQ49	160 DQ53	DDR_A_D53	DDR_A_D49
161 VSS52	162 VSS57		
163 NCTEST	164 CK1		M_CLK_DDR1 7
165 VSS30	166 CK1#		M_CLK_DDR#1 7
167 DQS#6	168 VSS45	DDR_A_DQS#6	
169 DQS6	170 DM6	DDR_A_DQS6	DDR_A_DM6
171 VSS31	172 VSS32		
173 DQ50	174 DQ54	DDR_A_D51	DDR_A_D54
175 DQ51	176 DQ55	DDR_A_D50	DDR_A_D55
177 VSS33	178 VSS35		
179 DQ56	180 DQ60	DDR_A_D57	DDR_A_D60
181 DQ57	182 DQ61	DDR_A_D61	DDR_A_D56
183 VSS3	184 VSS7		
185 DM7	186 DQS#7	DDR_A_DM7	DDR_A_DQS#7
187 VSS34	188 DQS7		DDR_A_DQS7
189 DQ58	190 VSS36	DDR_A_D62	
191 DQ59	192 DQ62	DDR_A_D59	DDR_A_D58
193 VSS14	194 DQ63		DDR_A_D63
195 SDA	196 VSS13	2,12,26 CGDAT_SMB_M	
197 SCL	198 SA0	2,12,26 CGCLK_SMB_M	
199 VDD(SPD)	200 SA1		

+3.3V

R363 10K_4
R365 10K_4

CKE 0,1
CLOCK 0,1

SMbus address A0

CN24 — PC4800 DDR2 SDRAM SO-DIMM (200P)

DIMM2_5.2

V_DDR_MCH_REF, +1.8V_SUS

DDR_B_DM[0..7] 8
DDR_B_D[0..63] 8
DDR_B_DQS[0..7] 8
DDR_B_DQS#[0..7] 8
DDR_B_MA[0..13] 8,12

1 VREF	2 VSS46	DDR_B_D0	DDR_B_D4
3 VSS47	4 DQ4	DDR_B_D5	DDR_B_D1
5 DQ0	6 DQ5		
7 DQ1	8 VSS15		DDR_B_DM0
9 VSS37	10 DM0		
11 DQS#0	12 VSS5	DDR_B_DQS#0	DDR_B_D7
13 DQS0	14 DQ6	DDR_B_DQS0	DDR_B_D6
15 VSS48	16 DQ7		
17 DQ2	18 VSS16	DDR_B_D3	DDR_B_D12
19 DQ3	20 DQ12	DDR_B_D2	DDR_B_D13
21 VSS38	22 DQ13		
23 DQ8	24 VSS17	DDR_B_D9	DDR_B_DM1
25 DQ9	26 DM1	DDR_B_D8	
27 VSS49	28 VSS53		
29 DQS#1	30 CK0	DDR_B_DQS#1	M_CLK_DDR3 7
31 DQS1	32 CK0#	DDR_B_DQS1	M_CLK_DDR#3 7
33 VSS39	34 VSS41		
35 DQ10	36 DQ14	DDR_B_D10	DDR_B_D11
37 DQ11	38 DQ15	DDR_B_D14	DDR_B_D15
39 VSS50	40 VSS54		
41 VSS18	42 VSS20		
43 DQ16	44 DQ20	DDR_B_D21	DDR_B_D17
45 DQ17	46 DQ21	DDR_B_D20	DDR_B_D16
47 VSS1	48 VSS6		
49 DQS#2	50 NC3	DDR_B_DQS#2	PM_EXTTS#0 7,12
51 DQS2	52 DM2	DDR_B_DQS2	DDR_B_DM2
53 VSS19	54 VSS21		
55 DQ18	56 DQ22	DDR_B_D22	DDR_B_D19
57 DQ19	58 DQ23	DDR_B_D23	DDR_B_D18
59 VSS22	60 VSS24		
61 DQ24	62 DQ28	DDR_B_D28	DDR_B_D24
63 DQ25	64 DQ29	DDR_B_D29	DDR_B_D25
65 VSS23	66 VSS25		
67 DM3	68 DQS#3	DDR_B_DM3	DDR_B_DQS#3
69 NC4	70 DQS3		DDR_B_DQS3
71 VSS9	72 VSS10		
73 DQ26	74 DQ30	DDR_B_D30	DDR_B_D27
75 DQ27	76 DQ31	DDR_B_D26	DDR_B_D31
77 VSS4	78 VSS8		
79 CKE0	80 CKE1	7,12 DDR_CKE3_DIMMB	DDR_CKE4_DIMMB 7,12
81 VDD7	82 VDD8		
83 NC1	84 A15		
85 A16_BA2	86 A14	8,12 DDR_B_BS2	DDR_B_MA14 8,12
87 VDD9	88 VDD11		
89 A12	90 A11	DDR_B_MA12	DDR_B_MA11
91 A9	92 A7	DDR_B_MA9	DDR_B_MA7
93 A8	94 A6	DDR_B_MA8	DDR_B_MA6
95 VDD5	96 VDD4		
97 A5	98 A4	DDR_B_MA5	DDR_B_MA4
99 A3	100 A2	DDR_B_MA3	DDR_B_MA2
101 A1	102 A0	DDR_B_MA1	DDR_B_MA0
103 VDD10	104 VDD12		
105 A10/AP	106 BA1	DDR_B_MA10	DDR_B_BS1 8,12
107 BA0	108 RAS#	8,12 DDR_B_BS0	DDR_B_RAS# 8,12
109 WE#	110 S0#	8,12 DDR_B_WE#	DDR_CS2_DIMMB# 7,12
111 VDD2	112 VDD1		
113 CAS#	114 ODT0	8,12 DDR_B_CAS#	M_ODT2 7,12
115 S1#	116 A13	7,12 DDR_CS3_DIMMB#	DDR_B_MA13
117 VDD3	118 VDD6		
119 ODT1	120 NC2	7,12 M_ODT3	
121 VSS11	122 VSS12		
123 DQ32	124 DQ36	DDR_B_D36	DDR_B_D37
125 DQ33	126 DQ37	DDR_B_D34	DDR_B_D32
127 VSS26	128 VSS28		
129 DQS#4	130 DM4	DDR_B_DQS#4	DDR_B_DM4
131 DQS4	132 VSS42	DDR_B_DQS4	
133 VSS2	134 DQ38		DDR_B_D39
135 DQ34	136 DQ39	DDR_B_D38	DDR_B_D33
137 DQ35	138 VSS55	DDR_B_D35	
139 VSS27	140 DQ44		DDR_B_D45
141 DQ40	142 DQ45	DDR_B_D41	DDR_B_D44
143 DQ41	144 VSS43	DDR_B_D40	
145 VSS29	146 DQS#5		DDR_B_DQS#5
147 DM5	148 DQS5	DDR_B_DM5	DDR_B_DQS5
149 VSS51	150 VSS56		
151 DQ42	152 DQ46	DDR_B_D47	DDR_B_D42
153 DQ43	154 DQ47	DDR_B_D43	DDR_B_D46
155 VSS40	156 VSS44		
157 DQ48	158 DQ52	DDR_B_D53	DDR_B_D48
159 DQ49	160 DQ53	DDR_B_D49	DDR_B_D52
161 VSS52	162 VSS57		
163 NCTEST	164 CK1		M_CLK_DDR4 7
165 VSS30	166 CK1#		M_CLK_DDR#4 7
167 DQS#6	168 VSS45	DDR_B_DQS#6	
169 DQS6	170 DM6	DDR_B_DQS6	DDR_B_DM6
171 VSS31	172 VSS32		
173 DQ50	174 DQ54	DDR_B_D55	DDR_B_D54
175 DQ51	176 DQ55	DDR_B_D50	DDR_B_D51
177 VSS33	178 VSS35		
179 DQ56	180 DQ60	DDR_B_D57	DDR_B_D56
181 DQ57	182 DQ61	DDR_B_D61	DDR_B_D60
183 VSS3	184 VSS7		
185 DM7	186 DQS#7	DDR_B_DM7	DDR_B_DQS#7
187 VSS34	188 DQS7		DDR_B_DQS7
189 DQ58	190 VSS36	DDR_B_D62	
191 DQ59	192 DQ62	DDR_B_D63	DDR_B_D59
193 VSS14	194 DQ63		DDR_B_D58
195 SDA	196 VSS13	CGDAT_SMB_M	
197 SCL	198 SA0	CGCLK_SMB_M	
199 VDD(SPD)	200 SA1		

GND 202

+3.3V

R53 10K_4 +3.3V
R54 10K_4

CKE 2,3
CLOCK 3,4

SMbus address A4

+3.3V 2,5,7,8,10,12,14,15,16,17,18,19,20,21,22,23,24,26,27,30,31,32,33

+1.8V_SUS
C119 0.1U/16V/X7R_4
C117 0.1U/16V/X7R_4

Place these Caps near So-Dimm1.

+1.8V_SUS
C182 *330U/2.5V_7343
C144 C103 C101 C113 C122 2.2U/6.3V/X5R_6

+1.8V_SUS
C127 C95 C151 C107 0.1U/16V/X7R_4

V_DDR_MCH_REF, +3.3V
C505 C508 0.1U/16V/X7R_4, 2.2U/6.3V/X5R_6
C47 C48 2.2U/6.3V/X5R_6, 0.1U/16V/X7R_4

Place these Caps near So-Dimm2.

+1.8V_SUS
C149 C138 C110 C125 C140 2.2U/6.3V/X5R_6

+1.8V_SUS
C129 C142 C99 C132 0.1U/16V/X7R_4

V_DDR_MCH_REF, +3.3V
C501 C507 0.1U/16V/X7R_4, 2.2U/6.3V/X5R_6
C40 C43 2.2U/6.3V/X5R_6, 0.1U/16V/X7R_4

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR SO-DIMM(200P)	1A
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RTC

AZ Interface(MDC, CODEC, HDMI)

AC-TX for SATA

SB Strap

ICH8-M LAN100_SLP Strap (Internal VR for VccLAN1_05 and VccCL1.05)

LAN100_SLP	Low = Internal VR disable High = Internal VR enable(Default)

ICH8M Internal VR Enable Strap (Internal VR for VccSus1.05, VccSus1.5, VccCL1.5)	
ICH_INTVRMEN	Low = Internal VR Disabled High = Internal VR Enabled(Default)

XOR Chain Entrance Strap		
ICH TP3	HDA SDOUT	Description
0	0	RSVD
0	1	Enter XOR Chain
1	0	Normal Operation (Default)
1	1	Set PCIE port config bit 1

Reserved for Intel Nineveh design.

Place all series terms close to ICH9 except for SDIN input lines,which should be close to source.Placement of R603, R600, R607 & R612 should equal distance to the T split trace point as R604, R599, R606 & R608 respective. Basically,keep the same distance from T for all series termination resistors.

Distance between the ICH-9 M and cap on the "P" signal should be identical distance between the ICH-9 M and cap on the "N" signal for same pair.

Place within 500mils of ICH9 ball

EMC reserved

ICH9M REV 1.0

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (CPU,IDE,SATA,LPC,AC97,LAN)	1A
Date: Tuesday, September 16, 2008	Sheet 14 of 43	

Place TX DC blocking caps close ICH8.

OC# pull up

RP49 10P8R-10K

USB_OC2#	6	5	+3.3V_SUS
OC9#	7	4	USB_OC3#
USB_OC5#	8	3	WLAN_RF_OFF#
USB_OC4#	9	2	USB_OC0#
+3.3V_SUS	10	1	OC#_NWC

+3.3V_SUS	R234	2	1	10K_4 OC10#
	R231	2	1	10K_4 OC11#
	R238	2	1	10K_4 USB_OC7#
	R237	2	1	10K_4 USB_OC1#

MiniCard-1 (WLAN) / MiniCard-2 / Express Card (NEWCARD)

26	PCIE_RX1-				N29 PERN1
26	PCIE_RX1+				N28 PERP1
26	PCIE_TX1-	C230	0.1U/16V/X7R_4	PCIE_TXN1_C	P27 PETN1
26	PCIE_TX1+	C233	0.1U/16V/X7R_4	PCIE_TXP1_C	P26 PETP1
26	PCIE_RX2-				L29 PERN2
26	PCIE_RX2+				L28 PERP2
26	PCIE_TX2-	C237	0.1U/16V/X7R_4	PCIE_TXN2_C	M27 PETN2
26	PCIE_TX2+	C242	0.1U/16V/X7R_4	PCIE_TXP2_C	M26 PETP2
32	PCIE_RXN3				J29 PERN3
32	PCIE_RXP3				J28 PERP3
32	PCIE_TXN3	C247	0.1U/16V/X7R_4	PCIE_TXN3_C	K27 PETN3
32	PCIE_TXP3	C262	0.1U/16V/X7R_4	PCIE_TXP3_C	K26 PETP3
		T12			G29 PERN4
		T12			G28 PERP4
		T12			H27 PETN4
		T56			H26 PETP4
		T13			E29 PERN5
		T13			E28 PERP5
		T12			F27 PETN5
		T62			F26 PETP5
21	PCIE_RX6-/GLAN_RX-				C29 PERN6/GLAN_RXN
21	PCIE_RX6+/GLAN_RX+	C268	0.1U/16V/X7R_4	GLAN_TXN_C	C28 PERP6/GLAN_RXP
21	PCIE_TX6-/GLAN_TX-	C267	0.1U/16V/X7R_4	GLAN_TXP_C	D27 PETN6/GLAN_TXN
21	PCIE_TX6+/GLAN_TX+				D26 PETP6/GLAN_TXP

U25D

PCI-Express / Direct Media Interface

DMI0RXN	V27	DMI_MTX_IRX_N0 7
DMI0RXP	V26	DMI_MTX_IRX_P0 7
DMI0TXN	U29	DMI_MRX_ITX_N0 7
DMI0TXP	U28	DMI_MRX_ITX_P0 7
DMI1RXN	Y27	DMI_MTX_IRX_N1 7
DMI1RXP	Y26	DMI_MTX_IRX_P1 7
DMI1TXN	W29	DMI_MRX_ITX_N1 7
DMI1TXP	W28	DMI_MRX_ITX_P1 7
DMI2RXN	AB27	DMI_MTX_IRX_N2 7
DMI2RXP	AB26	DMI_MTX_IRX_P2 7
DMI2TXN	AA29	DMI_MRX_ITX_N2 7
DMI2TXP	AA28	DMI_MRX_ITX_P2 7
DMI3RXN	AD27	DMI_MTX_IRX_N3 7
DMI3RXP	AD26	DMI_MTX_IRX_P3 7
DMI3TXN	AC29	DMI_MRX_ITX_N3 7
DMI3TXP	AC28	DMI_MRX_ITX_P3 7
DMI_CLKN	T26	CLK_PCIE_ICH# 2
DMI_CLKP	T25	CLK_PCIE_ICH 2
DMI_ZCOMP	AF29	
DMI_IRCOMP	AF28	R219 24.9/F_4 +1.5V_PCIE_ICH

Place within 500mils of ICH9

SPI

SPI_CLK_R	D23	SPI_CLK
SPI_CS0#_R	D24	SPI_CS0#
SPI_CS1#_R	F23	SPI_CS1#/GPIO58/CLGPIO6
SPI_MOSI_R	D25	SPI_MOSI
SPI_MISO_R	E23	SPI_MISO

USB

USB_OC0#	N4	OC0#/GPIO59
USB_OC1#	N5	OC1#/GPIO40
USB_OC2#	N6	OC2#/GPIO41
USB_OC3#	P5	OC3#/GPIO42
USB_OC4#	M1	OC4#/GPIO43
USB_OC5#	N2	OC5#/GPIO29
WLAN_RF_OFF#	M4	OC6#/GPIO30
USB_OC7#	M3	OC7#/GPIO31
OC#_NWC	N3	OC8#/GPIO44
OC9#	N1	OC9#/GPIO45
OC10#	P5	OC10#/GPIO46
OC11#	P3	OC11#/GPIO47

28 USB_OC1#
28 USB_OC2#
26,31 WLAN_RF_OFF#
32 OC#_NWC

R464 22.6/F USB_RBIAS_PN — USBRBIAS / USBRBIAS#

placed within 500-mils of the ICH9M

ICH9M REV 1.0

USBP0N	AC5	USBP0- 28
USBP0P	AC4	USBP0+ 28
USBP1N	AD3	USBP1- 28
USBP1P	AD2	USBP1+ 28
USBP2N	AC1	USBP2- 28
USBP2P	AC2	USBP2+ 28
USBP3N	AA5	USBP3- 32
USBP3P	AA4	USBP3+ 32
USBP4N	AB2	USBP4- 26
USBP4P	AB3	USBP4+ 26
USBP5N	AA1	USBP5- 28
USBP5P	AA2	USBP5+ 28
USBP6N	W5	USBP6- T49
USBP6P	W4	USBP6+ T51
USBP7N	Y3	USBP7- 26
USBP7P	Y2	USBP7+ 26
USBP8N	W1	USBP8- 18
USBP8P	W2	USBP8+ 18
USBP9N	V2	USBP9- 29
USBP9P	V3	USBP9+ 29
USBP10N	U5	ICH_USBP10- T54
USBP10P	U4	ICH_USBP10+ T53
USBP11N	U1	ICH_USBP11- T122
USBP11P	U2	ICH_USBP11+ T123

- USB-0
- USB-1
- TO Board USB-0
- NEWCARD
- MiniCard-1 (WLAN)
- TO Board USB-1
- MiniCard-2(reserved)
- WEB CAM
- BLUETOOTH

SPI ROM

20 mil

C256 *0.1U/16V/X7R_4 FAI Remove

C257 *0.1U/16V/X7R_4

R251 *10K/F_4 — R295 *10K/F_4

U10 *MX25L512MC-12G

SPI_CS#0	R293	*22_4	SPI_CS#0_R	
SPI_CLK	R252	*22_4	SPI_CLK_R	
SPI_MOSI	R253	*22_4	SPI_MOSI_R	
SPI_MISO	R294	*22_4	SPI_MISO_R	
SPI_HOLD#				
SPI_WP#				

EC B-12 /15 Add U31 for HDCP support.

512K byte SPI ROM

PCI Pullups

+3.3V_S5	R492	2	1	10K_4 PCI_PME#
+3.3V	R269			8.2K_4 PCI_FRAME#

RP34 10P8R-8.2K

PCI_IRDY#	6	5	PCI_PERR#
PCI_PLOCK#	7	4	PCI_PIRQD#
PCI_TRDY#	8	3	PCI_STOP#
PCI_PIRQC#	9	2	PCI_DEVSEL#
+3.3V	10	1	

RP50 10P8R-8.2K

ICH_GPIO3_PIRQF#	6	5	PCI_PIRQB#
ICH_GPIO2_PIRQE#	7	4	ICH_GPIO4_PIRQG#
PCI_PIRQA#	8	3	PCI_REQ0#
PCI_SERR#	9	2	ICH_GPIO5_PIRQH#
+3.3V	10	1	

PCI

U25B

AD0	D11	REQ0#	F1	PCI_REQ0# 23
AD1	C8	GNT0#	G4	PCI_GNT0# 23
AD2	D9	REQ1#/GPIO50	B6	BOARD_ID1 16
AD3	E12	GNT1#/GPIO51	A7	PCI_GNT1# T139
AD4	F9	REQ2#/GPIO52	F13	BOARD_ID2 16
AD5	C9	GNT2#/GPIO53	F12	PCI_GNT2# T61
AD6	E10	REQ3#/GPIO54	E6	BOARD_ID3 16
AD7	B7	GNT3#/GPIO55	F6	PCI_GNT3#
AD8	C7			
AD9	C5	C/BE0#	D8	C/BE0# 23
AD10	G11	C/BE1#	B4	C/BE1# 23
AD11	F8	C/BE2#	D6	C/BE2# 23
AD12	F11	C/BE3#	A5	C/BE3# 23
AD13	E7			
AD14	A3	IRDY#	D3	PCI_IRDY# 23
AD15	D2	PAR	E3	PCI_PAR 23
AD16	F10	PCIRST#	R1	PCIRST# 20,23
AD17	D5	DEVSEL#	C6	PCI_DEVSEL# 23
AD18	D10	PERR#	E4	PCI_PERR#
AD19	B3	PLOCK#	C2	PCI_PLOCK#
AD20	E7	SERR#	J4	PCI_SERR#
AD21	C3	STOP#	A4	PCI_STOP# 23
AD22	E3	TRDY#	F5	PCI_TRDY# 23
AD23	E4	FRAME#	D7	PCI_FRAME# 23
AD24	C1			
AD25	G7	PLTRST#	C14	PLTRST#_NB
AD26	H7	PCICLK	D4	CLK_PCI_ICH 2
AD27	D1	PME#	R2	PCI_PME# 23
AD28	G5			
AD29	H6			
AD30	G1			
AD31	H3			

23 AD[0..31]

Reserved for EMI. Place resister and cap close to ICH.

CLK_PCI_ICH — R273 *10_4 — C275 *10P/50V/COG_4

PLTRST#_NB 7

+3.3V_SUS — C288 0.1U/16V/X7R_4 — U11 TC7SH08FU(F) — PLTRST# 7,21,22,26,32 — R299 100K_4

Interrupt I/F

23 PCI_PIRQA#	PCI_PIRQA#	J5	PIRQA#	PIRQE#/GPIO2 H4 ICH_GPIO2_PIRQE# T77
T131	PCI_PIRQB#	E1	PIRQB#	PIRQF#/GPIO3 K6 ICH_GPIO3_PIRQF# T71
T57	PCI_PIRQC#	J6	PIRQC#	PIRQG#/GPIO4 E2 ICH_GPIO4_PIRQG# T129
T79	PCI_PIRQD#	C4	PIRQD#	PIRQH#/GPIO5 G2 ICH_GPIO5_PIRQH# T125

ICH9M REV 1.0

Boot BIOS Strap

SPI_CS1#_R — R259 *1K_4
PCI_GNT0# — R260 *1K_4

		GNT0#	SPI_CS1#
LPC	11	No stuff	No stuff
PCI	10	No stuff	Stuff
SPI	01	Stuff	No stuff

PCI_GNT3# — R258 *1K_4

A16 away override strap.

Low = A16 swap override enabled.
High = Default.

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
A3	ICH9-M (USB,DMI,PCIE,PCI)	1A
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Non-iAMT ASF 2.0

Option to " Disable " clkrun. Pulling it down will keep the clks running.

Place these close to ICH8.

Board ID	ID3	ID2	ID1	ID0
INTEL SENTAROSA	1	1	1	1
INTEL MENTAVIRA	1	1	0	0
AMD	1	0	1	1
NVIDIA	1	0	0	1

Modify for FAI

GPIO[20]--Integrated Pull-Down 20K.

Modify for FAI

No Reboot strap.

ACZ_SPKR	Low = Default. High = No Reboot.

Non-iAMT For ME

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (PM,GPIO,SMB,CL)	1A
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U25E

ICH9M REV 1.0

EC A-04/01 chamge C479,C493 to 10, R448,R417 to 100 ohm for USB 1.0 can't work and meet Intel Spec.

10 mil

20 mil

20 mil

FB_330ohm+-25%_100mHz_ 1.5A_0.09 ohm DC

10uH+-20%_100mA

1uH+-20%_800mA

U25F

ICH9M REV 1.0

Modify for C-TEST

EC C-7 /8 only UMA Stuff.

Vout=1.25(1+R1/R2)

Impact ICH9M VCCHDA and VCCSUSHDA supply 1.5V/3.3V

Support INT HDMI HDA interface. These power only support 1.5V.Device must to meet.

NOTE:
If (G)MCH's HD Audio signals are connected to ICH9M for iHDMI, VCCHDA and VCCSUSHDA on ICH9M should be only on 1.5V. These power pins on ICH9M can be supplied with 3.3V if and only if (G)MCH's HDA is not connected to ICH9M. Consequently, only 1.5V audio/modem codecs can be used on the platform.

WWAN Noise - ICH improvements

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH9-M (POWER,GND)	1A
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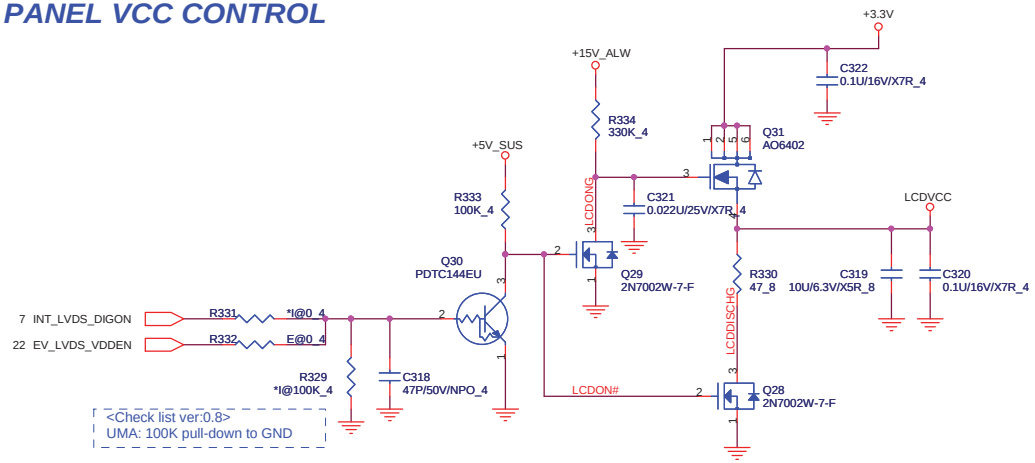
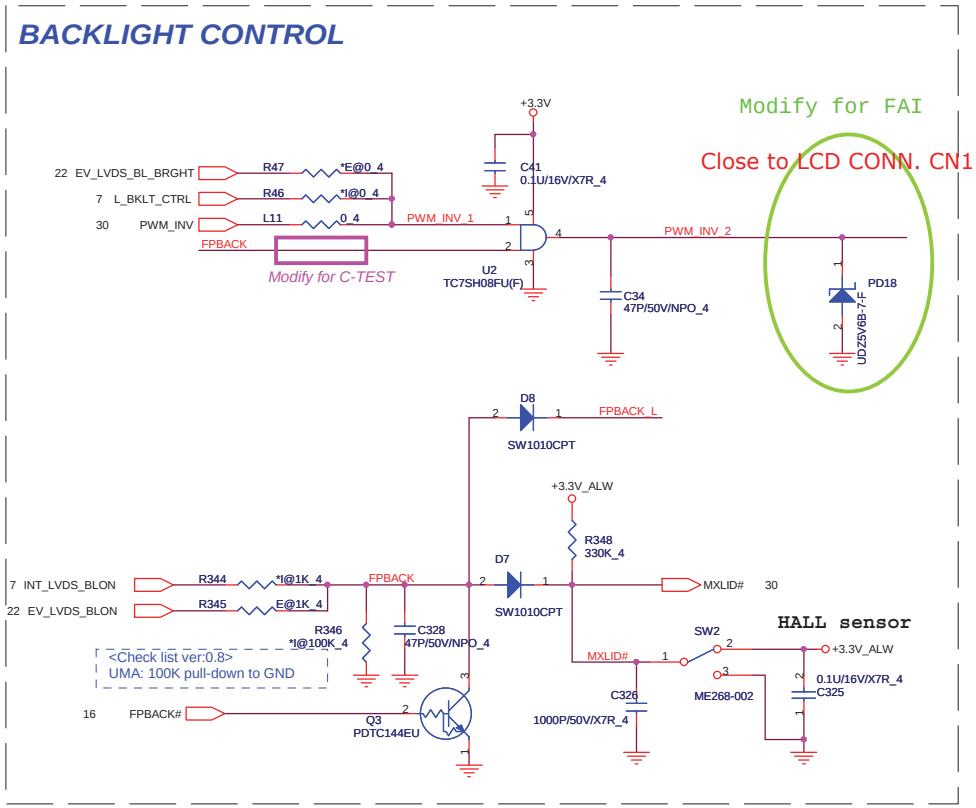
WEB CAM(Include BACKLIGHT function)

PANEL VCC CONTROL

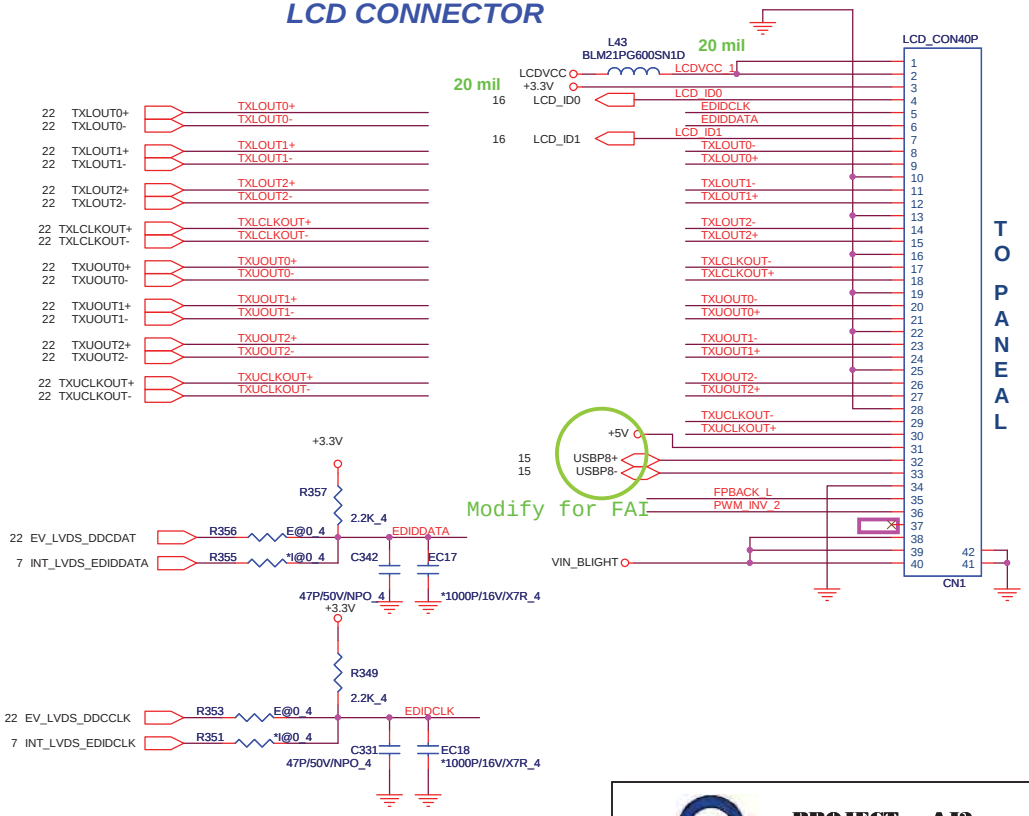


	Single LVDS 1366*768	Dial LVDS 1920*1080
LCD_ID0	TBD	TBD
LCD_ID1	HIGH	LOW

BACKLIGHT CONTROL



LCD CONNECTOR



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	LVDS/LCD CONN/LID/WEB CAM	1A
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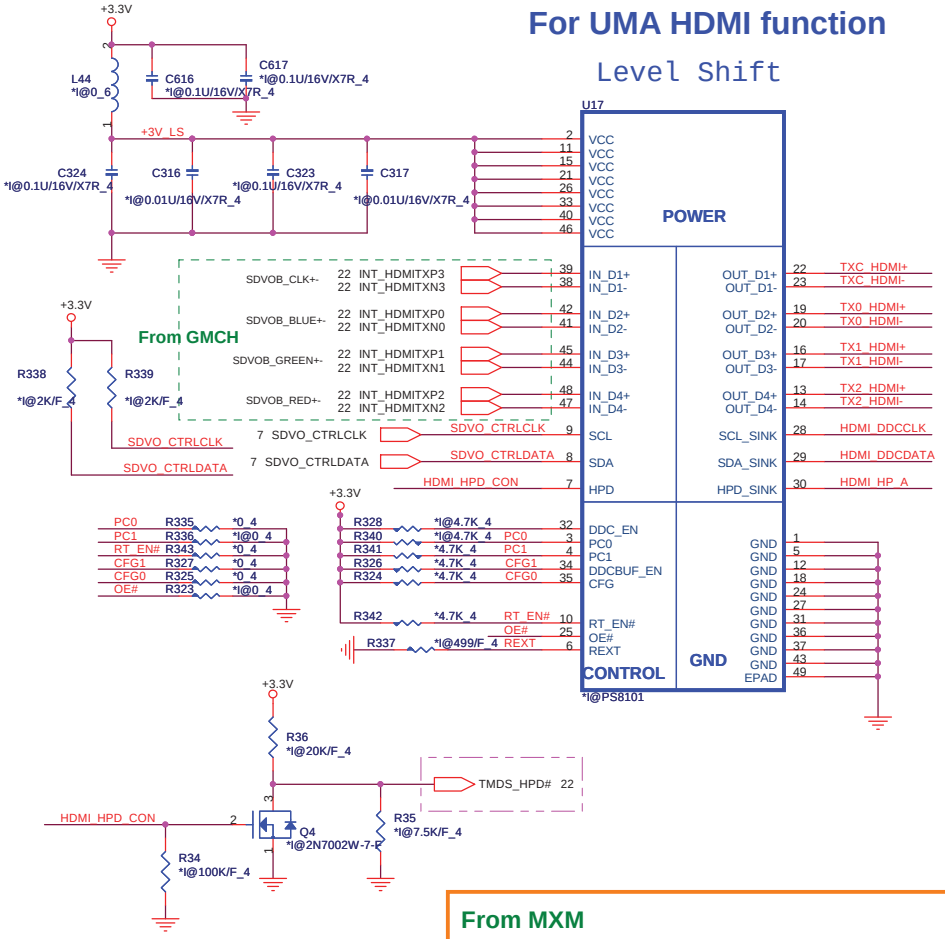
For UMA HDMI function

Level Shift



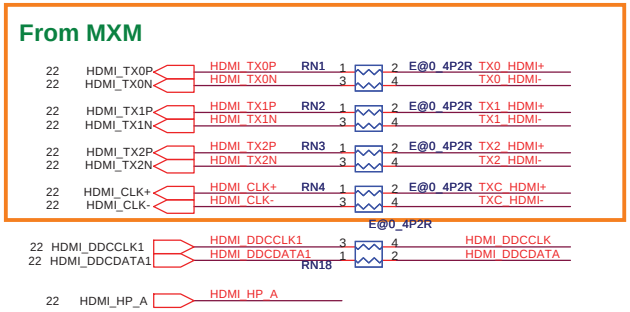
EQUALIZATION SETTING

PC1:PC0=0:0	8dB
PC1:PC0=0:1	4dB Recommanded
PC1:PC0=1:0	12dB
PC1:PC0=1:1	0dB

SCLZ/SDAZ Low-level input/output Voltage

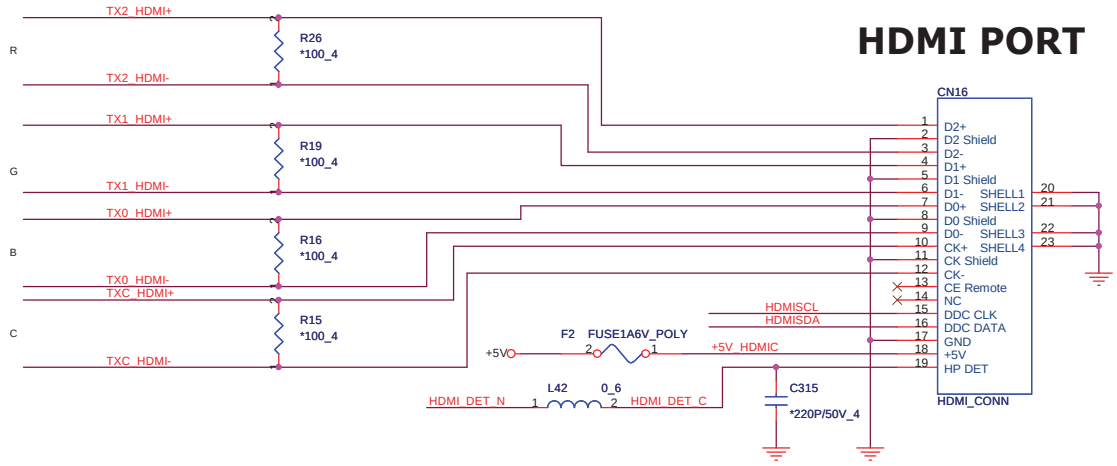
CFG1:CFG0=0:0	VIL:<0.4V VOL:0.6V (Default)
CGF1:CGF0=0:1	VIL:<0.36V VOL:0.55V
CGF1:CGF0=1:0	VIL:<0.44V VOL:0.65V
CGF1:CGF0=1:1	VIL:<0.36V VOL:0.6V

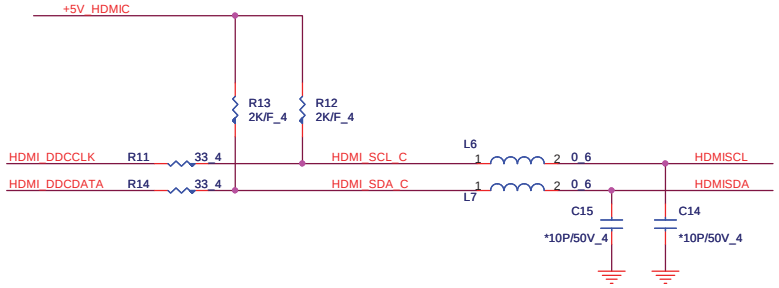
From MXM

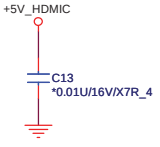


MXM DOES NOT NEED LEVEL SHIFT.
BYPASS PATH RESISTERS.

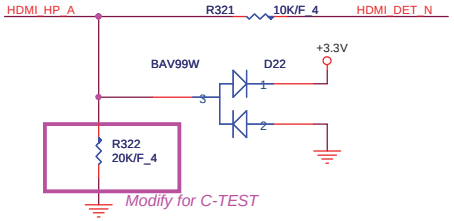
HDMI PORT







for EMI request



Modify for C-TEST

PROJECT : AJ2			
Quanta Computer Inc.			
Size: Custom	Document Number: HDMI		Rev: 1A
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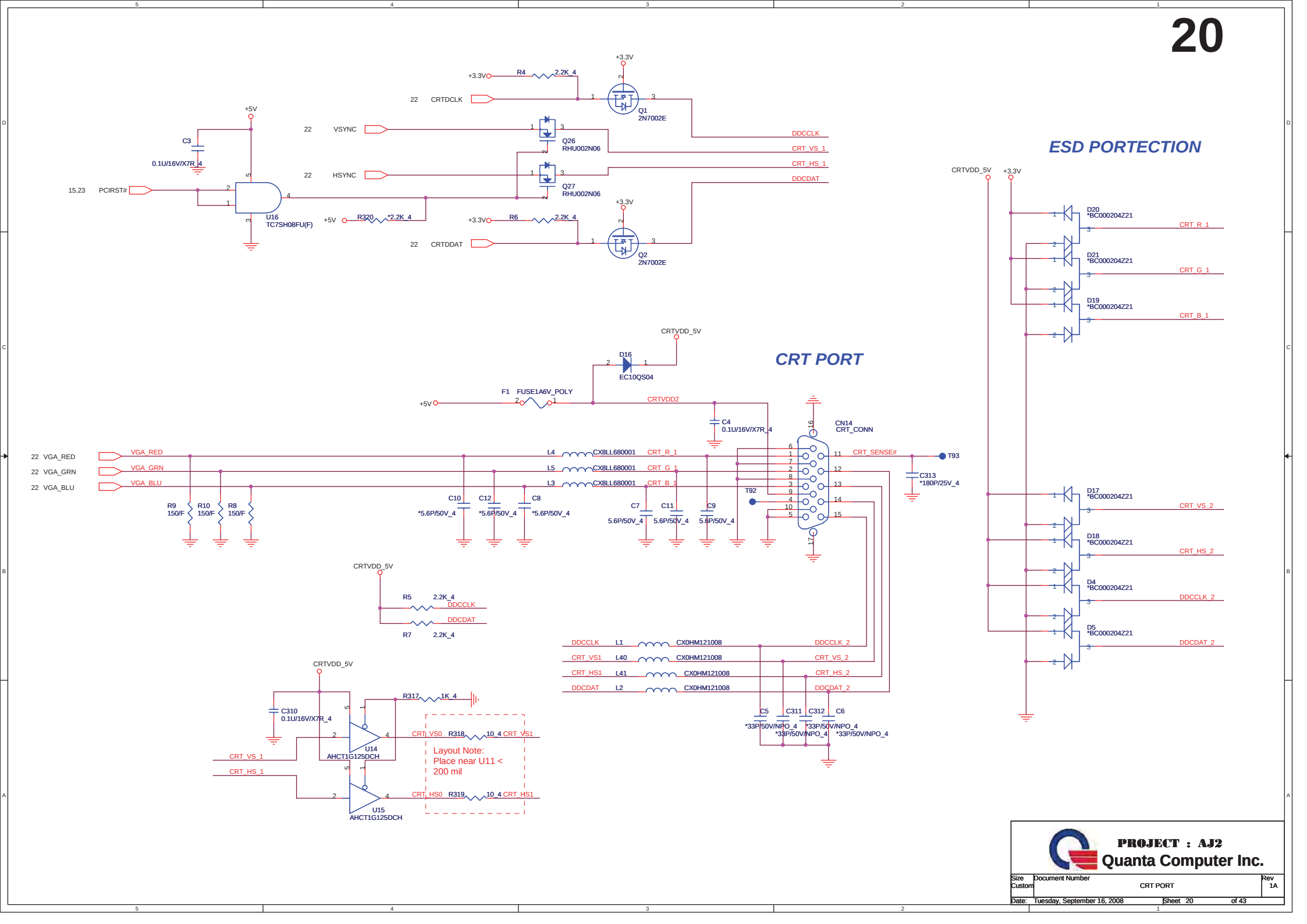

PROJECT : AJ2

Quanta Computer Inc.

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Custom	CRT PORT	1A
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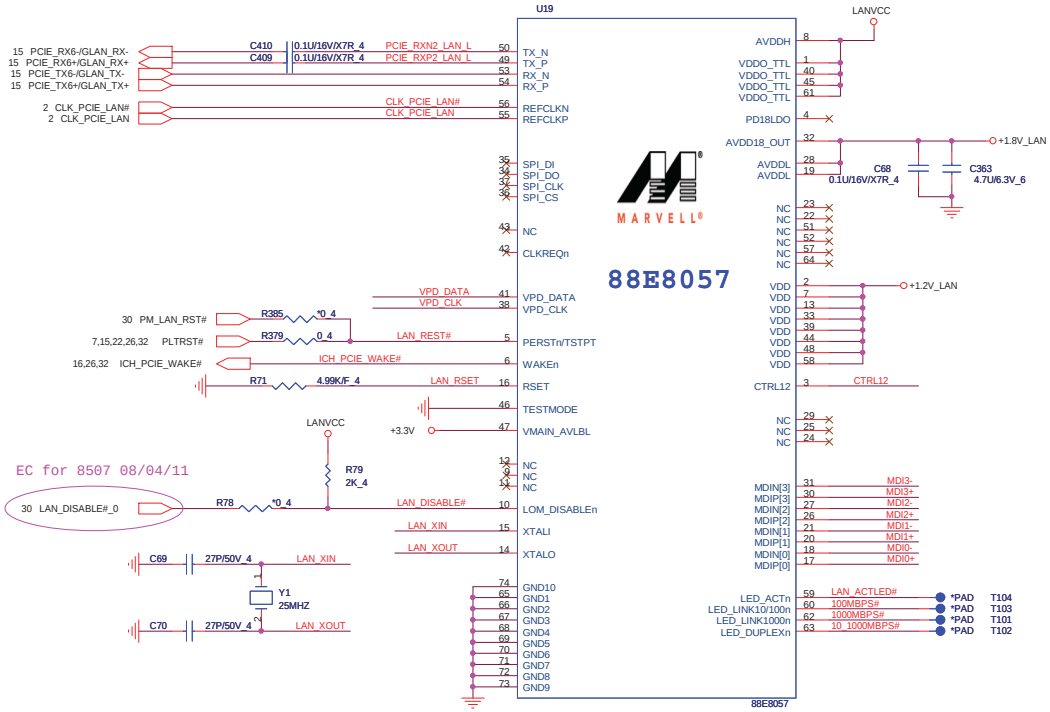
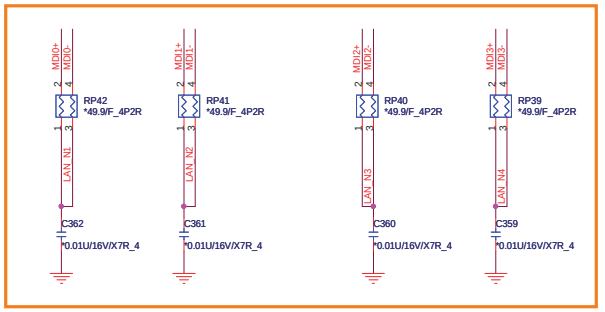
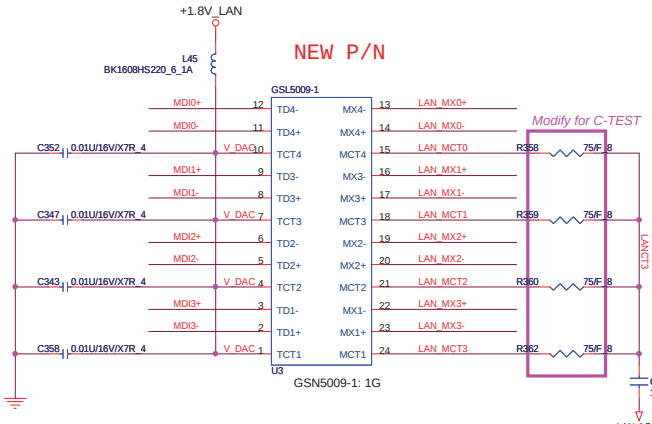
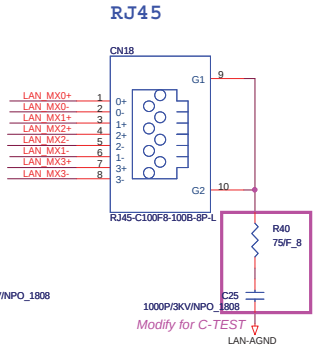
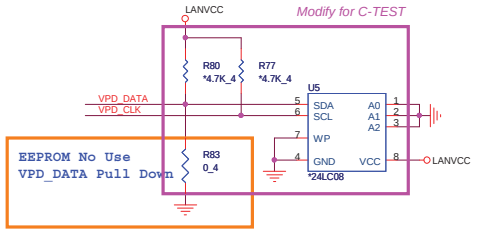


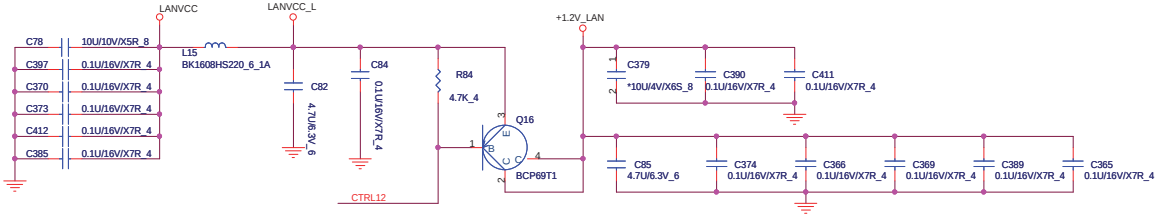


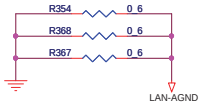






	ASM	No ASM
Use BIOS	R89	R90, R88,U2
EEPROM	R90, R88,U2	R89





PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN(Marvell 88E8057)	1A

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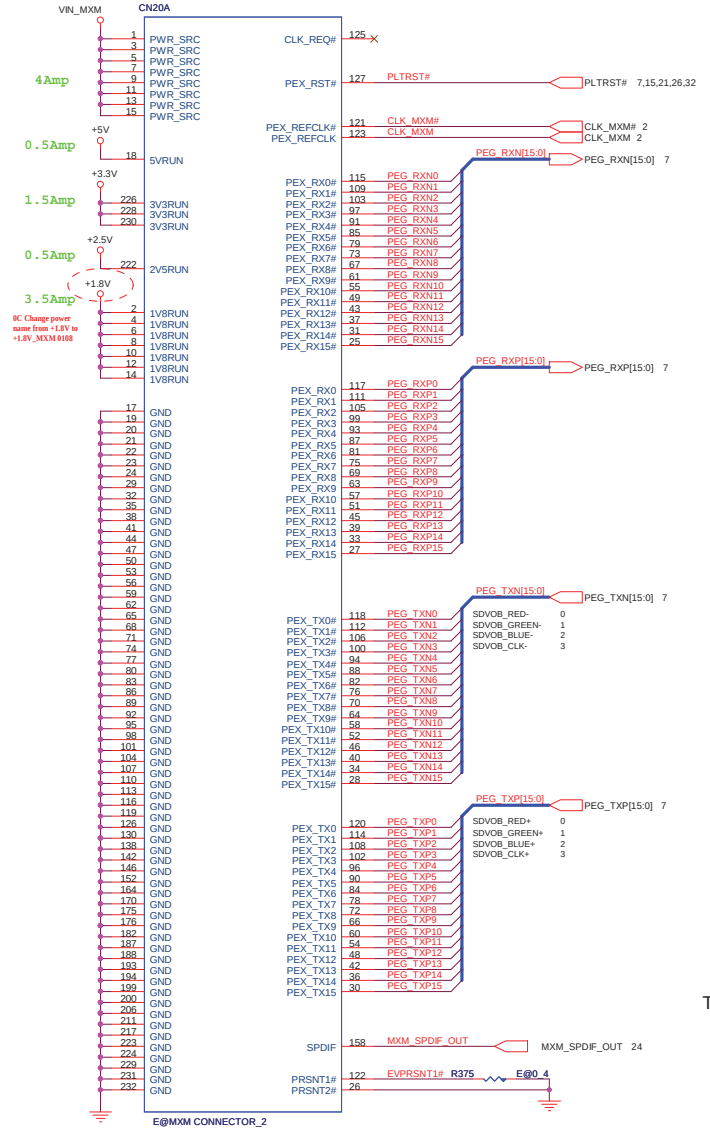

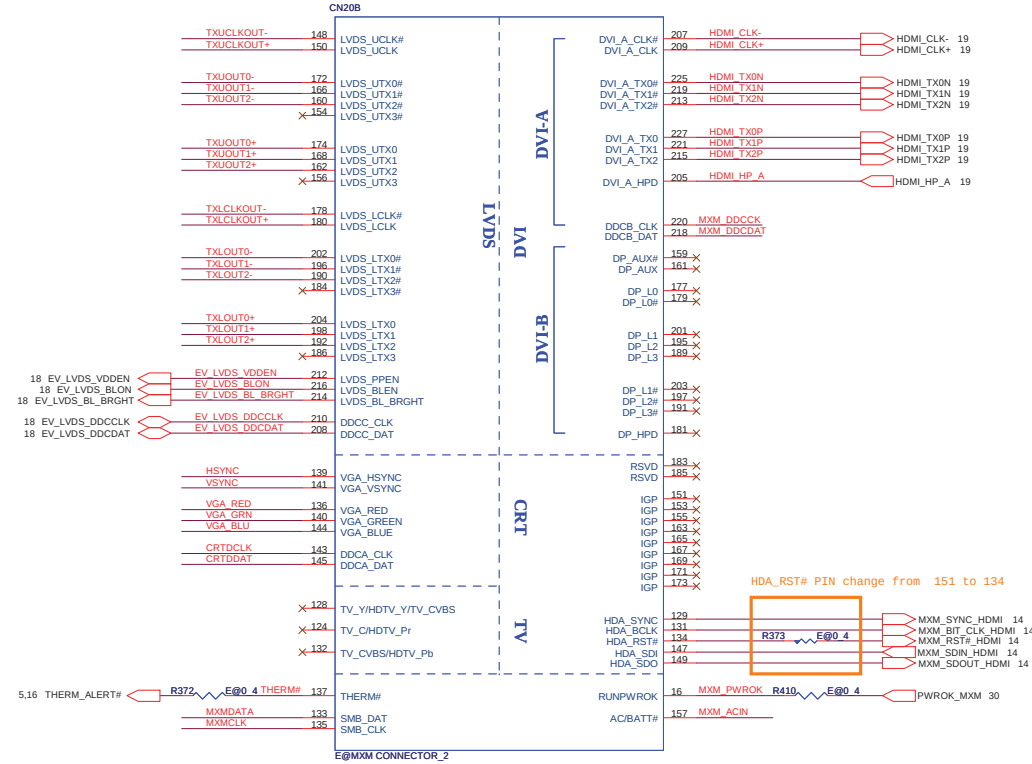

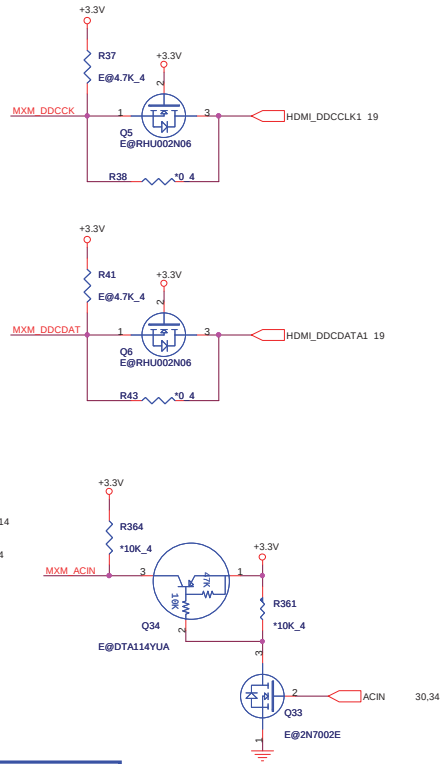

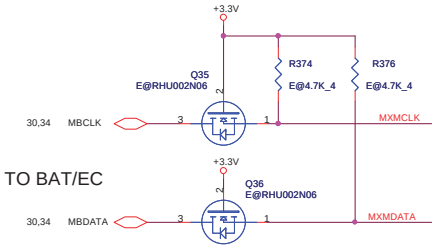

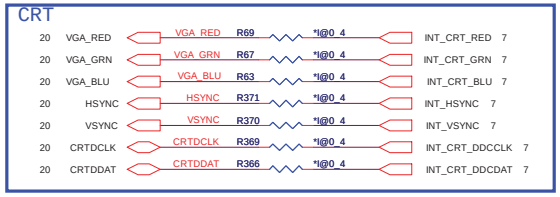

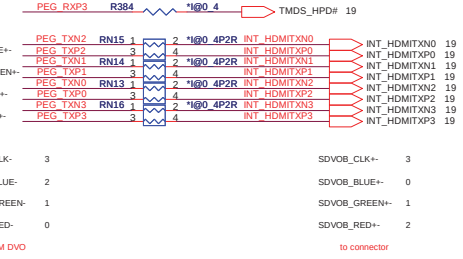

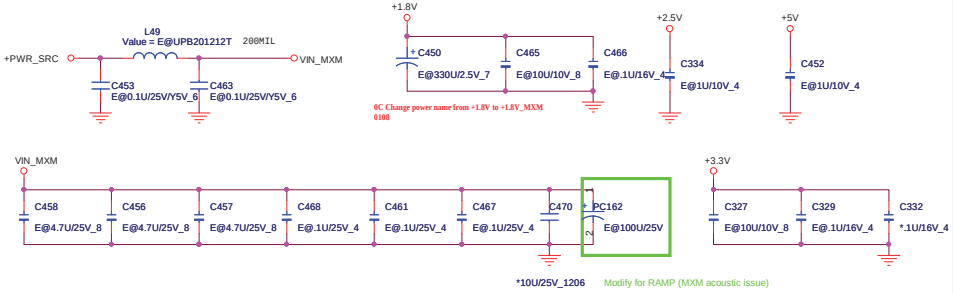

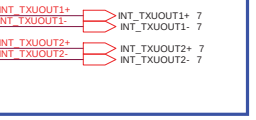

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	MXM	1A
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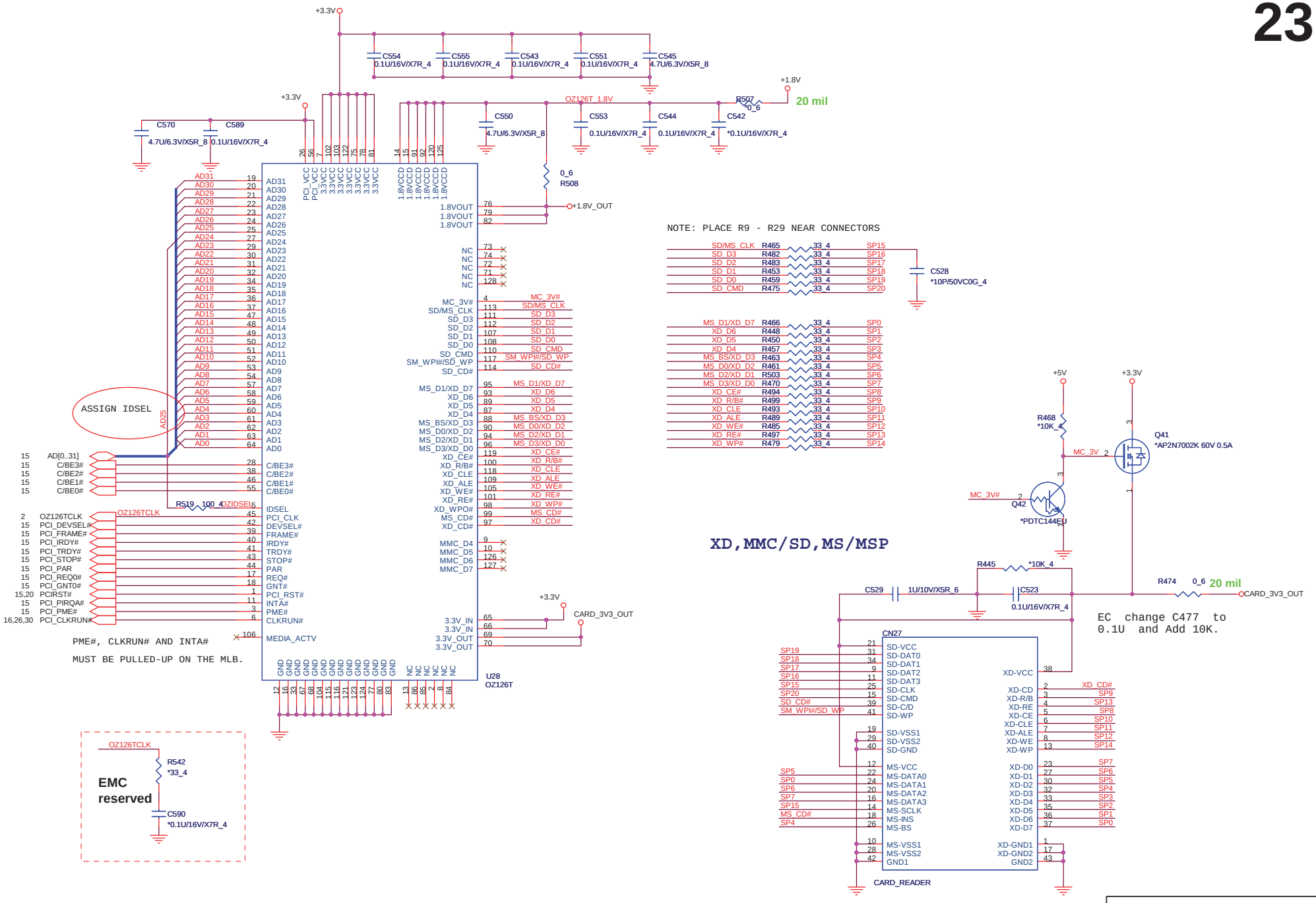

PROJECT : AJ2			
Quanta Computer Inc.			
Size: Custom	Document Number: OZ126T(CARD READER)		Rev: 1A
Date: Tuesday, September 16, 2008		Sheet 23	of 43

AUDIO CODEC

CX20561

PC Beep GAIN CONTROL

GAIN	GPIO1	GPIO2
0dB	10K	10K
-6dB	omit	omit
-12dB	10K	omit
-18dB	omit	omit

add pin 49 for QFN 8/21

PC BEEP

Change to correct size 0603

Change correct footprint to 0402

Int. Stereo Speakers

Modify for C-TEST

EXT. Mic in

Modify for FAI

Normal Close

Headphone out + Spdif Out

EMC reserved

Modify for FAI

Modify for C-TEST

Normal Open

AUDIO AMPLIFIER

TPA6017A2/FAN7031/LM4874

AUDIO JACK

Modify for FAI

Modify for C-TEST

Normal Close

6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

Place close U29

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO(CX20561)&CONN	1A

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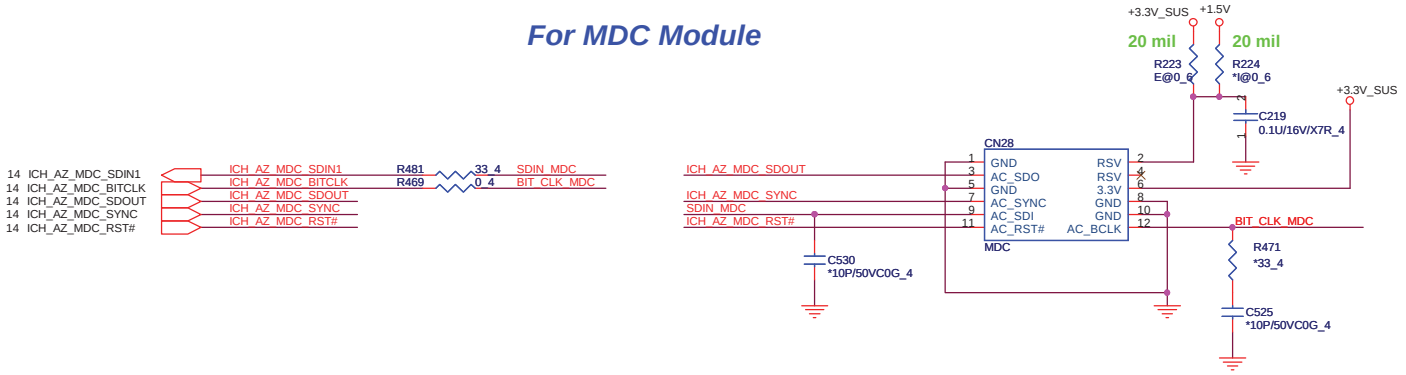
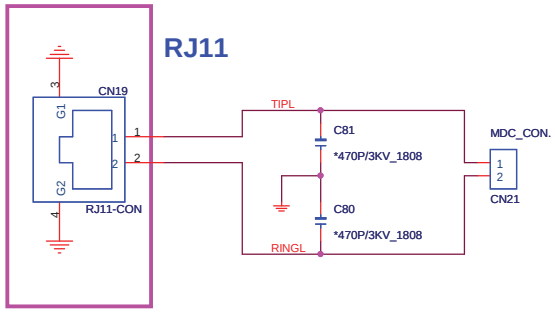
For MDC Module



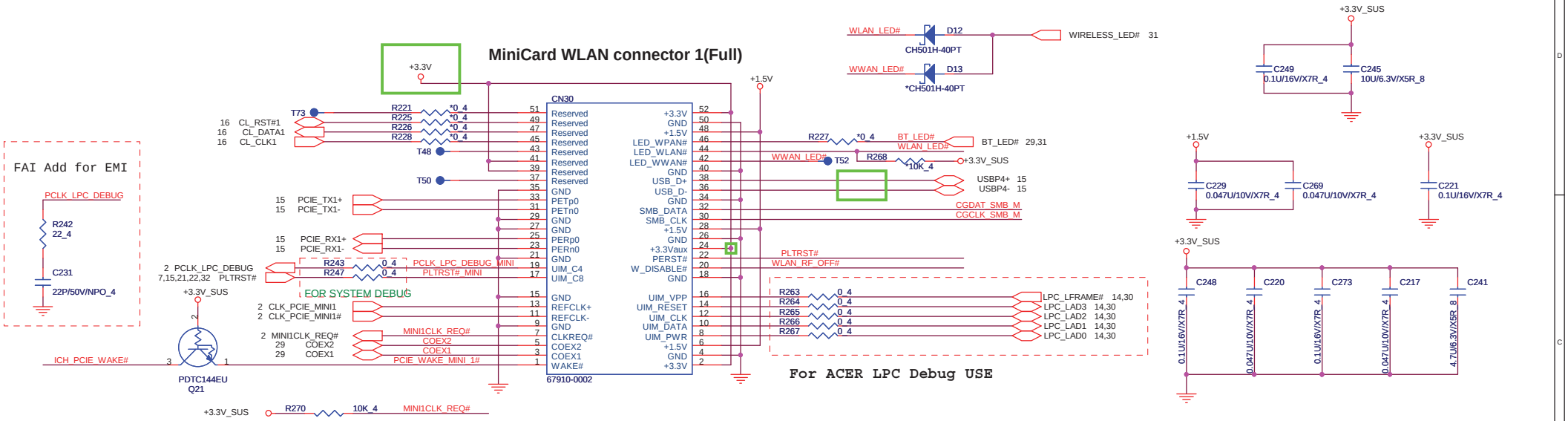
Change P/N



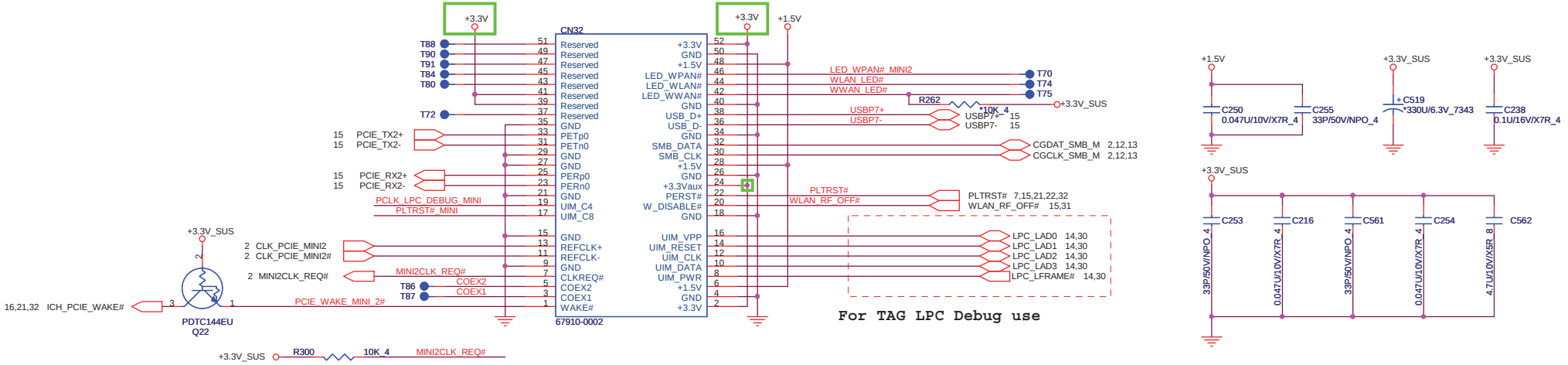
PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MODEM(MDC)/RJ11 BOARD	1A
Date: Tuesday, September 16, 2008	Sheet 25	of 43

MiniCard WLAN connector 1(Full)



MiniCard connector 2 (half)

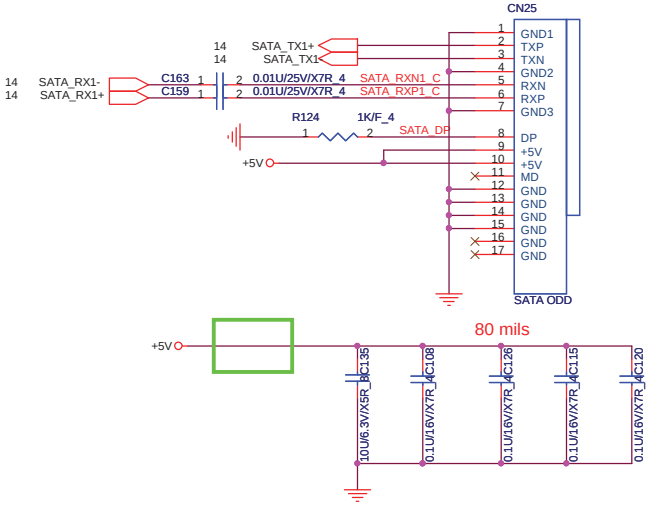


PROJECT : AJ2

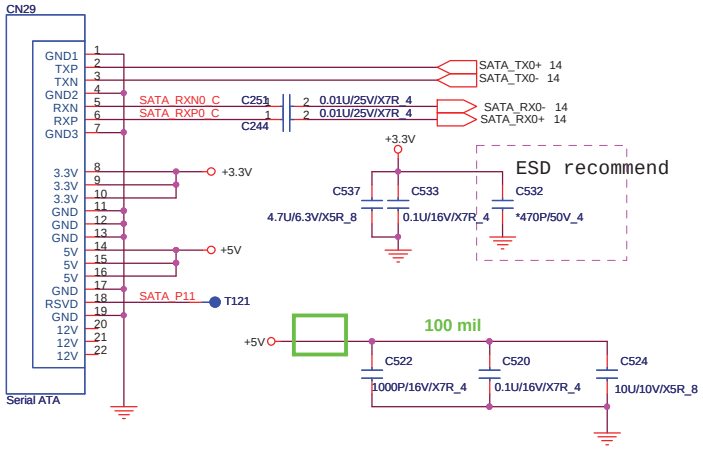
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI PCI-E Card	1A
Date: Tuesday, September 16, 2008	Sheet 26	of 43

SATA CD-ROM



SATA CONNECTOR



PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDD ODD	1A

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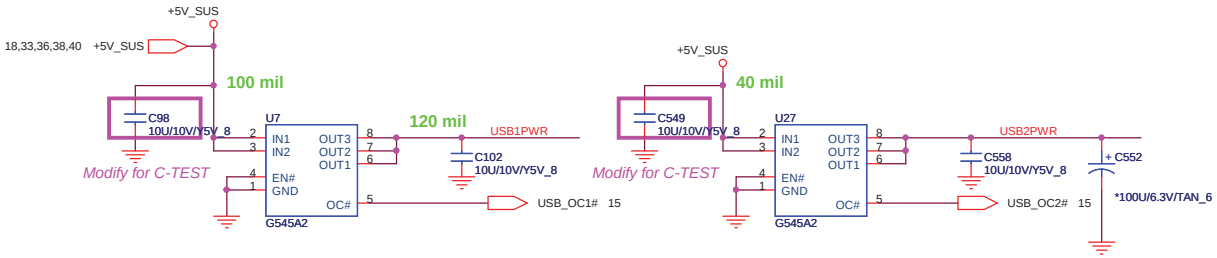

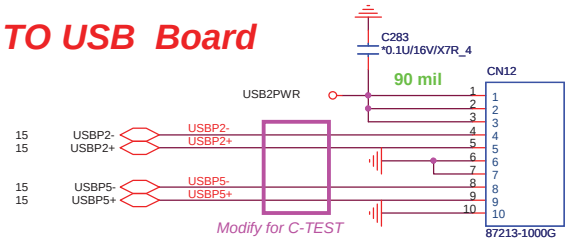

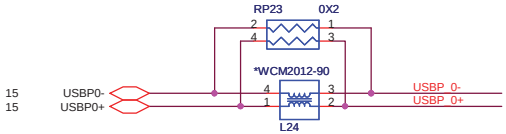

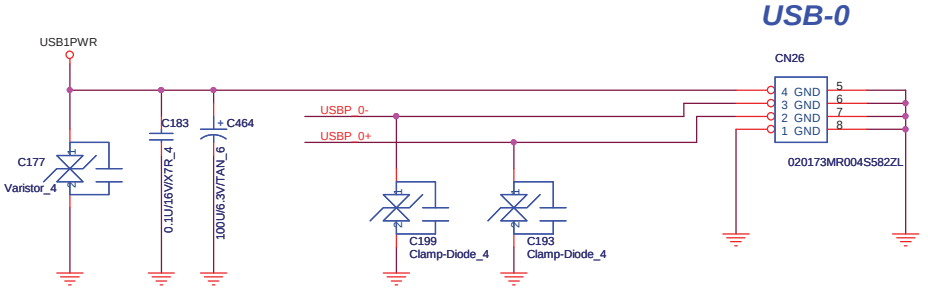

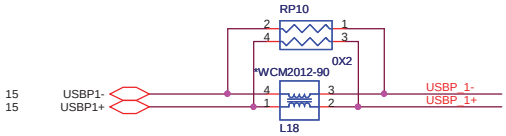

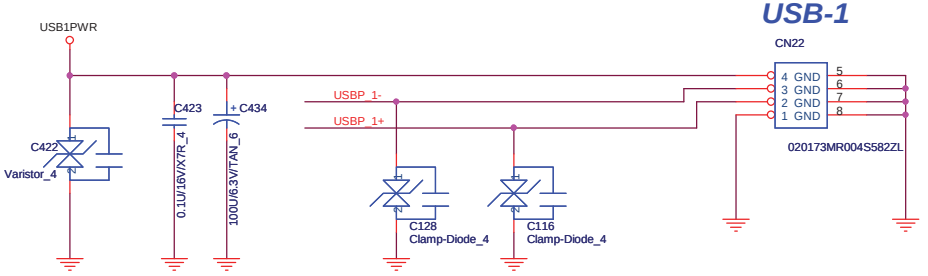

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	USB CONN	1A
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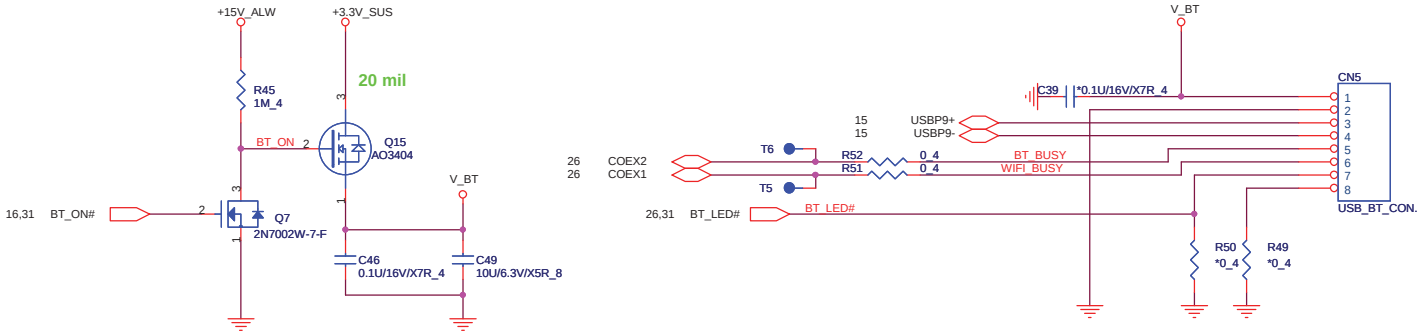
BLUETOOTH CONNECTOR



PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BT	1A

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IT8502

POWER SWITCH

Didital Mic & Light Sensor

16Mbit (2M Byte), SPI

TO MMB/ THM

TO BAT/MXM

ESD recommend

EMC reserved

(For PLL Power)

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

TMKBC Function	
High	Enable
Low	Disable

R3444	FLASH TYPE SELECT
High	LPC/FWH FLASH ROM
Low	SPI FLASH ROM (Default)

	R580	C631	C632
For IT8502IX	0 OHM	Remove	Remove
For IT8502JX	Remove	0.1uF	Remove

EC The same as SA6 Add R580,C631,C632 for ITE8502JX use.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

Layout Note:
Place R226,R205,R210 within 500 mils from SPI Flash.

Modify for C-TEST

Modify for F VERSION

*ORANGE LED

ORANGE LED

CLOSE TO SW1

Power ON S/W

The ID is for M/B rev: E, LED behavior

E@G9091-330T11U(SOT23-5)

W25X16VSSIG

PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KBC-IT8502	1A

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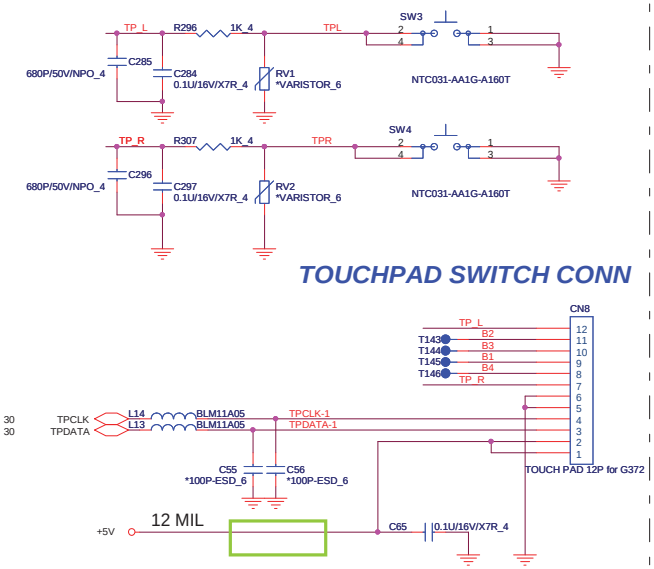
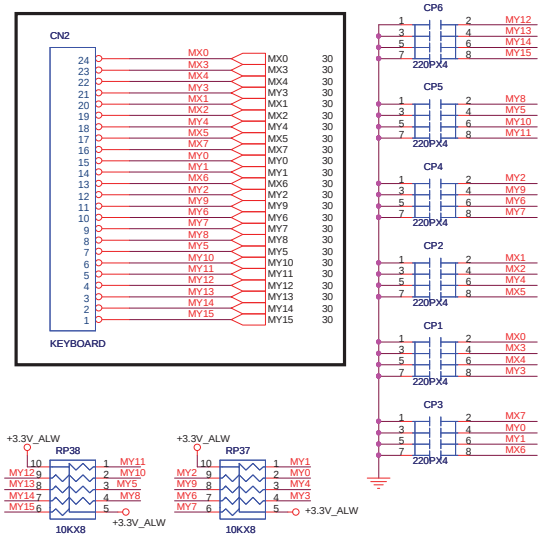
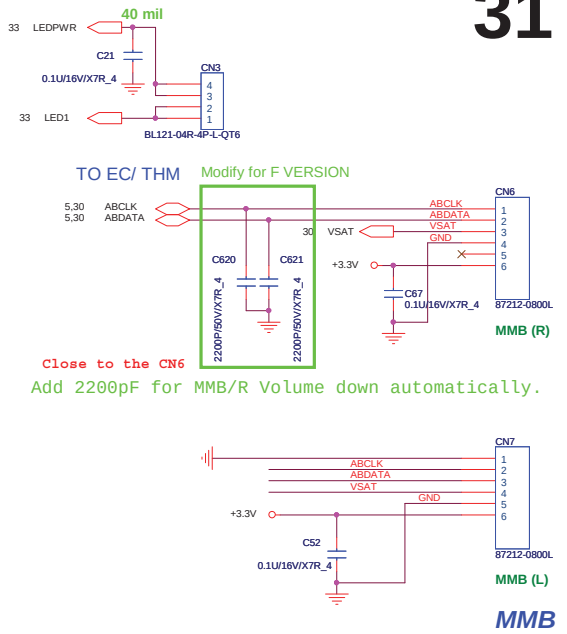
TOUCHPAD SWITCH CONN



KEYBOARD
For New Keyboard use.

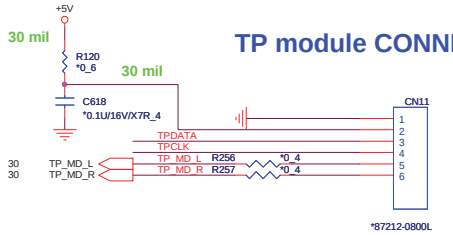


LED Power

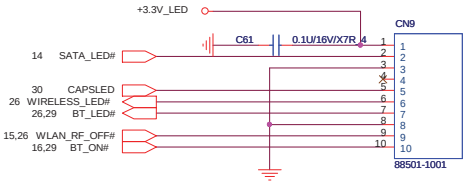


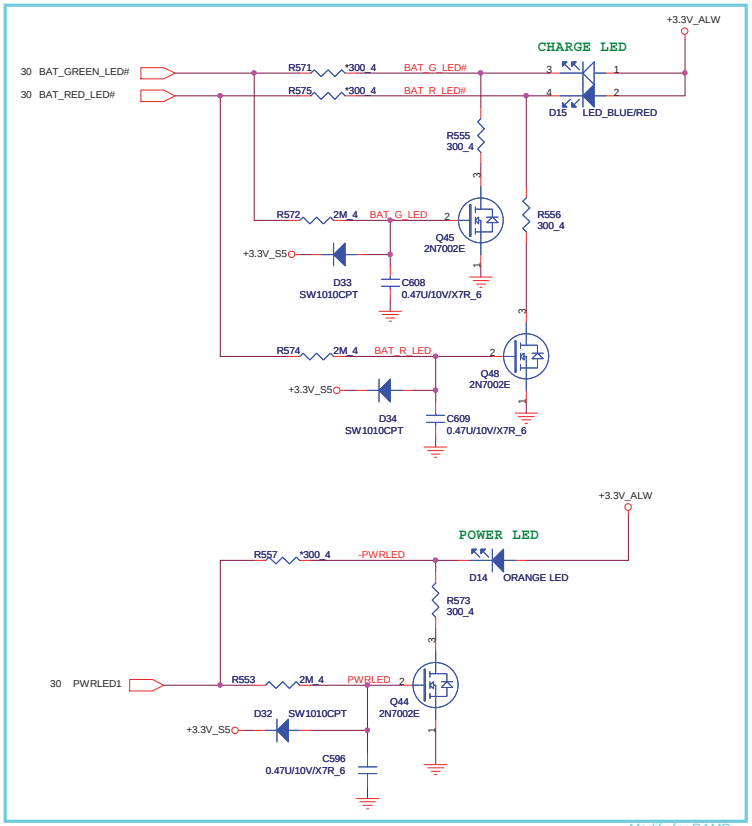
MMB

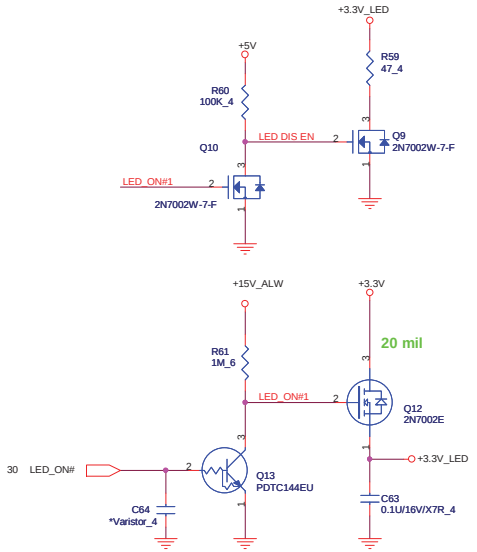
TP module CONNECTOR



To LED board







PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TP/KB/LED/MMB	1A
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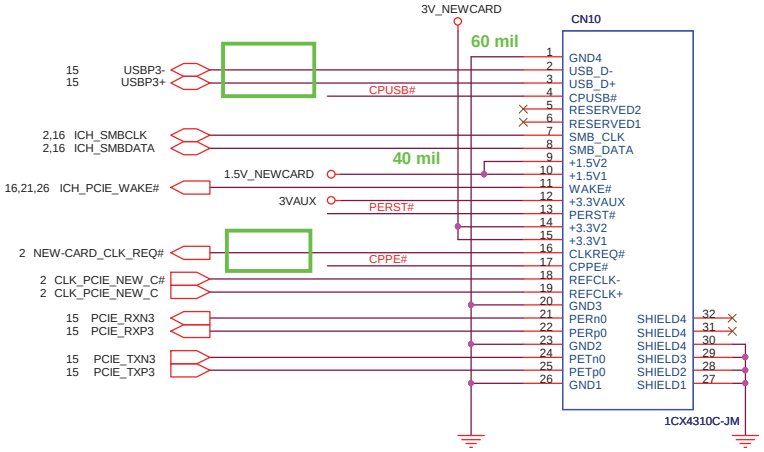
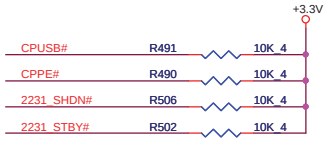
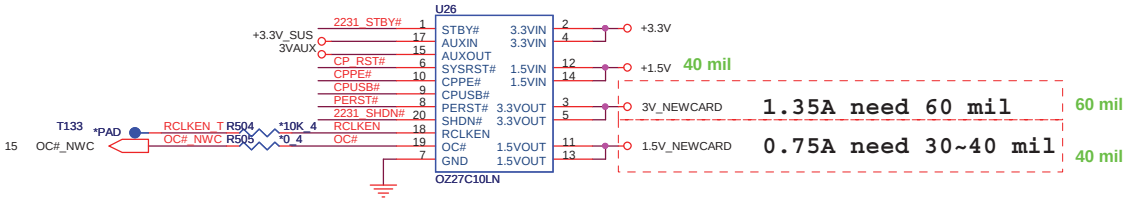
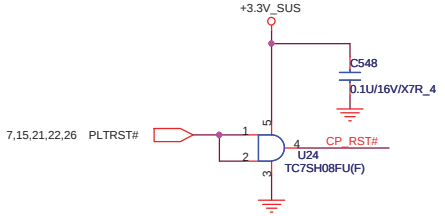
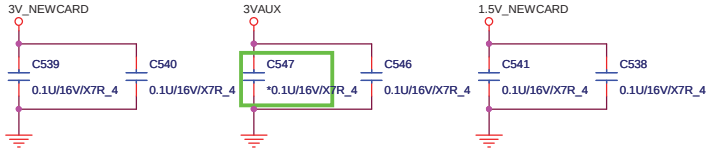
NEWCARD











PROJECT : AJ2
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD	1A
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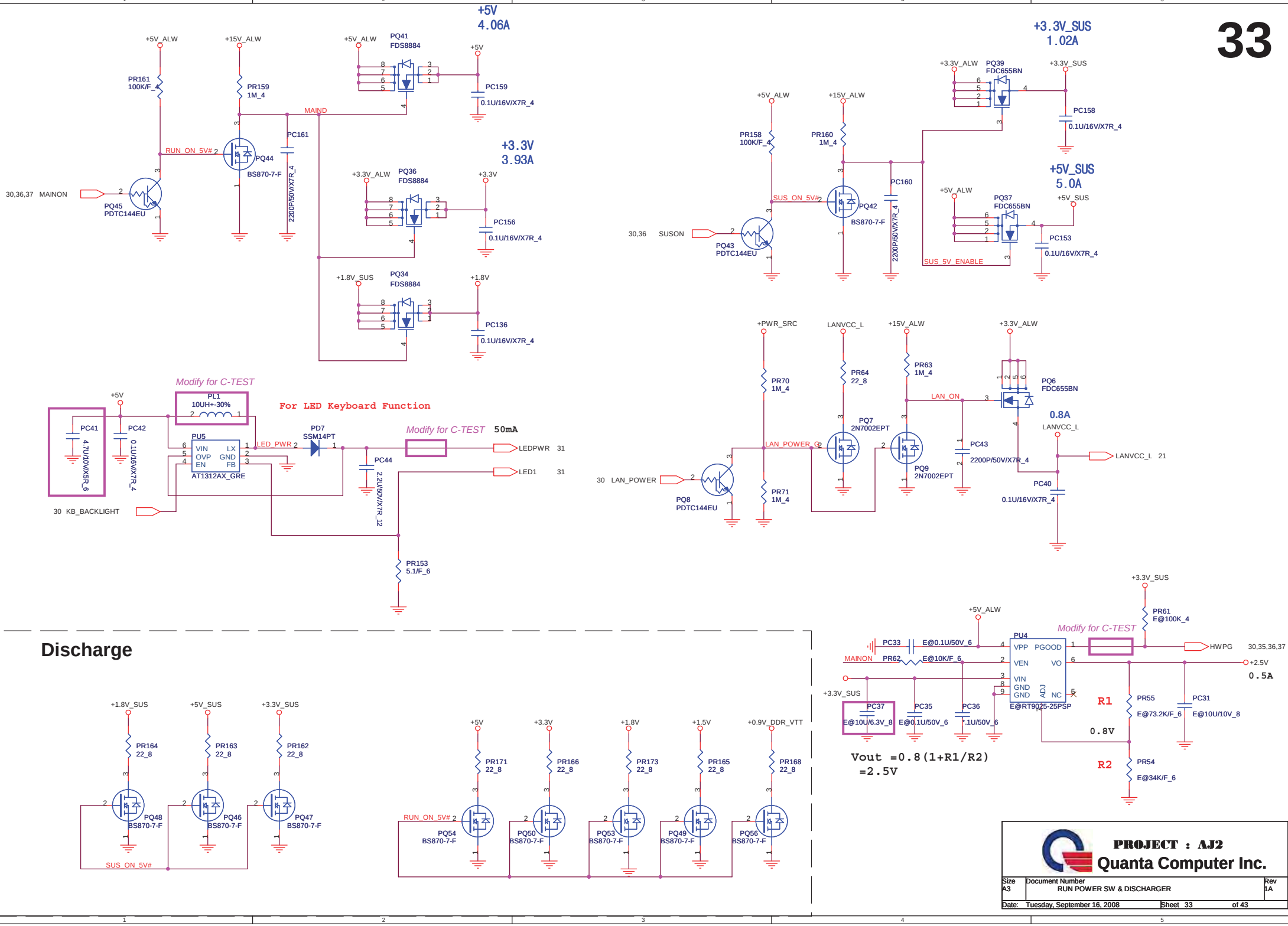

Discharge

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
A3	RUN POWER SW & DISCHARGER	1A
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90W P/N:DFPJ05MR006
65W P/N:DFPJ05MR007

PJ1 DCJK-2DC-G756-X06-5P-H
SP@POWER_JACK
PF1 LITTLE-7A-1206
PL4 UPB201212T
PL5 UPB201212T
PD10 PDS1040-13
PD11 P4SMAJ20A
PR87 RL3720WT-R020
PR1 *0_4
PQ1 *IMD2
PC1 *0.1U/50V_6
PR3 *200K/F_6
PQ2 PDTA124EU
PQ15 FDD6685_NL
PC69 1U/25V_8
PR130 10K_6
PR2 *0_4
PC70 0.1U/50V_6
PR4 *200K/F_6
PR7 *0_4
PR33 10K/F_4
PQ23 PDTA124EU
PR31 15K/F_4
PC96 1U/25V_8
PQ24 DMN601K-7
PD13 1N4148WS-7-F
PR108 1M/F_6
PR22 2_6
PR21 20_6
PC97 0.1U/50V_6
PC105 2.2U/10V/X5R_8
PR117 4.7_6
PC101 4.7U/10V_8
1N4148WS-7-F PD3
PR23 2_2_6
PC15 0.22U/25V_6
PQ21 SI4800BDY
PL12 UPB201212T
PC86 0.1U/50V_6
PC87 220P/50V/X7R_4
PC7 10U/25V_12
PC88 10U/25V_12
PR9 *33K/F_6
PR8 *0_4
PR6 200K/F_6
PR10 *10K/F_6
PR5 100K/F_6
PQ3 *DMN601K-7
PQ14 FDD6685_NL
PC2 0.1U/50V_6
PR104 20_6
PR105 20_6
PC17 0.047U/25V_4
PR95 RL3720WT-R030
PL11 10UH 30% 4.4A
ER4 2_2_6
EC15 2200P/50V/X7R_6
PQ16 SI4800BDY
PC89 10U/25V_1206
PC90 10U/25V_1206
PC91 0.1U/50V_6
1N4148WS-7-F PD4
PR32 10_6
PC21 0.1U/50V_6
PR128 100K/F_4
PR127 100K/F_4
PR129 12.4K/F_4
PR126 20K/F_4
PR119 11K/F_6
PR118 *514K_6
PR133 29.4K/F_6
PR132 *514K_6
PU1 ISL6251A
PR131 100K/F_4
PD15 CH501H-40PT
PQ28 DMN601K-7
PR123 *100/F_6
PC107 *1U/25V_6
PC113 *0.1U/16V_6
PR122 *475K/F_6
PR136 *10K/F_4
PQ30 DMN601K-7
PU8 *G1331
PR135 0_6
PC112 *100P/50V_4
PR134 *332K/F_6
PR137 *10K/F_4
PQ29 *DMN601K-7
PR115 100K_4
PC110 6800P/50V_4
PR125 10K/F_4
PC109 100P/50V_4
PC115 0.01U/50V_4
PR124 *100_4
PC114 *3300P/50V_4
PC108 100P/50V_4
PR116 0_4
PQ26 DMN601K-7
PR152 100K/F_6
PC132 0.01U/50V/X7R_6
PR154 14K/F_6
PR14 10K/F_4
PD16 RB500V-40
PR40 *0_6
PC4 0.1U/16V/X7R_4
PL8 UPB201212T
PL10 UPB201212T
PF2 BUS-10A-1206
BAT_CONN
CN15
PR13 200/F_4
PR12 200/F_4
PD2 UDZSV6B-7-F
PD1 UDZSV6B-7-F

Modify for C-TEST
Float = 4.2V / CELL
ACLIM : 65W/ 3.22A --> 0.629V
CC-SET : 6 CELLS/ 2.5A --> 1V
9 CELLS/ 3A --> 1.212V
CELL-SET = Hi ---->4S
CELL-SET = Low ---->3S
Place close to EC,
TO EC/MXM

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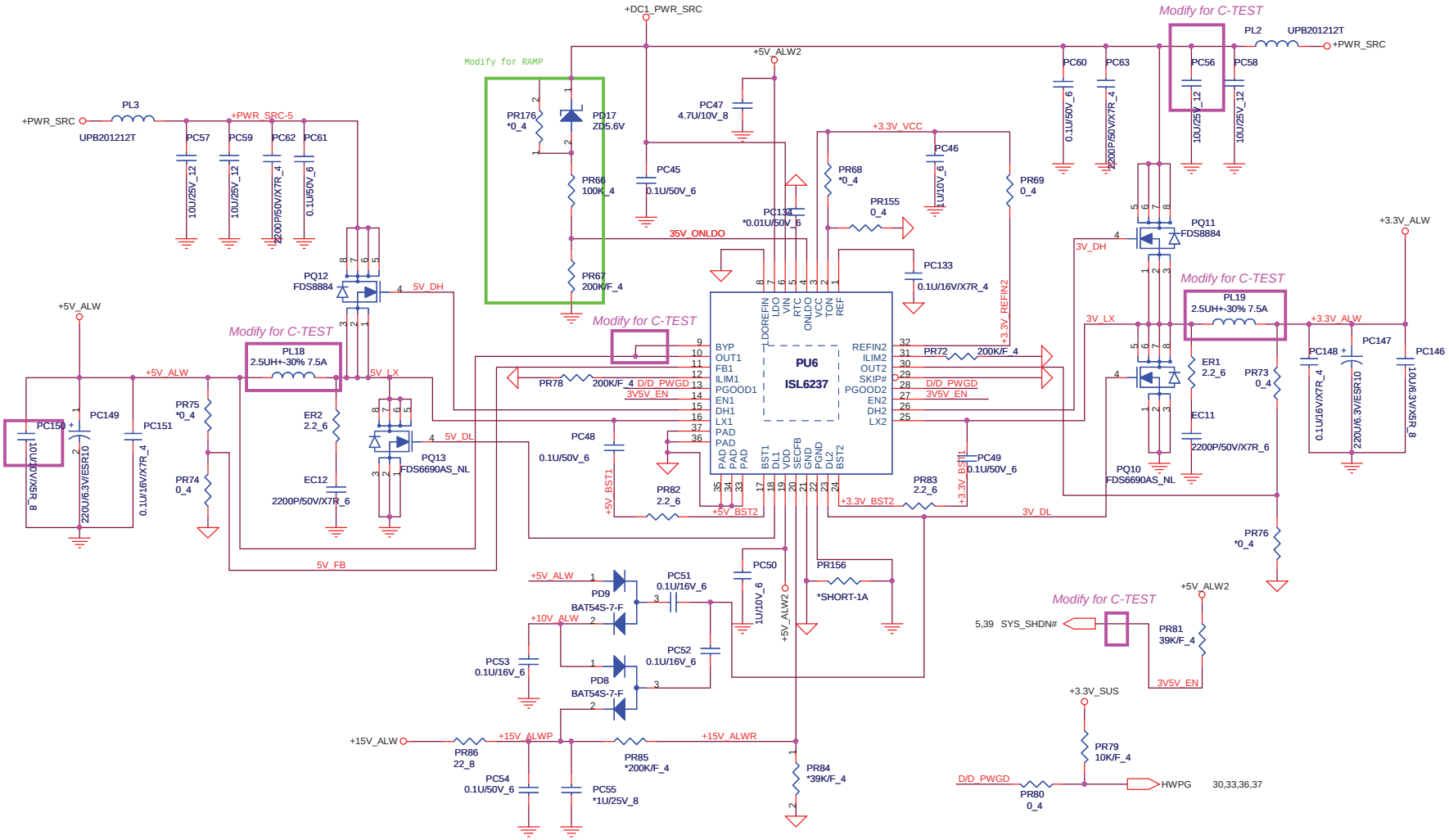
EC C-7 /8 Stuff PC56.



PROJECT : AJ2

Quanta Computer Inc.

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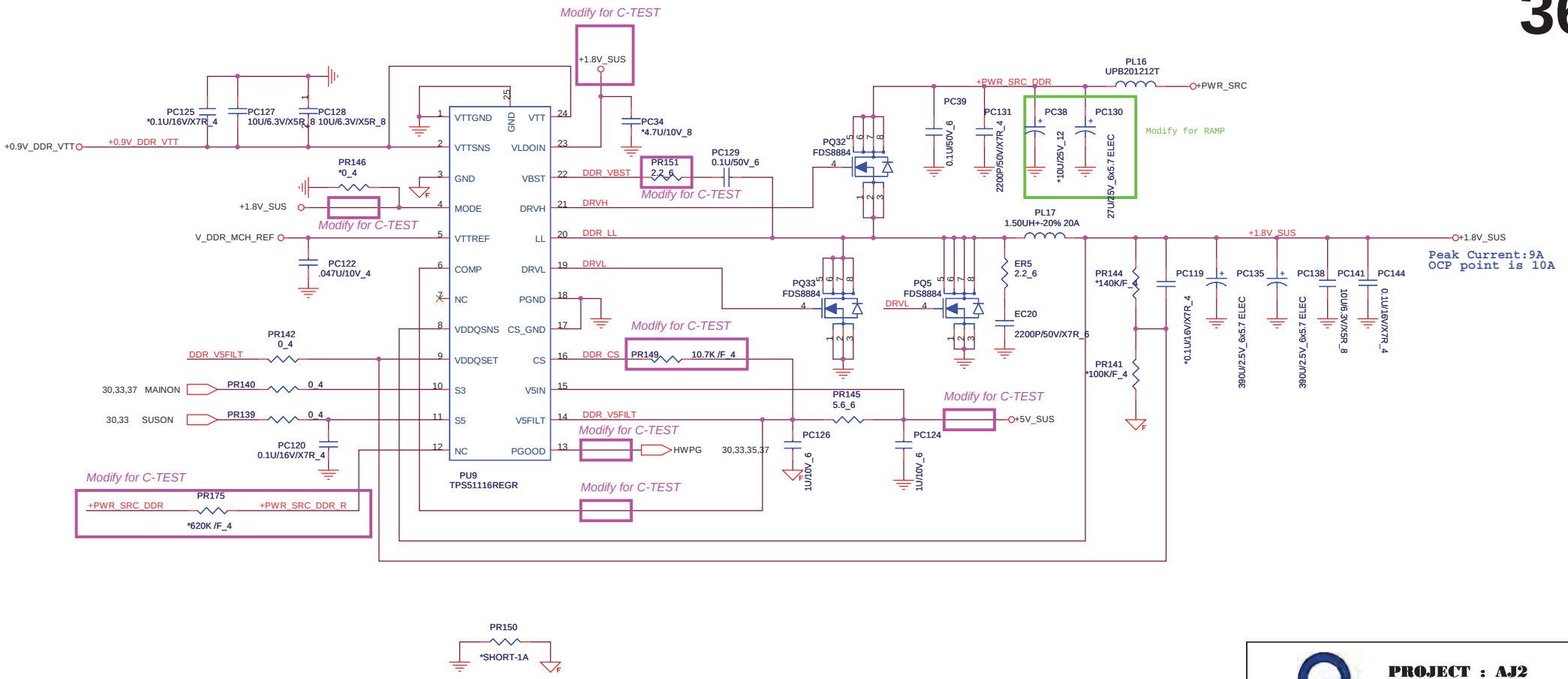

PROJECT : AJ2

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2_1.8VSUS,0.9V	1A
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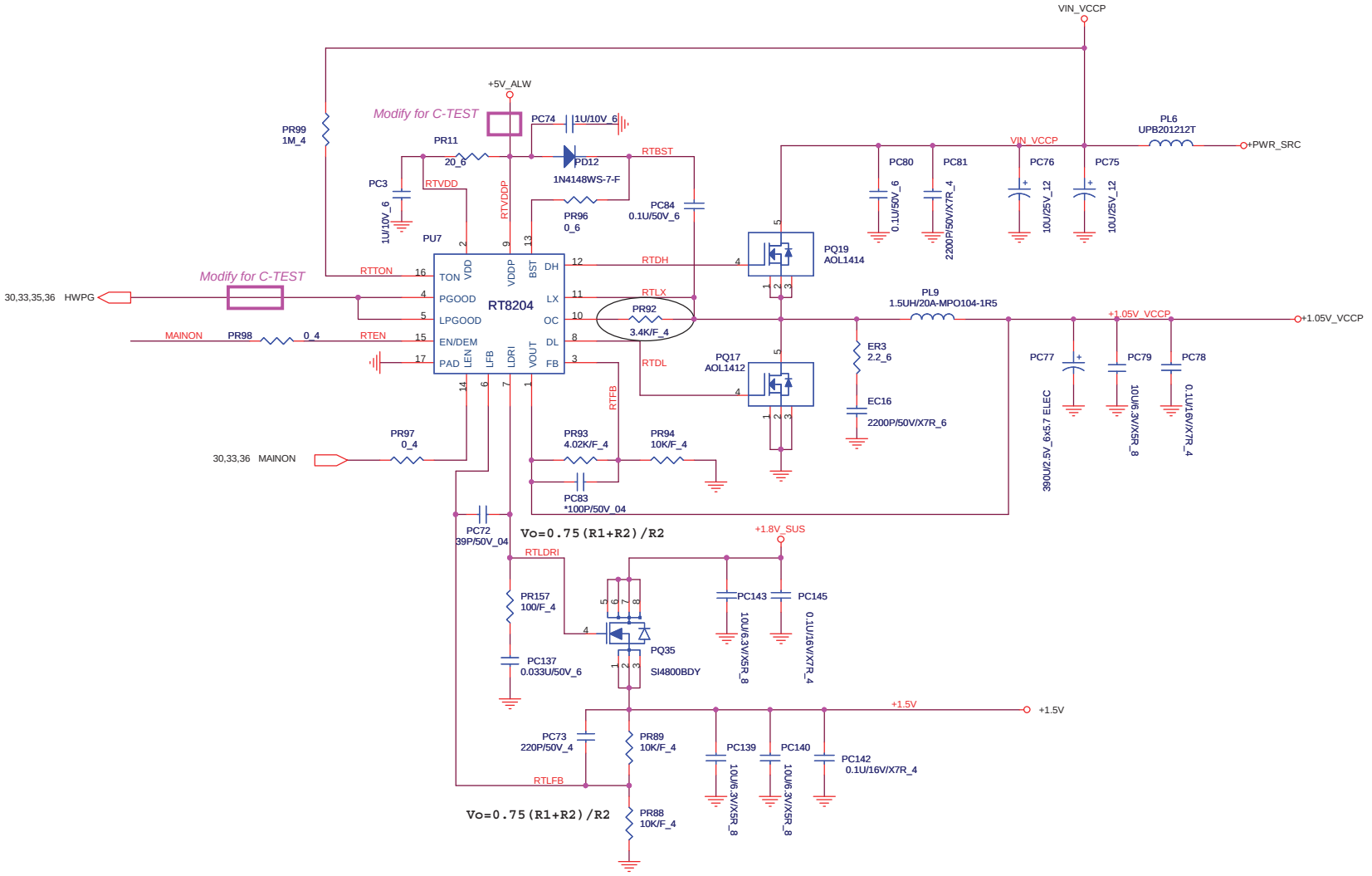

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Custom	+1.5v&1.05V	1A

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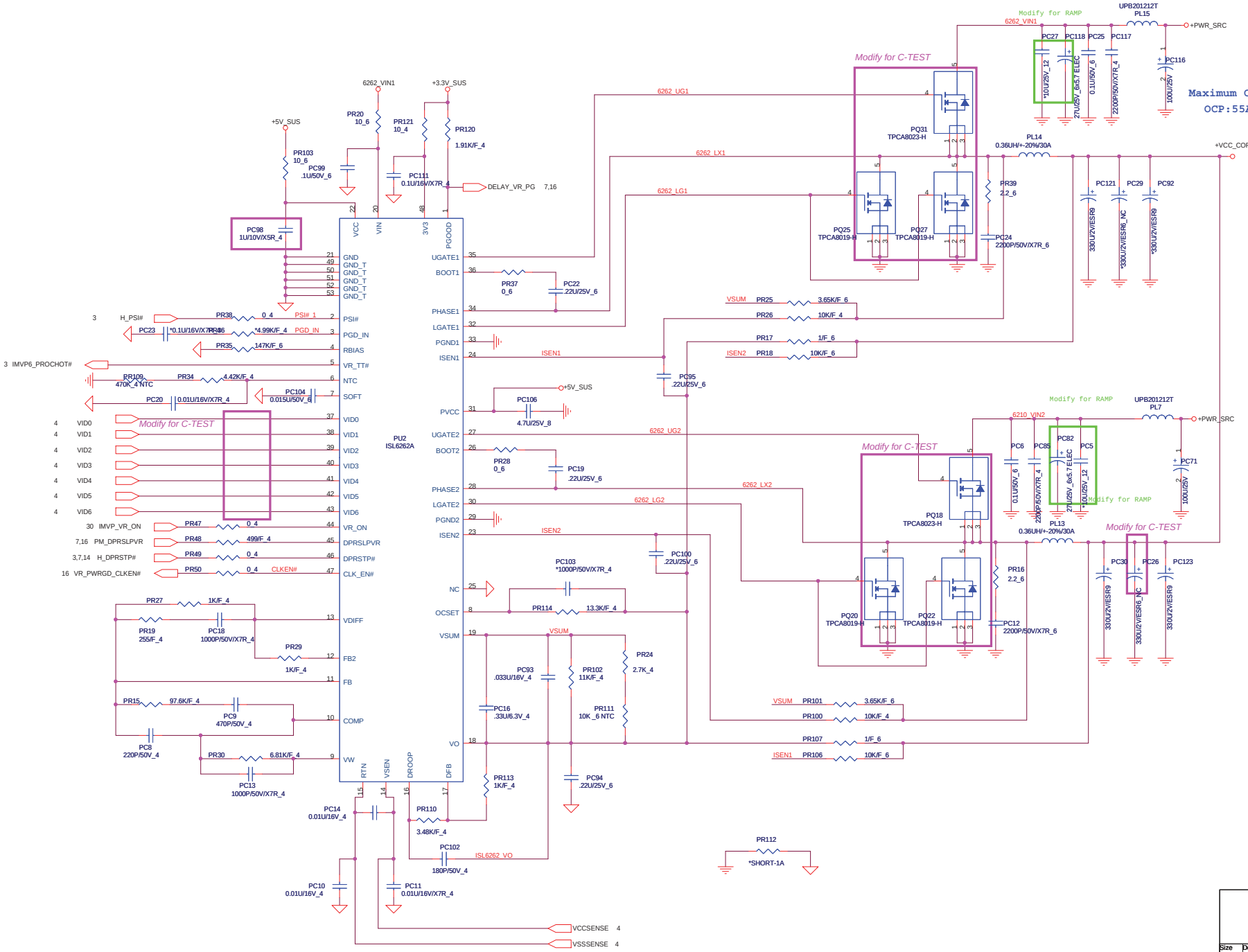
Maximum Current: 44A
OCP:55A
Modify for C-TEST
Modify for RAMP
PU2
ISL6262A
UPB201212T
PL15
PL14
0.36UH/+-20%/30A
PL13
PL7
PQ31
TPCA8023-H
PQ25
TPCA8019-H
PQ27
TPCA8019-H
PQ18
TPCA8023-H
PQ20
TPCA8019-H
PQ22
TPCA8019-H
+PWR_SRC
+VCC_CORE
+5V_SUS
+3.3V_SUS
6262_VIN1
6210_VIN2
6262_UG1
6262_LG1
6262_LX1
6262_UG2
6262_LG2
6262_LX2
ISEN1
ISEN2
VSUM
ISL6262_VO
DELAY_VR_PG 7,16
H_PSI#
PSI# 1
PGD_IN
PM_DPRSLPVR 7,16
H_DPRSTP# 3,7,14
VR_PWRGD_CLKEN# 16
IMVP_VR_ON 30
IMVP6_PROCHOT# 3
CLKEN#
VCCSENSE 4
VSSSENSE 4
*SHORT-1A
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Rev 1A
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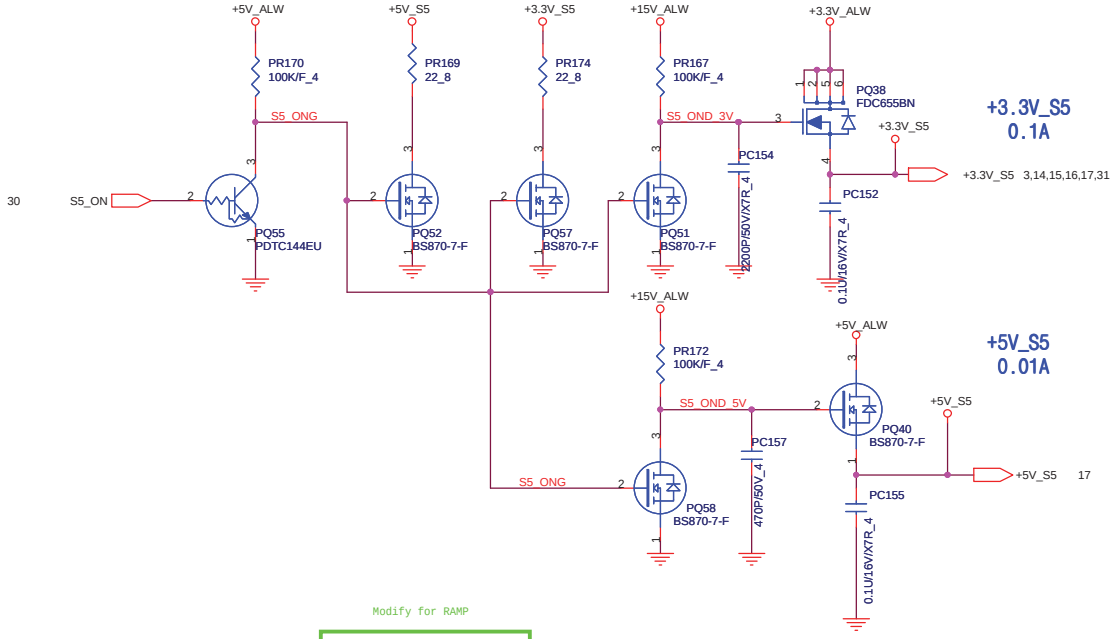

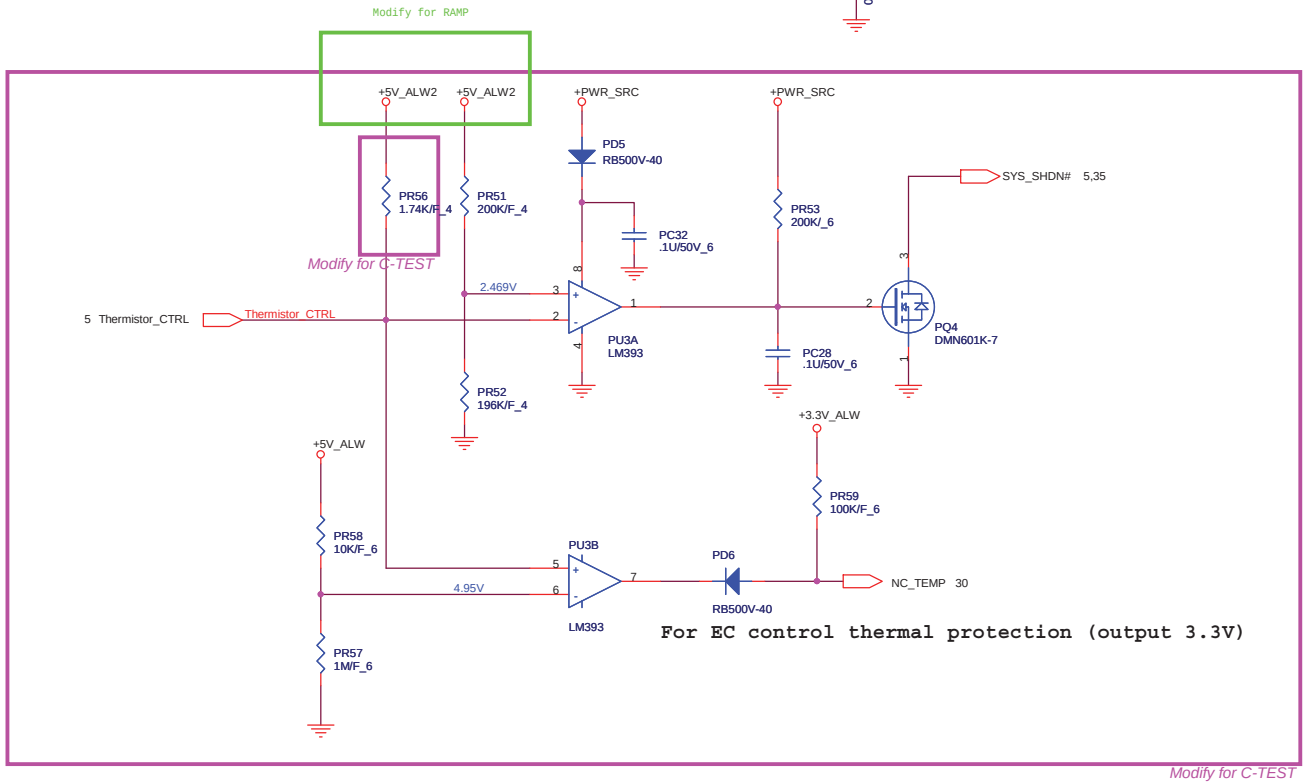

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A-Type H-C315D102P2

HOLE2 *H-C315D110P2

HOLE30 *H-C315D110P2

B-Type H-C315D118P2 *12 PCS.

HOLE20 *H-C315D118P2

HOLE3 *H-C315D118P2

HOLE19 *H-C315D118P2

HOLE33 *H-C315D118P2

HOLE34 *H-C315D118P2

HOLE15 *H-C315D118P2

HOLE4 *H-C315D118P2

HOLE9 *H-C315D118P2

HOLE22 *H-C315D118P2

HOLE32 *H-C315D118P2

C-Type H-TC315D169P1

CPU SCREW HOLE

HOLE8 *h-c236d169i209p2

HOLE13 *h-c236d169i209p2

HOLE14 *h-c236d169i209p2

HOLE7 *h-c236d169i209p2

for wirless wire

HOLE5 *H-C295D295N

for MXM NUT*4

HOLE11 E@H-C236D142P2

HOLE12 E@H-C236D142P2

HOLE16 E@H-C236D142P2

HOLE17 E@H-C236D142P2

for MDC NUT*2

HOLE28 H-C236D142P2

HOLE24 H-C236D142P2

for NB UNT

HOLE23 H-TC169BC236D142P2

Modify for C-TEST

HOLE1 H-TC169BC236D142P2

HOLE6 H-TC169BC236D142P2

Add new hole boss

HOLE21 h-c276d118p2

for Mini PCIE NUT*4

HOLE29 H-TC160BC236D142P2

HOLE27 H-TC160BC236D142P2

HOLE25 H-TC160BC236D142P2

HOLE26 H-TC160BC236D142P2

HOLE10 E@H-C236D142P2

HOLE18 E@H-C236D142P2

Full

Half

EMI Use

+5V_SUS

EC7 0.1U/16V/X7R_4

EC19 0.1U/16V/X7R_4

EC22 0.1U/16V/X7R_4

EC24 0.1U/16V/X7R_4

+3.3V_ALW

EC8 0.1U/16V/X7R_4

EC23 0.1U/16V/X7R_4

EC21 0.1U/16V/X7R_4

+1.05V_VCCP

EC10 0.1U/16V/X7R_4

EC6 0.1U/16V/X7R_4

+15V_ALW

EC5 0.1U/25V_4

EC13 0.1U/25V_4

EC9 0.1U/25V_4

+PWR_SRC

+1.05V_VCCP

EC1 1000P/50V/X7R_4

EC4 1000P/50V/X7R_4

EC2 1000P/50V/X7R_4

EC3 1000P/50V/X7R_4

MODEM

PAD1 FDBF1006

Modify for C-TEST

Power JACK ESD PAD

PAD2 CON1_10

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EC A06 page7 R154,R157 Change HSYNC,VSYNC value form 30.1 to 24.9/F
EC A08 page7 R418 Change LVDS_IBG value form 24K/F to 2.4K/F
EC A07 page7 R159 Change CRTIREF value form 75/F to 1K/F
EC A03 page9 Modify to*E@0_6 R91,R93 for UMA BOM .
EC A04 page16 Add R544,R561 for LCD GPIO fucction use!.
EC A19.page18 Change R344,345 value from 0 ohm to 1K ohm for lid S/W function .
EC A19.page18 ADD L11 Del R46,R47 for EC Backlight control function .
EC A04 page19 Del R341,D6 for HDMI LEVEL SHIFT use!.
EC A17.page19 Modify to correct net,ADD RN18 for MXM HDMI SCH.
EC A17.page21 Change Value to 75_6 (R40,358,359,360,362) ;C379 change to 10uf/4v.
EC A10 page22 C457,C468 Modify to *E@XX for UMA BOM.
EC A16.page22 Modify to correct net for UMA HDMI SCH.
EC A14.page25 Del C80,C81 CAP. for MDC RJ11 BOM.
EC A01 page28 USB CONN CN22,CN26 PIN define USB +-data swape it.
EC A05 page28 Change C102,C558 value&footprint 10U/10V_0805 (CH6102M9A01)
EC A12 page30 Del R120,R121 FOR Change the SMBus from 117 & 118 to 115 & 116 .
EC A02 page30 Modify LAN_DISABLE#_0 form pin68 to pin56.
EC A11 page31 Modify CN8 SCH. for TUCHPAD G372 PIN Define.
EC A15.page31 Modify MMB(L) CN7.Pin6 net TO GND .
EC A18.page31 Del. T/P module CONNECTOR SCH .
EC A20 page31 Modify LED POWER CONN. CN3 PIN define .
EC A09 page37 PR93 Change value from 4.7K/F to 4.02K/F for +1.05V use.
EC A13.page40 Del Hole11,12,16,17 MXM NUT for UMA BOM.

B-test to C-test EC list

1.EC page2 _Remove 0 ohm resistance array(RP18,RP19,RP20,RP21,RP29,RP22,RP28,RP27,RP26,RP25).

2.EC page7 _Remove R89,R86 and NET(PLTRST#_R).

3.EC page10 _Change L56,L57 to R560,R559.

4.EC page15 _Not stuff U10,C257,R251,R293,R252,R253,R294,R295.

5.EC page17 _Not stuff U22,C510,R446,R431,C514 for MXM.

6.EC page18 _Remove 0 ohm resistance L10.

7.EC page18 _Modify LCD Connector's pin definition(PIN37 from GND to NC).

8.EC page19 _Change R322 value form 100K/F to 20K/F.

9.EC page21 _Not stuff U5,R77,R80 ; stuff R83.

10.EC page21 _Change R358,R359,R360,R362,R40 footprint from 0603 to 0805.

11.EC page21 _Change C25 value from 1500pF to 1000pF(same as C66).

12.EC page24 _Modify SPEAKER Connector's pin definition(mirror).

13.EC page24 _Change C298,C305,C304,C302,C303 footprint from 0603 to 0402.

14.EC page28 _Remove 0 ohm resistance array RP32,RP33.

15.EC page28 _Change C98,C549 value from 22uF to 10uF.

16.EC page30 _Add R552(1k) and R121(*10k) to pull low and pull high.

17.EC page30 _Remove R122(10k) and net EC_GPB7.

18.EC page30 _Change R1,R2(*),R3(*) value from 150 ohm to 300 ohm.

19.EC page31 _Modify MMB Connector's pin definition(mirror:CN6,CN7).

20.EC page31 _Modify LED Display circuit.

21.EC page33 _Change PL1 value from 22UH to 10UH.

22.EC page33 _Remove 0 ohm resistance PR65,PR60.

23.EC page34 _Change PL11's part number to CV01044TZ01.

24.EC page34 _Add PD16 and PR40(*) on BAT CON's pin3 to avoid leakage current.

25.EC page34 _Change PR95 part number to CS+0308FL00.

26.EC page34 _Change PR133 value from 11k/F ohm to 29.4k/F ohm .

27.EC page34 _Change PR119 value from 16k/F(MXM) or 75K/F(UMA) ohm to 11k/F(MXM) or 178K/F(UMA) ohm .

28.EC page35 _Change PL19 and PL18 part number to CV-2575TZ04.

29.EC page35 _Short PU6 pin9 and pin10.

30.EC page35 _Remove 0 ohm resistance PR77.

31.EC page35 _Stuff PC56.

32.EC page36 _Remove 0 ohm resistance PR147,PR148,PR138,PR143.

33.EC page36 _Modify PU9 pin23's net from +1.8V_SUSP to +1.8V_SUS.

34.EC page36 _Add PR175(*) connect to PU9 pin12 and pull high to +PWR_SRC_DDR(buffer).

35.EC page36 _Change PR149 value from 14k/F ohm to 10.7k/F ohm.

36.EC page36 _Change PR151 value from 0 ohm to 2.2 ohm.

37.EC page37 _Remove 0 ohm resistance PR90,PR91.

38.EC page38 _Remove 0 ohm resistance PR40,PR41,PR42,PR43,PR44,PR45,PR46.

39.EC page38 _Change PQ31 and PQ18 part number to BAM80230000.

40.EC page38 _Change PQ25,PQ27,PQ20,PQ22 part number to BAM80190000.

41.EC page38 _Change PC26 part number to CH733RM8874.

42.EC page39 _Stuff PR51,PR52,PR53,PR56,PR57,PR58,PR59,PC28, PC32,PD5, PD6,PQ4,PU3 for EC control thermal protection.

43.EC page40 _Change HOLE23's NUT to FBAJ2003010.

44.EC page40 _Add SPRING PAD1 to fix MODEM's cable.

C-test to FAI list

1.EC page2 _Change C188,C189 value form 30P to 27P for RCT timing.
2.EC page2 _Change UAM BOM add original RP24 for LVDS spread spectrum clock issue.
3.EC page16 _Change BOARD_ID0 resister to pull low. (remove R201 and add R202).
4.EC page16 _Add C612 0.1uF/16v_4 near R27810/F_4 fix RTC CMOS checksum error.
5.EC page18 _Add PD18 Close to LCD CONN. CN1 fix U2 break down .
6.EC page18 _Del. USB8+- data remove the RP1&L8;Del. R32 0 ohm.
7.EC page18 _Change value C325 from 0.1U/16V/Y5V to 0.1U/16V/X7R .
8.EC page24_ Change GND CN33,34,35 from ADO_GND to Digtal_GND for ESD solution.
9.EC page24_Add *C619 Varistor_0402 near R310 for ESD use.
10.EC page26_Change net CN30,32 name from +3.3v_sus to +3.3v .
11.EC page30_Del. R552 for EC change to"slowly pulse" detect pin use .
12.EC page30_Add +3.3V C54,C62 0.1UF/16V;C610,C611 100P/50V near CN4.
13.EC page30_Move the R539,R534 from 24 page to 30 page.
14.EC page31_Modify BOM to POWER,Charge LED bevhavior "solwly pulse" .
15.EC page26,27,31,32_Del. 0 ohm RP30,RP31,R230,R233,R254,R255,R229,L20,L59,L12,R569,R248 cost doown .
16.EC page22_ ADD PC162 100U/25V.
17.EC page35_ ADD PD17 ;Change value PR67 to 200K/F_4 PR66 to 100K/F_4.
18.EC page36_Change value PC130 to 27U/25V .
19.EC page38_Change value PC118 to 27U/25V .

20.EC page30_ ADD LDO(PU10) circuit to reduce DMIC noise.
21.EC page31_Add 2200pF(C620,C621) for MMB/R Volume down automatically issue.
22.EC page21_Change transformer's PCB footprint.