AJ6 SYSTEM DIAGRAM

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SVCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

DDRII-SODIMM1 PAGE 6,7 — DDRII 667/800 MHz

DDRII-SODIMM2 PAGE 6,7 — DDRII 667/800 MHz

AMD Griffin Lion Sabie
S1G2 Processor
638P (uPGA)/35W
PAGE 3,4,5

CPU THERMAL SENSOR PAGE 5

14.31818MHz

CLOCK GEN
SLG8SP628
PAGE 2

CPU_CLK
NBGFX_CLK
NBGPP_CLK
SBLINK_CLK
SBSRC_CLK

HT3

PCI-E

PCI-Express 16X

NORTH BRIDGE
RS780MN
29mm X 29mm, 528pin BGA
PAGE 8,9,10,11,

HDMI PAGE 18

CRT PAGE 20

LVDS PAGE 19

MXM CONN
PAGE 17

LAN
PCIE-LAN
MARVELL_88E8057
(10/100/GagaLAN)
PAGE 21

Express Card X1
(NEW CARD)
PAGE 30

Mini PCI-E Card
(Wireless LAN)
PAGE 25

RJ45 PAGE 21

PCIE X4

SOUTH BRIDGE
SB700
21mm X 21mm, 528pin BGA
4.5W(Ext)
4.3W(Int)
PAGE 12,13.14.15.16

SATA - HDD PAGE 24 — SATA0 300MB

SATA - ODD PAGE 24 — SATA4 300MB

USB2.0

7 Camera PAGE 19

1 Bluetooth PAGE 26

4,5 Mini PCI-E X2 PAGE 25

11 Express Card X1 (NEW CARD) PAGE 30

0,2,8,9 USB2.0 Ports X2 PAGE27

USB (small/B) X2 PAGE26

PCI BUS / 33MHz

CARD reader
OZ126T
PAGE 22

Azalia

CX20561
AUDIO CODEC
PAGE 23

MDC CONN
PAGE 26

RJ11
PAGE 26

AUDIO Amplifier
TPA6017A2
PAGE 23

AUDIO CONN
(Phone/ MIC)
PAGE 23

Speaker Conn.
PAGE 23

LPC

Keyboard PAGE 29
Touch Pad PAGE 29

KBC
ITE
IT8502
PAGE 28

FAN PAGE 28

SPI FLASH PAGE 28

SYSTEM CHARGER PAGE 31

SYSTEM POWER PAGE 32

DDR II SMDDR_VTERM
1.8V/1.8VSUS
PAGE 34

VCCP +1.2V & +1.1V
PAGE 33

CPU CORE +VCORE0 +VCORE1
PAGE 37

SMBUS TABLE		
SB--SCL0/SD0	Clock gen /DDR2/DDR2 thermal/Accelerometer	+3V
SB--SCL1/SD1	Wlan Card	+3V/S5
SB--SCL2/SD2	epress card	+3v/S5
EC --SCL/SD	Battery charge/discharge	+3VPCU
EC--SCL2/SD2	VGA thermal/system thermal	+3V

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

Date: Monday, August 18, 2008 | Sheet 1 of 39

CLOCKS name	UMA	RS780	Clock pin function
NBGFX_CLKP NBGFX_CLKN	RP64 STUFF	RP64 STUFF	to NB for VGA reference clock
EXT_GFX_CLKP EXT_GFX_CLKN	RP5053 NC	RP5053 STUFF	to M86-M external reference clock
NBGPP_CLKP NBGPP_CLKN	RP70 STUFF	RP70 NC	to NB for RX780 for PCIEX2 interface reference clock only RS780 is internal share with AC-LINK clock,RS780 not need
SBLINK_CLKP SBLINK_CLKN	RP72 STUFF	RP72 STUFF	to NB for AC-LINK reference clock

60 ohm, 0.5A
+1.2V
L43 BLM18PG221SN1D(220,1.4A)_6
600 ohms@100Mhz
C648 100P/50V/NPO_4
C532 10U/6.3V_8
C512 0.1U/10V/X5R_4
C515 0.1U/10V/X5R_4
C531 0.1U/10V/X5R_4
C513 0.1U/10V/X5R_4
C524 0.1U/10V/X5R_4
+1.2V_CLKVDDIO
EMI request. 18/08/2008
DCR: 0.5 ohm
600 ohms@100Mhz
+3V_CLKVDD
+3.3V
L45 BLM18PG221SN1D(220,1.4A)_6
60 ohm, 0.5A
C537 10U/6.3V_8
C516 0.1U/10V/X5R_4
C526 0.1U/10V/X5R_4
C538 0.1U/10V/X5R_4
C546 0.1U/10V/X5R_4
C547 0.1U/10V/X5R_4
C514 0.1U/10V/X5R_4
C530 0.1U/10V/X5R_4
C511 0.1U/10V/X5R_4

EMI reserved

U23
QFN64
SLG8SP628VTR
RELTAK AL000880001

+3V_CLKVDD
Place very close to C/G
L44 BLM18PG221SN1D(220,1.4A)_6
+3V_CLK_VDDA
C545 2.2U/6.3V/X5R_6
C552 0.1U/10V/X5R_4
+1.2V_CLKVDDIO

VDDDOT VDDSRC VDDATIG VDDSB_SRC VDDSATA VDDCPU VDDHTT VDDREF VDD48
VDDSRC_IO0 VDDSRC_IO1 VDDATIG_IO VDDSB_SRC_IO VDDCPU_IO
GND48 GNDDOT GNDSRC0 GNDSRC1 GNDATIG GNDSB_SRC GNDSATA GNDCPU GNDHTT GNDREF

C289 33P/50V/NPO_4 CG_XIN
Y2 14.318MHZ
C288 33P/50V/NPO_4 CG_XOUT
CG_XIN CG_XOUT X1 X2

(6,7,13) PCLK_SMB
(6,7,13) PDAT_SMB
PCLK_SMB PDAT_SMB SMBCLK SMBDAT
CLK_PD# PD#
(25) MINI1CLK_REQ#
(25) MINI2CLK_REQ#
(30) NEW-CARD_CLK_REQ#
CLKREQ0# CLKREQ1# CLKREQ2# CLKREQ3# CLKREQ4#
TGND0 TGND1 TGND2 TGND3 TGND4 TGND5 TGND6 TGND7 TGND8 TGND9

Place within 0.5" of CLKGEN

CPUK8_0T CPUK8_0C — RP51 — CPUCLK0P CPUCLK0N — R385 *261_4 — CPUCLKP CPUCLKN
ATIG0T ATIG0C ATIG1T ATIG1C — RP43 RP44 — NBGFXCLK0P NBGFXCLK0N EXTGFXCLK0P EXTGFXCLK0N
SB_SRC0T SB_SRC0C SB_SRC1T SB_SRC1C — RP48 RP42 — PCILANCLK0P PCILANCLK0N SBLINKCLK0P SBLINKCLK0N
SRC0T SRC0C SRC1T SRC1C SRC2T SRC2C SRC3T SRC3C SRC4T SRC4C — RP46 RP45 RP47 RP49 RP50 — PCIEMINICLK1P PCIEMINICLK1N PCIEMINICLK2P PCIEMINICLK2N NBGPPCLK0P NBGPPCLK0N PCIENEWCLK0P PCIENEWCLK0N SBSRCCLK0P SBSRCCLK0N
SRC6T/SATAT SRC6C/SATAC SRC7T/27M_SS SRC7C/27M_NS — CLK_VGA_27M_SS CLK_VGA_27M_NSS — T38 T37 T39 T113
HTT0T/66M HTT0C/66M — NBHTREFCLK0P NBHTREFCLK0N — R375 0_4 R374 0_4 — NBHT_REFCLKP NBHT_REFCLKN
48MHz_0 — CLK48MUSB — R363 33_4 — CLK_48M_USB
REF0/SEL_HTT66 REF1/SEL_SATA REF2/SEL_27 — SEL_HT66 SEL_SATA SEL_27

0_4P2R

CPUCLKP (3) CPUCLKN (3)
NBGFX_CLKP (10) NBGFX_CLKN (10) EXT_GFX_CLKP (17) EXT_GFX_CLKN (17)
PCIE_LAN_CLKP (21) PCIE_LAN_CLKN (21) SBLINK_CLKP (10) SBLINK_CLKN (10)
PCIE_MINI1_CLKP (25) PCIE_MINI1_CLKN (25) PCIE_MINI2_CLKP (25) PCIE_MINI2_CLKN (25) NBGPP_CLKP (10) NBGPP_CLKN (10) PCIE_NEW_CLKP (30) PCIE_NEW_CLKN (30) SBSRC_CLKP (12) SBSRC_CLKN (12)
NBHT_REFCLKP (10) NBHT_REFCLKN (10)
CLK_48M_USB (13)

C536 *10P/50VC0G_4

Ra R377 158/F_4
Rb R389 90.9/F_4
EXT_NB_OSC (10)

	RX780	RS780
	1.8V	1.1V
Ra	82.5R	158R
Rb	130R	90.9R

RES CHIP 130 1/16W +-1%(0402)L-F -->CS11302FB15
RES CHIP 158 1/16W +-1%(0402) -->CS11582FB00
RES CHIP 90.9 1/16W +-1%(0402) -->CS09092FB15
RES CHIP 82.5 1/16W +-1%(0402) -->CS08252FB11

Clock chip has internal serial terminations
for differential pairs, external resistors are
reserved for debug purpose.

+3V_CLKVDD
R171 8.2K_4
SEL_SATA
SEL_27
R175 *8.2K_4
R376 8.2K_4
RS780M/RX780M

+3.3V
CLK_PD#
R373 8.2K_4

* default

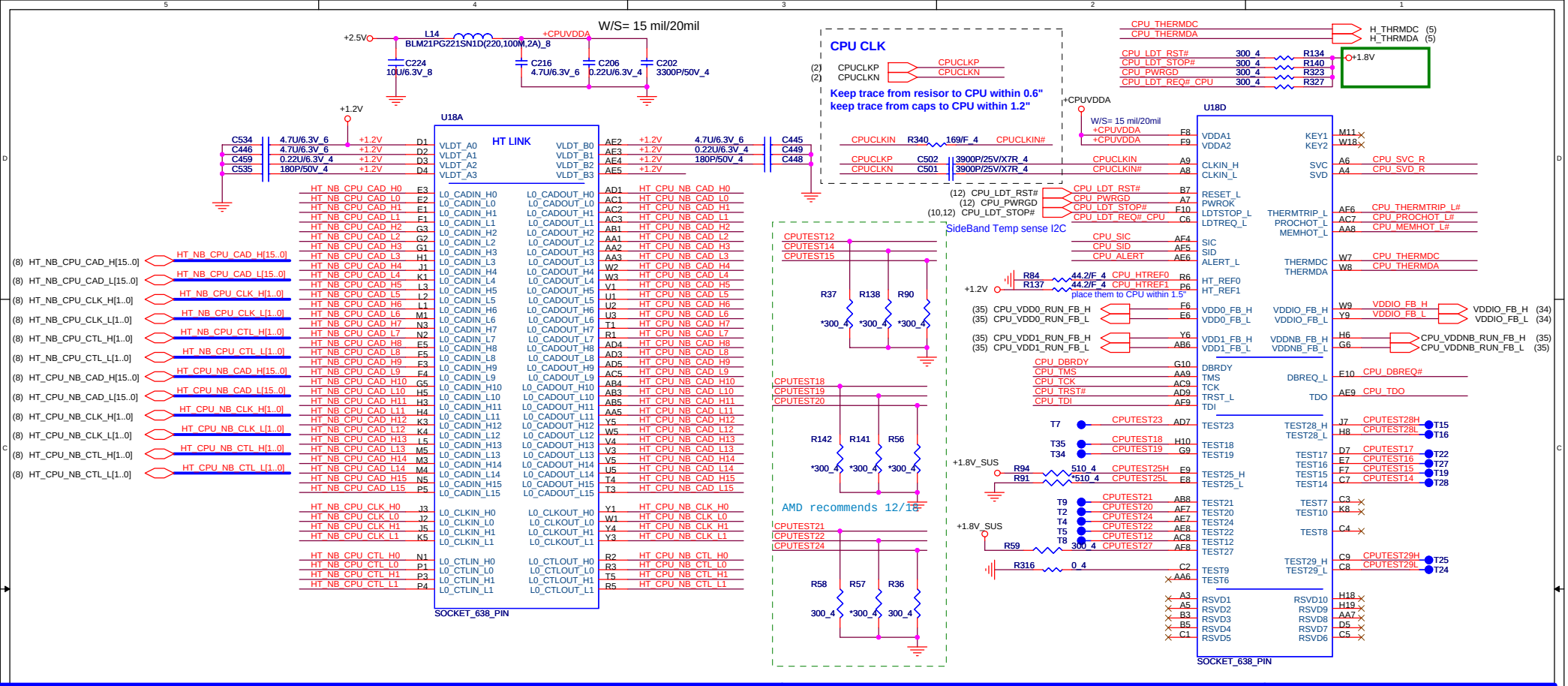
SEL_HTT66	1	66 MHz 3.3V single ended HTT clock
	0*	100 MHz differential HTT clock
SEL_SATA	1*	100 MHz non-spreading differential SRC clock
	0	100 MHz spreading differential SRC clock
SEL_27	1	27MHz and 27M SS outputs
	0*	100 MHz SRC clock

SLG8SP628VTR P/N : AL8SP628000
RTM880N-796 P/N : AL000880000

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Clock Gen	3B
Date: Thursday, August 21, 2008	Sheet 2 of 39	


W/S= 15 mil/20mil
L14
BLM21PG221SN1D(220,100M,2A)_8
+2.5V
+CPUVDDA
C224 10U/6.3V_8
C216 4.7U/6.3V_6
C206 0.22U/6.3V_4
C202 3300P/50V_4
+1.2V
U18A
HT LINK
SOCKET_638_PIN
CPU CLK
Keep trace from resisor to CPU within 0.6"
keep trace from caps to CPU within 1.2"
CPUCLKP
CPUCLKN
R340 169/F_4
C502 3900P/25V/X7R_4
C501 3900P/25V/X7R_4
SideBand Temp sense I2C
R37 R138 R90
R142 R141 R56
R58 R57 R36
AMD recommends 12/18
U18D
SOCKET_638_PIN
CPU_THERMDC
CPU_THERMDA
H_THRMDC (5)
H_THRMDA (5)
+1.8V
R84 44.2/F_4 CPU_HTREF0
R137 44.2/F_4 CPU_HTREF1
place them to CPU within 1.5"
CPU_DBRDY
CPU_TMS
CPU_TCK
CPU_TRST#
CPU_TDI
CPU_DBREQ#
CPU_TDO
R94 510_4 CPUTEST25H
R91 *510_4 CPUTEST25L
R59 300_4 CPUTEST27
R316 0_4
+1.8V_SUS
Serial VID
R326 *2.2K_4
R128 1K_4
R131 1K_4
R133 0_4
R130 0_4
R325 0_4
R132 *220_4
R129 *220_4
R322 *220_4
CPU_SVC
CPU_SVD
CPU_PWRGD_SVID_REG
VFIX MODE
VID Override Circuit
SVC SVD Voltage Output
0 0 1.4V
0 1 1.2V
1 0 1.0V
1 1 0.8V
HDT Connector
C504 0.1U/10V/X5R_4
R344 20K_4
R345 34.8K_4
CNTR_VREF
Q43 *BSS138_NL/SOT23
Q44 BSS138_NL/SOT23
R343 0_4
R342 1K_4
R341 0_4
G1 *SHORT_PAD1
for debug only
R42 10K_4
R43 300_4
Q8 MMBT3904
R38 10K_4
R39 300_4
Q7 MMBT3904
R40 10K_4
R41 300_4
Q9 MMBT3904
R53 390_4
R54 390_4
R55 1K_4
R139 300_4
CPU_SIC
CPU_SID
CPU_ALERT
CPU_DBREQ#
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size Custom
Document Number S1G2 HT,CTL I/F 1/3
Rev 1A
Date: Monday, August 18, 2008
Sheet 3 of 39

Processor Memory Interface

PLACE THEM CLOSE TO CPU WITHIN 1"

U18B — SOCKET_638_PIN

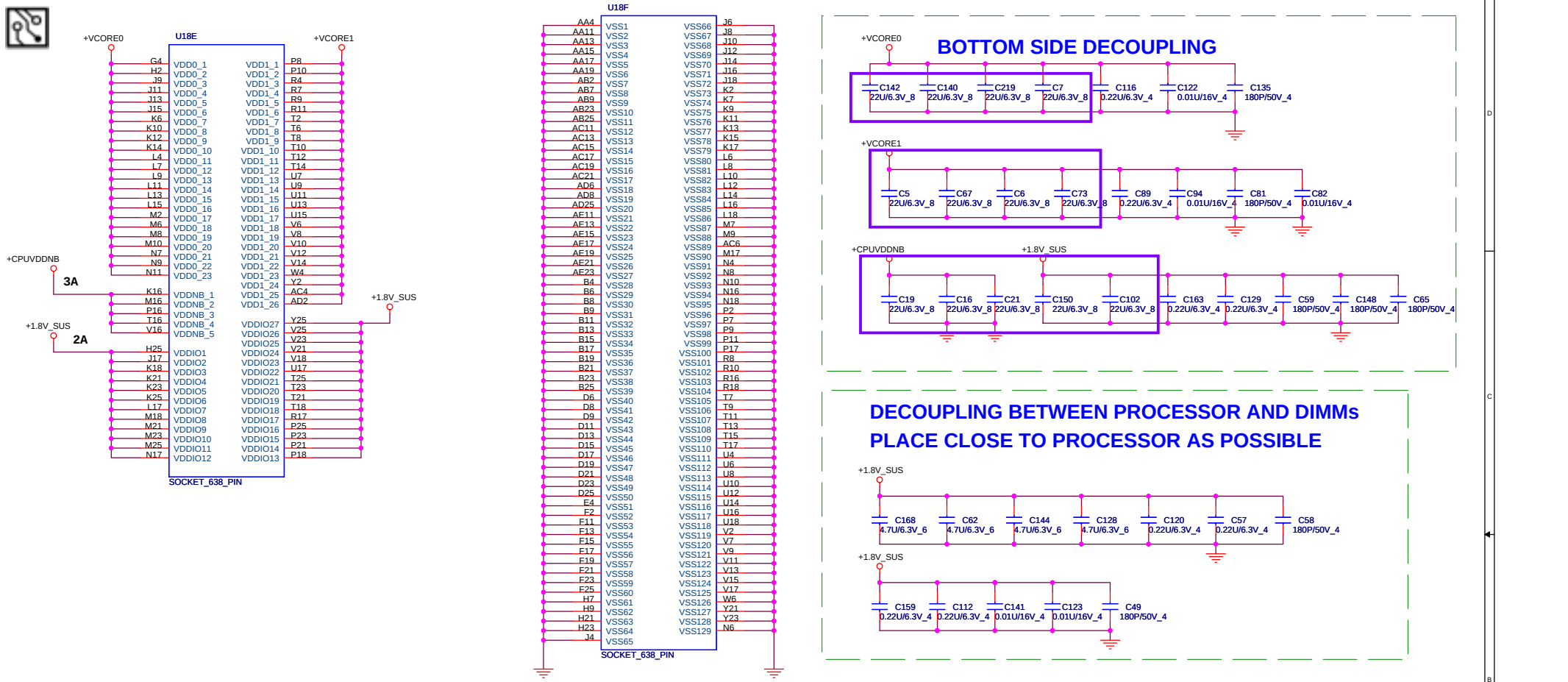
U18C — MEM:DATA — SOCKET_638_PIN

750 mA

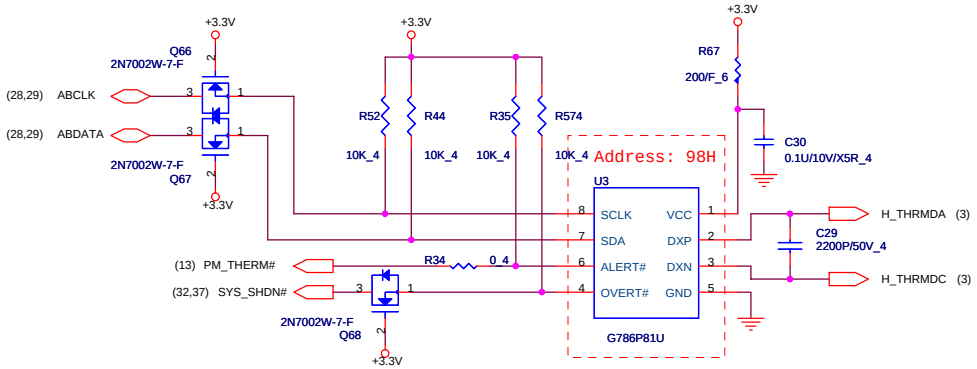
Place close to socket

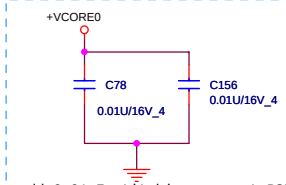
Close to CPU within 1200 mils

Project	PROJECT : AJ6
Company	Quanta Computer Inc.
Size	Custom
Document Number	S1G2 DDRII MEMORY I/F 2/3
Rev	1A
Date	Monday, August 18, 2008
Sheet	4 of 39

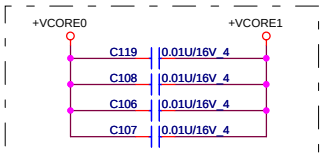


PROCESSOR POWER AND GROUND





add 0.01uF stitching caps at RS780 (near HT pin out) side for connecting CPU_CORE and GND planes.
(Around 1 cap with 6~8 HT pairs)



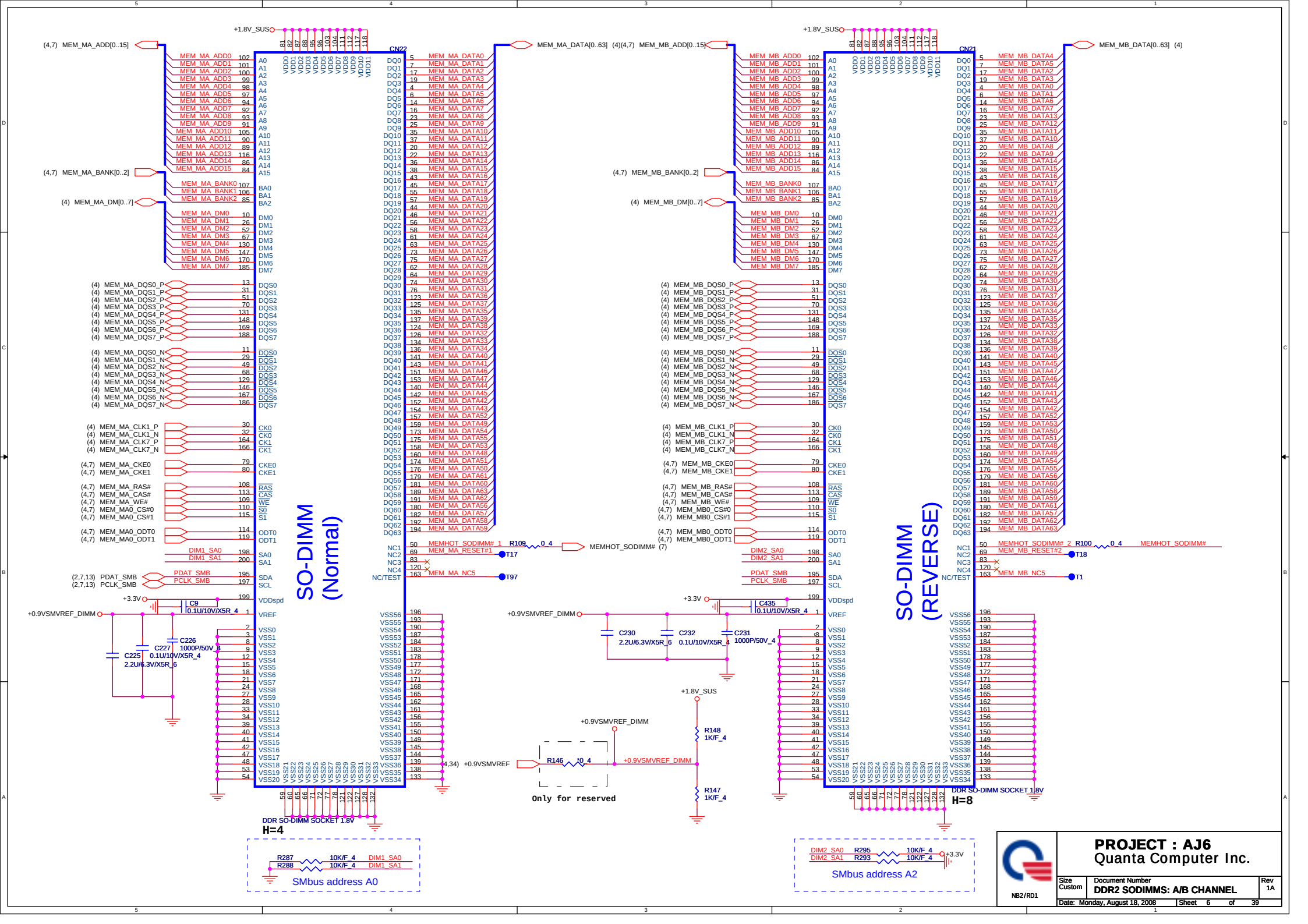
For fix HyperTransport nets across plane splits

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	S1G2 PWR & GND 3/3	2A

Date: Tuesday, August 19, 2008 | Sheet 5 of 39

NB2/RD1


SO-DIMM (Normal)
SO-DIMM (REVERSE)
CN22
CN21
DDR SO-DIMM SOCKET 1.8V
H=4
DDR SO-DIMM SOCKET 1.8V
H=8
Only for reserved
SMbus address A0
SMbus address A2
PROJECT : AJ6
Quanta Computer Inc.
DDR2 SODIMMS: A/B CHANNEL
NB2/RD1
Date: Monday, August 18, 2008
Sheet 6 of 39

(4,6) MEM_MA_ADD[0..15] → MEM_MA_ADD[0..15]
(4,6) MEM_MA_BANK[0..2] → MEM_MA_BANK[0..2]

+0.9VSMVTT

(4,6) MEM_MA_CKE0 — MEM_MA_CKE0 RP35 — MEM_MA_BANK2 — MEM_MA_ADD12 RP32 — MEM_MA_ADD9 — MEM_MA_ADD8 RP27 — MEM_MA_ADD5 — MEM_MA_ADD3 RP23 — MEM_MA_ADD1 — MEM_MA_ADD10 RP17 — MEM_MA_BANK0 — MEM_MA_WE# RP14 — MEM_MA_CAS# — MEM_MA0_ODT1 RP9 — MEM_MA0_CS#1 — MEM_MA_ADD15 RP34 — MEM_MA_CKE1 — MEM_MA_ADD7 RP30 — MEM_MA_ADD14 — MEM_MA_ADD6 RP26 — MEM_MA_ADD11 — MEM_MA_ADD2 RP21 — MEM_MA_ADD4 — MEM_MA_BANK1 RP19 — MEM_MA_ADD0 — MEM_MA0_CS#0 RP12 — MEM_MA_RAS# — MEM_MA_ADD13 RP10 — MEM_MA0_ODT0

(4,6) MEM_MA_WE#
(4,6) MEM_MA_CAS#
(4,6) MEM_MA0_ODT1
(4,6) MEM_MA0_CS#1
(4,6) MEM_MA_CKE1
(4,6) MEM_MA0_CS#0
(4,6) MEM_MA_RAS#
(4,6) MEM_MA0_ODT0

47_4P2R_4

C126 C154 C84 C130 C99 C44 C90 C97 C93 C47 C111 C117 C74 C48 C88 C109
0.1U/10V/X5R_4
+1.8V_SUS

(4,6) MEM_MB_ADD[0..15] → MEM_MB_ADD[0..15]
(4,6) MEM_MB_BANK[0..2] → MEM_MB_BANK[0..2]

+0.9VSMVTT

(4,6) MEM_MB_CKE0 — MEM_MB_CKE0 RP31 — MEM_MB_BANK2 — MEM_MB_ADD12 RP28 — MEM_MB_ADD9 — MEM_MB_ADD8 RP24 — MEM_MB_ADD5 — MEM_MB_ADD3 RP22 — MEM_MB_ADD1 — MEM_MB_ADD10 RP16 — MEM_MB_BANK0 — MEM_MB_WE# RP13 — MEM_MB_CAS# — MEM_MB0_ODT1 RP8 — MEM_MB0_CS#1 — MEM_MB_CKE1 RP33 — MEM_MB_ADD15 — MEM_MB_ADD7 RP29 — MEM_MB_ADD14 — MEM_MB_ADD6 RP25 — MEM_MB_ADD11 — MEM_MB_ADD2 RP20 — MEM_MB_ADD4 — MEM_MB_BANK1 RP18 — MEM_MB_ADD0 — MEM_MB0_CS#0 RP15 — MEM_MB_RAS# — MEM_MB0_ODT0 RP11 — MEM_MB_ADD13

(4,6) MEM_MB_WE#
(4,6) MEM_MB_CAS#
(4,6) MEM_MB0_ODT1
(4,6) MEM_MB0_CS#1
(4,6) MEM_MB_CKE1
(4,6) MEM_MB0_CS#0
(4,6) MEM_MB_RAS#
(4,6) MEM_MB0_ODT0

47_4P2R_4

C103 C121 C66 C95 C52 C79 C76 C69 C113 C151 C153 C155 C45 C152 C127 C157
0.1U/10V/X5R_4
+1.8V_SUS

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C54 C60 C75 C61 C167 C92
0.1U/10V/X5R_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

PLACE CLOSE TO PROCESSOR WITHIN 1.5 INCH

+1.8V_SUS

C143 C80 C145 C164 C55 C46
0.1U/10V/X5R_4

PLACE CLOSE TO SOCKET(PER EMI/EMC)

Close DDR2 socket

U17 *DS75U+T&R
A0 A1 A2 SDA SCL +VS O.S GND

+3.3V
C434 0.1U/10V/X5R_4
MEMHOT_SODIMM#
PDAT_SMB
PCLK_SMB
(2,6,13) PDAT_SMB
(2,6,13) PCLK_SMB
Address:92h

R289 *10K/F_4
R285 *10K/F_4
R286 *33_4
Q31 *2N7002E-G
Q32 *2N7002E-G
CPU_MEMHOT# (3,13)

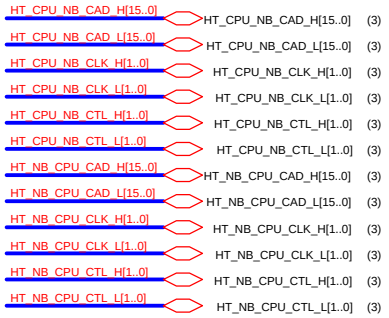
+3.3V R292 10K/F_4 MEMHOT_SODIMM# MEMHOT_SODIMM# (6)

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR2 SODIMMS TERMINATIONS	1A

Date: Monday, August 18, 2008 | Sheet 7 of 39

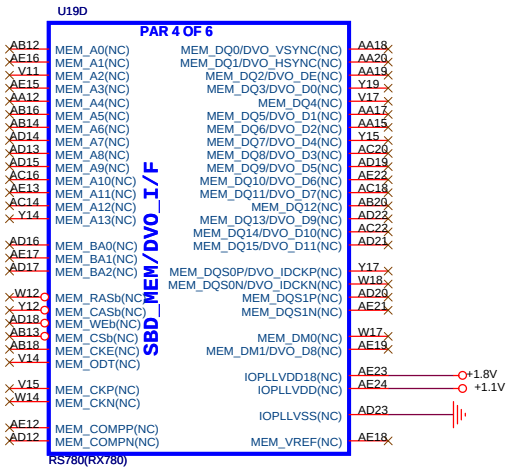


signals	RS780	RX780
HT_TXCALP	R641 300 ohm 1%	R641 1.21k ohm 1%
HT_TXCALN		
HT_RXCALP	R655 300 ohm 1%	R655 1.21k ohm 1%
HT_RXCALN		

RES CHIP 1.21K 1/16W +-1%(0402)
P/N : CS21212FB18

RES CHIP 300 1/16W +-1%(0402)
P/N : CS13002FB00

This block is for UMA RS780 only , RX780 NC



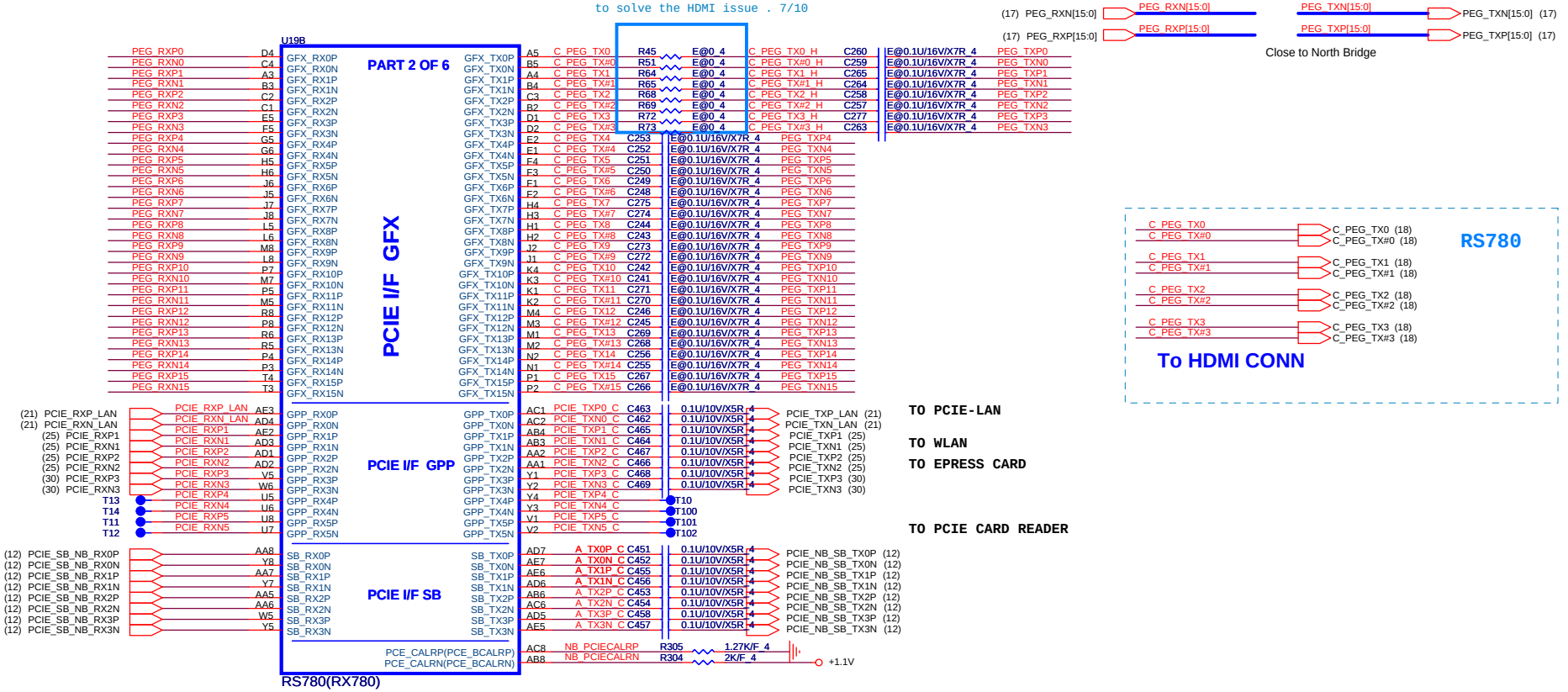
PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-HT LINK I/F 1/4	1A

NB2/RD1

Date: Monday, August 18, 2008 | Sheet 8 of 39

to solve the HDMI issue . 7/10



RX780/RS740/RS780 difference table (PCIE LINK)

	RX780/RS780
NB_PCIECALRP	1.27K (GND)
GPP4	GPP4
GPP5	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS780MN-PCIE I/F 2/4	3A

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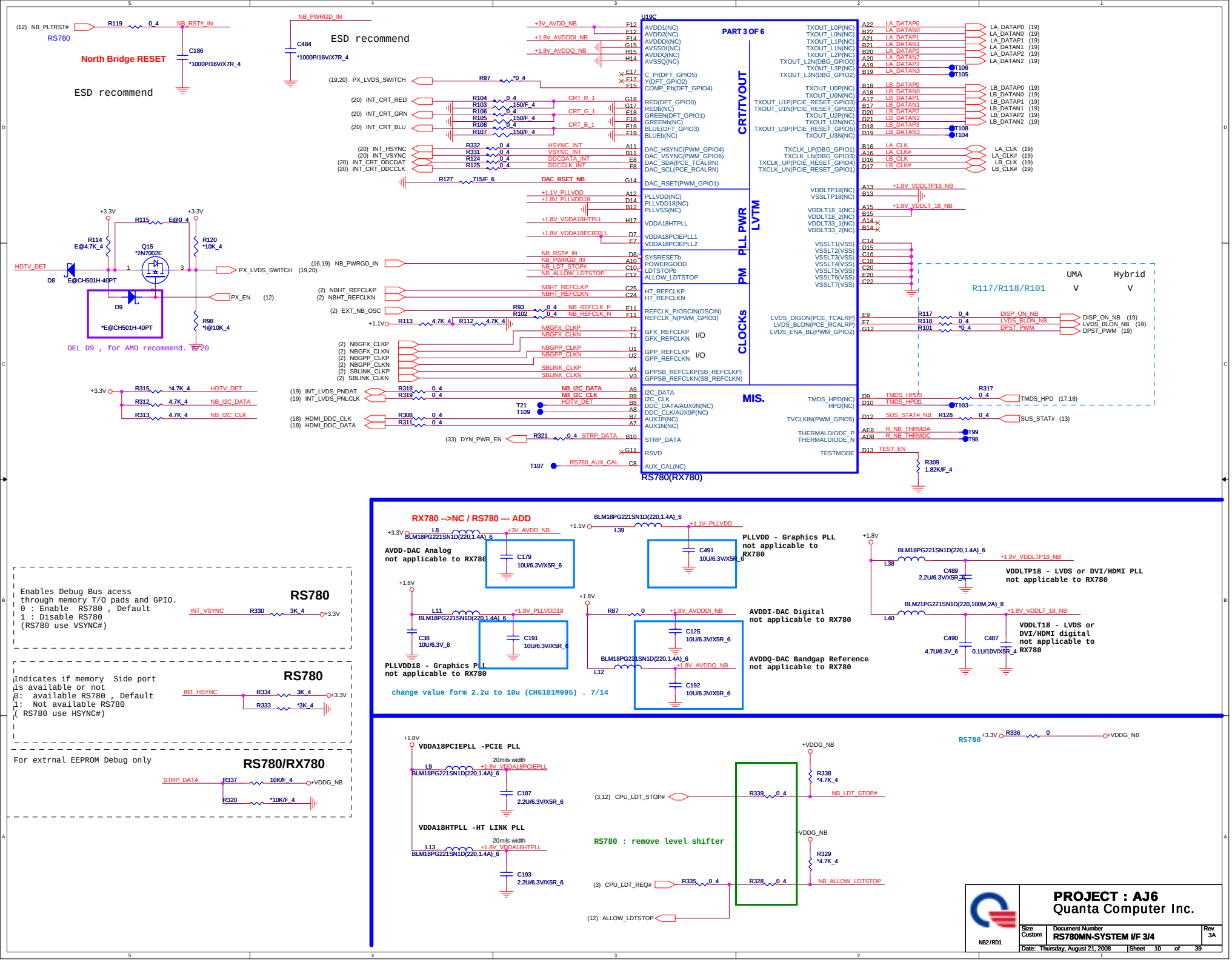
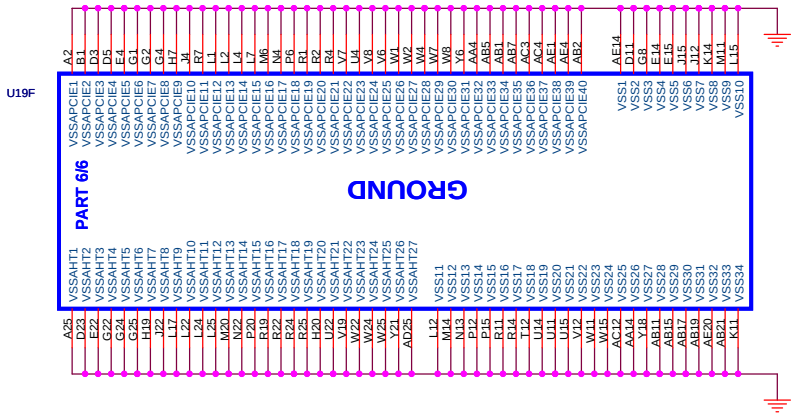
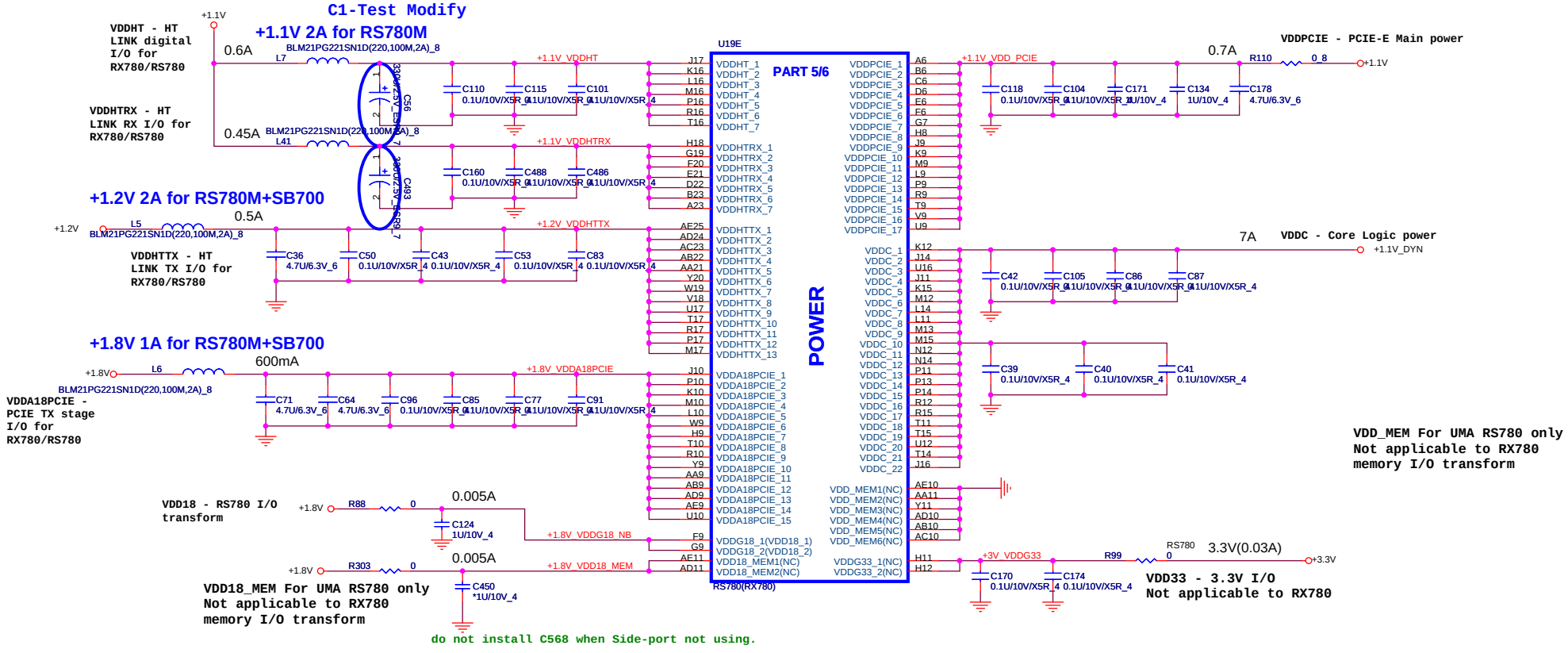
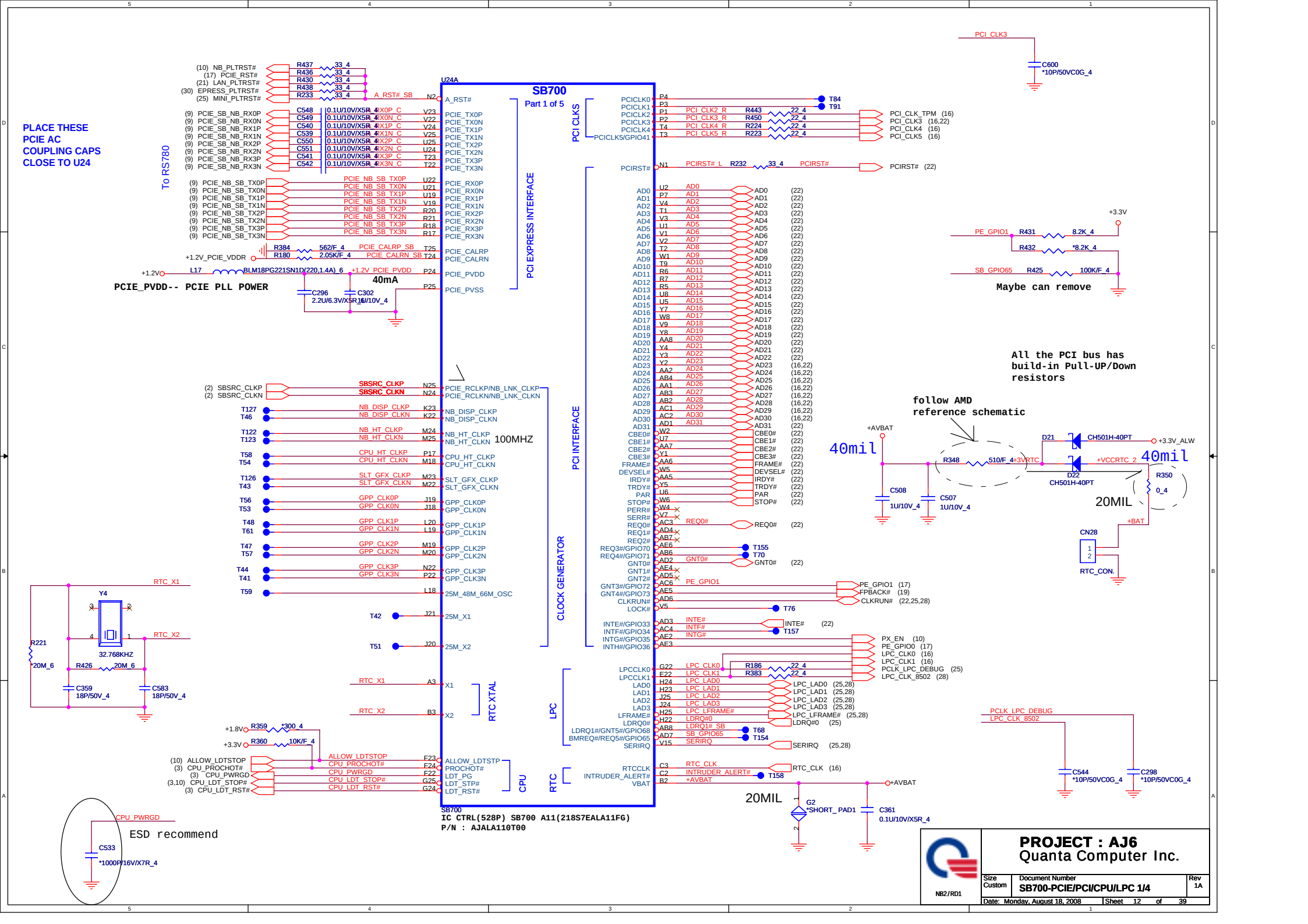

(12) NB_PLTRST#
R119 0_4 NB_RST#_IN
RS780
North Bridge RESET
C186 *1000P/16V/X7R_4
ESD recommend
NB_PWRGD_IN
C484 *1000P/16V/X7R_4
ESD recommend
U19C
PART 3 OF 6
CRT/TVOUT
PLL PWR
LVTM
PM
CLOCKs
MIS.
RS780(RX780)
(19,20) PX_LVDS_SWITCH R97 *0_4
(20) INT_CRT_RED R104 0_4 CRT_R_1
(20) INT_CRT_GRN R103 150/F_4 R106 0_4 CRT_G_1
(20) INT_CRT_BLU R105 150/F_4 R108 0_4 CRT_B_1
R107 150/F_4
(20) INT_HSYNC R332 0_4 HSYNC_INT
(20) INT_VSYNC R331 0_4 VSYNC_INT
(20) INT_CRT_DDCDAT R124 0_4 DDCDATA_INT
(20) INT_CRT_DDCCLK R125 0_4 DDCCLK_INT
R127 715/F_6 DAC_RSET_NB
+3V_AVDD_NB
+1.8V_AVDDDI_NB
+1.8V_AVDDQ_NB
+1.1V_PLLVDD
+1.8V_PLLVDD18
+1.8V_VDDA18HTPLL
+1.8V_VDDA18PCIEPLL
(16,19) NB_PWRGD_IN
NB_RST#_IN
NB_PWRGD_IN
NB_LDT_STOP#
NB_ALLOW_LDTSTOP
(2) NBHT_REFCLKP
(2) NBHT_REFCLKN
NBHT_REFCLKP
NBHT_REFCLKN
(2) EXT_NB_OSC R93 0_4 R102 0_4 NB_REFCLK_P NB_REFCLK_N
+1.1V R113 4.7K_4 R112 4.7K_4
(2) NBGFX_CLKP
(2) NBGFX_CLKN
(2) NBGPP_CLKP
(2) NBGPP_CLKN
(2) SBLINK_CLKP
(2) SBLINK_CLKN
NBGFX_CLKP
NBGFX_CLKN
NBGPP_CLKP
NBGPP_CLKN
SBLINK_CLKP
SBLINK_CLKN
(19) INT_LVDS_PNDAT R318 0_4 NB_I2C_DATA
(19) INT_LVDS_PNCLCK R319 0_4 NB_I2C_CLK
HDTV_DET
(18) HDMI_DDC_CLK R308 0_4
(18) HDMI_DDC_DATA R311 0_4
(33) DYN_PWR_EN R321 0_4 STRP_DATA
T107 RS780_AUX_CAL
T21
T109
+3.3V R115 E@0_4 R114 E@4.7K_4 R120 *10K_4
Q15 *2N7002E
HDTV_DET
D8 E@CH501H-40PT
PX_LVDS_SWITCH (19,20)
PX_EN (12)
D9 *E@CH501H-40PT
R98 *1@10K_4
DEL D9 , for AMD recommend. 8/20
+3.3V R315 *4.7K_4 HDTV_DET
R312 4.7K_4 NB_I2C_DATA
R313 4.7K_4 NB_I2C_CLK
TXOUT_L0P(NC) TXOUT_L0N(NC) TXOUT_L1P(NC) TXOUT_L1N(NC) TXOUT_L2P(DBG_GPIO0) TXOUT_L2N(DBG_GPIO1) TXOUT_L3P(NC) TXOUT_L3N(DBG_GPIO2)
LA_DATAP0 LA_DATAN0 LA_DATAP1 LA_DATAN1 LA_DATAP2 LA_DATAN2 LA_DATAP3 LA_DATAN3
TXOUT_U0P(NC) TXOUT_U0N(NC) TXOUT_U1P(PCIE_RESET_GPIO3) TXOUT_U1N(PCIE_RESET_GPIO2) TXOUT_U2P(NC) TXOUT_U2N(NC) TXOUT_U3P(PCIE_RESET_GPIO5) TXOUT_U3N(NC)
LB_DATAP0 LB_DATAN0 LB_DATAP1 LB_DATAN1 LB_DATAP2 LB_DATAN2 LB_DATAP3 LB_DATAN3
TXCLK_LP(DBG_GPIO1) TXCLK_LN(DBG_GPIO3) TXCLK_UP(PCIE_RESET_GPIO4) TXCLK_UN(PCIE_RESET_GPIO1)
LA_CLK LA_CLK# LB_CLK LB_CLK#
VDDLTP18(NC) VSSLTP18(NC)
+1.8V_VDDLTP18_NB
VDDLT18_1(NC) VDDLT18_2(NC) VDDLT33_1(NC) VDDLT33_2(NC)
+1.8V_VDDLT_18_NB
VSSLT1(VSS) VSSLT2(VSS) VSSLT3(VSS) VSSLT4(VSS) VSSLT5(VSS) VSSLT6(VSS) VSSLT7(VSS)
UMA Hybrid
R117/R118/R101 V V
LVDS_DIGON(PCE_TCALRP) LVDS_BLON(PCE_RCALRP) LVDS_ENA_BL(PWM_GPIO2)
DISP_ON_NB LVDS_BLON_NB DPST_PWM
TMDS_HPD(NC) HPD(NC)
TMDS_HPD0 TMDS_HPD1
TMDS_HPD (17,18)
TVCLKIN(PWM_GPIO5)
SUS_STAT#_NB R126 0_4 SUS_STAT# (13)
THERMALDIODE_P THERMALDIODE_N
R_NB_THRMDA R_NB_THRMDC
TESTMODE
TEST_EN R309 1.82K/F_4
RX780 -->NC / RS780 --- ADD
AVDD-DAC Analog not applicable to RX780
PLLVDD - Graphics PLL not applicable to RX780
PLLVDD18 - Graphics PLL not applicable to RX780
AVDDI-DAC Digital not applicable to RX780
AVDDQ-DAC Bandgap Reference not applicable to RX780
VDDLTP18 - LVDS or DVI/HDMI PLL not applicable to RX780
VDDLT18 - LVDS or DVI/HDMI digital not applicable to RX780
change value form 2.2u to 10u (CH6101M995) . 7/14
Enables Debug Bus acess through memory T/O pads and GPIO.
0 : Enable RS780 , Default
1 : Disable RS780
(RS780 use VSYNC#)
RS780
INT_VSYNC R330 3K_4 +3.3V
Indicates if memory Side port is available or not
0: available RS780 , Default
1: Not available RS780
(RS780 use HSYNC#)
RS780
INT_HSYNC R334 3K_4 R333 *3K_4 +3.3V
For extrnal EEPROM Debug only
RS780/RX780
STRP_DATA R337 10K/F_4 +VDDG_NB
R320 *10K/F_4
VDDA18PCIEPLL -PCIE PLL
VDDA18HTPLL -HT LINK PLL
20mils width
RS780 : remove level shifter
(3,12) CPU_LDT_STOP#
(3) CPU_LDT_REQ#
(12) ALLOW_LDTSTOP
R338 *4.7K_4
R339 0_4 NB_LDT_STOP#
R329 *4.7K_4
R335 0_4
R328 0_4 NB_ALLOW_LDTSTOP
RS780 +3.3V R336 0 +VDDG_NB
PROJECT : AJ6
Quanta Computer Inc.
Size Custom
Document Number RS780MN-SYSTEM I/F 3/4
Rev 3A
Date: Thursday, August 21, 2008
Sheet 10 of 39
NB2/RD1



RX780/RS780 POWER DIFFERENCE TABLE

PIN NAME	RX780	RS780	PIN NAME	RX780	RS780
VDDHT	+1.1V	+1.1V	IOPLLVDD	NC	+1.1V
VDDHTRX	+1.1V	+1.1V	AVDD	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	AVDDDI	NC	+1.8V
VDDA18PCIE	+1.8V	+1.8V	AVDDQ	NC	+1.8V
VDDG18	+1.8V	+1.8V	PLLVDD	NC	+1.1V
VDD18_MEM	NC	+1.8V	PLLVDD18	NC	+1.8V
VDDPCIE	+1.1V	+1.1V	VDDA18PCIEPLL	+1.8V	+1.8V
VDDC	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V
VDD_MEM	NC	+1.8V/1.5V	VDDLTP18	NC	+1.8V
VDDG33	NC	+3.3V	VDDLT18	NC	+1.8V
IOPLLVDD18	NC	+1.8V	VDDLT33	NC	NC




PLACE THESE
PCIE AC
COUPLING CAPS
CLOSE TO U24
To RS780
SB700
Part 1 of 5
PCI CLKS
PCI EXPRESS INTERFACE
PCI INTERFACE
CLOCK GENERATOR
LPC
RTC XTAL
CPU
RTC
PCIE_PVDD-- PCIE PLL POWER
40mA
100MHZ
20MIL
40mil
follow AMD
reference schematic
All the PCI bus has
build-in Pull-UP/Down
resistors
Maybe can remove
ESD recommend
SB700
IC CTRL(528P) SB700 A11(218S7EALA11FG)
P/N : AJALA110T00
PROJECT : AJ6
Quanta Computer Inc.
SB700-PCIE/PCI/CPU/LPC 1/4
Monday, August 18, 2008

NC only ,Can't be install

+3.3V_SUS
R461 *2.2K_4 SB_TEST0
R256 *2.2K_4 SB_TEST1
R242 *2.2K_4 SB_TEST2

+3.3V_SUS
R236 *10K/F_4 SWI#

+3.3V
R170 2.2K_4 PCLK_SMB
R173 2.2K_4 PDAT_SMB

SCL0/SDATA0 is 3V tolerance
AMD datasheet define it

Clock gen/Robson
/DDR2/DDR2
thermal/Accelerometer

+3.3V_S5
SCL1/SDATA1 is 3V/S5 tolerance
AMD datasheet define it
R245 2.2K_4 SB_SMBCLK1
R244 2.2K_4 SB_SMBDATA1

+3.3V_S5
SCL2/SDATA2 is 3V/S5 tolerance
AMD datasheet define it
R381 2.2K_4 SB_SCLK2
R380 2.2K_4 SB_SDATA2
R249 1K_4 DNBSWON#

+3.3V
R406 10K_4 GPIO10
R240 *4.7K_4 SUS_STAT#
R179 *10K_4 GPIO0
R182 *10K_4 GPIO39
R185 *10K_4 GPIO40
R167 10K_4 GPIO4
R400 10K_4 GPIO6

Not connected (internal pull-down).
remove external pull up resistor.

G3
2 1 SYS_RST#
*SHORT_PAD1

To Azalia

ADD HDA for MXM 0215

ACZ_SDOUT R453 33_4 ACZ_SDOUT_AUDIO (23)
R455 E@33_4 ACZ_SDOUT_MXM (17)
ACZ_SYNC R250 33_4 ACZ_SYNC_AUDIO (23)
R238 E@33_4 ACZ_SYNC_MXM (17)
ACZ_BCLK R444 33_4 BIT_CLK_AUDIO (23)
R239 E@33_4 ACZ_BITCLK_MXM (17)
ACZ_RST# R459 33_4 ACZ_RST#_AUDIO (23)
R460 E@33_4 ACZ_RESET#_MXM (17)
ACZ_SDIN2_R R248 0_4 ACZ_SDIN2 (17)
ACZ_SDIN0_R R243 0_4 ACZ_SDIN0 (23)

To Modem Board

ACZ_SDOUT R454 33_4 ACZ_SDOUT_AUDIO_MDC (26)
C603 *10P/50VC0G_4
ACZ_SYNC R246 33_4 ACZ_SYNC_AUDIO_MDC (26)
C374 *10P/50VC0G_4
ACZ_BCLK R445 33_4 BIT_CLK_AUDIO_MDC (26)
C375 *10P/50VC0G_4
ACZ_RST# R463 33_4 ACZ_RST#_AUDIO_MDC (26)
ACZ_SDIN1_R R410 33_4 ACZ_SDIN1 (26)

MXM

D23 CH501H-40PT
(3,7) CPU_MEMHOT#
(5) PM_THERM#
R419 *0_4 CPU_MEMHOT#_IN
R420 *10K/F_4 +3.3V SMBALERT#_1

(30) NEWCARD_DETECT
(26) USB_OC2#
(27) USB_OC1#
T169 SB_JTAG_TDO
SB_JTAG_TCK
SB_JTAG_TDI
SB_JTAG_RST#
T163

ACZ_BCLK
ACZ_SDOUT
ACZ_SDIN0_R
ACZ_SDIN1_R
ACZ_SDIN2_R
T89
ACZ_SYNC
(16) ACZ_RST#
ACZ_RST#

HD audio
interface is
3.3V voltage

ADD GPIO pin for MXM 0215

+3.3V
(17) MXM_PRESENT#
T50 MXM_RUNPWROK
R361 22K_4 HDD_AUX_RST#
T45 MXM_PWR_EN

U24D

SB700

Part 4 of 5

(22) PCI_PME# PCI_PME#
T167 RI#
T74 SLP_S2
(28) SUSB# R231 0_4 SUSB#_R
(28) SUSC# R234 0_4 SUSC#_R
(28) DNBSWON#
(16) SB_PWRGD_IN SB_PWRGD_IN
(10) SUS_STAT# SUS_STAT#
SB_TEST2
SB_TEST1
SB_TEST0
(28) GATEA20 GATEA20
(28) RCIN# RCIN#
(28) SCI# SCI#
(28) KBSMI# KBSMI#
T161 SYS_RST#
(21,25,30) PCIE_WAKE# PCIE_WAKE#
(28) SWI# R235 0_4 SWI#_R
(3) CPU_THERMTRIP# CPU_THERMTRIP#
(16) WD_PWRGD WD_PWRGD
(28) RSMRST# R456 0_4 RSMRST#_R

GPIO10
GPIO6
GPIO4
GPIO0
GPIO39
GPIO40
(23) ACZ_SPKR
(2,6,7) PCLK_SMB
(2,6,7) PDAT_SMB
(25) SB_SMBCLK1
(25) SB_SMBDATA1
(25) SB_SMBDATA2
(17) PE_RESET_MXM#
T160 PM_BATLOW#
T52 SES_INT
T79 GEVENT7#

USBCLK/14M_25M_48M_OSC
USB_RCOMP
USB_FSD13P
USB_FSD13N
USB_FSD12P
USB_FSD12N
USB_HSD11P
USB_HSD11N
USB_HSD10P
USB_HSD10N
USB_HSD9P
USB_HSD9N
USB_HSD8P
USB_HSD8N
USB_HSD7P
USB_HSD7N
USB_HSD6P
USB_HSD6N
USB_HSD5P
USB_HSD5N
USB_HSD4P
USB_HSD4N
USB_HSD3P
USB_HSD3N
USB_HSD2P
USB_HSD2N
USB_HSD1P
USB_HSD1N
USB_HSD0P
USB_HSD0N

PCI_PME#/GEVENT4#
RI#/EXTEVNT0#
SLP_S2/GPM9#
SLP_S3#
SLP_S5#
PWR_BTN#
PWR_GOOD
SUS_STAT#
TEST2
TEST1
TEST0
GA20IN/GEVENT0#
KBRST#/GEVENT1#
LPC_PME#/GEVENT3#
LPC_SMI#/EXTEVNT1#
S3_STATE/GEVENT5#
SYS_RESET#/GPM7#
WAKE#/GEVENT8#
BLINK/GPM6#
SMBALERT#/THRMTRIP#/GEVENT2#
NB_PWRGD
RSMRST#

SATA_IS0#/GPIO10
CLK_REQ3#/SATA_IS1#/GPIO6
SMARTVOLT/SATA_IS2#/GPIO4
CLK_REQ0#/SATA_IS3#/GPIO0
CLK_REQ1#/SATA_IS4#/FANOUT3/GPIO39
CLK_REQ2#/SATA_IS5#/FANIN3/GPIO40
SPKR/GPIO2
SCL0/GPOC0#
SDA0/GPOC1#
SCL1/GPOC2#
SDA1/GPOC3#
DDC1_SCL/GPIO9
DDC1_SDA/GPIO8
LLB#/GPIO66
SHUTDOWN#/GPIO5
DDR3_RST#/GEVENT7#

USB_OC6#/IR_TX1/GEVENT6#
USB_OC5#/IR_TX0/GPM5#
USB_OC4#/IR_RX0/GPM4#
USB_OC3#/IR_RX1/GPM3#
USB_OC2#/GPM2#
USB_OC1#/GPM1#
USB_OC0#/GPM0#

AZ_BITCLK
AZ_SDOUT
AZ_SDIN0/GPIO42
AZ_SDIN1/GPIO43
AZ_SDIN2/GPIO44
AZ_SDIN3/GPIO46
AZ_SYNC
AZ_RST#
AZ_DOCK_RST#/GPM8#

IMC_GPIO0
IMC_GPIO1
SPI_CS2#/IMC_GPIO2
IDE_RST#/F_RST#/IMC_GPO3
IMC_GPIO4
IMC_GPIO5
IMC_GPIO6
IMC_GPIO7

IMC_GPIO8
IMC_GPIO9
IMC_PWM0/IMC_GPIO10
SCL2/IMC_GPIO11
SDA2/IMC_GPIO12
SCL3_LV/IMC_GPIO13
SDA3_LV/IMC_GPIO14
IMC_PWM1/IMC_GPIO15
IMC_PWM2/IMC_GPO16
IMC_PWM3/IMC_GPO17
IMC_GPIO18
IMC_GPIO19
IMC_GPIO20
IMC_GPIO21
IMC_GPIO22
IMC_GPIO23
IMC_GPIO24
IMC_GPIO25
IMC_GPIO26
IMC_GPIO27
IMC_GPIO28
IMC_GPIO29
IMC_GPIO30
IMC_GPIO31
IMC_GPIO32
IMC_GPIO33
IMC_GPIO34
IMC_GPIO35
IMC_GPIO36
IMC_GPIO37
IMC_GPIO38
IMC_GPIO39
IMC_GPIO40
IMC_GPIO41

ACPI / WAKE UP EVENTS
USB MISC
USB 1.1
USB 2.0
GPIO
USB OC
HD AUDIO
INTEGRATED uC
INTEGRATED uC

C8 CLK_48M_USB_L CLK_48M_USB (2)
G8 USB_RCOMP_SB R204 11.8K/F
R418 *33_4
C577 *0.1U/10V_4

E6 USB_FSD13P T81
E7 USB_FSD13N T71
E7 USB_FSD12P T66
E8 USB_FSD12N T67

H11 USBP9+ (27)
J10 USBP9- (27) USB Connector EMI recommend

E11 T62
F11 T65
A11 T142
B11 T145

C10 USBP5+ (25)
D10 USBP5- (25) Min-Card

G11 USBP8+ (27)
H12 USBP8- (27) USB Connector

E12 T64
E14 T63

C12 USBP2+ (26)
D12 USBP2- (26) USB Connector

B12 USBP4+ (25)
A12 USBP4- (25) WLAN Min-Card

G12 USBP11+ (30)
G14 USBP11- (30) NEW CARD

H14 USBP7+ (19)
H15 USBP7- (19) Carama USB

A13 USBP1+ (26)
B13 USBP1- (26) BLUETOOTH

B14 USBP0+ (26)
A14 USBP0- (26) USB Connector

SB_SCLK2 (30)
SB_SDATA2 (30)
SB_GPIO16 (16)
SB_GPIO17 (16) SPI/LPC define

CN13
+3.3V_SUS
SB JTAG
SB_JTAG_TCK
SB_JTAG_TDO
SB_JTAG_TDI
SB_TEST1
SB_JTAG_RST#
*S/W JTAG DEBUG

SB700

NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.	
Size Custom	Document Number SB700-ACPI/GPIO/USB 2/4	Rev 1A
Date: Monday, August 18, 2008	Sheet 13 of 39	

SATA PORT 0,1,2,3 can support AHCI mode

SATA1

PLACE SATA AC COUPLING CAPS CLOSE TO SB700

(24) SATA_TXP0 — C581 0.01U/16V_4 — SATA_TXP0_C — AD9 SATA_TX0P
(24) SATA_TXN0 — C578 0.01U/16V_4 — SATA_TXN0_C — AE9 SATA_TX0N
(24) SATA_RXN0 — AB10 SATA_RX0N
(24) SATA_RXP0 — AC10 SATA_RX0P

T148 — SATA_TXP1_C — AE10 SATA_TX1P
T147 — SATA_TXN1_C — AD10 SATA_TX1N

T144 — SATA_RXN1_C — AD11 SATA_RX1N
T146 — SATA_RXP1_C — AE11 SATA_RX1P

AB12 SATA_TX2P
AC12 SATA_TX2N

AE12 SATA_RX2N
AD12 SATA_RX2P

AD13 SATA_TX3P
AE13 SATA_TX3N

AB14 SATA_RX3N
AC14 SATA_RX3P

SATA PORT 4,5 are only support IDE mode

SATA ODD

(24) SATA_TXP4 — C575 0.01U/16V_4 — SATA_TXP4_C — AE14 SATA_TX4P
(24) SATA_TXN4 — C574 0.01U/16V_4 — SATA_TXN4_C — AD14 SATA_TX4N
(24) SATA_RXN4 — AD15 SATA_RX4N
(24) SATA_RXP4 — AE15 SATA_RX4P

T139 — SATA_TXP5_C — AB16 SATA_TX5P
T143 — SATA_TXN5_C — AC16 SATA_TX5N

T140 — SATA_RXN5_C — AE16 SATA_RX5N
T141 — SATA_RXP5_C — AD16 SATA_RX5P

R201 1K/F_4 — SATA_RBIAS_PN — V12 SATA_CAL

SATA_X1 — Y12 SATA_X1
SATA_X2 — AA12 SATA_X2

SB_SATA_LED# — W11 SATA_ACT#/GPIO67

+3.3V — R163 10K/F_4 — +1.2V_PLLVDD_SATA — AA11 PLLVDD_SATA
+3V_XTLVDD_SATA — W12 XTLVDD_SATA

PLACE SATA_CAL RES VERY CLOSE TO BALL OF SB700

NOTE:
R201 IS 1K 1% FOR 25MHz XTAL, 4.99K 1% FOR 100MHz INTERNAL CLOCK

PLVDD_SATA-- SATA PLL POWER

XTLVDD_SATA-- SATA crystal power

C338 33P/50V/NPO_4 — SATA_X1
Y3 25MHZ
R198 10M_6
C327 33P/50V/NPO_4 — SATA_X2

U24B

SB700
Part 2 of 5

SERIAL ATA
SATA PWR

IF THERE IS NO IDE, TEST POINTS FOR DEBUG BUS IS MANDATORY

ATA 66/100/133

IDE_IORDY AA24 T114
IDE_IRQ AA25 T115
IDE_A0 Y22 T40
IDE_A1 AB23 T120
IDE_A2 Y23 T119
IDE_DACK# AB24 T118
IDE_DRQ AD25 T117
IDE_IOR# AC25 T125
IDE_IOW# AC24 T116
IDE_CS1# Y25 T124
IDE_CS3# Y24 T121

IDE_D0/GPIO15 AD24 — R388 0_4 — WLAN_RF_OFF# — WLAN_RF_OFF# (25,29)
IDE_D1/GPIO16 AD23 T129
IDE_D2/GPIO17 AE22 T131
IDE_D3/GPIO18 AC22 T130
IDE_D4/GPIO19 AD21 T132
IDE_D5/GPIO20 AE20 T135
IDE_D6/GPIO21 AB20 T133
IDE_D7/GPIO22 AD19 T138
IDE_D8/GPIO23 AE19 T137
IDE_D9/GPIO24 AC20 T134
IDE_D10/GPIO25 AD20 T136
IDE_D11/GPIO26 AE21 BOARD_ID0
IDE_D12/GPIO27 AB22 BOARD_ID1
IDE_D13/GPIO28 AD22 BOARD_ID2
IDE_D14/GPIO29 AE23 BOARD_ID3
IDE_D15/GPIO30 AC23 BOARD_ID4

SPI ROM

SPI_DI/GPIO12 G6 T73
SPI_DO/GPIO11 D2 T164
SPI_CLK/GPIO47 D1 T165
SPI_HOLD#/GPIO31 F4 T83
SPI_CS#/GPIO32 F3 T85

LAN_RST#/GPIO13 U15 — R193 0_4 — BT_ON# (26,29)
ROM_RST#/GPIO14 J1 — ROM_RST# — T159

HW MONITOR

FANOUT0/GPIO3 M8 — SB_FANOUT0 — T72
FANOUT1/GPIO48 M5 — SB_FANOUT1 — T75
FANOUT2/GPIO49 M7

FANIN0/GPIO50 P5 — SB_FANTACH0 — T87
FANIN1/GPIO51 P8 — SB_FANTACH1 — T77
FANIN2/GPIO52 R8 — PORT_80_PWR_DWN — T69

TEMP_COMM C6 — TEMP_COMM
TEMPIN0/GPIO61 B6 — TEMPIN0 — T150
TEMPIN1/GPIO62 A6 — TEMPIN1 — T149
TEMPIN2/GPIO63 A5 — MB_THRMDA_SB — T153
TEMPIN3/TALERT#/GPIO64 B5 — T151

VIN0/GPIO53 A4
VIN1/GPIO54 B4
VIN2/GPIO55 C4
VIN3/GPIO56 D4
VIN4/GPIO57 D5
VIN5/GPIO58 D6
VIN6/GPIO59 A7
VIN7/GPIO60 B7

AVDD F6 — 5mA — +3V_VDD_HWM — L24 0 — +3.3V
AVSS G7 — C358 *0.1U/10V_4 — C356 *2.2U/6.3V_6

AVDD--H/W monitor Analog power

SB700

+3.3V — C280 0.1U/10V/X5R_4
(29) SATA_LED# — U12 TC7SH08FU — SB_SATA_LED#

+1.2V — (1.2V @ 60mA) — L23 BLM18PG221SN1D(220,1.4A)_6 — +1.2V_PLLVDD_SATA — 77mA
C346 1U/10V_4
C345 0.1U/10V/X5R_4

+3.3V — (3.3V @ 1.2mA) — L25 BLM18PG221SN1D(220,1.4A)_6 — +3V_XTLVDD_SATA — 1mA
C357 1U/10V_4
Place near ball

+3.3V
R392 E@10K/F_4 BOARD_ID0 R391 *I@10K/F_4
R184 *10K/F_4 BOARD_ID1 R183 10K/F_4
R372 *10K/F_4 BOARD_ID2 R387 10K/F_4
R371 *10K/F_4 BOARD_ID3 R386 10K/F_4
R368 10K/F_4 BOARD_ID4 R370 *10K/F_4

Modify 5/7/2008

	UMA	MXM
ID0	0	1
ID1	0	0
ID2	0	0
ID3	0	0
ID4	1	1

change the board ID. 7/10

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-ACPI/GPIO/USB 2/4	3A

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NB2/RD1

PLACE ALL THE DECOUPLING CAPS ON
THIS SHEET CLOSE TO SB AS POSSIBLE.

For SB700 issue(6/22)
A1-1 chip bug
use A1-2 chip can remove

SB700
Part 3 of 5

SB700
Part 5 of 5

POWER

GROUND

VDDQ--3.3V I/O power
0.8A

1.8V : FLASH MEMORY MODE(DEFAULT)
3.3V: IDE MODE

VDD-- S/B CORE power
604mA

CKVDD_1.2V-- Internal
clock Generator I/O
power
286mA

VDD33_18--3.3V IDE I/O power
1.8V flash memory I/O power
0.45A

PCIE_VDDR--PCIE I/O power
844mA

S5_3.3--3.3v standby power
0.01A

S5_1.2V--1.2V standby power
0.22A

AVDD_SATA--SATA phy power
0.2A

0.2A

For support USB wakeup-->3V_S5

AVDDTX--USB Phy
Analog I/O power
0.2A

V5_VREF--PCI 5V TOLERANCE
4mA

7mA

44mA

16mA

USB_PHY_1.2V--USB Phy
digital power

AVDDC--USB Analog PLL power

AVDDCK_1.2--USB Phy
digital power

AVDDCK_3.3--Analog
system PLL power

PROJECT : AJ6	
Quanta Computer Inc.	
Size: Custom	Document Number: SB700-PWR/DECOUPLING 4/4
Rev: 2A	
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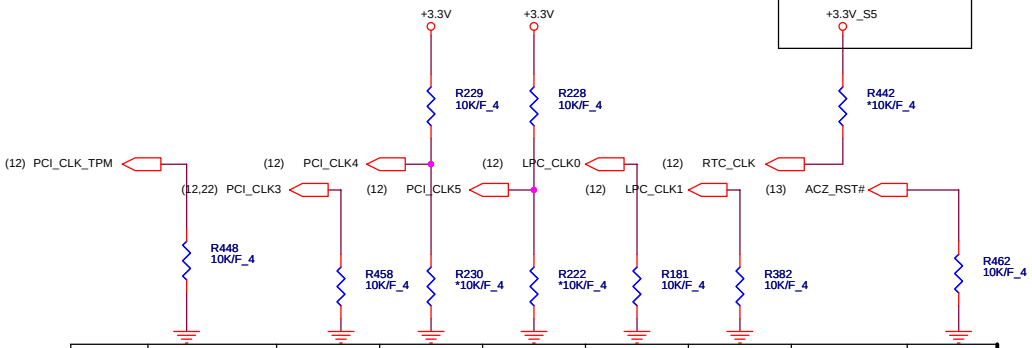
NB2/RD1	

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

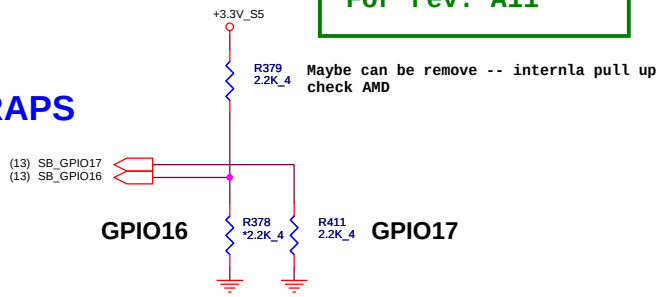
It must ready refore RSMRST#

REQUIRED STRAPS



	PCI_CLK_TPM	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST#
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT

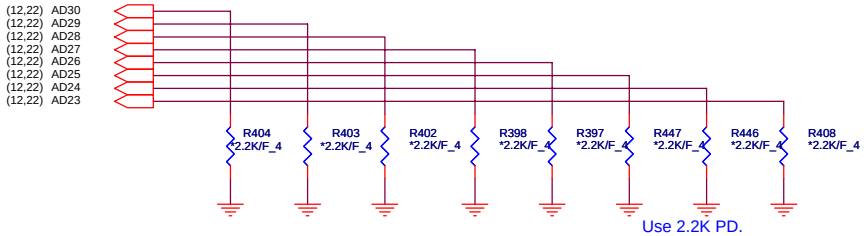
For rev. A11



TYPE	GPIO16	GPIO17
FWH	L : 2.2K pull down	L : 2.2K pull down
LPC	NC	L : 2.2K pull down
SPI	L : 2.2K pull down	NC
RSVD	NC	NC

DEBUG STRAPS

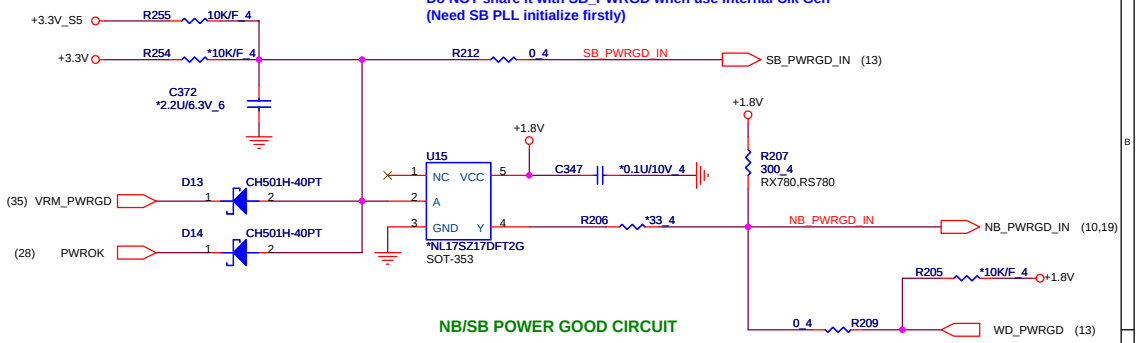
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]



Use 2.2K PD.

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

NB_PWRGD_IN:
RS780/RX780 = 1.8V; RS740 = 3.3V
Do NOT share it with SB_PWRGD when use Internal Clk Gen
(Need SB PLL initialize firstly)



NB/SB POWER GOOD CIRCUIT

AL17SZ17000	IC(5P) NL17SZ17DFT2G(SOT-353)	SOT-353
ALUC1G17000	IC OTHER(5P) SN74AUC1G17DBVR(SOT23-5)	SOT23-5

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB700-STRAPS	1A

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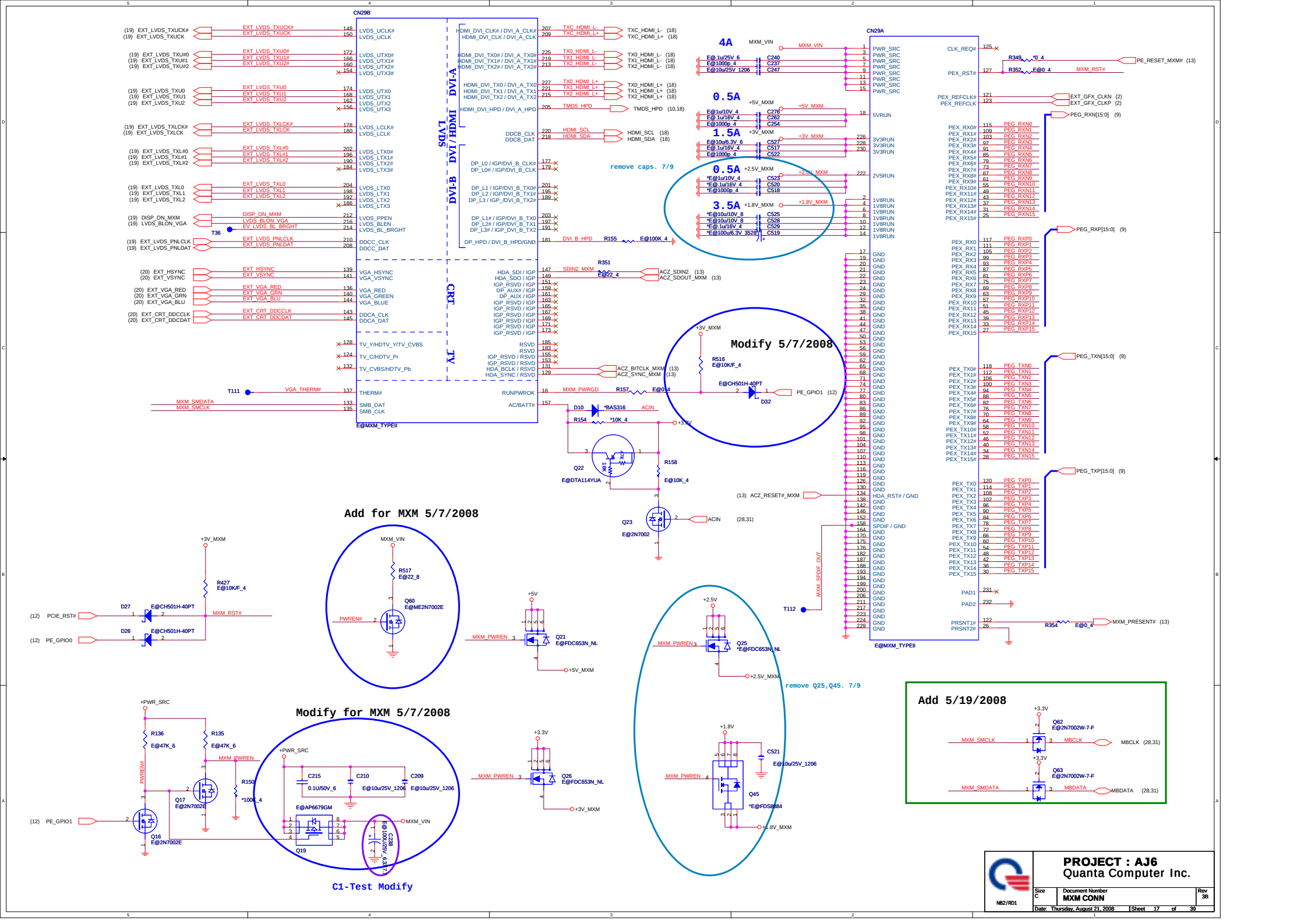
CN29B
LVDS
DVI-A
DVI / HDMI
DVI-B
CRT
TV
EXT_LVDS_TXUCK#
EXT_LVDS_TXUCK
EXT_LVDS_TXU#0
EXT_LVDS_TXU#1
EXT_LVDS_TXU#2
EXT_LVDS_TXU0
EXT_LVDS_TXU1
EXT_LVDS_TXU2
EXT_LVDS_TXLCK#
EXT_LVDS_TXLCK
EXT_LVDS_TXL#0
EXT_LVDS_TXL#1
EXT_LVDS_TXL#2
EXT_LVDS_TXL0
EXT_LVDS_TXL1
EXT_LVDS_TXL2
DISP_ON_MXM
LVDS_BLON_VGA
EV_LVDS_BL_BRGHT
EXT_LVDS_PNLCLK
EXT_LVDS_PNLDAT
EXT_HSYNC
EXT_VSYNC
EXT_VGA_RED
EXT_VGA_GRN
EXT_VGA_BLU
EXT_CRT_DDCCLK
EXT_CRT_DDCDAT
VGA_THERM#
MXM_SMDATA
MXM_SMCLK
LVDS_UCLK#
LVDS_UCLK
LVDS_UTX0#
LVDS_UTX1#
LVDS_UTX2#
LVDS_UTX3#
LVDS_UTX0
LVDS_UTX1
LVDS_UTX2
LVDS_UTX3
LVDS_LCLK#
LVDS_LCLK
LVDS_LTX0#
LVDS_LTX1#
LVDS_LTX2#
LVDS_LTX3#
LVDS_LTX0
LVDS_LTX1
LVDS_LTX2
LVDS_LTX3
LVDS_PPEN
LVDS_BLEN
LVDS_BL_BRGHT
DDCC_CLK
DDCC_DAT
VGA_HSYNC
VGA_VSYNC
VGA_RED
VGA_GREEN
VGA_BLUE
DDCA_CLK
DDCA_DAT
TV_Y/HDTV_Y/TV_CVBS
TV_C/HDTV_Pr
TV_CVBS/HDTV_Pb
THERM#
SMB_DAT
SMB_CLK
E@MXM_TYPEII
HDMI_DVI_CLK# / DVI_A_CLK#
HDMI_DVI_CLK / DVI_A_CLK
HDMI_DVI_TX0# / DVI_A_TX0#
HDMI_DVI_TX1# / DVI_A_TX1#
HDMI_DVI_TX2# / DVI_A_TX2#
HDMI_DVI_TX0 / DVI_A_TX0
HDMI_DVI_TX1 / DVI_A_TX1
HDMI_DVI_TX2 / DVI_A_TX2
HDMI_DVI_HPD / DVI_A_HPD
DDCB_CLK
DDCB_DAT
DP_L0 / IGP/DVI_B_CLK#
DP_L0# / IGP/DVI_B_CLK
DP_L1 / IGP/DVI_B_TX0#
DP_L2 / IGP/DVI_B_TX1#
DP_L3 / IGP_/DVI_B_TX2#
DP_L1# / IGP/DVI_B_TX0
DP_L2# / IGP/DVI_B_TX1
DP_L3# / IGP_DVI_B_TX2
DP_HPD / DVI_B_HPD/GND
HDA_SDI / IGP
HDA_SDO / IGP
IGP_RSVD / IGP
DP_AUX# / IGP
DP_AUX / IGP
IGP_RSVD / IGP
IGP_RSVD / IGP
IGP_RSVD / IGP
IGP_RSVD / IGP
IGP_RSVD / IGP
IGP_RSVD / IGP
RSVD
RSVD
IGP_RSVD / RSVD
IGP_RSVD / RSVD
HDA_BCLK / RSVD
HDA_SYNC / RSVD
RUNPWROK
AC/BATT#
TXC_HDMI_L-
TXC_HDMI_L+
TX0_HDMI_L-
TX1_HDMI_L-
TX2_HDMI_L-
TX0_HDMI_L+
TX1_HDMI_L+
TX2_HDMI_L+
TMDS_HPD
HDMI_SCL
HDMI_SDA
DVI_B_HPD
SDIN2_MXM
ACZ_BITCLK_MXM
ACZ_SYNC_MXM
MXM_PWRGD
ACIN
remove caps. 7/9
CN29A
4A
MXM_VIN
E@1u/25V_6
E@1000p_4
E@10u/25V_1206
C240
C237
C247
0.5A
+5V_MXM
E@1u/10V_4
E@1u/16V_4
E@1000p_4
C276
C262
C254
1.5A
+3V_MXM
E@10u/6.3V_6
E@1u/16V_4
E@1000p_4
C527
C517
C522
0.5A
+2.5V_MXM
*E@1u/10V_4
*E@1u/16V_4
*E@1000p_4
C523
C520
C518
3.5A
+1.8V_MXM
*E@10u/10V_8
*E@10u/10V_8
*E@1u/16V_4
*E@100u/6.3V_3528
C525
C528
C529
C519
PWR_SRC
5VRUN
3V3RUN
2V5RUN
1V8RUN
GND
SPDIF / GND
HDA_RST# / GND
CLK_REQ#
PEX_RST#
PEX_REFCLK#
PEX_REFCLK
PEX_RX0#
PEX_RX1#
PEX_RX2#
PEX_RX3#
PEX_RX4#
PEX_RX5#
PEX_RX6#
PEX_RX7#
PEX_RX8#
PEX_RX9#
PEX_RX10#
PEX_RX11#
PEX_RX12#
PEX_RX13#
PEX_RX14#
PEX_RX15#
PEG_RXN0
PEG_RXN1
PEG_RXN2
PEG_RXN3
PEG_RXN4
PEG_RXN5
PEG_RXN6
PEG_RXN7
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PEG_RXP11
PEG_RXP12
PEG_RXP13
PEG_RXP14
PEG_RXP15
PEG_TXN0
PEG_TXN1
PEG_TXN2
PEG_TXN3
PEG_TXN4
PEG_TXN5
PEG_TXN6
PEG_TXN7
PEG_TXN8
PEG_TXN9
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PEG_TXP6
PEG_TXP7
PEG_TXP8
PEG_TXP9
PEG_TXP10
PEG_TXP11
PEG_TXP12
PEG_TXP13
PEG_TXP14
PEG_TXP15
PAD1
PAD2
PRSNT1#
PRSNT2#
PE_RESET_MXM#
MXM_RST#
EXT_GFX_CLKN
EXT_GFX_CLKP
MXM_PRESENT#
MXM_SPDIF_OUT
Modify 5/7/2008
R516
E@10K/F_4
D32
E@CH501H-40PT
PE_GPIO1
R157
E@0_4
D10
*BAS316
R154
*10K_4
Q22
E@DTA114YUA
R158
E@10K_4
Q23
E@2N7002
ACIN
ACZ_RESET#_MXM
T112
Add for MXM 5/7/2008
R427
E@10K/F_4
D27
D26
PCIE_RST#
PE_GPIO0
MXM_RST#
R517
E@22_8
Q60
E@ME2N7002E
PWREN#
Q21
E@FDC653N_NL
MXM_PWREN
remove Q25,Q45. 7/9
Q25
*E@FDC653N_NL
Modify for MXM 5/7/2008
R136
E@47K_6
R135
E@47K_6
Q17
E@2N7002E
R150
*100K_4
Q16
E@2N7002E
C215
0.1U/50V_6
C210
E@10u/25V_1206
C209
E@10u/25V_1206
E@AP6679GM
Q19
C208
E@1000u/6.3V_6.3*7.7
Q26
E@FDC653N_NL
C521
E@10u/25V_1206
Q45
*E@FDS8884
Add 5/19/2008
Q62
E@2N7002W-7-F
MXM_SMCLK
MBCLK
MBCLK (28,31)
Q63
E@2N7002W-7-F
MXM_SMDATA
MBDATA
MBDATA (28,31)
C1-Test Modify
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size C
Document Number
MXM CONN
Rev 3B
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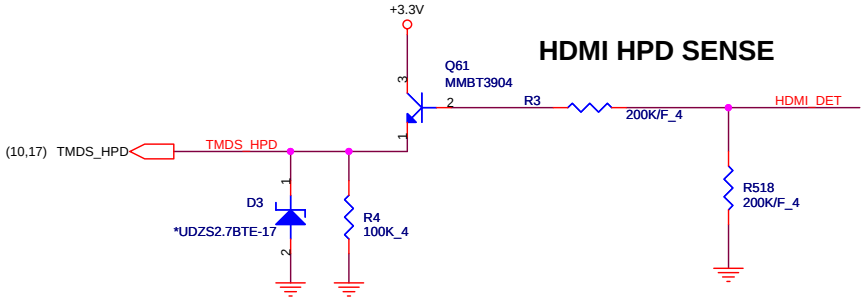
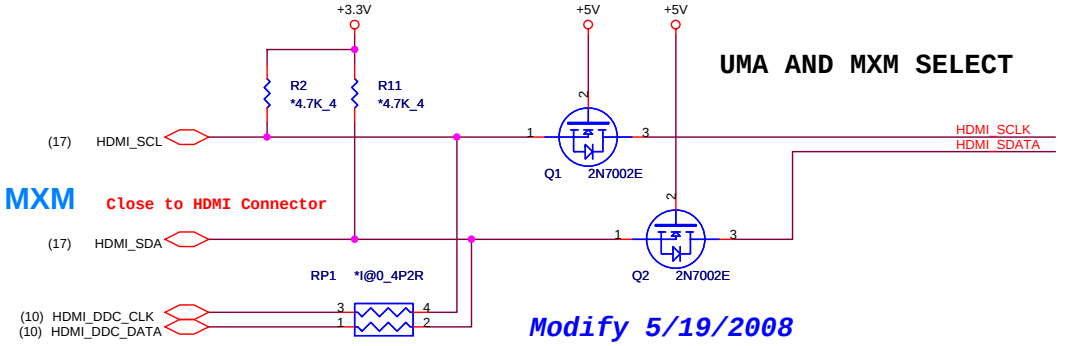
HDMI HPD SENSE



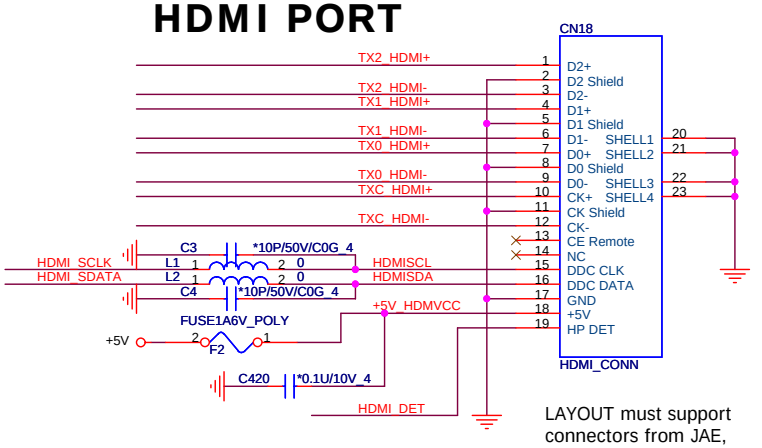
Modify 5/19/2008

UMA AND MXM SELECT



Modify 5/19/2008

HDMI PORT



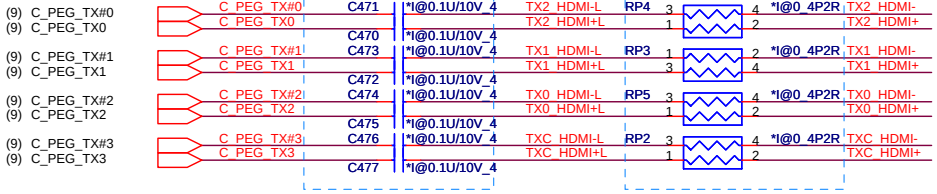
LAYOUT must support connectors from JAE, Molex, and Acon

Modify 5/26/2008

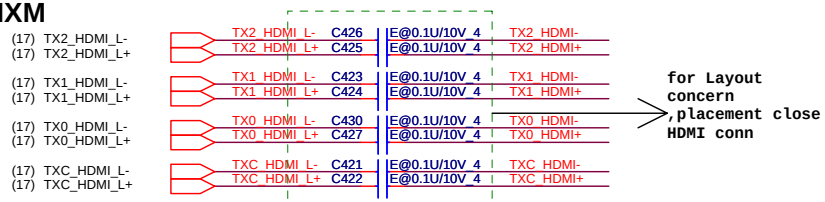
From RS780M

for Layout concern ,placement close north bridge

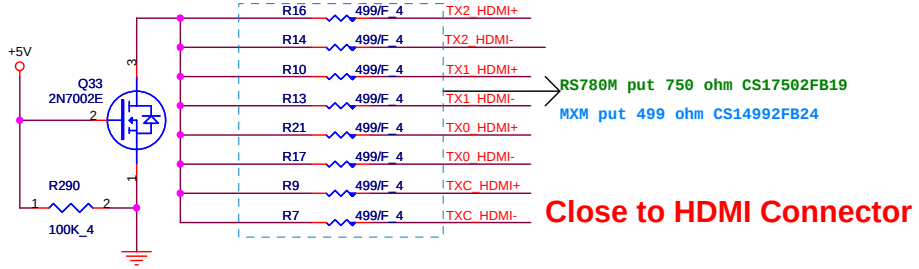
for Layout concern ,placement close HDMI conn



MXM



for Layout concern ,placement close HDMI conn

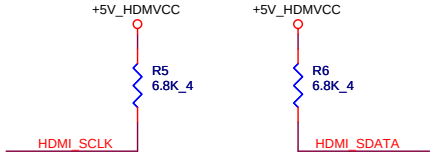


RS780M put 750 ohm CS17502FB19

MXM put 499 ohm CS14992FB24

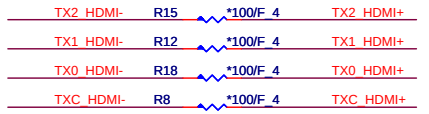
Close to HDMI Connector

Modify 5/19/2008



Close to HDMI Connector

DDC4 is 5V tolerance , the MOSFET level shifter no need



RS780: Pulled up to +5.0 V on the Northbridge side with a 4.7k 5% resistor

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

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B	HDMI CONN	2A
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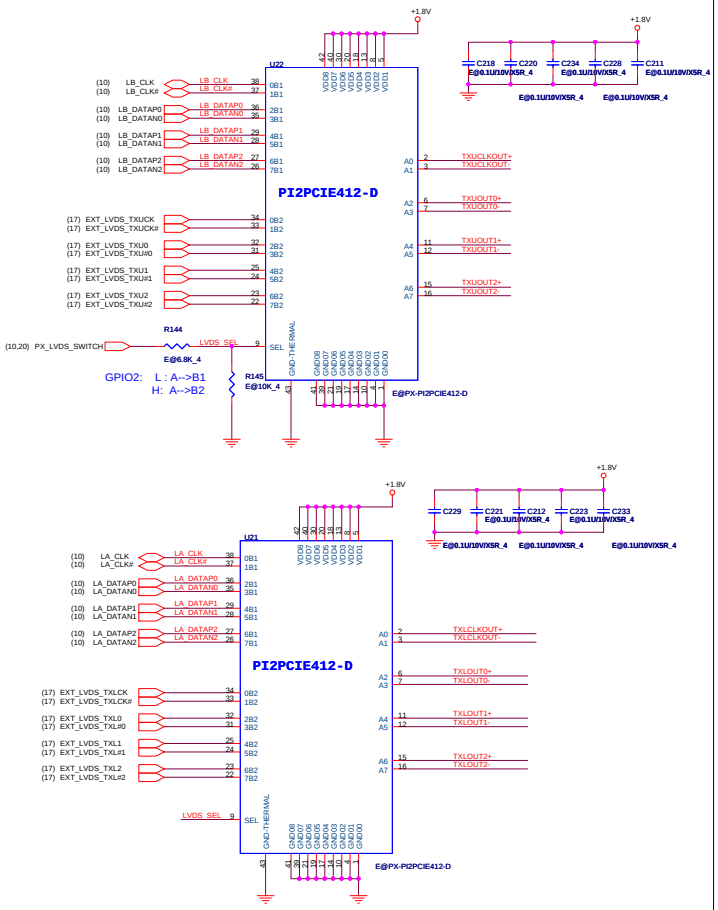
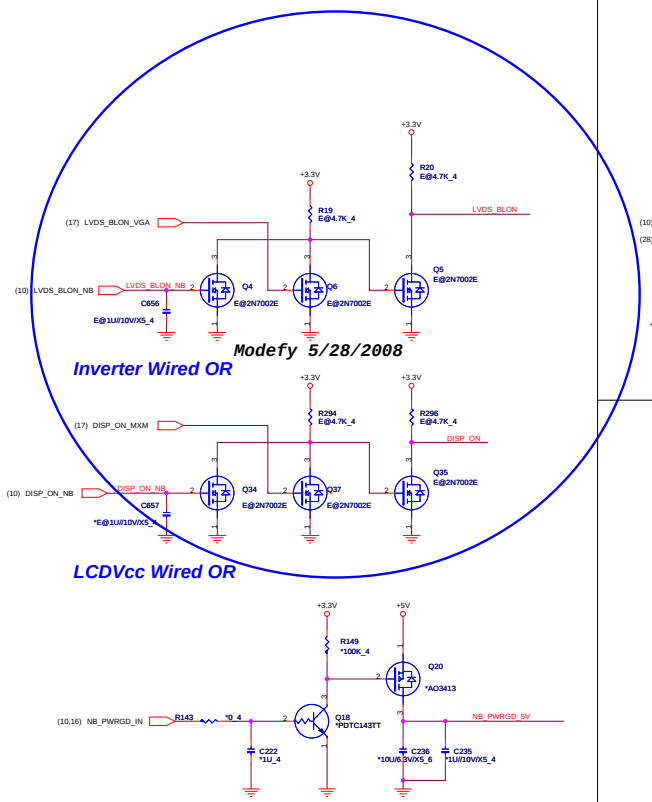


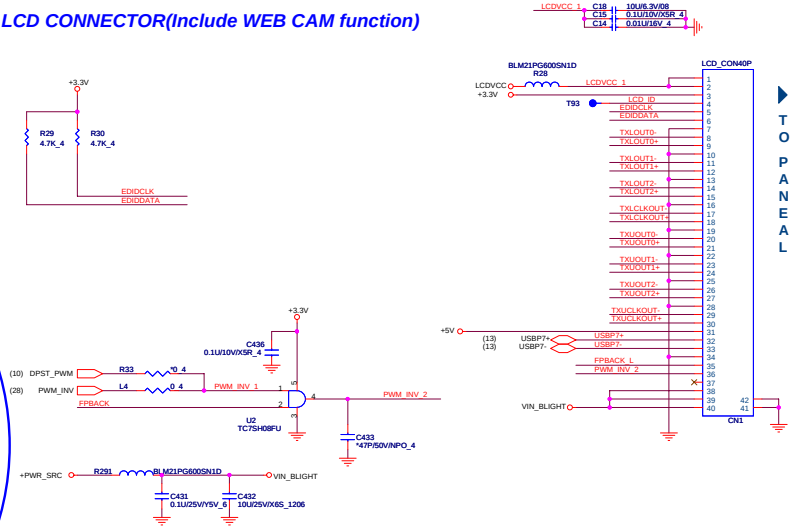


Modefy 5/28/2008

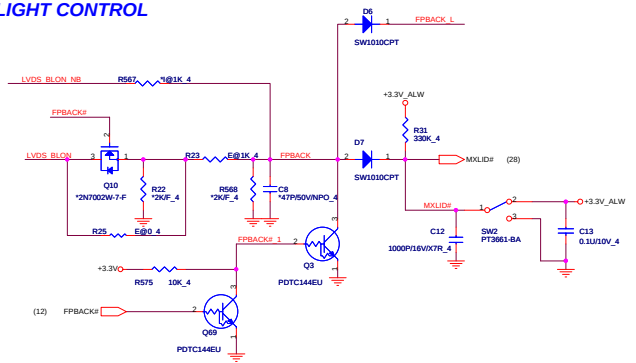
Inverter Wired OR

LCDVcc Wired OR

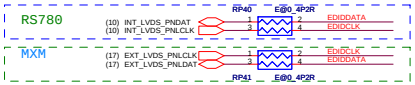
LCD CONNECTOR(Include WEB CAM function)



BACKLIGHT CONTROL

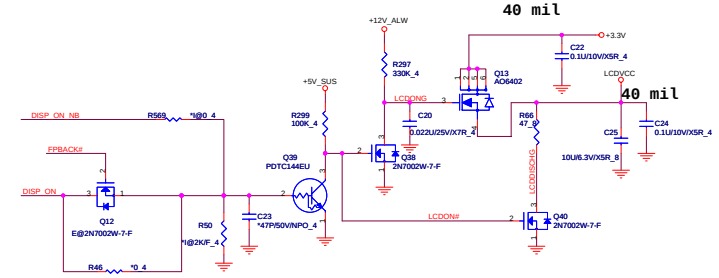


Close to NB & VGA between



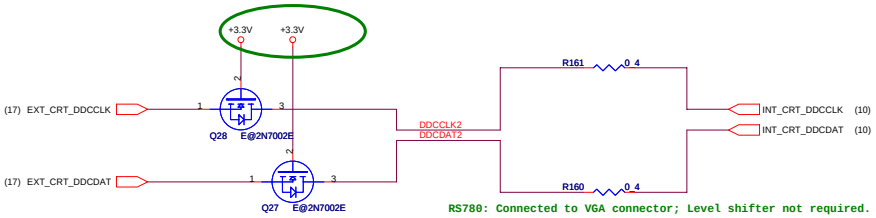
Close to NB & VGA between

PANEL VCC CONTROL

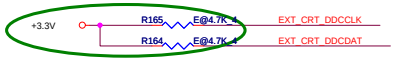


NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.	
Size: Custom	Document Number: LCD CONN & MUX	Rev: 3A
Date: Thursday, August 21, 2008	Sheet 19 of 39	

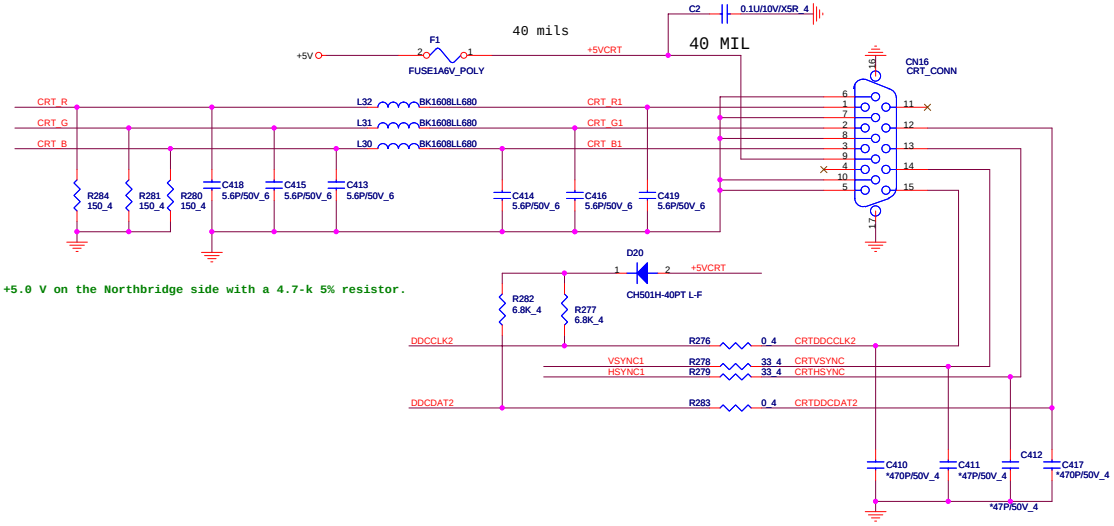
CRT PORT



RS780: Connected to VGA connector; Level shifter not required.

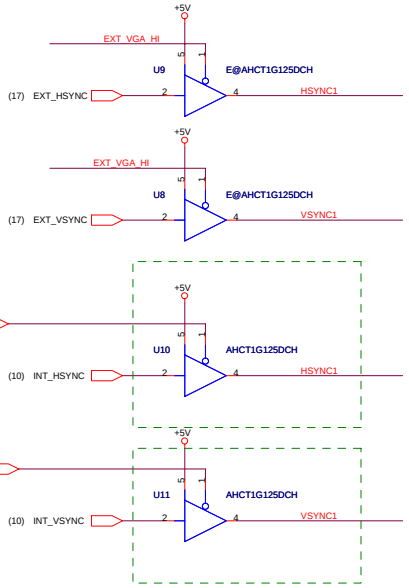


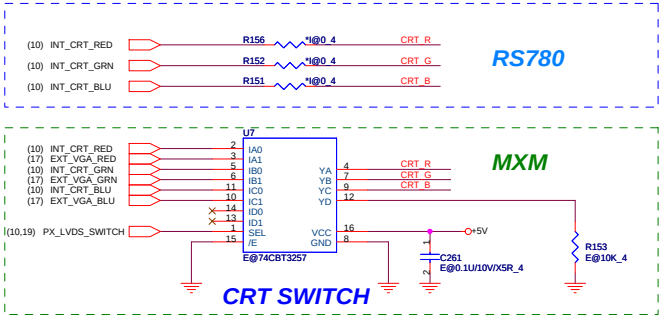
	RS780	Hybrid
Q28,Q27	X	V
R165,R164	X	V



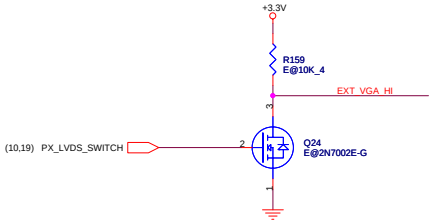
RS780: Pulled up to +5.0 V on the Northbridge side with a 4.7-k 5% resistor.

U9/U8 FOR RS780 ONLY
U8/U9/U10/U11 FOR RS780+MXM HYBRID





inputs		function
/E	SET	
L	L	Y - port 0
L	H	Y - port 1
H	X	Disconnect



PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
C	CRT CONN & MUX	1A

NB2/RD1

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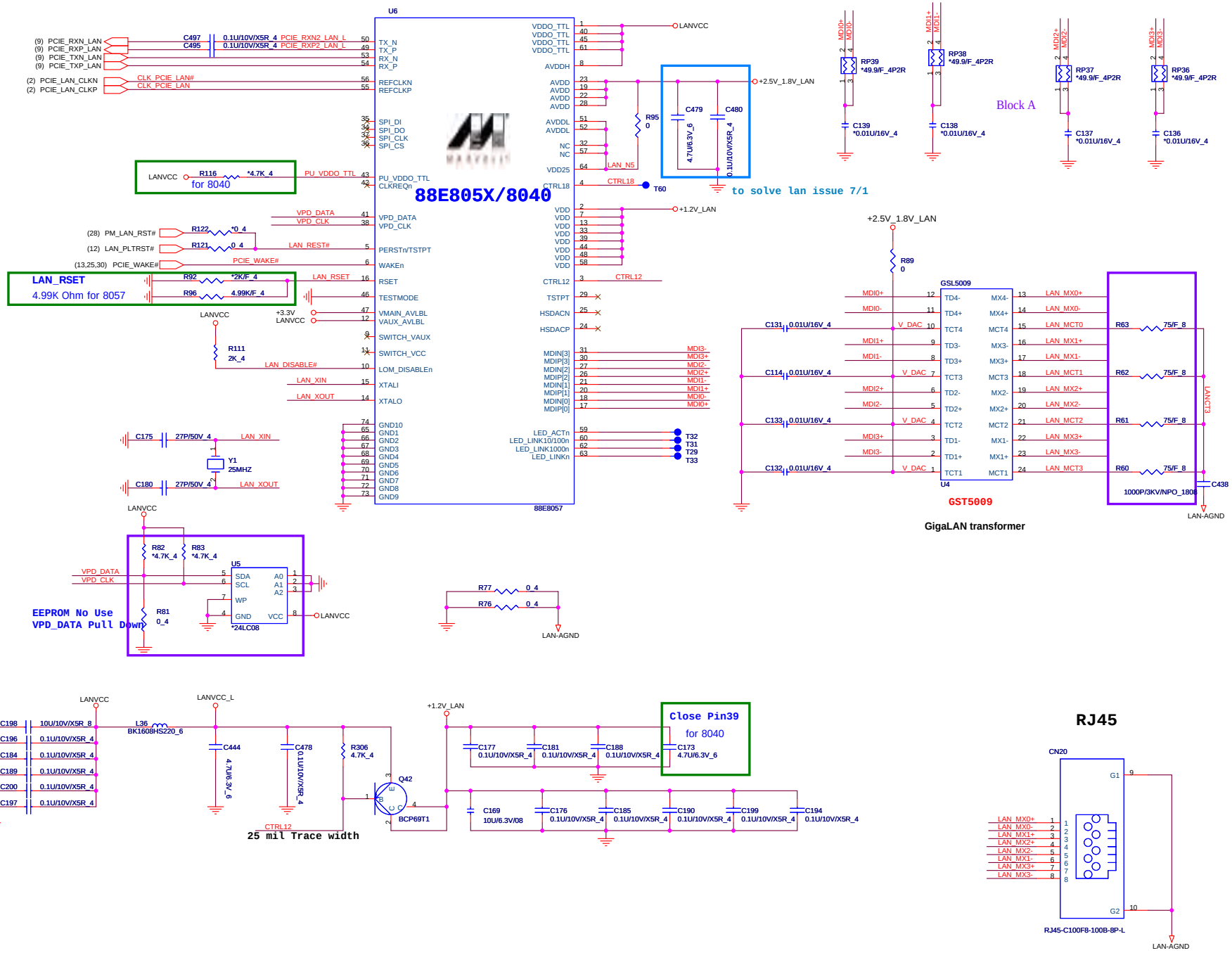
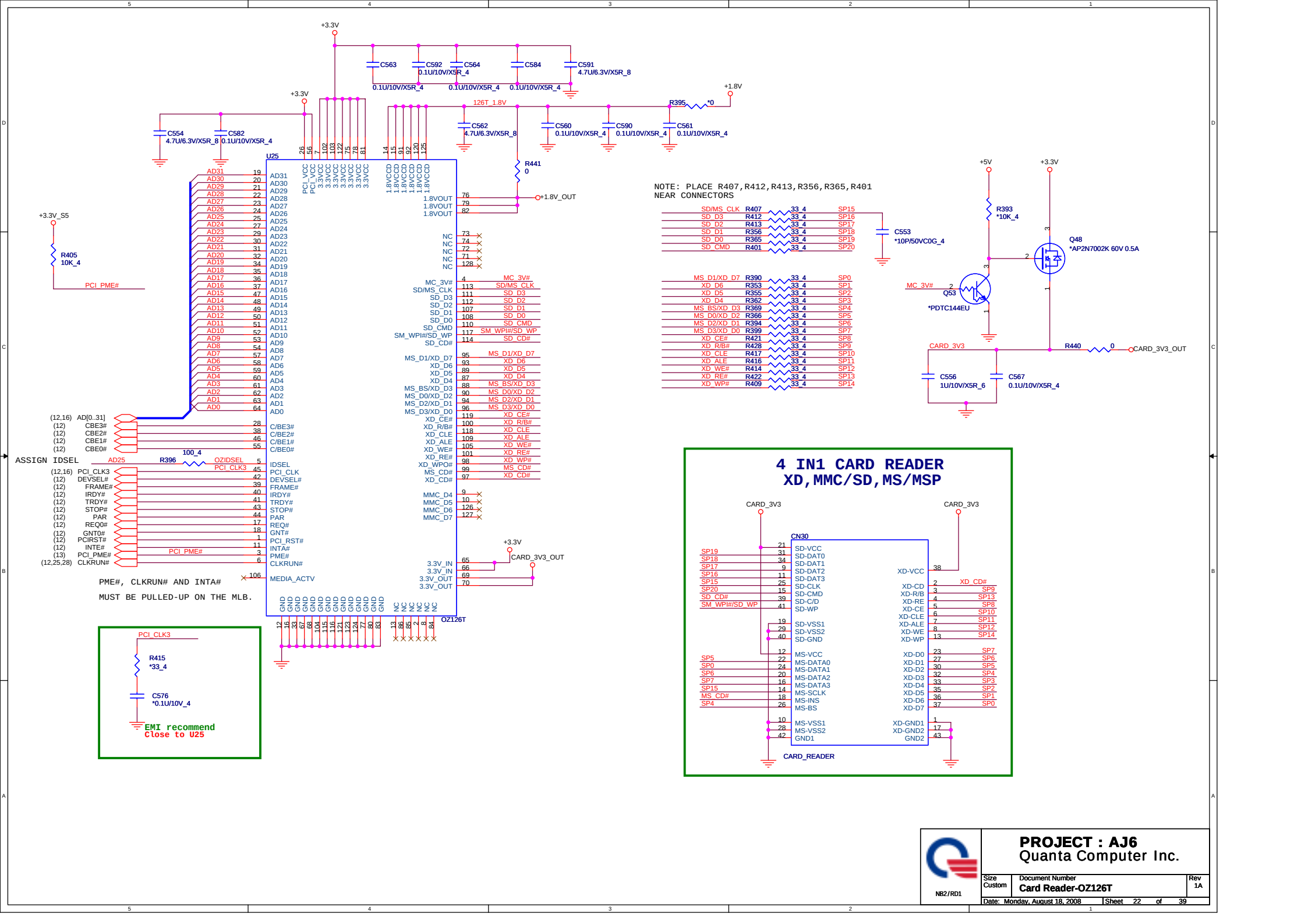
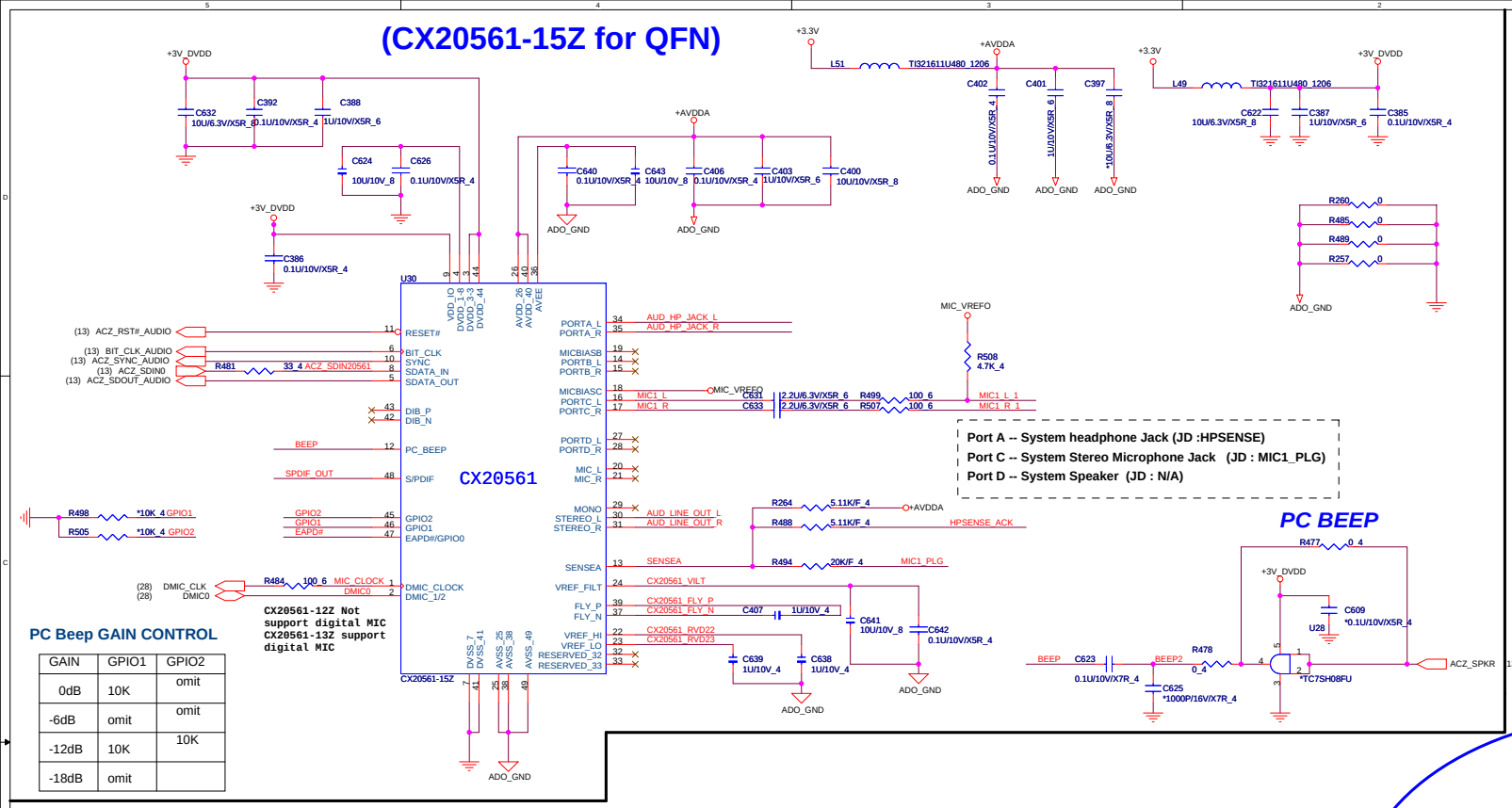


NB2/RD1	PROJECT : AJ6 Quanta Computer Inc.	
Size: Custom	Document Number: LAN(Marvell 88E8040&55)	Rev: 3A
Date: Thursday, August 21, 2008	Sheet 21 of 39	


+3.3V
C563
C592
0.1U/10V/X5R_4
C564
C584
C591
4.7U/6.3V/X5R_8
+1.8V
R395
*0
126T_1.8V
C554
4.7U/6.3V/X5R_8
C582
0.1U/10V/X5R_4
C562
C560
C590
C561
U25
R441
0
+1.8V_OUT
NOTE: PLACE R407,R412,R413,R356,R365,R401
NEAR CONNECTORS
+3.3V_S5
R405
10K_4
PCI_PME#
SD/MS_CLK R407 33_4 SP15
SD_D3 R412 33_4 SP16
SD_D2 R413 33_4 SP17
SD_D1 R356 33_4 SP18
SD_D0 R365 33_4 SP19
SD_CMD R401 33_4 SP20
C553
*10P/50VC0G_4
MS_D1/XD_D7 R390 33_4 SP0
XD_D6 R353 33_4 SP1
XD_D5 R355 33_4 SP2
XD_D4 R362 33_4 SP3
MS_BS/XD_D3 R369 33_4 SP4
MS_D0/XD_D2 R366 33_4 SP5
MS_D2/XD_D1 R394 33_4 SP6
MS_D3/XD_D0 R399 33_4 SP7
XD_CE# R421 33_4 SP8
XD_R/B# R428 33_4 SP9
XD_CLE R417 33_4 SP10
XD_ALE R416 33_4 SP11
XD_WE# R414 33_4 SP12
XD_RE# R422 33_4 SP13
XD_WP# R409 33_4 SP14
+5V
+3.3V
R393
*10K_4
Q48
*AP2N7002K 60V 0.5A
MC_3V#
Q53
*PDTC144EU
CARD_3V3
R440
0
CARD_3V3_OUT
C556
1U/10V/X5R_6
C567
0.1U/10V/X5R_4
(12,16) AD[0..31]
(12) CBE3#
(12) CBE2#
(12) CBE1#
(12) CBE0#
ASSIGN IDSEL
AD25
R396
100_4
OZIDSEL
PCI_CLK3
(12,16) PCI_CLK3
(12) DEVSEL#
(12) FRAME#
(12) IRDY#
(12) TRDY#
(12) STOP#
(12) PAR
(12) REQ0#
(12) GNT0#
(12) PCIRST#
(12) INTE#
(13) PCI_PME#
(12,25,28) CLKRUN#
PME#, CLKRUN# AND INTA#
MUST BE PULLED-UP ON THE MLB.
MEDIA_ACTV
OZ126T
PCI_CLK3
R415
*33_4
C576
*0.1U/10V_4
EMI recommend
Close to U25
4 IN1 CARD READER
XD,MMC/SD,MS/MSP
CARD_3V3
CN30
SD-VCC
SD-DAT0
SD-DAT1
SD-DAT2
SD-DAT3
SD-CLK
SD-CMD
SD-C/D
SD-WP
SD-VSS1
SD-VSS2
SD-GND
MS-VCC
MS-DATA0
MS-DATA1
MS-DATA2
MS-DATA3
MS-SCLK
MS-INS
MS-BS
MS-VSS1
MS-VSS2
GND1
XD-VCC
XD-CD
XD-R/B
XD-RE
XD-CE
XD-CLE
XD-ALE
XD-WE
XD-WP
XD-D0
XD-D1
XD-D2
XD-D3
XD-D4
XD-D5
XD-D6
XD-D7
XD-GND1
XD-GND2
GND2
CARD_READER
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size Custom
Document Number
Card Reader-OZ126T
Rev 1A
Date: Monday, August 18, 2008
Sheet 22 of 39

(CX20561-15Z for QFN)



CX20561-12Z Not support digital MIC
CX20561-13Z support digital MIC

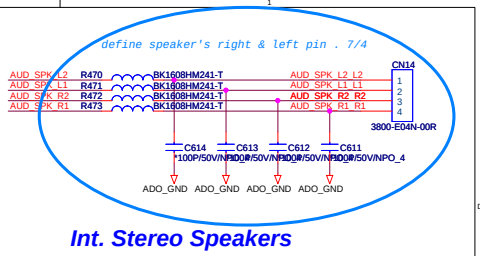
Port A -- System headphone Jack (JD :HPSENSE)
Port C -- System Stereo Microphone Jack (JD : MIC1_PLG)
Port D -- System Speaker (JD : N/A)

PC Beep GAIN CONTROL

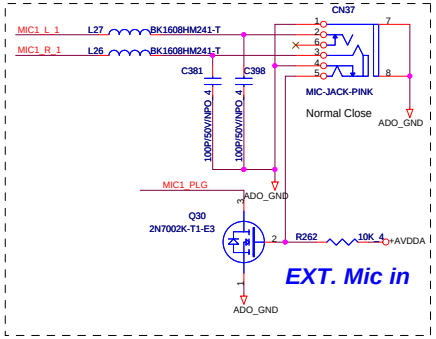
GAIN	GPIO1	GPIO2
0dB	10K	omit
-6dB	omit	omit
-12dB	10K	10K
-18dB	omit	

PC BEEP

Int. Stereo Speakers

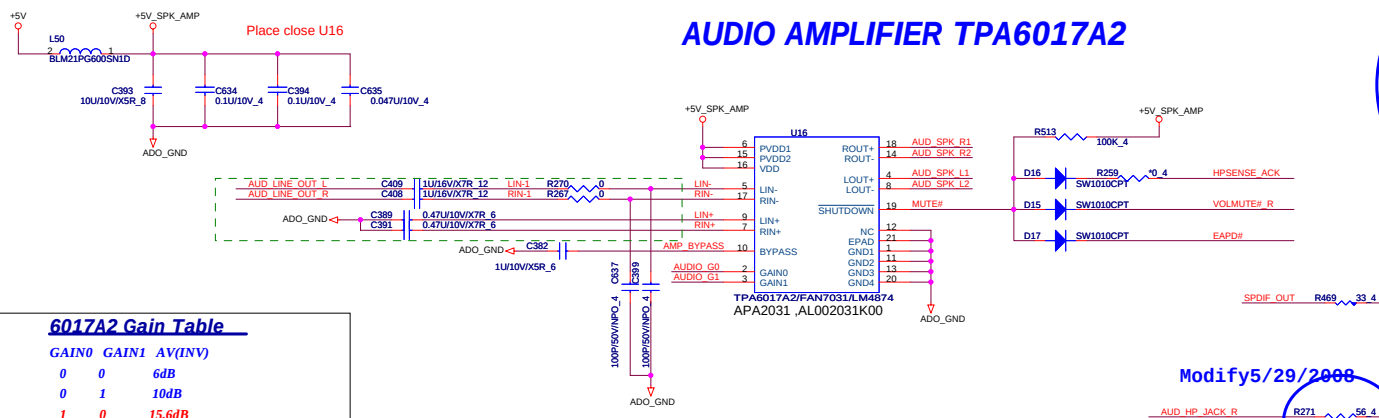


EXT. Mic in



Headphone out + Spdif Out (normal open)

AUDIO AMPLIFIER TPA6017A2

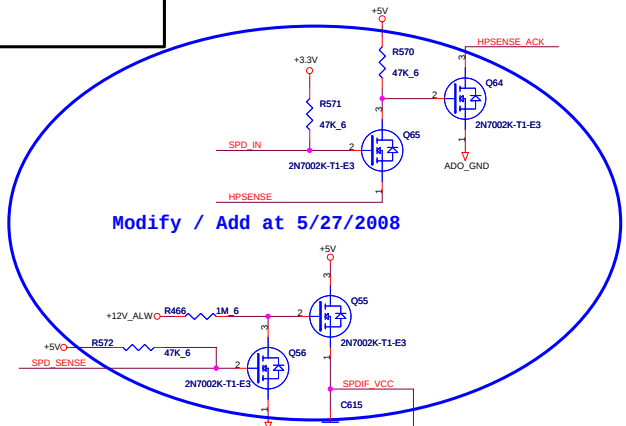


6017A2 Gain Table

GAIN0	GAIN1	AV(INV)
0	0	6dB
0	1	10dB
1	0	15.6dB
1	1	21.6dB

change Gain from 15.6 to 10 db. 7/8

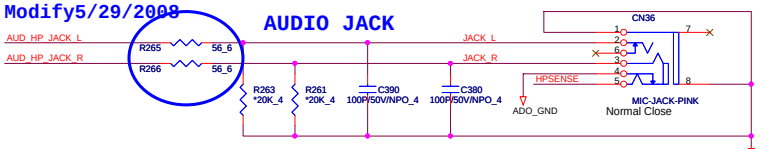
Modify / Add at 5/27/2008



Modify5/29/2008

Modify5/29/2008

AUDIO JACK



PROJECT : AJ6	
Quanta Computer Inc.	
Size: C	Document Number: AUDIO(CX20561)&CONN
Rev: 3A	
NB2/RD1	
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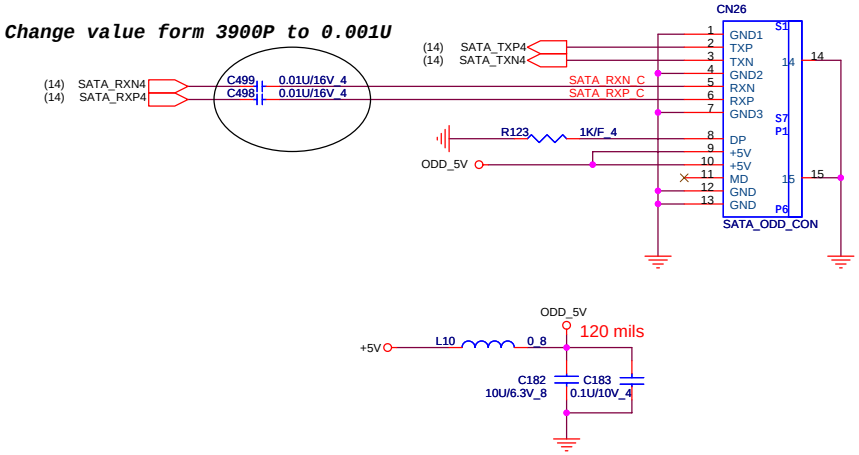
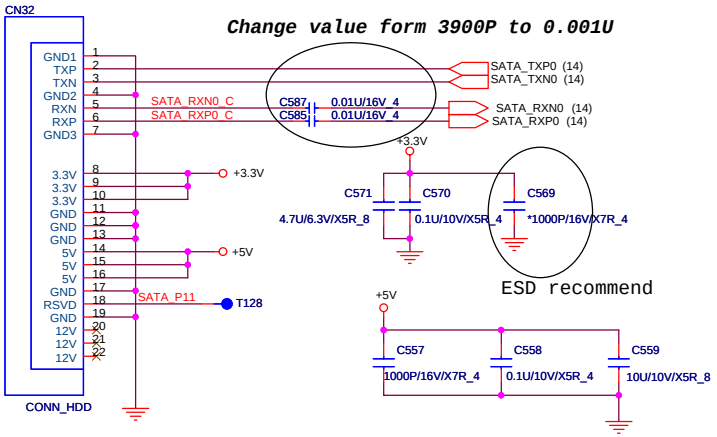
SATA CD-ROM

NEW PART check Pin define

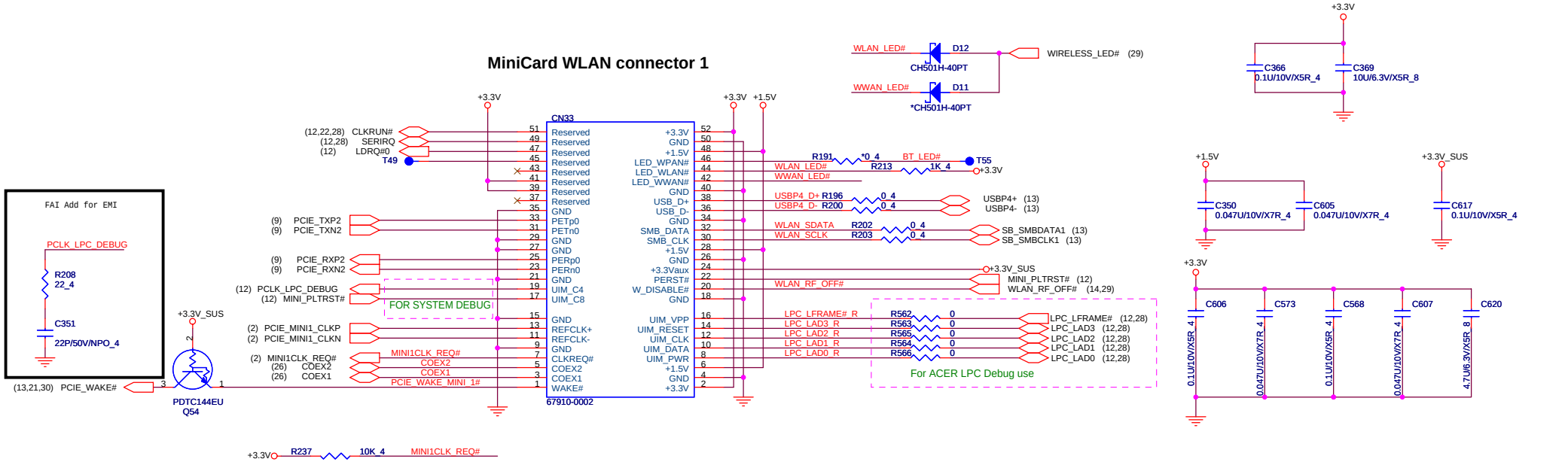


SATA CONNECTOR

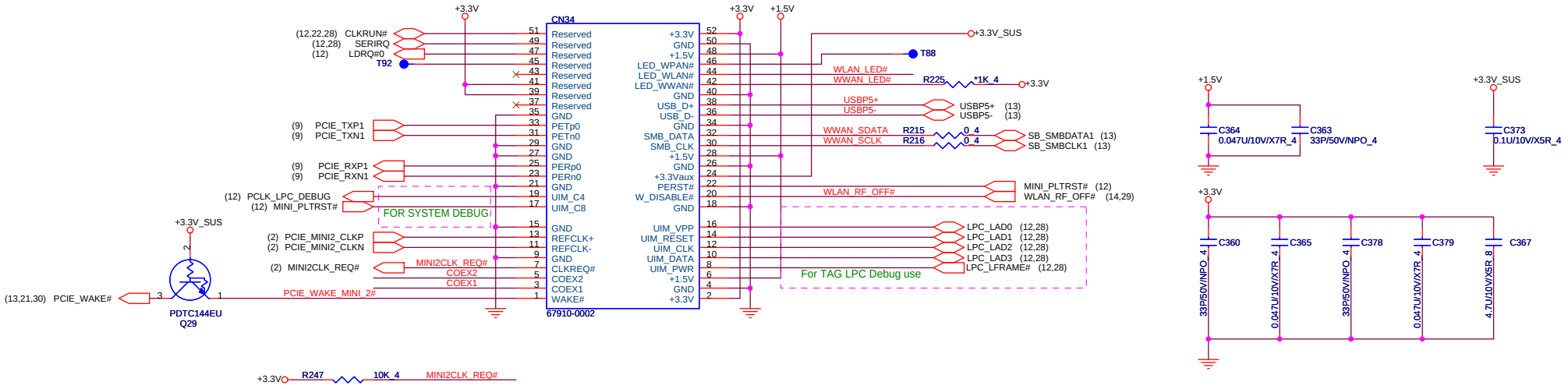


NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **SATA HDD ODD**	Rev: 3A
Date: Monday, August 18, 2008	Sheet 24 of 39	

MiniCard WLAN connector 1

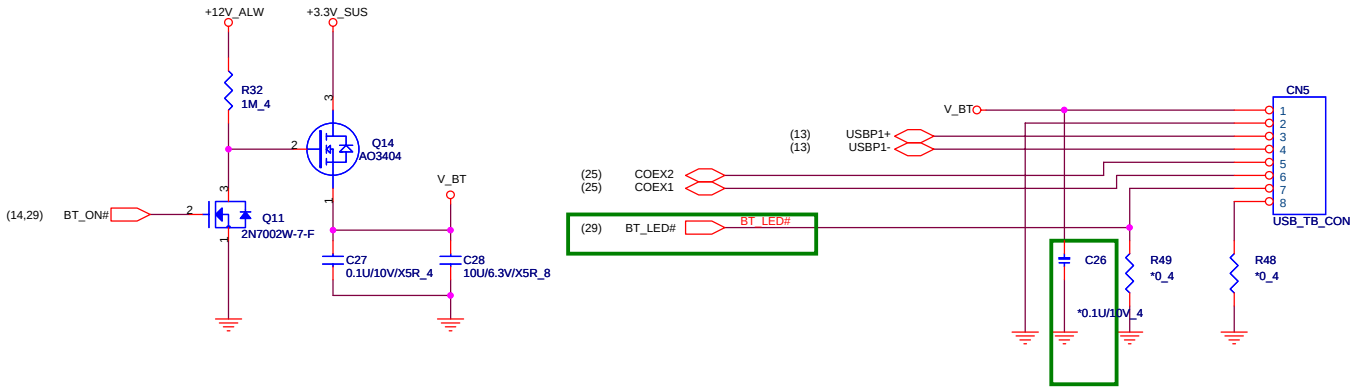


MiniCard connector 2

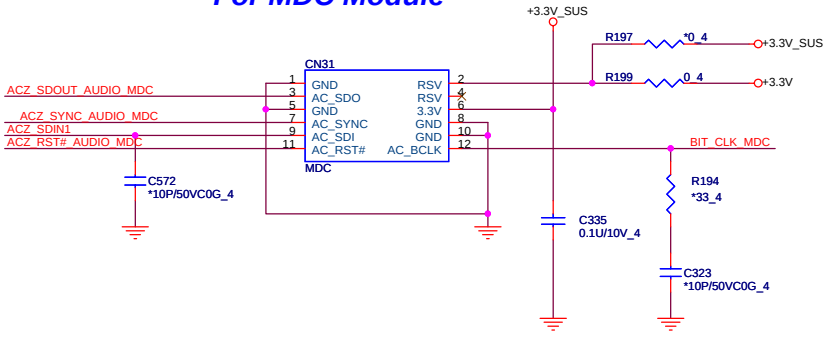


NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **MINI PCI-E Card X2**	Rev: 2A
Date: Monday, August 18, 2008	Sheet 25 of 39	

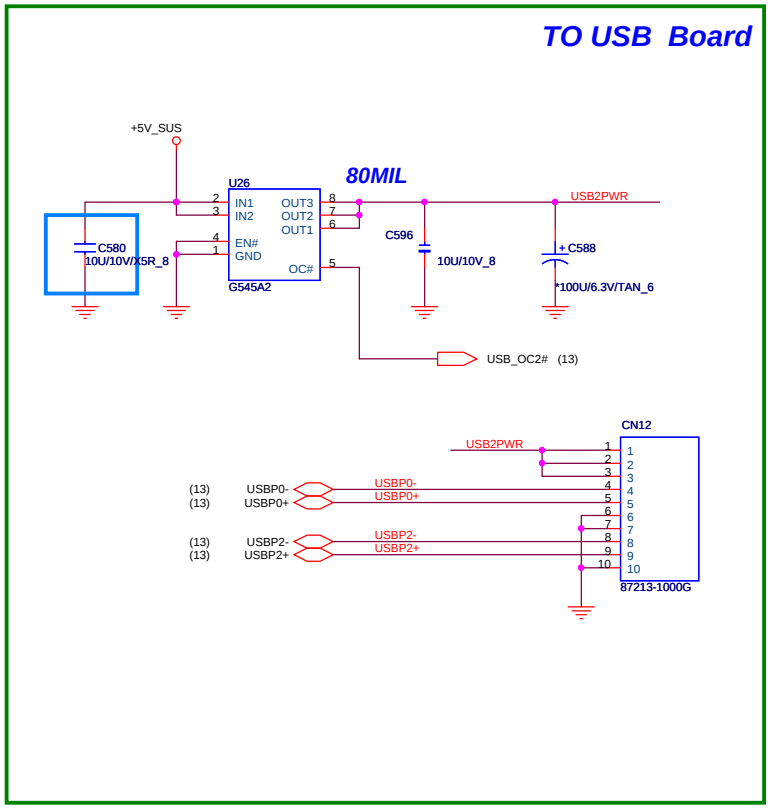
BLUETOOTH CONNECTOR



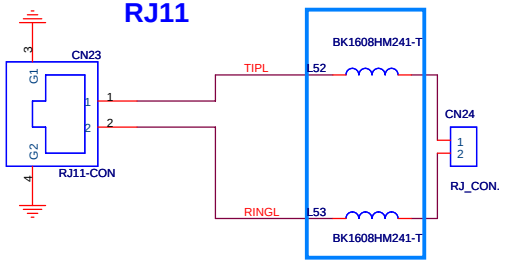
For MDC Module



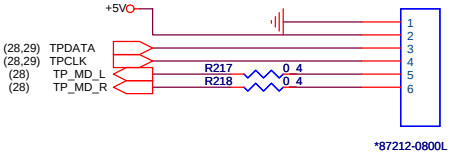
TO USB Board



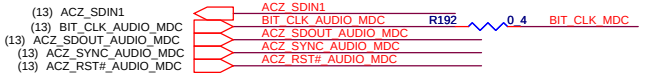
RJ11



TP module CONNECTOR



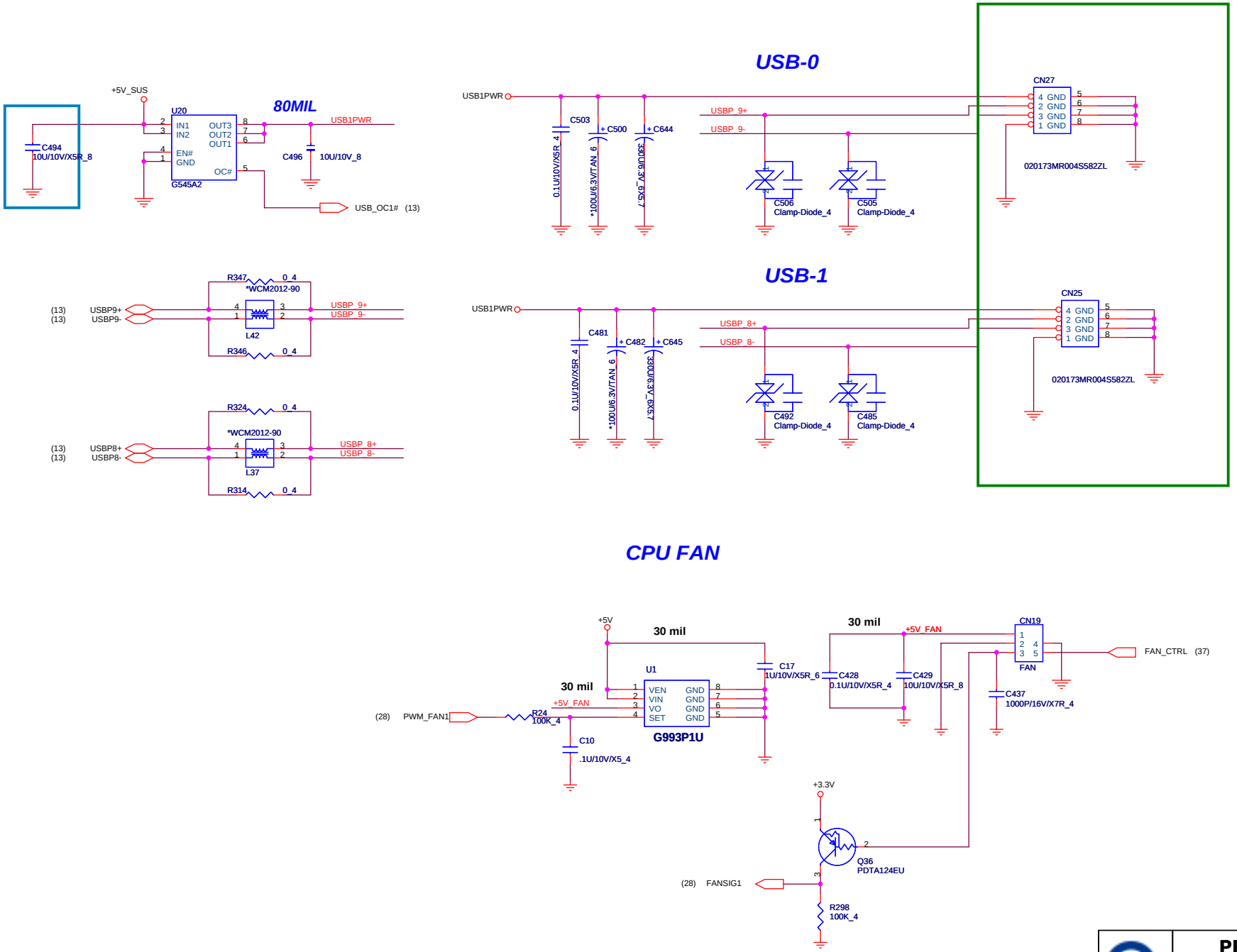
check Footprint & PN



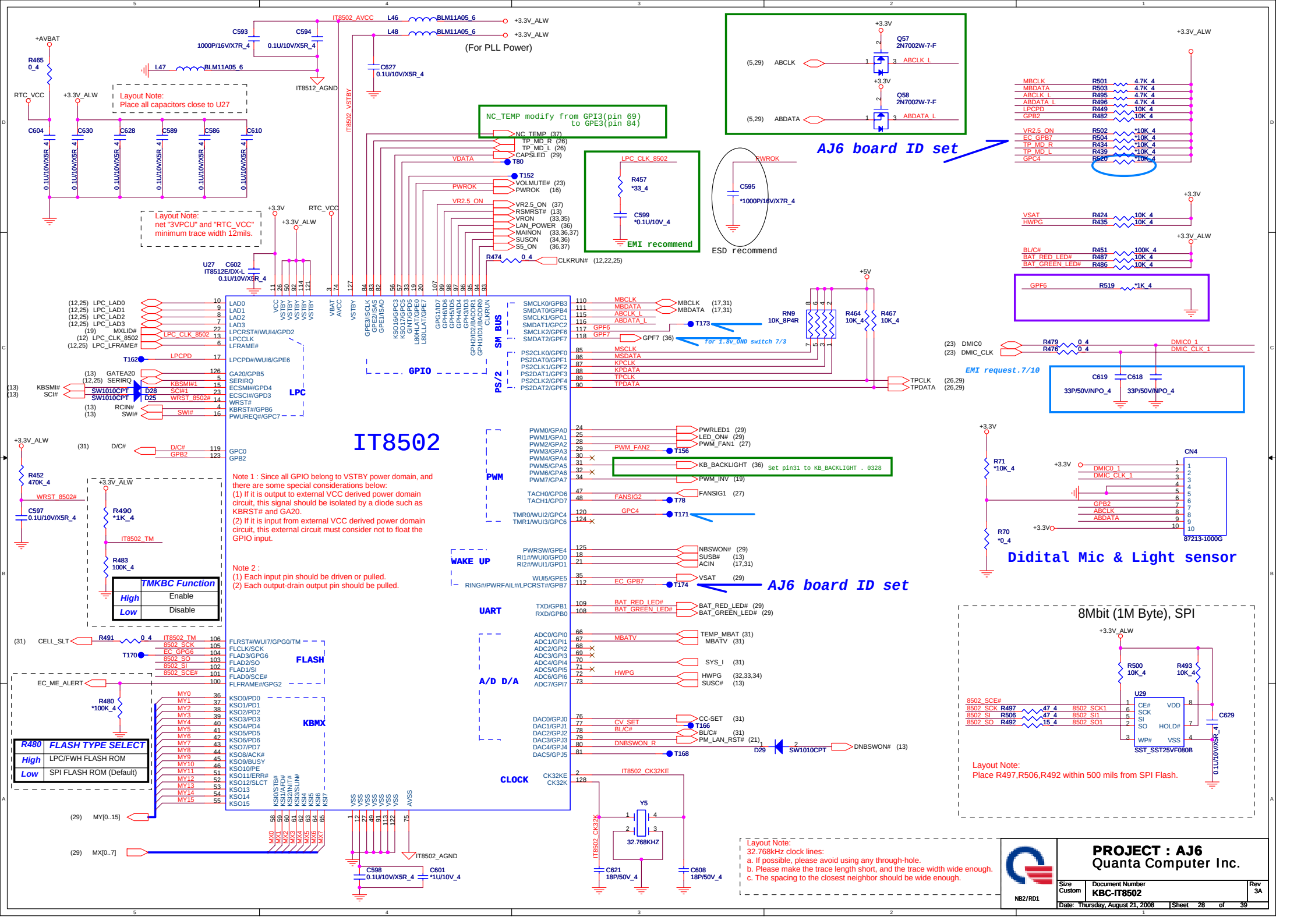
NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Bluetooth,RJ11, MDC,Small/B	3A
Date: Thursday, August 21, 2008	Sheet 26 of 39	



NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **USB CONN X3ports**	Rev: 2A
Date: Monday, August 18, 2008	Sheet 27 of 39	


IT8502
SM BUS
PS/2
GPIO
LPC
PWM
WAKE UP
UART
A/D D/A
CLOCK
FLASH
KBMX
Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.
Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.
Layout Note:
Place all capacitors close to U27
Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.
(For PLL Power)
NC_TEMP modify from GPI3(pin 69)
to GPE3(pin 84)
EMI recommend
ESD recommend
AJ6 board ID set
AJ6 board ID set
EMI request.7/10
for 1.8V_DND switch 7/3
Set pin31 to KB_BACKLIGHT . 0328
Didital Mic & Light sensor
8Mbit (1M Byte), SPI
Layout Note:
Place R497,R506,R492 within 500 mils from SPI Flash.
Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.
TMKBC Function
High Enable
Low Disable
R480 FLASH TYPE SELECT
High LPC/FWH FLASH ROM
Low SPI FLASH ROM (Default)
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Size Custom
Document Number KBC-IT8502
Rev 3A
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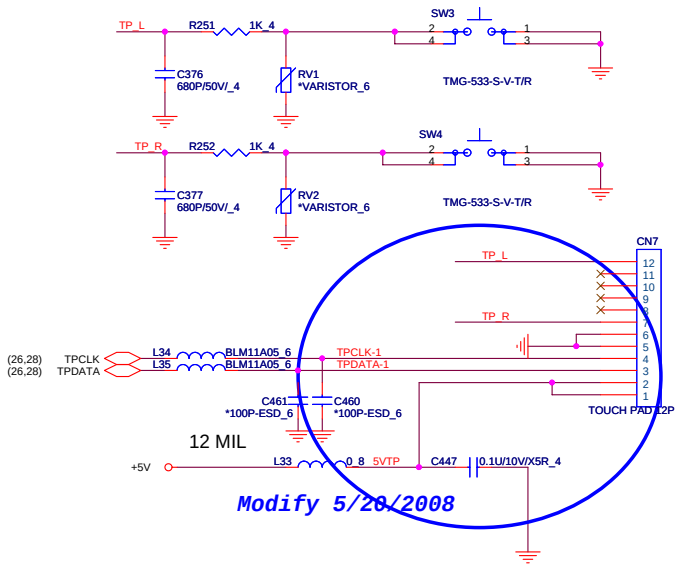
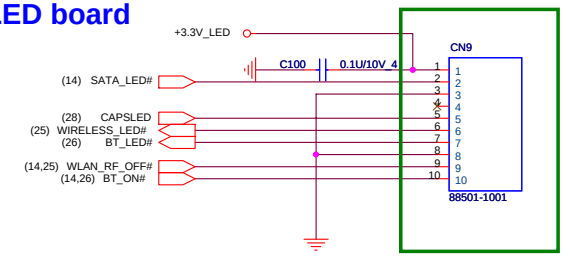
TOUCHPAD SWITCH CONN

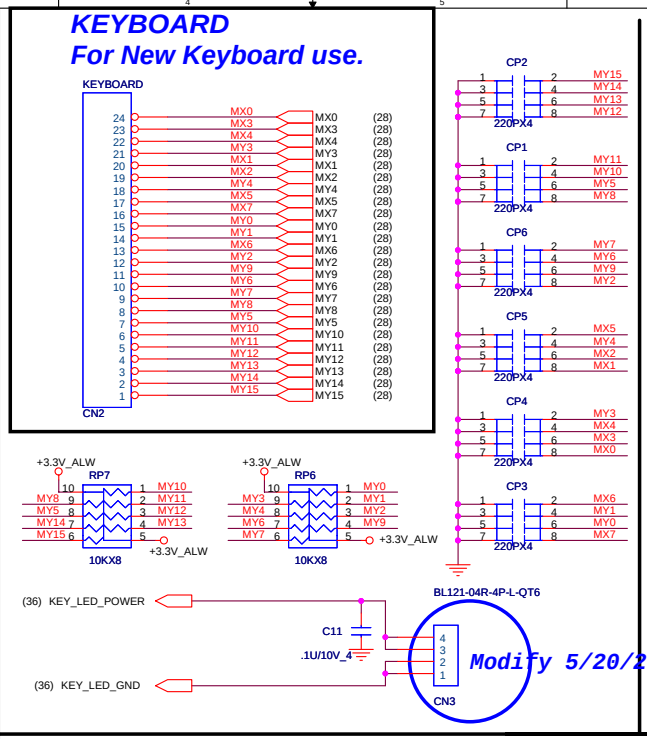


Modify 5/20/2008

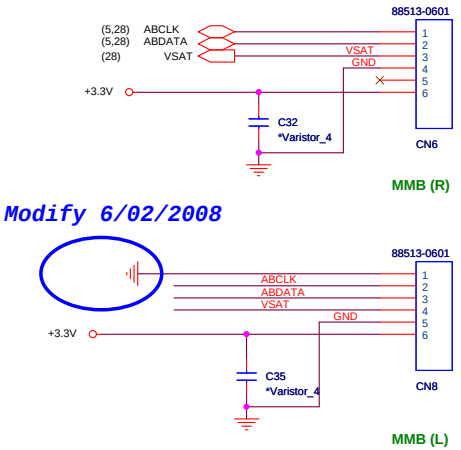
To LED board



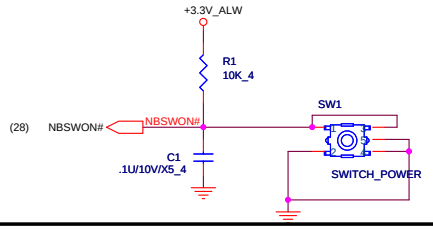
KEYBOARD
For New Keyboard use.



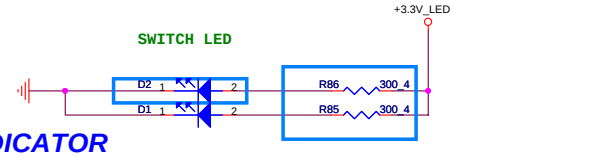
Modify 5/20/2008

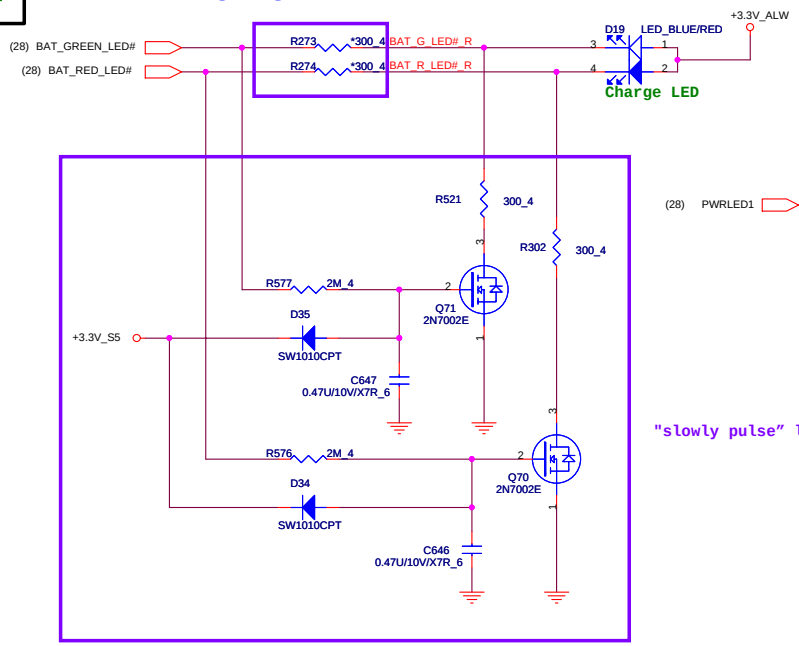


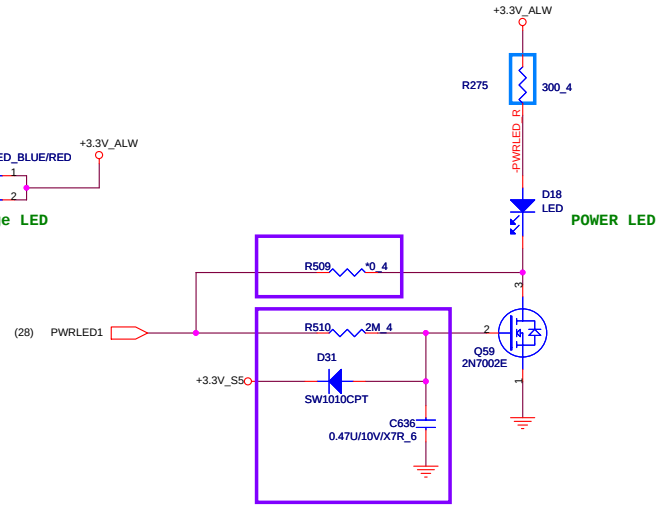
Modify 6/02/2008



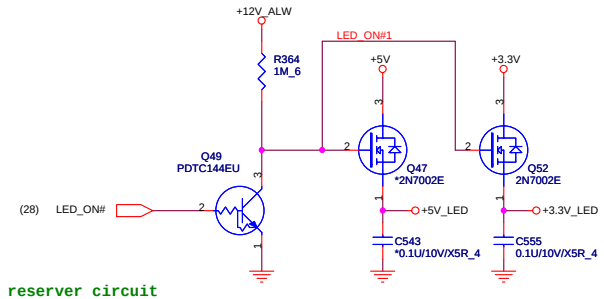
LED INDICATOR



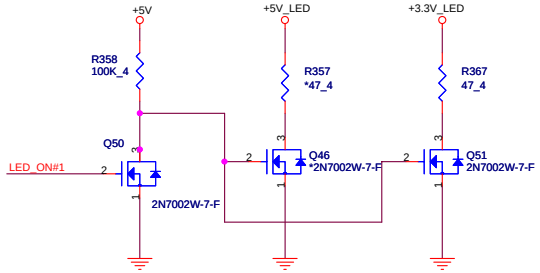




"slowly pulse" light to dark about 2 second ,Modify by 8/18



reserver circuit



NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.		
	Size: Custom	Document Number: TP/KB/LED/SW CONN.	Rev: 3B
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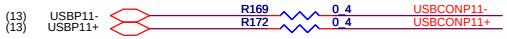
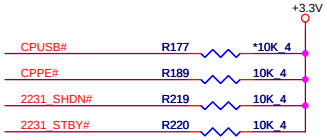
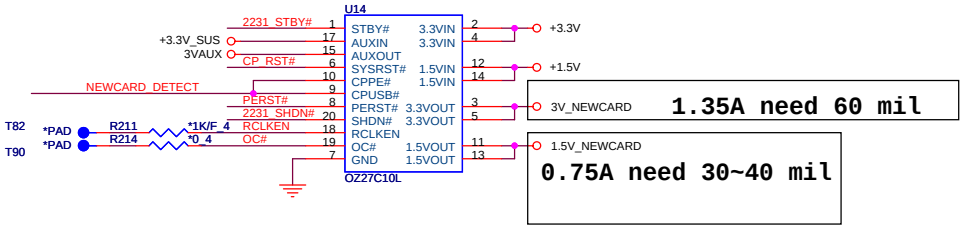
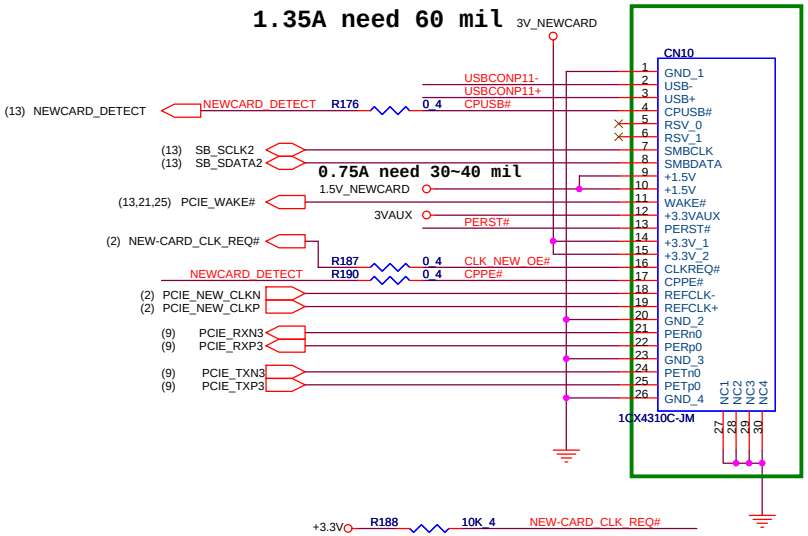
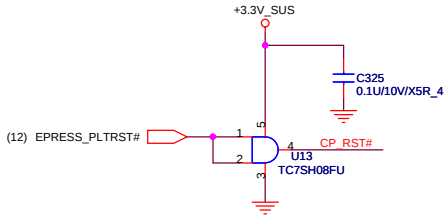
NEWCARD

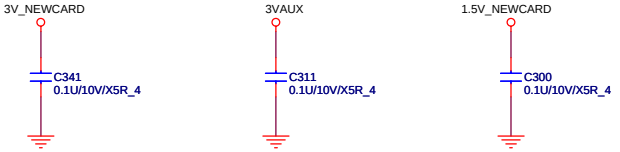












NB2/RD1	**PROJECT : AJ6** Quanta Computer Inc.	
Size: Custom	Document Number: **NEW CARD**	Rev: 1A
Date: Monday, August 18, 2008	Sheet 30 of 39	

BATTERY CHARGER

TOP DC_JACK
MXM 90W (DFPJ05MR006) Blue
UMA 65W (DFPJ05MR007) yellow

Place close to EC,

Modify 8/18/2008

Place these CAPs close to FETs

R1

R2

ADP TYPE	Rhigh	P/N
65W	178K/F_4	CS41782FB11
90W	11K/F_4	CS31102FB11

CELL_SLT = 1 -- 3 S (Cells = GND 3S)
CELL_SLT = 0 -- 4 S (Cells = VDD 4S)

Setting the Vin min to 12V
For ACSET 1.26V

Setting the Vin min to 17V
For EN = 1.06V

V ACLIM = VREF * (Rlow // 152K) / (Rhigh // 152K + Rlow// 152K)
Iin_max = (1/R1)[(0.05/Vref) * Vaclim + 0.05]

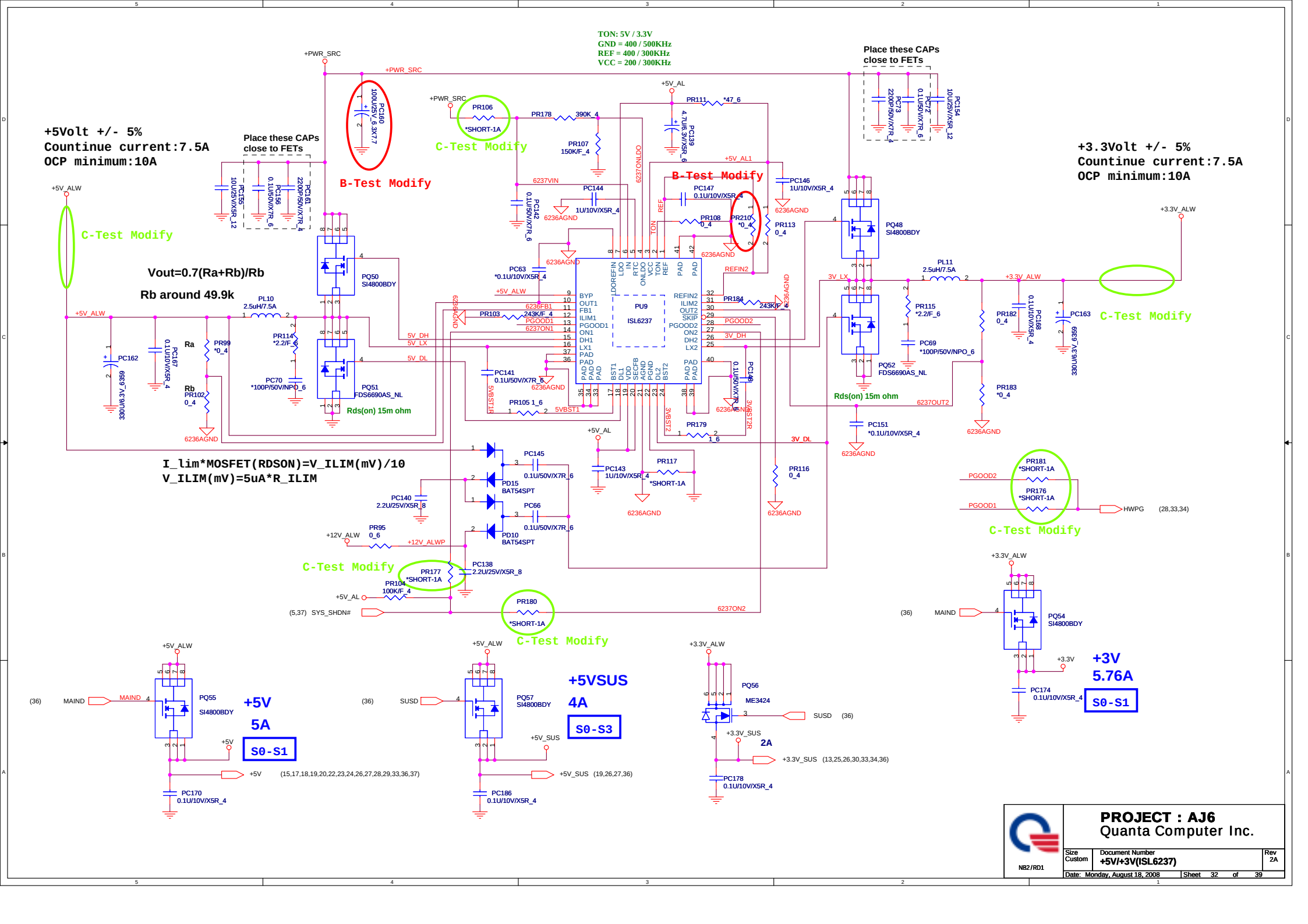
Charging Curret setting =>
I chg = 165mV / R2 * (Vchlim / 3.3V)

Input Current monitor
V icm = 19.9 * (Vcsip - Vcsin)

VADJ =
VERF >> 4.2V +5%
Float >> 4.2V
GND >> 4.2 -5%

Battery Low 7.5V

PROJECT : AJ6	
Quanta Computer Inc.	
Size: Custom	Document Number: CHARGER (ISL6251)
Rev: 3A	
Date: Thursday, August 21, 2008	Sheet 31 of 39
NB2/RD1	


TON: 5V / 3.3V
GND = 400 / 500KHz
REF = 400 / 300KHz
VCC = 200 / 300KHz
+5Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
+3.3Volt +/- 5%
Countinue current:7.5A
OCP minimum:10A
Place these CAPs close to FETs
Place these CAPs close to FETs
B-Test Modify
B-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
C-Test Modify
Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k
I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM
Rds(on) 15m ohm
Rds(on) 15m ohm
PU9
ISL6237
PQ48 SI4800BDY
PQ50 SI4800BDY
PQ51 FDS6690AS_NL
PQ52 FDS6690AS_NL
PQ54 SI4800BDY
PQ55 SI4800BDY
PQ56 ME3424
PQ57 SI4800BDY
PD15 BAT54SPT
PD10 BAT54SPT
PL10 2.5uH/7.5A
PL11 2.5uH/7.5A
+5V
5A
S0-S1
+5VSUS
4A
S0-S3
+3V
5.76A
S0-S1
2A
PROJECT : AJ6
Quanta Computer Inc.
+5V/+3V(ISL6237)
Monday, August 18, 2008
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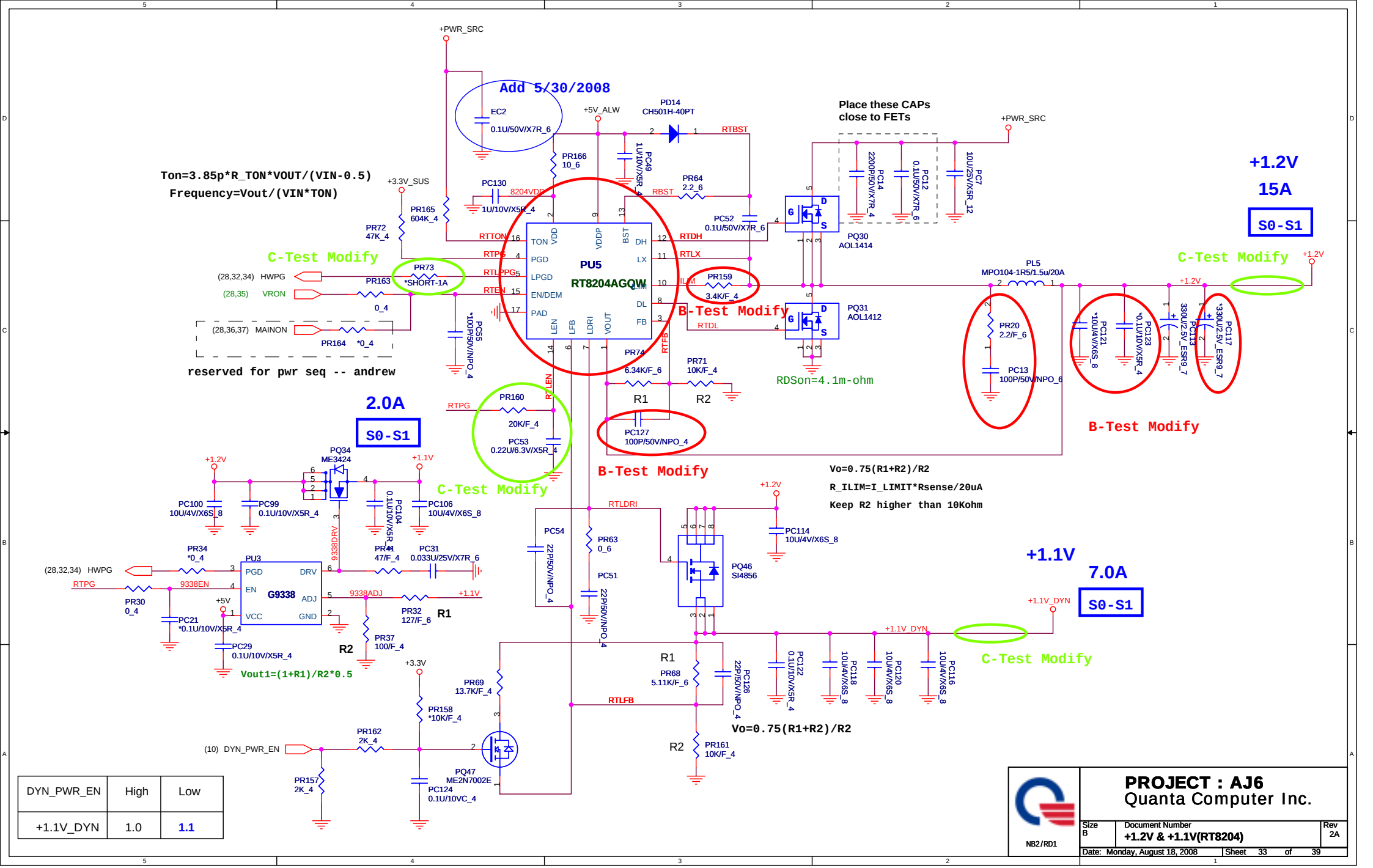
NB2/RD1



DYN_PWR_EN	High	Low
+1.1V_DYN	1.0	1.1

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
B	+1.2V & +1.1V(RT8204)	2A

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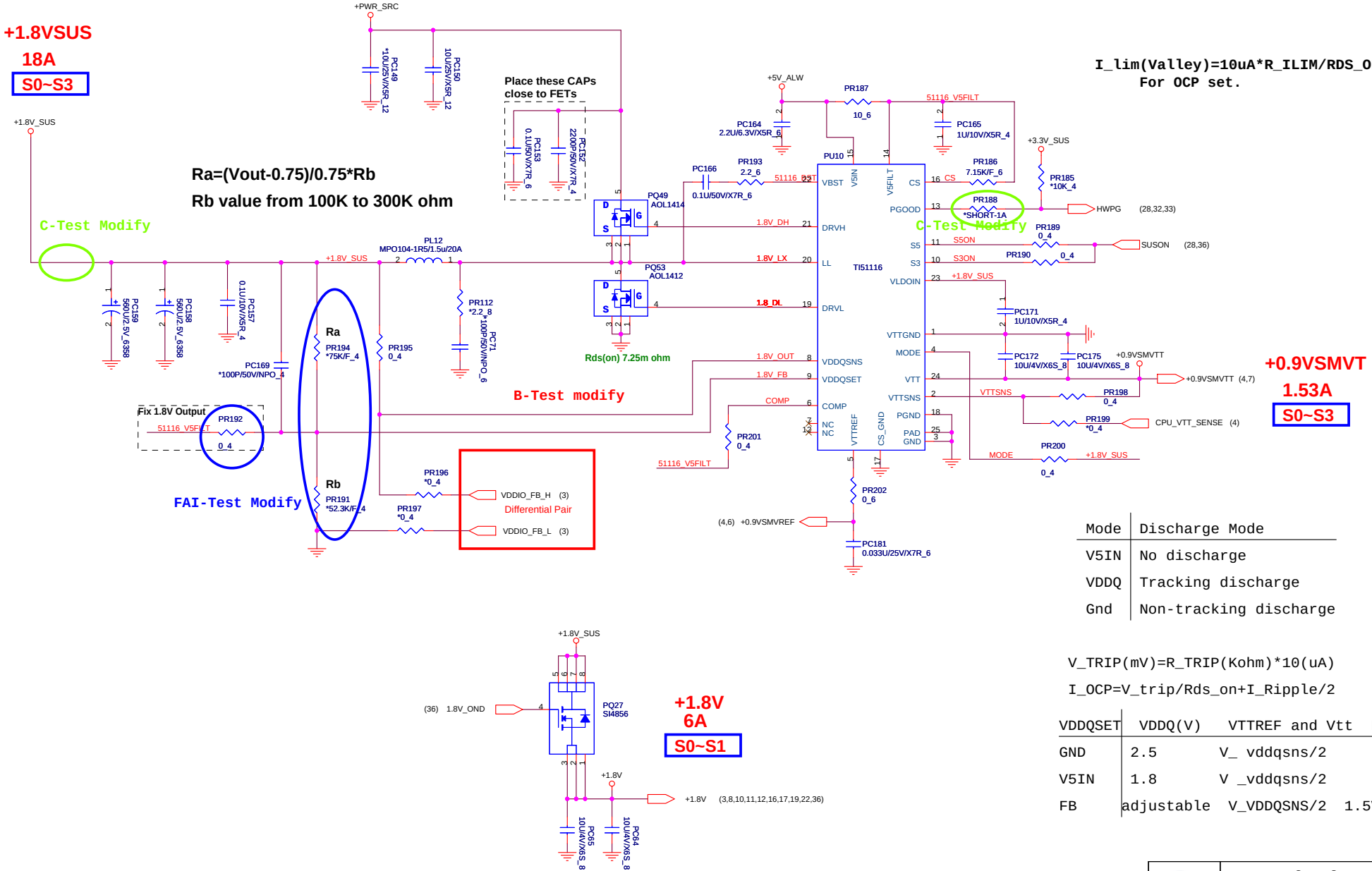
+1.8VSUS
18A
S0~S3
+PWR_SRC
Place these CAPs close to FETs
I_lim(Valley)=10uA*R_ILIM/RDS_ON
For OCP set.
Ra=(Vout-0.75)/0.75*Rb
Rb value from 100K to 300K ohm
C-Test Modify
B-Test modify
FAI-Test Modify
Fix 1.8V Output
Rds(on) 7.25m ohm
Differential Pair
TI51116
+0.9VSMVT
1.53A
S0~S3
+1.8V
6A
S0~S1
Mode | Discharge Mode
V5IN | No discharge
VDDQ | Tracking discharge
Gnd | Non-tracking discharge
V_TRIP(mV)=R_TRIP(Kohm)*10(uA)
I_OCP=V_trip/Rds_on+I_Ripple/2
VDDQSET | VDDQ(V) | VTTREF and Vtt | Note
GND | 2.5 | V_ vddqsns/2 | DDR
V5IN | 1.8 | V _vddqsns/2 | DDR2
FB | adjustable | V_VDDQSNS/2 | 1.5V<VDDQ<3V
PROJECT : AJ6
Quanta Computer Inc.
NB2/RD1
Document Number
1.8VSUS/DDR_VTER/+1.8V/2.5V
Size Custom
Rev 2A
Date: Tuesday, August 19, 2008
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OFS/VFIXEN	Offset & Droop	SVI	VFIX
GND	0	0	X
+3.3V	X	X	0
+5V	X	0	X

Metal VID Codes

SVC	SVD	Output
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

VFIXEN VID Codes

SVC	SVD	Output
0	0	1.4
0	1	1.2
1	0	1.0
1	1	0.8

C-Test Modify

Close to CPU socket

B-Test Modify

C1-Test Modify

FAI Modify

Pin 49 is GND Pin

ISL6265HRTZ-T

Close to CPU socket

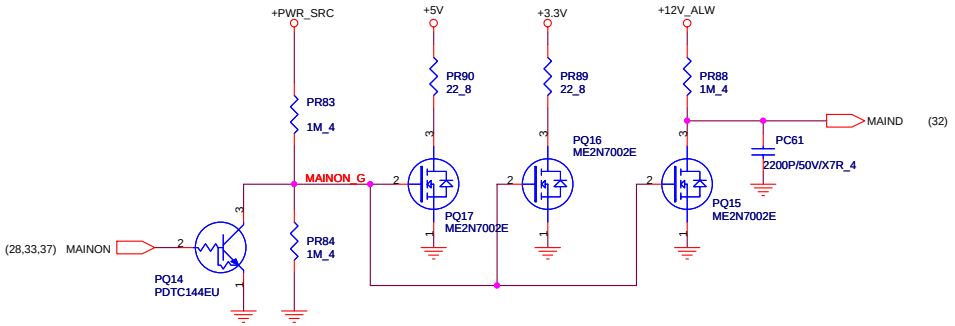
Parallel

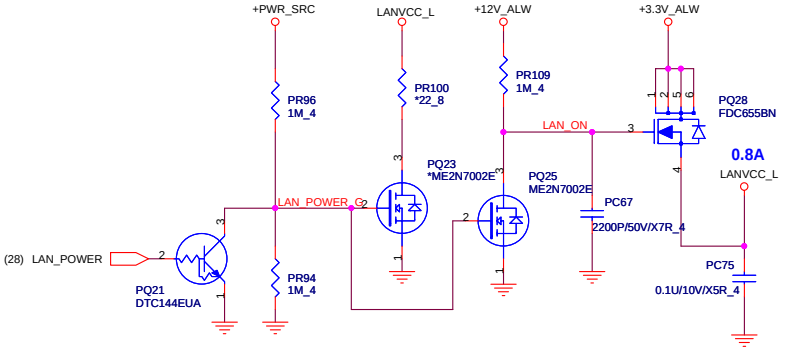
Close to CPU socket

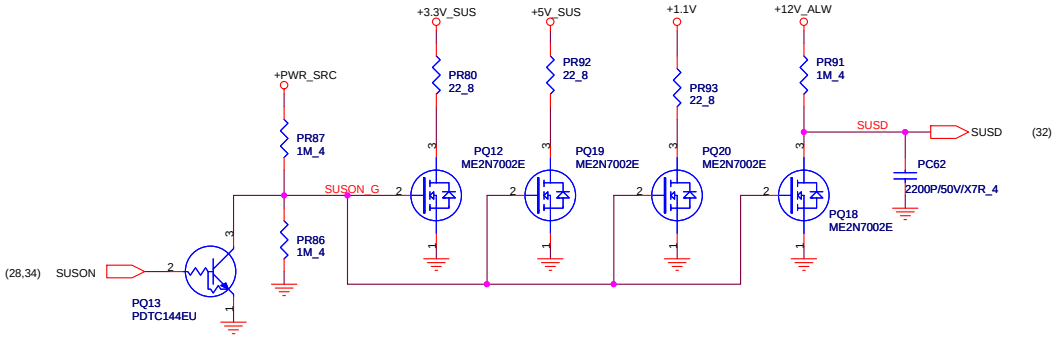
Reserve for uni-plane

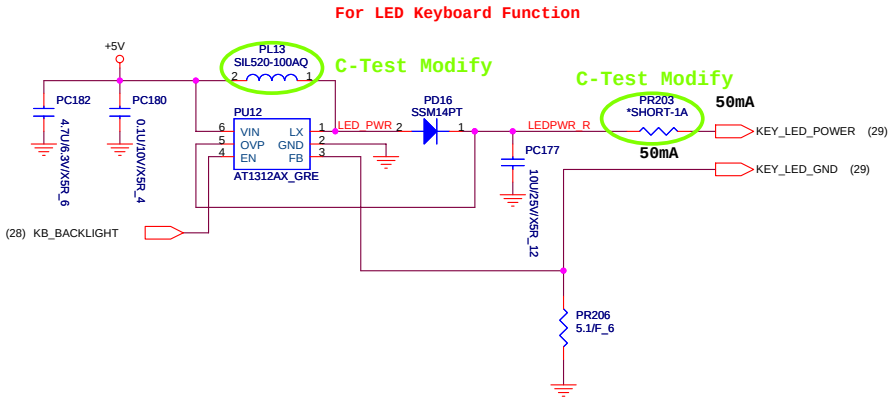
Reserve for uni-plane

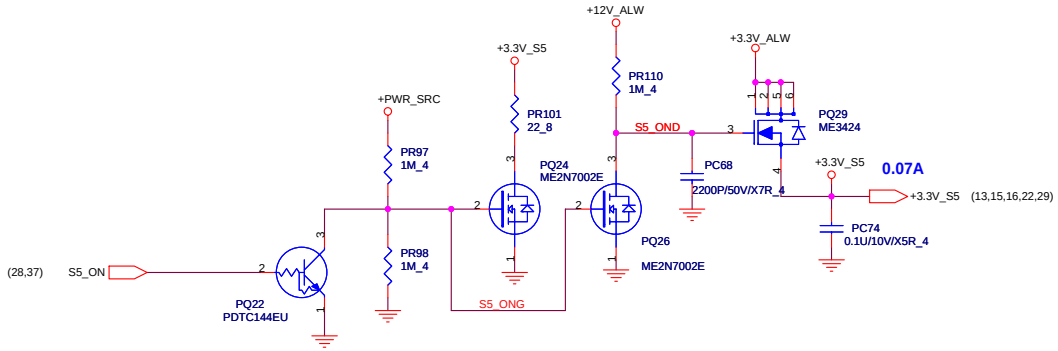
PROJECT : AJ6	
Quanta Computer Inc.	
Size: C	Document Number: CPU_CORE(ISL6265)
Rev: 3B	
NB2/RD1	
Date: Thursday, August 21, 2008	Sheet 35 of 39

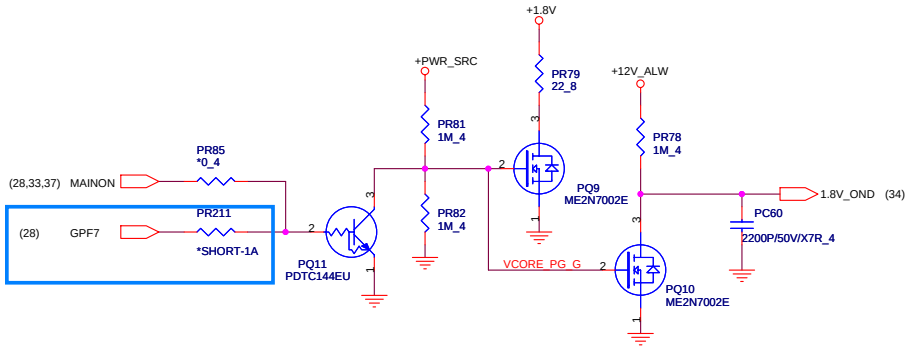












PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	2A

N82/RD1

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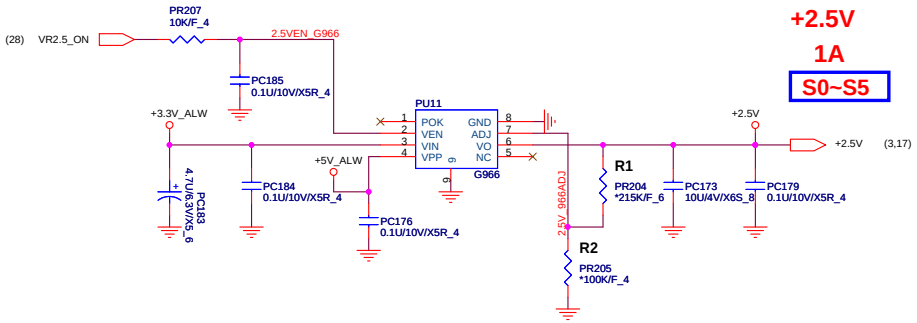
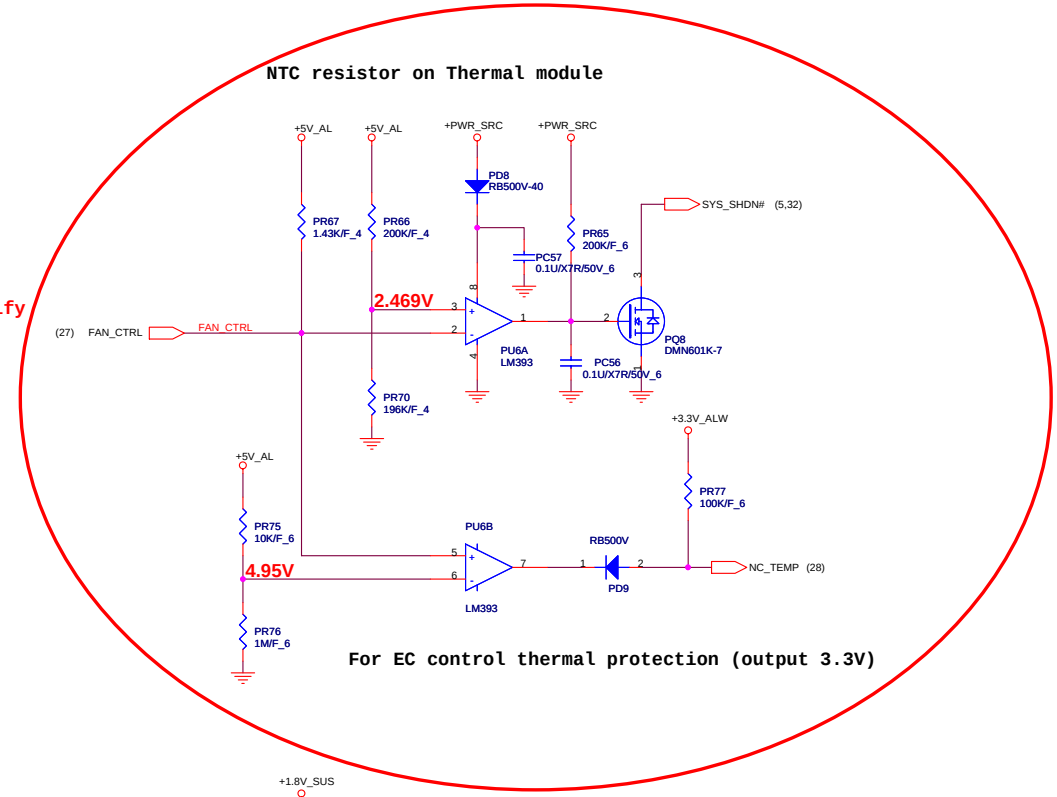


+2.5V

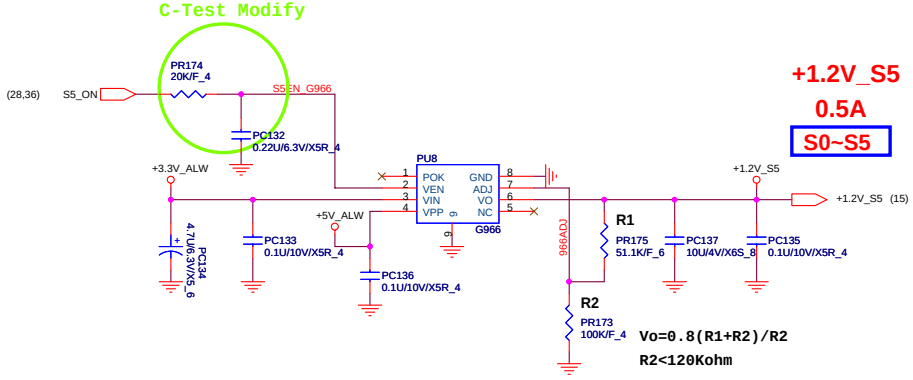
1A

S0~S5

B-Test Modify



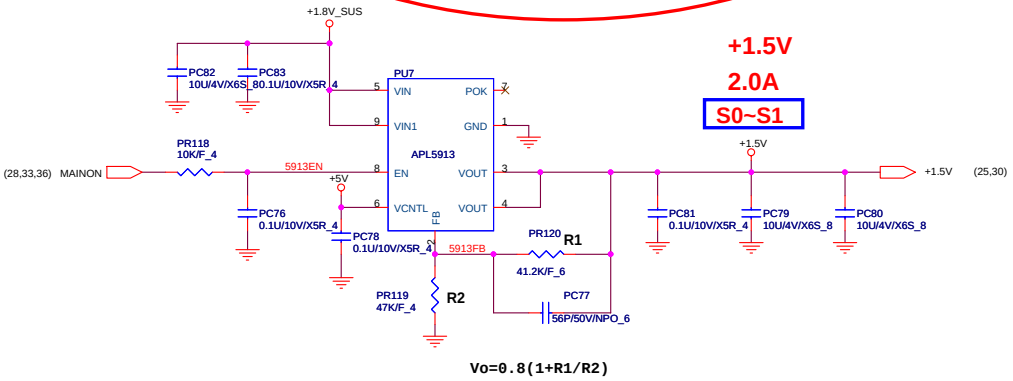
C-Test Modify



+1.2V_S5

0.5A

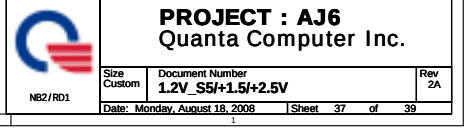
S0~S5

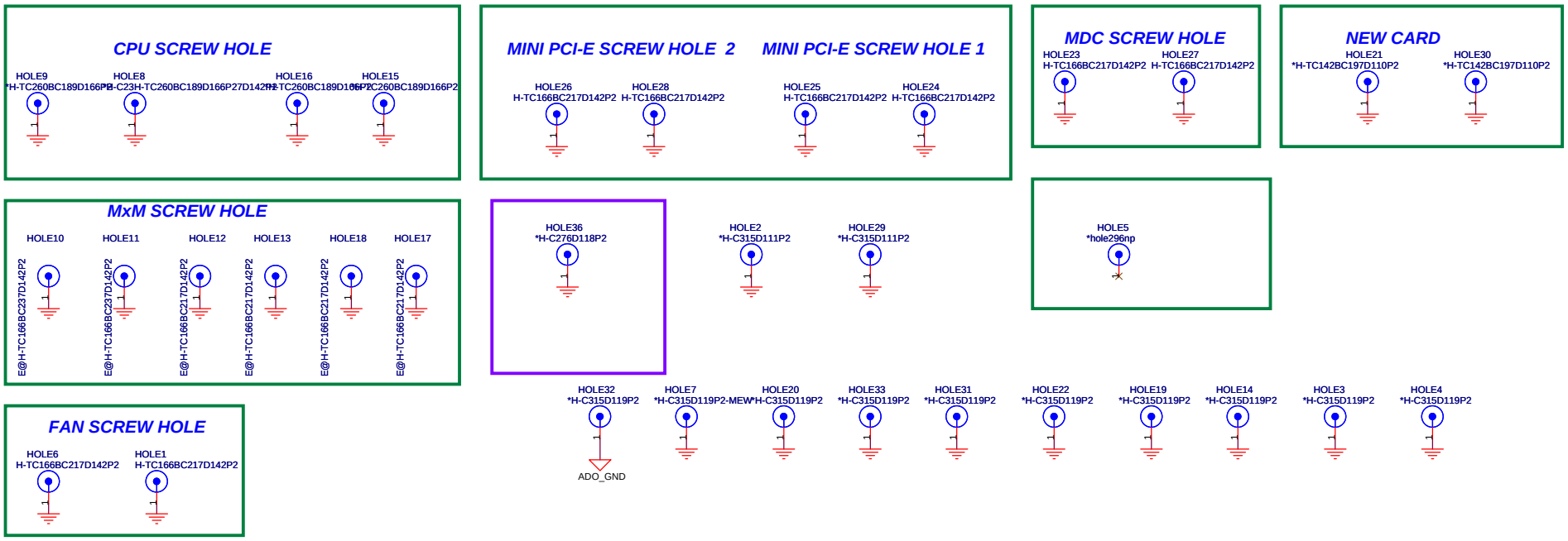


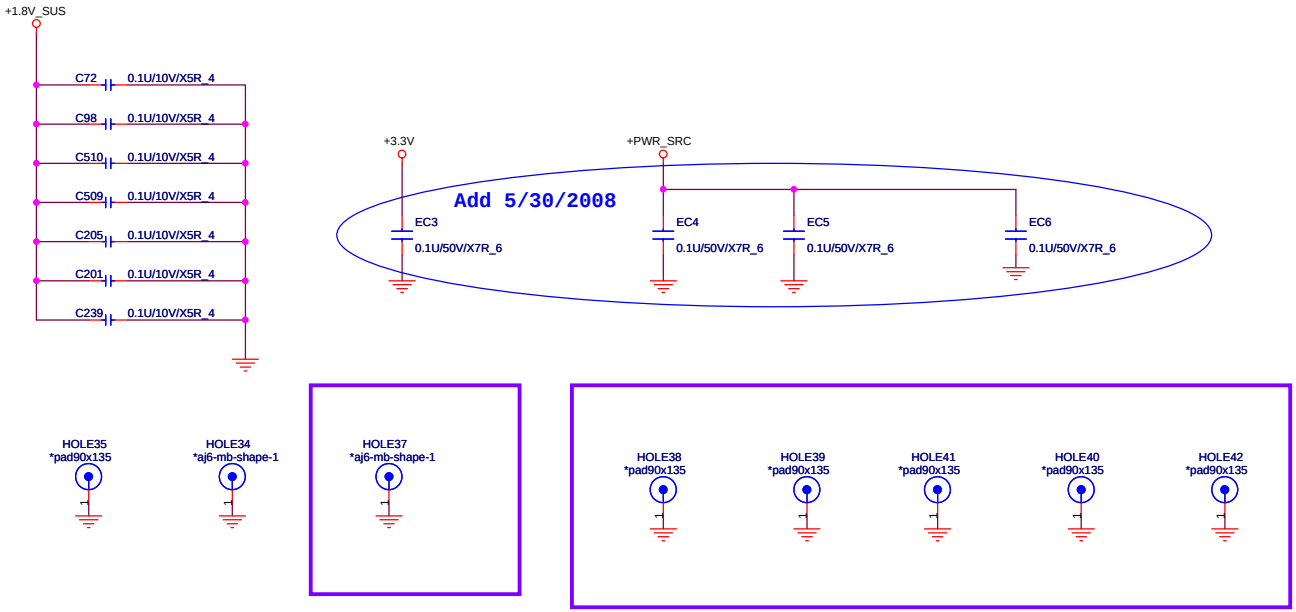
+1.5V

2.0A

S0~S1







EMI request 19/08/2008

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EMI PAD &Hole	2A
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MODEL: REV

CHANGE LIST

AJ6 MB

PAGE	FROM	TO
1	1A	
2	1A	3B
3	1A	
4	1A	
5	2A	
6	1A	
7	1A	
8	1A	
9	3A	
10	3A	
11	1A	3B
12	1A	
13	1A	
14	3A	
15	2A	
16	1A	
17	3A	3B
18	2A	
19	3A	
20	1A	
21	3A	
22	1A	
23	3A	
24	3A	
25	2A	
26	3A	
27	2A	
28	3A	
29	3A	3B
30	1A	
31	3A	
32	2A	
33	2A	
34	2A	
35	2A	3B
36	2A	
37	2A	
38	2A	
39	3A	3B

AJ6 MB

1A

First release

2A

Page5:Add Q66,Q67 for EC drivinng / Add Q68,R574 & swap U3 pin4, pin6 for system shootdown
Page9:Change PCIE CAP. from X5R to X7R & modify C_PEG_TX for UMA's HDMI detect issue
Page10:Delet R115 for UMA SKU.
Page15:Modify R83,R184,R368,R370,R371,R372,R,386,R387,R391,R392 for board ID / Chanhe C338,C327 for accuracy
Page17:Add Q60,R517 for MXM discharge / Add R516,D32 for MXM timming / Modify C215,C210,C209,Q19,C238 for MXM power express /Add Q62,Q63 for MXM smbus
Page18:Add Q61,R518 for HDMI HPD sense issue / modify Q1,Q2 for UMA HDMI smbus issue / delete D4,D5 & change R5,R6 value
Page19:Modify & add Q69,C656,C657R567,R569 for LCD slight light issue / Add RP40 for MXM
Page21:Add R95 for Lan chip power / change R60,R61,R62,R63 package
Page23:Add Q64,Q65,R570,R571,R572 for SPDIF's LED issue / Change R271,R272,R265,R266 for volume issue /Change R473,R472,R471,R470 for EMI issue
Page25:Add R562,R563,R564,R565,R566 for Acer LPC debug use / Add D12,R213 for WLAN LED
Page26:Delete MODEM CAP. C166,C165
Page27:Add C644,C645 for USB
Page28:Modify U27 pin112 to AJ6 board ID setting / Swap pin98 & pin107 / Delete C601 for IT8502 issue /Change C621, C608 of value for accuracy
Page29:Swap NC7,CN3 connector & modify circuit / Modify CN8 circuit / Delete R357 is no use
Page32:Add a resister to connect PU9 pin1 and pin32 / Add PC160 in the circuit.
Page33:Change PU5 PN from AL008204000 to AL08204001 / Change PR159 PN to CS23402FB08 / Add PR20, PC13, PC127 in the circuit / Delete PC117, PC123, PC121 in the circuit
Page34:Change PR191 from 51.1K/F_4 to 52.3K/F_4 (CS35232FB10).
Page35:Delete PC17, PC18 in the circuit / Add PC91 in the circuit
Page36:Add PR90,PR89,PR80,PR92,PR93,PR101,PR79,PQ17,PQ16,PQ12,PQ19,PQ20,PQ24,PQ9 in the circuit for discharge
Page37:Add PR67, PR66, PD8, PC57, PR65, PQ8, PC56, PU6, PR70, PR75, PR76, PD9, PR77 in the circuit for Acer thermal protection
Page38:Add EC3,EC4,EC5,EC6 for EMI

3A

Page9:Add R45,R51,R64,R65,R68,R69,R72,E73 to solve the HDMI issue
Page10 : for CRT filicker, change C179,C191,C491,C125,C192 value from 2.2u to 10u.
Page14 : change the board ID. 7/10
Page17 : Duo to cost down, so to remove Q25 ,Q45 from MXM BOM.
Page19 : add LCD panel circuit to fix white display when system boot up.
Page21 : to solve the Lan issue, ADD C479,C480
Page23 : change Gain from 15.6 to 10 db. 7/8
Page24 : Change C498,C499 ,C585,C587 value form 3900P to 0.001U
Page26 : to solve the EMI issue, ADD L52,L53
Page28 : For EMI request. add C618,C619 7/10
Page26 : to solve the EMI issue, ADD L52,L53
Page29 : Change R509 PN from 2M to 0ohm. Change R85,R86,R275 ,R273,R274 to 300 ohm, Del D31& C636 & D2 from BOM
Page26 : to solve the EMI issue, ADD L52,L53
Page31 : PL13 PN change to CV01014TZ01

3B

Page2 : ADD C648(CH11006JB00) , for EMI request (+1.2v)
Page11 :Change C56 and C493 from 4.7u/6.3V to 330u/2V (CH733RY8802) to solve" HIGH POWER NOSIE ISSUE"
Page17 :Add C238 (CC71004MZ81) to solve" HIGH POWER NOSIE ISSUE"
Page29 :For slowly pulse" light to dark about 2 second, ADD R510,R576,R577, Q70,Q71,D34,D35 ,C636,C646,C647 ,R302 ,R521 ; DEL R273,R274,R509
Page35 :Change PC90 and PC92 from 10u/25V to 27u/25V (CC62704MZ02) to solve" HIGH POWER NOSIE ISSUE"

Project :AJ6 MB | **MB Assy' P/N: 31AJ6MB0030/40** | **Document No.:**

Approved by : Johnny_O | **Drawing by :Kenneth Huang** | **DATE:** 2008/8/19

NB2/RD1

PROJECT : AJ6
Quanta Computer Inc.

Size: Custom | Document Number: EC | Rev: 3B

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