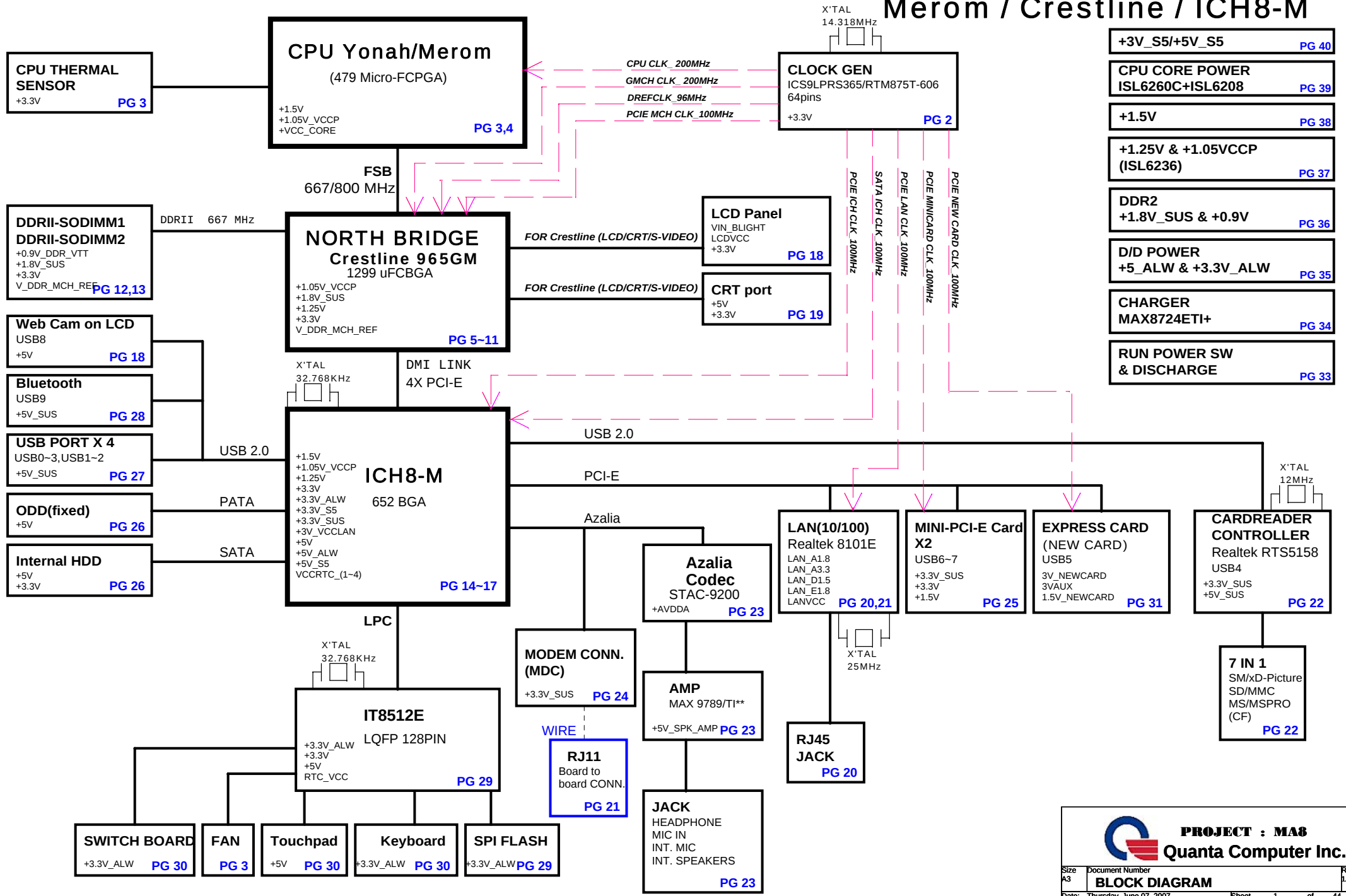
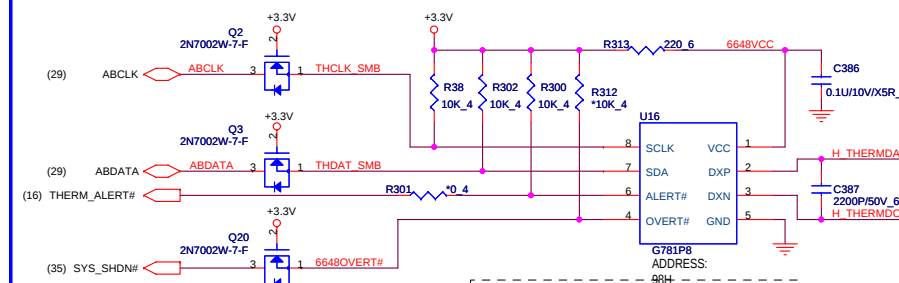


MA8 BLOCK DIAGRAM

Merom / Crestline / ICH8-M

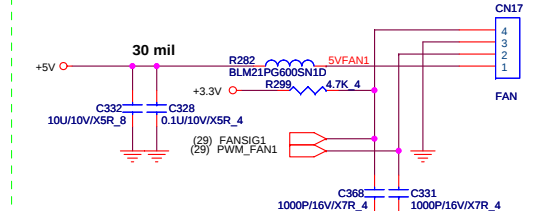
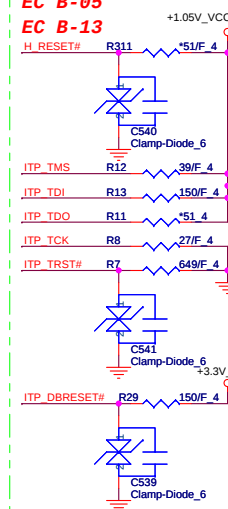


CPU Thermal monitor



CPU FAN

EC B-01

EC B-05
EC B-13

Populate ITP700Flex for bringup

ITP700 layout guidelines

Signal	Resistor Value	Connect To	Resistor Placement
TDI	150 ohm ± 5%	VCCP	Place the pull-up near CPU
TMS	39 ohm ± 1%	VCCP	Within 200ps of ITP connector
TRST#	500 to 600 ohm ± 5%	GND	Place the pull-up near CPU
TCK	27 ohm ± 1%	GND	Connect to TCK pin of CPU and then connect it to F80 pin of ITP connector in daisy chain. Place the pull-down near TCK0 pin of ITP connector
TDO	51 ohm ± 5%	VCCP	Place the pull-up near CPU
RESET#	22.6 ohm ± 1% series resistor and pullup 51 ohm ± 1%.	VCCP	Connect to CPURST# pin of GMCH through the series resistor placed within 200ps of ITP connector. Place the pull-up after the series resistor from ITP connector.

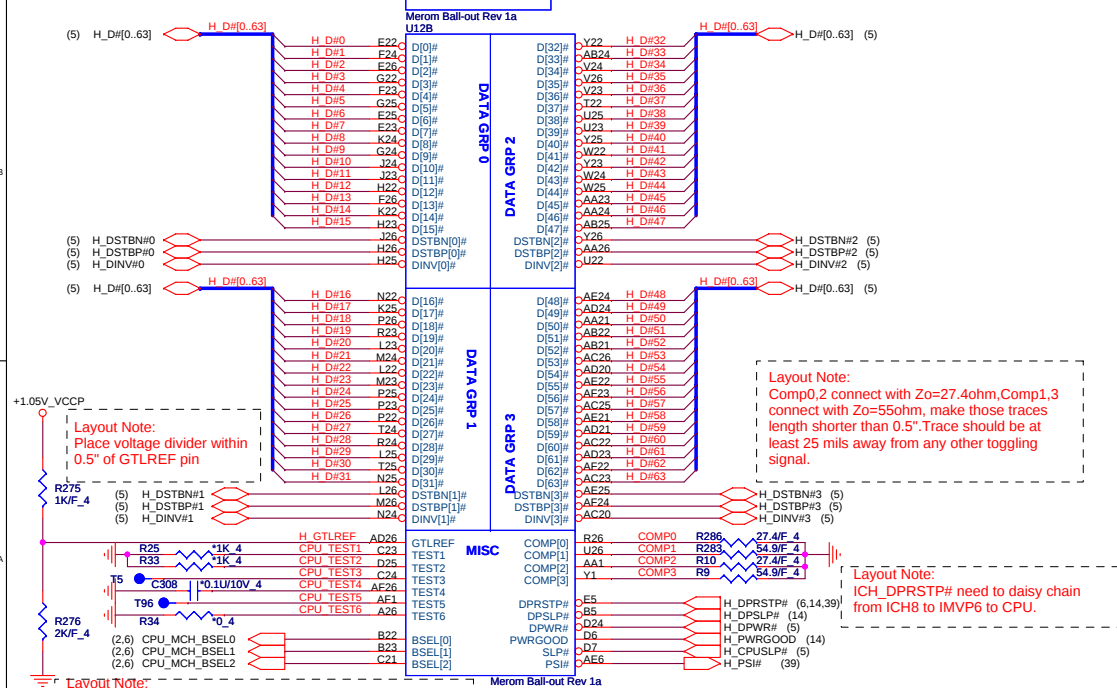
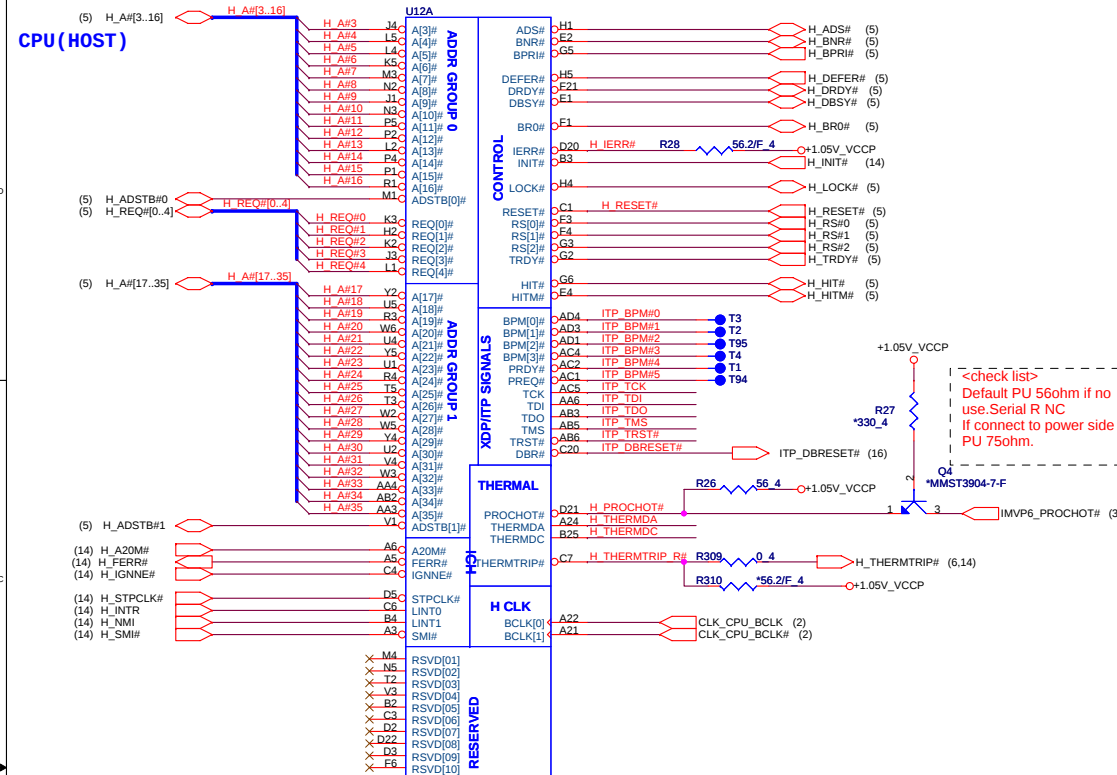
Layout Note:
Comp0,2 connect with Zo=27.4ohm, Comp1,3 connect with Zo=55ohm, make those traces length shorter than 0.5". Trace should be at least 25 mils away from any other toggling signal.

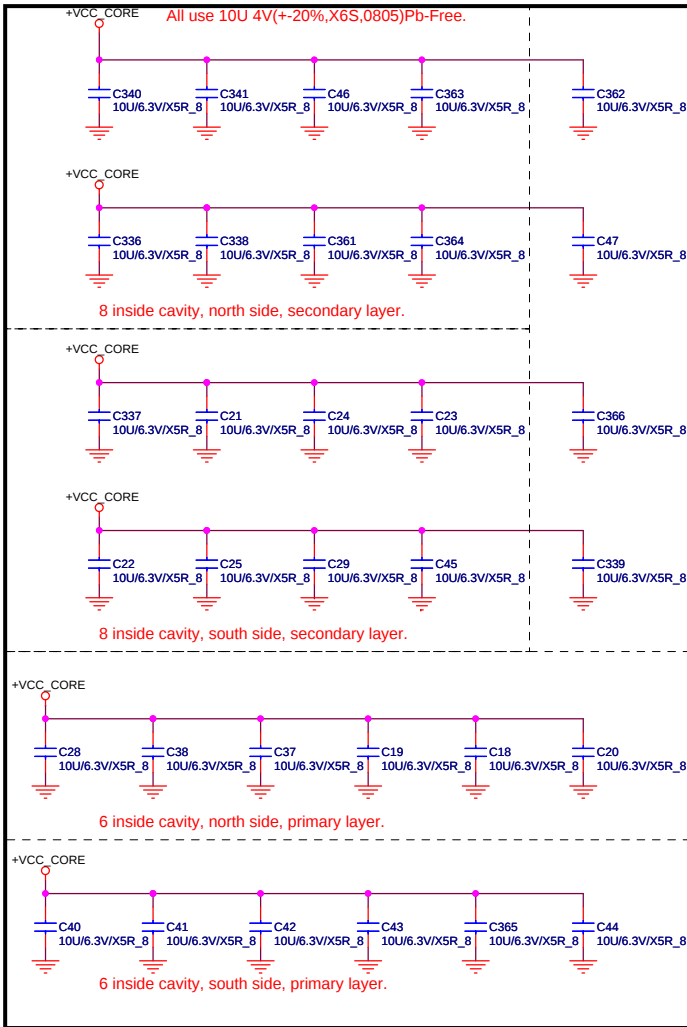
Layout Note:
ICH_DPRSTP# need to daisy chain from ICH8 to IMVP6 to CPU.



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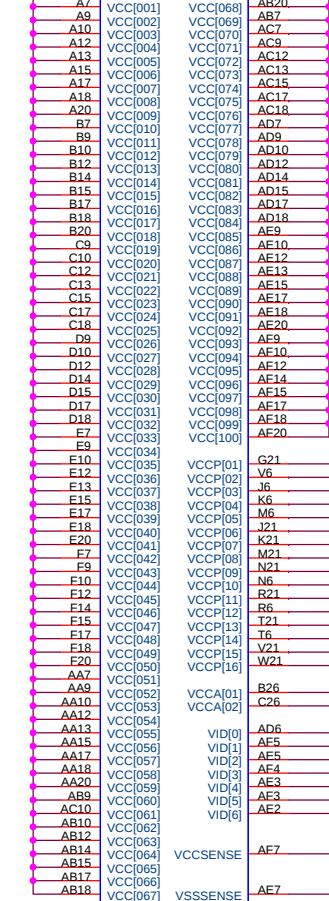
CPU (HOST)





+VCC_CORE

U12C



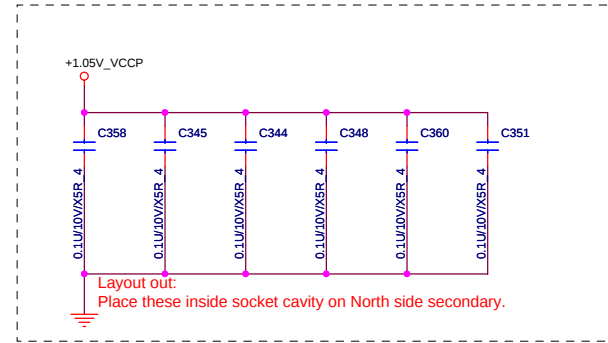
<REV.NO. 0.5/REF.NO.19343>

Ivcc Max 52A

Ivccp Max 6A(VCCP supply before Vcc stable)

Max 2A(VCCP supply after Vcc stable)

Ivcca Max 130mA



+1.05V_VCCP

C335
330U/2V_7343

+1.5V

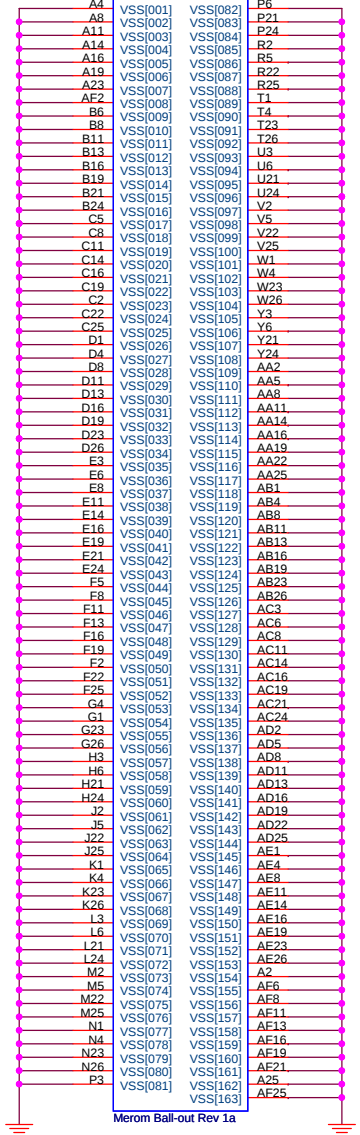
+VCC_CORE

0.01U/16V/X7R_4

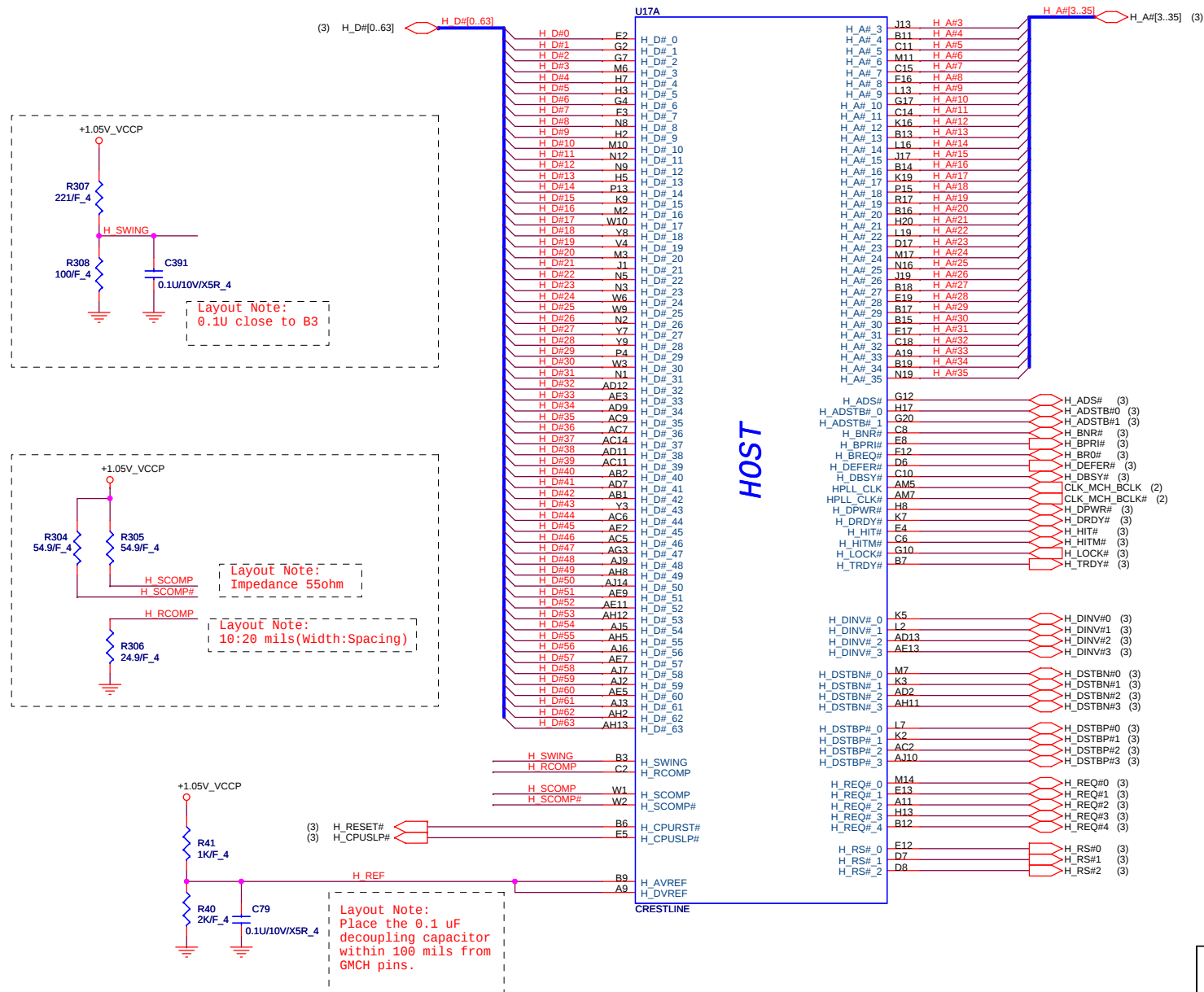
R279
100F_6Layout Note:
Place C68, C64 near PIN B26.

Layout Note:
Route VCCSENSE and VSSSENSE
traces at 27.4ohms and length
matched to within 25 mil. Place PU
and PD within 2 inch of CPU.

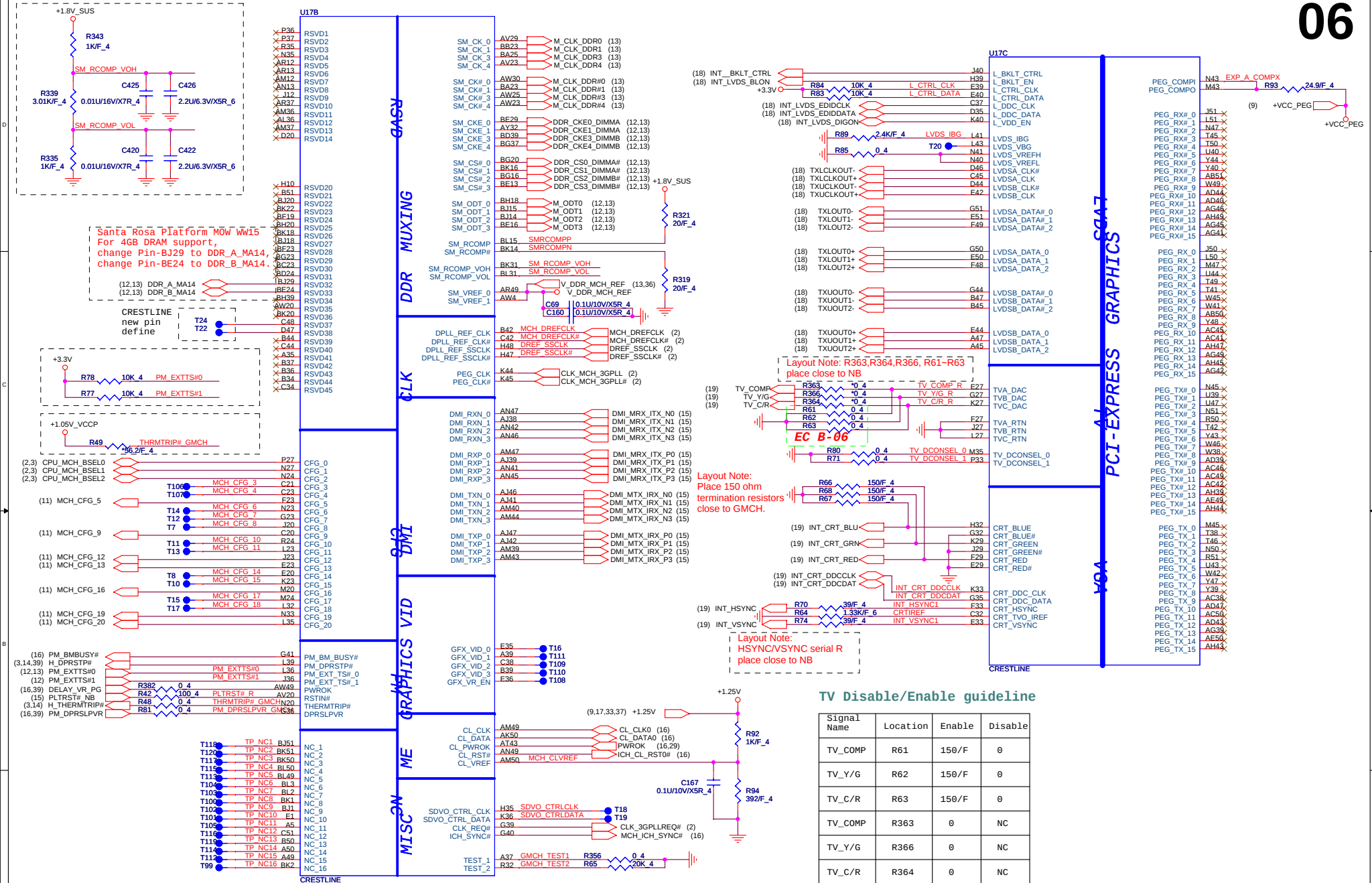
U12D

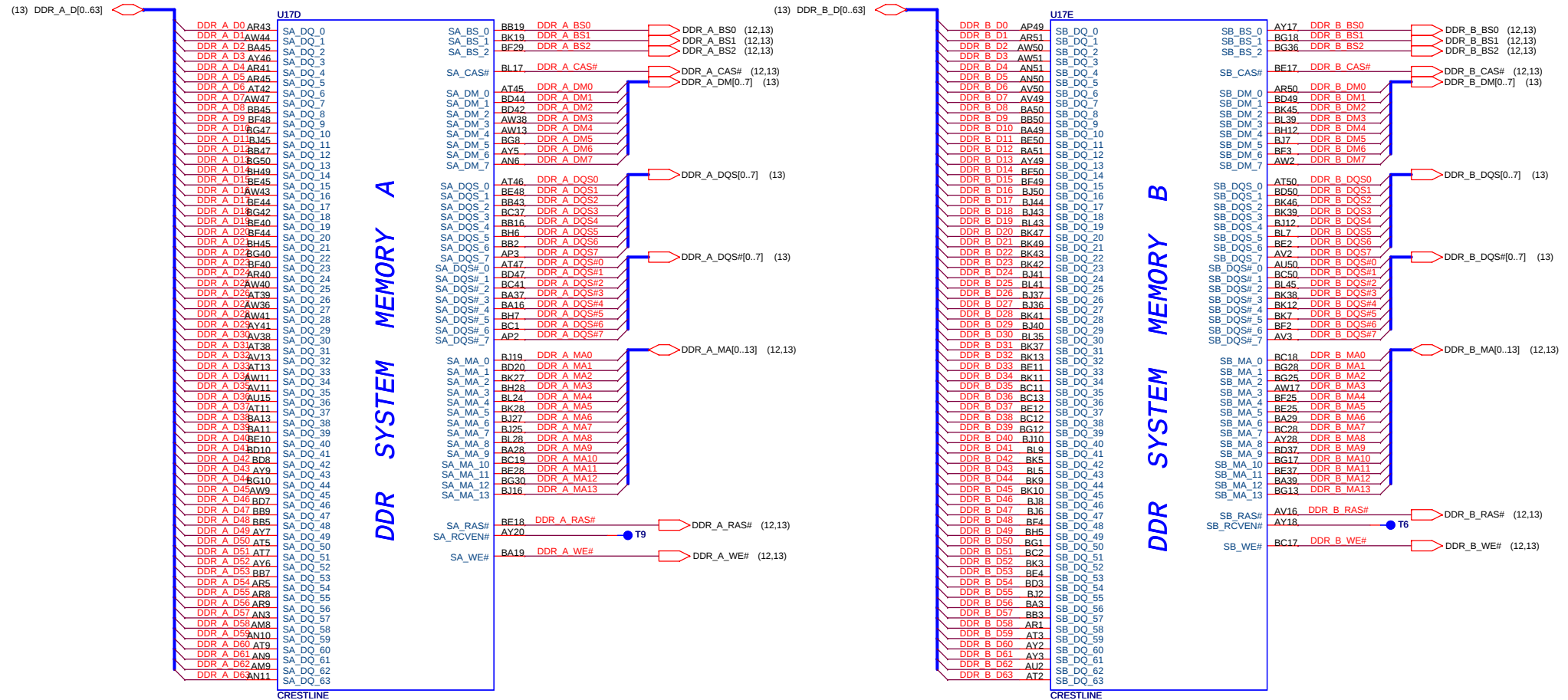


PROJECT : MA8
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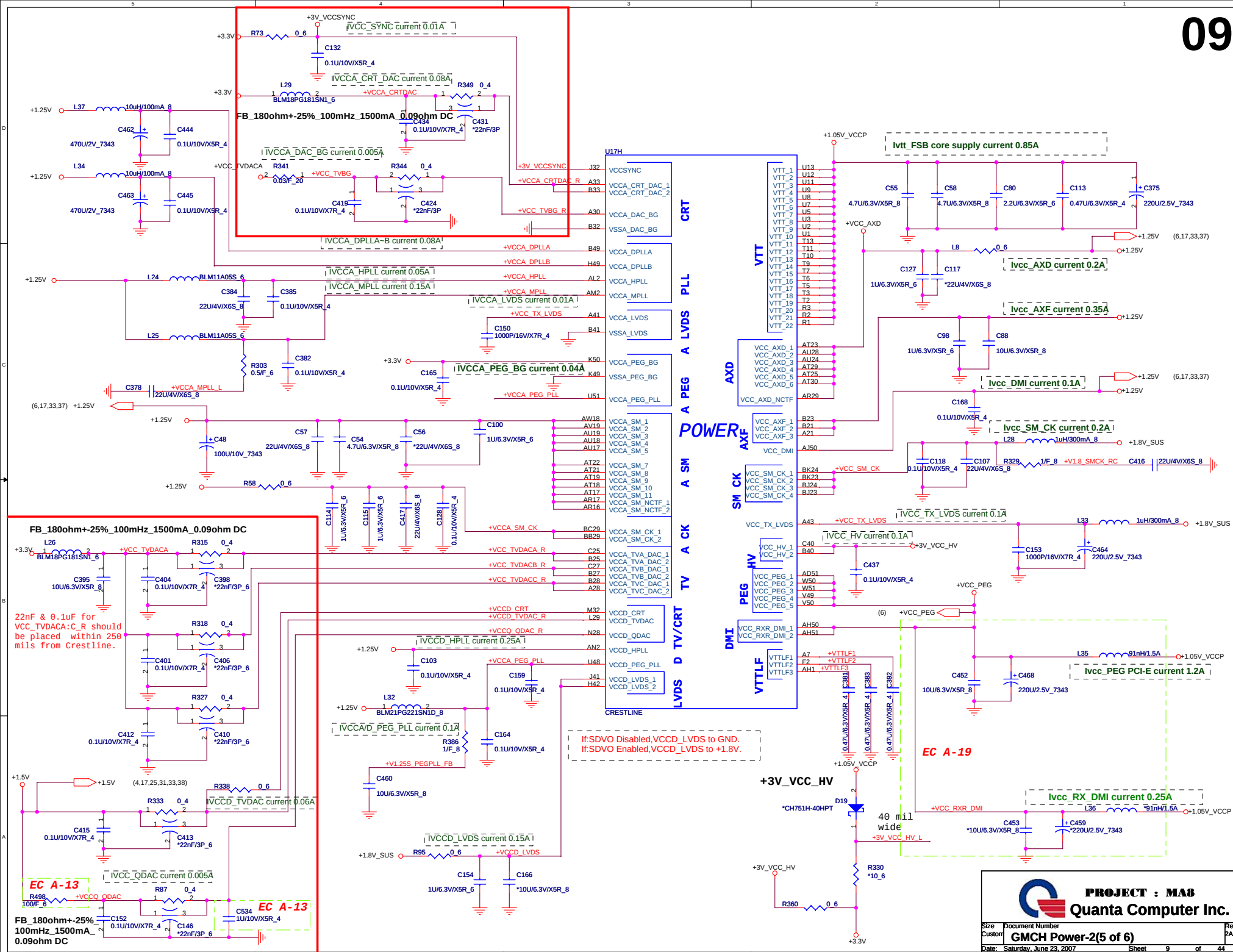


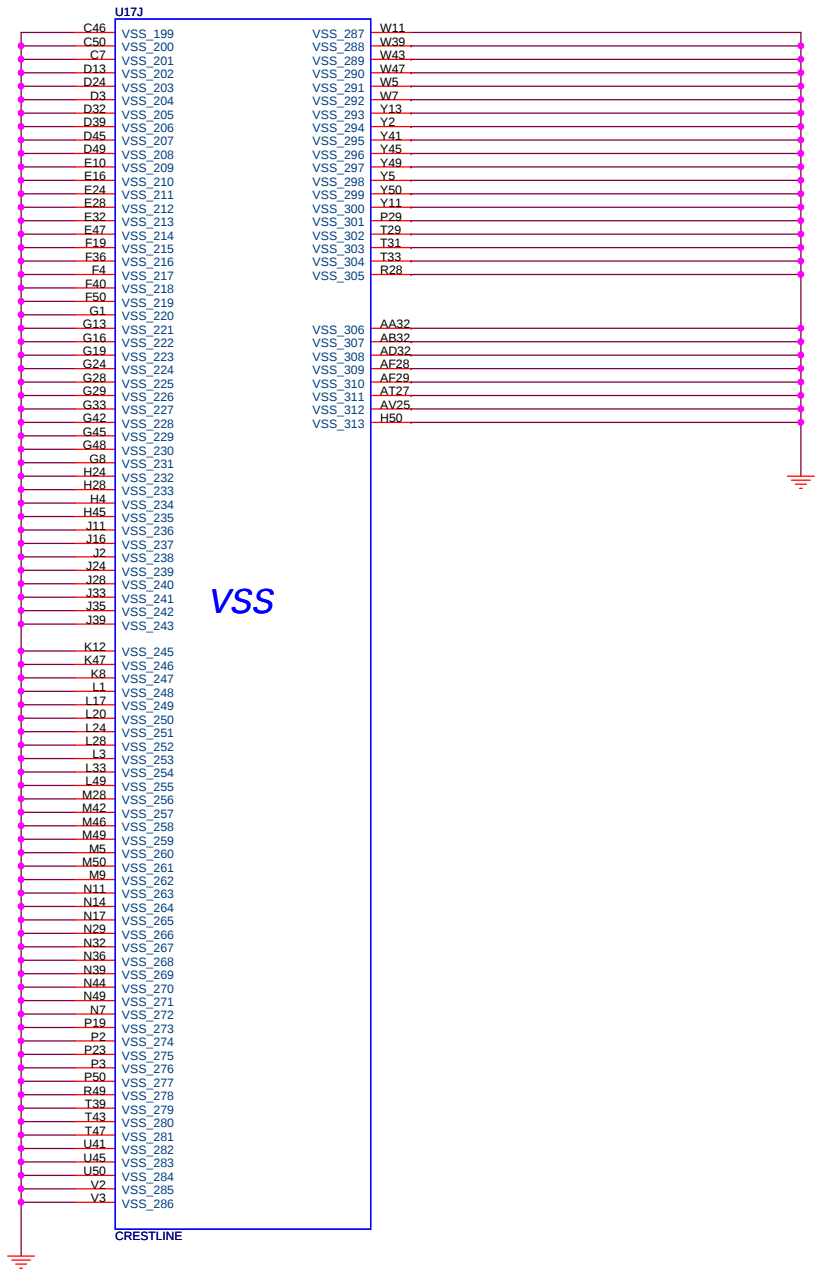
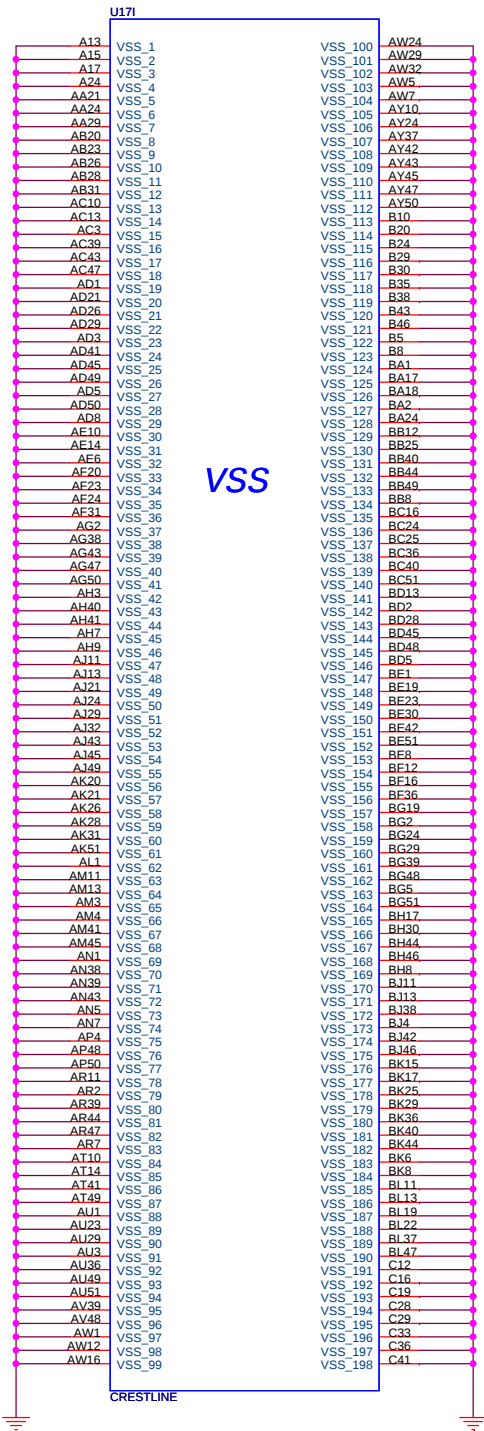
PROJECT : MA8
Quanta Computer Inc.





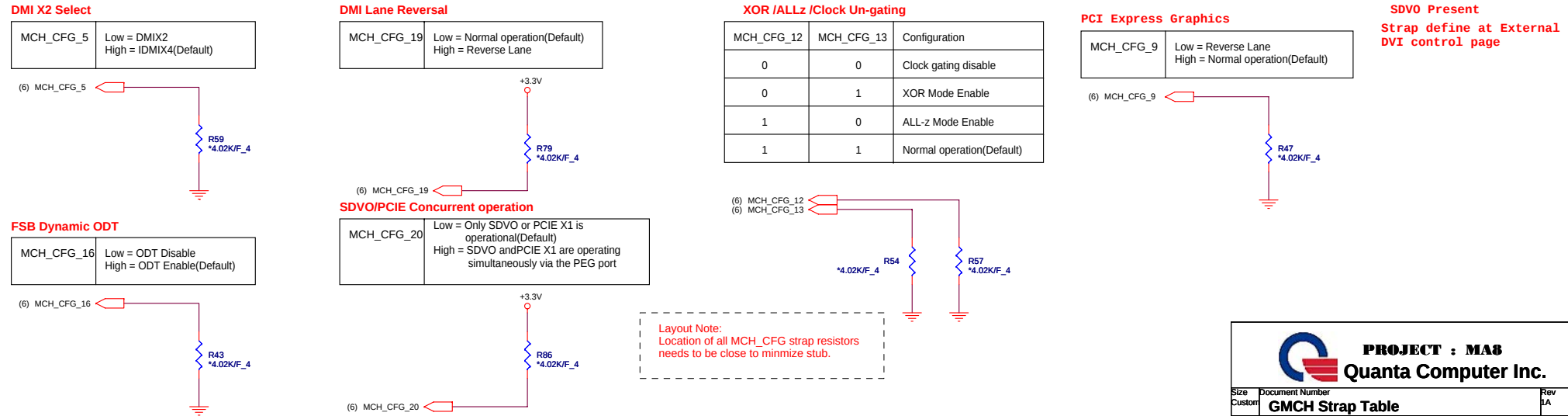
PROJECT : MA8
Quanta Computer Inc.



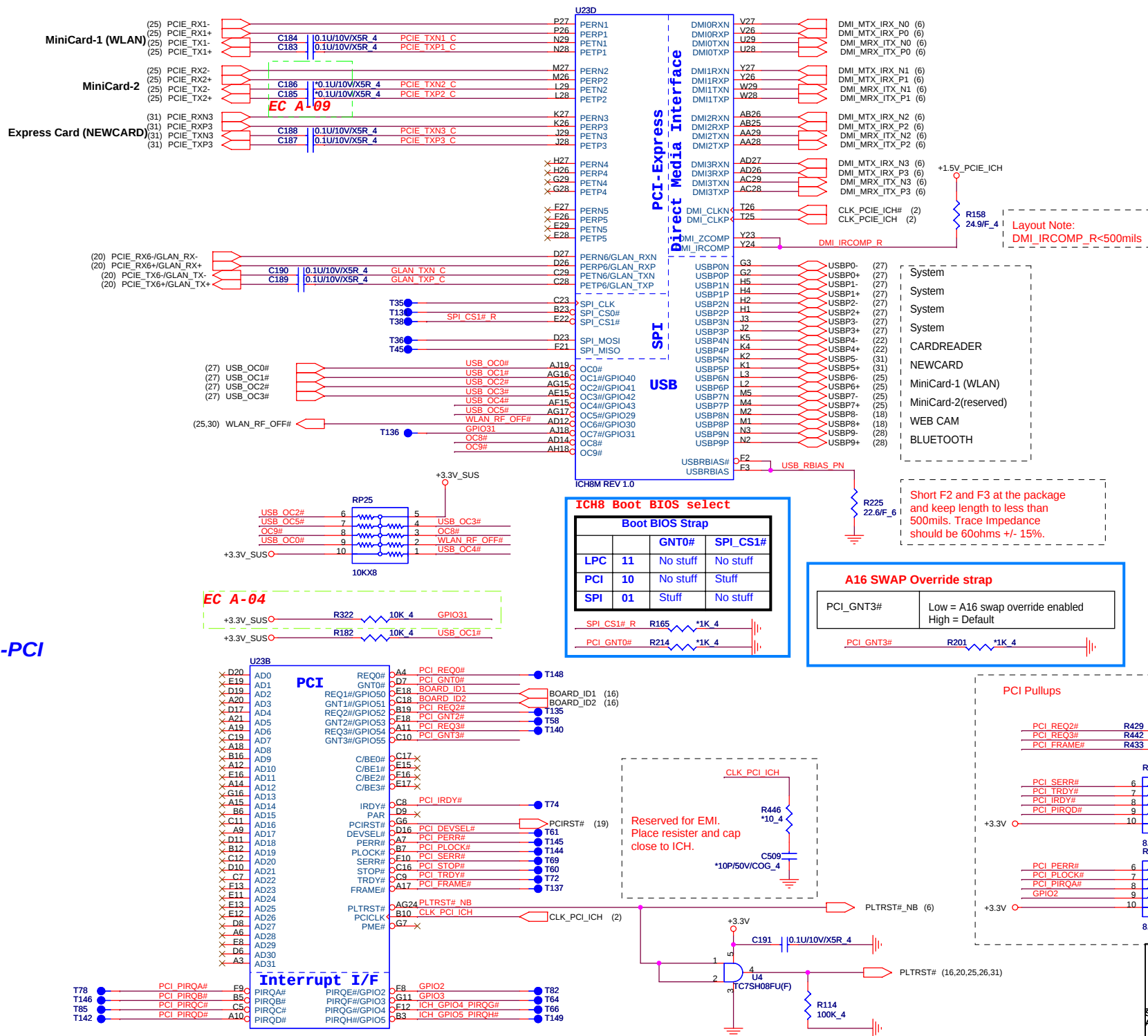


All strap are sampled with respect to the leading edge of the GMCH Power OK(PWROK) Signal
CFG[17:3] Have internal Pull-up
CFG[18:19] Have internal Pull-down
Any CFG signal strapping option not list below should be left NC Pin

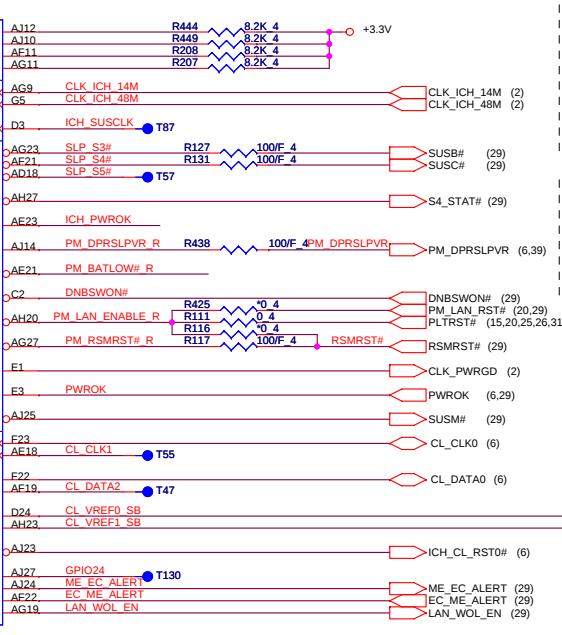
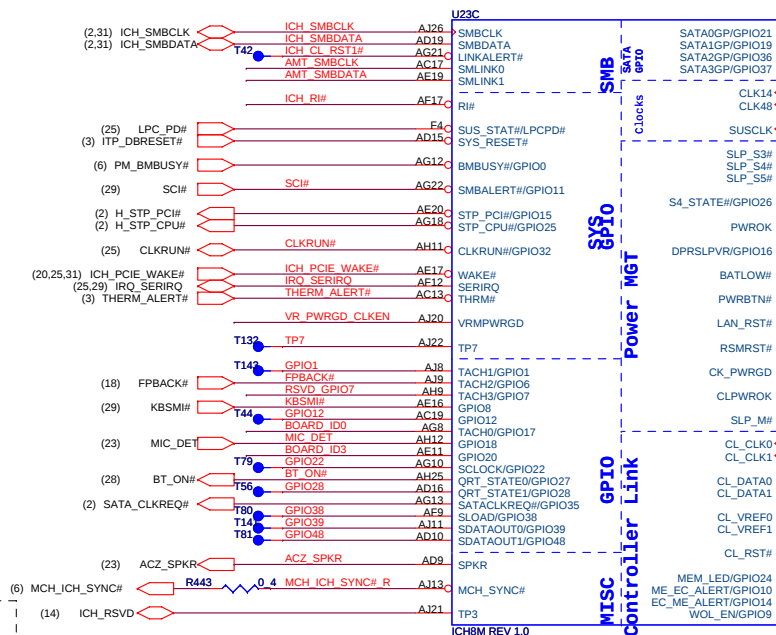
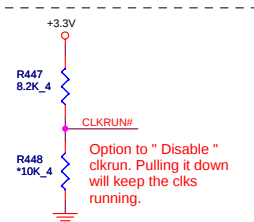
Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	Reserved	
CFG7	CPU Strap	0 = Reserved 1 = Mobile CPU(Default)
CFG8	Low power PCI Express	0 = Normal mode 1 = Low Power mode
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALLZ	00 = Reserved 01 = XOR Mode Enable 10 = All-Z Mode Enabled 11 = Normal operation(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
SDVO_CTRLDATA	SDVO Present	0 = No SDVO Card present(Default) 1 = SDVO Card Present
CFG19	DMI Lane Reversal	0 = Normal operation(Default) 1 = Reverse Lanes
CFG20	SDVO/PCIE concurrent	0 = Only SDVO or PCIE x1 is operation(Default) 1 = SDVO and PCIE x1 are operating simultaneously via the PEG port



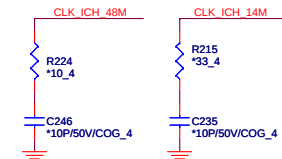
Place TX DC blocking caps close ICH8.



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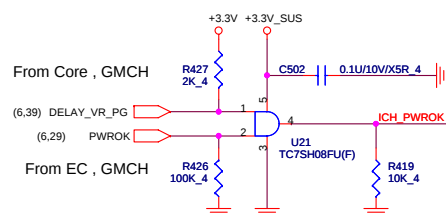
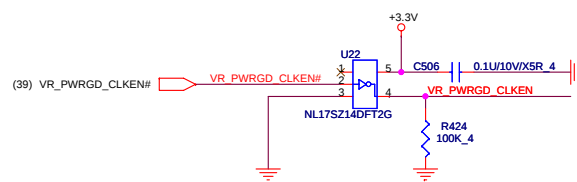
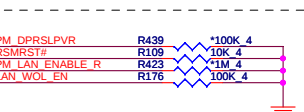
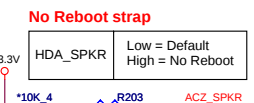
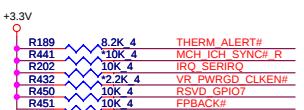
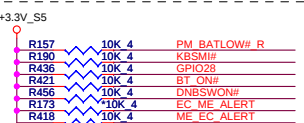


Place these close to ICH8.



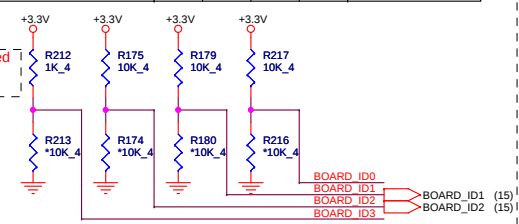
If no use internal LAN MAC connect LAN_RST# to PLTRST#

Use internal LAN MAC connect LAN_RST# to RSMRST# should go high no sooner than 10 ms after both VccLAN3_3 and VccLAN1_5 have reached their nominal voltages.



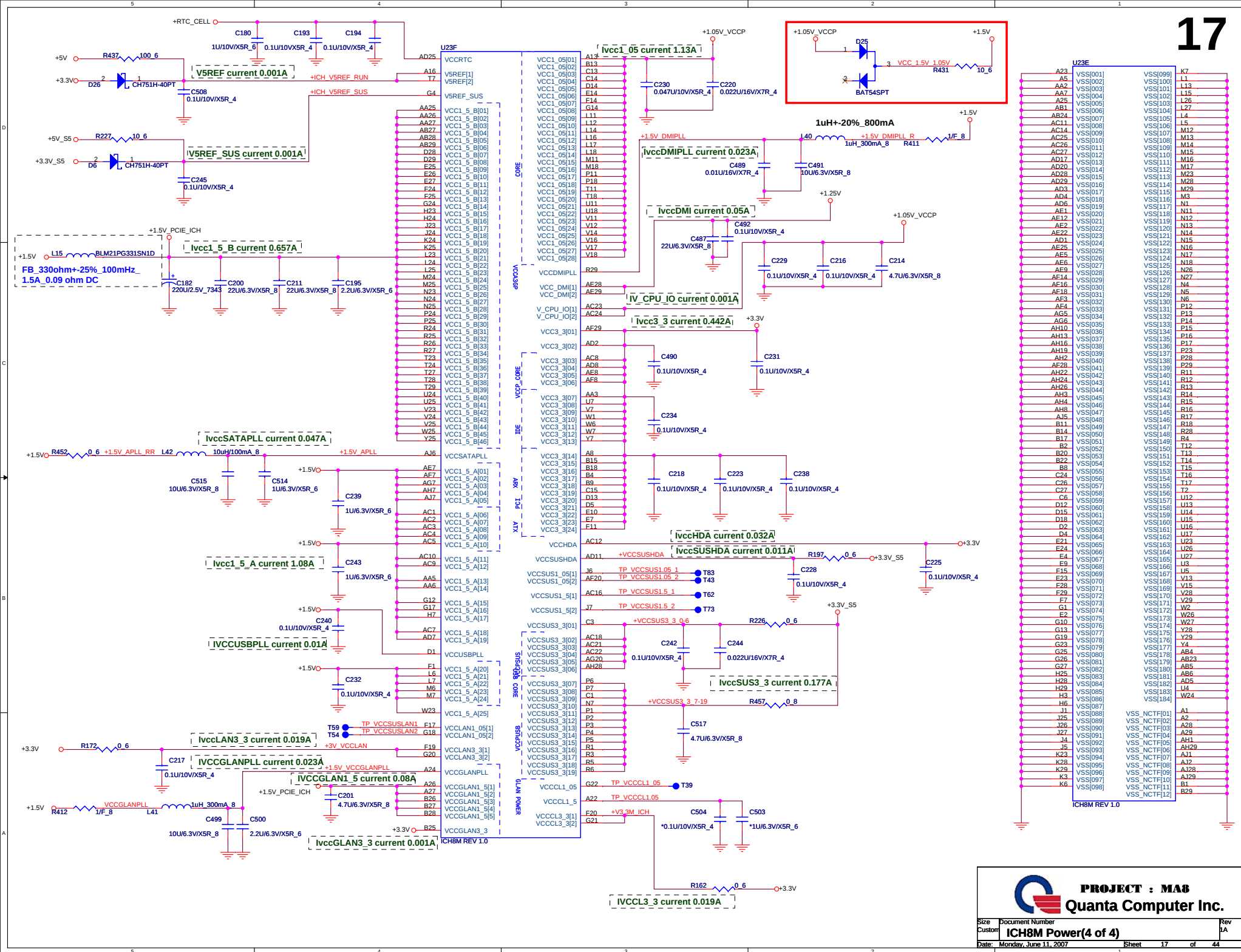
Board ID	ID3	ID2	ID1	ID0	Remark
1.Default(C-test)	1	1	1	1	
2.RSV	1	0	0	0	
3.RSV	1	0	0	1	
4.RSV	1	0	1	0	
5.RSV	1	0	1	1	
6.RSV	1	1	0	0	
7.RSV	1	1	0	1	
8.RSV	1	1	1	0	

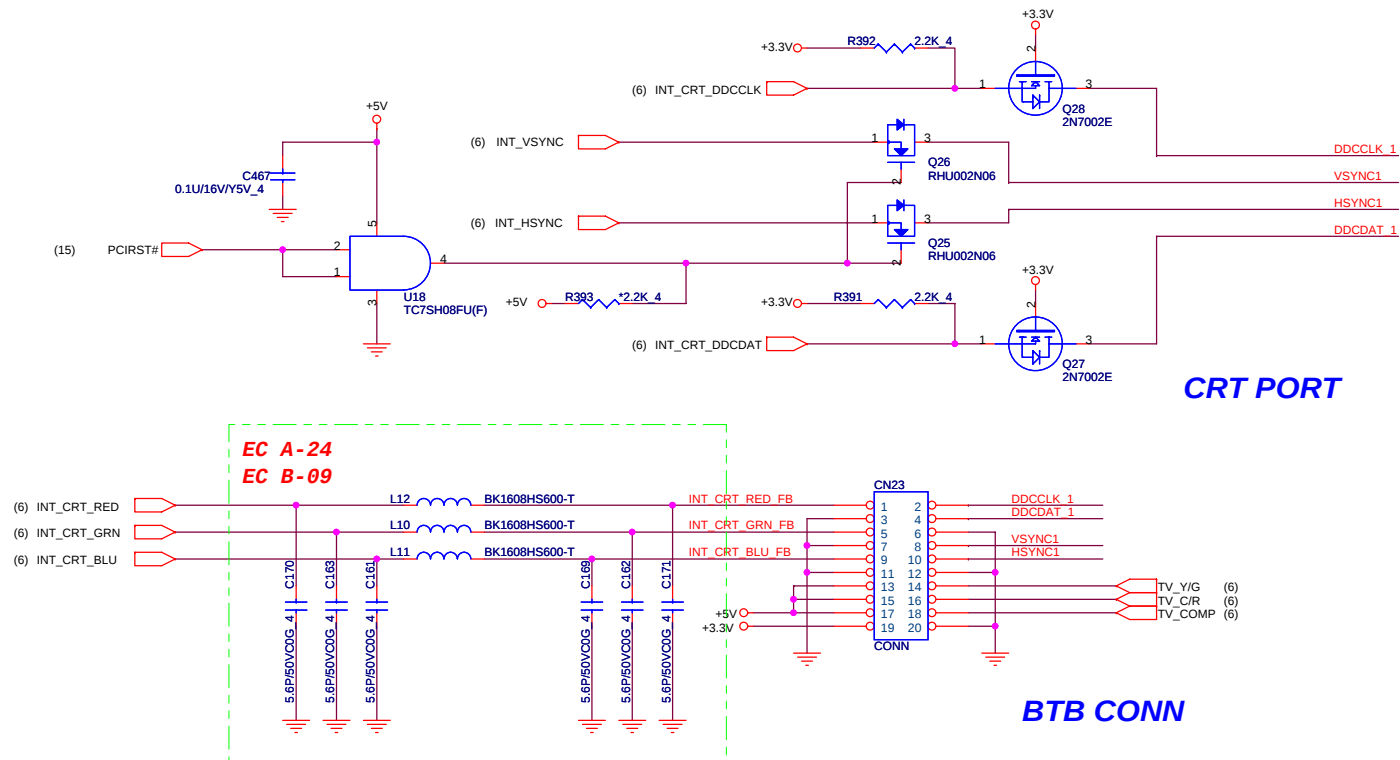
I[GPIO20]-Integrated Pull-Down 20K.

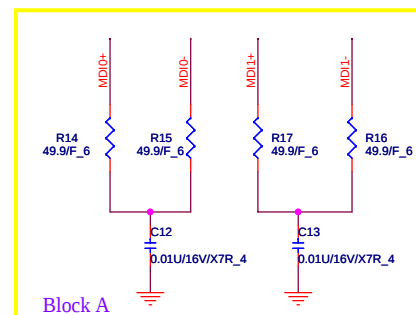
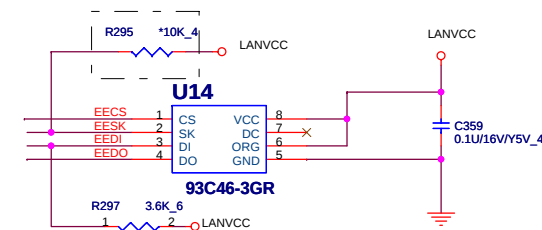
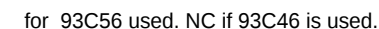
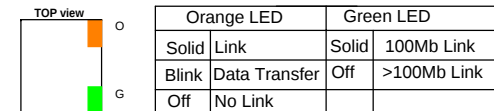


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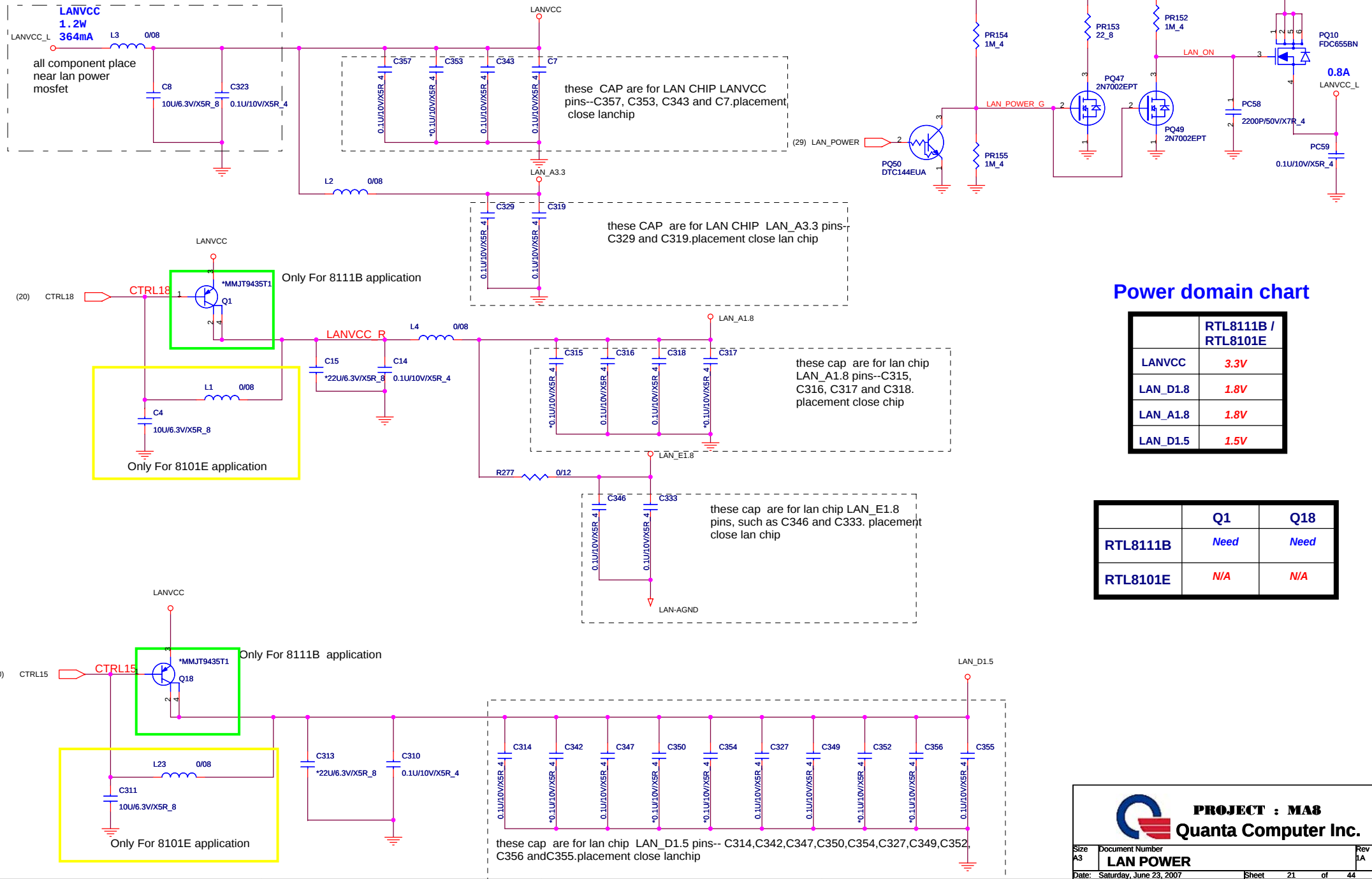




PARTS REFERENCE	RTL8101E	RTL8111B
R14 R15 R16 R17	ASM	NoASM

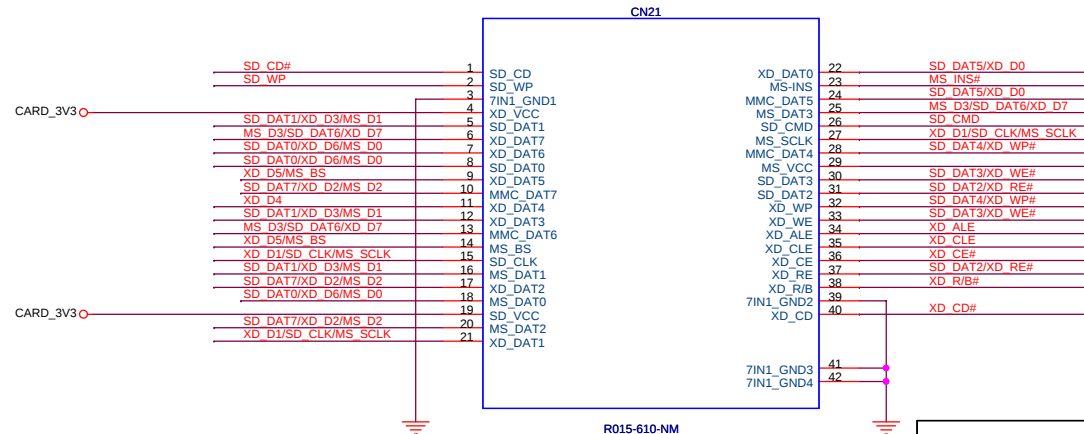
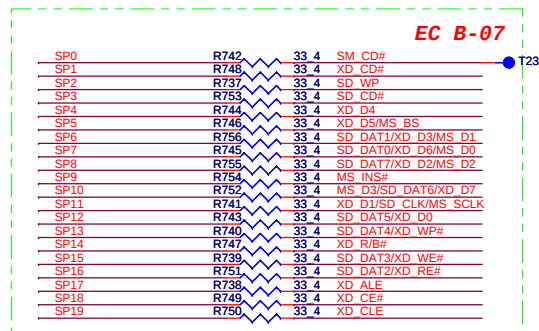
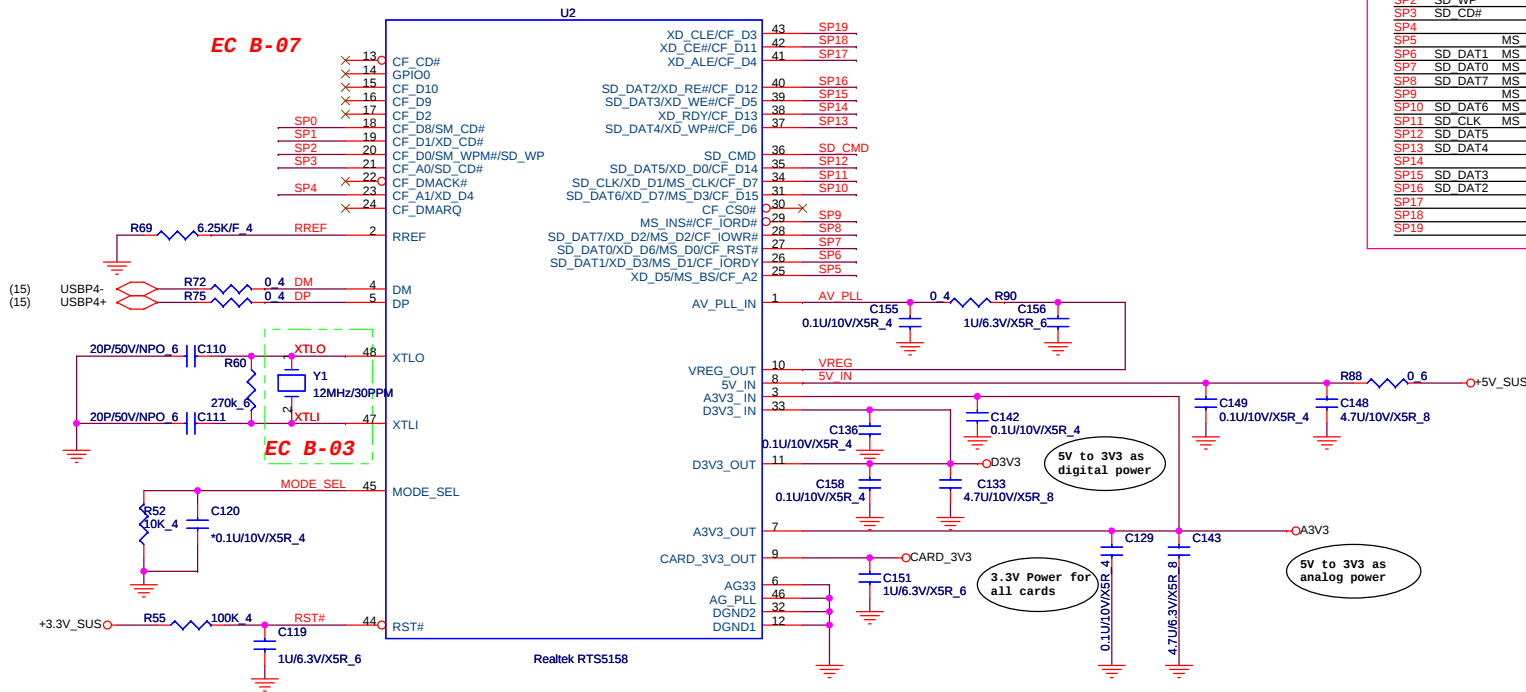
T : Stuffed for RTL8111B(10/100/1000)

E : Stuffed for 8101E(10/100)



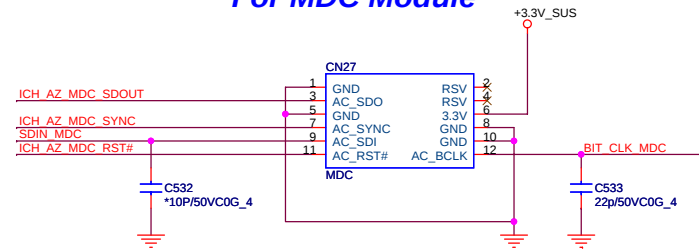
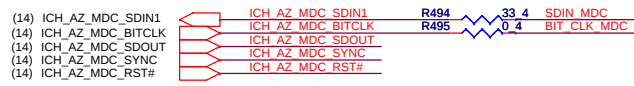
Note:

SP0	SD/MMC	MS	XD
SP1			XD CD#
SP2	SD WP		
SP3	SD CD#		
SP4			XD D4
SP5		MS BS	XD D5
SP6	SD DAT1	MS D1	XD D3
SP7	SD DAT0	MS D0	XD D6
SP8	SD DAT7	MS D2	XD D2
SP9		MS INS#	
SP10	SD DAT6	MS D3	XD D7
SP11	SD CLK	MS SCLK	XD D1
SP12	SD DAT5		XD D0
SP13	SD DAT4		XD WP#
SP14			XD R/B#
SP15	SD DAT3		XD WE#
SP16	SD DAT2		XD RE#
SP17			XD ALE
SP18			XD CE#
SP19			XD CLE

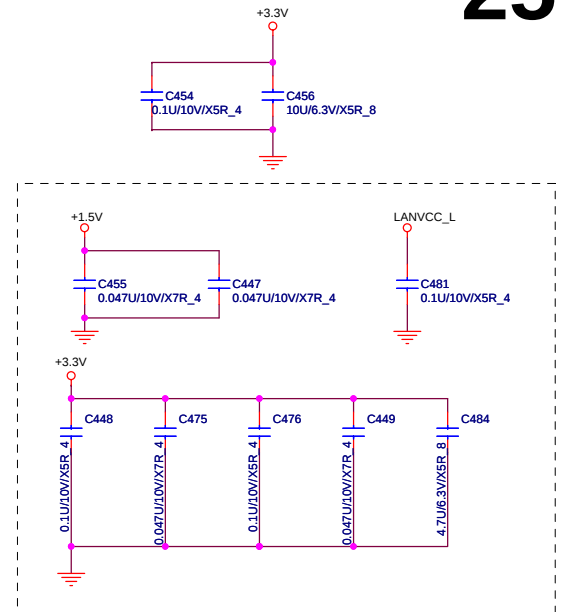


EC A-05

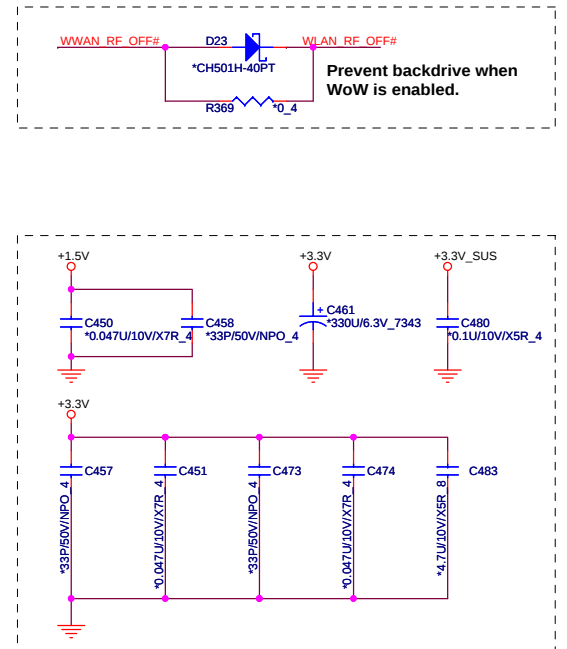
For MDC Module



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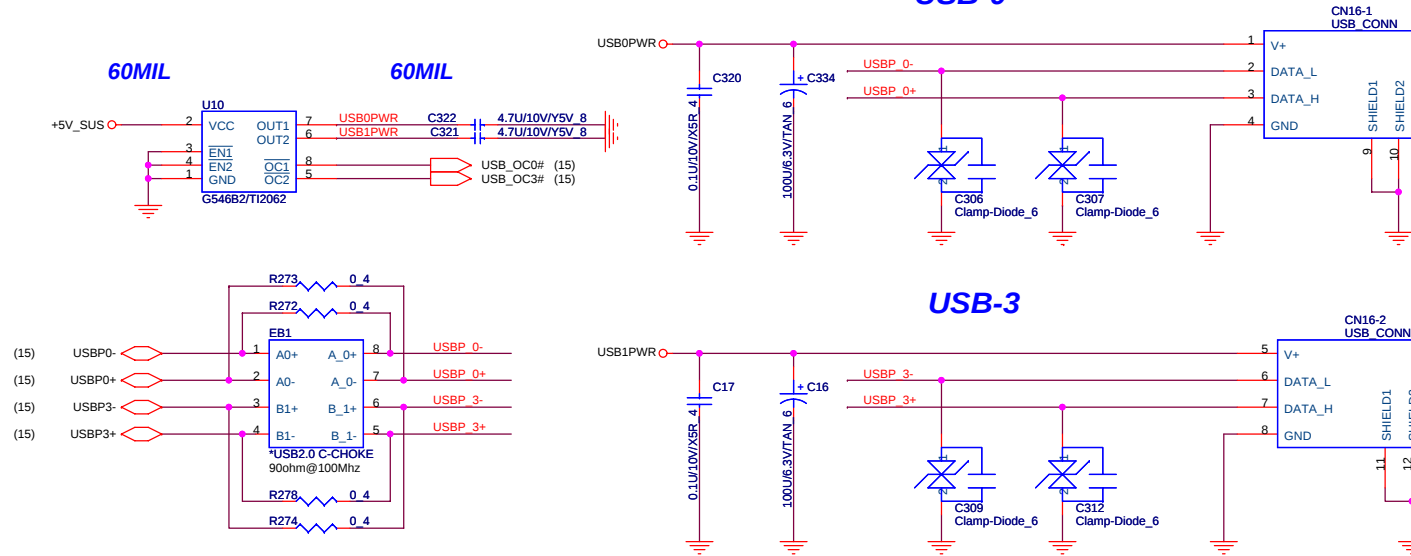


EC A-09



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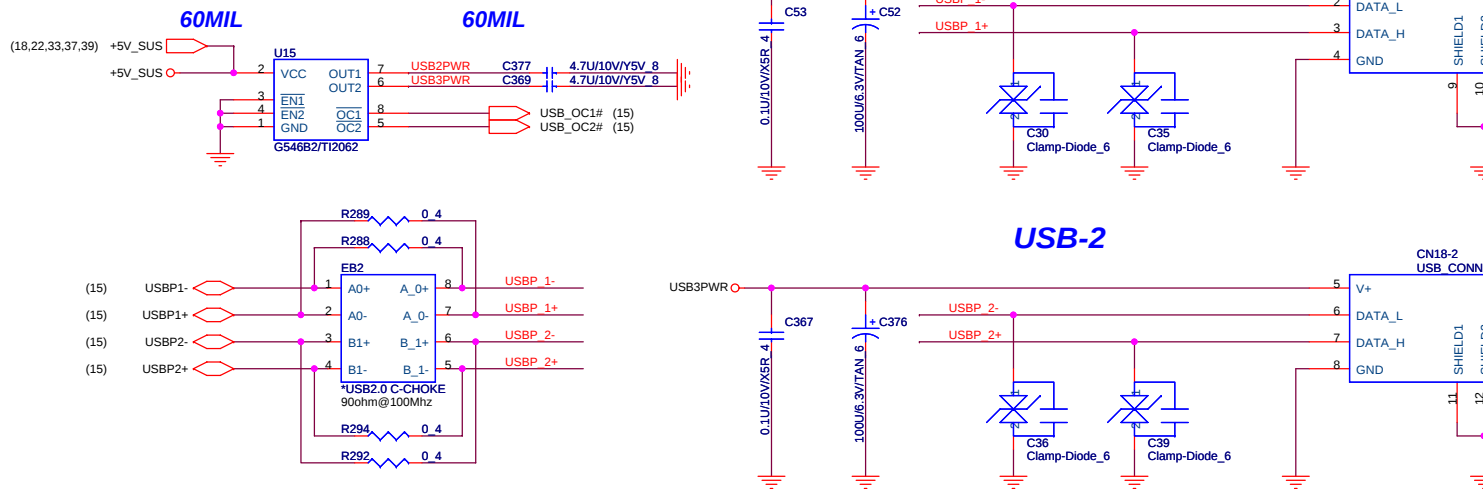
USB-0



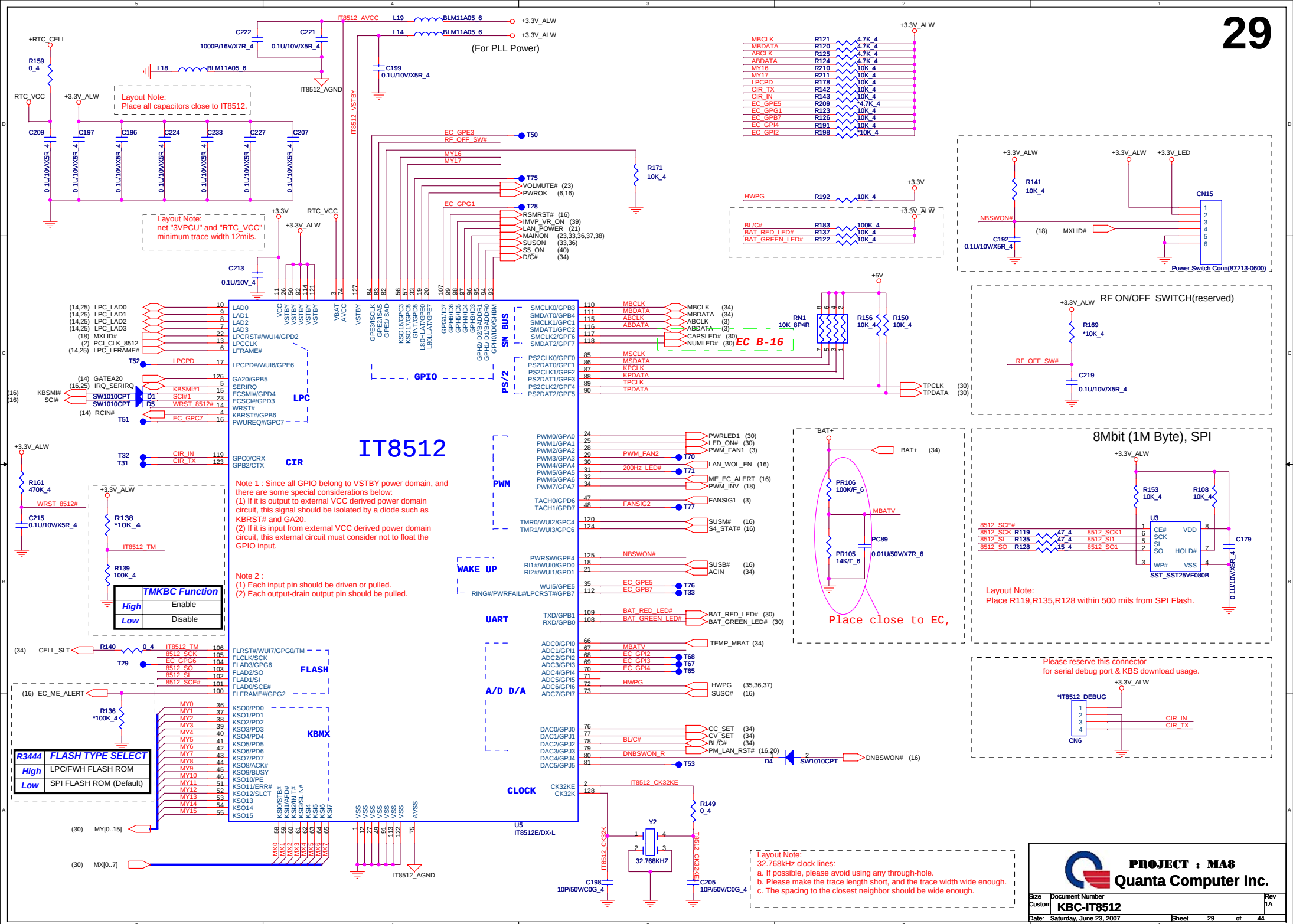
USB-3

USB-1

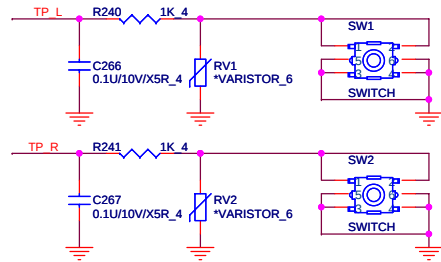
USB-2



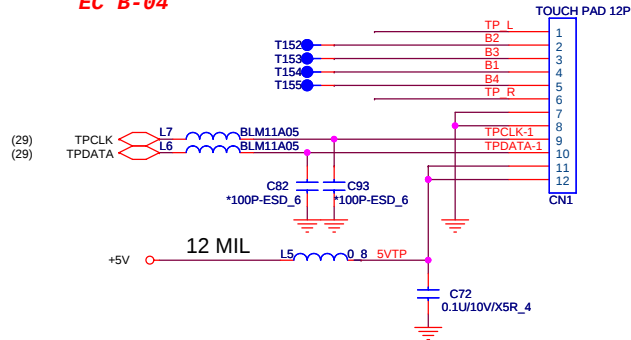
PROJECT : MA8
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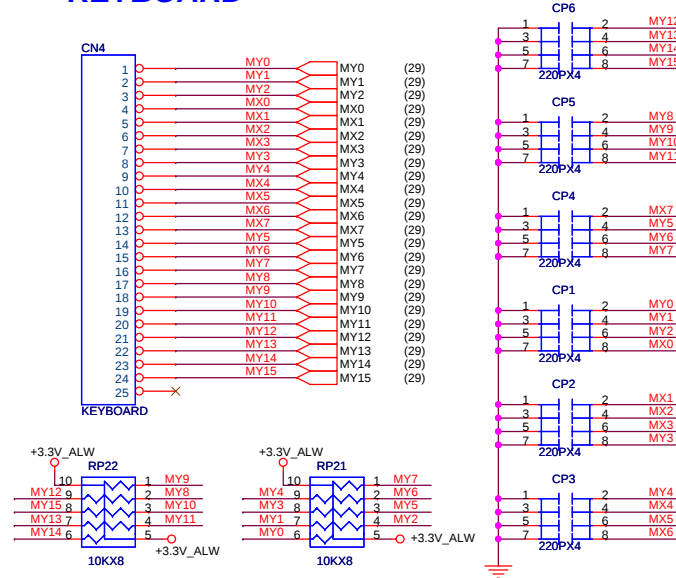
TOUCHPAD SWITCH CONN



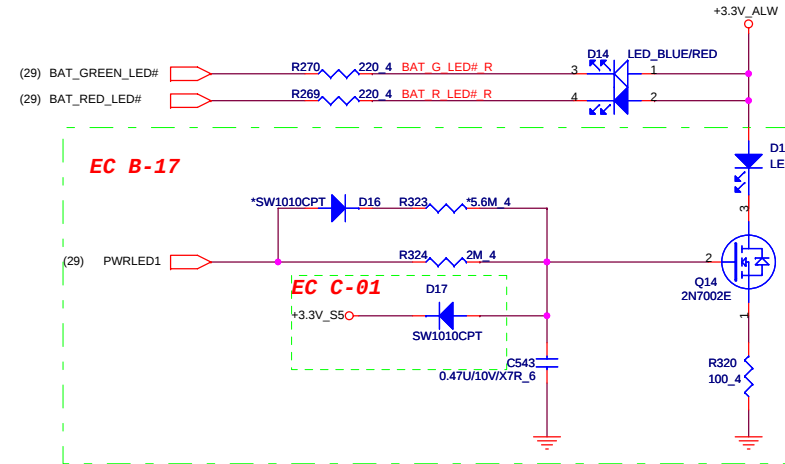
EC A-16
EC B-04



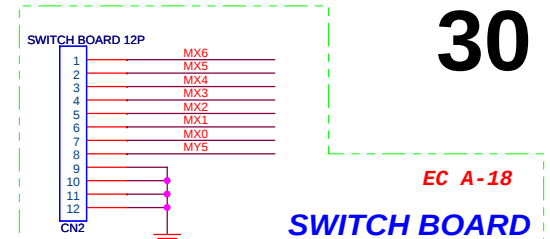
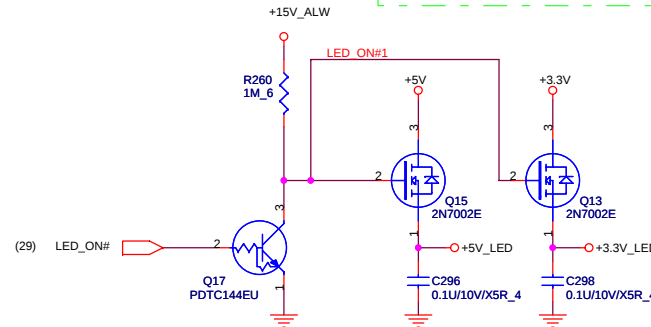
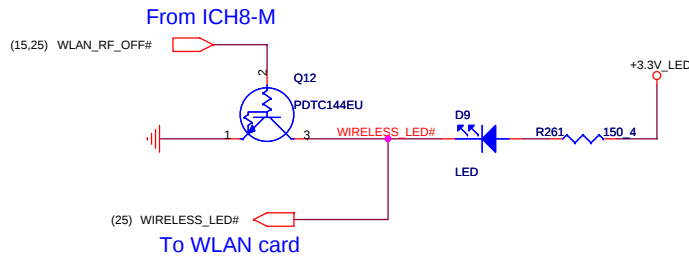
KEYBOARD



LED INDICATOR

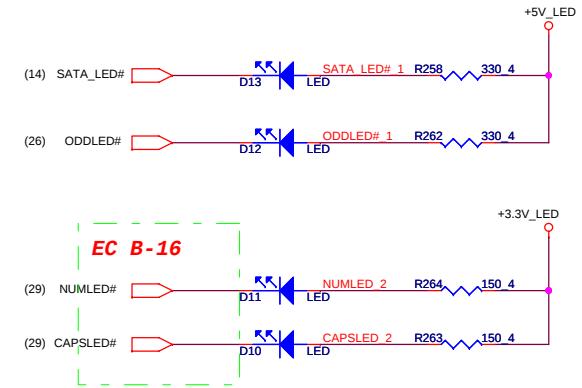


WIRELESS LED



30

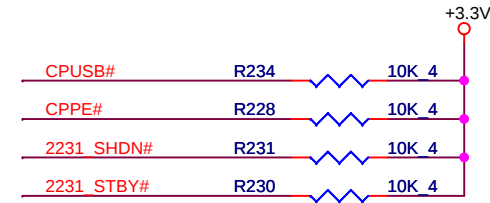
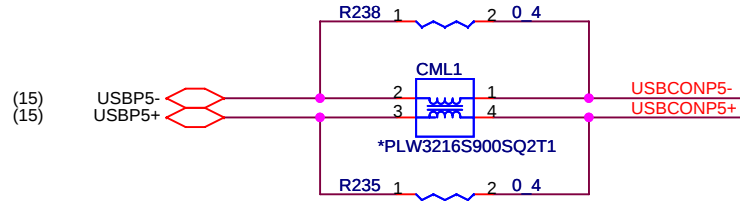
EC A-18
SWITCH BOARD



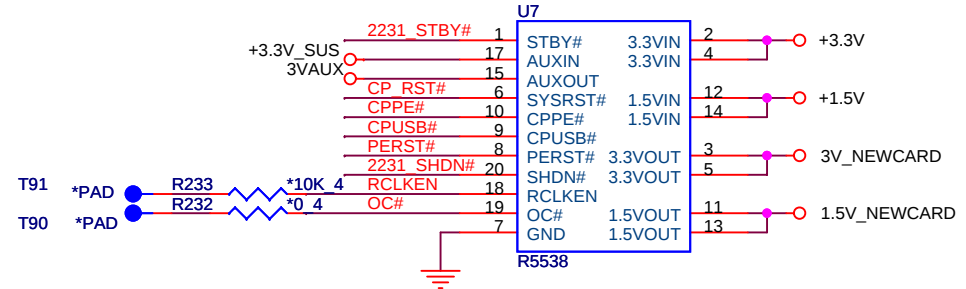
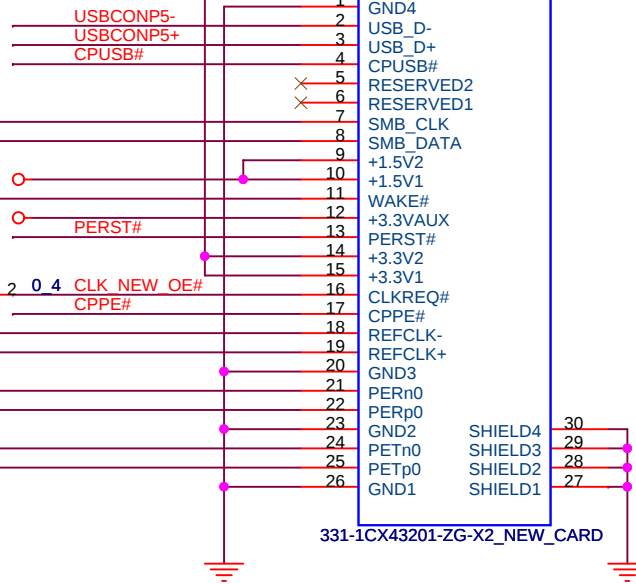
PROJECT : MA8
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Size A3 Document Number TP/KB/LED/SW. BOARD
Date: Saturday, June 23, 2007 Sheet 30 of 44

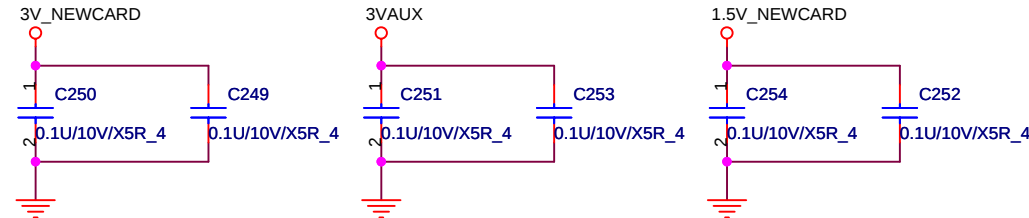
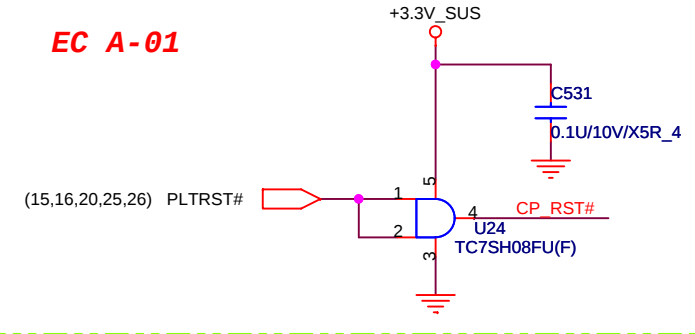
NEWCARD



3V_NEWCARD

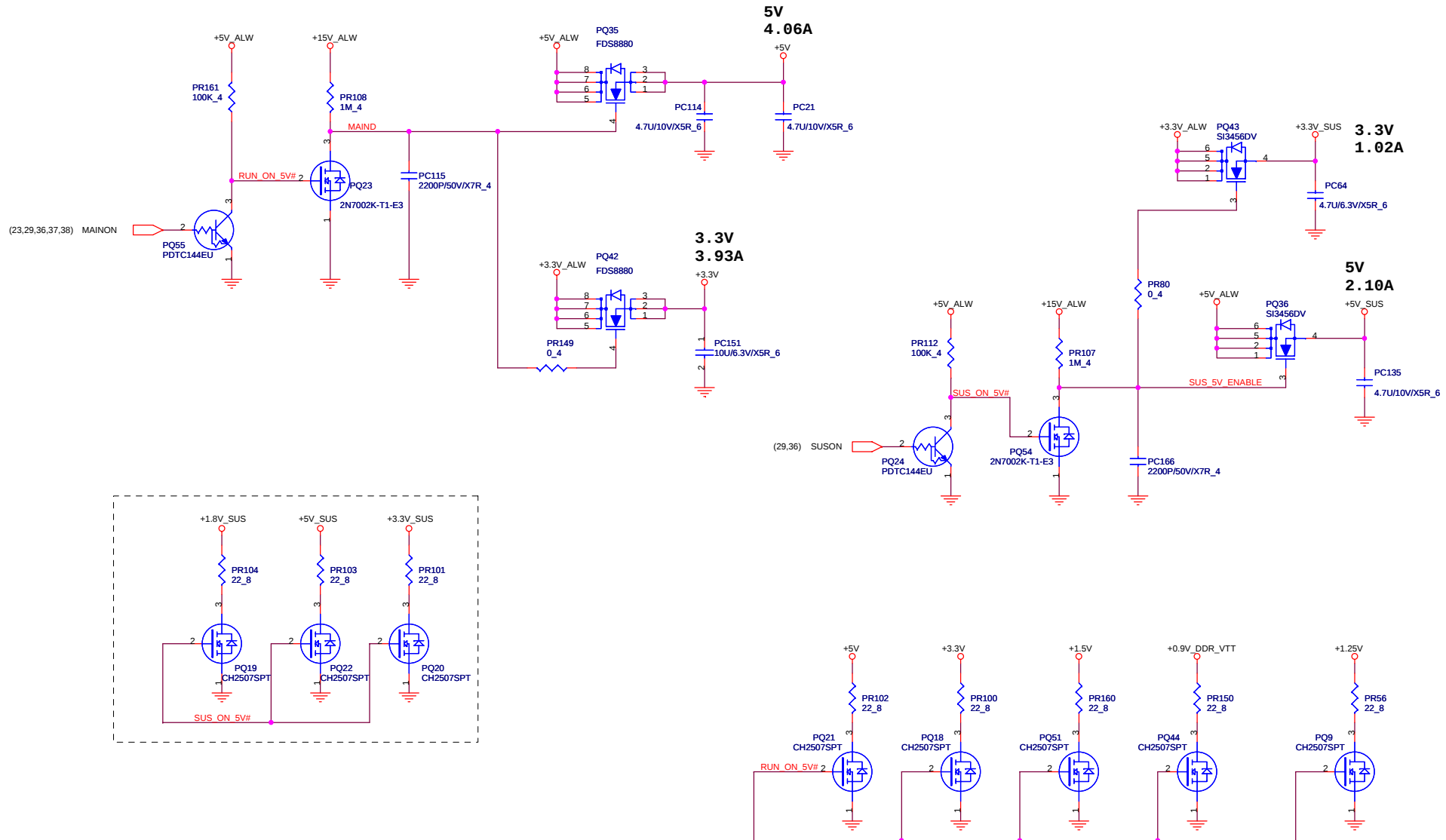


EC A-01

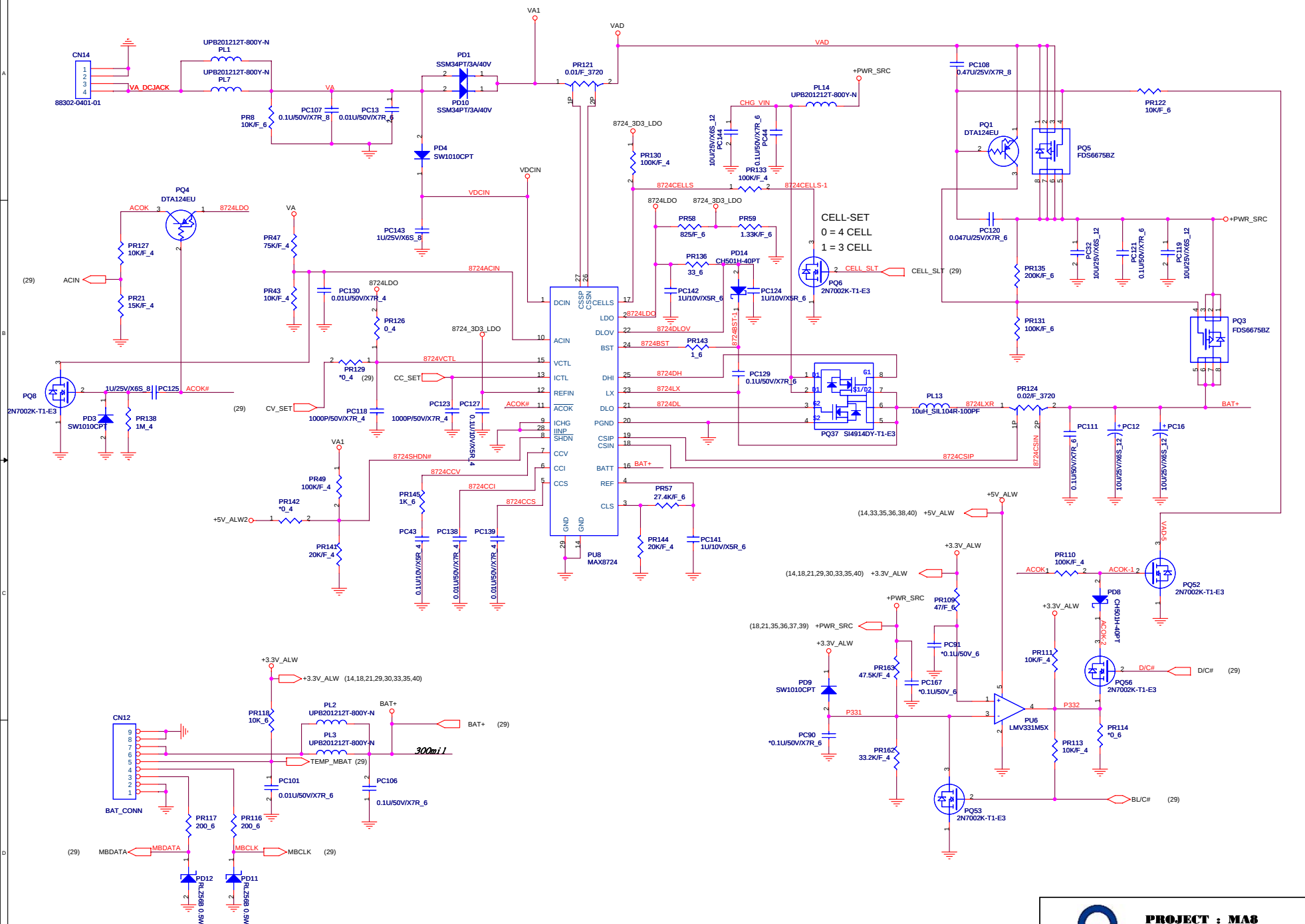


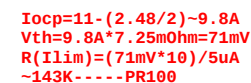
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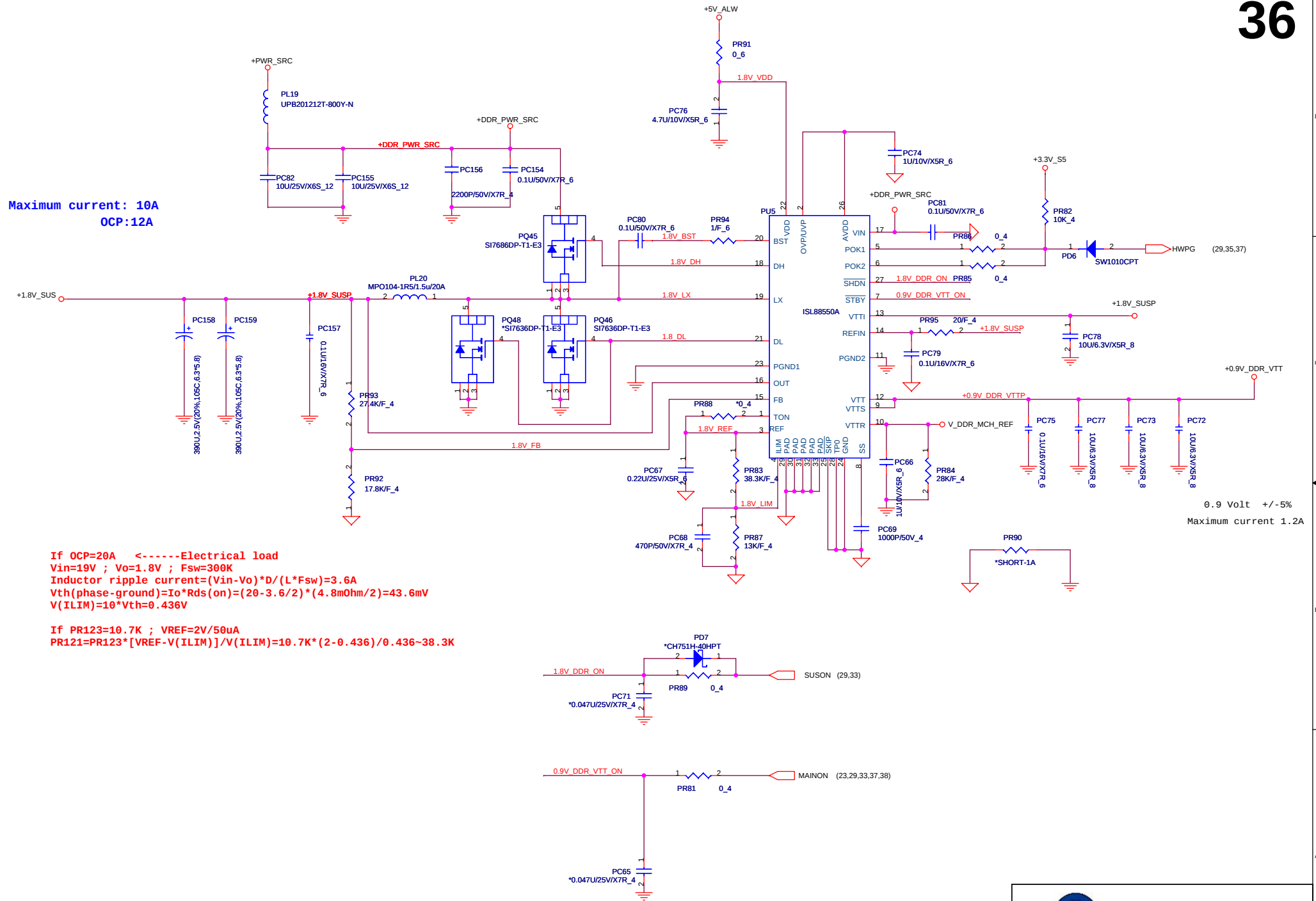


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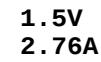
Maximum current: 10A
OCP:12A



If OCP=20A <-----Electrical load
 $V_{in}=19V$; $V_o=1.8V$; $F_{sw}=300K$
 Inductor ripple current= $(V_{in}-V_o)*D/(L*F_{sw})=3.6A$
 $V_{th}(\text{phase-ground})=I_o*R_{ds(on)}=(20-3.6/2)*(4.8m\Omega/2)=43.6mV$
 $V(ILIM)=10*V_{th}=0.436V$

If $PR123=10.7K$; $V_{REF}=2V/50\mu A$
 $PR121=PR123*[V_{REF}-V(ILIM)]/V(ILIM)=10.7K*(2-0.436)/0.436\sim 38.3K$

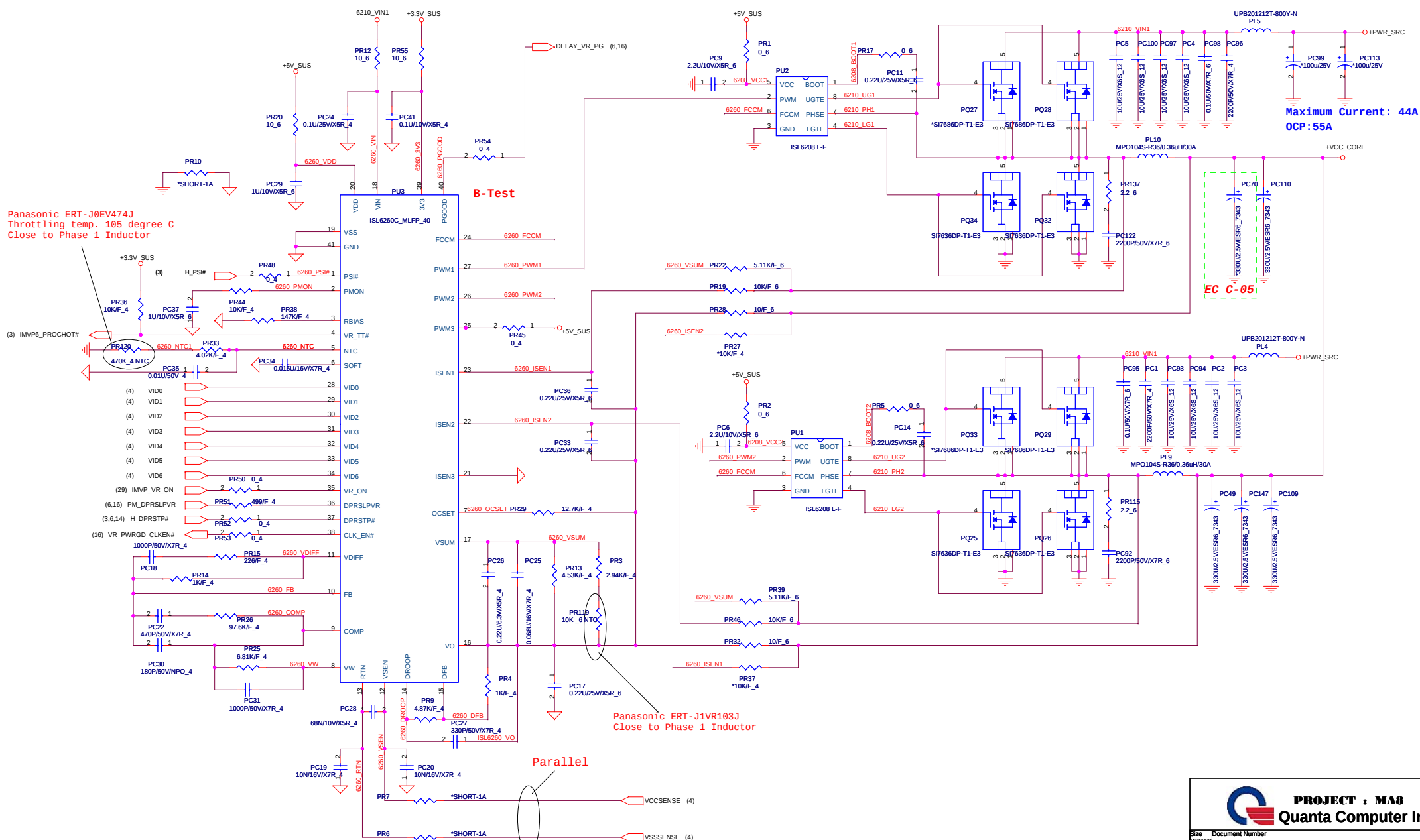
0.9 Volt +/-5%
 Maximum current 1.2A

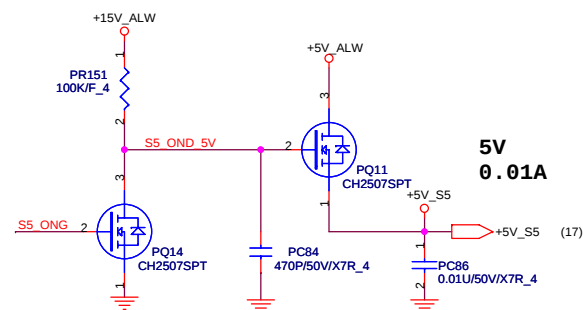
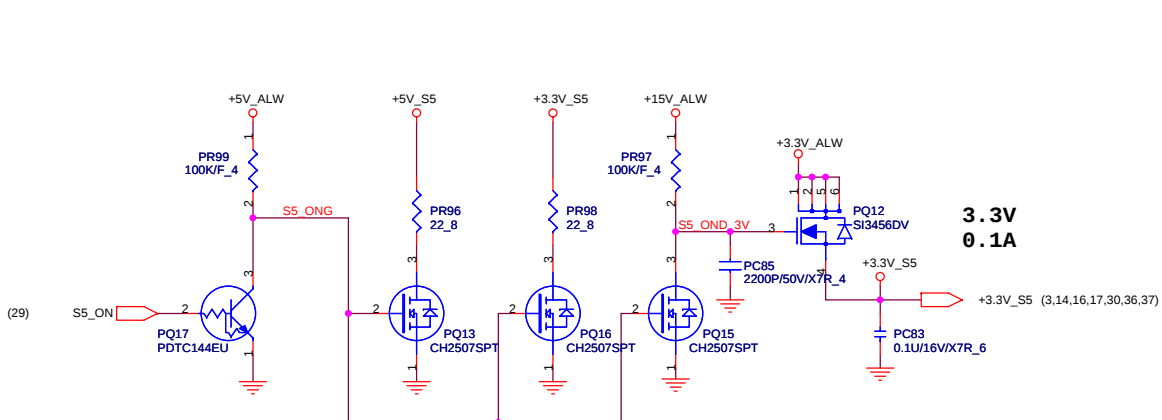




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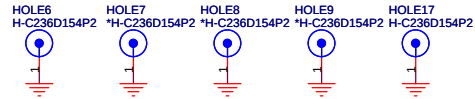




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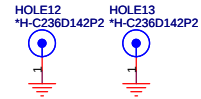
EC A-23 EC B-11

CPU SCREW HOLE

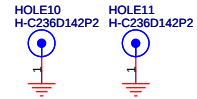


EC A-08

MINI PCI-E SCREW HOLE 2

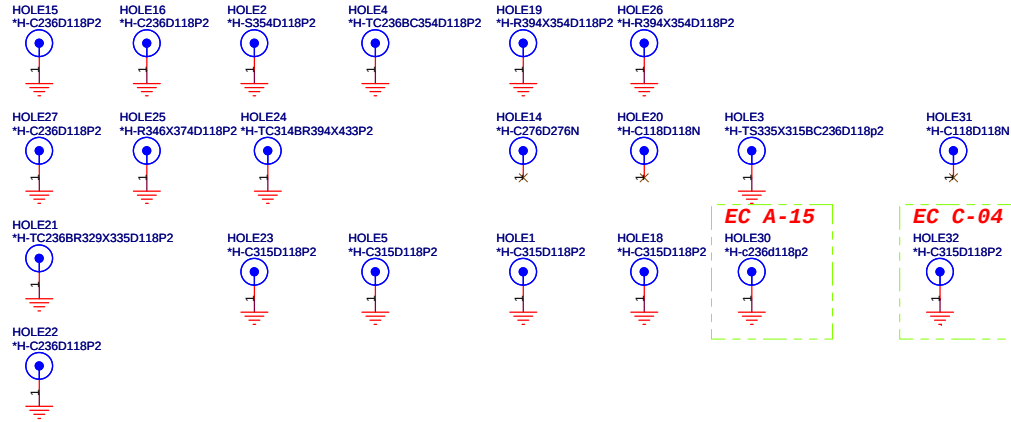
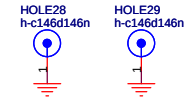


MINI PCI-E SCREW HOLE 1



EC A-06

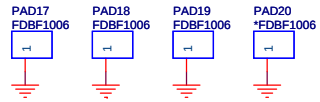
MDC SCREW HOLE



EC A-15

EC C-04

MODEM



PROJECT : MA8
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A-test to B-test EC list

MA8 Schematic EC Tracking Record A (for A --> B) JAN. 22, 2007

EC #/Page/Description/Part Affected

EC A-01 /31/ Add C531 & U24 to prevent leakage of current.

EC A-02 /30/ Remove CN2,L27,R322,R323 to eliminate Finger Print function according to latest hardware spec. from customer.

EC A-03 /18/ Remove resistor array chip RN2-RN9(0 Ohm) for LVDS

EC A-04 /15/ Add pull high resistor R322(10K_4) to OC#7

EC A-05 /24/ Change MODEM from MOM(modem on motherboard) to MDC(modem daughter card).So replace whole page of SILICON SI3054+SI3080(MODEM) with MDC board to board Conn. schematic.
R494,R495,C532,C533,CN27 were added in this schematic.

EC A-06 /41/ Add MDC SCREW HOLE==>HOLE28,HOLE29.

EC A-07 /23/ Remove R464 & depop R459 to normalize VOLMUTE# function

EC A-08 /41/ Depop 2 MINI PCI-E SCREW HOLE ==>HOLE12,HOLE13.

EC A-09 /25&15/ Depop MiniCard connector 2 and related parts as following list CN25,R96,R97,Q30,R380,R381,R390,C451,C457,C473,C474,C483,C450,C458,C480,D23,C185,C186

EC A-10 /18/ Remove R76 & R350 which connect to INT_LVDS_EDIDDATA & INT_LVDS_EDIDCLK respectively.

EC A-11 /18/ Remove C432, add R504,R464,R496,R497 for camera function

EC A-12 /14/ Change RTC from rechargeable to NON rechargeable.So, disable charging circuit by depop Q7,R186,R187,R205,R206 & replace CN5(Wire type) by BT1(Socket type).

EC A-13 /09/ Replace L9 with R498 & add C534(CRT signal quality)

EC A-14 /23/ Change the value of C301 & C302 from 1U/10V/X5R_6 to 2.2U/6.3V/X5R_6 for internal MIC function. Add internal MIC shcematic including following parts,R499,C536,R501,C535,C538,R503,CN28,R519,R520,C537,U25.

EC A-15 /41/ Add HOLE30 for keyboard

EC A-16 /30/ Change touchpad from TM61~G307 to TM61~G372 for cost down reason. But reserve schematic of G307 ,so add R505-R518 for the convenience of making option between G307 & G372.

EC A-17 /20/ Remove D16-D18,C2,C5 and add R194 for cost down reason.

EC A-18 /30/ Add CN2 for switch board.

EC A-19 /09/ Connect Pin AH50 & AH51 of U17 to +VCC_PEG, depop C542,C468,L35

EC A-20 /20/ Change U1 from NS892405 to NS892404 for layout

EC A-21 /20/ Add C600 for better signal intergrity due to PCIE_TX6-/GLAN_TX- & PCIE_TX6+/GLAN_TX+ change refrence plane on MB.

EC A-22 /20/ Delete CHASSIS_GND which connect with RJ45 for ESD. Remove C1,C11,C303,C305

EC A-23 /41/ Change Hole6,Hole7,Hole8,Hole9 to non-PTH hole to improve ESD.

EC A-24 /19/ Change L10,L11,L12 to 0 Ohm, depop C161,C162,C163,C169,C170,C171 to improve CRT performance.

B-test to C-test EC list

MA8 Schematic EC Tracking Record B (for B --> C) MAR. 20, 2007
EC #/Page/Description/Part Affected

- EC B-01 /03/ Reverse pin define of CN17 for layout.
- EC B-02 /23/ Add R521(1K ohm) to pull down MIC_DET for no MIC sku
- EC B-03 /22/ Change the Y1, 12MHz (foot print: XTAL-3_2X2_5-2_3X1_9) to the big size (Y5: FSX-7B) for cost down reason.
- EC B-04 /30/ Remove R505-R518 which provide the option between TM61~G307 & TM61~G372 on B-test. C-test will use only TM61~G372.
- EC B-05 /03/ Stuff ITP resistor R7,R8,R12,R13,R29.
- EC B-06 /06/ R61,R62,R63 change to 0 Ohm for cost down.
- EC B-07 /22/ Change R737-R756 from 0ohm to 33ohm.
- EC B-08 /20/ Connect pin13-16 of CN13 to GND to improve ESD.
- EC B-09 /19/ Change L10,L11,L12 to BK1608HS600-T, pop up C161,C162,C163,C169,C170,C171 to improve EMI.
- EC B-10 /18/ Add C432(1000p) to +5V at pin32 of CN3.
- EC B-11 /41/ Connect Hole6-9 to GND to improve ESD.
- EC B-12 /23/ C282,C283,C284,C285 change from capacitor to varistor.
- EC B-13 /03/ Add varistor C539,C540,C541 in parallel to ITP_DBRESET#,H_RESET# & ITP_TRST# respectively.
- EC B-14 /23/ Add R316 & R317 both 0ohm resistor between analog GND plane and digital GND.
- EC B-15 /02/ Remove R104(GCLK_SEL) due to MA8 don't support external VGA
- EC B-16 /29/30/ Remove Q14,Q16 and change NUMLED#/CAPLED# to low active for cost down reason.
- EC B-17 /30/ Change PWRLLED schematic for cost down reason.

C-test to FAI EC list

MA8 Schematic EC Tracking Record C (for C --> FAI) June. 01, 2007

EC #/Page/Description/Part Affected

- EC C-01 /30/ Add D17 to discharge C543 when power off.So, D15 will not light up at the beginning of power turn on.
- EC C-02 /26/ Add pull high R256(4.7K) & R255(8.2K) separately to IDE_IRQ & IDE_DIORDY according to intel DSGL.
- EC C-03 /23/ Add C546,C547,C548 for ESD solution.
- EC C-04 /41/ Add Hole32.
- EC C-05 /39/ Add back PC70 for +VCC_CORE