MA3 BLOCK DIAGRAM

AMD Athlon 64 & Sempron / RS482M / IXP400

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : VCC
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : GND
- LAYER 6 : BOT

DDR-SODIMM1 P9

DDR-SODIMM2 P10

DDR 266,333,400MHz

AMD Athlon 64 & Sempron CPU
754 Pins (uPGA)
P3,4

CPU THERMAL SENSOR
GMT-781
P3

14.318MHz

CPUCLK, CPUCLK#

CLOCK GEN
CY28RS480/ ICS951412
P2

SBLINKCLK, SBLINKCLK#
NBSRCCLK, NBSRCCLK#
HTREFCLK

HyperTransport I/O BUS
Link 16x16

SYSTEM POWER 1.2V & VTT_DDR P35

CPU CORE MAX1544 POWER P36

SYSTEM MAX1999 POWER(3/5V) P33

SYSTEM POWER MAX1845 (2.5VSUS/1.8VSUS) P34

BATT CHARGER MAX1722 P32

DISCHARGE P31

CRT port P18 — R.G,B

LCD Panel P18 — LVDS X1

S-VIDEO P18 — TV-OUT

NORTH BRIDGE RS480M/RS482M
705 BGA
INTEGRATED VGA FUNCTION
Based on Redeon 9600
P5,6,7,8

OSC14M

300MHz

64MB LFB/RS480M
P12

SRC_LAN, SRC_LAN#

A-LINK 2X PCI-E

32.768KHz

1X PCI-E

NBSRCCLK, NBSRCCLK#

USB PORT 0, 1, 2,3 P30 — USB 2.0

1st IDE - HDD P29 — ATA 66/100/133

2nd IDE - ODD P29 — ATA 66/100/133

IXP400
564 BGA
P13,14,15,16,17

33MHZ, 3.3V PCI
PCLK_7411
PCLK_MINI

24.576MHz 48MHz

AC97

PWRCLKP
PWRCLKN
DIB_DATAN
DIB_DATAP

AC97
CX20468-31
P24

LAN
Marvell
88E8036
P21

MINI-PCI
P23

CARDBUS / IEEE 1394/CARD READER
TI 7411
P19,20

24.576MHz 25MHz

32.768KHz PCLK_591 **3.3V LPC, 33MHz**

PC97551
TQFP 176
P27

SMARTDAA MODEM,
DAA_20493-21
P25

AMP
TPA0312
P26

3 IN 1
CARD READER SD/MMC, MS
P20

CARDBUS SLOT X1
P19

1394 CONN
P20

WIRE

FAN P28

Touchpad P28

Keyboard P28

FLASH P27

RJ11 JACK P22

AUDIO JACK P26

RJ45 JACK P22

PCI DEVICES IRQ ROUTING

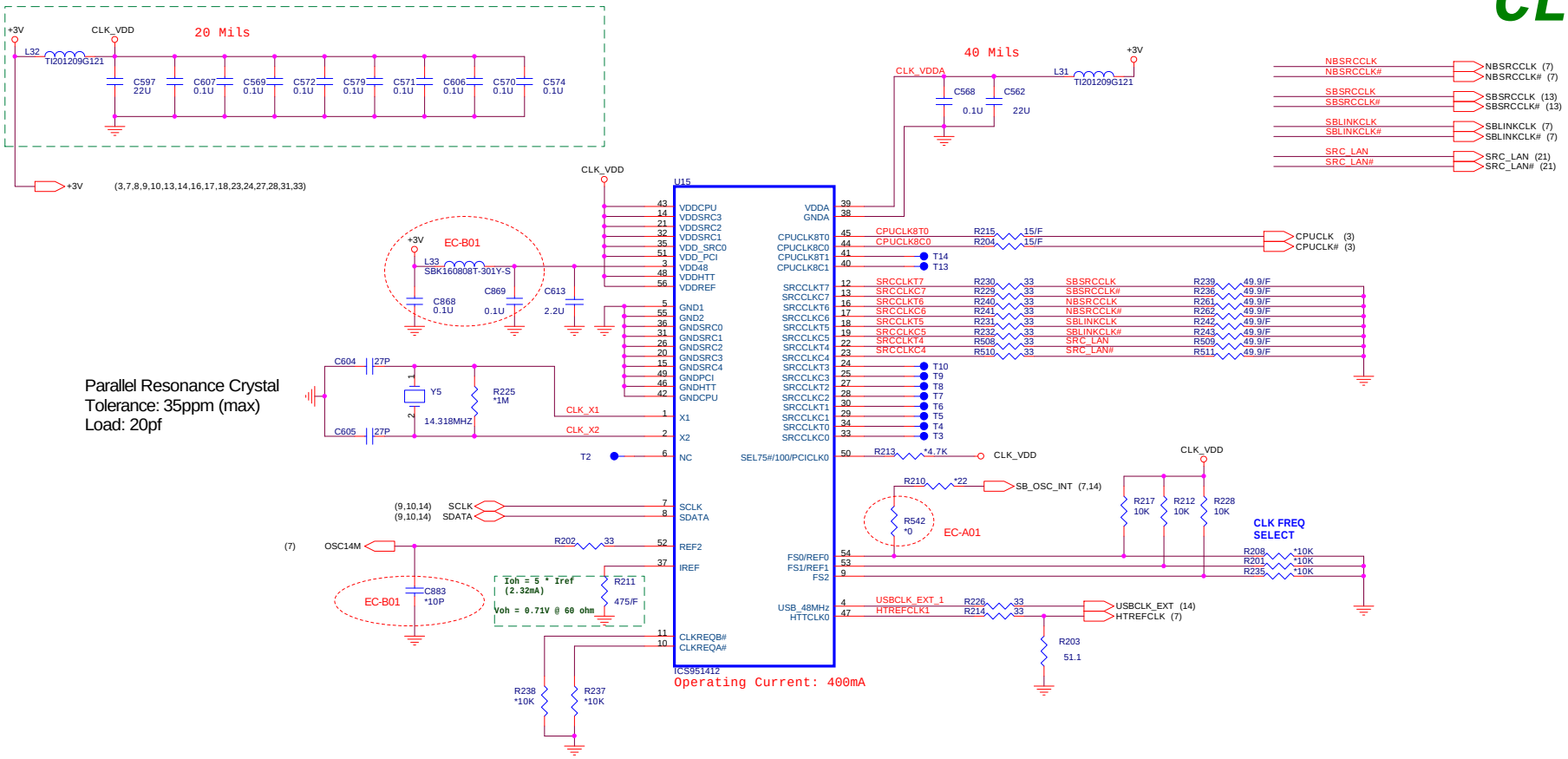
DEVICE	IDSEL #	REQ/GNT #	PCI_INT
MINIPCI SLOT	AD18	1	F,G
CardBus/1394	AD25	4	E,F,H

PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3B

Date: Thursday, October 27, 2005 Sheet 1 of 37

CLK



Layout Note:

1- PLACE ALL THE SERIES TERMINATION RESISTORS AS CLOSE AS CKG. AS POSSIBLE

2- ROUTE ALL CPUCLK/#, NBSRCCLK/#, SBSRCCLK/#, SBLINKCLK/# AS DIFFERENT PAIR RULE

3- PUT DECOUPLING CAPS CLOSE TO CKG. POWER PIN

EXT CLK FREQUENCY SELECT TABLE(MHZ)

FS2	FS1	FS0	CPU	SRCCLK [2:1]	HTT	PCI	USB	COMMENT
0	0	0	Hi-Z	100.00	Hi-Z	Hi-Z	48.00	Reserved
0	0	1	X	100.00	X/3	X/6	48.00	Reserved
0	1	0	180.00	100.00	60.00	30.00	48.00	Reserved
0	1	1	220.00	100.00	36.56	73.12	48.00	Reserved
1	0	0	100.00	100.00	66.66	33.33	48.00	Reserved
1	0	1	133.33	100.00	66.66	33.33	48.00	Reserved
1	1	1	200.00	100.00	66.66	33.33	48.00	Normal HAMMER operation

PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	EXT CLOCK GENERATOR	3A
Date: Thursday, October 27, 2005	Sheet 2 of 37	

CPU

20 Mils width to pin
100 Mils width to capacitor
250 Mils width to PWM

U30A
AMD K8
LDT

U30C
AMD K8
CTL & DBG

Near Socket754

STUFF WHEN CONFIGURED AS 16-BIT LINK

H/W MONITOR

Output current(Max):
300mA

50 Mils, routing as 15 mils width if the distance from bead to cpu pin less than 1000 mils.

Rb Vout=1.25(1+Ra/Rb)
Ra=Rb(Vout/1.25-1)

PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU H.T/CTL I/F	3B
Date: Thursday, October 27, 2005	Sheet 3 of 37	

CPU

20 mils width to CPU pins.

U30E
AMD K8
GROUND

U30B
AMD K8
MEMORY

U30D
AMD K8
POWER

LAYOUT: Place close to CPU.

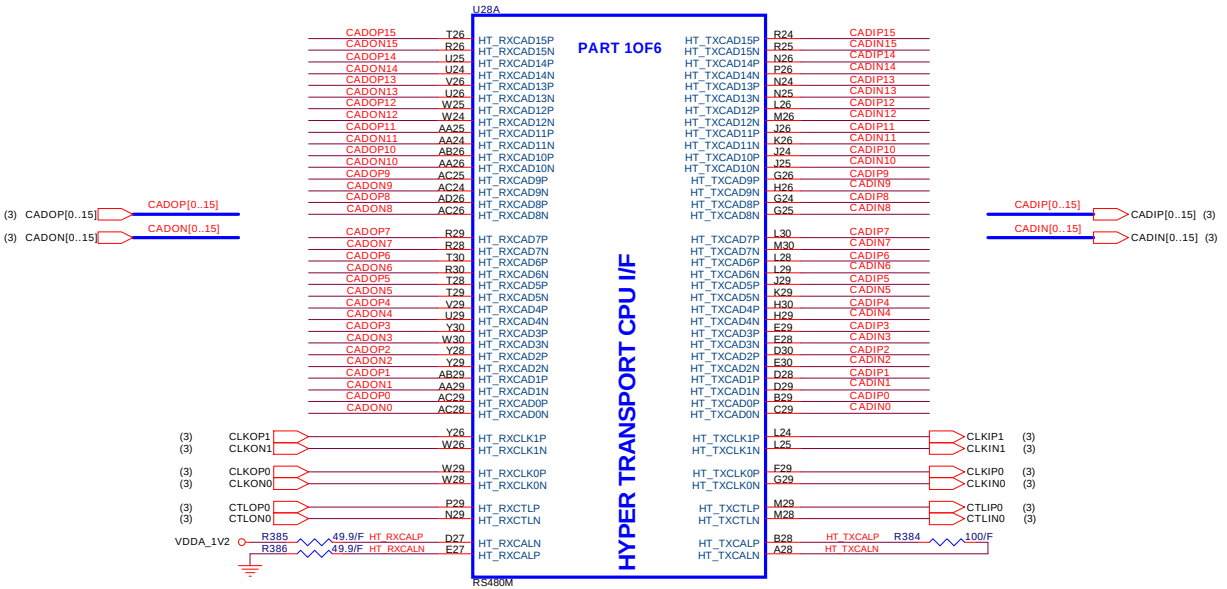
60 mils

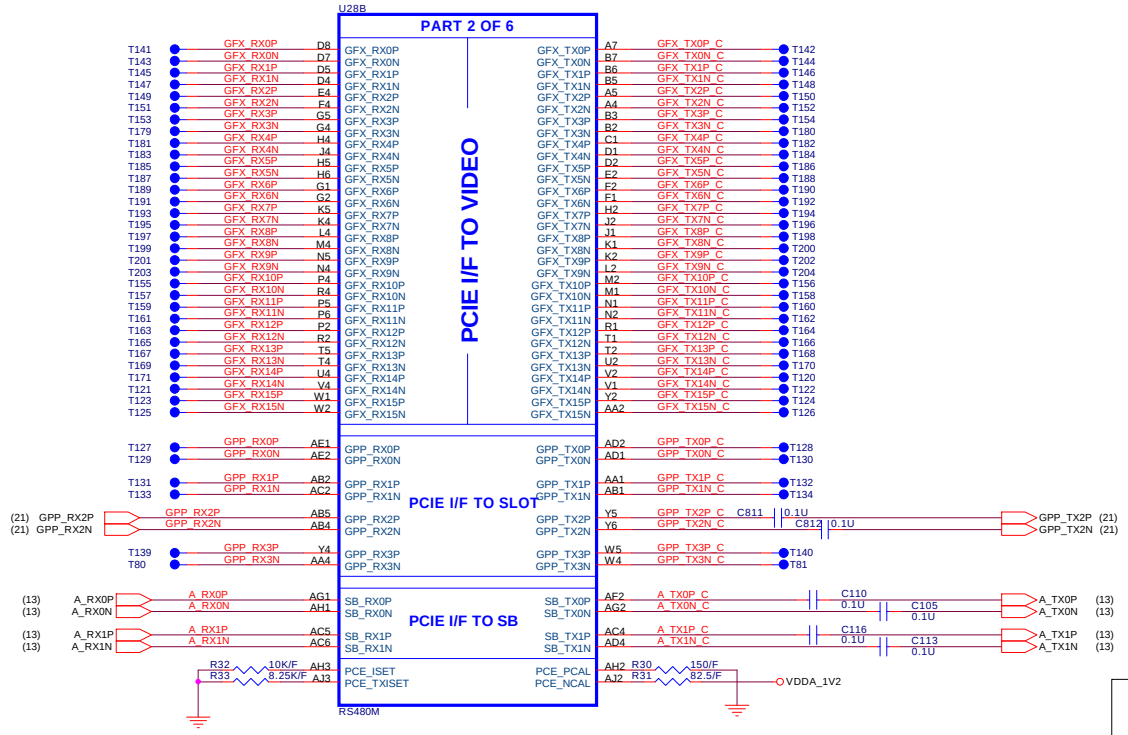
W/S 15/20 mils

PROJECT : MA3	
Quanta Computer Inc.	
Size: Custom	Document Number: CPU DDR/POWER I/F
Rev: 1A	
Date: Thursday, October 27, 2005	Sheet 4 of 37

Link 0 Is Clawhammer <--> RS480

CLG



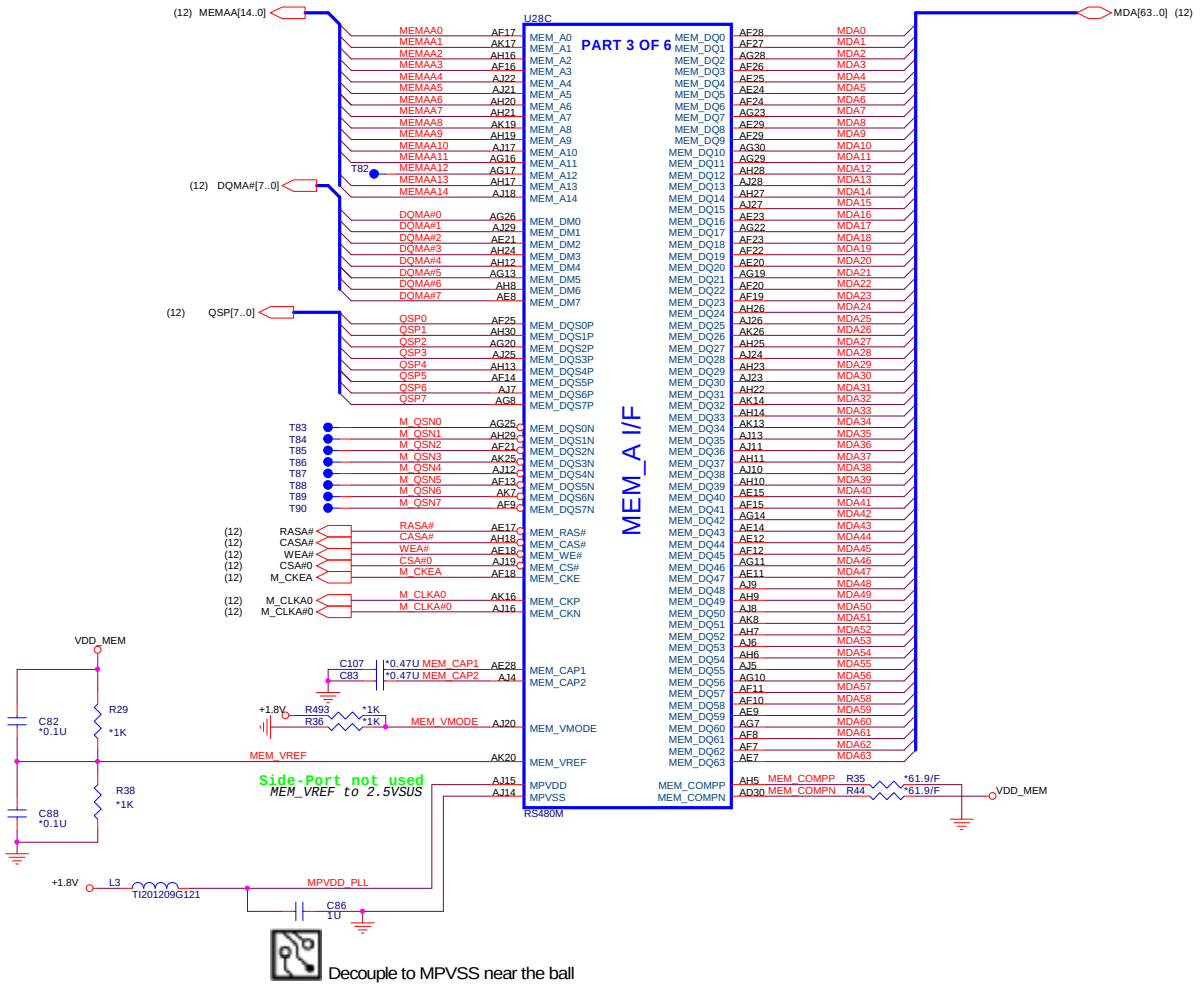


PROJECT : MA3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-HT A-LINK0	1A
Date: Thursday, October 27, 2005	Sheet 5 of 37	

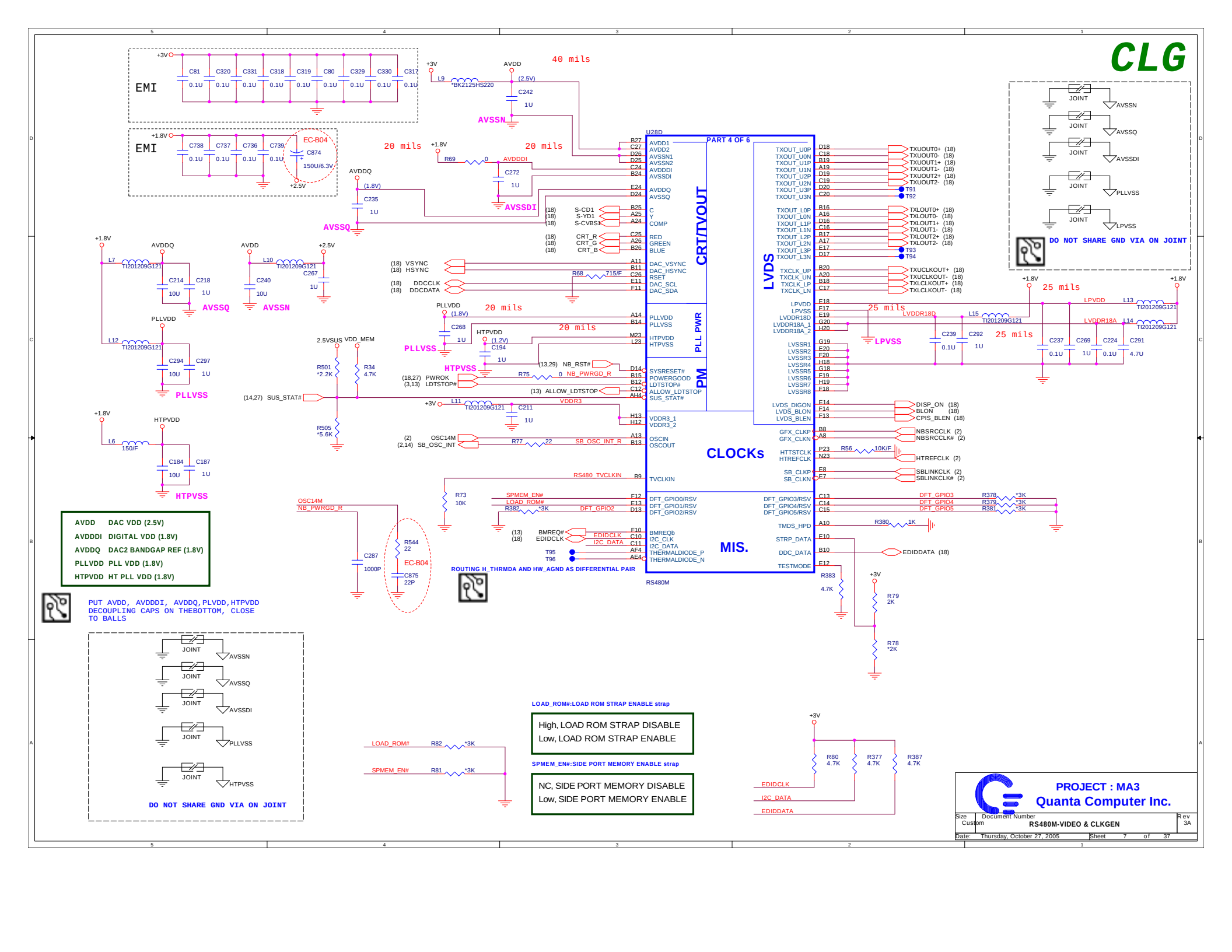
CLG



PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RS480M-SIDE PORT MEM I/F	1A

Date: Thursday, October 27, 2005 Sheet 6 of 37


CLG
EMI
EMI
EC-B04
EC-B04
U28D
PART 4 OF 6
CRT/TVOUT
LVDS
PLL PWR
PM
CLOCKs
MIS.
RS480M
AVDD1
AVDD2
AVSSN1
AVSSN2
AVDDI
AVSSDI
AVDDQ
AVSSQ
C
Y
COMP
RED
GREEN
BLUE
DAC_VSYNC
DAC_HSYNC
RSET
DAC_SCL
DAC_SDA
PLLVDD
PLLVSS
HTPVDD
HTPVSS
SYSRESET#
POWERGOOD
LDTSTOP#
ALLOW_LDTSTOP
SUS_STAT#
VDDR3_1
VDDR3_2
OSCIN
OSCOUT
TVCLKIN
DFT_GPIO0/RSV
DFT_GPIO1/RSV
DFT_GPIO2/RSV
BMREQb
I2C_CLK
I2C_DATA
THERMALDIODE_P
THERMALDIODE_N
TXOUT_U0P
TXOUT_U0N
TXOUT_U1P
TXOUT_U1N
TXOUT_U2P
TXOUT_U2N
TXOUT_U3P
TXOUT_U3N
TXOUT_L0P
TXOUT_L0N
TXOUT_L1P
TXOUT_L1N
TXOUT_L2P
TXOUT_L2N
TXOUT_L3P
TXOUT_L3N
TXCLK_UP
TXCLK_UN
TXCLK_LP
TXCLK_LN
LVDS_DIGON
LVDS_BLON
LVDS_BLEN
GFX_CLKP
GFX_CLKN
HTTSTCLK
HTREFCLK
SB_CLKP
SB_CLKN
DFT_GPIO3/RSV
DFT_GPIO4/RSV
DFT_GPIO5/RSV
TMDS_HPD
STRP_DATA
DDC_DATA
TESTMODE
LPVDD
LVDDR18D
LVDDR18A_1
LVDDR18A_2
LVSSR1
LVSSR2
LVSSR3
LVSSR4
LVSSR5
LVSSR6
LVSSR7
LVSSR8
JOINT
AVSSN
AVSSQ
AVSSDI
PLLVSS
LPVSS
DO NOT SHARE GND VIA ON JOINT
AVDD DAC VDD (2.5V)
AVDDDI DIGITAL VDD (1.8V)
AVDDQ DAC2 BANDGAP REF (1.8V)
PLLVDD PLL VDD (1.8V)
HTPVDD HT PLL VDD (1.8V)
PUT AVDD, AVDDDI, AVDDQ,PLVDD,HTPVDD DECOUPLING CAPS ON THEBOTTOM, CLOSE TO BALLS
ROUTING H_THRMDA AND HW_AGND AS DIFFERENTIAL PAIR
LOAD_ROM#:LOAD ROM STRAP ENABLE strap
High, LOAD ROM STRAP DISABLE
Low, LOAD ROM STRAP ENABLE
SPMEM_EN#:SIDE PORT MEMORY ENABLE strap
NC, SIDE PORT MEMORY DISABLE
Low, SIDE PORT MEMORY ENABLE
PROJECT : MA3
Quanta Computer Inc.
RS480M-VIDEO & CLKGEN
Size Custom
Document Number
Rev 3A
Date: Thursday, October 27, 2005
Sheet 7 of 37

CLG

NB RS480 POWER STATES

Power Signal	S0	S1	S3	S4/S5	G3
VDDHT	ON	ON	OFF	OFF	OFF
VDDR,VDDRCK	ON	ON	ON	ON	OFF
VDD18	ON	ON	OFF	OFF	OFF
VDDC	ON	ON	OFF	OFF	OFF
VDDA18	ON	ON	OFF	OFF	OFF
VDDA12	ON	ON	OFF	OFF	OFF
AVDD	ON	ON	OFF	OFF	OFF
AVDDDI	ON	ON	OFF	OFF	OFF
PLLVDD	ON	ON	OFF	OFF	OFF
HTPVDD	ON	ON	OFF	OFF	OFF
VDDR3	ON	ON	OFF	OFF	OFF
LPVDD	ON	ON	OFF	OFF	OFF
LVDDR18D	ON	ON	OFF	OFF	OFF
LVDDR18A	ON	ON	OFF	OFF	OFF

U28F
RS480M
PAR 6 OF 6
GROUND

U28E
PART 5 OF 6
POWER
RS480M

VDDA_1V2
VDDHT
VDDA12
VDDA18
+1.8V
VDD_MEM
VDD18
+3V
120 mils
20 mils

R85 FBMJ2125HM330-T
R63 FBMJ2125HM330-T
R66 TI201209G121
L4 TI201209G121

D9 BAV99
D8 BAV99

3.3V_2.7

PUT DECOUPLING CAPS ON THE TOP, CLOSE TO BALLS
CONNECT VSSA22,VSSA59,VSS30,VSS89 to the ground.

Notice the trace width.

PROJECT : MA3
Quanta Computer Inc.

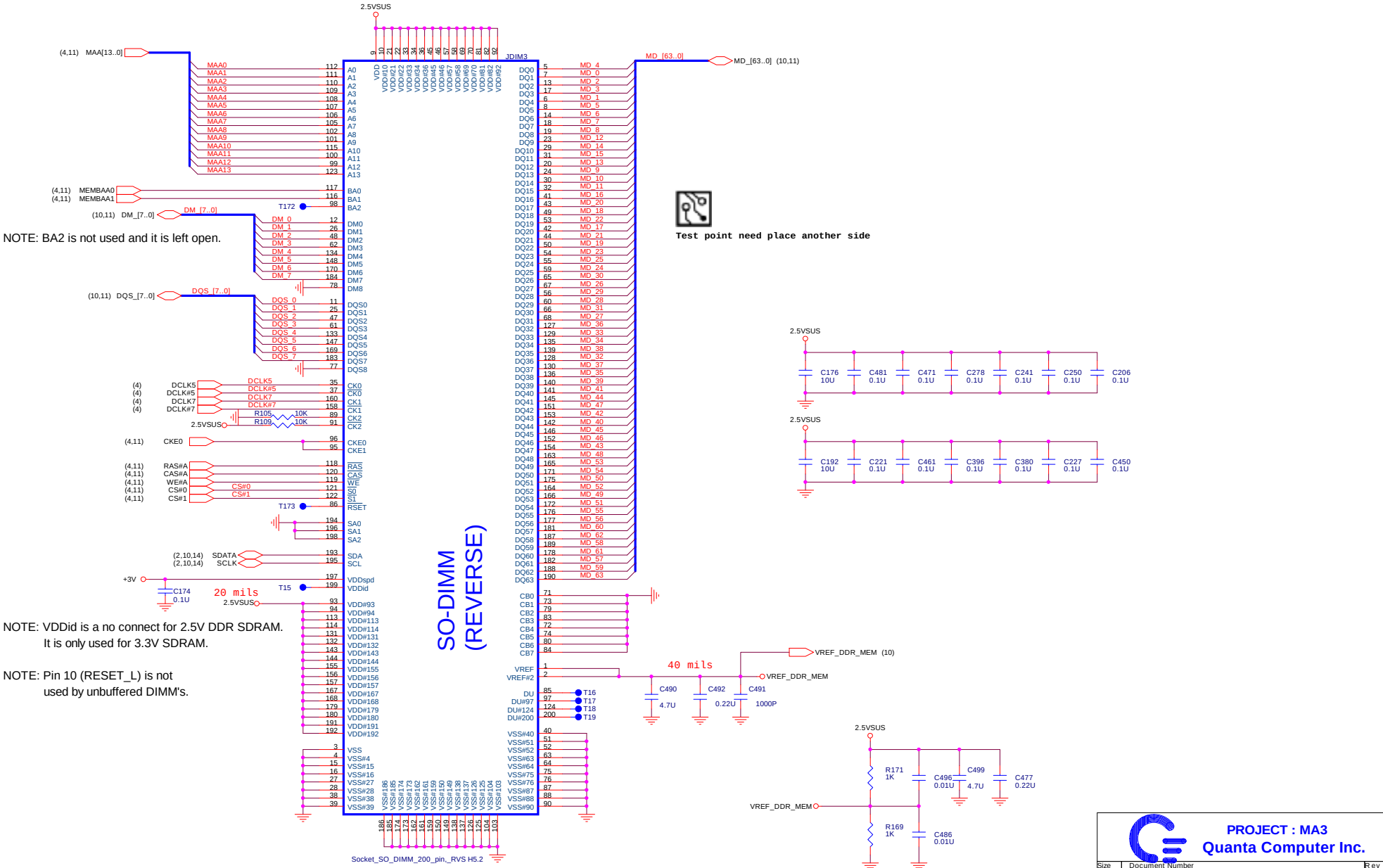
Size	Document Number	Rev
Custom	RS480M-POWER	1A

Date: Thursday, October 27, 2005 Sheet 8 of 37

Unbuffered DDR Near SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU

DDR



PROJECT : MA3
Quanta Computer Inc.

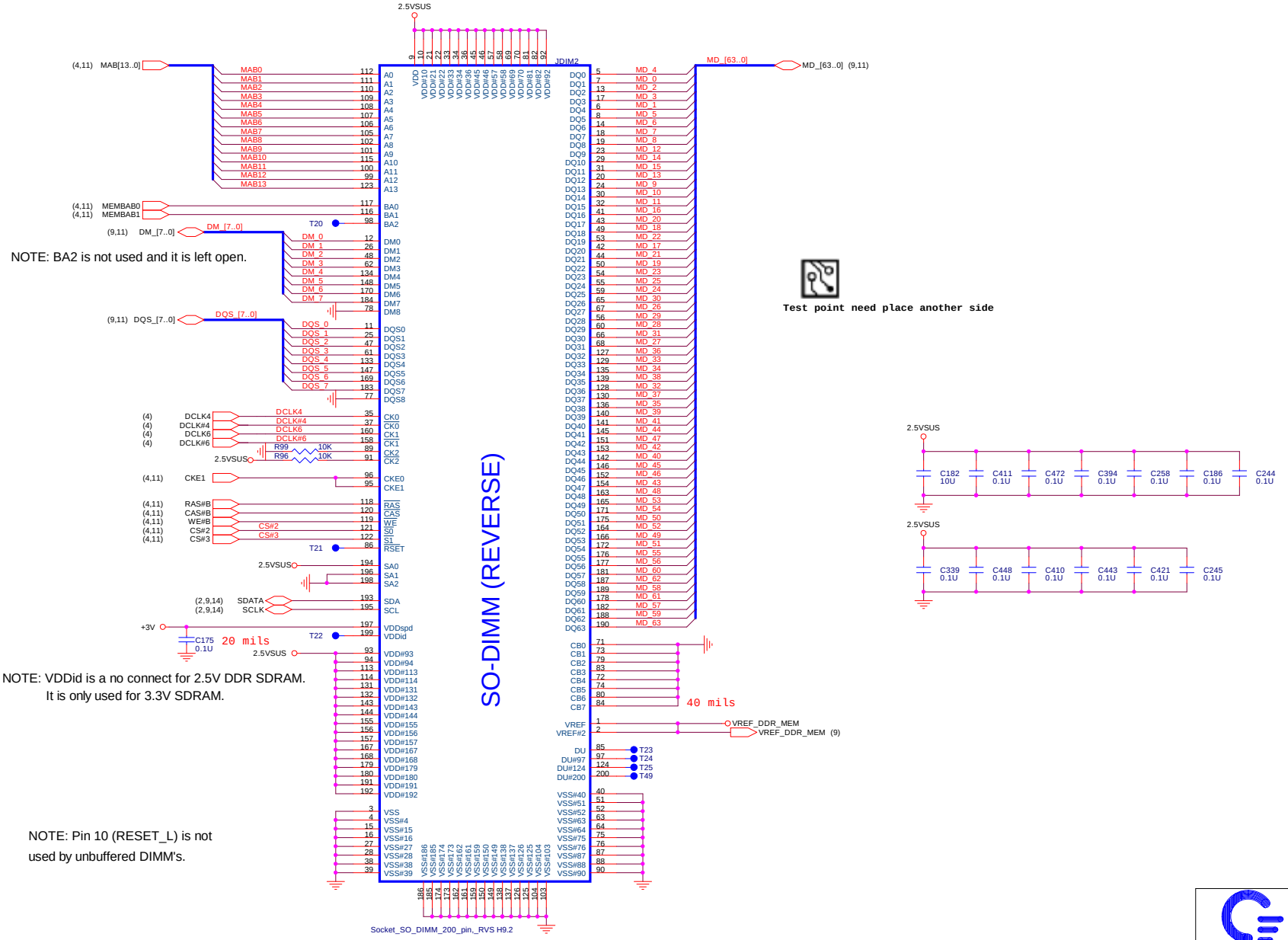
Size	Document Number	Rev
Custom	DDR NEAR SO-DIMM	1A

Date: Thursday, October 27, 2005 Sheet 9 of 37

Unbuffered DDR Far SODIMM Socket

ALLEGRO ROOM PROPERTY
AMD CPU

DDR



NOTE: BA2 is not used and it is left open.

NOTE: VDDid is a no connect for 2.5V DDR SDRAM.
It is only used for 3.3V SDRAM.

NOTE: Pin 10 (RESET_L) is not used by unbuffered DIMM's.

Test point need place another side

PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR FAR SO-DIMM	1A

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DDR

(4) MD[63..0] MD[63..0]
(4) DQS[7..0] DQS[7..0]
(4) DM[7..0] DM[7..0]

MD58 RN126 1 2 10X2 MD_58
MD62 3 4 MD_62
MD56 RN128 1 2 10X2 MD_56
MD60 3 4 MD_60
MD63 RN125 1 2 10X2 MD_63
MD59 3 4 MD_59
MD57 RN127 1 2 10X2 MD_57
MD61 3 4 MD_61
MD54 RN130 1 2 10X2 MD_54
MD50 3 4 MD_50
MD52 RN131 1 2 10X2 MD_52
MD49 3 4 MD_49
MD55 RN129 1 2 10X2 MD_55
MD51 3 4 MD_51
MD53 RN132 1 2 10X2 MD_53
MD48 3 4 MD_48
MD43 RN133 1 2 10X2 MD_43
MD46 3 4 MD_46
MD45 RN135 1 2 10X2 MD_45
MD40 3 4 MD_40
MD47 RN134 1 2 10X2 MD_47
MD42 3 4 MD_42
MD41 RN136 1 2 10X2 MD_41
MD44 3 4 MD_44
MD34 RN137 1 2 10X2 MD_34
MD38 3 4 MD_38
MD32 RN139 1 2 10X2 MD_32
MD37 3 4 MD_37
MD39 RN138 1 2 10X2 MD_39
MD35 3 4 MD_35
MD33 RN140 1 2 10X2 MD_33
MD36 3 4 MD_36
MD27 RN141 1 2 10X2 MD_27
MD31 3 4 MD_31
MD24 RN143 1 2 10X2 MD_24
MD25 3 4 MD_25
MD26 RN142 1 2 10X2 MD_26
MD30 3 4 MD_30
MD29 RN144 1 2 10X2 MD_29
MD28 3 4 MD_28
MD18 RN145 1 2 10X2 MD_18
MD22 3 4 MD_22
MD17 RN148 1 2 10X2 MD_17
MD21 3 4 MD_21
MD19 RN146 1 2 10X2 MD_19
MD23 3 4 MD_23
MD20 RN147 1 2 10X2 MD_20
MD16 3 4 MD_16
MD15 RN150 1 2 10X2 MD_15
MD14 3 4 MD_14
MD9 RN151 1 2 10X2 MD_9
MD13 3 4 MD_13
MD10 RN149 1 2 10X2 MD_10
MD11 3 4 MD_11
MD8 RN152 1 2 10X2 MD_8
MD12 3 4 MD_12
MD7 RN153 1 2 10X2 MD_7
MD6 3 4 MD_6
MD0 RN155 1 2 10X2 MD_0
MD4 3 4 MD_4
MD3 RN154 1 2 10X2 MD_3
MD2 3 4 MD_2
MD5 RN156 1 2 10X2 MD_5
MD1 3 4 MD_1

DQS0 R159 10 DQS_0
DQS1 R141 10 DQS_1
DQS2 R117 10 DQS_2
DQS3 R111 10 DQS_3
DQS4 R83 10 DQS_4
DQS5 R71 10 DQS_5
DQS6 R60 10 DQS_6
DQS7 R58 10 DQS_7

DM0 R162 10 DM_0
DM1 R153 10 DM_1
DM2 R119 10 DM_2
DM3 R113 10 DM_3
DM4 R84 10 DM_4
DM5 R74 10 DM_5
DM6 R65 10 DM_6
DM7 R57 10 DM_7

(9,10) MD_[63..0] MD_[63..0]

MD_2 RN85 1 2 68X4
MD_7 3 4
MD_6 5 6
MD_3 7 8
MD_4 RN84 1 2 68X4
MD_0 3 4
MD_5 5 6
MD_1 7 8
MD_14 RN82 1 2 68X4
MD_15 3 4
MD_10 5 6
MD_11 7 8
MD_8 RN81 1 2 68X4
MD_12 3 4
MD_13 5 6
MD_9 7 8
MD_18 RN79 1 2 68X4
MD_22 3 4
MD_19 5 6
MD_23 7 8
MD_16 RN78 1 2 68X4
MD_20 3 4
MD_17 5 6
MD_21 7 8
MD_26 RN76 1 2 68X4
MD_30 3 4
MD_31 5 6
MD_27 7 8
MD_25 RN75 1 2 68X4
MD_24 3 4
MD_29 5 6
MD_28 7 8
MD_34 RN63 1 2 68X4
MD_38 3 4
MD_35 5 6
MD_39 7 8
MD_36 RN61 1 2 68X4
MD_33 3 4
MD_32 5 6
MD_37 7 8
MD_47 RN60 1 2 68X4
MD_42 3 4
MD_46 5 6
MD_43 7 8
MD_41 RN59 1 2 68X4
MD_44 3 4
MD_40 5 6
MD_45 7 8
MD_54 RN57 1 2 68X4
MD_50 3 4
MD_51 5 6
MD_55 7 8
MD_48 RN56 1 2 68X4
MD_53 3 4
MD_52 5 6
MD_49 7 8
MD_63 RN53 1 2 68X4
MD_62 3 4
MD_58 5 6
MD_59 7 8
MD_56 RN54 1 2 68X4
MD_60 3 4
MD_61 5 6
MD_57 7 8

DM_7 RN52 1 2 68X2
DQS_7 3 4
DM_5 RN58 1 2 68X2
DQS_5 3 4
DM_3 RN74 1 2 68X2
DQS_3 3 4
DM_1 RN80 1 2 68X2
DQS_1 3 4
DM_6 RN55 1 2 68X2
DQS_6 3 4
DM_4 RN62 1 2 68X2
DQS_4 3 4
DM_2 RN77 1 2 68X2
DQS_2 3 4
DM_0 RN83 1 2 68X2
DQS_0 3 4

(9,10) DQS_[7..0] DQS_[7..0]
(9,10) DM_[7..0] DM_[7..0]

VTT_DDR (4,31,35) VTT_DDR

(4,9) MAA[13..0]
MAA4 RN68 1 2 47X4
MAA8 3 4
MAA2 5 6
MAA0 7 8
MAA3 RN71 1 2 47X4
MAA5 3 4
MAA1 5 6
MAA10 7 8
MAA7 RN73 1 2 47X4
MAA9 3 4
MAA11 5 6
MAA6 7 8
MAA12 R98 47
MAA13

(4,9) CKE0 R101 47
(4,10) CKE1 R106 47

(4,9) MEMBAA0
(4,9) WE#A MAA13
(4,9) CS#0 CS#0
RN65 1 2 47X4 3 4 5 6 7 8

(4,9) CS#1 CS#1
(4,9) RAS#A
(4,9) MEMBAA1
(4,9) CAS#A
RN64 1 2 47X4 3 4 5 6 7 8

(4,10) MAB[13..0]
MAB2 RN70 1 2 47X4
MAB4 3 4
MAB5 5 6
MAB6 7 8
MAB3 RN69 1 2 47X4
MAB1 3 4
MAB10 5 6
7 8

(4,10) RAS#B
MAB8 RN72 1 2 47X4
MAB9 3 4
MAB7 5 6
MAB11 7 8
MAB12 R103 47

RN66 1 2 47X4 3 4 5 6 7 8
(4,10) MEMBAB0
(4,10) WE#B
(4,10) CS#2 CS#2
MAB13

RN67 1 2 47X4 3 4 5 6 7 8
(4,10) CS#3 CS#3
(4,10) CAS#B
(4,10) MEMBAB1
MAB0

Place on each end of the VTT island.
VTT_DDR
C522 10U C523 10U

LAYOUT: Locate close to Clawhammer socket.
VTT_DDR 2.5VSUS
C508 150U
C432 150U/6.3V C498 *150U/6.3V C474 4.7U C301 0.22U

LAYOUT: Place on VTT fill near Clawhammer and near DIMMs
VTT_DDR
C213 1000P C351 100P C290 100P C332 1000P C349 1000P C300 100P C151 100P C145 1000P

LAYOUT: Place a cap every 1 in. on VTT traces between Clawhammer and DDR.
VTT_DDR
C150 0.22U C140 4.7U C480 0.22U C515 4.7U C387 0.22U C139 4.7U C161 0.22U C328 4.7U C307 0.22U C416 4.7U C156 0.22U C516 4.7U C173 0.22U C528 4.7U C160 0.22U C521 4.7U C525 0.22U C527 4.7U

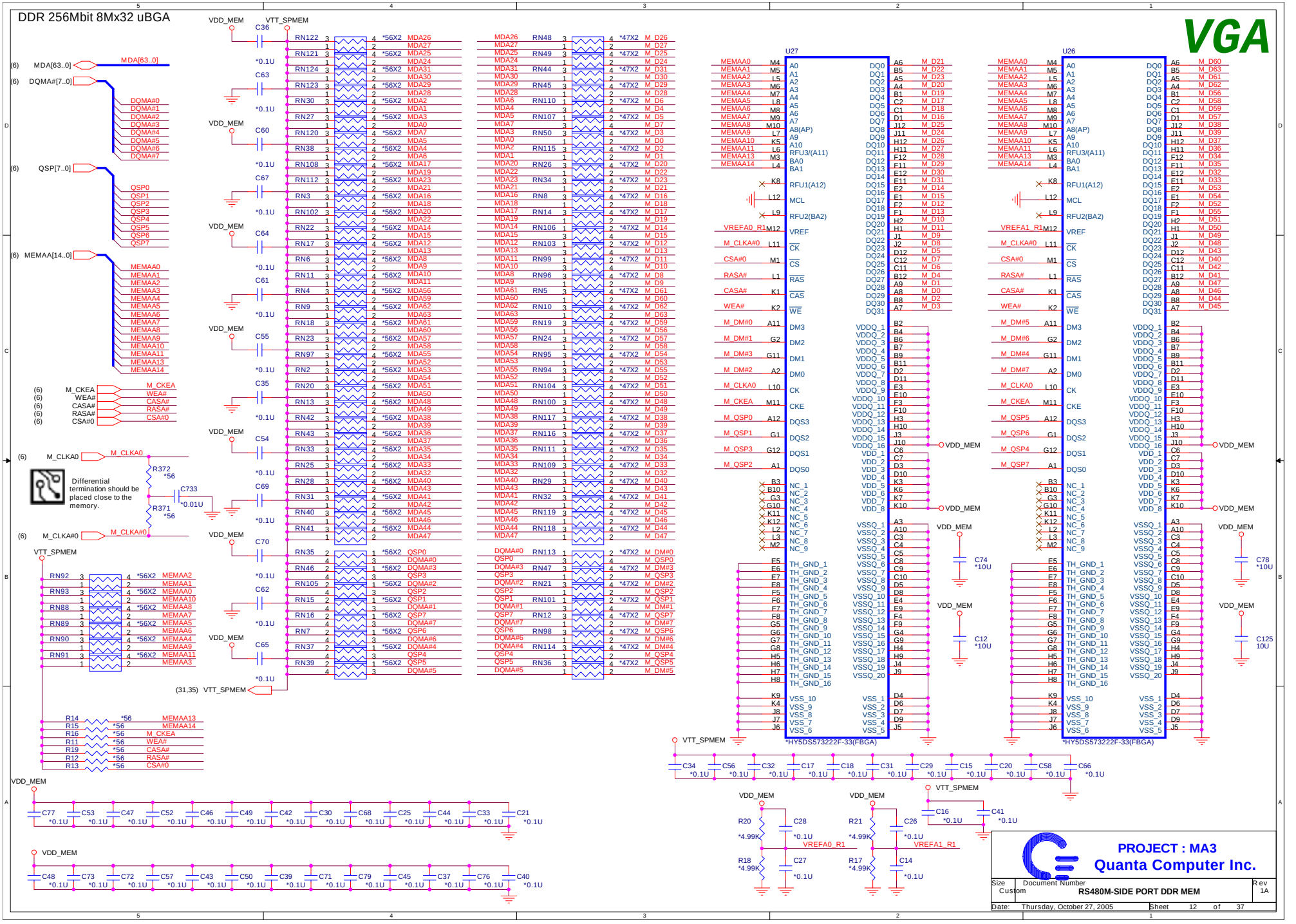
LAYOUT: Place alternating caps to GND and VDD_2.5_SUS in a single line along VTT_DDR_SUS island.
VTT_DDR
C256 C219 C404 C409 C370 C364 C321 C153 C147 C365 C283 C374 C306 C393 C489 C204 C407 C148 C144 C277 C453 C430 C238 C446 C157 C350 C344 C314 C417 C379 C384 C397 C413 C154
all 0.1U

VTT_DDR 2.5VSUS
C524 C482 C249 C193 C223 C773 C146 C422 C509 C414 C360 C149 C170 C772 C143 C158 C771 C373 C155 C425 C447 C280 C313 C451 C470 C372 C398 C473 C159 C152 C493 C529 C395
all 0.1U

PROJECT : MA3
Quanta Computer Inc.
Size: Custom | Document Number: DDR SO-DIMM TERMINATION | Rev: 1A
Date: Thursday, October 27, 2005 | Sheet 11 of 37

DDR 256Mbit 8Mx32 uBGA

VGA



CLG

PLACE THESE CAPS CLOSE TO THE CONNECTOR

PLACE THESE COMPONENTSCLOSE TO U600, AND USE GROUND GUILD FOR 32K_X1 AND 32K_X2

C610 AND C611 CLOSE THE BALL R30 OF U600

LENGTH OF (PCI_CLK9_R + PCI_CLK9_FB) SHOULD BE AS SHORT AS POSSIBLE

C755 Placement closed to SB

RTC

EC-A02

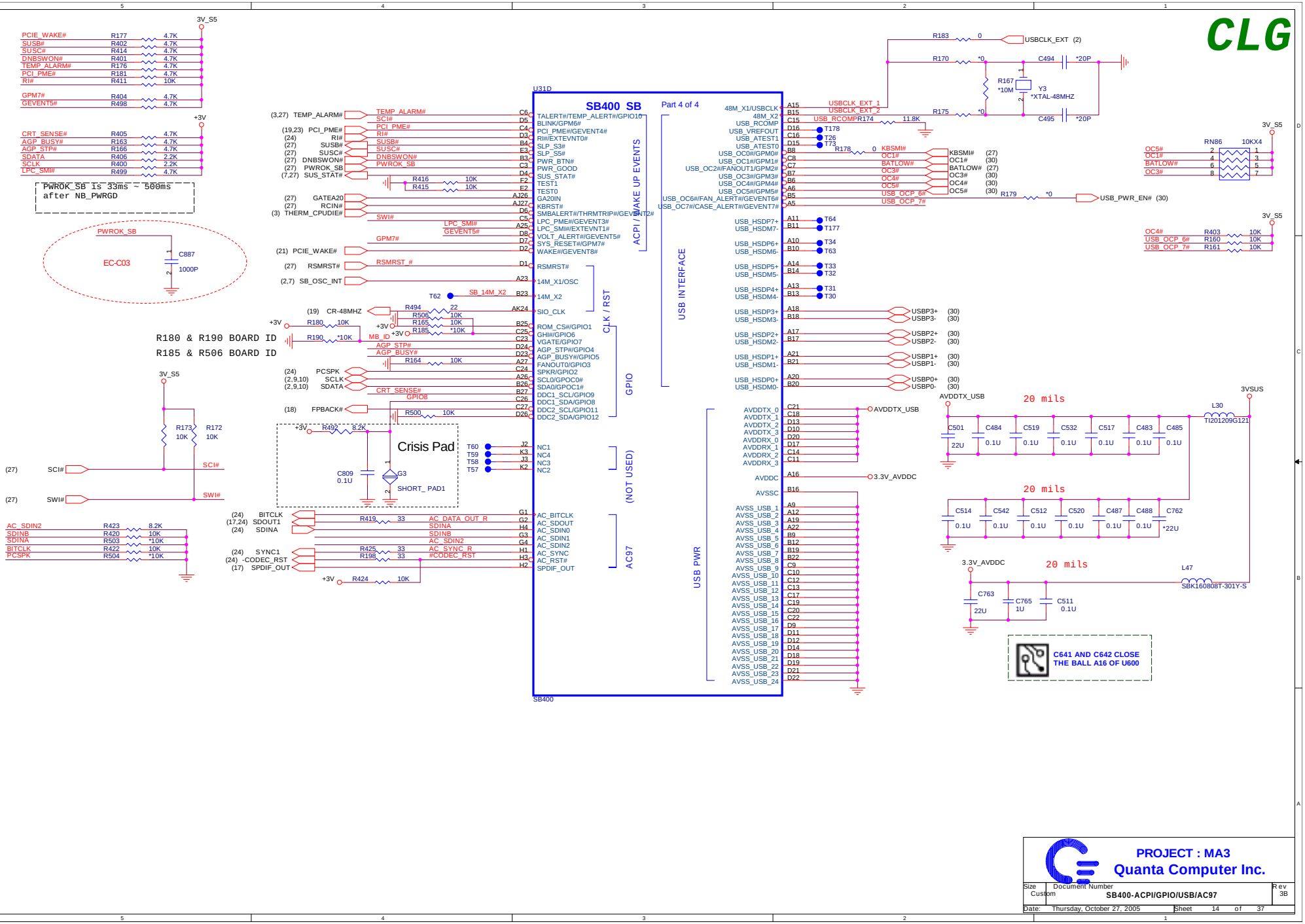
EC-B04

EC-B05

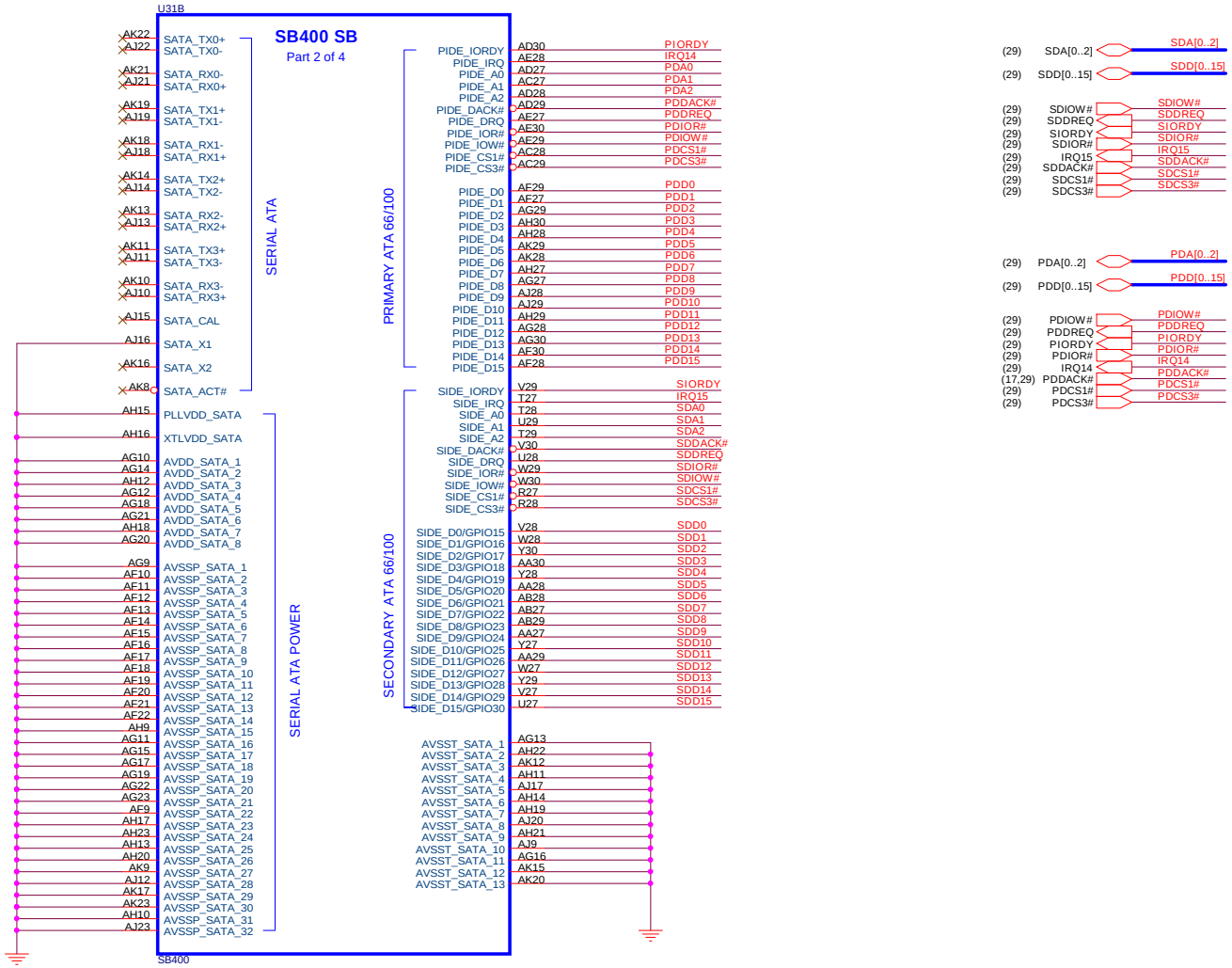
EC-B06

EC-B07

PROJECT : MA3	Quanta Computer Inc.
Size: C	Document Number: SB400-PCIE/PCI/CPU/LPC
Rev: 3A	
Date: Thursday, October 27, 2005	Sheet 13 of 37


CLG
SB400 SB
Part 4 of 4
U31D
SB400
PWROK_SB is 33ms ~ 500ms after NB_PWRGD
EC-C03
R180 & R190 BOARD ID
R185 & R506 BOARD ID
Crisis Pad
SHORT_ PAD1
ACPI / WAKE UP EVENTS
CLK / RST
GPIO
(NOT USED)
AC97
USB INTERFACE
USB PWR
USBCLK_EXT (2)
USB_PWR_EN# (30)
AVDDTX_USB
3.3V_AVDDC
3VSUS
20 mils
C641 AND C642 CLOSE THE BALL A16 OF U600
PROJECT : MA3
Quanta Computer Inc.
SB400-ACPI/GPIO/USB/AC97
Rev 3B
Thursday, October 27, 2005
Sheet 14 of 37

CLG

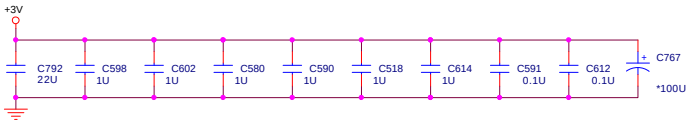


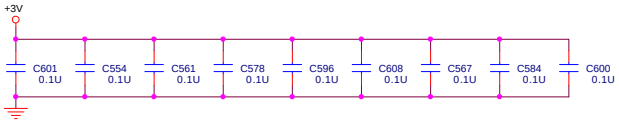
PROJECT : MA3
Quanta Computer Inc.

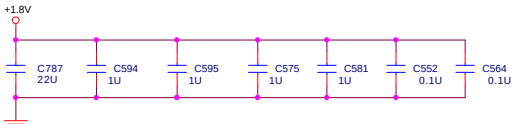
Size	Document Number	Rev
Custom	SB400-SATA/IDE	1A
Date: Thursday, October 27, 2005	Sheet 15 of 37	

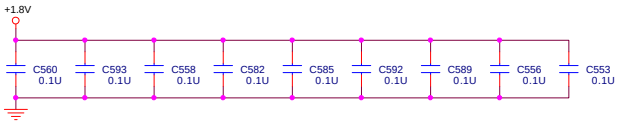
CLG

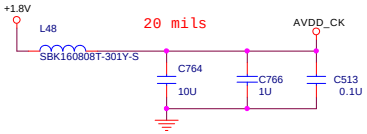
PLACE ALL THE DECOUPLING CAPS ON THIS SHEET CLOSE TO SB AS POSSIBLE.

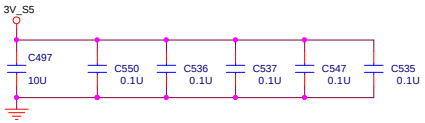


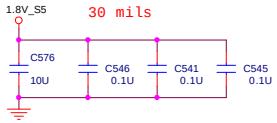


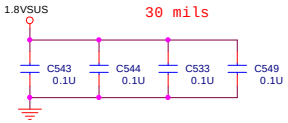


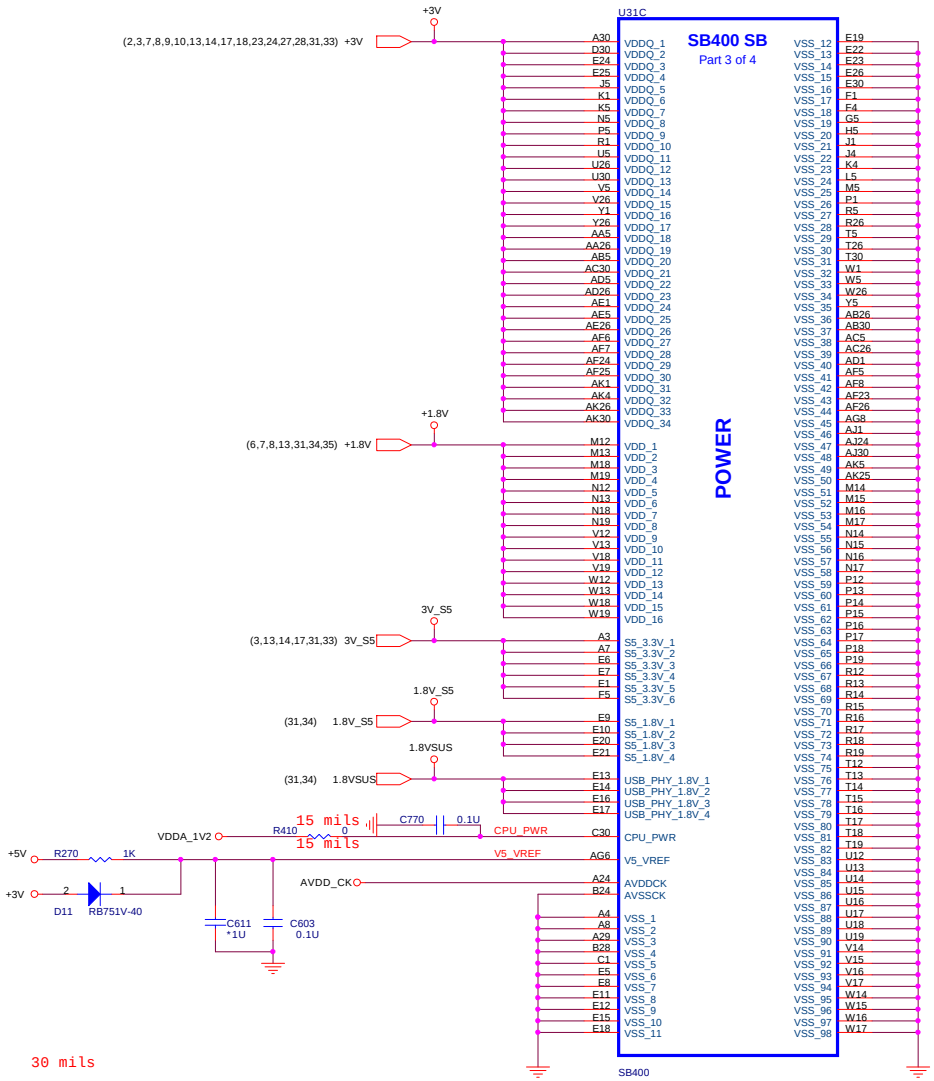












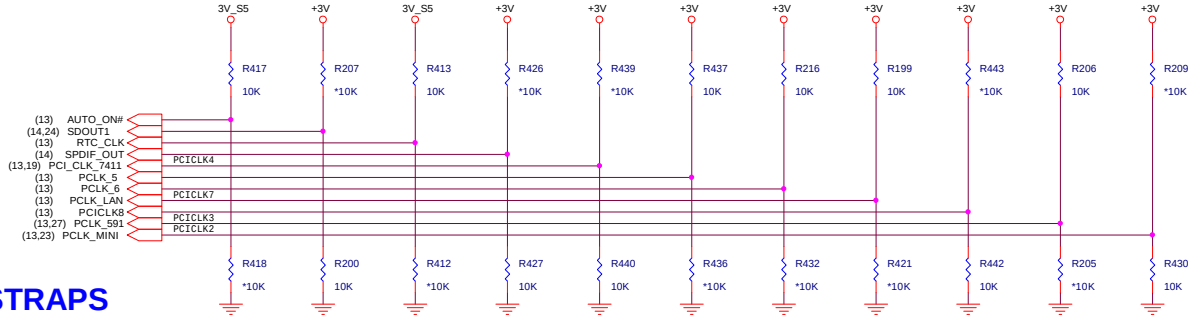
PROJECT : MA3

Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-POWER & DECOUPLING	1A

Date: Thursday, October 27, 2005 Sheet 16 of 37

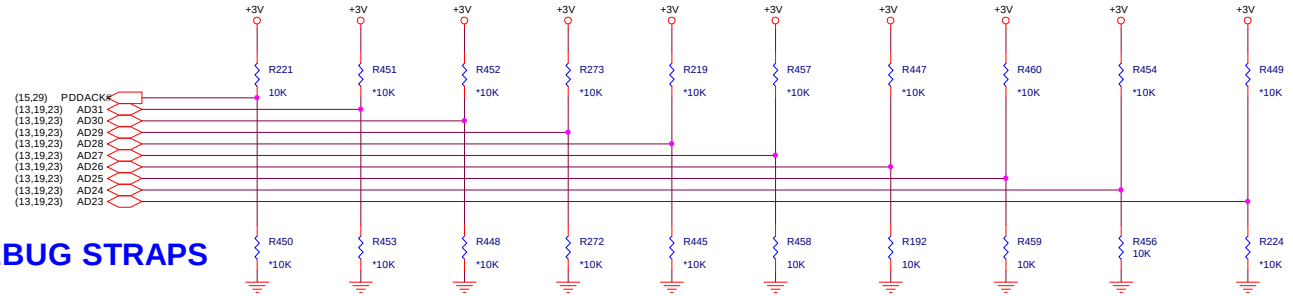
CLG



REQUIRED STRAPS

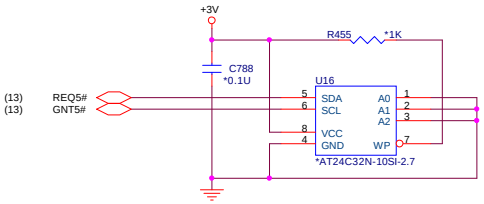
OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

	ACPWRON	AC_SDOUT	RTC_CLK	SPDIF_OUT	PCI_CLK_7411	PCLK_5	PCLK_6	PCLK_LAN	PCI_CLK8	PCLK_591	PCLK_MINI
					PCI_CLK4	PCI_CLK5	PCI_CLK6	PCI_CLK7	PCI_CLK8	PCI_CLK3	PCI_CLK2
PULL HIGH	MANUAL PWR ON DEFAULT	USE DEBUG STRAPS	INTERNAL RTC DEFAULT	SIO 24MHz	Internal USB PLL	14MHz OSC MODE DEFAULT	CPU I/F = K8 DEFAULT	ROM TYPE H,H = PCI ROM H,L = PMC LPC ROM		USB PHY PWRDOWN DISABLE DEFAULT	48MHz XTAL MODE
PULL LOW	AUTO PWR ON	IGNORE DEBUG STRAPS DEFAULT	EXTERNAL RTC (NOT SUPPORTED W/ IT8712)	SIO 48MHz DEFAULT	External USB 48MHz DEFAULT	48MHz XTAL MODE	CPU I/F = P4	L,H = NORMAL LPC ROM DEFAULT L,L = FWH ROM		USB PHY PWRDOWN ENABLE	48MHz OSC MODE



DEBUG STRAPS

	PDACK#	PCI_AD31	PCI_AD30	PCI_AD29	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE SHORT RESET	Reserved	Reserved	Reserved	Reserved	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved
PULL LOW	USE LONG RESET DEFAULT					USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	



SB PCIE EEPROM STRAPS

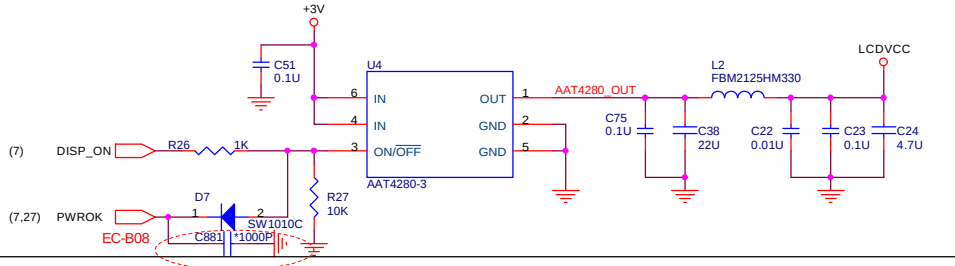
PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SB400-STRAPS	1A

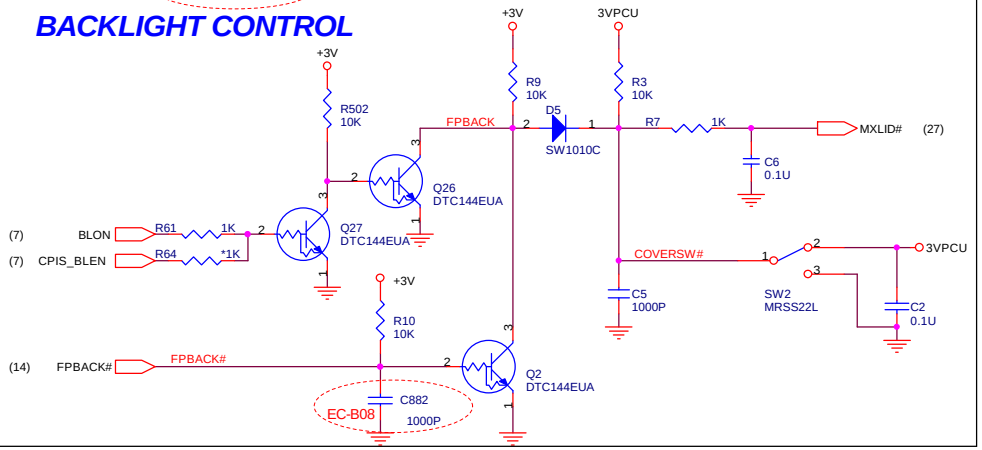
Date: Thursday, October 27, 2005 Sheet 17 of 37

VGA

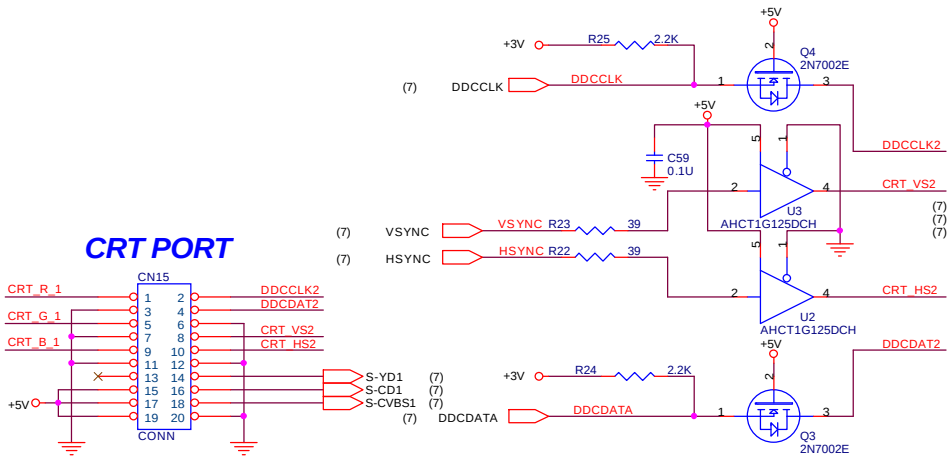
PANEL VCC CONTROL



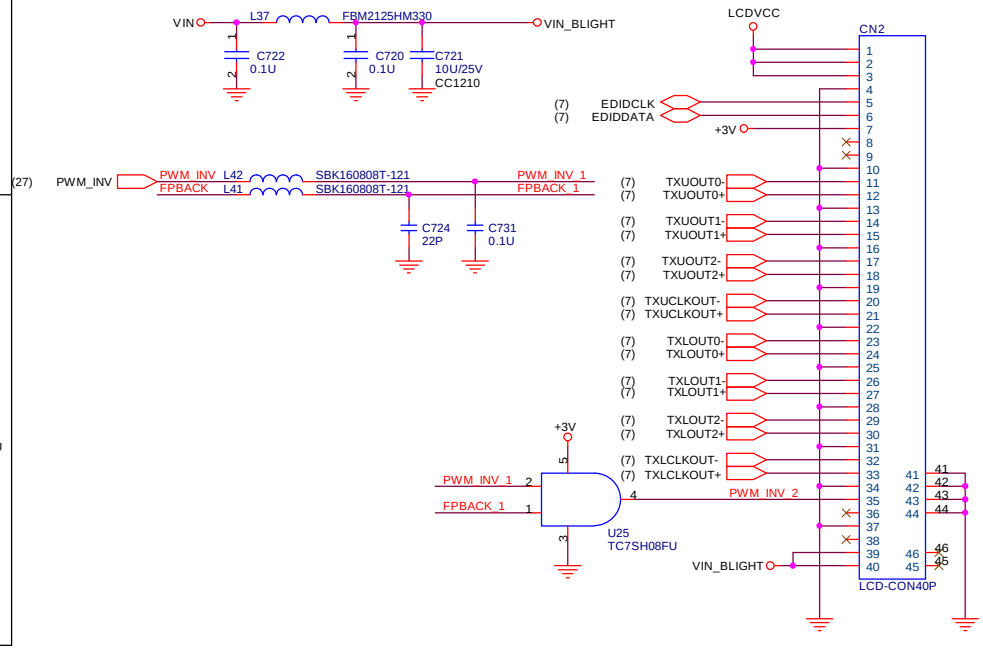
BACKLIGHT CONTROL

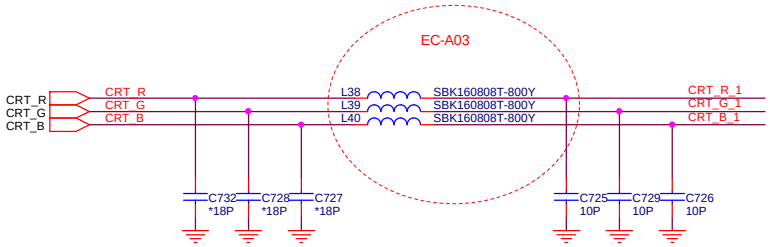


CRT PORT



LCD CONNECTOR





PROJECT : MA3

Quanta Computer Inc.

Size	Document Number	Rev
B	LCD LVDS & CRT CON	3A

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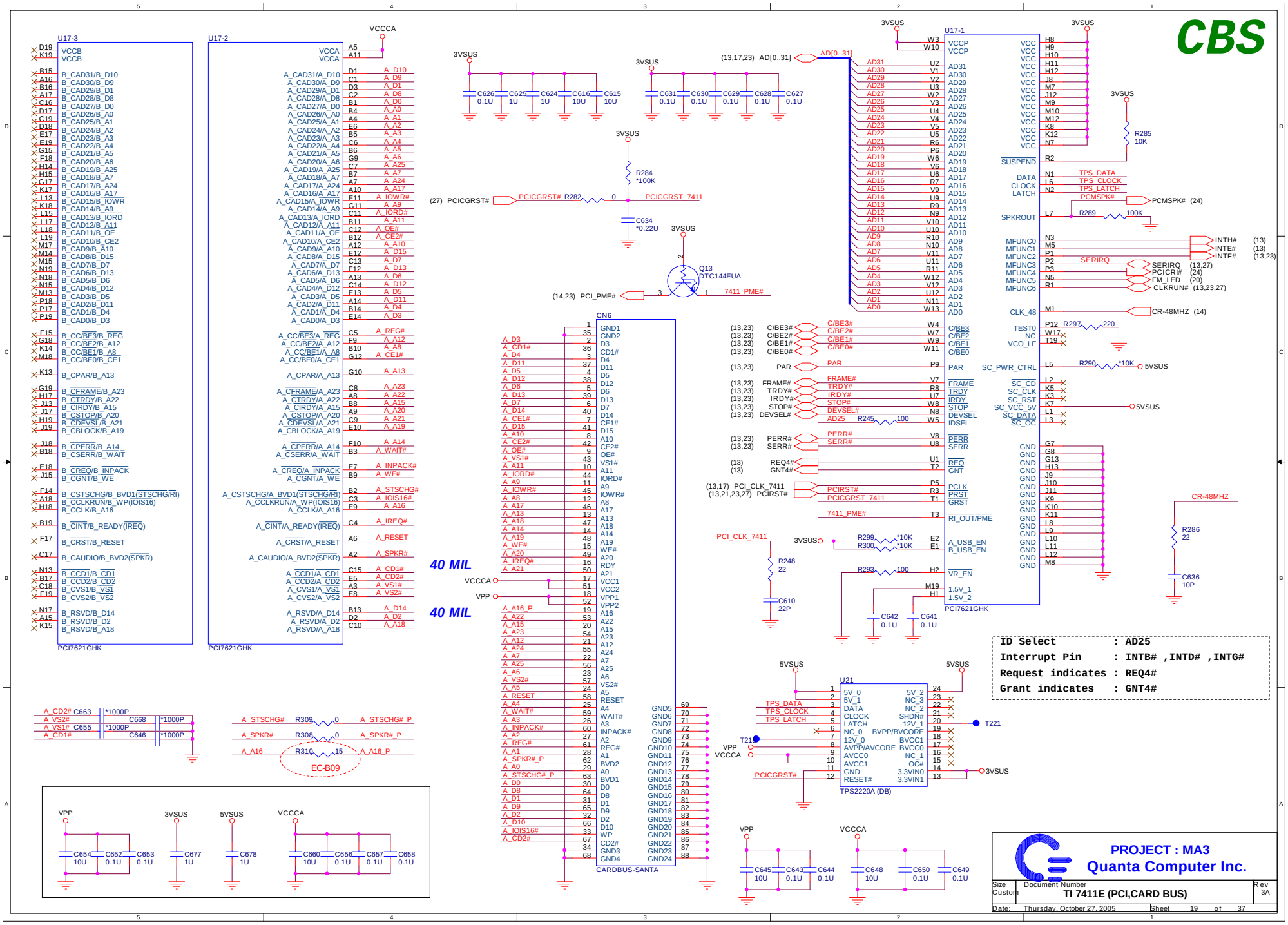
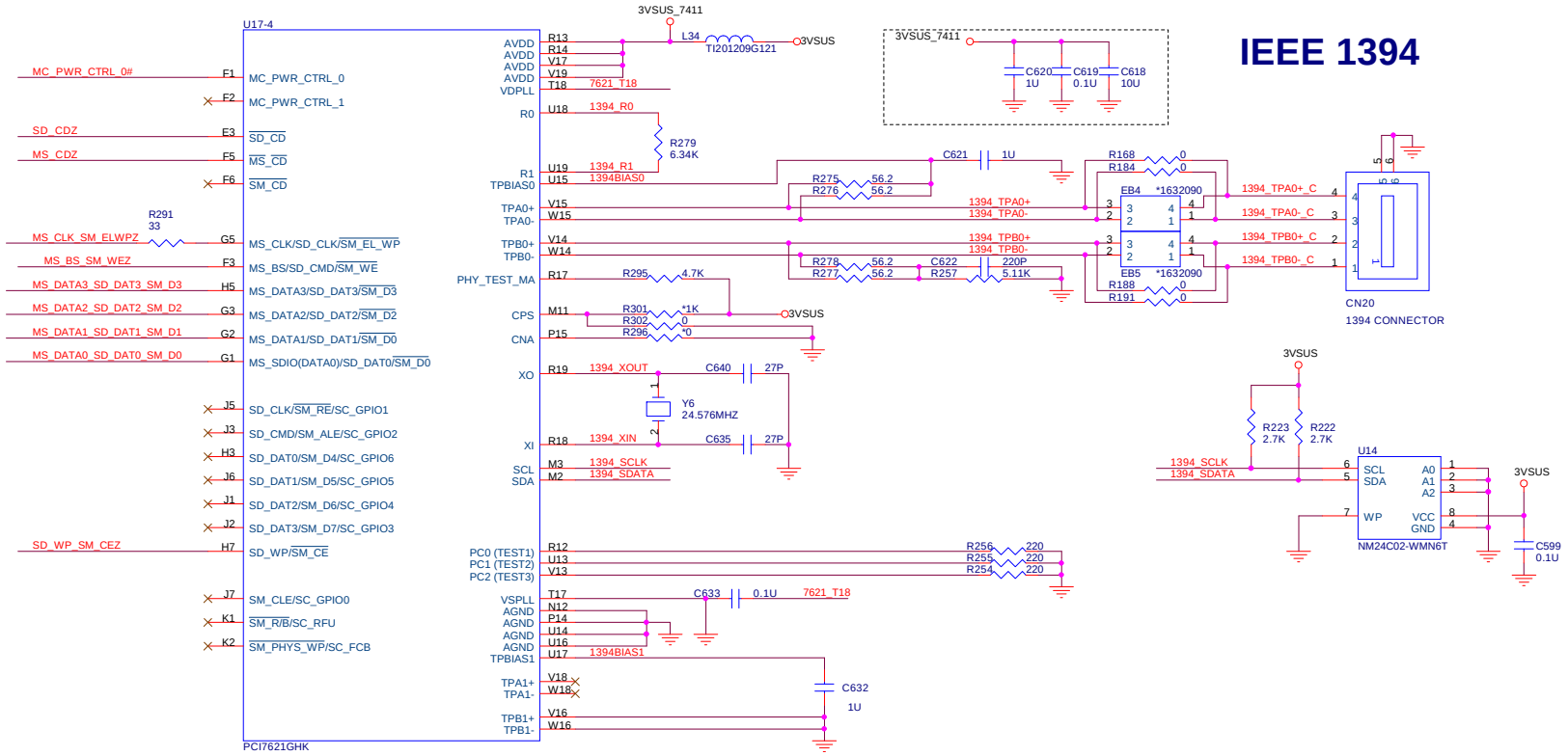

CBS
U17-3
U17-2
U17-1
PCI7621GHK
CN6
CARDBUS-SANTA
U21
TPS2220A (DB)
40 MIL
40 MIL
EC-B09
ID Select : AD25
Interrupt Pin : INTB# ,INTD# ,INTG#
Request indicates : REQ4#
Grant indicates : GNT4#
PROJECT : MA3
Quanta Computer Inc.
TI 7411E (PCI,CARD BUS)
Size Custom
Document Number
Rev 3A
Date: Thursday, October 27, 2005
Sheet 19 of 37

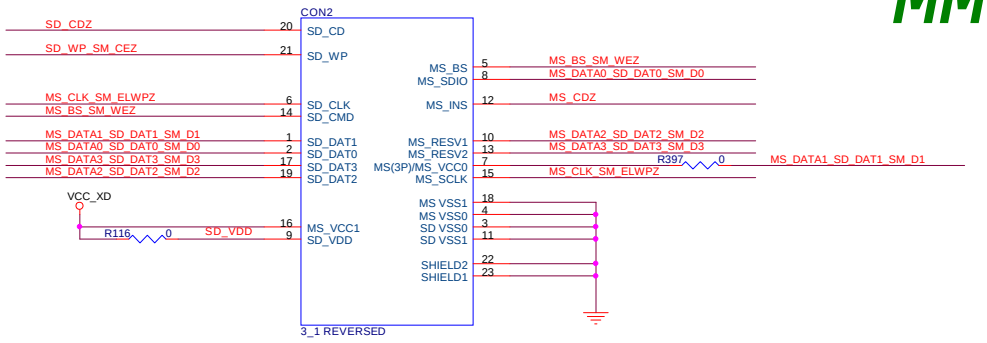
FIW

IEEE 1394

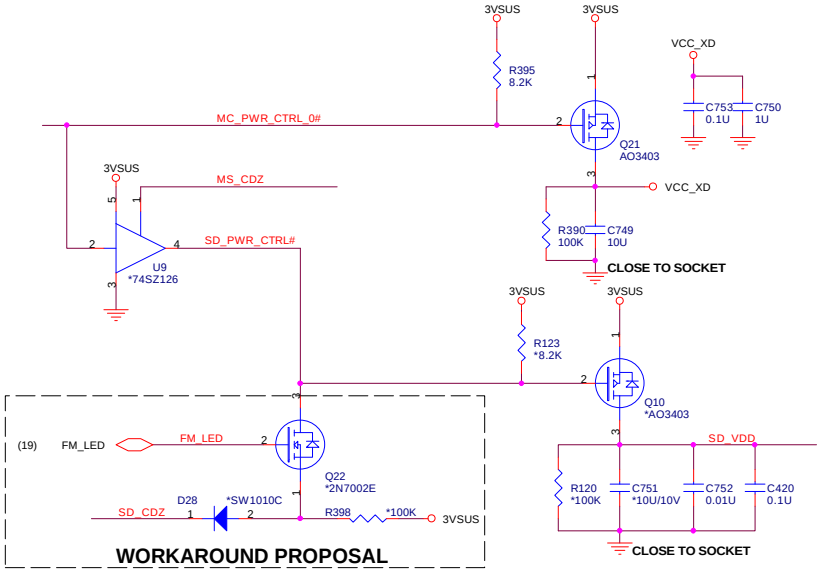


MMC

4 IN1 CARD READER



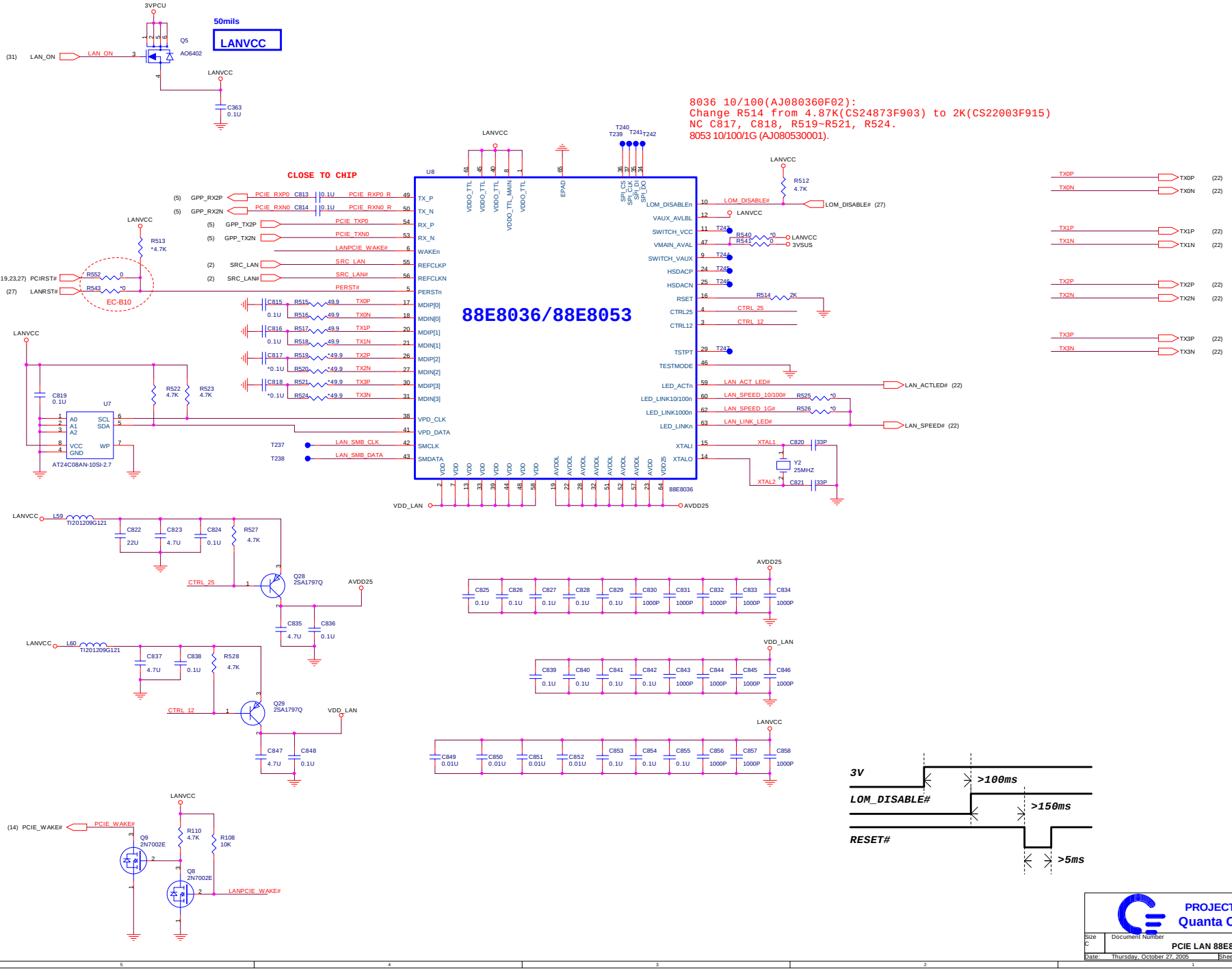
Supporting MMC/SD/MS/MS Pro Cards



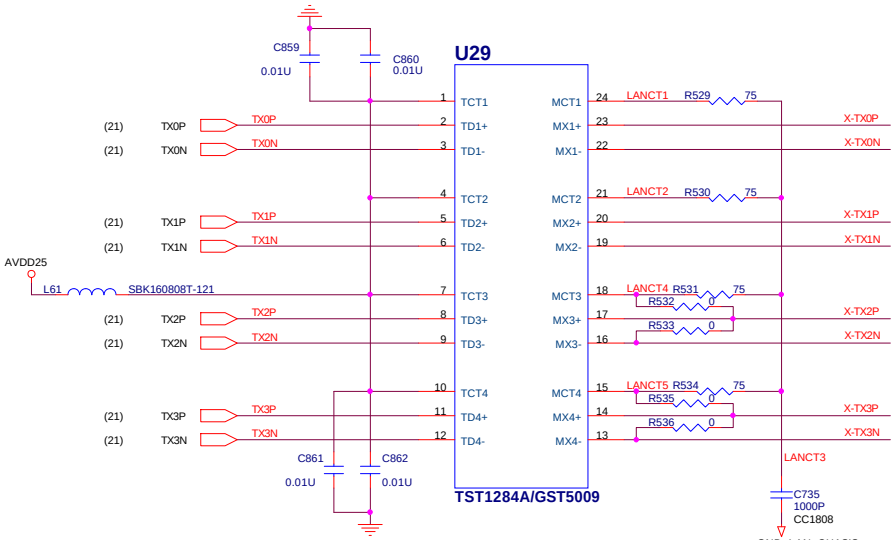
PROJECT : MA3
Quanta Computer Inc.

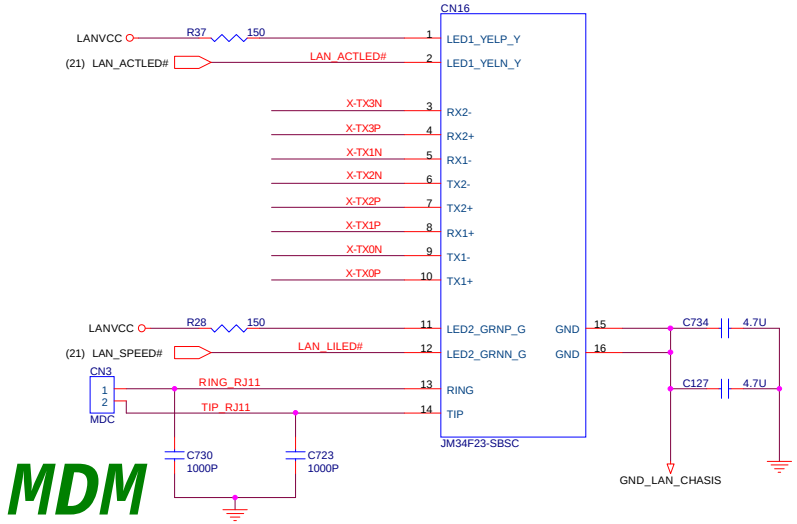
Size	Document Number	Rev
Custom	TI 7411E (1394 & CARD_READER)	1A
Date: Thursday, October 27, 2005	Sheet 20 of 37	

LAN

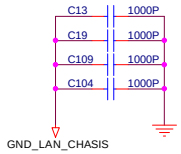

50mils
LANVCC
3VPCU
Q5
AO6402
(31) LAN_ON
C363 0.1U
8036 10/100(AJ080360F02):
Change R514 from 4.87K(CS24873F903) to 2K(CS22003F915)
NC C817, C818, R519~R521, R524.
8053 10/100/1G (AJ080530001).
CLOSE TO CHIP
U8
88E8036/88E8053
EC-B10
R513 *4.7K
R552 0
R543 *0
(13,19,23,27) PCIRST#
(27) LANRST#
PCIE_RXP0_C813 0.1U PCIE_RXP0_R
PCIE_RXN0_C814 0.1U PCIE_RXN0_R
PCIE_TXP0
PCIE_TXN0
LANPCIE_WAKE#
SRC_LAN
SRC_LAN#
PERST#
R512 4.7K
LOM_DISABLE#
R540 *0
R541 0
3VSUS
R514 2K
CTRL_25
CTRL_12
LAN_ACT_LED#
LAN_SPEED_10/100#
LAN_SPEED_1G#
LAN_LINK_LED#
R525 *0
R526 *0
LAN_ACTLED# (22)
LAN_SPEED# (22)
C820 33P
C821 33P
Y2 25MHZ
AT24C08AN-10SI-2.7
U7
R522 4.7K
R523 4.7K
C819 0.1U
LAN_SMB_CLK
LAN_SMB_DATA
VDD_LAN
AVDD25
L59 TI201209G121
L60 TI201209G121
C822 22U
C823 4.7U
C824 0.1U
R527 4.7K
Q28 2SA1797Q
C835 4.7U
C836 0.1U
C837 4.7U
C838 0.1U
R528 4.7K
Q29 2SA1797Q
C847 4.7U
C848 0.1U
C825 0.1U
C826 0.1U
C827 0.1U
C828 0.1U
C829 0.1U
C830 1000P
C831 1000P
C832 1000P
C833 1000P
C834 1000P
C839 0.1U
C840 0.1U
C841 0.1U
C842 0.1U
C843 1000P
C844 1000P
C845 1000P
C846 1000P
C849 0.01U
C850 0.01U
C851 0.01U
C852 0.01U
C853 0.1U
C854 0.1U
C855 0.1U
C856 1000P
C857 1000P
C858 1000P
(14) PCIE_WAKE#
Q9 2N7002E
Q8 2N7002E
R110 4.7K
R108 10K
TX0P (22)
TX0N (22)
TX1P (22)
TX1N (22)
TX2P (22)
TX2N (22)
TX3P (22)
TX3N (22)
3V
>100ms
LOM_DISABLE#
>150ms
RESET#
>5ms
PROJECT : MA3
Quanta Computer Inc.
PCIE LAN 88E8036/88E8053
Size C
Rev 3A
Date: Thursday, October 27, 2005
Sheet 21 of 37

LAN





MDM



PROJECT : MA3
Quanta Computer Inc.

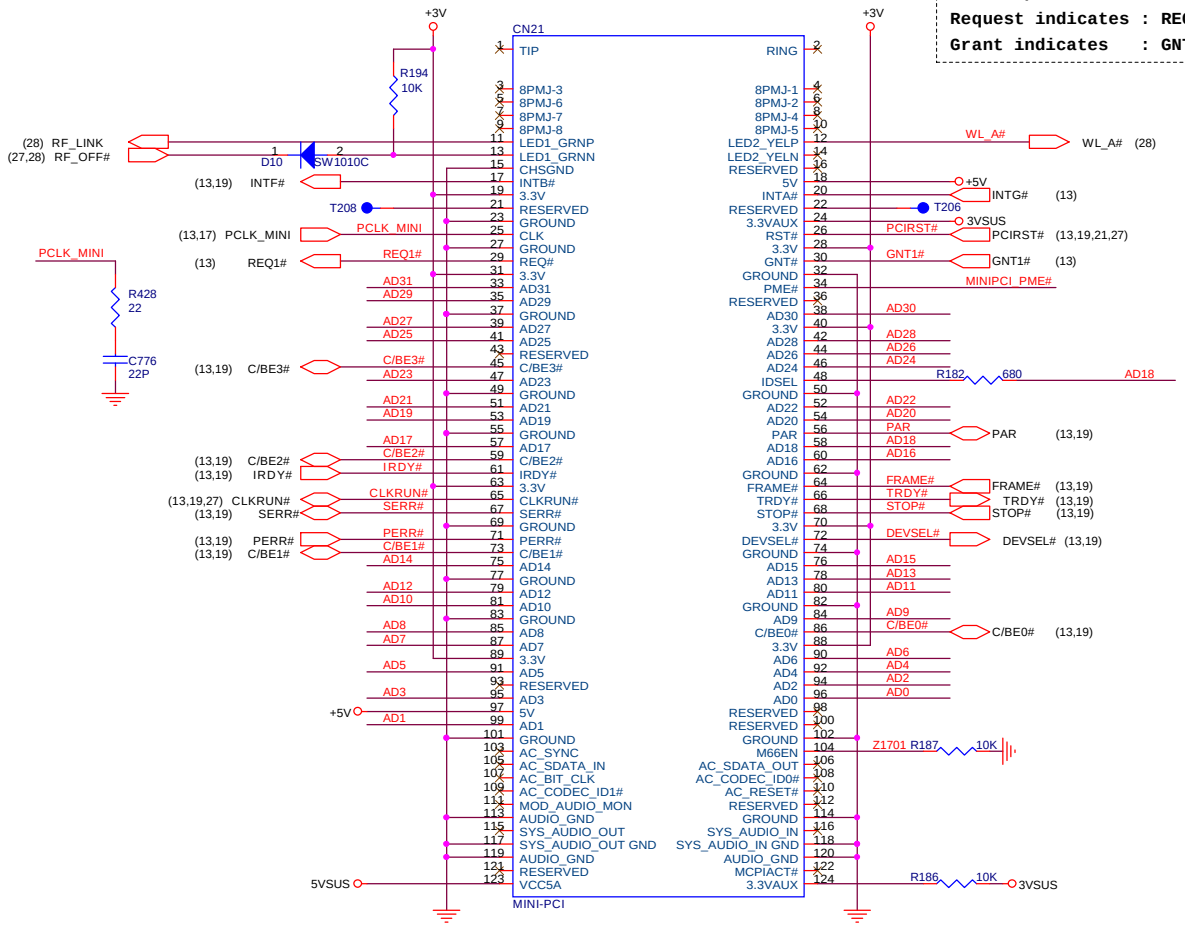
Size	Document Number	Rev
Custom	LAN, RJ11, RJ45	1A
Date: Thursday, October 27, 2005	Sheet 22 of 37	

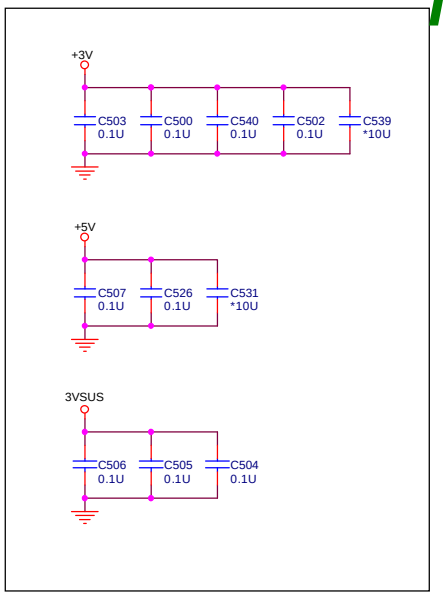
MPC

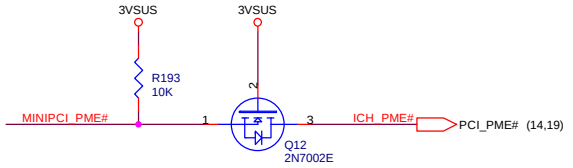
TYPE III MINI PCI SOCKET

AD[0..31] — AD[0..31] (13,17,19)

ID Select	:	AD18
Interrupt Pin	:	INTG# , INTF#
Request indicates	:	REQ1#
Grant indicates	:	GNT1#







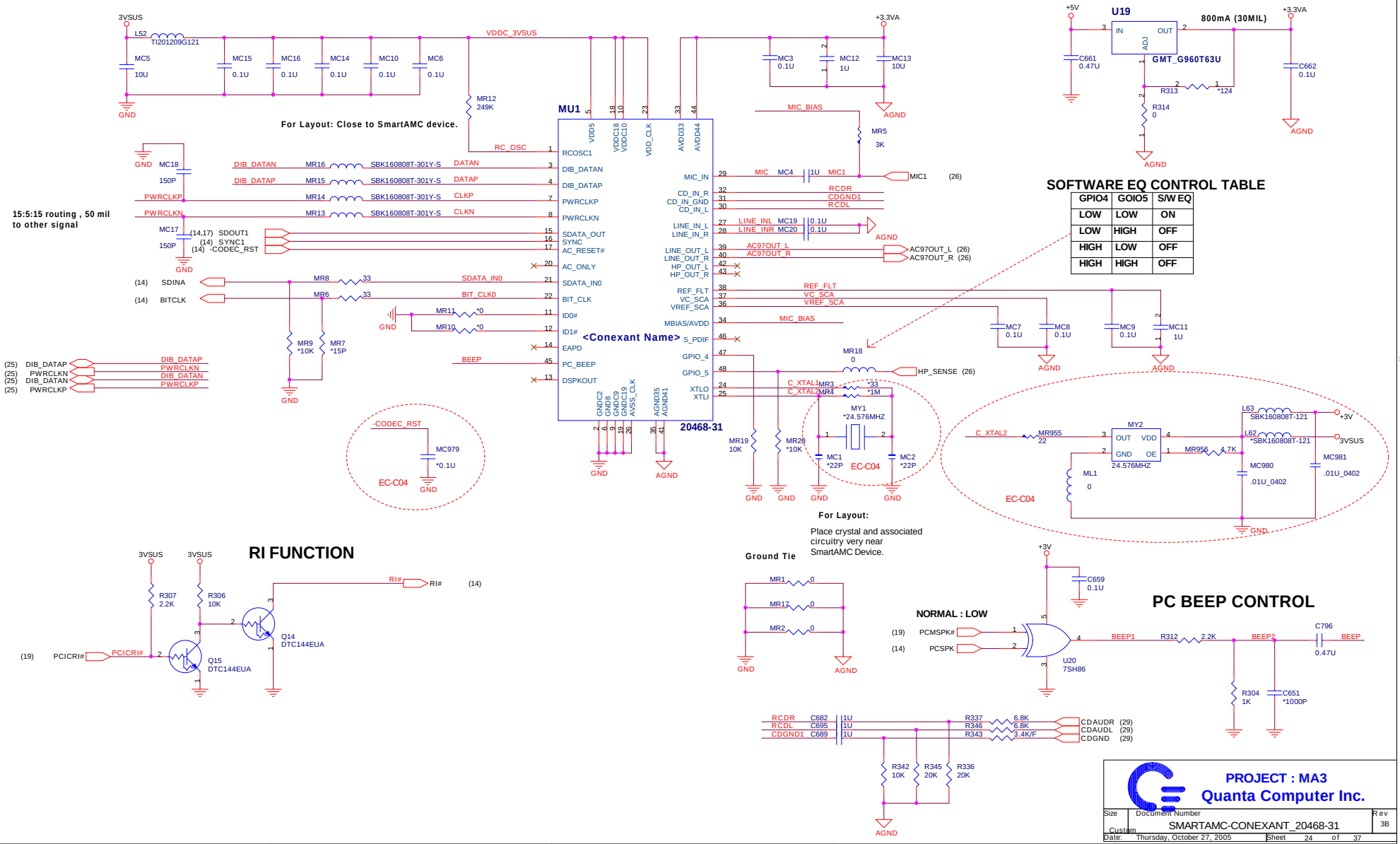
PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
B	MINI PCI Socket & MDC	1A
Date: Thursday, October 27, 2005	Sheet 23 of 37	

SMARTAMC-CONEXANT_20468-31

ADO

For Layout:
Place decoupling caps near the power pins of SmartAMC device.



PROJECT : MA3
Quanta Computer Inc.

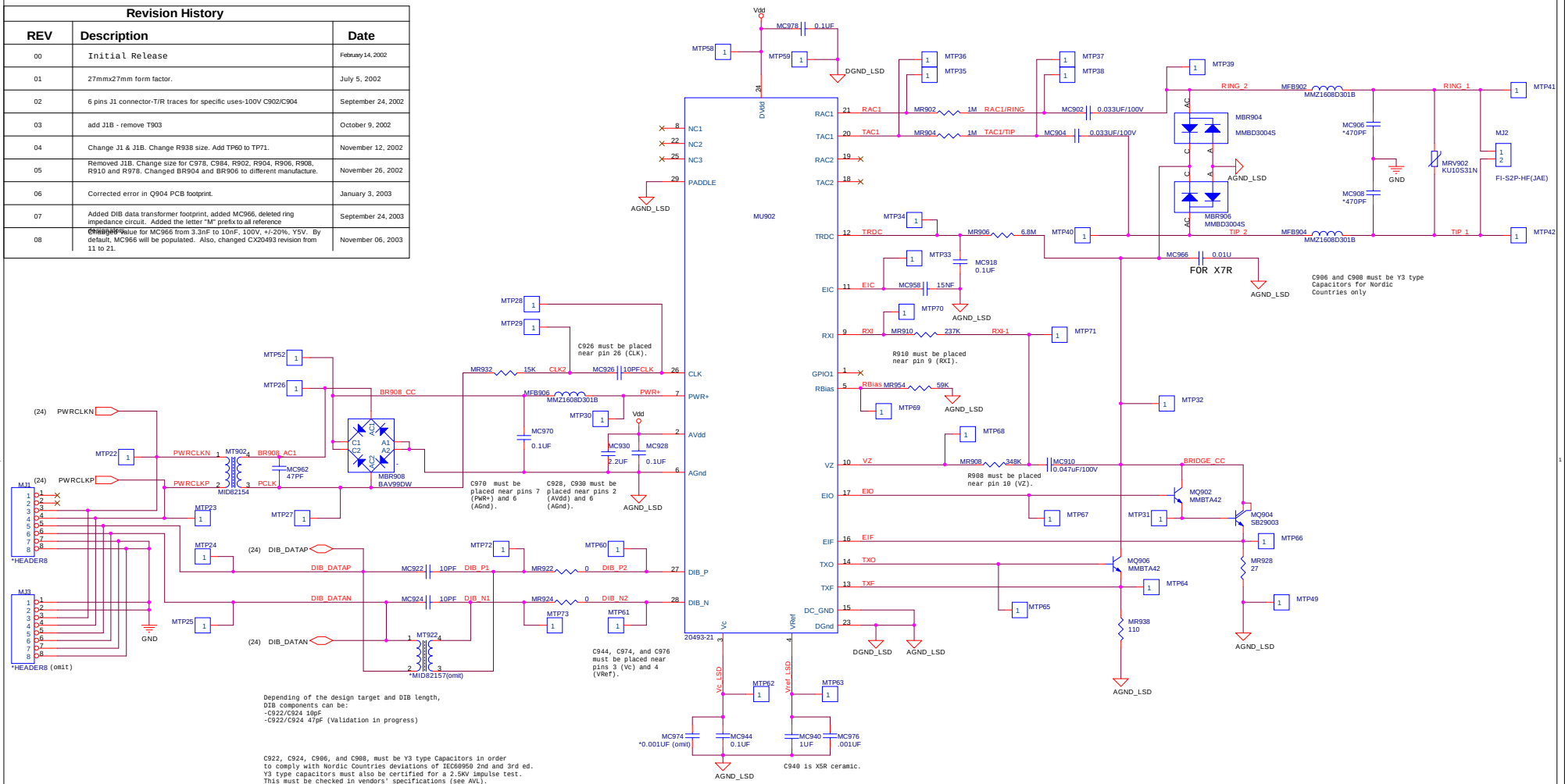
Size	Document Number	Rev
Custom	SMARTAMC-CONEXANT_20468-31	3B

Date: Thursday, October 27, 2005 Sheet 24 of 37

SMARTDAA_20493-21

MDM

Revision History		
REV	Description	Date
00	Initial Release	February 14, 2002
01	27mmx27mm form factor.	July 5, 2002
02	6 pins J1 connector-T/R traces for specific uses-100V C902/C904	September 24, 2002
03	add J1B - remove T903	October 9, 2002
04	Change J1 & J1B. Change R938 size. Add TP60 to TP71.	November 12, 2002
05	Removed J1B. Change size for C978, C984, R902, R904, R906, R908, R910 and R978. Changed BR904 and BR906 to different manufacture.	November 26, 2002
06	Corrected error in Q904 PCB footprint.	January 3, 2003
07	Added DIB data transformer footprint, added MC966, deleted ring impedance circuit. Added the letter "M" prefix to all reference designators.	September 24, 2003
08	Changed value for MC966 from 3.3nF to 10nF, 100V, +/-20%, Y5V. By default, MC966 will be populated. Also, changed CX20493 revision from 11 to 21.	November 06, 2003

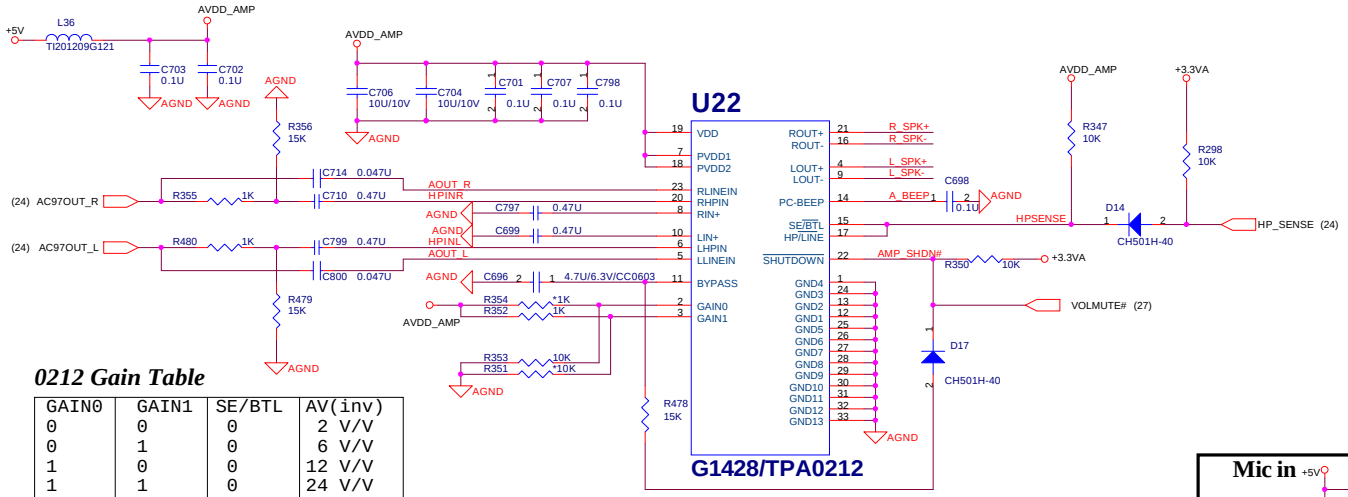


PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SMARTAMC-DAA_20493-21	1A
Date: Thursday, October 27, 2005	Sheet 25 of 37	

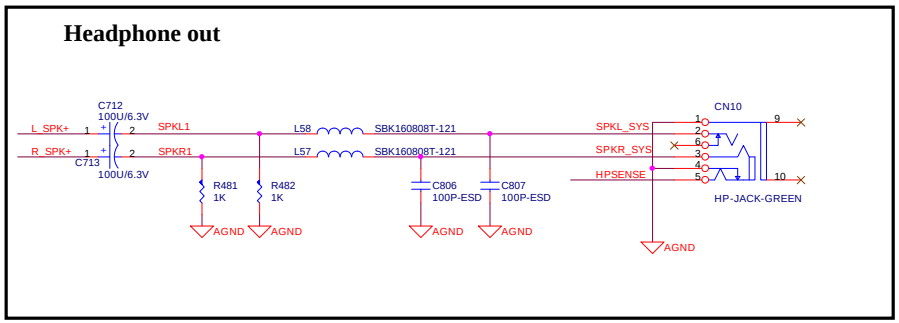
AUDIO AMPLIFIER

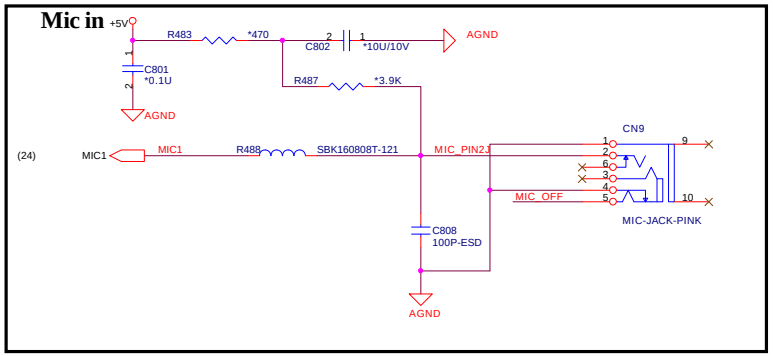
ADO

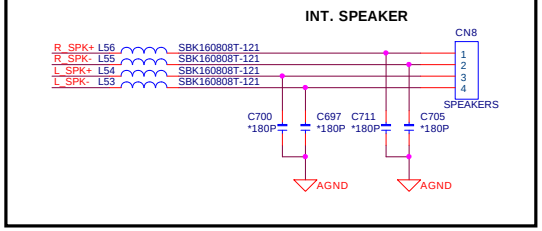


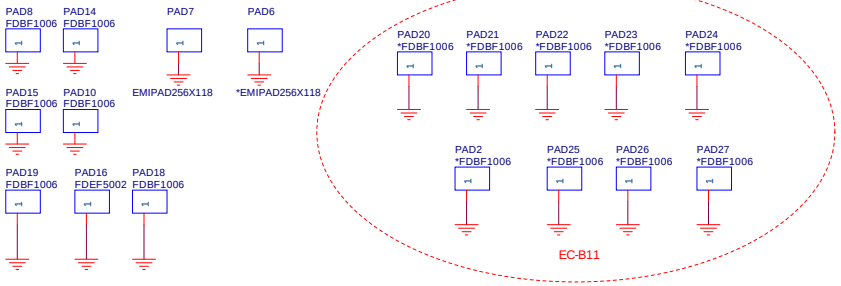
0212 Gain Table

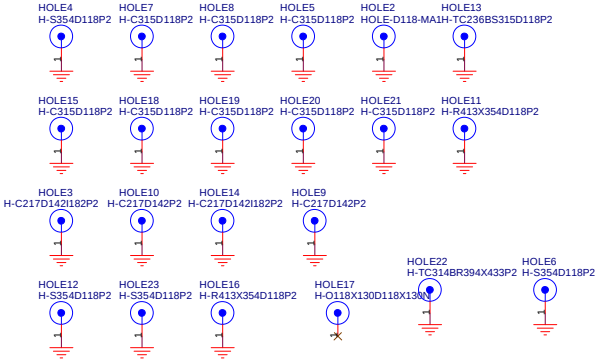
GAIN0	GAIN1	SE/BTL	AV(inv)
0	0	0	2 V/V
0	1	0	6 V/V
1	0	0	12 V/V
1	1	0	24 V/V
X	X	1	1 V/V











PROJECT : MA3
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AUDIO AMP & JACK	3A
Date: Thursday, October 27, 2005	Sheet 26 of 37	

KBC-NS97551L

KBC

FWH

POWER SWITCH

LDRQ#(pin 8) internal is no use

U18

PC97551VPC

U12

*39VF040
*TS0P32

Pin 103 internal is "A19",Can't use to GPIO

SHBM=1: Enable shared memory with host BIOS

BADDR1-0	I/O Address	
	Index	Data
0 0	2E	2F
0 1	4E	4F
1 0	(HCFGBAH, HCFGBAL)	(HCFGBAH, HCFGBAL)+1
1 1	Reserved	

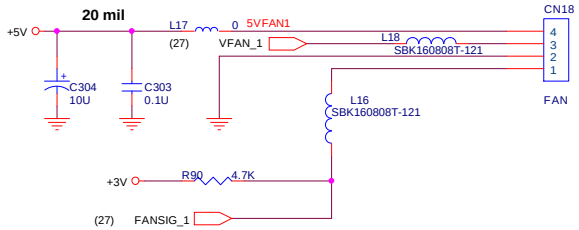
Should have a 0.1uF capacitor close to every GND-VCC pair + one larger cap on the supply.

POP FOR 97551

PROJECT :	MA3
Quanta Computer Inc.	
Size: Custom	Document Number: KBC-PC87551VPC
Rev:	3A
Date: Thursday, October 27, 2005	Sheet 27 of 37

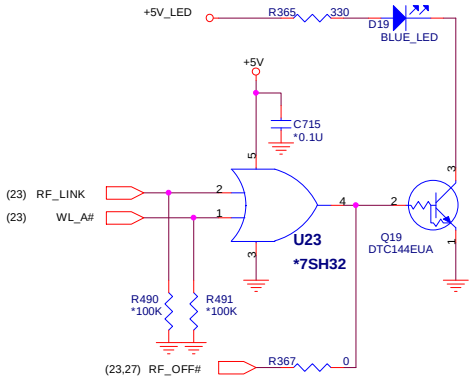
FAN OUT PWM CONNECTOR

THM



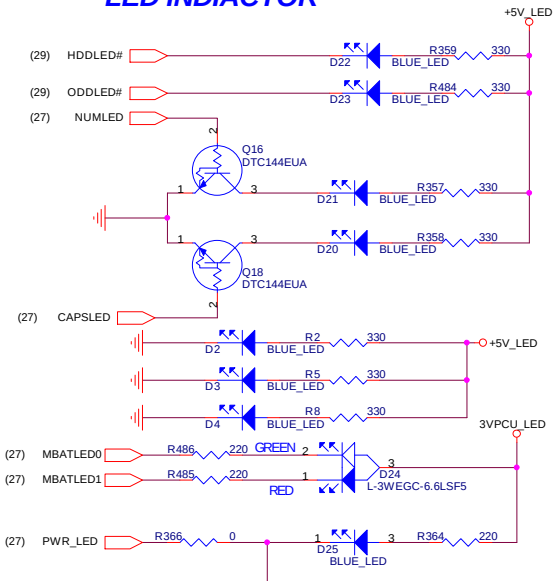
UIF

WIRELESS LED



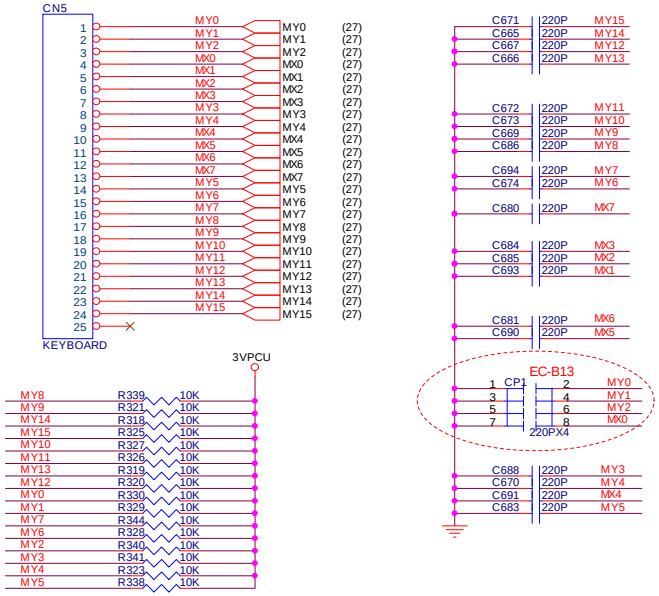
UIF

LED INDIACTOR



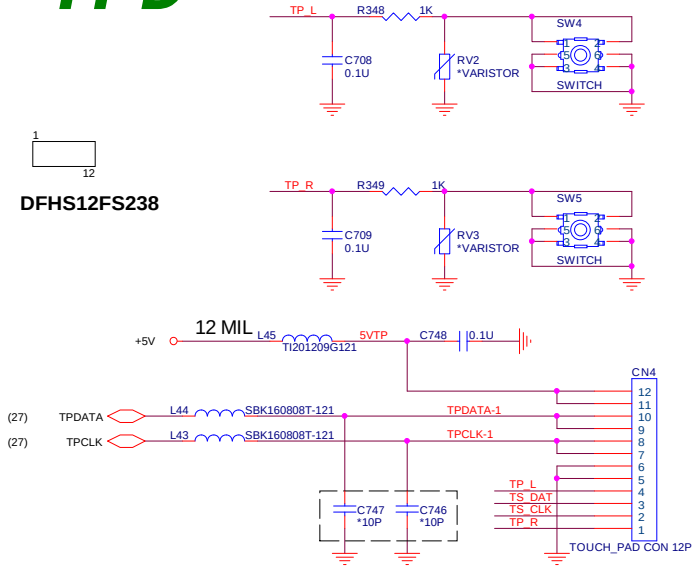
KEYBOARD

KBC



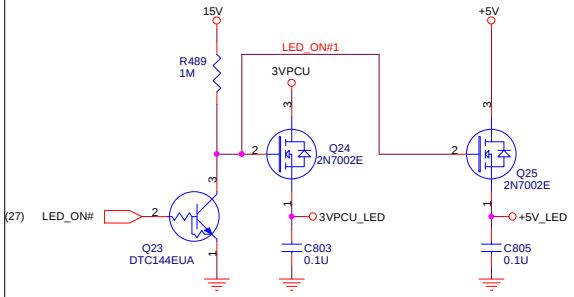
TPD

TOUCHPAD



1
12

DFHS12FS238



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Size	Document Number	Rev
Custom	K/B & FAN & LED & SW	3A
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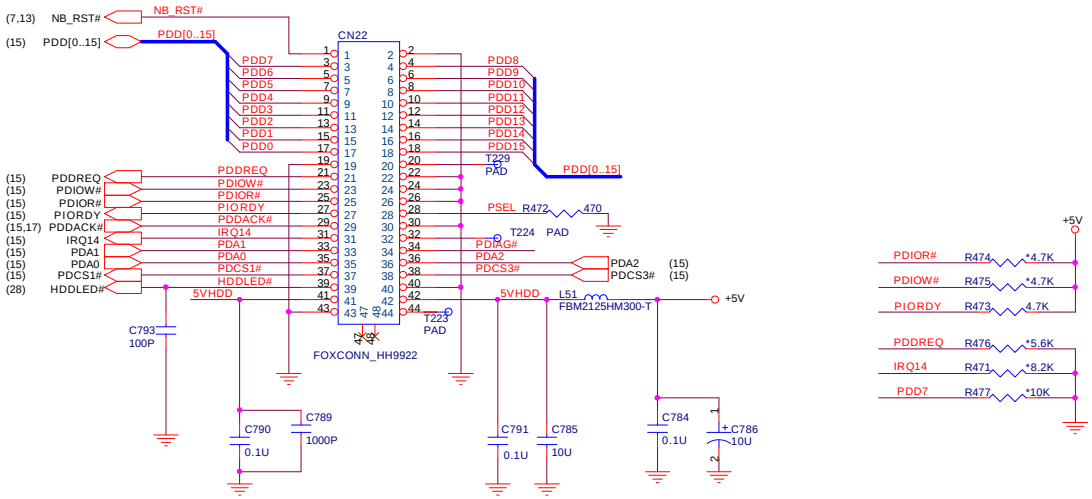
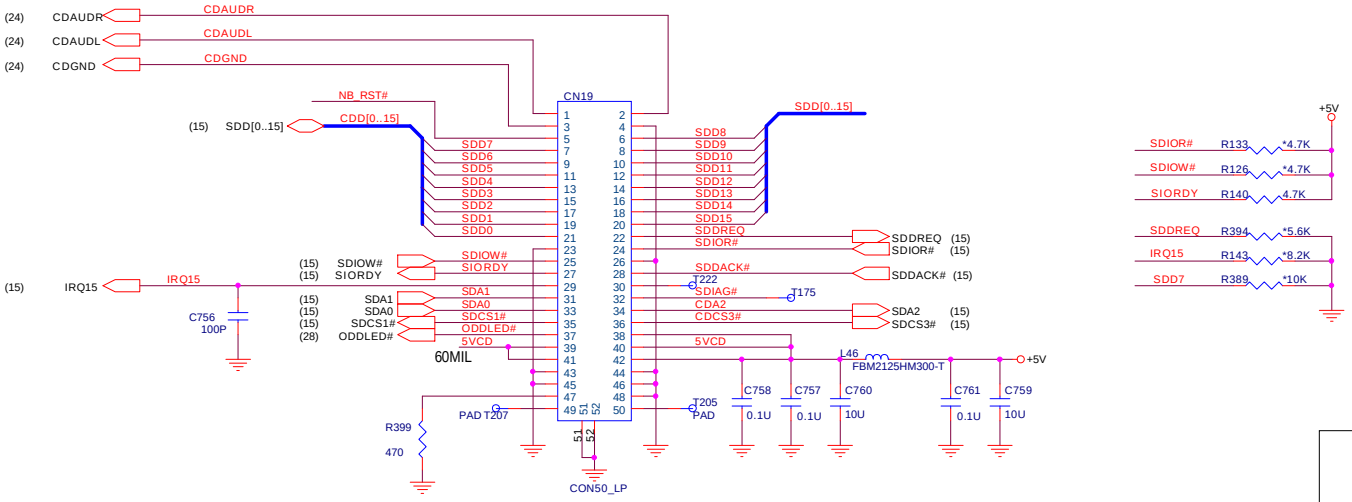
IDE

HDD connector



CD-ROM connector



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	IDE (HDD&CD_ROM	1A
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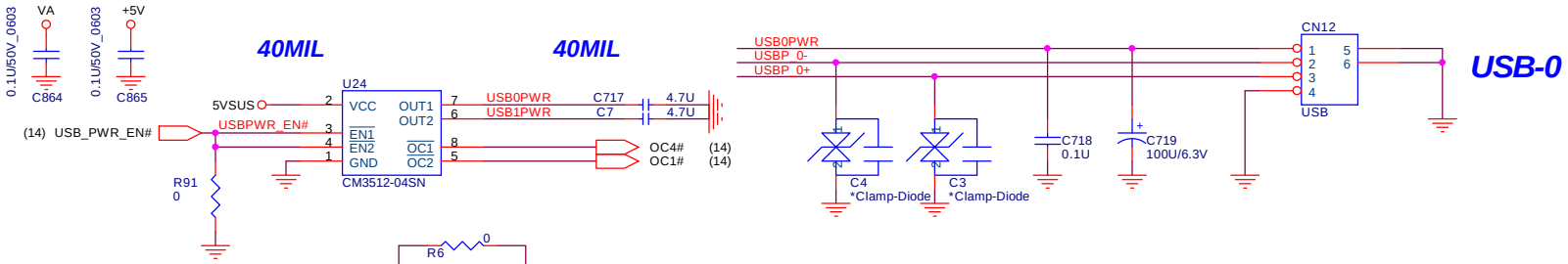
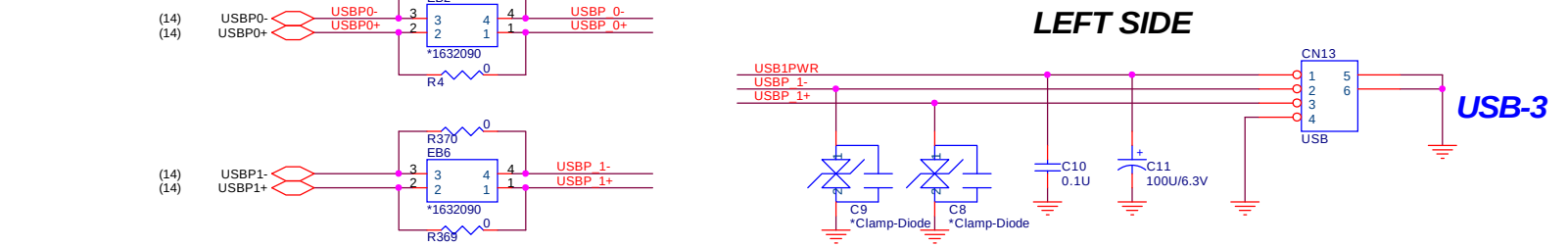
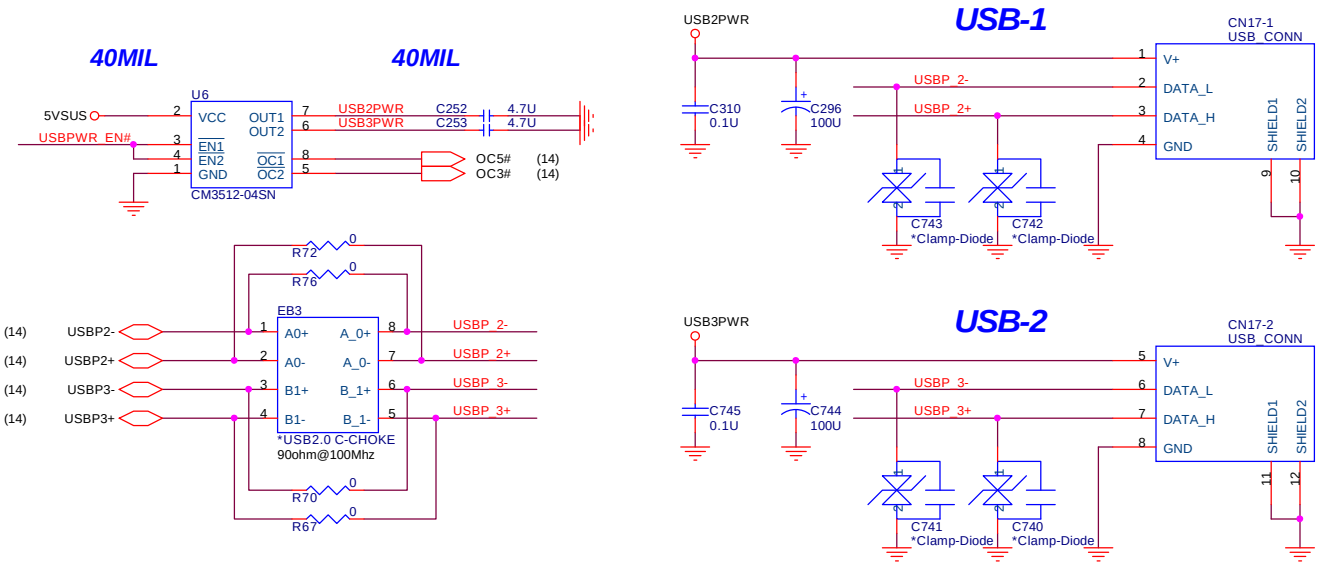
USB

LEFT SIDE



LEFT SIDE





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Size	Document Number	Rev
Custom	USB Ports	1A
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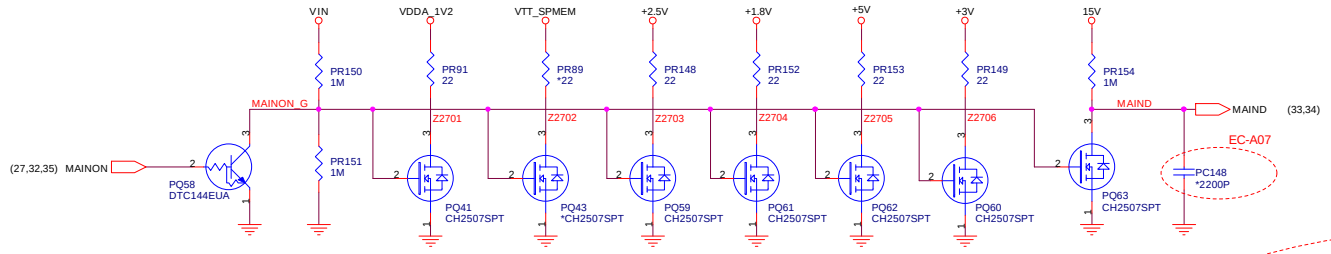

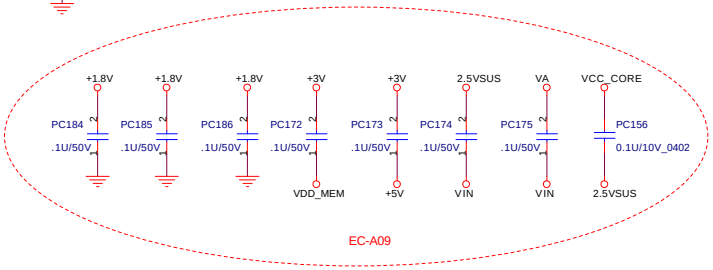

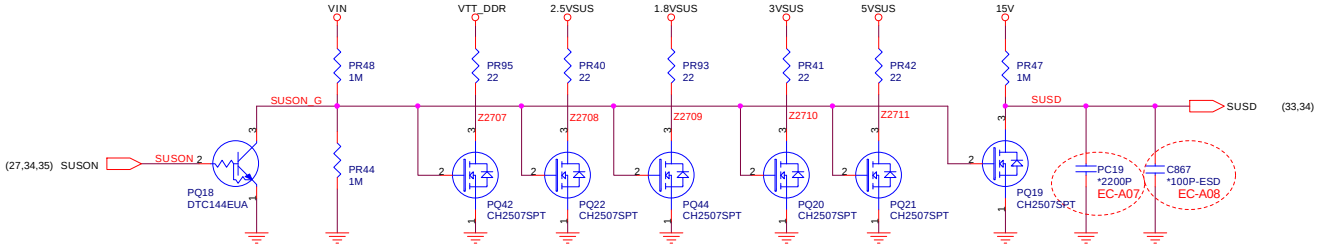

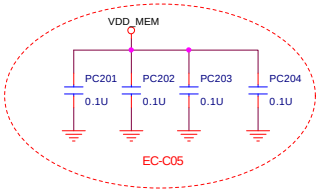

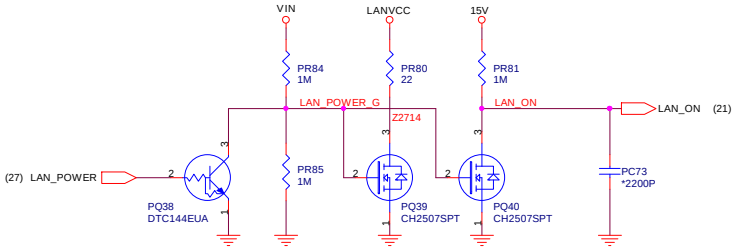

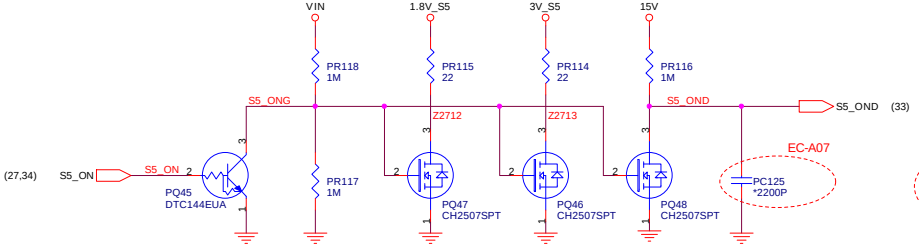

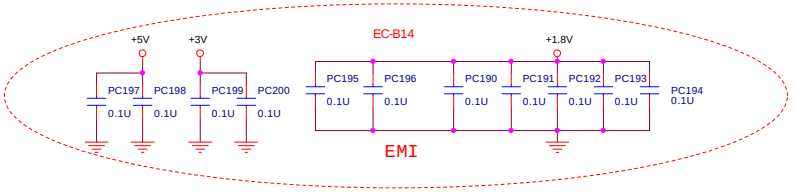

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Size	Document Number	Rev
Custom	DISCHARGE	3B
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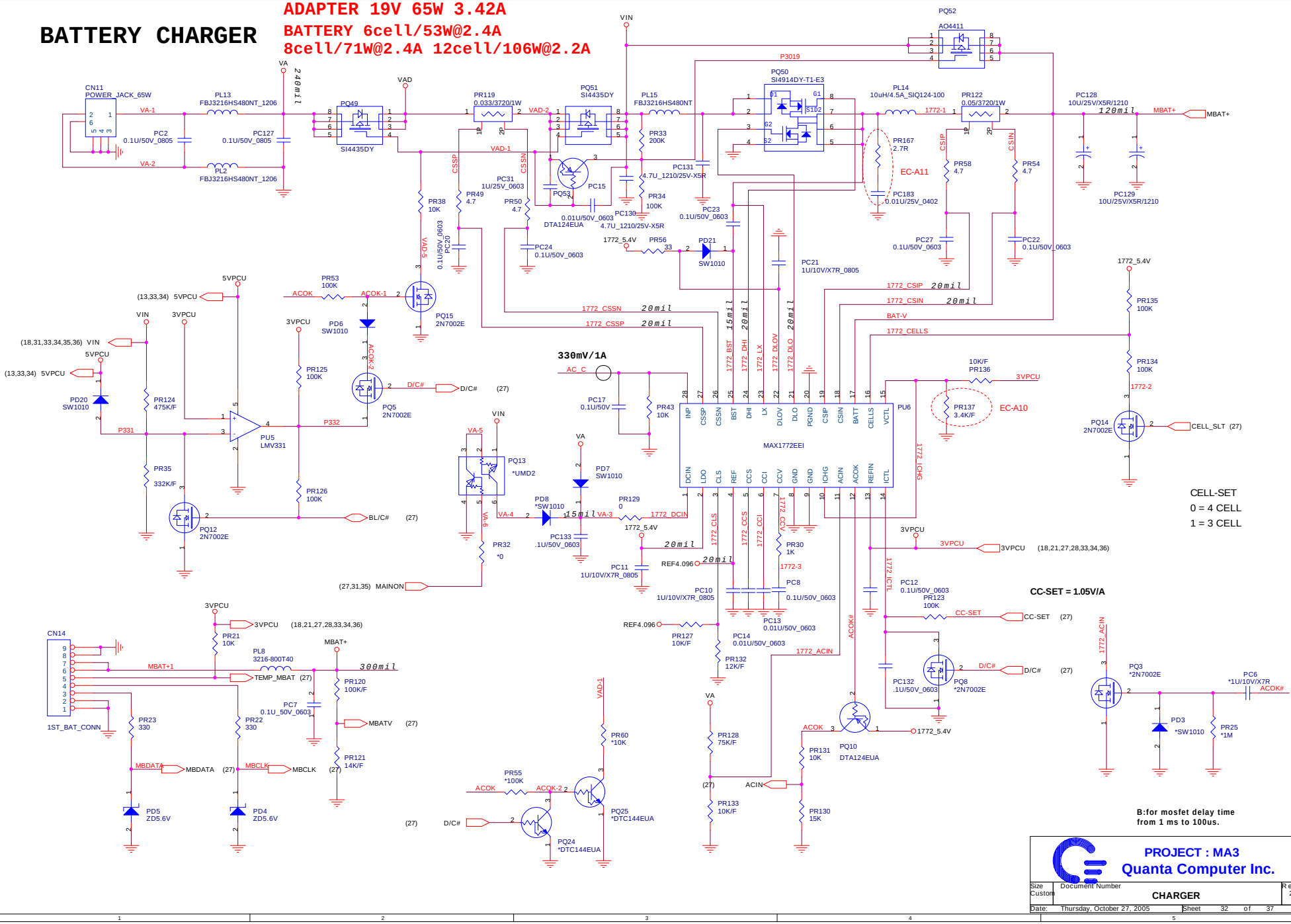
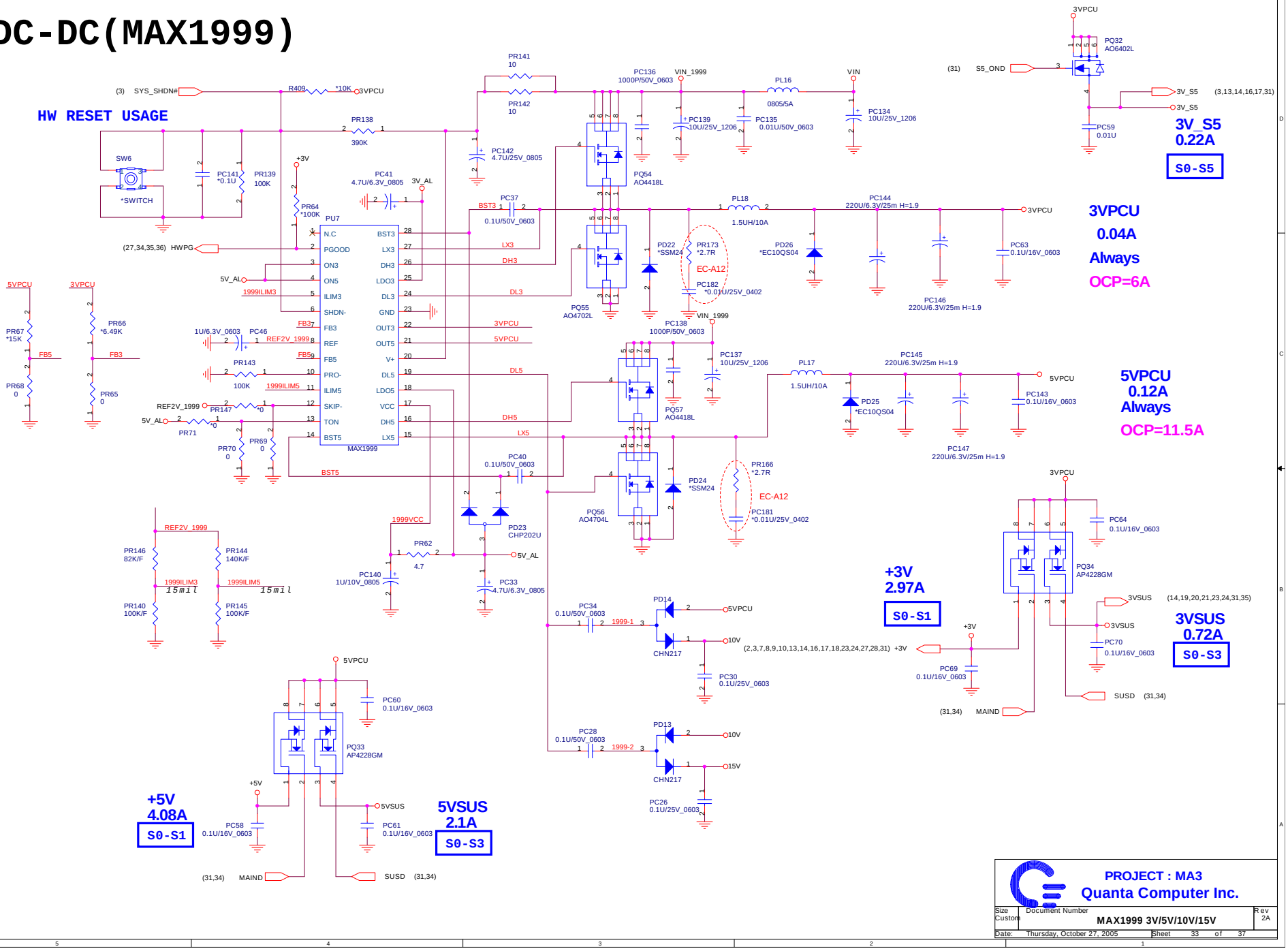
BATTERY CHARGER

ADAPTER 19V 65W 3.42A
BATTERY 6cell/53W@2.4A
8cell/71W@2.4A 12cell/106W@2.2A



DC-DC(MAX1999)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1999 3V/5V/10V/15V	2A
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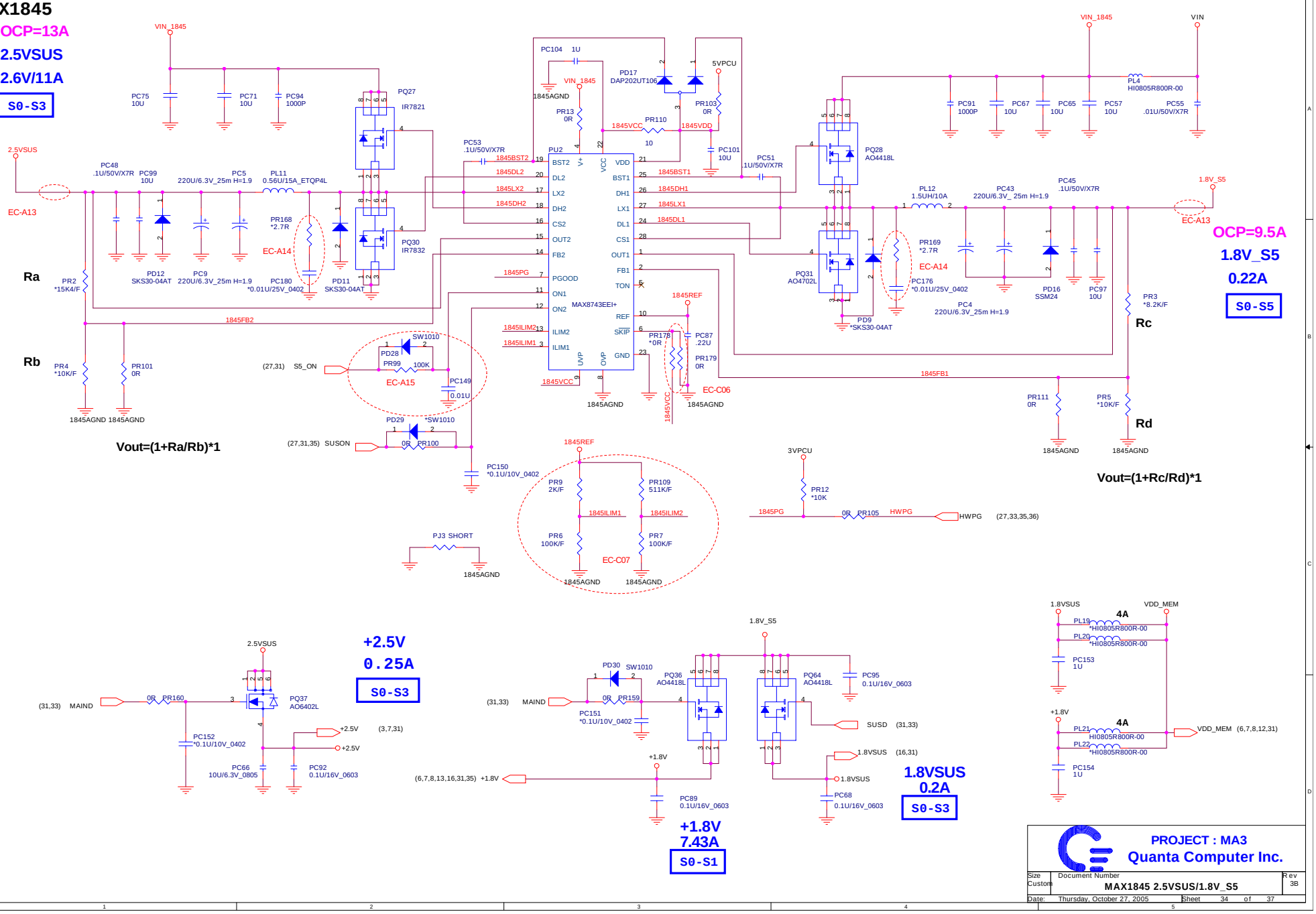
MAX1845

OCP=13A
2.5VSUS
2.6V/11A
S0-S3



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1845 2.5VSUS/1.8V_S5	3B
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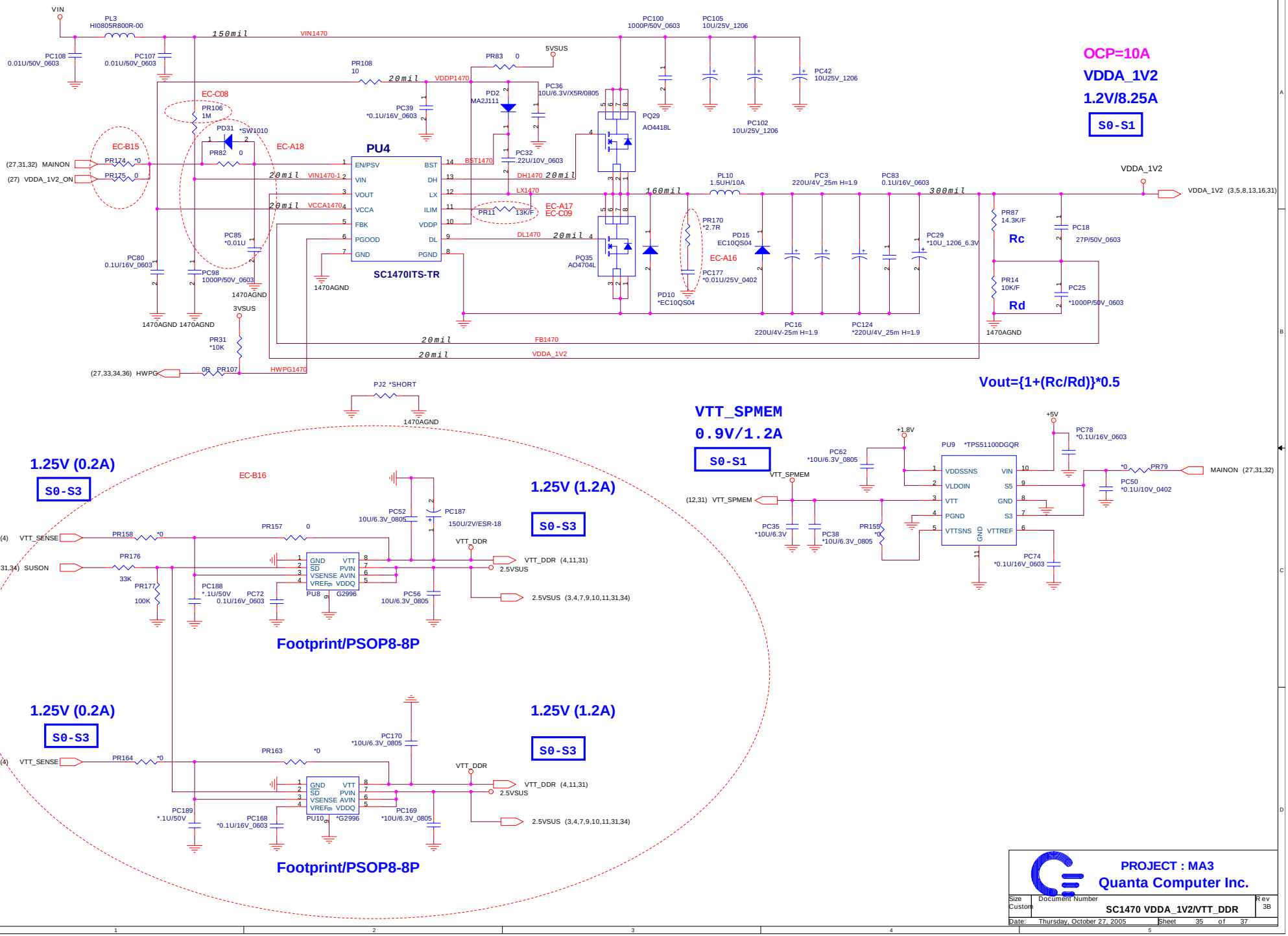
OCP=10A
VDDA_1V2
1.2V/8.25A
S0-S1
PU4
SC1470ITS-TR
Vout={1+(Rc/Rd)}*0.5
VTT_SPMEM
0.9V/1.2A
S0-S1
1.25V (0.2A)
S0-S3
1.25V (1.2A)
S0-S3
Footprint/PSOP8-8P
1.25V (0.2A)
S0-S3
1.25V (1.2A)
S0-S3
Footprint/PSOP8-8P
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Quanta Computer Inc.
SC1470 VDDA_1V2/VTT_DDR
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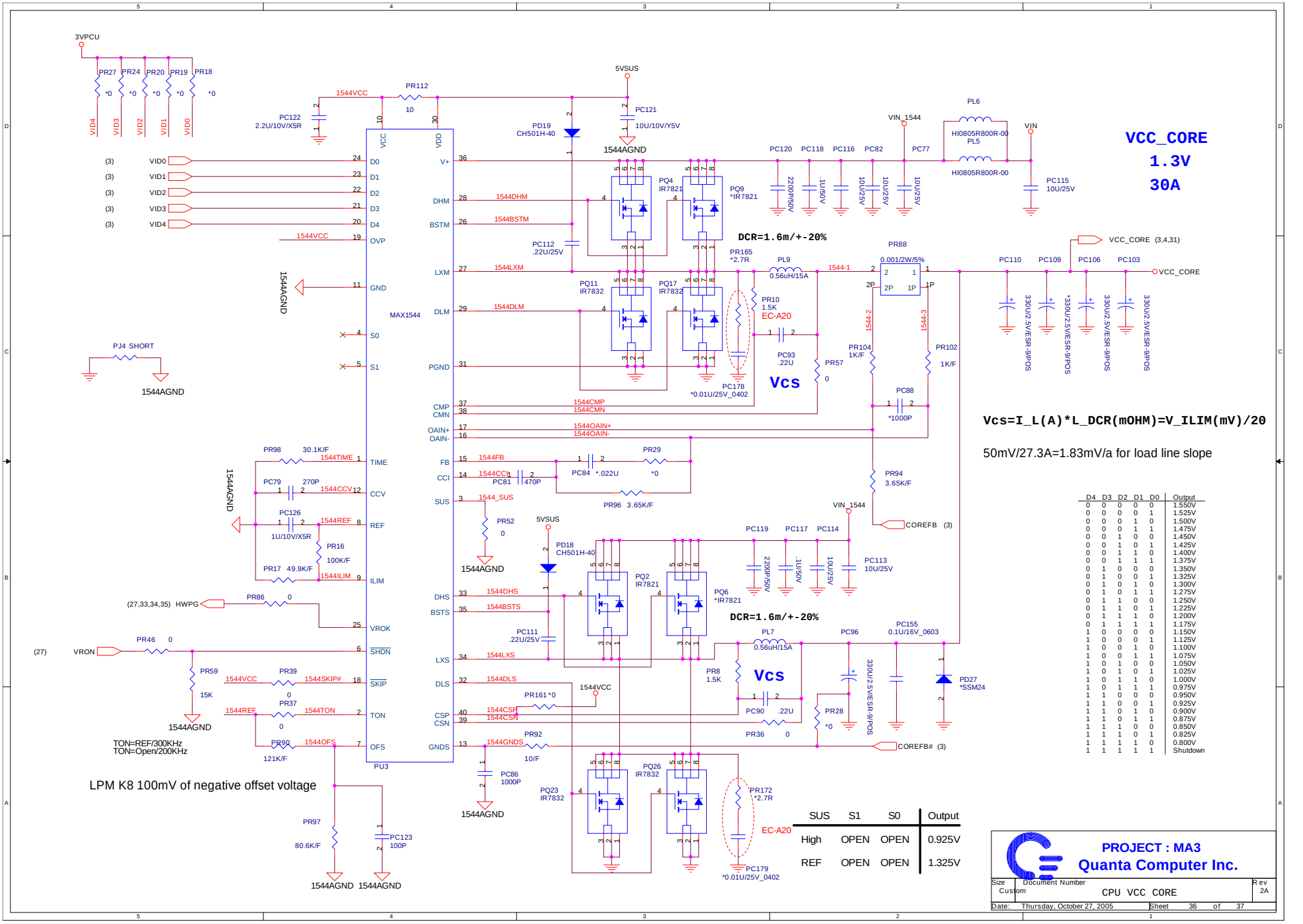

SUS	S1	S0	Output
High	OPEN	OPEN	0.925V
REF	OPEN	OPEN	1.325V

D4	D3	D2	D1	D0	Output
0	0	0	0	0	1.550V
0	0	0	0	1	1.525V
0	0	0	1	0	1.500V
0	0	0	1	1	1.475V
0	0	1	0	0	1.450V
0	0	1	0	1	1.425V
0	0	1	1	0	1.400V
0	0	1	1	1	1.375V
0	1	0	0	0	1.350V
0	1	0	0	1	1.325V
0	1	0	1	0	1.300V
0	1	0	1	1	1.275V
0	1	1	0	0	1.250V
0	1	1	0	1	1.225V
0	1	1	1	0	1.200V
0	1	1	1	1	1.175V
1	0	0	0	0	1.150V
1	0	0	0	1	1.125V
1	0	0	1	0	1.100V
1	0	0	1	1	1.075V
1	0	1	0	0	1.050V
1	0	1	0	1	1.025V
1	0	1	1	0	1.000V
1	0	1	1	1	0.975V
1	1	0	0	0	0.950V
1	1	0	0	1	0.925V
1	1	0	1	0	0.900V
1	1	0	1	1	0.875V
1	1	1	0	0	0.850V
1	1	1	0	1	0.825V
1	1	1	1	0	0.800V
1	1	1	1	1	Shutdown

Size	Custom
Document Number	CPU VCC CORE
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CHANGE LIST

Stage	Page	EC.	Change Description
A	Preliminary		
B	P.2	EC-A01	Add R542 & reserve it for EMI solution.
	P.13	EC-A02	Change C555,C566,C586 from reserve to 33PF for EMI solution.
	P.18	EC-A03	Change L38~L40 for meet RGB signal rising/falling time.
	P.19	EC-A04	Change R310 from 47 to 33 for meet CLK signal Slew Rate time.
	P.27	EC-A05	Add C866 for ESD solution.
		EC-A06	Change R244 from 0 to Diode for battery low signal.
	P.31	EC-A07	Change PC19,PC125,PC148 from 2200pF to reserve it for power sequence.
		EC-A08	Add C867 for ESD solution.
		EC-A09	Add PC156,PC172~PCPC175,PC184~PC186 for EMI solution.
	P.32	EC-A10	Change PR137 from 2.61K to 3.4K for charge volatge.
		EC-A11	Add PR167,PC183 & reserve it for EMI solution.
	P.33	EC-A12	Add PR173,PC182,PR166,PC181 & reserve it for EMI solution.
	P.34	EC-A13	Delete reserve resister PR15 & PR61.
		EC-A14	Add PR168,PC180,PR169,PC176 & reserve it for EMI solution.
		EC-A15	Change PR99,PC149 from 0 ,reserve to 100K,0.01uF & add PD28 for power sequence.
	P.35	EC-A16	Add PR170,PC177 & reserve it for EMI solution.
		EC-A17	Change PR11 from 13K to 24K for VDDA_1V2 OCP set.
		EC-A18	Change PR82,PC85 from 0 to 220K,0.01uF & add PD31 for power sequence.
		EC-A19	Add PU10 For VTT_DDR power rating.
	P.36	EC-A20	Add PR165,PC178,PR172,PC179 & reserve it for EMI solution.
C	P.2	EC-B01	Change L33 EMI FILTER from 120 to 300 and add C868,C869,C883 for EMI solution.
	P.3	EC-B02	Add R553,C884 for EMI solution.
	P.3	EC-B03	Add C870,C871,C872,C873 for ESD solution.
	P.7	EC-B04	Add C874,R544,C875 for EMI solution.
	P.13	EC-B05	Change BT2 connecter.
	P.13	EC-B06	Add R545~R548 & C877~C880 for EMI solution.
	P.13	EC-B07	Add C876 for ESD solution.
	P.18	EC-B08	Add C881,C882 for ESD solution.
	P.19	EC-B09	Change R310 from 33 to 15 for meet signal rising/falling time.
	P.21	EC-B10	Change LAN-Reset from LANRST# to PCIRST# & add R552.
	P.26	EC-B11	Add PAD20~PAD27 for EMI solution.
	P.27	EC-B12	Add net VDDA_1V2_ON for CPU power sequence.
	P.28	EC-B13	Add CP1 & delete C675,C676,C687,C692 for EMI solution.
	P.31	EC-B14	Add PC190~PC194 & PC195~PC200 for EMI solution.
	P.35	EC-B15	Add PR174,PR175 for CPU power sequence.
	P.35	EC-B16	Change PU8,PU10 for VTT_DDR power rating.
D	P.2	EC-C01	Add C885 for EMI solution.
	P.2	EC-C02	Add C886 and change R150 from 680 to 120 for ESD solution.
	P.14	EC-C03	Add C887 for ESD solution.
	P.24	EC-C04	Add MR955,MY2,ML1,MR956,L63,L62,MC979,MC980,MC981 for ESD solution.
	P.31	EC-C05	Add PC201~PC204 for EMI solution.
	P.34	EC-C06	Add PR178,PR179 for enable skip mode.
	P.34	EC-C07	Change PR6,PR9 to 100K,2K for 1.8V OCP and Change PR7,PR109 to 100K,511K for 2.5V OCP.
	P.35	EC-C08	Change PR106 to 1M for operation frequency to 300KHz.
	P.35	EC-C09	Change PR11 to 13K for 1.2V OCP.

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