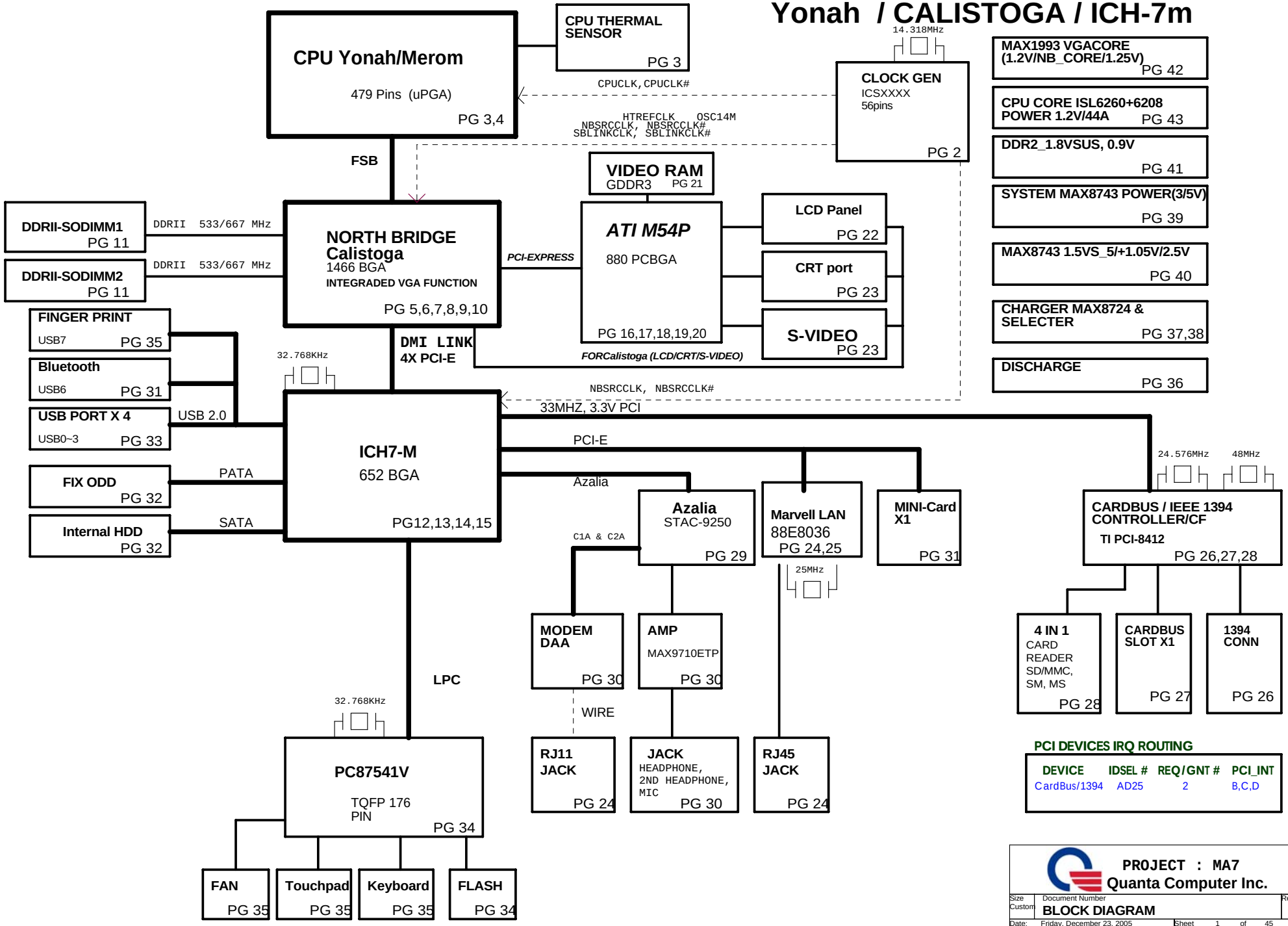
MA7 BLOCK DIAGRAM

Yonah / CALISTOGA / ICH-7m



PCI DEVICES IRQ ROUTING

DEVICE	IDSEL #	REQ/GNT #	PCI_INT
CardBus/1394	AD25	2	B,C,D

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	BLOCK DIAGRAM	3A

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FSC	FSB	FSA	CPU	SRC	PCI
1	0	1	100	100	33
0	0	1	133	100	33
0	1	1	166	100	33
0	1	0	200	100	33
0	0	0	266	100	33
1	0	0	333	100	33
1	1	0	400	100	33
1	1	1	200	100	33

Default

25 mils

L44 ACB2012L-120-T

+3V — 120 ohms@100Mhz — VDD_PCI

C452 0.1U, C461 0.1U, C701 10U-6.3V_8

R516 2.2/F_6 VDD_48

C462 0.1U, C700 10U-6.3V_8

R515 1_6 VDD_REF

C698 0.1U, C699 10U-6.3V_8

+3V — U16 — (14) VR_PWRGD_CK410 — VR_PWRGD_CK410# — SN74LVC1G04DCKR

L26 ACB2012L-120-T

+3V — 120 ohms@100Mhz — VDD_SRC_CPU

25 mils

C697 0.1U, C456 0.1U, C447 0.1U, C693 0.1U, C455 10U-6.3V_8

R506 2.2/F_6 VDD_A

C696 0.1U, C695 10U-6.3V_8

Close to IC <500mils

VDD_A

C411 33P — CG_XIN

Y3 CL=20 - 22P 14.318MHZ

C451 33P — CG_XOUT

+3V — R281 *10K

(43) VR_PWRGD_CK410# — VR_PWRGD_CK410#

(14) PM_STPPCI# — PM_STPPCI#

(14) PM_STPCPU# — PM_STPCPU#

(11,31) CGCLK_SMB — CGCLK_SMB

(11,31) CGDAT_SMB — CGDAT_SMB

(14) CLKUSB_48 — R305 15_R_48M

(28) CLK48M — R316 15

CLK_BSEL0 — R315 2.2K

CLK_BSEL1

CLK_BSEL2 — R238 4.7K

VDD_REF

VDD_SRC_CPU

VDD_PCI

VDD_SRC_CPU

VDD_48

Iref=5mA, Ioh=4*Iref — R509 475/F_6 IREF

(7) DREFCLK — DREFCLK — RP43 — R_DOT96

(7) DREFCLK# — DREFCLK# — R_DOT96#

33X2

U14

XTAL_IN, XTAL_OUT

Vtt_PwrGd#/PD, PCI/SRC_STOP#, CPU_STOP#

SCLK, SDATA

FSA/USB_48MHz, FSB/TEST_MODE, FSC/REF1

VDD_REF, VDD_CPU, VDD_PCI_1, VDD_PCI_2, VDD_SRC0, VDD_SRC1, VDD_SRC2, VDD_48, IREF

DOT96MHz, DOT96MHz#

GND_48, GND_REF, GND_PCI_1, GND_PCI_2, GND_SRC, GND_CPU

ICS954206AG-

CK-410M

REF0, CPU0/CPU0#, CPU1/CPU1#, CPU2_ITP/SRC7/CPU2#_ITP/SRC7#, SRC6/SRC6#, SRC5/SRC5#, SRC4_SATA/SRC4#_SATA, SRC3/SRC3#, SRC2/SRC2#, SRC1/SRC1#, SRC0/DREFSSCLK/SRC0#/DREFSSCLK#, PCI5, PCI4, PCI3, PCI2, PCIF1/100_96M#, PCIF0/ITP_EN

SMbus address D2 /IDT

IDT CV140 /56pins

ICS954206AGT /56pins

Place these termination to close CK410M.

14M_REF — R240 33 — 14M_ICH (14)

C395 *10P

RHCLK_CPU, RHCLK_CPU# — RP38 — 33X2 — CLK_CPU_BCLK (3), CLK_CPU_BCLK# (3)

RHCLK_MCH, RHCLK_MCH# — RP39 — 33X2 — CLK_MCH_BCLK (5), CLK_MCH_BCLK# (5)

T220, T221

RSRC_MINICARD1, RSRC_MINICARD1# — RP41 — 33X2 — SRC_MINICARD1 (31), SRC_MINICARD1# (31)

R_PCIE_LAN, R_PCIE_LAN# — RP42 — 33X2 — CLK_PCIE_LAN (24), CLK_PCIE_LAN# (24)

R_SATA, R_SATA# — RP48 — 33X2 — CLK_PCIE_SATA (12), CLK_PCIE_SATA# (12)

R_PCIE_PEG, R_PCIE_PEG# — RP47 — 33X2 — CLK_PCIE_PEG (16), CLK_PCIE_PEG# (16)

R_MCH, R_MCH# — RP46 — 33X2 — CLK_PCIE_3GPLL (7), CLK_PCIE_3GPLL# (7)

R_PCIE_ICH, R_PCIE_ICH# — RP45 — 33X2 — CLK_PCIE_ICH (13), CLK_PCIE_ICH# (13)

R_DREFSSCLK, R_DREFSSCLK# — RP44 — 33X2 — DREFSSCLK (7), DREFSSCLK# (7)

R_PCLK_551 — R284 33 — PCLK_551 (34)

R_PCLK_7412 — R283 33 — PCLK_7412 (26)

T223, T224

R_PCLK_ICH — R304 33 — PCLK_ICH (13)

R_PCLK — R303 33 — PCLK_LPC_DEBUG (31)

R285 10K

R313 *10K — +3V

R314 *10K — +3V

R286 10K

DREFSSCLK Frequency Select.
"0" : 96MHz
"1" : 100MHz

CLK	ATI	INTEL
RP53	49.9	X
RP47	33	X

Place these termination to close CK410M.

RP35 49.9/FX2: CLK_CPU_BCLK, CLK_CPU_BCLK#

RP36 49.9/FX2: CLK_MCH_BCLK, CLK_MCH_BCLK#

RP51 49.9/FX2: CLK_PCIE_ICH#, CLK_PCIE_ICH

RP55 49.9/FX2: CLK_PCIE_LAN, CLK_PCIE_LAN#

RP58 49.9/FX2: SRC_MINICARD1, SRC_MINICARD1#

RP54 49.9/FX2: CLK_PCIE_SATA#, CLK_PCIE_SATA

RP53 49.9/FX2: CLK_PCIE_PEG#, CLK_PCIE_PEG

RP52 49.9/FX2: CLK_PCIE_3GPLL#, CLK_PCIE_3GPLL

RP50 49.9/FX2: DREFSSCLK#, DREFSSCLK

RP49 49.9/FX2: DREFCLK#, DREFCLK

+1.05V — R318 56

(3) CPU_BSEL0 — R317 0 — CLK_BSEL0 — R320 1K — MCH_BSEL0 (7)

R319 1K — R328 *0 — XDP_BPM#1 (3)

+1.05V — R236 1K

(3) CPU_BSEL1 — R233 0 — CLK_BSEL1 — R234 1K — MCH_BSEL1 (7)

R235 *0 — R220 *0 — XDP_BPM#2 (3)

Stuff 0 ohm for 533MHz, NC for 667MHz

+1.05V — R223 1K

(3) CPU_BSEL2 — R224 0 — CLK_BSEL2 — R222 1K — MCH_BSEL2 (7)

R225 *0 — R221 *0 — XDP_BPM#3 (3)

+3V

Q14 RHU002N06 — R241 10K — R242 10K

(14) PDAT_SMB — CGDAT_SMB

Q15 RHU002N06

(14) PCLK_SMB — CGCLK_SMB

These are for backdrive issue

PCLK_ICH, PCLK_551, PCLK_7412

C472 15P, C473 *10P, C478 15P

(3,7,8,9,11,12,13,14,15,16,17,18,19,22,23,24,28,31,32,34,35,36,39,42,43) +3V — +3V

(3,4,5,7,8,9,12,15,36,40) +1.05V — +1.05V

PROJECT : MA7

Quanta Computer Inc.

Size	Document Number	Rev
Custom	CLOCK GENERATOR	3A

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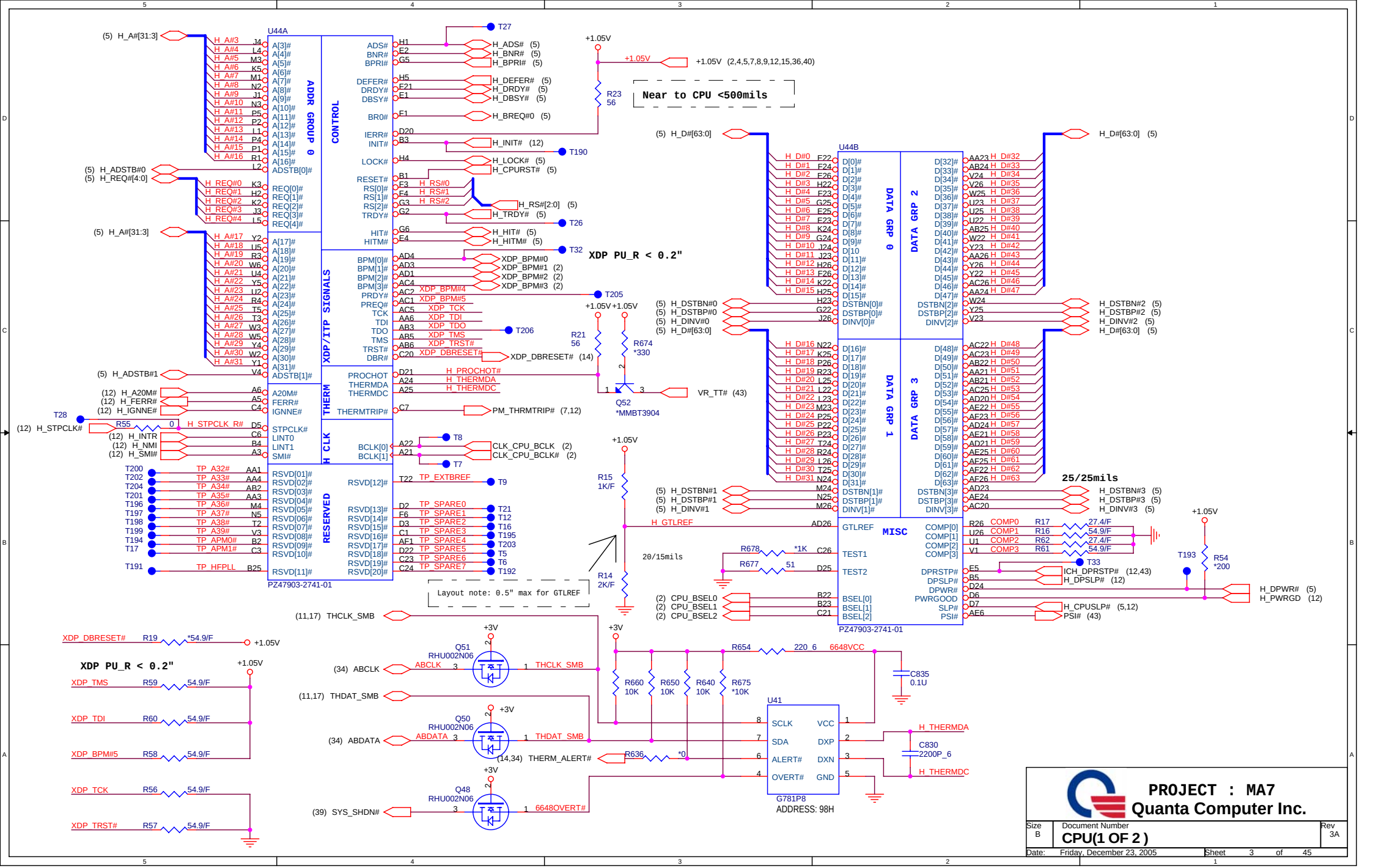
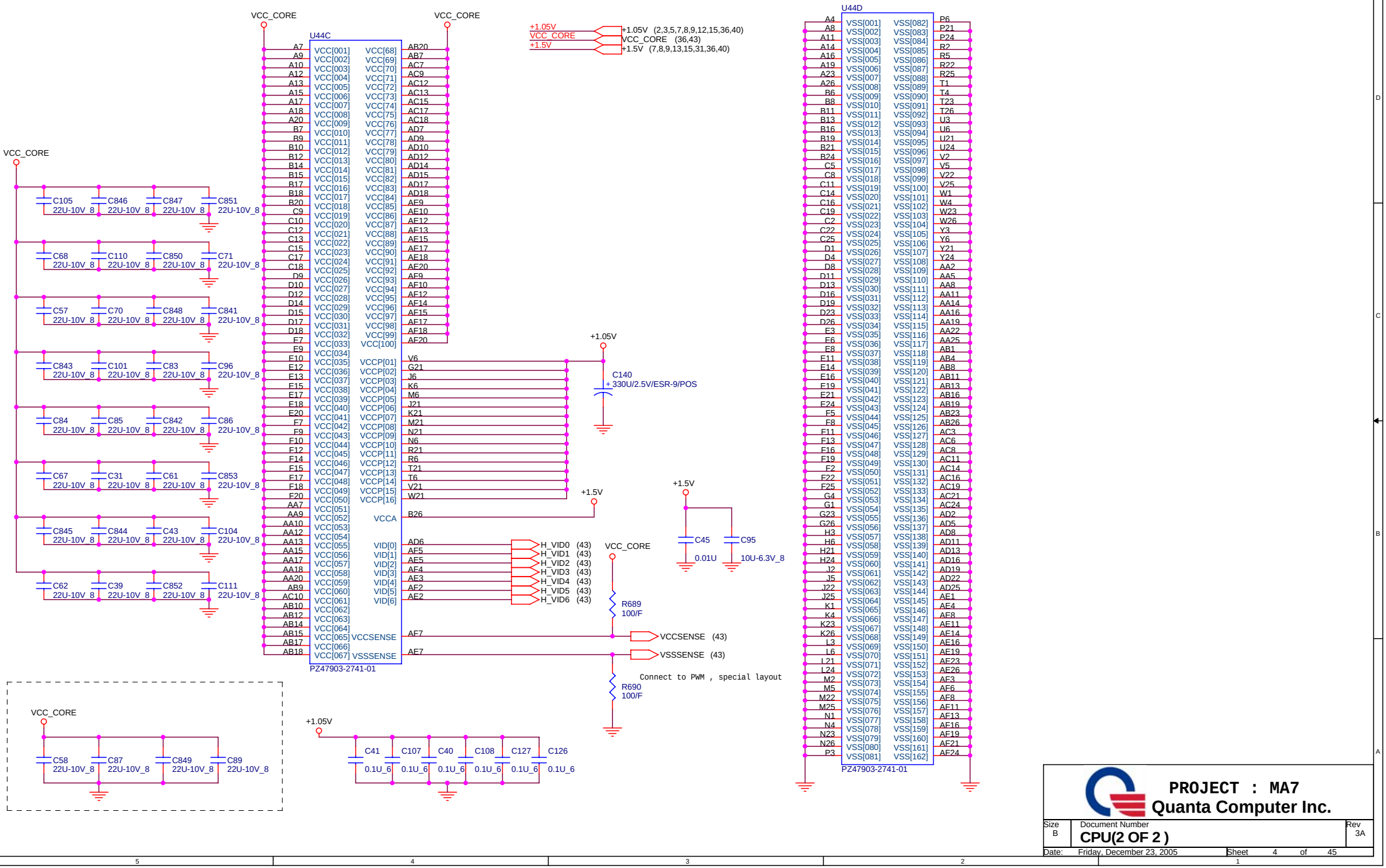

U44A
ADDR GROUP 0
CONTROL
XDP/ITP SIGNALS
THERM
H CLK
RESERVED
PZ47903-2741-01
U44B
DATA GRP 0
DATA GRP 2
DATA GRP 1
DATA GRP 3
MISC
PZ47903-2741-01
Near to CPU <500mils
XDP PU_R < 0.2"
Layout note: 0.5" max for GTLREF
25/25mils
U41
G781P8
ADDRESS: 98H
PROJECT : MA7
Quanta Computer Inc.
CPU(1 OF 2)
Friday, December 23, 2005


VCC_CORE
U44C
PZ47903-2741-01
C105 C846 C847 C851 22U-10V_8
C68 C110 C850 C71 22U-10V_8
C57 C70 C848 C841 22U-10V_8
C843 C101 C83 C96 22U-10V_8
C84 C85 C842 C86 22U-10V_8
C67 C31 C61 C853 22U-10V_8
C845 C844 C43 C104 22U-10V_8
C62 C39 C852 C111 22U-10V_8
C58 C87 C849 C89 22U-10V_8
+1.05V
VCC_CORE
+1.5V
+1.05V (2,3,5,7,8,9,12,15,36,40)
VCC_CORE (36,43)
+1.5V (7,8,9,13,15,31,36,40)
C140
330U/2.5V/ESR-9/POS
C45 0.01U
C95 10U-6.3V_8
R689 100/F
R690 100/F
VCCSENSE (43)
VSSSENSE (43)
Connect to PWM , special layout
C41 C107 C40 C108 C127 C126 0.1U_6
U44D
PZ47903-2741-01
PROJECT : MA7
Quanta Computer Inc.
Size B
Document Number
CPU(2 OF 2)
Rev 3A
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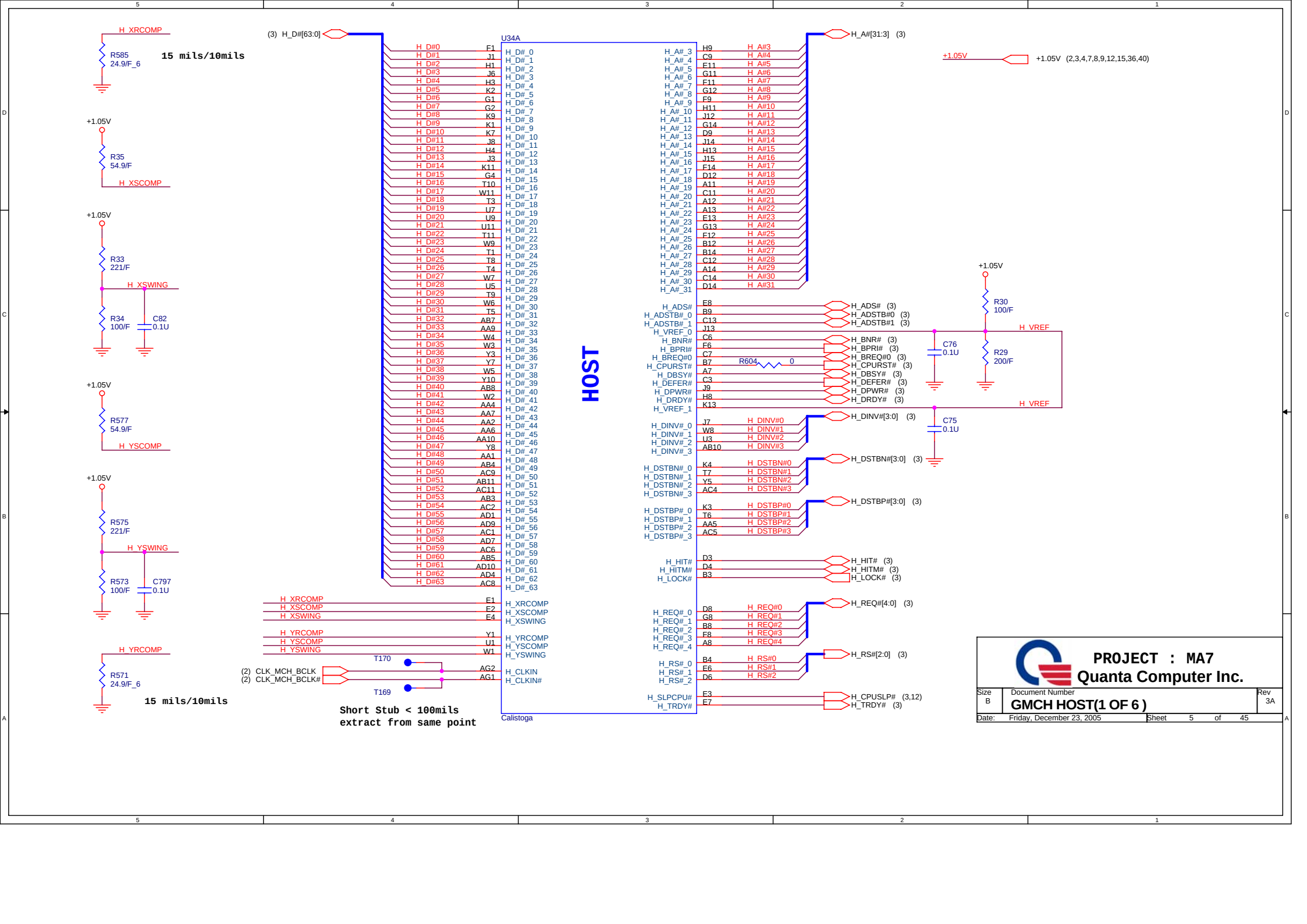
H_XRCOMP
R585
24.9/F_6
15 mils/10mils
+1.05V
R35
54.9/F
H_XSCOMP
+1.05V
R33
221/F
H_XSWING
R34
100/F
C82
0.1U
+1.05V
R577
54.9/F
H_YSCOMP
+1.05V
R575
221/F
H_YSWING
R573
100/F
C797
0.1U
H_YRCOMP
R571
24.9/F_6
15 mils/10mils
(3) H_D#[63:0]
U34A
HOST
Calistoga
H_D#0 F1
H_D#1 J1
H_D#2 H1
H_D#3 J6
H_D#4 H3
H_D#5 K2
H_D#6 G1
H_D#7 G2
H_D#8 K9
H_D#9 K1
H_D#10 K7
H_D#11 J8
H_D#12 H4
H_D#13 J3
H_D#14 K11
H_D#15 G4
H_D#16 T10
H_D#17 W11
H_D#18 T3
H_D#19 U7
H_D#20 U9
H_D#21 U11
H_D#22 T11
H_D#23 W9
H_D#24 T1
H_D#25 T8
H_D#26 T4
H_D#27 W7
H_D#28 U5
H_D#29 T9
H_D#30 W6
H_D#31 T5
H_D#32 AB7
H_D#33 AA9
H_D#34 W4
H_D#35 W3
H_D#36 Y3
H_D#37 Y7
H_D#38 W5
H_D#39 Y10
H_D#40 AB8
H_D#41 W2
H_D#42 AA4
H_D#43 AA7
H_D#44 AA2
H_D#45 AA6
H_D#46 AA10
H_D#47 Y8
H_D#48 AA1
H_D#49 AB4
H_D#50 AC9
H_D#51 AB11
H_D#52 AC11
H_D#53 AB3
H_D#54 AC2
H_D#55 AD1
H_D#56 AD9
H_D#57 AC1
H_D#58 AD7
H_D#59 AC6
H_D#60 AB5
H_D#61 AD10
H_D#62 AD4
H_D#63 AC8
H_XRCOMP E1
H_XSCOMP E2
H_XSWING E4
H_YRCOMP Y1
H_YSCOMP U1
H_YSWING W1
T170
T169
(2) CLK_MCH_BCLK
(2) CLK_MCH_BCLK#
AG2
AG1
H_CLKIN
H_CLKIN#
Short Stub < 100mils
extract from same point
H_A#_3 H9
H_A#_4 C9
H_A#_5 E11
H_A#_6 G11
H_A#_7 F11
H_A#_8 G12
H_A#_9 F9
H_A#_10 H11
H_A#_11 J12
H_A#_12 G14
H_A#_13 D9
H_A#_14 J14
H_A#_15 H13
H_A#_16 J15
H_A#_17 F14
H_A#_18 D12
H_A#_19 A11
H_A#_20 C11
H_A#_21 A12
H_A#_22 A13
H_A#_23 E13
H_A#_24 G13
H_A#_25 F12
H_A#_26 B12
H_A#_27 B14
H_A#_28 C12
H_A#_29 A14
H_A#_30 C14
H_A#_31 D14
H_A#[31:3] (3)
H_A#3
H_A#4
H_A#5
H_A#6
H_A#7
H_A#8
H_A#9
H_A#10
H_A#11
H_A#12
H_A#13
H_A#14
H_A#15
H_A#16
H_A#17
H_A#18
H_A#19
H_A#20
H_A#21
H_A#22
H_A#23
H_A#24
H_A#25
H_A#26
H_A#27
H_A#28
H_A#29
H_A#30
H_A#31
+1.05V
+1.05V (2,3,4,7,8,9,12,15,36,40)
H_ADS# E8
H_ADSTB#_0 B9
H_ADSTB#_1 C13
H_VREF_0 J13
H_BNR# C6
H_BPRI# F6
H_BREQ#0 C7
H_CPURST# B7
H_DBSY# A7
H_DEFER# C3
H_DPWR# J9
H_DRDY# H8
H_VREF_1 K13
H_ADS# (3)
H_ADSTB#0 (3)
H_ADSTB#1 (3)
H_BNR# (3)
H_BPRI# (3)
H_BREQ#0 (3)
H_CPURST# (3)
H_DBSY# (3)
H_DEFER# (3)
H_DPWR# (3)
H_DRDY# (3)
R604
0
+1.05V
R30
100/F
H_VREF
C76
0.1U
R29
200/F
H_VREF
C75
0.1U
H_DINV#_0 J7
H_DINV#_1 W8
H_DINV#_2 U3
H_DINV#_3 AB10
H_DINV#0
H_DINV#1
H_DINV#2
H_DINV#3
H_DINV#[3:0] (3)
H_DSTBN#_0 K4
H_DSTBN#_1 T7
H_DSTBN#_2 Y5
H_DSTBN#_3 AC4
H_DSTBN#0
H_DSTBN#1
H_DSTBN#2
H_DSTBN#3
H_DSTBN#[3:0] (3)
H_DSTBP#_0 K3
H_DSTBP#_1 T6
H_DSTBP#_2 AA5
H_DSTBP#_3 AC5
H_DSTBP#0
H_DSTBP#1
H_DSTBP#2
H_DSTBP#3
H_DSTBP#[3:0] (3)
H_HIT# D3
H_HITM# D4
H_LOCK# B3
H_HIT# (3)
H_HITM# (3)
H_LOCK# (3)
H_REQ#_0 D8
H_REQ#_1 G8
H_REQ#_2 B8
H_REQ#_3 F8
H_REQ#_4 A8
H_REQ#0
H_REQ#1
H_REQ#2
H_REQ#3
H_REQ#4
H_REQ#[4:0] (3)
H_RS#_0 B4
H_RS#_1 E6
H_RS#_2 D6
H_RS#0
H_RS#1
H_RS#2
H_RS#[2:0] (3)
H_SLPCPU# E3
H_TRDY# E7
H_CPUSLP# (3,12)
H_TRDY# (3)
PROJECT : MA7
Quanta Computer Inc.
Size B
Document Number
GMCH HOST(1 OF 6)
Rev 3A
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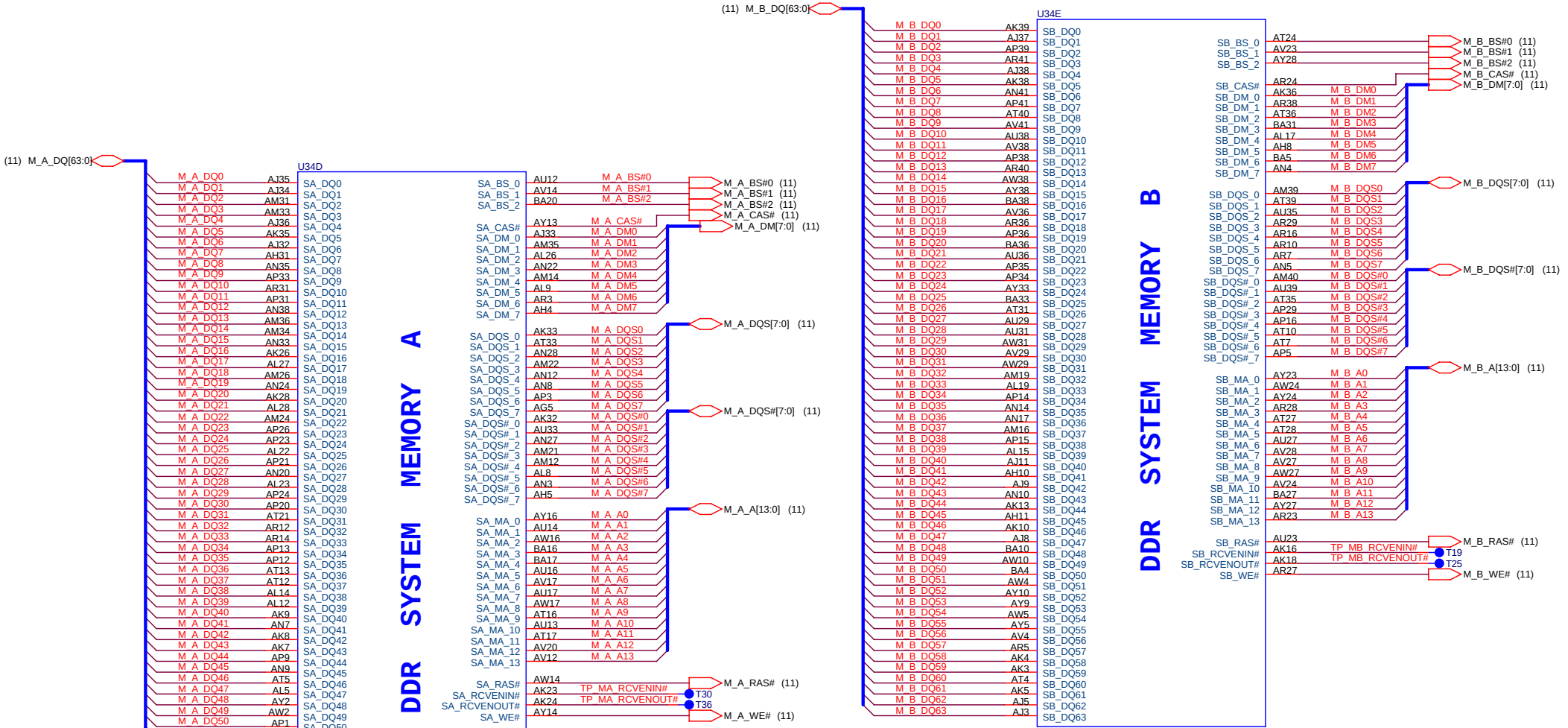
(11) M_A_DQ[63:0]
U34D
DDR SYSTEM MEMORY A
Calistoga
(11) M_B_DQ[63:0]
U34E
DDR SYSTEM MEMORY B
Calistoga
PROJECT : MA7
Quanta Computer Inc.
Size B
Document Number
GMCH DDR(2 OF 6)
Rev 3A
Date: Friday, December 23, 2005
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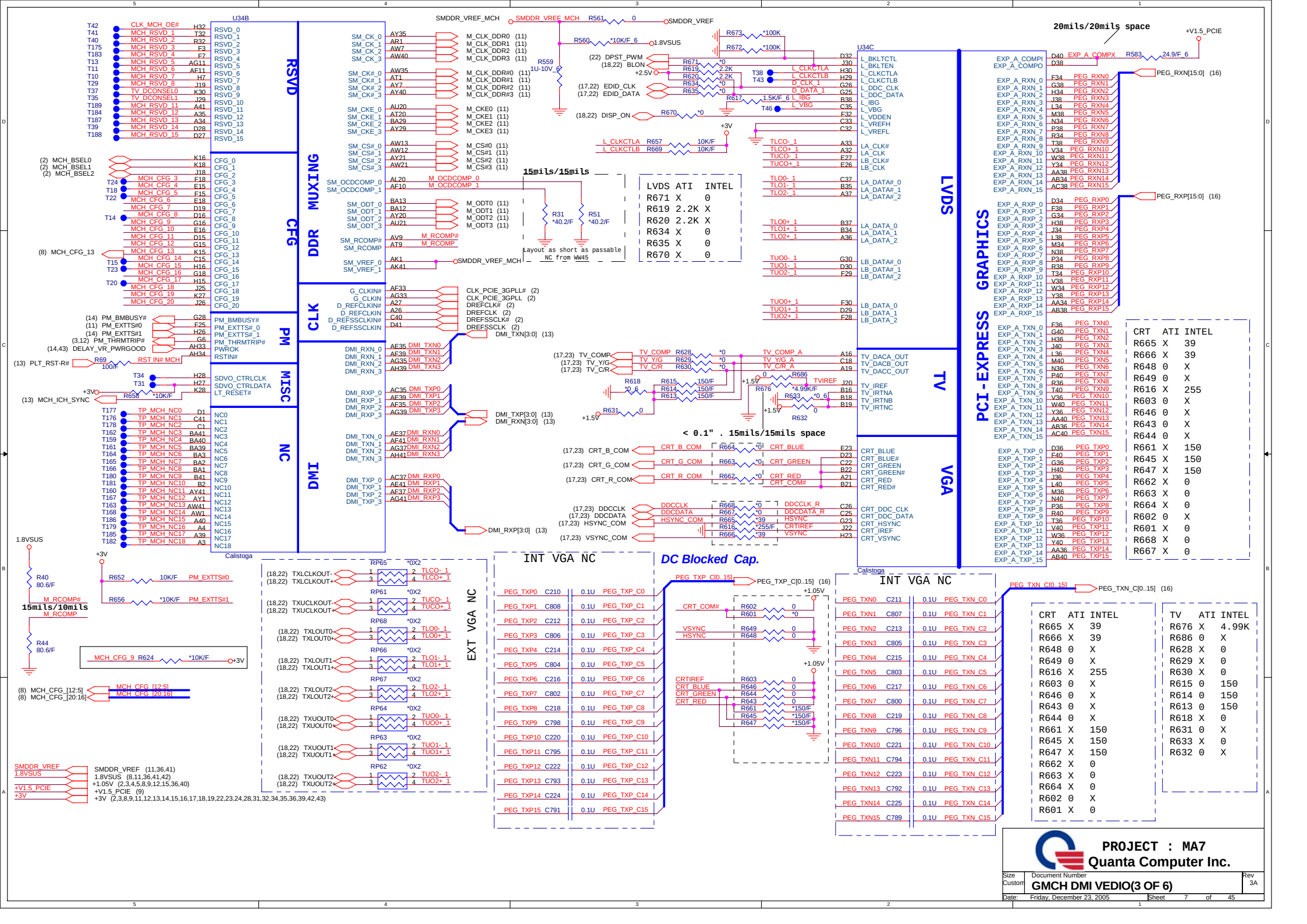
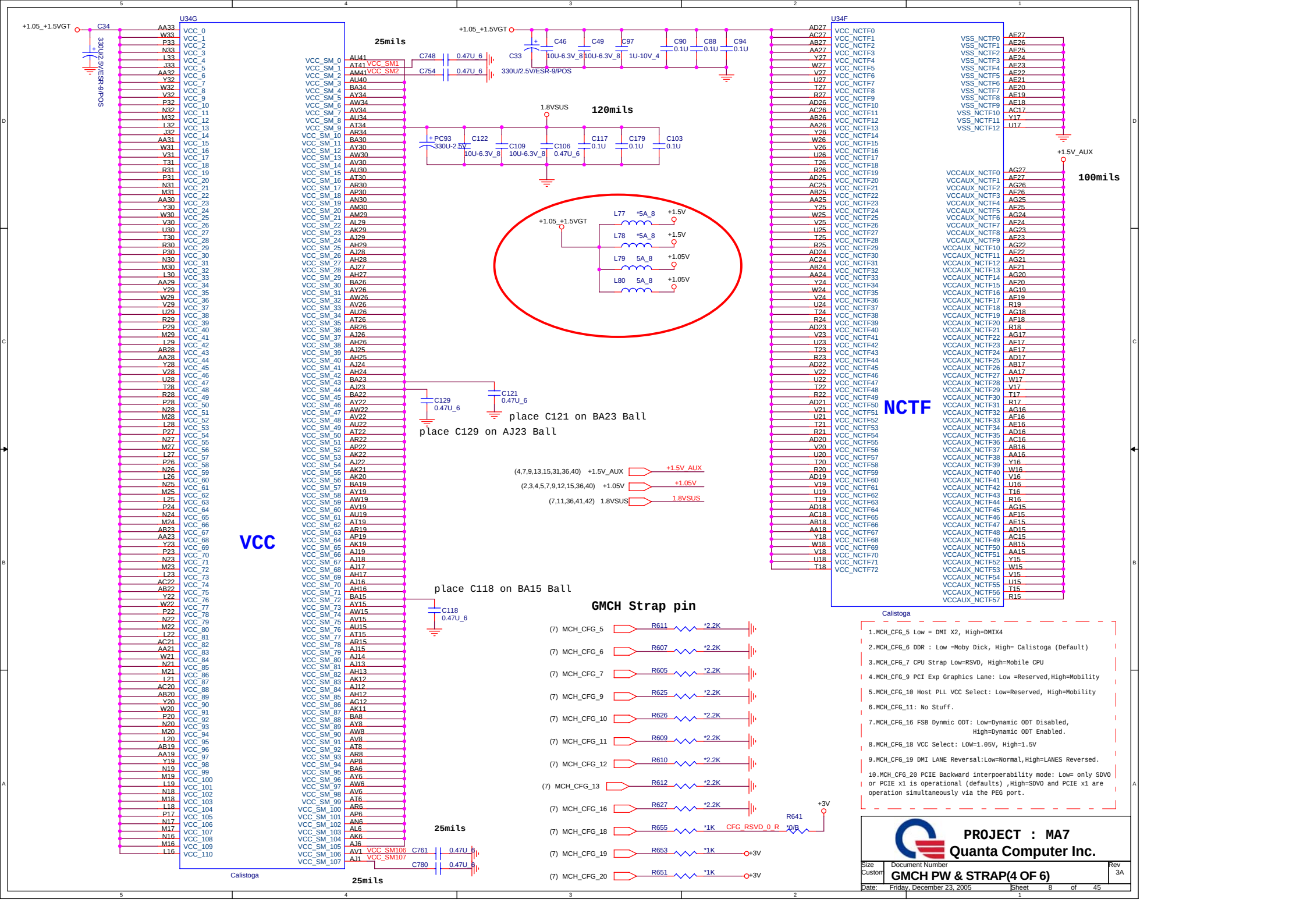

U34B
RSVD
CFG
MUXING
DDR
CLK
PM
MISC
NC
DMI
Calistoga
U34C
LVDS
TV
VGA
PCI-EXPRESS GRAPHICS
20mils/20mils space
15mils/15mils
< 0.1" . 15mils/15mils space
DC Blocked Cap.
INT VGA NC
EXT VGA NC
LVDS ATI INTEL
R671 X 0
R619 2.2K X
R620 2.2K X
R634 X 0
R635 X 0
R670 X 0
CRT ATI INTEL
R665 X 39
R666 X 39
R648 0 X
R649 0 X
R616 X 255
R603 0 X
R646 0 X
R643 0 X
R644 0 X
R661 X 150
R645 X 150
R647 X 150
R662 X 0
R663 X 0
R664 X 0
R602 0 X
R601 X 0
R667 X 0
TV ATI INTEL
R676 X 4.99K
R686 0 X
R628 X 0
R629 X 0
R630 X 255
R615 0 150
R614 0 150
R613 0 150
R618 X 0
R631 0 X
R633 X 0
R632 0 X
PROJECT : MA7
Quanta Computer Inc.
GMCH DMI VEDIO(3 OF 6)
Size Custom
Document Number
Rev 3A
Date: Friday, December 23, 2005
Sheet 7 of 45


U34G
U34F
VCC
NCTF
Calistoga
25mils
120mils
100mils
1.8VSUS
+1.05_+1.5VGT
+1.5V_AUX
330U/2.5V/ESR-9/POS
place C121 on BA23 Ball
place C129 on AJ23 Ball
place C118 on BA15 Ball
GMCH Strap pin
PROJECT : MA7
Quanta Computer Inc.
GMCH PW & STRAP(4 OF 6)
Friday, December 23, 2005
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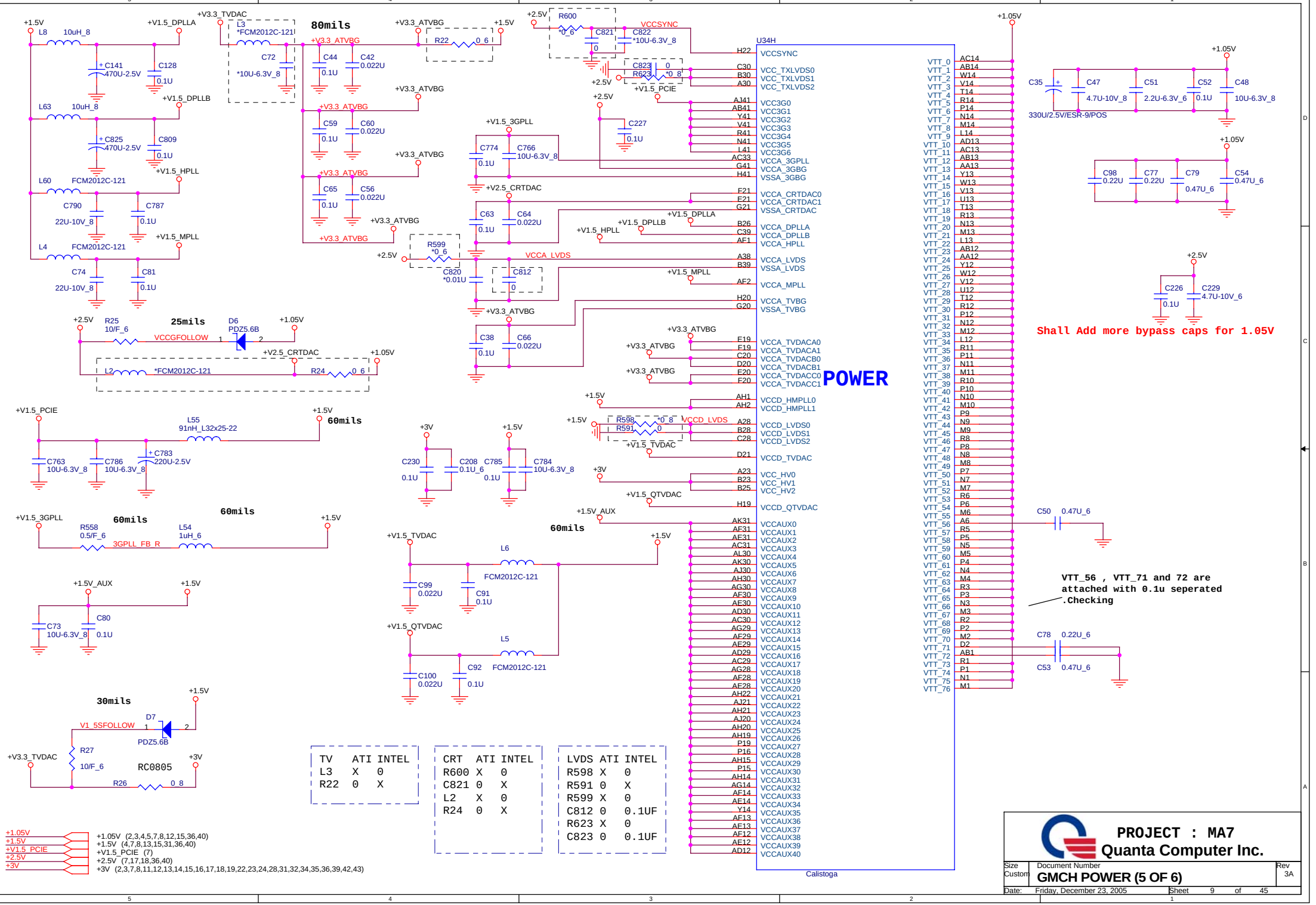
1.MCH_CFG_5 Low = DMI X2, High=DMIX4
2.MCH_CFG_6 DDR : Low =Moby Dick, High= Calistoga (Default)
3.MCH_CFG_7 CPU Strap Low=RSVD, High=Mobile CPU
4.MCH_CFG_9 PCI Exp Graphics Lane: Low =Reserved,High=Mobility
5.MCH_CFG_10 Host PLL VCC Select: Low=Reserved, High=Mobility
6.MCH_CFG_11: No Stuff.
7.MCH_CFG_16 FSB Dynmic ODT: Low=Dynamic ODT Disabled, High=Dynamic ODT Enabled.
8.MCH_CFG_18 VCC Select: LOW=1.05V, High=1.5V
9.MCH_CFG_19 DMI LANE Reversal:Low=Normal,High=LANES Reversed.
10.MCH_CFG_20 PCIE Backward interpoerability mode: Low= only SDVO or PCIE x1 is operational (defaults) ,High=SDVO and PCIE x1 are operation simultaneously via the PEG port.


POWER
U34H
Calistoga
80mils
60mils
25mils
30mils
Shall Add more bypass caps for 1.05V
VTT_56 , VTT_71 and 72 are attached with 0.1u seperated .Checking
TV ATI INTEL
L3 X 0
R22 0 X
CRT ATI INTEL
R600 X 0
C821 0 X
L2 X 0
R24 0 X
LVDS ATI INTEL
R598 X 0
R591 0 X
R599 X 0
C812 0 0.1UF
R623 X 0
C823 0 0.1UF
+1.05V (2,3,4,5,7,8,12,15,36,40)
+1.5V (4,7,8,13,15,31,36,40)
+V1.5_PCIE (7)
+2.5V (7,17,18,36,40)
+3V (2,3,7,8,11,12,13,14,15,16,17,18,19,22,23,24,28,31,32,34,35,36,39,42,43)
PROJECT : MA7
Quanta Computer Inc.
Size Custom
Document Number GMCH POWER (5 OF 6)
Rev 3A
Date: Friday, December 23, 2005
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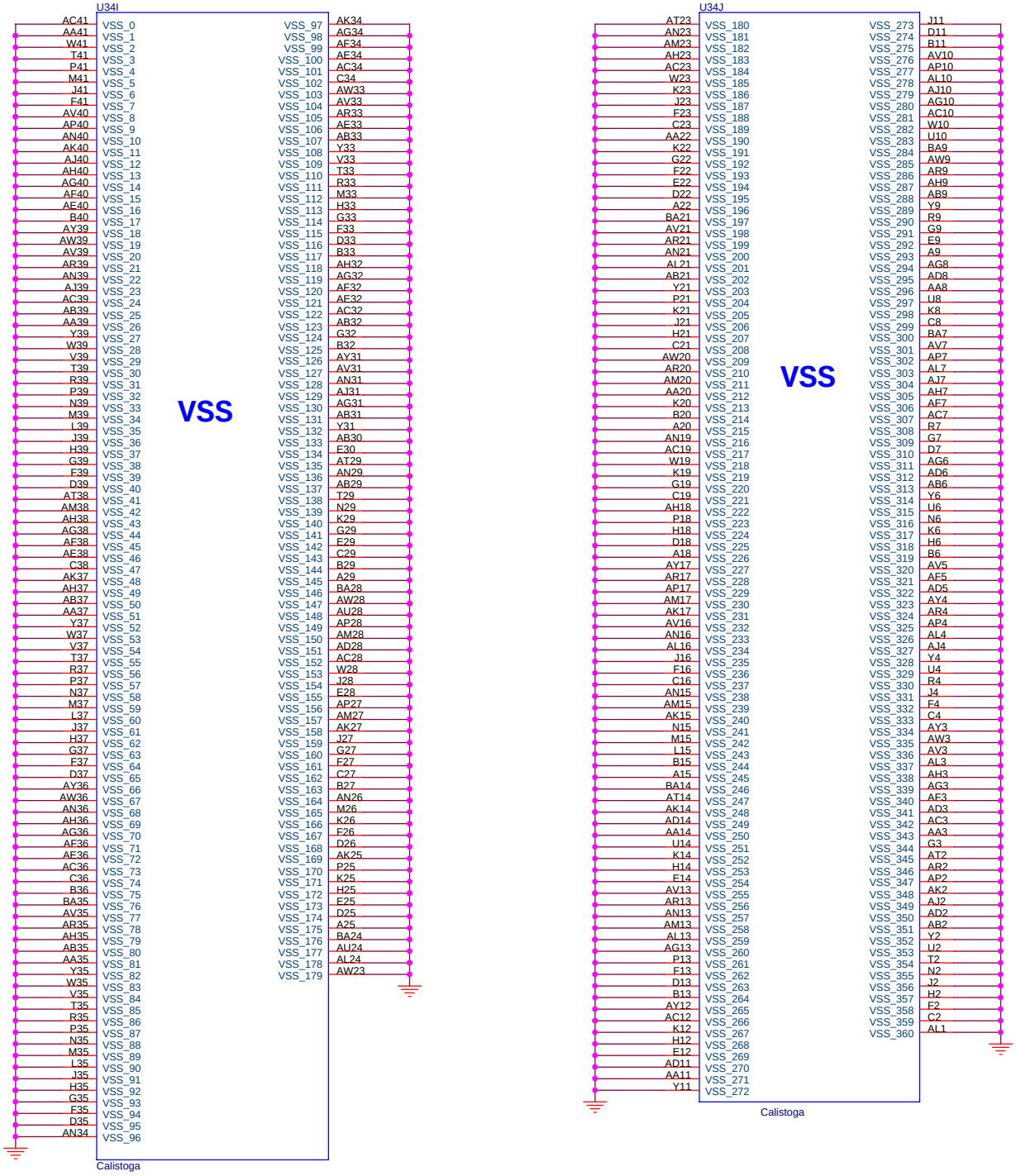


PROJECT : MA7	
Quanta Computer Inc.	
Size: Custom	Document Number: GMCH GND(6 OF 6)
Rev: 3A	
Date: Friday, December 23, 2005	Sheet 10 of 45

M_A_DM[0..7] (6)
M_A_DQ[63:0] (6)
M_A_DQS[7:0] (6)
M_A_DQS#[7:0] (6)
M_A_A[13:0] (6)

1.8VSUS

JDIM2

PC4800 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM	1	VREF	VSS46	2	
M_A_DQ1	3	VSS47	DQ4	4	M_A_DQ4
M_A_DQ5	5	DQ0	DQ5	6	M_A_DQ0
	7	DQ1	VSS15	8	
M_A_DQS#0	9	VSS37	DM0	10	M_A_DM0
M_A_DQS0	11	DQS#0	VSS5	12	
	13	DQS0	DQ6	14	M_A_DQ7
M_A_DQ2	15	VSS48	DQ7	16	M_A_DQ6
M_A_DQ3	17	DQ2	VSS16	18	
	19	DQ3	DQ12	20	M_A_DQ13
M_A_DQ14	21	VSS38	DQ13	22	M_A_DQ12
M_A_DQ8	23	DQ8	VSS17	24	
	25	DQ9	DM1	26	M_A_DM1
M_A_DQS#1	27	VSS49	VSS53	28	
M_A_DQS1	29	DQS#1	CK0	30	M_CLK_DDR0 (7)
	31	DQS1	CK0#	32	M_CLK_DDR#0 (7)
M_A_DQ9	33	VSS39	VSS41	34	
M_A_DQ15	35	DQ10	DQ14	36	M_A_DQ11
	37	DQ11	DQ15	38	M_A_DQ10
	39	VSS50	VSS54	40	
	41			42	
M_A_DQ21	43	VSS18	VSS20	44	M_A_DQ20
M_A_DQ17	45	DQ16	DQ20	46	M_A_DQ16
	47	DQ17	DQ21	48	
M_A_DQS#2	49	VSS1	VSS6	50	PM_EXTTS#0 (7)
M_A_DQS2	51	DQS#2	NC3	52	M_A_DM2
	53	DQS2	DM2	54	
M_A_DQ23	55	VSS19	VSS21	56	M_A_DQ18
M_A_DQ19	57	DQ18	DQ22	58	M_A_DQ22
	59	DQ19	DQ23	60	
M_A_DQ24	61	VSS22	VSS24	62	M_A_DQ28
M_A_DQ25	63	DQ24	DQ28	64	M_A_DQ29
	65	DQ25	DQ29	66	
M_A_DM3	67	VSS23	VSS25	68	M_A_DQS#3
	69	DM3	DQS#3	70	M_A_DQS3
	71	NC4	DQS3	72	
M_A_DQ30	73	VSS9	VSS10	74	M_A_DQ27
M_A_DQ31	75	DQ26	DQ27	76	M_A_DQ26
	77	DQ27	VSS12	78	
M_CKE0	79	VSS4	CKE1	80	M_CKE1 (7)
	81	CKE0	VDD8	82	
	83	VDD7	NC2	84	
M_A_BS#2	85	NC1	A15	86	
	87	A16_BA2	A14	88	
M_A_A12	89	VDD9	VDD11	90	M_A_A11
M_A_A9	91	A12	A11	92	M_A_A7
M_A_A8	93	A9	A7	94	M_A_A6
	95	A8	A6	96	
M_A_A5	97	VDD5	VDD4	98	M_A_A4
M_A_A3	99	A5	A4	100	M_A_A2
M_A_A1	101	A3	A2	102	M_A_A0
	103	A1	A0	104	
M_A_A10	105	VDD10	VDD12	106	M_A_BS#1
M_A_BS#0	107	A10/AP	BA1	108	M_A_RAS#
M_A_WE#	109	BA0	RAS#	110	M_A_CS#0
	111	WE#	S0#	112	
M_A_CAS#	113	VDD2	VDD1	114	M_ODT0
M_CS#1	115	CAS#	ODT0	116	M_A_A13
	117	S1#	A13	118	
M_ODT1	119	VDD3	VDD6	120	
	121	ODT1	NC2	122	
M_A_DQ37	123	VSS11	VSS12	124	M_A_DQ35
M_A_DQ36	125	DQ32	DQ36	126	M_A_DQ32
	127	DQ33	DQ37	128	
M_A_DQS#4	129	VSS26	VSS28	130	M_A_DM4
M_A_DQS4	131	DQS#4	DM4	132	
	133	DQS4	VSS42	134	M_A_DQ33
M_A_DQ39	135	VSS2	DQ38	136	M_A_DQ34
M_A_DQ38	137	DQ34	DQ39	138	
	139	DQ35	VSS55	140	M_A_DQ45
M_A_DQ40	141	VSS27	DQ44	142	M_A_DQ44
M_A_DQ41	143	DQ40	DQ45	144	
	145	DQ41	VSS43	146	M_A_DQS#5
M_A_DM5	147	VSS29	DQS#5	148	M_A_DQS5
	149	DM5	DQS5	150	
M_A_DQ42	151	VSS51	VSS56	152	M_A_DQ46
M_A_DQ43	153	DQ42	DQ46	154	M_A_DQ47
	155	DQ43	DQ47	156	
M_A_DQ53	157	VSS40	VSS44	158	M_A_DQ49
M_A_DQ52	159	DQ48	DQ52	160	M_A_DQ48
	161	DQ49	DQ53	162	
	163	VSS52	VSS57	164	M_CLK_DDR1
	165	NCTEST	CK1	166	M_CLK_DDR#1
M_A_DQS#6	167	VSS30	CK1#	168	
M_A_DQS6	169	DQS#6	VSS45	170	M_A_DM6
	171	DQS6	DM6	172	
M_A_DQ50	173	VSS31	VSS32	174	M_A_DQ54
M_A_DQ51	175	DQ50	DQ54	176	M_A_DQ55
	177	DQ51	DQ55	178	
M_A_DQ56	179	VSS33	VSS35	180	M_A_DQ57
M_A_DQ60	181	DQ56	DQ60	182	M_A_DQ61
	183	DQ57	DQ61	184	
M_A_DM7	185	VSS3	VSS7	186	M_A_DQS#7
	187	DM7	DQS7	188	M_A_DQS7
M_A_DQ62	189	VSS34	VSS36	190	
M_A_DQ58	191	DQ58	DQ62	192	M_A_DQ59
	193	DQ59	DQ63	194	M_A_DQ63
CGDAT_SMB	195	VSS14	VSS13	196	
CGCLK_SMB	197	SDA	SA0	198	
	199	SCL	SA1	200	
		VDD(SPD)			

PC4800 DDR2

+3V

M_CKE0 (7) M_CKE1 (7)
M_A_BS#2 (6)
M_A_BS#0 (6) M_A_BS#1 (6)
M_A_WE# (6) M_A_RAS# (6)
M_A_CAS# (6) M_CS#0 (7)
M_CS#1 (7)
M_ODT0 (7)
M_ODT1 (7)

R36 10K_6 R38 10K_6

SMDDR_VREF_DIMM R182 0 SMDDR_VREF (7,36,41)
R199 *10K/F_6 R200 *10K/F_6 1.8VSUS

CLOCK 0,1
CKE 0,1
(Channel A)
SMbus address A0
High=9.2mm

SMDDR_VTERM
C201 0.1U C143 0.1U C180 0.1U C131 0.1U C149 0.1U C169 0.1U C200 0.1U C187 0.1U C195 0.1U C139 0.1U C157 0.1U C133 0.1U C188 0.1U

Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

M_B_DM[0..7] (6)
M_B_DQ[63:0] (6)
M_B_DQS[7:0] (6)
M_B_DQS#[7:0] (6)
M_B_A[13:0] (6)

1.8VSUS

JDIM1

PC4800 DDR2 SDRAM SO-DIMM (200P)

SMDDR_VREF_DIMM	1	VREF	VSS46	2	
M_B_DQ1	3	VSS47	DQ4	4	M_B_DQ4
M_B_DQ5	5	DQ0	DQ5	6	M_B_DQ0
	7	DQ1	VSS15	8	
M_B_DQS#0	9	VSS37	DM0	10	M_B_DM0
M_B_DQS0	11	DQS#0	VSS5	12	
	13	DQS0	DQ6	14	M_B_DQ7
M_B_DQ2	15	VSS48	DQ7	16	M_B_DQ6
M_B_DQ3	17	DQ2	VSS16	18	
	19	DQ3	DQ12	20	M_B_DQ12
M_B_DQ8	21	VSS38	DQ13	22	M_B_DQ13
M_B_DQ9	23	DQ8	VSS17	24	
	25	DQ9	DM1	26	M_B_DM1
M_B_DQS#1	27	VSS49	VSS53	28	
M_B_DQS1	29	DQS#1	CK0	30	M_CLK_DDR3 (7)
	31	DQS1	CK0#	32	M_CLK_DDR#3 (7)
M_B_DQ10	33	VSS39	VSS41	34	
M_B_DQ11	35	DQ10	DQ14	36	M_B_DQ15
	37	DQ11	DQ15	38	M_B_DQ14
	39	VSS50	VSS54	40	
	41			42	
M_B_DQ17	43	VSS18	VSS20	44	M_B_DQ16
M_B_DQ20	45	DQ16	DQ20	46	M_B_DQ21
	47	DQ17	DQ21	48	
M_B_DQS#2	49	VSS1	VSS6	50	PM_EXTTS#0 (7)
M_B_DQS2	51	DQS#2	NC3	52	M_B_DM2
	53	DQS2	DM2	54	
M_B_DQ19	55	VSS19	VSS21	56	M_B_DQ18
M_B_DQ23	57	DQ18	DQ22	58	M_B_DQ22
	59	DQ19	DQ23	60	
M_B_DQ28	61	VSS22	VSS24	62	M_B_DQ24
M_B_DQ29	63	DQ24	DQ28	64	M_B_DQ25
	65	DQ25	DQ29	66	
M_B_DM3	67	VSS23	VSS25	68	M_B_DQS#3
	69	DM3	DQS#3	70	M_B_DQS3
	71	NC4	DQS3	72	
M_B_DQ30	73	VSS9	VSS10	74	M_B_DQ26
M_B_DQ31	75	DQ26	DQ27	76	M_B_DQ27
	77	DQ27	VSS12	78	
M_CKE2	79	VSS4	CKE1	80	M_CKE3 (7)
	81	CKE0	VDD8	82	
	83	VDD7	NC2	84	
M_B_BS#2	85	NC1	A15	86	
	87	A16_BA2	A14	88	
M_B_A12	89	VDD9	VDD11	90	M_B_A11
M_B_A9	91	A12	A11	92	M_B_A7
M_B_A8	93	A9	A7	94	M_B_A6
	95	A8	A6	96	
M_B_A5	97	VDD5	VDD4	98	M_B_A4
M_B_A3	99	A5	A4	100	M_B_A2
M_B_A1	101	A3	A2	102	M_B_A0
	103	A1	A0	104	
M_B_A10	105	VDD10	VDD12	106	M_B_BS#1
M_B_BS#0	107	A10/AP	BA1	108	M_B_RAS#
M_B_WE#	109	BA0	RAS#	110	M_CS#2
	111	WE#	S0#	112	
M_B_CAS#	113	VDD2	VDD1	114	M_ODT2
M_CS#3	115	CAS#	ODT0	116	M_B_A13
	117	S1#	A13	118	
M_ODT3	119	VDD3	VDD6	120	
	121	ODT1	NC2	122	
M_B_DQ37	123	VSS11	VSS12	124	M_B_DQ33
M_B_DQ36	125	DQ32	DQ36	126	M_B_DQ32
	127	DQ33	DQ37	128	
M_B_DQS#4	129	VSS26	VSS28	130	M_B_DM4
M_B_DQS4	131	DQS#4	DM4	132	
	133	DQS4	VSS42	134	M_B_DQ34
M_B_DQ39	135	VSS2	DQ38	136	M_B_DQ38
M_B_DQ35	137	DQ34	DQ39	138	
	139	DQ35	VSS55	140	M_B_DQ45
M_B_DQ40	141	VSS27	DQ44	142	M_B_DQ44
M_B_DQ41	143	DQ40	DQ45	144	
	145	DQ41	VSS43	146	M_B_DQS#5
M_B_DM5	147	VSS29	DQS#5	148	M_B_DQS5
	149	DM5	DQS5	150	
M_B_DQ47	151	VSS51	VSS56	152	M_B_DQ46
M_B_DQ42	153	DQ42	DQ46	154	M_B_DQ43
	155	DQ43	DQ47	156	
M_B_DQ49	157	VSS40	VSS44	158	M_B_DQ52
M_B_DQ53	159	DQ48	DQ52	160	M_B_DQ48
	161	DQ49	DQ53	162	
	163	VSS52	VSS57	164	M_CLK_DDR2
	165	NCTEST	CK1	166	M_CLK_DDR#2
M_B_DQS#6	167	VSS30	CK1#	168	
M_B_DQS6	169	DQS#6	VSS45	170	M_B_DM6
	171	DQS6	DM6	172	
M_B_DQ55	173	VSS31	VSS32	174	M_B_DQ51
M_B_DQ50	175	DQ50	DQ54	176	M_B_DQ54
	177	DQ51	DQ55	178	
M_B_DQ61	179	VSS33	VSS35	180	M_B_DQ56
M_B_DQ57	181	DQ56	DQ60	182	M_B_DQ60
	183	DQ57	DQ61	184	
M_B_DM7	185	VSS3	VSS7	186	M_B_DQS#7
	187	DM7	DQS7	188	M_B_DQS7
M_B_DQ63	189	VSS34	VSS36	190	
M_B_DQ58	191	DQ58	DQ62	192	M_B_DQ59
	193	DQ59	DQ63	194	M_B_DQ62
CGDAT_SMB	195	VSS14	VSS13	196	
CGCLK_SMB	197	SDA	SA0	198	
	199	SCL	SA1	200	
		VDD(SPD)			

PC4800 DDR2

(2,31) CGDAT_SMB
(2,31) CGCLK_SMB
+3V

M_CKE2 (7) M_CKE3 (7)
M_B_BS#2 (6)
M_B_BS#0 (6) M_B_BS#1 (6)
M_B_WE# (6) M_B_RAS# (6)
M_B_CAS# (6) M_CS#2 (7)
M_CS#3 (7)
M_ODT2 (7)
M_ODT3 (7)

R37 10K_6 R39 10K_6

CLOCK 3,4
CKE 2,3
(Channel B)
SMbus address A1
High=5.2mm

SMDDR_VTERM
C134 0.1U C175 0.1U C189 0.1U C159 0.1U C152 0.1U C167 0.1U C138 0.1U C168 0.1U C148 0.1U C194 0.1U C181 0.1U C177 0.1U C136 0.1U

Place these Caps near So-Dimm1.
C154 0.1U C137 0.1U C144 0.1U C142 0.1U
C706 2.2U-6.3V_6 C704 2.2U-6.3V_6 C709 2.2U-6.3V_6 C707 2.2U-6.3V_6 C705 2.2U-6.3V_6 C708 2.2U-6.3V_6

Place these Caps near So-Dimm2.
C178 0.1U C172 0.1U C146 0.1U C160 0.1U
C158 2.2U-6.3V_6 C151 2.2U-6.3V_6 C688 2.2U-6.3V_6 C687 2.2U-6.3V_6 C145 2.2U-6.3V_6 C135 2.2U-6.3V_6

+3V
C93 2.2U-6.3V_6 C102 0.1U
C694 2.2U-6.3V_6 C691 0.1U

SMDDR_VREF_DIMM
C346 2.2U-6.3V_6 C339 0.1U
C344 2.2U-6.3V_6 C330 0.1U

M_ODT0
M_A_RAS# RP6 56X2
M_A_A8 RP17 56X2
M_A_A5 RP15 56X2
M_A_A3 SMDDR_VTERM
M_A_A1

M_A_A7
M_CKE1 RP28 56X2
M_A_A10 RP11 56X2
M_A_BS#0 RP19 56X2
M_A_A4 RP13 56X2
M_A_A11 SMDDR_VTERM
M_A_A2
M_A_A6

M_A_A0
M_A_BS#1 RP9 56X2
M_A_A12 RP21 56X2
M_A_A9 RP7 56X2
M_A_WE# SMDDR_VTERM
M_A_CAS#

M_B_BS#1
M_B_A0 RP12 56X2
M_B_A3 RP14 56X2
M_B_A1 RP16 56X2
M_B_A8 SMDDR_VTERM
M_B_A5

M_B_A4
M_B_A2 RP18 56X2
M_B_A12 RP20 56X2
M_B_A9 RP27 56X2
M_B_A7 RP26 56X2
M_B_A11 SMDDR_VTERM
M_B_BS#2
M_CKE2

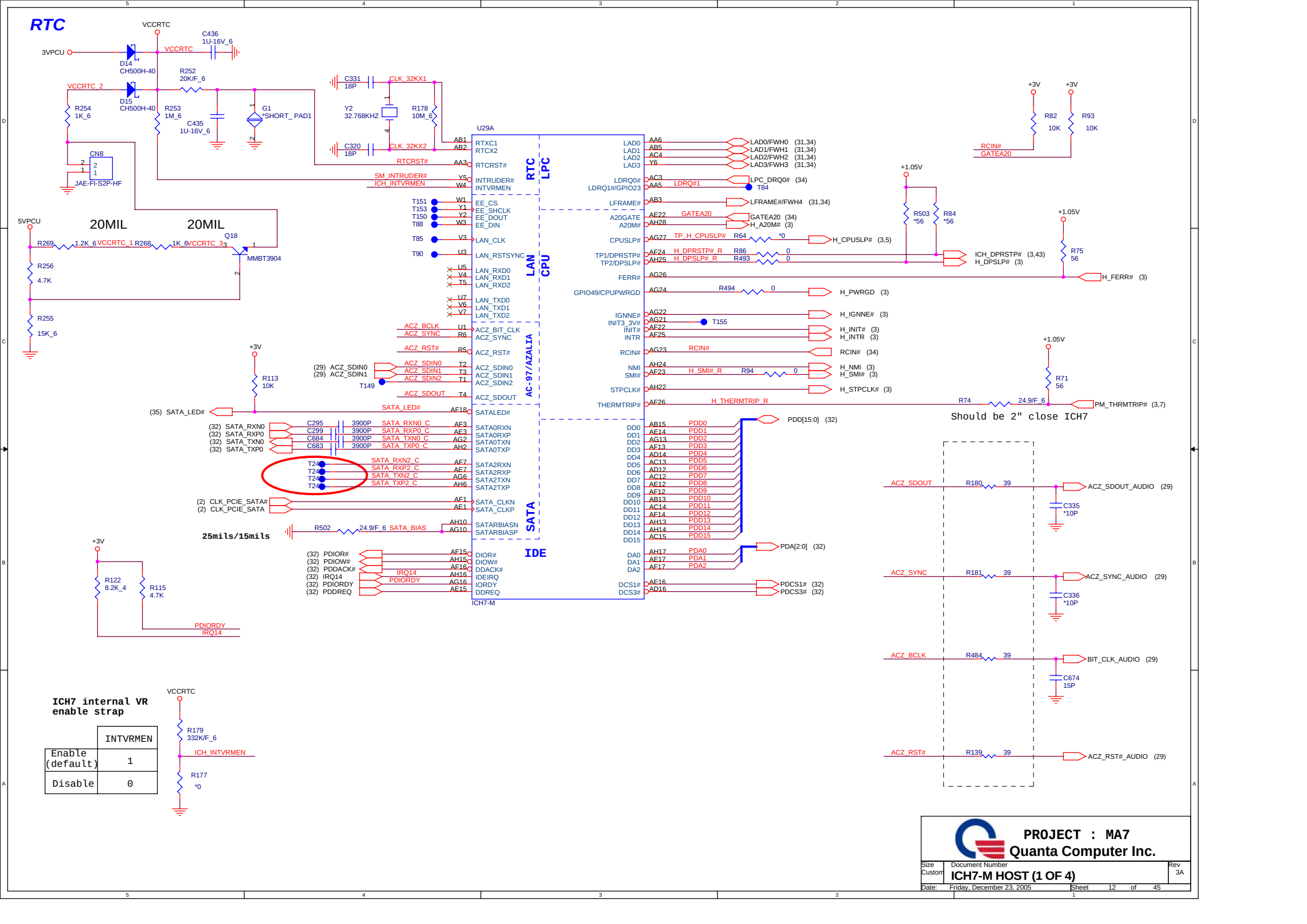
M_B_A13
M_B_RAS# RP8 56X2
M_B_CAS# RP4 56X2
M_B_WE# RP10 56X2
M_B_BS#0 SMDDR_VTERM
M_A_A10

M_A_A13
M_CS#0 RP3 56X2
M_CS#2 RP5 56X2
M_ODT2 RP1 56X2
M_CS#3 RP2 56X2
M_ODT3 SMDDR_VTERM
M_CS#1
M_ODT1
M_B_A6
M_CKE3 RP29 56X2
M_CKE0 RP30 56X2
M_A_BS#2 SMDDR_VTERM

(2,3,7,8,9,12,13,14,15,16,17,18,19,22,23,24,28,31,32,34,35,36,39,42,43) +3V
(7,8,36,41,42) 1.8VSUS
(36,41) SMDDR_VTERM
(7,36,41) SMDDR_VREF

+3V
R703 *0
U5
C123 *0.1U
(3,17) THDAT_SMB
(3,17) THCLK_SMB
R43 *0
R50 *0
(2,31) CGDAT_SMB
(2,31) CGCLK_SMB
R41 *0
R42 *0
A0
A1
A2
SDA
SCL
+VS
O.S
GND
*LM75CIMM3

Quanta Computer Inc.	PROJECT : MA7		
Size: Custom	Document Number: DDR II SODIMM		Rev: 3A
Date: Friday, December 23, 2005	Sheet 11 of 45		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VCCRTC
3VPCU
C436
1U-16V_6
D14
CH500H-40
R252
20K/F_6
VCCRTC_2
D15
CH500H-40
R254
1K_6
R253
1M_6
C435
1U-16V_6
G1
*SHORT_ PAD1
CN8
JAE-FI-S2P-HF
C331
18P
CLK_32KX1
Y2
32.768KHZ
R178
10M_6
C320
18P
CLK_32KX2
RTCRST#
SM_INTRUDER#
ICH_INTVRMEN
U29A
RTXC1
RTXC2
RTCRST#
INTRUDER#
INTVRMEN
RTC
LPC
EE_CS
EE_SHCLK
EE_DOUT
EE_DIN
LAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
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CPU
ACZ_BCLK
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ACZ_SDIN2
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ACZ_BIT_CLK
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ACZ_RST#
ACZ_SDIN0
ACZ_SDIN1
ACZ_SDIN2
ACZ_SDOUT
AC-97/AZALIA
SATA_LED#
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
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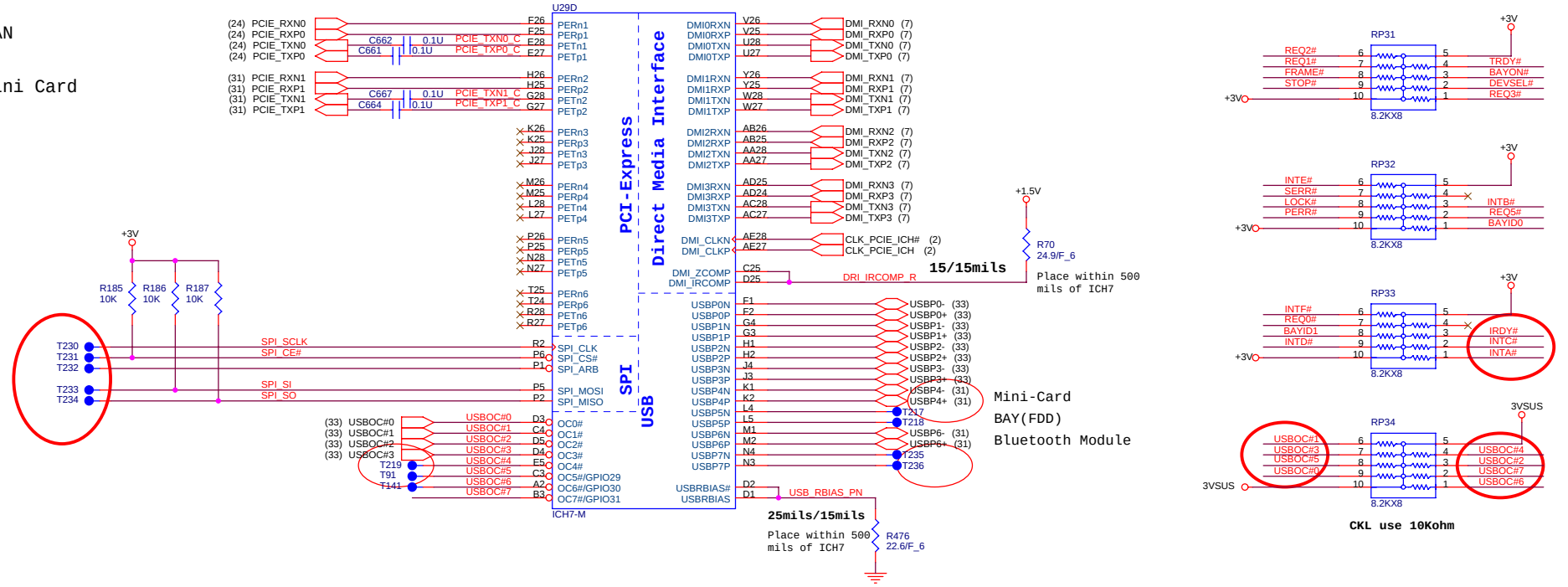
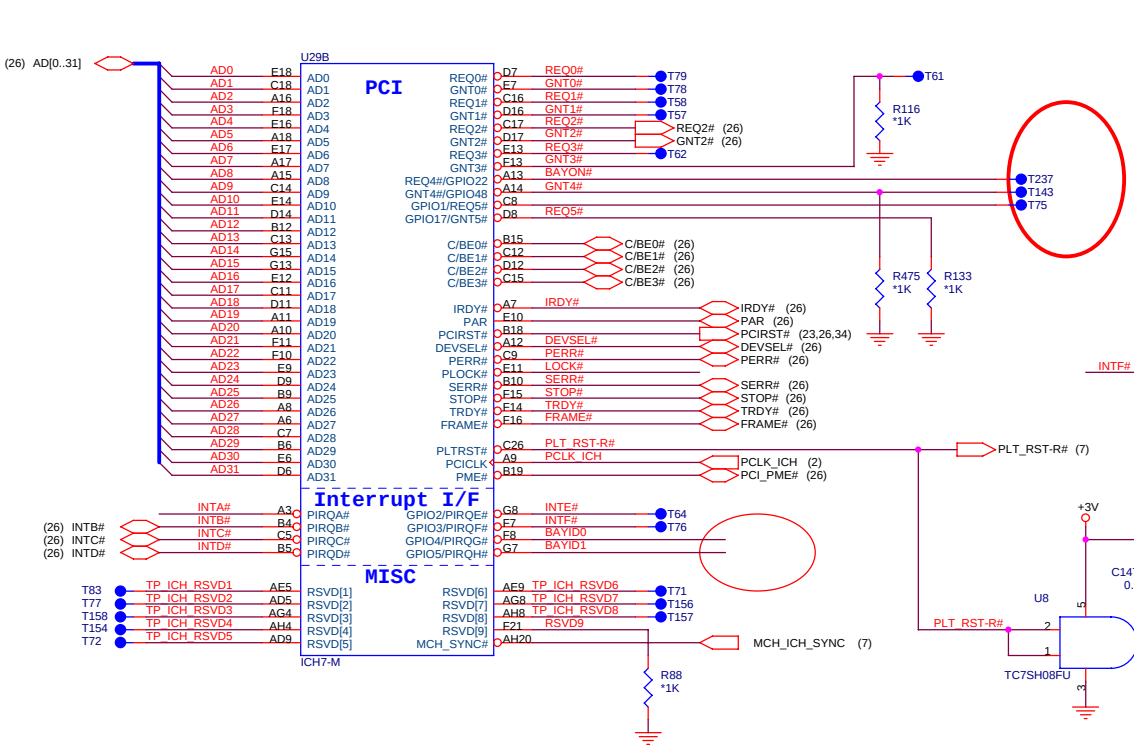
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIASN
SATARBIASP
SATA
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
IDE
ICH7-M
LAD0
LAD1
LAD2
LAD3
LDRQ0#
LDRQ1#/GPIO23
LFRAME#
A20GATE
A20M#
CPUSLP#
TP1/DPRSTP#
TP2/DPSLP#
FERR#
GPIO49/CPUPWRGD
IGNNE#
INIT3_3V#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THERMTRIP#
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
LAD0/FWH0 (31,34)
LAD1/FWH1 (31,34)
LAD2/FWH2 (31,34)
LAD3/FWH3 (31,34)
LPC_DRQ0# (34)
LDRQ#1
LFRAME#/FWH4 (31,34)
GATEA20 (34)
H_A20M# (3)
H_CPUSLP# (3,5)
ICH_DPRSTP# (3,43)
H_DPSLP# (3)
H_FERR# (3)
H_PWRGD (3)
H_IGNNE# (3)
H_INIT# (3)
H_INTR (3)
RCIN# (34)
H_NMI (3)
H_SMI# (3)
H_STPCLK# (3)
PM_THRMTRIP# (3,7)
PDD[15:0] (32)
PDA[2:0] (32)
PDCS1# (32)
PDCS3# (32)
+3V
+1.05V
R82
10K
R93
10K
R503
*56
R84
*56
R75
56
R71
56
R74
24.9/F_6
Should be 2" close ICH7
5VPCU
20MIL
20MIL
Q18
MMBT3904
R269
1.2K_6
VCCRTC_1
R268
1K_6
VCCRTC_3
R256
4.7K
R255
15K_6
R113
10K
(35) SATA_LED#
(32) SATA_RXN0
(32) SATA_RXP0
(32) SATA_TXN0
(32) SATA_TXP0
C295
C299
C684
C683
3900P
SATA_RXN0_C
SATA_RXP0_C
SATA_TXN0_C
SATA_TXP0_C
SATA_RXN2_C
SATA_RXP2_C
SATA_TXN2_C
SATA_TXP2_C
(2) CLK_PCIE_SATA#
(2) CLK_PCIE_SATA
R502
24.9/F_6
SATA_BIAS
25mils/15mils
R122
8.2K_4
R115
4.7K
PDIORDY
IRQ14
(32) PDIOR#
(32) PDIOW#
(32) PDDACK#
(32) IRQ14
(32) PDIORDY
(32) PDDREQ
ACZ_SDOUT
R180
39
ACZ_SDOUT_AUDIO (29)
C335
*10P
ACZ_SYNC
R181
ACZ_SYNC_AUDIO (29)
C336
*10P
ACZ_BCLK
R484
BIT_CLK_AUDIO (29)
C674
15P
ACZ_RST#
R139
ACZ_RST#_AUDIO (29)
ICH7 internal VR enable strap
INTVRMEN
Enable (default) 1
Disable 0
R179
332K/F_6
R177
*0
PROJECT : MA7
Quanta Computer Inc.
Size Custom
Document Number
ICH7-M HOST (1 OF 4)
Rev 3A
Date: Friday, December 23, 2005
Sheet 12 of 45

Tekoa LAN

PCI-E Mini Card





ICH7 Boot BIOS select

	STRAP	GNT5# R1	GNT4# R2
LPC (default)	11	UNSTUFF	UNSTUFF
PCI	10	UNSTUFF	STUFF
SPI	01	STUFF	UNSTUFF

PCI DEVICE	IDSEL#	REQ# / GNT#	Interrupts
PCI7412	AD25	REQ2# / GNT2#	INT B/C/D#

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ICH7-M PCI E (2 OF 4)	3A

Date: Friday, December 23, 2005 Sheet 13 of 45

R473
No stuff-->boot
Stuff-->No boot

to Clock Gen & DIMM

U29C

SMB
SATA GPIO
Clocks
SYS GPIO
Power MGT
GPIO

ICH7-M

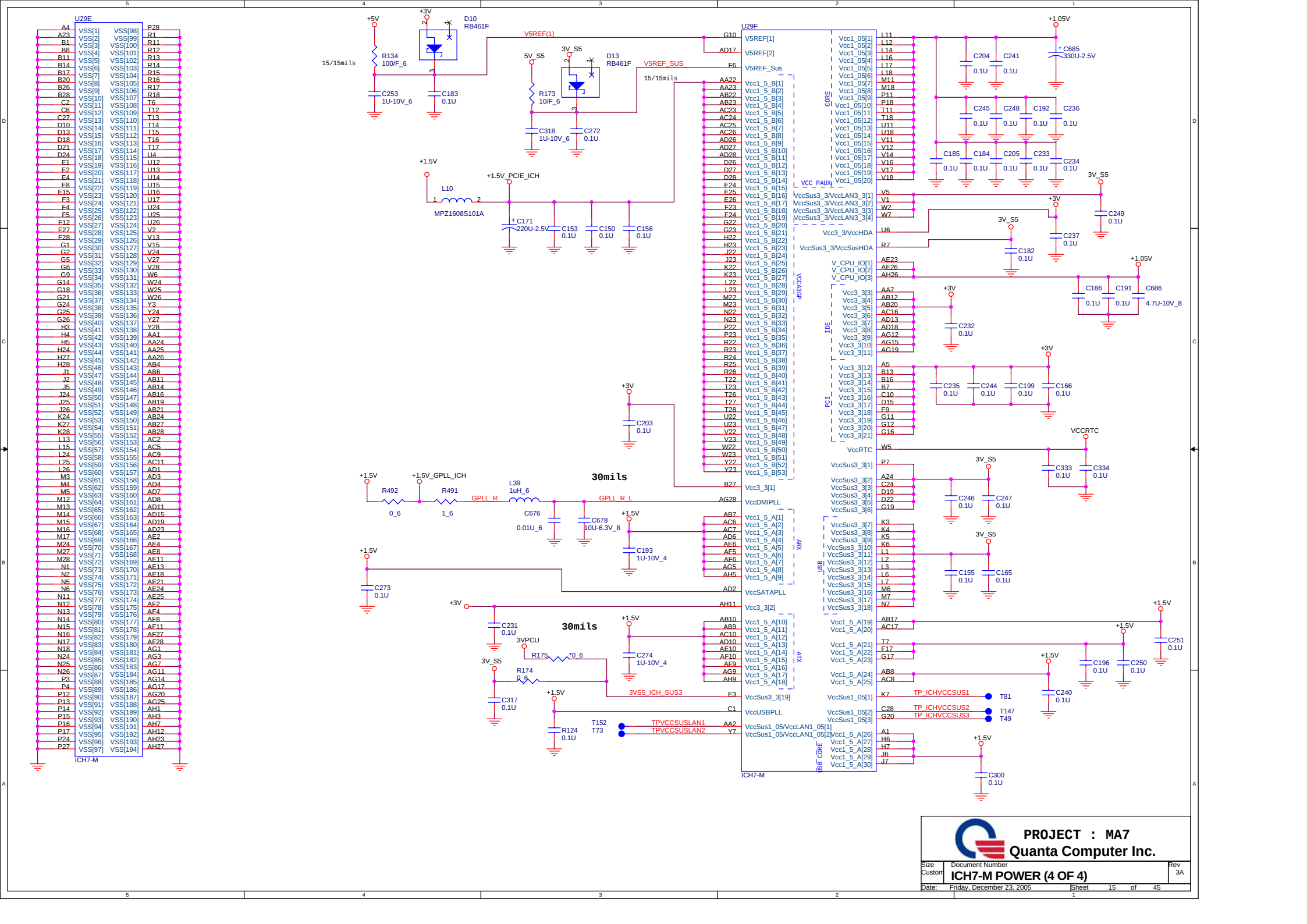
GPI025 /Suspend rail is a HW strap", don't pull down .

Board ID	ID:0	ID0:1
ID1:0		
ID1:1		

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
B	ICH7-M GPIO (3 OF 4)	3A

Date: Friday, December 23, 2005 Sheet 14 of 45


U29E
ICH7-M
U29F
ICH7-M
D10
RB461F
D13
RB461F
V5REF(1)
V5REF_SUS
15/15mils
R134
100/F_6
C253
1U-10V_6
C183
0.1U
R173
10/F_6
C318
1U-10V_6
C272
0.1U
L10
MPZ1608S101A
C171
220U-2.5V
C153
0.1U
C150
0.1U
C156
0.1U
C203
0.1U
30mils
R492
0_6
R491
1_6
L39
1uH_6
C676
0.01U_6
C678
10U-6.3V_8
C193
1U-10V_4
C273
0.1U
C231
0.1U
3VPCU
R175
*0_6
R174
0_6
C317
0.1U
C274
1U-10V_4
3VS5_ICH_SUS3
R124
0.1U
T152
T73
TPVCCSUSLAN1
TPVCCSUSLAN2
C204
C241
C685
330U-2.5V
C245
C248
C192
C236
C185
C184
C205
C233
C234
C249
C237
C182
C232
C186
C191
C686
4.7U-10V_8
C235
C244
C199
C166
C333
C334
C246
C247
C155
C165
C196
C250
C251
C240
C300
TP_ICHVCCSUS1
TP_ICHVCCSUS2
TP_ICHVCCSUS3
T81
T147
T49
PROJECT : MA7
Quanta Computer Inc.
ICH7-M POWER (4 OF 4)
Size Custom
Document Number
Rev 3A
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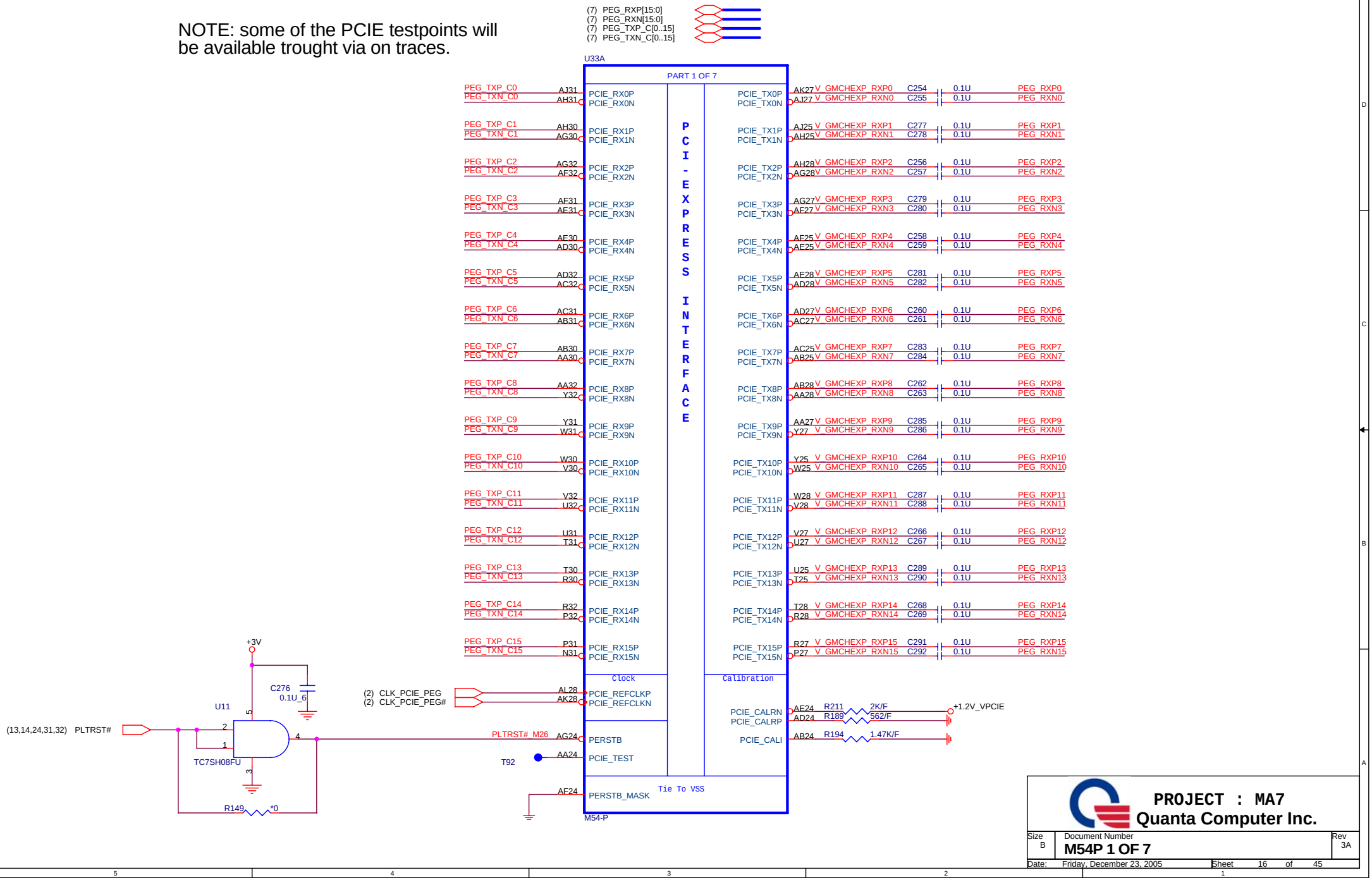
NOTE: some of the PCIE testpoints will be available trought via on traces.



PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
B	M54P 1 OF 7	3A

Date: Friday, December 23, 2005 Sheet 16 of 45

MEMORY CLOCK SPREAD SPECTRUM

U10
CY25819
MK1726-8

CRT

TV_OUT

Memory ID

Thermal Sensor

U38
G781-1P8
ADDRESS: 9AH

10 mil trace /
10 mil space

PLACE CLOSE TO ASIC

DVPDATA_[23:20]	Memory Chanel	Vendor	Part No	Package organized
0000			Reserved	
0001	A	Samsung	K4J55323QG-BC20 256M(8Mx32) GDDR3-136P	64M memory aperture
0010	B	Samsung	K4J55323QG-BC20 256M(8Mx32) GDDR3-136P	64M memory aperture
0011	A& B	Samsung	K4J55323QG-BC20 256M(8Mx32) GDDR3-136P	128M memory aperture
0100	A	Hynix	HY5RS573225AFP-2 256M(8Mx32) GDDR3-136P	64M memory aperture
0101	B	Hynix	HY5RS573225AFP-2 256M(8Mx32) GDDR3-136P	64M memory aperture
0110	A& B	Hynix	HY5RS573225AFP-2 256M(8Mx32) GDDR3-136P	128M memory aperture
0111	A	Infineon	HYB18H256321AF-12 256M(8Mx32)GDDR3-136P	64M memory aperture
1000	B	Infineon	HYB18H256321AF-12 256M(8Mx32)GDDR3-136P	64M memory aperture
1001	A& B	Infineon	HYB18H256321AF-12 256M(8Mx32)GDDR3-136P	128M memory aperture
1010			Reserved	
1011			Reserved	
1100			Reserved	
1101	A	Infineon	HYB18H512321AFL-20 512M(16Mx32)GDDR3-136P	128M memory aperture
1110	B	Infineon	HYB18H512321AFL-20 512M(16Mx32)GDDR3-136P	128M memory aperture
1111	A& B	Infineon	HYB18H512321AFL-20 512M(16Mx32)GDDR3-136P	256M memory aperture

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
C	M54P 2 OF 7	3A

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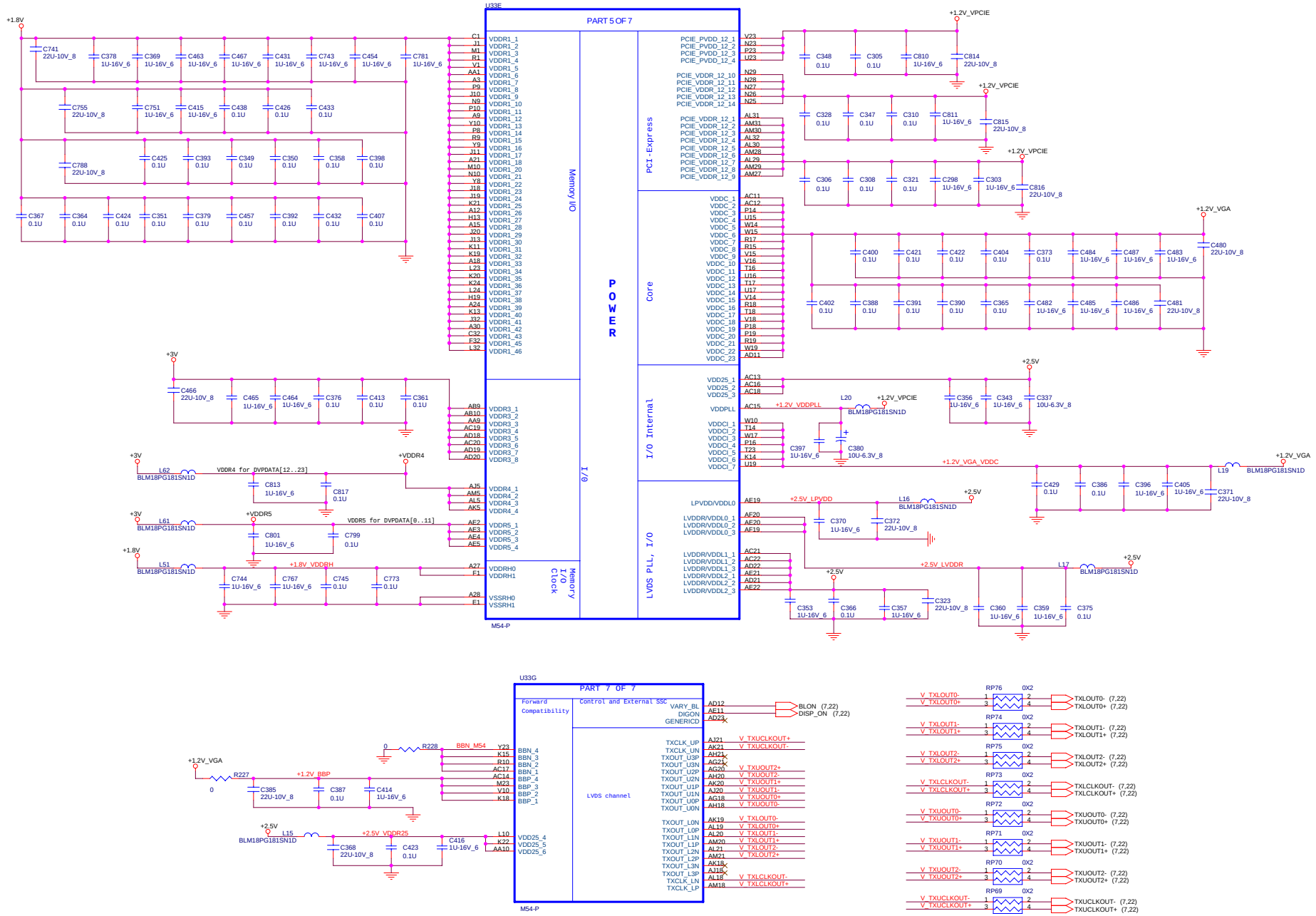
U33E
PART 5 OF 7
POWER
Memory I/O
I/O
Core
I/O Internal
PCI-Express
LVDS PLL, I/O
Memory I/O Clock
M54-P
+1.8V
+3V
+1.2V_VPCIE
+1.2V_VGA
+2.5V
+VDDR4
+VDDR5
+1.2V_VDDPLL
+1.2V_VGA_VDDC
+2.5V_LPVDD
+1.8V_VDDRH
+2.5V_VDDR25
+2.5V_LVDDR
VDDR4 for DVPDATA[12..23]
VDDR5 for DVPDATA[0..11]
BLM18PG181SN1D
U33G
PART 7 OF 7
Forward Compatibility
Control and External SSC
LVDS channel
BLON (7,22)
DISP_ON (7,22)
RP76 0X2
RP74 0X2
RP75 0X2
RP73 0X2
RP72 0X2
RP71 0X2
RP70 0X2
RP69 0X2
PROJECT : MA7
Quanta Computer Inc.
M54P POWER
Size C
Document Number
Rev 3A
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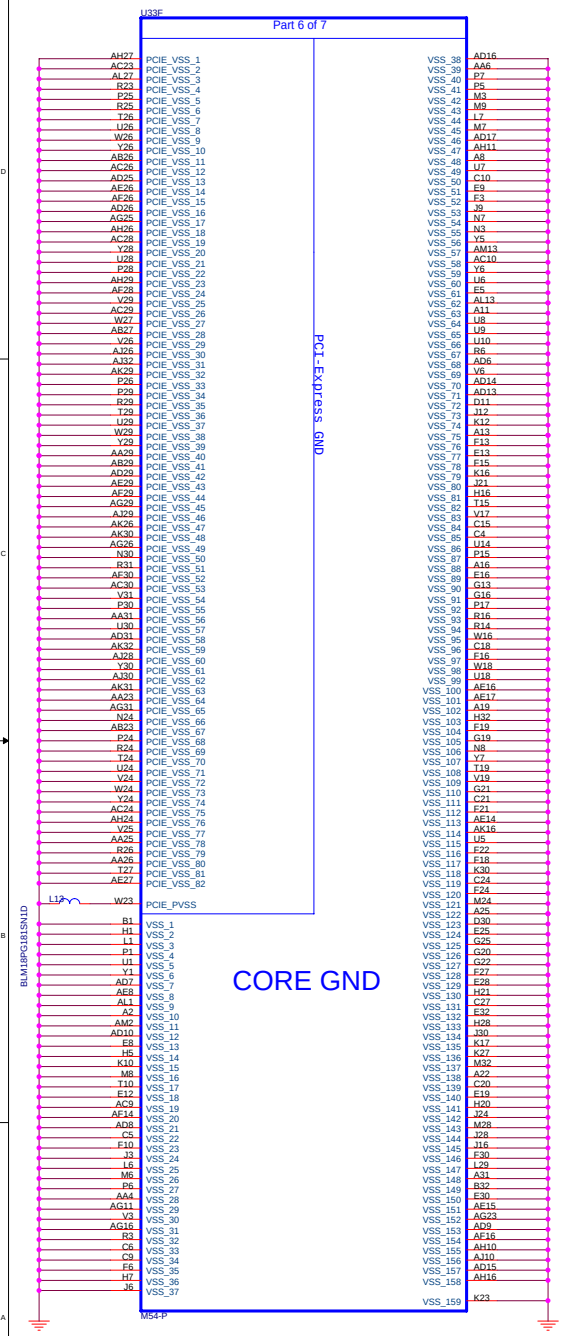
Sheet 18 of 45

LCDDATA(15,19)



(17) GPIO[13..0]

GPIO[13..0]

Overlap pads to save space and to prevent assembly of both resistors.

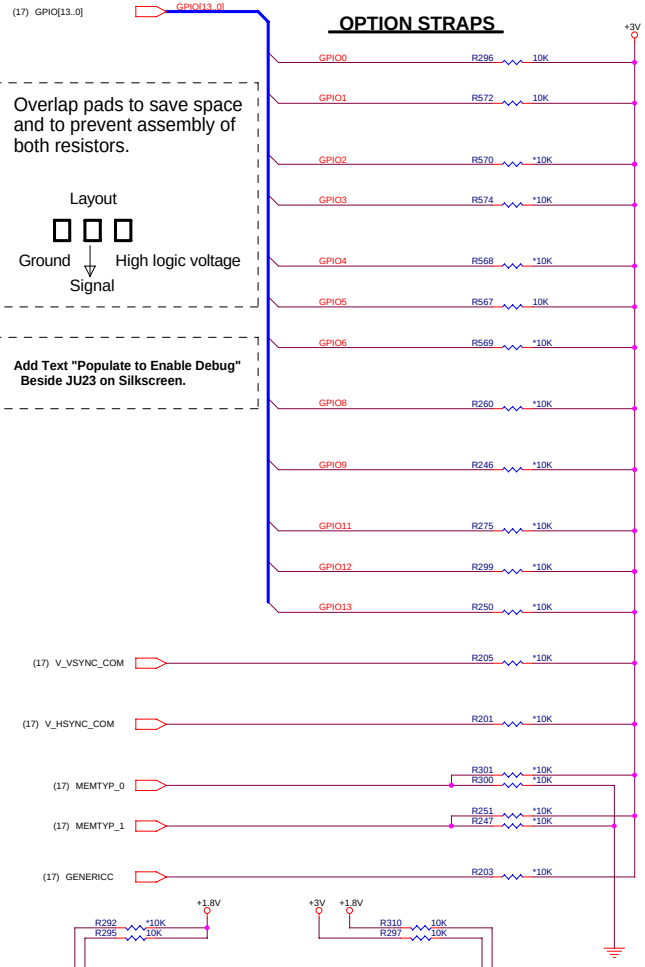
Layout

Ground ↓ High logic voltage

Signal

Add Text "Populate to Enable Debug" Beside JU23 on Silkscreen.

OPTION STRAPS



MEMTYP[0:1]

GPIO[26:25]	Vendor	Part No	Package organized
00	Samsung	K4J55323QG-BC20	256M(8Mx32) GDDR3
01	Samsung	K4J52324QC-BC20	512M(16Mx32) GDDR3
10	Infineon	HYB18H256321AF-12	256M(8Mx32) GDDR3
11	Infineon	HYB18H512321AFL-20	512M(16Mx32) GDDR3
	Hynix	HY5RS123235F-	512M(16Mx32) GDDR3

Memory Aperture Size Select
When no ROM is attached, GPIO[9] is set to 0.
GPIO[13:12] is used to select the memory aperture size.
GPIO[13:12] = 00: 128M memory aperture, same as ROM strap 00
GPIO[13:12] = 01: 256M memory aperture, same as ROM strap 01
GPIO[13:12] = 10: 64M memory aperture, same as ROM strap 10
GPIO[13:12] = 11: reserved, same as ROM strap 11

M54-P Strap

STRAPS	PIN	DESCRIPTION	ASIC DEFAULT
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 50% Tx output swing 1.full Tx output swing	
TX_DEEMPH_EN	GPIO1	Transmitter De-emphasis Enable 0: Tx de-emphasis disabled 1.Tx de-emphasis enabled	
	GPIO(3:2)	RSVD	
DEBUG_ACCESS	GPIO4	Strap to set the debug muxes to bring out DEBUG signals even if registers are inaccessible	0
	GPIO5	RSVD	
	GPIO6	RSVD	
Force_Compliance	GPIO8	Force chip to get to compliance state quickly for Tester purposes	0
ROMIDCFG(3:0)	GPIO(9,13:11)	If no ROM attached, comtrols chip IDis. If rom attached identifies ROM type 000x - No ROM, MEM_AP_SIZE=00 001x - No ROM,MEM_AP_SIZE=01 010x - No Rom, MEM_AP_SIZE=10 011x - No ROM,MEM_AP_SIZE=11 1000 - Parallel ROM, chip IDis from ROM 1001 - Serial AT25F1024 ROM (Atmel), chip IDis from ROM 1010 - Serial AT45DB011 ROM (Atmel), chip IDis from ROM 1011 - Serial M25P10 ROM (ST), chip IDis from ROM **1100 - Serial M25P05 ROM (ST), chip IDis from ROM** 1100 - Serial NX25F011B ROM (ISSI), chip IDis from ROM	
VIP_DEVICE	VSYNC	Indicates if any slave VIP host devices drove this pin low during reset. 0- Slave VIP host port deviced present. 1-No slave VIP port devices reporting presence during reset	No default
	H2SYNC, V2SYNC ,GENERICC	RSVD	
	VSYNC	RSVD	
	HSYNC	RSVD	
	PCIE_TEST	RSVD	

Board Straps

REV. 0.3

STRAPS	PIN	DESCRIPTION	VALUE
MEMTYPE(1:0)	DVALID, PSYNC.	Memory connected to R420 identification for BIOS **00 - Samsung GDDR 3 memory 144 Ball BGA package** 01 - TBD 10 - TBD 11 - TBD	000
DC_Strap1	GPIO(10)	Internal TMDS Enabled 0 - Disabled **1 - Enabled**	1
DC_Strap2	LCDDATA(13)	Video Capture Enabled **0 - Disabled** 1 - Not detected	0
DC_Strap3	LCDDATA(14)	HDTV out detect **0 - Detected** 1 - Enabled	1
DC_Strap4, DEMUX_SEL	LCDDATA(15,19)	Video capture enable 00 - DAC2 Off **01 - DAC2 On as CRT** 10 - DAC2 On as TVOUT 11 - DAC2 On as TVOUT and CRT	01
PAL/NTSC	LCDDATA(18)	TVO Standard Default (Resistor pull-up and switch short to GND) **0 - PAL (on board resistor pull-down and switch closed)** **1 -NTSC (on board resistor pull-up)**	1

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
C	M54P CORE GND & OPTION STRAPS(4 OF 6)	3A

Date: Friday, December 23, 2005 Sheet 19 of 45

RV410 MEMORY CHANNELS A and B

Channel A

(21) DQA_[63..0]

U33C

Part 3 of 7

MEMORY INTERFACE A

DQA_0 M31 … DQA_63 J14

MAA[15..0] (21)

MAA_0 D26 … MAA_15 C25

A_BA2 (21)
A_BA0 (21)
A_BA1 (21)

DQMAb_0 H31 … DQMAb_7 J17

DQMA0# (21) … DQMA7# (21)

read strobe

QSA_0 J31 … QSA_7 H15

RDQSA0 (21) … RDQSA7 (21)

write strobe

QSA_0B K31 … QSA_7B J15

WDQSA0 (21) … WDQSA7 (21)

ODTA F29
ODTA1 D24

CLKA0 D31
CLKA0b E31

CLKA0 (21)
CLKA0# (21)

CKEA0 B30 — CKEA0 (21)

RASA0b B28 — RASA0# (21)

CASA0b C29 — CASA0# (21)

WEA0b B31 — WEA0# (21)

CSA0b_0 B29 — CSA0_0# (21)
CSA0b_1 C28

CLKA1 B20
CLKA1b C19

CLKA1 (21)
CLKA1# (21)

CKEA1 C22 — CKEA1 (21)

RASA1b B24 — RASA1# (21)

CASA1b B22 — CASA1# (21)

WEA1b B21 — WEA1# (21)

CSA1b_0 B23 — CSA1_0# (21)
CSA1b_1 C23

M54-P

+1.8V
R150 40.2/F
VRAM_REF0
R151 100/F
C293 0.1U

+1.8V
R160 40.2/F
VRAM_REF1
R153 100/F
C296 0.1U

MVREFD_0 C31
MVREFS_0 C30

Channel B

U33D

Part 4 of 7

MEMORY INTERFACE B

DQB_0 B12 … DQB_63 W9

MAB_0 G4 … MAB_15 H3

DQMBb_0 B8 … DQMBb_7 T9

read strobe

QSB_0 B9 … QSB_7 V8

write strobe

QSB_0B B10 … QSB_7B V9

ODTB D6
ODTB1 J4

CLKB0 B4
CLKB0b B5

CKEB0 C2

RASB0b E2

CASB0b D3

WEB0b B2

CSB0b_0 D2
CSB0b_1 E3

CLKB1 N2
CLKB1b P3

CKEB1 L3

RASB1b J2

CASB1b L2

WEB1b M2

CSB1b_0 K2
CSB1b_1 K3

MVREFD_1 B3
MVREFS_1 C3

DRAM_RST AA3
TEST_MCLK AA5
TEST_YCLK AA2
MEMTEST AA7

M54-P

+1.8V
R270 40.2/F
VRAM_REF2
VRAM_REF3
R273 100/F
C448 0.1U

+1.8V
R280 40.2/F
R278 100/F
C459 0.1U

R277 2.2K
R267 4.7K
R276 4.7K
R263 24.9F

(21) DRAM_RST

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	M54P 3/4 OF 7	3A

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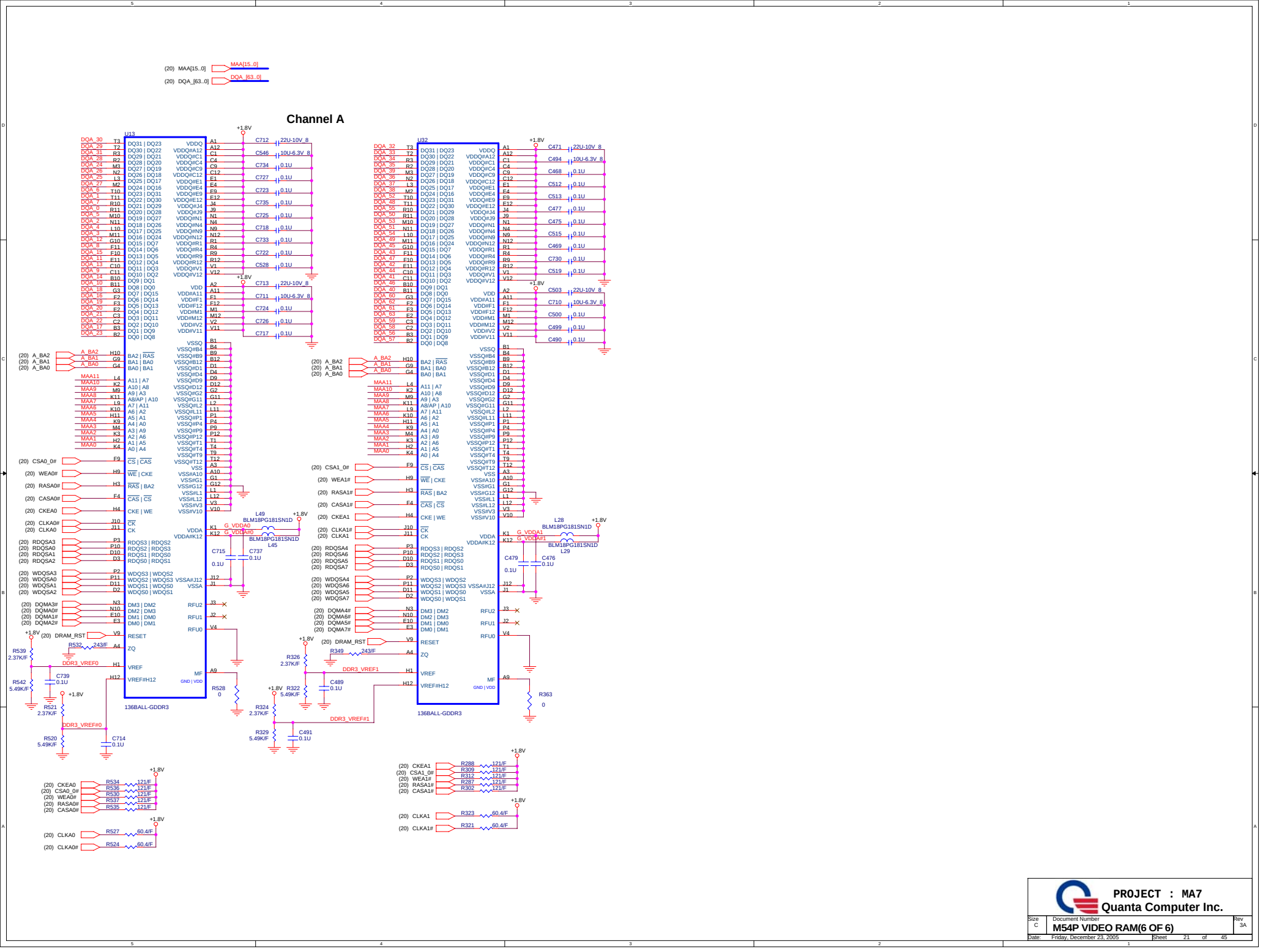
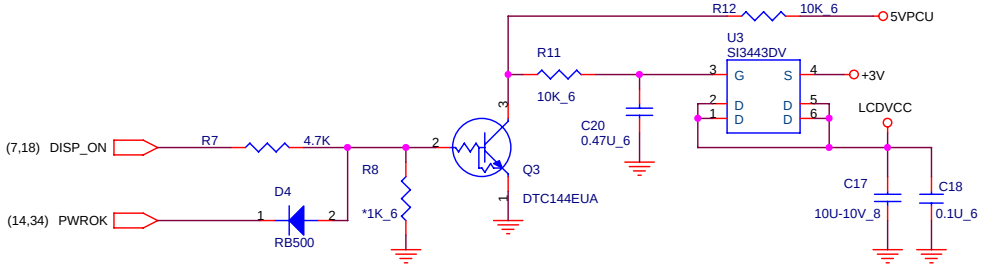
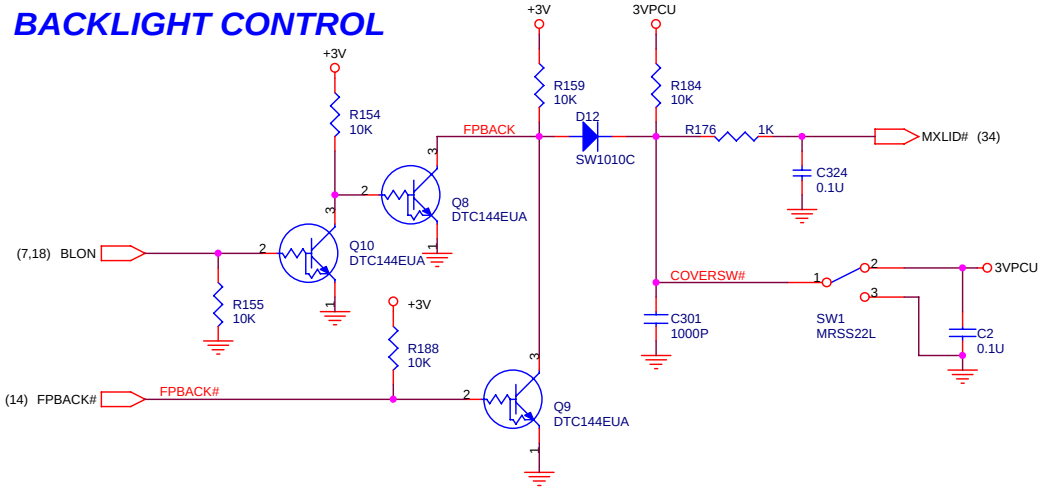

(20) MAA[15..0]
MAA[15..0]
(20) DQA_[63..0]
DQA_[63..0]
Channel A
U13
U32
136BALL-GDDR3
+1.8V
DRAM_RST
DDR3_VREF0
DDR3_VREF1
DDR3_VREF#0
DDR3_VREF#1
PROJECT : MA7
Quanta Computer Inc.
M54P VIDEO RAM(6 OF 6)
Size C
Document Number
Rev 3A
Date: Friday, December 23, 2005
Sheet 21 of 45

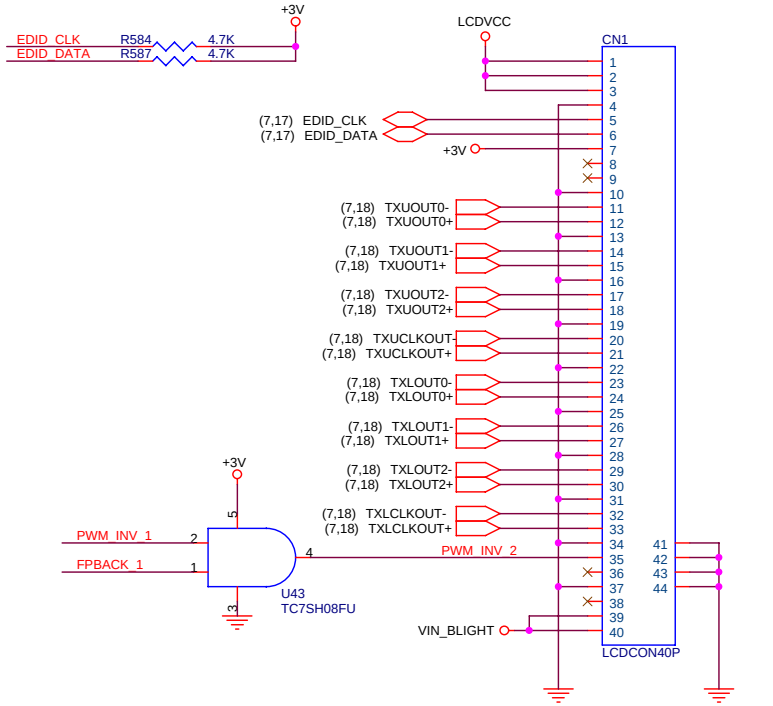
PANEL VCC CONTROL

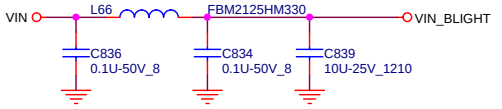


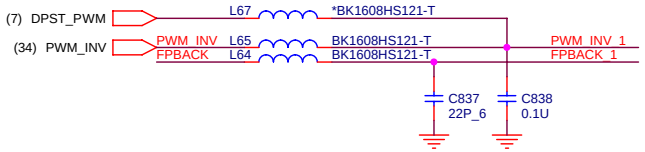
BACKLIGHT CONTROL



LCD CONNECTOR



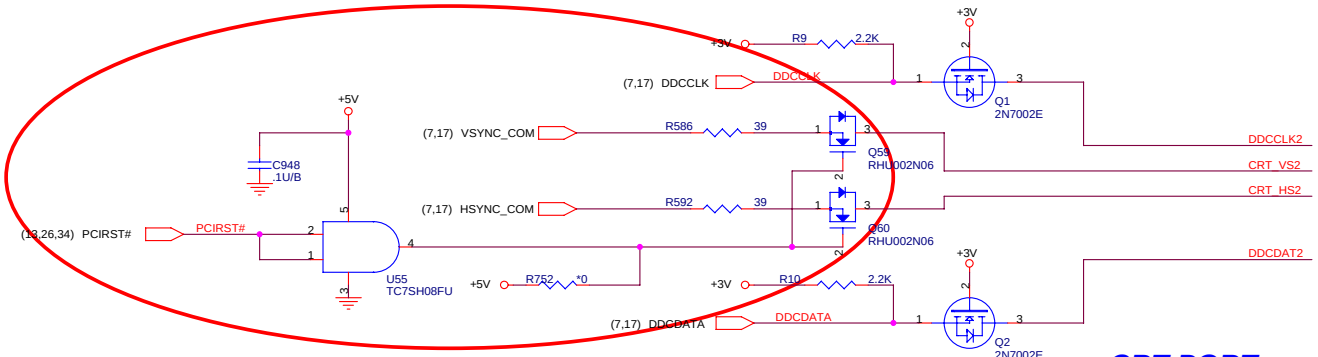




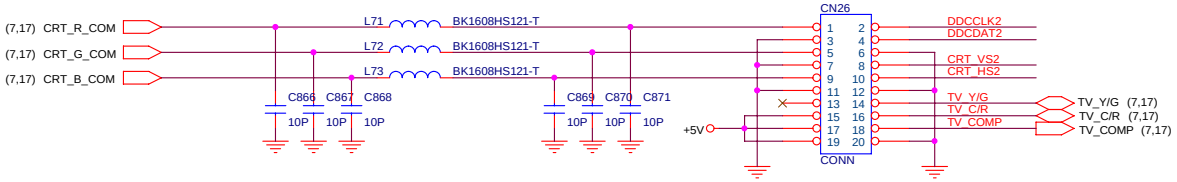
PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
B	LCD CONN	3A

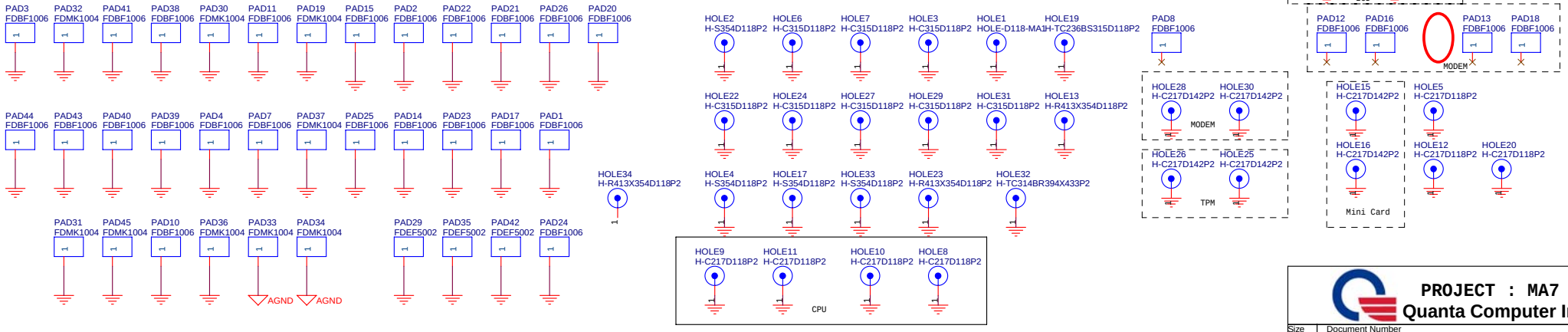
Date: Friday, December 23, 2005 Sheet 22 of 45



CRT PORT



TV-OUT



PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA(TV/CRT/PANEL)	3A

Date: Friday, December 23, 2005 Sheet 23 of 45

C: 88E8053 LF PN: AJ080530010 (20050414)

1Mbits

C: Add 9 X GND Pad for LAN controller. (20050411)

C: Add these GND pin for via hole to GND Plane.

C: Add RC (R37 change to 200K, Add C101) delay to control LOM_DISABLE#. (20050411)

CLOSE CHIP

DELAY PIN10 AT LEAST 150ms

88E8038/88E8055

FOR 8038	
R325	2K
R328	NC

Install for 8038

NI for 8038

C: Widen to 20 mils. AVDD25 to 20 mils.(20050411)

C: Widen to 20 mils. VDD to 20 mils.(20050411)

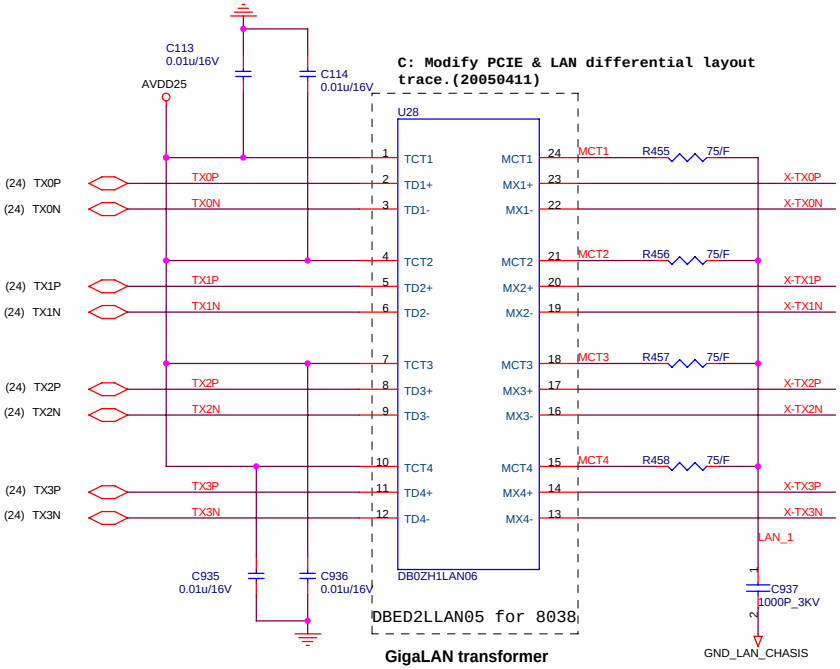
PLACEMENT CLOSE TO EACH OTHER

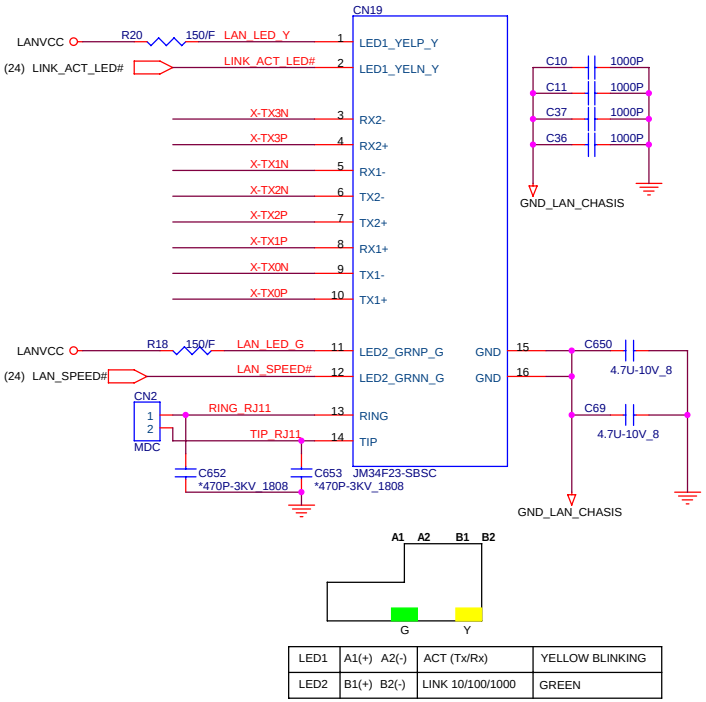
0804 REDUCING THE LANVCC NOISE

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN 88E8038 & RJ11,RJ45	3A

Date: Friday, December 23, 2005 Sheet 24 of 45



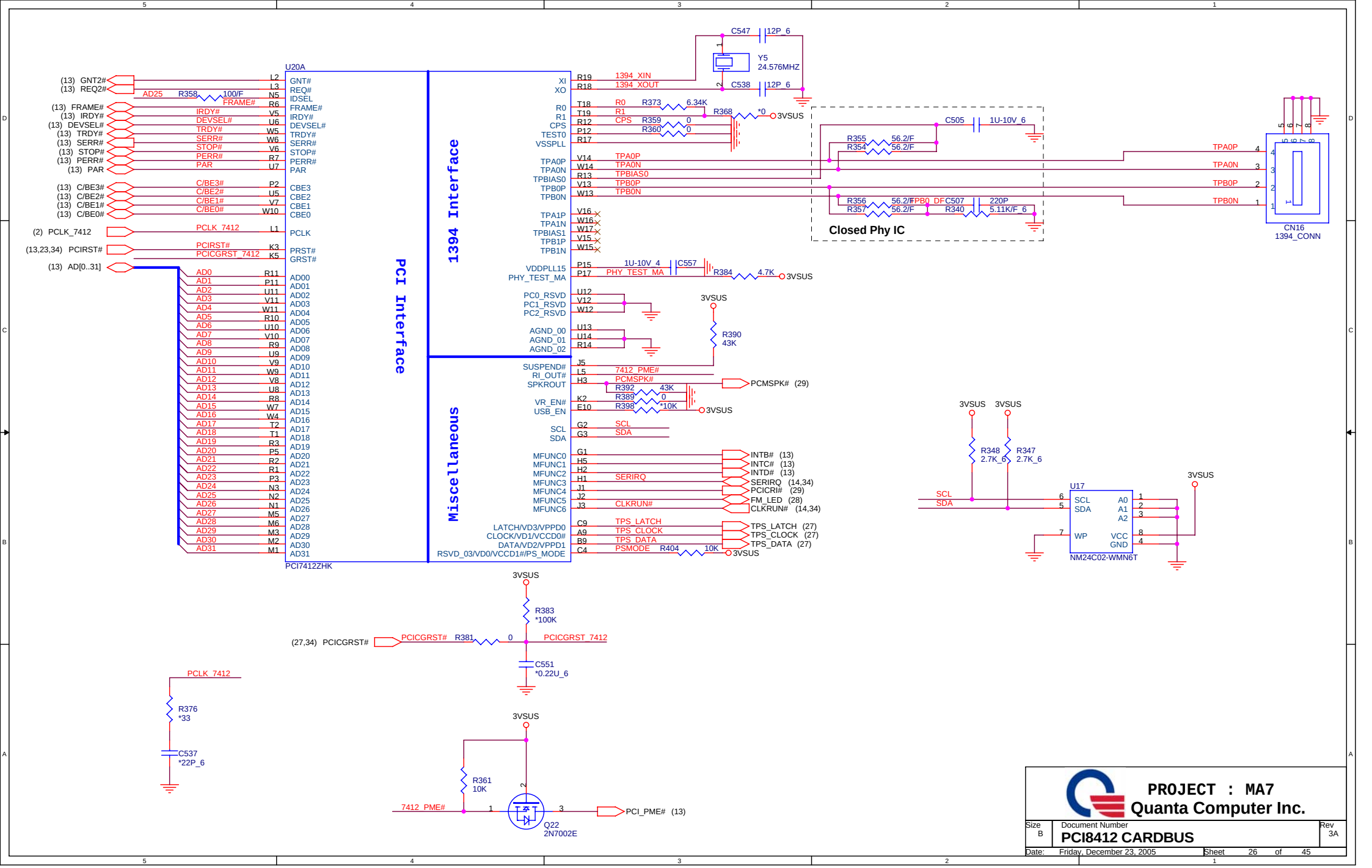


LED1	A1(+) A2(-)	ACT (Tx/Rx)	YELLOW BLINKING
LED2	B1(+) B2(-)	LINK 10/100/1000	GREEN

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LAN Power	3A

Date: Friday, December 23, 2005 Sheet 25 of 45


U20A
PCI Interface
1394 Interface
Miscellaneous
PCI7412ZHK
Closed Phy IC
CN16
1394_CONN
U17
NM24C02-WMN6T
Y5
24.576MHZ
3VSUS
PCLK_7412
PCICGRST_7412
PCI_PME#
Q22
2N7002E
PROJECT : MA7
Quanta Computer Inc.
PCI8412 CARDBUS
Size B
Document Number
Rev 3A
Date: Friday, December 23, 2005
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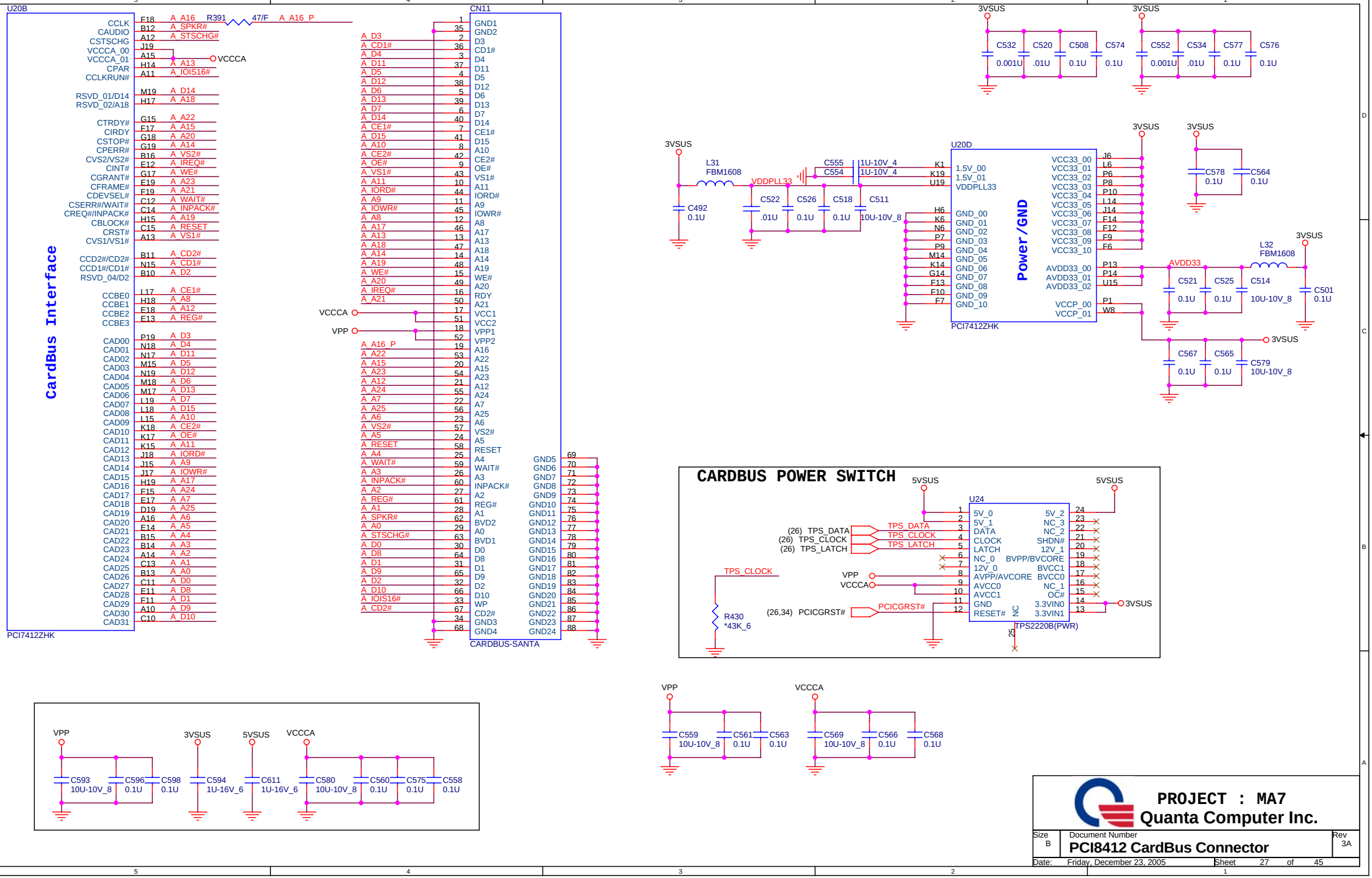
U20B
CardBus Interface
PCI7412ZHK
CN11
CARDBUS-SANTA
R391
47/F
A_A16_P
VCCCA
VPP
U20D
Power/GND
PCI7412ZHK
3VSUS
5VSUS
L31
FBM1608
L32
FBM1608
VDDPLL33
AVDD33
CARDBUS POWER SWITCH
U24
TPS2220B(PWR)
TPS_DATA
TPS_CLOCK
TPS_LATCH
PCICGRST#
R430
*43K_6
PROJECT : MA7
Quanta Computer Inc.
PCI8412 CardBus Connector
Size B
Document Number
Rev 3A
Date: Friday, December 23, 2005
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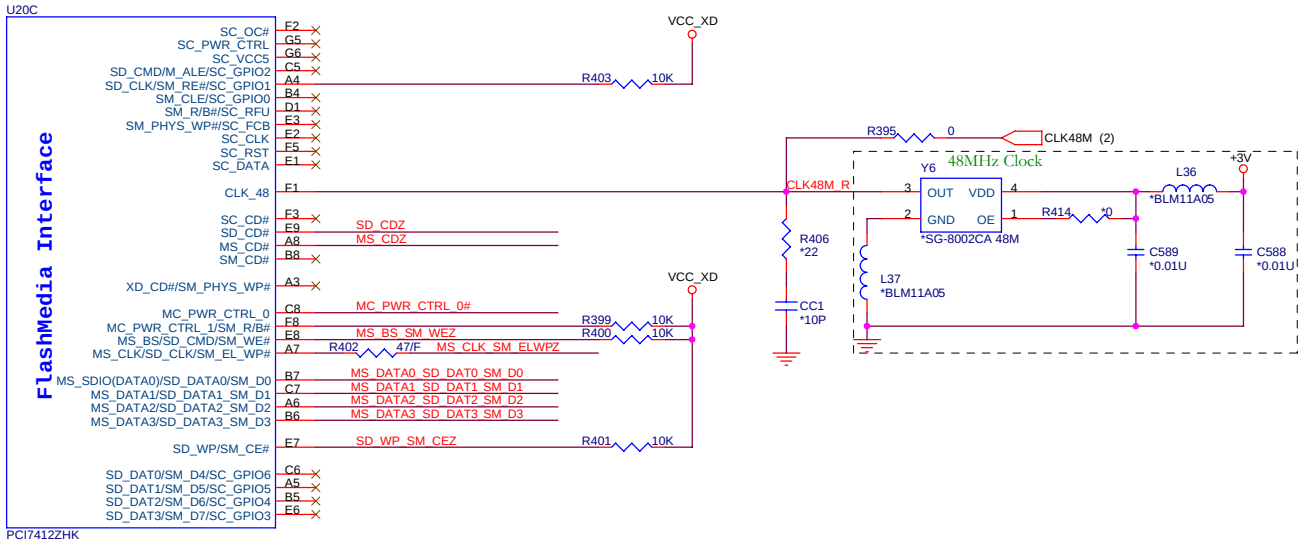
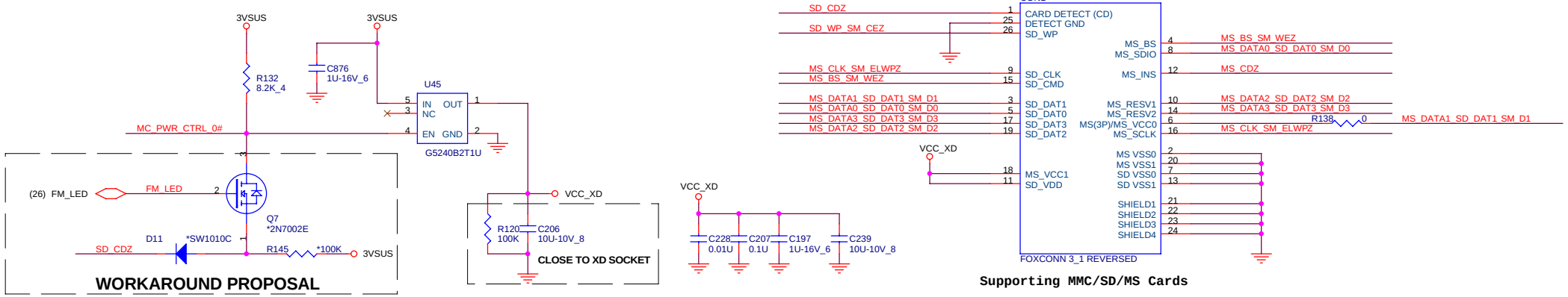


3 IN1 CARD READER



Supporting MMC/SD/MS Cards

PROJECT : MA7
Quanta Computer Inc.

Size	Document Number	Rev
Custom	PC8412 CARD_READER	3A

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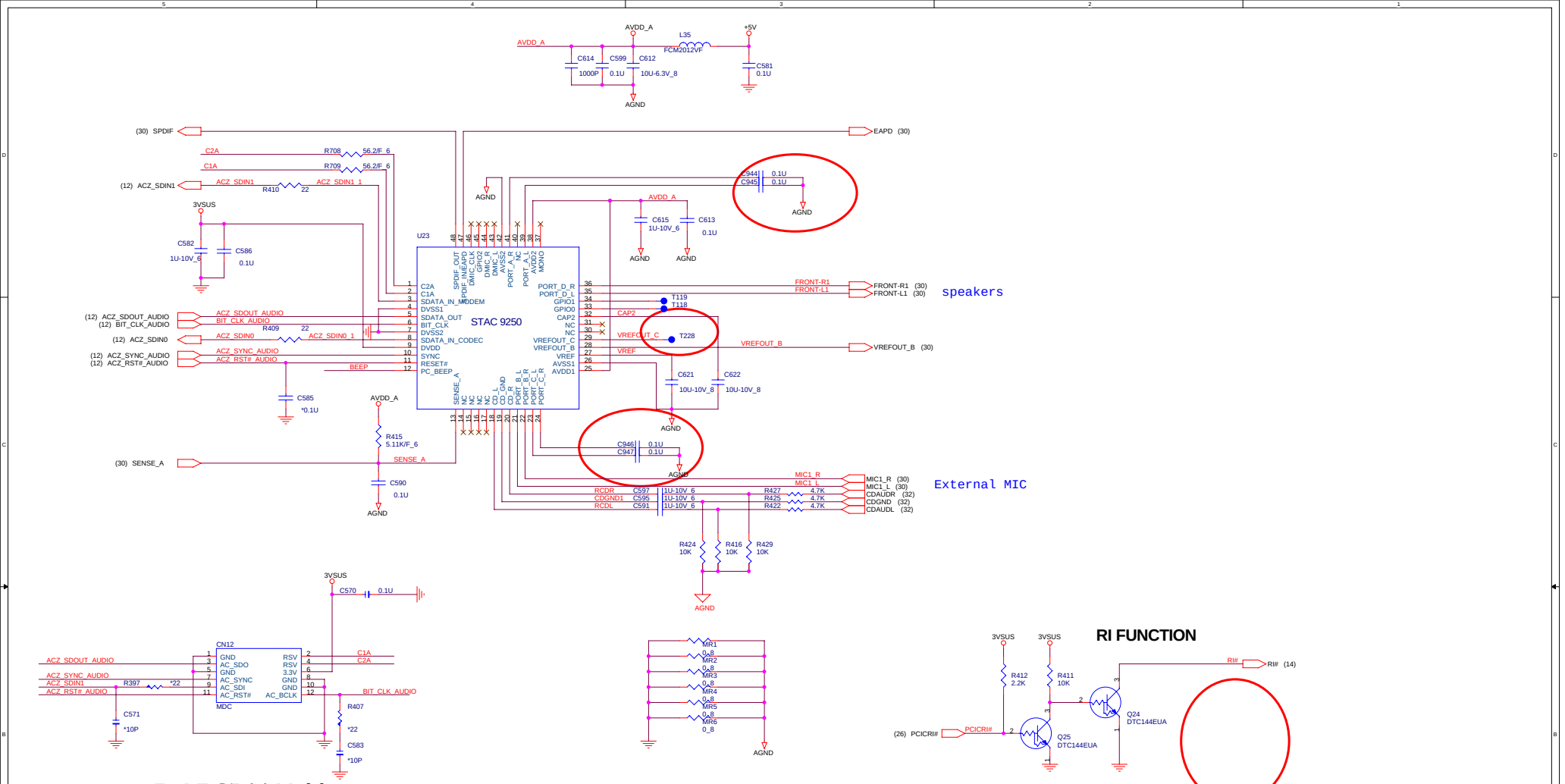
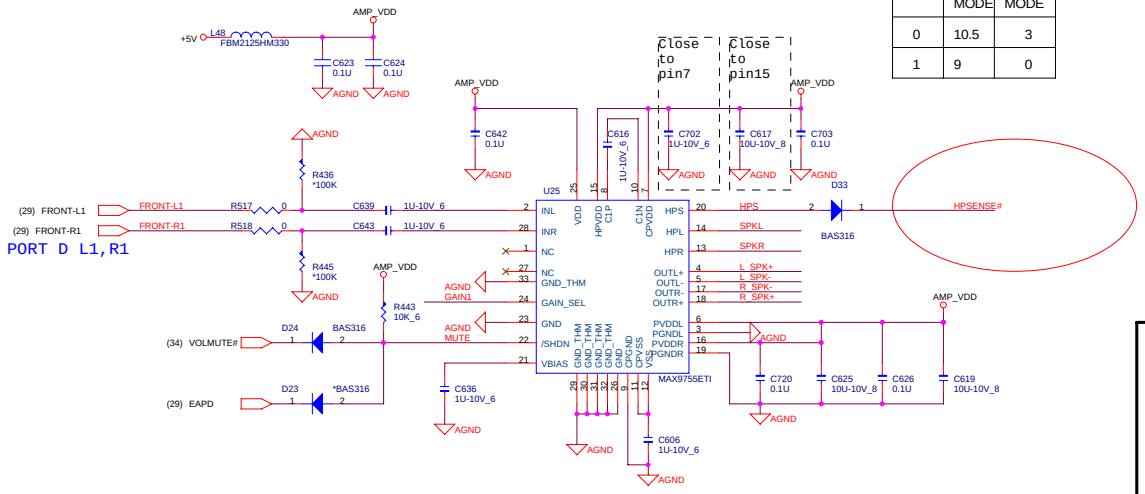
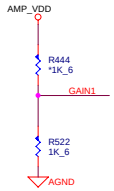


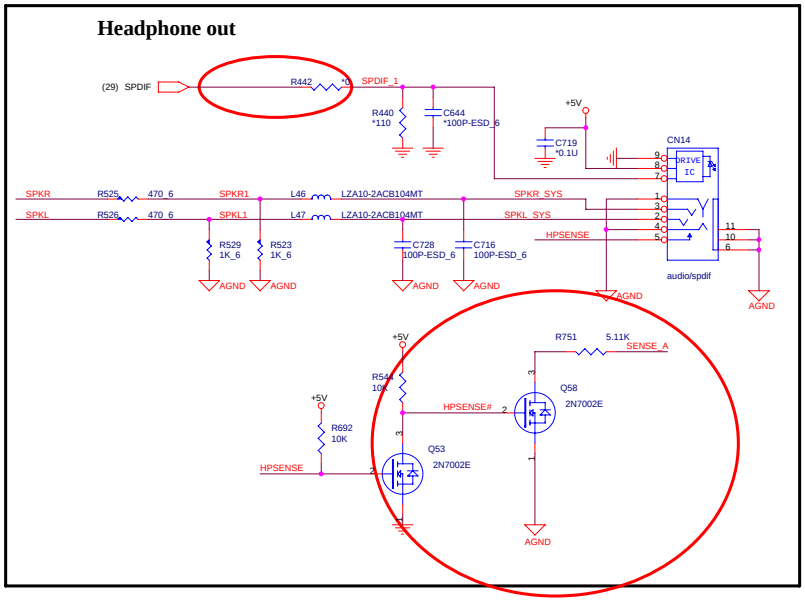
For MDC/DAA Module

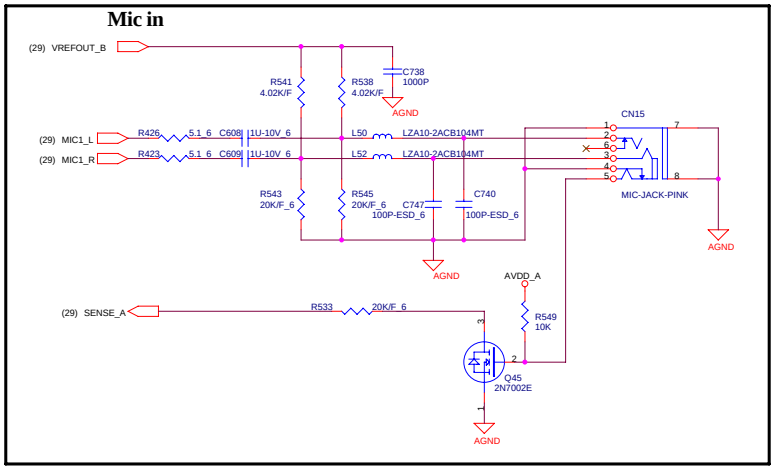
AUDIO AMPLIFIER-MAX9755

GAIN1	SPKR MODE	HP MODE
0	10.5	3
1	9	0

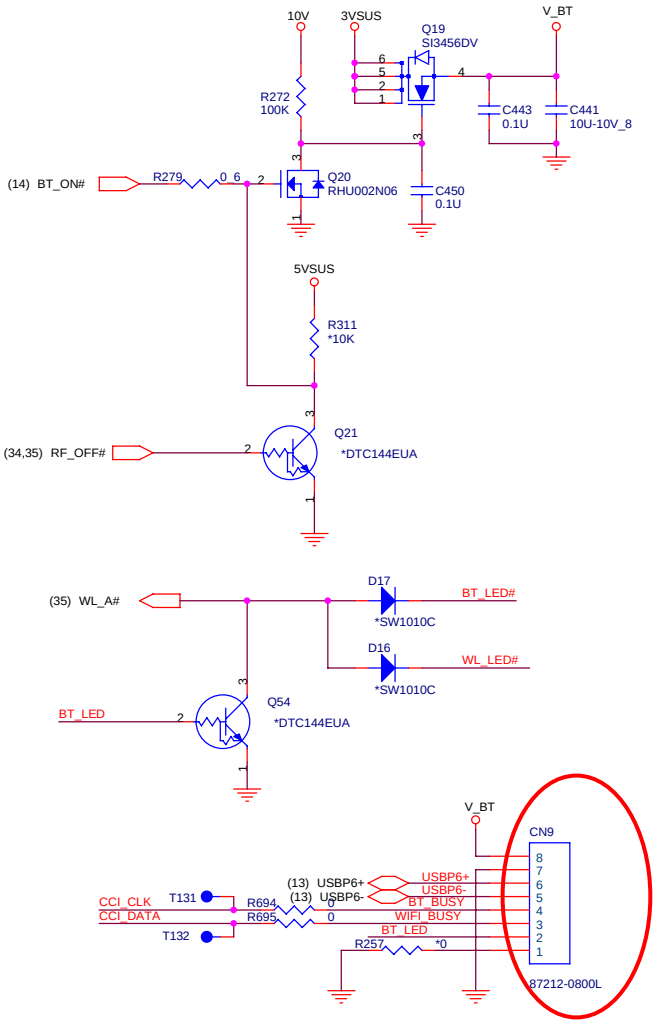




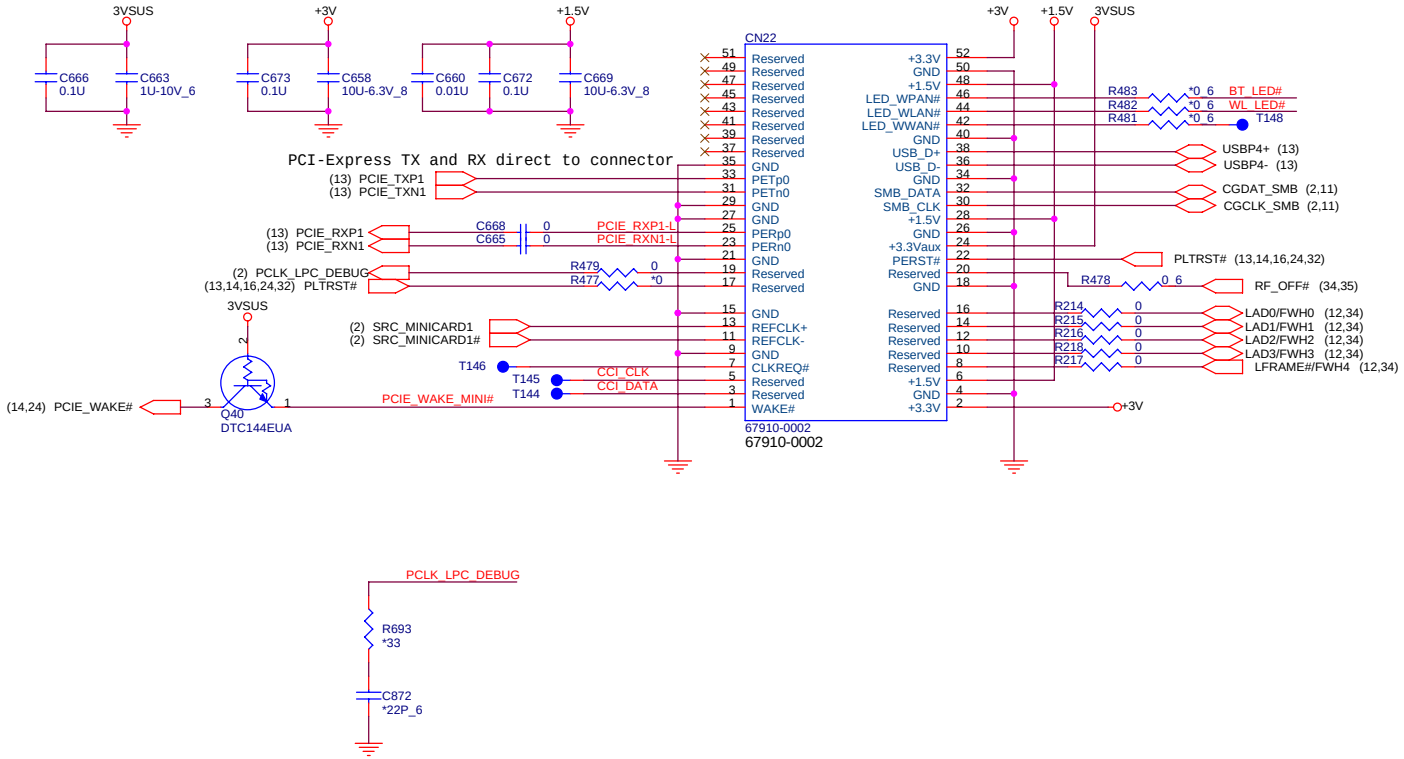




BLUETOOTH CONNECTOR



Mini PCI-E Card 1



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Quanta Computer Inc.

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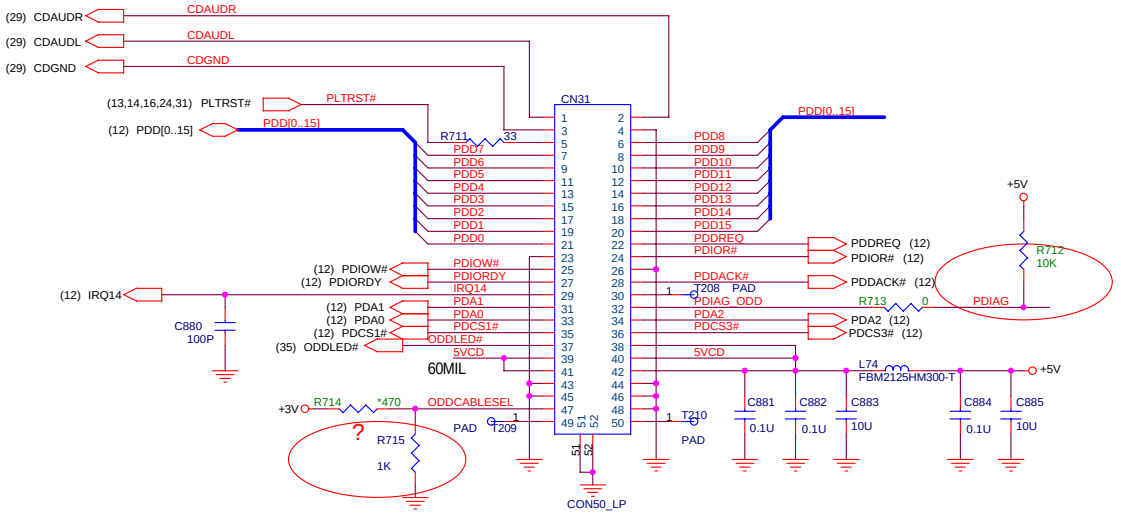
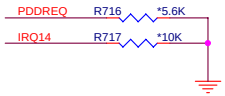
For fix ODD change 0427

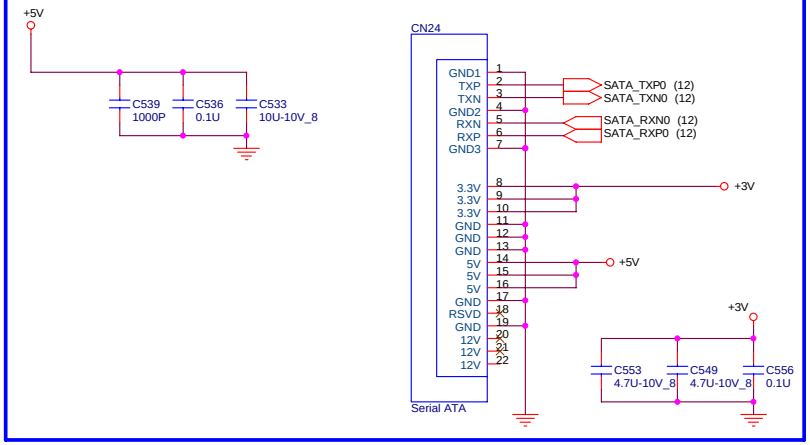
CD-ROM connector





SATA CONNECTOR

MASTER



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Quanta Computer Inc.			
Size: Custom	Document Number: SATA HDD, CD-ROM		Rev: 3A
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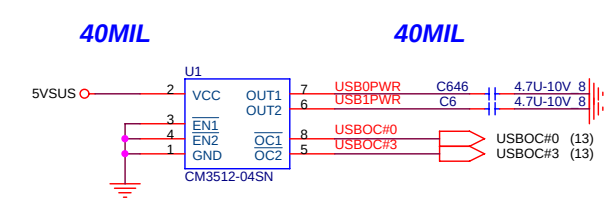
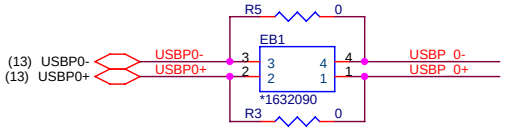
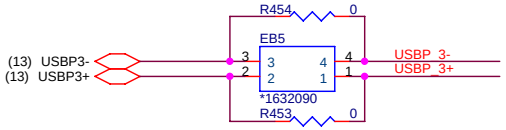
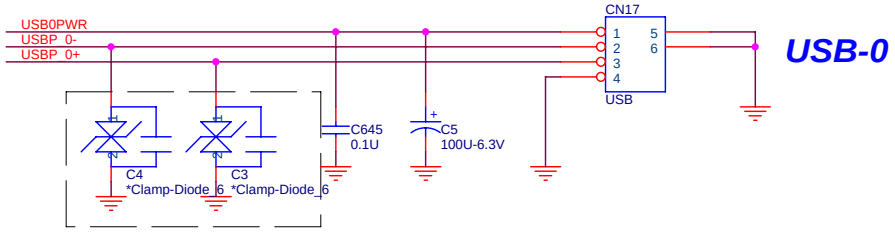
LEFT SIDE

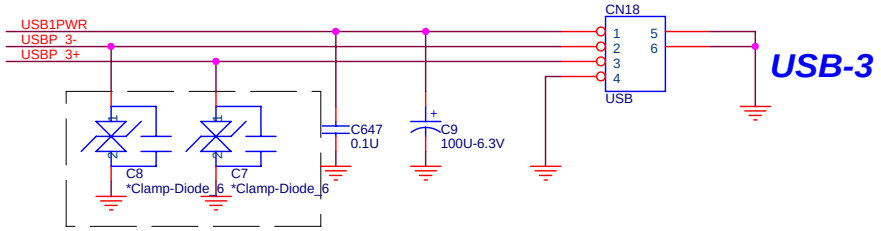


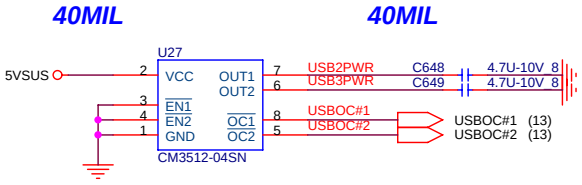


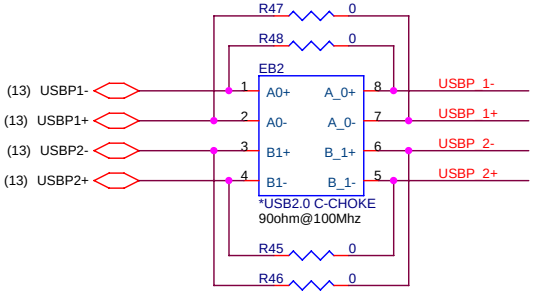


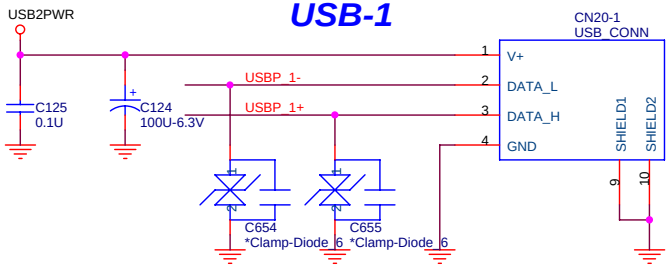


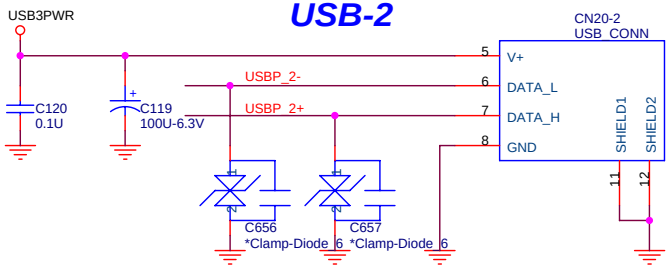
LEFT SIDE











(27,31,36,39,41) 5VSUS

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	**USB Ports**	3A
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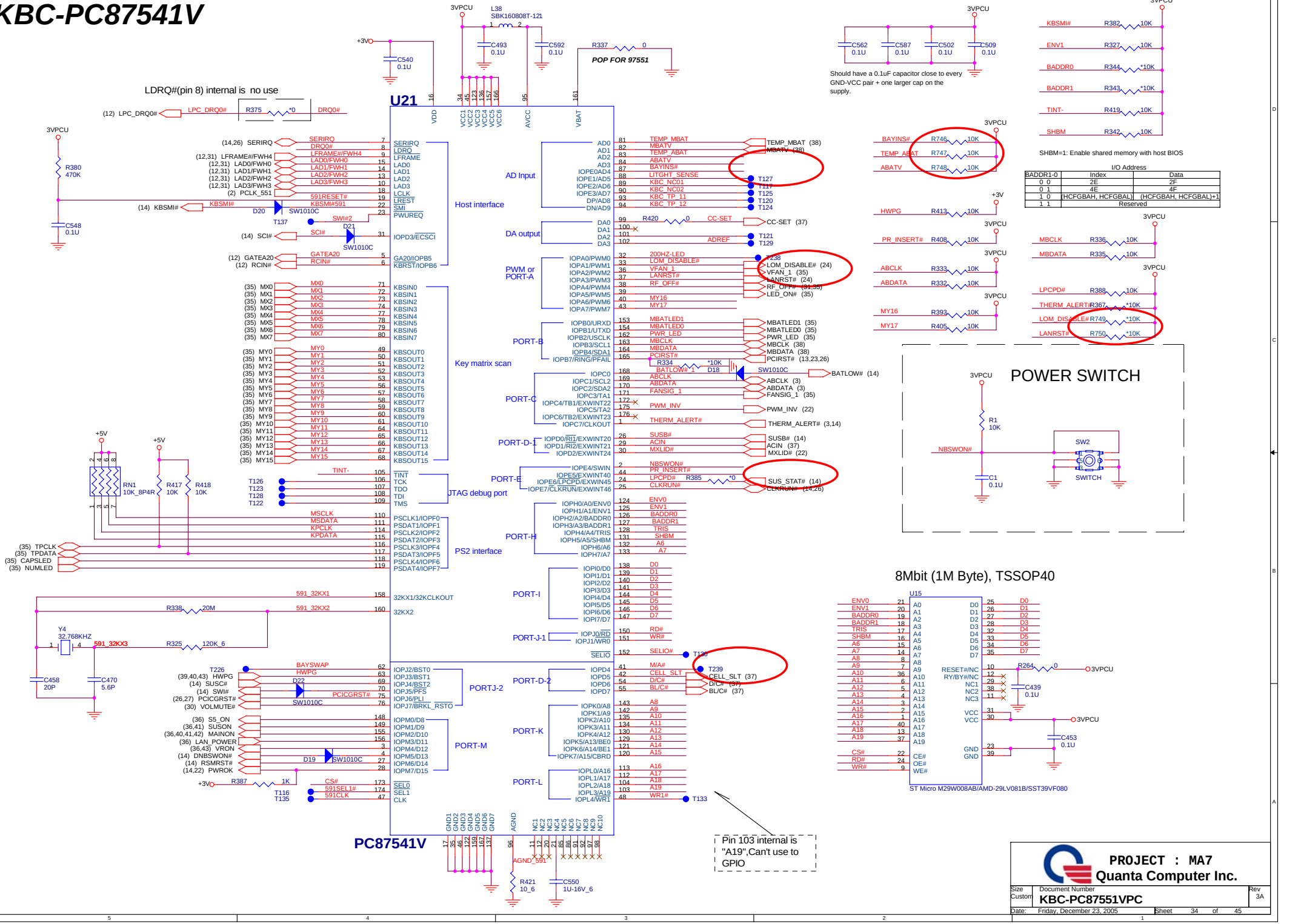
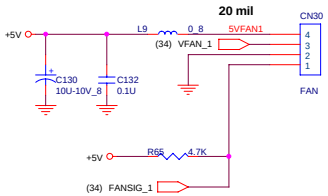
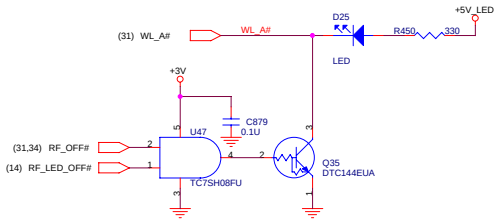
KBC-PC87541V



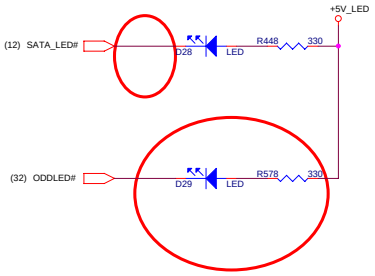
FAN OUT PWM CONNECTOR

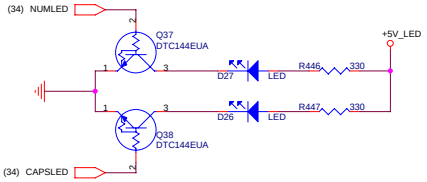


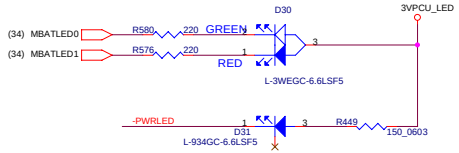
WIRELESS LED



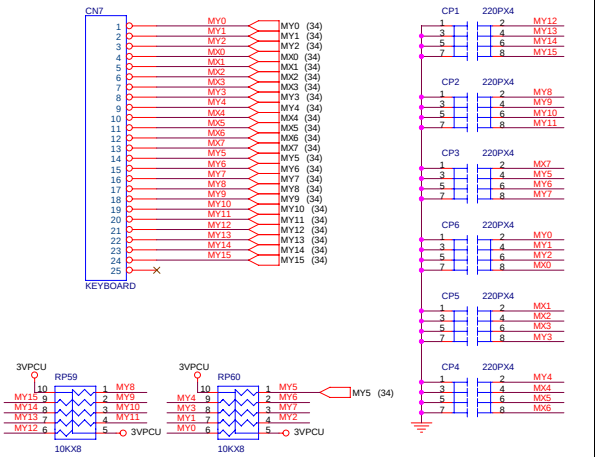
LED INDIACTOR



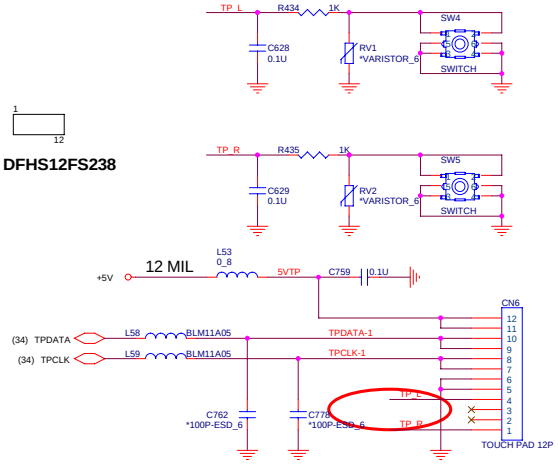


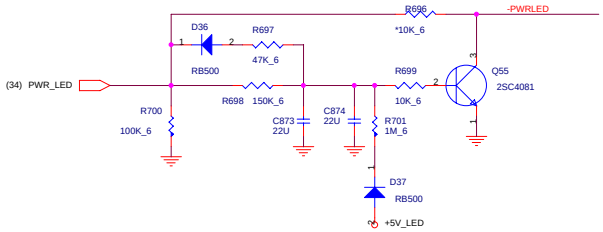


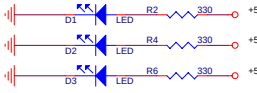
KEYBOARD

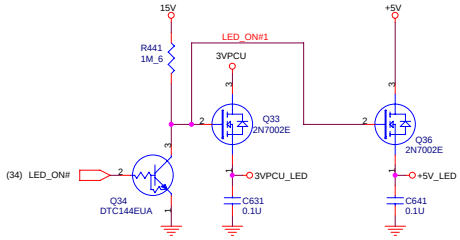


TOUCHPAD









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Quanta Computer Inc.

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C	TPM/TP/KEY/BTB	3A

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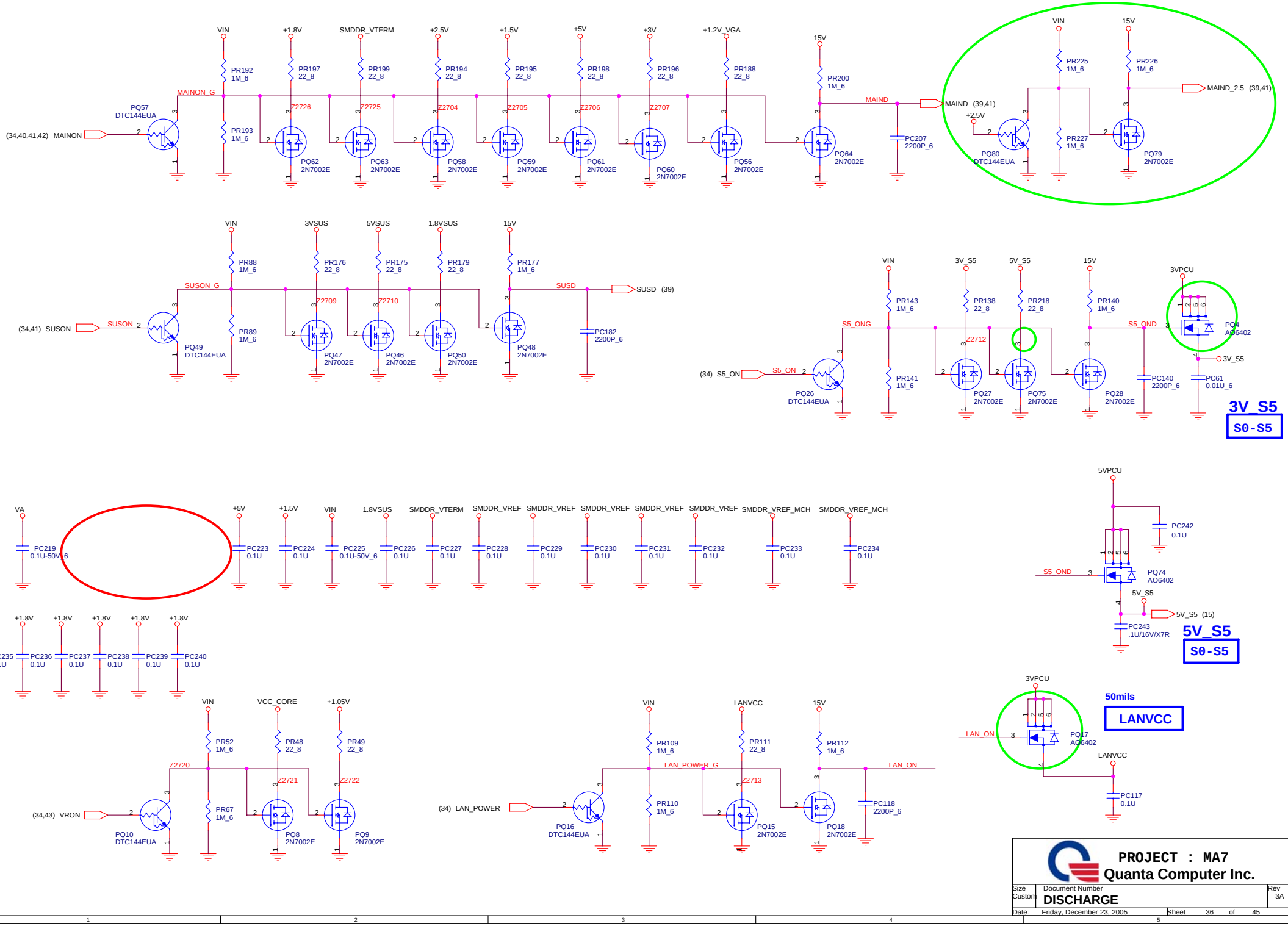
VIN
+1.8V
SMDDR_VTERM
+2.5V
+1.5V
+5V
+3V
+1.2V_VGA
15V
PR192 1M_6
PR197 22_8
PR199 22_8
PR194 22_8
PR195 22_8
PR198 22_8
PR196 22_8
PR188 22_8
PR200 1M_6
MAINON_G
MAIND
(34,40,41,42) MAINON
PQ57 DTC144EUA
PR193 1M_6
Z2726
Z2725
Z2704
Z2705
Z2706
Z2707
PQ62 2N7002E
PQ63 2N7002E
PQ58 2N7002E
PQ59 2N7002E
PQ61 2N7002E
PQ60 2N7002E
PQ56 2N7002E
PQ64 2N7002E
PC207 2200P_6
MAIND (39,41)
+2.5V
PR225 1M_6
PR226 1M_6
MAIND_2.5 (39,41)
PR227 1M_6
PQ80 DTC144EUA
PQ79 2N7002E
VIN
3VSUS
5VSUS
1.8VSUS
15V
PR88 1M_6
PR176 22_8
PR175 22_8
PR179 22_8
PR177 1M_6
SUSON_G
SUSD
SUSD (39)
(34,41) SUSON
SUSON
PR89 1M_6
Z2709
Z2710
PQ49 DTC144EUA
PQ47 2N7002E
PQ46 2N7002E
PQ50 2N7002E
PQ48 2N7002E
PC182 2200P_6
VIN
3V_S5
5V_S5
15V
3VPCU
PR143 1M_6
PR138 22_8
PR218 22_8
PR140 1M_6
S5_ONG
S5_OND
Z2712
(34) S5_ON
S5_ON
PR141 1M_6
PQ26 DTC144EUA
PQ27 2N7002E
PQ75 2N7002E
PQ28 2N7002E
PQ4 AO6402
PC140 2200P_6
PC61 0.01U_6
3V_S5
3V_S5
S0-S5
VA
PC219 0.1U-50V_6
+5V
+1.5V
VIN
1.8VSUS
SMDDR_VTERM
SMDDR_VREF
SMDDR_VREF
SMDDR_VREF
SMDDR_VREF
SMDDR_VREF
SMDDR_VREF_MCH
SMDDR_VREF_MCH
PC223 0.1U
PC224 0.1U
PC225 0.1U-50V_6
PC226 0.1U
PC227 0.1U
PC228 0.1U
PC229 0.1U
PC230 0.1U
PC231 0.1U
PC232 0.1U
PC233 0.1U
PC234 0.1U
5VPCU
PC242 0.1U
S5_OND
PQ74 AO6402
5V_S5
5V_S5 (15)
PC243 .1U/16V/X7R
5V_S5
S0-S5
+1.8V
PC235 0.1U
PC236 0.1U
PC237 0.1U
PC238 0.1U
PC239 0.1U
PC240 0.1U
VIN
VCC_CORE
+1.05V
PR52 1M_6
PR48 22_8
PR49 22_8
Z2720
Z2721
Z2722
(34,43) VRON
PR67 1M_6
PQ10 DTC144EUA
PQ8 2N7002E
PQ9 2N7002E
VIN
LANVCC
15V
PR109 1M_6
PR111 22_8
PR112 1M_6
LAN_POWER_G
LAN_ON
Z2713
(34) LAN_POWER
PR110 1M_6
PQ16 DTC144EUA
PQ15 2N7002E
PQ18 2N7002E
PC118 2200P_6
3VPCU
50mils
LANVCC
LAN_ON
PQ17 AO6402
LANVCC
PC117 0.1U
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Quanta Computer Inc.
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Custom
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DISCHARGE
Rev
3A
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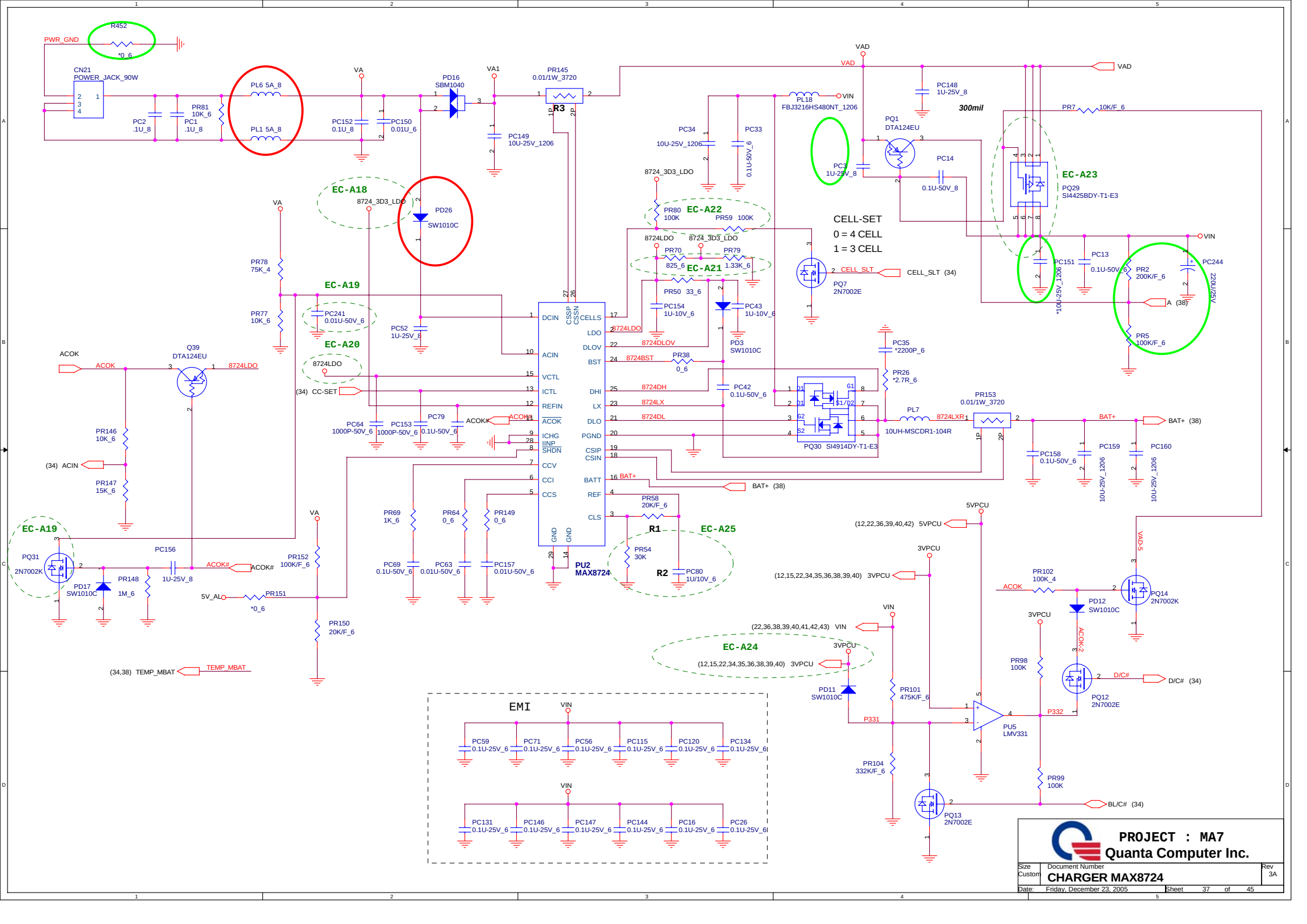

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Quanta Computer Inc.

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Custom	CHARGER MAX8724	3A

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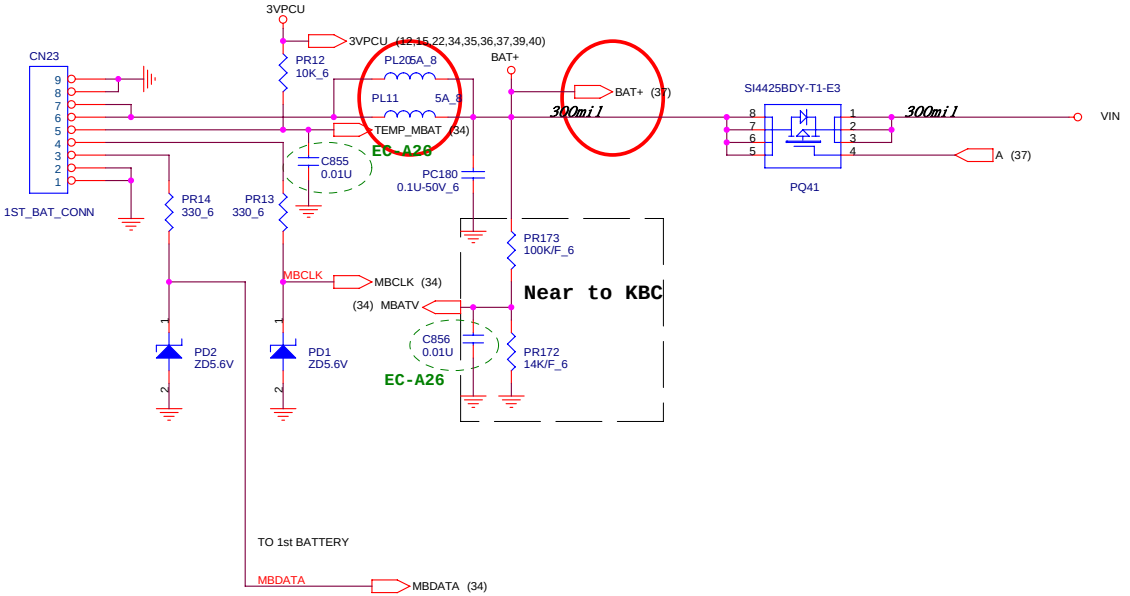

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Quanta Computer Inc.

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Custom	BBATT SELECTER	3A

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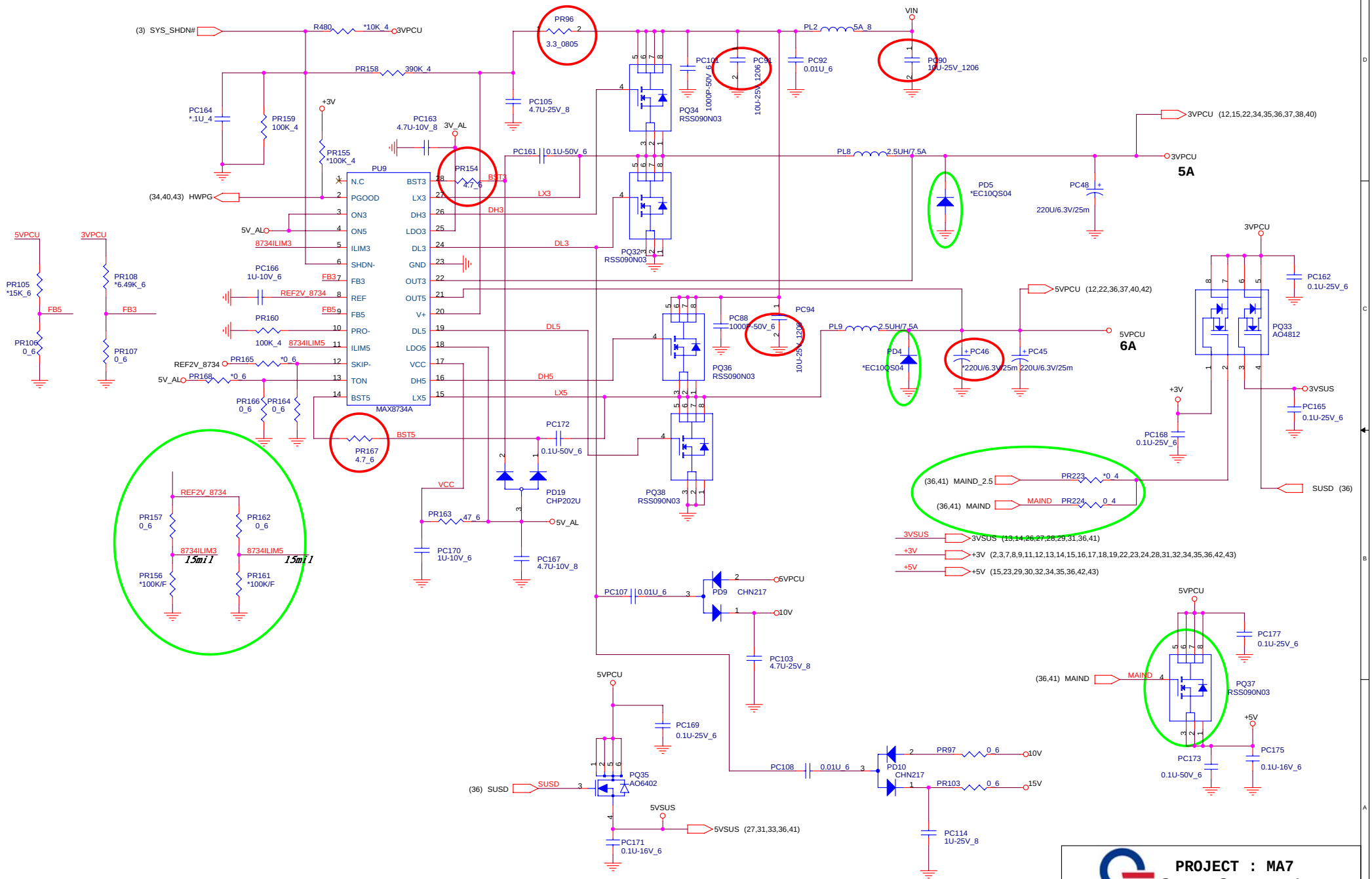
DC-DC(MAX8734A)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	3V/5V	3A
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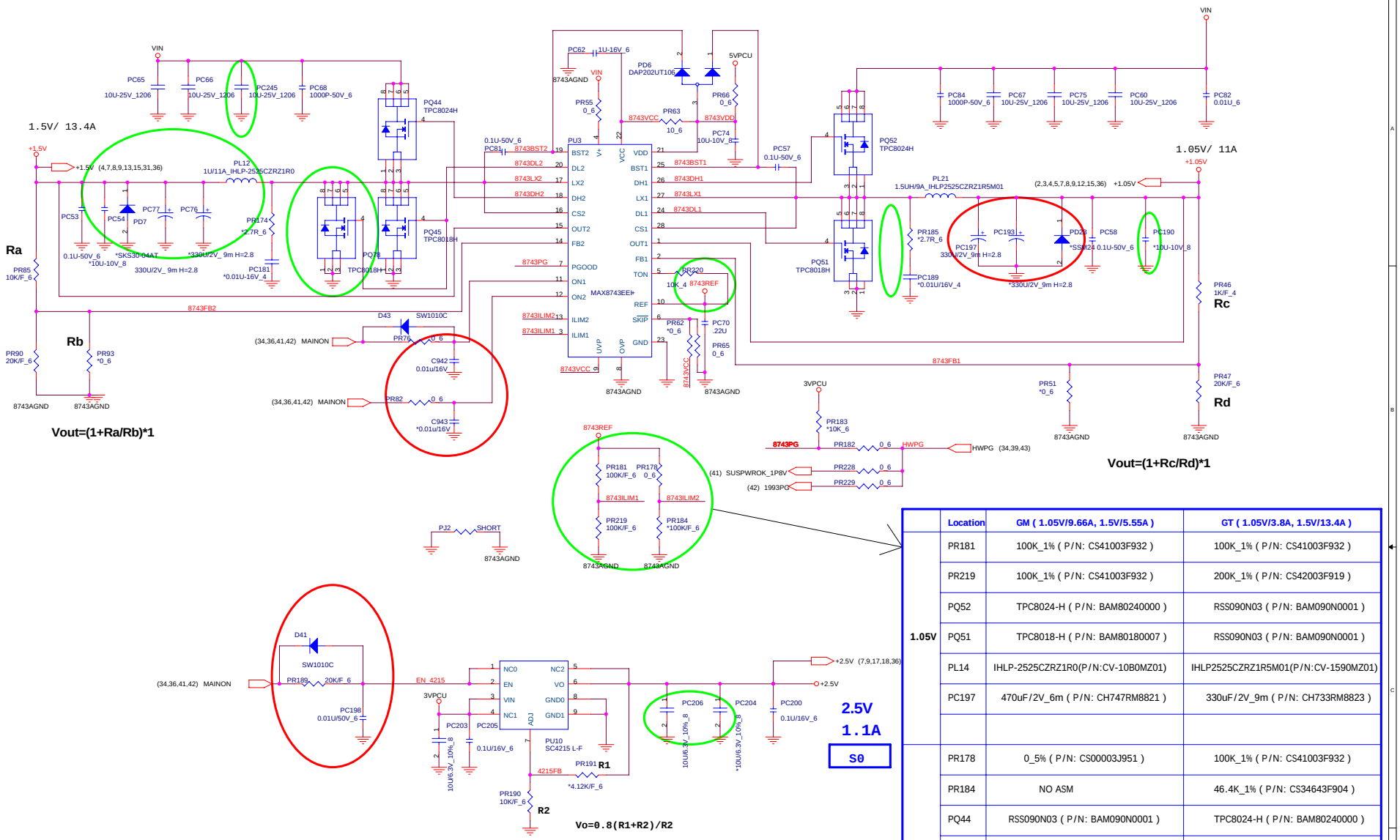

	Location	GM (1.05V/9.66A, 1.5V/5.55A)	GT (1.05V/3.8A, 1.5V/13.4A)
1.05V	PR181	100K_1% (P/N: CS41003F932)	100K_1% (P/N: CS41003F932)
	PR219	100K_1% (P/N: CS41003F932)	200K_1% (P/N: CS42003F919)
	PQ52	TPC8024-H (P/N: BAM80240000)	RSS090N03 (P/N: BAM090N0001)
	PQ51	TPC8018-H (P/N: BAM80180007)	RSS090N03 (P/N: BAM090N0001)
	PL14	IHLP-2525CZRZ1R0(P/N:CV-10B0MZ01)	IHLP2525CZRZ1R5M01(P/N:CV-1590MZ01)
	PC197	470uF/2V_6m (P/N: CH747RM8821)	330uF/2V_9m (P/N: CH733RM8823)
1.5V	PR178	0_5% (P/N: CS00003J951)	100K_1% (P/N: CS41003F932)
	PR184	NO ASM	46.4K_1% (P/N: CS34643F904)
	PQ44	RSS090N03 (P/N: BAM090N0001)	TPC8024-H (P/N: BAM80240000)
	PQ45	RSS090N03 (P/N: BAM090N0001)	TPC8018-H (P/N: BAM80180007)
	PQ?	NO ASM	TPC8018-H (P/N: BAM80180007)
	PL14	IHLP2525CZRZ1R5M01(P/N:CV-1590MZ01)	IHLP-2525CZRZ1R0(P/N:CV-10B0MZ01)
	PC77	330uF/2V_9m (P/N: CH733RM8823)	470uF/2V_6m (P/N: CH747RM8821)

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX8743 1.5VS_5/+1.05V/2.5V	3A

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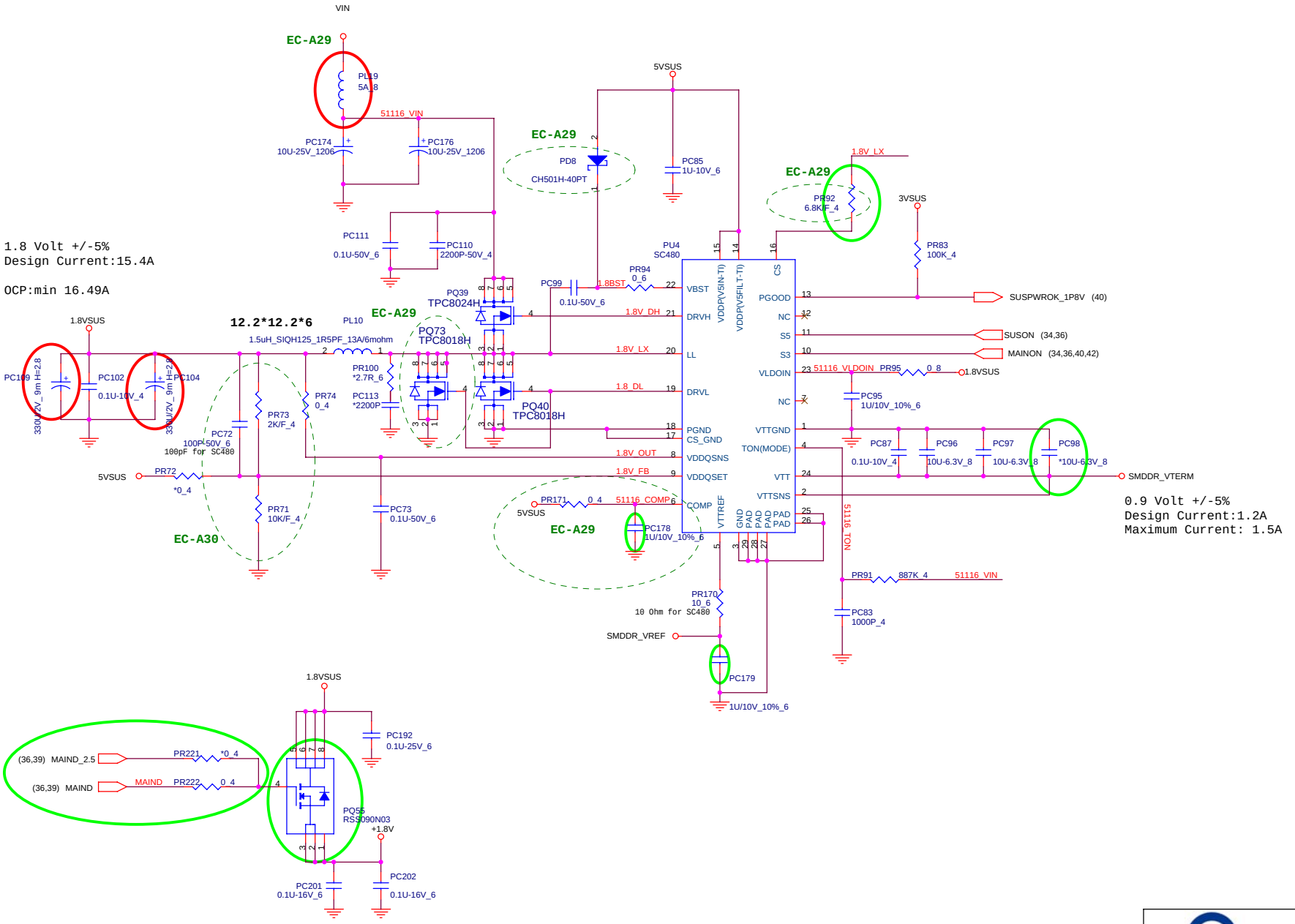

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	1.8V/0.9V/VGA1.2V	3A
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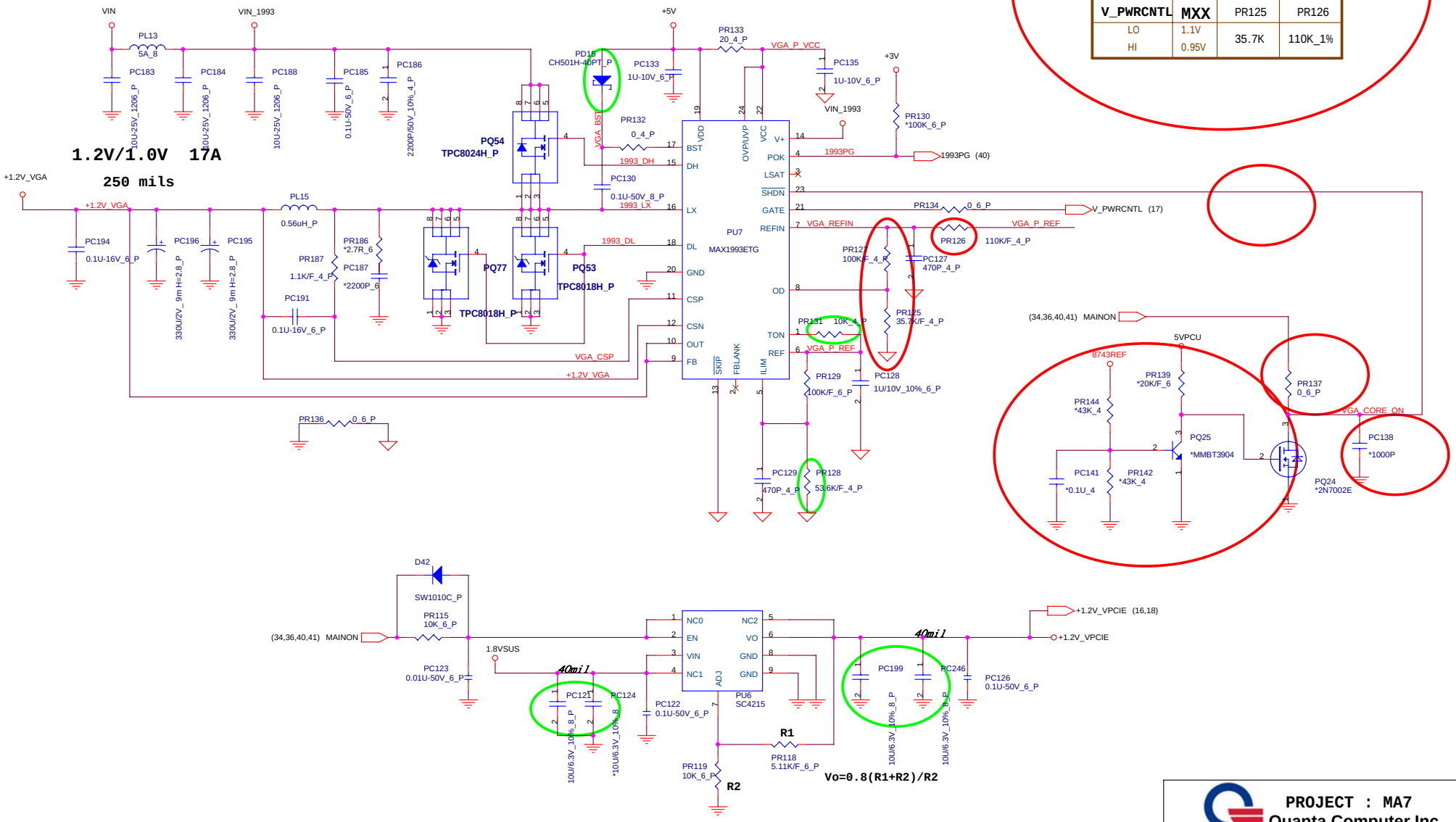
V_PWRCNTL	MXX	PR125	PR126
LO	1.2V	51.1K_1%	100K_1%
HI	1.0V		

V_PWRCNTL	MXX	PR125	PR126
LO	1.1V	35.7K	110K_1%
HI	0.95V		



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	VGA_CORE & +VGA1.2V	3A
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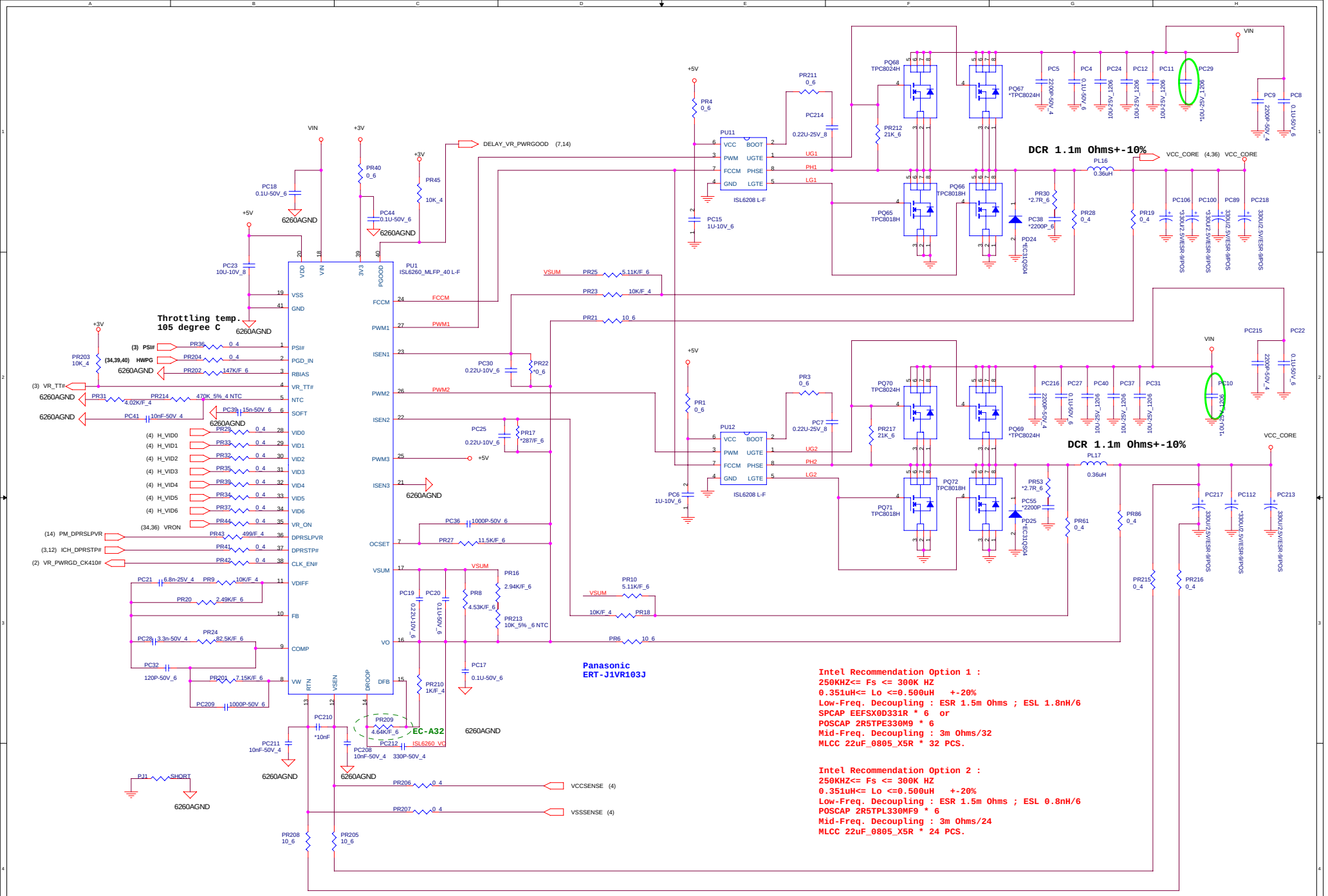
VIN
+5V
+3V
DELAY_VR_PWRGOOD (7,14)
PU1 ISL6260_MLFP_40 L-F
PU11 ISL6208 L-F
PU12 ISL6208 L-F
PQ68 TPC8024H
PQ67 *TPC8024H
PQ66 TPC8018H
PQ65 TPC8018H
PQ70 TPC8024H
PQ69 *TPC8024H
PQ72 TPC8018H
PQ71 TPC8018H
PD24 *EC31QS04
PD25 *EC31QS04
PL16 0.36uH
PL17 0.36uH
VCC_CORE (4,36) VCC_CORE
DCR 1.1m Ohms+-10%
DCR 1.1m Ohms+-10%
Throttling temp.
105 degree C
6260AGND
Panasonic
ERT-J1VR103J
EC-A32
Intel Recommendation Option 1 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 1.8nH/6
SPCAP EEFSX0D331R * 6 or
POSCAP 2R5TPE330M9 * 6
Mid-Freq. Decoupling : 3m Ohms/32
MLCC 22uF_0805_X5R * 32 PCS.
Intel Recommendation Option 2 :
250KHZ<= Fs <= 300K HZ
0.351uH<= Lo <=0.500uH +-20%
Low-Freq. Decoupling : ESR 1.5m Ohms ; ESL 0.8nH/6
POSCAP 2R5TPL330MF9 * 6
Mid-Freq. Decoupling : 3m Ohms/24
MLCC 22uF_0805_X5R * 24 PCS.
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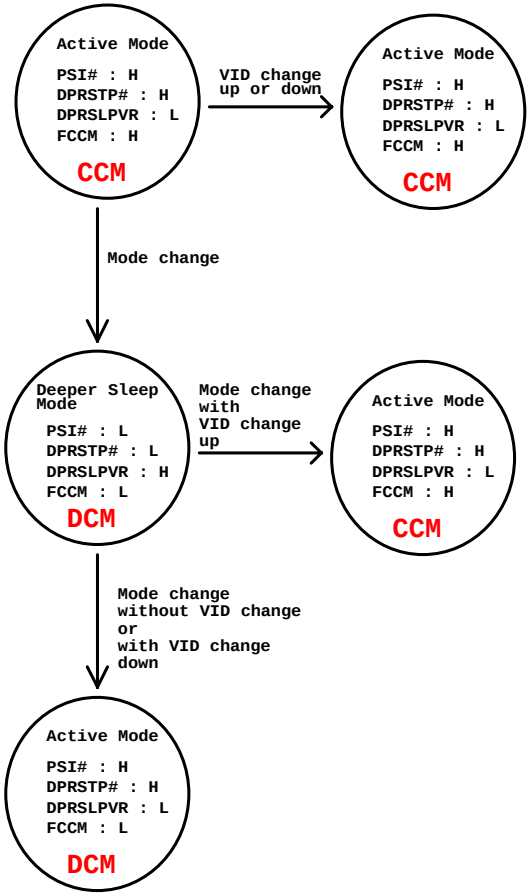
IMVP Spec. Rev. 0.8

(Nom.)	Yonah-2M	Meron
HFM	1.2875 V	1.1500 V
LFM	0.8375 V	0.8375 V
Deeper	0.7625 V	0.7625 V
VBOOT	1.2000 V	1.2000 V
SLOPE	-2.1 mV/A	-2.1 mV/A

(Max.)	Yonah-2M	Meron
HFM	36 A	44 A
LFM	9.5 A	12.5 A
Deeper	3.5 A	5.5 A
Dynamic	27 A	34.5 A
TDC	26 A	32 A

Vo	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.5000	0	0	0	0	0	0	0
1.4375	0	0	0	0	1	0	1
1.4000	0	0	0	1	0	0	0
1.3000	0	0	1	0	0	0	0
1.2875	0	0	1	0	0	0	1
1.2000	0	0	1	1	0	0	0
1.1500	0	0	1	1	1	0	0
1.1000	0	1	0	0	0	0	0
1.0000	0	1	0	1	0	0	0
0.9625	0	1	0	1	0	1	1
0.9000	0	1	1	0	0	0	0
0.8375	0	1	1	0	1	0	1
0.8000	0	1	1	1	0	0	0
0.7625	0	1	1	1	0	1	1
0.7500	0	1	1	1	1	0	0
0.7000	1	0	0	0	0	0	0
0.6000	1	0	0	1	0	0	0
0.5000	1	0	1	0	0	0	0
0.3000	1	1	0	0	0	0	0

CCM : Continuous Conduction Mode
DCM : Dis-Continuous Mode



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MA7 / Schematic EC Tracking Record A (for A-Test-> B Test) Oct. 28, 2005

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