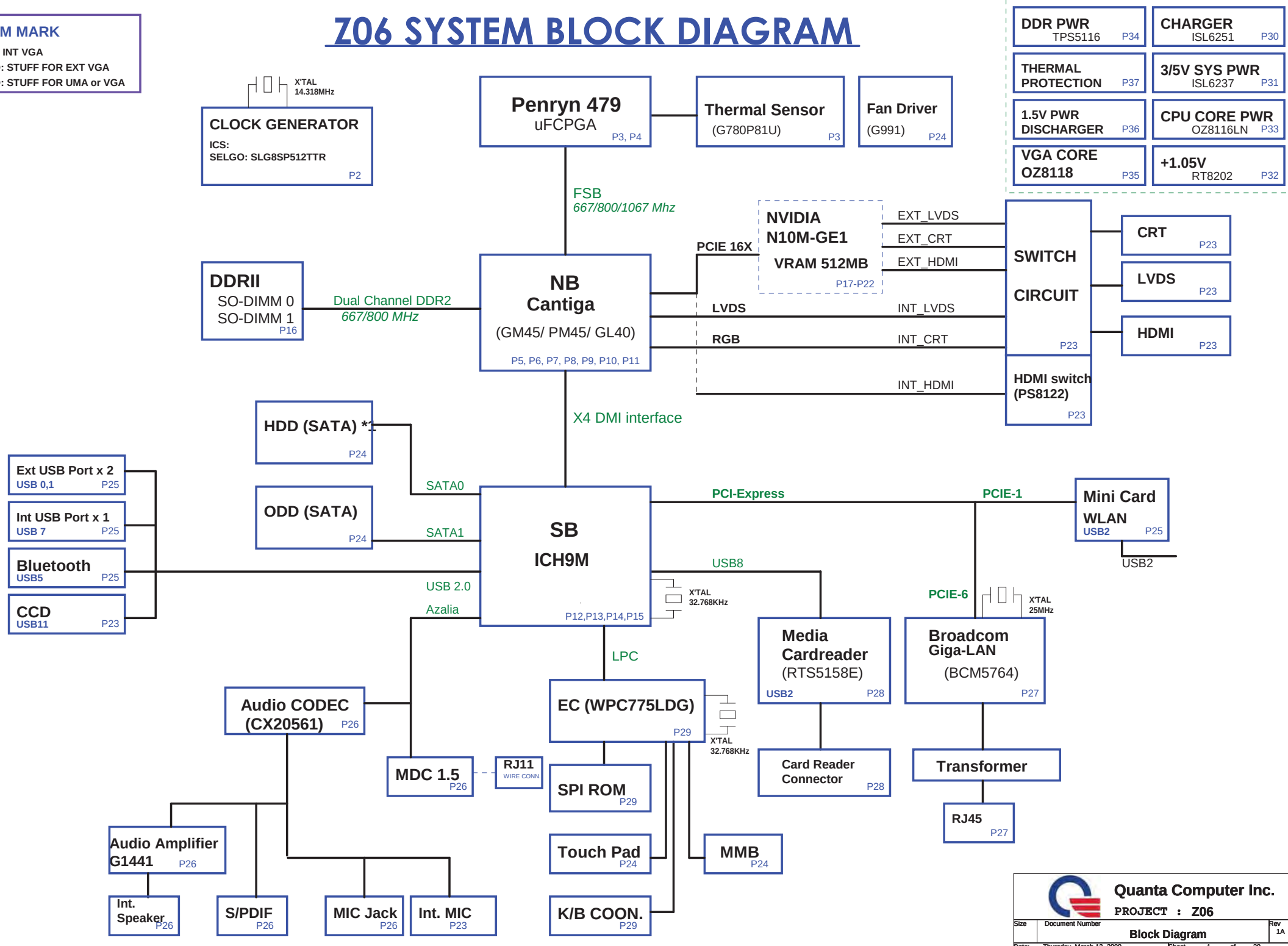
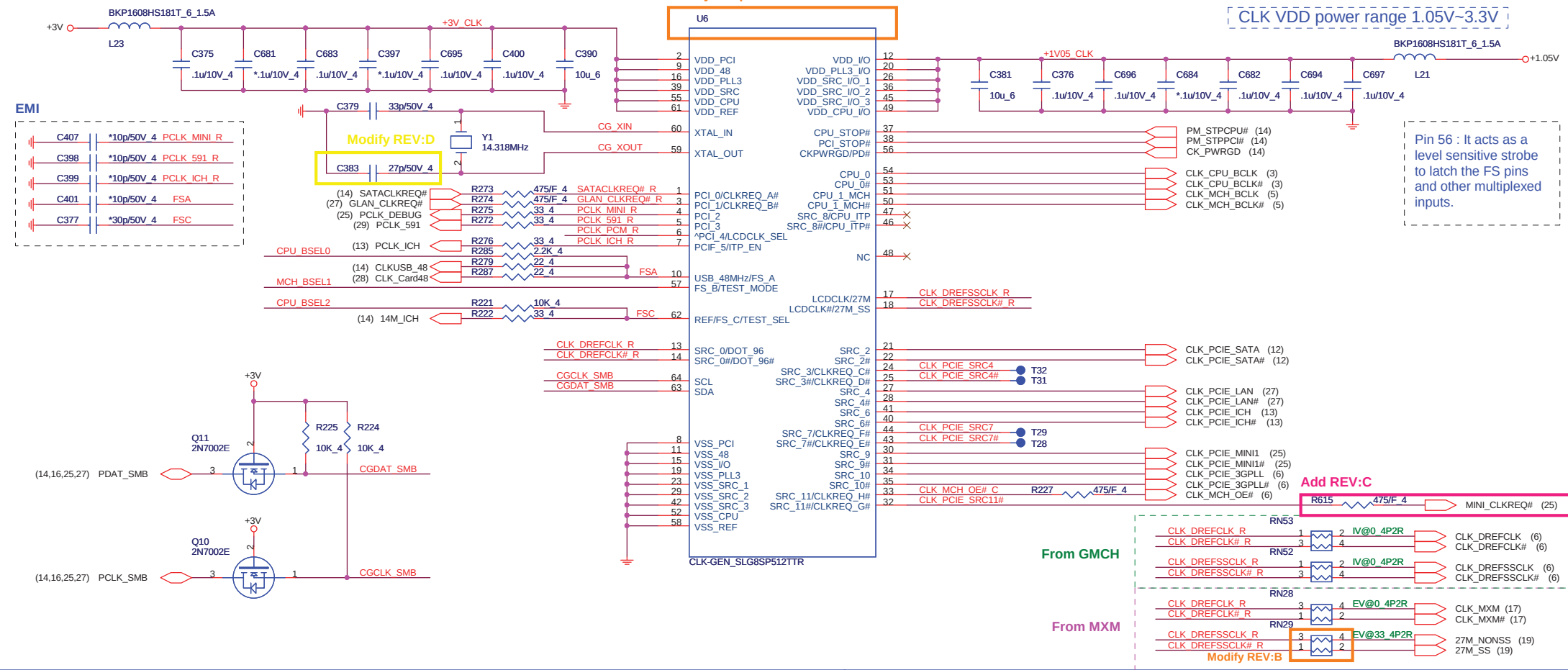


Z06 SYSTEM BLOCK DIAGRAM

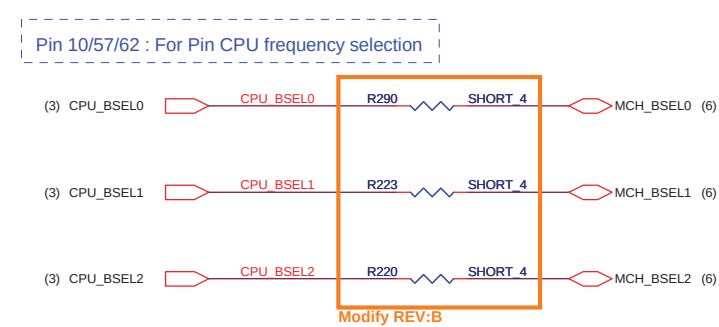
BOM MARK
IV@: INT VGA
EV@: STUFF FOR EXT VGA
SP@: STUFF FOR UMA or VGA



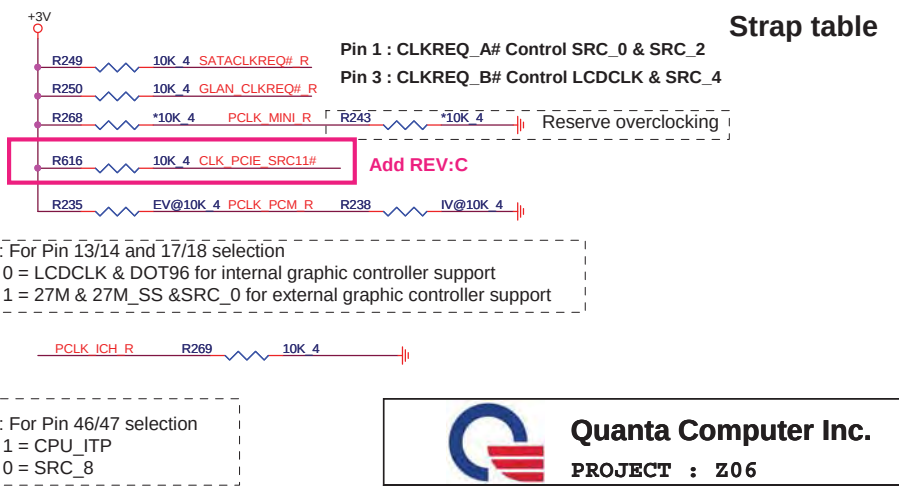
Clock Generator



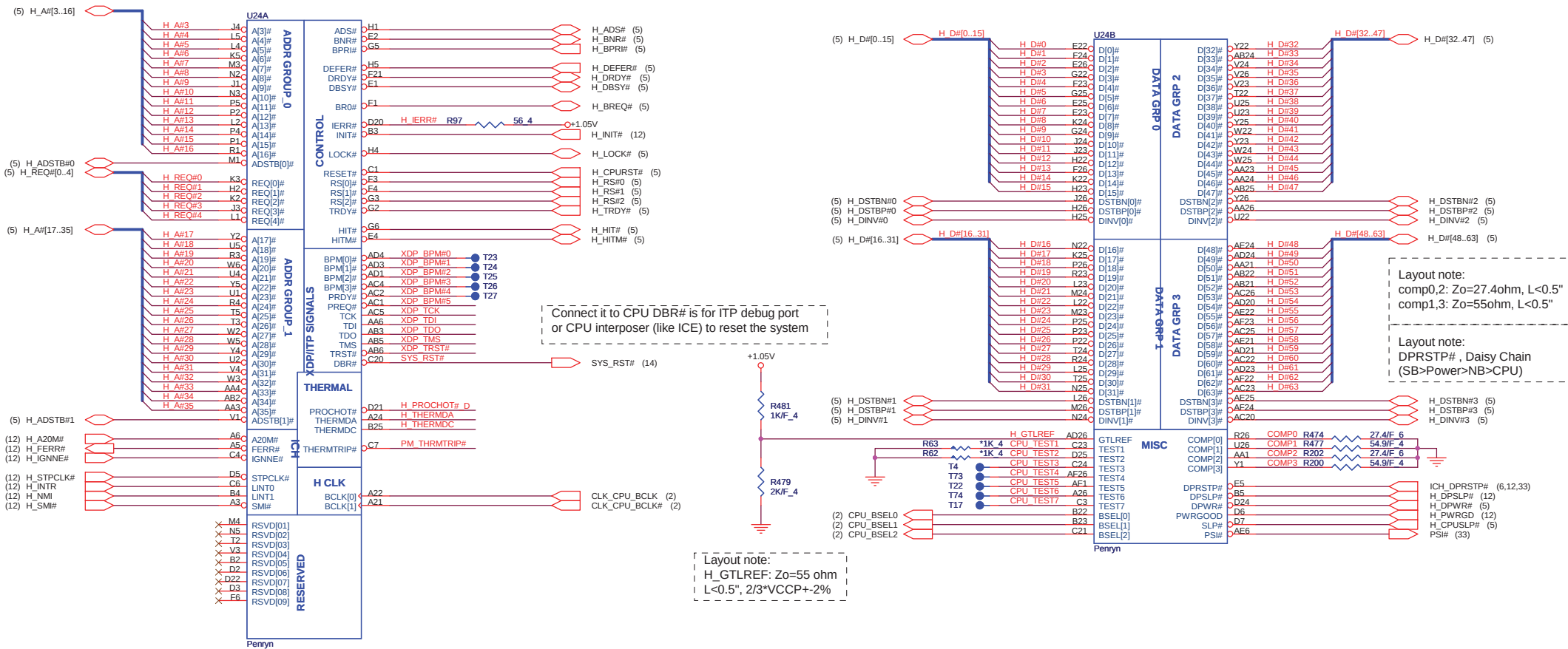
CPU Clock select



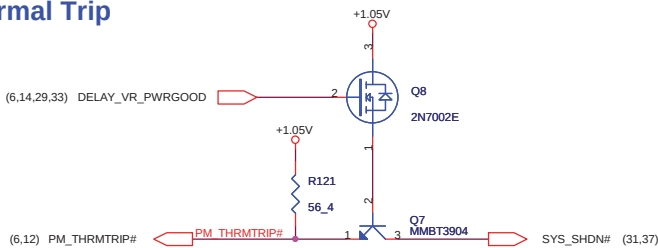
BSEL Frequency Select Table			
FSC	FSB	FSA	Frequency
0	0	0	266Mhz
0	0	1	133Mhz
0	1	1	166Mhz
0	1	0	200Mhz
1	1	0	400Mhz
1	1	1	Reserved
1	0	1	100Mhz
1	0	0	333Mhz



CLOCK GENERATOR



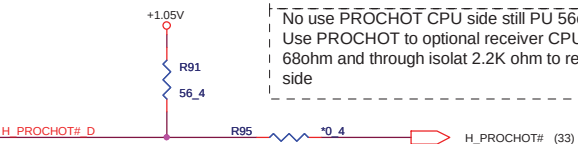
Thermal Trip



Processor hot

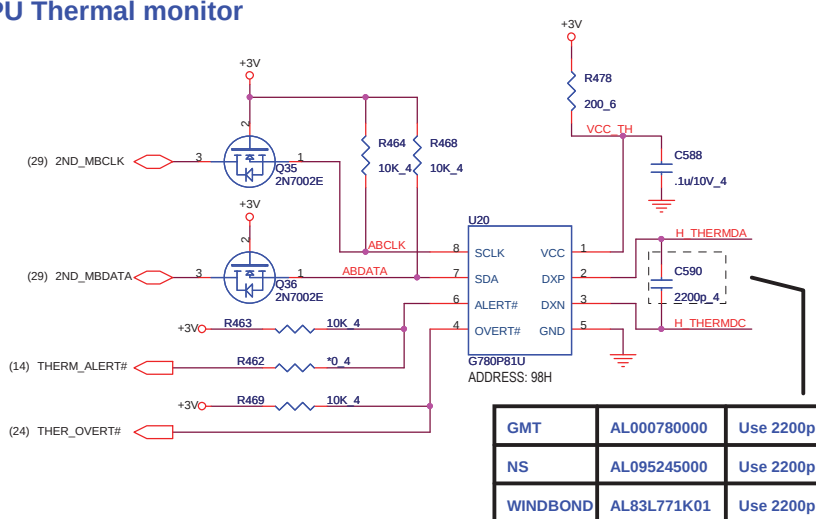
No use Thermal trip CPU side still PU 56ohm.
Use Thermal trip can share PU at SB side

No use PROCHOT CPU side still PU 56ohm.
Use PROCHOT to optional receiver CPU side PU 68ohm and through isolat 2.2K ohm to receiver side

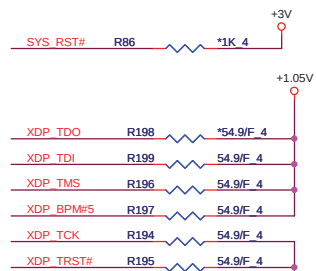


CPU 1/2

CPU Thermal monitor



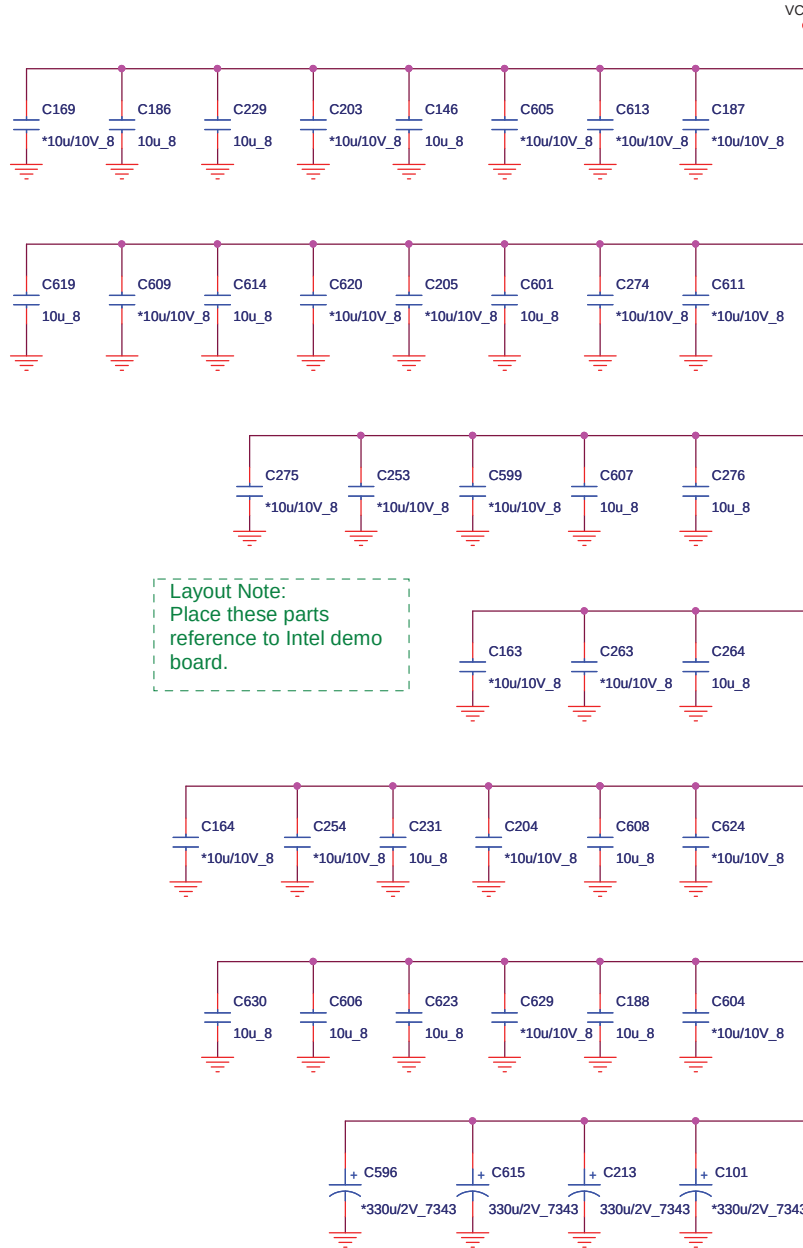
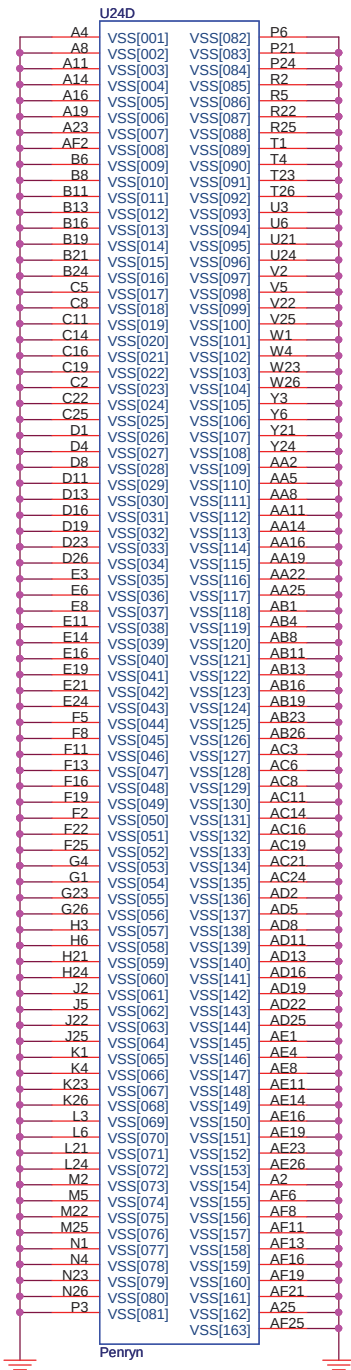
XDP PU/PD



XDP_DBRESET# and XDP_TDO reserve for XDP

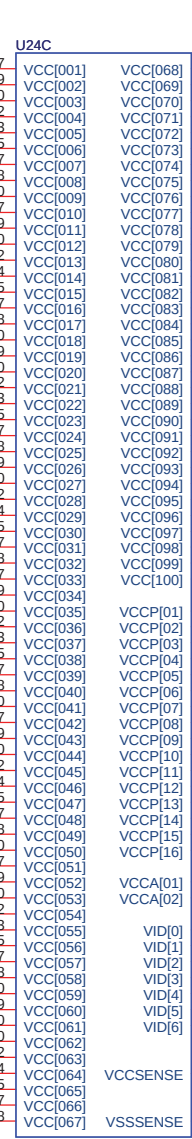


Quanta Computer Inc.
PROJECT : Z06



Layout Note:
Place these parts
reference to Intel demo
board.

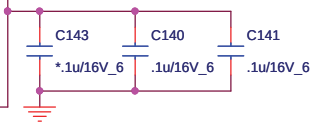
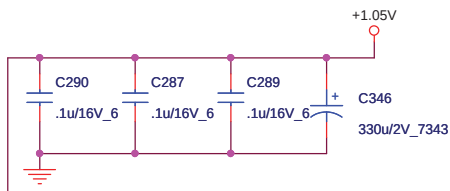
Montevina platform : Early Reference Board Schematics Feb 2007. Rev 1.0
stuff 22U*34, NC 22U*2
stuff 330U*2, NC330U*2



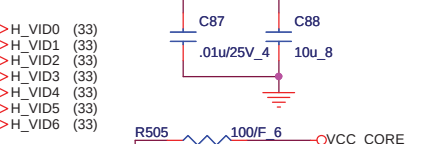
VCC:38A (Low power type)
VCC:47A (Standard type)

Layout Note:
Inside CPU center cavity in 2 rows

VCCP : 2.5A(Supply after VCC Stable)
4.5A(Supply before VCC Stable)



VCCA:130mA

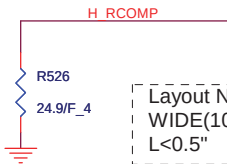
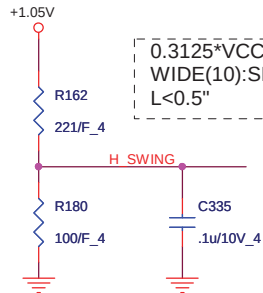


Layout Note:
Z0=27.4,PU/PD L<1"



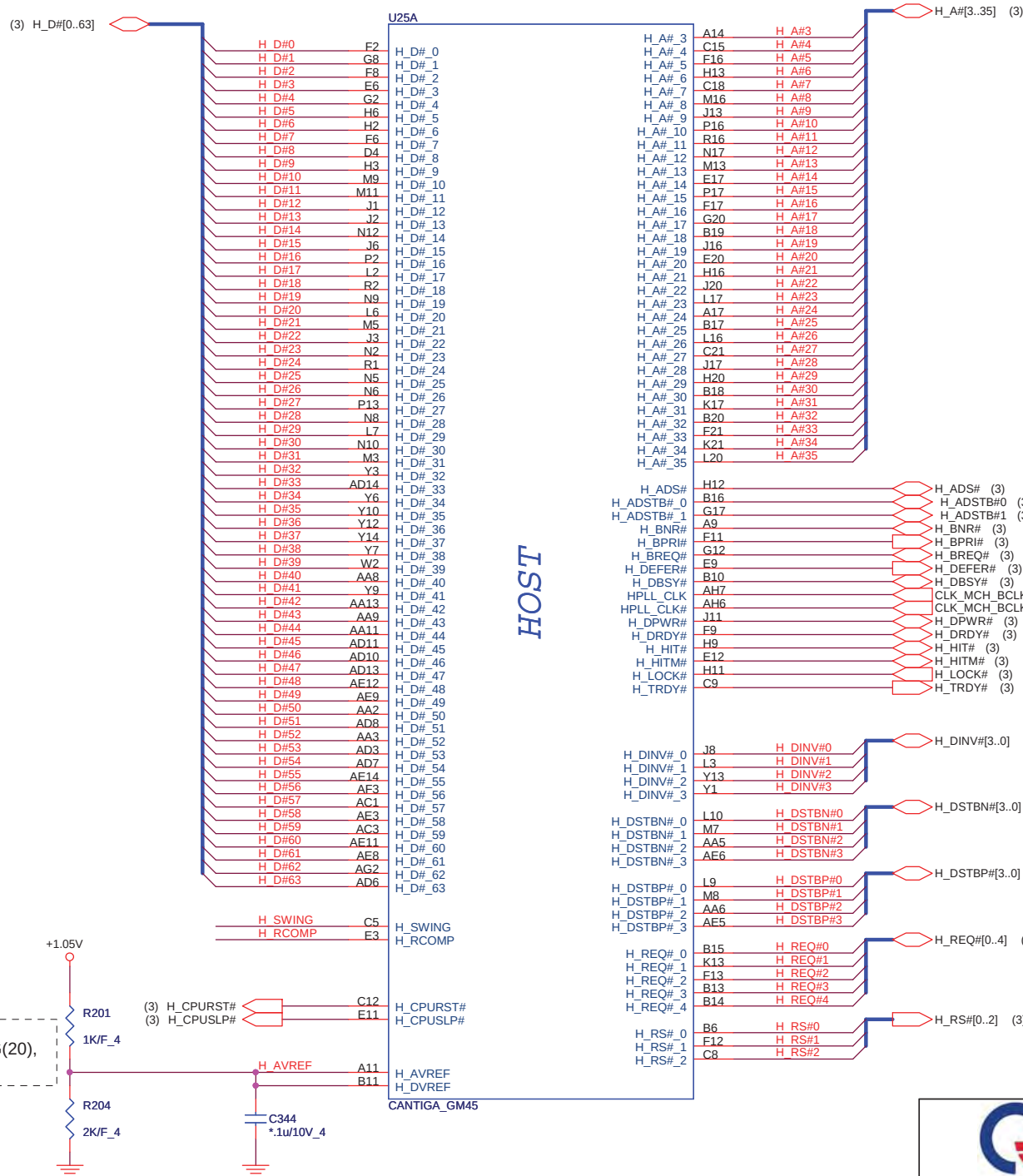
Quanta Computer Inc.
PROJECT : Z06

U25	QCI P/N
Intel Cantiga GM45-B3	AJSLB940T04
Intel Cantiga PM45-B3	AJSLB970T06
Intel Cantiga GL40-A1	AJSLGGM0T04



Layout Note:
WIDE(10):SPACING(20),
L<0.5"

$\frac{2}{3} * VCCP$
WIDE(10):SPACING(20),
L<0.5"



Quanta Computer Inc.

PROJECT : Z06

Size	Document Number	Rev 1A
Date: Thursday, March 12, 2009	GMCH HOST	

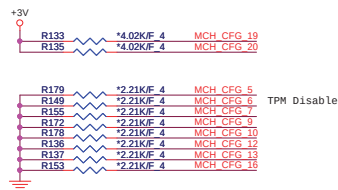
Sheet 5 of 39

GMCH (CANTIGA)

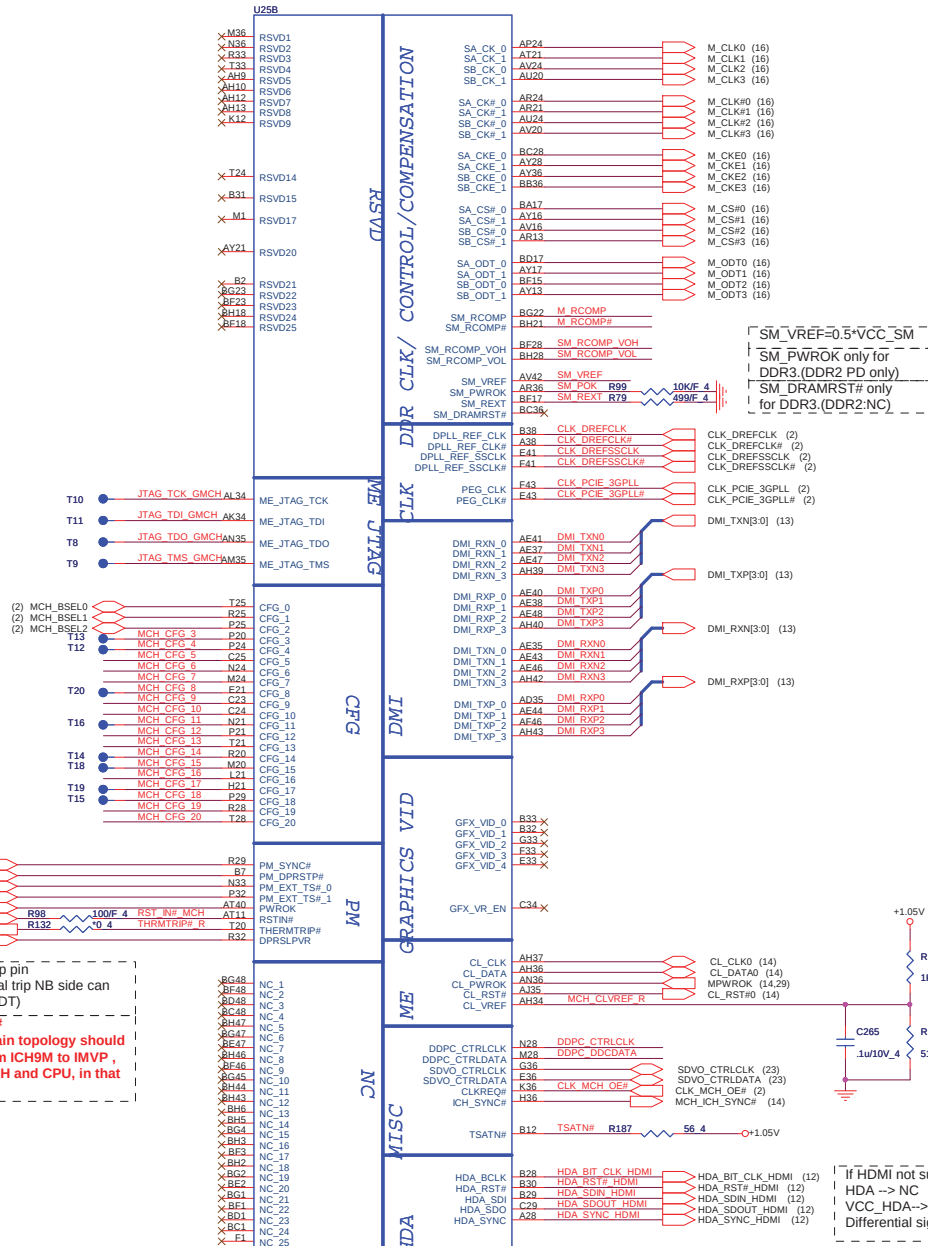
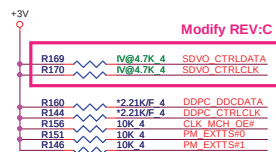
Strap table

Pin Name	Strap description	Configuration
CFG[2:0]	FSB Frequency Select	000= FSB 1066MHz 010 = FSB 800MHz 011 = FSB 667MHz
CFG[4:3]	Reserved	
CFG5	DMI X2 Select	0 = DMI X2 1 = DMI X4(Default)
CFG6	iTPM Host Interface	0 = iTPM Host Interface is enabled 1 = iTPM Host Interface is disabled(Default)
CFG7	ME TLS Confidentiality	0 = AMT Firmware will use TLS cipher suite with no confidentiality 1 = AMT Firmware will use TLS cipher suite with confidentiality(Default)
CFG8	Reserved	
CFG9	PCIe Graphics Lane Reversal	0 = Reverse Lanes 1 = Normal operation(Default)
CFG10	PCIe Loopback enable	0 = Enabled 1 = Disabled (Default)
CFG11	Reserved	
CFG12	ALLZ	0 = ALLZ mode enable 1 = disable(Default)
CFG13	XOR	0 = XOR mode enable 1 = disable(Default)
CFG[15:14]	Reserved	
CFG16	FSB Dynamic ODT	0 = Dynamic ODT disable 1 = Dynamic ODT Enable(Default)
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	0 = Normal (Default) 1 = Lanes Reversed
CFG20	Digital Display Port (SDVO/DP/iHDMI) Concurrent with PCIe	0 = Only Digital Display port (SDVO/DP/iHDMI) or PCIe is operational (Default) 1 = Digital Display port (SDVO/DP/iHDMI) and PCIe are operating simultaneously via PEG port
SDVO_CTRLDATA	SDVO Present	0 = No SDVO/HDMI Device Present(Default) 1 = SDVO/HDMI Device present
DDPC_CTRLDATA	Digital Display Present	0 = Digital display(HDMI/DP) device absent(Default) 1 = Digital display(HDMI/DP) device present

Strap pin

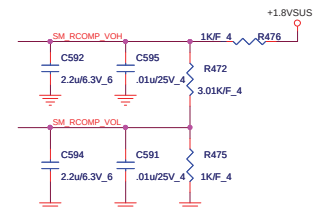


Modify REV:C

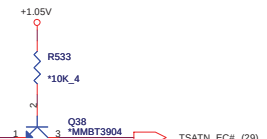


SM_VREF.Default use voltage divider for
poor layout cause +SMDDR_VREF not
meet spec.And Intel circuit PU/PD is
1K,But Check list PU/PD is 10K.

INTEL FAE Suggest PD for Ext graphics



NB Thermaltrip



Check list note : $\overline{CL_VREF}=0.35V$

```

┌ DDPC_CTRL for HDMI port C ─┐
└ SDVO_CTRL for HDMI port B ┘

```

<Checklist ver0.8>

If TSATN# is not used, then it must be terminated with a 56- pull-up resistor to VCCP.

<Pin out check issue>

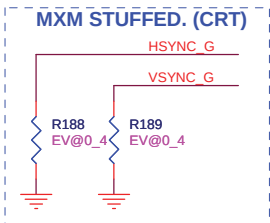
I Cantiga EDS 0.7 change Ball B12 to TSATN# from TSATN I

**Quanta Computer Inc.**

PROJECT : Z06

Size	Document Number	Rev
	GMCH DMI	1A
Date:	Thursday, March 12, 2009	Sheet 6 of 39

EV@ **IV&EV Dis/Enable setting**
If LVDS no use, all signal can N



PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
PEG_TX_8
PEG_TX_9
PEG_TX_10
PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

PEG_TX_0
PEG_TX_1
PEG_TX_2
PEG_TX_3
PEG_TX_4
PEG_TX_5
PEG_TX_6
PEG_TX_7
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PEG_TX_11
PEG_TX_12
PEG_TX_13
PEG_TX_14
PEG_TX_15

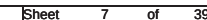
J42	C PEG TXP0	C348
L46	C PEG TXP1	C669
M48	C PEG TXP2	C673
M39	C PEG TXP3	C349
M43	C PEG TXP4	C333
R47	C PEG TXP5	C645
N37	C PEG TXP6	C352
T39	C PEG TXP7	C651
U36	C PEG TXP8	C637
U39	C PEG TXP9	C311
Y39	C PEG TXP10	C270
Y46	C PEG TXP11	C628
AA36	C PEG TXP12	C257
AA39	C PEG TXP13	C249
AD42	C PEG TXP14	C199
AD46	C PEG TXP15	C617

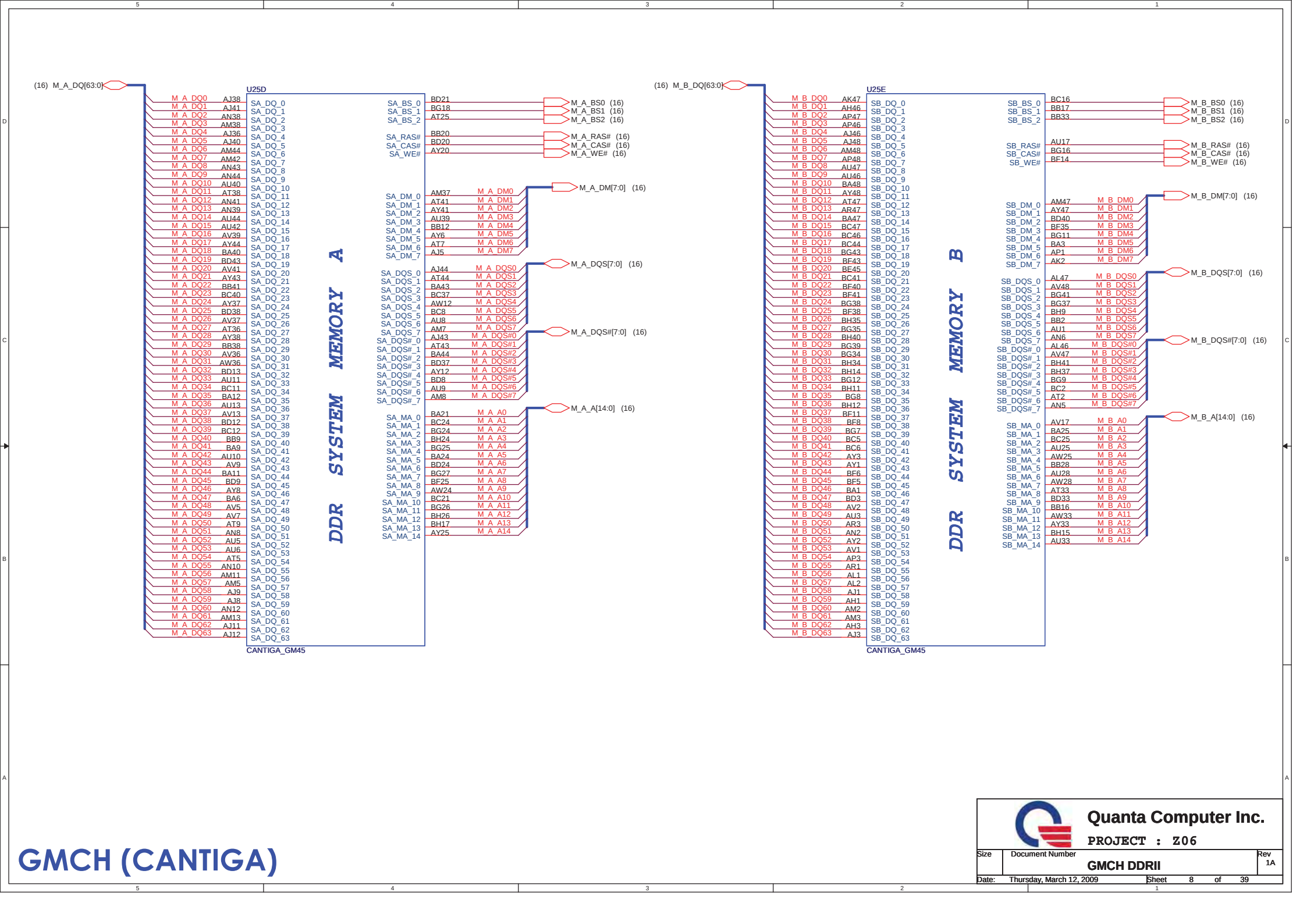
.1u10V 4	PEG	TXP0
.1u10V 4	PEG	TXP1
.1u10V 4	PEG	TXP2
.1u10V 4	PEG	TXP3
EV@.1u10V 4	PEG	TXP4
EV@.1u10V 4	PEG	TXP5
EV@.1u10V 4	PEG	TXP6
EV@.1u10V 4	PEG	TXP7
EV@.1u10V 4	PEG	TXP8
EV@.1u10V 4	PEG	TXP9
EV@.1u10V 4	PEG	TXP10
EV@.1u10V 4	PEG	TXP11
EV@.1u10V 4	PEG	TXP12
EV@.1u10V 4	PEG	TXP13
EV@.1u10V 4	PEG	TXP14
EV@.1u10V 4	PEG	TXP15

R185 SP@150/F 4 INT CRT BLU

R173 SP@150/F 4 INT CRT GRN

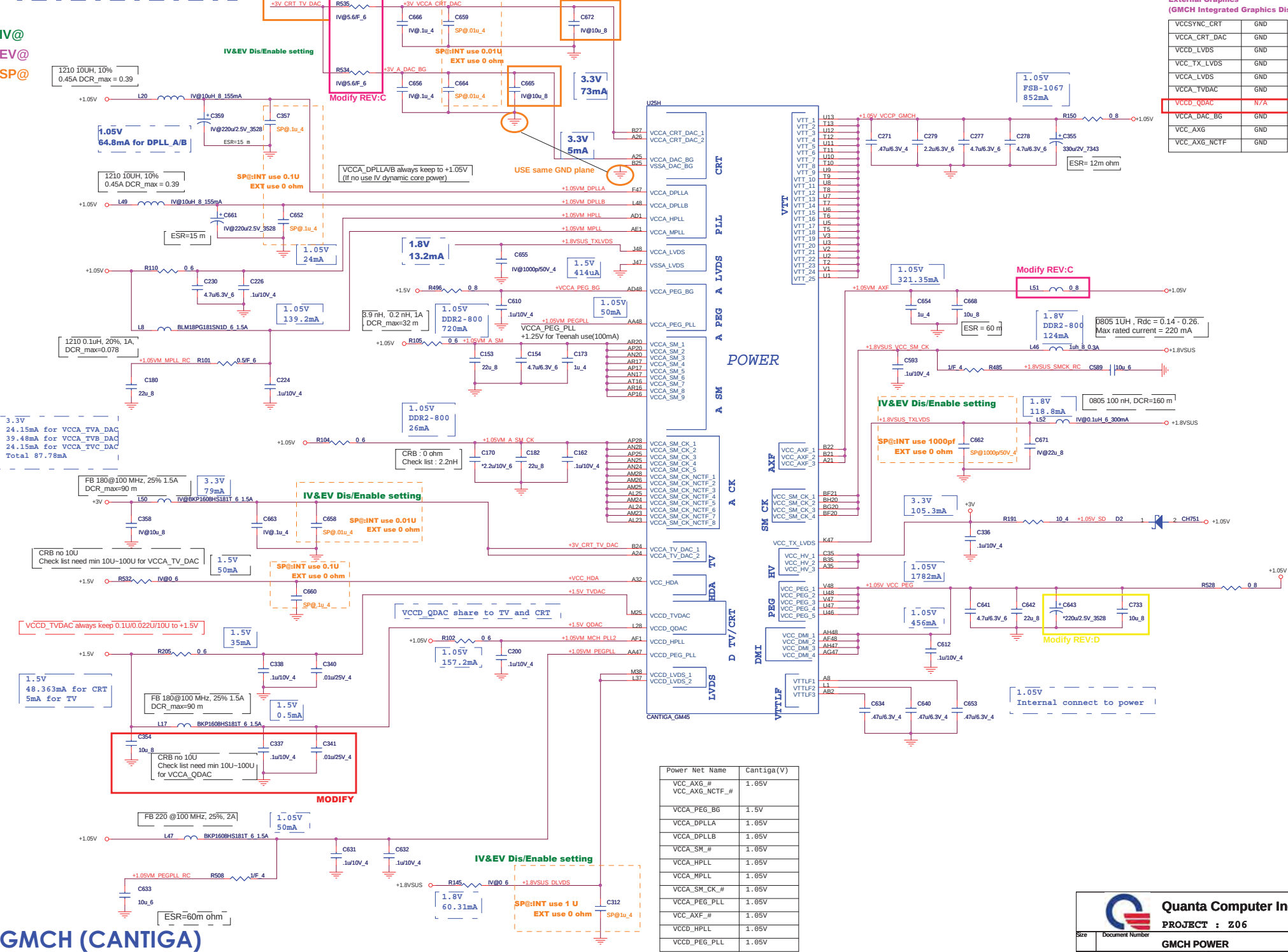
R164 SP@150/F 4 INT CRT RED





IV@
EV@
SP@

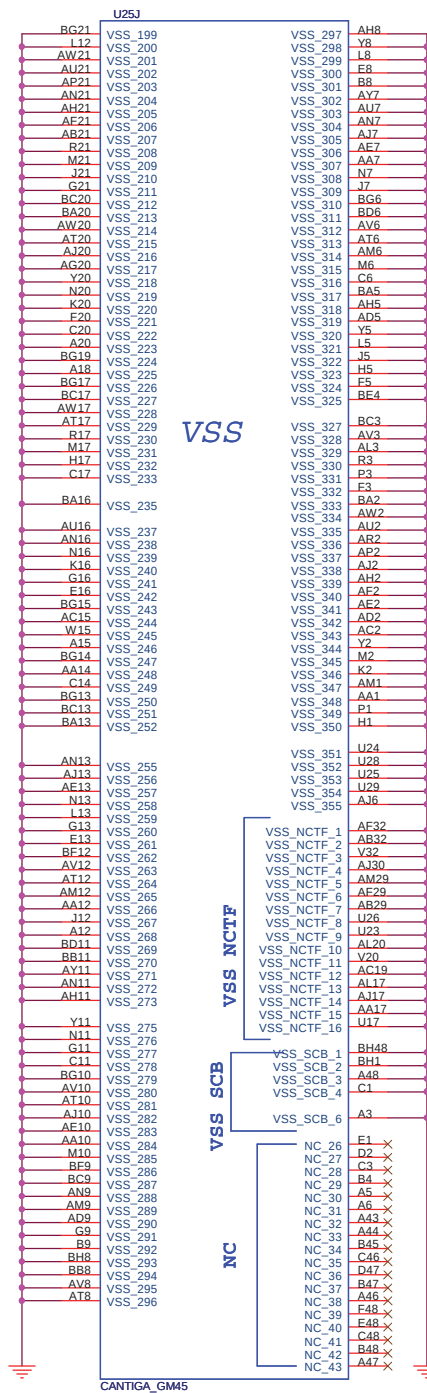
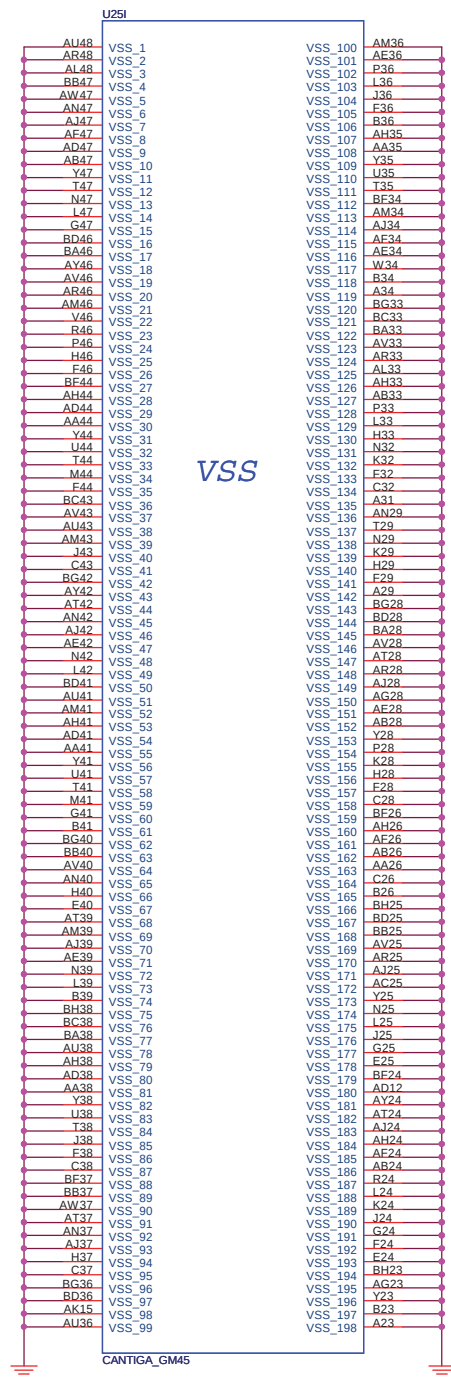
Power consumption reference to Intel
Cantiga_chipset_EDS_Volum1_Section_10



External Graphics
(GMCH Integrated Graphics Disable)

VCCSYNC_CRT	GND
VCCA_CRT_DAC	GND
VCCD_LVDS	GND
VCC_TX_LVDS	GND
VCCA_LVDS	GND
VCCA_TV_DAC	GND
VCCD_QDAC	N/A
VCCA_DAC_BG	GND
VCC_AXG	GND
VCC_AXG_NCTF	GND

GMCH (CANTIGA)

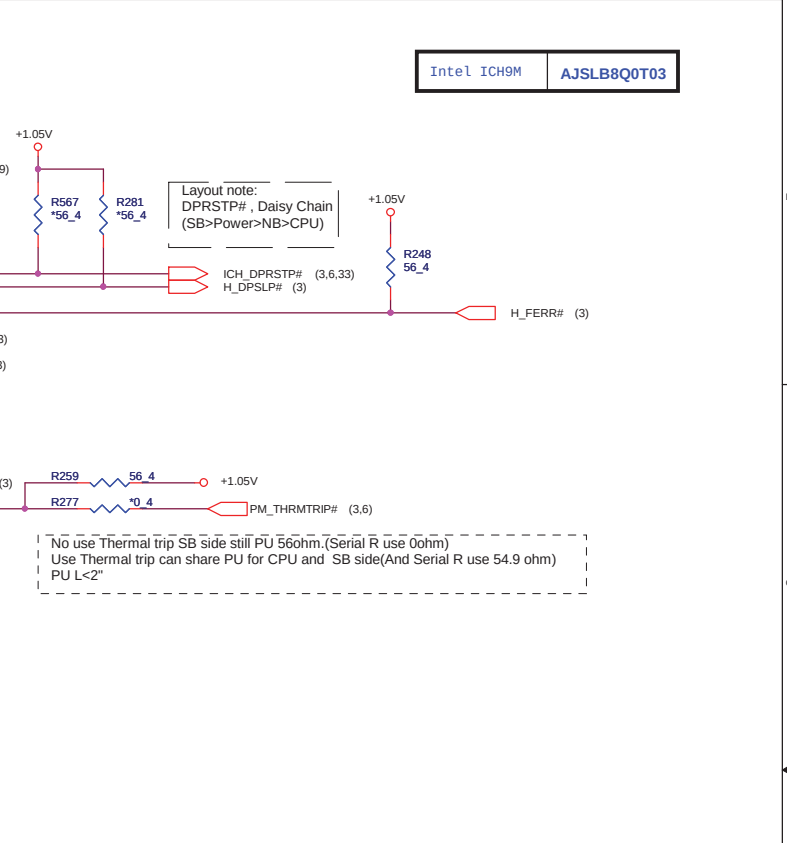
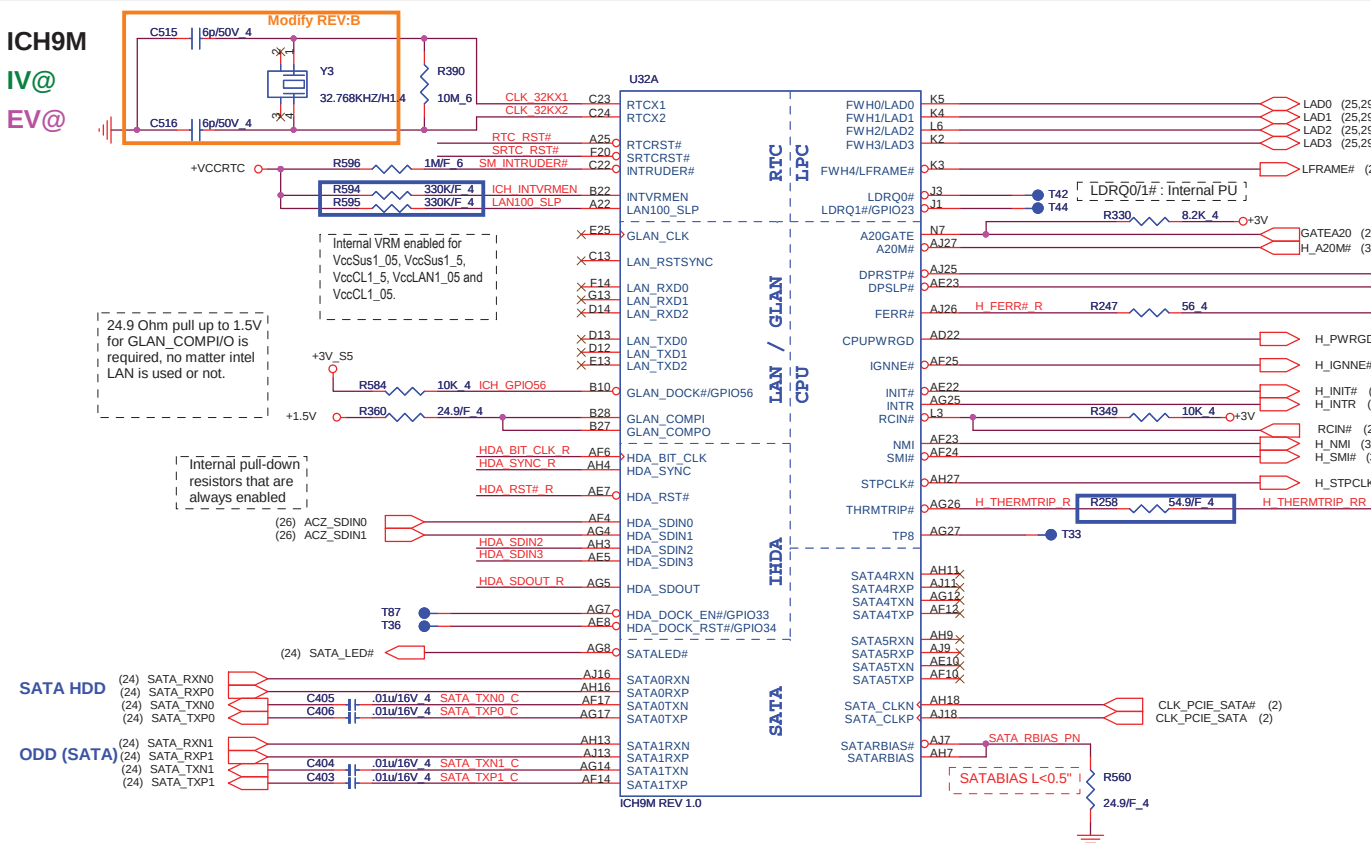


ICH9M

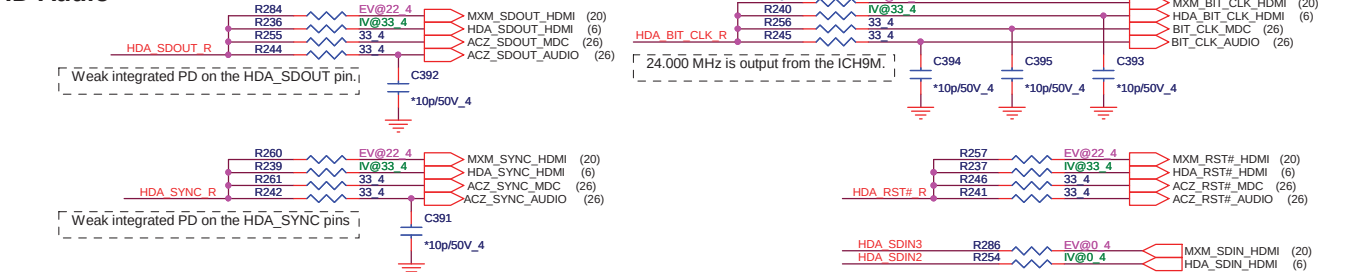
IV@

EV@

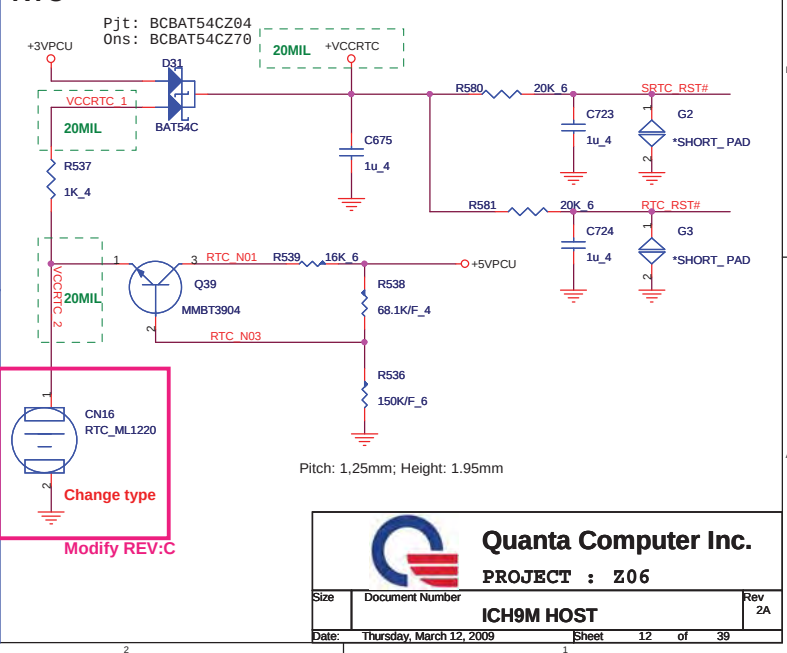
Intel ICH9M AJSLB8Q0T03



HD Audio



RTC

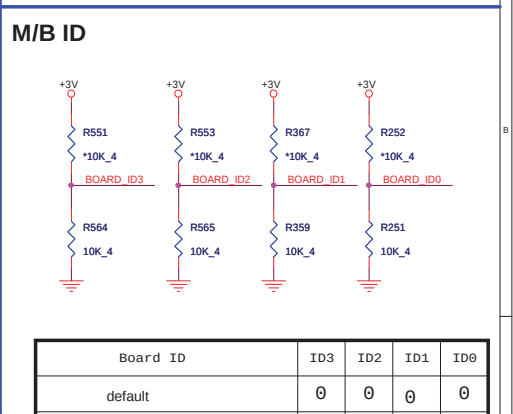
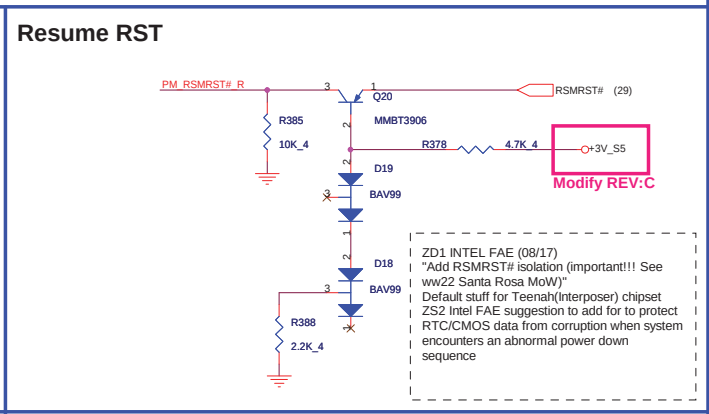
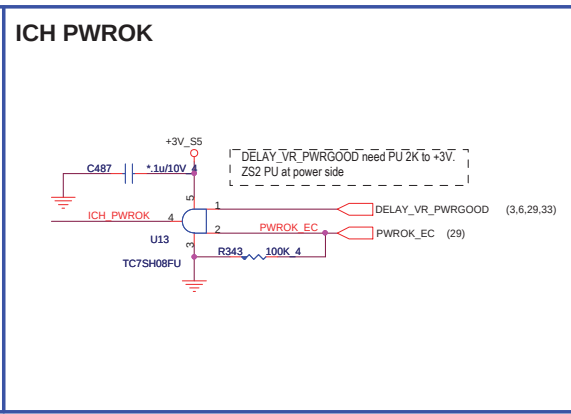
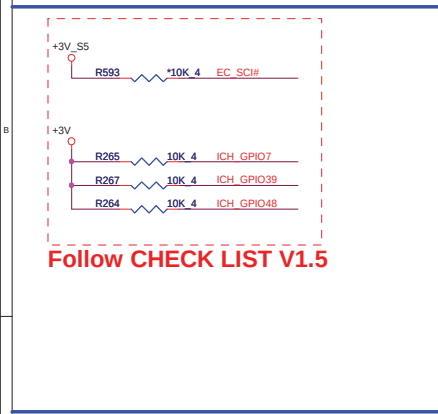
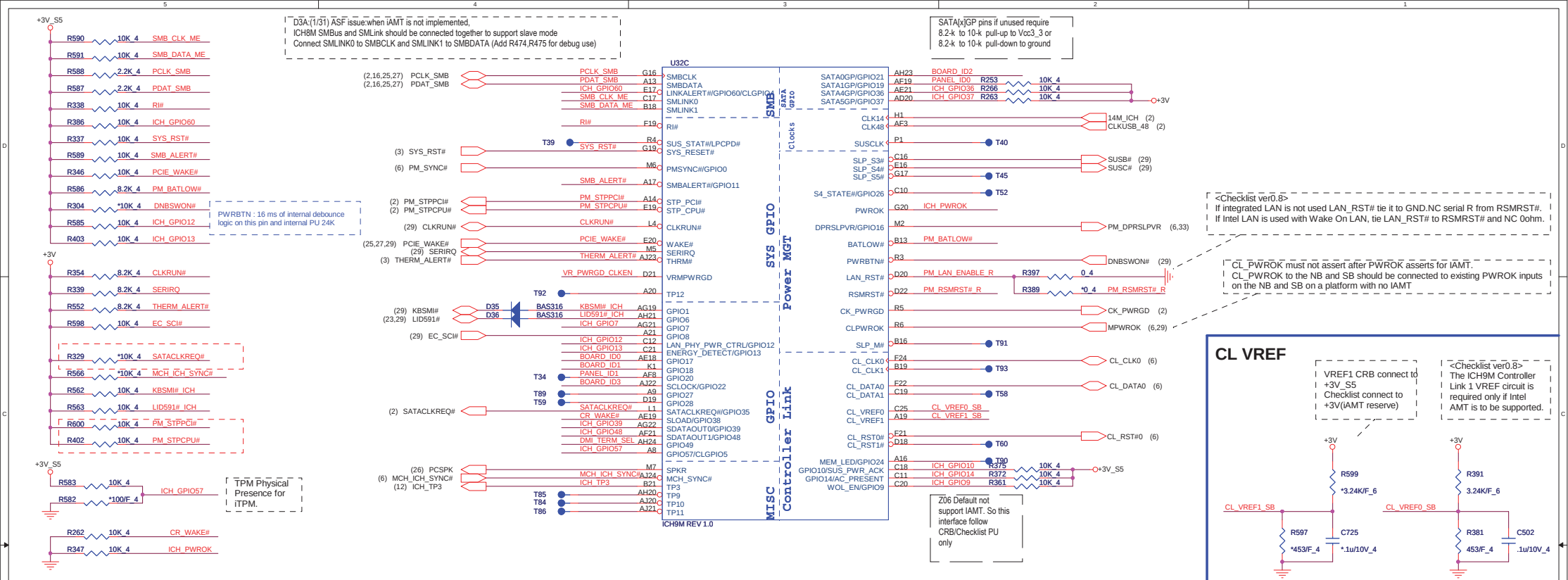


South Bridge Strap Pin (1/3)

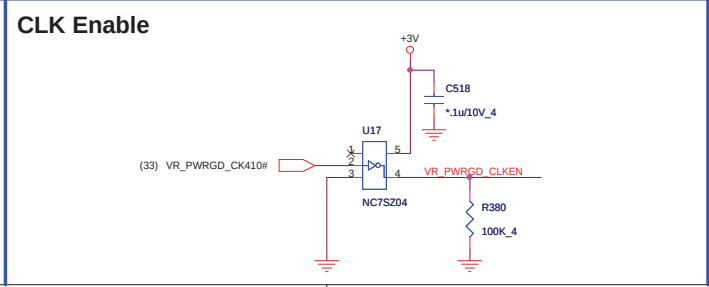
Pin Name	Strap description	Sampled	Configuration		PU/PD
HDA_DOCK_EN/ GPIO33	Flash Descriptor Security Override Strap	PWROK	0 = The Flash Descriptor Security will be overridden. 1 = The security measures defined in the Flash Descriptor will be in effect		This strap should only be enabled in manufacturing environments using an external pull-up resistor.
SATALED#	PCI Express Lane Reversal (Lanes 1-4)	PWROK	Internal PU		
TP3	XOR Chain Entrance	PWROK	ICH_TP3	HDA_SDOUT	Description
HDA_SDOUT	XOR Chain Entrance /PCI Express* Port Config 1 bit 1(Port 1-4)	PWROK	0	0	RSVD
			0	1	Enter XOR Chain
			1	0	Normal opration(Default)
			1	1	Set PCIE port config bit 1



Pin Name	Strap description	Sampled	Configuration			PU/PD
HDA_SYNC	PCI Express Port Config 1 bit 0 (Port 1-4)	PWROK	0 = Default 1 = Setting bit 0			
GNT2# / GPIO53	PCI Express Port Config 2 bit 2 (Port 5-6)	PWROK	0 = Setting bit 2 1 = Default			
GNT1# / GPIO51	ESI Strap(Server Only)	PWROK	0 = DMI for ESI-compatible 1 = Default			
GNT3# / GPIO55	Top-Block Swap Override	PWROK	0 = "top-block swap" mode 1 = Default			
SPI_MOSI	Integrated TPM Enable	CLPWROK	0 = INT TPM disable(Default) 1 = INT TPM enable			
GNT0#	Boot BIOS Selection 0	PWROK	PCI_GNT#0	SPI_CS#1	Boot Location	
			0	1	SPI	
SPI_CS1# / GPIO58 / CLGPIO6	Boot BIOS Selection 1	CLPWROK	1	0	PCI	
			1	1	LPC(Default)	



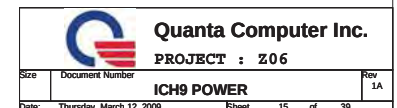
South Bridge Strap Pin (3/3)				
Pin Name	Strap description	Sampled	Configuration	PU/PD
GPIO20	Reserved	PWROK		
SPKR	No Reboot	PWROK	0 = Default 1 = No Reboot mode	PCSPK R316 *1K 4 +3V
GPIO49	DMI Termination Voltage	PWROK	0 = for desktop applications 1 = for mobile applications Internal PU	DMI_TERM_SEL R554 *1K 4



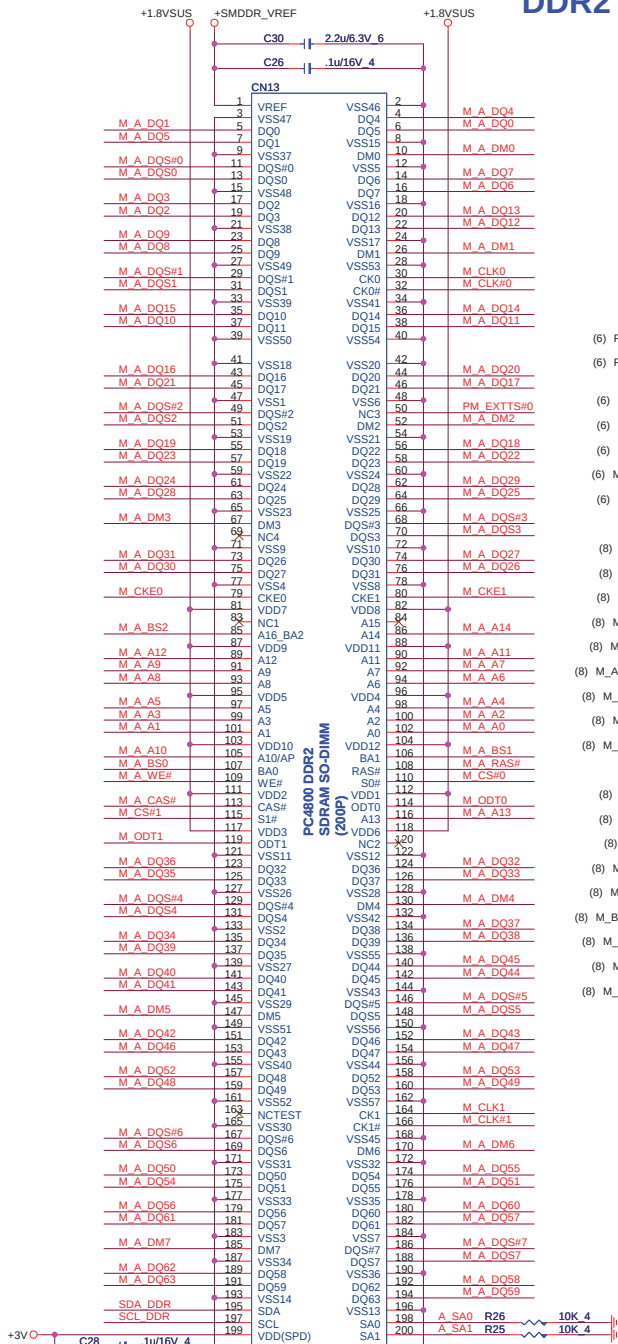
Quanta Computer Inc.
PROJECT : Z06

Size Document Number ICH9M GPIO Rev 1A

Date: Thursday, March 12, 2009 Sheet 14 of 39

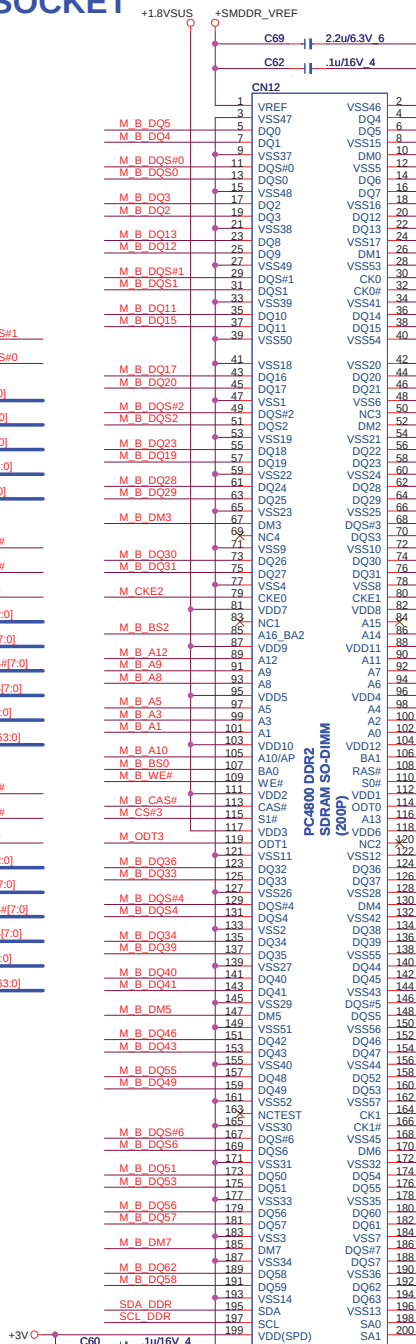


DDR2 SO-DIMM SOCKET



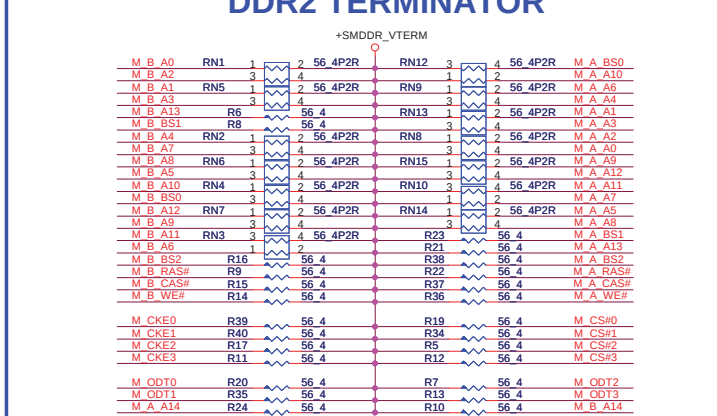
CLOCK 0,1,2
CKE 0,1

SMbus address A0

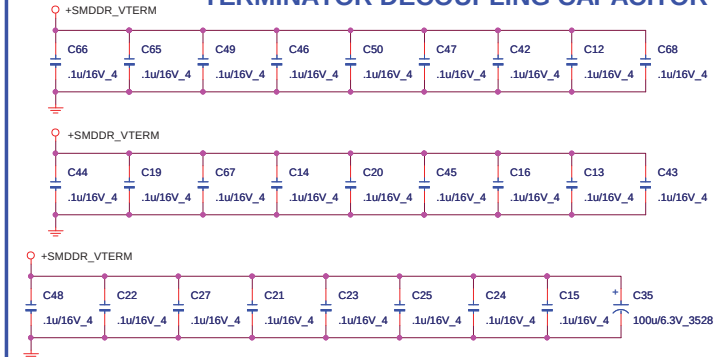


CLOCK 3,4,5
CKE 2,3

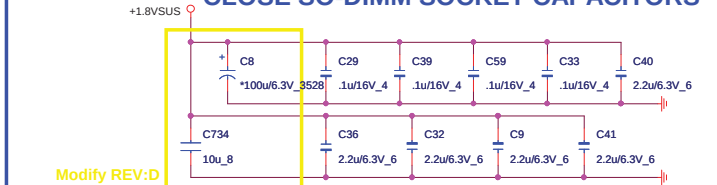
SMbus address A1



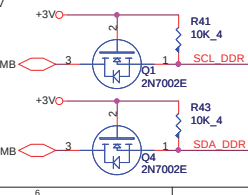
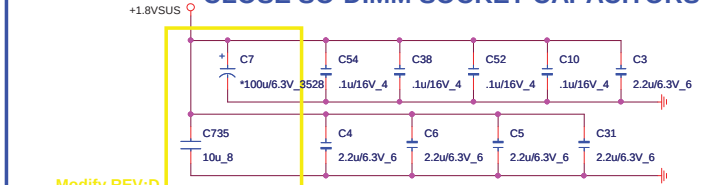
TERMINATOR DECOUPLING CAPACITOR

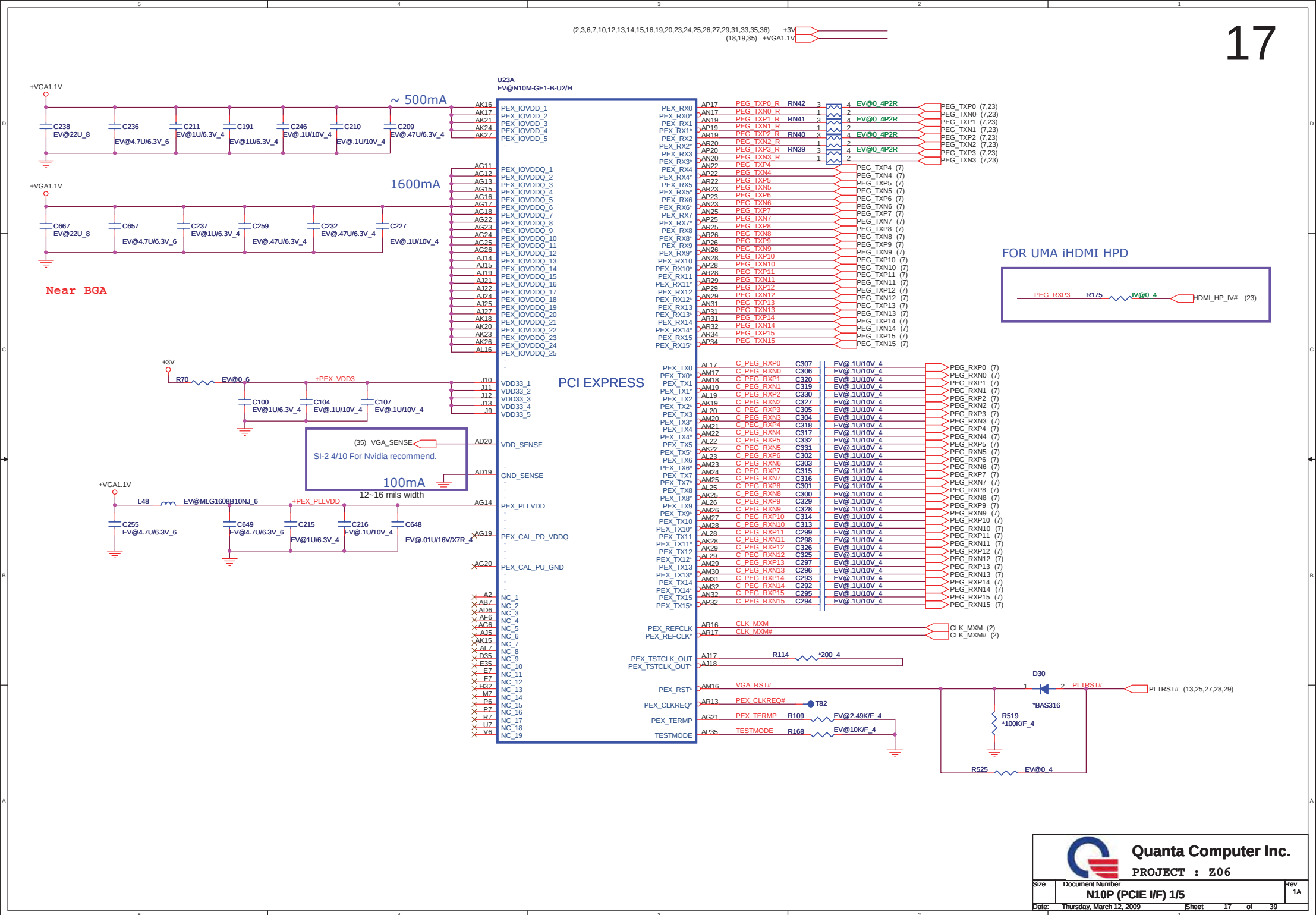


CLOSE SO-DIMM SOCKET CAPACITORS



CLOSE SO-DIMM SOCKET CAPACITORS

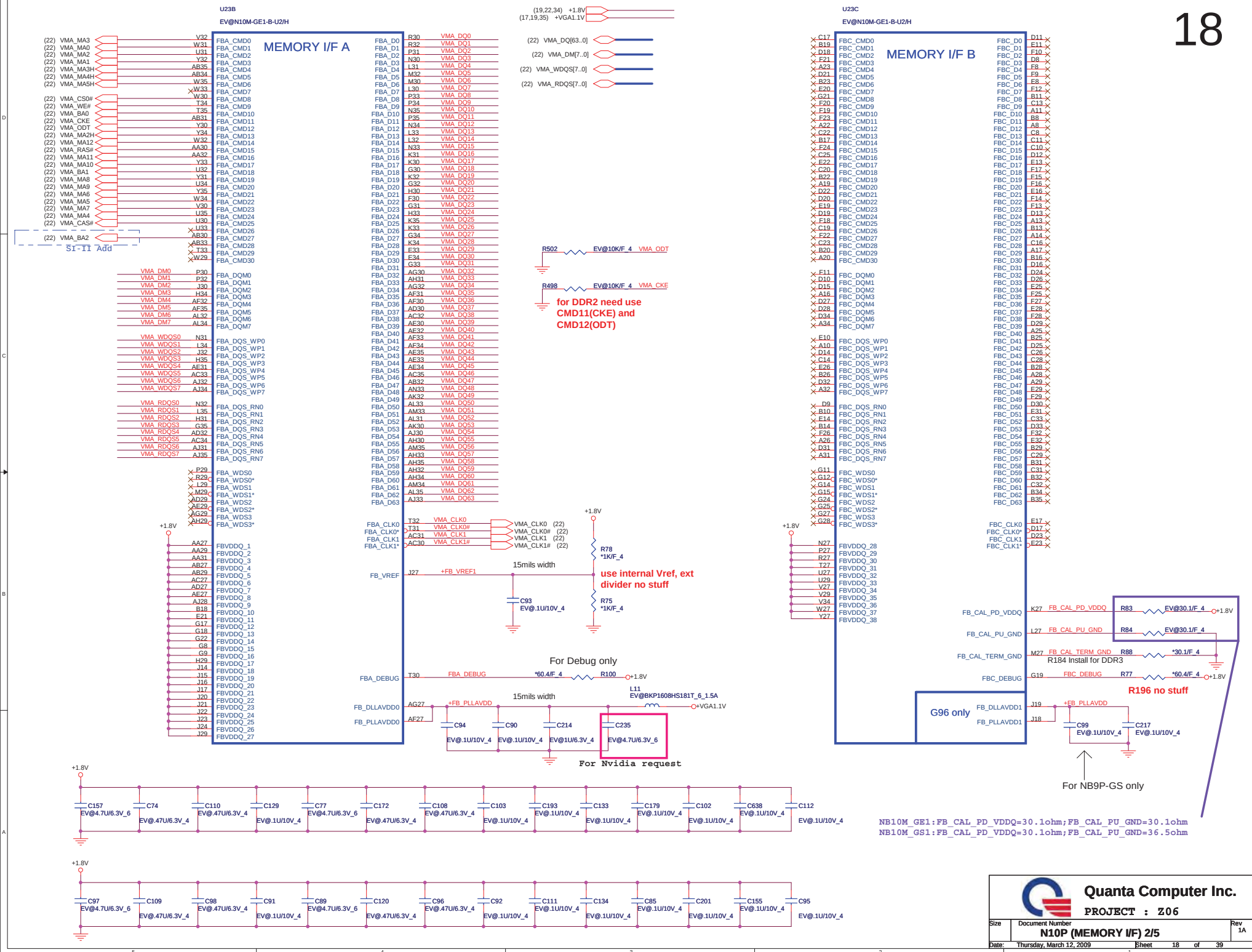




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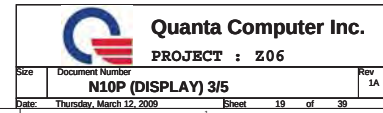
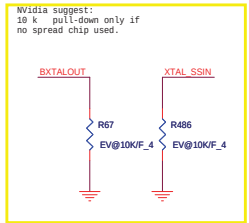
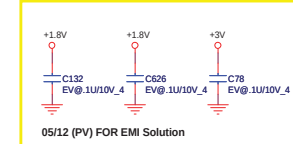
PROJECT : Z06

Size	Document Number	Rev
	N10P (PCIE I/F) 1/5	1A
Date:	Thursday, March 12, 2009	Sheet 17 of 39





STUFF PDs on XTALSSIN and XTALOUTBUFF WHEN EXT_SS IS NOT USED

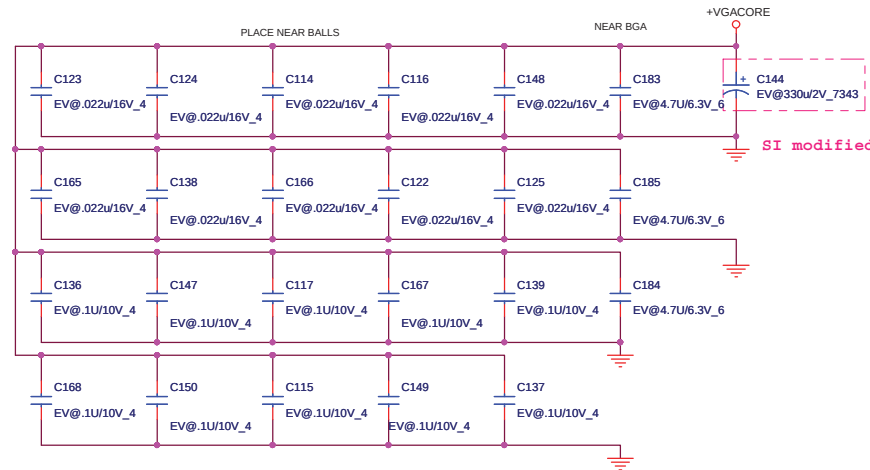


U23F

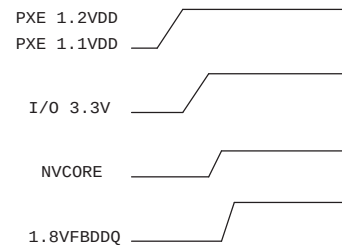
EV@N10M-GE1-B-U2/H

NVWDD

Module Pin	Function	Module Pin	Function	Module Pin	Function	Module Pin	Function
AB11	VDD_001	VDD_057	P21				
AB13	VDD_002	VDD_058	P23				
AB15	VDD_003	VDD_059	P25				
AB17	VDD_004	VDD_060	R12				
AB19	VDD_005	VDD_061	R13				
AB21	VDD_006	VDD_062	R14				
AB23	VDD_007	VDD_063	R15				
AB25	VDD_008	VDD_064	R16				
AC11	VDD_009	VDD_065	R17				
AC12	VDD_010	VDD_066	R18				
AC13	VDD_011	VDD_067	R19				
AC14	VDD_012	VDD_068	R20				
AC15	VDD_013	VDD_069	R21				
AC16	VDD_014	VDD_070	R22				
AC17	VDD_015	VDD_071	R23				
AC18	VDD_016	VDD_072	R24				
AC19	VDD_017	VDD_073	R25				
AC20	VDD_018	VDD_074	T12				
AC21	VDD_019	VDD_075	T14				
AC22	VDD_020	VDD_076	T16				
AC23	VDD_021	VDD_077	T18				
AC24	VDD_022	VDD_078	T20				
AC25	VDD_023	VDD_079	T22				
AD12	VDD_024	VDD_080	T24				
AD14	VDD_025	VDD_081	V11				
AD16	VDD_026	VDD_082	V13				
AD18	VDD_027	VDD_083	V15				
AD22	VDD_028	VDD_084	V17				
AD24	VDD_029	VDD_085	V19				
L11	VDD_030	VDD_086	V21				
L12	VDD_031	VDD_087	V23				
L13	VDD_032	VDD_088	V25				
L14	VDD_033	VDD_089	W11				
L15	VDD_034	VDD_090	W12				
L16	VDD_035	VDD_091	W13				
L17	VDD_036	VDD_092	W14				
L18	VDD_037	VDD_093	W15				
L19	VDD_038	VDD_094	W16				
L20	VDD_039	VDD_095	W17				
L21	VDD_040	VDD_096	W18				
L22	VDD_041	VDD_097	W19				
L23	VDD_042	VDD_098	W20				
L24	VDD_043	VDD_099	W21				
L25	VDD_044	VDD_100	W22				
M12	VDD_045	VDD_101	W23				
M14	VDD_046	VDD_102	W24				
M16	VDD_047	VDD_103	W25				
M18	VDD_048	VDD_104	Y12				
M20	VDD_049	VDD_105	Y14				
M22	VDD_050	VDD_106	Y16				
M24	VDD_051	VDD_107	Y18				
P11	VDD_052	VDD_108	Y20				
P13	VDD_053	VDD_109	Y22				
P15	VDD_054	VDD_110	Y24				
P17	VDD_055	VDD_111					
P19	VDD_056						

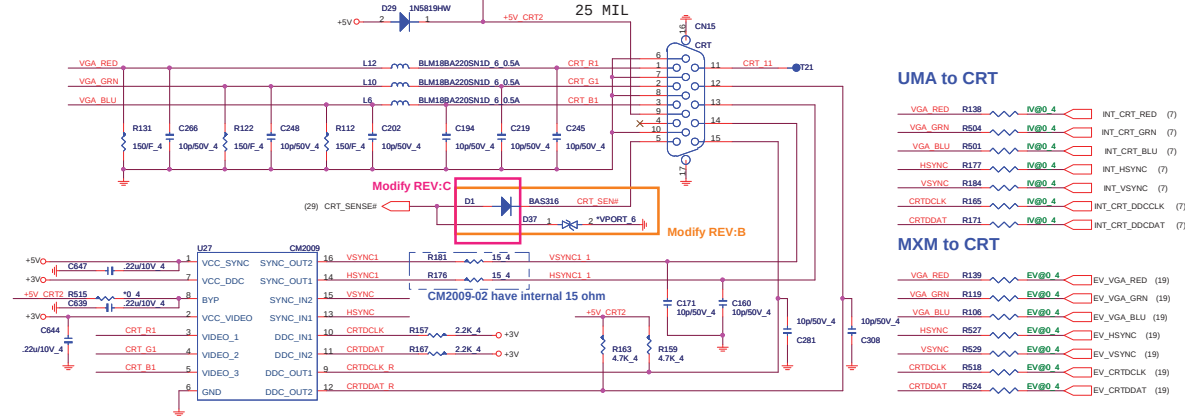


NB9M: VGACORE +0.90V (Normal) , +1.09V

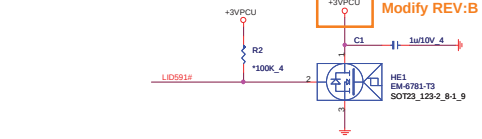


A111	GND 1	GND 096	F15
A112	GND 2	GND 097	F18
A113	GND 3	GND 098	E27
A114	GND 4	GND 099	E22
A115	GND 5	GND 100	E30
A116	GND 6	GND 101	E6
A117	GND 7	GND 102	E9
A118	GND 8	GND 103	F2
A119	GND 9	GND 104	F31
A12	GND 10	GND 105	F34
A120	GND 11	GND 106	F5
A121	GND 12	GND 107	J2
A122	GND 13	GND 108	J31
A123	GND 14	GND 109	J34
A124	GND 15	GND 110	L9
A125	GND 16	GND 111	M11
A126	GND 17	GND 112	M13
A127	GND 18	GND 113	M15
A128	GND 19	GND 114	M17
A129	GND 20	GND 115	M19
A130	GND 21	GND 116	M2
A131	GND 22	GND 117	M22
A132	GND 23	GND 118	M21
A133	GND 24	GND 119	M25
A134	GND 25	GND 120	M3
A135	GND 26	GND 121	M34
A136	GND 27	GND 122	M35
A137	GND 28	GND 123	M5
A138	GND 29	GND 124	N11
A139	GND 30	GND 125	N13
A140	GND 31	GND 126	N14
A141	GND 32	GND 127	N15
A142	GND 33	GND 128	N16
A143	GND 34	GND 129	N17
A144	GND 35	GND 130	N18
A145	GND 36	GND 131	N19
A146	GND 37	GND 132	N20
A147	GND 38	GND 133	N21
A148	GND 39	GND 134	N22
A149	GND 40	GND 135	N23
A150	GND 41	GND 136	N24
A151	GND 42	GND 137	N25
A152	GND 43	GND 138	P12
A153	GND 44	GND 139	P14
A154	GND 45	GND 140	P16
A155	GND 46	GND 141	P18
A156	GND 47	GND 142	P20
A157	GND 48	GND 143	P22
A158	GND 49	GND 144	P24
A159	GND 50	GND 145	P2
A160	GND 51	GND 146	R31
A161	GND 52	GND 147	R34
A162	GND 53	GND 148	R35
A163	GND 54	GND 149	T11
A164	GND 55	GND 150	T13
A165	GND 56	GND 151	T15
A166	GND 57	GND 152	T17
A167	GND 58	GND 153	T19
A168	GND 59	GND 154	T21
A169	GND 60	GND 155	T23
A170	GND 61	GND 156	T25
A171	GND 62	GND 157	T27
A172	GND 63	GND 158	T29
A173	GND 64	GND 159	T31
A174	GND 65	GND 160	T34
A175	GND 66	GND 161	T35
A176	GND 67	GND 162	T37
A177	GND 68	GND 163	T39
A178	GND 69	GND 164	T41
A179	GND 70	GND 165	T43
A180	GND 71	GND 166	T45
A181	GND 72	GND 167	T47
A182	GND 73	GND 168	T49
A183	GND 74	GND 169	T51
A184	GND 75	GND 170	T53
A185	GND 76	GND 171	T55
A186	GND 77	GND 172	T57
A187	GND 78	GND 173	T59
A188	GND 79	GND 174	T61
A189	GND 80	GND 175	T63
A190	GND 081	GND 176	T65
A191	GND 082	GND 177	T67
A192	GND 083	GND 178	T69
A193	GND 084	GND 179	T71
A194	GND 085	GND 180	T73
A195	GND 086	GND 181	T75
A196	GND 087	GND 182	T77
A197	GND 088	GND 183	T79
A198	GND 089	GND 184	T81
A199	GND 090	GND 185	T83
A200	GND 091	GND 186	T85
A201	GND 092	GND 187	T87
A202	GND 093	GND 188	T89
A203	GND 094	GND 189	T91
A204	GND 095	GND 190	T93
A205		GND 191	T95

CRT



Lid Switch

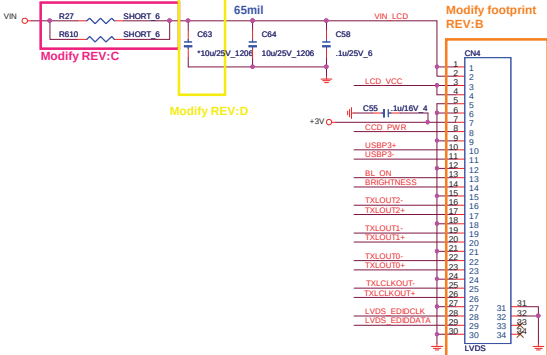


BRIGHTNESS

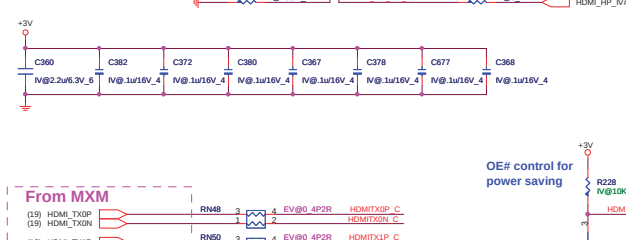
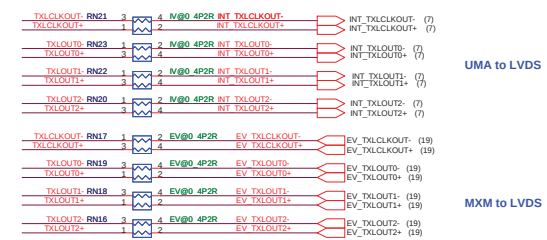
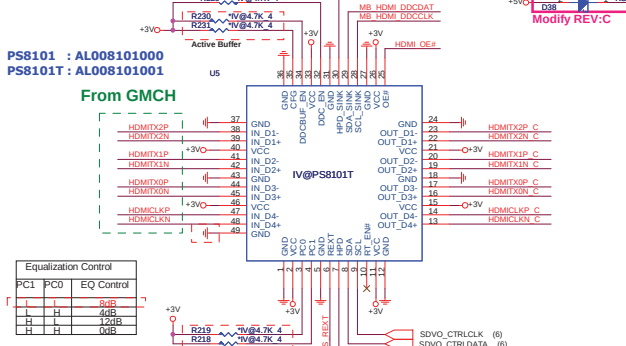
DPST



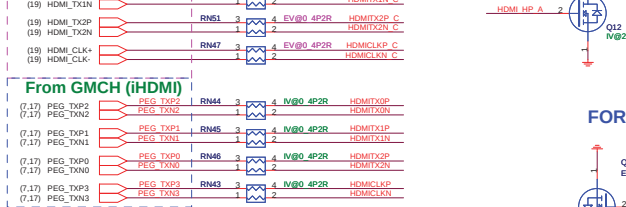
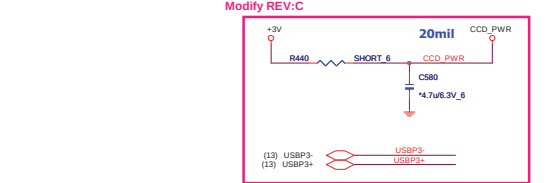
LVDS



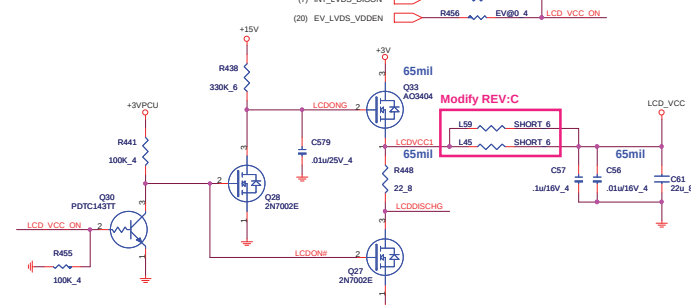
HDMI



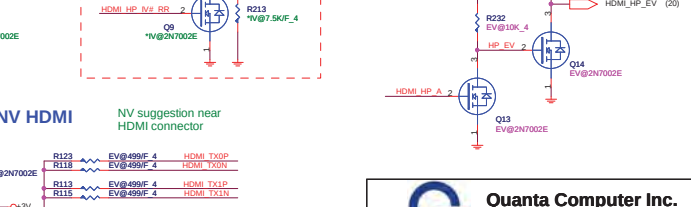
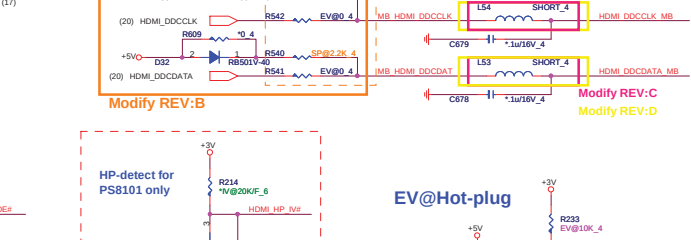
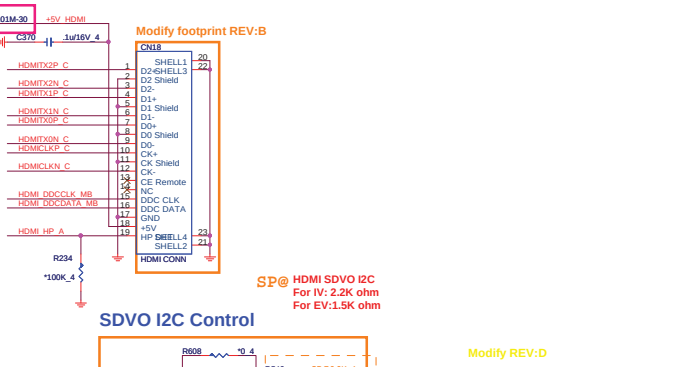
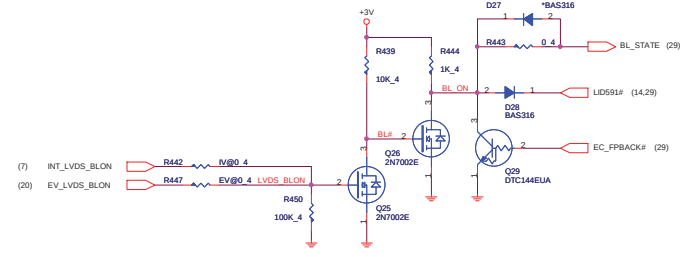
Camera



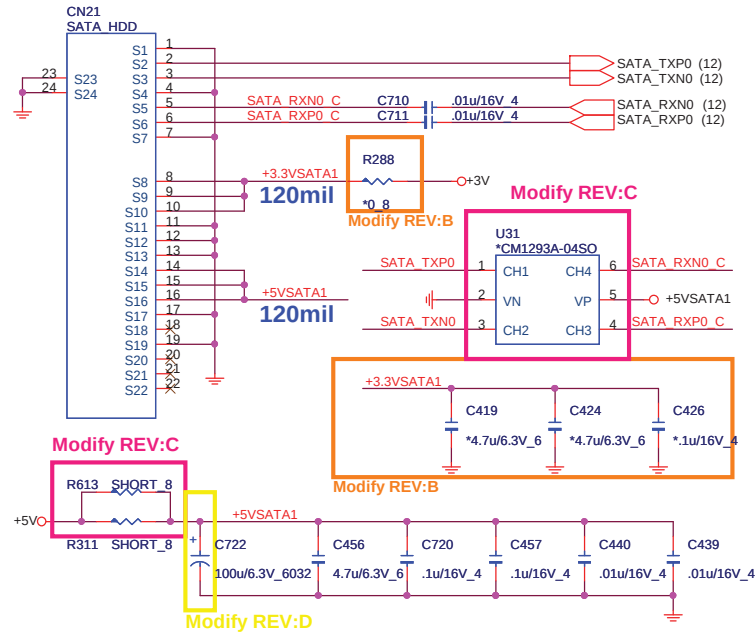
LCD_ON



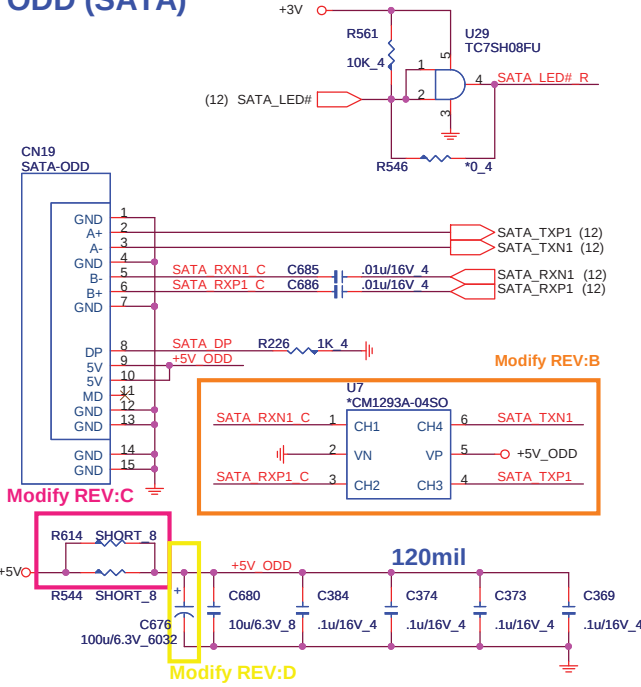
Backlight Control



SATA HDD

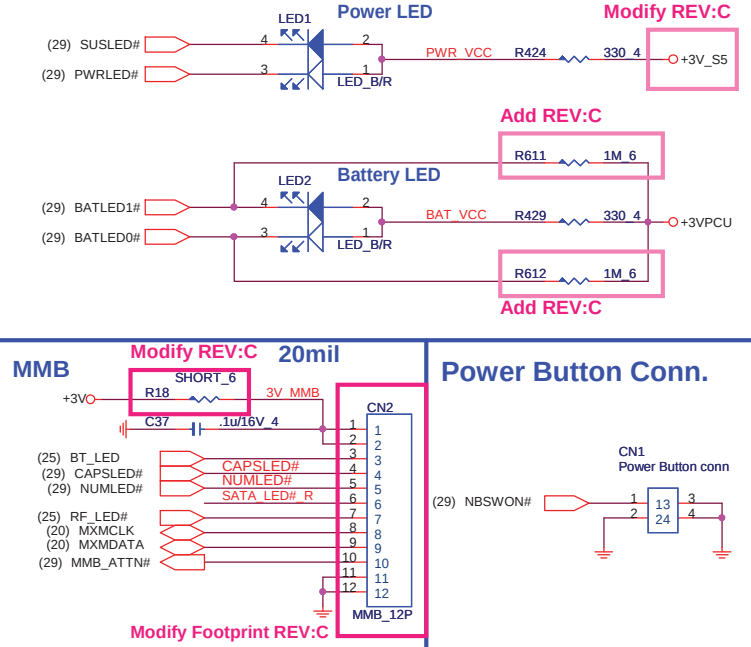


ODD (SATA)

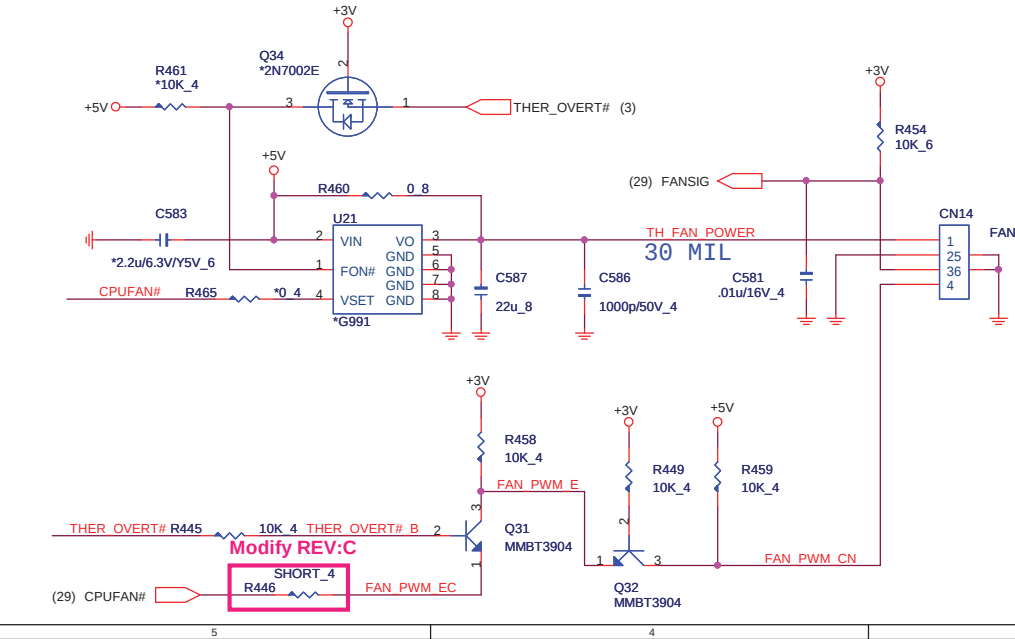


LED

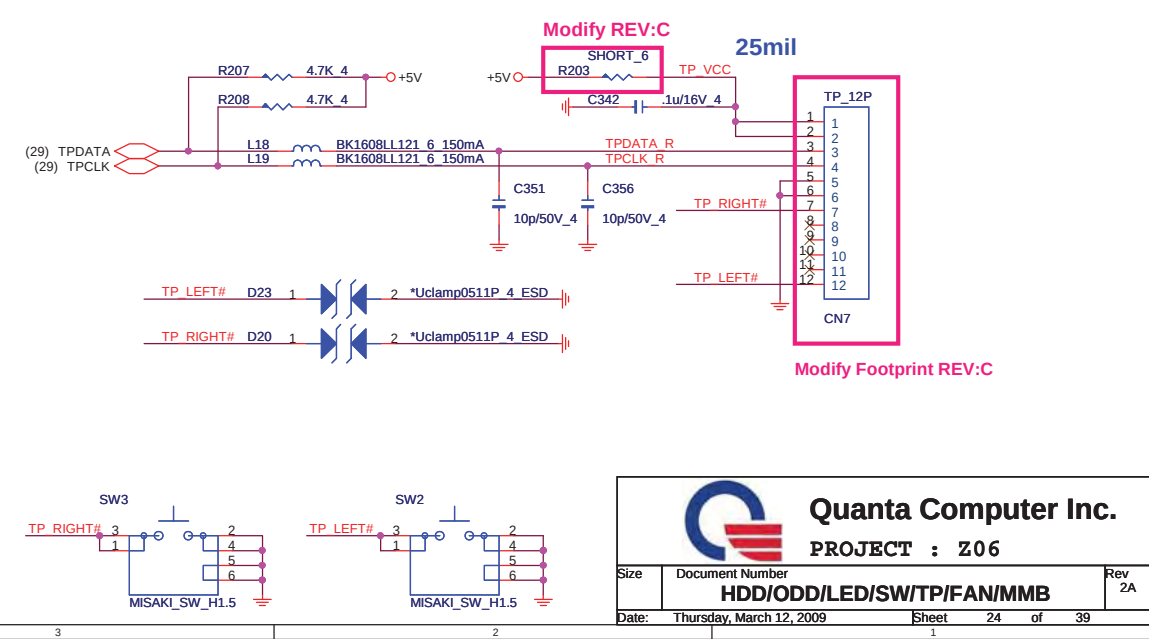
Power/Suspend: Blue/ Red



FAN



TP CONN

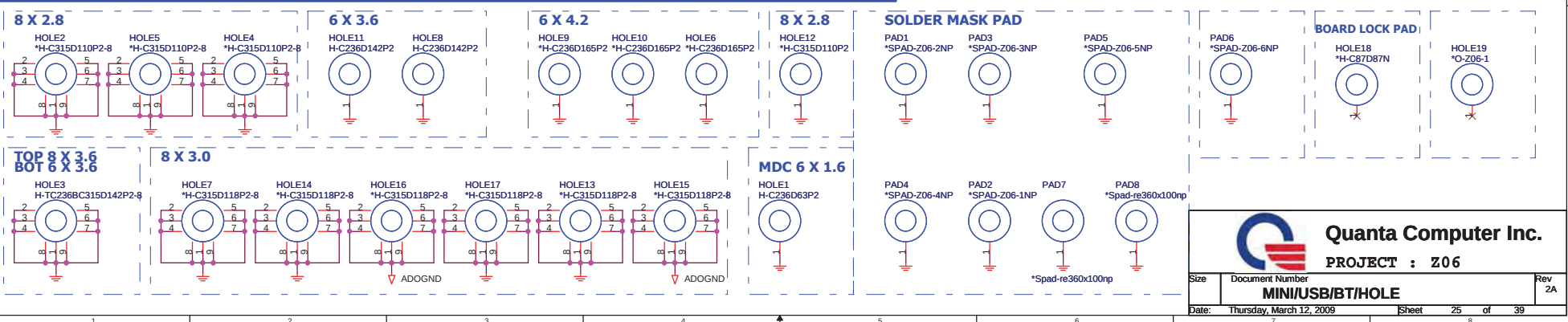
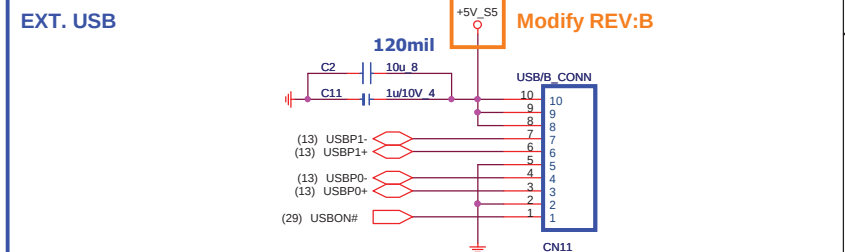
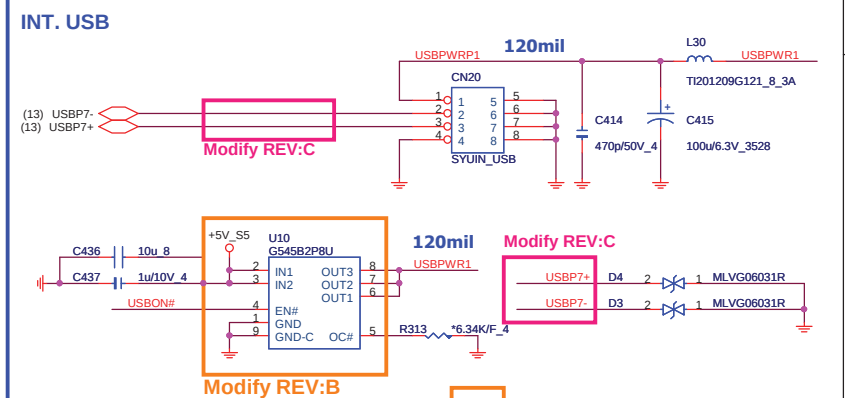
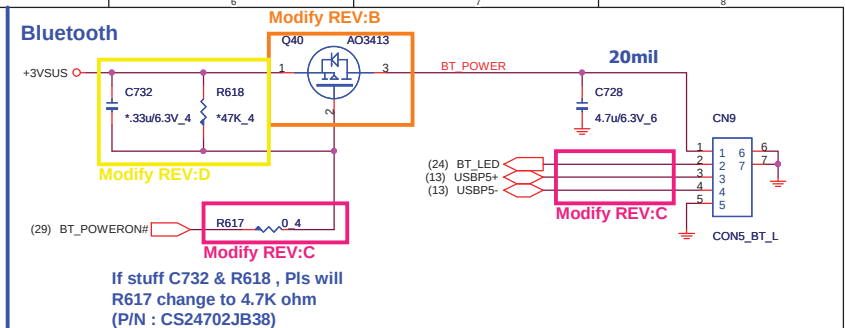
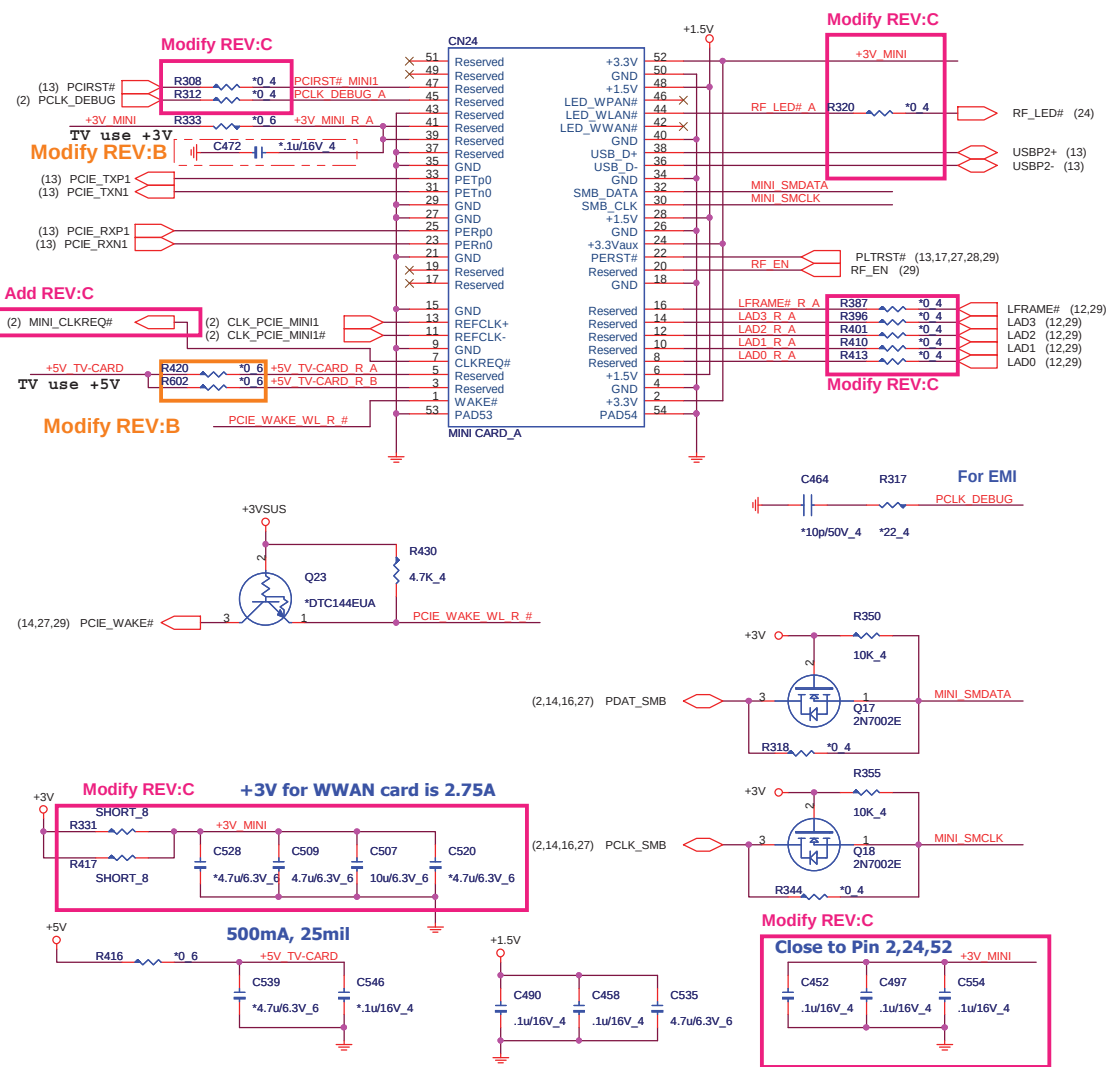


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PROJECT : Z06

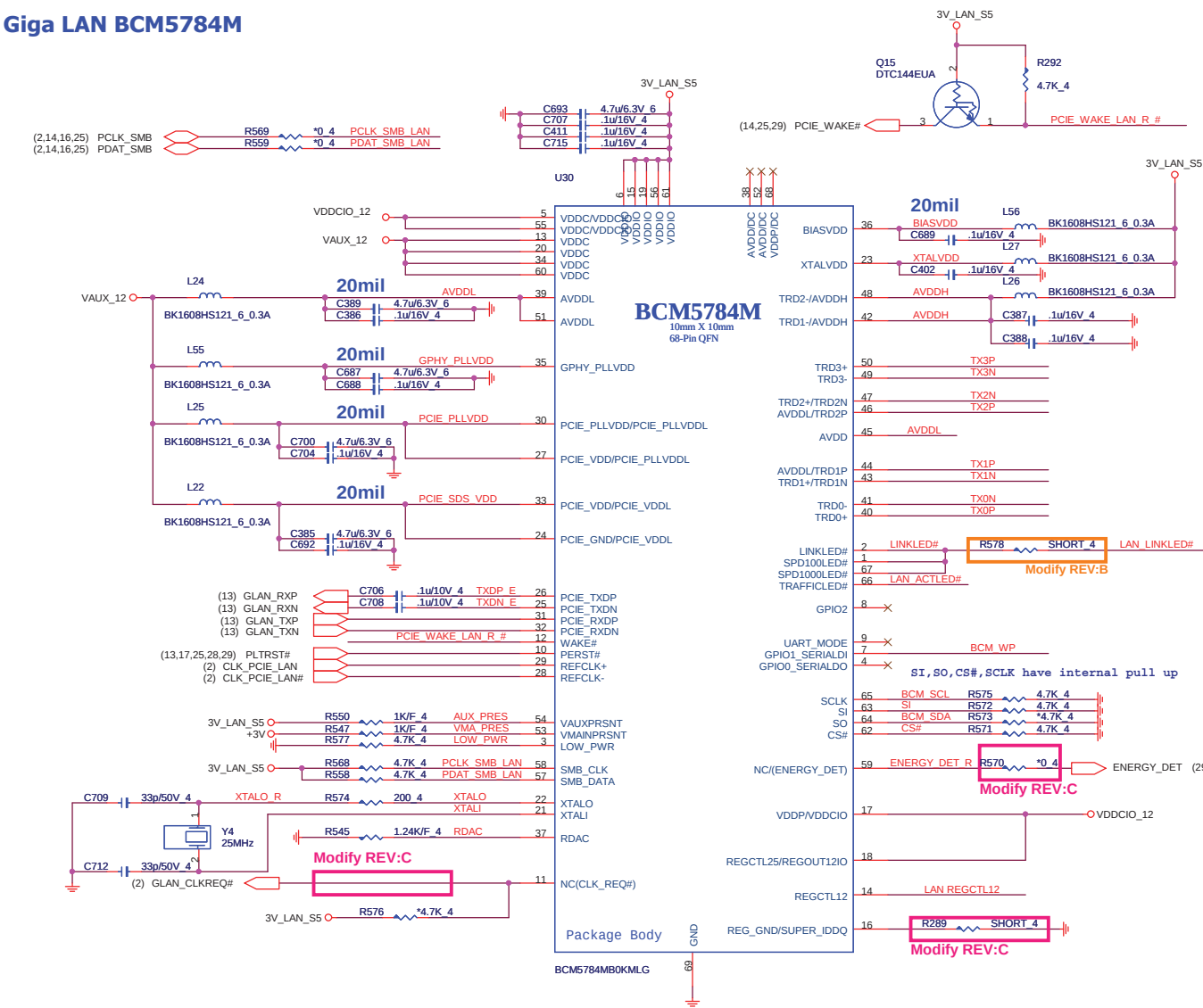
Size	Document Number	Rev
	HDD/ODD/LED/SW/TP/FAN/MMB	2A
Date:	Thursday, March 12, 2009	Sheet 24 of 39

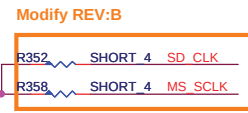
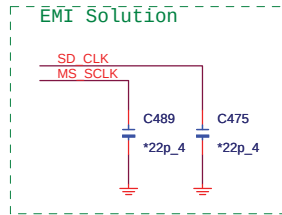
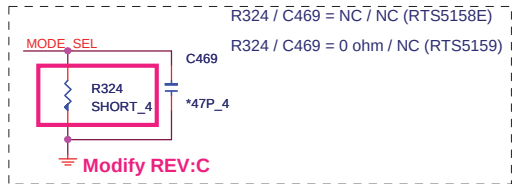
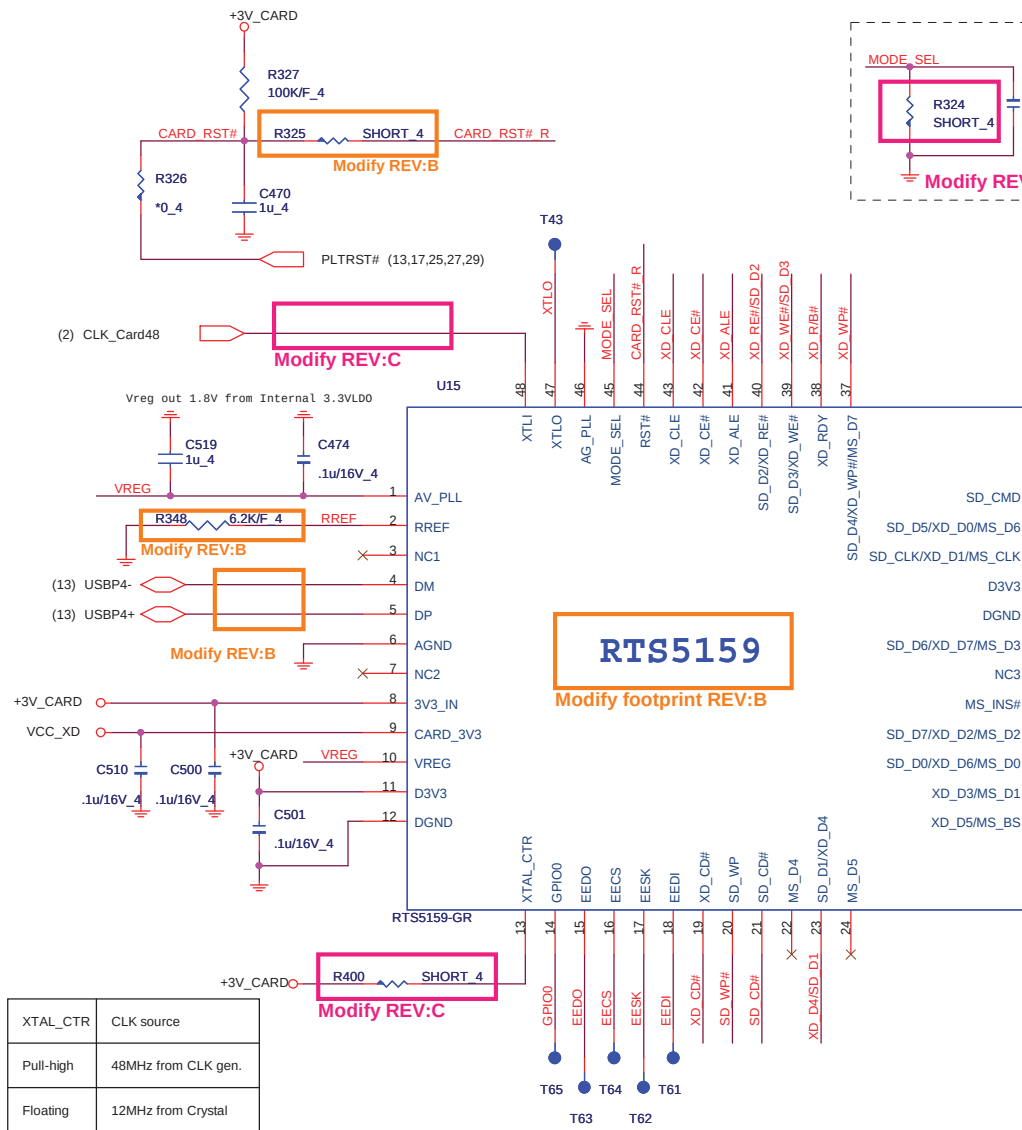
MINI-CARD



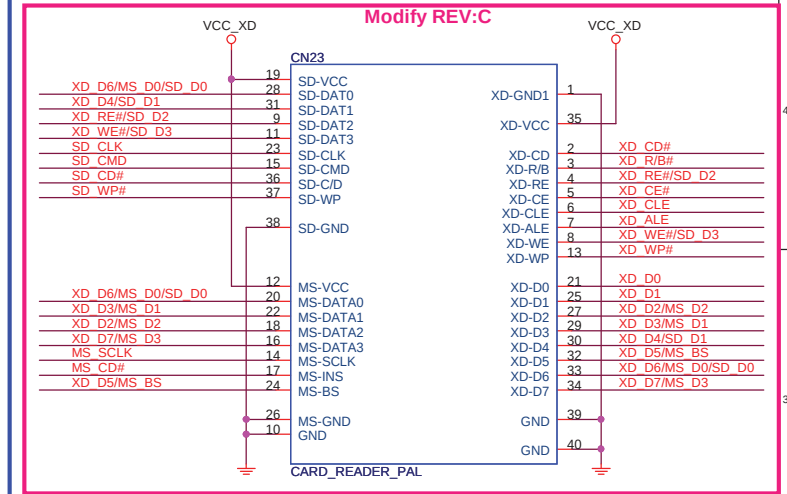
Size	Document Number CODEC/AMP/MDC	Rev 2A
Date:	Thursday, March 12, 2009	Sheet 26 of 39

Giga LAN BCM5784M

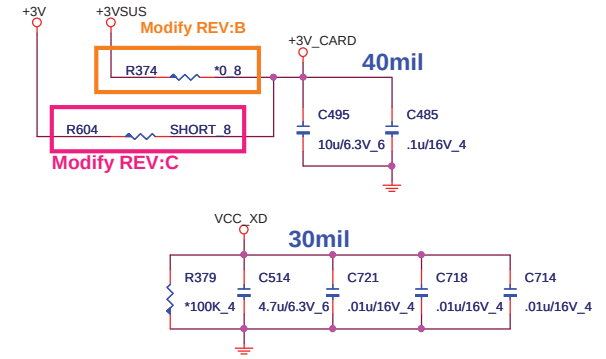




4 IN 1 CARD READER

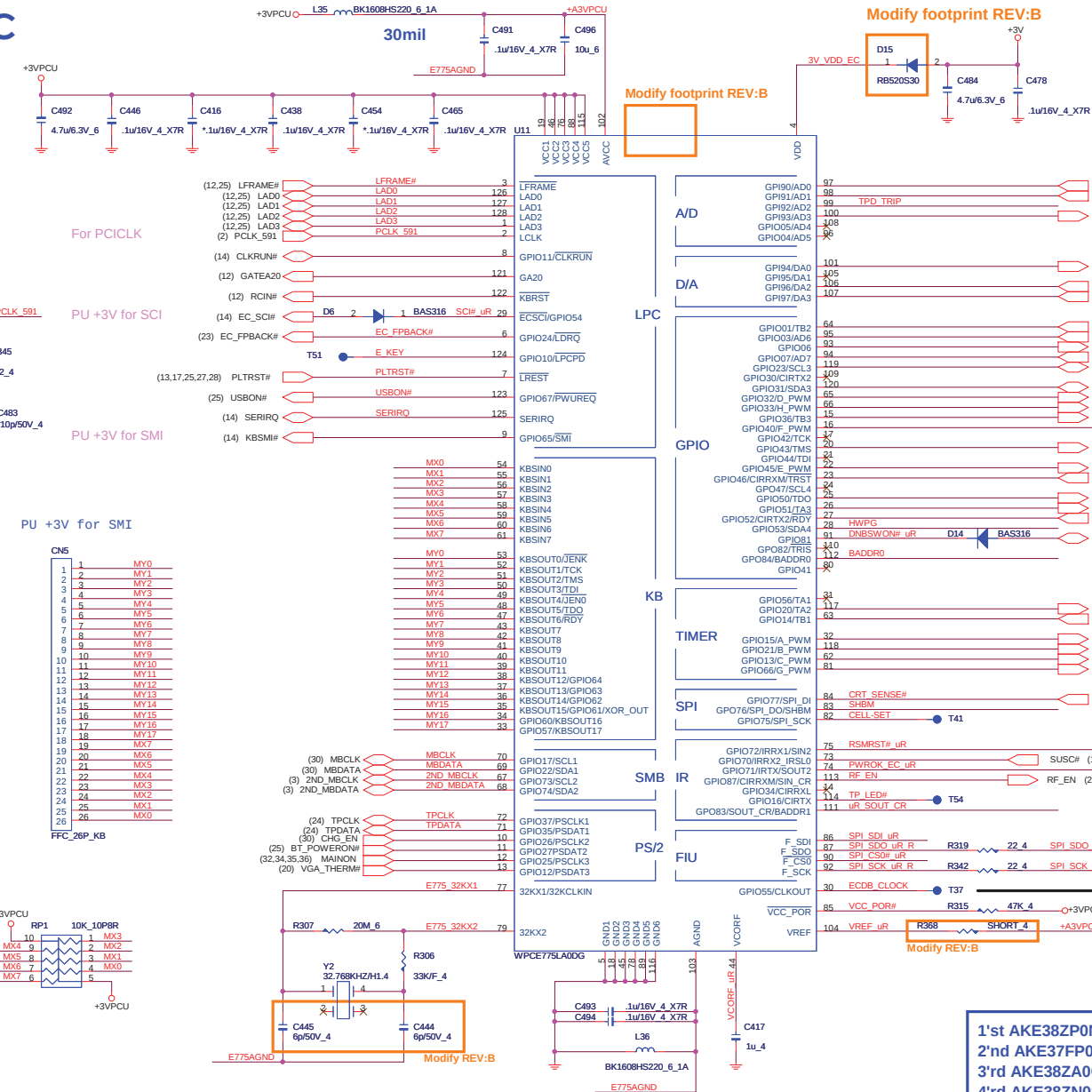


CARDREADER POWER




Quanta Computer Inc.
PROJECT : Z06

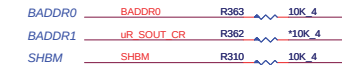
Size	Document Number	Rev
	CARD READER RTS5159	2A
Date:	Thursday, March 12, 2009	Sheet 28 of 39



I/O ADDRESS SETTING

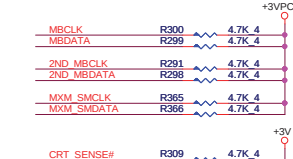
I/O Address		
BADDR1-0	Index	Data
0 0	XOR TREE TEST MODE	
0 1	CORE DEFINED	
1 0	2Eh	2Fh
1 1	164Eh	164Fh

SHBM=0: Enable shared memory with host BIOS

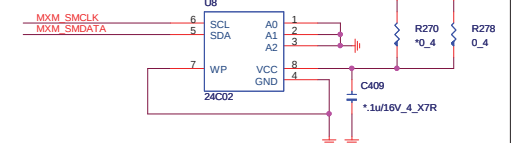


1/13 Confirm by vendor mail :
 Disabled ('1') if using FW-H device on LPC.
 Enabled ('0') if using SPI flash for both system BIOS and EC firmware

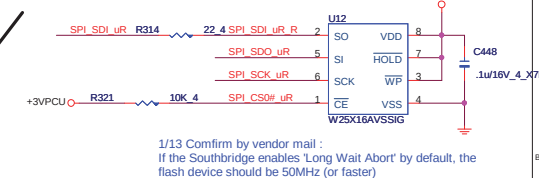
SM BUS PU



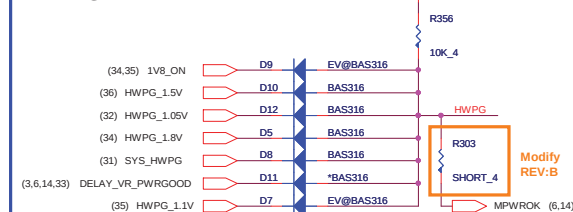
ACER ID



SPI FLASH



HWPG



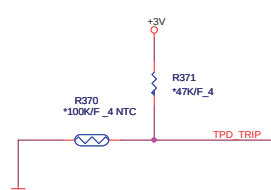
INTERNAL KEYBOARD STRIP SET



POWER-ON PAD



Thermal Sensor

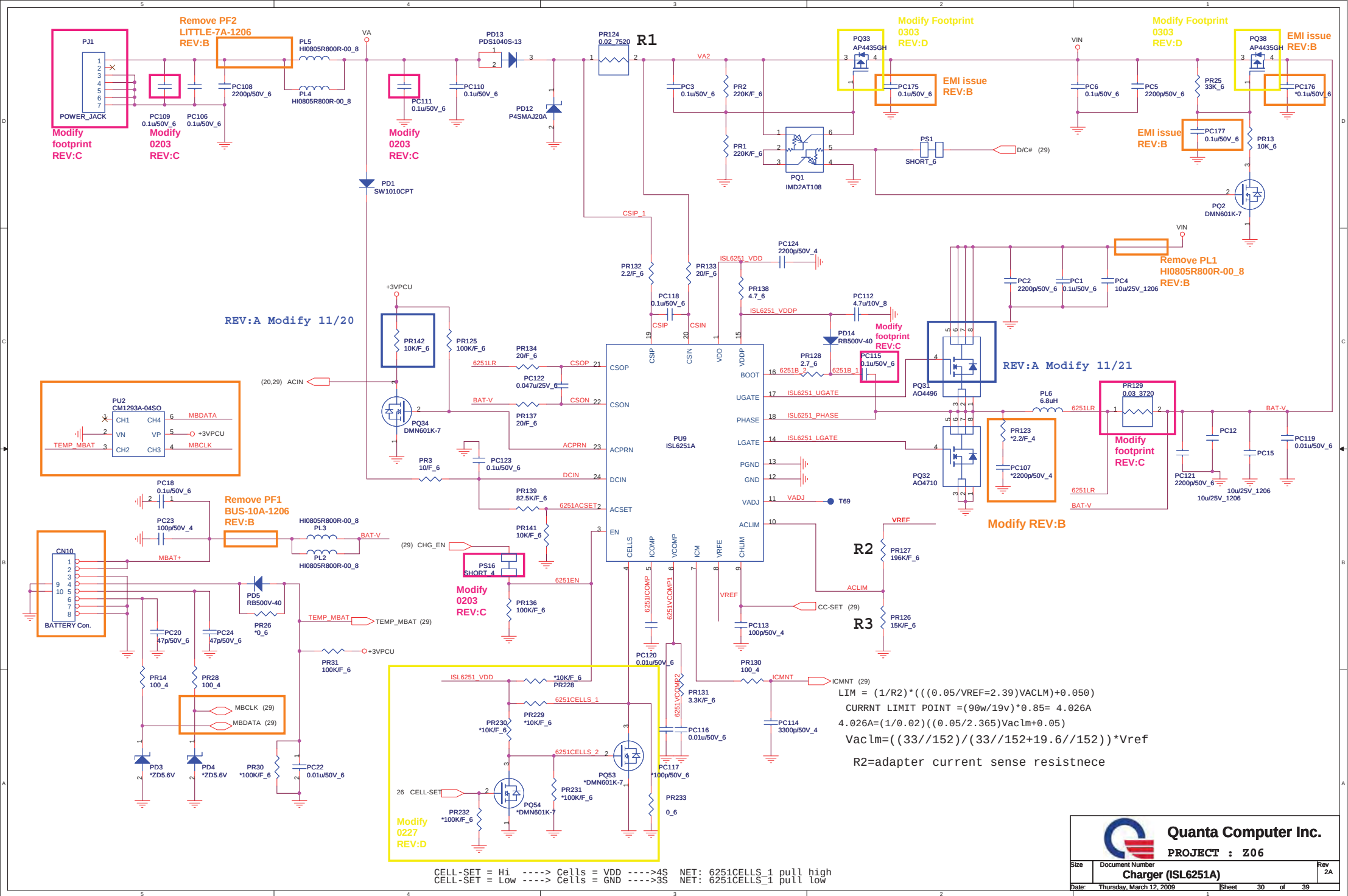


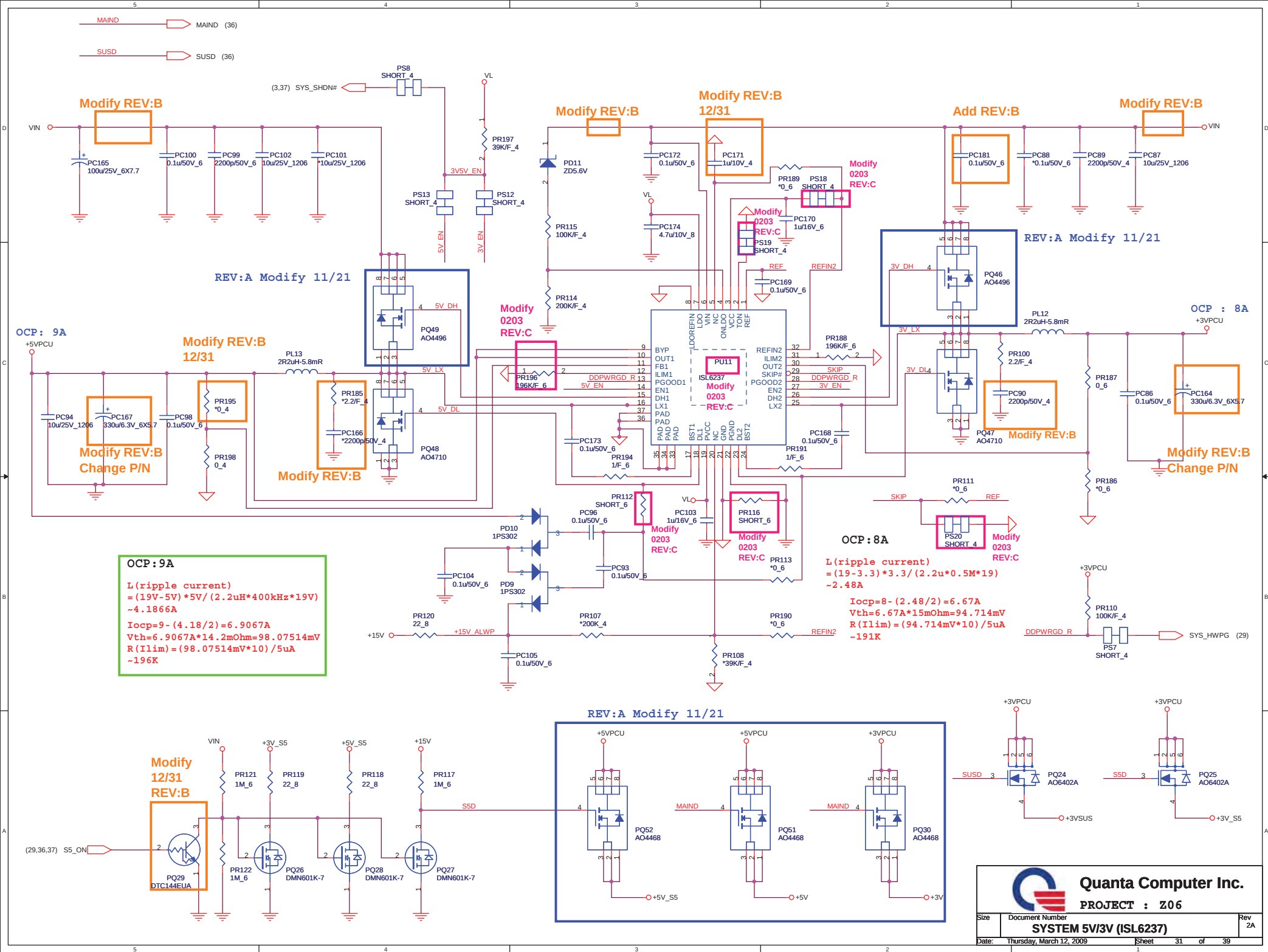
Quanta Computer Inc.

PROJECT : Z06

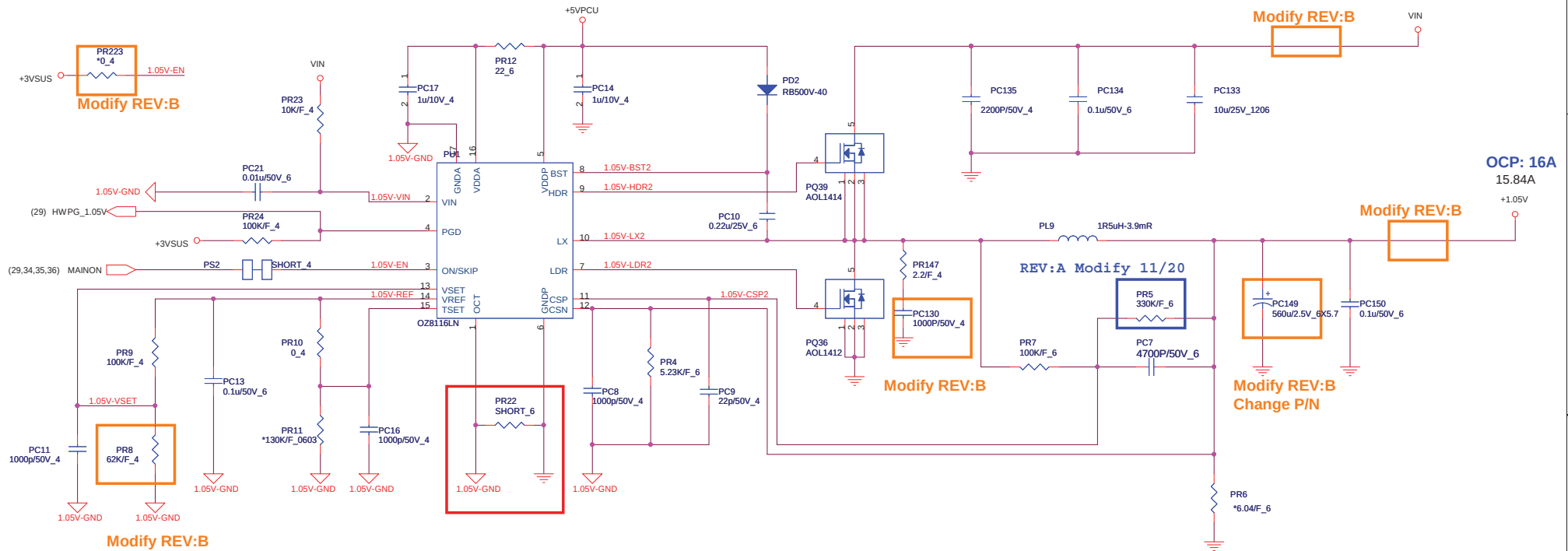
Size Document Number **WPCE775C_0DG & FLASH** Rev 2A

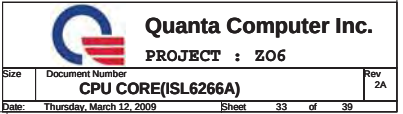
Date: Thursday, March 12, 2009 Sheet 29 of 30





VTT 1.05V





+3VSUS PR225 *0.4 S3 1.8V

Modify REV:B

Modify
0203
REV:C

Modify REV:B

OCP: 13A
13A
+1.8VSUS

Modify REV:B

Modify REV:B
Change P/N

Add REV:B for EMI Request

Modify
0203
REV:C

Modify REV:B
REV:A Modify 11/20

Modify REV:B
REV:A Modify 11/20

$$V_{out} = (PR150/PR149) \times 0.75 + 0.75$$

AO1412 $R_{ds(on)} = 3. \sim 4.6m\Omega$

OCP=15.5+0.5A

$L(\text{ripple current})$
 $= (19-1.8) \times 1.8 / (2.2u \times 400k \times 19)$
 $\sim 1.03A$

$4.6m \times 16 = RILIM \times 10uA$

$RILIM = 7.13K \sim 7.15K$

$(10u \times PR154) / R_{ds(on)} + \Delta I / 2 = I_{ocp}$

Modify REV:B
12/31

(29,32,34,36) MAINON

MAINON

(20) GPU_VID1

(20) GPU_VID0

(29,34) 1V8_ON

+3VSUS

MAINON

Vout = 0.8 (1+R1/R2)

= 1.5V

PC83 EV@0.1u/50V_6

PC80 EV@1000p/50V_4

PC84 EV@0.22u/10V_4

PC87 EV@332K/F_4

PC88 EV@2.2K_4

PC89 EV@100K/F_6

PC90 EV@158K/F_6

PC91 EV@121K/F_6

PC92 EV@33K/F_5

PC93 EV@0.1u/50V_6

PC94 EV@63.4K/F_6

PC95 EV@2N7002E

PC96 EV@2N7002E

PC97 EV@0.22u/10V_4

PC98 EV@100K/F_6

PC99 EV@100K/F_6

PC100 EV@100K/F_6

PC101 EV@100K/F_6

PC102 EV@100K/F_6

PC103 EV@100K/F_6

PC104 EV@100K/F_6

PC105 EV@100K/F_6

PC106 EV@100K/F_6

PC107 EV@100K/F_6

PC108 EV@100K/F_6

PC109 EV@100K/F_6

PC110 EV@100K/F_6

PC111 EV@100K/F_6

PC112 EV@100K/F_6

PC113 EV@100K/F_6

PC114 EV@100K/F_6

PC115 EV@100K/F_6

PC116 EV@100K/F_6

PC117 EV@100K/F_6

PC118 EV@100K/F_6

PC119 EV@100K/F_6

PC120 EV@100K/F_6

PC121 EV@100K/F_6

PC122 EV@100K/F_6

PC123 EV@100K/F_6

PC124 EV@100K/F_6

PC125 EV@100K/F_6

PC126 EV@100K/F_6

PC127 EV@100K/F_6

PC128 EV@100K/F_6

PC129 EV@100K/F_6

PC130 EV@100K/F_6

PC131 EV@100K/F_6

PC132 EV@100K/F_6

PC133 EV@100K/F_6

PC134 EV@100K/F_6

PC135 EV@100K/F_6

PC136 EV@100K/F_6

PC137 EV@100K/F_6

PC138 EV@100K/F_6

PC139 EV@100K/F_6

PC140 EV@100K/F_6

PC141 EV@100K/F_6

PC142 EV@100K/F_6

PC143 EV@100K/F_6

PC144 EV@100K/F_6

PC145 EV@100K/F_6

PC146 EV@100K/F_6

PC147 EV@100K/F_6

PC148 EV@100K/F_6

PC149 EV@100K/F_6

PC150 EV@100K/F_6

PC151 EV@10u/6.3V_8

PC152 EV@10u/6.3V_8

PC153 EV@0.1u/10V_4

PC154 EV@1u/10V_4

PC155 EV@10u/6.3V_8

PC156 EV@10u/6.3V_8

PC157 EV@0.1u/10V_4

PC158 EV@0.047u/16V_4

PC159 EV@10u/6.3V_8

PC160 EV@10u/25V_1206

PC161 EV@2200p/50V_4

PC162 EV@0.1u/50V_6

PC163 EV@330u/2V_7343

PC164 EV@330u/2V_7343

PC165 EV@10u/6.3V_8

PC166 EV@10u/6.3V_8

PC167 EV@4700p/50V_6

PC168 EV@51F_6

PC169 EV@10u/6.3V_8

PC170 EV@10u/6.3V_8

PC171 EV@330K/F_4

PC172 EV@1000p/50V_4

PC173 EV@22p/50V_4

PC174 EV@0.22u/25V_6

PC175 EV@0.22u/25V_6

PC176 EV@1u/16V_6

PC177 EV@100K_4

PC178 EV@100K_4

PC179 EV@34K/F_6

PC180 EV@13K/F_6

PC181 EV@100K_4

PC182 EV@2.2_4

PC183 EV@100K/F_6

PC184 EV@4700p/50V_6

PC185 EV@51F_6

PC186 EV@10u/6.3V_8

PC187 EV@10u/6.3V_8

PC188 EV@10u/6.3V_8

PC189 EV@10u/6.3V_8

PC190 EV@10u/6.3V_8

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PC192 EV@10u/6.3V_8

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PC195 EV@10u/6.3V_8

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PC203 EV@10u/6.3V_8

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PC206 EV@10u/6.3V_8

PC207 EV@10u/6.3V_8

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PC209 EV@10u/6.3V_8

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PC211 EV@10u/6.3V_8

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PC213 EV@10u/6.3V_8

PC214 EV@10u/6.3V_8

PC215 EV@10u/6.3V_8

PC216 EV@10u/6.3V_8

PC217 EV@10u/6.3V_8

PC218 EV@10u/6.3V_8

PC219 EV@10u/6.3V_8

PC220 EV@10u/6.3V_8

PC221 EV@10u/6.3V_8

PC222 EV@10u/6.3V_8

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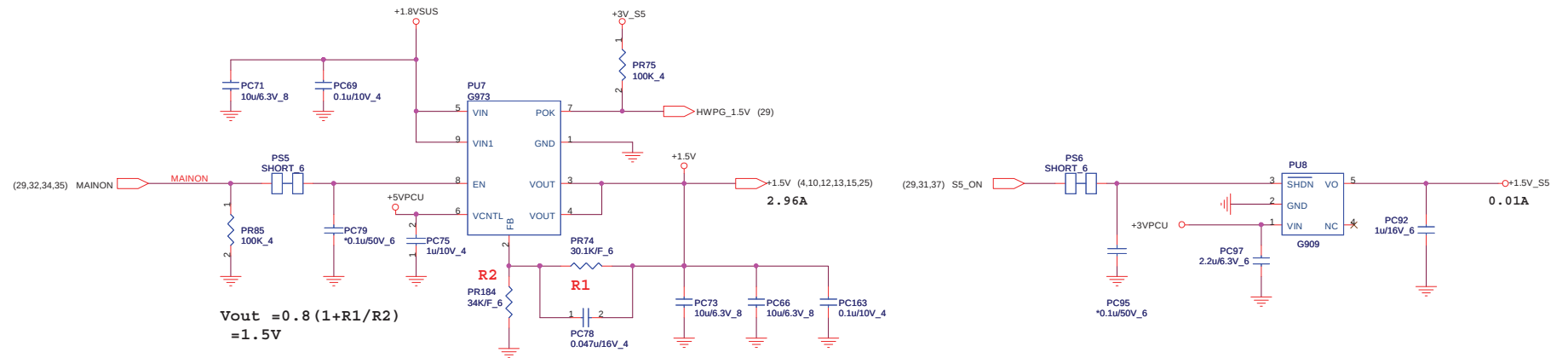
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PC33



Modify REV:B

