Compal Confidential

JE50/HM50/SJV50_BZ

P5WE6/P5WH6/P5WS6 Schematics Document

AMD Brazos

Brazos with Zacate / Hudson M1 / Seymour XT

DIS only / UMA only / PX Muxless / PX Muxless with BACO

2010-11-16

LA-7092P REV: 1.0

ZZZ

PCB

Part Number = DAZ0IC00100

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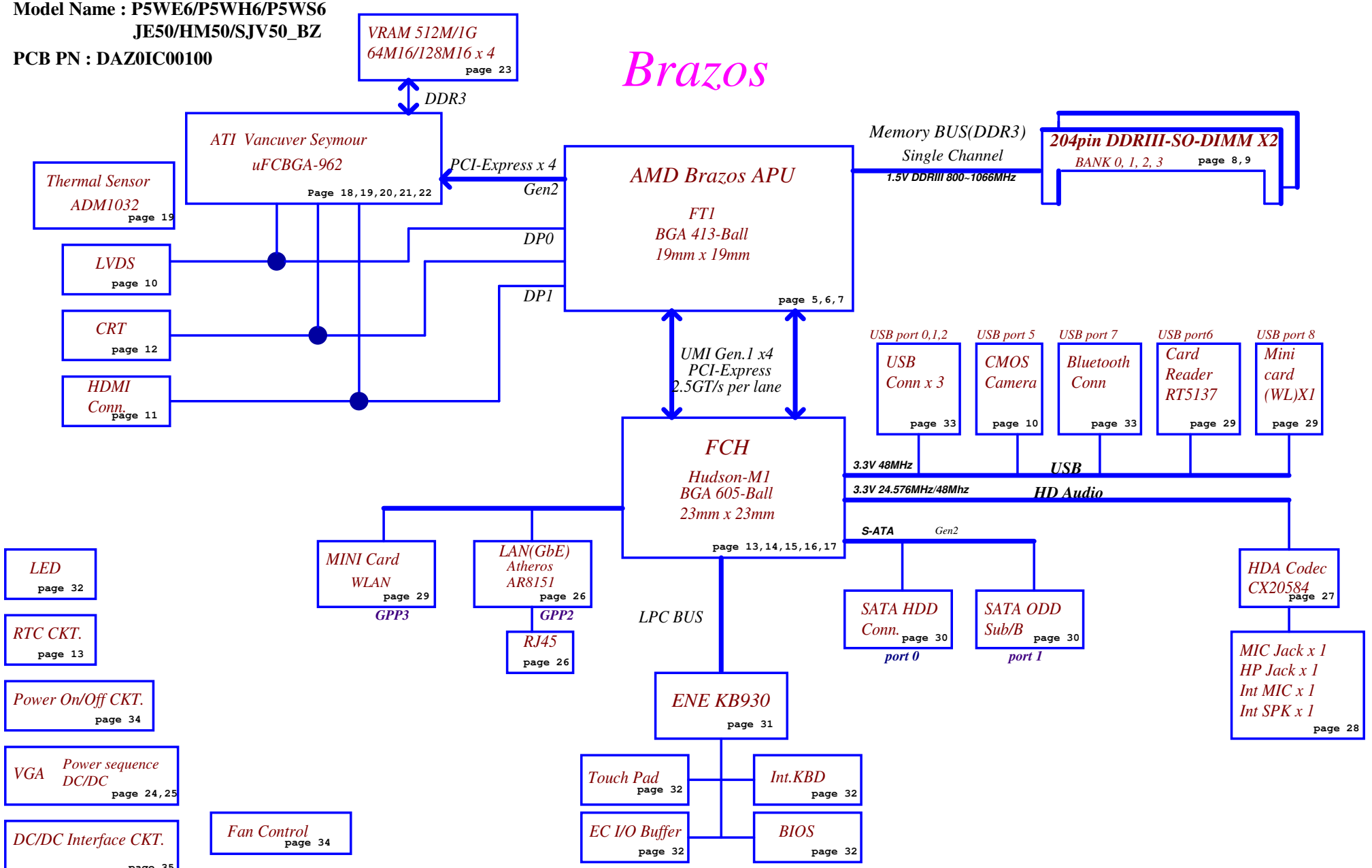
Model Name : P5WE6/P5WH6/P5WS6
JE50/HM50/SJV50_BZ

PCB PN : DAZ0IC00100

Brazos



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Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VSB	VSB always on power rail	ON	ON	ON*
+3VALW	3.3V always on power rail	ON	ON	ON*
+5VALW	5V always on power rail	ON	ON	ON*
+1.1VALW	1.1V always on power rail	ON	ON	ON*
+APU_CORE	Core voltage for CPU (0.7-1.2V)	ON	OFF	OFF
+APU_CORE_NB	1.0V switched power rail	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDRIII	ON	ON	OFF
+0.75VS	0.75VS switched power rail for DDR terminator	ON	OFF	OFF
+1.05VS	1.05V switched power rail for APU VDD10	ON	OFF	OFF
+1.1VS	1.1VS switched power rail	ON	OFF	OFF
+1.8VS	1.8V switched power rail	ON	OFF	OFF
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VS	5V switched power rail	ON	OFF	OFF
+VGA_CORE	Core voltage for GPU	ON	OFF	OFF
+3VSG	3.3V switched power rail for GPU	ON	OFF	OFF
+1.8VSG	1.8V switched power rail for GPU	ON	OFF	OFF
+1.5VSG	1.5V switched power rail for GPU	ON	OFF	OFF
+1.0VSG	1.0V switched power rail for GPU	ON	OFF	OFF
+3V_LAN	3.3V power rail for LAN	ON	ON	ON
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1 (Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%
Ra/Rc/Re	100K +/- 5%

Board ID	Rb / Rd / Rf	V_{AD_BID} min	V_{AD_BID} typ	V_{AD_BID} max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V

BOARD ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

EC SM Bus1 address

Device	Address	HEX

EC SM Bus2 address

Device	Address	HEX
ADM1032 (GPU)	1001-101xb	9AH

SM Bus Controller 0

(FCH_SMB1 ~ FCH_SMB4, SMB_ALERT#)

Device	Address	HEX
APU SIC/SID (FCH_SMB3)		
H_THERMTRIP# (FCH_ALERT#)		

SM Bus Controller 1

(FCH_SMB0)

Device	Address	HEX
DDR DIMM1 (FCH_SMB0)	1001-000xb	90
DDR DIMM2 (FCH_SMB0)	1001-001xb	92
WLAN (FCH_SMB0)		

BOARD ID Table

Board ID	PCB Revision
0	*w/ X'tal X1*
1	*wo/ X'tal X1*
2	
3	
4	
5	
6	
7	

Project ID Table

Board ID	PCB Revision
0	
1	
2	
3	
4	
5	
6	
7	

BTO Option Table

BTO Item	BOM Structure
Display from APU	UMA@
Display from VGA	DISO@
Use VGA	VGA@
Muxless w/BACO	BACO@
Muxless wo/BACO	WOBACO@
Muxless	PX@
w/Vancouver Serise	VAN@
w/Manhttan Serise	MAN@
Bluetooth	BT@
AR8151	8151@
Seymour	Seymour@
wo/Muxless	WOPX@
wo/VGA	WOVGA@
APU 1.5G	15G@
APU 1.6G	16G@

*UMA only : UMA@ BT@ 8151@ WOVGA@ WOPX@

VGA Chip SEL:
1. Seymour@ + Van@
2. Robson@ + Man@

APU Chip SEL:
1. 16G@
2. 15G@

*DIS only : VGA@ DISO@ WOBACO@ BT@ 8151@ WOPX@

*Muxless w/BACO : UMA@ VGA@ PX@ BACO@ BT@ 8151@

Muxless wo/BACO : UMA@ VGA@ PX@ WOBACO@ BT@ 8151@

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Title	Notes List		
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Power-Up/Down Sequence

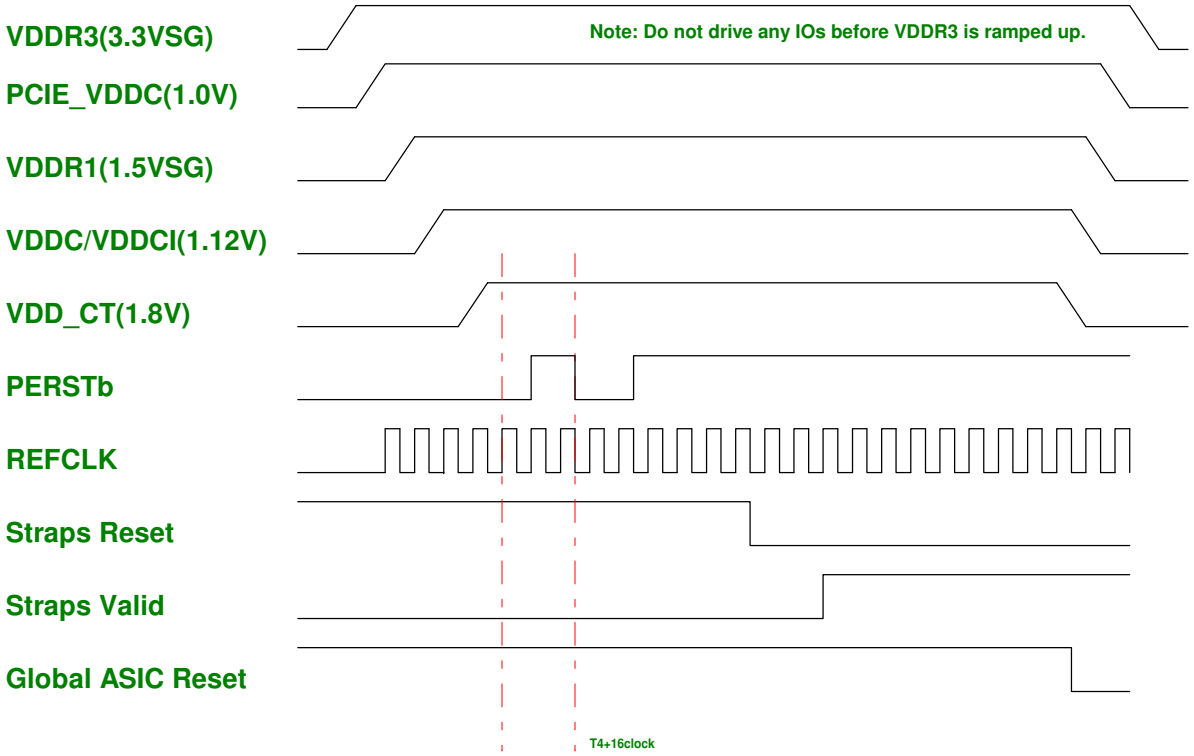
1. All the ASIC supplies must fully reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred.

2. VDDR3 should ramp-up before or simultaneously with VDDC.

3. For LVDS, DPx_VDD10 should ramp-up before DPx_VDD18 and the PCIe Reference clock should begin before DPx_VDD18. For power-down, DPx_VDD18 should ramp-down before DPx_VDD10.

4. The external pull-ups on the DDC/AUX signals (if applicable) should ramp-up before or after both VDDC and VDD_CT have ramped up.

5.VDDC and VDD_CT should not ramp-up simultaneously. (e.g., VDDC should reach 90% before VDD_CT starts to ramp-up (or vice versa).)



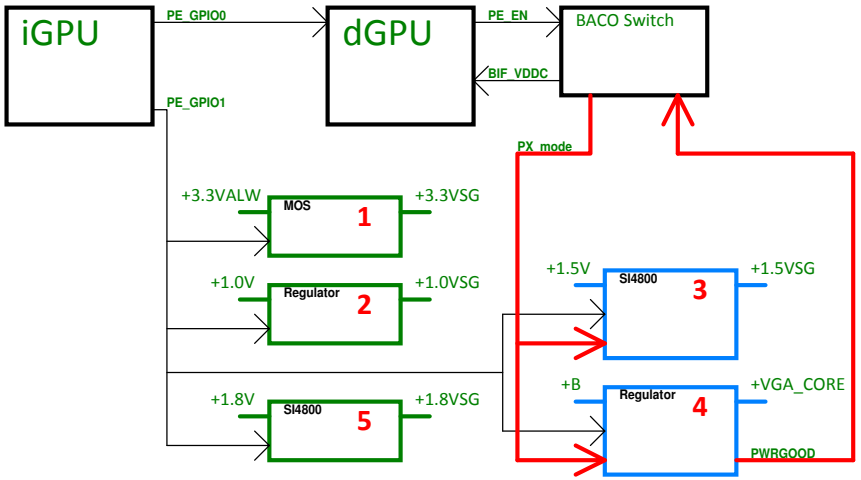
Without BACO option :

PE_GPIO0 : Low -> Reset dGPU ; High ->Normal operation
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON

BACO option :

PE_GPIO0 : High ->Normal operation (dGPU is not reseton BACO mode)
PE_GPIO1 : Low -> dGPU Power OFF ; High -> dGPU Power ON (always High)

dGPU Power Pins	Voltage	PX 3.0	BACO Mode	Max current
PCIE_PVDD, PCIE_VDDR, TSVDD, VDDR4, VDD_CT, DPE_PVDD, DP[F:E]_VDD18, DP[D:A]_PVDD, DP[D:A]_VDD18, AVDD, VDD1DI, A2VDDQ, VDD2DI, DPLL_PVDD, MPV18, and SPV18	1.8V	OFF	ON	1679mA
DP[F:E]_VDD10, DP[D:A]_VDD10, DPLL_VDDC, and SPV10	1.0V	OFF	ON	575mA
PCIE_VDDC	1.0V	OFF	ON	2A
VDDR3 , and A2VDD	3.3V	OFF	ON	190mA
BIF_VDDC (current consumption = 55mA@1.0V, in BACO mode)	Same as VDDC	OFF	ON Same as PCIE_VDDC	70mA
VDDR1	1.5V	OFF	OFF	2.8A
VDDC/VDDCI	1.12V	OFF	OFF	12.9A



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Compal Electronics, Inc.

Title: dGPU Block Diagram

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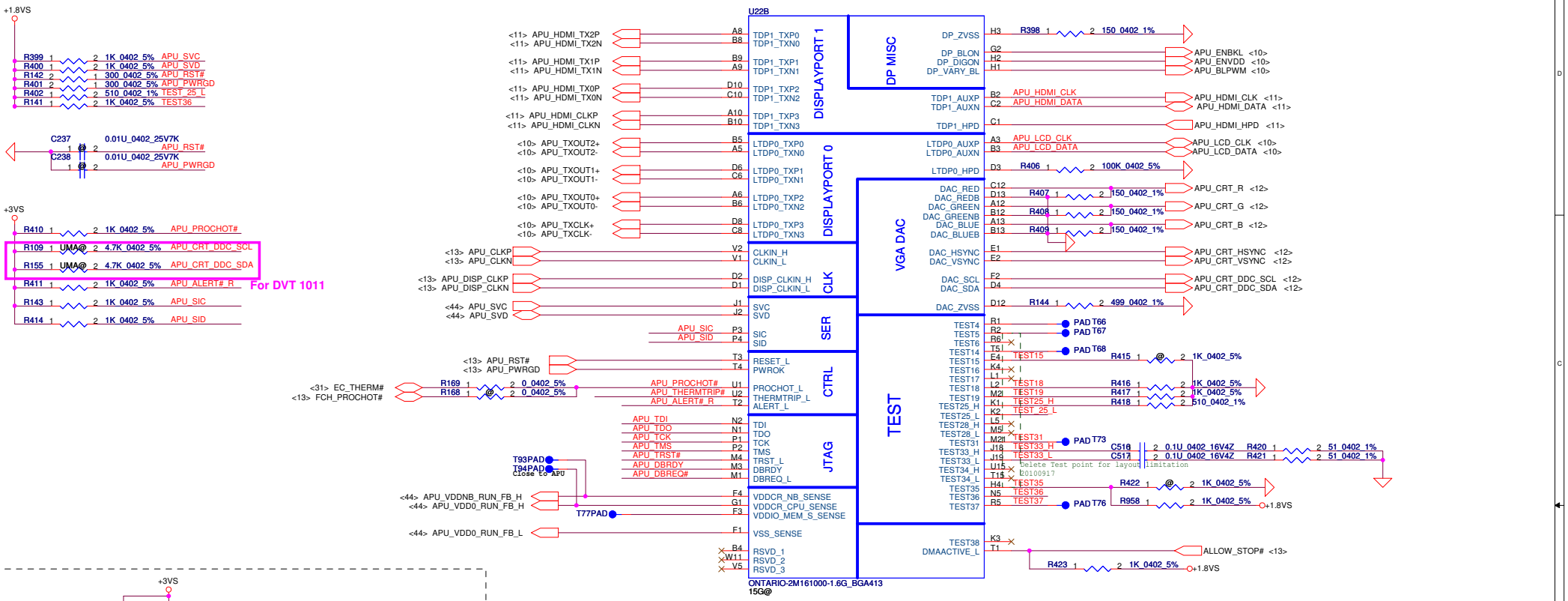
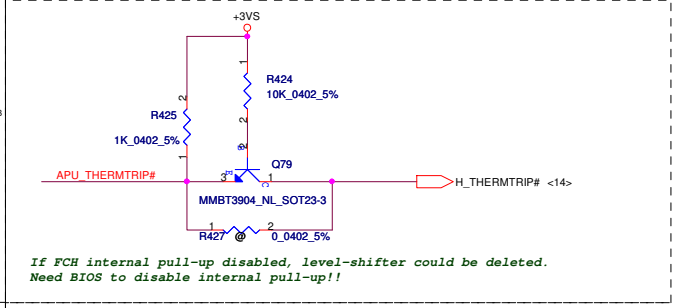
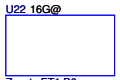
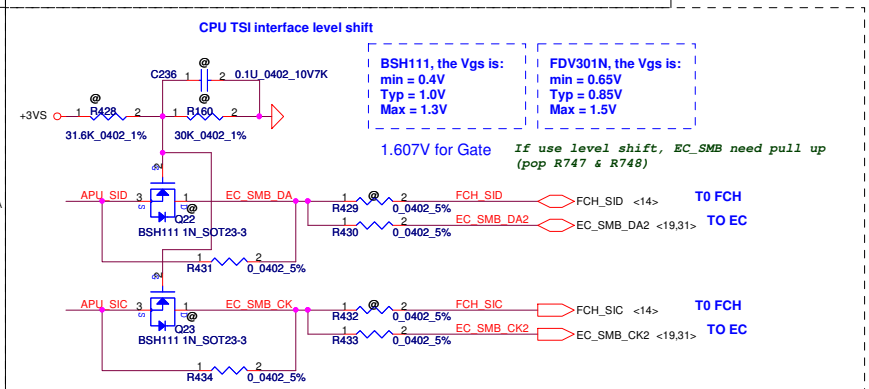


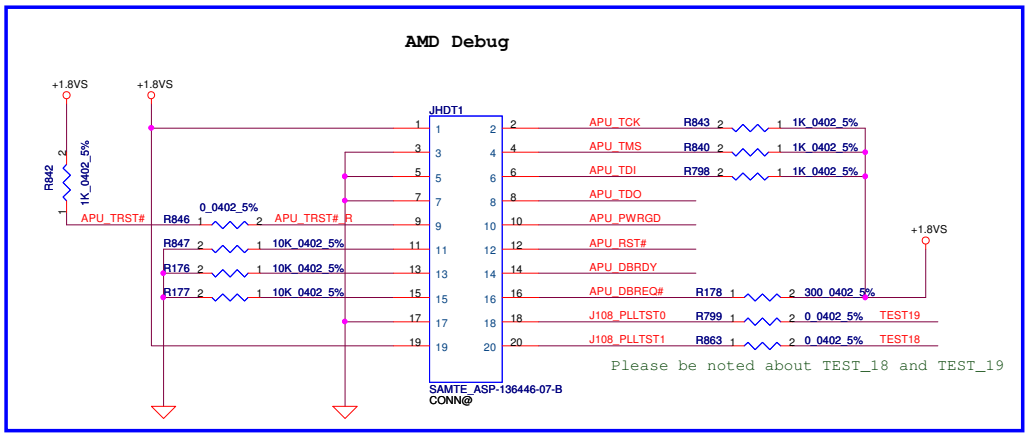
APU : SA00004DO60 (S IC ZACATE 2M151132B1240 1.5G BGA)

APU : SA000046G80 (S IC ZACATE 2M161232B2240 1.6G BGA)









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Title	FT1 CTRL/DP/CRT		
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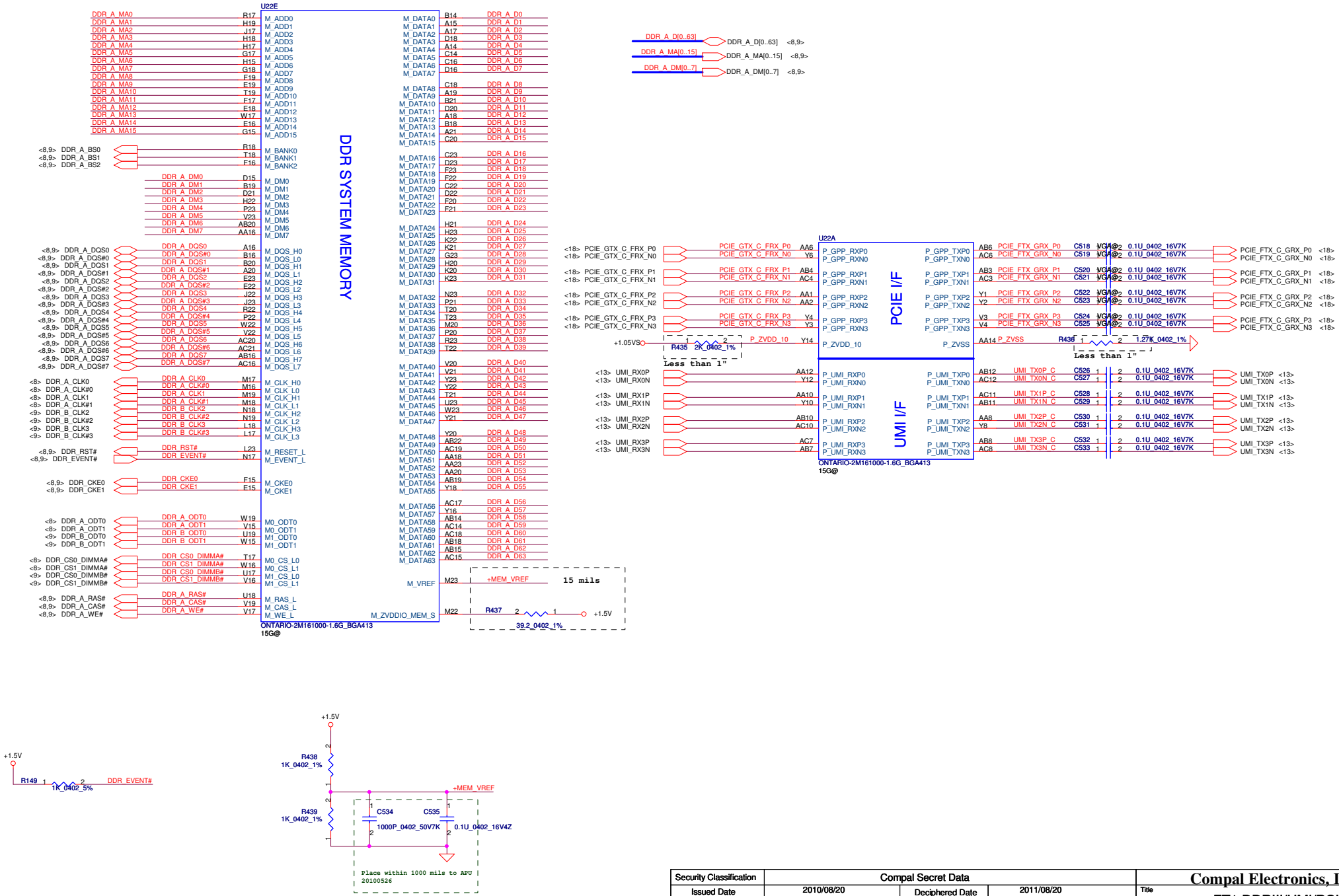

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Title: FT1 DDRIII/UMI/PCIE

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Custom	LA-7092P P5WE6/H6/S6	1.0

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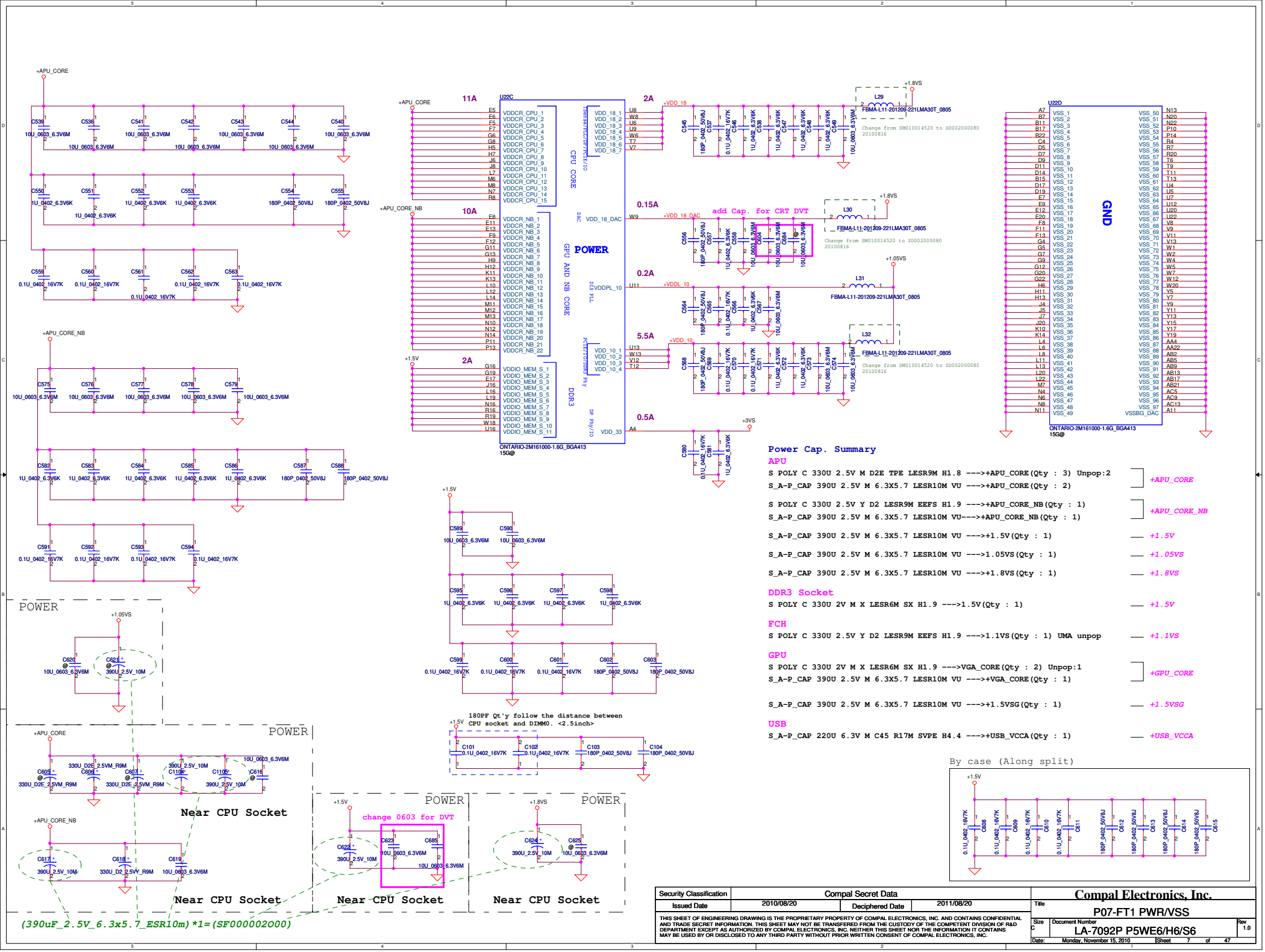

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Title: P07-FT1 PWR/VSS

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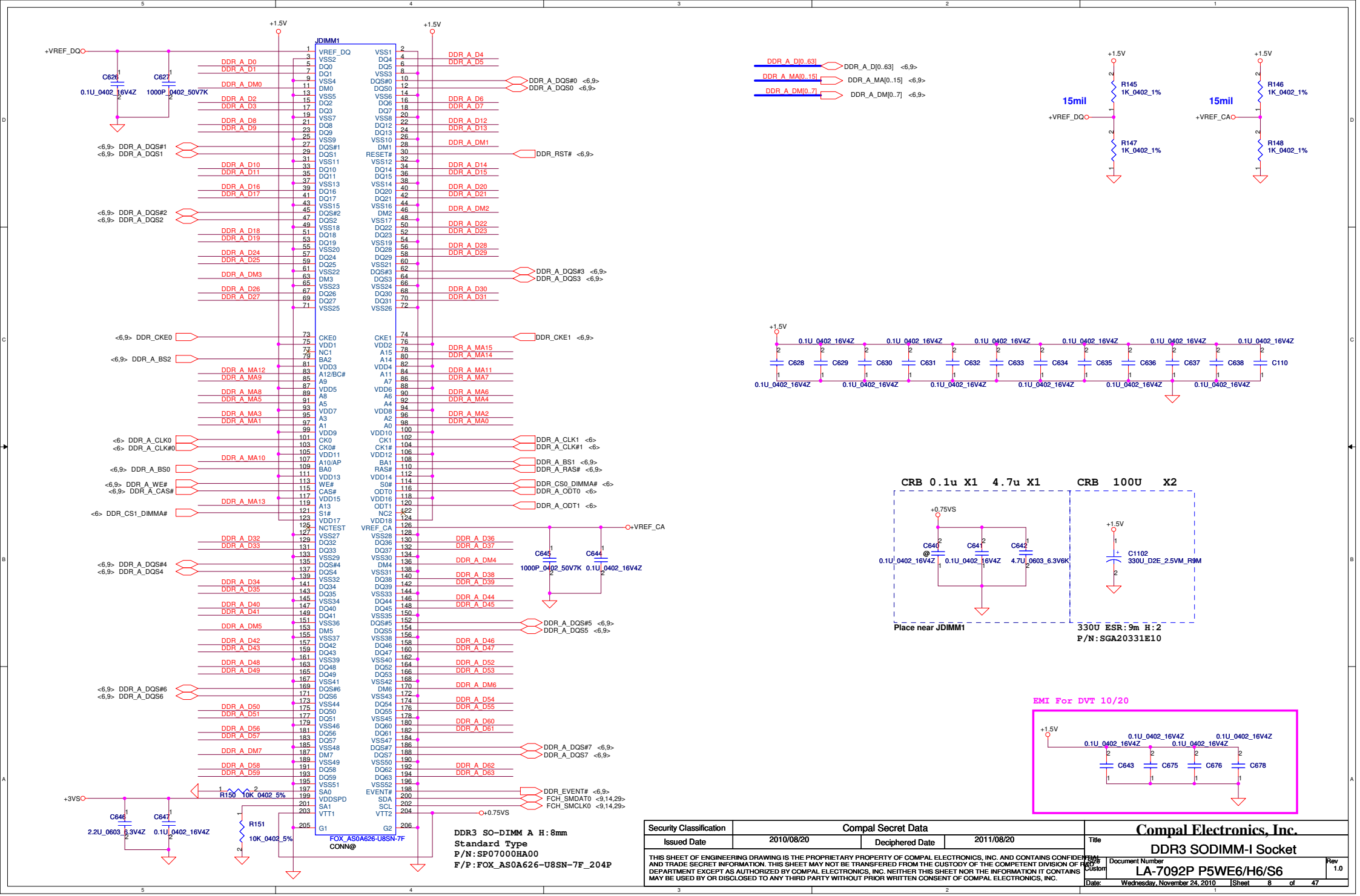

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Title: DDR3 SODIMM-I Socket

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Custom	LA-7092P P5WE6/H6/S6	1.0

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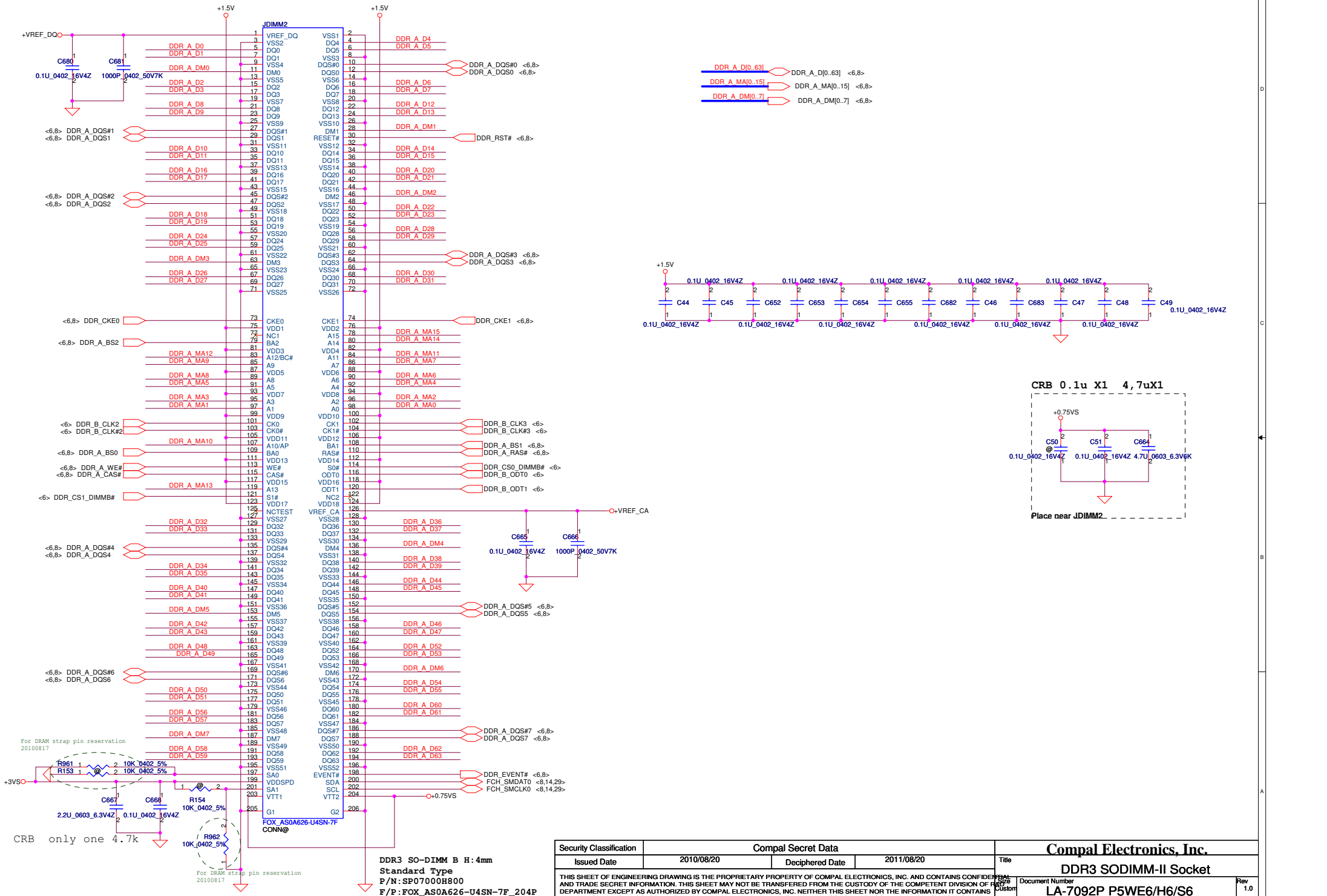

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Compal Electronics, Inc.

Title: DDR3 SODIMM-II Socket

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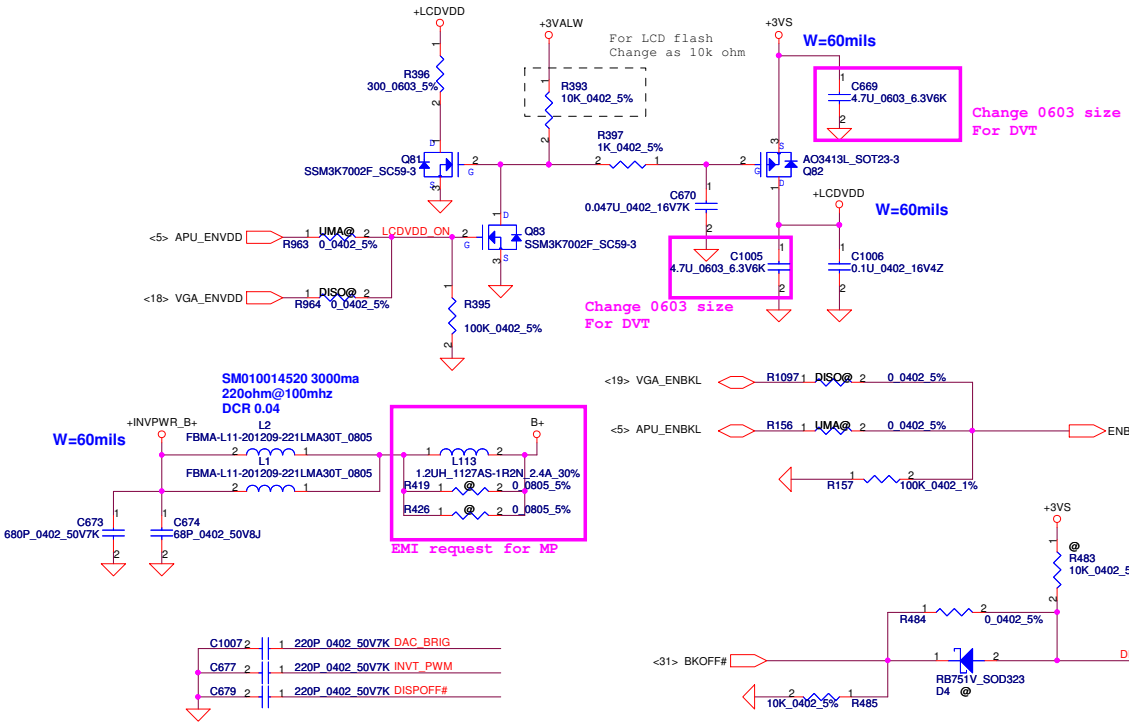
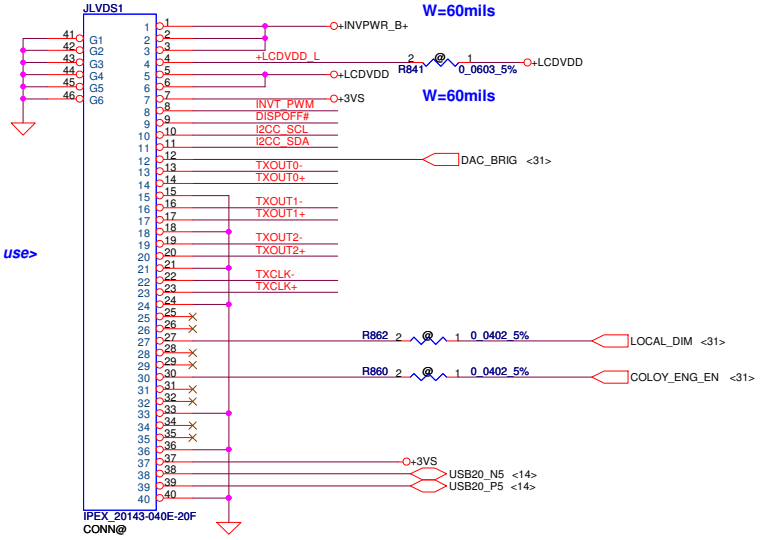
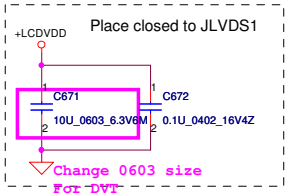
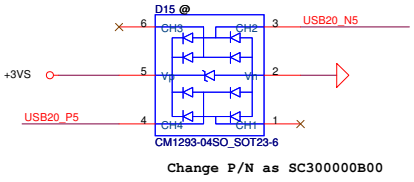
LCD POWER CIRCUIT



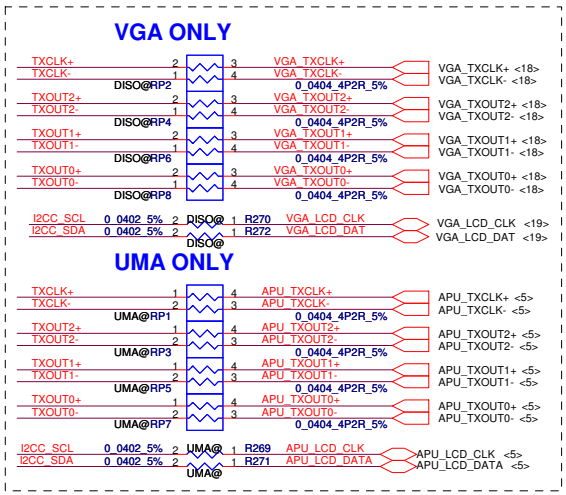
LCD/LED PANEL Conn.

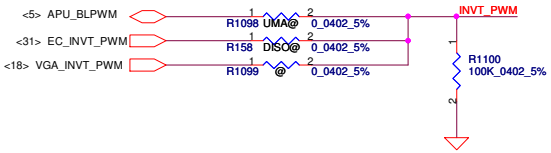






Change P/N as SC300000B00





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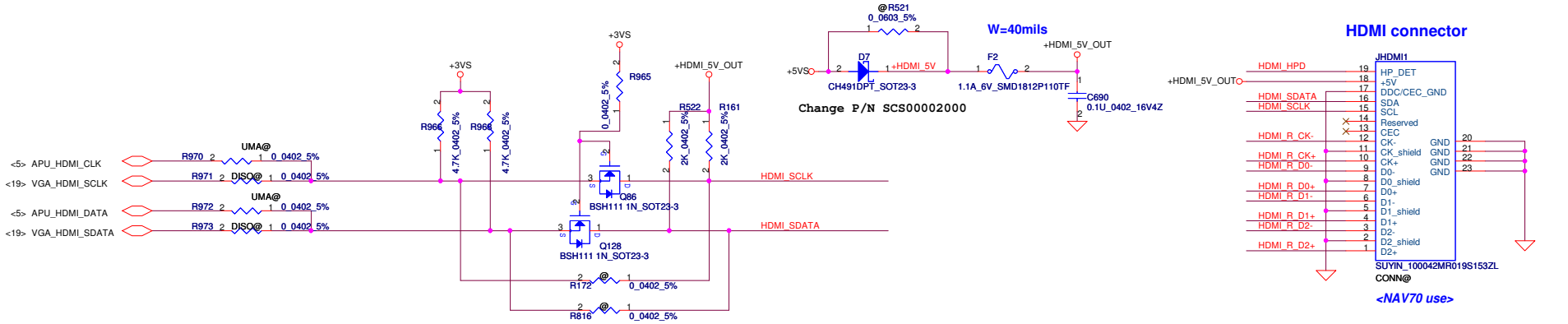
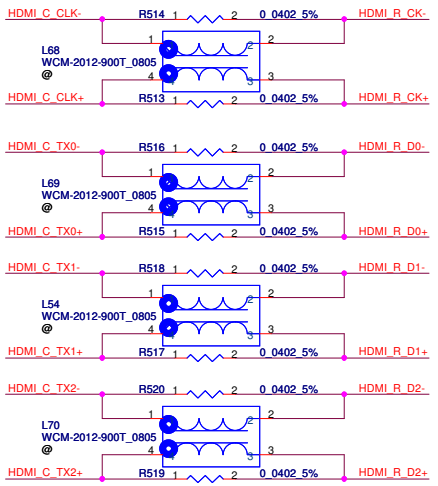
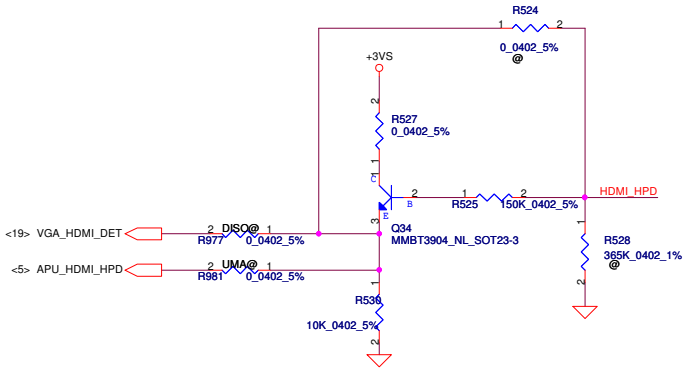


Place closed to JHDMI1

SM070001310 400ma 90ohm@100mhz DCR 0.3

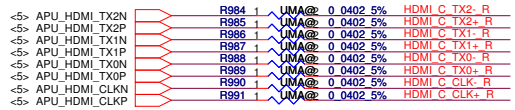




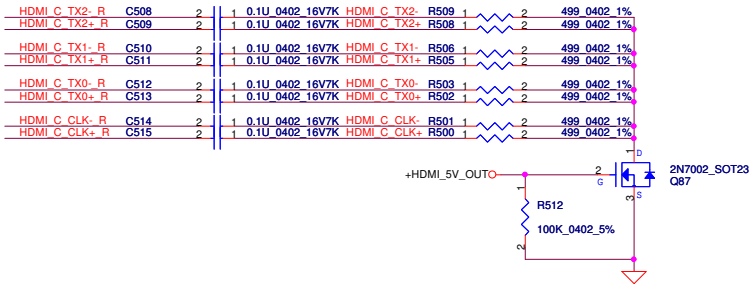
Use common via on related pair

From VGA

From APU



Place closed to JHDMI1



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/20	Deciphered Date 2011/08/20	Title: HDMI Connector

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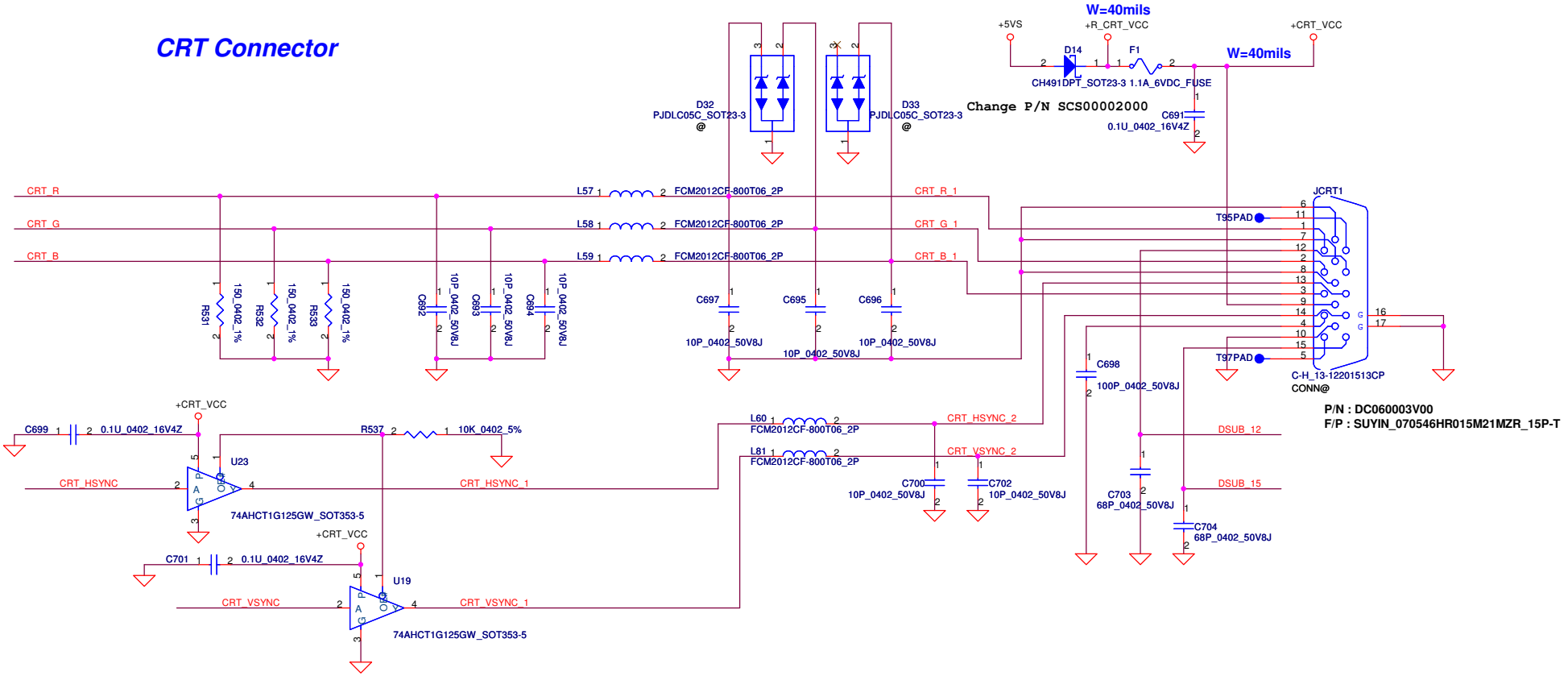
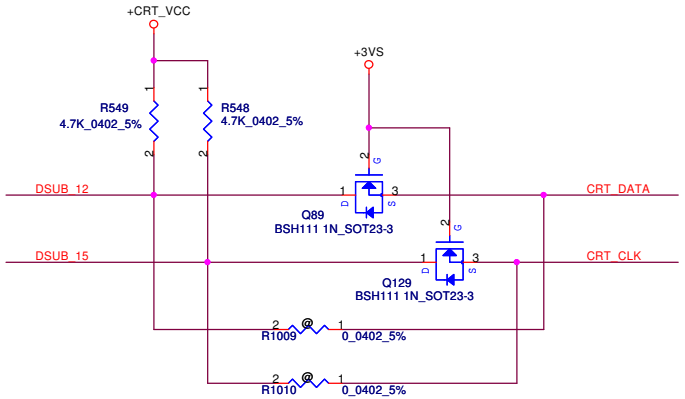
Size: Custom	Document Number: LA-7092P P5WE6/H6/S6		Rev: 1.0
Date: Wednesday, November 24, 2010	Sheet 11 of 47		

CRT Connector



Close to Conn side



Use common via on related pair

From APU

<5> APU_CRT_R	APU_CRT_R	R995	UMA@	0_0402_5%	CRT_R
<5> APU_CRT_G	APU_CRT_G	R996	UMA@	0_0402_5%	CRT_G
<5> APU_CRT_B	APU_CRT_B	R997	UMA@	0_0402_5%	CRT_B
<5> APU_CRT_HSYNC	APU_CRT_HSYNC	R998	UMA@	0_0402_5%	CRT_HSYNC
<5> APU_CRT_VSYNC	APU_CRT_VSYNC	R999	UMA@	0_0402_5%	CRT_VSYNC
<5> APU_CRT_DDC_SDA	APU_CRT_DDC_SDA	R1000	UMA@	0_0402_5%	CRT_DATA
<5> APU_CRT_DDC_SCL	APU_CRT_DDC_SCL	R1001	UMA@	0_0402_5%	CRT_CLK

From VGA

<19> VGA_CRT_R	VGA_CRT_R	R1002	DISO@	0_0402_5%	CRT_R
<19> VGA_CRT_G	VGA_CRT_G	R1003	DISO@	0_0402_5%	CRT_G
<19> VGA_CRT_B	VGA_CRT_B	R1004	DISO@	0_0402_5%	CRT_B
<19> VGA_CRT_HSYNC	VGA_CRT_HSYNC	R1005	DISO@	0_0402_5%	CRT_HSYNC
<19> VGA_CRT_VSYNC	VGA_CRT_VSYNC	R1006	DISO@	0_0402_5%	CRT_VSYNC
<19> VGA_CRT_DATA	VGA_CRT_DATA	R1007	DISO@	0_0402_5%	CRT_DATA
<19> VGA_CRT_CLK	VGA_CRT_CLK	R1008	DISO@	0_0402_5%	CRT_CLK

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: CRT Connector

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

Date: Wednesday, November 24, 2010 | Sheet 12 of 47

For PCIE device reset on FS1 (GFX,GLAN,WLAN,LVDS Travis)

For DVT 1011

U31E

PCIE_RST# P1
A_RST# L1

<31> A_RST#

PCIE_RST_L
A_RST_L

PCI EXPRESS I/F

<6> UMI_RX0P C53 0.1U_0402_16V7K UMI_RX0P_C AD26
<6> UMI_RX0N C54 0.1U_0402_16V7K UMI_RX0N_C AD27
<6> UMI_RX1P C55 0.1U_0402_16V7K UMI_RX1P_C AC28
<6> UMI_RX1N C56 0.1U_0402_16V7K UMI_RX1N_C AC29
<6> UMI_RX2P C57 0.1U_0402_16V7K UMI_RX2P_C AB29
<6> UMI_RX2N C58 0.1U_0402_16V7K UMI_RX2N_C AB28
<6> UMI_RX3P C59 0.1U_0402_16V7K UMI_RX3P_C AB26
<6> UMI_RX3N C60 0.1U_0402_16V7K UMI_RX3N_C AB27

UMI_TX0P
UMI_TX0N
UMI_TX1P
UMI_TX1N
UMI_TX2P
UMI_TX2N
UMI_TX3P
UMI_TX3N

<6> UMI_TX0P AE24
<6> UMI_TX0N AE23
<6> UMI_TX1P AD25
<6> UMI_TX1N AD24
<6> UMI_TX2P AC24
<6> UMI_TX2N AC25
<6> UMI_TX3P AB25
<6> UMI_TX3N AB24

UMI_RX0P
UMI_RX0N
UMI_RX1P
UMI_RX1N
UMI_RX2P
UMI_RX2N
UMI_RX3P
UMI_RX3N

R560 590_0402_1%
R561 2K_0402_1%
+PCIE_VDDAN

PCIE_CALRP AD29
PCIE_CALRN AD28

LAN
WLAN

<26> PCIE_FTX_C_DRX_P2 C61 0.1U_0402_16V7K PCIE_FTX_DRX_P2 AA28
<26> PCIE_FTX_C_DRX_N2 C62 0.1U_0402_16V7K PCIE_FTX_DRX_N2 AA29
<29> PCIE_FTX_C_DRX_P3 C717 0.1U_0402_16V7K PCIE_FTX_DRX_P3 Y29
<29> PCIE_FTX_C_DRX_N3 C63 0.1U_0402_16V7K PCIE_FTX_DRX_N3 Y28

GPP_TX0P
GPP_TX0N
GPP_TX1P
GPP_TX1N
GPP_TX2P
GPP_TX2N
GPP_TX3P
GPP_TX3N

W28
Y27
Y26
W29

GPP_RX0P
GPP_RX0N
GPP_RX1P
GPP_RX1N
GPP_RX2P
GPP_RX2N
GPP_RX3P
GPP_RX3N

AA22
Y21
AA25
AA24

<26> PCIE_FRX_DTX_P2 W23
<26> PCIE_FRX_DTX_N2 V24
<29> PCIE_FRX_DTX_P3 W24
<29> PCIE_FRX_DTX_N3 W25

close to FCH within 1"

PCIE_RCLKP/NB_LNK_CLKP M23
PCIE_RCLKN/NB_LNK_CLKN P23

CLOCK GENERATOR

<5> APU_DISP_CLKP R564 0_0402_5% APU_DISP_CLKP_R U29
<5> APU_DISP_CLKN R565 0_0402_5% APU_DISP_CLKN_R U28

NB_DISP_CLKP
NB_DISP_CLKN

NB_HT_CLKP T26
NB_HT_CLKN T27

<5> APU_CLKP R162 0_0402_5% APU_CLKP_R V21
<5> APU_CLKN R163 0_0402_5% APU_CLKN_R T21

CPU_HT_CLKP
CPU_HT_CLKN

<18> CLK_PCIE_VGA R569 0_0402_5% CLK_PCIE_VGA_R V23
<18> CLK_PCIE_VGA# R570 0_0402_5% CLK_PCIE_VGA#_R T23

SLT_GFX_CLKP
SLT_GFX_CLKN

LAN
<26> CLK_PCIE_LAN R571 0_0402_5% CLK_PCIE_LAN_R L29
<26> CLK_PCIE_LAN# R572 0_0402_5% CLK_PCIE_LAN#_R L28

GPP_CLK0P
GPP_CLK0N

WLAN
<29> CLK_PCIE_MINI1 R573 0_0402_5% CLK_PCIE_MINI1_R N29
<29> CLK_PCIE_MINI1# R574 0_0402_5% CLK_PCIE_MINI1#_R N28

GPP_CLK1P
GPP_CLK1N

M29
M28

GPP_CLK2P
GPP_CLK2N

T25
V25

GPP_CLK3P
GPP_CLK3N

L24
L23

GPP_CLK4P
GPP_CLK4N

P25
M25

GPP_CLK5P
GPP_CLK5N

P29
P28

GPP_CLK6P
GPP_CLK6N

N26
N27

GPP_CLK7P
GPP_CLK7N

T29
T28

GPP_CLK8P
GPP_CLK8N

Follow result by vender 10/11

<29> CLK_SD_48M L25
14M_25M_48M_OSC

C66 27P_0402_50V8J
C67 27P_0402_50V8J
Y3
1M_0603_5%
R576
25MHZ_20PF_7A25000012

25M_CLK_X1 L26
25M_X1

25M_CLK_X2 L27
25M_X2

21807-A11-HUDSON-M1_FCBGA605

Close to FCH

C64 22P_0402_50V8J
C65 22P_0402_50V8J
R563 20M_0603_5%
Y4
32.768KHZ_12.5PF_Q13MC14610050_10PPM
RTC_32KHI
RTC_32KHO

FCH : SA000046H60 (S IC 218-0792001 A12 HUDSON-M1 FCBGA 605P)
FCH : SA000046H70 (S IC 218-0792006 A13 HUDSON-M1 FCBGA 605P)
FCH : SA000046HA0 R1

PCI CLKS

PCICLK0 W2 PADT96
PCICLK1/GPO36 W1 PCI_CLK1 <17>
PCICLK2/GPO37 W3 PCI_CLK2 <17>
PCICLK3/GPO38 W4 PCI_CLK3 <17>
PCICLK4/14M_OSC/GPO39 Y1 PCI_CLK4 <17>

PCIRST_L V2 PADT92

PCI I/F

AD0/GPIO0 AA1
AD1/GPIO1 AA4
AD2/GPIO2 AA3
AD3/GPIO3 AB1
AD4/GPIO4 AA5
AD5/GPIO5 AB2
AD6/GPIO6 AB6
AD7/GPIO7 AB5
AD8/GPIO8 AA6
AD9/GPIO9 AC2
AD10/GPIO10 AC3
AD11/GPIO11 AC4
AD12/GPIO12 AC1
AD13/GPIO13 AD1
AD14/GPIO14 AD2
AD15/GPIO15 AC6
AD16/GPIO16 AE2
AD17/GPIO17 AE1
AD18/GPIO18 AF8
AD19/GPIO19 AE3
AD20/GPIO20 AF1
AD21/GPIO21 AG1
AD22/GPIO22 AF2
AD23/GPIO23 AE9
AD24/GPIO24 AD9
AD25/GPIO25 AC11
AD26/GPIO26 AF6
AD27/GPIO27 AF4
AD28/GPIO28 AF3
AD29/GPIO29 AH2
AD30/GPIO30 AG2
AD31/GPIO31 AH3
CBE0_L AA8
CBE1_L AD5
CBE2_L AD8
CBE3_L AA10
FRAME_L AE8
DEVSEL_L AB9
IRDY_L AJ3
TRDY_L AE7
PAR AC5
STOP_L AF5
PERR_L AE6
SERR_L AE4
REQ0_L AE11
REQ1_L/GPIO40 AH5
REQ2_L/CLK_REQ8_L/GPIO41 AH4
REQ3_L/CLK_REQ5_L/GPIO42 AC12
GNT0_L AD12
GNT1_L/GPO44 AJ5
GNT2_L/GPO45 AH6
GNT3_L/CLK_REQ7_L/GPIO46 AB12
CLKRUN_L AB11
LOCK_L AD7

INTE_L/GPIO32 AJ6
INTF_L/GPIO33 AG6
INTG_L/GPIO34 AG4
INTH_L/GPIO35 AJ4

PCI_AD23 <17>
PCI_AD24 <17>
PCI_AD25 <17>
PCI_AD26 <17>
PCI_AD27 <17>

PE_GPIO0 <18>
PE_GPIO1 <24,35>

R99 10K_0402_5%

VGA_PWRGD_R

LPC

LPCCLK0 H24 R853 0_0402_5% LPC_CLK0 <17>
LPCCLK1 H25 R575 22_0402_5% LPC_CLK0_EC <31>
LAD0 J27 LPC_AD0 <31>
LAD1 J26 LPC_AD1 <31>
LAD2 H29 LPC_AD2 <31>
LAD3 H28 LPC_AD3 <31>
LFRAME_L G28 LPC_FRAME# <31>
LDRQ0_L J25
LDRQ1_L/CLK_REQ6_L/GPIO49 AA18
SERIRQ/GPIO48 AB19 SERIRQ <31>

CPU

ALLOW_LDTSTP/DMA_ACTIVE_L G21 ALLOW_STOP# <5>
PROCHOT_L H21 FCH_PROCHOT# <5>
LDT_PG K19 APU_PWRGD <5>
LDT_STP_L G22
LDT_RST_L J24 APU_RST# <5>

RTC

32K_X1 C1 RTC_32KHI
32K_X2 C2 RTC_32KHO

RTCCLK D2 RTC_CLK <17,31>
INTRUDER_ALERT_L B2
VDDBT_RTC_G B1

C1272 0.1U_0402_16V4Z
C1271 1U_0402_6.3V4Z
R864 510_0402_5% W=20mils
R865 0_0603_5%
for Clear CMOS

+RTCVCC
C1270 0.1U_0402_16V4Z
D23 DAN202UT106_SC70-3
+RTCBATT
R179 1K_0402_5%
+CHGRTC

+3VALW
C1234 0.1U_0402_16V4Z
A_RST# R175 33_0402_5%
C1233 150P_0402_50V8J
R174 8.2K_0402_5%
U28 NC7SZ08P5X_NL_SC70-5
PLT_RST# <18,26,29>
PCIE_RST# R582 0_0402_5%

+1.8VS +3VS
R164 10K_0402_5%
APU_PWRGD
FDV301N_NL_SOT23-3 Q90
H_PWRGD_L <44>

+3VALW
C1199 0.1U_0402_16V4Z
U33 NC7SZ08P5X_NL_SC70-5
VGA_PWRGD <24,43>
VGA_PWRGD_R
R830 0_0402_5%
R838 100K_0402_5%
R839 0_0402_5%
For DVT 1011

RTC BATT Conn.

+RTCBATT
CONN@ JBATT2
SUYIN_060003HA002G202ZL
P/N: SP07000OU00
F/P: SUYIN_060003HA002G202ZL_2P

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Issued Date	2010/08/20	Deciphered Date	2011/08/20

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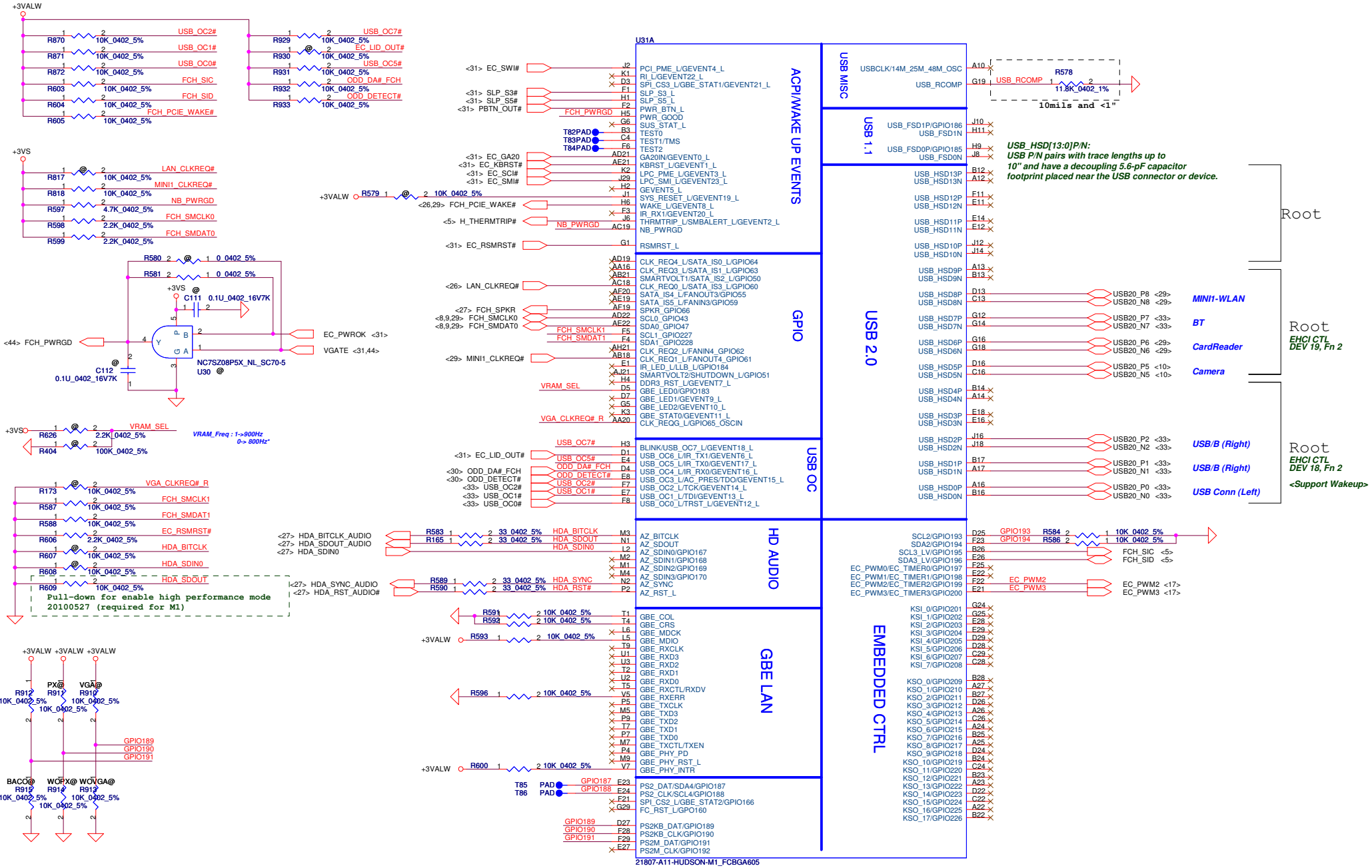
Compal Electronics, Inc.

Title: FCH PCIE/PCI/ACPI/LPC/RTC

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

Date: Wednesday, November 24, 2010 | Sheet 13 of 47



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Issued Date	2010/08/20	Deciphered Date	2011/08/20

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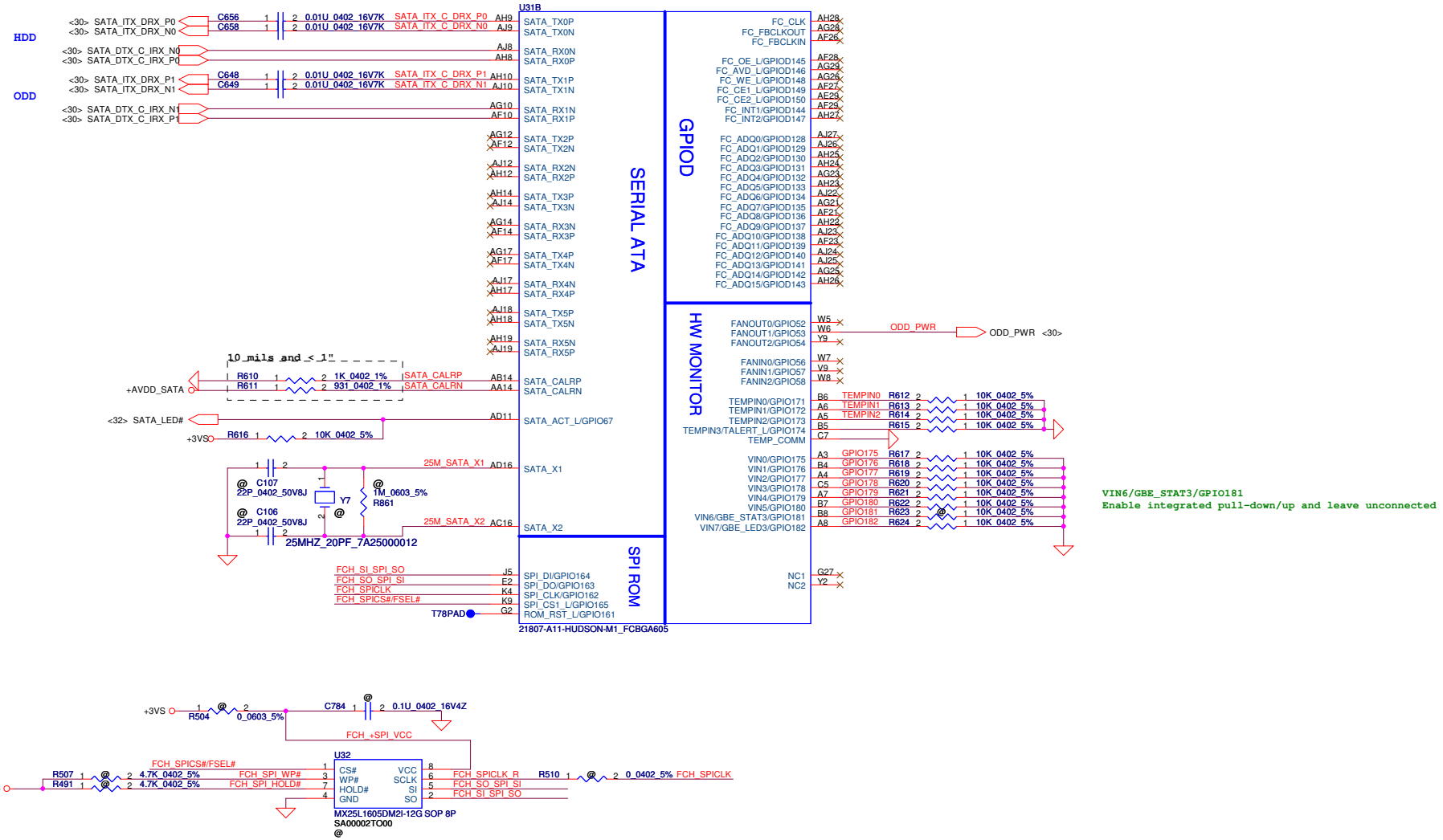
Compal Electronics, Inc.	
Title	FCH HDA/USB/ACPI
Size: B/5 Custom	Document Number: LA-7092P P5WE6/H6/S6
Rev	1.0
Date: Wednesday, November 24, 2010	Sheet 14 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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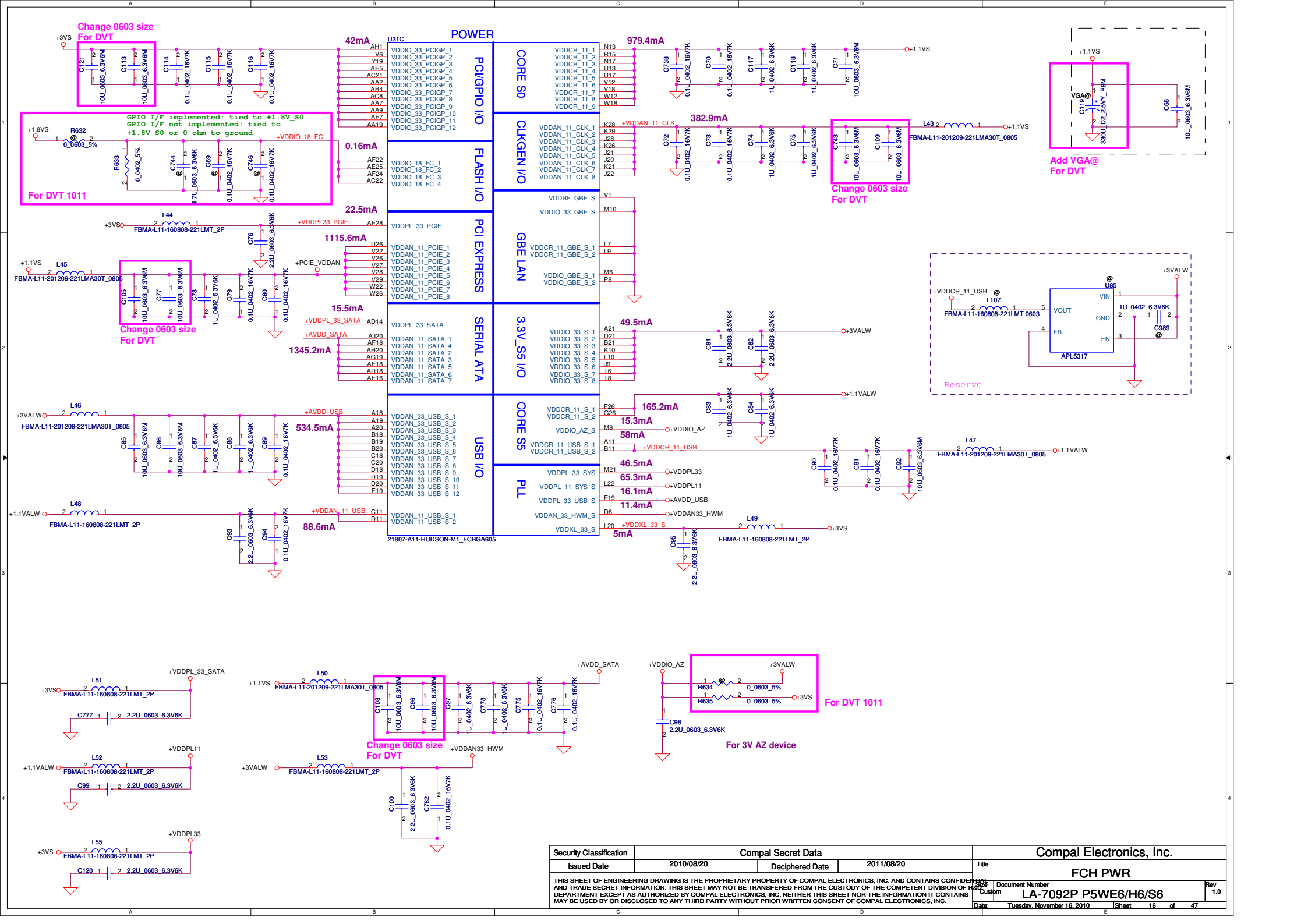
Compal Electronics, Inc.

Title: FCH-SATA/SPI

Size: B (Custom) | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

Date: Wednesday, November 24, 2010 | Sheet 15 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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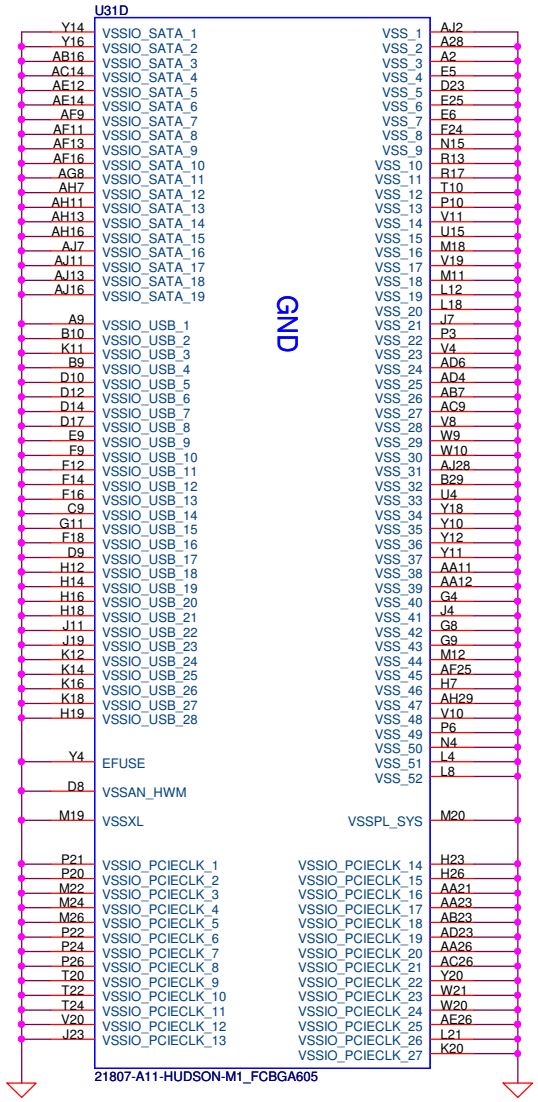
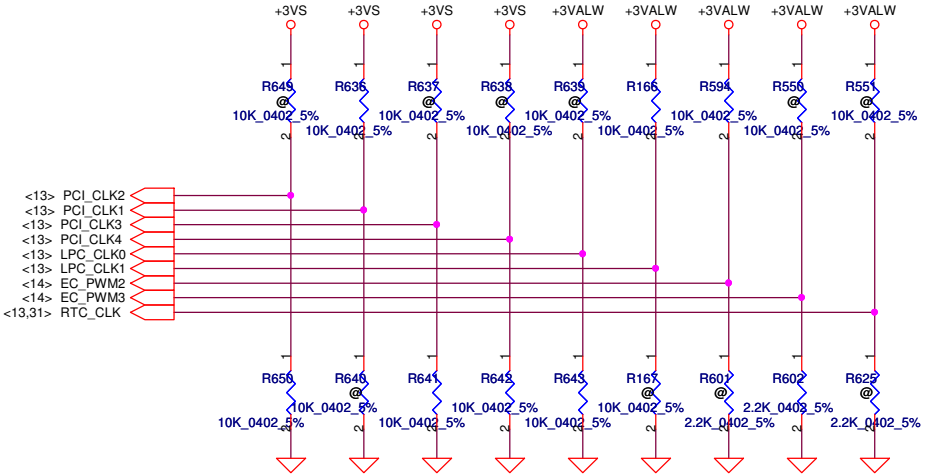
Compal Electronics, Inc.			
Title: FCH PWR			
Size: Custom	Document Number: LA-7092P P5WE6/H6/S6		Rev: 1.0
Date: Tuesday, November 16, 2010	Sheet 16 of 47		



REQUIRED STRAPS

Check Internal PU/PD

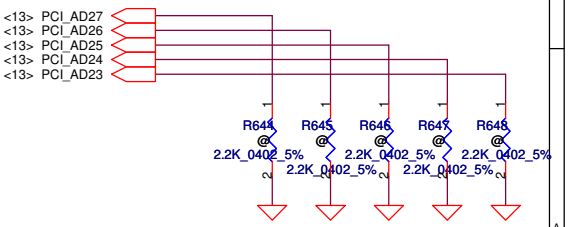
	PCI_CLK2	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	RTC_CLK	EC_PWM2 EC_PWM3
PULL HIGH	WATCHDOG TIMER ENABLE	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAP	NON Fusion CLOCK Mode	internal EC ENABLE	Internal CLKGEN Mode DEFAULT	S5 PLUS MODE DISABLED DEFAULT	LPC ROM (H.L) DEFAULT
PULL LOW	WATCHDOG TIMER DISABLE DEFAULT	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	Fusion CLOCK Mode DEFAULT	internal EC DISABLE DEFAULT	External CLKGEN Mode	S5 PLUS MODE ENABLED	SPI ROM(L,H)



DEBUG STRAPS

FCH M1 HAS 15K INTERNAL PU FOR PCI_AD[27:23]

		PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23 Enable ROM Straps
PULL HIGH		USE internal PLL generated PLL CLK DEFAULT	ILA AUTORUN Disabled DEFAULT	Selects FC PLL DEFAULT	Disable I2C ROM DEFAULT	Required Setting DEFAULT
PULL LOW		BYPASS PCI PLL	ILA AUTORUN Enabled	FC PLL bypassed	Getting Value from I2C EPROM	Reserved



Check AD29,AD28 strap function check default

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2010/08/20	Deciphered Date 2011/08/20	Title: FCH-VSS/Strap
			Size: B; Document Number: LA-7092P P5WE6/H6/S6; Rev: 1.0
			Date: Wednesday, November 24, 2010; Sheet 17 of 47

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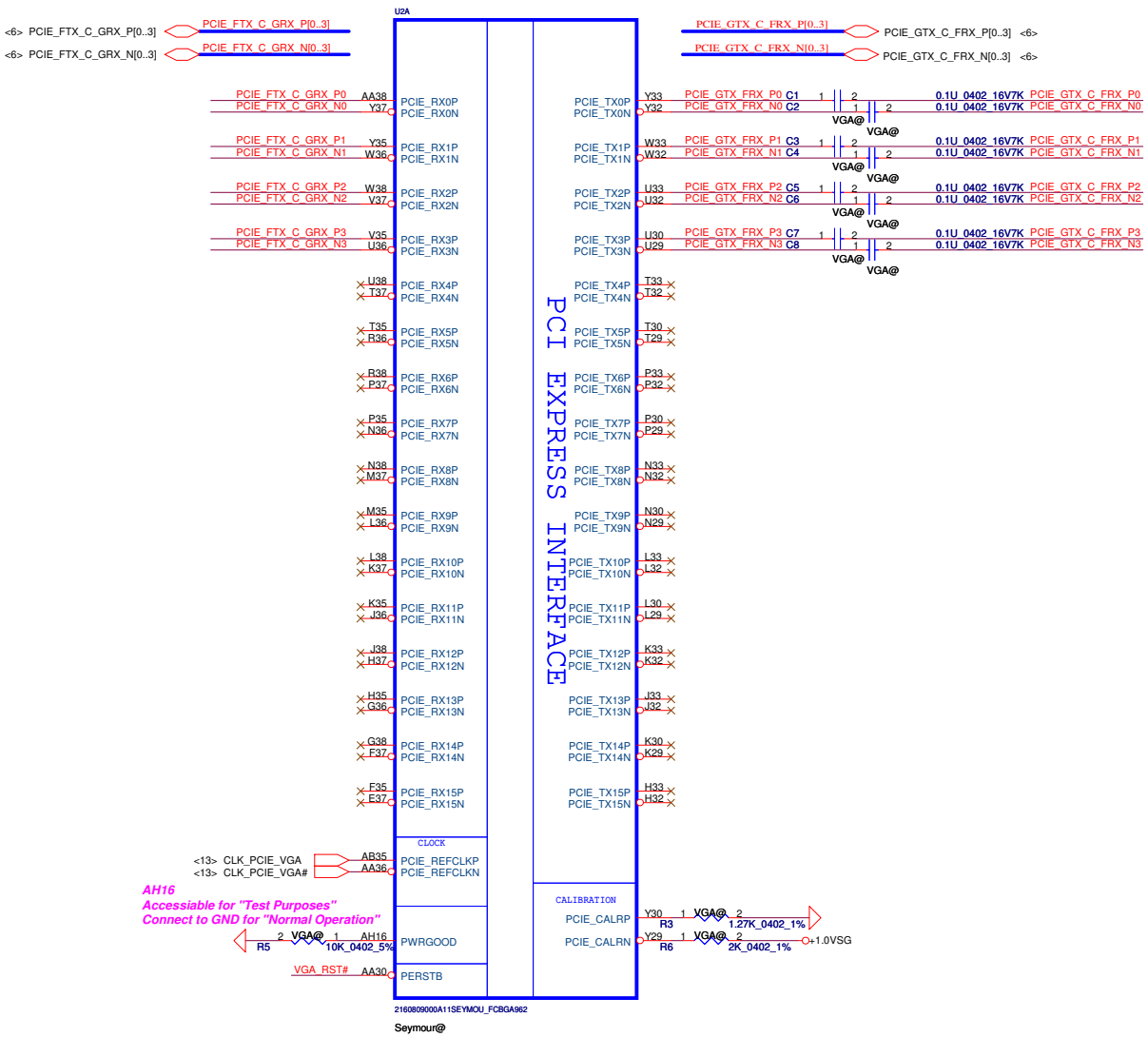
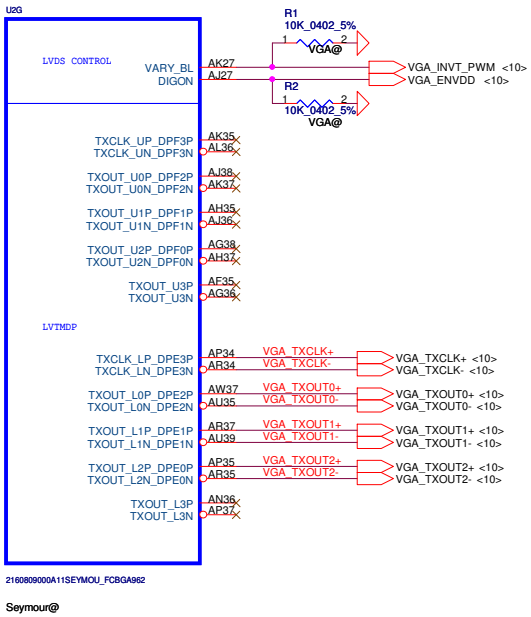
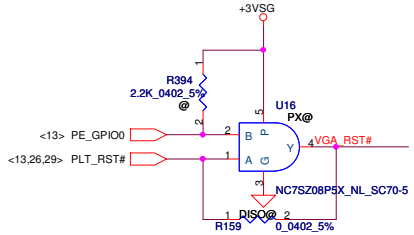
GFX PCIE LANE REVERSAL



add for VB support.





Seymour XT P/N: SA000047H10 (S IC 216-0809000 A11 SEYMOUR XT M2)

Robson XT P/N: SA00004DR20 (S IC 216-0774211 A11 Robson XT M2)

U2 Robson@

Robson XT-M2 A11

Robson A11 (SA00004DR20)

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Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: Vancouver_ PCIE / LVDS

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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Strap Name		Pin Straps description <all internal PD>	Setting
VIP_DEVICE_EN	V2SYNC (GENLK_VSYNC)	VIP Device Strap Enable indicates to the software driver 0: Driver would ignore the value sampled on VHAD_0 during reset 1: VHAD_0 to determine whether or not a VIP slave device	0
VGA_DIS	GPIO9	VGA Disable determines 0: VGA Controller capacity enabled 1: The device will not be recognized as the system's VGA controller	0
TX_PWRS_ENB	GPIO0	Transmitter Power Saving Enable 0: 80% Tx output swing for mobile mode 1: full Tx output swing (Default setting for Desktop)	1
TX_DEEMPH_EN	GPIO1	PCI Express Transmitter De-emphasis Enable 0: Tx de-emphasis diabled for mobile mode 1: Tx de-emphasis enabled (Defailt setting for desktop)	1
CONFIG[2] CONFIG[1] CONFIG[0]	GPIO13 GPIO12 GPIO11	GPIO13,12,11 (config 2,1,0) : memory apertures a) If BIOS_ROM_EN = 1, then Config[2:0] defines the ROM type. CONFIG[3:0] 128 MB 000 b) If BIOS_ROM_EN = 0, then Config[2:0] defines the primary memory aperture size. 256 MB 001 * 64 MB 010	001
BIOS_ROM_EN	GPIO22	Enable external BIOS ROM device 0: Diable, 1: Enable	0
AUD[1] AUD[0]	HSYNC VSYNC	00: No audio function; 10: Audio for DisplayPort only; 01: Audio for DisplayPort and HDMI if adapter is detected; 11: Audio for both DisplayPort and HDMI	11
BIF_GEN2_EN	GPIO2	0= Advertises the PCI-E device as 2.5 GT/s capable at power-on 1= Advertises the PCI-E device as 5.0 GT/s capable at power-on 5.0 GT/s capability will be controlled by software	0
RESERVED	H2SYNC (GENLK_CLK) GPIO8 GPIO21 GENERICC GPIO5	Internal use only. THIS PAD HAS AN INTERNAL PULL-DOWN AND MUST BE 0 V AT RESET. The pad may be left unconnected	DNI

Don't have this strap on Whistler and Seymour

External VGA Thermal Sensor

U4 VGA@ ADM1032ARMZ-2REEL_MSOP8

Address 1001 101X b

Robson (XT)/Seymour(XT)

VRAM \ Location	VRAM_ID3 <vendor1>	VRAM_ID2 <pcs>	VRAM_ID1 <vendor2>	VRAM_ID0 <size>
Samsung SA00004GS10 G-die K4W1G1646G-BC11	0	0 <4 pcs>	1	1
Hynix SA00003242O Orion-die H5TQ1G63BFR-12C	1	1 <4 pcs>	0	0
Hynix SA00004lS40 Vega-die H5TQ1G63DFR-11C	1	1 <4 pcs>	1	0

change VGA@ as DISO@ For PVT

Internal PD

PD-Reset

FLASH ROM

U5 TYPE 1 M25P10-AVMN6P

AL31 Manhattan/Vancouver is NC, Boardway is ADC input(0-1V) use measure regulator current or temperature

GPIO_0 will use to control PSI in the future product

Change 0603 size For DVT

In Whistler and Seymour, change to GENLK_CLK, GENLK_VSYNC for Global Swap Lock on multiple GPUs

Except A2VSSQ change to TSVSSQ, others are NC on Whistler and Seymour

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Compal Electronics, Inc.

Title: Vancouver_Strape/DP/HDMI//CRT

Size	Document Number	Rev
Custom	LA-7092P P5WE6/H6/S6	1.0

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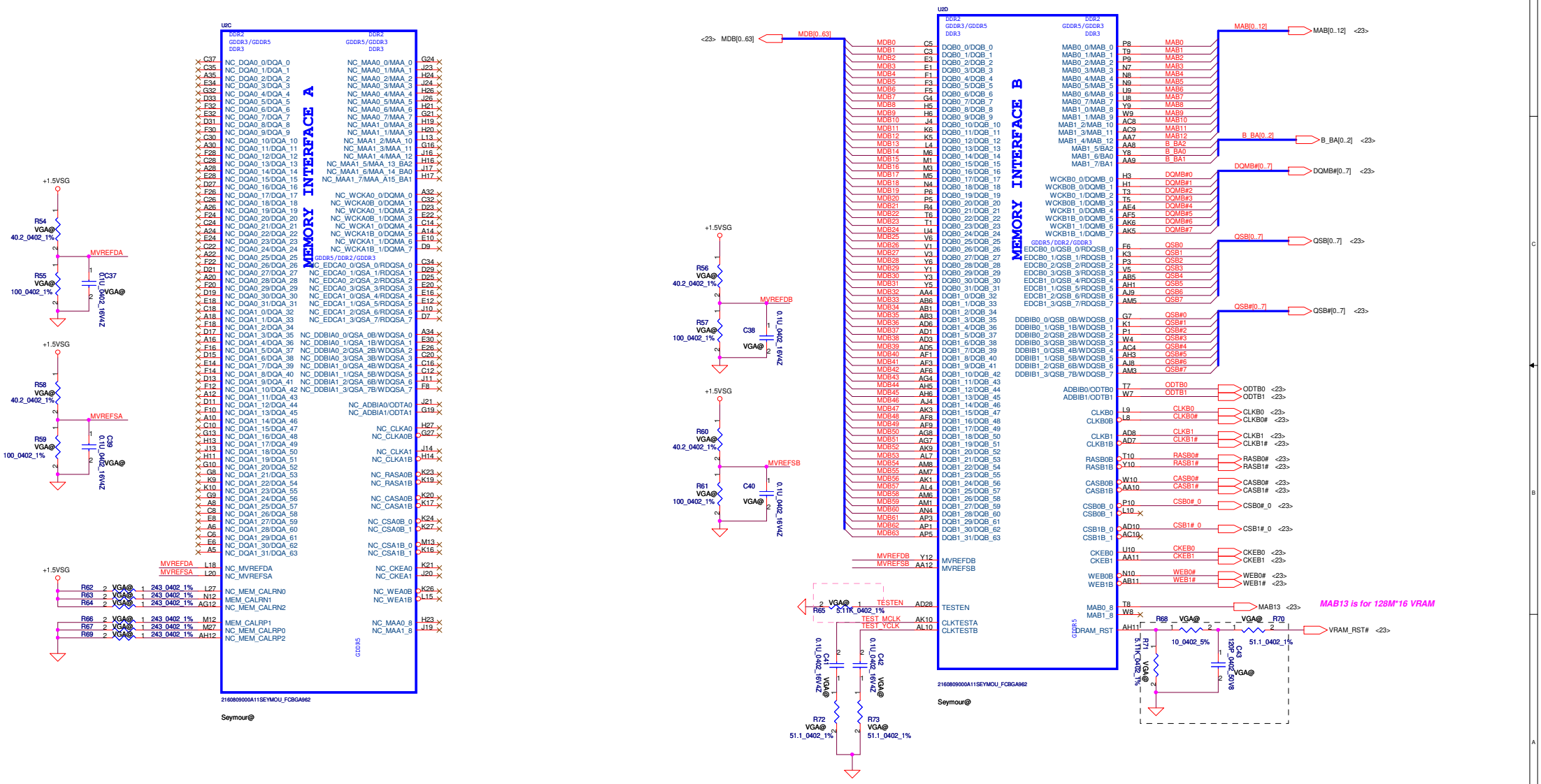
Robson,Seymour only support single channel memory (channel B only)



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Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: Vancouver_Memory

Size	Document Number	Rev
Custom	LA-7092P P5WE6/H6/S6	1.0

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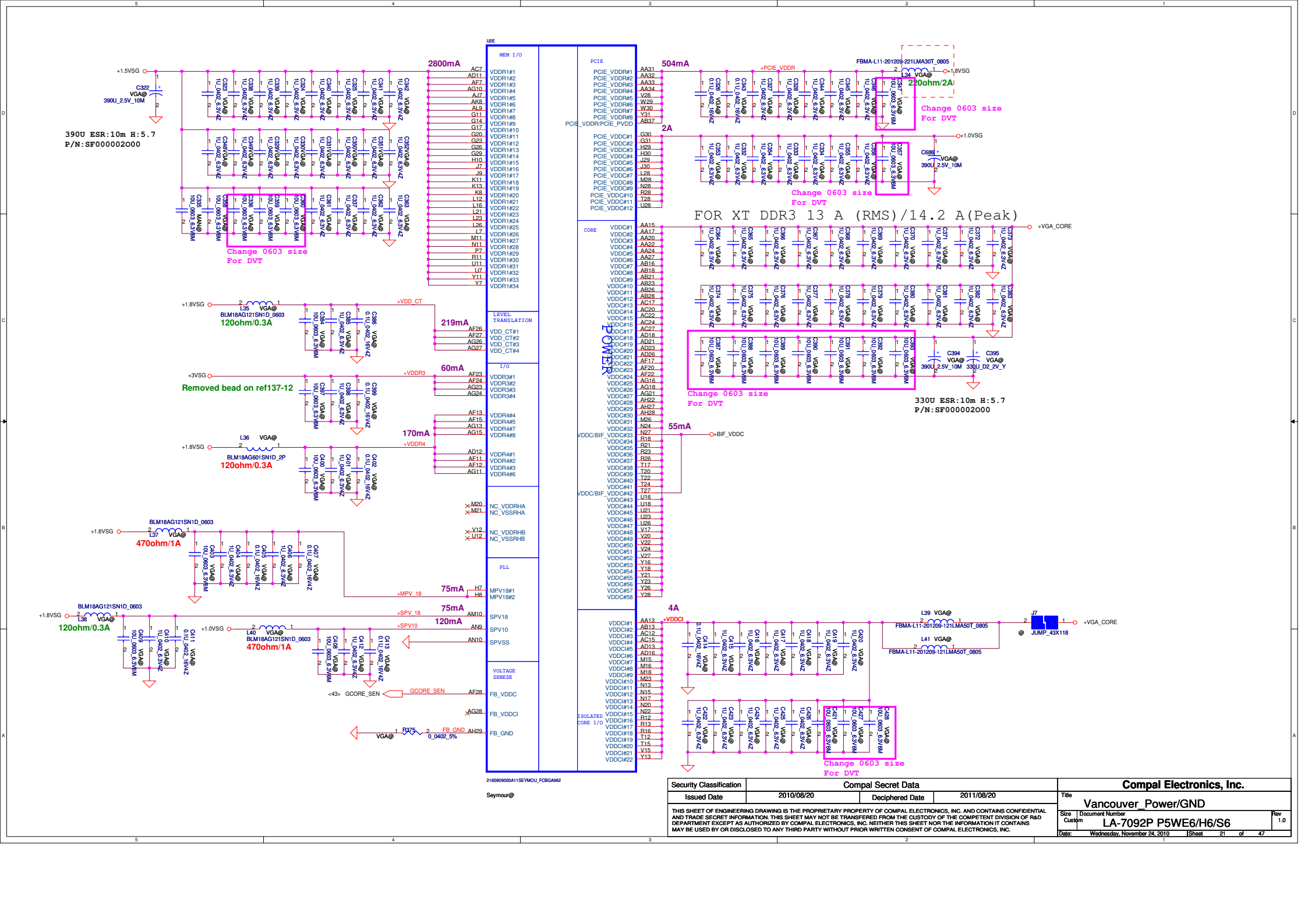

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Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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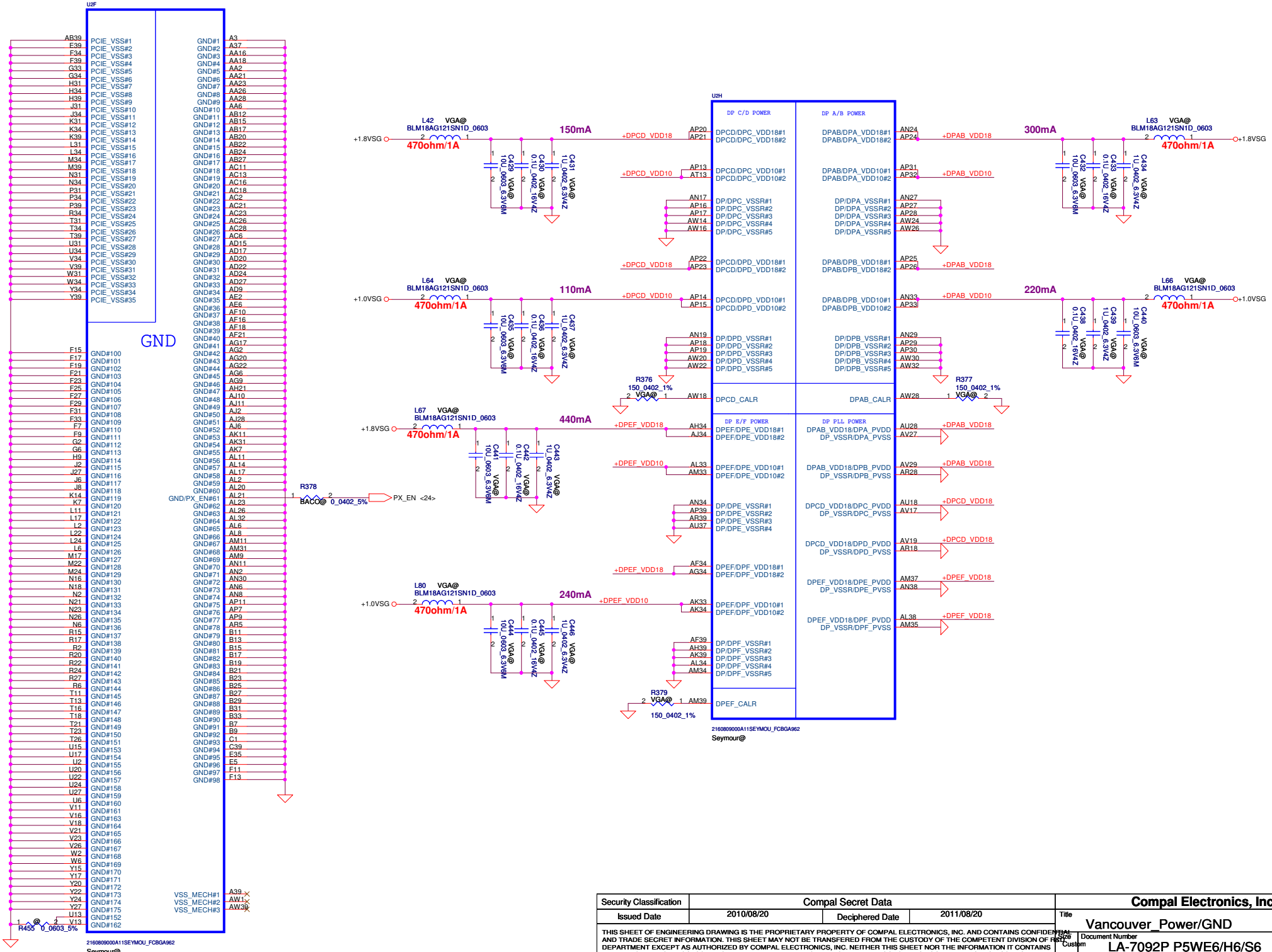

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: Vancouver_Power/GND

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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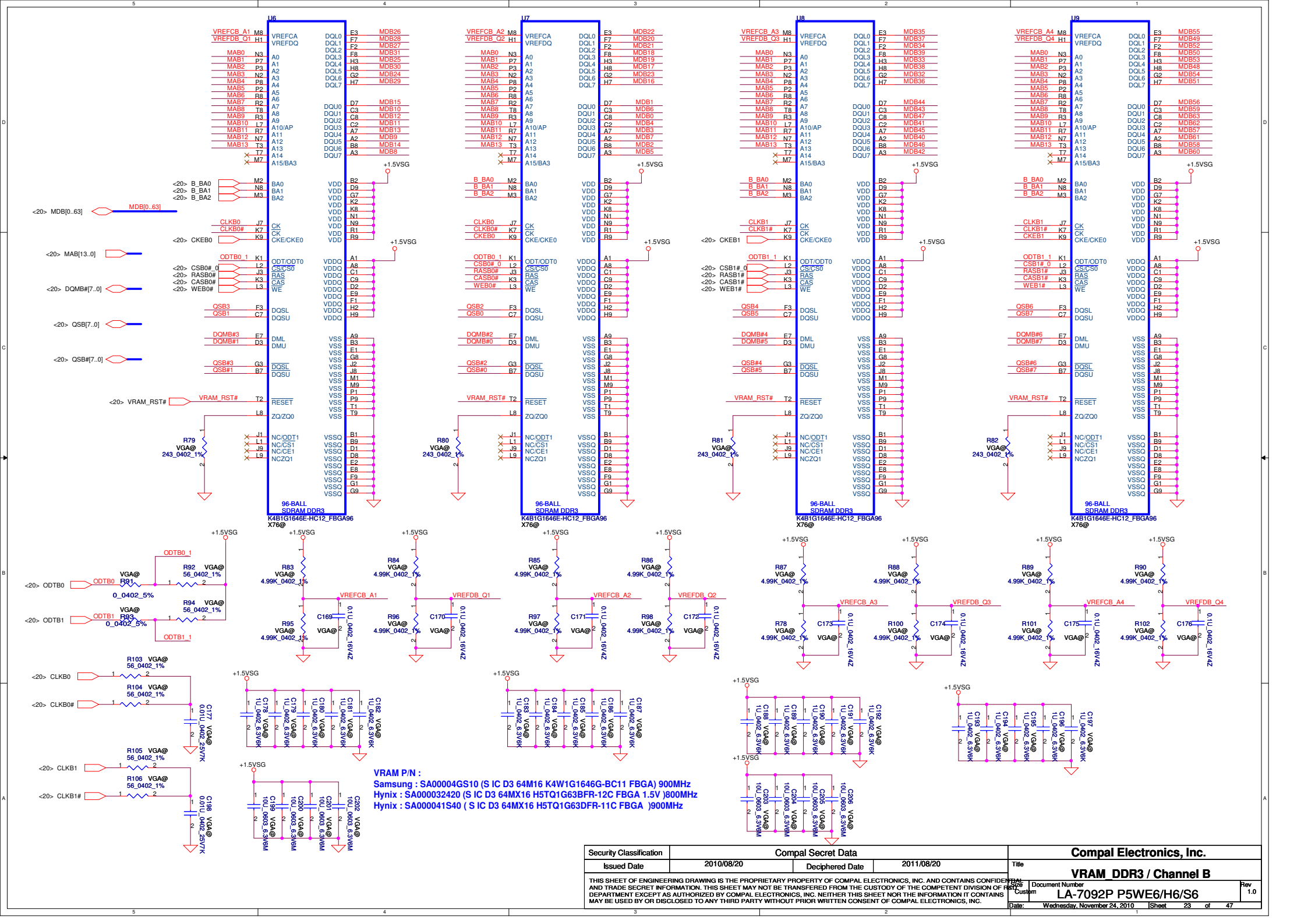

VRAM P/N :

Samsung : SA00004GS10 (S IC D3 64M16 K4W1G1646G-BC11 FBGA) 900MHz

Hynix : SA000032420 (S IC D3 64MX16 H5TQ1G63BFR-12C FBGA 1.5V)800MHz

Hynix : SA000041S40 (S IC D3 64MX16 H5TQ1G63DFR-11C FBGA)900MHz

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Compal Electronics, Inc.

Title: **VRAM_DDR3 / Channel B**

Size	Document Number	Rev
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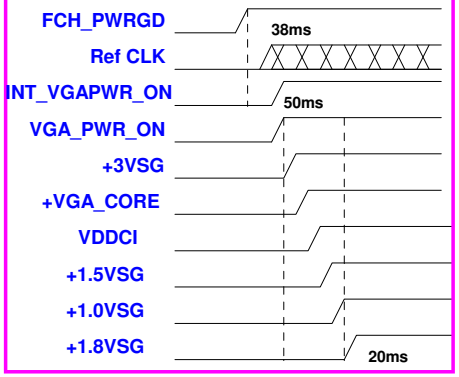
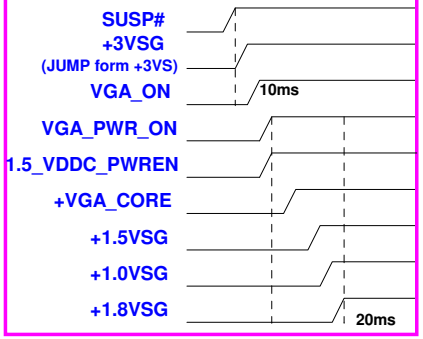
Power Sequence of Granville



For PX sequence, >1mS delay is required between PE_GPIO1 and VGA_PWR_ON

Power Sequence of Whistler and Seymour

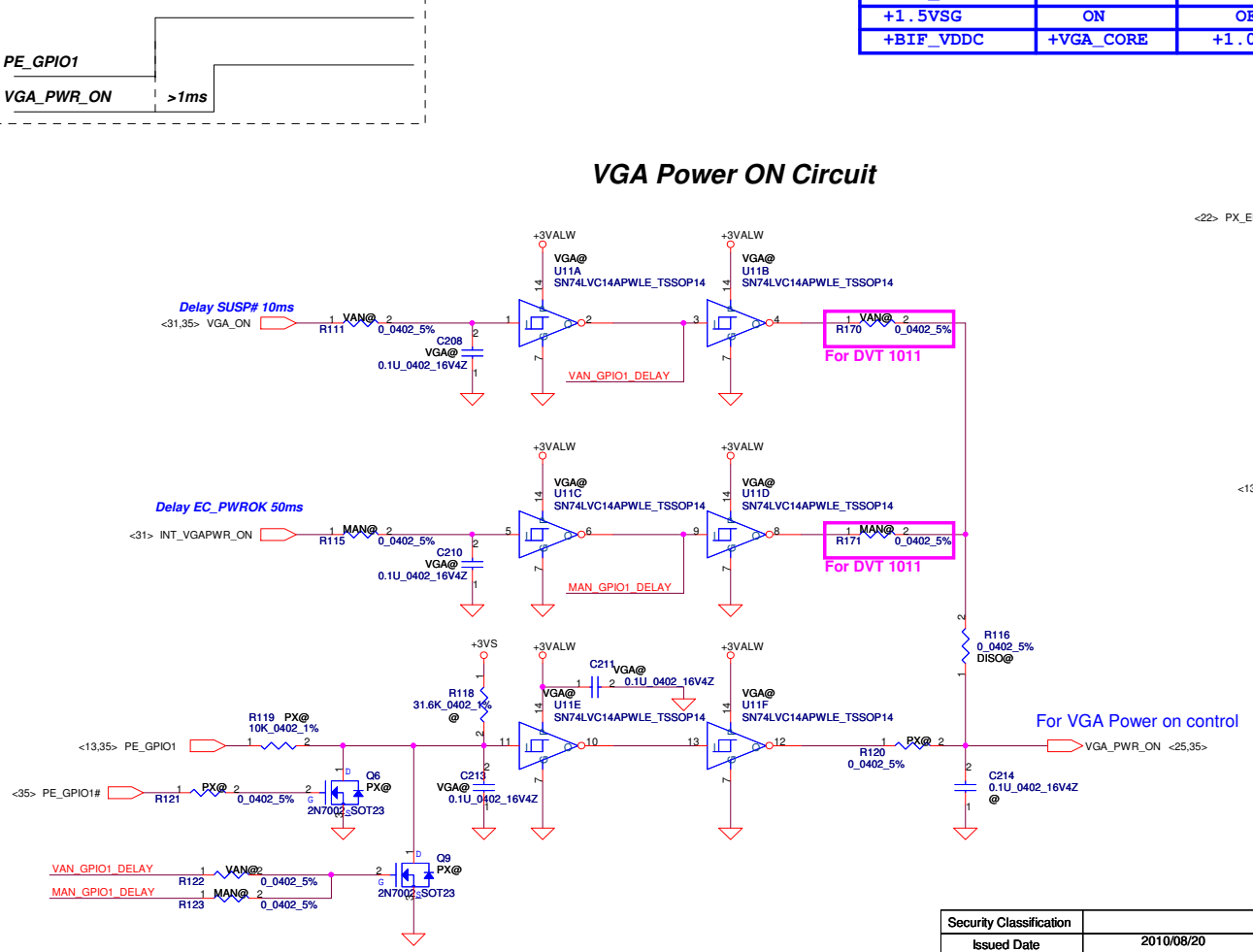


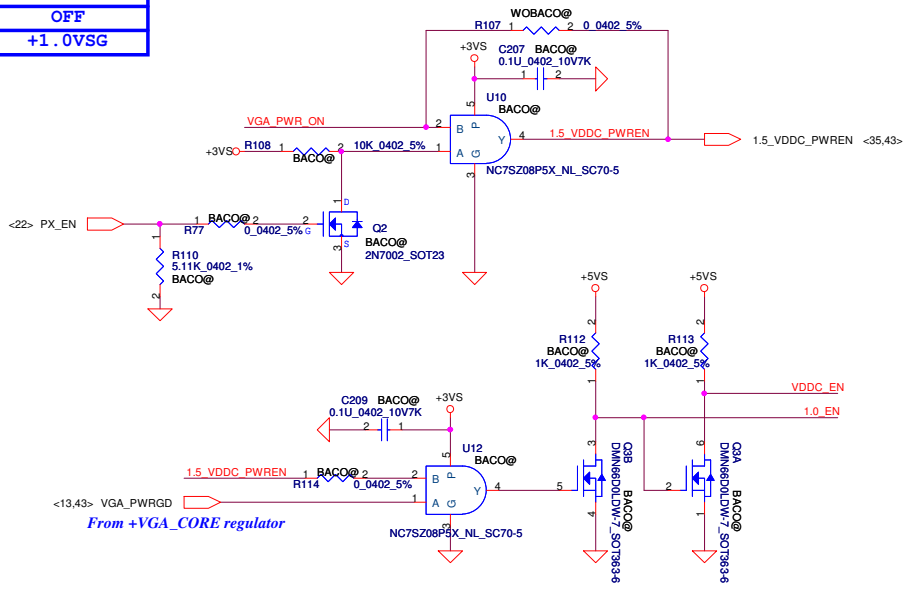
VGA Muxless and Dis only Status Mapping table			
	Dis only	Muxless High performance GPU	Muxless Power-saving GPU
VGA_PWR_ON	1	1	0
1.5_VDDC_PWREN	1	1	0
+3.3VSG	ON	ON	OFF
+1.8VSG	ON	ON	OFF
+1.0VSG	ON	ON	OFF
+VGA_CORE	ON	ON	OFF
+1.5VSG	ON	ON	OFF
+BIF_VDDC	+VGA_CORE	+VGA_CORE	OFF

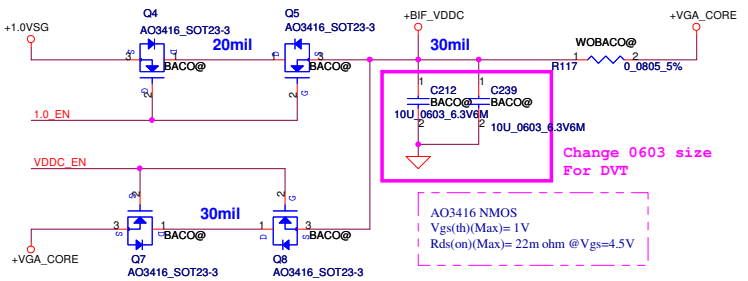
VGA Muxless with BACO Status Mapping table		
	Normal mode	BACO mode
PX_EN	0	1
1.5_VDDC_PWREN	1	0
VDDC_EN	1	0
1.0_EN	0	1
+3.3VSG	ON	ON
+1.8VSG	ON	ON
+1.0VSG	ON	ON
+VGA_CORE	ON	OFF
+1.5VSG	ON	OFF
+BIF_VDDC	+VGA_CORE	+1.0VSG

VGA Power Enable Signal Mapping table		
	Graville	Whistler and Seymour
VGA_PWR_ON source signal	INT_VGAPWR_ON	VGA_ON
+3.3VSG	VGA_PWR_ON	SUSP#
+1.8VSG	VGA_PWR_ON	VGA_PWR_ON
+1.0VSG	VGA_PWR_ON	VGA_PWR_ON
+VDDCI	VGA_PWR_ON	Combine with +VGA_CORE
+VGA_CORE	VGA_PWR_ON	1.5_VDDC_PWREN
+1.5VSG	VGA_PWR_ON	1.5_VDDC_PWREN

VGA Power ON Circuit







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Compal Electronics, Inc.

Title: VGA power sequence and BACO

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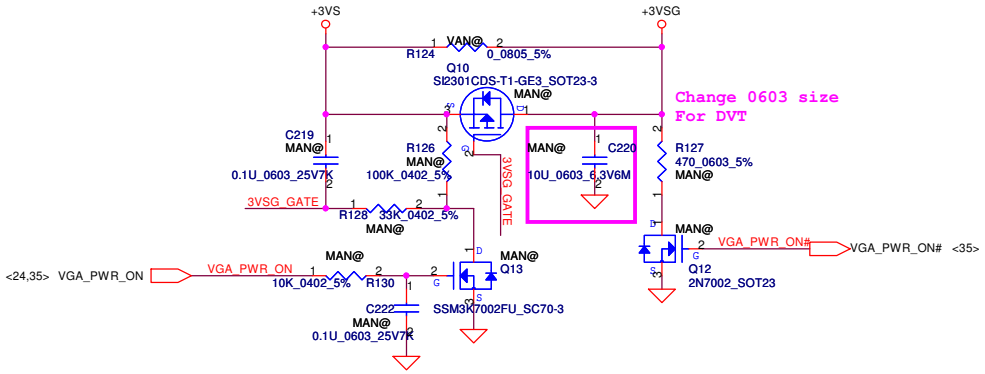
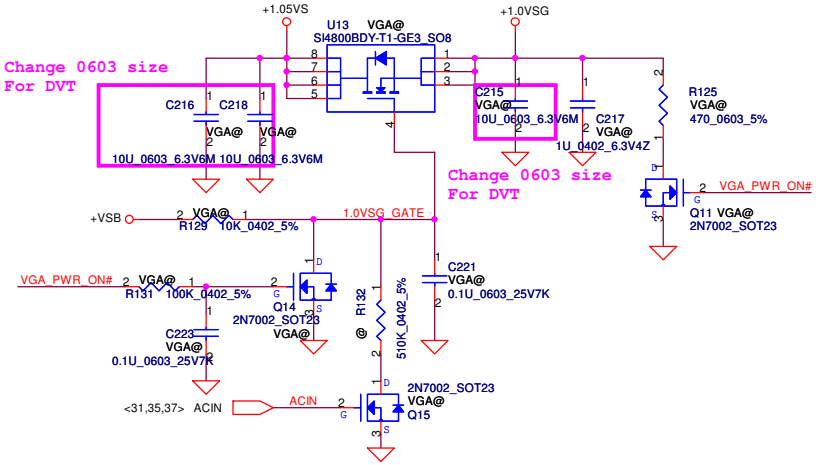
+3.3VS TO +3.3VSG



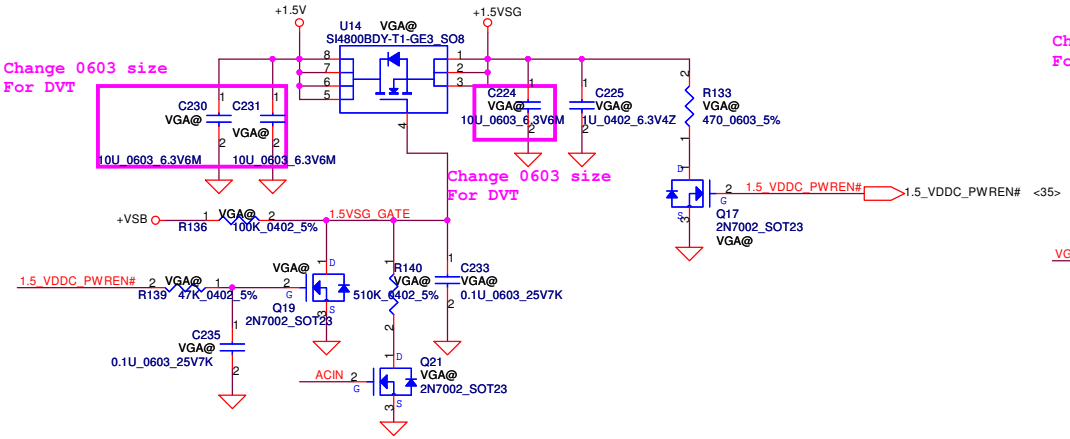
1.05VS TO +1.0VSG

Change P/N SB548000210



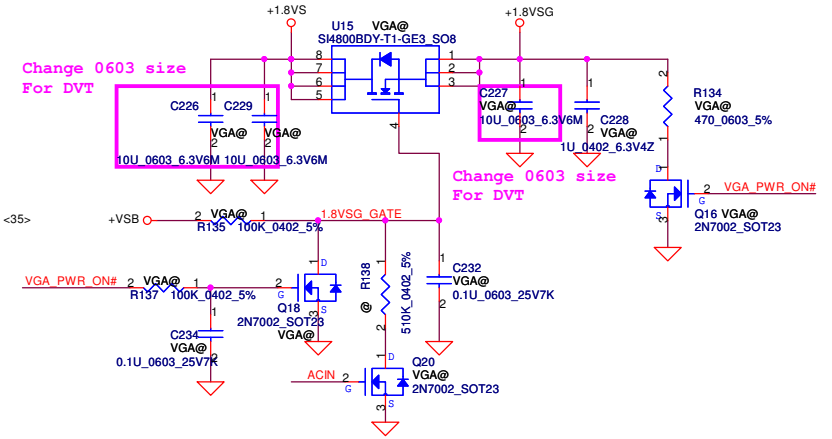
+1.5V TO +1.5VSG

Change P/N SB548000210



+1.8VS TO +1.8VSG

Change P/N SB548000210



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Compal Electronics, Inc.

Title: VGA DC Interface

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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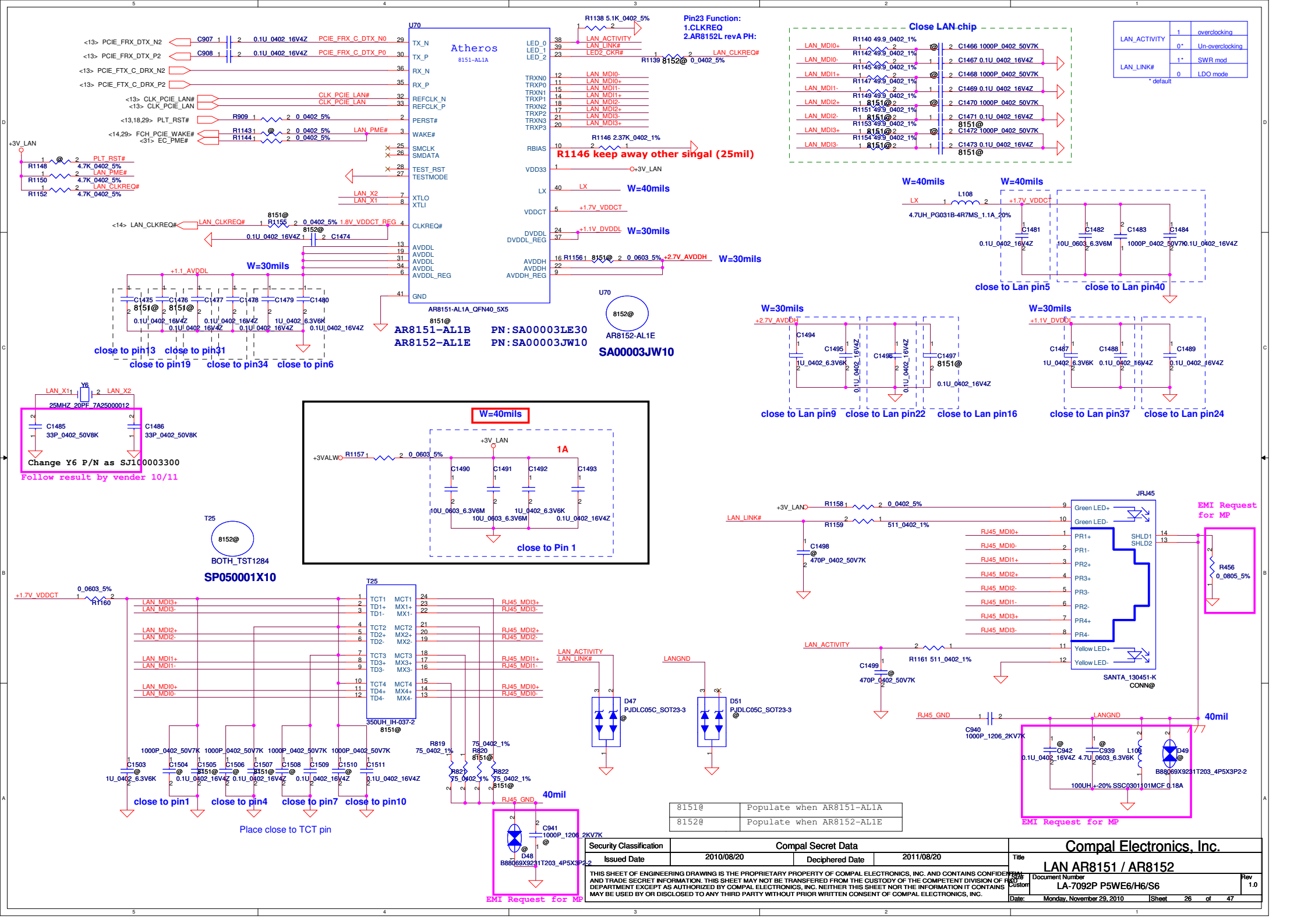

LAN_ACTIVITY	1	overclocking
	0 *	Un-overclocking
LAN_LINK#	1 *	SWR mod
	0	LDO mode

* default

8151@	Populate when AR8151-AL1A
8152@	Populate when AR8152-AL1E

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Compal Electronics, Inc.

Title: LAN AR8151 / AR8152

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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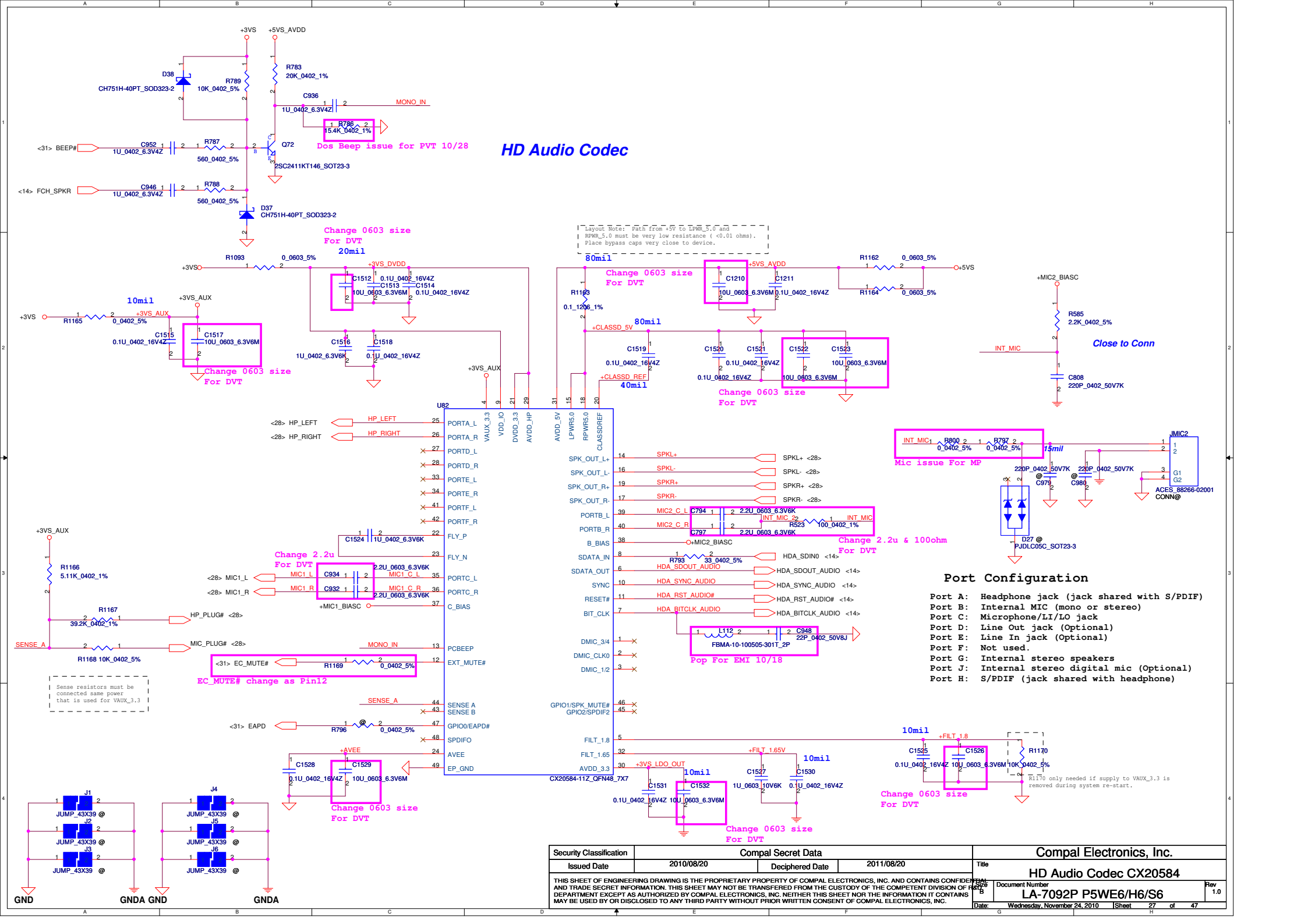
HD Audio Codec



Port Configuration

```
Port A:  Headphone jack (jack shared with S/PDIF)
Port B:  Internal MIC (mono or stereo)
Port C:  Microphone/LI/LO jack
Port D:  Line Out jack (Optional)
Port E:  Line In jack (Optional)
Port F:  Not used.
Port G:  Internal stereo speakers
Port J:  Internal stereo digital mic (Optional)
Port H:  S/PDIF (jack shared with headphone)
```

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Compal Electronics, Inc.

Title: HD Audio Codec CX20584

Size: B | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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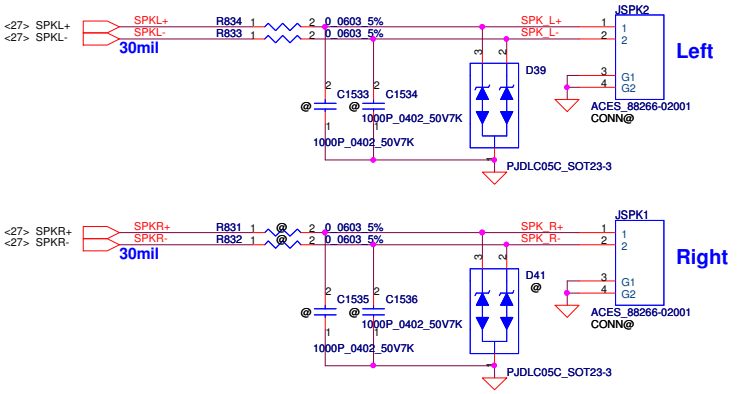
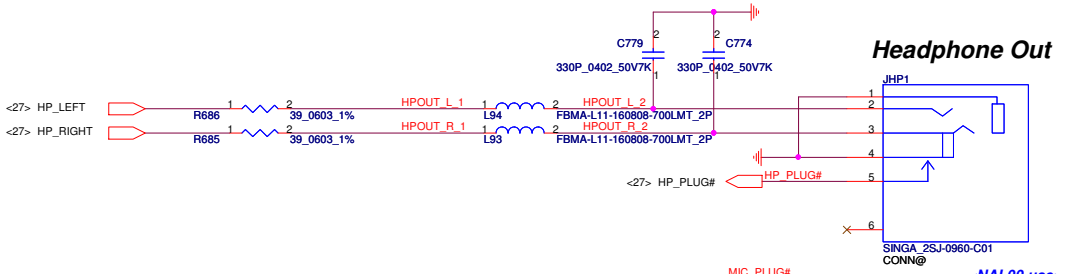
Int. Speaker Conn.



Headphone Out



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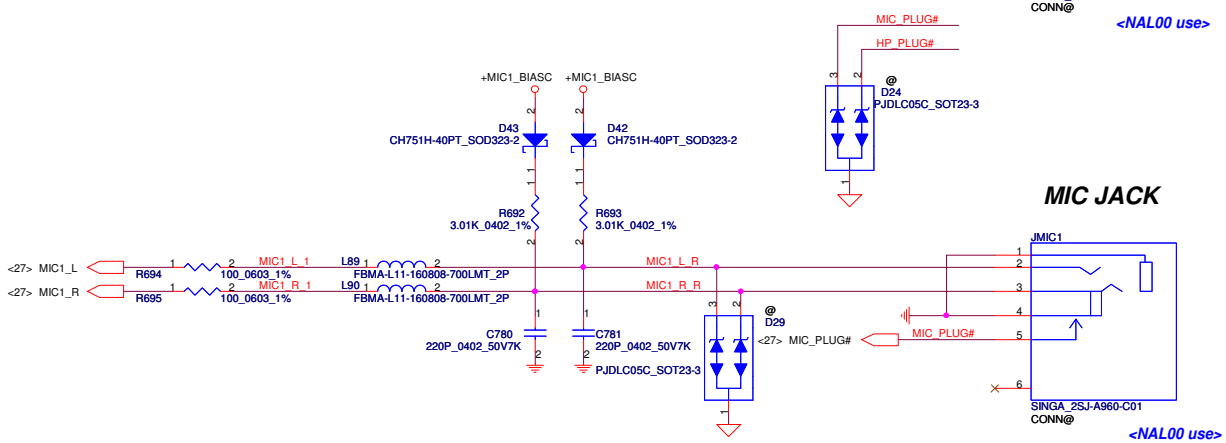
MIC JACK



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Compal Electronics, Inc.			
Title: Amplifier & Audio Jack			
Size: B	Document Number: LA-7092P P5WE6/H6/S6		Rev: 1.0
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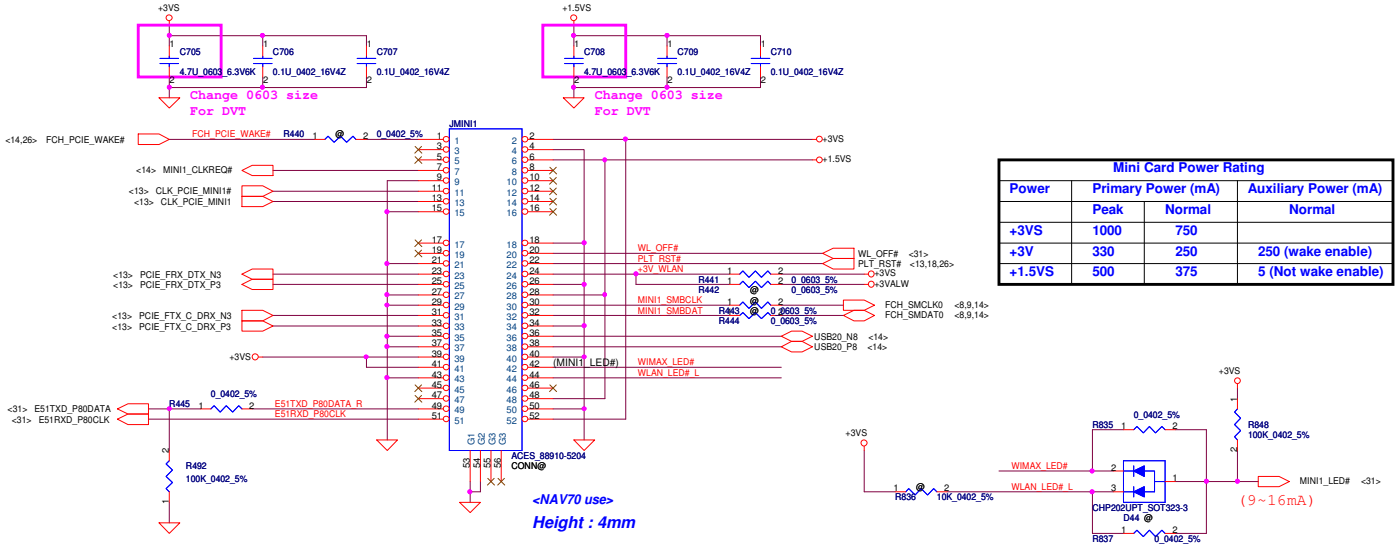
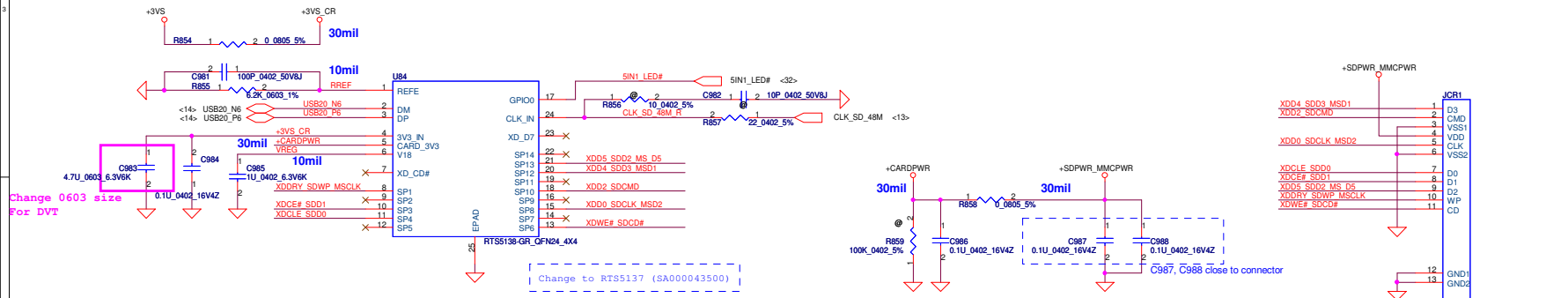
Mini-Express Card for WLAN



Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

Card Reader RTS5138 / RTS5137
(only SD+MMC function)

Card Reader Connector



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Compal Electronics, Inc.

Title: MINI CARD / CardReader RTS5137

Size | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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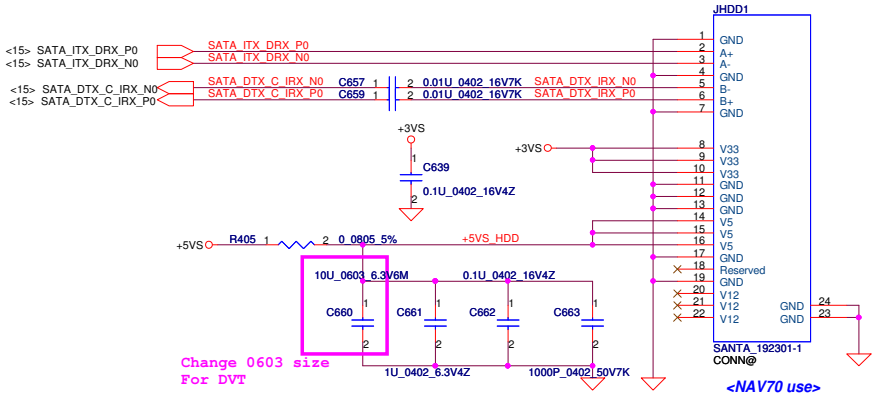
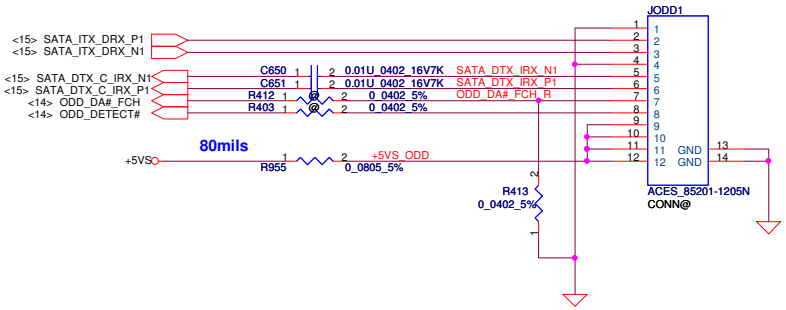
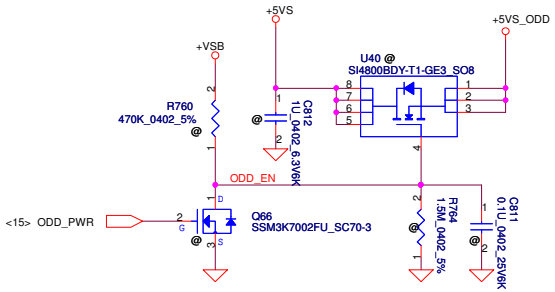
SATA HDD Conn.



SATA ODD FFC Conn.





Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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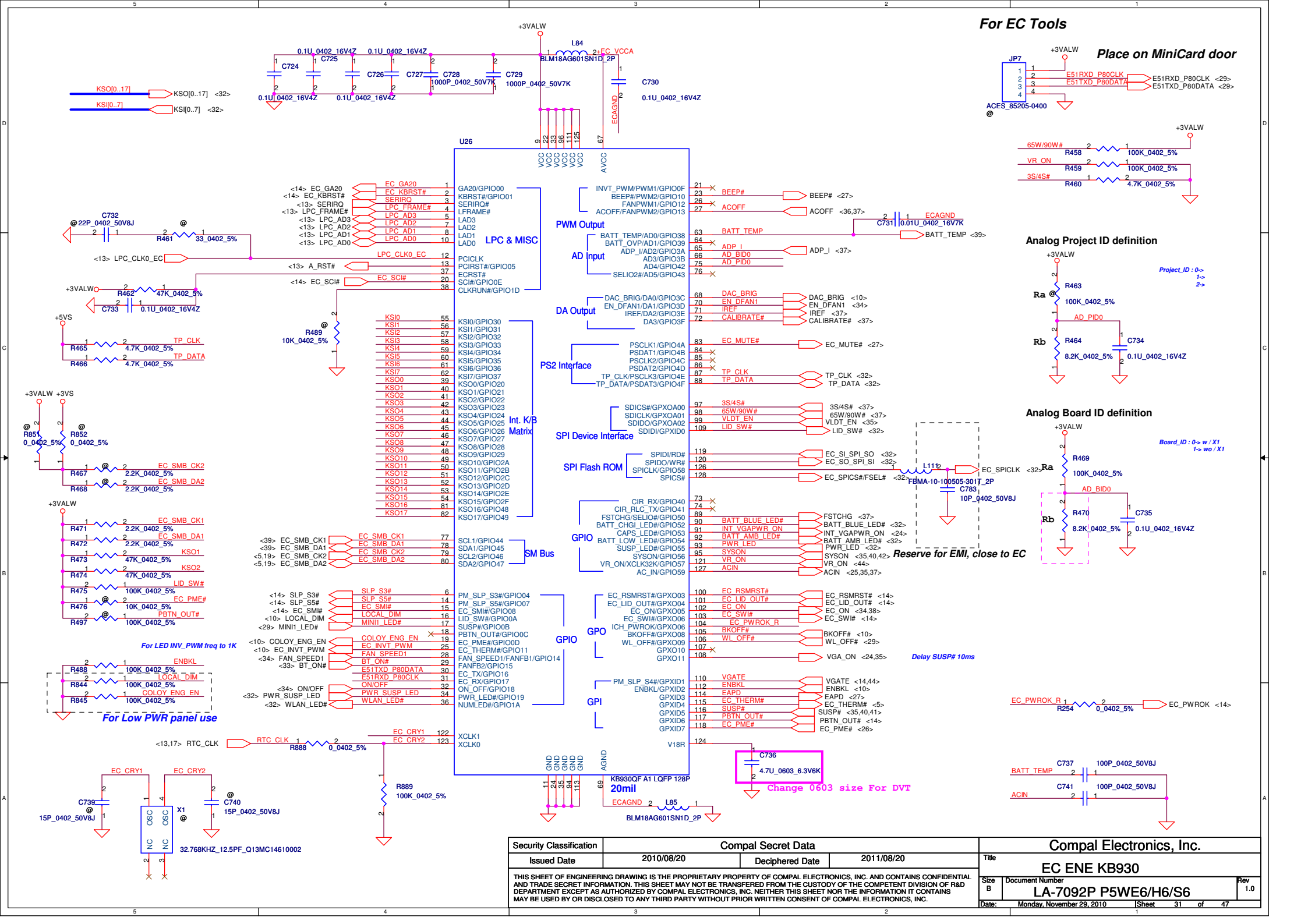
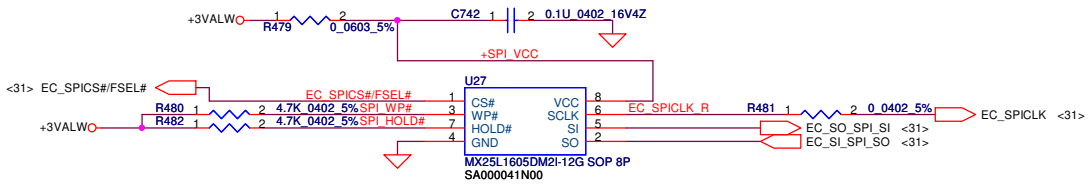
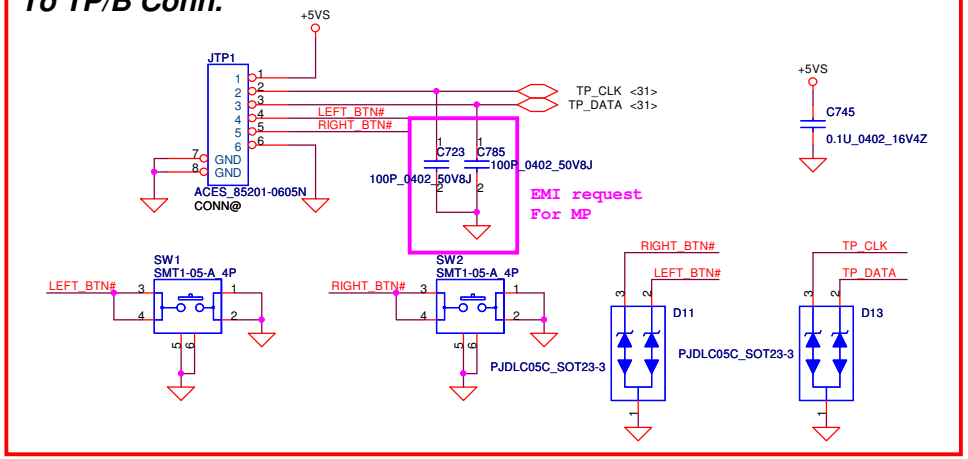
Compal Electronics, Inc.		
Title: HDD & ODD CONN		
Size: B	Document Number: LA-7092P P5WE6/H6/S6	Rev: 1.0
Date: Wednesday, November 24, 2010	Sheet 30 of 47	

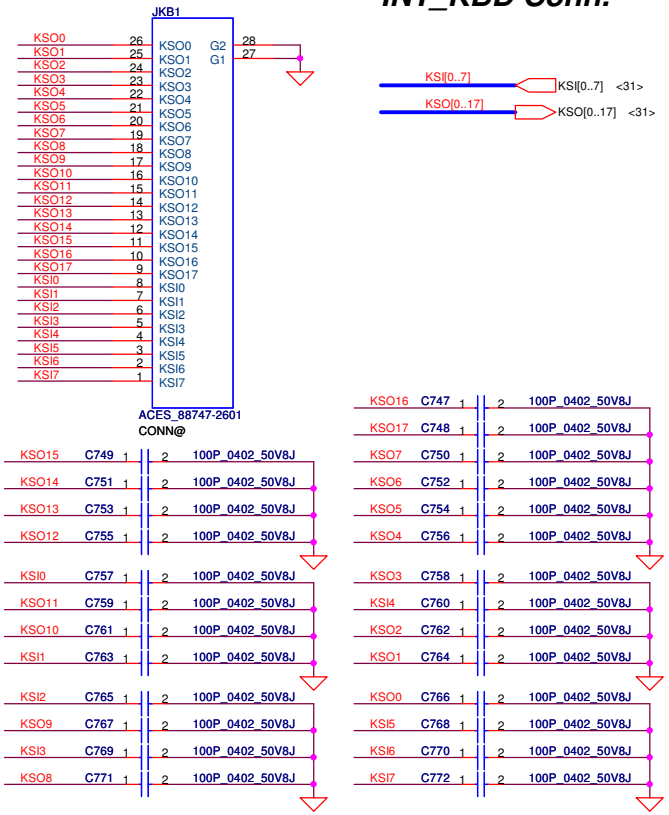

For EC Tools
Place on MiniCard door
U26
KB930QF A1 LQFP 128P
20mil
LPC & MISC
PWM Output
AD Input
DA Output
PS2 Interface
SPI Device Interface
SPI Flash ROM
Int. K/B Matrix
SM Bus
GPIO
GPO
GPI
Analog Project ID definition
Analog Board ID definition
Reserve for EMI, close to EC
For LED INV_PWM freq to 1K
For Low PWR panel use
Delay SUSP# 10ms
Change 0603 size For DVT
32.768KHZ_12.5PF_Q13MC14610002
Security Classification
Compal Secret Data
Issued Date
2010/08/20
Deciphered Date
2011/08/20
Compal Electronics, Inc.
EC ENE KB930
LA-7092P P5WE6/H6/S6
Rev 1.0
Monday, November 29, 2010
Sheet 31 of 47

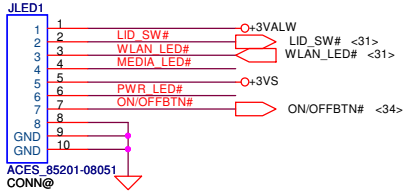


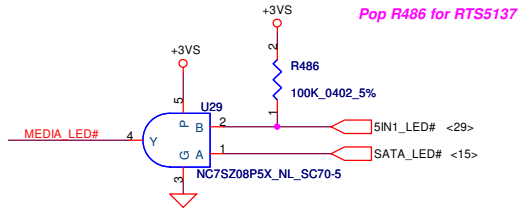
To TP/B Conn.

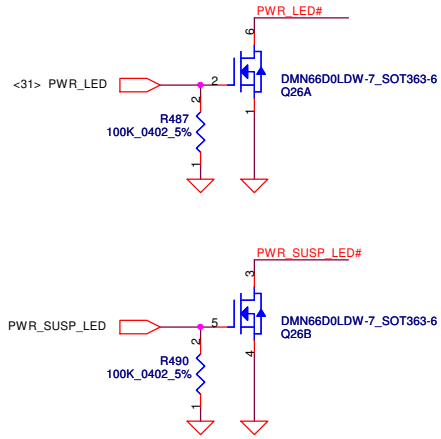


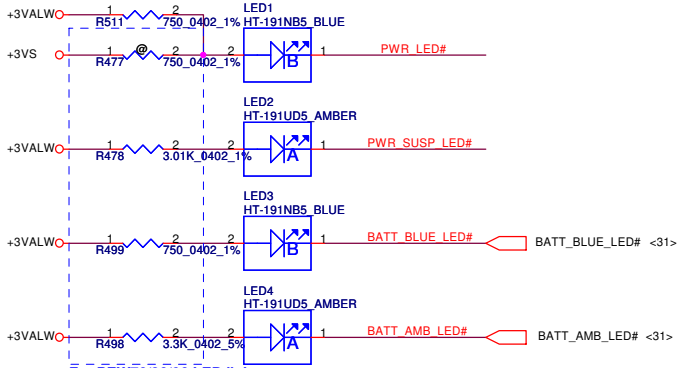
INT_KBD Conn.











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Issued Date	2010/08/20	Deciphered Date	2011/08/20

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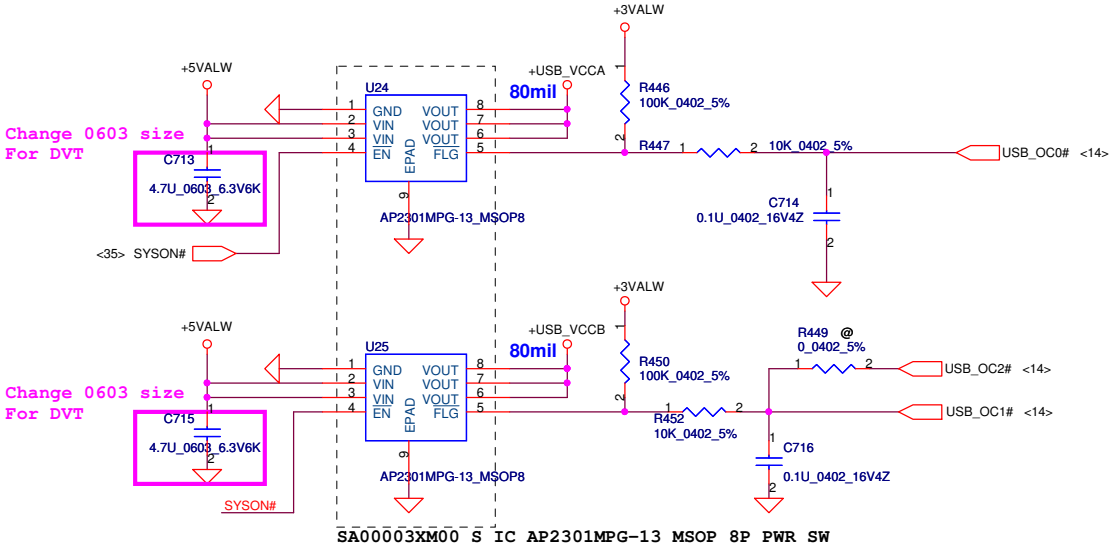
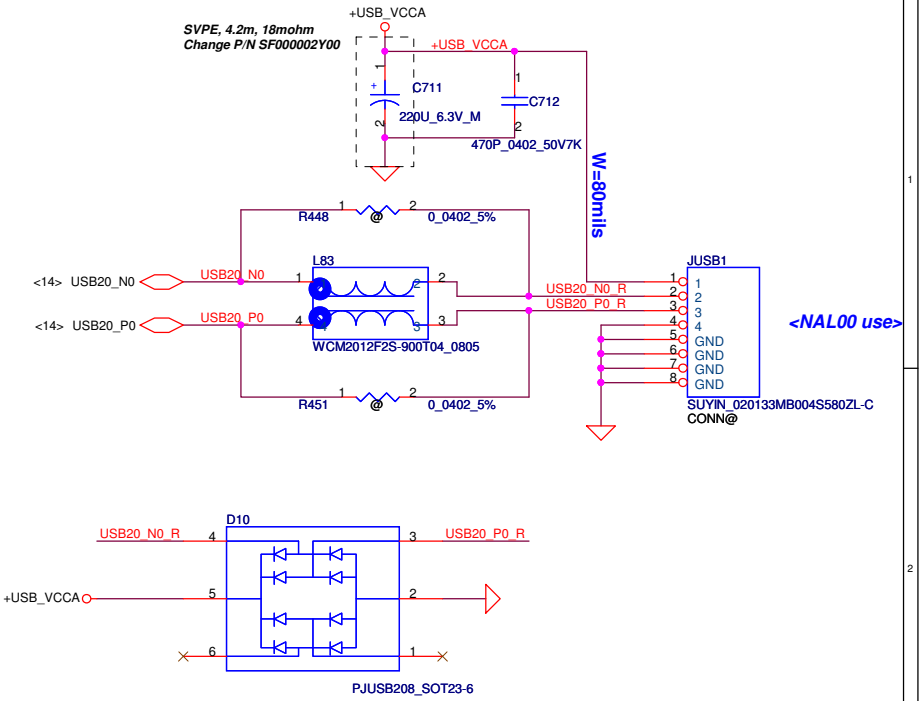
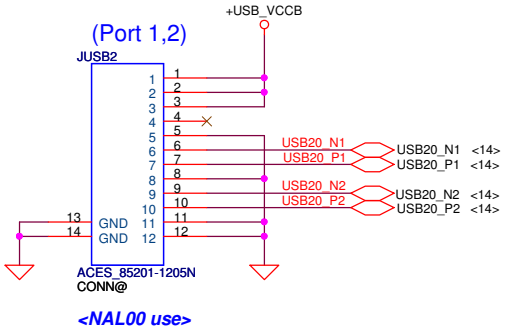
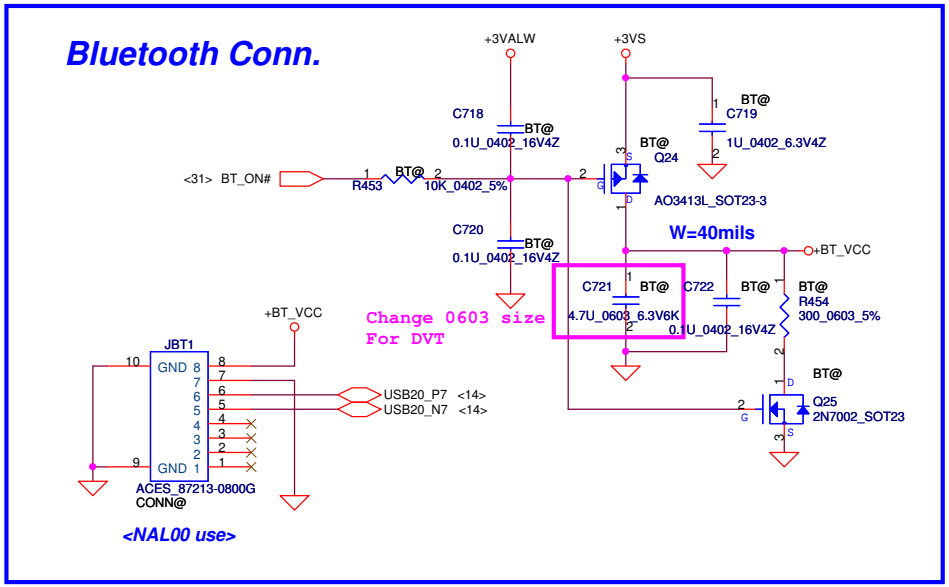
Compal Electronics, Inc.			
Title	KB/TP/LED/SPI ROM/PWRb		
Size: B	Document Number: LA-7092P P5WE6/H6/S6		Rev: 1.0
Date: Wednesday, November 24, 2010	Sheet 32 of 47		





To USB/B Connector





Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: USB/BT/USBsub

Size: Custom | Document Number: LA-7092P P5WE6/H6/S6 | Rev: 1.0

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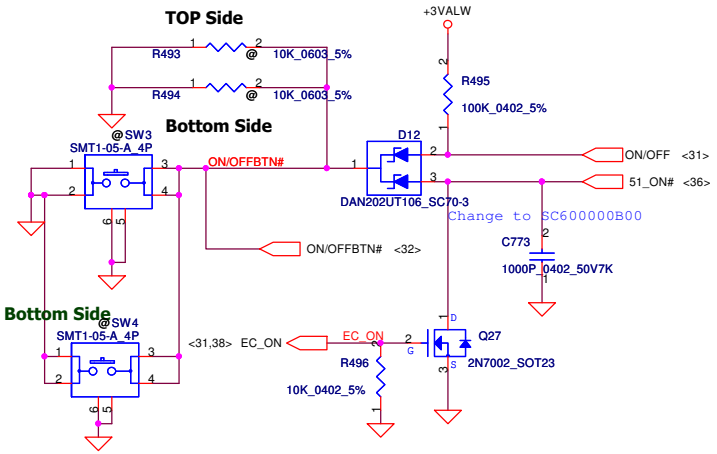
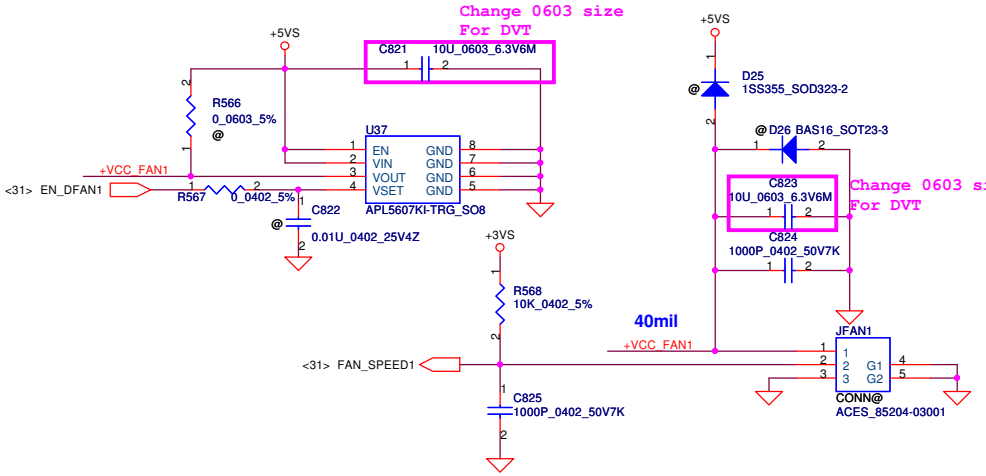
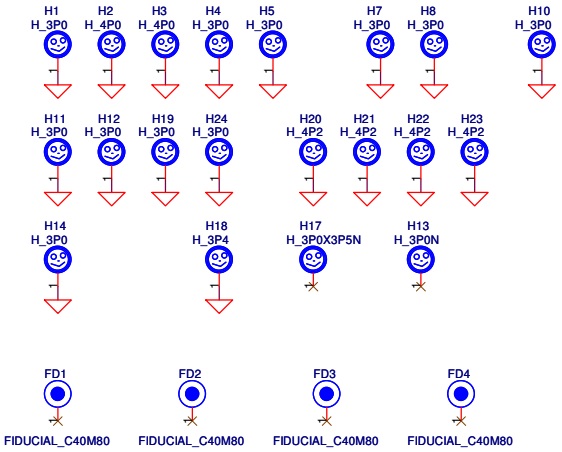
ON/OFF switch *Power Button*



FAN1 Conn





Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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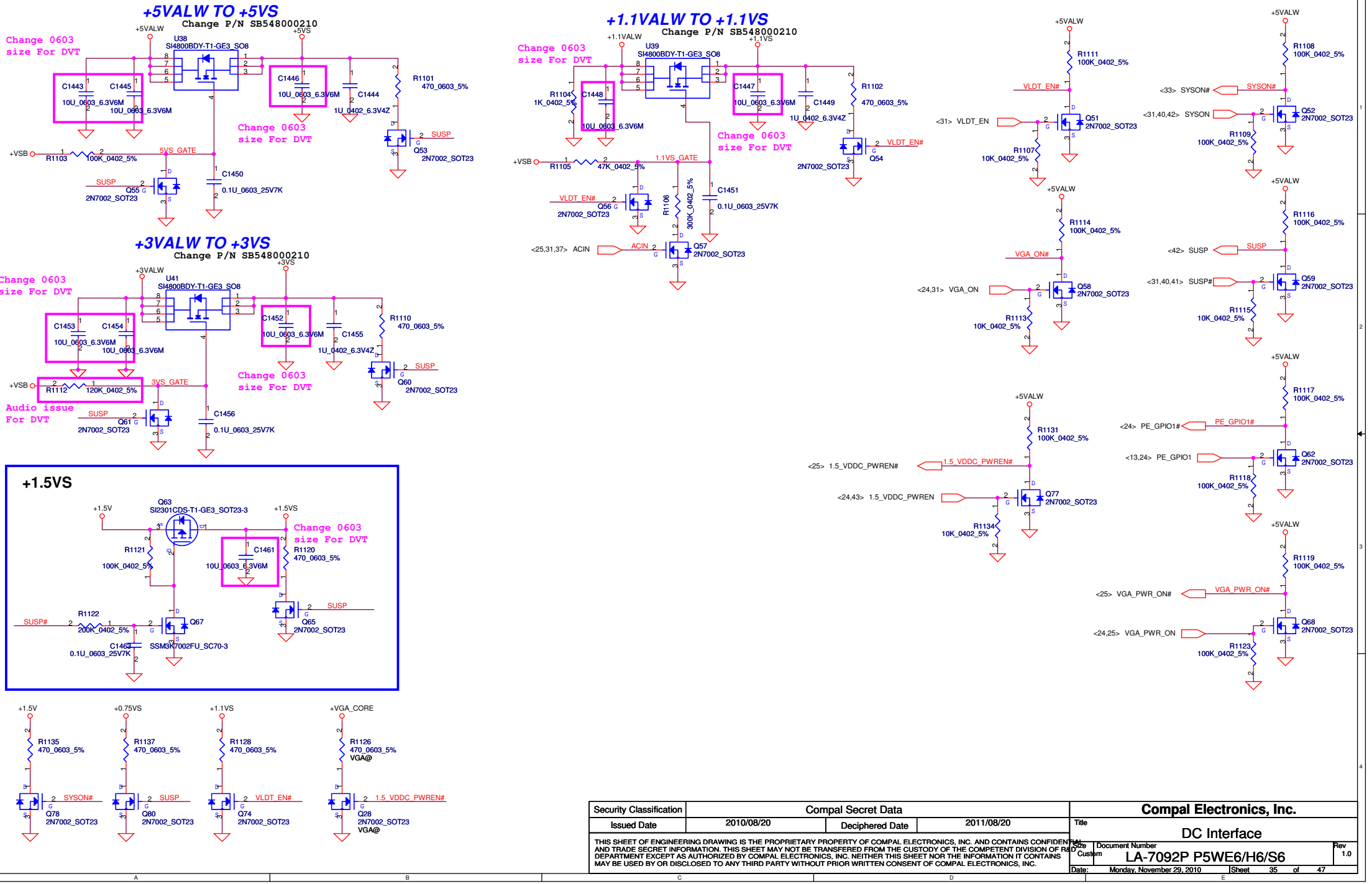
Compal Electronics, Inc.

Title: Other IO/USB (right)

Size	Document Number	Rev
Custom	LA-7092P P5WE6/H6/S6	1.0

Date: Wednesday, November 24, 2010 | Sheet 34 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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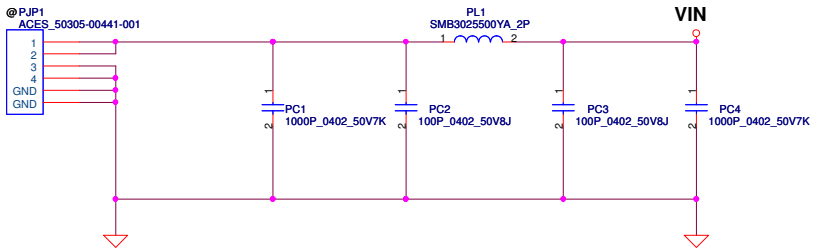
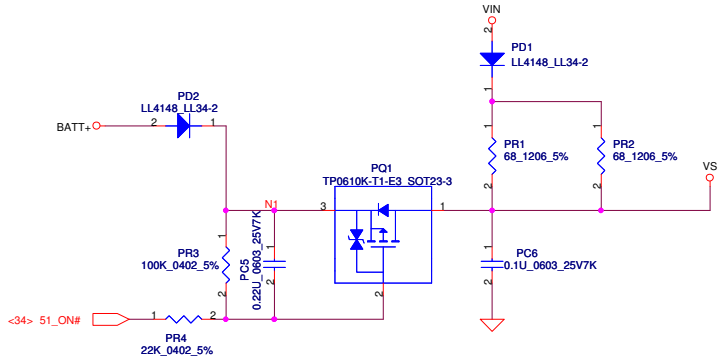
Compal Electronics, Inc.

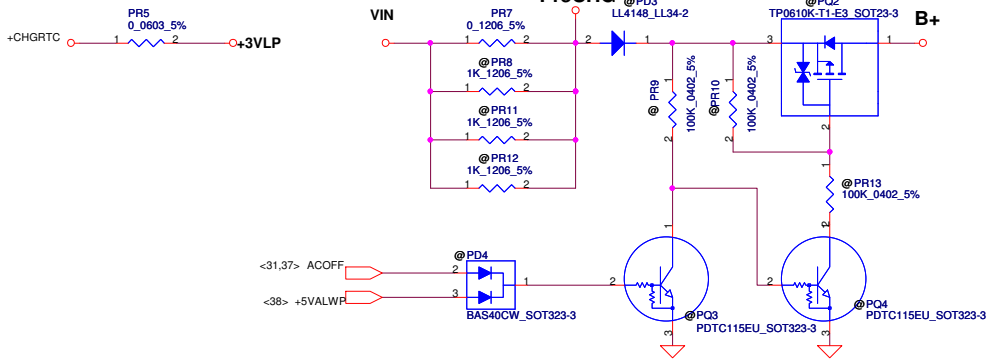
Title: DC Interface

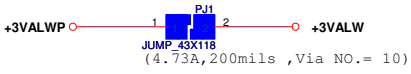
Size	Document Number	Rev
Custom	LA-7092P P5WE6/H6/S6	1.0

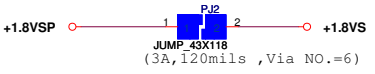
Date: Monday, November 29, 2010 | Sheet 35 of 47

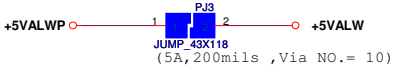


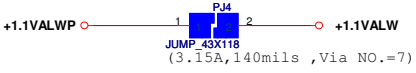


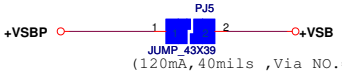


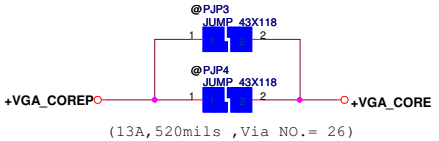


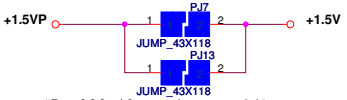


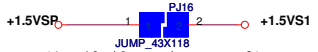












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Issued Date	2010/07/13	Deciphered Date	2011/07/13

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Compal Electronics, Inc.

Title: PWR DCIN / Pre-charge

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

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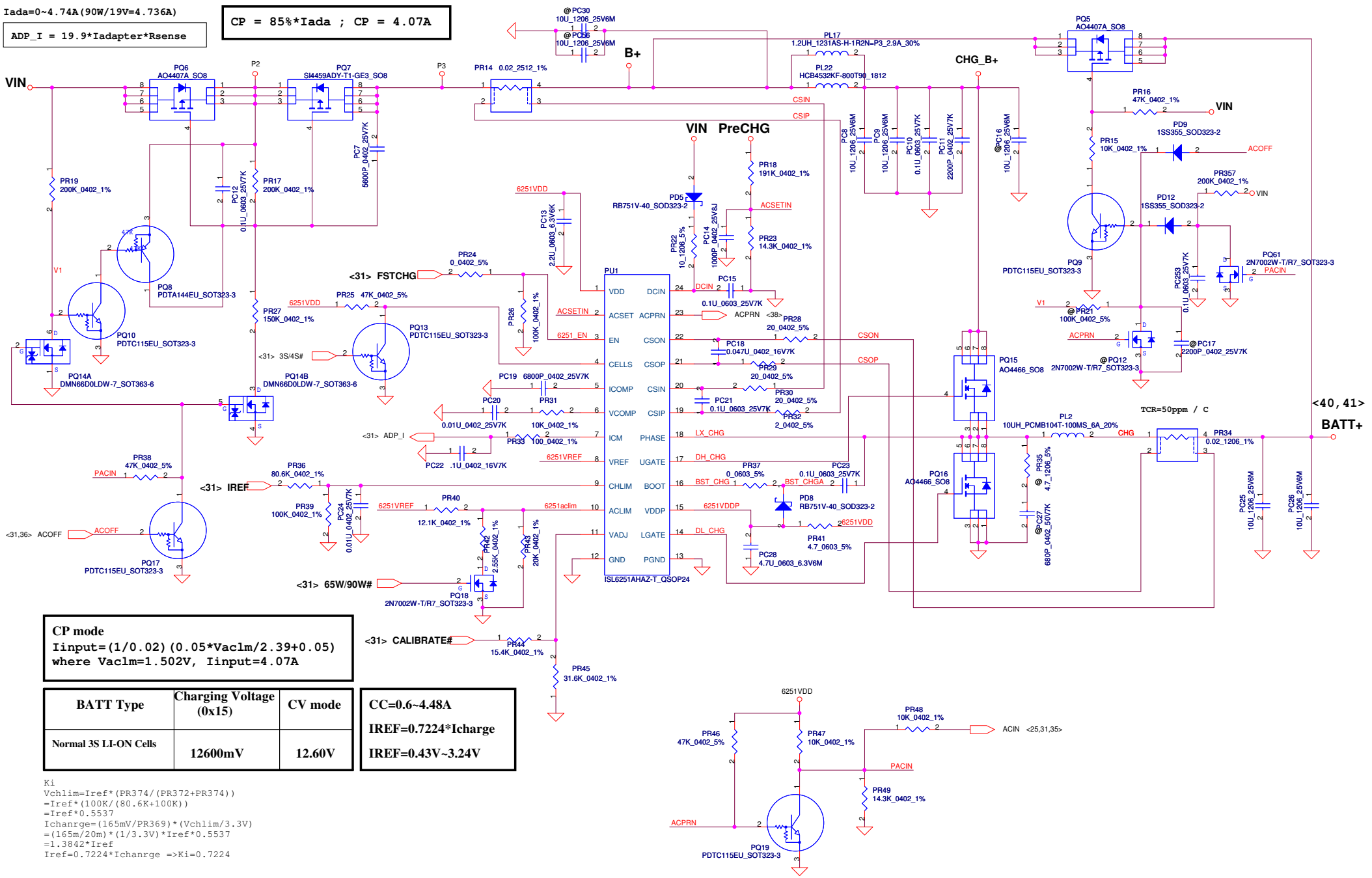
Iada=0~4.74A(90W/19V=4.736A)

ADP_I = 19.9*Iadapter*Rsense

CP = 85%*Iada ; CP = 4.07A



CP mode

Iinput=(1/0.02)(0.05*Vaclm/2.39+0.05)

where Vaclm=1.502V, Iinput=4.07A

BATT Type	Charging Voltage (0x15)	CV mode
Normal 3S LI-ON Cells	12600mV	12.60V

CC=0.6~4.48A

IREF=0.7224*Icharge

IREF=0.43V~3.24V

Ki

Vchlim=Iref*(PR374/(PR372+PR374))

=Iref*(100K/(80.6K+100K))

=Iref*0.5537

Ichanrge=(165mV/PR369)*(Vchlim/3.3V)

=(165m/20m)*(1/3.3V)*Iref*0.5537

=1.3842*Iref

Iref=0.7224*Ichanrge =>Ki=0.7224

Kv

Rinternal ic=514K Rec=3K R1=PR379=15.4K R2=PR381=31.6K

R=514K//31.6K//(15.4K+3k)=11.372K

r=514K//514K//31.6K=28.14K

Vcell=0.175*Vadj+3.99v

4.2V=0.175*Vadj+3.99V =>Vadj=1.2V

Vadj=Vref*(R/(R+514K))+CALIBRATE*(r/(r=514K))

1.1483=CALIBRATE*0.6046 =>CALIBRATE=1.899

1.899=(4.2-(Vcell+A*0.175))*Kv=(4.2-(4.2+A*0.175))*Kv

A=Vref*(R/(R+514K))=0.052

Kv=9.451

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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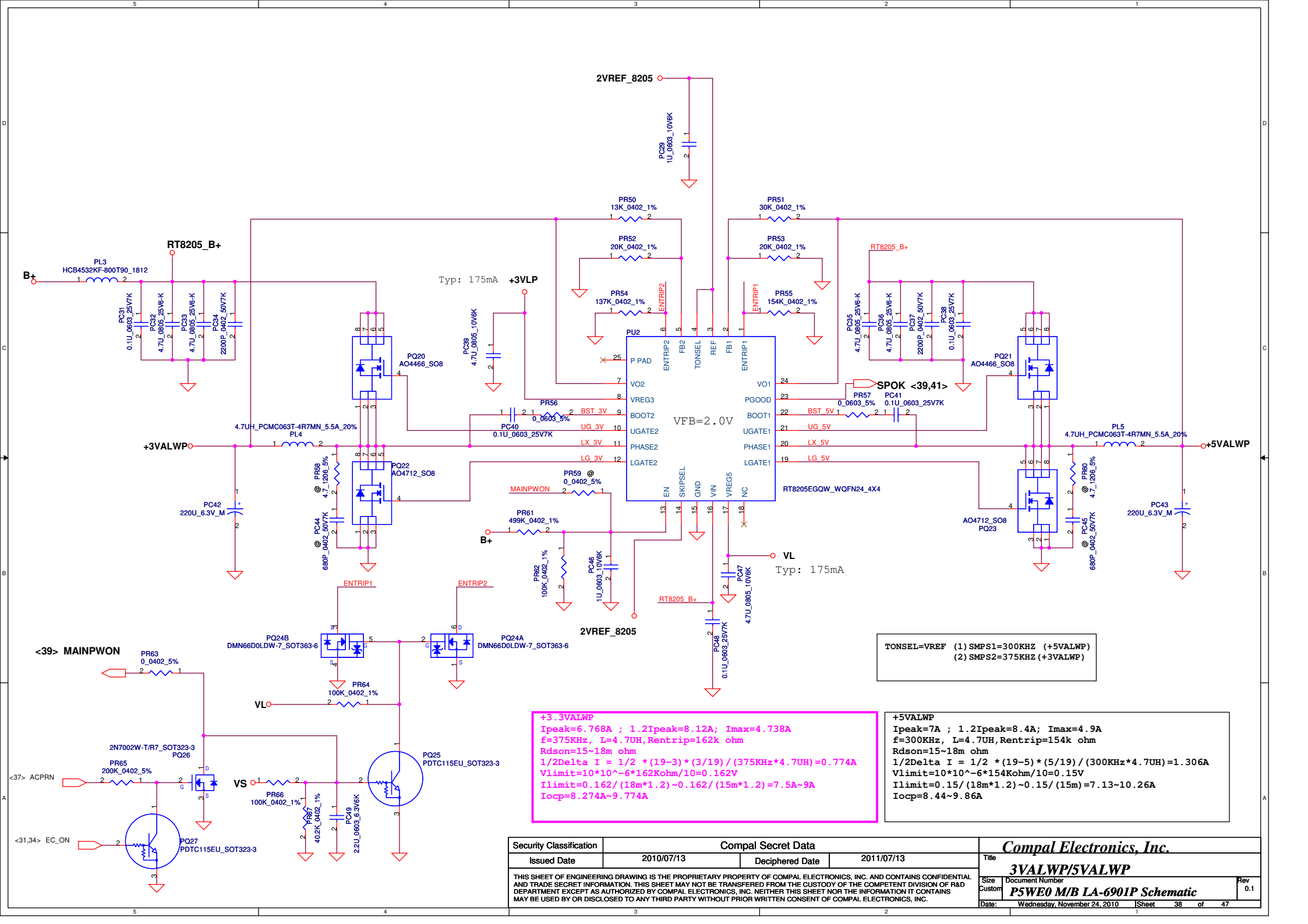
Compal Electronics, Inc.

Title: PWR-CHARGER

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Wednesday, November 24, 2010 | Sheet 37 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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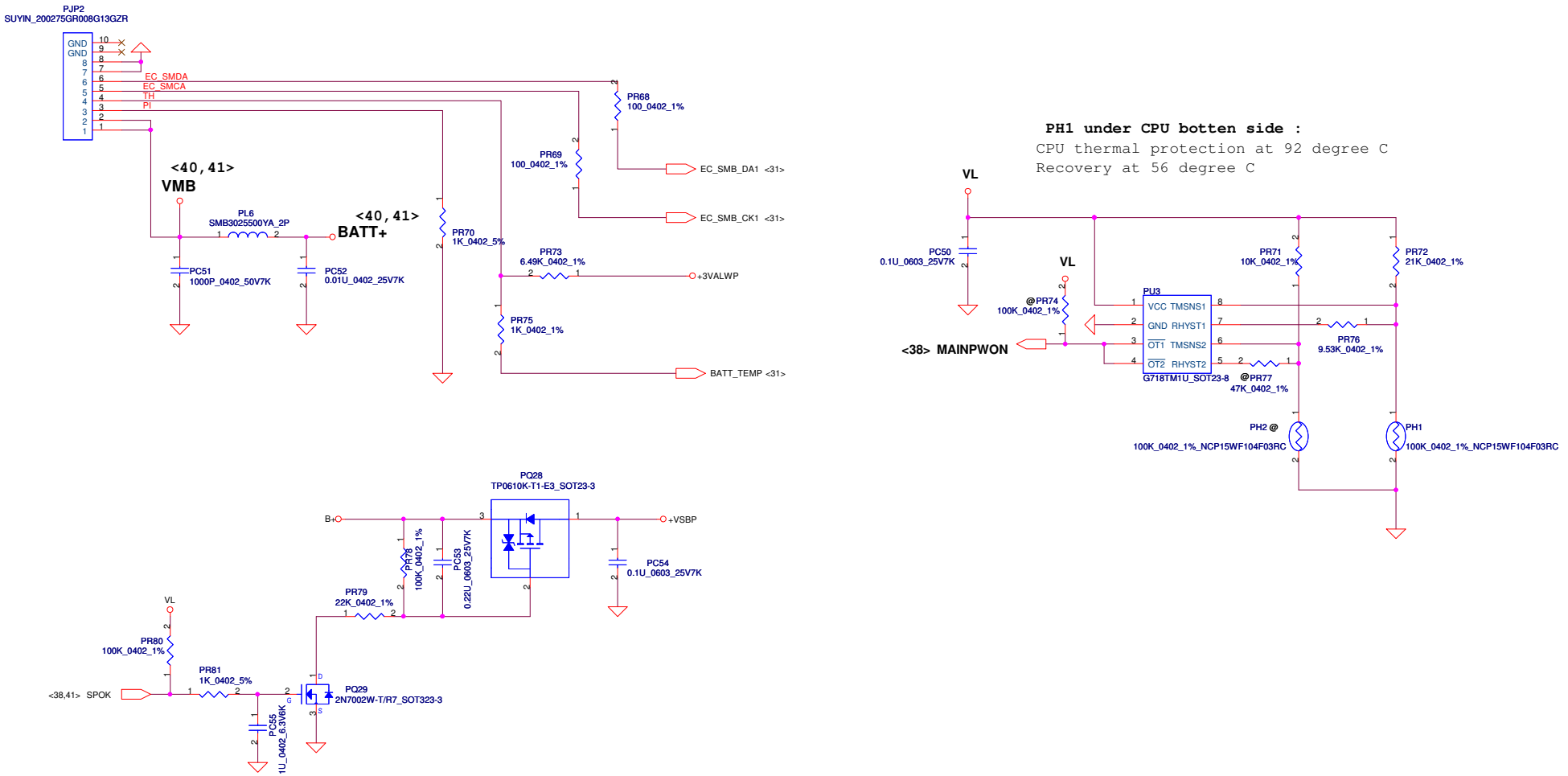
Compal Electronics, Inc.

Title: 3VALWP/5VALWP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Wednesday, November 24, 2010 | Sheet 38 of 47



Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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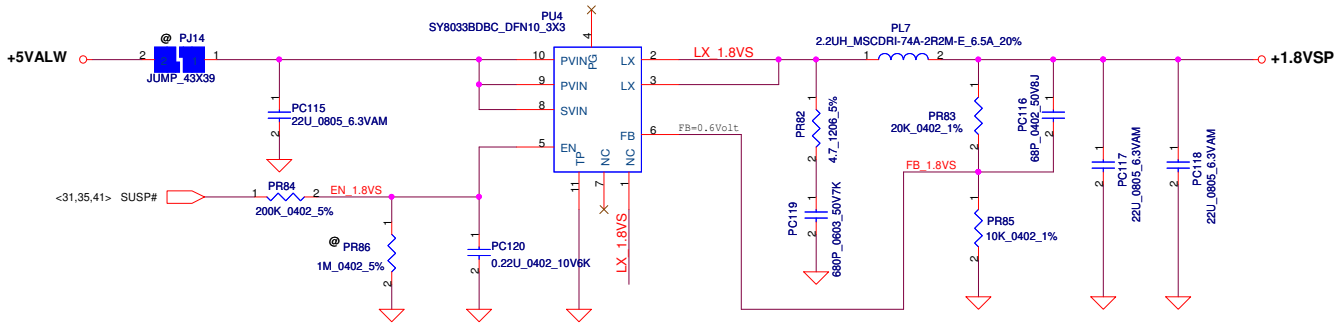
Compal Electronics, Inc.

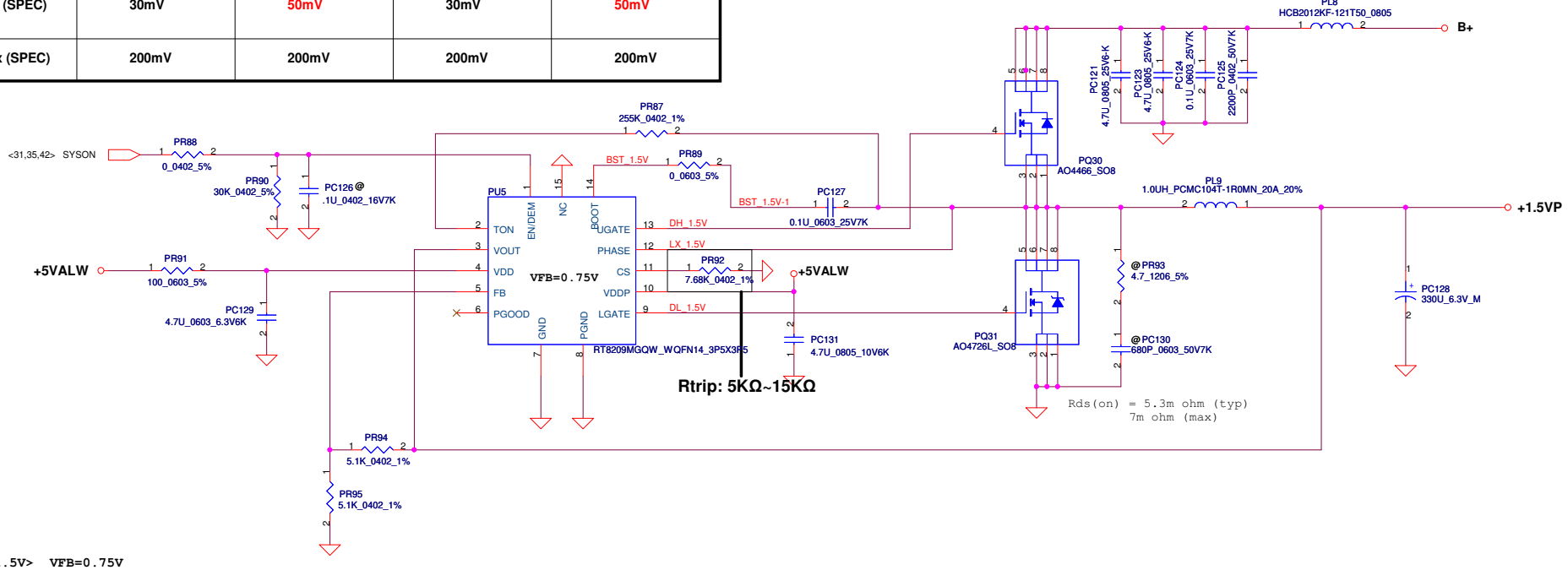
Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: P5WE0 M/B LA-6901P Schematic | Rev: 0.1

Date: Wednesday, November 24, 2010 | Sheet 39 of 47



	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV



<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=280KHz

Cout ESR=17 mohm Rdson(max)=7 mohm Rdson(typ)=5.3 mohm
Ipeak=9.45A, Imax=6.615A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.93A
=>1/2Delta I=2.467A
Vtrip=Rtrip*10uA=0.0768
Iocpmin=Vtrip/(Rds(on)(max)*1.2)+Delta I/2=11.61A
Iocpmax=Vtrip/(Rds(on)(typ)*1.2)+Delta I/2=14.54A
Iocp=11.61A~14.54A

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

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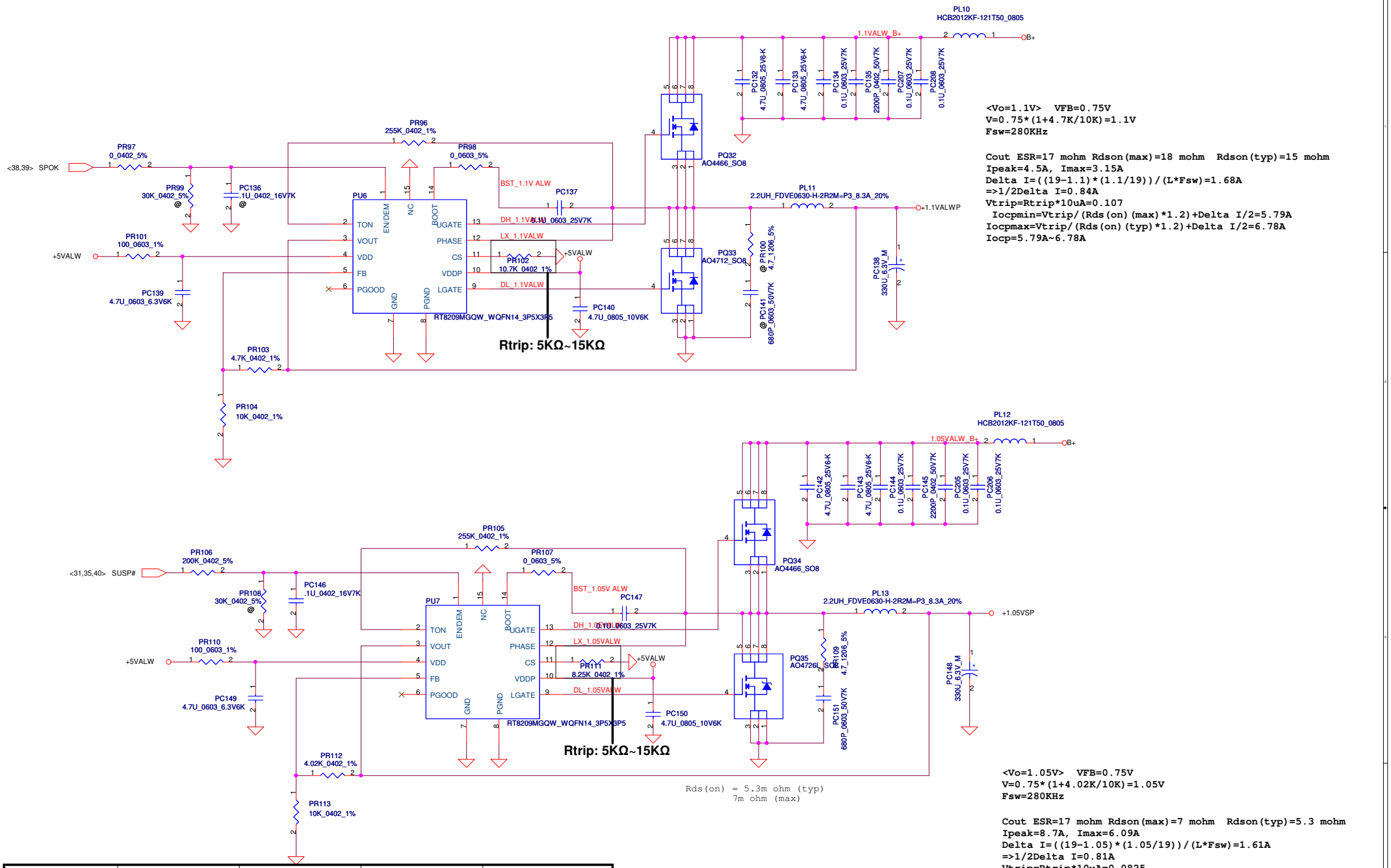
Compal Electronics, Inc.

Title: 1.8VSP/1.5VP

Size: Custom | Document Number | Rev: 0.1

Date: Wednesday, November 24, 2010 | Sheet 40 of 47



	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

Security Classification	Compal Secret Data		
Issued Date	2010/01/25	Deciphered Date	2009/04/28

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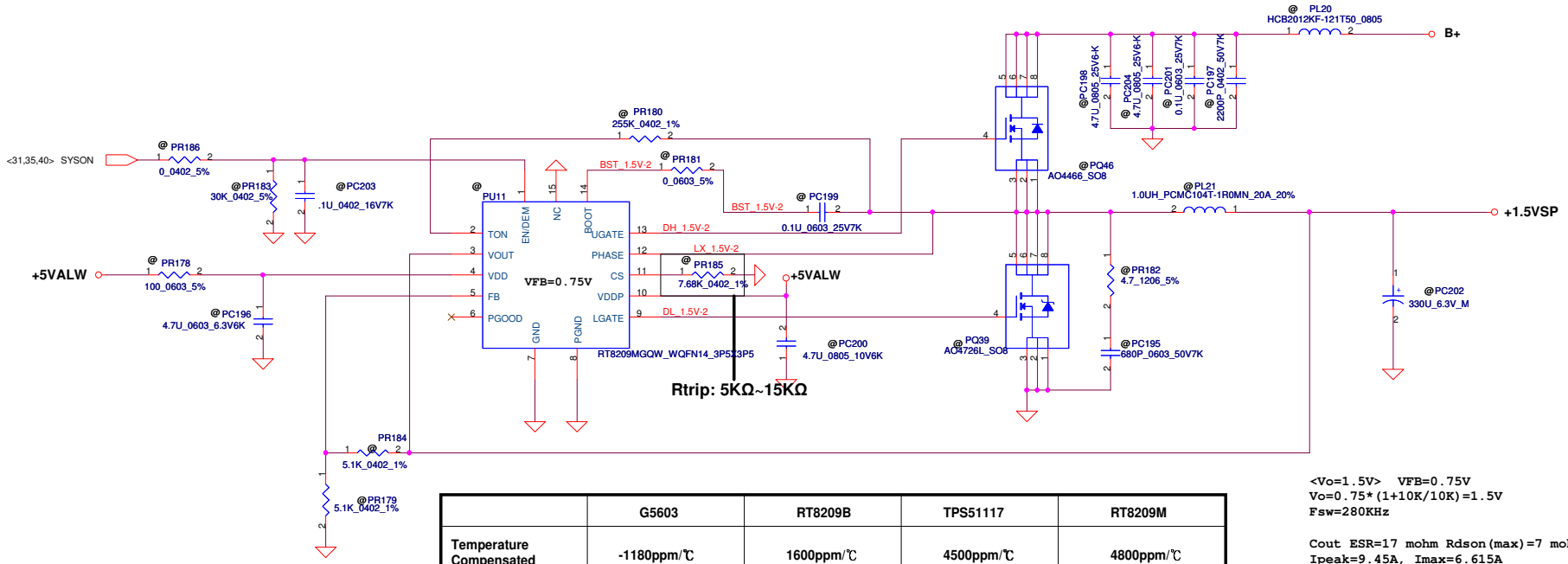
Compal Electronics, Inc.

Title: 1.1VALWP/1.05VSP

Size: Custom | Document Number | Rev: 0.1

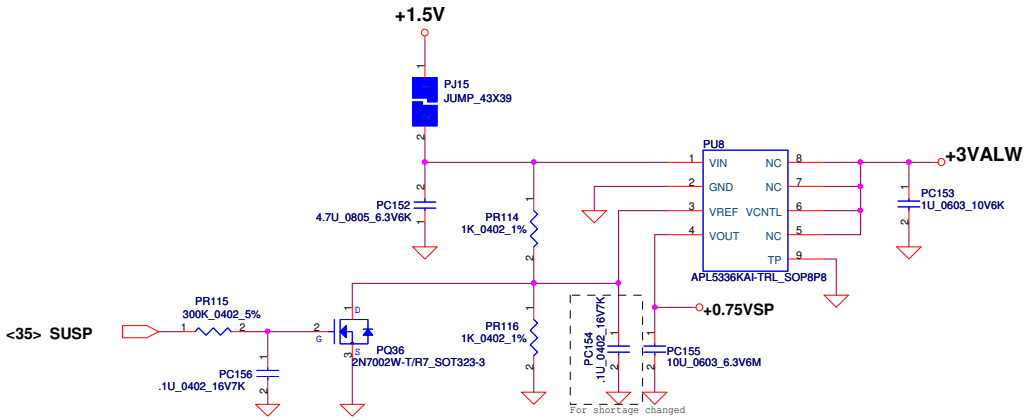
Date: Wednesday, November 24, 2010 | Sheet 41 of 47



	G5603	RT8209B	TPS51117	RT8209M
Temperature Compensated	-1180ppm/℃	1600ppm/℃	4500ppm/℃	4800ppm/℃
Vtrip_min (SPEC)	30mV	50mV	30mV	50mV
Vtrip_max (SPEC)	200mV	200mV	200mV	200mV

<Vo=1.5V> VFB=0.75V
Vo=0.75*(1+10K/10K)=1.5V
Fsw=280KHz

Cout ESR=17 mohm Rdson(max)=7 mohm Rdson(typ)=5.3 mohm
Ipeak=9.45A, Imax=6.615A
Delta I=((19-1.5)*(1.5/19))/(L*Fsw)=4.93A
=>1/2Delta I=2.467A
Vtrip=Rtrip*10uA=0.0768
 Iocpmin=Vtrip/(Rds(on)(max)*1.2)+Delta I/2=11.61A
Iocpmax=Vtrip/(Rds(on)(typ)*1.2)+Delta I/2=14.54A
Iocp=11.61A~14.54A



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

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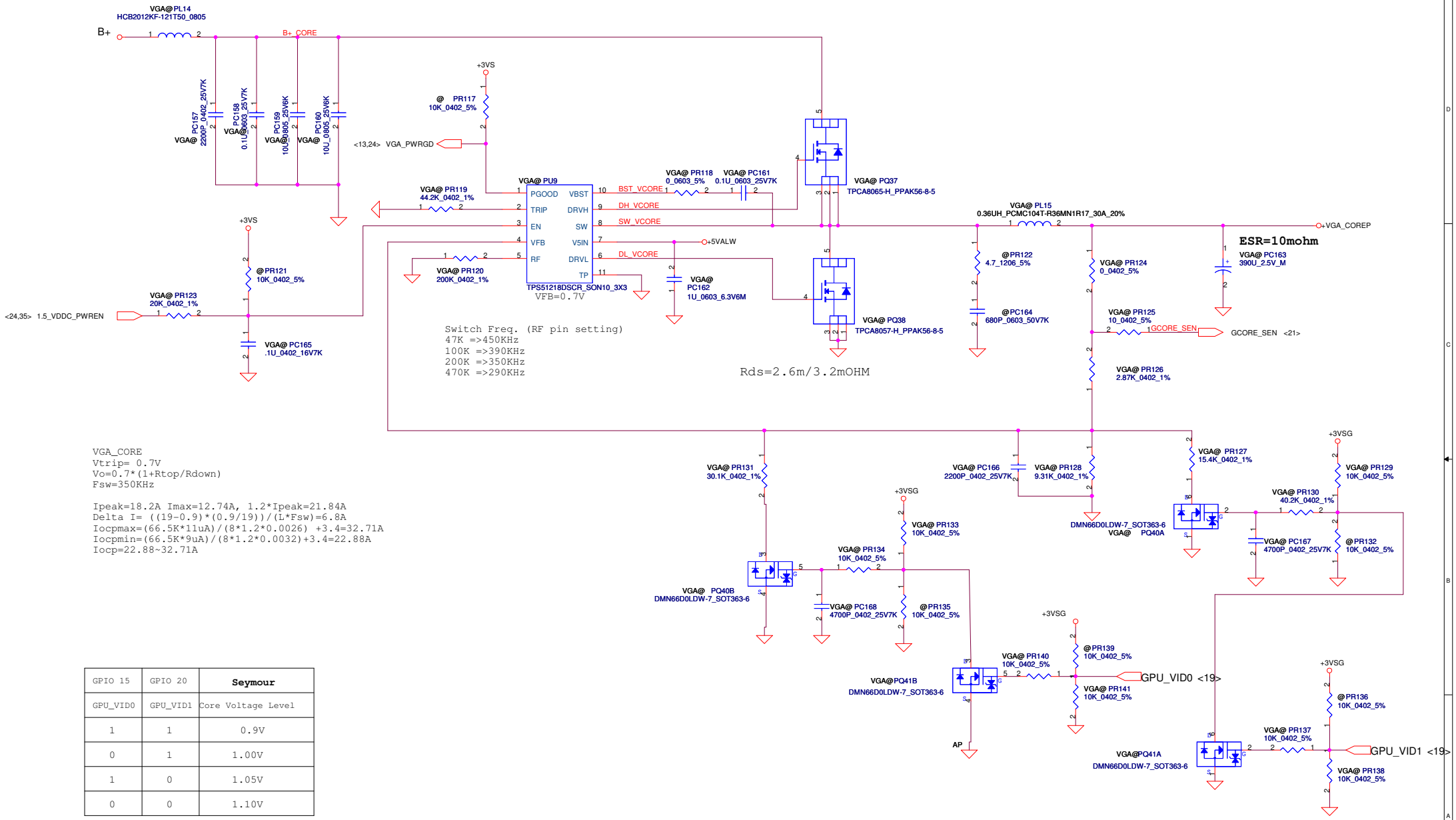
Compal Electronics, Inc.

Title: 0.75VSP

Size: B | Document Number | Rev: 0.3

Date: Wednesday, November 24, 2010 | Sheet 42 of 47



GPIO 15	GPIO 20	Seymour
GPU_VID0	GPU_VID1	Core Voltage Level
1	1	0.9V
0	1	1.00V
1	0	1.05V
0	0	1.10V

Security Classification	Compal Secret Data		
Issued Date	2010/07/13	Deciphered Date	2011/07/13

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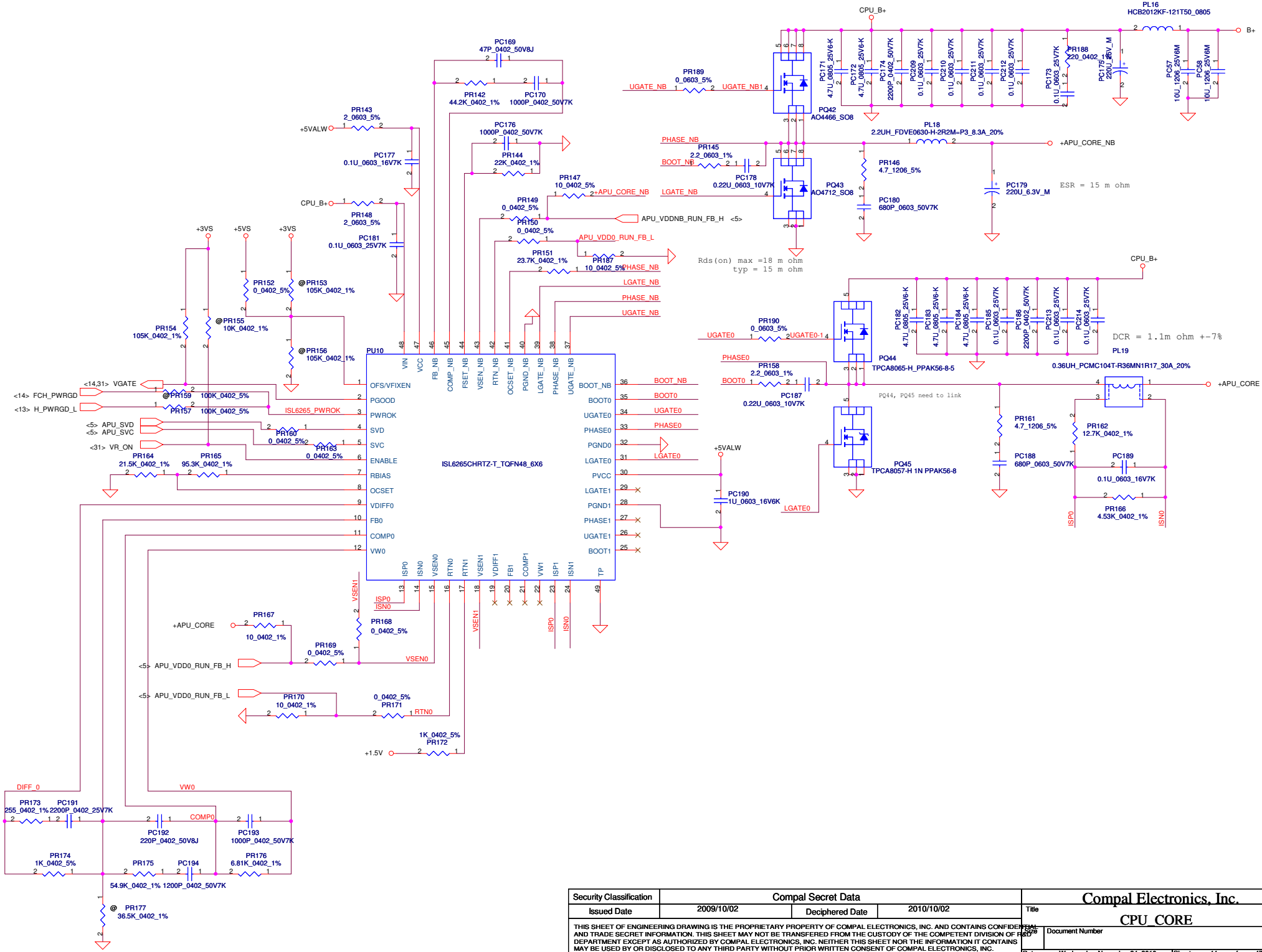
Compal Electronics, Inc.			
Title	+VGA_COREP		
Size Custom	Document Number P5WE6/S6/H6		Rev 0.1
Date: Wednesday, November 24, 2010	Sheet 43 of 47		



Security Classification	Compal Secret Data		
Issued Date	2009/10/02	Deciphered Date	2010/10/02

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Compal Electronics, Inc.

Title: CPU_CORE

Size: D | Document Number | Rev: 0.3

Date: Wednesday, November 24, 2010 | Sheet 44 of 47

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	0.75VSP EN RC value	HW adjust timing	0.1	42	Change PR115 from SD028000080 to SD028300380(S RES 1/16W 300K +-5% 0402) Add PC156 SE076104K80(S CER CAP .1U 16V K X7R 0402)	2010/09/24	DVT
2	1.8VSP EN RC value	HW adjust timing	0.1	40	Change PR84 from SD028000080 to SD028200380(S RES 1/16W 200K +-5% 0402) Add PC120 SE095224K00(S CER CAP 0.22U 10V K X5R 0402)	2010/09/24	DVT
3	1.05VSP EN RC value	HW adjust timing	0.1	41	Change PR106 from SD028000080 to SD028200380(S RES 1/16W 200K +-5% 0402) Add PC146 SE076104K80(S CER CAP .1U 16V K X7R 0402)	2010/09/24	DVT
4	VGA_COREP EN RC value	HW adjust timing	0.1	43	Change PR123 from SD034100280 to SD034200280(S RES 1/16W 20K +-1% 0402)	2010/09/24	DVT
5	change BOM structure	1.5VSP change BOM structure to VGA@ for cost down of UMA	0.1	42	Change PU11, PL21, PQ39, PQ46, PR178, PR179, PR180, PR181, PR184, PR185, PR186, PC196, PC197, PC198, PC199, PC200, PC201, PC202, PC204 BOM structure to VGA@ del PL20 SM01000C000(S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2010/10/05	DVT
6	Adjust APU_CORE_NB OCP	Adjust APU_CORE_NB OCP to 15A	0.1	44	Change PR151 from SD034110280 to SD034237280(S RES 1/16W 23.7K +-1% 0402)	2010/10/07	DVT
7	Add input choke in charger circuit.	Add input choke for EMI ISN test in charger circuit.	0.1	37	Change PL17 from SM010018710 to SH00000IY00(S COIL 1.2UH +-30% 1231AS-H-1R2N=P3 2.9A)	2010/10/18	DVT
8	Add snubber	Add snubber in APU_COREP and APU_CORE_NB circuit.	0.1	44	Add PR146, PR161 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC180, PC188 SE025681K80(S CER CAP 680P 50V K X7R 0603) Add PR188 SD034220080(S RES 1/16W 220 +-1% 0402)	2010/10/18	DVT
9	Add snubber and input Cup.	Add snubber and input Cup. in 1.05VSP circuit.	0.1	41	Add PR161 SD001470B80(S RES 1/4W 4.7 +-5% 1206) Add PC188 SE025681K80(S CER CAP 680P 50V K X7R 0603) Add PC205, PC206 SE042104K80(S CER CAP .1U 25V K X7R 0603)	2010/10/18	DVT
10	Add input Cup.	Add input Cup. in 1.1VALWP circuit for EMI test.	0.1	41	Add PC207, PC208 SE042104K80(S CER CAP .1U 25V K X7R 0603)	2010/10/18	DVT
11	Add input Cup.	Add input Cup. and H/S gate resistance in CPU_COREP circuit for EMI ISN test.	0.1	44	Add PC209, PC210, PC211, PC212 SE042104K80(S CER CAP .1U 25V K X7R 0603) Add PC57, PC58 SE142106M80(S CER CAP 10U 25V M X5R 1206 H1.7) Add PR189, PR190 SD013000080(S RES 1/10W 0 +-5% 0603)	2010/10/19	DVT
12	Adjust VGA_COREP VID value	Adjust VGA_COREP VID value	0.1	43	Change PR128 from SD034100280 to SD034931180(S RES 1/16W 9.31K +-1% 0402) Change PR127 from SD034200280 to SD034154280(S RES 1/16W 15.4K +-1% 0402) Change PR131 from SD000009K00 to SD034301280(S RES 1/16W 30.1K +-1% 0402)	2010/10/21	DVT
13	change BOM structure	1.5VSP change BOM structure to @ for cost down	0.1	42	Change PU11, PL21, PQ39, PQ46, PR178, PR179, PR180, PR181, PR184, PR185, PR186, PC196, PC197, PC198, PC199, PC200, PC201, PC202, PC204 BOM structure to @ del PL20 SM01000C000(S SUPPRE_ TAI-TECH HCB2012KF-121T50 0805)	2010/10/21	DVT
14	change main source	change main source for reduce source	0.1	42	Change PQ36 from SB000009610 to SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010/10/26	DVT
15	Adjust VGA_COREP VID timing	Adjust VGA_COREP VID timing to avoid OVP.	0.1	43	Change PR130 from SD028100280 to SD034402280(S RES 1/16W 40.2K +-1% 0402)	2010/11/01	DVT
16	Delete precharge circuit	Delete precharge circuit to avoid adapter UVP.	0.1	36	del PR8, PR11, PR12 SD001100180(S RES 1/4W 1K +-5% 1206) del PD3 SC100001Y80(S DIO LL4148 LL-34 PANJIT) del PR9, PR10, PR13 SD028100380(S RES 1/16W 100K +-5% 0402) change PR7 SD001100180 to SD011000080(S RES 1/4W 0 +-5% 1206)	2010/11/01	DVT

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Issued Date	2010/04/12	Deciphered Date	2010/10/12

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Compal Electronics, Inc.

Title	PIR (PWR)	
Size: Custom	Document Number: PEW96 LA-6552P	Rev: 0.1
Date: Monday, November 15, 2010	Sheet 45 of 47	

Version change list (P.I.R. List)

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
1	Delete precharge circuit	Delete precharge circuit to avoid adapter UVP.	0.1	36	del PQ2 SB906100210(S TR TP0610K-T1-E3 1P SOT23) del PQ3, PQ4 SB301150200(S TR PDTC115EU NPN SOT323) del PD4 SCS00001200(S SCH DIO BAS40CW SOT-323)	2010/11/01	DVT
2	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	change PQ7 SB00000DL00 to SB00000I600(S TR SI4459ADY-T1-GE3 1P SO8)	2010/11/01	DVT
3	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	del PR21 SD034100380(S RES 1/16W 100K +-1% 0402) del PC17 SE075222K80(S CER CAP 2200P 25V K X7R 0402) del PQ12 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010/11/01	DVT
4	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	Add PR357 SD034200380(S RES 1/16W 200K +-1% 0402) add PC253 SE042104K80(S CER CAP .1U 25V K X7R 0603) add PQ61 SB000006800(S TR 2N7002W T/R7 1N SOT-323)	2010/11/01	DVT
5	Delete precharge 連動 circuit	Delete precharge 連動 circuit to avoid adapter UVP.	0.1	37	Add PD9, PD12 SC100001K00(S DIO 1SS355 SOD323 T/R-5K)	2010/11/01	DVT
6	Add input Cup.	Add input Cup. in CPU_COREP circuit for EMI ISN test.	0.1	44	Add PC213, PC214 SE042104K80(S CER CAP .1U 25V K X7R 0603)	2010/11/12	PVT
7							
8							
9							
10							
11							
12							
13							
14							
15							
16							

Security Classification	Compal Secret Data		
Issued Date	2010/04/12	Deciphered Date	2010/10/12

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Compal Electronics, Inc.
Title: PIR (PWR)
Size: Custom | Document Number: PEW96 LA-6552P | Rev: 0.1
Date: Monday, November 15, 2010 | Sheet 46 of 47

PHASE	PAGE	Modification list	PURPOSE
0.1	P08	First release	Base on PEW96, change platform (NB,CPU-->APU,SB820-->FCH)
0.2	P--	C220, C336, C347, C357, C359, C360, C387, C388, C389, C390, C391, C392, C393, C421, C427, C428, C1461 change 0603 size	Follow Standard Part 0805-->0603
0.2	P--	C721 C669, C1005, C705, C708, C713, C715, C736, C794, C797, C932, C934, C983 change 0603 size	Follow Standard Part 0805-->0603
0.2	P--	C215, C216, C218, C224, C226, C227, C229, C230, C231, C660, C671, C821, C823, C1210, C1517, C1522, C1526, C1529, C1532, C1512, C1523, C1443, C1445, C1446, C1447, C1448, C1452, C1453, C1454 change 0603 size	Follow Standard Part 0805-->0603
0.2	P35	R1122 change as 200k ohm, C1463 change as 0.1UF	Adjust sequence
0.2	P5	Add R109, R155	Pull up 4.7k ohm for CRT EDIE
0.2	P16	Unpop R632, C744, C69, C746; Pop R633	+VDDIO_18_FC Tie to GND for Nun-share ROM
0.2	P16	Add R635; Unpop R634	AMD suggestion for +VDDIO_AZ
0.2	P24	Add R170, R171	For DISO BOM option
0.2	P13	Add U33, C1199, R830, R838, R839	For VGA_PWRGD
0.2	P13	Remove C52, R557	For A_RST#
0.2	P27	EC_MUTE# change as 12 PIN form 46 PIN in Codec	For External Mute Fail issue
0.2	P16	C113, C77, C743, C96 change 0603 size and add C121, C105, C108, C109	22uF cap. change two 10uF cap. 0603 size
0.2	P19	C14 change 0603 size and add C52	22uF cap. change two 10uF cap. 0603 size
0.2	P13	C66, C67 change 27pF	Follow suggestion by TXC result
0.2	P26	C1485, C1486 change 33pF	Follow suggestion by TXC result
0.2	P33	C711 Change as SF000003I00	Material shortage
0.2	P9	Add C643, C675, C676, C678	For DDR3 moat issue
0.2	P26	Remove C939 ; Reserve C941, D48, D49, D51, L109	For LAN
0.2	P7	Add C604, C684	For CRT Moniter issue
0.3	P--	C212, C623 change 0603 size ; add C628, C685	Follow Standard Part 0805-->0603
0.3	P27	R786 change as 15k ohm	Dos Beep issue
0.3	P19	change R21, R22 as DISO@	Device Menage Audio issue
1.0	P27	Add R797, R800	Mic noise issue
1.0	P26,10	Reverse C939, C942, R456, R419, R426	for EMI ISN solution
1.0	P32	Add C753, C785	for EMI request

Change footprint
20100812 : For cost down purpose to change parts

Security Classification	Compal Secret Data		
Issued Date	2010/08/20	Deciphered Date	2011/08/20

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Compal Electronics, Inc.

Title: HW-PIR

Size	Document Number	Rev
B	LA-7092P P5WE6/H6/S6	1.0

Date: Tuesday, November 16, 2010 Sheet 47 of 47