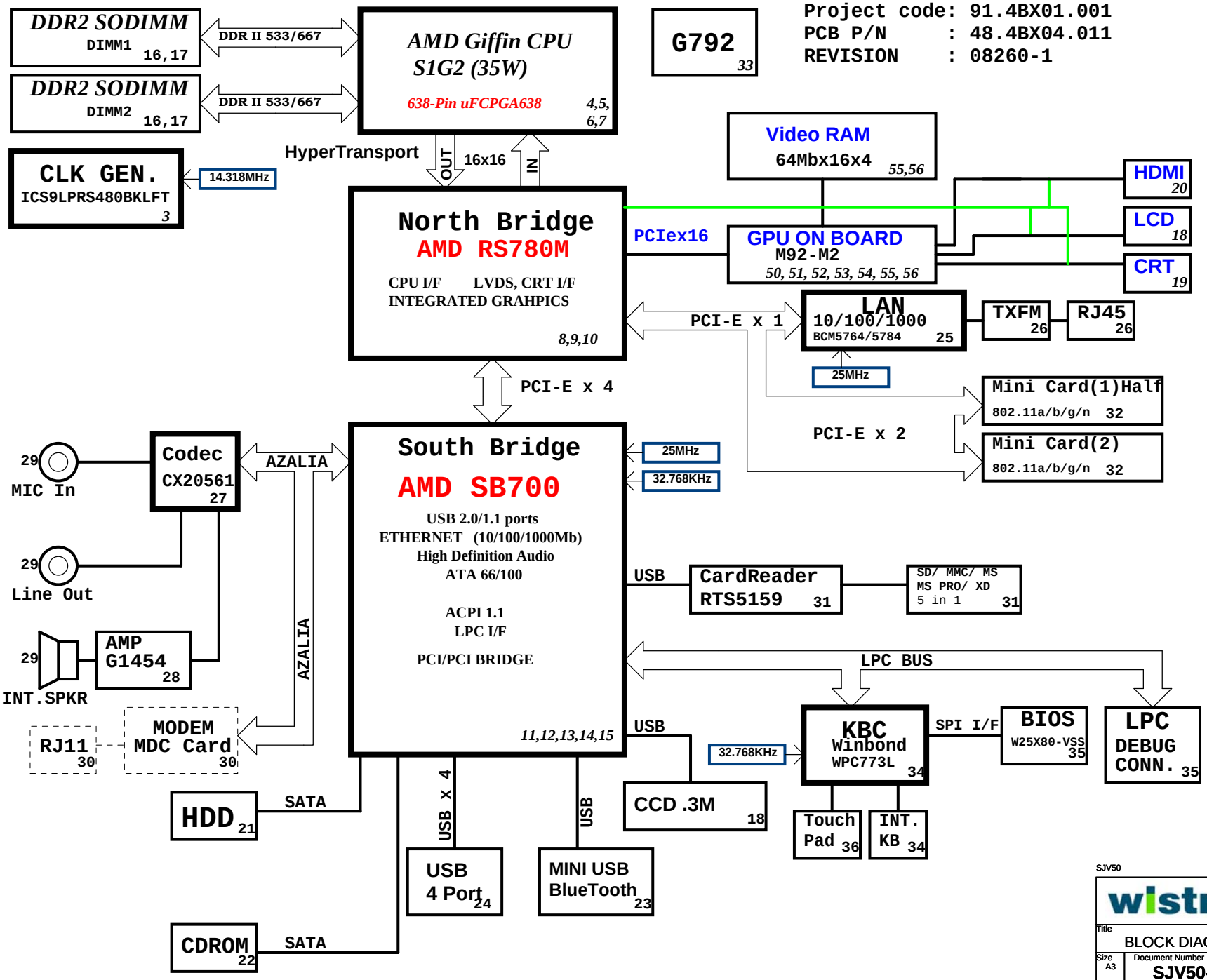
SJV50-PU Block Diagram



PCB Layer Stackup
L1: Signal 1
L2: VCC
L3: Inner Signal 2
L4: Inner Signal 3
L5: GND
L6: Signal 4

CPU V_CORE

INPUT	OUTPUT
DCBATOUT	VCC_CORE_S0

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	1D1V_S0 1D2V_S0 1D8V_S3

SYSTEM DC/DC

INPUT	OUTPUT
DCBATOUT	5V_S5 3D3V_S5

SYSTEM LDO

INPUT	OUTPUT
1D8V_S3	0D9V_S3

SYSTEM LDO

INPUT	OUTPUT
3D3V_S5 3D3V_S0 3D3V_S0	1D2V_S5 2D5V_S0 1D5V_S0

SYSTEM LDO

INPUT	OUTPUT
DCBATOUT	5V_AUX_S5 3D3V_AUX_S5

Battery Charger

INPUTS	OUTPUTS
AD+ BAT+	DCBATOUT

SJV50

wistron

Wistron Incorporated
21F, 88, Hsin Tai Wu Rd
Hsichih, Taipei

Title: BLOCK DIAGRAM

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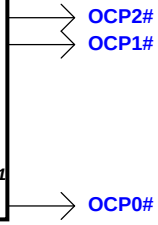
PCIE

PCIE0	LAN
PCIE1	MINICARD1
PCIE2	MINICARD2
PCIE3	

USB	
Pair	Device
11	CardReader
10	CCD
9	Mini Card2
8	USB4
7	USB1
6	USB2
5	BlueTooth
4	NC
3	NC
2	NC
1	Mini Card1
0	USB3



SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: USB&PCIE ROUTING

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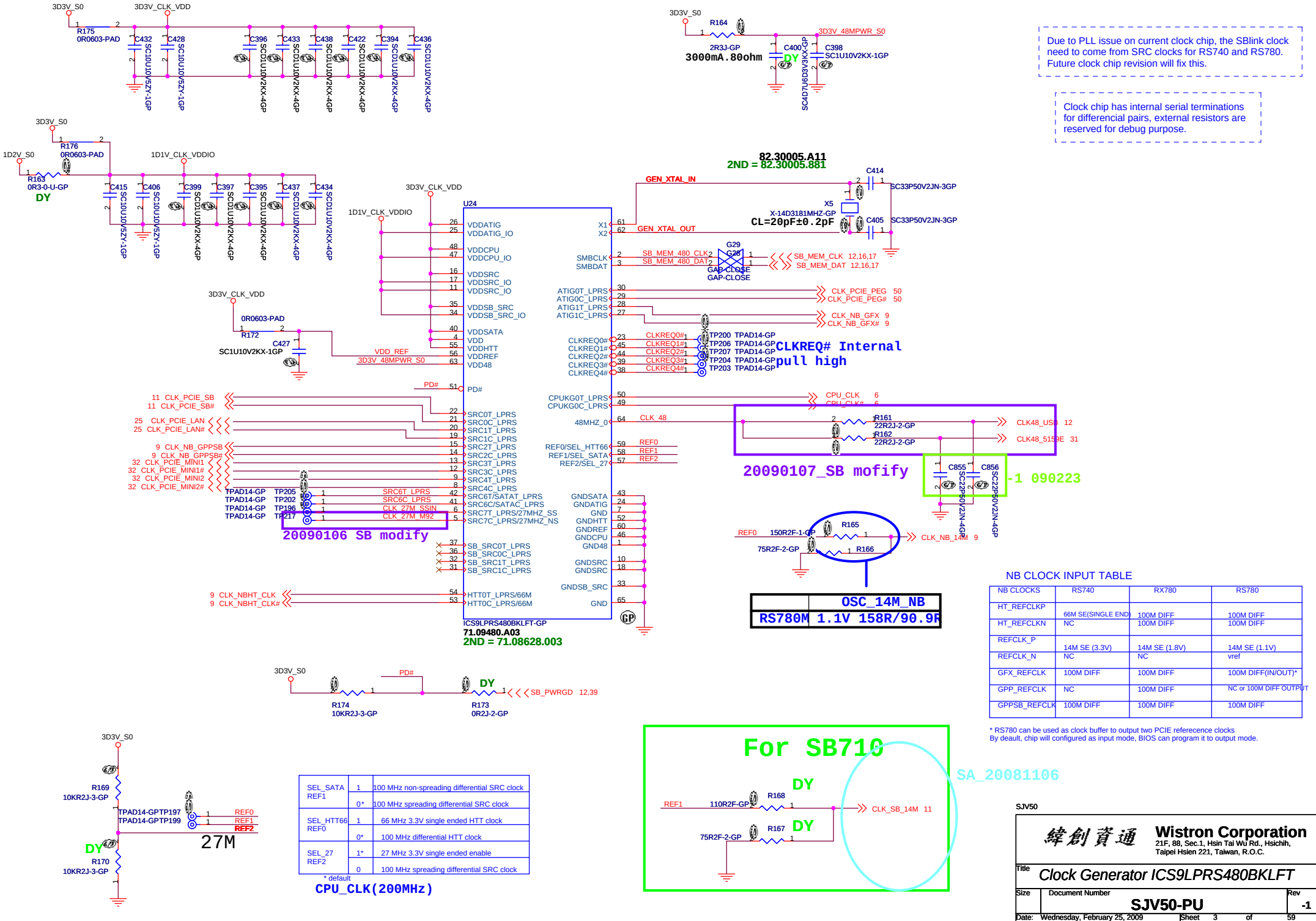
3D3V_S0
3D3V_CLK_VDD
R175 0R0603-PAD
C432 SC10U10V5ZY-1GP
C428 SC10U10V5ZY-1GP
C396 SCD1U10V2KX-4GP
C433 SCD1U10V2KX-4GP
C438 SCD1U10V2KX-4GP
C422 SCD1U10V2KX-4GP
C394 SCD1U10V2KX-4GP
C436 SCD1U10V2KX-4GP
3D3V_S0
R164
2R3J-GP
3000mA.80ohm
3D3V_48MPWR_S0
C400 DY
C398 SC1U10V2KX-1GP
SC4D7U6D3V3KX-GP
Due to PLL issue on current clock chip, the SBlink clock need to come from SRC clocks for RS740 and RS780. Future clock chip revision will fix this.
Clock chip has internal serial terminations for differencial pairs, external resistors are reserved for debug purpose.
3D3V_S0
R176 0R0603-PAD
1D2V_S0
R163 0R3-0-U-GP
DY
1D1V_CLK_VDDIO
C415 SC10U10V5ZY-1GP
C406 SC10U10V5ZY-1GP
C399 SCD1U10V2KX-4GP
C397 SCD1U10V2KX-4GP
C395 SCD1U10V2KX-4GP
C437 SCD1U10V2KX-4GP
C434 SCD1U10V2KX-4GP
82.30005.A11
2ND = 82.30005.881
3D3V_CLK_VDD
1D1V_CLK_VDDIO
U24
VDDATIG
VDDATIG_IO
VDDCPU
VDDCPU_IO
VDDSRC
VDDSRC_IO
VDDSRC_IO
VDDSB_SRC
VDDSB_SRC_IO
VDDSATA
VDD
VDDHTT
VDDREF
VDD48
GEN_XTAL_IN
GEN_XTAL_OUT
X5
X-14D3181MHZ-GP
CL=20pF±0.2pF
C414 SC33P50V2JN-3GP
C405 SC33P50V2JN-3GP
SMBCLK
SMBDAT
SB_MEM_480_CLK
SB_MEM_480_DAT
G29 G28 GAP-CLOSE GAP-CLOSE
SB_MEM_CLK 12,16,17
SB_MEM_DAT 12,16,17
ATIG0T_LPRS
ATIG0C_LPRS
ATIG1T_LPRS
ATIG1C_LPRS
CLK_PCIE_PEG 50
CLK_PCIE_PEG# 50
CLK_NB_GFX 9
CLK_NB_GFX# 9
CLKREQ0#
CLKREQ1#
CLKREQ2#
CLKREQ3#
CLKREQ4#
TP200 TPAD14-GP
TP206 TPAD14-GP
TP207 TPAD14-GP
TP204 TPAD14-GP
TP203 TPAD14-GP
CLKREQ# Internal pull high
3D3V_CLK_VDD
0R0603-PAD
R172
C427 SC1U10V2KX-1GP
VDD_REF
3D3V_48MPWR_S0
PD#
11 CLK_PCIE_SB
11 CLK_PCIE_SB#
25 CLK_PCIE_LAN
25 CLK_PCIE_LAN#
9 CLK_NB_GPPSB
9 CLK_NB_GPPSB#
32 CLK_PCIE_MINI1
32 CLK_PCIE_MINI1#
32 CLK_PCIE_MINI2
32 CLK_PCIE_MINI2#
SRC0T_LPRS
SRC0C_LPRS
SRC1T_LPRS
SRC1C_LPRS
SRC2T_LPRS
SRC2C_LPRS
SRC3T_LPRS
SRC3C_LPRS
SRC4T_LPRS
SRC4C_LPRS
SRC6T/SATAT_LPRS
SRC6C/SATAC_LPRS
SRC7T_LPRS/27MHZ_SS
SRC7C_LPRS/27MHZ_NS
TPAD14-GP TP205
TPAD14-GP TP202
TPAD14-GP TP196
TPAD14-GP TP217
SRC6T_LPRS
SRC6C_LPRS
CLK_27M_SSIN
CLK_27M_M92
20090106 SB modify
SB_SRC0T_LPRS
SB_SRC0C_LPRS
SB_SRC1T_LPRS
SB_SRC1C_LPRS
9 CLK_NBHT_CLK
9 CLK_NBHT_CLK#
HTT0T_LPRS/66M
HTT0C_LPRS/66M
ICS9LPRS480BKLFT-GP
71.09480.A03
2ND = 71.08628.003
CPUKG0T_LPRS
CPUKG0C_LPRS
CPU_CLK 6
CPU_CLK# 6
48MHZ_0
CLK_48
R161 22R2J-2-GP
R162 22R2J-2-GP
CLK48_USB 12
CLK48_515DE 31
20090107_SB mofify
REF0/SEL_HTT66
REF1/SEL_SATA
REF2/SEL_27
REF0
REF1
REF2
GNDSATA
GNDATIG
GND
GNDHTT
GNDREF
GNDCPU
GND48
GNDSRC
GNDSRC
GNDSB_SRC
GND
C855 SC22P50V2JN-4GP
C856 SC22P50V2JN-4GP
-1 090223
REF0
150R2F-1-GP
75R2F-2-GP
R165
R166
CLK_NB_14M 9
OSC_14M_NB
RS780M 1.1V 158R/90.9R
3D3V_S0
PD#
DY
SB_PWRGD 12,39
R174 10KR2J-3-GP
R173 0R2J-2-GP
NB CLOCK INPUT TABLE
NB CLOCKS | RS740 | RX780 | RS780
HT_REFCLKP | 66M SE(SINGLE END) | 100M DIFF | 100M DIFF
HT_REFCLKN | NC | 100M DIFF | 100M DIFF
REFCLK_P | 14M SE (3.3V) | 14M SE (1.8V) | 14M SE (1.1V)
REFCLK_N | NC | NC | vref
GFX_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF(IN/OUT)*
GPP_REFCLK | NC | 100M DIFF | NC or 100M DIFF OUTPUT
GPPSB_REFCLK | 100M DIFF | 100M DIFF | 100M DIFF
* RS780 can be used as clock buffer to output two PCIE refererence clocks
By deault, chip will configured as input mode, BIOS can program it to output mode.
3D3V_S0
R169 10KR2J-3-GP
TPAD14-GPTP197
TPAD14-GPTP199
REF0
REF1
REF2
27M
DY
R170 10KR2J-3-GP
SEL_SATA REF1
1 100 MHz non-spreading differential SRC clock
0* 100 MHz spreading differential SRC clock
SEL_HTT66 REF0
1 66 MHz 3.3V single ended HTT clock
0* 100 MHz differential HTT clock
SEL_27 REF2
1* 27 MHz 3.3V single ended enable
0 100 MHz spreading differential SRC clock
* default
CPU_CLK(200MHz)
For SB710
SA_20081106
DY
REF1
110R2F-GP
R168
CLK_SB_14M 11
DY
75R2F-2-GP
R167
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
Clock Generator ICS9LPRS480BKLFT
Size
Document Number
SJV50-PU
Rev
-1
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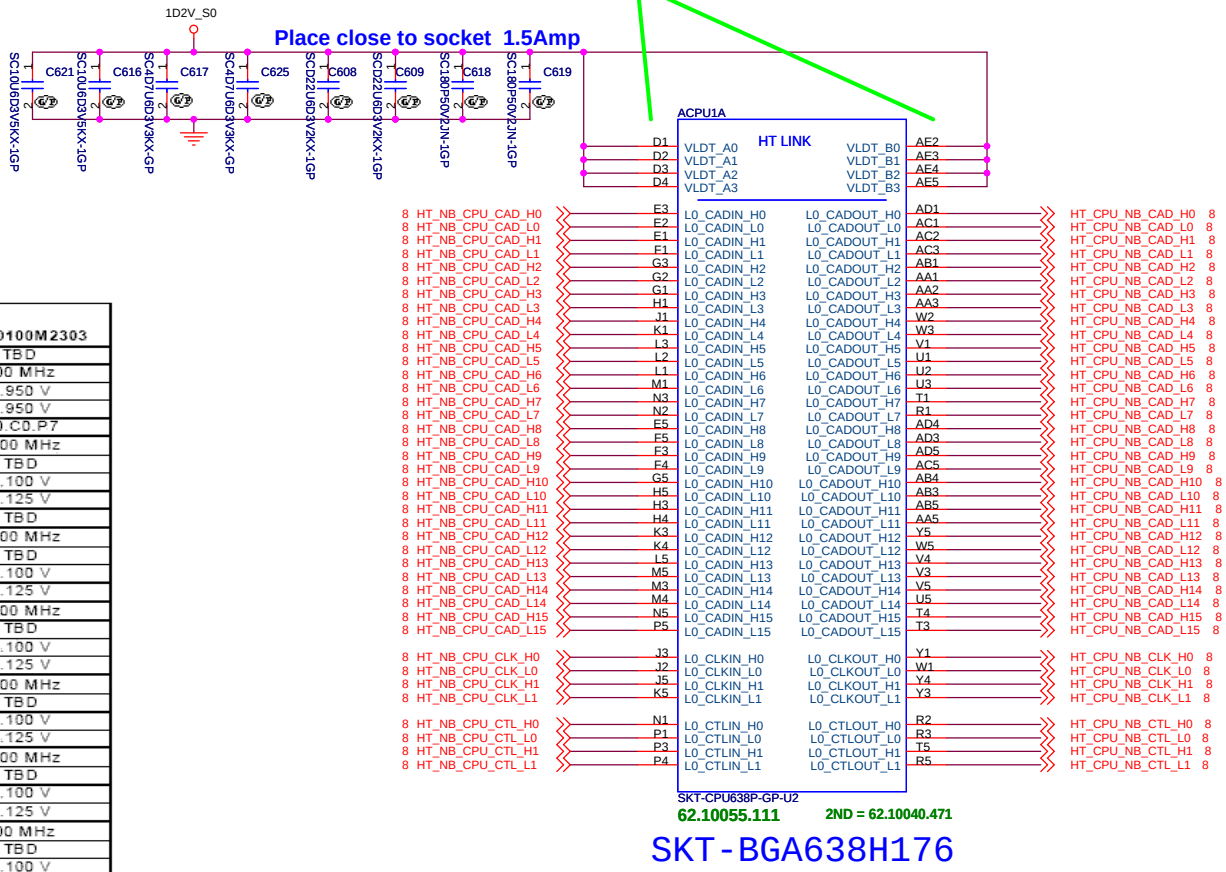
Placement note:
10ux1,4.7ux1,0.22ux1,180px1 for each group



State	Specification	Notes	2M200100M2303
S0.C0.Px	Tcase Max	3	TBD
	NB COF	1	400 MHz
	VID_VDDNB Min	2	0.950 V
	VID_VDDNB Max	2	0.950 V
	Startup P-state		S0.C0.P7
S0.C0.P0	CPU COF	1	2000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
	IDD Max	3	TBD
S0.C0.P1	CPU COF	1	1800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P2	CPU COF	1	1500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P3	CPU COF	1	1300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P4	CPU COF	1	1000 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P5	CPU COF	1	800 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P6	CPU COF	1	500 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V
S0.C0.P7	CPU COF	1	300 MHz
	TDP	3	TBD
	VID_VDD Min	2	1.100 V
	VID_VDD Max	2	1.125 V

SJV50

緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (1 of 4)***

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Placement note:
4.7ux2,0.22ux1,180px1 for each group
Place near to CPU

4.7u x 4 | 0.22u X 2 | 180P x 2

C122 DY C123 C135 DY C128 C150 C149 C139 C140

SC4D7U6D3V3KX-GP SCD22U6D3V2KX-4GP SCD22U6D3V2KX-1GP SC180P50V2JN-1GP

0D9V_S3

R315 39D2R2F-L-GP 1D8V_S3
R317 39D2R2F-L-GP TP125 TPAD14-GP MEM_RSVD_M1

ACPU1B

MEM:CMD/CTRL/CLK

D10	VTT1	VTT5	W10
C10	VTT2	VTT6	AC10
B10	VTT3	VTT7	AB10
AD10	VTT4	VTT8	AA10
		VTT9	A10
AE10	MEMZP		
AE10	MEMZN	VTT_SENSE	Y10
H16	RSVD_M1	MEMVREF	W17
		RSVD_M2	B18
T19	MA0_ODT0	MB0_ODT0	W26
V22	MA0_ODT1	MB0_ODT1	W23
U21	MA1_ODT0	MB1_ODT0	Y26
V19	MA1_ODT1		
T20	MA0_CS_L0	MB0_CS_L0	V26
U19	MA0_CS_L1	MB0_CS_L1	W25
U20	MA1_CS_L0	MB1_CS_L0	U22
V20	MA1_CS_L1		
J22	MA_CKE0	MB_CKE0	J25
J20	MA_CKE1	MB_CKE1	H26
N19	MA_CLK_H5	MB_CLK_H5	P22
N20	MA_CLK_L5	MB_CLK_L5	R22
E16	MA_CLK_H1	MB_CLK_H1	A17
F16	MA_CLK_L1	MB_CLK_L1	A18
Y16	MA_CLK_H7	MB_CLK_H7	AF18
AA16	MA_CLK_L7	MB_CLK_L7	AF17
P19	MA_CLK_H4	MB_CLK_H4	R26
P20	MA_CLK_L4	MB_CLK_L4	R25
N21	MA_ADD0	MB_ADD0	P24
M20	MA_ADD1	MB_ADD1	N24
N22	MA_ADD2	MB_ADD2	P26
M19	MA_ADD3	MB_ADD3	N23
M22	MA_ADD4	MB_ADD4	N26
L20	MA_ADD5	MB_ADD5	L23
M24	MA_ADD6	MB_ADD6	N25
L21	MA_ADD7	MB_ADD7	L24
L19	MA_ADD8	MB_ADD8	M26
K22	MA_ADD9	MB_ADD9	K26
R21	MA_ADD10	MB_ADD10	T26
L22	MA_ADD11	MB_ADD11	L26
K20	MA_ADD12	MB_ADD12	L25
V24	MA_ADD13	MB_ADD13	W24
K24	MA_ADD14	MB_ADD14	J23
K19	MA_ADD15	MB_ADD15	J24
R20	MA_BANK0	MB_BANK0	R24
R23	MA_BANK1	MB_BANK1	U26
J21	MA_BANK2	MB_BANK2	J26
R19	MA_RAS_L	MB_RAS_L	U25
T22	MA_CAS_L	MB_CAS_L	U24
T24	MA_WE_L	MB_WE_L	U23

SKT-CPU638P-GP-U2
62.10055.111

2ND = 62.10055.251

CLOSE TO CPU

1D8V_S3
C208 SCD1U10V2KX-4GP
VREF_DDR_CLAW
RN25 SRN1KJ-7-GP
C217 SC1U10V6MX-3GP
C235 SC1K50V2KX-1GP
C232 SCD1U10V2KX-4GP
DY

TP115 TPAD14-GP VTT_SENSE
TP140 TPAD14-GP MEM_RSVD_M2

MEM_MA0_ODT0 MEM_MA0_ODT1
MEM_MA0_CS#0 MEM_MA0_CS#1
MEM_MA_CKE0 MEM_MA_CKE1
MEM_MA_CLK0_P MEM_MA_CLK0_N MEM_MA_CLK1_P MEM_MA_CLK1_N
MEM_MA_ADD0 MEM_MA_ADD1 MEM_MA_ADD2 MEM_MA_ADD3 MEM_MA_ADD4 MEM_MA_ADD5 MEM_MA_ADD6 MEM_MA_ADD7 MEM_MA_ADD8 MEM_MA_ADD9 MEM_MA_ADD10 MEM_MA_ADD11 MEM_MA_ADD12 MEM_MA_ADD13 MEM_MA_ADD14 MEM_MA_ADD15
MEM_MA_BANK0 MEM_MA_BANK1 MEM_MA_BANK2
MEM_MA_RAS# MEM_MA_CAS# MEM_MA_WE#

MEM_MB_ODT0 16 MEM_MB_ODT1 16
MEM_MB_CS#0 16 MEM_MB_CS#1 16
MEM_MB_CKE0 16 MEM_MB_CKE1 16
MEM_MB_CLK0_P 16 MEM_MB_CLK0_N 16 MEM_MB_CLK1_P 16 MEM_MB_CLK1_N 16
MEM_MB_ADD0 16 MEM_MB_ADD1 16 MEM_MB_ADD2 16 MEM_MB_ADD3 16 MEM_MB_ADD4 16 MEM_MB_ADD5 16 MEM_MB_ADD6 16 MEM_MB_ADD7 16 MEM_MB_ADD8 16 MEM_MB_ADD9 16 MEM_MB_ADD10 16 MEM_MB_ADD11 16 MEM_MB_ADD12 16 MEM_MB_ADD13 16 MEM_MB_ADD14 16 MEM_MB_ADD15 16
MEM_MB_BANK0 16 MEM_MB_BANK1 16 MEM_MB_BANK2 16
MEM_MB_RAS# 16 MEM_MB_CAS# 16 MEM_MB_WE# 16

ACPU1C

MEM:DATA

MEM_MA_DATA0	G12	MA_DATA0	MB_DATA0	C11	MEM_MB_DATA0 16
MEM_MA_DATA1	F12	MA_DATA1	MB_DATA1	A11	MEM_MB_DATA1 16
MEM_MA_DATA2	H14	MA_DATA2	MB_DATA2	A14	MEM_MB_DATA2 16
MEM_MA_DATA3	G14	MA_DATA3	MB_DATA3	B14	MEM_MB_DATA3 16
MEM_MA_DATA4	H11	MA_DATA4	MB_DATA4	G11	MEM_MB_DATA4 16
MEM_MA_DATA5	H12	MA_DATA5	MB_DATA5	E11	MEM_MB_DATA5 16
MEM_MA_DATA6	C13	MA_DATA6	MB_DATA6	D12	MEM_MB_DATA6 16
MEM_MA_DATA7	E13	MA_DATA7	MB_DATA7	A13	MEM_MB_DATA7 16
MEM_MA_DATA8	H15	MA_DATA8	MB_DATA8	A15	MEM_MB_DATA8 16
MEM_MA_DATA9	E15	MA_DATA9	MB_DATA9	A16	MEM_MB_DATA9 16
MEM_MA_DATA10	E17	MA_DATA10	MB_DATA10	A19	MEM_MB_DATA10 16
MEM_MA_DATA11	H17	MA_DATA11	MB_DATA11	A20	MEM_MB_DATA11 16
MEM_MA_DATA12	E14	MA_DATA12	MB_DATA12	C14	MEM_MB_DATA12 16
MEM_MA_DATA13	F14	MA_DATA13	MB_DATA13	D14	MEM_MB_DATA13 16
MEM_MA_DATA14	C17	MA_DATA14	MB_DATA14	C18	MEM_MB_DATA14 16
MEM_MA_DATA15	G17	MA_DATA15	MB_DATA15	D18	MEM_MB_DATA15 16
MEM_MA_DATA16	G18	MA_DATA16	MB_DATA16	D20	MEM_MB_DATA16 16
MEM_MA_DATA17	C19	MA_DATA17	MB_DATA17	A21	MEM_MB_DATA17 16
MEM_MA_DATA18	D22	MA_DATA18	MB_DATA18	D24	MEM_MB_DATA18 16
MEM_MA_DATA19	E20	MA_DATA19	MB_DATA19	C25	MEM_MB_DATA19 16
MEM_MA_DATA20	E18	MA_DATA20	MB_DATA20	B20	MEM_MB_DATA20 16
MEM_MA_DATA21	F18	MA_DATA21	MB_DATA21	C20	MEM_MB_DATA21 16
MEM_MA_DATA22	B22	MA_DATA22	MB_DATA22	B24	MEM_MB_DATA22 16
MEM_MA_DATA23	C23	MA_DATA23	MB_DATA23	C24	MEM_MB_DATA23 16
MEM_MA_DATA24	F20	MA_DATA24	MB_DATA24	E23	MEM_MB_DATA24 16
MEM_MA_DATA25	F22	MA_DATA25	MB_DATA25	E24	MEM_MB_DATA25 16
MEM_MA_DATA26	H24	MA_DATA26	MB_DATA26	G25	MEM_MB_DATA26 16
MEM_MA_DATA27	J19	MA_DATA27	MB_DATA27	G26	MEM_MB_DATA27 16
MEM_MA_DATA28	E21	MA_DATA28	MB_DATA28	C26	MEM_MB_DATA28 16
MEM_MA_DATA29	E22	MA_DATA29	MB_DATA29	D26	MEM_MB_DATA29 16
MEM_MA_DATA30	H20	MA_DATA30	MB_DATA30	G23	MEM_MB_DATA30 16
MEM_MA_DATA31	H22	MA_DATA31	MB_DATA31	G24	MEM_MB_DATA31 16
MEM_MA_DATA32	Y24	MA_DATA32	MB_DATA32	AA24	MEM_MB_DATA32 16
MEM_MA_DATA33	AB24	MA_DATA33	MB_DATA33	AA23	MEM_MB_DATA33 16
MEM_MA_DATA34	AB22	MA_DATA34	MB_DATA34	AD24	MEM_MB_DATA34 16
MEM_MA_DATA35	AA21	MA_DATA35	MB_DATA35	AE24	MEM_MB_DATA35 16
MEM_MA_DATA36	W22	MA_DATA36	MB_DATA36	AA26	MEM_MB_DATA36 16
MEM_MA_DATA37	W21	MA_DATA37	MB_DATA37	AA25	MEM_MB_DATA37 16
MEM_MA_DATA38	Y22	MA_DATA38	MB_DATA38	AD26	MEM_MB_DATA38 16
MEM_MA_DATA39	AA22	MA_DATA39	MB_DATA39	AE25	MEM_MB_DATA39 16
MEM_MA_DATA40	Y20	MA_DATA40	MB_DATA40	AC22	MEM_MB_DATA40 16
MEM_MA_DATA41	AA20	MA_DATA41	MB_DATA41	AD22	MEM_MB_DATA41 16
MEM_MA_DATA42	AA18	MA_DATA42	MB_DATA42	AE20	MEM_MB_DATA42 16
MEM_MA_DATA43	AB18	MA_DATA43	MB_DATA43	AF20	MEM_MB_DATA43 16
MEM_MA_DATA44	AB21	MA_DATA44	MB_DATA44	AF24	MEM_MB_DATA44 16
MEM_MA_DATA45	AD21	MA_DATA45	MB_DATA45	AF23	MEM_MB_DATA45 16
MEM_MA_DATA46	AD19	MA_DATA46	MB_DATA46	AC20	MEM_MB_DATA46 16
MEM_MA_DATA47	Y18	MA_DATA47	MB_DATA47	AD20	MEM_MB_DATA47 16
MEM_MA_DATA48	AD17	MA_DATA48	MB_DATA48	AD18	MEM_MB_DATA48 16
MEM_MA_DATA49	W16	MA_DATA49	MB_DATA49	AE18	MEM_MB_DATA49 16
MEM_MA_DATA50	W14	MA_DATA50	MB_DATA50	AC14	MEM_MB_DATA50 16
MEM_MA_DATA51	Y14	MA_DATA51	MB_DATA51	AD14	MEM_MB_DATA51 16
MEM_MA_DATA52	Y17	MA_DATA52	MB_DATA52	AF19	MEM_MB_DATA52 16
MEM_MA_DATA53	AB17	MA_DATA53	MB_DATA53	AC18	MEM_MB_DATA53 16
MEM_MA_DATA54	AB15	MA_DATA54	MB_DATA54	AF16	MEM_MB_DATA54 16
MEM_MA_DATA55	AD15	MA_DATA55	MB_DATA55	AF15	MEM_MB_DATA55 16
MEM_MA_DATA56	AB13	MA_DATA56	MB_DATA56	AF13	MEM_MB_DATA56 16
MEM_MA_DATA57	AD13	MA_DATA57	MB_DATA57	AC12	MEM_MB_DATA57 16
MEM_MA_DATA58	Y12	MA_DATA58	MB_DATA58	AB11	MEM_MB_DATA58 16
MEM_MA_DATA59	W11	MA_DATA59	MB_DATA59	Y11	MEM_MB_DATA59 16
MEM_MA_DATA60	AB14	MA_DATA60	MB_DATA60	AE14	MEM_MB_DATA60 16
MEM_MA_DATA61	AA14	MA_DATA61	MB_DATA61	AE14	MEM_MB_DATA61 16
MEM_MA_DATA62	AB12	MA_DATA62	MB_DATA62	AF11	MEM_MB_DATA62 16
MEM_MA_DATA63	AA12	MA_DATA63	MB_DATA63	AD11	MEM_MB_DATA63 16
MEM_MA_DM0	E12	MA_DM0	MB_DM0	A12	MEM_MB_DM0 16
MEM_MA_DM1	C15	MA_DM1	MB_DM1	B16	MEM_MB_DM1 16
MEM_MA_DM2	E19	MA_DM2	MB_DM2	A22	MEM_MB_DM2 16
MEM_MA_DM3	F24	MA_DM3	MB_DM3	E25	MEM_MB_DM3 16
MEM_MA_DM4	AC24	MA_DM4	MB_DM4	AB26	MEM_MB_DM4 16
MEM_MA_DM5	Y19	MA_DM5	MB_DM5	AE22	MEM_MB_DM5 16
MEM_MA_DM6	AB16	MA_DM6	MB_DM6	AC16	MEM_MB_DM6 16
MEM_MA_DM7	Y13	MA_DM7	MB_DM7	AD12	MEM_MB_DM7 16
MEM_MA_DQS0_P	G13	MA_DQS_H0	MB_DQS_H0	C12	MEM_MB_DQS0_P 16
MEM_MA_DQS0_N	H13	MA_DQS_L0	MB_DQS_L0	B12	MEM_MB_DQS0_N 16
MEM_MA_DQS1_P	G16	MA_DQS_H1	MB_DQS_H1	D16	MEM_MB_DQS1_P 16
MEM_MA_DQS1_N	G15	MA_DQS_L1	MB_DQS_L1	C16	MEM_MB_DQS1_N 16
MEM_MA_DQS2_P	C22	MA_DQS_H2	MB_DQS_H2	A24	MEM_MB_DQS2_P 16
MEM_MA_DQS2_N	C21	MA_DQS_L2	MB_DQS_L2	A23	MEM_MB_DQS2_N 16
MEM_MA_DQS3_P	G22	MA_DQS_H3	MB_DQS_H3	F26	MEM_MB_DQS3_P 16
MEM_MA_DQS3_N	G21	MA_DQS_L3	MB_DQS_L3	E26	MEM_MB_DQS3_N 16
MEM_MA_DQS4_P	AD23	MA_DQS_H4	MB_DQS_H4	AC25	MEM_MB_DQS4_P 16
MEM_MA_DQS4_N	AC23	MA_DQS_L4	MB_DQS_L4	AC26	MEM_MB_DQS4_N 16
MEM_MA_DQS5_P	AB19	MA_DQS_H5	MB_DQS_H5	AF21	MEM_MB_DQS5_P 16
MEM_MA_DQS5_N	AB20	MA_DQS_L5	MB_DQS_L5	AF22	MEM_MB_DQS5_N 16
MEM_MA_DQS6_P	Y15	MA_DQS_H6	MB_DQS_H6	AE16	MEM_MB_DQS6_P 16
MEM_MA_DQS6_N	W15	MA_DQS_L6	MB_DQS_L6	AD16	MEM_MB_DQS6_N 16
MEM_MA_DQS7_P	W12	MA_DQS_H7	MB_DQS_H7	AE12	MEM_MB_DQS7_P 16
MEM_MA_DQS7_N	W13	MA_DQS_L7	MB_DQS_L7	AE12	MEM_MB_DQS7_N 16

SKT-CPU638P-GP-U2
62.10055.111

2ND = 62.10055.251

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (2 of 4)***

Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 5 of 59

The Processor has reached a preset maximum operating temperature. 100℃
I=Active HTC
O=FAN

LYAOUT:ROUTE VDDA TRACE APPROX. 50mils WIDE(USE 2X25 mil TRACES TO EXIT BALL FIELD) AND 500 mils LONG.

IF 0 ohm IS NOT GOOD ENOUGH, TRY 68.00082.491

SA_20081127

-1 090213

Cloce To CPU

For HDT DBG

internal pull high 300 ohm

LAYOUT: Route FBCLKOUT_H/L differentially impedance 80

20081126

CPU exceeds to 125℃

SA_20081030

HDT Connectors

CPU_DBREQ#	7	8	
CPU_DBRDY	9	10	
CPU_TCK	11	12	
CPU_TMS	13	14	
CPU_TDI	15	16	
CPU_TRST#	17	18	
CPU_TDO	19	20	
	21	22	
1D8V_S3	23	24	
		26	

SMC-CONN26A-FP

HDT_RST#

SJV50

Wistron Corporation
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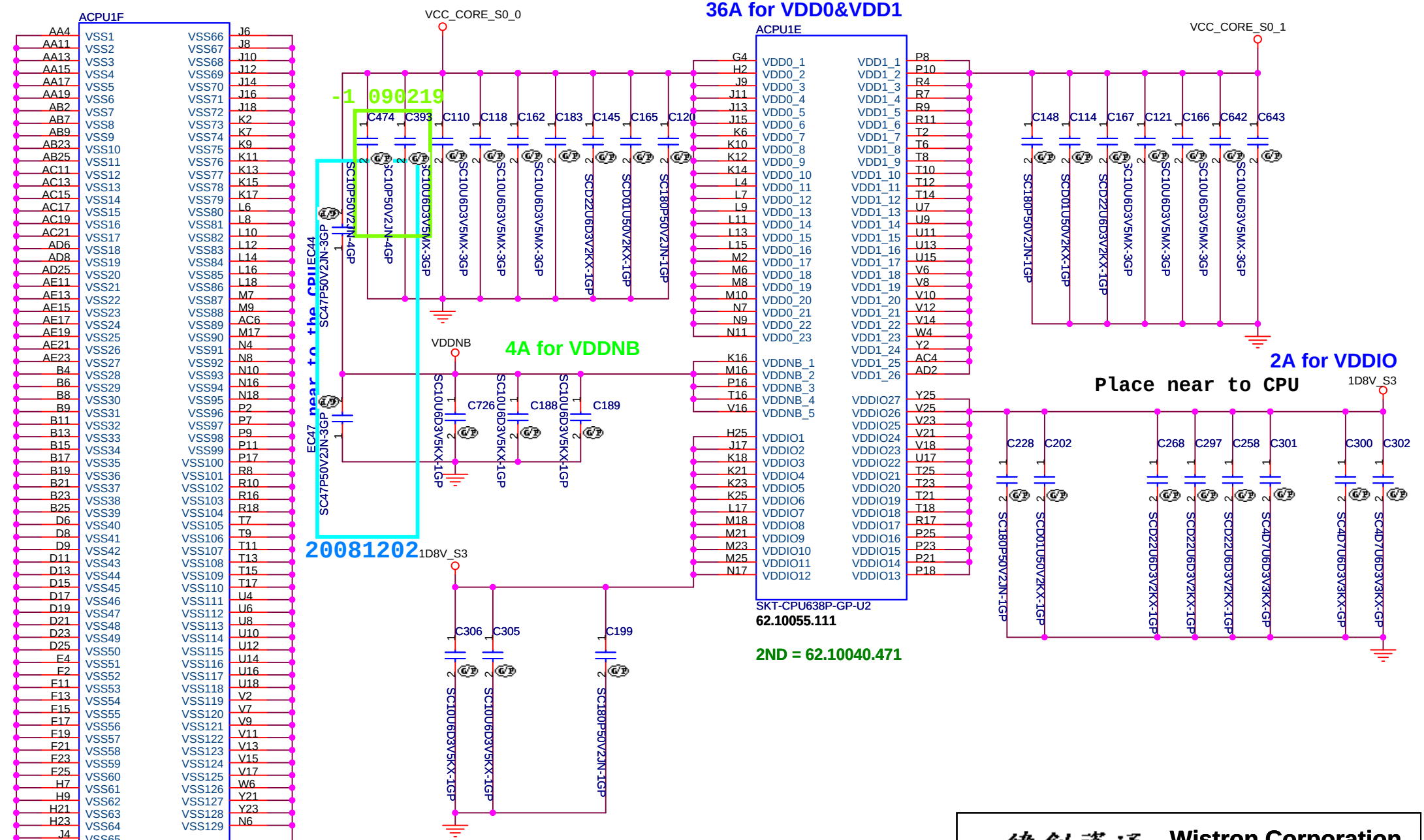
Taipei Hsien 221, Taiwan, R.O.C.

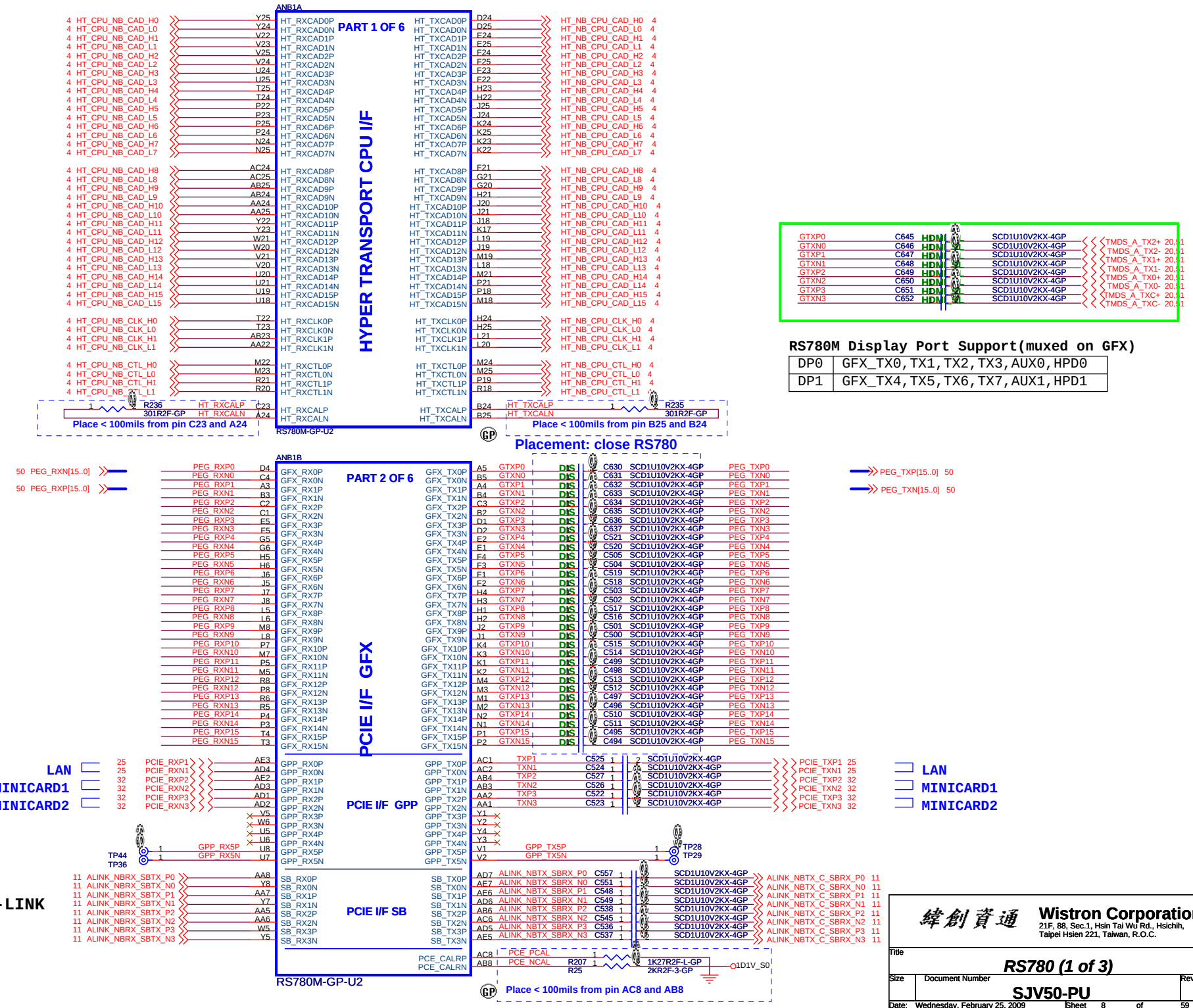
Title: CPU (3 of 4)

Size | Document Number: SJV50-PU | Rev: -1

Date: Wednesday, February 25, 2009 | Sheet 6 of 59



緯創資通	**Wistron Corporation**	
	21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CPU (4 of 4)***	
Size	Document Number: **SJV50-PU**	Rev: **-1**
Date: Wednesday, February 25, 2009	Sheet 7 of 59	



RS780M Display Port Support(muxed on GFX)

DP0	GFX_TX0,TX1,TX2,TX3,AUX0,HPD0
DP1	GFX_TX4,TX5,TX6,TX7,AUX1,HPD1

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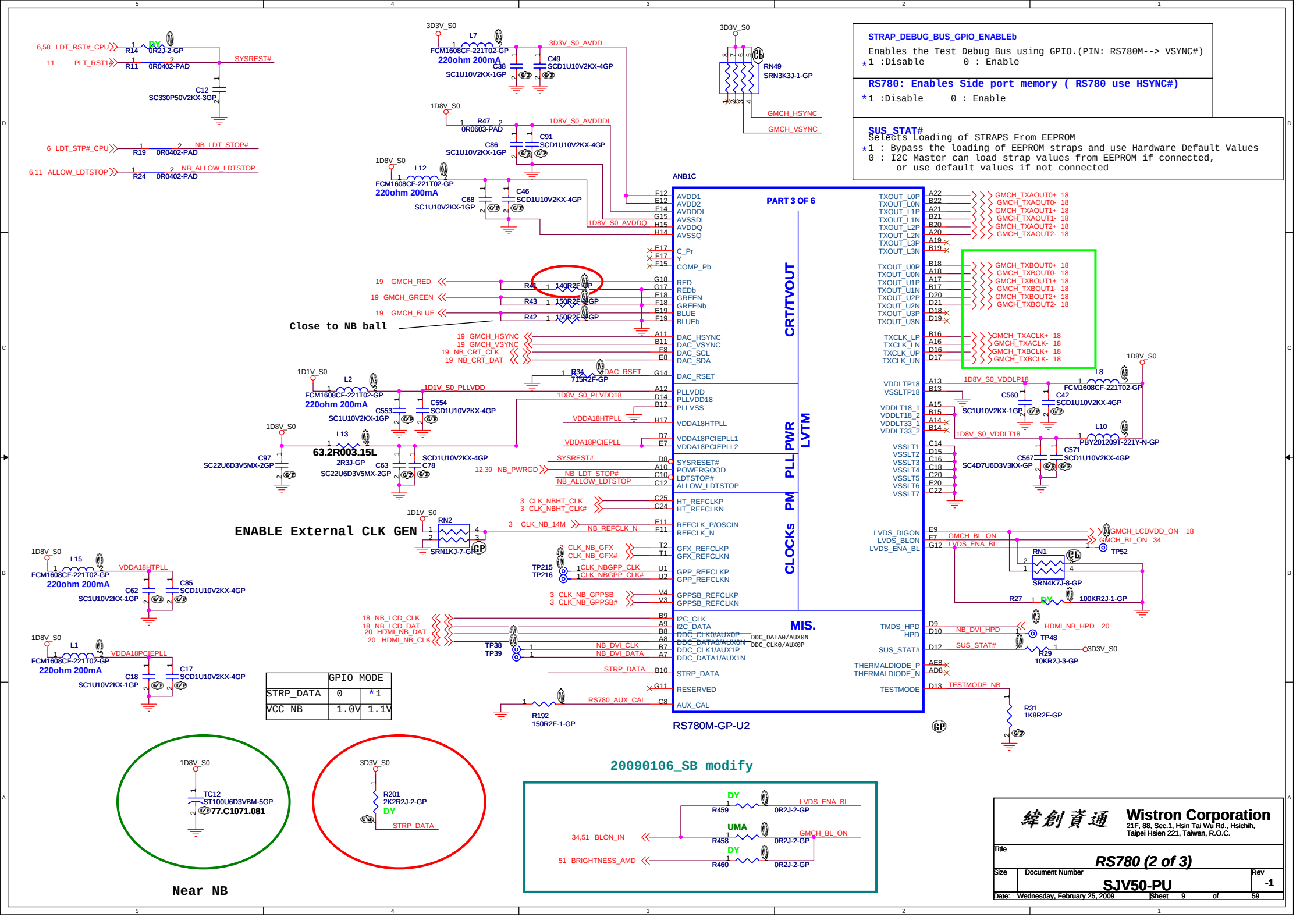
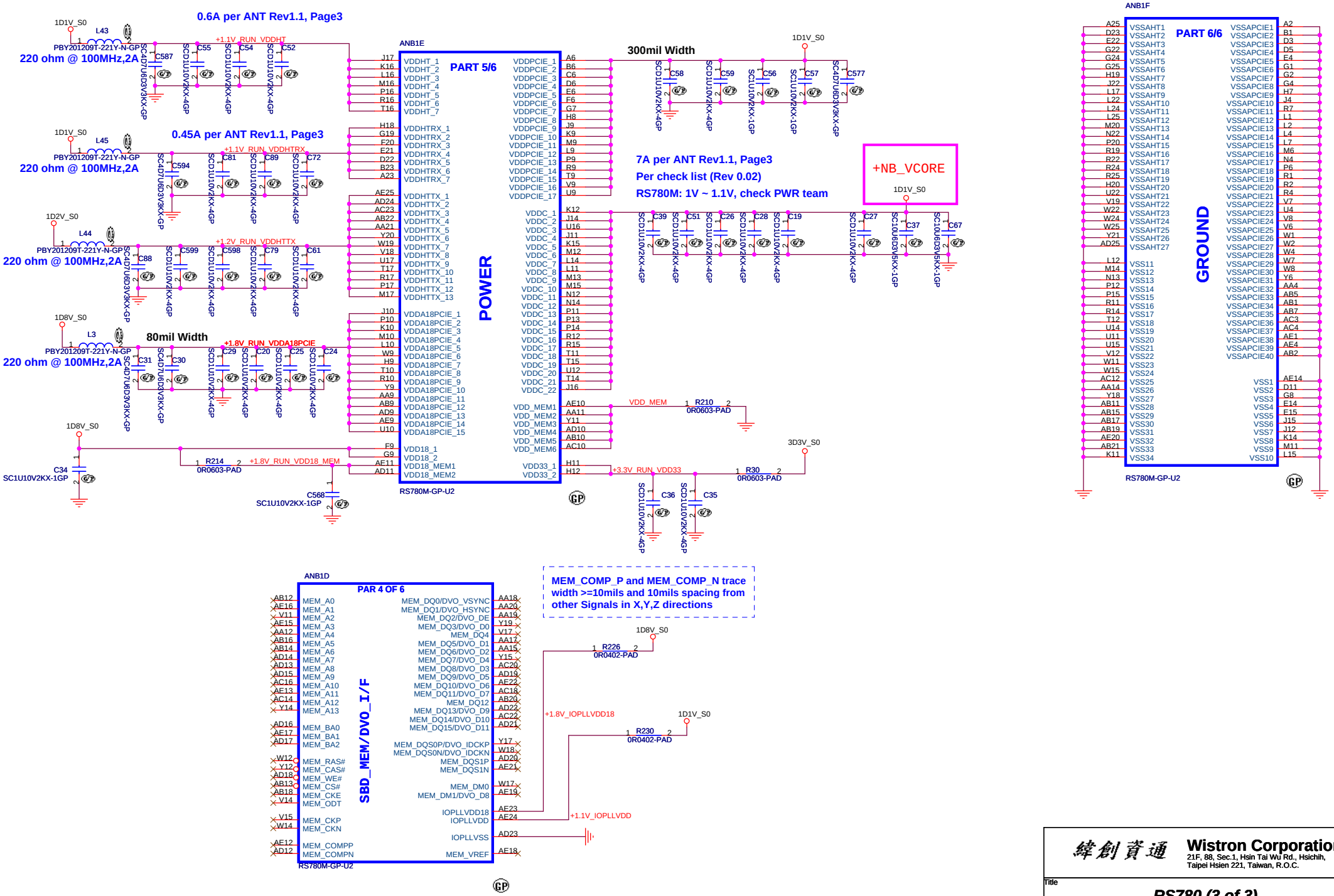
Title: RS780 (1 of 3)

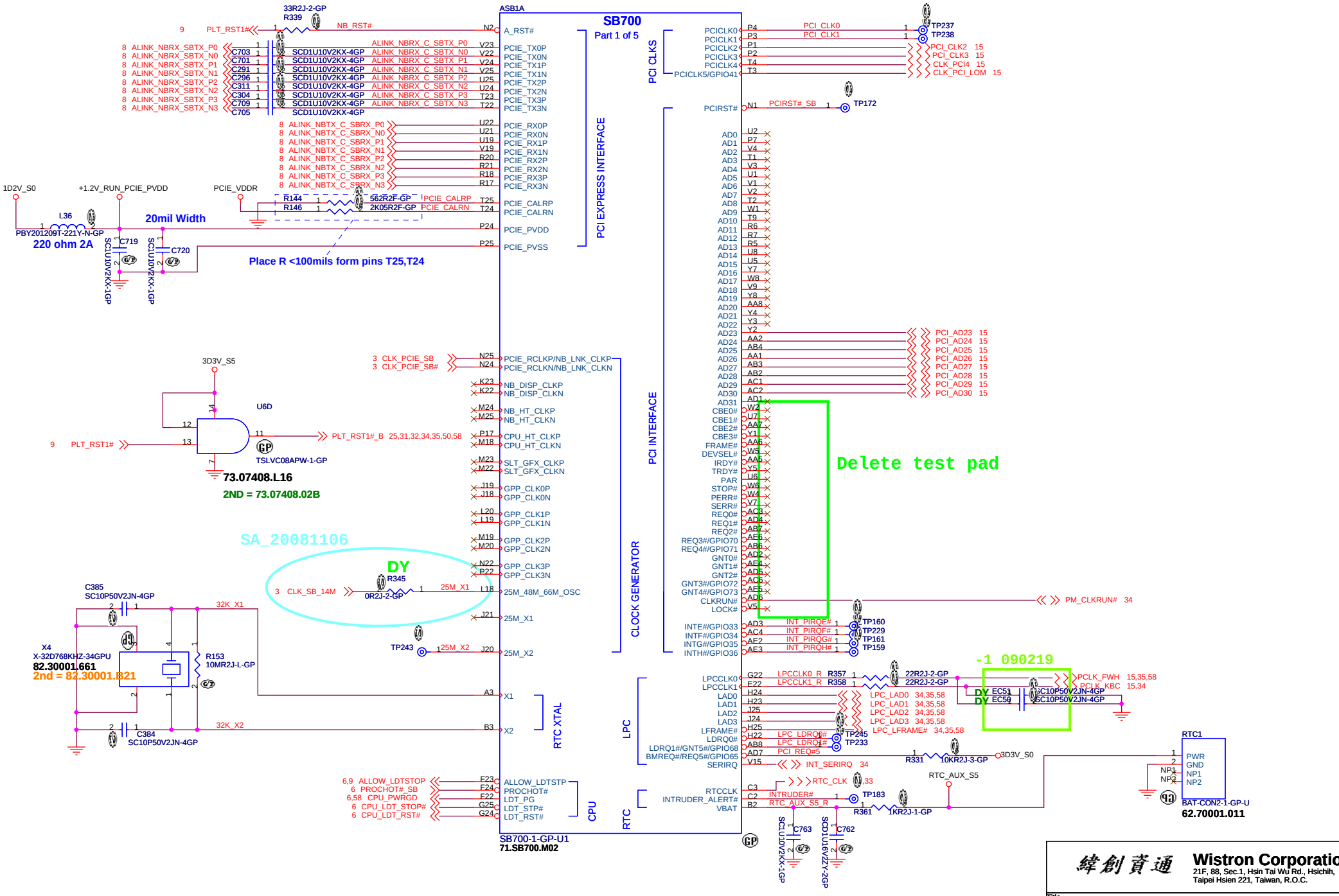
Size: | Document Number: SJV50-PU | Rev: -1

Date: Wednesday, February 25, 2009 | Sheet 8 of 59

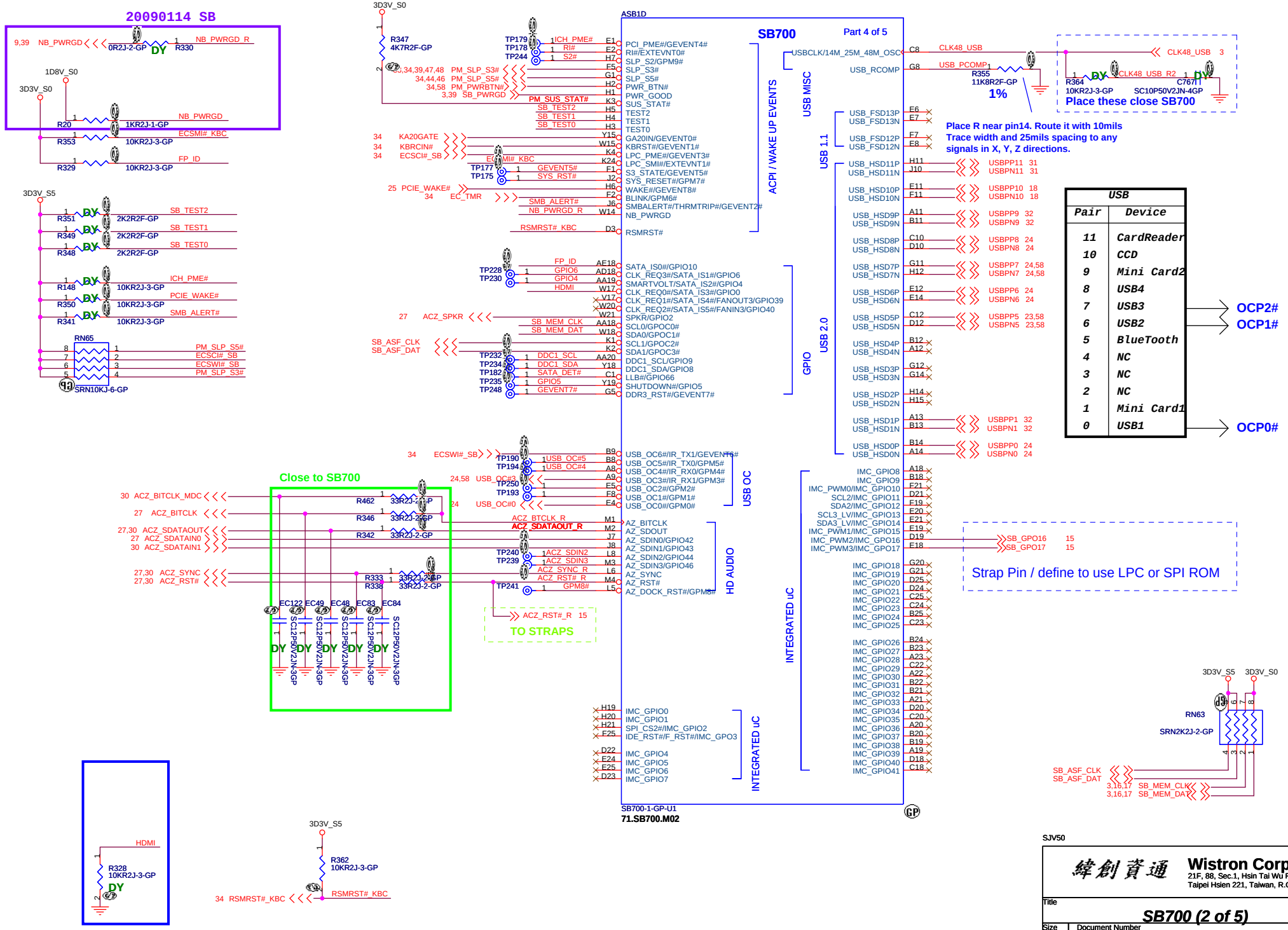


	GPIO MODE	
STRP_DATA	0	*1
VCC_NB	1.0V	1.1V


0.6A per ANT Rev1.1, Page3
0.45A per ANT Rev1.1, Page3
80mil Width
300mil Width
7A per ANT Rev1.1, Page3
Per check list (Rev 0.02)
RS780M: 1V ~ 1.1V, check PWR team
+NB_VCORE
ANB1E
PART 5/6
POWER
RS780M-GP-U2
ANB1F
PART 6/6
GROUND
RS780M-GP-U2
ANB1D
PAR 4 OF 6
SBD_MEM/DVO_I/F
RS780M-GP-U2
MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
RS780 (3 of 3)
SJV50-PU
-1
Wednesday, February 25, 2009
10
59



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title	***SB700 (1 of 5)***		
Size	Document Number **SJV50-PU**		Rev -1
Date: Wednesday, February 25, 2009	Sheet 11 of 59		



SJV50

Wistron Corporation
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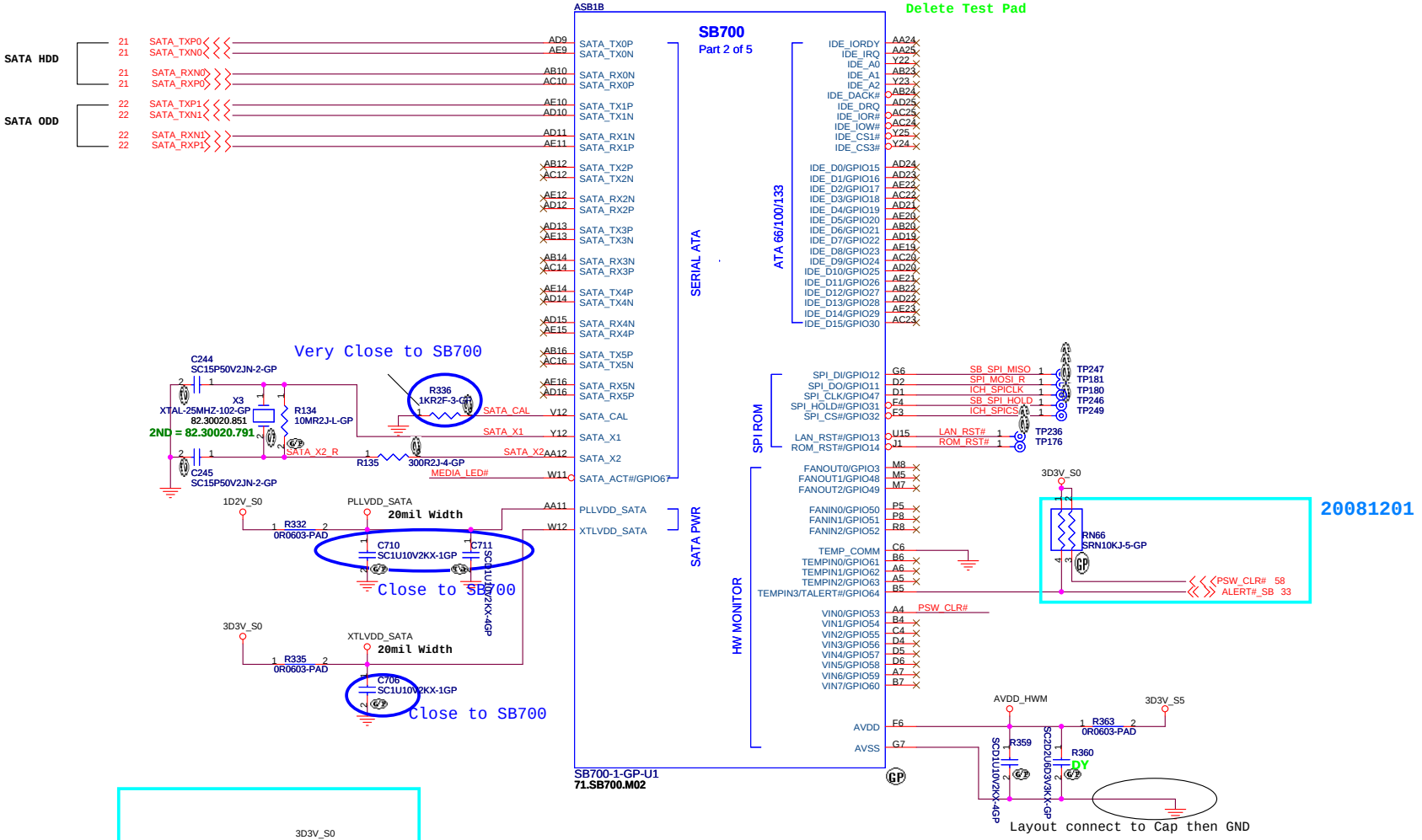
Title: SB700 (2 of 5)

Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 12 of 59



SJV50

Wistron Corporation
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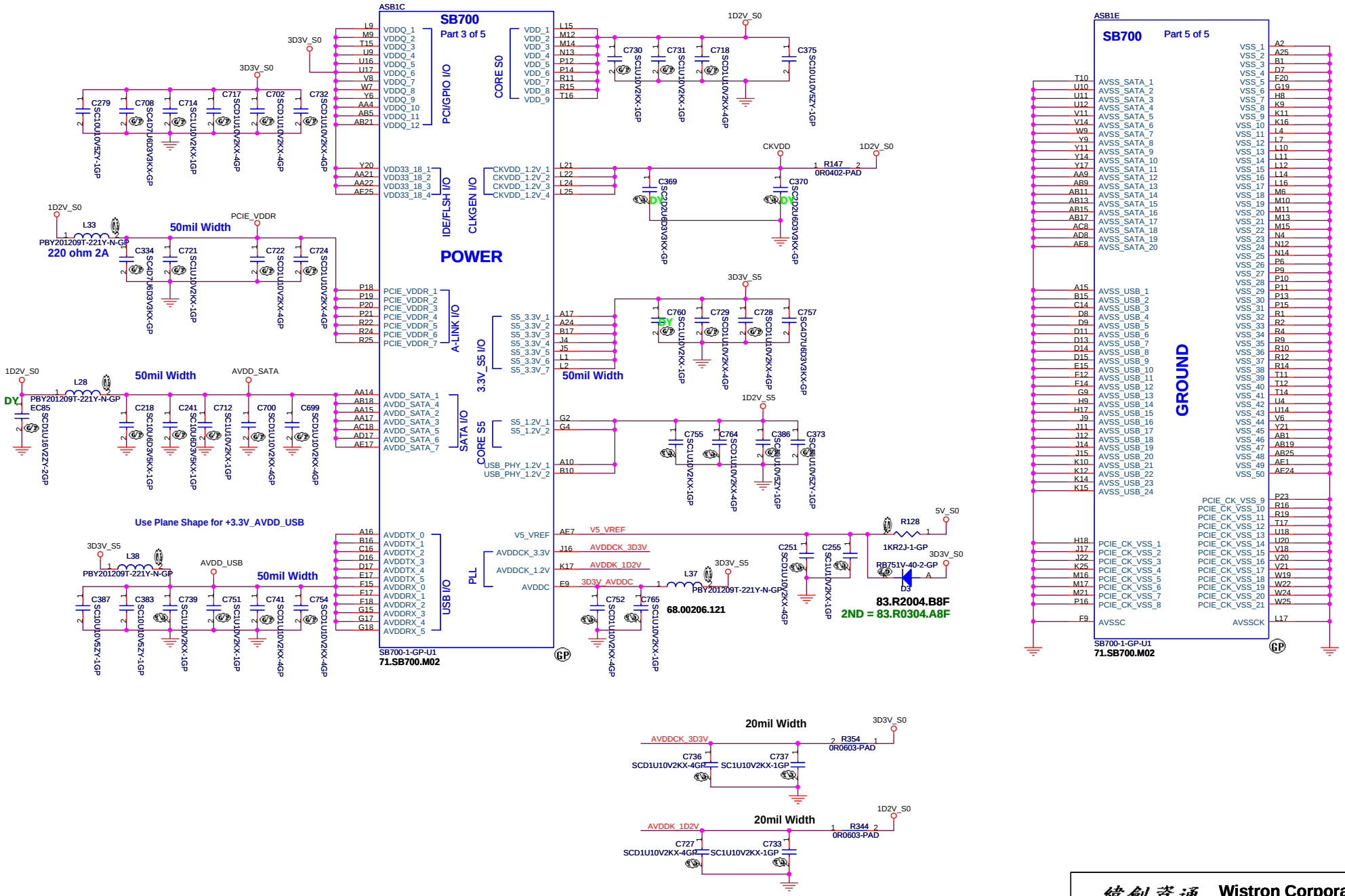
Taipei Hsien 221, Taiwan, R.O.C.

Title: SB700 (3 of 5)

Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 13 of 59



Wistron Corporation		
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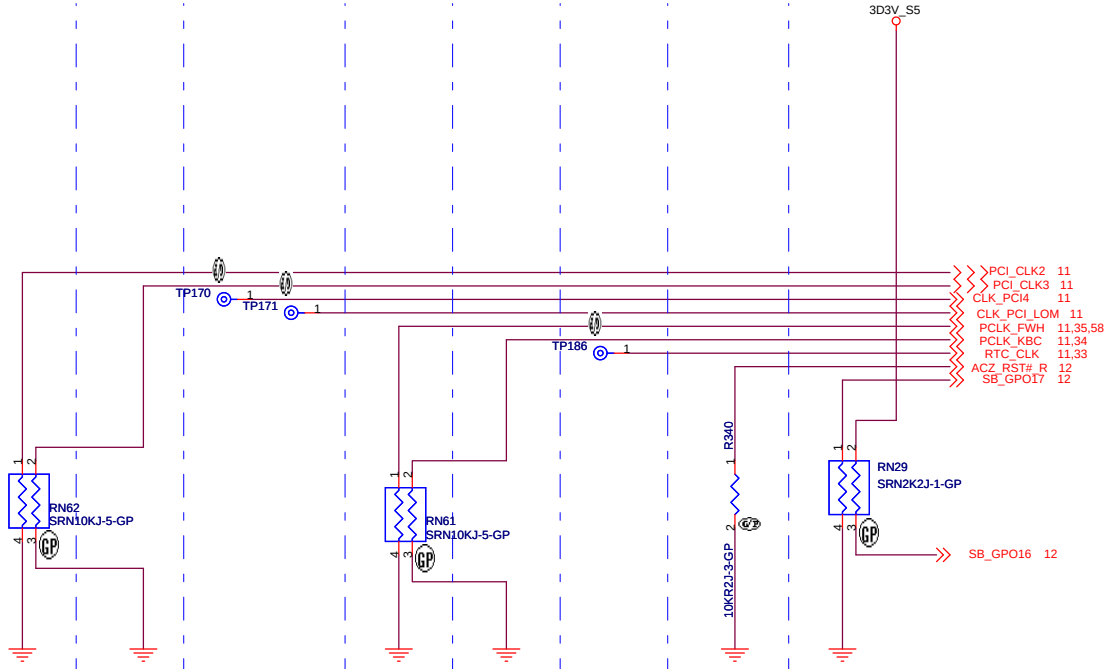
Title	SB700 (4 of 5)	
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 14 of 59	

Delete DY Parts

REQUIRED STRAPS

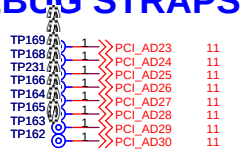
REQUIRED SYSTEM STRAPS



	PCI_CLK2	PCI_CLK3	CLK_PCI_LOM CLK_PCI4	PCLK_FWH	PCLK_KBC	RTCCLK	AZ_RST#	SB_GPO17 , SB_GPO16
PULL HIGH	WatchDOG (NB_PWRGD) ENABLED	USE DEBUG STRAPS	RESERVED	IMC ENABLED	CLKGEN ENABLED (Use Internal)	INTERNAL RTC DEFAULT	ENABLE PCI ROM BOOT	ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT
PULL LOW	WatchDog (NB_PWRGD) DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT		IMC DISABLED DEFAULT	CLKGEN DISABLED (Use External) DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	DISABLE PCI ROM BOOT DEFAULT	L, H = LPC ROM L, L = FWH ROM

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTCCLK

DEBUG STRAPS



	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23	PCI_AD30 PCI_AD29
PULL HIGH	USE LONG RESET (DEFAULT)	USE PCI PLL (DEFAULT)	USE ACPI BCLK (DEFAULT)	USE IDE PLL (DEFAULT)	USE DEFAULT PCIE STRAPS (DEFAULT)	Reserved (DEFAULT)	Reserved
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	Reserved	

Note: SB700 has 15K internal PU FOR PCI_AD[30:23]

緯創資通 Wistron Corporation
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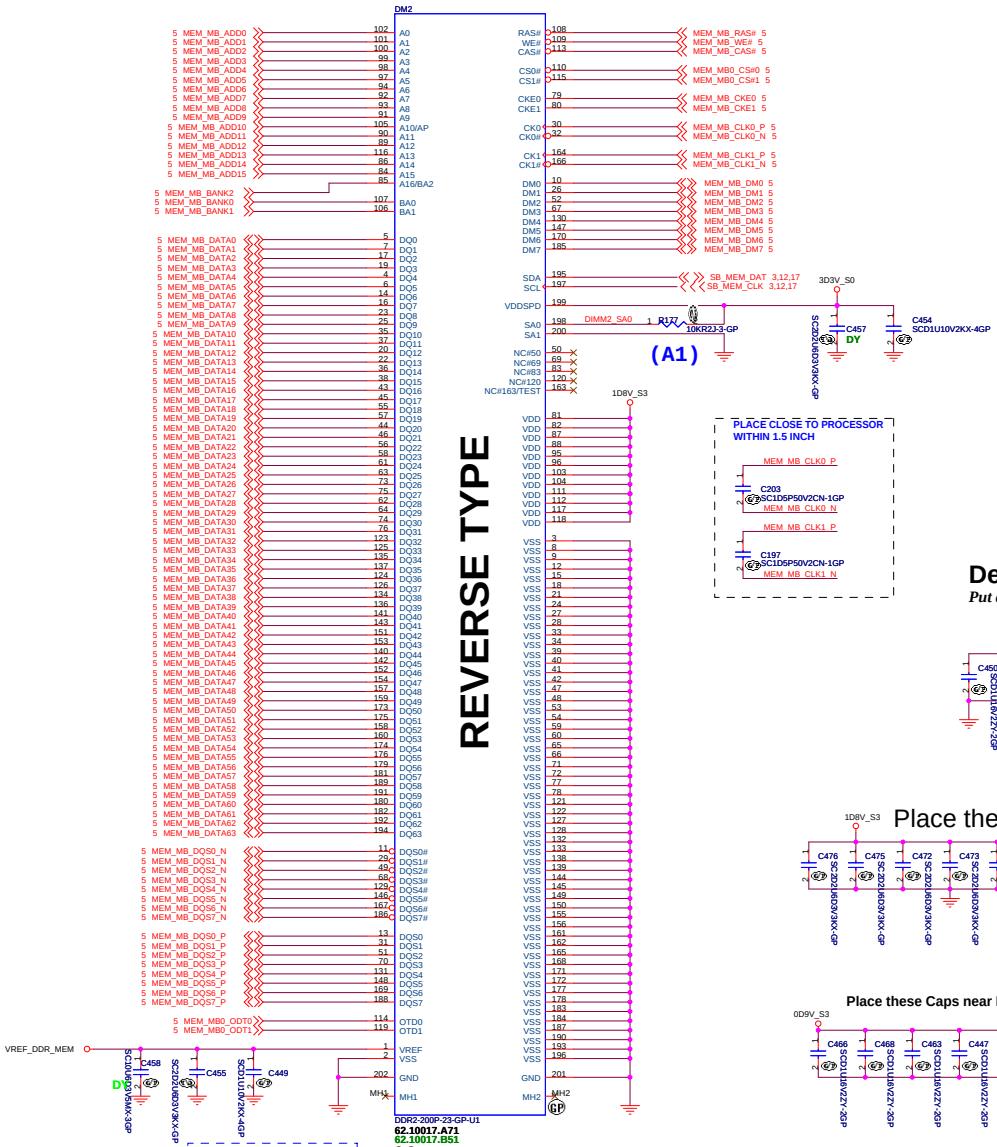
Title: SB700 (5 of 5)

Size: | Document Number: SJV50-PU | Rev: -1

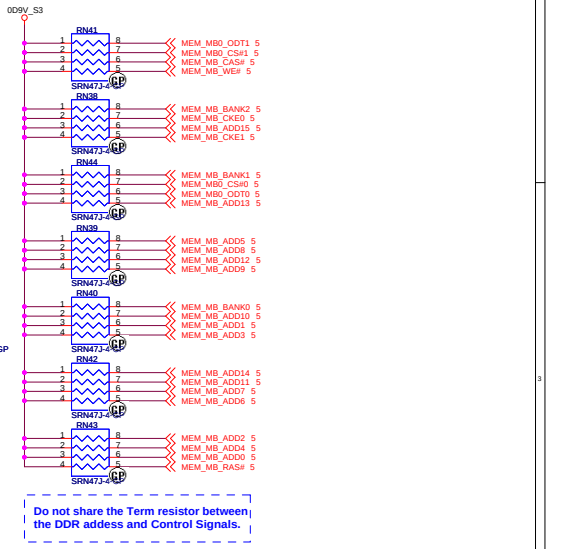
Date: Wednesday, February 25, 2009 Sheet 15 of 59

DDR2 SOCKET_2 (9.2mm)



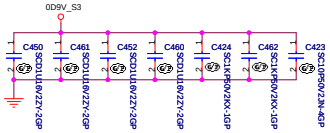
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor



Decoupling Capacitor

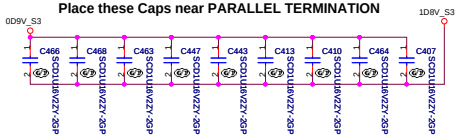
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM2

Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION



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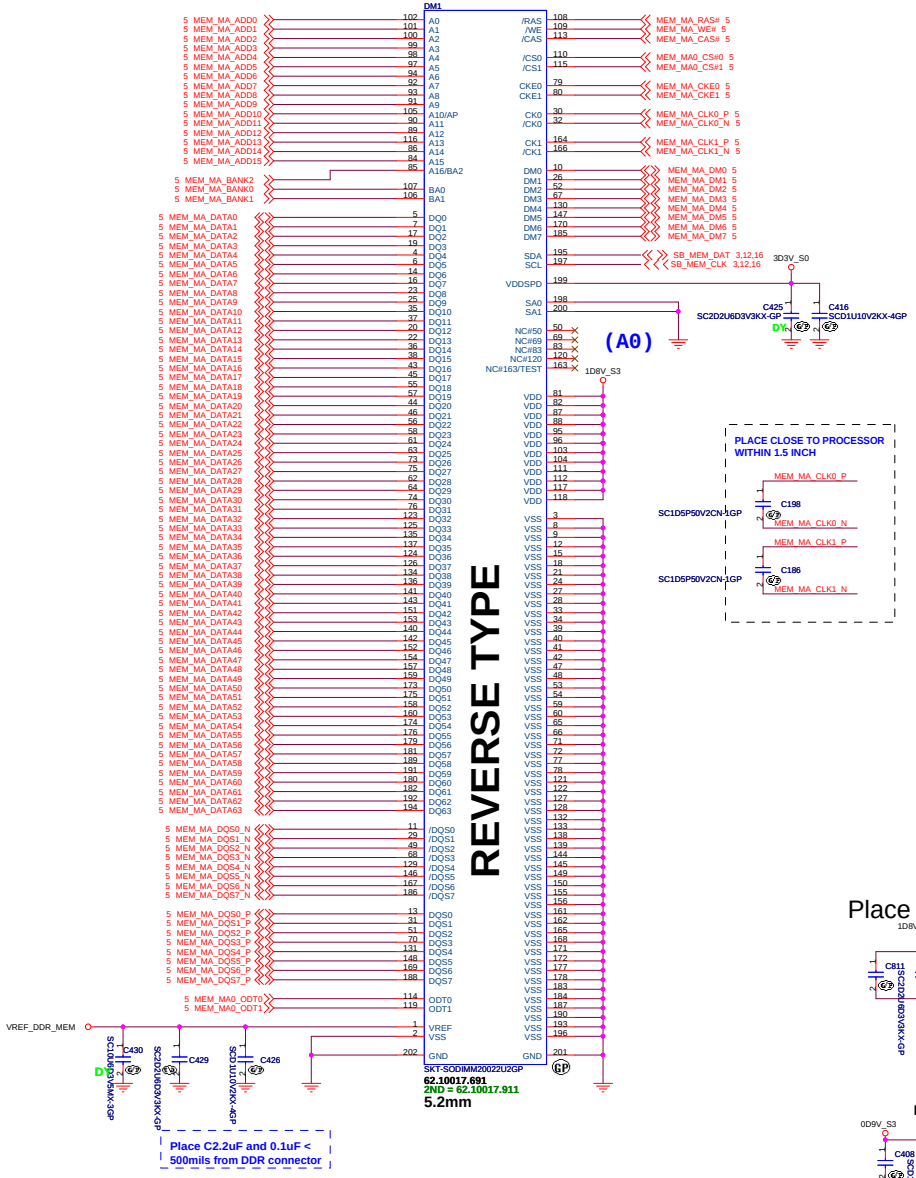
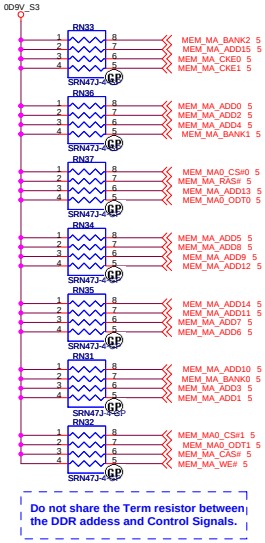
Title: DDR2 Socket_2		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 16 of 59	

DDR2 SOCKET_1 (5.2mm)



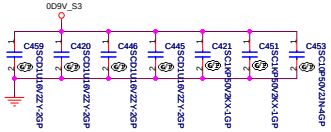
PARALLEL TERMINATION

Put decap near power(0.9V) and pull-up resistor

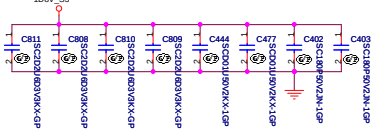


Decoupling Capacitor

Put decap near power(0.9V) and pull-up resistor

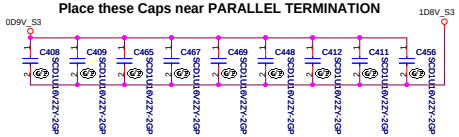


Place these Caps near DM2

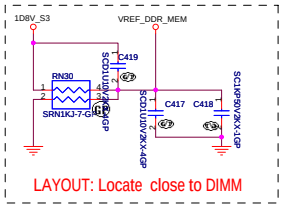


Layout Note:
Place one cap close to every 2 pullup resistors terminated to 0D9V_S3

Place these Caps near PARALLEL TERMINATION

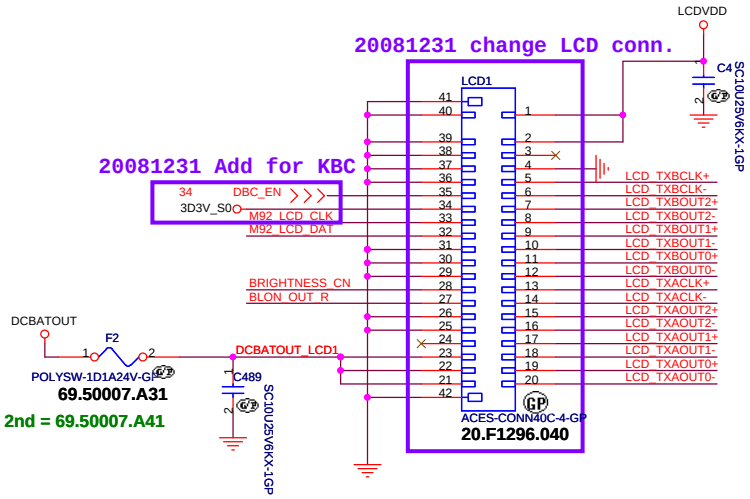


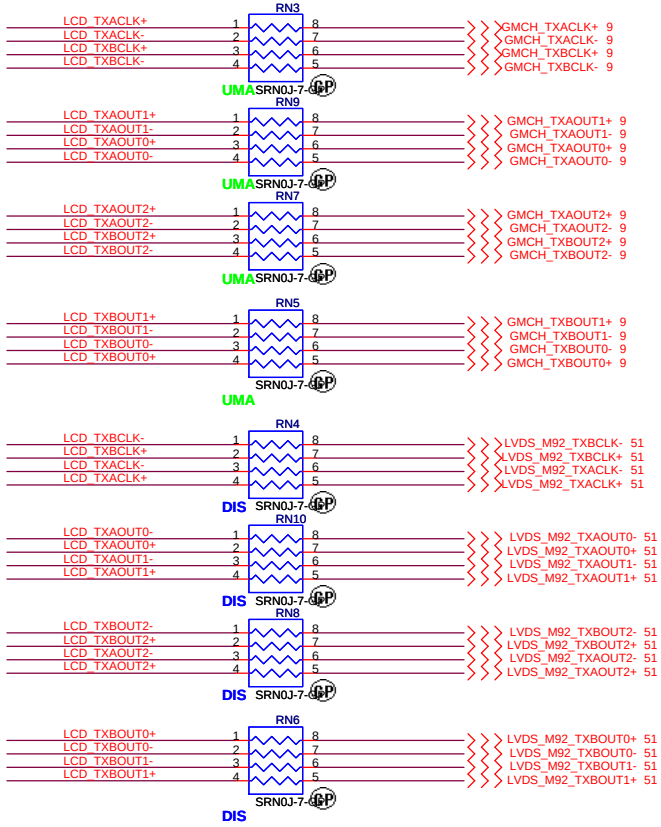
DDR_VREF

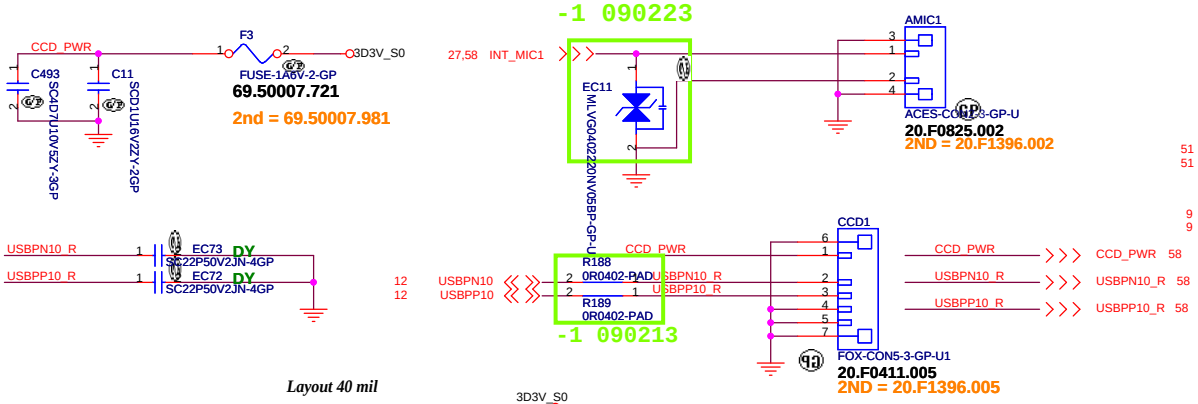


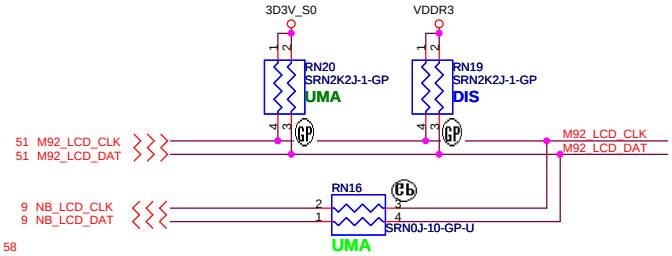
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	*DDR2 Socket_1*	
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 17 of 59	

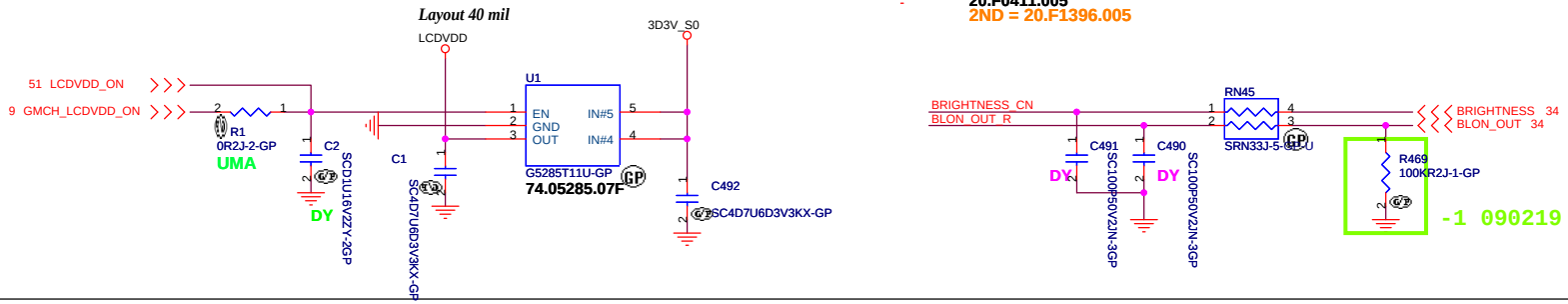
LCD/CCD CONN











SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: LED & LCD CONN / CCD

Size	Document Number	Rev
	SJV50-PU	-1

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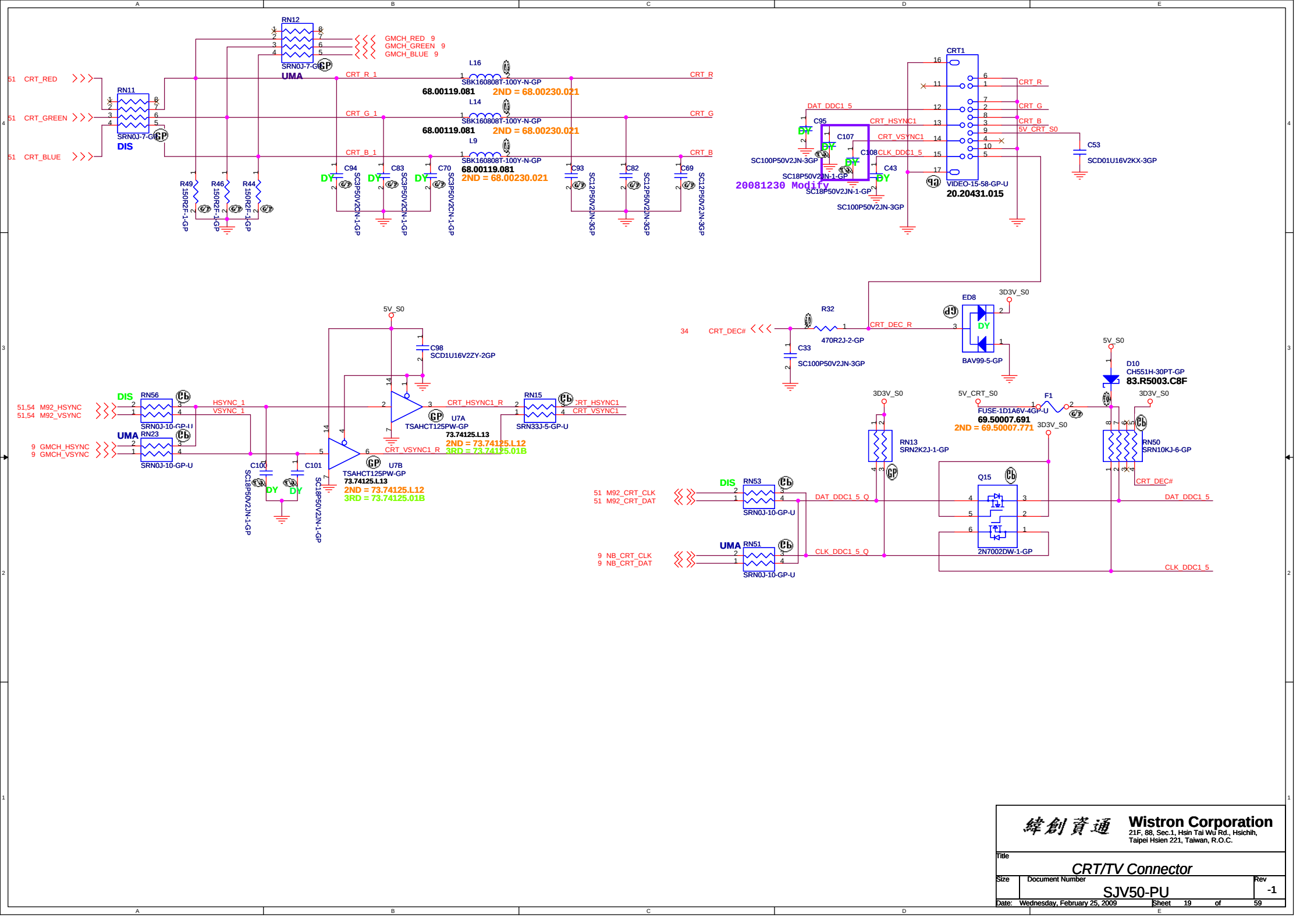
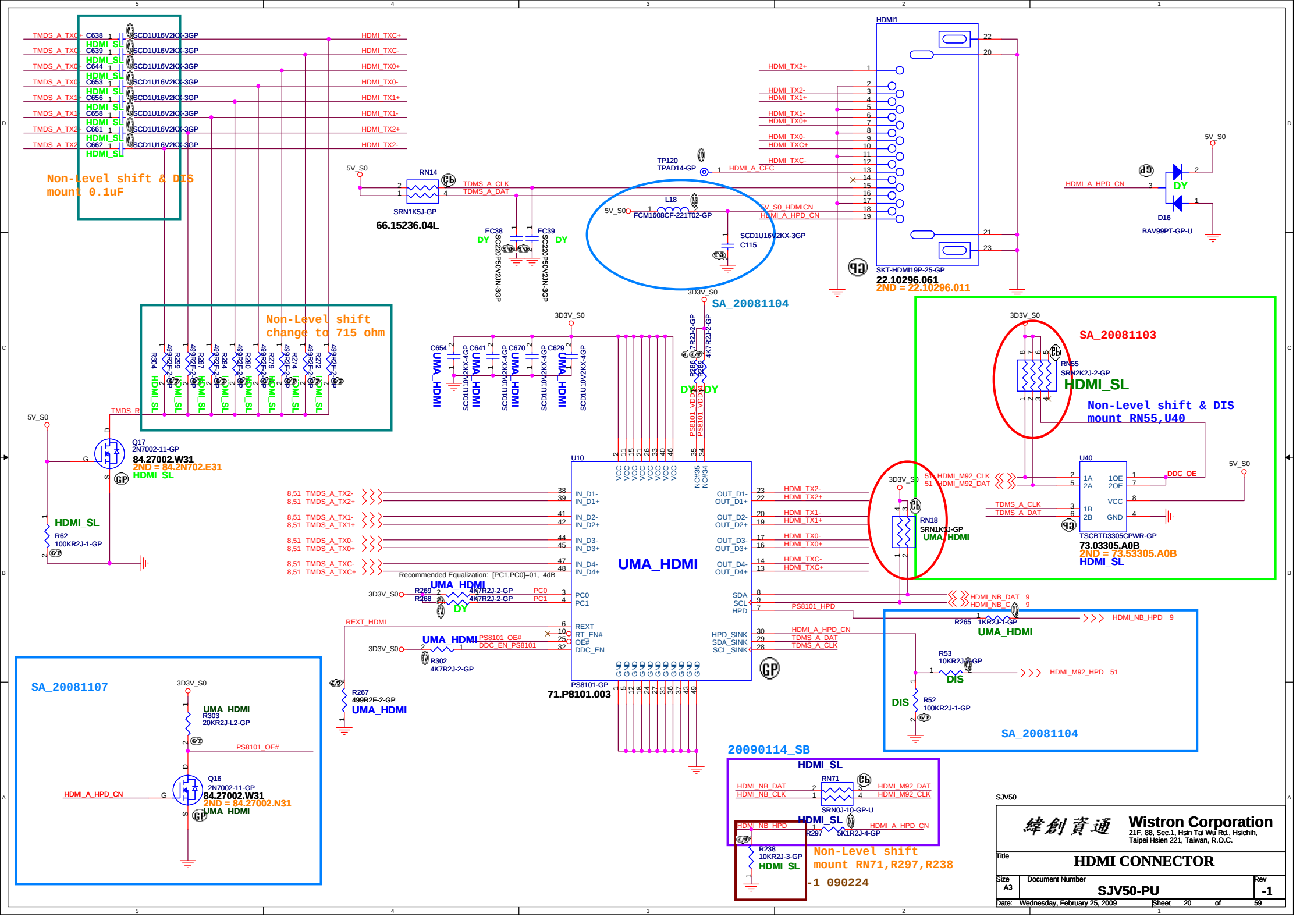
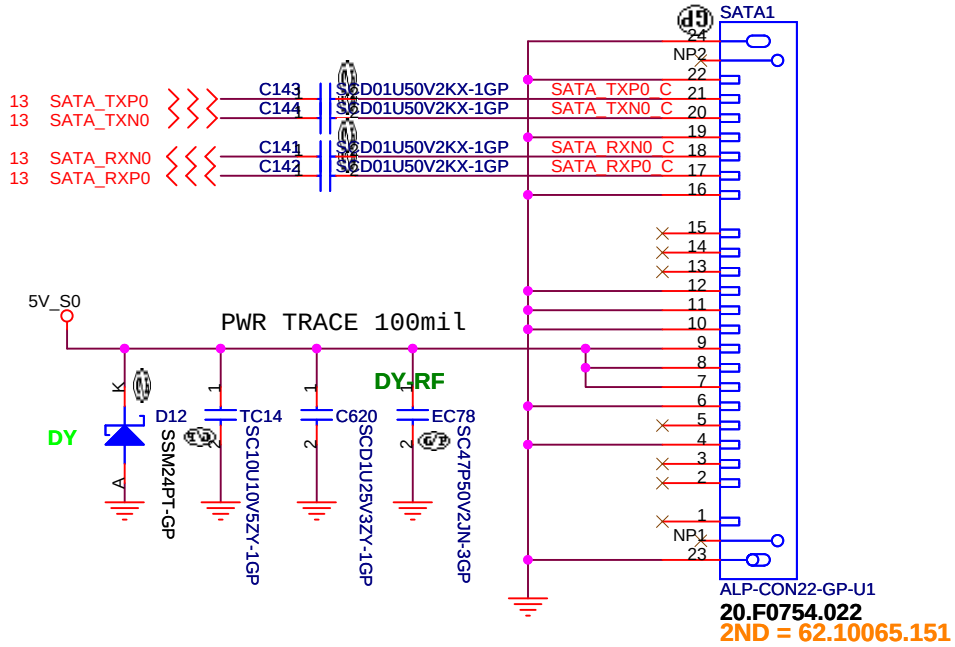


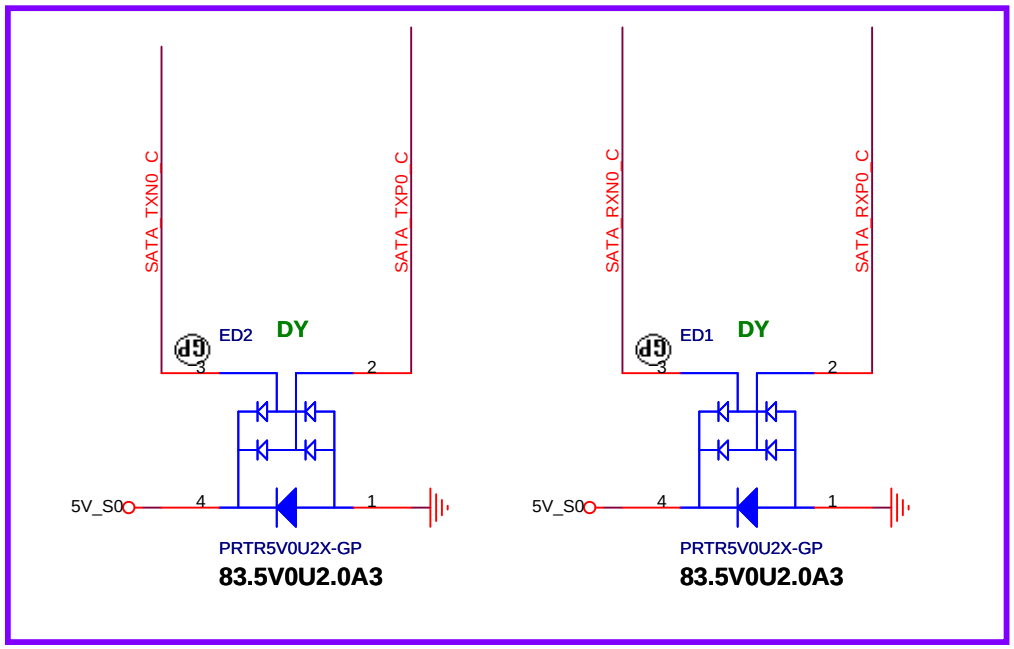
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*CRT/TV Connector*	
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 19 of 59	


Non-Level shift & DIS mount 0.1uF
Non-Level shift change to 715 ohm
SA_20081104
SA_20081103
Non-Level shift & DIS mount RN55,U40
SA_20081107
SA_20081104
20090114_SB
Non-Level shift mount RN71,R297,R238
HDMI_SL
UMA_HDMI
DY
DIS
Recommended Equalization: [PC1,PC0]=01, 4dB
66.15236.04L
22.10296.061
2ND = 22.10296.011
84.27002.W31
2ND = 84.2N702.E31
73.03305.A0B
2ND = 73.53305.A0B
71.P8101.003
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
HDMI CONNECTOR
SJV50-PU
-1
Wednesday, February 25, 2009
20 of 59

SATA HDD Connector





SA_20081112

SJV50

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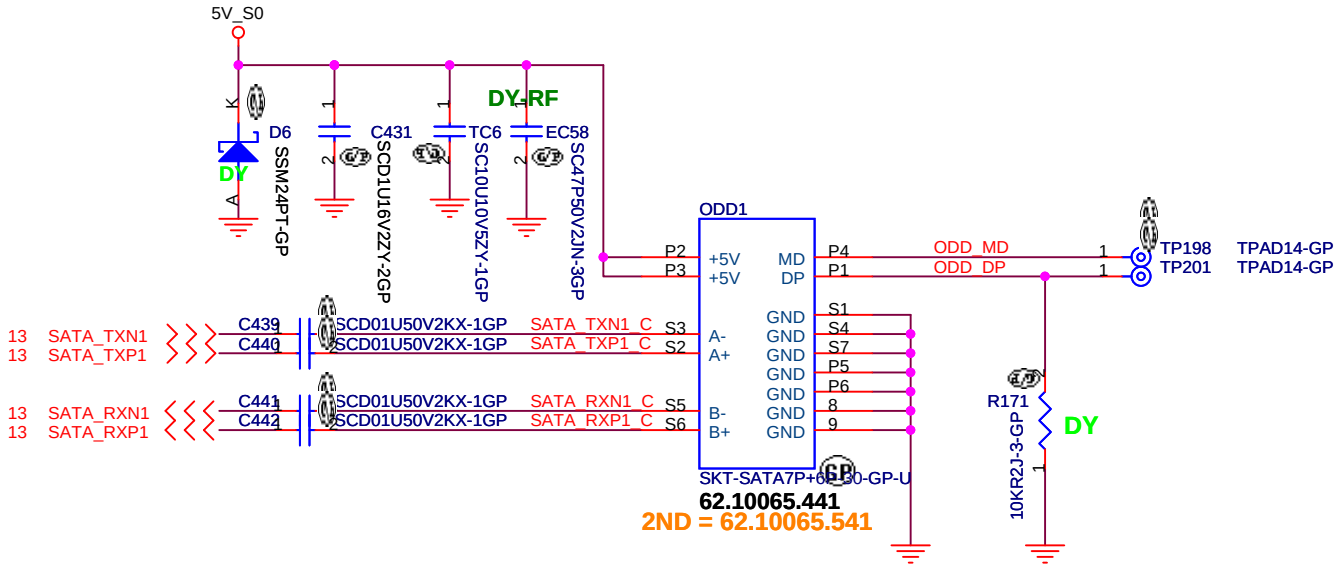
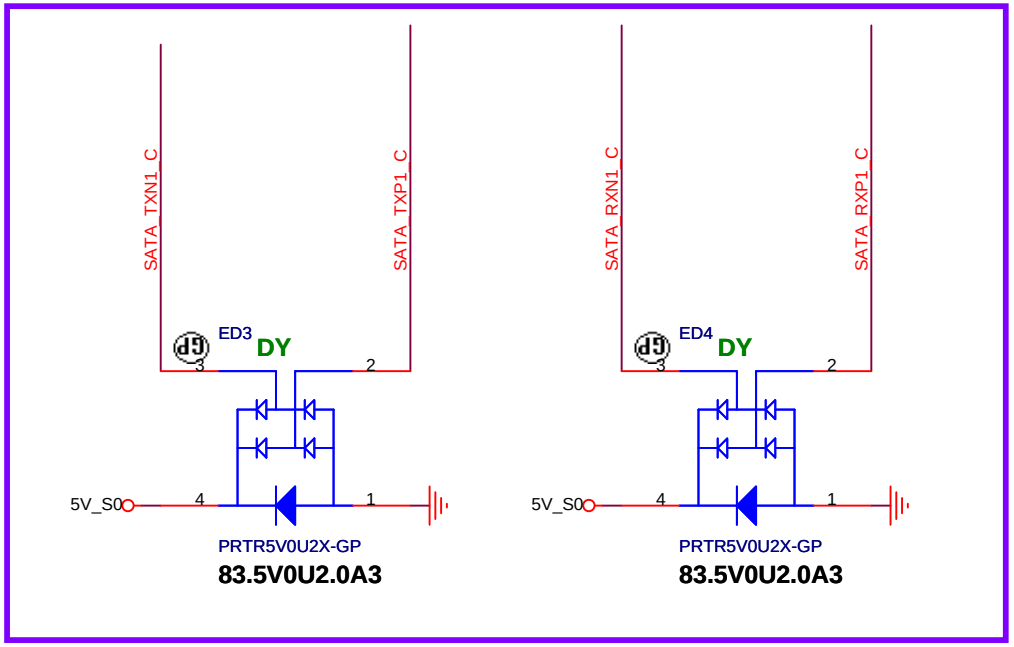
Taipei Hsien 221, Taiwan, R.O.C.

Title	***HDD***	
Size	Document Number **SJV50-PU**	Rev -1
Date: Wednesday, February 25, 2009	Sheet 21 of 59	

SATA ODD Connector





SA_20081112

SJV50

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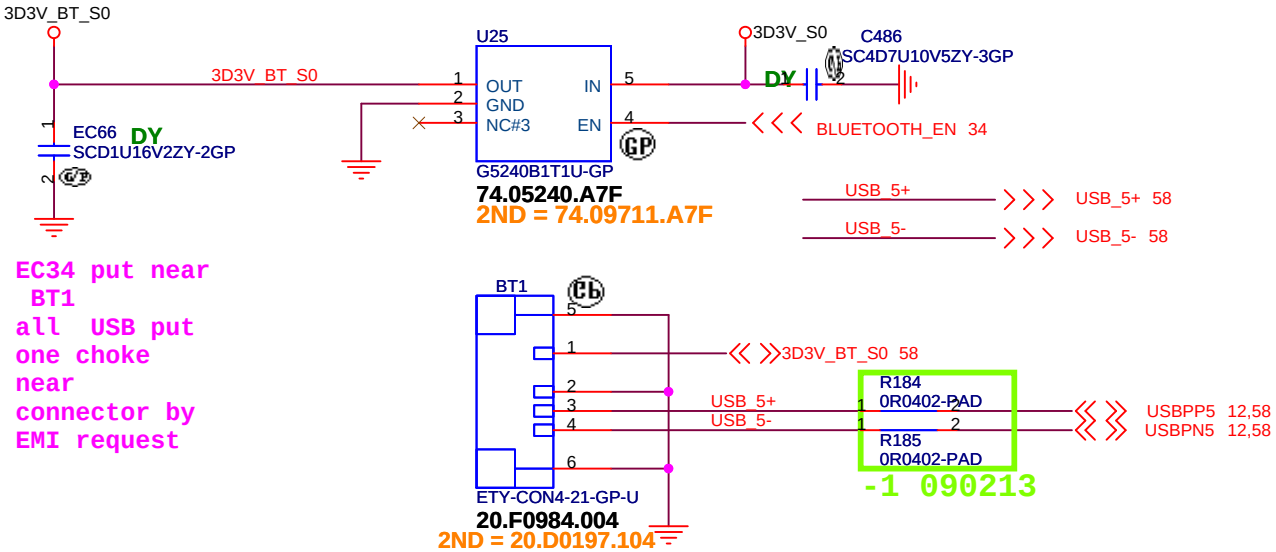
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ODD

Size | Document Number: SJV50-PU | Rev: -1

Date: Wednesday, February 25, 2009 | Sheet 22 of 59

BLUETOOTH MODULE



SJV50

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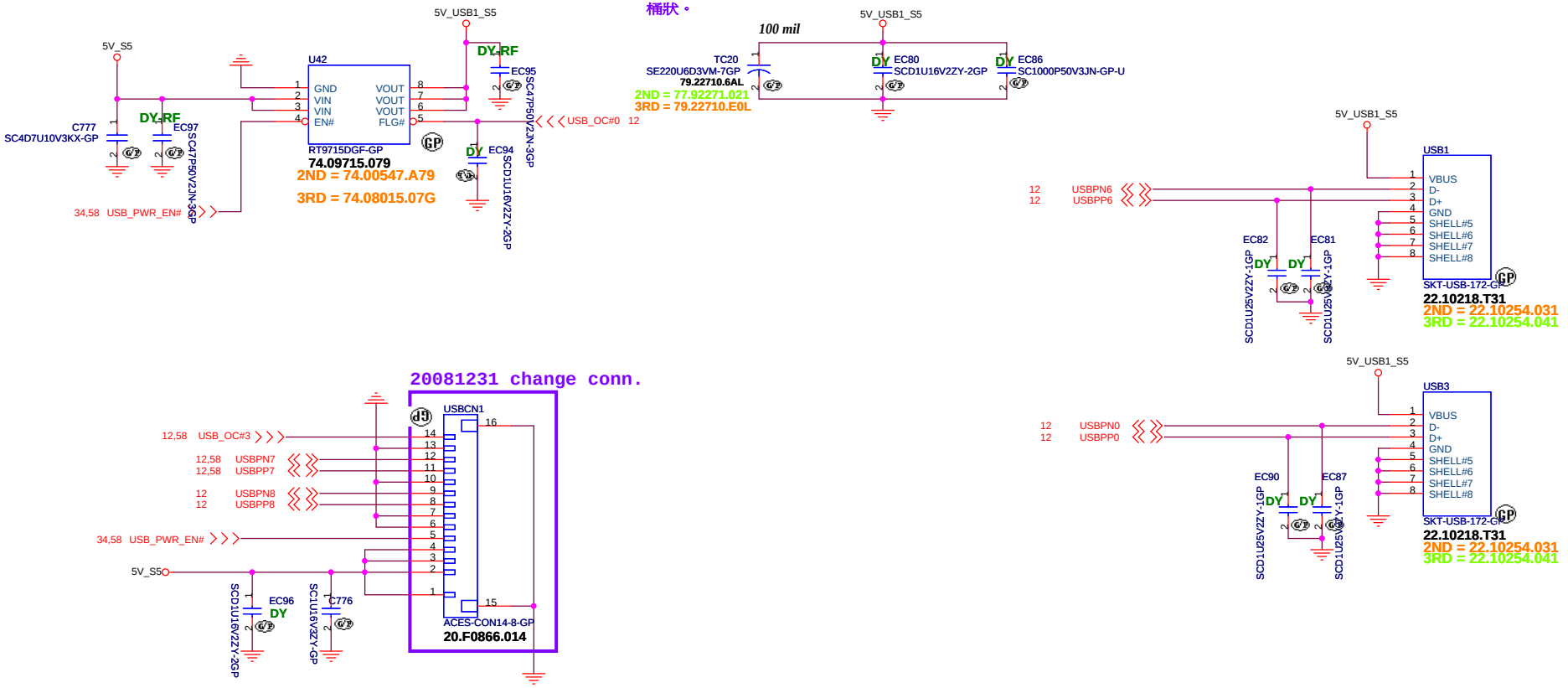
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***BLUETOOTH***

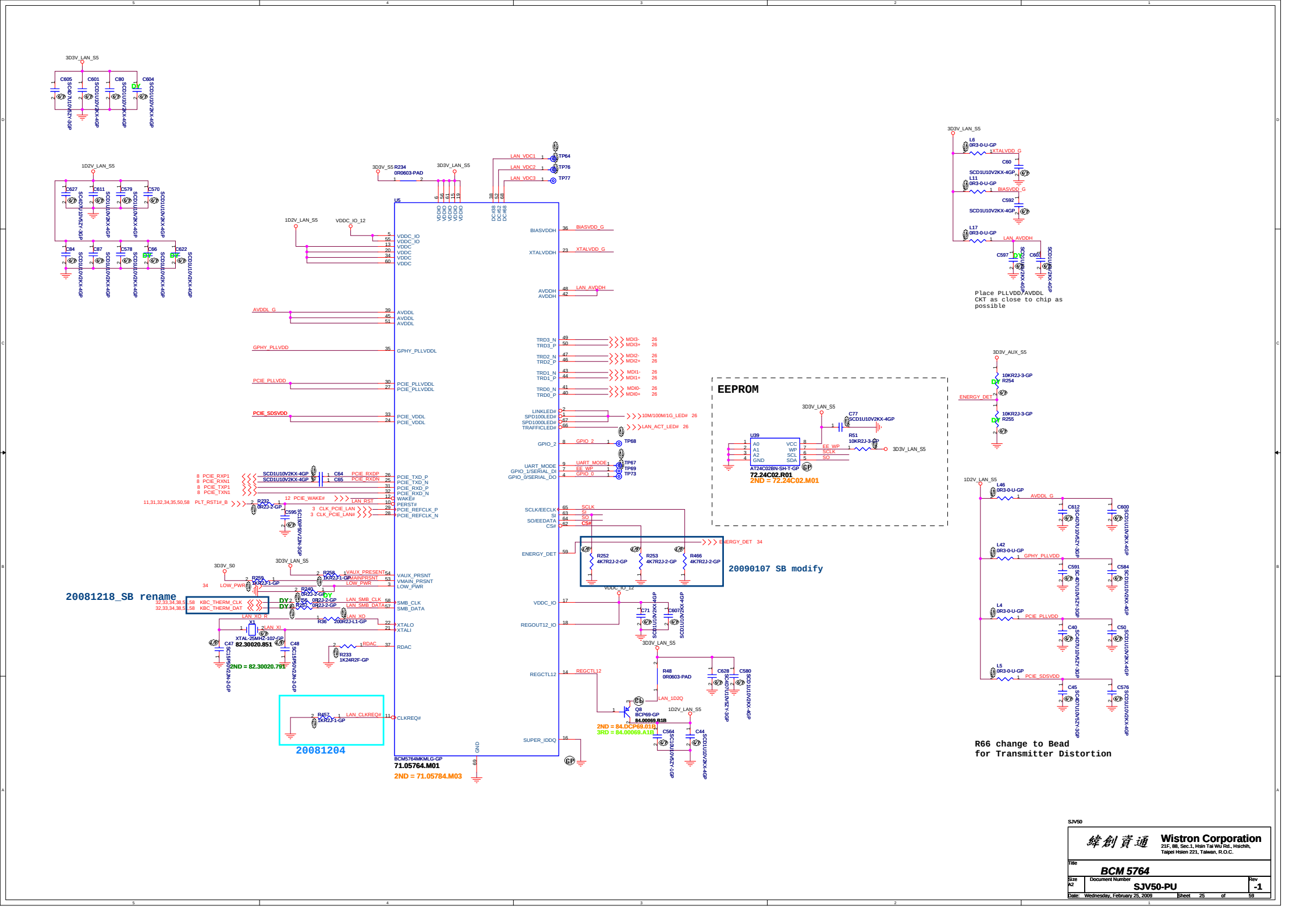
Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 23 of 59

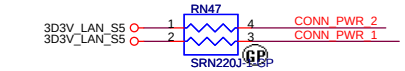


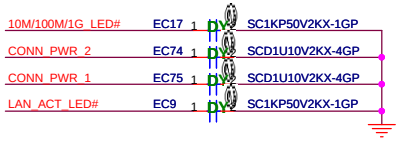
PD UMA

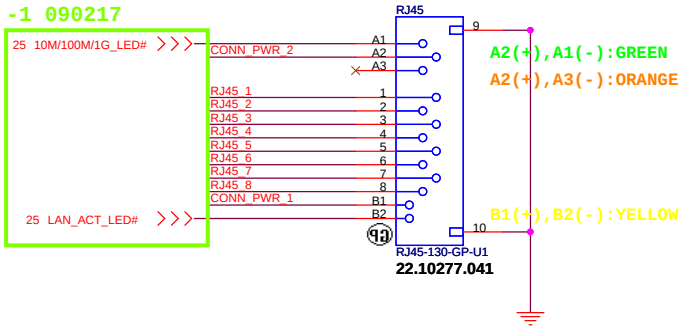
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: **USB Connector**		
Size	Document Number: **SJV50-PU**	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 24 of 59	


3D3V_LAN_S5
1D2V_LAN_S5
U5
BCM5764MKMLG-GP
71.05764.M01
2ND = 71.05784.M03
EEPROM
U39
AT24C02BN-SH-T-GP
72.24C02.R01
2ND = 72.24C02.M01
20081218_SB rename
20090107 SB modify
20081204
Place PLLVDD/AVDDL CKT as close to chip as possible
R66 change to Bead for Transmitter Distortion
2ND = 82.30020.781
2ND = 84.DCP69.01B
3RD = 84.00069.A1B
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
BCM 5764
SJV50-PU
-1
Wednesday, February 25, 2009

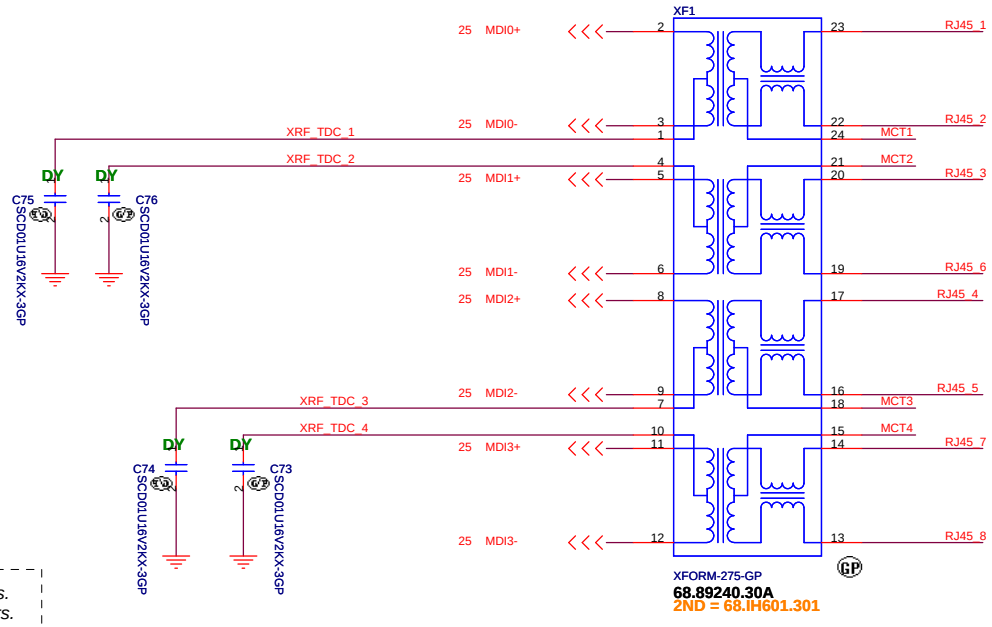
LAN Connector



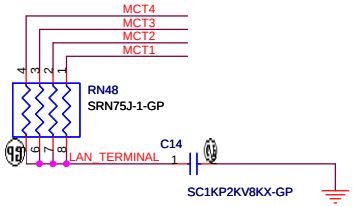




GIGA Lan Transformer



1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.



10/100 LAN Transformer	RJ45 PIN
TD+ --> TX+	RJ45-1
TD- --> TX-	RJ45-2
RD+ --> RX+	RJ45-3
RD- --> RX-	RJ45-6

SJV50

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Title: **LAN Connector**

Size	Document Number	Rev
A3	SJV50-PU	-1

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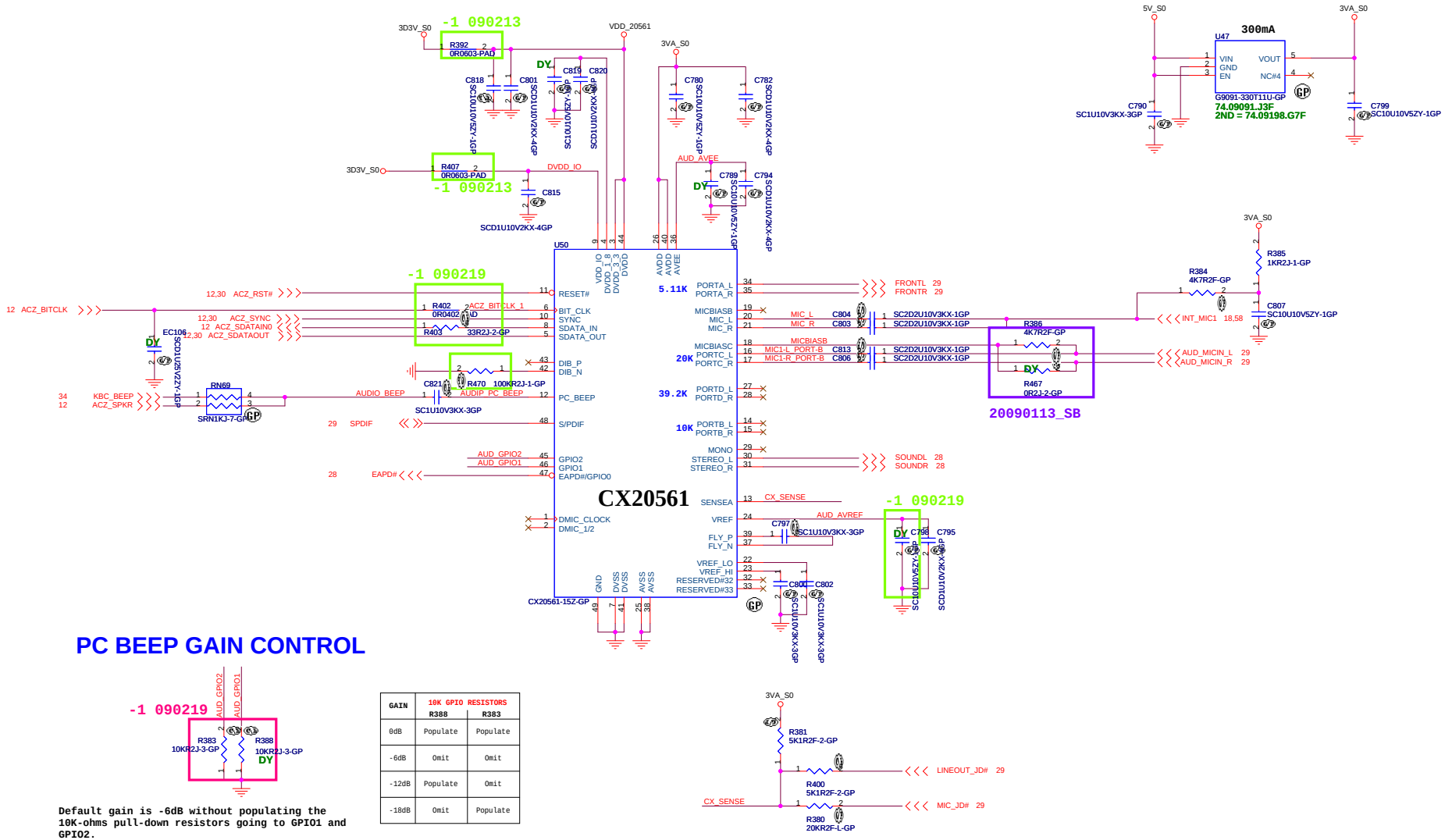

PC BEEP GAIN CONTROL

GAIN	10K GPIO RESISTORS	
	R388	R383
0dB	Populate	Populate
-6dB	Omit	Omit
-12dB	Populate	Omit
-18dB	Omit	Populate

Default gain is -6dB without populating the 10K-ohms pull-down resistors going to GPIO1 and GPIO2.

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Title: AZALIA CODEC - CX20561

Size | Document Number: SJV50-PU | Rev: -1

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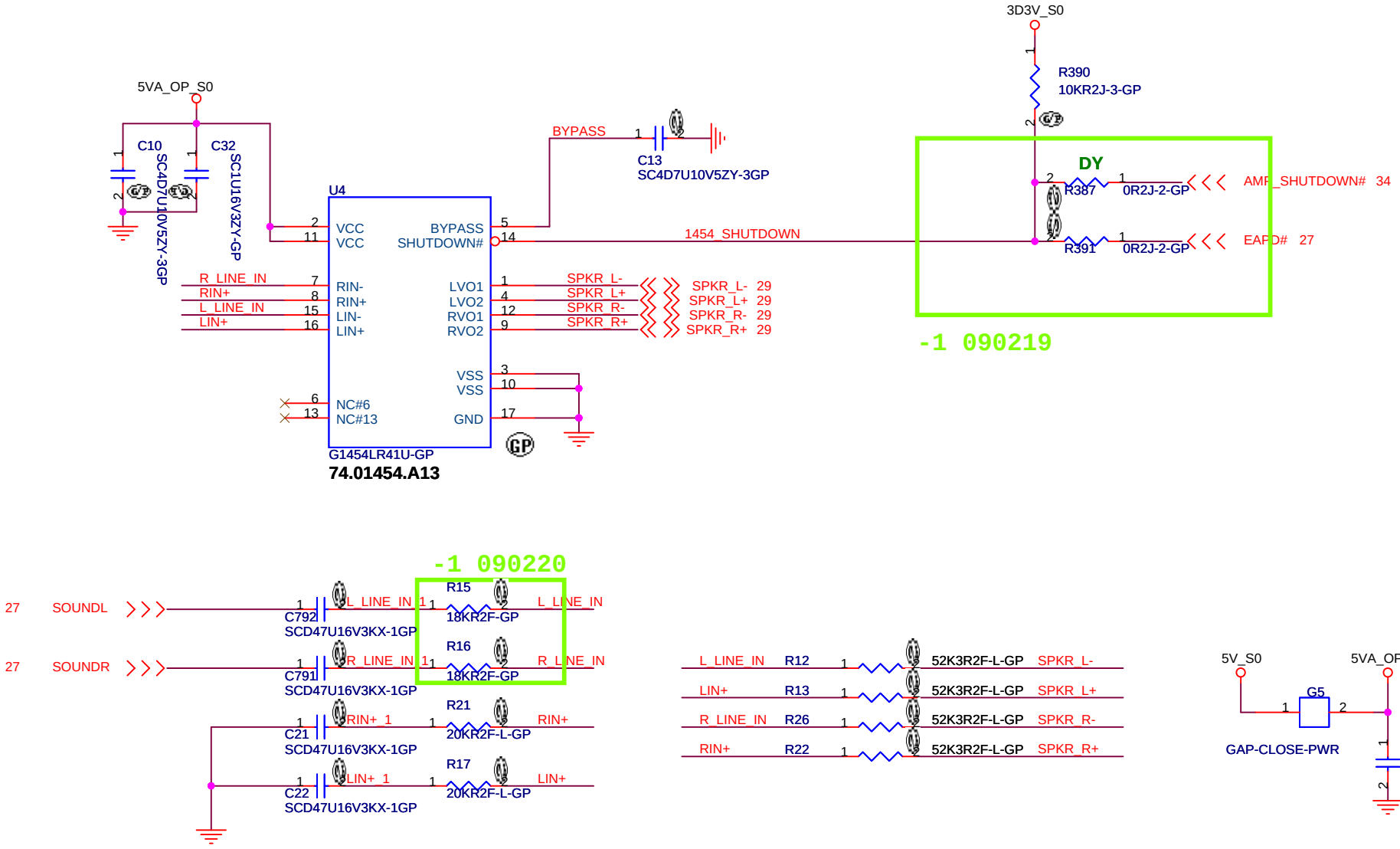
AUDIO OP AMPLIFIER



PD UMA

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: AUDIO AMP (G1454)		
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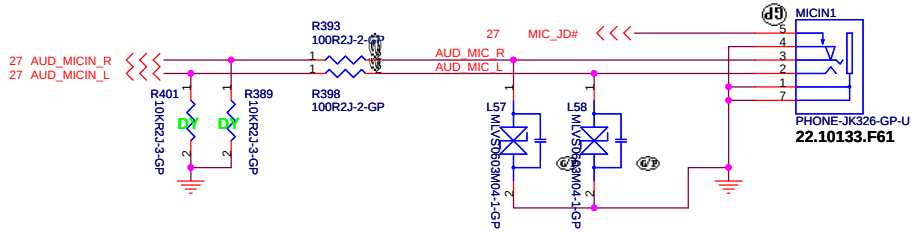
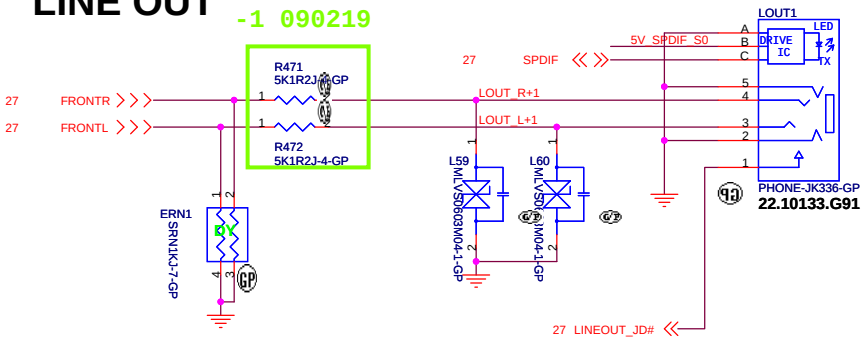
Date: Wednesday, February 25, 2009	Sheet 28 of 59	

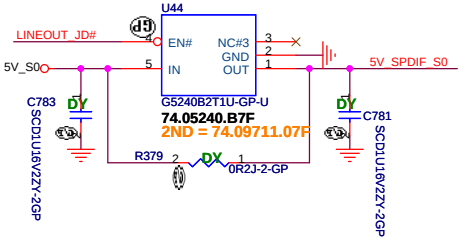
MIC IN



LINE OUT

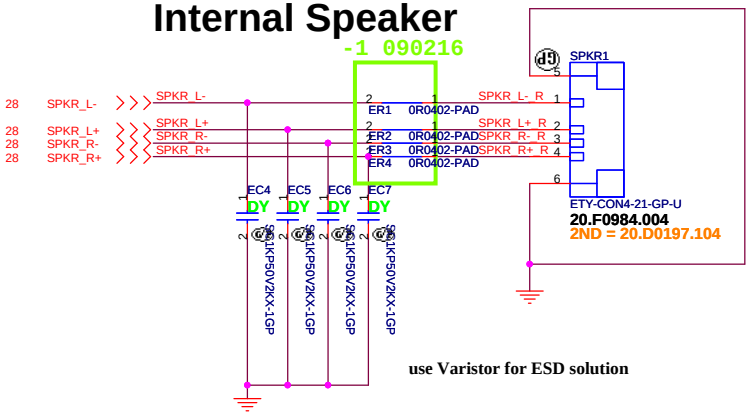
-1 090219





Internal Speaker

-1 090216



use Varistor for ESD solution

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Audio Jack**

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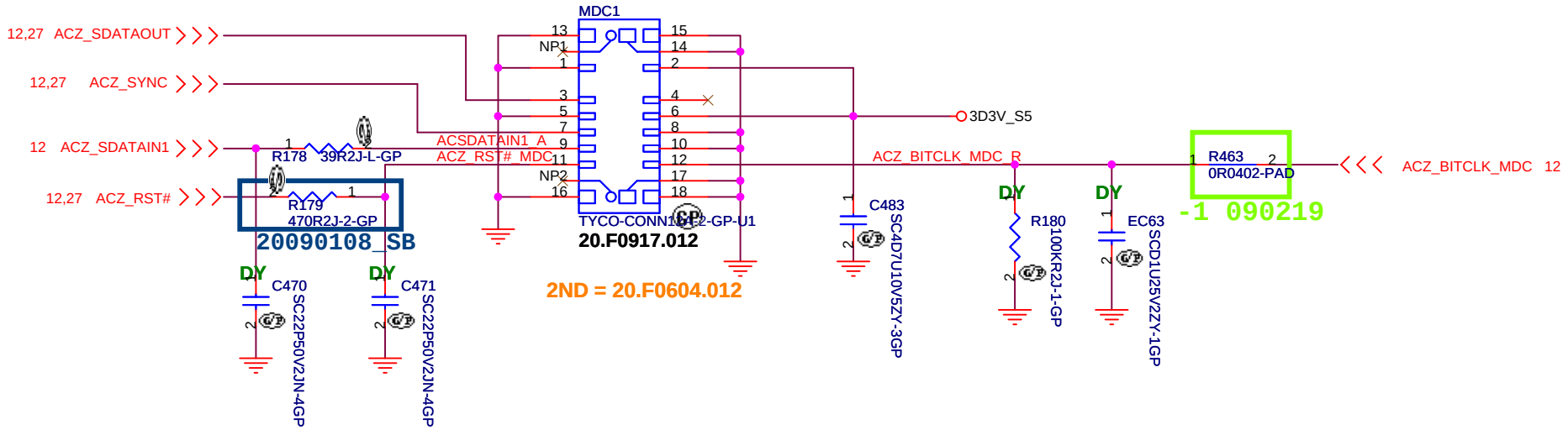
MDC 1.5 CONN



SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***USB Connector***

Size	Document Number	Rev
	SJV50-PU	-1

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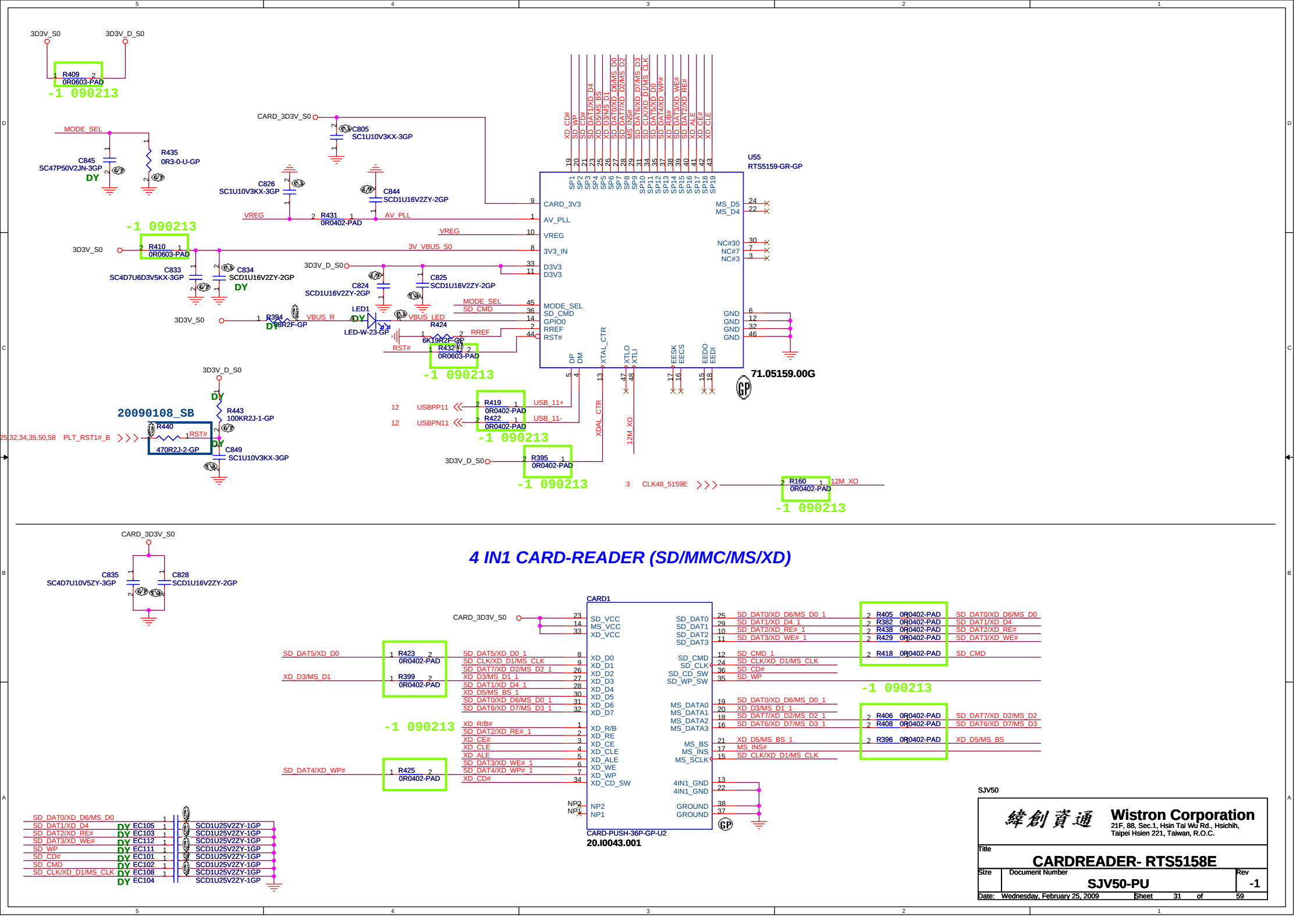
4 IN1 CARD-READER (SD/MMC/MS/XD)
U55
RTS5159-GR-GP
71.05159.00G
CARD1
CARD-PUSH-36P-GP-U2
20.I0043.001
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
CARDREADER- RTS5158E
SJV50-PU
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-1
Date: Wednesday, February 25, 2009
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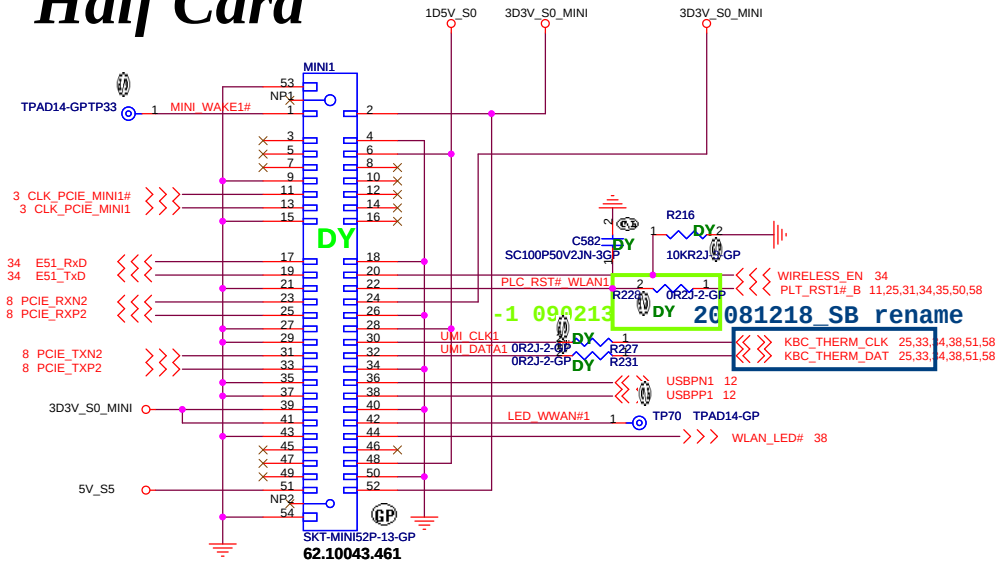
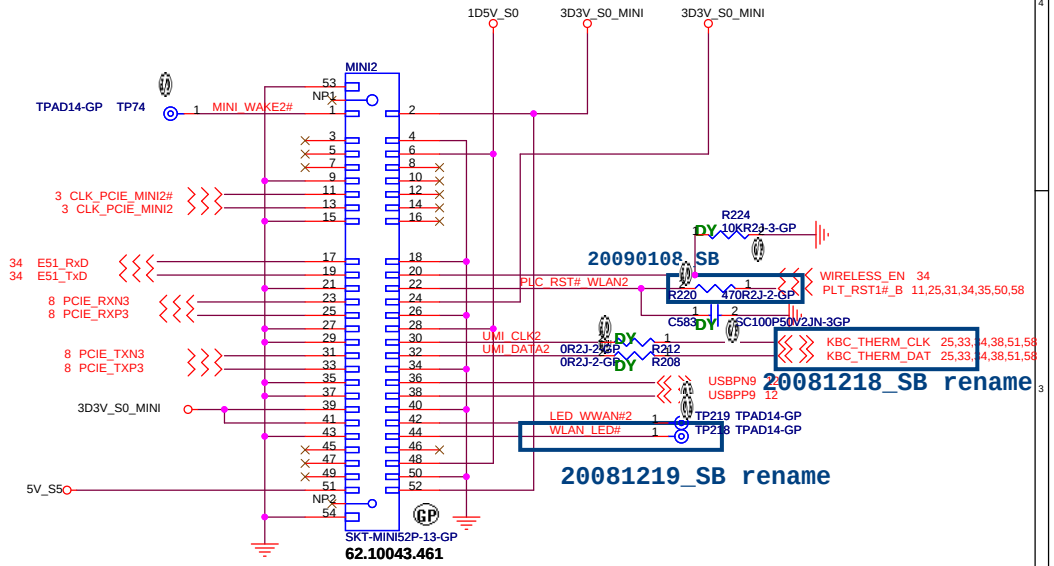
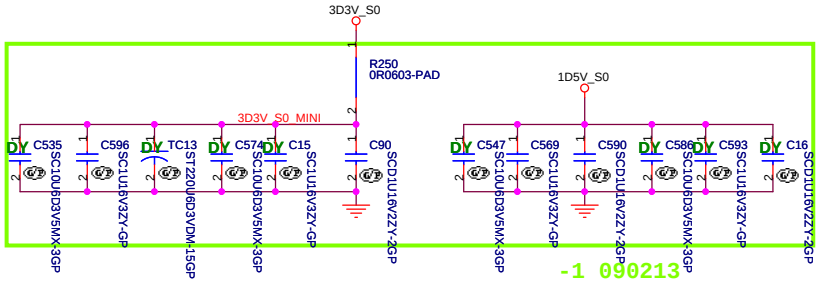
Mini Card Connector

Half Card

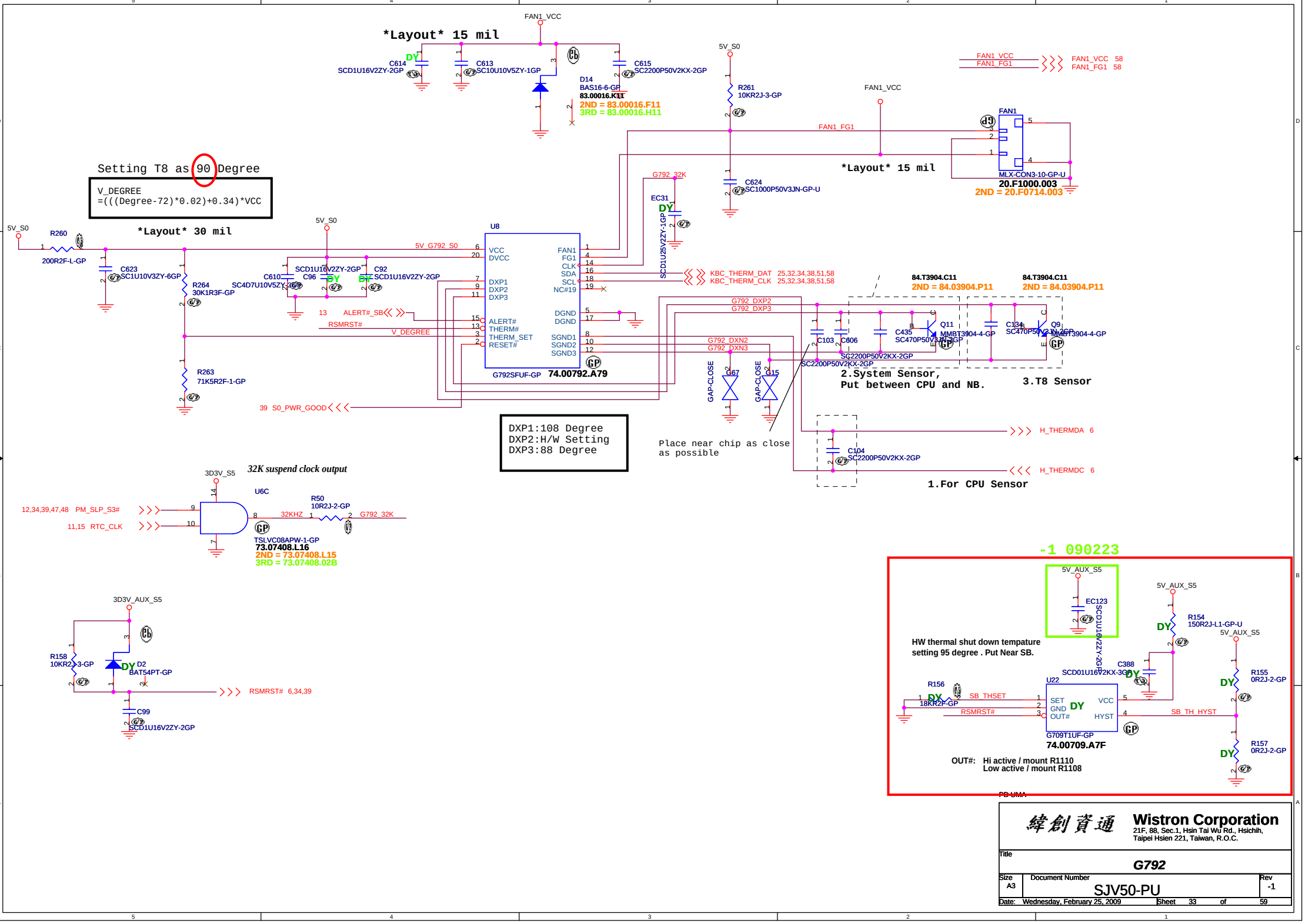






SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: MINI CARD		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 32 of 59	


Layout 15 mil
FAN1_VCC
C614 SCD1U16V2ZY-2GP
C613 SC10U10V5ZY-1GP
C615 SC2200P50V2KX-2GP
D14 BAS16-6-GP
83.00016.K11
2ND = 83.00016.F11
3RD = 83.00016.H11
5V_S0
R261 10KR2J-3-GP
FAN1_VCC 58
FAN1_FG1 58
FAN1_FG1
FAN1
MLX-CON3-10-GP-U
20.F1000.003
2ND = 20.F0714.003
C624 SC1000P50V3JN-GP-U
Setting T8 as 90 Degree
V_DEGREE
=(((Degree-72)*0.02)+0.34)*VCC
Layout 30 mil
R260 200R2F-L-GP
C623 SC1U10V3ZY-6GP
R264 30K1R3F-GP
R263 71K5R2F-1-GP
C610 SCD1U16V2ZY-2GP
C96 SC4D7U10V5ZY-1GP
C92 SCD1U16V2ZY-2GP
5V_G792_S0
U8
VCC
DVCC
DXP1
DXP2
DXP3
ALERT#
THERM#
THERM_SET
RESET#
FAN1
FG1
CLK
SDA
SCL
NC#19
DGND
DGND
SGND1
SGND2
SGND3
G792SFUF-GP
74.00792.A79
G792_32K
EC31 SCD1U25V2ZY-1GP
KBC_THERM_DAT 25,32,34,38,51,58
KBC_THERM_CLK 25,32,34,38,51,58
13 ALERT#_SB
RSMRST#
V_DEGREE
39 S0_PWR_GOOD
G792_DXP2
G792_DXP3
G792_DXN2
G792_DXN3
GAP-CLOSE
G67
C15
C103
C606
C435 SC470P50V2JN-2GP
Q11 MMBT3904-4-GP
C134 SC470P50V2JN-2GP
Q9 MMBT3904-4-GP
84.T3904.C11
2ND = 84.03904.P11
SC2200P50V2KX-2GP
2.System Sensor,
Put between CPU and NB.
3.T8 Sensor
DXP1:108 Degree
DXP2:H/W Setting
DXP3:88 Degree
Place near chip as close as possible
C104 SC2200P50V2KX-2GP
H_THERMDA 6
H_THERMDC 6
1.For CPU Sensor
3D3V_S5
32K suspend clock output
U6C
R50 10R2J-2-GP
12,34,39,47,48 PM_SLP_S3#
11,15 RTC_CLK
32KHZ
G792_32K
TSLVC08APW-1-GP
73.07408.L16
2ND = 73.07408.L15
3RD = 73.07408.02B
3D3V_AUX_S5
R158 10KR2J-3-GP
D2 BAT54PT-GP
RSMRST# 6,34,39
C99 SCD1U16V2ZY-2GP
-1 090223
5V_AUX_S5
EC123 SCD01U16V2KX-3GP
HW thermal shut down tempature setting 95 degree . Put Near SB.
R156 18KR2F-GP
SB_THSET
RSMRST#
U22
SET
GND
OUT#
VCC
HYST
G709T1UF-GP
74.00709.A7F
SB_TH_HYST
R154 150R2J-L1-GP-U
C388 SCD01U16V2KX-3GP
R155 0R2J-2-GP
R157 0R2J-2-GP
OUT#: Hi active / mount R1110
Low active / mount R1108
PB UMA
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
G792
Size A3
Document Number
SJV50-PU
Rev -1
Date: Wednesday, February 25, 2009
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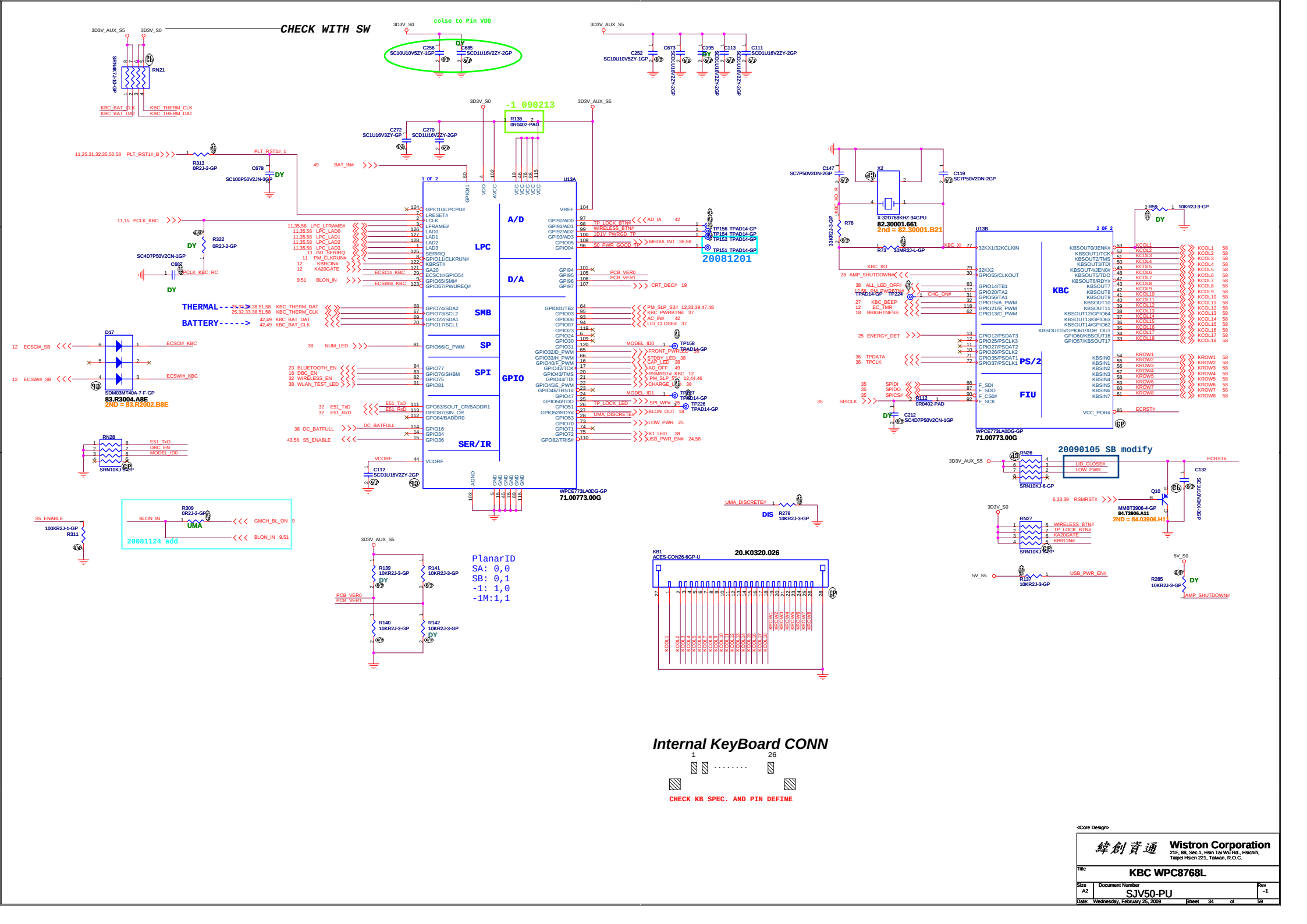
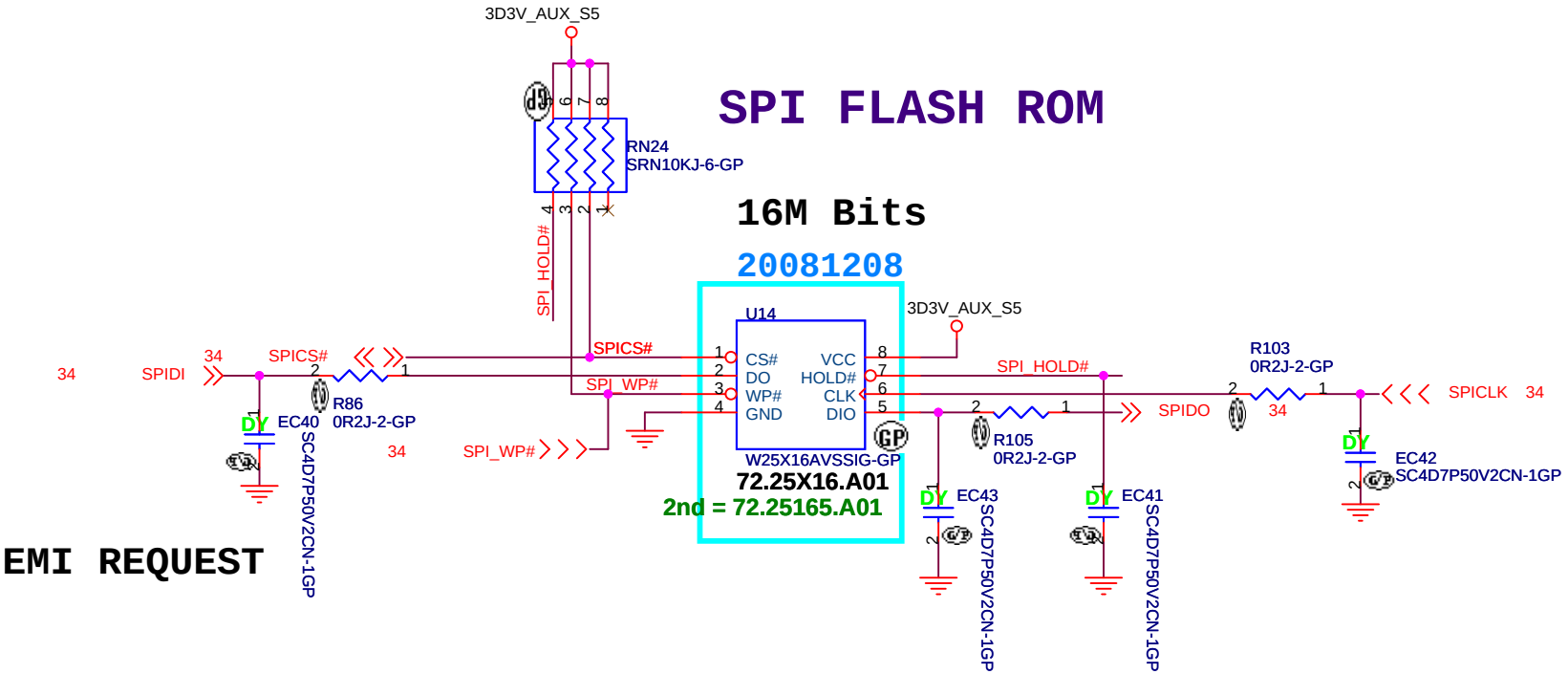
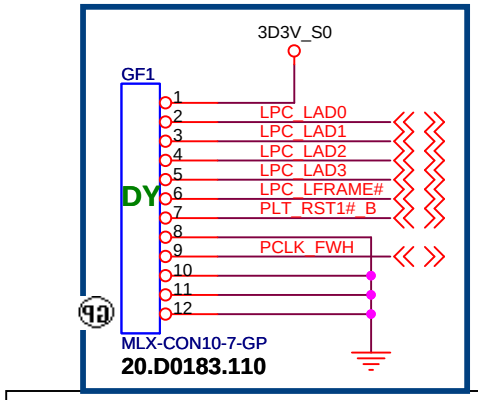

CHECK WITH SW
colse to Pin VDD
-1 090213
U13A
WPCE773LA0DG-GP
71.00773.00G
A/D
LPC
D/A
SMB
SP
SPI
GPIO
SER/IR
THERMAL-------> 25,32,33,38,51,58 KBC_THERM_DAT 25,32,33,38,51,58 KBC_THERM_CLK
BATTERY-----> 42,49 KBC_BAT_DAT 42,49 KBC_BAT_CLK
20081201
83.R3004.A8E
2ND = 83.R2002.B8E
82.30001.661
2nd = 82.30001.B21
71.00773.00G
20090105 SB modify
20081124 add
PlanarID
SA: 0,0
SB: 0,1
-1: 1,0
-1M:1,1
20.K0320.026
Internal KeyBoard CONN
CHECK KB SPEC. AND PIN DEFINE
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
KBC WPC8768L
SJV50-PU
Wednesday, February 25, 2009

SPI FLASH ROM



Connector FOR DEBUG BOARD

20081219



LPC_LAD0 11,34,58
LPC_LAD1 11,34,58
LPC_LAD2 11,34,58
LPC_LAD3 11,34,58
LPC_LFRAME# 11,34,58
PLT_RST1#_B 11,25,31,32,34,50,58

PCLK_FWH 11,15,58

Boot Device must have ID[3:0] = 0000
Has internal pull-down resistors
All may be left floated
FPET7 Elec. P3-46

SJV50

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Title: BIOS		
Size: A4	Document Number: SJV50-PU	Rev: -1
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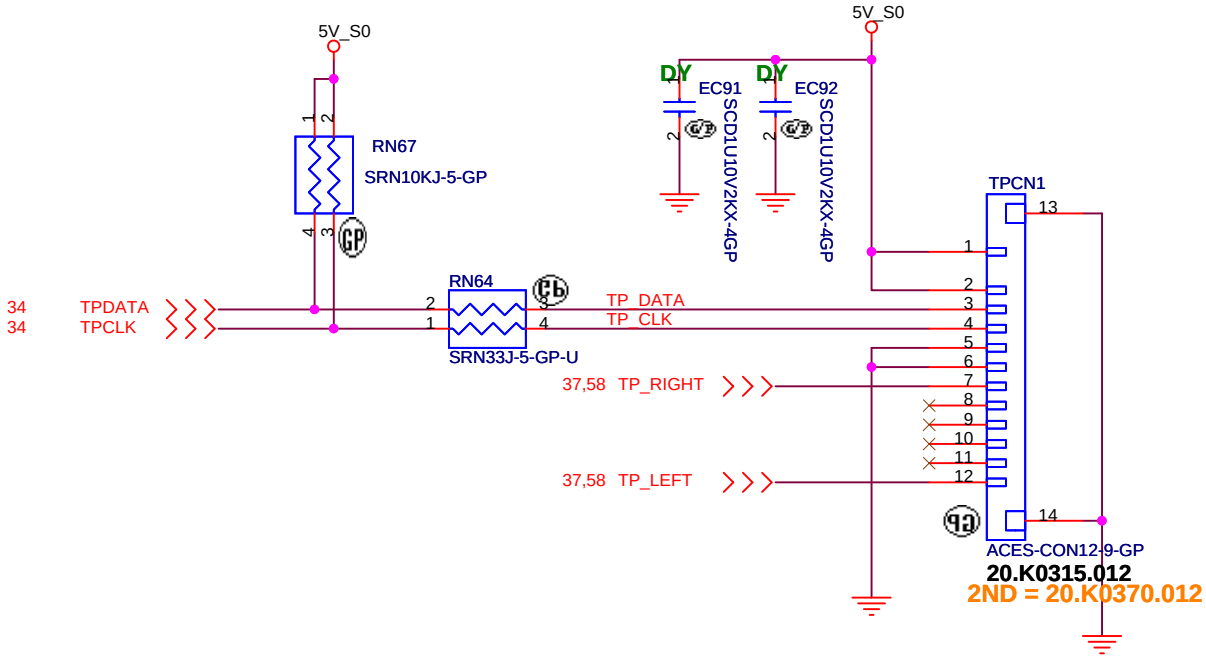
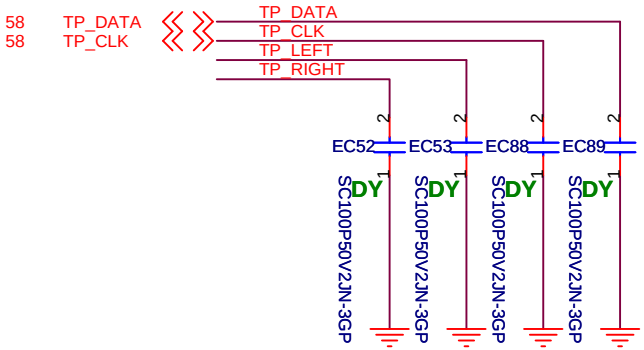
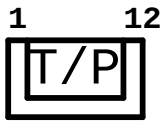
TOUCH PAD





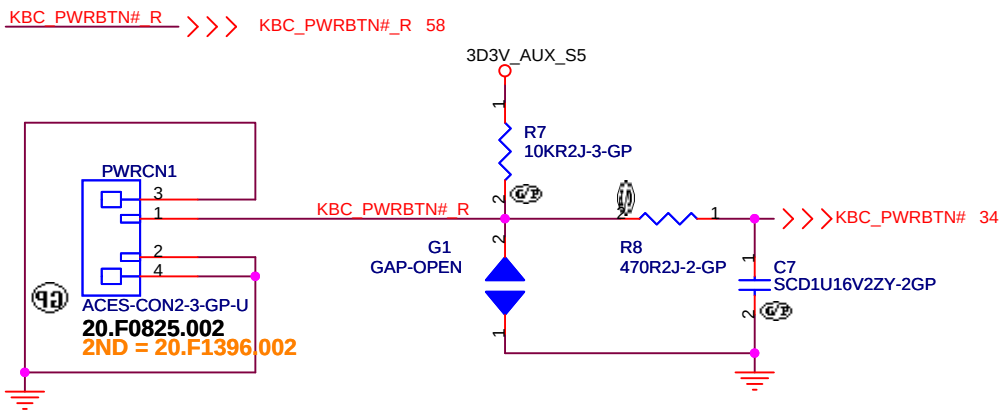


SJV50

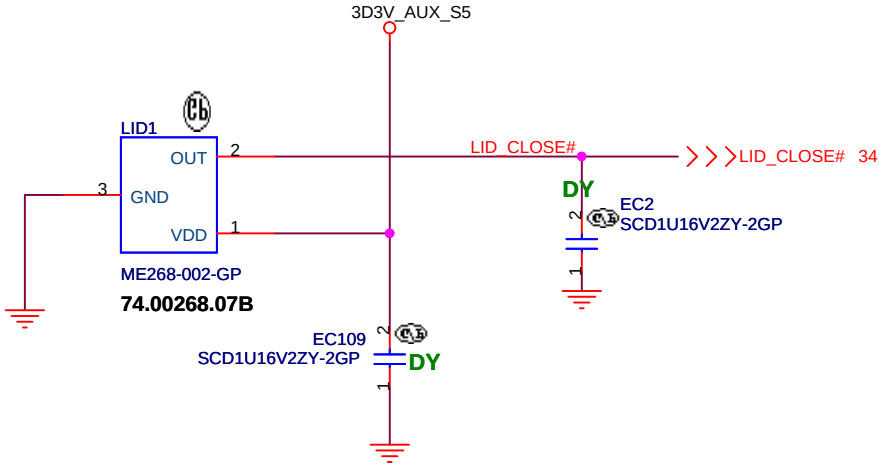
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***TouchPad***	
Size	Document Number **SJV50-PU**	Rev -1
Date: Wednesday, February 25, 2009	Sheet 36 of 59	

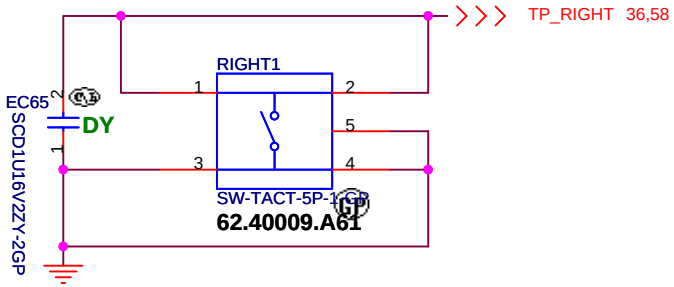
Power Button Board



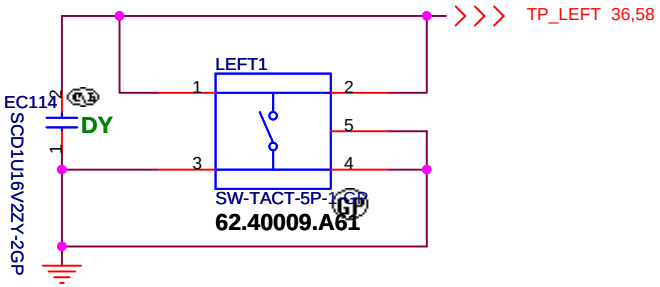
Cover Up Switch



RIGHT



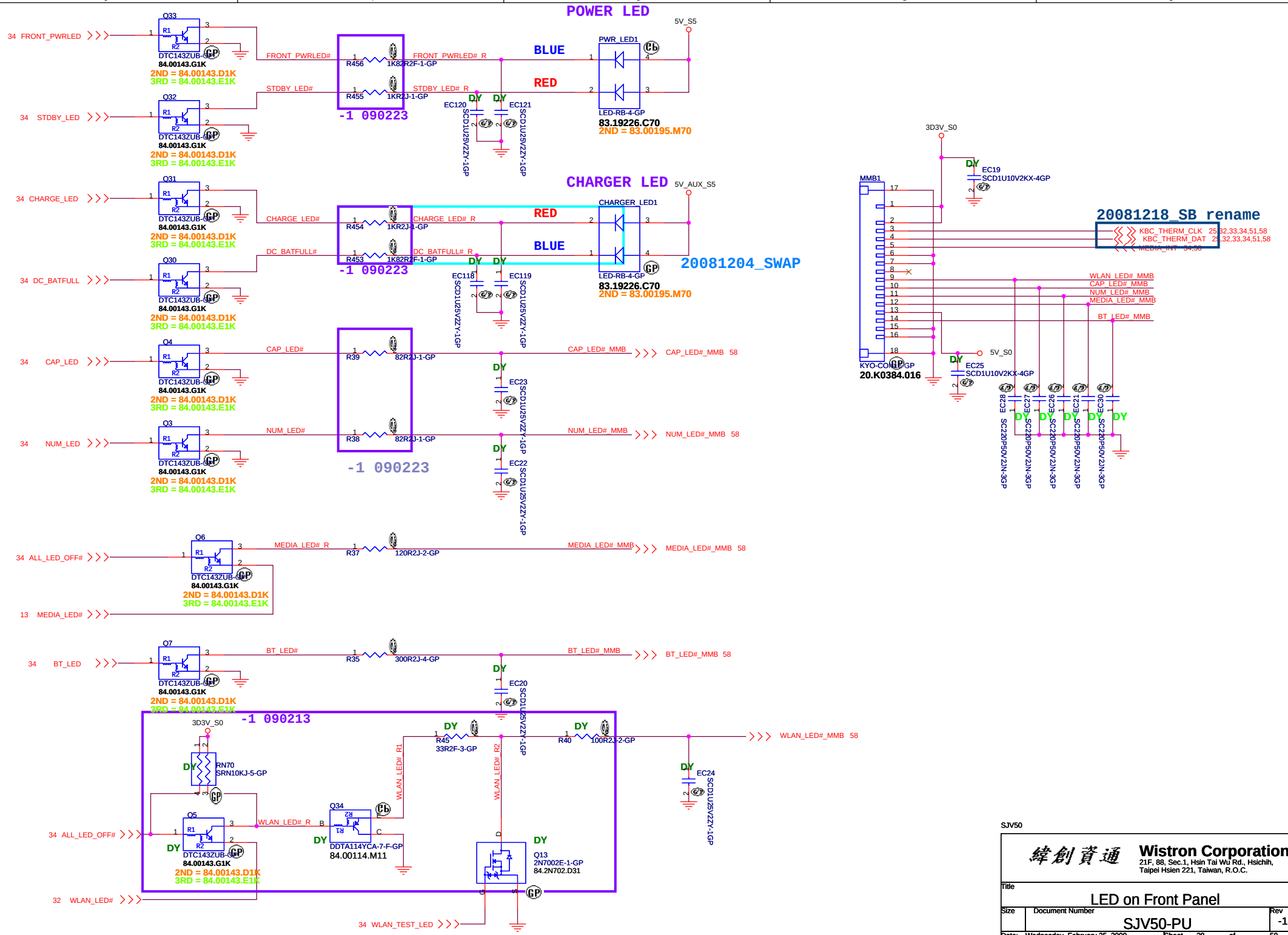
LEFT



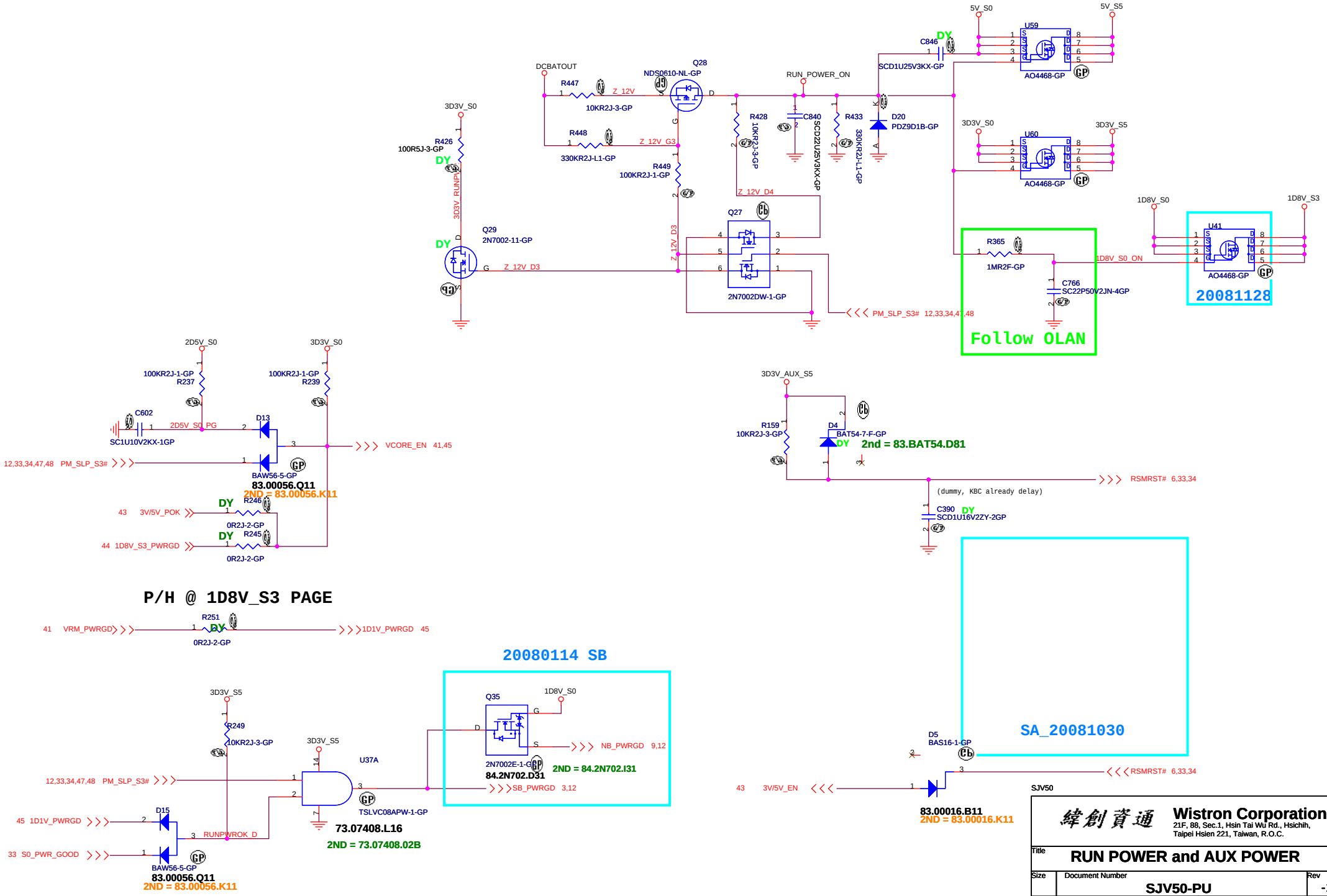
SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Switchs*		
Size	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 37 of 59	


POWER LED
CHARGER LED
20081204_SWAP
20081218_SB_rename
-1 090223
-1 090213
BLUE
RED
5V_S5
5V_AUX_S5
3D3V_S0
5V_S0
PWR_LED1
CHARGER_LED1
LED-RB-4-GP
83.19226.C70
2ND = 83.00195.M70
FRONT_PWRLED
STDBY_LED
CHARGE_LED
DC_BATFULL
CAP_LED
NUM_LED
ALL_LED_OFF#
MEDIA_LED#
BT_LED
WLAN_LED#
WLAN_TEST_LED
FRONT_PWRLED#
STDBY_LED#
CHARGE_LED#
DC_BATFULL#
CAP_LED#_MMB
NUM_LED#_MMB
MEDIA_LED#_MMB
BT_LED#_MMB
WLAN_LED#_MMB
KBC_THERM_CLK
KBC_THERM_DAT
WLAN_LED#_MMB
CAP_LED#_MMB
NUM_LED#_MMB
MEDIA_LED#_MMB
BT_LED#_MMB
DTC143ZUB-GP
84.00143.G1K
2ND = 84.00143.D1K
3RD = 84.00143.E1K
1K82R2F-1-GP
1KR2J-1-GP
82R2J-1-GP
120R2J-2-GP
300R2J-4-GP
33R2F-3-GP
100R2J-2-GP
SCD1U25V2ZY-1GP
SCD1U10V2KX-4GP
SCD1U10V2KX-3GP
SRN10KJ-5-GP
DDTA114YCA-7-F-GP
84.00114.M11
2N7002E-1-GP
84.2N702.D31
KYO-CONN-GP
20.K0384.016
SJV50
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
LED on Front Panel
SJV50-PU
Rev -1
Date: Wednesday, February 25, 2009
Sheet 38 of 59

Run Power



SJV50

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **RUN POWER and AUX POWER**

Size	Document Number	Rev
	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 39 of 59

CPU_CORE
ISL6264

VID0
VID1
VID2
VID3
VID4
VID5

VID Setting
VID0(I / 3.3V)
VID1(I / 3.3V)
VID2(I / 3.3V)
VID3(I / 3.3V)
VID4(I / 3.3V)
VID5(I / 3.3V)

Output Signal
VROK()

MAX8760_VRM

Output Power
VCC_CORE_PWR(O)

VCC_CORE_S0(Imax=35A)

VCORE_EN

Input Signal
EN (I / 3.3V)

COREFB
COREFB#

Voltage Sense
VSEN(I / Vcore)
RGND(I / Vcore)

DCBATOUT
5V_S0
3D3V_S0

Input Power
VCC(I)
VCC(I)
VCC(I)

TI TPS51125
3D3V/5V

DCBATOUT_51120
DCBATOUT_51120

Input Signal
51120_EN2 FOR 3.3V
51120_EN1 FOR 5.0V
VIN
VIN
REG5V_IN(I / 5V)

Output Signal
PGOUT(OD / 5V)

Pull High (3D3V)

Input Power

Output Power
5V(O)
3D3V(O)

5V_AUX_S5
3D3V_AUX_S5
5V_S5 (5.4A)
3D3V_S5 (4A)

1D5V_S0

3D3V_S0 → INPUT / OUT → 1D5V_S0

G957

1D2V_S5

3D3V_S5 → INPUT / OUT → 1D2V_S5

G9091

2D5V_S0

3D3V_S0 → INPUT / OUT → 2D5V_S0

G9091

0D9V_S3

5V_S5 → INPUT / OUT → 0D9V_S3

RT9026

Adapter

AD_OFF
AD_JK
5V_AUX_S5

Input Signal
(I)

Output Signal
(O)

AD_IN

Input Power
VCC(I)
VCC(I)

Output Power
VCC(O)

AD+

Charger_MAX8731

CHARGE_OFF
BT_TH
BAT+SENSE
BT_SCL_5
BT_SDA_5
FLASH_GPIO1
FLASH_GPIO2
AC_IN

AD+

Input Signal
CLS (I / 3.3V)
THM (I / 3.3V)
BATT (I / 3.3V)
SCL (IO / 5V)
SDA (IO / 5V)
RESET#/PB5 (I/5V)
PB0/MOSI/AIN0
PB0/MOSI/AIN0

Output Signal
LDO (O / 5.4V)
XTAL2/PB4 (O/5V)
XTAL1/PB3 (O/5V)

AD_IN
CHARGE_LED#
BL2#

Output Power
VCC (O)
VCC (O)

DCBATOUT
BT+

Input Power
DCIN (I)

TI TPS51124
1.8V / 1.2V

PM_SLP_S5#

Input Signal
S5
S3

Output Signal
PGOOD(OD / 3.3V)

1D8V_S3_PG

Input Power
VCC(I)
VCC(I)

DCBATOUT
5V_S5

Output Power
VCC(O)
VCC(O)

1.8V_S3
1.2V_S0

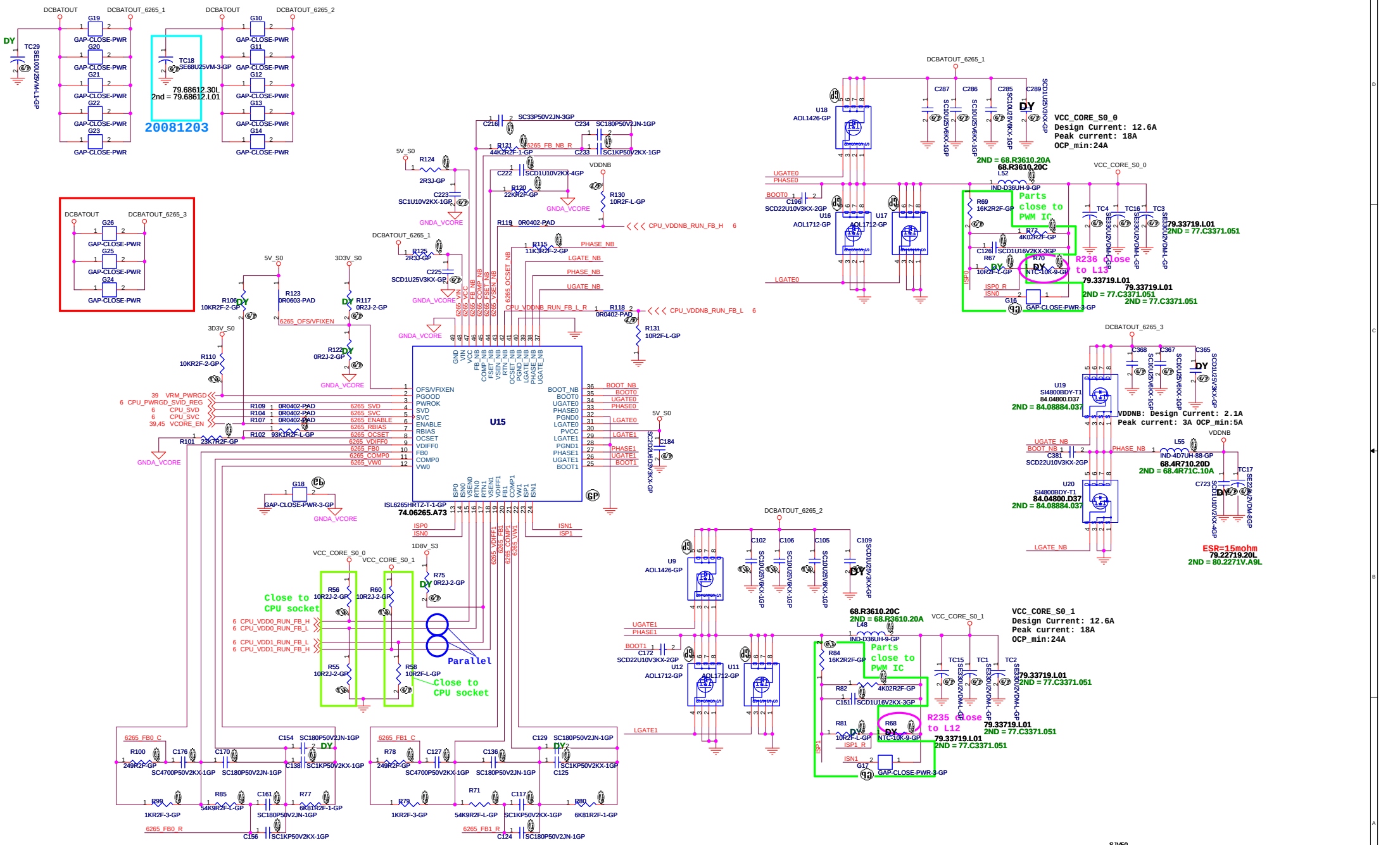
SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Block Diagram

Size	Document Number	Rev
A3	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 40 of 59



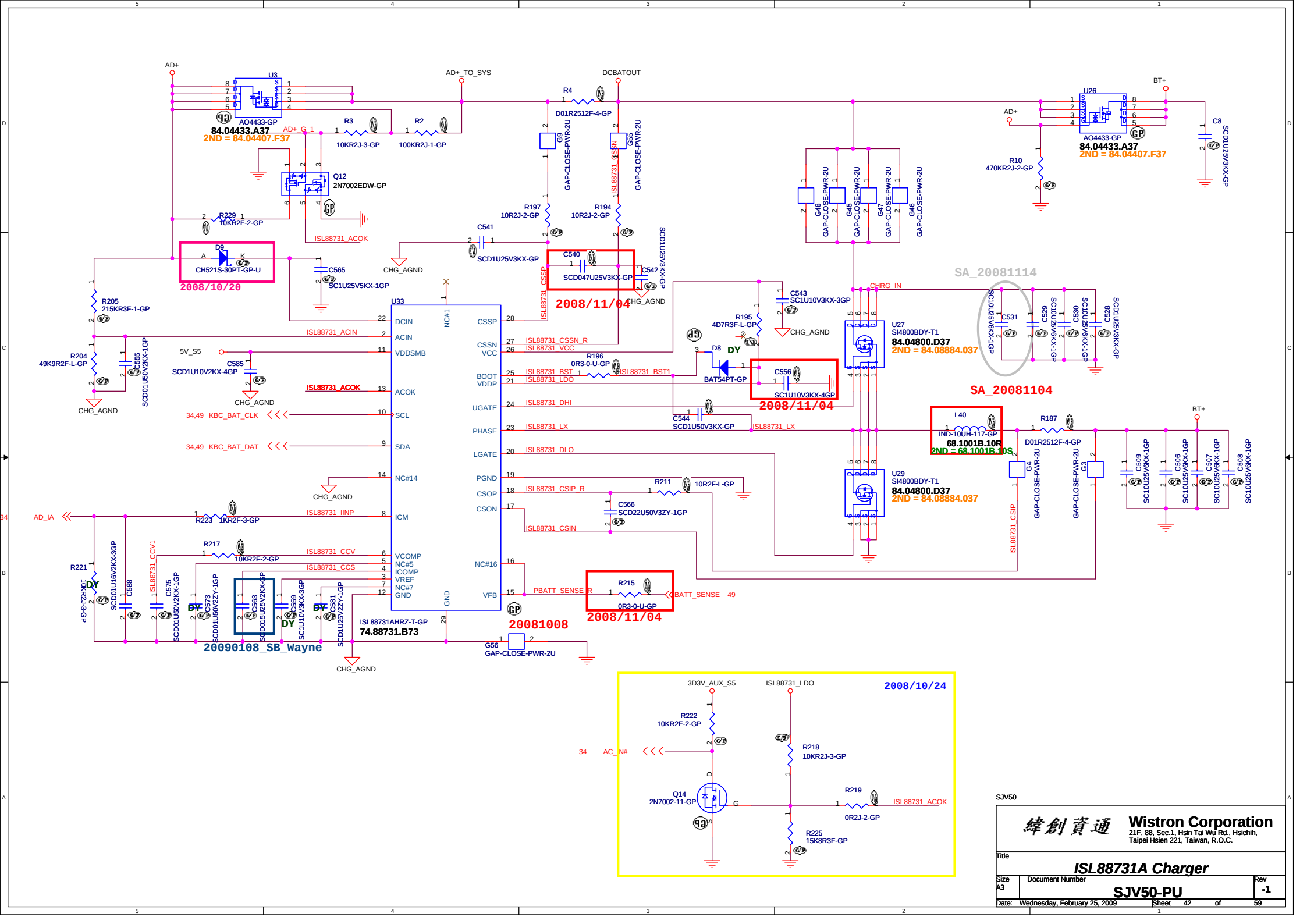
SJV50

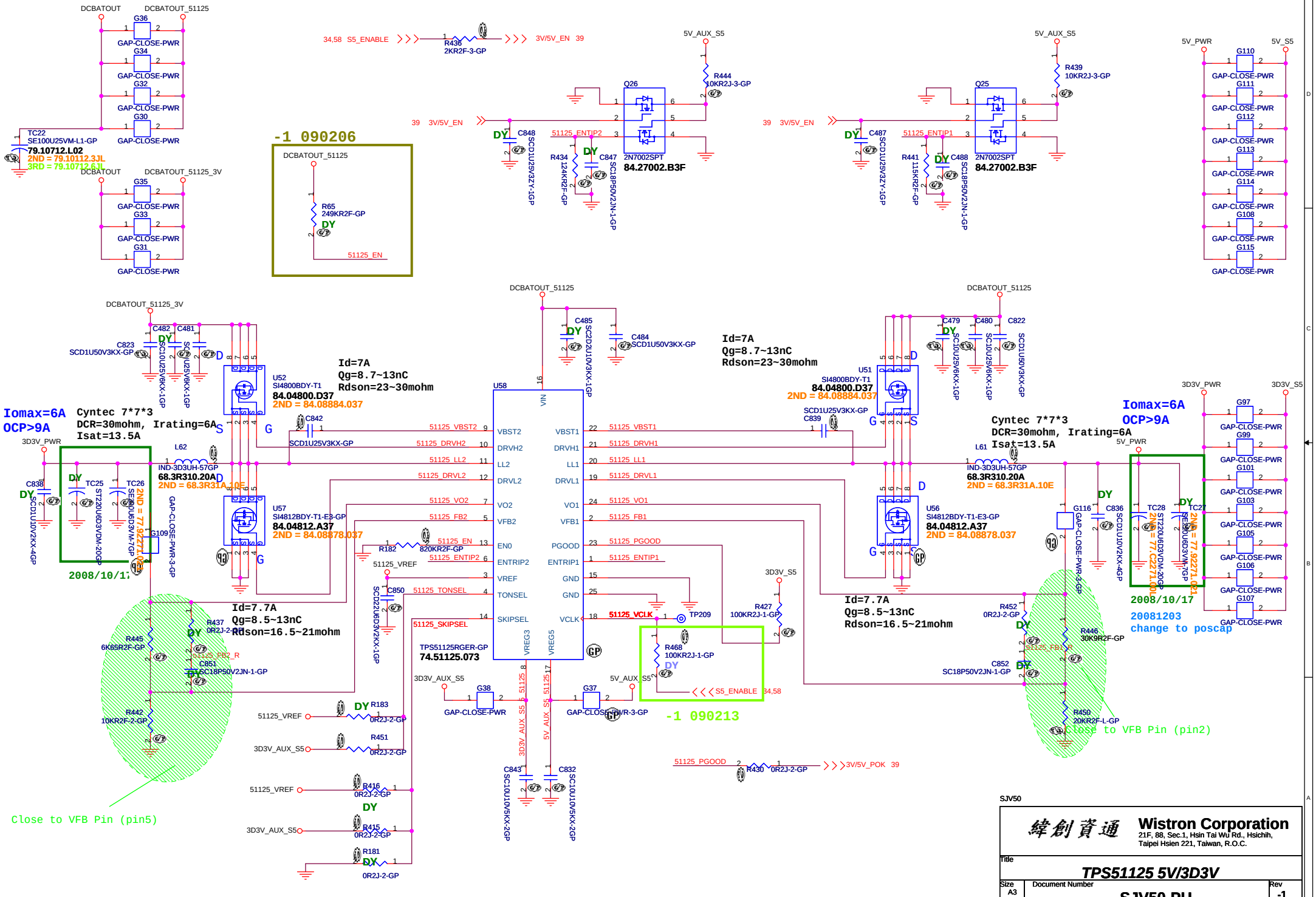
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

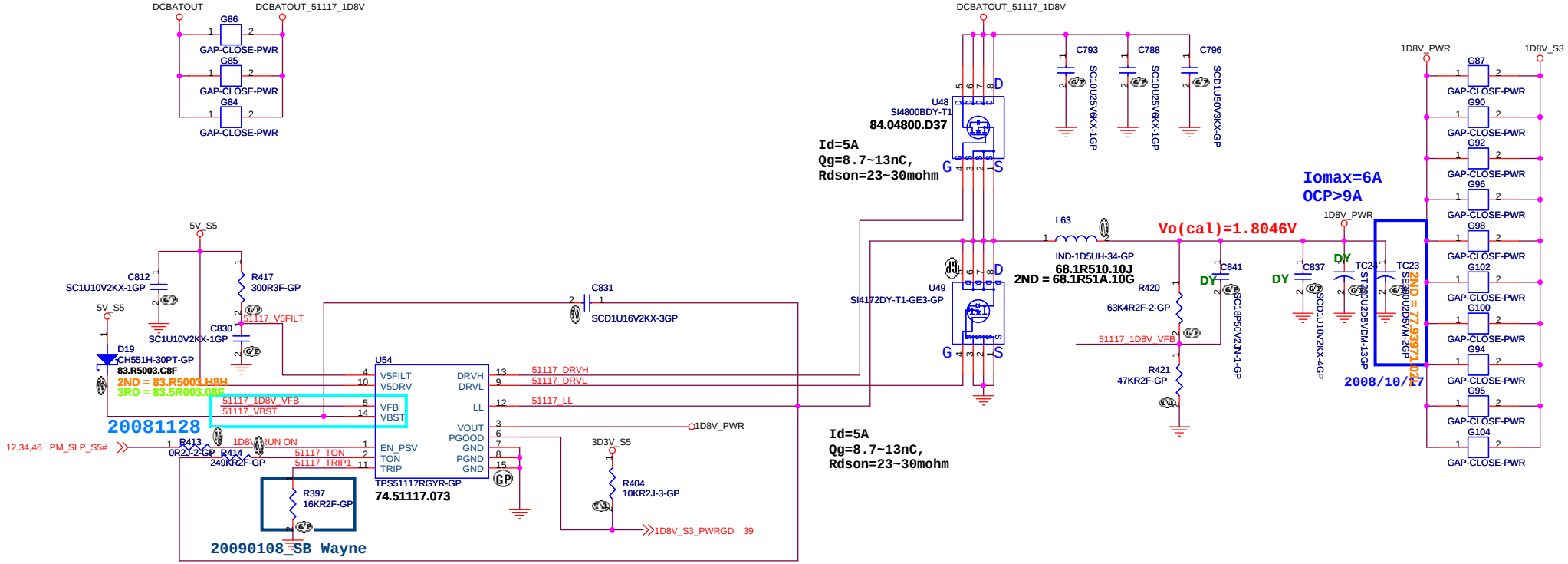
Title: CPU Vcore (ISL6265HR)

Size	Document Number	Rev
Custom	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 41 of 59

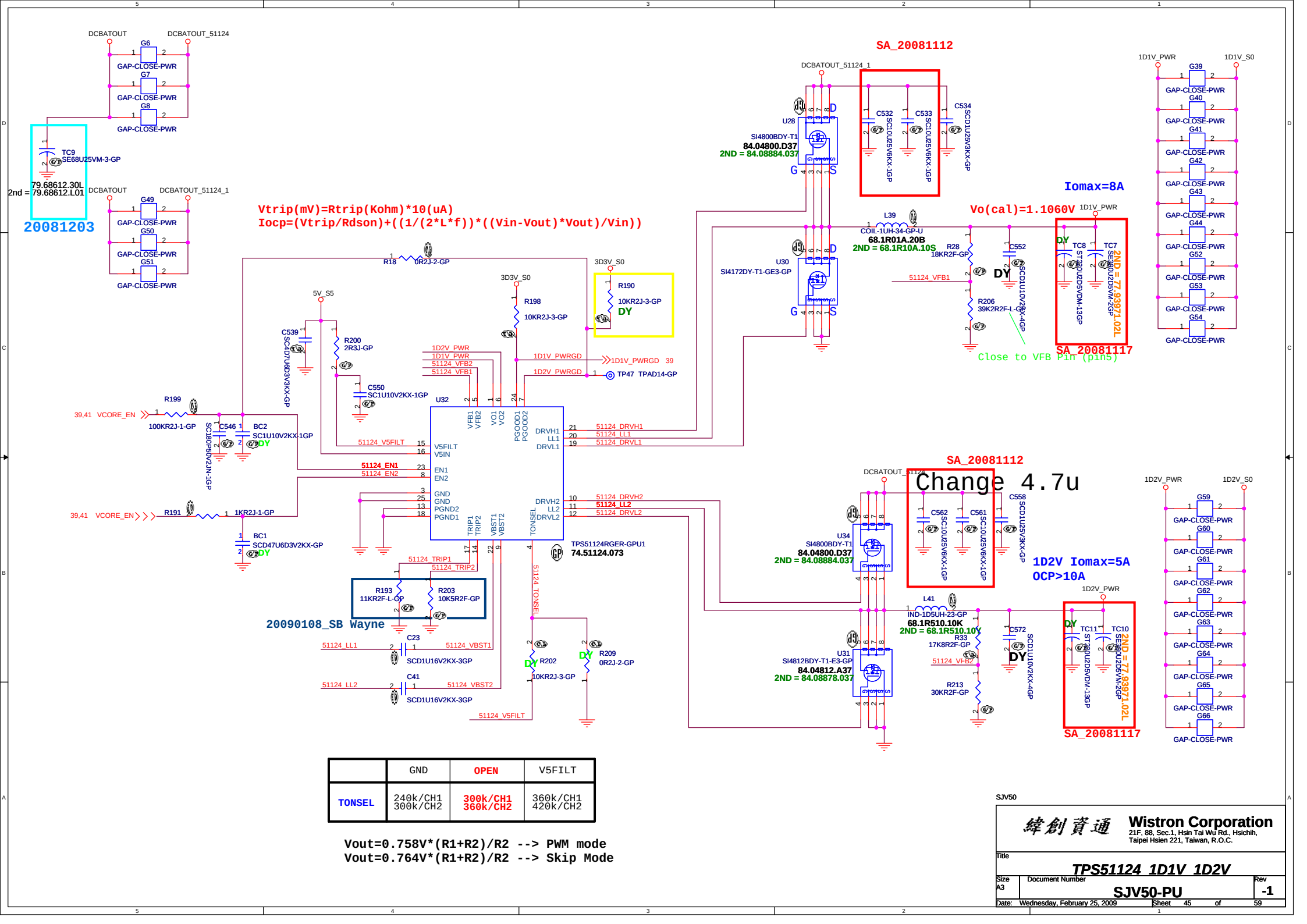

AD+
U3
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
AD+_TO_SYS
DCBATOUT
R4
D01R2512F-4-GP
R3
10KR2J-3-GP
R2
100KR2J-1-GP
Q12
2N7002EDW-GP
R229
10KR2F-2-GP
ISL88731_ACOK
D9
CH521S-30PT-GP-U
2008/10/20
C565
SC1U25V5KX-1GP
CHG_AGND
C541
SCD1U25V3KX-GP
R197
10R2J-2-GP
R194
10R2J-2-GP
C540
SCD047U25V3KX-GP
C542
2008/11/04
ISL88731_CSSP
ISL88731_GSFN
G9
G55
GAP-CLOSE-PWR-2U
U26
AO4433-GP
84.04433.A37
2ND = 84.04407.F37
R10
470KR2J-2-GP
C8
SCD1U25V3KX-GP
BT+
G48
G45
G47
G46
R205
215KR3F-1-GP
R204
49K9R2F-L-GP
C555
SCD01U50V2KX-1GP
C585
SCD1U10V2KX-4GP
5V_S5
U33
ISL88731AHRZ-T-GP
74.88731.B73
DCIN
ACIN
VDDSMB
ACOK
SCL
SDA
NC#14
ICM
VCOMP
NC#5
ICOMP
VREF
NC#7
GND
CSSP
CSSN
VCC
BOOT
VDDP
UGATE
PHASE
LGATE
PGND
CSOP
CSON
NC#16
VFB
ISL88731_ACIN
ISL88731_CSSN_R
ISL88731_VCC
ISL88731_BST
ISL88731_LDO
ISL88731_DHI
ISL88731_LX
ISL88731_DLO
ISL88731_CSIP_R
ISL88731_CSIN
ISL88731_IINP
ISL88731_CCV
ISL88731_CCS
PBATT_SENSE_R
34,49 KBC_BAT_CLK
34,49 KBC_BAT_DAT
AD_IA
R223
1KR2F-3-GP
R217
10KR2F-2-GP
R221
C588
C575
SCD01U50V2KX-1GP
C573
C563
C559
C581
SCD1U25V2ZY-1GP
20090108_SB_Wayne
20081008
G56
GAP-CLOSE-PWR-2U
R215
0R3-0-U-GP
2008/11/04
IBATT_SENSE
49
R196
0R3-0-U-GP
R195
4D7R3F-L-GP
D8
BAT54PT-GP
DY
C556
SC1U10V3KX-4GP
2008/11/04
C544
SCD1U50V3KX-GP
C543
SC1U10V3KX-3GP
CHRG_IN
U27
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
U29
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
SA_20081114
SA_20081104
C531
C529
C530
C528
SC10U25V6KX-1GP
L40
IND-10UH-117-GP
68.1001B.10R
2ND = 68.1001B.10S
R187
D01R2512F-4-GP
G4
G3
C509
C506
C507
C508
SC10U25V6KX-1GP
R211
10R2F-L-GP
C566
SCD22U50V3ZY-1GP
3D3V_AUX_S5
ISL88731_LDO
2008/10/24
R222
10KR2F-2-GP
R218
10KR2J-3-GP
Q14
2N7002-11-GP
R219
0R2J-2-GP
R225
15K8R3F-GP
AC_N#
ISL88731_ACOK
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
ISL88731A Charger
Size
A3
Document Number
SJV50-PU
Rev
-1
Date: Wednesday, February 25, 2009
Sheet 42 of 59


DCBATOUT
DCBATOUT_51125
G36
GAP-CLOSE-PWR
G34
GAP-CLOSE-PWR
G32
GAP-CLOSE-PWR
G30
GAP-CLOSE-PWR
TC22
SE100U25VM-L1-GP
79.10712.L02
2ND = 79.10112.3JL
3RD = 79.10712.6JL
DCBATOUT_51125_3V
G35
GAP-CLOSE-PWR
G33
GAP-CLOSE-PWR
G31
GAP-CLOSE-PWR
34,58 S5_ENABLE
R436
2KR2F-3-GP
3V/5V_EN 39
5V_AUX_S5
R444
10KR2J-3-GP
Q26
39 3V/5V_EN
C848
SCD1U25V3ZY-1GP
51125_ENTIP2
R434
124KR2F-GP
C847
SC18P50V2JN-1-GP
2N7002SPT
84.27002.B3F
-1 090206
DCBATOUT_51125
R65
249KR2F-GP
DY
51125_EN
R439
10KR2J-3-GP
Q25
C487
51125_ENTIP1
R441
115KR2F-GP
C488
5V_PWR
5V_S5
G110
G111
G112
G113
G114
G108
G115
DCBATOUT_51125_3V
C823
SCD1U50V3KX-GP
C482
C481
SC1U25V6KX-1GP
U52
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
Id=7A
Qg=8.7~13nC
Rdson=23~30mohm
C842
SCD1U25V3KX-GP
Iomax=6A
OCP>9A
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
3D3V_PWR
L62
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
C838
SCD1U10V2KX-4GP
TC25
ST220U6D3VDM-20GP
TC26
SE330U6D3VM-7GP
2ND = 77.82271.L01
G109
GAP-CLOSE-PWR-3-GP
2008/10/17
U57
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
R182
820KR2F-GP
51125_VREF
C850
SCD22U6D3V2KX-1GP
51125_TONSEL
51125_SKIPSEL
TPS51125RGER-GP
74.51125.073
U58
VIN
VBST2
DRVH2
LL2
DRVL2
VO2
VFB2
EN0
ENTRIP2
VREF
TONSEL
SKIPSEL
VREG3
VREG5
VBST1
DRVH1
LL1
DRVL1
VO1
VFB1
PGOOD
ENTRIP1
GND
GND
VCLK
51125_VBST2
51125_DRVH2
51125_LL2
51125_DRVL2
51125_VO2
51125_FB2
51125_EN
51125_ENTIP2
51125_TONSEL
51125_SKIPSEL
51125_VBST1
51125_DRVH1
51125_LL1
51125_DRVL1
51125_VO1
51125_FB1
51125_PGOOD
51125_ENTIP1
51125_VCLK
TP209
R437
0R2J-2-GP
R445
6K65R2F-GP
51125_FB2_R
C851
SC18P50V2JN-1-GP
R442
10KR2F-2-GP
Close to VFB Pin (pin5)
R183
0R2J-2-GP
R451
0R2J-2-GP
R416
0R2J-2-GP
R415
0R2J-2-GP
R181
0R2J-2-GP
3D3V_AUX_S5
5V_AUX_S5
G38
GAP-CLOSE-PWR
G37
GAP-CLOSE-PWR-3-GP
C843
C832
SC10U10V5KX-2GP
R468
100KR2J-1-GP
S5_ENABLE 34,58
-1 090213
R427
100KR2J-1-GP
51125_PGOOD
R430
0R2J-2-GP
3V/5V_POK 39
C485
SC2D2U10V3KX-1GP
C484
SCD1U50V3KX-GP
Id=7A
Qg=8.7~13nC
Rdson=16.5~21mohm
U51
SI4800BDY-T1
84.04800.D37
2ND = 84.08884.037
C839
C479
C480
C822
SC10U25V6KX-1GP
U56
SI4812BDY-T1-E3-GP
84.04812.A37
2ND = 84.08878.037
Id=7.7A
Qg=8.5~13nC
Rdson=16.5~21mohm
L61
IND-3D3UH-57GP
68.3R310.20A
2ND = 68.3R31A.10E
Cyntec 7*7*3
DCR=30mohm, Irating=6A
Isat=13.5A
Iomax=6A
OCP>9A
3D3V_S5
G116
C836
SCD1U10V2KX-4GP
TC28
ST220U6D3VDM-20GP
TC27
SE330U6D3VM-7GP
2ND = 77.82271.L01
2008/10/17
20081203
change to poscap
R452
0R2J-2-GP
R446
30K9R2F-GP
51125_FB1_R
C852
SC18P50V2JN-1-GP
R450
20KR2F-L-GP
Close to VFB Pin (pin2)
G97
G99
G101
G103
G105
G106
G107
SJV50
緯創資通
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
TPS51125 5V/3D3V
Size
A3
Document Number
SJV50-PU
Rev
-1
Date: Wednesday, February 25, 2009
Sheet 43 of 59



SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***TPS51124_1D8V/1D2V***	
Size A3	Document Number **SJV50-PU**	Rev **-1**
Date: Wednesday, February 25, 2009	Sheet 44 of 59	



	GND	OPEN	V5FILT
TONSEL	240k/CH1 300k/CH2	300k/CH1 360k/CH2	360k/CH1 420k/CH2

Vout=0.758V*(R1+R2)/R2 --> PWM mode
Vout=0.764V*(R1+R2)/R2 --> Skip Mode

SJV50

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

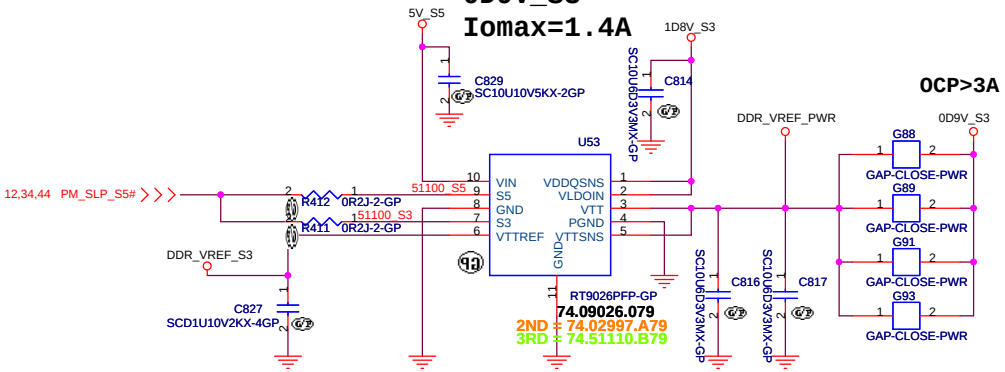
Title: TPS51124 1D1V 1D2V

Size	Document Number	Rev
A3	SJV50-PU	-1

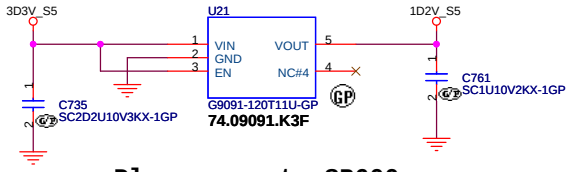
Date: Wednesday, February 25, 2009 Sheet 45 of 59

0D9V_S3
Iomax=1.4A

OCP>3A



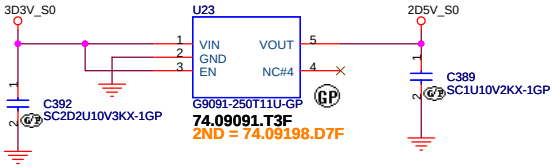
1D2V_S5
Iomax=0.2A



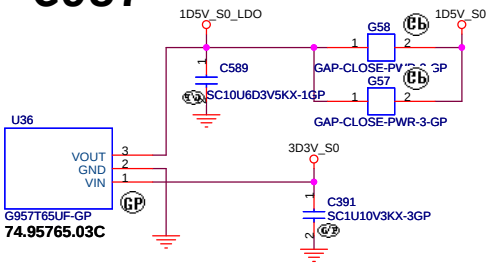
Place near to SB600

2D5V_S0
Iomax=200mA

OCP>430mA



G957
1D5V_S0
Iomax=1A

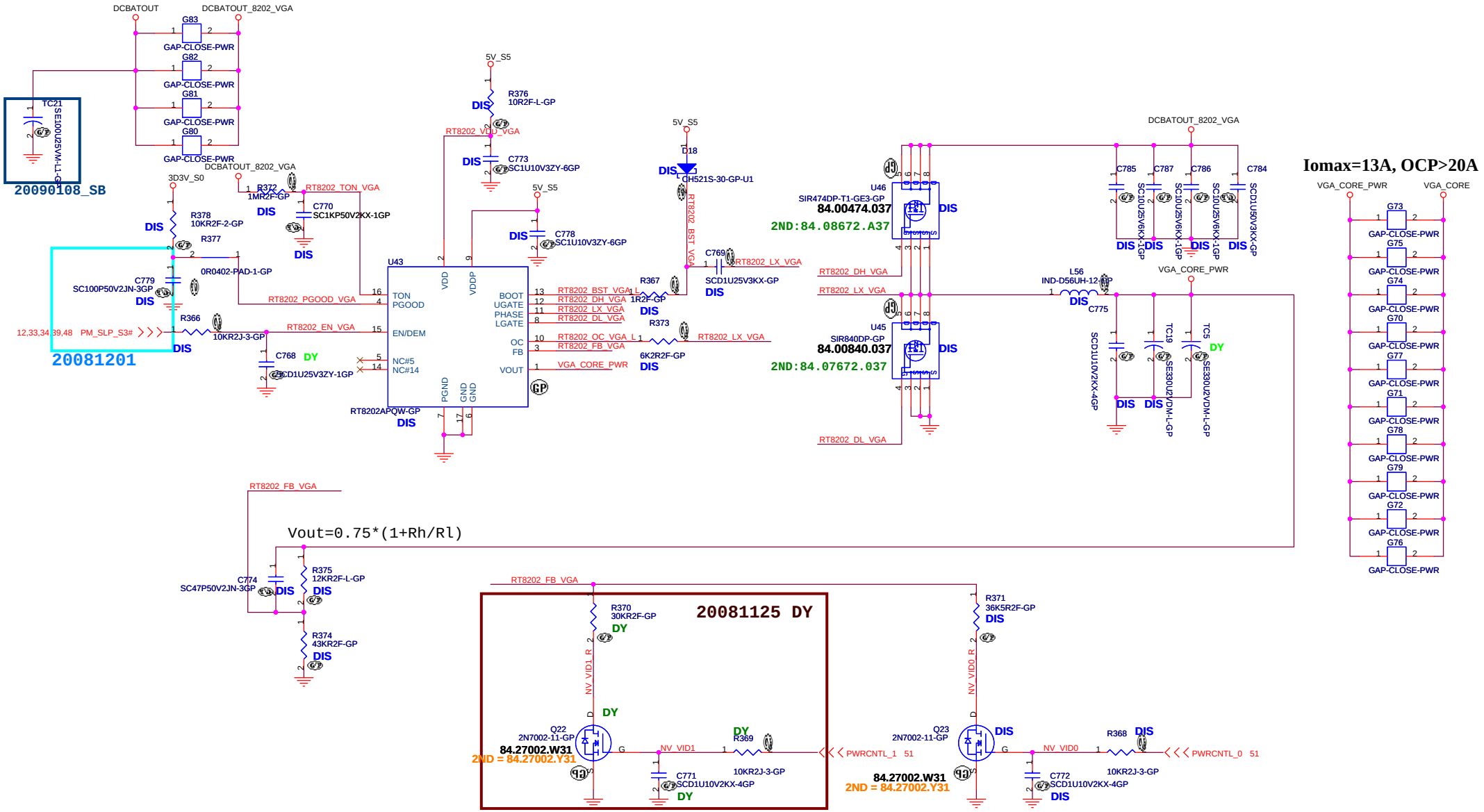


For MINI Card power SW

<Core Design>

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

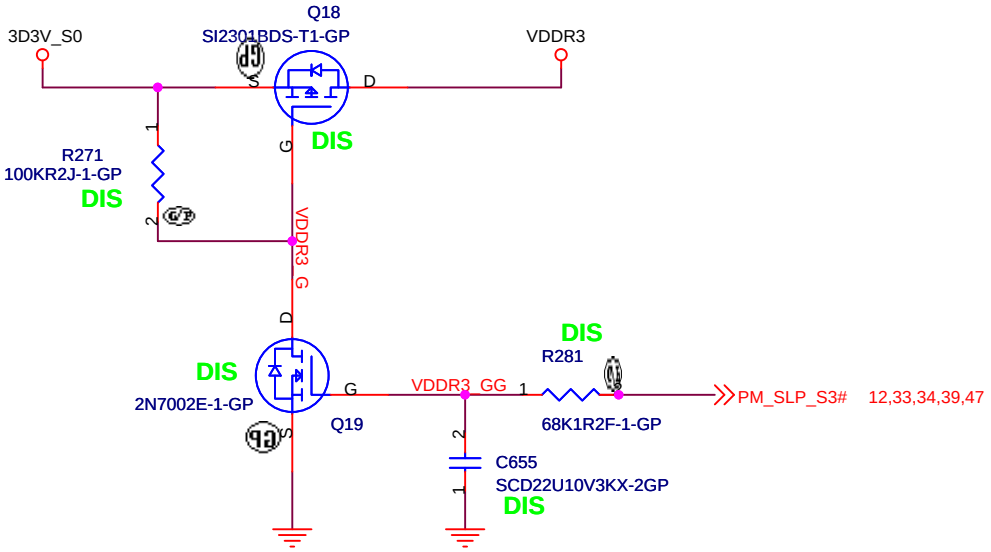
Title: *2D5V/1D5V0D9V*		
Size: A3	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 46 of 59	



SJV50

緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	RT8202A_VGA CORE	
Size	Document Number SJV50-PU	Rev -1
Date: Wednesday, February 25, 2009	Sheet 47 of 59	



SJV50

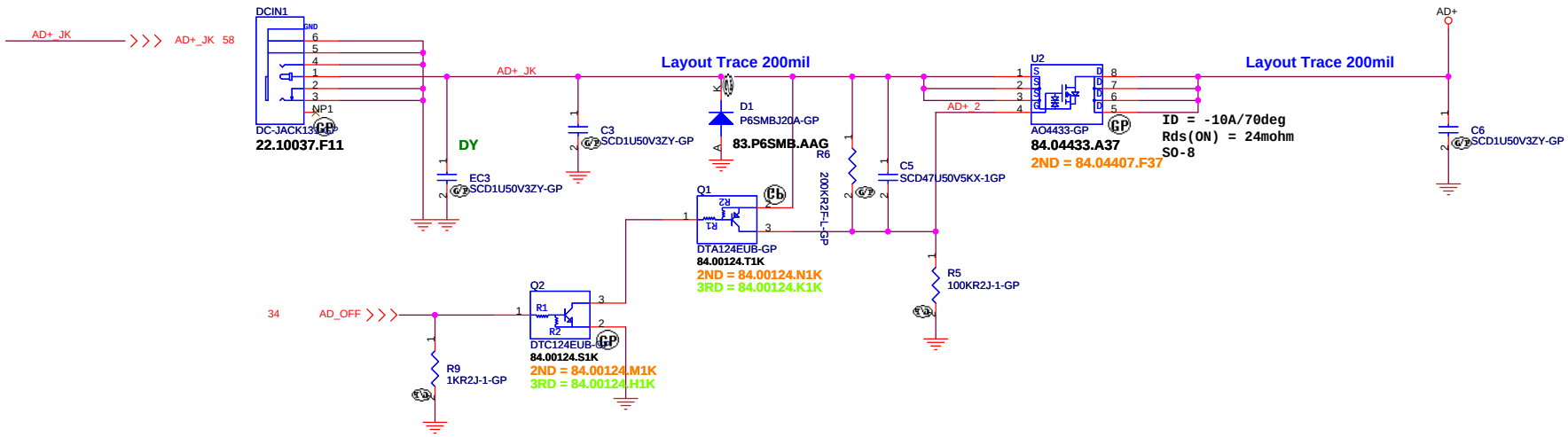
緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *VDDR3*

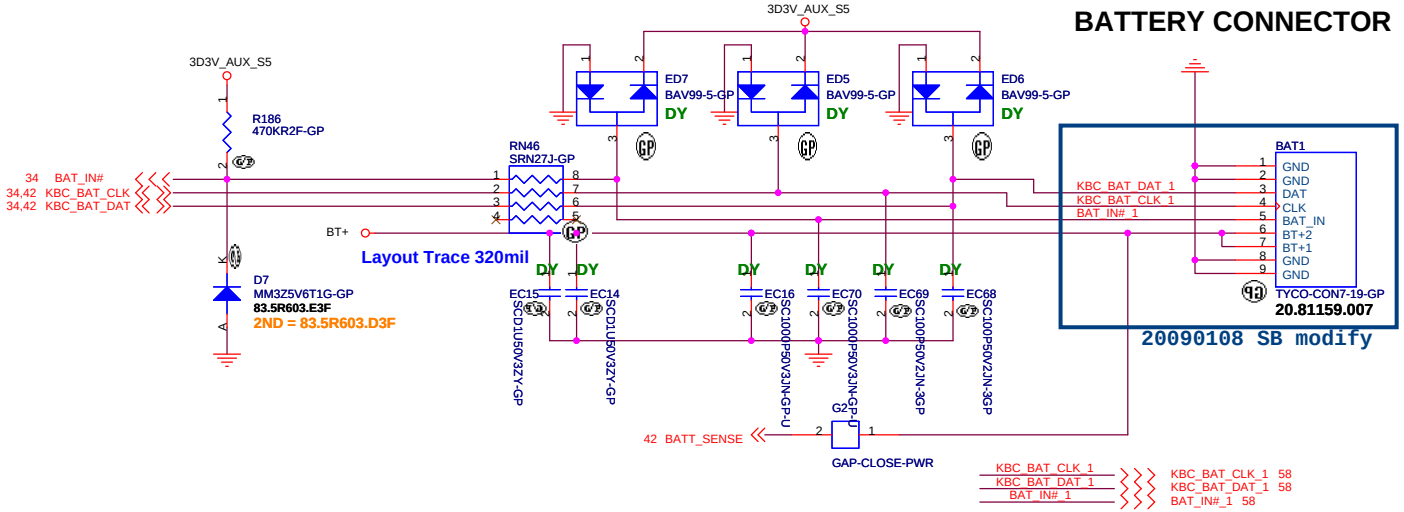
Size	Document Number	Rev
A4	SJV50-PU	-1

Date: Wednesday, February 25, 2009 Sheet 48 of 59

Adaptor in to generate DCBATOUT



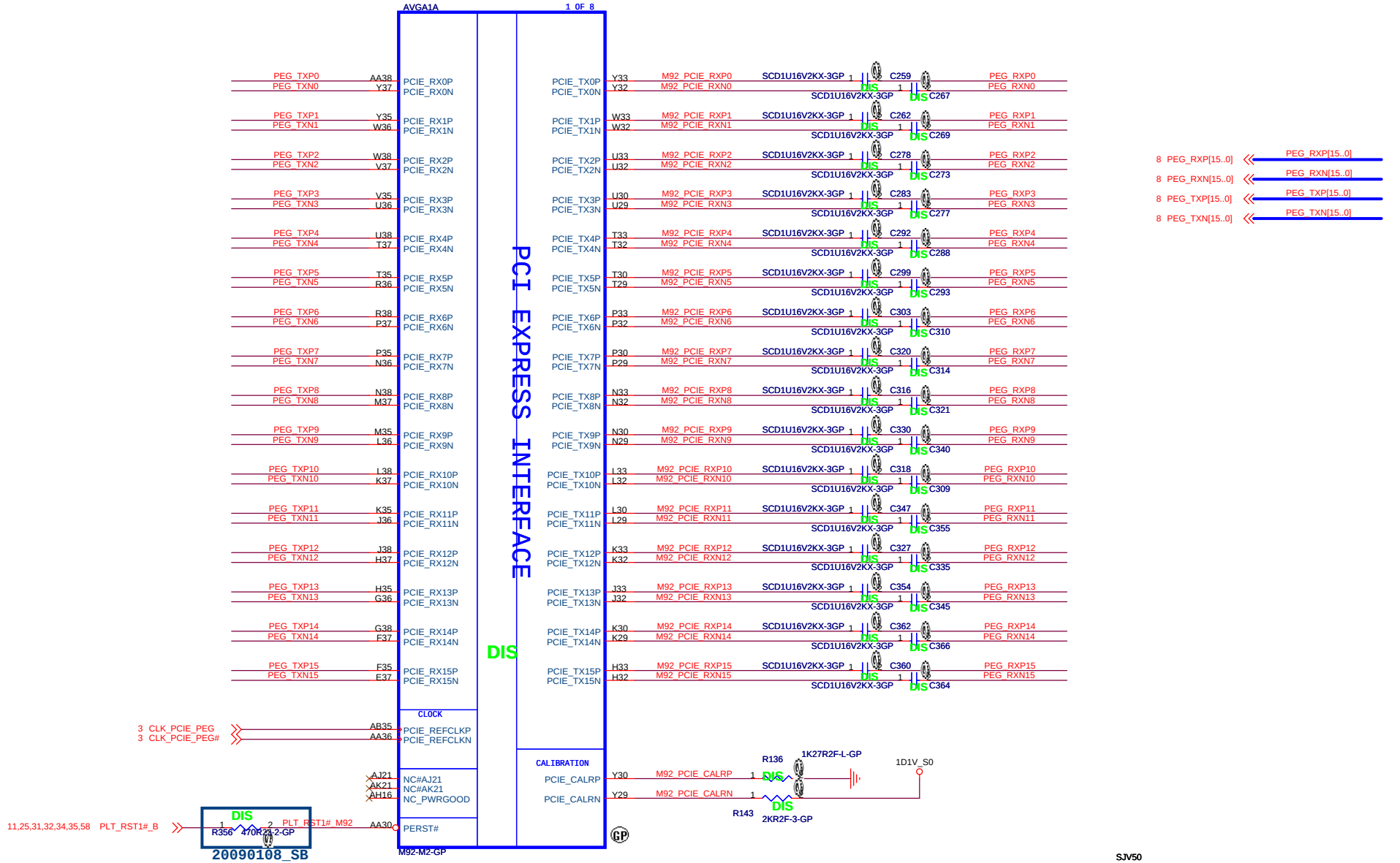
BATTERY CONNECTOR



SJV50

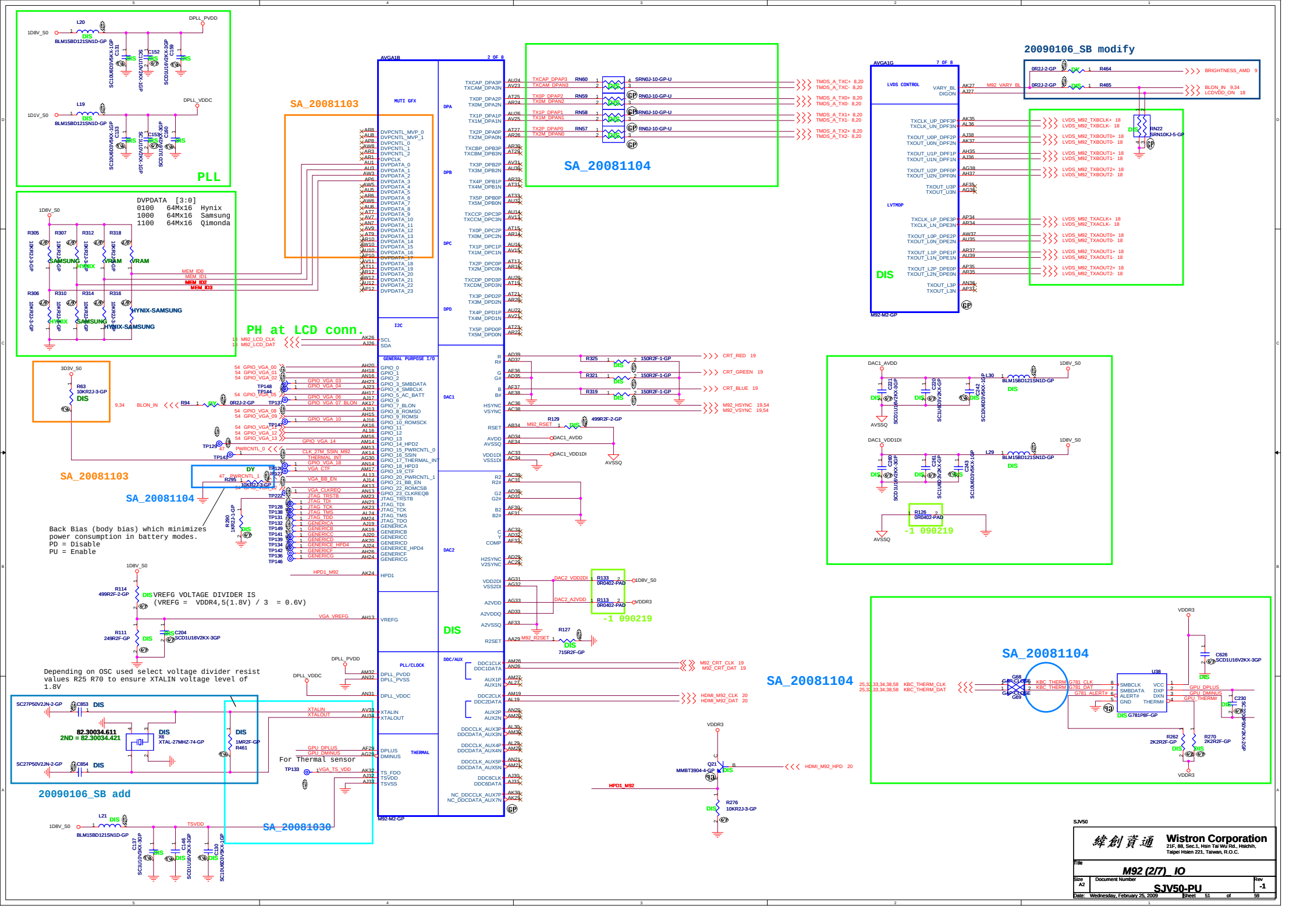
緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

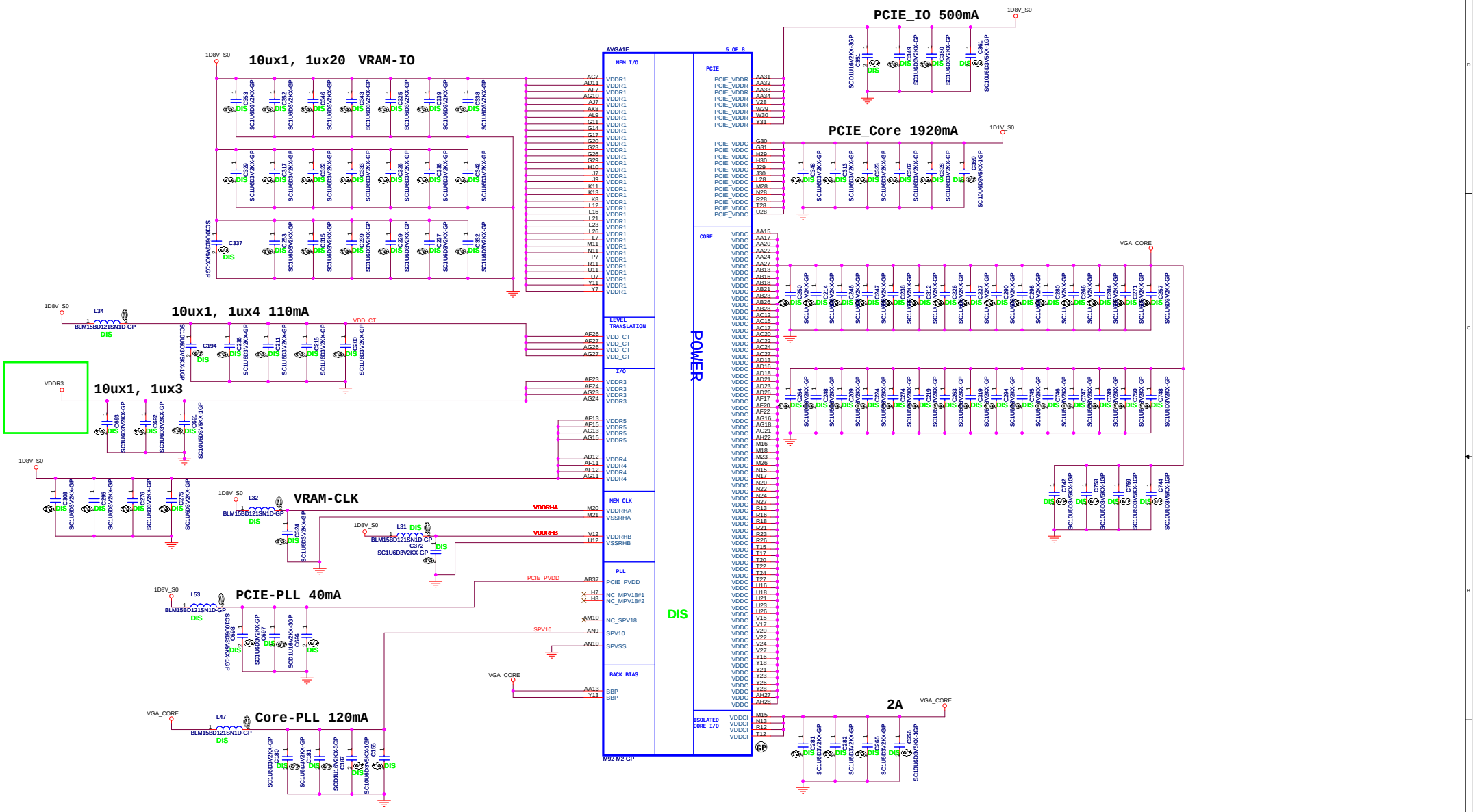
Title	AD/BATT CONN	
Size A3	Document Number SJV50-PU	Rev -1
Date: Wednesday, February 25, 2009	Sheet 49 of 59	



SJV50

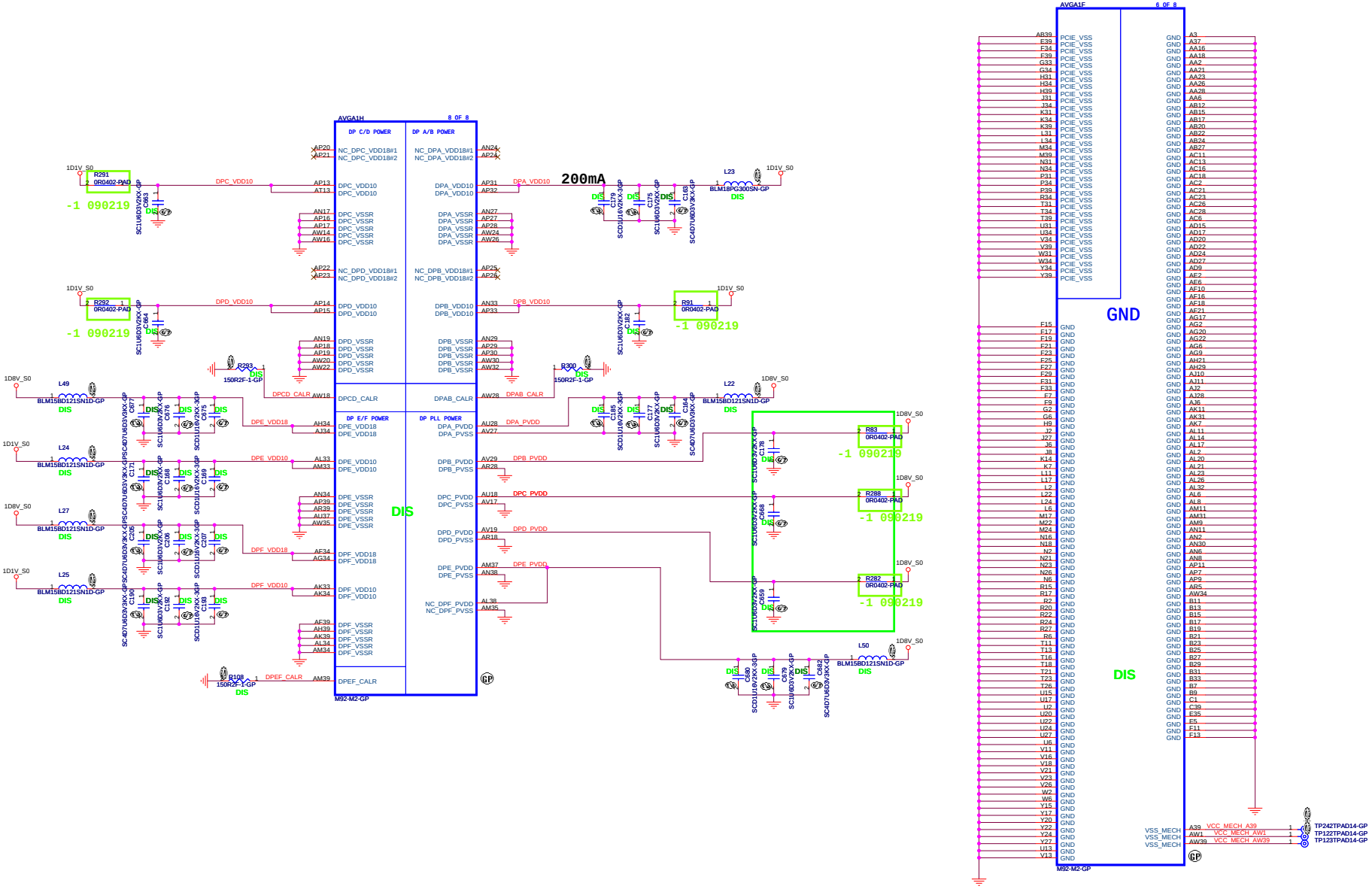
緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: *M92 (1/7) PCIE*		
Size: A3	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 50 of 59	


PLL
SA_20081103
SA_20081104
SA_20081030
20090106_SB modify
20090106_SB add
PH at LCD conn.
DVPDATA [3:0]
0100 64Mx16 Hynix
1000 64Mx16 Samsung
1100 64Mx16 Qimonda
Back Bias (body bias) which minimizes power consumption in battery modes.
PD = Disable
PU = Enable
VREFG VOLTAGE DIVIDER IS (VREFG = VDDR4,5(1.8V) / 3 = 0.6V)
Depending on OSC used select voltage divider resist values R25 R70 to ensure XTALIN voltage level of 1.8V
For Thermal sensor
-1 090219
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.
M92 (2/7)_IO
SJV50-PU
-1



SJV50

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.		
Title: M92 (3/7) Power		
Size: A2	Document Number: SJV50-PU	Rev: -1
Date: Wednesday, February 25, 2009	Sheet 52 of 59	



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緯創資通	Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	M92 (4/7)_DP POWER_GND	
Size: A2	Document Number: SJV50-PU	Rev: -1
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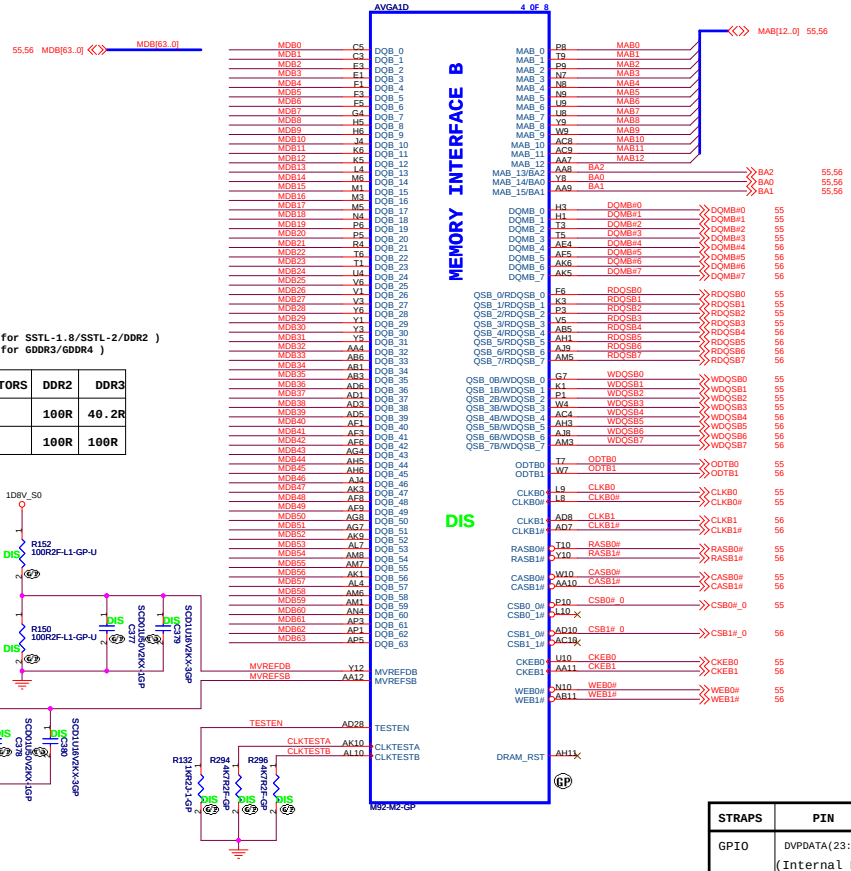
M92-M2 uses memory group B only

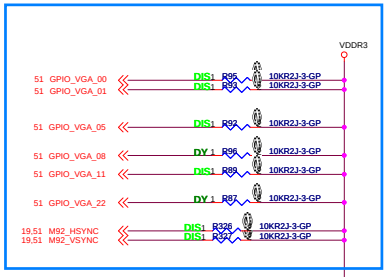


(0.5 * VDDR1) (for SSTL-1.8/SSTL-2/DDR2)
(0.7 * VDDR1) (for GDDR3/GDDR4)

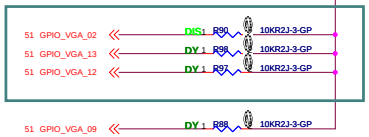
DIVIDER RESISTORS	DDR2	DDR3
MVREF TO 1.8V	100R	40.2R
MVREF TO GND	100R	100R

STRAPS	PIN	DESCRIPTION
GPIO	DVPDATA(23:20) (Internal PD)	Initialization Behavior: This signal is input during reset (no reference clock is required). After reset, the default state is output low (0 V). The signals above can be left unconnected if not used.

SA_20081104



SA_20081105



HDMI must only be enabled on systems that are legally entitled. It is the responsibility of the system designer to ensure that the system is entitled to support this feature.

AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

H2SYNC, GENERICC

PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

GPIO_28_TDO , GPIO21_BB_EN

If BIOS_ROM_EN (GPIO22) = 0		If BIOS_ROM_EN (GPIO22) = 1		
Size of the primary memory apertures	GPIO[13,12,11]	Manufacturer	Part Number	GPIO[13,12,11]
V 128MB	x000	ST Microelectronics	M25P05A	0100
256MB	x001		M25P10A	0101
64MB	x010		M25P20	0101
32MB	x		M25P40	0101
512MB	x		M25P80	0101
1GB	x	Chingis (formerly PMC)	Pm25LV512A	0100
2GB	x		Pm25LV010A	0101
4GB	x			

STRAPS	PIN	DESCRIPTION	RECOMMENDED SETTINGS 0= DO NOT INSTALL RESISTOR 1 = INSTALL 10K RESISTOR X = DESIGN DEPENDANT NA = NOT APPLICABLE
TX_PWRS_ENB (Internal PD)	GPIO0	PCIE FULL TX OUTPUT SWING Tansmitter Power Savings Enable 0= 50% Tx output swing 1= Full Tx output swing	1
TX_DEEMPH_EN (Internal PD)	GPIO1	Transmitter De-emphasis Enable 0= Tx de-emphasis disabled 1= Tx de-emphasis enabled	1
BIF_GEN2_EN_A	GPIO2	PCIE GNE2 ENABLED 0 = Advertises the PCI-E device as 2.5GT/s 1 = Advertises the PCI-E device as 5GT/s	1
AC_BATT	GPIO5	AC (Performance mode) = 3.3 V Battery saving mode = 0.0 V	
ROMSO	GPIO8	BIF_CLK_PM_EN Serial ROM Output from ROM	0
ROMSI	GPIO9	VGA ENABLED Serial ROM Input to ROM	0
ROMIDCFG[3:0] (Internal PD)	GPIO[13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT if BIOS_ROM_EN=1,then Config[3:0] defines the ROM type if BIOS_ROM_EN=0,then Config[3:0] defines the primary memory apeture size	X X X
PWRCNTL_[1,0]	GPIO[15,20]	Power control signals to control the core voltage regulator	
BB_EN	GPIO21	Back Bias (body bias) which minimizes power consumption in battery modes. 0V = Disable 3D3V = Enable	0
AUD[1] AUD[0] (Internal PD)	VGA_HSYNC VGA_VSYNC	AUD[1:0] 00:No audio function 01:Audio for DisplayPort and HDMI (if adapter is detected) 10:Audio for DisplayPort only 11:Audio for both DisplayPort and HDMI	1
CCBYPASS	GENERICC		0

SJV50

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Title: M92 (5/7) Memory Straps

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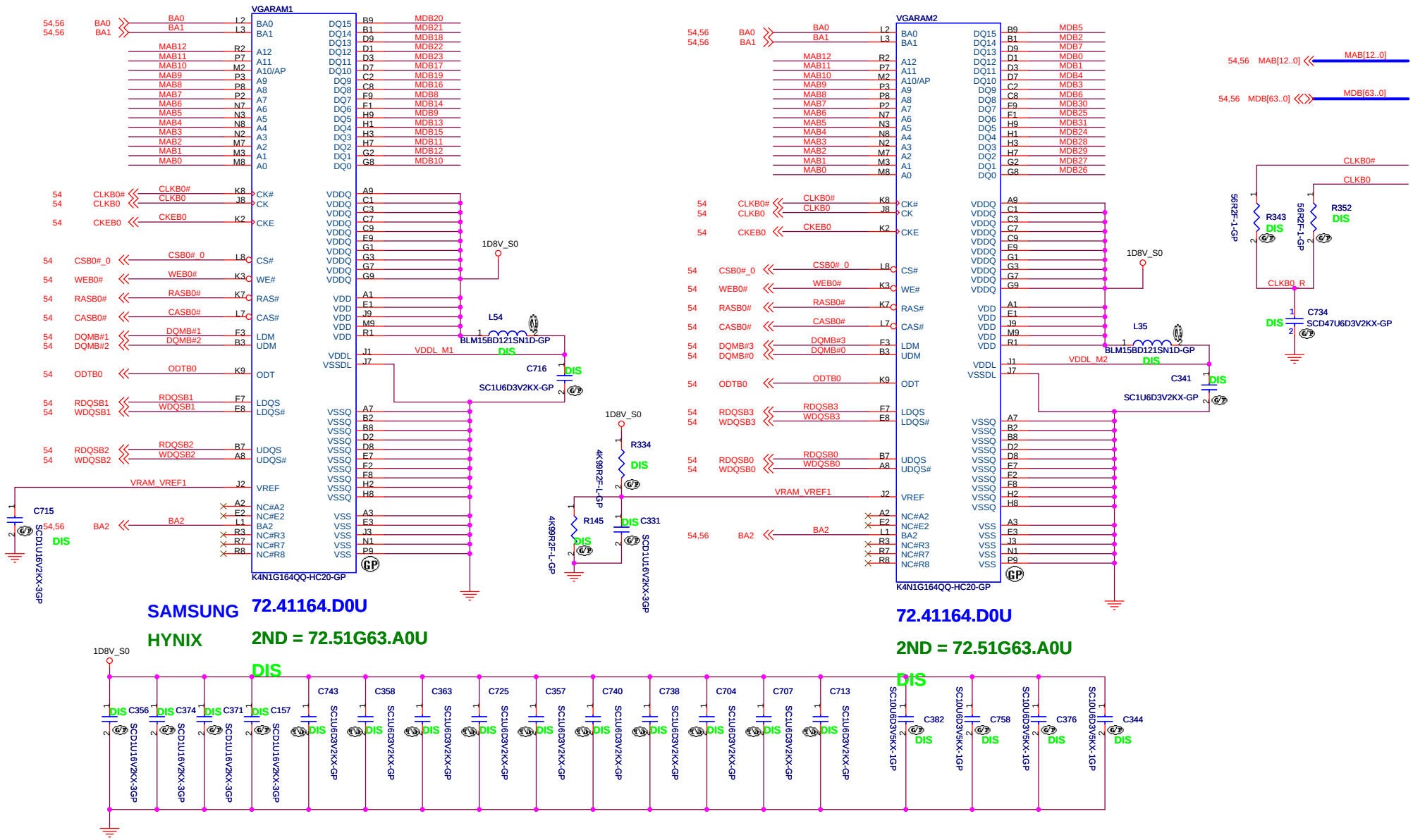

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緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M92 (6/7) VRAM B0***	
Size: A3	Document Number: **SJV50-PU**	Rev: -1
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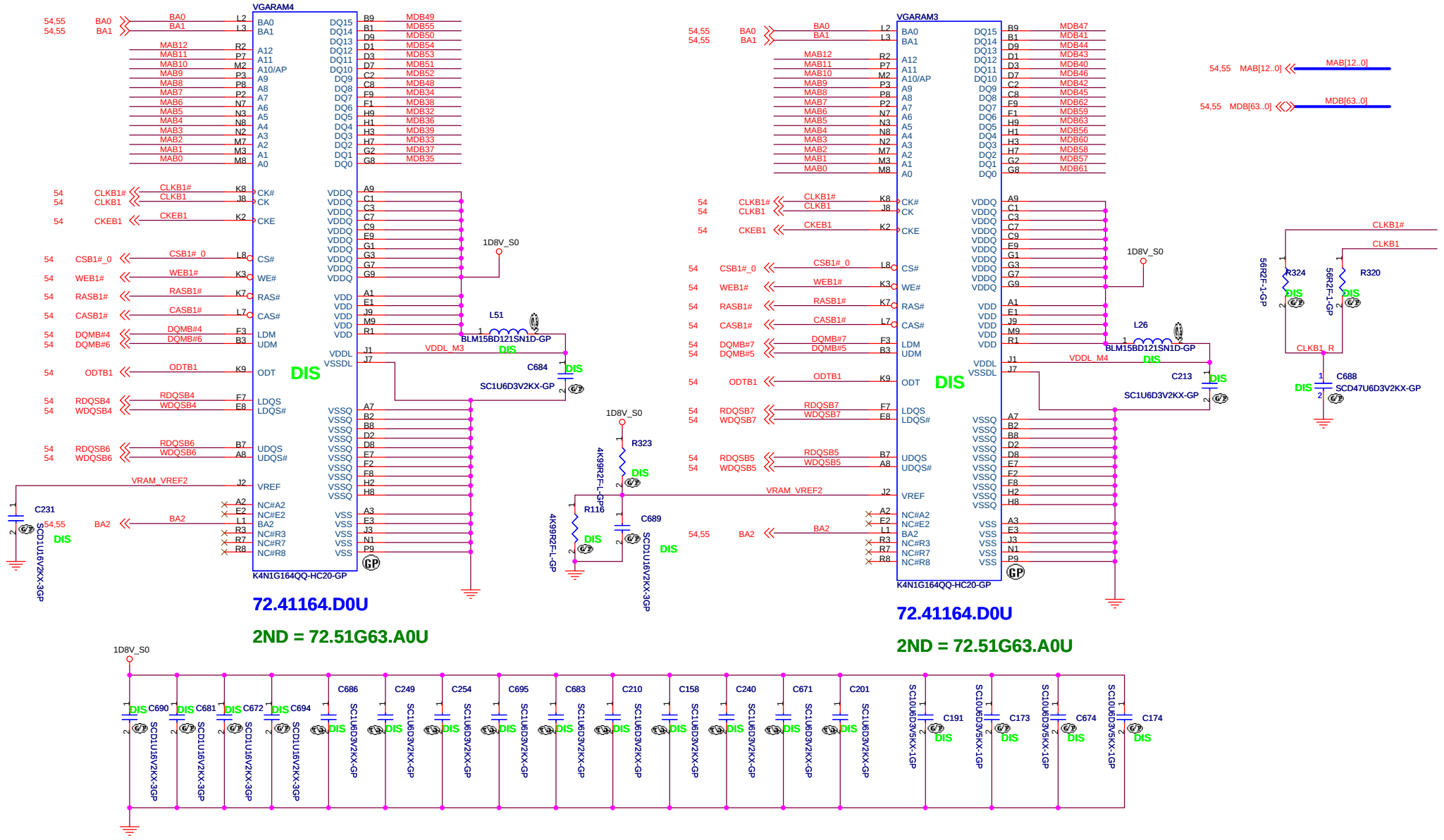

SJV50

緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***M92 (7/7) VRAM B1***	
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SA

SB

-1

5V_S0

U7C
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12
3RD = 73.74125.01B

5V_S0

U7D
TSAHCT125PW-GP
73.74125.L13
2ND = 73.74125.L12
3RD = 73.74125.01B

GND1 GND2 GND3 GND4 GND5

HOLE355X355R111-S1-GP

GND6 GND7 GND8 GND9 GND10

HOLE355X355R111-S1-GP

-1_0205

-1_0217

H7 HOLE236R142 34.42Y01.031 Type-M

H8 HOLE236R142 34.42Y01.031 Type-M

H15 HOLE276R110 34.4B804.001 DY

H20 HOLE276R110 34.4B804.001 DY

H11 HOLE276R142 34.42Y01.031 Type-I

H12 HOLE276R142 34.42Y01.031 Type-I

H13 HOLE276R142 34.42Y01.031 Type-I

H14 HOLE276R142 34.42Y01.031 Type-I

H16 HOLE276R142 34.42Y01.031 Type-I

H17 HOLE276R142 34.42Y01.031 Type-I

SPR1 SPRING-71-GP 34.4H551.001

SPR2 SPRING-71-GP DY 34.4H551.001

SPR3 SPRING-71-GP DY 34.4H551.001

20081203

20081202

DCBATOUT

-1 090223_EMI

-1 090223_EMI

1D1V_S0

5V_S5

5V_S0

3D3V_S0

SJV50

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Taipei Hsien 221, Taiwan, R.O.C.

Title: EMI/Spring/Boss

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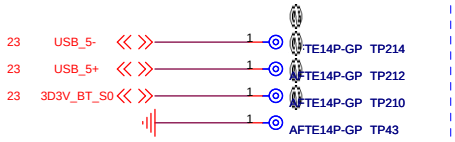
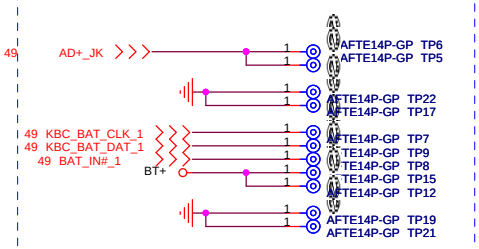
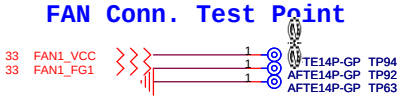
BT Conn. Test Point



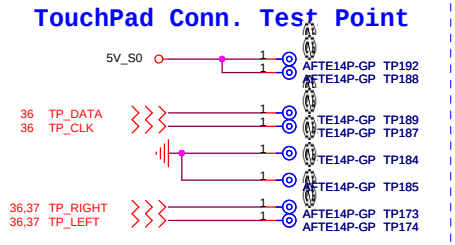
AD+, BAT Conn. Test Point



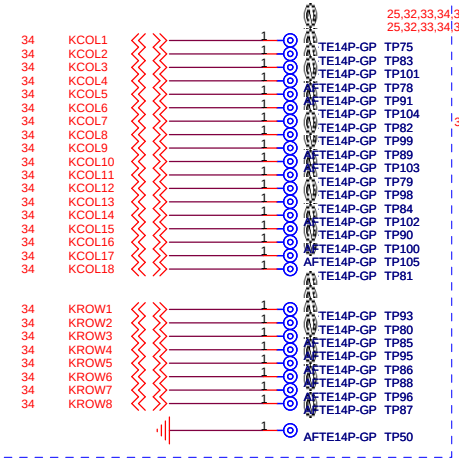
FAN Conn. Test Point



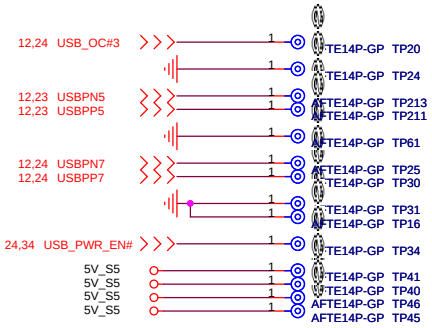
TouchPad Conn. Test Point



KB Conn. Test Point

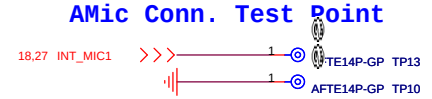


USBCN1 Conn. Test Point

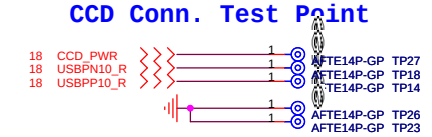


PowerButton Conn. Test Point

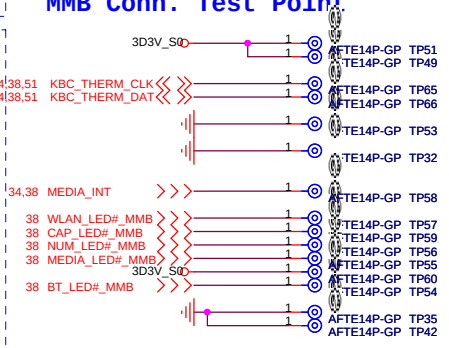
AMic Conn. Test Point



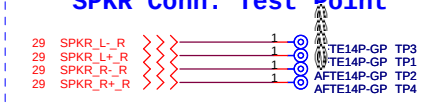
CCD Conn. Test Point



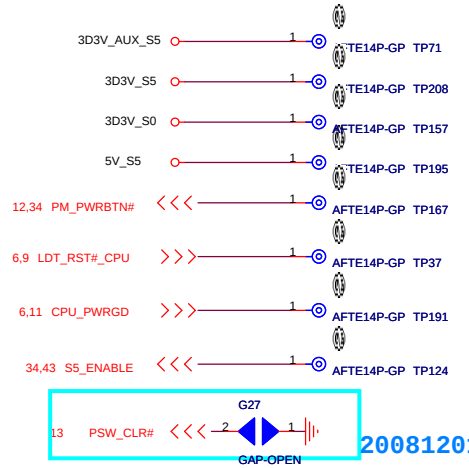
MMB Conn. Test Point



SPKR Conn. Test Point

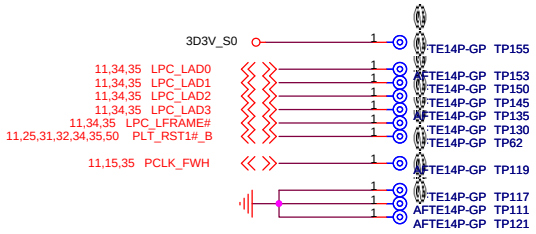


Check test point



20081201

Test Point放在Dimm Door打開可量測處



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Title: *Test point*

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Title

Change List

Size | Document Number | Rev

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