Compal Confidential

ZIWB2/ZIWB3/ZIWE1
DIS M/B Schematics Document

Intel Boardwell U Processor with DDR3L
AMD Topaz XT / Jet LE

2014-02-10

LA-B091P

REV：1.0

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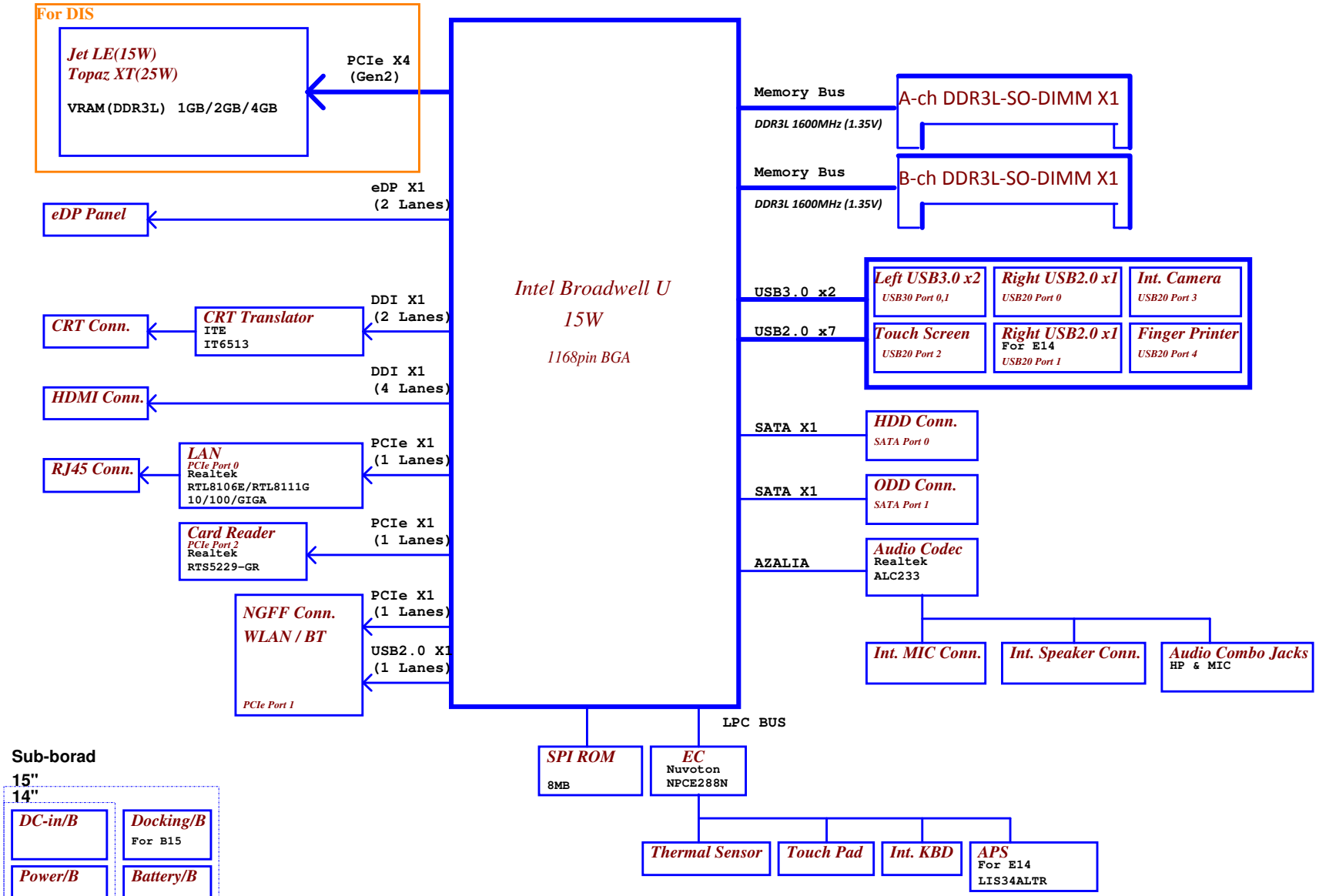
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	Cover Page		
Size: C	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 1 of 55		



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Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	MB Block Diagram		
Size C	Document Number		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 2 of 55		

Voltage Rails

power plane / State	+B	+5VALW +3VALW	+1.5V	+5VS +3VS +1.5VS +V1.05S_VCCP +VCC_CORE +VGA_CORE +VCC_GFXCORE_AXG +1.8VS +0.75VS +1.05VS
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

USB Port Table

	USB 2.0	Port	3 External USB Port
EHCI1	UHCI0	0	USB Port (Left Side) USB3.0
		1	USB Port (Left Side) USB3.0
	UHCI1	2	Touch Screen
		3	Camera
	UHCI2	4	
		5	
	UHCI3	6	
		7	
EHCI2	UHCI4	8	
		9	USB Port (Right Side USB-BD)
	UHCI5	10	Mini Card(WLAN)
		11	Card Reader
	UHCI6	12	
		13	

BOM Structure Table

Item	BOM Structure	
ZIWB2 (14")	B14@	
ZIWB3 (15")	B15@	
ZIWE1 (14")	E14@	
CPU_SA00006SM20	i5_4200U@	
CPU_SA00007AM00	QFSY@	
CPU_SA00006SU30	i3_4100U@	
CPU_SA000072Q10	i3_4005U@	
CPU_SA00006SX20	i3_4010U@	
LAN 10/100 Transformer	100@	
LAN GIGA Transformer	GIGA@	
LAN Switch mode	SWITCH@	
LAN RTL8106E-CG	8106ELDO@	
LAN RTL8111GS-CG	8111GLDO@	
LAN RTL8106EUS-CG	8106ESW@	
LAN RTL8111GUS-CG	8111GSW@	
Audio_233	233@	
Audio_233VB	233VB@	
For B15	Docking@	
For B14, E14	NoDocking@	
For Deep Sleep	DS3@	
For No Deep Sleep	NoDS3@	
WLAN Support ISCT	ISCT@	
WLAN No Support ISCT	NoISCT@	
For Intel ZERO ODD	ZODD@	
For No Intel ZERO ODD	NoZODD@	
For Green CLK	GCLK@	
For No Green CLK	NoGCLK@	
For No Green CLK	NoGCLKDIS@	Only in DIS Schematic
Green CLK IC For DIS	GCLKDIS@	
Green CLK IC For UMA	GCLKUMA@	
GPU support Dual Rank	DR@	Only in DIS Schematic
GPU Jet LE	JET@	
GPU Topaz XT	TOPAZ@	
For DIS	PX@	
For UMA	UMA@	
Camera	COMS@	
APS (G-sensor)	GS@	
Touch Screen	TS@	
HDMI	HDMI@	
USB 2.0	USB2@	
USB 3.0	USB3@	
Full HD Panel (2 Lane)	FHD@	
ENE EC 9012	9012@	
HDMI Royalty	45@	
Connector	ME@	No USE
VRAM indentify	X76@	
Un-pop component for EMI	@EMI@	
Un-pop component for ESD	@ESD@	
DA600140000	PCB_14_DIS@	
DA600141000	PCB_14_UMA@	
DA600140100	PCB_15_DIS@	
DA600141100	PCB_15_UMA@	

EC SM Bus1 address

Device	Address
Smart Battery	0001 011x

EC SM Bus2 address

Device	Address
Thermal Sensor	0100 1100

PCH SM Bus address

Device	Address	
DDR_JDIMM1	1010 000x	A0h
DDR_JDIMM2	1010 010x	A4h

AMD-GPU SM Bus address

Device	Address	
Internal thermal sensor	0100 0001	41h

SMBUS Control Table

	SOURCE	VGA	BATT	KB9012	SODIMM	WLAN	Thermal Sensor	PCH
SMB_EC_CK1 SMB_EC_DA1	KB9012 +3VALW	X	V +3VALW	X	X	X	X	X
SMB_EC_CK2 SMB_EC_DA2	KB9012 +3VS	V +3VGS	X	X	X	X	V +3VS	V +3VALW
PCH_SMBCLK PCH_SMBDATA	PCH +3VALW	X	X	X	V +3VS	V +3VS	X	X
PCH_SML0CLK PCH_SML0DATA	PCH +3VALW	X	X	X	X	X	X	X
SML1CLK SML1DATA	PCH +3VALW	V +3VGS	X	V +3VS	X	X	V +3VS	X

STATE \ SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON	HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)	LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)	LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)	LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)	LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

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Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	Notes List		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 3 of 55		

Topaz XT_VRAM_STRAP

		X76@ Vendor (UV5, UV6, UV7, UV8)	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	X76@ R_pd RV24
2GBytes	ZZZ01 TH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ02 TS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	1	0	0	1	8.45K	2K
1GBytes	ZZZ03 TM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	2	0	1	0	4.53K	2K
1GBytes	ZZZ04 TH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ05 TM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ06 TS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	5	1	0	1	3.24K	5.62K
1GBytes	ZZZ07 TM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	6	1	1	0	3.4K	10K
2GBytes	ZZZ08 TM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	7	1	1	1	4.75K	NC

ZZZ01 TH2G@ 2G HYNIX X7653638L01 | ZZZ02 TS1G@ 1G SAMSUNG X7653938L03 | ZZZ03 TM1G@ 1G MICRON X7653938L02 | ZZZ04 TH1G@ 1G HYNIX X7653938L01

Jet LE_VRAM_STRAP

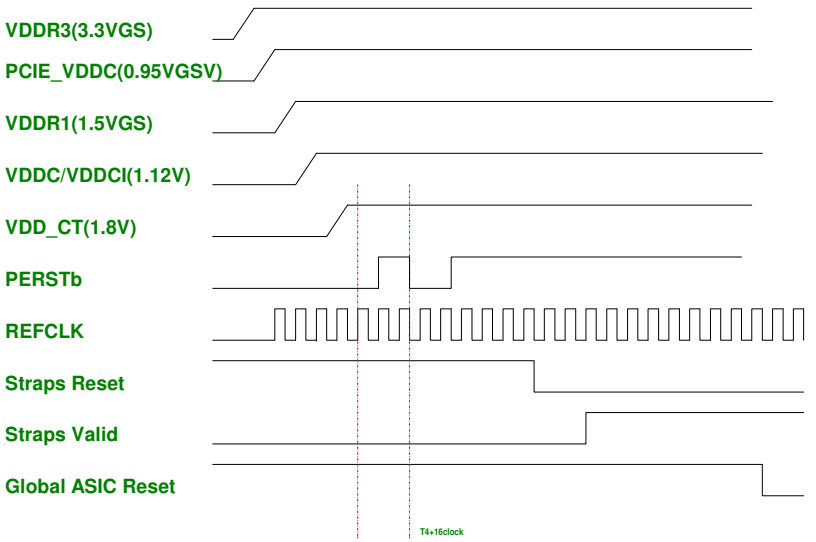
		X76@ Vendor (UV5, UV6, UV7, UV8)	ID	PS_3[3]	PS_3[2]	PS_3[1]	X76@ R_pu RV21	X76@ R_pd RV24
1GBytes	ZZZ09 JH1G@	Hynix 2048Mbits SA00006H400 128Mx16 H5TC2G63FFR-11C	0	0	0	0	NC	4.75K
1GBytes	ZZZ10 JM1G@	Micron 2048Mbits SA000067500 128Mx16 MT41J128M16JT-093G:K	1	0	0	1	8.45K	2K
1GBytes	ZZZ11 JS1G@	Samsung 2048Mbits SA000068U40 128Mx16 K4W2G1646Q-BC1A	2	0	1	0	4.53K	2K
2GBytes	ZZZ12 JH2G@	Hynix 4096Mbits SA00006E800 256Mx16 H5TC4G63AFR-11C	3	0	1	1	6.98K	4.99K
2GBytes	ZZZ13 JS2G@	Samsung 4096Mbits SA000076P00 256Mx16 K4W4G1646D-BC1A	4	1	0	0	4.53K	4.99K
2GBytes	ZZZ14 JM2G@	Micron 4096Mbits SA000077K00 256Mx16 MT41J256M16HA-093G:E	5	1	0	1	3.24K	5.62K
2GBytes	ZZZ08 JM2G2@	Micron 4096Mbits SA000065D00 256Mx16 MT41K256M16HA-107G:E	6	1	1	0	3.4K	10K
1GBytes	ZZZ16 JM1G2@	Micron 2048Mbits SA00005XB00 128Mx16 MT41K128M16JT-107G:K	7	1	1	1	4.75K	NC

ZZZ09 JH1G@ 1G HYNIX X7653638L07 | ZZZ10 JM1G@ 1G MICRON X7653638L08 | ZZZ11 JS1G@ 1G SAMSUNG X7653638L09 | ZZZ12 JH2G@ 2G HYNIX X7653638L04

Power-Up/Down Sequence

"Mars" has the following requirements with regards to power-supply sequencing to avoid damaging the ASIC:

- All the ASIC supplies must reach their respective nominal voltages within 20 ms of the start of the ramp-up sequence, though a shorter ramp-up duration is preferred. The maximum slew rate on all rails is 50 mV/µs.
- The external pull ups on the DDC/AUX signals (if applicable) should ramp up before or after both VDDC and VDD_CT have ramped up.
- VDDC and VDD_CT should not ramp up simultaneously. For example, VDDC should reach 90% before VDD_CT starts to ramp up (or vice versa).
- For power down, reversing the ramp-up sequence is recommended.



R_pu (Ω)	R_pd (Ω)	Bits [3:1]
NC	4750	000
8450	2000	001
4530	2000	010
6980	4990	011
4530	4990	100
3240	5620	101
3400	10000	110
4750	NC	111

Note: 0402 1% resistors are required.

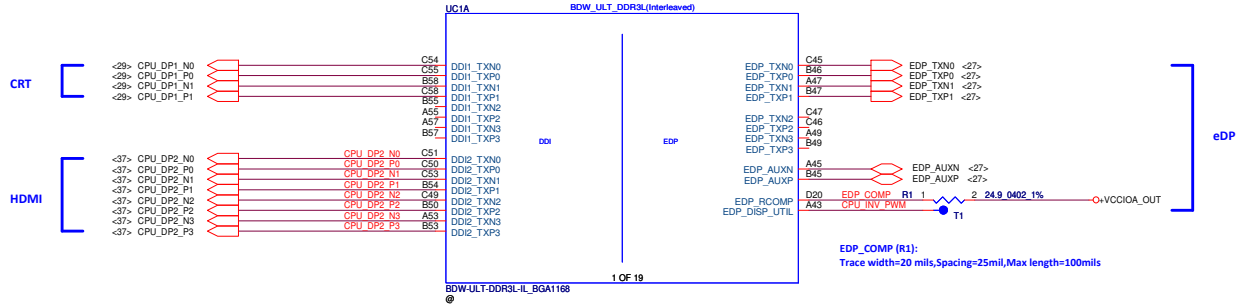
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	VGA Notes List		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 4 of 55		

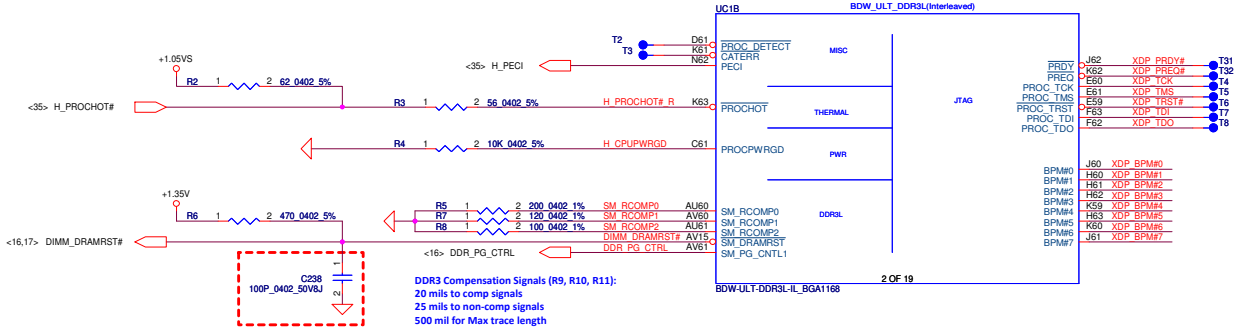
DAZ
DA600140000
PCB 14I LA-B091P REV0 M/B DIS 3
PCB_14_DIS@

DAZ
DA600140100
PCB 14K LA-B091P REV0 M/B DIS 6
PCB_15_DIS@

DAZ
DA600141000
PCB 14I LA-B092P REV0 M/B UMA 3
PCB_14_UMA@

DAZ
DA600141100
PCB 14K LA-B092P REV0 M/B UMA 6
PCB_15_UMA@





UC1
SA00007G020
Intel 2957U 1.4G 2M D0 2cBGA CPU
2957U@

UC1
SA00007G220
S IC CL8064701569500 QFAN D0 1.7G BGA
3558U@

UC1
SA00006SL70
S IC CL8064701477202 QEVD C0 1.8G BGA
i7_4500U@

UC1
SA00006SM80
S IC CL8064701477702 SR170 C0 1.6G C38!
i5_4200U@

UC1
SA00007AM00
S IC CL8064701614813 QFSY C0 1.6G BGA
QFSY@

UC1
SA00006SU50
S IC CL8064701476302 SR16P C0 1.8G C38!
i3_4100U@

UC1
SA000072Q70
S IC CL8064701478404 QEAR D0 1.7G C38
i3_4005U@

UC1
SA00006SX80
S IC CL8064701478202 SR16Q C0 1.7G C38!
i3_4010U@

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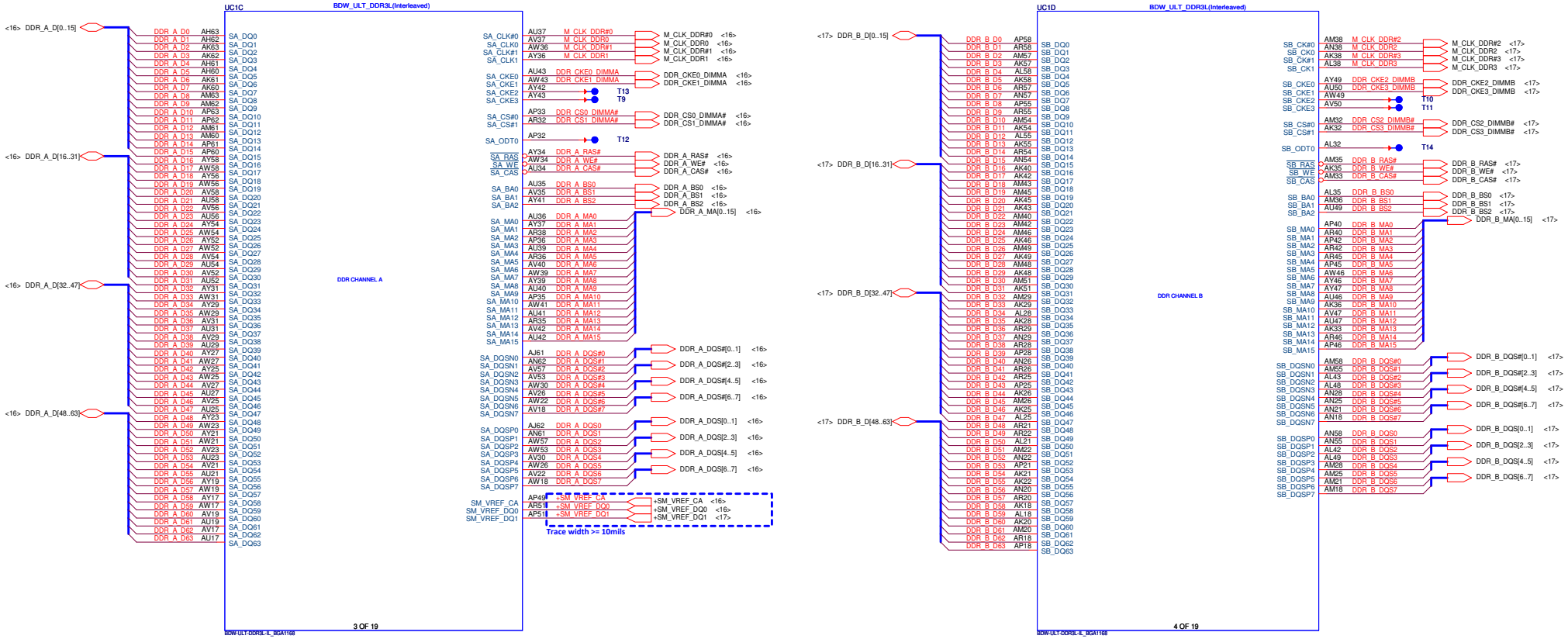
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(1/11) DDI,MSIC,XDP		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 5 of 55		

Interleaved Memory



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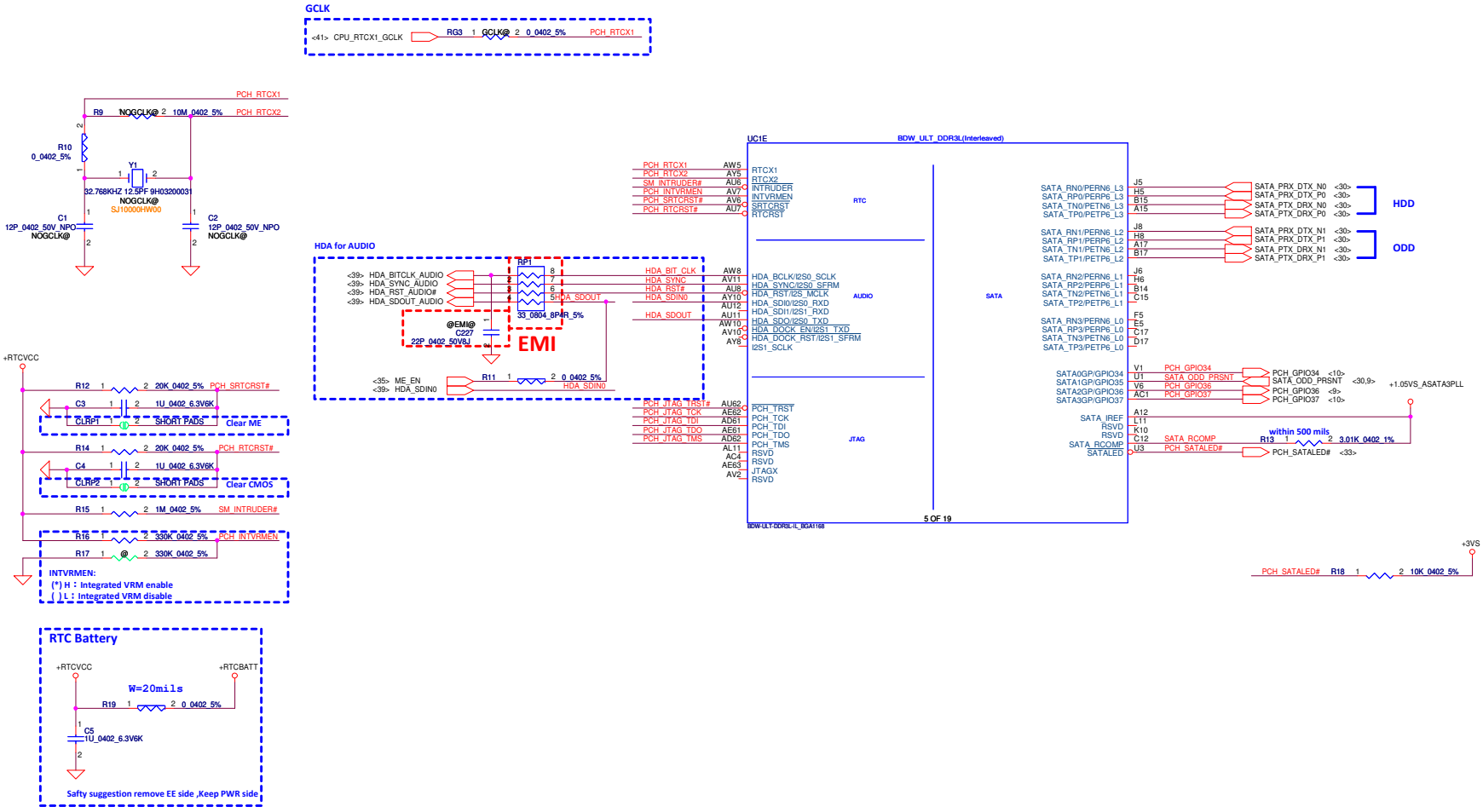
Issued Date	2011/06/24	Deciphered Date	2012/07/12
		Title	HSW MCP(2/11) DDRIII
		Size / Document Number	C / LA-B091P
		Rev	1.0
		Date: Wednesday, February 12, 2014	Sheet 6 of 55



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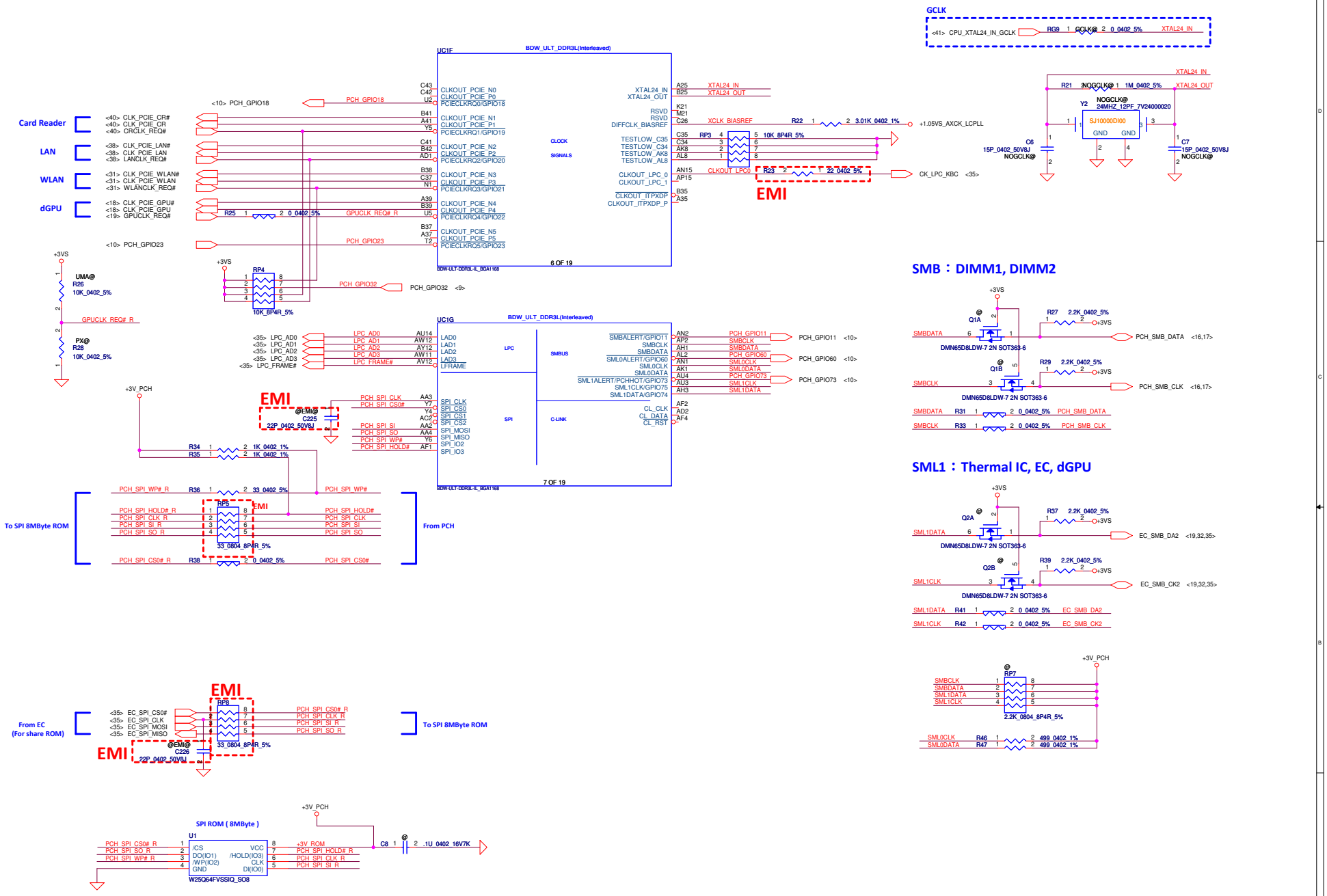
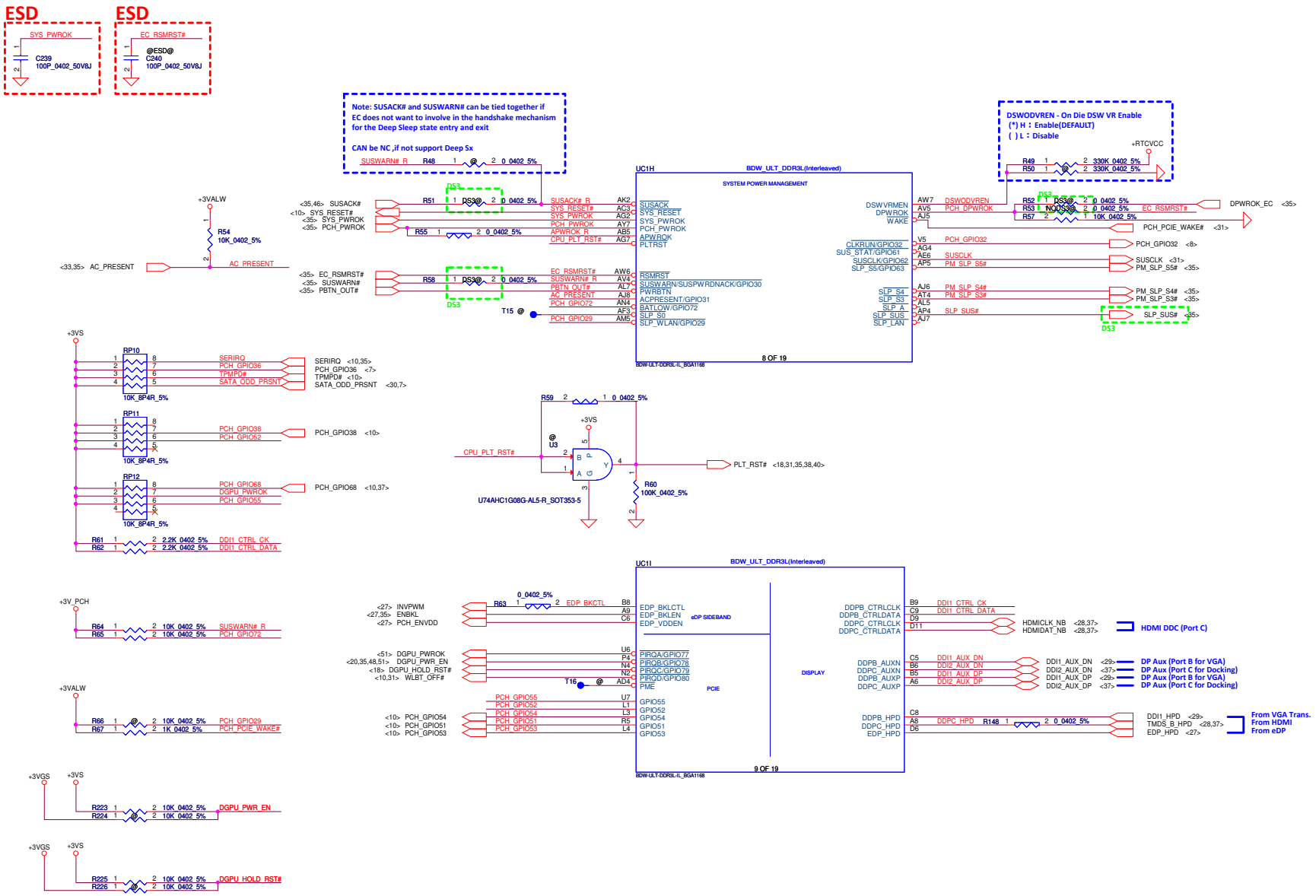
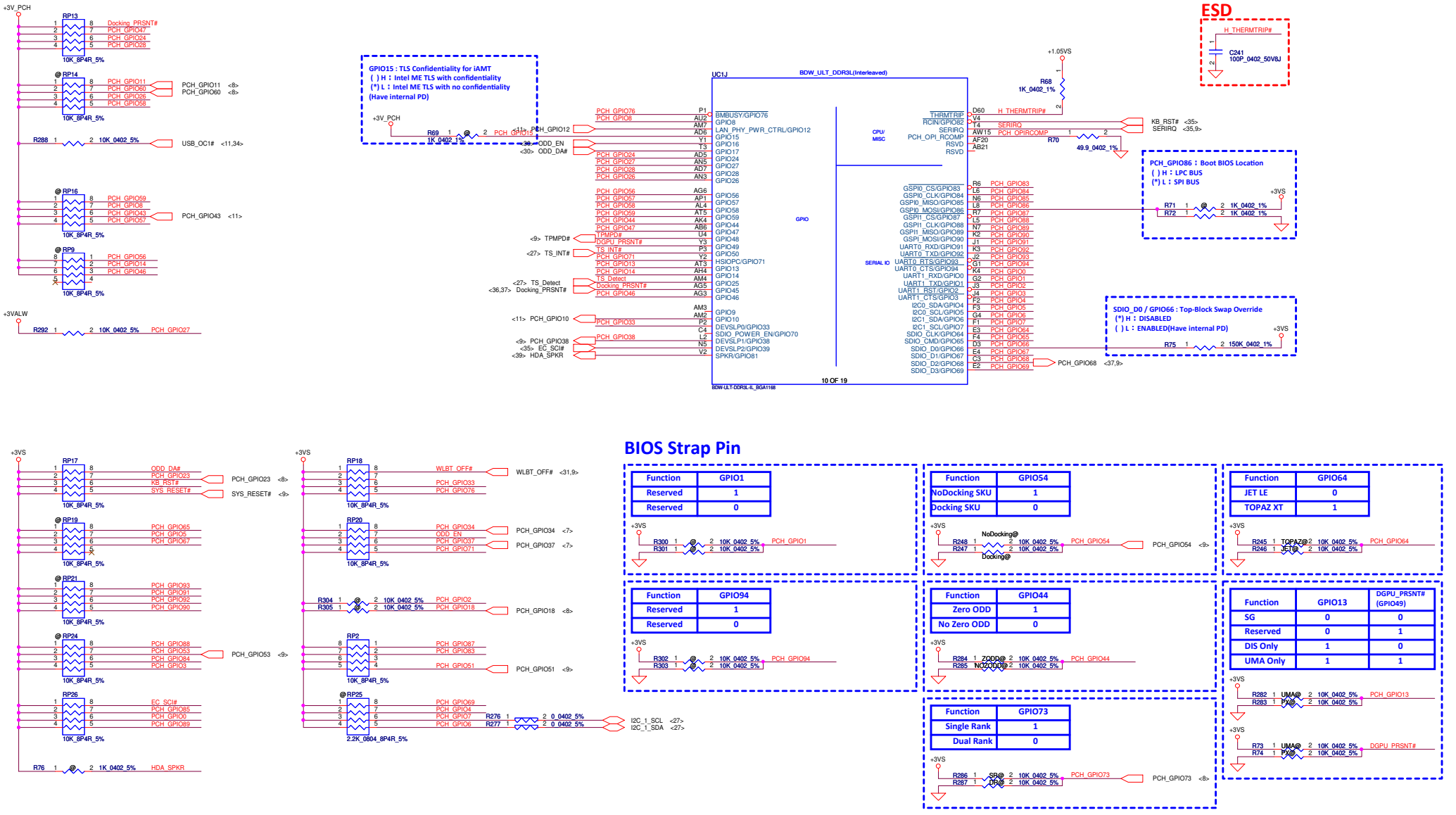
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(3/11) RTC,SATA,XDP		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 7 of 55		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(4/11) CLK,SPI,SMBUS		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 8 of 55		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(5/11) PM,GPIO,DDI		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 9 of 55		



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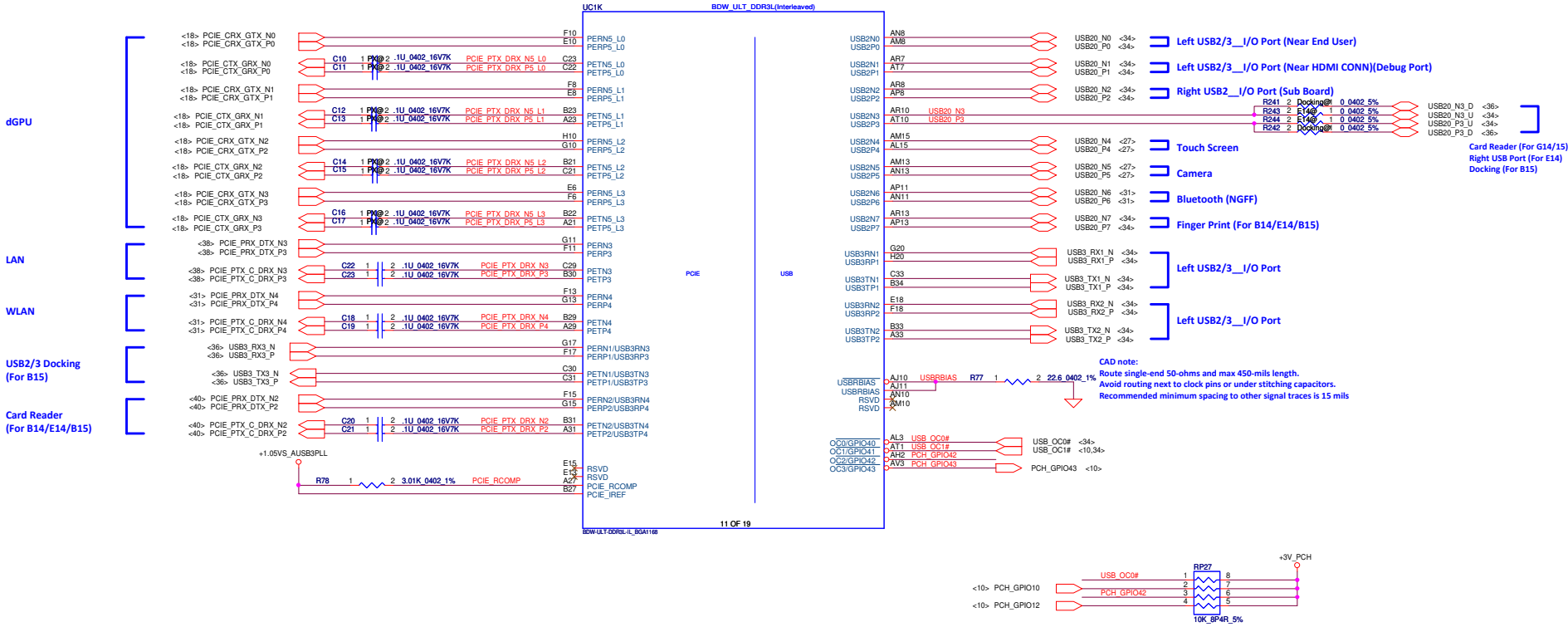
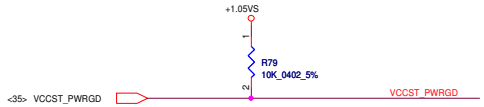
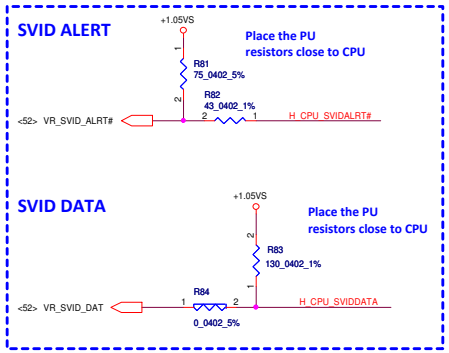
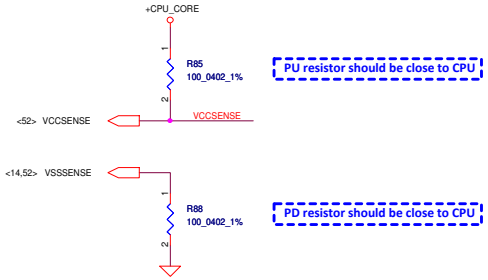
Compal Electronics, Inc.			
Title	HSW MCP(6/11) GPIO,LPIO		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 10 of 55		

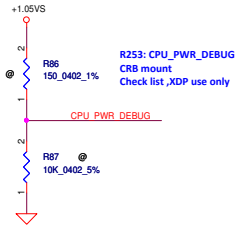


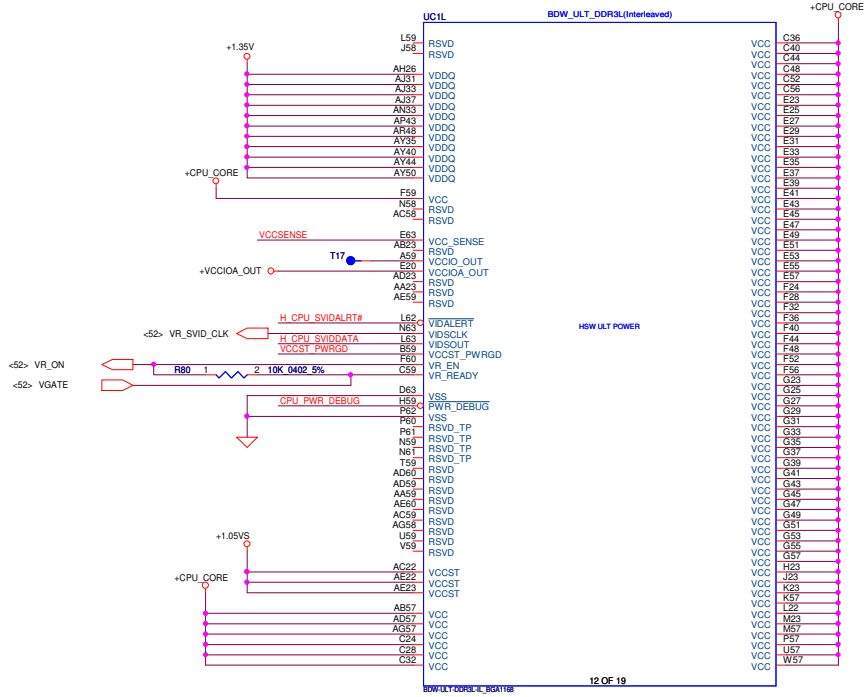
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(7/11) PCIE,USB		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 11 of 55		

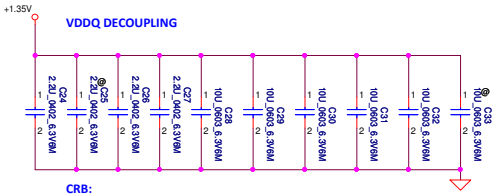












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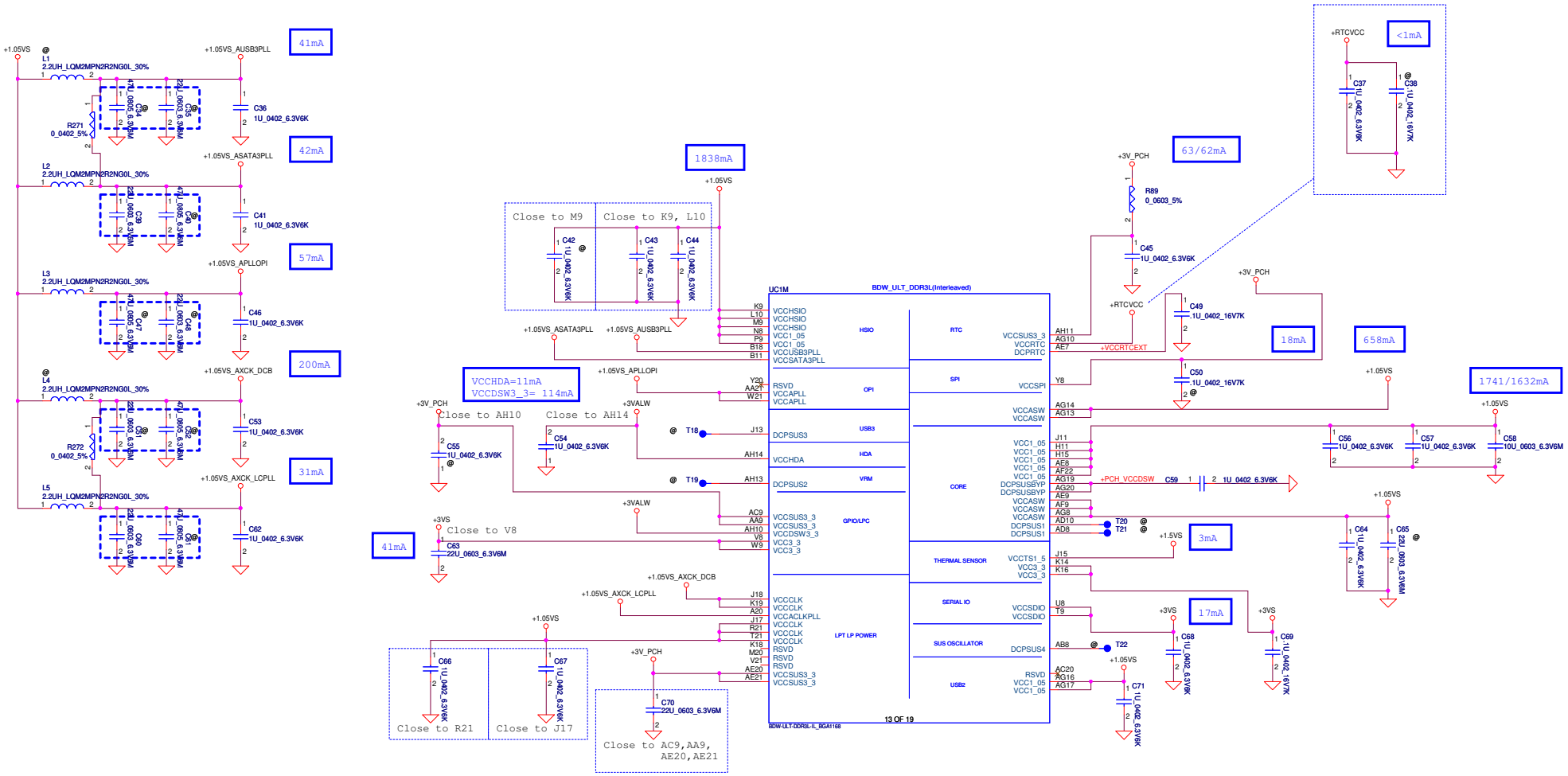
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(8/11) Power		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 12 of 55		



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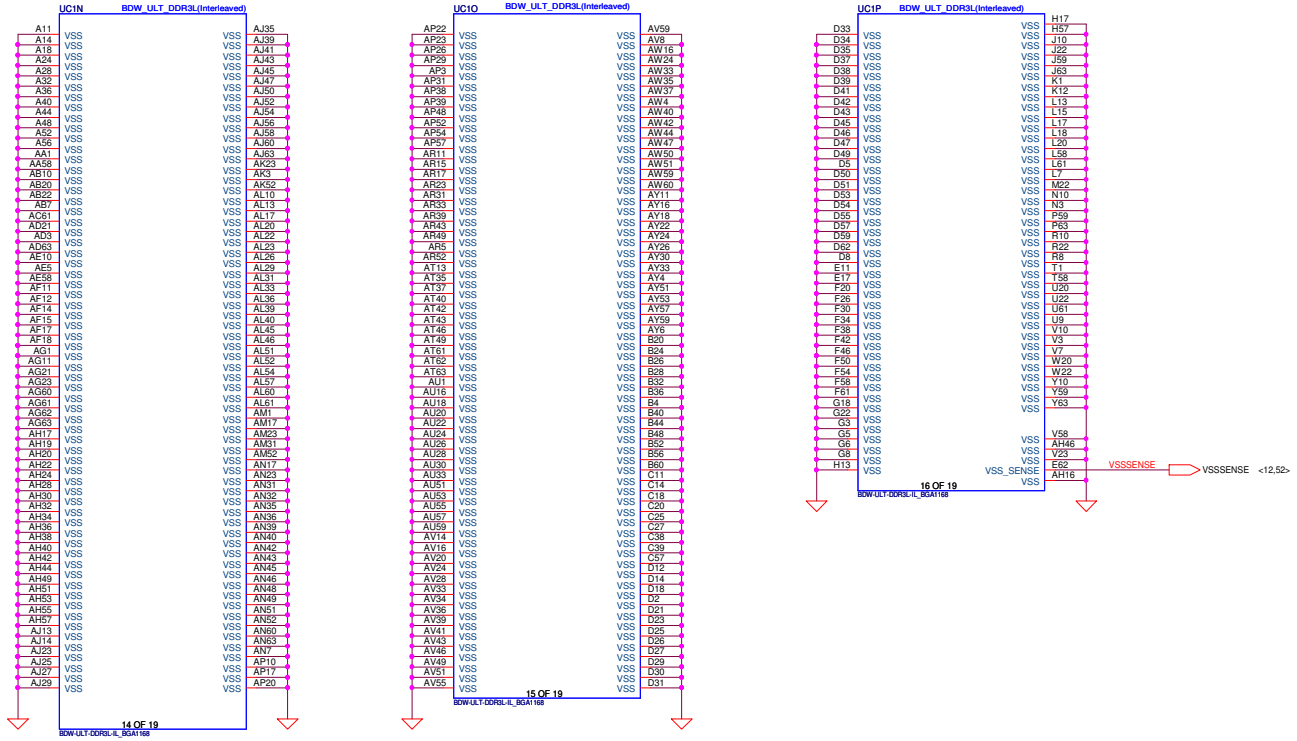
			Title: HSW MCP(9/11) Power
			Size: C; Document Number: LA-B091P; Rev: 1.0
			Date: Wednesday, February 12, 2014; Sheet 13 of 55



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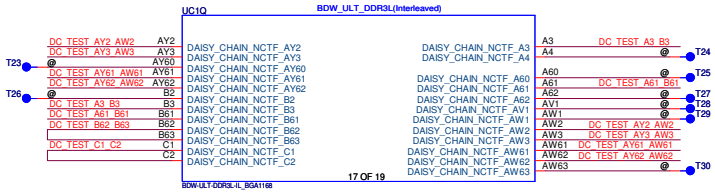
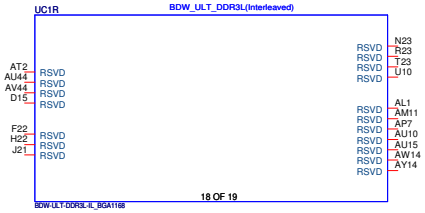
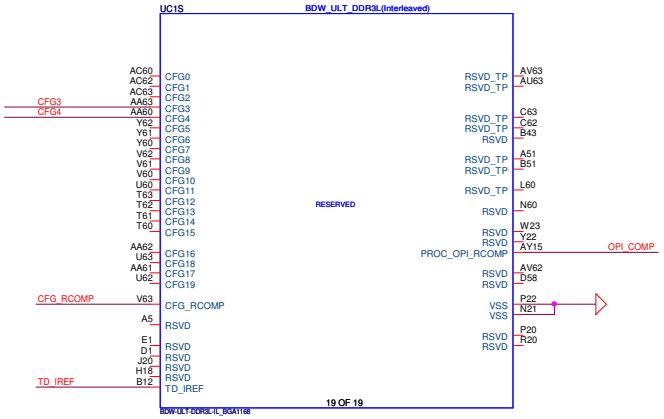
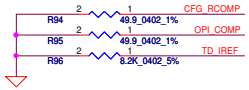
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HSW MCP(10/11) GND		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 14 of 55		

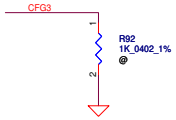




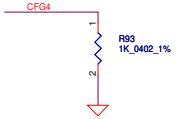




CFG Straps for Processor



Physical Debug Enable (DFX Privacy)	
CFG3	1: DISABLED 0: ENABLED; SET DFX ENABLED BIT IN DEBUG INTERFACE MSR



Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
		Title	HSW MCP(11/11) RSVD
		Size: C	Document Number: LA-B091P
		Date: Wednesday, February 12, 2014	Sheet 15 of 55

DIMM1 Reverse Type Near CPU

D/DQ Signals link to CPU
CMD Signals from CPU
Clock Signals from CPU
CTL Signals from CPU
SMBUS Signals link to CPU

Layout Note: Place near JDIMM1

Layout Note: Place near JDIMM1.203,204

Layout Note: Place near JDIMM1.199

Address : 00

ESD

DDR3L SODIMM ODT GENERATION

U4 74AUP1G07GW TSSOP 5P BUFFER

For ODT & VTT power control

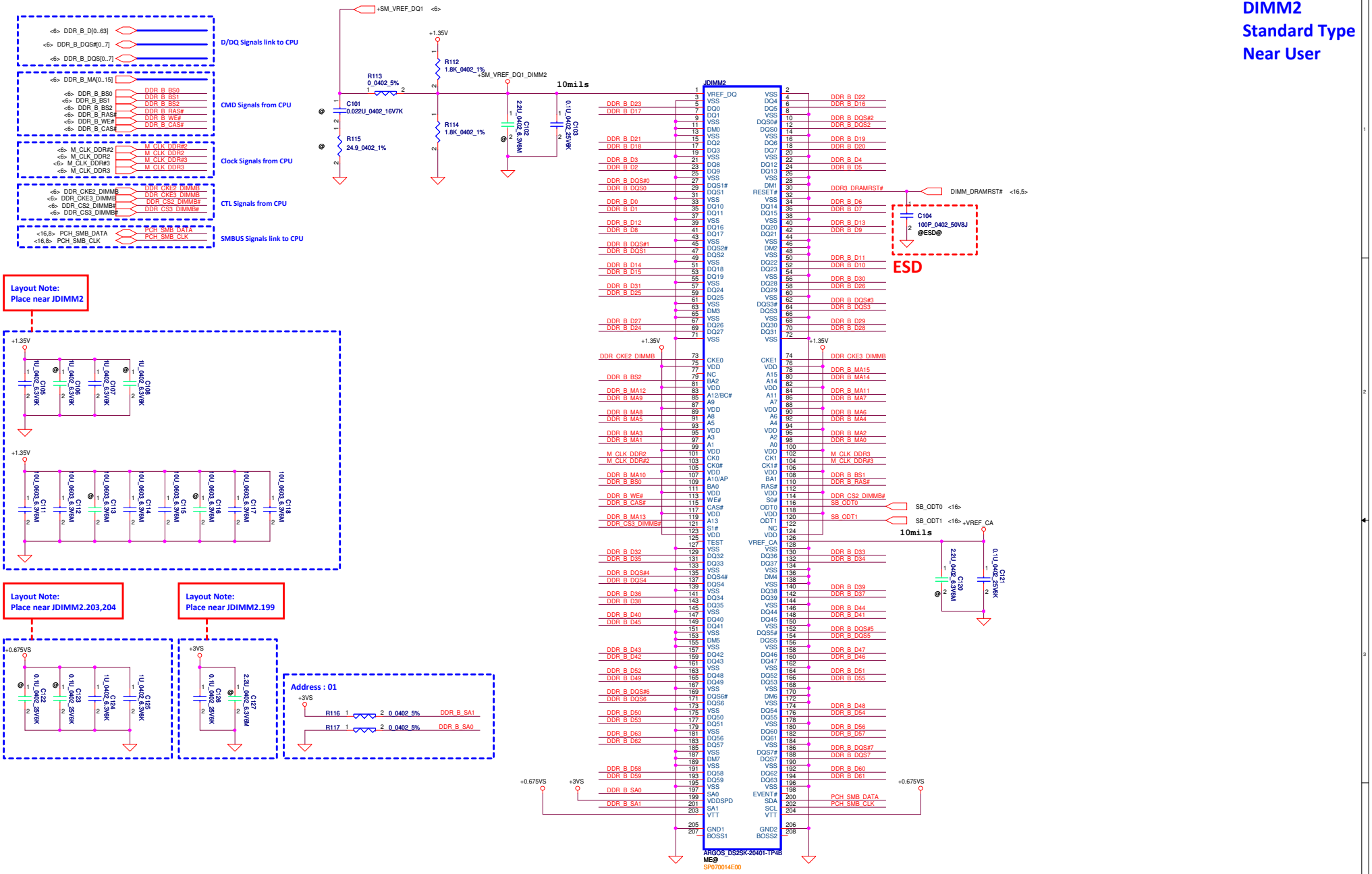
Q9 LBSS138LT1G_SOT-23-3

Interleaved Memory

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

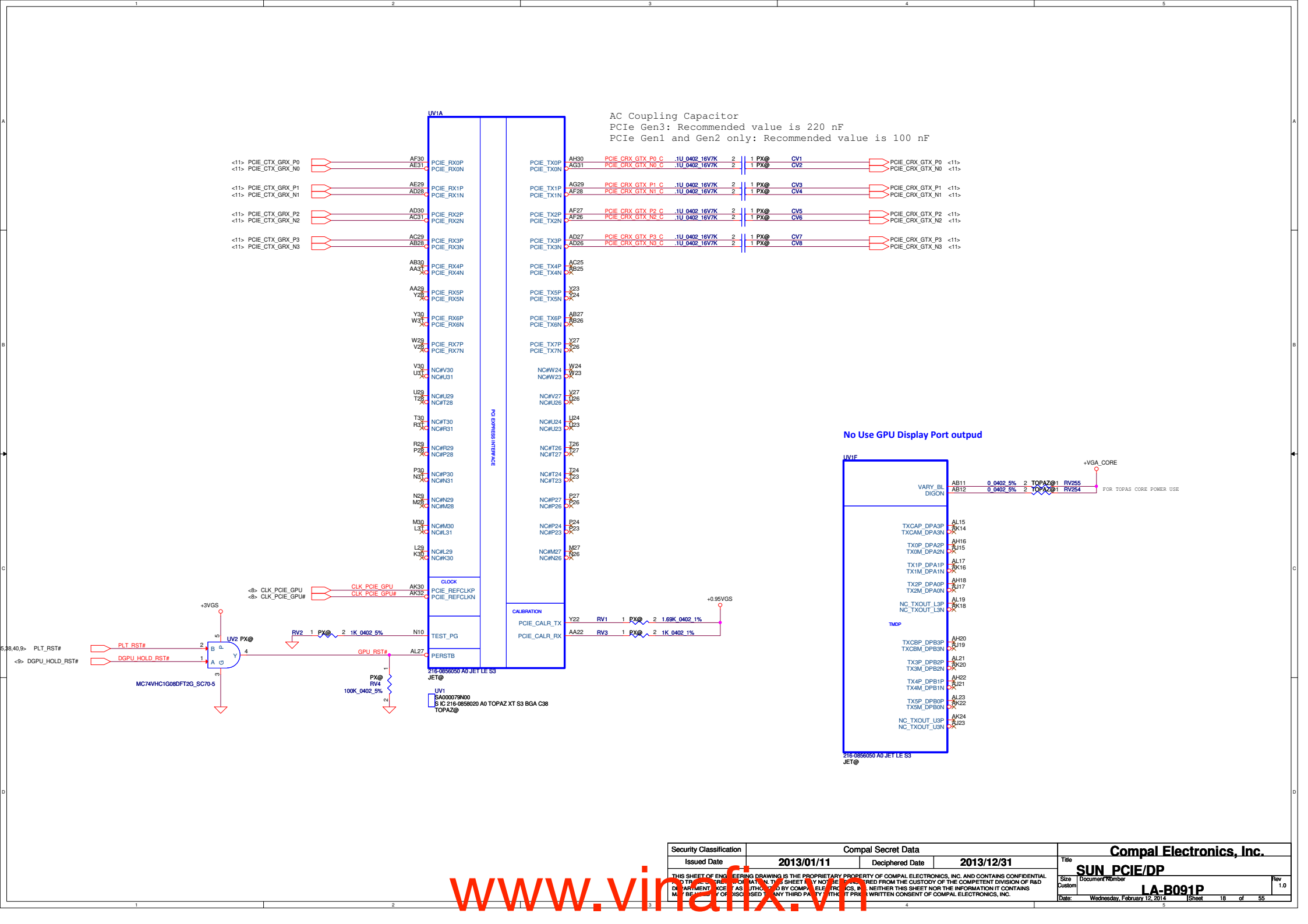
Compal Electronics, Inc.			
Title	DDR3L_DIMMA		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 16 of 55		

DIMM2
Standard Type
Near User



Interleaved Memory

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	DDR3L DIMMB		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 17 of 55		



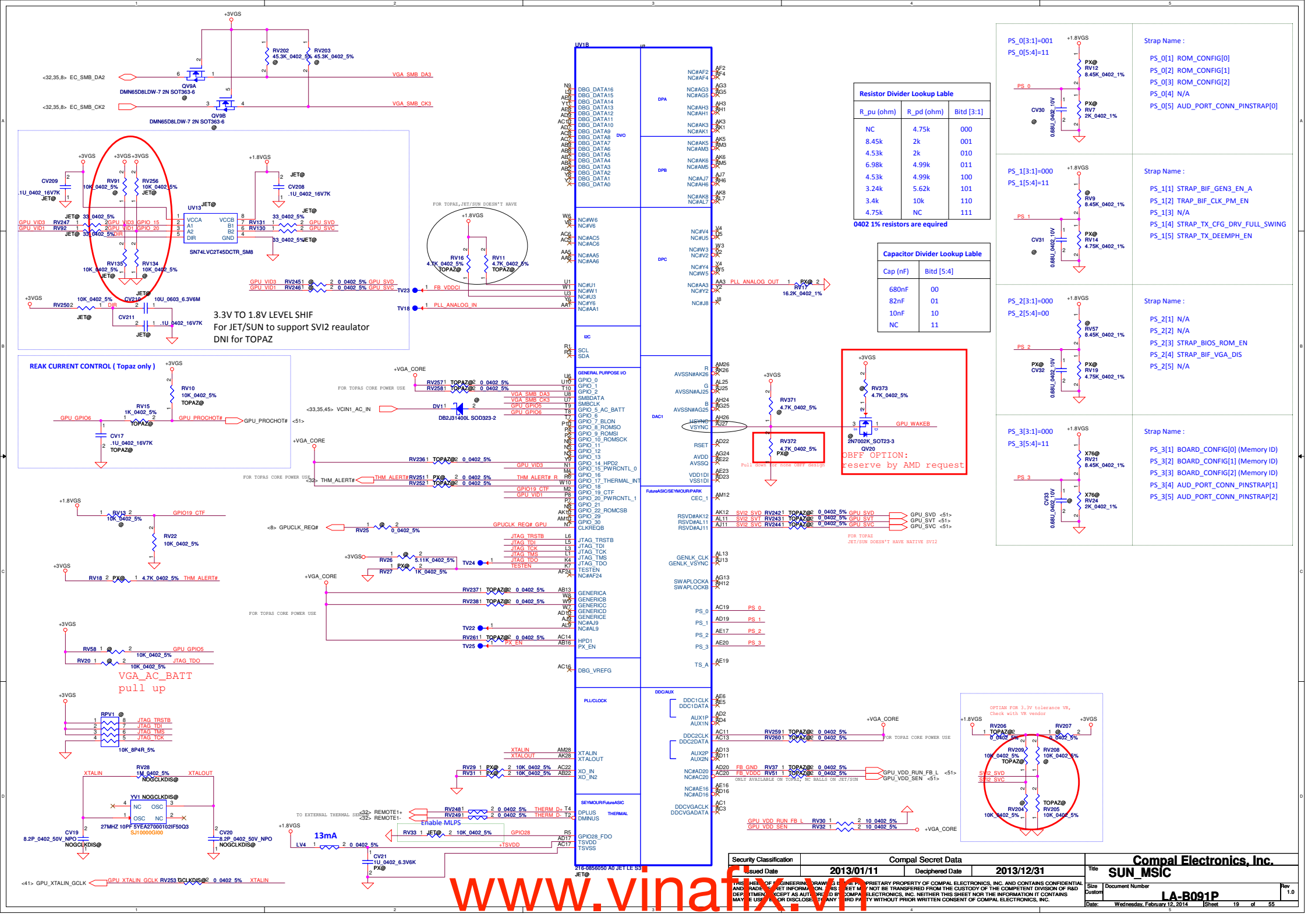
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_PCIE/DP

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 18 of 55



Resistor Divider Lookup Lable

R_pu (ohm)	R_pd (ohm)	Bitd [3:1]
NC	4.75k	000
8.45k	2k	001
4.53k	2k	010
6.98k	4.99k	011
4.53k	4.99k	100
3.24k	5.62k	101
3.4k	10k	110
4.75k	NC	111

0402 1% resistors are equired

Capacitor Divider Lookup Lable

Cap (nF)	Bitd [5:4]
680nF	00
82nF	01
10nF	10
NC	11

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

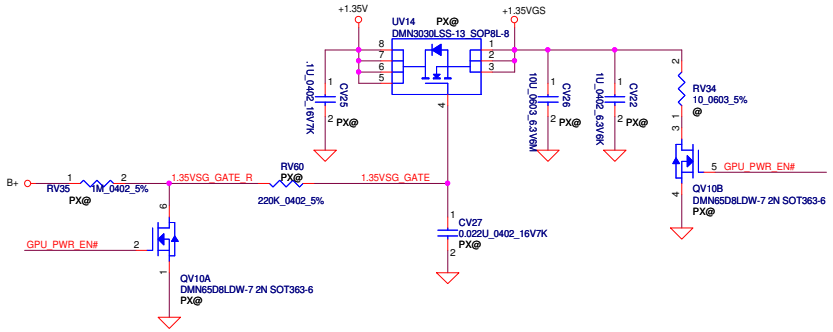
Compal Electronics, Inc.

Title: SUN_MSIC

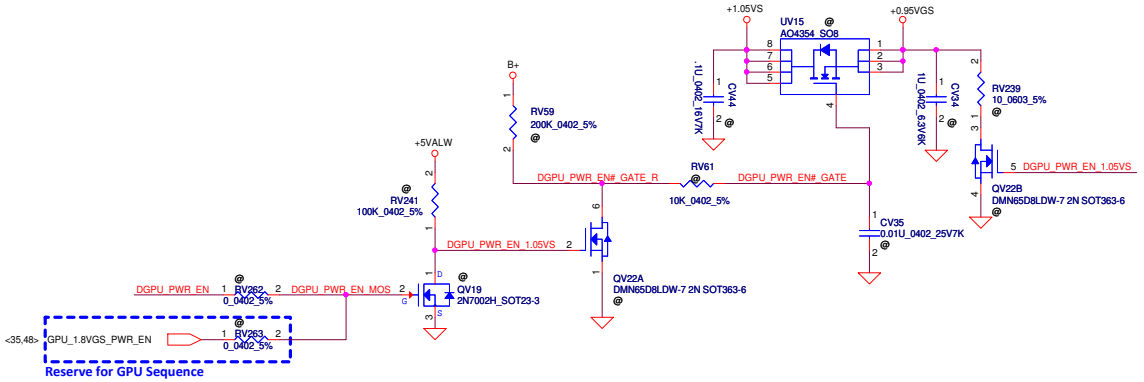
Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 19 of 55

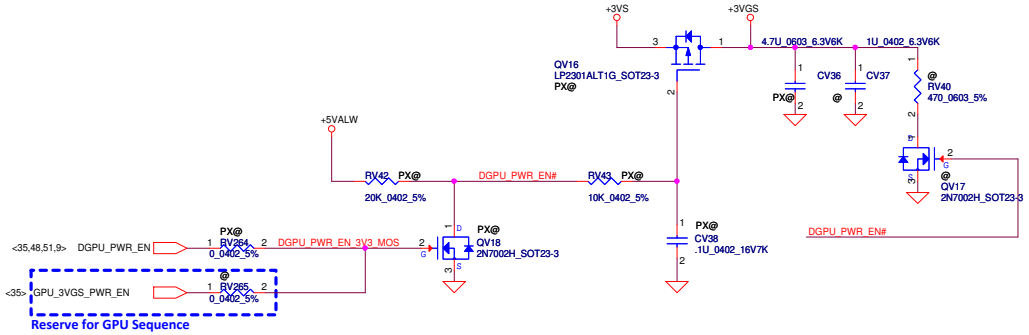
+1.35VS to +1.35VGS (6.234A)



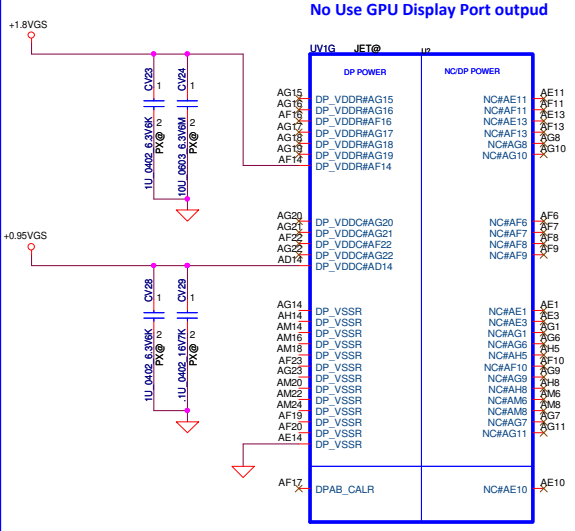
+1.05VS to +0.95VGS

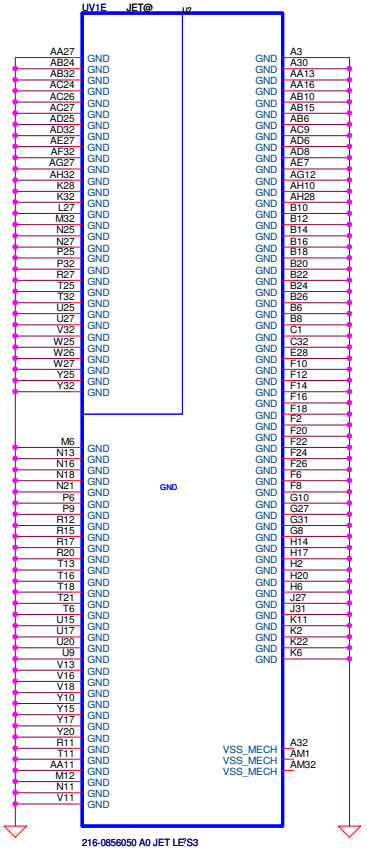


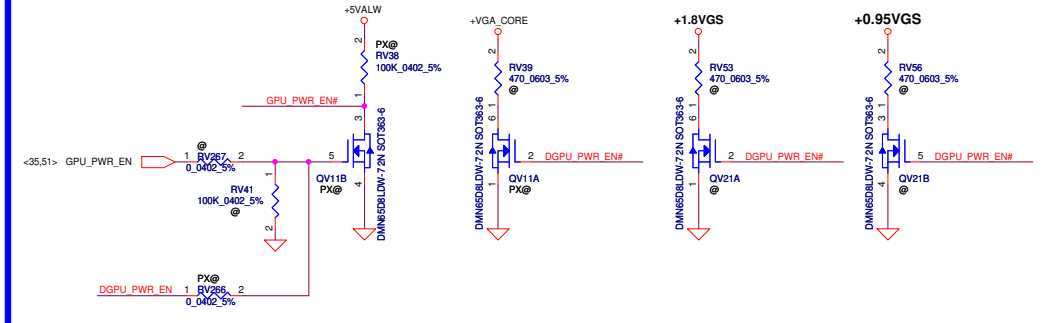
+3VS to +3VS_VGA (25mA)



No Use GPU Display Port outpud







Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power/GND

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 20 of 55

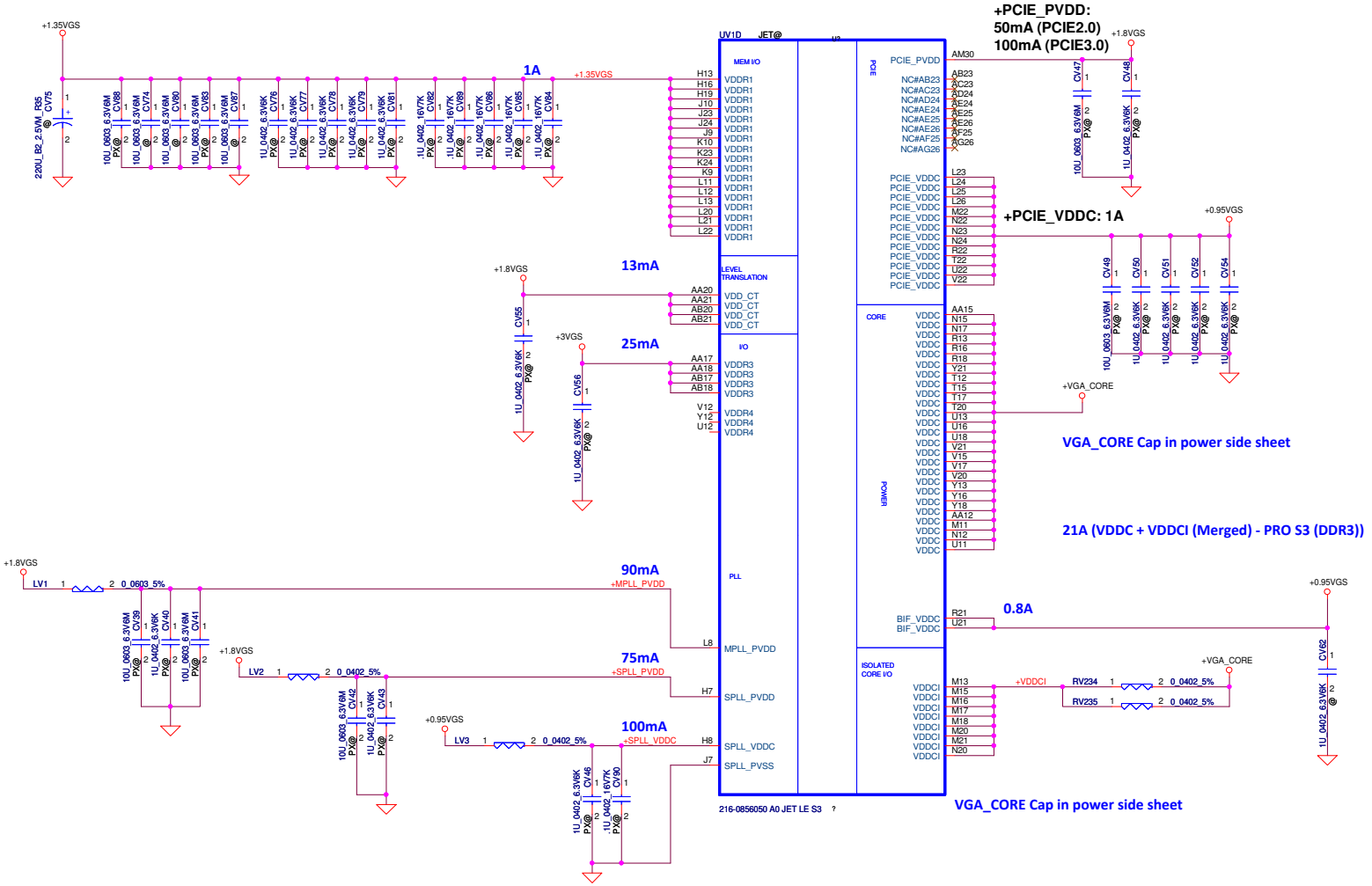
+VGA_CORE		10uF	2.2uF	1uF	0.1uF
VDDC	TBD	7	16	4	3
VDDCI	3.5A				

+0.95VGS		10uF	1uF	0.1uF
PCIE_VDDC	1A	1	5(1@)	0
BIF_VDDC	0.8A	0	1(1@)	0
SPLL_VDDC	100mA	0	1	1

+1.35VGS		10uF	1uF	0.1uF	0.01uF
VDDR1	1.5A	5(3@)	5	5	0

+1.8VGS		10uF	1uF	0.1uF
PCIE_PVDD	100mA	1	1	0
MPLL_PVDD	130mA	2	1	0
SPLL_PVDD	75mA	0	1	0
VDDR4	(300mA)	0	0	0
VDD_CT	13mA	0	1	0
+TSVDD	13mA	0	1	0
+DP_VDDR		1	1	0
+DP_VDDC		0	1	1

+3VGS		10uF	1uF	0.1uF
VDDR3	25mA	0	1	0



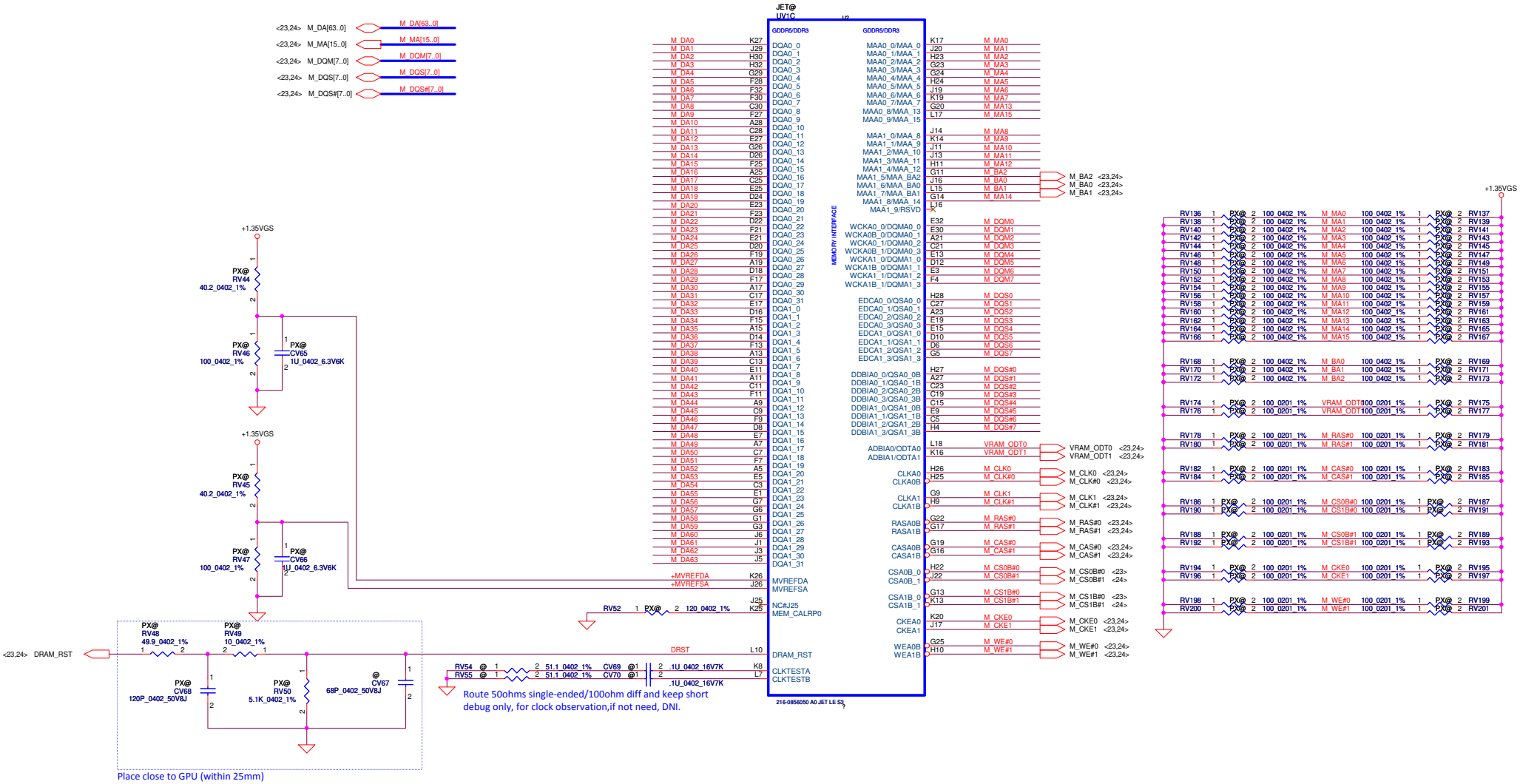
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_Power

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 21 of 55



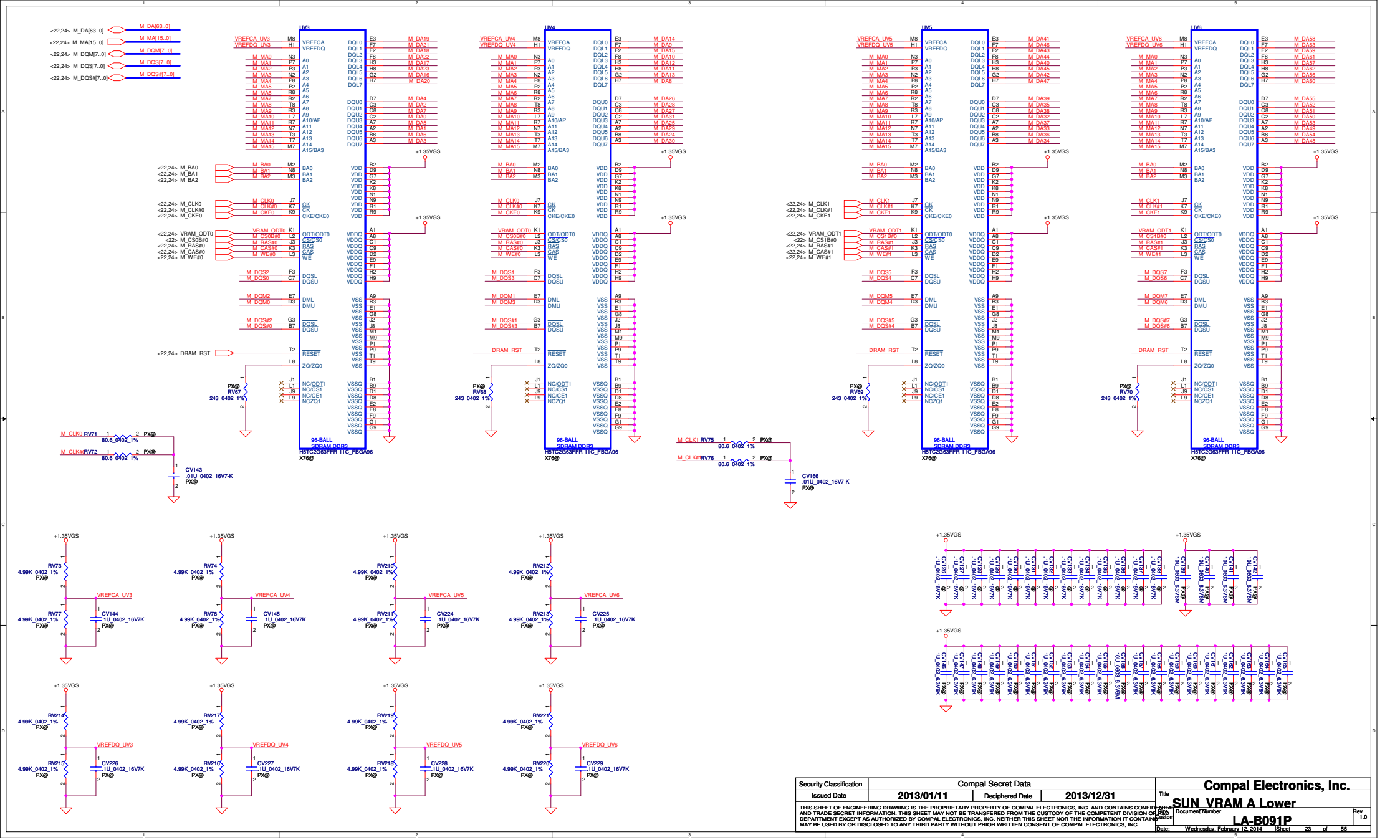
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_MEM

Size: Custom | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 22 of 55



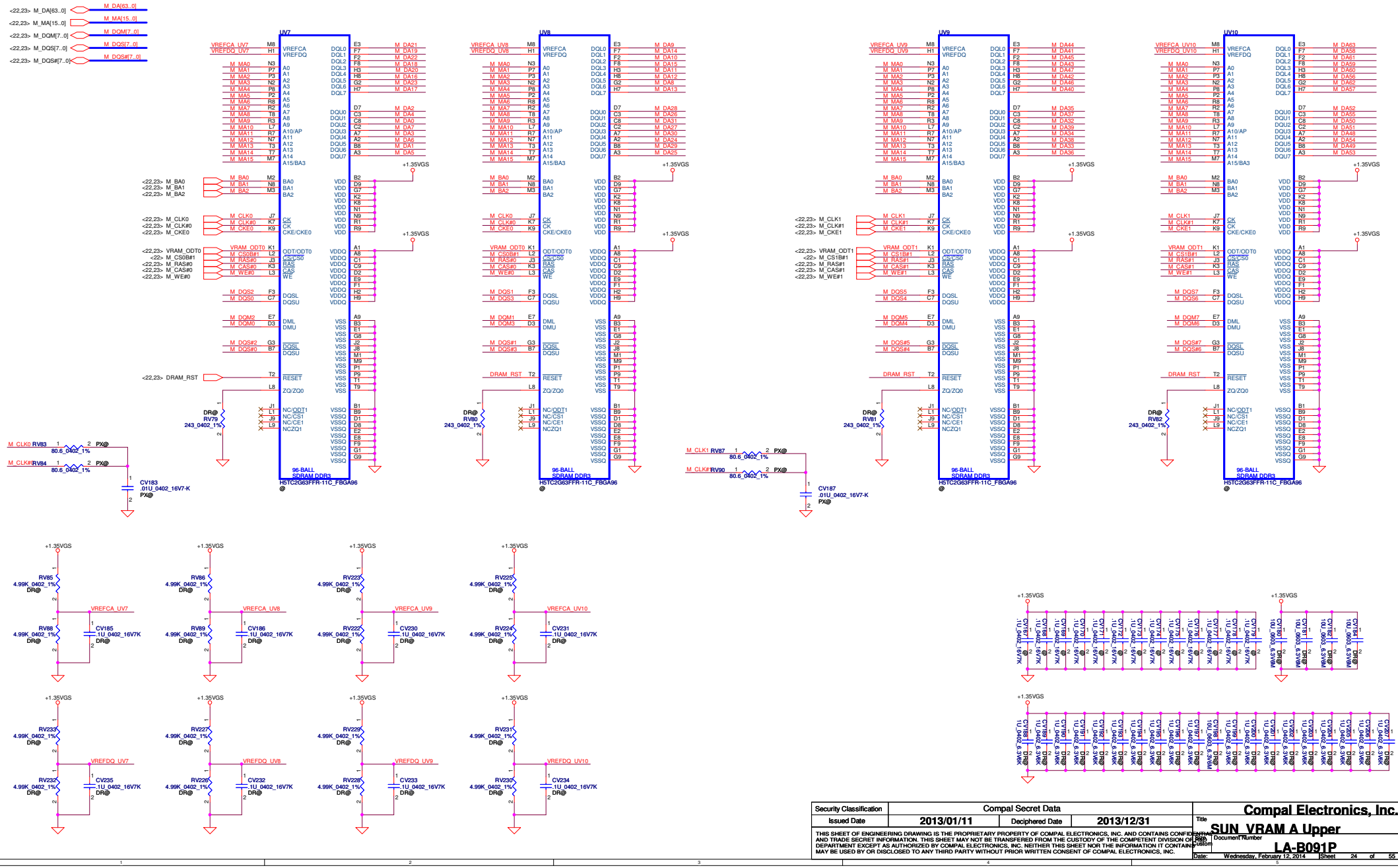
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_VRAM A Lower

Size: B | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 23 of 55



Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: SUN_VRAM A Upper

Size: B | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 24 of 55

Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_VRAM A Lower**

Size	Document Number	Rev
Custom	LA-B091P	1.0

Date: Wednesday, February 12, 2014 | Sheet 25 of 55

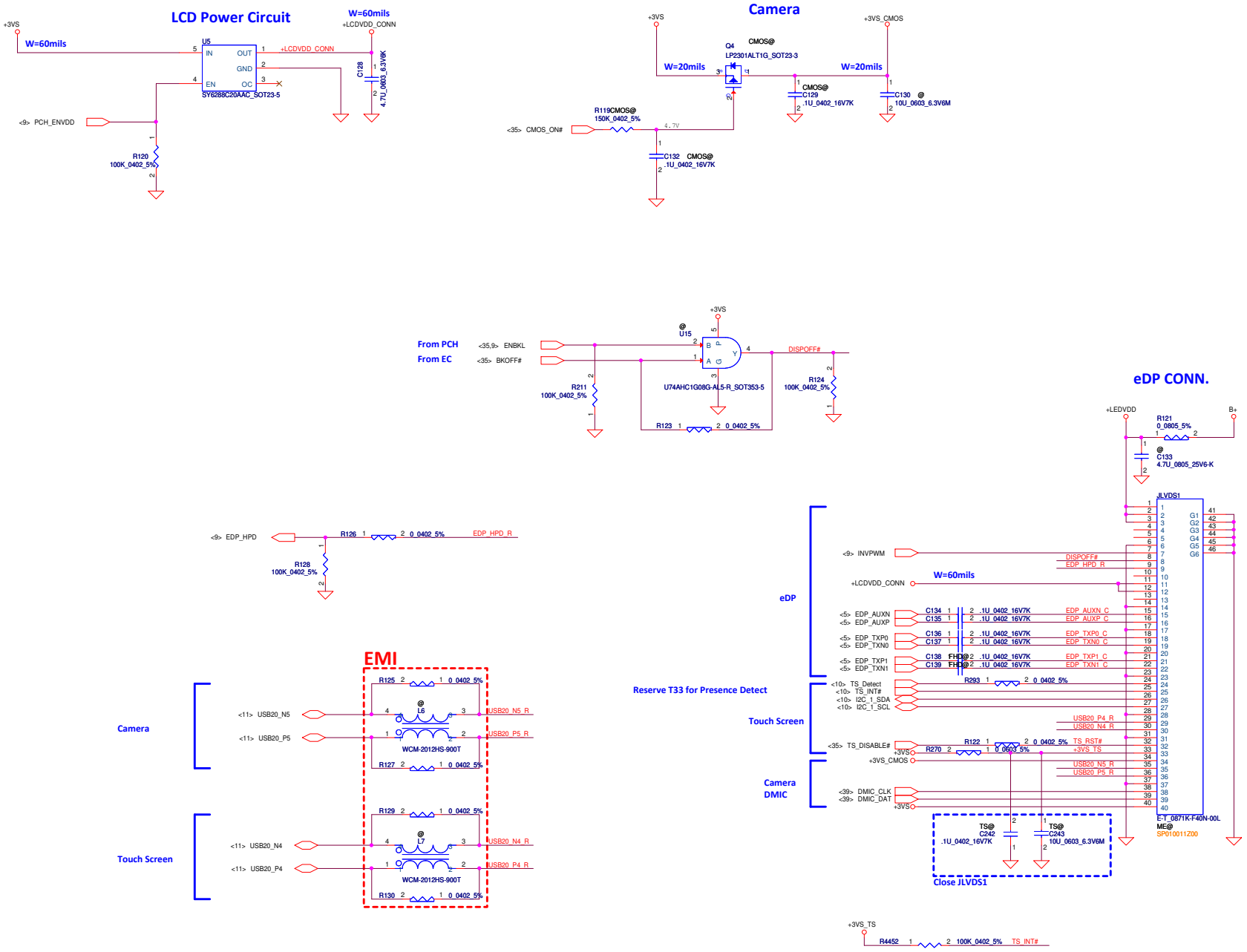
Security Classification	Compal Secret Data		
Issued Date	2013/01/11	Deciphered Date	2013/12/31

Compal Electronics, Inc.

Title: **SUN_VRAM A Upper**

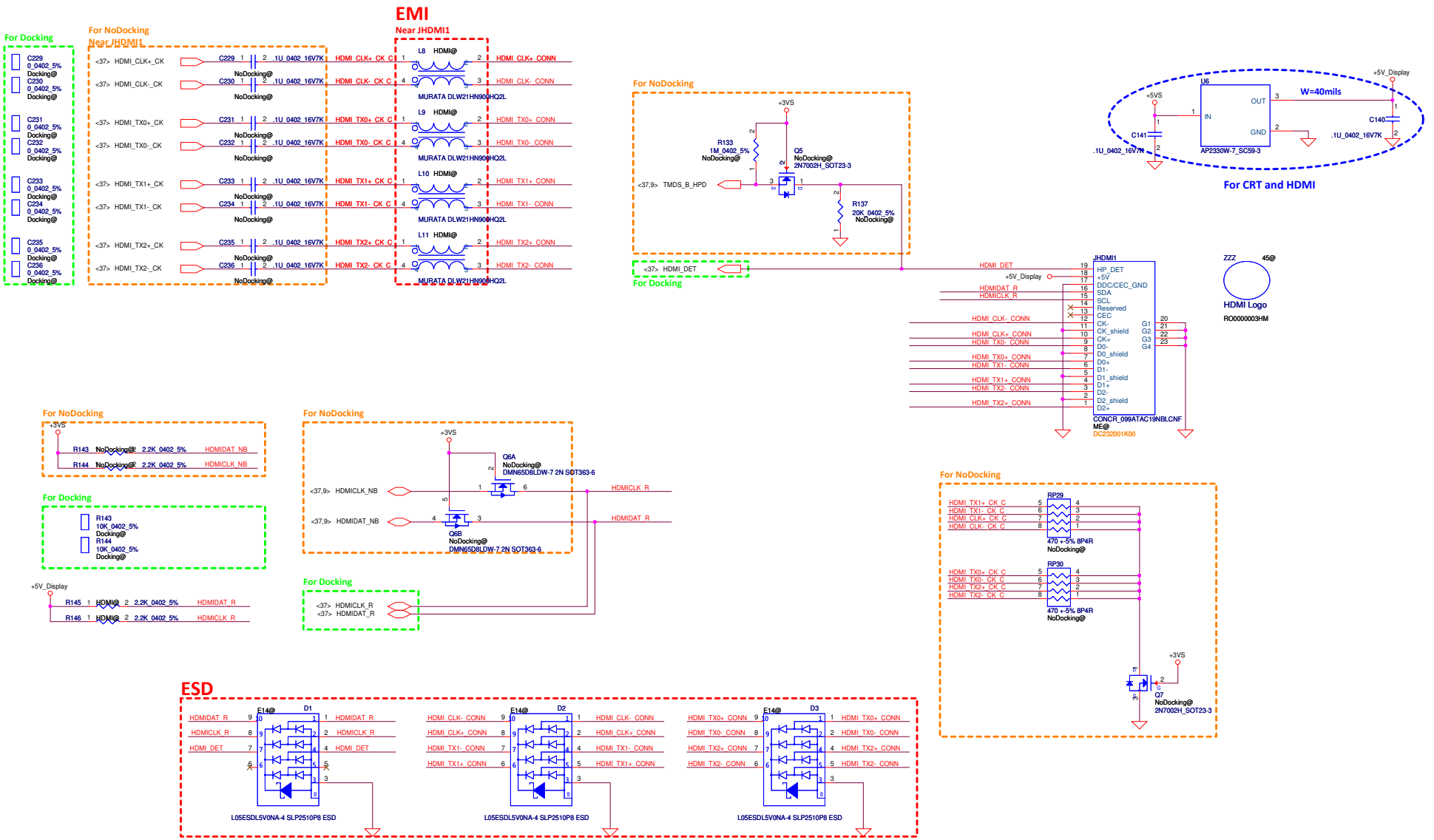
Size: Custom | Document Number: **LA-B091P** | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 26 of 55

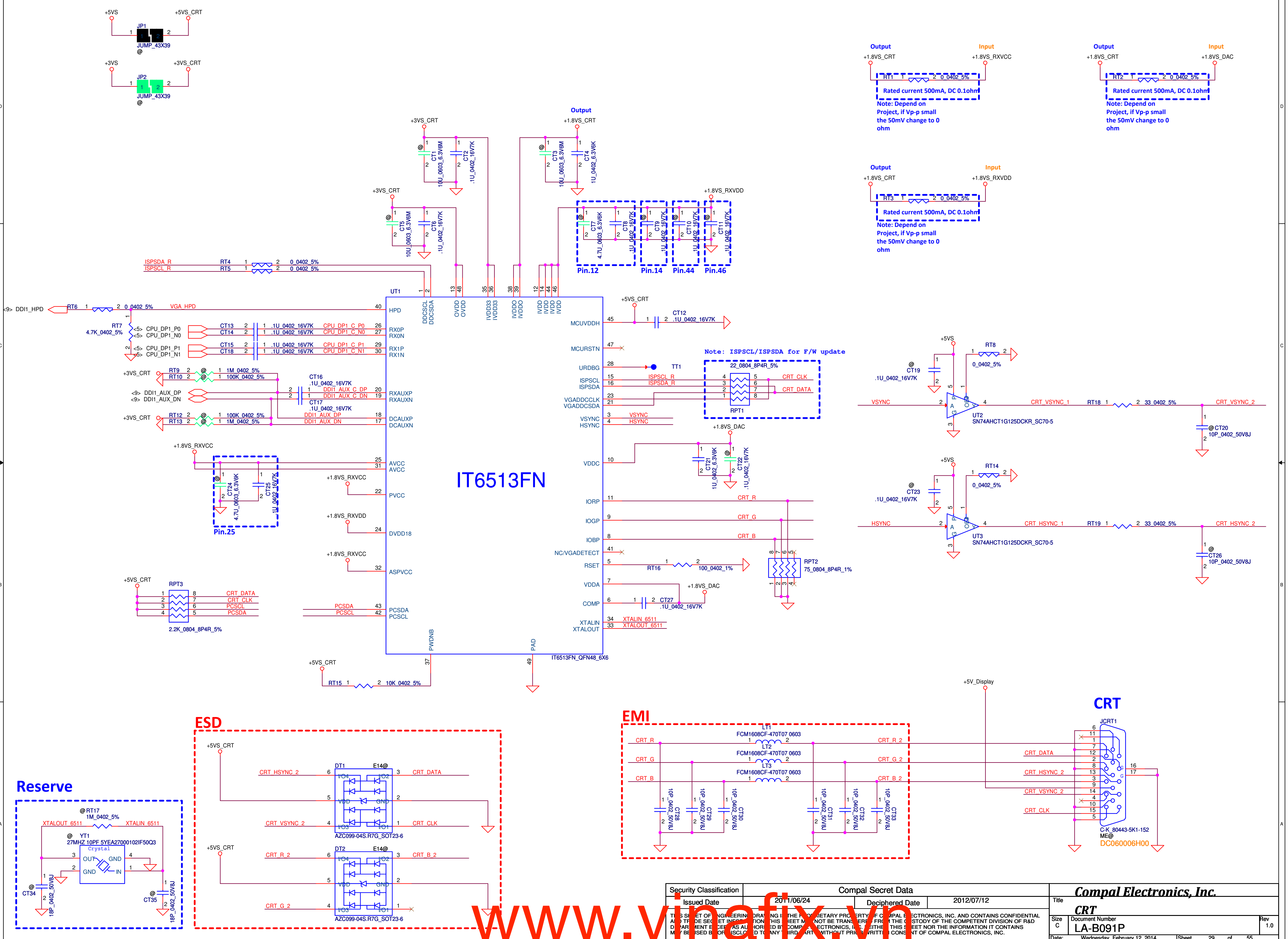


Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	LVDS/CAMERA		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 27 of 55		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HDMI CONN		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 28 of 55		



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

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Compal Electronics, Inc.

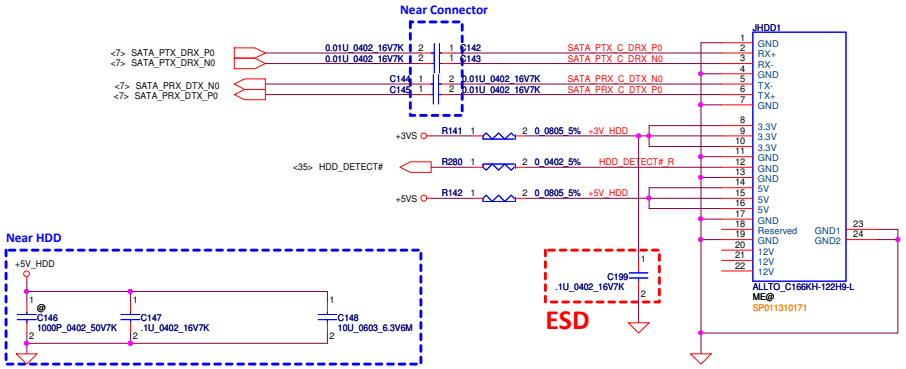
Title: CRT

Size: C | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 29 of 55

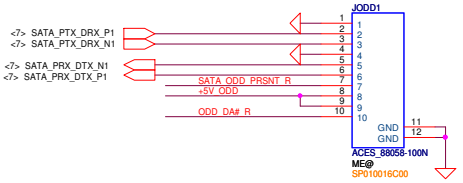
HDD

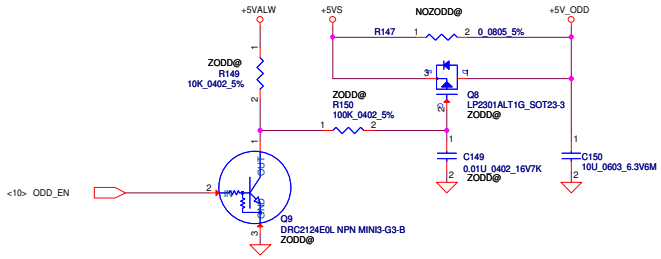
SATA HDD Conn.



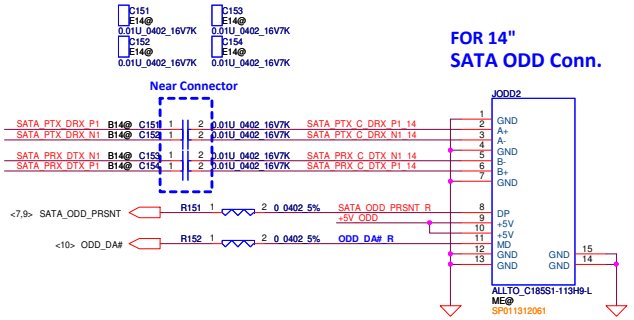
ODD

FOR 15" SATA ODD FFC Conn.





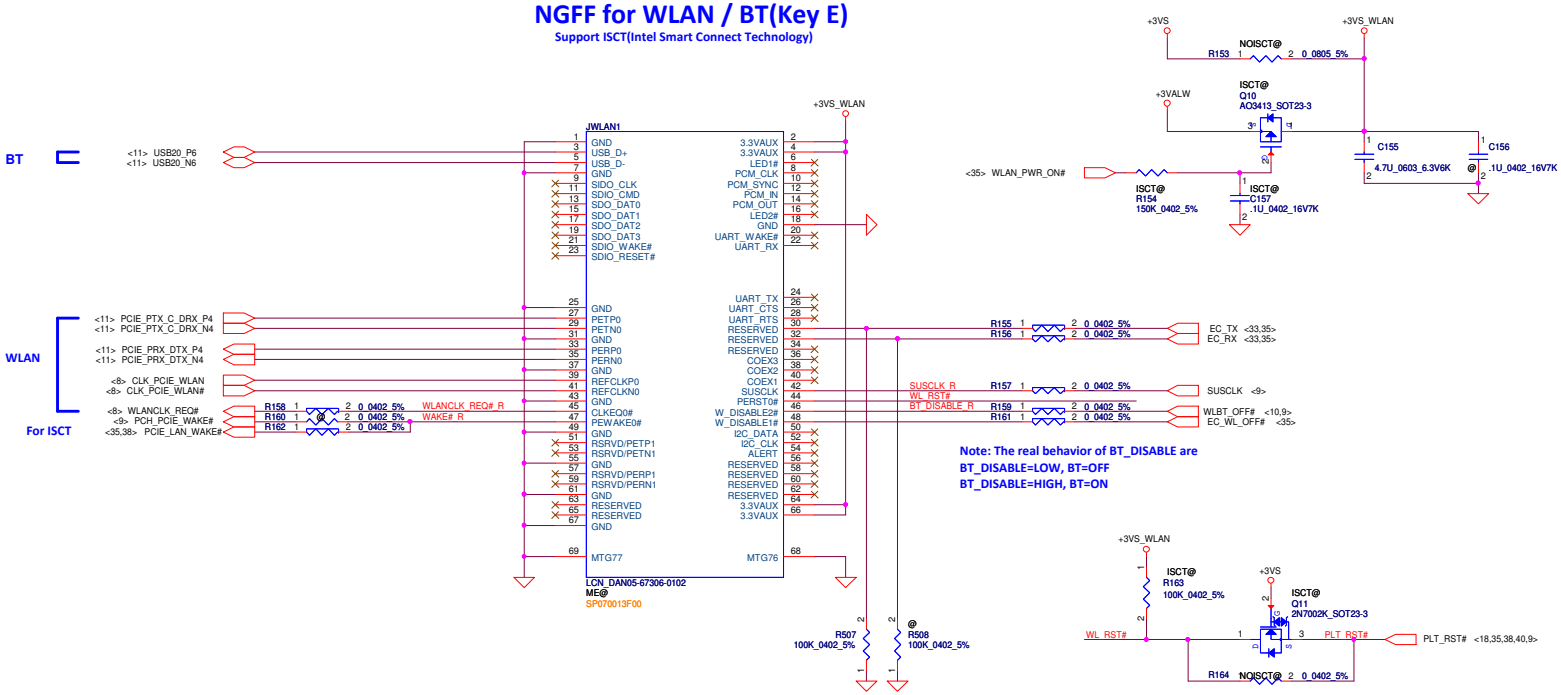
FOR 14" SATA ODD Conn.



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HDD/ODD/BT Connector		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 30 of 55		

NGFF for WLAN / BT(Key E)

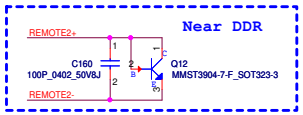
Support ISCT(Intel Smart Connect Technology)



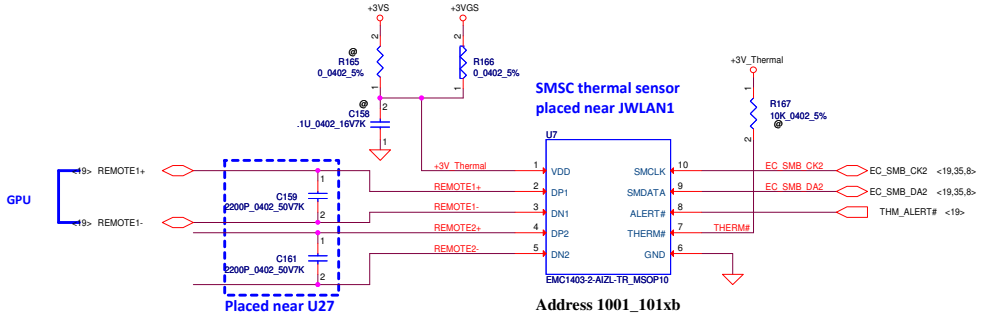
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	Mini-Card/NEW Card/SIM		
Size	Document Number	LA-B091P	Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 31 of 55		

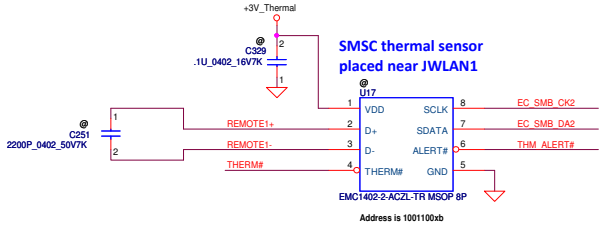
3 Channel

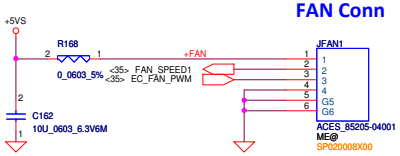


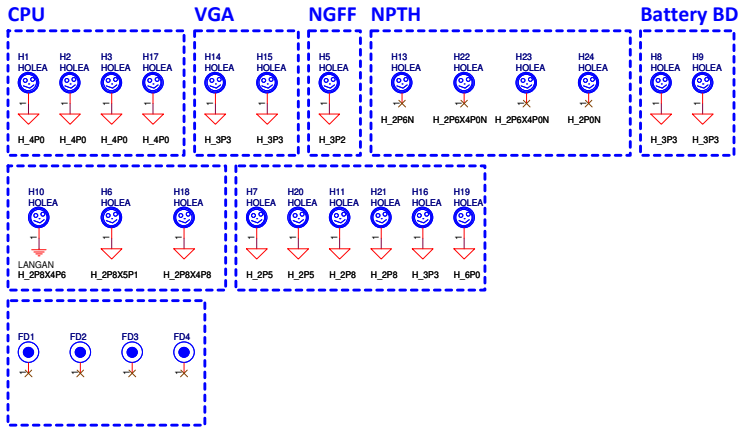
REMOTE1,2+/-:
Trace width/space:10/10 mil
Trace length:<8"



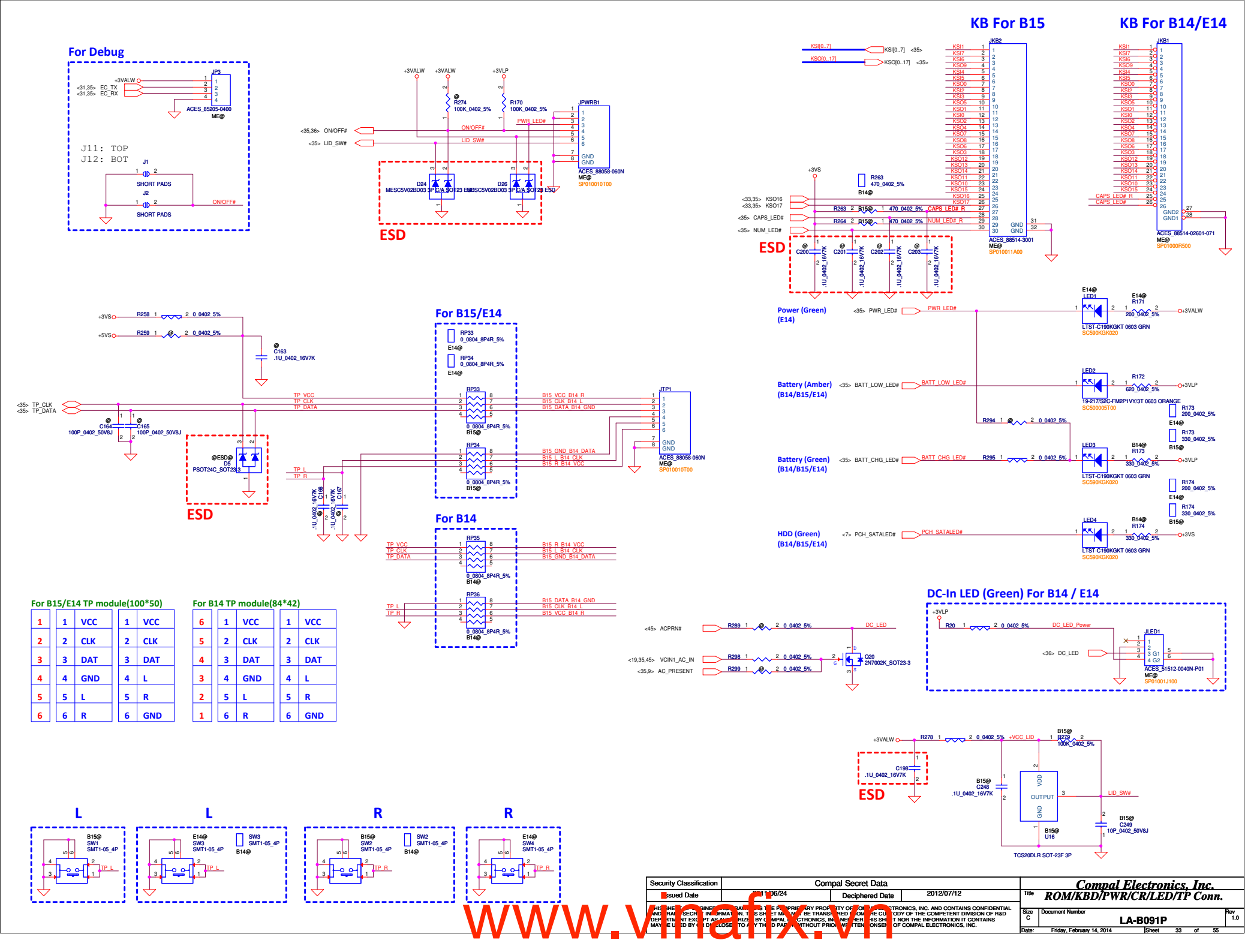
2 Channel



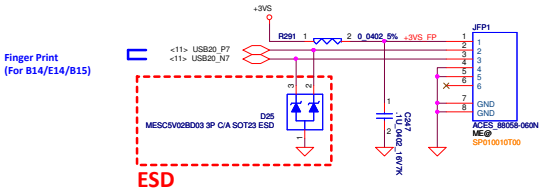




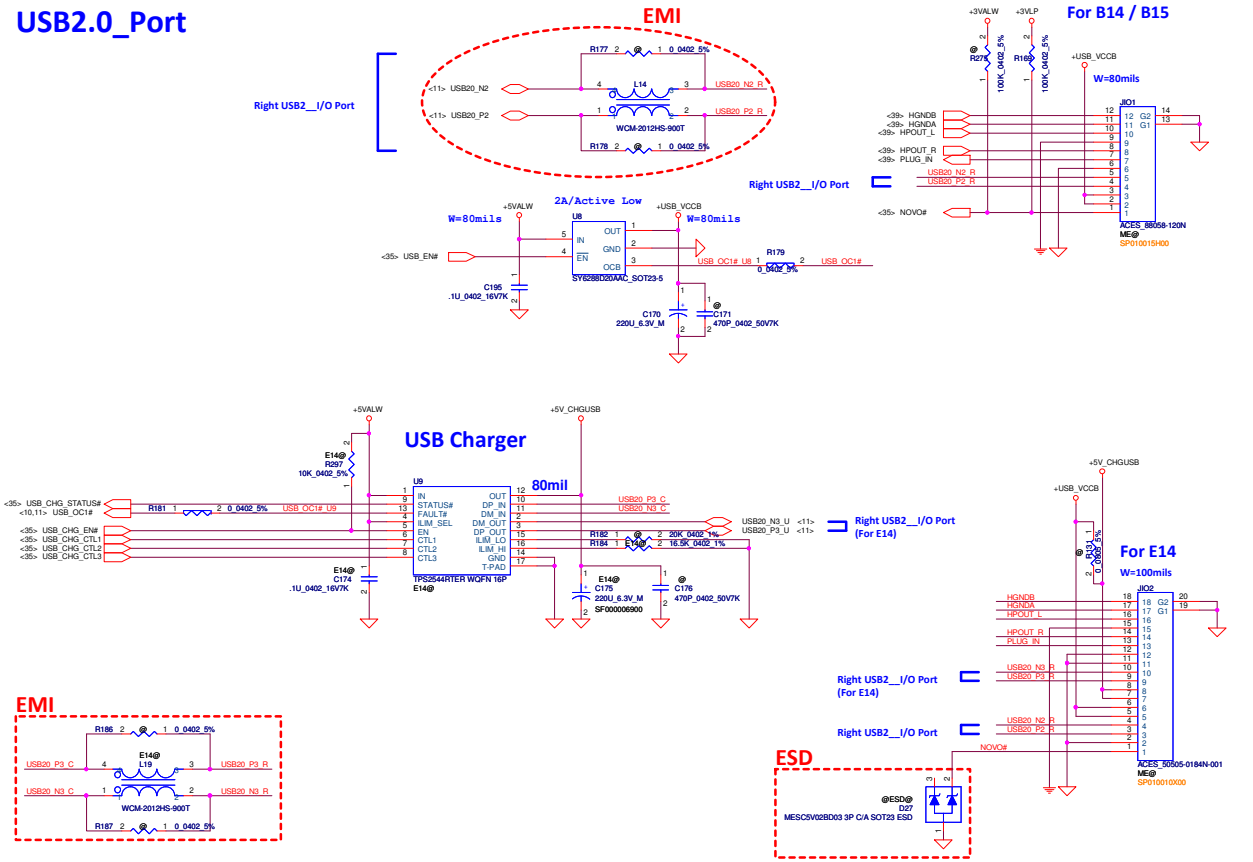
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	Fintek-Thermal IC/FAN/screw		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 32 of 55		



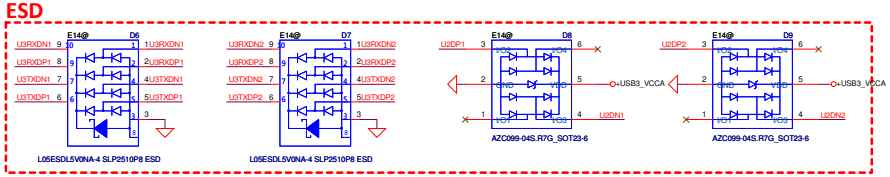
Finger Print



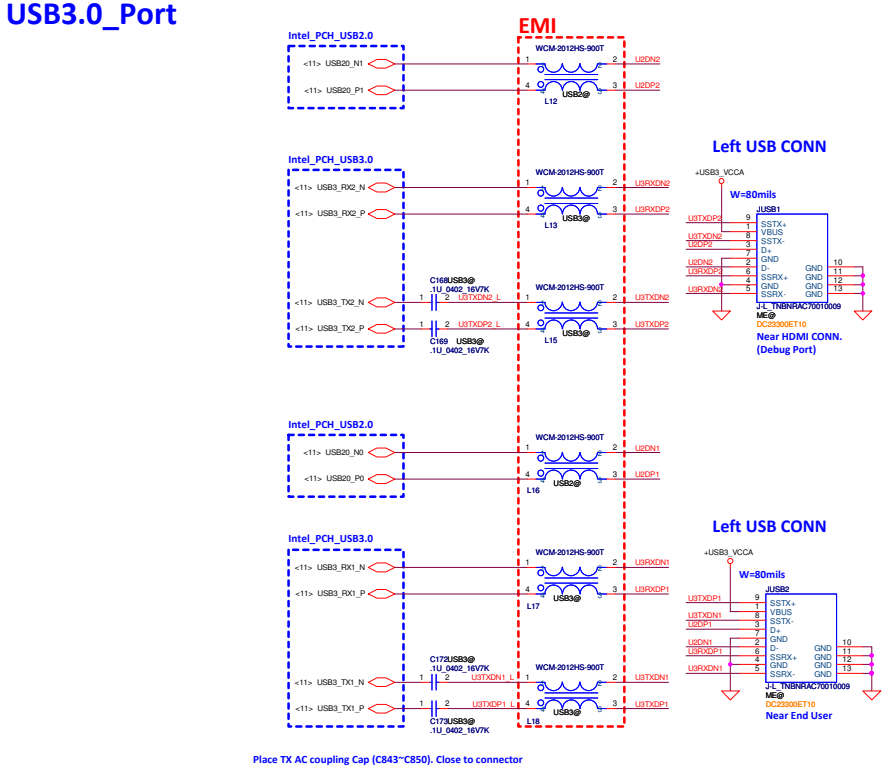
USB2.0_Port



ESD

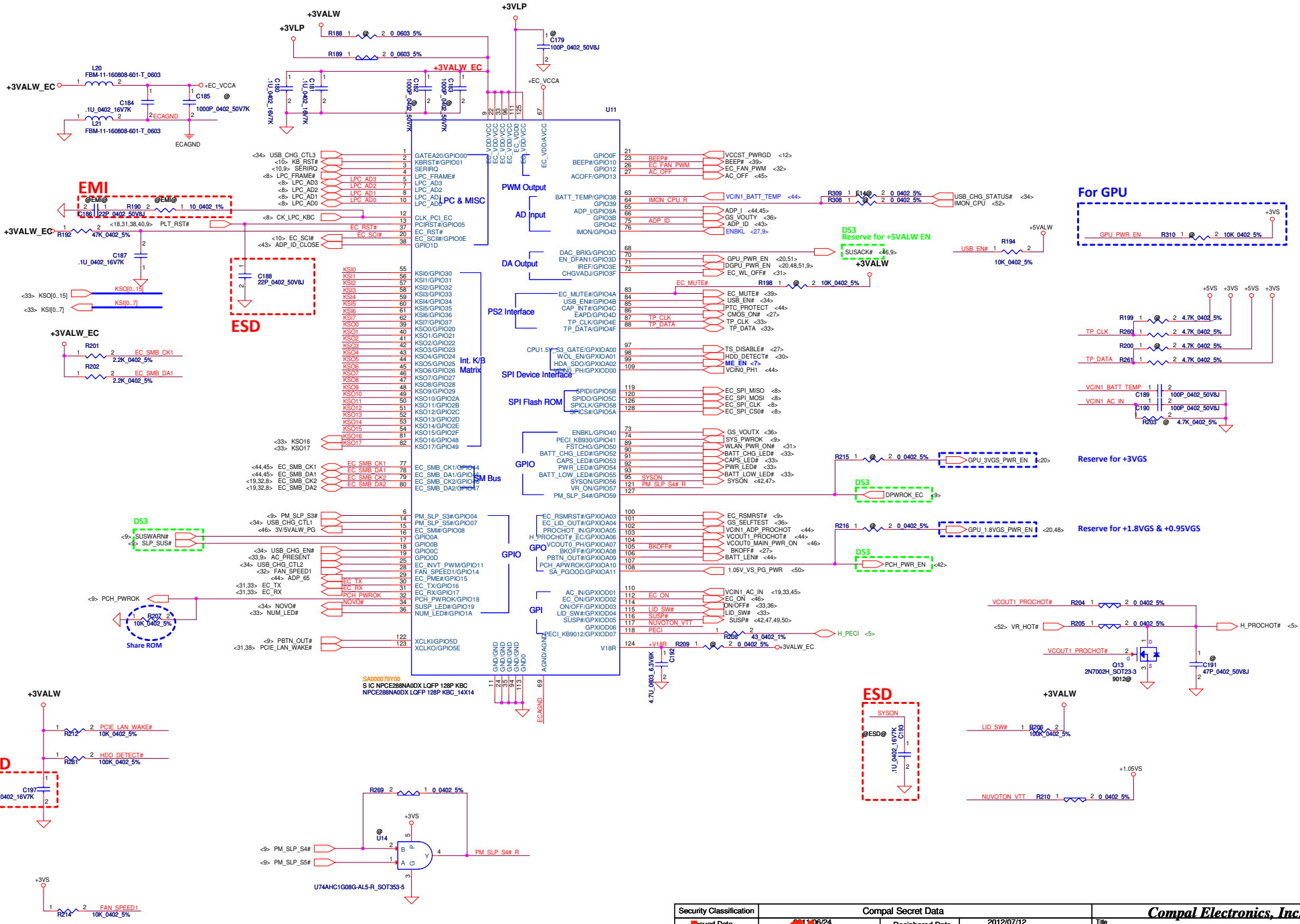


USB3.0_Port



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12	Title: USB3.0/Left USB Ports

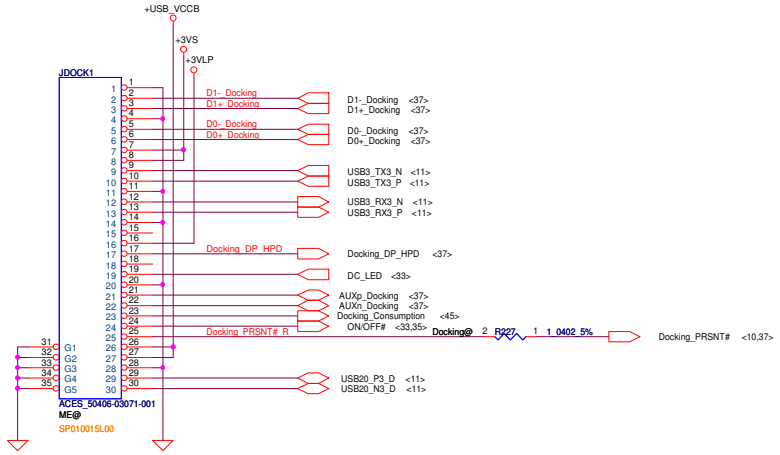
Size: B	Document Number		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 34 of 55		



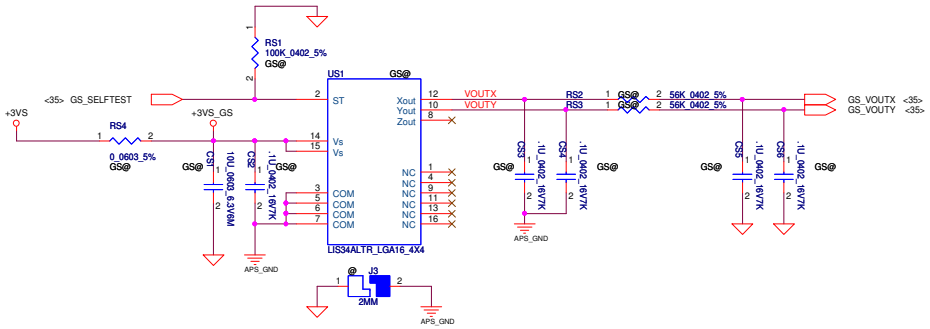
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: BIOS & EC I/O Port			
Size: C	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 35 of 55		

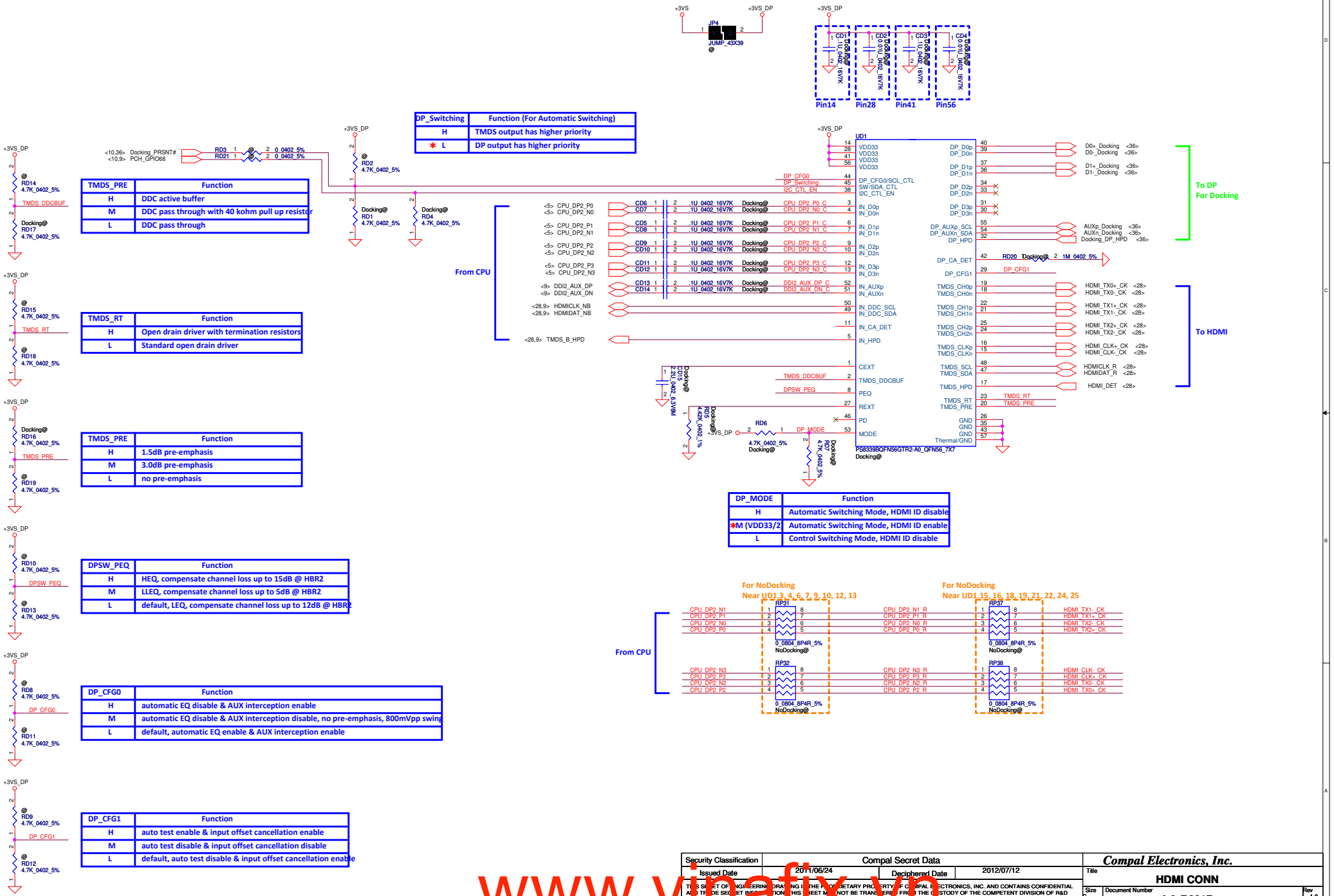
To Docking BD

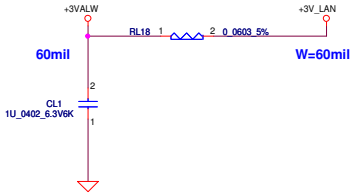


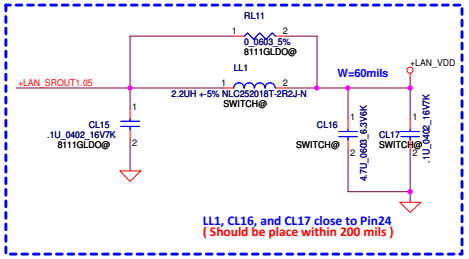
APS (G-Sensor)



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title: Docking			
Size: C	Document Number: LA-B091P		Rev: 1.0
Date: Wednesday, February 12, 2014		Sheet 36 of 55	

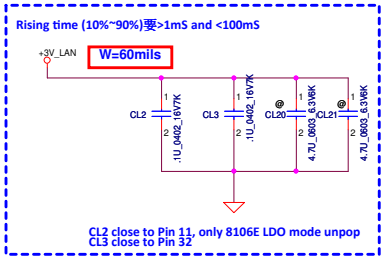


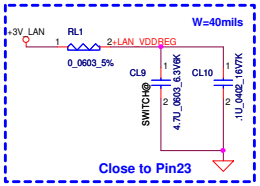


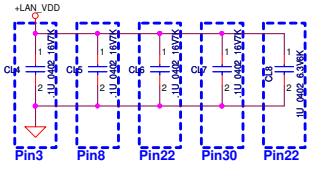


		1.0 V source	LL1	CL16, CL17	CL9, CL10	RL11	CL15
SA00005V700	RTL8111G	LDO	X	X	X	O	O
	~~RTL8111G~~	~~External~~	~~X~~	~~X~~	~~X~~	~~X~~	~~O~~
	RTL8111GS/ RTL8111GUS/ RTL8106EUS	SWR	O	O	O	X	X
SA00006Y00	RTL8106E	LDO	X	X	X	X	X

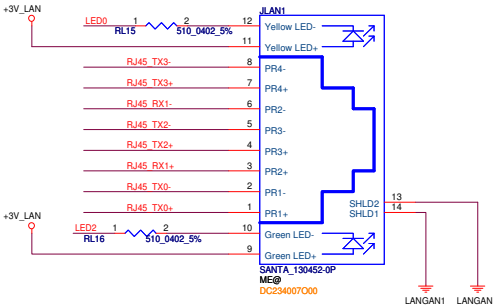
Please refer to the table above when using different 1.0V supply source.
For RTL8111GS, RTL8111GUS, RTL8106E and RTL8106EUS, External 1.0V Supply Is Not Permitted.



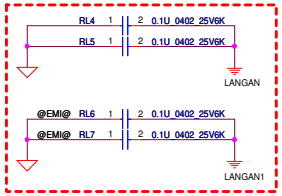


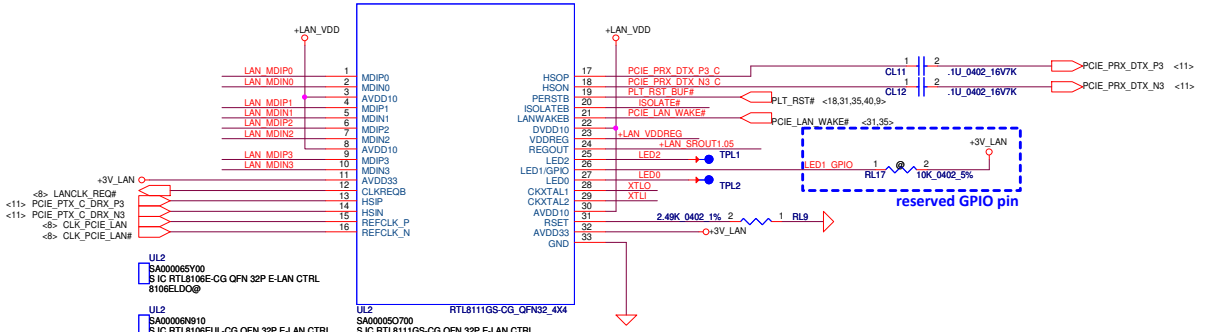


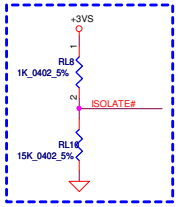
RJ-45 CONN.

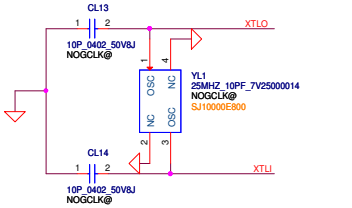


EMI

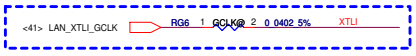




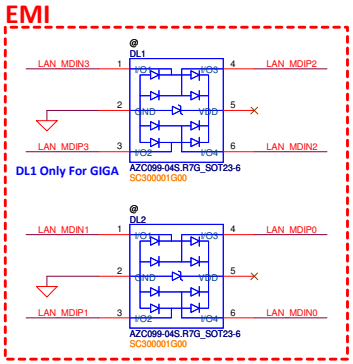




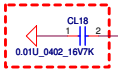
GCLK

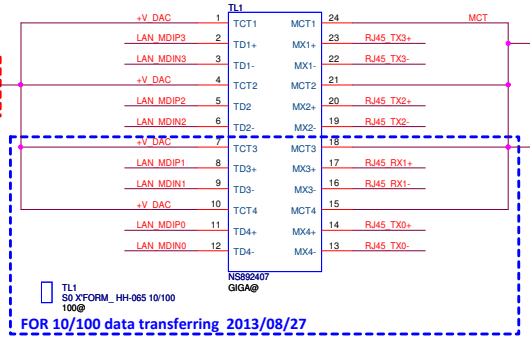


EMI

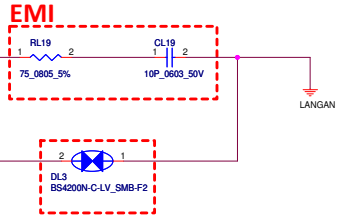


EMI



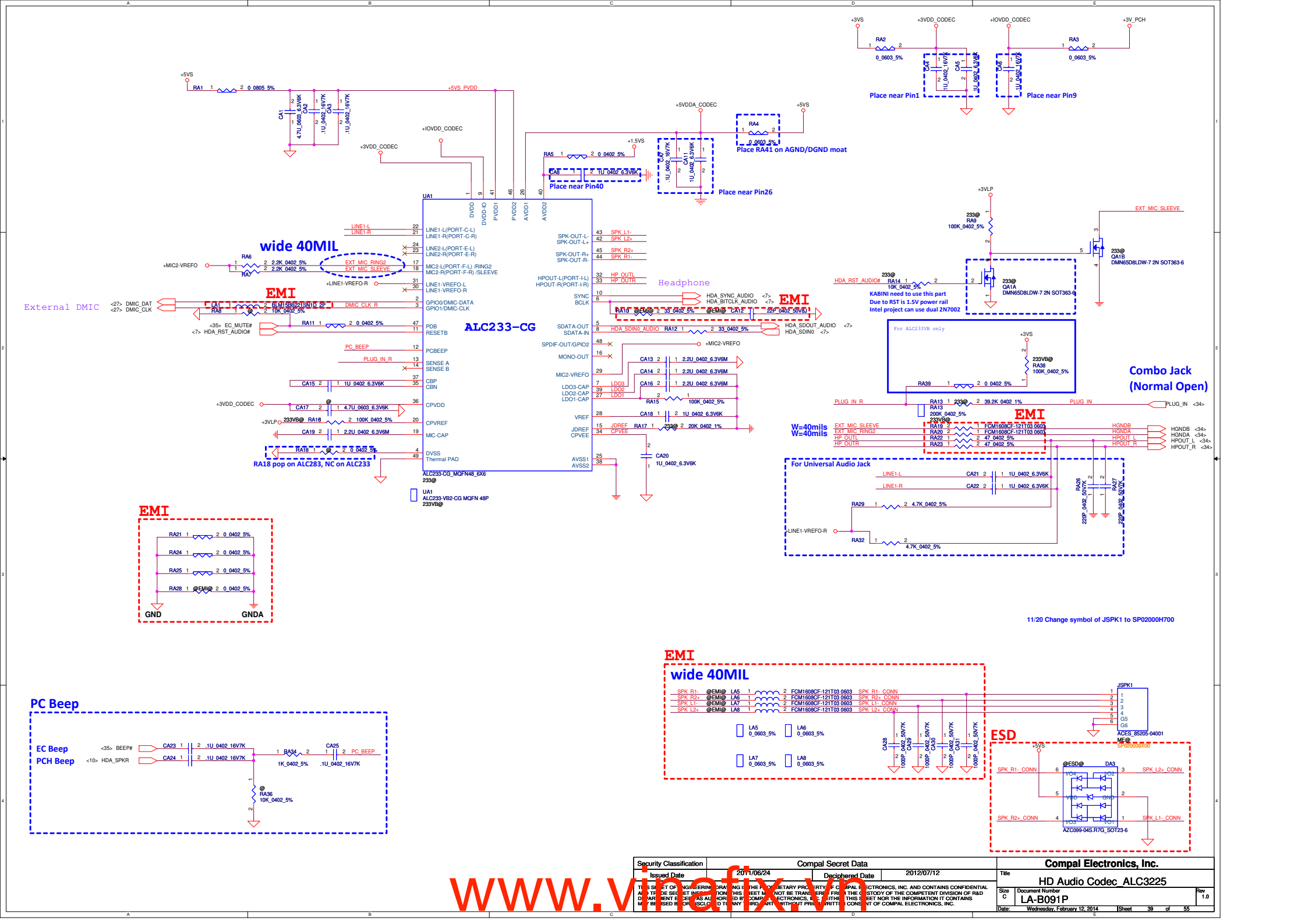


EMI

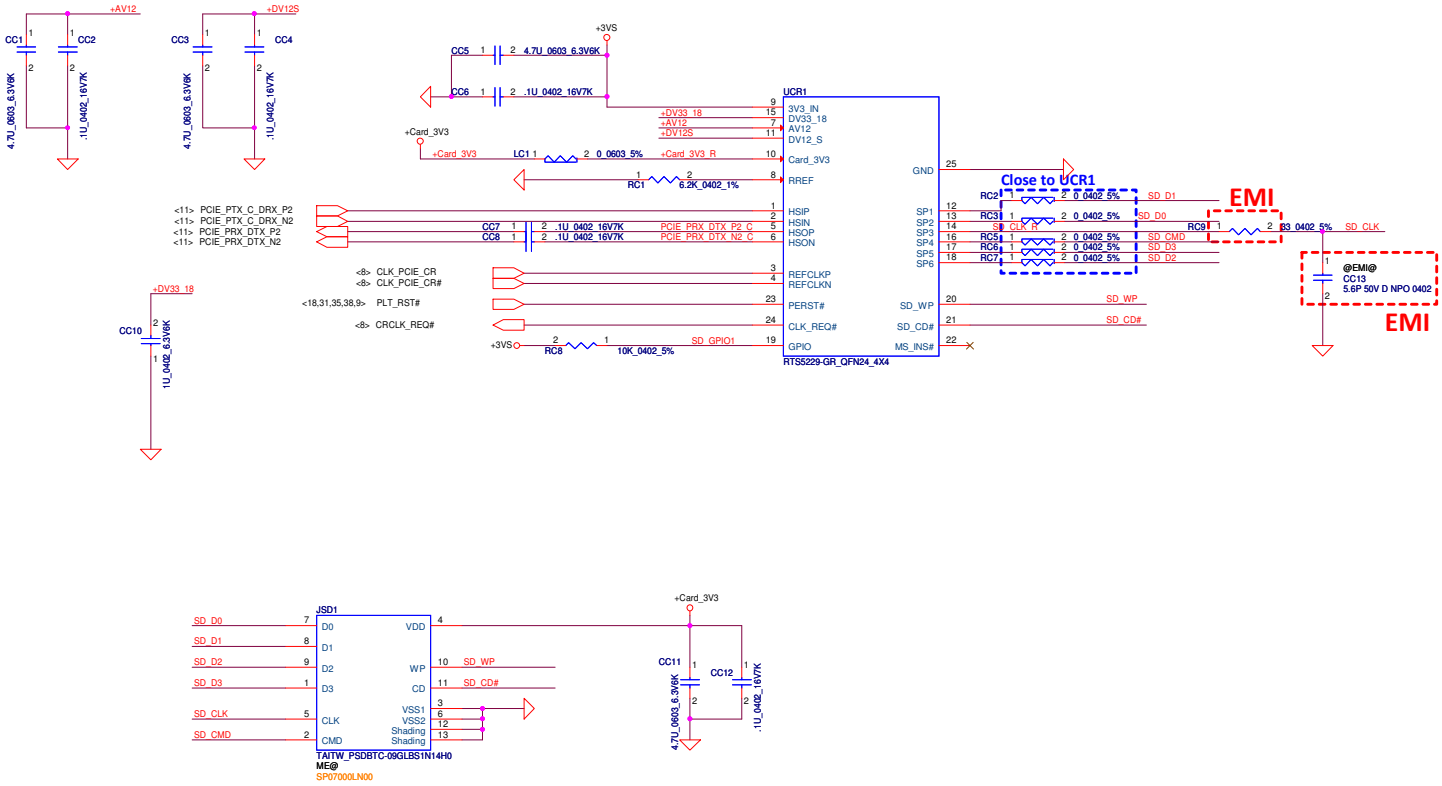


EMI

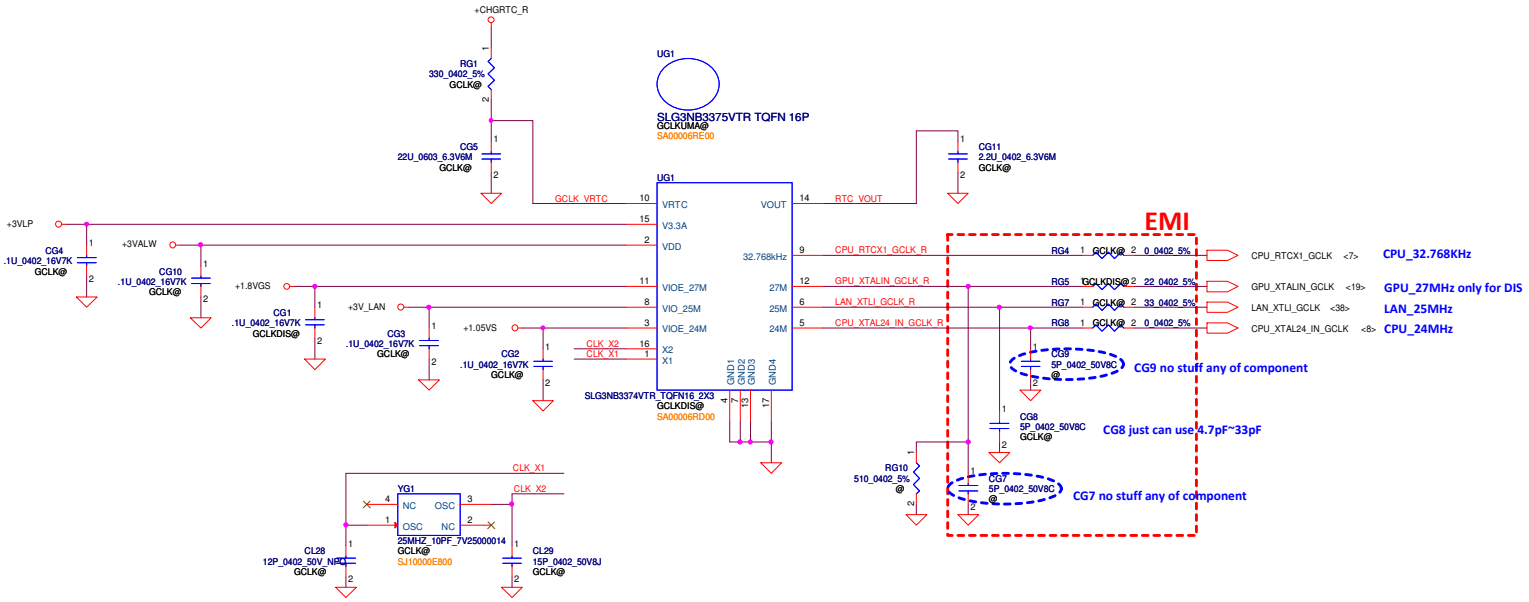
Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: LAN RTL8411-CG
			Size: C; Document Number: LA-B091P; Rev: 1.0
			Date: Wednesday, February 12, 2014; Sheet 38 of 55



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	HD Audio Codec_ALC3225		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 39 of 55		



Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	P24-CardRead/RTS5229		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 40 of 55		



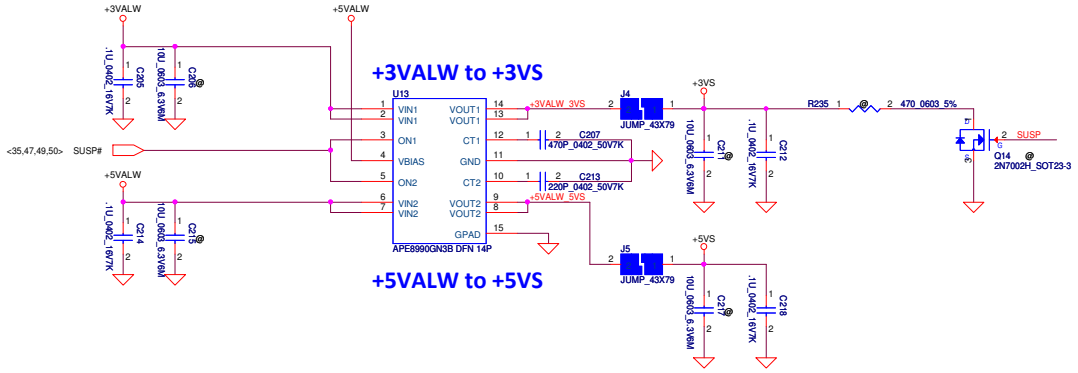
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

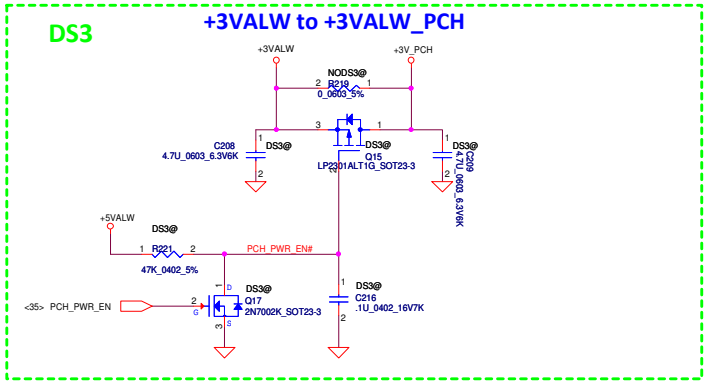
Compal Electronics, Inc.

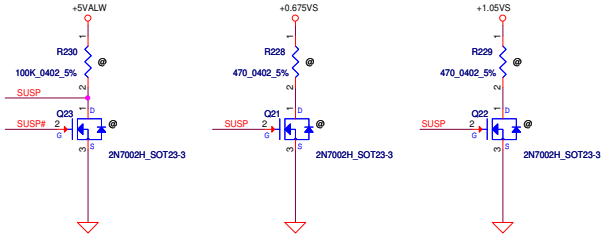
Title: GCLK

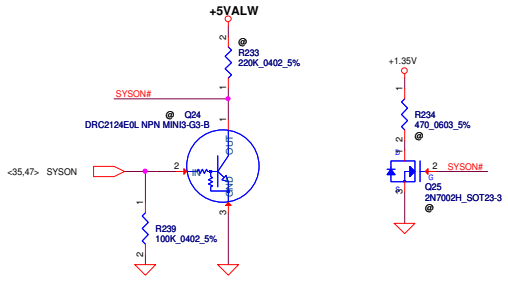
Size: | Document Number: LA-B091P | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 41 of 55

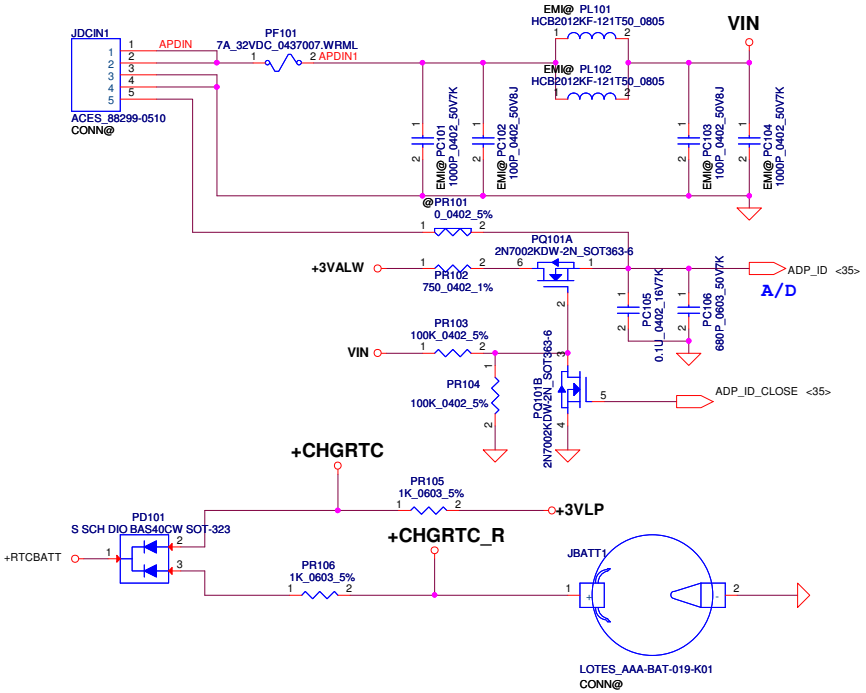








Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	DC Interface		
Size C	Document Number LA-B091P		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 42 of 55		



RTC Battery

ADP_ID

AC Adapter	90W	65W
R(K ohm)	open	10
ADP_ID(V)	3.3	1.65
Detection voltage	>2.64	1.32~1.98

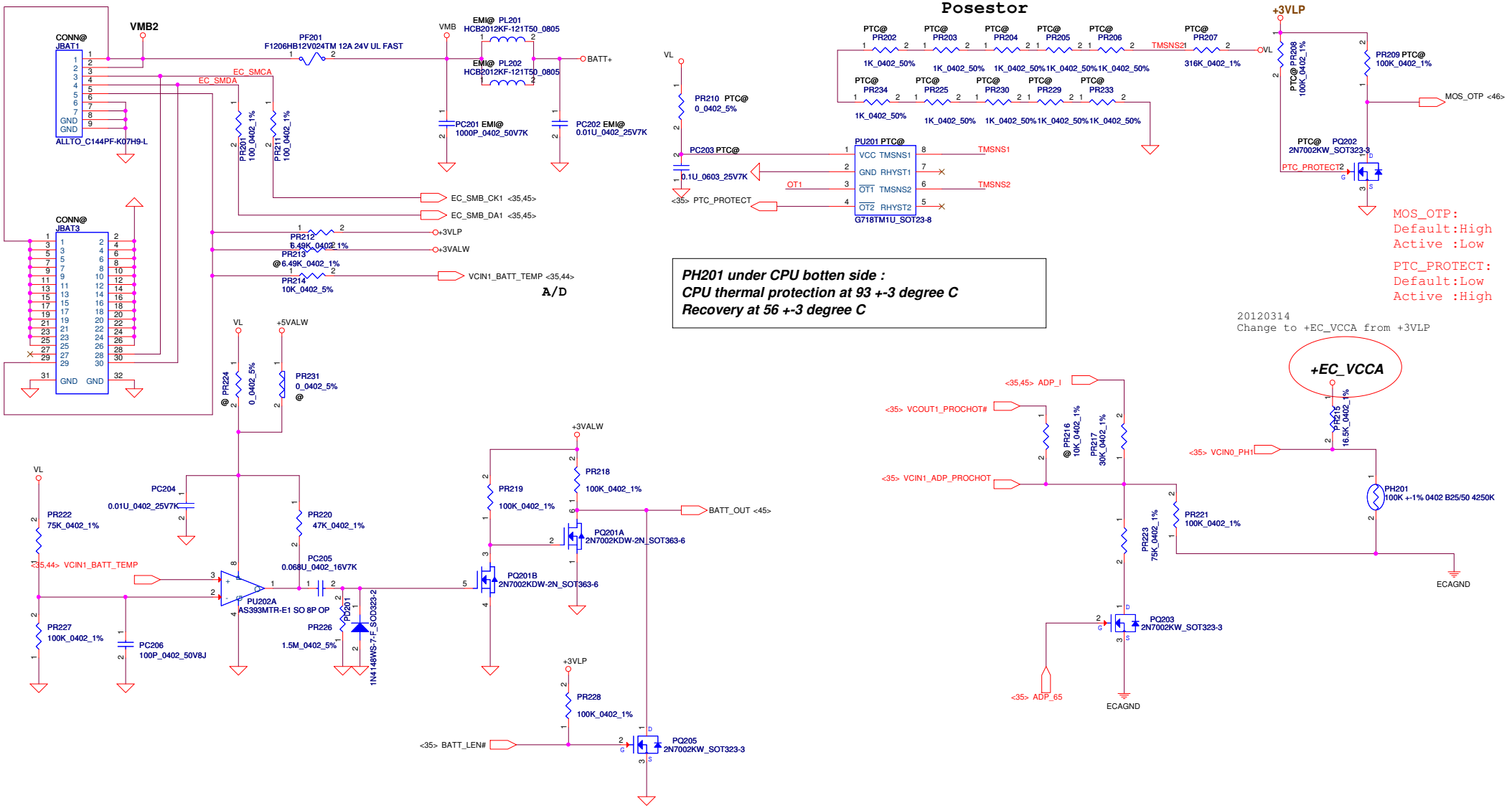
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR DCIN / RTC Battery

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 43 of 55



135W: 150W(Turbo_V=1.2) active 135W(Turbo_V=1.072) recovery
90W : 100W(Turbo_V=1.2) active 90W(Turbo_V=0.903) recovery
65W : 70W(Turbo_V=1.2) active 65W(Turbo_V=0.818) recovery
45W : 65W(Turbo_V=1.2) active 45W(Turbo_V=0.803) recovery

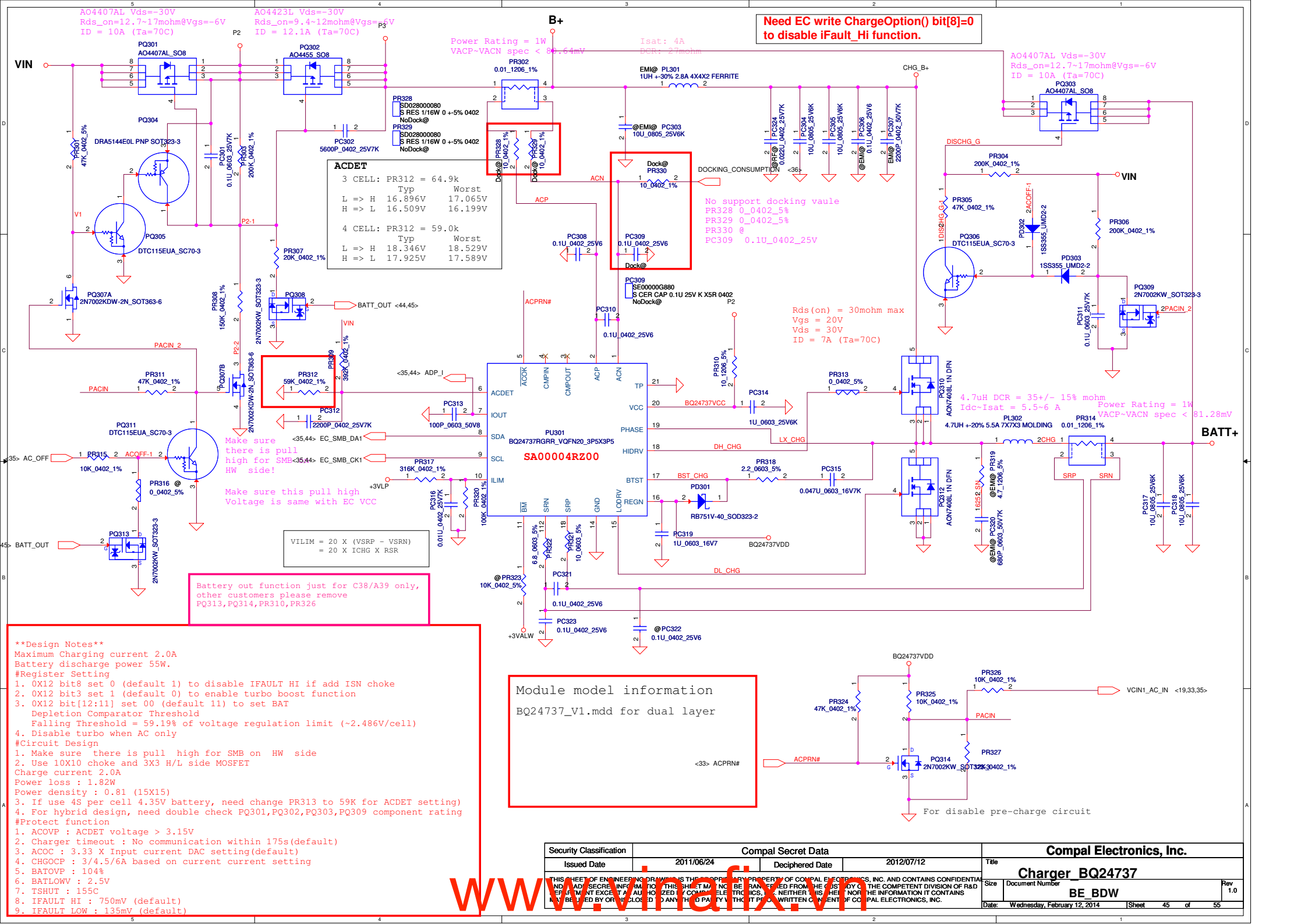
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR-BATTERY CONN/OTP

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 44 of 55

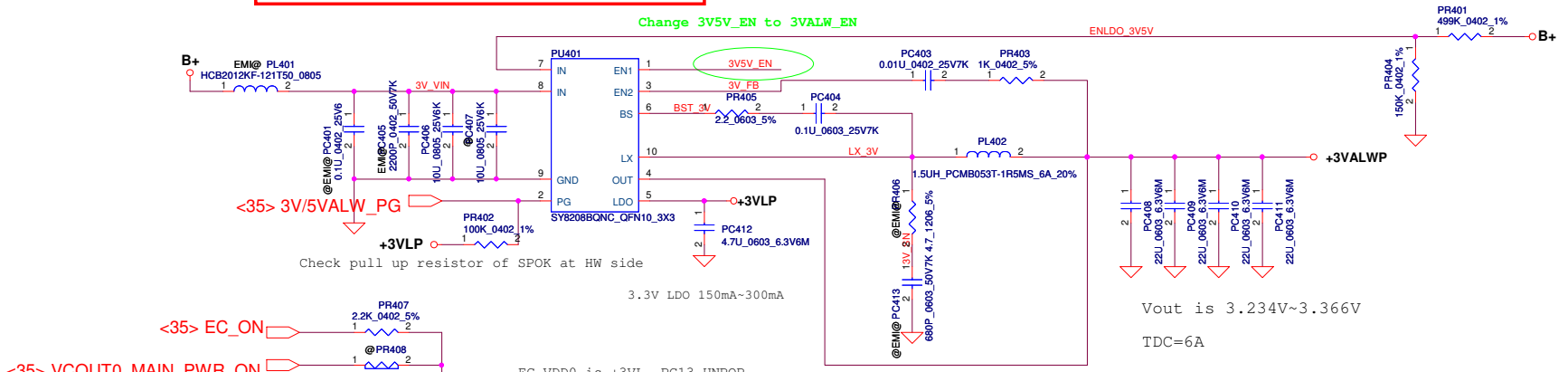


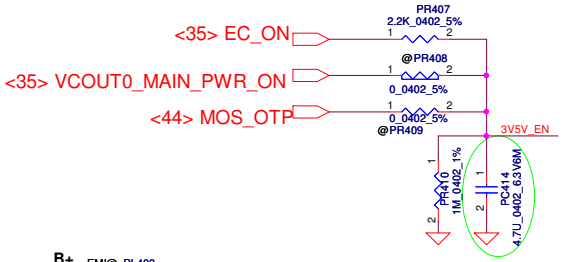
Module model information

SY8208B_V2.mdd

EN1 and EN2 dont't floating

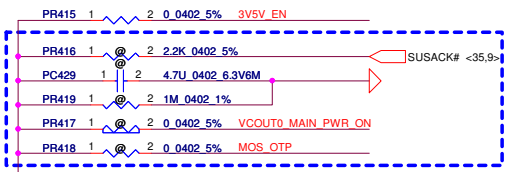
Change 3V5V_EN to 3VALW_EN



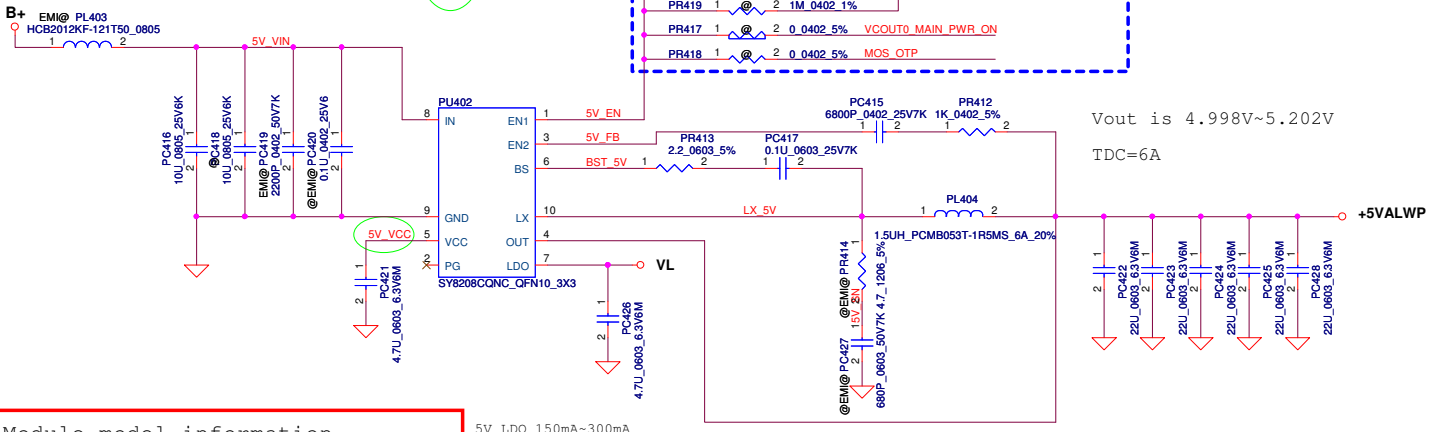


EC VDD0 is +3VL, PC13 UNPOP
EC VDD0 is +3VALW, PC13 POP

EN1 and EN2 dont't floating



Reserve for USB Charger



Vout is 4.998V~5.202V

TDC=6A

5V LDO 150mA~300mA

Module model information

SY8208C_V2.mdd

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: +3VALW/+5VALW

Size: Custom | Document Number: BE_BDW | Rev: 1.0

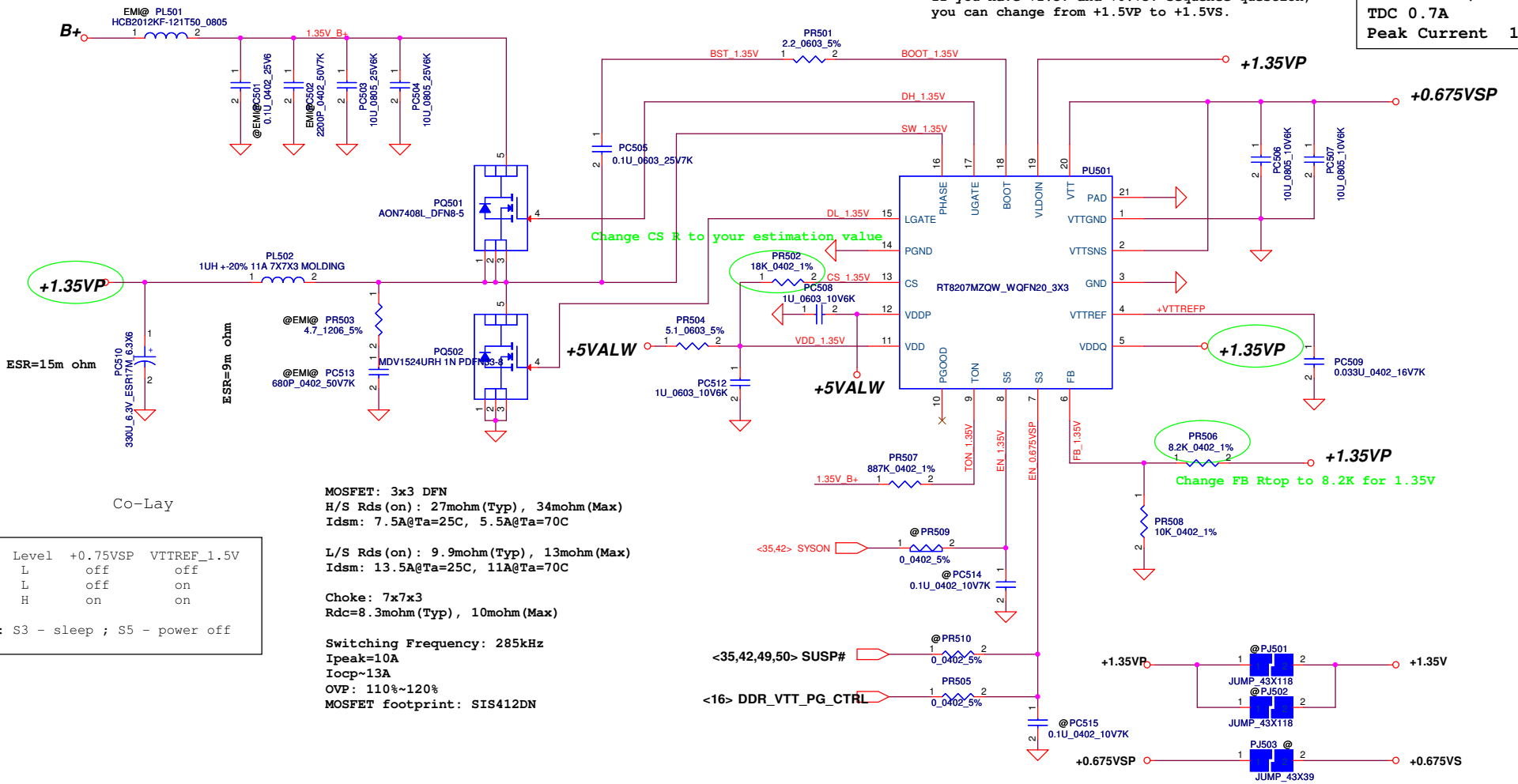
Date: Wednesday, February 12, 2014 | Sheet 46 of 55

Module model information

RT8207M_V1.mdd For Single layer
RT8207M_V2.mdd For Dual layer

Pin19 need pull separate from +1.5VP.
If you have +1.5V and +0.75V sequence question,
you can change from +1.5VP to +1.5VS.

0.75Volt +/- 5%
TDC 0.7A
Peak Current 1A



Co-Lay

MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 34mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 9.9mohm(Typ), 13mohm(Max)
Idsm: 13.5A@Ta=25C, 11A@Ta=70C

Choke: 7x7x3
Rdc=8.3mohm(Typ), 10mohm(Max)

Switching Frequency: 285kHz
Ipeak=10A
Iocp~13A
OVP: 110%~120%
MOSFET footprint: SIS412DN

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	on
S0	H	on	on

Note: S3 - sleep ; S5 - power off

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

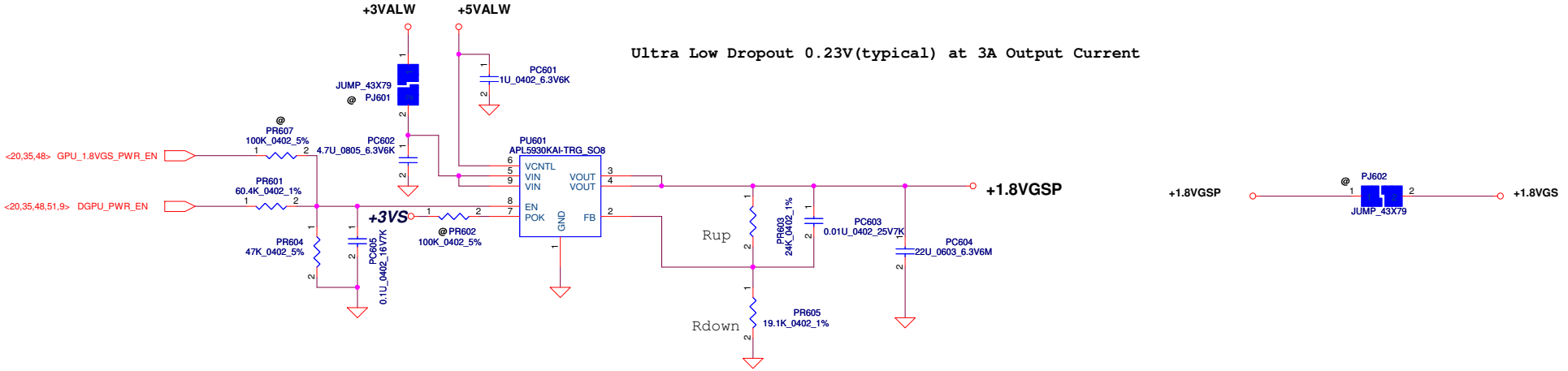
Title: RT8207M

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 47 of 55

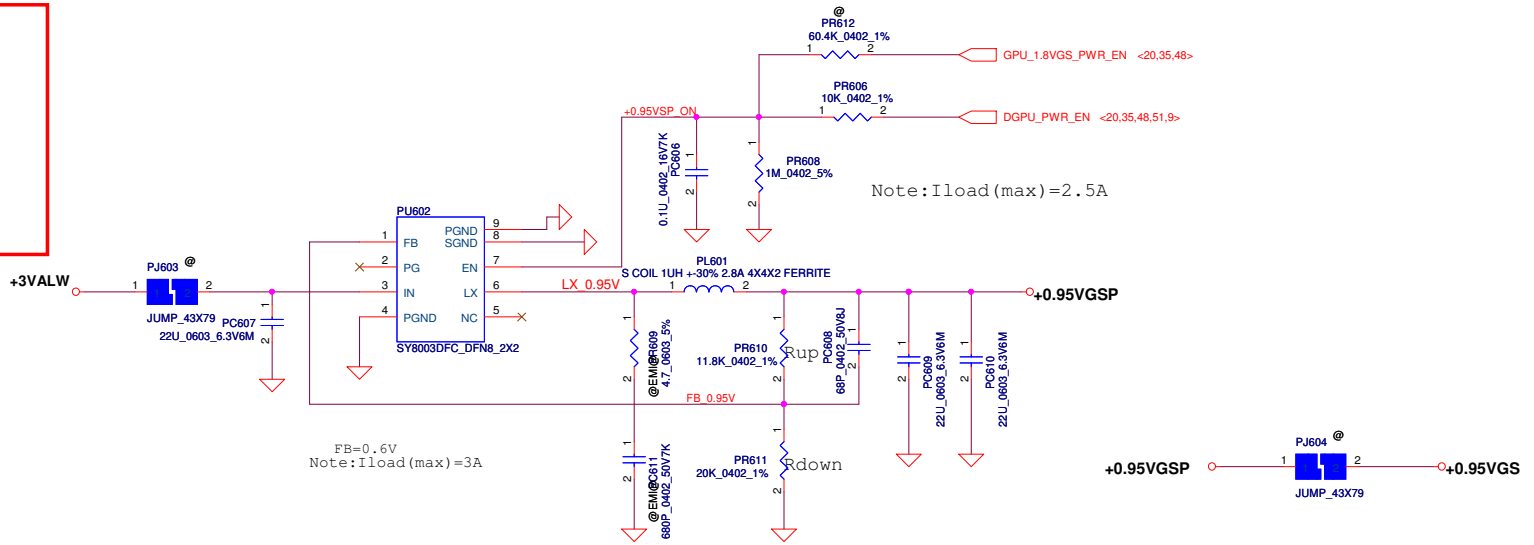
Module model information

APL5930_V1.mdd



Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

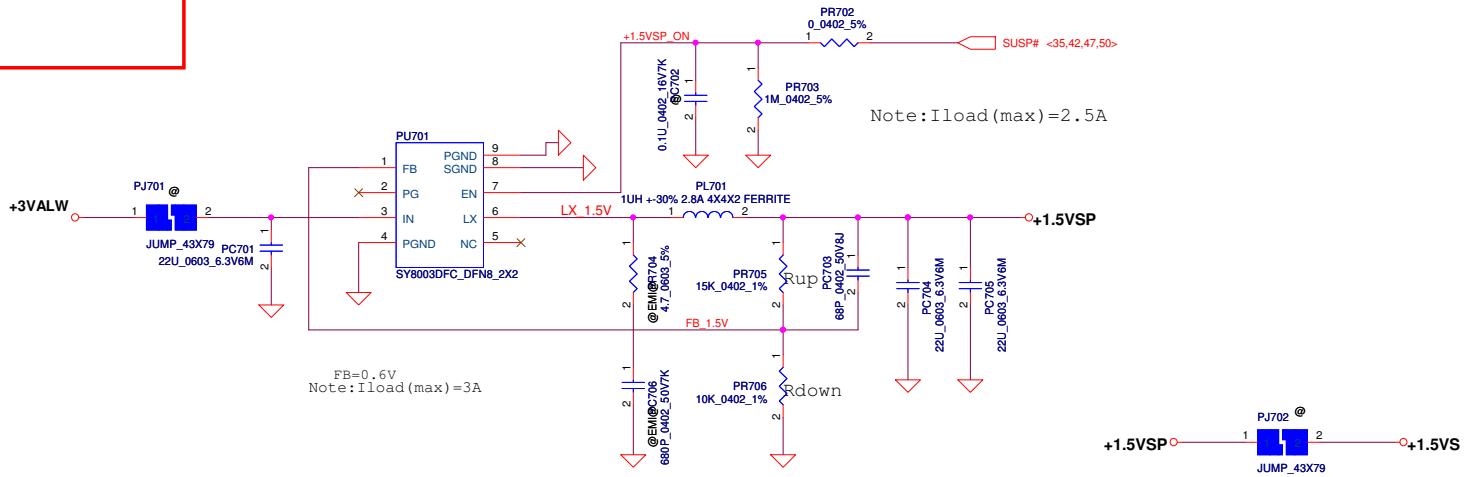
Title: +1.8VGS-+0.95VVGS

Size: Custom | Document Number: BE_BDW | Rev: 1.0

Date: Wednesday, February 12, 2014 | Sheet 48 of 55

Module model information

SY8003_V1.mdd



Note:
When design Vin=5V, please stuff snubber to prevent Vin damage

Vout=0.6V* (1+Rup/Rdown)

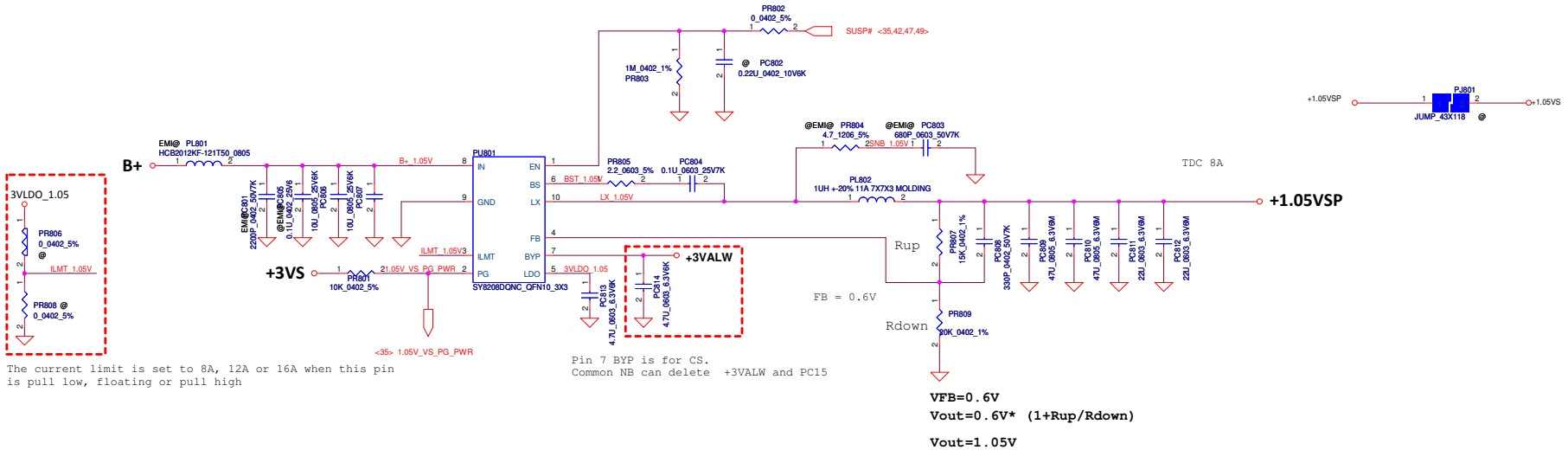
Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title: +1.5VS			
Size: Custom	Document Number: BE_BDW		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 49 of 55		

Module model information

SY8208D_V1.mdd

EN pin don't floating
If have pull down resistor at HW side, pls delete PR2



The current limit is set to 8A, 12A or 16A when this pin is pull low, floating or pull high

Pin 7 BYP is for CS.
Common NB can delete +3VALW and PC15

VFB=0.6V
Vout=0.6V* (1+Rup/Rdown)

Vout=1.05V

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date	2012/07/12
Title	+1.05VS		
Size C	Document Number BE_BDW		Rev 1.0
Date: Wednesday, February 12, 2014	Sheet 50 of 55		

Module model information

ISL62771_V1A.mdd for IC portion

ISL62771_V1B.mdd for SW portion

+VGA_CORE

AMD TOPAZ
TDC 31A, EDC 46.5A
OCP min 58.1A

AMD JET LE
TDC 20A, EDC 30A
OCP min 37.5A

Fsw=400K Hz

SH00000NX00 (DCR:1.4± 5%)

Reserve for GPU Sequence

25W

15W

PR1046 set 536 ohm to OCP 26.32A

GPU 15W setting

PR931=536 ohm, PR924=1K ohm, PC925=0.1uF,
PR944 =0 ohm, PR920=10K ohm, PC924=0.022U
PC961 @, PC962 @, PR938 @ and PR939 @
while PR931=536 ohm to set OCP for GPU 15W application.

+VGA_CORE

Security Classification	Compal Secret Data		Compal Electronics, Inc.
Issued Date	2011/06/24	Deciphered Date 2012/07/12	Title: PWR-+VGA_CORE
			Size: Custom; Document Number: BE_BDW; Rev: 1.0
			Date: Wednesday, February 12, 2014; Sheet 51 of 55

Module model information:
ISL95813 (for 15W & 28W CPU)

Base on BDW PDDG Rev_0_73		
Location	15W TDC 14A MAX 32A OCP 39A Loadline=-2.0mv/A	Note
PR1120	499 Ohm	OCP
PR537	1.27kOhm	Droop
PC528	0.022uF	RC Match
PR507	90.9kOhm	PROG1
PR703	93.1kOhm	IMON
PC518	0.1uF (0402)	RC Filter

H-side MOS: MDV1525URH
Rds(on):
<10.1mohm@Vgs=10V
<14.0mohm@Vgs=4.5V
Id :24A@Vgs=10V

L-side MOS: MDU1511RH
Rds(on):
<2.4mohm@Vgs=10V
<3.3mohm@Vgs=4.5V
Id :100A@Vgs=10V

Choke: 0.12UH (Size:7*7*3)
Rdc=0.62mohm +-5%
Heat Rating Current=41.5A
Saturation Current=41A

+1.05VS
Follow intel guideline
PR1102 130_0402_1%
PR1103 54.9_0402_1%
PC1102 1U_0402_6.3V6K

Note:
VR_SVID_ALRT# Pull high on HW side

<12> VR_SVID_DAT
<12> VR_SVID_ALRT#
<12> VR_SVID_CLK
<12> VR_ON
<12> VGATE
<35> IMON_CPU
<35> VR_HOT#

PR1104 169K_0402_1%
Note:
PR1104=169K
=>Icc(max)=33A
fsw=700KHz

PU1101
ISL95813HRZ-T_QFN20_3X4
PAD, SCLK, ALERT#, SDA, PRGM1
VR_ON, PGOOD, IMON, VR_HOT#, NTC, COMP
LGATE, PHASE, UGATE, BOOT, VCC, PRGM2
FB, RTN, ISUMN, ISUMP

@PR1101 1.91K_0402_1%
PR1122 1.5K_0402_1%
PC1101 1000P_0402_50V7K
PR1106 97.6K_0402_1%
PH1101 470K +-5% 0402 B25/50 4700K
PR1110 3.83K_0402_1%
PR1111 27.4K_0402_1%
PC1109 47P_0402_50V8J

PR1105 0_0603_5%
PR1108 2.2_0603_5%
PC1108 0.22U_0603_16V7K
PC1111 0.1U_0402_25V6
PR1112 124K_0402_1%

Note:
PR1112=124K
=>Slew rate=53mV/us
Vboot = 1.7V

PQ1101 MDV1525URH_PDRN33-8-5
PQ1103 MDU1511RH_POWERDFN56-8-5
PQ1102 MDU1511RH_POWERDFN56-8-5

CPU_B+
PC1103 10U_0805_25V6K
PC1104 10U_0805_25V6K
EMI@PC1105 0.01U_0402_50V7K
EMI@PC1106 220P_0402_50V7K
PC1107 0.022U_0402_25V7K
@RF@ 0.022U_0402_25V7K
PC1123 33U_25V_M
PC1122 68U_25V_M
EMI@ PL1103 HCB2012KF-121T50_0805
@EMI@ PL1104 HCB2012KF-121T50_0805
B+

PL1102 .15UH 20% PCME064T-R15MS0R667 36A
+CPU_CORE
PR1109 3.65K_0603_1%
@EMI@PR1107 4.7_1206_5%
@EMI@PC1110 680P_0603_50V7K

+5VS

Over temperature protection:
OTP Setting: 100C active
Pin5 (NTC) voltage <0.88V, Protect
Pin5 (NTC) voltage >0.92v, recovery

PR1113 909_0402_1%
33P_0402_50V8J @PC1112
PC1113 6800P_0402_25V7K

Droop
PR1116 1.27K_0402_1%
@PR1114 2K_0402_1%
@PR1115 10_0402_1%
@PC1114 330P_0402_50V7K
@PC1115 390P_0402_50V7K

RC Match
PR1117 4.99M_0402_1%
PC1116 0.033U_0402_25V7K
PC1117 0.1U_0402_16V4Z
PR1118 4.42K_0402_1%
PR1119 11K_0402_1%
PH1102 10K +-5% 0402 B25/50 4250K

<12> VCCSENSE
<12,14> VSSSENSE

@PC1118 330P_0402_50V7K
@PC1119 0.082U_0402_16V7K
PC1120 0.01U_0402_50V7K

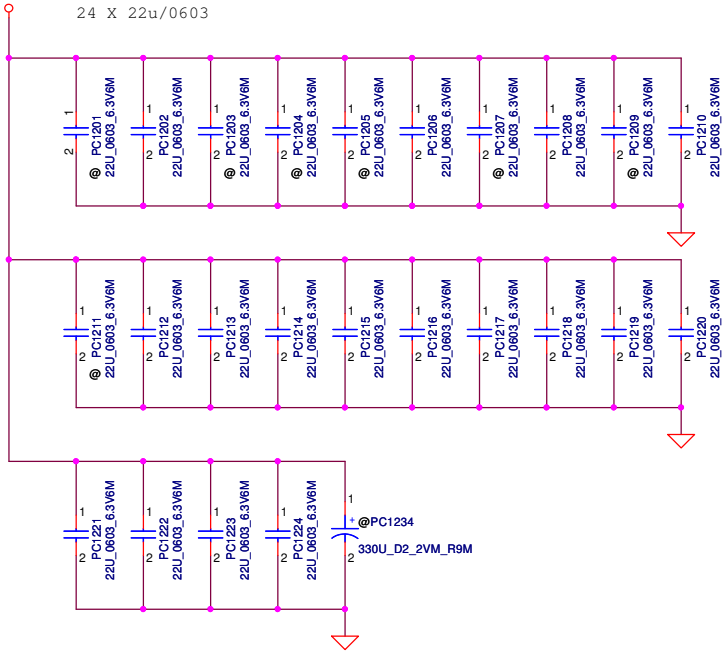
OCP Setting
PR1120 287_0402_1%

@PC1121 4700P_0402_25V7K
@PR1121 1.5K_0402_1%

Local sense put on HW site

Compal Electronics, Inc.
Title: ISL95813 for BDW-Y&U(15W/28W) CPU
Size: Document Number: BE_BDW Rev: 1.0
Date: Wednesday, February 12, 2014 Sheet 52 of 55

+CPU_CORE



Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.

Title: PWR-PROCESSOR DECOUPLING

Size	Document Number	Rev
Custom	BE_BDW	1.0

Date: Wednesday, February 12, 2014 Sheet 53 of 55

Version change list (P.I.R. List)

Item	Reason for change	PG#	Modify List	Date	Phase
1					
2					
3					
4					
6					
7					
8					
9					
10					
11					
12					
13					
14					
15					
16					
17					

Security Classification	Compal Secret Data		
Issued Date	2011/06/24	Deciphered Date	2012/07/12

Compal Electronics, Inc.			
Title	PIR (PWR)		
Size: Custom	Document Number: BE_BDW		Rev: 1.0
Date: Wednesday, February 12, 2014	Sheet 54 of 55		

ZIWB2/ZIWB3/ZIWE1 HW PIR List

Item	Page	MODIFICATION LIST	PURPOSE
			EVT TO DVT
1	P.36	Modify DP_SEL schematic	Because the first design is wrong.
2	P.34	Delete D28	It already reserve in sub BD
3	P.36	Modify HPD schematic	Because the first design is wrong.
4	P.36	Modify DP AUX schematic	Cap already reserve in sub BD
5	P.20	Reserve +1.05VS to +0.95VGS	AMD's suggestion
6	P.33	Add D26 for ESD	
7	P.42	Add RV198, RV199	AMD's suggestion
8	P.22~24	Add GPU Termination Resistance	AMD's suggestion
			DVT TO PVT
1	P.35	change U11.111 power rail to +3VLP	It only use +3VLP
2	P.33	un-pop R294, pop R295.	B series's LED need to follow E series
3	P.10	Add R247, R248	For BIOS Stap Pin
4	P.20	Add RV60, delete RV36	for GPU Sequence
5	P.20	Add RV61, delete RV240	for GPU Sequence
6	P.37	Change DP Switch IC solution	For HDMI audio issue
7	P.35	Add C197 for ESD	
8	P.33	Add C198 for ESD	
9	P.30	Add C199 for ESD	
			PVT TO PRE-MP
1	P.33	Reserve R298, R299 for DC-in LED control	To avoid LED shimmer
2	P.38	Change DL1 and DL2 footprint for ESD	