Intel Calpella BlOCK DIAGRAM

Intel Calpella Arrandale UMA

01

POWER

SYSTEM RESET CIRCUIT

BATT CHARGER

AC/BATT CONNECTOR

RUN POWER SW

+3V_S5/+5V_S5

+3V_SUS/+5V_SUS

+5V_RUN/+3V_RUN/+1.8V_RUN

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT

+1.05V_PCH

+1.05V_VTT

CPU VR

DC/DC
+3VPCU/+5VPCU/

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

DDR3-SODIMM1 CHA

DDR3-SODIMM2 CHB

Dual Channel DDR3
1066 1.5V

FDI

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD

SATA

SATA-HDD

SATA

MDC

IHDA

AUDIO/AMP
ALC269

Audio SPK conn

Audio Jacks

LVDS

VGA

USB2.0 x 3

USB2.0

PCIEx1

PCIEx2

Panel Connector

CRT CONN.

USB conn x 3

Card Reader SD MS CARD
RTS5159

LAN
Realtek 10/100/ LAN RTL8103EL

MINI-CARD
WLAN

LPC

SPI

FLASH 2Mbyts

EC
ITE8502

18X8

Keyboard

SPI

PS/2

FLASH 2Mbyts

Touchpad

Quanta Computer Inc.
PROJECT : FH1

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	BLOCK DIAGRAM	1A

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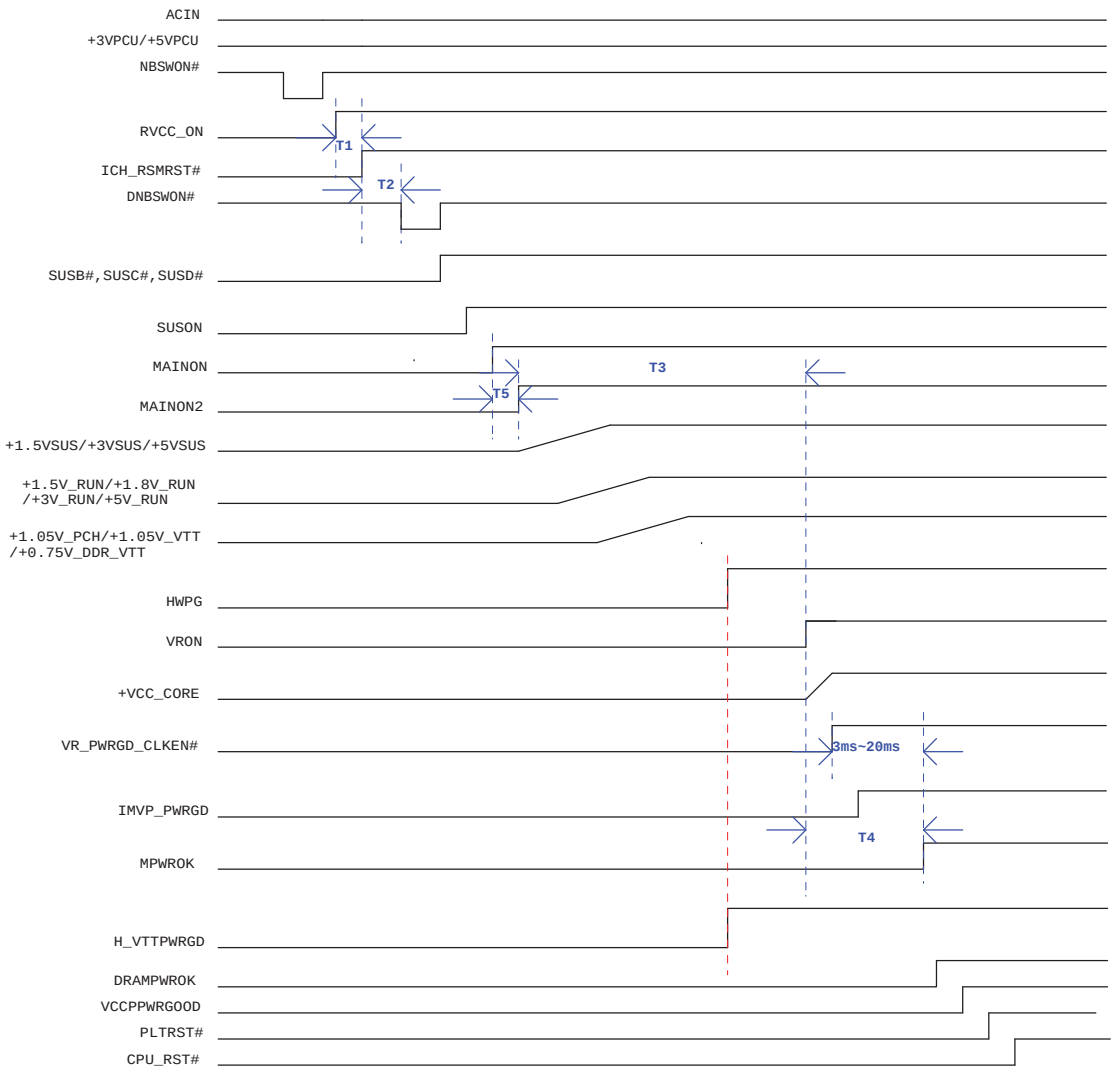
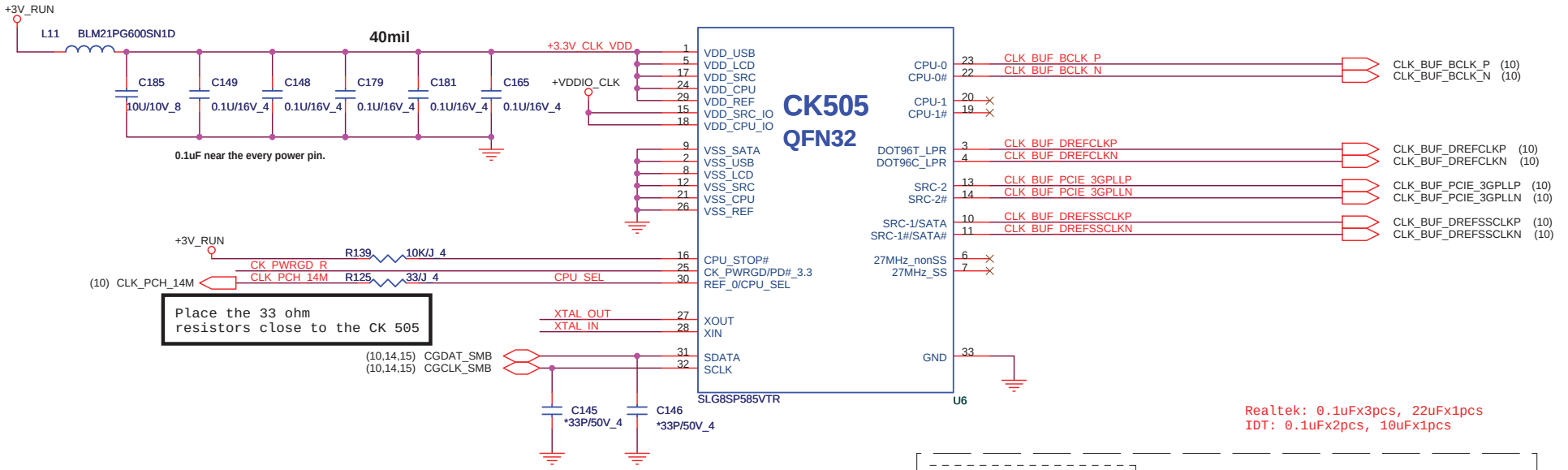
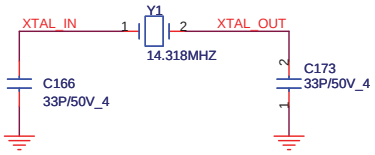
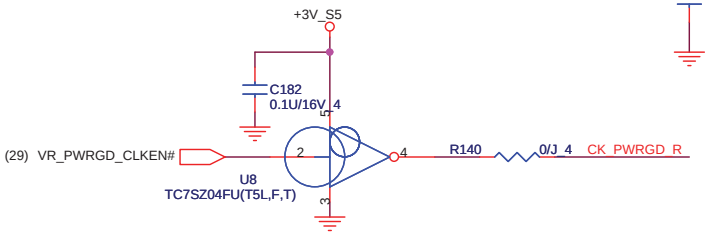
Power Sequence

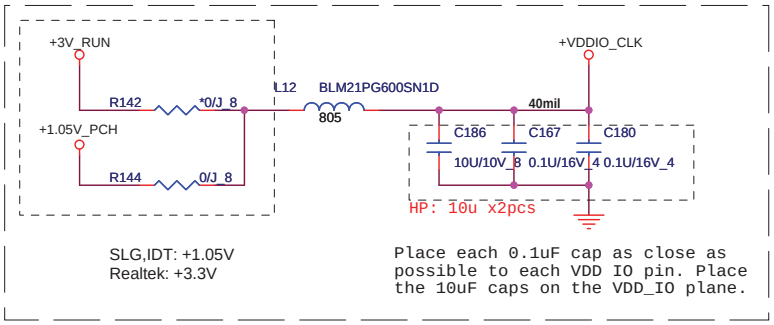


T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us

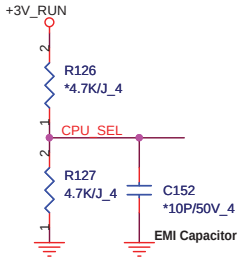








+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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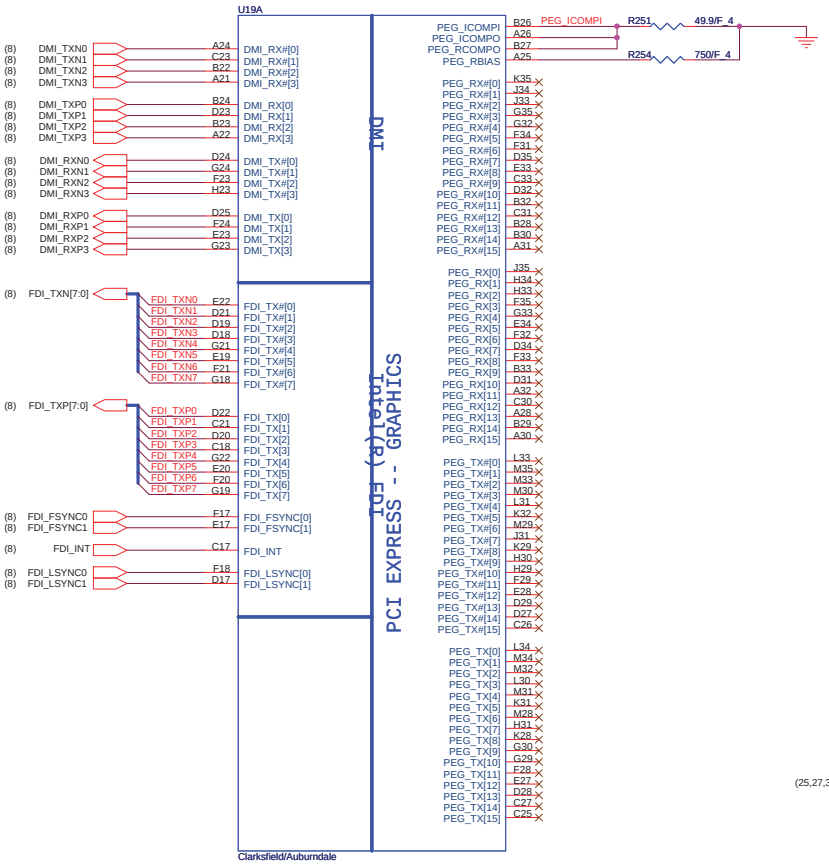

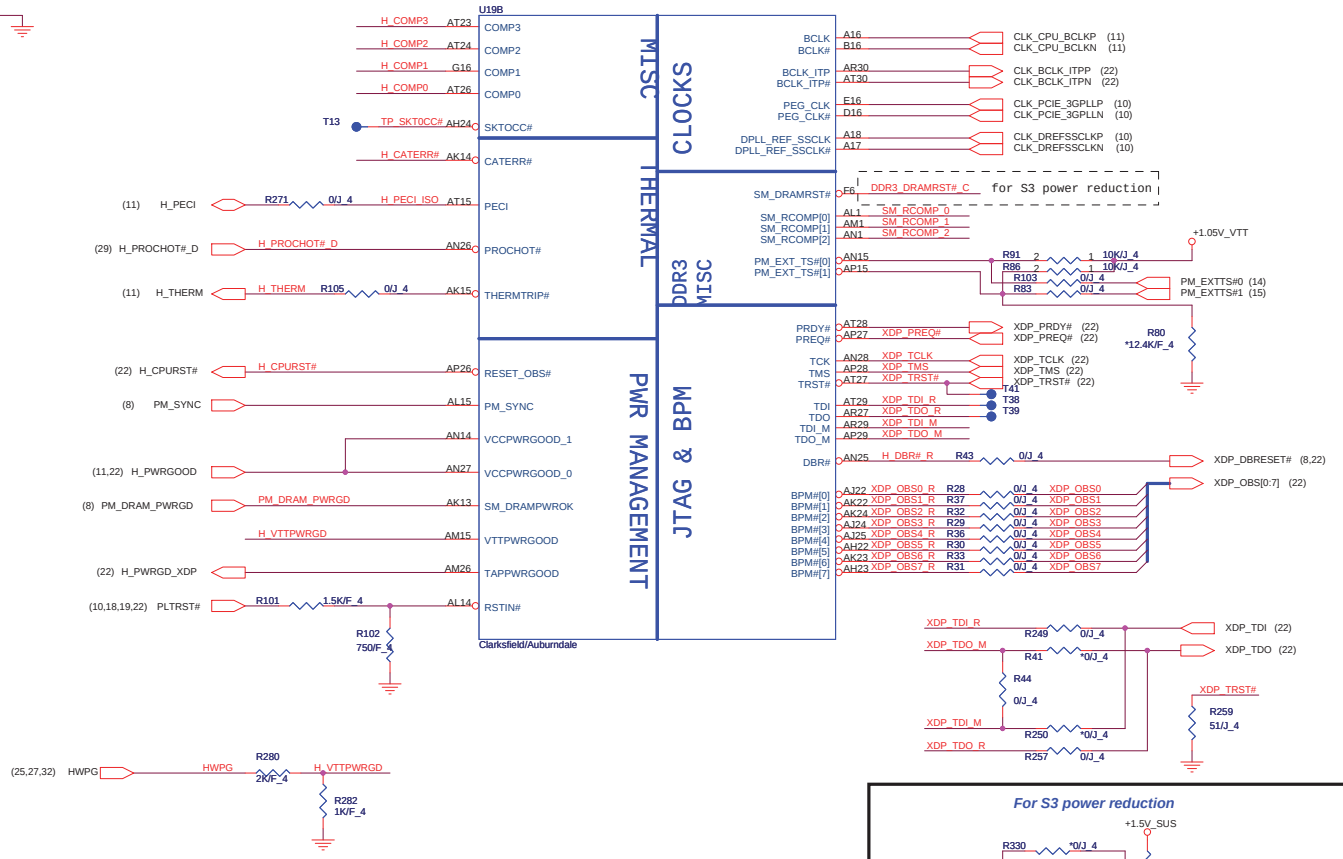

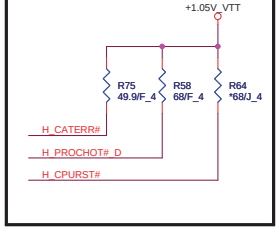

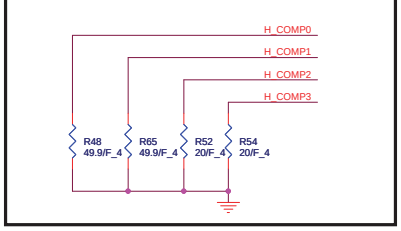

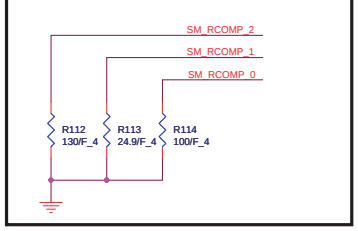

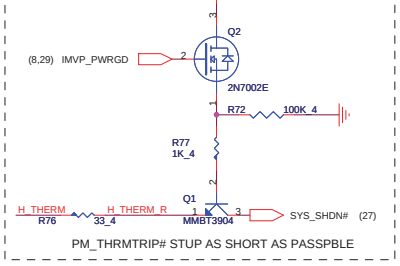

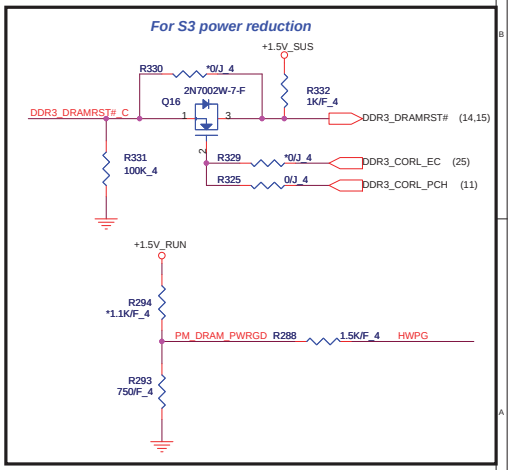

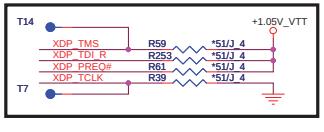

Quanta Computer Inc.

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ARRANDALE PROCESSOR (DDR3)

05

U19C

DDR SYSTEM MEMORY A

(14) M_A_DQ[63:0]

M_A_DQ0 A10 SA_DQ[0]
M_A_DQ1 C10 SA_DQ[1]
M_A_DQ2 C7 SA_DQ[2]
M_A_DQ3 A7 SA_DQ[3]
M_A_DQ4 B10 SA_DQ[4]
M_A_DQ5 D10 SA_DQ[5]
M_A_DQ6 E10 SA_DQ[6]
M_A_DQ7 A8 SA_DQ[7]
M_A_DQ8 D8 SA_DQ[8]
M_A_DQ9 F10 SA_DQ[9]
M_A_DQ10 E6 SA_DQ[10]
M_A_DQ11 E7 SA_DQ[11]
M_A_DQ12 E9 SA_DQ[12]
M_A_DQ13 B7 SA_DQ[13]
M_A_DQ14 E7 SA_DQ[14]
M_A_DQ15 C6 SA_DQ[15]
M_A_DQ16 H10 SA_DQ[16]
M_A_DQ17 G8 SA_DQ[17]
M_A_DQ18 K7 SA_DQ[18]
M_A_DQ19 J8 SA_DQ[19]
M_A_DQ20 G7 SA_DQ[20]
M_A_DQ21 G10 SA_DQ[21]
M_A_DQ22 J7 SA_DQ[22]
M_A_DQ23 J10 SA_DQ[23]
M_A_DQ24 L7 SA_DQ[24]
M_A_DQ25 M6 SA_DQ[25]
M_A_DQ26 M8 SA_DQ[26]
M_A_DQ27 L9 SA_DQ[27]
M_A_DQ28 L6 SA_DQ[28]
M_A_DQ29 K8 SA_DQ[29]
M_A_DQ30 N8 SA_DQ[30]
M_A_DQ31 P9 SA_DQ[31]
M_A_DQ32 AH5 SA_DQ[32]
M_A_DQ33 AF5 SA_DQ[33]
M_A_DQ34 AK6 SA_DQ[34]
M_A_DQ35 AK7 SA_DQ[35]
M_A_DQ36 AF6 SA_DQ[36]
M_A_DQ37 AG5 SA_DQ[37]
M_A_DQ38 AJ7 SA_DQ[38]
M_A_DQ39 AJ6 SA_DQ[39]
M_A_DQ40 AJ10 SA_DQ[40]
M_A_DQ41 AJ9 SA_DQ[41]
M_A_DQ42 AL10 SA_DQ[42]
M_A_DQ43 AK12 SA_DQ[43]
M_A_DQ44 AK8 SA_DQ[44]
M_A_DQ45 AL7 SA_DQ[45]
M_A_DQ46 AK11 SA_DQ[46]
M_A_DQ47 AL8 SA_DQ[47]
M_A_DQ48 AN8 SA_DQ[48]
M_A_DQ49 AM10 SA_DQ[49]
M_A_DQ50 AR11 SA_DQ[50]
M_A_DQ51 AL11 SA_DQ[51]
M_A_DQ52 AM9 SA_DQ[52]
M_A_DQ53 AN9 SA_DQ[53]
M_A_DQ54 AT11 SA_DQ[54]
M_A_DQ55 AP12 SA_DQ[55]
M_A_DQ56 AM12 SA_DQ[56]
M_A_DQ57 AN12 SA_DQ[57]
M_A_DQ58 AM13 SA_DQ[58]
M_A_DQ59 AT14 SA_DQ[59]
M_A_DQ60 AT12 SA_DQ[60]
M_A_DQ61 AL13 SA_DQ[61]
M_A_DQ62 AR14 SA_DQ[62]
M_A_DQ63 AP14 SA_DQ[63]

(14) M_A_BS0 AC3 SA_BS[0]
(14) M_A_BS1 AB2 SA_BS[1]
(14) M_A_BS2 U7 SA_BS[2]

(14) M_A_CAS# AE1 SA_CAS#
(14) M_A_RAS# AB3 SA_RAS#
(14) M_A_WE# AE9 SA_WE#

SA_CK[0] AA6 M_A_CLKP0 (14)
SA_CK#[0] AA7 M_A_CLKN0 (14)
SA_CKE[0] P7 M_A_CKE0 (14)

SA_CK[1] Y6 M_A_CLKP1 (14)
SA_CK#[1] Y5 M_A_CLKN1 (14)
SA_CKE[1] P6 M_A_CKE1 (14)

SA_CS#[0] AE2 M_A_CS0# (14)
SA_CS#[1] AE8 M_A_CS1# (14)

SA_ODT[0] AD8 M_A_ODT0 (14)
SA_ODT[1] AF9 M_A_ODT1 (14)

SA_DM[0] B9 M_A_DM0
SA_DM[1] D7 M_A_DM1
SA_DM[2] H7 M_A_DM2
SA_DM[3] M7 M_A_DM3
SA_DM[4] AG6 M_A_DM4
SA_DM[5] AM7 M_A_DM5
SA_DM[6] AN10 M_A_DM6
SA_DM[7] AN13 M_A_DM7
M_A_DM[7:0] (14)

SA_DQS#[0] C9 M_A_DQSN0
SA_DQS#[1] F8 M_A_DQSN1
SA_DQS#[2] J9 M_A_DQSN2
SA_DQS#[3] N9 M_A_DQSN3
SA_DQS#[4] AH7 M_A_DQSN4
SA_DQS#[5] AK9 M_A_DQSN5
SA_DQS#[6] AP11 M_A_DQSN6
SA_DQS#[7] AT13 M_A_DQSN7
M_A_DQSN[7:0] (14)

SA_DQS[0] C8 M_A_DQSP0
SA_DQS[1] F9 M_A_DQSP1
SA_DQS[2] H9 M_A_DQSP2
SA_DQS[3] M9 M_A_DQSP3
SA_DQS[4] AH8 M_A_DQSP4
SA_DQS[5] AK10 M_A_DQSP5
SA_DQS[6] AN11 M_A_DQSP6
SA_DQS[7] AR13 M_A_DQSP7
M_A_DQSP[7:0] (14)

SA_MA[0] Y3 M_A_A0
SA_MA[1] W1 M_A_A1
SA_MA[2] AA8 M_A_A2
SA_MA[3] AA3 M_A_A3
SA_MA[4] V1 M_A_A4
SA_MA[5] AA9 M_A_A5
SA_MA[6] V8 M_A_A6
SA_MA[7] T1 M_A_A7
SA_MA[8] Y9 M_A_A8
SA_MA[9] U6 M_A_A9
SA_MA[10] AD4 M_A_A10
SA_MA[11] T2 M_A_A11
SA_MA[12] U3 M_A_A12
SA_MA[13] AG8 M_A_A13
SA_MA[14] T3 M_A_A14
SA_MA[15] V9 M_A_A15
M_A_A[15:0] (14)

Clarksfield/Auburndale

Channel A DQ[15,32,48,54], DM[5]
Requires minimum 12mils spacing
with all other signals, including data signals.

U19D

DDR SYSTEM MEMORY - B

(15) M_B_DQ[63:0]

M_B_DQ0 B5 SB_DQ[0]
M_B_DQ1 A5 SB_DQ[1]
M_B_DQ2 C3 SB_DQ[2]
M_B_DQ3 B3 SB_DQ[3]
M_B_DQ4 E4 SB_DQ[4]
M_B_DQ5 A6 SB_DQ[5]
M_B_DQ6 A4 SB_DQ[6]
M_B_DQ7 C4 SB_DQ[7]
M_B_DQ8 D1 SB_DQ[8]
M_B_DQ9 D2 SB_DQ[9]
M_B_DQ10 F2 SB_DQ[10]
M_B_DQ11 F1 SB_DQ[11]
M_B_DQ12 C2 SB_DQ[12]
M_B_DQ13 F5 SB_DQ[13]
M_B_DQ14 F3 SB_DQ[14]
M_B_DQ15 G4 SB_DQ[15]
M_B_DQ16 H6 SB_DQ[16]
M_B_DQ17 G2 SB_DQ[17]
M_B_DQ18 J6 SB_DQ[18]
M_B_DQ19 J3 SB_DQ[19]
M_B_DQ20 G1 SB_DQ[20]
M_B_DQ21 G5 SB_DQ[21]
M_B_DQ22 J2 SB_DQ[22]
M_B_DQ23 J1 SB_DQ[23]
M_B_DQ24 J5 SB_DQ[24]
M_B_DQ25 K2 SB_DQ[25]
M_B_DQ26 L3 SB_DQ[26]
M_B_DQ27 M1 SB_DQ[27]
M_B_DQ28 K5 SB_DQ[28]
M_B_DQ29 K4 SB_DQ[29]
M_B_DQ30 M4 SB_DQ[30]
M_B_DQ31 N5 SB_DQ[31]
M_B_DQ32 AF3 SB_DQ[32]
M_B_DQ33 AG1 SB_DQ[33]
M_B_DQ34 AJ3 SB_DQ[34]
M_B_DQ35 AK1 SB_DQ[35]
M_B_DQ36 AG4 SB_DQ[36]
M_B_DQ37 AG3 SB_DQ[37]
M_B_DQ38 AJ4 SB_DQ[38]
M_B_DQ39 AH4 SB_DQ[39]
M_B_DQ40 AK3 SB_DQ[40]
M_B_DQ41 AK4 SB_DQ[41]
M_B_DQ42 AM6 SB_DQ[42]
M_B_DQ43 AN2 SB_DQ[43]
M_B_DQ44 AK5 SB_DQ[44]
M_B_DQ45 AK2 SB_DQ[45]
M_B_DQ46 AM4 SB_DQ[46]
M_B_DQ47 AM3 SB_DQ[47]
M_B_DQ48 AP3 SB_DQ[48]
M_B_DQ49 AN5 SB_DQ[49]
M_B_DQ50 AT4 SB_DQ[50]
M_B_DQ51 AN6 SB_DQ[51]
M_B_DQ52 AN4 SB_DQ[52]
M_B_DQ53 AN3 SB_DQ[53]
M_B_DQ54 AT5 SB_DQ[54]
M_B_DQ55 AT6 SB_DQ[55]
M_B_DQ56 AN7 SB_DQ[56]
M_B_DQ57 AP6 SB_DQ[57]
M_B_DQ58 AP8 SB_DQ[58]
M_B_DQ59 AT9 SB_DQ[59]
M_B_DQ60 AT7 SB_DQ[60]
M_B_DQ61 AP9 SB_DQ[61]
M_B_DQ62 AR10 SB_DQ[62]
M_B_DQ63 AT10 SB_DQ[63]

(15) M_B_BS0 AB1 SB_BS[0]
(15) M_B_BS1 W5 SB_BS[1]
(15) M_B_BS2 R7 SB_BS[2]

(15) M_B_CAS# AC5 SB_CAS#
(15) M_B_RAS# Y7 SB_RAS#
(15) M_B_WE# AC6 SB_WE#

SB_CK[0] W8 M_B_CLKP0 (15)
SB_CK#[0] W9 M_B_CLKN0 (15)
SB_CKE[0] M3 M_B_CKE0 (15)

SB_CK[1] V7 M_B_CLKP1 (15)
SB_CK#[1] V6 M_B_CLKN1 (15)
SB_CKE[1] M2 M_B_CKE1 (15)

SB_CS#[0] AB8 M_B_CS0# (15)
SB_CS#[1] AD6 M_B_CS1# (15)

SB_ODT[0] AC7 M_B_ODT0 (15)
SB_ODT[1] AD1 M_B_ODT1 (15)

SB_DM[0] D4 M_B_DM0
SB_DM[1] F1 M_B_DM1
SB_DM[2] H3 M_B_DM2
SB_DM[3] K1 M_B_DM3
SB_DM[4] AH1 M_B_DM4
SB_DM[5] AL2 M_B_DM5
SB_DM[6] AR4 M_B_DM6
SB_DM[7] AT8 M_B_DM7
M_B_DM[7:0] (15)

SB_DQS#[0] D5 M_B_DQSN0
SB_DQS#[1] F4 M_B_DQSN1
SB_DQS#[2] J4 M_B_DQSN2
SB_DQS#[3] L4 M_B_DQSN3
SB_DQS#[4] AH2 M_B_DQSN4
SB_DQS#[5] AL4 M_B_DQSN5
SB_DQS#[6] AR5 M_B_DQSN6
SB_DQS#[7] AR8 M_B_DQSN7
M_B_DQSN[7:0] (15)

SB_DQS[0] C5 M_B_DQSP0
SB_DQS[1] E3 M_B_DQSP1
SB_DQS[2] H4 M_B_DQSP2
SB_DQS[3] M5 M_B_DQSP3
SB_DQS[4] AG2 M_B_DQSP4
SB_DQS[5] AL5 M_B_DQSP5
SB_DQS[6] AP5 M_B_DQSP6
SB_DQS[7] AR7 M_B_DQSP7
M_B_DQSP[7:0] (15)

SB_MA[0] U5 M_B_A0
SB_MA[1] V2 M_B_A1
SB_MA[2] T5 M_B_A2
SB_MA[3] V3 M_B_A3
SB_MA[4] R1 M_B_A4
SB_MA[5] T8 M_B_A5
SB_MA[6] R2 M_B_A6
SB_MA[7] R6 M_B_A7
SB_MA[8] R4 M_B_A8
SB_MA[9] R5 M_B_A9
SB_MA[10] AB5 M_B_A10
SB_MA[11] P3 M_B_A11
SB_MA[12] R3 M_B_A12
SB_MA[13] AF7 M_B_A13
SB_MA[14] P5 M_B_A14
SB_MA[15] N1 M_B_A15
M_B_A[15:0] (15)

Clarksfield/Auburndale

Channel B DQ[16,18,36,42,56,57,60,61,62]
Requires minimum 12mils spacing
with all other signals, including data signals.

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CPU Core Power

ARRANDALE PROCESSOR (GRAPHICS POWER)

+VCC_CORE=4.8 max

+1.05V_VTT=1.8 max

U19F

U19G

CPU CORE SUPPLY 1.1V RAIL POWER

CPU VIDS

SENSE LINES

GRAPHICS VIDS SENSE LINES

GRAPHICS POWER

DDR3 - 1.5V RAILS

FDI PEG & DMI 1.1V 1.8V

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for intel validation purpose.

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

Clarksfield/Auburndale

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

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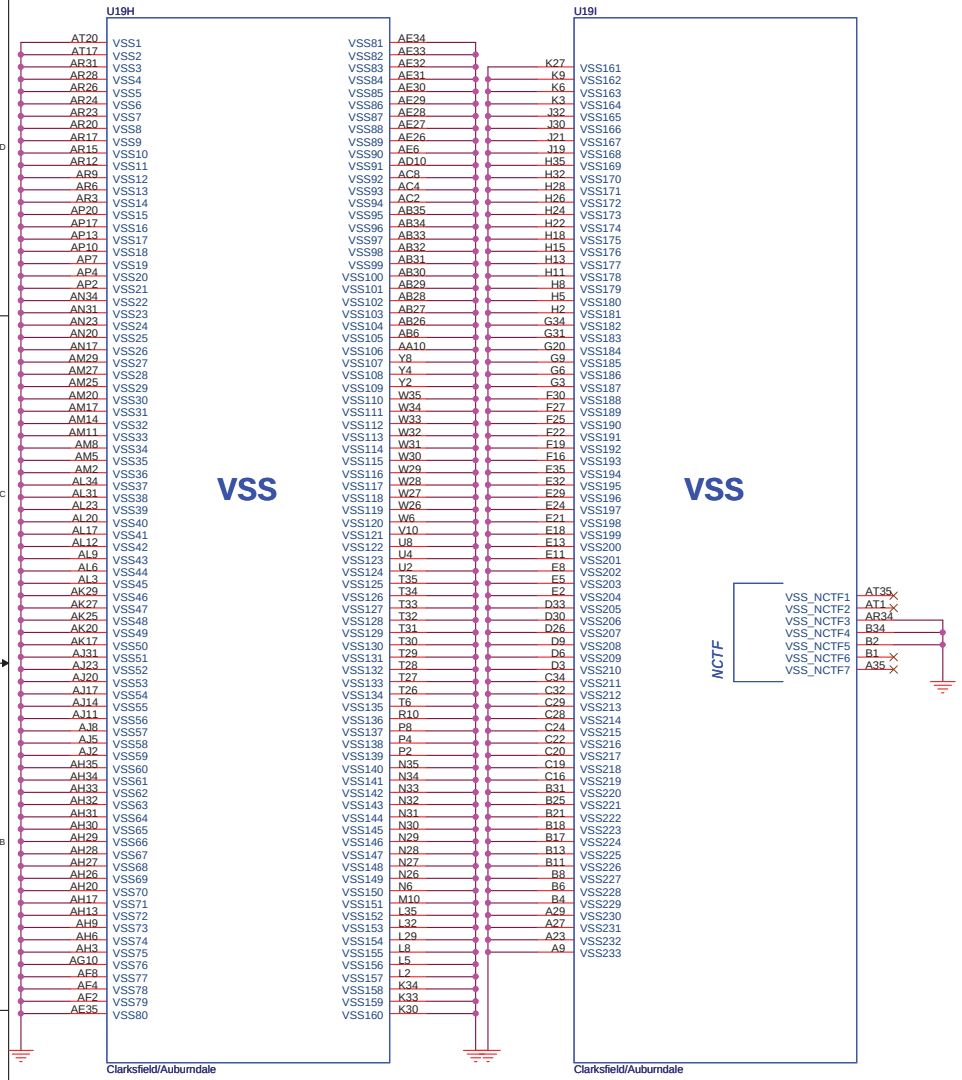
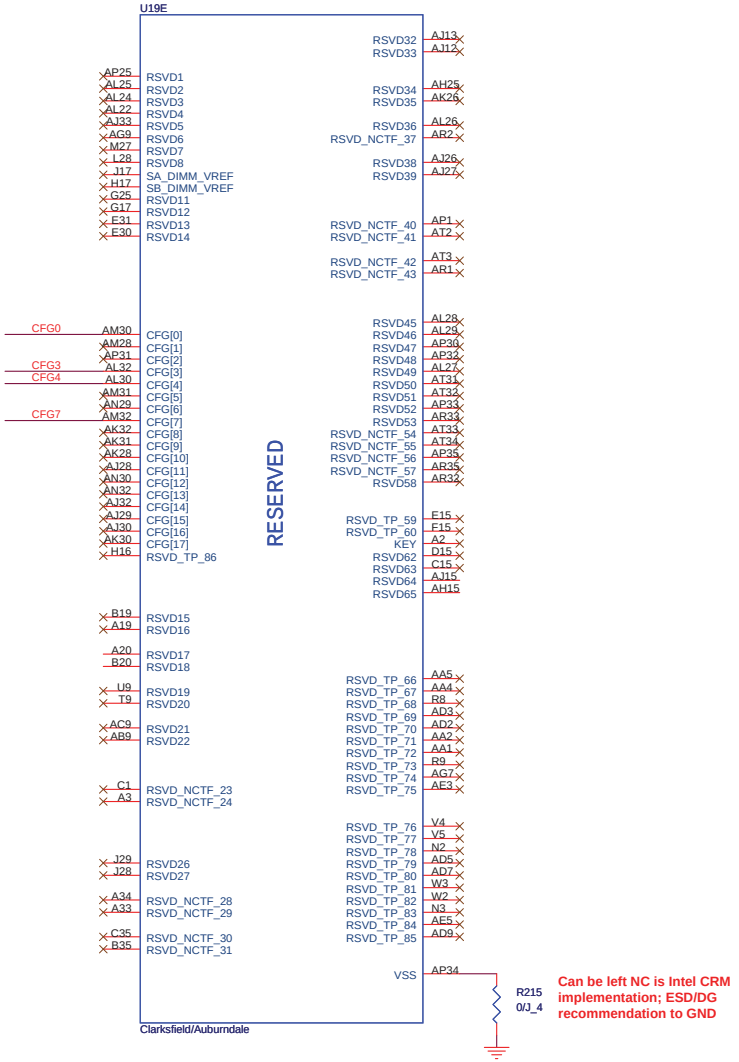
ARRANDALE PROCESSOR (GND)

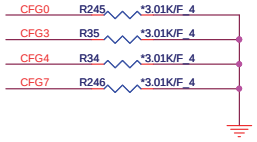


ARRANDALE PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

Quanta Computer Inc.
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	ARRANDALE 4/4	1A
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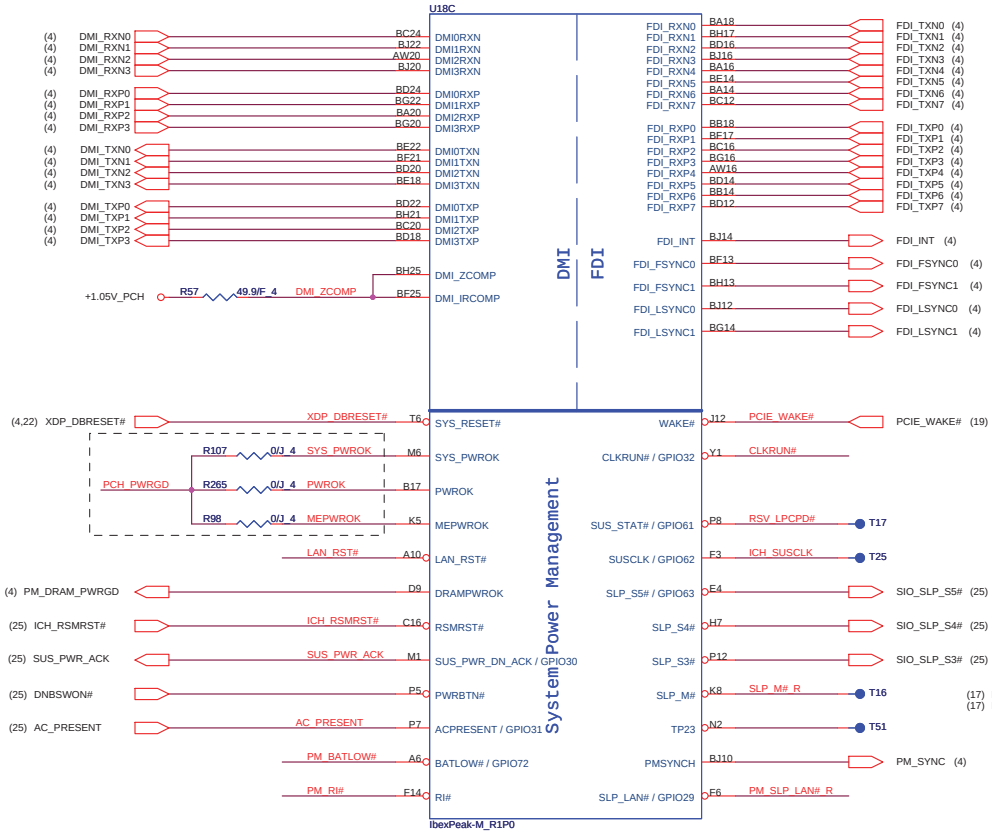
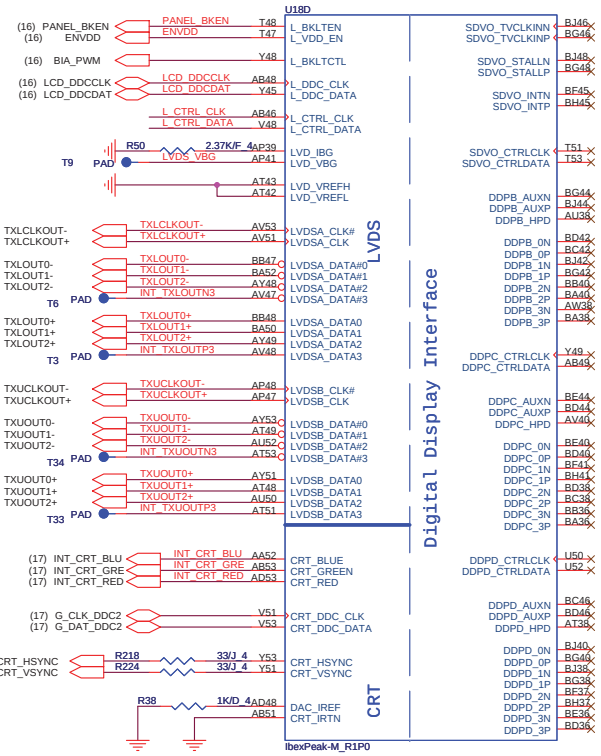
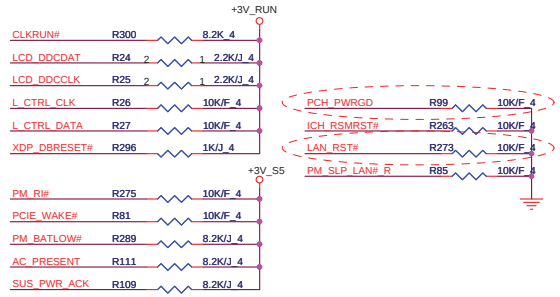
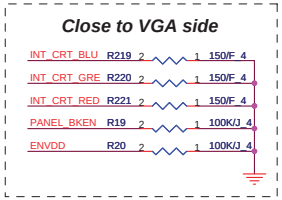
IBEX PEAK-M (DMI,FDI,GPIO)

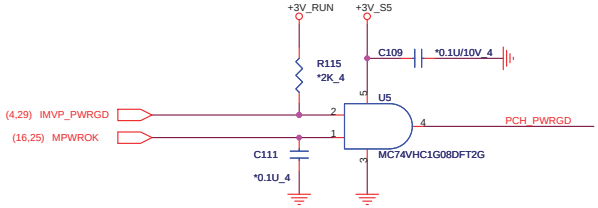


IBEX PEAK-M (LVDS,DDI)









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	IBEX PEAK-M 1/6	1A

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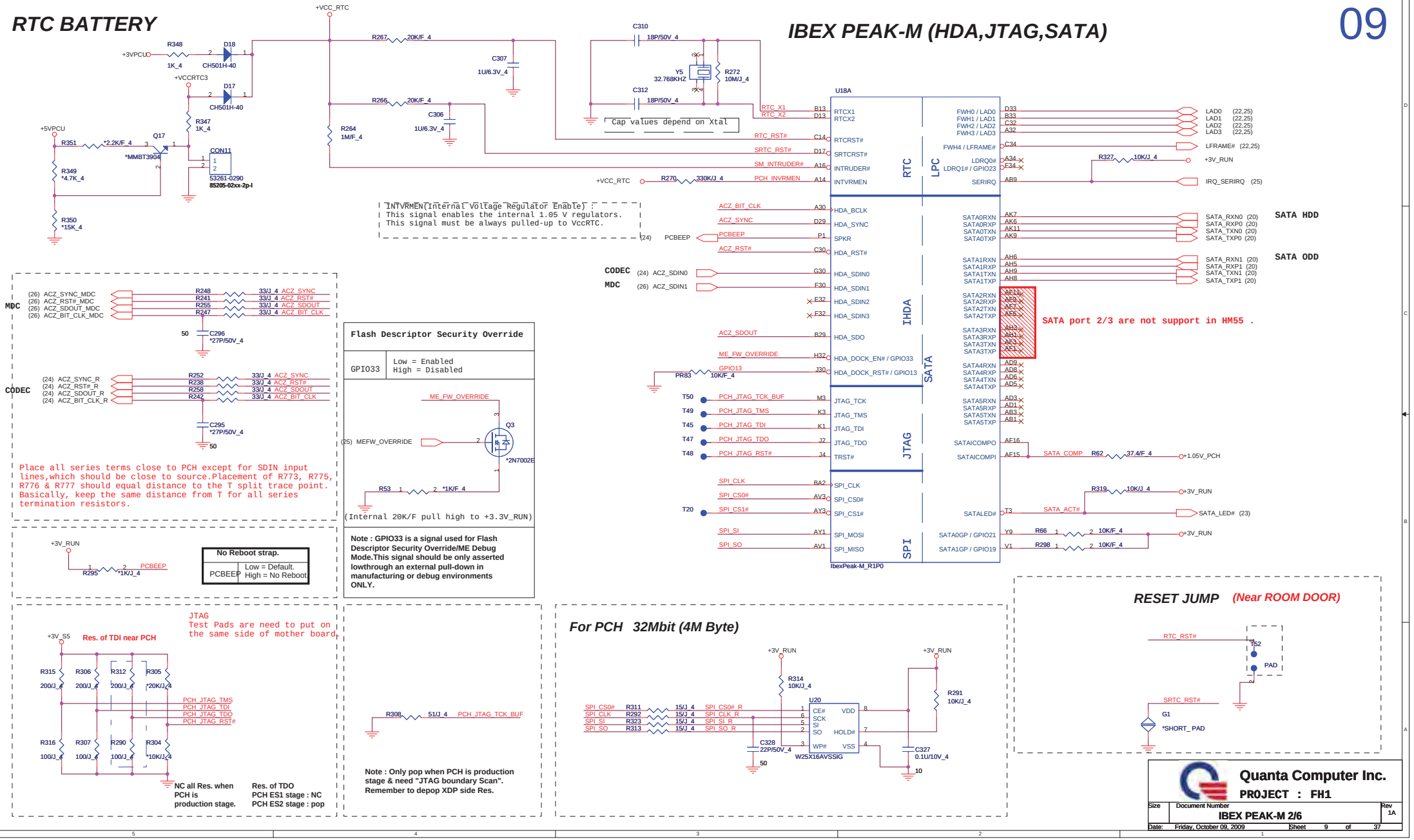
RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09



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PROJECT : FH1

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	IBEX PEAK-M 2/6	1A

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IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.

PCIE port 7/8 are not support in HM55 .

USB port 6/7 are not support in HM55 .

USB PORT 1(DB)
USB PORT 2(MB)
USB PORT 4(MB)
CAMERA
BT
WLAN
CARD READER

PCIRST#:
DG(V1.0) P277
Can be left unconnected.

PAR:
SC(V1.0) P36
Can be left unconnected
if not using PCI.

PME:
DG(V1.0) P277
Can be left unconnected.

CLKOUT_PCI[0..4]:
22 ohm series resistor is recommend
(single & double load) on PDG v1.1

OC0#~OC7#:
DG(V1.0)P214
Pin Default Port Mapping
OC0# Port0,Port1
OC1# Port2,Port3
OC2# Port4,Port5

CLKOUT_PEG_A_P/N,CLKOUT_PEG_B_P/N,
CLKOUT_DMI_P/N,support GEN-1 and GEN-2

SML0CLK/SML0DATA:
DG(V1.1) P255: The 82577 SMBus signals (SMB_DATA and SMB_CLK) cannot be connected to any other devices other than the PCH. Connect the SMB_DATA and SMB_CLK pins to the PCH SML0DATA and SML0CLK pins, respectively.

FOR DDR3 SPD/CLOCK GE
EXPRESS CARD/MINI CAR
0 FOR INTEL LAN
1 FOR EC

CLKOUTFLEX3:
EDS(V1.0) :support 48MHz
33MHz and 14.31818MHz.

CLKOUTFLEX[0..3]:
PDG v1.1: 22 ohm series resistor is
recommend (PCI & non PCI routing,
single & double load)

PCIECLKRQ{0,3,4,5,6,7}# should have a
10K pull-up to +V3.3A.PCIECLKRQ{1,2}
should have a 10K pull-up to +3.3S

Reserve capacitor pads for improving WWAN.

Non-iAMT

Add Buffers as needed for Loading and fanout concerns.

Boot BIOS Strap

PCI_GNT0#	GNT#1	Boot BIOS Location
0	0	LPC
0	1	PCI
1	0	Reserved (NAND)
1	1	SPI

Quanta Computer Inc.
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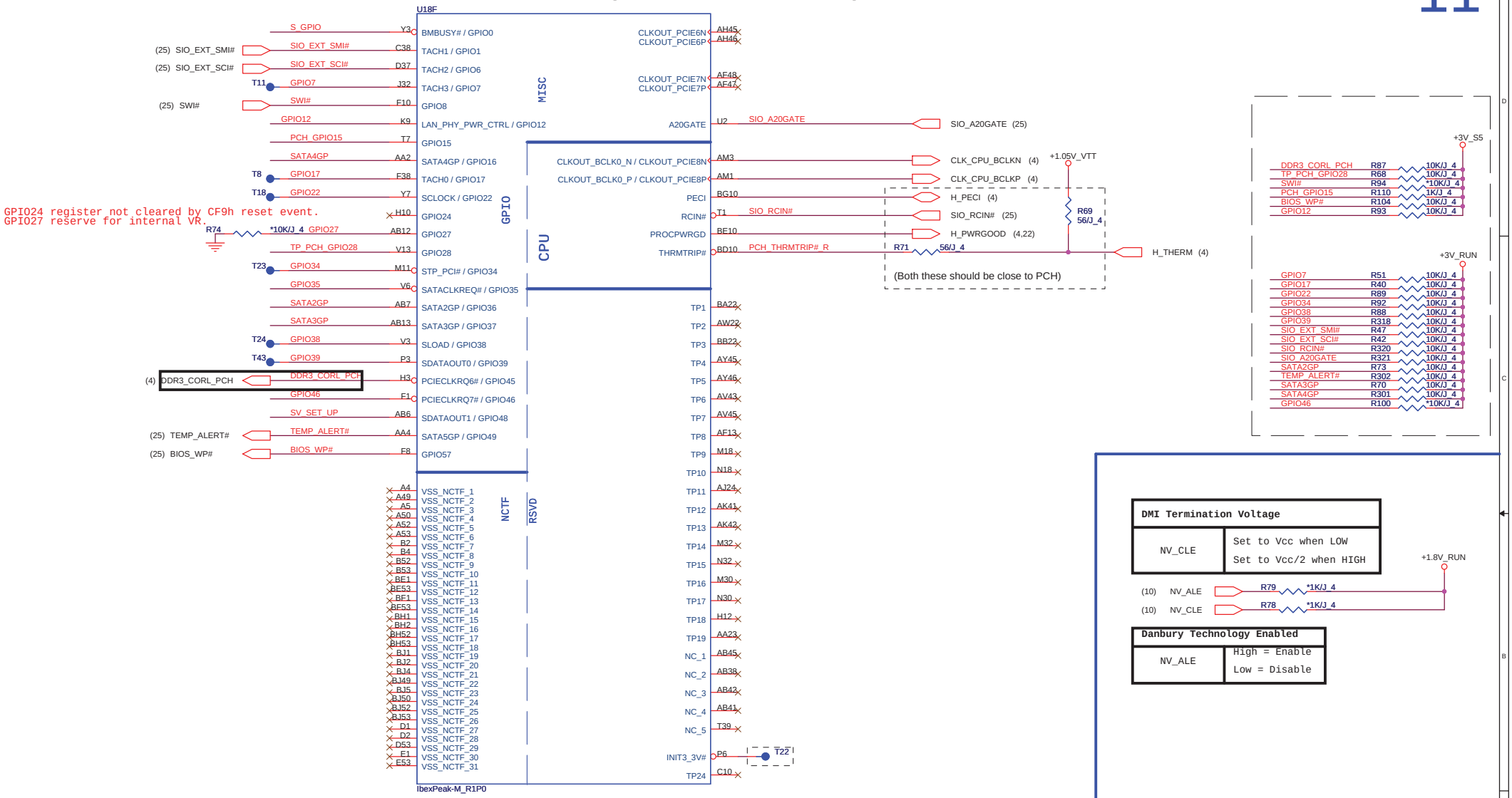
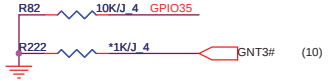
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



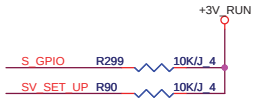
DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default

Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high



BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is for intel BIOS validation purpose.

Quanta Computer Inc.
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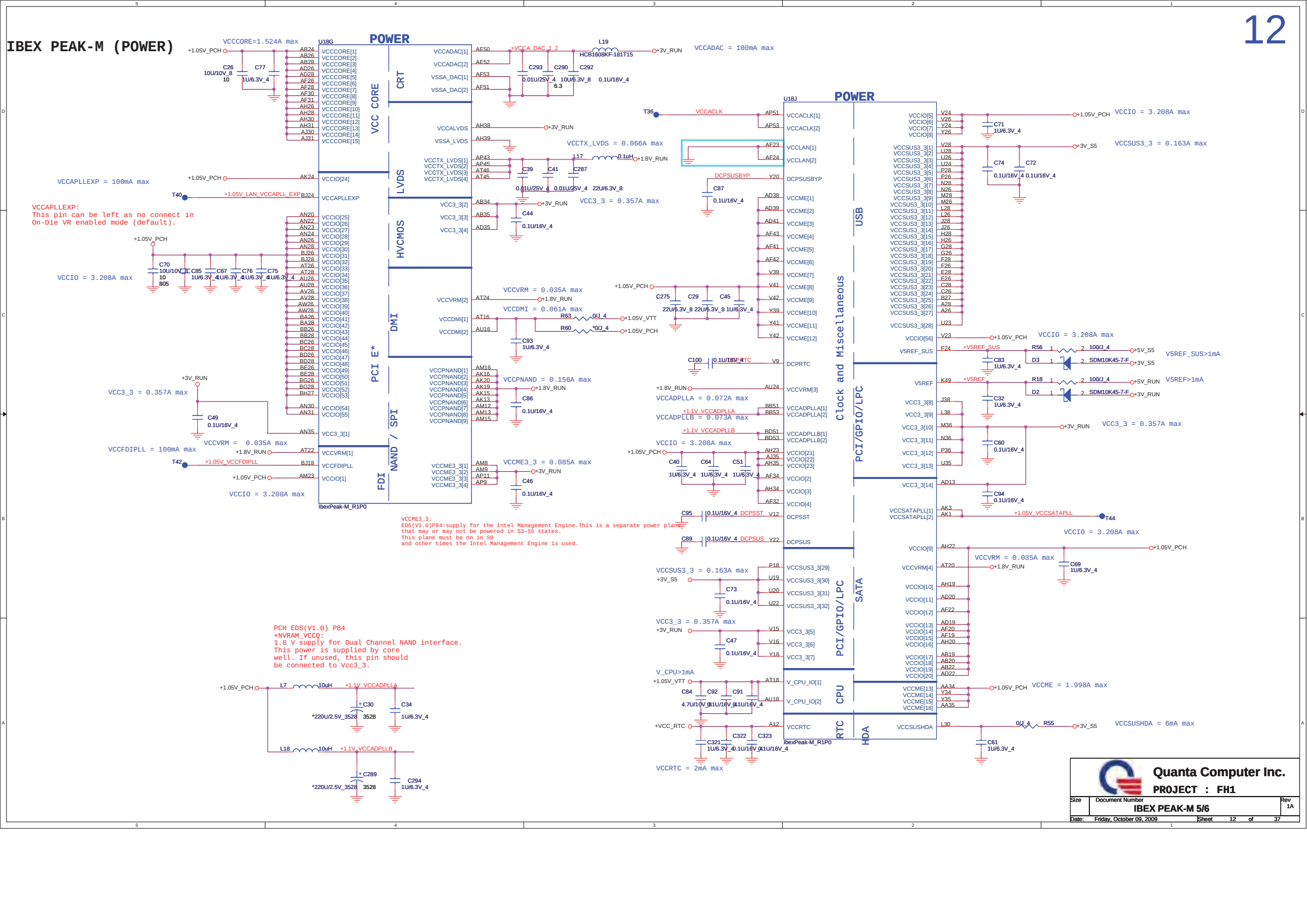
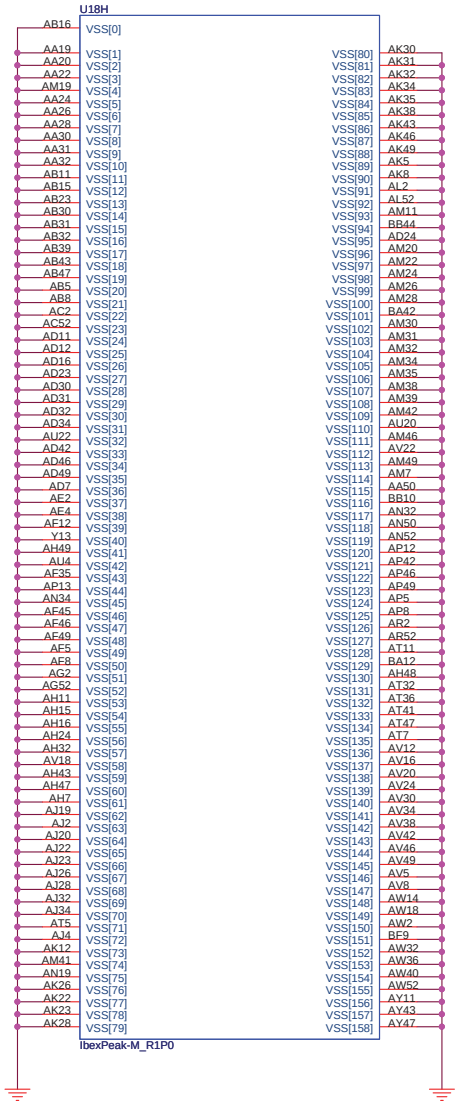
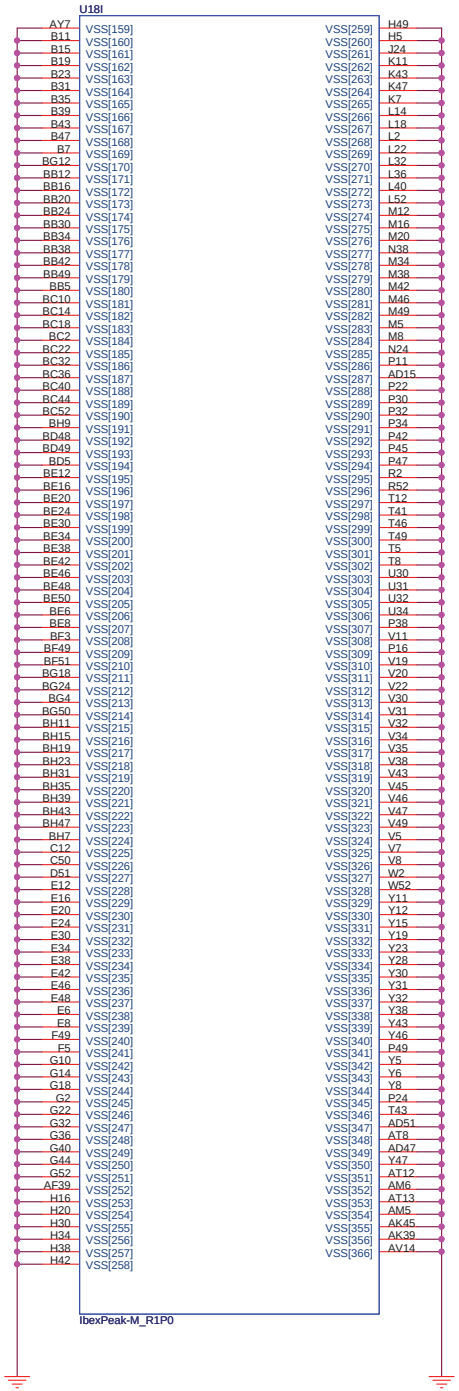
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





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PROJECT : FH1

Size	Document Number	Rev
	IBEX PEAK-M 6/6	1A

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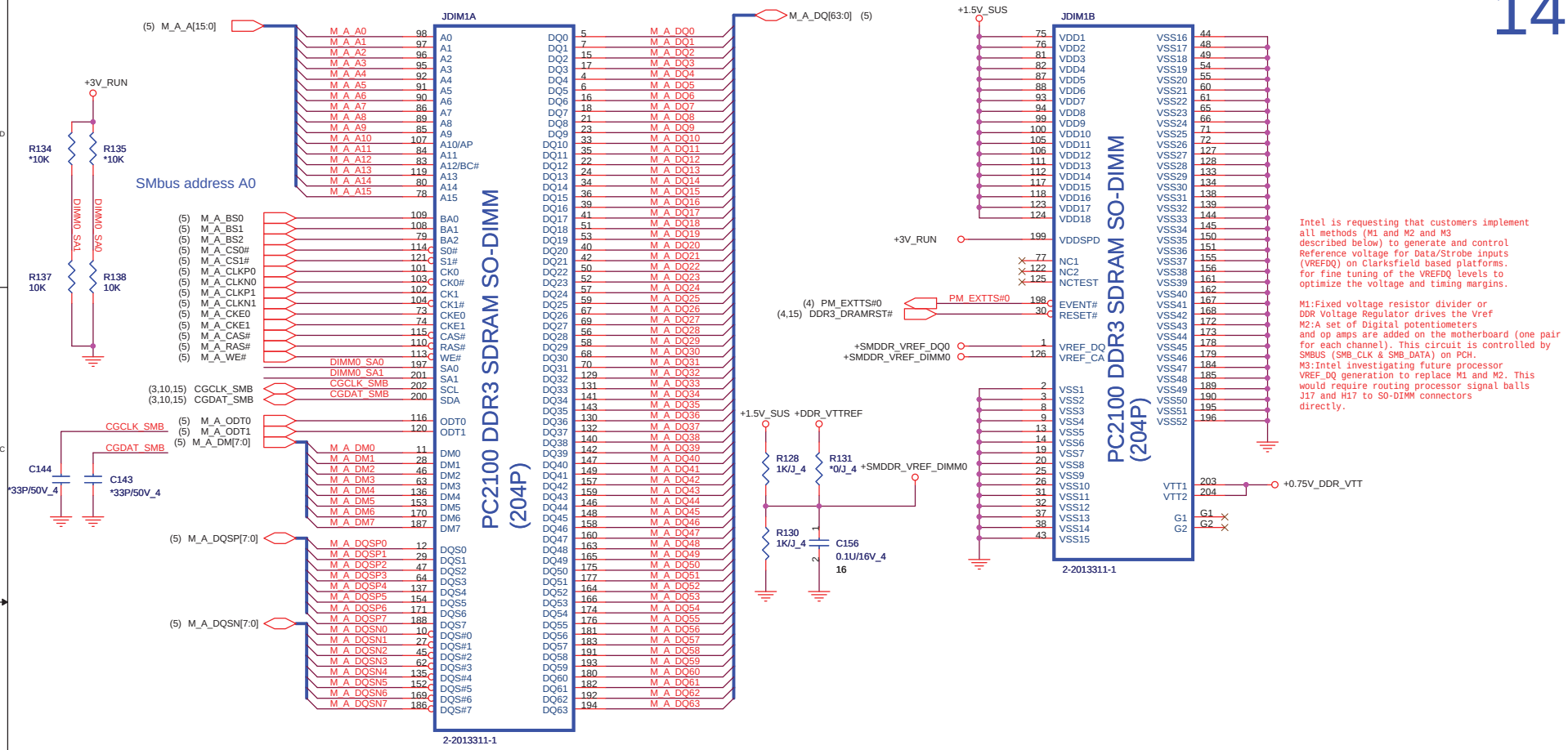
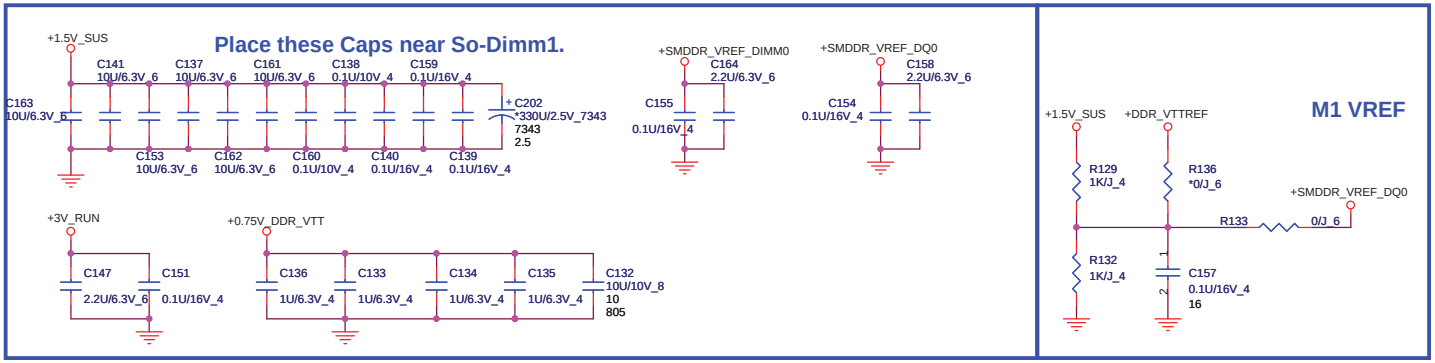


Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DDR3 DIMM-1	Rev: 1A
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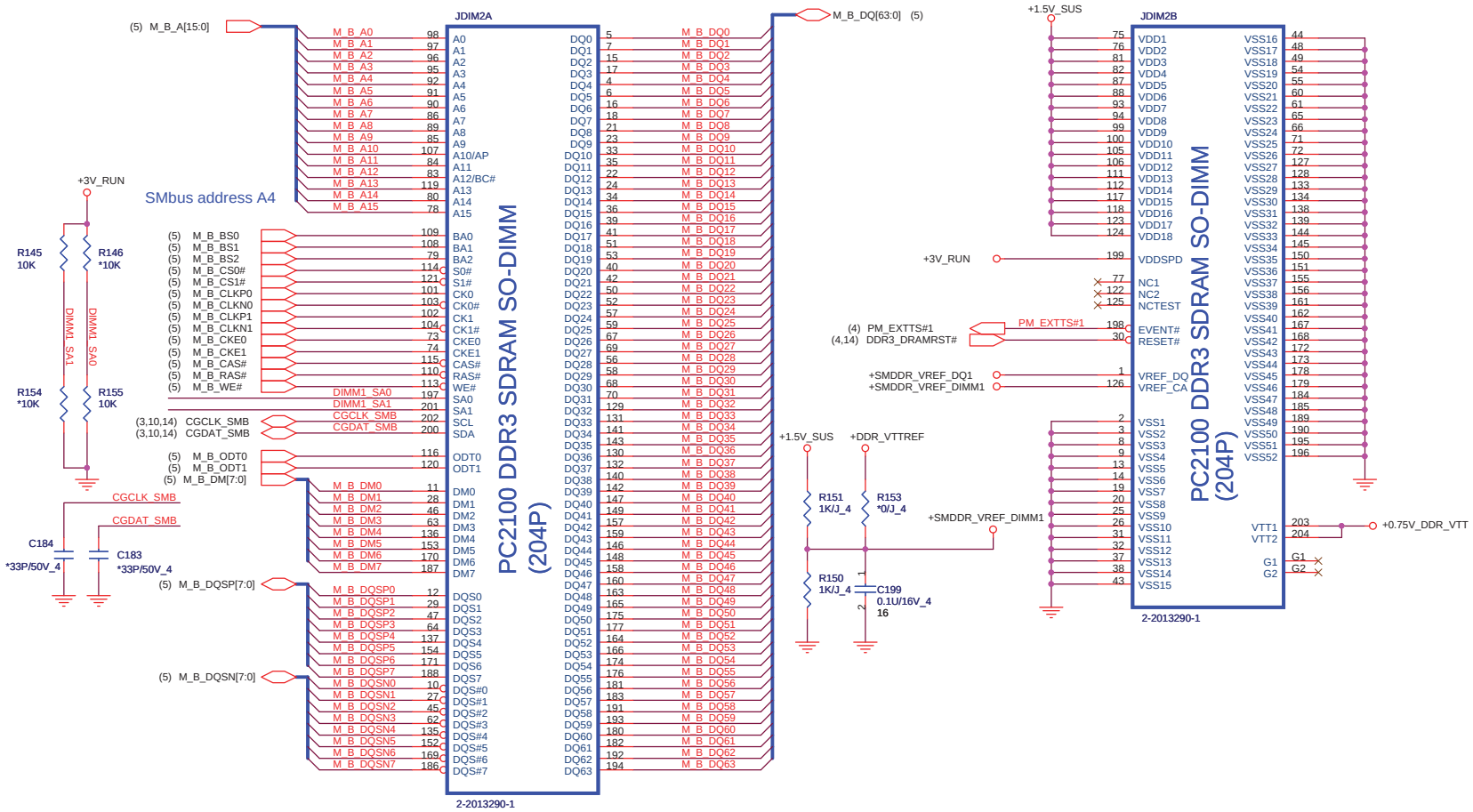

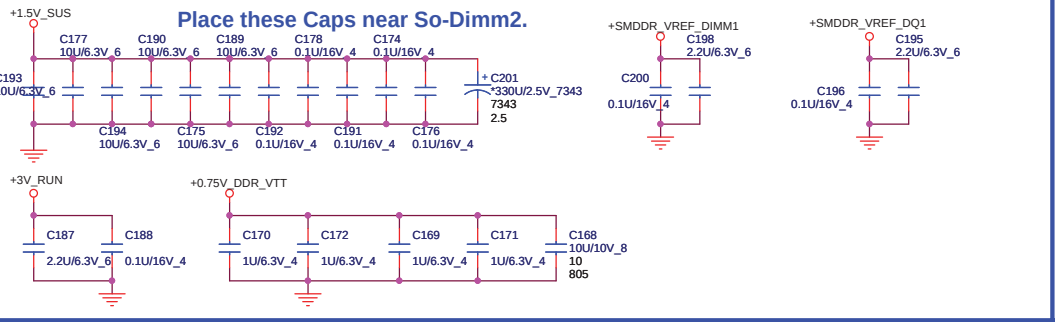

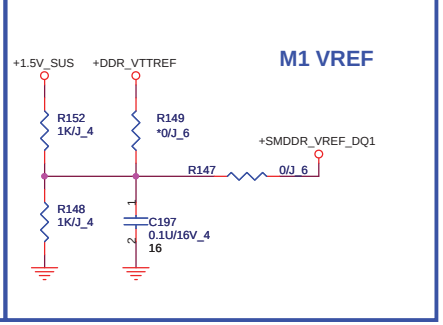

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PROJECT : FH1

Size	Document Number	Rev
	DDR3 DIMM-2	1A
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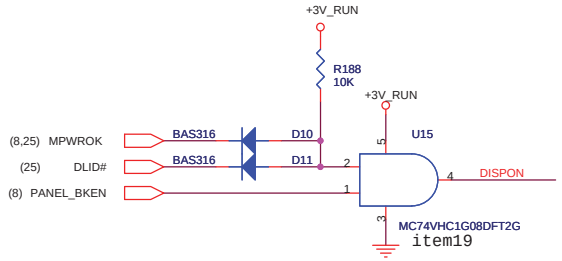
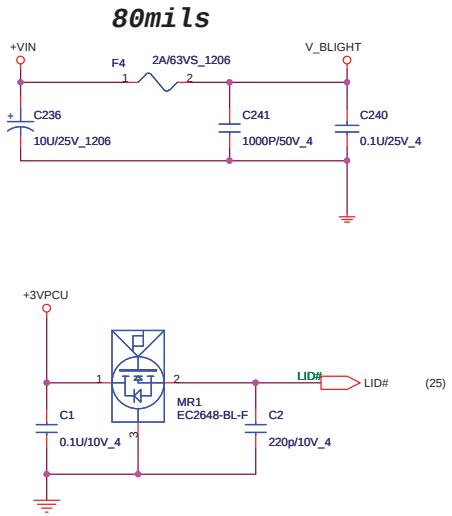
Backlight Control(LDS)

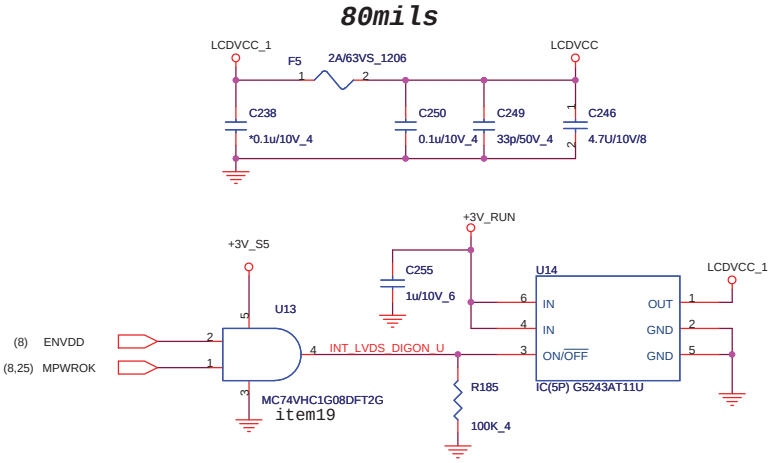


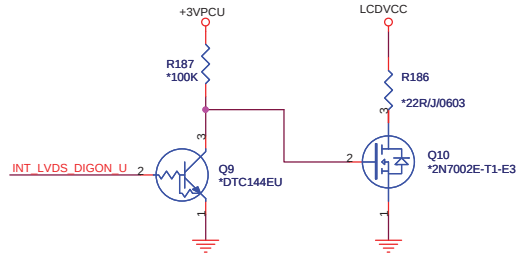
BACKLIGHT POWER



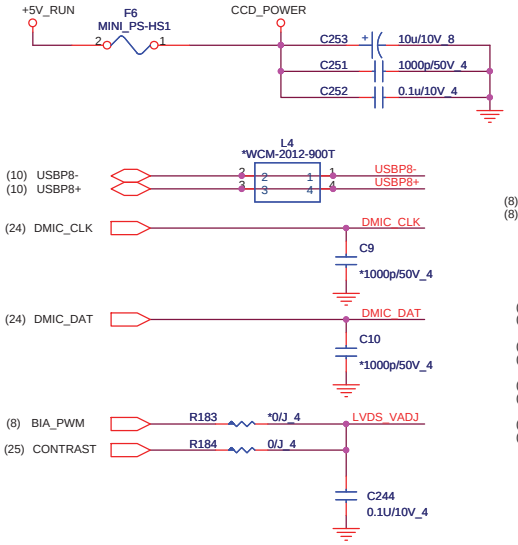
LED Panel POWER SWITCH(LVDS)

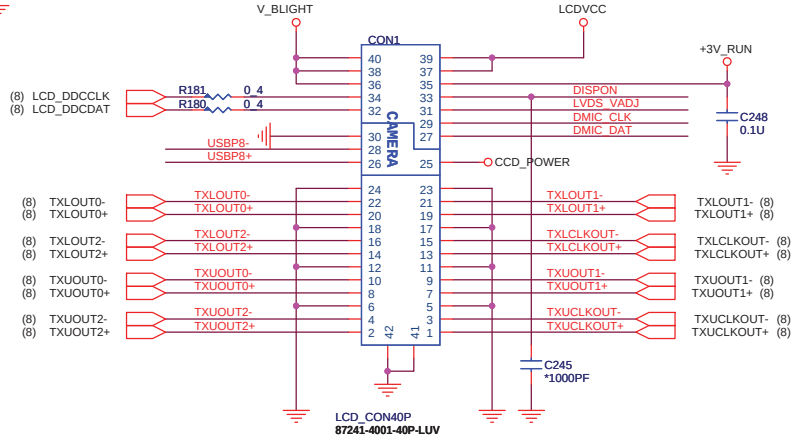
16





LVDS/CCD





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PROJECT : FH1

Size	Document Number	Rev
	LCD/LED Panel/CCD	1A
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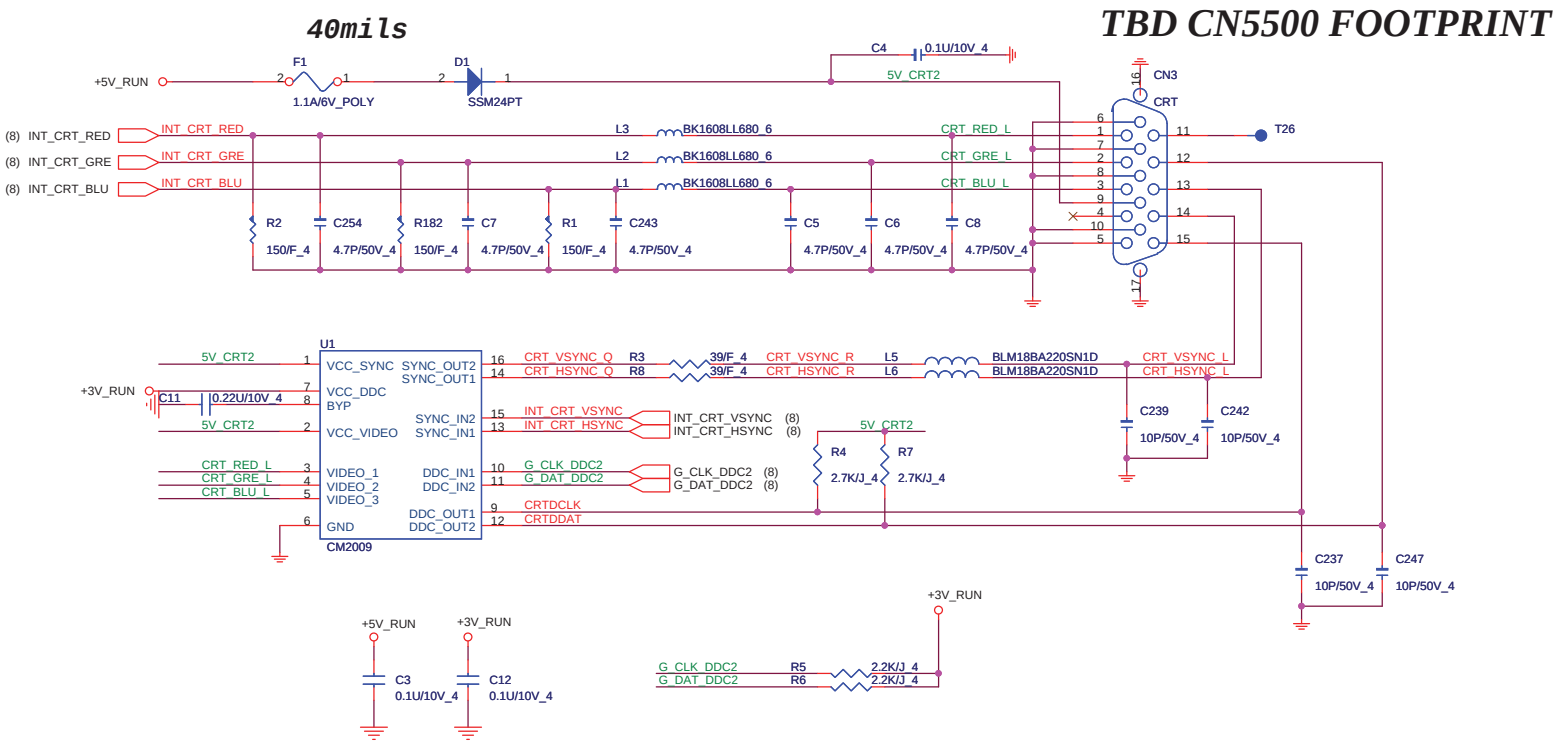
CRT CONN/DDC LEVEL SHIFT



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PROJECT : FH1		
Size	Document Number: CRT CONN/DDC LEVEL SHIFT	Rev: 1A
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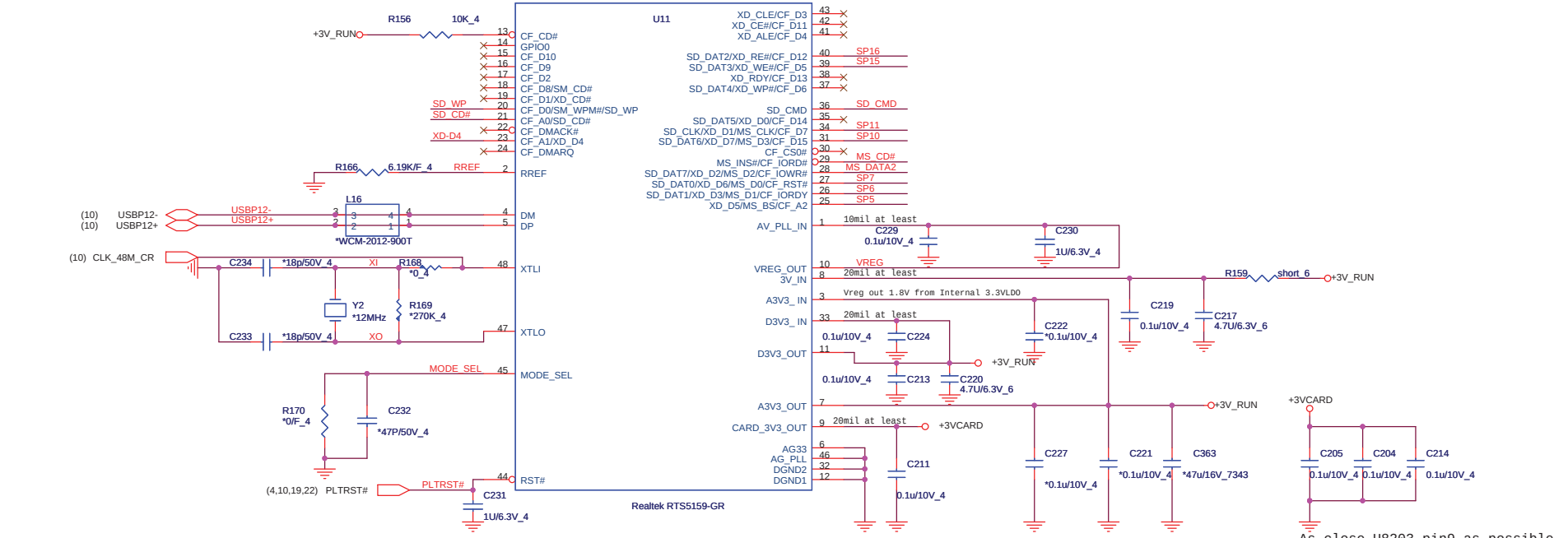
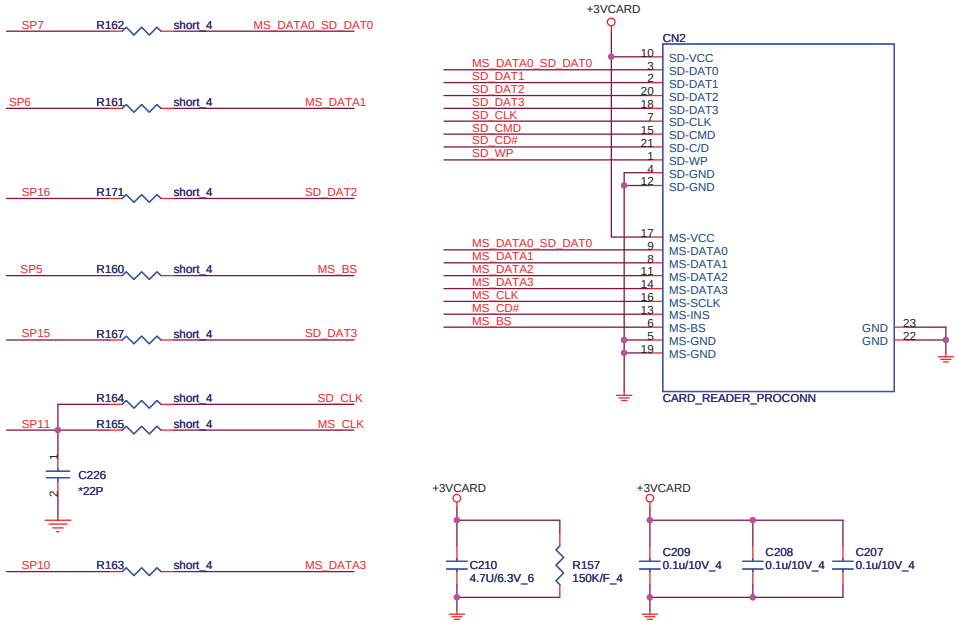
Card Reader



As close U8203 pin9 as possible

XD-D4 R158 short_4 SD_DAT1

For 5158E



Quanta Computer Inc.

PROJECT : FH1

Size	Document Number	Rev
	Card Reader RTS5159	1A

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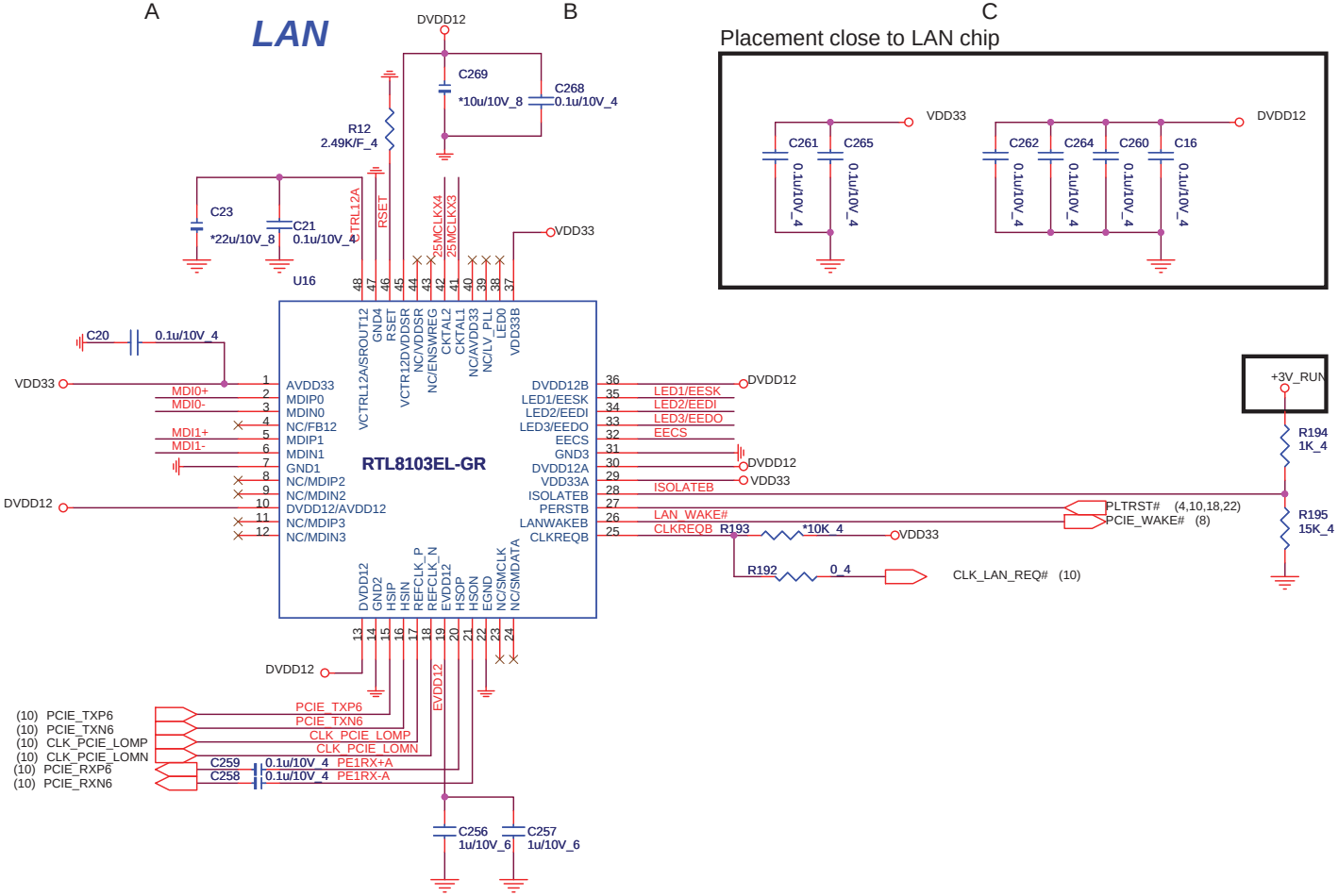
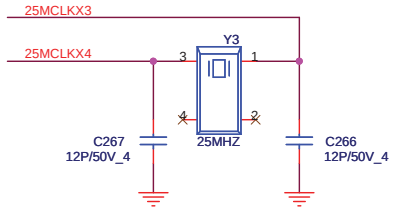
LAN



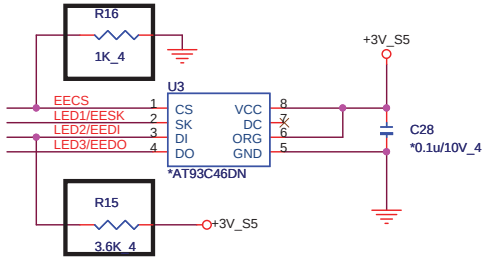
Placement close to LAN chip

X'tal 25MHz

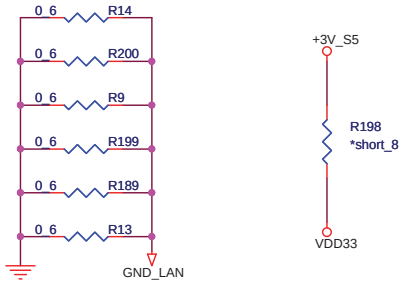


19

LAN EEPROM

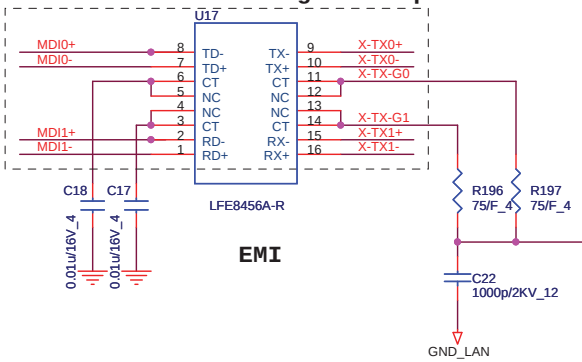


LAN Power

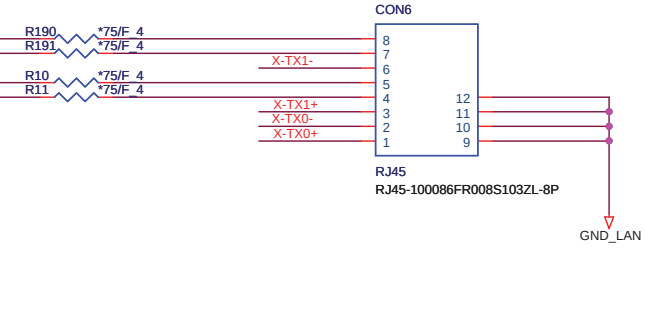


10/100 Transformer

signal swap



RJ45



Quanta Computer Inc.		
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Size	Document Number: LAN_RTL8103EL/RJ45	Rev: 1A
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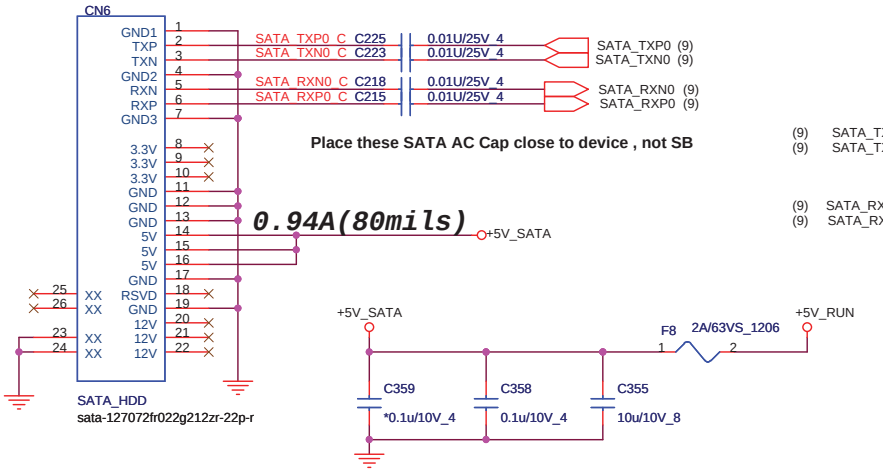
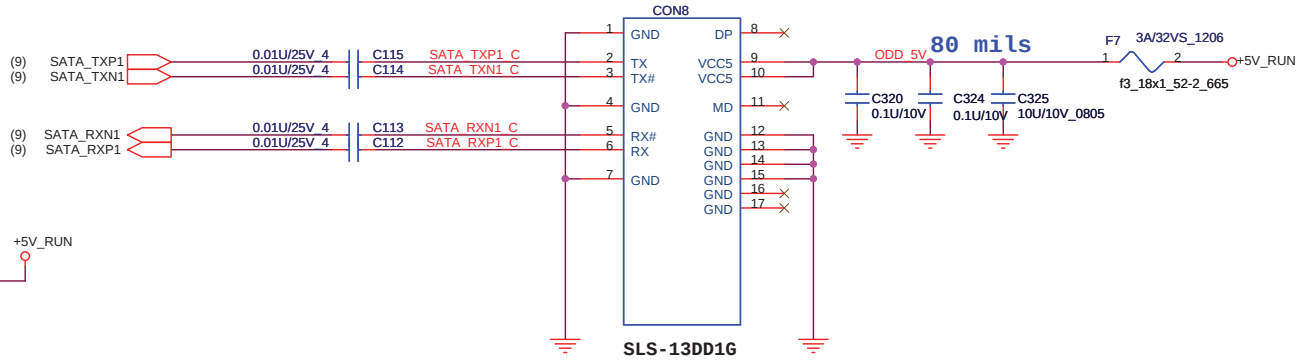
REQ by layout

2.5" SATA HDD

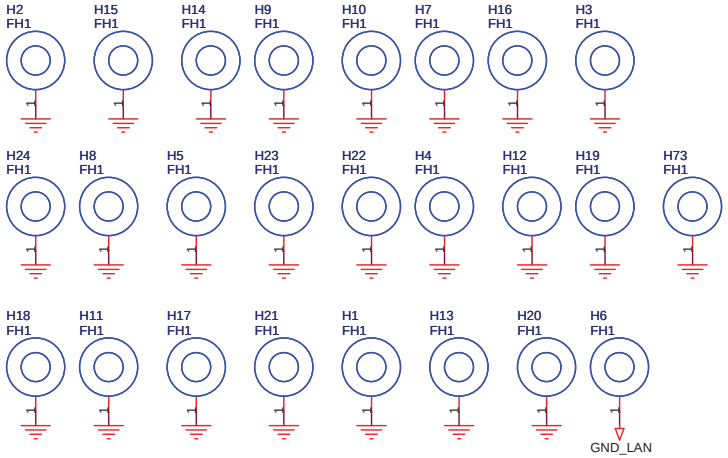


SATA ODD

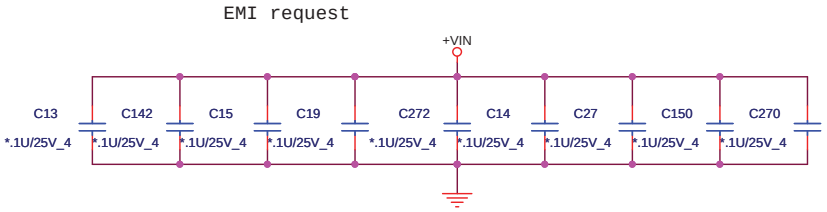
ODD CONN



Hole



Decoupling Cap



Quanta Computer Inc.

PROJECT : FH1

Size	Document Number	Rev
	HDD/ ODD/HOLE	1A

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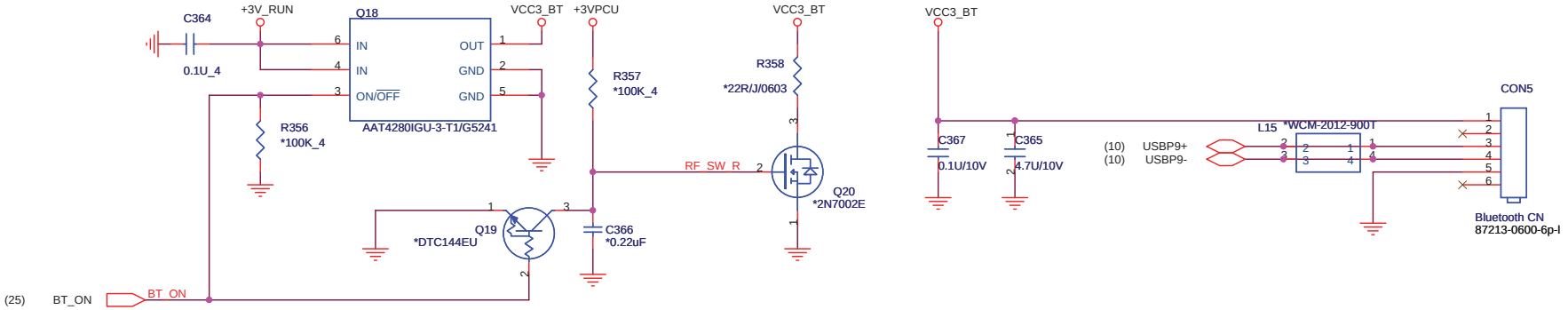
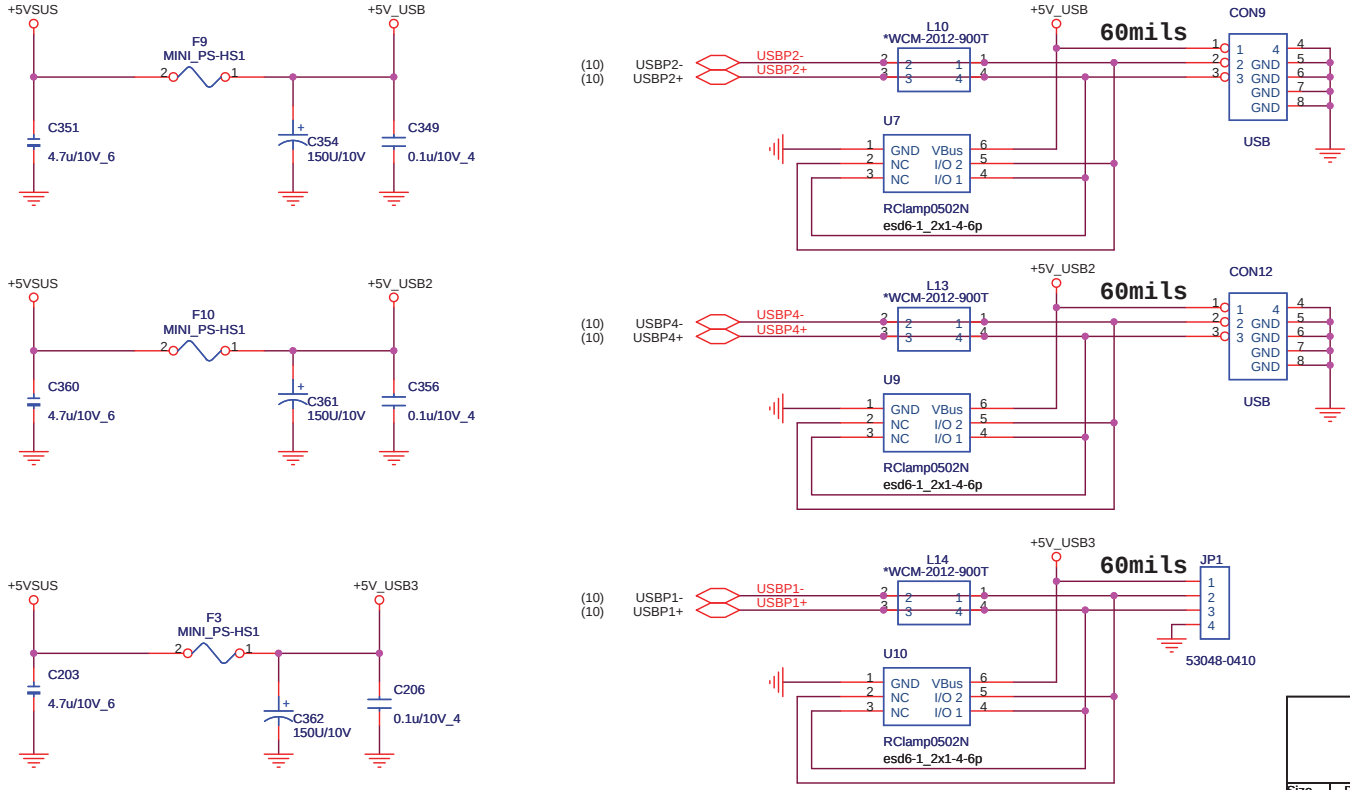
BuleTooth (BTM)



USB Connector



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: USB/BLUE TOOTH	Rev: 1A
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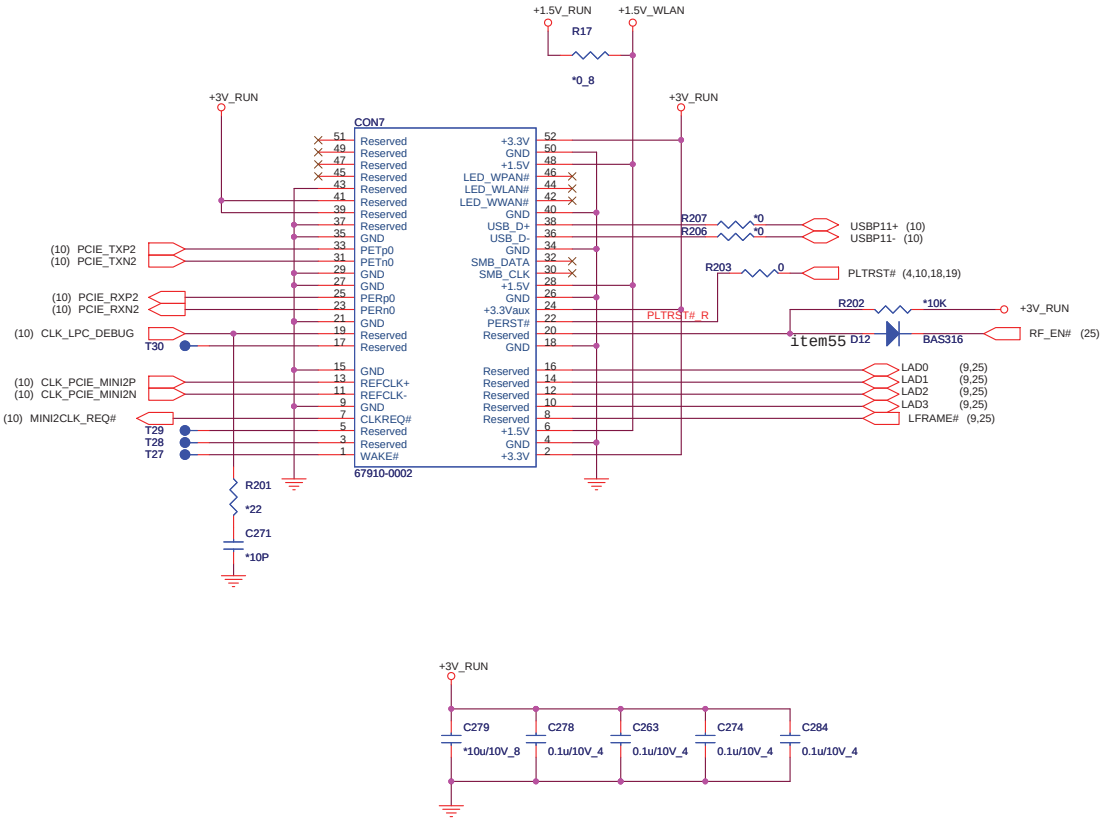
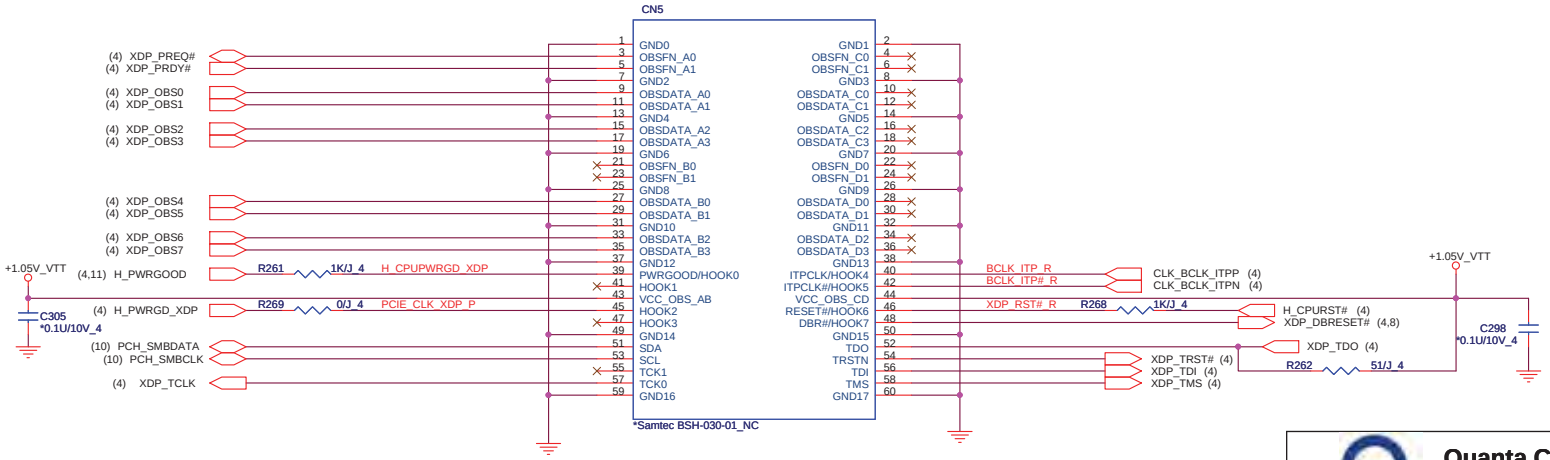
MINI CARD (WLAN)



XDP



It is for debug. requesst vendeer provide 200 pcs sample.

Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: MINI CARD(WLAN)/XDP	Rev: 1A
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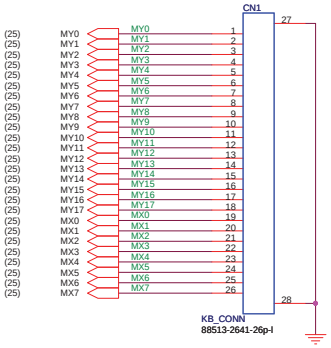
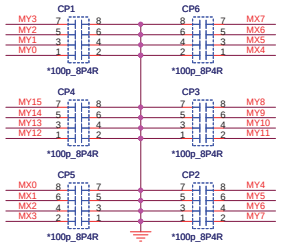
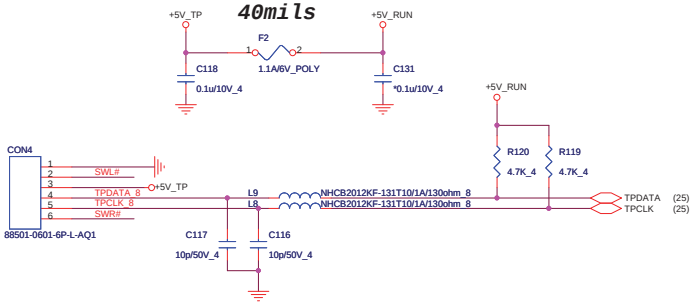
Keyboard(KBC)

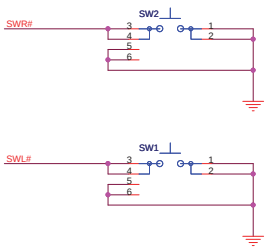


For EMI Reserve Caps for debug

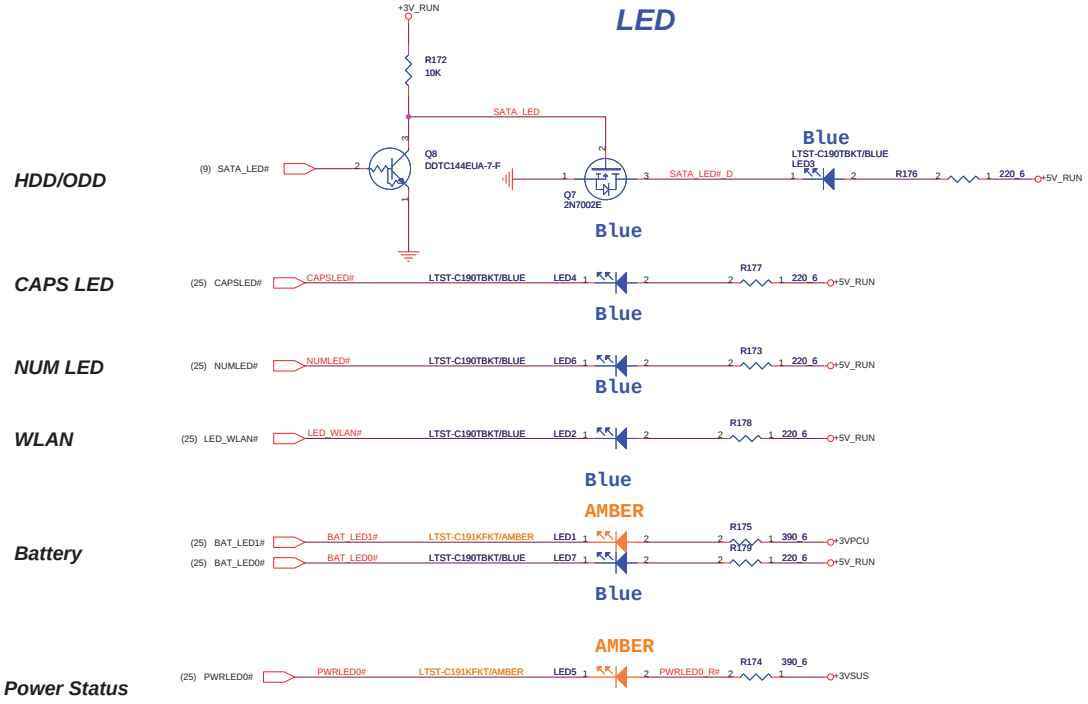


Touch Pad





LED



Quanta Computer Inc.

PROJECT : FH1

Size	Document Number	Rev
	KB/TOUCH PAD/LED	1A

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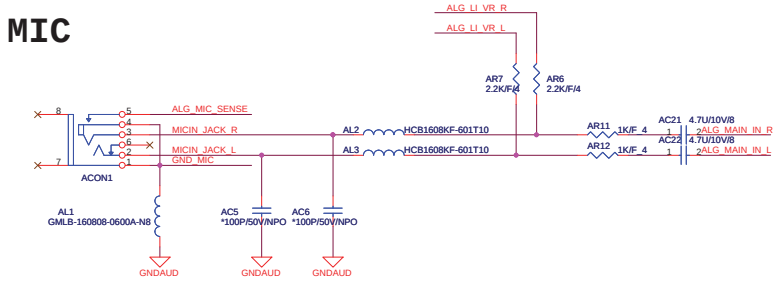
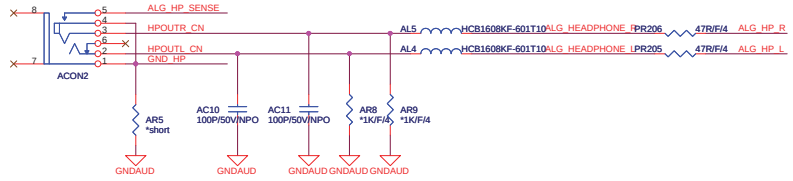
Codec ALC269

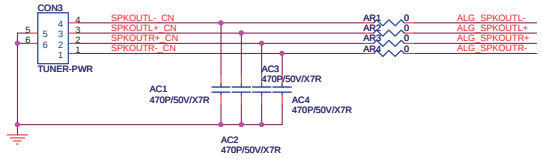
MIC



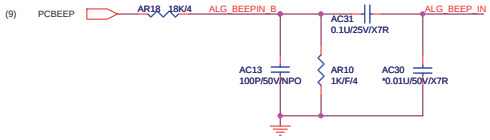
HP



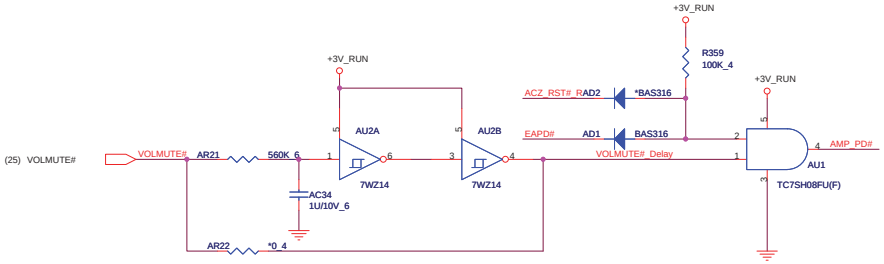
SPKR

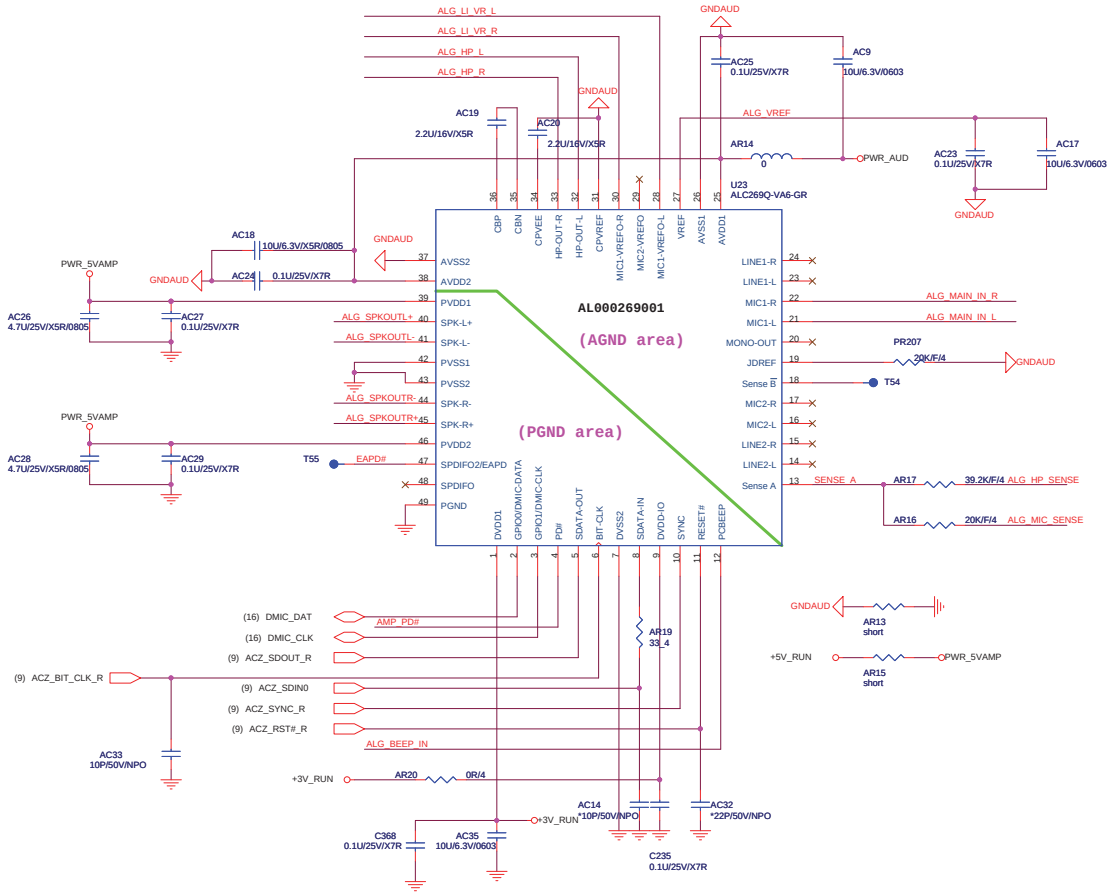


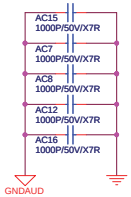
BEEP

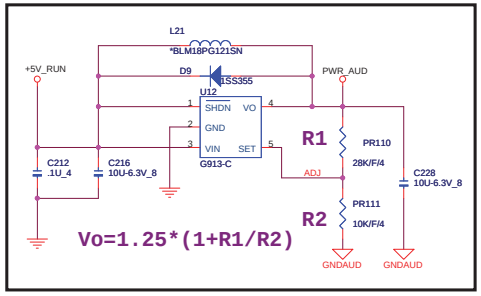


VOLMUTE









Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	CODEC (ALC269)		1A
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EC(KBC)

IT8502

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC"
minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

BIOS Write Protect

2MB

Near ROOM DOOR

MB Type	MODEL_ID0	MODEL_ID1

Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	EC_ITE8502	1A

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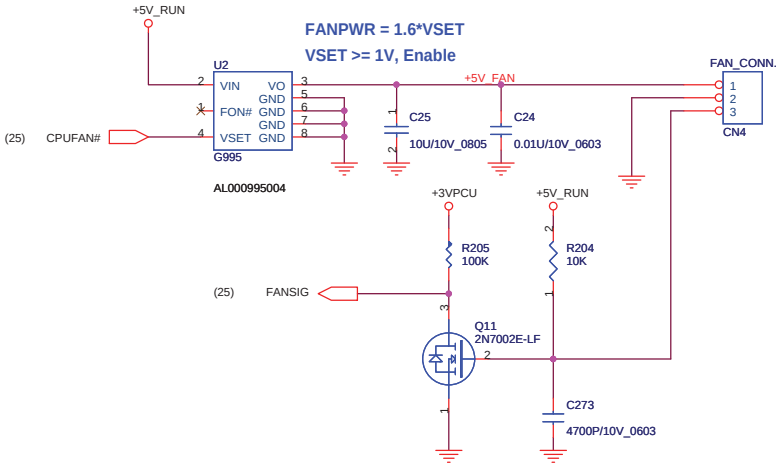
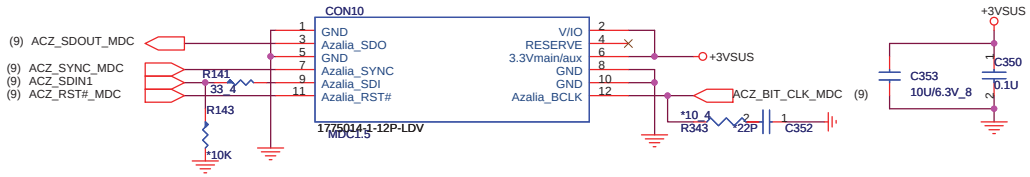
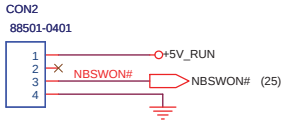
CPU FAN CTRL



MDC



SW BOARD CON



Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	FAN/SW CON/MDC	1A

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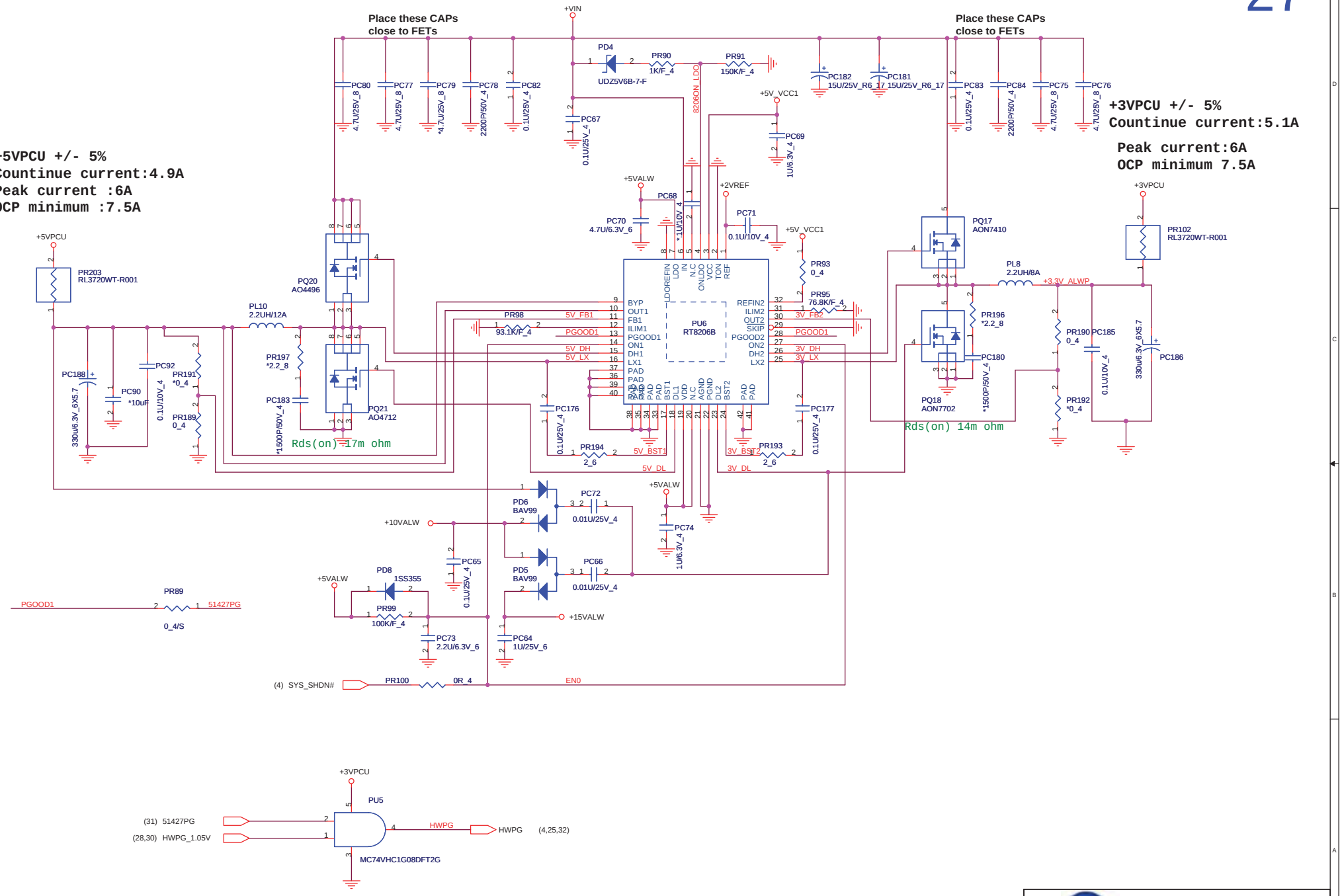
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

Place these CAPs close to FETs

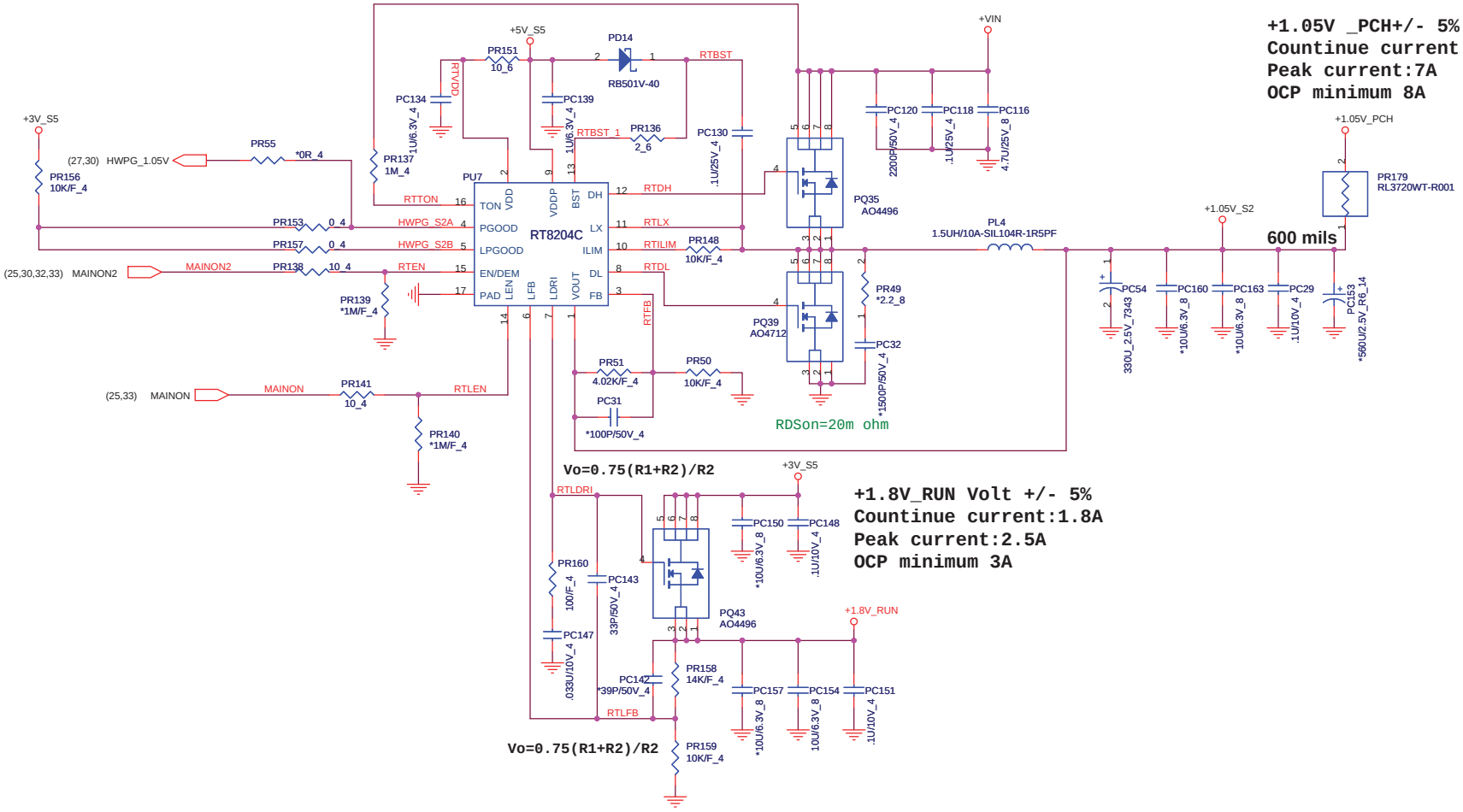
Place these CAPs close to FETs

+5VPCU +/- 5%
Countinue current:4.9A
Peak current :6A
OCP minimum :7.5A

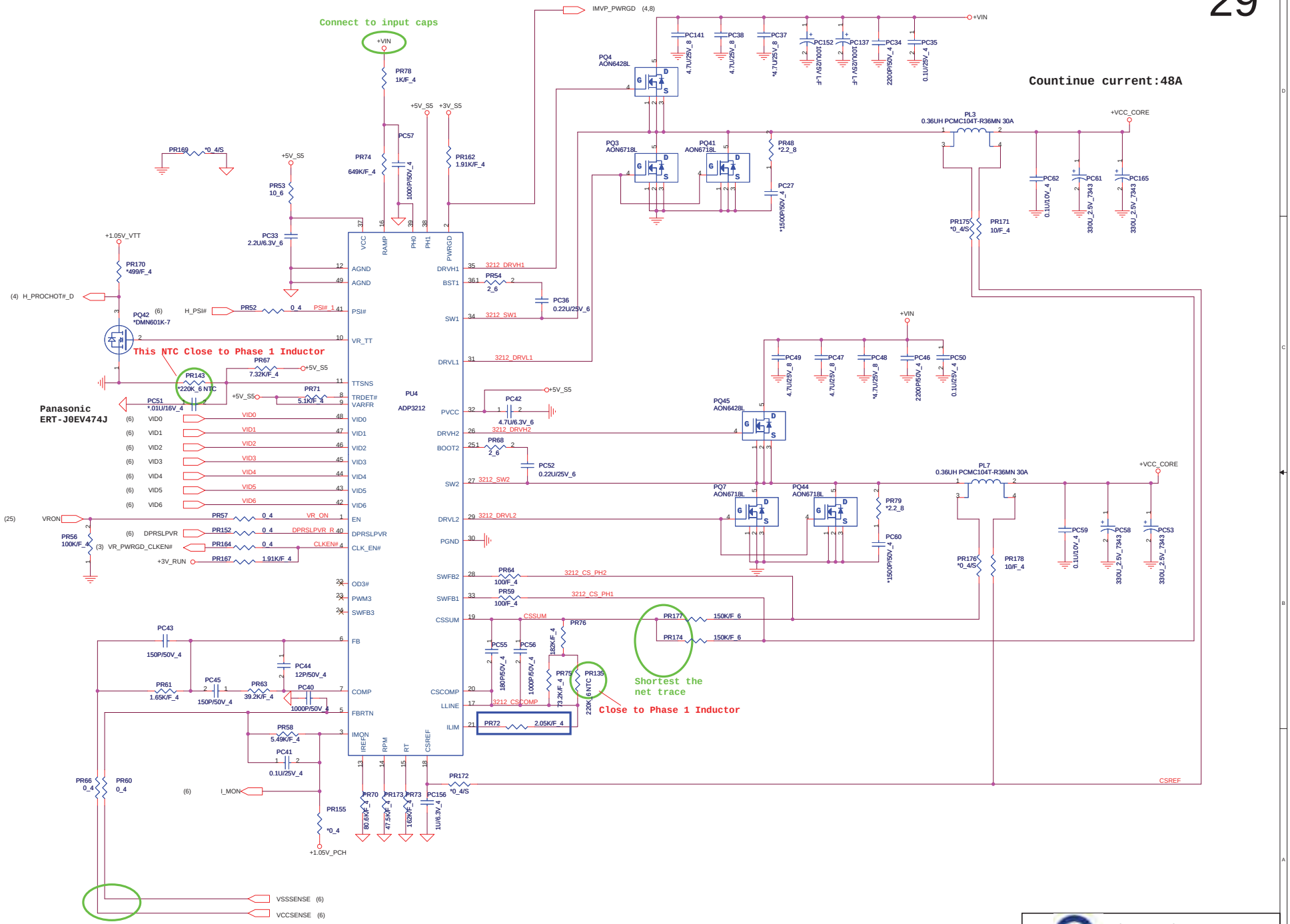
+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: +5V/+3V (RT8206B)	Rev: 1A
Date: Friday, October 09, 2009	Sheet 27 of 37	



Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	+1.05V/+1.8V (RT8204C)		1A
Date: Friday, October 09, 2009		Sheet 28 of 37	



Quanta Computer Inc.

PROJECT : FH1

Size	Document Number	Rev
	CPU Core (ADP3212)	1A

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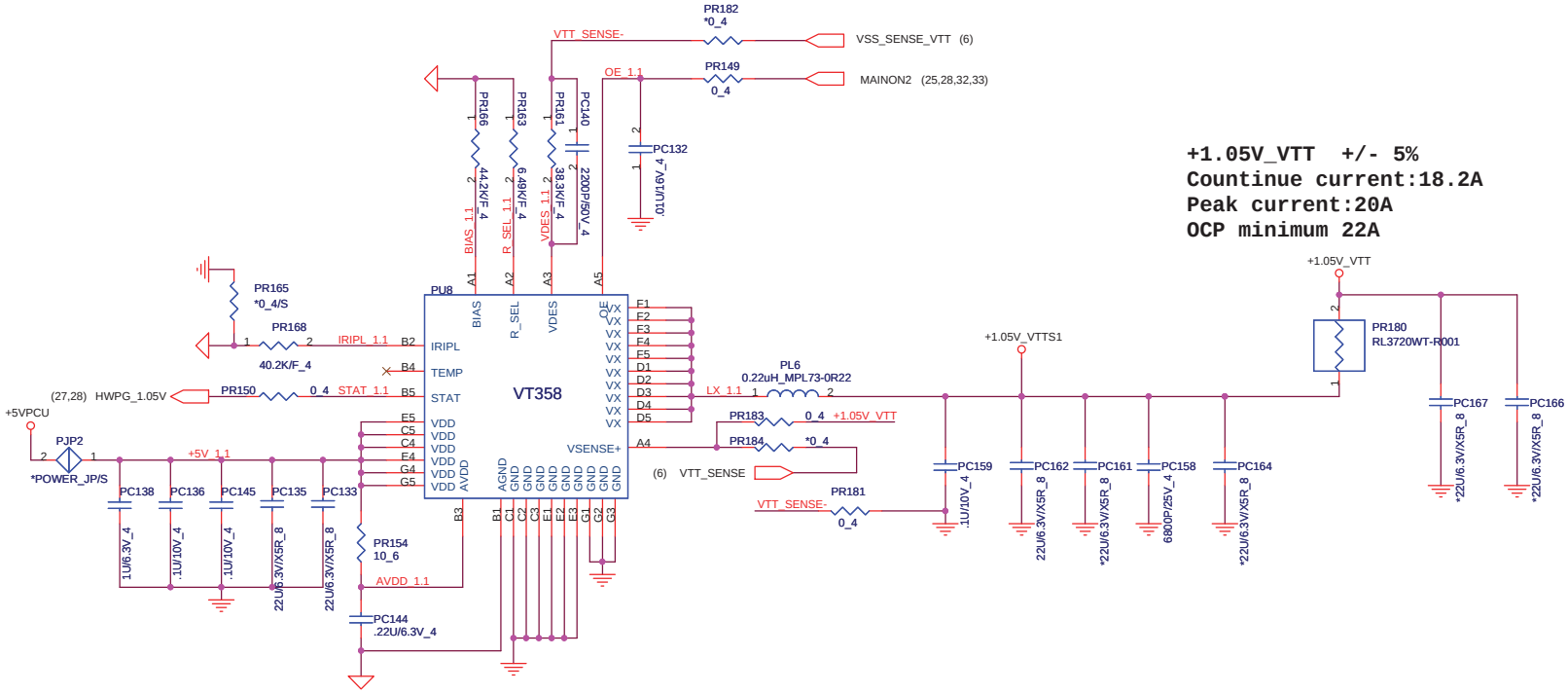
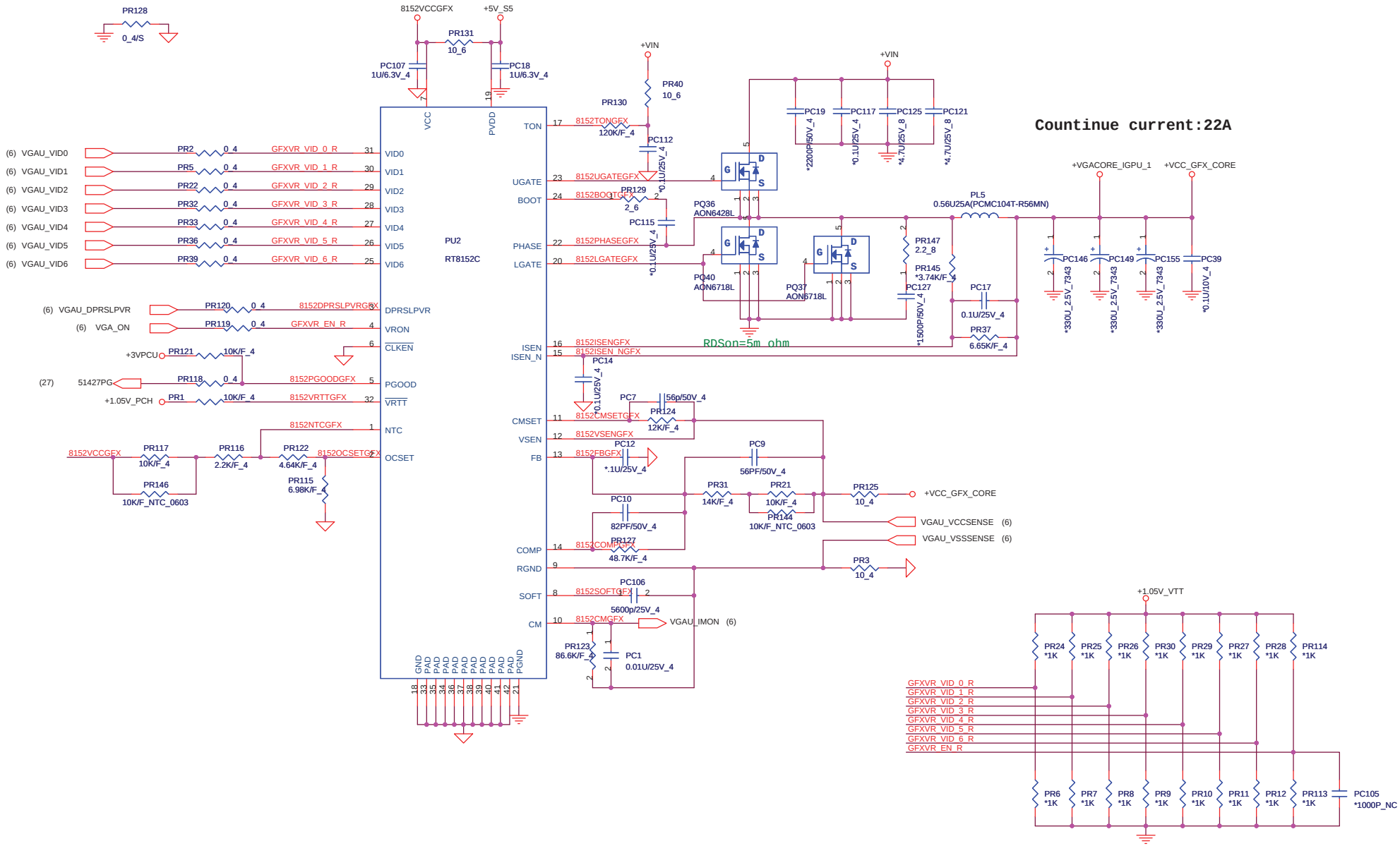


Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: +1.05V_VTT (VT358)	Rev: 1A
Date: Friday, October 09, 2009	Sheet 30 of 37	



Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	UMA GPU CORE (RT8152C)		1A
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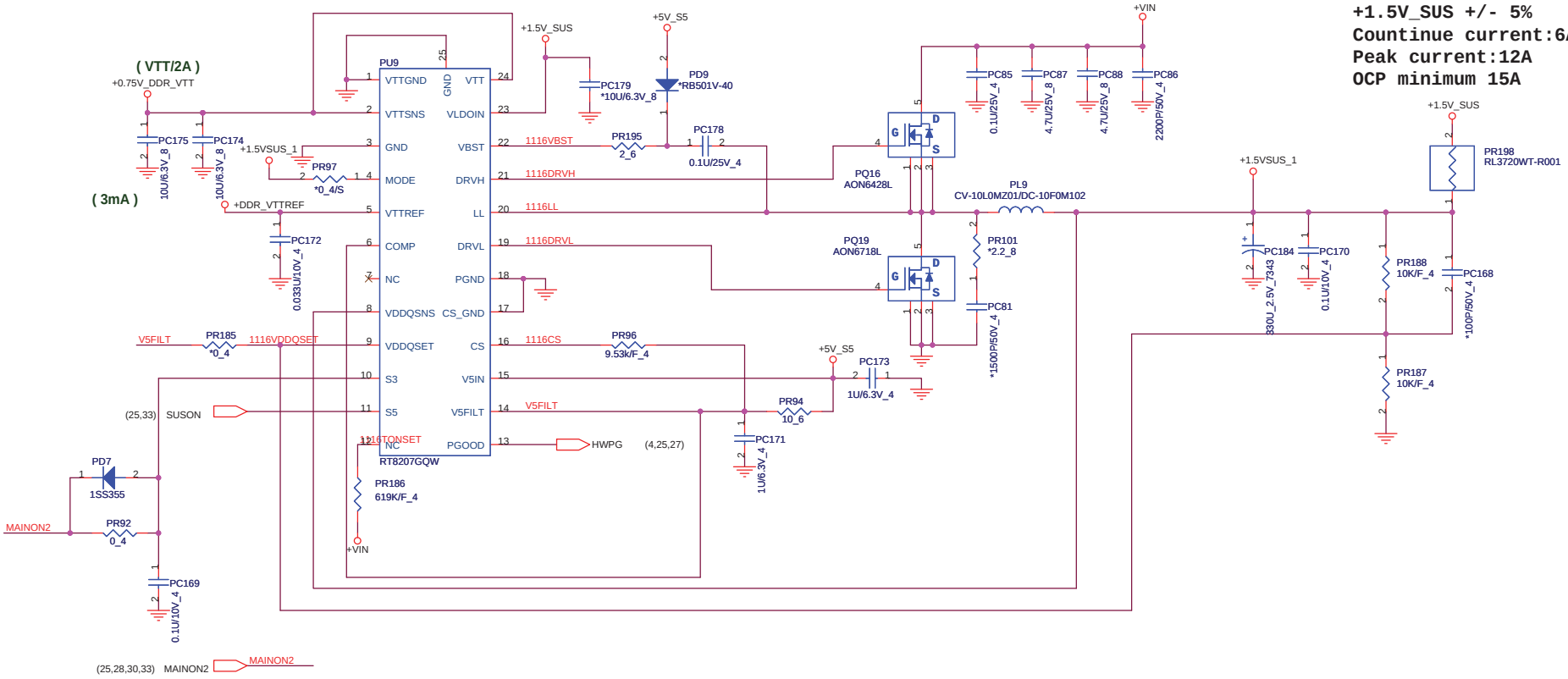
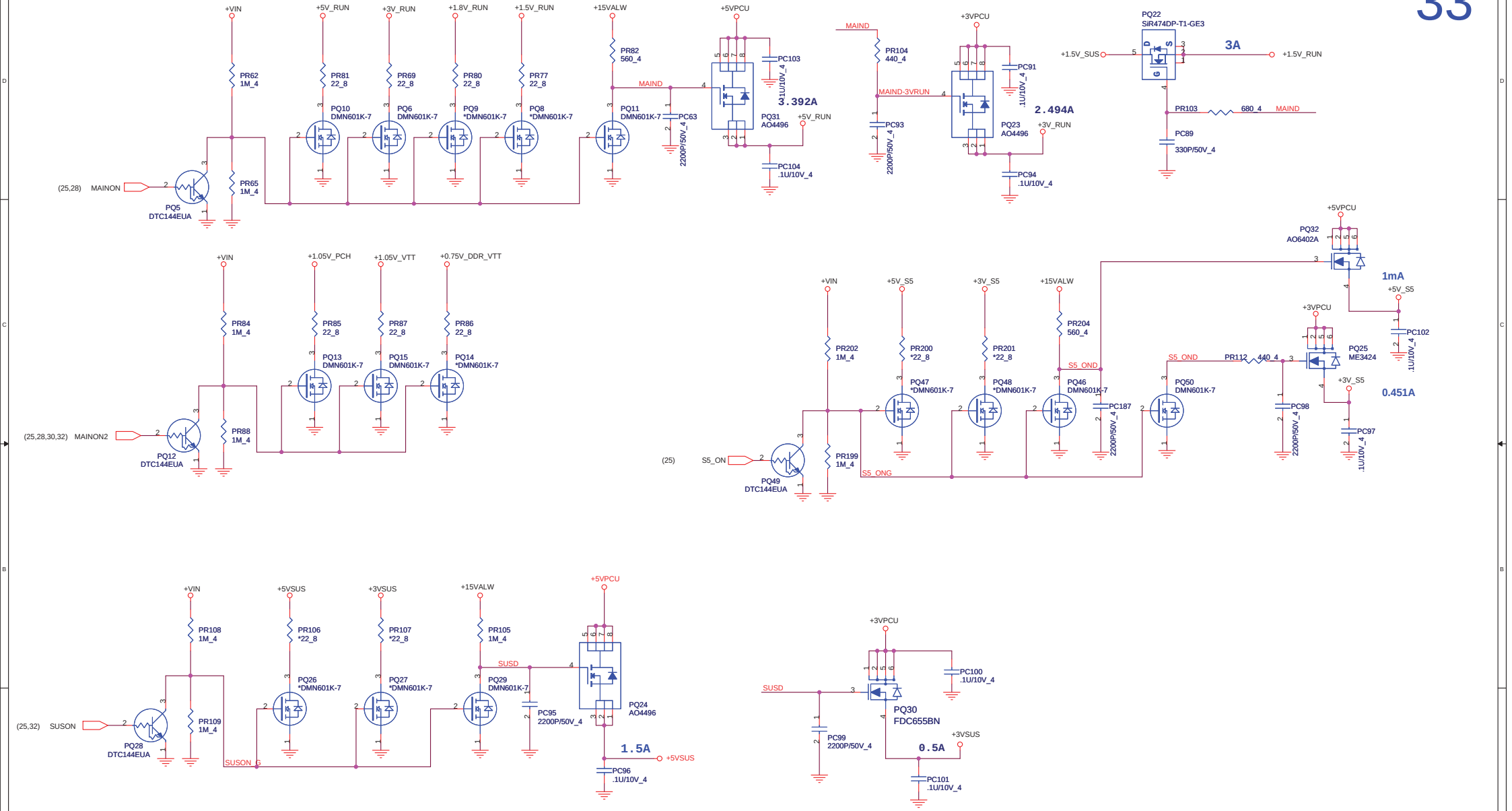
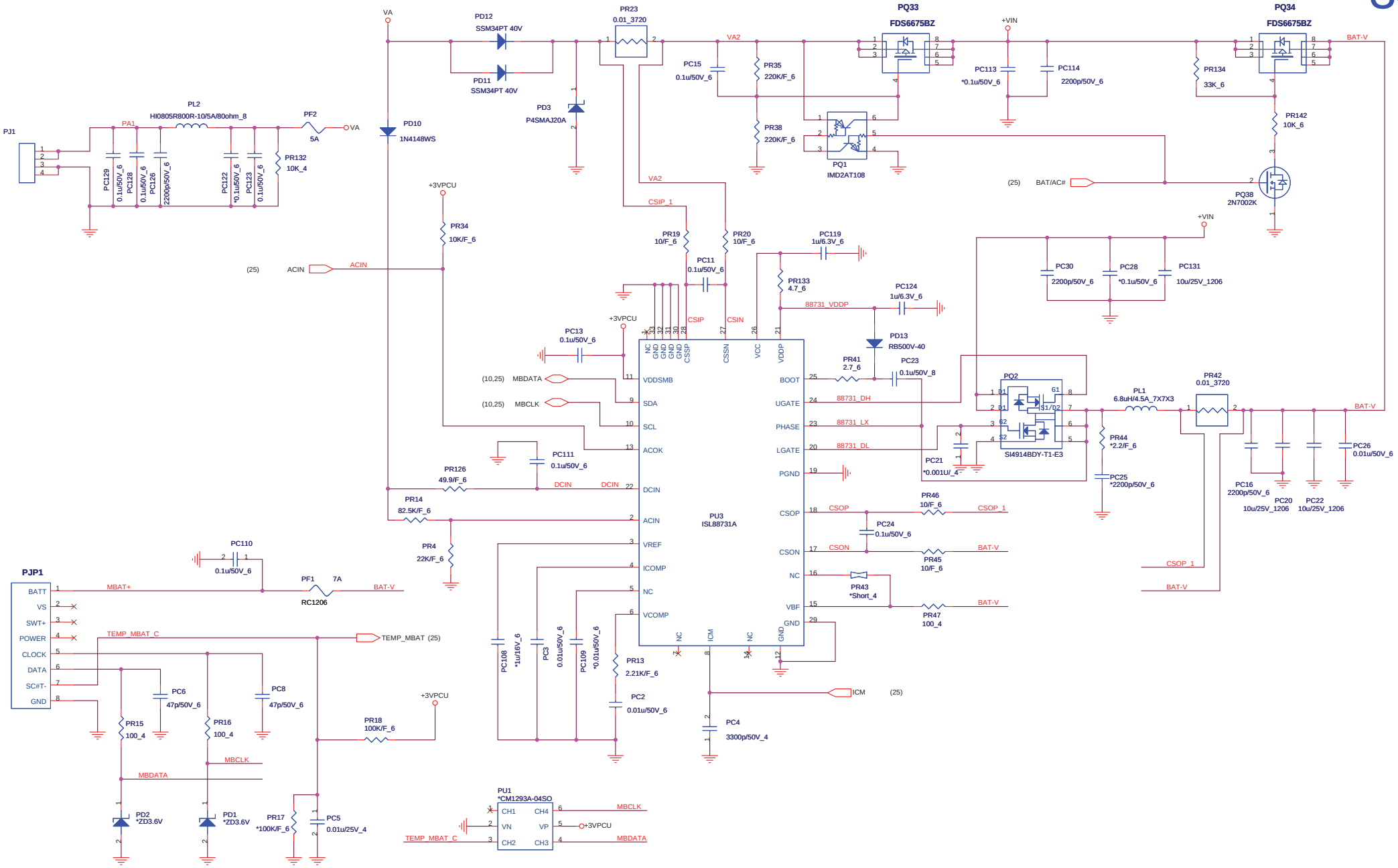
+1.5V_SUS +/- 5%
Countinue current:6A
Peak current:12A
OCP minimum 15A



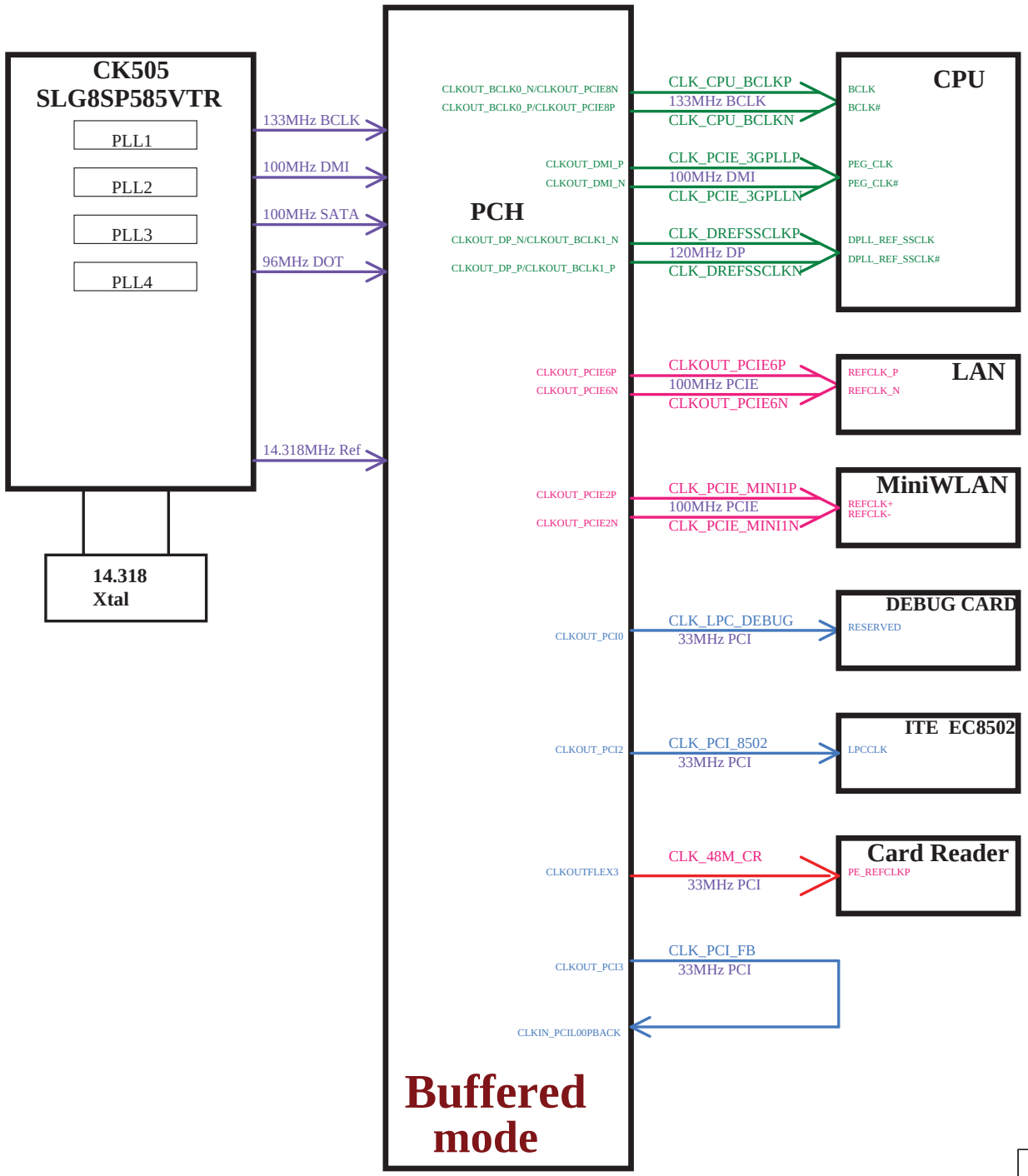
Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Friday, October 09, 2009	Sheet 32 of 37	



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DISCHARGE/3VS5/5VS5/LAN	Rev: 1A
Date: Friday, October 09, 2009	Sheet 33 of 37	



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: CHARGER (ISL88731)	Rev: 1A
Date: Friday, October 09, 2009	Sheet 34 of 37	



Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	Clock Distribution	1A

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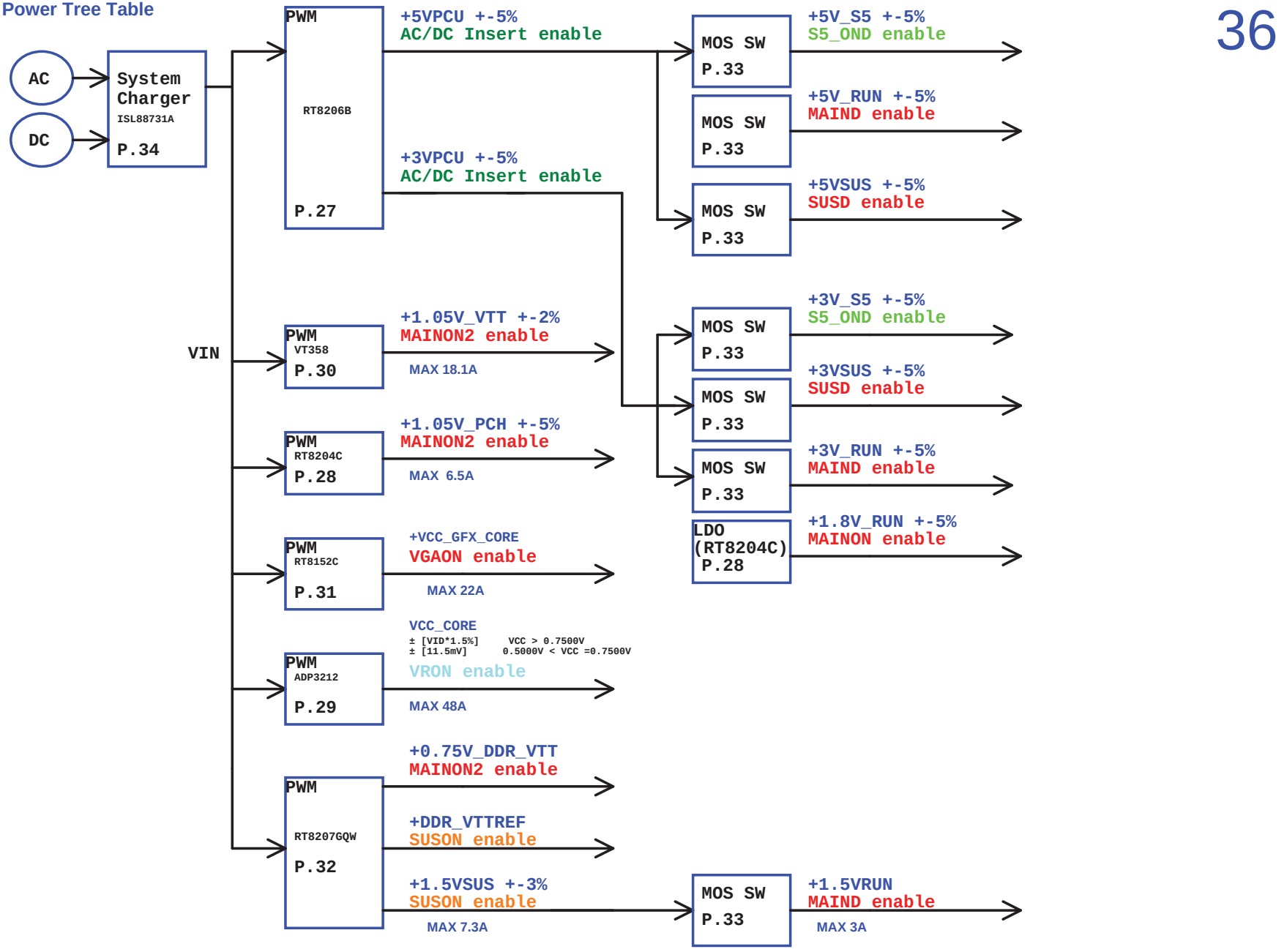
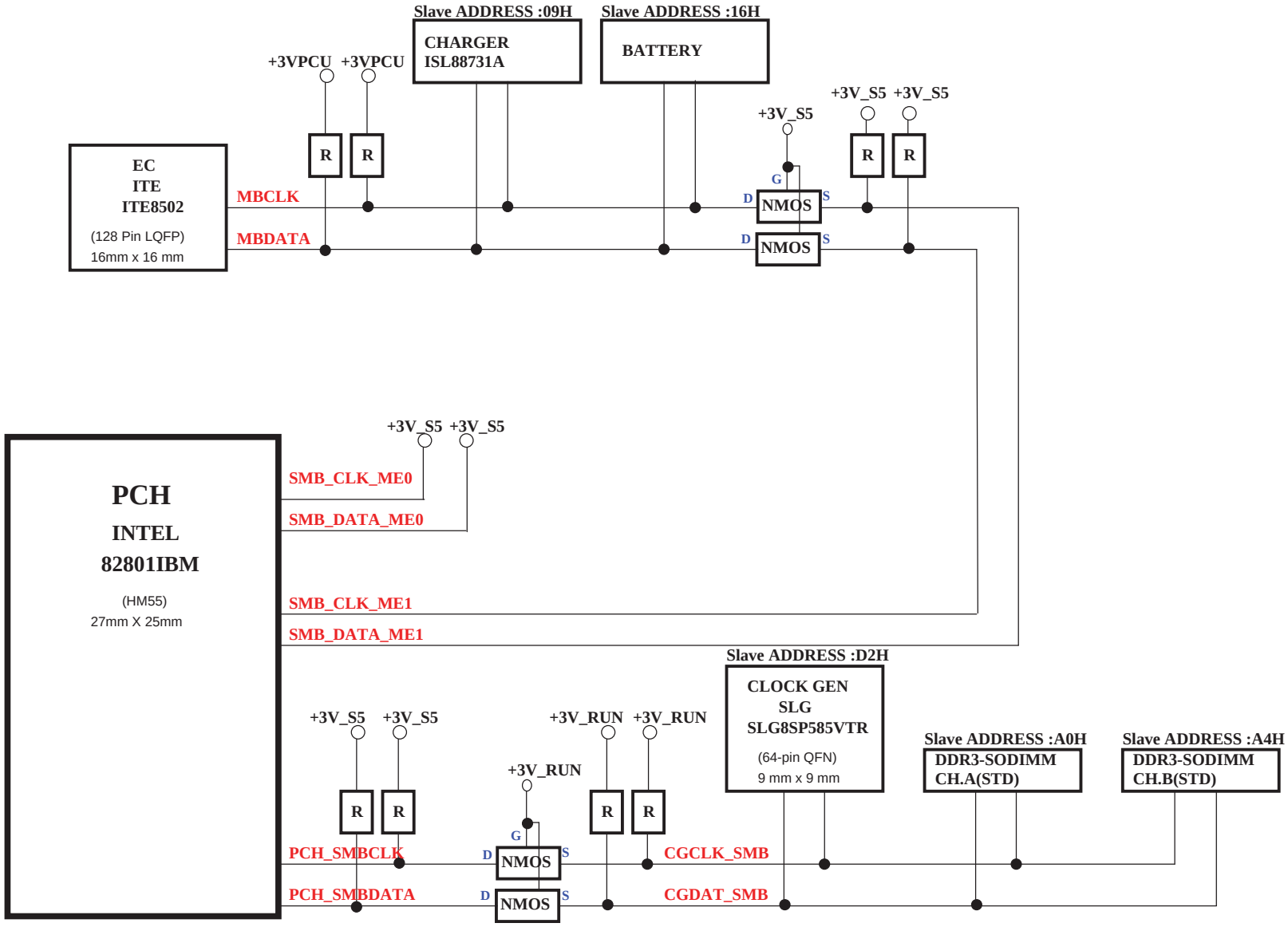
Power Tree Table



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: Power Tree	Rev 1A
Date: Friday, October 09, 2009	Sheet 36 of 37	



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: SM BUS	Rev: 1A
Date: Friday, October 09, 2009	Sheet 37 of 37	