ARES/ARTEMIS Block Diagram

SI - PHASE

PCB STACK UP

- LAYER 1 : TOP
- LAYER 2 : SGND1
- LAYER 3 : IN1
- LAYER 4 : IN2
- LAYER 5 : VCC
- LAYER 6 : IN3
- LAYER 7 : SGND2
- LAYER 8 : BOT

RUN POWER SW PG 36,37

AC/BATT CONNECTOR PG 34

BATT CHARGER PG 34

CPU VR PG 38

DC/DC +3VSUS +5VSUS PG 33

Turion64 Sempron

25W/35W
AMD Socket S1 638P
PG 2,3,4

DDRII-SODIMM1 PG 5 — *DDRII 667mhz*

DDRII-SODIMM2 PG 5 — *DDRII 667mhz*

HT Link

nVIDIA MCP67 MCP67D

Integraded VGA Function
836PIN
PG 5,6,7,8,9,10,11

PCI-E X 1

Mini PCI-E Card
PCI Express Mini Card
(Wireless LAN/WAN)
PG 27

Express Card
(NEW CARD)
PG 28

SIM CARD PG 27

PCI-Express 16X

NVDIA NB8M-64bit
Graphics
PG 12,13,14,15,16,17

Option for 17" only
HDMI CON PG 18

TV_OUT

CRT_OUT

CRT/S-VIDEO PG 19

LVDS(2 Channel)

Panel Connector
15" / 17" PG 18

CLOCK INTERFACE

SATA1

Option for 17" only
SATA - HDD PG 26

SATA0

SATA - HDD PG 26

PATA (66/100/133)

PATA- CD-ROM PG 26

USB2.0

Bluetooth PG 28

FingrPrint PG 28

USB2.0 I/O Ports X3 PG 26

Camera 1.3MP PG 23

Mini PCI-E Card x1
Express Card x1
Cable Docking x1

PCI BUS / 33MHz

LAN

HD AUDIO

Cable Docking PG 31

- TV_OUT
- VGA
- RJ-45
- CIR/Pwr btn
- SPDIF Out
- Stereo MIC
- Headphone Jack
- USB Port
- VOL Cntr

LPC

TPM SLB9635 PG 28

Keyboard Touch Pad PG 29

CIR PG 23

Capacitive Sense SW PG 29

ENE KBC
KB3920 Bx
KB3926
PG 30,31

X-Bus

FAN PG 31

SPI ROM PG 30

Conexant
Venice AMOM
CX20549-12
PG 23

Two-element microphone PG 23

Audio Jacks
-Phone
-SPDIF
-MIC
PG 23

AUDIO Amplifier TPA0312 PG 25

Jack to Speaker PG 25

MDC DAA CX20548-S PG 24

MODEM RJ 11 PG 20

REALTEK
RTL8201CL (10/100)
RTL8211B (10/100/Gigabit)
PG 20

LAN RJ45 PG 20

RICOH
RICOH R5C832
R5C833
PG 21

IEEE1394 CONN PG 21

Memory Card Reader PG 22

PCI ROUTING TABLE	IDSEL	INTERUPT	DEVICE
REQ0# / GNT0#	AD21	INTA#,INTB#	RICOH832

VAULE DEFINE

A=0603,B=0805,C=1206,F=1%,
OTHER IS 0402
V=Y5V,U=Y5U,R=X5R,S=X6S,
X=X7R,G=COG,O=NPO

EXAMPLE

10R=10ohm(0402)
10A=10ohm(0603)
10B=10ohm(0805)
10C=10ohm(1206)
10/F=10ohm(0402 and 1%)

EXAMPLE

0.1U/16V/R=0.1U/16V/X5R(0402)
0.47UA/10V/X=0.47U/10V/X7R(0603)
10UB/10V/U=10U/10V/Y5U(0805)

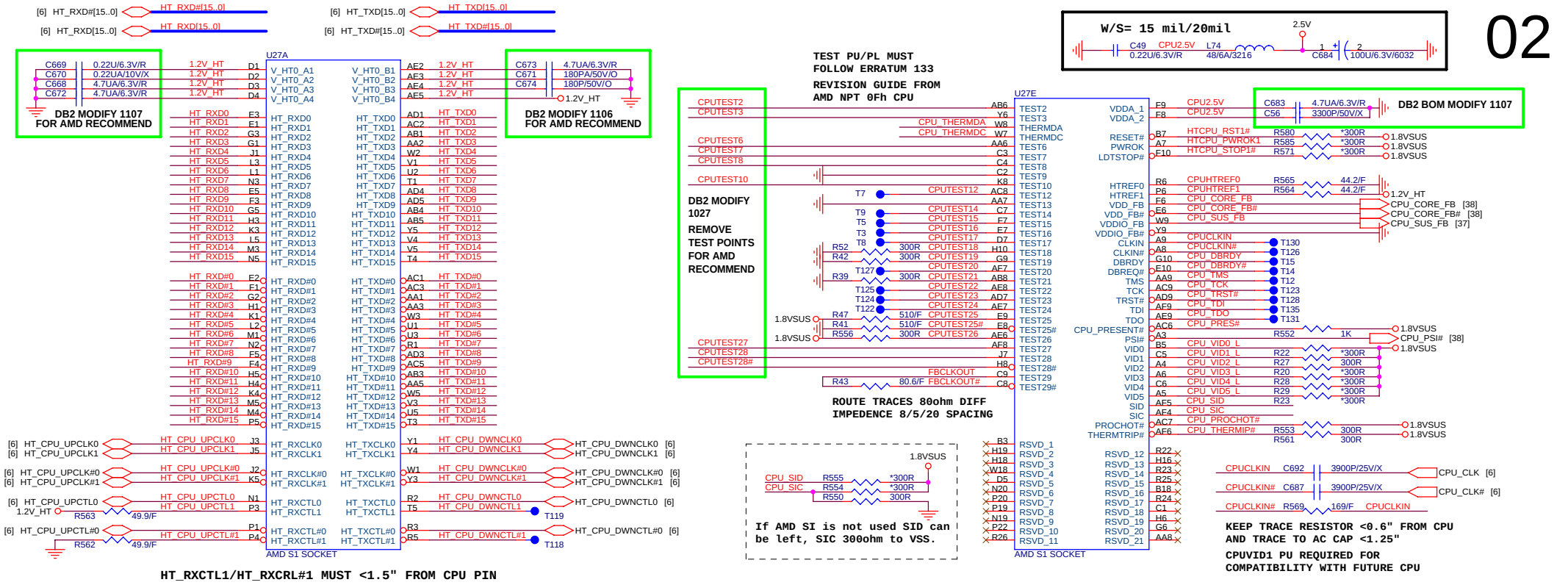
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

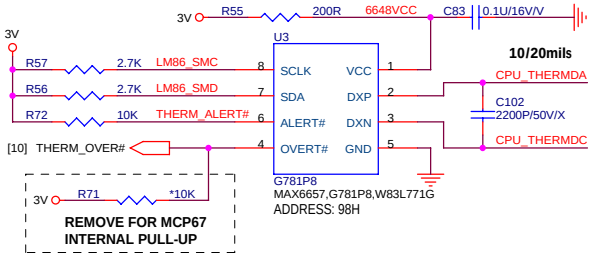
Size	Document Number	Rev
Custom	BLOCK DIAGRAM	C2A

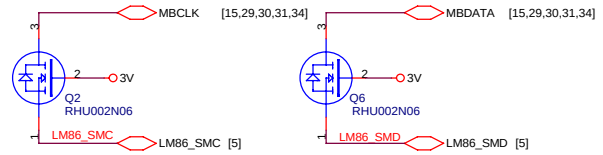
Date: Wednesday, December 20, 2006 Sheet 1 of 40

02



CPU THERMAL SENSOR & CONTROL

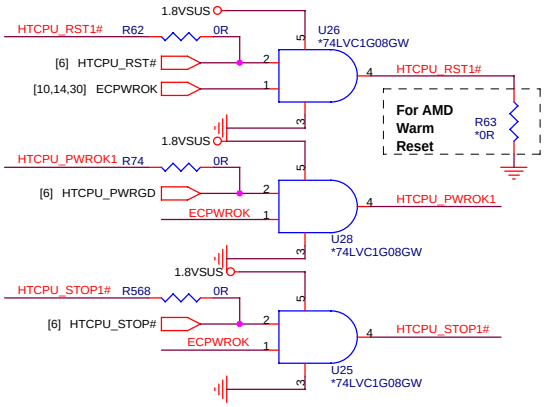




MBCLK/MBDATA NEED PU TO 3VPCU

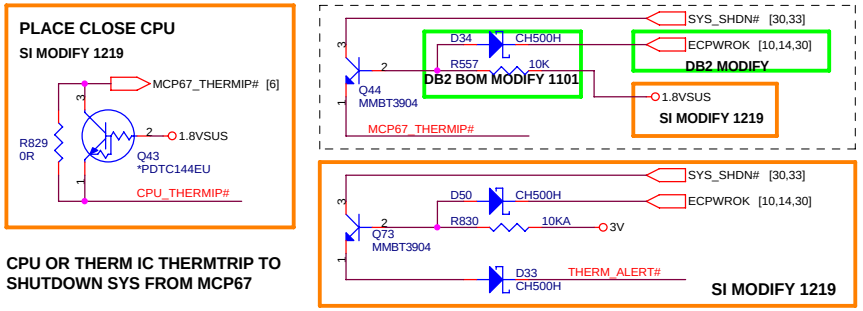
HT LINK CONTROL LEVEL SHIFTER

MUST KEEP LOW DURING S3-S5 TO MEET HT IO LINK SPEC



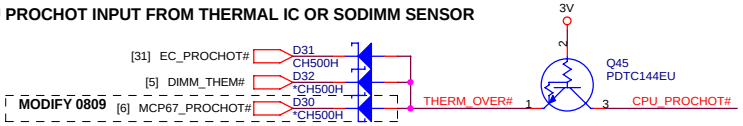
FOLLOW AMD AND NVIDIA RECOMMEND 0904

OVER TEMP CONTROL



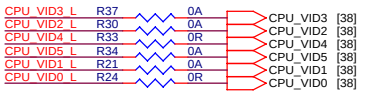
CPU OR THERM IC THERMTRIP TO
SHUTDOWN SYS FROM MCP67

CPU PROCHOT INPUT FROM THERMAL IC OR SODIMM SENSOR



1.2V_HT [6,10,11]
1.8VSUS [3,4,5,6,32,36,37]
2.5V [13,32,36]
3V [5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

NEED TO CONFIRM NVIDIA FOR
THE USAGE CONNECTION TO SB

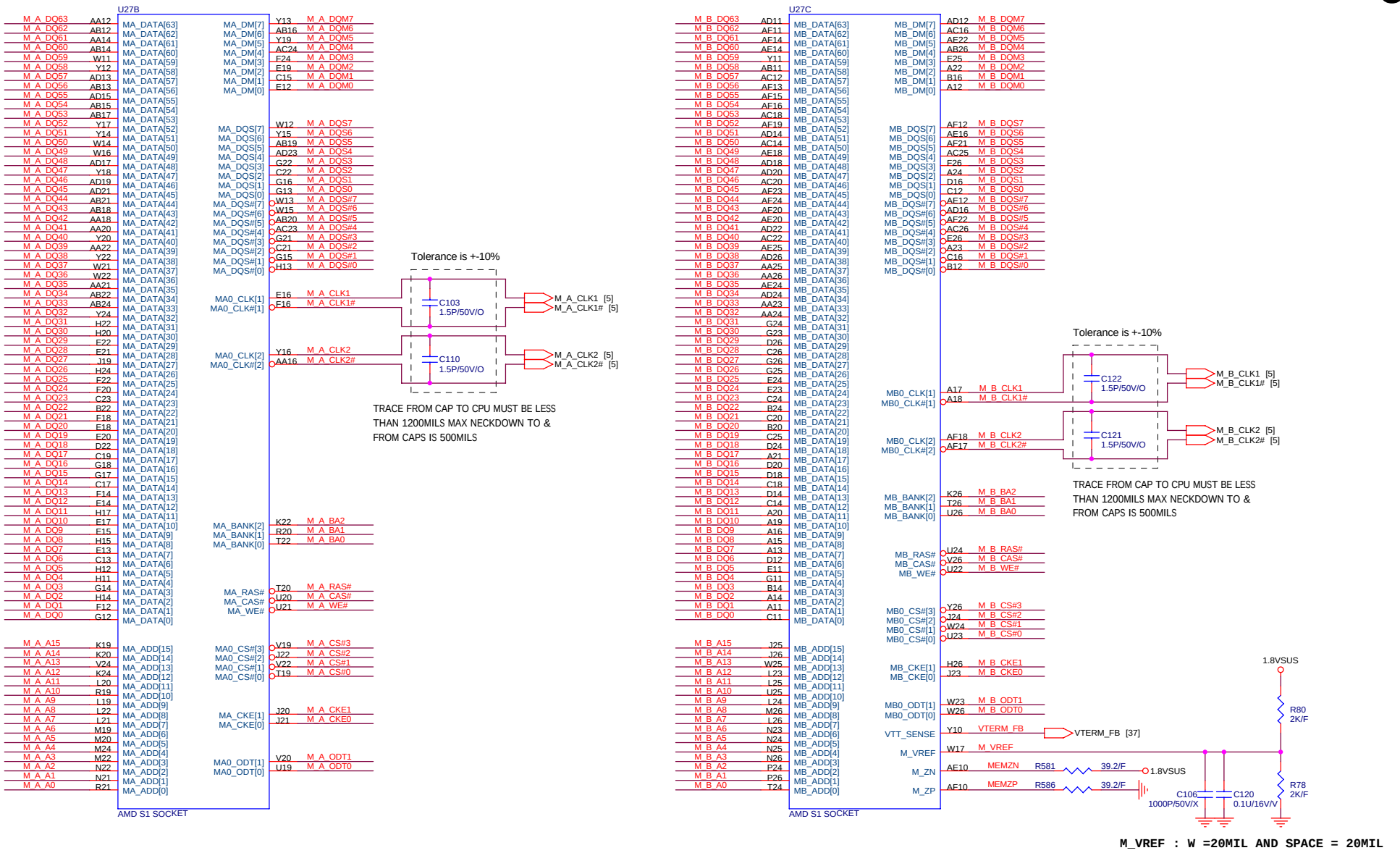


NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (HT_I/F,CTL)	C2A

Date: Wednesday, December 20, 2006 Sheet 2 of 40


U27B
M_A_DQ63 AA12
M_A_DQ62 AB12
M_A_DQ61 AA14
M_A_DQ60 AB14
M_A_DQ59 W11
M_A_DQ58 Y12
M_A_DQ57 AD13
M_A_DQ56 AB13
M_A_DQ55 AD15
M_A_DQ54 AB15
M_A_DQ53 AB17
M_A_DQ52 Y17
M_A_DQ51 Y14
M_A_DQ50 W14
M_A_DQ49 W16
M_A_DQ48 AD17
M_A_DQ47 Y18
M_A_DQ46 AD19
M_A_DQ45 AD21
M_A_DQ44 AB21
M_A_DQ43 AB18
M_A_DQ42 AA18
M_A_DQ41 AA20
M_A_DQ40 Y20
M_A_DQ39 AA22
M_A_DQ38 Y22
M_A_DQ37 W21
M_A_DQ36 W22
M_A_DQ35 AA21
M_A_DQ34 AB22
M_A_DQ33 AB24
M_A_DQ32 Y24
M_A_DQ31 H22
M_A_DQ30 H20
M_A_DQ29 E22
M_A_DQ28 E21
M_A_DQ27 J19
M_A_DQ26 H24
M_A_DQ25 F22
M_A_DQ24 F20
M_A_DQ23 C23
M_A_DQ22 B22
M_A_DQ21 F18
M_A_DQ20 E18
M_A_DQ19 E20
M_A_DQ18 D22
M_A_DQ17 C19
M_A_DQ16 G18
M_A_DQ15 G17
M_A_DQ14 C17
M_A_DQ13 F14
M_A_DQ12 E14
M_A_DQ11 H17
M_A_DQ10 E17
M_A_DQ9 E15
M_A_DQ8 H15
M_A_DQ7 E13
M_A_DQ6 C13
M_A_DQ5 H12
M_A_DQ4 H11
M_A_DQ3 G14
M_A_DQ2 H14
M_A_DQ1 F12
M_A_DQ0 G12
MA_DATA[63]
MA_DATA[62]
MA_DATA[61]
MA_DATA[60]
MA_DATA[59]
MA_DATA[58]
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MA_DATA[7]
MA_DATA[6]
MA_DATA[5]
MA_DATA[4]
MA_DATA[3]
MA_DATA[2]
MA_DATA[1]
MA_DATA[0]
MA_DM[7] Y13 M_A_DQM7
MA_DM[6] AB16 M_A_DQM6
MA_DM[5] Y19 M_A_DQM5
MA_DM[4] AC24 M_A_DQM4
MA_DM[3] F24 M_A_DQM3
MA_DM[2] E19 M_A_DQM2
MA_DM[1] C15 M_A_DQM1
MA_DM[0] E12 M_A_DQM0
MA_DQS[7] W12 M_A_DQS7
MA_DQS[6] Y15 M_A_DQS6
MA_DQS[5] AB19 M_A_DQS5
MA_DQS[4] AD23 M_A_DQS4
MA_DQS[3] G22 M_A_DQS3
MA_DQS[2] C22 M_A_DQS2
MA_DQS[1] G16 M_A_DQS1
MA_DQS[0] G13 M_A_DQS0
MA_DQS#[7] W13 M_A_DQS#7
MA_DQS#[6] W15 M_A_DQS#6
MA_DQS#[5] AB20 M_A_DQS#5
MA_DQS#[4] AC23 M_A_DQS#4
MA_DQS#[3] G21 M_A_DQS#3
MA_DQS#[2] C21 M_A_DQS#2
MA_DQS#[1] G15 M_A_DQS#1
MA_DQS#[0] H13 M_A_DQS#0
MA0_CLK[1] E16 M_A_CLK1
MA0_CLK#[1] F16 M_A_CLK1#
MA0_CLK[2] Y16 M_A_CLK2
MA0_CLK#[2] AA16 M_A_CLK2#
Tolerance is +-10%
C103 1.5P/50V/O
C110 1.5P/50V/O
M_A_CLK1 [5]
M_A_CLK1# [5]
M_A_CLK2 [5]
M_A_CLK2# [5]
TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS
MA_BANK[2] K22 M_A_BA2
MA_BANK[1] R20 M_A_BA1
MA_BANK[0] T22 M_A_BA0
MA_RAS# T20 M_A_RAS#
MA_CAS# U20 M_A_CAS#
MA_WE# U21 M_A_WE#
M_A_A15 K19
M_A_A14 K20
M_A_A13 V24
M_A_A12 K24
M_A_A11 L20
M_A_A10 R19
M_A_A9 L19
M_A_A8 L22
M_A_A7 L21
M_A_A6 M19
M_A_A5 M20
M_A_A4 M24
M_A_A3 M22
M_A_A2 N22
M_A_A1 N21
M_A_A0 R21
MA_ADD[15]
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MA_ADD[2]
MA_ADD[1]
MA_ADD[0]
MA0_CS#[3] V19 M_A_CS#3
MA0_CS#[2] J22 M_A_CS#2
MA0_CS#[1] V22 M_A_CS#1
MA0_CS#[0] T19 M_A_CS#0
MA_CKE[1] J20 M_A_CKE1
MA_CKE[0] J21 M_A_CKE0
MA0_ODT[1] V20 M_A_ODT1
MA0_ODT[0] U19 M_A_ODT0
AMD S1 SOCKET
U27C
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M_B_DQ62 AE11
M_B_DQ61 AE14
M_B_DQ60 AE14
M_B_DQ59 Y11
M_B_DQ58 AB11
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MB_DM[7] AD12 M_B_DQM7
MB_DM[6] AC16 M_B_DQM6
MB_DM[5] AF22 M_B_DQM5
MB_DM[4] AB26 M_B_DQM4
MB_DM[3] E25 M_B_DQM3
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MB_DM[0] A12 M_B_DQM0
MB_DQS[7] AF12 M_B_DQS7
MB_DQS[6] AE16 M_B_DQS6
MB_DQS[5] AF21 M_B_DQS5
MB_DQS[4] AC25 M_B_DQS4
MB_DQS[3] F26 M_B_DQS3
MB_DQS[2] A24 M_B_DQS2
MB_DQS[1] D16 M_B_DQS1
MB_DQS[0] C12 M_B_DQS0
MB_DQS#[7] AE12 M_B_DQS#7
MB_DQS#[6] AD16 M_B_DQS#6
MB_DQS#[5] AF22 M_B_DQS#5
MB_DQS#[4] AC26 M_B_DQS#4
MB_DQS#[3] F26 M_B_DQS#3
MB_DQS#[2] A23 M_B_DQS#2
MB_DQS#[1] C16 M_B_DQS#1
MB_DQS#[0] B12 M_B_DQS#0
MB0_CLK[1] A17 M_B_CLK1
MB0_CLK#[1] A18 M_B_CLK1#
MB0_CLK[2] AF18 M_B_CLK2
MB0_CLK#[2] AF17 M_B_CLK2#
Tolerance is +-10%
C122 1.5P/50V/O
C121 1.5P/50V/O
M_B_CLK1 [5]
M_B_CLK1# [5]
M_B_CLK2 [5]
M_B_CLK2# [5]
TRACE FROM CAP TO CPU MUST BE LESS THAN 1200MILS MAX NECKDOWN TO & FROM CAPS IS 500MILS
MB_BANK[2] K26 M_B_BA2
MB_BANK[1] T26 M_B_BA1
MB_BANK[0] U26 M_B_BA0
MB_RAS# U24 M_B_RAS#
MB_CAS# V26 M_B_CAS#
MB_WE# U22 M_B_WE#
MB0_CS#[3] Y26 M_B_CS#3
MB0_CS#[2] J24 M_B_CS#2
MB0_CS#[1] W24 M_B_CS#1
MB0_CS#[0] U23 M_B_CS#0
MB_CKE[1] H26 M_B_CKE1
MB_CKE[0] J23 M_B_CKE0
MB0_ODT[1] W23 M_B_ODT1
MB0_ODT[0] W26 M_B_ODT0
VTT_SENSE Y10 VTERM_FB
VTERM_FB [37]
M_VREF W17 M_VREF
M_ZN AE10 MEMZN
M_ZP AF10 MEMZP
R581 39.2/F
R586 39.2/F
1.8VSUS
R80 2K/F
R78 2K/F
C106 1000P/50V/X
C120 0.1U/16V/V
M_VREF : W =20MIL AND SPACE = 20MIL
M_B_A15 J25
M_B_A14 J26
M_B_A13 W25
M_B_A12 L23
M_B_A11 L25
M_B_A10 U25
M_B_A9 L24
M_B_A8 M26
M_B_A7 L26
M_B_A6 N23
M_B_A5 N24
M_B_A4 N25
M_B_A3 N26
M_B_A2 P24
M_B_A1 P26
M_B_A0 T24
MB_ADD[15]
MB_ADD[14]
MB_ADD[13]
MB_ADD[12]
MB_ADD[11]
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MB_ADD[9]
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MB_ADD[4]
MB_ADD[3]
MB_ADD[2]
MB_ADD[1]
MB_ADD[0]
AMD S1 SOCKET
[5] M_A_DQ[0..63]
M_A_DQ[0..63]
[4,5] M_A_A[0..15]
M_A_A[0..15]
[5] M_A_DQM[0..7]
M_A_DQM[0..7]
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M_A_DQS[0..7]
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M_A_DQS#[0..7]
[4,5] M_A_BA[0..2]
M_A_BA[0..2]
[4,5] M_A_CS#[0..3]
M_A_CS#[0..3]
M_A_RAS#
M_A_CAS#
M_A_WE#
M_A_RAS# [4,5]
M_A_CAS# [4,5]
M_A_WE# [4,5]
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M_A_ODT[0..1]
M_A_CKE[0..1] [4,5]
M_A_ODT[0..1] [4,5]
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M_B_A[0..15]
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M_B_DQS#[0..7]
[4,5] M_B_BA[0..2]
M_B_BA[0..2]
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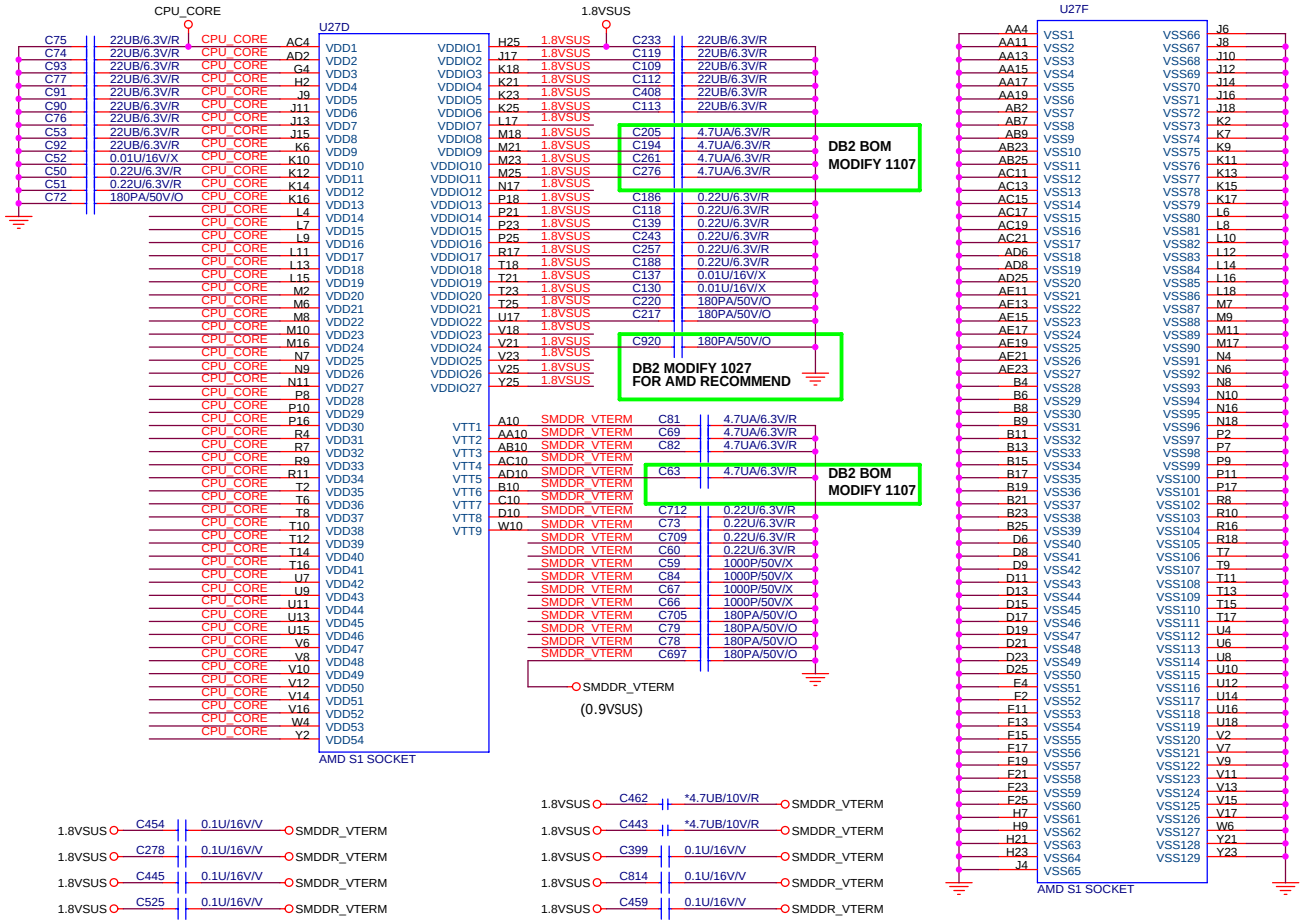
M_B_CS#[0..3]
M_B_RAS#
M_B_CAS#
M_B_WE#
M_B_RAS# [4,5]
M_B_CAS# [4,5]
M_B_WE# [4,5]
M_B_CKE[0..1]
M_B_ODT[0..1]
M_B_CKE[0..1] [4,5]
M_B_ODT[0..1] [4,5]
1.8VSUS [2,4,5,6,32,36,37]
NB5/RD2/HW1
PROJECT : AT1
Quanta Computer Inc.
Size Custom
Document Number CPU (MEM_I/F)
Rev C2A
Date: Wednesday, December 20, 2006 Sheet 3 of 40

CPU POWER PLANE AND BY PASS CAP

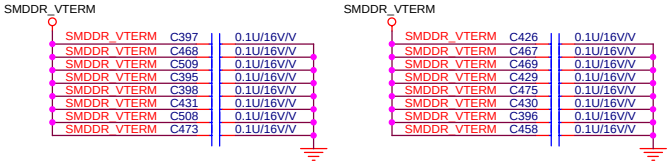


DDR2 TERMINATION BYPASS CAP

04

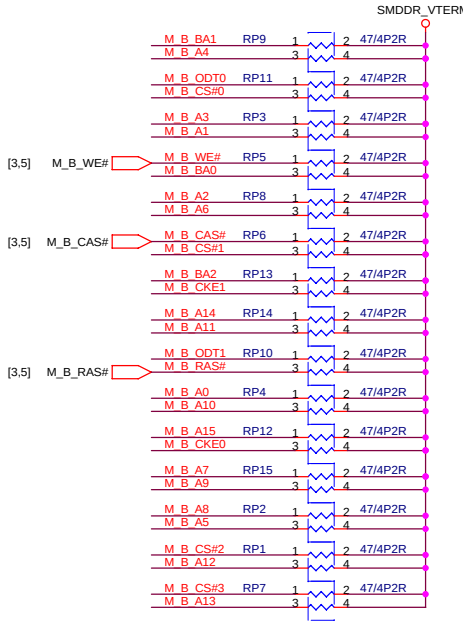
CHANNEL A

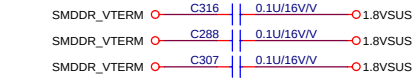
CHANNEL B



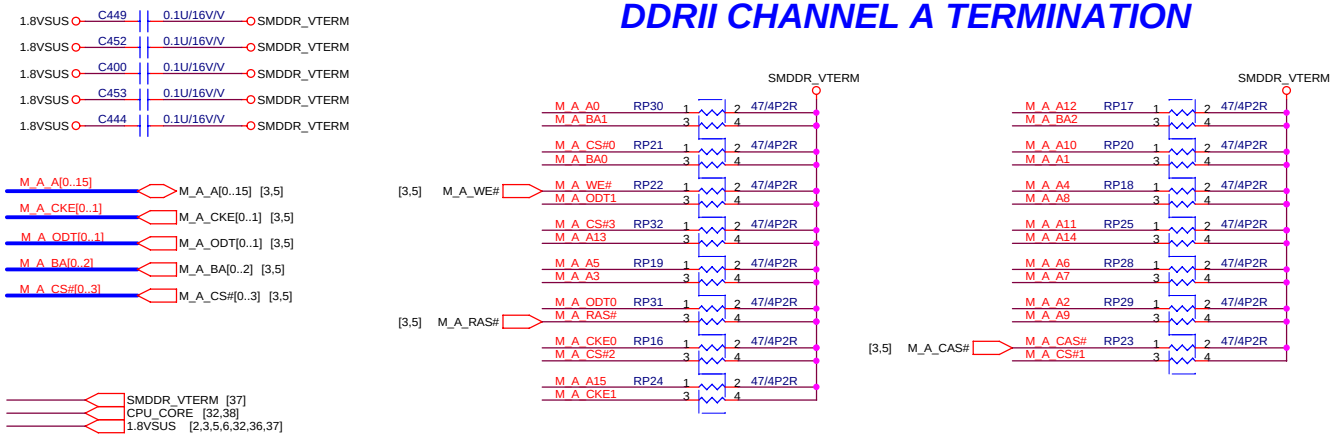
Layout note: Place one cap close to every 2 pullup resistors terminated to SMDDR_VTERM

DDRII CHANNEL B TERMINATION





DDRII CHANNEL A TERMINATION



NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU (POWER,GND),DDR2_TERM	C2A

Date: Wednesday, December 20, 2006 Sheet 4 of 40

M_A_RAS# M_A_CAS# M_A_WE# → M_A_RAS# [3,4] M_A_CAS# [3,4] M_A_WE# [3,4]

M_A_CLK1 M_A_CLK1# M_A_CLK2 M_A_CLK2# → M_A_CLK1 [3] M_A_CLK1# [3] M_A_CLK2 [3] M_A_CLK2# [3]

M_A_BA[0..2] → M_A_BA[0..2] [3,4]

M_A_CS#[0..3] → M_A_CS#[0..3] [3,4]

M_A_CKE[0..1] → M_A_CKE[0..1] [3,4]

M_A_ODT[0..1] → M_A_ODT[0..1] [3,4]

M_A_DQ[0..63] → M_A_DQ[0..63] [3]

M_A_A[15..0] → M_A_A[15..0] [3,4]

M_A_DQM[0..7] → M_A_DQM[0..7] [3]

M_A_DQS[0..7] → M_A_DQS[0..7] [3]

M_A_DQS#[0..7] → M_A_DQS#[0..7] [3]

M_B_RAS# M_B_CAS# M_B_WE# → M_B_RAS# [3,4] M_B_CAS# [3,4] M_B_WE# [3,4]

M_B_CLK1 M_B_CLK1# M_B_CLK2 M_B_CLK2# → M_B_CLK1 [3] M_B_CLK1# [3] M_B_CLK2 [3] M_B_CLK2# [3]

M_B_BA[0..2] → M_B_BA[0..2] [3,4]

M_B_CS#[0..3] → M_B_CS#[0..3] [3,4]

M_B_CKE[0..1] → M_B_CKE[0..1] [3,4]

M_B_ODT[0..1] → M_B_ODT[0..1] [3,4]

M_B_DQ[0..63] → M_B_DQ[0..63] [3]

M_B_A[0..15] → M_B_A[0..15] [3,4]

M_B_DQM[0..7] → M_B_DQM[0..7] [3]

M_B_DQS[0..7] → M_B_DQS[0..7] [3]

M_B_DQS#[0..7] → M_B_DQS#[0..7] [3]

CKE 0,1

PC2100 DDR2 SDRAM SO-DIMM (200P)

M_A_DQ5	5	DQ0	DQ32	123	M_A_DQ32
M_A_DQ1	7	DQ1	DQ33	125	M_A_DQ36
M_A_DQ2	17	DQ2	DQ34	135	M_A_DQ34
M_A_DQ3	19	DQ3	DQ35	137	M_A_DQ37
M_A_DQ0	4	DQ4	DQ36	124	M_A_DQ33
M_A_DQ4	6	DQ5	DQ37	126	M_A_DQ38
M_A_DQ6	14	DQ6	DQ38	134	M_A_DQ39
M_A_DQ7	16	DQ7	DQ39	136	M_A_DQ35
M_A_DQ9	23	DQ8	DQ40	141	M_A_DQ40
M_A_DQ8	25	DQ9	DQ41	143	M_A_DQ41
M_A_DQ10	35	DQ10	DQ42	151	M_A_DQ42
M_A_DQ14	37	DQ11	DQ43	153	M_A_DQ46
M_A_DQ13	20	DQ12	DQ44	140	M_A_DQ44
M_A_DQ12	22	DQ13	DQ45	142	M_A_DQ45
M_A_DQ15	36	DQ14	DQ46	152	M_A_DQ43
M_A_DQ11	38	DQ15	DQ47	154	M_A_DQ47
M_A_DQ17	43	DQ16	DQ48	157	M_A_DQ55
M_A_DQ21	45	DQ17	DQ49	159	M_A_DQ54
M_A_DQ18	55	DQ18	DQ50	173	M_A_DQ49
M_A_DQ16	57	DQ19	DQ51	175	M_A_DQ52
M_A_DQ20	44	DQ20	DQ52	158	M_A_DQ48
M_A_DQ19	46	DQ21	DQ53	160	M_A_DQ53
M_A_DQ22	56	DQ22	DQ54	174	M_A_DQ50
M_A_DQ23	58	DQ23	DQ55	176	M_A_DQ51
M_A_DQ24	61	DQ24	DQ56	179	M_A_DQ57
M_A_DQ25	63	DQ25	DQ57	181	M_A_DQ61
M_A_DQ27	73	DQ26	DQ58	189	M_A_DQ63
M_A_DQ30	75	DQ27	DQ59	191	M_A_DQ62
M_A_DQ28	62	DQ28	DQ60	180	M_A_DQ56
M_A_DQ29	64	DQ29	DQ61	182	M_A_DQ60
M_A_DQ26	74	DQ30	DQ62	192	M_A_DQ59
M_A_DQ31	76	DQ31	DQ63	194	M_A_DQ58

M_A_A0	102	A0	DM0	10	M_A_DQM0
M_A_A1	101	A1	DM1	26	M_A_DQM1
M_A_A2	100	A2	DM2	52	M_A_DQM2
M_A_A3	99	A3	DM3	67	M_A_DQM3
M_A_A4	98	A4	DM4	130	M_A_DQM4
M_A_A5	97	A5	DM5	147	M_A_DQM5
M_A_A6	94	A6	DM6	170	M_A_DQM6
M_A_A7	92	A7	DM7	185	M_A_DQM7
M_A_A8	93	A8	DQS0	13	M_A_DQS0
M_A_A9	91	A9	DQS0	11	M_A_DQS#0
M_A_A10	105	A10/AP	DQS1	31	M_A_DQS1
M_A_A11	90	A11	DQS1	29	M_A_DQS#1
M_A_A12	89	A12	DQS2	51	M_A_DQS2
			DQS2	49	M_A_DQS#2
M_A_BA0	107	BA0	DQS3	70	M_A_DQS3
M_A_BA1	106	BA1	DQS3	68	M_A_DQS#3
M_A_BA2	85	NC/BA2	DQS4	131	M_A_DQS4
			DQS4	129	M_A_DQS#4
M_A_CLK1	30	CLK0	DQS5	148	M_A_DQS5
M_A_CLK1#	32	CLK0	DQS5	146	M_A_DQS#5
			DQS6	169	M_A_DQS6
M_A_CLK2	164	CLK1	DQS6	167	M_A_DQS#6
M_A_CLK2#	166	CKL1	DQS7	188	M_A_DQS7
			DQS7	186	M_A_DQS#7
DDR_SMBCLK	197	SCL			
DDR_SMBDTA	195	SDA	CS0	110	M_A_CS#0
DIM1_SA0	198	SA0	CS1	115	M_A_CS#1
DIM1_SA1	200	SA1	RAS	108	M_A_RAS#
			CAS	113	M_A_CAS#
3V	199	VDDSPD	WE	109	M_A_WE#
			CKE0	79	M_A_CKE0
			CKE1	80	M_A_CKE1

CN28A
2-1734073-1

HEIGHT=9.2mm

R320 10K DIM1_SA0
R321 10K DIM1_SA1
SMbus address A0

DDR_SMBDTA — Q13 2N7002E — CGDAT_SMB [10]

DDR_SMBCLK — Q11 2N7002E — CGCLK_SMB [10]

CKE 2,3

PC2100 DDR2 SDRAM SO-DIMM (200P)

M_B_DQ1	5	DQ0	DQ32	123	M_B_DQ36
M_B_DQ4	7	DQ1	DQ33	125	M_B_DQ37
M_B_DQ3	17	DQ2	DQ34	135	M_B_DQ38
M_B_DQ2	19	DQ3	DQ35	137	M_B_DQ34
M_B_DQ0	4	DQ4	DQ36	124	M_B_DQ32
M_B_DQ5	6	DQ5	DQ37	126	M_B_DQ33
M_B_DQ7	14	DQ6	DQ38	134	M_B_DQ39
M_B_DQ6	16	DQ7	DQ39	136	M_B_DQ35
M_B_DQ9	23	DQ8	DQ40	141	M_B_DQ44
M_B_DQ8	25	DQ9	DQ41	143	M_B_DQ41
M_B_DQ14	35	DQ10	DQ42	151	M_B_DQ47
M_B_DQ15	37	DQ11	DQ43	153	M_B_DQ46
M_B_DQ12	20	DQ12	DQ44	140	M_B_DQ40
M_B_DQ13	22	DQ13	DQ45	142	M_B_DQ45
M_B_DQ10	36	DQ14	DQ46	152	M_B_DQ42
M_B_DQ11	38	DQ15	DQ47	154	M_B_DQ43
M_B_DQ17	43	DQ16	DQ48	157	M_B_DQ55
M_B_DQ20	45	DQ17	DQ49	159	M_B_DQ54
M_B_DQ19	55	DQ18	DQ50	173	M_B_DQ53
M_B_DQ18	57	DQ19	DQ51	175	M_B_DQ48
M_B_DQ16	44	DQ20	DQ52	158	M_B_DQ51
M_B_DQ21	46	DQ21	DQ53	160	M_B_DQ50
M_B_DQ22	56	DQ22	DQ54	174	M_B_DQ49
M_B_DQ23	58	DQ23	DQ55	176	M_B_DQ52
M_B_DQ24	61	DQ24	DQ56	179	M_B_DQ57
M_B_DQ25	63	DQ25	DQ57	181	M_B_DQ60
M_B_DQ30	73	DQ26	DQ58	189	M_B_DQ62
M_B_DQ31	75	DQ27	DQ59	191	M_B_DQ59
M_B_DQ28	62	DQ28	DQ60	180	M_B_DQ61
M_B_DQ29	64	DQ29	DQ61	182	M_B_DQ56
M_B_DQ27	74	DQ30	DQ62	192	M_B_DQ58
M_B_DQ26	76	DQ31	DQ63	194	M_B_DQ63

M_B_A0	102	A0	DM0	10	M_B_DQM0
M_B_A1	101	A1	DM1	26	M_B_DQM1
M_B_A2	100	A2	DM2	52	M_B_DQM2
M_B_A3	99	A3	DM3	67	M_B_DQM3
M_B_A4	98	A4	DM4	130	M_B_DQM4
M_B_A5	97	A5	DM5	147	M_B_DQM5
M_B_A6	94	A6	DM6	170	M_B_DQM6
M_B_A7	92	A7	DM7	185	M_B_DQM7
M_B_A8	93	A8	DQS0	13	M_B_DQS0
M_B_A9	91	A9	DQS0	11	M_B_DQS#0
M_B_A10	105	A10/AP	DQS1	31	M_B_DQS1
M_B_A11	90	A11	DQS1	29	M_B_DQS#1
M_B_A12	89	A12	DQS2	51	M_B_DQS2
			DQS2	49	M_B_DQS#2
M_B_BA0	107	BA0	DQS3	70	M_B_DQS3
M_B_BA1	106	BA1	DQS3	68	M_B_DQS#3
M_B_BA2	85	NC/BA2	DQS4	131	M_B_DQS4
			DQS4	129	M_B_DQS#4
M_B_CLK1	30	CLK0	DQS5	148	M_B_DQS5
M_B_CLK1#	32	CLK0	DQS5	146	M_B_DQS#5
			DQS6	169	M_B_DQS6
M_B_CLK2	164	CLK1	DQS6	167	M_B_DQS#6
M_B_CLK2#	166	CKL1	DQS7	188	M_B_DQS7
			DQS7	186	M_B_DQS#7
DDR_SMBCLK	197	SCL			
DDR_SMBDTA	195	SDA	CS0	110	M_B_CS#0
DIM2_SA0	198	SA0	CS1	115	M_B_CS#1
DIM2_SA1	200	SA1	RAS	108	M_B_RAS#
			CAS	113	M_B_CAS#
3V	199	VDDSPD	WE	109	M_B_WE#
			CKE0	79	M_B_CKE0
			CKE1	80	M_B_CKE1

CN26A
1565917-4

HEIGHT=5.2mm

DIM2_SA0 R280 10K
DIM2_SA1 R266 10K
3V
SMbus address A2

DDR_SMBDTA R281 2.2K → 3V

DDR_SMBCLK R282 2.2K → 3V

SMDDR_VREF_DIMM → VREF

C526 C819 C840 C813 C815 C402 C817 C821 C822 C824 C816 — 2.2UA/6.3V/R or 0.1U/16V/V — 1.8VSUS

1.8VSUS

M_A_ODT0 M_A_ODT1 → ODT0 ODT1

M_A_CS#2 M_A_A15 M_A_A14 M_A_A13 M_A_CS#3 → NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59

PC2100 DDR2 SDRAM SO-DIMM (200P)

CN28B
2-1734073-1

SMDDR_VREF_DIMM → VREF

C820 C818 C466 C838 C839 C836 C835 C401 C450 C823 C837 — 2.2UA/6.3V/R or 0.1U/16V/V — 1.8VSUS

1.8VSUS

M_B_ODT0 M_B_ODT1 → ODT0 ODT1

M_B_CS#2 M_B_A15 M_B_A14 M_B_A13 M_B_CS#3 → NC_1 NC_2 NC_3 NC_4/A15 NC_5/A14 NC_6/A13 NC_7 NC_8

VDD_1 VDD_2 VDD_3 VDD_4 VDD_5 VDD_6 VDD_7 VDD_8 VDD_9 VDD_10 VDD_11 VDD_12

VSS_1 VSS_2 VSS_3 VSS_4 VSS_5 VSS_6 VSS_7 VSS_8 VSS_9 VSS_10 VSS_11 VSS_12 VSS_13 VSS_14 VSS_15 VSS_16 VSS_17 VSS_18 VSS_19 VSS_20 VSS_21 VSS_22 VSS_23 VSS_24 VSS_25 VSS_26 VSS_27 VSS_28 VSS_29 VSS_30 VSS_31 VSS_45 VSS_46 VSS_47 VSS_48 VSS_49 VSS_50 VSS_51 VSS_52 VSS_53 VSS_54 VSS_55 VSS_56 VSS_57 VSS_58 VSS_59

PC2100 DDR2 SDRAM SO-DIMM (200P)

CN26B
1565917-4

SO-DIMM BYPASS PLACEMENT :

Place these Caps near So-Dimm1.

No Vias Between the Trace of PIN to CAP.

Close DDR2 socket

3V
C520 0.1U/16V/V 3V — 3V C507 *2.2UA/6.3V/R
C483 2.2UA/6.3V/R — C463 0.1U/16V/V

SMDDR_VREF_DIMM — R259 *0R — SMDDR_VREF [37]

R258 2K/F — R253 2K/F — 1.8VSUS

C474 C407 0.1U/16V/V 2.2UA/6.3V/R — SMDDR_VREF_DIMM — C457 C472 0.1U/16V/V 2.2UA/6.3V/R

SMDDR_VREF_DIMM :

TRACE WIDTH > 20 MIL
PUT BYPASS CAP ON EACH DIMM

Address:92h

U34 (*G751 (LM75CIMM3))

3V — A0 A1 A2 — +VS — C804 *0.1U/16V/V

O.S — DIMM_THEM# — DIMM_THEM# [2]

[2] LM86_SMD
[2] LM86_SMC
LM86_SMD LM86_SMC — SDA SCL — GND

3V — R673 *10K — DIMM_THEM#

1.8VSUS [2,3,4,6,32,36,37]
3V [2,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

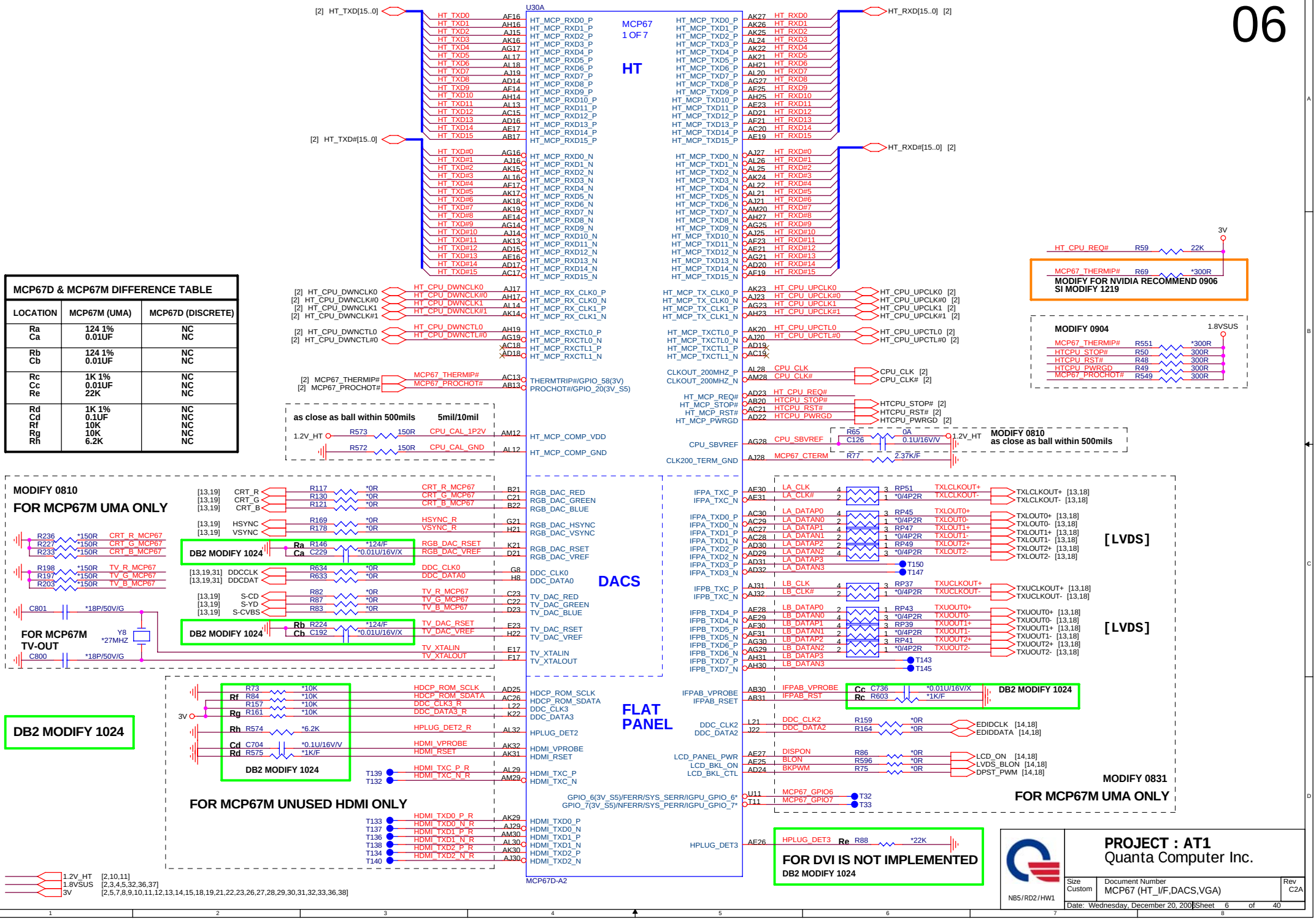
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

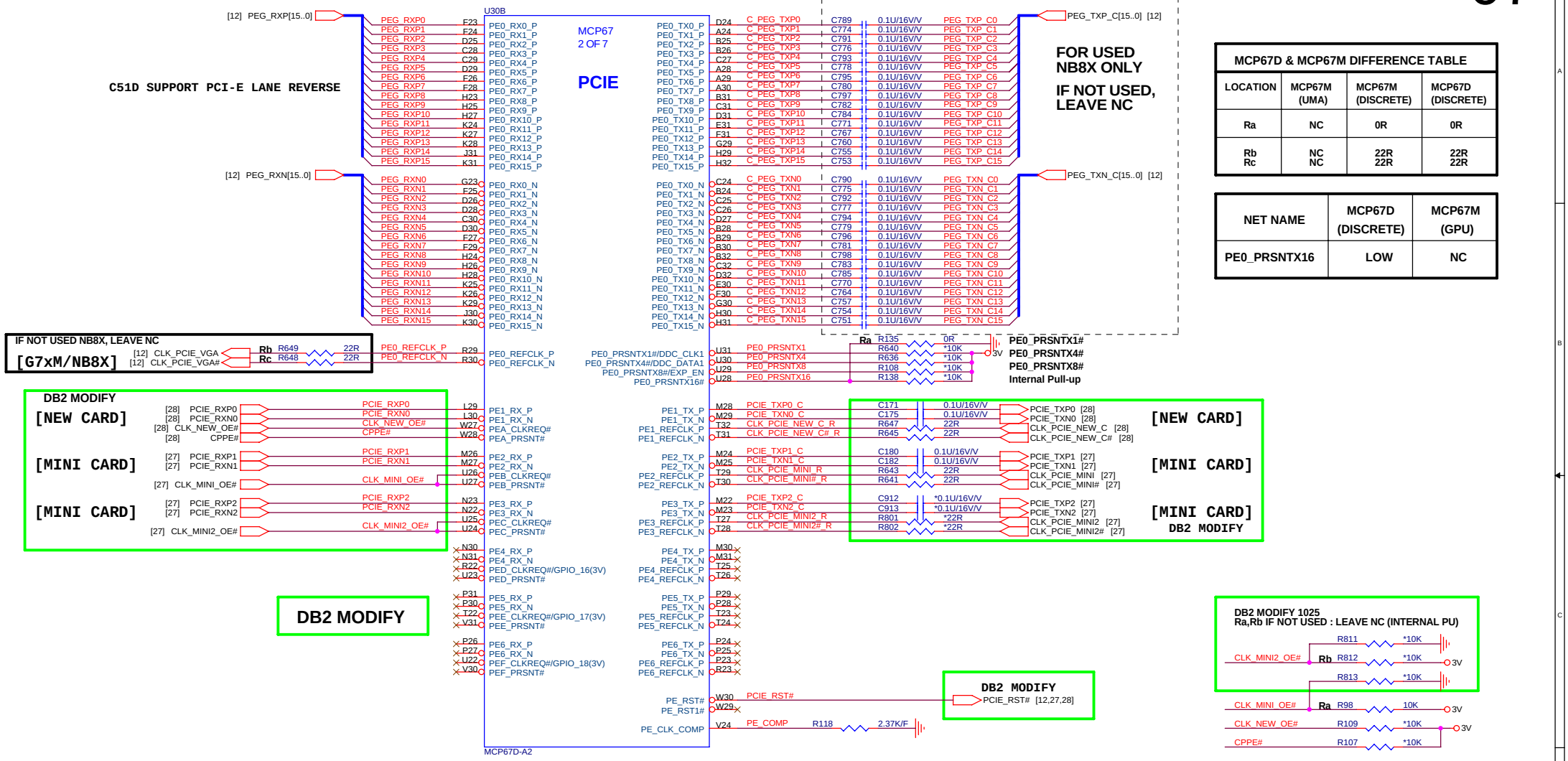
Size	Document Number	Rev
Custom	DDR SO-DIMMx2 (200P)	C2A

Date: Wednesday, December 20, 2006 Sheet 5 of 40

MCP67D & MCP67M DIFFERENCE TABLE		
LOCATION	MCP67M (UMA)	MCP67D (DISCRETE)
Ra Ca	124 1% 0.01UF	NC NC
Rb Cb	124 1% 0.01UF	NC NC
Rc Cc Re	1K 1% 0.01UF 22K	NC NC NC
Rd Cd Rf Rg Rh	1K 1% 0.1UF 10K 10K 6.2K	NC NC NC NC NC



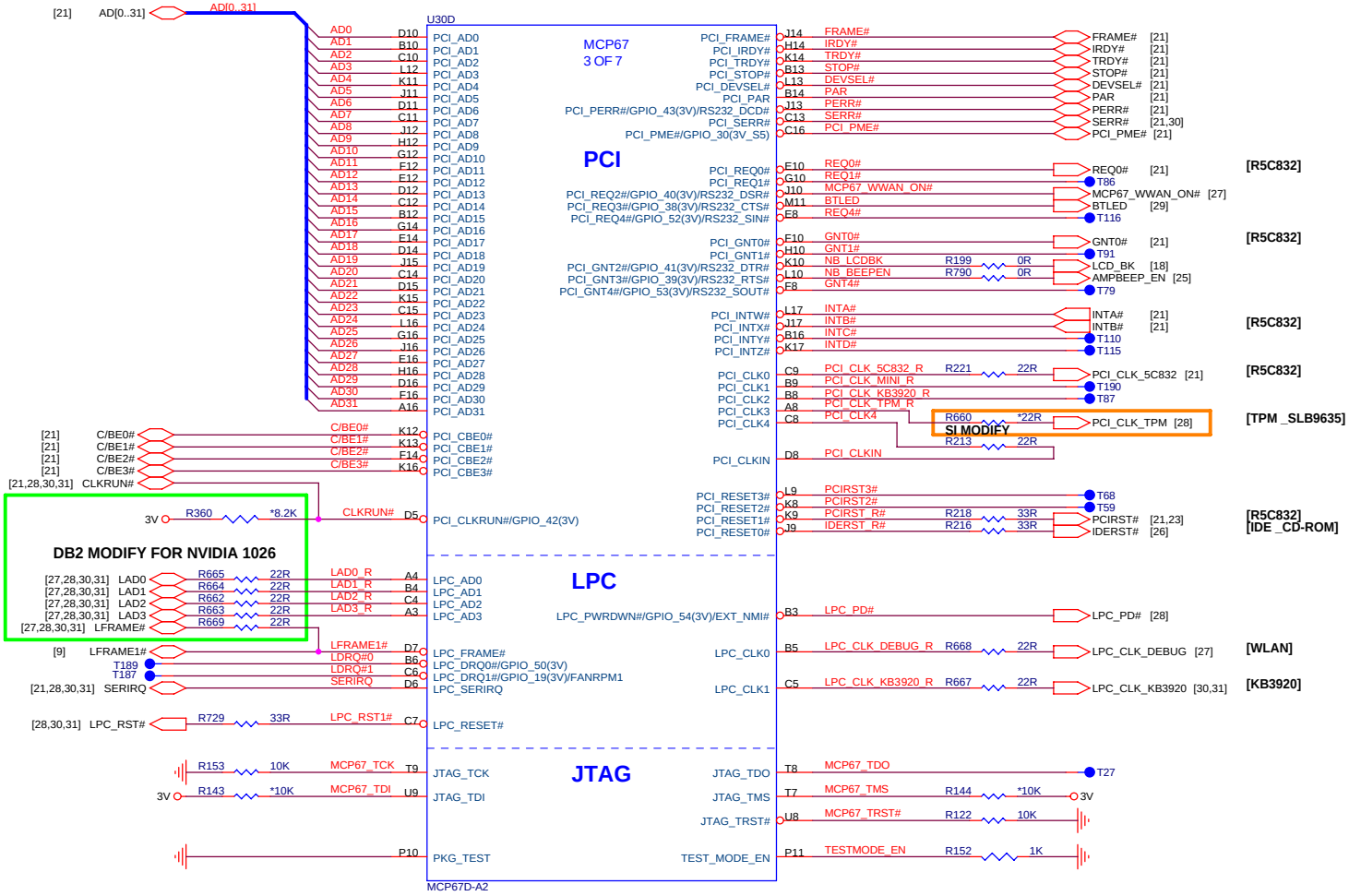
PROJECT : AT1	
Quanta Computer Inc.	
Size: Custom	Document Number: MCP67 (HT_I/F,DACS,VGA)
Rev: C2A	
NB5/RD2/HW1	Date: Wednesday, December 20, 2006 Sheet 6 of 40



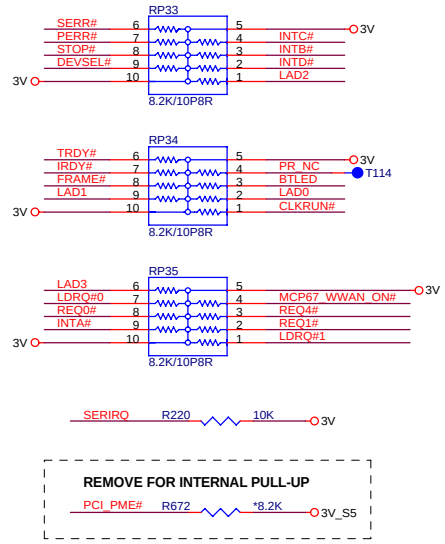
MCP67D & MCP67M DIFFERENCE TABLE			
LOCATION	MCP67M (UMA)	MCP67M (DISCRETE)	MCP67D (DISCRETE)
Ra	NC	0R	0R
Rb Rc	NC NC	22R 22R	22R 22R

NET NAME	MCP67D (DISCRETE)	MCP67M (GPU)
PE0_PRSNTX16	LOW	NC

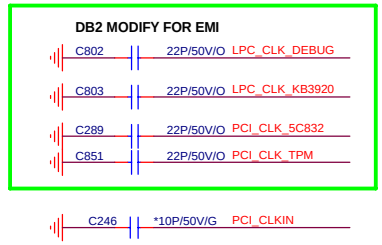
PROJECT :	AT1
Quanta Computer Inc.	
Size: Custom	Document Number: MCP67 (PCI-E_I/F)
Rev: C2A	
NB5/RD2/HW1	Date: Wednesday, December 20, 2006 Sheet 7 of 40



PCI/LPC PULL-UP

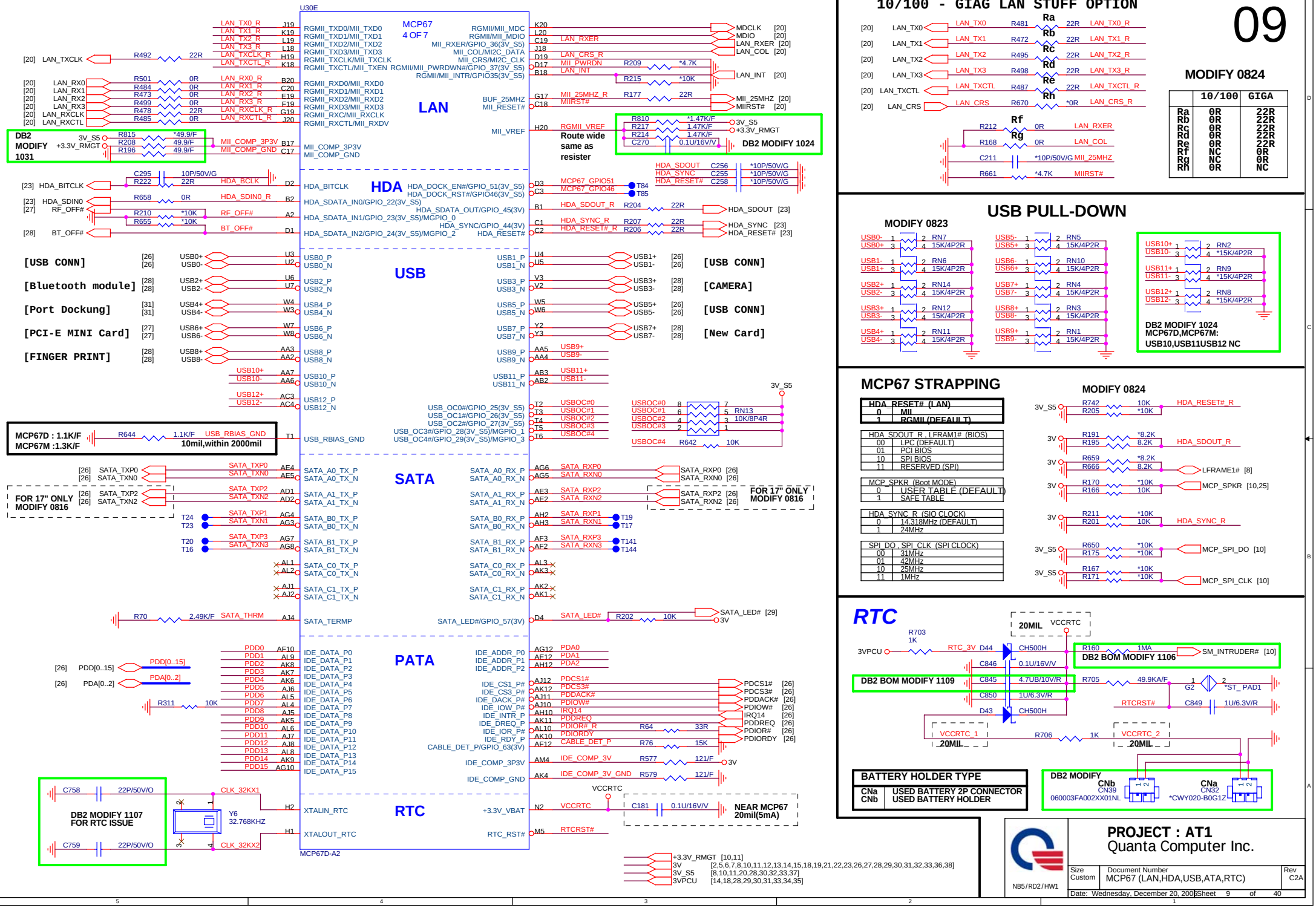


CLOCK BYPASS



3V [2,5,6,7,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [9,10,11,20,28,30,32,33,37]

PROJECT : AT1 Quanta Computer Inc.		
NB5/RD2/HW1	Size: Custom Document Number: MCP67 (PCI,LPC,JTAG)	Rev: C2A
	Date: Wednesday, December 20, 2006	Sheet 8 of 40



10/100 - GIAG LAN STUFF OPTION

09

MODIFY 0824

	10/100	GIGA
Ra	0R	22R
Rb	0R	22R
Rc	0R	22R
Rd	0R	22R
Re	0R	22R
Rf	NC	0R
Rg	NC	0R
Rh	0R	NC

USB PULL-DOWN

MODIFY 0823

DB2 MODIFY 1024
MCP67D,MCP67M:
USB10,USB11USB12 NC

MCP67 STRAPPING

HDA_RESET# (LAN)
0 MII
1 RGMII (DEFAULT)

HDA_SDOUT_R , LFRAM1# (BIOS)
00 LPC (DEFAULT)
01 PCI BIOS
10 SPI BIOS
11 RESERVED (SPI)

MCP_SPKR (Boot MODE)
0 USER TABLE (DEFAULT)
1 SAFE TABLE

HDA_SYNC_R (SIO CLOCK)
0 14.318MHz (DEFAULT)
1 24MHz

SPI_DO , SPI_CLK (SPI CLOCK)
00 31MHz
01 42MHz
10 25MHz
11 1MHz

MODIFY 0824

RTC

BATTERY HOLDER TYPE	
CNa	USED BATTERY 2P CONNECTOR
CNb	USED BATTERY HOLDER

DB2 MODIFY
CNb CN39 060003FA002XX01NL
CNa CN32 *CWY020-B0G1Z

NEAR MCP67 20mil(5mA)

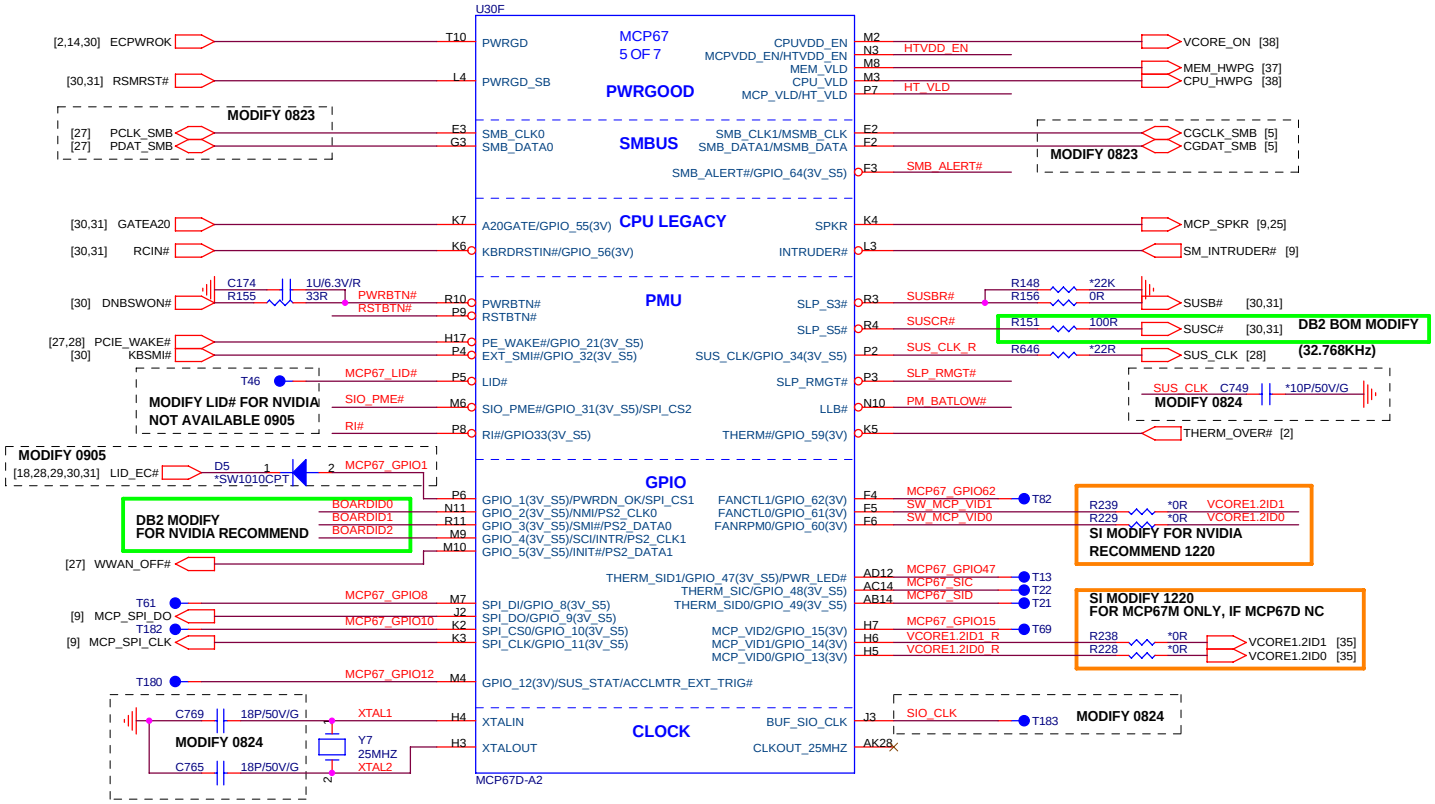
+3.3V_RMGT [10,11]
3V [2,5,6,7,8,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,10,11,20,28,30,32,33,37]
3VPCU [14,18,28,29,30,31,33,34,35]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

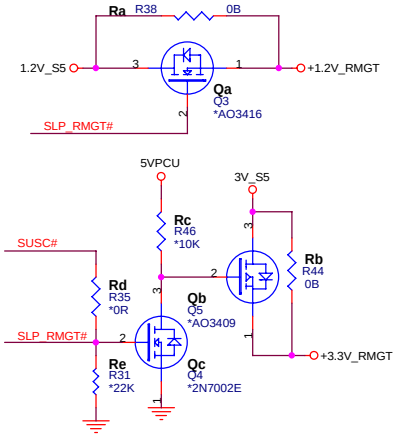
Size	Document Number	Rev
Custom	MCP67 (LAN,HDA,USB,ATA,RTC)	C2A

Date: Wednesday, December 20, 2006 Sheet 9 of 40



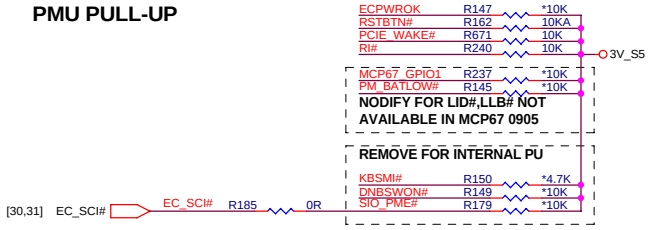
CORE POWER CIRCIUT FOR SLEEP MODE
MCP67M SUPPORT ONLY

10



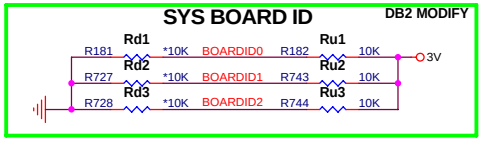
MCP67M & MCP67D DIFFERENCE TABLE		
	MCP67M UMA	MCP67D DISCRETE
Ra	NC	STUFF
Rb	NC	STUFF
Rc	STUFF	NC
Rd	NC	NC
Re	STUFF	NC
Qa	STUFF	NC
Qb	STUFF	NC
Qc	NC	NC

PMU PULL-UP



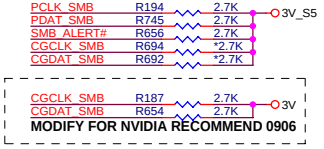
SKU (BOARD ID)	AT1A (DISCRETE)	AT1A (UMA)	AT1B (UMA ONLY)	AT2A (DISCRETE)	AT2A (UMA)
Board ID	X10	X00	X00	X11	X01
ID0 STUFF	Rd1	Rd1	Rd1	Ru1	Ru1
ID1 STUFF	Ru2	Rd2	Rd2	Ru2	Rd2
ID2 STUFF	Rd3				

Board ID :	0/1	0/1	0/1
DIFINE	RESERVE / RESERVE	UMA / DISCRETE	AT1 / AT2

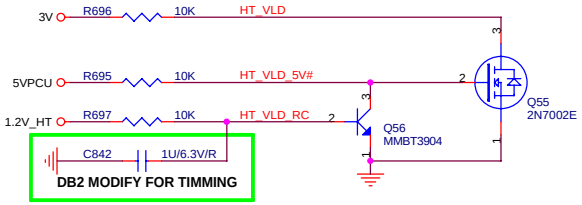


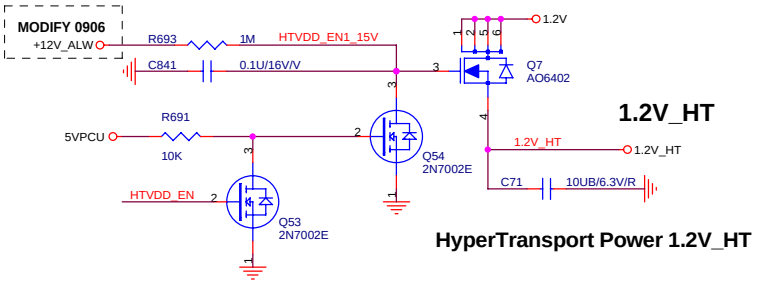
CPU LEGACY PULL-UP

SMB/I2C PULL-UP



HyperTransport Link 1.2 V_HT Power Valid





+1.2V_RMGT [11]
1.2V_S5 [11,32,35]
1.2V_HT [2,6,11]
1.2V [11,12,13,15,36]
+3.3V_RMGT [9,11]
3V [2,5,6,7,8,9,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,9,11,20,28,30,32,33,37]
5VPCU [23,33,34,35,36,37,38]
+12V_ALW [18,32,33]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (PG,SMB,PMU,GPIO,CLK)	C2A

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MCP67 POWER PLANE/GND & BYPASS

4717mA

390mA

242mA

100mA

52mA

1533mA

308mA

75mA

350mA

47mA

15mA

25mA

268mA

52mA

30mA

117mA

8mA

91mA

70mA

15mA

127mA

DB2 BOM MODIFY 1106
FOR LEAD-FREE

DB2 MODIFY 1024

DB2 MODIFY 1024
FOR USED
MCP67M
UMA ONLY

NVIDIA
RECOMMEND

La STUFF
Lb EMPTY
FOR MCP6B

DB2 MODIFY 1024

ONLY FOR MCP67D (DISCRETE)

MCP67 Signal Name	Component
+3VDAC	NC
+1.8V_IFP	NC
+3.3V_HDMI	NC
+3.3V_PLL_IFPP	NC
+3.3V_PLL	NC

TRACE WIDTH / SPACING :

+1.2V_HT_PLL	25mil / 10mil
+3.3V_PLL	25mil / 10mil
+3VDAC	25mil / 10mil
+1.8V_IFP	
+3.3V_HDMI	25mil / 10mil
+3.3V_PLL_IFPP	25mil / 10mil
1.2V_PEA	25mil / 10mil
+1.2V_PED	25mil / 10mil
+1.2V_PLLPE	25mil / 10mil
+1.2V_PLLPE_SS	25mil / 10mil
+1.2V_SP_D	25mil / 10mil
+1.2V_SP_A	25mil / 10mil
+1.2V_PLL_SP_VDD	
+1.2V_PLL_SP_SS	25mil / 10mil
+1.2V_RMGT	
+3.3V_RMGT	
+3.3V_PLL_MAC_DUAL	
+3.3V_USB_DUAL	25mil / 10mil
1.2V_DUAL	25mil / 10mil
+3V_DUAL	25mil / 10mil
+1.2V_RBB	25mil / 10mil

3V [2,5,6,7,8,9,10,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3V_S5 [8,9,10,20,28,30,32,33,37]
+3.3V_RMGT [9,10]
1.8V [13,15,16,17,32,37]
1.2V_VCORE [35,36]
1.2V [10,12,13,15,36]
1.2V_HT [2,6,10]
1.2V_S5 [10,32,35]
+1.2V_RMGT [10]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MCP67 (POWER,GND)	C2A

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U33F

AA12 GND_0	GND_80 D4	
AA2 GND_1	GND_81 D7	
AA21 GND_2	GND_82 F11	
AA31 GND_3	GND_83 F14	
AB27 GND_4	GND_84 F19	
AB6 GND_5	GND_85 F2	
AC10 GND_6	GND_86 F22	
AC23 GND_7	GND_87 F25	
AC29 GND_8	GND_88 F31	
AC4 GND_9	GND_89 F8	
AD16 GND_10	GND_90 G26	
AD17 GND_11	GND_91 G29	
AD2 GND_12	GND_92 G4	
AD31 GND_13	GND_93 G7	
AE17 GND_14	GND_94 H27	
AE27 GND_15	GND_95 H6	
AE6 GND_16	GND_96 J16	
AE11 GND_17	GND_97 J17	
AE26 GND_18	GND_98 J2	
AE29 GND_19	GND_99 J31	
AE4 GND_20	GND_100 K10	
AE7 GND_21	GND_101 K23	
AG10 GND_22	GND_102 K29	
AG11 GND_23	GND_103 K4	
AG14 GND_24	GND_104 L27	
AG15 GND_25	GND_105 L6	
AG19 GND_26	GND_106 M12	
AG2 GND_27	GND_107 M2	
AG22 GND_28	GND_108 M31	
AG31 GND_29	GND_109 N15	
AG8 GND_30	GND_110 N18	
AH24 GND_31	GND_111 N29	
AJ10 GND_32	GND_112 N4	
AJ13 GND_33	GND_113 P15	
AJ16 GND_34	GND_114 P18	
AJ17 GND_35	GND_115 P27	
AJ20 GND_36	GND_116 P6	
AJ23 GND_37	GND_117 R13	
AJ26 GND_38	GND_118 R14	
AJ29 GND_39	GND_119 R15	
AJ4 GND_40	GND_120 R18	
AJ7 GND_41	GND_121 R19	
AK2 GND_42	GND_122 R2	
AK28 GND_43	GND_123 R20	
AK31 GND_44	GND_124 R31	
AL11 GND_45	GND_125 T16	
AL14 GND_46	GND_126 T17	
AL19 GND_47	GND_127 T24	
AL22 GND_48	GND_128 T29	
AL25 GND_49	GND_129 T4	
AL3 GND_50	GND_130 U16	
AL6 GND_51	GND_131 U17	
AL9 GND_52	GND_132 U24	
AM13 GND_53	GND_133 U29	
AM16 GND_54	GND_134 U8	
AM17 GND_55	GND_135 V13	
AM20 GND_56	GND_136 V14	
AM23 GND_57	GND_137 V15	
AM26 GND_58	GND_138 V18	
AM29 GND_59	GND_139 V19	
B12 GND_60	GND_140 V2	
B15 GND_61	GND_141 V20	
B18 GND_62	GND_142 V31	
B21 GND_63	GND_143 W15	
B24 GND_64	GND_144 W18	
B27 GND_65	GND_145 W27	
B3 GND_66	GND_146 W6	
B30 GND_67	GND_147 Y15	
B6 GND_68	GND_148 Y18	
B9 GND_69	GND_149 Y29	
C2 GND_70	GND_150 Y4	
C31 GND_71	GND_151 AL10	
D10 GND_72	GND_152 AM10	
D13 GND_73	GND_153 AG13	
D16 GND_74		
D17 GND_75		
D20 GND_76		
D23 GND_77		
D26 GND_78		
D29 GND_79		

NB8M-GS-B-A1/H

[7] PEG_RXP0	PEG_RXP0	C215	0.1U/16V/V	C_PEG_RXP0	AJ15
[7] PEG_RXN0	PEG_RXN0	C227	0.1U/16V/V	C_PEG_RXN0	AK15
[7] PEG_RXP1	PEG_RXP1	C222	0.1U/16V/V	C_PEG_RXP1	AH16
[7] PEG_RXN1	PEG_RXN1	C231	0.1U/16V/V	C_PEG_RXN1	AG16
[7] PEG_RXP2	PEG_RXP2	C238	0.1U/16V/V	C_PEG_RXP2	AG17
[7] PEG_RXN2	PEG_RXN2	C254	0.1U/16V/V	C_PEG_RXN2	AH17
[7] PEG_RXP3	PEG_RXP3	C252	0.1U/16V/V	C_PEG_RXP3	AG18
[7] PEG_RXN3	PEG_RXN3	C260	0.1U/16V/V	C_PEG_RXN3	AH18
[7] PEG_RXP4	PEG_RXP4	C269	0.1U/16V/V	C_PEG_RXP4	AK18
[7] PEG_RXN4	PEG_RXN4	C280	0.1U/16V/V	C_PEG_RXN4	AJ18
[7] PEG_RXP5	PEG_RXP5	C275	0.1U/16V/V	C_PEG_RXP5	AJ19
[7] PEG_RXN5	PEG_RXN5	C286	0.1U/16V/V	C_PEG_RXN5	AH19
[7] PEG_RXP6	PEG_RXP6	C310	0.1U/16V/V	C_PEG_RXP6	AG20
[7] PEG_RXN6	PEG_RXN6	C299	0.1U/16V/V	C_PEG_RXN6	AH20
[7] PEG_RXP7	PEG_RXP7	C285	0.1U/16V/V	C_PEG_RXP7	AG21
[7] PEG_RXN7	PEG_RXN7	C293	0.1U/16V/V	C_PEG_RXN7	AH21
[7] PEG_RXP8	PEG_RXP8	C309	0.1U/16V/V	C_PEG_RXP8	AK21
[7] PEG_RXN8	PEG_RXN8	C321	0.1U/16V/V	C_PEG_RXN8	AJ21
[7] PEG_RXP9	PEG_RXP9	C326	0.1U/16V/V	C_PEG_RXP9	AJ22
[7] PEG_RXN9	PEG_RXN9	C334	0.1U/16V/V	C_PEG_RXN9	AH22
[7] PEG_RXP10	PEG_RXP10	C331	0.1U/16V/V	C_PEG_RXP10	AG23
[7] PEG_RXN10	PEG_RXN10	C338	0.1U/16V/V	C_PEG_RXN10	AH23
[7] PEG_RXP11	PEG_RXP11	C346	0.1U/16V/V	C_PEG_RXP11	AK24
[7] PEG_RXN11	PEG_RXN11	C351	0.1U/16V/V	C_PEG_RXN11	AJ24
[7] PEG_RXP12	PEG_RXP12	C359	0.1U/16V/V	C_PEG_RXP12	AJ25
[7] PEG_RXN12	PEG_RXN12	C349	0.1U/16V/V	C_PEG_RXN12	AH25
[7] PEG_RXP13	PEG_RXP13	C373	0.1U/16V/V	C_PEG_RXP13	AH26
[7] PEG_RXN13	PEG_RXN13	C363	0.1U/16V/V	C_PEG_RXN13	AG26
[7] PEG_RXP14	PEG_RXP14	C367	0.1U/16V/V	C_PEG_RXP14	AK27
[7] PEG_RXN14	PEG_RXN14	C376	0.1U/16V/V	C_PEG_RXN14	AJ27
[7] PEG_RXP15	PEG_RXP15	C375	0.1U/16V/V	C_PEG_RXP15	AJ28
[7] PEG_RXN15	PEG_RXN15	C366	0.1U/16V/V	C_PEG_RXN15	AH27

[7] PEG_TXP_C0	PEG_TXP_C0	AK13
[7] PEG_TXN_C0	PEG_TXN_C0	AK14
[7] PEG_TXP_C1	PEG_TXP_C1	AM14
[7] PEG_TXN_C1	PEG_TXN_C1	AM15
[7] PEG_TXP_C2	PEG_TXP_C2	AL15
[7] PEG_TXN_C2	PEG_TXN_C2	AL16
[7] PEG_TXP_C3	PEG_TXP_C3	AK16
[7] PEG_TXN_C3	PEG_TXN_C3	AK17
[7] PEG_TXP_C4	PEG_TXP_C4	AL17
[7] PEG_TXN_C4	PEG_TXN_C4	AL18
[7] PEG_TXP_C5	PEG_TXP_C5	AM18
[7] PEG_TXN_C5	PEG_TXN_C5	AM19
[7] PEG_TXP_C6	PEG_TXP_C6	AK19
[7] PEG_TXN_C6	PEG_TXN_C6	AK20
[7] PEG_TXP_C7	PEG_TXP_C7	AL20
[7] PEG_TXN_C7	PEG_TXN_C7	AL21
[7] PEG_TXP_C8	PEG_TXP_C8	AM21
[7] PEG_TXN_C8	PEG_TXN_C8	AM22
[7] PEG_TXP_C9	PEG_TXP_C9	AK22
[7] PEG_TXN_C9	PEG_TXN_C9	AK23
[7] PEG_TXP_C10	PEG_TXP_C10	AL23
[7] PEG_TXN_C10	PEG_TXN_C10	AL24
[7] PEG_TXP_C11	PEG_TXP_C11	AM24
[7] PEG_TXN_C11	PEG_TXN_C11	AM25
[7] PEG_TXP_C12	PEG_TXP_C12	AK25
[7] PEG_TXN_C12	PEG_TXN_C12	AK26
[7] PEG_TXP_C13	PEG_TXP_C13	AL26
[7] PEG_TXN_C13	PEG_TXN_C13	AL27
[7] PEG_TXP_C14	PEG_TXP_C14	AM27
[7] PEG_TXN_C14	PEG_TXN_C14	AM28
[7] PEG_TXP_C15	PEG_TXP_C15	AL28
[7] PEG_TXN_C15	PEG_TXN_C15	AL29

[7] CLK_PCIE_VGA	CLK_PCIE_VGA	AH14
[7] CLK_PCIE_VGA#	CLK_PCIE_VGA#	AJ14
	VGA_RST#	AH15

U33A

PCIE

PEX_TX0	PEX_TX0#
PEX_TX1	PEX_TX1#
PEX_TX2	PEX_TX2#
PEX_TX3	PEX_TX3#
PEX_TX4	PEX_TX4#
PEX_TX5	PEX_TX5#
PEX_TX6	PEX_TX6#
PEX_TX7	PEX_TX7#
PEX_TX8	PEX_TX8#
PEX_TX9	PEX_TX9#
PEX_TX10	PEX_TX10#
PEX_TX11	PEX_TX11#
PEX_TX12	PEX_TX12#
PEX_TX13	PEX_TX13#
PEX_TX14	PEX_TX14#
PEX_TX15	PEX_TX15#
PEX_RX0	PEX_RX0#
PEX_RX1	PEX_RX1#
PEX_RX2	PEX_RX2#
PEX_RX3	PEX_RX3#
PEX_RX4	PEX_RX4#
PEX_RX5	PEX_RX5#
PEX_RX6	PEX_RX6#
PEX_RX7	PEX_RX7#
PEX_RX8	PEX_RX8#
PEX_RX9	PEX_RX9#
PEX_RX10	PEX_RX10#
PEX_RX11	PEX_RX11#
PEX_RX12	PEX_RX12#
PEX_RX13	PEX_RX13#
PEX_RX14	PEX_RX14#
PEX_RX15	PEX_RX15#
PEX_REFCLK	PEX_REFCLK#
PEX_RST#	
RFU0	RFU1
PEX_TSTCLK_OUT	PEX_TSTCLK_OUT#

NB8M-GS-B-A1/H

VGA_VDD

PEX_IOVDD_0	AD23	C292	0.1U/16V/V	1.2V
PEX_IOVDD_1	AF23	C296	0.1U/16V/V	
PEX_IOVDD_2	AF24	C371	1U/6.3V/R	
PEX_IOVDD_3	AF25	C237	1U/6.3V/R	
PEX_IOVDD_4	AG24			
PEX_IOVDD_5	AG25	C808	4.7UB/10V/R	DB2 BOM MODIFY 1109

PLACE NEAR GPU

VGA_VDDQ

PEX_IOVDDQ_0	AC16			
PEX_IOVDDQ_1	AC17			1.2V
PEX_IOVDDQ_2	AC21	C320	0.1U/16V/V	
PEX_IOVDDQ_3	AC22	C361	0.1U/16V/V	
PEX_IOVDDQ_4	AE18	C291	0.47UA/10V/X	
PEX_IOVDDQ_5	AE21	C308	0.47UA/10V/X	
PEX_IOVDDQ_6	AE22	C347	1U/6.3V/R	
PEX_IOVDDQ_7	AE12	C264	1U/6.3V/R	
PEX_IOVDDQ_8	AF18	C319	10UA/6.3V/R	
PEX_IOVDDQ_9	AF21	C332	0.1U/16V/V	
PEX_IOVDDQ_10	AF22	C314	0.1U/16V/V	

PLACE NEAR GPU

VDD_0	K16			VGA_CORE
VDD_1	K17			
VDD_2	N13	C312	0.1U/16V/V	
VDD_3	N14	C311	0.1U/16V/V	
VDD_4	N16	C325	0.1U/16V/V	
VDD_5	N17	C329	0.1U/16V/V	
VDD_6	N19	C274	0.1U/16V/V	
VDD_7	P13	C271	10UA/6.3V/R	
VDD_8	P14	C324	0.1U/16V/V	
VDD_9	P16	C284	1U/6.3V/R	
VDD_10	P17	C273	0.1U/16V/V	
VDD_11	P19	C267	0.1U/16V/V	
VDD_12	R16	C283	0.1U/16V/V	
VDD_13	R17	C330	0.1U/16V/V	
VDD_15	T14	C272	10UA/6.3V/R	
VDD_16	T15	C297	0.47UA/10V/X	
VDD_17	T18	C335	0.47UA/10V/X	
VDD_18	T19	C249	0.47UA/10V/X	
VDD_19	U13	C268	0.47UA/10V/X	

PLACE NEAR GPU

VDD_20	U14	C318	1U/6.3V/R	
VDD_21	U15	C317	1U/6.3V/R	
VDD_22	U18	C298	0.47UA/10V/X	
VDD_23	U19	C304	0.47UA/10V/X	
VDD_24	V16	C322	0.47UA/10V/X	
VDD_25	V17	C277	0.47UA/10V/X	
VDD_26	W13	C337	0.47UA/10V/X	
VDD_27	W14	C341	0.47UA/10V/X	
VDD_28	W16	C300	10UA/6.3V/R	
VDD_29	W17			
VDD_30	W19			
VDD_31	Y13			
VDD_32	Y14			
VDD_33	Y16			
VDD_34	Y17			
VDD_35	Y19			
VDD_36	Y20			

1.2V [10,11,13,15,36]
VGA_CORE [35]
3V [2,5,6,7,8,9,10,11,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

VDD_LP_0	P20			
VDD_LP_1	T20			
VDD_LP_2	T23			
VDD_LP_3	U20			
VDD_LP_4	U23			
VDD_LP_5	W20			
VDD_SENSE	N20	VDD_SENSE	C328	*0.01U/16V/X
GND_SENSE	M21	GND_SENSE		

T94 T95

VDD33_0	AC11	VGA_VDD3	R119	0B 3V
VDD33_1	AC12			
VDD33_2	AC24	C198	0.1U/16V/V	
VDD33_3	AD24	C197	0.1U/16V/V	
VDD33_4	AE11	C193	0.1U/16V/V	
VDD33_5	AE12	C362	0.47UA/10V/X	
VDD33_6	H7	C250	0.47UA/10V/X	
VDD33_7	J7	C230	0.47UA/10V/X	
VDD33_8	K7	C199	1U/6.3V/R	
VDD33_9	L10			
VDD33_10	L7			
VDD33_11	L8			
VDD33_12	M10			

PLACE NEAR GPU

PEX_PLLAVDD	AE15	15mil	L14	10nHA/0.3A 1.2V
PEX_PLLDVDD	AE15	PEX_PLLAVDD	C263	1U/6.3V/R
PEX_PLLGND	AE16	PEX_PLLDVDD	C135	0.01U/16V/X
			C134	0.1U/16V/V
			C128	4.7UA/6.3V/R
		15mil	L12	10nHA/0.3A 1.2V
			C131	1U/6.3V/R
			C123	0.01U/16V/X
			C282	0.1U/16V/V
			C101	4.7UA/6.3V/R
NV_PLLAVDD	T13	15mil NV_PLLAVDD		VGA_CORE

PLACE NEAR GPU

SI MODIFY 1215
FOR NVIDIA RECOMMEND

NC_0	AM8	
NC_1	AM9	
NC_2	B32	
SPDIF	J6	SPDIF_VGA

3V
D2 CH501H
D1 CH501H
SPDIF_VGA
Ra R126 *24.3K/F
Rb R120 *3.4KA/F
SI MODIFY
C166 C 0.01U/16V/X
SPDIF
SPDIF [23,31]
Rc R136 *76.8/F

For 3.3V swing, we can remove Ra, Rb and Rc and replace C with 0ohm resistor.

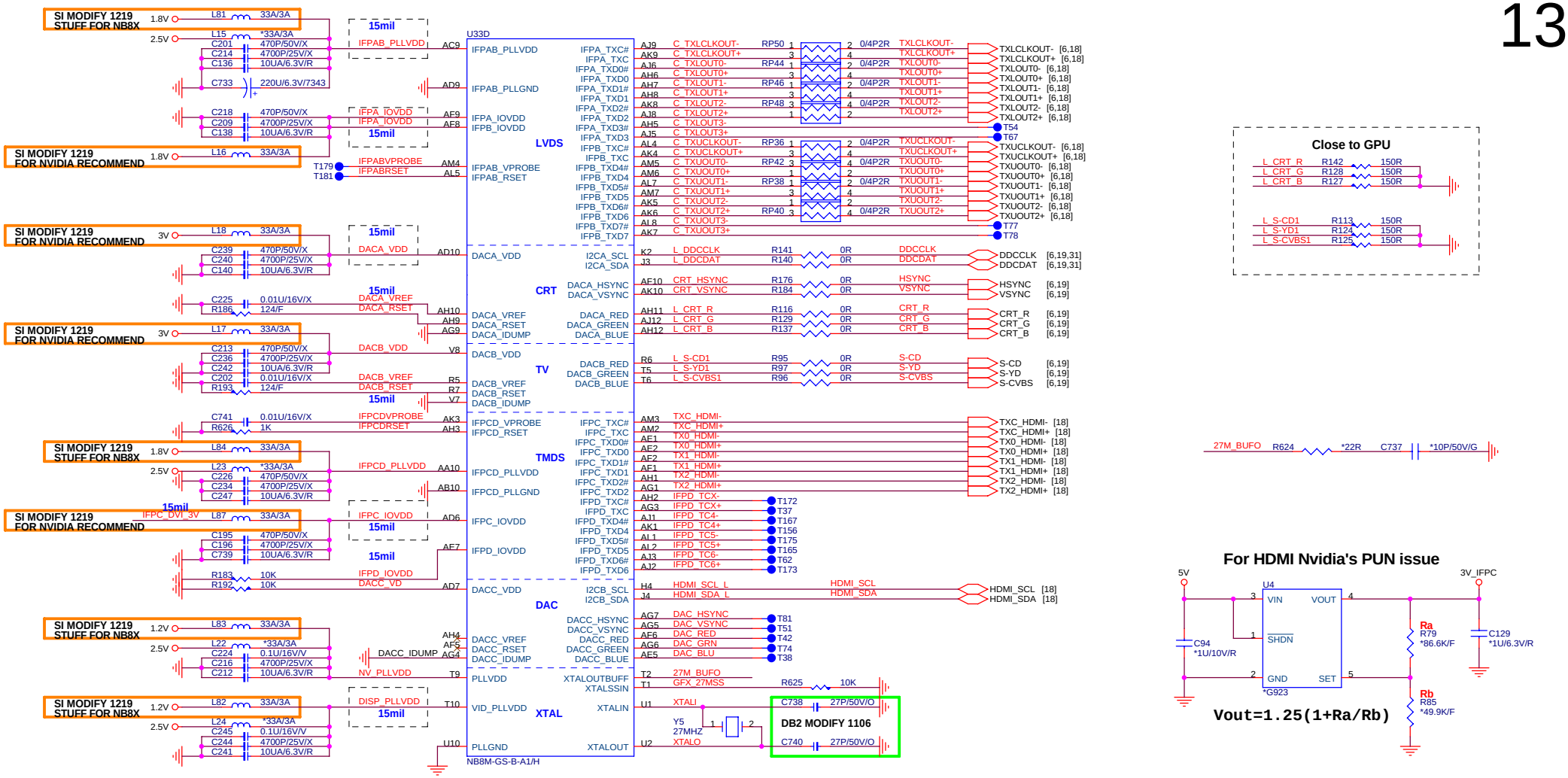
[7,27,28] PCIE_RST#
C761 0.1U/16V/V
3V
U31
*TC7SH08FU
R653 100K
T88 VGA_RFU0
T93 VGA_RFU1
T186 PEX_TSTCK
T184 PEX_TSTCK#
G7XM:STUFF,G8X:NC
D41 CH500H

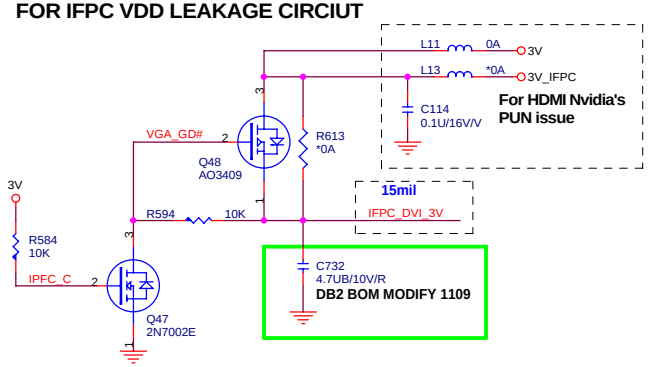
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M (PCIE_I/F,GND)	C2A

Date: Wednesday, December 20, 2006 Sheet 12 of 40





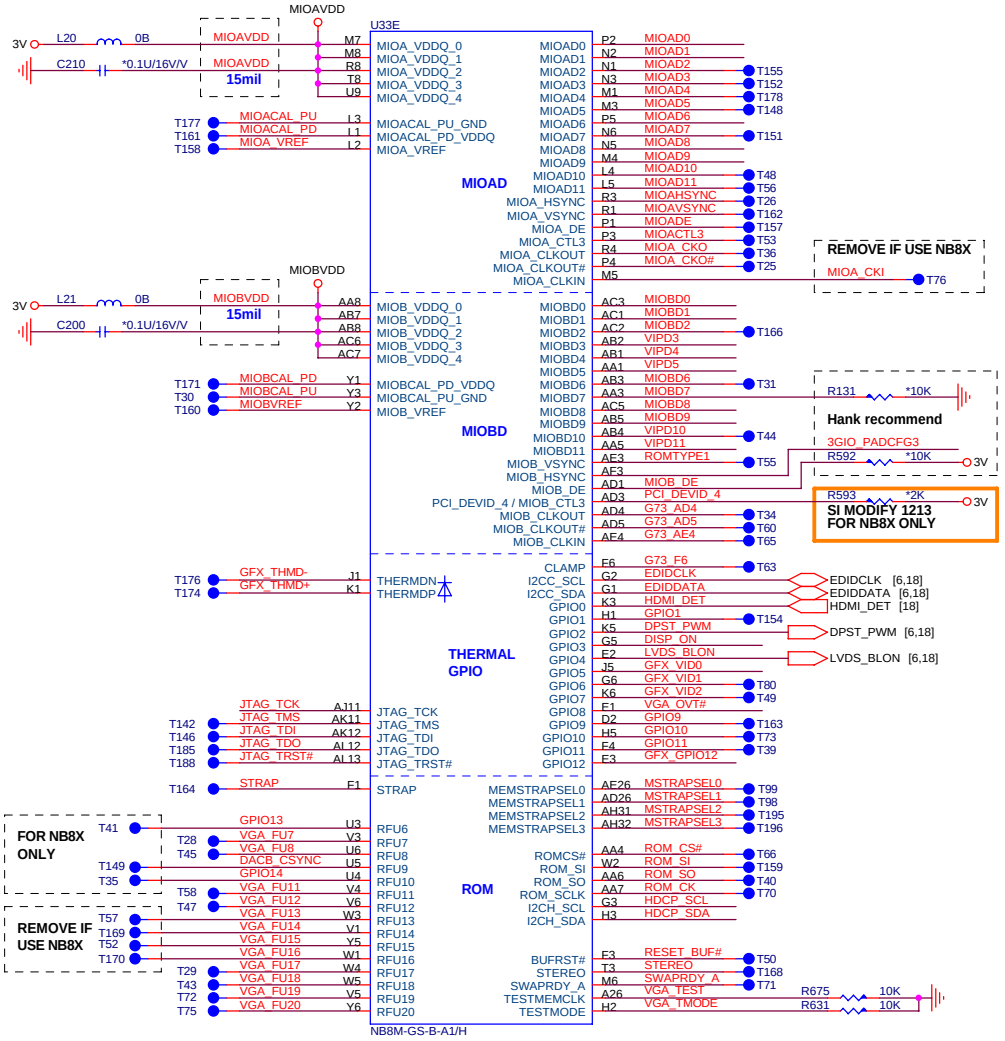
1.2V [10,11,12,15,36]
1.8V [11,15,16,17,32,37]
2.5V [2,32,36]
3V [2,5,6,7,8,9,10,11,12,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
5V [18,19,22,23,25,26,27,28,29,31,32,33,36,38]

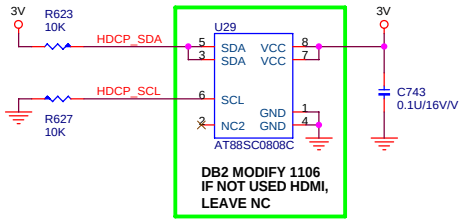
NB5/RD2/HW1

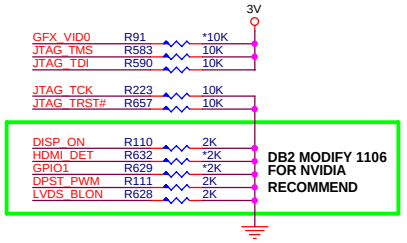
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M (LVDS,CRT,TV,HDMI)	C2A

Date: Wednesday, December 20, 2006 Sheet 13 of 40

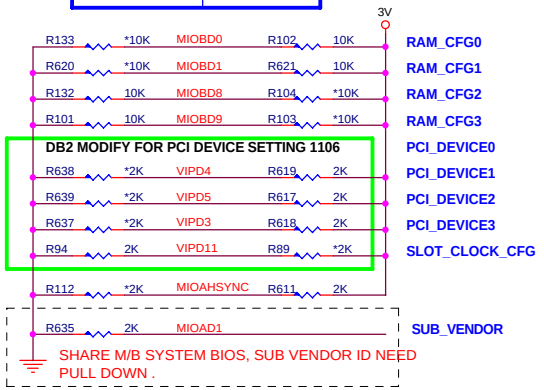


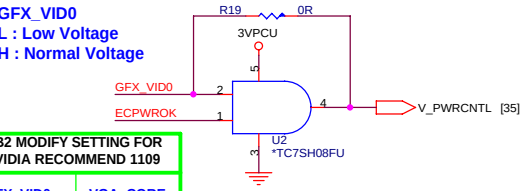




PCI DEVICE ID SETTING

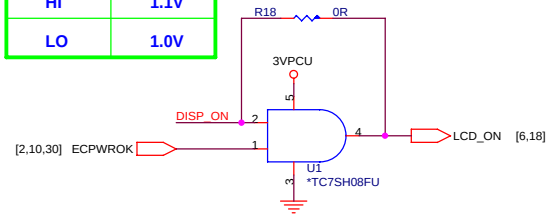
PCI_DEVICE[4:0]	DESCRIPTION
00111	NB8M
OTHERS	RESERVED





DB2 MODIFY SETTING FOR NVIDIA RECOMMEND 1109

GFX_VID0 (GPIO5)	VGA_CORE (NB8X)
HI	1.1V
LO	1.0V

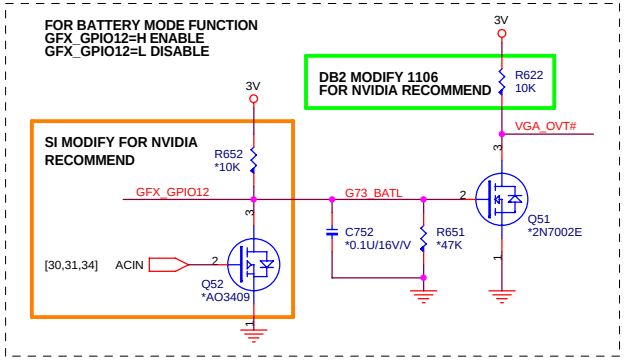


NB8X 64bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
0001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
0010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
0011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
0110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
0111	DDR2 32Mx16x4, 64bit, 256MB	Hynix
1000	DDR2 16Mx16x2, 32bit, 64MB	Elpida
1001	DDR2 16Mx16x2, 32bit, 64MB	Samsung
1010	DDR2 16Mx16x2, 32bit, 64MB	Infineon
1011	DDR2 16Mx16x2, 32bit, 64MB	Hynix
others	Reserved	

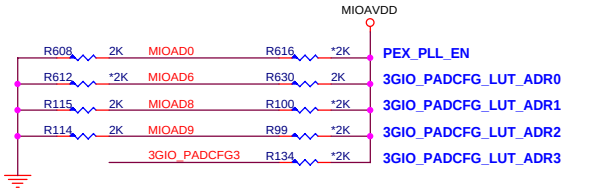
NB8X 128bit VRAM Configuration Table

RAM_CFG[3:0]	DESCRIPTION	Vendor
0000	DDR2 16Mx16x8, 128bit, 256MB	Elpida
0001	DDR2 16Mx16x8, 128bit, 256MB	Samsung
0010	DDR2 16Mx16x8, 128bit, 256MB	Infineon
0011	DDR2 16Mx16x8, 128bit, 256MB	Hynix
0100	Reserved	
0101	DDR2 32Mx16x8, 128bit, 512MB	Samsung
0110	DDR2 32Mx16x8, 128bit, 512MB	Infineon
0111	DDR2 32Mx16x8, 128bit, 512MB	Hynix
1000	DDR2 16Mx16x4, 64bit, 128MB	Elpida
1001	DDR2 16Mx16x4, 64bit, 128MB	Samsung
1010	DDR2 16Mx16x4, 64bit, 128MB	Infineon
1011	DDR2 16Mx16x4, 64bit, 128MB	Hynix
1100	Reserved	
1101	DDR2 32Mx16x4, 64bit, 256MB	Samsung
1110	DDR2 32Mx16x4, 64bit, 256MB	Infineon
1111	DDR2 32Mx16x4, 64bit, 256MB	Hynix



3GIO_PADCFG STRAP

3GIO_PDACFG[3:0]	DESCRIPTION
0000	DESKTOP
0001	MOBILE
OTHERS	RESERVED



3V [2,5,6,7,8,9,10,11,12,13,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]
3VPCU [9,18,28,29,30,31,33,34,35]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NV_NB8M (ROM,GPIO,STRAP)	C2A

Date: Wednesday, December 20, 2006 Sheet 14 of 40

Channel C is available for 128bit only

U33B

VMA_DQ0 N27 … VMA_DQ63 AE28 — FBAD0 … FBAD63 — FBA

VMA_DM0 M29, VMA_DM1 M30, VMA_DM2 G30, VMA_DM3 F29, VMA_DM4 AA29, VMA_DM5 AK30, VMA_DM6 AC30, VMA_DM7 AG30 — FBADQM0 … FBADQM7

VMA_WDQS0 L28, VMA_WDQS1 K31, VMA_WDQS2 G32, VMA_WDQS3 G28, VMA_WDQS4 AB28, VMA_WDQS5 AL32, VMA_WDQS6 AE32, VMA_WDQS7 AH30 — FBADQS_WP0 … FBADQS_WP7

VMA_RDQS0 M28, VMA_RDQS1 K32, VMA_RDQS2 G31, VMA_RDQS3 G27, VMA_RDQS4 AA28, VMA_RDQS5 AL31, VMA_RDQS6 AE31, VMA_RDQS7 AH29 — FBADQS_RN0 … FBADQS_RN7

FBVDD_0 … FBVDD_19 — A12, A15, A18, A21, A24, A27, A3, A30, A6, A9, AA32, AD32, AG32, AK32, C32, F32, J32, M32, R32, V32 — 1.8V

C420 … C356: 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.47UA/10V/X, 0.47UA/10V/X, 0.47UA/10V/X, 0.47UA/10V/X, 10UA/6.3V/R, 10UA/6.3V/R

PLACE NEAR GPU

FBVDDQ_0 … FBVDDQ_23 — AA25, AA26, AB25, AB26, G11, G12, G15, G18, G21, G22, H11, H12, H15, H18, H21, H22, L25, L26, M25, M26, R25, R26, V25, V26 — 1.8V

C343 … C812: 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.1U/16V/V, 0.47UA/10V/X, 0.47UA/10V/X, 0.47UA/10V/X, 0.47UA/10V/X, 10UA/6.3V/R, 10UA/6.3V/R

PLACE NEAR GPU

FBA_CMD0 … FBA_CMD26 — P32, U27, P31, U30, Y31, W32, W31, T32, V27, T28, T31, U32, W29, W30, T27, V28, V30, U31, R27, V29, T30, W28, R29, R30, P29, U28, Y32

VMA_MA3 [16] … VMA_MA13 [16] — T196 (VMA_BA2), T193 (VMA_CAS#)

FBA_CLK0 … FBA_CLK1# — P28, R28, Y27, AA27 — VMA_CLK0 [16], VMA_CLK0# [16], VMA_CLK1 [16], VMA_CLK1# [16]

RFU2 — FBA_CMD27 — T194 — RESERVED FOR NB8X

RFU3 — Y30, AC26 — G73_AC26 — T96

FBA_DEBUG — AC27 — VMA_DEBUG — T97

FBA_REFCLK, FBA_REFCLK# — D32, D31 — VMA_REFCK — T199, VMA_REFCK# — T197 — REMOVE IF USE NB8X

FBA_PLLVDD/H_PLLVDD — G23 — L32 220A/0.2A; C377 0.1U/16V/V; C378 4.7UA/6.3V/R; 1.2V — DB2 MODIFY 1024 STUFF FOR NB8X

FBA_PLLAVDD — G25 — FBA_PLLAVDD — 15mil — L40 33A/3A — 1.2V

FBA_PLLGND — G24 — C389 470P/50V/X; C391 4700P/25V/X; C406 4.7UA/6.3V/R; C370 0.1U/16V/V — For EMI

VREF=FBVDDQ*Rbot/(Rtop+Rbot)

1.8V — R682 1K — FB_VREF1 — 15mil — E32 — FB_VREF1

DB2 MODIFY 1103 STUFF FOR NB8X — R680 1K; C825 0.1U/16V/V

NB8M-GS-B-A1/H

U33C

VMC_DQ0 B7 … VMC_DQ63 E19 — FBCD0 … FBCD63 — FBC

VMC_DM0 A4, VMC_DM1 F11, VMC_DM2 F5, VMC_DM3 C9, VMC_DM4 C28, VMC_DM5 F24, VMC_DM6 C24, VMC_DM7 E20 — FBCDQM0 … FBCDQM7

VMC_WDQS0 C5, VMC_WDQS1 E10, VMC_WDQS2 E5, VMC_WDQS3 B8, VMC_WDQS4 A29, VMC_WDQS5 D25, VMC_WDQS6 B25, VMC_WDQS7 E20 — FBCDQS_WP0 … FBCDQS_WP7

VMC_RDQS0 C6, VMC_RDQS1 F9, VMC_RDQS2 E6, VMC_RDQS3 A8, VMC_RDQS4 B29, VMC_RDQS5 E25, VMC_RDQS6 A25, VMC_RDQS7 F21 — FBCDQS_RN0 … FBCDQS_RN7

FBVTT_0 … FBVTT_17 — AA23, AB23, H16, H17, J10, J23, J24, J9, K11, K12, K21, K22, K24, K9, L23, M23, T25, U25 — 1.8V

C344 … C327: 0.1U/16V/V, 1U/6.3V/R, 0.1U/16V/V, 0.1U/16V/V, 0.47UA/10V/X, 0.47UA/10V/X, 10UA/6.3V/R, 0.1U/16V/V, 0.1U/16V/V, 0.47UA/10V/X, 0.47UA/10V/X, 10UA/6.3V/R

PLACE NEAR GPU

FBC_CMD0 … FBC_CMD26 — C13, A16, A13, B17, B20, A19, B19, B14, E16, A14, C15, B16, E17, C19, D15, C17, A17, C16, D14, F16, C14, C18, E14, B13, E15, F15, A20

VMC_MA3 … VMC_BA2 — T92

VMC_CS0# … VMC_CAS# — VMC_MA13 — T192

FBC_CLK0, FBC_CLK0#, FBC_CLK1, FBC_CLK1# — E13, E13, F18, E17 — VMC_CLK0, VMC_CLK0#, VMC_CLK1, VMC_CLK1#

RFU4 — C20 — FBC_CMD27 — T191

RFU5 — D1 — G73_D1 — T153

FBC_DEBUG — F12 — VMC_DEBUG — T90

FBC_REFCLK, FBC_REFCLK# — B1, C1 — VMC_REFCK, VMC_REFCK# — R610 *0R I2CS_SDA R609 *2.2K; R605 *0R I2CS_SCL R604 *2.2K; 3V — T83 (G73_G8)

RESERVED FOR NB8X

FBC_PLLVDD — G8

FBC_PLLAVDD — G10

FBC_PLLGND — G9

15mil — FBC_PLLAVDD — L27 *33A/3A — 1.2V

C221 *470P/50V/X; C251 *4700P/25V/X; C262 *4.7UA/6.3V/R

DB2 MODIFY 1103 IF NOT USED C PORT DDR2, FB_PLLAVDD LEAVE NC

FBCAL_PD_VDDQ — K26 — FBCAL_PD — R242 40.2A/F — 1.8V

FBCAL_PU_GND — H26 — FBCAL_PU — R243 40.2/F

FBCAL_TERM_GND — J26 — FBCAL_TERM — R241 *40.2/F

SI MODIFY FOR NVIDIA RECOMMEND 1220

15mil — FB_VREF2 — A28 — R677 *1K — 1.8V

C811 *0.1U/16V/V; R676 *1K

IF NOT USED C PORT DDR2, FB_VREF2 LEAVE NC

NB8M-GS-B-A1/H

VMA_RST# — R678 0R — VMA_ODT — VMA_ODT [16]

R679 10K

VMC_RST# — R226 *0R — VMC_ODT — VMC_ODT [17]

Ra

R225 *10K

Rb

DB2 MODIFY 1103 IF NOT USED C PORT DDR2, Ra,Rb LEAVE NC

MBDATA [2,29,30,31,34] — R820 *0R — Q71 *RHU002N06 — 3V — I2CS_SDA

MBCLK [2,29,30,31,34] — R821 *0R — Q72 *RHU002N06 — 3V — I2CS_SCL

SI MODIFY FOR NVIDIA RECOMMEND 1212

[16] VMA_DQ[63..0]
[16] VMA_DM[7..0]
[16] VMA_WDQS[7..0]
[16] VMA_RDQS[7..0]

[17] VMC_DQ[63..0]
[17] VMC_DM[7..0]
[17] VMC_WDQS[7..0]
[17] VMC_RDQS[7..0]

1.2V
1.8V
3V

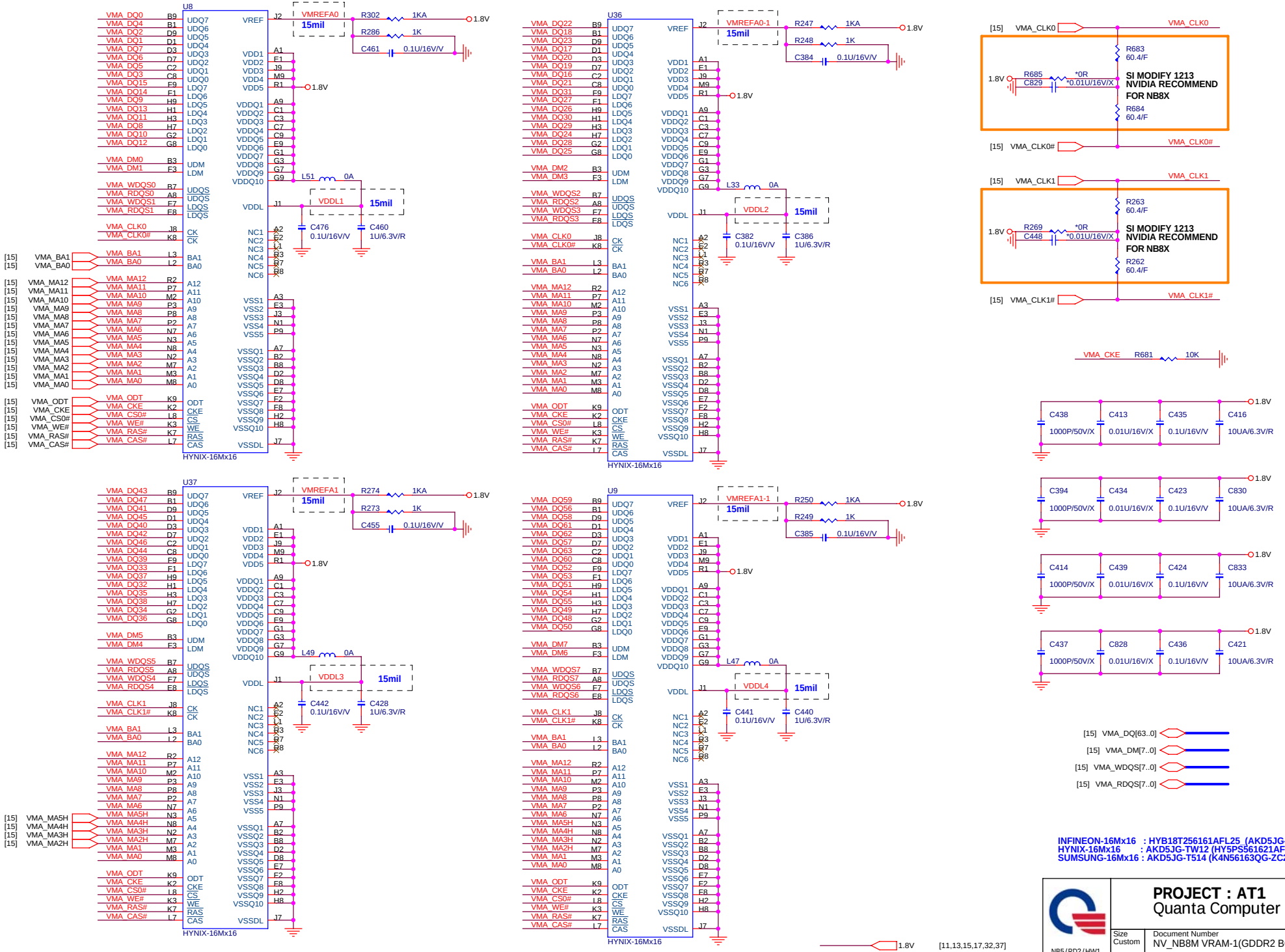
[10,11,12,13,36]
[11,13,16,17,32,37]
[2,5,6,7,8,9,10,11,12,13,14,18,19,21,22,23,26,27,28,29,30,31,32,33,36,38]

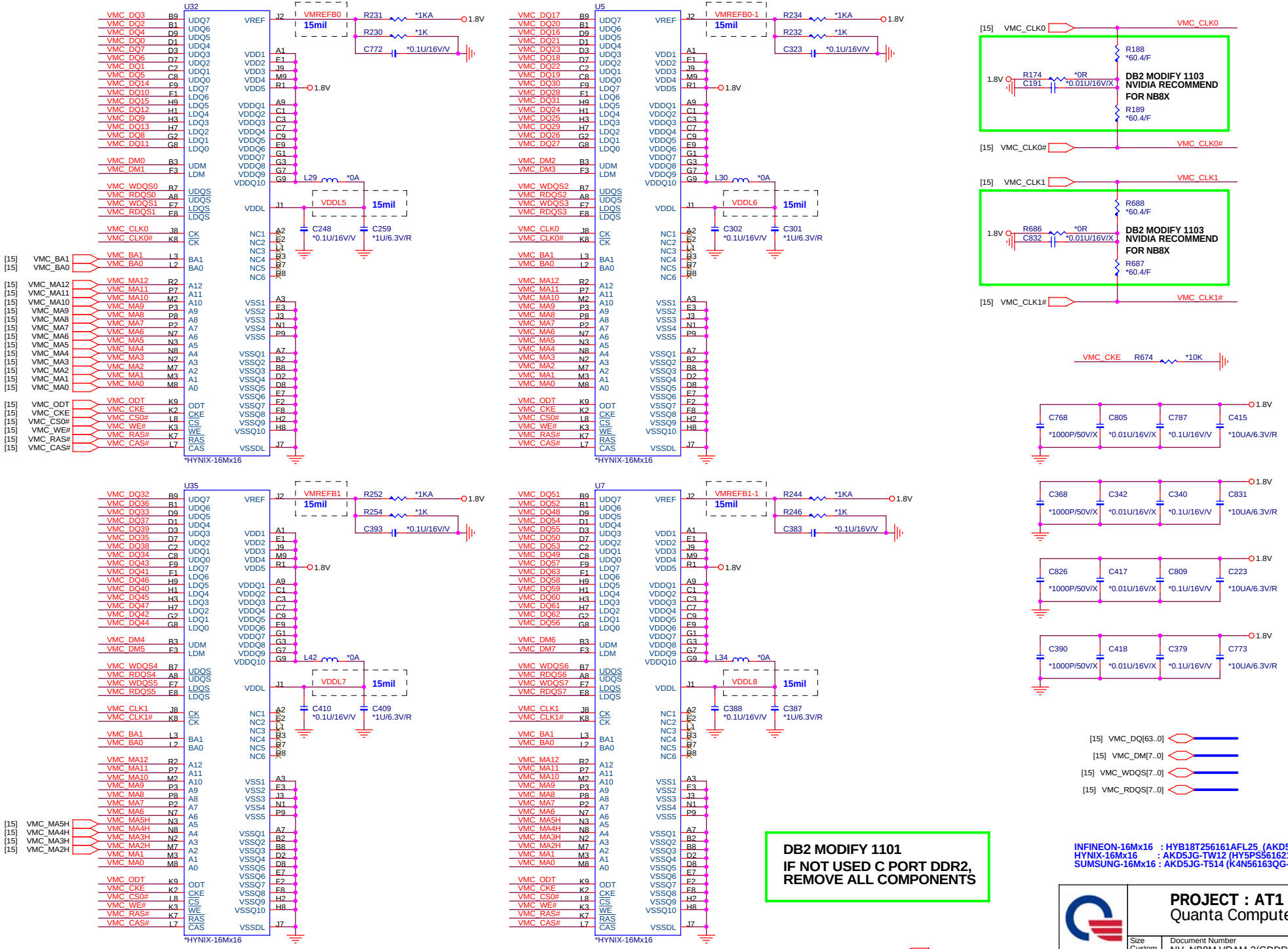
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

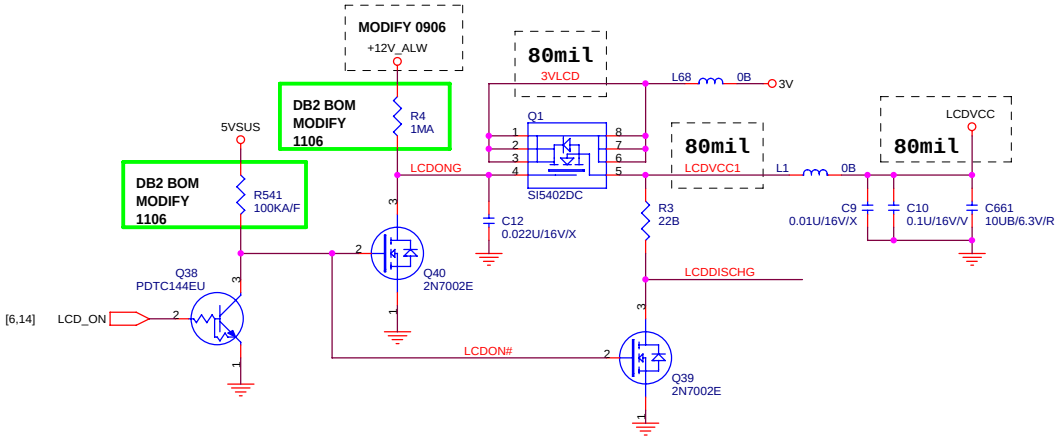
Size	Document Number	Rev
Custom	NV_NB8M (MEM_I/F)	C2A

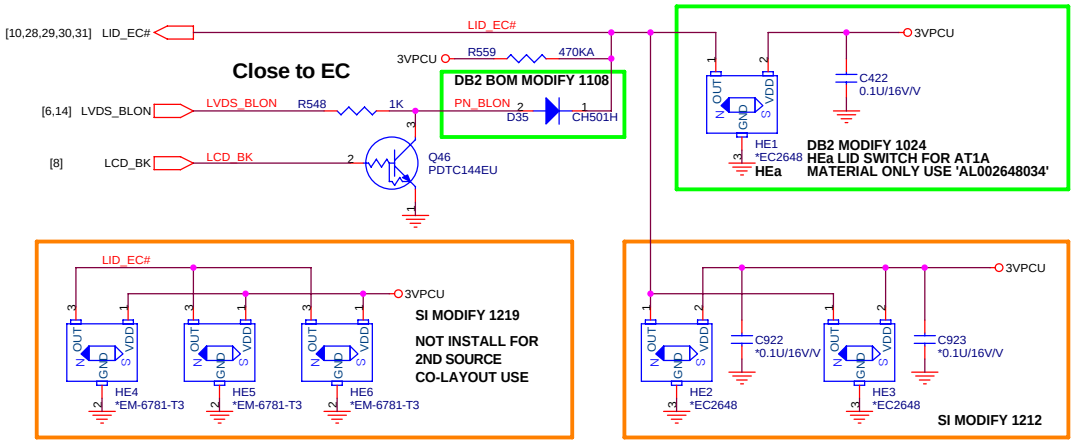
Date: Wednesday, December 20, 2006 Sheet 15 of 40

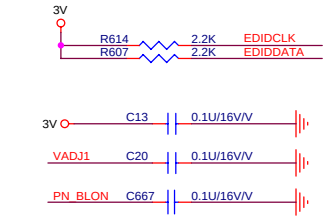

U8
U36
U37
U9
HYNIX-16Mx16
VREF
VMREFA0
VMREFA0-1
VMREFA1
VMREFA1-1
15mil
R302 1KA
R286 1K
C461 0.1U/16V/V
R247 1KA
R248 1K
C384 0.1U/16V/V
R274 1KA
R273 1K
C455 0.1U/16V/V
R250 1KA
R249 1K
C385 0.1U/16V/V
1.8V
VDD1
VDD2
VDD3
VDD4
VDD5
VDDQ1
VDDQ2
VDDQ3
VDDQ4
VDDQ5
VDDQ6
VDDQ7
VDDQ8
VDDQ9
VDDQ10
VDDL
VDDL1
VDDL2
VDDL3
VDDL4
L51 0A
L33 0A
L49 0A
L47 0A
C476 0.1U/16V/V
C460 1U/6.3V/R
C382 0.1U/16V/V
C386 1U/6.3V/R
C442 0.1U/16V/V
C428 1U/6.3V/R
C441 0.1U/16V/V
C440 1U/6.3V/R
VSS1
VSS2
VSS3
VSS4
VSS5
VSSQ1
VSSQ2
VSSQ3
VSSQ4
VSSQ5
VSSQ6
VSSQ7
VSSQ8
VSSQ9
VSSQ10
VSSDL
NC1
NC2
NC3
NC4
NC5
NC6
CK
CKE
CS
WE
RAS
CAS
ODT
BA0
BA1
UDM
LDM
UDQS
LDQS
UDQ7
LDQ7
[15] VMA_CLK0
VMA_CLK0
R683 60.4/F
R685 *0R
C829 *0.01U/16V/X
SI MODIFY 1213
NVIDIA RECOMMEND
FOR NB8X
R684 60.4/F
[15] VMA_CLK0#
VMA_CLK0#
[15] VMA_CLK1
VMA_CLK1
R263 60.4/F
R269 *0R
C448 *0.01U/16V/X
R262 60.4/F
[15] VMA_CLK1#
VMA_CLK1#
VMA_CKE R681 10K
C438 1000P/50V/X
C413 0.01U/16V/X
C435 0.1U/16V/V
C416 10UA/6.3V/R
C394 1000P/50V/X
C434 0.01U/16V/X
C423 0.1U/16V/V
C830 10UA/6.3V/R
C414 1000P/50V/X
C439 0.01U/16V/X
C424 0.1U/16V/V
C833 10UA/6.3V/R
C437 1000P/50V/X
C828 0.01U/16V/X
C436 0.1U/16V/V
C421 10UA/6.3V/R
[15] VMA_DQ[63..0]
[15] VMA_DM[7..0]
[15] VMA_WDQS[7..0]
[15] VMA_RDQS[7..0]
[15] VMA_BA1
[15] VMA_BA0
[15] VMA_MA12
[15] VMA_MA11
[15] VMA_MA10
[15] VMA_MA9
[15] VMA_MA8
[15] VMA_MA7
[15] VMA_MA6
[15] VMA_MA5
[15] VMA_MA4
[15] VMA_MA3
[15] VMA_MA2
[15] VMA_MA1
[15] VMA_MA0
[15] VMA_ODT
[15] VMA_CKE
[15] VMA_CS0#
[15] VMA_WE#
[15] VMA_RAS#
[15] VMA_CAS#
[15] VMA_MA5H
[15] VMA_MA4H
[15] VMA_MA3H
[15] VMA_MA2H
1.8V [11,13,15,17,32,37]
INFINEON-16Mx16 : HYB18T256161AFL25 (AKD5JG-T^08))
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25 1.8V)
SUMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25_1.8V)
NB5/RD2/HW1
PROJECT : AT1
Quanta Computer Inc.
Size Custom
Document Number NV_NB8M VRAM-1(GDDR2 BGA84)
Rev C2A
Date: Wednesday, December 20, 2006 Sheet 16 of 40

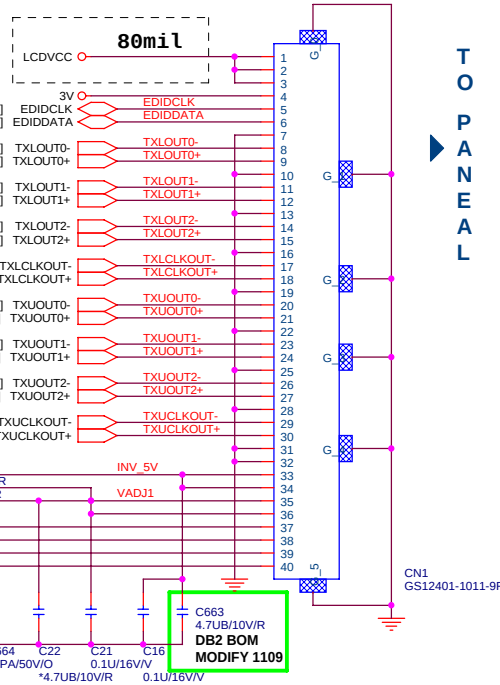

U32
U5
U35
U7
*HYNIX-16Mx16
VMREFB0
VMREFB0-1
VMREFB1
VMREFB1-1
15mil
R231 *1KA
R230 *1K
C772 *0.1U/16V/V
R234 *1KA
R232 *1K
C323 *0.1U/16V/V
R252 *1KA
R254 *1K
C393 *0.1U/16V/V
R244 *1KA
R246 *1K
C383 *0.1U/16V/V
1.8V
L29 *0A
L30 *0A
L42 *0A
L34 *0A
VDDL5
VDDL6
VDDL7
VDDL8
C248 *0.1U/16V/V
C259 *1U/6.3V/R
C302 *0.1U/16V/V
C301 *1U/6.3V/R
C410 *0.1U/16V/V
C409 *1U/6.3V/R
C388 *0.1U/16V/V
C387 *1U/6.3V/R
VMC_CLK0
VMC_CLK0#
VMC_CLK1
VMC_CLK1#
R188 *60.4/F
R189 *60.4/F
R688 *60.4/F
R687 *60.4/F
R174 *0R
C191 *0.01U/16V/X
R686 *0R
C832 *0.01U/16V/X
DB2 MODIFY 1103
NVIDIA RECOMMEND
FOR NB8X
VMC_CKE R674 *10K
C768 C805 C787 C415
C368 C342 C340 C831
C826 C417 C809 C223
C390 C418 C379 C773
*1000P/50V/X
*0.01U/16V/X
*0.1U/16V/V
*10UA/6.3V/R
[15] VMC_DQ[63..0]
[15] VMC_DM[7..0]
[15] VMC_WDQS[7..0]
[15] VMC_RDQS[7..0]
DB2 MODIFY 1101
IF NOT USED C PORT DDR2,
REMOVE ALL COMPONENTS
INFINEON-16Mx16 : HYB18T256161AFL25 (AKD5JG-T^08)
HYNIX-16Mx16 : AKD5JG-TW12 (HY5PS561621AFP-25 1.8V)
SUMSUNG-16Mx16 : AKD5JG-T514 (K4N56163QG-ZC25 1.8V)
1.8V [11,13,15,16,32,37]
PROJECT : AT1
Quanta Computer Inc.
NB5/RD2/HW1
Size Custom
Document Number NV_NB8M VRAM-2(GDDR2 BGA84)
Rev C2A
Date: Wednesday, December 20, 2006 Sheet 17 of 40

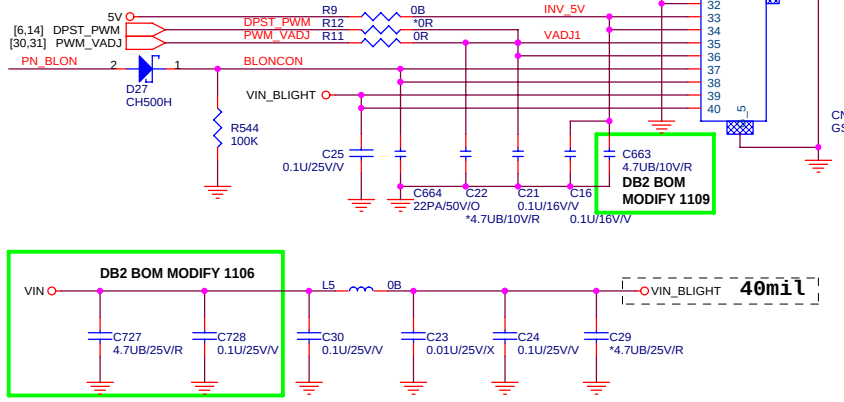
LCD CONNECTOR



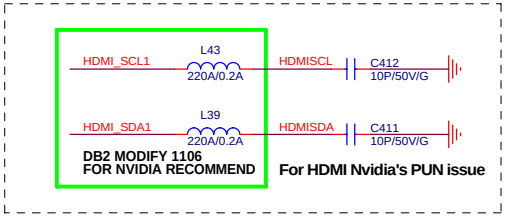


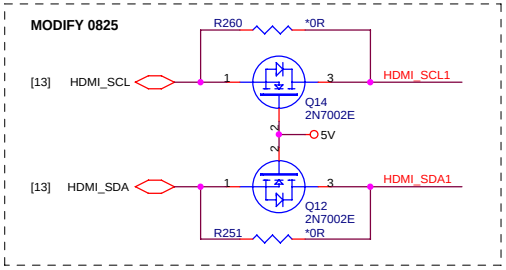


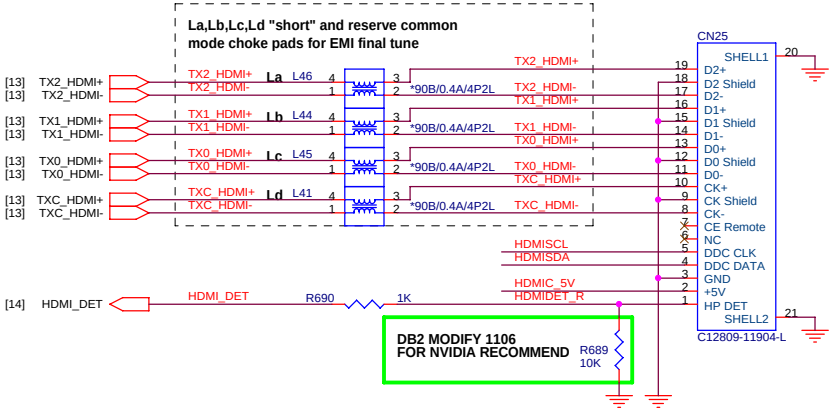


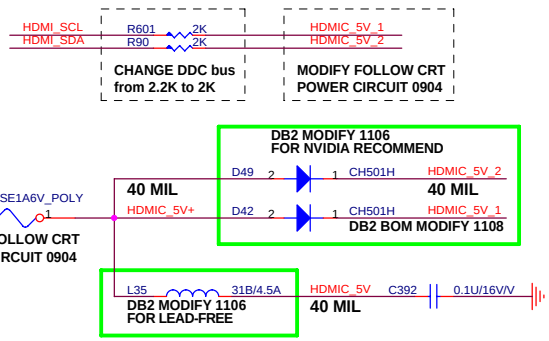


HDMI PORT









3V	[2,5,6,7,8,9,10,11,12,13,14,15,19,21,22,23,26,27,28,29,30,31,32,33,36,38]	
3VPCU	[9,14,28,29,30,31,33,34,35]	
5V	[13,19,22,23,25,26,27,28,29,31,32,33,36,38]	
5VSUS	[26,28,30,31,32,33,37]	
+12V_ALW	[10,32,33]	
VIN	[31,32,33,34,35,36,37,38]	

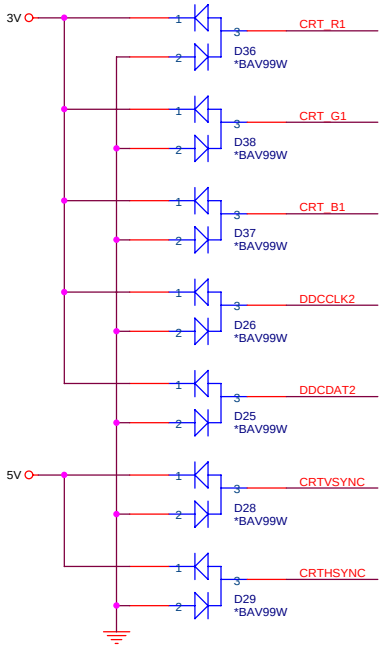
NB5/RD2/HW1

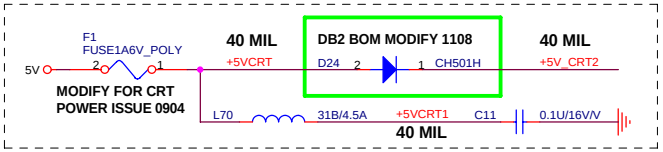
PROJECT : AT1
Quanta Computer Inc.

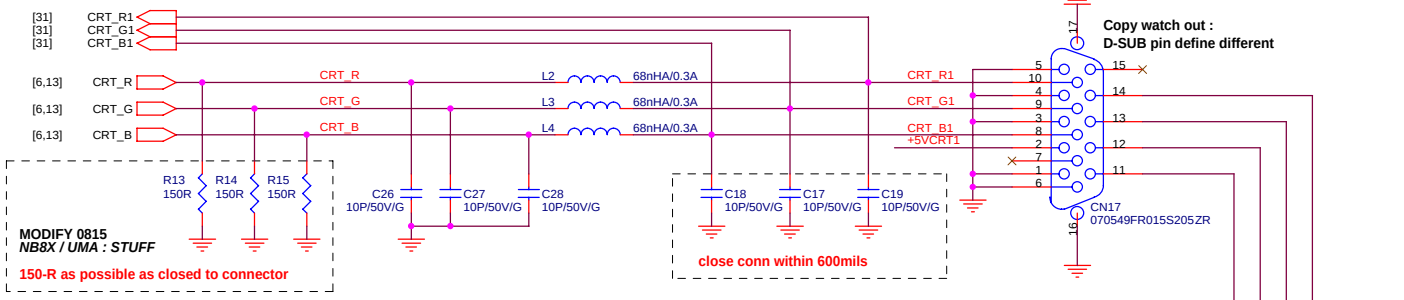
Size	Document Number	Rev
Custom	LCD,HDMI,LID_SW	C2A

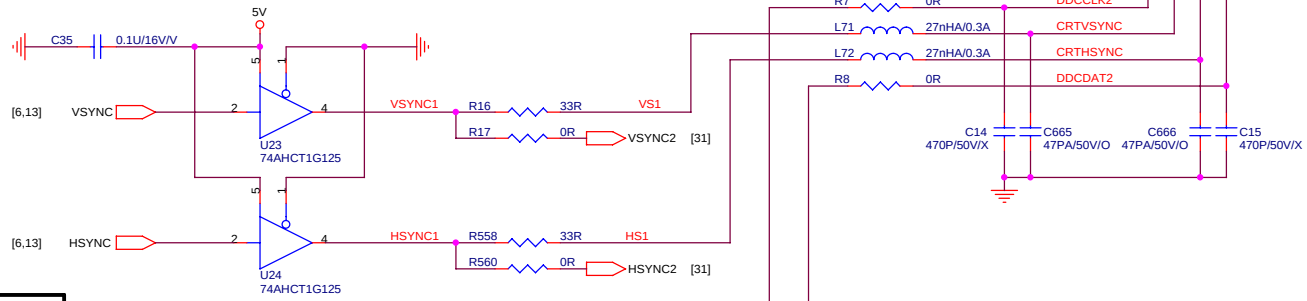
Date: Wednesday, December 20, 2006 Sheet 18 of 40

CRT PORT

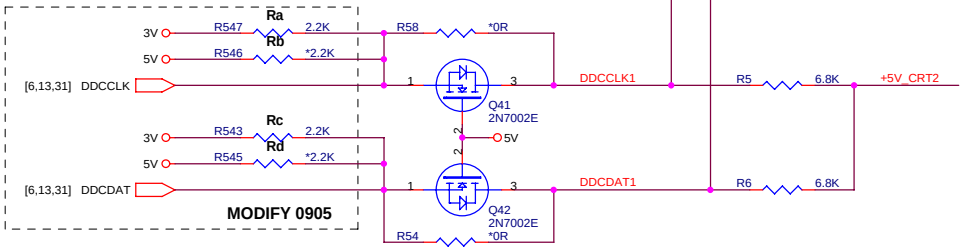






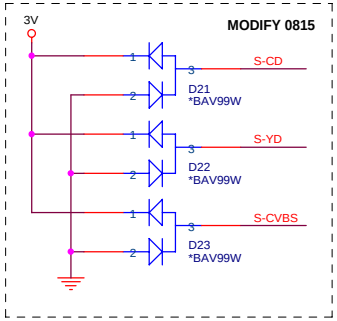


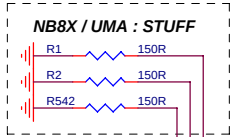
NB8X & MCP67M DIFFERENCE		
LOCATION	NB8X (DISCRETE)	MCP67M (UMA)
Ra Rb	2.2K NC	NC 2.2K
Rc Rd	2.2K NC	NC 2.2K

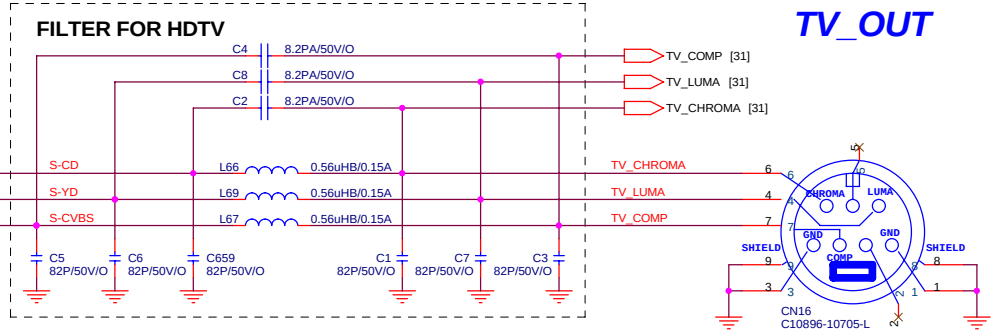


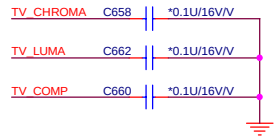
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,21,22,23,26,27,28,29,30,31,32,33,36,38]
5V [13,18,22,23,25,26,27,28,29,31,32,33,36,38]

TV_OUT







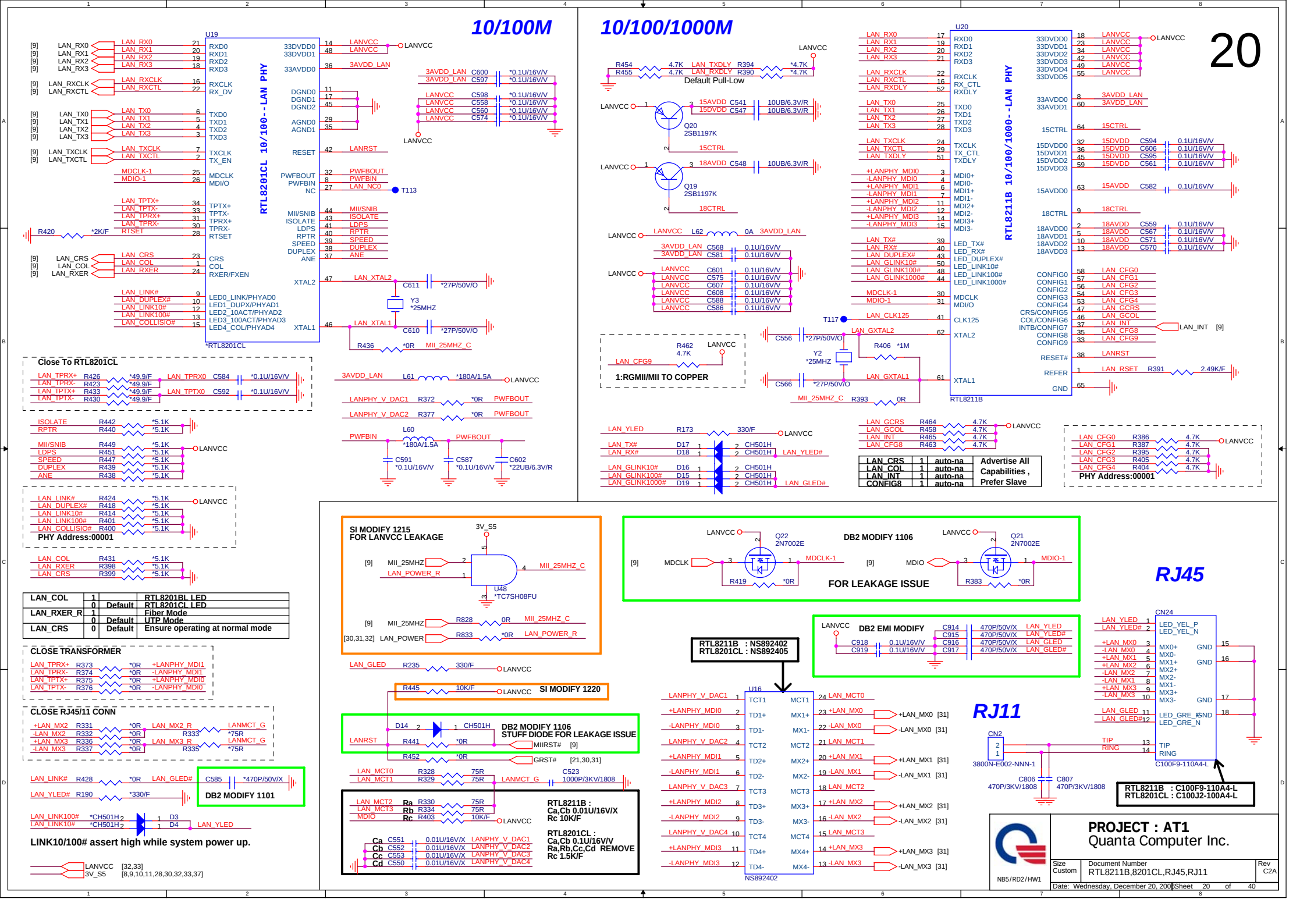


NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

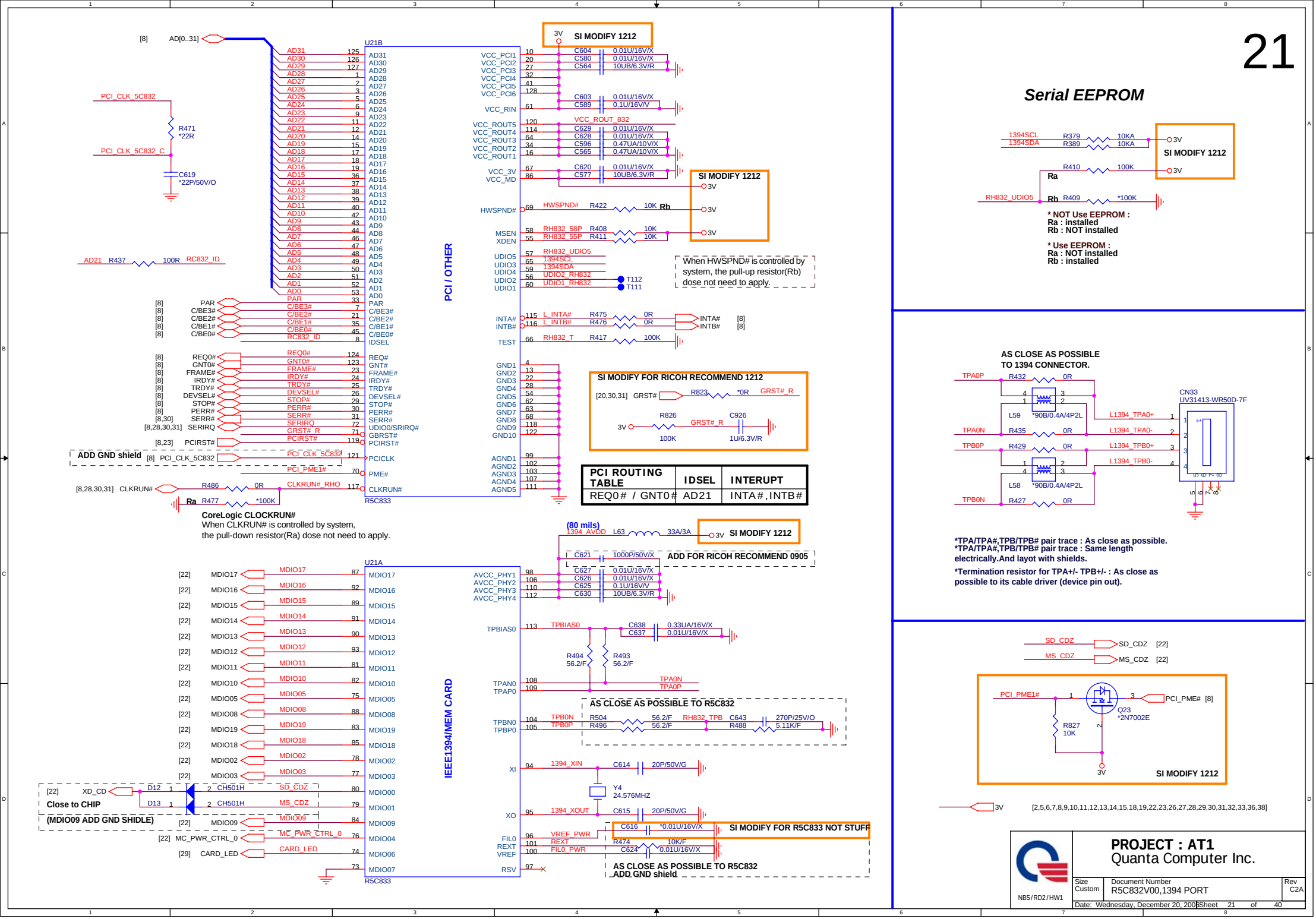
Size	Document Number	Rev
Custom	CRT,TV_OUT	C2A

Date: Wednesday, December 20, 2006 Sheet 19 of 40



LAN_COL	1		RTL8201BL LED
	0	Default	RTL8201CL LED
LAN_RXER_R	1		Fiber Mode
	0	Default	UTP Mode
LAN_CRS	0	Default	Ensure operating at normal mode

LAN_CRS	1	auto-na	Advertise All Capabilities , Prefer Slave
LAN_COL	1	auto-na	
LAN_INT	1	auto-na	
CONFIG8	1	auto-na	



Serial EEPROM

*TPA/TPA#,TPB/TPB# pair trace : As close as possible.
*TPA/TPA#,TPB/TPB# pair trace : Same length electrically.And layot with shields.

*Termination resistor for TPA+/- TPB+/- : As close as possible to its cable driver (device pin out).

3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,22,23,26,27,28,29,30,31,32,33,36,38]

PROJECT : AT1
Quanta Computer Inc.

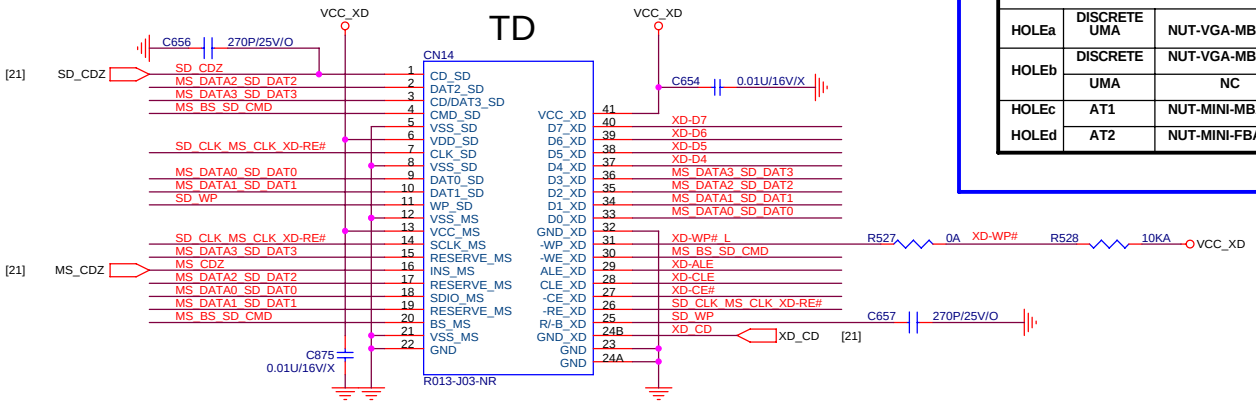
Size	Document Number	Rev
Custom	R5C832V00,1394 PORT	C2A

NB5/RD2/HW1

Date: Wednesday, December 20, 2006 Sheet 21 of 40

4 IN1 CARD READER
XD,MMC/SD,MS/MSP

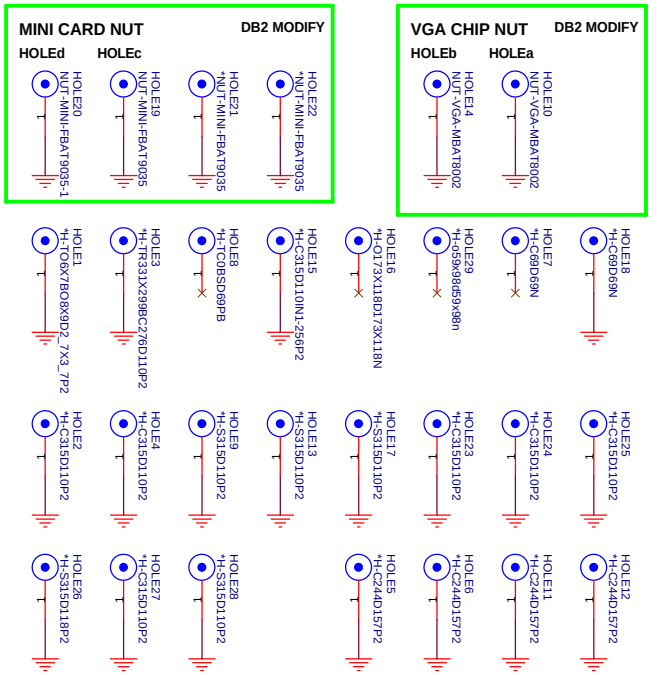
TD

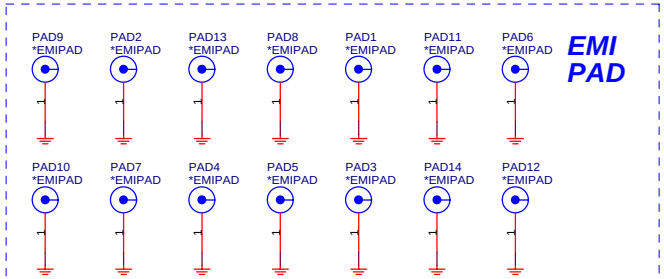


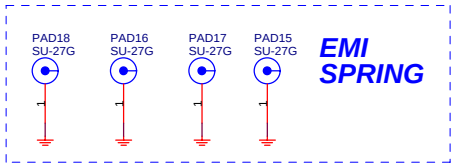
Note: Need to add WP# and CD# pad for Proconn

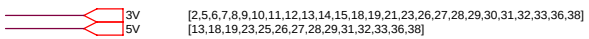
AT1 & AT2 AND DISCRETE & UMA DIFFERENCE TABLE		
HOLE	STATUS	NUT
HOLEa	DISCRETE UMA	NUT-VGA-MBAT8002
HOLEb	DISCRETE	NUT-VGA-MBAT8002
	UMA	NC
HOLEc	AT1	NUT-MINI-MBAT8004
HOLEd	AT2	NUT-MINI-FBAT9035

SCREW HOLE

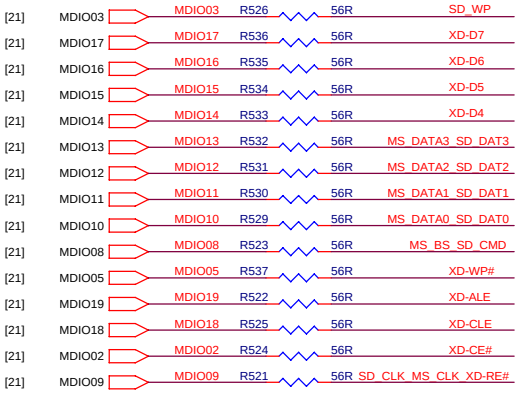


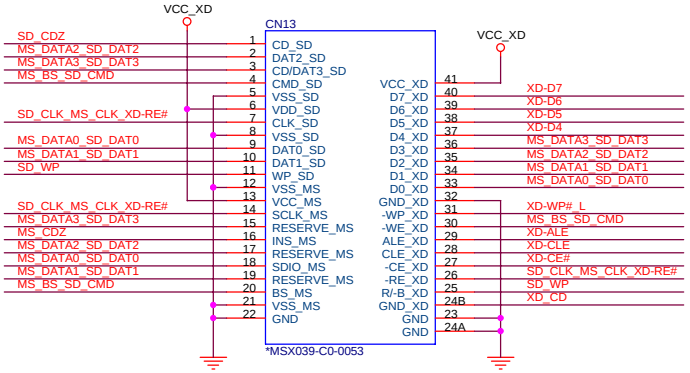




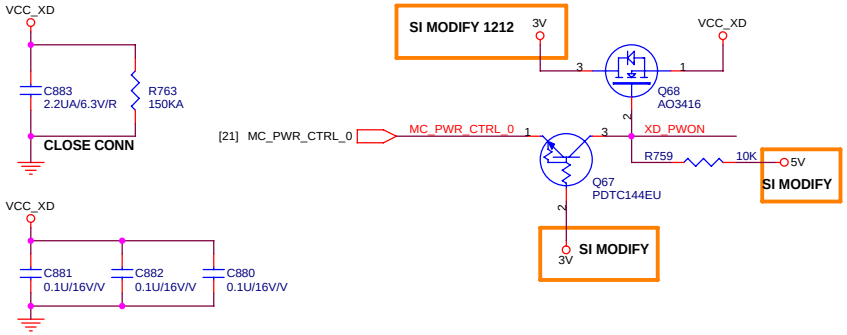


2ND SOURCE





*** NOT INSTALL FOR 2ND SOURCE CO-LAYOUT USED***



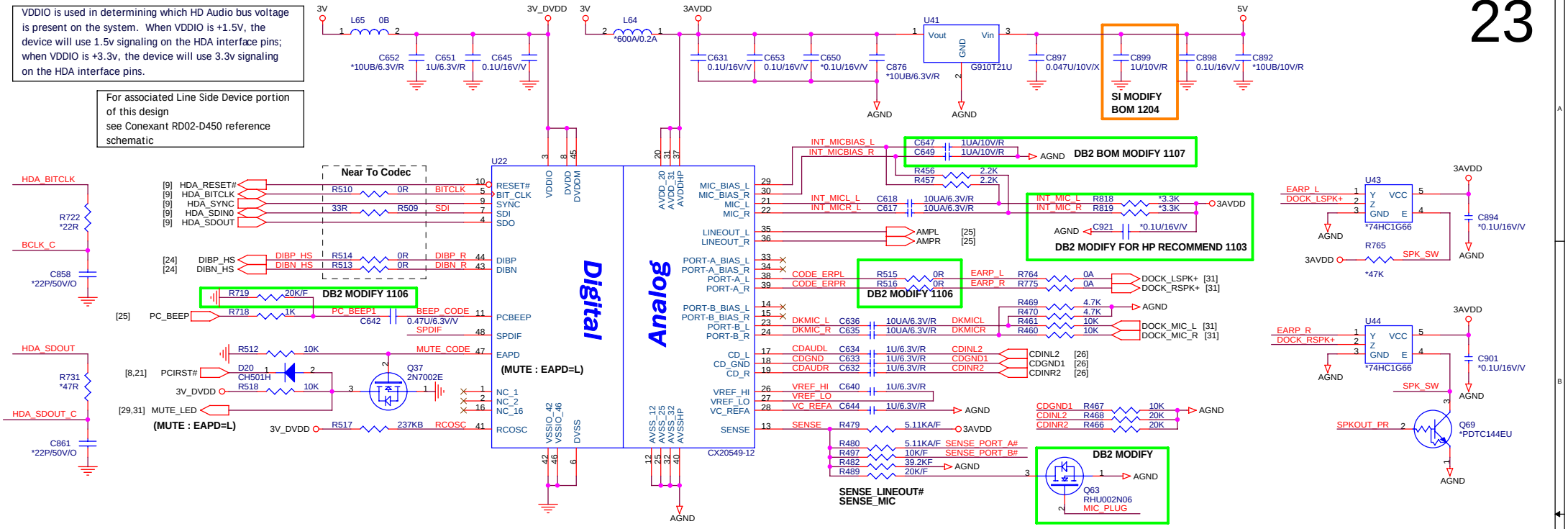
PROJECT : AT1
Quanta Computer Inc.

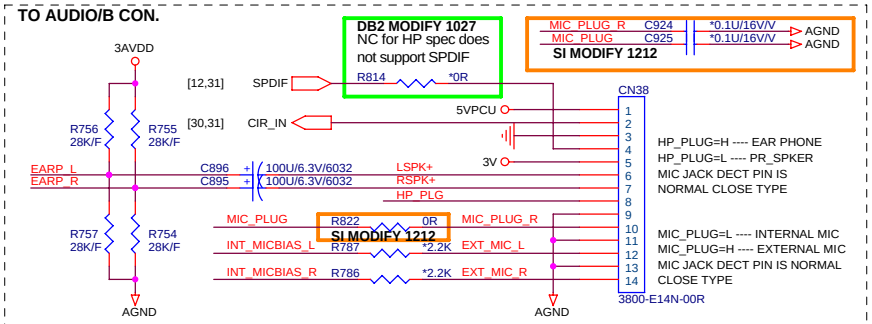
Size	Document Number	Rev
Custom	CARD_READER,HOLE,NUT,SPRING	C2A

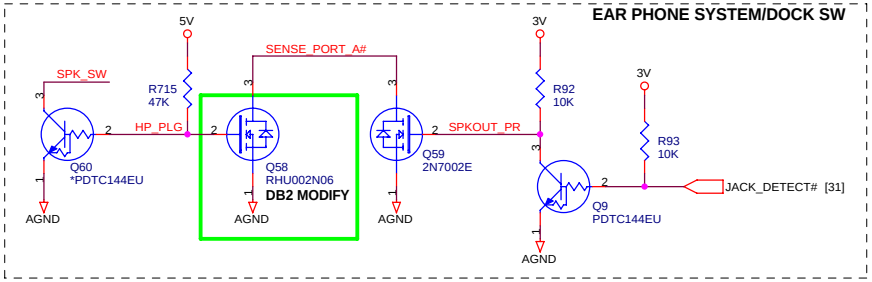
Date: Wednesday, December 20, 2006 Sheet 22 of 40

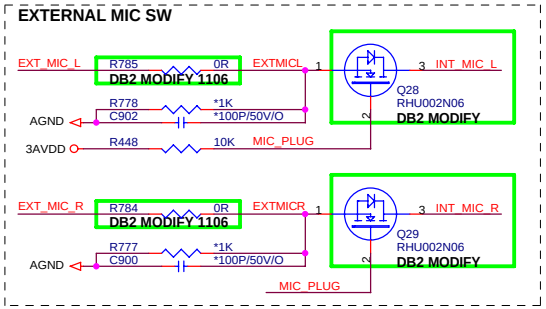
VDDIO is used in determining which HD Audio bus voltage is present on the system. When VDDIO is +1.5V, the device will use 1.5v signaling on the HDA interface pins; when VDDIO is +3.3v, the device will use 3.3v signaling on the HDA interface pins.

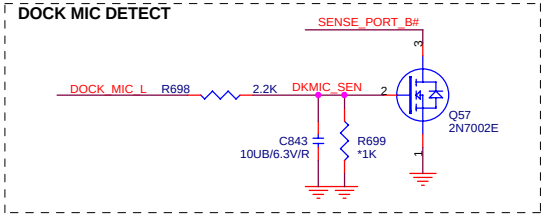
For associated Line Side Device portion of this design see Conexant RD02-D450 reference schematic

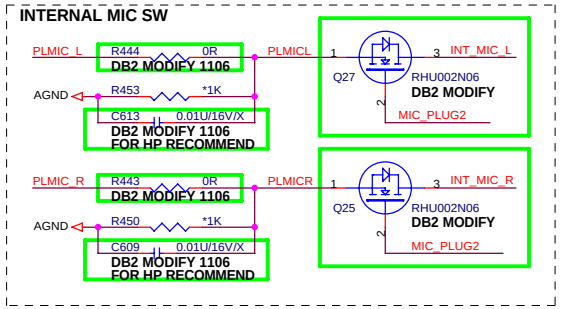


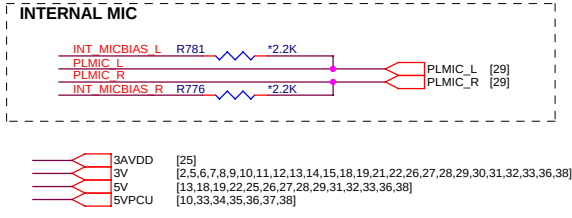






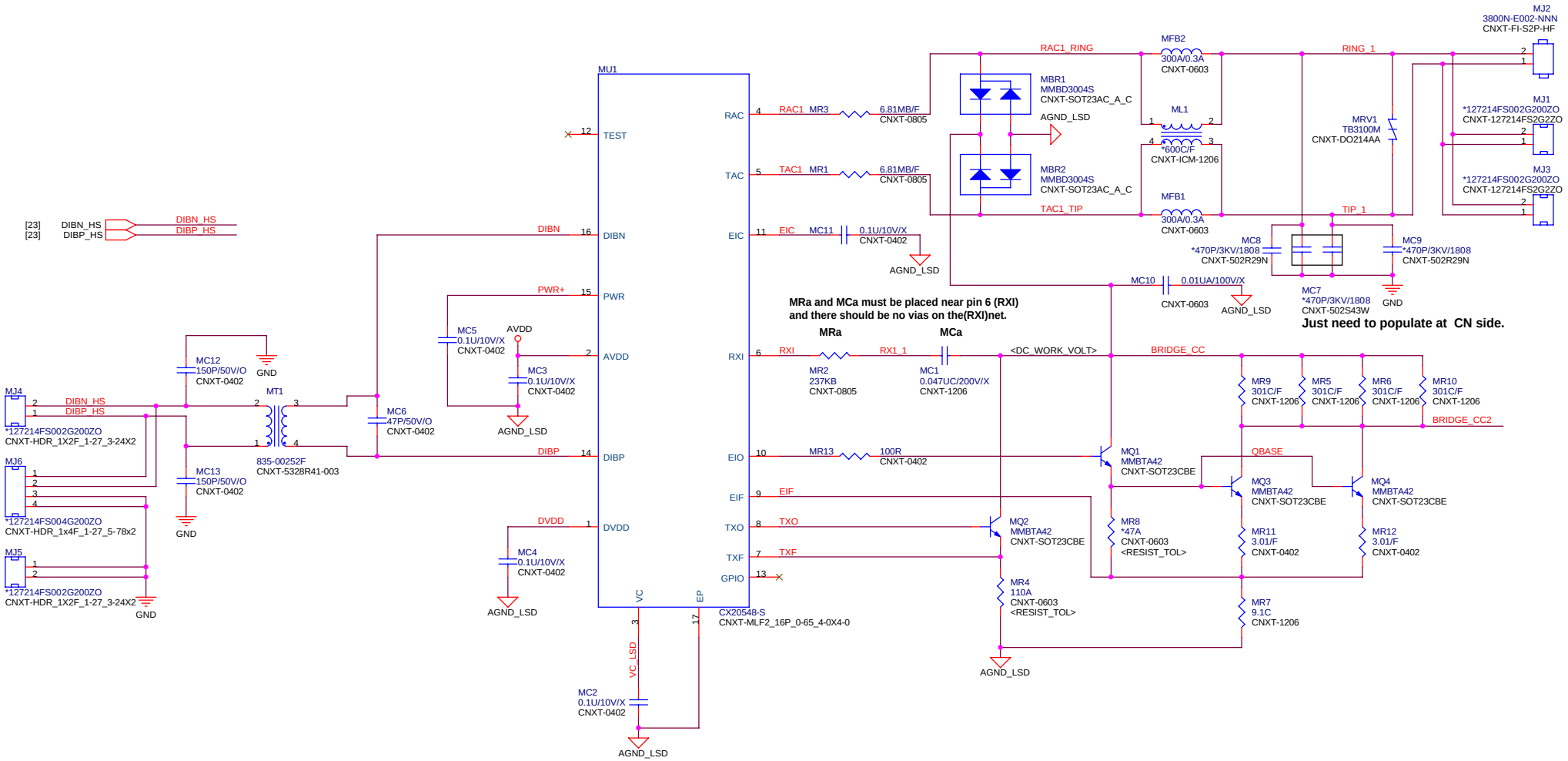






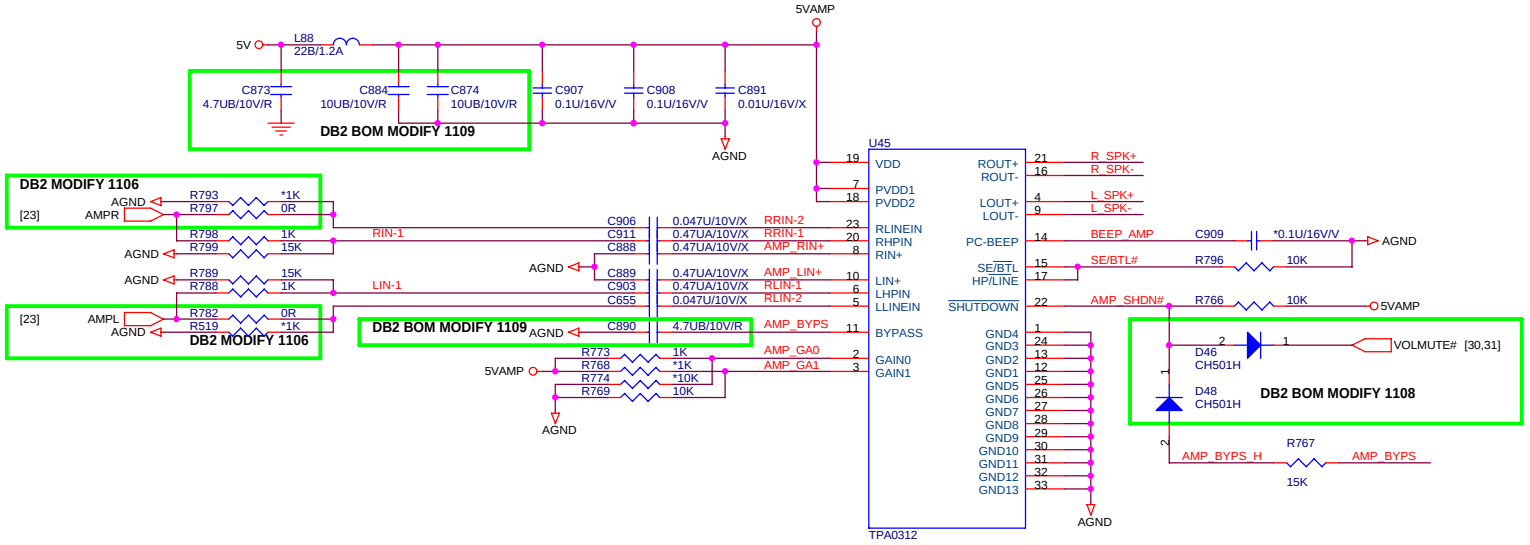
PROJECT : AT1	
Quanta Computer Inc.	
NB5/RD2/HW1	
Size: Custom	Document Number: HDA_CX20549-12,AUDIO_BOARD
Rev: C2A	
Date: Wednesday, December 20, 2006	Sheet 23 of 40

Revision History		
REV	Description	Date
0	Initial Release	April 26, 2005
4		



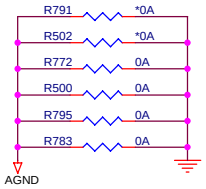
NB5/RD2/HW1	PROJECT : AT1 Quanta Computer Inc.		
	Size: Custom	Document Number: MODEM(DAA)_CX20548-S	Rev: C2A
	Date: Wednesday, December 20, 2005	Sheet 24 of 40	

AUDIO AMPLIFIER

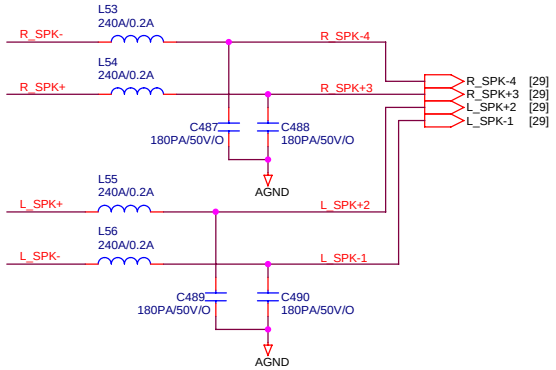


0312 Gain Table

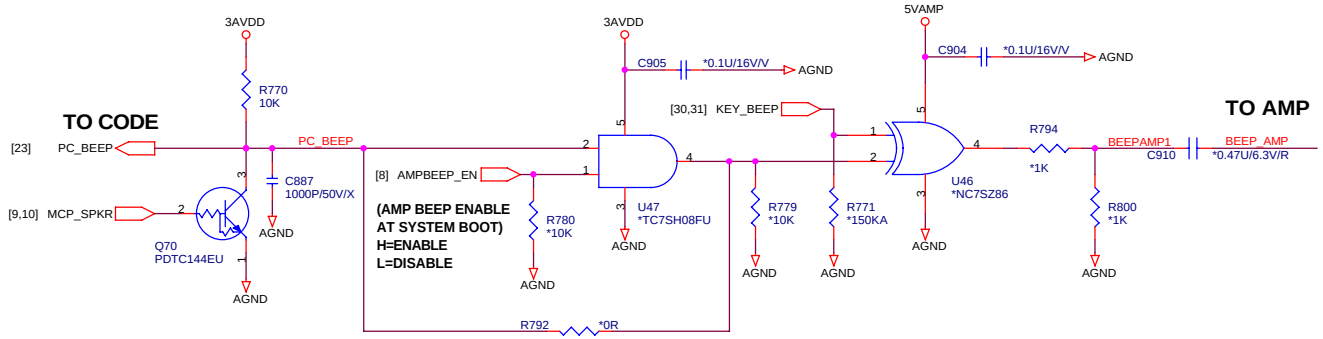
GAIN0	GAIN1	SE/BTL	AV(INV)
0	0	0	6dB
0	1	0	10dB
1	**0**	**0**	**15.6dB**
1	1	0	21.6dB
x	x	1	4.1dB



INT. SPEAKER



PCSPK BEEP



3AVDD [23]
5V [13,18,19,22,23,26,27,28,29,31,32,33,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	AMP_TPA0312	C2A

NB5/RD2/HW1

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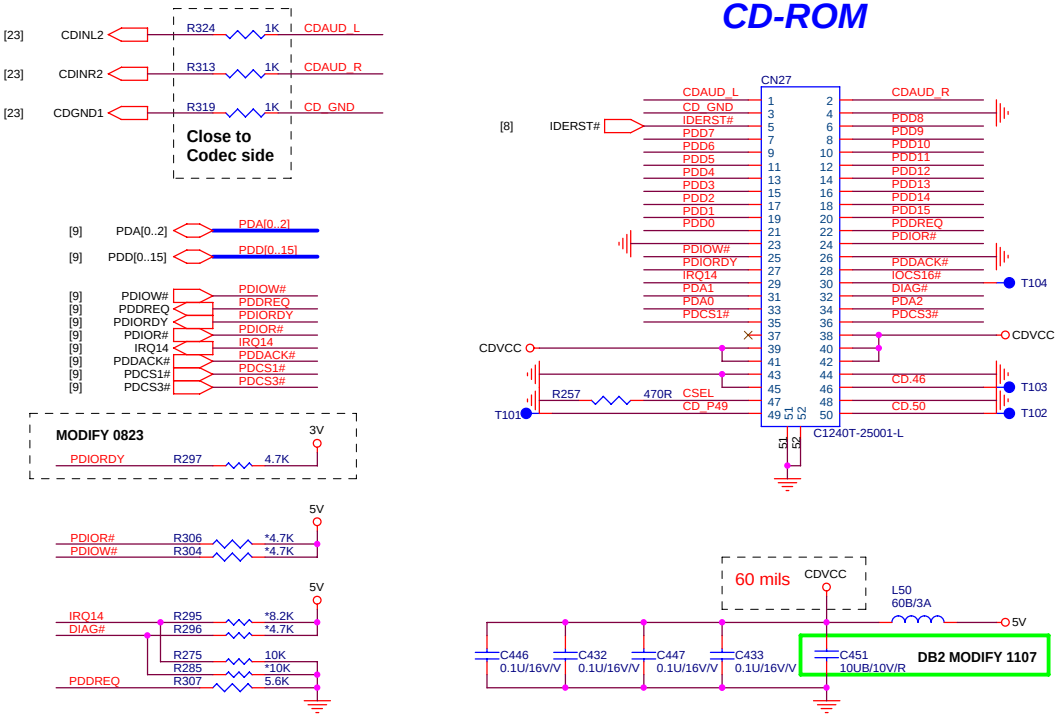
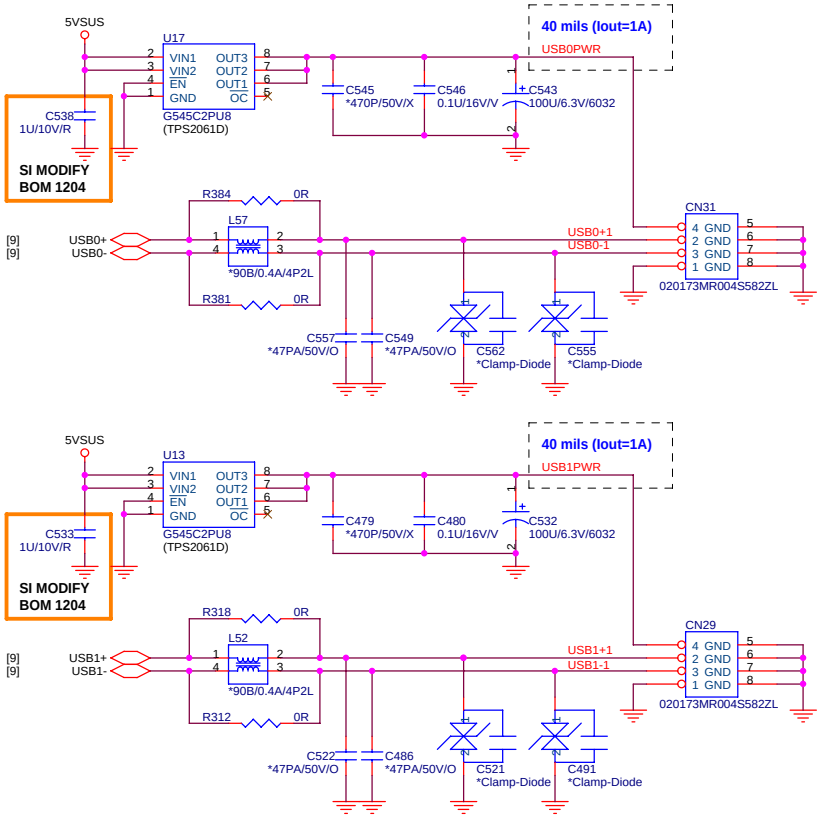
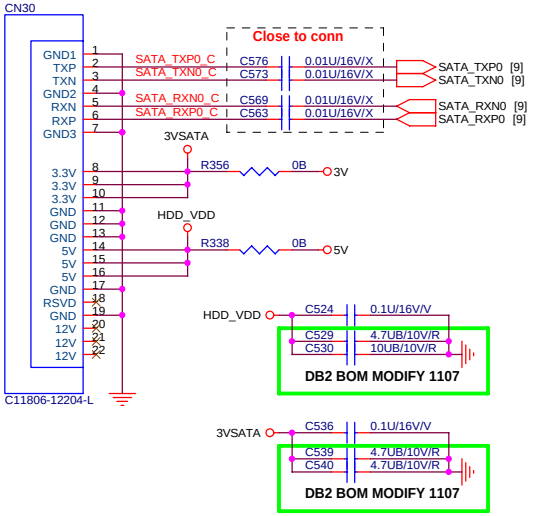
CD-ROM



USB DIP CONNECTOR X 2

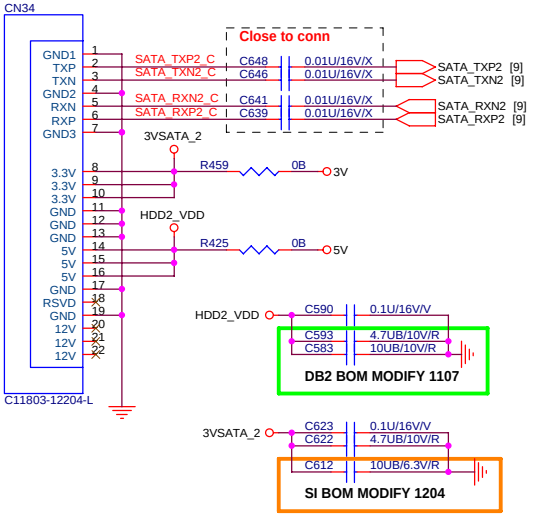


SATA_1 CONNECTOR

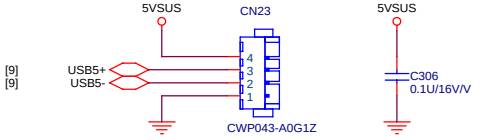


For 17"W Second HDD

SATA_2 CONNECTOR



USB WIRE TO DC BOARD X 1



3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,27,28,29,30,31,32,33,36,38]
5VSUS [18,28,30,31,32,33,37]
5V [13,18,19,22,23,25,27,28,29,31,32,33,36,38]

NB5/RD2/HW1

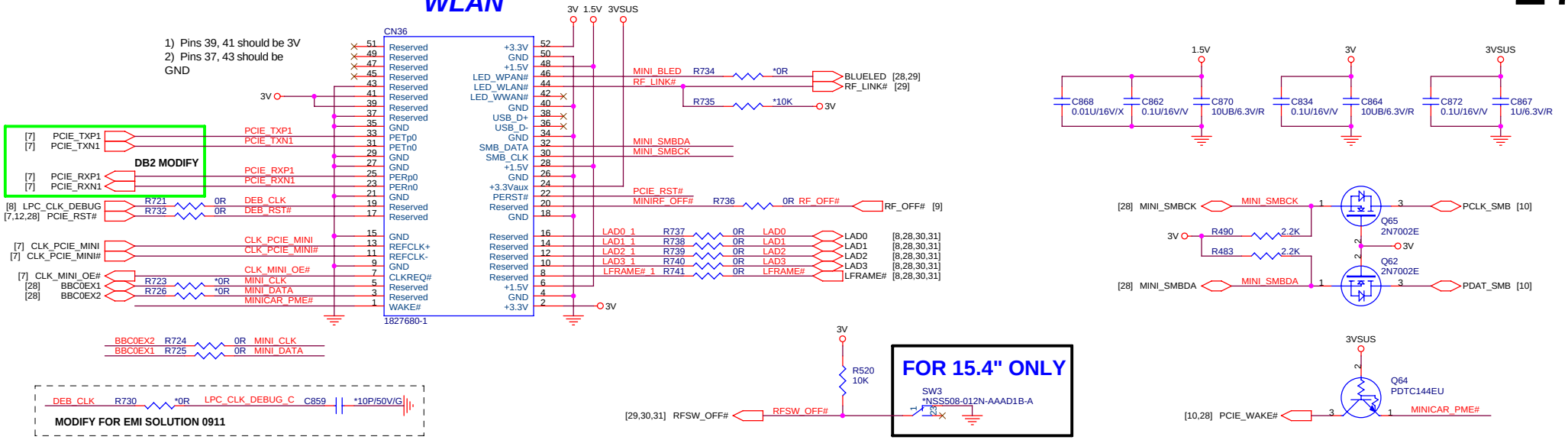
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	SATA HDDx2,CD-ROM,USBx3	C2A

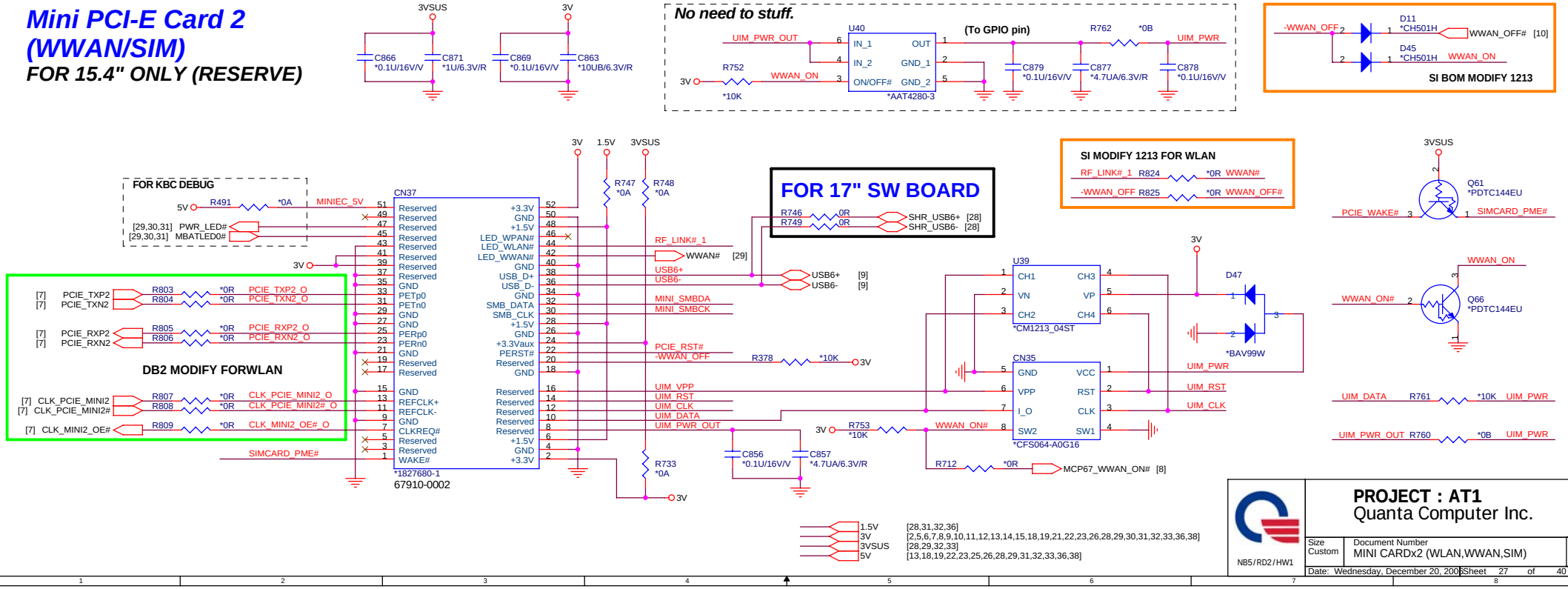
Date: Wednesday, December 20, 2006 Sheet 26 of 40

Mini PCI-E Card 1
WLAN

1) Pins 39, 41 should be 3V
2) Pins 37, 43 should be GND



Mini PCI-E Card 2
(WWAN/SIM)
FOR 15.4" ONLY (RESERVE)



1.5V	[28,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,28,29,30,31,32,33,36,38]
3VSUS	[28,29,32,33]
5V	[13,18,19,22,23,25,26,28,29,31,32,33,36,38]

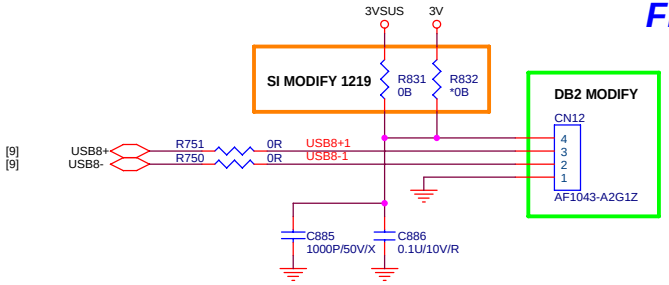
PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MINI CARDx2 (WLAN,WWAN,SIM)	C2A

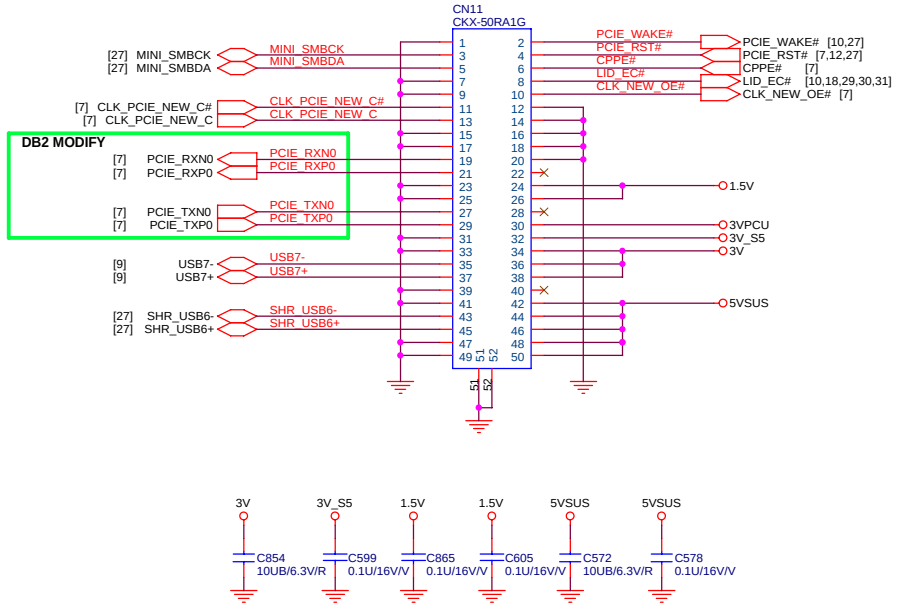
NB5/RD2/HW1

Date: Wednesday, December 20, 2006 Sheet 27 of 40

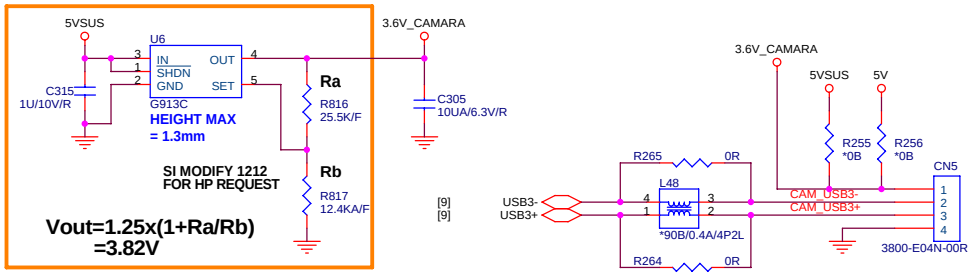
FINGER PRINT



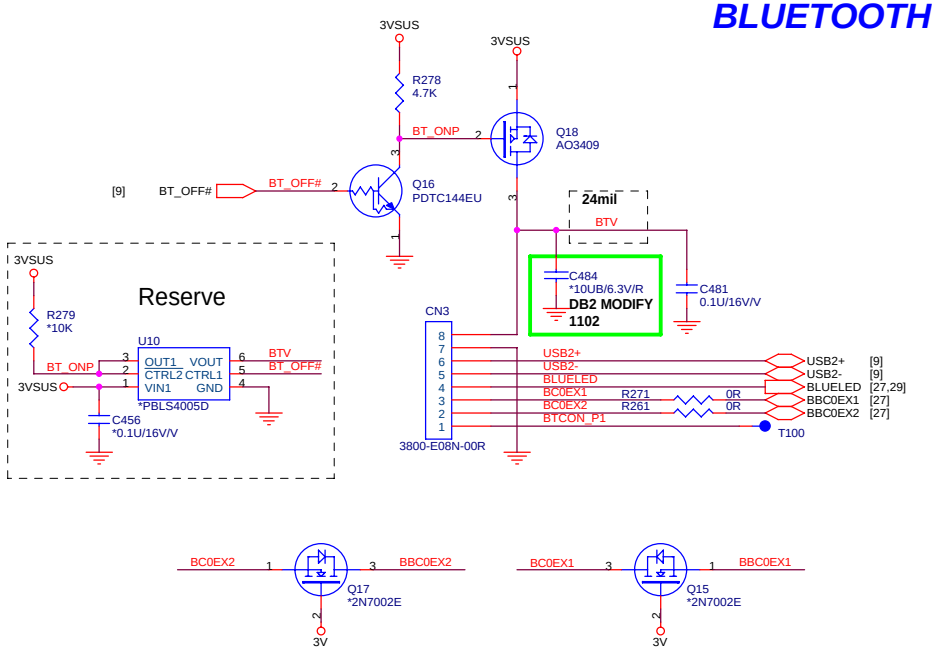
NEW CARD



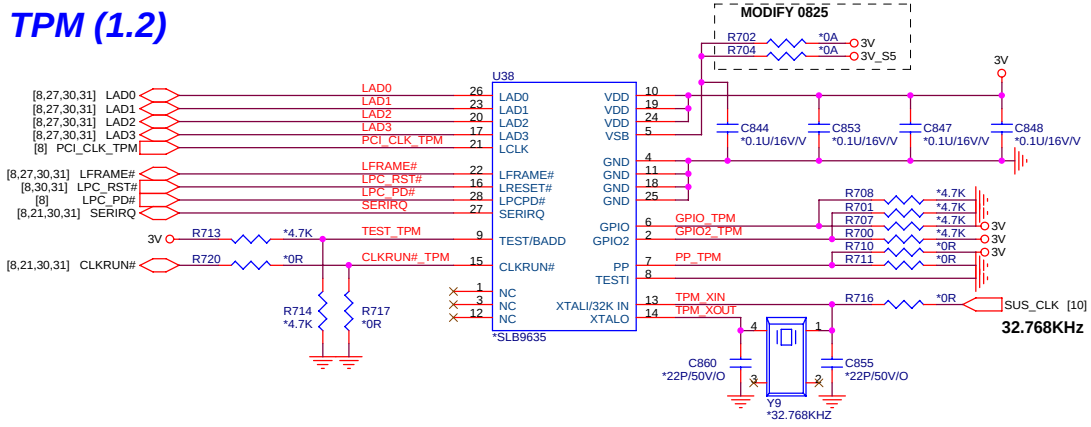
CAMERA



BLUETOOTH



TPM (1.2)



Address

	BADD
HIGH	4EH/4F (dafault)
LOW	2EH/2FH

*** DEFAULT**

PP (PHYSICAL PRESENCE)	
*L	PLATFORM PROTECT
H	USER ACCESS

1.5V	[27,31,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,29,30,31,32,33,36,38]
3VSUS	[27,29,32,33]
3V_S5	[8,9,10,11,20,30,32,33,37]
3VPCU	[9,14,18,29,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,29,31,32,33,36,38]
5VSUS	[18,26,30,31,32,33,37]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	NEW CARD,CAMER,TPM,F/P,B/T	C2A

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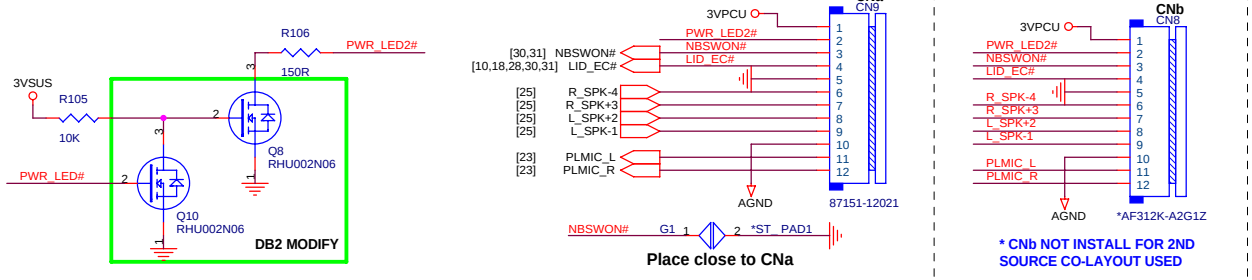
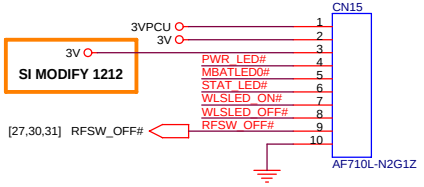
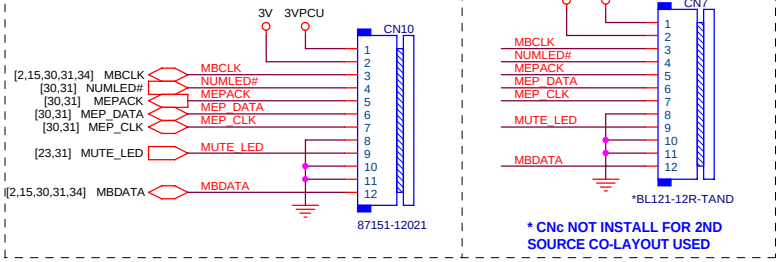
FOR POWER ON AND INTERNAL SPK / MIC SW BOARD



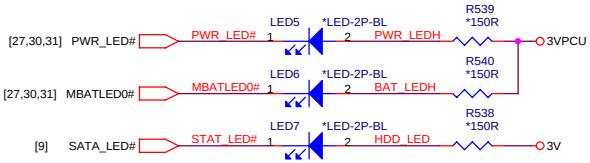
FOR 17" LED AND WIRLESS SW BOARD



FOR QLB SW BOARD

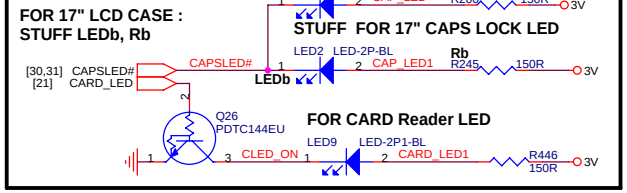


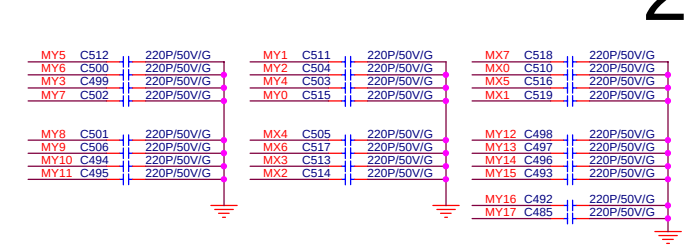
STUFF FOR 15.4" LED USED



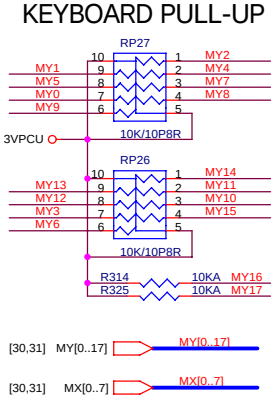
FOR 15.4" LCD CASE : STUFF LEDa, Ra

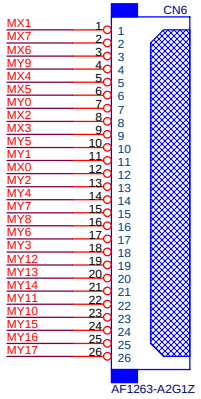
FOR 17" LCD CASE : STUFF LEDb, Rb

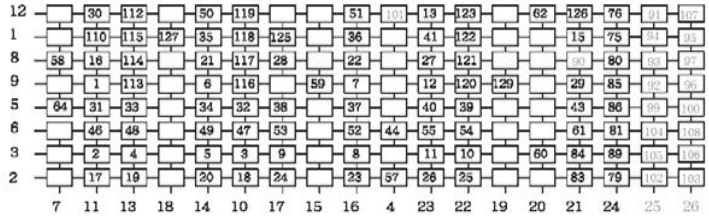


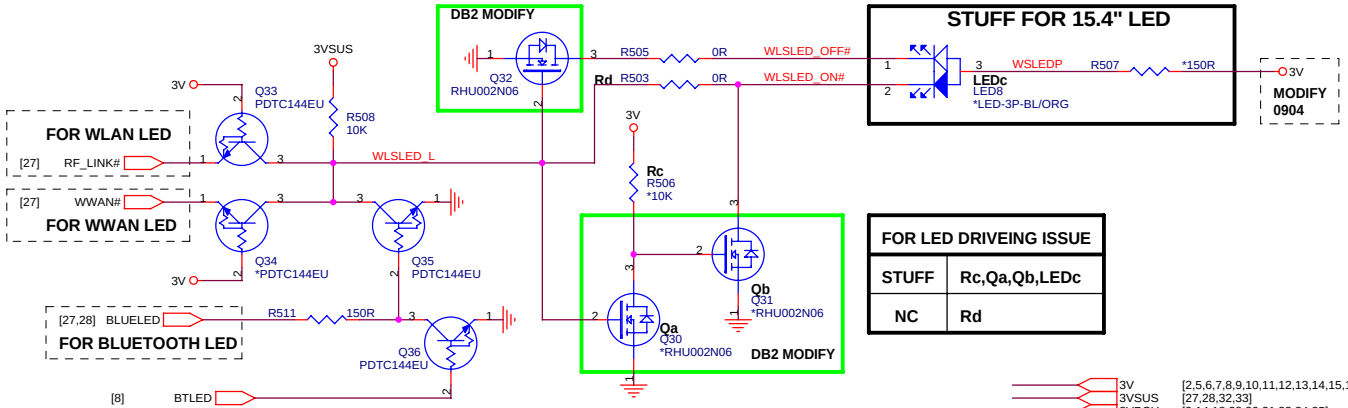


KEYBOARD PULL-UP



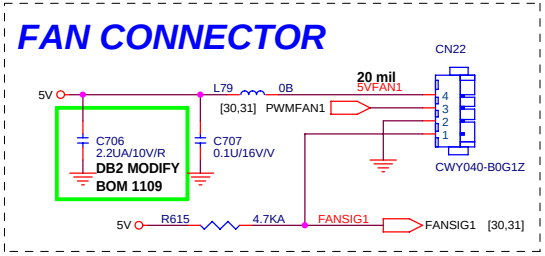






FOR LED DRIVEING ISSUE	
STUFF	Rc,Qa,Qb,LEDc
NC	Rd

FAN CONNECTOR



3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,30,31,32,33,36,38]
3VSUS	[27,28,32,33]
3VPCU	[9,14,18,28,30,31,33,34,35]
5V	[13,18,19,22,23,25,26,27,28,31,32,33,36,38]

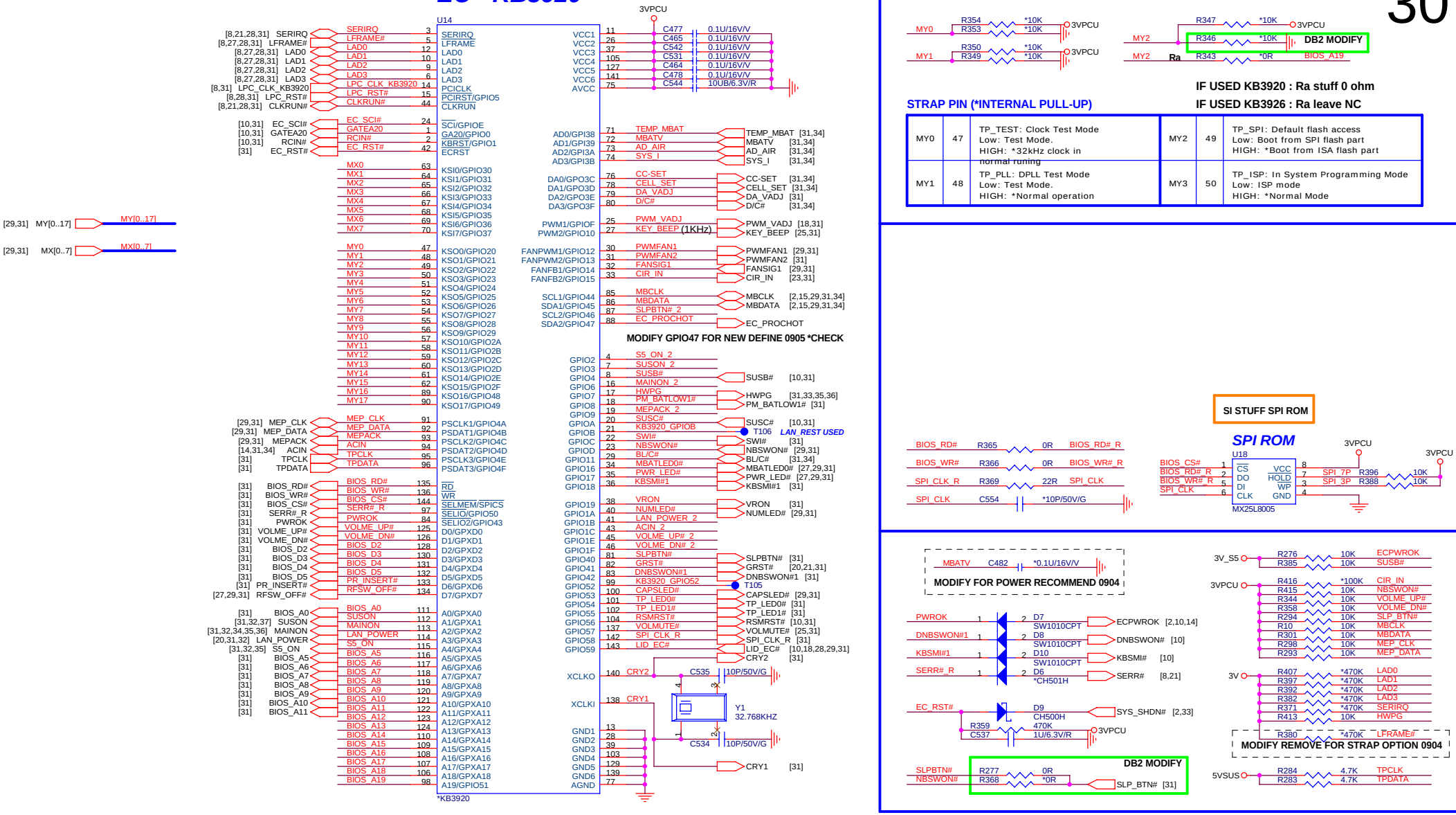
NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB,FAN,LED,SW (PWR,QLB,LED)	C2A

Date: Wednesday, December 20, 2006 Sheet 29 of 40

EC - KB3920



[29,31] MY[0..17] — MY[0..17]

[29,31] MX[0..7] — MX[0..7]

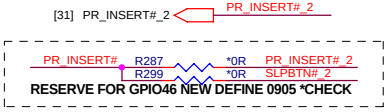
STRAP PIN (*INTERNAL PULL-UP)

MY0	47	TP_TEST: Clock Test Mode Low: Test Mode. HIGH: *32kHz clock in normal runing	MY2	49	TP_SPI: Default flash access Low: Boot from SPI flash part HIGH: *Boot from ISA flash part
MY1	48	TP_PLL: DPLL Test Mode Low: Test Mode. HIGH: *Normal operation	MY3	50	TP_ISP: In System Programming Mode Low: ISP mode HIGH: *Normal Mode

IF USED KB3920 : Ra stuff 0 ohm

IF USED KB3926 : Ra leave NC

SI STUFF SPI ROM



DB2 MODIFY

3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,31,32,33,36,38]
3V_S5 [8,9,10,11,20,28,32,33,37]
3VPCU [9,14,18,28,29,31,33,34,35]
5VSUS [18,26,28,31,32,33,37]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	KB3920,SPI_ROM	C2A

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EC - KB3926

U15

KB3926

[8,21,28,30] SERIRQ	SERIRQ	3	SERIRQ				
[8,27,28,30] LFRAME#	LFRAME#	4	LFRAME				
[8,27,28,30] LAD0	LAD0	10	LAD0				
[8,27,28,30] LAD1	LAD1	8	LAD1				
[8,27,28,30] LAD2	LAD2	7	LAD2				
[8,27,28,30] LAD3	LAD3	5	LAD3				
[8,30] LPC_CLK_KB3920	LPC_CLK_KB3920	12	PCICLK				
[8,28,30] LPC_RST#	LPC_RST#	13	PCIRST/GPIO5				
[8,21,28,30] CLKRUN#	CLKRUN#	38	CLKRUN				
[10,30] EC_SCI#	EC_SCI#	20	SCI/GPIOE				
[10,30] GATEA20	GATEA20	1	GA20/GPIO0				
[10,30] RCIN#	RCIN#	2	KBRST/GPIO1				
[30] EC_RST#	EC_RST#	37	ECRST				
	MX0	55	KSI0/GPIO30				
	MX1	56	KSI1/GPIO31				
	MX2	57	KSI2/GPIO32				
	MX3	58	KSI3/GPIO33				
	MX4	59	KSI4/GPIO34				
	MX5	60	KSI5/GPIO35				
	MX6	61	KSI6/GPIO36				
	MX7	62	KSI7/GPIO37				
	MY0	39	KSO0/GPIO20				
	MY1	40	KSO1/GPIO21				
	MY2	41	KSO2/GPIO22				
	MY3	42	KSO3/GPIO23				
	MY4	43	KSO4/GPIO24				
	MY5	44	KSO5/GPIO25				
	MY6	45	KSO6/GPIO26				
	MY7	46	KSO7/GPIO27				
	MY8	47	KSO8/GPIO28				
	MY9	48	KSO9/GPIO29				
	MY10	49	KSO10/GPIO2A				
	MY11	50	KSO11/GPIO2B				
	MY12	51	KSO12/GPIO2C				
	MY13	52	KSO13/GPIO2D				
	MY14	53	KSO14/GPIO2E				
	MY15	54	KSO15/GPIO2F				
	MY16	81	KSO16/GPIO48				
	MY17	82	KSO17/GPIO49				
[29,30] MEP_CLK	MEP_CLK	83	PSCLK1/GPIO4A				
[29,30] MEP_DATA	MEP_DATA	84	PSDAT1/GPIO4B				
[29,30] MEPACK	MEPACK	85	PSCLK2/GPIO4C				
[14,30,34] ACIN	ACIN	86	PSDAT2/GPIO4D				
[30] TPCLK	TPCLK	87	PSCLK3/GPIO4E				
[30] TPDATA	TPDATA	88	PSDAT3/GPIO4F				
[30] BIOS_RD#	BIOS_RD#	119	RD				
[30] BIOS_WR#	BIOS_WR#	120	WR				
[30] BIOS_CS#	BIOS_CS#	128	SELMEM/SPICS				
[30] SERR#_R	SERR#_R	89	SELIO/GPIO50				
[30] PWROK	PWROK	76	SELIO2/GPIO43				
[30] VOLME_UP#	VOLME_UP#	109	D0/GPXD0				
[30] VOLME_DN#	VOLME_DN#	110	D1/GPXD1				
[30] BIOS_D2	BIOS_D2	112	D2/GPXD2				
[30] BIOS_D3	BIOS_D3	114	D3/GPXD3				
[30] BIOS_D4	BIOS_D4	115	D4/GPXD4				
[30] BIOS_D5	BIOS_D5	116	D5/GPXD5				
[30] PR_INSERT#	PR_INSERT#	117	D6/GPXD6				
[27,29,30] RFSW_OFF#	RFSW_OFF#	118	D7/GPXD7				
[30] BIOS_A0	BIOS_A0	97	A0/GPXA0				
[30,32,37] SUSON	SUSON	98	A1/GPXA1				
[30,32,34,35,36] MAINON	MAINON	99	A2/GPXA2				
[20,30,32] LAN_POWER	LAN_POWER	100	A3/GPXA3				
[30,32,35] S5_ON	S5_ON	101	A4/GPXA4				
[30] BIOS_A5	BIOS_A5	102	A5/GPXA5				
[30] BIOS_A6	BIOS_A6	103	A6/GPXA6				
[30] BIOS_A7	BIOS_A7	104	A7/GPXA7				
[30] BIOS_A8	BIOS_A8	105	A8/GPXA8				
[30] BIOS_A9	BIOS_A9	106	A9/GPXA9				
[30] BIOS_A10	BIOS_A10	107	A10/GPXA10				
[30] BIOS_A11	BIOS_A11	108	A11/GPXA11				
T108	KB3926_V18R	124	V18R				
			VCC1	9			
			VCC2	22			
			VCC3	33			
			VCC4	96			
			VCC5	111			
			VCC6	125			
			AVCC	67	3VPCU		
			AD0/GPI3B	63	TEMP_MBAT	TEMP_MBAT [30,34]	
			AD1/GPI39	64	MBATV	MBATV [30,34]	
			AD2/GPI3A	65	AD_AIR	AD_AIR [30,34]	
			AD3/GPI3B	66	SYS_I	SYS_I [30,34]	
			DA0/GPO3C	68	CC-SET	CC-SET [30,34]	
			DA1/GPO3D	70	CELL_SET	CELL_SET [30,34]	
			DA2/GPO3E	71	DA_VADJ	DA_VADJ [30]	
			DA3/GPO3F	72	D/C#	D/C# [30,34]	
			PWM1/GPIOE	21	PWM_VADJ	PWM_VADJ [18,30]	
			PWM2/GPIO10	23	KEY_BEEP (1KHz)	KEY_BEEP [25,30]	
			FANPWM1/GPIO12	26	PWMFAN1	PWMFAN1 [29,30]	
			FANPWM2/GPIO13	27	PWMFAN2	PWMFAN2 [30]	
			FANFB1/GPIO14	28	FANSIG1	FANSIG1 [29,30]	
			FANFB2/GPIO15	29	CIR_IN	CIR_IN [23,30]	
			SCL1/GPIO44	77	MBCLK	MBCLK [2,15,29,30,34]	
			SDA1/GPIO45	78	MBDATA	MBDATA [2,15,29,30,34]	
			SCL2/GPIO46	79	PR_INSERT#_2	PR_INSERT#_2 [30]	
			SDA2/GPIO47	80	EC_PROCHOT#	EC_PROCHOT# [2]	
			GPIO4	6	SUSB#	SUSB# [10,30]	
			GPIO7	14	HWPG	HWPG [30,33,35,36]	
			GPIO8	15	PM_BATLOW1#	PM_BATLOW1# [30]	
			GPIOA	16	SUSC#	SUSC# [10,30]	
			GPIOB	17	KB3926_GPIOB	T107 LAN_REST USED	
			GPIOC	18	SWI#	SWI# [30]	
			GPIOD	19	NBSWON#	NBSWON# [29,30]	
			GPIO11	25	BL/C#	BL/C# [30,34]	
			GPIO16	30	MBATLED0#	MBATLED0# [27,29,30]	
			GPIO17	31	PWR_LED#	PWR_LED# [27,29,30]	
			GPIO18	32	KBSMI#1	KBSMI#1 [30]	
			GPIO19	34	VRON	VRON [30]	
			GPIO1A	36	NUMLED#	NUMLED# [29,30]	
			GPIO40	73	SLPBTN#	SLPBTN# [30]	
			GPIO41	74	GRST#	GRST# [20,21,30]	
			GPIO42	75	DNBSWON#1	DNBSWON#1 [30]	
			GPIO52	90	KB3926_GPIO52	T109	
			GPIO53	91	CAPSLED#	CAPSLED# [29,30]	
			GPIO54	92	TP_LED0#	TP_LED0# [30]	
			GPIO55	93	TP_LED1#	TP_LED1# [30]	
			GPIO56	95	RSMRST#	RSMRST# [10,30]	
			GPIO57	121	VOLMUTE#	VOLMUTE# [25,30]	
			GPIO58	126	SPI_CLK_R	SPI_CLK_R [30]	
			GPIO59	127	LID_EC#	LID_EC# [10,18,28,29,30]	
			XCLKO	123	CRY2	[30]	
			XCLKI	122	CRY1	[30]	
			GND1	11			
			GND2	24			
			GND3	35			
			GND4	94			
			GND5	113			
			AGND	69			

MODIFY GPIO46,47 FOR NEW DEFINE 0905 *CHECK

SPI H/W STRAPPING

BIOS_A0 R315 1K

DB2 MODIFY 1101

[29,30] MY[0..17] — MY[0..17]

[29,30] MX[0..7] — MX[0..7]

LPC_CLK_KB3920 R421 *0R LPC_CLK_KB3920_C C579 *10P/50V/G

MODIFY FOR EMI SOLUTION 0911

CABLE DOCK

CN21

QL1122L-H212CR-7F-44P

DB2 MODIFY 1107 FOR EMI SOLUTION

[19] CRT_G1	CRT_G1	R36	120/0.5A	CRT_GDK	38		
[19] CRT_R1	CRT_R1	R32	120/0.5A	CRT_RDK	40		
[6,13,19] DDCDAT	DDCDAT	R51	0R	DDAT_DK	34		
[19] CRT_B1	CRT_B1	R40	120/0.5A	CRT_BDK	36		
[19] HSYNC2	HSYNC2	R25	0R	HSY_DK	30		
[6,13,19] DDCCLK	DDCCLK	R53	0R	DCLK_DK	32		
				USB4-1	26		
[19] VSYNC2	VSYNC2	R26	0R	VSY_DK	28		
				USB4+1	24		
[20] +LAN_MX3	+LAN_MX3				18		
[20] -LAN_MX3	-LAN_MX3				20		
[20] +LAN_MX2	+LAN_MX2				14		
[20] -LAN_MX2	-LAN_MX2				16		
[20] +LAN_MX1	+LAN_MX1				10		
[20] -LAN_MX1	-LAN_MX1				12		
[20] +LAN_MX0	+LAN_MX0				6		
[20] -LAN_MX0	-LAN_MX0				8		
VIN					2		
					4		
					42		
					46		
					44	VA_P	
					43	VA_P	
					39		
					37	SYD_DK R566 0R	TV_LUMA
					35	SCD_DK R567 0R	TV_CHROMA
					33	SCVBS_DK R570 0R	TV_COMP
					31	VIDEO_GND R576 0R	
					29	CIRIN_DK R578 0R	CIR_IN
					27	PWR_ON	
					25	MUTE_LED	MUTE_LED [23,29]
					23	SLP_BTN#	SLP_BTN# [30]
					21	JACK_DETECT#	JACK_DETECT# [23]
					19	VOLME_UP#	VOLME_UP# [30]
					17	VOLME_DN#	VOLME_DN# [30]
					15	SPDIF_DOCK	
					13	AUDIO_G R606 0R	AGND
					11	RSPK_DK	
					9	LSPK_DK	
					7	RMIC_DK R588 0R	DOCK_MIC_R [23]
					5	LMIC_DK R599 0R	DOCK_MIC_L [23]
					3	MIC_GND R597 0R	AGND
					1	DOCK_PRESENT	
					41		
					45		

SPDIF C723 *270P/25V/O

JACK_DETECT# C713 270P/25V/O

CIR_IN C710 *120P/50V/O

VOLME_DN# C716 *120P/50V/O

DB2 MODIFY 1030 FOR POWER RECOMMEND

VA L89 0.015B/4A L73 0.015B/4A

150 mils VA_P

C681 0.1U/25V/V C682 0.1U/25V/V MODIFY 0831

5VSUS R582 1K DK_PWRON D40 SW1010CPT

DB2 MODIFY 1106

5V D39 SW1010CPT

R60 1.5K/F PWR_ON

S0: 4V
S3: 2.5V
S4/S5: 0V
*Check voltage on DB

3VPCU R595 *100K

[30] PR_INSERT# R600 *0R PR_INSERT_L#

DOCK_PRESENT R598 1K DKPR# Q50 *MMBT3904

R602 2KA/F

1.5V R587 33R SPDDK_V SPD_DK L80 0A SPDIF_DOCK

Q49 MMBT3904

[12,23] SPDIF SPDIF R591 510/F SPDIF_DK R589 510/F

C722 68P/50V/G

RSPK_DK R67 *0R C107 100U/6.3V/3528 DOCK_RSPK+ [23]

LSPK_DK C142 100U/6.3V/3528 DOCK_LSPK+ [23]

R81 *0R

[9] USB4- [9] USB4+ R61 0R L8 *90B/0.33A/4P2L R66 0R USB4-1 USB4+1

RESERVE FOR EMI SOULTION

TV_LUMA	C55	*82P/50V/O
TV_CHROMA	C64	*82P/50V/O
TV_COMP	C70	*82P/50V/O
SYD_DK	C685	*82P/50V/O
SCD_DK	C690	*82P/50V/O
SCVBS_DK	C699	*82P/50V/O
RSPK_DK	C104	*10P/50V/G
LSPK_DK	C116	*10P/50V/G
RMIC_DK	C721	*10P/50V/G
LMIC_DK	C725	*10P/50V/G
USB4+1	C95	*10P/50V/G
USB4-1	C88	*10P/50V/G
CRT_GDK	C36	*10P/50V/G
CRT_RDK	C33	*10P/50V/G
CRT_BDK	C57	*10P/50V/G
CRT_G1	C37	*10P/50V/G
CRT_R1	C32	*10P/50V/G
CRT_B1	C46	*10P/50V/G
HSY_DK	C31	*10P/50V/G
VSY_DK	C87	*10P/50V/G
DDAT_DK	C65	*10P/50V/G
DCLK_DK	C85	*10P/50V/G
+LAN_MX0	C762	*10P/50V/G
-LAN_MX0	C766	*10P/50V/G
+LAN_MX1	C125	*10P/50V/G
-LAN_MX1	C117	*10P/50V/G
+LAN_MX2	C281	*10P/50V/G
-LAN_MX2	C294	*10P/50V/G
+LAN_MX3	C786	*10P/50V/G
-LAN_MX3	C788	*10P/50V/G

TOUCH PAD CONNECTOR

SW1 MX4 MY7 TACT-SWITCH

(Amber) TP_LED0# LED3 TPLD1 *150R R342 3V

(Blue) TP_LED1# TPLD2 *150R R341 3V

*LED-4P-BL/ORG

FOR 15.4"

SW2 MX4 MY7 TACT-SWITCH

(Amber) TP_LED0# LED4 TPLD3 150R R402 3V

(Blue) TP_LED1# TPLD4 150R R412 3V

LED-4P-BL/ORG

FOR 17"

5VSUS C403 0.1U/16V/V L36 80A/0.6A L37 220A/0.2A L38 220A/0.2A TPCLK TPDATA

25 mils 5VTP

TPCLK-1 TPDATA-1

CN4 AF1043-A2G1Z

C404 *10P/50V/G C405 *10P/50V/G

1.5V	[27,28,32,36]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,32,33,36,38]
3VPCU	[9,14,18,28,29,30,33,34,35]
5VSUS	[18,26,28,30,32,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,32,33,36,38]
VA	[34]
VIN	[18,32,33,34,35,36,37,38]

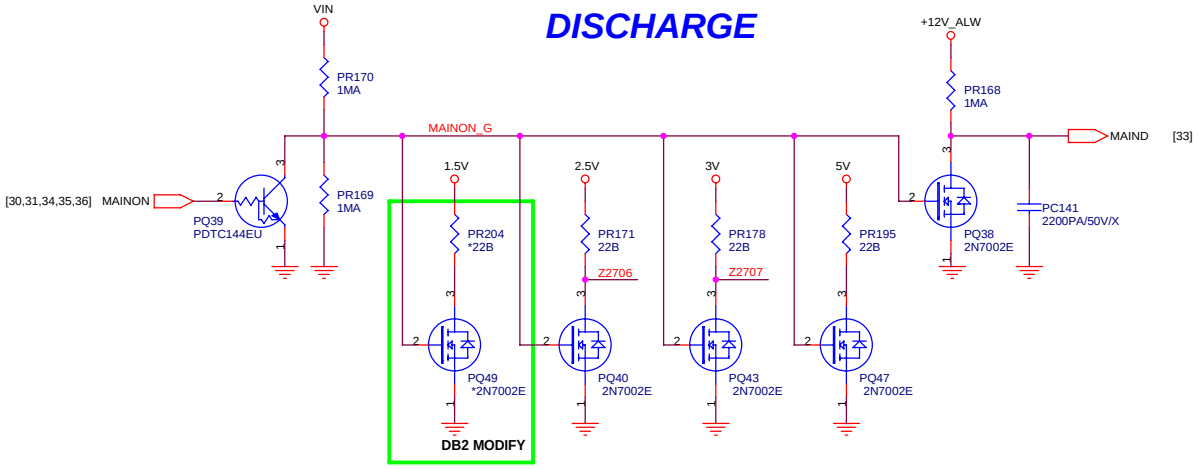
NB5/RD2/HW1

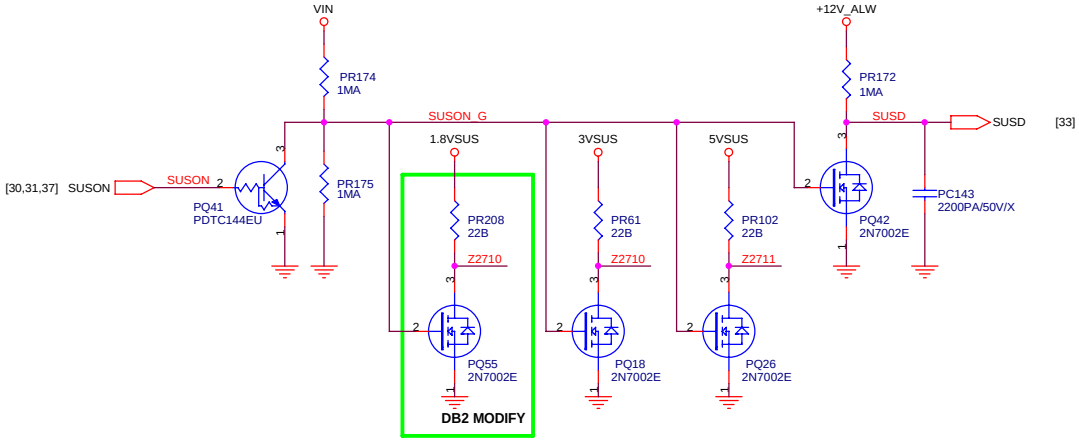
PROJECT : AT1
Quanta Computer Inc.

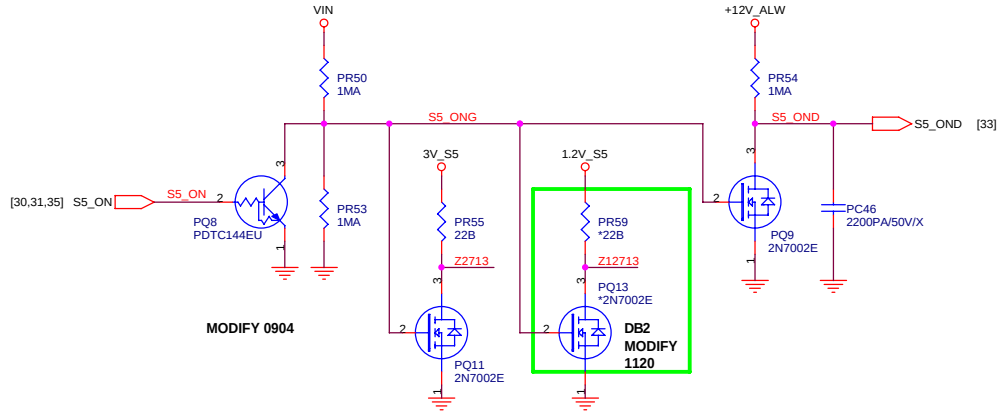
Size	Document Number	Rev
Custom	KB3926,DOCKING,TOUCH_PAD	C2A

Date: Wednesday, December 20, 2006 Sheet 31 of 40

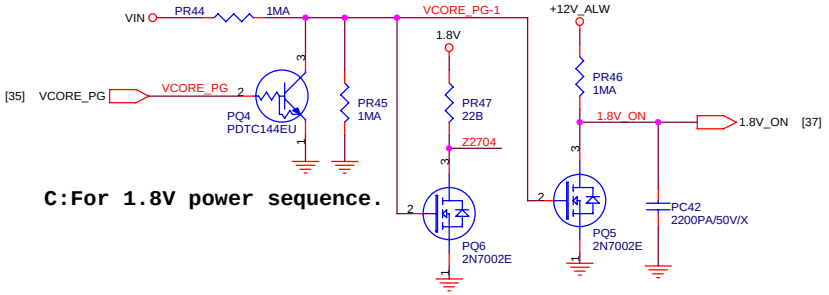
DISCHARGE



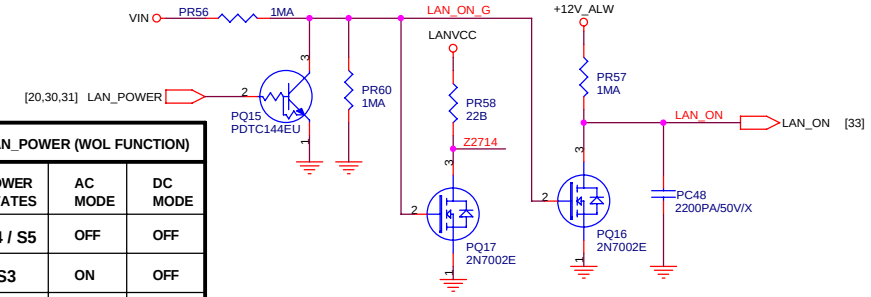




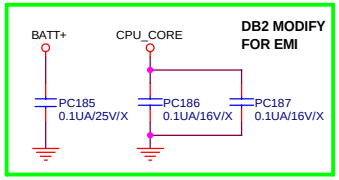
SI POWER MODIFY



C:For 1.8V power sequence.



LAN_POWER (WOL FUNCTION)		
POWER STATES	AC MODE	DC MODE
S4 / S5	OFF	OFF
S3	ON	OFF
S0	ON	ON



CPU_CORE	[4,38]
1.2V_S5	[10,11,35]
1.5V	[27,28,31,36]
1.8V	[11,13,15,16,17,37]
1.8VSUS	[2,3,4,5,6,36,37]
2.5V	[2,13,36]
LANVCC	[20,33]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,33,36,38]
3VSUS	[27,28,29,33]
3V_S5	[8,9,10,11,20,28,30,33,37]
5V	[13,18,19,22,23,25,26,27,28,29,31,33,36,38]
5VSUS	[18,26,28,30,31,33,37]
+12V_ALW	[10,18,33]
VIN	[18,31,33,34,35,36,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	DISCHARGE	C2A

Date: Wednesday, December 20, 2006 Sheet 32 of 40

DC/DC 3VPCU/ 5VPCU/ +12V_ALW

TOPN: OUT1/OUT2
GND=400KHz/500KHz
REF = 400KHz /300KHz
VCC5=200KHz/300KHz

5 Volt +/- 5%

5VPCU
C/C:8A
P/C:10A

Vout=0.7(Ra+Rb)/Rb
Rb around 49.9k

3.3 Volt +/- 5%

3VPCU
C/C:8A
P/C:10A

Place these CAPs close to FETs

Place these CAPs close to FETs

PU6 ISL6236

Rds(on) 13m ohm

Rds(on) 13m ohm

I_lim*MOSFET(RDSON)=V_ILIM(mV)/10
V_ILIM(mV)=5uA*R_ILIM

DB2 MODIFY

DB2 MODIFY

SI power

SI power

SI power

SI power

SI power

4.59A
S0-S1

5A
S0-S3

LANVCC
0.2A

3V
9.0A
S0-S1

1A
S0-S5

1.6A
S0-S3

+12V_ALW	[10,18,32]
LANVCC	[20,32]
3V	[2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,36,38]
3VSUS	[27,28,29,32]
3V_S5	[8,9,10,11,20,28,30,32,37]
3VPCU	[9,14,18,28,29,30,31,34,35]
5V	[13,18,19,22,23,25,26,27,28,29,31,32,36,38]
5VSUS	[18,26,28,30,31,32,37]
5VPCU	[10,23,34,35,36,37,38]
VIN	[18,31,32,34,35,36,37,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ISL6236 (5VPCU,3VPCU)	C2A

NB5/RD2/HW1

Date: Wednesday, December 20, 2006 Sheet 33 of 40

Adapter
19V/3.4A/65W
19V/4.75A/90W

MAX8724

Battery 6/8/12cell

34

From Docking CNN

360mil

FOR AT2 17"

FOR AT1 15.4"

Setting the Vin min to 8V

V=I*0.01*3*R

I_INPUT=V_CLS/4.096*0.075/0.01

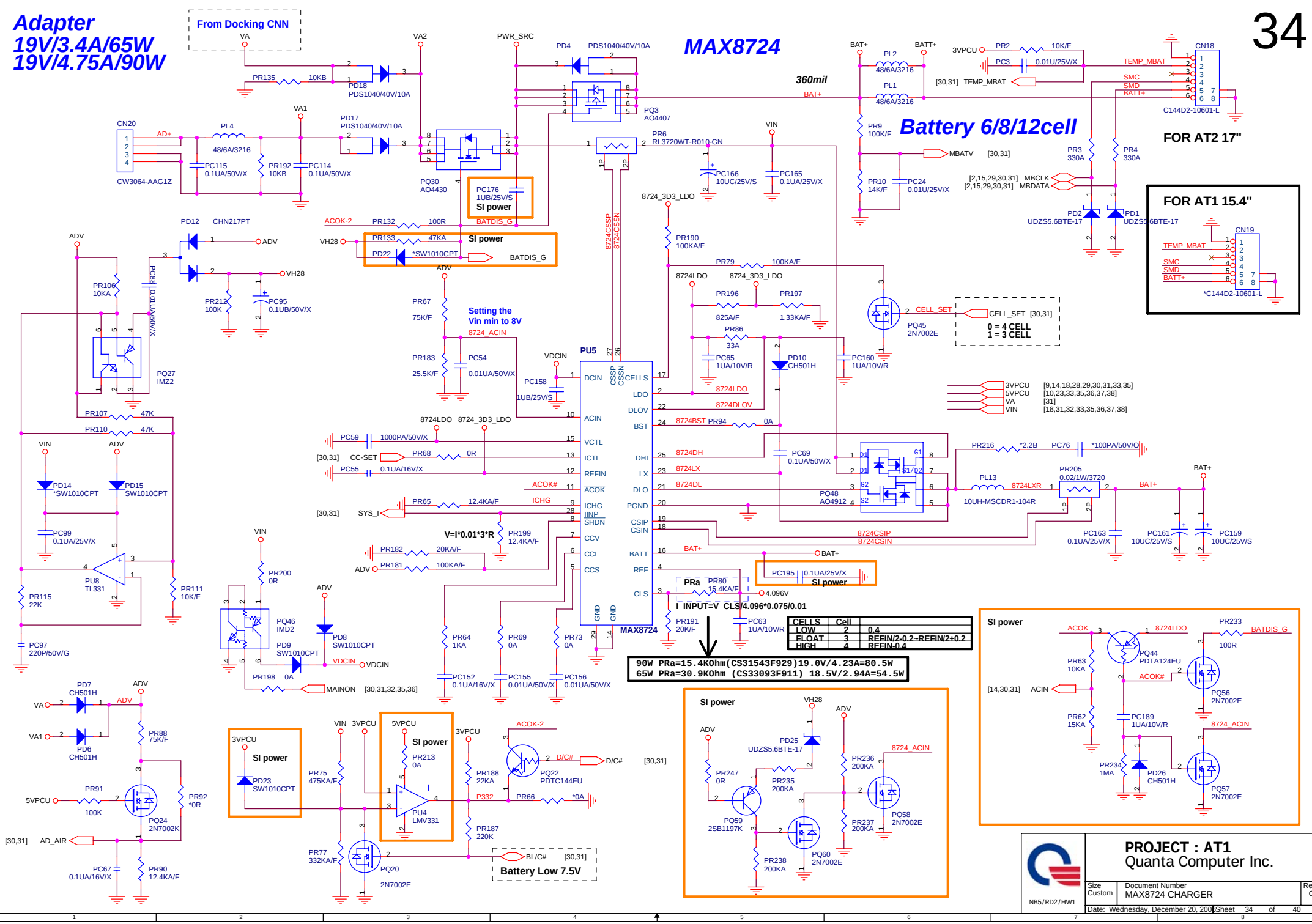
CELLS	Cell	
LOW	2	0.4
FLOAT	3	REFIN/2-0.2~REFIN/2+0.2
HIGH	4	REFIN-0.4

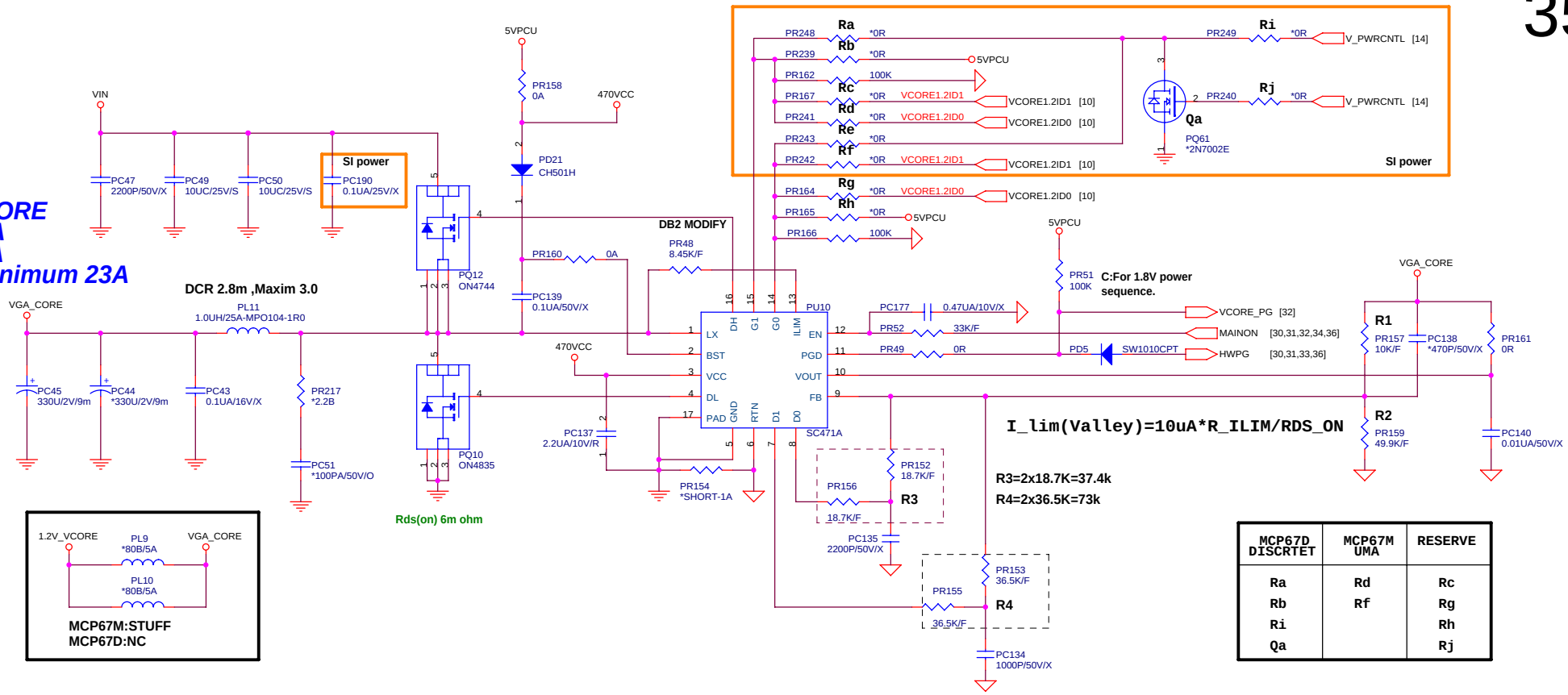
90W PRa=15.4KOhm(CS31543F929)19.0V/4.23A=80.5W
65W PRa=30.9KOhm (CS33093F911) 18.5V/2.94A=54.5W

0 = 4 CELL
1 = 3 CELL

Battery Low 7.5V

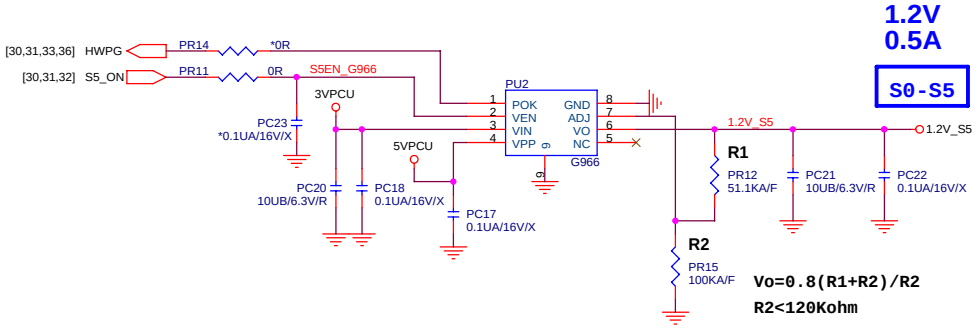
SI power





MCP67D DISCRTET	MCP67M UMA	RESERVE
Ra	Rd	Rc
Rb	Rf	Rg
Ri		Rh
Qa		Rj

INPUTS		OUTPUTS			VGA_CORE
G0	G1	OD1	OD2	OD3	
0	0	0.75x(1+R1/R2+R1/R3+R1/R4)			1.2V
0	1	0.75x(1+R1/R2+R1/R3)			1.1V
1	0	0.75x(1+R1/R2+R1/R4)			1.0V
1	1	0.75x(1+R1/R2)			0.9V



GFX_VID0
H: Normal Voltage
L: Low Voltage

VGACORECTL	NB8X	R2	R3/PR294	PR1293/PR295
HI	1.2V	CS43012FB10	NA	Mounted
LO	1.XV			

1.2V_S5 [10,11,32]
1.2V_VCORE [11,36]
VGA_CORE [12]
3VPCU [9,14,18,28,29,30,31,33,34]
5VPCU [10,23,33,34,36,37,38]
VIN [18,31,32,33,34,36,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

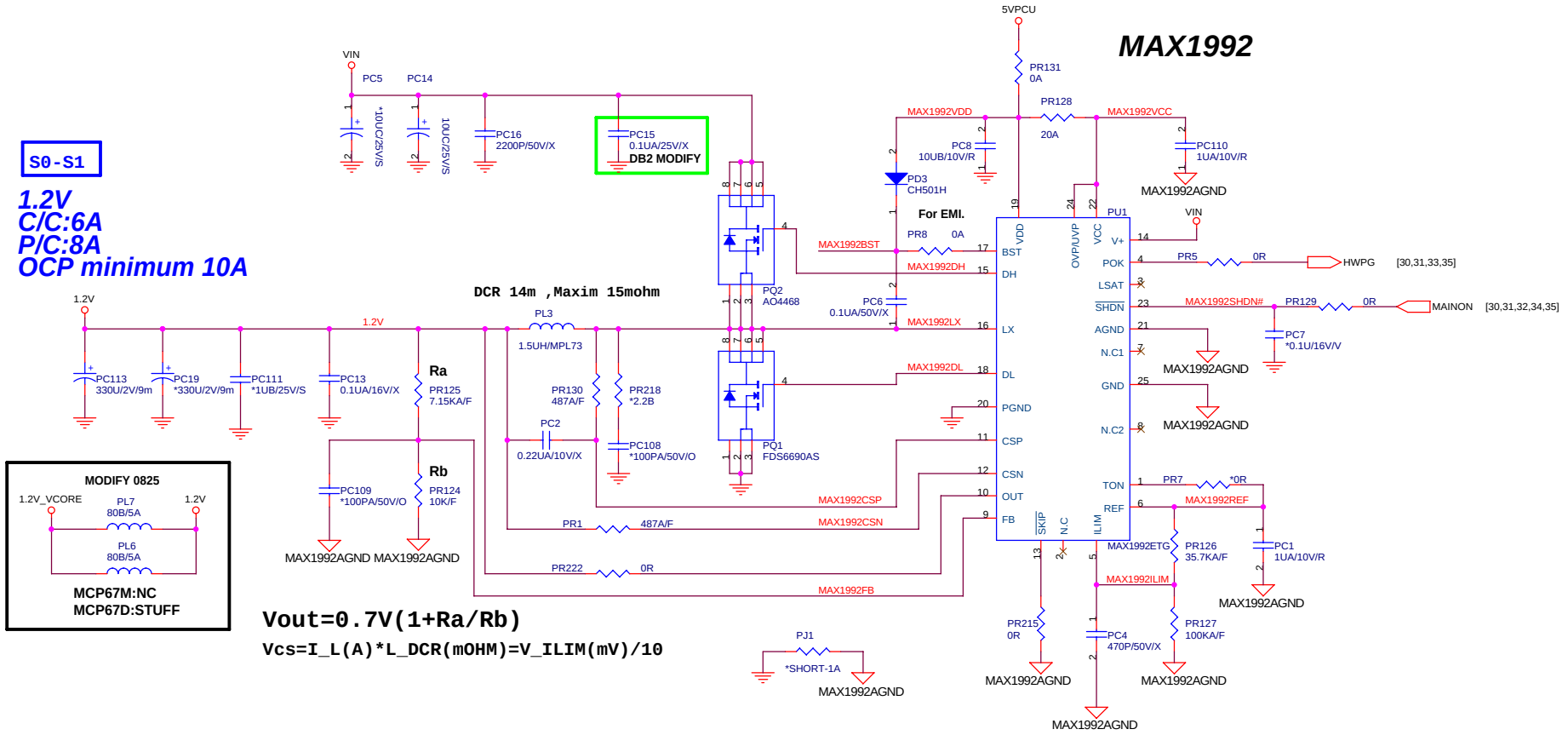
Size	Document Number	Rev
Custom	SC471A (VGA_CORE),1.2V_S5	C2A

Date: Wednesday, December 20, 2006 Sheet 35 of 40

MAX1992

S0-S1

1.2V
C/C:6A
P/C:8A
OCP minimum 10A



Vout=0.7V(1+Ra/Rb)

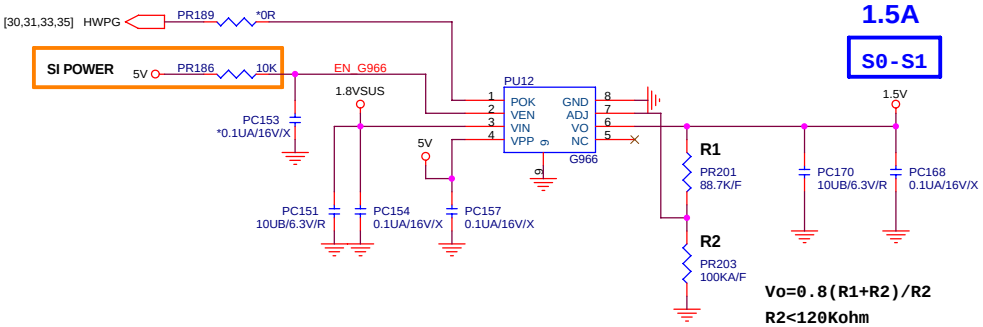
Vcs=I_L(A)*L_DCR(mOHM)=V_ILIM(mV)/10

MODIFY 0825

MCP67M:NC
MCP67D:STUFF

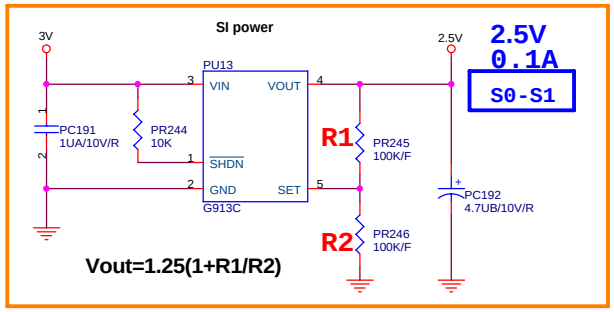
1.5A

S0-S1



Vo=0.8(R1+R2)/R2

R2<120Kohm



Vout=1.25(1+R1/R2)

1.2V_VCORE [11,35]
1.2V [10,11,12,13,15]
1.5V [27,28,31,32]
1.8VSUS [2,3,4,5,6,32,37]
2.5V [2,13,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,38]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,38]
5VPCU [10,23,33,34,35,37,38]
VIN [18,31,32,33,34,35,37,38]

NB5/RD2/HW1

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	MAX1992 (1.2V),1.5V,2.5V	C2A

Date: Wednesday, December 20, 2006 Sheet 36 of 40

S0-S3

1.8VSUS
C/C:12A
P/C:15.2A
OCP minimum 25A

1.8 Volt +/-5%

DCR 2.8m ,Maxim 3.0

Ra=(Vout-0.75)/0.75*Rb

Rb value from 100K to 300K ohm

Rds(on) 4.2m ohm

I_lim(Valley)=10uA*R_ILIM/RDS_ON

PR101 10K/F For OCP set.

S0-S3

SMDDR_VTERM
1.53A / 0.9V

SI MODIFY FOR POWER SEQUENCE 1211

0.9 Volt +/-5%
Design Current:1.5A
Maximum Current: 1.8A

Mode	Discharge Mode
V5IN	No discharge
VDDQ	Tracking discharge
Gnd	Non-tracking discharge

V_TRIP(mV)=R_TRIP(Kohm)*10(uA)

I_OCP=V_trip/Rds_on+I_Ripple/2

VDDQSET	VDDQ(V)	VTTREF and Vtt	Note
GND	2.5	V_ vddqsns/2	DDR
V5IN	1.8	V _vddqsns/2	DDR2
FB	adjustable	V_VDDQSNS/2	1.5V<VDDQ<3V

S0-S3

SMDDR_VTERM
0.9V
?A

0.9V/1.2A

1.8V
4.75A

S0-S1

SMDDR_VTERM [4]
1.8V [11,13,15,16,17,32]
1.8VSUS [2,3,4,5,6,32,36]
3V_S5 [8,9,10,11,20,28,30,32,33]
5VSUS [18,26,28,30,31,32,33]
5VPCU [10,23,33,34,35,36,38]
VIN [18,31,32,33,34,35,36,38]

PROJECT : AT1
Quanta Computer Inc.

Size	Document Number	Rev
Custom	TI51116 (1.8VSUS,VTER),1.8V	C2A

NB5/RD2/HW1

Date: Wednesday, December 20, 2006 Sheet 37 of 40

CPU_CORE MAX8774

Slew rate=(12.5mVus)*(71.5K/R_TIME)
VFB=V_VID+0.125(VREF-VOFS)
VRHOT is low when VTHRM below 1.5V
Tsw=16.26pF(R_TON+6.5K)ohm
CCV CAP=470pF*(2/total phase)*300kHZ/fsw

TON=200K Ohm/ 300K Hz

D5	D4	D3	D2	D1	D0	Output
0	0	0	0	0	0	1.5500V
0	0	0	0	0	1	1.5250V
0	0	0	0	1	0	1.5000V
0	0	0	0	1	1	1.4750V
0	0	0	1	0	0	1.4500V
0	0	0	1	0	1	1.4250V
0	0	0	1	1	0	1.4000V
0	0	0	1	1	1	1.3750V
0	0	1	0	0	0	1.3500V
0	0	1	0	0	1	1.3250V
0	0	1	0	1	0	1.3000V
0	0	1	0	1	1	1.2750V
0	0	1	1	0	0	1.2500V
0	0	1	1	0	1	1.2250V
0	0	1	1	1	0	1.2000V
0	0	1	1	1	1	1.1750V
0	1	0	0	0	0	1.1500V
0	1	0	0	0	1	1.1250V
0	1	0	0	1	0	1.1000V
0	1	0	0	1	1	1.0750V
0	1	0	1	0	0	1.0500V
0	1	0	1	0	1	1.0250V
0	1	0	1	1	0	1.0000V
0	1	0	1	1	1	0.9750V
0	1	1	0	0	0	0.9500V
0	1	1	0	0	1	0.9250V
0	1	1	0	1	0	0.9000V
0	1	1	0	1	1	0.8750V
0	1	1	1	0	0	0.8500V
0	1	1	1	0	1	0.8250V
0	1	1	1	1	0	0.8000V
0	1	1	1	1	1	0.7750V

D5	D4	D3	D2	D1	D0	Output
1	0	0	0	0	0	0.7625V
1	0	0	0	0	1	0.7500V
1	0	0	0	1	0	0.7375V
1	0	0	0	1	1	0.7250V
1	0	0	1	0	0	0.7125V
1	0	0	1	0	1	0.7000V
1	0	0	1	1	0	0.6875V
1	0	0	1	1	1	0.6750V
1	0	1	0	0	0	0.6625V
1	0	1	0	0	1	0.6500V
1	0	1	0	1	0	0.6375V
1	0	1	0	1	1	0.6250V
1	0	1	1	0	0	0.6125V
1	0	1	1	0	1	0.6000V
1	0	1	1	1	0	0.5875V
1	0	1	1	1	1	0.5750V
1	1	0	0	0	0	0.5625V
1	1	0	0	0	1	0.5500V
1	1	0	0	1	0	0.5375V
1	1	0	0	1	1	0.5250V
1	1	0	1	0	0	0.5125V
1	1	0	1	0	1	0.5000V
1	1	0	1	1	0	0.4875V
1	1	0	1	1	1	0.4750V
1	1	1	0	0	0	0.4625V
1	1	1	0	0	1	0.4500V
1	1	1	0	1	0	0.4375V
1	1	1	0	1	1	0.4250V
1	1	1	1	0	0	0.4125V
1	1	1	1	0	1	0.4000V
1	1	1	1	1	0	0.3875V
1	1	1	1	1	1	0.3750V

CPU_CORE
C/C:35A
P/C:35A
OCP minimum 44A

DCR=1.1m/+-5%

DB2 MODIFY

SI MODIFY FOR POWER SEQUENCE 1211

DB2 BOM MODIFY 1108

CPU_CORE [4,32]
3V [2,5,6,7,8,9,10,11,12,13,14,15,18,19,21,22,23,26,27,28,29,30,31,32,33,36]
5V [13,18,19,22,23,25,26,27,28,29,31,32,33,36]
5VPCU [10,23,33,34,35,36,37]
VIN [18,31,32,33,34,35,36,37]

PROJECT : AT1
Quanta Computer Inc.

NB5/RD2/HW1

Size	Document Number	Rev
Custom	MAX8774 (CPU_CORE)	C2A

Date: Wednesday, December 20, 2006 Sheet 38 of 40