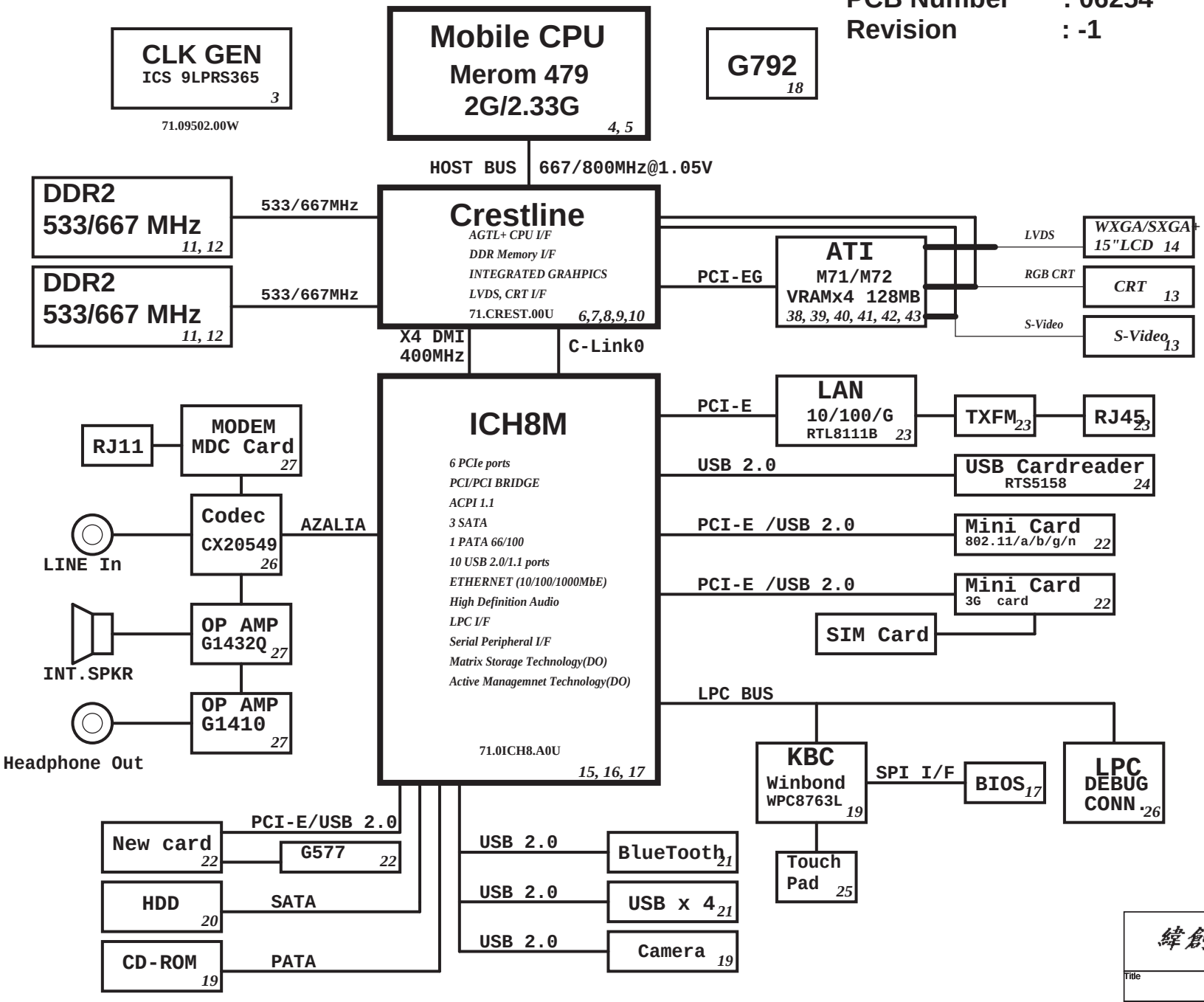
C45/C46 Block Diagram

C45 Project code: 91.4U501.001
C46 Project code: 91.4V001.001
PCB Number : 06254
Revision : -1



SYSTEM DC/DC
TPS51120

INPUTS	OUTPUTS
DCBATOUT	5V_S5(6A) 3D3V_S5(7A)

SYSTEM DC/DC
SC411

INPUTS	OUTPUTS
DCBATOUT	1D05V_S0(9.5A) 1D8V_S3(8.5A)

SC411 TPS5110

DCBATOUT	DDR_VREF_S0 (1.5A) DDR_VREF_S3

APL5913

1D8V_S3	1D5V_S0 (2A)

APL5915

3D3V_S0	2D5V_S0 (300mA)

APL5915

3D3V_S5	1D25V_S0

MAXIM CHARGER
MAX8725

INPUTS	OUTPUTS
DCBATOUT	CHG_PWR 18V 4.0A UP+5V 5V 100mA

CPU DC/DC
ISL6262

INPUTS	OUTPUTS
DCBATOUT	VCC_CORE_S0 0~1.3V 47A

PCB STACKUP

L1: Signal 1
L2: POWER
L3: Signal 2
L4: Signal 3
L5: GND
L6: Signal 4

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Title: BLOCK DIAGRAM

Size: Custom | Document Number: C45/C46 | Rev: -1

Date: Tuesday, April 24, 2007 | Sheet 1 of 45

ICH8M Functional Strap Definitions

Signal	Usage/When Sampled	Comment
HDA_SDOUT	XOR Chain Entrance/ PCIE Port Config1 bit1, Rising Edge of PWROK	Allows entrance to XOR Chain testing when TP3 pulled low.When TP3 not pulled low at rising edge of PWROK,sets bit1 of RPC.PC(Config Registers: offset 224h)
HDA_SYNC	PCIE config1 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-down. Sets bit0 of RPC.PC(Config Registers:Offset 224h)
GNT2#	PCIE config2 bit0, Rising Edge of PWROK.	This signal has a weak internal pull-up. Sets bit2 of RPC.PC2(Config Registers:Offset 0224h)
GPIO20	Reserved	This signal should not be pulled high.
GNT1#/ GPIO51	ESI Strap (Server Only) Rising Edge of PWROK	ESI compatible mode is for server platforms only. This signal should not be pulled low for desttop and mobile.
GNT3#	Top-Block Swap Override. Rising Edge of PWROK.	Sampled low:Top-Block Swap mode(inverts A16 for all cycles targeting FWH BIOS space). Note: Software will not be able to clear the Top-Swap bit until the system is rebooted without GNT3# being pulled down.
GNT0#/ SPI_CS1#	Boot BIOS Destination Selection. Rising Edge of PWROK.	Controllable via Boot BIOS Destination bit (Config Registers:Offset 3410h:bit 11:10). GNT0# is MSB, 01-SPI, 10-PCI, 11-LPC.
INTVRMEN	Integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM Enable/Disable. Always sampled.	Enables integrated VccSus1_05, VccSus1_5 and VccCL1_5 VRM's when sampled high
LAN100_SLP	Integrated VccLAN1_05 and VccCL1_05 VRM Enable/Disable. Always sampled.	Enables integrated VccLAN1_05 and VccCL1_05 VRM's when sampled high
SATALED#	PCI Express Lane Reversal. Rising Edge of PWROK.	Signal has weak internal pull-up. Sets bit 27 of MPC.LR(Device 28:Function 0:Offset D8)
SPKR	No Reboot. Rising Edge of PWROK.	If sampled high, the system is strapped to the "No Reboot" mode(ICH8 will disable the TCO Timer system reboot feature). The status is readable via the NO REBOOT bit.
TP3	XOR Chain Entrance. Rising Edge of PWROK.	This signal should not be pull low unless using XOR Chain testing.
GPIO33/ HDA_DOCK _EN#	Flash Descriptor Security Override Strap Rising Edge of PWROK	This signal has a weak internal pull-up. Sampled low:the Flash Descriptor Security will be overridden. If high,the security measures will be in effect.This should only be used in manufacturing environments.

ICH8M Integrated Pull-up and Pull-down Resistors

SIGNAL	Resistor Type/Value
HDA_BIT_CLK	PULL-DOWN 20K
HDA_RST#	NONE
HDA_SDIN[3:0]	PULL-DOWN 20K
HDA_SDOUT	PULL-DOWN 20K
HDA_SYNC	PULL-DOWN 20K
GNT[3:0]	PULL-UP 20K
GPIO[20]	PULL-DOWN 20K
LDA[3:0]#/FHW[3:0]#	PULL-UP 20K
LAN_RXD[2:0]	PULL-UP 10K
LDRQ[0]	PULL-UP 20K
LDRQ[1]/GPIO23	PULL-UP 20K
PME#	PULL-UP 20K
PWRBTN#	PULL-UP 20K
SATALED#	PULL-UP 15K
SPI_CS1#	PULL-UP 20K
SPI_CLK	PULL-UP 20K
SPI_MOSI	PULL-UP 20K
SPI_MISO	PULL-UP 20K
TACH_[3:0]	PULL-UP 20K
SPKR	PULL-DOWN 20K
TP[3]	PULL-UP 20K
USB[9:0][P,N]	PULL-DOWN 15K
CL_RST#	PULL-UP TBD

Crestline Strapping Signals and Configuration

Pin Name	Strap Description	Configuration
CFG[2:0]	FSB Frequency Select	010 = FSB800 011 = FSB667 others = Reserved
CFG[4:3]	Reserved	
CFG5	DMI x2 Select	0 = DMI x2 1 = DMI x4 (Default)
CFG[7:6]	Reserved	
CFG8	Low Power PCI Express	0 = Normal mode **1 = Low Power mode** (Default)
CFG9	PCI Express Graphics Lane Reversal	0 = Reverse Lanes,15->0,14->1 ect.. **1= Normal operation(Default):Lane Numbered in order**
CFG[11:10]	Reserved	
CFG[13:12]	XOR/ALL Z test straps	00 = Reserved 01 = XOR mode enabled 10 = All Z mode enabled **11 = Normal Operation** (Default)
CFG[15:14]	Reserved	Reserved
CFG16	FSB Dynamic ODT	0 = Dynamic ODT Disabled **1 = Dynamic ODT Enabled (Default)**
CFG[18:17]	Reserved	
CFG19	DMI Lane Reversal	**0 = Normal operation (Default):lane Numbered in order** 1 =Reverse Lane,4->0,3->1 ect...
CFG20	SDVO/PCIE Concurrent	**0 = Only SDVO or PCIE x1 is operational (Default)** 1 =SDVO and PCIE x1 are operating simultaneously via the PEG port
SDVOCRTL _DATA	SDVO Present	**0 = No SDVO Card present** (Default) 1= SDVO Card present

NOTE: All strap signals are sampled with respect to the leading edge of the Calistoga GMCH PWORK in signal.

ICH8M IDE Integrated Series Termination Resistors

DD[15:0], DIOW#, DIOR#, DREQ, DDACK#, IORDY, DA[2:0], DCS1#, DCS3#, IDEIRQ	approximately 33 ohm

PCI Routing

page 17

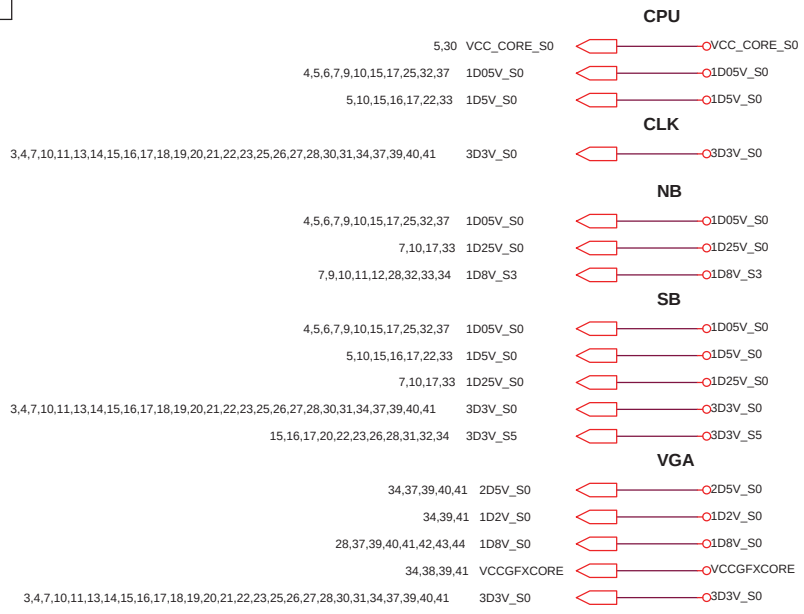
	IDSEL	INT	REQ	GNT

PCIE Routing

LANE1	LAN
LANE2	Express Card
LANE3	MiniCard WLAN
LANE4	USB Cardreader

USB Table

USB Pair	USB Device
0	USB1(ON BOARD)
1	USB2(EXT. USB)
2	USB3(EXT. USB)
3	USB4(EXT. USB)
4	MINICARD
5	USB Cardreader
6	MINICARD
7	NEW CARD
8	BLUETOOTH
9	WEBCAM



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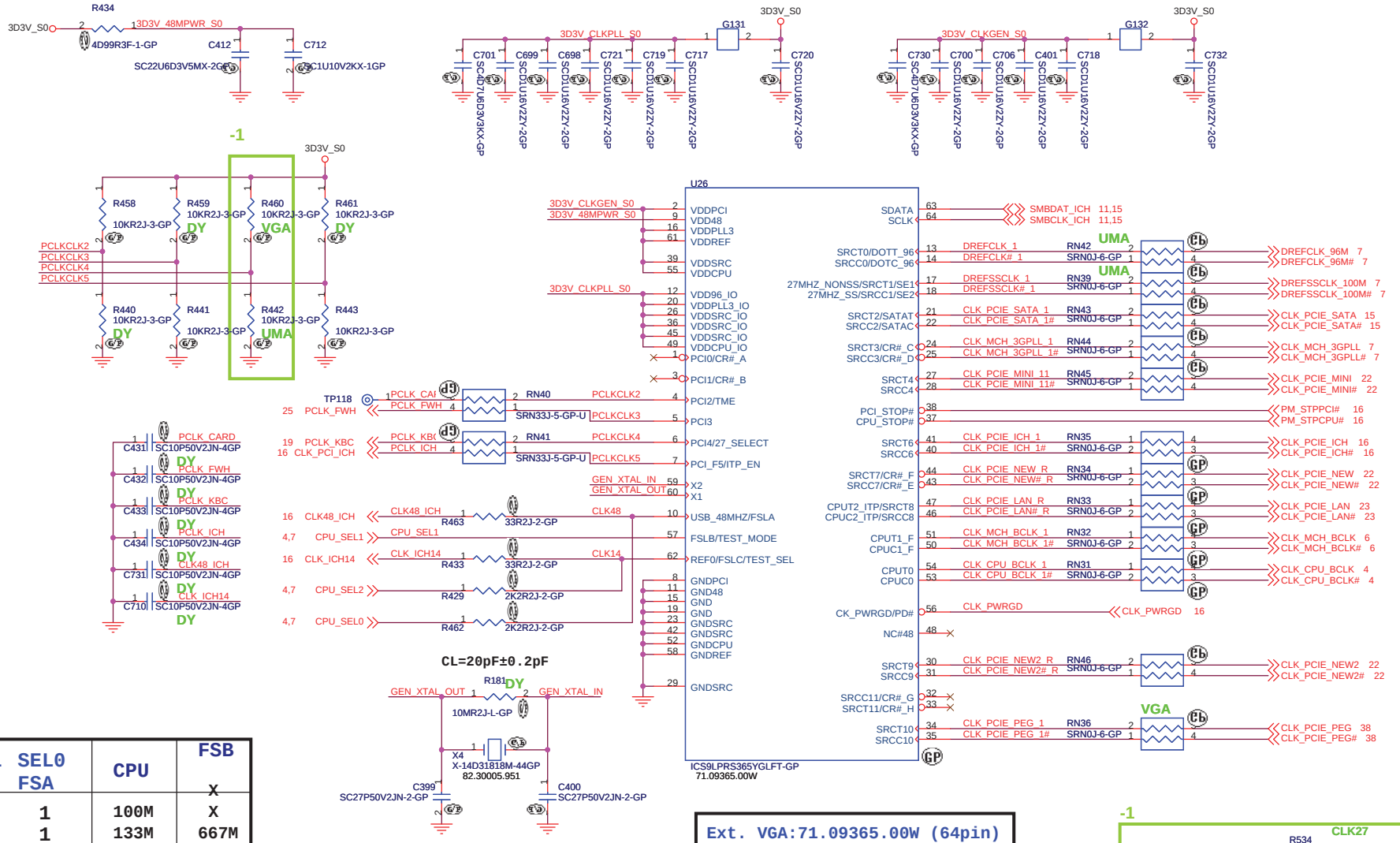
Title: **Reference**

Size: Custom | Document Number: C45/C46 | Rev: SA

Date: Wednesday, April 25, 2007 | Sheet 2 of 45



SEL2 FSC	SEL1 FSB	SEL0 FSA	CPU	FSB X
1	0	1	100M	X
0	0	1	133M	667M
0	1	1	166M	800M
0	1	0	200M	

PIN NAME	DESCRIPTION
PCI0/CR#_A	Byte 5, bit 7 0 = PCI0 enabled (default) 1= CR#_A enabled. Byte 5, bit 6 controls whether CR#_A controls SRC0 or SRC2 pair Byte 5, bit 6 0 = CR#_A controls SRC0 pair (default), 1= CR#_A controls SRC2 pair
PCI1/CR#_B	Byte 5, bit 5 0 = PCI1 enabled (default) 1= CR#_B enabled. Byte 5, bit 6 controls whether CR#_B controls SRC1 or SRC4 pair Byte 5, bit 4 0 = CR#_B controls SRC1 pair (default) 1= CR#_B controls SRC4 pair
PCI2/TME	0 = Overclocking of CPU and SRC Allowed 1 = Overclocking of CPU and SRC NOT allowed
PCI3/RC-5_EN	0 = Pin37 as CPU_STOP# , pin 38 as PCI_STOP#. 1 = Pins37,38 as SRC-5 differential pair.
PCI4/27M_SEL	0 = Pin17 as SRC-1, Pin18 as SRC-1#, Pin13 as DOT96, Pin14 as DOT96# 1 = Pin17 as 27MHz, Pin 18 as 27MHz_SS, Pin13 as SRC-0, Pin14 as SRC-0#
PCI_F5/ITP_EN	0 =SRC8/SRC8# 1 = ITP/ITP#

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Title: Clock Generator

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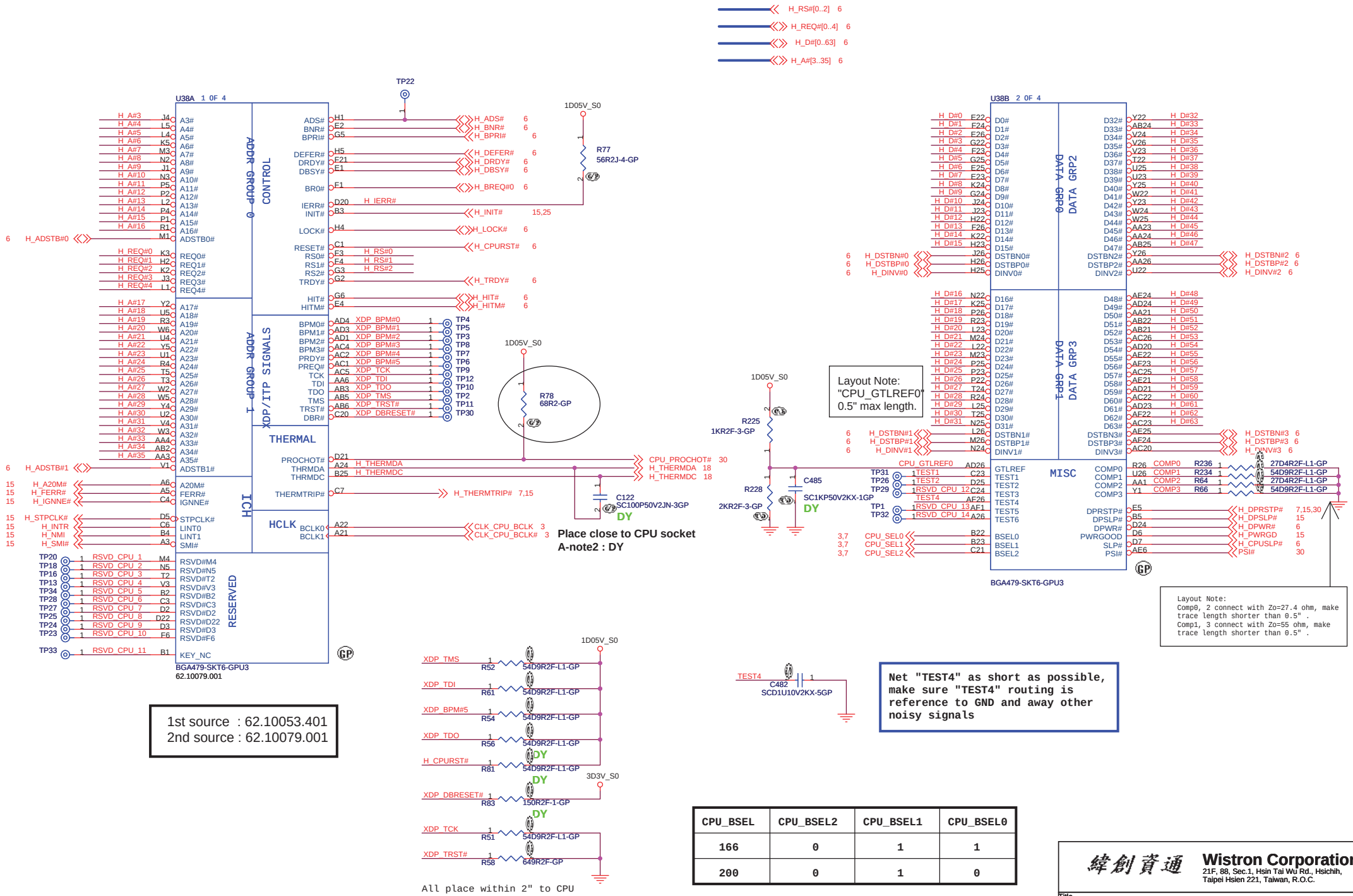
Date: Monday, May 07, 2007 | Sheet 3 of 45



CPU_BSEL	CPU_BSEL2	CPU_BSEL1	CPU_BSEL0
166	0	1	1
200	0	1	0

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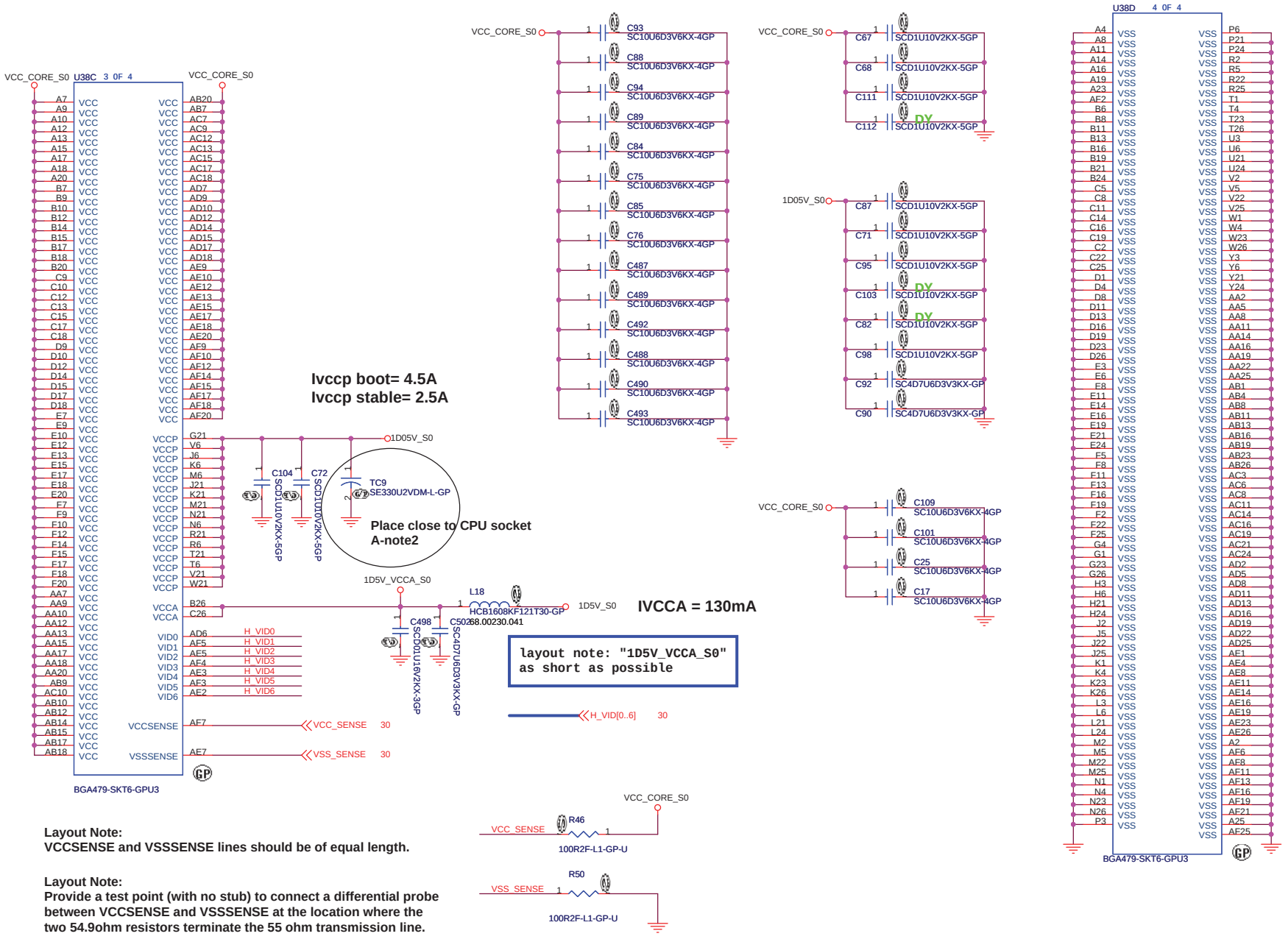
Title: **CPU (1 of 2) AGTL**

Size	Document Number	Rev
Custom	C45/C46	SA

Date: Wednesday, April 25, 2007 Sheet 4 of 45



Layout Note:
VCCSENSE and VSSSENSE lines should be of equal length.

Layout Note:
Provide a test point (with no stub) to connect a differential probe between VCCSENSE and VSSSENSE at the location where the two 54.9ohm resistors terminate the 55 ohm transmission line.

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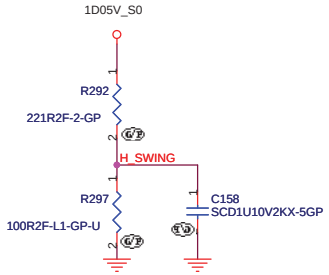
Title: ***CPU (2 of 2) POWER***

Size	Document Number	Rev
Custom	C45/C46	SA

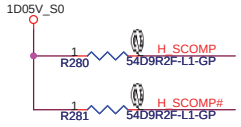
Date: Wednesday, April 25, 2007 Sheet 5 of 45

H_SWING routing Trace width and Spacing use 10 / 20 mil

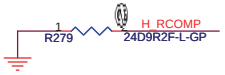
H_SWING Resistors and Capacitors close MCH 500 mil (MAX)



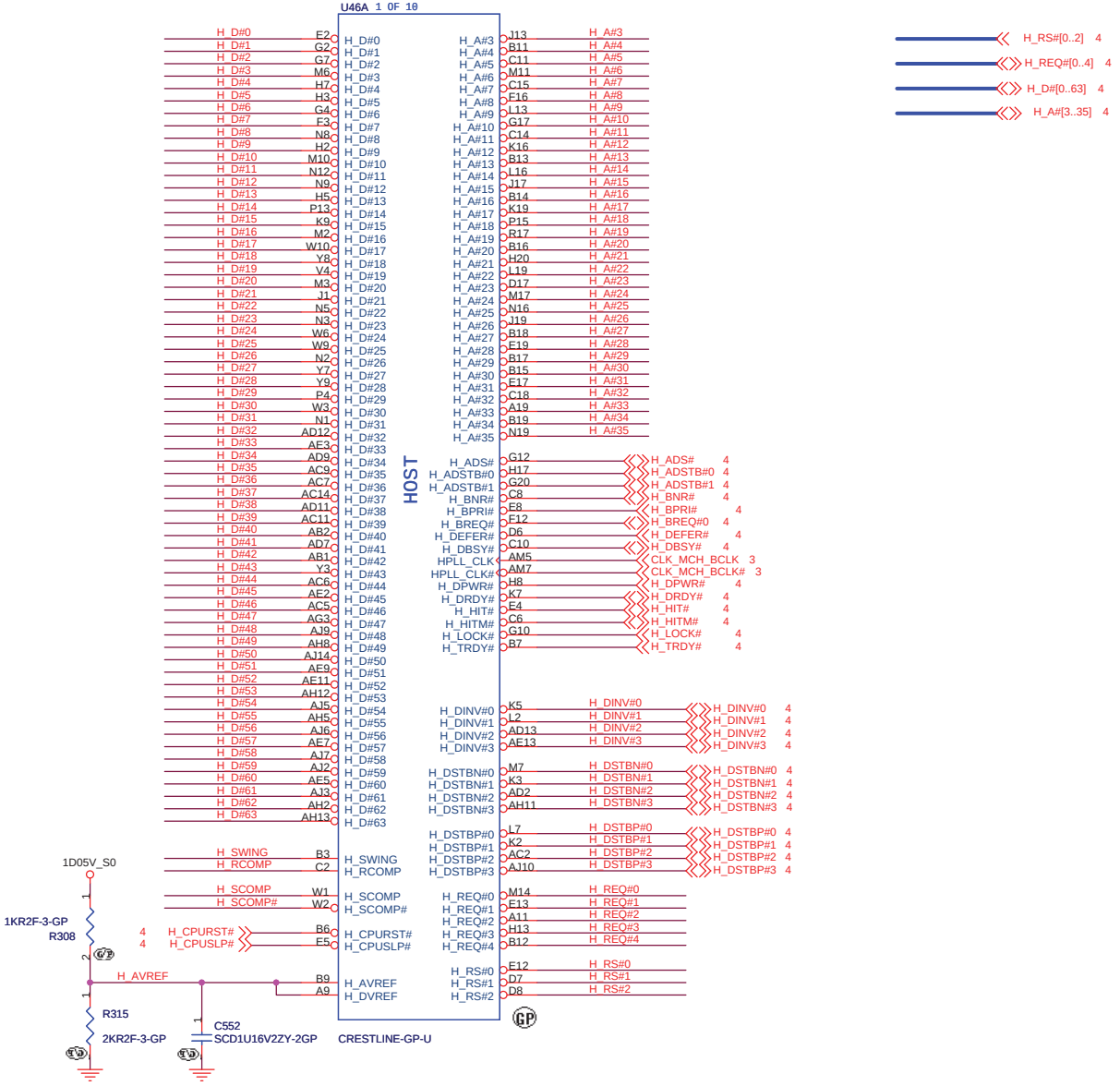
H_SCOMP and H_SCOMP# Resistors and Capacitors close MCH 500 mil (MAX)



H_RCOMP routing Trace width and Spacing use 10 / 20 mil



Place them near to the chip (< 0.5")



H_REF Decoupling Crestline close Crestline 100 mil

965GM (71.GM965.00U)
965PM (71.PM965.00U)

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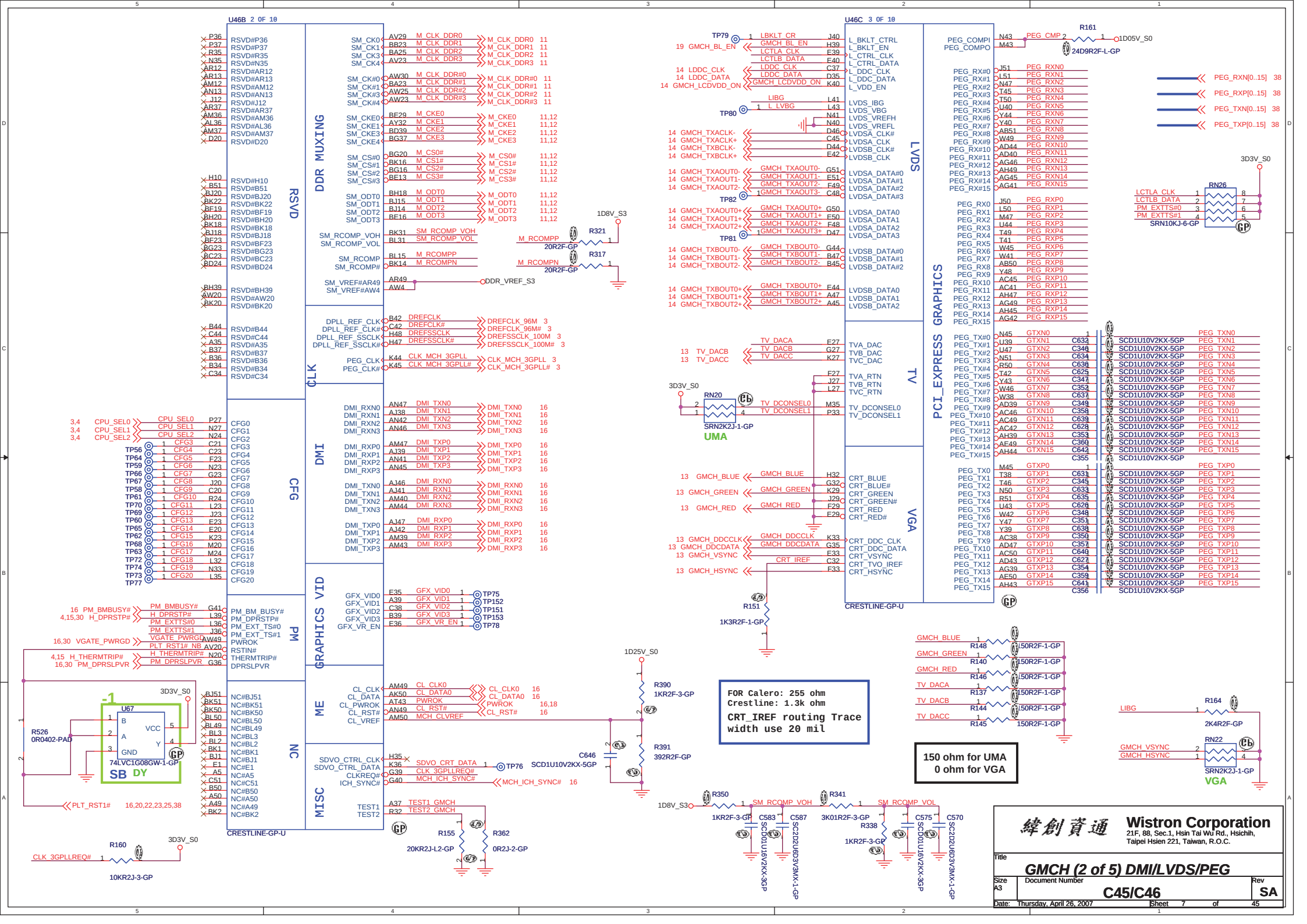
Title: **GMCH (1 of 5) AGTL**

Size: Custom | Document Number: **C45/C46** | Rev: **SA**

Date: Wednesday, April 25, 2007 | Sheet 6 of 45


U46B 2 OF 10
RSVD
DDR MUXING
CLK
DMI
CFG
GRAPHICS VID
PM
ME
MISC
NC
CRESTLINE-GP-U
U46C 3 OF 10
LVDS
TV
VGA
PCI_EXPRESS GRAPHICS
CRESTLINE-GP-U
UMA
VGA
SB DY
FOR Calero: 255 ohm
Crestline: 1.3k ohm
CRT_IREF routing Trace width use 20 mil
150 ohm for UMA
0 ohm for VGA
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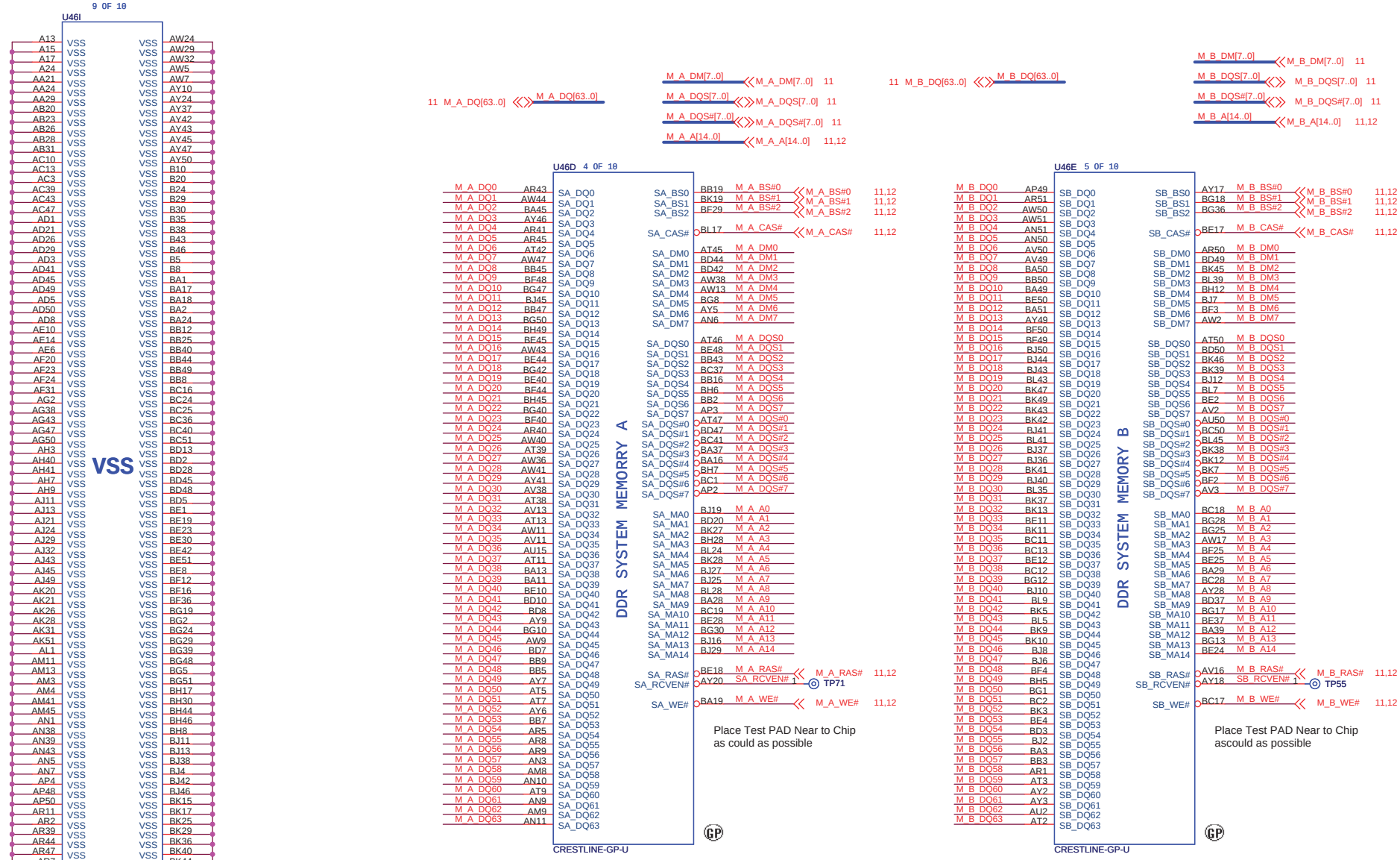
Title
GMCH (2 of 5) DMI/LVDS/PEG
Size A3
Document Number
C45/C46
Rev SA
Date: Thursday, April 26, 2007
Sheet 7 of 45



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Title: GMCH (3 of 5) MEMORY	
Size: Custom	Document Number: C45/C46
Rev: SA	
Date: Wednesday, April 25, 2007	Sheet 8 of 45

VCC_NCTF + VCC=1573mA

VCC_AXG_NCTF + VCC_AXG=7700mA

1573mA

3138mA

POWER

VCC CORE

VCC SM

VCC GFX NCTF

VCC GFX

VCC SM LF

FOR VCC CORE AND VCC NCTF

308 mils from the Edge
Coupling CAP

VCC NCTF

VSS NCTF

VSS SCB

VSS AXM

VSS AXM NCTF

VCC_AXM_NCTF + VCC_AXM=540mA

Place on the Edge

FOR VCC SM

Place CAP where LVDS and DDR2 taps
Place on the Edge

VSS

CRESTLINE-GP-U

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Title: GMCH (4 of 5) POWER1

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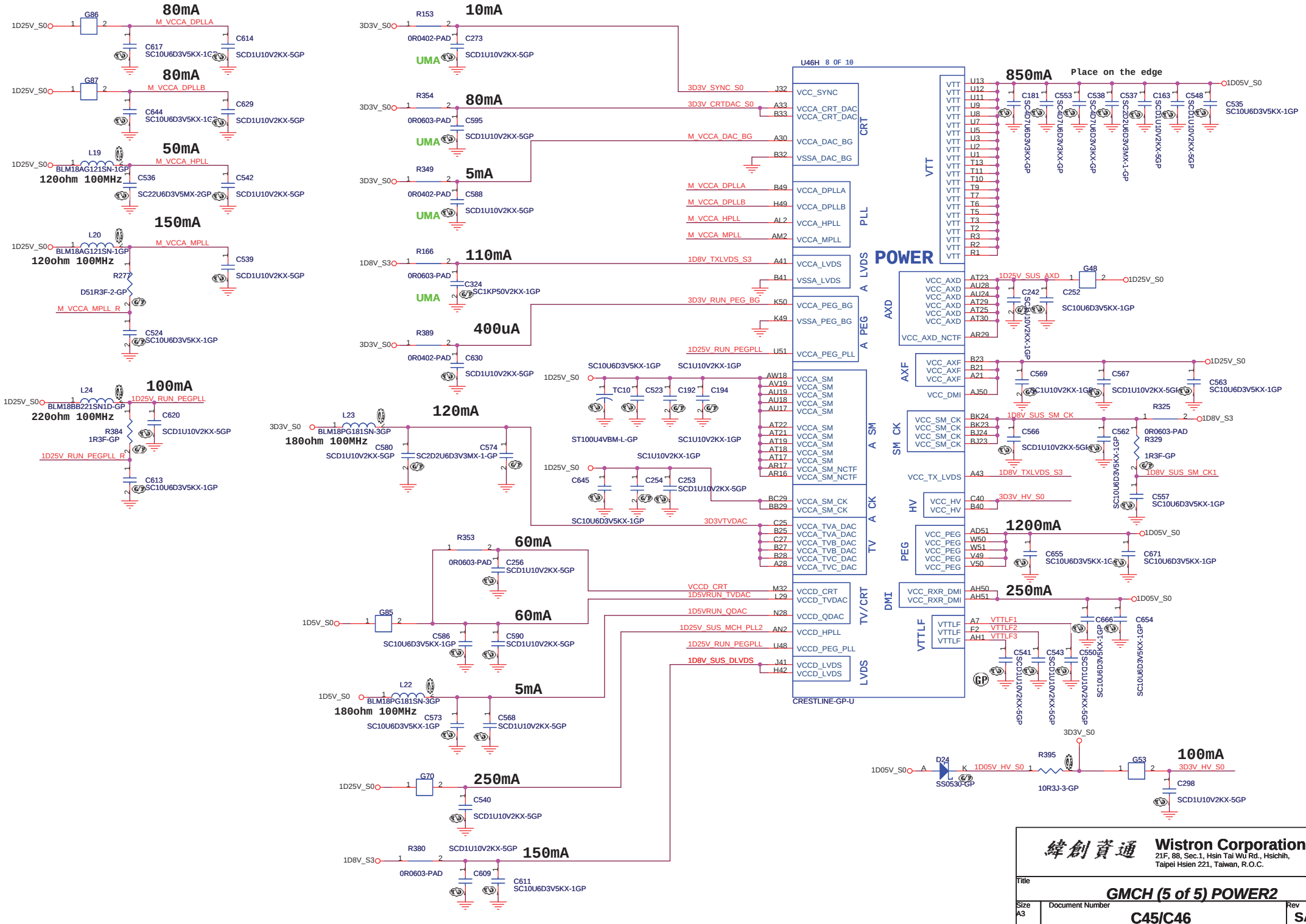
Date: Monday, April 23, 2007 | Sheet 9 of 45



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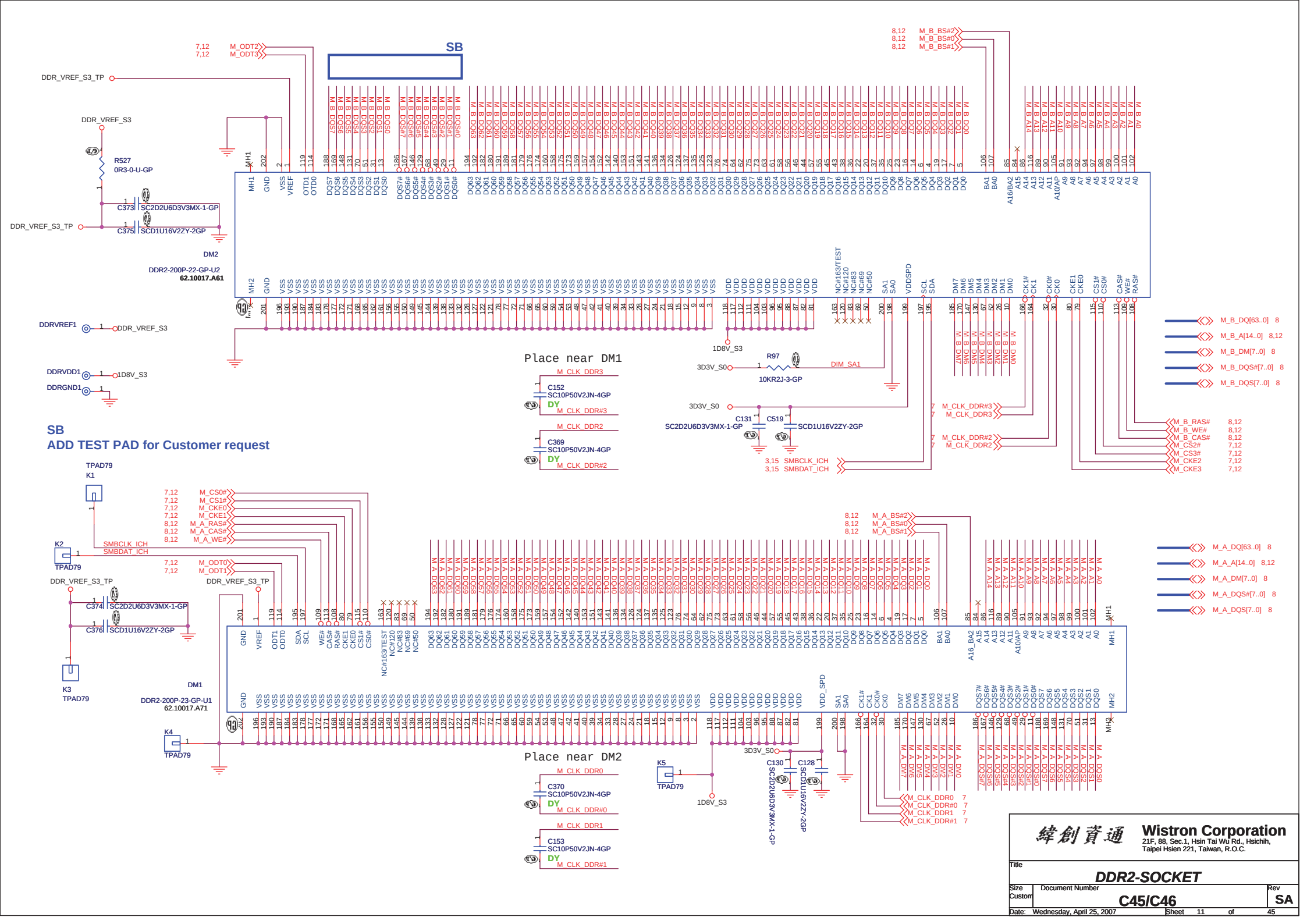
Title: GMCH (5 of 5) POWER2

Size	Document Number	Rev
A3	C45/C46	SA

Date: Tuesday, April 24, 2007 Sheet 10 of 45


SB
DDR_VREF_S3_TP
DDR_VREF_S3
R527
0R3-0-U-GP
C373
SC2D2U6D3V3MX-1-GP
C375
SCD1U16V2ZY-2GP
DM2
DDR2-200P-22-GP-U2
62.10017.A61
DDRVREF1
DDRVDD1
DDRGND1
1D8V_S3
3D3V_S0
R97
10KR2J-3-GP
DIM_SA1
Place near DM1
M_CLK_DDR3
C152
SC10P50V2JN-4GP
DY
M_CLK_DDR#3
M_CLK_DDR2
C369
SC10P50V2JN-4GP
DY
M_CLK_DDR#2
C131
C519
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
3,15 SMBCLK_ICH
3,15 SMBDAT_ICH
M_B_DQ[63..0] 8
M_B_A[14..0] 8,12
M_B_DM[7..0] 8
M_B_DQS#[7..0] 8
M_B_DQS[7..0] 8
SB
ADD TEST PAD for Customer request
TPAD79
K1
K2
K3
K4
K5
SMBCLK_ICH
SMBDAT_ICH
C374
SC2D2U6D3V3MX-1-GP
C376
SCD1U16V2ZY-2GP
DM1
DDR2-200P-23-GP-U1
62.10017.A71
Place near DM2
M_CLK_DDR0
C370
SC10P50V2JN-4GP
DY
M_CLK_DDR#0
M_CLK_DDR1
C153
SC10P50V2JN-4GP
DY
M_CLK_DDR#1
C130
C128
SC2D2U6D3V3MX-1-GP
SCD1U16V2ZY-2GP
M_A_DQ[63..0] 8
M_A_A[14..0] 8,12
M_A_DM[7..0] 8
M_A_DQS#[7..0] 8
M_A_DQS[7..0] 8
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Title
DDR2-SOCKET
Size
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Document Number
C45/C46
Rev
SA
Date: Wednesday, April 25, 2007
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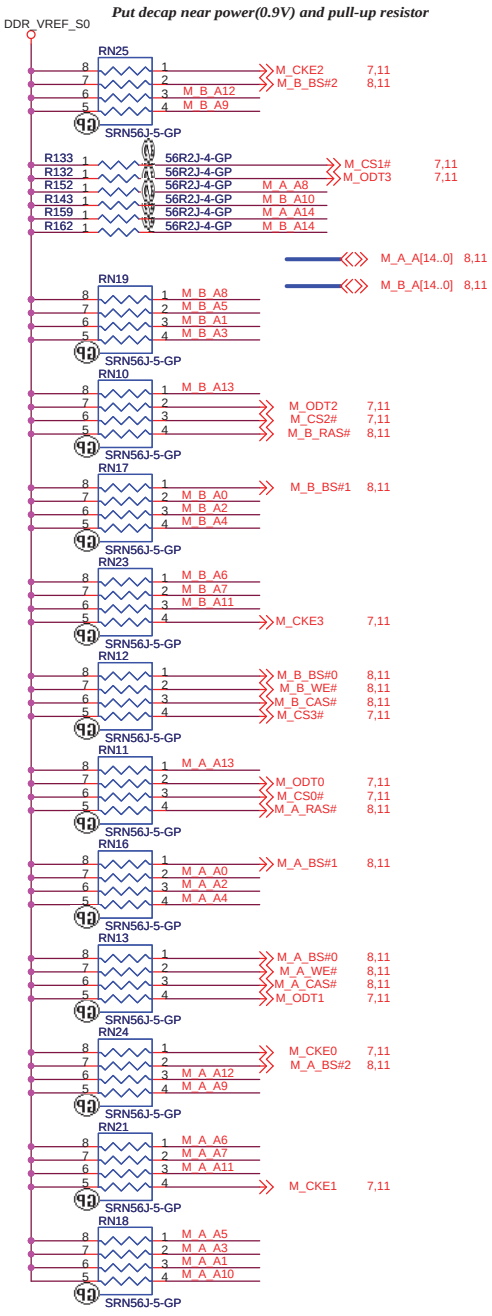
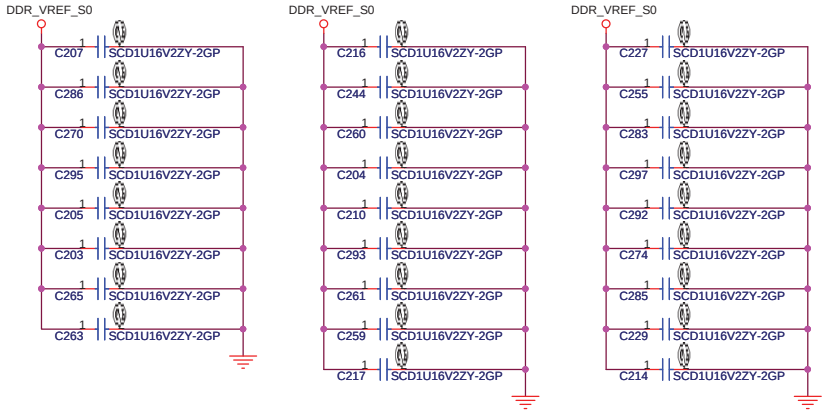
PARALLEL TERMINATION

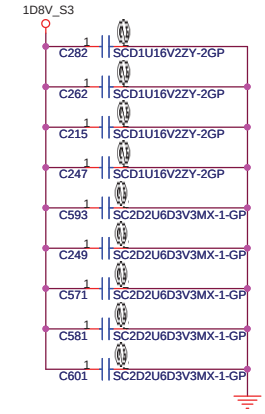


Decoupling Capacitor

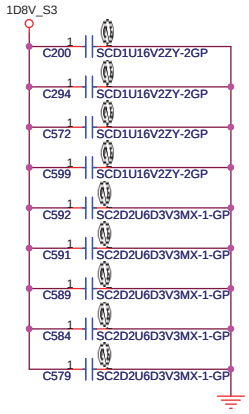
Put decap near power(0.9V) and pull-up resistor



Place these Caps near DM1



Place these Caps near DM2



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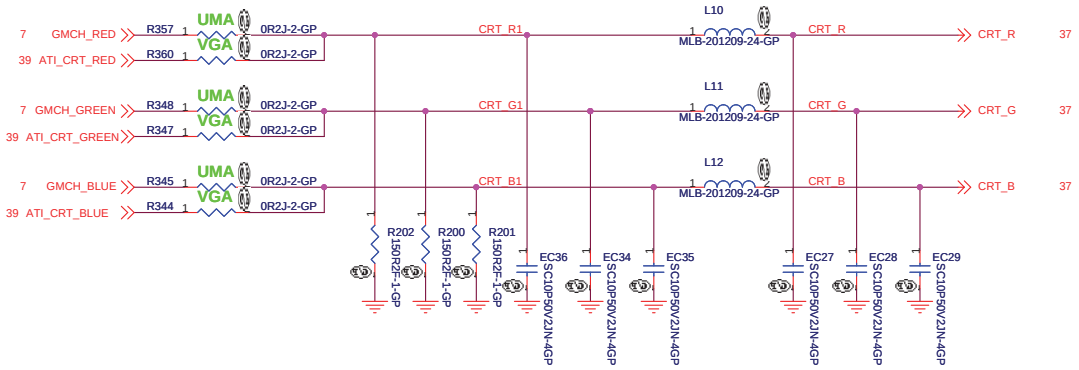
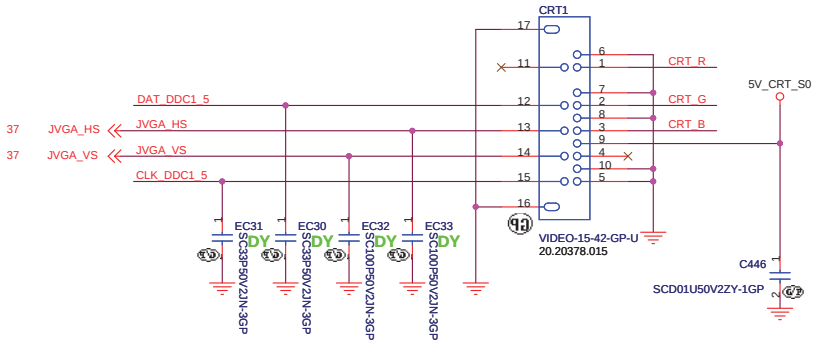
Title: DDR2-RESISTOR&CAPACITOR
Size: Custom | Document Number: C45/C46 | Rev: SA
Date: Wednesday, April 25, 2007 | Sheet 12 of 45

CRT CONNECTOR

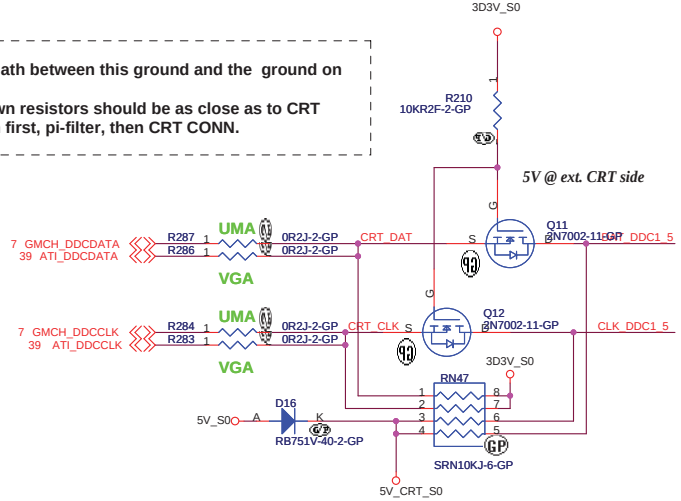
Layout Note:
Place these resistors close to the CRT-out connector

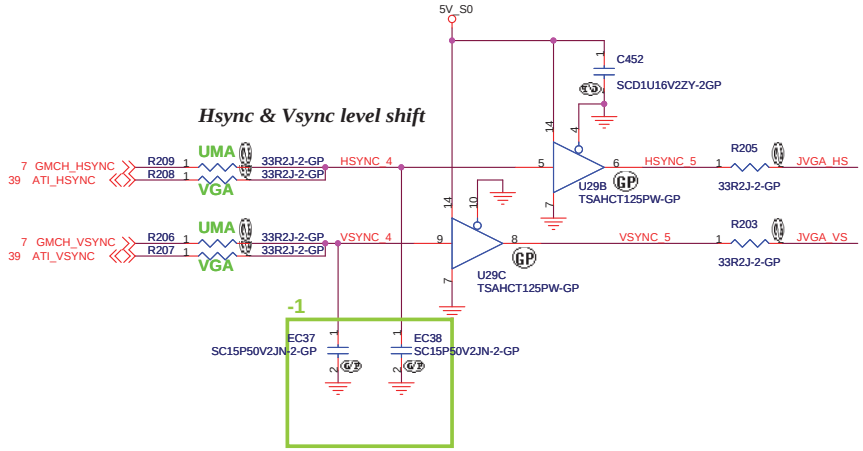
SB
Change L10, L11, L12 the same as X40



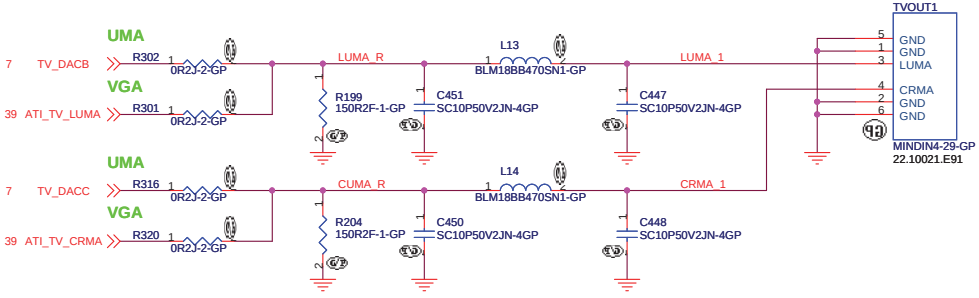


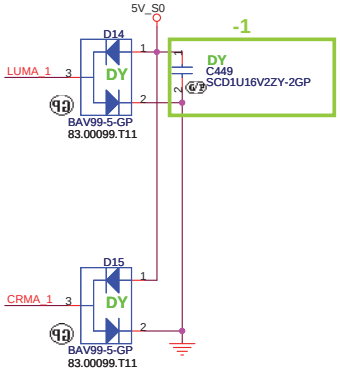
Layout Note:
*** Must be a ground return path between this ground and the ground on the VGA connector.**
Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.





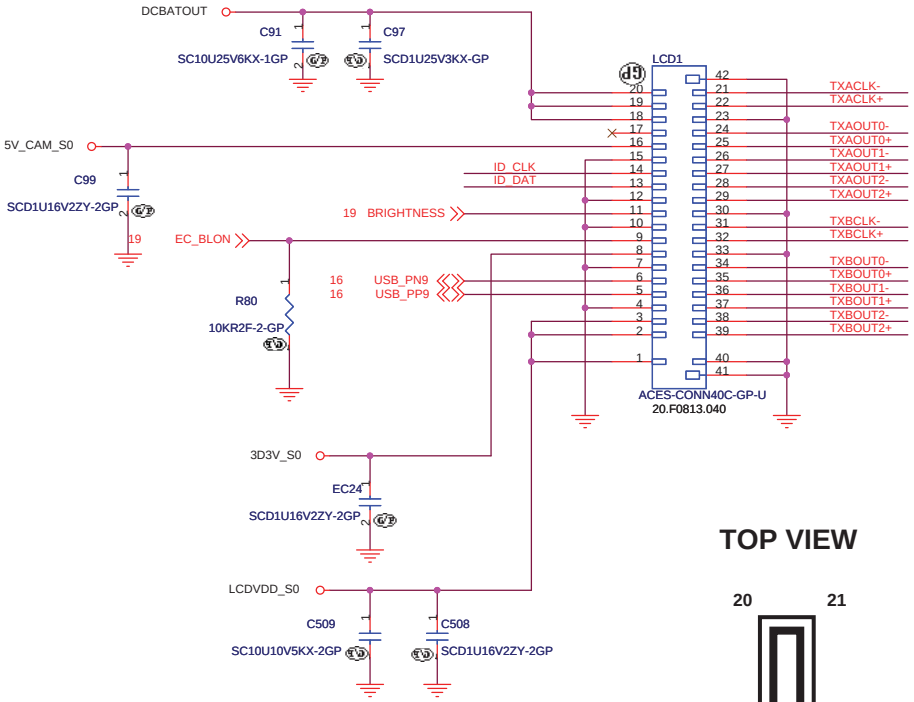
S-VIDEO CONNECTOR



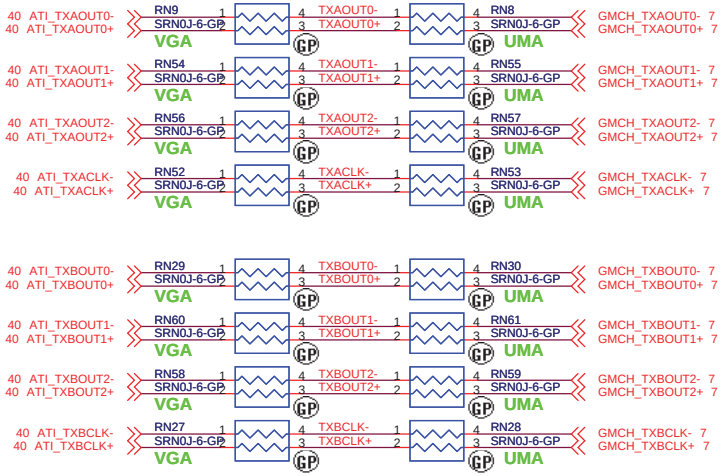


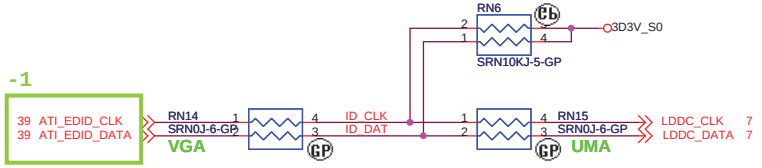
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***CRT/S-Video***	
Size: Custom	Document Number: **C45/C46**	Rev: **-1**
Date: Friday, April 27, 2007	Sheet 13 of 45	

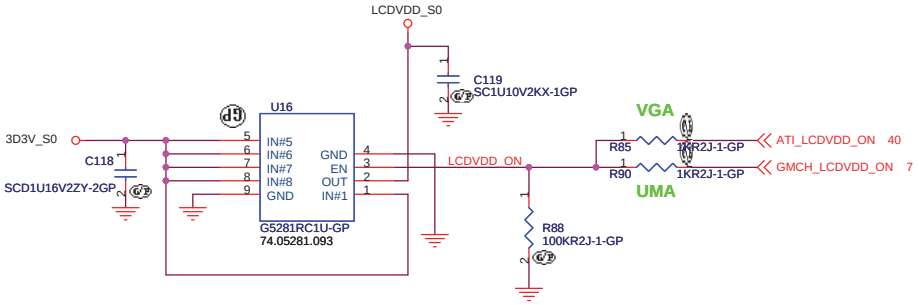
LCD CONNECTOR



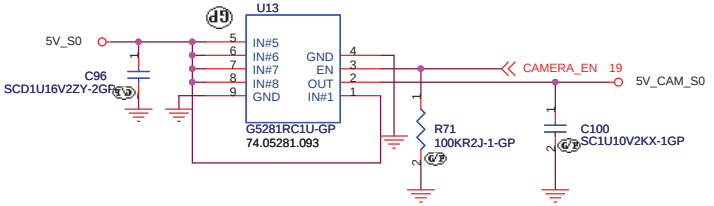
TOP VIEW







CAMERA POWER



緯創資通 Wistron Corporation
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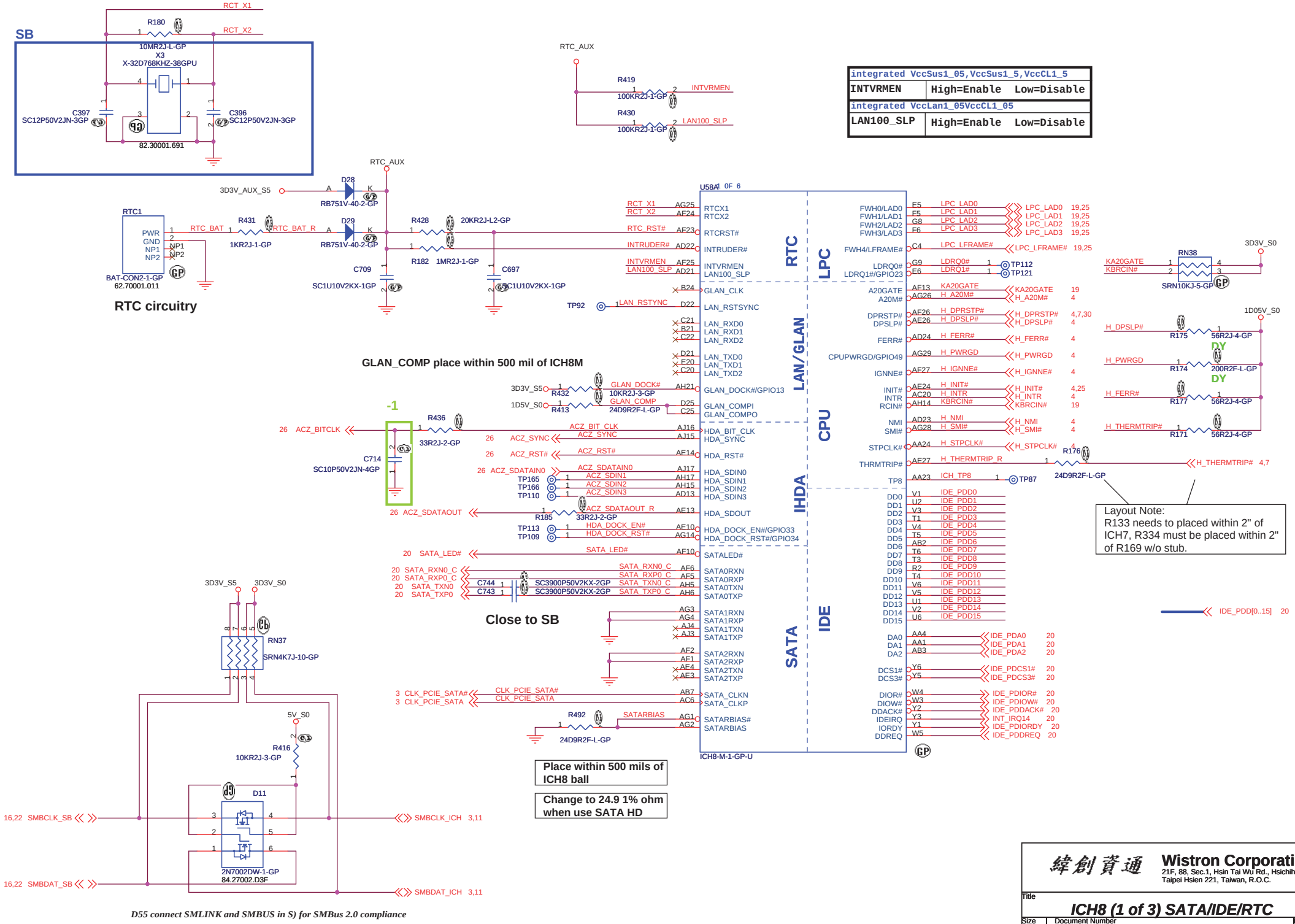
Title	LCD/DVI CONN	
Size A3	Document Number C45/C46	Rev SA
Date: Thursday, April 26, 2007	Sheet 14 of 45	


SB
RCT_X1
RCT_X2
R180
10MR2J-L-GP
X3
X-32D768KHZ-38GPU
C397
SC12P50V2JN-3GP
C396
SC12P50V2JN-3GP
82.30001.691
RTC_AUX
R419
100KR2J-1-GP
INTVRMEN
R430
100KR2J-1-GP
LAN100_SLP
integrated VccSus1_05,VccSus1_5,VccCL1_5
INTVRMEN High=Enable Low=Disable
integrated VccLan1_05VccCL1_05
LAN100_SLP High=Enable Low=Disable
RTC1
BAT-CON2-1-GP
62.70001.011
RTC_BAT
R431
1KR2J-1-GP
RTC_BAT_R
D28
RB751V-40-2-GP
D29
RB751V-40-2-GP
3D3V_AUX_S5
R428
20KR2J-L2-GP
R182
1MR2J-1-GP
C709
SC1U10V2KX-1GP
C697
SC1U10V2KX-1GP
RTC circuitry
U58A 1 OF 6
RTCX1
RTCX2
RTCRST#
INTRUDER#
INTVRMEN
LAN100_SLP
RTC
LPC
GLAN_CLK
LAN_RSTSYNC
LAN_RXD0
LAN_RXD1
LAN_RXD2
LAN_TXD0
LAN_TXD1
LAN_TXD2
GLAN_DOCK#/GPIO13
GLAN_COMPI
GLAN_COMPO
LAN/GLAN
GLAN_COMP place within 500 mil of ICH8M
R432
10KR2J-3-GP
R413
24D9R2F-L-GP
GLAN_DOCK#
GLAN_COMP
HDA_BIT_CLK
HDA_SYNC
HDA_RST#
HDA_SDIN0
HDA_SDIN1
HDA_SDIN2
HDA_SDIN3
HDA_SDOUT
HDA_DOCK_EN#/GPIO33
HDA_DOCK_RST#/GPIO34
CPU
IHDA
-1
R436
33R2J-2-GP
C714
SC10P50V2JN-4GP
R185
33R2J-2-GP
SATALED#
SATA0RXN
SATA0RXP
SATA0TXN
SATA0TXP
SATA1RXN
SATA1RXP
SATA1TXN
SATA1TXP
SATA2RXN
SATA2RXP
SATA2TXN
SATA2TXP
SATA_CLKN
SATA_CLKP
SATARBIAS#
SATARBIAS
SATA
IDE
C744
C743
SC3900P50V2KX-2GP
Close to SB
R492
24D9R2F-L-GP
Place within 500 mils of ICH8 ball
Change to 24.9 1% ohm when use SATA HD
ICH8-M-1-GP-U
FWH0/LAD0
FWH1/LAD1
FWH2/LAD2
FWH3/LAD3
FWH4/LFRAME#
LDRQ0#
LDRQ1#/GPIO23
A20GATE
A20M#
DPRSTP#
DPSLP#
FERR#
CPUPWRGD/GPIO49
IGNNE#
INIT#
INTR
RCIN#
NMI
SMI#
STPCLK#
THRMTRIP#
TP8
DD0
DD1
DD2
DD3
DD4
DD5
DD6
DD7
DD8
DD9
DD10
DD11
DD12
DD13
DD14
DD15
DA0
DA1
DA2
DCS1#
DCS3#
DIOR#
DIOW#
DDACK#
IDEIRQ
IORDY
DDREQ
LPC_LAD0
LPC_LAD1
LPC_LAD2
LPC_LAD3
LPC_LFRAME#
TP112
TP121
KA20GATE
H_A20M#
H_DPRSTP#
H_DPSLP#
H_FERR#
H_PWRGD
H_IGNNE#
H_INIT#
H_INTR
KBRCIN#
H_NMI
H_SMI#
H_STPCLK#
H_THERMTRIP_R
ICH_TP8
TP87
IDE_PDD0
IDE_PDD1
IDE_PDD2
IDE_PDD3
IDE_PDD4
IDE_PDD5
IDE_PDD6
IDE_PDD7
IDE_PDD8
IDE_PDD9
IDE_PDD10
IDE_PDD11
IDE_PDD12
IDE_PDD13
IDE_PDD14
IDE_PDD15
IDE_PDA0
IDE_PDA1
IDE_PDA2
IDE_PDCS1#
IDE_PDCS3#
IDE_PDIOR#
IDE_PDIOW#
IDE_PDDACK#
INT_IRQ14
IDE_PDIORDY
IDE_PDDREQ
R176
24D9R2F-L-GP
H_THERMTRIP# 4,7
Layout Note:
R133 needs to placed within 2" of ICH7, R334 must be placed within 2" of R169 w/o stub.
IDE_PDD[0..15] 20
RN38
SRN10KJ-5-GP
R175
56R2J-4-GP
R174
200R2F-L-GP
R177
56R2J-4-GP
R171
56R2J-4-GP
DY
1D05V_S0
3D3V_S0
RN37
SRN4K7J-10-GP
R416
10KR2J-3-GP
5V_S0
D11
2N7002DW-1-GP
84.27002.D3F
16,22 SMBCLK_SB
16,22 SMBDAT_SB
SMBCLK_ICH 3,11
SMBDAT_ICH 3,11
D55 connect SMLINK and SMBUS in S) for SMBus 2.0 compliance
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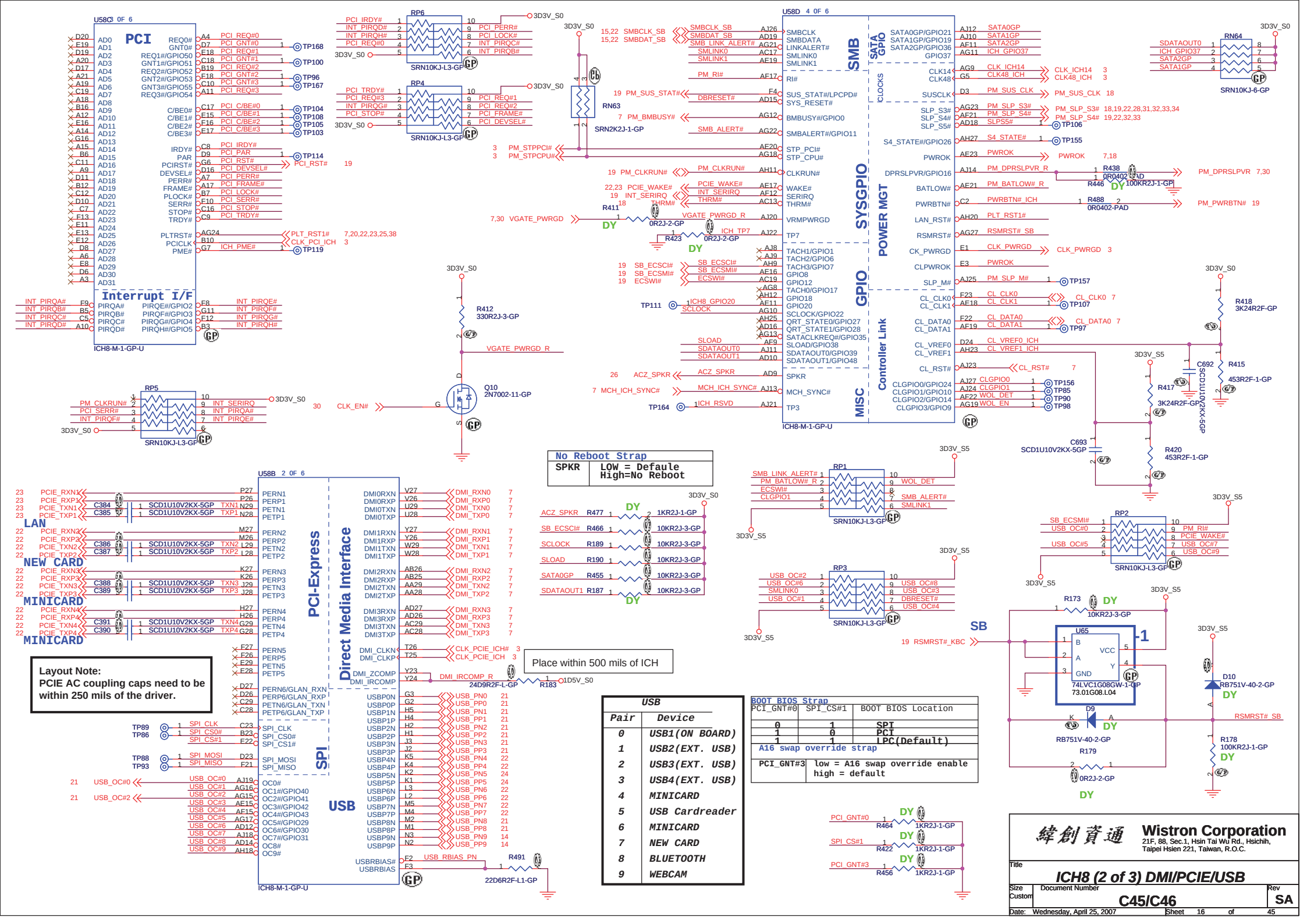
Title
ICH8 (1 of 3) SATA/IDE/RTC
Size Custom
Document Number
C45/C46
Rev
SA
Date: Friday, April 27, 2007
Sheet 15 of 45


U58C 3 OF 6
PCI
Interrupt I/F
ICH8-M-1-GP-U
U58D 4 OF 6
SMB
SATA GPIO
CLOCKS
POWER MGT
SYSGPIO
GPIO
Controller Link
MISC
ICH8-M-1-GP-U
U58B 2 OF 6
PCI-Express
Direct Media Interface
SPI
USB
ICH8-M-1-GP-U
No Reboot Strap
SPKR | LOW = Defaule High=No Reboot
USB
Pair | Device
0 USB1(ON BOARD)
1 USB2(EXT. USB)
2 USB3(EXT. USB)
3 USB4(EXT. USB)
4 MINICARD
5 USB Cardreader
6 MINICARD
7 NEW CARD
8 BLUETOOTH
9 WEBCAM
BOOT BIOS Strap
PCI_GNT#0 | SPI_CS#1 | BOOT BIOS Location
0 | 1 | SPI
1 | 0 | PCI
1 | 1 | LPC(Default)
A16 swap override strap
PCI_GNT#3 | low = A16 swap override enable high = default
Layout Note:
PCIE AC coupling caps need to be within 250 mils of the driver.
Place within 500 mils of ICH
LAN
NEW CARD
MINICARD
MINICARD
SB
Wistron Corporation
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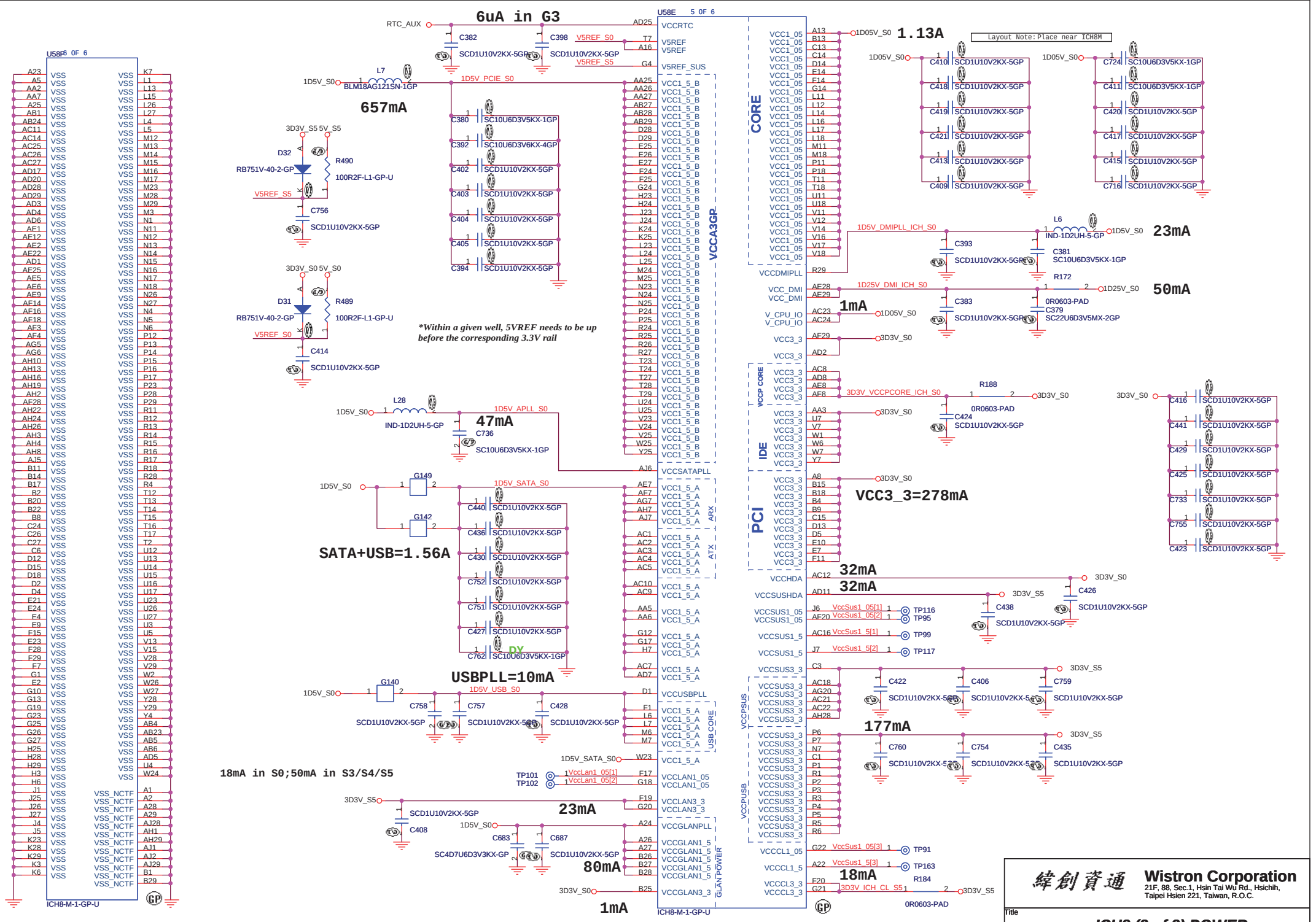
Title
ICH8 (2 of 3) DMI/PCIE/USB
Size Custom
Document Number
C45/C46
Rev SA
Date: Wednesday, April 25, 2007
Sheet 16 of 45


6uA in G3
1.13A
657mA
23mA
50mA
1mA
*Within a given well, 5VREF needs to be up before the corresponding 3.3V rail
47mA
SATA+USB=1.56A
VCC3_3=278mA
32mA
32mA
USBPLL=10mA
177mA
18mA in S0;50mA in S3/S4/S5
23mA
80mA
1mA
18mA
ICH8-M-1-GP-U
Layout Note: Place near ICH8M
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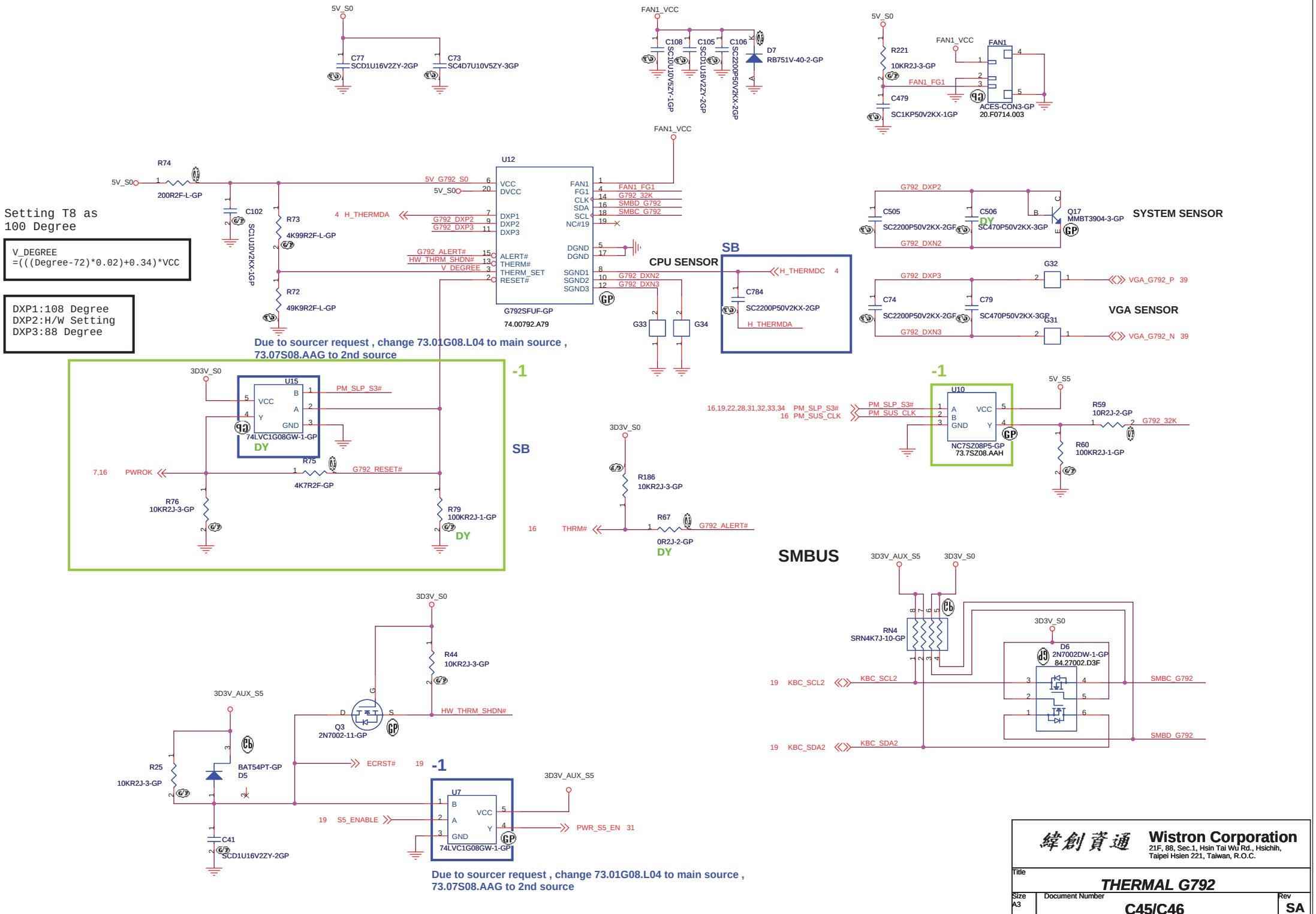
ICH8 (3 of 3) POWER
C45/C46
SA
Tuesday, April 24, 2007
17 of 45



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Title: THERMAL G792

Size	Document Number	Rev
A3	C45/C46	SA

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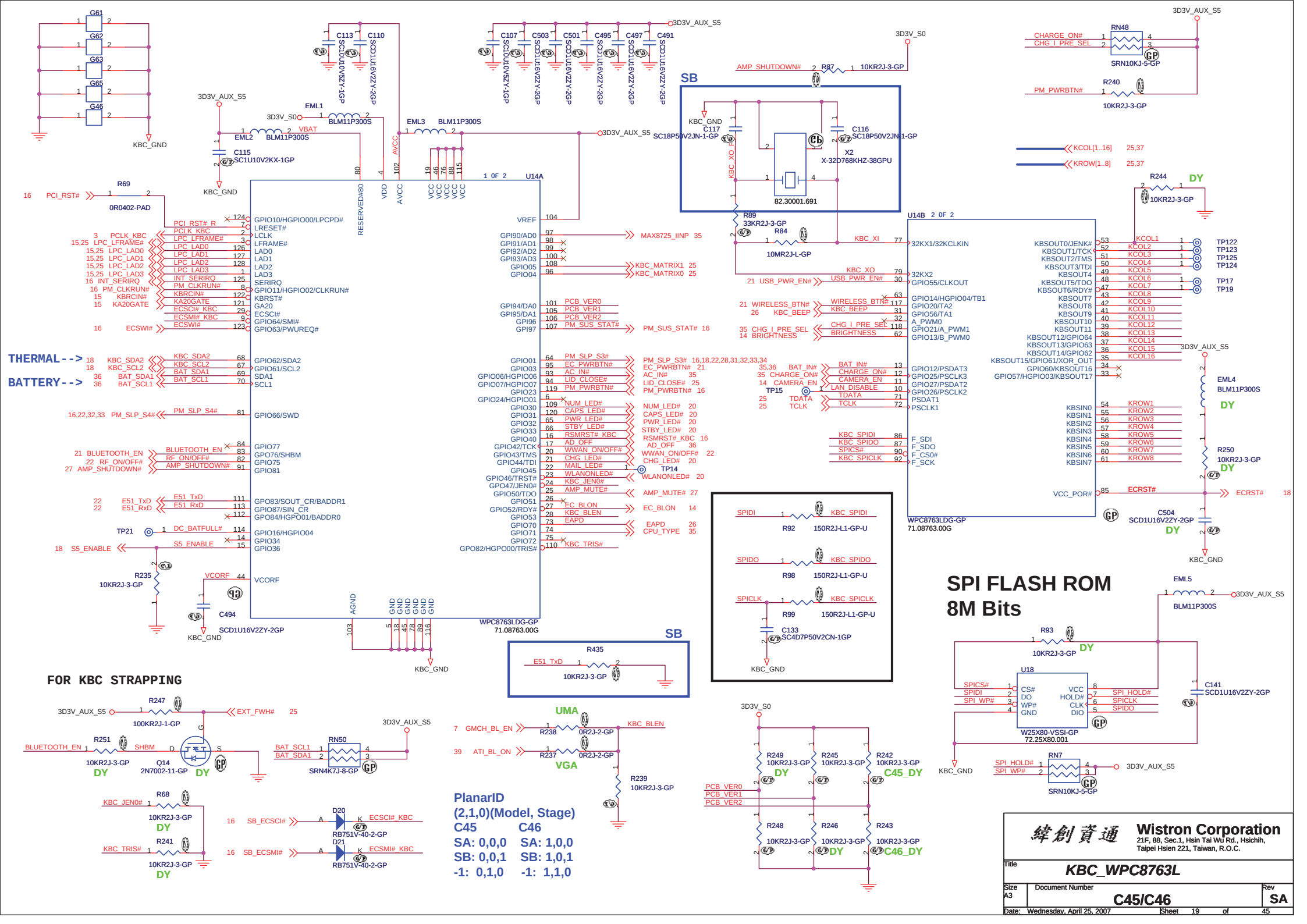
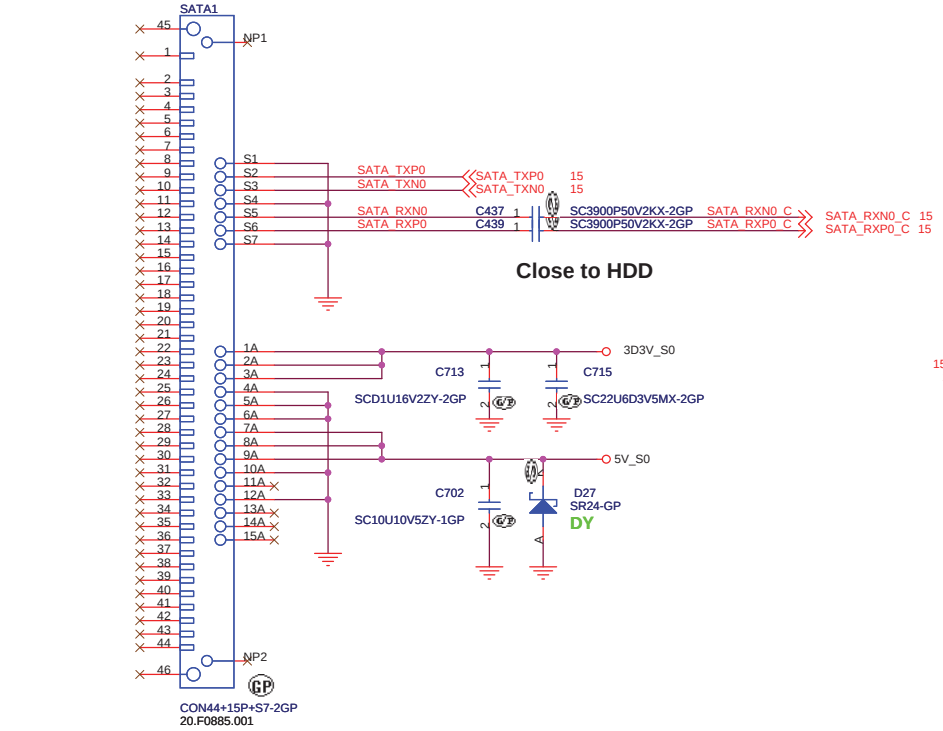
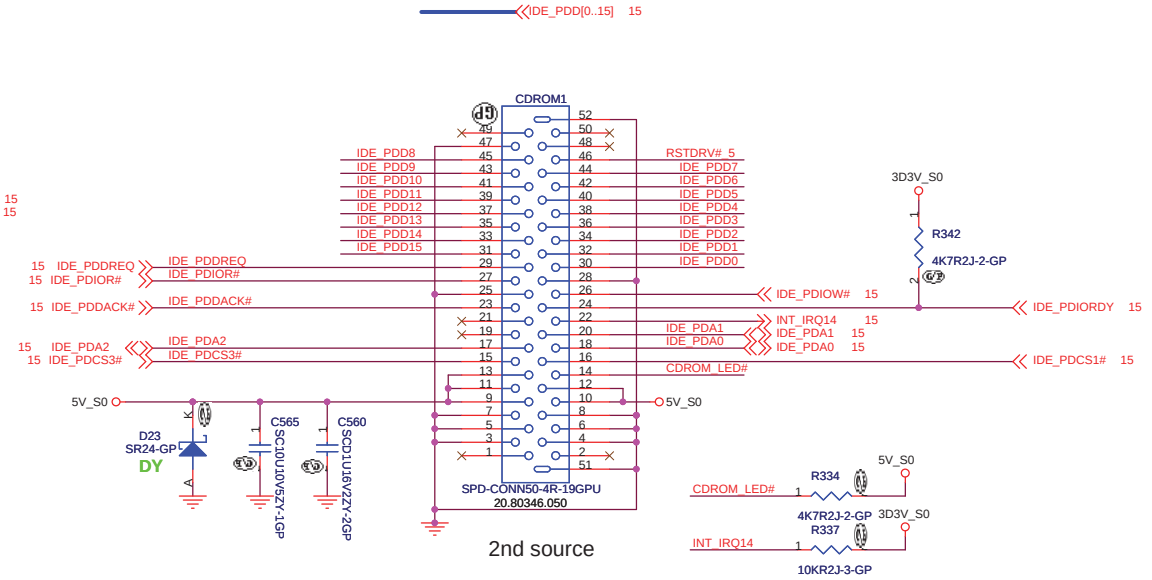

THERMAL - - >
BATTERY - - >
SB
FOR KBC STRAPPING
SPI FLASH ROM
8M Bits
UMA
VGA
PlanarID
(2,1,0)(Model, Stage)
C45 C46
SA: 0,0,0 SA: 1,0,0
SB: 0,0,1 SB: 1,0,1
-1: 0,1,0 -1: 1,1,0
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
KBC_WPC8763L
C45/C46
SA
Wednesday, April 25, 2007
19
45

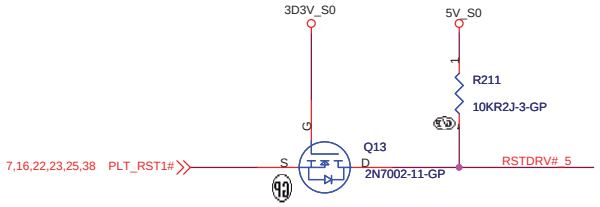
SATA HDD Connector

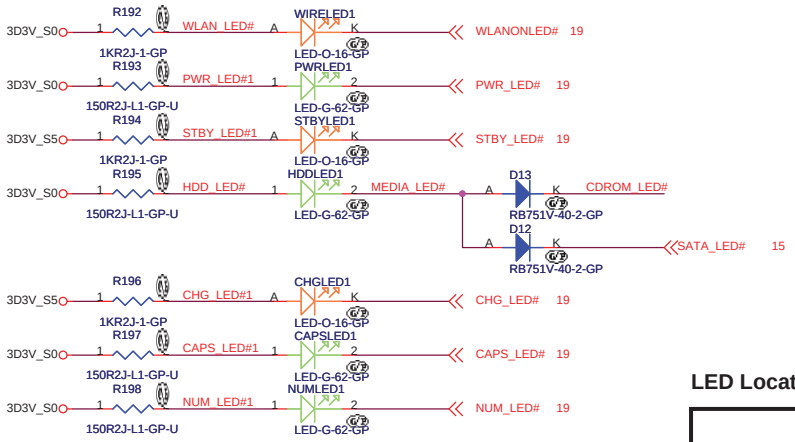


CD-ROM CONNECTOR

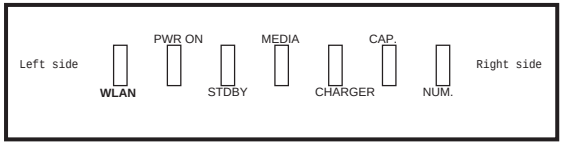


PCIRST# 3V to 5V level shift for HDD & CDROM





LED Location and Sequence (The edge of PCB,Top view)



緯創資通
Wistron Corporation
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Title: **HDD/CDROM/LED**

Size	Document Number	Rev
Custom	C45/C46	SA

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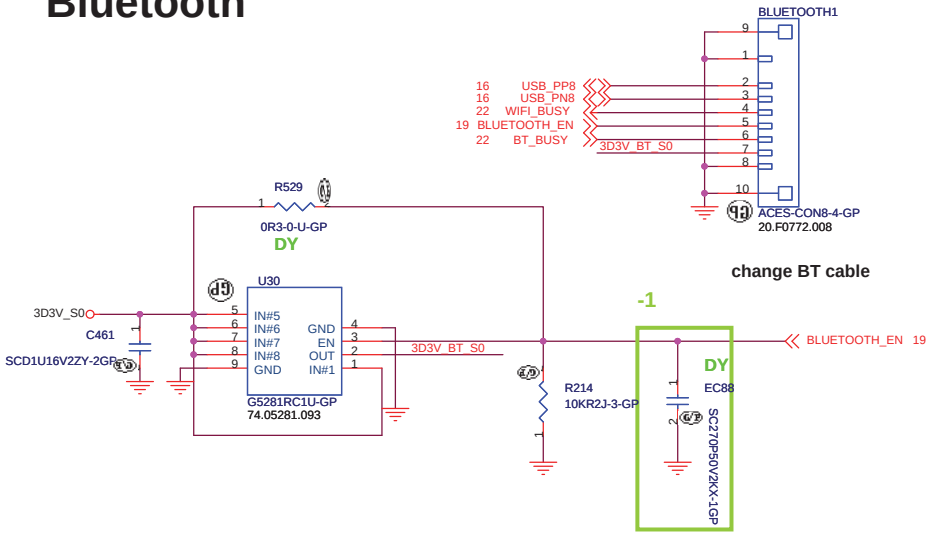
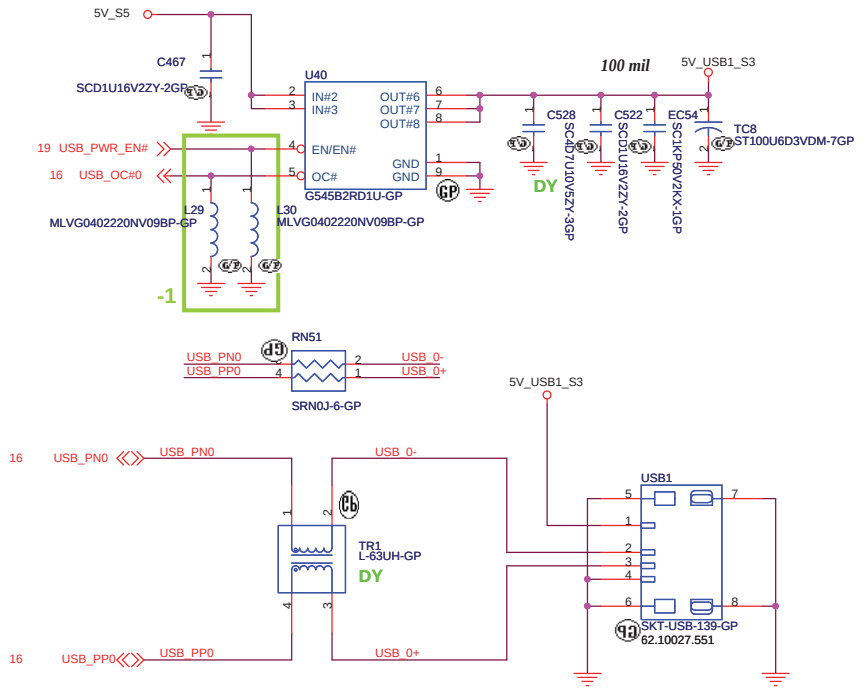
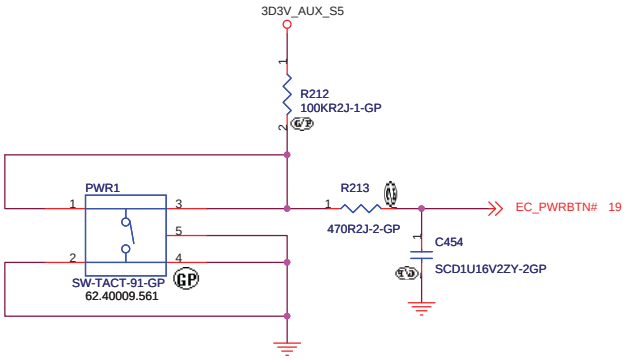
Bluetooth



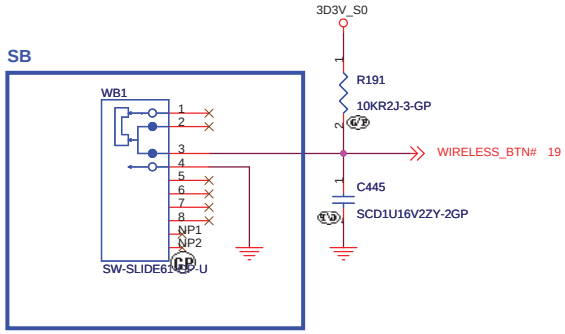
USB PORT



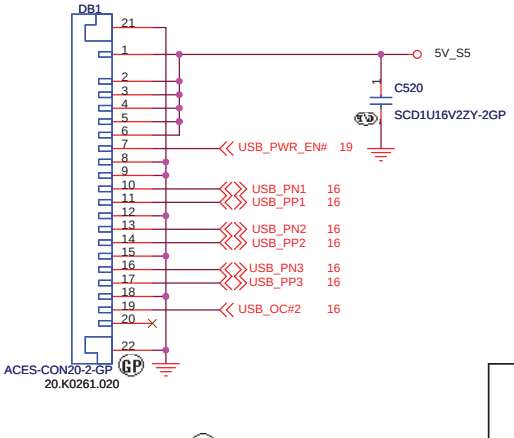
LAUNCH BOTTON



WIRELESS BOTTON



USB BOARD CONN



緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: USB/BT/DB/LAUNCH

Size: Custom | Document Number: C45/C46 | Rev: SA

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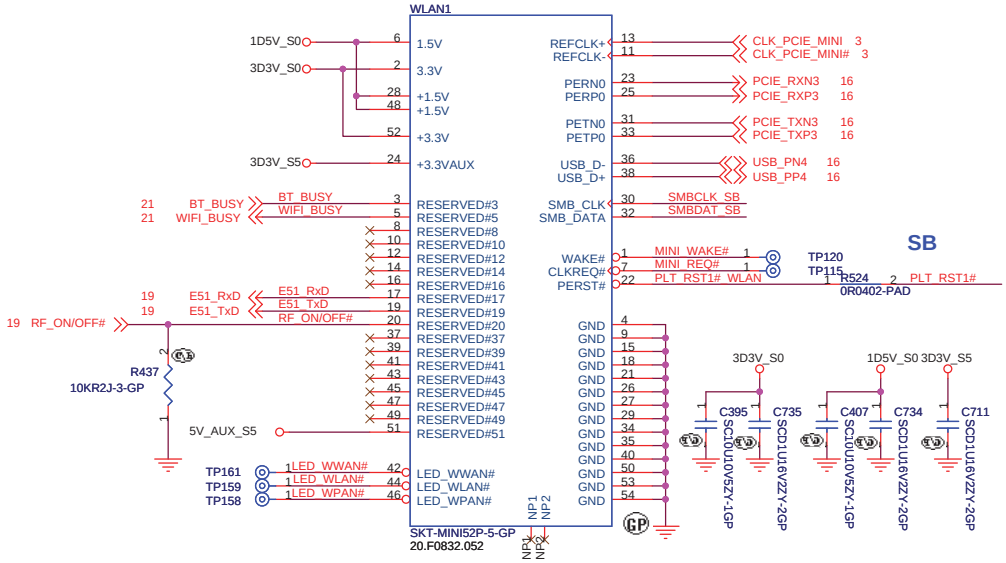
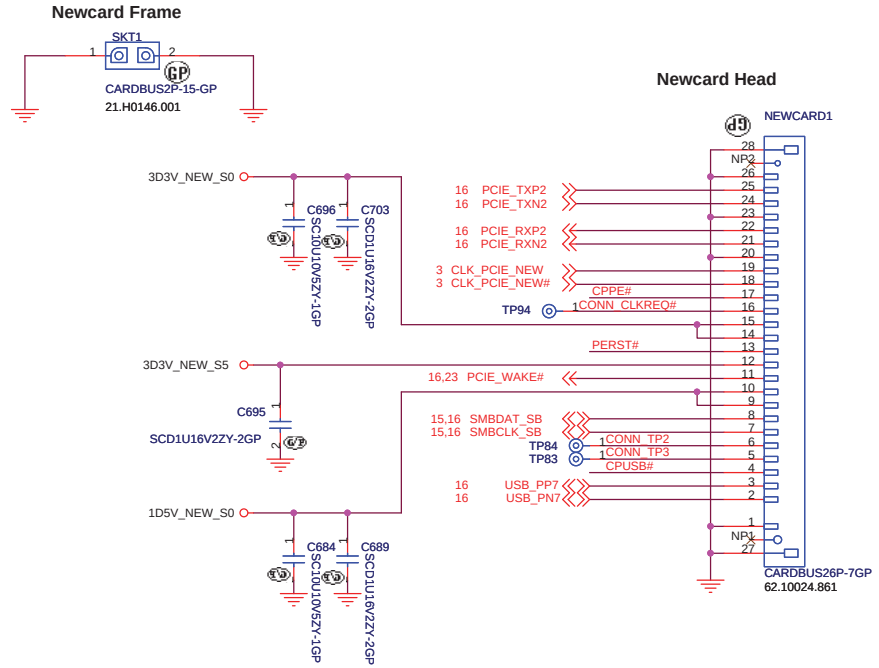
Mini Card Connector

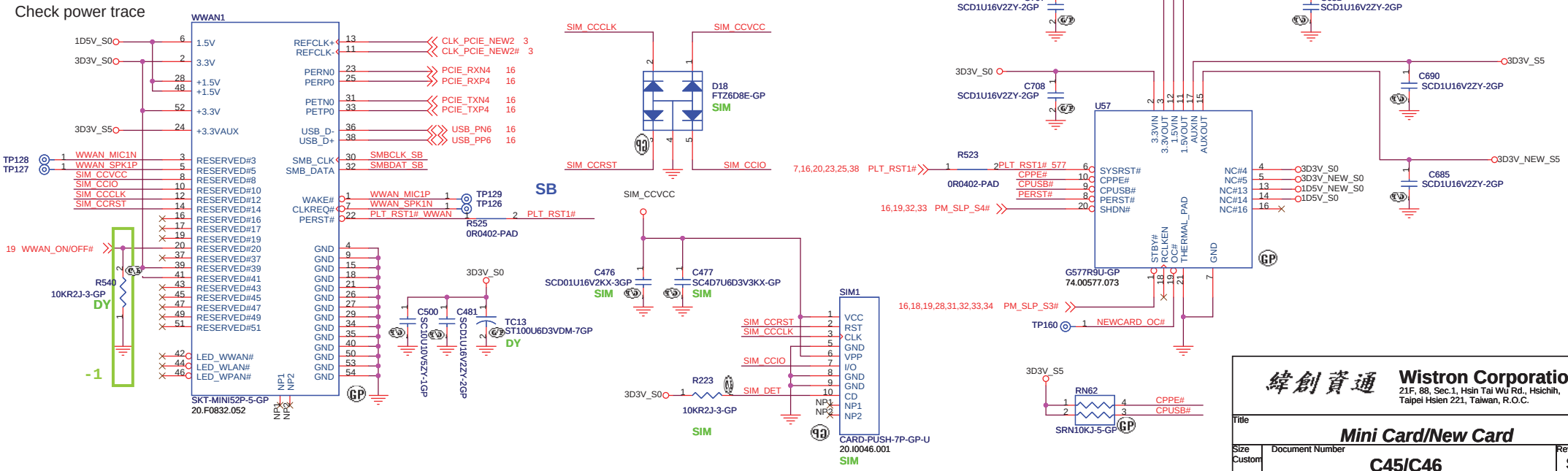


NEWCARD Connector



WWAN Connector

Check power trace



Place them Near to Chip

緯創資通 Wistron Corporation
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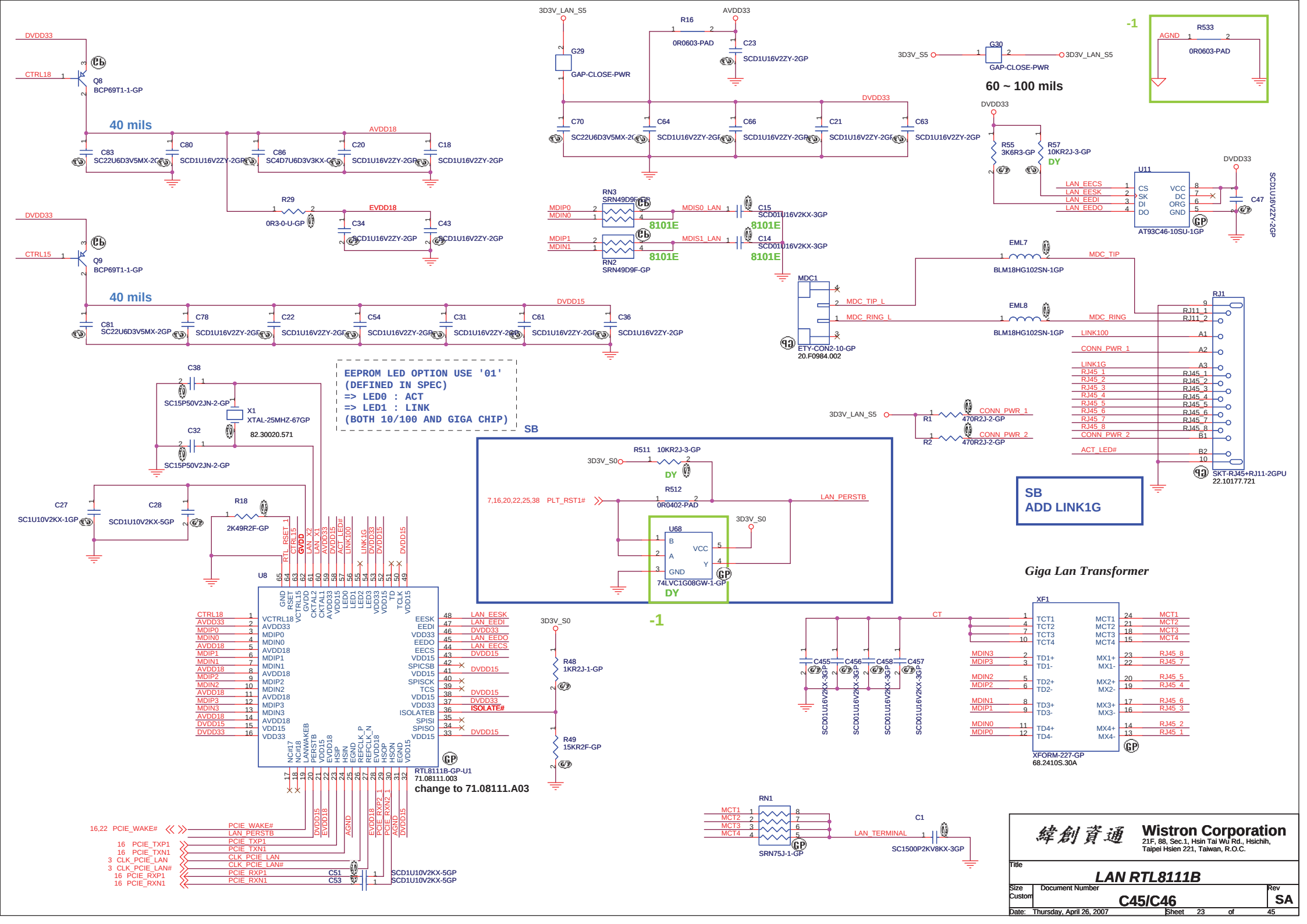
Taipei Hsien 221, Taiwan, R.O.C.

Title: **Mini Card/New Card**

Size	Document Number	Rev
Custom	C45/C46	SA

Date: Thursday, April 26, 2007 Sheet 22 of 45

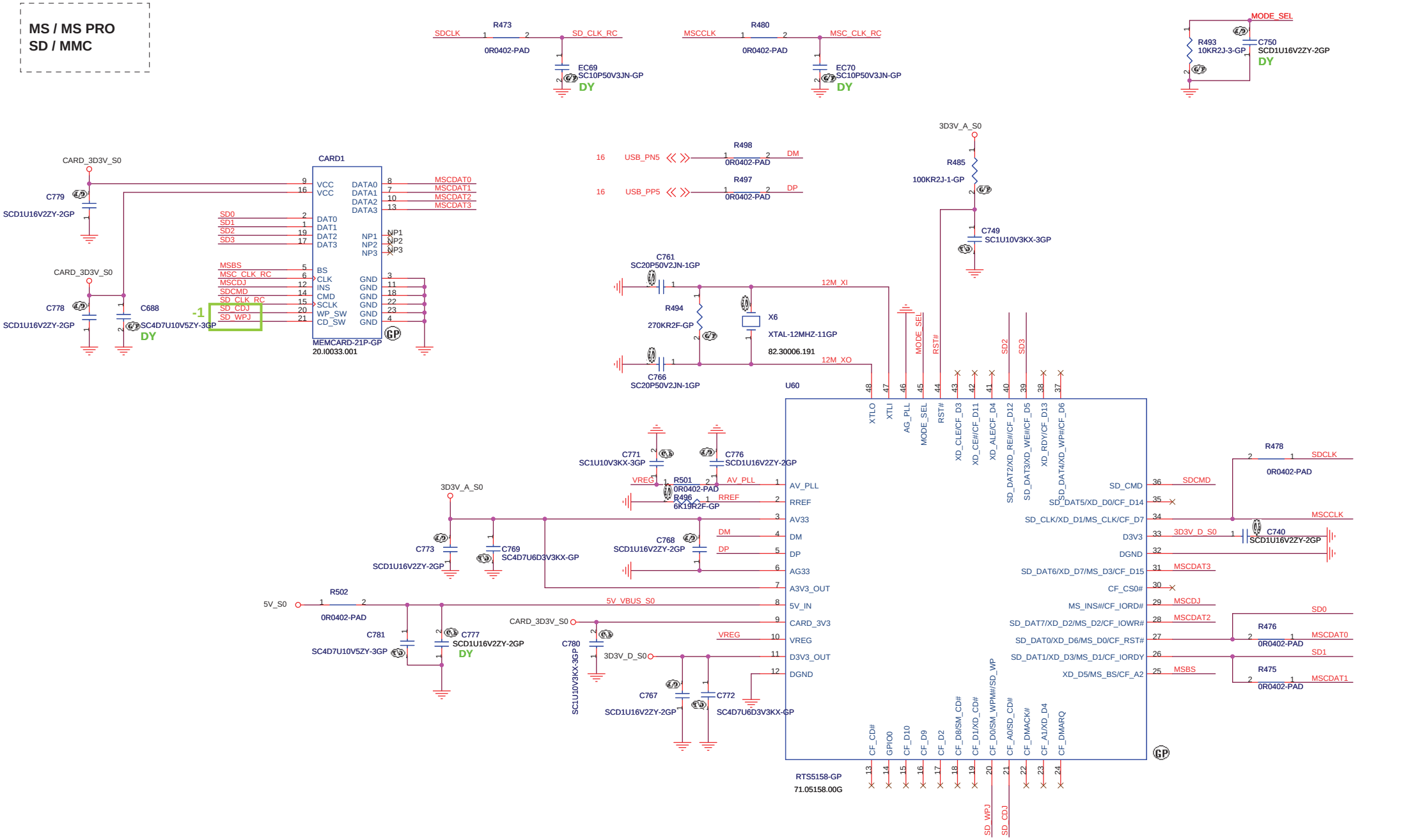


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **LAN RTL8111B**

Size	Document Number	Rev
Custom	C45/C46	SA

Date: Thursday, April 26, 2007 Sheet 23 of 45



緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title
USB Card Reader Controller

Size	Document Number	Rev
Custom	C45/C46	SA

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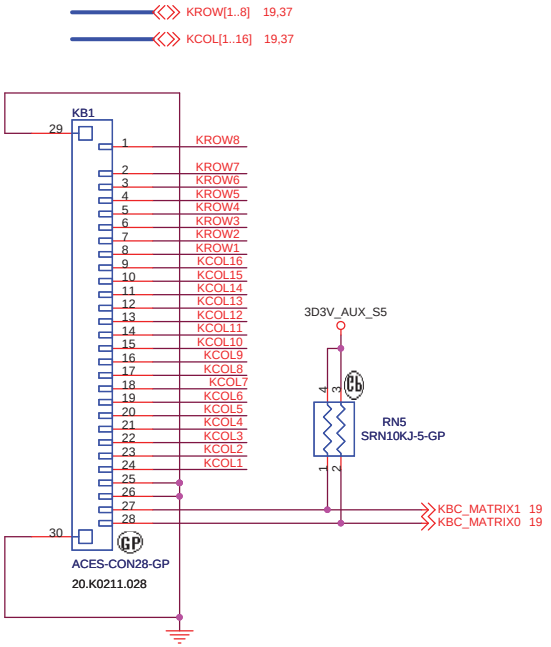
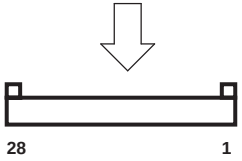
Internal KeyBoard Connector



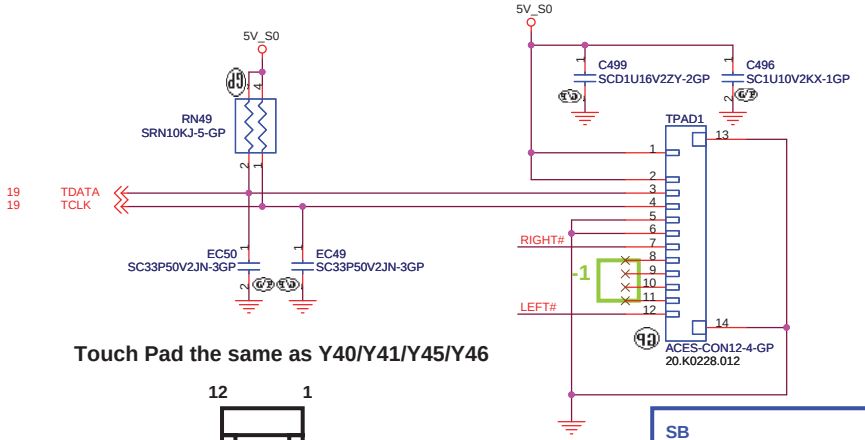
KEYBOARD MARTIX the same as Y40/Y41/Y45/Y46

Keyboard matrix (from vendor)

	US	Eur	Jap	Ohter
MATRIXID0#	1	0	1	0
MATRIXID1#	1	1	0	0



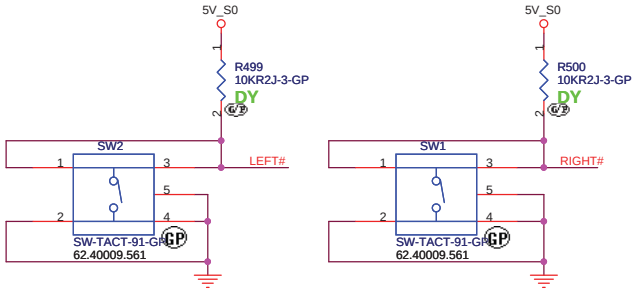
TouchPad Connector



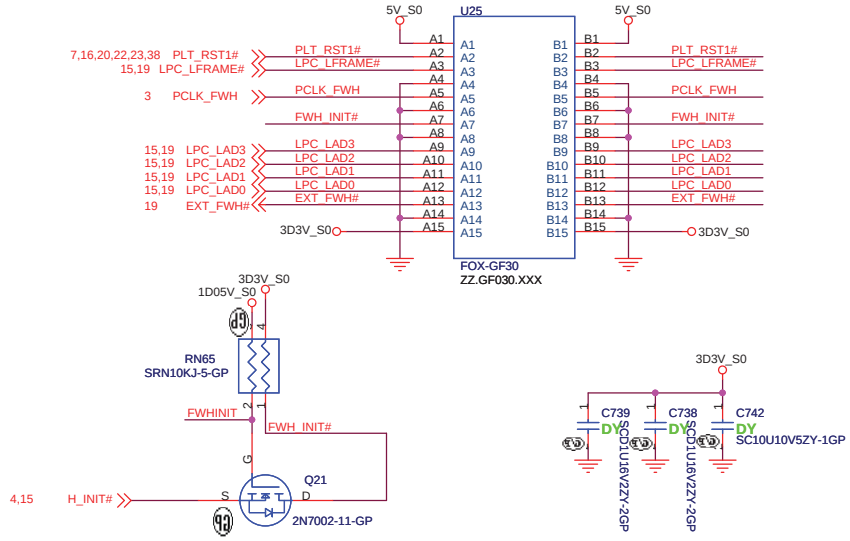
Touch Pad the same as Y40/Y41/Y45/Y46

SB
REVERSE TPAD1 PIN DEFINE

15" TOUCHPAD BUTTON SWITCH



GOLDEN FINGER FOR DEBUG BOARD

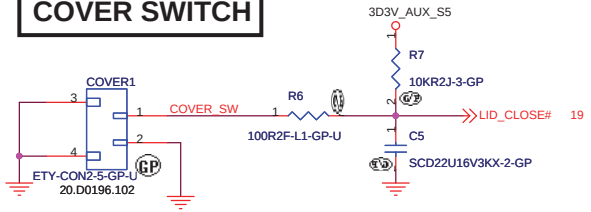


TOP VIEW

A15	(B1)
A14	(B2)
⋮	⋮
A2	(B14)
A1	(B15)

(BOTTOM VIEW)

COVER SWITCH



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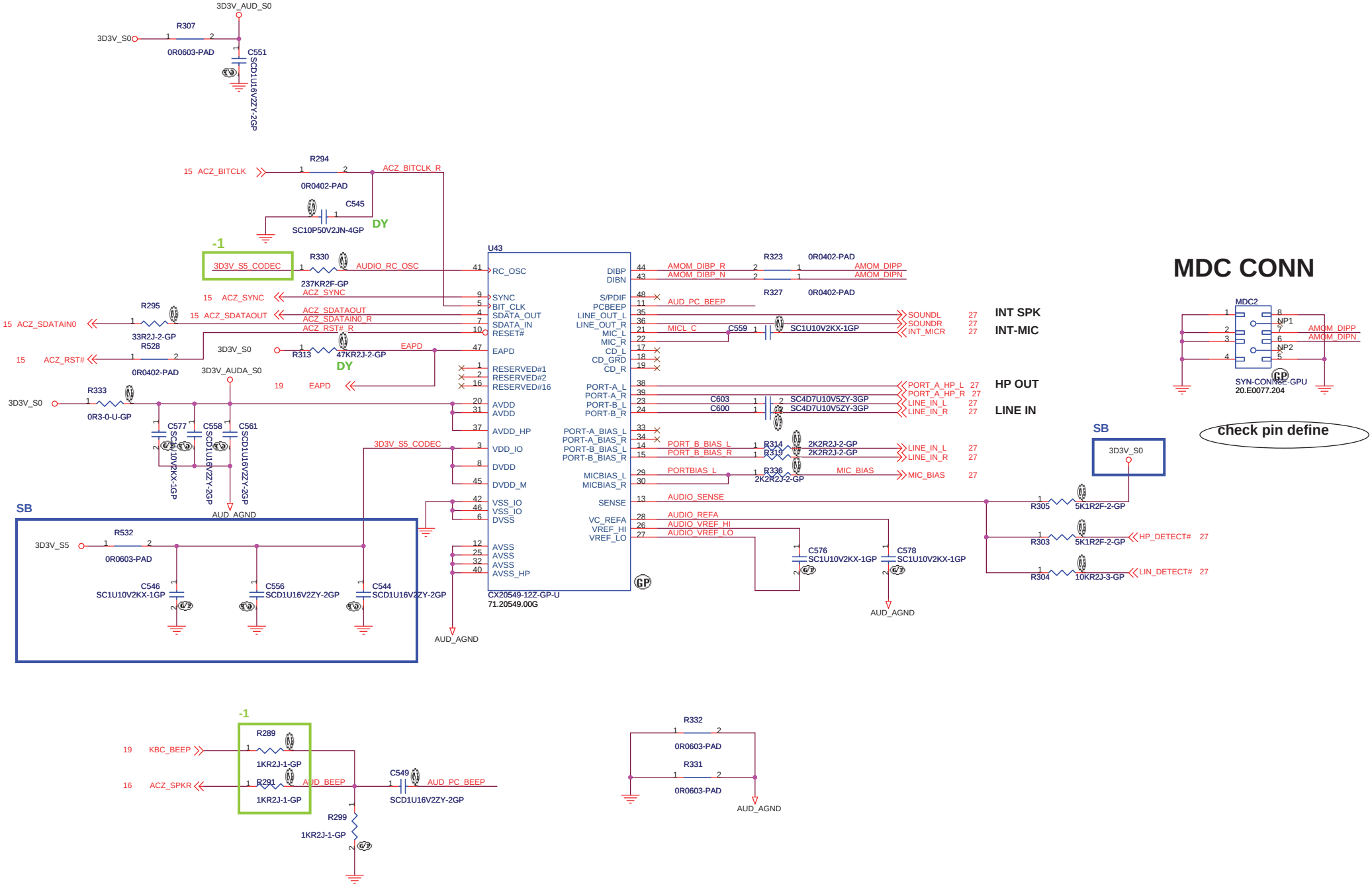
Taipei Hsien 221, Taiwan, R.O.C.

Title: **KeyBoard/TPAD/Debug**

Size: Custom | Document Number: **C45/C46** | Rev: **SA**

Date: Thursday, April 26, 2007 | Sheet 25 of 45



緯創資通 Wistron Corporation
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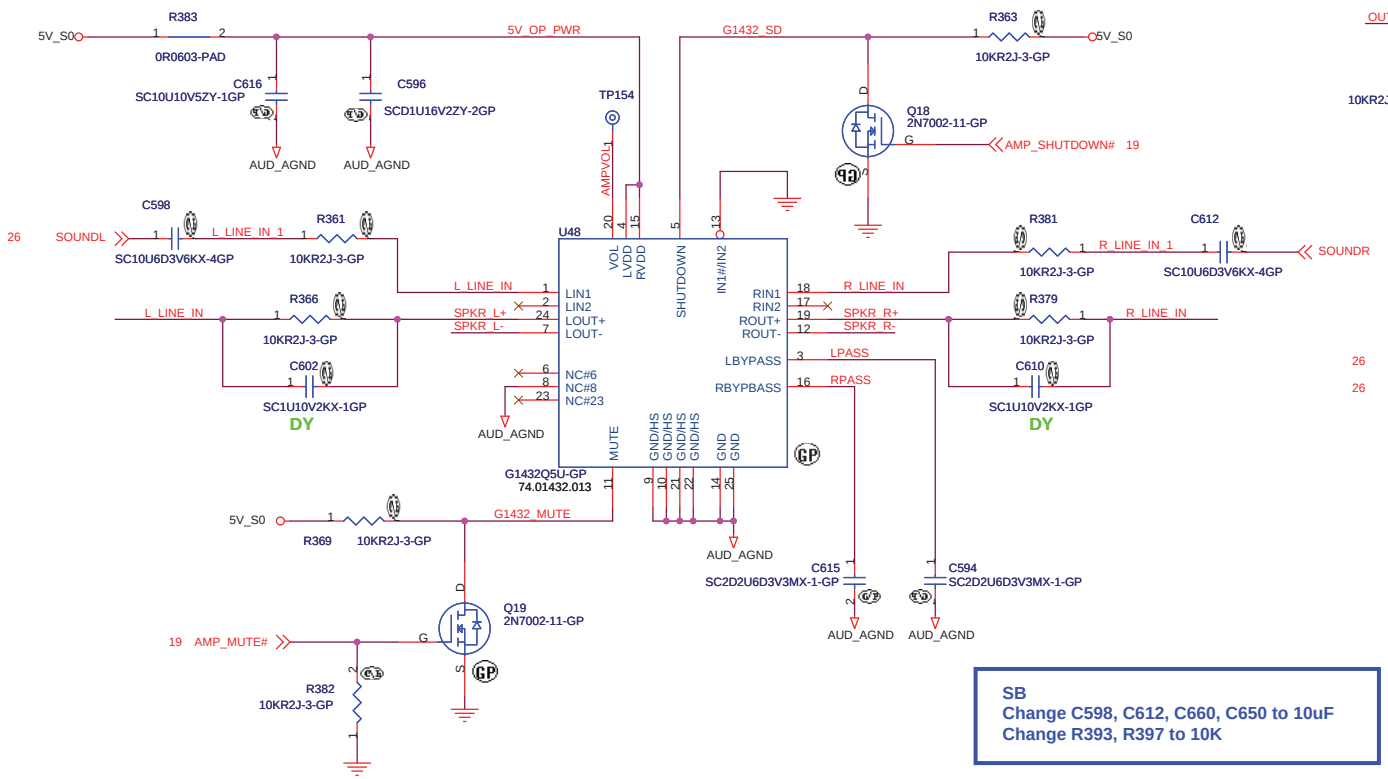
Taipei Hsien 221, Taiwan, R.O.C.

Title: **AUDIO CODEC CX20549-12Z/MDC**

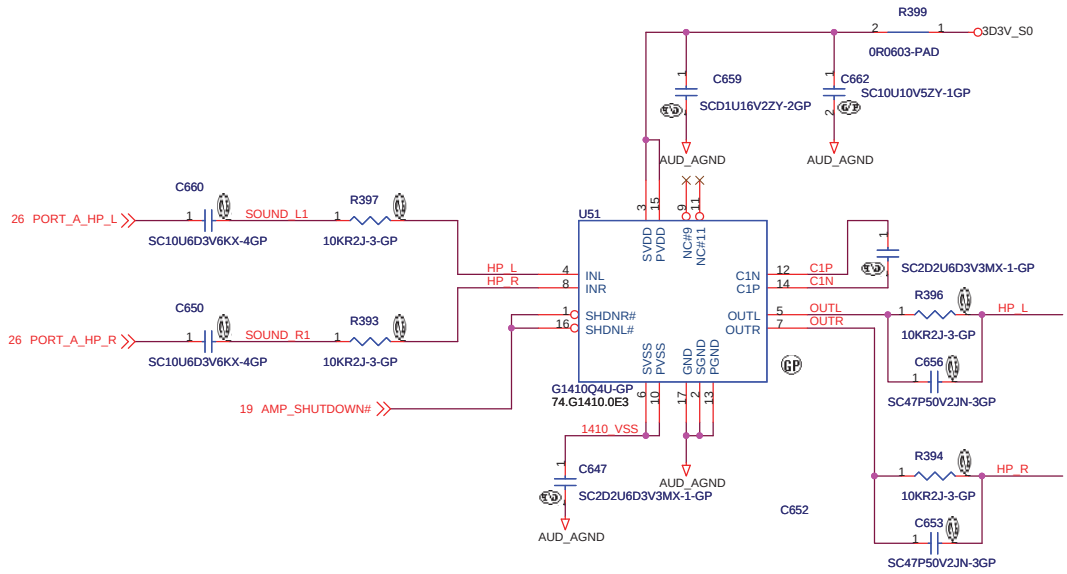
Size	Document Number	Rev
Custom	C45/C46	SA

Date: Thursday, April 26, 2007 Sheet 26 of 45

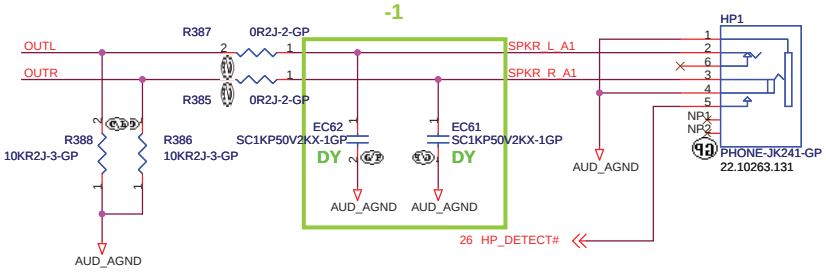
AUDIO AMPLIFIER



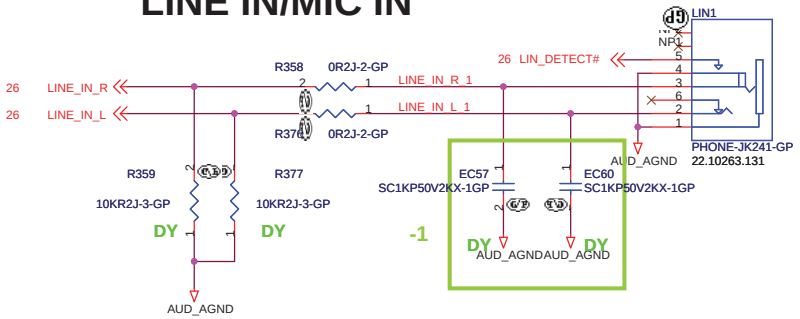
SB
Change C598, C612, C660, C650 to 10uF
Change R393, R397 to 10K



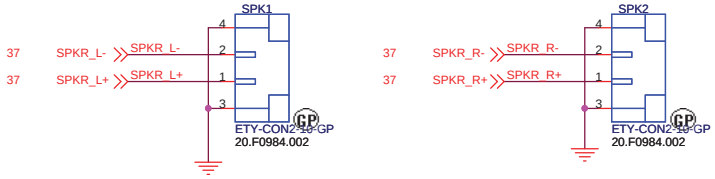
Headphone OUT



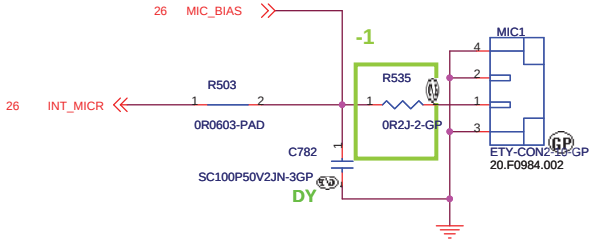
LINE IN/MIC IN



Internal Speaker



Internal MIC



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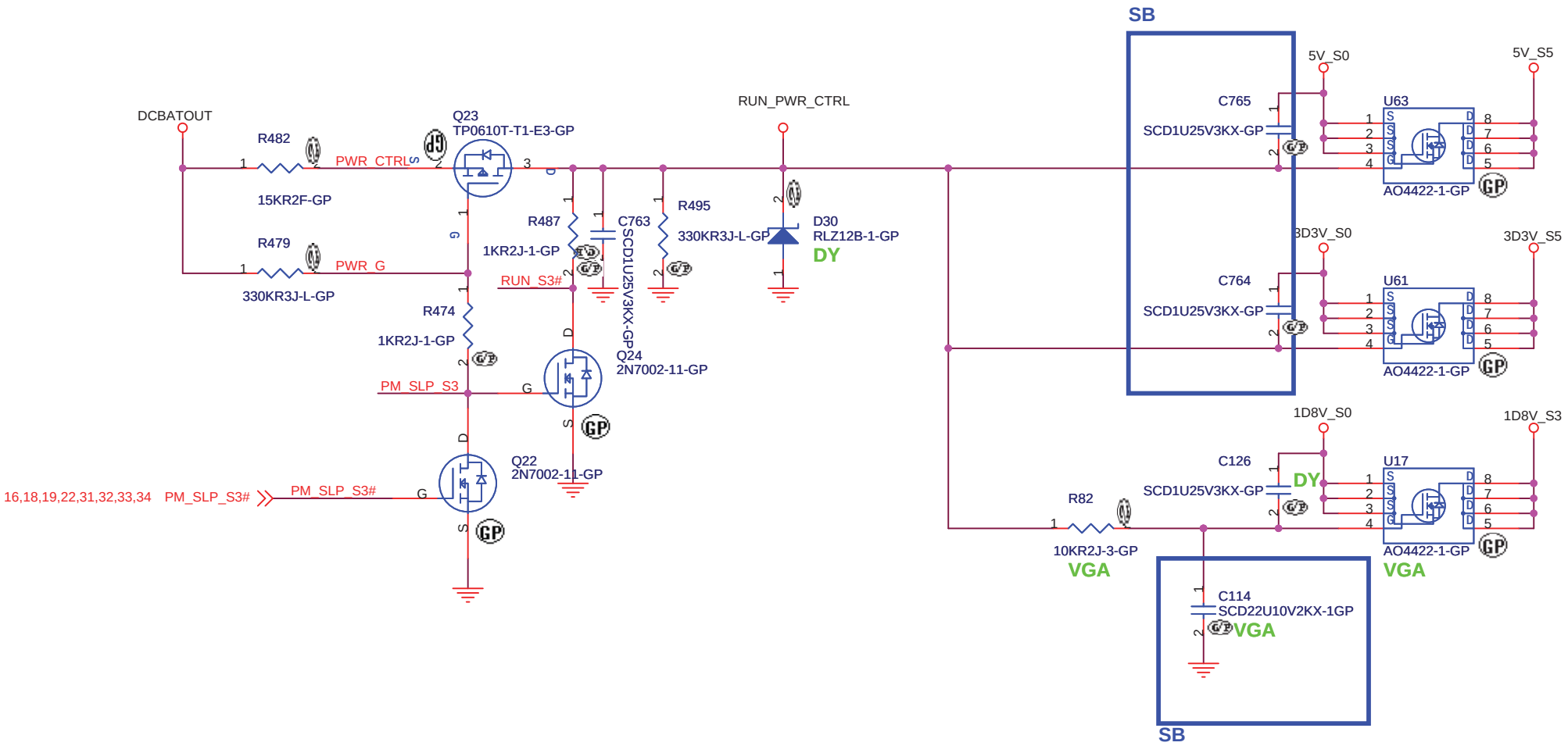
Title: ***Audio_AMP(G1432)& JACK***

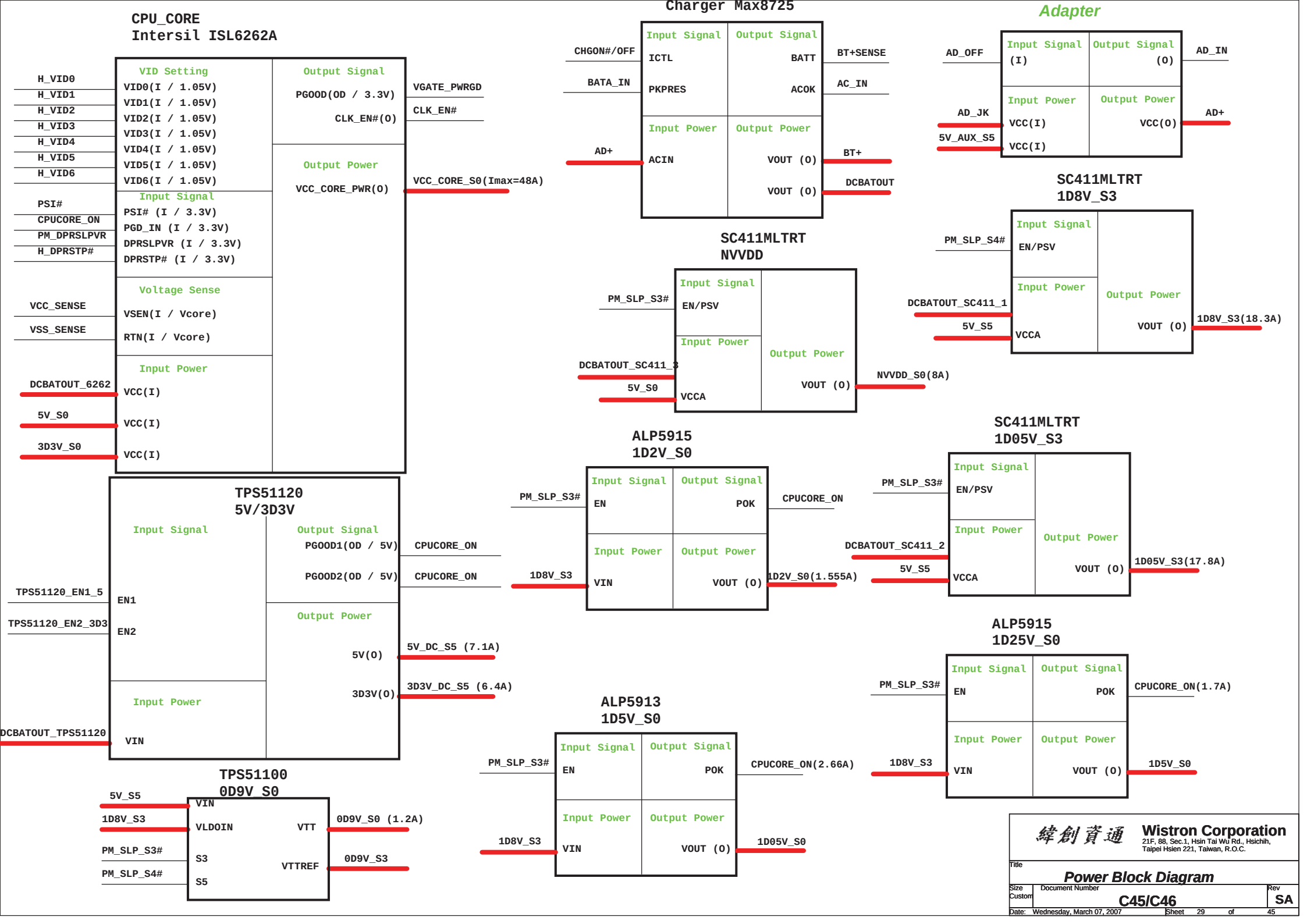
Size	Document Number	Rev
A3	C45/C46	SA

Date: Thursday, April 26, 2007 Sheet 27 of 45

Run Power



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***RUN POWER / CTRL LOGIC***	
Size A4	Document Number C45/C46	Rev **SA**
Date: Wednesday, April 25, 2007	Sheet 28 of 45	


CPU_CORE
Intersil ISL6262A
VID Setting
VID0(I / 1.05V)
VID1(I / 1.05V)
VID2(I / 1.05V)
VID3(I / 1.05V)
VID4(I / 1.05V)
VID5(I / 1.05V)
VID6(I / 1.05V)
H_VID0
H_VID1
H_VID2
H_VID3
H_VID4
H_VID5
H_VID6
Output Signal
PGOOD(OD / 3.3V)
CLK_EN#(O)
VGATE_PWRGD
CLK_EN#
Output Power
VCC_CORE_PWR(O)
VCC_CORE_S0(Imax=48A)
Input Signal
PSI# (I / 3.3V)
PGD_IN (I / 3.3V)
DPRSLPVR (I / 3.3V)
DPRSTP# (I / 3.3V)
PSI#
CPUCORE_ON
PM_DPRSLPVR
H_DPRSTP#
Voltage Sense
VSEN(I / Vcore)
RTN(I / Vcore)
VCC_SENSE
VSS_SENSE
Input Power
VCC(I)
VCC(I)
VCC(I)
DCBATOUT_6262
5V_S0
3D3V_S0
Charger Max8725
Input Signal
ICTL
PKPRES
Output Signal
BATT
ACOK
CHGON#/OFF
BATA_IN
BT+SENSE
AC_IN
Input Power
ACIN
Output Power
VOUT (O)
VOUT (O)
AD+
BT+
DCBATOUT
Adapter
Input Signal
(I)
Output Signal
(O)
AD_OFF
AD_IN
Input Power
VCC(I)
VCC(I)
Output Power
VCC(O)
AD_JK
5V_AUX_S5
AD+
SC411MLTRT
1D8V_S3
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S4#
DCBATOUT_SC411_1
5V_S5
1D8V_S3(18.3A)
SC411MLTRT
NVVDD
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S3#
DCBATOUT_SC411_3
5V_S0
NVVDD_S0(8A)
TPS51120
5V/3D3V
Input Signal
EN1
EN2
Output Signal
PGOOD1(OD / 5V)
PGOOD2(OD / 5V)
CPUCORE_ON
CPUCORE_ON
TPS51120_EN1_5
TPS51120_EN2_3D3
Output Power
5V(O)
3D3V(O)
5V_DC_S5 (7.1A)
3D3V_DC_S5 (6.4A)
Input Power
VIN
DCBATOUT_TPS51120
ALP5915
1D2V_S0
Input Signal
EN
Output Signal
POK
PM_SLP_S3#
CPUCORE_ON
Input Power
VIN
Output Power
VOUT (O)
1D8V_S3
1D2V_S0(1.555A)
SC411MLTRT
1D05V_S3
Input Signal
EN/PSV
Input Power
VCCA
Output Power
VOUT (O)
PM_SLP_S3#
DCBATOUT_SC411_2
5V_S5
1D05V_S3(17.8A)
ALP5915
1D25V_S0
Input Signal
EN
Output Signal
POK
PM_SLP_S3#
CPUCORE_ON(1.7A)
Input Power
VIN
Output Power
VOUT (O)
1D8V_S3
1D5V_S0
ALP5913
1D5V_S0
Input Signal
EN
Output Signal
POK
PM_SLP_S3#
CPUCORE_ON(2.66A)
Input Power
VIN
Output Power
VOUT (O)
1D8V_S3
1D05V_S0
TPS51100
0D9V_S0
VIN
VLDOIN
S3
S5
VTT
VTTREF
5V_S5
1D8V_S3
PM_SLP_S3#
PM_SLP_S4#
0D9V_S0 (1.2A)
0D9V_S3
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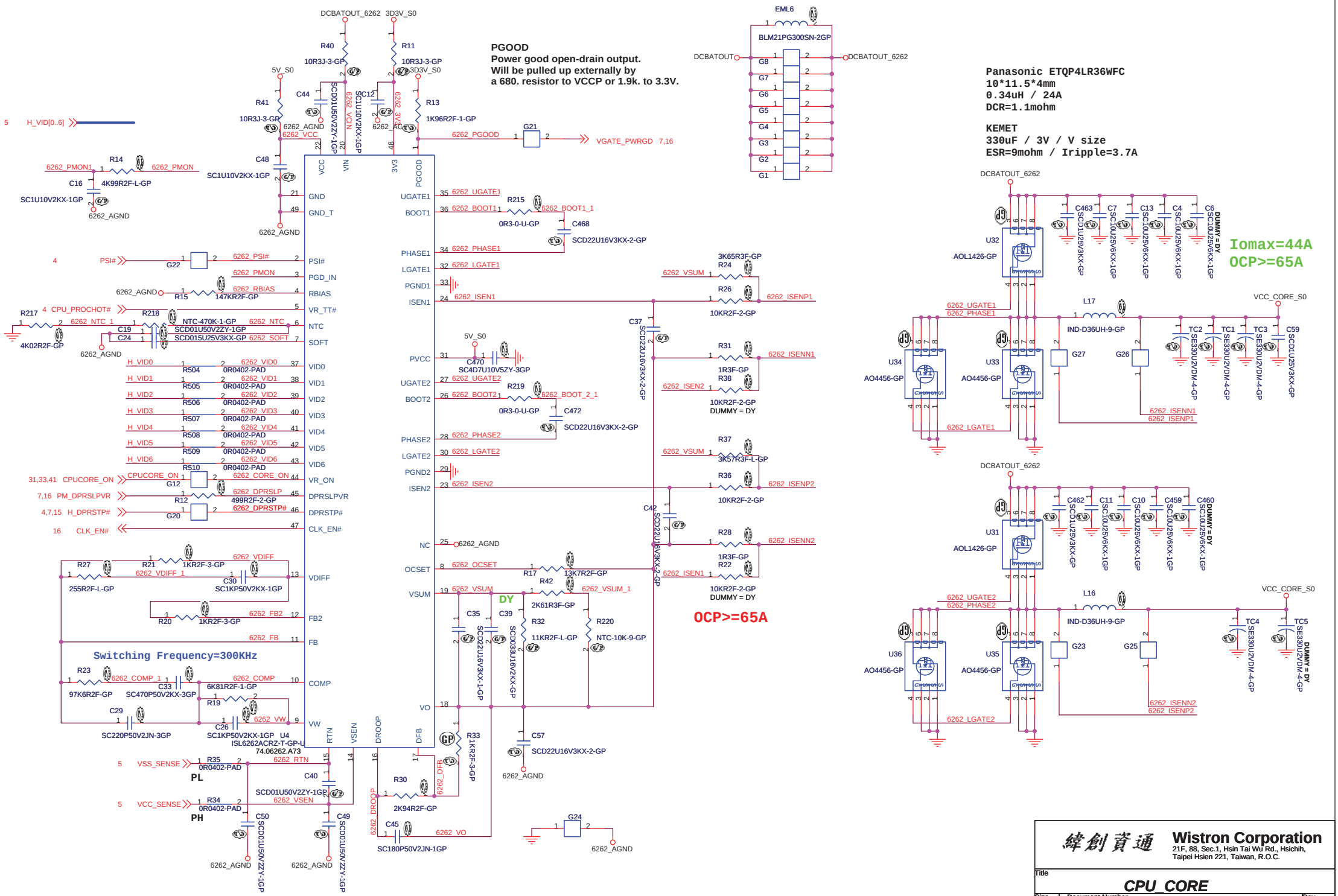
Title
Power Block Diagram
Size
Custom
Document Number
C45/C46
Rev
SA
Date: Wednesday, March 07, 2007
Sheet 29 of 45



Wistron Corporation			
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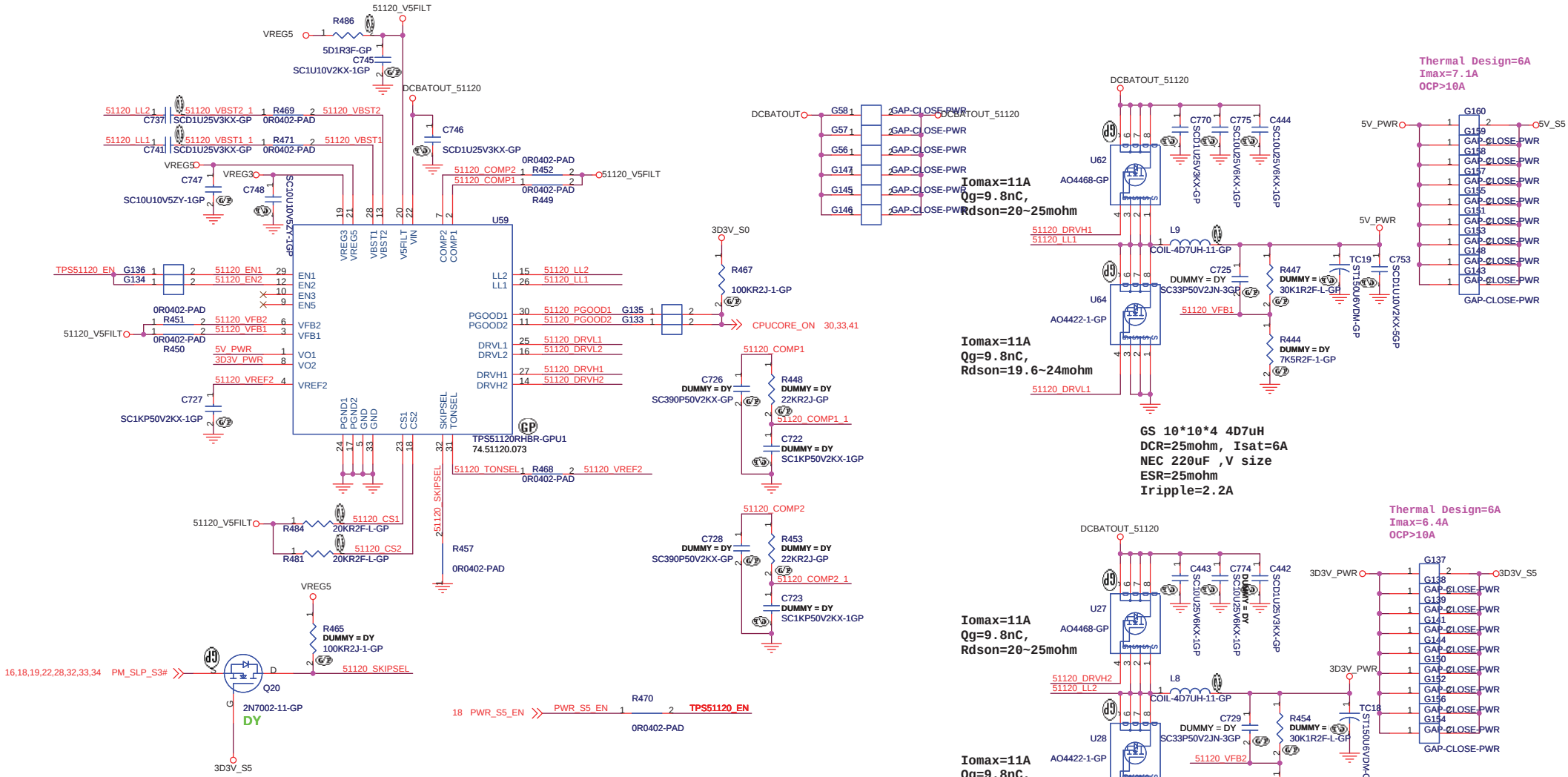
Title: CPU_CORE			
Size: Custom	Document Number: C45/C46	Rev: SA	
Date: Wednesday, April 25, 2007	Sheet 30 of 45		



	GND	VREF2	FLOAT	V5FILT
SKIPSEL	**AUTOSKIP**	AUTOSKIP /FAULTS OFF	PWM	PWM
COMP	N/A	N/A	CURRENT MODE	**D-Cap MODE**
TONSEL	380k/CH1 590k/CH2	290k/CH1 440k/CH2	**220k/CH1 330k/CH2**	180k/CH1 280k/CH2
VFB1	N/A	not use	ADJ.	**5V Fixed Output**
VFB2	N/A	not use	ADJ.	**3.3V Fixed Output**
EN1,EN2	Switcher OFF	not use	**Swithchr ON**	**Switcher ON**
EN3,EN5	LDO OFF	not use	**LDO ON**	VREG3 on

Vout=1V*(R1+R2)/R2

For TPS51120,
Vout=5V
1. If you use a 6.8uH inductor, the minimum ESR is 70m ohm.
2. If you use a 4.7uH inductor, the minimum ESR is 48m ohm.
3. If you use a 3.3uH inductor, the minimum ESR is 34m ohm.

Vout=3.3V
1. If you use a 4.7uH inductor, the minimum ESR is 51m ohm.
2. If you use a 3.3uH inductor, the minimum ESR is 36m ohm.
3. If you use a 2.5uH inductor, the minimum ESR is 27m ohm.

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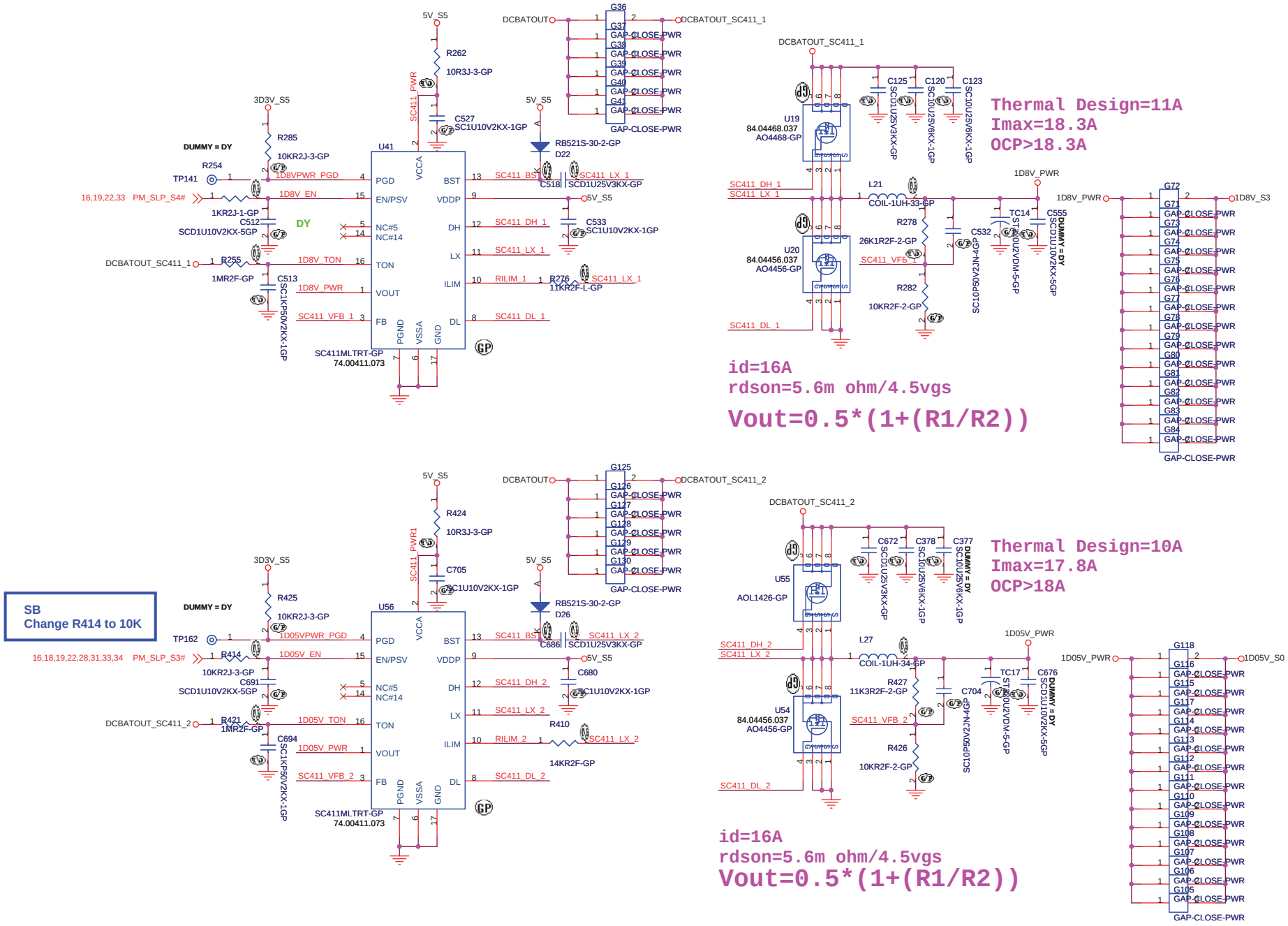
Title: ***TPS51120_3D3V_5V***

Size: Custom | Document Number: **C45/C46** | Rev: **SA**

Date: Wednesday, April 25, 2007 | Sheet 31 of 45



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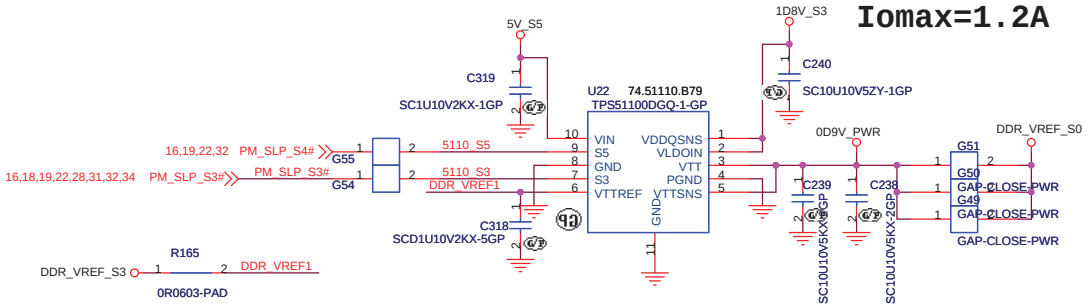
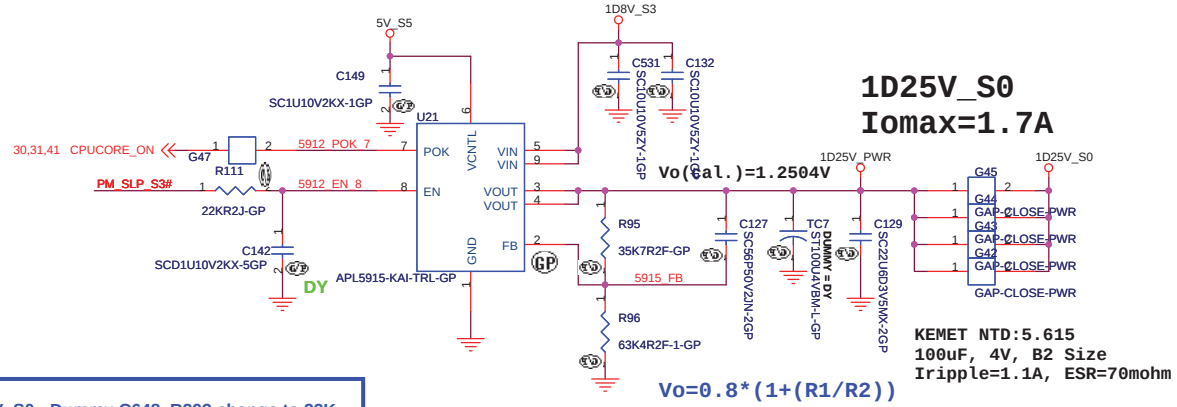
Title: SC411_1D05V/1D8V			
Size: Custom	Document Number: C45/C46		Rev: SA
Date: Wednesday, April 25, 2007		Sheet 32 of 45	

0D9V
Iomax=1.2A



Place near the Test point DDRVREF

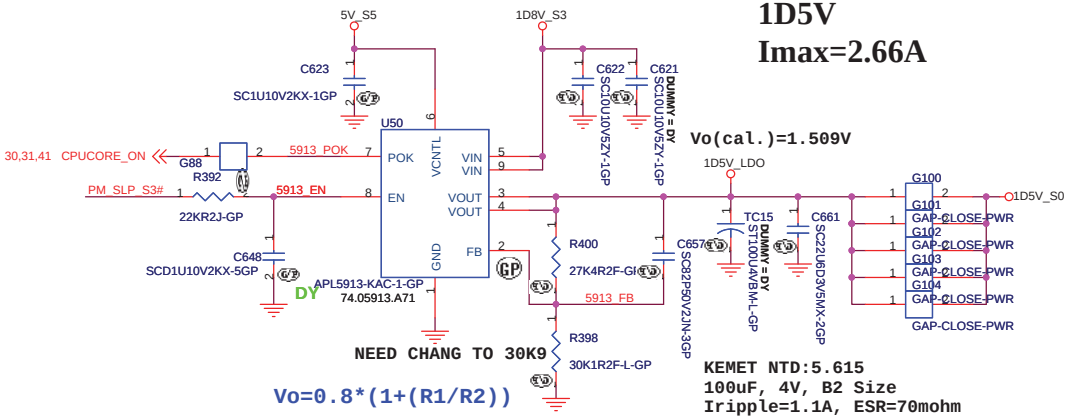
1D25V_S0
Iomax=1.7A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

SB
1D5V_S0 : Dummy C648, R392 change to 22K
1D25V_S0 : Dummy C142, R111 change to 22K

1D5V
Imax=2.66A



KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A, ESR=70mohm

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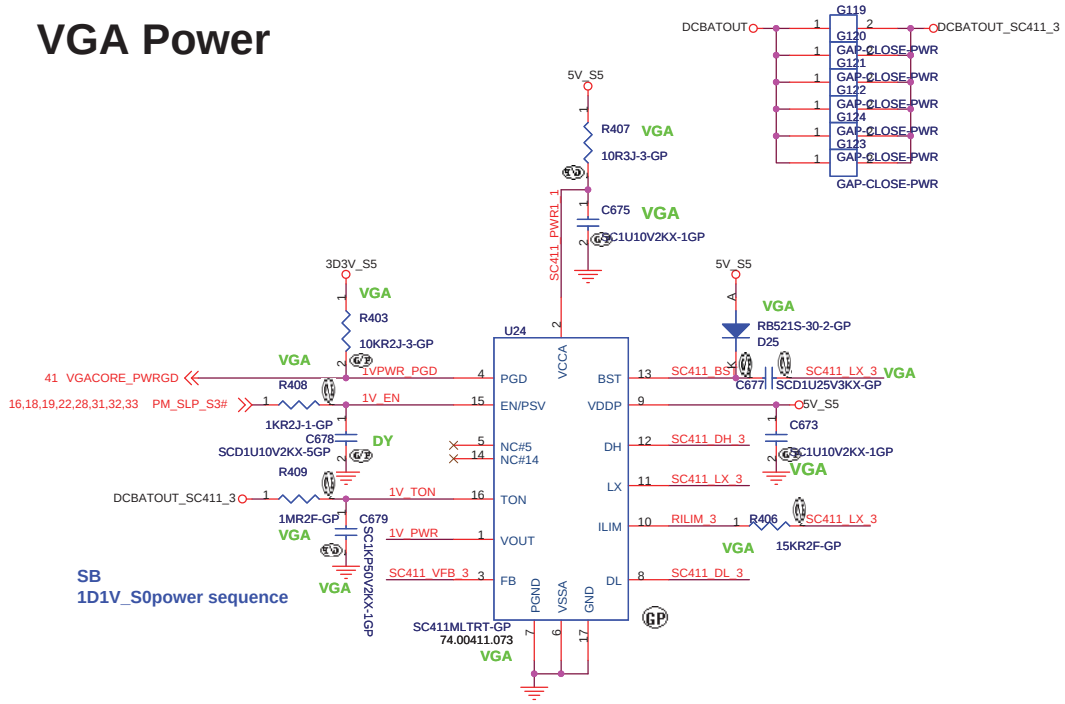
Title: 1D5V/0D9V/1D05V

Size: A3 | Document Number: C45/C46 | Rev: SA

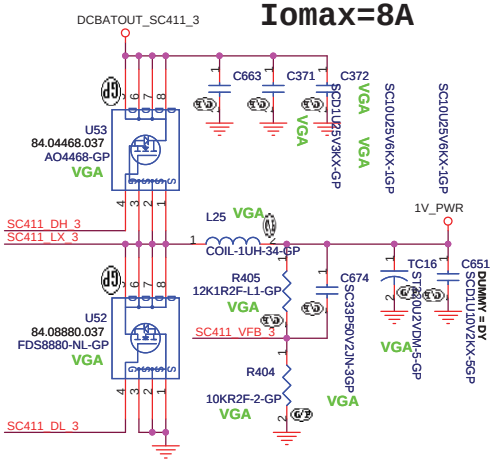
Date: Wednesday, April 25, 2007 | Sheet 33 of 45

VGA Power



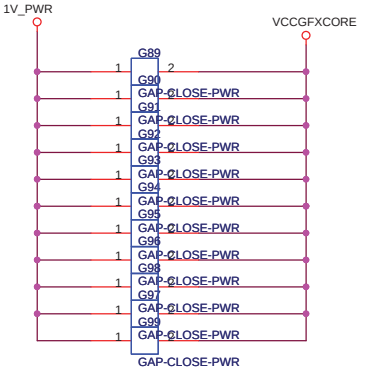
Thermal Design=8A
Imax=8A
OCP>14A

1V_S0
Iomax=8A



id=11.6A
rdson=12m ohm/4.5vgs

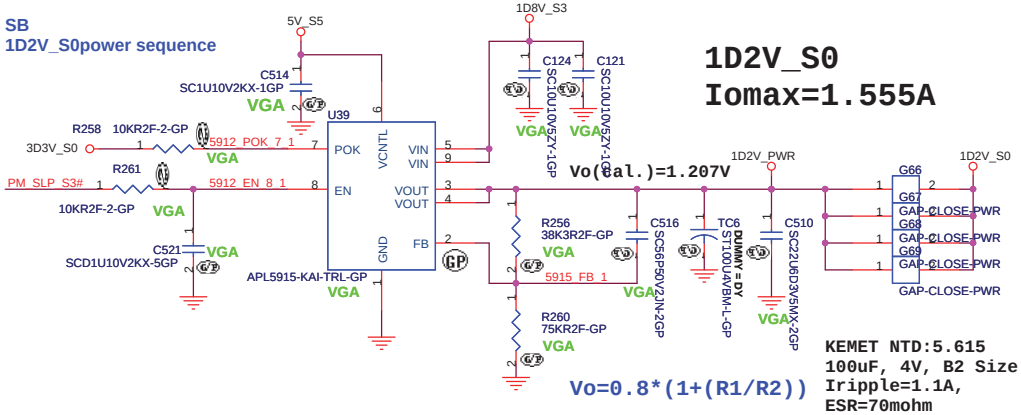
Vout=0.5*(1+(R1/R2))



R405
FOR M71 ---> 1.2V 14K (64.14025.6DL)
FOR M72 ---> 1.1V 12.1K (64.12125.6DL)

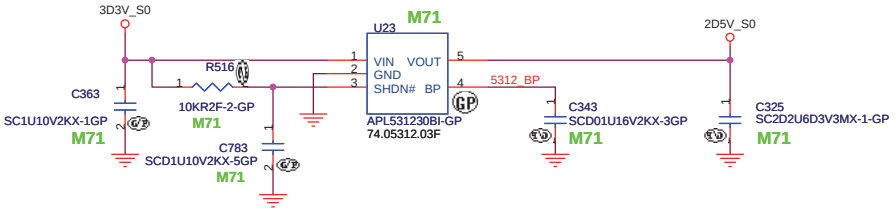
SB
1D2V_S0power sequence

1D2V_S0
Iomax=1.555A

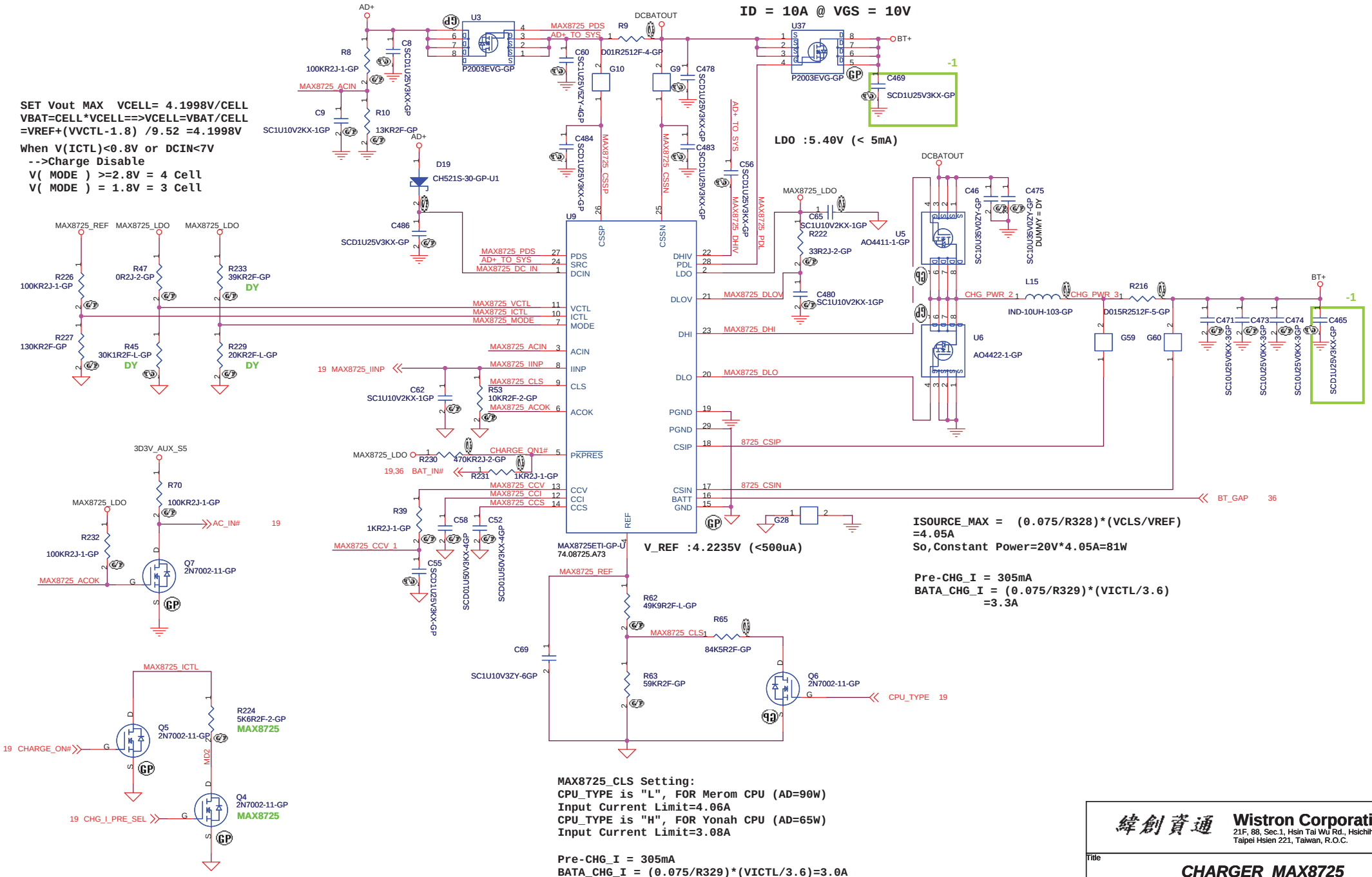


KEMET NTD:5.615
100uF, 4V, B2 Size
Iripple=1.1A,
ESR=70mohm

2D5V
Iomax=300mA

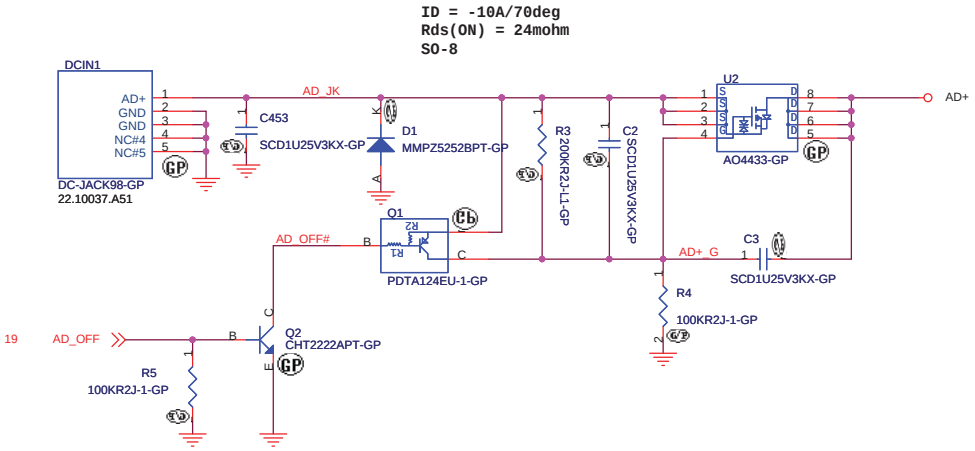


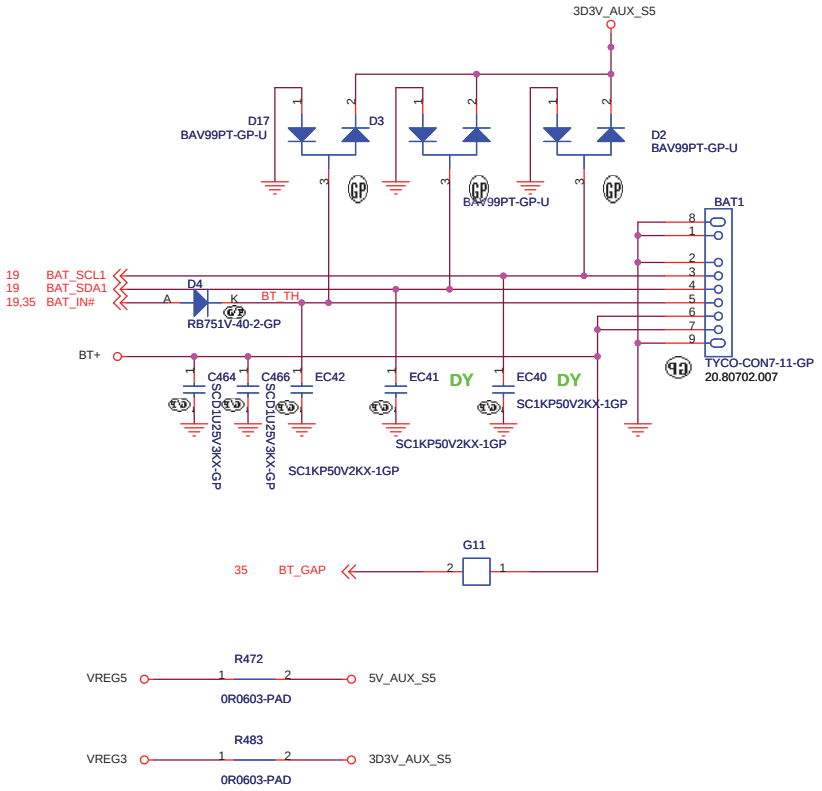
緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	**VGA POWER**	
Size A3	Document Number **C45/C46**	Rev **SA**
Date: Wednesday, April 25, 2007	Sheet 34 of 45	


ID = 10A @ VGS = 10V
SET Vout MAX VCELL= 4.1998V/CELL
VBAT=CELL*VCELL==>VCELL=VBAT/CELL
=VREF+(VVCTL-1.8) /9.52 =4.1998V
When V(ICTL)<0.8V or DCIN<7V
-->Charge Disable
V(MODE) >=2.8V = 4 Cell
V(MODE) = 1.8V = 3 Cell
LDO :5.40V (< 5mA)
V_REF :4.2235V (<500uA)
ISOURCE_MAX = (0.075/R328)*(VCLS/VREF)
=4.05A
So,Constant Power=20V*4.05A=81W
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R329)*(VICTL/3.6)
=3.3A
MAX8725_CLS Setting:
CPU_TYPE is "L", FOR Merom CPU (AD=90W)
Input Current Limit=4.06A
CPU_TYPE is "H", FOR Yonah CPU (AD=65W)
Input Current Limit=3.08A
Pre-CHG_I = 305mA
BATA_CHG_I = (0.075/R329)*(VICTL/3.6)=3.0A
U9
MAX8725ETI-GP-U
74.08725.A73
U3
P2003EVG-GP
U37
P2003EVG-GP
U5
AO4411-1-GP
U6
AO4422-1-GP
Q5 2N7002-11-GP
Q6 2N7002-11-GP
Q7 2N7002-11-GP
Q4 2N7002-11-GP
MAX8725
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
CHARGER_MAX8725
Size Custom
Document Number
C45/C46
Rev
SA
Date: Friday, April 27, 2007
Sheet 35 of 45

BATTERY CONNECTOR

Adaptor in to generate DCBATOUT





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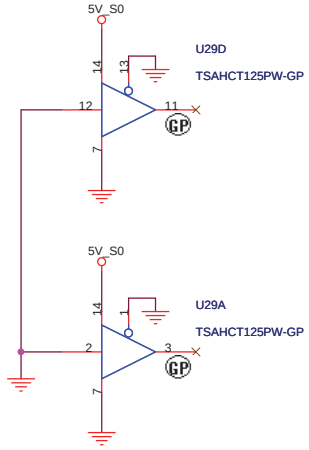
Title: **AD_IN/BAT Conn**

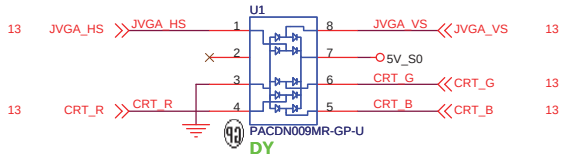
Size	Document Number	Rev
Custom	C45/C46	SA

Date: Friday, April 27, 2007 Sheet 36 of 45

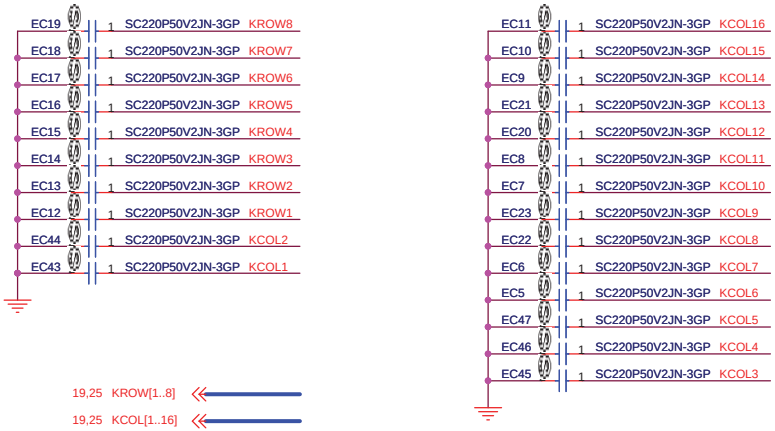
UNUSE Parts



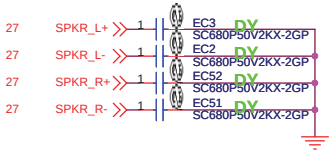
ESD Parts

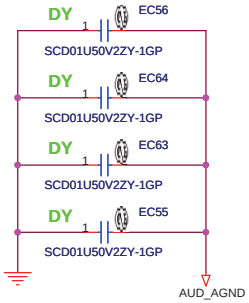


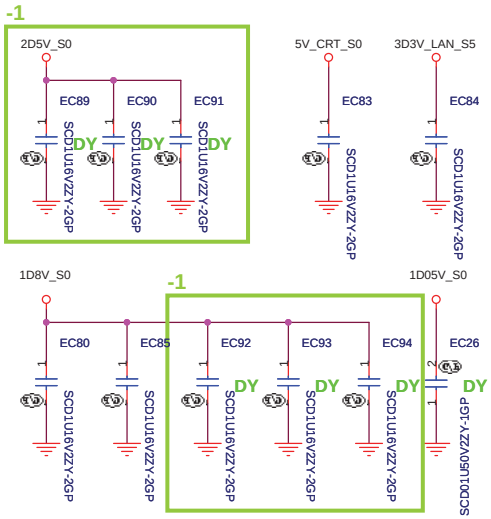
Keyboard EMI Caps

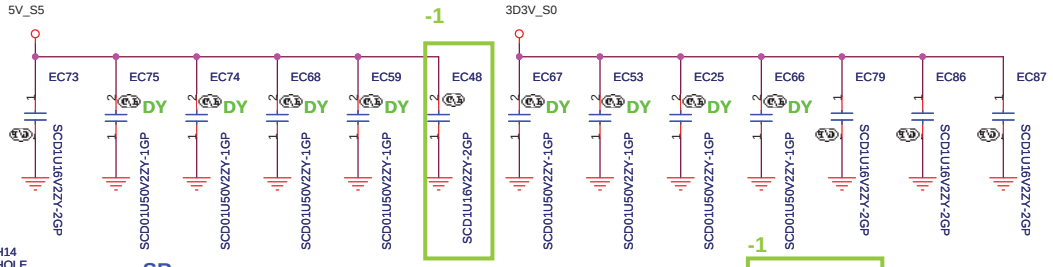


EMI Caps

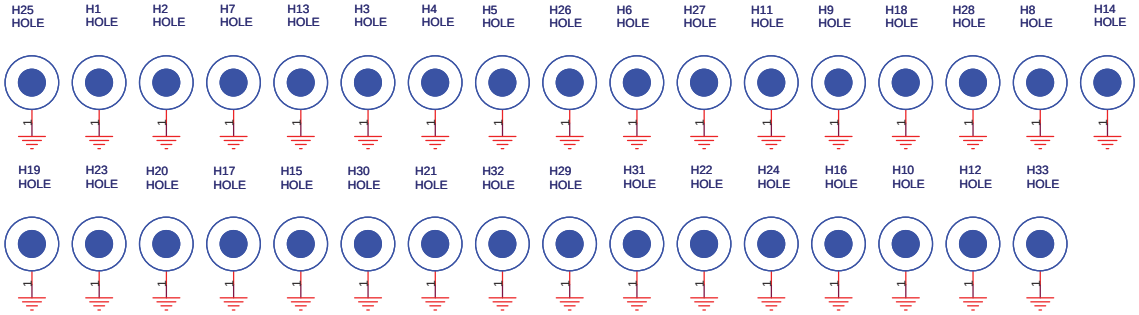








Holes

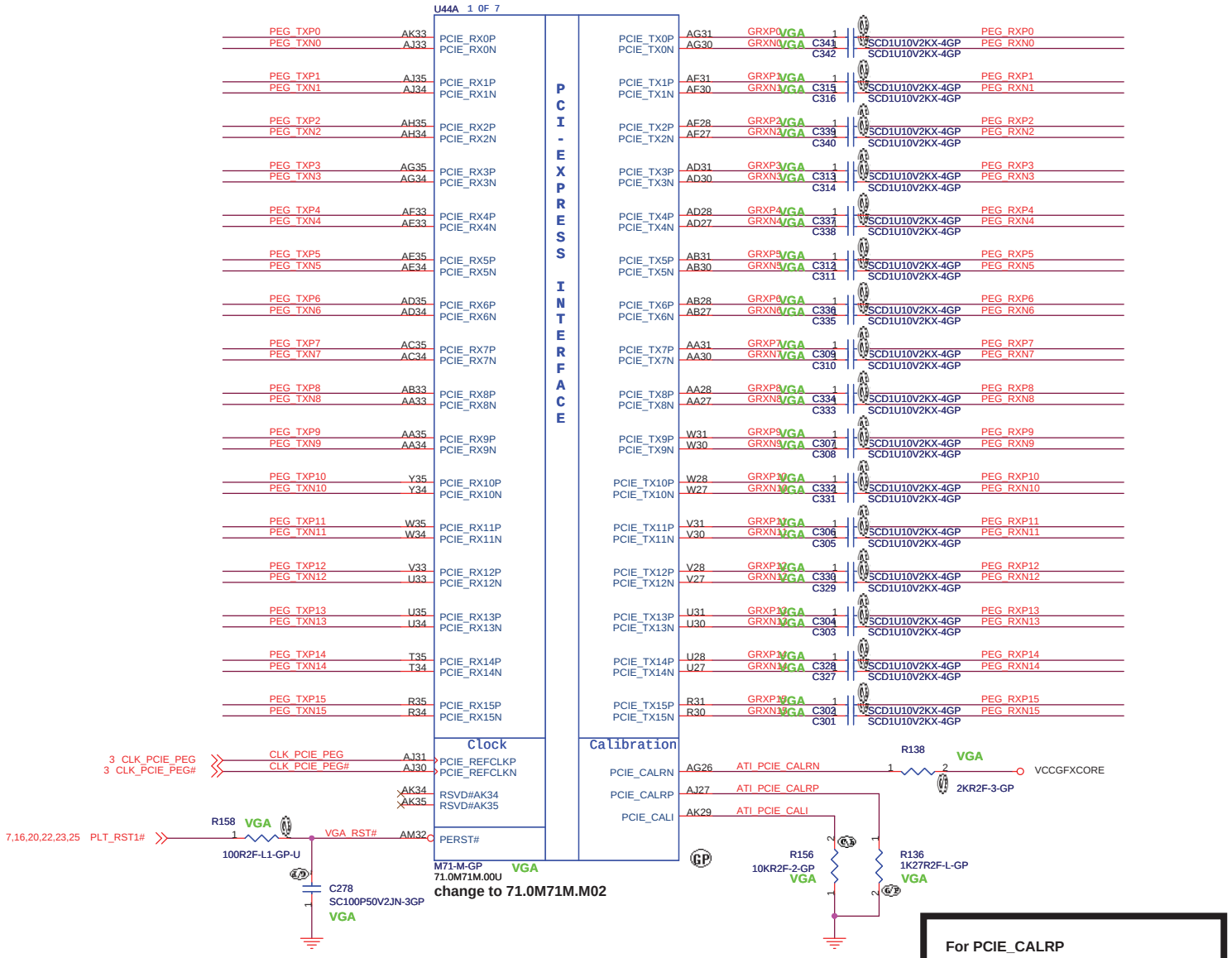


緯創資通 **Wistron Corporation**
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
Custom	C45/C46	SA

Date: Friday, April 27, 2007 Sheet 37 of 45



For PCIE_CALRP
1.27K to PCIE_VSS for M72M,M76M
562R to PCIE_VSS for M66M,M71M

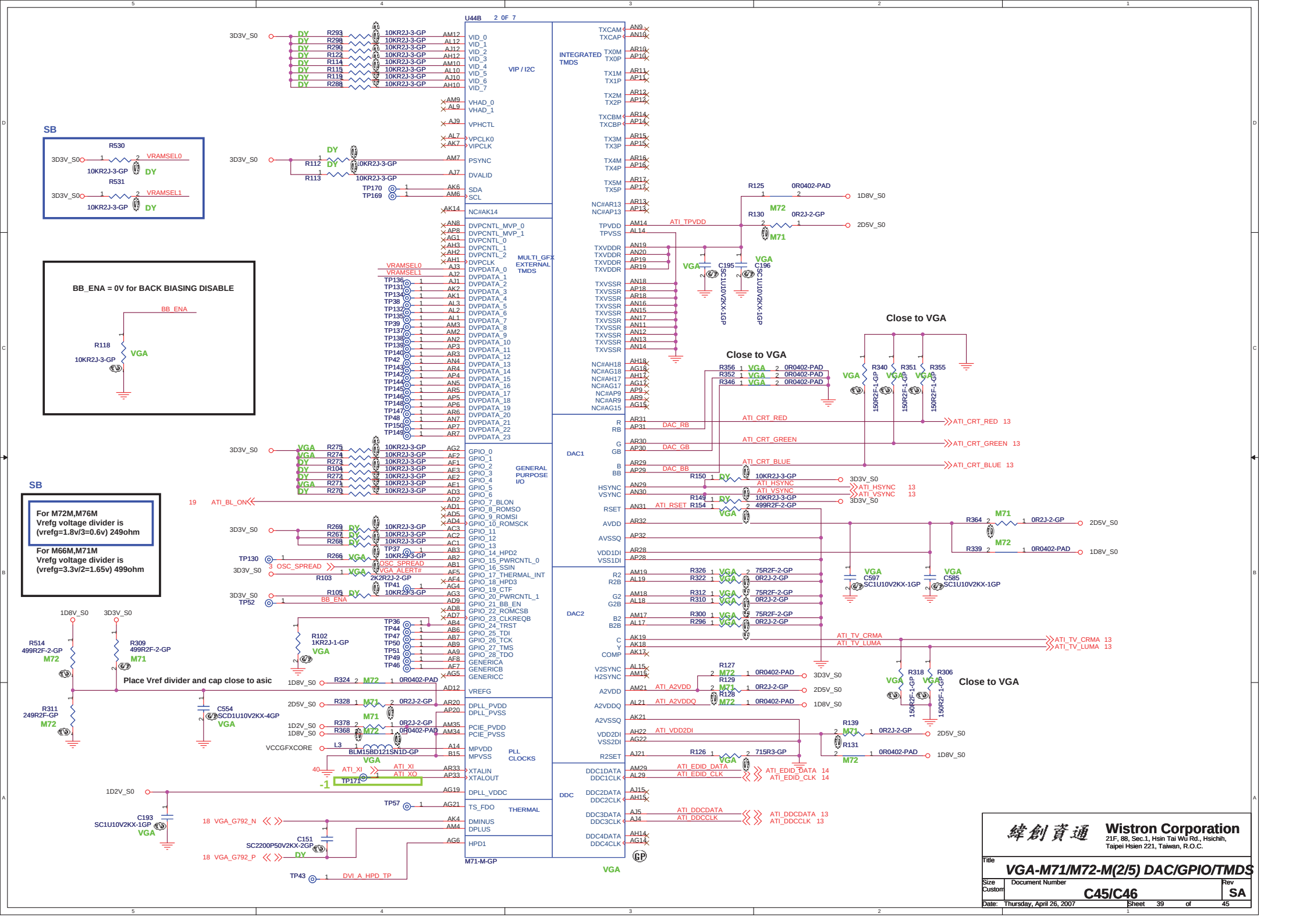
For PCIE_CALI
10K to PCIE_VSS for M72M,M76M
1.47K to PCIE_VSS for M66M,M71M

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-M71/M72-M(1/5) PCIE

Size: A3 | Document Number: C45/C46 | Rev: SA

Date: Wednesday, April 25, 2007 | Sheet 38 of 45


U44B 2 OF 7
VIP / I2C
INTEGRATED TMDS
MULTI_GFX EXTERNAL TMDS
GENERAL PURPOSE I/O
DAC1
DAC2
DDC
PLL CLOCKS
THERMAL
M71-M-GP
VGA
SB
R530
VRAMSEL0
R531
VRAMSEL1
10KR2J-3-GP
DY
BB_ENA = 0V for BACK BIASING DISABLE
BB_ENA
R118
VGA
SB
For M72M,M76M
Vrefg voltage divider is
(vrefg=1.8v/3=0.6v) 249ohm
For M66M,M71M
Vrefg voltage divider is
(vrefg=3.3v/2=1.65v) 499ohm
Place Vref divider and cap close to asic
Close to VGA
Close to VGA
Close to VGA
ATI_CRT_RED
ATI_CRT_GREEN
ATI_CRT_BLUE
ATI_HSYNC
ATI_VSYNC
ATI_TV_CRMA
ATI_TV_LUMA
ATI_EDID_DATA
ATI_EDID_CLK
ATI_DDCDATA
ATI_DDCCLK
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-M71/M72-M(2/5) DAC/GPIO/TMDS
Size Custom
Document Number
C45/C46
Rev
SA
Date: Thursday, April 26, 2007
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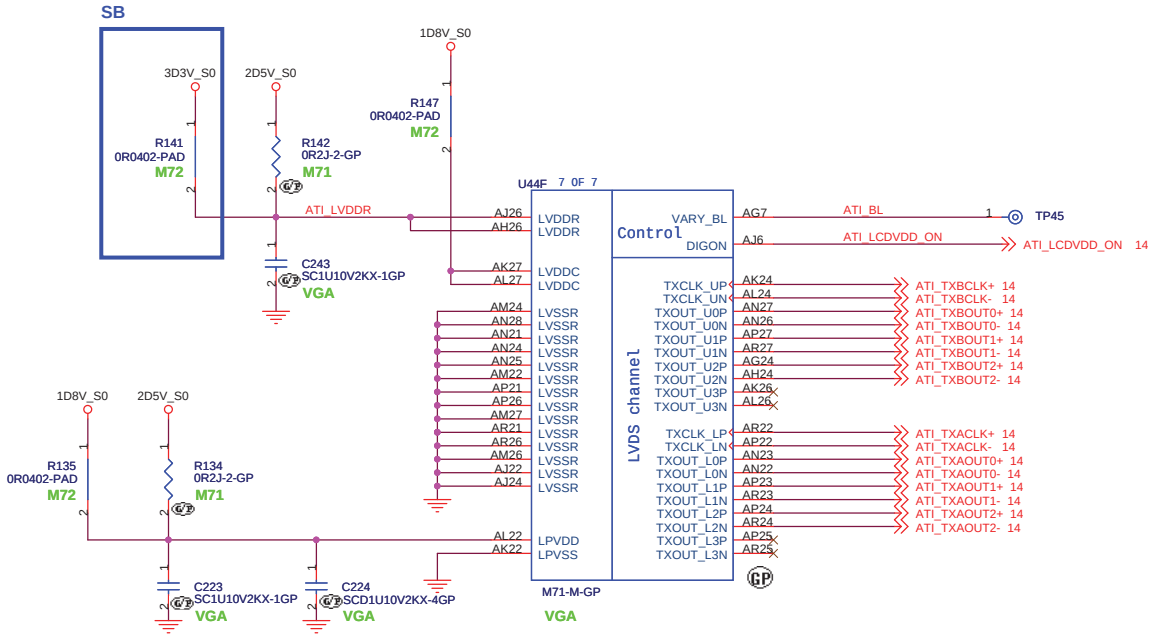

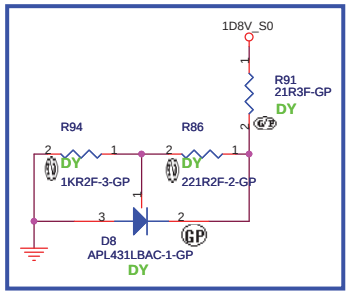

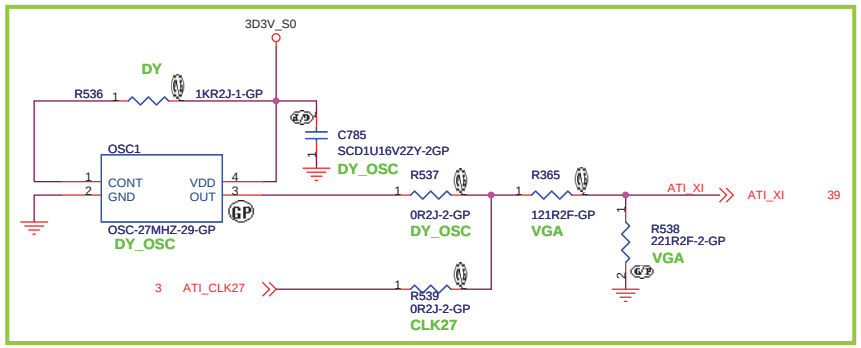

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Taipei Hsien 221, Taiwan, R.O.C.

Title: VGA-M71/M72-M(3/5)LVDS

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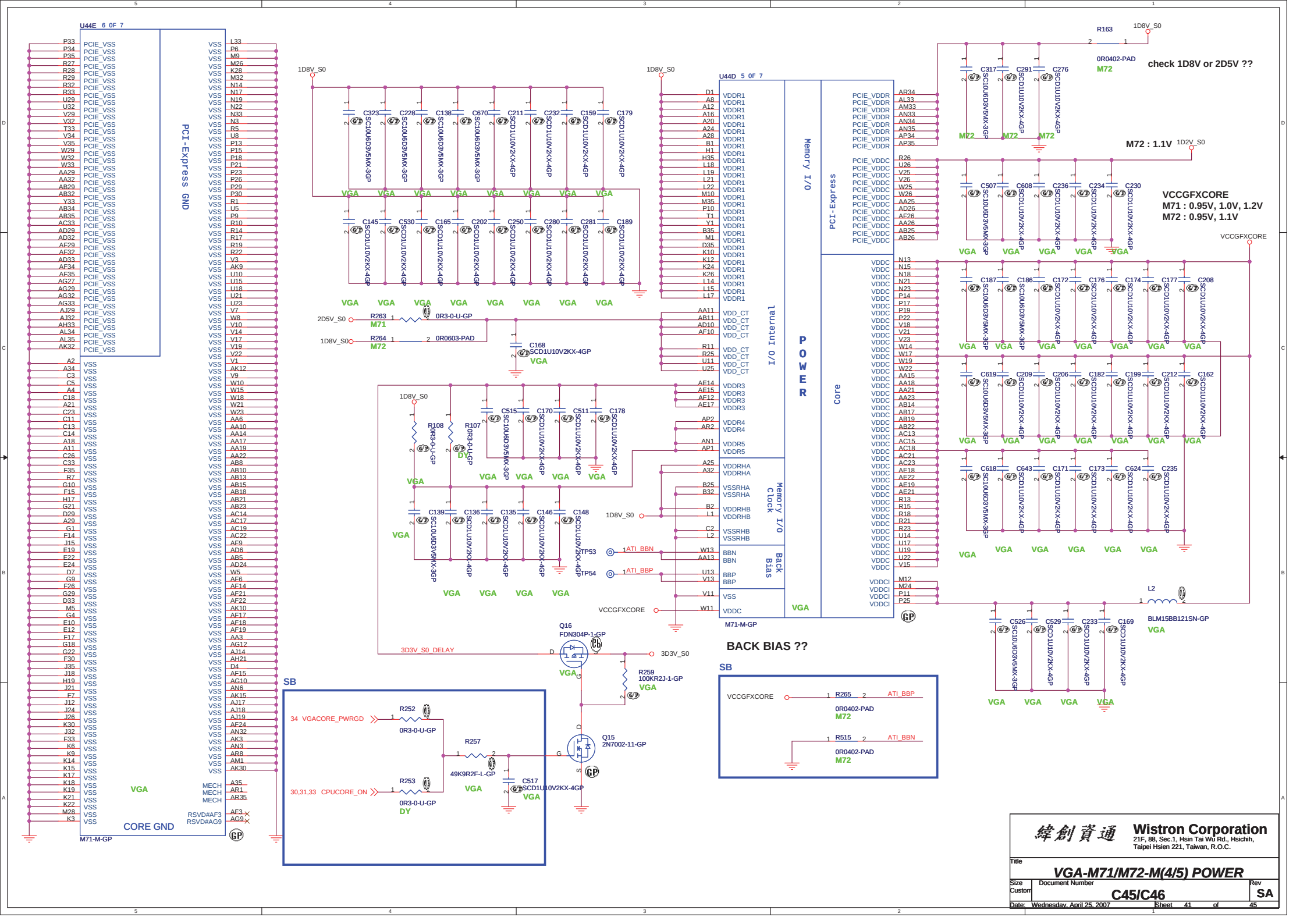
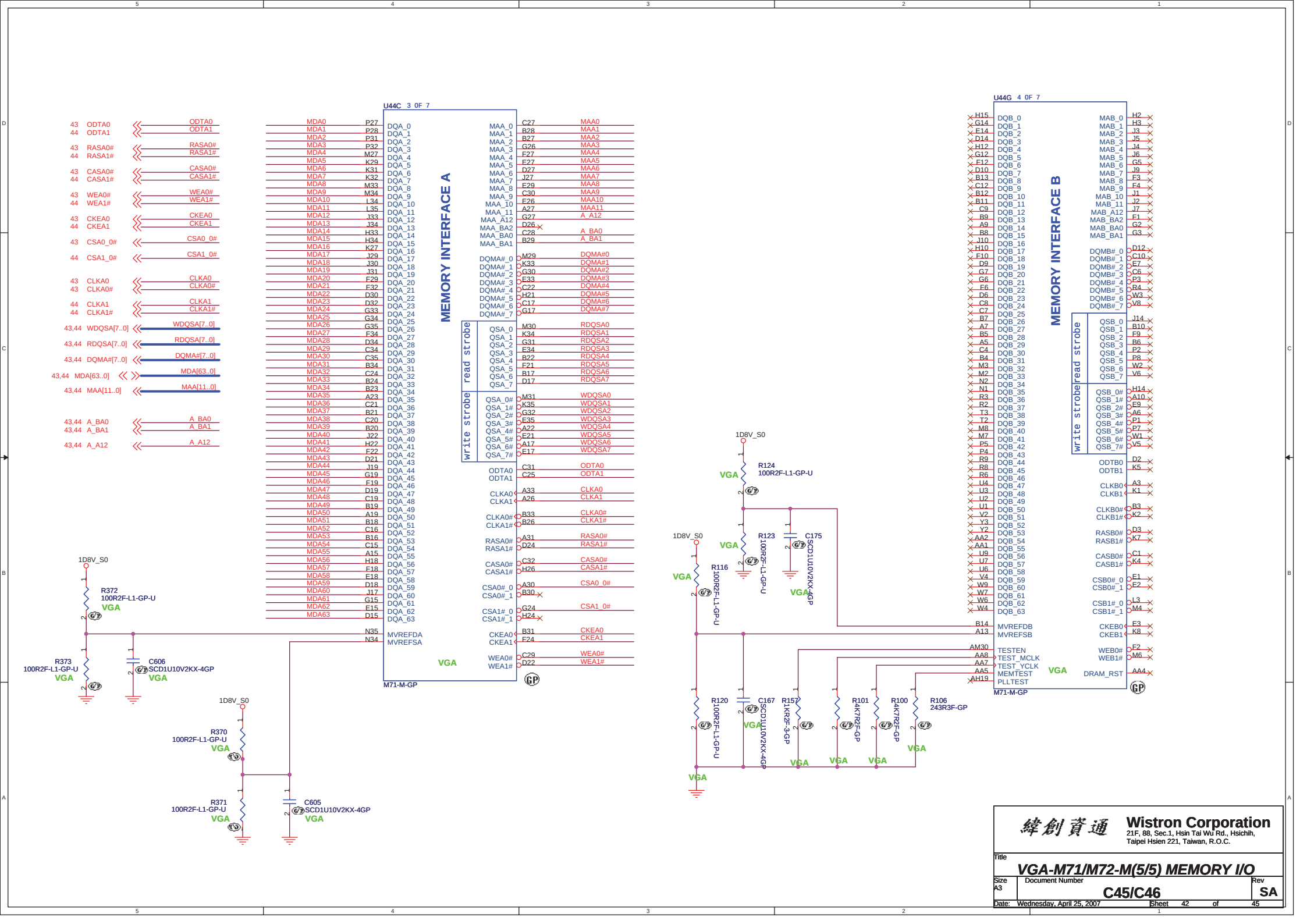

U44E 6 OF 7
PCI-Express GND
CORE GND
M71-M-GP
U44D 5 OF 7
Memory I/O
Internal I/O
POWER
PCI-Express
Core
Memory I/O Clock
Back Bias
M71-M-GP
BACK BIAS ??
SB
SB
check 1D8V or 2D5V ??
M72 : 1.1V
VCCGFXCORE
M71 : 0.95V, 1.0V, 1.2V
M72 : 0.95V, 1.1V
Q16
FDN304P-1-GP
Q15
2N7002-11-GP
L2
BLM15BB121SN-GP
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
VGA-M71/M72-M(4/5) POWER
C45/C46
SA
Wednesday, April 25, 2007
41
45


U44C 3 0F 7
MEMORY INTERFACE A
read strobe
write strobe
M71-M-GP
U44G 4 0F 7
MEMORY INTERFACE B
read strobe
write strobe
M71-M-GP
1D8V_S0
R372 100R2F-L1-GP-U
R373 100R2F-L1-GP-U
C606 SCD1U10V2KX-4GP
R370 100R2F-L1-GP-U
R371 100R2F-L1-GP-U
C605 SCD1U10V2KX-4GP
R124 100R2F-L1-GP-U
R123 100R2F-L1-GP-U
C175 SCD1U10V2KX-4GP
R116 100R2F-L1-GP-U
R120 100R2F-L1-GP-U
C167 SCD1U10V2KX-4GP
R157 1KR2F-3-GP
R101 4K7R2F-GP
R100 4K7R2F-GP
R106 243R3F-GP
VGA
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Title
VGA-M71/M72-M(5/5) MEMORY I/O
Size A3
Document Number C45/C46
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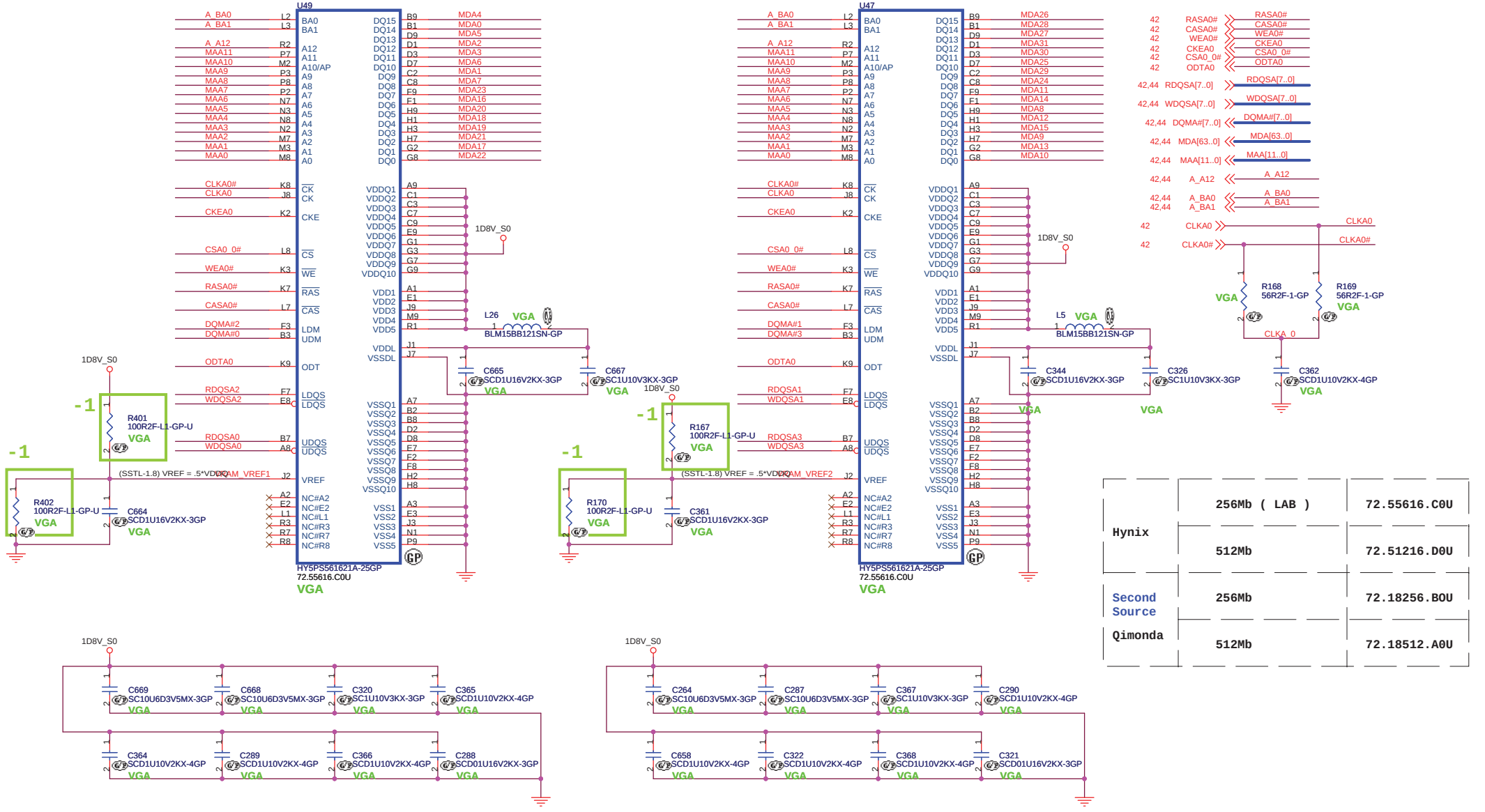
DDR2 BGA MEMORY (16M x 16)



Hynix	256Mb (LAB)	72.55616.C0U
	512Mb	72.51216.D0U
Second Source Qimonda	256Mb	72.18256.B0U
	512Mb	72.18512.A0U

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Title: VGA-VRAM(1/2)

Size: A3 | Document Number: C45/C46 | Rev: SA

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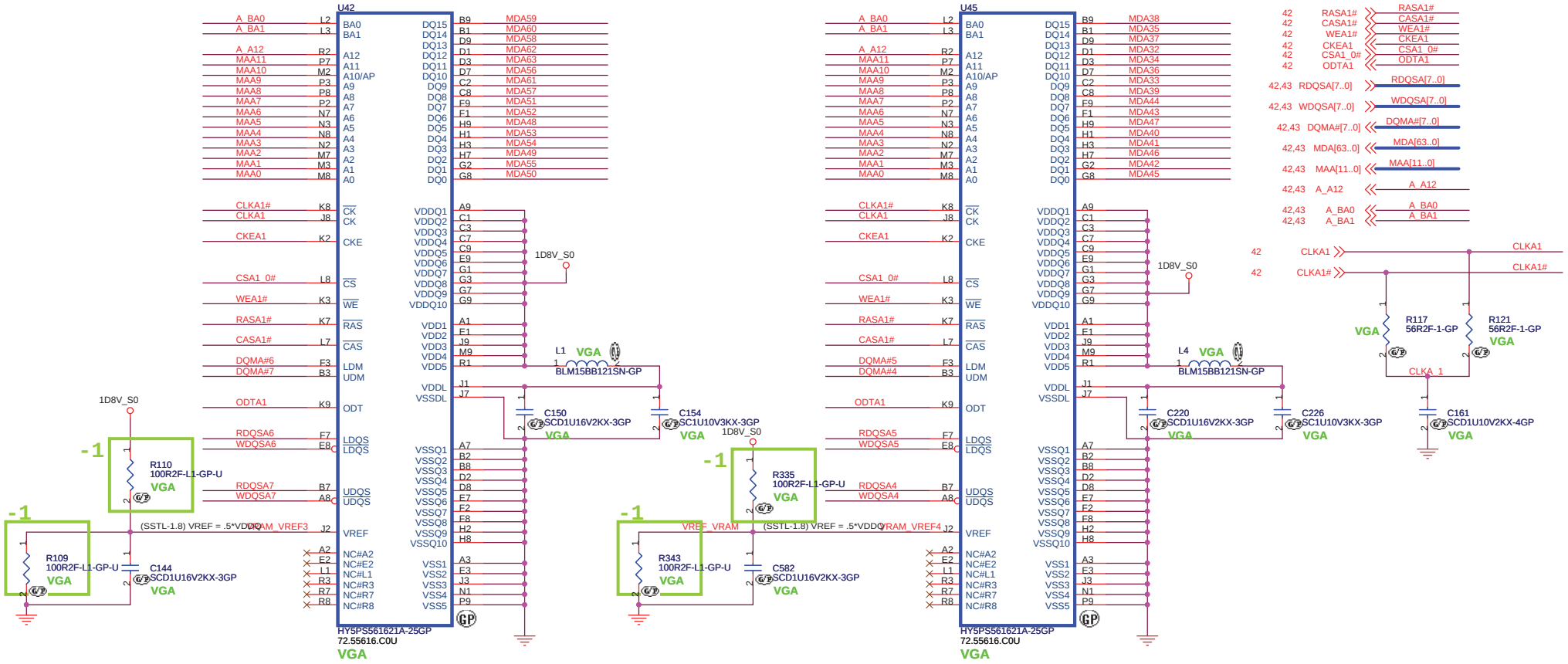
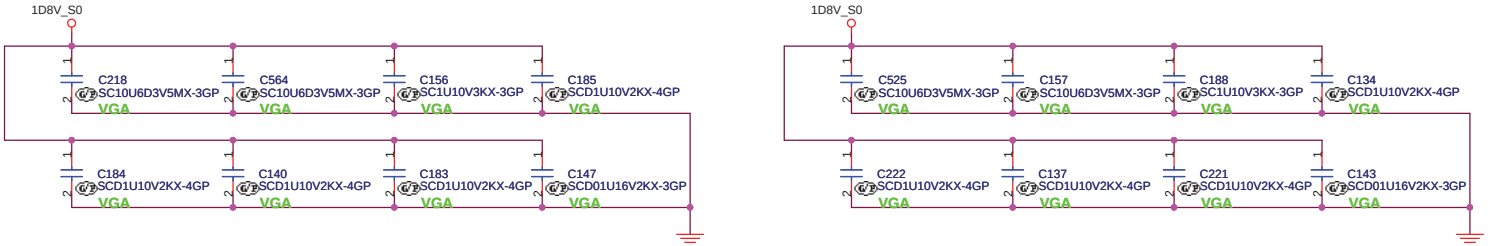
DDR2 BGA MEMORY (16M x 16)



Second Source: Qimonda 72.18256.B0U



緯創資通	**Wistron Corporation** 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	***VGA-VRAM(2/2)***	
Size A3	Document Number **C45/C46**	Rev **SA**
Date: Thursday, April 26, 2007	Sheet 44 of 45	

History

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2006/11/17
1. Schematic drawing start..
2006/12/12
1. Change to project name to C45/C46
2007/01/08
1. LAB gerber out

BOM Change (LAB)

==========

2006/12/29
1. VGA Change to M72, VRAM 128MB, but verify M71 (71.0M71M.M02) and M72(71.0M72M.M01) in LAB
2. 965GM (71.GM965.00U)
3. 965PM (71.PM965.00U)
4. RTS5158 (71.08111.A03)
5. ME stand off 34.4G901.001 (H23, H25, H9, H11) for MINI Card
6. ME stand off 34.4B601.001 (H26, H27) for MODEM
7. ME stand off 87.00055.120 (H4) for LVDS
8. ICH8-M (71.ICH8M.A0U)

LAB Chipset Part Number

C45:

NB: 71.CREST.M03
SB: 71.0ICH8.M08

C46:

NB: 71.CREST.A0U
SB: 71.0ICH8.M08

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: HISTORY

Size: A3 | Document Number: C45/C46 | Rev: SA

Date: Wednesday, March 07, 2007 | Sheet 45 of 45