Intel Calpella BlOCK DIAGRAM

Intel Calpella Arrandale UMA

01

POWER

SYSTEM RESET CIRCUIT

BATT CHARGER

AC/BATT CONNECTOR

RUN POWER SW

+3V_S5/+5V_S5

+3V_SUS/+5V_SUS

+5V_RUN/+3V_RUN/+1.8V_RUN

FAN & THERMAL

CLOCK
SLG8SP585VTR
(QFN-32)

POWER

REGULATOR
+1.5V_SUS/+0.75V_DDR_VTT

+1.05V_PCH

+1.05V_VTT

CPU VR

DC/DC
+3VPCU/+5VPCU/

CPU
Arrandale 35W
37.5mm X 37.5mm
(rPGA 989)

DDR3-SODIMM1 CHA

DDR3-SODIMM2 CHB

Dual Channel DDR3
1066 1.5V

FDI

DMI X 4

PCH
82801IBM
(HM55)
27mm X 25mm

SATA-ODD

SATA-HDD

SATA

SATA

IHDA

AUDIO/AMP
ALC269

Audio SPK conn

Audio Jacks

LPC

EC
ITE8502

18X8

Keyboard

SPI

PS/2

FLASH 2Mbyts

Touchpad

SPI

FLASH 2Mbyts

HDMI

LVDS

VGA

USB2.0 x 3

PCIEx1

PCIEx1

PCIEx1

PCIEx1

PS8101

HDMI

Panel Connector

CRT CONN.

USB conn x 3

Card Reader SD MS CARD
RTS5159

GLAN 10/100/1000 LAN
Realtek RTL8111E-GR

MINI-CARD
WLAN

NEW CARD

W83L351YG

MINI-CARD
3G

Quanta Computer Inc.

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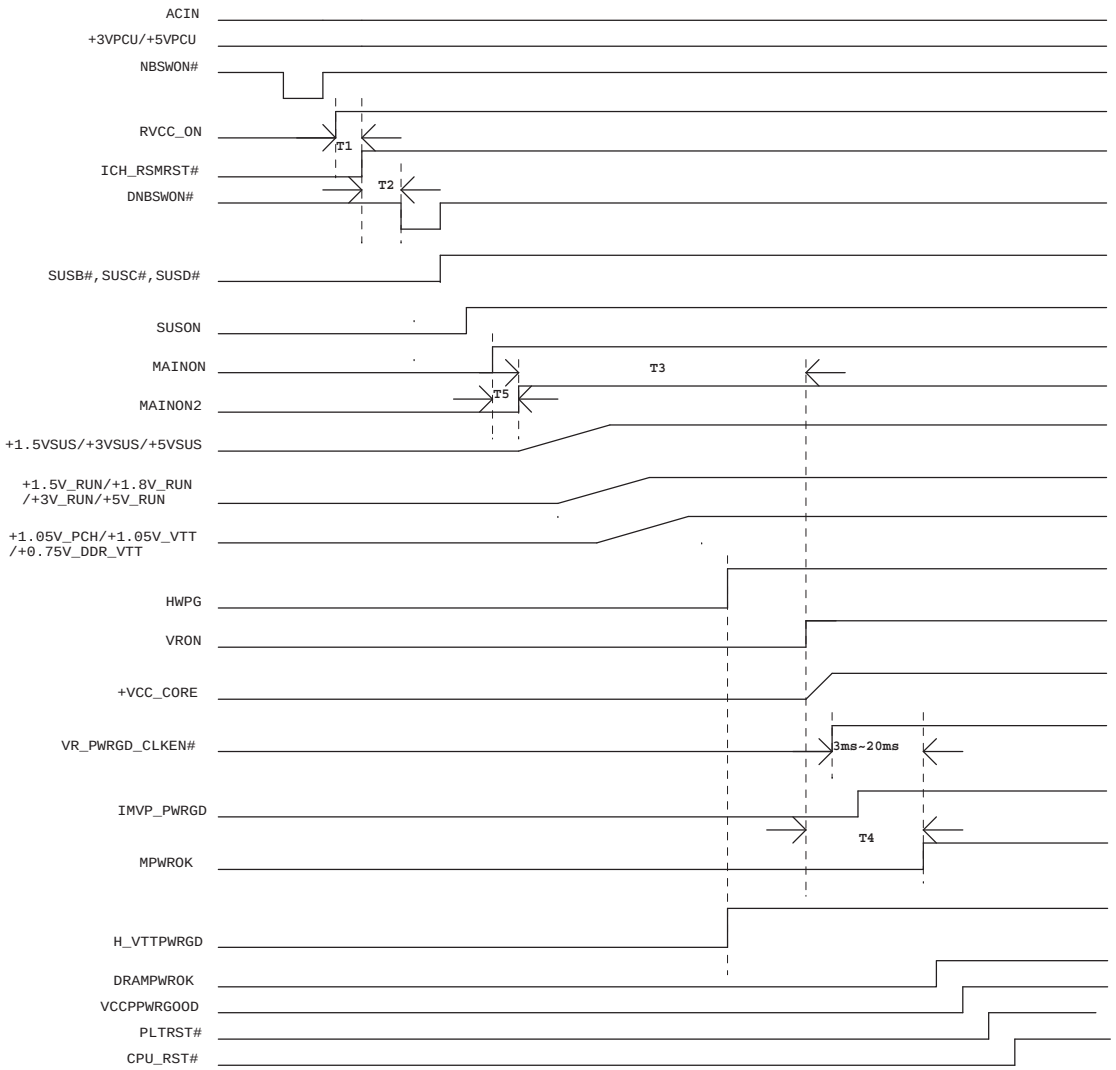
Power Sequence



T1: RVCCON TO RSMRST# = 30ms (spec:mini 10ms)
T2: RSMRST# TO-DNBSWON = 110ms (spec:mini 100ms)
T3: MAINON2 TO VRON = 110ms (spec:mini 99ms)
T4: VRON TO MPWROK = 10ms (HWPG NEED TO BE HIGH at that time)
Note: IMVP_CLK_EN# (inverted) assertion to SYS_PWROK/PCH_PWROK assertion.
SPEC:3ms~20ms
T5: MAINON to MAINON2 =500us

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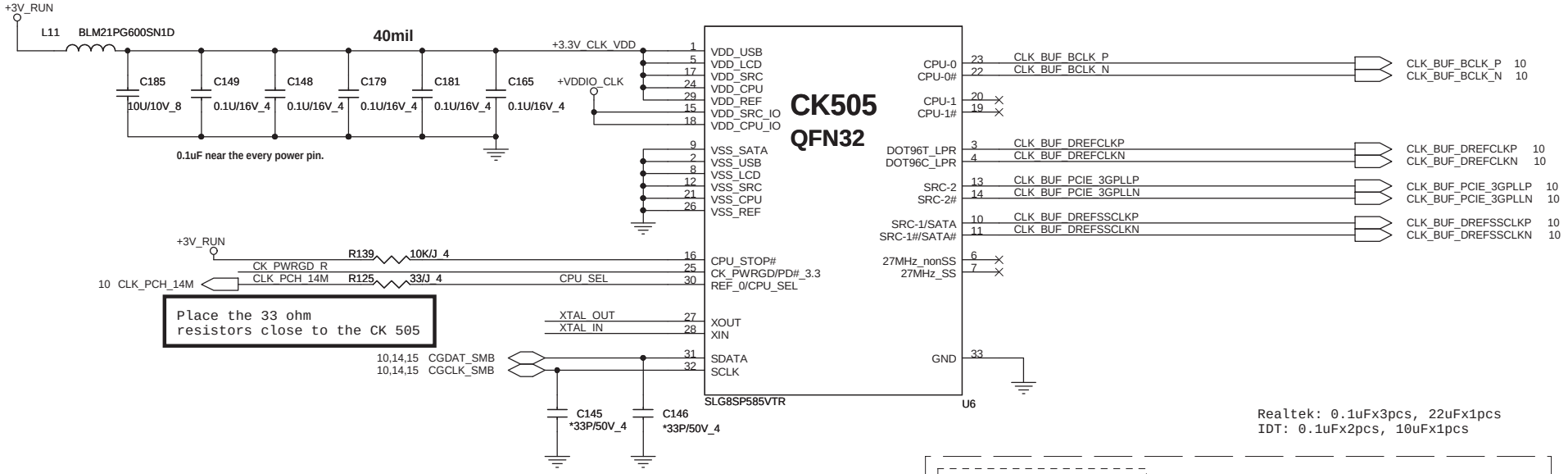
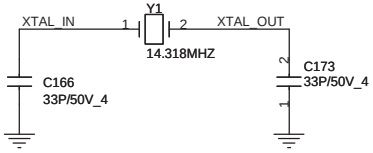
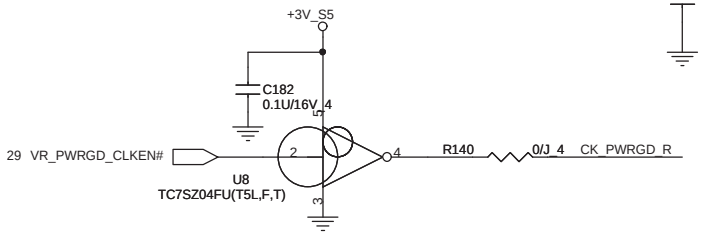
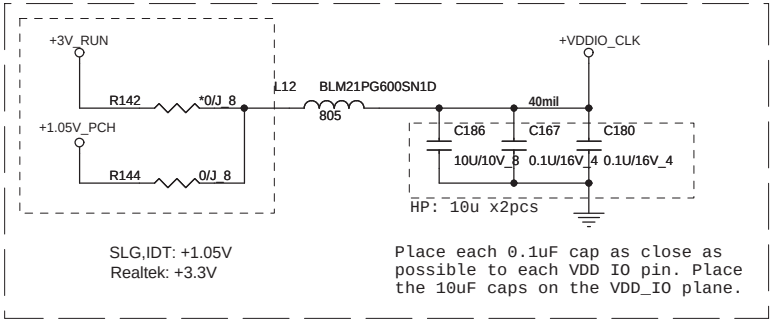


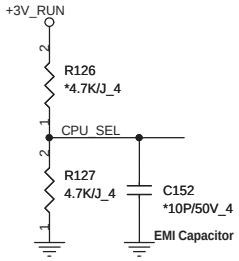






Realtek: 0.1uFx3pcs, 22uFx1pcs
IDT: 0.1uFx2pcs, 10uFx1pcs

+VDDIO_CLK:
SLG date sheet (V0.2) P15: Min 1.05V,Max3.465V.
Realtek date sheet(V1.2) P11: Min 1.05V,Max 3.3V.
IDT date sheet(V0.7) P10: Min 0.9975V,Max 3.465V.



PIN 30	CPU_0	CPU_1
0(default)	133MHz	133MHz
1(0.7V-1.5V)	100MHz	100MHz

CPU_SEL:
SLG date sheet (V0.2) P15:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
Realtek date sheet(V1.2) P11:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.
IDT date sheet(V0.7) P10:
High Voltage: Min 0.7V, Max 1.5V.
Low Voltage: Min Vss-0.3V, Max 0.35V.

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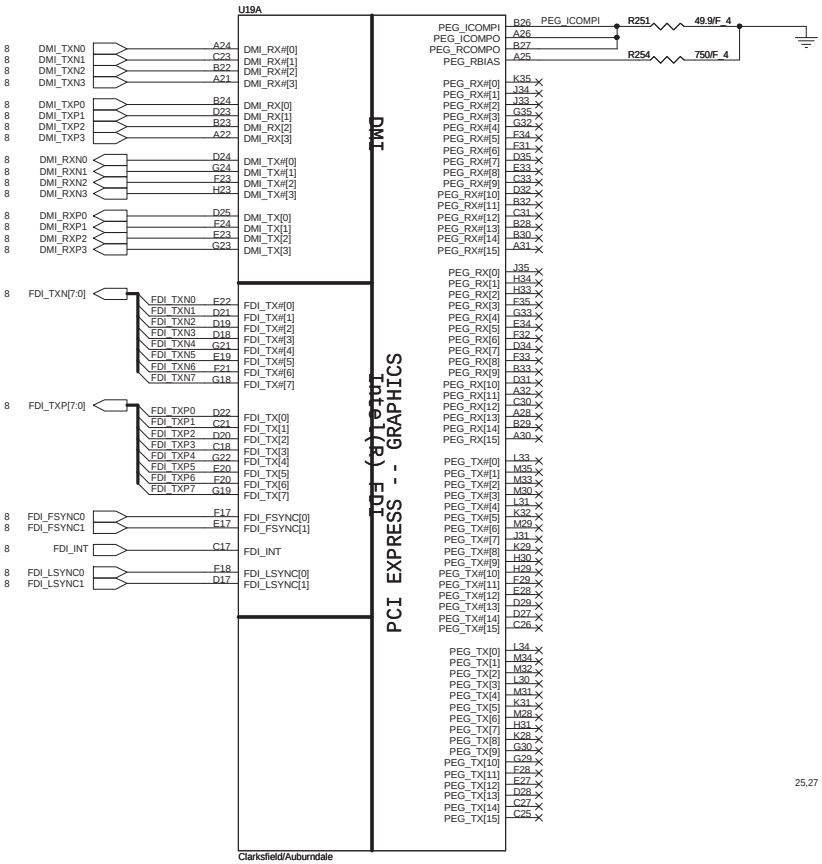
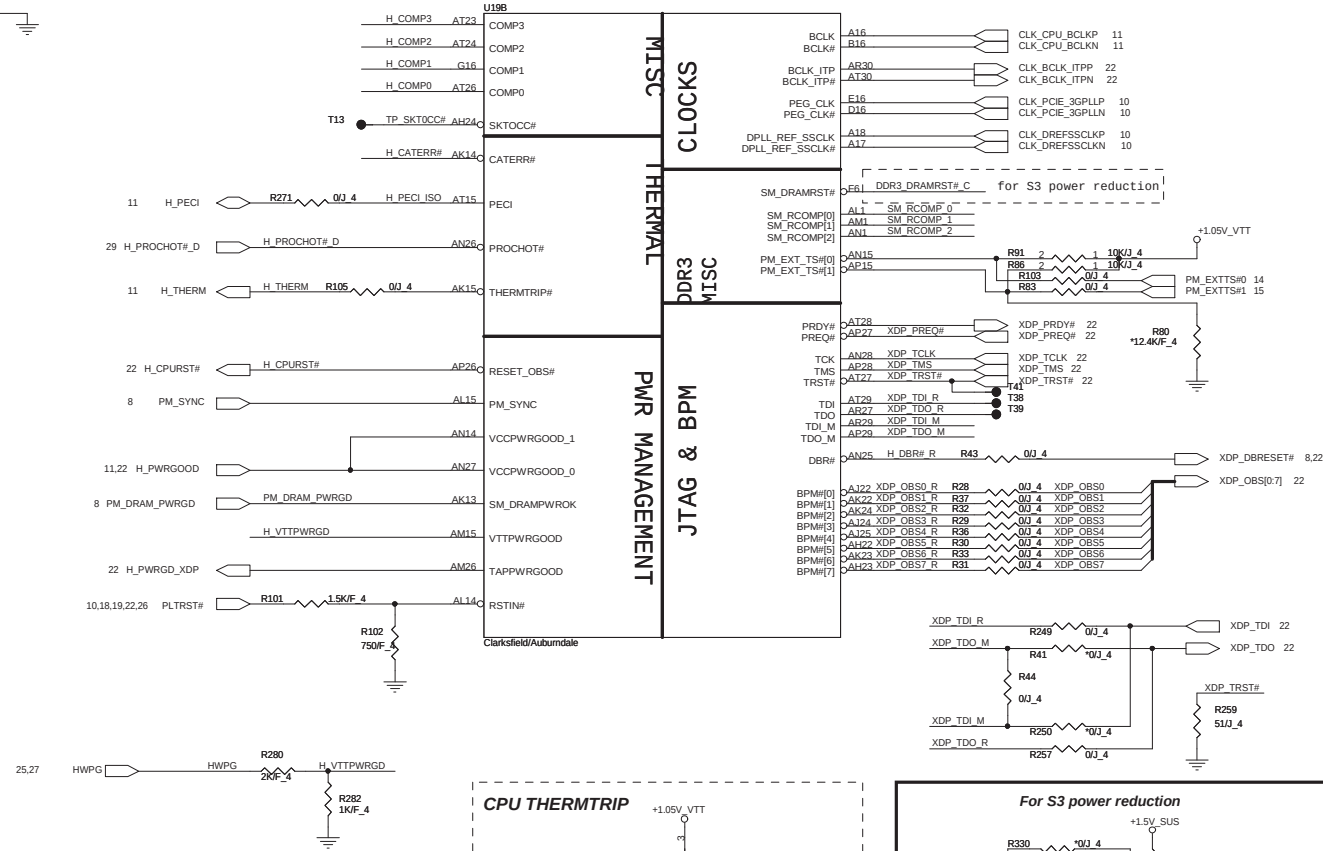
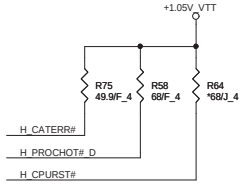
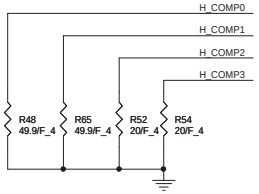




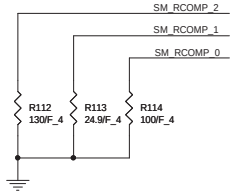
Processor Pullups

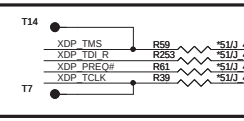


Processor Compensation Signals

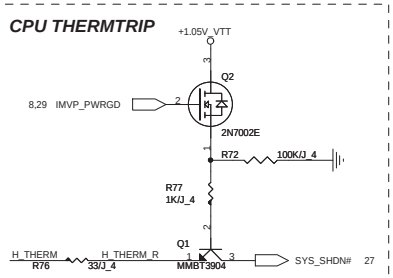


DDR3 Compensation Signals

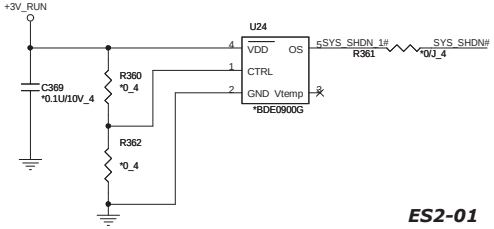




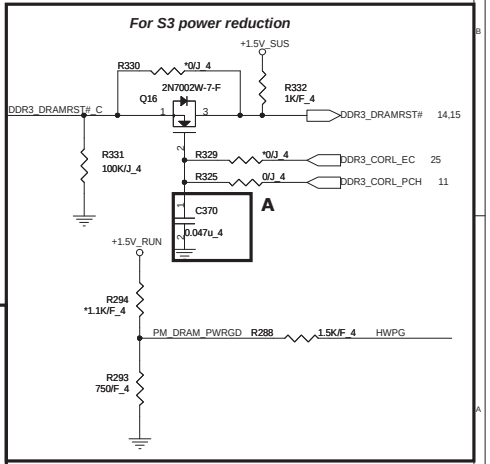
CPU THERMTRIP



CPU THERM SENSOR



For S3 power reduction



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ARRANDALE PROCESSOR (DDR3)

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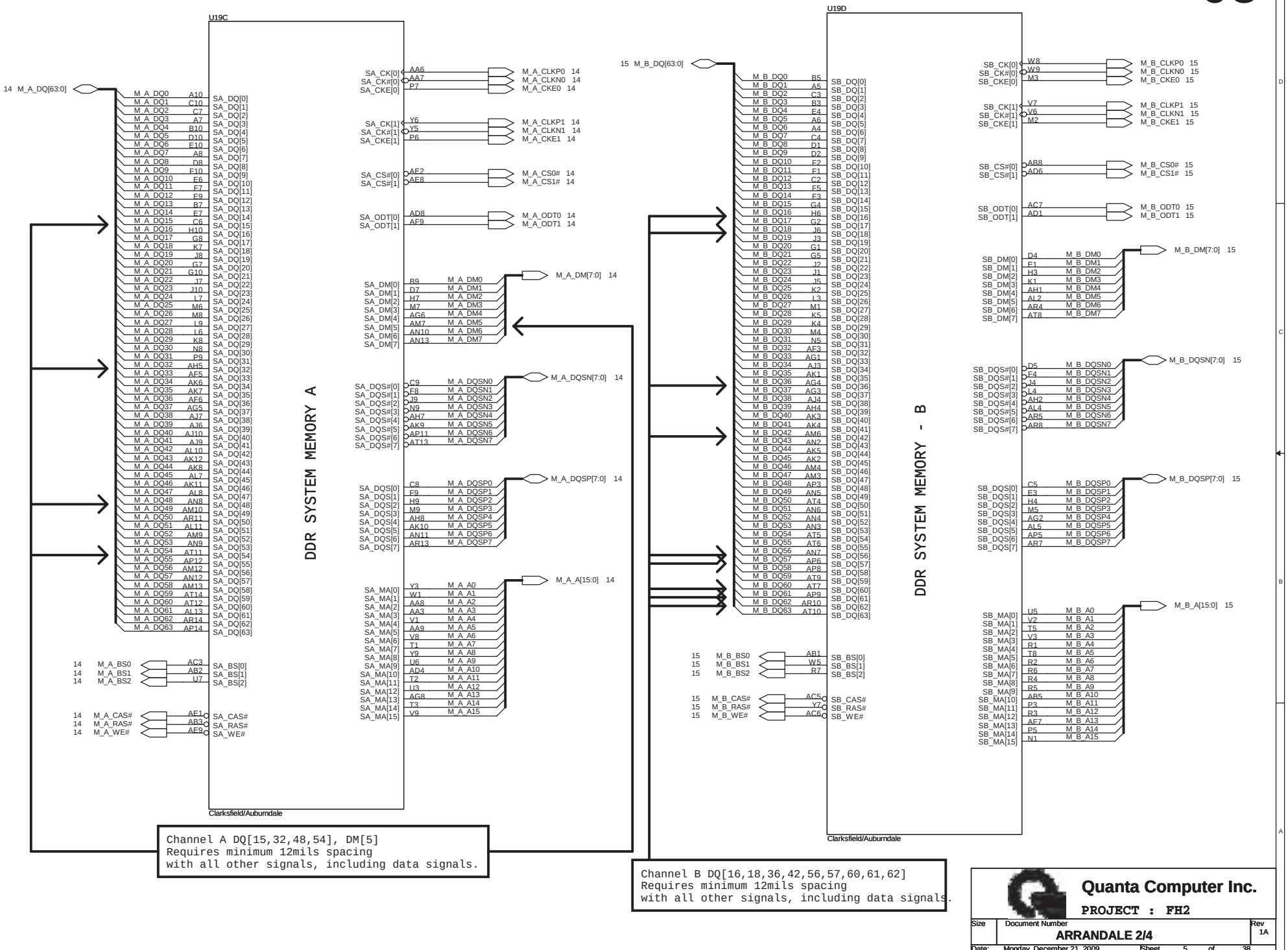

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ARRANDALE PROCESSOR (GRAPHICS POWER)

CPU Core Power

+VCC_CORE=4.8 max

U19F

+VCC_CORE

AG35 VCC1 AG34 VCC2 AG33 VCC3 AG32 VCC4 AG31 VCC5 AG30 VCC6 AG29 VCC7 AG28 VCC8 AG27 VCC9 AG26 VCC10 AF35 VCC11 AF34 VCC12 AF33 VCC13 AF32 VCC14 AF31 VCC15 AF30 VCC16 AF29 VCC17 AF28 VCC18 AF27 VCC19 AF26 VCC20 AD35 VCC21 AD34 VCC22 AD33 VCC23 AD32 VCC24 AD31 VCC25 AD30 VCC26 AD29 VCC27 AD28 VCC28 AD27 VCC29 AD26 VCC30 AC35 VCC31 AC34 VCC32 AC33 VCC33 AC32 VCC34 AC31 VCC35 AC30 VCC36 AC29 VCC37 AC28 VCC38 AC27 VCC39 AC26 VCC40 AA35 VCC41 AA34 VCC42 AA33 VCC43 AA32 VCC44 AA31 VCC45 AA30 VCC46 AA29 VCC47 AA28 VCC48 AA27 VCC49 AA26 VCC50 Y35 VCC51 Y34 VCC52 Y33 VCC53 Y32 VCC54 Y31 VCC55 Y30 VCC56 Y29 VCC57 Y28 VCC58 Y27 VCC59 Y26 VCC60 V35 VCC61 V34 VCC62 V33 VCC63 V32 VCC64 V31 VCC65 V30 VCC66 V29 VCC67 V28 VCC68 V27 VCC69 V26 VCC70 U35 VCC71 U34 VCC72 U33 VCC73 U32 VCC74 U31 VCC75 U30 VCC76 U29 VCC77 U28 VCC78 U27 VCC79 U26 VCC80 R35 VCC81 R34 VCC82 R33 VCC83 R32 VCC84 R31 VCC85 R30 VCC86 R29 VCC87 R28 VCC88 R27 VCC89 R26 VCC90 P35 VCC91 P34 VCC92 P33 VCC93 P32 VCC94 P31 VCC95 P30 VCC96 P29 VCC97 P28 VCC98 P27 VCC99 P26 VCC100

1.1V RAIL POWER

CPU CORE SUPPLY

VTT0_1 AH14 VTT0_2 AH12 VTT0_3 AH11 VTT0_4 AH10 VTT0_5 J14 VTT0_6 J13 VTT0_7 H14 VTT0_8 H12 VTT0_9 G14 VTT0_10 G13 VTT0_11 G12 VTT0_12 G11 VTT0_13 F14 VTT0_14 F13 VTT0_15 F12 VTT0_16 F11 VTT0_17 E14 VTT0_18 E12 VTT0_19 D14 VTT0_20 D13 VTT0_21 D12 VTT0_22 D11 VTT0_23 C14 VTT0_24 C13 VTT0_25 C12 VTT0_26 C11 VTT0_27 B14 VTT0_28 B12 VTT0_29 A14 VTT0_30 A13 VTT0_31 A12 VTT0_32 A11

+1.05V_VTT=1.8 max

+1.05V_VTT

C318 10U/6.3V_8 C103 10U/6.3V_8 C107 10U/6.3V_8 C311 10U/6.3V_8 C309 *10U/6.3V_8

C102 10U/6.3V_8 C105 10U/6.3V_8 C326 10U/6.3V_8 C99 10U/6.3V_8

+VCC_GFX_CORE

C97 10U/6.3V_8

+1.05V_VTT

C329 22U/6.3V_8 C313 22U/6.3V_8 C304 22U/6.3V_8

+C88 330U/2.5V_7343 C98 22U/6.3V_8 C63 22U/6.3V_8

VTT0_33 AF10 VTT0_34 AE10 VTT0_35 AC10 VTT0_36 AB10 VTT0_37 Y10 VTT0_38 W10 VTT0_39 U10 VTT0_40 T10 VTT0_41 J12 VTT0_42 J11 VTT0_43 J16 VTT0_44 J15

+1.05V_VTT

C308 22U/6.3V_8 C96 22U/6.3V_8

+1.05V_VTT

C319 22U/6.3V_8 C101 22U/6.3V_8

J24 J23 H25 VTT1_45 VTT1_46 VTT1_47

C317 22U/6.3V_8 C316 22U/6.3V_8

C331 22U/6.3V_8 C315 22U/6.3V_8

K26 J27 J26 J25 H27 G28 G27 G26 F26 E26 E25 VTT1_48 VTT1_49 VTT1_50 VTT1_51 VTT1_52 VTT1_53 VTT1_54 VTT1_55 VTT1_56 VTT1_57 VTT1_58

PDI & DMI

POWER

CPU VIDS

PSI# AN33 H_PSI# H_PSI# 29

VID[0] AK35 VID0 VID0 29
VID[1] AK33 VID1 VID1 29
VID[2] AK34 VID2 VID2 29
VID[3] AL35 VID3 VID3 29
VID[4] AL33 VID4 VID4 29
VID[5] AM33 VID5 VID5 29
VID[6] AM35 VID6 VID6 29
PROC_DPRSLPVR AM34 DPRSLPVR DPRSLPVR 29

VTT_SELECT G15 H_VTTVID1 30

VTT0_43,VTT0_44:(Intel feedback)
They are connected to hidden page for
intel validation purpose.

SENSE LINES

ISENSE AN35 I_MON 29

VCC_SENSE AJ34 VSS_SENSE AJ35 VCCSENSE 29 VSSSENSE 29

VTT_SENSE B15 VSS_SENSE_VTT A15 VTT_SENSE 30 VSS_SENSE_VTT 30

VSS_SENSE_VTT:
SC(V1.0)P20
Connect VSS_SENSE_VTT to GND
or can be left floating.
Note: CRB has the VSS_SENSE_VTT floating.

+VCC_CORE

R216 100/F_4

R217 100/F_4

VCC_SENSE & VSS_SENSE:
SC(V1.0)P19
100- ±1% pull-down to GND near processor

PROC_DPRSLPVR:
SC(V1.0)P19:
It is important to have the resistor stuffing options in the design for the Turbo functionality.
The stuffing and no-stuffing of the resistors will depend on the POC configuration of AUB and CFD
CRB(V1.0)P67:
uses 1K pull-up and pull-down resistors
CRB default setting is "1"

Clarksfield/Auburndale

U19G

VAXG1 AT21 VAXG2 AT19 VAXG3 AT18 VAXG4 AT16 VAXG5 AR21 VAXG6 AR19 VAXG7 AR18 VAXG8 AR16 VAXG9 AP21 VAXG10 AP19 VAXG11 AP18 VAXG12 AP16 VAXG13 AN21 VAXG14 AN19 VAXG15 AN18 VAXG16 AN16 VAXG17 AM21 VAXG18 AM19 VAXG19 AM18 VAXG20 AM16 VAXG21 AL21 VAXG22 AL19 VAXG23 AL18 VAXG24 AL16 VAXG25 AK21 VAXG26 AK19 VAXG27 AK18 VAXG28 AK16 VAXG29 AJ21 VAXG30 AJ19 VAXG31 AJ18 VAXG32 AJ16 VAXG33 AH21 VAXG34 AH19 VAXG35 AH18 VAXG36 AH16

GRAPHICS

POWER

SENSE LINES

VAXG_SENSE AR22 VSSAXG_SENSE AT22 VGAU_VCCSENSE 31 VGAU_VSSSENSE 31

GRAPHICS VIDs

GFX_VID[0] AM22 GFX_VID[1] AP22 GFX_VID[2] AN22 GFX_VID[3] AP23 GFX_VID[4] AM23 GFX_VID[5] AP24 GFX_VID[6] AN24 VGAU_VID0 31 VGAU_VID1 31 VGAU_VID2 31 VGAU_VID3 31 VGAU_VID4 31 VGAU_VID5 31 VGAU_VID6 31

R67 4.7K_4

GFX_VR_EN AR25 GFX_DPRSLPVR AT25 GFX_IMON AM24 VGA_ON VGAU_DPRSLPVR 31 VGA_ON 31 VGAU_IMON

R256 *1K/F_4

DDR3 - 1.5V RAILS

VDDQ1 AJ1 VDDQ2 AF1 VDDQ3 AE7 VDDQ4 AE4 VDDQ5 AC1 VDDQ6 AB7 VDDQ7 AB4 VDDQ8 Y1 VDDQ9 W7 VDDQ10 W4 VDDQ11 U1 VDDQ12 T7 VDDQ13 T4 VDDQ14 P1 VDDQ15 N7 VDDQ16 N4 VDDQ17 L1 VDDQ18 H1

+1.5V_RUN

C125 1U/6.3V_4 C124 1U/6.3V_4 C127 1U/6.3V_4 C128 1U/6.3V_4 C126 1U/6.3V_4

+C122 330U/2.5V_7343 7343 2.5 C121 22U/6.3V_8 C120 22U/6.3V_8

1.1V

VTT0_59 P10 VTT0_60 N10 VTT0_61 L10 VTT0_62 K10

+1.05V_VTT

C104 10U/6.3V_8 C106 10U/6.3V_8 +C110 *330U/2.5V_7343

VTT1_63 J22 VTT1_64 J20 VTT1_65 J18 VTT1_66 H21 VTT1_67 H20 VTT1_68 H19

C330 22U/6.3V_8 C314 22U/6.3V_8

1.8V

VCCPLL1 L26 VCCPLL2 L27 VCCPLL3 M26

+1.8V_RUN

C42 1U/6.3V_4 C50 1U/6.3V_4 C65 2.2U/6.3V_6 C66 4.7U/6.3V_6 C297 22U/6.3V_8

+VCC_CORE

C281 22U/6.3V_8 C54 22U/6.3V_8 C302 22U/6.3V_8 C52 22U/6.3V_8 C53 22U/6.3V_8 C291 22U/6.3V_8

C276 22U/6.3V_8 C38 22U/6.3V_8 C59 22U/6.3V_8 C58 22U/6.3V_8 C280 22U/6.3V_8 C285 22U/6.3V_8

C79 10U/6.3V_8 C56 10U/6.3V_8 C36 10U/6.3V_8 C81 10U/6.3V_8 C55 10U/6.3V_8 C299 10U/6.3V_8

C301 10U/6.3V_8 C300 10U/6.3V_8 C286 10U/6.3V_8 C80 10U/6.3V_8 C35 10U/6.3V_8 C82 10U/6.3V_8

C57 10U/6.3V_8 C37 10U/6.3V_8 C78 10U/6.3V_8 C303 10U/6.3V_8

+C277 *470U/6.3V_7343 +C90 *470U/6.3V_7343

+1.05V_VTT

R225 1K/J_4 R227 1K/J_4 R230 1K/J_4 R233 1K/J_4 R236 1K/J_4 R239 1K/J_4 R243 1K/J_4 R208 1K/J_4 R209 *1K/J_4

VID0 VID1 VID2 VID3 VID4 VID5 VID6 DPRSLPVR H_PSI#

R226 *1K/J_4 R228 *1K/J_4 R231 *1K/J_4 R234 1K/J_4 R237 1K/J_4 R240 *1K/J_4 R244 1K/J_4 R213 *1K/J_4 R214 1K/J_4

Note:
For Validating IMVP VR R814 should be STUFF and R827 NO_STUFF

Clarksfield/Auburndale

For S3 power reduction

Check to ensure that 4 stitching caps per SODIMM connector between SODIMM 1.5V and GND are placed as close as possible to the connectors – caps should be evenly distributed between the connectors

AUBURNDALE/CLARKSFIELD PROCESSOR (POWER)

Quanta Computer Inc.

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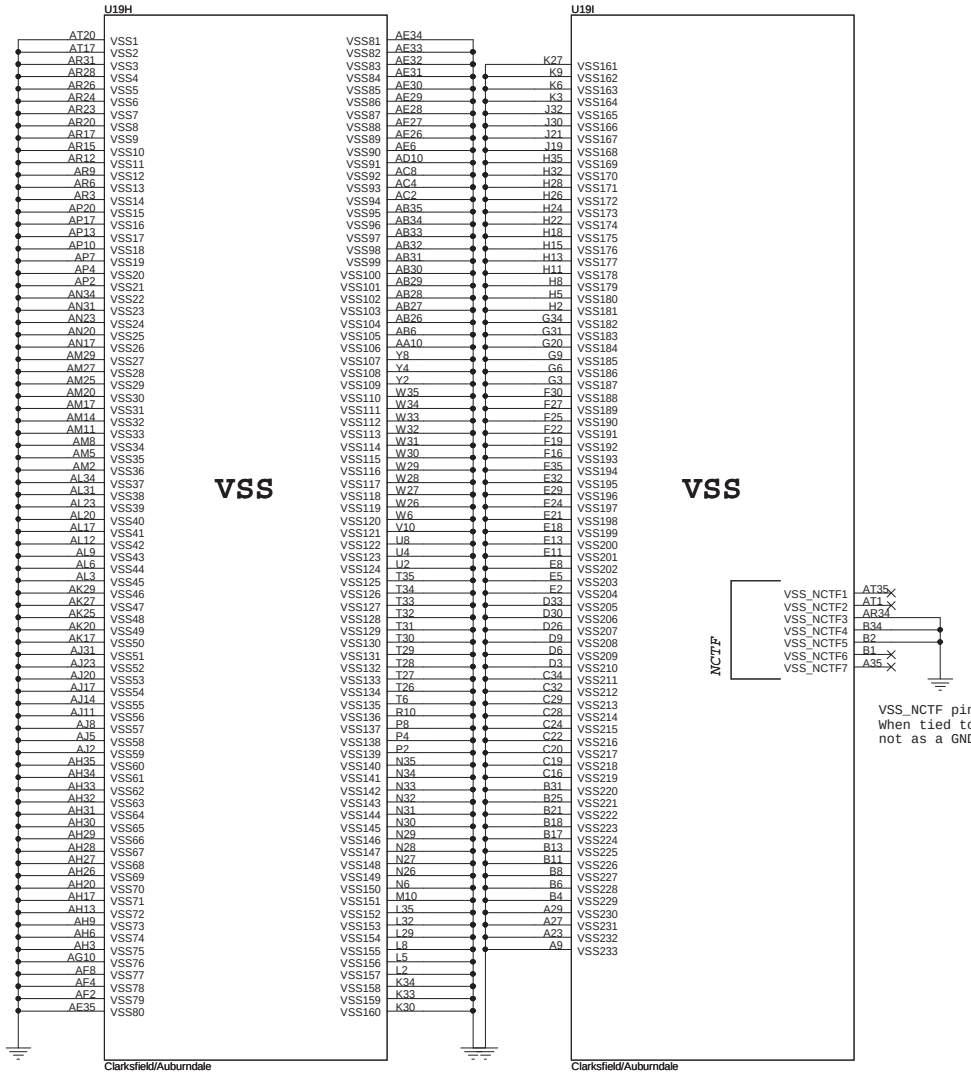
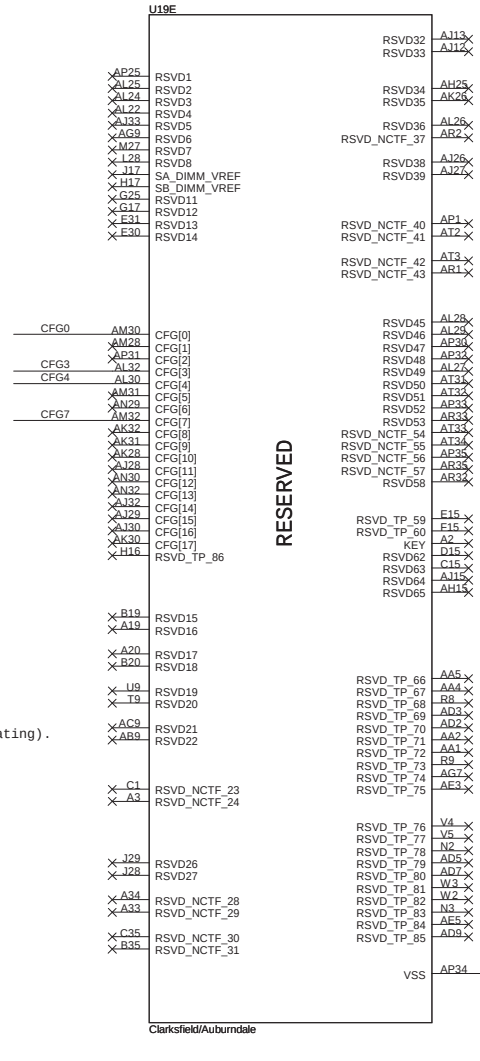
ARRANDALE PROCESSOR (GND)



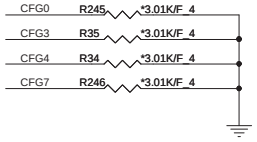
VSS_NCTF pins can be connected to GND or left as NC (floating). When tied to GND they should be routed as trace and not as a GND plane.

ARRANDALE PROCESSOR(RESERVED, CFG)



Can be left NC is Intel CRM implementation; ESD/DG recommendation to GND

The Clarkfield processor's PCI Express interface may not meet PCI Express 2.0 jitter specifications. Intel recommends placing a 3.01K +/- 5% pull down resistor to VSS on CFG[7] pin for both rPGA and BGA components. This pull down resistor should be removed when this issue is fixed.



	1	0
CFG4 (Display Port Presence)	Disabled; No Physical Display Port attached to Embedded Diplay Port	Enabled; An external Display port device is connected to the Embedded Display port
CFG0 (PCI-Epress Configuration Select)	Single PEG	Bifurcation enabled
CFG3 (PCI-Epress Static Lane Reversal)	Normal Operation	Lane Numbers Reversed

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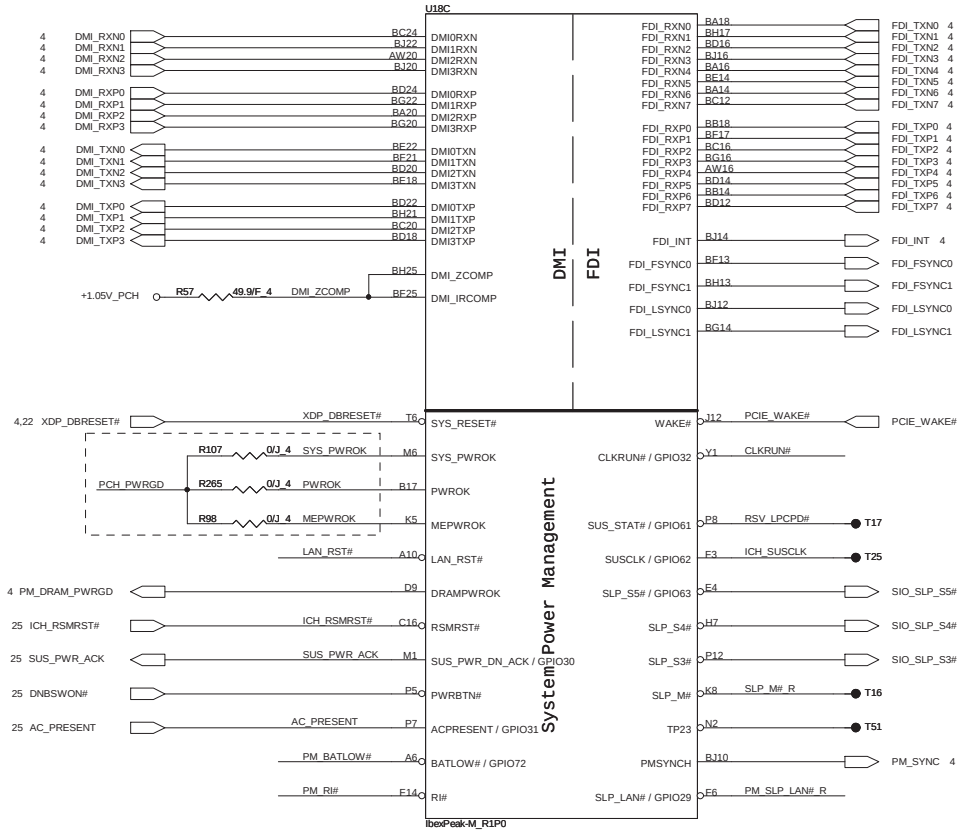
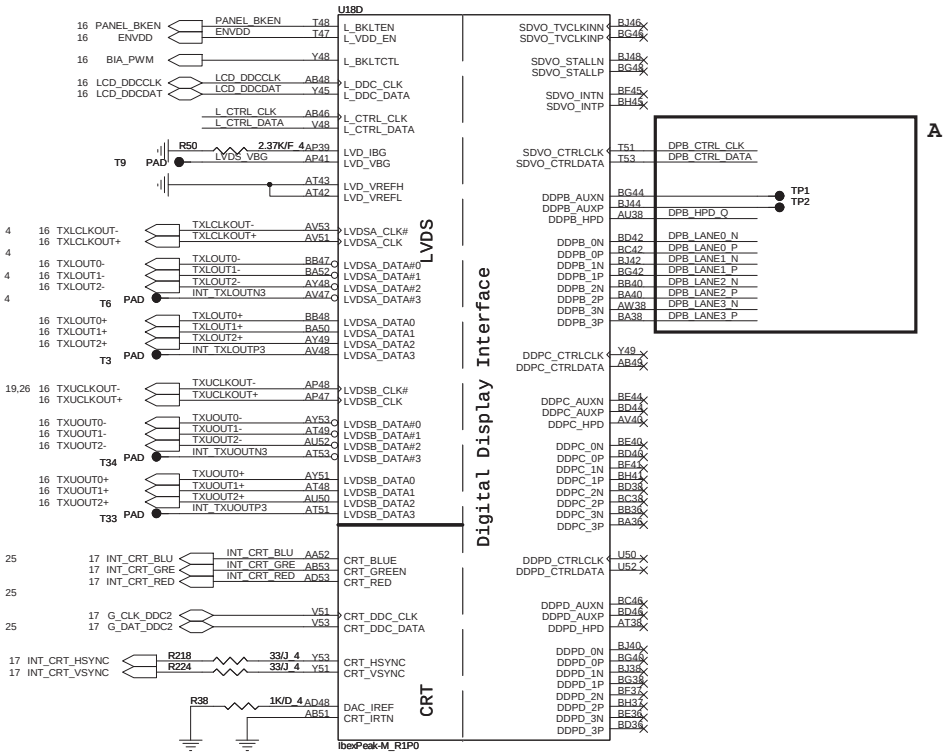
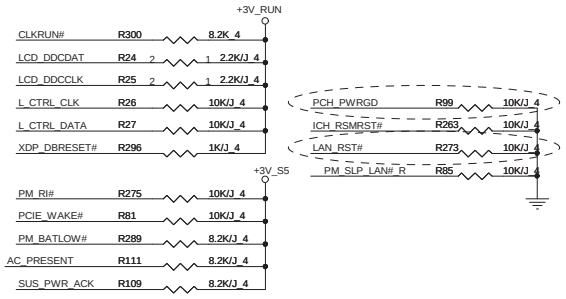
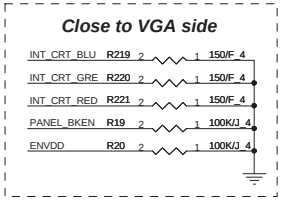
IBEX PEAK-M (DMI,FDI,GPIO)

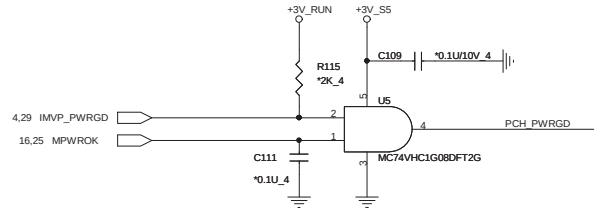


IBEX PEAK-M (LVDS,DDI)

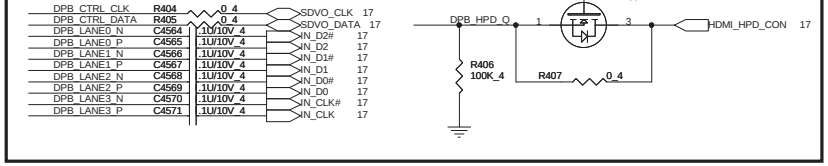








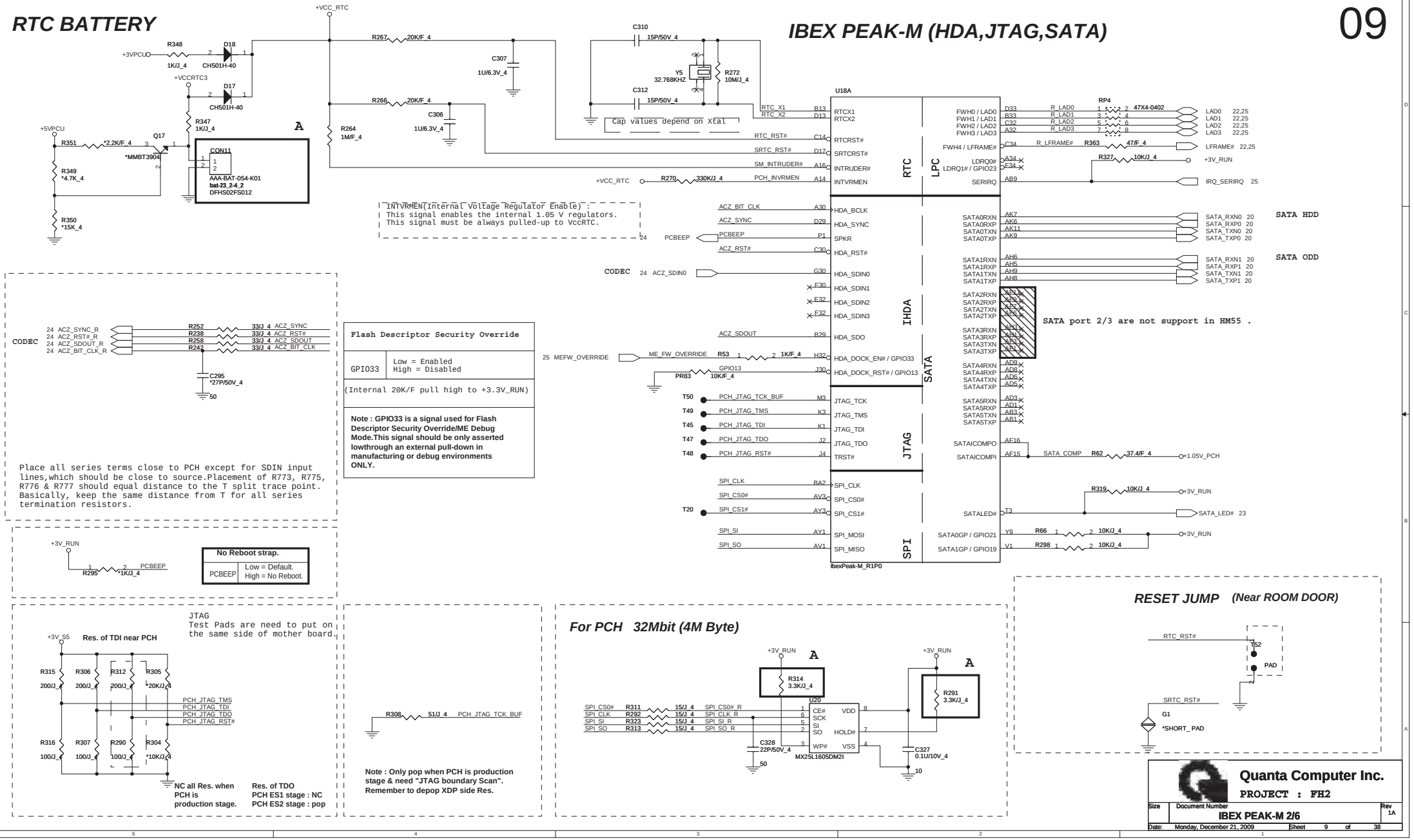
UMA HDMI signals



RTC BATTERY

IBEX PEAK-M (HDA,JTAG,SATA)

09



Place all series terms close to PCH except for SDIN input lines,which should be close to source.Placement of R773, R775, R776 & R777 should equal distance to the T split trace point. Basically, keep the same distance from T for all series termination resistors.

Flash Descriptor Security Override	
GPIO33	Low = Enabled High = Disabled
(Internal 20K/F pull high to +3.3V_RUN)	

Note : GPIO33 is a signal used for Flash Descriptor Security Override/ME Debug Mode.This signal should be only asserted lowthrough an external pull-down in manufacturing or debug environments ONLY.

No Reboot strap.	
PCBEEP	Low = Default. High = No Reboot.

JTAG
Test Pads are need to put on the same side of mother board.

NC all Res. when PCH is production stage.

Res. of TDO
PCH ES1 stage : NC
PCH ES2 stage : pop

Note : Only pop when PCH is production stage & need "JTAG boundary Scan". Remember to depop XDP side Res.

For PCH 32Mbit (4M Byte)

RESET JUMP (Near ROOM DOOR)

Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	IBEX PEAK-M 2/6	1A
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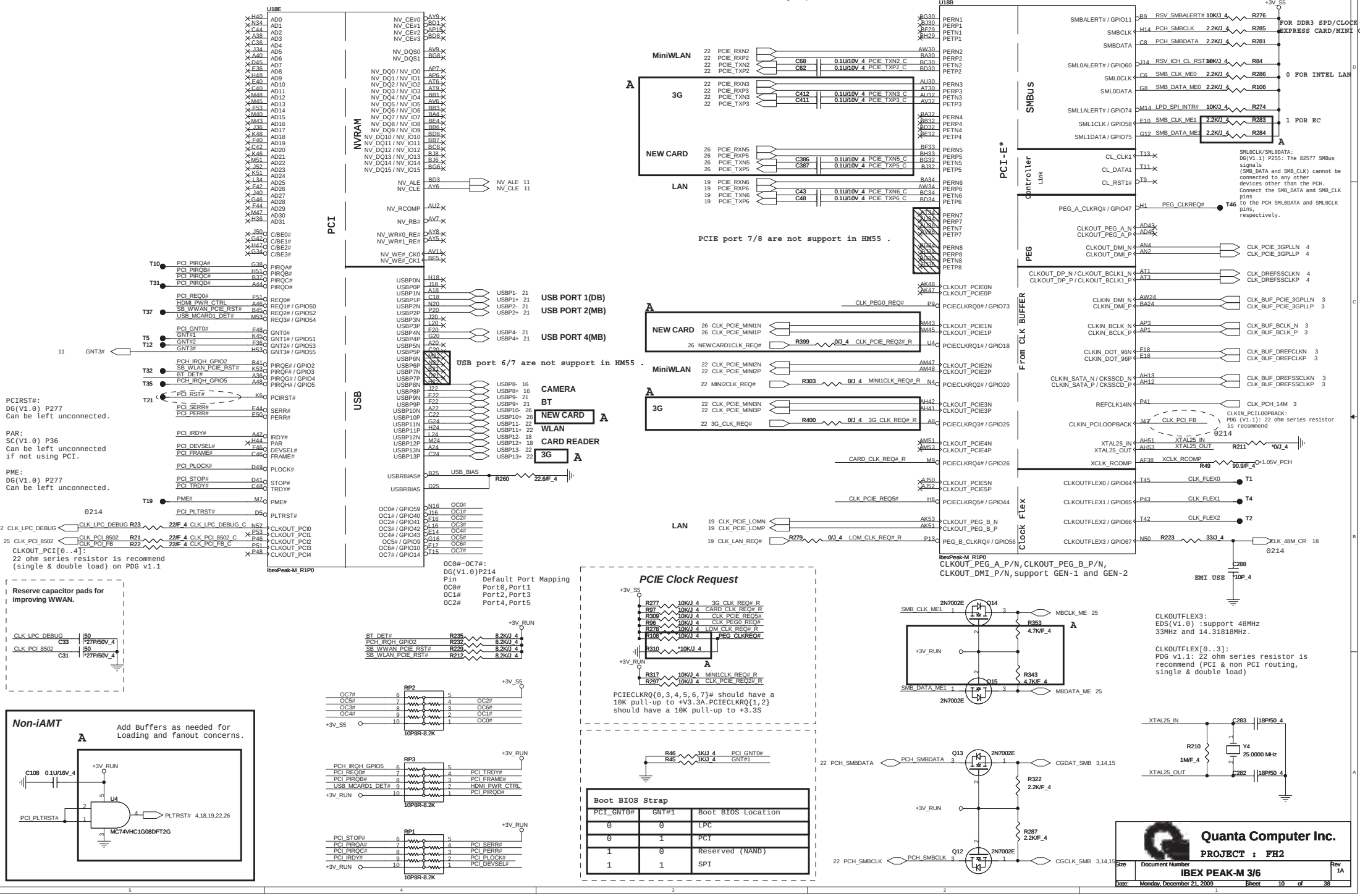
IBEX PEAK-M (PCI,USB,NVRAM)

IBEX PEAK-M (PCI-E,SMBUS,CLK)

Place TX DC blocking caps close PCH.



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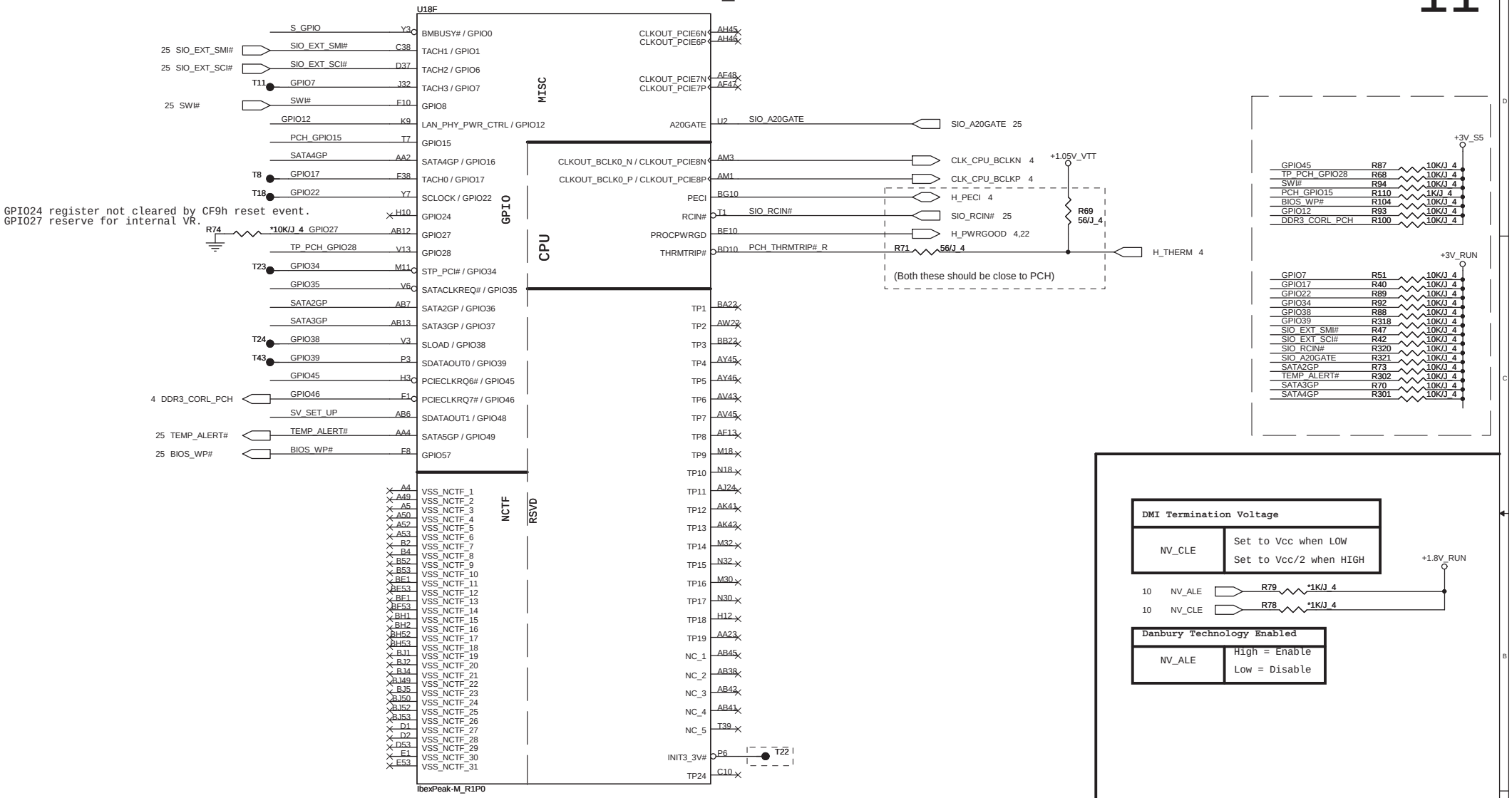
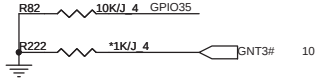
IBEX PEAK-M (GPIO,VSS_NCTF,RSVD)



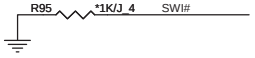
GPIO24 register not cleared by CF9h reset event.
GPIO27 reserve for internal VR.

DMI Termination Voltage	
NV_CLE	Set to Vcc when LOW Set to Vcc/2 when HIGH

Danbury Technology Enabled	
NV_ALE	High = Enable Low = Disable



A16 swap override Strap/Top-Block Swap Override jumper	
GNT3#	Low = A16 swap override/Top-Block Swap Override enabled High = Default



Integrated Clock Chip Enable (Reserve to validate for future platforms)	
RSV_WOL_EN (GPIO8)	Enable when sampled low Disable when sampled high

SV_SET_UP	1-X High = Strong (Default)

BMBUSY#:
If not used, require a weak pull-up (8.2- KΩ to 10 kΩ) to Vcc3_3.
CRB(V1.0)P28: it has 1K PU and 100 ohm on this net for validation purpose.

BMBUSY#:(Intel feedback)
Follow CRB checklist, 1K is
for intel BIOS validation purpose.

Quanta Computer Inc.
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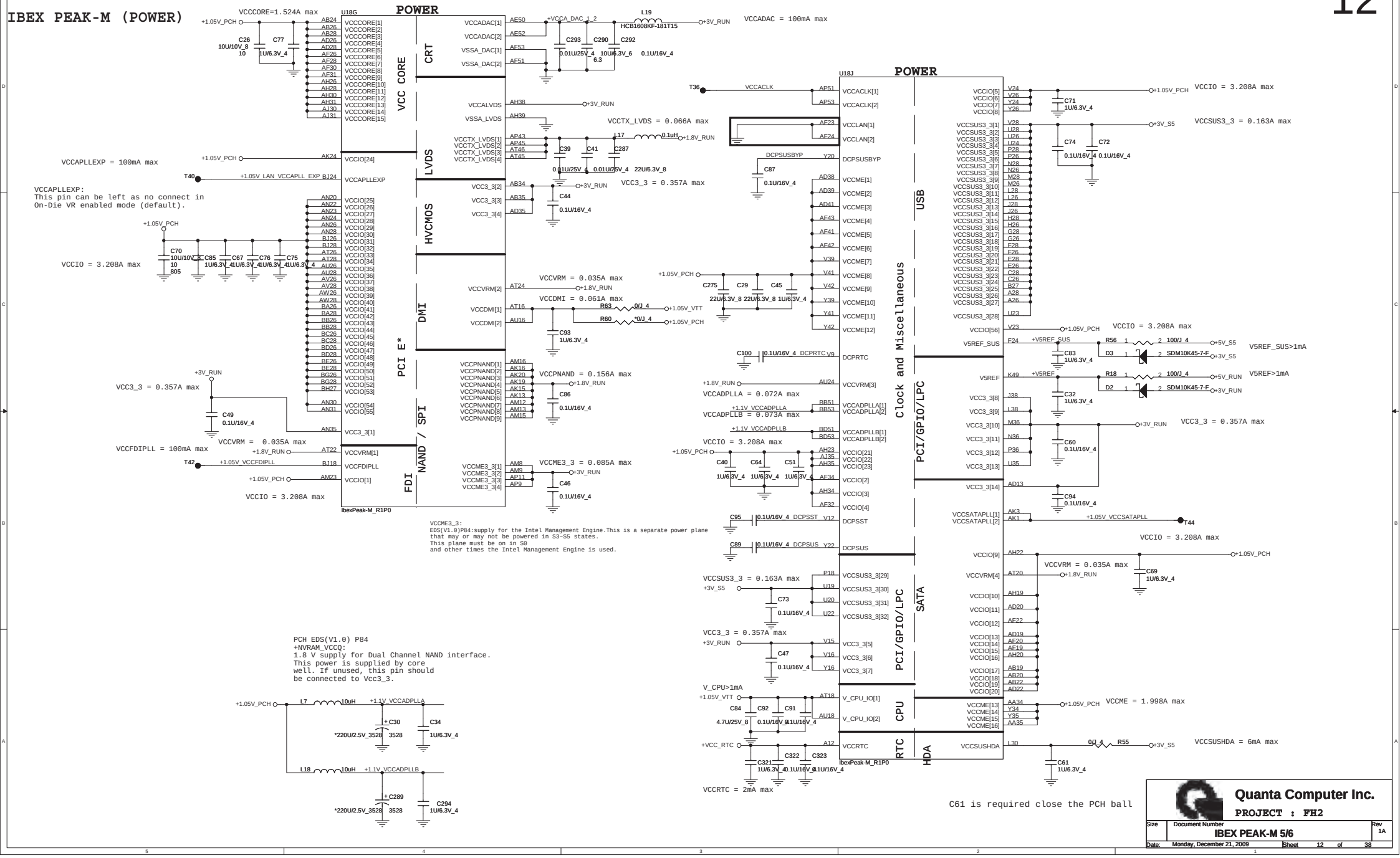
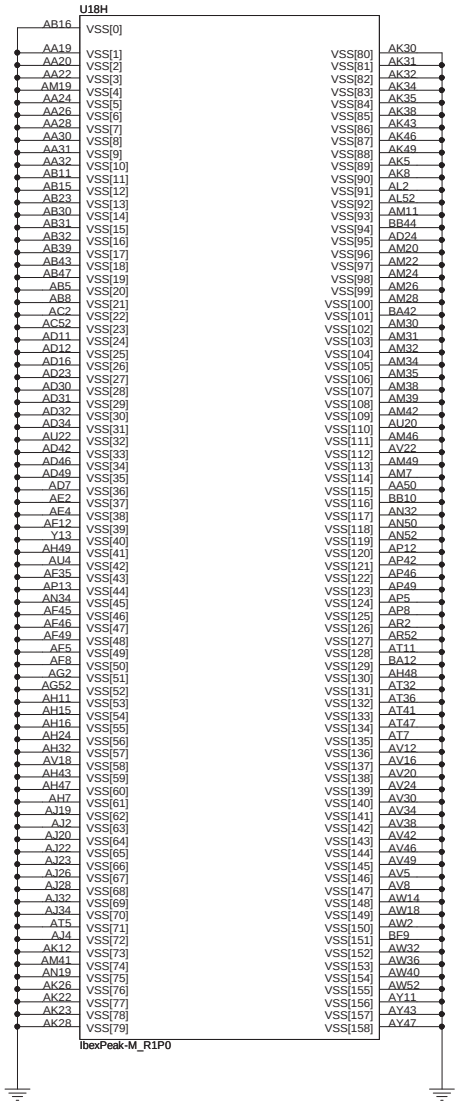
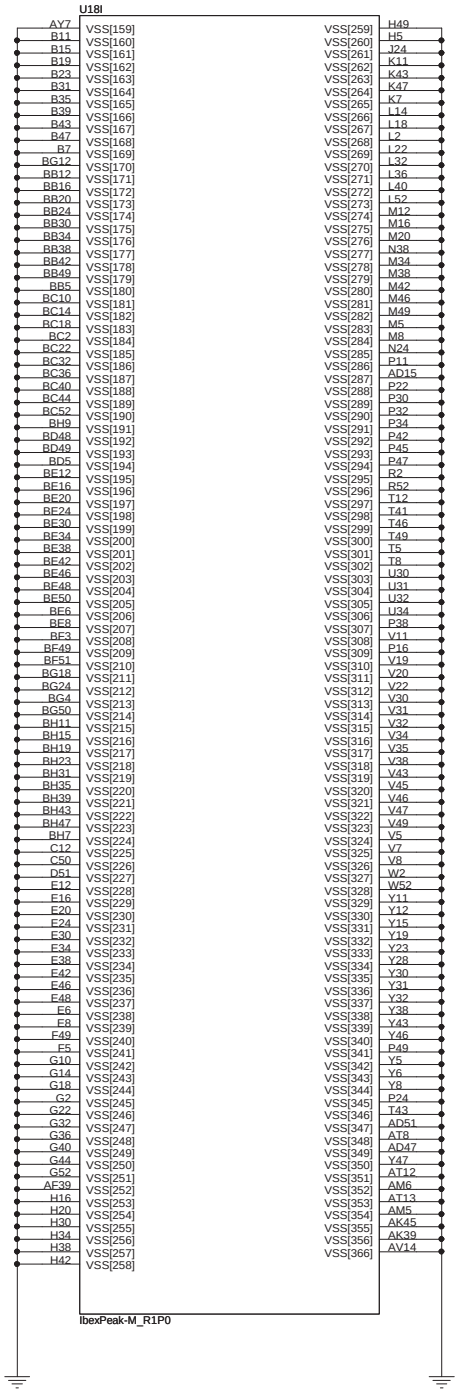
IBEX PEAK-M (POWER)



IBEX PEAK-M (GND)





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Size | Document Number: IBEX PEAK-M 6/6 | Rev: 1A
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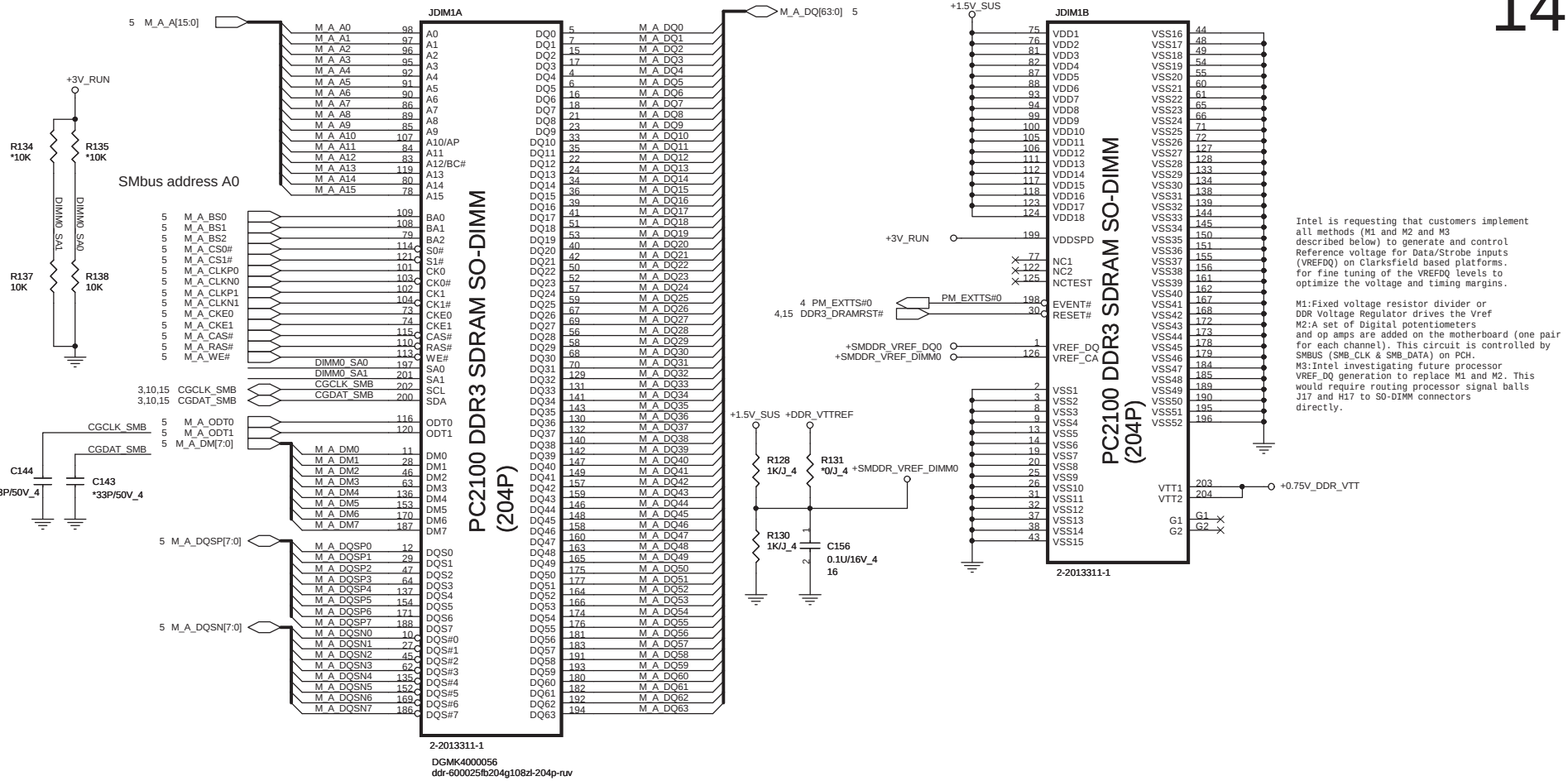
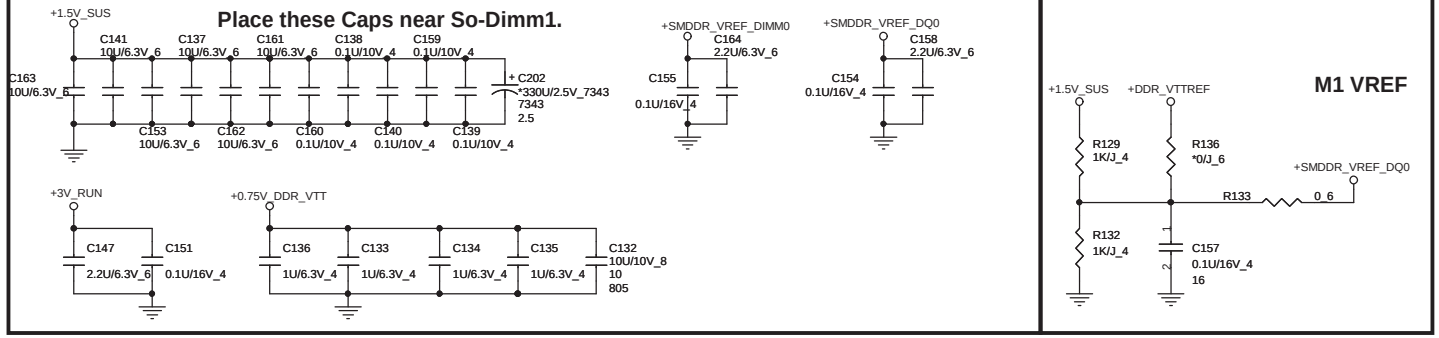


Intel is requesting that customers implement all methods (M1 and M2 and M3 described below) to generate and control Reference voltage for Data/Strobe inputs (VREFDQ) on Clarksfield based platforms. for fine tuning of the VREFDQ levels to optimize the voltage and timing margins.

M1:Fixed voltage resistor divider or DDR Voltage Regulator drives the Vref
M2:A set of Digital potentiometers and op amps are added on the motherboard (one pair for each channel). This circuit is controlled by SMBUS (SMB_CLK & SMB_DATA) on PCH.
M3:Intel investigating future processor VREF_DQ generation to replace M1 and M2. This would require routing processor signal balls J17 and H17 to SO-DIMM connectors directly.



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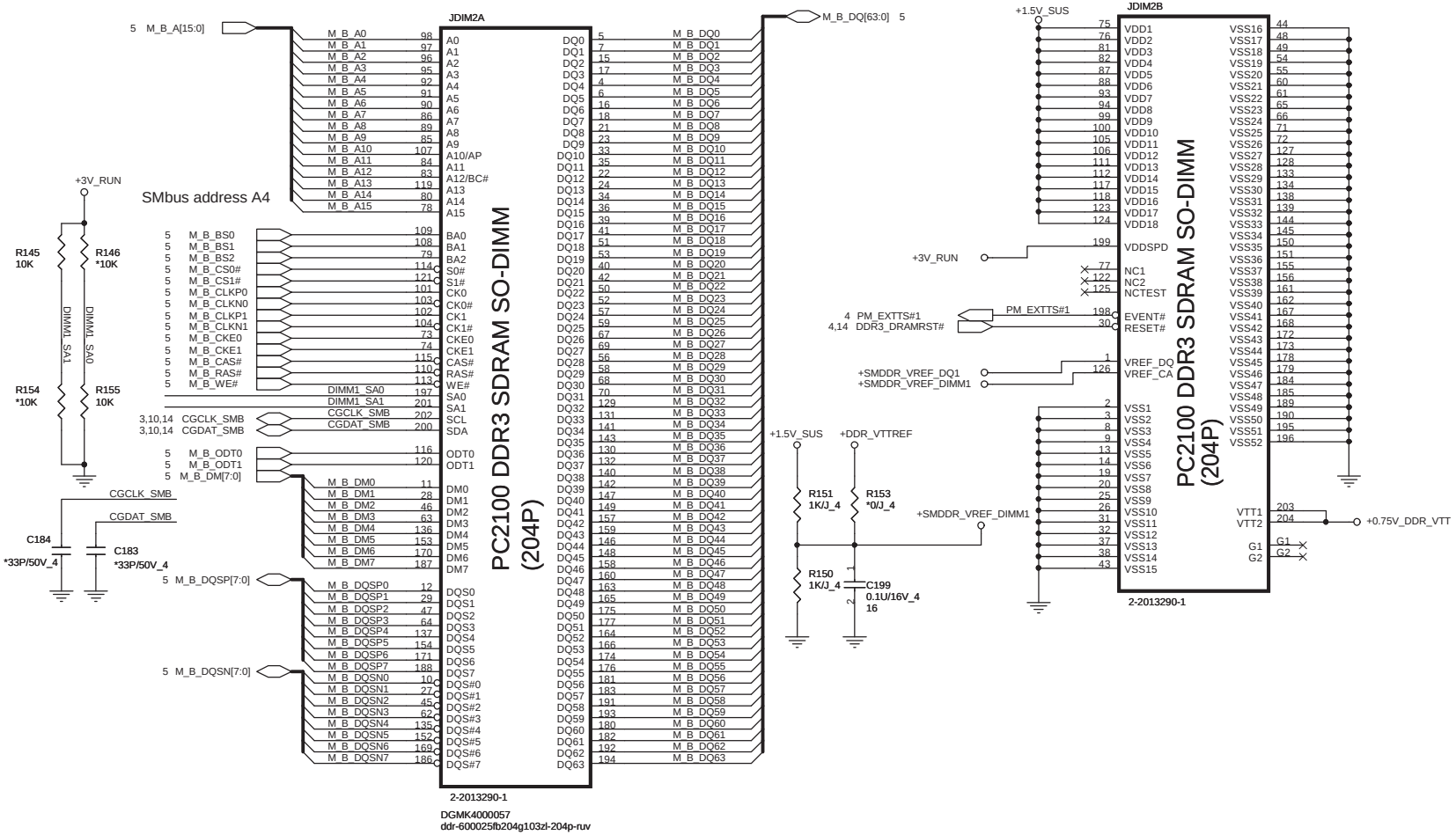
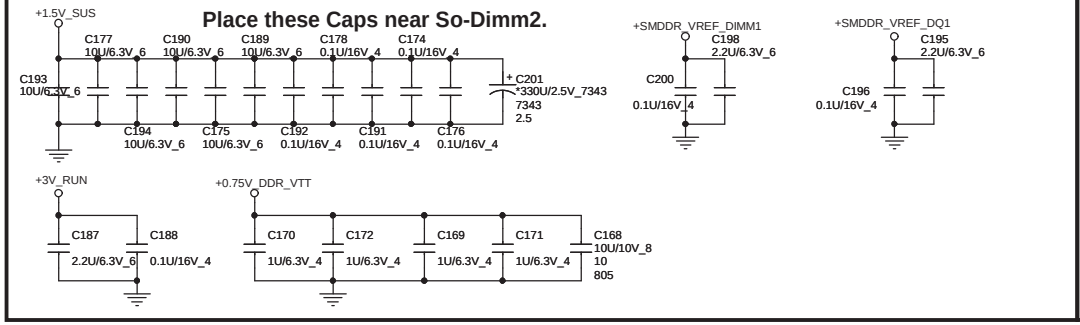
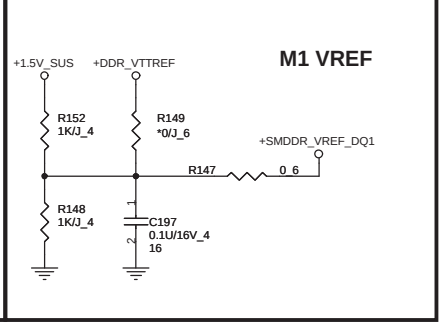


Place these Caps near So-Dimm2.



M1 VREF



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	DDR3 DIMM-2	1A
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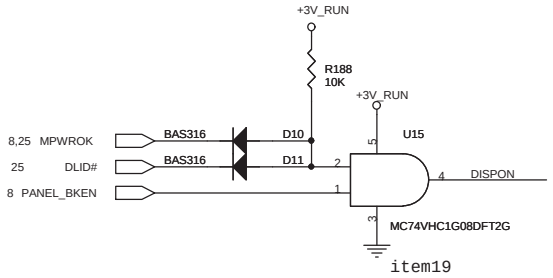
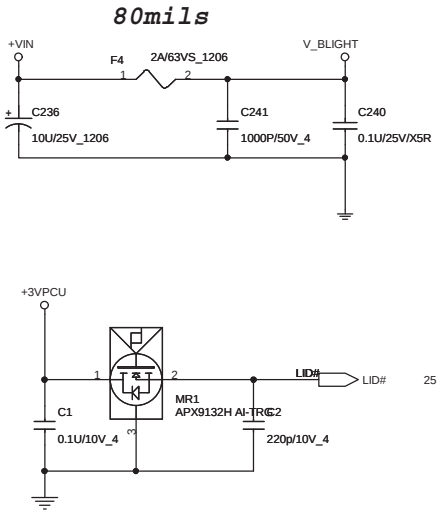
Backlight Control(LDS)

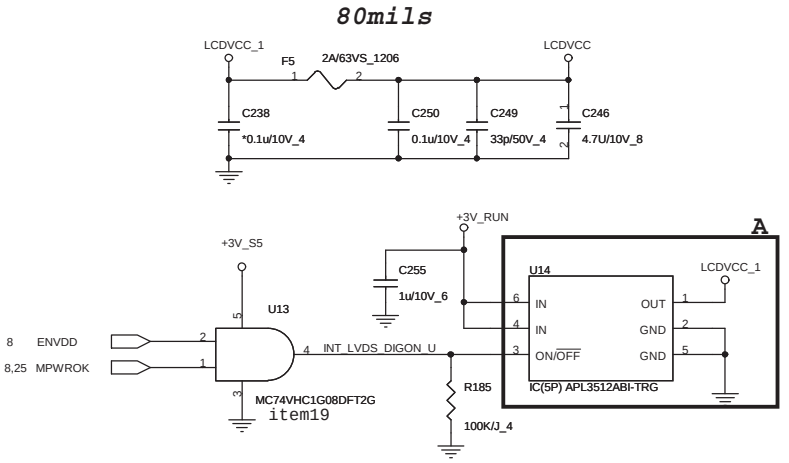


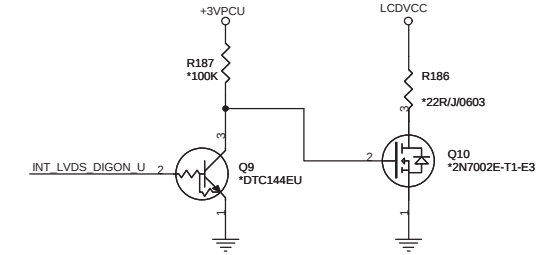
BACKLIGHT POWER



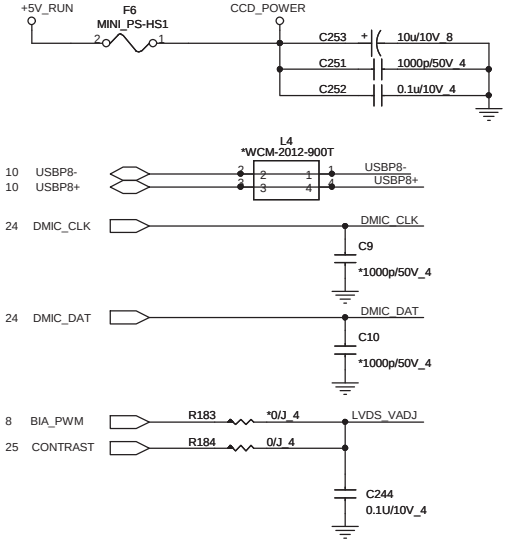
LED Panel POWER SWITCH(LVDS)

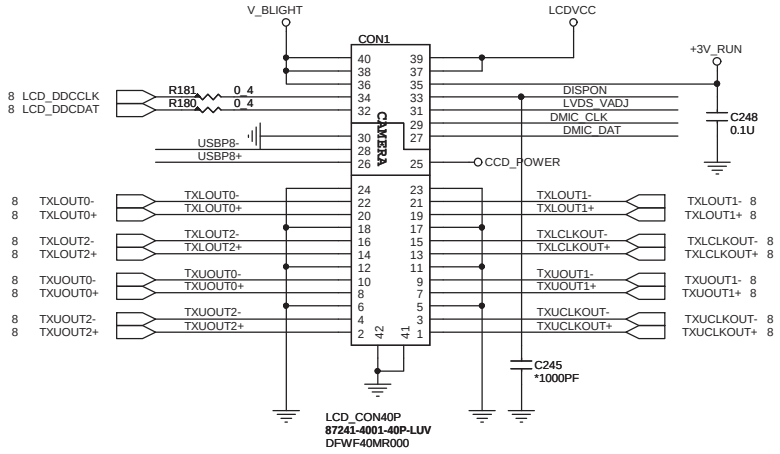
16

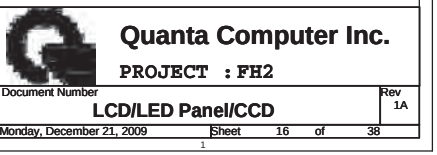




LVDS/CCD



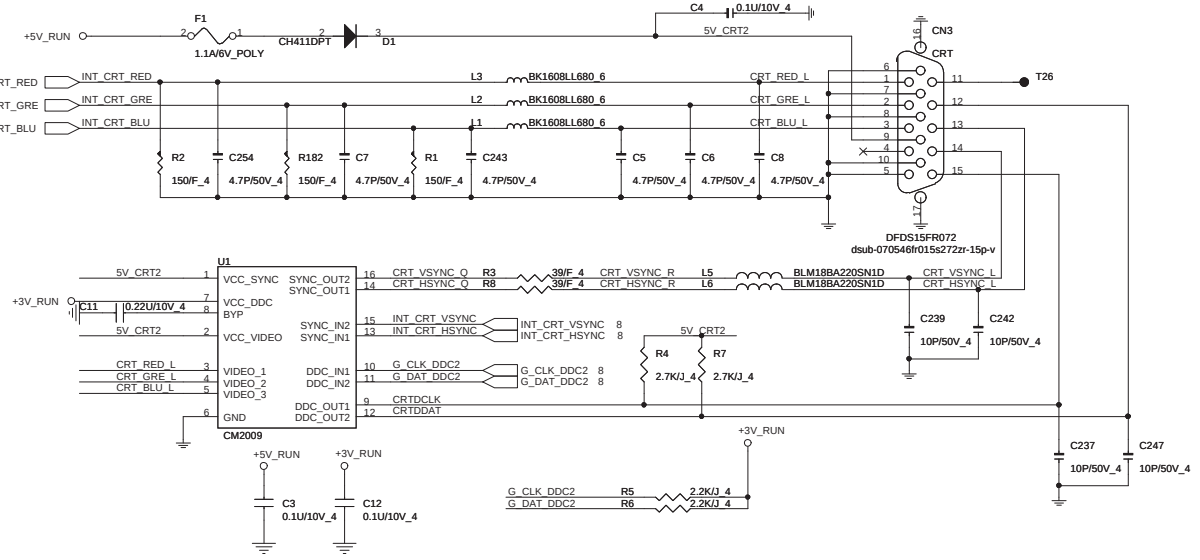


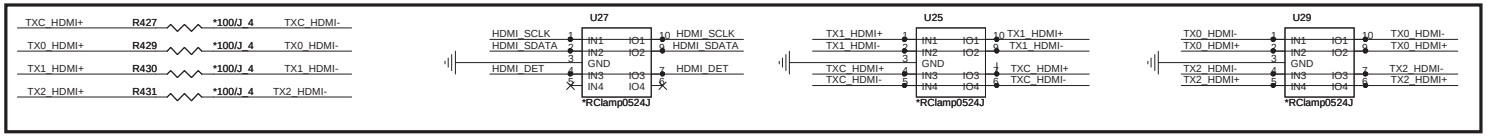


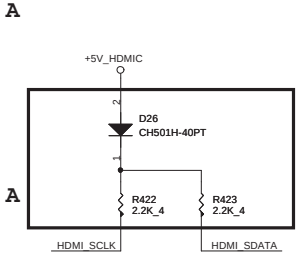
CRT CONN/DDC LEVEL SHIFT

40mils

TBD CN5500 FOOTPRINT



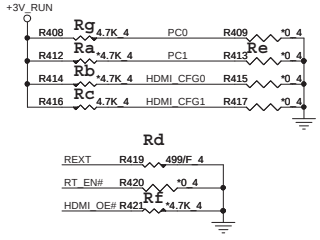


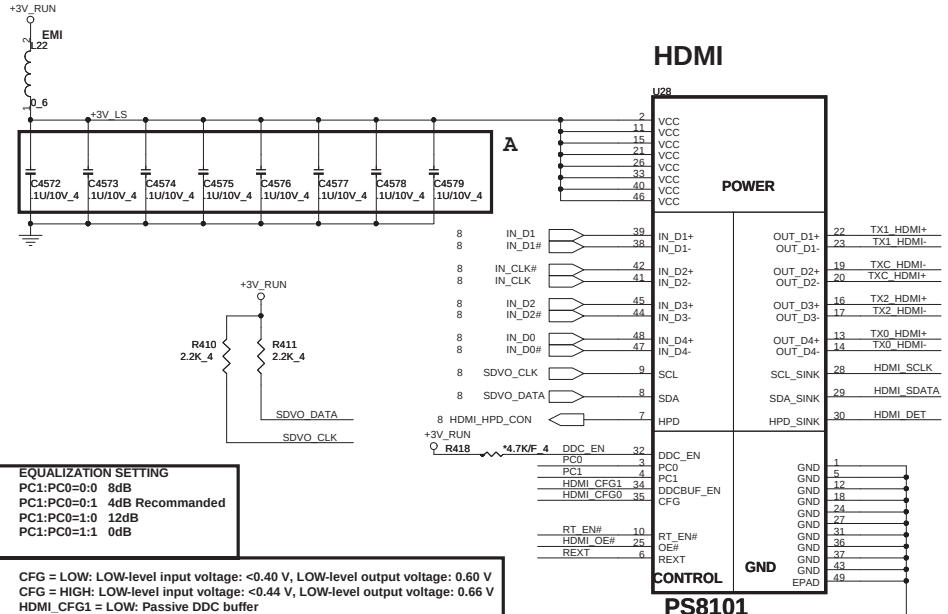


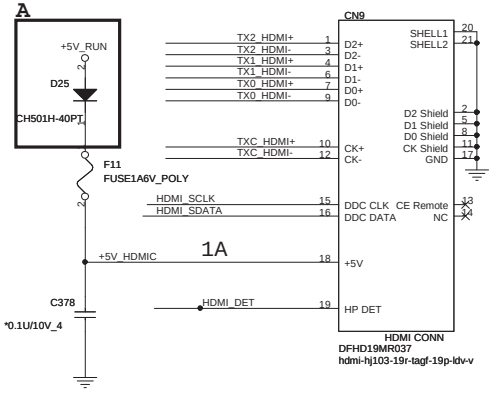
reserve for EMI

Signals		PDT	CHR	PIM
PC1	Ra	NC	4.7K	NC
HDMI_CFG0	Rb	NC	NC	NC
HDMI_CFG1	Rc	4.7K	NC	NC
REXT	Rd	499	1.2K	4.7K
PC1	Re	NC	NC	4.7K
HDMI_OE#	Rf	NC	4.7K	NC
PC0	Rg	4.7K	4.7K	4.7K

Vendor:PDT P/N:AL008101000
Vendor:CHR P/N:AL007318001
Vendor:PIM P/N:ALP411LS004







EQUALIZATION SETTING
PC1:PC0=0:0 8dB
PC1:PC0=0:1 4dB Recommanded
PC1:PC0=1:0 12dB
PC1:PC0=1:1 0dB

CFG = LOW: LOW-level input voltage: <0.40 V, LOW-level output voltage: 0.60 V
CFG = HIGH: LOW-level input voltage: <0.44 V, LOW-level output voltage: 0.66 V
HDMI_CFG1 = LOW: Passive DDC buffer
HDMI_CFG1 = HIGH: Active DDC buffer

Quanta Computer Inc.
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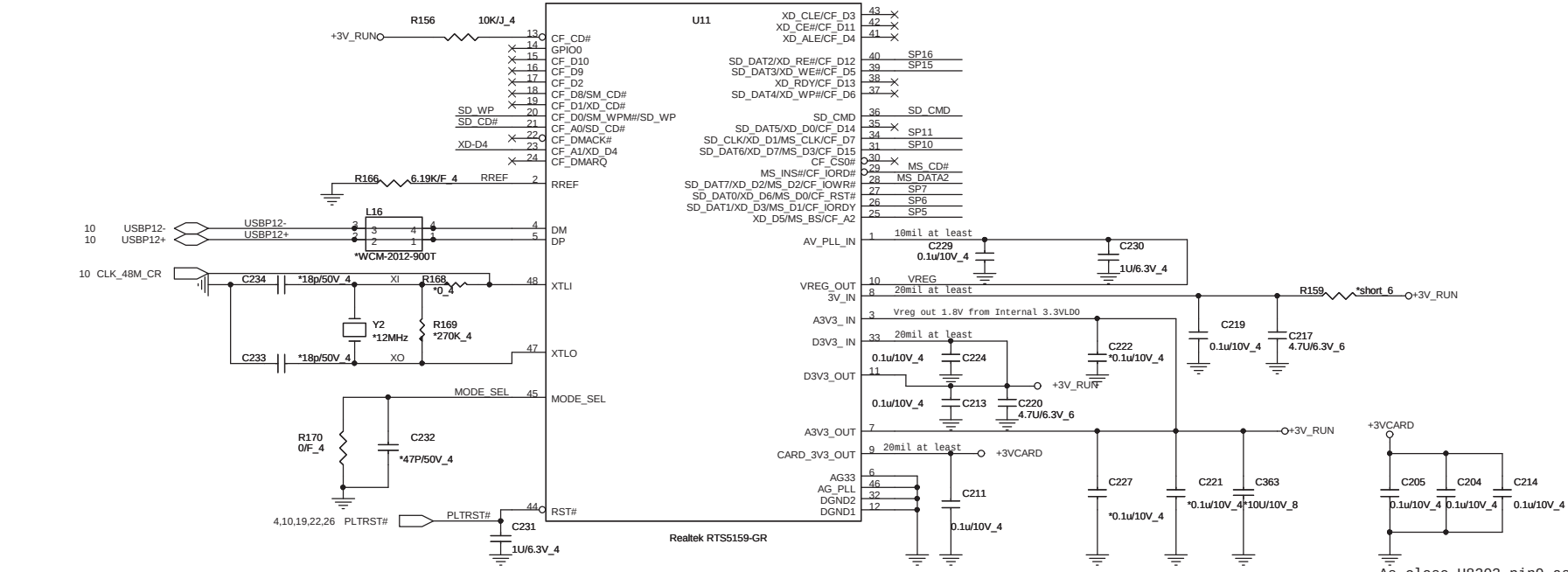
Card Reader



As close U8203 pin9 as possible

XD-D4 R158 short_4 SD_DAT1

For 5158E

SP7 R162 short_4 MS_DATA0_SD_DAT0

SP6 R161 short_4 MS_DATA1

SP16 R171 short_4 SD_DAT2

SP5 R160 short_4 MS_BS

SP15 R167 short_4 SD_DAT3

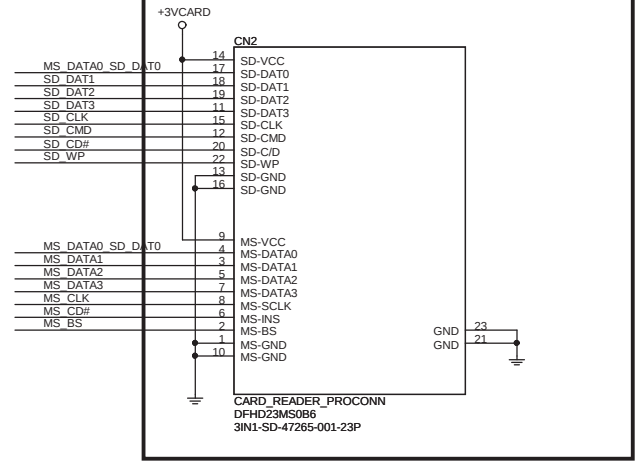
R164 short_4 SD_CLK

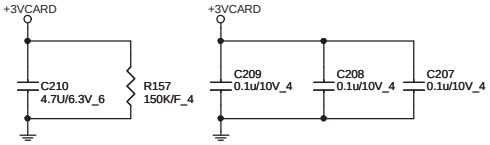
SP11 R165 short_4 MS_CLK

C226 *22P

SP10 R163 short_4 MS_DATA3

A





Quanta Computer Inc.

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Size	Document Number	Rev
	Card Reader RTS5159	1A
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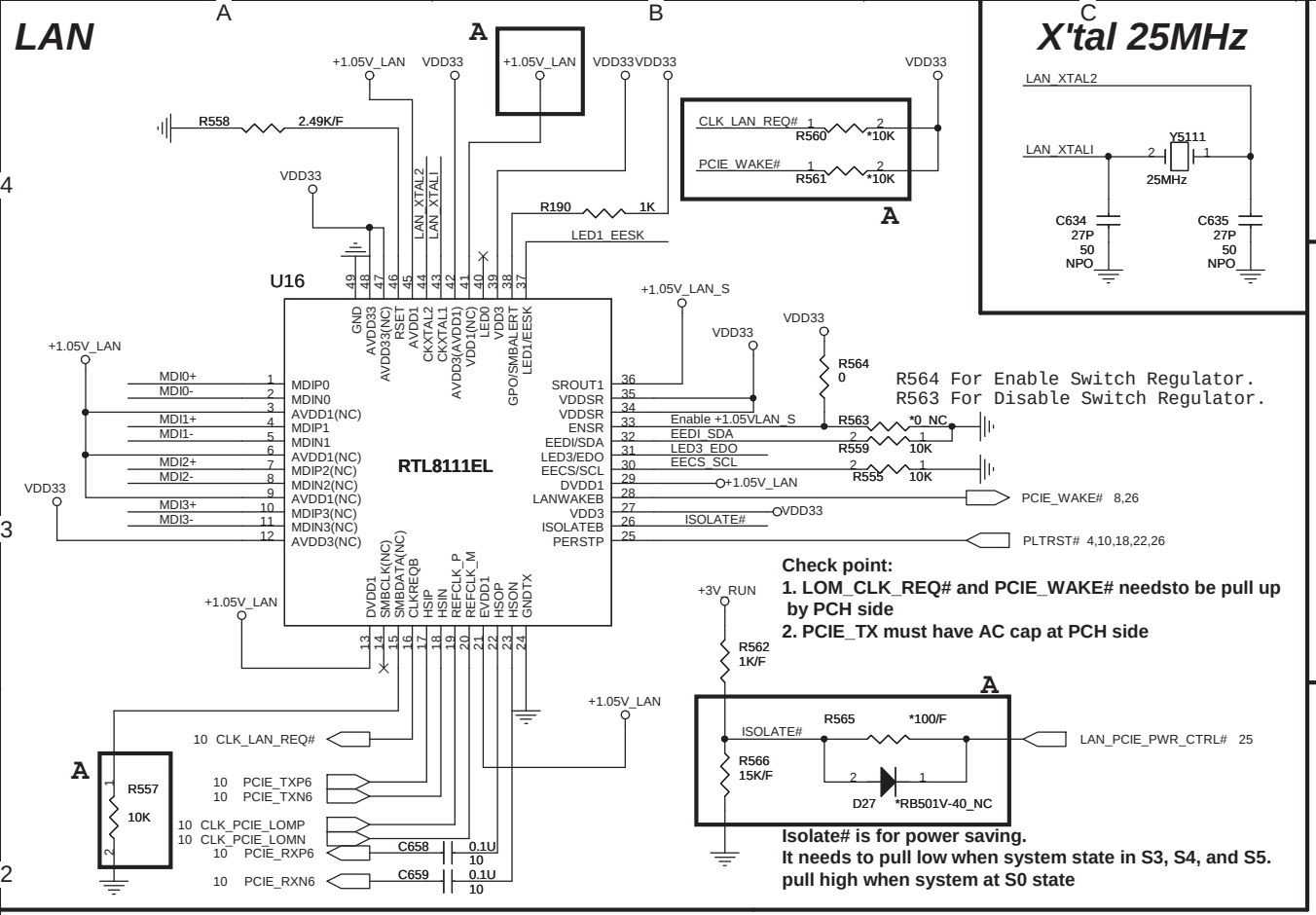
LAN



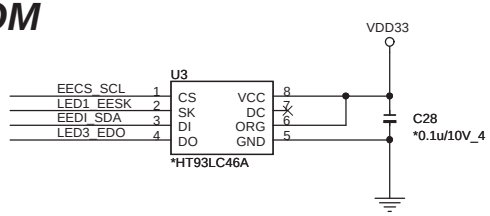
Check point:
1. LOM_CLK_REQ# and PCIE_WAKE# needsto be pull up by PCH side
2. PCIE_TX must have AC cap at PCH side

R564 For Enable Switch Regulator.
R563 For Disable Switch Regulator.

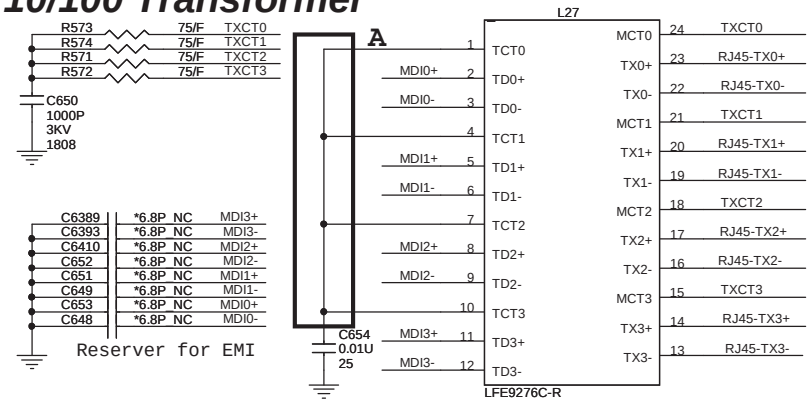
Isolate# is for power saving.
It needs to pull low when system state in S3, S4, and S5.
pull high when system at S0 state

X'tal 25MHz

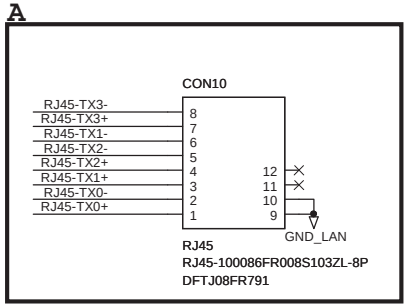
LAN EEPROM

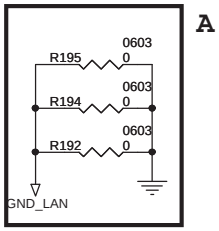


10/100 Transformer

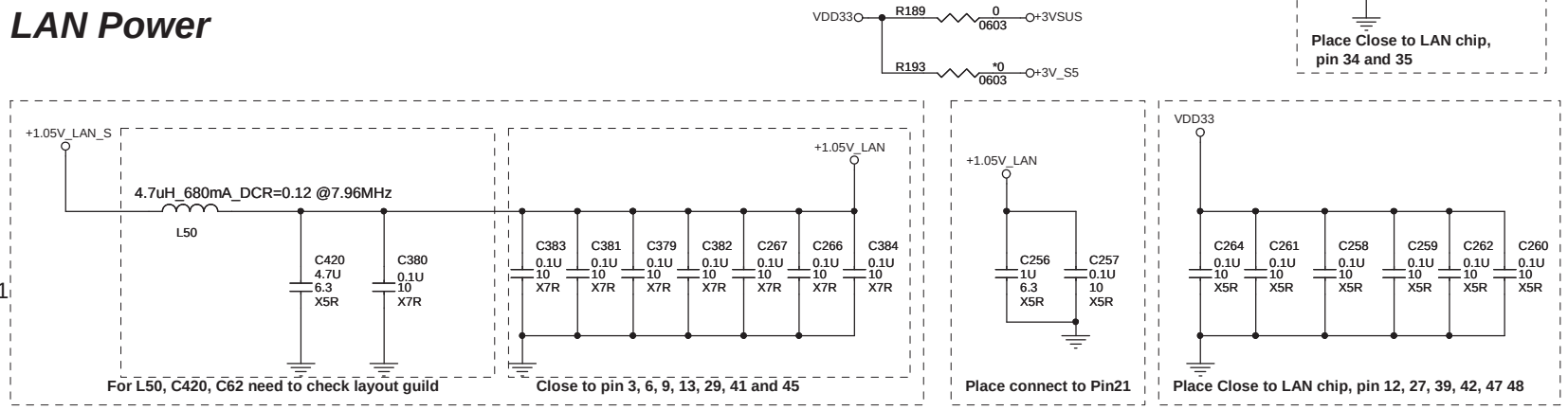


RJ45





LAN Power



For L50, C420, C62 need to check layout guild

Close to pin 3, 6, 9, 13, 29, 41 and 45

Place connect to Pin21

Place Close to LAN chip, pin 12, 27, 39, 42, 47 48

Place Close to LAN chip, pin 34 and 35

REQ by layout

Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: LAN_RTL8111E-GR/RJ45	Rev: 1A
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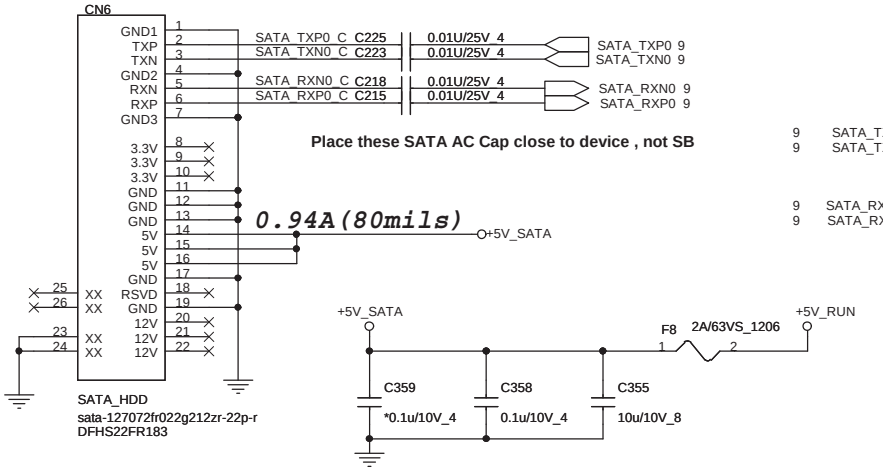
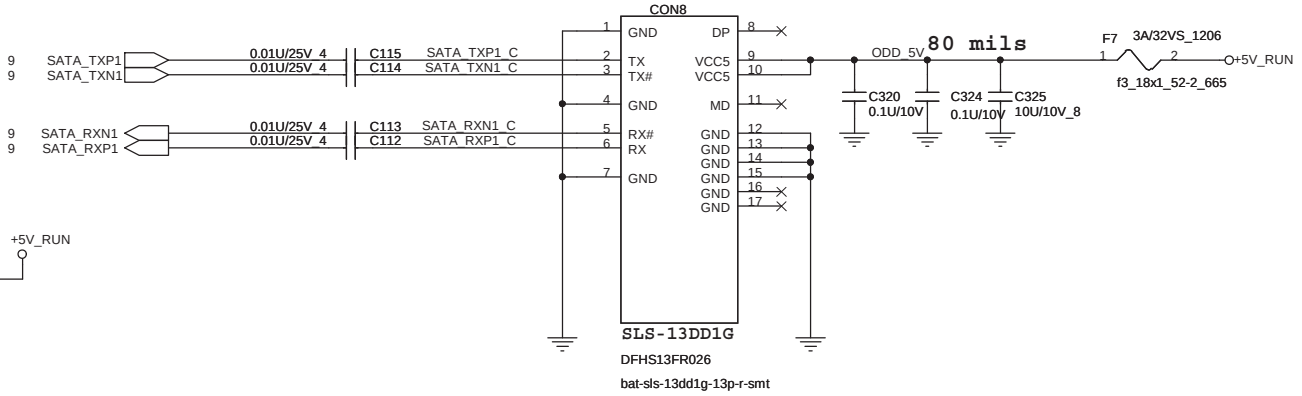
2.5" SATA HDD



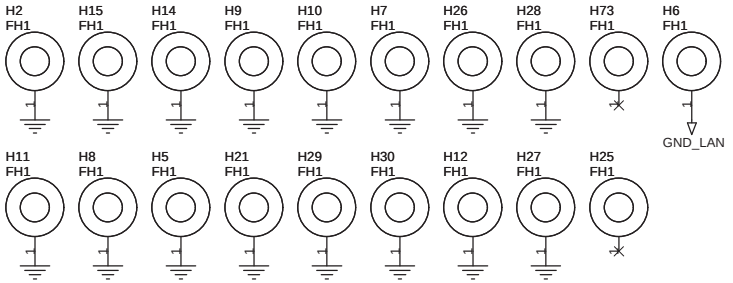
SATA ODD

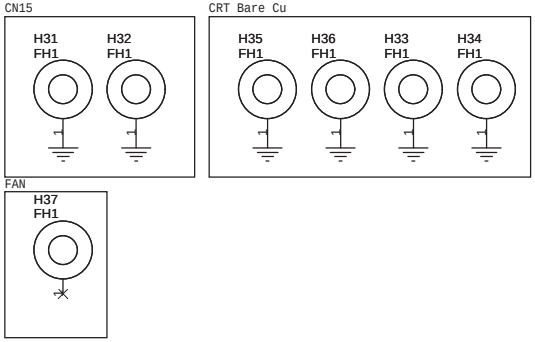
ODD CONN



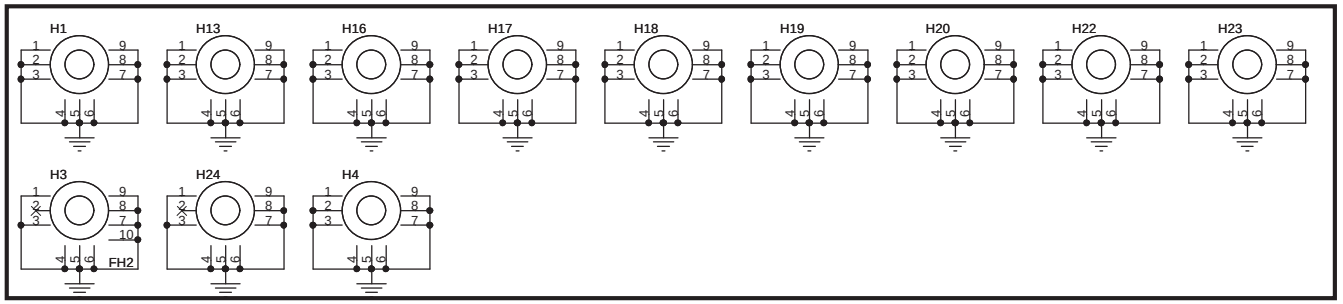
20

Hole

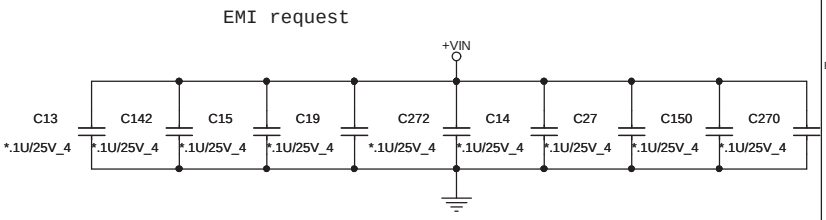




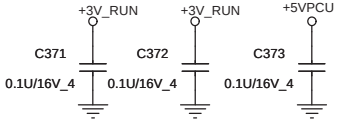
ESD



Decoupling Cap



EMI(Decoupling Cap)



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	HDD/ ODD/HOLE	1A
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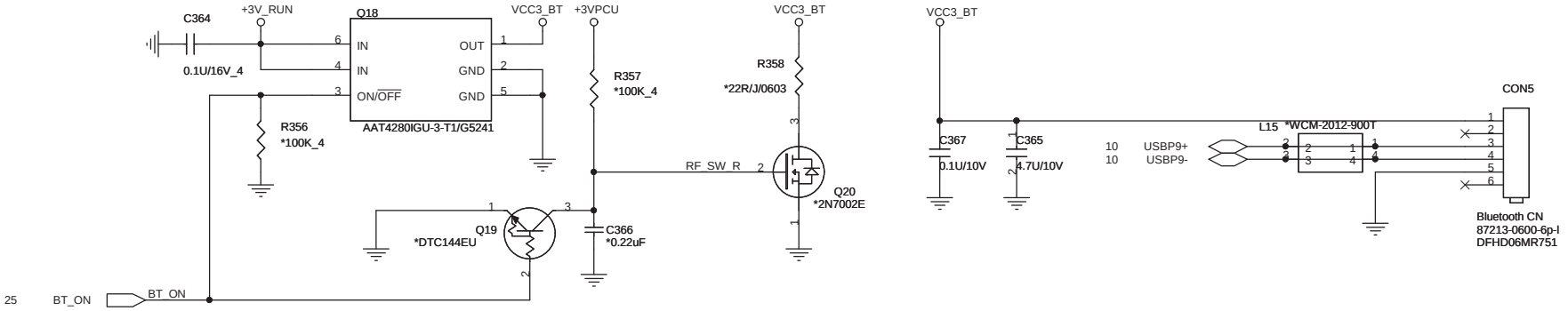
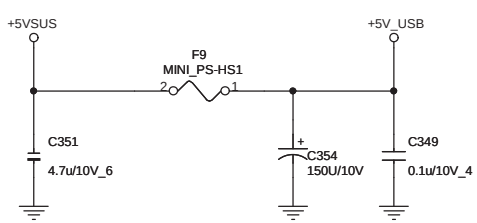
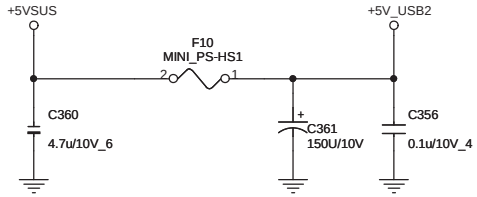
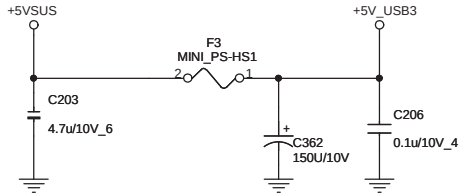
BuleTooth (BTM)

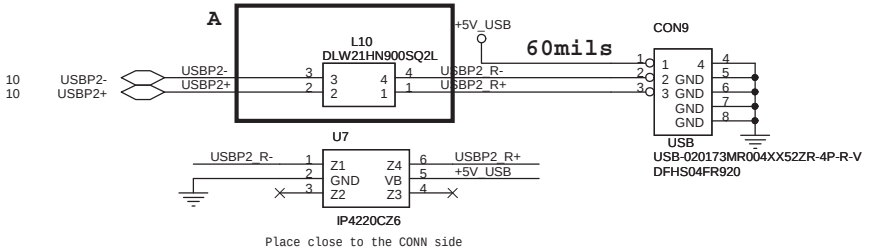


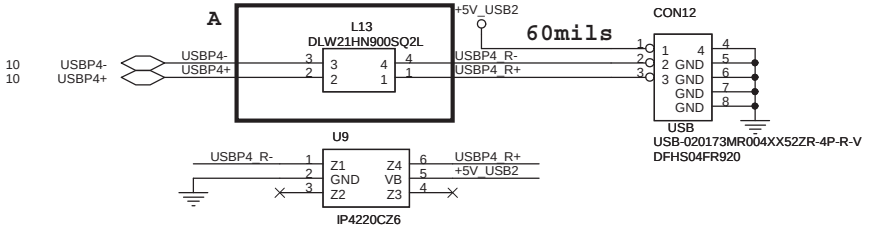
USB Connector

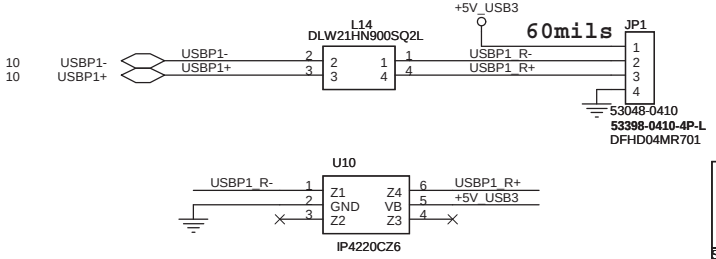












Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	USB/BLUE TOOTH	1A
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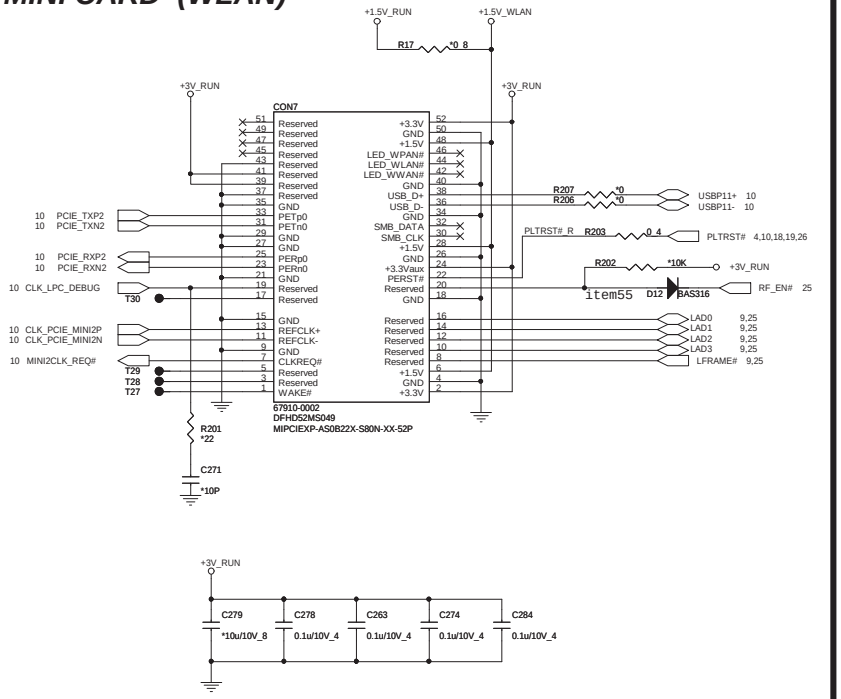
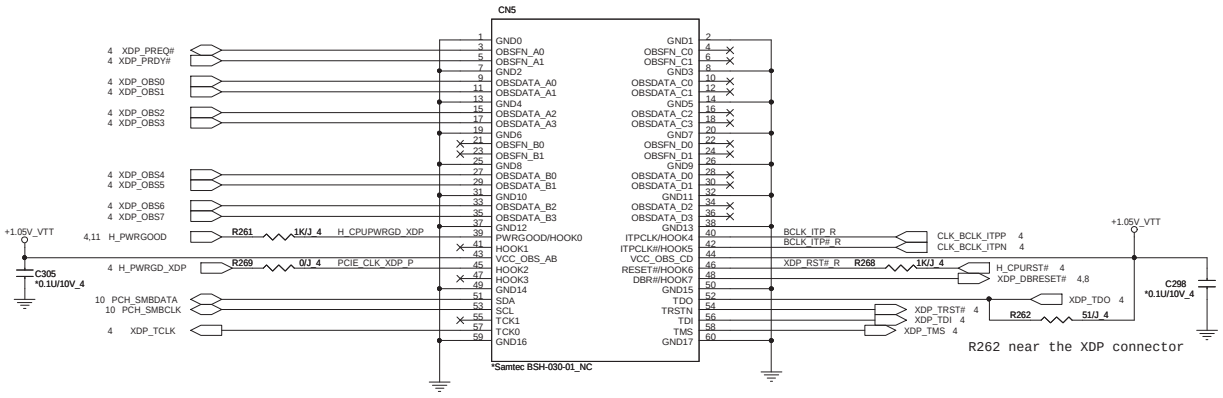
MINI CARD (WLAN)

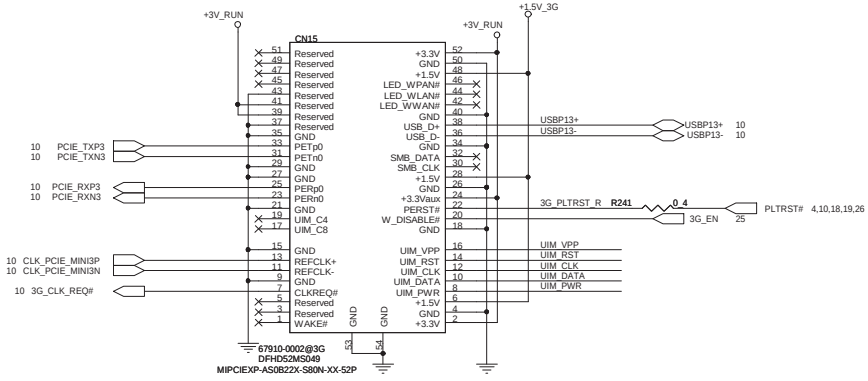


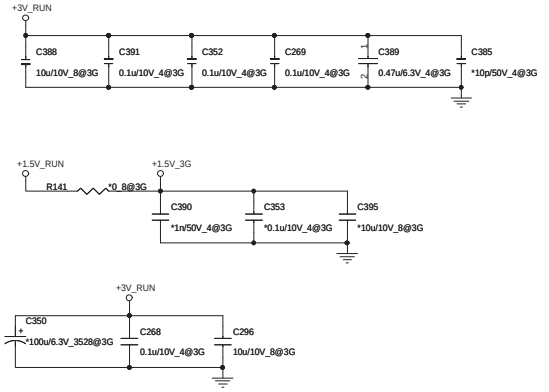
XDP

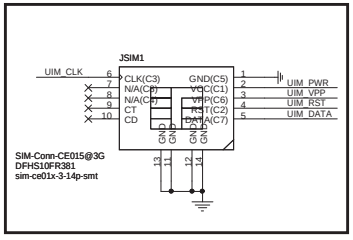


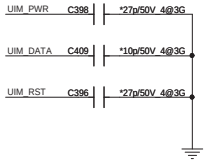
It is for debug. requesst vendeer provide 200 pcs sample.

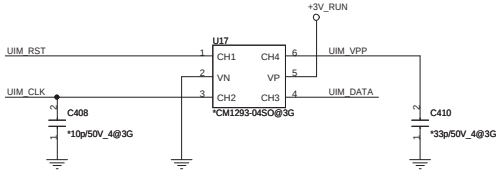
Mini Card2-3G(MNC)

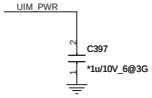












A

Quanta Computer Inc.		
PROJECT : FH2		
Size	Document Number: MINI CARD(WLAN/3G)/XDP	Rev 1A
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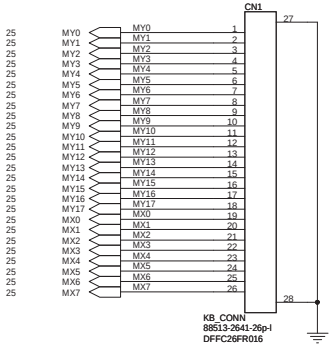
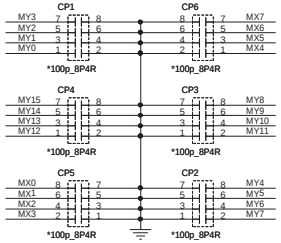
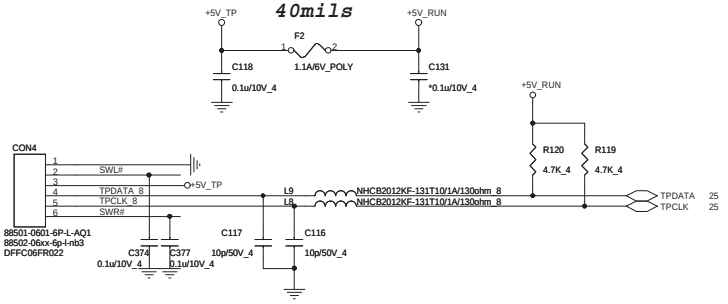
Keyboard(KBC)

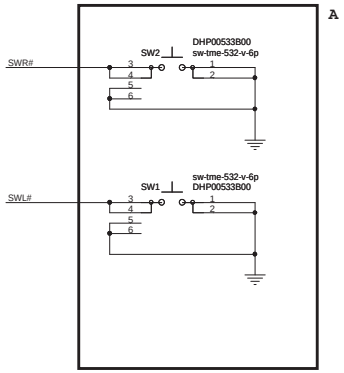


For EMI Reserve Caps for debug

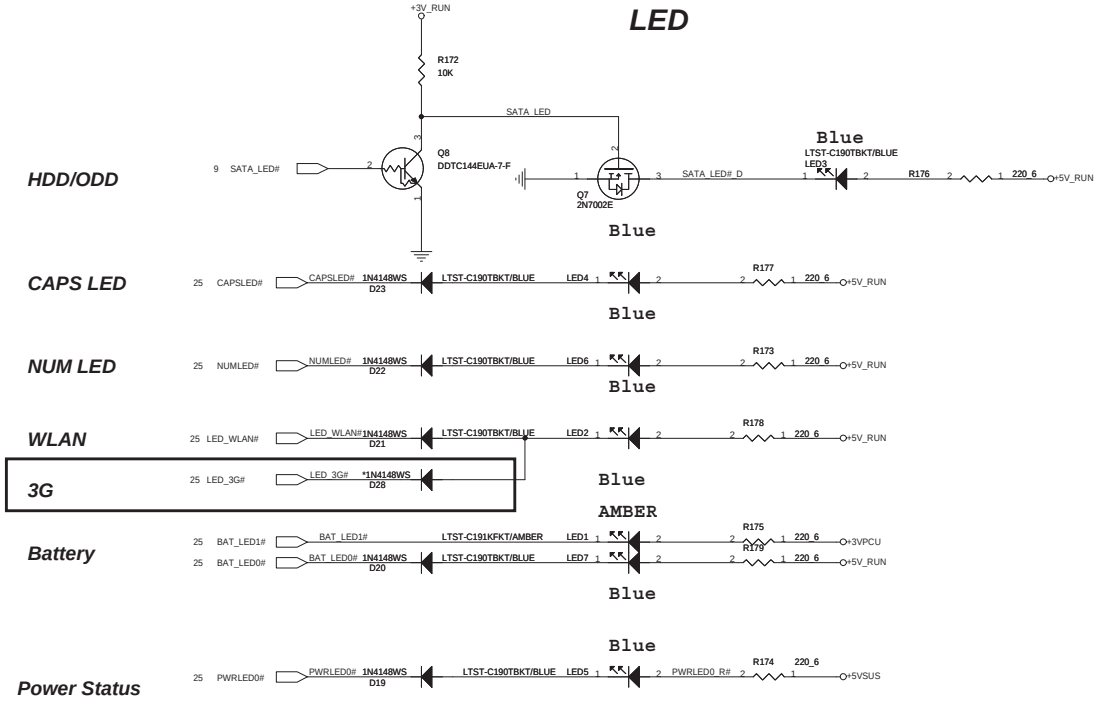


Touch Pad





LED



Quanta Computer Inc.
PROJECT : FH2
Size
Document Number
KB/TOUCH PAD/LED
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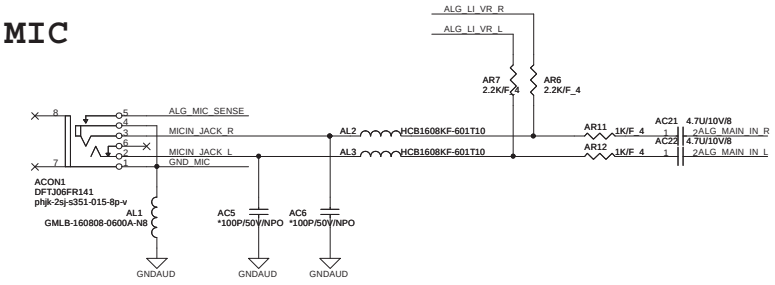
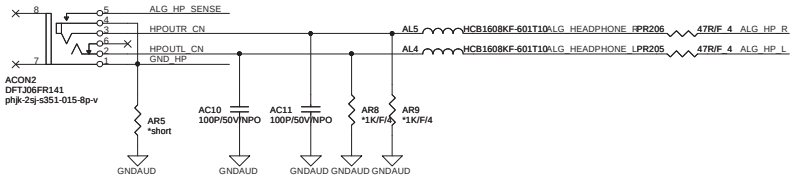
Codec ALC269

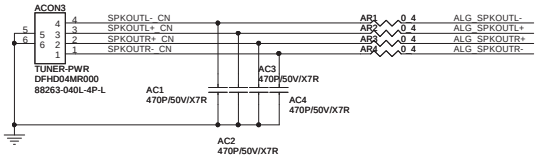
MIC



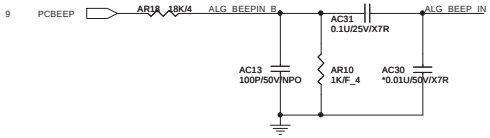
HP



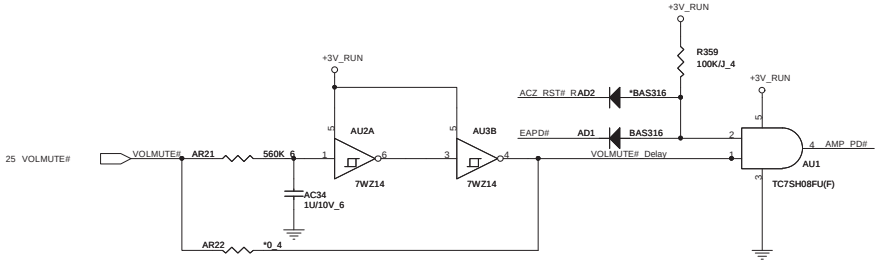
SPKR



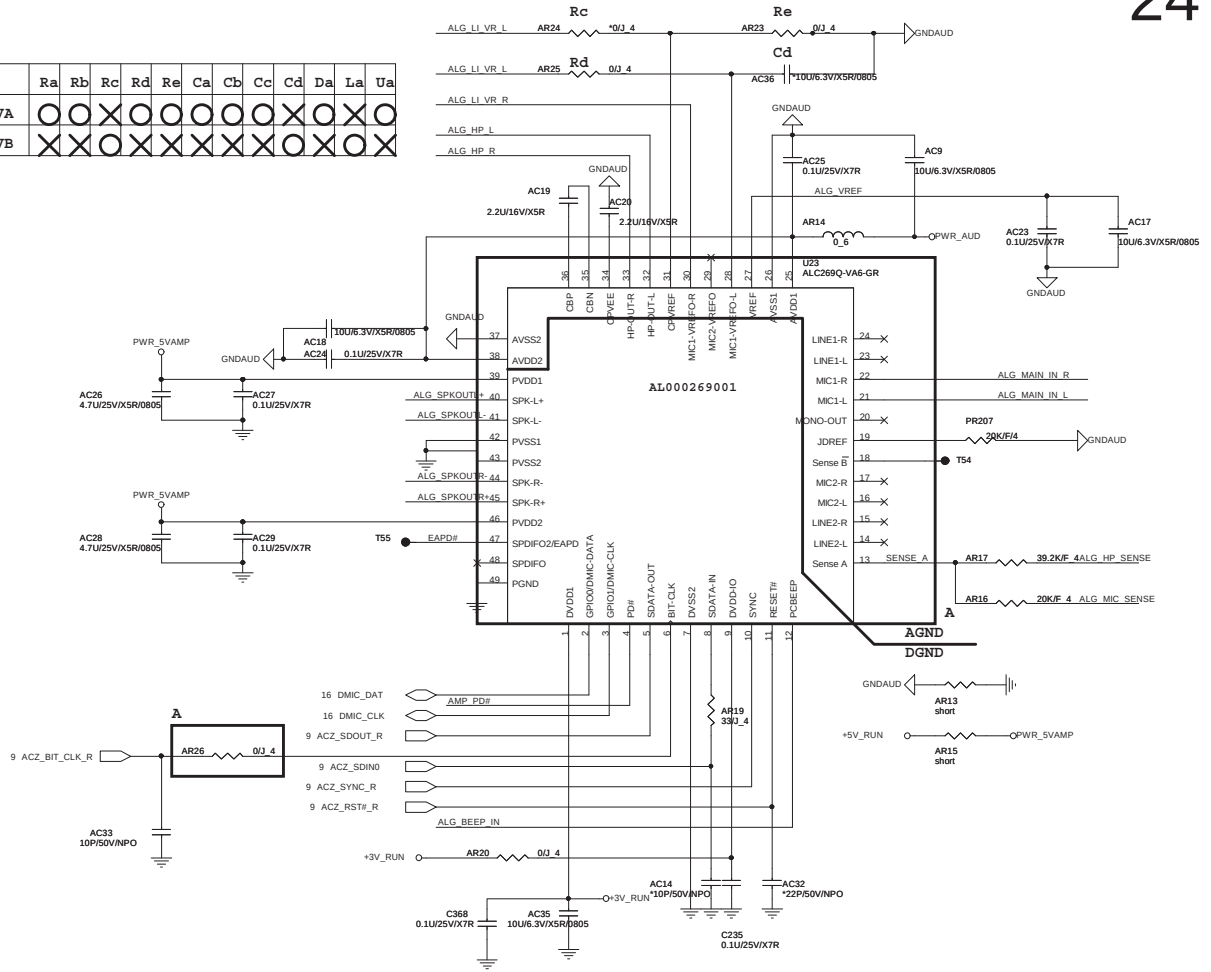
BEEP

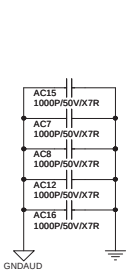


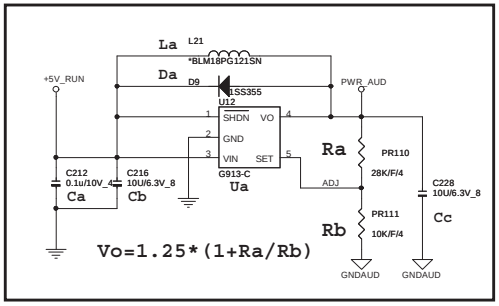
VOLMUTE



U23	Ra	Rb	Rc	Rd	Re	Ca	Cb	Cc	Cd	Da	La	Ua
ALC269Q-VA	O	O	X	O	O	O	O	O	X	O	X	O
ALC269Q-VB	X	X	O	X	X	X	X	X	O	X	O	X







Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	CODEC (ALC269)	1A
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EC(KBC)

IT8502

Layout Note:
Place all capacitors close to IT8502.

Layout Note:
net "3VPCU" and "RTC_VCC" minimum trace width 12mils.

Note 1 : Since all GPIO belong to VSTBY power domain, and there are some special considerations below:
(1) If it is output to external VCC derived power domain circuit, this signal should be isolated by a diode such as KBRST# and GA20.
(2) If it is input from external VCC derived power domain circuit, this external circuit must consider not to float the GPIO input.

Note 2 :
(1) Each input pin should be driven or pulled.
(2) Each output-drain output pin should be pulled.

Layout Note:
32.768kHz clock lines:
a. If possible, please avoid using any through-hole.
b. Please make the trace length short, and the trace width wide enough.
c. The spacing to the closest neighbor should be wide enough.

BIOS Write Protect

Near ROOM DOOR

PCB REV	MODEL_ID0	MODEL_ID1
C	LOW	LOW
D	HIGH	LOW
E	LOW	HIGH
F	HIGH	HIGH

Quanta Computer Inc.
PROJECT : FH2

Size	Document Number	Rev
	EC_ITE8502	1A

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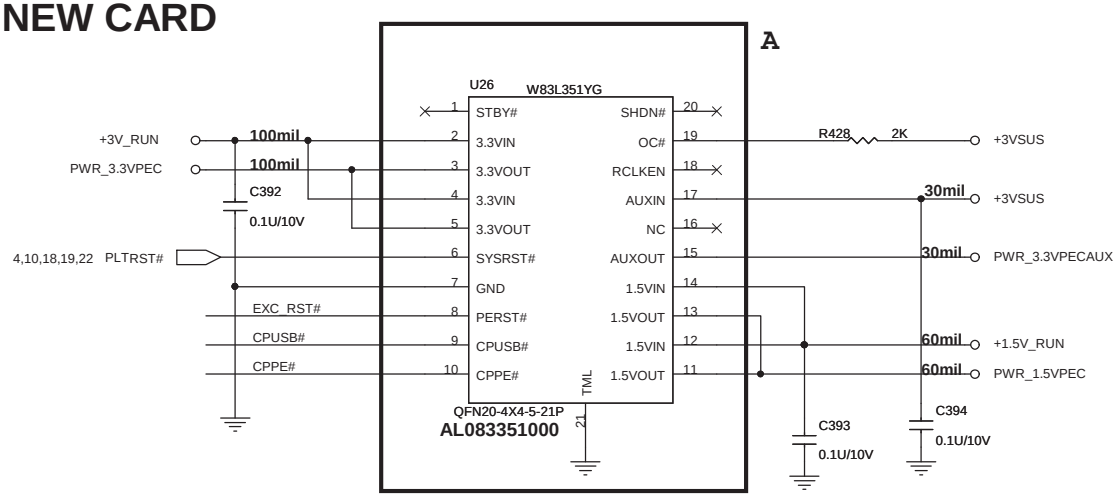
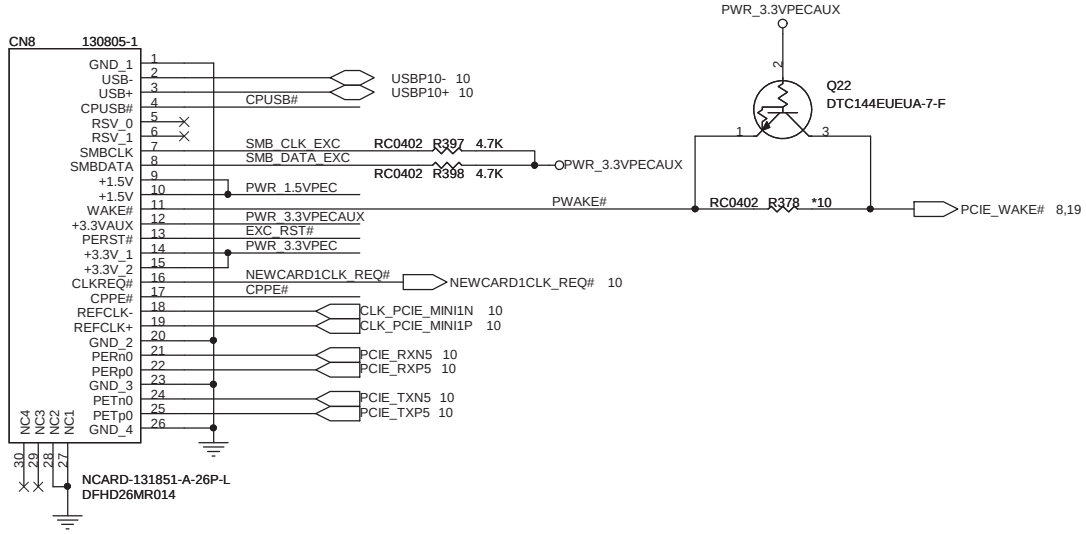
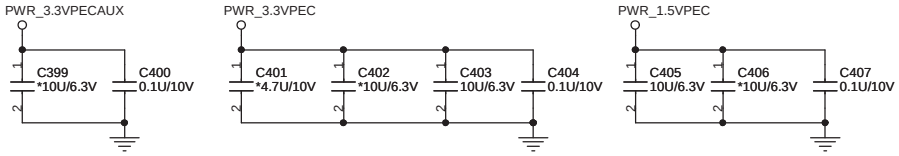
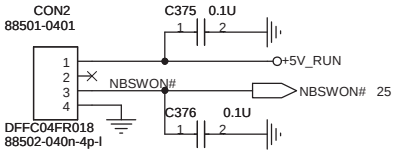
NEW CARD



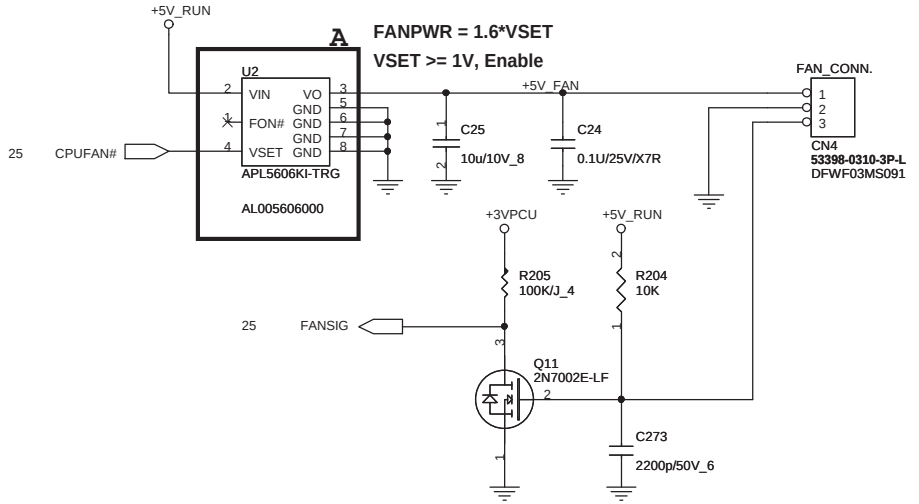




SW BOARD CON



CPU FAN CTRL



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	FAN/SW/NEWCARD	1A
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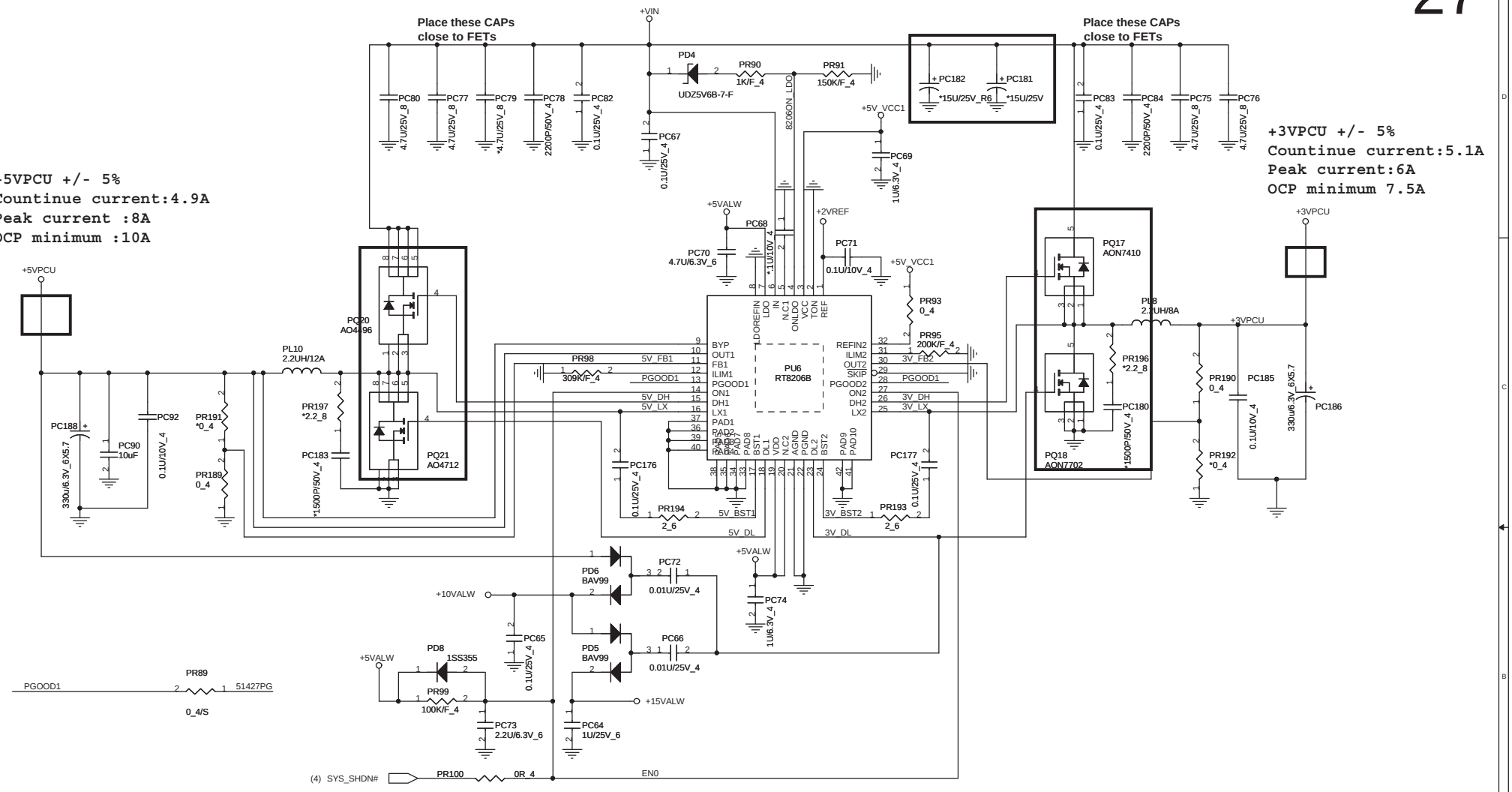
DC/DC +3V_ALW/+5V_ALW/+5V_ALW2 /+15V_ALW

+5VPCU +/- 5%
Countinue current:4.9A
Peak current :8A
OCP minimum :10A

+3VPCU +/- 5%
Countinue current:5.1A
Peak current:6A
OCP minimum 7.5A



Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	+5V/+3V (RT8206B)	1A
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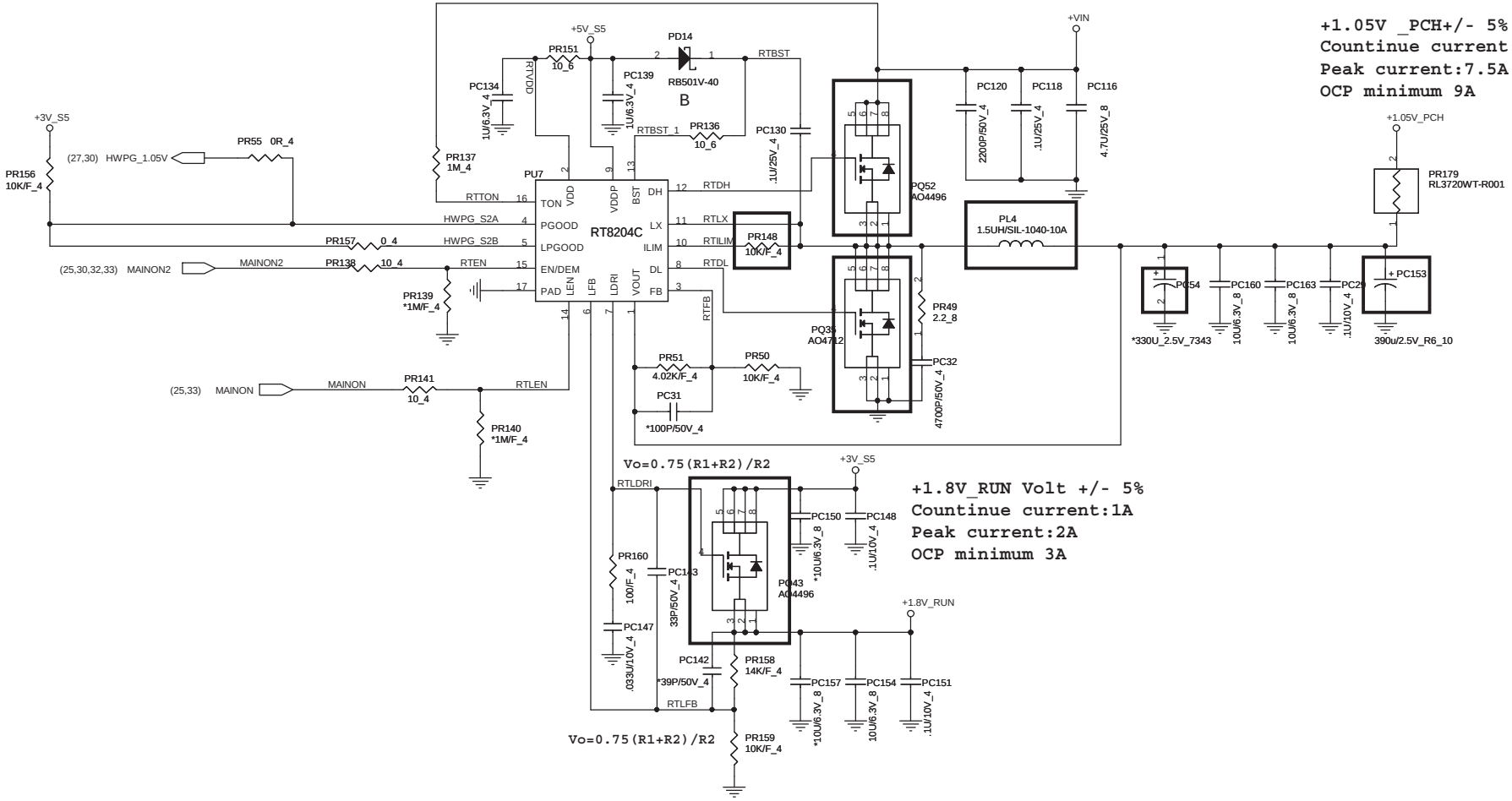

Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	+1.05V/+1.8V (RT8204C)		1A
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OSRSEL = GND	110mV
OSRSEL = REF	145\mV
OSRSEL = 3.3V	190\mV
OSRSEL = 5V	OFF

Countinue current:48A

PU4
TPS51621RHAR_QFN40_6X6

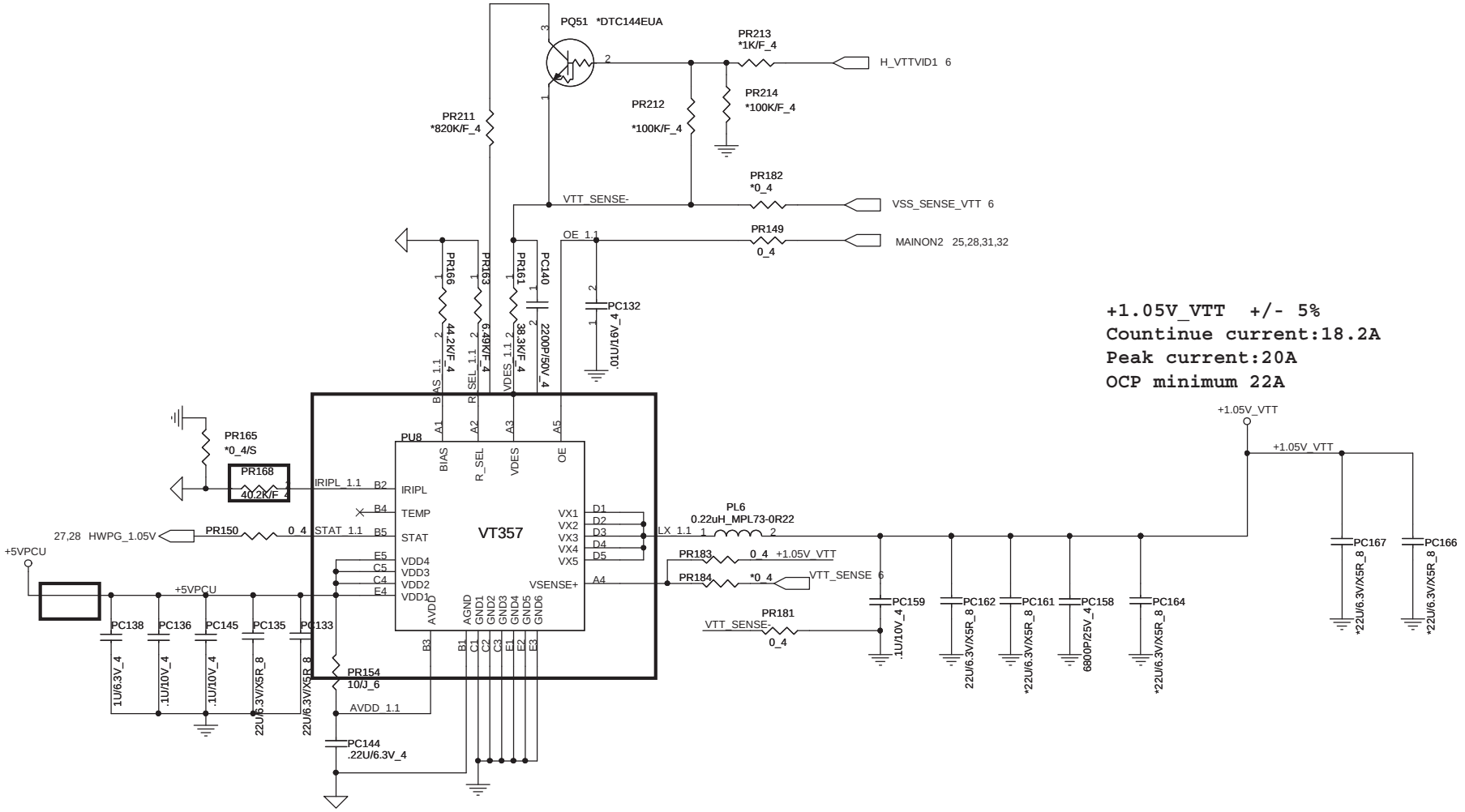
PL3
0.36UH PCMC104T-R36MN 30A

PL7
0.36UH PCMC104T-R36MN 30A

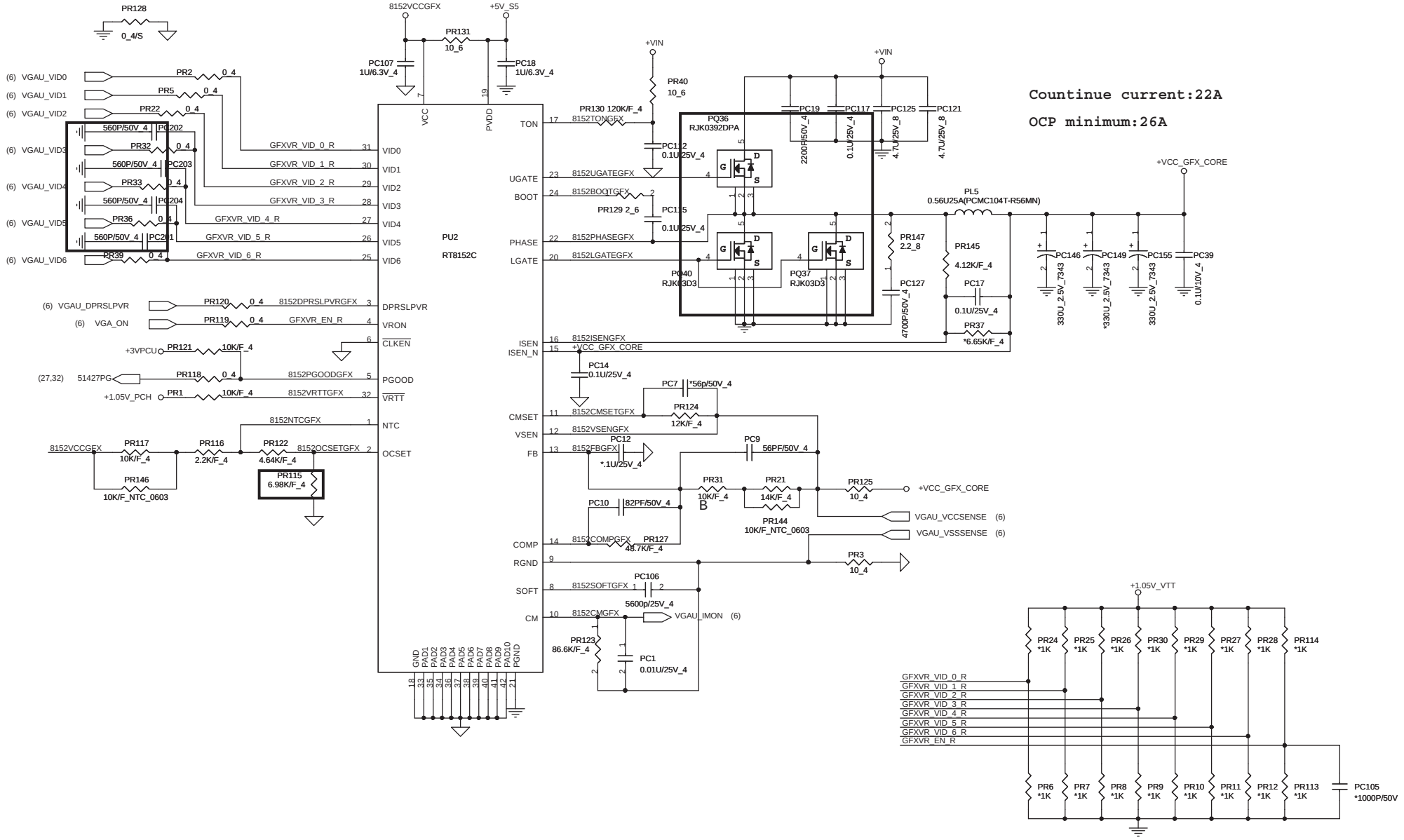
VID
VID5=1 VID4=0 VID3=0

Quanta Computer Inc.
PROJECT : FH1

Size	Document Number	Rev
	CPU Core (TPS51621)	1A
Date: Monday, December 21, 2009	Sheet 29 of 39	



Quanta Computer Inc.		
PROJECT : FH1A		
Size	Document Number: +1.05V_VTT (VT358)	Rev 1A
Date: Monday, December 21, 2009	Sheet 30 of 45	



Quanta Computer Inc.			
PROJECT : FH1			
Size	Document Number		Rev
	UMA GPU CORE (RT8152C)		1A
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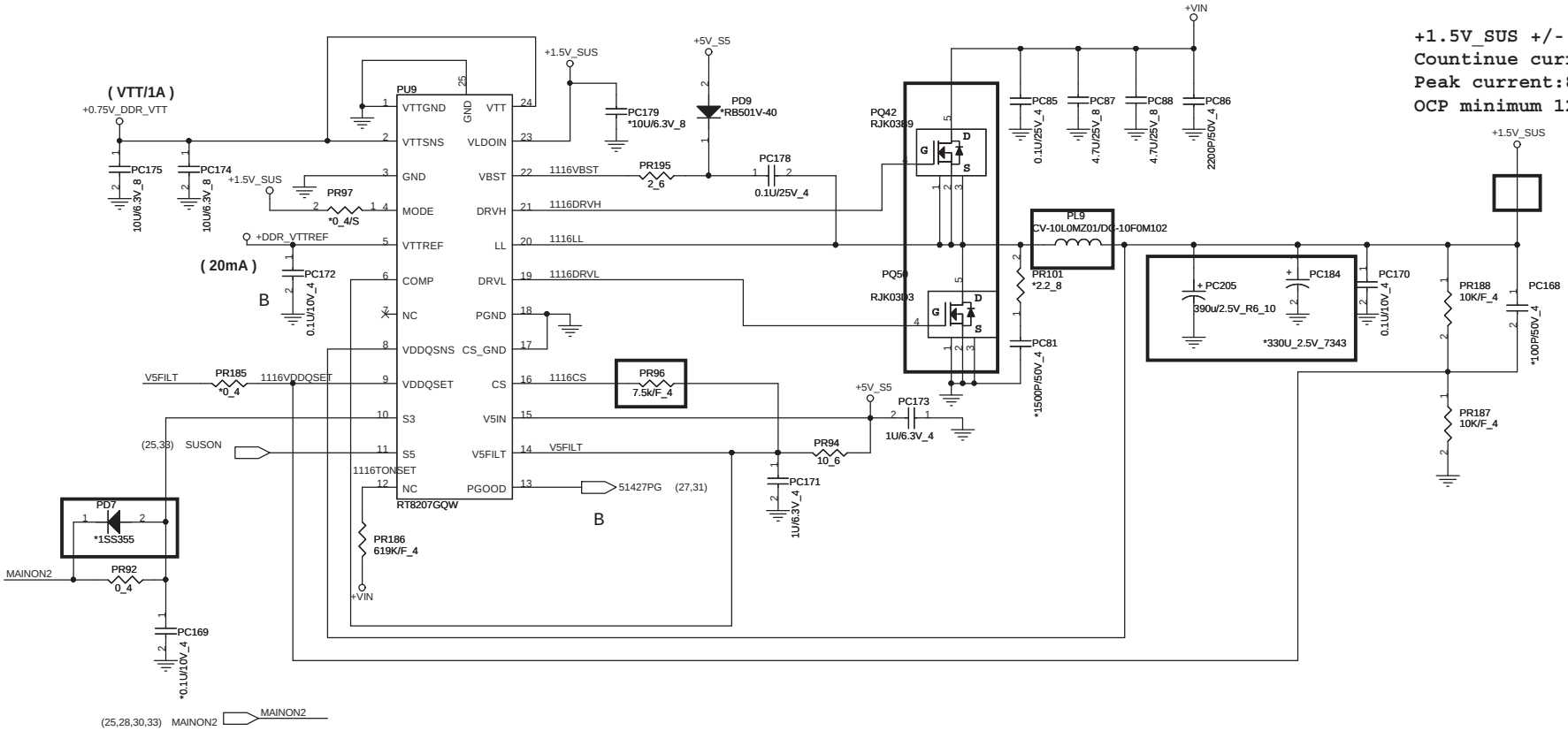
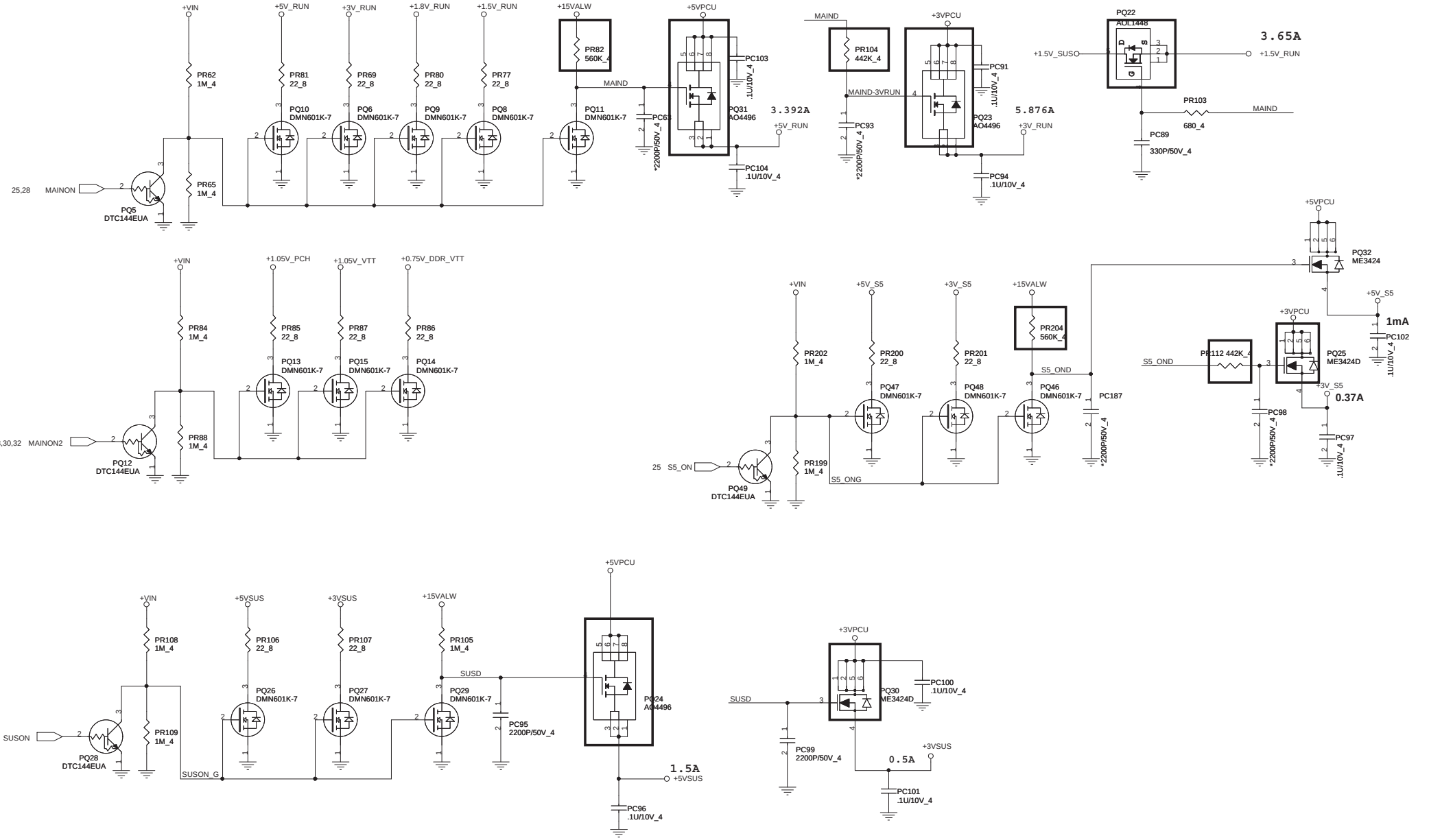


+1.5V_SUS +/- 5%
Countinue current:4A
Peak current:8A
OCP minimum 12A

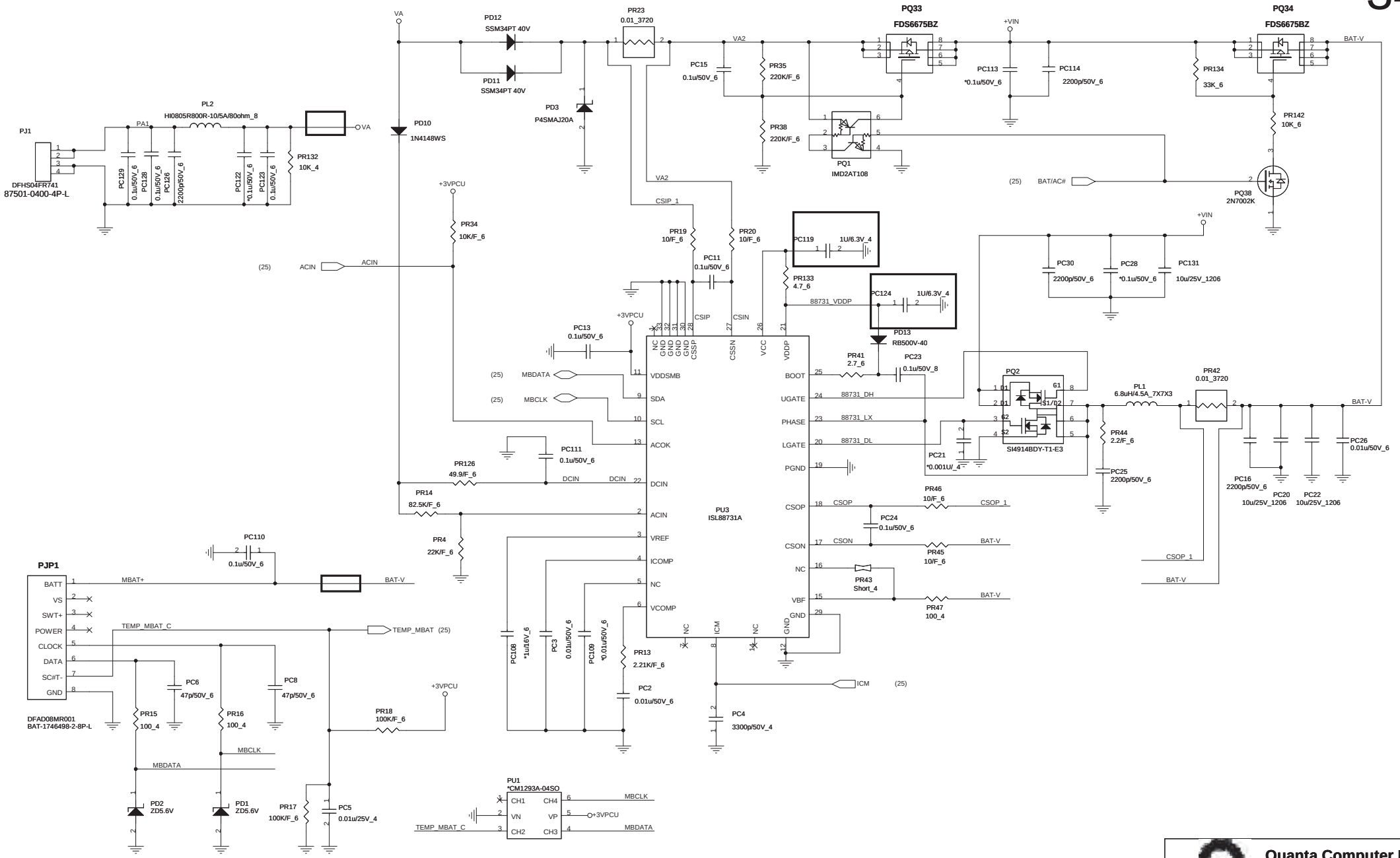
Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: DDR3 (RT8207)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 32 of 39	



Quanta Computer Inc.

PROJECT : FH2

Size	Document Number	Rev
	DISCHARGE/3VS5/5VS5/LAN	1A
Date: Monday, December 21, 2009	Sheet 33 of 38	



Quanta Computer Inc.		
PROJECT : FH1		
Size	Document Number: CHARGER (ISL88731)	Rev: 1A
Date: Monday, December 21, 2009	Sheet 34 of 39	