Inventec Corporation
R&D Division

Board name : Mother Board Schematic

Project : J11Eagle (Santa Rosa)

Version : 0.4

Initial Date : January 05, 2007

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Title
J11Eagle(Merom+Crestline+ICH8M)

Size	Document Number	Rev
C	Title	0.4

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J11Eagle (Santa Rosa) Schematic Ver : 0.4

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47. BATTERY CN
48. 1.05V/ETC0
49. EC control
50. BAY TR /GP/Stick BOARD
51. USB BOARD
52. GLIDE SW BOARD W/FP
53. STICK SW BOARD
54. EMI/ESD
55. GLIDE SW BOARD W/O FP

2. PCI & IRQ & DMA Description :

IDSEL	CHIP
AD19	OZ711MP1

PCIINT	CHIP
PCI_INT#0	OZ711MP1
PCI_INT#1	N/A
PCI_INT#2	N/A
PCI_INT#3	N/A

BUSMASTER

REQ	CHIP
REQ0 / GNT0	N/A
REQ1 / GNT1	OZ711MP1
REQ2 / GNT2	N/A
REQ3 / GNT3	N/A

19. ICH8M CPU/IDE/SATA(1/4)

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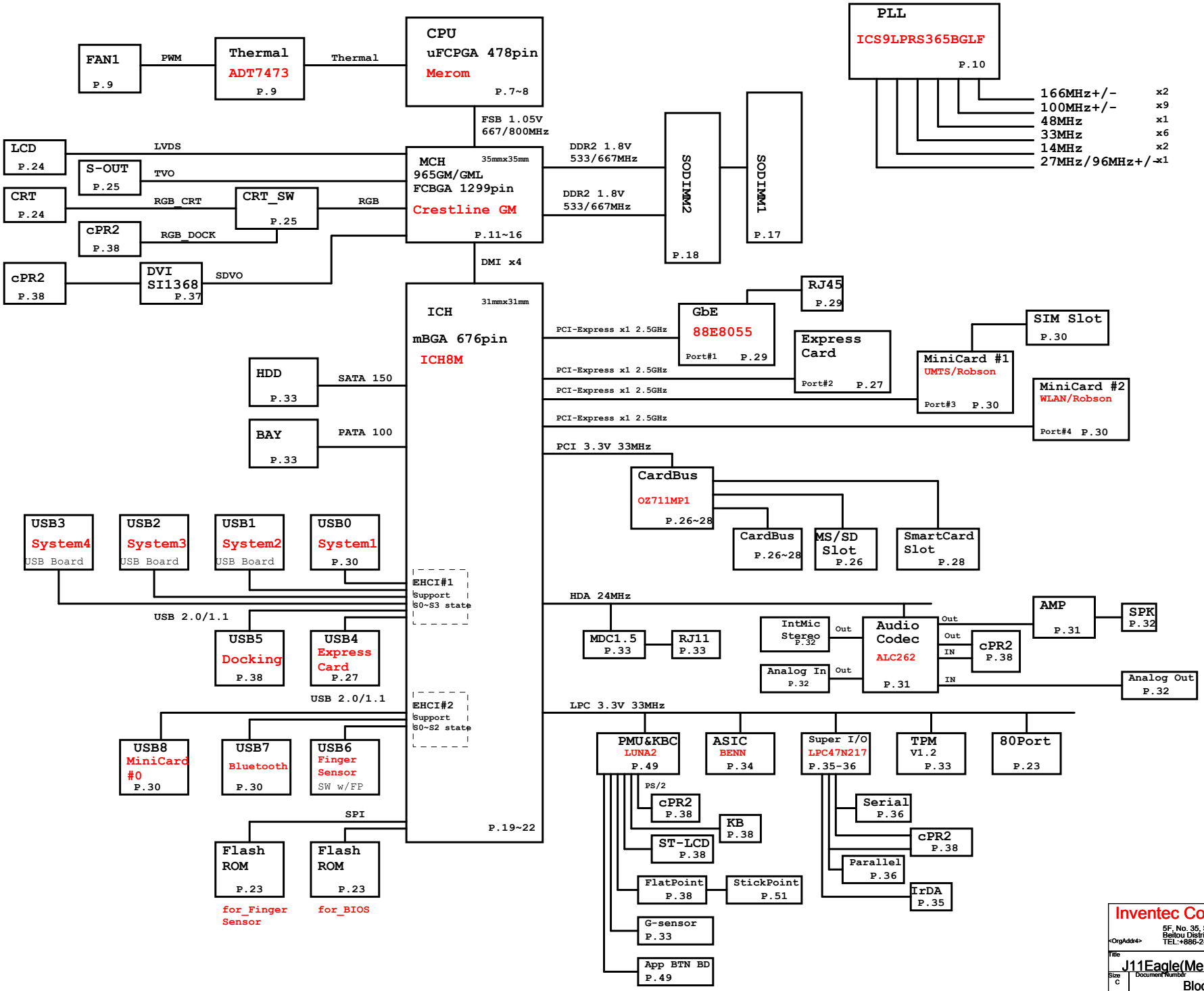
3. Block Diagram :



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4. Nat name Description :

Voltage Rails

PWR_DCIN	Primary DC system power supply
+5VLA	5.0V always on power rail by LATCH or ACIN
PWR_3VSTD	3.3V always on power rail by LATCH or ACIN
PWR_PMU	3.3V always on power rail by ECPWON
PWR_5VSUS	5.0V power rail by SLP_S5#_3R
PWR_3VSUS	3.3V power rail by SLP_S5#_3R
PWR_5VMAIN	5.0V switched power rail by SLP_S3#_3R
PWR_3VMAIN	3.3V switched power rail by SLP_S3#_3R
PWR_CPUCORE	Core Voltage for CPU
PWR_1.05VMAIN	1.05V power rail for AGTL+ termination/Core for GMCH by SLP_S3#_3R
PWR_1.5VMAIN	1.5V power rail for CPU PLL/DMI;PCIE;DDRII DLLs for GMCH/Core;PCIE for ICH7m by SLP_S3#_3R
PWR_1.8VSUS	1.8V power rail for DDRII by SLP_S5#_3R
PWR_DIMM_VTT	0.9V DDRII Termination Voltage by SLP_S3#_3R

Part Naming Conventions

C = Capacitor
CN = Connector
D = Diode
F = Fuse
L = Inductor
Q = Transistor
R = Resistor
RP = Resistor Pack
U = Arbitrary Logic Device
Y = Crystal and Osc

Net Name Suffix

= Active Low signal

5. Board Stack up Description

PCB Layers

Layer 1	Component Side, Microstrip signal Layer
Layer 2	Ground Plane
Layer 3	Stripline Layer
Layer 4	Power Plane
Layer 5	Stripline Layer
Layer 6	Stripline Layer
Layer 7	Ground Plane
Layer 8	Solder Side,Microstrip signal Layer

	Single End Impedance	Differential Impedance for Microstrip	Differential Impedance for Stripline
Host Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SRC Clock	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
Host Bus	55 ohm +/- 15%		
DDR2 CLK	42 ohm +/- 15%	70 ohm +/- 20%	70 ohm +/- 20%
DDR2 Strobe	55 ohm +/- 15%		85 ohm +/- 20%
DDR2 Bus	55 ohm +/- 15%		
DMI Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
PCIE Bus	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
SATA		95 ohm +/- 15%	100 ohm +/- 15%
SDVO	55 ohm +/- 15%	95 ohm +/- 15%	100 ohm +/- 15%
LVDS		100 ohm +/- 15%	100 ohm +/- 15%
USB		90 ohm +/- 15%	90 ohm +/- 15%
IEEE1394		110 ohm +/- 15%	110 ohm +/- 15%
Lan	50 ohm +/- 15%		

Power Rail	Destination	Voltage	S0 Current
PWR_CPUCORE	MeromHFM:	1.3319V~1.4375V~1.4591V	36A
	LFM:	0.9221V~0.9625V~0.9739V	
PWR_1.05VMAIN	Merom: AGTL+ termination	0.997V~1.05V~1.102V	2.5A
	965GM: Core	1.0V~1.05V~1.1V	4.6A
	965GM: AGTL+ termination	0.9475V~1.05V~1.1025V	1.4A
	ICH8m:		
PWR_1.5VMAIN	Merom PLL	1.425V~1.5V~1.575V	120mA
	965GM: PCIE	1.425V~1.5V~1.575V	1.5A
	965GM: LVDS	1.425V~1.5V~1.575V	60mA
	965GM: TVDAC	1.425V~1.5V~1.575V	24mA
	965GM: Various PLLS analog supply	1.425V~1.5V~1.575V	320mA
	965GM: DDR DLLS,DDRII,FSB HSIO	1.425V~1.5V~1.575V	1.885A
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	Mini Card:		
	Express Card:		
PWR_1.8VSUS	965GM: DDRII System Memory	1.7V~1.8V~1.9V	3.1A
	SO-DIMM:		
	965GM: LVDS analog	1.7V~1.8V~1.9V	10mA
	965GM: LVDS I/O	1.7V~1.8V~1.9V	60mA
	965GM: PCIE analog		2mA
	CLOCK GEN.		
PWR_DIMM_VTT	DDRII Terminator:	0.855V~0.9V~0.945V	1.0A
PWR_3VSUS	965GM: HV CMOS	3.135V~3.3V~3.465V	40mA
	965GM: TVDAC analog	3.135V~3.3V~3.465V	120mA
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	ICH8m:		
	Mini Card:		
	Express Card:		
	CLK Generator: ICS9LPRS365AGLF	3.135V~3.3V~3.465V	400mA
	Mini PCIe: WirelessLan		
	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	Azalia MDC:		
	HDD: SATA		
	965GM: CRT DAC		70mA
PWR_3VMAIN	CardBus: OZ711MP1	3.0V~3.3V~3.6V	
	CardBus: Slot voltage		
	Lan: Broadcom 88E8055		
	Card Reader: SD/MMC/MS		
	Azalia MDC: For wake up		
	Mini PCI: For wake up		
PWR_3VSTD	ICH8m:		
	ICH8m:		
	ICH8m:		
	LCD:	3.0V~3.3V~3.6V	1.0A
PWR_3VMAIN	Azalia Codec: ALC262	3.0V~3.3V~3.6V	
	Azalia MDC:		
	HDD: SATA	4.75V~5.0V~5.25V	Max: 1.0A ; R/W: 460mA ; STDBY: 70mA
	ODD: PATA	4.75V~5.0V~5.25V	Max: 1.8A ; R/W: 900mA ; STDBY: 45mA
	Audio AMP: G1412		
	Woofer AMP: G1432		
	Inverter:		
PWR_5VMAIN	CardBus: Slot voltage		
	USB: x 4 ports	5V	2.0A
PWR_3VSTD	EC:		
	ICH8m: RTC		
	Flash ROM: BIOS		

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6.Schematic modify Item and History :

V0.1 MODIFY LIST

1. Change R75 from 10K to 100K. (Page 39)
2. Change R291 from 470K to NU. (Page 27)

V0.2 MODIFY LIST

1. ADD DVI function. (Page 37)
2. U27 pin K1 and M1 (AVCC) have to be connected from CORE_VCC to PCI_VCC. (Page 26)
3. DG_AMP_SD# change from U54 Pin 47 to U54 Pin 3. (Page 26)
4. R457,R468 change to 100 Ohm 1%, R462 change to 5.1K Ohm 1%, R127 change to 100K 1% add R758 0 Ohm---- Adjust OCP 10A (Page 45)
5. R98 change to 2.2K 0.5%, R93 change to 39K 0.5% ---- Adjust Changer current. (Page 48)
6. Change X2 pin5 from GND to PWR_PMU (Page 34)
7. R102 change from 10K to 20K 1% ---- Adjust OCP 10A (Page 44)
8. Change R176 from 10K to 12K1% ---- Adjust OCP 7A (Page 47)
9. Change R616 from 4.7K to 475 Ohm ---- CLKREQ damping (Page 10)
10. R515 change from 1.3K to 1.27K ---- adjust CRT REFSET. (Page 12)
11. Del R622 and change D35 (PP gate) from PWR_3VSTD to PWR_5VSUS, change D35 (P gate) from PWR_3VSTD to PWR_3VSUS --- improve leakage. (Page 22)
12. R271 change from 3.48K to 3.9K, R238, R228 change from 2.1K to 2.67K.---- Ajust CPU Core load line (Page 39)
13. Change R132 from 243 Ohm to 249 Ohm ---- Ajust PWR_3VMAIN_ATBG (Page 15).
14. Change R433 (0 Ohm) to NU. (Page 30)
15. Change R56 from 1K to NU.--- Set DOCK EXIST. (Page 34)
16. Change R444 connect from DLY_SUSB# to DLY_SUSC#.--- Modify PWR_1.8VSUS power syquence. (Page 44)
17. R293,R641,R642,R564,R569 change power plane from PWR_3VSUS to PWR_3VMAIN. ---- for S3 leakage. (Page 10)
18. CL_VREF1_ICH pull up change from PWR_3VSTD to PWR_3VMAIN. (Page 21)
19. R351 from 100K to NU ---- follow FJ schematics. (Page 47)
20. Add 470k ohm to LCDCL##_LUNA (Page 49)
21. change Speaker lines dumping-resistersR391,R390,R389,R388 to Filter L66,L67,L68,L69. (Page 32)
22. C307, C311 change from 10PF to 15PF fro RTC. (Page 19)
23. Add R759 470K, R758 0 Ohm. (Page49)
24. R673 change 10K to 220K. (Page 30)
25. C654,C655 change from 0.1uf/10V to 0.1uf/25V.
26. R214,R215 change from 0 Ohm to 2.2 Ohm.
27. Change R719,R721 from 10K to 12.4K (Page 31)
28. Add R767,R768 voltage divide to add "Maximum Power Clampping Function" to avoide damaging the speaker. (Page 31)
29. Change G-sensor from KXPS5-3176 to LIS302ALK (Page 33)
30. M_VREF add R760 0 Ohm to connect to U37 Pin6. (Page 45)
31. TP16 connect to change from PWR_DIMM_VTT to M_VREF. (Page 17)
32. Add C842~C867, C870~C876 for EMI.
33. Change Q53, Q54 from SI2301BDS-T1-E3 to RVE002P03. (Page 43)
34. U34 Pin5 change from PWR_3VSTD to PWR_5VMAIN. (Page 39)
35. C354,C359,C337,C674,C676,C679 change from NU to 5P 50V for EMI.
36. RS47,RS52,RS53,RS55 change from 2.2K to NU, RS29,RS30,RS48,RS54change from 1K to NU. (Page33)
37. Change R31: 47K => 1K, R37:4.7K => 1K, C63: 0.01uF => None
38. Change R1,R2,C1,C2,U30 to NU (Page29)
39. R356 (0.01ohm)-> 0.015ohm, R33 (18k ohm)-> 12 k ohm, R28 (33k ohm) -> 10k ohm, R24 (30k ohm)-> 39k ohm (Page43)

V0.3 MODIFY LIST

1.Change Q113~Q120 from PDTC144EU to 2SC2412KR for SMBUS issue.
2.Change LAN_DISABLE# pull-up from PWR_PMU to PWR_3VLAN, Change U30,R1,R2 from NU to install. Add L72,L73,L74,L75 common chock for EMI. (Page 29)
3.Change D35 Pin P from PWR_3VSUS to PWR_3VSTD (Page 22)
4. Add "L71" between these signals as below picture for reduce the noise on 1.5VS_TVDAC (Page 15)
5. Remove U41, U48, Mount R664. Add the Pull-up for "SPI_CE#0" with PWR_3VMAIN(RS31 Pin 4) (Page 23).
6. Change U18 from PI5V330SQE to PI5V330SQ1(Page 25)
7. Change U50 from OZ2216S to OZ2206SN.(Page 27)
8. Change C700 from 1000pF/NU to 0.01uF for TPS2231_CLKEN drop. (Page 28)
9. Add R773, R772 0 Ohm between L57, C419 & L56 & C420. Swap Q112 Pin S & Pin D(Page 32)
10. Add MS request the micrphone performance. (Page 32)
11. Change Bay con pin for move glide pad con. and stick con. to bay board. (Page 33)
12. Change RF_ON_SW from SW1 Pin3 to pin1. (page 34)
13.Please add R774 & D37, D36, change r733 from 10K to 1K to the DVI control signals. (Page 37)
14. Change R63,R64,R65 from 75 to 200 fro VESA mesurement. (Page 38)
15. Add D38,D39 for discharge. (Page 39)
16. Change U26 PWRGD & CLKEN# pull up from PWR_3VMAIN. (Page 40)
17. Change R654 from 470K to 100K, and R646 from 47K to 10K. power on/off,S4 fail issue.(Page 41)
18. Change circuit for fix PWR_BT1ROM/PWR_BT2ROM signals don't work issue. (Page 42)
19. Change GPU VID0~VID4 default from 00100 to 00010. (Page 46)
20. Add and reserve USB switch circuit (page 51)
21. Change U1002 from AAT4610AIGV to FPF2101, Add RS1001 for A6,A7,D6,D7 to GND. (Page 52)

V0.3 MODIFY LIST

22. Change R772, R773 from 0 Ohm to 47 Ohm. (Page 32)
23. Del R123, R124, R758, and mount R769. (Page 46)
24. Del U56, R320, R321, R287, C772, and mount R288, R308, R309, R310, R311, R312, R313 , and OZ711MP1 change to OZ711SP2(Page 26)
25. LAN_RST# tie to GND.(Page 21)
26. Remove R189, R193 (Page 21)

V0.4 MODIFY LIST

1. LAN_RST# pull down with 10K Ohm. (Page 21)
2. Delete Pull-up(R2) for LAN_Disable.(Page 29)
3. Delete RS1001, and A6,A7,D6,D7 tie to GND(SW with FP Page 52)
4. ALG_HP_R_DOCK & ALG_HP_L_DOCK add 22K pull down, and change R59,R62 from 0 Ohm to 27K Ohm at V04. (Page 38)
5. CN14 pin37 tie to GND. (Page 30)
6. Change the G-sensor vender from ST-micro to KIONX. Change U14 and R101(1K)/R95 (NU) (Page 33).
7. For Express Card leakage issue, please consider following. * U45 pin2 : From "PWR_3VMAIN" to "PWR_3VSTD". * U45 pin20 : From "SUSC#" to "PWR_3VSTD". * U44 pin5 : From "PWR_3VMAIN" to "PWR_3VSTD" (Page 28)
8. Add U62(NU), R796 for SC_CD#, change R298 from NU to 10K, C398 from NU to 0.01uF, C391 from NU to 0.1uF. (Page26, 28)
9. Change R691,R698 : 22K => 100K, C743,C749 : 1000pF => 220pF for the internal MIC volume small (Page 32)
10. Change C395 from NU to 470uF
11. Delete L72,L73,L74,L75 (Page 29)
12.Change C307,C311 from 10pF to 15pF. (Page 19)
13. Add L72(100ohm bead)---NU, C890 (10uF)----NU for PWR_BL noise. (Page 24)
14. Change R684 from 10K to 1K.(Page 44)
15. Change R63,R64,R65 from 200 Ohm to 150 Ohm at V04 (Page 38)
16. Change C119 from 0.1uF to 1uF at V04 (Page30)

V0.2 Daughter Board Modify LIST

1.Change R1005 from 15K Ohm to 1.5K Ohm, and Net G_USBON add R1012 (NU) to CN1003 pin 14. (FingerPrinter Board)
2.C1011 change from U1001 Pin D8 to Pin D9.

V0.3 Daughter Board Modify LIST

1.Cut CN1-11pin & SW_GND1,then add zero-ohm resister between CN1-11pin & SW_GND1.(SW board)
2.Change R1012 to NU (Finger Printer board)
~~3.Mount: R1301, R1302, U1301, Remove: R1305, R1306 (FP board)~~

V0.4 Daughter Board Modify LIST

1. Delete RS1001, and A6,A7,D6,D7 tie to GND(Page 52)

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8. Layout Guideline :

Crestline DDRII Layout Guidelines

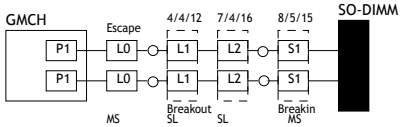
DDRII Signal Groups

Group	Signal Name
Data	M_A_DQ[63..0]/M_B_DQ[63..0] M_A_DM[7..0]/M_B_DM[7..0] M_A_DQS[7..0]/M_A_DQS#[7..0] M_B_DQS[7..0]/M_B_DQS#[7..0]
Address	M_A_A[13..0]/M_B_A[13..0] M_A_BS[2..0]/M_B_BS[2..0] M_A_RAS#/M_B_RAS# M_A_CAS#/M_B_CAS# M_A_WE#/M_B_WE#
Control	M_CS#[3..0] M_CKE[3..0] M_ODT[3..0]
Clock	M_CLK_DDR[3..0] M_CLK_DDR#[3..0]
FeedBack	SA_RCVEN#/SB_RCVEN#

Length Matching and Length Formulas

Signal Group	Minimum Length	Maximum Length
Control-to-Clock	Clock - 1.0"	Clock - 0.0"
Command-to-Clock	Clock - 1.0"	Clock + 1.0"
Strobe-to-Clock	Clock - 0.5"	Clock + 1.0"
Data-to-Strobe	Strobe - 220mils	Strobe - 180mils

CLK group : M_CLK_DDR[3..0],M_CLK_DDR#[3..0]

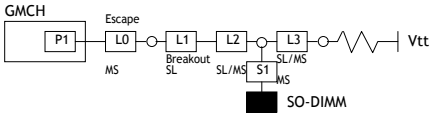


Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	42 +/- 15%
Differential Mode Impedance	70 +/- 20%
Package Length Range - P1	350 mils – 625 mils
Min. Serpentine Spacing	25 mils
Trace Length Limit - L0 (MS)	Length Limit: Max = 50 mils (Escape)
Trace Length Limit - L1 (SL) (Breakout length segment)	Length Limit: Max = 700 mils Min. Trace Spacng (Other) : 12 mils
Trace Length Limit - L2 (SL)	Min. Trace Spacng (Other) : 16 mils Nominal Trace Width : Outer: 8.5/4/8.5 Inner: L3= 7/4/7, L5&L6=8/4/8 Min. Trace Spacng (pair) : 4mils
Stub Length S1-Stub from via to SO-DIMM	Max = 200 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1	Min = 500 mils Max = 4000 mils
Total Length - P1 + L0 + L1 + L2 + S1	Max = 4500 mils Total Length for Channel A : X0 Total Length for Channel B : X1
Maximim Via Count	2 (Per side)
SCK to SCK# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length)	Match Channel A clocks to X0 +/- 20mils Match Channel A clocks to X1 +/- 20mils
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4/12 mils to other DDR2 Outer Layer : 5/15 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	CK to CK# spacing rule waived at connector spacing of 15 mils to other DDR2 Max. breakin length is 200 mils

Feedback group :
M_A_RCVENIN#,M_A_RCVENOUT#,M_B_RCVENIN#,M_B_RCVENOUT#

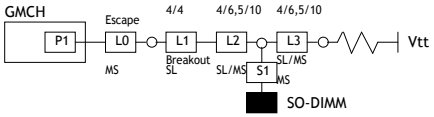
These signals are routed internally on the GMCH package and don't require any routing on the MB. As a result, can be left as NC.

Control group : M_CKE[3..0],M_CS#[3..0],M_ODT[3..0]



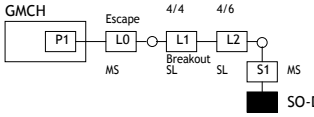
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15% L2 Seg.= 45Ohm +/- 15%
Nominal Trace Width	Inner Layer : L3=5.5 mils, L5&L6= 7 mils Outer Layer : 5 mils
Minimum CTRL Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	400–800 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CTRL </= (CLK-0.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Command group :
M_A_A[13..0],M_B_A[13..0],M_A_BS[2..0],M_B_BS[2..0],M_A_RAS#, M_B_RAS#,M_A_CAS#,M_B_CAS#,M_A_WE#,M_B_WE#



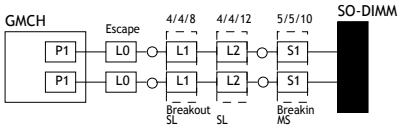
Topology	Point-to-Point with parallel termination
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : L5&L6= 4.5 mils Outer Layer : 5 mils
Minimum CMD Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	250–750 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Trace Length L3	Max = 1500 mils
Parallel Termination Resistor	56 +/- 5%
Maximim Via Count	3
CTRL to SCK/SCK# Length Matching (Total Length including package)	(CLK-1.0") </= CMD </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data group : M_A_DQ[63..0],M_B_DQ[63..0],M_A_DM[7..0],M_B_DM[7..0]



Topology	Point-to-Point
Reference Plane	Ground
Characteristic Trace Impedance	55 +/- 15%
Nominal Trace Width	Inner Layer : L5&L6= 4.5 mils Outer Layer : 5 mils
Minimum DQ Bus Trace Spacing	Inner Layer : 6 mils Outer Layer : 8 mils
Minimum Serpentine Spacing	Same as DQ-to-DQ routing
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length P1	750 mils +/- 350 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 700 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 4800 mils
Trace Length L3	Max = 1500 mils
Maximim Via Count	2
DQ/DM to DQS Length Matching (Total Length including package)	Match DQ/DM to [SDQS - 200mils] +/- 20mils, per byte lane
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 4 mils spacing allowed Outer Layer : 5 mils spacing allowed Max. breakout length is 500 mils

Data Strobe group : M_A_DQS[7..0],M_A_DQS[7..0]#,M_B_DQS[7..0],M_B_DQS[7..0]#



Topology	Differential Pair Point-to-Point
Reference Plane	Ground
Single Ended Trace Impedance	55 +/- 15%
Differential Mode Impedance	85 +/- 20%
Nominal Trace Width	Inner Layer :L3:5/5/5, L5&L6= 5/4/5 mils Outer Layer : 6/5/6 mils
Nominal DQS to DQS# Spacing (edge to edge)	Inner Layer : 4 mils Outer Layer : 5 mils
Minimum DQS to DQ Spacing	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Serpentine Spacing	Inner Layer : 8 mils Outer Layer : 10 mils
Minimum Spacing to Other DDR2	Inner Layer : 12 mils Outer Layer : 15 mils
Minimum Isolation Spacing to non-DDR2	25 mils
Package Length Range - P1	425–925 mils
Trace Length Limit - L0	Max = 250 mils (Escape)
Trace Length Limit - L1	Max = 500 mils (Breakout)
Stub Length S1-Stub from via to SO-DIMM	Max = 250 mils (Breakin)
MB Length Limits - L0 + L1 + L2 + S1 - From GMCH ball to SO-DIMM pad	Min = 500 mils Max = 4500 mils
Total Length - P1 + L0 + L1 + L2 + S1 - From GMCH die to SO-DIMM pad	Max = 5000 mils
Maximim Via Count	2 (Per side)
DQS to DQS# Length Matching	Match total length to within 5 mils
Clock to Clock Length Match (Total Length include package)	(CLK-0.5") </= DQS </= (CLK+1.0")
Breakout Exceptions (Reduce geometries for GMCH break-out region)	Inner Layer : 8 mils to other DDR2 Outer Layer : 10 mils to other DDR2 Max. breakout length is 500 mils
Breakin Exceptions (Reduce geometries for SO-DIMM break-in region)	DQS to DQS# spacing rule waived at connector spacing of 10 mils to other DDR2 Max. breakin length is 200 mils

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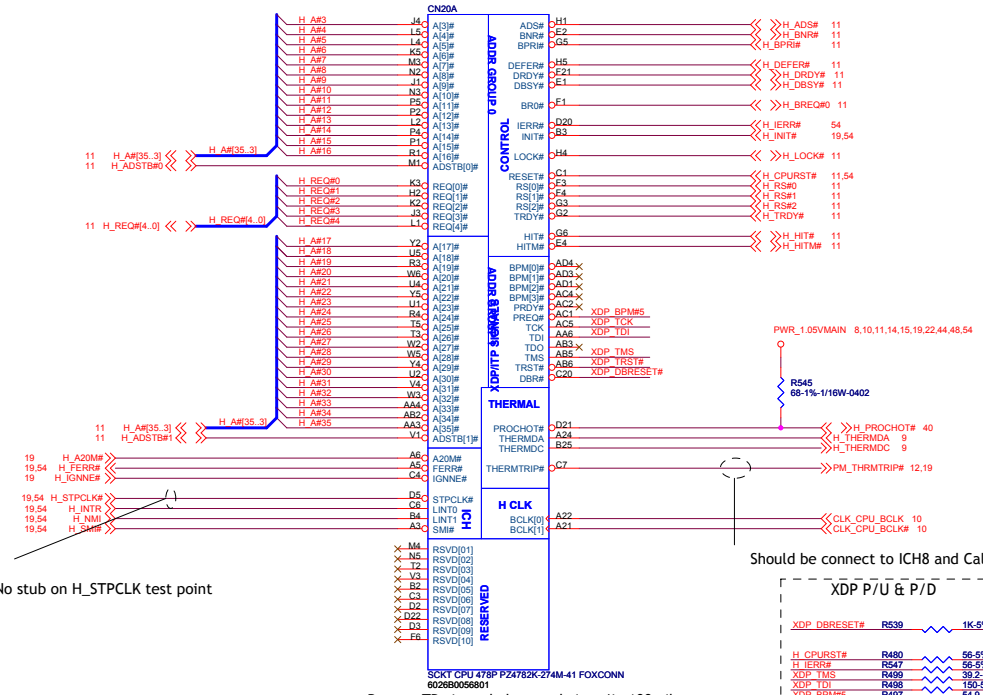
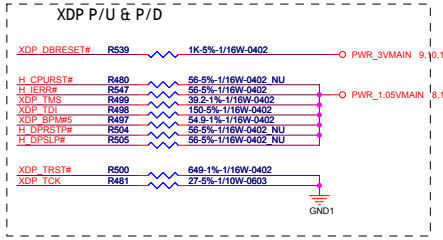


No stub on H_STPCLK test point

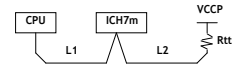
Should be connect to ICH8 and Calistoga without T-ing(no stub)

Rout to TP via and place gnd via w/in 100mils

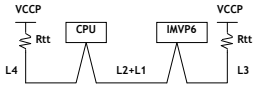
A#[32-39], APM#[0-1]:Leave escape routing on for future functionality



Topology : FERR#

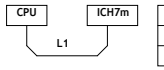


L1	L2	Rtt	Transmission Line
0.5" - 12"	0" - 3.0"	56 +/-5%	Micro-strip
0.5" - 12"	0" - 3.0"	56 +/-5%	Strip-line



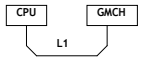
L1	L2	L3	L4	Rtt	Transmission Line
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Micro-strip
0.5" - 6.5"	0.5" - 6.5"	0" - 3.0"	0" - 3.0"	70 +/-5%	Strip-line

Topology : PWRGOOD



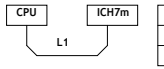
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : CPUSLP#



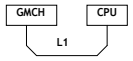
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : INTR , NMI , A20M# , DPSLP# , IGNNE# , INIT# , SMI# , STPCLK#



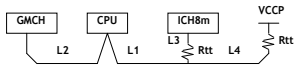
L1	Transmission Line
0.5" - 12"	Micro-strip
0.5" - 12"	Strip-line

Topology : RESET#



L1	Transmission Line
1" - 6"	Micro-strip
1" - 6"	Strip-line

Topology : THERMTRIP#

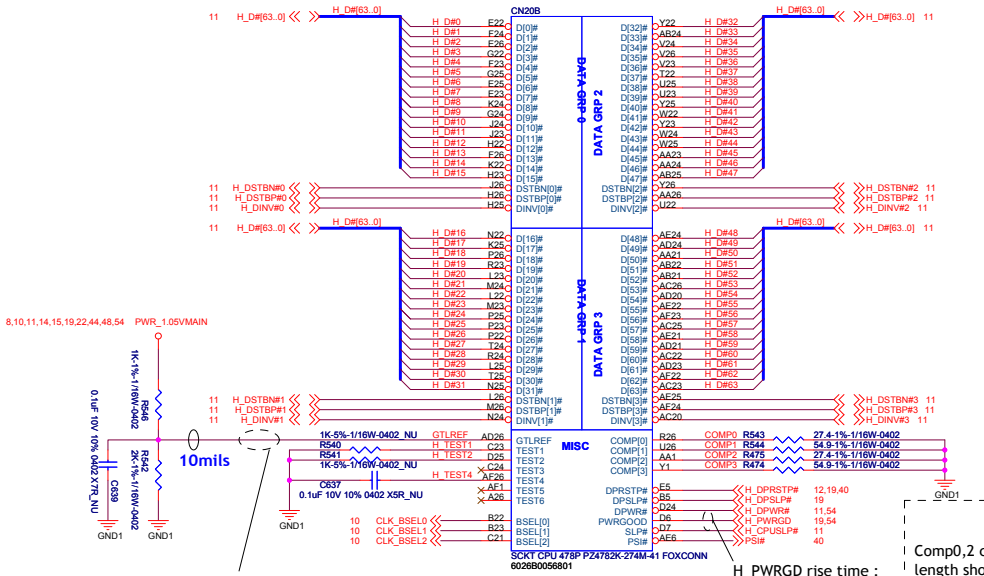


L1	L2	L1+L3	L3	L4	Rss	Rtt	Transmission Line
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Micro-strip
1" - 12"	1" - 6"	1" - 12"	0" - 3.0"	0" - 3.0"	24 +/-5%	56 +/-5%	Strip-line

FSB Common Clock Signal Layout Guide :

H_ADS# , H_BNR# , H_BPRI# , H_BR0# , H_DBSY# , H_DEFER# , H_DPWR# , H_DRDY# , H_HIT# , H_HITM# , H_LOCK# ,H_RS#[2..0] , H_TRDY# , H_CPURST#.

Transmission Line Type	Total Trace Length	Normal Impedance	Spacing (mils)
Strip-line(Int. Layer)	1.0 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
Micro-strip(Ext. Layer)			W=5 & S=10 mils



Zo=55ohm, 0.5" max for GTLREF, Space any other switch signals away from GTLREF with a minimum of 25mils.
Don't allow the GTLREF routing to create splits or discontinuities in the reference planes of the FSB signals

H_PWRGD rise time : Max : 15ns

Comp0,2 connect with Zo=27.4ohm, make trace length shorter than 0.5" and width is 18mils.
Comp1,3 connect with Zo=55ohm, make trace length shorter than 0.5" and width is 5mils

FSB Source Synchronous Data Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe-to-Strobe Complement Matching
H_D#[15..0] , H_DINV#0	+/- 100 mils	H_DSTBP#0, H_DSTBN#0	+/- 25 mils
H_D#[31..16] , H_DINV#1	+/- 100 mils	H_DSTBP#1, H_DSTBN#1	+/- 25 mils
H_D#[47..32] , H_DINV#2	+/- 100 mils	H_DSTBP#2, H_DSTBN#2	+/- 25 mils
H_D#[63..48] , H_DINV#3	+/- 100 mils	H_DSTBP#3, H_DSTBN#3	+/- 25 mils

FSB Source Synchronous Data Signal Routing Topology#1 :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)	
				Data-to-Data,Strobe-to-strobe	Strobe-to-Data
H_DINV#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=8 mils	N/A
H_DATA#[63..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=8 mils	N/A
H_DSTBN#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=4 mils	W=4 & S=12 mils
H_DSTBP#[3..0]	Strip-line	0.5 ~ 5.5 inch	55+/-15%	W=4 & S=4 mils	W=4 & S=12 mils

FSB Source Synchronous Address Length Variation and Strobe Matching Requirements :

Signals Name	Signals Matching	Strobes associated with the group	Strobe to Assoc. Address Signal Matching
H_A#[16..3] , H_REQ#[4..0]	+/- 200 mils	H_ADSTB#0	+/- 200 mils
H_A#[35..17]	+/- 200 mils	H_ADSTB#1	+/- 200 mils

*** No length matching requirements exist between H_ADSTB#0 and H_ADSTB#1

FSB Source Synchronous Address Signal Routing :

Signal Name	Transmission Line Type	Total Trace Length	Normal Impedance	Width & Spacing (mils)
H_A#[35..3]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
H_REQ#[4..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=8 mils
H_ADSTB#[1..0]	Strip-line	0.5 ~ 6.5 inch	55+/-15%	W=4 & S=12 mils

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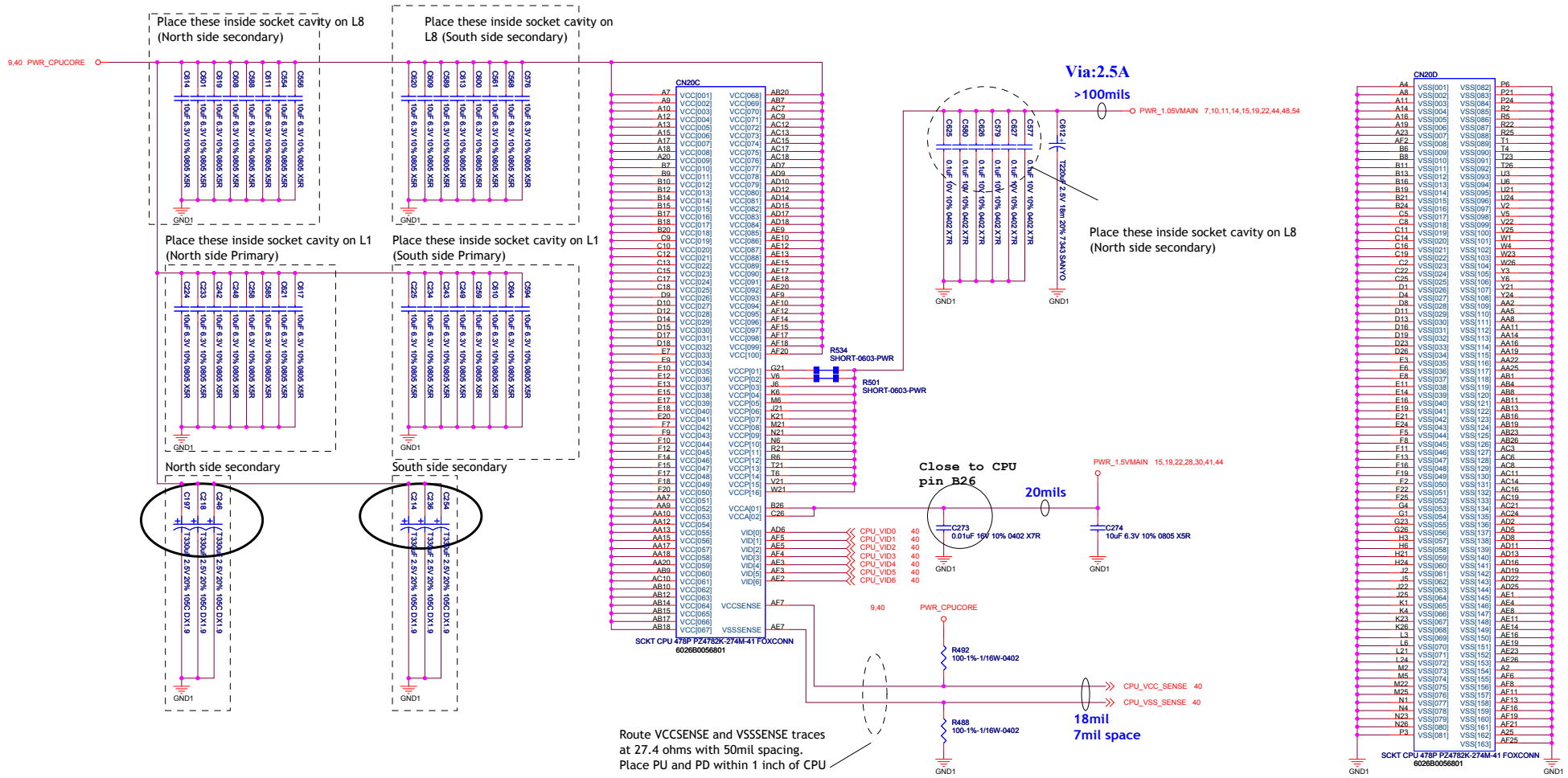
Size: C | Document Number: Merom Processor(1/2) | Rev: 0.4
Date: Monday, April 09, 2007 | Sheet 7 of 55



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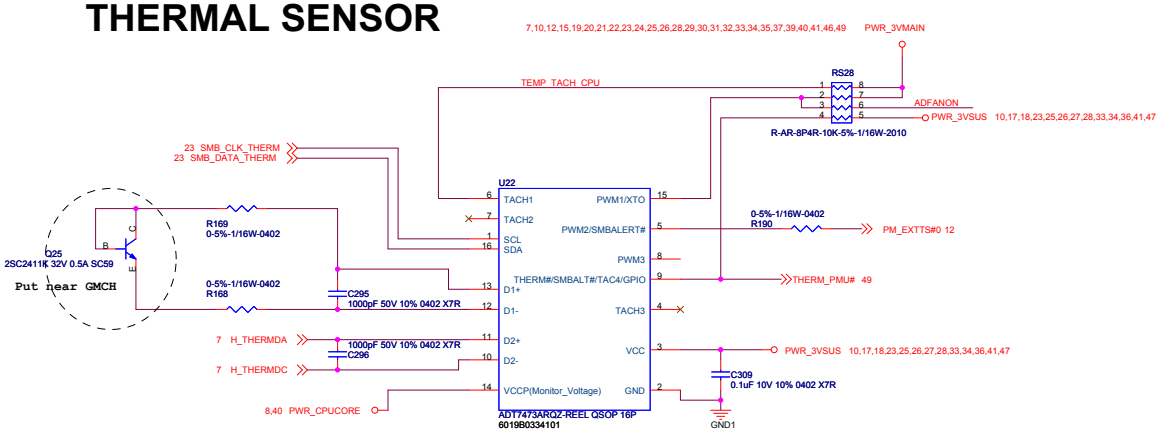
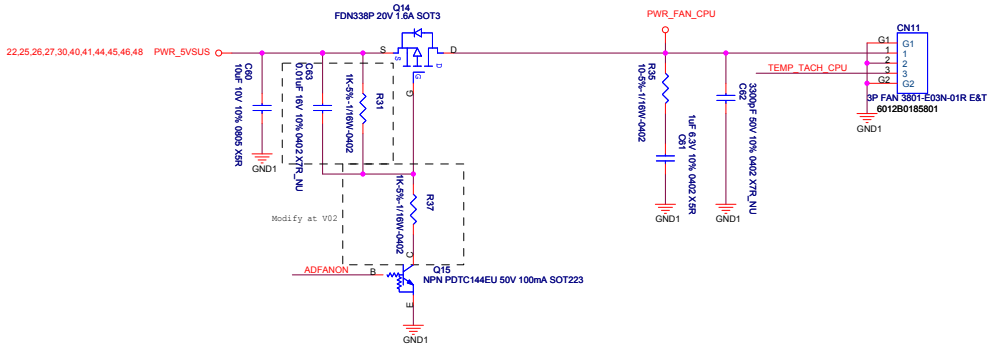
Date: Monday, April 09, 2007 | Sheet 8 of 55

THERMAL SENSOR





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Title		
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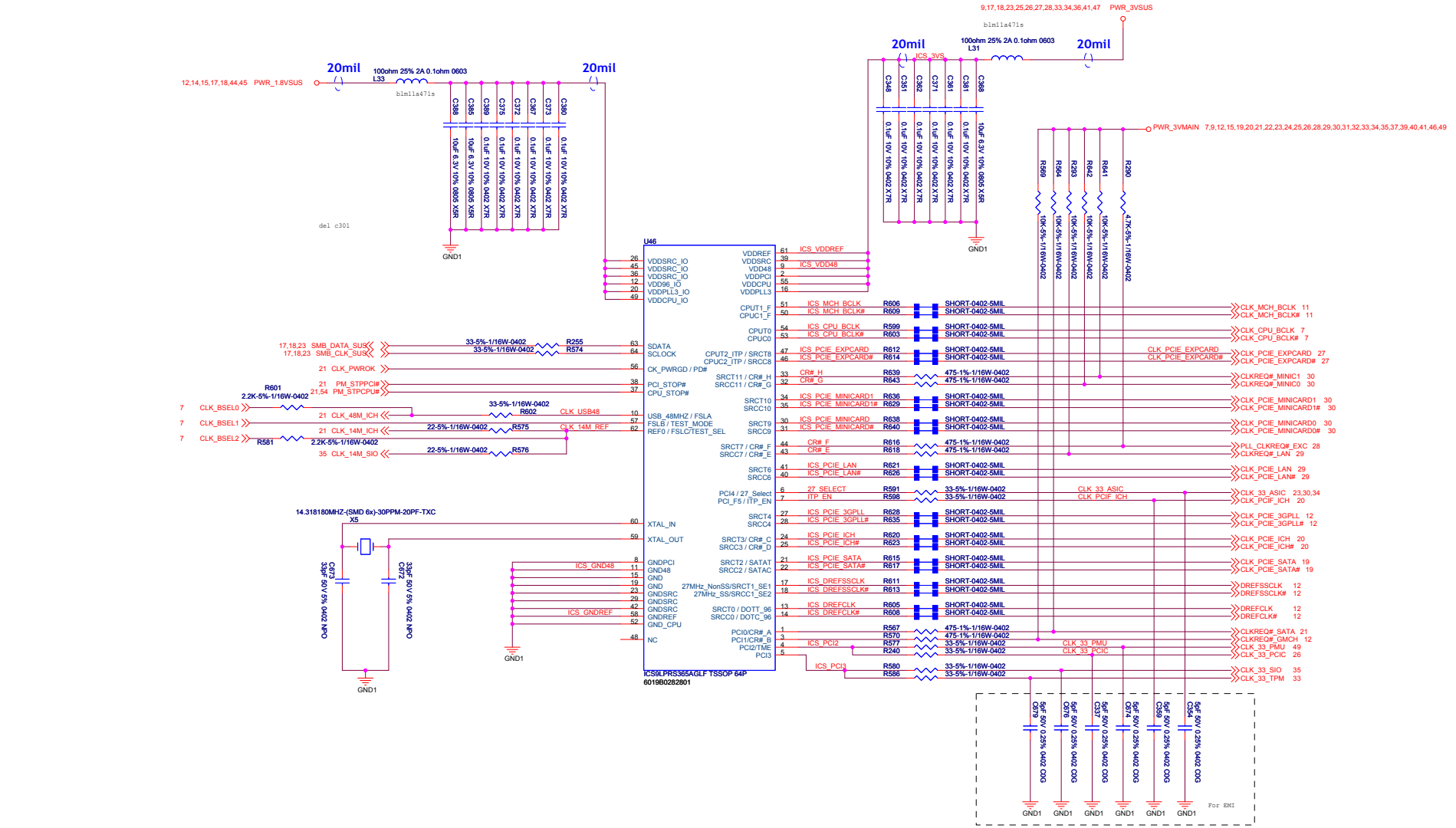

Clock Request table

CLKREQ#_pin	Clocks	Select	
CR#_A	SRCCLK0 SRCCLK2	V	Byte 5, bit 7=1 Byte 5, bit 6=1
CR#_B	SRCCLK1 SRCCLK4	V	Byte 5, bit 5=1 Byte 5, bit 4=1
CR#_E	SRCCLK6	V	Byte 6, bit 7=1
CR#_F	SRCCLK8	V	Byte 6, bit 6=1
CR#_G	SRCCLK9	V	Byte 6, bit 5=1
CR#_H	SRCCLK10	V	Byte 6, bit 4=1

FSA	FSB	FSC	FSB CLOCK FREQUENCY	HOST CLOCK FREQUENCY
1	1	0	667	166
0	1	0	800	200 ★

ITP_EN =0
SRC#/SRC#
ITP_EN =1
ITP/ITP#

27_Selet =0
LCD_SST 100MHZ
27_Selet =1
27MHZ non-spread clock

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Document Number: Clock Generator
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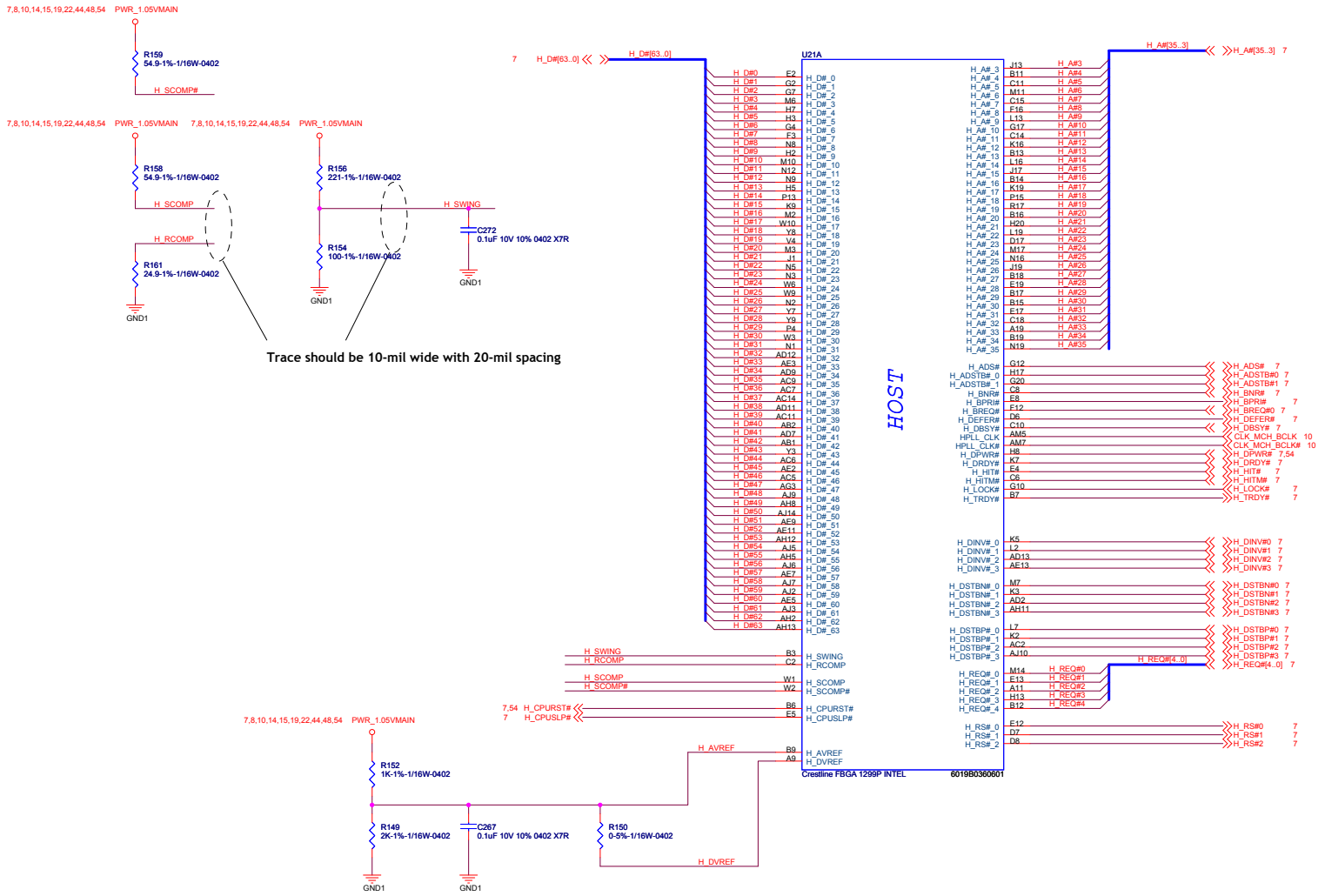

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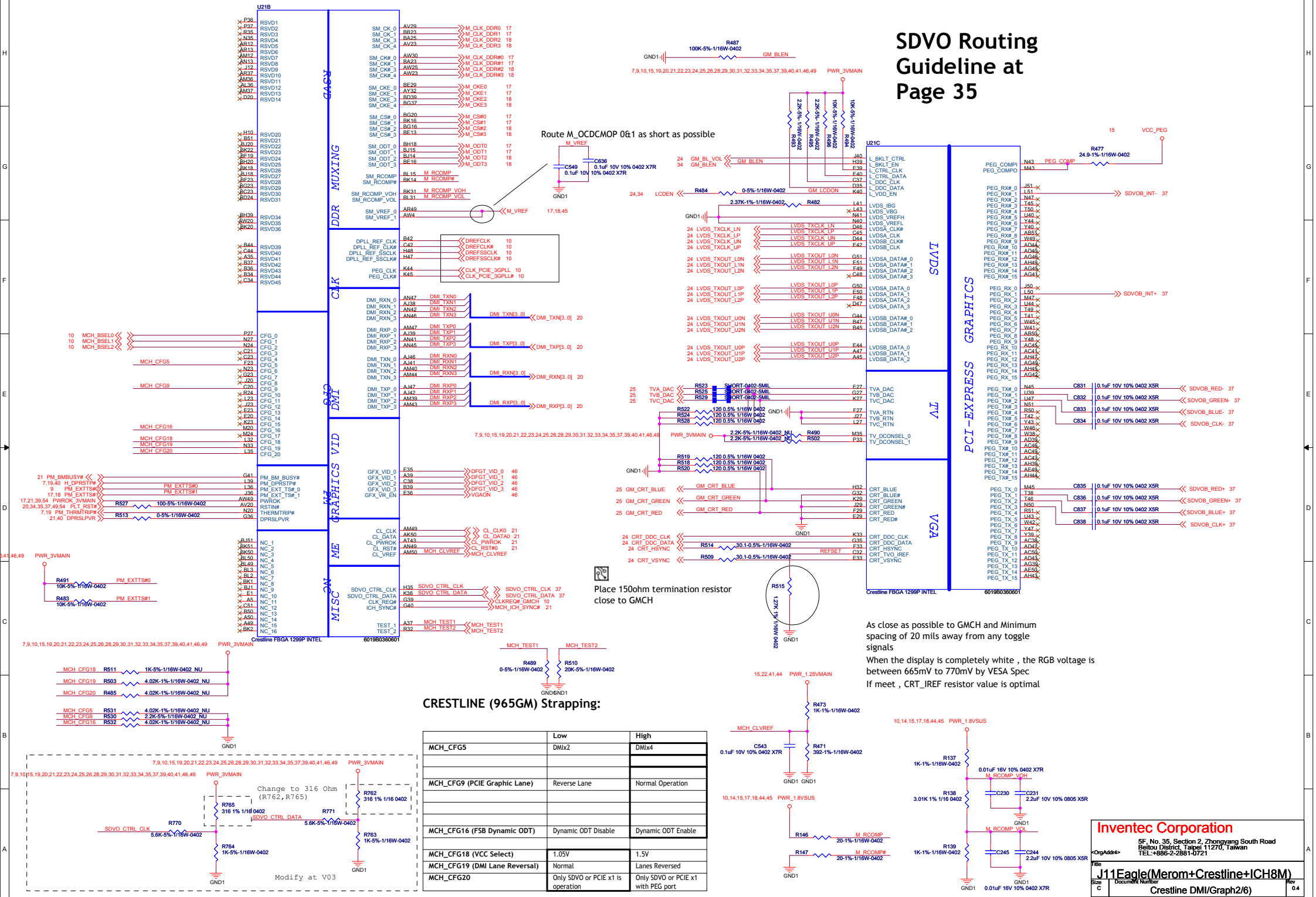
SDVO Routing Guideline at Page 35



CRESTLINE (965GM) Strapping:

	Low	High
MCH_CFG5	DMIx2	DMIx4
MCH_CFG9 (PCIE Graphic Lane)	Reverse Lane	Normal Operation
MCH_CFG16 (FSB Dynamic ODT)	Dynamic ODT Disable	Dynamic ODT Enable
MCH_CFG18 (VCC Select)	1.05V	1.5V
MCH_CFG19 (DMI Lane Reversal)	Normal	Lanes Reversed
MCH_CFG20	Only SDVO or PCIE x1 is operation	Only SDVO or PCIE x1 with PEG port

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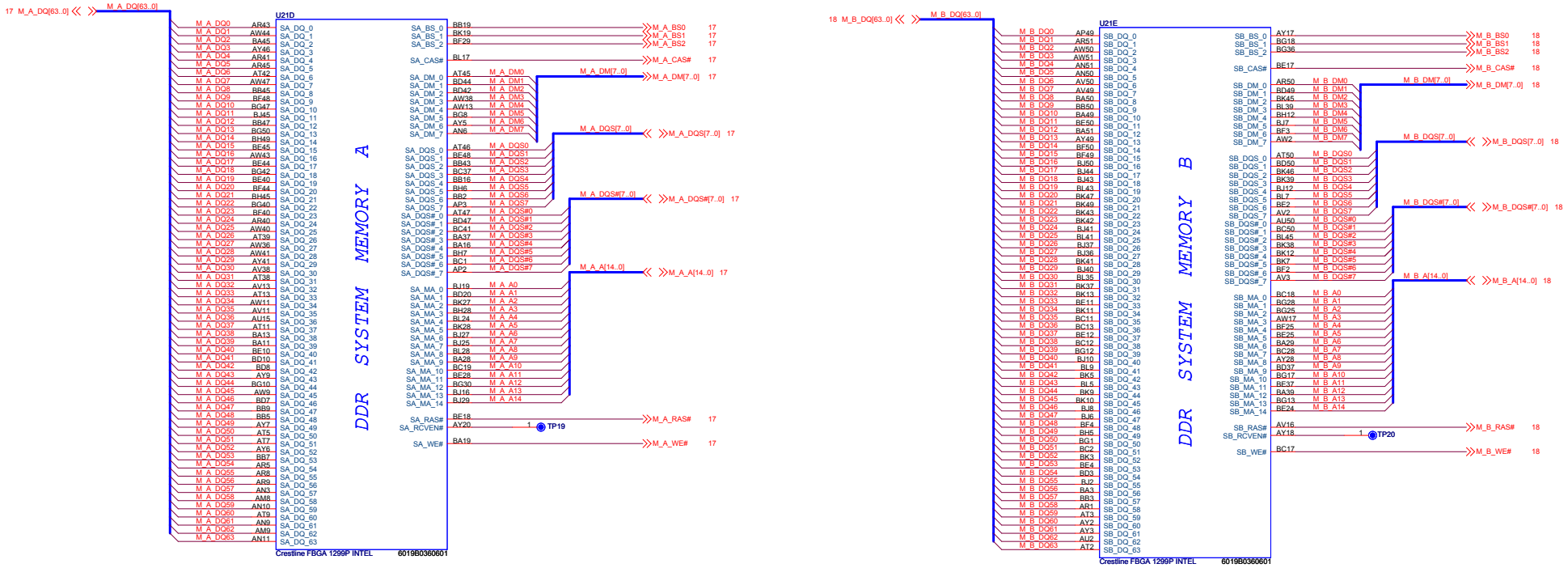

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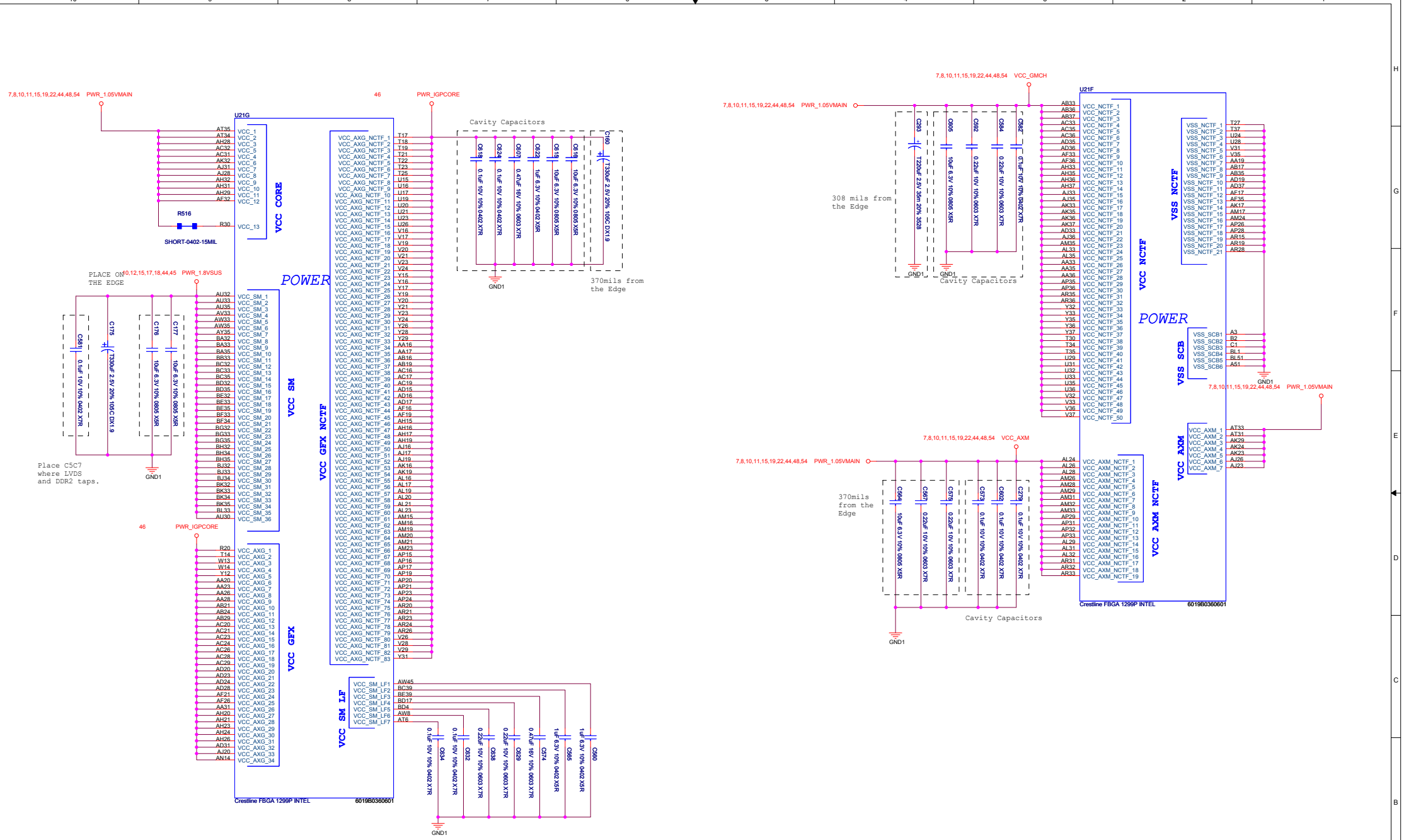
Size: C | Document Number: Crestline DDR2(3/6) | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 13 of 55



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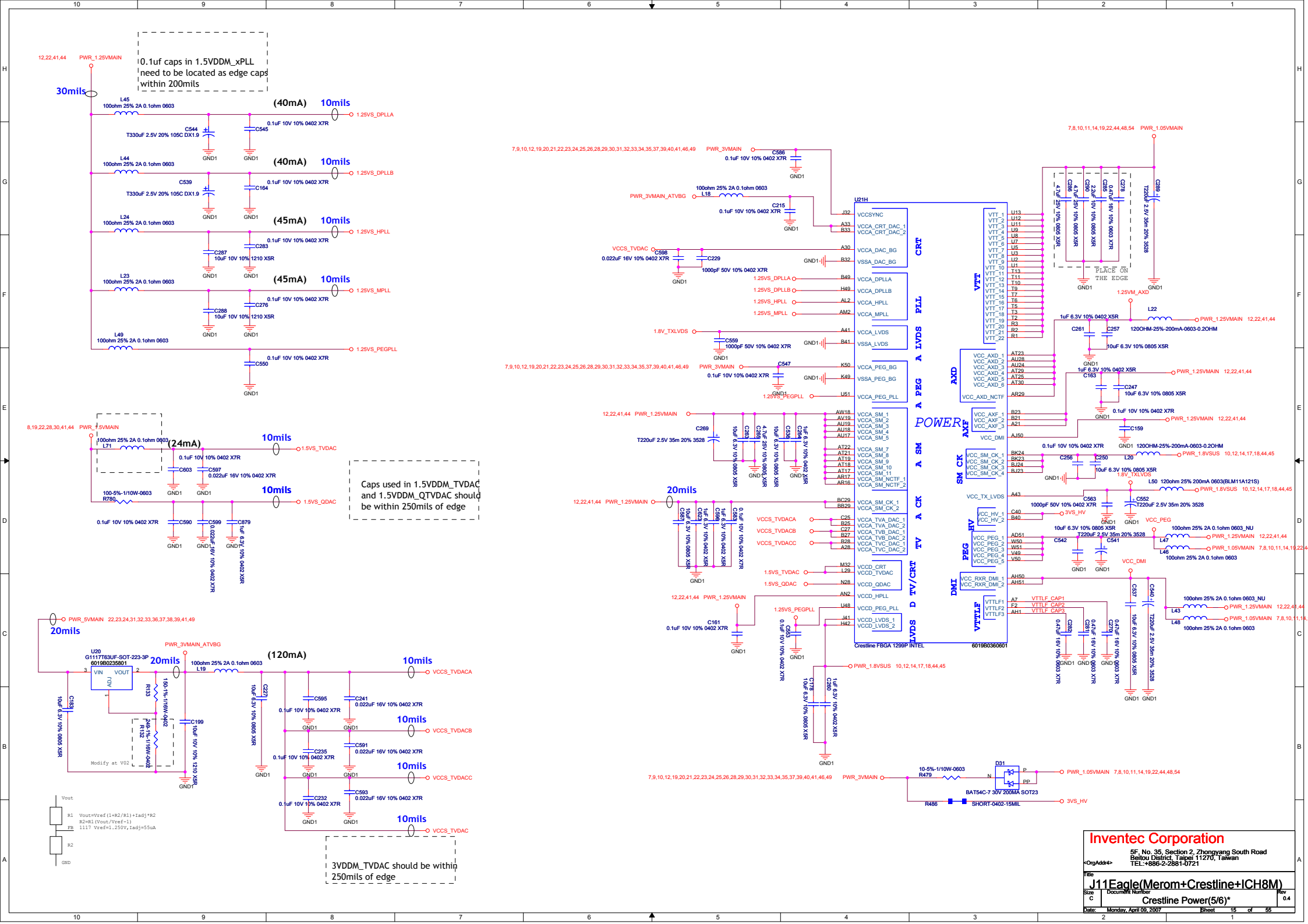
Size: C | Document Number: Crestline Power(4/6) | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 14 of 55


0.1uf caps in 1.5VDDM_xPLL need to be located as edge caps within 200mils
12,22,41,44 PWR_1.25VMAIN
30mils
L45 100ohm 25% 2A 0.1ohm 0603
(40mA)
10mils
1.25VS_DPLLA
C544 T330uF 2.5V 20% 105C DX1.9
C545 0.1uF 10V 10% 0402 X7R
L44 100ohm 25% 2A 0.1ohm 0603
1.25VS_DPLLB
C539 T330uF 2.5V 20% 105C DX1.9
C164 0.1uF 10V 10% 0402 X7R
L24 100ohm 25% 2A 0.1ohm 0603
(45mA)
1.25VS_HPLL
C287 10uF 10V 10% 1210 X5R
C283 0.1uF 10V 10% 0402 X7R
L23 100ohm 25% 2A 0.1ohm 0603
1.25VS_MPLL
C288 10uF 10V 10% 1210 X5R
C276 0.1uF 10V 10% 0402 X7R
L49 100ohm 25% 2A 0.1ohm 0603
1.25VS_PEGPLL
C550 0.1uF 10V 10% 0402 X7R
GND1
8,19,22,28,30,41,44 PWR_1.5VMAIN
L71 100ohm 25% 2A 0.1ohm 0603
(24mA)
1.5VS_TVDAC
C603 0.1uF 10V 10% 0402 X7R
C597 0.022uF 16V 10% 0402 X7R
R780 100-5%-1/10W-0603
1.5VS_QDAC
C590 0.1uF 10V 10% 0402 X7R
C599 0.022uF 16V 10% 0402 X7R
C879 1uF 6.3V 10% 0402 X5R
Caps used in 1.5VDDM_TVDAC and 1.5VDDM_QTVDAC should be within 250mils of edge
PWR_5VMAIN 22,23,24,31,32,33,36,37,38,39,41,49
20mils
U20 G1117T63UF-SOT-223-3P 6019B0235801
VIN VOUT ADJ
PWR_3VMAIN_ATVBG
20mils
100ohm 25% 2A 0.1ohm 0603 L19
(120mA)
10mils
VCCS_TVDACA
VCCS_TVDACB
VCCS_TVDACC
VCCS_TVDAC
C189 10uF 6.3V 10% 0805 X5R
R133 150-1%-1/16W-0402
R132 249-1%-1/16W-0402
Modify at V02
C199 10uF 10V 10% 1210 X5R
C227 10uF 6.3V 10% 0805 X5R
C595 0.1uF 10V 10% 0402 X7R
C241 0.022uF 16V 10% 0402 X7R
C235 0.1uF 10V 10% 0402 X7R
C591 0.022uF 16V 10% 0402 X7R
C232 0.1uF 10V 10% 0402 X7R
C593 0.022uF 16V 10% 0402 X7R
Vout
R1 Vout=Vref(1+R2/R1)+Iadj*R2
R2=R1(Vout/Vref-1)
FB 1117 Vref=1.250V,Iadj=55uA
R2
GND
3VDDM_TVDAC should be within 250mils of edge
7,9,10,12,19,20,21,22,23,24,25,26,28,29,30,31,32,33,34,35,37,39,40,41,46,49 PWR_3VMAIN
C586 0.1uF 10V 10% 0402 X7R
PWR_3VMAIN_ATVBG
100ohm 25% 2A 0.1ohm 0603 L18
C215 0.1uF 10V 10% 0402 X7R
VCCS_TVDAC
C598 0.022uF 16V 10% 0402 X7R
C229 1000pF 50V 10% 0402 X7R
1.25VS_DPLLA
1.25VS_DPLLB
1.25VS_HPLL
1.25VS_MPLL
1.8V_TXLVDS
C559 1000pF 50V 10% 0402 X7R
C547 0.1uF 10V 10% 0402 X7R
1.25VS_PEGPLL
12,22,41,44 PWR_1.25VMAIN
C269 T220uF 2.5V 35m 20% 3528
C283 10uF 6.3V 10% 0805 X5R
C285 4.7uF 25V 10% 0805 X5R
C526 10uF 6.3V 10% 0805 X5R
C284 1uF 6.3V 10% 0402 X5R
20mils
C287 10uF 6.3V 10% 0805 X5R
C523 1uF 6.3V 10% 0402 X5R
C286 1uF 6.3V 10% 0402 X5R
C525 0.1uF 10V 10% 0402 X7R
VCCS_TVDACA
VCCS_TVDACB
VCCS_TVDACC
1.5VS_TVDAC
1.5VS_QDAC
C161 0.1uF 10V 10% 0402 X7R
C553 0.1uF 10V 10% 0402 X7R
C178 10uF 6.3V 10% 0805 X5R
C260 1uF 6.3V 10% 0402 X5R
PWR_1.8VSUS 10,12,14,17,18,44,45
U21H
Crestline FBGA 1299P INTEL
6019B0360601
CRT
PLL
LVDS
PEG
SM
CK
TV
TV/CRT
POWER
VTT
AXD
AXF
SM CK
HV
PEG
DMI
VTTLF
7,8,10,11,14,19,22,44,48,54 PWR_1.05VMAIN
4.7uF 25V 10% 0805 X5R
4.7uF 25V 10% 0805 X5R
2.2uF 10V 10% 0805 X5R
0.47uF 16V 10% 0603 X7R
T220uF 2.5V 35m 20% 3528
PLACE ON THE EDGE
1.25VM_AXD
L22 120OHM-25%-200mA-0603-0.2OHM
C261 1uF 6.3V 10% 0402 X5R
C257 10uF 6.3V 10% 0805 X5R
C163 1uF 6.3V 10% 0402 X5R
C247 10uF 6.3V 10% 0805 X5R
PWR_1.25VMAIN 12,22,41,44
C159 0.1uF 10V 10% 0402 X7R
L20 120OHM-25%-200mA-0603-0.2OHM
PWR_1.8VSUS 10,12,14,17,18,44,45
C256 10uF 6.3V 10% 0805 X5R
C250
1.8V_TXLVDS
L50 120ohm 25% 200mA 0603(BLM11A121S)
C563 1000pF 50V 10% 0402 X7R
C552 T220uF 2.5V 35m 20% 3528
3VS_HV
VCC_PEG
100ohm 25% 2A 0.1ohm 0603_NU
L47
L46 100ohm 25% 2A 0.1ohm 0603
PWR_1.05VMAIN 7,8,10,11,14,19,22,44
C542 10uF 6.3V 10% 0805 X5R
T220uF 2.5V 35m 20% 3528
C541
VCC_DMI
VTTLF_CAP1
VTTLF_CAP2
VTTLF_CAP3
C537 10uF 6.3V 10% 0805 X5R
C540 T220uF 2.5V 35m 20% 3528
L43 100ohm 25% 2A 0.1ohm 0603_NU
L48 100ohm 25% 2A 0.1ohm 0603
C282 0.47uF 16V 10% 0603 X7R
C281 0.47uF 16V 10% 0603 X7R
C279 0.47uF 16V 10% 0603 X7R
PWR_3VMAIN
10-5%-1/10W-0603 R479
D31 BAT54C-7 30V 200MA SOT23
R486 SHORT-0402-15MIL
3VS_HV
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Title
J11Eagle(Merom+Crestline+ICH8M)
Size C
Document Number
Crestline Power(5/6)*
Rev 0.4
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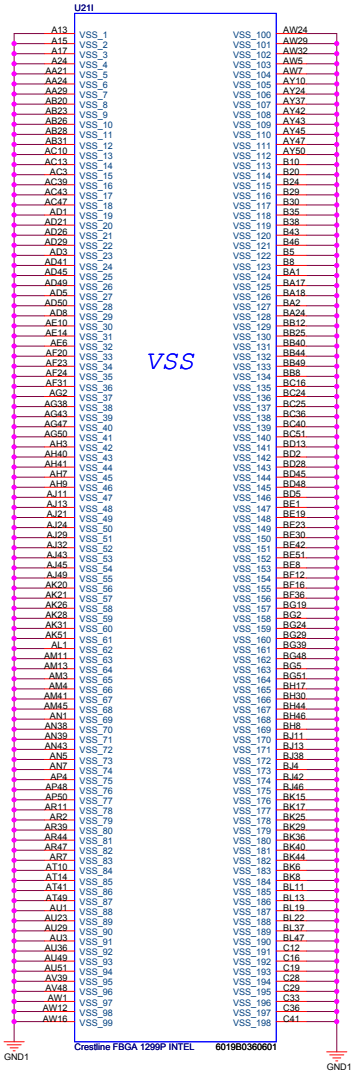
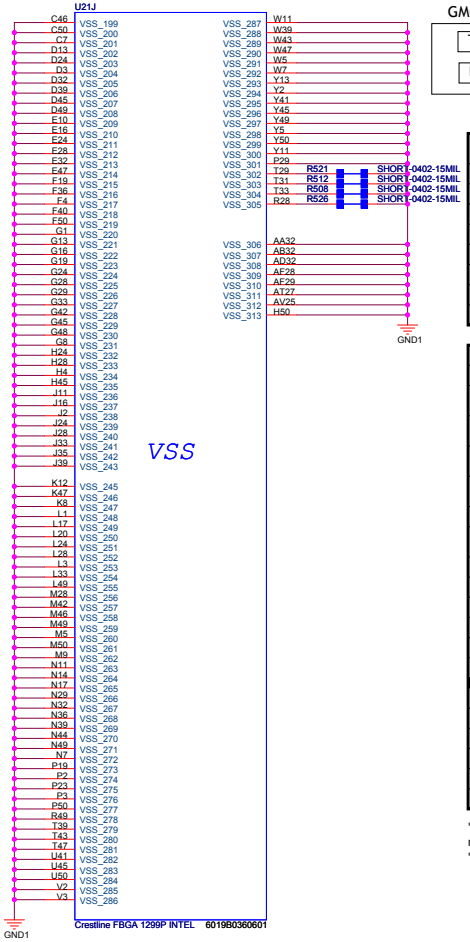
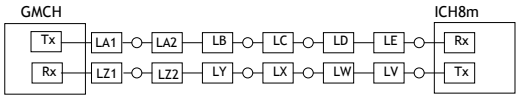




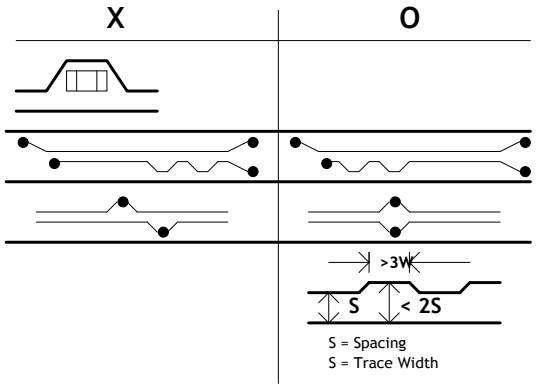
DMI Routing Guideline



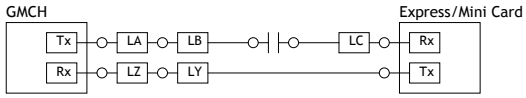
Breakout/in LA/LZ	Main Route LB/LY		Breakout/in LE/LV
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Microstrip	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Stripline
Stripline	Same Routing layer as LA/LZ	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Didderential Pair-Pitch	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 22 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (GMCH Breakout)	Max = 250 mils	
Trace Length-LB (GMCH Breakout to Via2)	Max = 3600 mils	
Trace Length-LC (Via2 to Via3)	Max = 5900 mils	
Trace Length-LD (Via3 to ICH7m Breakout)	Max = 3600 mils	
Trace Length-LE (ICH7m Breakout)	Max = 400 mils	
Trace Length-L1 (LA+LB+LC+LD+LE)	Max = 8000 mils	
Trace Length-LV (ICH7m Breakout)	Max = 400 mils	
Trace Length-LW (ICH7m Breakout to Via2)	Max = 3600 mils	
Trace Length-LX (Via2 to Via3)	Max = 5900 mils	
Trace Length-LY (Via3 to GMCH Breakout)	Max = 3600 mils	
Trace Length-LZ (GMCH Breakout)	Max = 400 mils	
Trace Length-L2 (LV+LW+LX+LY+LZ)	Max = 8000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



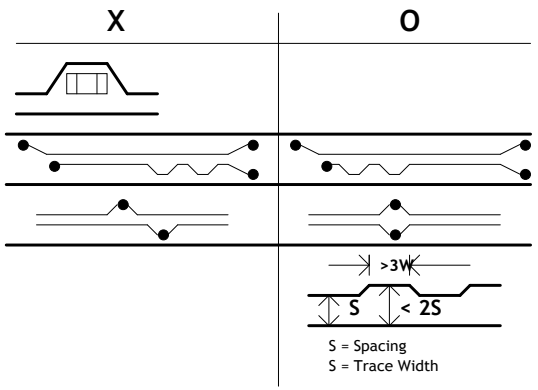
PCIE Routing Guideline



Breakout/in LA/LZ	Main Route LB/LC/LY	Main Route LD/LW	Breakout/in LE/LV
Stripline	Microstrip	Same Routing layer as LE/LV	Microstrip

Parameter	Main Route Guideline	Breakout Guideline
Uncoupled Single End Impedance	55 +/- 15%	55 +/- 15%
Nominal Trace Width	Inner Layer : 4 mils Outer Layer : 5 mils	
Nominal Differential Trace Space	Inner Layer : 7 mils Outer Layer : 7 mils	Inner Layer : 4 mils Outer Layer : 5 mils
Pair-to-Pair Pitch	Inner Layer : 37 mils Outer Layer : 37 mils	Inner Layer : 27 mils Outer Layer : 27 mils
Bus-to-Bus Pitch	Inner Layer : 20 mils Outer Layer : 20 mils	Inner Layer : 15 mils Outer Layer : 12 mils
Reference Plane	Ground	Ground
Splits/Voids	No routing over plane splits No routing over voids	
Trace Length-LA (ICH7m Breakout)	Max = 400 mils	
Trace Length-LB (ICH7m Breakout to AC cap)	Max = 10750 mils	
Trace Length-LC (AC cap to PCIe CN)	Max = 10750 mils	
Trace Length-L1 (LA+LB+LC)	Max = 12000 mils	
Trace Length-LY (PCIe CN to ICH7m Breakout)	Max = 11950 mils	
Trace Length-LZ (ICH7m Breakout)	Max = 400 mils	
Trace Length-L2 (LY+LZ)	Max = 12000 mils	

*** When routing near the edge of their reference plane , trace should maintain at least 40 mils space to the edge of the plane
*** Match the trace lengths of the complementary signals within each differential pair to +/- 5 mils



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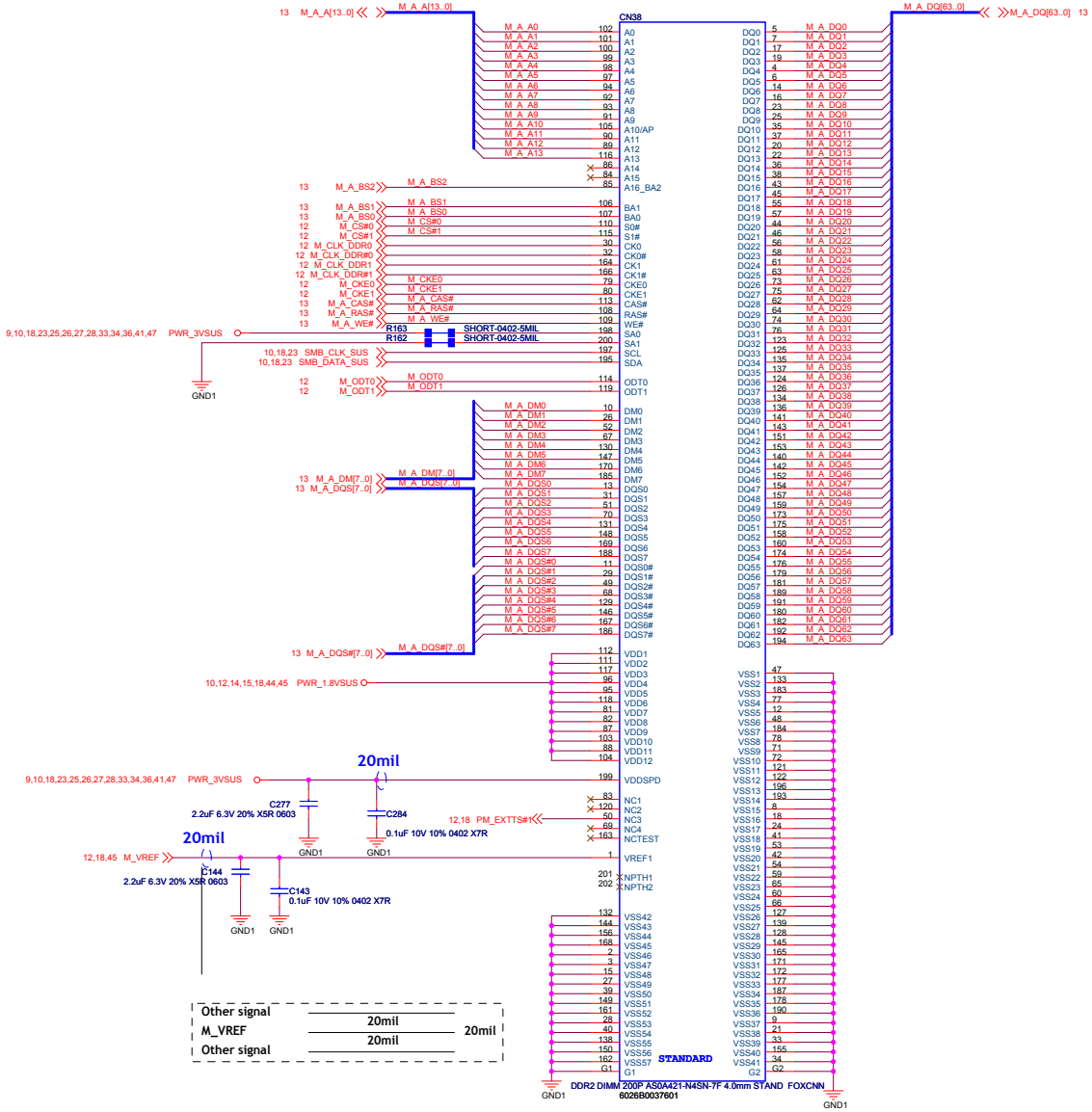
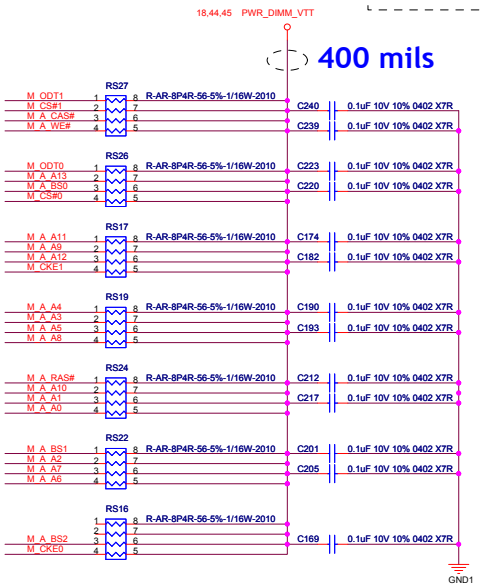
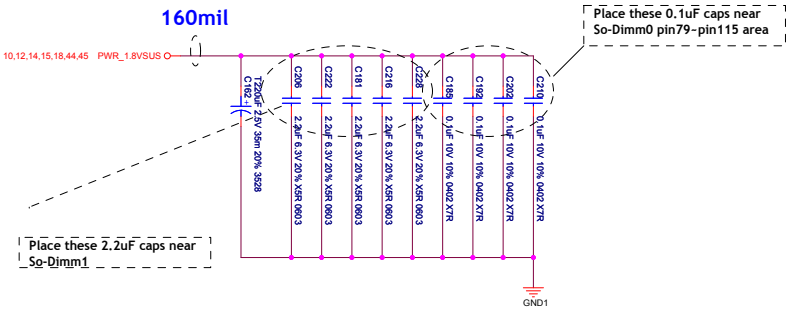
Size: C | Document Number: Crestline Ground(6/6) | Rev: 0.4
Date: Monday, April 09, 2007 | Sheet 16 of 55

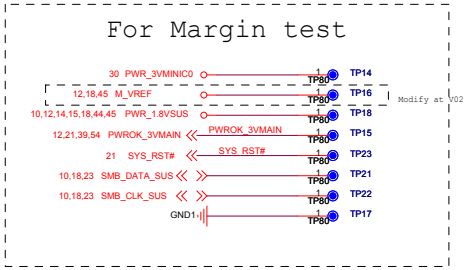
SO-DIMM0



Place one cap close to every 2 pullup resistors terminated to 0.9VDDT_DDRII







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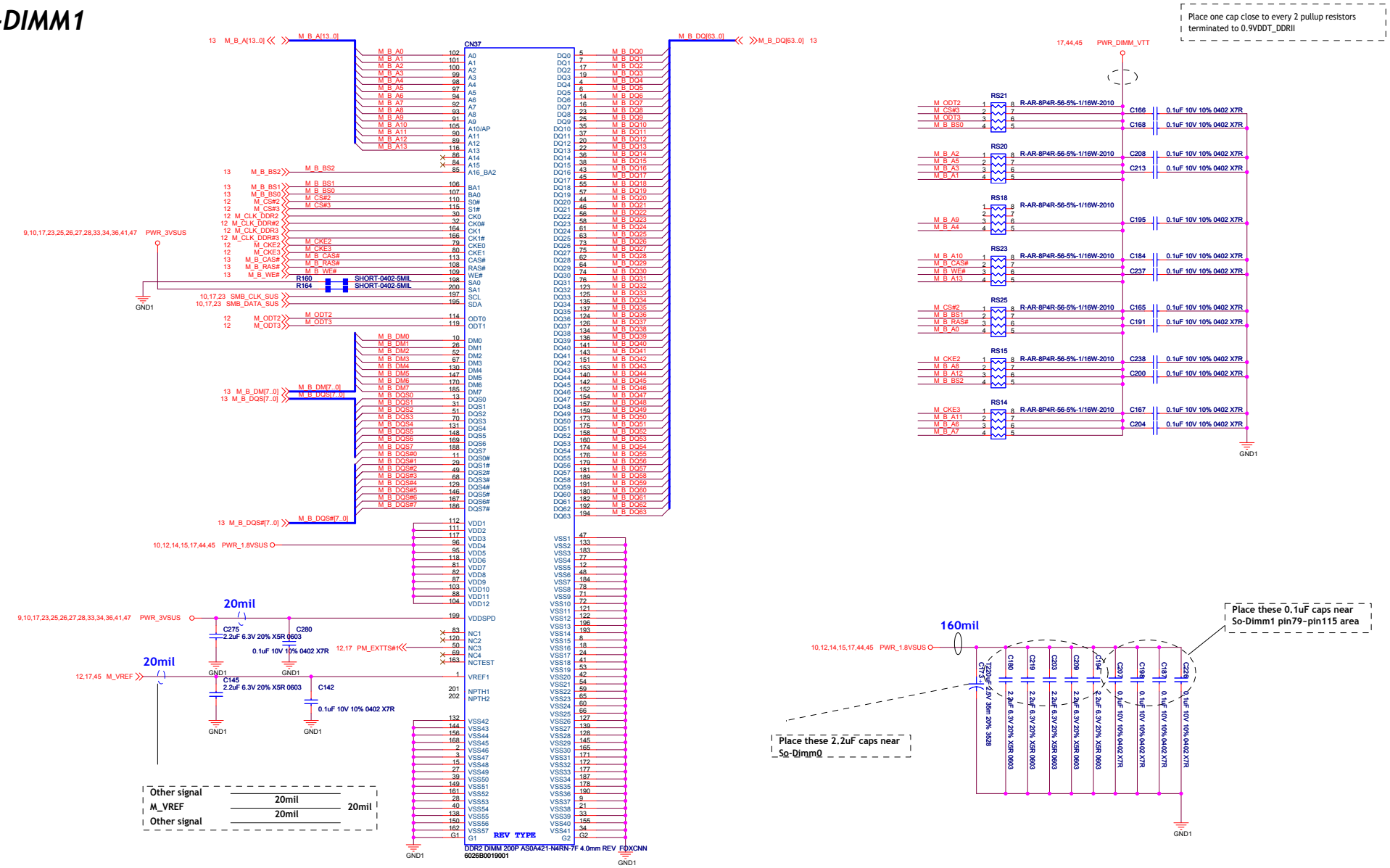
Size: C | Document Number: DDR2 SDRAM SO-DIMM0 | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 17 of 55

SO-DIMM1



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Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: DDR2 SDRAM SO-DIMM1 | Rev: 0.4

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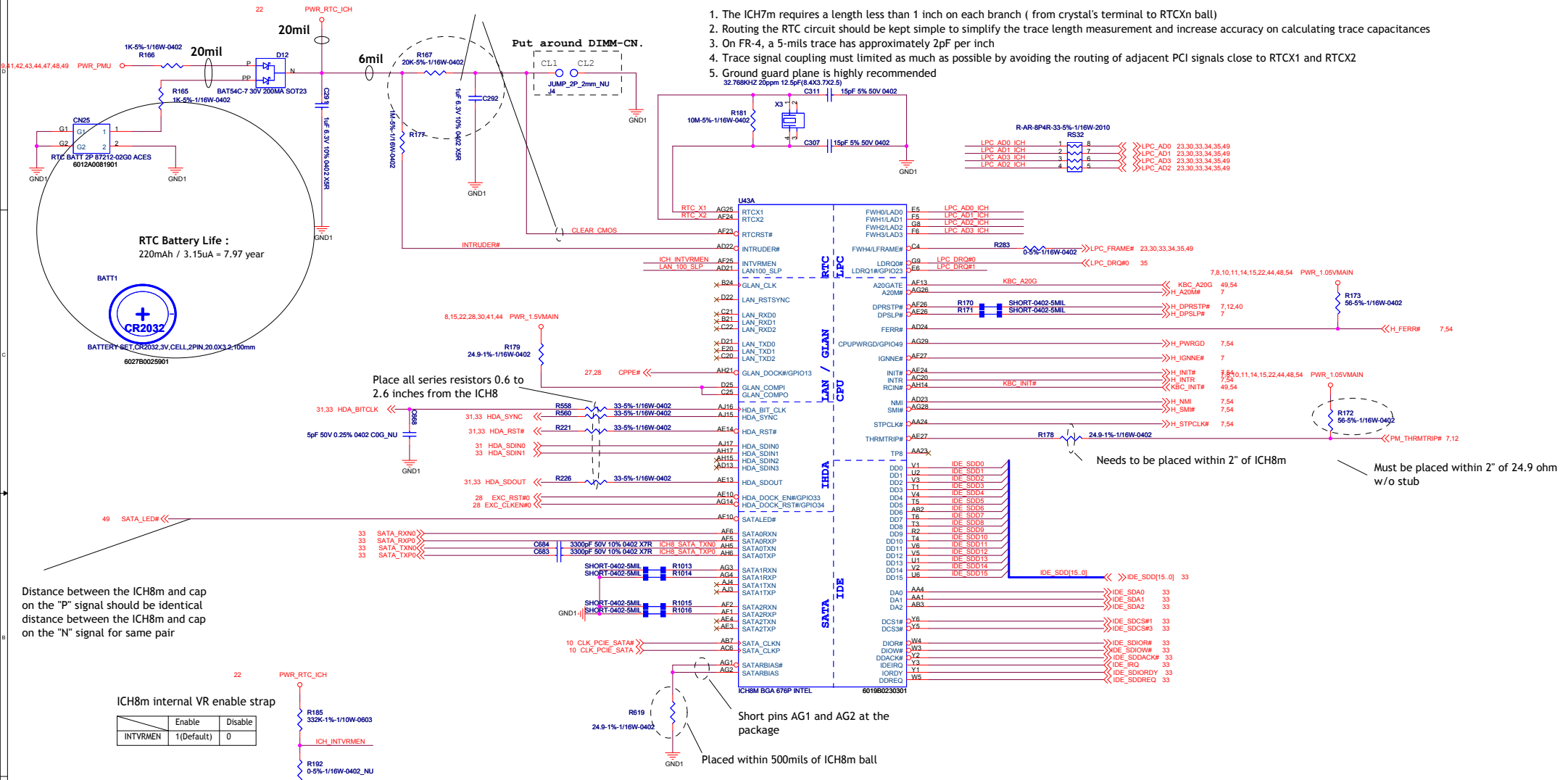
RTC Circuit

1. RC delay time should be in the range of 18~25ms
2. It is recommended that this larger capacitor and small resistor value in order to reduce the likelihood of glitching of RTCRST#

1. The ICH7m requires a length less than 1 inch on each branch (from crystal's terminal to RTCXn ball)
2. Routing the RTC circuit should be kept simple to simplify the trace length measurement and increase accuracy on calculating trace capacitances
3. On FR-4, a 5-mils trace has approximately 2pF per inch
4. Trace signal coupling must limited as much as possible by avoiding the routing of adjacent PCI signals close to RTCX1 and RTCX2
5. Ground guard plane is highly recommended



	Enable	Disable
INTVRMEN	1(Default)	0

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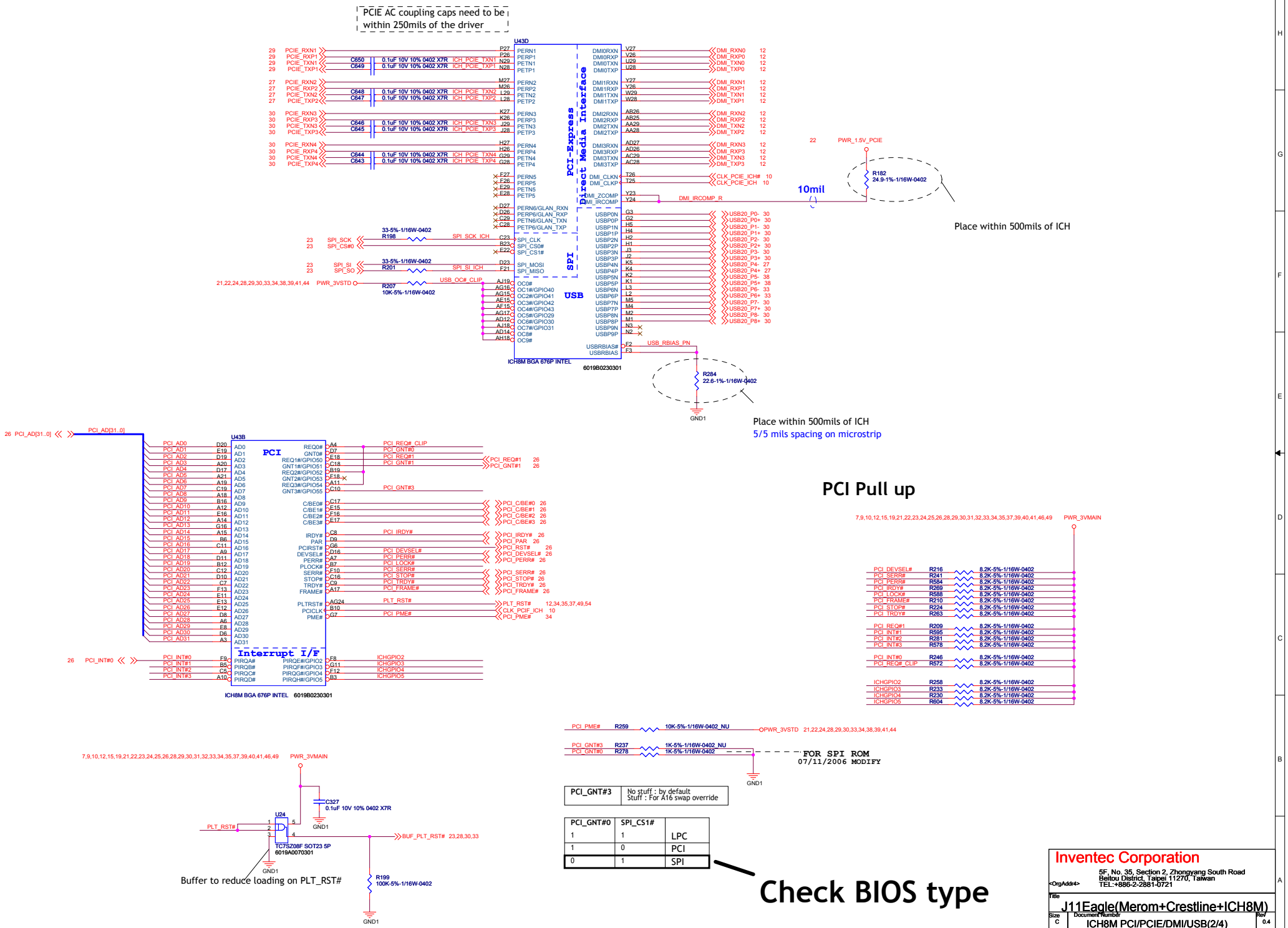
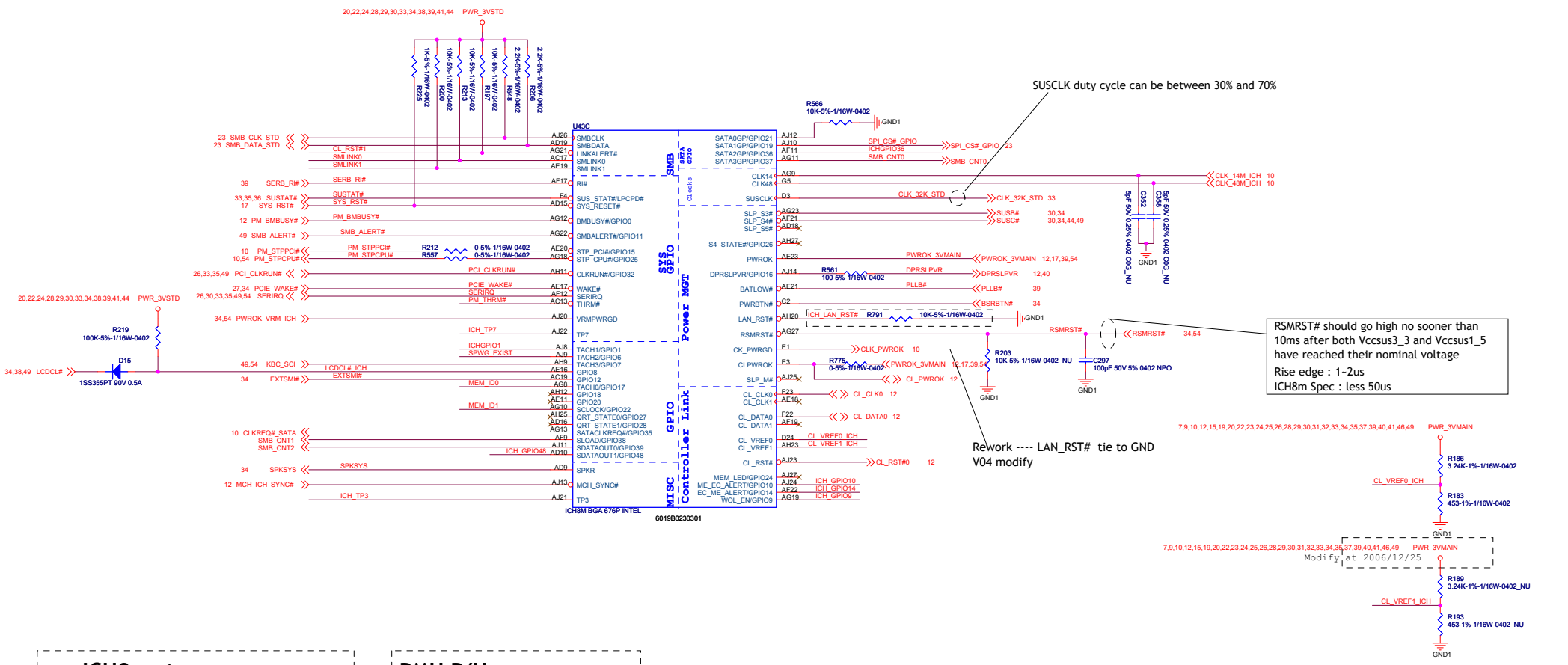
Size: C | Document Number: ICH8M CPU/IDE/SATA(1/4) | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 19 of 55



PCI_GNT#3	No stuff : by default Stuff : For A16 swap override

PCI_GNT#0	SPI_CS1#	
1	1	LPC
1	0	PCI
0	1	SPI



ICH8m strap

ACZ_SPKR	No stuff : by default Stuff : For NO reboot

SPKSYS R249 1K-5%-1/16W-0402_NU

Stuff for XOR chain testing

ICH_TP3 R555 1K-5%-1/16W-0402_NU

PMU P/U

EXTSMI#	R196	10K-5%-1/16W-0402
PLLB#	R91	8.2K-5%-1/16W-0402
PCIE_WAKE#	R217	1K-5%-1/16W-0402
SMB_ALERT#	R194	10K-5%-1/16W-0402
SERB_RI#	R208	10K-5%-1/16W-0402
PM_THRM#	R234	8.2K-5%-1/16W-0402
PCI_CLKRUN#	R568	8.2K-5%-1/16W-0402
ICHGPIO1	R589	10K-5%-1/16W-0402
PM_STPPCI#	R211	10K-5%-1/16W-0402_NU
PM_STPCPU#	R556	10K-5%-1/16W-0402_NU
SERIRQ	R245	10K-5%-1/16W-0402
SPWG_EXIST	R579	10K-5%-1/16W-0402
MEM_ID0	R596	10K-5%-1/16W-0402
MEM_ID1	R573	10K-5%-1/16W-0402
ICH_GPIO48	R257	10K-5%-1/16W-0402
ICH_TP7	R551	1K-5%-1/16W-0402_NU
ICHGPIO36	R242	10K-5%-1/16W-0402
DPRSLPVR	R562	100K-5%-1/16W-0402
ICH_GPIO10	R550	10K-5%-1/16W-0402
ICH_GPIO14	R188	10K-5%-1/16W-0402
ICH_GPIO9	R204	100K-5%-1/16W-0402
PWROK_3VMAIN	R572	10K-5%-1/16W-0402
PWROK_VRM_ICH	R78	100K-5%-1/16W-0402
SMB_CNT0	R755	10K-5%-1/16W-0402
SMB_CNT1	R756	10K-5%-1/16W-0402
SMB_CNT2	R757	10K-5%-1/16W-0402

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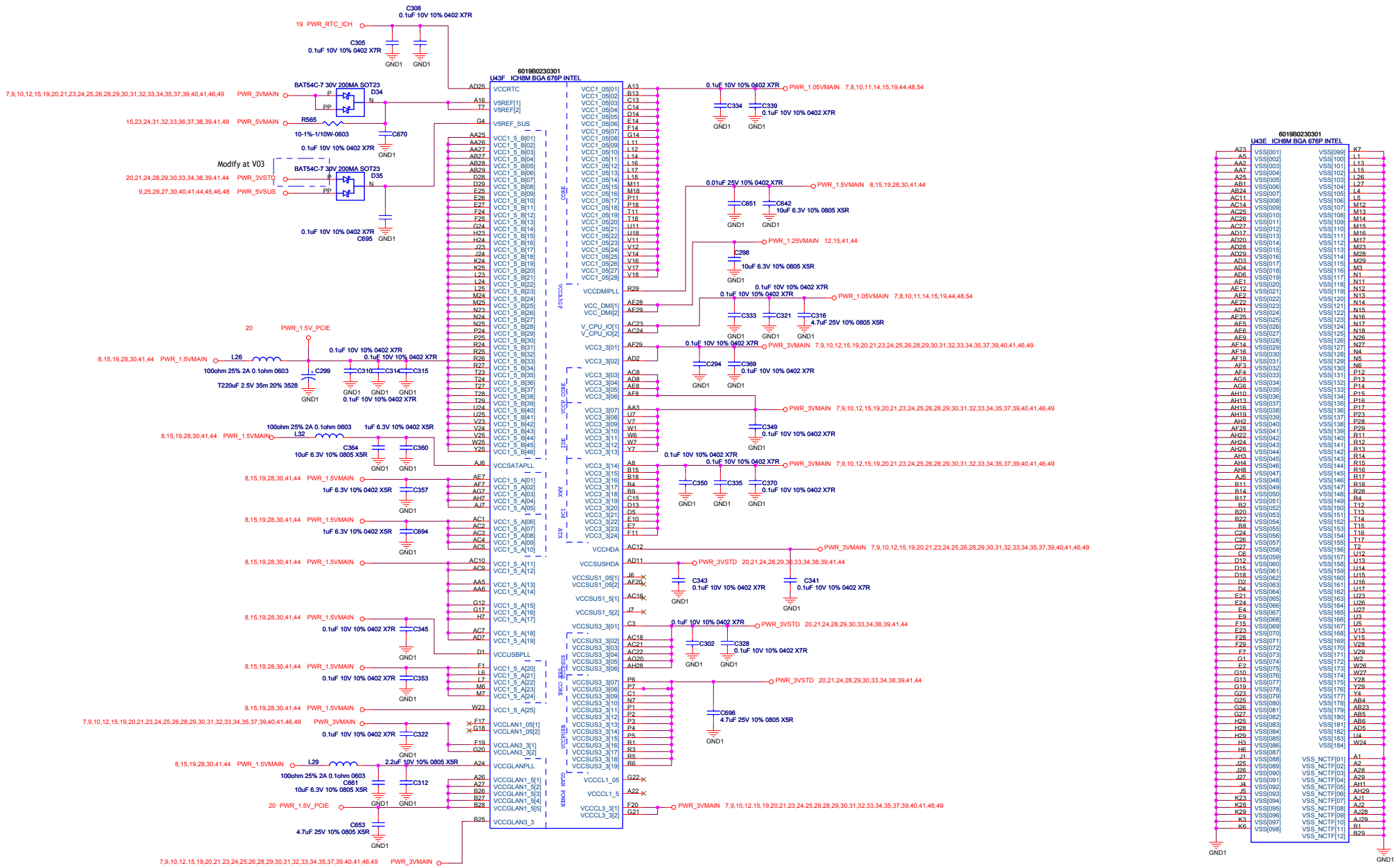
Size: C | Document Number: ICH8M GPIO(3/4) | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 21 of 55



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Title: J11Eagle(Merom+Crestline+ICH8M)

Size: Custom | Document Number: ICH8M Power/GND(4/4) | Rev: 0.4

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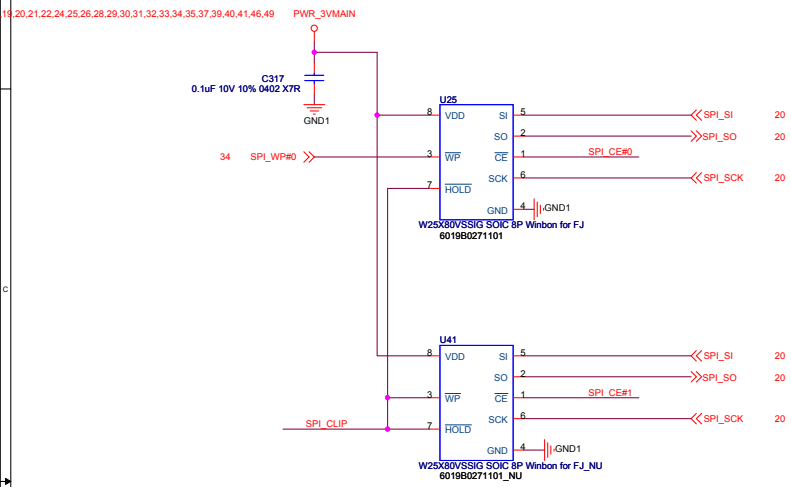
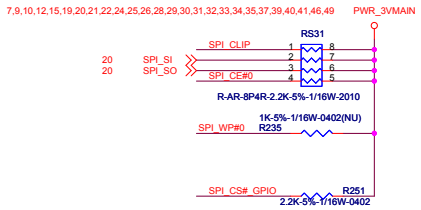
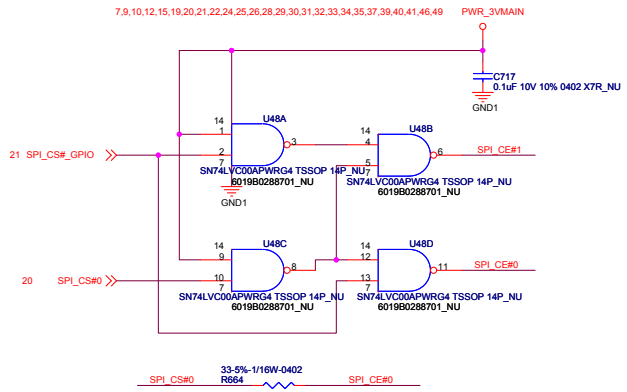
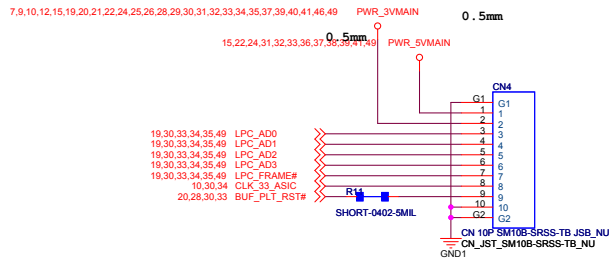
Delete at 2006/12/20

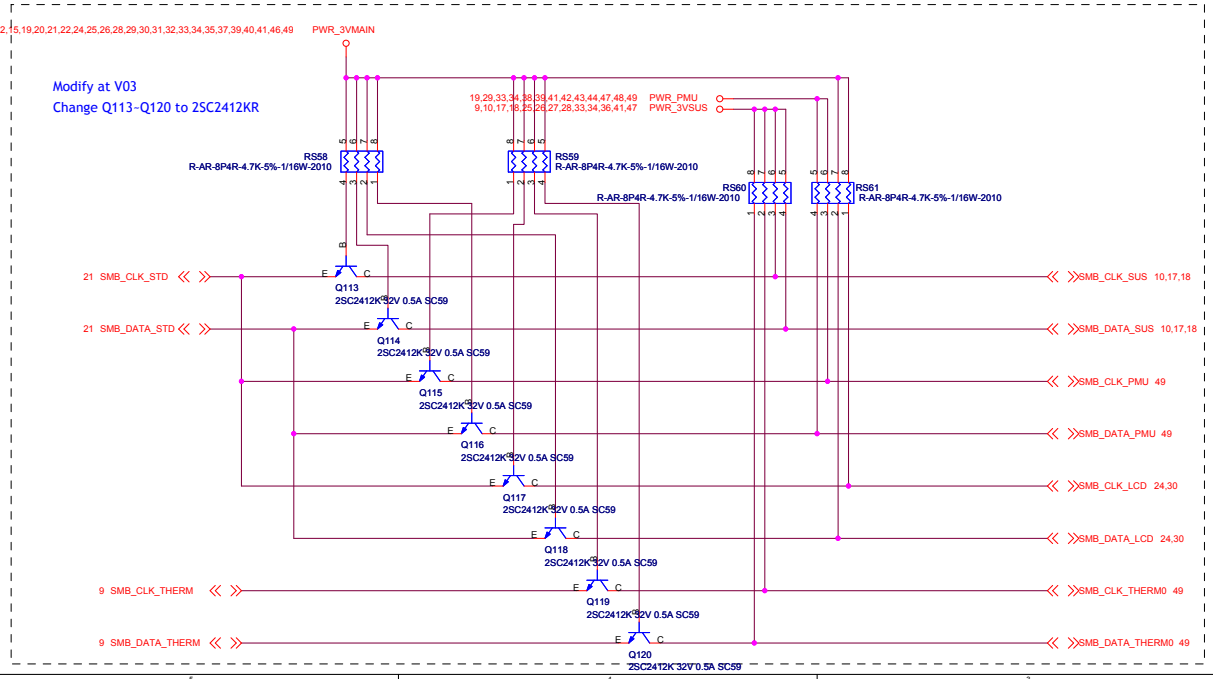








PORT80



Device	Hex	Address
ADT7473	5Ch	0101 110x b
MEM slot0	A2h	1010 000x b
MEM slot1	A4h	1010 010x b
PMU	32h	0011 001x b
LCD(SPWG)	A0h	1010 000x b
JEPICO	90h	1001 000x b

SMBCNT[2:0]	Device
0,0,0	DIMM SLOT 0/1,CLK GEN.
0,0,1	EC control
0,1,0	EC control,ADT7473
0,1,1	LCD(SPWG),MiniCard

CBT3253 NPUTS FUNCTION
OE S1 S0 FUNCTION
L L L A port = B1 port
L L H A port = B2 port
L H L A port = B3 port
L H H A port = B4 port
H X X Disconnect

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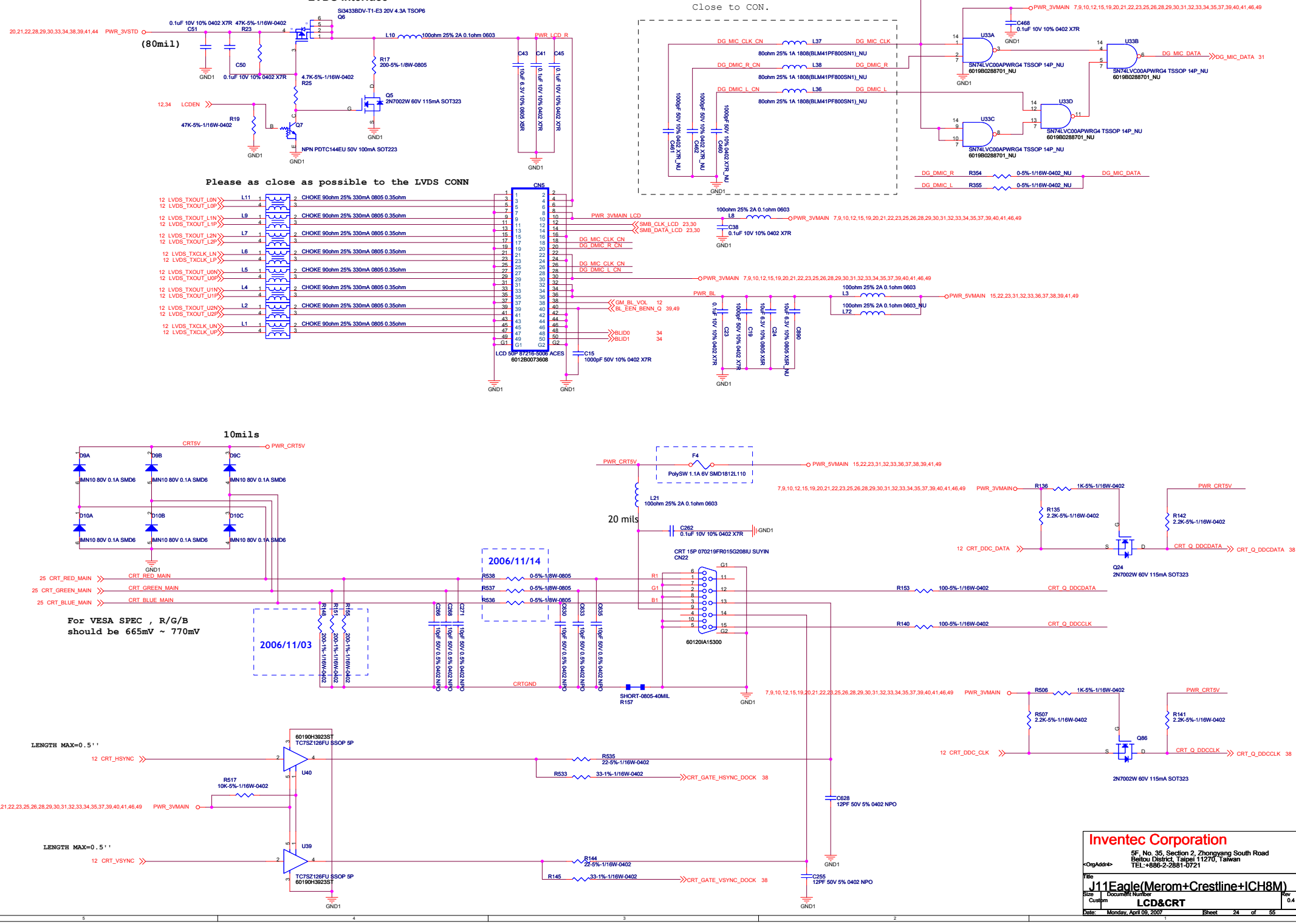
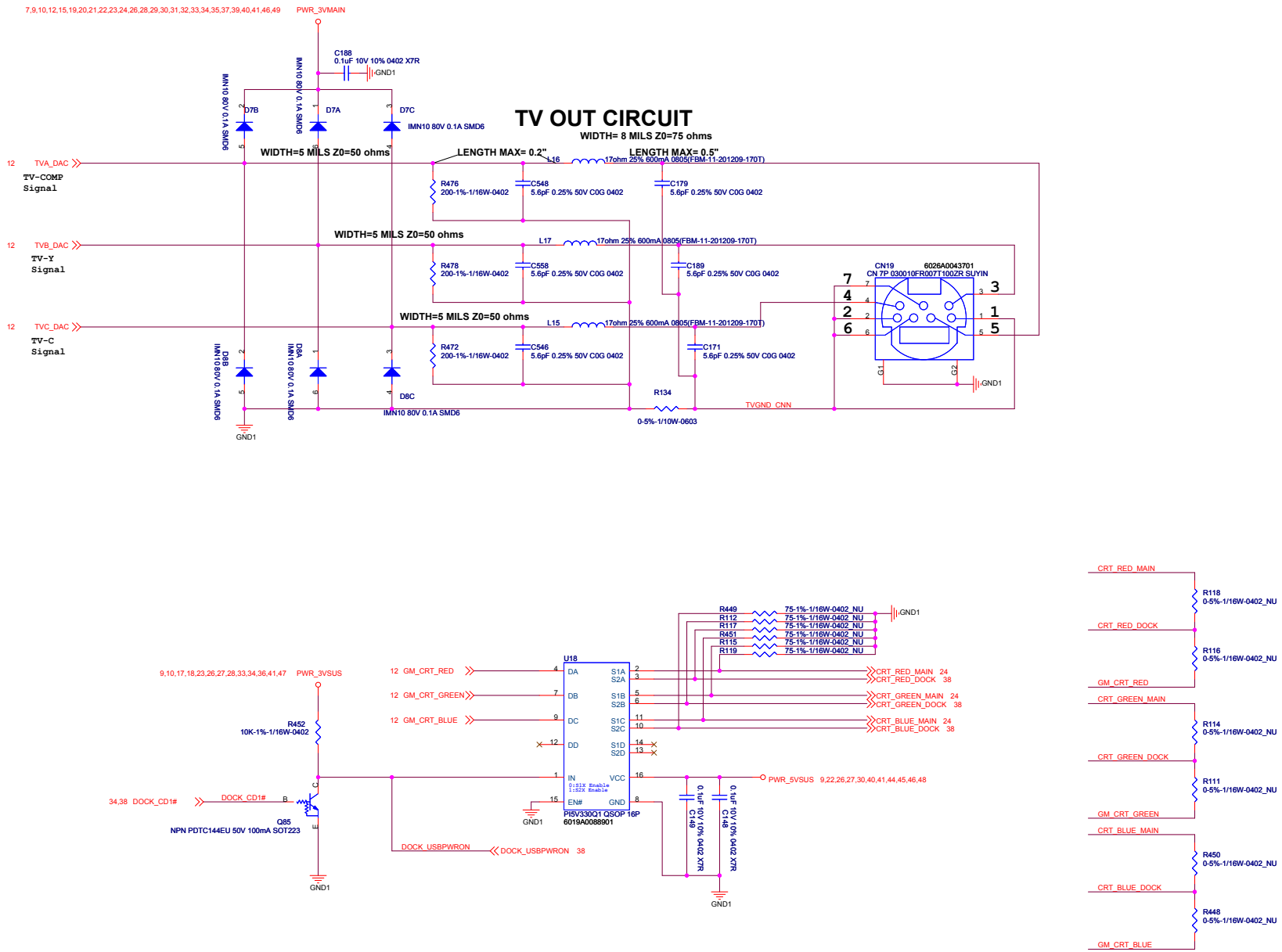
Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: BIOS/SMBUS_SW/80 PORT | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 23 of 55

LVDS Interface





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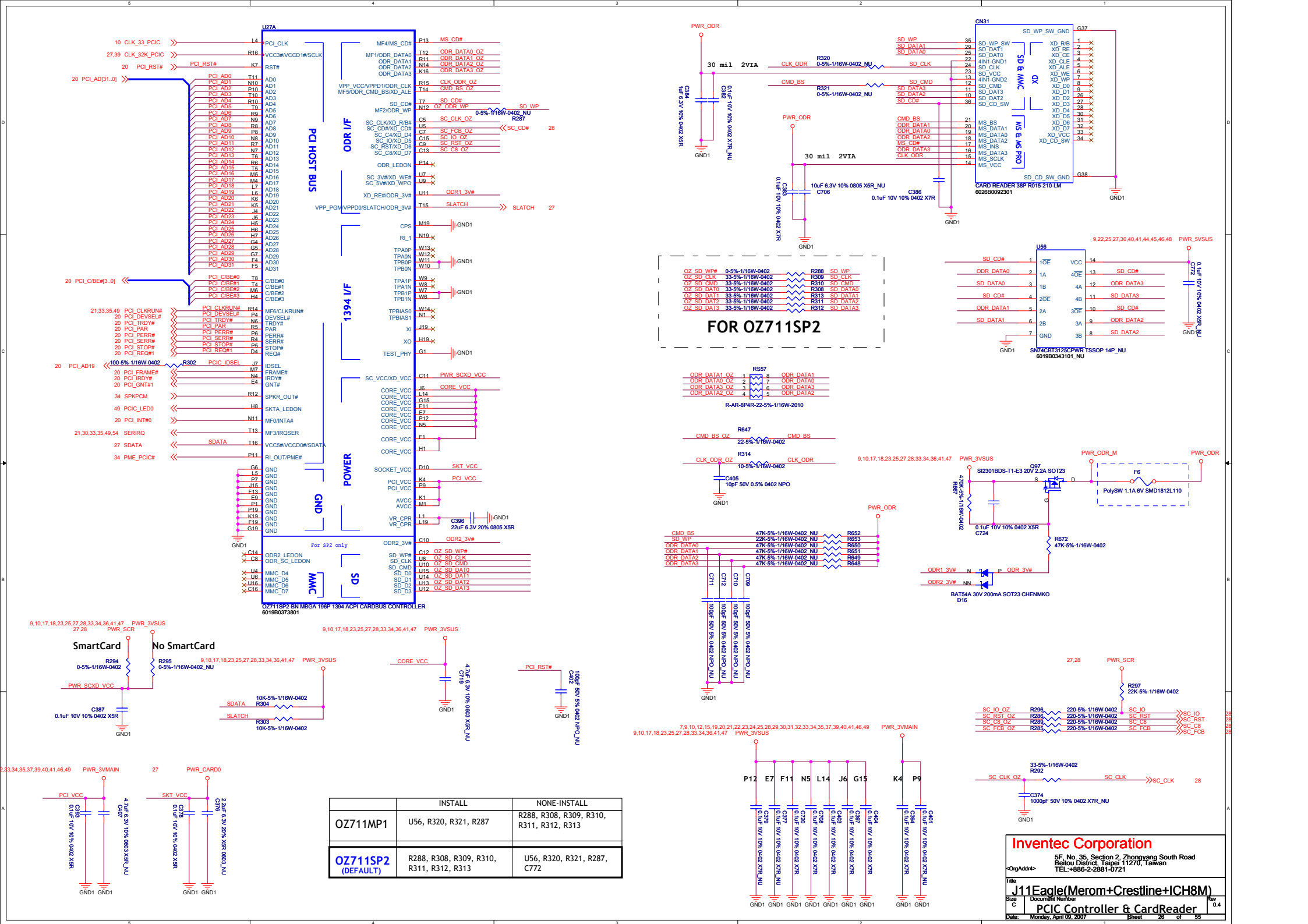
Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: TV OUT & CRT SW | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 25 of 55



	INSTALL	NONE-INSTALL
OZ711MP1	U56, R320, R321, R287	R288, R308, R309, R310, R311, R312, R313
OZ711SP2 (DEFAULT)	R288, R308, R309, R310, R311, R312, R313	U56, R320, R321, R287, C772

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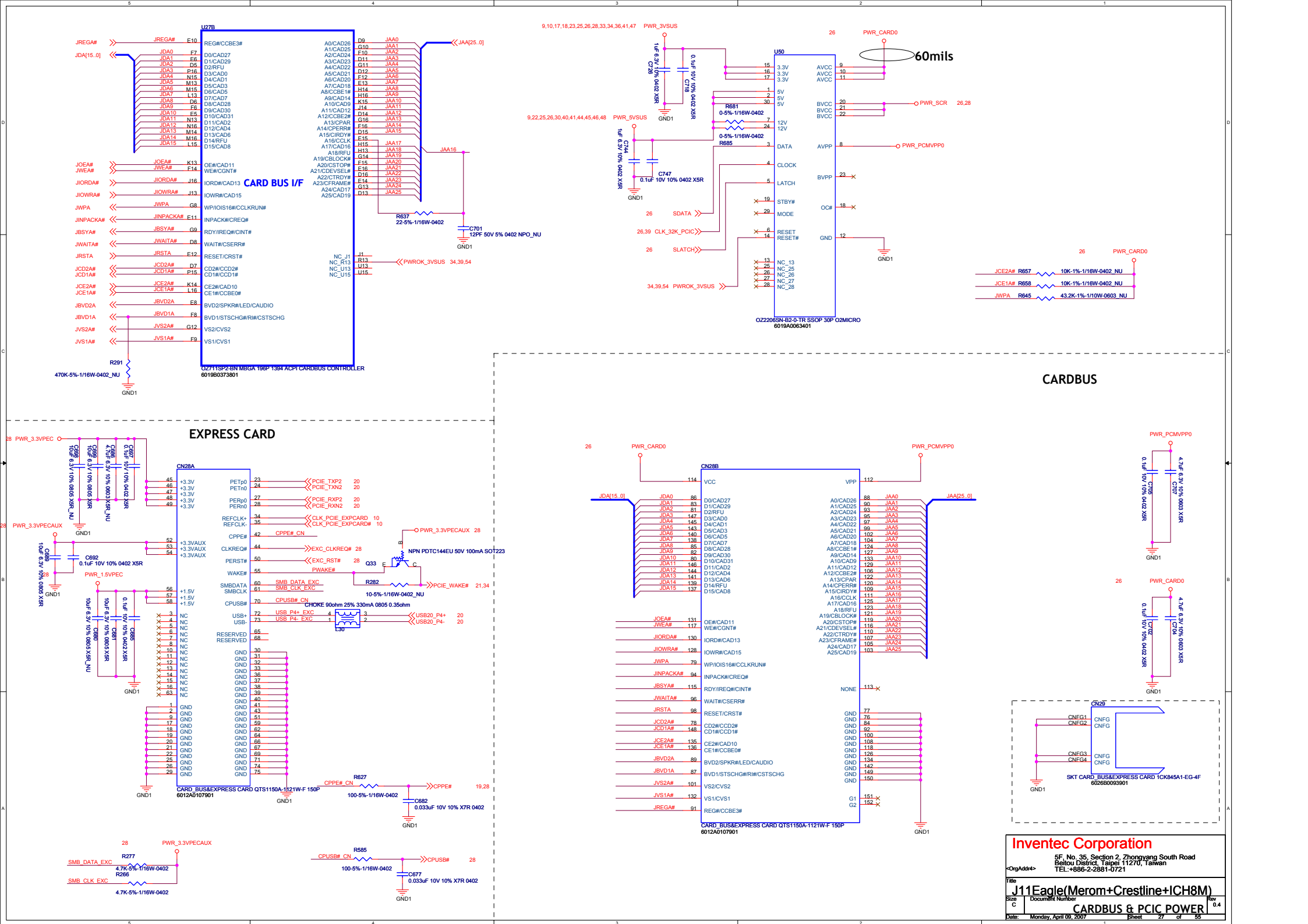
Size: C | Document Number: PCIC Controller & CardReader | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 26 of 55


CARDBUS
CARD BUS I/F
U27B
OZ711SP2-BN MBGA 196P 1394 ACPI CARDBUS CONTROLLER
6019B0373801
U50
OZ2206SN-B2-0-TR SSOP 30P O2MICRO
6019A0063401
60mils
EXPRESS CARD
CN28A
CARD_BUS&EXPRESS CARD QTS1150A-1121W-F 150P
6012A0107901
CN28B
CARD_BUS&EXPRESS CARD QTS1150A-1121W-F 150P
6012A0107901
CN29
SKT CARD_BUS&EXPRESS CARD 1CK845A1-EG-4F
6026B0093901
NPN PDTC144EU 50V 100mA SOT223
CHOKE 90ohm 25% 330mA 0805 0.35ohm
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 112701, Taiwan
TEL:+886-2-2881-0721
Title
J11Eagle(Merom+Crestline+ICH8M)
Size C
Document Number
CARDBUS & PCIC POWER
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Date: Monday, April 09, 2007
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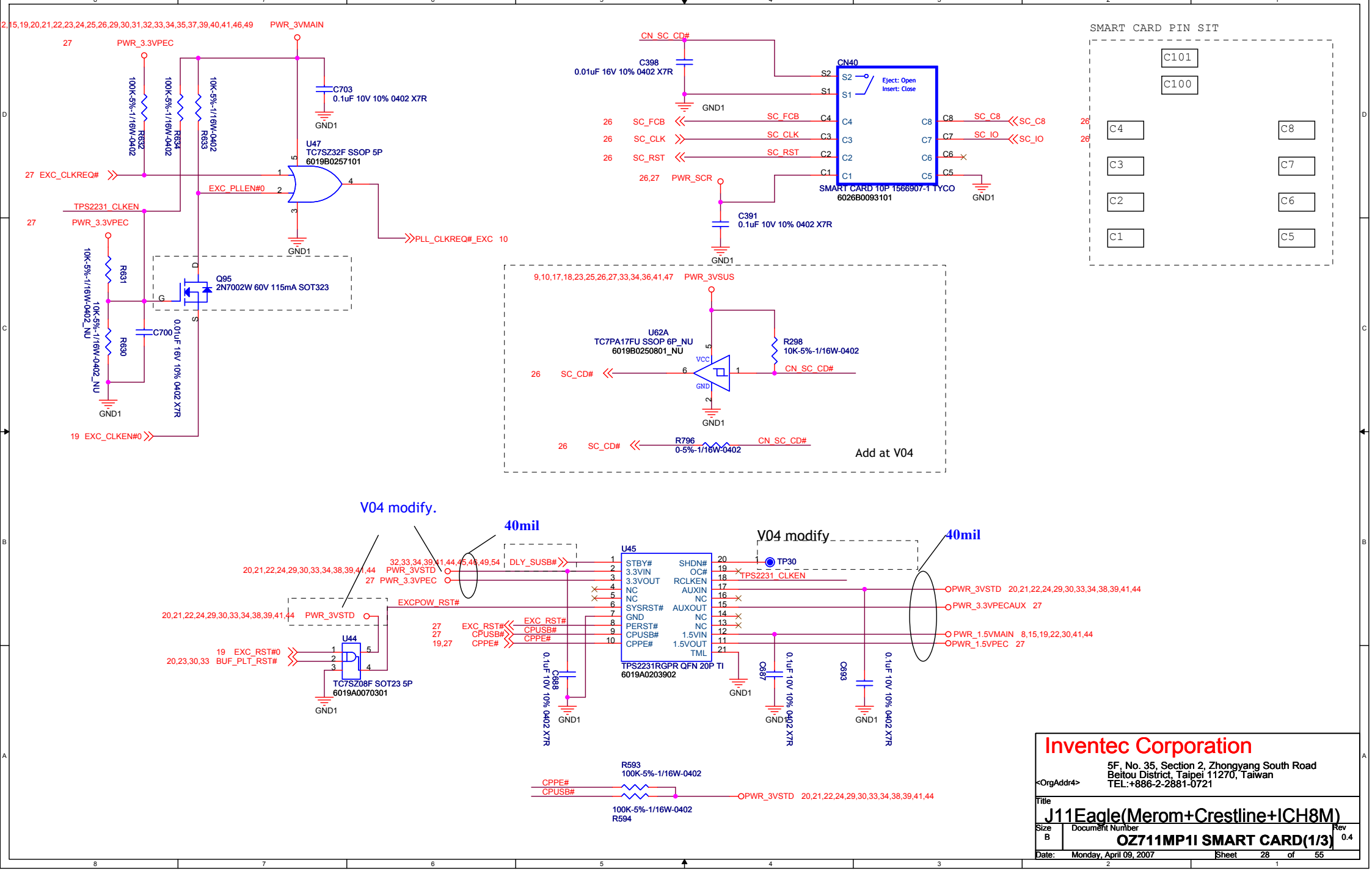

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Size: B | Document Number: OZ711MP1I SMART CARD(1/3) | Rev: 0.4

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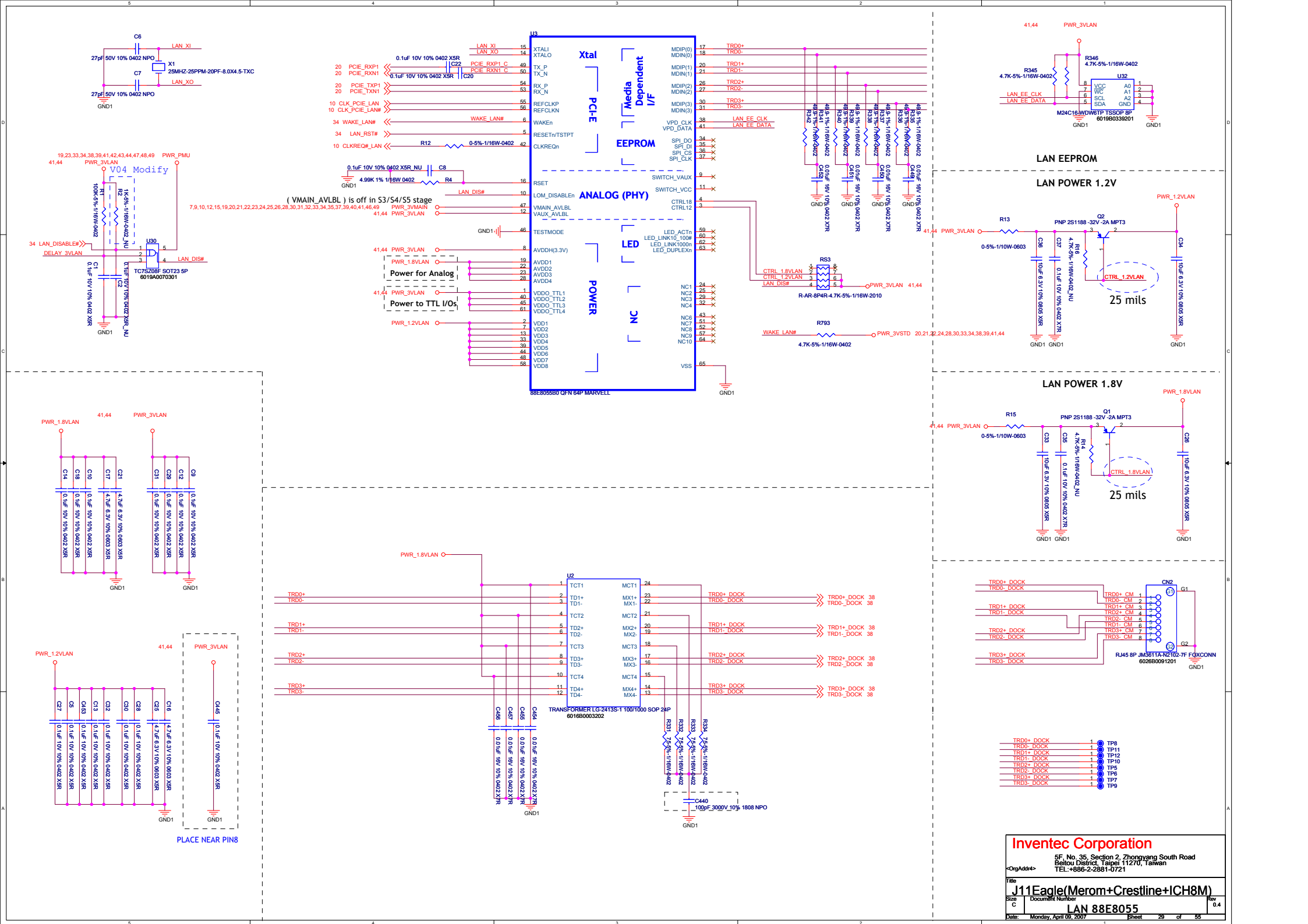
U3
88E8055B0 QFN 64P MARVELL
Xtal
PCI-E
Media Dependent I/F
EEPROM
ANALOG (PHY)
LED
POWER
NC
(VMAIN_AVLBL) is off in S3/S4/S5 stage
Power for Analog
Power to TTL I/Os
LAN EEPROM
LAN POWER 1.2V
LAN POWER 1.8V
25 mils
U2
TRANSFORMER LG-2413S-1 100/1000 SOP 24P
6016B0003202
CN2
RJ45 8P JM3611A-N2102-7F FOXCONN
6026B0091201
PLACE NEAR PIN8
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
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J11Eagle(Merom+Crestline+ICH8M)
LAN 88E8055
Monday, April 09, 2007
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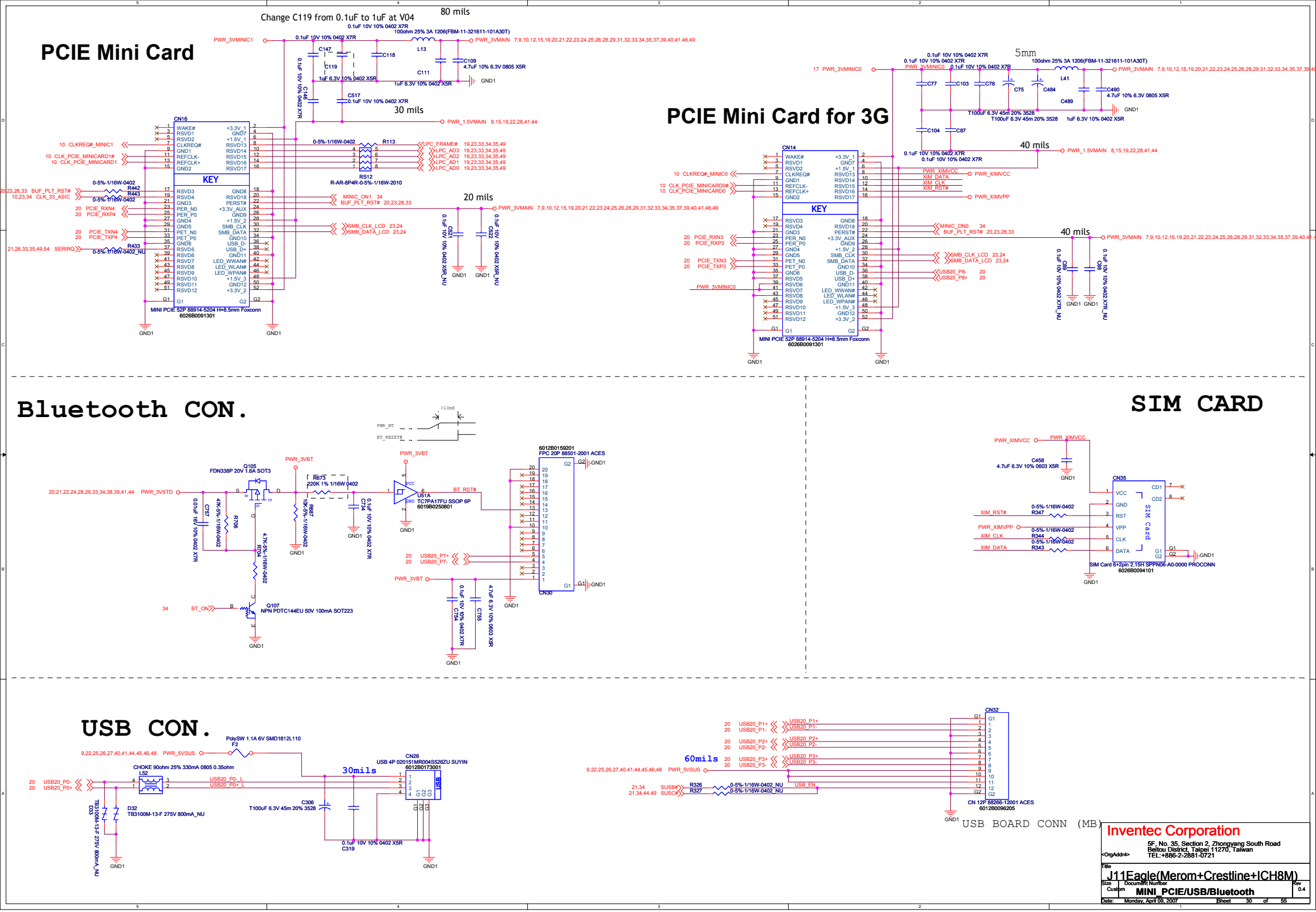

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Size: Custom | Document Number: MINI_PCIE/USB/Bluetooth | Rev: 0.4

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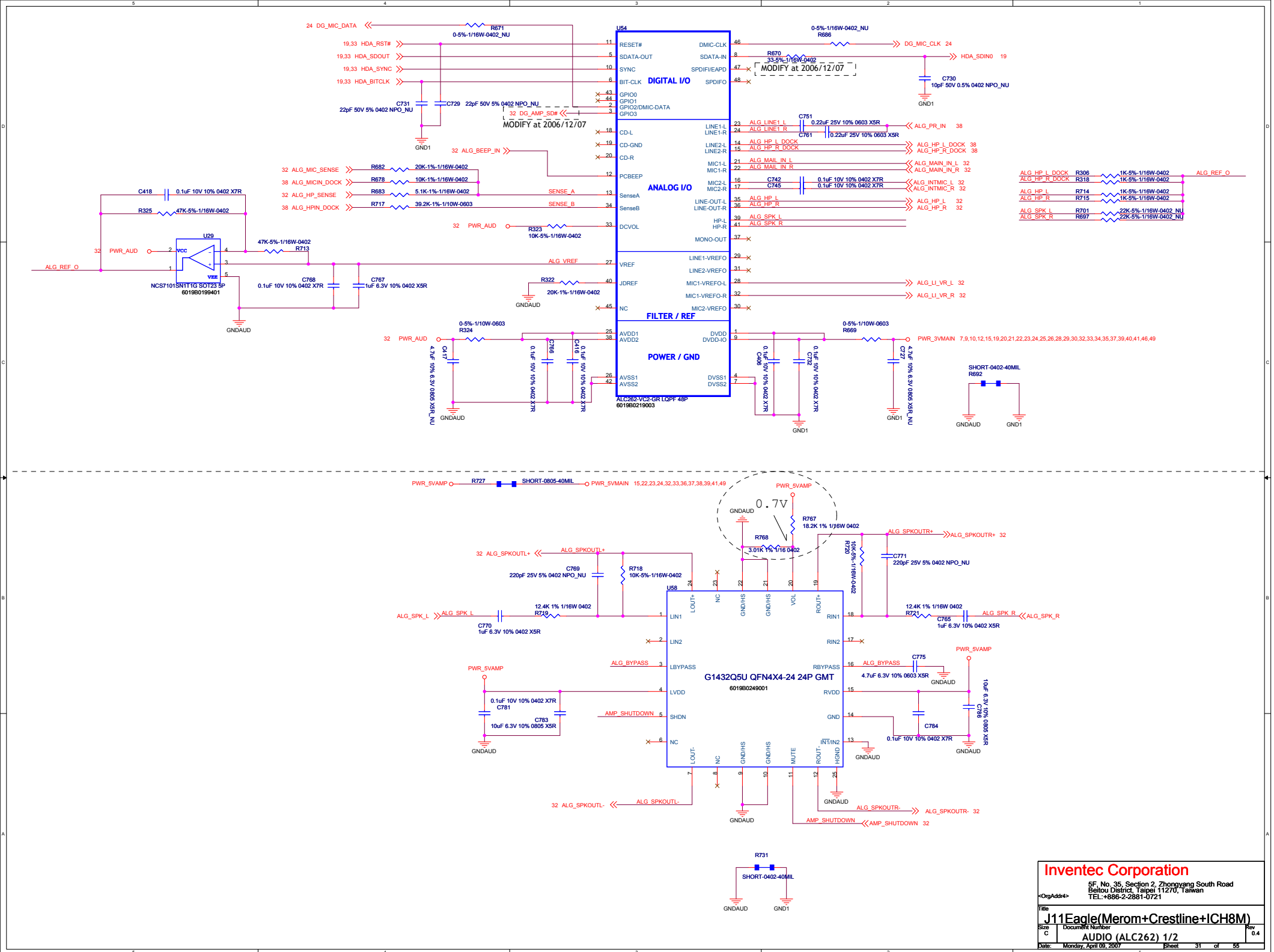
U54
DIGITAL I/O
ANALOG I/O
FILTER / REF
POWER / GND
ALC262-VC2-GR LQFP 48P
6019B0219003
MODIFY at 2006/12/07
U29
NCS7101SN1T1G SOT23 5P
6019B0199401
U58
G1432Q5U QFN4X4-24 24P GMT
6019B0249001
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 112?0, Taiwan
TEL:+886-2-2881-0721
Title
J11Eagle(Merom+Crestline+ICH8M)
AUDIO (ALC262) 1/2
Size C
Rev 0.4
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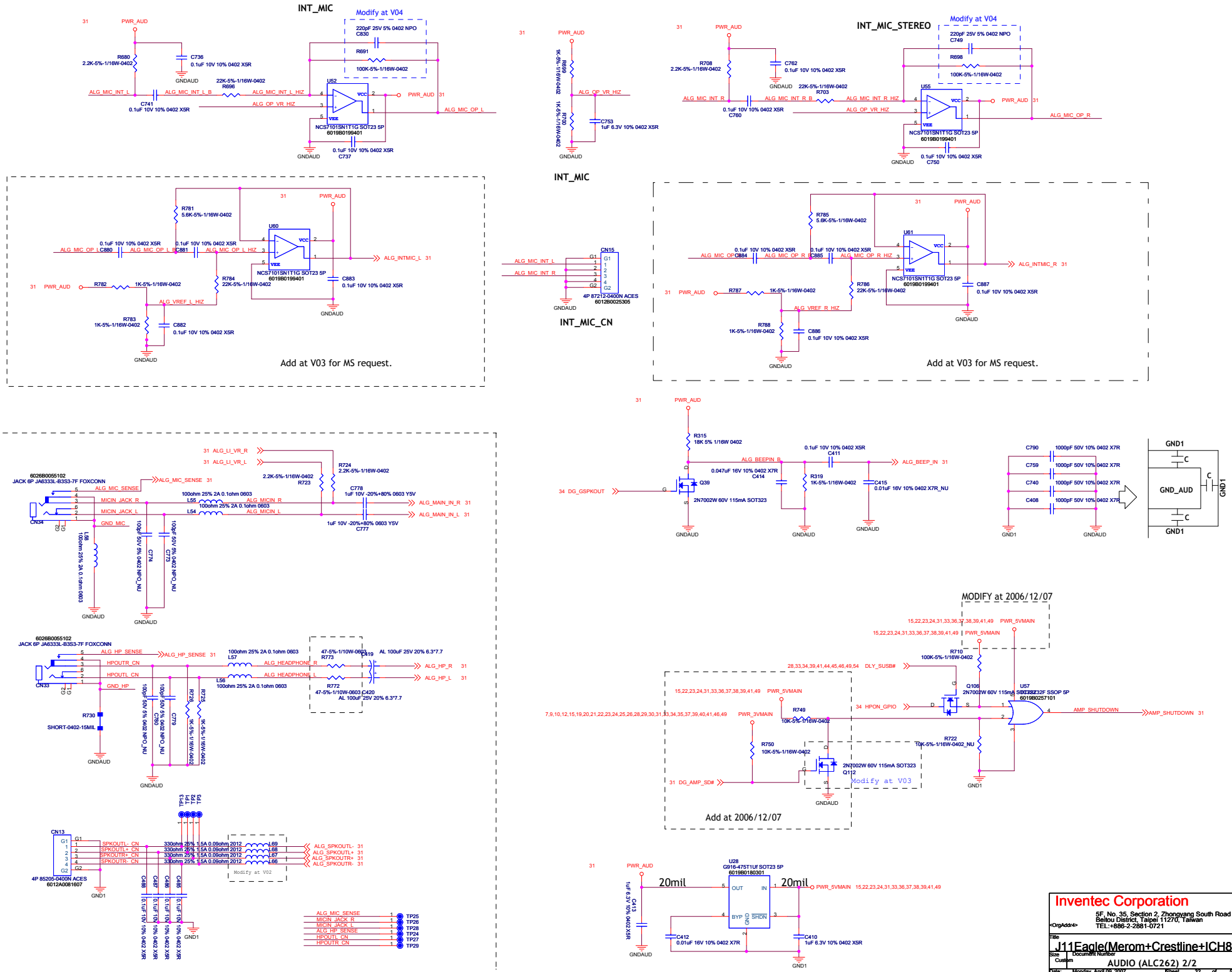
INT_MIC
Modify at V04
PWR_AUD
R680 2.2K-5%-1/16W-0402
C736 0.1uF 10V 10% 0402 X5R
GNDAUD
22K-5%-1/16W-0402 R696
ALG_MIC_INT_L
ALG_MIC_INT_L_B
ALG_MIC_INT_L_HIZ
C741 0.1uF 10V 10% 0402 X5R
ALG_OP_VR_HIZ
220pF 25V 5% 0402 NPO C830
R691 100K-5%-1/16W-0402
U52
NCS7101SN1T1G SOT23 5P 6019B0199401
ALG_MIC_OP_L
0.1uF 10V 10% 0402 X5R C737
R689 1K-5%-1/16W-0402
R690 1K-5%-1/16W-0402
ALG_OP_VR_HIZ
C753 1uF 6.3V 10% 0402 X5R
INT_MIC_STEREO
Modify at V04
R708 2.2K-5%-1/16W-0402
C762 0.1uF 10V 10% 0402 X5R
ALG_MIC_INT_R
0.1uF 10V 10% 0402 X5R C760
22K-5%-1/16W-0402 R703
ALG_MIC_INT_R_B
ALG_MIC_INT_R_HIZ
220pF 25V 5% 0402 NPO C749
R698 100K-5%-1/16W-0402
U55
NCS7101SN1T1G SOT23 5P 6019B0199401
ALG_MIC_OP_R
0.1uF 10V 10% 0402 X5R C750
R781 5.6K-5%-1/16W-0402
U60
NCS7101SN1T1G SOT23 5P 6019B0199401
ALG_MIC_OP_L_C880
ALG_MIC_OP_L_B
ALG_MIC_OP_L_HIZ
ALG_INTMIC_L
R782 1K-5%-1/16W-0402
R784 22K-5%-1/16W-0402
C883 0.1uF 10V 10% 0402 X5R
ALG_VREF_L_HIZ
R783 1K-5%-1/16W-0402
C882 0.1uF 10V 10% 0402 X5R
Add at V03 for MS request.
CN15
4P 87212-0400N ACES 6012B0025306
ALG_MIC_INT_L
ALG_MIC_INT_R
INT_MIC_CN
R785 5.6K-5%-1/16W-0402
U61
NCS7101SN1T1G SOT23 5P 6019B0199401
ALG_MIC_OP_R_C884
ALG_MIC_OP_R_B
ALG_MIC_OP_R_HIZ
ALG_INTMIC_R
R787 1K-5%-1/16W-0402
R786 22K-5%-1/16W-0402
C887 0.1uF 10V 10% 0402 X5R
ALG_VREF_R_HIZ
R788 1K-5%-1/16W-0402
C886 0.1uF 10V 10% 0402 X5R
Add at V03 for MS request.
R315 18K 5% 1/16W 0402
ALG_BEEPIN_B
0.1uF 10V 10% 0402 X5R C411
ALG_BEEP_IN
0.047uF 16V 10% 0402 X7R C414
R319 1K-5%-1/16W-0402
C415 0.01uF 16V 10% 0402 X7R_NU
34 DG_GSPKOUT
Q39 2N7002W 60V 115mA SOT323
C790 1000pF 50V 10% 0402 X7R
C759 1000pF 50V 10% 0402 X7R
C740 1000pF 50V 10% 0402 X7R
C408 1000pF 50V 10% 0402 X7R
GND1
GND_AUD
6026B0055102 JACK 6P JA6333L-B3S3-7F FOXCONN
CN34
ALG_MIC_SENSE
MICIN_JACK_R
MICIN_JACK_L
GND_MIC
ALG_LI_VR_R
ALG_LI_VR_L
2.2K-5%-1/16W-0402 R723
R724 2.2K-5%-1/16W-0402
100ohm 25% 2A 0.1ohm 0603 L55
100ohm 25% 2A 0.1ohm 0603 L54
ALG_MICIN_R
ALG_MICIN_L
C778 1uF 10V -20%+80% 0603 Y5V
ALG_MAIN_IN_R
ALG_MAIN_IN_L
1uF 10V -20%+80% 0603 Y5V C777
L58 100ohm 25% 2A 0.1ohm 0603
100pF 50V 5% 0402 NPO_NU C774
100pF 50V 5% 0402 NPO_NU C775
6026B0055102 JACK 6P JA6333L-B3S3-7F FOXCONN
CN33
ALG_HP_SENSE
HPOUTR_CN
HPOUTL_CN
GND_HP
100ohm 25% 2A 0.1ohm 0603 L57
100ohm 25% 2A 0.1ohm 0603 L56
ALG_HEADPHONE_R
ALG_HEADPHONE_L
47-5%-1/10W-0603 R773
47-5%-1/10W-0603 R772
AL 100uF 25V 20% 6.3*7.7 C419
AL 100uF 25V 20% 6.3*7.7 C420
ALG_HP_R
ALG_HP_L
R730 SHORT-0402-15MIL
100pF 50V 5% 0402 NPO_NU C780
100pF 50V 5% 0402 NPO_NU C779
R728 1K-5%-1/16W-0402
R729 1K-5%-1/16W-0402
CN13
4P 85205-0400N ACES 6012A0081607
SPKOUTL- CN
SPKOUTL+ CN
SPKOUTR+ CN
SPKOUTR- CN
330ohm 25% 1.5A 0.09ohm 2012 L69
330ohm 25% 1.5A 0.09ohm 2012 L68
330ohm 25% 1.5A 0.09ohm 2012 L67
330ohm 25% 1.5A 0.09ohm 2012 L66
Modify at V02
ALG_SPKOUTL-
ALG_SPKOUTL+
ALG_SPKOUTR+
ALG_SPKOUTR-
C488 0.1uF 10V 10% 0402 X5R
C487 0.1uF 10V 10% 0402 X5R
C486 0.1uF 10V 10% 0402 X5R
C485 0.1uF 10V 10% 0402 X5R
ALG_MIC_SENSE TP25
MICIN_JACK_R TP26
MICIN_JACK_L TP28
ALG_HP_SENSE TP24
HPOUTL_CN TP27
HPOUTR_CN TP29
MODIFY at 2006/12/07
15,22,23,24,31,33,36,37,38,39,41,49 PWR_5VMAIN
R710 100K-5%-1/16W-0402
28,33,34,39,41,44,45,46,49,54 DLY_SUSB#
Q108 2N7002W 60V 115mA SOT323
U57 SN74LVC32F SSOP 5P 6019B0257101
34 HPON_GPIO
AMP_SHUTDOWN
R749 10K-5%-1/16W-0402
R750 10K-5%-1/16W-0402
R722 10K-5%-1/16W-0402_NU
Q112 2N7002W 60V 115mA SOT323
31 DG_AMP_SD#
Modify at V03
Add at 2006/12/07
U28 G916-475T1Uf SOT23 5P 6019B0180301
20mil
OUT
IN
BYP
GND
SHDN
C413 1uF 6.3V 10% 0402X5R
C412 0.01uF 16V 10% 0402 X7R
C410 1uF 6.3V 10% 0402 X5R
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TEL:+886-2-2881-0721
J11Eagle(Merom+Crestline+ICH8M)
AUDIO (ALC262) 2/2
Size Custom
Document Number
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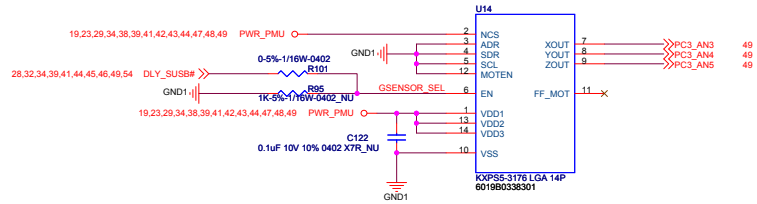
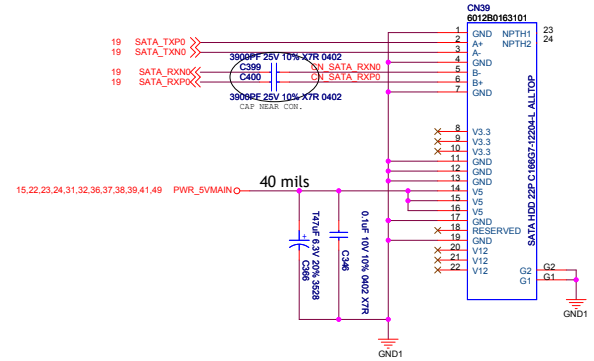
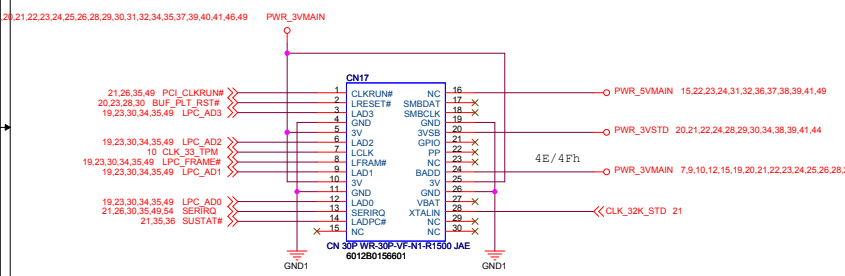


GSENSOR_SEL ---		
	0 : LIS302ALK	R101 reverse, R95 mount
	0 : KXPB5	R101 reverse, R95 mount
	1 : KXPS5-3176	R95 reverse, R101 mount

SATA CON.



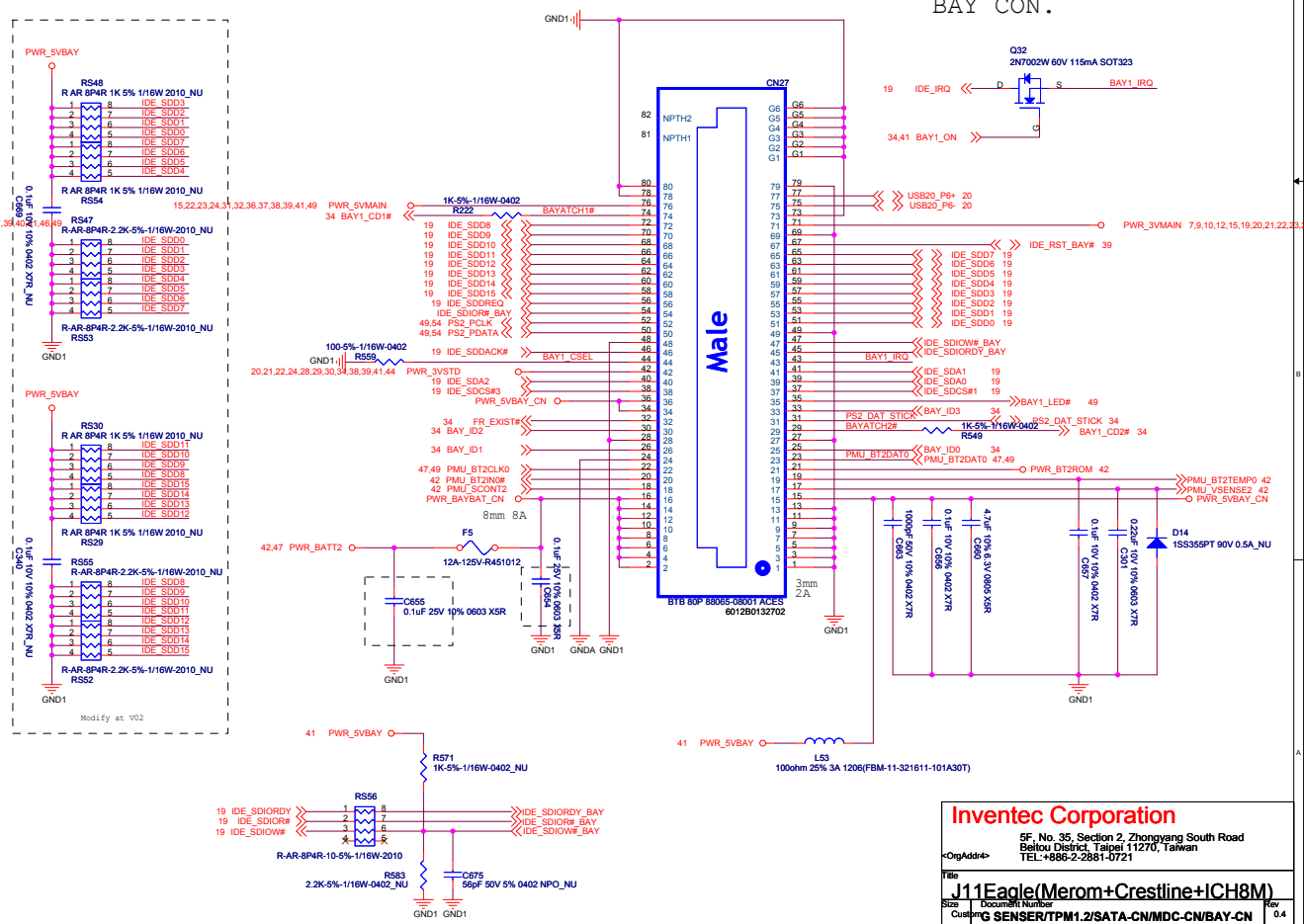
TPM CON.



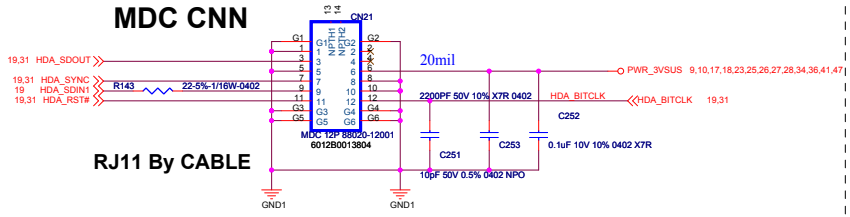
TPM Configuration

	High	Low
TPM_BADDR	4E/4Fh	2E/2Fh
TPM_PACCESS	Physical Presence ON	Physical Presence OFF

BAY CON.



MDC CNN



RJ11 By CABLE

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TEL:+886-2-2881-0721

Title	J11Eagle(Merom+Crestline+ICH8M)
Size	Custom
Document Number	G SENSER/TPM1.2/SATA-CN/MDC-CN/BAY-CN
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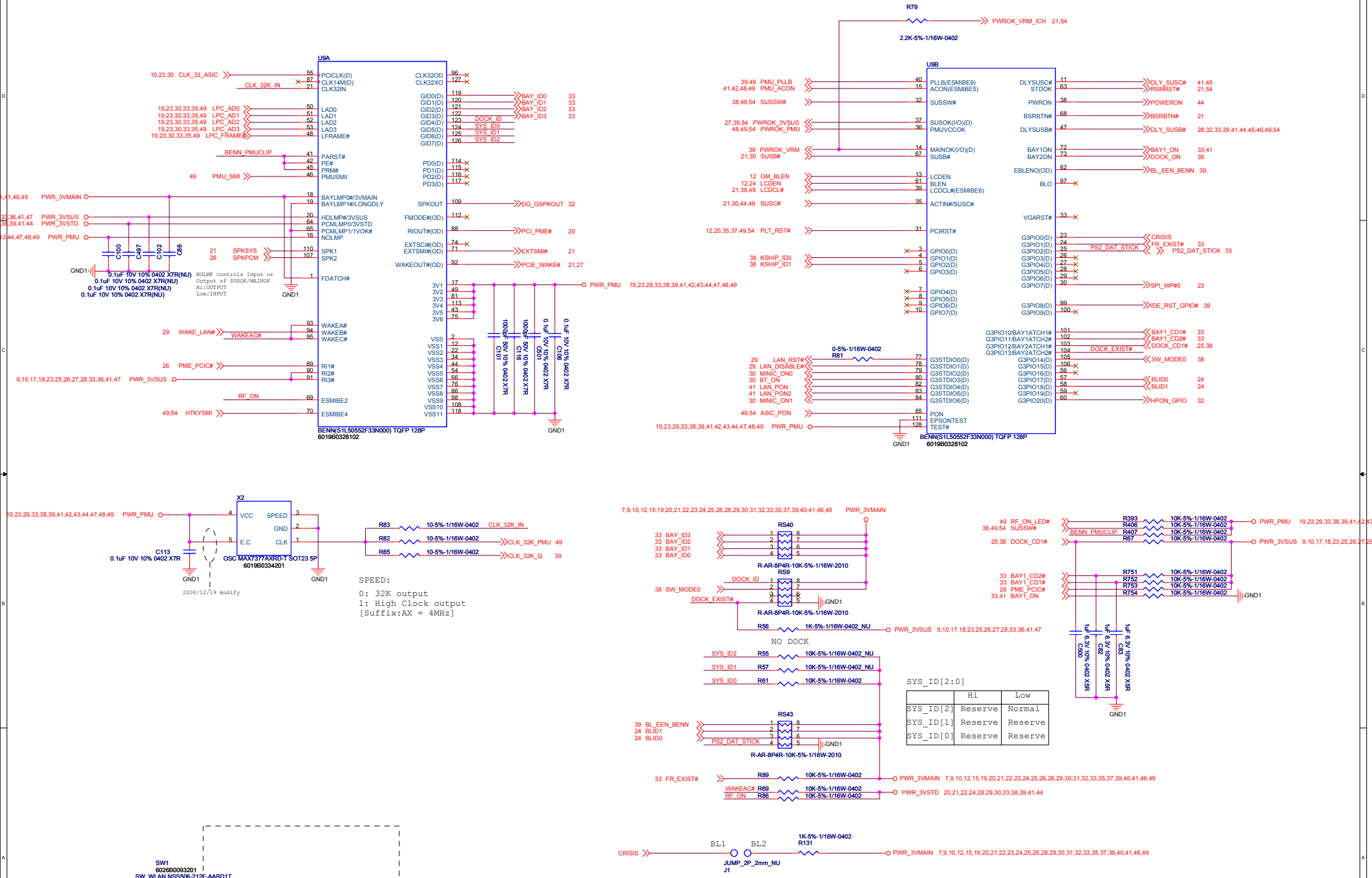

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Beitou District, Taipei 112701, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: BENN | Rev: 0.4

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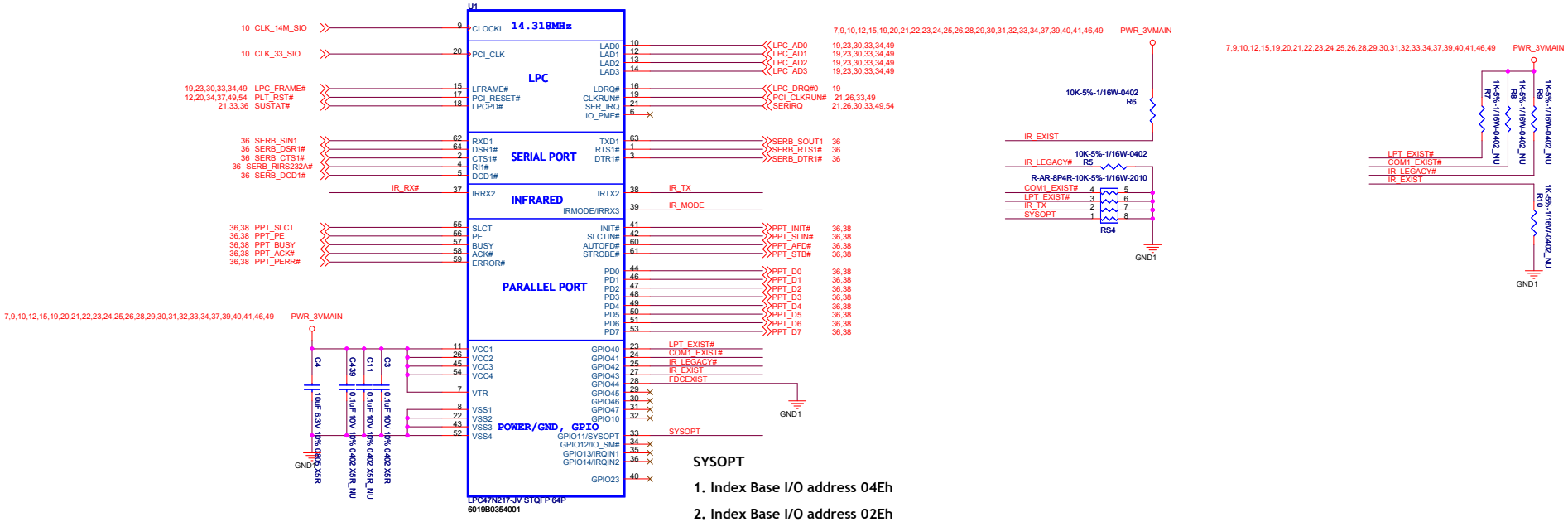
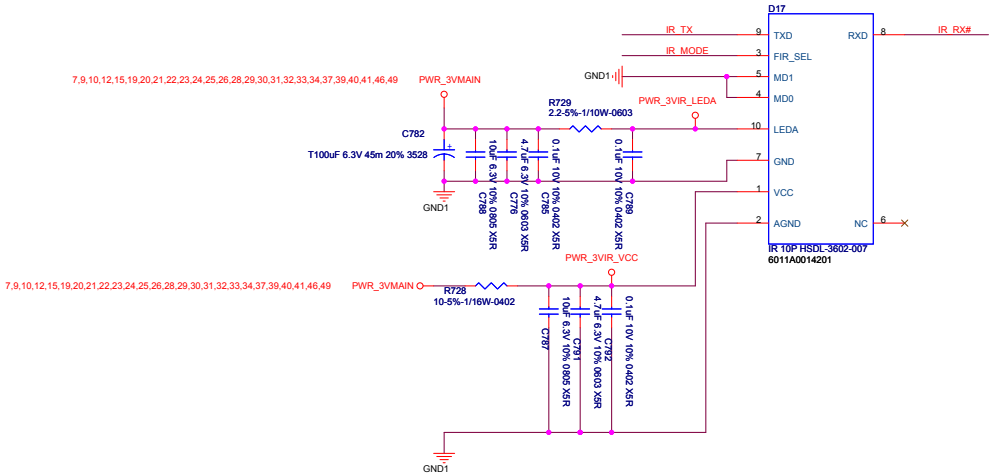


SYSOPT

1. Index Base I/O address 04Eh
2. Index Base I/O address 02Eh



Inventec Corporation
<OrgAddr4>
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Beitou District, Taipei 112?0, Taiwan
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Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: SUPER I/O & IrDA | Rev: 0.4

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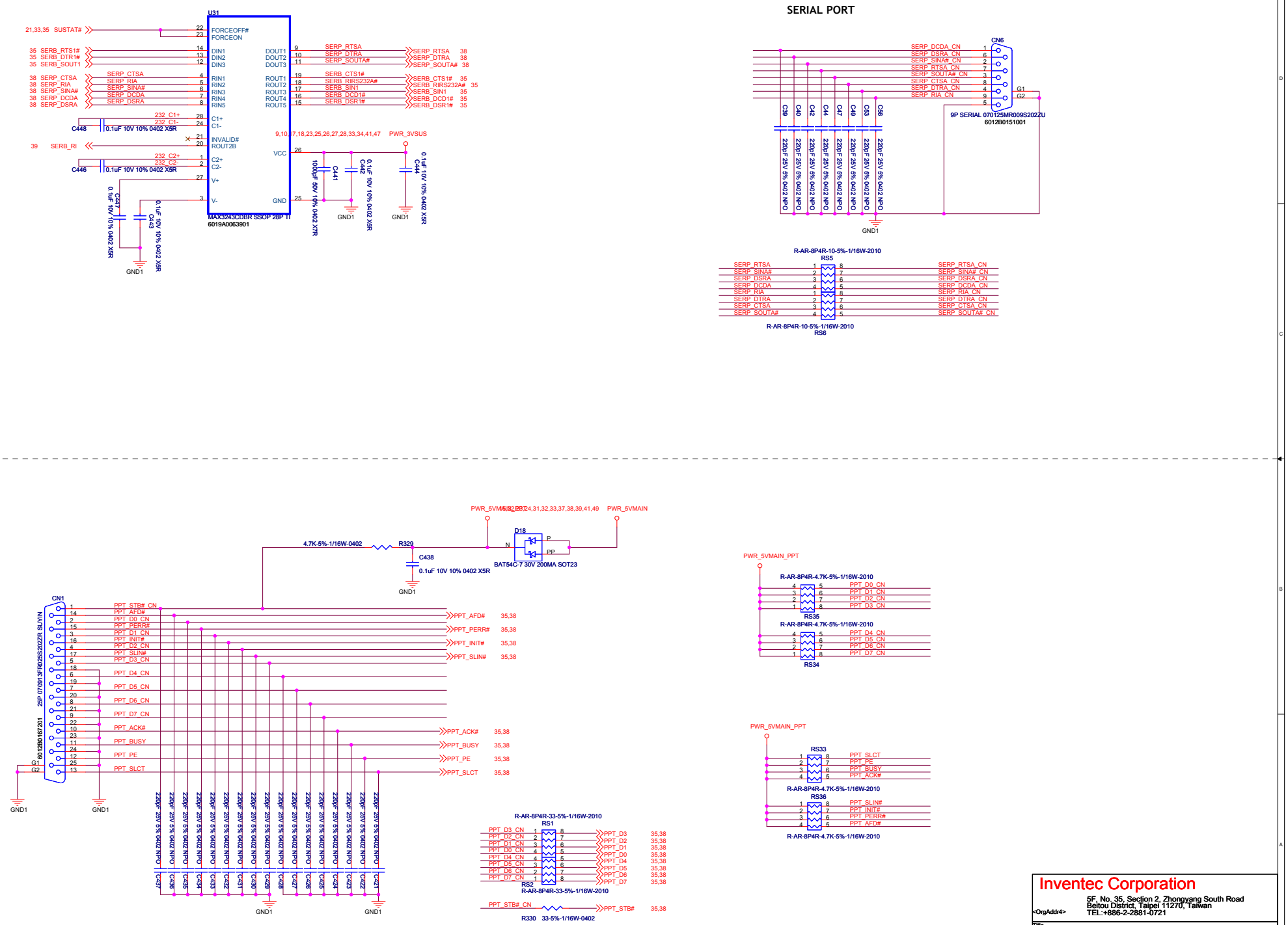
SERIAL PORT
U31
MAX3243CDBR SSOP 28P TI
6019A0063901
21,33,35 SUSTAT#
FORCEOFF#
FORCEON
DIN1
DIN2
DIN3
RIN1
RIN2
RIN3
RIN4
RIN5
C1+
C1-
INVALID#
ROUT2B
C2+
C2-
V+
V-
DOUT1
DOUT2
DOUT3
ROUT1
ROUT2
ROUT3
ROUT4
ROUT5
VCC
GND
SERB_RTS1#
SERB_DTR1#
SERB_SOUT1
SERB_CTSA
SERB_RIA
SERB_SINA#
SERB_DCDA
SERB_DSRA
SERB_RI
SERP_RTSA
SERP_DTRA
SERP_SOUTA#
SERP_CTSA
SERP_RIA
SERP_SINA#
SERP_DCDA
SERP_DSRA
SERB_CTS1#
SERB_RIRS232A#
SERB_SIN1
SERB_DCD1#
SERB_DSR1#
232_C1+
232_C1-
232_C2+
232_C2-
C448 0.1uF 10V 10% 0402 X5R
C446 0.1uF 10V 10% 0402 X5R
C447 0.1uF 10V 10% 0402 X5R
C443 0.1uF 10V 10% 0402 X5R
9,10,17,18,23,25,26,27,28,33,34,41,47 PWR_3VSUS
C441 100uF 50V 10% 0402 X7R
C442 0.1uF 10V 10% 0402 X5R
C444 0.1uF 10V 10% 0402 X5R
GND1
CN6
9P SERIAL 070125MR009S202ZU
6012B0151001
SERP_DCDA_CN
SERP_DSRA_CN
SERP_SINA#_CN
SERP_RTSA_CN
SERP_SOUTA#_CN
SERP_CTSA_CN
SERP_DTRA_CN
SERP_RIA_CN
C39 C40 C42 C44 C47 C49 C53 C56
220pF 25V 5% 0402 NPO
G1
G2
R-AR-8P4R-10-5%-1/16W-2010
RS5
RS6
SERP_RTSA
SERP_SINA#
SERP_DSRA
SERP_DCDA
SERP_RIA
SERP_DTRA
SERP_CTSA
SERP_SOUTA#
SERP_RTSA_CN
SERP_SINA#_CN
SERP_DSRA_CN
SERP_DCDA_CN
SERP_RIA_CN
SERP_DTRA_CN
SERP_CTSA_CN
SERP_SOUTA#_CN
PWR_5VMAIN
D18
BAT54C-7 30V 200MA SOT23
4.7K-5%-1/16W-0402
R329
C438 0.1uF 10V 10% 0402 X5R
CN1
25P 070913FR025S202ZR SUYIN
6012B0167201
PPT_STB# CN
PPT_AFD#
PPT_D0_CN
PPT_PERR#
PPT_D1_CN
PPT_INIT#
PPT_D2_CN
PPT_SLIN#
PPT_D3_CN
PPT_D4_CN
PPT_D5_CN
PPT_D6_CN
PPT_D7_CN
PPT_ACK#
PPT_BUSY
PPT_PE
PPT_SLCT
35,38
PWR_5VMAIN_PPT
R-AR-8P4R-4.7K-5%-1/16W-2010
RS35
RS34
RS33
RS36
R-AR-8P4R-33-5%-1/16W-2010
RS1
RS2
R330 33-5%-1/16W-0402
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721
Title
J11Eagle(Merom+Crestline+ICH8M)
Size C
Document Number
SERIAL PORT & PARALLEL PORT
Rev 0.4
Date: Monday, April 09, 2007
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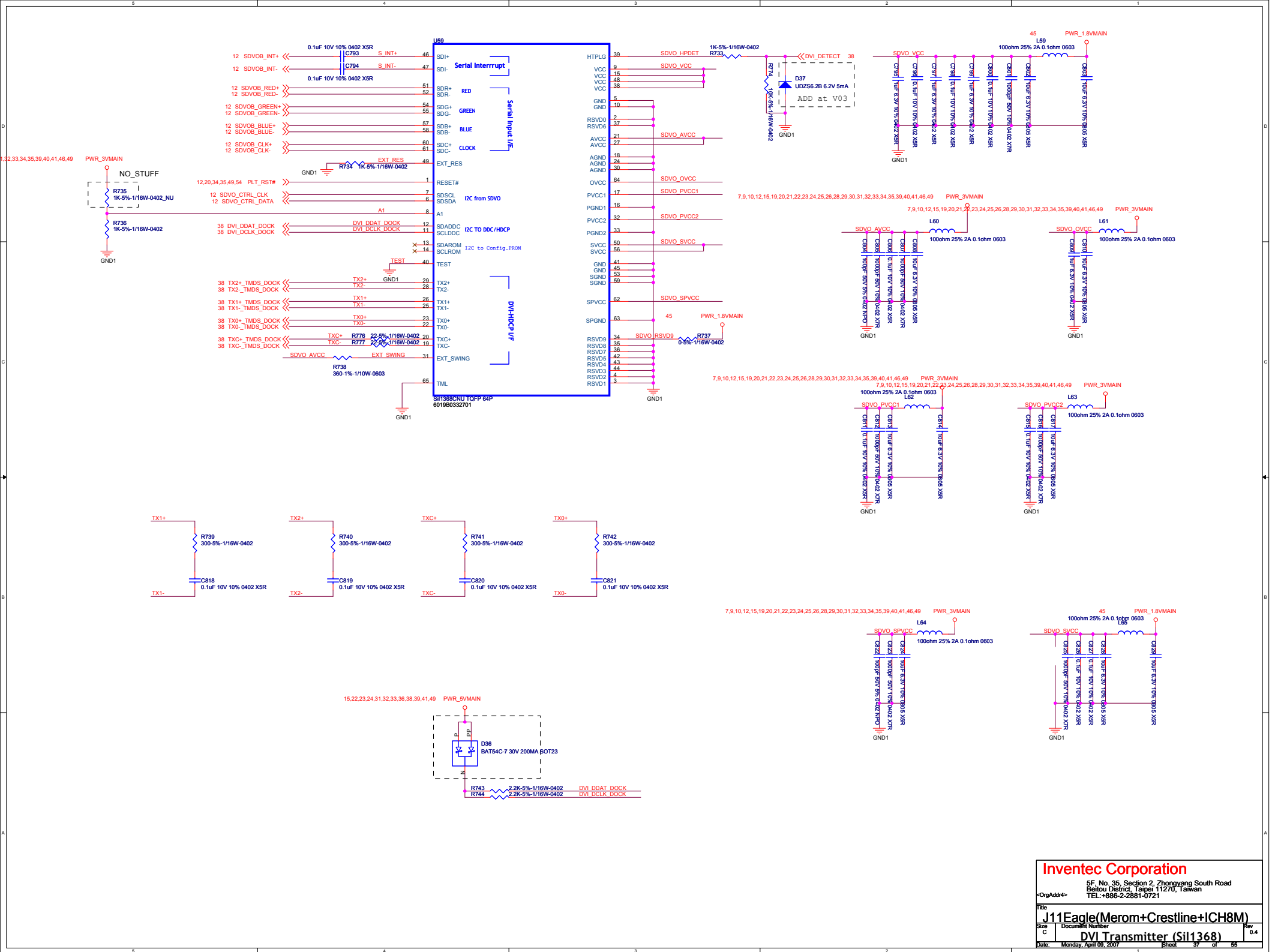

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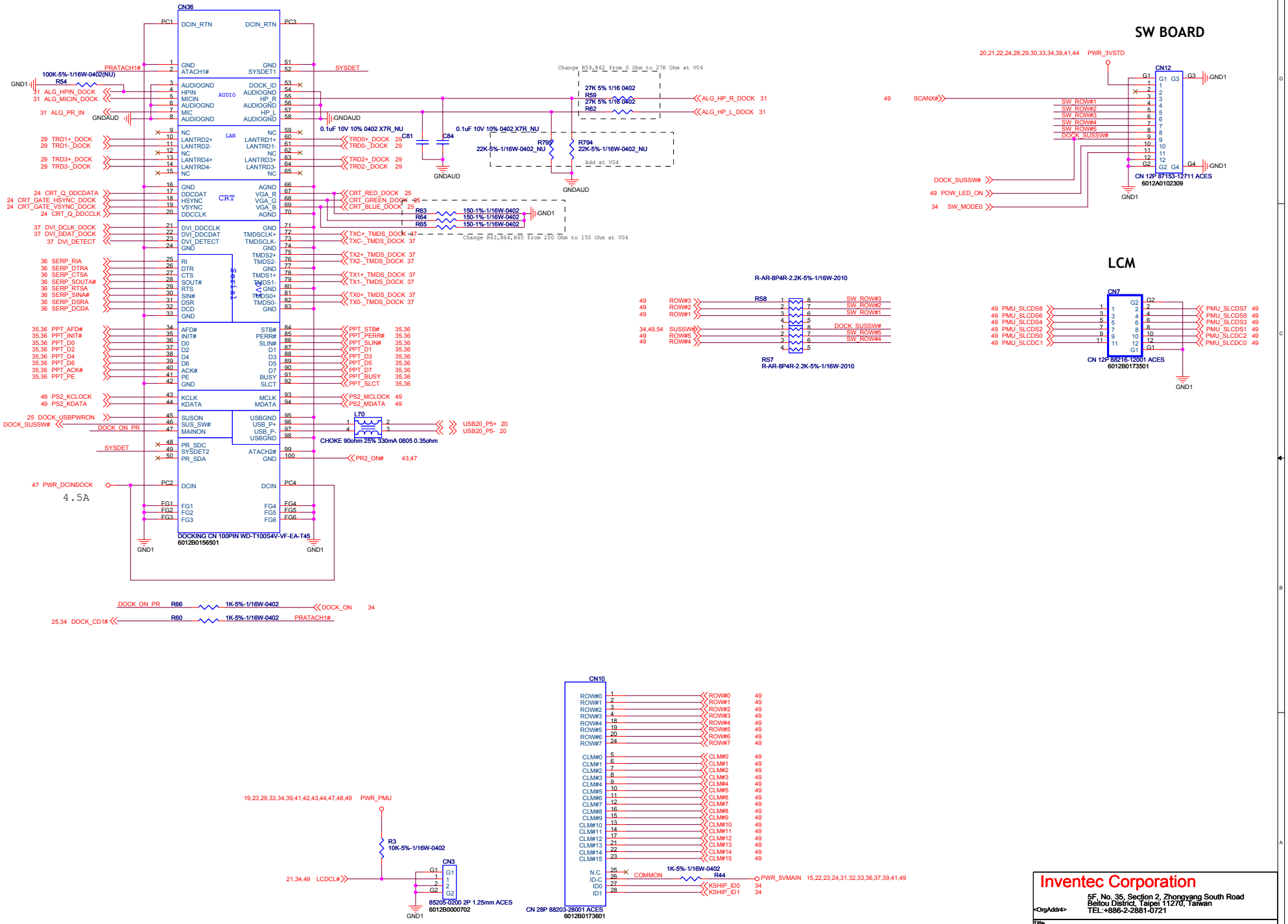
Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: DVI Transmitter (Sil1368) | Rev: 0.4

Date: Monday, April 09, 2007 | Sheet 37 of 55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DOCKING CN 100PIN WD-T100S4V-VF-EA-T45
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SW BOARD
CN12
CN 12P 87153-12711 ACES
6012A0102309
LCM
CN7
CN 12P 88216-12001 ACES
6012B0173501
RS8
R-AR-8P4R-2.2K-5%-1/16W-2010
RS7
R-AR-8P4R-2.2K-5%-1/16W-2010
L70
CHOKE 90ohm 25% 330mA 0805 0.35ohm
CN10
CN 28P 88203-28001 ACES
6012B0173601
CN3
85205-0200 2P 1.25mm ACES
6012B0000702
Change R59,R62 from 0 Ohm to 27K Ohm at V04
Change R63,R64,R65 from 200 Ohm to 150 Ohm at V04
Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
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TEL:+886-2-2881-0721
J11Eagle(Merom+Crestline+ICH8M)
DOCK/KB/ST-LCD CON
Monday, April 09, 2007
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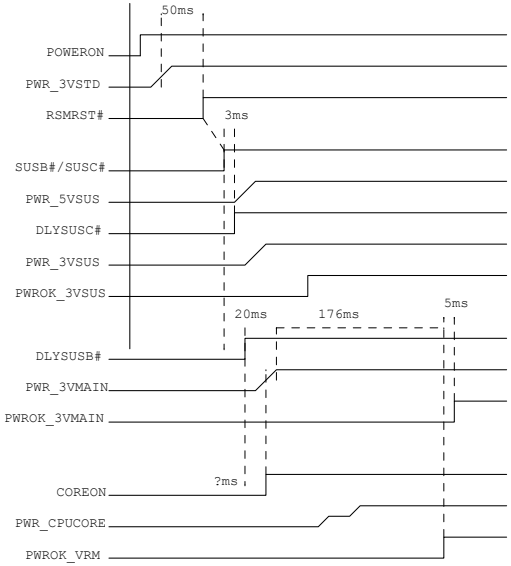

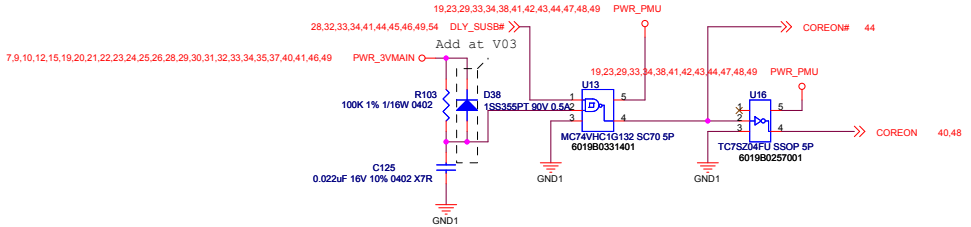

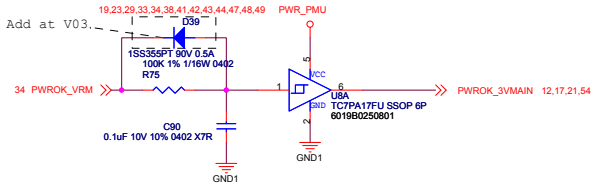

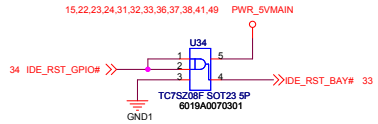

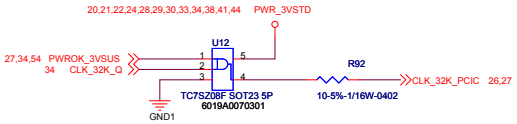

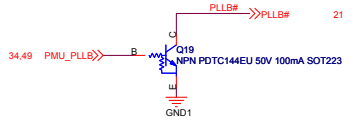

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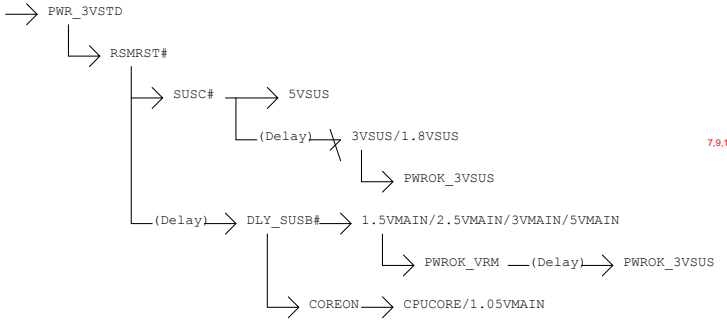

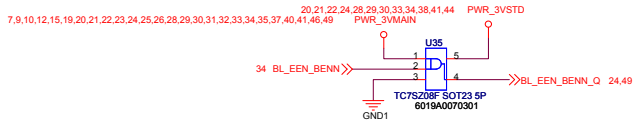

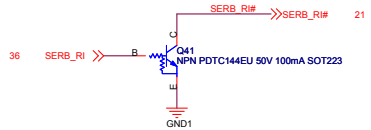

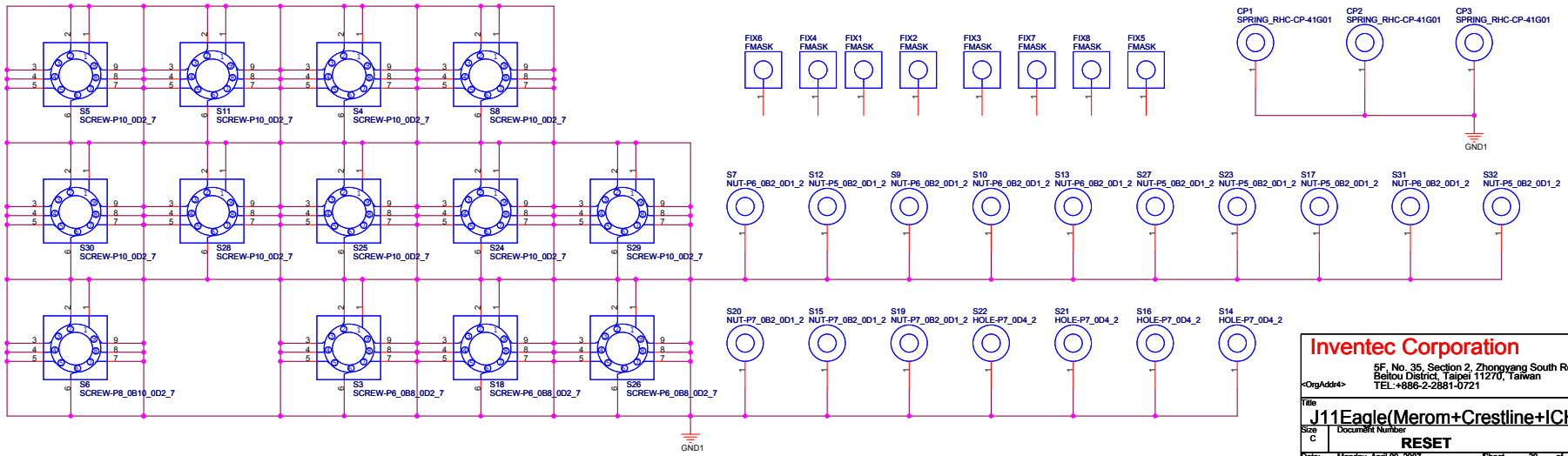

Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
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<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

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C	RESET	0.4

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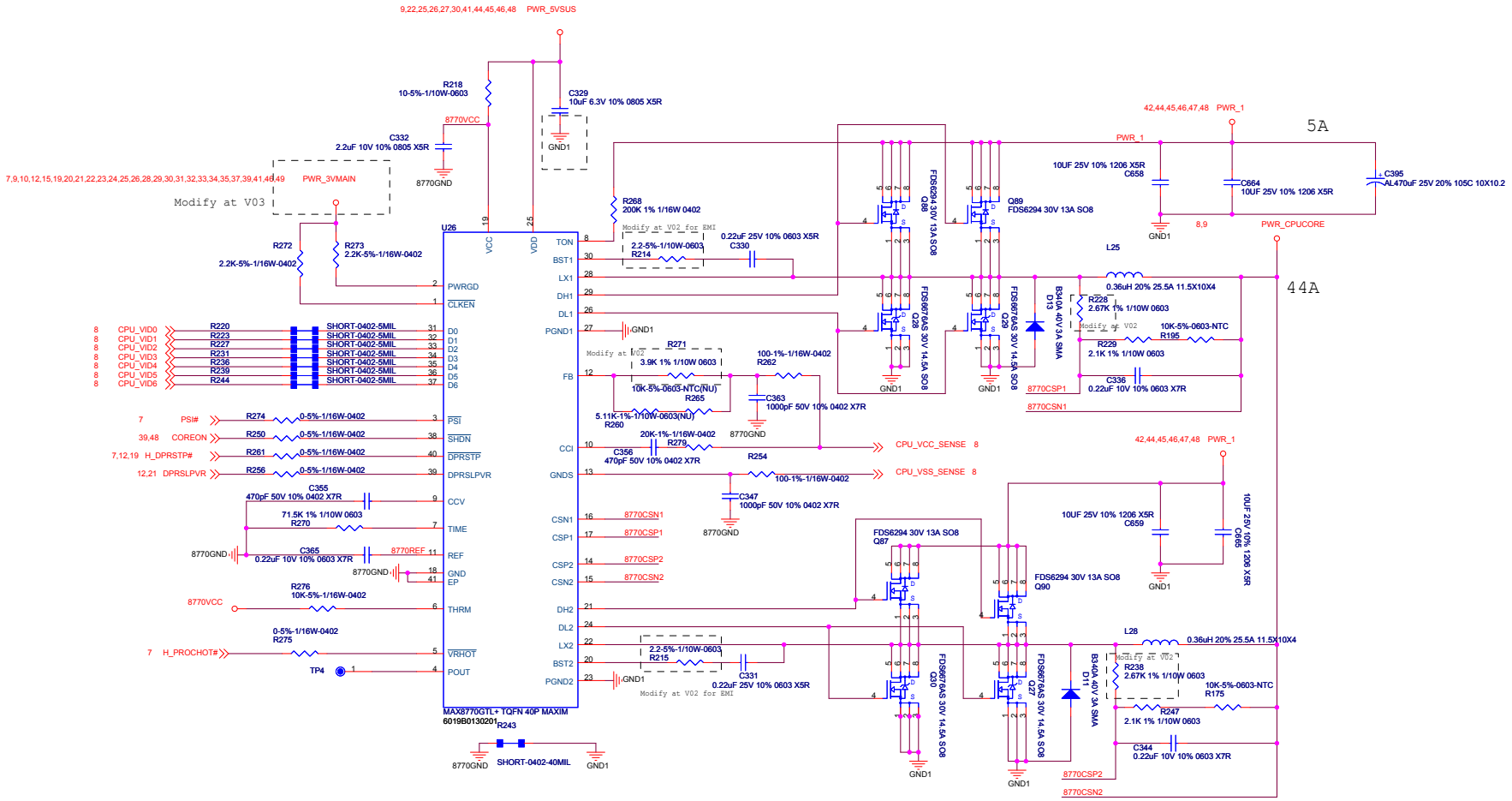

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5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

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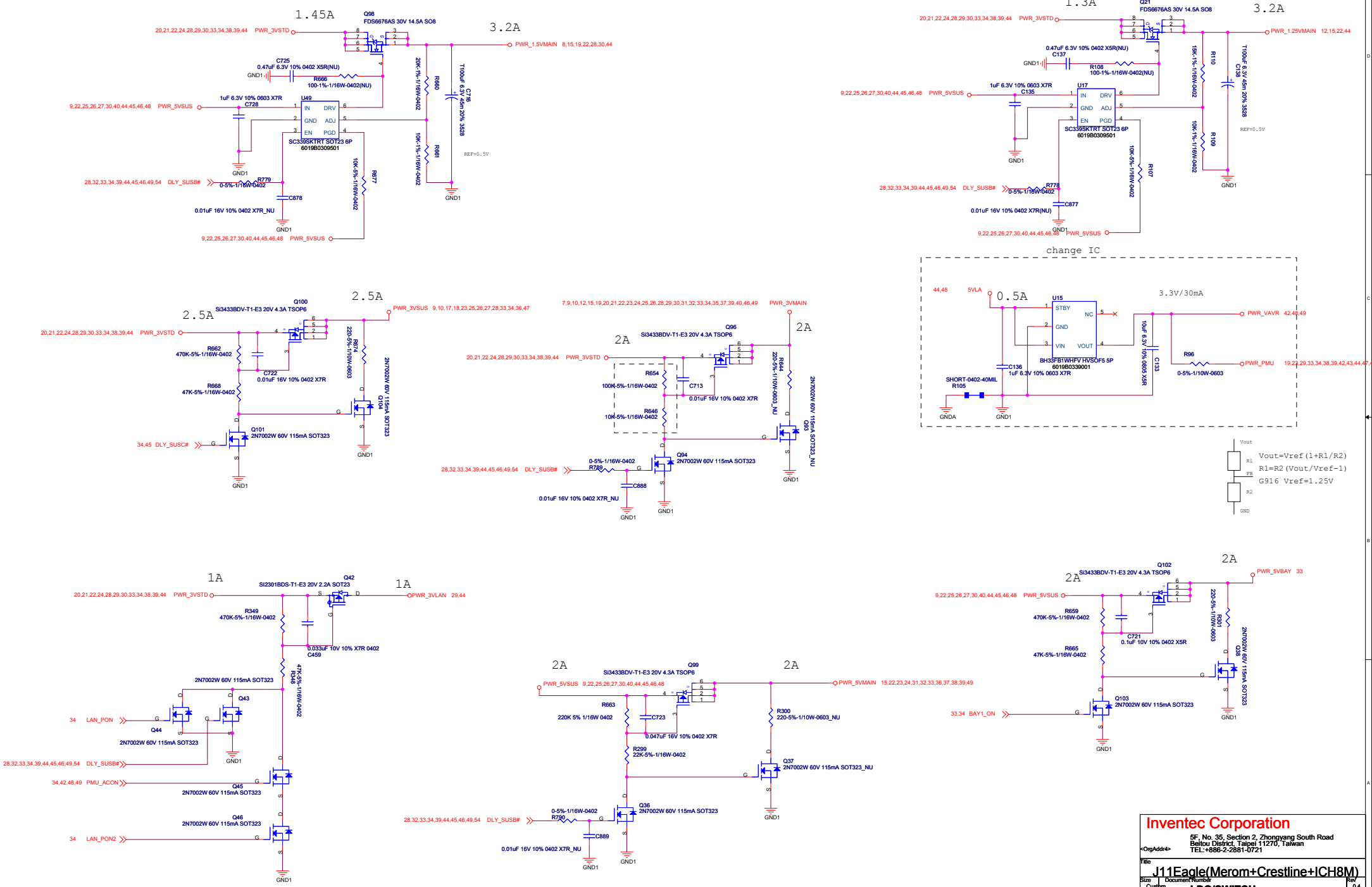

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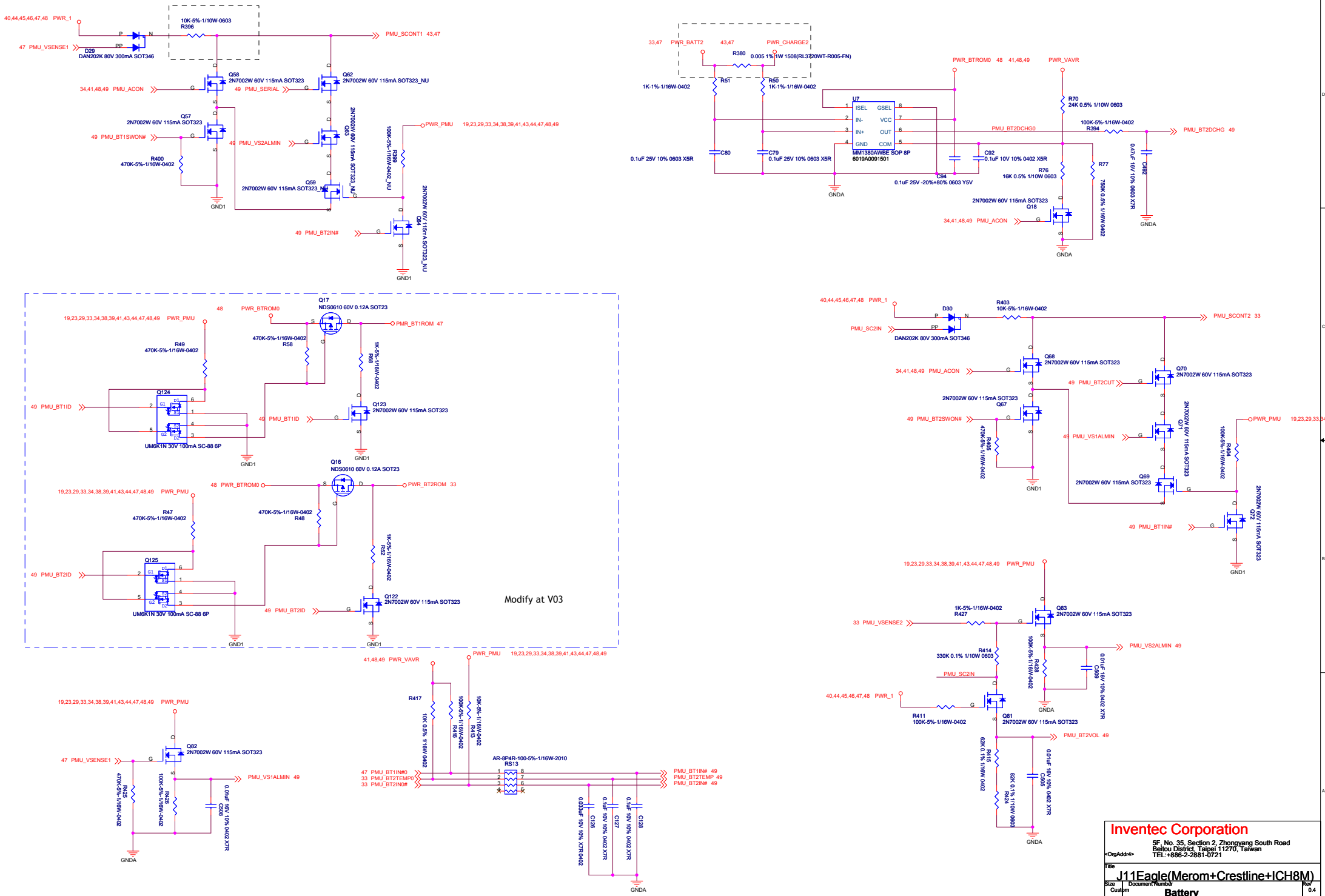

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Title: J11Eagle(Merom+Crestline+ICH8M)

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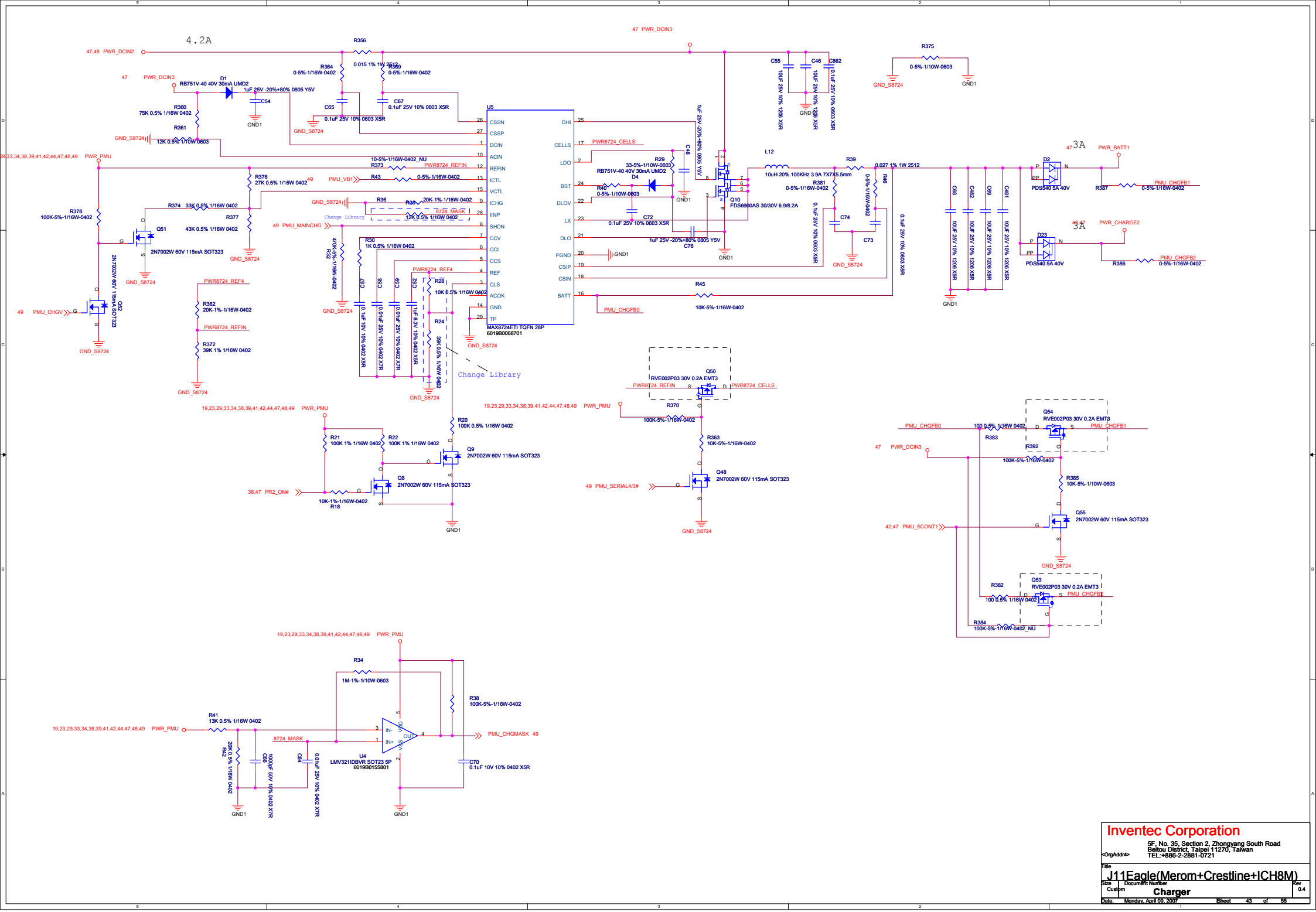

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Title: J11Eagle(Merom+Crestline+ICH8M)

Size: Custom | Document Number: Charger | Rev: 0.4

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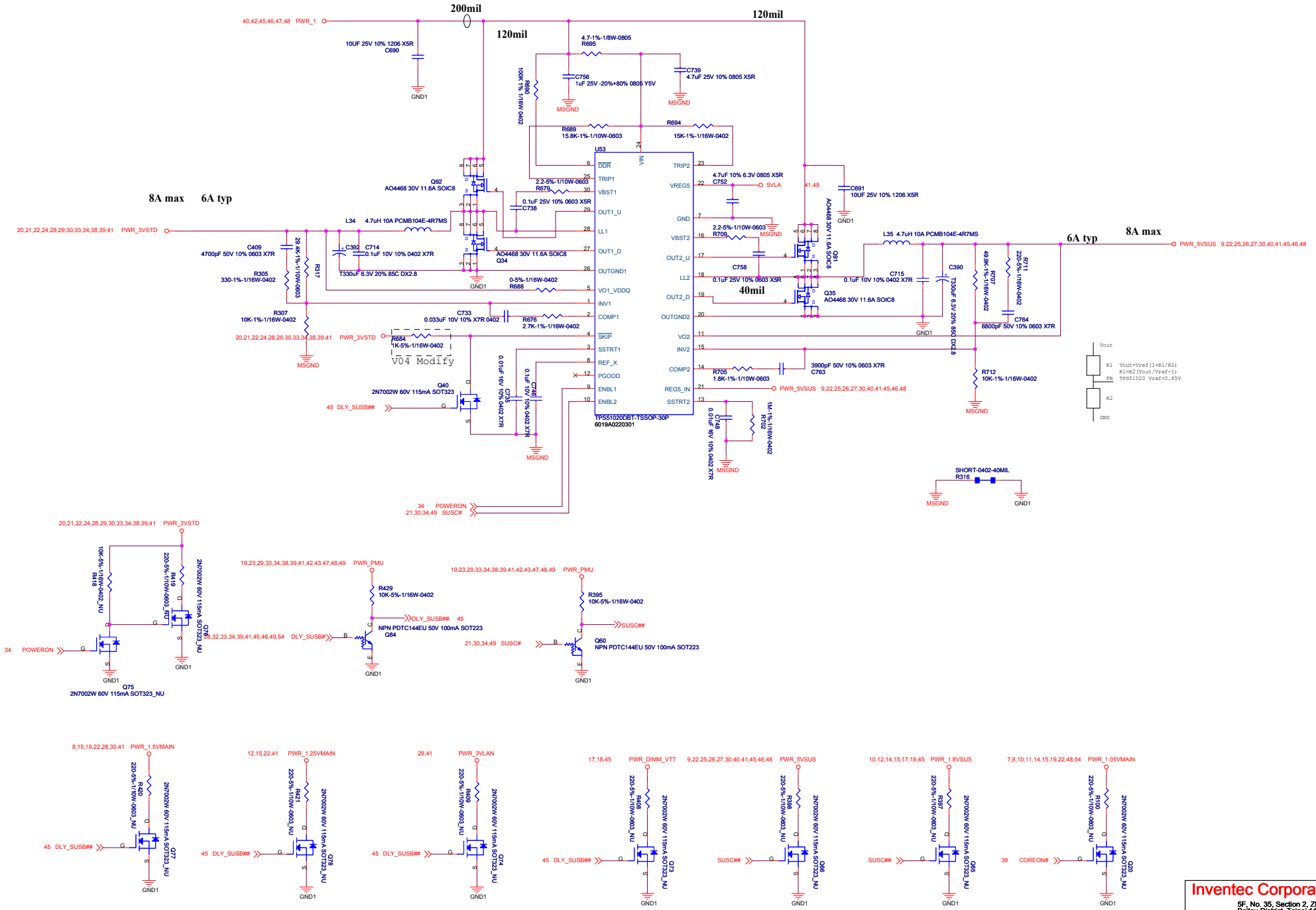

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<OrgAddr4> TEL:+886-2-2881-0721

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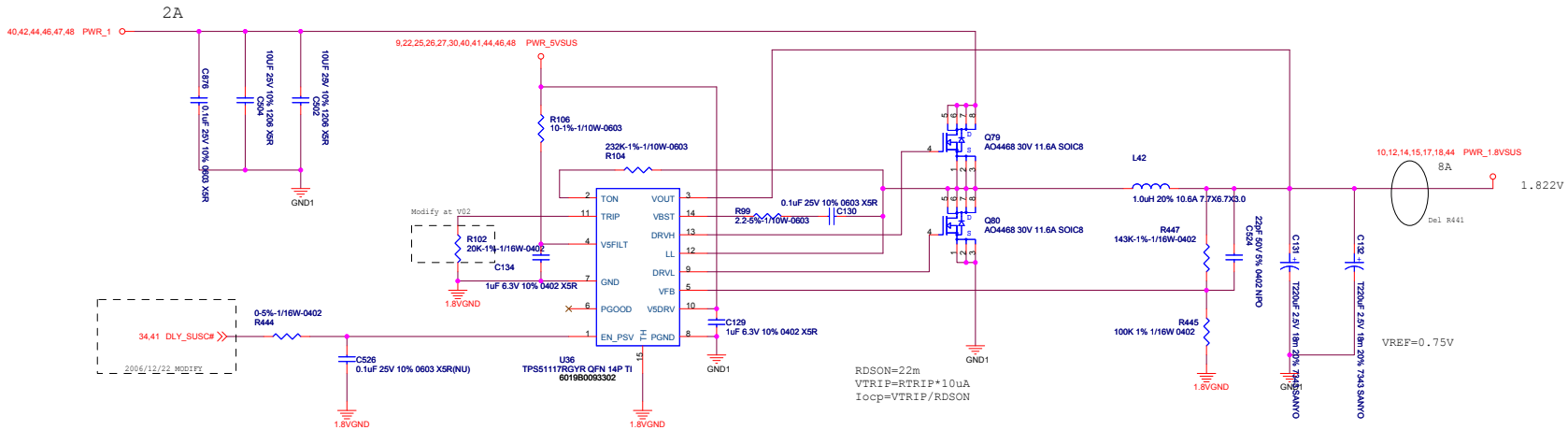
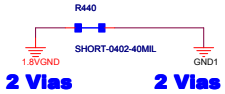
Date: Monday, April 09, 2007 | Sheet 44 of 55





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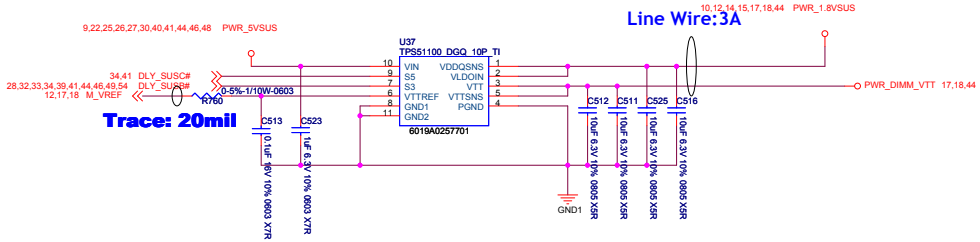

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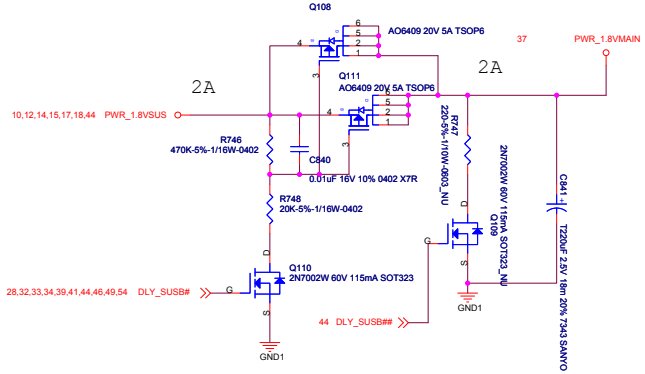

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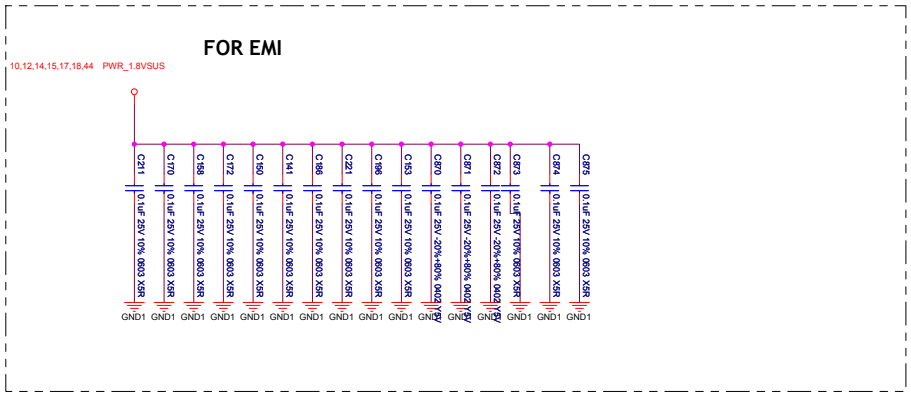

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Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

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Size	Document Number	Rev
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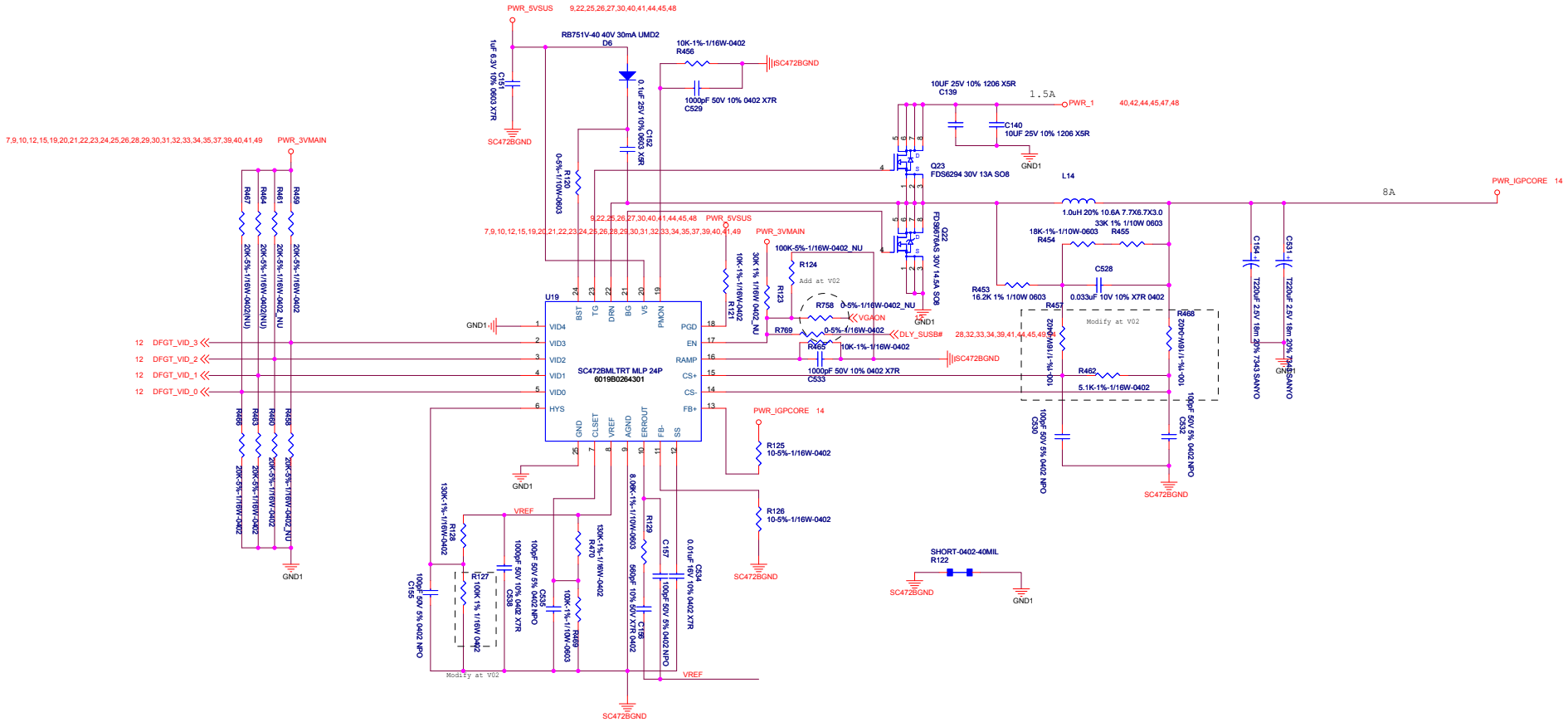

Inventec Corporation

<OrgAddr4> 5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

Size: Custom | Document Number: GPU_CORE | Rev: 0.4

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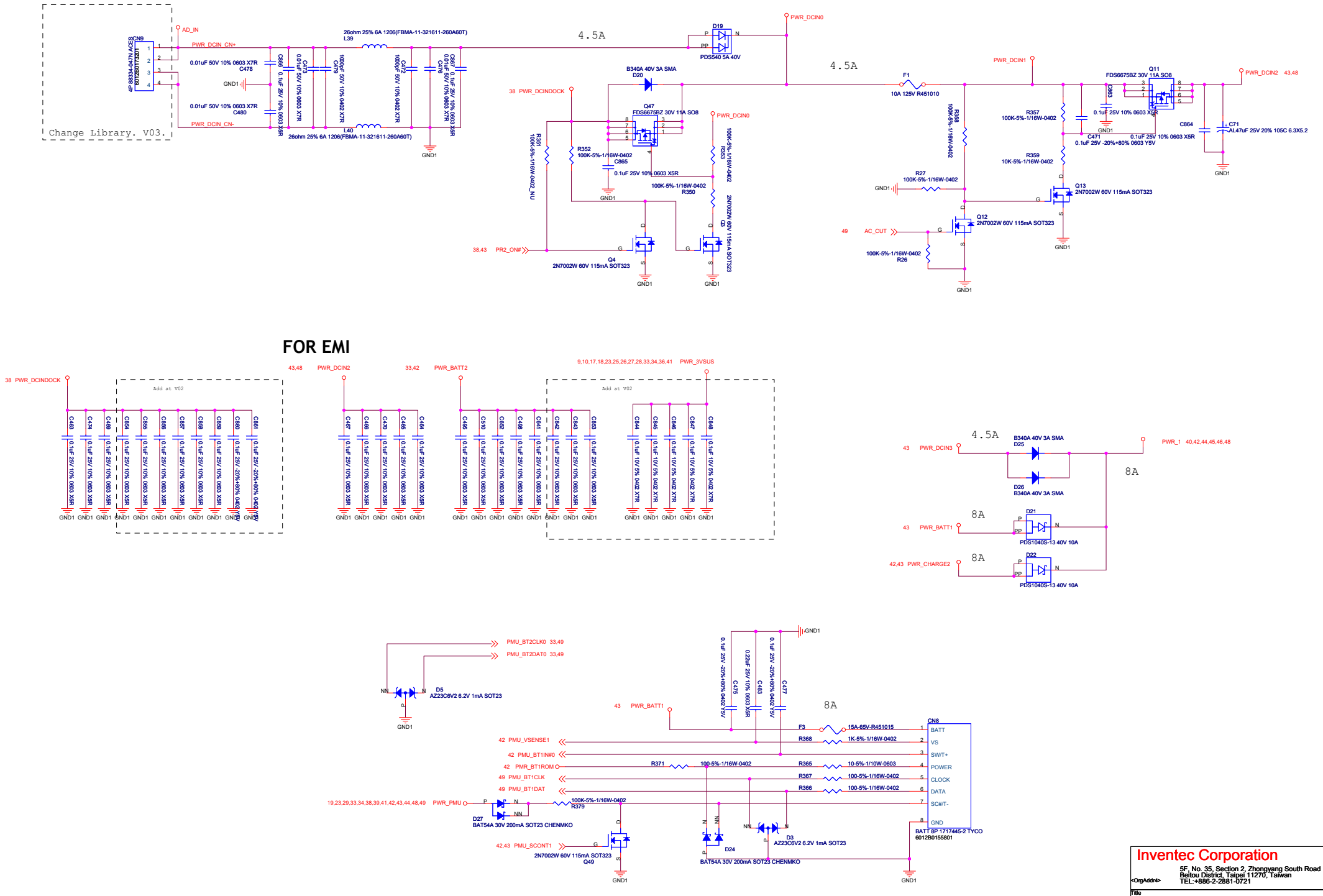

Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

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Size: Custom | Document Number: BATTERY CN | Rev: 0.4

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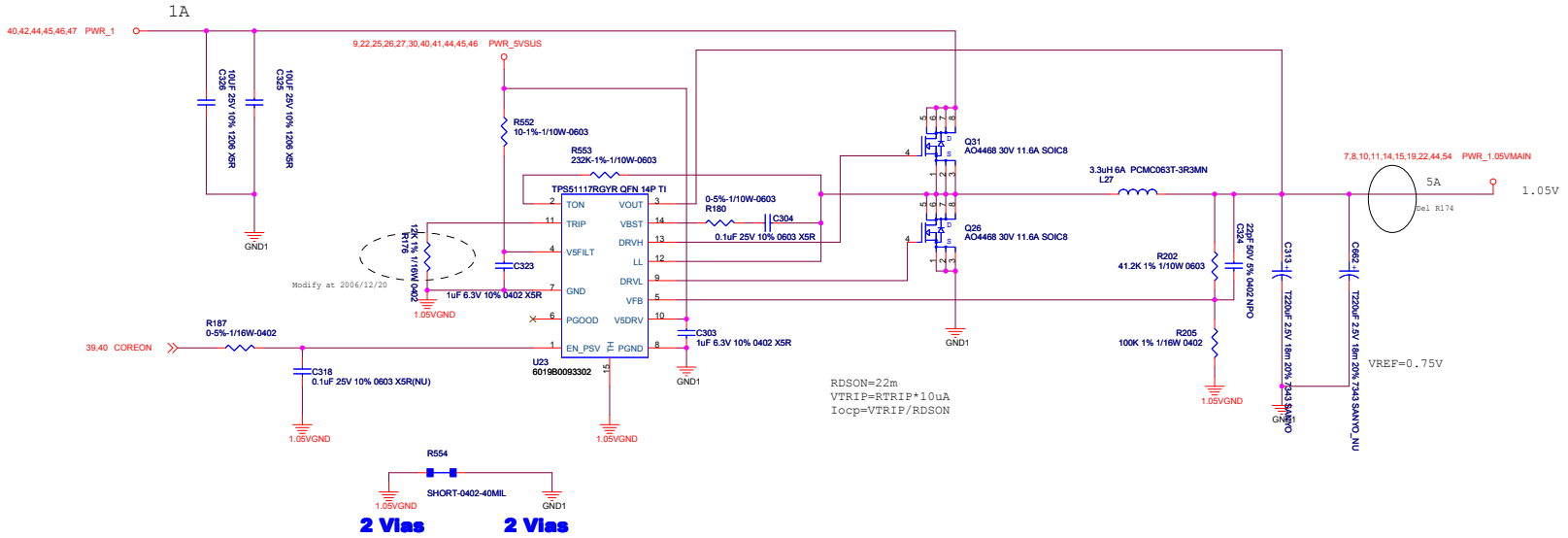

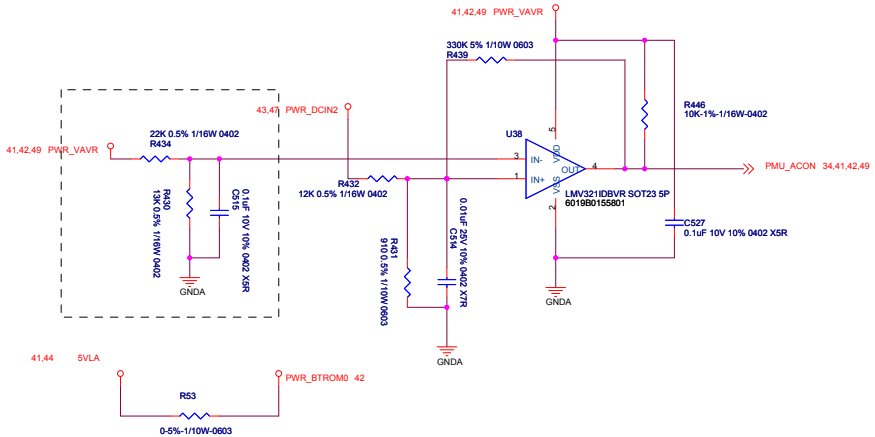

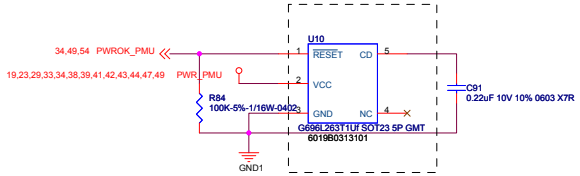

Inventec Corporation
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Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721
<OrgAddr4>

Title: J11Eagle(Merom+Crestline+ICH8M)

Size	Document Number	Rev
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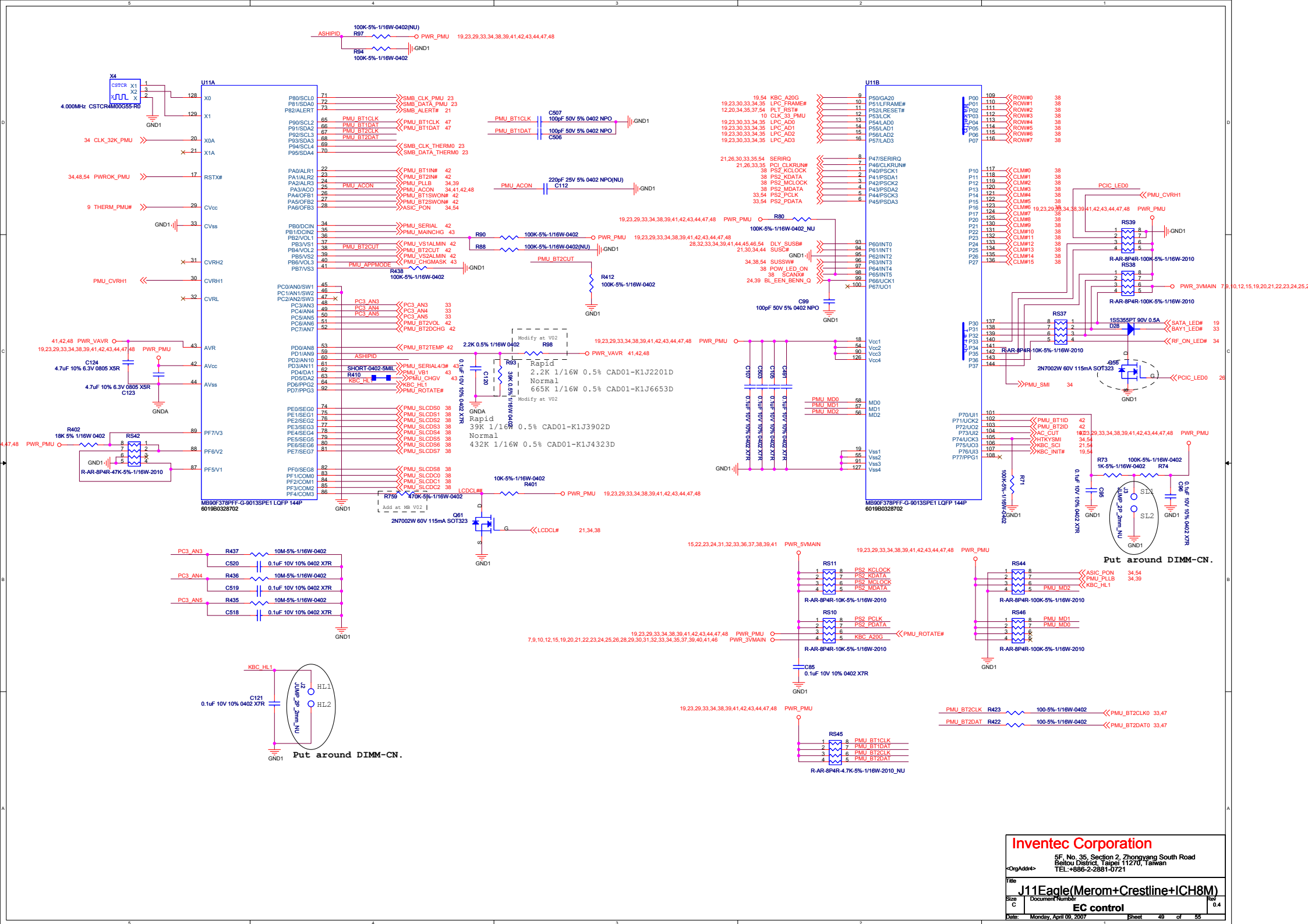

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Title: J11Eagle(Merom+Crestline+ICH8M)

Size: C | Document Number: EC control | Rev: 0.4

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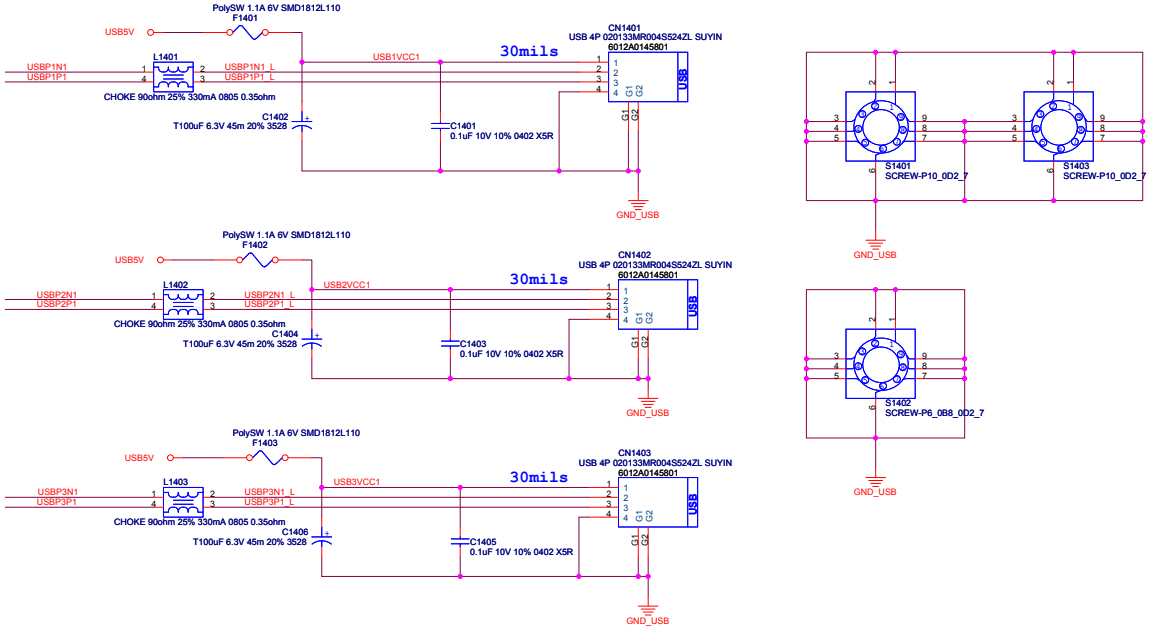

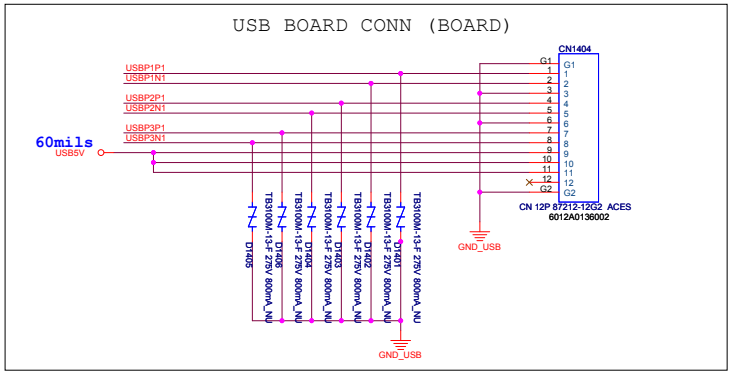

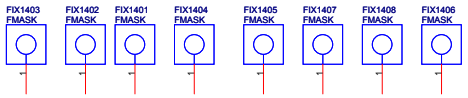

Inventec Corporation
5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

Size: Custom | Document Number: USB BOARD | Rev: 0.4

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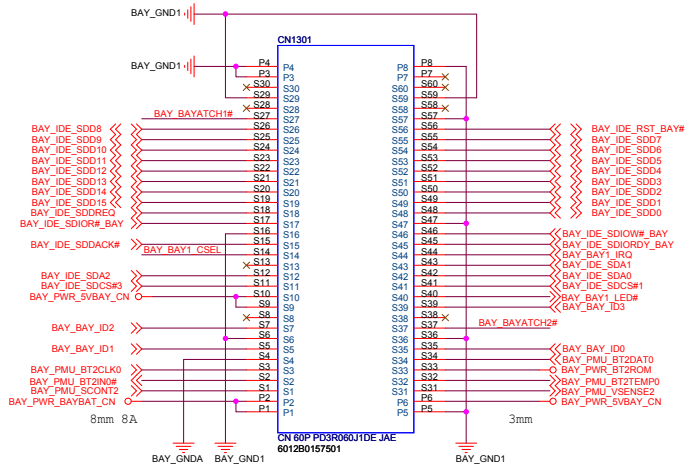

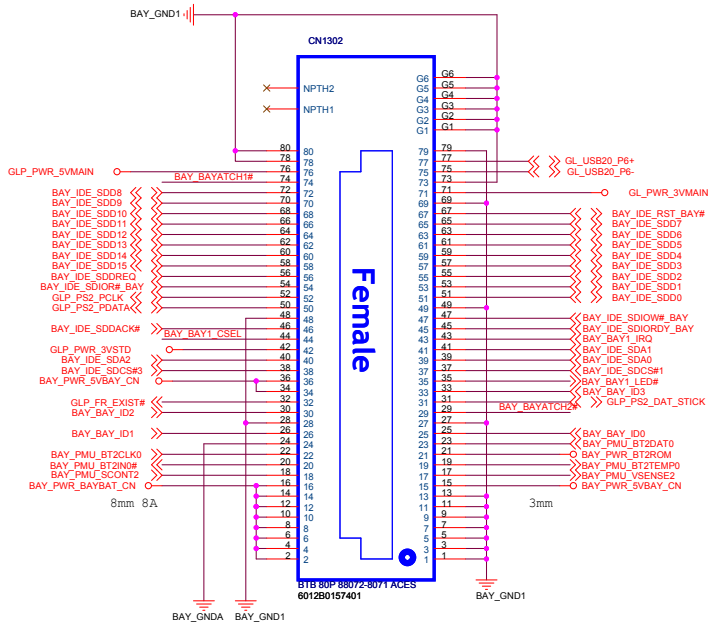

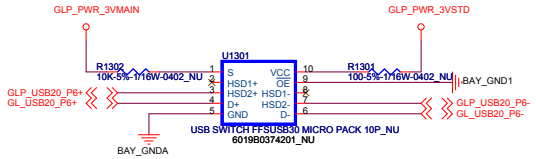

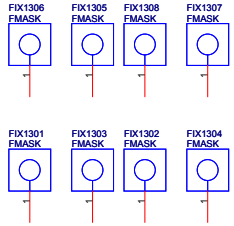

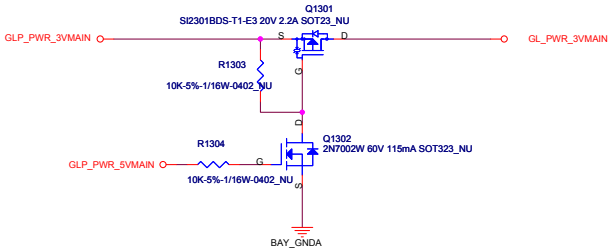

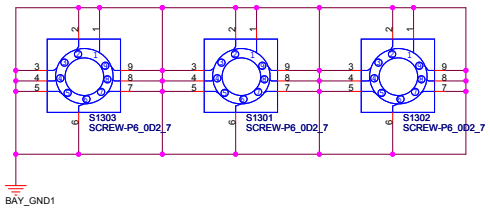

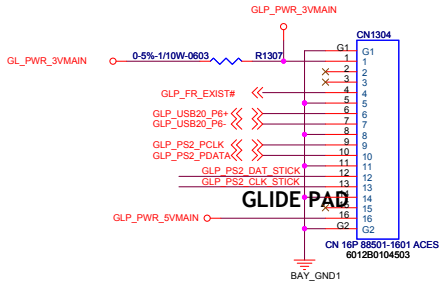

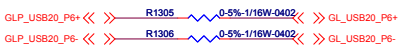

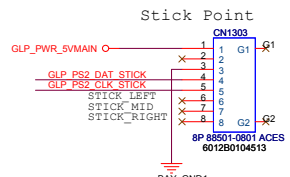

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5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 112?0, Taiwan
<OrgAddr4> TEL:+886-2-2881-0721

Title: J11Eagle(Merom+Crestline+ICH8M)

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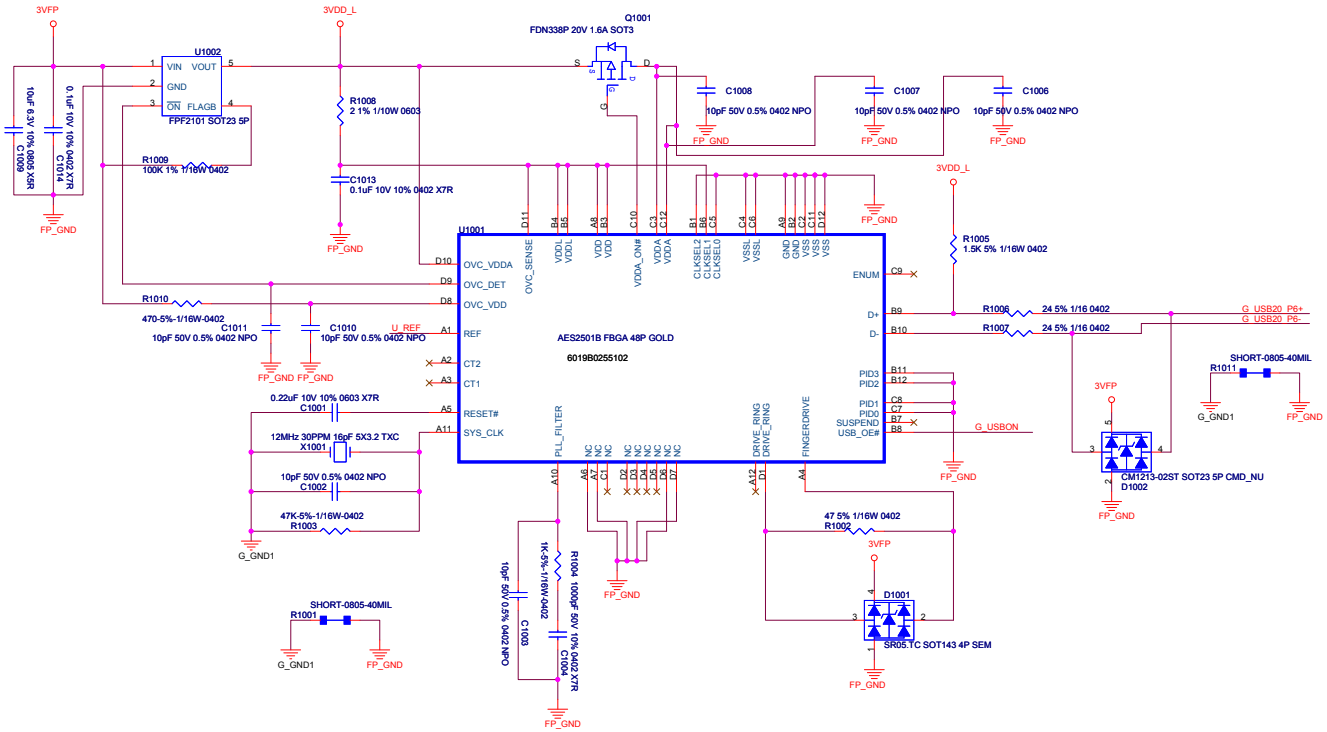
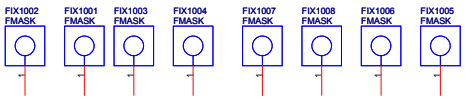
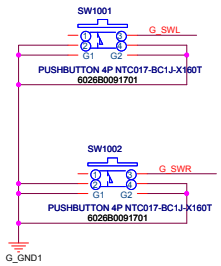
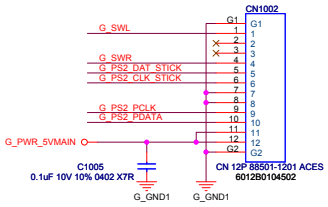


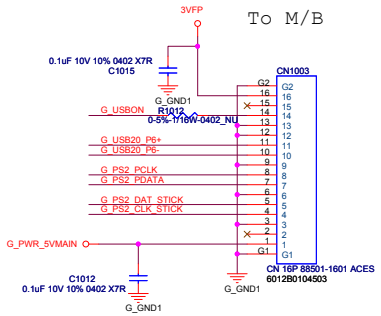




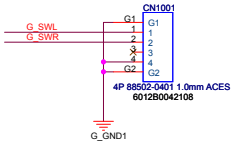
To Glide Pad



To M/B



To Stick switch board



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5F, No. 35, Section 2, Zhongyang South Road
Beitou District, Taipei 11270, Taiwan
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Title: J11Eagle(Merom+Crestline+ICH8M)

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Custom	GLIDE SW BOARD	0.4

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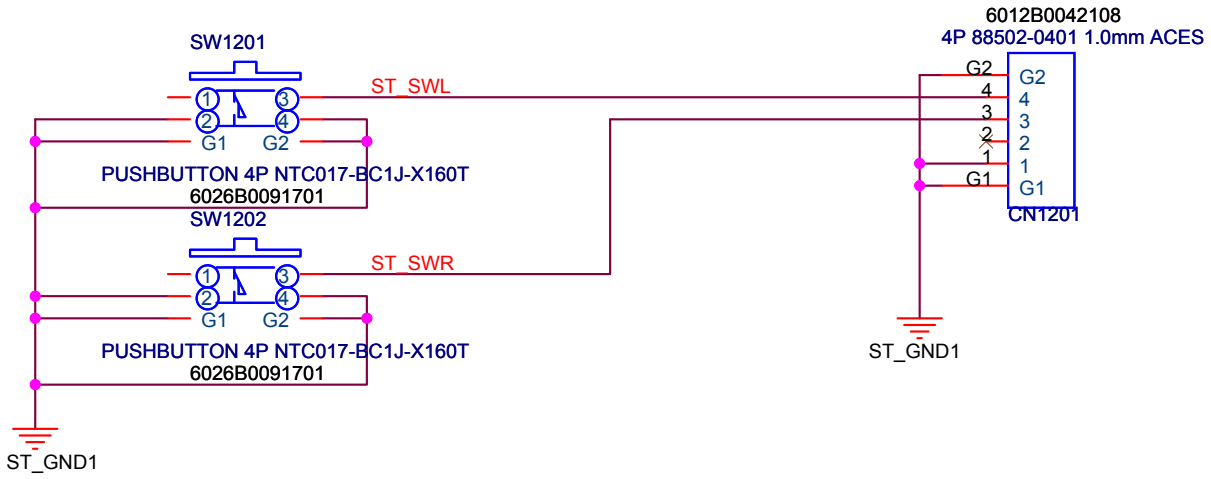
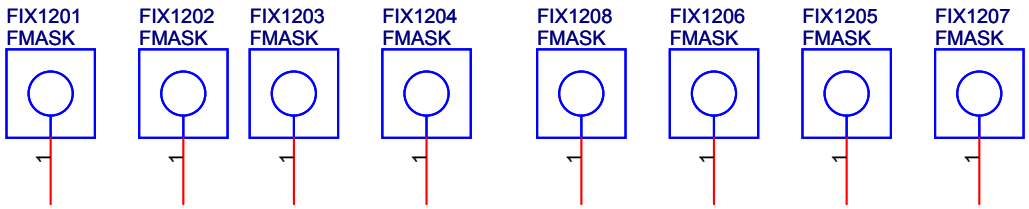
To Glide Pad switch board





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<OrgAddr4>

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Title

J11Eagle(Merom+Crestline+ICH8M)

Size	Document Number	Rev
A	STICK SW BOARD	0.4

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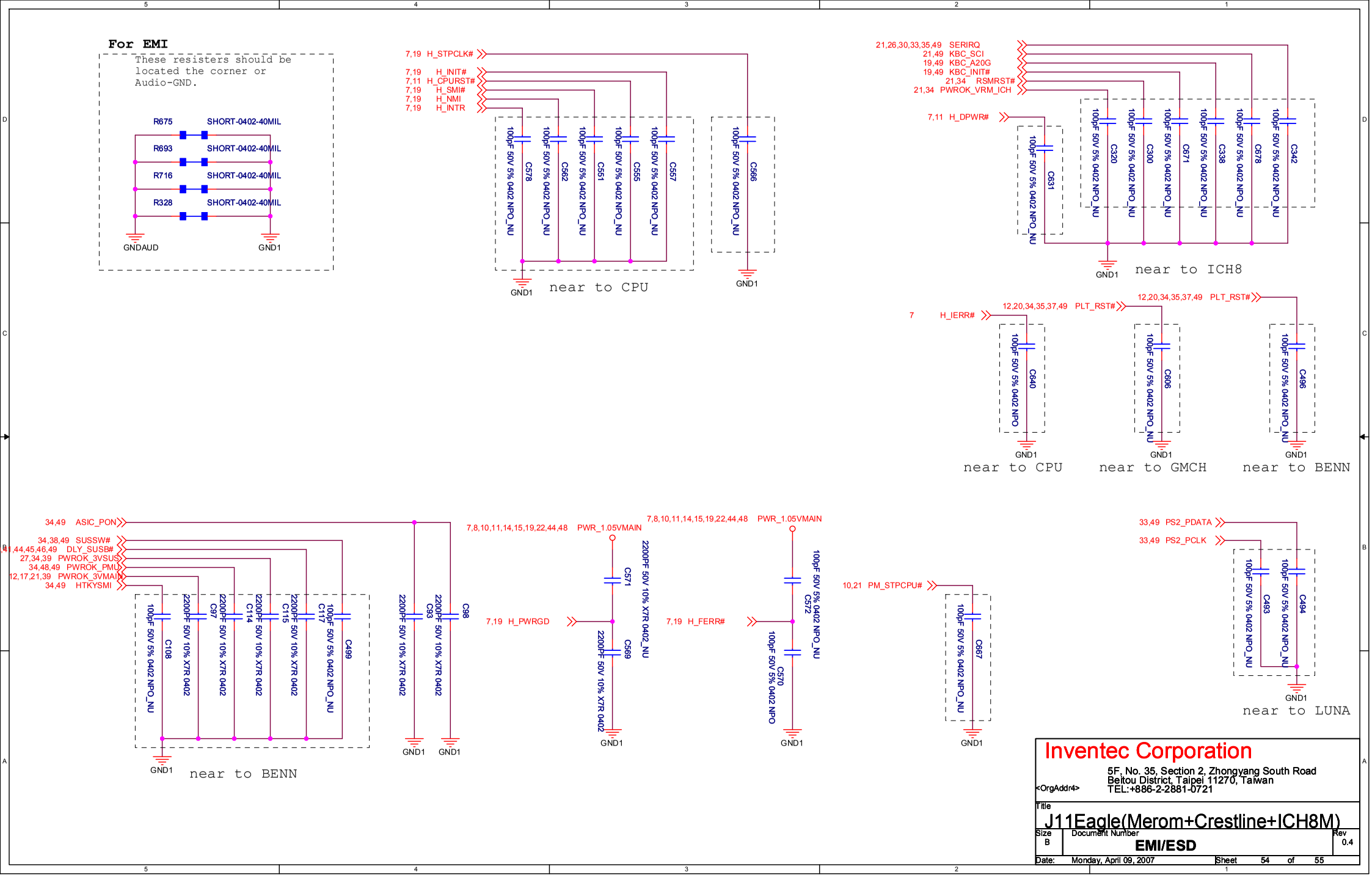
For EMI
These resisters should be located the corner or Audio-GND.
R675 SHORT-0402-40MIL
R693 SHORT-0402-40MIL
R716 SHORT-0402-40MIL
R328 SHORT-0402-40MIL
GNDAUD
GND1
7,19 H_STPCLK#
7,19 H_INIT#
7,11 H_CPURST#
7,19 H_SMI#
7,19 H_NMI
7,19 H_INTR
100pF 50V 5% 0402 NPO_NU C578
100pF 50V 5% 0402 NPO_NU C562
100pF 50V 5% 0402 NPO_NU C551
100pF 50V 5% 0402 NPO_NU C555
100pF 50V 5% 0402 NPO_NU C557
100pF 50V 5% 0402 NPO_NU C566
near to CPU
21,26,30,33,35,49 SERIRQ
21,49 KBC_SCI
19,49 KBC_A20G
19,49 KBC_INIT#
21,34 RSMRST#
21,34 PWROK_VRM_ICH
7,11 H_DPWR#
100pF 50V 5% 0402 NPO_NU C631
100pF 50V 5% 0402 NPO_NU C320
100pF 50V 5% 0402 NPO_NU C300
100pF 50V 5% 0402 NPO_NU C671
100pF 50V 5% 0402 NPO_NU C338
100pF 50V 5% 0402 NPO_NU C678
100pF 50V 5% 0402 NPO_NU C342
near to ICH8
7 H_IERR#
12,20,34,35,37,49 PLT_RST#
12,20,34,35,37,49 PLT_RST#
100pF 50V 5% 0402 NPO C640
100pF 50V 5% 0402 NPO_NU C606
100pF 50V 5% 0402 NPO_NU C496
near to CPU
near to GMCH
near to BENN
34,49 ASIC_PON
34,38,49 SUSSW#
1,44,45,46,49 DLY_SUSB#
27,34,39 PWROK_3VSUS
34,48,49 PWROK_PMU
12,17,21,39 PWROK_3VMAIN
34,49 HTKYSMI
100pF 50V 5% 0402 NPO_NU C108
2200PF 50V 10% X7R 0402 C97
2200PF 50V 10% X7R 0402 C114
2200PF 50V 10% X7R 0402 C115
2200PF 50V 10% X7R 0402 C117
100pF 50V 5% 0402 NPO_NU C499
2200PF 50V 10% X7R 0402 C93
2200PF 50V 10% X7R 0402 C98
near to BENN
7,8,10,11,14,15,19,22,44,48 PWR_1.05VMAIN
C571 2200PF 50V 10% X7R 0402_NU
7,19 H_PWRGD
C569 2200PF 50V 10% X7R 0402
7,8,10,11,14,15,19,22,44,48 PWR_1.05VMAIN
100pF 50V 5% 0402 NPO_NU C572
7,19 H_FERR#
C570 100pF 50V 5% 0402 NPO
10,21 PM_STPCPU#
100pF 50V 5% 0402 NPO_NU C667
33,49 PS2_PDATA
33,49 PS2_PCLK
100pF 50V 5% 0402 NPO_NU C493
100pF 50V 5% 0402 NPO_NU C494
near to LUNA
Inventec Corporation
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Beitou District, Taipei 11270, Taiwan
TEL:+886-2-2881-0721
<OrgAddr4>
Title
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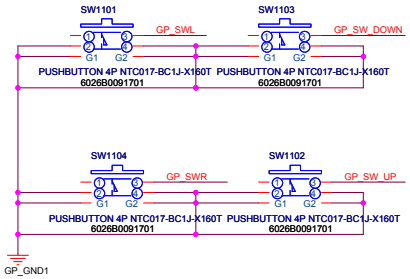
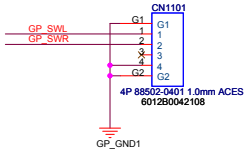
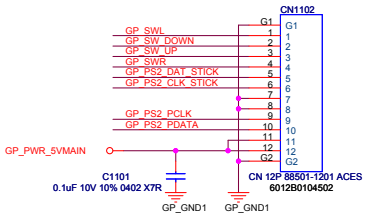
Size B
Document Number
EMI/ESD
Rev 0.4
Date: Monday, April 09, 2007
Sheet 54 of 55



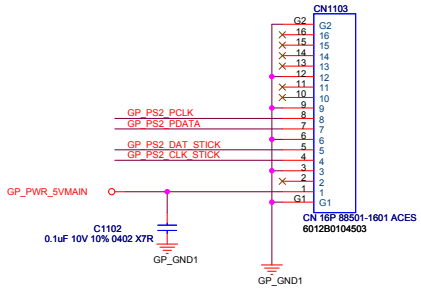
To Stick switch board

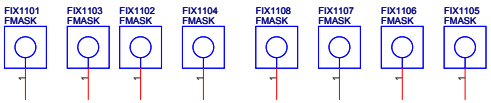


To Glide Pad



To M/B





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Size	Document Number	Rev
C	GLIDE SW BOARD W/O FP	0.4

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