Round Rock 13.3" Schematics Document

Haswell ULT

2013-06-28
REV : SSI

DY : None Installed
XDP: For CPU XDP Debug Port installed
PCH_XDP: For PCH XDP Debug Port installed

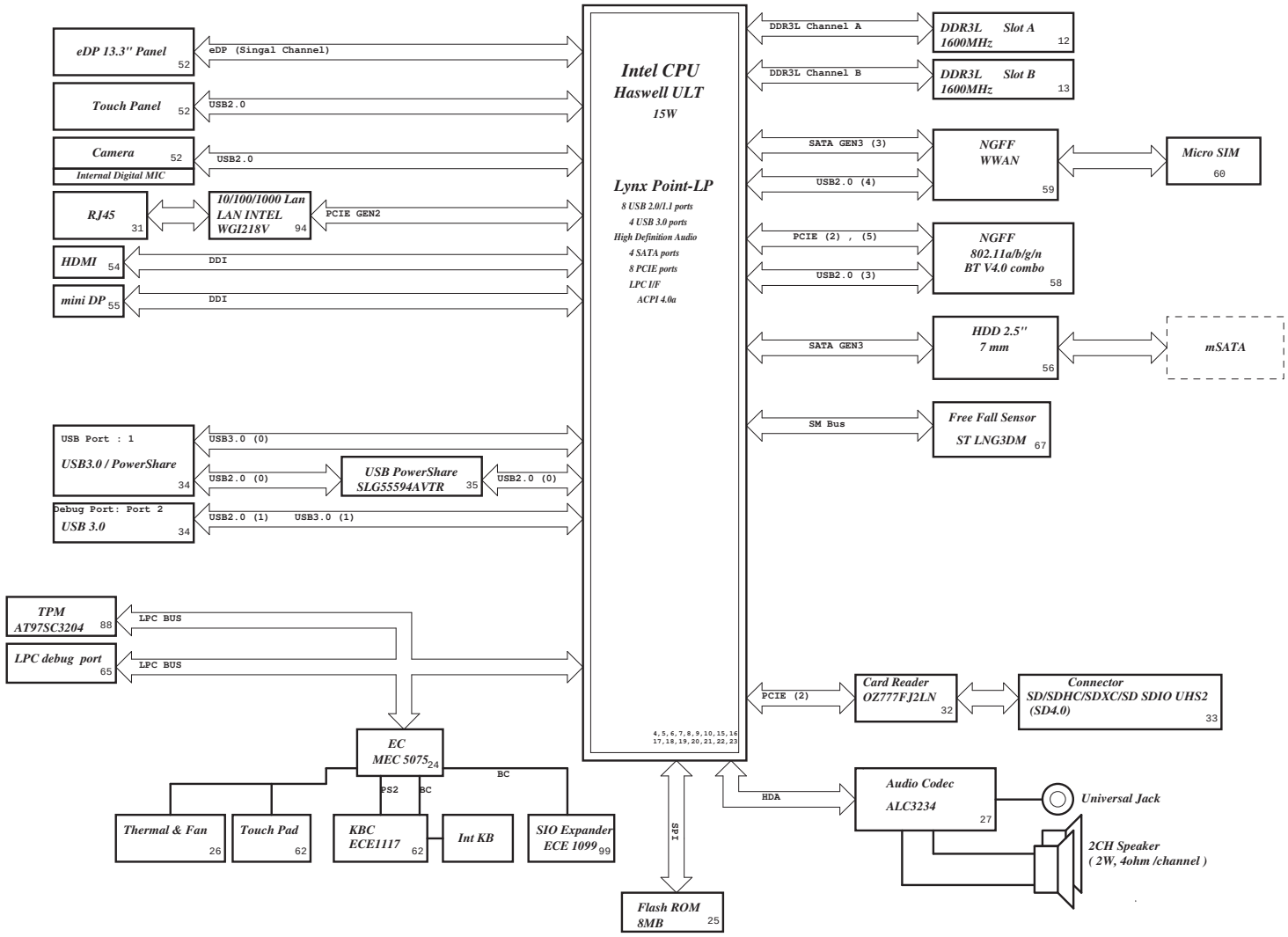
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	*Cover Page*	
Size: A3	Document Number: *Round Rock 13.3" UMA*	Rev: *X00*
Date: Friday, June 28, 2013	Sheet 1 of 107	

Round Rock 13.3" Block Diagram

Project code : 91.4OA01.001
PCB P/N : 13229
Revision : X00



CHARGER BQ24715	44
INPUTS	OUTPUTS
AD+ BT+	DCBATOUT

SYSTEM DC/DC TPS51275	45
INPUTS	OUTPUTS
DCBATOUT	3D3V_AUX_S5 3D3V_S5 5V_S5

CPU DC/DC TPS51622	46~47
INPUTS	OUTPUTS
DCBATOUT	VCC_CORE

SYSTEM DC/DC TPS51363	48
INPUTS	OUTPUTS
DCBATOUT	1D05V_M

SYSTEM DC/DC TPS51363 & APL5338	49
INPUTS	OUTPUTS
DCBATOUT	1D35V_S3 0D675V_S0 DDR_VREF_S3

Load Switches	36
INPUTS	OUTPUTS
5V_S5	5V_S0
3D3V_S5	3D3V_S0 3D3V_S5_PCH 3D3V_M 3D3V_LAN 1D05V_MODPHY
1D05V_M	1D05V_S0

PCB LAYER(FR4-6 Layer)	
L1:Top L2:PWR/GND L3:Signal L4:Signal L5:PWR/GND	L6:Bottom

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Title: Block Diagram

Size	Document Number	Rev
A2	Round Rock 13.3" UMA	X00

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Title	***CPU (PCIE/DMI/FDI)***	
Size: A4	Document Number: ***Round Rock 13.3" UMA***	Rev: ***X00***
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SSID = CPU

+V1.05S_VCCST

R401 1 2 62R2J-GP H_PROCHOT#

99 CPU_DETECT# R403 1 2 0R2J-2-GP PROC_DETECT# D61
24 H_PECI R402 1 2 0R2J-2-GP TP402 1 H_CATERR# K61
H_PECI_R N62
24,42,44,46 H_PROHOT# R404 1 2 56R2J-4-GP H_PROCHOT#_R K62
R405 1 2 10KR2J-3-GP H_CPUPWRGD C61
SSI_0625 EC401 DY SC1KP50V2KX-1GP
SM_RCOMP_0 AU60
SM_RCOMP_1 AV60
SM_RCOMP_2 AU61
SM_DRAMRST# AV15
AV61
14 DDR_PG_CTRL

CPU1B 2 OF 19

PROC_DETECT# MISC
CATERR#
PECI
PROCHOT# THERMAL
PROCPWRGD PWR
SM_RCOMP0 DDR3
SM_RCOMP1
SM_RCOMP2
SM_DRAMRST#
SM_PG_CNTL1

HASWELL-3-GP-U

JTAG

PRDY# J62 XDP_PRDY# 96
PREQ# K62 XDP_PREQ# 96
PROC_TCK E60 XDP_TCK 96
PROC_TMS E61 XDP_TMS 96
PROC_TRST# E59 XDP_TRST# 19,96
PROC_TDI F63 XDP_TDI 96
PROC_TDO F62 XDP_TDO 96

BPM#0 J60 XDP_BPM0 XDP_BPM0 96
BPM#1 H60 XDP_BPM1 XDP_BPM1 96
BPM#2 H61 XDP_BPM2 TP401
BPM#3 H62 XDP_BPM3 TP403
BPM#4 K59 XDP_BPM4 TP404
BPM#5 H63 XDP_BPM5 TP405
BPM#6 K60 XDP_BPM6 TP406
BPM#7 J61 XDP_BPM7 TP407

Design Guideline:
SM_RCOMP keep routing length less than 500 mils.

R408 1 2 200R2F-L-GP SM_RCOMP_0
R410 1 2 120R2F-GP SM_RCOMP_1
R411 1 2 100R2F-L1-GP-U SM_RCOMP_2

1D05V_M

XDP_TMS R406 1 XDP 2 51R2J-2-GP
XDP_TDI R407 1 XDP 2 51R2J-2-GP
XDP_TDO R409 1 XDP 2 51R2J-2-GP

XDP_TCK R412 1 DY 2 51R2J-2-GP
XDP_TRST# R413 1 DY 2 51R2J-2-GP

XDP_BPM0 R414 1 DY 2 0R2J-2-GP XDP_BPM1

Layout Note: Colse to DIMM

1D35V_S3

R415
470R2J-2-GP

SM_DRAMRST# R416 1 2 0R2J-2-GP DDR3_DRAMRST#_1 12
R417 1 2 0R2J-2-GP DDR3_DRAMRST#_2 13

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Title: CPU (THERMAL/CLOCK/PM)

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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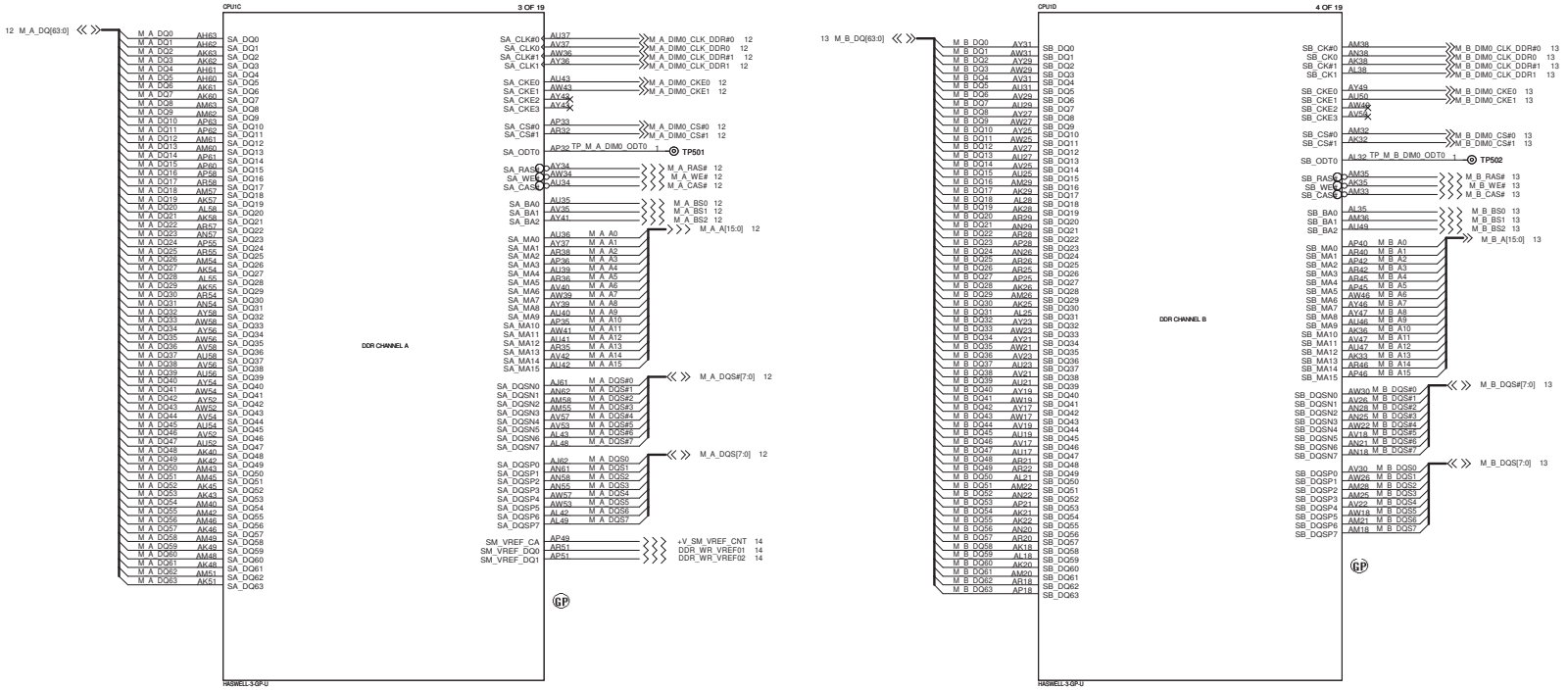
SSID = CPU



<Core Design>

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Title: CPU (DDR)

Size: A2 | Document Number: Round Rock 13.3" UMA | Rev: X00

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SSID = CPU

EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE	
CFG0	0:Lane Reversed 1:(Default) Normal Operation; No stall

CFG0 — R601 1KR2J-1-GP

PCH/PCH LESS MODE SELECTION	
CFG1	0:Lane Reversed 1:(Default) Normal Operation

CFG1 — R602 1KR2J-1-GP

X01-20130204

Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

CFG4 — R606 1KR2J-1-GP

ALLOW THE USE OF NOA ON LOCKED UNITS	
CFG8	1: Enable(Default): Noa will be disable in locked units and enable in un-locked units 0: Enable Noa will be available pegardless of the locking of the unit

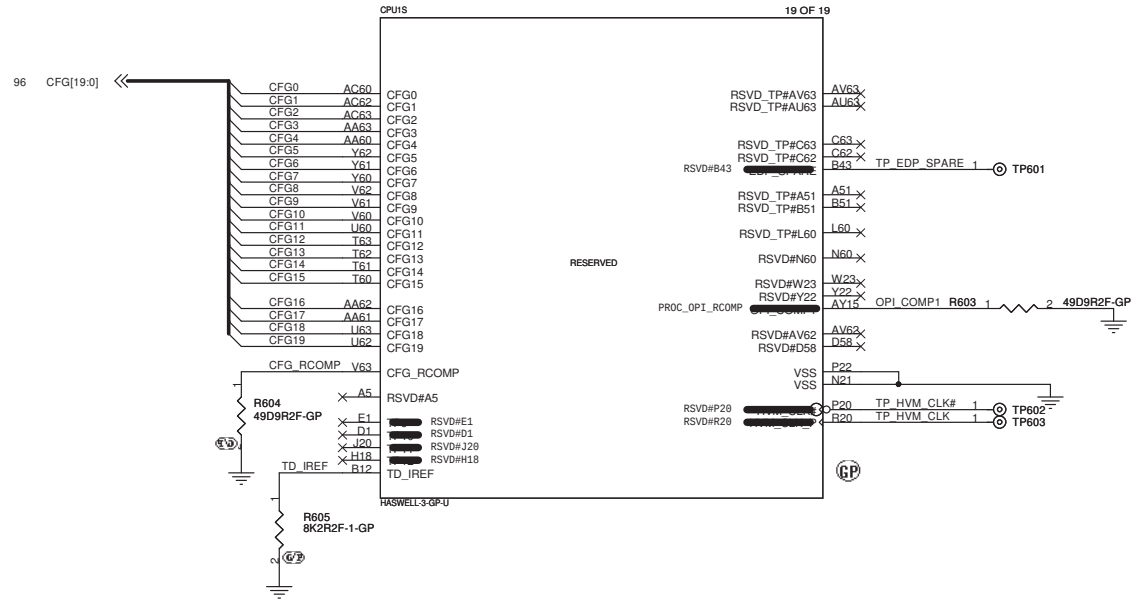
CFG8 — R607 1KR2J-1-GP

NO SVID PROTOCOL CAPABLE VR CONNECTED	
CFG9	1: VRS support SVID protocol are present 0:No VR support SVID is present The chip will not generate(OR Respond to) SVID activity

CFG9 — R608 1KR2J-1-GP

SAFE MODE BOOT	
CFG10	1: POWER FEATURES ACTIVATED DURING RESET 0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED

CFG10 — R609 1KR2J-1-GP



<Core Design>

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Title: CPU (RESERVED)

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	X00

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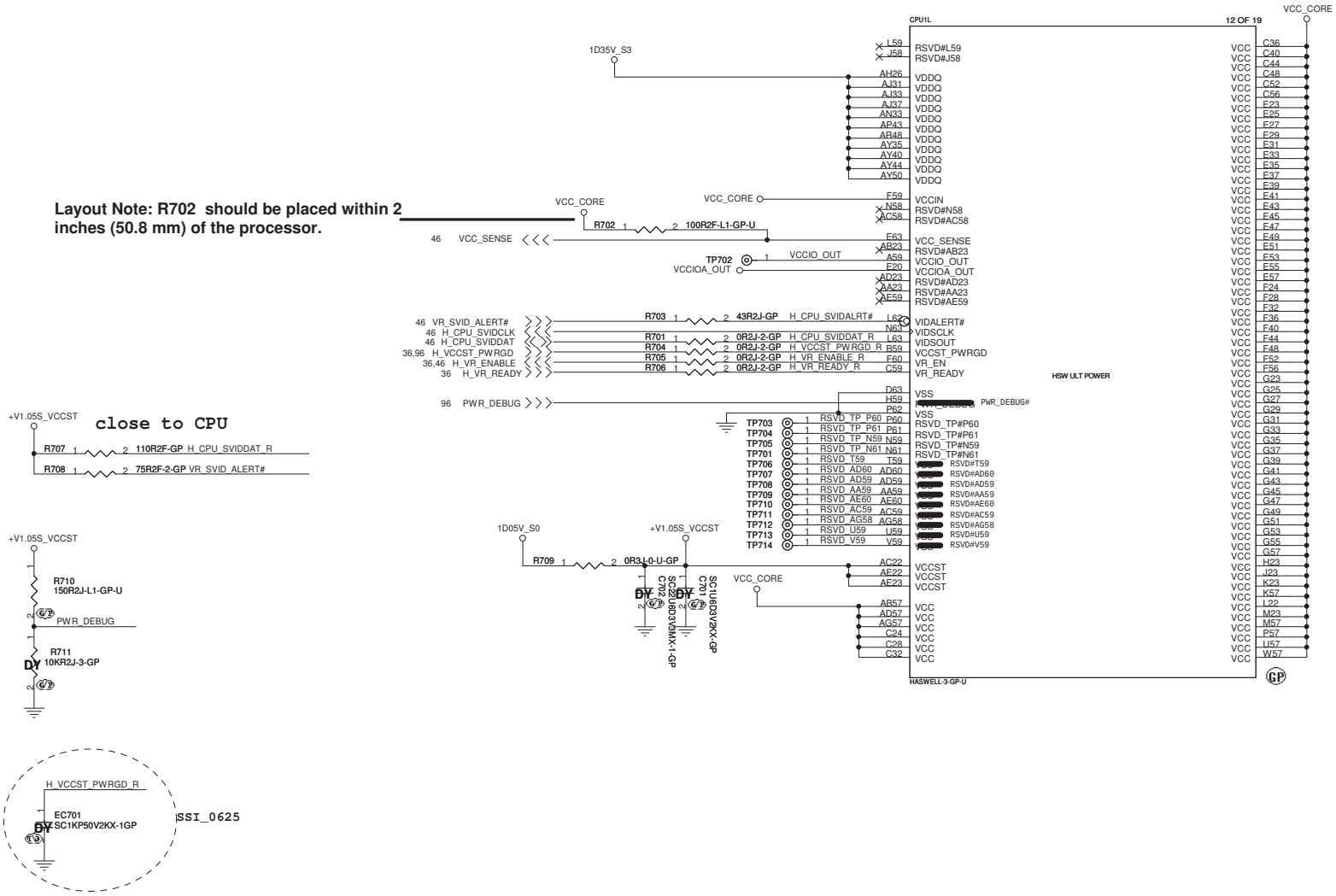
SSID = CPU



<Core Design>

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Title	CPU (VCC_CORE)	
Size: Custom	Document Number: Round Rock 13.3" UMA	Rev: X00
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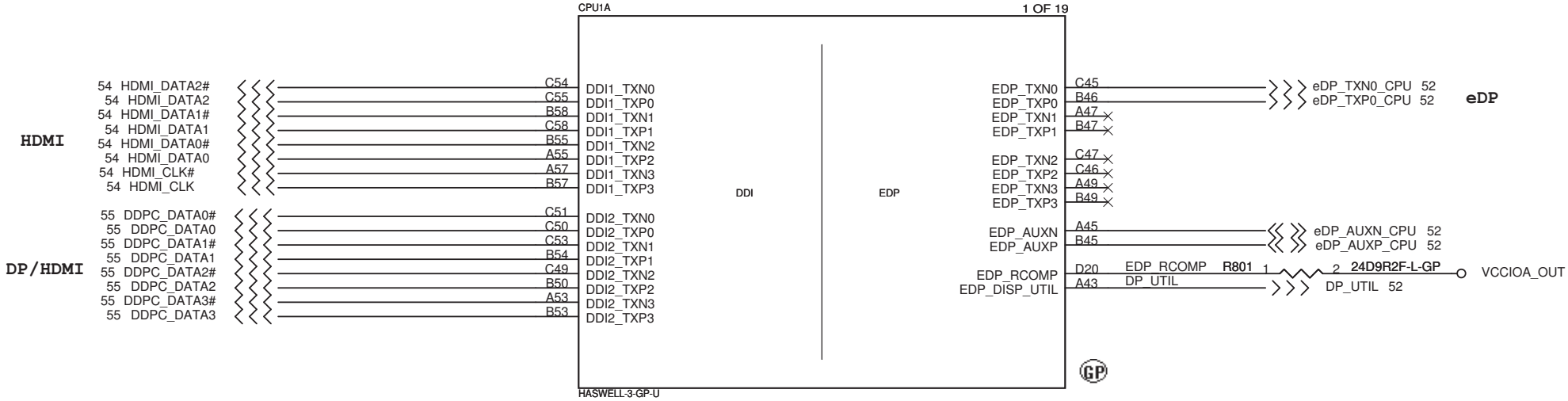
SSID = CPU



DDI	HDMI	Display Port
DDI_TXN0	HDMI_DATA2_N	DP_LANE0_N
DDI_TXP0	HDMI_DATA2_P	DP_LANE0_P
DDI_TXN1	HDMI_DATA1_N	DP_LANE1_N
DDI_TXP1	HDMI_DATA1_P	DP_LANE1_P
DDI_TXN2	HDMI_DATA0_N	DP_LANE2_N
DDI_TXP2	HDMI_DATA0_P	DP_LANE2_P
DDI_TXN3	HDMI_CK_N	DP_LANE3_N
DDI_TXP3	HDMI_CK_P	DP_LANE3_P

<Core Design>

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Title: ***CPU (DDI/EDP)***

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

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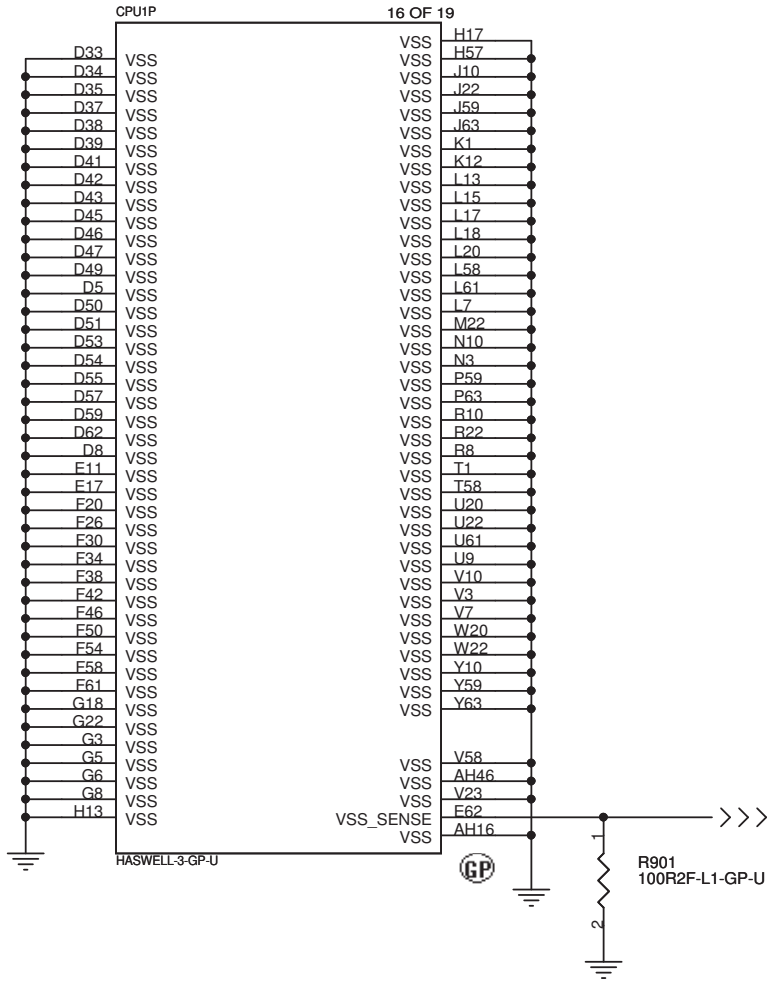
SSID = CPU



Layout Note: R901 should be placed within 2 inches (50.8 mm) of the processor.
Net Rule: VCC_SENSE and VSS_SENSE differential signals

<Core Design>

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Title: ***CPU (VSS)***

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

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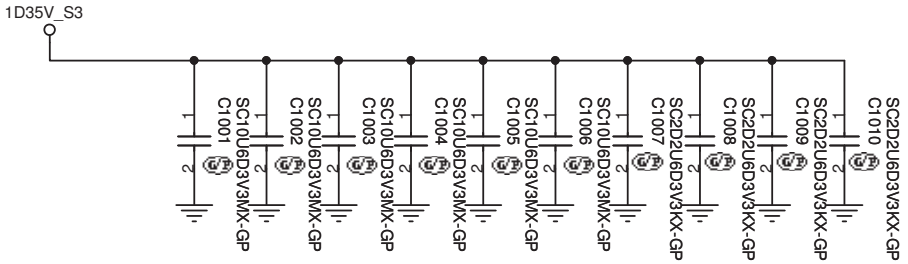

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Title: ***CPU (Power CAP1)***

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

Date: Friday, June 28, 2013 Sheet 10 of 107

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<Core Design>

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Title	CPU (Power CAP2)	
Size: A	Document Number: Round Rock 13.3" UMA	Rev: X00
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SSID = MEMORY

DQS1	DQ0 M_A_DQ13 DQ1 M_A_DQ8 DQ2 M_A_DQ14 DQ3 M_A_DQ10 DQ4 M_A_DQ9 DQ5 M_A_DQ12 DQ6 M_A_DQ15 DQ7 M_A_DQ11
DQS3	DQ8 M_A_DQ29 DQ9 M_A_DQ28 DQ10 M_A_DQ30 DQ11 M_A_DQ31 DQ12 M_A_DQ25 DQ13 M_A_DQ24 DQ14 M_A_DQ27 DQ15 M_A_DQ26
DQS5	DQ16 M_A_DQ44 DQ17 M_A_DQ41 DQ18 M_A_DQ43 DQ19 M_A_DQ47 DQ20 M_A_DQ45 DQ21 M_A_DQ40 DQ22 M_A_DQ42 DQ23 M_A_DQ46
DQS6	DQ24 M_A_DQ51 DQ25 M_A_DQ50 DQ26 M_A_DQ49 DQ27 M_A_DQ48 DQ28 M_A_DQ52 DQ29 M_A_DQ53 DQ30 M_A_DQ54 DQ31 M_A_DQ55
DQS0	DQ32 M_A_DQ0 DQ33 M_A_DQ1 DQ34 M_A_DQ2 DQ35 M_A_DQ6 DQ36 M_A_DQ5 DQ37 M_A_DQ4 DQ38 M_A_DQ3 DQ39 M_A_DQ7
DQS2	DQ40 M_A_DQ21 DQ41 M_A_DQ20 DQ42 M_A_DQ17 DQ43 M_A_DQ16 DQ44 M_A_DQ18 DQ45 M_A_DQ19 DQ46 M_A_DQ22 DQ47 M_A_DQ23
DQS4	DQ48 M_A_DQ36 DQ49 M_A_DQ33 DQ50 M_A_DQ34 DQ51 M_A_DQ38 DQ52 M_A_DQ37 DQ53 M_A_DQ32 DQ54 M_A_DQ35 DQ55 M_A_DQ39
DQS7	DQ56 M_A_DQ62 DQ57 M_A_DQ58 DQ58 M_A_DQ60 DQ59 M_A_DQ61 DQ60 M_A_DQ63 DQ61 M_A_DQ59 DQ62 M_A_DQ56 DQ63 M_A_DQ57

Layout Note:
Place these caps close to VREF_CA

M_VREF_CA_DIMMA

SCD1U10V2KX-5GP C1201

Layout Note:
Place these caps close to VREF_DQ

M_VREF_DQ_DIMMA

SCD1U10V2KX-5GP C1204 · SC2R2U10V3KX-1GP C1205 · SCD1U10V2KX-5GP C1206

0D675V_S0

Place these caps close to VTT1 and VTT2.

SC10U6D3V2KX-6GP C1217 · SC10U6D3V2KX-6GP C1218 · SC10U6D3V2KX-6GP C1219

DM1

5 M_A_A[15:0] → M_A_A0 … M_A_A15 → A0 … A15, A16/BA2

NP1, NP2

RAS# 110 → M_A_RAS# 5
WE# 113 → M_A_WE# 5
CAS# 115 → M_A_CAS# 5

CS0# 114 → M_A_DIM0_CS#0 5
CS1# 121 → M_A_DIM0_CS#1 5

CKE0 73 → M_A_DIM0_CKE0 5
CKE1 74 → M_A_DIM0_CKE1 5

CK0 101 → M_A_DIM0_CLK_DDR0 5
CK0# 103 → M_A_DIM0_CLK_DDR#0 5

CK1 102 → M_A_DIM0_CLK_DDR1 5
CK1# 104 → M_A_DIM0_CLK_DDR#1 5

5 M_A_BS2 → BA0
5 M_A_BS0 → BA1
5 M_A_BS1
5 M_A_DQ[63:0] → M_A_DQ0 … M_A_DQ63 → DQ0 … DQ63

DM0 11, DM1 28, DM2 46, DM3 63, DM4 136, DM5 153, DM6 170, DM7 187

SDA 200 → PCH_SMBDATA 13,18,67,96
SCL 202 → PCH_SMBCLK 13,18,67,96

EVENT# 198

VDDSPD 199 ← 3D3V_S0

C1203 SCD1U10V2KX-5GP

SA0 197, SA1 201

NC#1 77, NC#2 122, NC#TEST 125

1D05V_S3 → VDD1 75, VDD2 76, VDD3 81, VDD4 82, VDD5 87, VDD6 88, VDD7 93, VDD8 94, VDD9 99, VDD10 100, VDD11 105, VDD12 106, VDD13 111, VDD14 112, VDD15 117, VDD16 118, VDD17 123, VDD18 124

VSS 2, 3, 8, 9, 13, 14, 19, 20, 25, 26, 31, 32, 37, 38, 43, 44, 48, 49, 54, 55, 60, 61, 65, 66, 71, 72, 127, 128, 133, 134, 138, 139, 144, 145, 150, 151, 155, 156, 161, 162, 167, 168, 172, 173, 178, 179, 184, 185, 189, 190, 195, 196, 205, 206

M_A_DQS#1 10, M_A_DQS#3 27, M_A_DQS#5 45, M_A_DQS#6 62, M_A_DQS#0 135, M_A_DQS#2 152, M_A_DQS#4 169, M_A_DQS#7 186 → DQS0# … DQS7#

5 M_A_DQS#[7:0]

M_A_DQS1 12, M_A_DQS3 29, M_A_DQS5 47, M_A_DQS6 64, M_A_DQS0 137, M_A_DQS2 154, M_A_DQS4 171, M_A_DQS7 188 → DQS0 … DQS7

5 M_A_DQS[7:0]

14 M_A_DIM0_ODT0 → ODT0 116
14 M_A_DIM0_ODT1 → ODT1 120

M_VREF_CA_DIMMA → VREF_CA 126
M_VREF_DQ_DIMMA → VREF_DQ 1

4 DDR3_DRAMRST#_1 → RESET# 30

SCD1U10V2KX-5GP C1220 · 0D675V_S0 → VTT1 203, VTT2 204

H =4mm

DDR3-204P-106-GP
62.10017.X31
2nd = 62.10024.G11

Note:
If SA0 DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0 DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32

1D05V_S3

DM1 DECOUPLING

SC10U6D3V3MX-GP C1207 · SC10U6D3V3MX-GP C1208 · SC10U6D3V3MX-GP C1209 · SC10U6D3V3MX-GP C1210 · SC10U6D3V3MX-GP C1211 · SC10U6D3V3MX-GP C1212 · SC10U6D3V3MX-GP C1213 · SC10U6D3V3MX-GP C1214

Layout Note:
Place these Caps near DM1.

SCD1U10V2KX-5GP C1215 · SCD1U10V2KX-5GP C1216

<Core Design>

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Title: **DDR3L-SODIMM1**

Size: A2 | Document Number: **Round Rock 13.3" UMA** | Rev: **X00**

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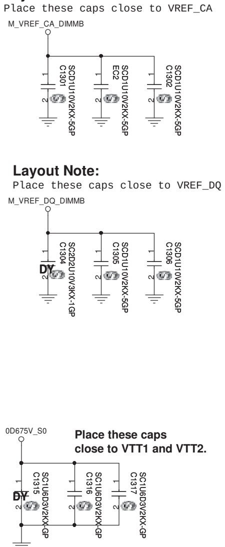
SSID = MEMORY

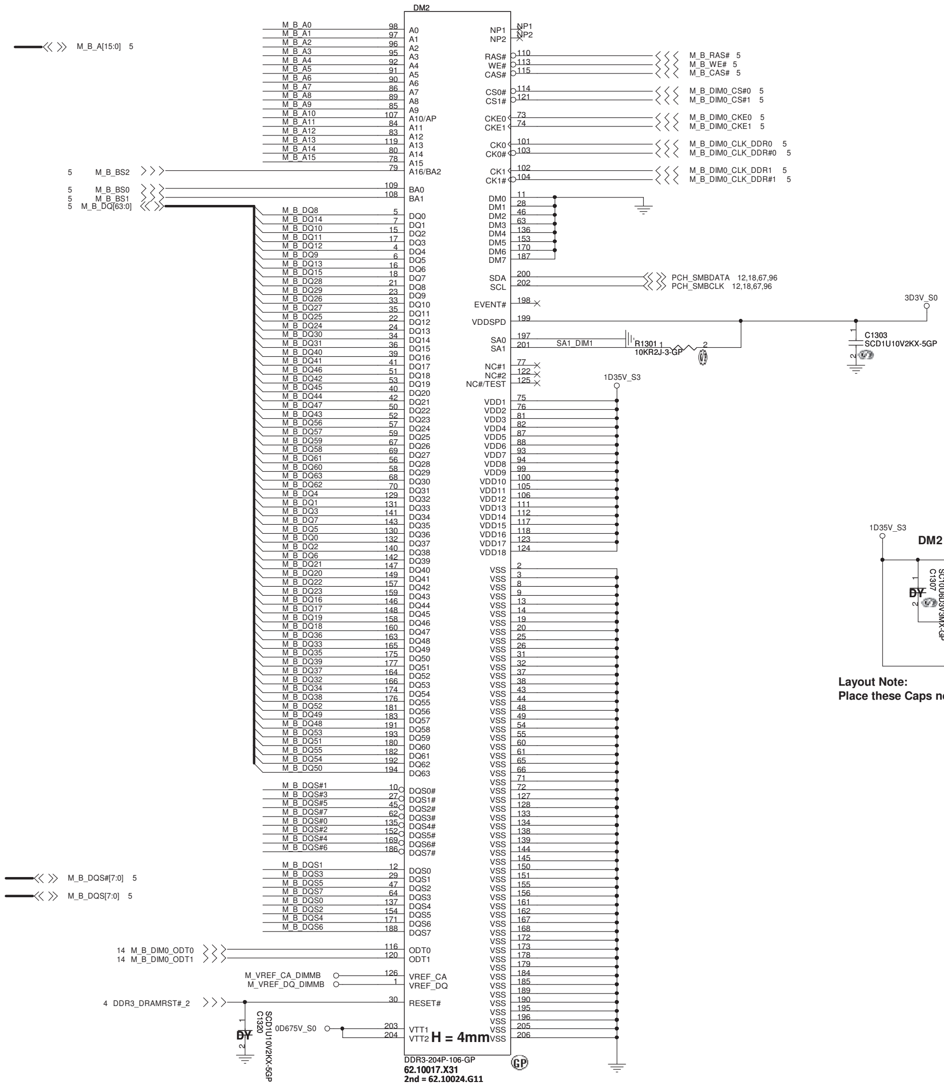
Layout Note:
Place these caps close to VREF_CA

Layout Note:
Place these caps close to VREF_DQ

Place these caps close to VTT1 and VTT2.



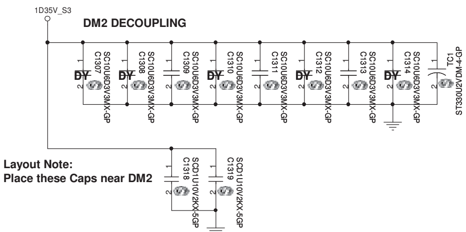
DQS1	DQ0	M_B_DQ8
	DQ1	M_B_DQ14
	DQ2	M_B_DQ10
	DQ3	M_B_DQ11
	DQ4	M_B_DQ12
	DQ5	M_B_DQ9
	DQ6	M_B_DQ13
	DQ7	M_B_DQ15
DQS3	DQ8	M_B_DQ28
	DQ9	M_B_DQ29
	DQ10	M_B_DQ26
	DQ11	M_B_DQ27
	DQ12	M_B_DQ25
	DQ13	M_B_DQ24
	DQ14	M_B_DQ30
	DQ15	M_B_DQ31
DQS5	DQ16	M_A_DQ40
	DQ17	M_A_DQ41
	DQ18	M_A_DQ46
	DQ19	M_A_DQ42
	DQ20	M_A_DQ45
	DQ21	M_A_DQ44
	DQ22	M_A_DQ47
	DQ23	M_A_DQ43
DQS7	DQ24	M_A_DQ56
	DQ25	M_A_DQ57
	DQ26	M_A_DQ59
	DQ27	M_A_DQ58
	DQ28	M_A_DQ61
	DQ29	M_A_DQ60
	DQ30	M_A_DQ63
	DQ31	M_A_DQ62
DQS0	DQ32	M_A_DQ4
	DQ33	M_A_DQ1
	DQ34	M_A_DQ3
	DQ35	M_A_DQ7
	DQ36	M_A_DQ5
	DQ37	M_A_DQ0
	DQ38	M_A_DQ2
	DQ39	M_A_DQ6
DQS2	DQ40	M_A_DQ21
	DQ41	M_A_DQ20
	DQ42	M_A_DQ22
	DQ43	M_A_DQ23
	DQ44	M_A_DQ16
	DQ45	M_A_DQ17
	DQ46	M_A_DQ19
	DQ47	M_A_DQ18
DQS4	DQ48	M_A_DQ36
	DQ49	M_A_DQ33
	DQ50	M_A_DQ35
	DQ51	M_A_DQ39
	DQ52	M_A_DQ37
	DQ53	M_A_DQ32
	DQ54	M_A_DQ34
	DQ55	M_A_DQ38
DQS6	DQ56	M_A_DQ52
	DQ57	M_A_DQ49
	DQ58	M_A_DQ48
	DQ59	M_A_DQ53
	DQ60	M_A_DQ51
	DQ61	M_A_DQ55
	DQ62	M_A_DQ54
	DQ63	M_A_DQ50



Note:
SO-DIMMB SPD Address is 0xA4
SO-DIMMB TS Address is 0x34

SO-DIMMB is placed farther from the Processor than SO-DIMMA

DM2 DECOUPLING



Layout Note:
Place these Caps near DM2

<Core Design>

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Title		
DDR3L-SODIMM1		
Size A2	Document Number: *Round Rock 13.3" UMA*	Rev *X00*
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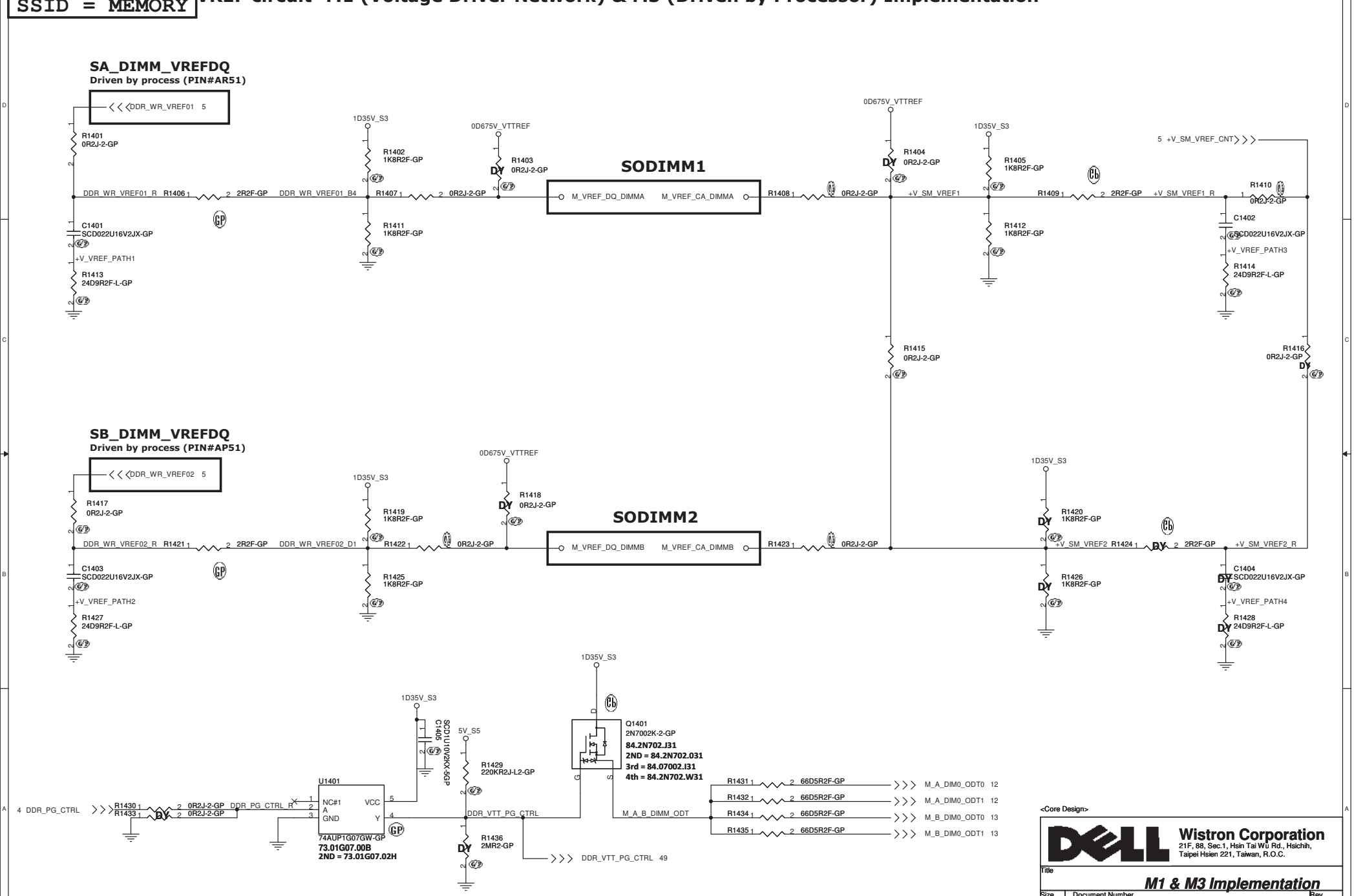
SSID = MEMORY

VREF circuit -M1 (Voltage Driver Network) & M3 (Driven by Processor) Implementation



<Core Design>

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Title: M1 & M3 Implementation

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

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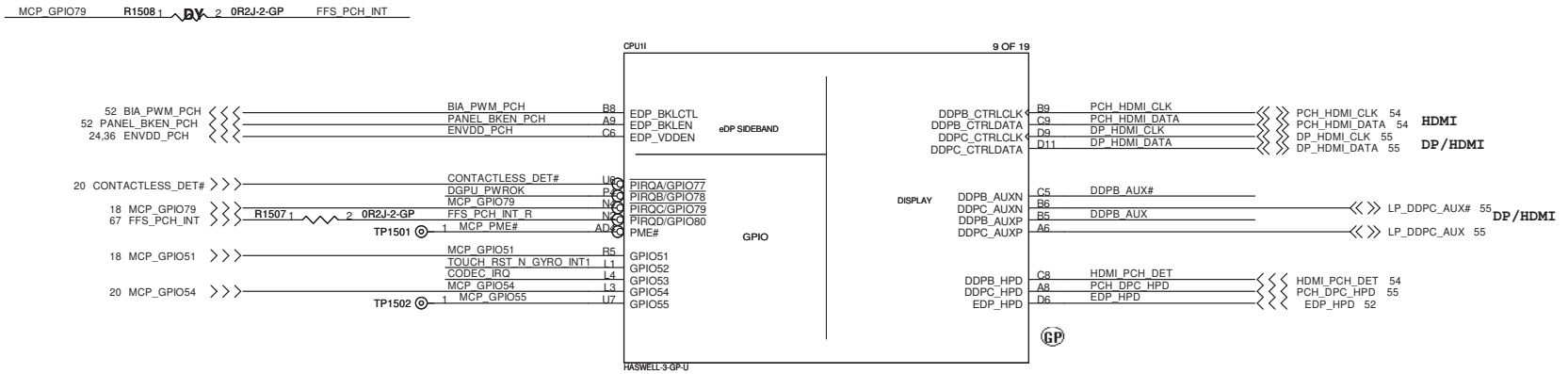

<Core Design>

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Title: CPU (/DDI/PCI)

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

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SSID = PCH

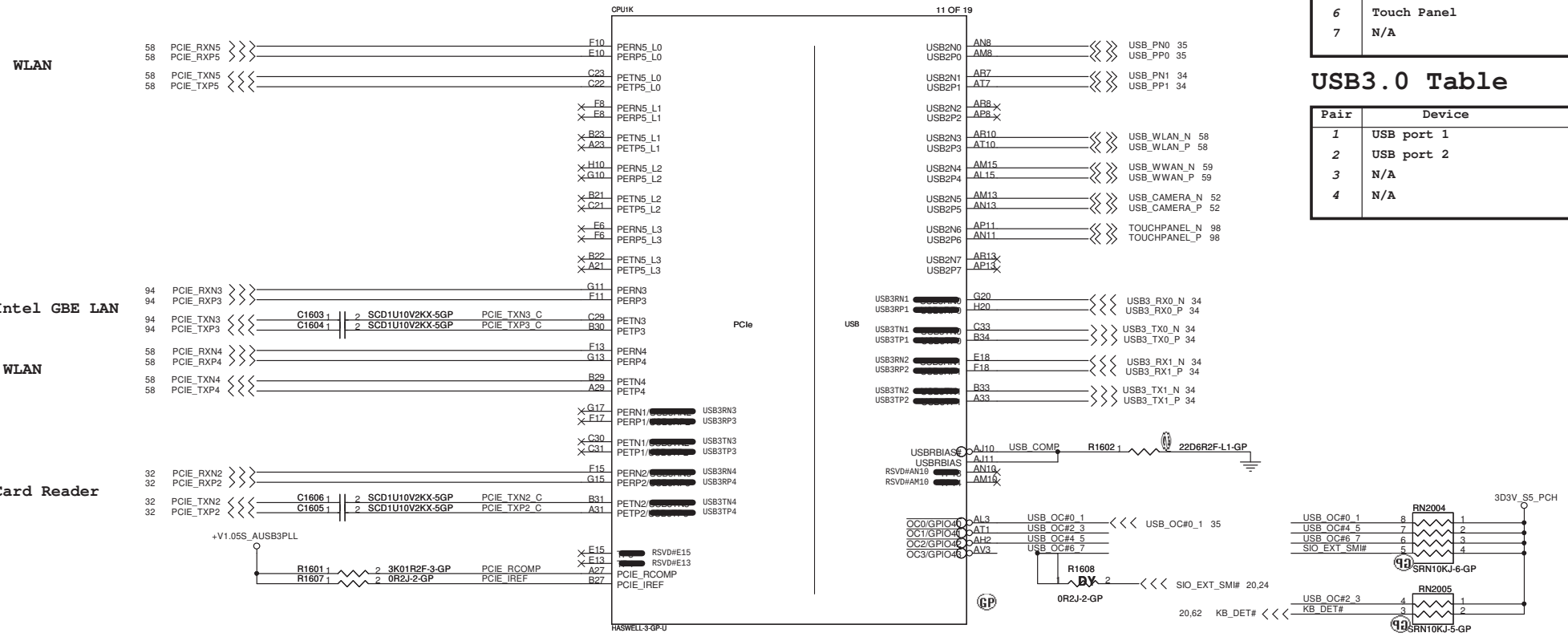
USB2.0 Table

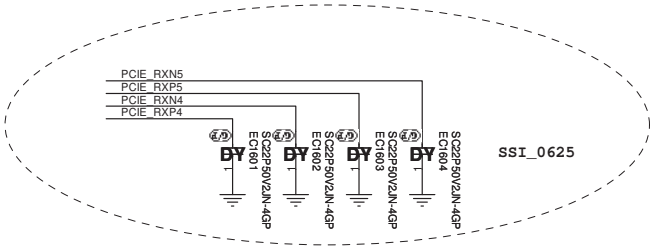
Pair	Device
0	USB port 2 (usb charger)
1	USB port 1 (win debug)
2	N/A
3	WLAN (BT)
4	WWAN
5	CAMERA
6	Touch Panel
7	N/A

USB3.0 Table

Pair	Device
1	USB port 1
2	USB port 2
3	N/A
4	N/A

Shark Bay ULT:
USB Ext. port 1
External debug port use on Shark Bay platform





<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

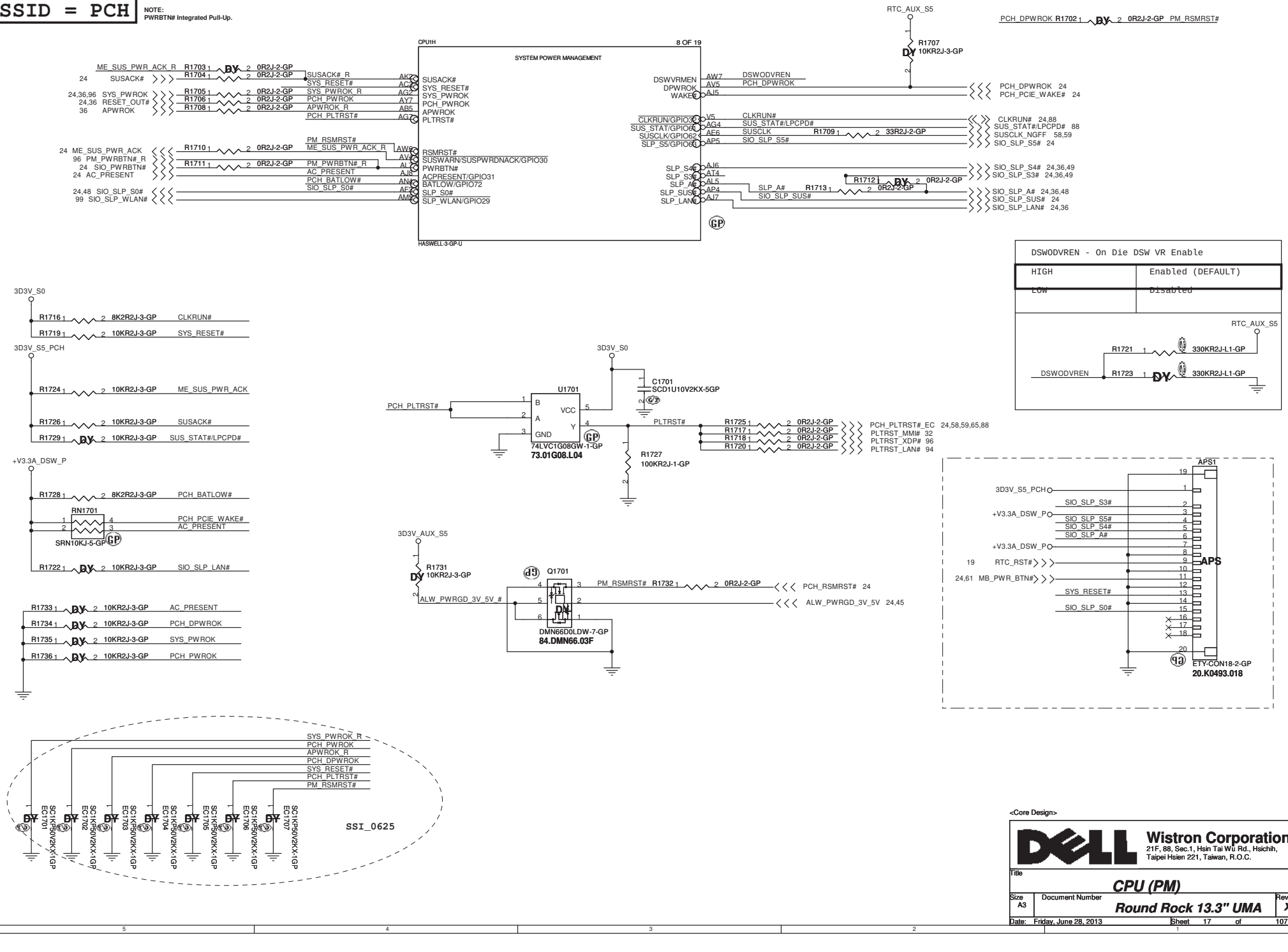
Title: CPU (PCIE/USB)

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 16 of 107

SSID = PCH

NOTE:
PWRBTN# Integrated Pull-Up.



DSWODVREN - On Die DSW VR Enable

HIGH	Enabled (DEFAULT)
LOW	Disabled

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (PM)

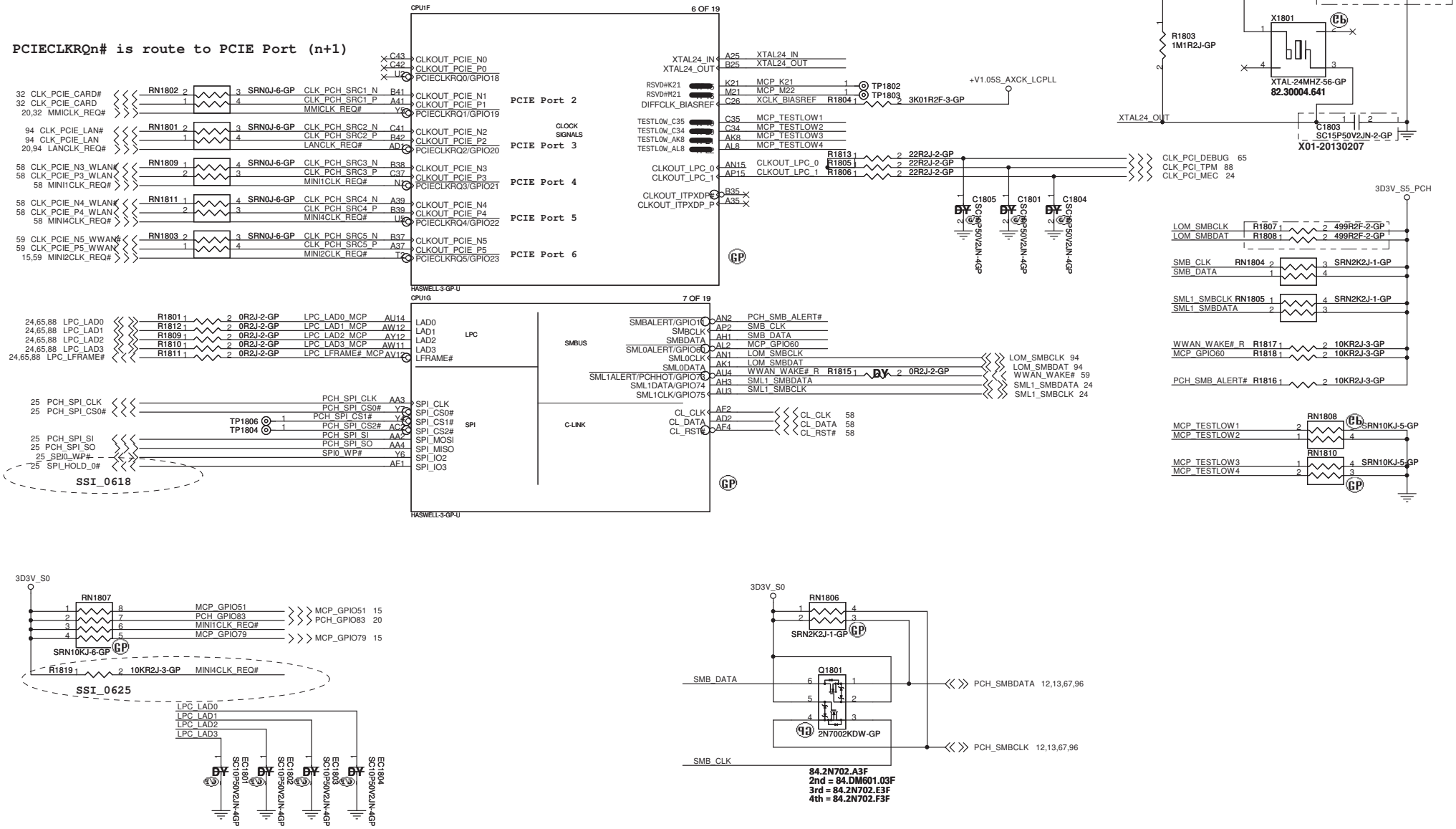
Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 17 of 107

SSID = PCH

PCIECLKRQ1# and PCIECLKRQ2#
Support S0 power only

PCIECLKRQn# is route to PCIE Port (n+1)



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **CPU (CLOCK/SMBUS/CL/LPC/SPI)**

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 18 of 107

SSID = PCH

RTC_AUX_S5

RN1901 SRN20KJ-GP-U

G1902 GAP-OPEN

C1902 SC1U6D3V3KX-2GP

G1901 GAP-OPEN

C1903 SC1U6D3V3KX-2GP

INTVRMEN- Integrated SUS 1.05V VRM Enable
High - Enable internal VRs
Low - Enable external VRs

CPU1E — 5 OF 19 — HASWELL-3-GP-U

RTC_AUX_S5

R1901 1M1R2J-GP
R1903 330KR2F-L-GP

RTC_X1 AW5 — RTCX1
RTC_X2 AY5 — RTCX2
SM_INTRUDER# AU8 — INTRUDER#
PCH_INTVRMEN AV7 — INTVRMEN
SRTC_RST# AV8 — SRTCRST#
RTC_RST# AU7 — RTCRST#

17 RTC_RST# <<<

RTC

HDA_BITCLK AW8 — HDA_BCLK/I2S0_SCLK
HDA_SYNC AV11 — HDA_SYNC/I2S0_SFRM
HDA_RST# AU9 — HDA_RST/I2S_MCLK
AY10 — HDA_SDI0/I2S0_RXD
AU12 — HDA_SDI1/I2S1_RXD
AU11 — HDA_SDO/I2S0_TXD
AW10 — [redacted] — HAD_DOCK_EN/I2S1_TXD#
AV10 — HDA_DOCK_RST/I2S1_SFRM
AY8 — I2S1_SCLK

27 HDA_SDIN0 >>>
99 ME_FWP >>>
R1904 1KR2J-1-GP HDA_SDOUT

AUDIO

RTC_X1
R1905 10MR2J-L-GP RTC_X2
R1906 0R2J-2-GP
X1901 XTAL-32D768KHZ-65-GP 82.30001.841
C1901 SC12P50V2JN-3GP
C1904 SC12P50V2JN-3GP

4,96 XDP_TRST# >>>
96 PCH_JTAG_TCK >>>
R1907 0R2J-2-GP DY
R1908 0R2J-2-GP DY

XDP_TRST#_R AU62 — PCH_TRST#
PCH_JTAG_TCK_BUF AE62 — PCH_TCK
PCH_JTAG_TDI AD61 — PCH_TDI
PCH_JTAG_TDO AE61 — PCH_TDO
PCH_JTAG_TMS AD62 — PCH_TMS
AL11 — RSVD#AL11
AC4 — RSVD#AC4
PCH_JTAGX AE63 — JTAGX
AV2 — RSVD#AV2

JTAG

96 PCH_JTAGX >>>

SATA

SATA_RN0/PERN6_L3 J5 — SATA_RXN0 56
SATA_RP0/PERP6_L3 H5 — SATA_RXP0 56
SATA_TN0/PETN6_L3 B15 — SATA_TXN0 56
SATA_TP0/PETP6_L3 A15 — SATA_TXP0 56

HDD

SATA_RN1/PERN6_L2 J8
SATA_RP1/PERP6_L2 H8
SATA_TN1/PETN6_L2 A17
SATA_TP1/PETP6_L2 B17

SATA_RN2/PERN6_L1 J6
SATA_RP2/PERP6_L1 H6
SATA_TN2/PETN6_L1 B14
SATA_TP2/PETP6_L1 C15

SATA_RN3/PERN6_L0 F5 — SATA_RN3/PERN6_L0 59
SATA_RP3/PERP6_L0 E5 — SATA_RP3/PERP6_L0 59
SATA_TN3/PETN6_L0 C17 — SATA_TN3/PETN6_L0 59
SATA_TP3/PETP6_L0 D17 — SATA_TP3/PETP6_L0 59

WWAN

SATA0GP/GPIO34 V1 — MPCIE_RST# 58
SATA1GP/GPIO35 U1 — HDD_DET# — HDD_DET# 56
SATA2GP/GPIO36 V6 — MCP_GPIO36
SATA3GP/GPIO37 AC1 — NGFF_PCIE_SATA# 99

SATA_IREF A12 — SATA_IREF R1909 0R2J-2-GP
RSVD#L11 L11 — MCP_L11 — TP1901
RSVD#K10 K10 — MCP_K10 — TP1902
SATA_RCOMP C12 — SATA_RCOMP R1910 3K01R2F-3-GP
SATALED# U3 — SATA_LED# 61

+V1.05S_ASATA3PLL

27 HDA_CODEC_SYNC — R1911 33R2J-2-GP — HDA_SYNC
27 HDA_CODEC_SDOUT — R1912 33R2J-2-GP — HDA_SDOUT
27 HDA_CODEC_RST# — R1913 33R2J-2-GP — HDA_RST#
27 HDA_CODEC_BITCLK — R1914 33R2J-2-GP — HDA_BITCLK

C1905 SC27P50V2JN-2-GP DY

Flash Descriptor Security Overide	
HDA_SDOUT	Low = Default High = Enable

+V3.3A_1.5A_HDA
R1917 1KR2J-1-GP DY HDA_SDOUT

3D3V_S0

SATA_LED# — R1915 10KR2J-3-GP DY
HDD_DET# — R1931 10KR2J-3-GP
MCP_GPIO36 — R1920 10KR2J-3-GP

1D05V_M

PCH_JTAGX — R1919 PCH XDP 51R2J-2-GP
PCH_JTAG_TMS — R1921 PCH XDP 51R2J-2-GP
PCH_JTAG_TDI — R1922 PCH XDP 51R2J-2-GP
PCH_JTAG_TDO — R1923 PCH XDP 51R2J-2-GP
PCH_JTAG_TCK_BUF — R1924 PCH XDP 51R2J-2-GP

PCH_JTAG_TDO — R1928 PCH XDP 0R2J-2-GP >>> CPU_XDP_TDO_PCH 96
PCH_JTAG_TDI — R1929 PCH XDP 0R2J-2-GP <<< CPU_XDP_TDI_PCH 96
PCH_JTAG_TMS — R1930 PCH XDP 0R2J-2-GP <<< CPU_XDP_TMS_PCH 96

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (RTC/SATA/HDA/JTAG)

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 19 of 107

SSID = PCH

+V3.3A_DSW_P

RN2001 (CB) SRN10KJ-5-GP
- PM_LANPHY_ENABLE
- EC_WAKE#

3D3V_S5_PCH

- R2005 10KR2J-3-GP SIO_EXT_WAKE#
- R2006 10KR2J-3-GP PCH_NFC_RST
- R2008 10KR2J-3-GP NFC_IRQ
- R2004 10KR2J-3-GP MCP_GPIO15
- R2015 10KR2J-3-GP MEDIACARD_PWREN

Vendor ask just pull up to 3D3V_S0

RN1601 (GP) SRN10KJ-6-GP
- SNSR_HUB_PWREN
- MCP_GPIO9
- SLATE_MODE
- SNSR_HUB_RST#

EDS no ask GPIO9 required external PH

3D3V_S0

- R2009 10KR2J-3-GP MEDIACARD_IRQ#
- R2019 100KR2J-1-GP SIO_EXT_SCI#
- R2020 DY 1KR2F-3-GP HDA_SPKR
- R2024 2K2R2J-2-GP I2C0_SDA
- R2025 2K2R2J-2-GP I2C0_SCL
- R2026 2K2R2J-2-GP DAT_I2C_TP_SIO
- R2027 2K2R2J-2-GP CLK_I2C_TP_SIO
- R2028 100KR2J-1-GP MCP_GPIO91
- R2029 100KR2J-1-GP MCP_GPIO92
- R2041 20KR2J-L2-GP TPM_ID1
- R2007 10KR2J-3-GP MCP_GPIO3
- R2043 100KR2J-1-GP MCP_GPIO48

EDS no ask GPIO48 required external PH

RN2009 (GP) SRN10KJ-6-GP
- DBC_PANEL_EN
- LANCLK_REQ#
- MPHYP_PWR_EN

LANCLK_REQ# 18,94

RN2008 (GP) SRN10KJ-6-GP
- CAM_MIC_CBL_DET#
- TPM_ID0
- USH_DET#
- SLP_ME_CSW_DEV#

RN2007 (GP) SRN10KJ-6-GP
- FFS_INT2
- MCP_GPIO94
- LCD_CBL_DET#
- MCP_GPIO93

EDS no ask GPIO94 required external PH

RN2006 (GP) SRN10KJ-6-GP
- MCP_GPIO54
- MCP_GPIO0
- 3.3V_mSATA_EN

MCP_GPIO54 15

RN2003 (GP) SRN10KJ-6-GP
- SIO_RCIN#
- MMICLK_REQ#
- IRQ_SERIRQ
- CONTACTLESS_DET#

MMICLK_REQ# 18,32

CONTACTLESS_DET# 15

- R2054 DY 10KR2J-3-GP NFC_IRQ
- R2055 100KR2J-1-GP 3.3V_CAM_EN#
- R2057 10KR2J-3-GP PCH_AUDIO_PWR

24 SIO_EXT_WAKE#
94 PM_LANPHY_ENABLE
94 LAN_RST#
24,94 LAN_WAKE#
R2011 0R2J-2-GP
24 EC_WAKE#
TP2001 MCP_GPIO17
TP2002 MCP_GPIO24
NFC_IRQ
EC_WAKE#
PCH_NFC_RST
16,62 KB_DET#
TP2008 MCP_GPIO14
52 3.3V_CAM_EN#
3.3V_CAM_EN#
SNSR_HUB_RST#
16,24 SIO_EXT_SMI#
R2013 0R2J-2-GP
SIO_EXT_SMI#_R
SNSR_HUB_PWREN
32 MEDIACARD_IRQ#
MEDIACARD_IRQ#
MCP_GPIO48
TP2003 MCP_GPIO49
98 TOUCH_PANEL_INTR#
32 MEDIACARD_RST#
32 MEDIACARD_PWREN
MEDIACARD_PWREN
SLATE_MODE
TP2004 MCP_GPIO59
36 MPHYP_PWR_EN
MPHYP_PWR_EN
MCP_GPIO9
TP2006 MCP_GPIO10
56 mSATA_DEVSLP
59 NGFF_DEVSLP1
R2017 DY 0R2J-2-GP MCP_GPIO38
24 SIO_EXT_SCI#
SIO_EXT_SCI#
TP2007 MCP_GPIO70
27 HDA_SPKR
HDA_SPKR

No Reboot Strap	
HDA_SPKR	Low = Default High = No Reboot

CPU1J — 10 OF 19 — HASWELL-3-GP-U http://adf.ly/3o8pJ

GPIO
- P1 PCH_AUDIO_PWR
- AU2 SIO_EXT_WAKE#
- AM1 PM_LANPHY_ENABLE
- AD6 MCP_GPIO15
- Y1 BMBUSY/GPIO76
- T3 GPIO8
- AD5 LAN_PHY_PWR_CTRL/GPIO12
- AN3 GPIO15
- AN5 GPIO16
- AD7 GPIO17
- GPIO24
- GPIO26
- GPIO27
- GPIO28
- AT3 KB_DET#
- AH4 GPIO13
- AM4 GPIO14
- AK4 GPIO25
- AG5 GPIO44
- AG3 GPIO45
- AB6 GPIO46
- U4 GPIO47
- Y3 GPIO48
- P3 GPIO49
- AG6 GPIO50
- AP1 GPIO56
- AL4 GPIO57
- AT5 GPIO58
- Y2 GPIO59
- AM3 HSIOPC/GPIO71
- AM2 GPIO9
- P2 GPIO10
- L2 DEVSLP0/GPIO33
- N5 DEVSLP1/GPIO38
- C4 DEVSLP2/GPIO39
- V2 SDIO_POWER_EN/GPIO70
- SPKR/GPIO81

CPU/MISC
- AW15 PCH_OPIRCOMP
- AE20 RSVD#AF20
- AB21 RSVD#AB21

LPIO
- R6 GSPI0_CS/GPIO83
- L6 GSPI0_CLK/GPIO84
- N6 GSPI0_MISO/GPIO85
- L8 GSPI0_MOSI/GPIO86
- R7 GSPI1_CS/GPIO87
- L5 GSPI1_CLK/GPIO88
- N7 GSPI1_MISO/GPIO89
- K2 GSPI1_MOSI/GPIO90
- J1 UART0_RXD/GPIO91
- K3 UART0_TXD/GPIO92
- J2 UART0_RTS/GPIO93
- G1 UART0_CTS/GPIO94
- K4 UART1_RXD/GPIO0
- G2 UART1_TXD/GPIO1
- J3 UART1_RST/GPIO2
- J4 UART1_CTS/GPIO3
- F2 I2C0_SDA/GPIO4
- F3 I2C0_SCL/GPIO5
- G4 I2C1_SDA/GPIO6
- F1 I2C1_SCL/GPIO7
- E3 SDIO_CLK/GPIO64
- F4 SDIO_CMD/GPIO65
- D3 SDIO_D0/GPIO66
- E4 SDIO_D1/GPIO67
- C3 SDIO_D2/GPIO68
- E2 SDIO_D3/GPIO69

THRMTRIP
- D60 H_THERMTRIP# R
- V4 RCIN/GPIO8
- T4 SERIRQ

R2014 0R2J-2-GP
- H_THERMTRIP# 24
- SIO_RCIN# 24
- IRQ_SERIRQ 24,88

R2016 49D9R2F-GP

+V1.05S_VCCST

R2012 1KR2J-1-GP CRB: ULTWTM1 1K Goliad is DY.

- PCH_GPIO83 18
- MCP_GPIO84 15
- 3.3V_mSATA_EN 59
- BBS_BIT
- DBC_PANEL_EN 52
- 3.3V_TP_EN 15,62
- 3.3V_TS_EN 15,98
- 3.3V_HDD_EN 15,56
- MCP_GPIO91
- MCP_GPIO92
- MCP_GPIO93
- MCP_GPIO94
- MCP_GPIO0
- FFS_INT2 67
- LCD_CBL_DET# 52
- MCP_GPIO3
- I2C0_SDA
- I2C0_SCL
- DAT_I2C_TP_SIO
- CLK_I2C_TP_SIO
- USH_DET#
- CAM_MIC_CBL_DET# 52
- MCP_GPIO66
- TPM_ID0
- TPM_ID1
- SLP_ME_CSW_DEV# 99

EDS ask GPIO3 need external PH onpage94

3D3V_S0

R2044 DY 10KR2J-3-GP

BBS_BIT

R2049 DY 1KR2J-1-GP

3D3V_S0

R2045 DY 10KR2J-3-GP

MCP_GPIO66

R2051 DY 1KR2F-3-GP

BOOT BIOS Strap	
GPIO86	BOOT BIOS Location
0	SPI(Default)
1	LPC

TOP-BLOCK SWAP OVERRIDE
GPIO66
HIGH pop R20545
LOW pop R2051(DEFAULT)

<Core Design>

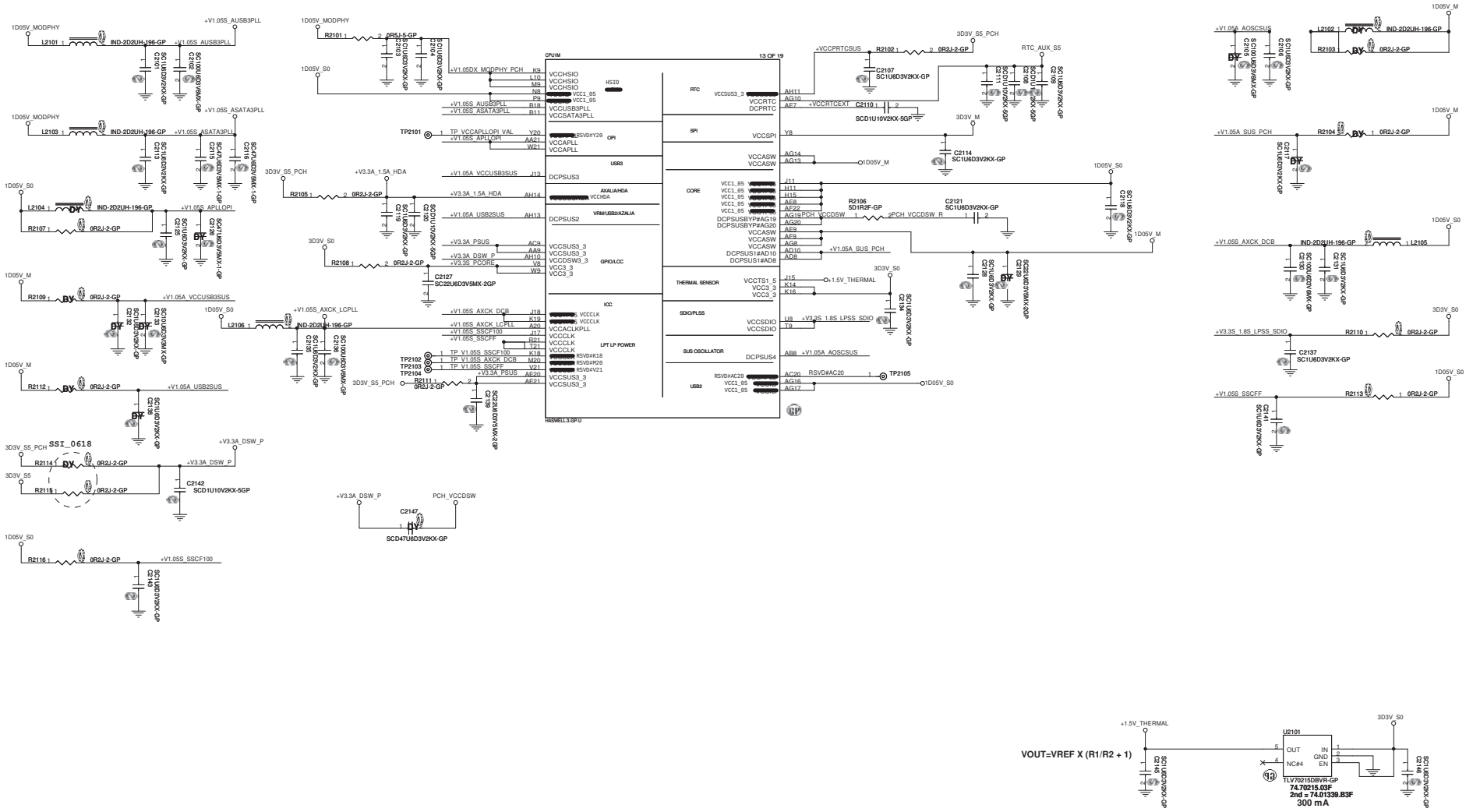
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (GPIO/CPU)

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 20 of 107

SSID = PCH



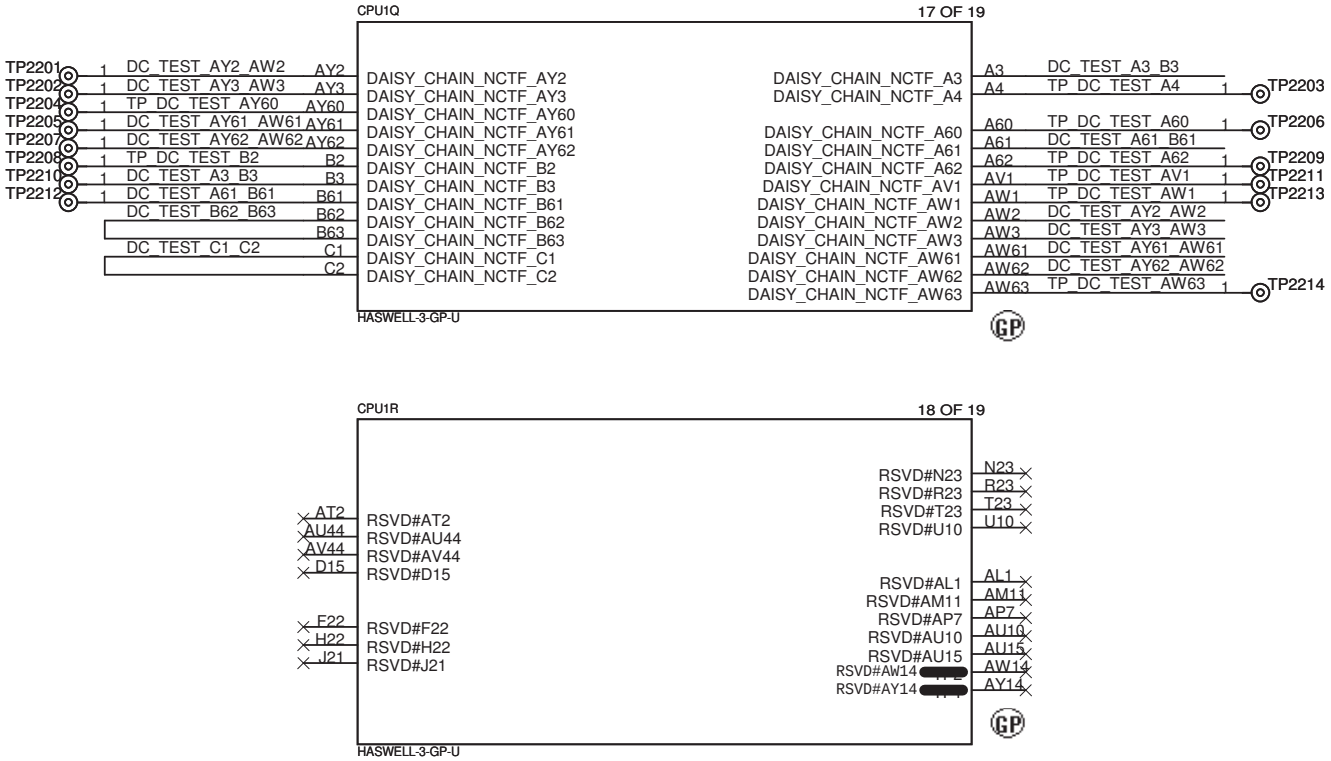
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: CPU (POWER1)

Size: A2 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 21 of 107



<Core Design>

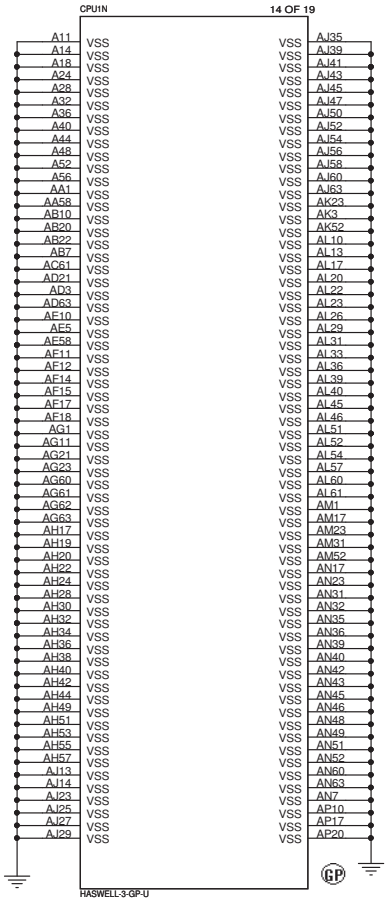
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

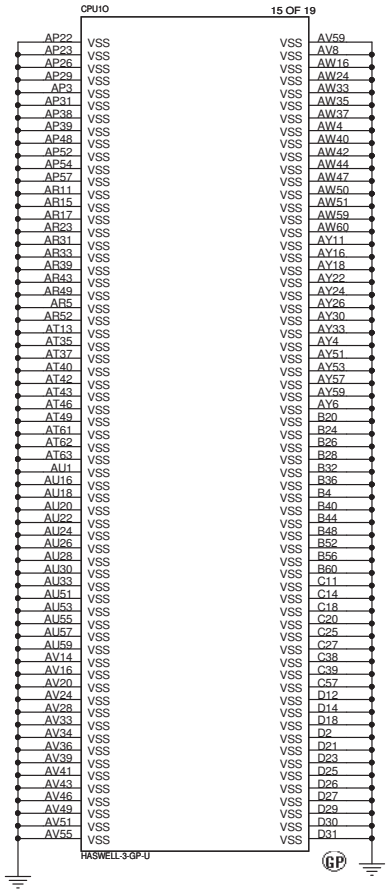
Title: ***CPU (RSVD)***

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

Date: Friday, June 28, 2013 Sheet 22 of 107

SSID = PCH





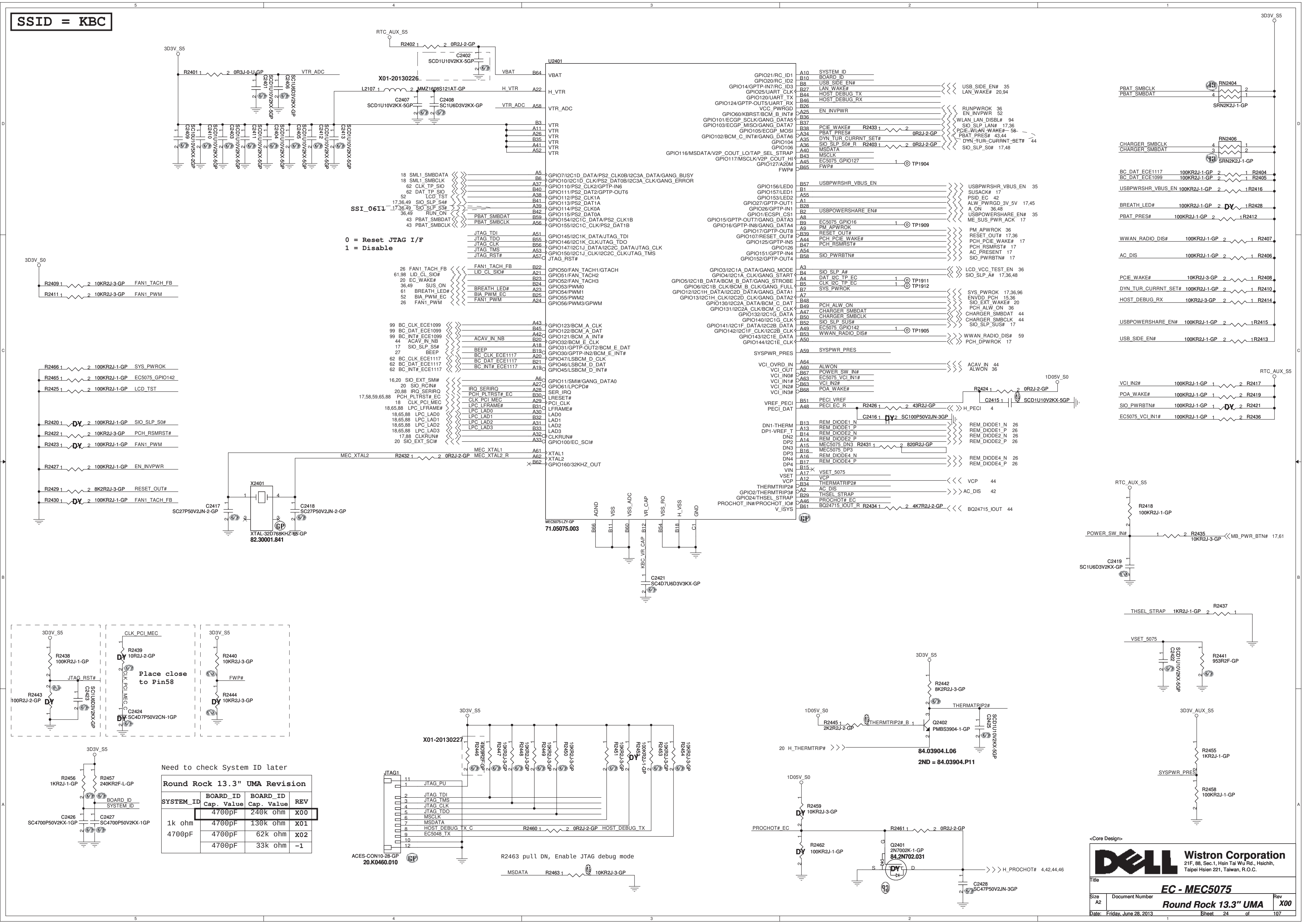
<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***CPU (VSS)***

Size: A3 | Document Number: ***Round Rock 13.3" UMA*** | Rev: ***X00***

Date: Friday, June 28, 2013 | Sheet 23 of 107



Round Rock 13.3" UMA Revision

SYSTEM_ID	BOARD_ID Cap. Value	BOARD_ID Cap. Value	REV
1k ohm 4700pF	4700pF	240k ohm	X00
	4700pF	130k ohm	X01
	4700pF	62k ohm	X02
	4700pF	33k ohm	-1

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

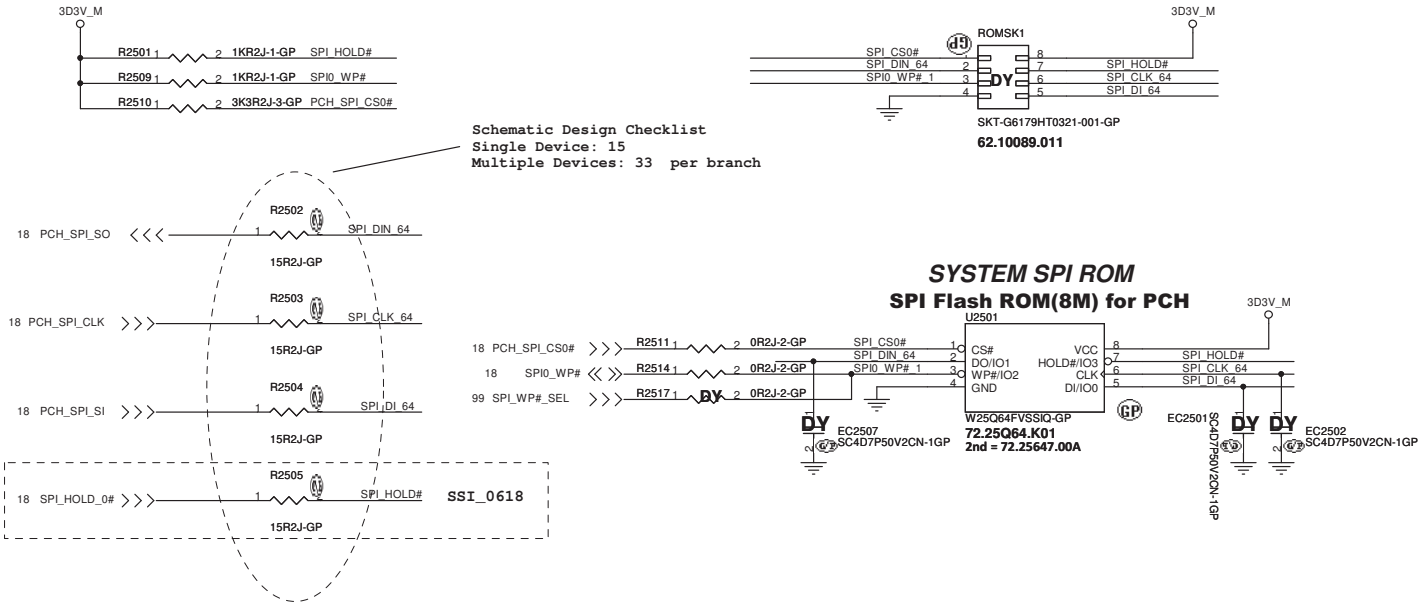
Title: EC - MEC5075

Size: A2 | Document Number: Round Rock 13.3" UMA | Rev: X00

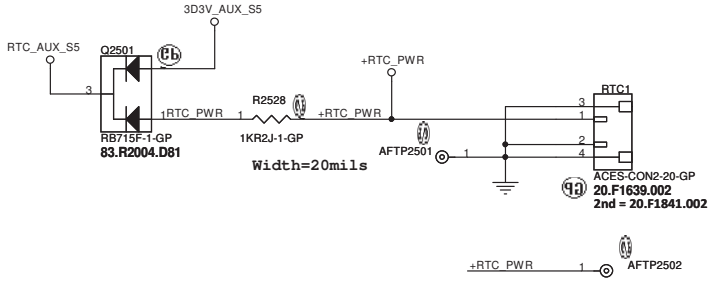
Date: Friday, June 28, 2013 | Sheet 24 of 107

SSID = Flash.ROM

SPI ROM Equal length need to less than 500mil



SSID = RTC



<Core Design>

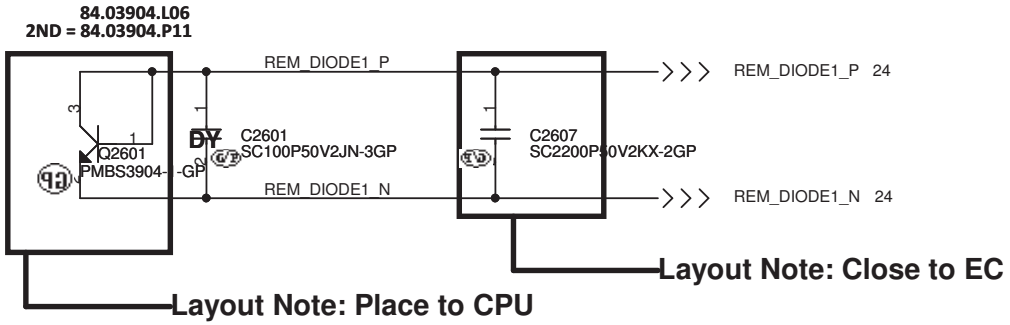
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

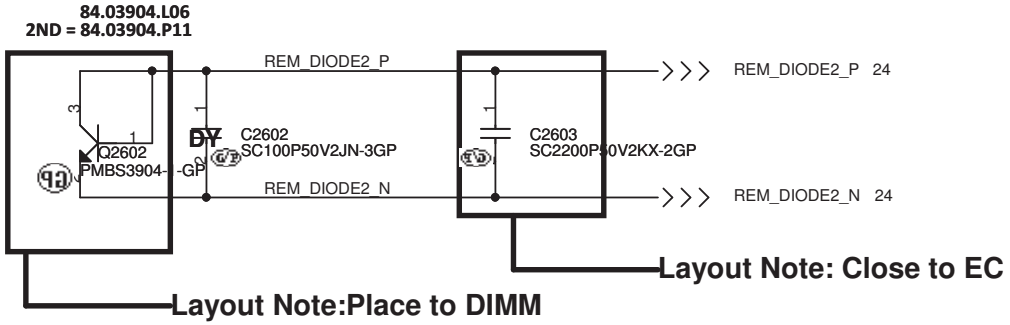
Title: Flash/RTC

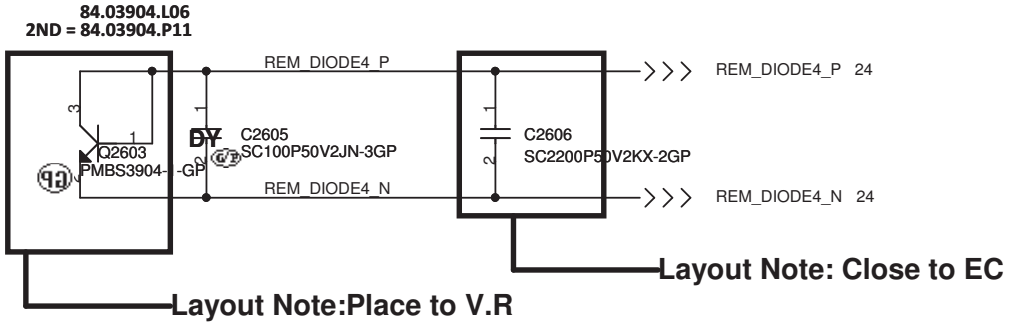
Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: AX00

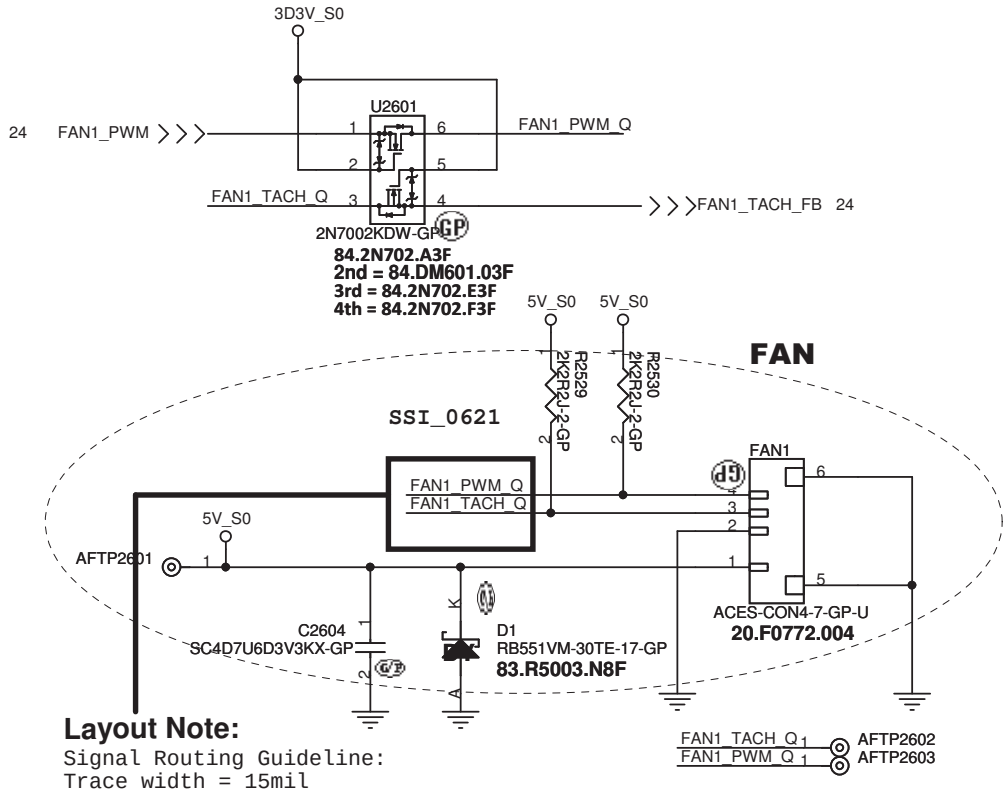
Date: Friday, June 28, 2013 | Sheet 25 of 107

SSID = Thermal







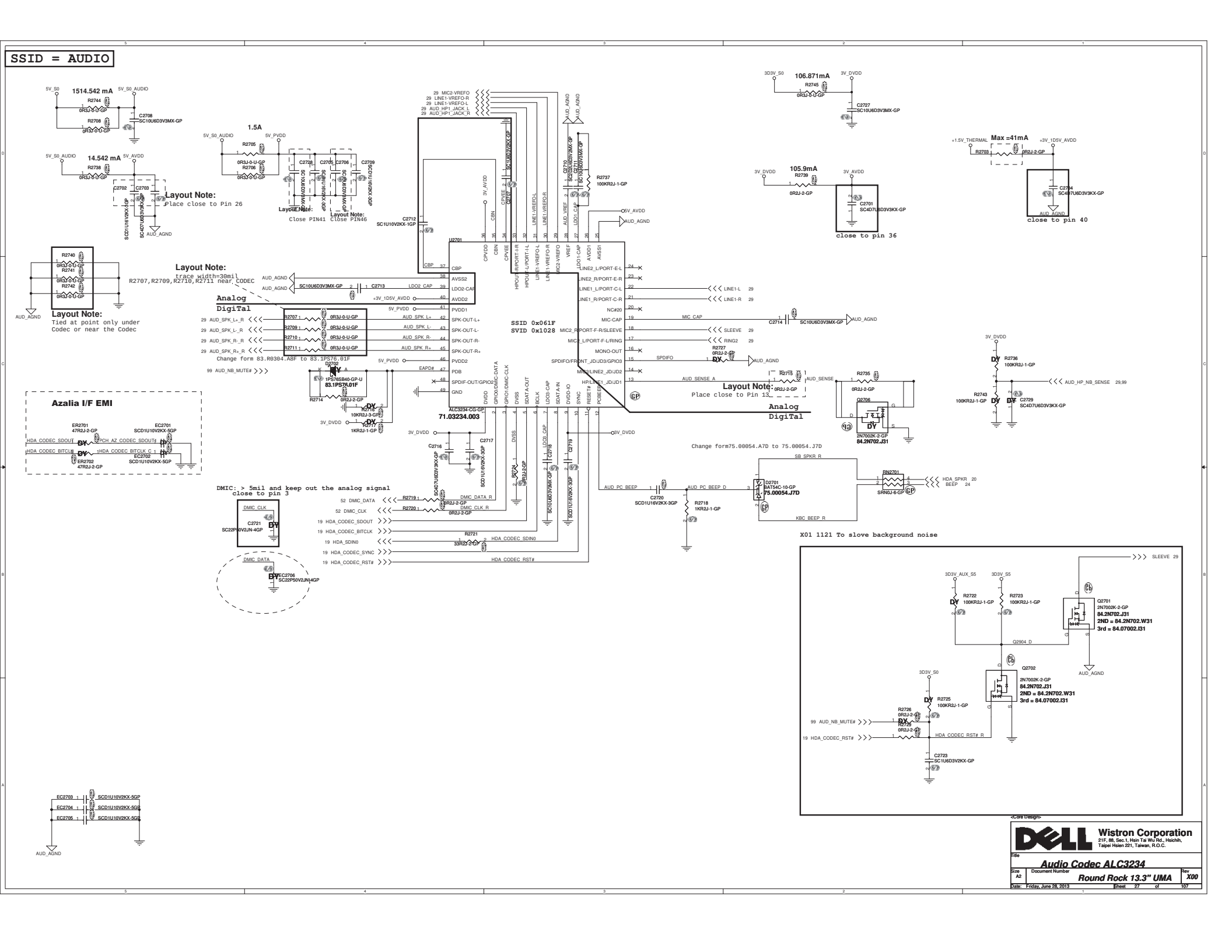


<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***Thermal/Fan***		
Size: A4	Document Number: ***Round Rock 13.3" UMA***	Rev: ***X00***
Date: Friday, June 28, 2013	Sheet 26 of 107	

SSID = AUDIO


1514.542 mA
14.542 mA
1.5A
106.871mA
105.9mA
Max =41mA
Layout Note:
Place close to Pin 26
Close PIN41 Close PIN46
close to pin 36
close to pin 40
Layout Note:
trace width=30mil
R2707,R2709,R2710,R2711 near CODEC
Layout Note:
Tied at point only under
Codec or near the Codec
Layout Note:
Place close to Pin 13
Analog
DigiTal
SSID 0x061F
SVID 0x1028
Change form 83.R0304.A8F to 83.1PS76.01F
Change form75.00054.A7D to 75.00054.J7D
71.03234.003
Azalia I/F EMI
DMIC: > 5mil and keep out the analog signal
close to pin 3
X01 1121 To slove background noise
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.
Audio Codec ALC3234
Round Rock 13.3" UMA
X00
Friday, June 28, 2013
27
107

(Blanking)

<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

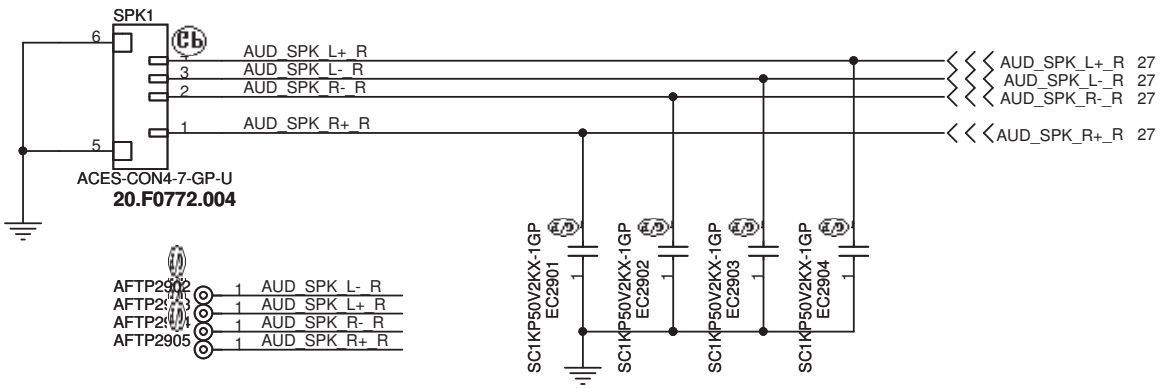
Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

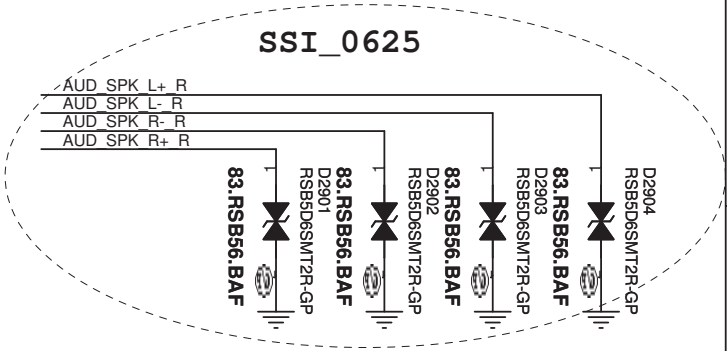
Date: Friday, June 28, 2013 Sheet 28 of 107

SSID = AUDIO

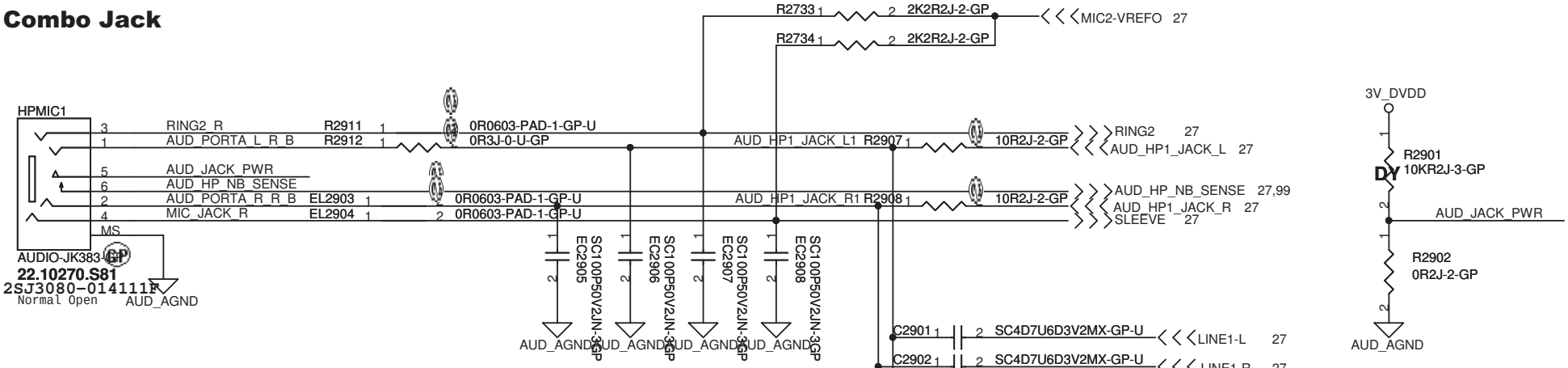
Speaker

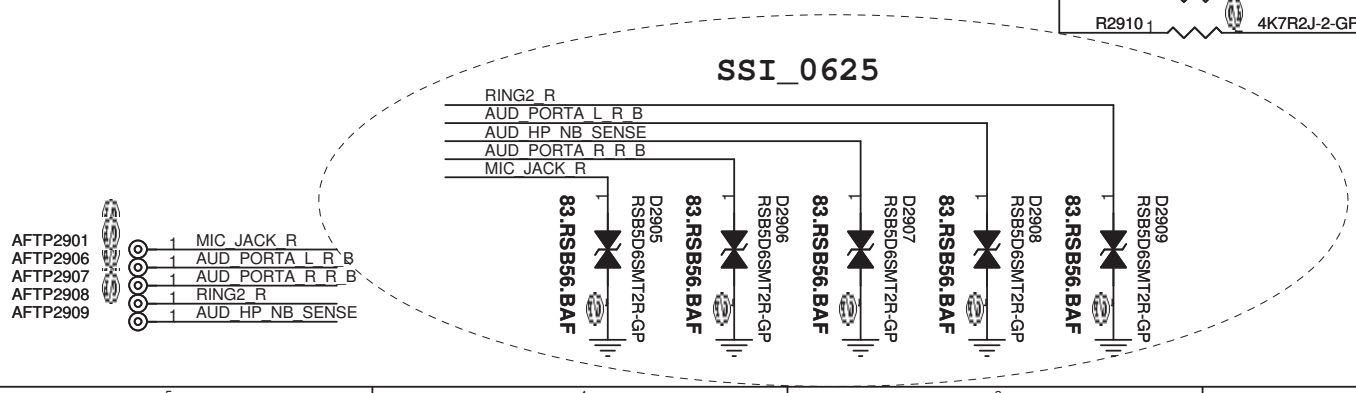
2W/ch





Combo Jack





<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: **Speaker/HPMIC CONN**

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 29 of 107

(Blanking)

<Core Design>

Wistron Corporation
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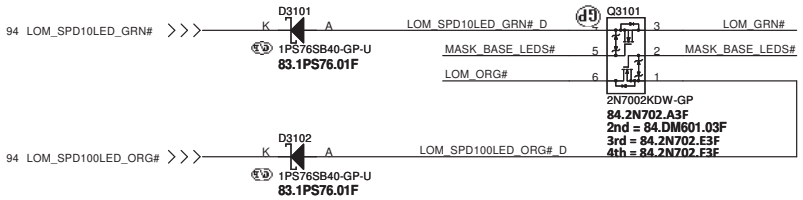
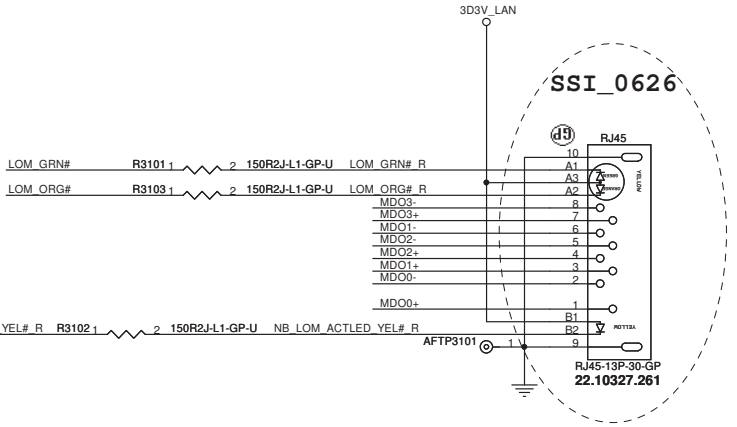
Title: ***Reserved***

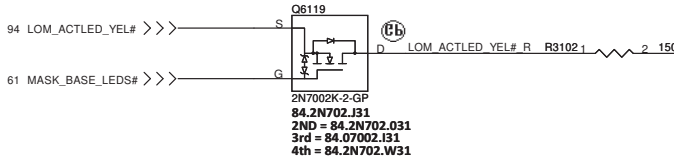
Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

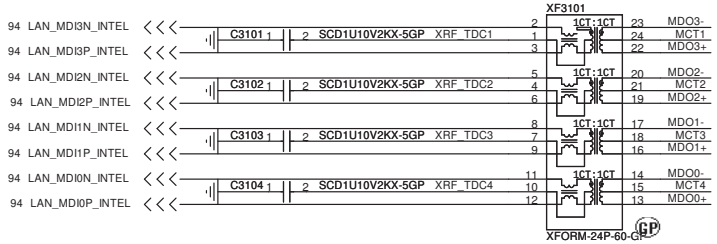
Date: Friday, June 28, 2013 Sheet 30 of 107

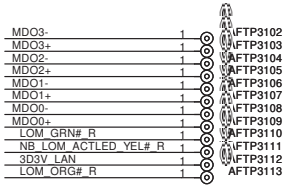
SSID = LOM

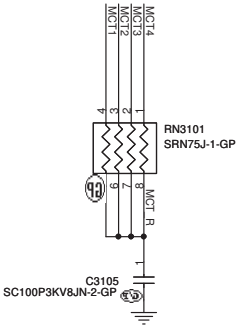












<Core Design>

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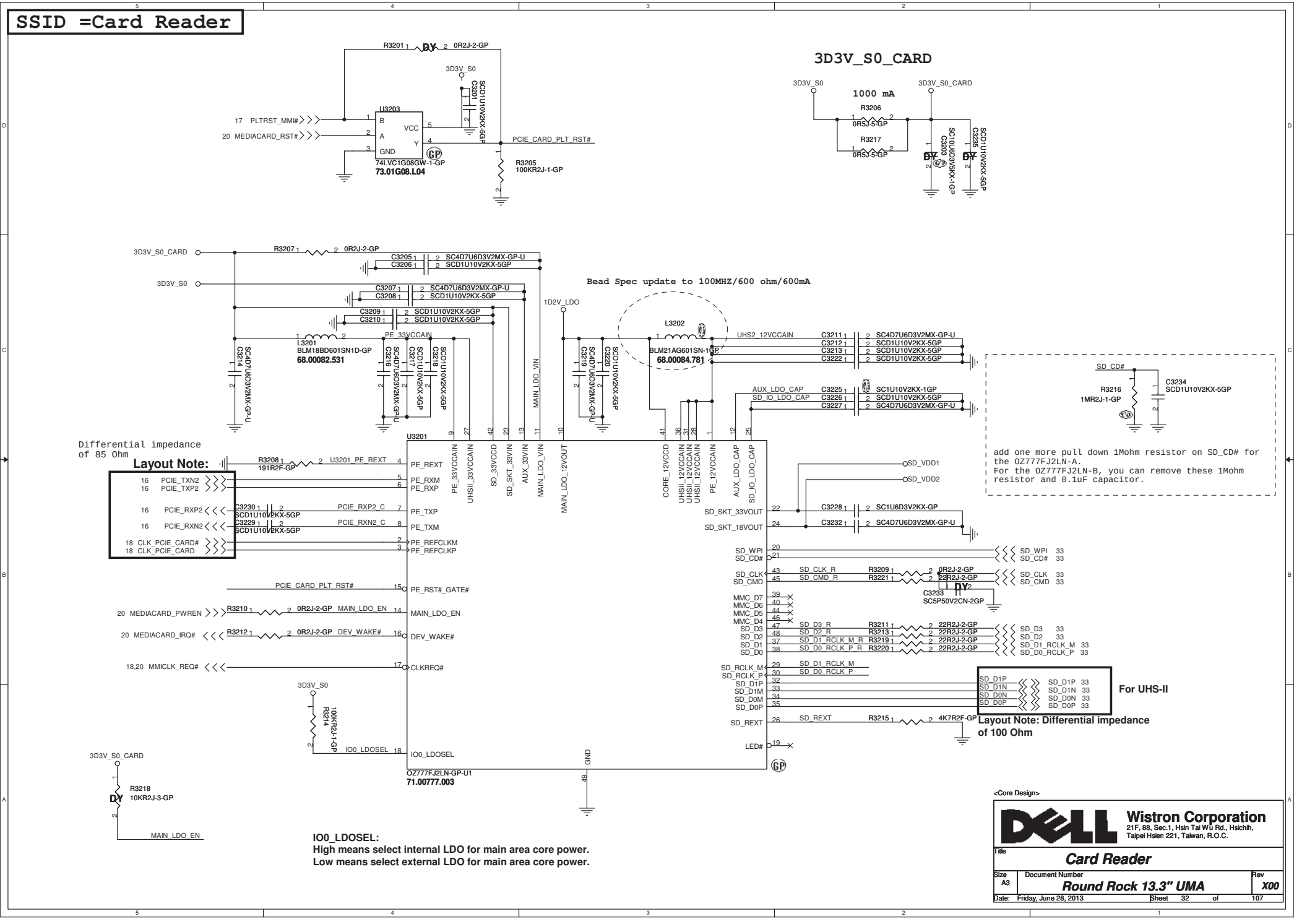
Taipei Hsien 221, Taiwan, R.O.C.

Title: *RJ45/Transformer*

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 31 of 107

SSID =Card Reader



<Core Design>

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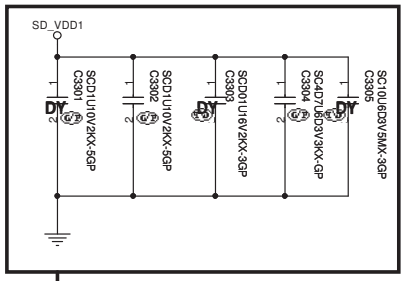
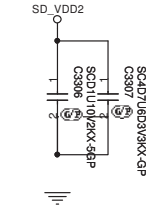
Taipei Hsien 221, Taiwan, R.O.C.

Title	Card Reader	
Size A3	Document Number: Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013	Sheet 32 of 107	

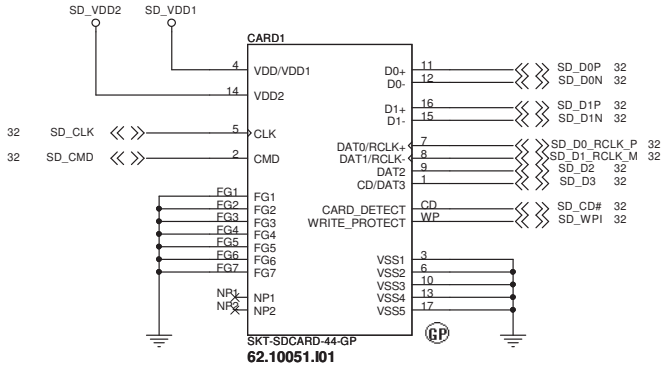
SSID =Card Reader

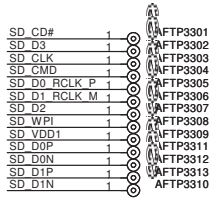


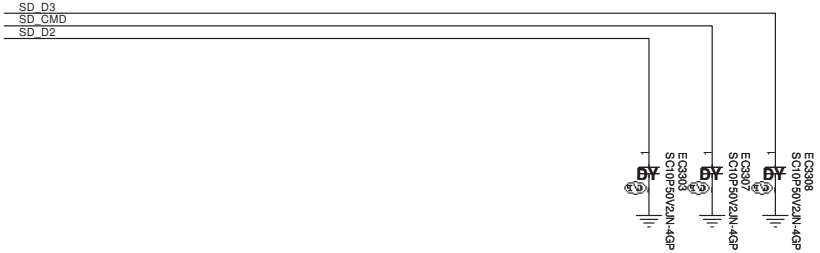
Layout Note:Close to Card Reader CONN

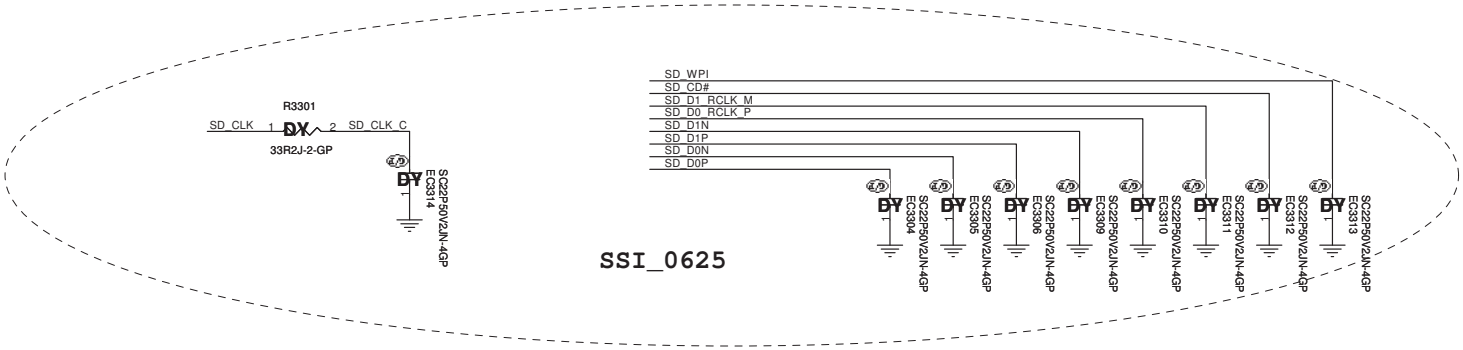


SD 4.0 Card Connector



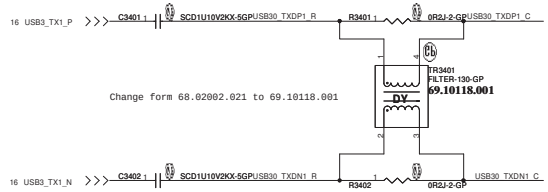




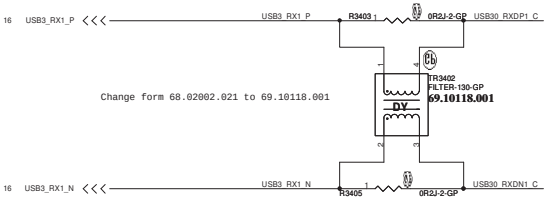


Title	Card Reader CONN	
Size A3	Document Number: Round Rock 13.3" UMA	Rev: X00
Date: Friday, June 28, 2013	Sheet 33 of 107	

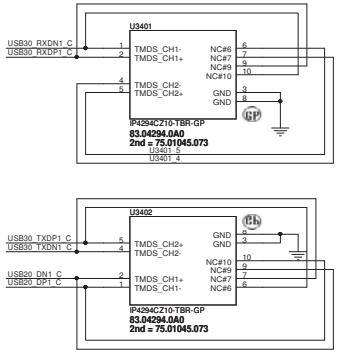
SSID = USB

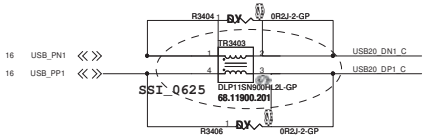


Change form 68.02002.021 to 69.10118.001

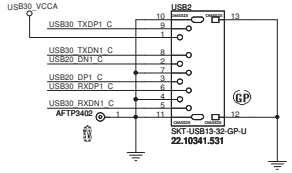


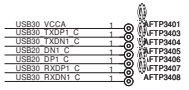
Change form 68.02002.021 to 69.10118.001

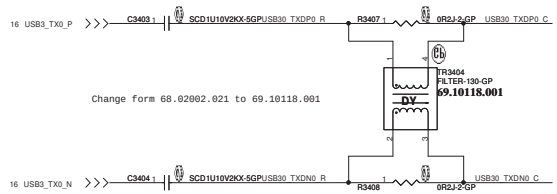




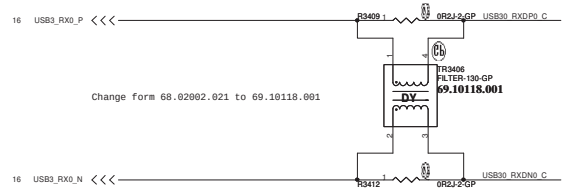
EXT Port2 Right Side



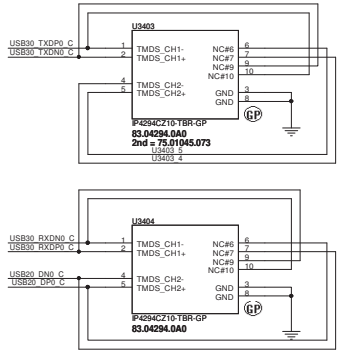


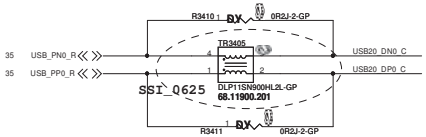


Change form 68.02002.021 to 69.10118.001

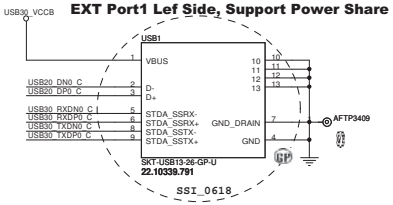


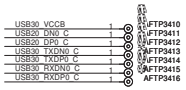
Change form 68.02002.021 to 69.10118.001





EXT Port1 Lef Side, Support Power Share





<Core Design>

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Title: **USB 3.0 Port**

Size	Document Number	Rev
A2	Round Rock 13.3" UMA	X00

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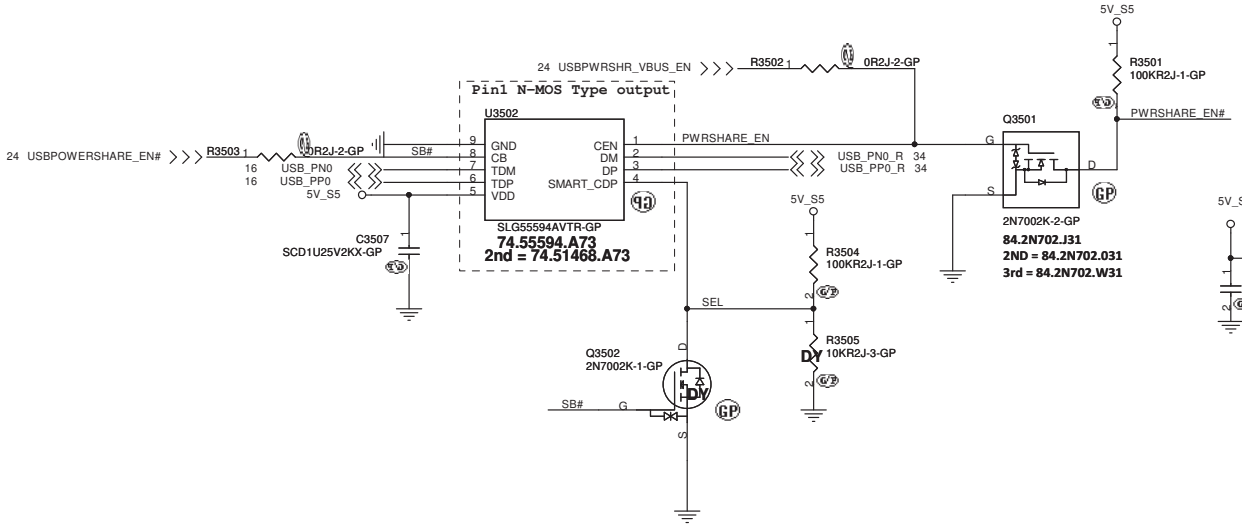
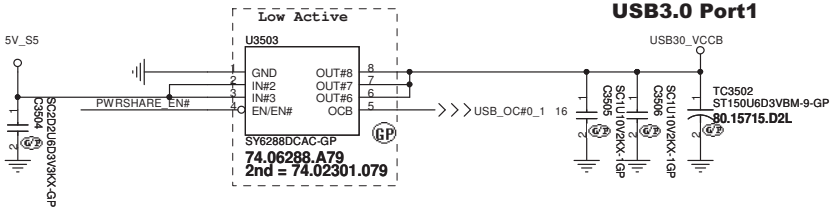
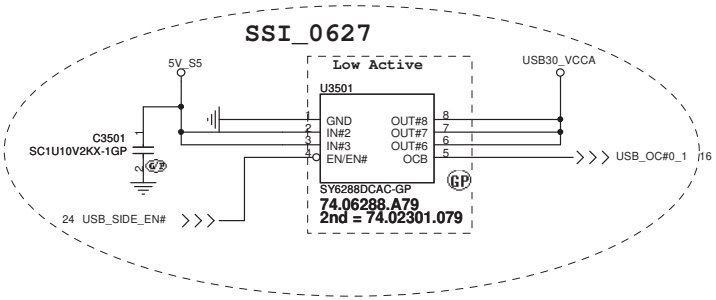
SSID = USB

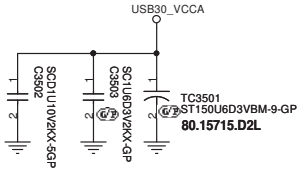




USB Power SW (U3501 & U3503)

Vendor	Vendor P/N	Wistron P/N	Priority
Silergy	SY6288DCAC	74.06288.A79	1ST
DII (Diodes)	AP2301MPG-13	74.02301.079	2ND
			3RD





<Core Design>

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Title: USB3.0 Power SW

Size | Document Number: Round Rock 13.3" UMA | Rev: X00

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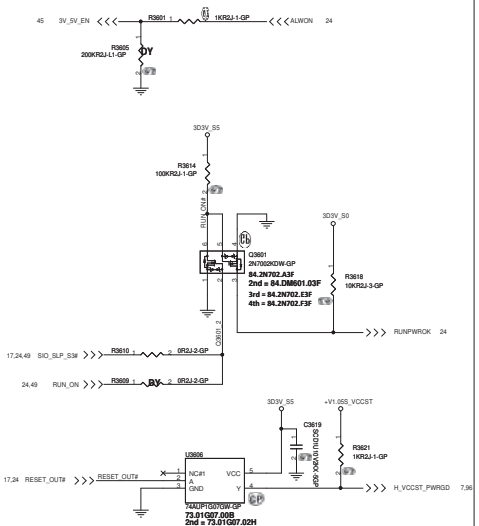
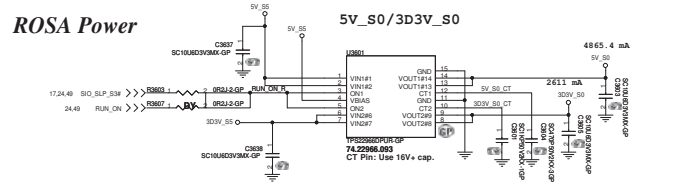
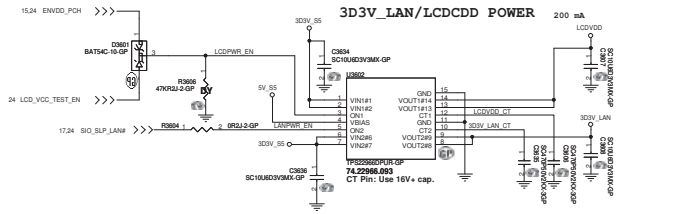
SSID = Reset.Suspend

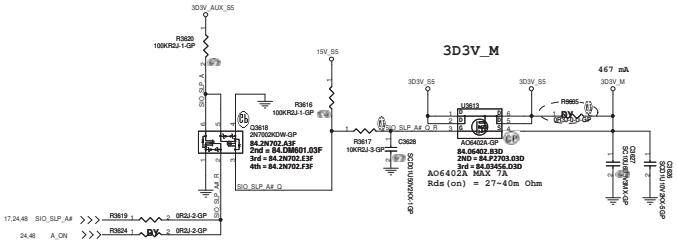
Power Sequence

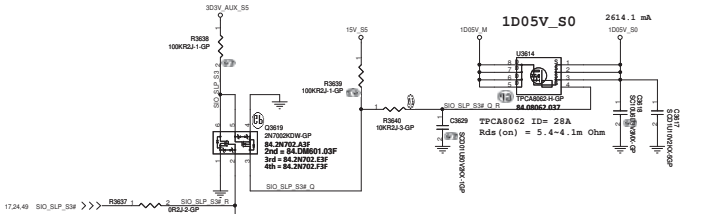


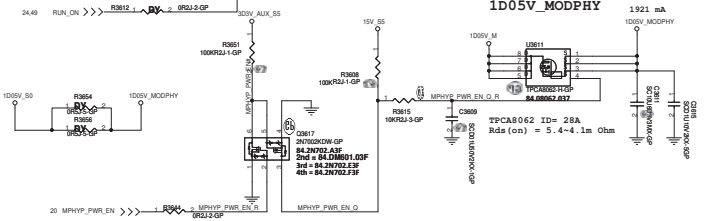
ROSA Power

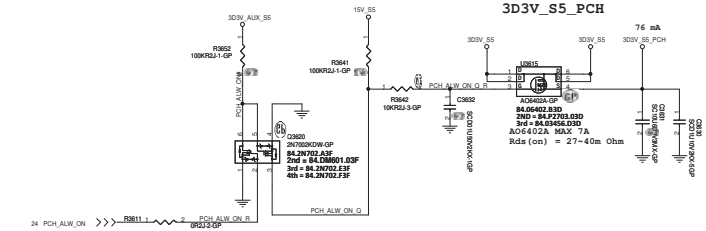


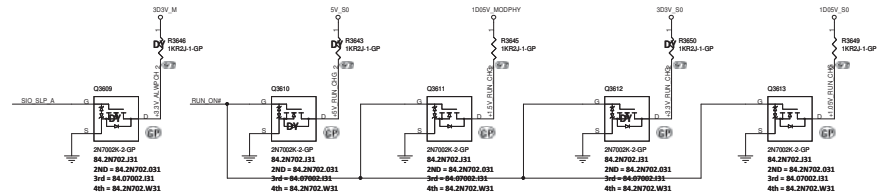


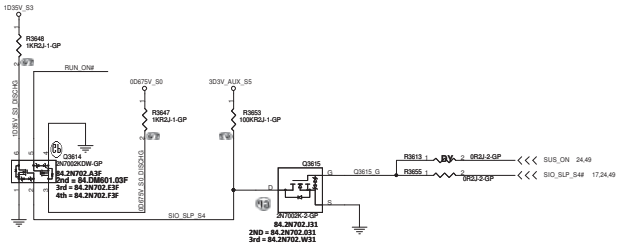




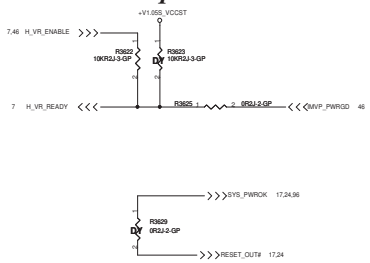


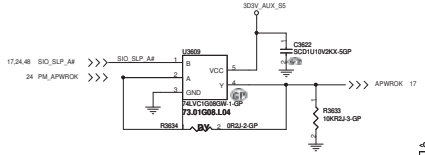






Intel Power Sequence





<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title: Power Plane Enable

Size	Document Number	Rev
Custom	Round Rock 13.3" UMA	X00
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SSID = Reset.Suspend

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<Core Design>

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Title
S3 Reduction

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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<Core Design>

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Title
Reserved

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

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SSID = OBFF

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<Core Design>

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Title
Reserved

Size	Document Number	Rev
A4	*Round Rock 13.3" UMA*	*X00*

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(Blanking)

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title
Reserved

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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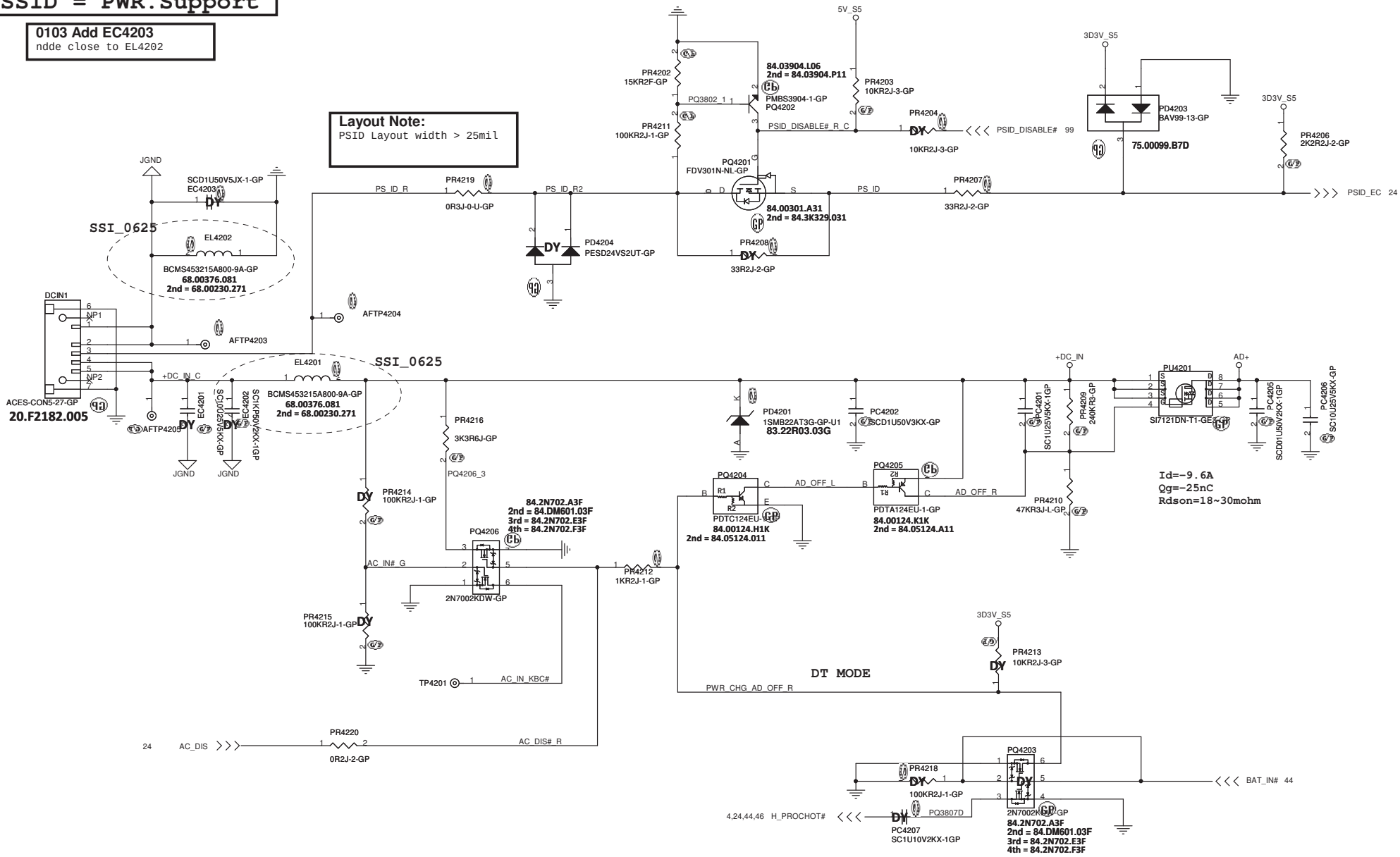
SSID = PWR.Support

0103 Add EC4203
ndde close to EL4202

Layout Note:
PSID Layout width > 25mil



<Core Design>

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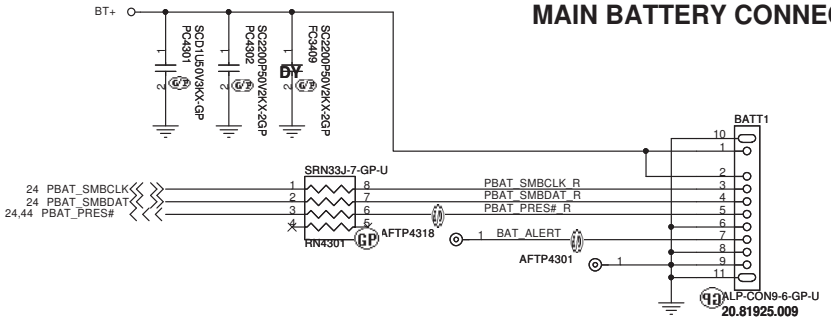
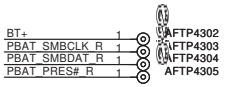
Taipei Hsien 221, Taiwan, R.O.C.

Title	*DCIN JACK*	
Size A3	Document Number *Round Rock 13.3" UMA*	Rev *X00*
Date: Friday, June 28, 2013	Sheet 42 of 107	

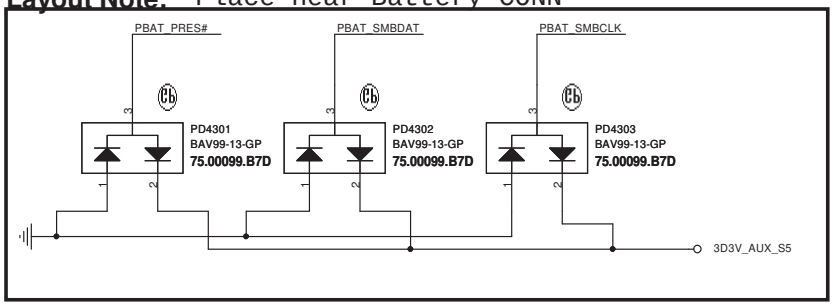
SSID = PWR.Support

MAIN BATTERY CONNECTOR





Layout Note: Place near Battery CONN



<Core Design>

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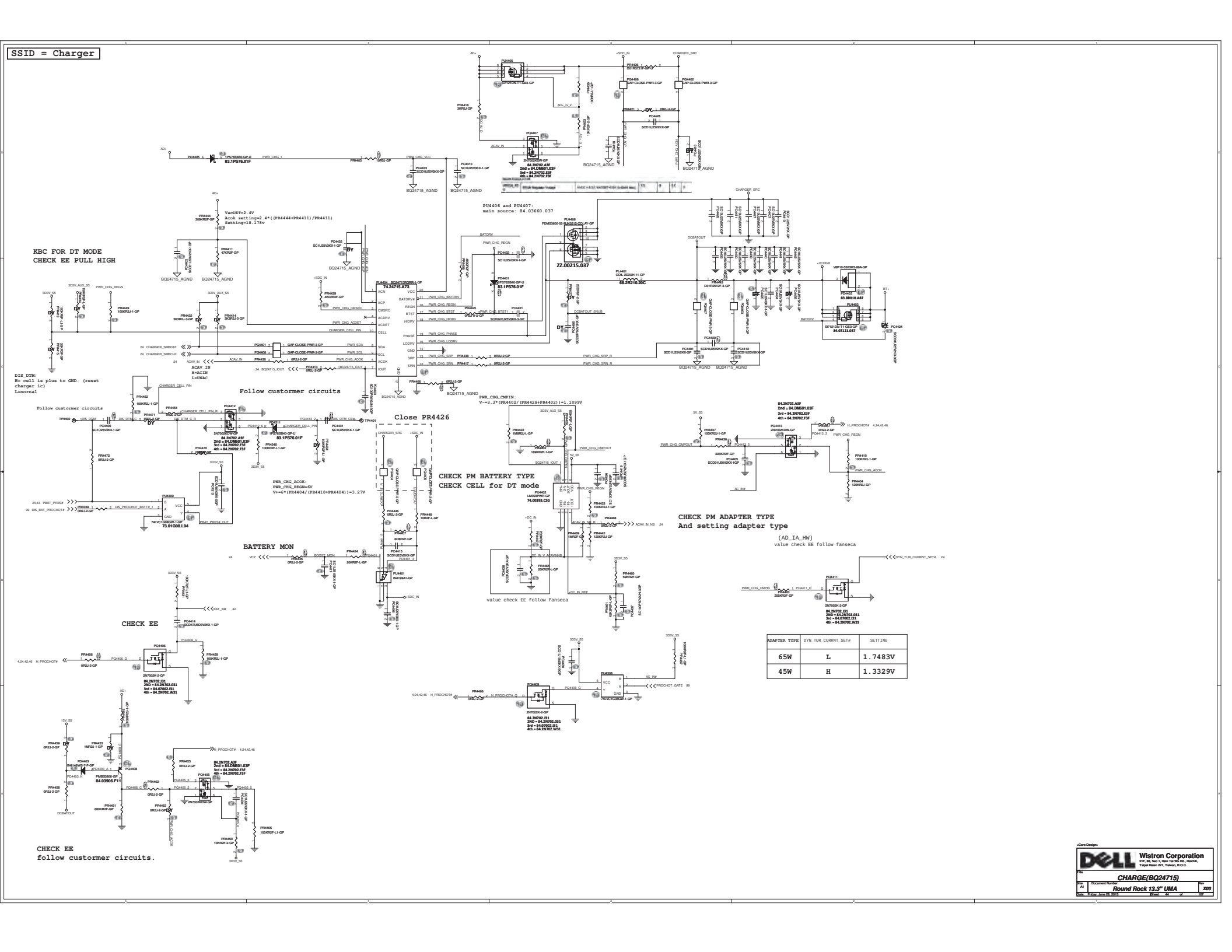
Taipei Hsien 221, Taiwan, R.O.C.

Title	BATTERY CONN	
Size: A3	Document Number: Round Rock 13.3" UMA	Rev: X00
Date: Friday, June 28, 2013	Sheet 43 of 107	

SSID = Charger



ADAPTER TYPE	DYN_TUR_CURRNT_SET#	SETTING
65W	L	1.7483V
45W	H	1.3329V

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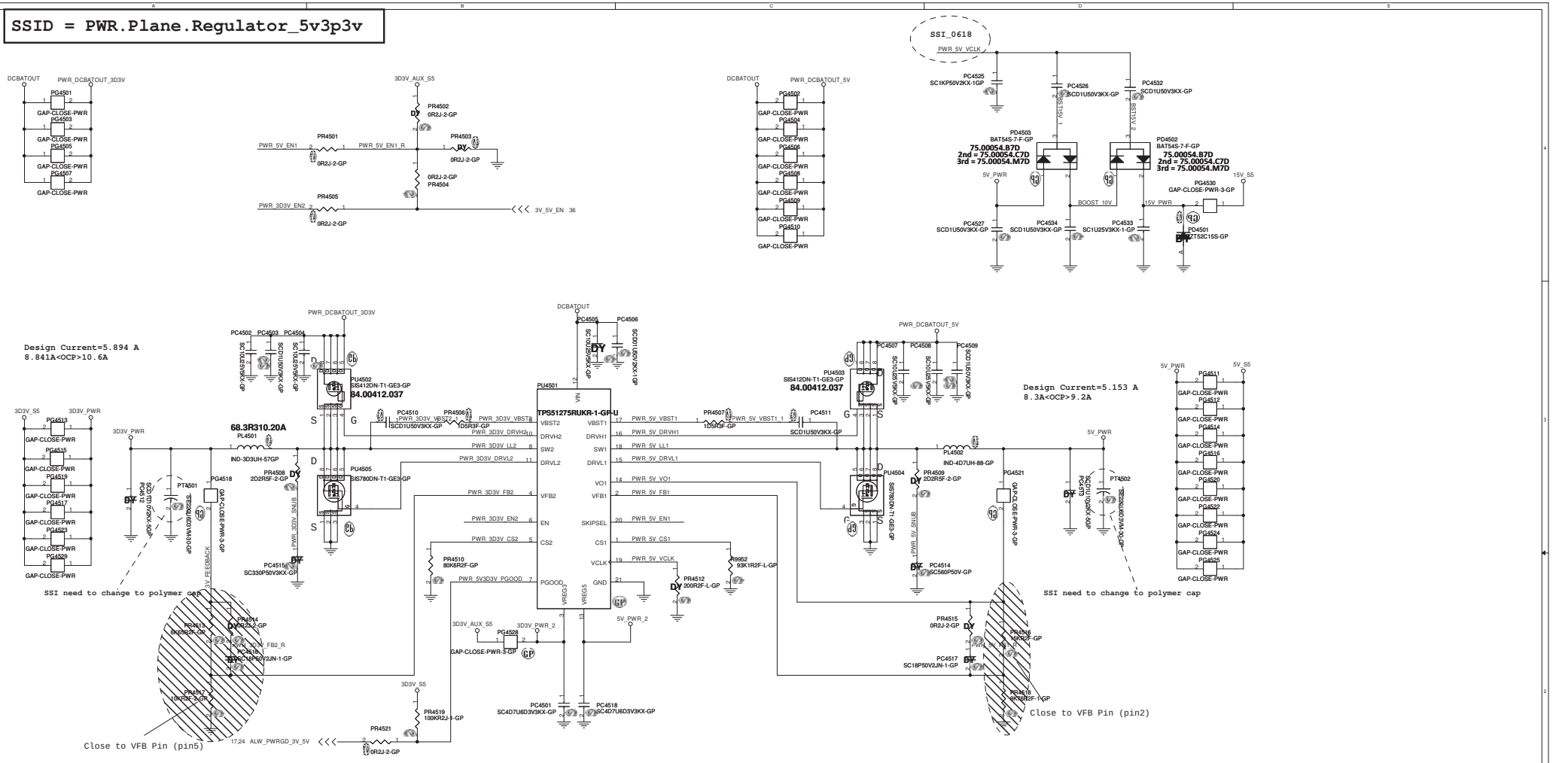
Taipei Hsien 221, Taiwan, R.O.C.

File: CHARGE(BQ24715)

Size: A4 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 08, 2012 | Sheet 44 of 59

SSID = PWR.Plane.Regulator_5v3p3v



I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

I/P cap: CHIP CAP C 10U 25V K0805 X5R/ 78.10622.51L
Inductor: CHIP IND 3.3UH PCMC063T-3R3MN Cyntec 28mohm/30mohm Isat =13.5Arms 68.3R310.20A
O/P cap: CHIP CAP POL 220U 6.3V M 6.3*4.5 /Matsuti/ 17mOhm / 77.52271.09L
H/S:SIS412DN-T1-GE3 / 24mOhm/30mOhm@4.5Vgs / 84.00412.037
L/S:SIS406DN-T1-GE3 / 11.5mOhm/14.5mOhm@4.5Vgs / 84.00406.037

<Core Design>

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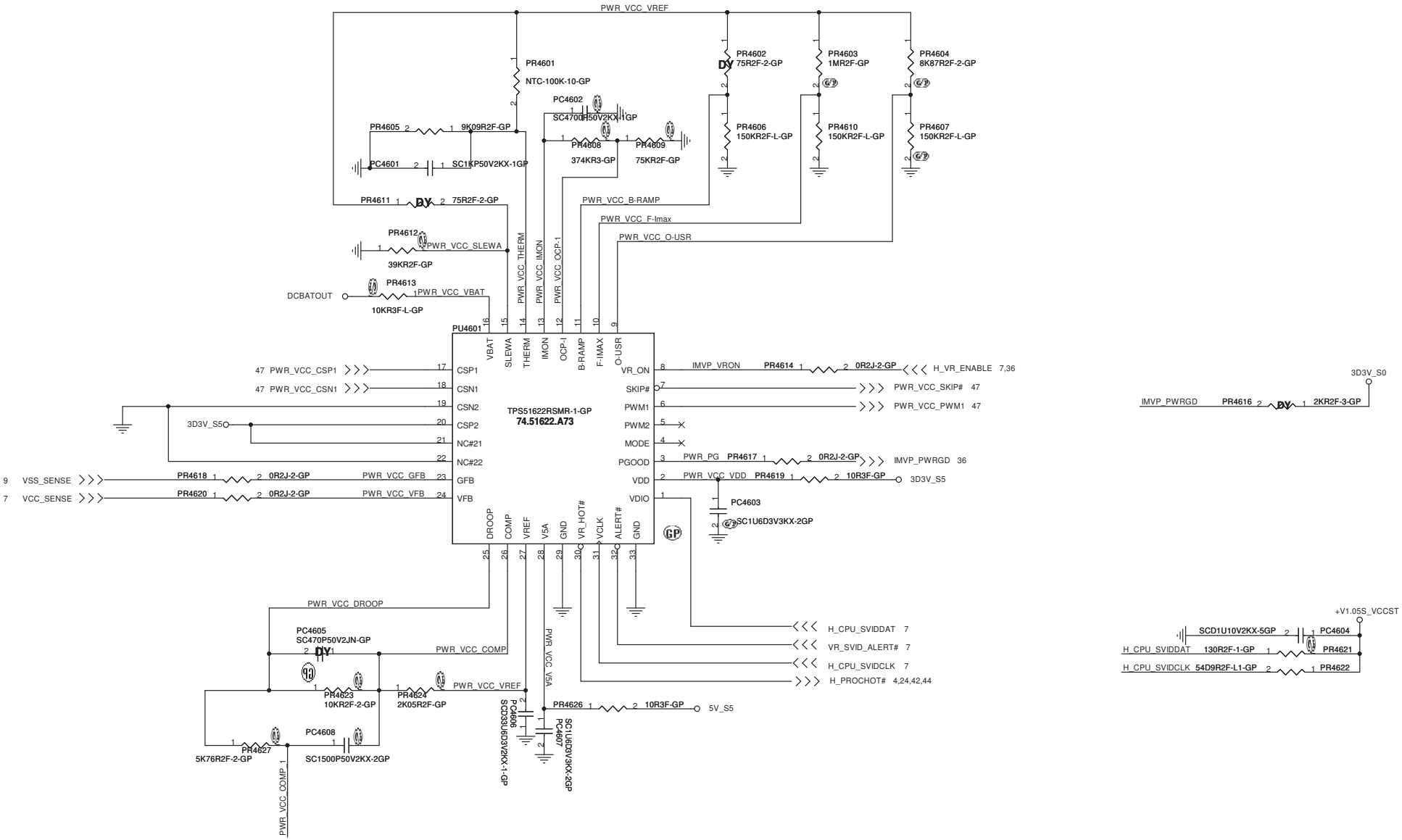
Taipei Hsien 221, Taiwan, R.O.C.

Title: 3V/5V TPS51275

Size	Document Number	Rev
A2	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 45 of 107

SSID = CPU.Regulator



<Core Design>

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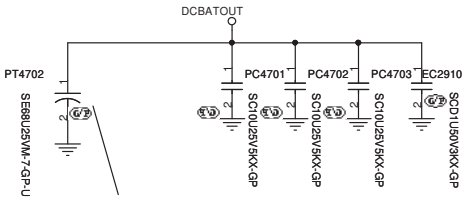
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51622_CPUCORE(1/2)

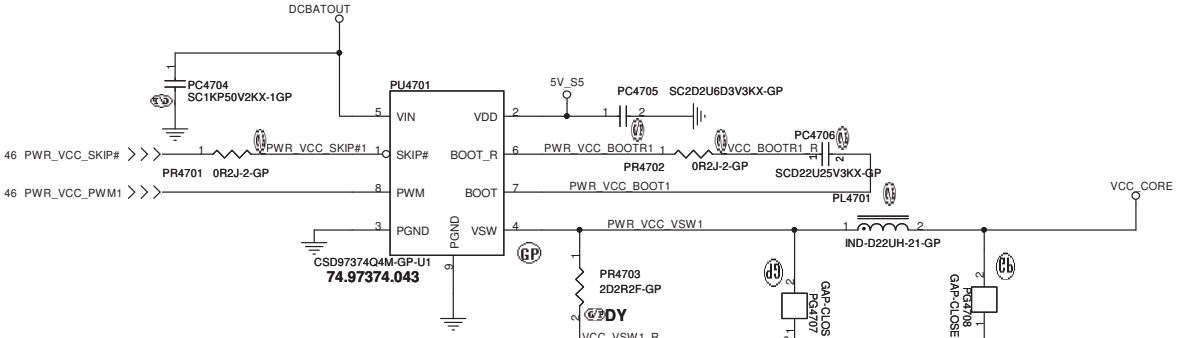
Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

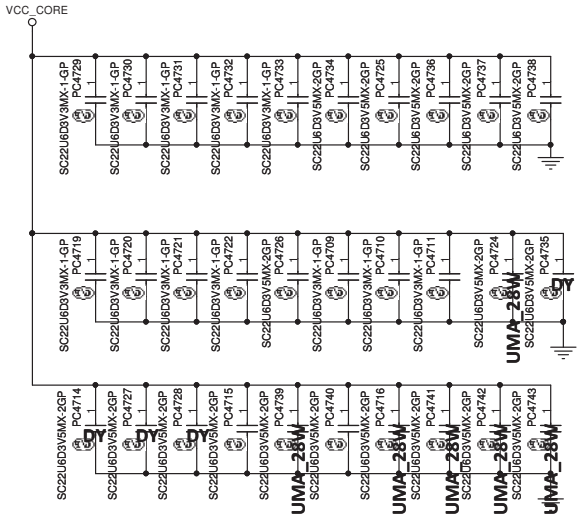
Date: Friday, June 28, 2013 | Sheet 46 of 107

SSID = CPU.Regulator



For acoustic noice





<Core Design>

Wistron Corporation
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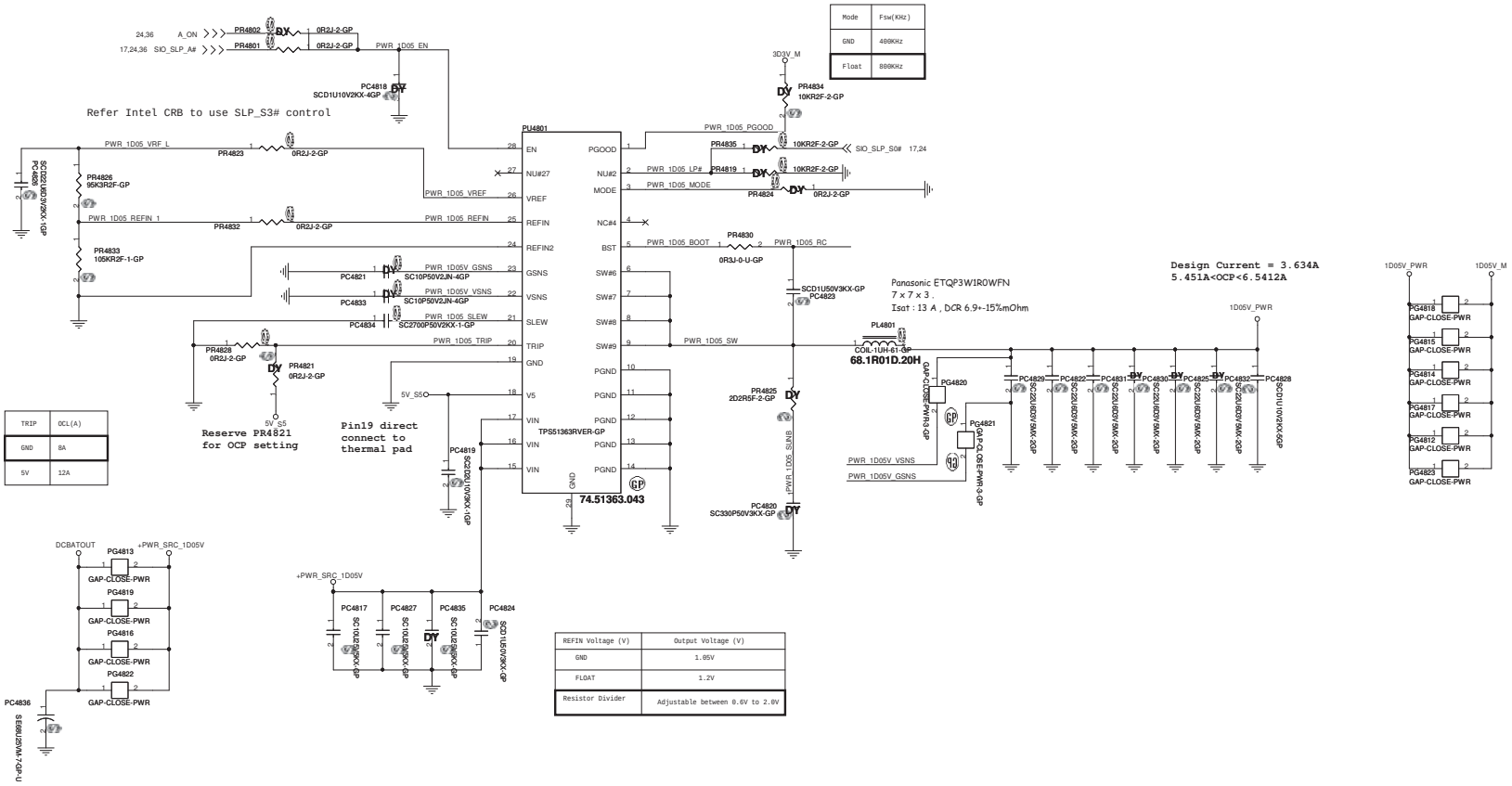
Title	TPS51622_CPUCORE(2/2)	
Size A3	Document Number Round Rock 13.3" UMA	Rev X00
Date: Friday, June 28, 2013	Sheet 47 of 107	

SSID = PWR.Plane.Regulator_1p05v



<Core Design>

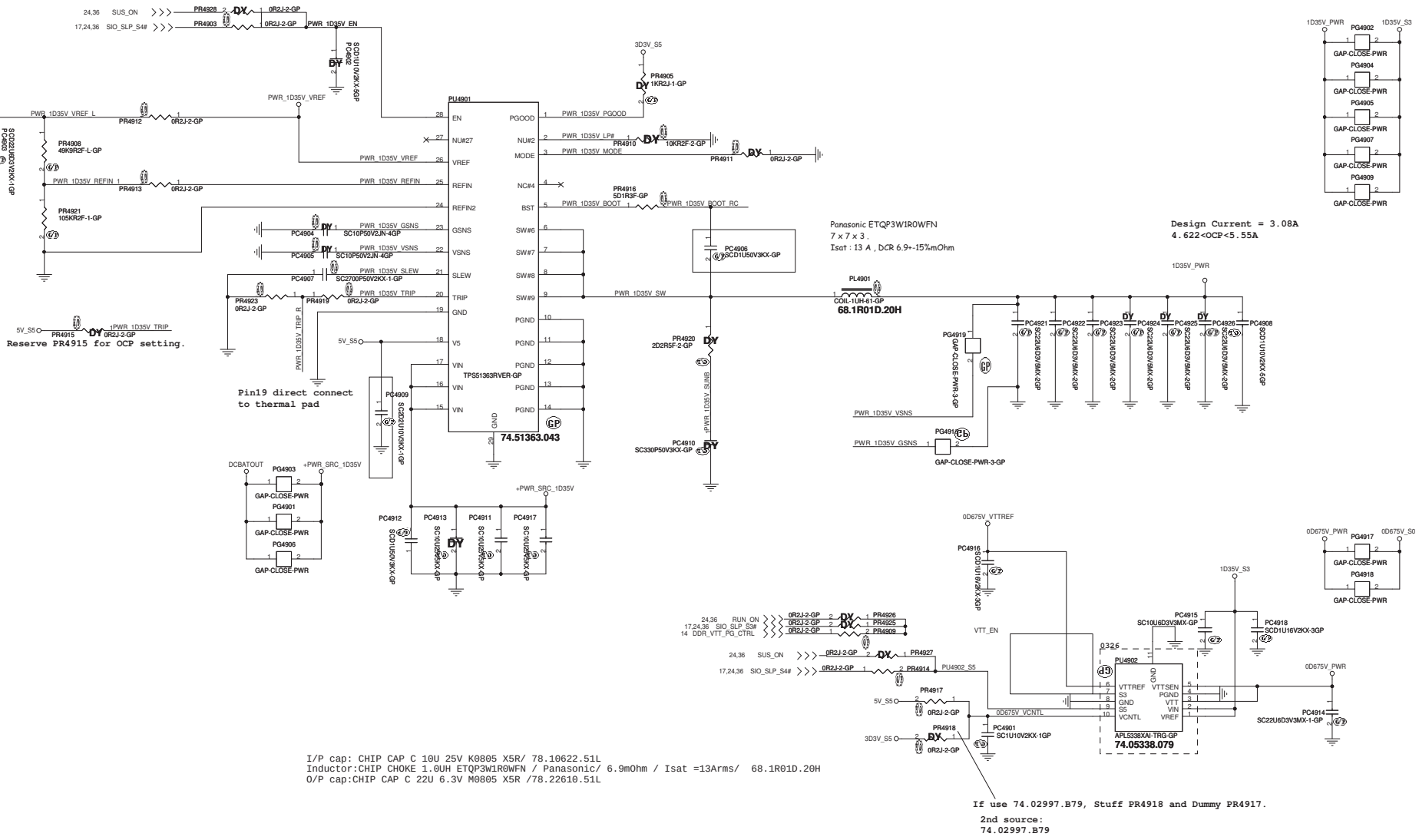
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363_1D05V_M

Size: A2 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 48 of 107

SSID = PWR.Plane.Regulator_1p35v0p675v



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: TPS51363+5338_1D35V & 0D675V

Size	Document Number	Rev
C	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 49 of 107

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<Core Design>

Wistron Corporation
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Title
Reserved

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	

Date: Friday, June 28, 2013 Sheet 50 of 107

(Blanking)

<Core Design>

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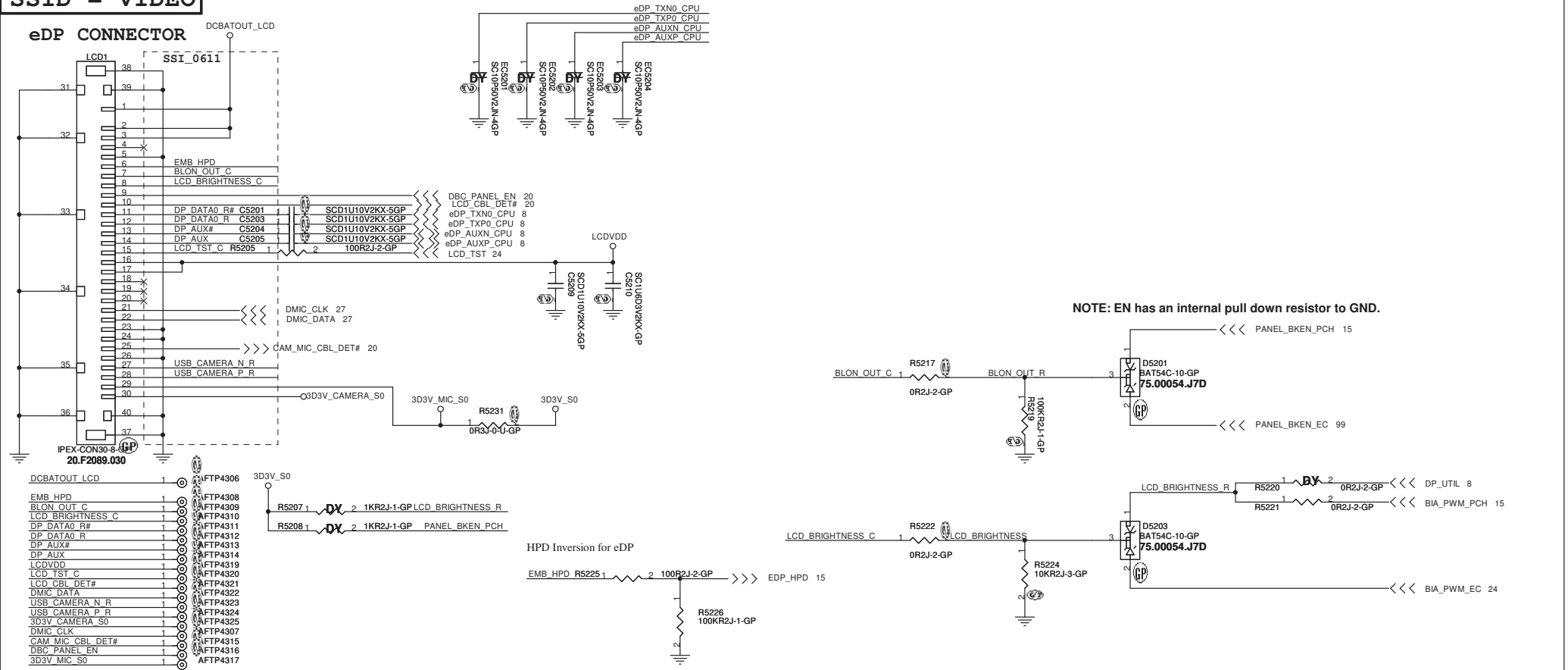
Title
Reserved

Size	Document Number	Rev
A4	*Round Rock 13.3" UMA*	*X00*

Date: Friday, June 28, 2013 Sheet 51 of 107

SSID = VIDEO

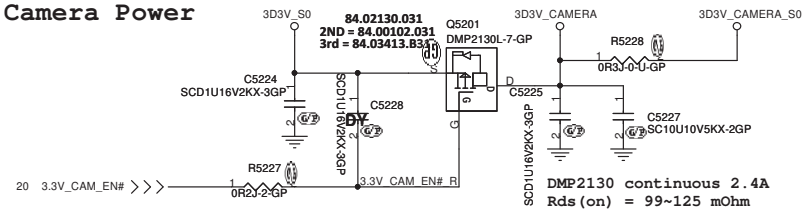
eDP CONNECTOR

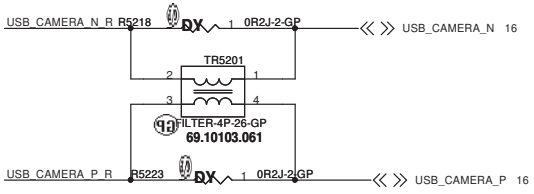


HPD Inversion for eDP

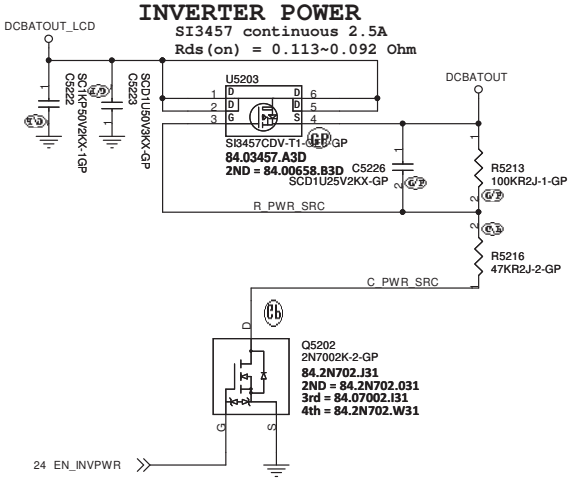
NOTE: EN has an internal pull down resistor to GND.

Camera Power





INVERTER POWER



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **eDP Connector**

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	X00

Date: Friday, June 28, 2013 Sheet 52 of 107

(Blanking)

<Core Design>

Wistron Corporation
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Title

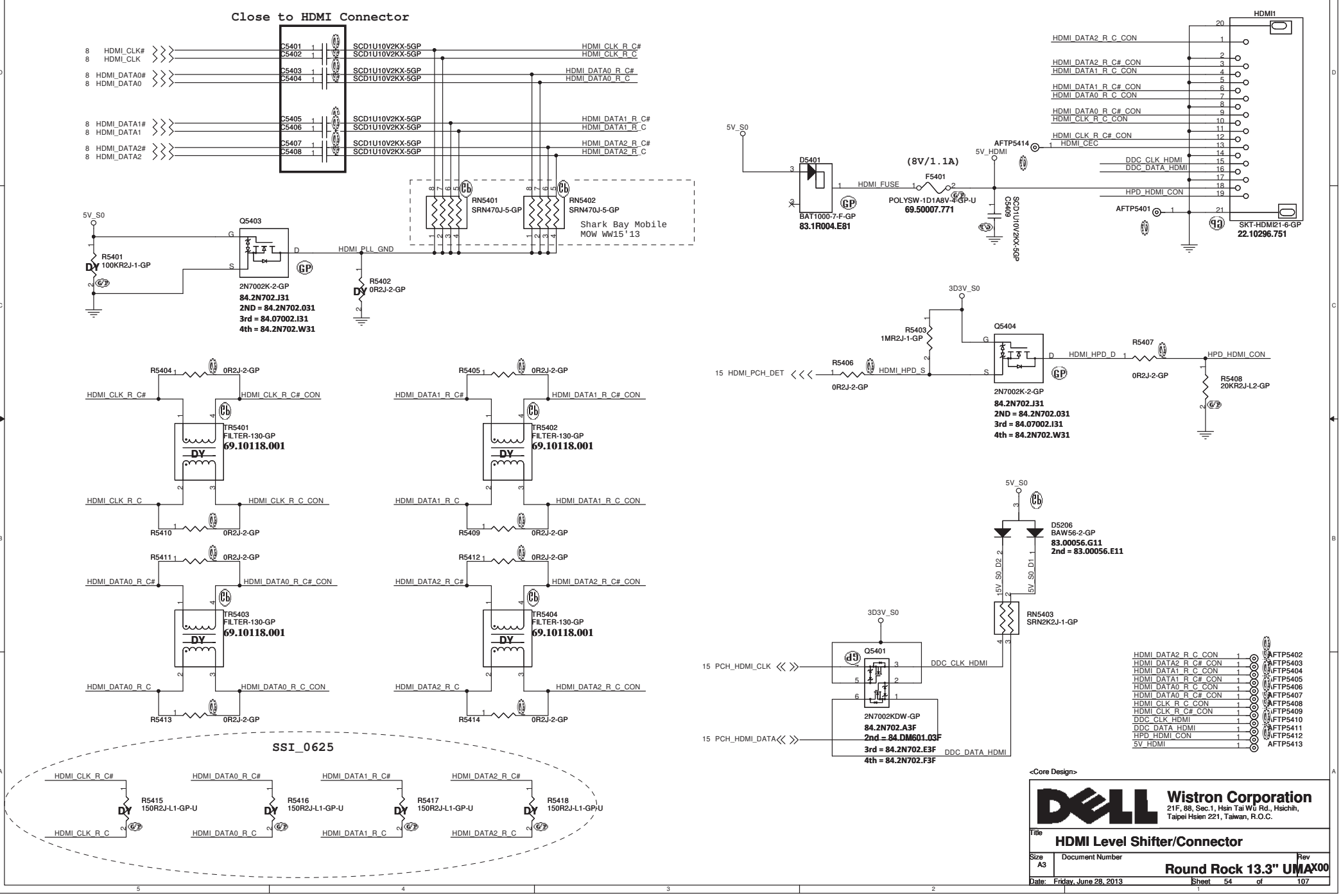
Reserved

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

Date: Friday, June 28, 2013 Sheet 53 of 107

SSID = VIDEO

HDMI CONNECTOR



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: **HDMI Level Shifter/Connector**

Size	Document Number	Rev
A3	Round Rock 13.3" UMA	AX00

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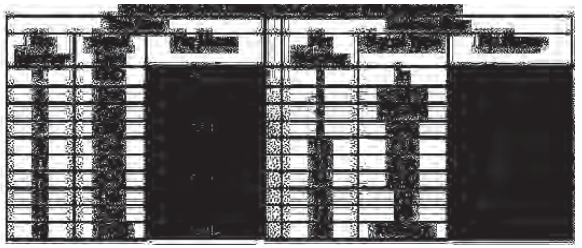
SSID = VIDEO

SSI_0625

INPUT		SWITCH
OE#	S	
L	L	nA to nB1
L	H	nA to nB2
H	X	Switch Off



SSI_0625

SSI_0626

SSI_0626

<Core Design>

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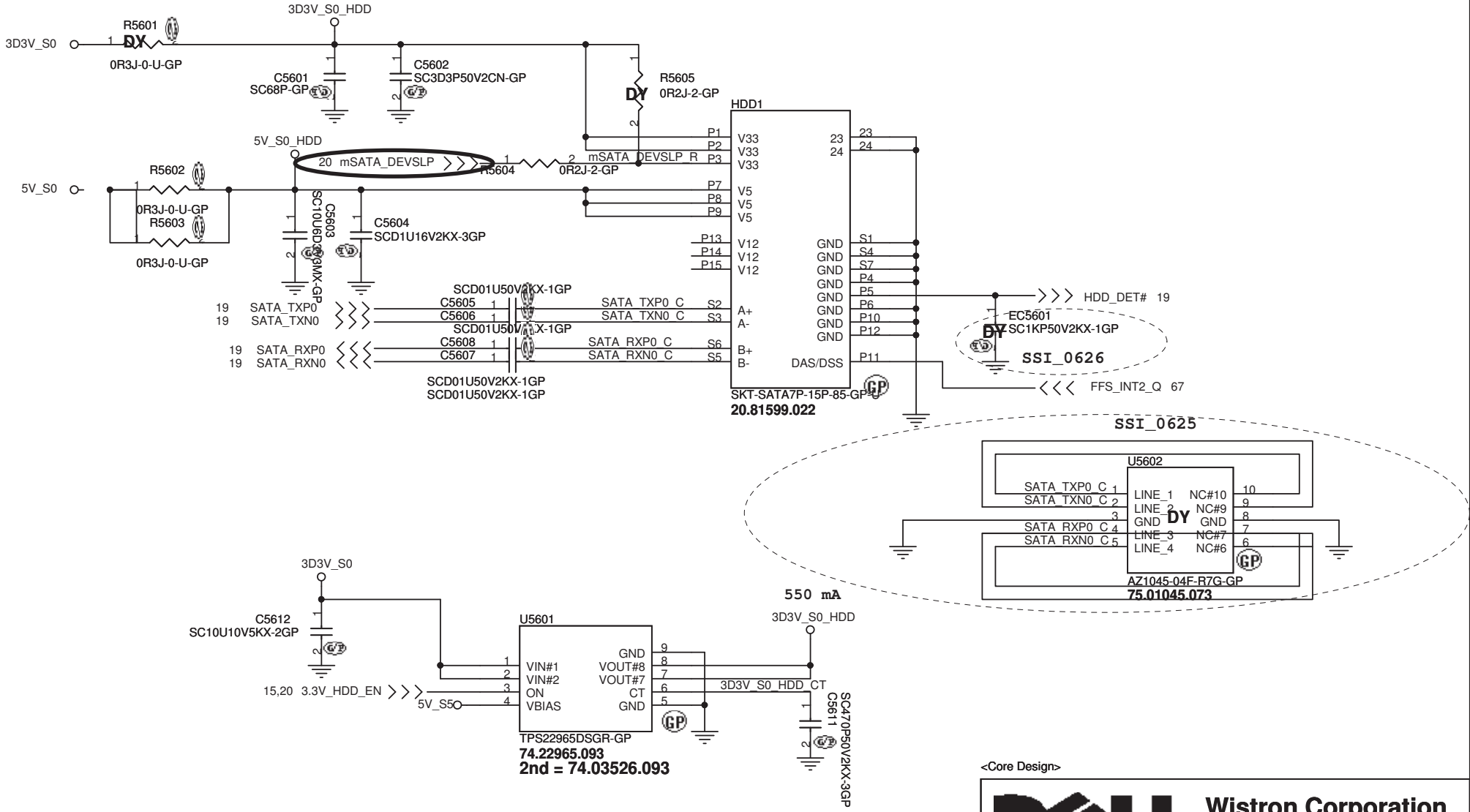
Title: Mini Display Port

Size: A3 | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 55 of 107

SSID = SATA



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *HDD*		
Size: A4	Document Number: *Round Rock 13.3" UMA*	Rev: *X00*
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<Core Design>

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Title

Reserved

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

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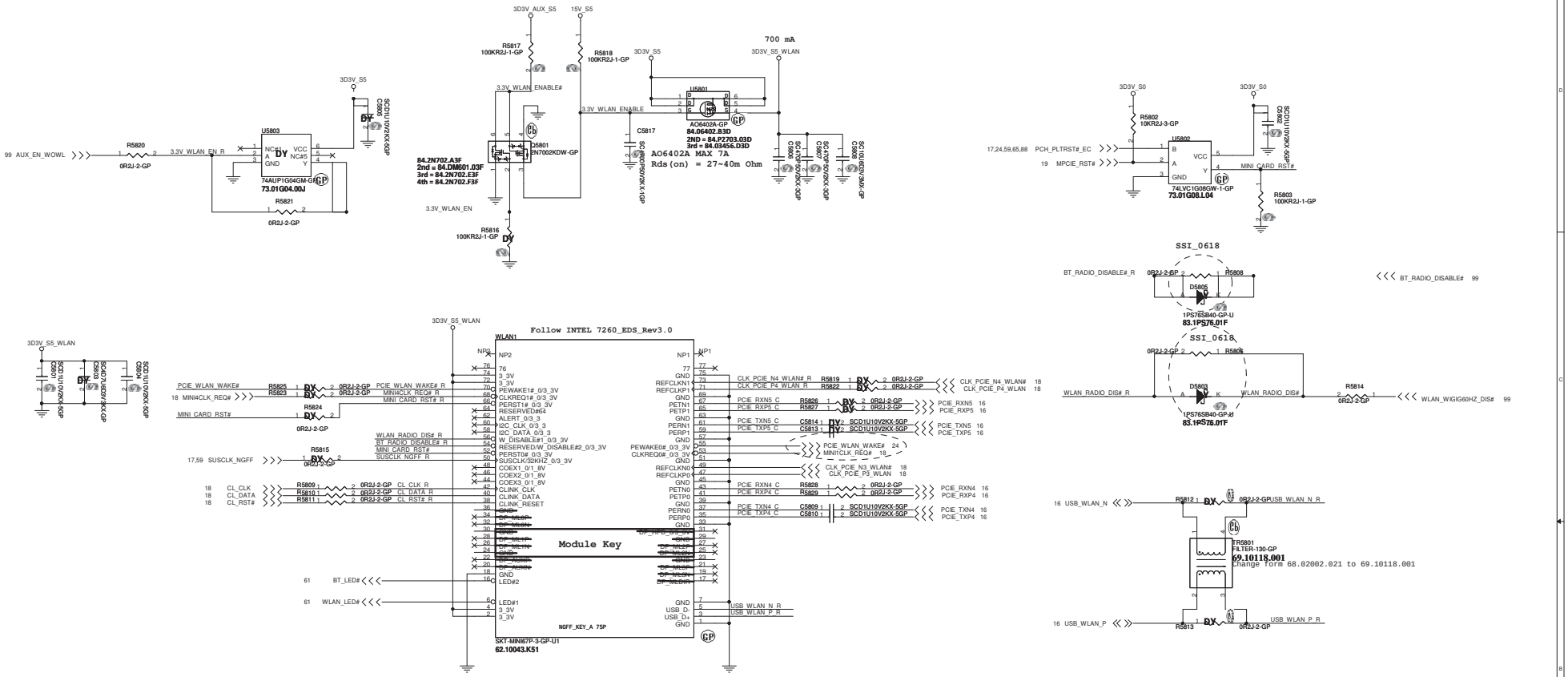
SSID = WIRELESS



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

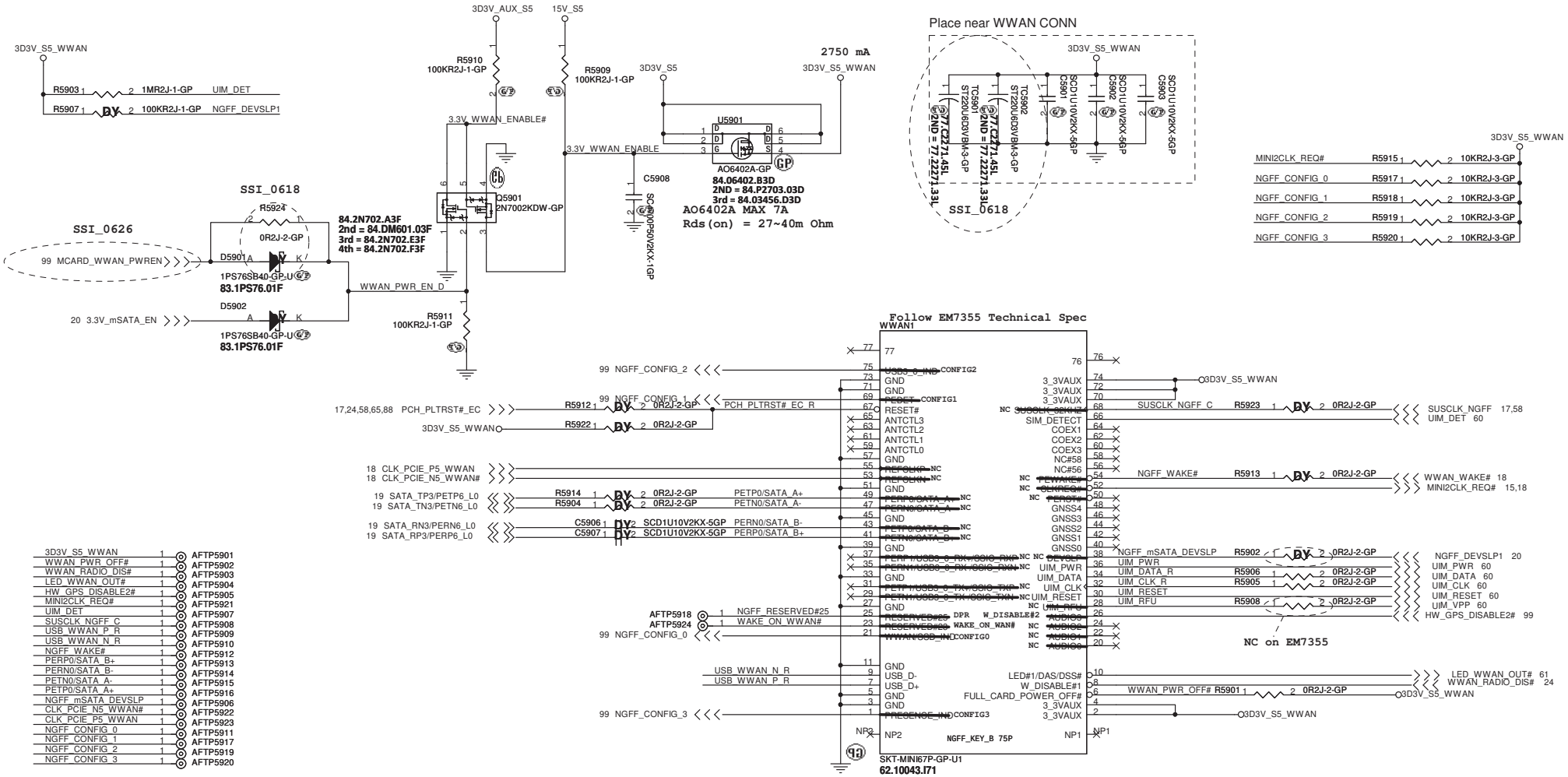
Title: **MINICARD(WLAN)**

Size: | Document Number: **Round Round 13.3" UMA** | Rev: **X00**

Date: Friday, June 28, 2013 | Sheet 58 of 107

SSID = WIRELESS

NGFF(WWAN/SSD)



STATE #	CONFIG_0	CONFIG_1	CONFIG_2	CONFIG_3	Module Type
0	GND	GND	GND	GND	SSD – SATA
1	GND	NC	GND	GND	SSD - PCIe
8	NC	GND	GND	GND	WWAN
14	NC	GND	NC	NC	HCA - PCIe
15	NC	NC	NC	NC	No Module Present

<Core Design>

Wistron Corporation
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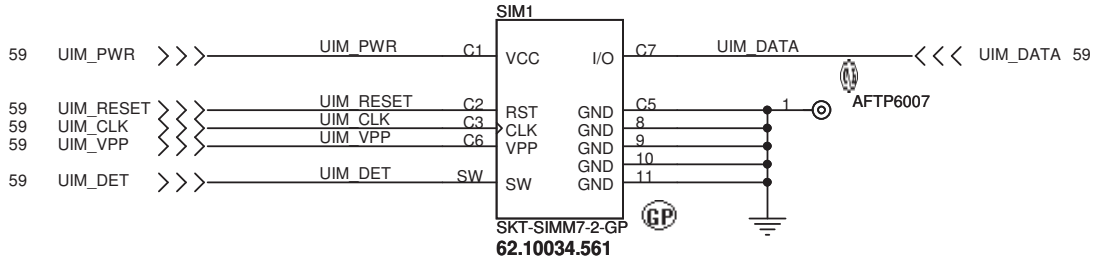
Taipei Hsien 221, Taiwan, R.O.C.

Title: NGFF-WWAN/SSD

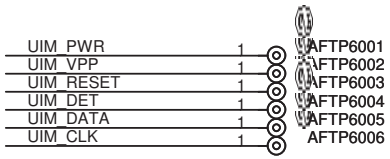
Size | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 59 of 107

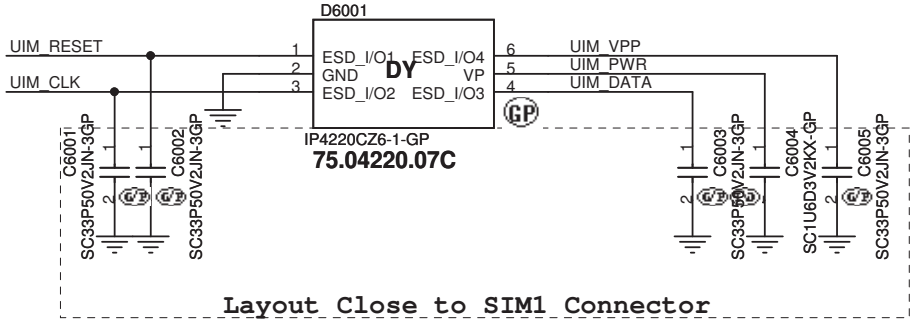
SSID =WIRELESS



PIN	62.10034.561 Micro SIM PinDefine
C1	VCC
C2	RST
C3	CLK
C4	Reserve
C5	GND
C6	VPP
C7	I/O
SW	SIM Card Detect
8	PTH GND
9	PTH GND
10	PTH GND
11	PTH GND



Change from 83.00005.BAE to 75.04220.07C



<Core Design>

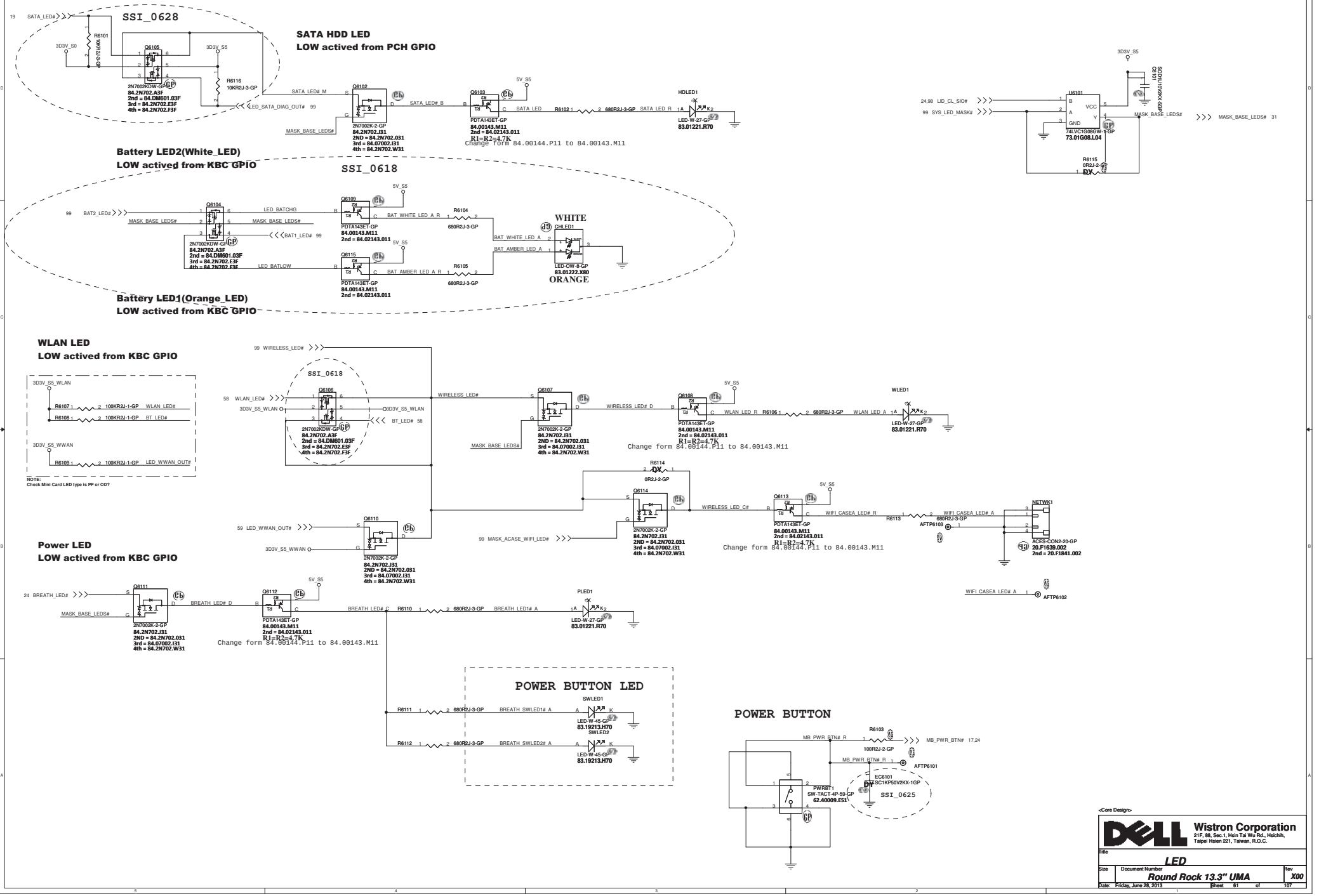
Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: mSATA

Size | Document Number: Round Rock 13.3" UMA | Rev: X00

Date: Friday, June 28, 2013 | Sheet 60 of 107

SSID = User.Interface



<Core Design>

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title	LED	
Size	Document Number: Round Rock 13.3" UMA	Rev: X00
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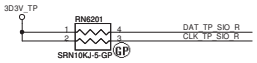
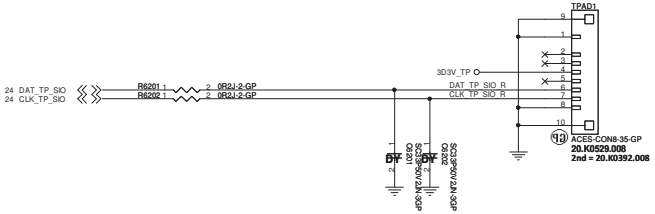
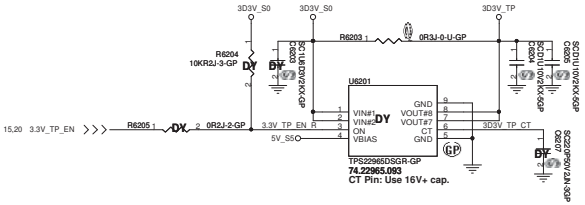
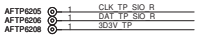
SSID = KBC	SSID = Touch.Pad



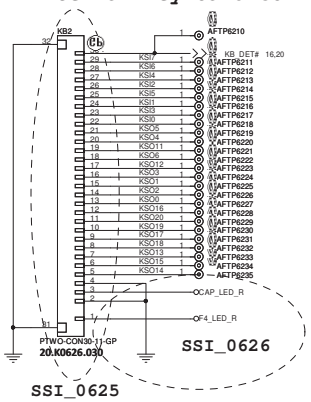
TouchPad Connector





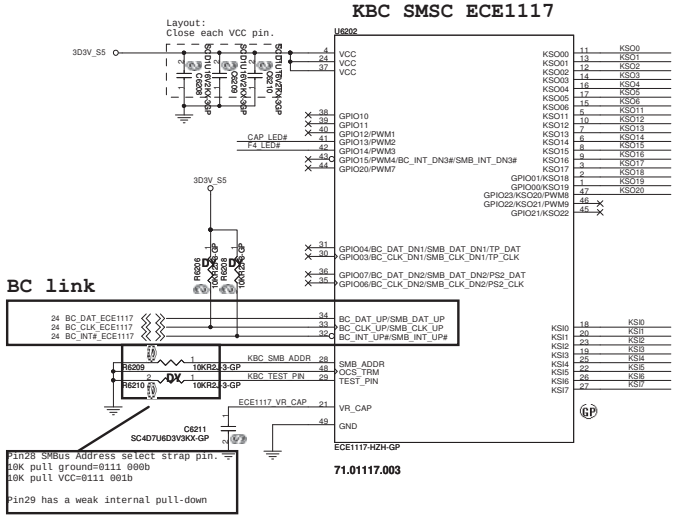


Internal KeyBoard Connector

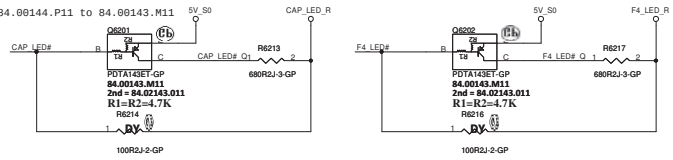


MB Pin NO.	Description	Module Pin NO.
30	Diagnostic	1
29	KSI[7]:S8	2
28	KSI[6]:S7	3
27	KSI[4]:S5	4
26	KSI[2]:S3	5
25	KSI[5]:S6	6
24	KSI[1]:S2	7
23	KSI[3]:S4	8
22	KSI[0]:S1	9
21	KSO[5]:D6	10
20	KSO[4]:D5	11
19	KSO[11]:D8	12
18	KSO[6]:D7	13
17	KSO[12]:D9	14
16	KSO[3]:D4	15
15	KSO[1]:D2	16
14	KSO[2]:D3	17
13	KSO[0]:D1	18
12	KSO[16]:D13	19
11	KSO[20]:D17	20
10	KSO[19]:D16	21
9	KSO[17]:D14	22
8	KSO[18]:D15	23
7	KSO[13]:D10	24
6	KSO[15]:D12	25
5	KSO[14]:D11	26
4	GND	27
3	Caps Lock LED	28
2	GND	29
1	F4 LED	30

KBC SMSC ECE1117



Change form 84.00144.P11 to 84.00143.M11



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: Key Board/Touch Pad

Size	Document Number	Rev
	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

IO CONN

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
Hall Sensor

Size	Document Number	Rev
	Round Rock 13.3" UMA	***X00***

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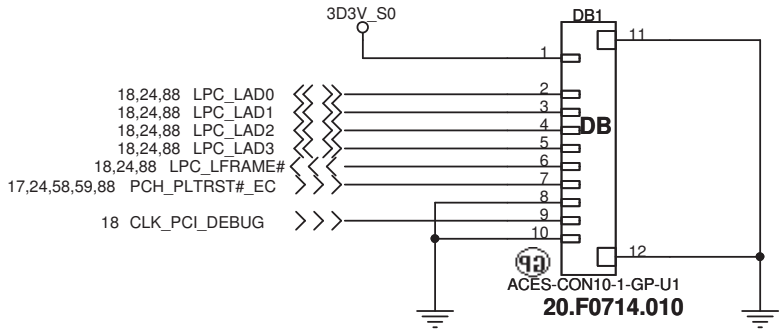
SSID = DEBUG PORT

SB modify to test pad



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title	***Debug connector***	
Size	Document Number: ***Round Rock 13.3" UMA***	Rev: ***X00***
Date: Friday, June 28, 2013	Sheet 65 of 107	

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

SENSOR

Size	Document Number	Rev
A3	**Round Rock 13.3" UMA**	**X00**

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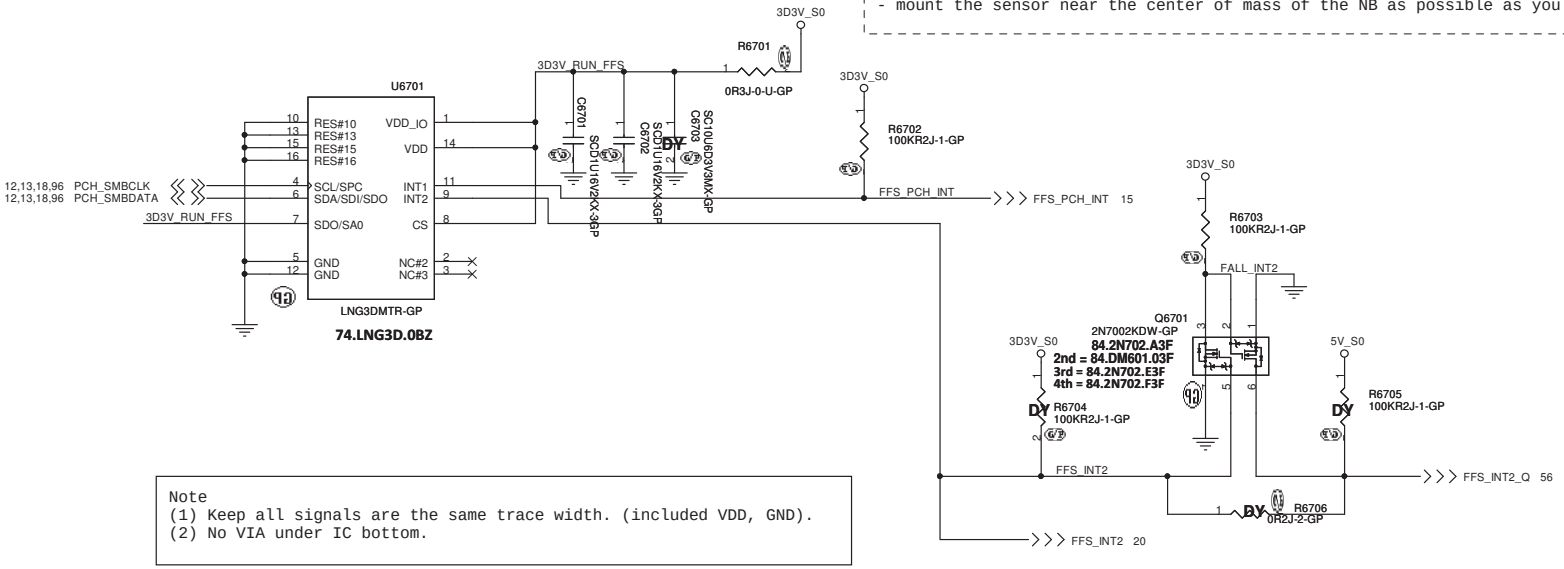
SSID = User.interface

Free Fall Sensor

Note
- no via, trace, under the sensor (keep out area around 2mm)
- stay away from the screw hole or metal shield soldering joints
- design PCB pad based on our sensor LGA pad size (add 0.1mm)
- solder stencil opening to 90% of the PCB pad size
- solder stencil opening to 90% of the PCB pad size
- mount the sensor near the center of mass of the NB as possible as you can



Note
(1) Keep all signals are the same trace width. (included VDD, GND).
(2) No VIA under IC bottom.

<Core Design>

Wistron Corporation
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Title	Free Fall Sensor	
Size A3	Document Number: Round Rock 13.3" UMA	Rev X00
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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: *Thunderbolt (1/5)*

Size: A3 | Document Number: *Round Rock 13.3" UMA* | Rev: *X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

Thunderbolt (2/5)

Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title	***Thunderbolt (3/5)***	
Size: A	Document Number: ***Round Rock 13.3" UMA***	Rev: ***X00***
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<Core Design>

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Title

Thunderbolt (4/5)

Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

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<Core Design>

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Title

Thunderbolt (5/5)

Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title

GPU (1/5) PEG

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

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Title

GPU (2/5) DIGITAL

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
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Title
GPU (3/5) VRAM

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
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Title

GPU (4/5) GPIO

Size	Document Number	Rev
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<Core Design>

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Title

GPU (5/5) PWR/GND

Size	Document Number	Rev
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<Core Design>

Wistron Corporation
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Title
VRAM1,2 (1/4)

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
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Title

VRAM3,4 (2/4)

Size	Document Number	Rev
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<Core Design>

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Title

VRAM5,6 (3/4)

Size	Document Number	Rev
A	***Round Rock 13.3" UMA***	***X00***

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<Core Design>

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Title
VRAM7,8 (4/4)

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

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Title

VGA_CORE

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

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Title

DISCRETE VGAPOWER

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
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Title

Switchable GFXLCD

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
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Title

Switchable GFXCRT

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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DCBATOUT SC1KP50V2KX-1GP FC8601
DCBATOUT SC1KP50V2KX-1GP FC8602
DCBATOUT SC1KP50V2KX-1GP EC8601
DCBATOUT SC1KP50V2KX-1GP EC8604
DCBATOUT SC1KP50V2KX-1GP EC8605

5V_S5 SC1KP50V2KX-1GP FC8603
5V_S5 SC1KP50V2KX-1GP FC8614
5V_S5 SC1KP50V2KX-1GP FC8615
5V_S5 SC1KP50V2KX-1GP FC8616

3D3V_S0 SC1KP50V2KX-1GP FC8611
3D3V_S0 SC1KP50V2KX-1GP FC8612

SPR1 SPRING-52-GP **34.4T025.001**
SPR2 SPRING-52-GP **34.4T025.001**
SPR3 SPRING-52-GP **34.4T025.001**

SPR4 SPRING-64-GP **34.4H602.001**
SPR5 SPRING-64-GP **34.4H602.001**
SPR6 SPRING-64-GP **34.4H602.001**
SPR7 SPRING-64-GP **34.4H602.001**
SPR8 SPRING-64-GP **34.4H602.001**

H1 HOLE335R115-GP **ZZ.00PAD.D01**
H2 HOLE335R115-GP **ZZ.00PAD.D01**
H3 HOLE335R115-GP **ZZ.00PAD.D01**
H4 HOLE335R115-GP **ZZ.00PAD.D01**
H5 HOLE335R115-GP **ZZ.00PAD.D01**
H6 HOLE335R115-GP **ZZ.00PAD.D01**
H7 HT85B95X975R29-S-GP **ZZ.00PAD.D71**
H8 HT85B95X975R29-S-GP **ZZ.00PAD.D71**
H9 HOLE335R115-GP **ZZ.00PAD.D01**

H10 HOLE197R166-1-GP **ZZ.00PAD.V71**
H11 HOLE197R166-1-GP **ZZ.00PAD.V71**
H12 HOLE197R166-1-GP **ZZ.00PAD.V71**
H13 HOLE197R99-1-GP **ZZ.00PAD.J71**

HS1 STF236R126H101-GP **34.4Z003.001**
HS2 STF237R113H63-GP **34.44P03.101**
HS3 STF236R126H101-GP **34.4Z003.001**

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: ***UNUSED PARTS/EMI Capacitors***

Size	Document Number	Rev
	Round Rock 13.3" UMA	***X00***

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SSID = USH

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<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title: *USH Board Connector*

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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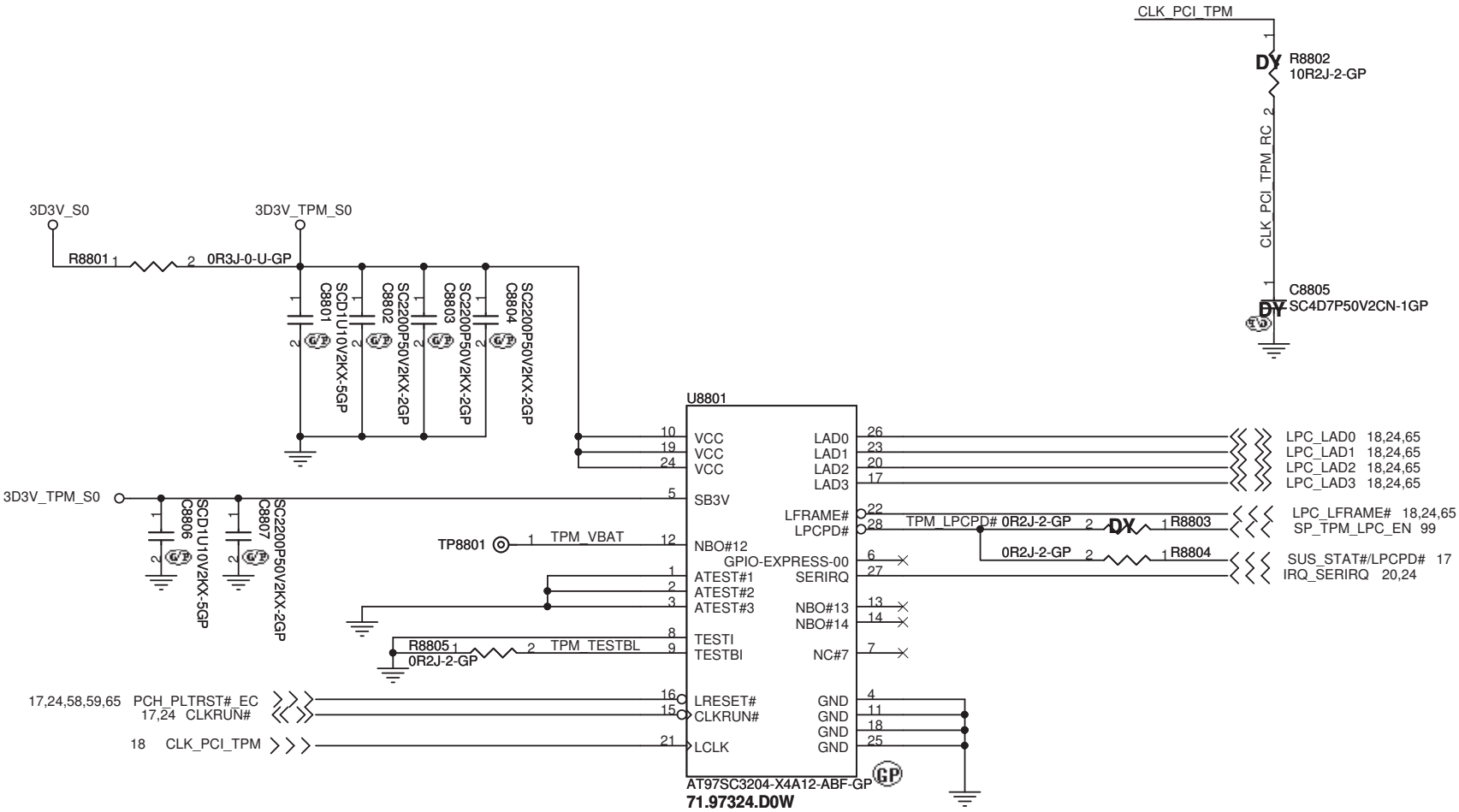
SSID = TPM

Place close to Pin 21



<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title: ***TPM***		
Size	Document Number: ***Round Rock 13.3" UMA***	Rev: ***X00***
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<Core Design>

Wistron Corporation
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Title: Finger Print

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title
NFC Connector

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Smart Card

Size	Document Number	Rev
	Round Rock 13.3" UMA	*X00*

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<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title
Reserved

Size	Document Number	Rev
A	Round Rock 13.3" UMA	X00

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SSID = Docking

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<Core Design>

Wistron Corporation
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Title
DOCKING

Size	Document Number	Rev
A4	Round Rock 13.3" UMA	X00

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SSID = LOM

PM_LANPHY_ENABLE
C9401 SCD1U10V2KX-5GP DY

NOTE:PM_LANPHY_ENABLE must be connected to PCH's GPIO12/LAN_PHY_PWR_CTRL. This GPIO12 pin must be set as "LAN_PHY_PC" function through FITC tool.

3D3V_LAN
R9401 DY 4K7R2F-GP LAN_WAKE#_R

NOTE:LANWAKE must be connected to PCH's GPIO27

U9401

18,20 LANCLK_REQ# — CLK_REQ#
LAN_RST#_R — PE_RST#
18 CLK_PCIE_LAN — PE_CLKP
18 CLK_PCIE_LAN# — PE_CLKN
16 PCIE_RXP3 — C9402 SCD1U10V2KX-5GP PCIE_RXDP3 — PETP
16 PCIE_RXN3 — C9403 SCD1U10V2KX-5GP PCIE_RXDN3 — PETN
16 PCIE_TXP3 — PERP
16 PCIE_TXN3 — PERN
PCIE

MDI_PLUS0 / MDI_MINUS0 — LAN_MDI0P_INTEL 31 / LAN_MDI0N_INTEL 31
MDI_PLUS1 / MDI_MINUS1 — LAN_MDI1P_INTEL 31 / LAN_MDI1N_INTEL 31
MDI_PLUS2 / MDI_MINUS2 — LAN_MDI2P_INTEL 31 / LAN_MDI2N_INTEL 31
MDI_PLUS3 / MDI_MINUS3 — LAN_MDI3P_INTEL 31 / LAN_MDI3N_INTEL 31
MDI

18 LOM_SMBCLK — RN9401 SRN0J-6-GP — LOM_SMBCLK_R — SMB_CLK
18 LOM_SMBDAT — LOM_SMBDAT_R — SMB_DATA
SMBUS

20,24 LAN_WAKE# — R9405 0R2J-2-GP LAN_WAKE#_R — LANWAKE#
20 PM_LANPHY_ENABLE — R9406 0R2J-2-GP LAN_DISABLE# — LAN_DISABLE#
99 LAN_DISABLE#_R — R9418 0R2J-2-GP

31 LOM_ACTLED_YEL# — LED0
31 LOM_SPD100LED_ORG# — LED1
31 LOM_SPD10LED_GRN# — LED2
LED

3D3V_LAN
TP8802 LAN_JTAG_TDI — JTAG_TDI
TP8803 LAN_JTAG_TDO — JTAG_TDO
R9407 DY 10KR2J-3-GP LAN_JTAG_TMS — JTAG_TMS
R9408 DY 10KR2J-3-GP LAN_JTAG_TCK — JTAG_TCK
JTAG

LANXOUT_C — XTAL_OUT
LANXIN_C — XTAL_IN

R9409 1KR2J-1-GP TEST_EN — TEST_EN
R9410 3K01R2F-3-GP RBIAS — RBIAS

WGI218V-GP
71.00218.B03

SVR_EN_N — R9402 0R2J-2-GP
SVR_EN# — R9403 DY 4K7R2F-GP — 3D3V_LAN
RSVD1_VCC3P3 — RSVD1_VCC3P3 — R9404 4K7R2F-GP

VDD3P_IN / VDD3P3_4 / VDD3P3_15 / VDD3P3_19 / VDD3P3_29 — 3D3V_LAN
C9404 SCD1U10V2KX-5GP
C9405 SC1U16D3V2KX-GP
C9406 SC22U6D3V5MX-2GP

VDD0P9_8 / VDD0P9_11 / VDD0P9_16 / VDD0P9_22 / VDD0P9_37 / VDD0P9_40 / VDD0P9_43 / VDD0P9_46 / VDD0P9_47 — VDD0P9_LAN
CTRL0P9 — CTRL_0P9 — L9401 IND-4D7UH-192-GP **68.4R750.20C** DCR=50mohm
GND
C9407 SC22U6D3V3MX-1-GP
C9408 SCD1U10V2KX-5GP
C9409 DY SC10U6D3V3MX-GP

0D9V Power Options
SVR_EN_N: Pull High External
Pull Low Internal

Internal SVR	*Shared with external 1.05V SVR*
L9401: STUFF	*L9401: NO STUFF*
R9413: NO STUFF	*R9413: STUFF*
R9402: STUFF	*R9402: NO STUFF*
R9403: NO STUFF	*R9403: STUFF*

*NOTE: Clarkville has 0.9V internal SVR. However it is also possible to disable this 0.9V iSVR and Clarkville can support the external 1.05V supply. When sharing, make sure the 1.05V_LAN is controlled by the SLP_LAN signal.

Note : LAN Chip must be changed to I218LM (71.00218.E03)

3D3V_LAN
R9411 DY 10KR2F-GP
LAN_DISABLE#_R
R9412 DY 10KR2F-GP

3D3V_LAN
SCD1U10V2KX-5GP C9410
LOM_SPD10LED_GRN# — U9402 B
LOM_SPD100LED_ORG# — A
GND
VCC
Y — WLAN_LAN_DISBL# 24
74LVC1G08GW-1-GP
73.01G08.L04
Connect to EC

C9411 SC12P50V2JN-3GP
LANXOUT_C
X9401 XTAL-25MHZ-155-GP **82.30020.D41**
LANXIN_C
C9413 SC12P50V2JN-3GP

NOTE: In most designs Cstray=~6 pF, so C7=C8 should be ~24 pF as a good starting point for a Cload=18 pF crystal. If 24 pF cap is not available, 22 pF or 27 pF value can be used as a starting point. Value will vary depending on the specific board layout stackup and which crystal part is used. Each design should check crystal's ppm to make sure it is within the Clarkville specification

3D3V_S0
R9414 10KR2F-GP
17 PLTRST_LAN# — U9403 B
20 LAN_RST# — A
GND
VCC
Y — LAN_RST#_R
74LVC1G08GW-1-GP
73.01G08.L04
R9416 100KR2J-1-GP
3D3V_S0
SCD1U10V2KX-5GP C9412

<Core Design>

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
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Title: **LAN INTEL WGI218LM**
Size: A3 | Document Number: **Round Rock 13.3" UMA** | Rev: X00
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<Core Design>

Wistron Corporation
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Title

LAN SW

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	*X00*

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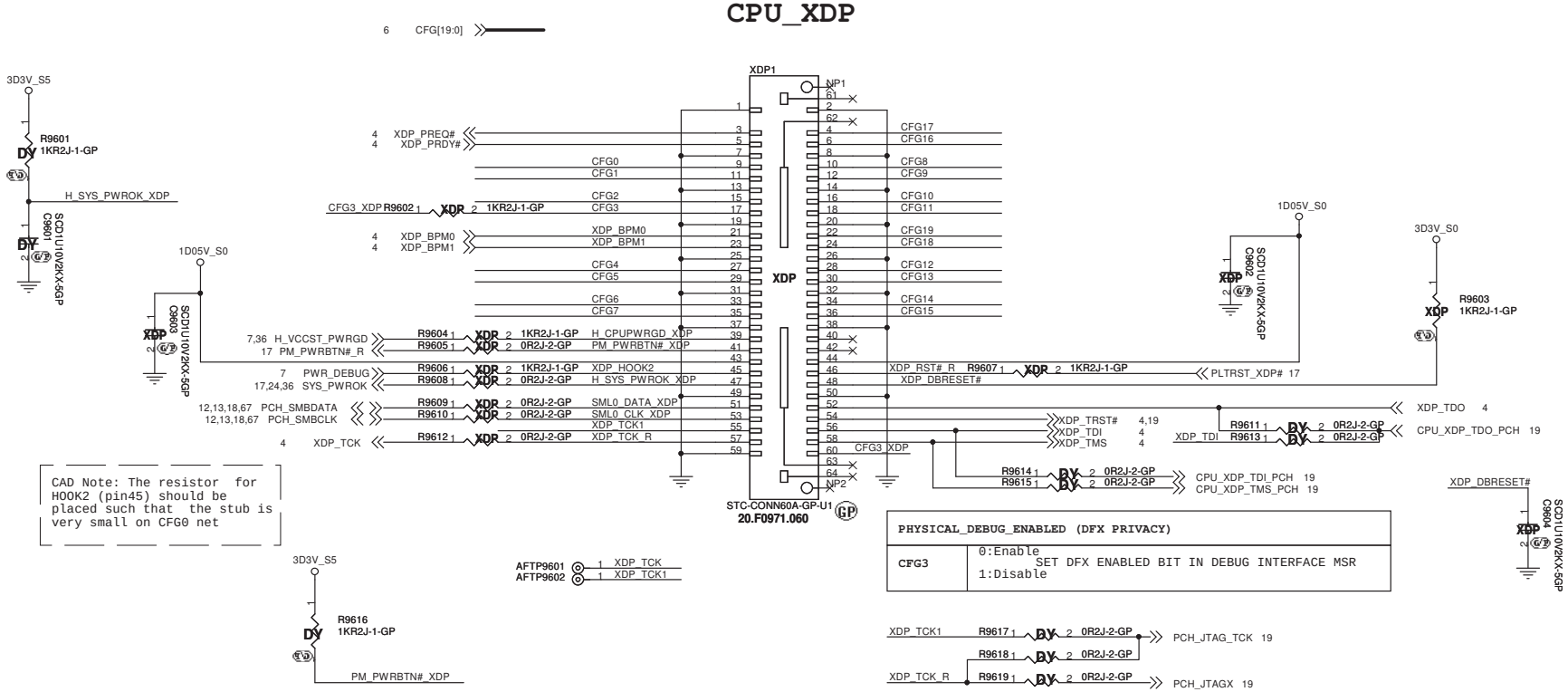
SSID = CPU_XDP

CPU_XDP



PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	
CFG3	0:Enable SET DFX ENABLED BIT IN DEBUG INTERFACE MSR 1:Disable

<Core Design>

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Title		
CPU_XDP		
Size: A3	Document Number: Round Rock 13.3" UMA	Rev: X00
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<Core Design>

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Title

USB2.0 HUB

Size	Document Number	Rev
A4	***Round Rock 13.3" UMA***	***X00***

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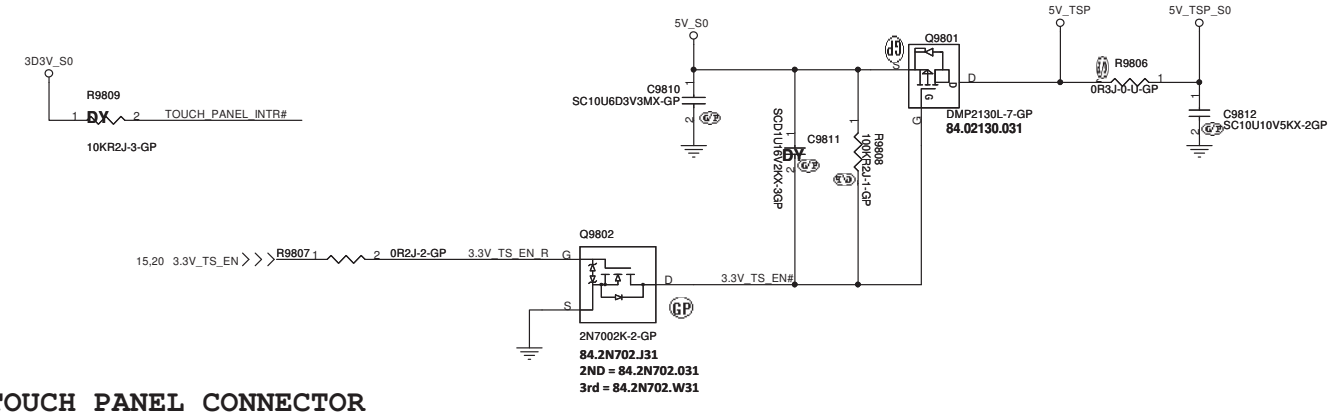
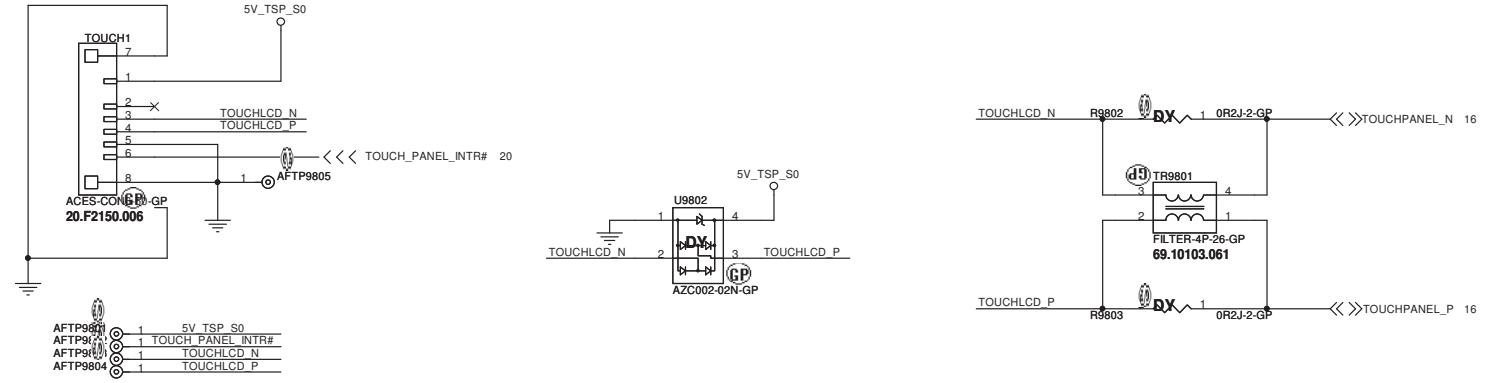
SSID = User.Interface

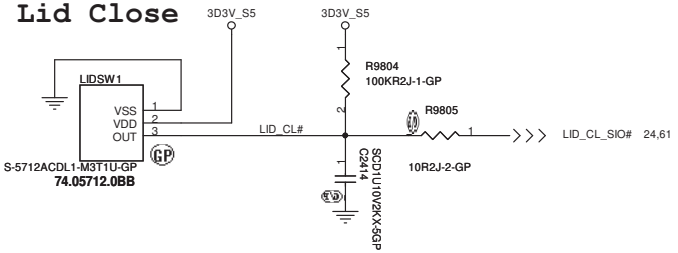
TOUCH PANEL POWER



TOUCH PANEL CONNECTOR



Lid Close



<Core Design>

Wistron Corporation
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Title: Function Button

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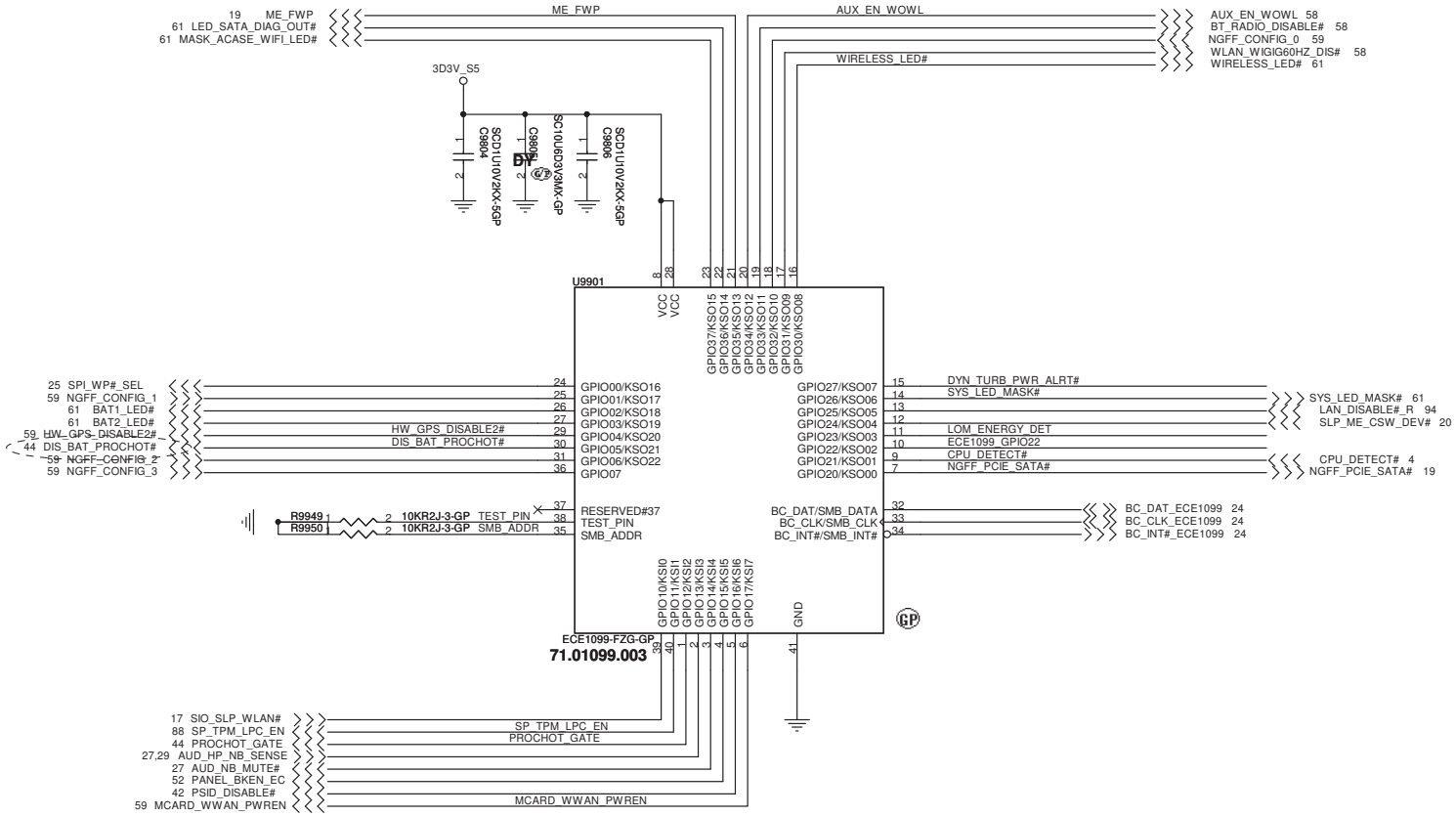
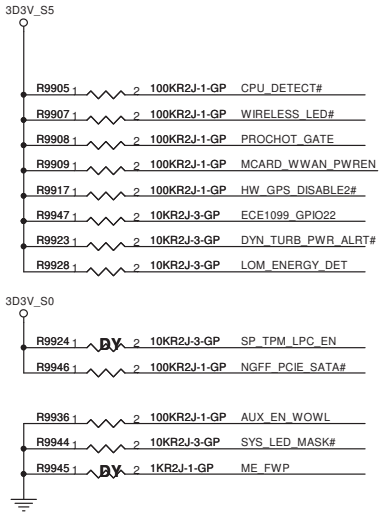
SSID = SIO





<Core Design>

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Title: SIO - ECE1099

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