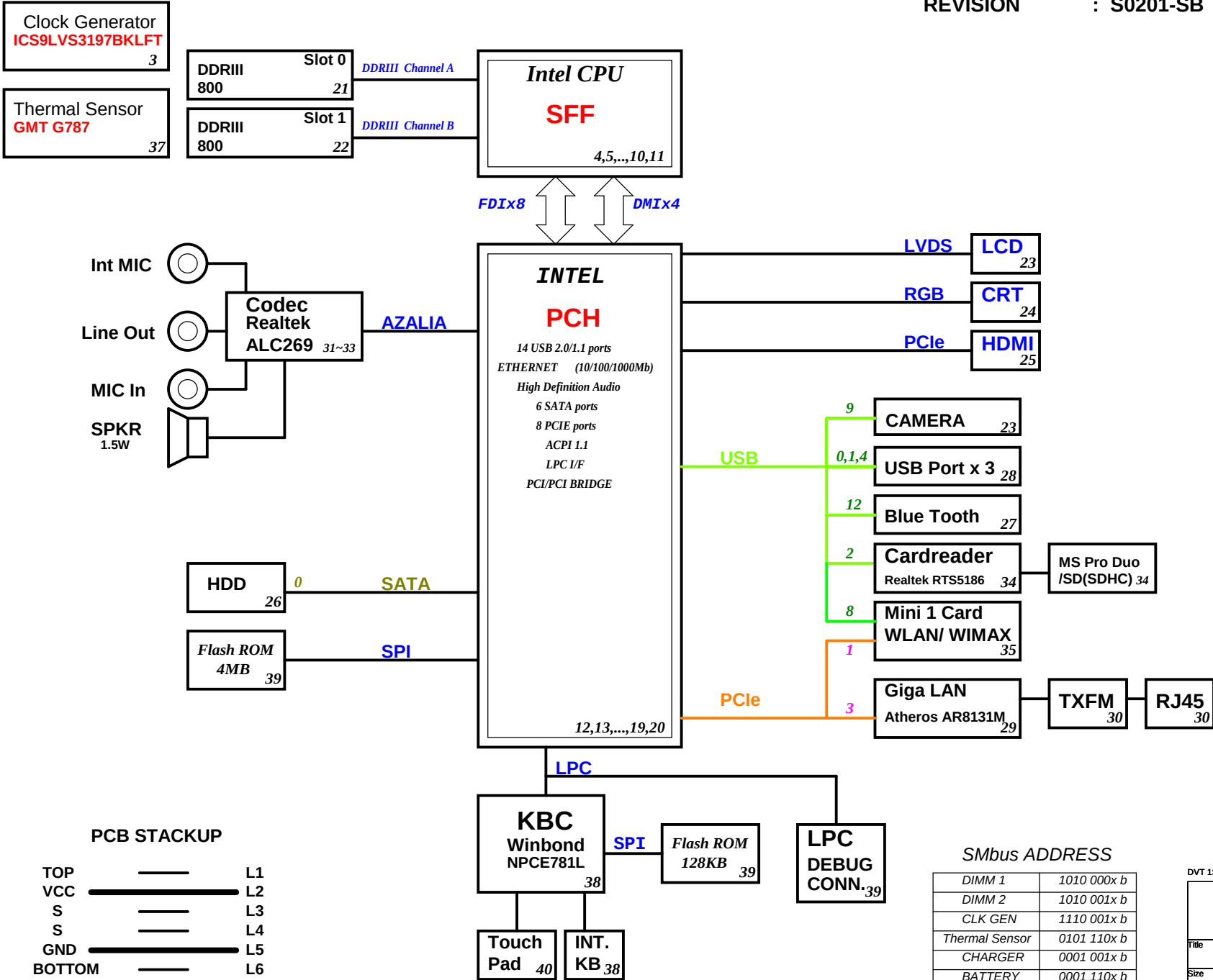


TUCANA Block Diagram

PROJECT CODE : 91.4KK01.001
PCB P/N : 48.4KK01.0SB
REVISION : S0201-SB

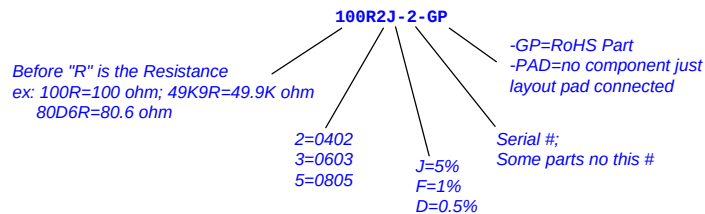


SYSTEM DC/DC RT8223		47
INPUTS	OUTPUTS	
DCBATOUT	5V_S5(6A)	
	3D3V_S5(5A)	
	5V_AUX_S5	
	3D3V_AUX_S5	
RT8209		49
INPUTS	OUTPUTS	
DCBATOUT	1D05V_S0(20A)	
RT8209		48
INPUTS	OUTPUTS	
DCBATOUT	1D5V_S3(9.4A)	
RT9026		51
INPUTS	OUTPUTS	
5V_S5	DDR_VREF_S3	1.2A
CHARGER BQ24751		52
INPUTS	OUTPUTS	
DCBATOUT	CHG_PWR	18V 6.0A
CPU DC/DC ADP3211		46
INPUTS	OUTPUTS	
DCBATOUT	VCC_CORE	27A
GFX Core ADP3211		50
INPUTS	OUTPUTS	
DCBATOUT	VCC_GFXCORE	11A

PCH Strapping

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-down. Do not pull high.
GNT3#/ GPIO55	Default Mode: Internal pull-up. Low (0) = Top Block Swap Mode (Connect to ground with 4.7-kΩ weak pull-down resistor).
INTVRMEN	High (1) = Integrated VRM is enabled Low (0) = Integrated VRM is disabled
GNT0#, GNT1#	Default (SPI): Left both GNT0# and GNT1# floating. No pull up required. Boot from PCI: Connect GNT1# to ground with 1-kΩ pull-down resistor. Leave GNT0# Floating. Boot from LPC: Connect both GNT0# and GNT1# to ground with 1-kΩ pull-down resistor.
GNT2#/ GPIO53	Default - Internal pull-up. Low (0)= Configures DMI for ESI compatible operation (for servers only. Not for mobile/desktops).
GPIO33	Default: Do not pull low. Disable ME in Manufacturing Mode: Connect to ground with 1-kΩ pull-down resistor.
SPI_MOSI	Enable iTPM: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable iTPM: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to Vcc3_3 with 8.2-kΩ weak pull-up resistor. Disable Danbury: Connect to ground with 4.7-kΩ weak pull-down resistor.
NC_CLE	Weak internal pull-up. Do not pull low.
HAD_DOCK_EN#/ GPIO[33]	Low (0): Flash Descriptor Security will be overridden. High (1) : Flash Descriptor Security will be in effect.
HDA_SDO	Weak internal pull-down. Do not pull high.
HDA_SYNC	Weak internal pull-down. Do not pull high.
GPIO15	Weak internal pull-down. Do not pull high.
GPIO8	Weak internal pull-up. Do not pull low.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

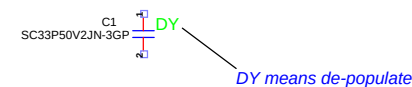
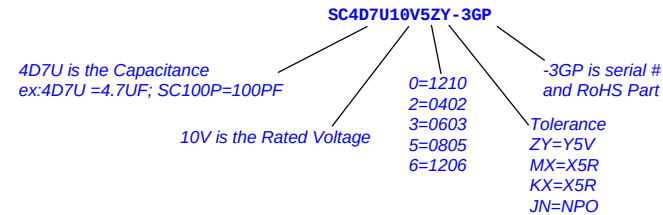
Resistor



Processor Strapping

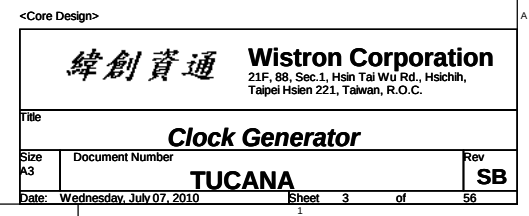
Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[4]	Embedded DisplayPort Presence	1: Disabled - No Physical Display Port attached to Embedded DisplayPort. 0: Enabled - An external Display Port device is connected to the Embedded Display Port.	1
CFG[3]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[0]	PCI-Express Configuration Select	1: Single PCI-Express Graphics 0: Bifurcation enabled	1
CFG[7]	Reserved - Temporarily used for early Clarksfield samples.	Clarksfield (only for early samples pre-ES1) - Connect to GND with 3.01K Ohm/5% resistor Note: Only temporary for early CFD samples (rPGA/BGA) [For details please refer to the WW33 MoW and sighting report]. For a common motherboard design (for AUB and CFD), the pull-down resistor should be used. Does not impact AUB functionality.	0

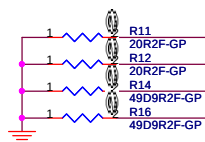
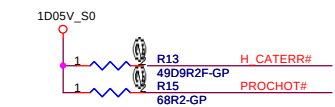
Capacitor



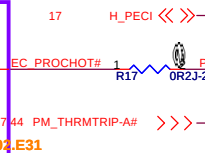
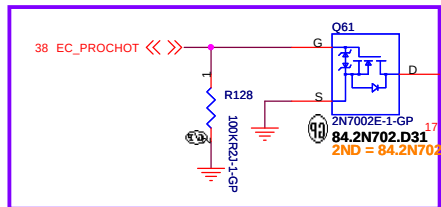
DVT 1ST

緯創資通		Wistron Corporation	
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.			
Title			
Reference			
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A3		SB	
Date: Wednesday, July 07, 2010		Sheet	2 of 56





DVT 2010702



From PCH

14 PM_DRAM_PWRGD >>>

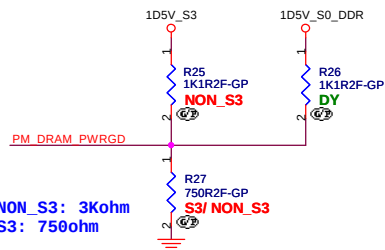
49 H_VTTPWRGD >>>

16,29,34,35,38,39,44 PLT_RST# >>>

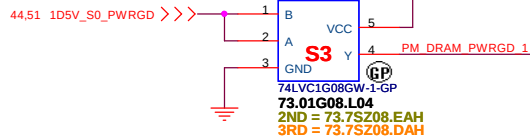
1K5R2F-2-GP

R23 750R2F-GP

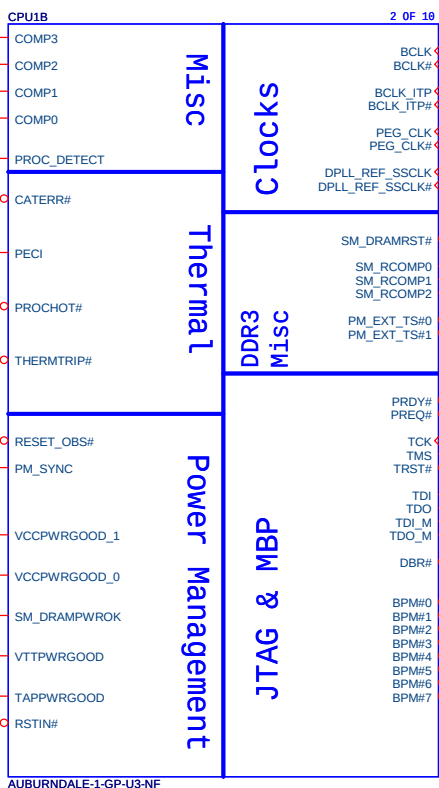
PM_DRAM_PWRGD 1 1K5R2F-2-GP PM_DRAM_PWRGD 1
S3



NON_S3: 3Kohm
S3: 750ohm



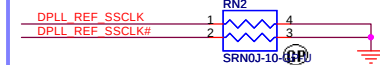
U2 74LVC1G08GW-1-GP
73.01G08.L04
2ND = 73.7SZ08.EAH
3RD = 73.7SZ08.DAH



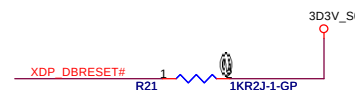
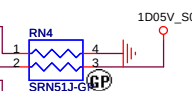
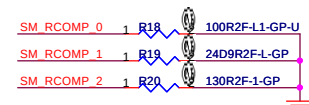
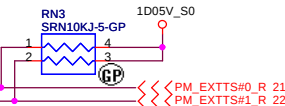
Clocks

DDR3 Misc

JTAG & MBP



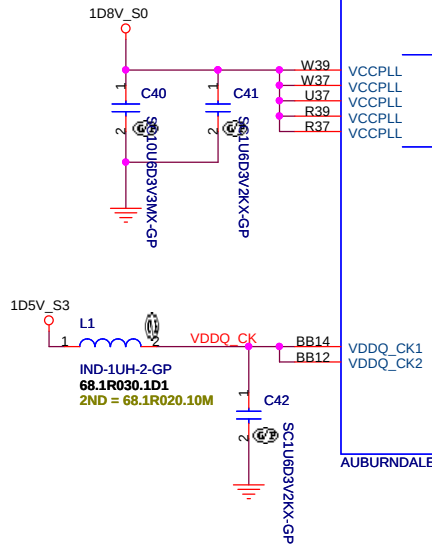
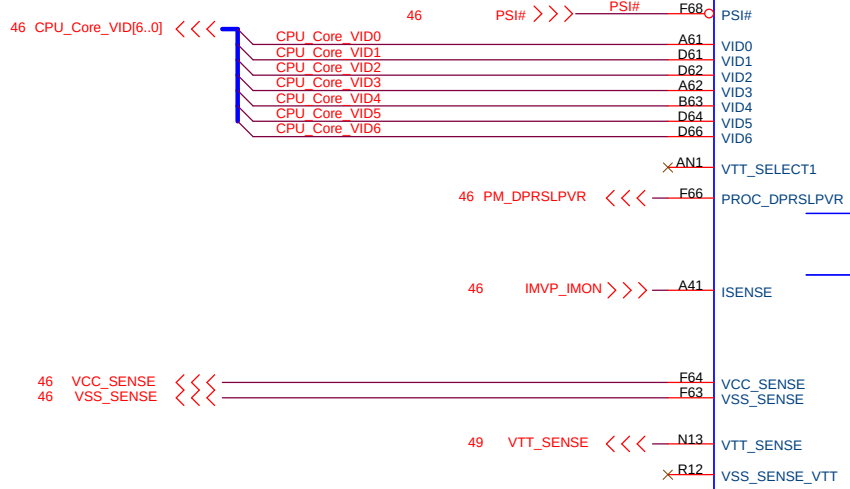
If supports integrated graphics but without Embedded DisplayPort(eDP), these pins can also be connected to GND directly.



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Title		CPU SFF 2 of 8(CLK/Thermal)	
Size	Document Number	Rev	
A3		SB	
Date: Wednesday, July 07, 2010		Sheet 5 of 56	



Please note that the VTT Rail Values are Auburndale
 VTT=1.05V; Clarksfield
 VTT=1.1V

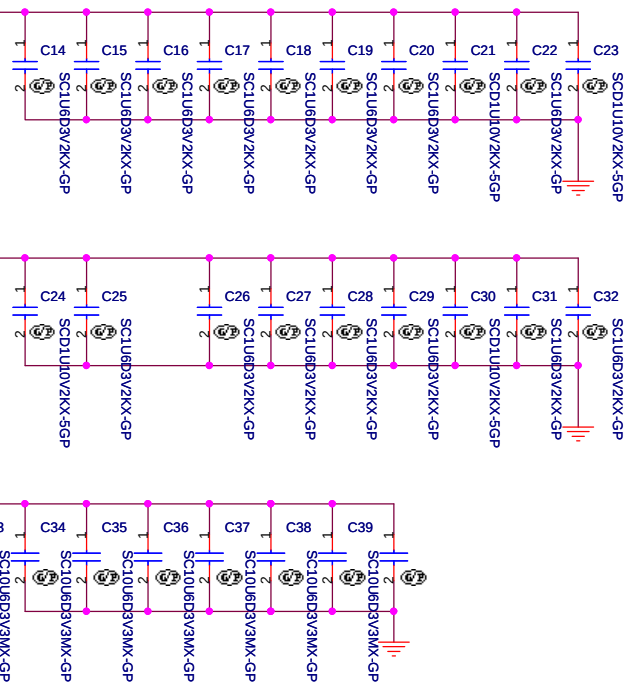
CPU VIDS

SENSE LINES

1.8V POWER

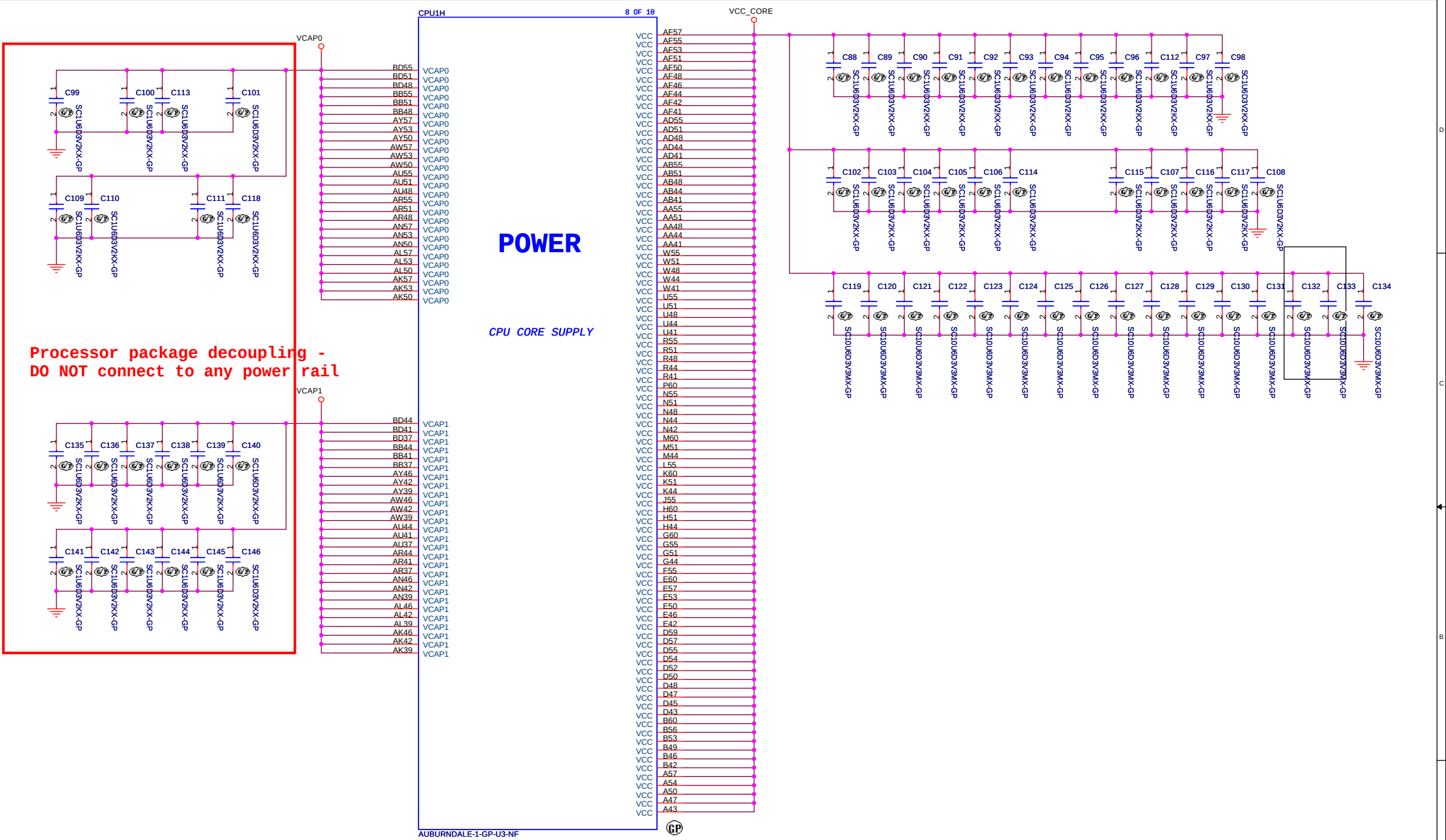
6 OF 10

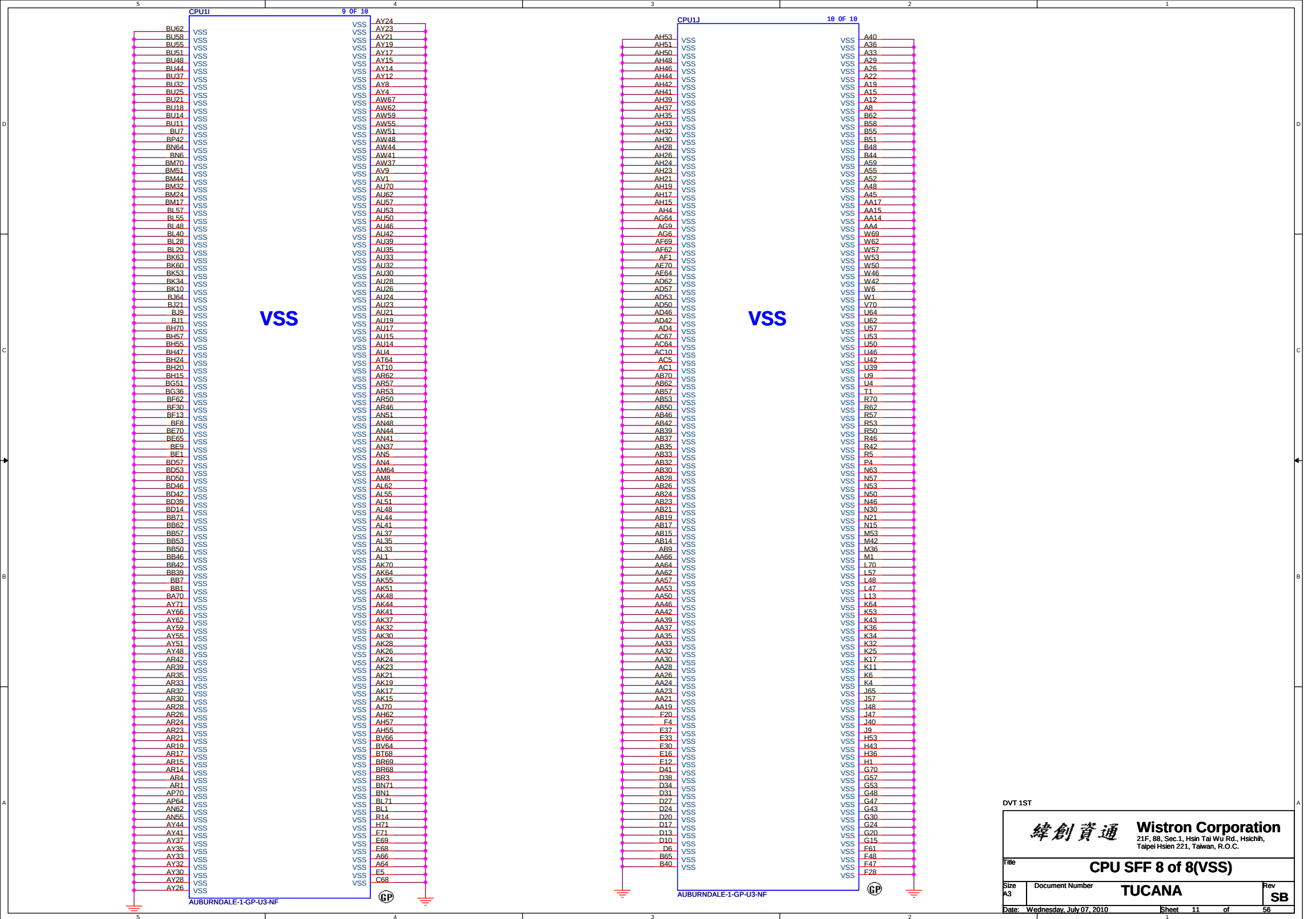
- VTTO
- AW14
- AW12
- AU60
- AU59
- AU12
- AR60
- AR59
- AR12
- AN60
- AN59
- AN35
- AN33
- AN17
- AN15
- AN14
- AN12
- AM10
- AL60
- AL59
- AL17
- AL15
- AL14
- AL12
- AK35
- AK33
- AF39
- AF37
- AF35
- AF33
- AF32
- AF30
- AD39
- BF60
- BF59
- BD60
- BD59
- BB60
- BB59
- AY60
- AW60
- AW35
- AW33
- AD37
- AD35
- AD33
- AD32
- AD30
- W35
- W33
- W32
- W30
- W28
- W26
- W24
- W23
- U35
- U33
- U32
- U30
- U28
- U26
- U24
- U23
- R35
- R33
- R32
- R30
- R28
- R26
- R24
- R23
- AY10
- AN9

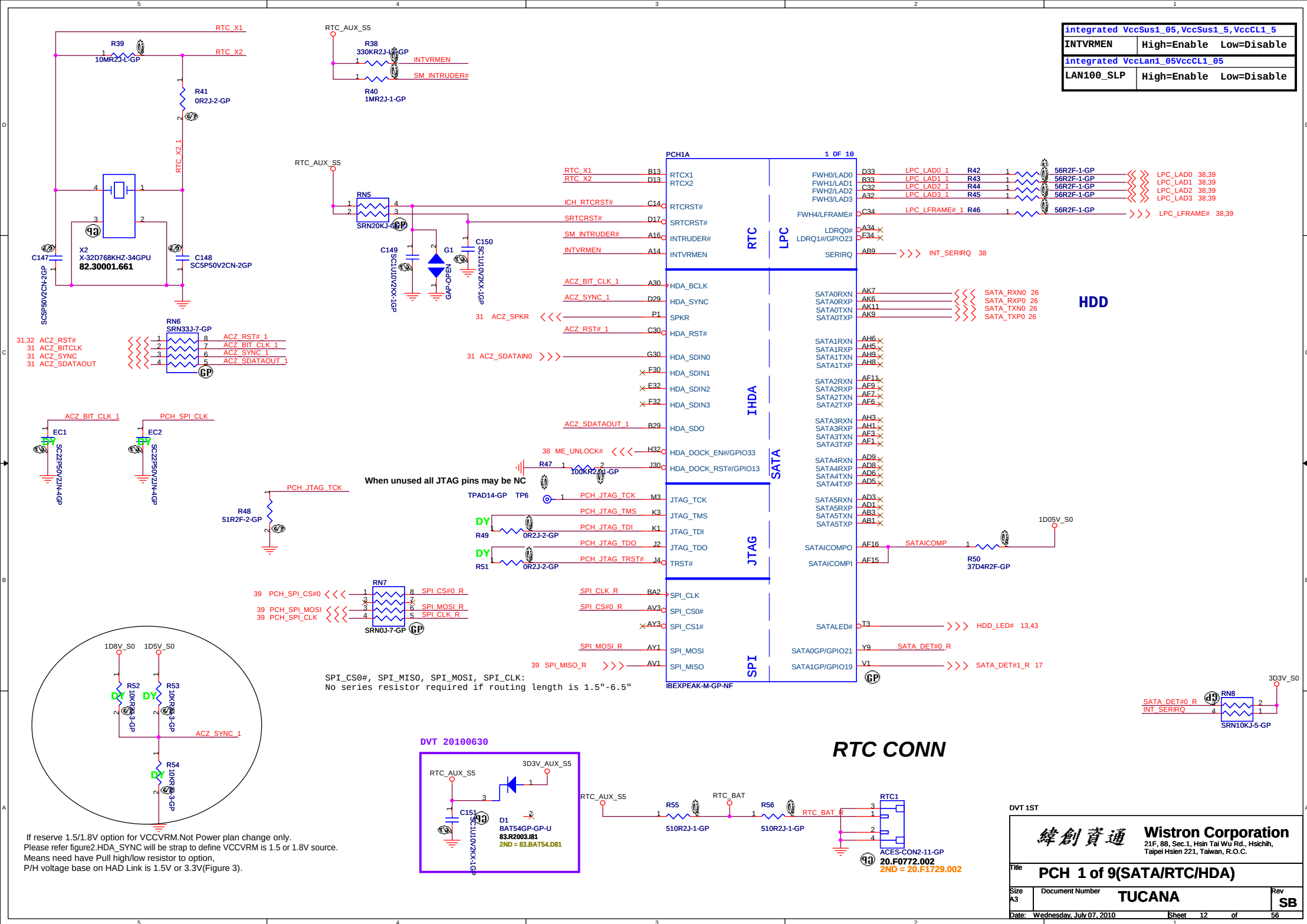


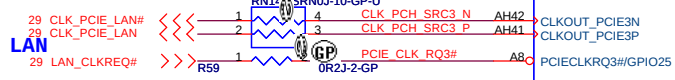
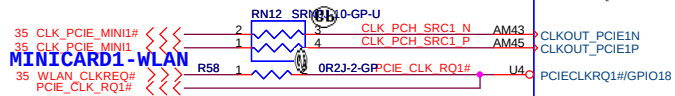
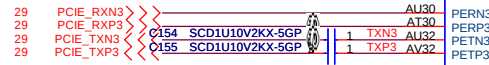
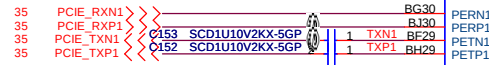
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		Title CPU SFF 4 of 8(Power/VTT)	
Size Custom	Document Number	TUCANA	
Date: Wednesday, July 07, 2010	Sheet 7	of	56

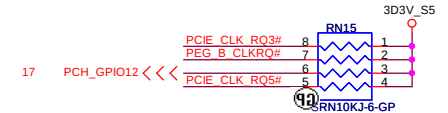
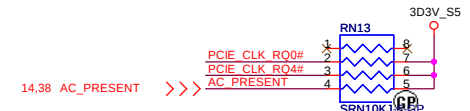
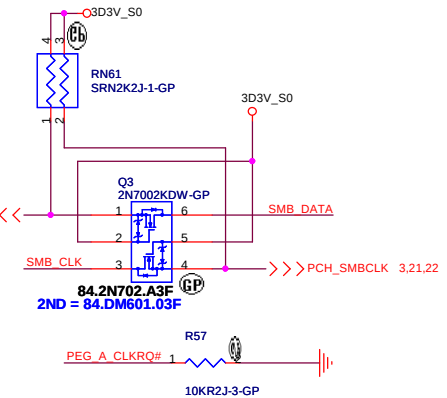
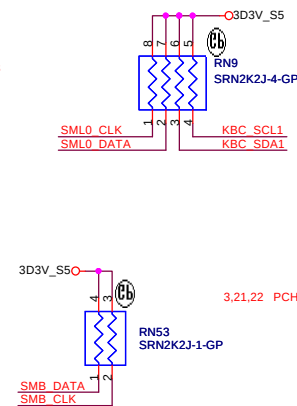
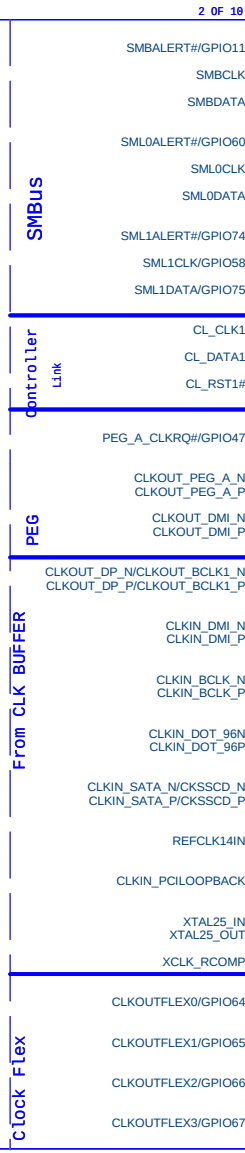
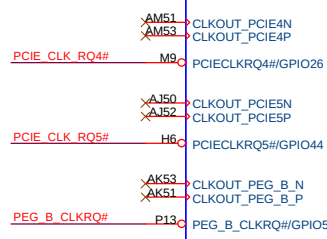




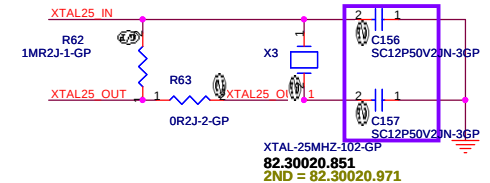




PCIECLKRQ{1,2} should have a 10K pull-up to +1.05VS (But CRB is pull-up to +3VS).



DVT 20100625
Change C156,C157 to 12pF
for Crystal vendor Test



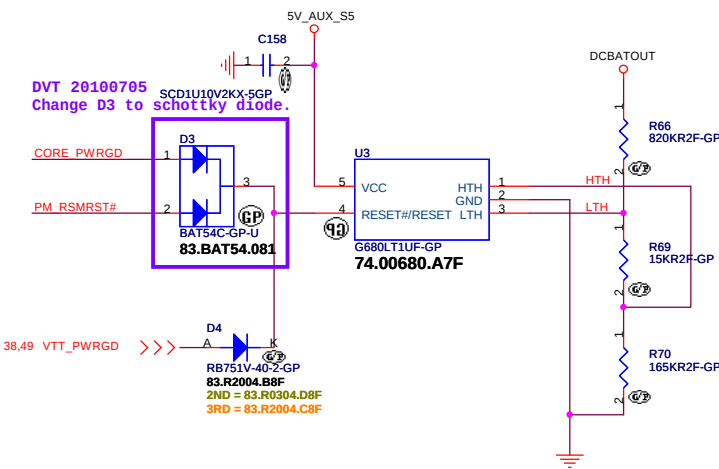
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Taipei Hsien 221, Taiwan, R.O.C.

Size A3	Document Number TUCANA	Rev SP
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Date: Wednesday, July 07, 2010 Sheet 13 of 56

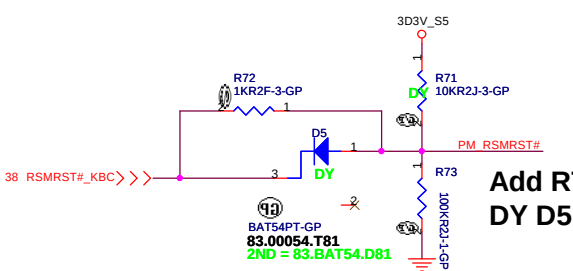


Delete PM_PWRBTN# pull high

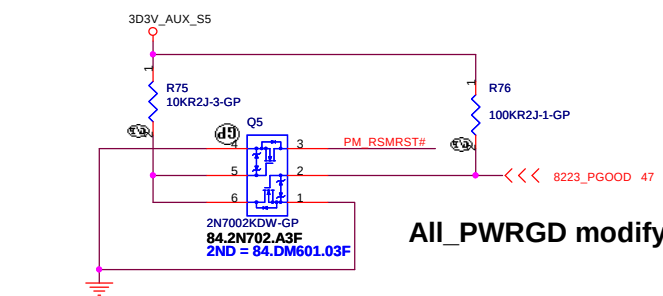


$$V_L = 1.245 \cdot \left(\frac{R1+R2+R3}{R2+R3} \right)$$

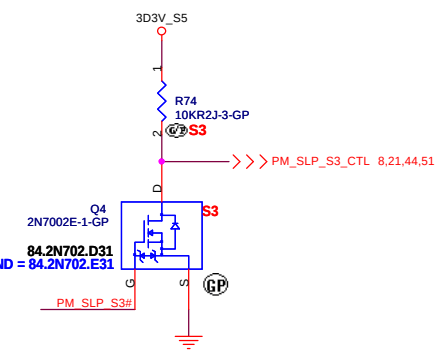
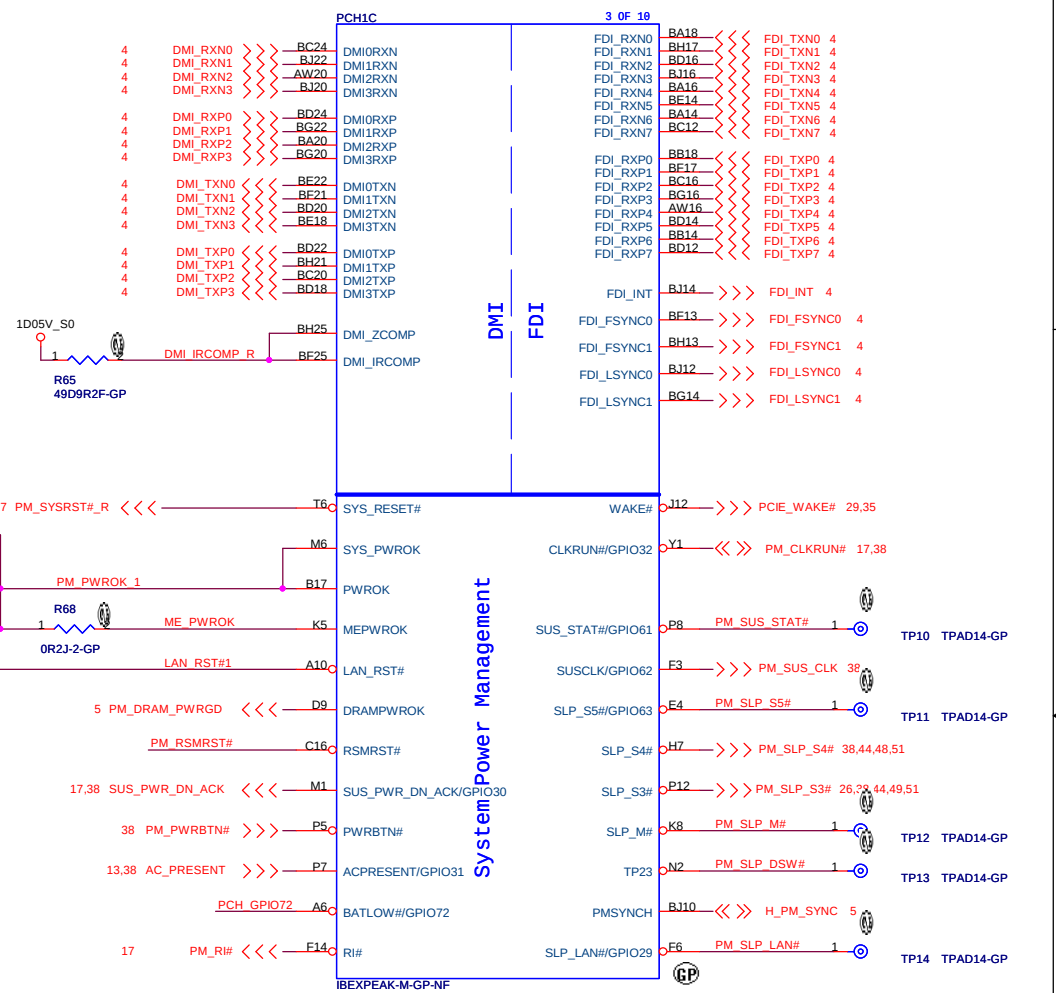
$$V_h = 1.245 \cdot \left(\frac{R1+R2+R3}{R3} \right)$$



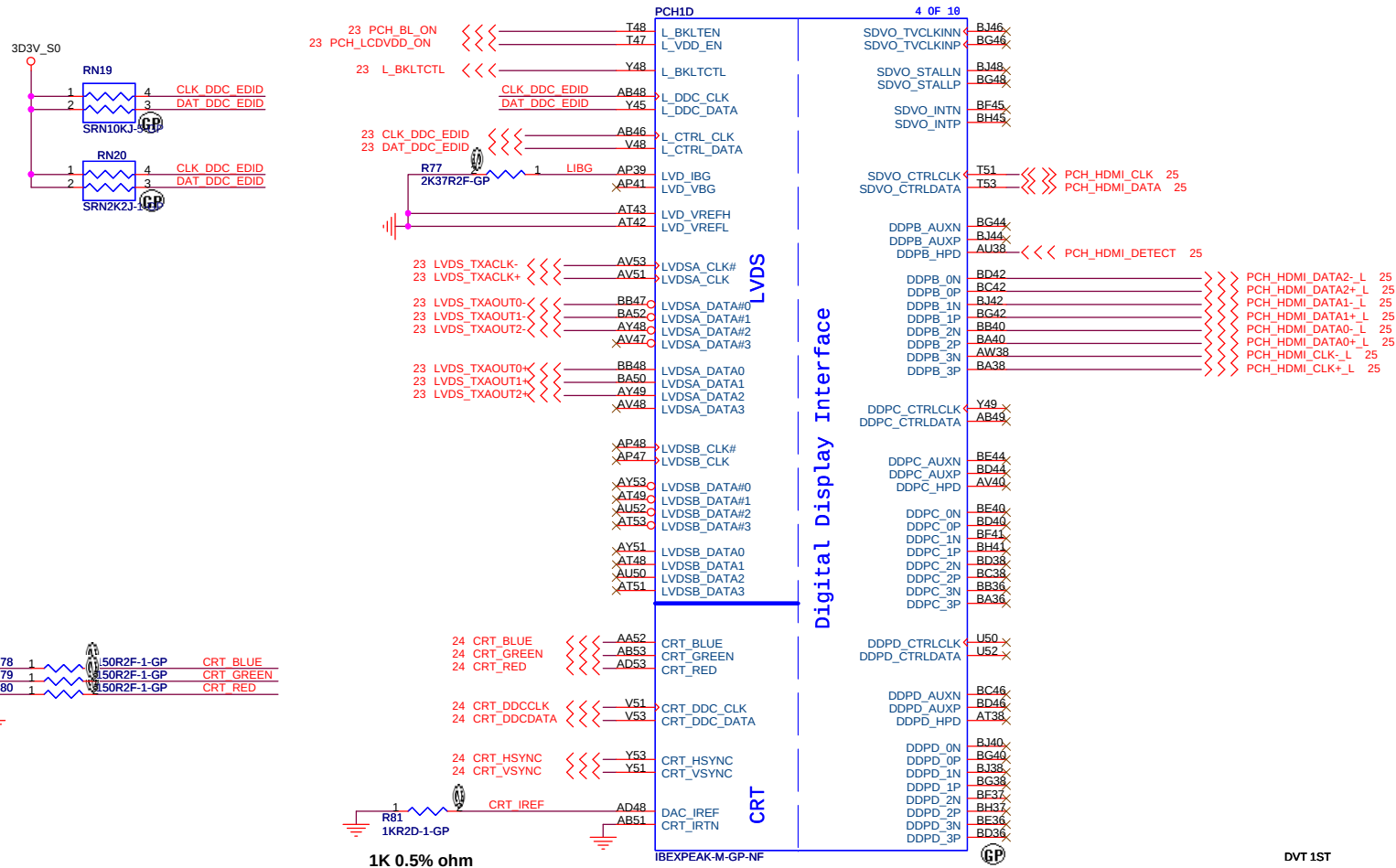
Add RTC Data lose function
DY D5



All_PWRGD modify 51123_PGOOD from 3V/5V power



Panel backlight enable control for LVDS -
used to gate power into the backlight circuit



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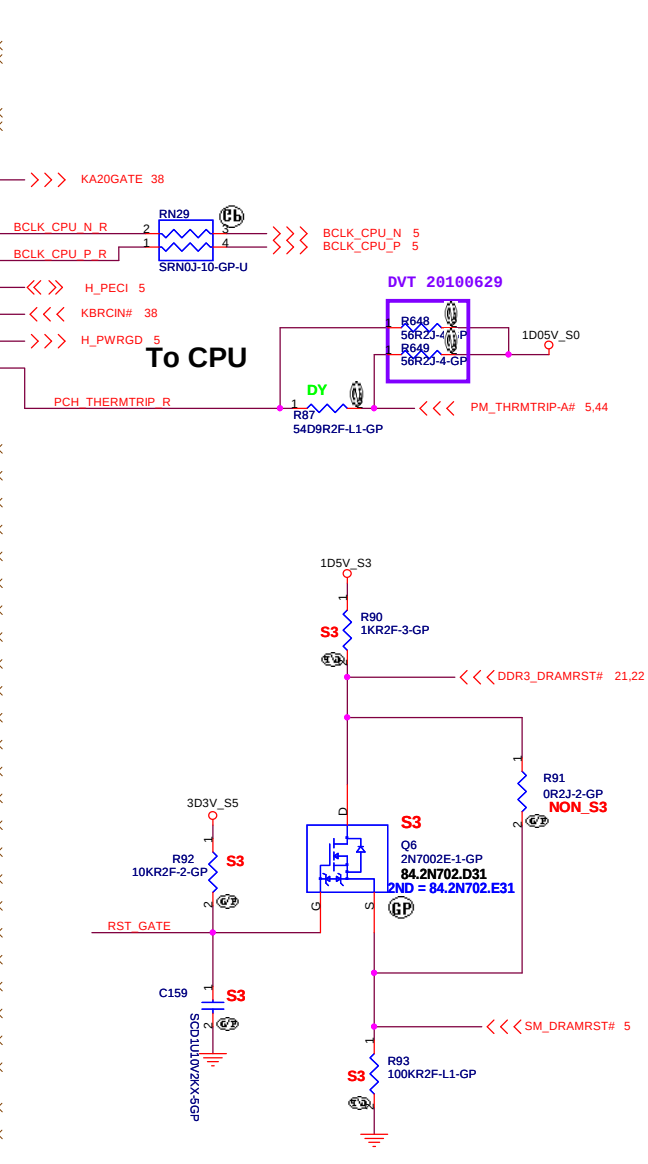
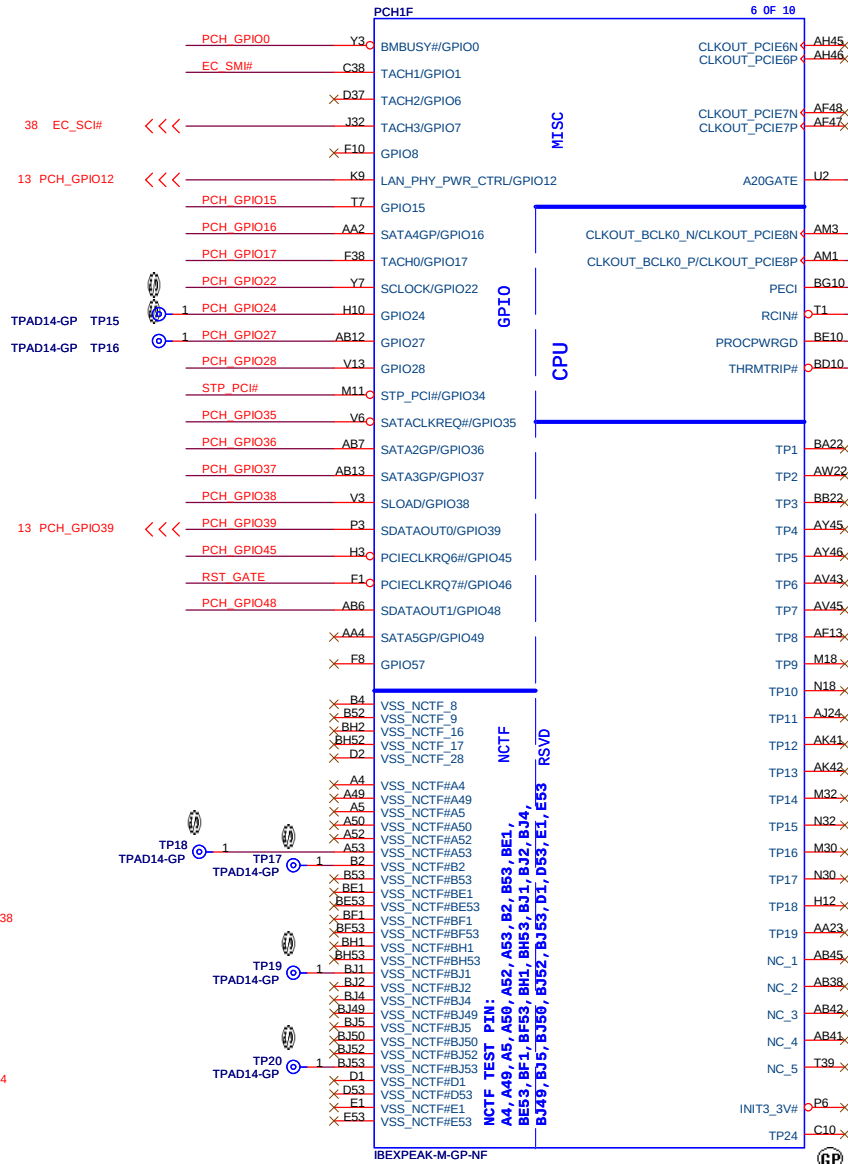
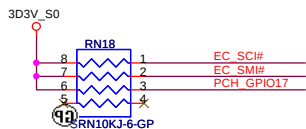
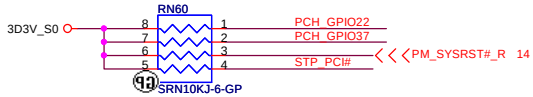
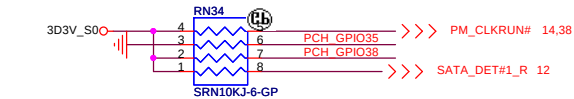
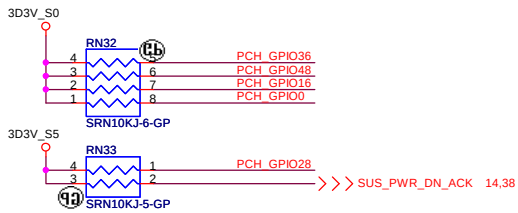
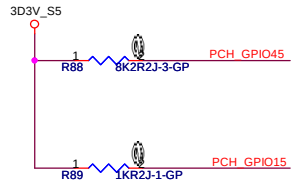
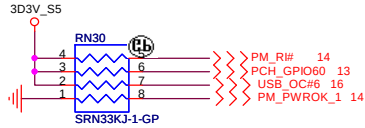
Title			PCH 4 of 9(LVDS/CRT/DP)		
Size	Document Number	TUCANA			Rev
Custom					SB
Date:	Wednesday, July 07, 2010	Sheet	15	of	56

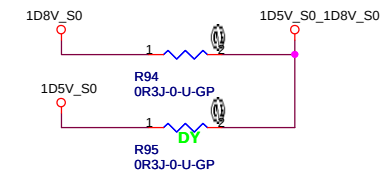
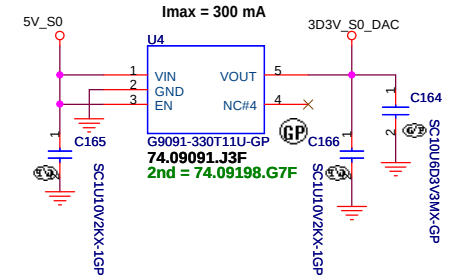
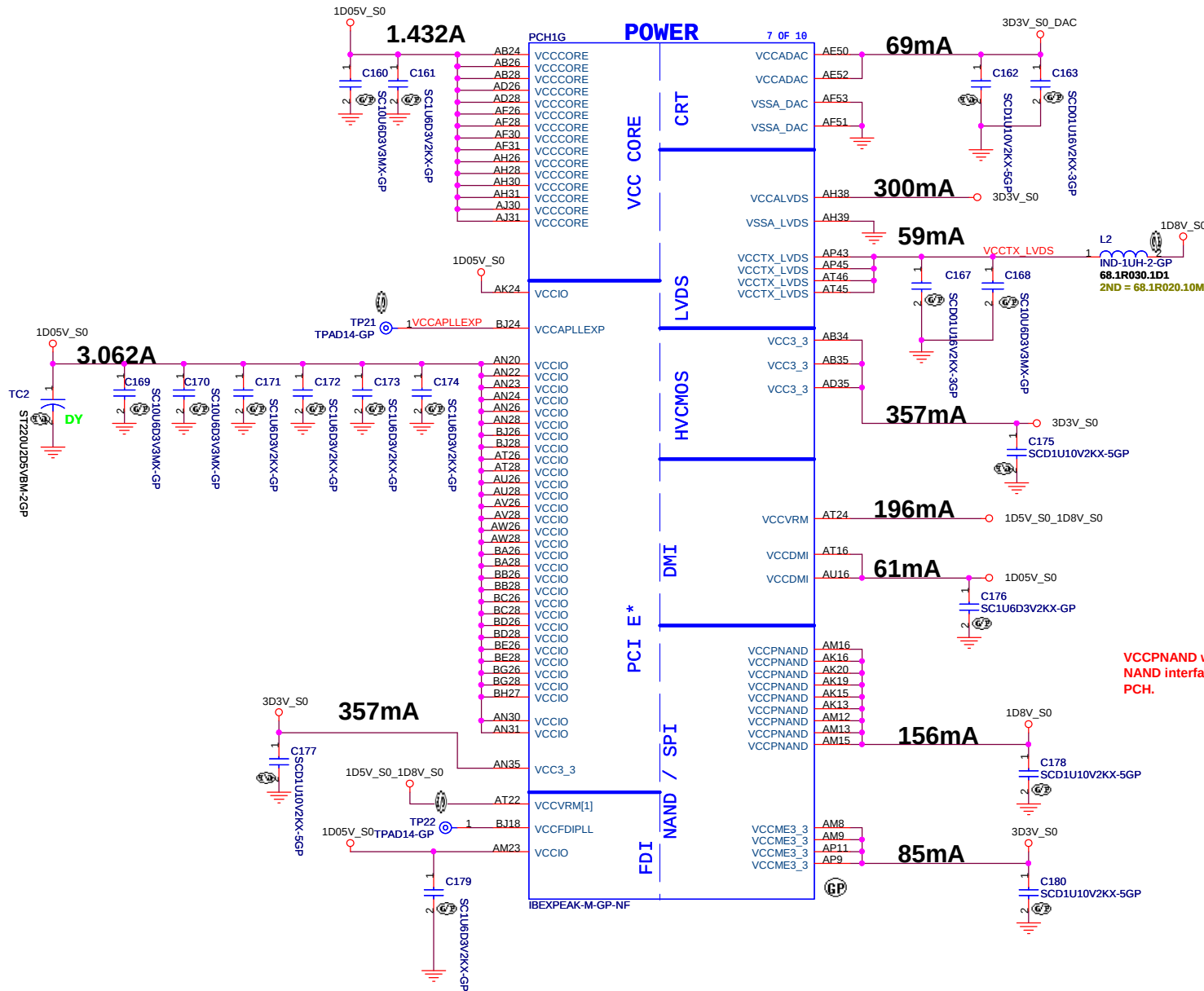
GPIO8 has a weak[20K] internal pull up.
No need to have external pull down/up.
GPIO8 pin set to high at reset.

GPIO15 has a weak[20K] internal pull down.
No need to have external pull up/down.
GPIO 15 pin is set to low at reset.

Low : ME Crypto TLS with no confidentiality
High : ME Crypto TLS with confidentiality

GPIO27 has a weak[20K] internal pull up.
To enable on-die PLL Voltage regulator,
should not place external pull down.



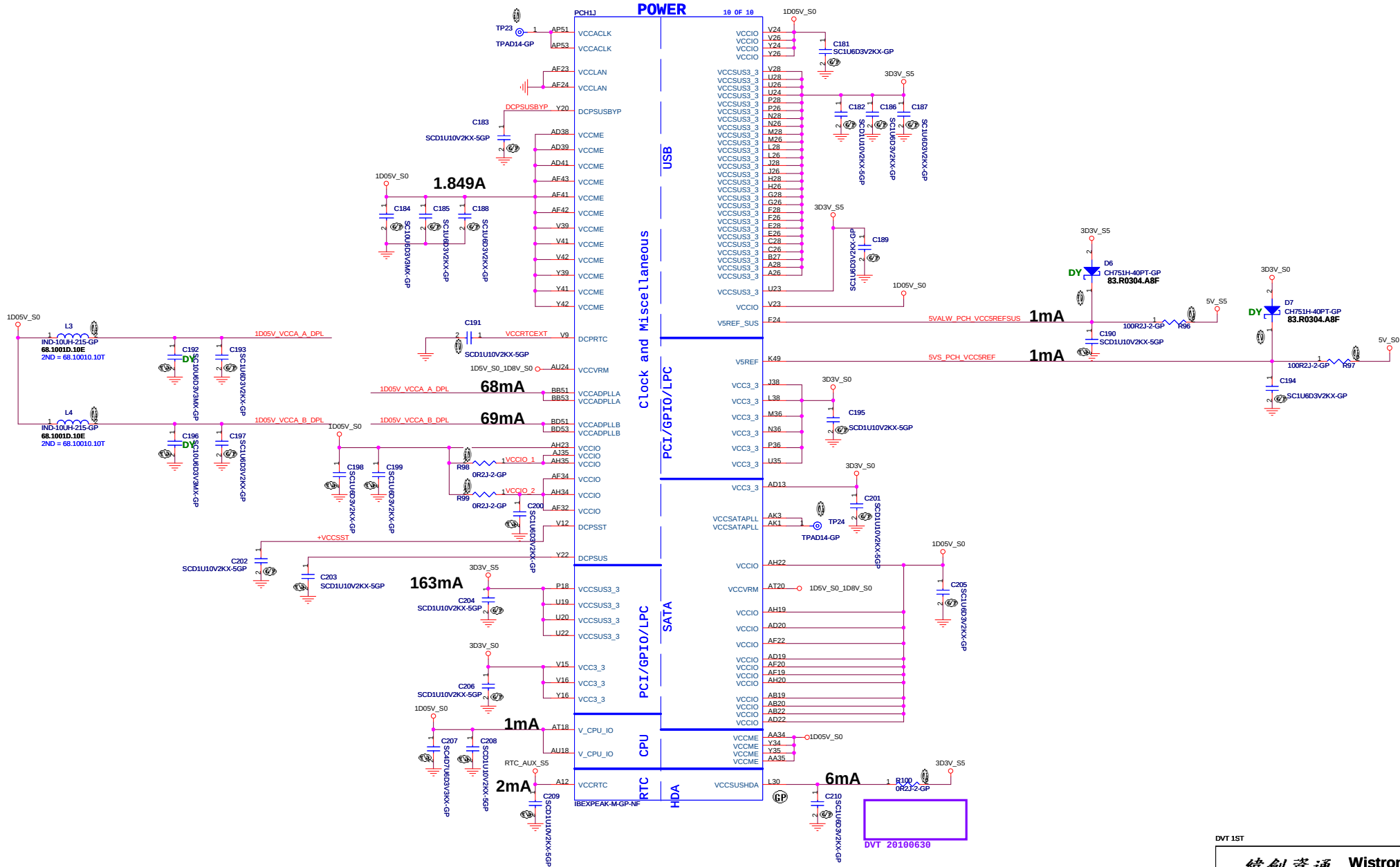


VCCPNAND which power the DC NAND interface must be powered even if dual channel NAND interface is not connected since it also supplies power to other functions inside PCH.

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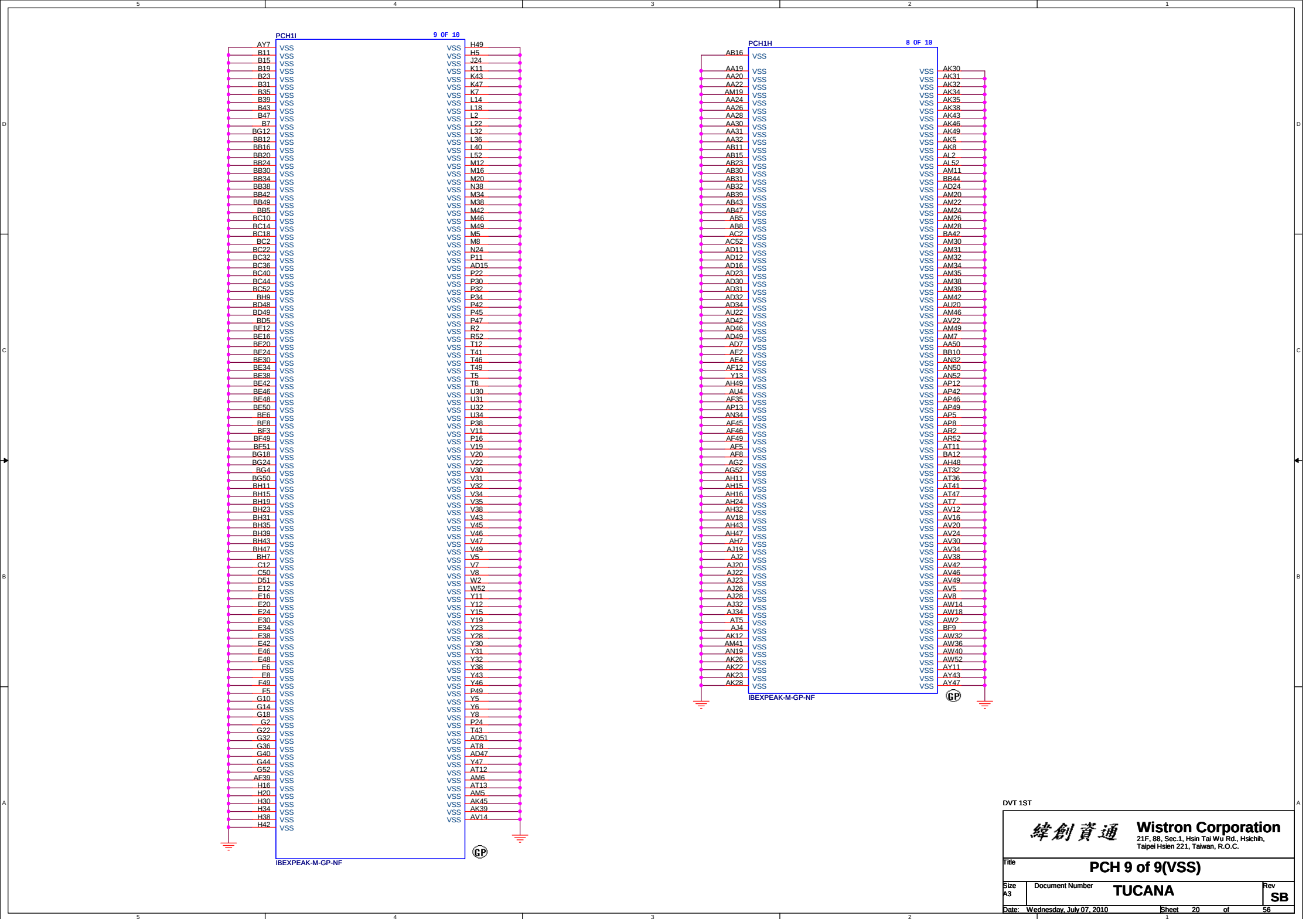
Title		
PCH 7 of 9(PWR/VCORE/LVDS)		
Size	Document Number	Rev
Custom	TUCANA	SB
Date:	Wednesday, July 07, 2010	Sheet 18 of 56



DVT 1ST

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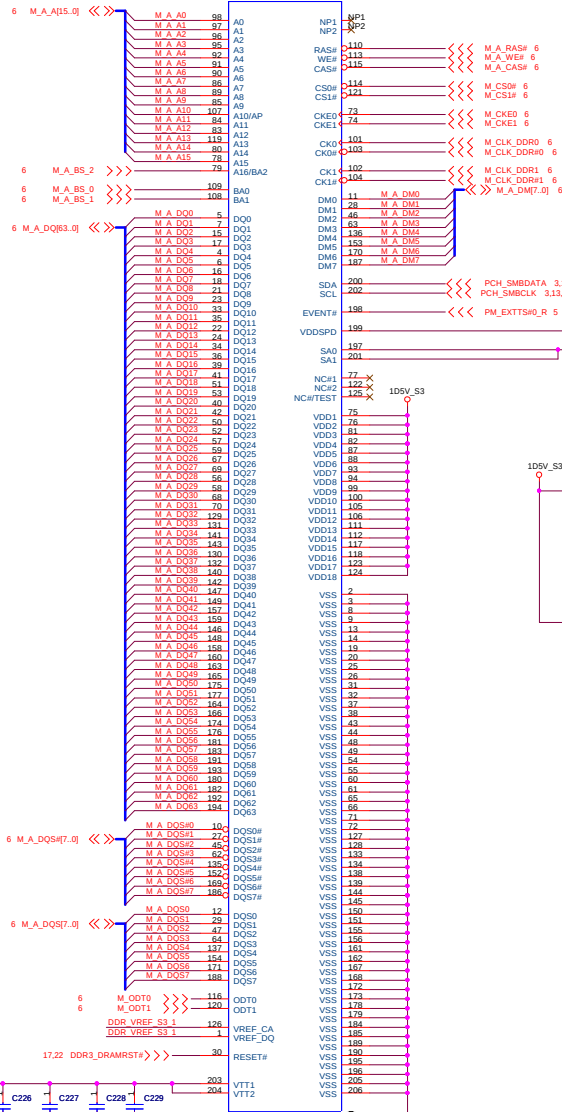
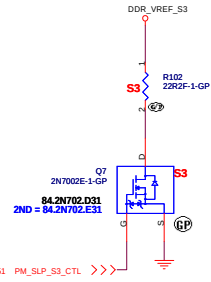
Title			
PCH 8 of 9(PWR\ SATA\ USB)			
Size Custom	Document Number		Rev
	TUCANA		SI
Date: Wednesday, July 07, 2010		Sheet 19 of	56



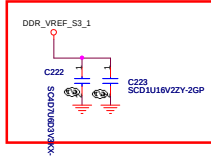
DVT 1ST

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Title PCH 9 of 9(VSS)			
Size A3	Document Number TUCANA	Rev SB	
Date: Wednesday, July 07, 2010		Sheet 20	of 56

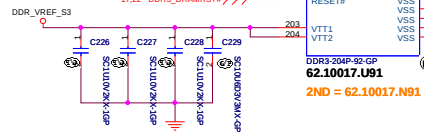
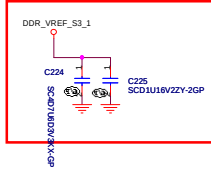
DDR3 SOCKET_1



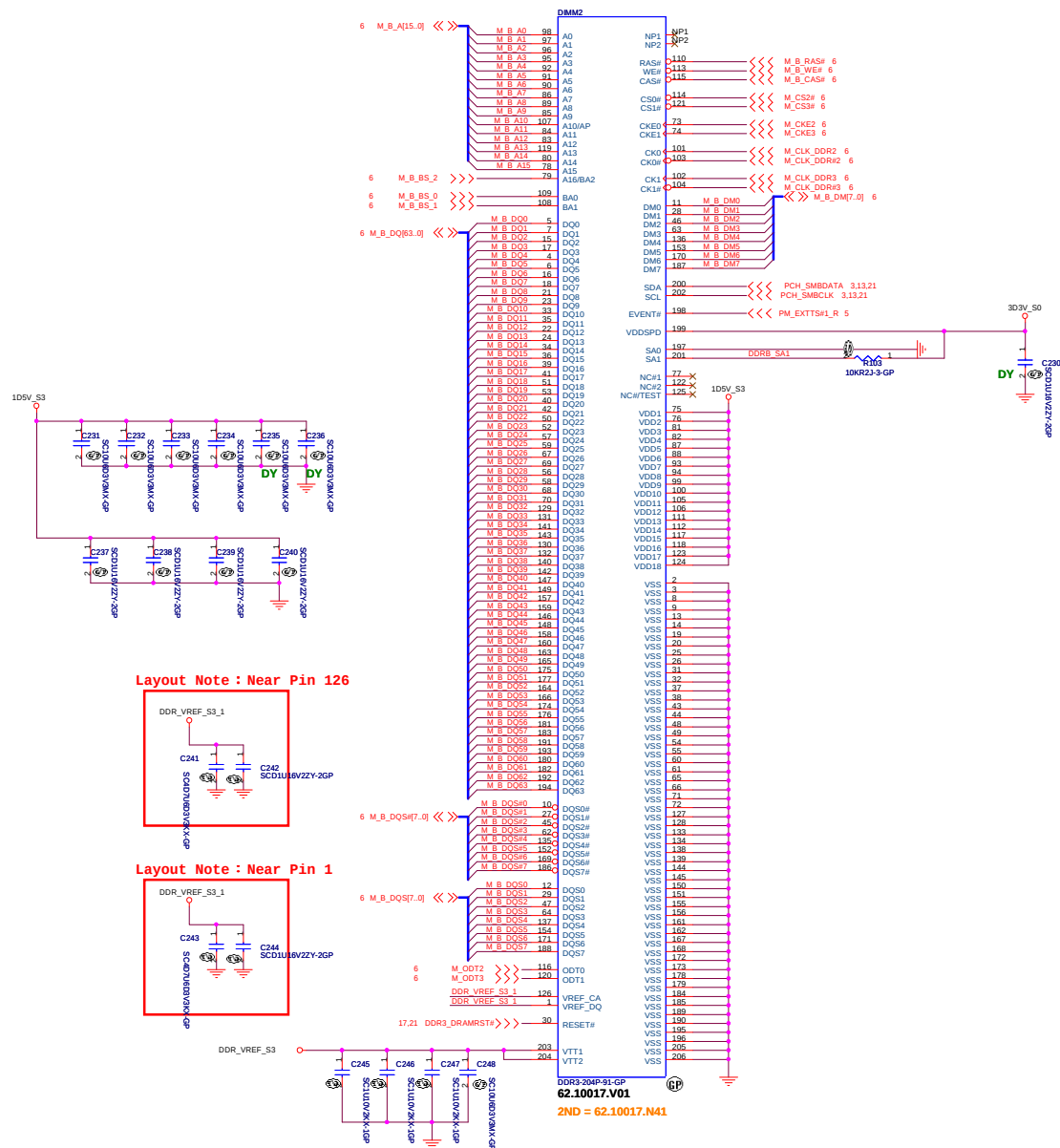
Layout Note : Near Pin 126



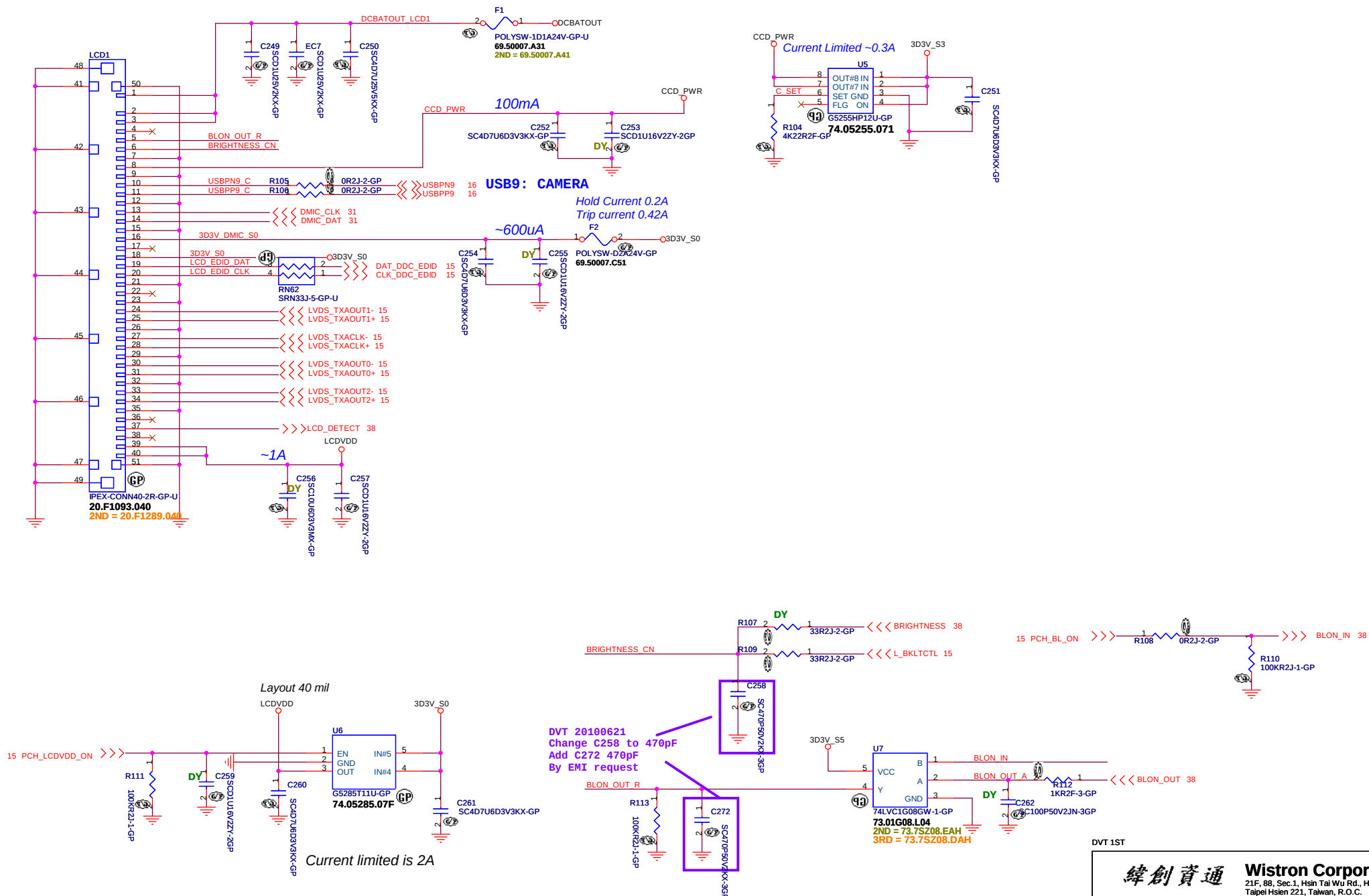
Layout Note : Near Pin 1



DDR3 SOCKET_2



LCD/CCD CONN



DVT 1ST

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Taipei Hsien 221, Taiwan, R.O.C.

Title

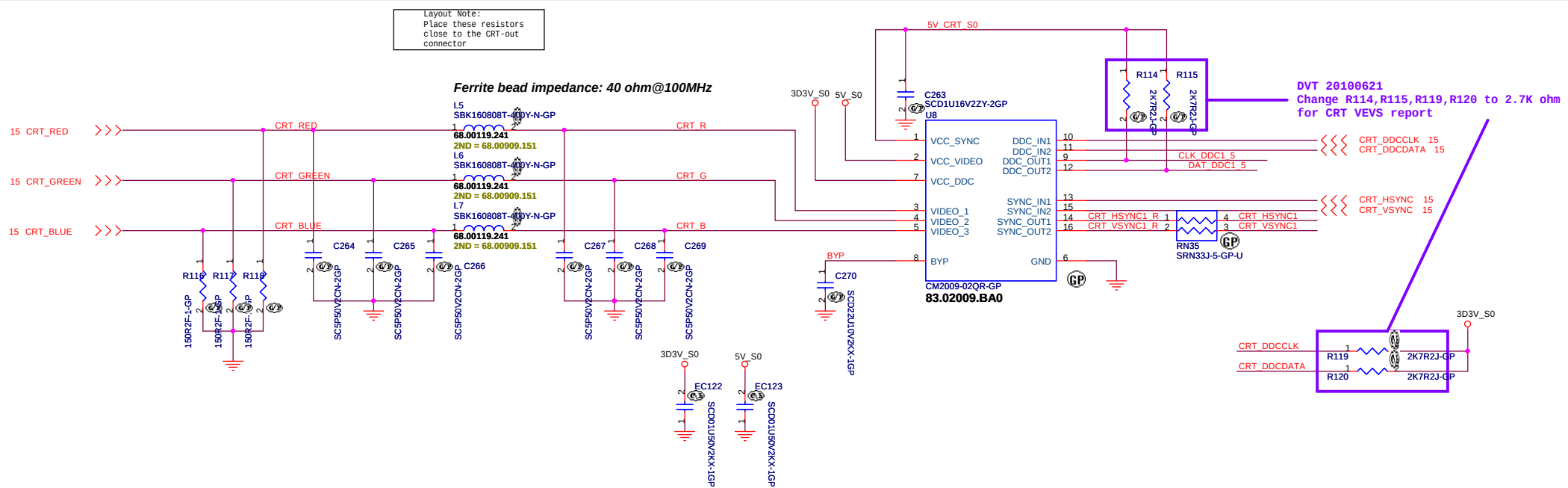
LCD CONN

Size	Document Number
------	-----------------

TUCANA

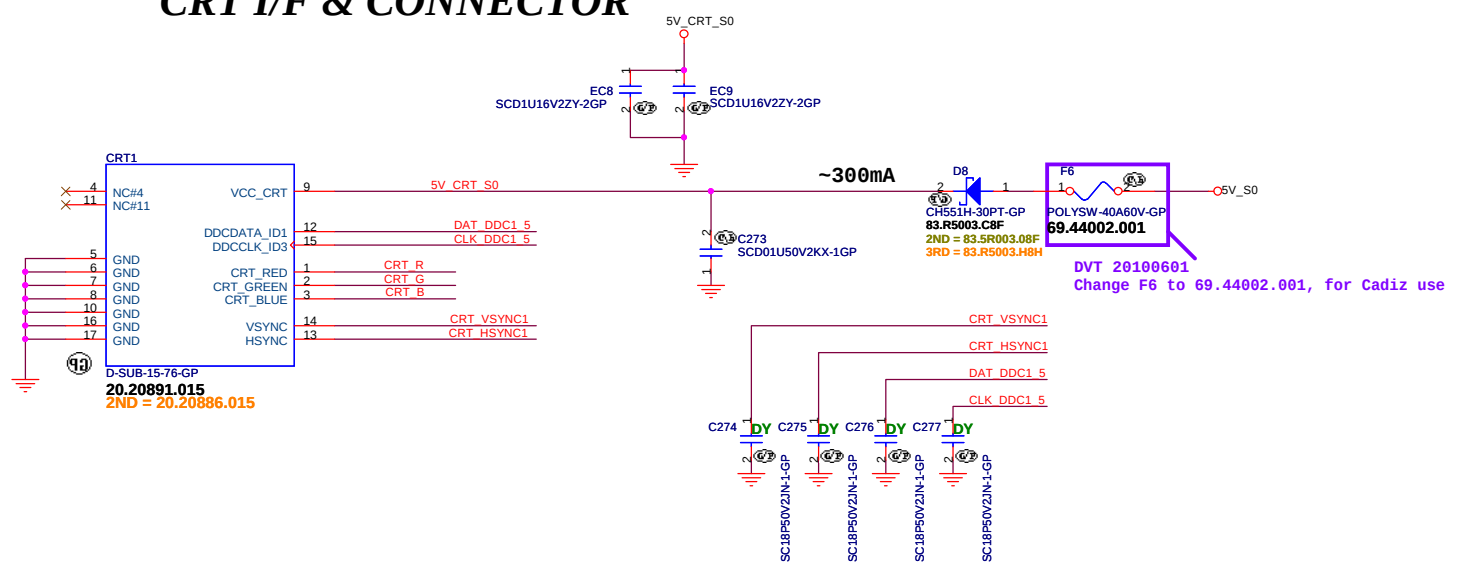
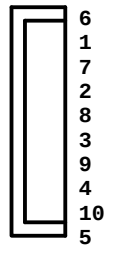
Date: Wednesday, July 07, 2010

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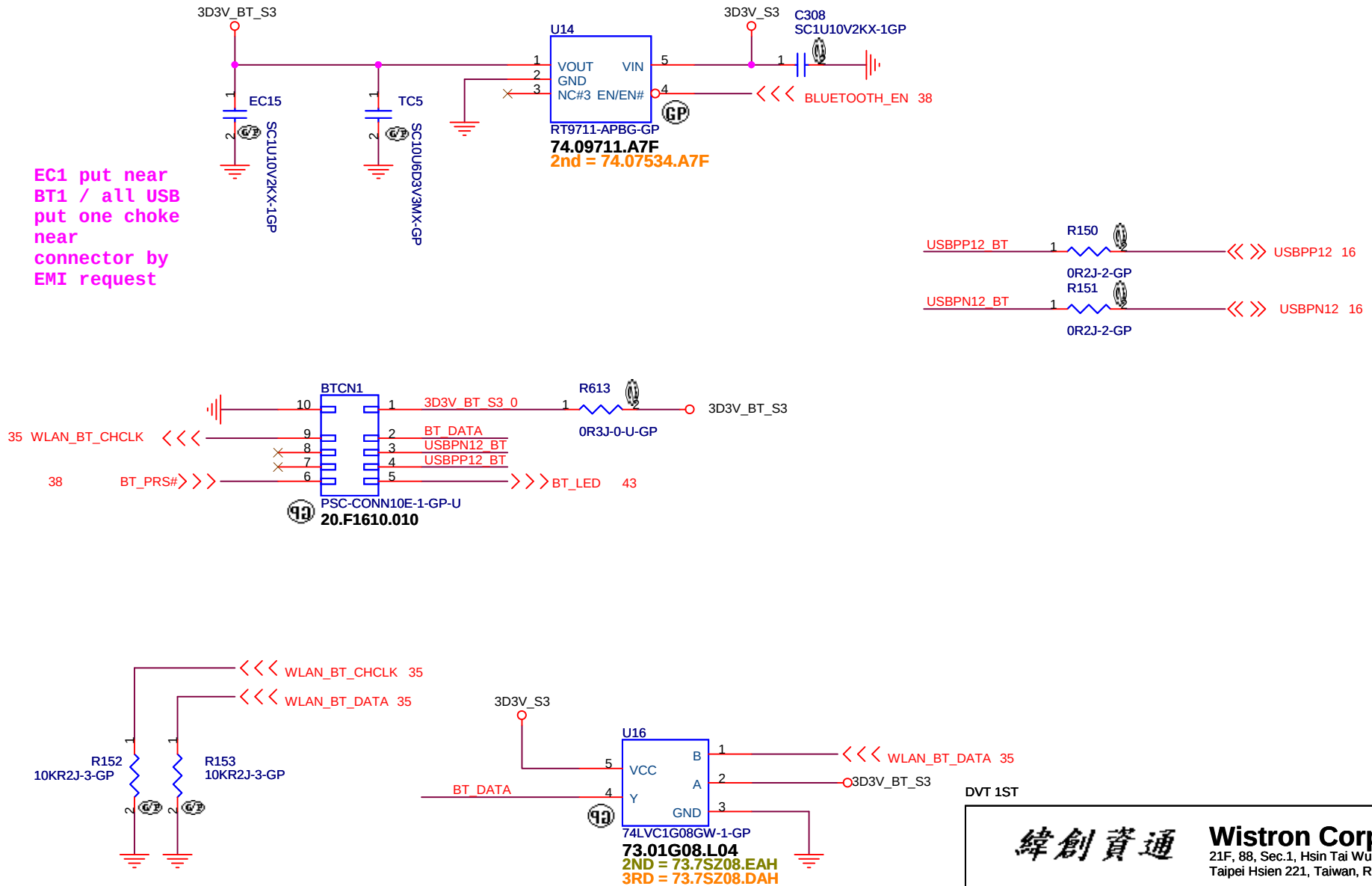
Layout Note:
 * Must be a ground return path between this ground and the ground on the VGA connector.
 Pi-filter & 150 Ohm pull-down resistors should be as close as to CRT CONN. RGB will hit 75 Ohm first, pi-filter, then CRT CONN.

CRT I/F & CONNECTOR



Bluetooth

EC1 put near
BT1 / all USB
put one choke
near
connector by
EMI request



DVT 1ST

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

Bluetooth

Size

Document Number

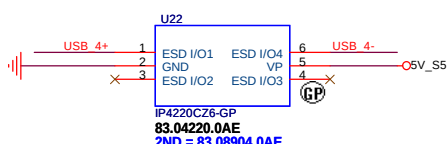
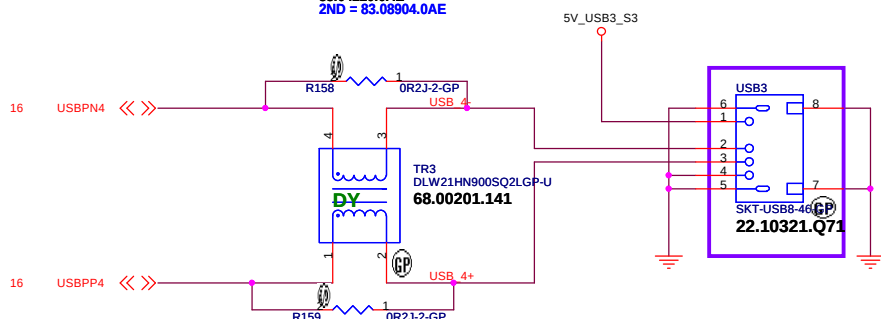
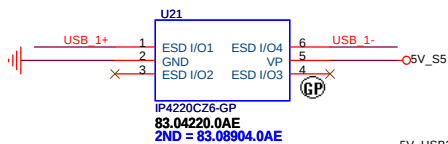
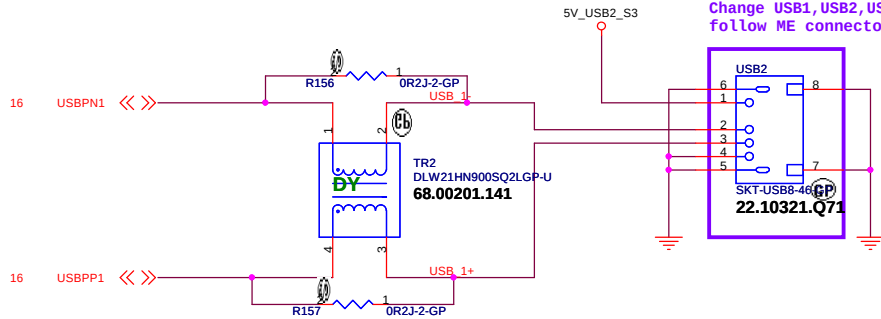
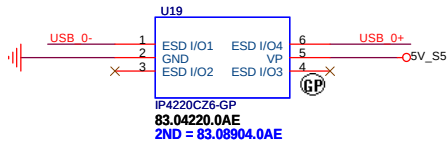
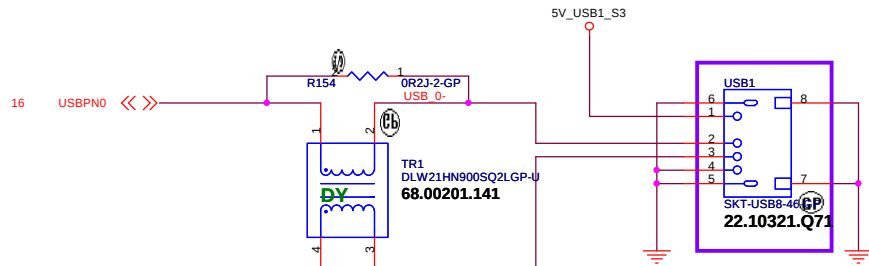
TUCANA

Rev

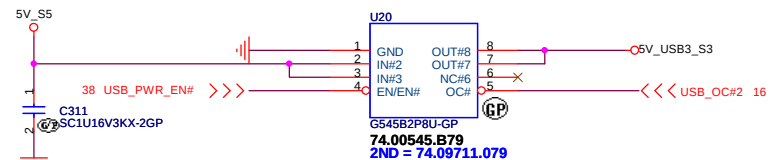
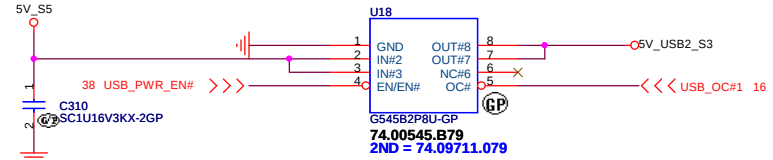
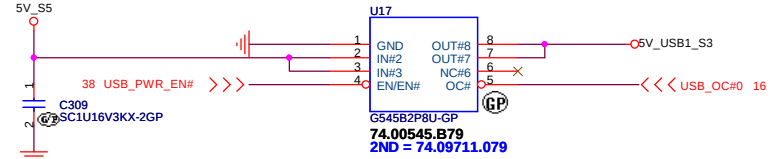
SB

Date: Wednesday, July 07, 2010

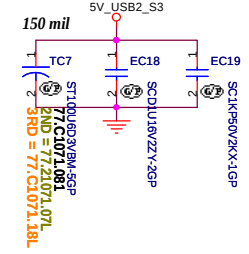
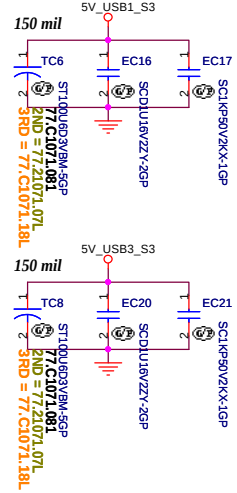
Sheet 27 of 56

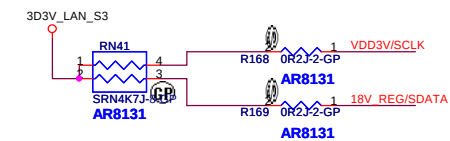
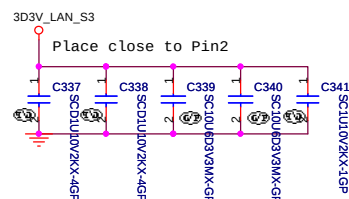
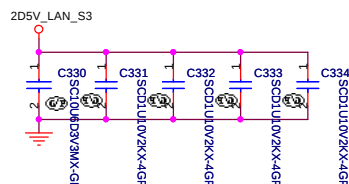
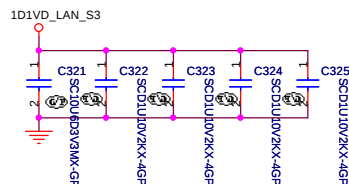
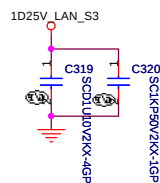
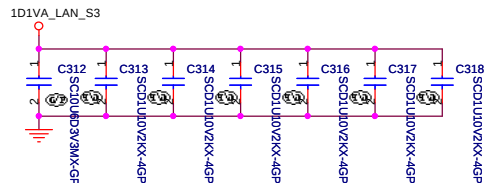


DVT 20100604
Change USB1,USB2,USB3 to 22.10321.Q71
follow ME connector list.

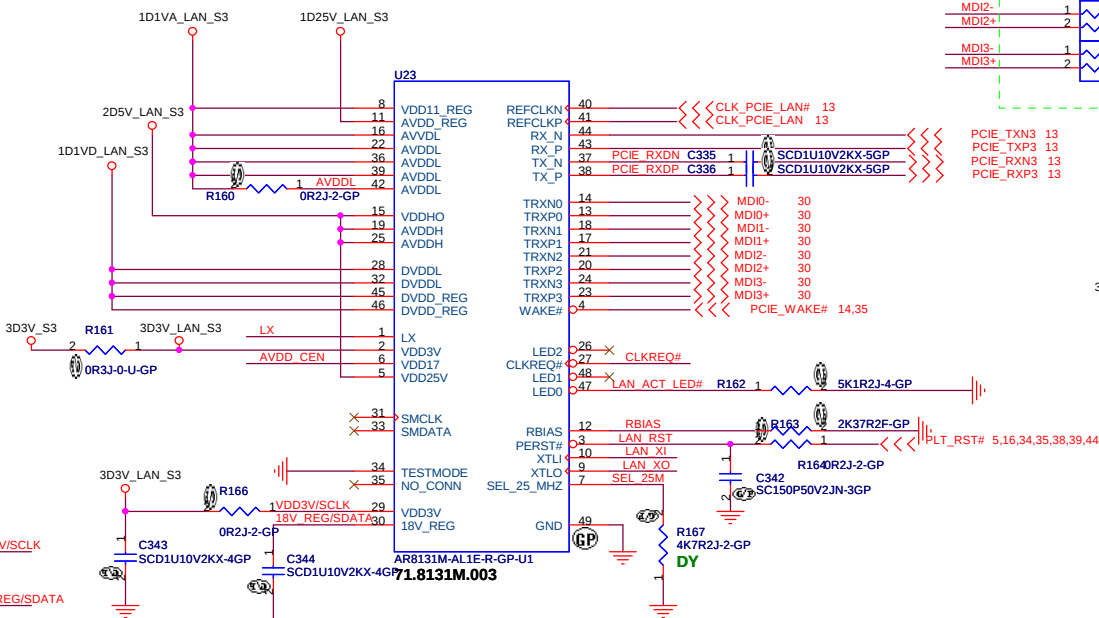
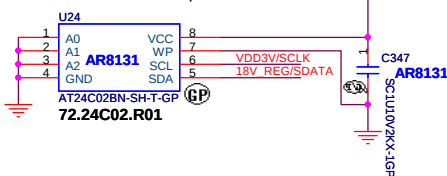


U17,U18,U20 Current Limit 1.5A

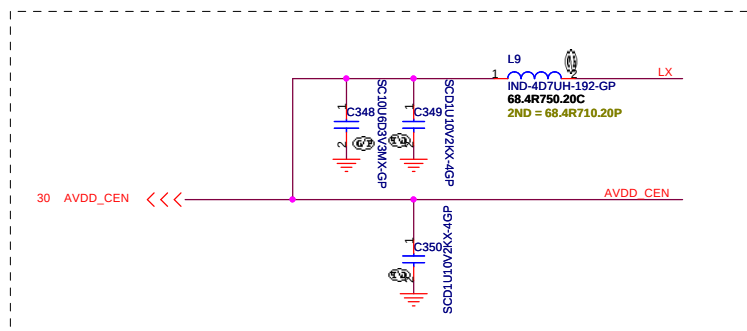




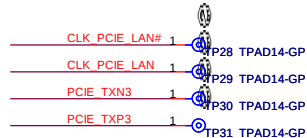
for AR8131 chip



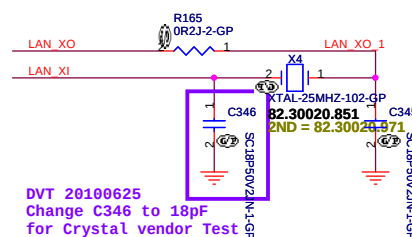
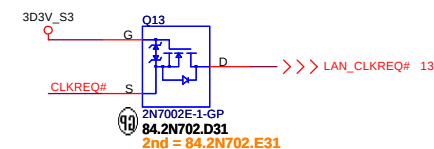
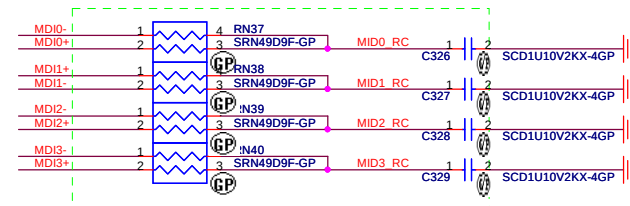
For AR8131: RN41,R168,R169,U24,C347 are need to stuff.
For AR8131M: RN41,R168,R169,U24,C347 are DY



Close to U3



Close to LAN_AR8131



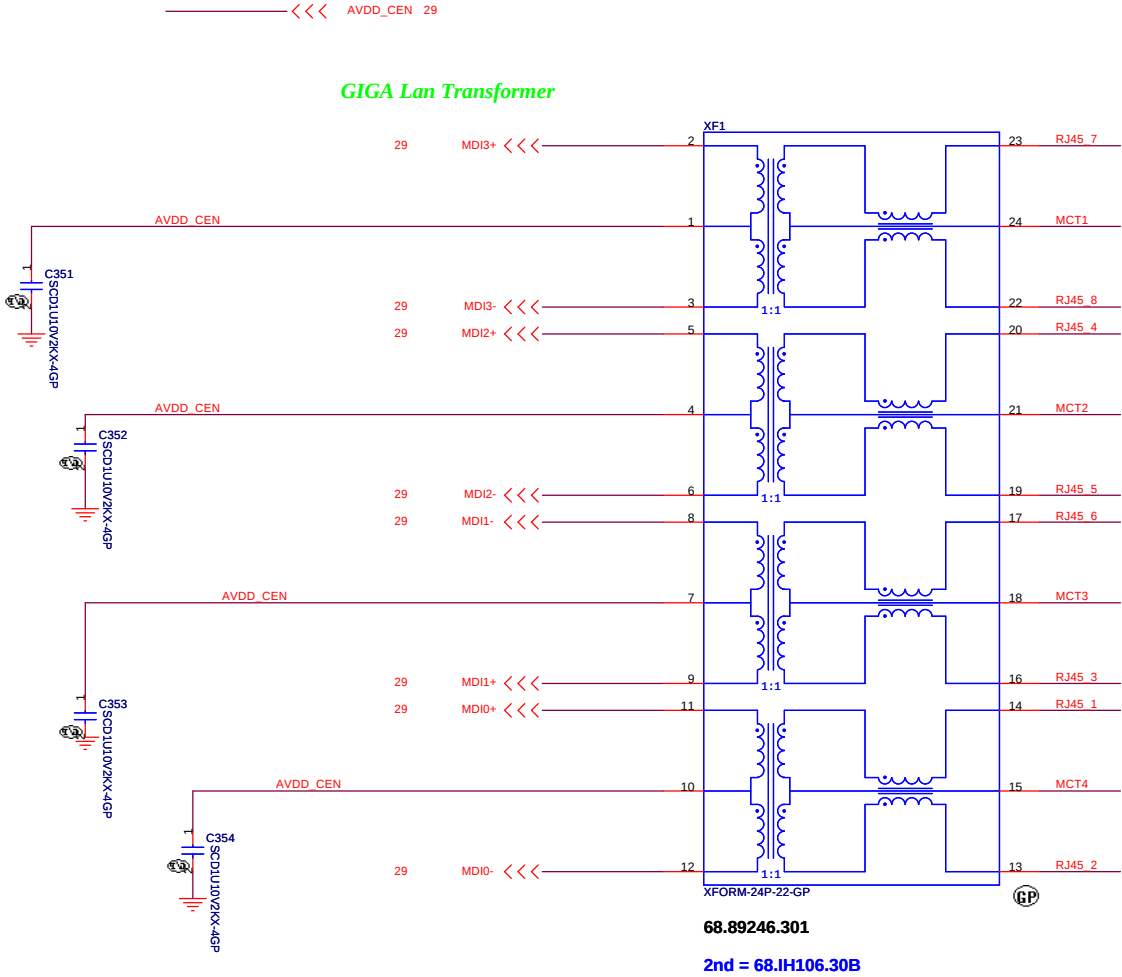
DVT 20100625
Change C346 to 18pF
for Crystal vendor Test

DVT 1ST

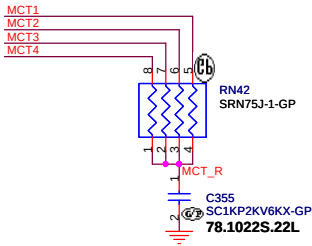
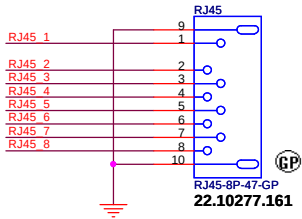
- 1.route on bottom as differential pairs.
2.Tx+/Tx- are pairs. Rx+/Rx- are pairs.
3.No vias, No 90 degree bends.
4.pairs must be equal lengths.
5.6mil trace width,12mil separation.
6.36mil between pairs and any other trace.
7.Must not cross ground moat,except RJ-45 moat.

LAN Transformer

GIGA Lan Transformer

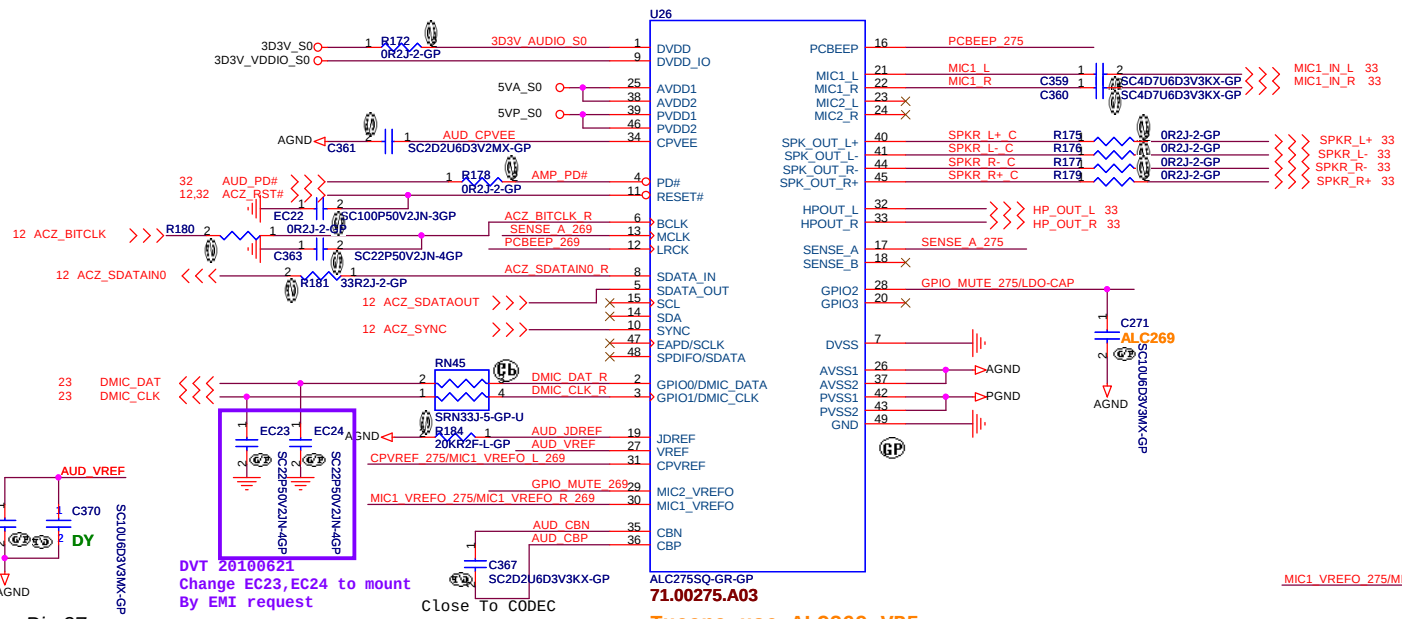
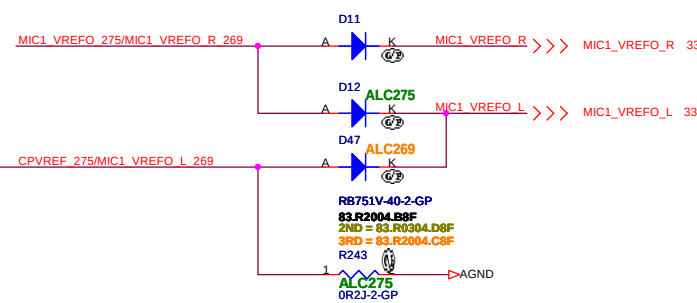
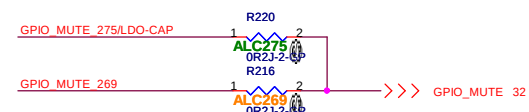
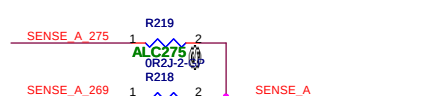
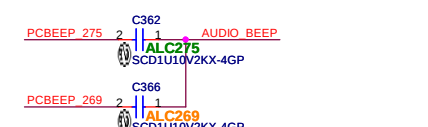
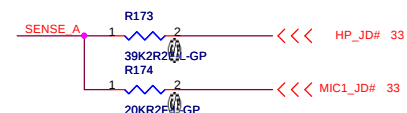
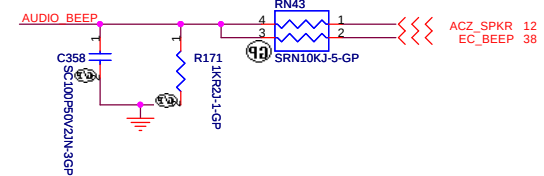
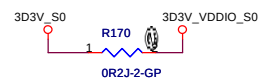


LAN Connector



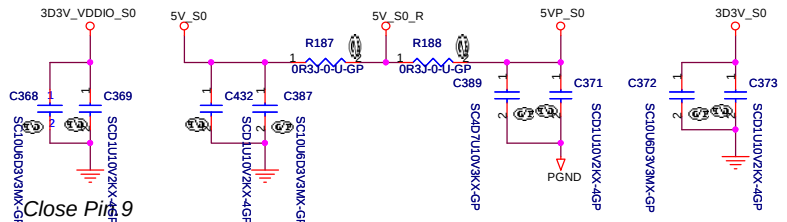
DVT 1ST

緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
LAN CONN			
Size	Document Number		Rev
TUCANA			SB
Date:	Wednesday, July 07, 2010	Sheet 30 of	56

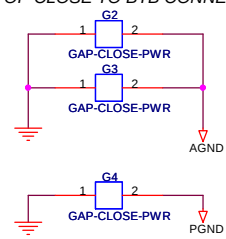


ALC275SQ-GR-GP
71.00275.A03

Tucana use ALC269-VB5
71.00269.E03

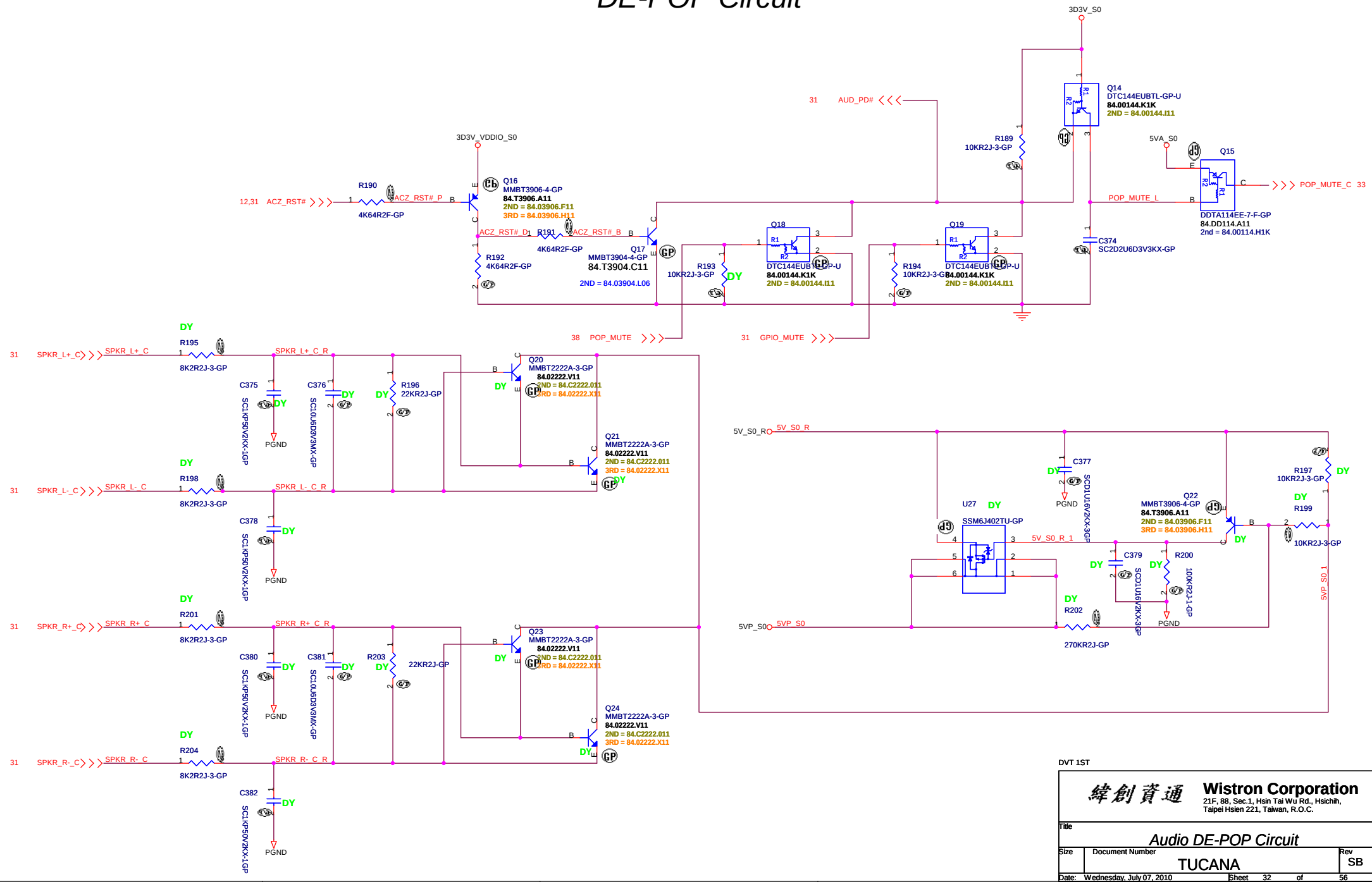


Close Pin.39 and Pin.46

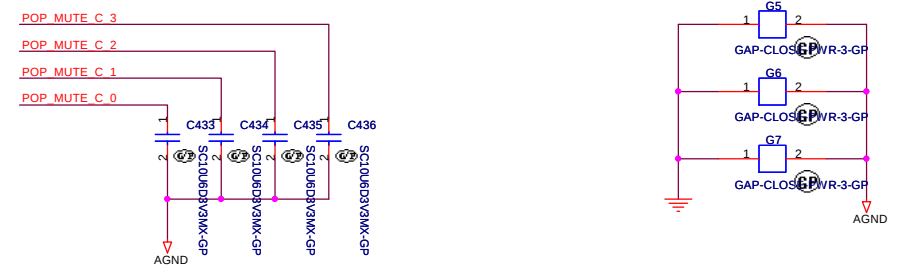
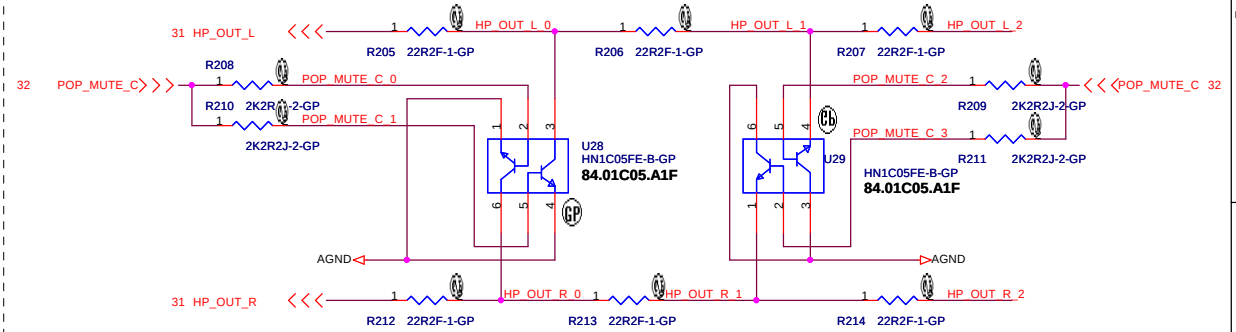
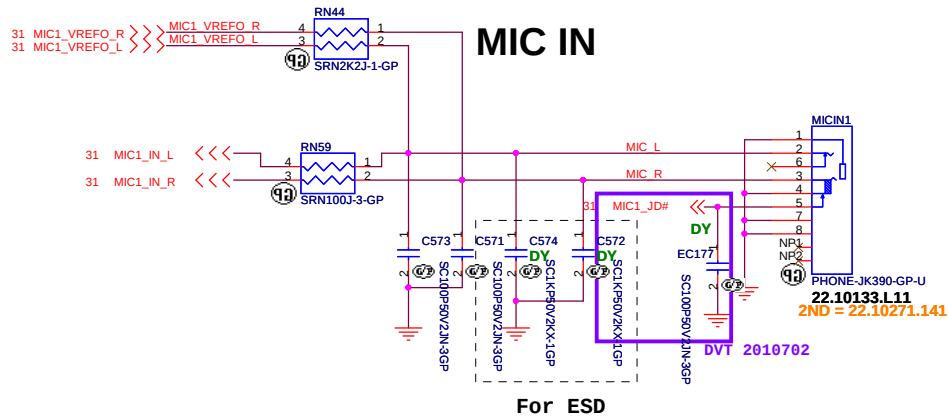
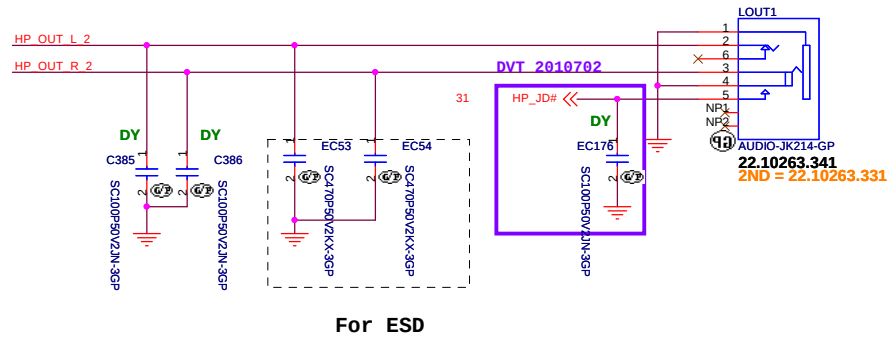


Close Pin.1

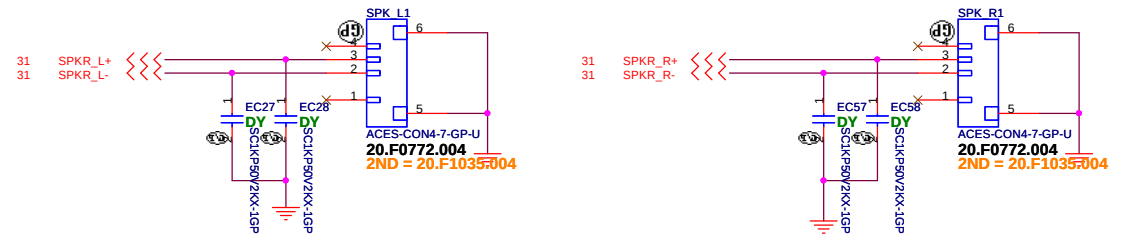
DE-POP Circuit



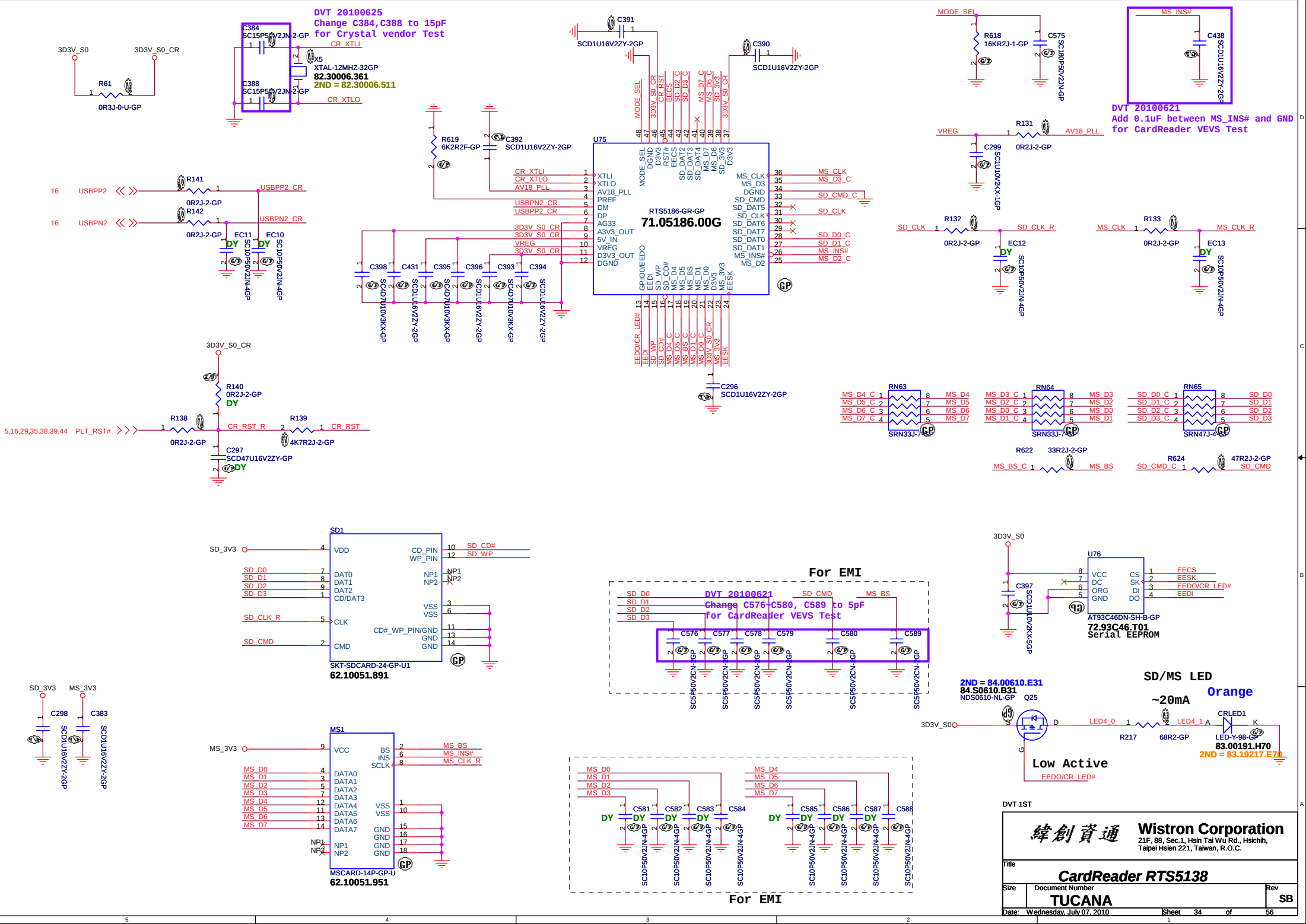
LINE OUT



Internal Speaker CONN



DVT 1ST

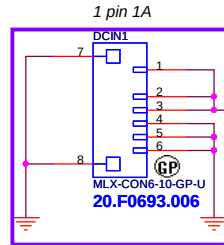


1

Place near MINI1

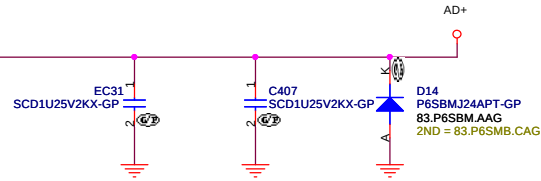


DC IN Connector



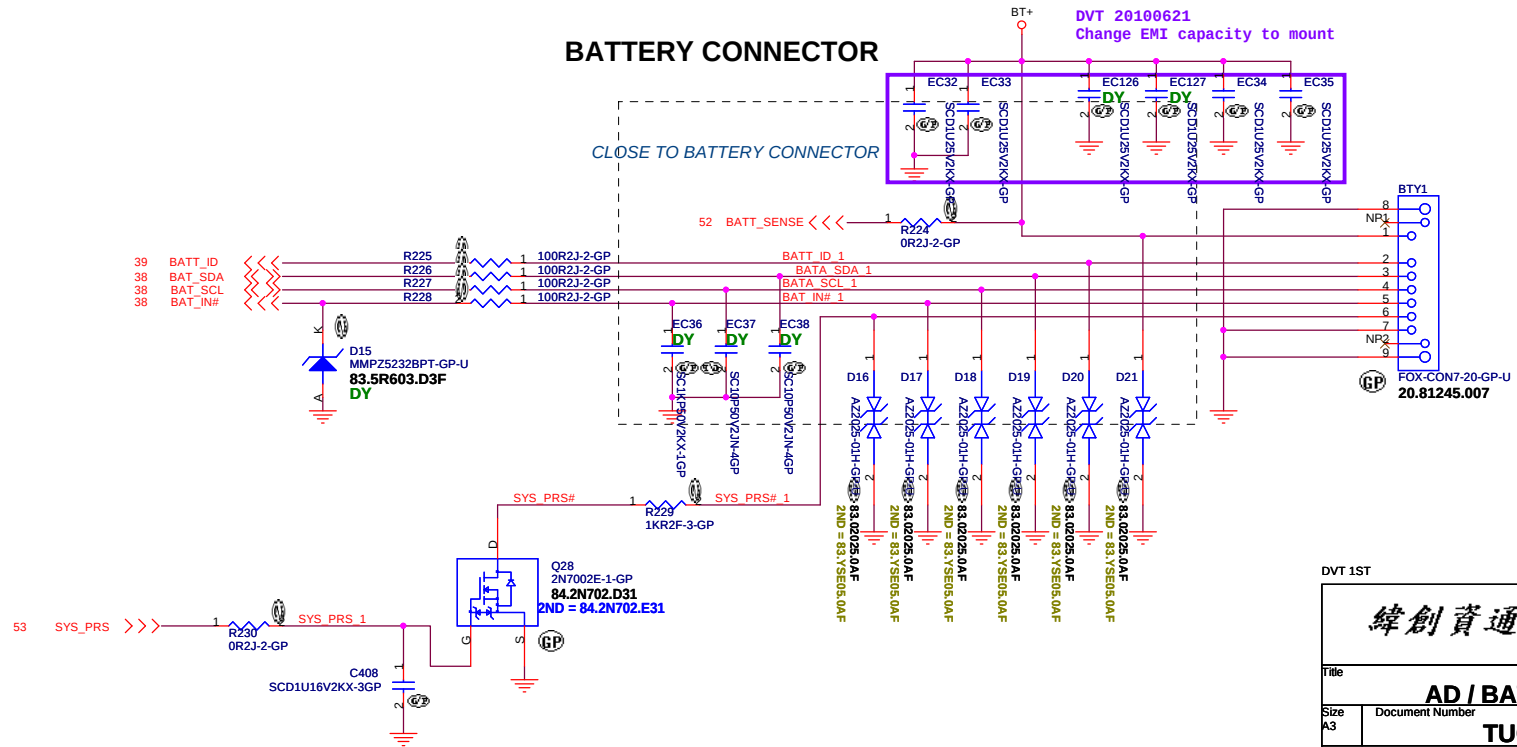
DVT 20100610
Change DCIN1 to 20.F0693.006
(follow connector list)

Adaptor in to generate DCBATOUT



BATTERY CONNECTOR

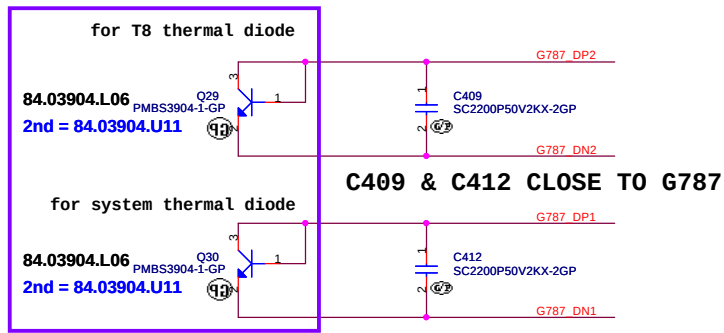
CLOSE TO BATTERY CONNECTOR



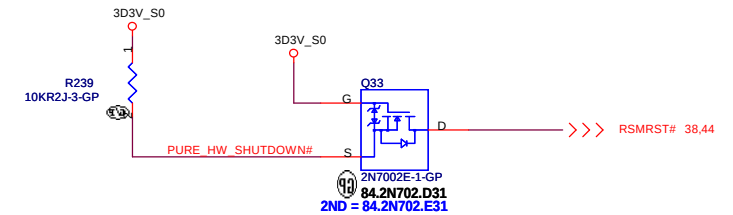
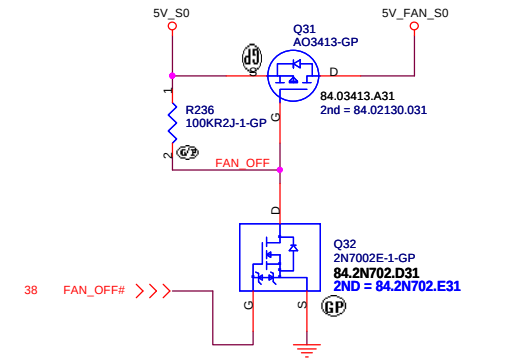
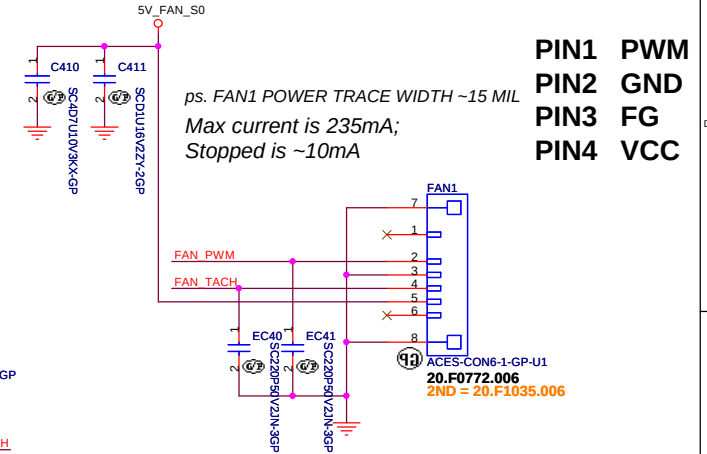
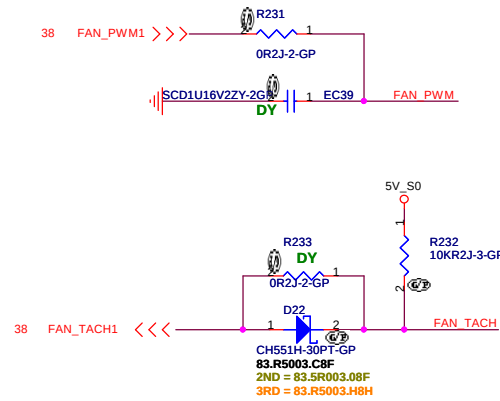
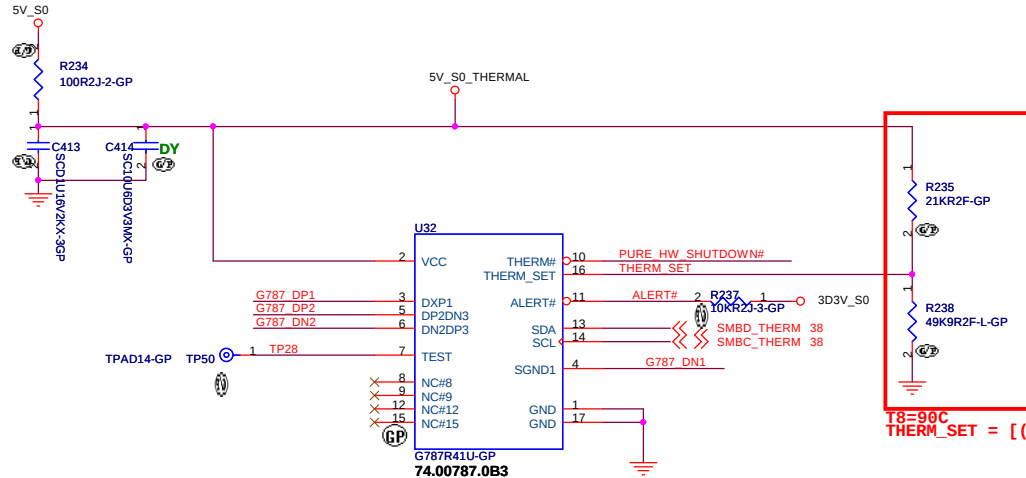
DVT 1ST

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

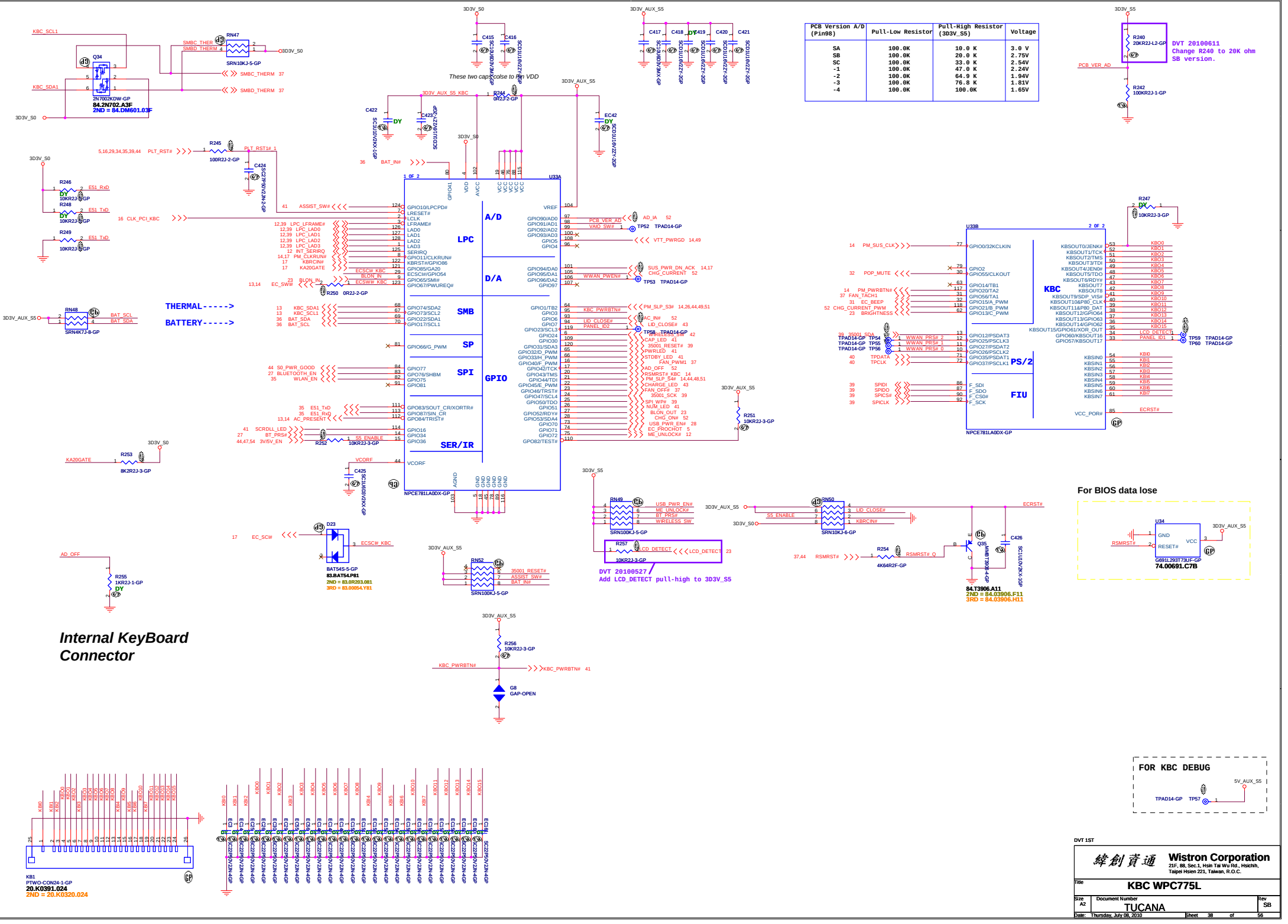
Title		
AD / BATT CONN		
Size	Document Number	Rev
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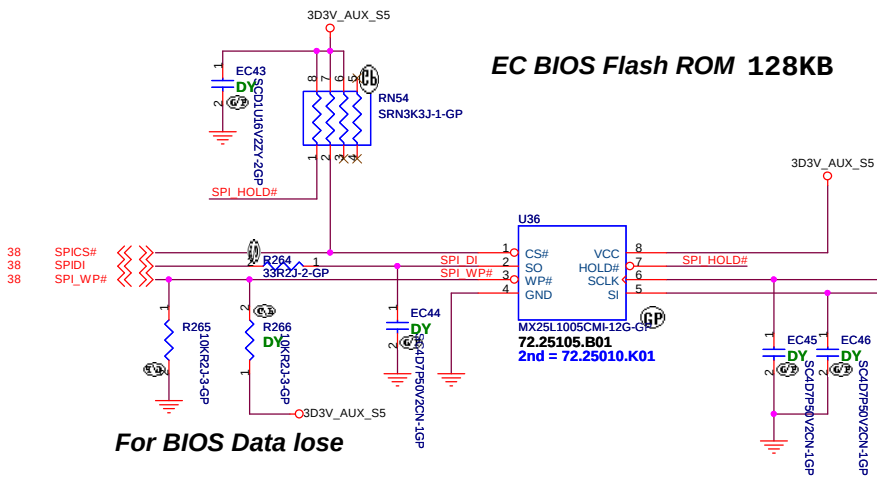


DVT 20100705
Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design



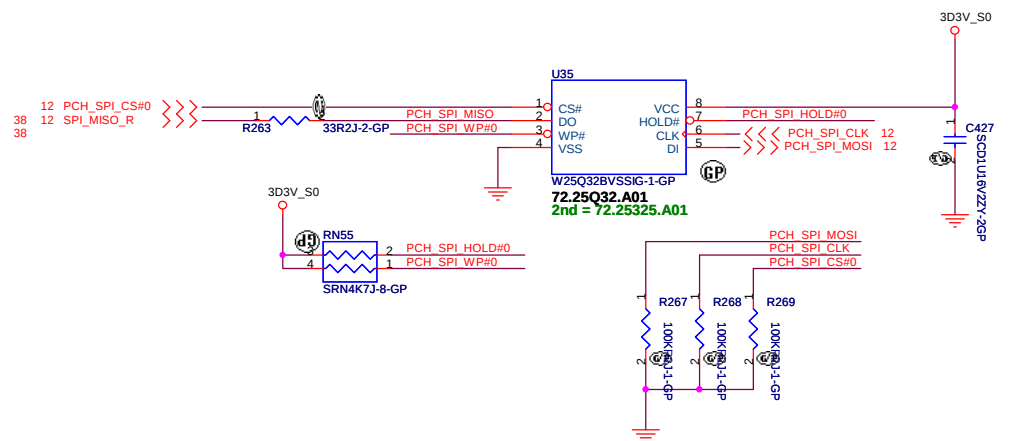
DVT 1ST



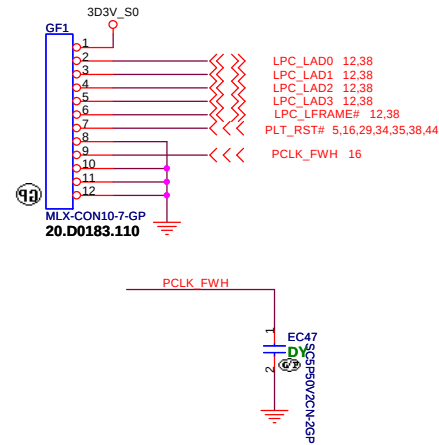


For BIOS Data lose

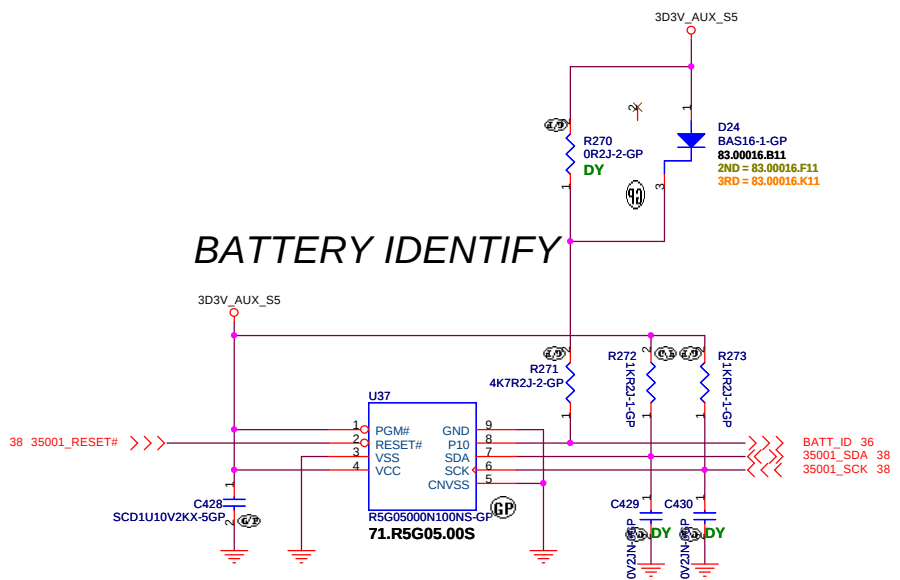
System BIOS Flash ROM (4MB)

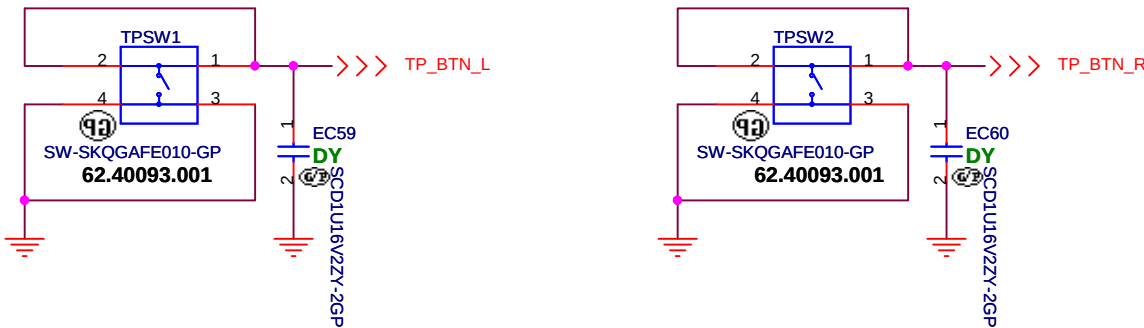
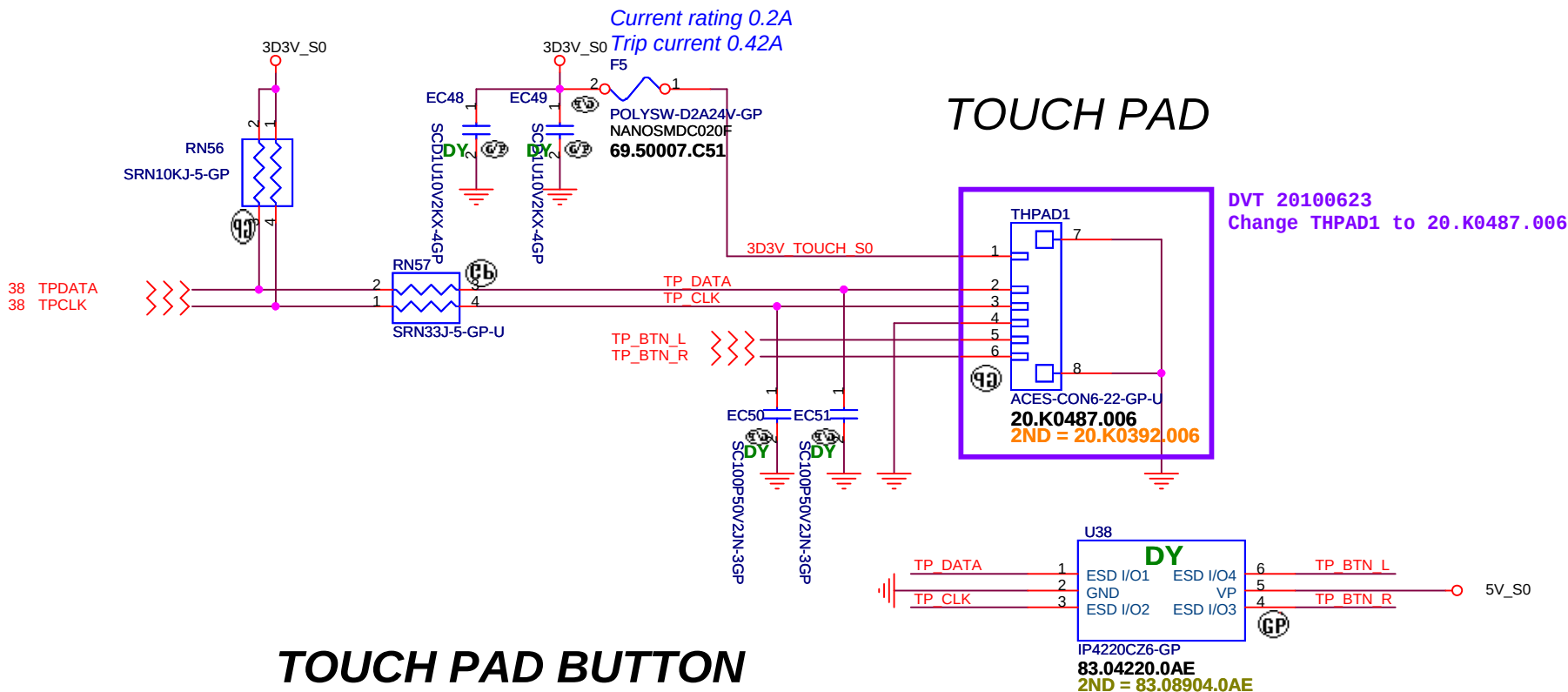


GOLDEN FINGER FOR DEBUG BOARD CONNECTOR (only install it on EVT)



BATTERY IDENTIFY





DVT 1ST

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

TouchPad

Size
A4

Document Number

TUCANA

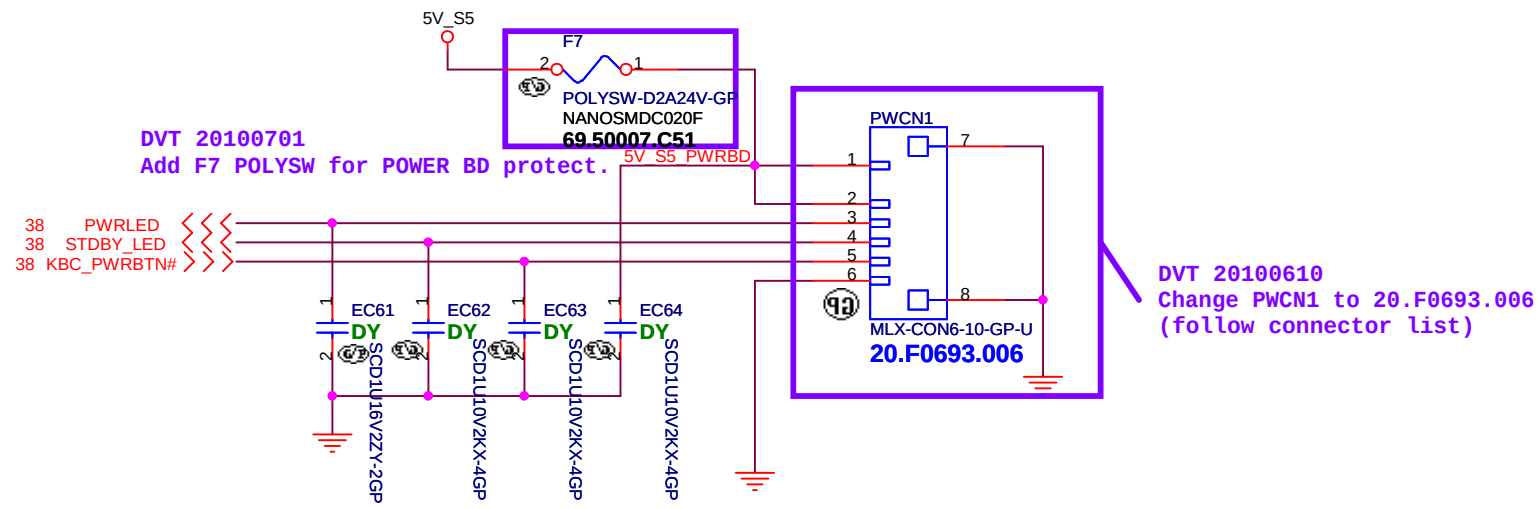
Rev

SB

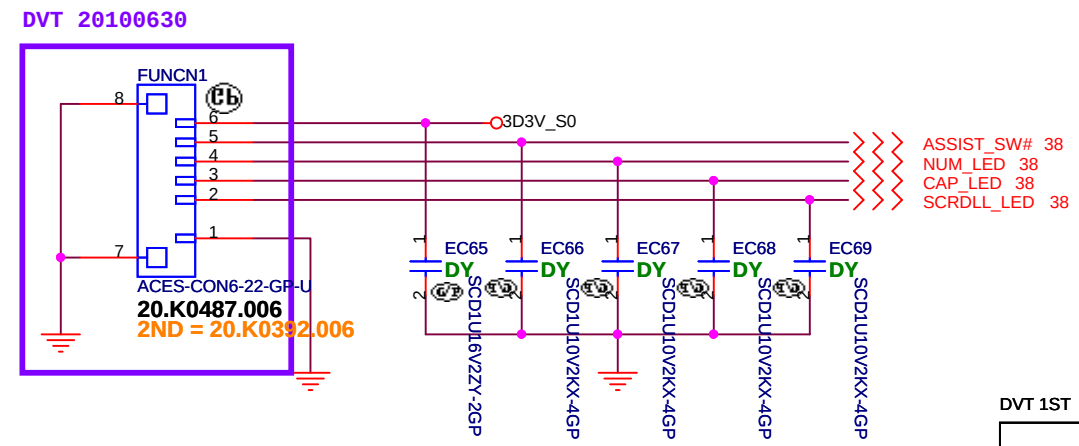
Date: Wednesday, July 07, 2010

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POWER BUTTON BD CONN



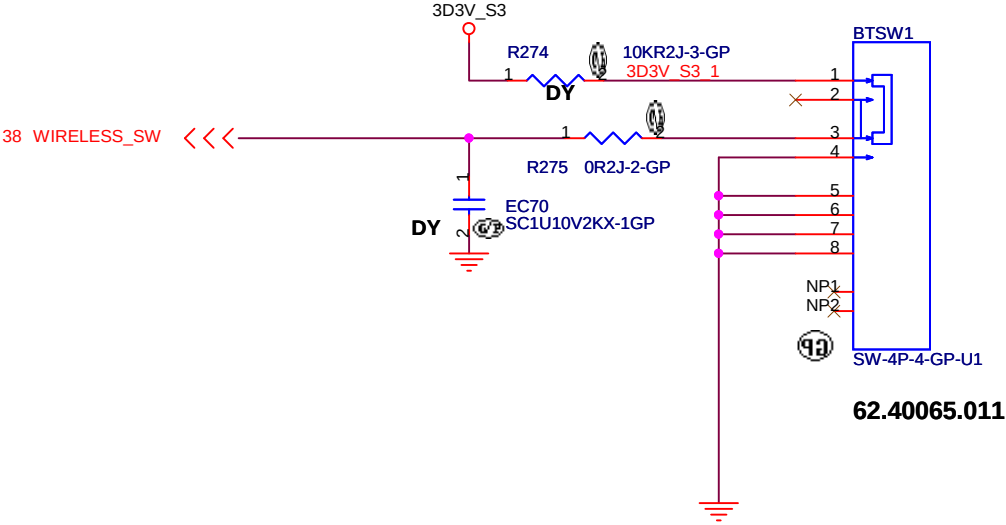
FUNCTION BD CONN



DVT 1ST

緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title	
FUNCTION BD & POWER BD	
Size	Document Number
	TUCANA
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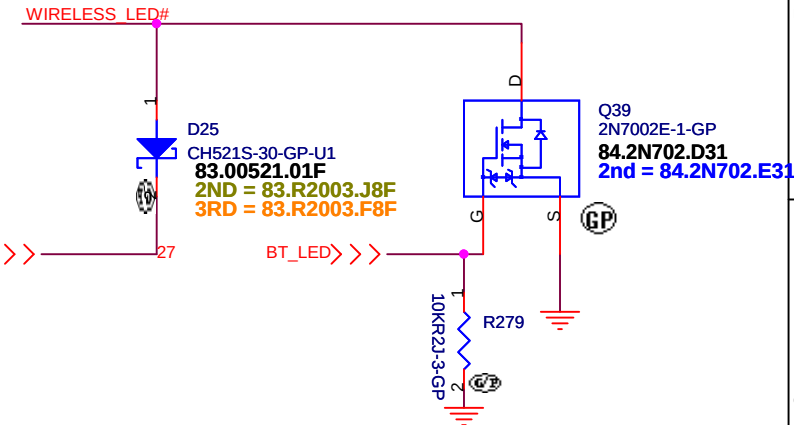
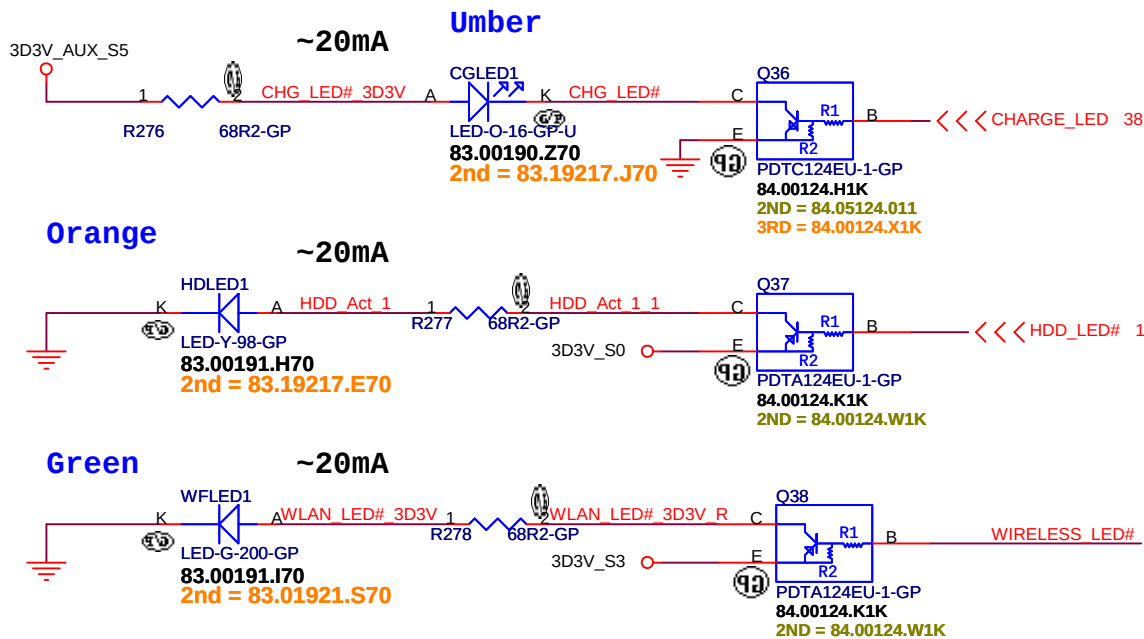
WLAN SWITCH



DVT 1ST

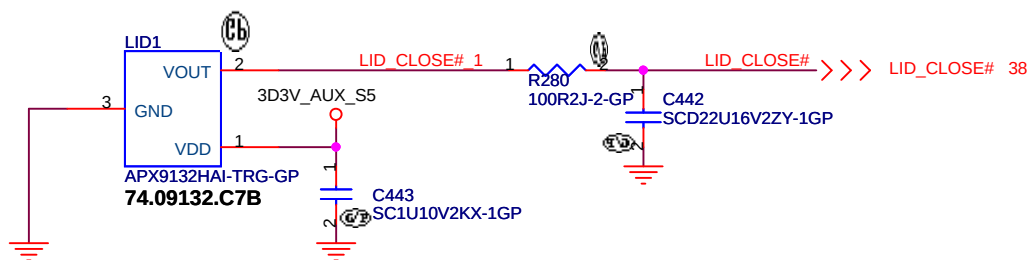
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Switch			
Size	Document Number		Rev
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LED



active	High	Low
WWAN(W_DISABLE#)	ON	OFF
WLAN(WLAN_LED#)	OFF	ON
Bluetooth(BT_LED)	ON	OFF

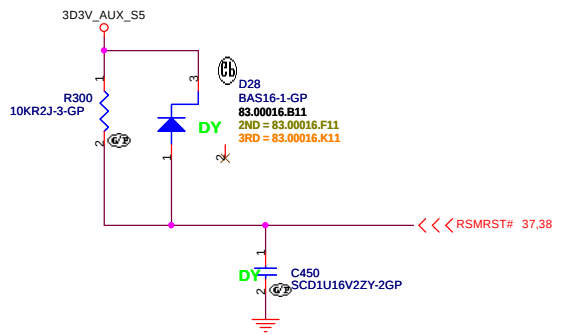
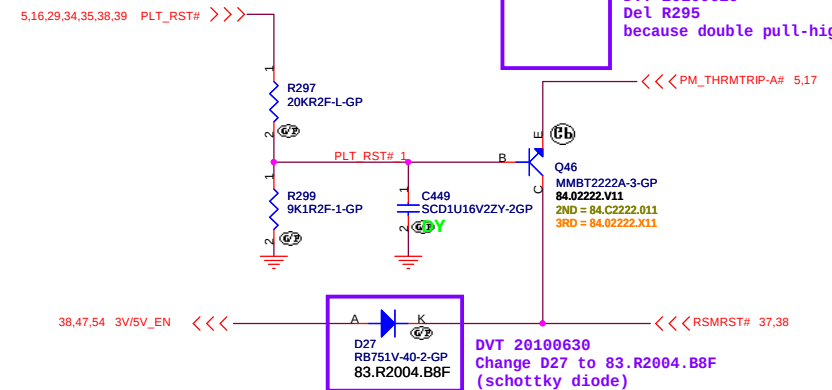
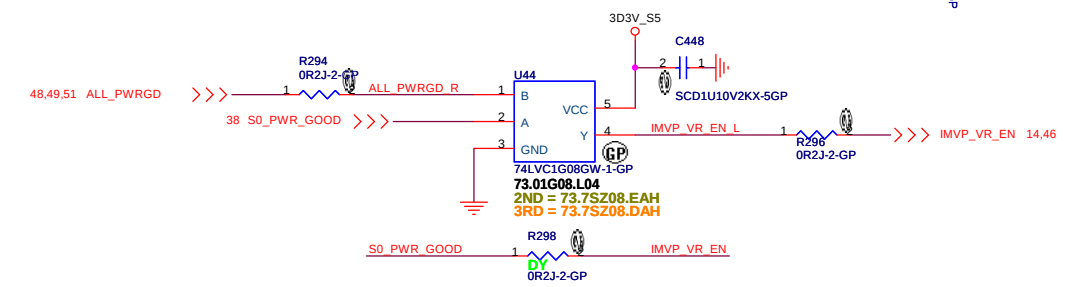
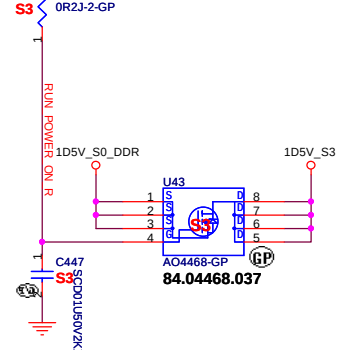
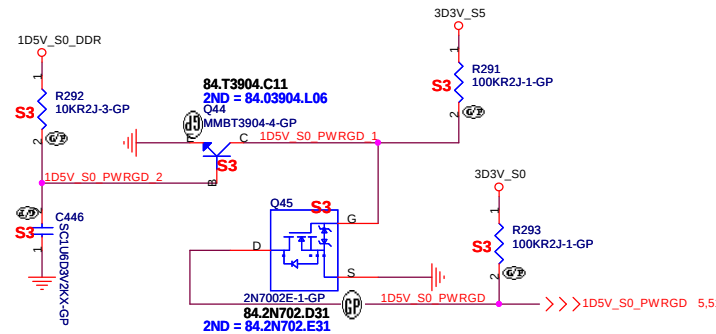
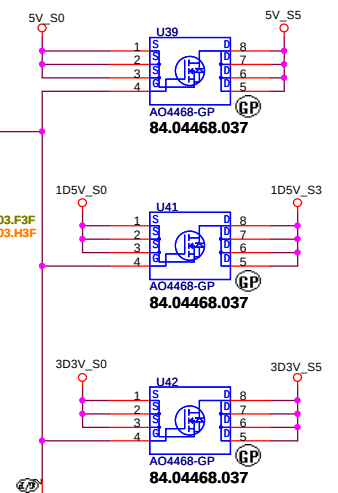
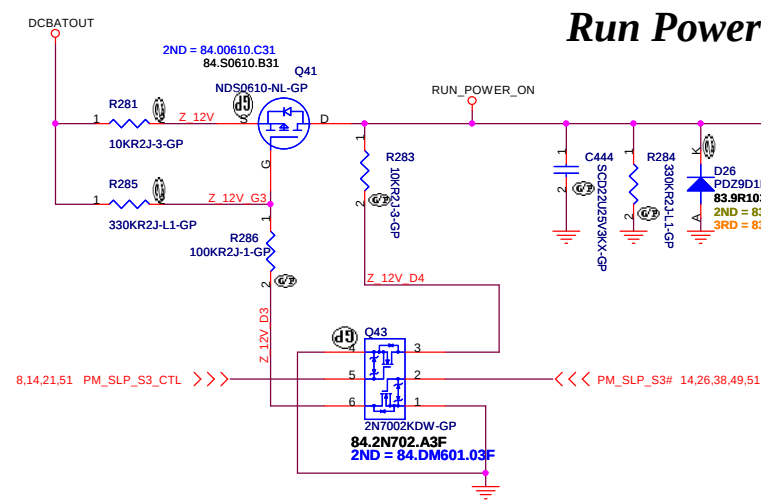
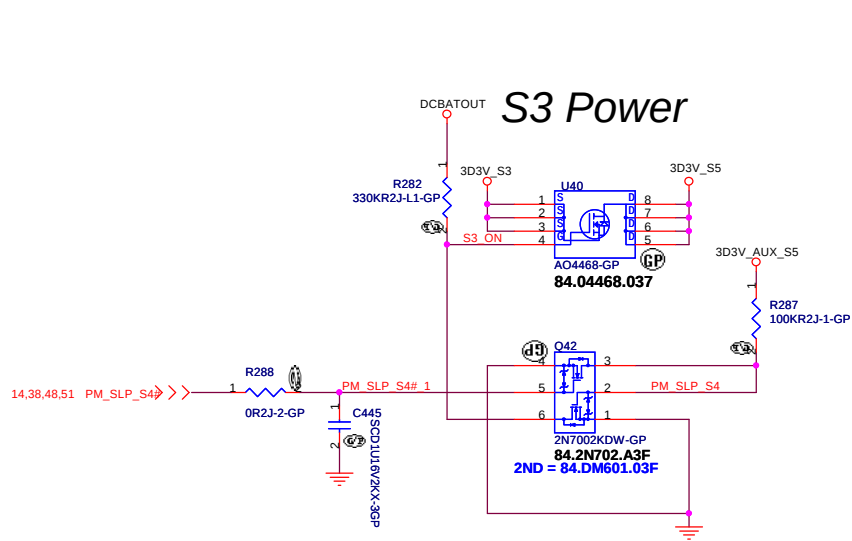
Cover Up Switch



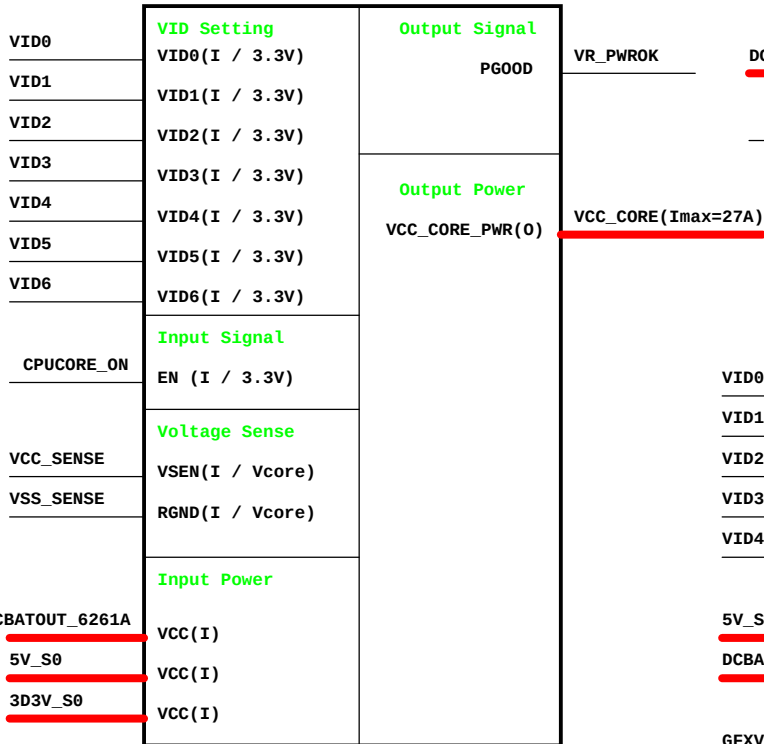
Common wireless SW(mechanical)	ON							
WLAN SW(software)	ON	OFF	ON	OFF	ON	OFF	ON	OFF
WWAN SW(software)	ON	ON	OFF	OFF	ON	ON	OFF	OFF
Bluetooth SW(software)	ON	ON	ON	ON	OFF	OFF	OFF	OFF
LED	TURN ON							OFF

DVT 1ST

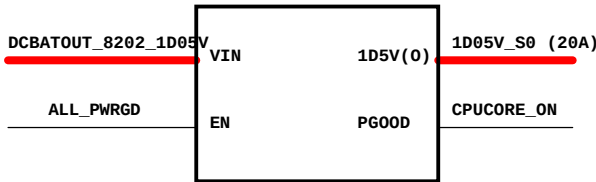
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
<i>Lid Switch & LED</i>			
Size	Document Number		Rev
	TUCANA		SB
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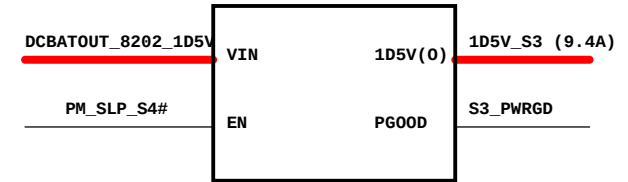
CPU_CORE
ADP3211



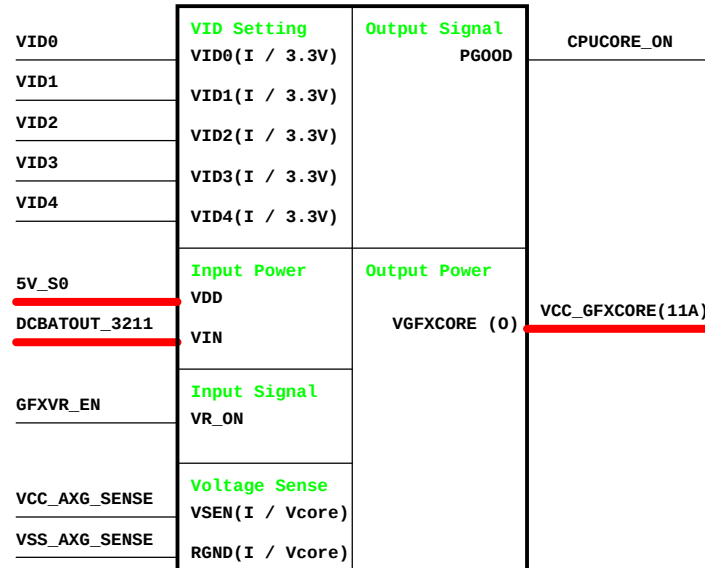
RT8209 1D05V_S0



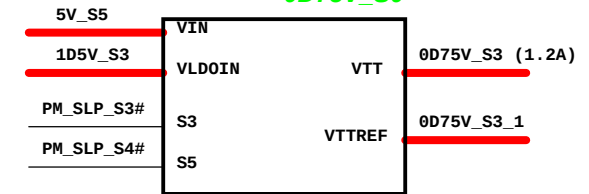
RT8209 1D5V_S3



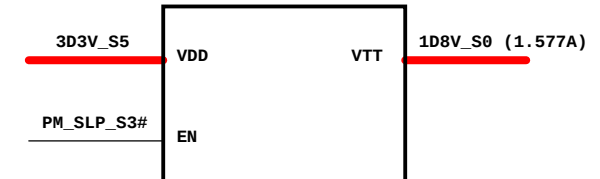
GFX_CORE/ VGA_CORE
ADP3211



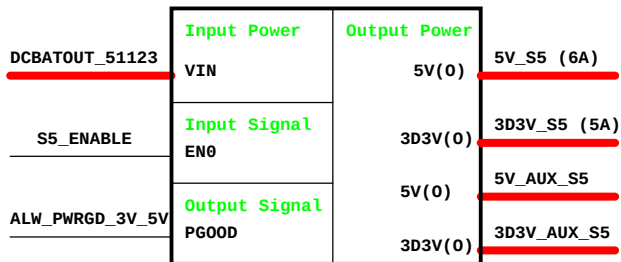
RT9026 0D75V_S0



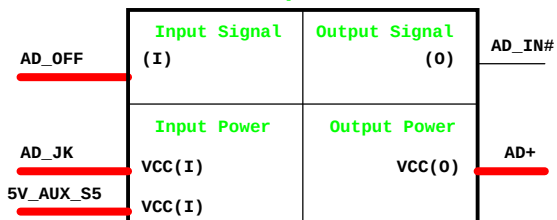
RT8015 1D8V_S0



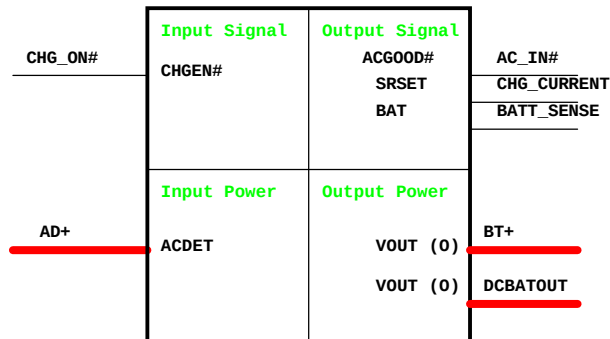
5V/3D3V
RT8223



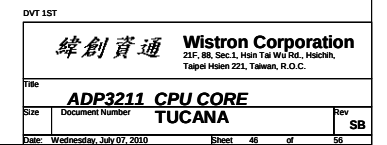
Adapter



Charger BQ24751



DVT 1ST



DCBATOUT

DCBATOUT_8209_105

1 2

GAP-CLOSE-PWR

G49

1 2

GAP-CLOSE-PWR

G51

1 2

GAP-CLOSE-PWR

G53

1 2

GAP-CLOSE-PWR

TC28

1 2

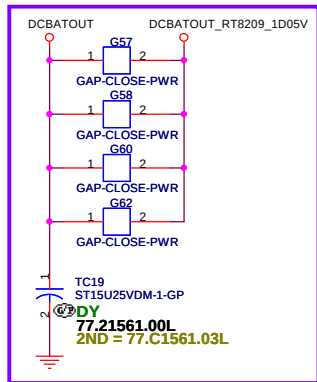
STMicroelectronics

7721561

[illegible][illegible]

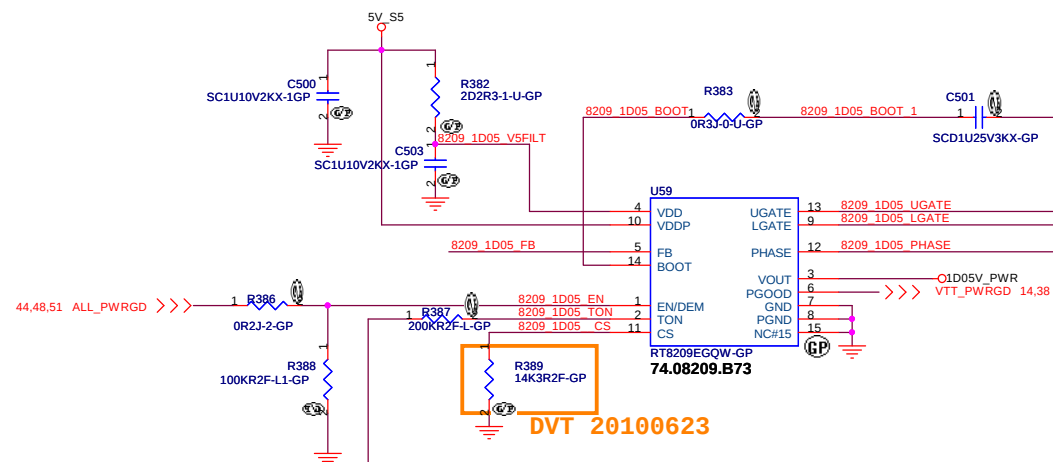
20100331

Title			
RT8209 1D5V			
Size	Document Number	Rev	SB
TUCANA			
Date:	Wednesday, July 07, 2010	Sheet 48 of 56	



DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

RT8209 1D05V



Id=24A
Qg=11nC
Rdson=9.4~13.5mohm

20100428

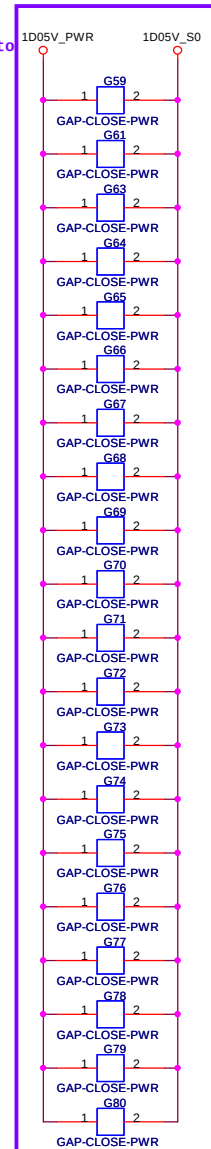
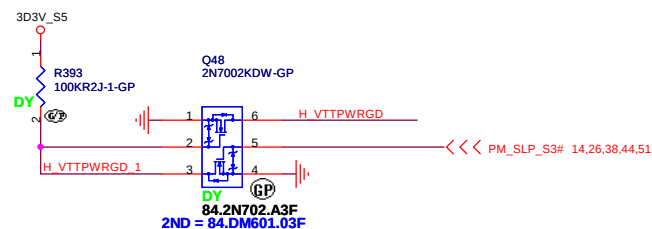
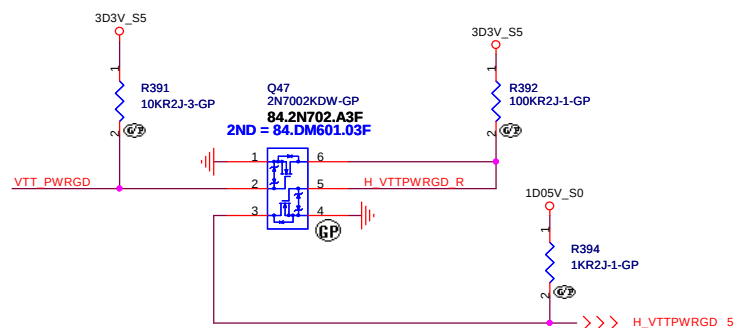
Id=50A
Qg=46nC
Rdson=2.3~3.6mohm

DVT 20100622
Mag. 0.56uH
DCR=1.6~1.8mohm
Idc=25A, Isat=40A

Iomax=20A
OCP>30A

$$V_{out}=0.75 \cdot (1+R1/R2)$$

The processor needs to be warned about the VTT rails shutdown at least 100 ns before the VTT rail falls to -5% of nominal value.



DVT 20100701
Change OPEN-GAP to
CLOSE-GAP

DVT 1ST

DCBATTOUT

DCBATTOUT_3211_GFX

G61

GAP-CLOSE-PWR

G62

GAP-CLOSE-PWR

G63

GAP-CLOSE-PWR

G64

GAP-CLOSE-PWR

G65

GAP-CLOSE-PWR

G66

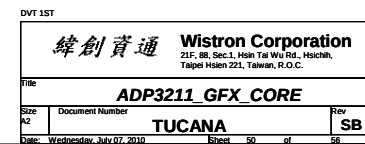
GAP-CLOSE-PWR

TC22

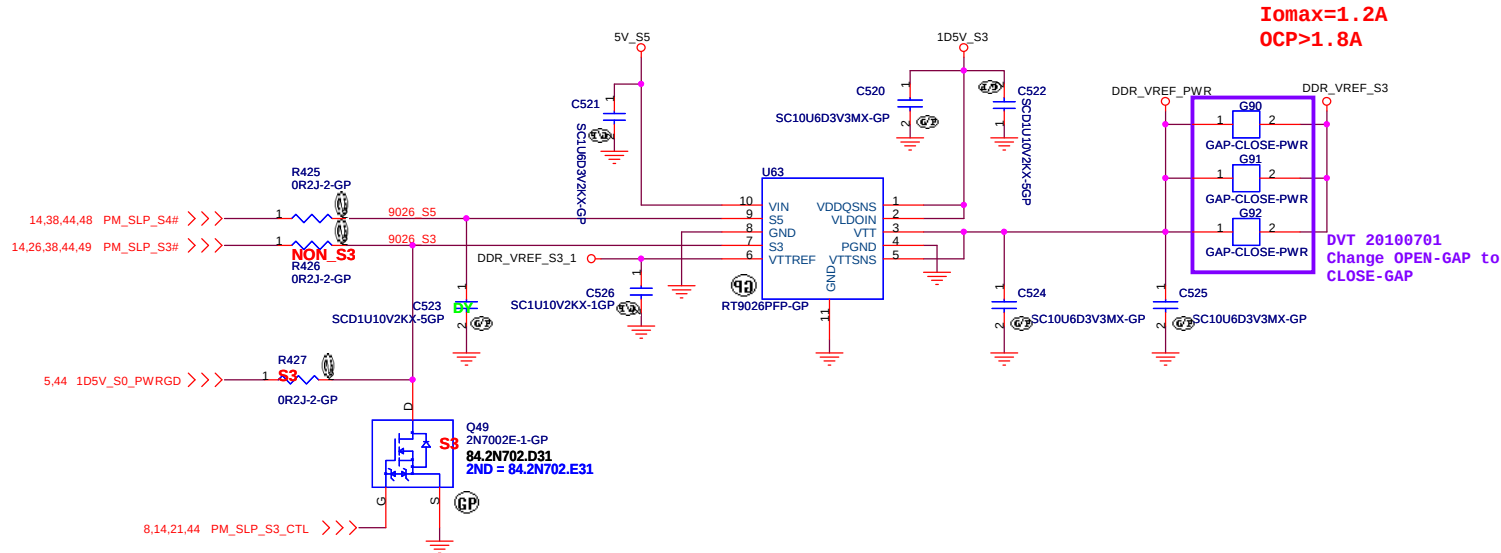
ST150/25VDM-1-6P

77.21561.00L

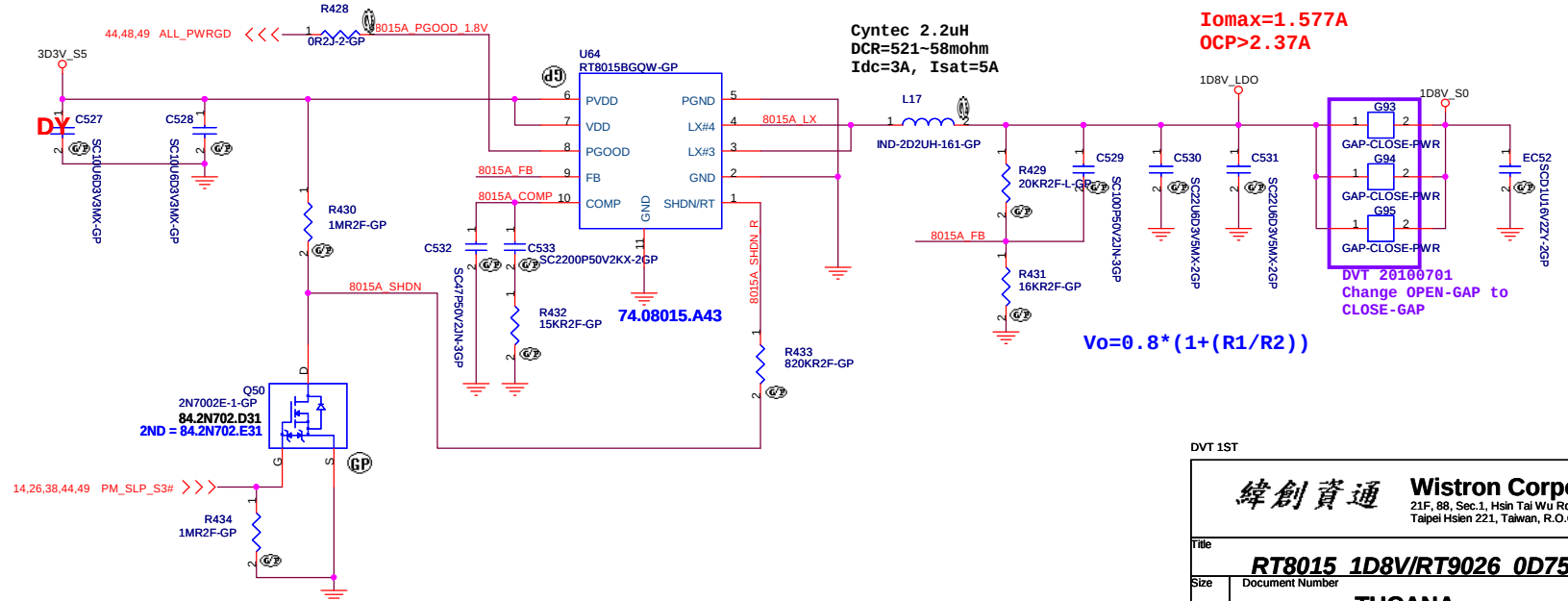
2ND = 77.1561.03L



RT9026 for 0D75V_S3



RT8015 for 1D8V_S0



DVT 1ST

緯創資通

Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title

RT8015 1D8V/RT9026 0D75

Size

Document Number

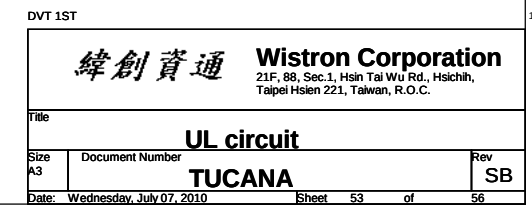
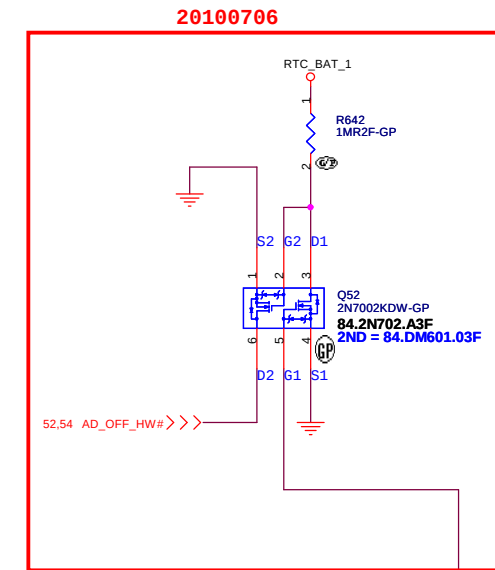
TUCANA

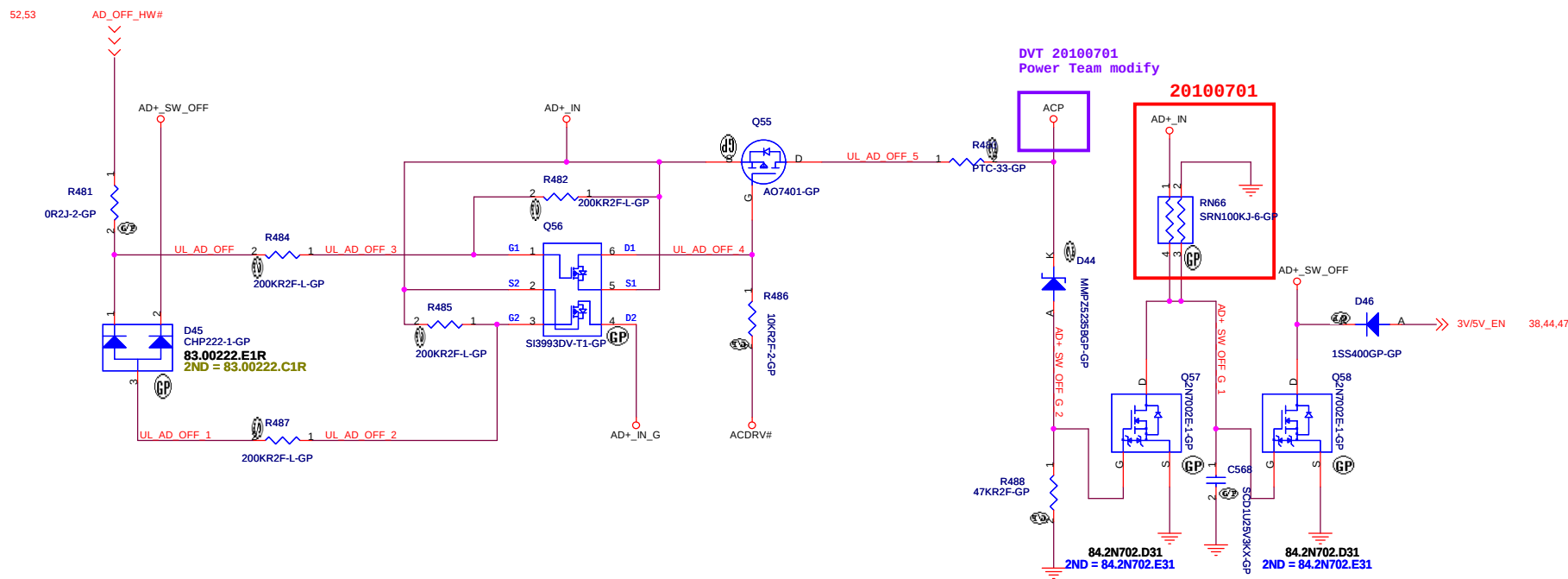
Rev

SB

Date: Wednesday, July 07, 2010

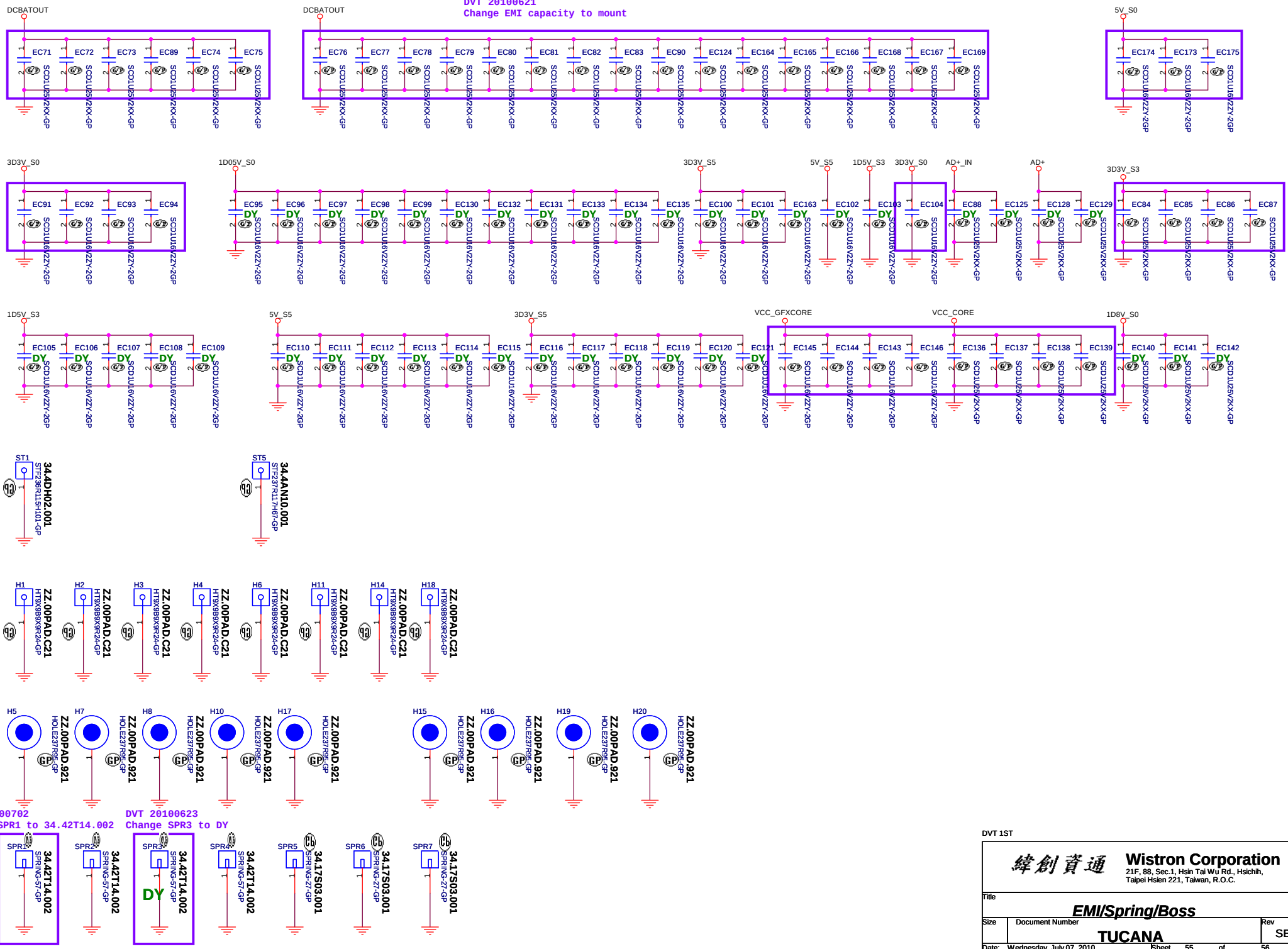
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DVT 1ST

緯創資通		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
UVP Protect			
Size A3	Document Number	Rev SB	
TUCANA			
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EVT

2010/5/17	P.52[BQ24751_Charger]	Del D31 2nd 3rd source	2010/7/2	P.38[KBC_NPCE781L / KB]	Rename H_PROCHOT# to EC_PROCHOT
2010/5/17	P.25[HDMI CONN_PS8101]	Change 2nd source to 69.4R500.151		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add R128 for EC_PROCHOT pull-low to Gnd
2010/5/24	P.26[HDD Connector]	Change R148 to 3.3K ohm, add C437 for PM_SLP_S3# Delay		P.5[CPU SFF(2 of 8)-CLK/Thermal]	Add Q61 for EC_PROCHOT to PROCHOT#
2010/5/27	P.38[KBC_NPCE781L / KB]	Add LCD_DETECT pull-high to 3D3V_S5		P.33[Audio Jack]	Add EC176 for HP_JD# to GND , Set Dummy for ESD.
2010/5/31	P.52[BQ24751_Charger]	Mount C546,R451,R449,Q51 for battery can't Changer			Add EC177 for MIC1_JD# to GND , Set Dummy for ESD.
2010/6/1	P.24[CRT CONN]	Change F6 to 69.44002.001, for Cadiz use		P.55[EMI/Spring/Boss]	Change SPR1 to 34.42T14.002
2010/6/4	P.33[Audio Jack]	Change MICIN1 to 20.10133.L11 , follow connector list			
	P.28[USB]	Change USB1,USB2,USB3 connector to 22.10321.Q71 [follow ME connector list]	2010/7/5	P.14[PCH (3 of 9)-DMI/FDI]	Change D3 to schottky diode.
2010/6/10	P.36[AD / BATT CONN]	Change DCIN1 to 20.F0693.006 (follow connector list)		P.37[Thermal / Fan Controllor]	Delete Q29,Q30 main source 84.T3904.C11, follow CARAVEL-CP design
	P.41[FUNCTION BD & POWER BD]	Change PWCN1 to 20.F0693.006 (follow connector list)	2010/7/6	P.53[UL CIRCUIT]	Rename R642 Pin1 contact to RTC_BAT_1 (Old use RTC_BAT),follow CARAVEL-CP
2010/6/11	P.41[FUNCTION BD & POWER BD]	Del FUNCN2 connector by ME request			
	P.38[KBC_NPCE781L / KB]	Change R240 to 20K ohm SB version.			
	P.25[HDMI CONN_PS8101]	Change R614~R617 to 200R2J , Set mount. [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C283,C364 to 1uF [for EMI request]			
	P.25[HDMI CONN_PS8101]	Change C282,C285 to 1KpF [for EMI request]			
2010/6/21	P.16[PCH (5 of 9)-PCI/USB]	Add PCI_REQ2# Pull-High to 3D3V_S0 by hang-up issue			
	P.31[Audio Codec ALC269]	Change EC23,EC24 to mount [for EMI request]			
	P.55[EMI/Spring/Boss]	Change DCBATOUT capacity to mount (EC71~83,EC89,EC90,EC124,EC164~169) [for EMI request]			
		Change 5V_S0 capacity to mount (EC173~EC175) [for EMI request]			
		Change 3D3V_S0 capacity to mount (EC91~94,EC104) [for EMI request]			
		Change 3D3V_S3 capacity to mount (EC84~87) [for EMI request]			
		Change VCC_GFXCORE capacity to mount (EC142~146) [for EMI request]			
		Change VCC_CORE capacity to mount (EC136~139) [for EMI request]			
	P.36[AD / BATT CONN]	Change BT+ capacity to mount (EC32~35) [for EMI request]			
	P.23[LCD CONN]	Change C258 to 470pF (BRIGHTNESS_CN) [for EMI request]			
	P.34[CardReader RTS5186]	Add C272 between BLON_OUT_R and Gnd [for EMI request]			
		Change C576~580,C589 to 5pF [CardReader VEVs test]			
	P.24[CRT CONN]	Add 0.1uF between MS_INS# and GND [CardReader VEVs test]			
		Change R114,R115,R119,R120 to 2.7K ohm [CRT VEVs report]			
2010/6/22	P.53[UL CIRCUIT]	UL Circuit modify. [Prevent the RTC_BAT keep protecting.]			
2010/6/23	P.40[TouchPad]	Change THPAD1 to 20.K0487.006 [Follow ME connector list]			
	P.55[EMI/Spring/Boss]	Change SPR3 to DY [for EMI request]			
	P.53[UL CIRCUIT]	Add D42(83.00400.D1F), D41(83.00400.D1F) components. [Reduce the RTC_BAT discharge]			
		connect R467 pin1 to D41 and D42 pin k. [Reduce the RTC_BAT discharge]			
	P.46[ADP3211_CPU CORE]	connect D42 pin A to AD+_in. [Reduce the RTC_BAT discharge]			
		connect D41 pin A to ACP_UVP [Reduce the RTC_BAT discharge]			
		Change U45 to 84.08030.037 [Improve High side Vgs induce voltage]			
		Change U47 to 84.08028.037 [Improve High side Vgs induce voltage]			
		Change U48 to 84.08028.037 [Improve High side Vgs induce voltage]			
		add these statements. [follow Power Team design]			
	P.47[RT8223_5V/3D3V]	Change R316 to 7.87K ohm (old use 7.32K ohm) [Tune CPU Imon value]			
	P.48[RT8209_1D5V]	Change C465 to 680pF (old use 560pF) [Tune CPU load line value]			
	P.49[RT8209_1D05V]	Change R353 to 84.5K ohm (old use 97.6K ohm) [Adjust OCP value]			
		Change L13 to 2.2uH (old use 3.3uH) [IC needs higher sensing voltage to detect it.]			
	P.50[ADP3211_GFX_CORE]	Change R377 to 7.5K ohm (old use 11.5K ohm) [Adjust OCP value]			
		Change R389 to 14.3K ohm (old use 10.2K ohm) [Adjust OCP value]			
		Change L15 to 0.56uH (old use 0.45uH) [Reduce the output ripple voltage]			
		Change R419 to 56.2K ohm (old use 53.6K ohm) [Tune GFX load line value]			
		Change TC26 to mount.(old Dummy) [Improve under-shoot voltage phenomenon]			
2010/6/25	P.13[PCH (2 of 9)-PCIE/CLK/SMB]	Change C156,C157 to 12pF [for Crystal vendor Test]			
	P.29[LAN AR8131M]	Change C346 to 18pF [for Crystal vendor Test]			
	P.34[CardReader RTS5186]	Change C384,C388 to 15pF [for Crystal vendor Test]			
2010/6/29	P.17[PCH (6 of 9)-GPIO/RSVD]	Change RN31 to R648,R649 (56 ohm) for pull-high 1.05V_S0			
		Del R295 , because double pull-high			
2010/6/30	P.41[FUNCTION BD & POWER BD]	Change pin define of the FUNCN1 connector [follow the way of FFC folder for ME]			
	P.19[PCH (8 of 9)-PWR\SATA\USB]	Del R101 , only use 3D3V_S5			
	P.12[PCH (1 of 9)-SATA/RTC/HDA]	Change D1 to 83.R2003.I81 (SCHOTTKY DIODE)			
	P.25[HDMI CONN_PS8101]	Change Q12 to 84.2N702.D31 (ESD Protected 1.0KV)			
	P.44[RUN POWER]	Change D27 to 83.R2004.B8F (schottky diode)			
2010/7/1	P.46[ADP3211_CPU CORE]	Change OPEN-GAP to CLOSE-GAP (G9~14)			
	P.47[RT8223_5V/3D3V]	Change OPEN-GAP to CLOSE-GAP (G18,G22,G26,G30,G20,G24,G28,G32)			
		Change OPEN-GAP to CLOSE-GAP (G19,G23,G27,G31,G34,G36)			
	P.48[RT8209_1D5V]	Change OPEN-GAP to CLOSE-GAP (G21,G25,G29,G33,G35,G37,G38)			
		Change OPEN-GAP to CLOSE-GAP (G47,G49,G51,G53)			
	P.49[RT8209_1D05V]	Change OPEN-GAP to CLOSE-GAP (G43~46,G48,G50,G52,G54~56)			
		Change OPEN-GAP to CLOSE-GAP (G57,G58,G60,G62)			
	P.50[ADP3211_GFX_CORE]	Change OPEN-GAP to CLOSE-GAP (G59,G61,G63~80)			
	P.51[RT8015_1D8V/ RT9026_0D75]	Change OPEN-GAP to CLOSE-GAP (G81~86)			
	P.41[FUNCTION BD & POWER BD]	Change OPEN-GAP to CLOSE-GAP (G90~95)			
	P.54[UVP Protect]	Add F7 POLYSW for POWER BD 5V_S5 protect.			
		Delete R483 and add RN66. (RN66 part number is 66.10436.04L)			
		Connect AD+_IN to RN66 pin 1.			
		Connect RN66 pin2 to GND.			
	P.53[UL CIRCUIT]	Connect RN66 pin3 and pin4 to AD+_SW_OFF_G_1			
		Change R468 part number to the 64.36025.6DL			
		Change R469 to the part number 64.30025.6DL			
		Cummy R471 and mount D39.			
		Delete D40 and RN58.			
		Add R642. (Part number is 64.10045.6DL)			
		Connect R642 pin 1 to RTC_BAT.			
		Connect R642 pin2 to Q52 pin 2 and pin3.			
		Connect ACP to R435 pin 1.			
	P.52[BQ24751_Charger]	UPDATE BTCN1 PCB LAYOUT (REMOVE THE NPTH)			
	P.27[Bluetooth]				

<Core Design>