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Intel Skylake-U Platform

Skylake-U CPU (TDP 15W) SoC

Project Information

Phase: EVT

PCB AND SILKSCREEN COLOR		
Program Phase	**Color of PCB**	**Silkscreen**
EVT	**RED**	**YELLOW**
DVT	**LIGHT BLUE**	**YELLOW**
PVT/MVB / PRODUCTION	**GREEN**	**WHITE**

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PROJECT: HP-Hawaii

Size	Document Number	Rev
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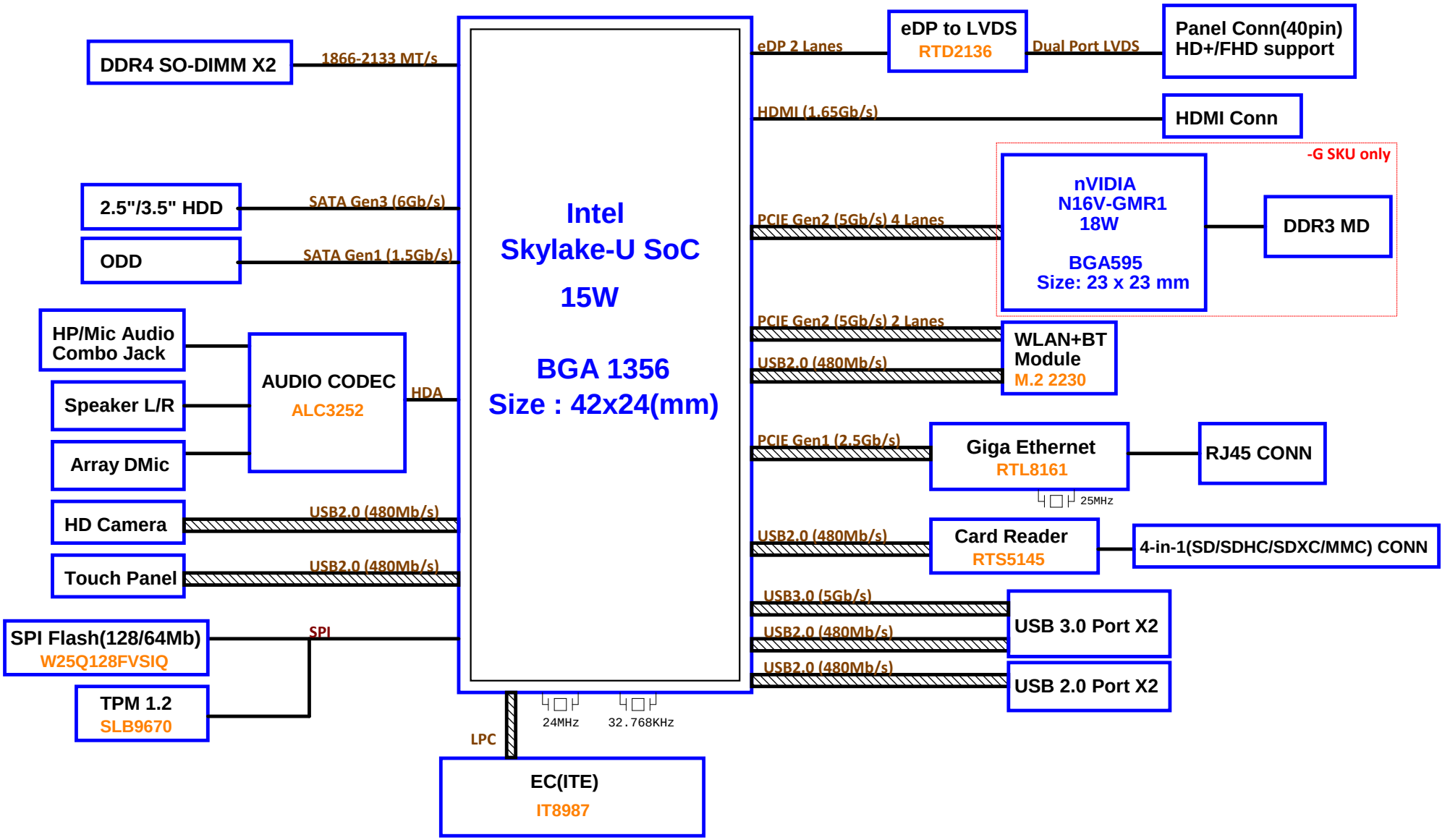
Intel Skylake-U Platform Block Diagram (Hawaii-G/-U)



[5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,7,17,46,48] +VCCIO
[5,6,7,10,43,46] +VCCSTPLL

HDMI

U21A SKL_ULT ?

[22] IN_D2# → E55 DDI1_TXN[0]
[22] IN_D2 → F55 DDI1_TXP[0]
[22] IN_D1# → E58 DDI1_TXN[1]
[22] IN_D1 → F58 DDI1_TXP[1]
[22] IN_D0# → F53 DDI1_TXN[2]
[22] IN_D0 → G53 DDI1_TXP[2]
[22] IN_CLK# → F56 DDI1_TXN[3]
[22] IN_CLK → G56 DDI1_TXP[3]

C50 DDI2_TXN[0]
D50 DDI2_TXP[0]
C52 DDI2_TXN[1]
D52 DDI2_TXP[1]
A50 DDI2_TXN[2]
B50 DDI2_TXP[2]
D51 DDI2_TXN[3]
C51 DDI2_TXP[3]

DDI

EDP

DISPLAY SIDEBANDS

EDP_TXN[0] C47 → INT_EDP_TXN0 → INT_EDP_TXN0 [20]
EDP_TXP[0] C46 → INT_EDP_TXP0 → INT_EDP_TXP0 [20]
EDP_TXN[1] D46 → INT_EDP_TXN1 → INT_EDP_TXN1 [20]
EDP_TXP[1] C45 → INT_EDP_TXP1 → INT_EDP_TXP1 [20]
EDP_TXN[2] A45
EDP_TXP[2] B45
EDP_TXN[3] A47
EDP_TXP[3] B47

EDP_AUXN E45 → INT_EDP_AUXN → INT_EDP_AUXN [20]
EDP_AUXP F45 → INT_EDP_AUXP → INT_EDP_AUXP [20]

EDP_DISP_UTIL B52

DDI1_AUXN G50
DDI1_AUXP F50
DDI2_AUXN E48
DDI2_AUXP F48
DDI3_AUXN G46
DDI3_AUXP F46

[22] SDVO_CLK → L13 GPP_E18/DDPB_CTRLCLK
[22] SDVO_DATA → L12 GPP_E19/DDPB_CTRLDATA

+3V R208 2.2K_4 → NZ N8 GPP_E20/DDPC_CTRLCLK
GPP_E21/DDPC_CTRLDATA

TP22 → N11 GPP_E22/DDPD_CTRLCLK
N12 GPP_E23/DDPD_CTRLDATA

+VCCIO R116 24.9/F_4 → EDP_RCOMP E52 EDP_RCOMP

GPP_E13/DDPB_HPD0 L9 → PCH_HDMI_HPD → PCH_HDMI_HPD [22]
GPP_E14/DDPC_HPD1 L7
GPP_E15/DDPD_HPD2 L8
GPP_E16/DDPE_HPD3 N9
GPP_E17/EDP_HPD L10 → EDP_HPD → EDP_HPD [20]

EDP_BKLTEN R12 → PCH_LVDS_BLON → PCH_EDP_BLON [21]
EDP_BKLTCTL R11 → PCH_DPST_PWM → PCH_DPST_PWM [20]
EDP_VDDEN U13 → PCH_LCDVCC_EN → PCH_LCDVCC_EN [21]

SKL_ULT
REV = 1

1 OF 20

?

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

Reserve EDP_HPD opposites circuit!

+3V
R505 *10K_4 → EDP_HPD
R504 100K_4

U21D SKL_ULT ?

TP45 → CATERR# D63
[29] EC_PECI → EC_PECI A54
[29,43,47] H_PROCHOT# → R408 499/F_4 → PROCHOT# C65
PM_THRMTRIP# C63
THERMTRIP# A65
SKTOCC#

CPU MISC

[17] XDP_BPM0 → C55 BPM#[0]
[17] XDP_BPM1 → D55 BPM#[1]
B54 BPM#[2]
C56 BPM#[3]

[26] RF_OFF → A6 GPP_E3/CPU_GP0
A7 GPP_E7/CPU_GP1
BA5 GPP_B3/CPU_GP2
AY5 GPP_B4/CPU_GP3

R170 49.9/F_4 → PROC_POPIRCOMP AT16
R164 49.9/F_4 → PCH_OPI_RCOMP AU16
R79 49.9/F_4 → EDRAM_OPIO_RCOMP H66
R80 49.9/F_4 → EOPIO_RCOMP H65

PROC_POPIRCOMP
PCH_OPIRCOMP
OPCE_RCOMP
OPC_RCOMP

JTAG

PROC_TCK B61 → XDP_TCK0 → XDP_TCK0 [17]
PROC_TDI D60 → XDP_TDI_CPU → XDP_TDI_CPU [17]
PROC_TDO A61 → XDP_TDO_CPU → XDP_TDO_CPU [17]
PROC_TMS C60 → XDP_TMS_CPU → XDP_TMS_CPU [17]
PROC_TRST# B59 → XDP_TRST#_CPU → XDP_TRST#_CPU [17]

PCH_JTAG_TCK B56 → JTAG_TCK_PCH → JTAG_TCK_PCH [17]
PCH_JTAG_TDI D59 → JTAG_TDI_PCH → JTAG_TDI_PCH [17]
PCH_JTAG_TDO A56 → JTAG_TDO_PCH → JTAG_TDO_PCH [17]
PCH_JTAG_TMS C59 → JTAG_TMS_PCH → JTAG_TMS_PCH [17]
PCH_TRST# C61 → XDP_TRST#_CPU
JTAGX A59 → JTAGX_PCH → JTAGX_PCH [17]

SKL_ULT
REV = 1

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+VCCSTPLL
PM_THRMTRIP# R422 1K_4

Processor pull-up (CPU)
TO BE REPLACED WITH 1K OHMS FOR SKL . 470 OHM IS FOR I/P

PLACE NEAR CPU

+VCCIO
XDP_TMS_CPU R435 *51_4
XDP_TDI_CPU R436 *51_4
XDP_TDO_CPU R427 *51_4

+VCCSTPLL
H_PROCHOT# R406 1K_4
XDP_TCK0 R430 51_4
XDP_TRST#_CPU R439 51_4

EC-PV-01

+VCCIO R428 *0/S_4 →
R431 *51_4 → JTAGX_PCH
R440 51_4 → JTAG_TMS_PCH
R444 51_4 → JTAG_TDI_PCH
R448 51_4 → JTAG_TDO_PCH
R443 51_4 → JTAG_TCK_PCH

Close to Chipset

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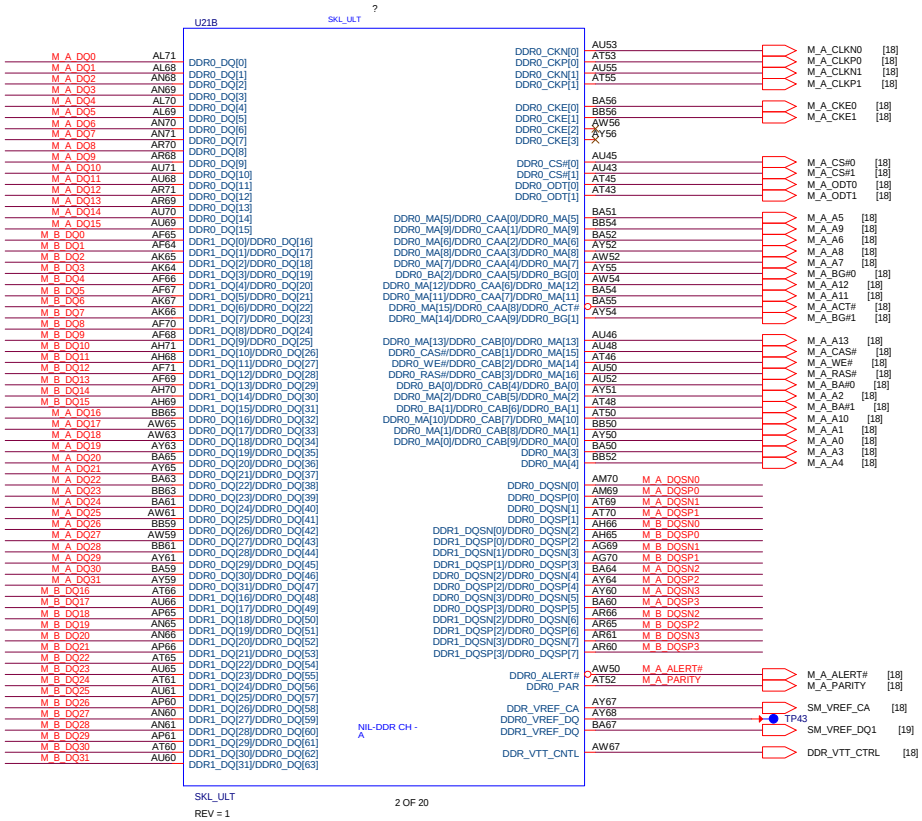
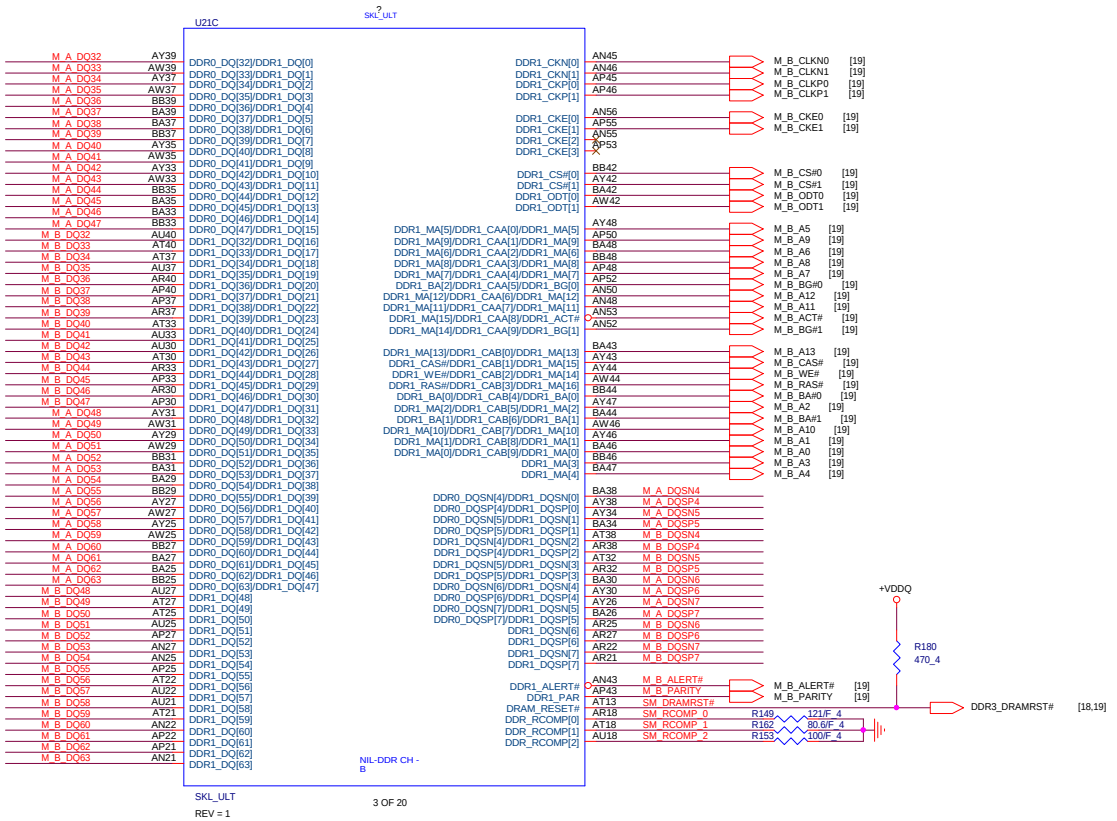
SkyLake ULT Processor (DDR4 IL)





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[11,12,13,15,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[3,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[21,23,27,28,32,39,40,41,43,45,46,47,48,52] +5V_S5
[3,7,17,46,48] +VCCIO
[3,6,7,10,43,46] +VCCSTPLL
[14,16] +3V_RTC_2

U21K SKL_ULT ?
SYSTEM POWER MANAGEMENT

[24,26,29,31,33] PLTRST#
[17] SYS_RESET#
[17,29] RSMRST#
R485 *0/S_4 RSMRST#_R
R403 *10K_4 H_VCCST_PWRGD
EC-PV-01
[17,29] HWPG R484 *0/S_4
[29] EC_SUSPWRACK
[29] EC_SUSACK#
*0_4 R580
*0_4 R192
[24,26] PCIE_WAKE#
TP23
TP58
TP18

PLTRST# AN10
SYS_RESET# B5
RSMRST# AY17
PROCPWRGD A68
H_VCCST_PWRGD B65
SYS_PWROK B6
PCH_PWROK BA20
DPWROK BB20
SUSWARN# AR13
SUSACK# AP11
PCIE_WAKE# BB15
PCIE_LAN_WAKE# AM15
LAN_DIS# AW17
AT15

GPP_B13/PLTRST#
SYS_RESET#
RSMRST#
PROCPWRGD
VCCST_PWRGD
SYS_PWROK
PCH_PWROK
DSW_PWROK
GPP_A13/SUSWARN#/SUSPWRDNACK
GPP_A15/SUSACK#
WAKE#
GPD2/LAN_WAKE#
GPD11/LANPHYPC
GPD7/RSVD

GPP_B12/SLP_S0# AT11 PM_SLP_S0#
GPD4/SLP_S3# AP15
GPD5/SLP_S4# BA16
GPD10/SLP_S5# AY16
SLP_SUS# AN15
SLP_LAN# AW15 SLP_LAN#
GPD9/SLP_WLAN# BB17 SLP_WLAN#
GPD6/SLP_A# AN16
GPD3/PWRBTN# BA15 DNBSWON#
GPD1/ACPRESENT AY15 AC_PRESENT_EC
GPD0/BATLOW# AU13 PM_BATLOW_N_EC
GPP_A11/PME# AU11
INTRUDER# AP16 INTRUDER#_R R177 1M_4 +3V_RTC_2
GPP_B11/EXT_PWR_GATE# AM10 EXT_PWR_GATE#
GPP_B2/VRALERT# AM11

PM_SLP_S0# [17,29]
SUSB# [17,29]
SUSC# [17,29]
SLP_S5# [17,29]
PM_SLP_SUS# [29]
TP62
TP60
SLP_A# [17]
TP31
DNBSWON# [17,29]
AC_PRESENT_EC [29]
TP27

SKL_ULT
REV = 1
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?

PCH Pull-high/low(CLG)

+3V_S5
SUSWARN# R189 *10K_4
SUSACK# R191 *10K_4
PM_BATLOW_N_EC R181 10K_4

+3V_S5
PCIE_WAKE# R493 1K_4
AC_PRESENT_EC R490 10K_4
PCIE_LAN_WAKE# R187 10K_4
EXT_PWR_GATE# R186 *20K/F_4

+3V
SYS_RESET# R500 10K_4
PLTRST# R222 *10K/F_4
R223 100K/F_4
RSMRST# R487 10K_4
DPWROK R481 *100K/F_4

RSMRST#
SYS_RESET#
PLTRST#
EC5 *220P/50V_4
C554 *220P/50V_4
C549 *220P/50V_4

[29] EC_DPWROK
RSMRST# R483 *0_4 DPWROK
EC_DPWROK R538 *0/S_4
EC-PV-01

Close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"

+VCCIO +VCCSTPLL
R401 1K_4
R405 *1K_4
HWPG D14 1 2 RB500V-40 H_VCCST_PWRGD_R R404 60.4_4 H_VCCST_PWRGD
C512 *10P/50V_4

+VCCIO +5V_S5 +3V_S5
R478 15K_4
R479 100K_4
R476 10K_4
HWPG
+1.0V_PWRGD_G2 2 Q31 2N7002K
R475 100K_4
+1.0V_PWRGD_G1 2 Q32 METR3904-G
C530 0.1U/16V_4
R480 100K_4

System PWR_OK(CLG)

SYS_PWROK
EC-PV-01
R496 *0/S_4
EC_PWROK
EC_PWROK [29]
C552 *0.1U/16V_4
R497 100K/F_4

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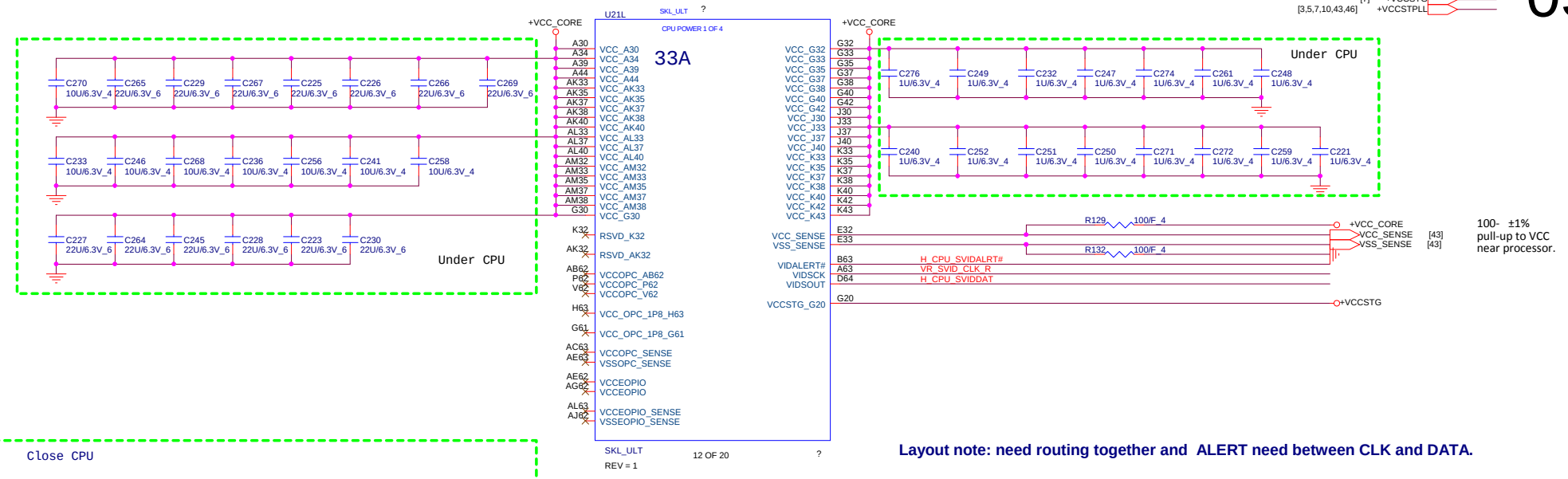
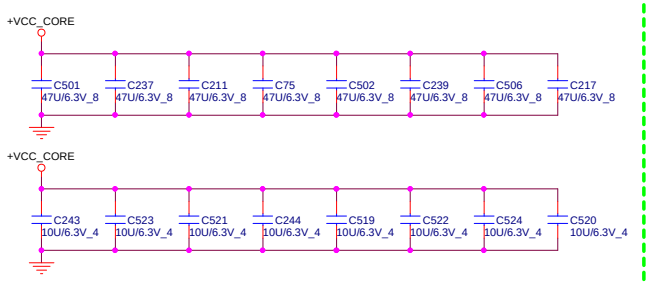
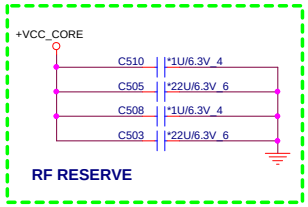
[32,43,44] +VCC_CORE
[7] +VCCSTG
[3,5,7,10,43,46] +VCCSTPLL



100- ±1% pull-up to VCC near processor.

Close CPU

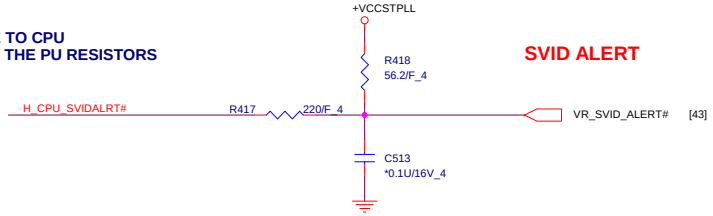




Layout note: need routing together and ALERT need between CLK and DATA.

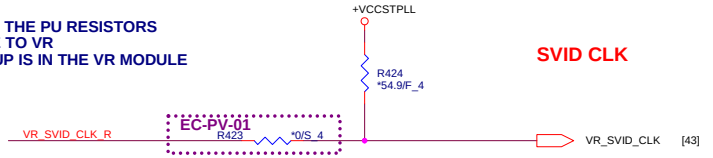
CLOSE TO CPU
PLACE THE PU RESISTORS

SVID ALERT



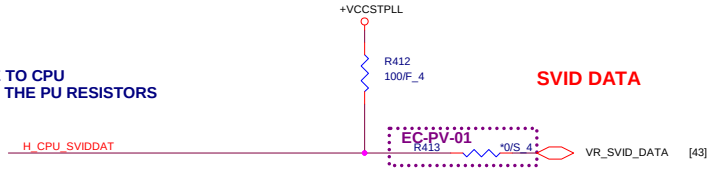
PLACE THE PU RESISTORS
CLOSE TO VR
PULL UP IS IN THE VR MODULE

SVID CLK



CLOSE TO CPU
PLACE THE PU RESISTORS

SVID DATA



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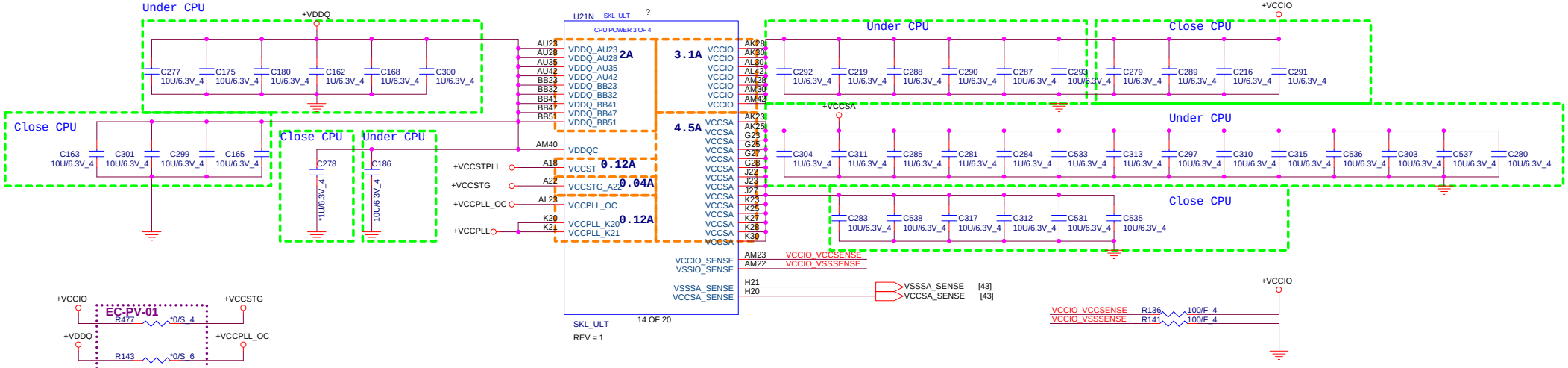
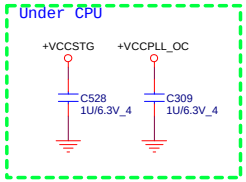
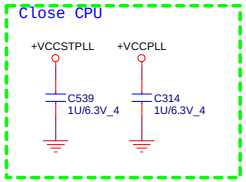
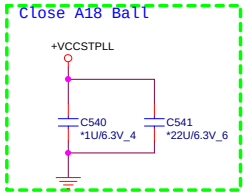
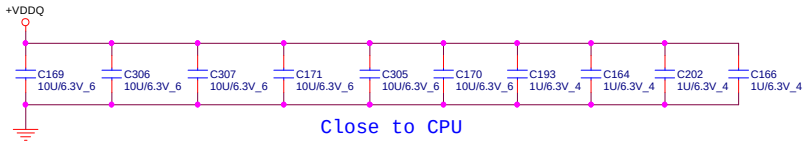
[3,5,17,46,48] +VCCIO
[43,45] +VCCSA
[4,18,19,32,40] +VDDQ
[3,5,6,10,43,46] +VCCSTPLL
[6] +VCCSTG











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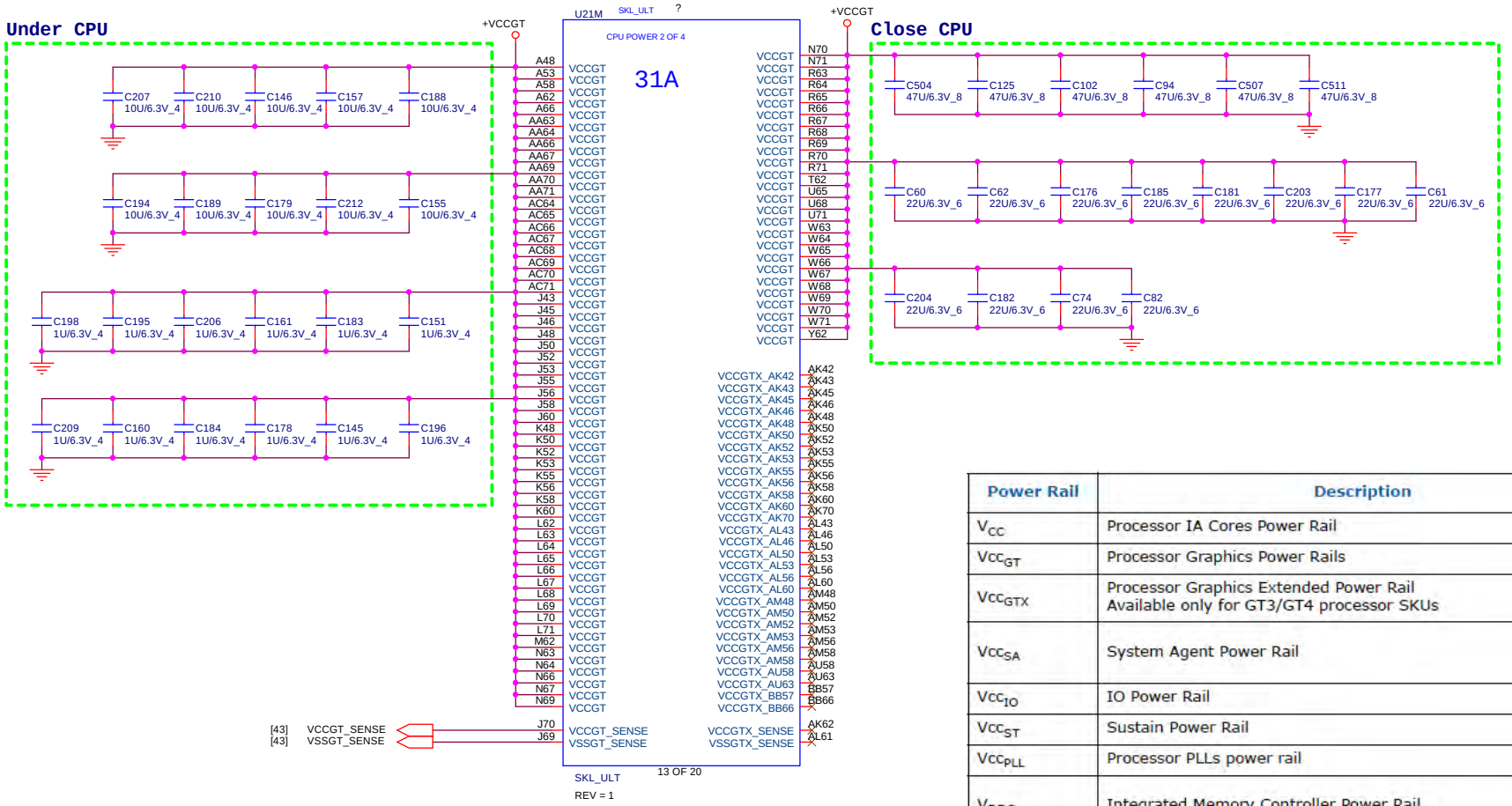
+VCCGT [43,44]



Power Rail	Description	Control
V_{CC}	Processor IA Cores Power Rail	SVID
Vcc_{GT}	Processor Graphics Power Rails	SVID
Vcc_{GTX}	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
Vcc_{SA}	System Agent Power Rail	SVID/Fixed (SKU dependent)
Vcc_{IO}	IO Power Rail	Fixed
Vcc_{ST}	Sustain Power Rail	Fixed
Vcc_{PLL}	Processor PLLs power rail	Fixed
V_{DDQ}	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
Vcc_{OPC}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{OPC_1P8}	Processor OPC power rail (available only in SKU's with OPC)	Fixed
Vcc_{EOPIO}	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

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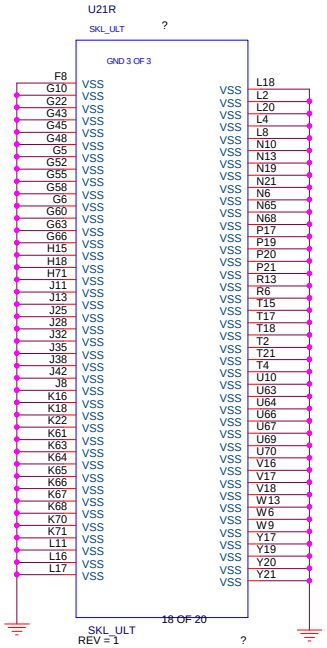

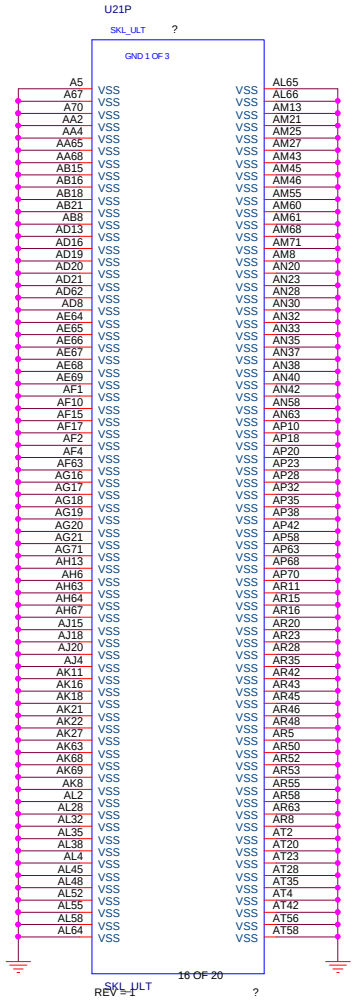

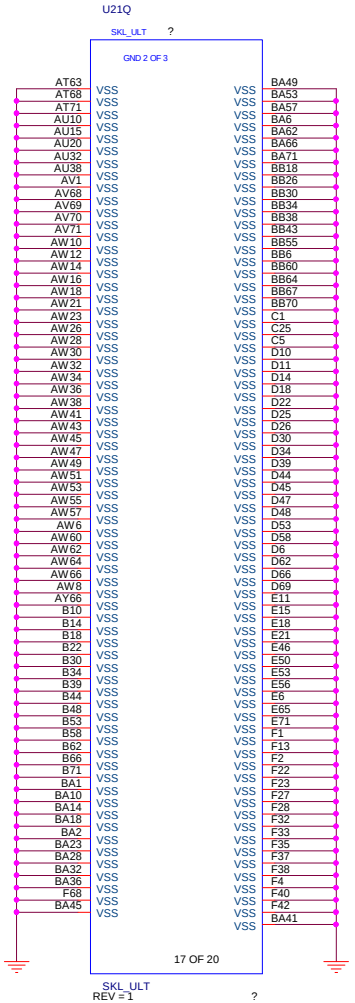

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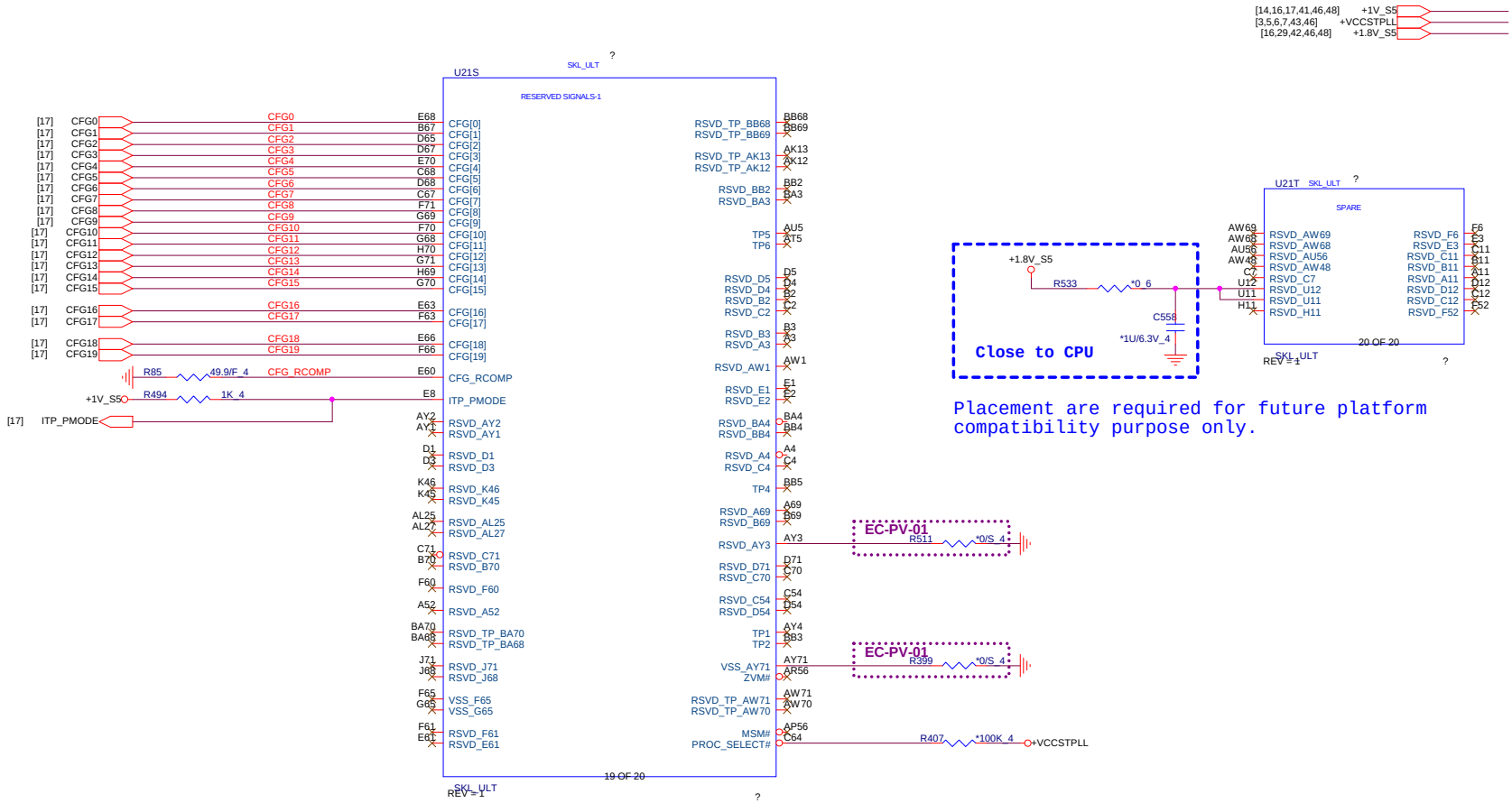

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (Physcial Debug Enable) DFX Privacy	Disable:	Enable: Set DFX Enable in DFX interface MSR	CFG3 R400 *1K_4
CFG4 (DP Presence Strap)	Disable; No physical DP attached to eDP	Enable; An ext DP device is connected to eDP	CFG4 R402 1K_4

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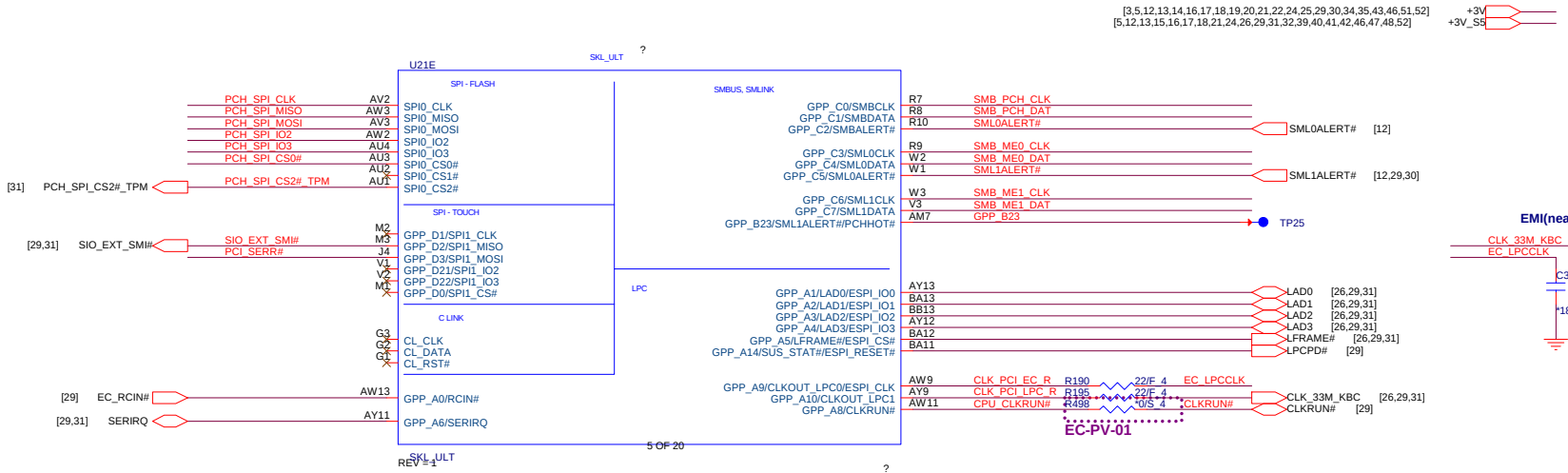
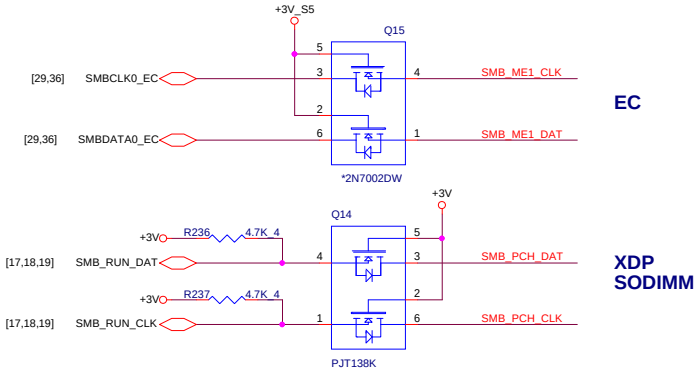
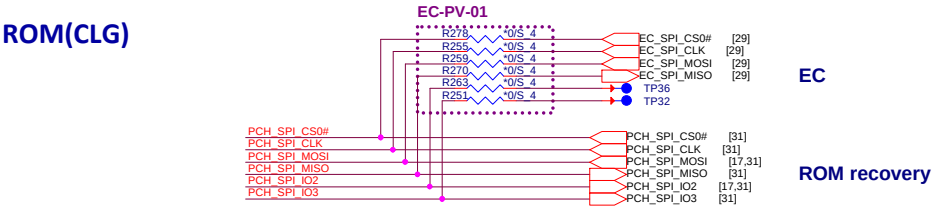


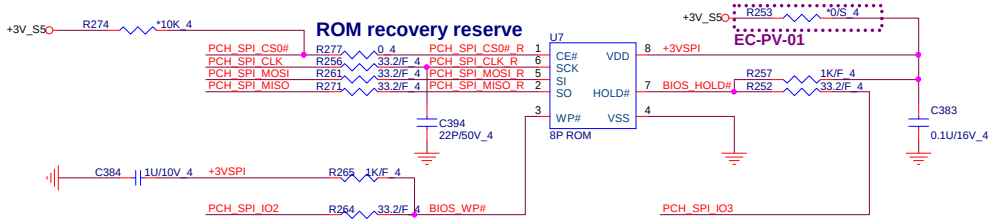
GPIO Pull UP

SMBus/Pull-up(CLG)



PCH SPI ROM(CLG)





Vender	Size	P/N
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GD	8MB	AKE2EZN0Q00 (GD25B64CSIGR)
Socket		DFHS08FS023

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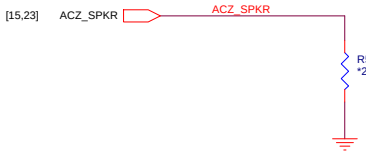
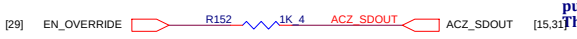
[3,5,11,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

Functional Strap Definitions

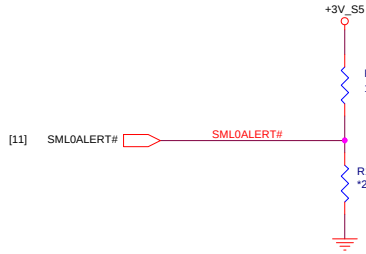
DESIGN NOTE:
WEAK PULL UP RESISTOR PRESENT ON THIS NET



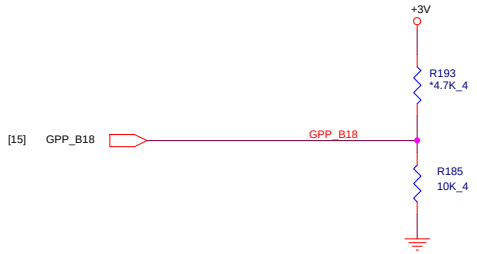
TOP SWAP OVERRIDE
HIGH - TOP SWAP ENABLE
LOW-DISABLED
HIGH: LPC SELECTED FOR SYSTEM FLASH
WEAK INTERNAL PD



No Boot:
The signal has a weak internal pull-down.
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.
This function is useful when running ITP/XDP.



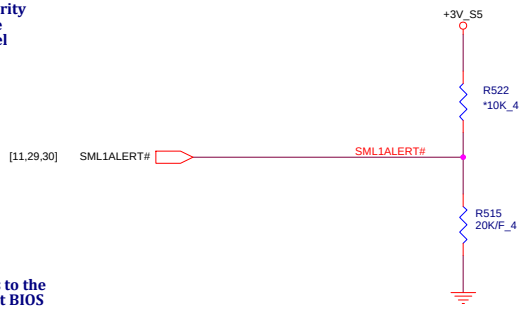
No Boot:
The signal has a weak internal pull-down.
0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality).
1 = Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



No Boot:
The signal has a weak internal pull-down.
0 = Disable No Reboot mode.
1 = Enable No Reboot mode
(PCH will disable the TCO Timer system reboot feature).
This function is useful when running ITP/XDP.

No Boot:
The signal has a weak internal pull-down.
This field determines the destination of accesses to the BIOS memory range. Also controllable using Boot BIOS Destination bit (Chipset Configuration Registers: Offset 3410h:Bit 10). This strap is used in conjunction with Boot BIOS Destination Selection 0 strap.

Bit 10	Boot BIOS Destination
0	SPI
1	LPC



No Boot:
The signal has a weak internal pull-down.
0 = LPC Is selected for EC.
1 = eSPI Is selected for EC.

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PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU Strap	1A

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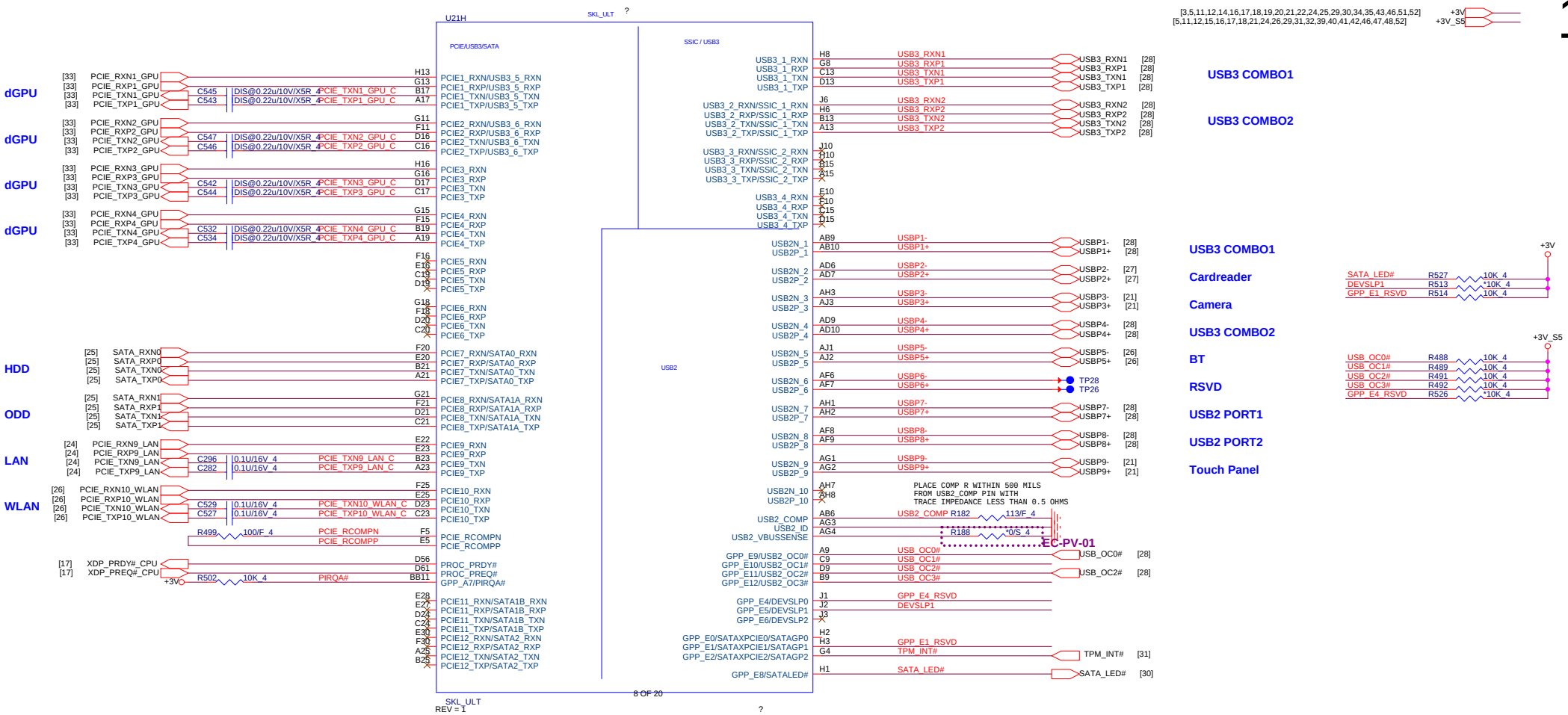

PCI-E Port Mapping Table

PCI-E	Function	CLK REQ	Function
PORT-1	dGPU	PORT-0	dGPU
PORT-2	dGPU	PORT-1	
PORT-3	dGPU	PORT-2	WLAN
PORT-4	dGPU	PORT-3	LAN
PORT-5		PORT-4	
PORT-6		PORT-5	
PORT-7	HDD		
PORT-8	ODD		
PORT-9	LAN		
PORT-10	WLAN		
PORT-11			
PORT-12			

USB3.0 Port Mapping Table

USB3.0	Function
PORT-1	USB3 COMBO1
PORT-2	USB3 COMBO2
PORT-3	NC
PORT-4	NC

USB2.0 Port Mapping Table

USB2.0	Function
PORT-1	USB3 COMBO1
PORT-2	Cardreader
PORT-3	Camera
PORT-4	USB3 COMBO2
PORT-5	BT
PORT-6	NC
PORT-7	USB2 PORT1
PORT-8	USB2 PORT2
PORT-9	Touch Panel
PORT-10	NC

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PROJECT: HP-Hawaii

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[5,16] +3V_RTC_2
[3,5,11,12,13,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,16,17,41,46,48] +1V_S5

U21J SKL_ULT ?

CLOCK SIGNALS

WLAN
LAN

[33] CLK_GFX_N → CLK_GFX_N → D42 CLKOUT_PCIE_N0
[33] CLK_GFX_P → CLK_GFX_P → C42 CLKOUT_PCIE_P0
[33] PCIE_CLKREQ_VGA# → PCIE_CLKREQ_VGA# → AR10 GPP_B5/SRCCLKREQ0#

B42 CLKOUT_PCIE_N1
A42 CLKOUT_PCIE_P1
PCIE_CLKREQ1# → AT7 GPP_B6/SRCCLKREQ1#

[26] CLK_PCIE_WLANN → CLK_PCIE_WLANN → D41 CLKOUT_PCIE_N2
[26] CLK_PCIE_WLANP → CLK_PCIE_WLANP → C41 CLKOUT_PCIE_P2
[26] PCIE_CLKREQ_WLAN# → PCIE_CLKREQ_WLAN# → AT8 GPP_B7/SRCCLKREQ2#

[24] CLK_PCIE_LANN → CLK_PCIE_LANN → D40 CLKOUT_PCIE_N3
[24] CLK_PCIE_LANP → CLK_PCIE_LANP → C40 CLKOUT_PCIE_P3
[24] PCIE_CLKREQ_LAN# → PCIE_CLKREQ_LAN# → AT10 GPP_B8/SRCCLKREQ3#

B40 CLKOUT_PCIE_N4
A40 CLKOUT_PCIE_P4
PCIE_CLKREQ4# → AU8 GPP_B9/SRCCLKREQ4#

E40 CLKOUT_PCIE_N5
E39 CLKOUT_PCIE_P5
PCIE_CLKREQ5# → AU7 GPP_B10/SRCCLKREQ5#

10 OF 20
SKL_ULT REV = 1

CLKOUT_ITPXDP_N → F43 CK_XDP_N_R → 4 *0_4P2R_4 3 → CK_XDP_N [17]
CLKOUT_ITPXDP_P → E43 CK_XDP_P_R → 2 1 → CK_XDP_P [17]

RP1 install for XDP

GPD8/SUSCLK → BA17 PCH_SUSCLK → TP59

XTAL24_IN → E37 XTAL24_IN
XTAL24_OUT → E35 XTAL24_OUT → +1V_S5

XCLK_BIASREF → E42 XCLK_BIASREF → R461 2.7K/F_4 → R462 *60.4/F_4

Co-lay 60ohm 1% to GND for Cannonlake use

RTCX1 → AM18 RTC_X1
RTCX2 → AM20 RTC_X2

SRTCRST# → AN18 SRTC_RST#
RTCRST# → AM16 RTC_RST# → RTC_RST# [17]

CLK_REQ/Strap Pin(CLG)

+3V
10K_4 R212 PCIE_CLKREQ4#
10K_4 R197 PCIE_CLKREQ_WLAN#
10K_4 R196 PCIE_CLKREQ_LAN#
10K_4 R211 PCIE_CLKREQ1#
10K_4 R210 PCIE_CLKREQ5#
10K_4 R213 PCIE_CLKREQ_VGA#

U21I SKL_ULT ?

CSI-2

A36 CSI2_DN0
B36 CSI2_DP0
C36 CSI2_DN1
D36 CSI2_DP1
C35 CSI2_DN2
D35 CSI2_DP2
A35 CSI2_DN3
B35 CSI2_DP3

C31 CSI2_DN4
D31 CSI2_DP4
C33 CSI2_DN5
D33 CSI2_DP5
A31 CSI2_DN6
B31 CSI2_DP6
A33 CSI2_DN7
B33 CSI2_DP7

A29 CSI2_DN8
B29 CSI2_DP8
C28 CSI2_DN9
D28 CSI2_DP9
A27 CSI2_DN10
B27 CSI2_DP10
C27 CSI2_DN11
D27 CSI2_DP11

CSI2_CLKN0 → C37
CSI2_CLKP0 → D37
CSI2_CLKN1 → C32
CSI2_CLKP1 → D32
CSI2_CLKN2 → C29
CSI2_CLKP2 → D29
CSI2_CLKN3 → B26
CSI2_CLKP3 → A26

CSI2_COMP → E13 CSI2_RCOMP → R165 100/F_4
GPP_D4/FLASHTRIG → B7 GPP_D4 → TP61

EMMC

GPP_F13/EMMC_DATA0 → AP2
GPP_F14/EMMC_DATA1 → AP1
GPP_F15/EMMC_DATA2 → AP3
GPP_F16/EMMC_DATA3 → AN3
GPP_F17/EMMC_DATA4 → AN1
GPP_F18/EMMC_DATA5 → AN2
GPP_F19/EMMC_DATA6 → AM4
GPP_F20/EMMC_DATA7 → AM1

GPP_F21/EMMC_RCLK → AM2
GPP_F22/EMMC_CLK → AM3
GPP_F12/EMMC_CMD → AP4

EMMC_RCOMP → AT1 EMMC_RCOMP → R184 200/F_4

9 OF 20
SKL_ULT REV = 1

RTC Clock 32.768KHz

EC-SI-12

C355 12P/50V_4 — Y3 32.768KHz — C356 12P/50V_4
RTC_X1 — R224 10M_4 — RTC_X2

External Crystal

EC-SI-12

C360 12P/50V_4
XTAL24_IN — R130 1M_4 — 24MHZ +-30PPM Y2 — XTAL24_OUT
C273 12P/50V_4

RTC Circuitry(RTC)

RTC Power trace width 20mils.

+3V_ALW → R554 1.5K_4
+3V_RTC_2
+3V_RTC_0

R555 45.3K_4 — D18 RB500V-40
R553 1K_4 +3V_RTC_1 — D17 RB500V-40

R567 20K/F_4 → RTC_RST#
R566 20K/F_4 → SRTC_RST#

C589 1U/6.3V_4
C590 *220P/50V_4
C581 1U/6.3V_4
C588 1U/6.3V_4

CN20 CONNDIPHOUSING2P

RTC_RST# → Q35 2N7002K → EC_RTC_RST → EC_RTC_RST [29]
R561 10K_4

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Size	Document Number	Rev
Custom	SKL CPU CLK/eMMC	1A

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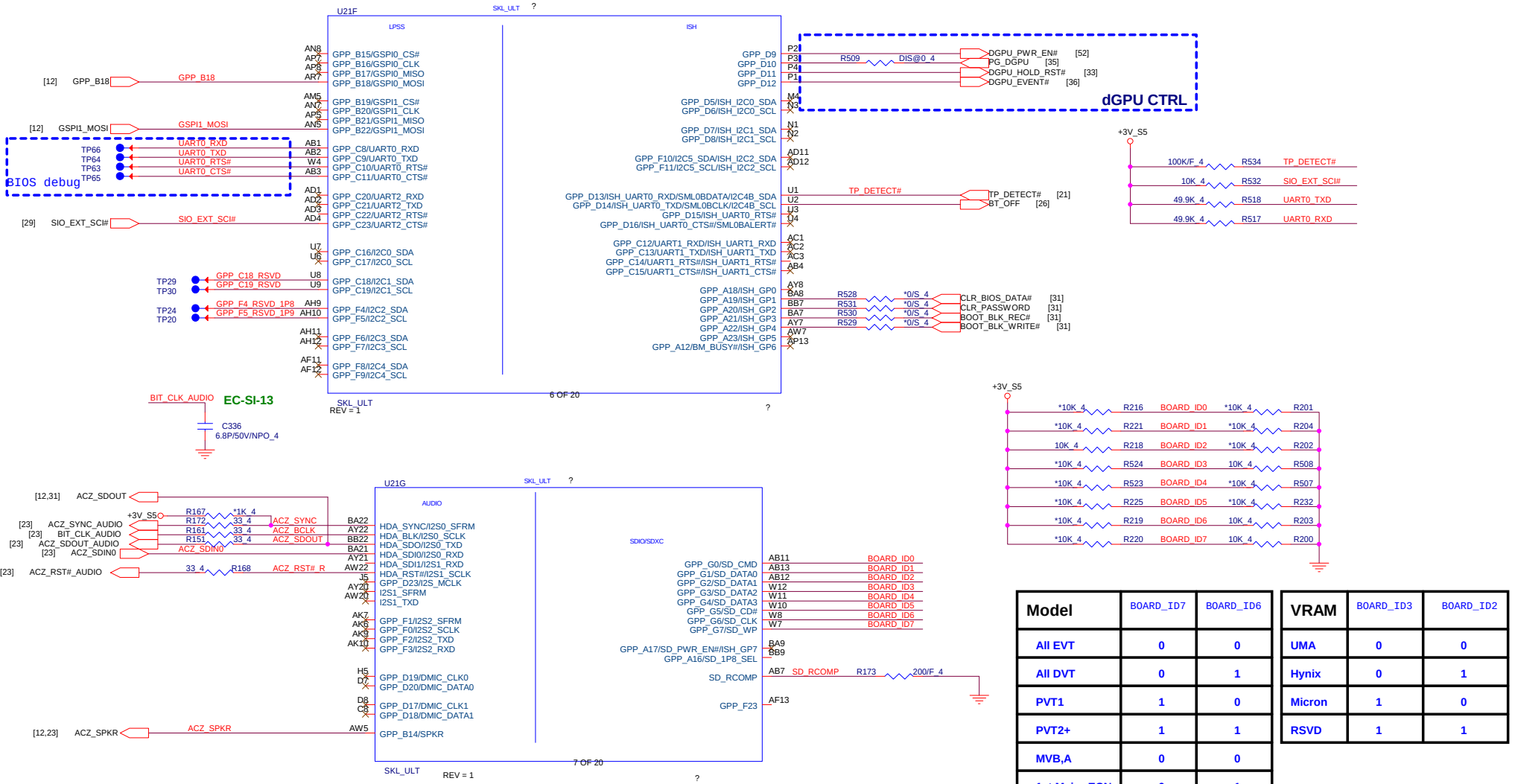
[5,11,12,13,16,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52]
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52]
+3V_S5
+3V



Model	BOARD_ID7	BOARD_ID6
All EVT	0	0
All DVT	0	1
PVT1	1	0
PVT2+	1	1
MVB,A	0	0
1st Major ECN	0	1
2nd Major ECN	1	0
3rd Major ECN	1	1

VRAM	BOARD_ID3	BOARD_ID2
UMA	0	0
Hynix	0	1
Micron	1	0
RSVD	1	1

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PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU HDA/GPIO	1A

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[10,14,17,41,46,48] +1V_S5
[10,29,42,46,48] +1.8V_S5
[5,11,12,13,15,17,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5
[5,14] +3V_RTC_2
[3,5,11,12,13,14,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V

U21O
SKL_ULT
CPU POWER 4 OF 4

VCCPRIM_1P0 AB19, AB20, P18 — 2.899A
VCCPRIM_CORE AF18, AF19, V20, V21 — 2.57A
DCPDSW_1P0 AL1
VCCMPHYAON_1P0 K17, L1
VCCMPHYGT_1P0_N15 N15, N16, N17 — 1.714A
VCCMPHYGT_1P0_P15 P15, P16
VCCAMPHYPLL_1P0 K15, L15
VCCAPLL_1P0 V15 — 0.03A
VCCPRIM_1P0_AB17 AB17, Y18
VCCDSW_3P3_AD17 AD17, AD18 — 0.09A
VCCDSW_3P3_AJ17 AJ17
VCCHDA AJ19
VCCSPI AJ16
VCCSRAM_1P0 AF20, AF21, T19, T20
VCCPRIM_3P3_AJ21 AJ21
VCCPRIM_1P0_AK20 AK20
VCCAPLLEBB N18

VCCPGPPA AK15 +VCCPGPPA
VCCPGPPB AG15 +VCCPGPPB
VCCPGPPC Y16 +VCCPGPPC
VCCPGPPD Y15 +VCCPGPPD
VCCPGPPE T16 +VCCPGPPE
VCCPGPPF AF16 +VCCPGPPF
VCCPGPPG AD15 +VCCPGPPG
VCCPRIM_3P3_V19 V19
VCCPRIM_1P0_T1 T1 +VCCPRIM_1.0V_T1
VCCATS_1P8 AA1 +VCCATS_1.8V
VCCRTCPRIM_3P3 AK17 +VCCRTCPRIM_3.3V
VCCRTC_AK19 AK19 +VCCRTC
VCCRTC_BB14 BB14
DCPRTC BB10 DCPRTC
VCCCLK1 A14 +VCCCLK1
VCCCLK2 K19 +VCCCLK2
VCCCLK3 L21 +VCCCLK3
VCCCLK4 N20 +VCCCLK4
VCCCLK5 L19 +VCCCLK5
VCCCLK6 A10 +VCCCLK6
GPP_B0/CORE_VID0 AN11 CORE_VID0
GPP_B1/CORE_VID1 AN13 CORE_VID1

SKL_ULT
REV = 1
15 OF 20

+VCCPRIM: C335 1U/6.3V_4; C316 1U/6.3V_4
+1V_S5: C316 1U/6.3V_4; R174 *0/S_6; C318 1U/6.3V_4; C338 1U/6.3V_4; C348 47U/6.3V_8; R163 *0/S_6; C341 1U/6.3V_4; R155 *0/S_6; R148 *0/S_6; C337 1U/6.3V_4; R247 *0/S_6; R146 *0/S_6; C322 1U/6.3V_4; R169 *0/S_6; R150 *0/S_6; R154 *0/S_6; C333 1U/6.3V_4
+VCCDSW_1.0V: C556 1U/6.3V_4
+VCCMPHYAON_1P0: R174 *0/S_6; C318 1U/6.3V_4
+VCCAMPHYPLL_1P0: R163 *0/S_6; C341 1U/6.3V_4
+VCCAPLL_1.0V: R155 *0/S_6
+VCCPRIM: R148 *0/S_6; C337 1U/6.3V_4
+3V_S5: R214 *0/S_4; C342 0.1U/10V_4; C324 0.1U/10V_4; R247 *0/S_6; R169 *0/S_6
+V3.3DX_1.5DX_ADO: L17 120/2A_6
+3V_ALW: R246 *0_6
+VCCSPI: R247 *0/S_6
+VCCSRAM_1.0V: R146 *0/S_6; C322 1U/6.3V_4
+VCCPRIM_3.3V: R169 *0/S_6
+VCCPRIM_1.0V: R150 *0/S_6
+VCCAPLLEBB: R154 *0/S_6; C333 1U/6.3V_4

EC-PV-01
RF

+3V_S5: C345 1U/6.3V_4; R179 *0/S_6
+1V_S5: R501 *0/S_6; R482 *0/S_6; R166 *0/S_6; R158 *0/S_6; R175 *0/S_6; R171 *0/S_6; R486 *0/S_6
+1.8V_S5: R520 *0/S_6
+3V_RTC_2: R178 *0/S_4
DCPRTC: C555 0.1U/16V_4
+VCCRTCPRIM_3.3V: R248 *0/S_6
+VCCCLK6: C550 1U/6.3V_4
CORE_VID0: TP21
CORE_VID1: TP19

20mils

+V3.3DX_1.5DX_ADO: EC-PV-01 R176 *0/S_4 +3V
+1V_S5: C548 *1U/6.3V_4; C551 *22U/6.3V_6
+3V_S5: EC-PV-01 R198 *0/S_6 (+VCCPGPPA); R226 *0/S_6 (+VCCPGPPB); R249 *0/S_6 (+VCCPGPPC); R250 *0/S_6 (+VCCPGPPD); R194 *0/S_6 (+VCCPGPPE); R215 *0/S_6 (+VCCPGPPG)
+1.8V_S5: R519 *0/S_6 (+VCCPGPPF)
+VCCATS_1.8V: C557 1U/6.3V_4
+VCCRTC: C343 0.1U/16V_4; C344 1U/6.3V_4
+VCCRTCPRIM_3.3V: C363 1U/6.3V_4; C364 0.1U/16V_4
+VCCPGPPB: C354 *1U/6.3V_4
+VCCPGPPC: C365 *1U/6.3V_4
+VCCPGPPE: C349 1U/6.3V_4

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Custom	SKL CPU Power (PCH)	1A
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[3,5,11,12,13,14,16,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[10,14,16,41,46,48] +1V_S5
[3,5,7,46,48] +VCCIO
[5,11,12,13,15,16,18,21,24,26,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

CPU XDP

CN1 *Samtec BSH-030-01

EC-PV-01

*0_4 R70 CFG3 1K_4 R69
[10] CFG3
[13] XDP_PREQ#_CPU
[13] XDP_PRDY#_CPU
[10] CFG0
[10] CFG1
[10] CFG2
TP44
CFG0 R78 1K_4 CFG1 CFG2 CFG3
[3] XDP_BPM0
[3] XDP_BPM1
[10] CFG4
[10] CFG5
[10] CFG6
[10] CFG7
[5,29] RSMRST#
[5,29] DNBSWON#
1K_4 R67
+1V_S5
CFG0 R65 *0/S_4 PWR_DEBUG
HOOK3
[11,18,19] SMB_RUN_DAT
[11,18,19] SMB_RUN_CLK
R57 *0/S_4 SMB_RUN_DAT_XDP
R54 *0/S_4 SMB_RUN_CLK_XDP
XDP_TCK1
XDP_TCK0
[3] XDP_TCK0

1	XDP_PRESENT#	GND1	60
2	PROC_PREQ#	OBSFN_C0	59
3	OBSFN_A1	OBSFN_C1	58
4	GND2	GND3	57
5	OBSDATA_A0	OBSDATA_C0	56
6	OBSDATA_A1	OBSDATA_C1	55
7	GND4	GND5	54
8	OBSDATA_A2	OBSDATA_C2	53
9	OBSDATA_A3	OBSDATA_C3	52
10	GND6	GND7	51
11	OBSFN_B0	OBSFN_D0	50
12	OBSFN_B1	OBSFN_D1	49
13	GND8	GND9	48
14	OBSDATA_B0	OBSDATA_D0	47
15	OBSDATA_B1	OBSDATA_D1	46
16	GND10	GND11	45
17	OBSDATA_B2	OBSDATA_D2	44
18	OBSDATA_B3	OBSDATA_D3	43
19	GND12	GND13	42
20	HOOK0	ITPCLK/HOOK4	41
21	HOOK1	ITPCLK#/HOOK5	40
22	VCC_OBS_AB	VCC_OBS_CD	39
23	HOOK2	HOOK6/RESET#	38
24	HOOK3	HOOK7/DBR#	37
25	GND14	GND15	36
26	XDP_SDA	XDP_TDO	35
27	XDP_SCL	XDP_TRSTn	34
28	XDP_TCK1	XDP_TDI	33
29	XDP_TCK0	XDP_TMS	32
30	GND16	GND(XDP_PRESENT#)	31

CFG17 CFG16 CFG8 CFG9 CFG10 CFG11 CFG19 CFG18 CFG12 CFG13 CFG14 CFG15
ITP_PMODE SYS_RESET# XDP_TDO XDP_TRST# XDP_TDI XDP_TMS XDP_PRS

CFG17 [10] CFG16 [10] CFG8 [10] CFG9 [10] CFG10 [10] CFG11 [10] CFG19 [10] CFG18 [10] CFG12 [10] CFG13 [10] CFG14 [10] CFG15 [10]
CK_XDP_P [14] CK_XDP_N [14] +1V_S5 ITP_PMODE [10] TP2

XDP_PRS R52 *0/S_4 R53 *0_4 PCH_SPI_IO2 [11,31]
EC-PV-01

[11,31] PCH_SPI_MOSI R61 *0_4 HOOK3 R62 *1K_4 +3V_S5

+3V *1K_4 R59 SYS_RESET#
C85 *0.1U/16V_4

+VCCIO
R398 150/F_4
PWR_DEBUG
R64 *10K_4

+1V_S5
C99 0.1U/16V_4
C97 0.1U/16V_4

APS

CN2 *50501-0180N-001

EC-PV-01 R205 *0/S_4
+3V_S5
SUSB# [5,29]
SLP_S5# [5,29]
SUSC# [5,29]
SLP_A# [5]
RTC_RST# [14]
DNBSWON#
SYS_RESET# [5]
R199 *0_4_S PM_SLP_S0# [5,29]

C515 0.1U/16V_4
+3V R463 *0_4_S XDP_TDO
[5,29] HWPG
XDP_TDI
XDP_TMS
XDP_TRST#

U19 *SN74CBTLV3126RGYR

14	VCC		
2	1A	1B	3
1	1OE		
5	2A	2B	6
4	2OE		
9	3A	3B	8
10	3OE		
12	4A	4B	11
13	4OE		
	DPAD		15
	GND		7

XDP_TDO_CPU [3] XDP_TDI_CPU [3] XDP_TMS_CPU [3] XDP_TRST#_CPU [3]

[3] JTAGX_PCH
[3] JTAG_TMS_PCH
[3] JTAG_TDI_PCH
[3] JTAG_TDO_PCH
[3] JTAG_TCK_PCH

+VCCIO R450 51_4
R449 *0_4 XDP_TDO
XDP_TCK0
XDP_TMS
XDP_TDI
XDP_TDO
R446 *0_4 XDP_TDI
R445 *0_4 XDP_TCK0
XDP_TCK1

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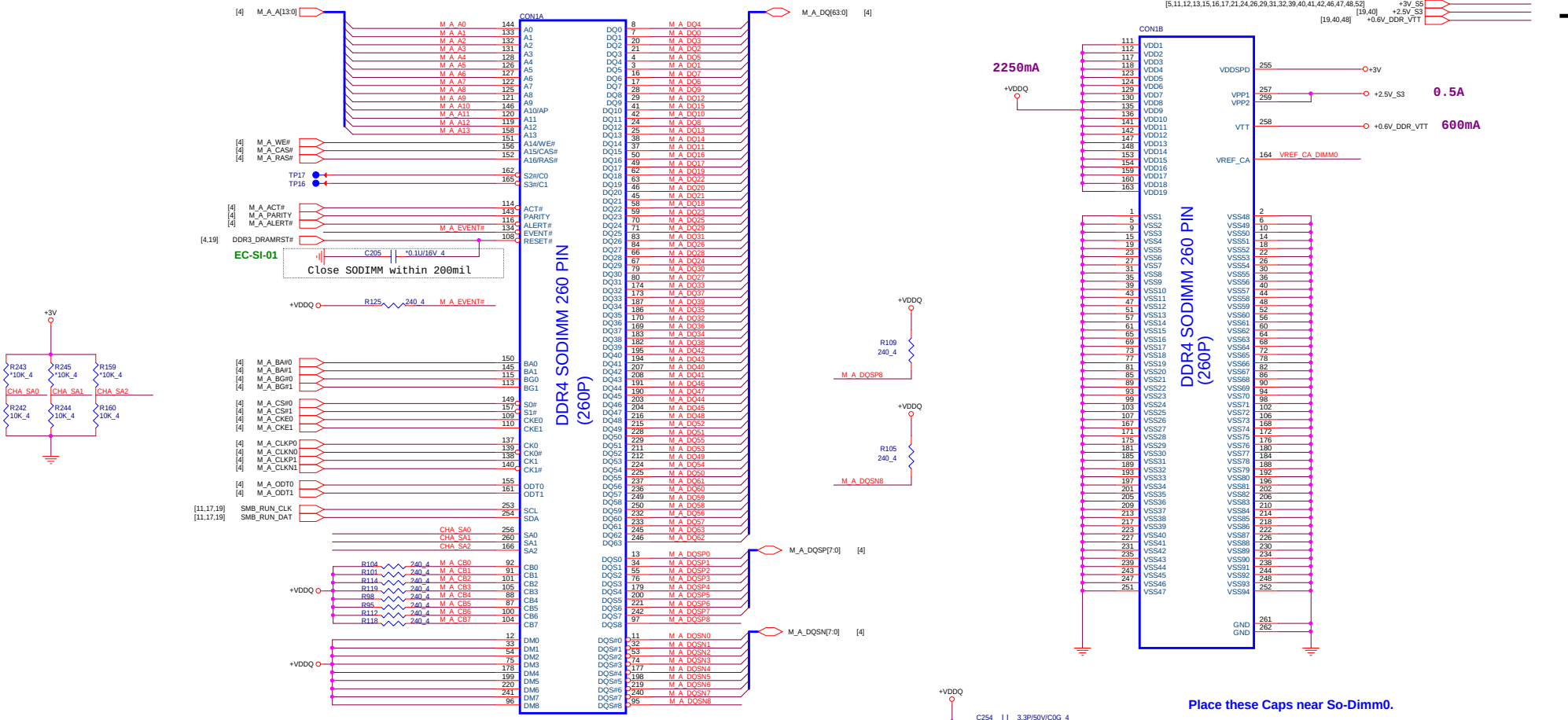
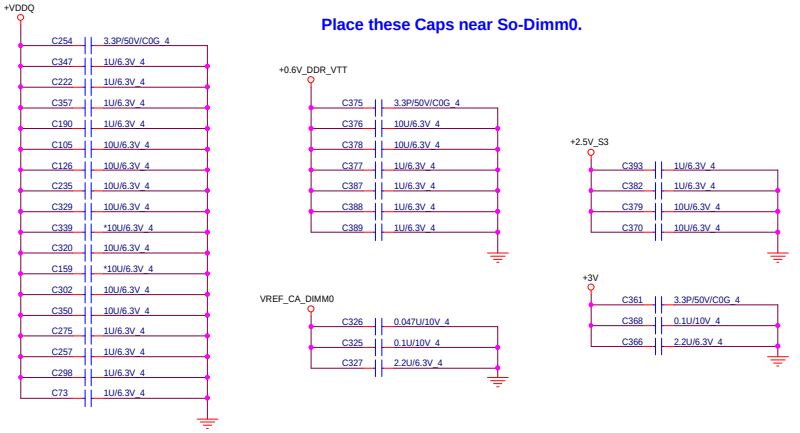
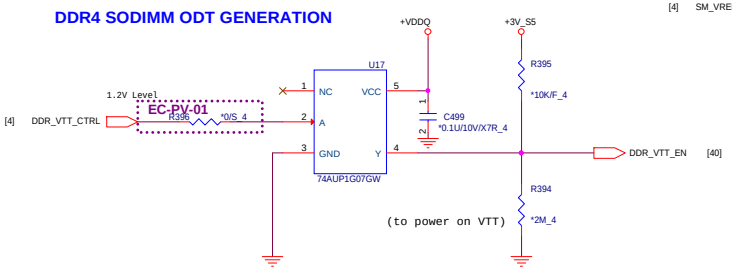
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SKL CPU XDP/APS	1A
Date: Wednesday, March 09, 2016	Sheet 17 of 58	

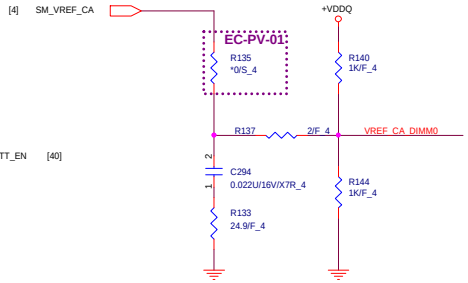




DDR4 SODIMM ODT GENERATION



VREF CA DIMM0 Solution

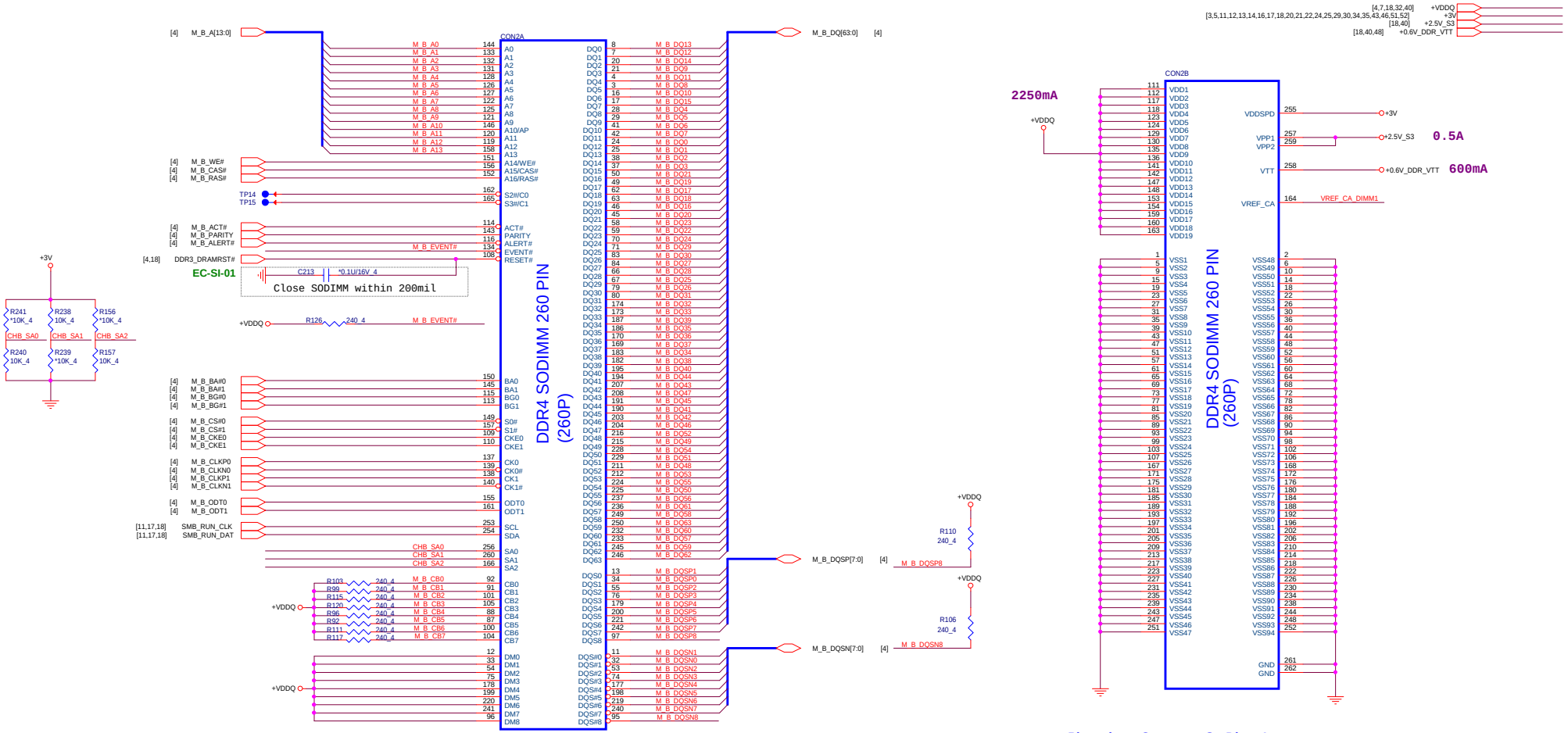


Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DDR4 SODIMM H=8	1A

Date: Tuesday, February 02, 2016 Sheet 18 of 58


CON2A
DDR4 SODIMM 260 PIN
(260P)
EC-SI-01
Close SODIMM within 200mil
CON2B
2250mA
0.5A
600mA
VREF_CA_DIMM1
Place these Caps near So-Dimm1
VREF CA DIMM1 Solution
EC-PV-01
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
DDR4 SODIMM H=4

eDP to LVDS (RTD2136N-CG)

[3,5,11,12,13,14,16,17,18,19,21,22,24,25,29,30,34,35,43,46,51,52] +3V

Trace width of DVCC33 >40mils

+3V — L13 PBY160808T-600Y-N — DVCC33
C25 10U/6.3V/X5R_6
C18 0.1U/10V/X5R_4

DP input signals

[3] EDP_HPD — R26 1K/F_4
R31 *100K/F_4
eDP_HPD with pull down 100K-ohm on PCH side.

[3] INT_EDP_AUXN — C473 0.1U/10V/X5R_4
[3] INT_EDP_AUXP — C472 0.1U/10V/X5R_4
[3] INT_EDP_TXP0 — C471 0.1U/10V/X5R_4
[3] INT_EDP_TXN0 — C470 0.1U/10V/X5R_4
[3] INT_EDP_TXP1 — C469 0.1U/10V/X5R_4
[3] INT_EDP_TXN1 — C468 0.1U/10V/X5R_4

+3V — L14 PBY160808T-600Y-N — AVCC33
C38 10U/6.3V/X5R_6
C33 0.1U/10V/X5R_4
C32 0.1U/10V/X5R_4 CLOSE to PIN5

SWR_V12 — C23 0.1U/10V/X5R_4 CLOSE to PIN43
2136_BKLT_EN
EDID_DAT
EDID_CLK
SDA
SCL

C31 0.1U/10V/X5R_4 CLOSE to PIN11
R387 12K/F_6

U15 RTD2136N-CG(QFN)

RTD2136N

1	eDP_HPD_R	DP_HPD	
2	TEST_MODE	TEST_MODE	
3	2136_AUXN	AUX-CH_N	
4	2136_AUXP	AUX-CH_P	
5	AVCC33	DP_V33	
6		DP_GND	
7	DPD_TXP0_C	LANE0P	
8	DPD_TXN0_C	LANE0N	
9	DPD_TXP1_C	LANE1P	
10	DPD_TXN1_C	LANE1N	
11	SWR_V12	DP_V12	
12	DP_REXT	DP_REXT	
13	CIICSCL1		
14	CIICSDA1		
15	SWR_VCCK		
16	SWR_LX		
17	SWR_VDD		
18	GPIO/PWM0UT		
19	GPIO/PWM1		
20	GPIO/PWM1N		
21	PVCC		
22	TXE3+		
23	TXE3-		
24			
25		TXEC+	
26		TXEC-	
27		TXE2+	
28		TXE2-	
29		TXE1+	
30		TXE1-	
31		TXE0+	
32		TXE0-	
33		TXO3+	
34		TXO3-	
35		TXOC+	
36		TXOC-	
37	TXO2+		
38	TXO2-		
39	TXO1+		
40	TXO1-		
41	TXO0+		
42	TXO0-		
43	VCCK		
44	MICSCL1		
45	MICSDA1		
46	MICSCL0		
47	MICSDA0		
48	EPD		
49			

GPIO/PWM0/PWM0UT

ODD_CH
LVDS_TX_ON0 [21]
LVDS_TX_OP0 [21]
LVDS_TX_ON1 [21]
LVDS_TX_OP1 [21]
LVDS_TX_ON2 [21]
LVDS_TX_OP2 [21]
LVDS_TXCLK_ON [21]
LVDS_TXCLK_OP [21]
LVDS_TX_ON3 [21]
LVDS_TX_OP3 [21]

EVEN_CH
LVDS_TX_EN0 [21]
LVDS_TX_EP0 [21]
LVDS_TX_EN1 [21]
LVDS_TX_EP1 [21]
LVDS_TX_EN2 [21]
LVDS_TX_EP2 [21]
LVDS_TXCLK_EN [21]
LVDS_TXCLK_EP [21]
LVDS_TX_EN3 [21]
LVDS_TX_EP3 [21]

ISP_SCL
ISP_SDA
SWR_V12

PCH_DPST_PWM
2136_LVDS_PWREN
2136_VADJ

DVCC33 — C22 0.1U/10V/X5R_4 CLOSE to PIN22

Trace width of SWR_V12 and SWR_LX >60mils
L9/C536/C113 close to Pin17 within 200mils
SWR_V12 — L12 *0/S_8_SWR_LX
C27 0.1U/10V/X5R_4
C29 22U/6.3V/X5R_6

Trace width of DVCC33 >40mils
DVCC33
C21 0.1U/10V/X5R_4
C14 22U/6.3V/X5R_6

C5023/C5024 close to Pin18 within 200mils

SWR MODE /LDO MODE

	4.7-uH	0 Olm
SWR_182mW	Connect	NC
LDO_357mW	NC	Connect

GPIO & TESTing signals

TEST_MODE
[50] 2136_VADJ
[21] 2136_LVDS_PWREN
[21] 2136_BKLT_EN
[3] PCH_DPST_PWM
R386 100K/F_4
R365 100K/F_4
2136_VADJ
C465 100P/50V/NPO_4
R368 100K/F_4

In System Programing

slave address=0xA8

DVCC33 — R381 4.7K/F_4 — R373 4.7K/F_4
[29] LVDS_SCL — EC-PV-01 R379 *0/S_4 — ISP_SCL
[29] LVDS_SDA — R372 *0/S_4 — ISP_SDA

RTD2136N: Mode Selestion		MODE_CFG0 (PIN47)	
		0	1
MODE_CFG1(PIN48)	0	X	EP MODE
	1	ROM ONLY MODE	EEPROM MODE

Program EEPROM (F/W.EDID)

slave address=0xA8

DVCC33 — R384 *4.7K/F_4 — SCL
DVCC33 — R385 4.7K/F_4 — SDA
MODE_CFG1(PIN48) MODE_CFG0 (PIN47)

DVCC33 — C475 *0.1U/10V/X5R_4
Pin_45 EDID_DAT — EC-PV-01 R371 *0/S_4 — FW_ROM_SDA
Pin_46 EDID_CLK — R378 *0/S_4 — FW_ROM_SCL
U16 *M24C64: VCC WP SDA A2 SCL A1 GND A0

The Program EEPROM must be 2 byte addressing device

DDC

DVCC33 — R377 4.7K/F_4
DVCC33 — R370 *4.7K/F_4
Pin_46 EDID_CLK
Pin_45 EDID_DAT
R376 *4.7K/F_4
R369 4.7K/F_4
SCL — R383 4.7K/F_4

Reserve pull down for EPMODE

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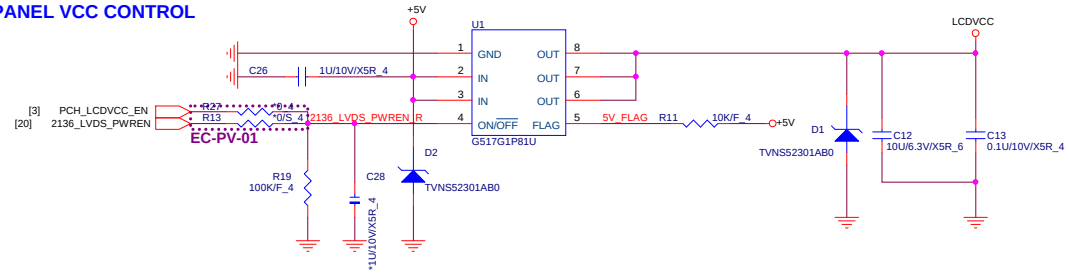
Quanta Computer Inc.
PROJECT: HP-Hawaii

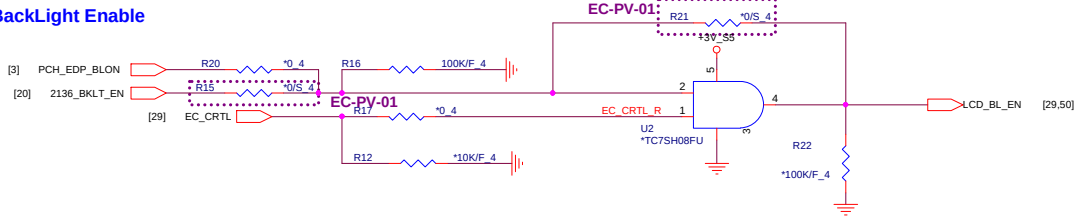
Size	Document Number	Rev
Custom	eDP to LVDS converter	1A

Date: Thursday, January 28, 2016 Sheet 20 of 58

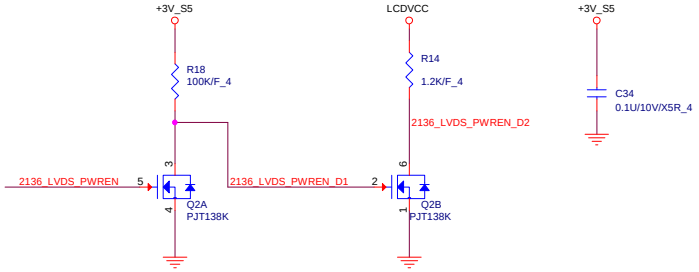
PANEL VCC CONTROL



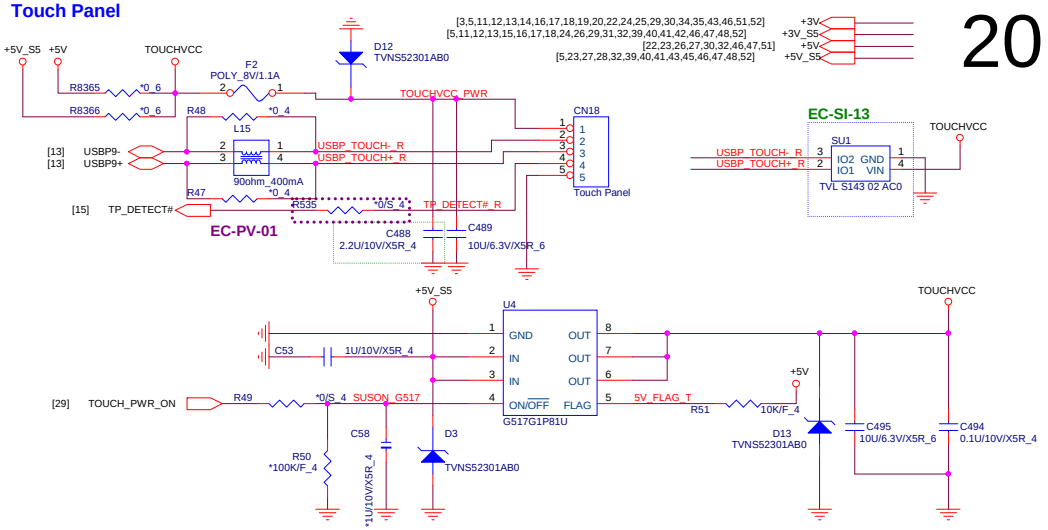
BackLight Enable



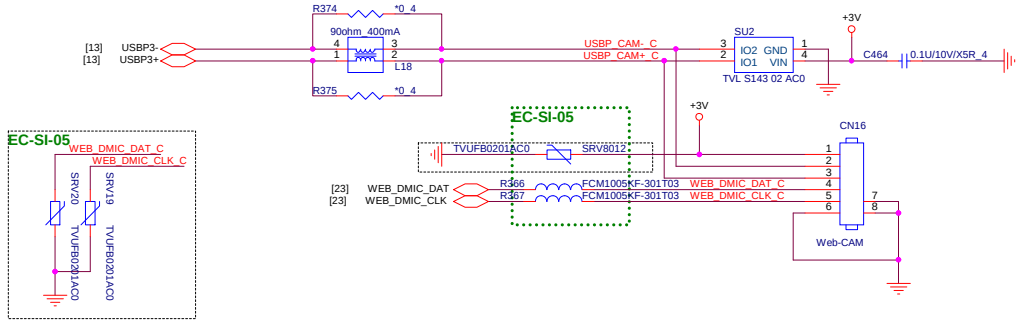
LCDVCC Discharge Circuit

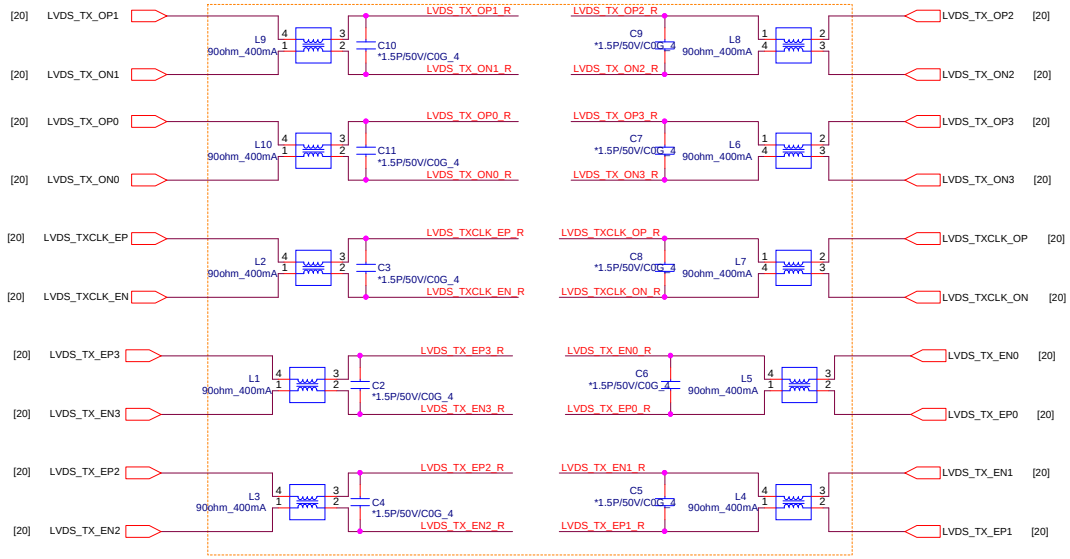


Touch Panel

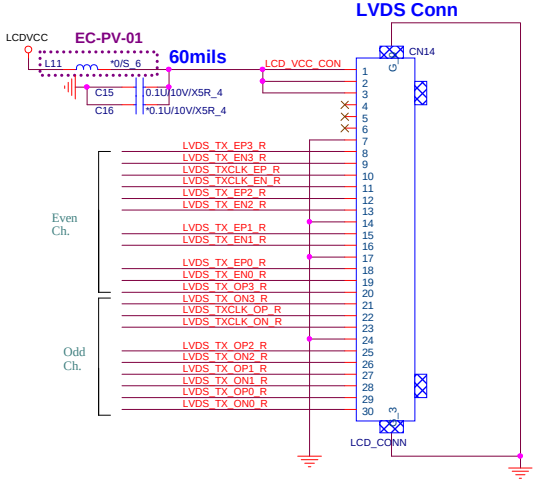


CCD CONN





LVDS Conn



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Quanta Computer Inc.

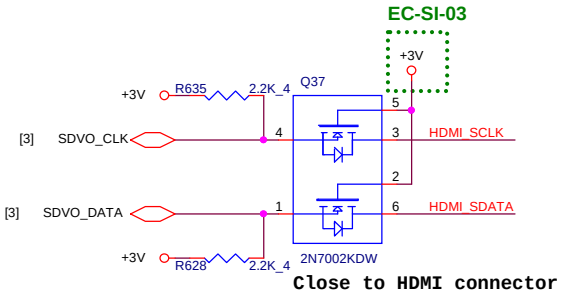
PROJECT: HP-Hawaii

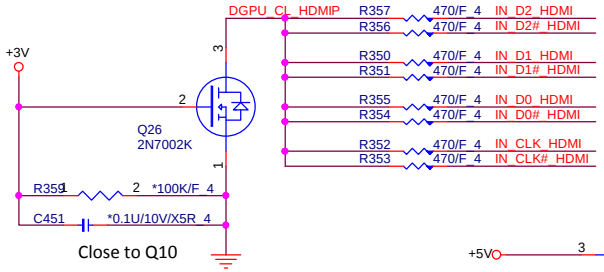
Size	Document Number	Rev
Custom	LVDS CONN/DDC/Touch Panel	1A
Date: Thursday, March 17, 2016	Sheet 21 of 58	

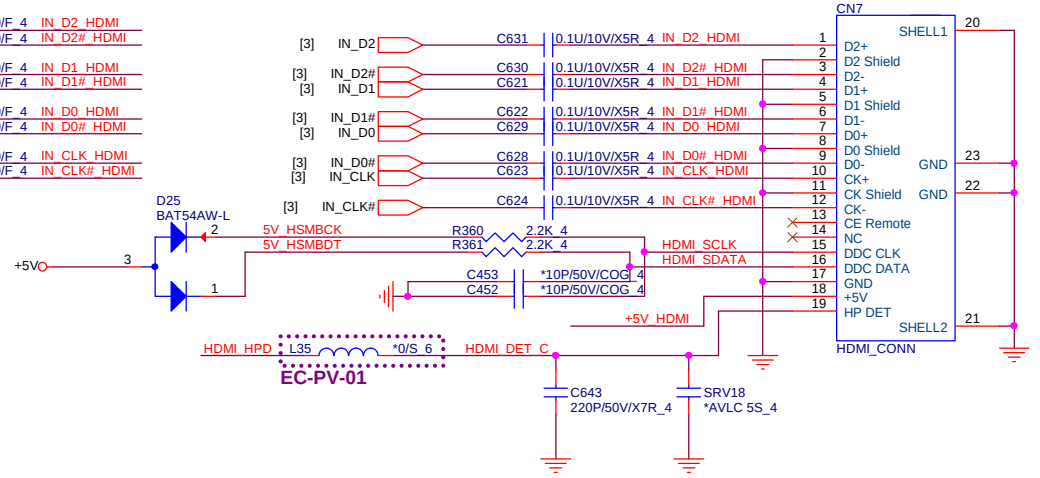
HDMI CONN

[3,5,11,12,13,14,16,17,18,19,20,21,24,25,29,30,34,35,43,46,51,52]
[21,23,26,27,30,32,46,47,51]
+3V
+5V

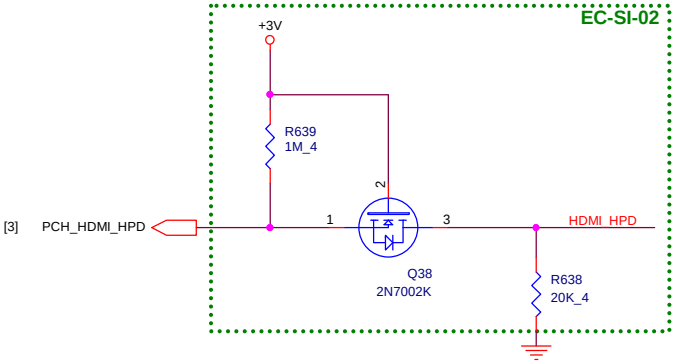
EC-SI-03



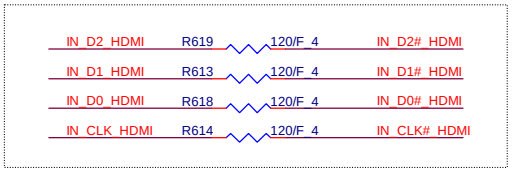


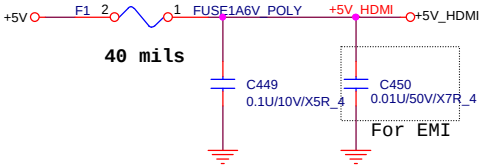


EC-SI-02

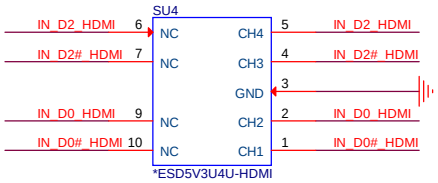


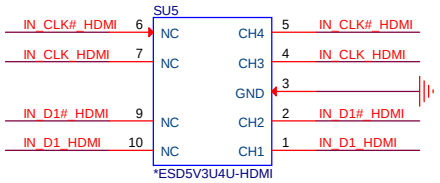
For EMI

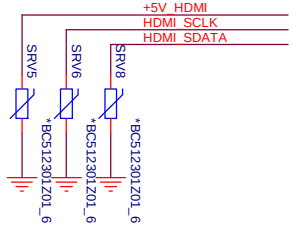




For ESD







Layout note:Place close to HDMI Conn

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Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	HDMI	1A

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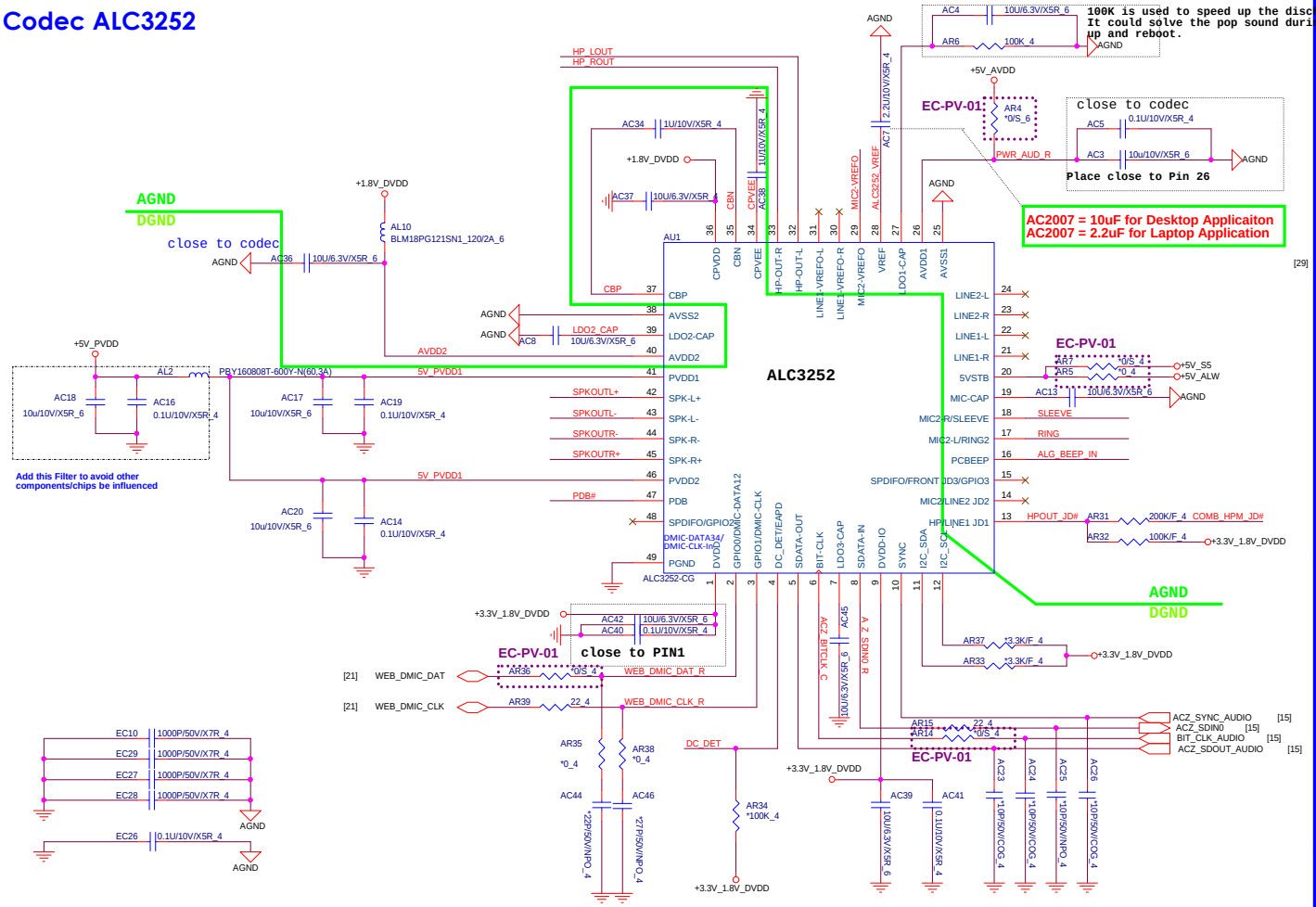
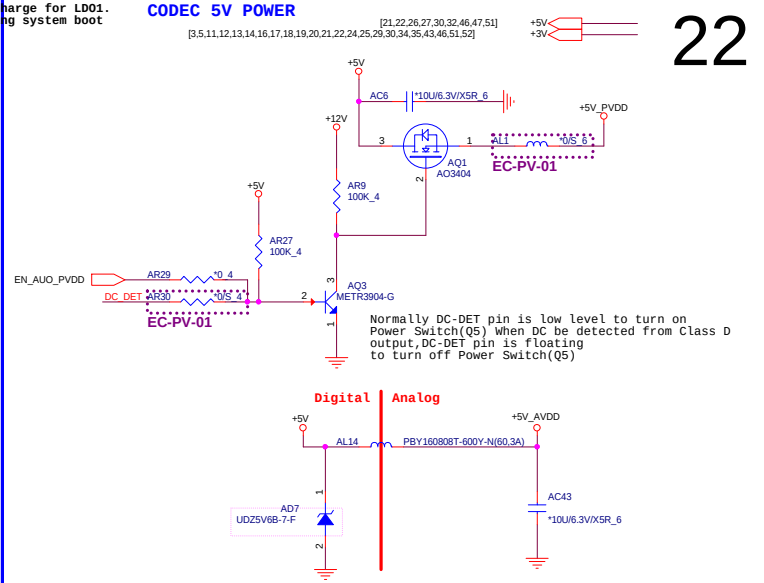
Codec ALC3252

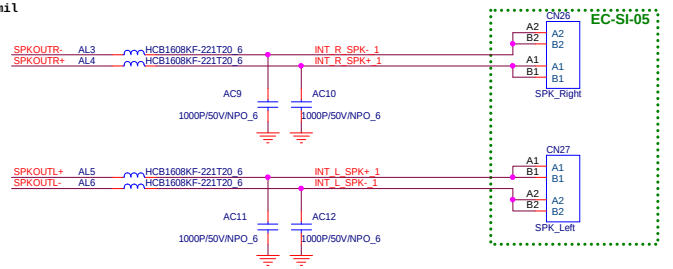


CODEC 5V POWER

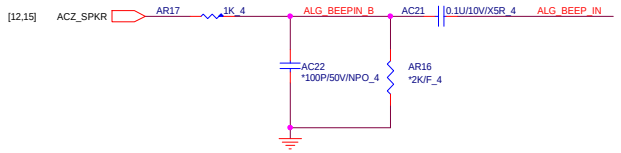


Internal Speaker (2W, 4 ohm)

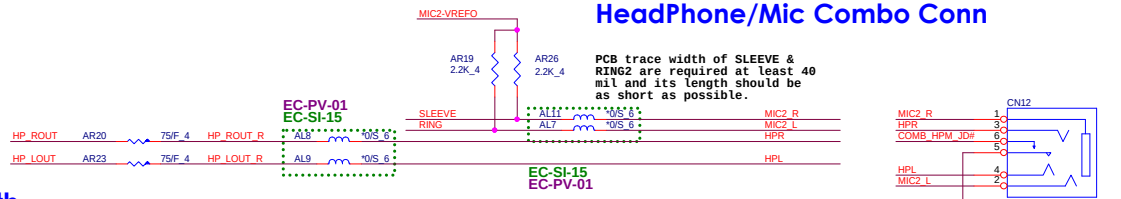
Trace width for SPK-L+/SPK-L-/SPK-R+/SPK-R-
4 ohm : 40mil
8 ohm : 20mil



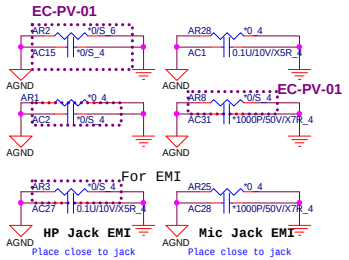
PC BEEP

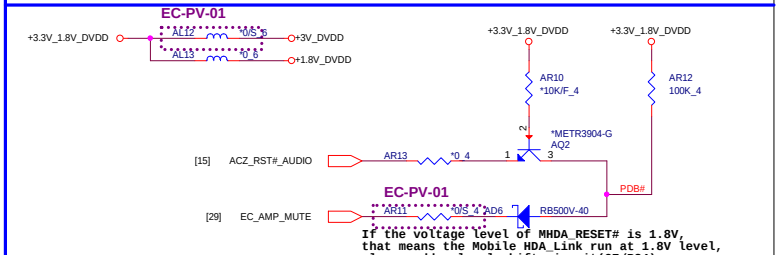


HeadPhone/Mic Combo Conn



CODEC Return Path





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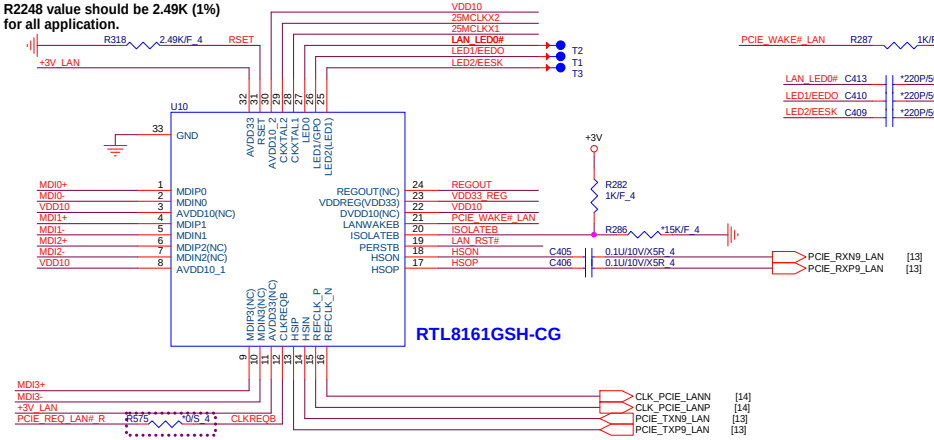
Quanta Computer Inc.

PROJECT: HP-Hawaii

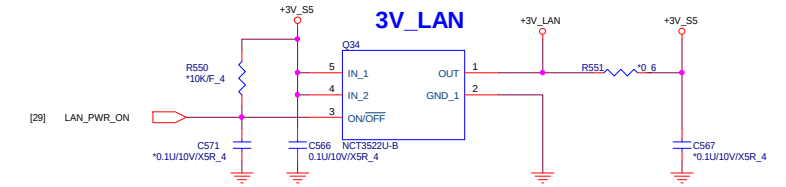
Size	Document Number	Rev
Custom	Audio CODEC	1A

Date: Tuesday, March 22, 2016 Sheet 23 of 58

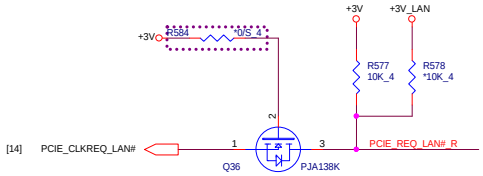
R2248 value should be 2.49K (1%) for all application.

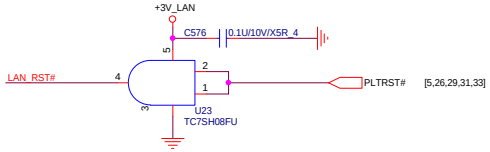


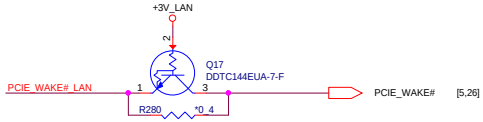
3V_LAN



EC-PV-01

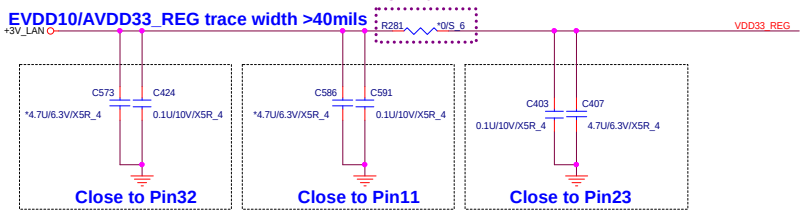




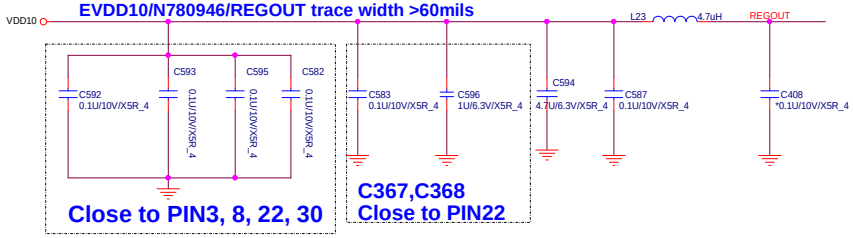


EC-PV-01

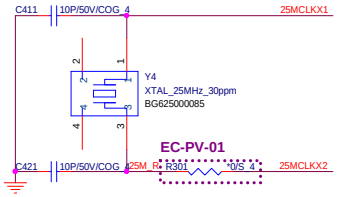
EVDD10/AVDD33_REG trace width >40mils



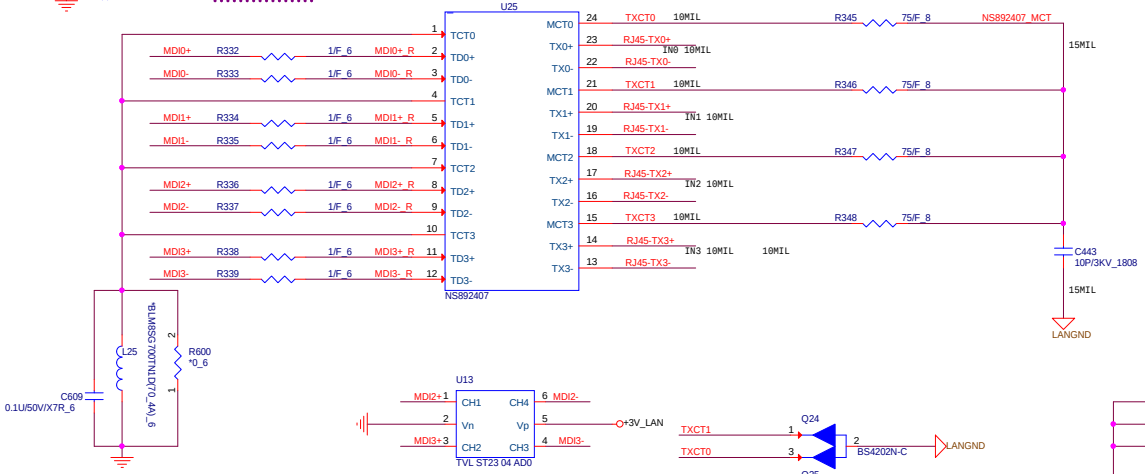
EVDD10/N780946/REGOUT trace width >60mils

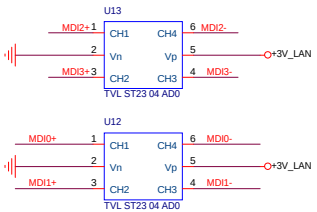


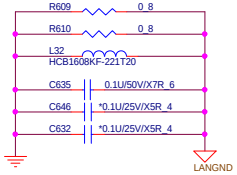
X'tal 25MHz



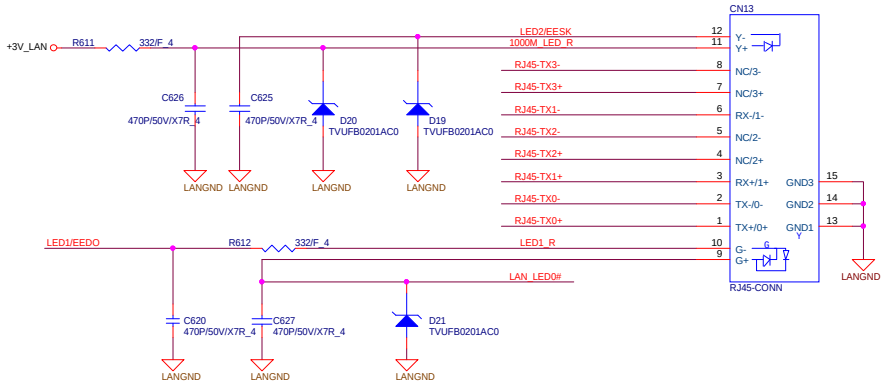
EC-PV-01







LAN Conn



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Quanta Computer Inc.

PROJECT: HP-Hawaii

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Custom	LAN/RJ45	1A

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HDD REDRIVER

C44,C45,C46,C47 CLOSE TO RE-DRIVER IC

[13] SATA_TXP0 — C616 *0.01U/50V/X7R_4, R341 *0/S_4 — SATA_TX0_P_RE — SATA_TX0_P_CON [26]
[13] SATA_TXN0 — C614 *0.01U/50V/X7R_4, R340 *0/S_4 — SATA_TX0_N_RE — SATA_TX0_N_CON [26]
[13] SATA_RXN0 — C612 *0.01U/50V/X7R_4, R331 *0/S_4 — SATA_RX0_N_RE — SATA_RX0_N_CON [26]
[13] SATA_RXP0 — C610 *0.01U/50V/X7R_4, R330 *0/S_4 — SATA_RX0_P_RE — SATA_RX0_P_CON [26]

3 PAD DESIGN

EC-PV-01

[3,5,11,12,13,14,16,17,18,19,20,21,22,24,29,30,34,35,43,46,51,52] +3V

+3V — R592 *0/S_4 — +3V_HDD_REDRIVER

EC-PV-01

+3V
R607 *4.7K_4 — HDD_A_EQ1
R606 *4.7K_4 — HDD_A_EQ2
R608 *4.7K_4 — HDD_B_EQ2
R605 *4.7K_4 — HDD_B_EQ1
R603 *4.7K_4
R602 *4.7K_4
R604 *4.7K_4
R601 *4.7K_4

+3V_HDD_REDRIVER
C618 *4.7U/6.3V/X5R_4
C619 *0.1U/10V/X5R_4
C602 *4.7U/6.3V/X5R_4
C604 *0.1U/10V/X5R_4

U24 *PS8527BTQFN20GTR2-A2

6 VCC			
16 VCC		REXT	10 U21_REXT R598 *4.99K/F_4
HDD_A_EQ1 18 A_EQ1		B_EQ2	17 HDD_B_EQ2
HDD_A_EQ2 19 A_EQ2		B_EQ1	20 HDD_B_EQ1
SATA_TX0_P_RE 1 IN0P		OUT0P	15 SATA_TXP0+_R [26]
SATA_TX0_N_RE 2 IN0M		OUT0M	14 SATA_TXN0-_R [26]
SATA_RX0_N_RE 4 OUT1N		IN1N	12 SATA_RXN0-_R [26]
SATA_RX0_P_RE 5 OUT1P		IN1P	11 SATA_RXP0+_R [26]
+3V R593 *10K/F_4 U21_EN 7 EN		GND	3, 13, 22
+3V R597 *4.7K_4 U21_A_DE 9 A_DE		EP_AGND	23
R595 *4.7K_4 U21_B_DE 8 B_DE		EP	24
R594 *4.7K_4	R596 *4.7K_4	21	25

ODD REDRIVER

C53,C57,C58,C59 CLOSE TO RE-DRIVER IC

[13] SATA_TXP1 — C417 *0.01U/50V/X7R_4, R573 *0/S_4 — SATA_TX1_P_RE — SATA_TX1_P_CON [26]
[13] SATA_TXN1 — C416 *0.01U/50V/X7R_4, R572 *0/S_4 — SATA_TX1_N_RE — SATA_TX1_N_CON [26]
[13] SATA_RXN1 — C415 *0.01U/50V/X7R_4, R571 *0/S_4 — SATA_RX1_N_RE — SATA_RX1_N_CON [26]
[13] SATA_RXP1 — C414 *0.01U/50V/X7R_4, R570 *0/S_4 — SATA_RX1_P_RE — SATA_RX1_P_CON [26]

3 PAD DESIGN

EC-PV-01

+3V — R599 *0/S_4 — +3V_ODD_REDRIVER

EC-PV-01

+3V
R583 *4.7K_4 — ODD_A_EQ1
R576 *4.7K_4 — ODD_A_EQ2
R586 *4.7K_4 — ODD_B_EQ2
R574 *4.7K_4 — ODD_B_EQ1
R322 *4.7K_4
R319 *4.7K_4
R324 *4.7K_4
R305 *4.7K_4

+3V_ODD_REDRIVER
C427 *4.7U/6.3V/X5R_4
C426 *0.1U/10V/X5R_4
C422 *4.7U/6.3V/X5R_4
C418 *0.1U/10V/X5R_4

U11 *PS8527BTQFN20GTR2-A2

6 VCC			
16 VCC		REXT	10 U19_REXT *4.99K/F_4 R329
ODD_A_EQ1 18 A_EQ1		B_EQ2	17 ODD_B_EQ2
ODD_A_EQ2 19 A_EQ2		B_EQ1	20 ODD_B_EQ1
SATA_TX1_P_RE 1 IN0P		OUT0P	15 SATA_TXP1+_R [26]
SATA_TX1_N_RE 2 IN0M		OUT0M	14 SATA_TXN1-_R [26]
SATA_RX1_N_RE 4 OUT1N		IN1N	12 SATA_RXN1-_R [26]
SATA_RX1_P_RE 5 OUT1P		IN1P	11 SATA_RXP1+_R [26]
+3V R320 *10K/F_4 U19_EN 7 EN		GND	3, 13, 22
+3V R328 *4.7K_4 U19_A_DE 9 A_DE		EP_AGND	23
R325 *4.7K_4 U19_B_DE 8 B_DE		EP	24
R323 *4.7K_4	R326 *4.7K_4	21	25

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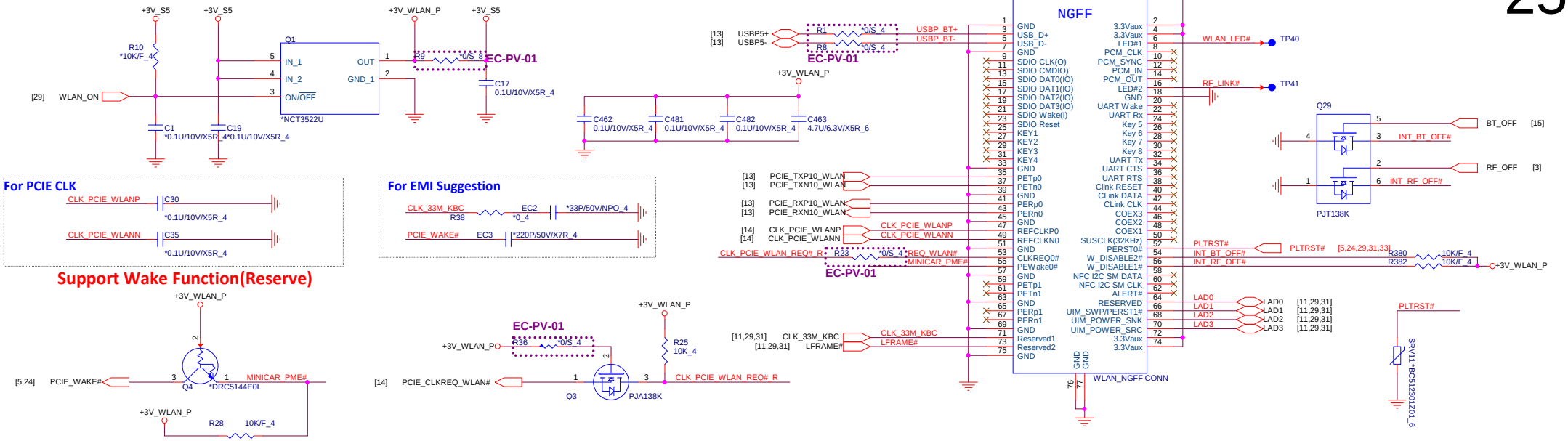
Mini Card WLAN/BT(Option) PCIe M.2_power(S5)

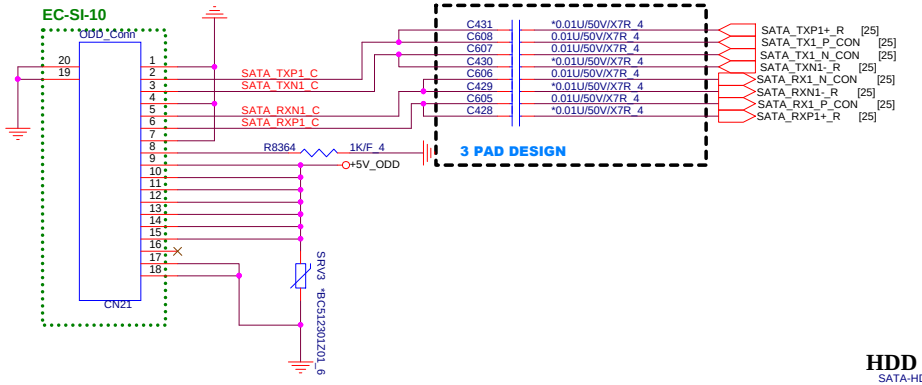


For PCIE CLK

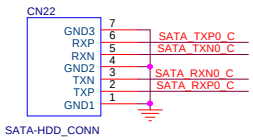
For EMI Suggestion

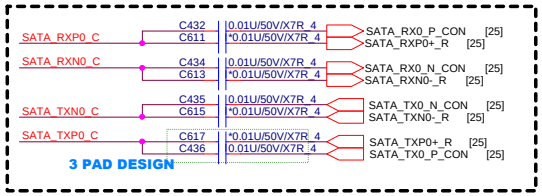
Support Wake Function(Reserve)

ODD

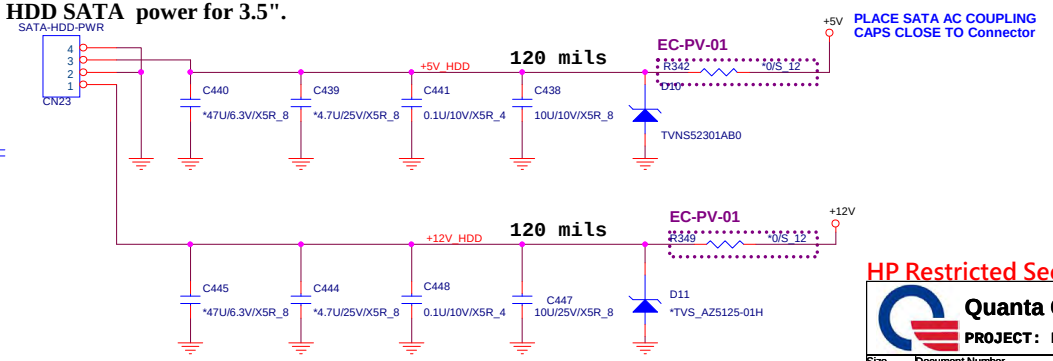


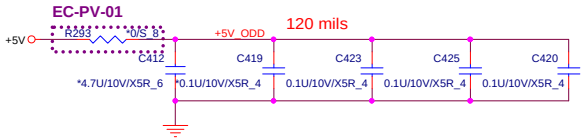
HDD SATA signal for 3.5".

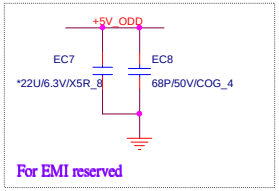




HDD SATA power for 3.5".







[21,22,23,27,30,32,46,47,51] +5V
[3,5,11,12,13,14,16,17,18,19,20,21,22,24,25,29,30,34,35,43,46,51,52] +3V
[5,11,12,13,15,16,17,18,21,24,29,31,32,39,40,41,42,46,47,48,52] +3V_S5

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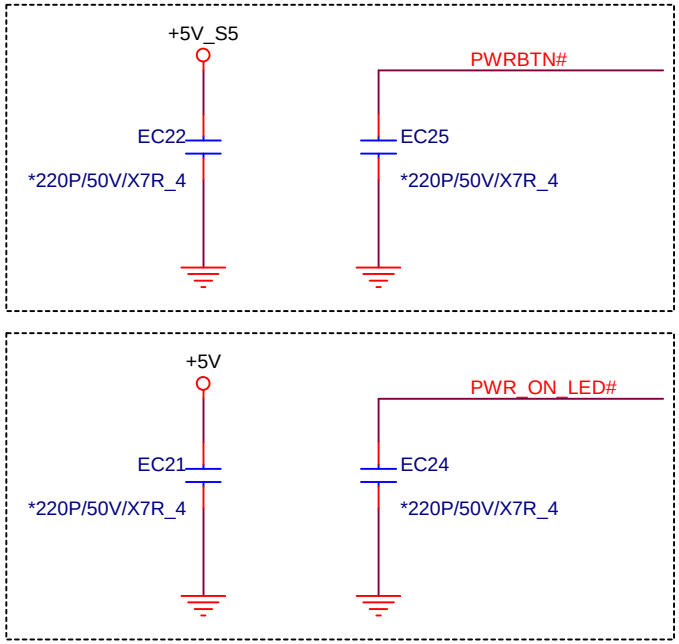
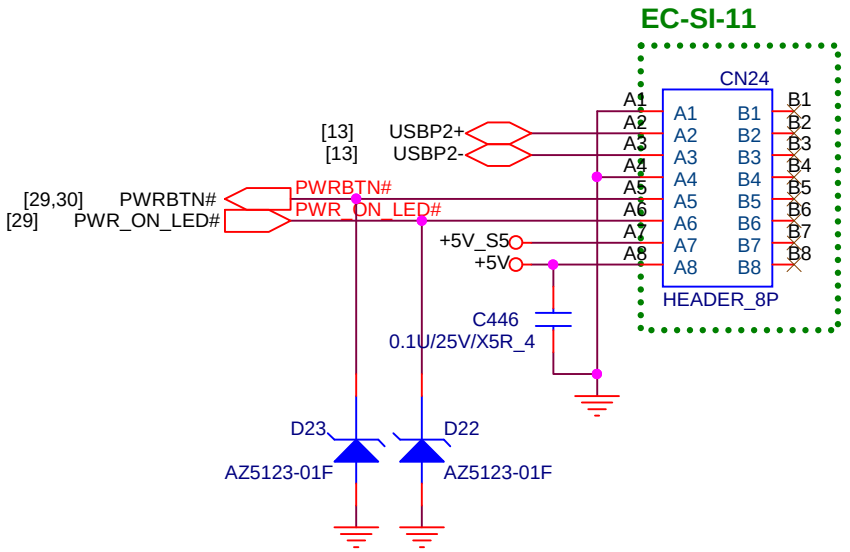
Card reader/Power button conn





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Size	Document Number	Rev
A	Card reader/PWR BTN CONN	1A
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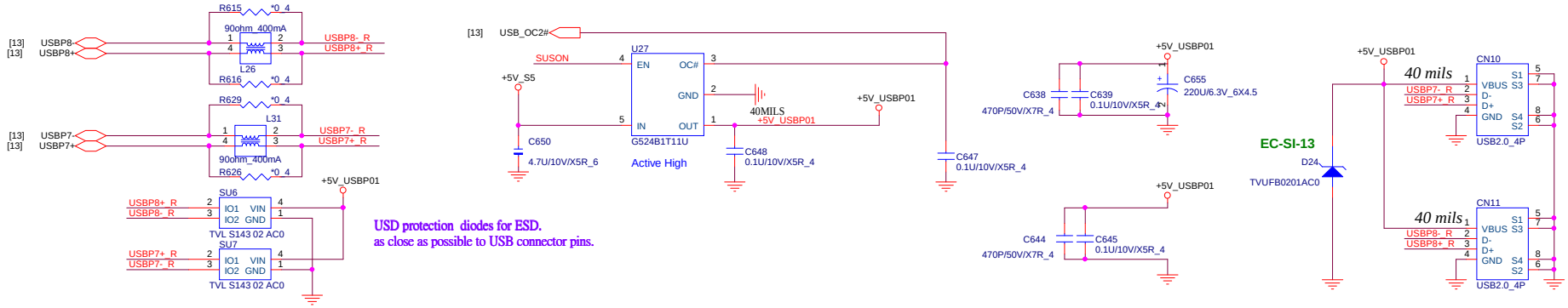
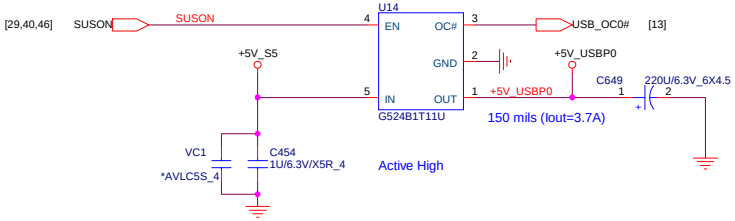
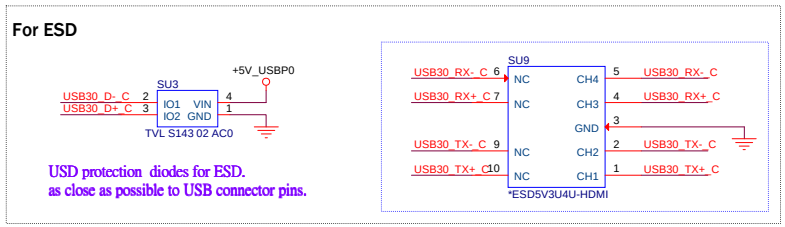
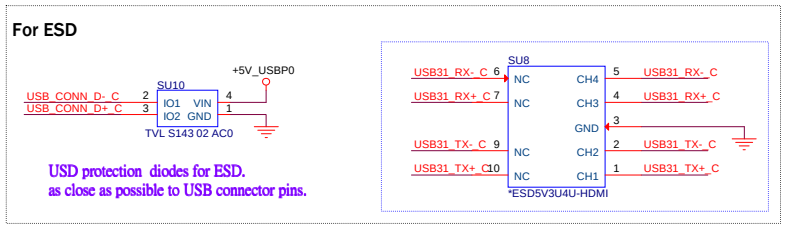
USB 2.0

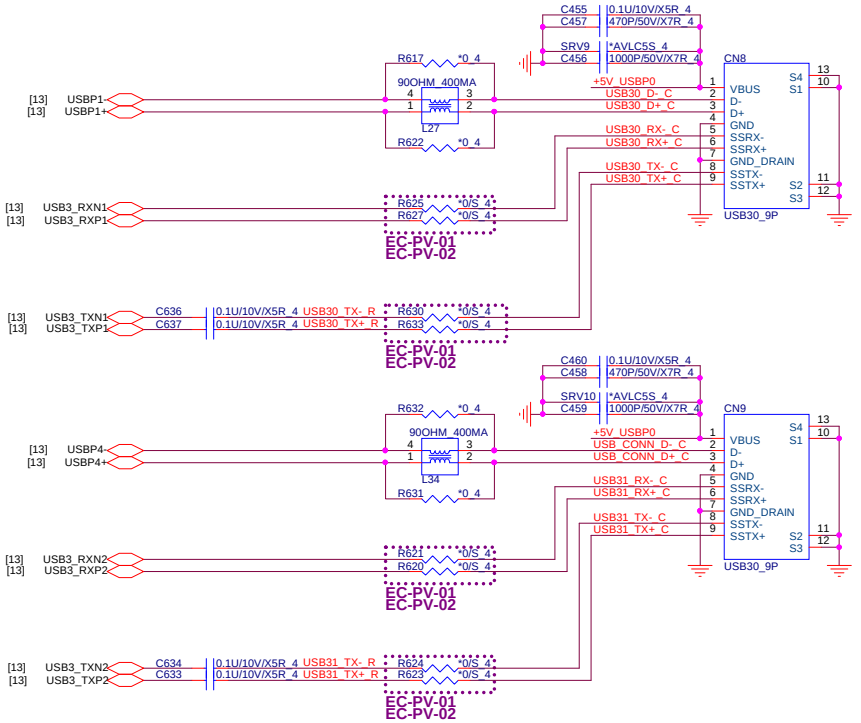


USB 2.0/3.0 Combo









[5,21,23,27,32,39,40,41,43,45,46,47,48,52] +5V_S5

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Size	Document Number	Rev
Custom	USB2.0/USB3.0/Hole/EMI	1A

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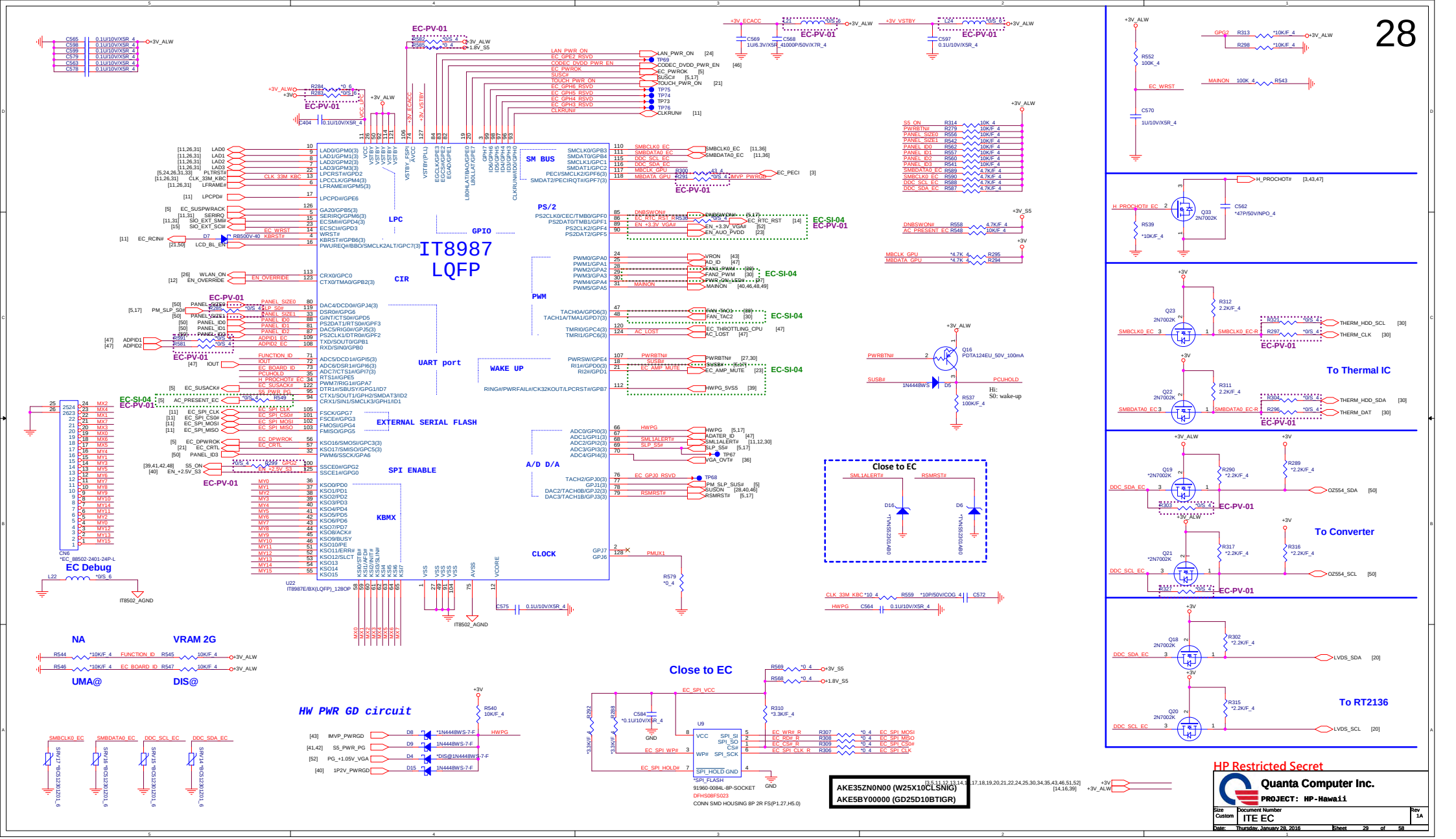
28
IT8987
LQFP
LPC
GPIO
SM BUS
PS/2
CIR
PWM
UART port
WAKE UP
EXTERNAL SERIAL FLASH
SPI ENABLE
KBMX
A/D D/A
CLOCK
EC Debug
NA
VRAM 2G
UMA@
DIS@
HW PWR GD circuit
Close to EC
Close to EC
To Thermal IC
To Converter
To RT2136
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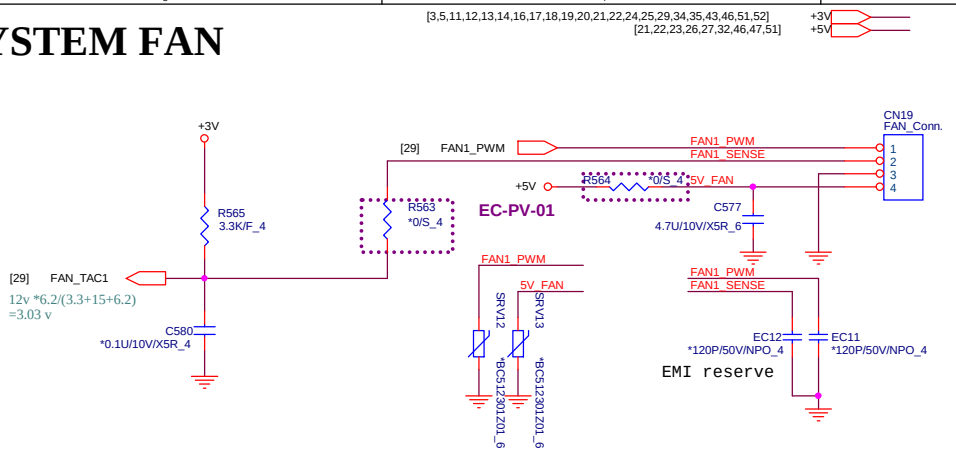
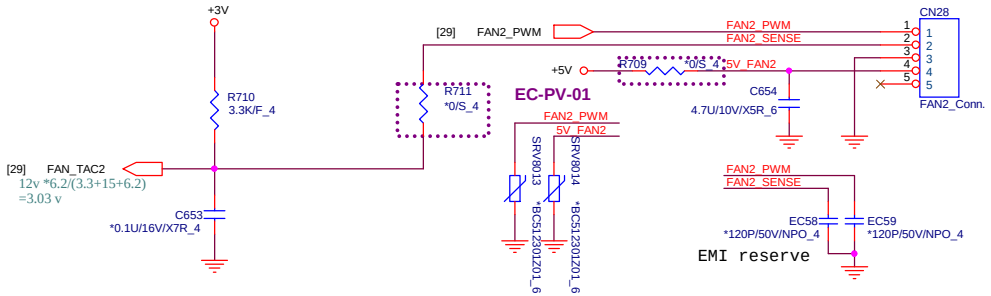
PROJECT: HP-Hawaii
ITE EC
AKE35ZN00N00 (W25X10CLSNIG)
AKE5BY00000 (GD25D10BTIGR)

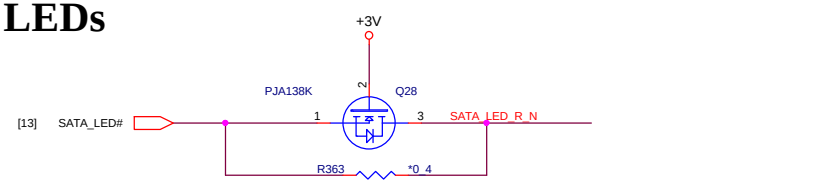
SYSTEM FAN

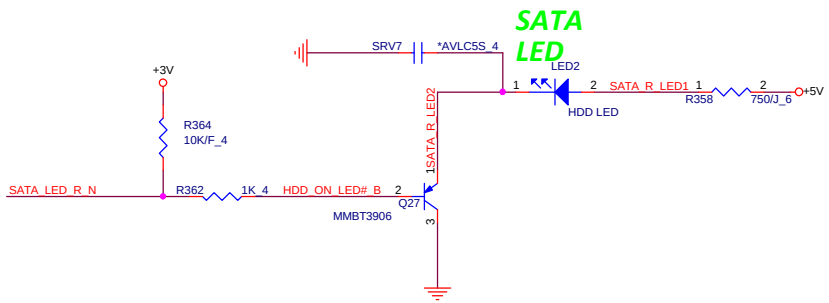


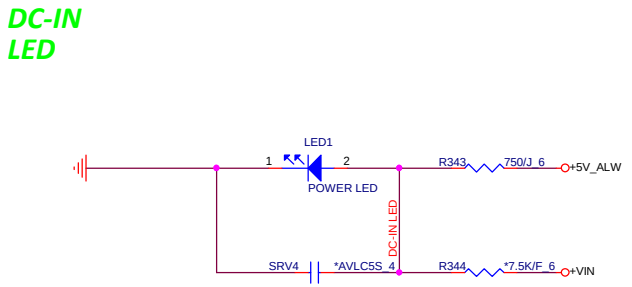
2nd SYSTEM FAN (RSVD)



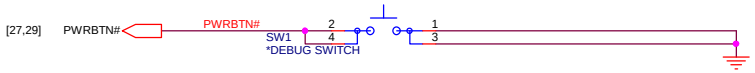
LEDs



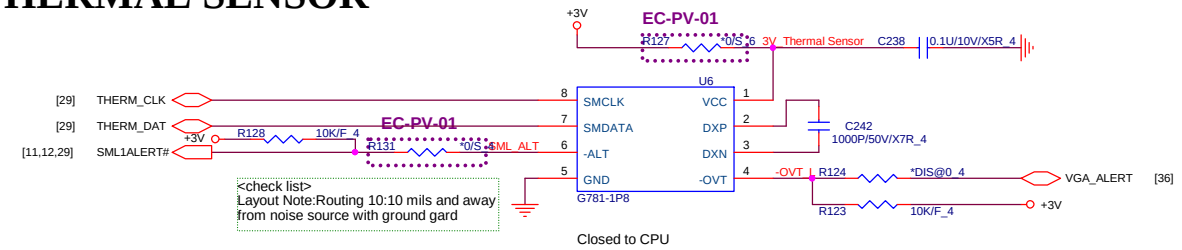




SW1 For Debug.MP will remove it.



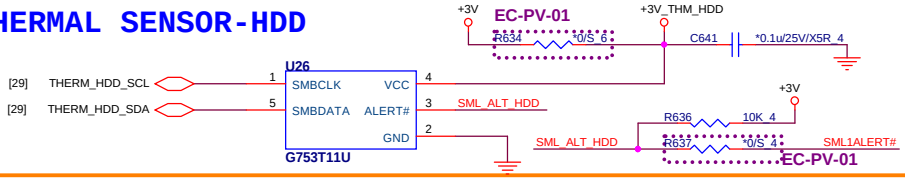
THERMAL SENSOR



Ambient

Slave Adress						
A6	A5	A4	A3	A2	A1	A0
1	0	0	1	0	0	0

THERMAL SENSOR-HDD



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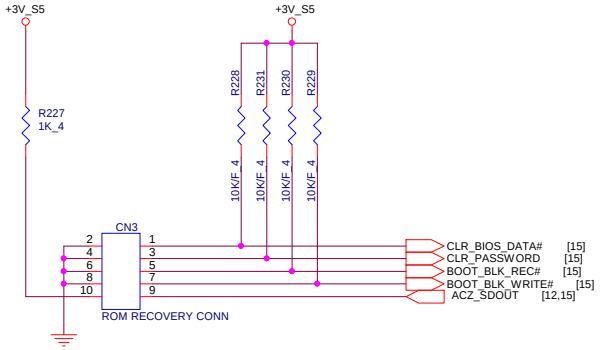
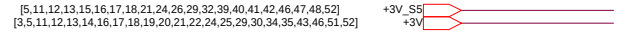
CLR_CMOS

Jumper	Pre-production	Production
BOOT_BLK_Recovery	X	X
BOOT_BLK_Enable	O	X

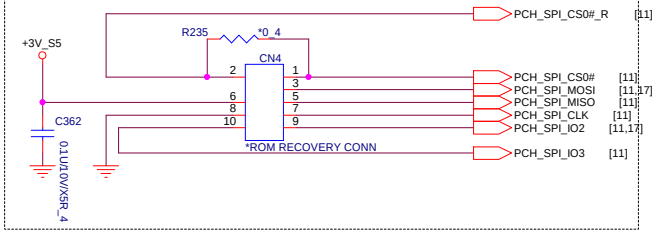
Jumper	Type
Pop	CLR_BIOS_DAT
Pop	CLR_PASSWD
Pop	BOOT_BLK_Recovery
Pop	BOOT_BLK_Enable



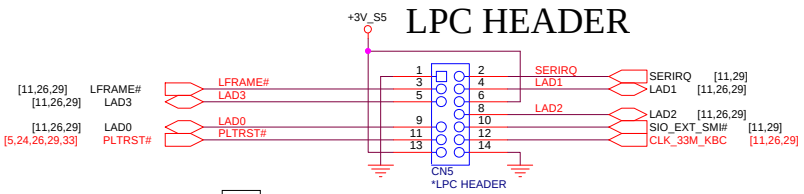


ON Chip select:Default:iinsatall (PROTO only)
CONN MINI JUMPER 2P FS (P2.0,H5.0)

ROM recovery (for pre-production only)

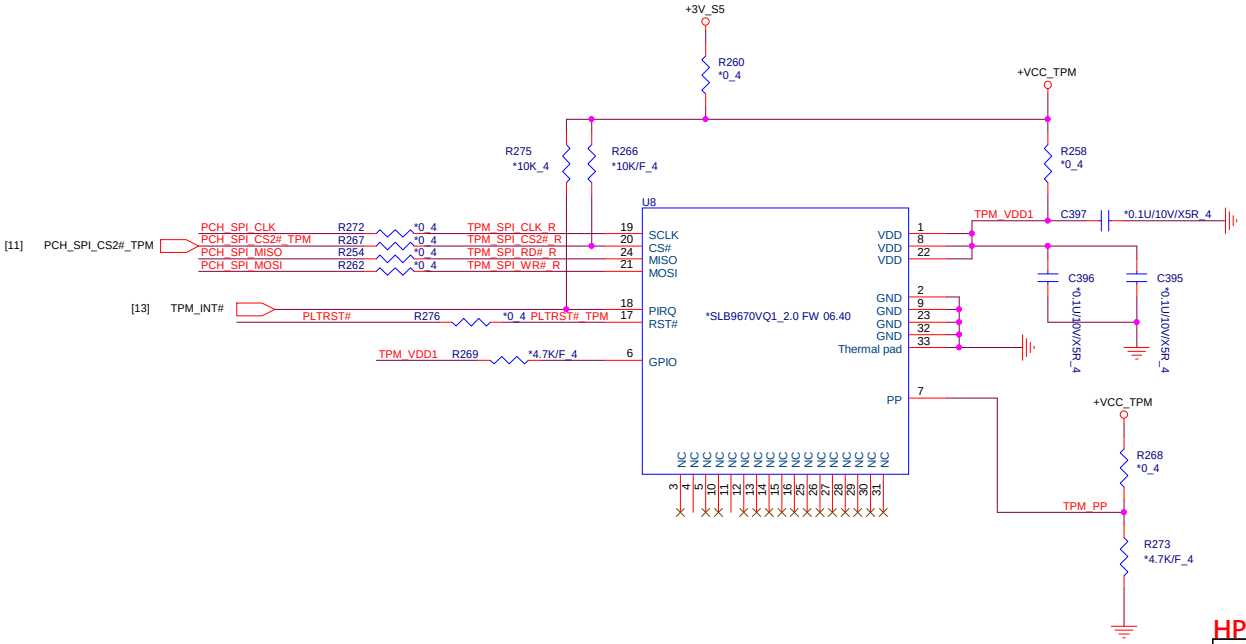


LPC HEADER



CLR_PASSWORD Default:install
CONN MINI JUMPER 2P FS (P2.0,H5.0)

TPM (1.2 or 2.0)



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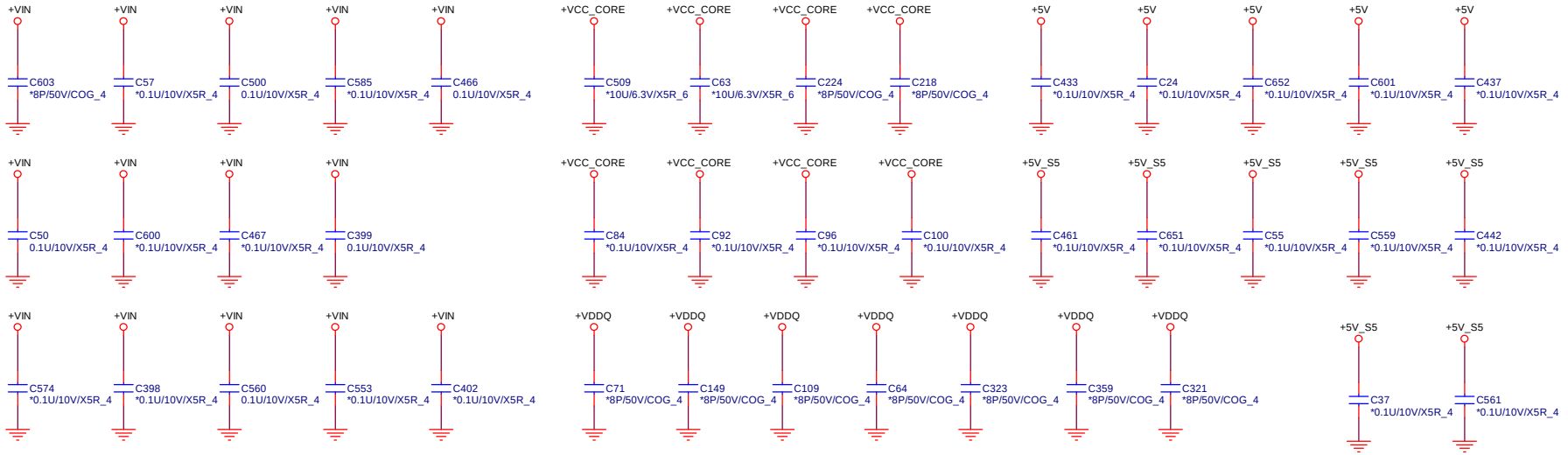
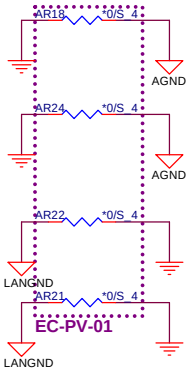
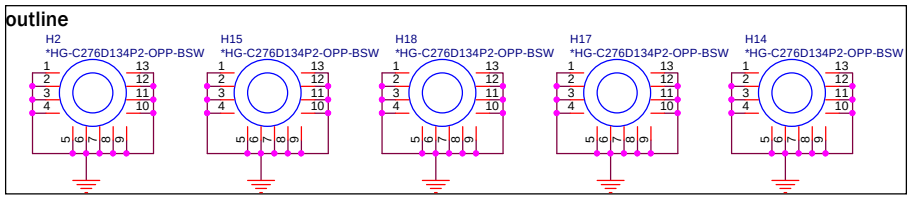
RF/EMI Suggestion

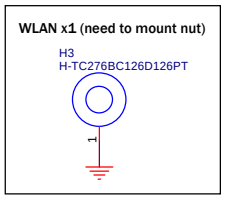
[4,7,18,19,40] +VDDQ
[6,43,44] +VCC_CORE
[30,39,40,41,43,44,45,46,47,48,49,50,51,52] +VIN

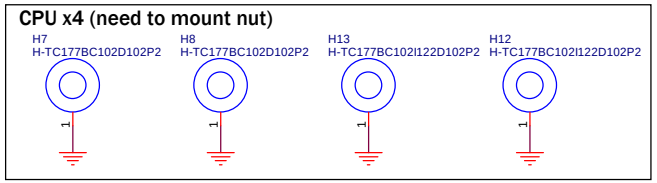


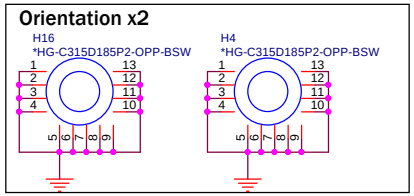


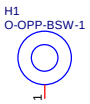
Holes

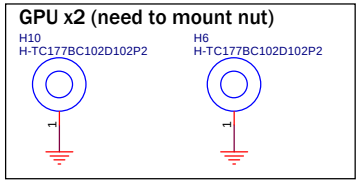


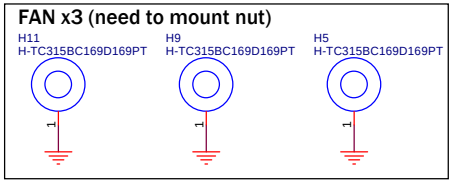


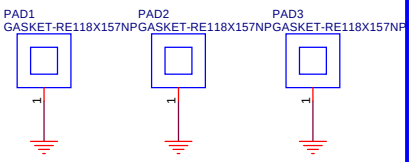


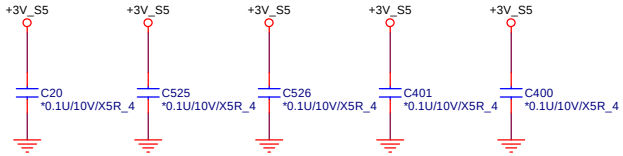












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PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	EMI/RF/Holes	1A
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[34,35,52] +1.05V_VGA
[35,36,37,51,52] +3.3V_VGA

U18A

1/14 PCI_EXPRESS

PEX_IOVDD + PEX_IOVDDQ = 1.042A

+1.05V_VGA

Near GPU
C70 DIS@22U/6.3VS_6
C69 *DIS@22U/6.3VS_6
C65 *DIS@10U/6.3VS_6
C68 DIS@10U/6.3VS_6
C93 DIS@4.7U/6.3V_6

C88 DIS@1U/6.3V_4
C83 *DIS@1U/6.3V_4

Under GPU

AA22 AB23 AC24 AD25 AE26 AE27 — PEX_IOVDD

C119 DIS@22U/6.3VS_6
C95 *DIS@22U/6.3VS_6
C80 *DIS@10U/6.3VS_6
C103 DIS@10U/6.3VS_6
C79 DIS@4.7U/6.3V_6

Near GPU

C72 DIS@1U/6.3V_4
C66 *DIS@1U/6.3V_4

Under GPU

AA10 AA12 AA13 AA16 AA18 AA19 AA20 AA21 AA22 AC23 AD24 AE25 AF26 AF27 — PEX_IOVDDQ

PEX_PLL_HVDD + PEX_SVDD_3V3 = 143mA

+3.3V_VGA

C134 DIS@0.1U/16V_4
C143 DIS@4.7U/6.3V_6
C154 DIS@4.7U/6.3V_6

Near GPU

AA8 AA9 — PEX_PLL_HVDD
AB8 — PEX_SVDD_3V3

[51] VGA_VDD_SEN — F2 — VDD_SENSE
[51] VGA_GND_SEN — F1 — GND_SENSE

*DIS@200/F_4 R397
PEX_TSTCLK AF22 — PEX_TSTCLK_OUT
PEX_TSTCLK# AE22 — PEX_TSTCLK_OUT
CX300T30001 Change to 0ohm

+1.05V_VGA R68 DIS@0_6

Near GPU
DIS@4.7U/6.3V_6 C106
DIS@1U/6.3V_4 C114
PEX_PLLVDD AA14 AA15 — PEX_PLLVDD

DIS@0.1U/16V_4 C115
Under GPU

PEX_PLLVDD = 130mA

DIS@10K/F_4 R102 TESTMODE AD9 — TESTMODE

DIS@2.49K/F_4 R55 PEX_TERMP AF25 — PEX_TERMP

PEX_WAKE AB6 — C173 *DIS@0.1U/16V_4
PEX_RST AC7 VGA_RST# — R86 *DIS@0/short_4 — PEGX_RST# [36]
PEX_CLKREQ AC6 PEX_CLKREQ# — R453 DIS@10K/F_4 — +3.3V_VGA
PEX_REFCLK AE8 — CLK_GFX_P [14]
PEX_REFCLK AD8 — CLK_GFX_N [14]

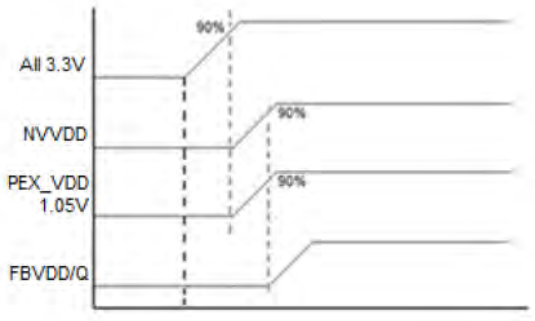
PEX_TX0	AC9	C_PCIE_RXP1_GPU C142	DIS@0.22u/10V/X5R_4	PCIE_RXP1_GPU [13]
PEX_TX0	AB9	C_PCIE_RXN1_GPU C147	DIS@0.22u/10V/X5R_4	PCIE_RXN1_GPU [13]
PEX_RX0	AG6	PCIE_TXP1_GPU		PCIE_TXP1_GPU [13]
PEX_RX0	AG7	PCIE_TXN1_GPU		PCIE_TXN1_GPU [13]
PEX_TX1	AB10	C_PCIE_RXP2_GPU C123	DIS@0.22u/10V/X5R_4	PCIE_RXP2_GPU [13]
PEX_TX1	AC10	C_PCIE_RXN2_GPU C128	DIS@0.22u/10V/X5R_4	PCIE_RXN2_GPU [13]
PEX_RX1	AF7	PCIE_TXP2_GPU		PCIE_TXP2_GPU [13]
PEX_RX1	AE7	PCIE_TXN2_GPU		PCIE_TXN2_GPU [13]
PEX_TX2	AD11	C_PCIE_RXP3_GPU C130	DIS@0.22u/10V/X5R_4	PCIE_RXP3_GPU [13]
PEX_TX2	AC11	C_PCIE_RXN3_GPU C135	DIS@0.22u/10V/X5R_4	PCIE_RXN3_GPU [13]
PEX_RX2	AE9	PCIE_TXP3_GPU		PCIE_TXP3_GPU [13]
PEX_RX2	AF9	PCIE_TXN3_GPU		PCIE_TXN3_GPU [13]
PEX_TX3	AC12	C_PCIE_RXP4_GPU C116	DIS@0.22u/10V/X5R_4	PCIE_RXP4_GPU [13]
PEX_TX3	AB12	C_PCIE_RXN4_GPU C118	DIS@0.22u/10V/X5R_4	PCIE_RXN4_GPU [13]
PEX_RX3	AG9	PCIE_TXP4_GPU		PCIE_TXP4_GPU [13]
PEX_RX3	AG10	PCIE_TXN4_GPU		PCIE_TXN4_GPU [13]

PEX_TX4 AB13 AC13
PEX_RX4 AF10 AE10
PEX_TX5 AD14 AC14
PEX_RX5 AE12 AF12
PEX_TX6 AC15 AB15
PEX_RX6 AG12 AG13
PEX_TX7 AB16 AC16
PEX_RX7 AF13 AE13
PEX_TX8 AD17 AC17
PEX_RX8 AE15 AF15
PEX_TX9 AC18 AB18
PEX_RX9 AG15 AG16
PEX_TX10 AB19 AC19
PEX_RX10 AF16 AE16
PEX_TX11 AD20 AC20
PEX_RX11 AE18 AF18
PEX_TX12 AC21 AB21
PEX_RX12 AG18 AG19
PEX_TX13 AD23 AE23
PEX_RX13 AF19 AE19
PEX_TX14 AF24 AE24
PEX_RX14 AE21 AF21
PEX_TX15 AG24 AG25
PEX_RX15 AG21 AG22

NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC

GF117 GF119

bga595-nvidia-n13p-gv2-s-a2 COMMON



+3.3V_VGA

U5
DIS@TC7SH08FU
C215
DIS@0.1U/16V_4

[5,24,26,29,31] PLTRST#
[15] DGPU_HOLD_RST#
SYS_PEX_RST_R466
*DIS@0_4 SYS_PEX_RST_MON#
[36] GPU_PEX_RST_HOLD#
R473 *DISG@0/short_4

U20
*DIS@TC7SH08FU
C517
*DIS@0.1U/16V_4
PEGX_RST#
R474
DIS@100K/F_4

+3.3V_VGA

R90
DIS@10K/F_4
Q12
DIS@2N7002K
Q8
DIS@2N7002K
PEX_CLKREQ#
PCIE_CLKREQ_VGA# [14]

R464
*DIS@100K/F_4
SYS_PEX_RST_MON# [36]

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Quanta Computer Inc.
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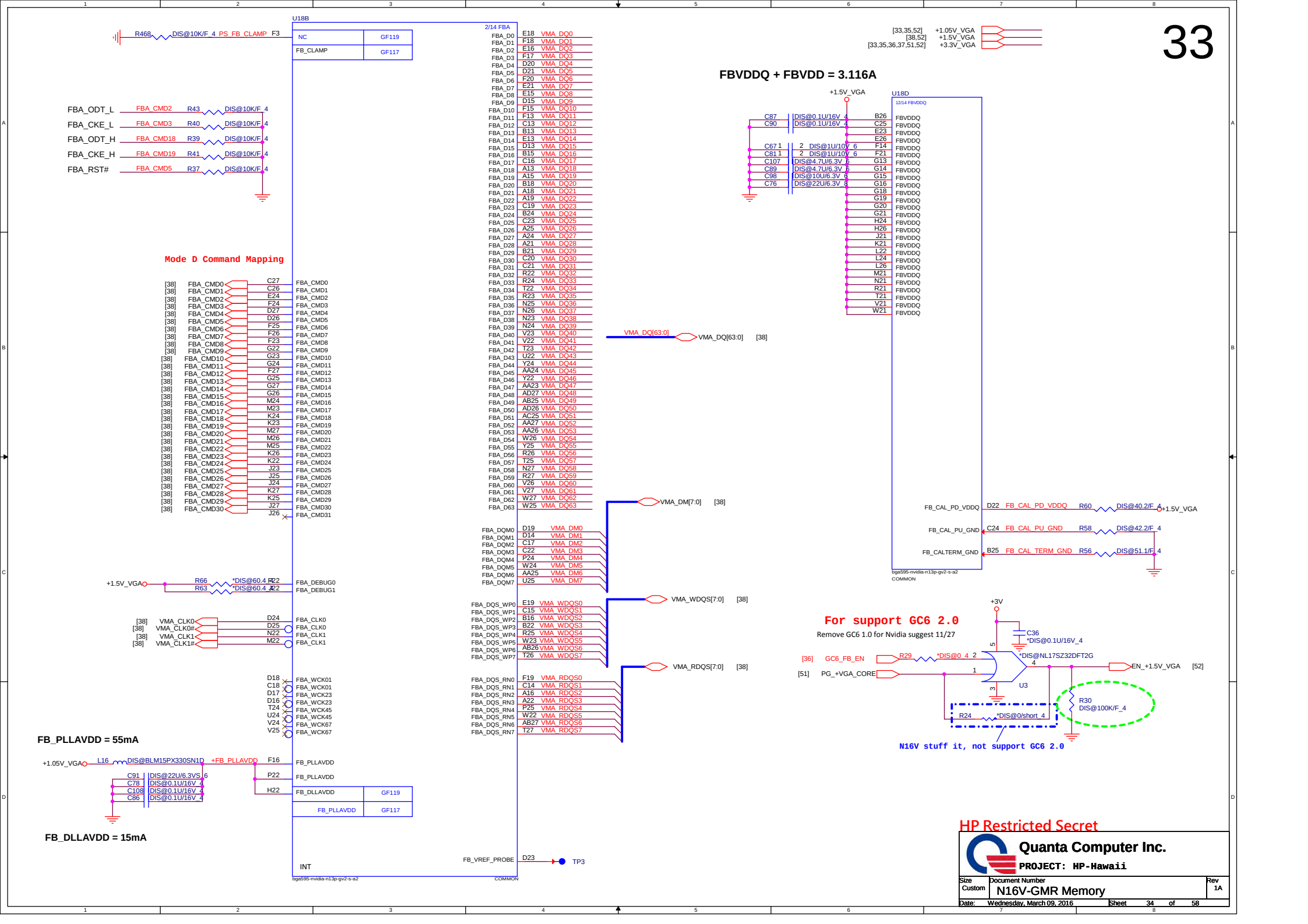
U18B
2/14 FBA
R468 DIS@10K/F_4 PS_FB_CLAMP F3
NC GF119
FB_CLAMP GF117
FBA_ODT_L FBA_CMD2 R43 DIS@10K/F_4
FBA_CKE_L FBA_CMD3 R40 DIS@10K/F_4
FBA_ODT_H FBA_CMD18 R39 DIS@10K/F_4
FBA_CKE_H FBA_CMD19 R41 DIS@10K/F_4
FBA_RST# FBA_CMD5 R37 DIS@10K/F_4
Mode D Command Mapping
FBA_CMD0 C27
FBA_CMD1 C26
FBA_CMD2 E24
FBA_CMD3 F24
FBA_CMD4 D27
FBA_CMD5 D26
FBA_CMD6 F25
FBA_CMD7 F26
FBA_CMD8 F23
FBA_CMD9 G22
FBA_CMD10 G23
FBA_CMD11 G24
FBA_CMD12 F27
FBA_CMD13 G25
FBA_CMD14 G27
FBA_CMD15 G26
FBA_CMD16 M24
FBA_CMD17 M23
FBA_CMD18 K24
FBA_CMD19 K23
FBA_CMD20 M27
FBA_CMD21 M26
FBA_CMD22 M25
FBA_CMD23 K26
FBA_CMD24 K22
FBA_CMD25 J23
FBA_CMD26 J25
FBA_CMD27 J24
FBA_CMD28 K27
FBA_CMD29 K25
FBA_CMD30 J27
FBA_CMD31 J26
+1.5V_VGA R66 *DIS@60.4 R22 FBA_DEBUG0
R63 *DIS@60.4 J22 FBA_DEBUG1
VMA_CLK0 D24 FBA_CLK0
VMA_CLK0# D25 FBA_CLK0
VMA_CLK1 N22 FBA_CLK1
VMA_CLK1# M22 FBA_CLK1
FBA_WCK01 D18
FBA_WCK01 C18
FBA_WCK23 D17
FBA_WCK23 D16
FBA_WCK45 T24
FBA_WCK45 U24
FBA_WCK67 V24
FBA_WCK67 V25
FB_PLLAVDD = 55mA
+1.05V_VGA L16 DIS@BLM15PX330SN1D +FB_PLLAVDD F16
C91 DIS@22U/6.3VS_6
C78 DIS@0.1U/16V_4
C108 DIS@0.1U/16V_4
C86 DIS@0.1U/16V_4
FBA_PLLAVDD P22
FBA_PLLAVDD H22
FB_DLLAVDD GF119
FB_PLLAVDD GF117
FB_DLLAVDD = 15mA
INT
bga595-nvidia-n13p-gv2-s-a2
COMMON
FBA_D0 E18 VMA_DQ0
FBA_D1 F18 VMA_DQ1
FBA_D2 E16 VMA_DQ2
FBA_D3 F17 VMA_DQ3
FBA_D4 D20 VMA_DQ4
FBA_D5 D21 VMA_DQ5
FBA_D6 F20 VMA_DQ6
FBA_D7 E21 VMA_DQ7
FBA_D8 E15 VMA_DQ8
FBA_D9 D15 VMA_DQ9
FBA_D10 F15 VMA_DQ10
FBA_D11 F13 VMA_DQ11
FBA_D12 C13 VMA_DQ12
FBA_D13 B13 VMA_DQ13
FBA_D14 E13 VMA_DQ14
FBA_D15 D13 VMA_DQ15
FBA_D16 B15 VMA_DQ16
FBA_D17 C16 VMA_DQ17
FBA_D18 A13 VMA_DQ18
FBA_D19 A15 VMA_DQ19
FBA_D20 B18 VMA_DQ20
FBA_D21 A18 VMA_DQ21
FBA_D22 A19 VMA_DQ22
FBA_D23 C19 VMA_DQ23
FBA_D24 B24 VMA_DQ24
FBA_D25 C23 VMA_DQ25
FBA_D26 A25 VMA_DQ26
FBA_D27 A24 VMA_DQ27
FBA_D28 A21 VMA_DQ28
FBA_D29 B21 VMA_DQ29
FBA_D30 C20 VMA_DQ30
FBA_D31 C21 VMA_DQ31
FBA_D32 R22 VMA_DQ32
FBA_D33 R24 VMA_DQ33
FBA_D34 T22 VMA_DQ34
FBA_D35 R23 VMA_DQ35
FBA_D36 N25 VMA_DQ36
FBA_D37 N26 VMA_DQ37
FBA_D38 N23 VMA_DQ38
FBA_D39 N24 VMA_DQ39
FBA_D40 V23 VMA_DQ40
FBA_D41 V22 VMA_DQ41
FBA_D42 T23 VMA_DQ42
FBA_D43 U22 VMA_DQ43
FBA_D44 Y24 VMA_DQ44
FBA_D45 AA24 VMA_DQ45
FBA_D46 Y22 VMA_DQ46
FBA_D47 AA23 VMA_DQ47
FBA_D48 AD27 VMA_DQ48
FBA_D49 AB25 VMA_DQ49
FBA_D50 AD26 VMA_DQ50
FBA_D51 AC25 VMA_DQ51
FBA_D52 AA27 VMA_DQ52
FBA_D53 AA26 VMA_DQ53
FBA_D54 W26 VMA_DQ54
FBA_D55 Y25 VMA_DQ55
FBA_D56 R26 VMA_DQ56
FBA_D57 T25 VMA_DQ57
FBA_D58 N27 VMA_DQ58
FBA_D59 R27 VMA_DQ59
FBA_D60 V26 VMA_DQ60
FBA_D61 V27 VMA_DQ61
FBA_D62 W27 VMA_DQ62
FBA_D63 W25 VMA_DQ63
VMA_DQ[63:0]
VMA_DQ[63:0] [38]
FBA_DQM0 D19 VMA_DM0
FBA_DQM1 D14 VMA_DM1
FBA_DQM2 C17 VMA_DM2
FBA_DQM3 C22 VMA_DM3
FBA_DQM4 P24 VMA_DM4
FBA_DQM5 W24 VMA_DM5
FBA_DQM6 AA25 VMA_DM6
FBA_DQM7 U25 VMA_DM7
VMA_DM[7:0] [38]
FBA_DQS_WP0 E19 VMA_WDQS0
FBA_DQS_WP1 C15 VMA_WDQS1
FBA_DQS_WP2 B16 VMA_WDQS2
FBA_DQS_WP3 B22 VMA_WDQS3
FBA_DQS_WP4 R25 VMA_WDQS4
FBA_DQS_WP5 W23 VMA_WDQS5
FBA_DQS_WP6 AB26 VMA_WDQS6
FBA_DQS_WP7 T26 VMA_WDQS7
VMA_WDQS[7:0] [38]
FBA_DQS_RN0 F19 VMA_RDQS0
FBA_DQS_RN1 C14 VMA_RDQS1
FBA_DQS_RN2 A16 VMA_RDQS2
FBA_DQS_RN3 A22 VMA_RDQS3
FBA_DQS_RN4 P25 VMA_RDQS4
FBA_DQS_RN5 W22 VMA_RDQS5
FBA_DQS_RN6 AB27 VMA_RDQS6
FBA_DQS_RN7 T27 VMA_RDQS7
VMA_RDQS[7:0] [38]
FB_VREF_PROBE D23 TP3
[33,35,52] +1.05V_VGA
[38,52] +1.5V_VGA
[33,35,36,37,51,52] +3.3V_VGA
FBVDDQ + FBVDD = 3.116A
+1.5V_VGA
U18D
12/14 FBVDDQ
C87 DIS@0.1U/16V_4
C90 DIS@0.1U/16V_4
C67 DIS@1U/10V_6
C81 DIS@1U/10V_6
C107 DIS@4.7U/6.3V_6
C89 DIS@4.7U/6.3V_6
C98 DIS@10U/6.3V_6
C76 DIS@22U/6.3V_8
B26 C25 E23 E26 F14 F21 G13 G14 G15 G16 G18 G19 G20 G21 H24 H26 J21 K21 L22 L24 L26 M21 N21 R21 T21 V21 W21 FBVDDQ
FB_CAL_PD_VDDQ D22 FB_CAL_PD_VDDQ R60 DIS@40.2/F_4 +1.5V_VGA
FB_CAL_PU_GND C24 FB_CAL_PU_GND R58 DIS@42.2/F_4
FB_CALTERM_GND B25 FB_CAL_TERM_GND R56 DIS@51.1/F_4
bga595-nvidia-n13p-gv2-s-a2
COMMON
For support GC6 2.0
Remove GC6 1.0 for Nvidia suggest 11/27
+3V
C36 *DIS@0.1U/16V_4
[36] GC6_FB_EN R29 *DIS@0_4
[51] PG_+VGA_CORE
*DIS@NL17SZ32DFT2G
U3
EN_+1.5V_VGA [52]
R24 *DIS@0/short_4
R30 DIS@100K/F_4
N16V stuff it, not support GC6 2.0
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
Size Custom
Document Number N16V-GMR Memory
Rev 1A
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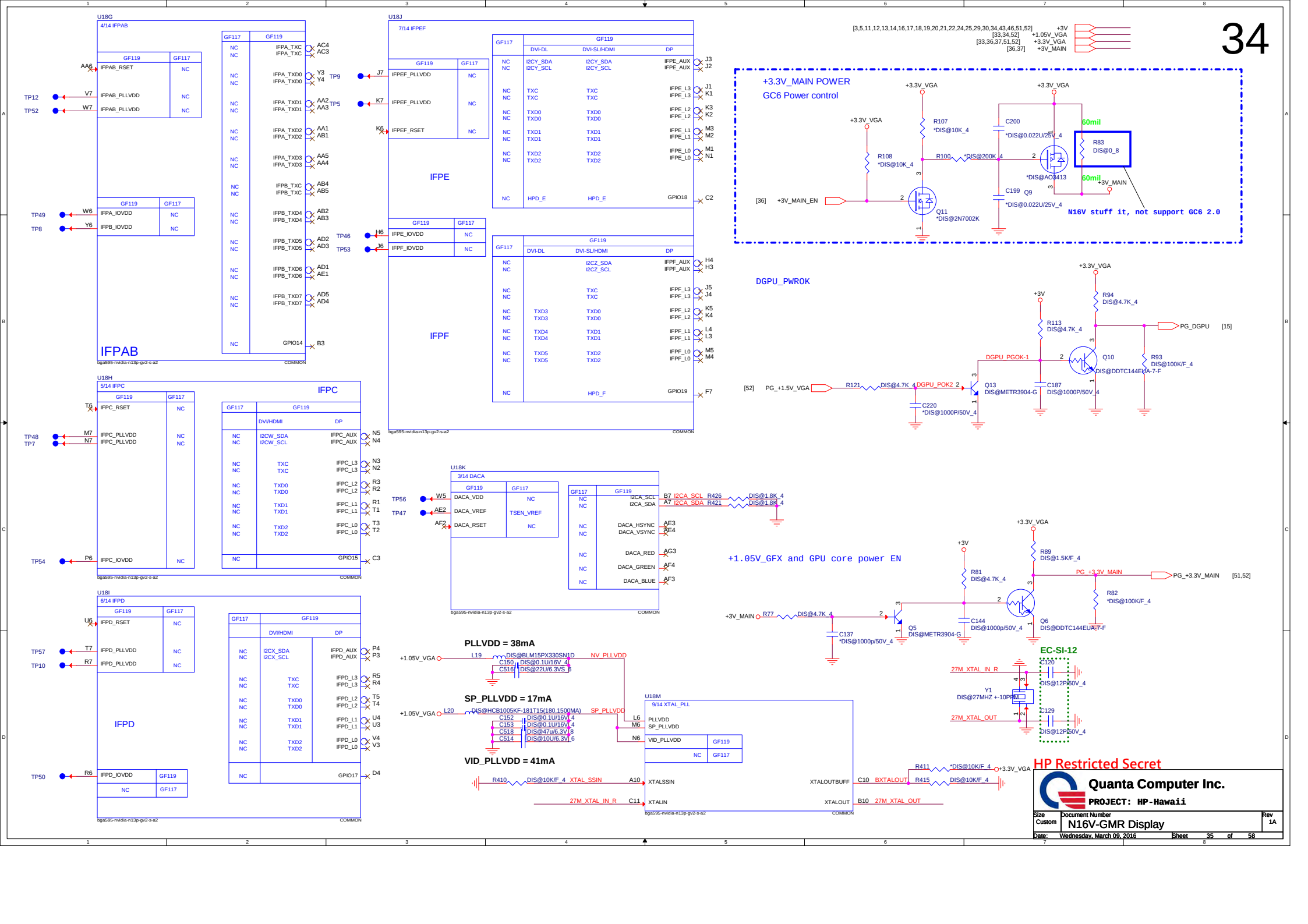
U18G
4/14 IFPAB
IFPAB
U18J
7/14 IFPEF
IFPE
IFPF
U18H
5/14 IFPC
IFPC
U18K
3/14 DACA
U18I
6/14 IFPD
IFPD
U18M
9/14 XTAL_PLL
+3.3V_MAIN POWER
GC6 Power control
N16V stuff it, not support GC6 2.0
DGPU_PWROK
+1.05V_GFX and GPU core power EN
PLLVDD = 38mA
SP_PLLVDD = 17mA
VID_PLLVDD = 41mA
EC-SI-12
HP Restricted Secret
Quanta Computer Inc.
PROJECT: HP-Hawaii
N16V-GMR Display
Size Custom
Rev 1A
Date: Wednesday, March 09, 2016
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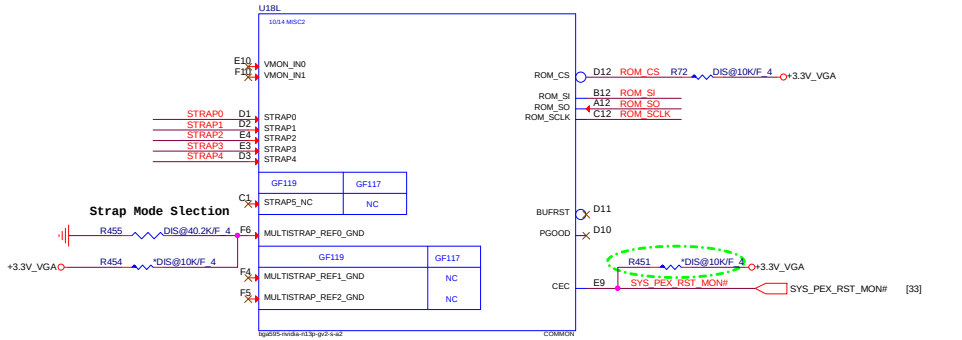

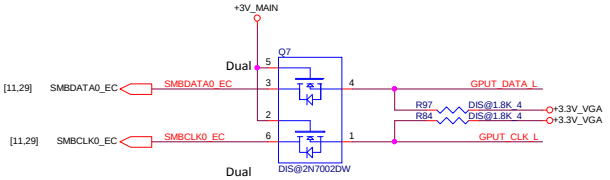

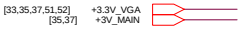

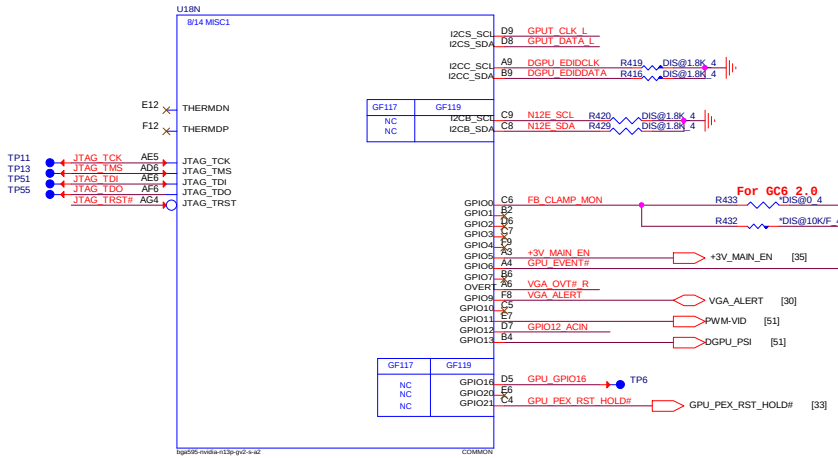

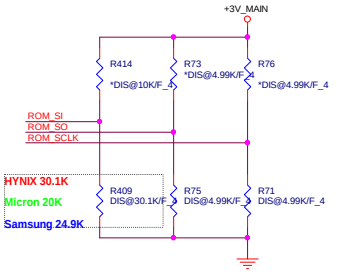

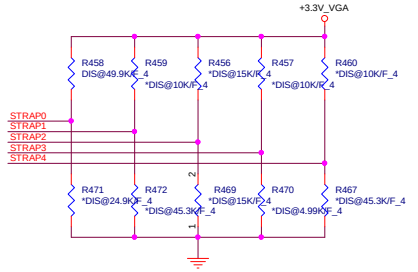

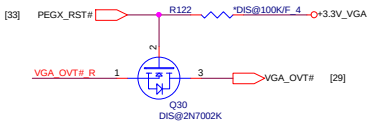

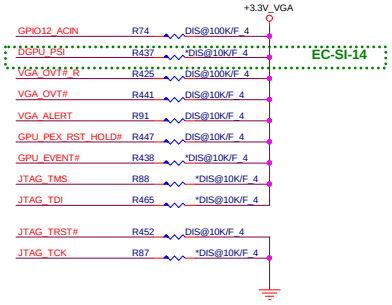

GPIO ASSIGNMENTS

GPIO	I/O	PIN	USAGE
0	IN	FB_CLAMP_MON	FB Clamp monitor (GC6 1.0)
0	OUT	GC6_FB_EN	GC6 FB Enable (GC6 2.0)
5	OUT	+3V_MAIN_EN	Enable GC6 +3V_MAIN
6	OUT	FB_CLAMP_REQ#	Active low FB Clamp toggle request (GC6 1.0)
6	IN	DGPU_EVENT#	DGPU EVENT from CPU (GC6 2.0)
8	OUT	VGA_OVT#	ACTIVE LOW THERMAL OVER TEMP
9	OUT	ALERT	ACTIVE LOW THERMAL ALERT
11	OUT	PWR_VID	GPU CORE_VDD PWM Control signal
12	IN	PWR_LEVEL	AC Power detect or power supply overdraw input
13	OUT	PSI	Phase Shedding

N16V-GMR1 DID=0x134F

GB2B-64

```
ROM_SCLK = Stuff 4.99K pull down
ROM_SO   = Stuff 4.99K pull down
STRAP0   = Stuff 49.9K pull up
STRAP1   = NC
STRAP2   = NC
STRAP3   = NC
STRAP4   = NC
ROM_SI   = VRAM Configuration follow below table
```

Logical Strap Bit Mapping

	PU-VDD	PD	QCI P/N
4.99K	1000	0000	CS24992FB26
10K	1001	0001	CS31002FB26
15K	1010	0010	CS31502FB24
20K	1011	0011	CS32002FB29
24.9K	1100	0100	CS32492FB16
30.1K	1101	0101	CS33012FB18
34.8K	1110	0110	CS33482FB06
45.3K	1111	0111	CS34532FB18

ROM_SI

RAMCFG [3:0]	DESCRIPTION 1.5V DDR3	Vendor	Vendor P/N	ROM_SI	STN B/S	Configuration
	256Mx16					
0011	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Micron	MT41J256M16LY-091G:N	PD 20K ohm	AKD59GSTL02	Single Rank or
1001	DDR3 256Mx16, 64bit, 4Gb,1000MHz	HYNIX	H5TC4G63CFR-N0C	PD 30.1K ohm	AKD5PZDTW03	Single Rank stuffing
1000	DDR3 256Mx16, 64bit, 4Gb,1000MHz	Samsung	K4W4G1646E-BC1A	PD 24.9K ohm	AKD5PGDT502	for Dual Rank

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Size	Document Number	Rev
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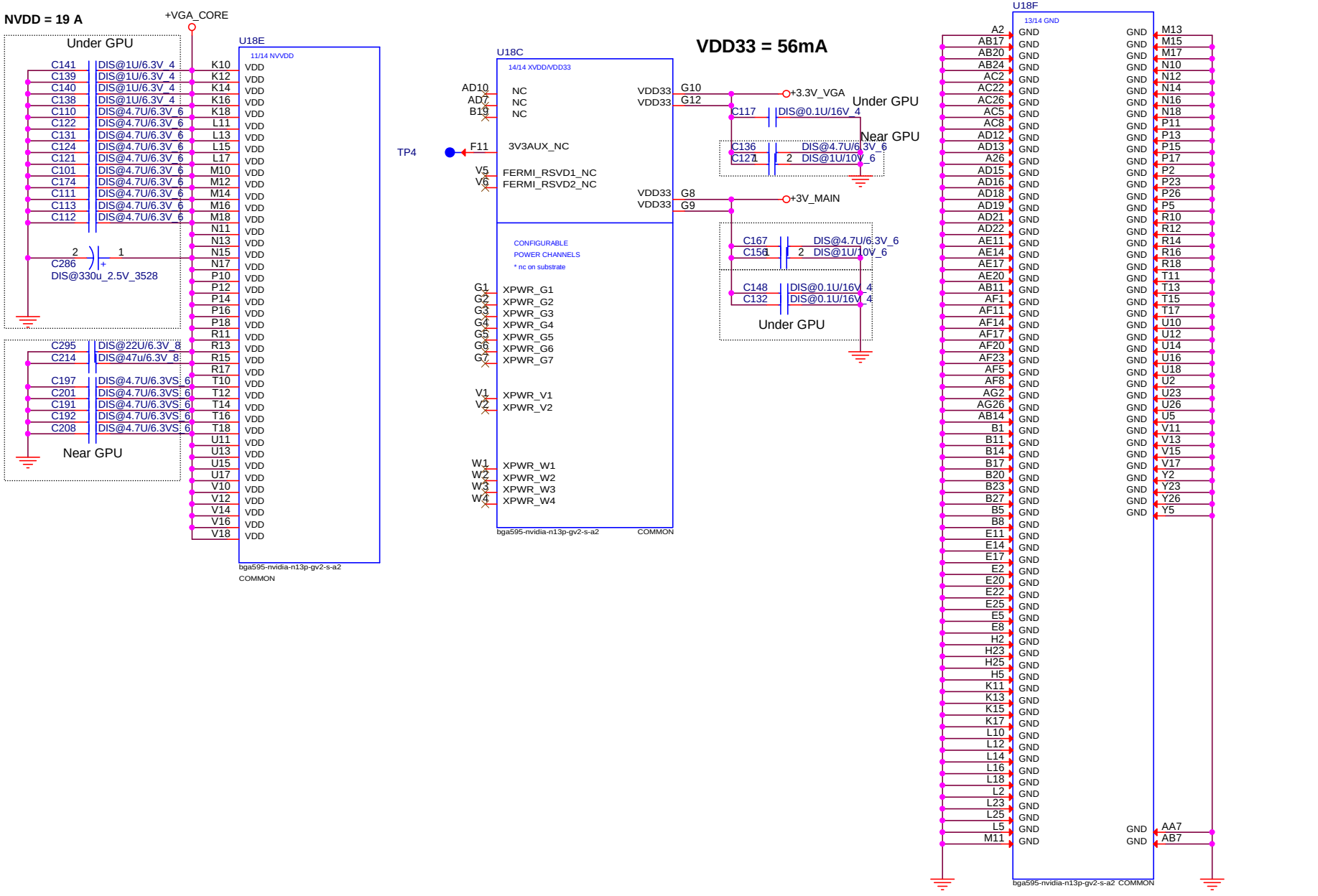

HP Restricted Secret

Quanta Computer Inc.

PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR Power/GND	1A

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CHANNEL A: 2048MB DDR3X16

[34] VMA_DQ[63..0]
[34] VMA_DM[7..0]
[34] VMA_WDQS[7..0]
[34] VMA_RDQS[7..0]

[33,34,35,52] +1.05V_VGA
[34,52] +1.5V_VGA

VRAM2 — DIS@VRAM _DDR3_256MX16
VRAM4 — DIS@VRAM _DDR3_256MX16
VRAM1 — DIS@VRAM _DDR3_256MX16
VRAM3 — DIS@VRAM _DDR3_256MX16

Should be 240 Ohms +-1%

R42 DIS@243/F_4
R393 DIS@243/F_4
R44 DIS@243/F_4
R392 DIS@243/F_4

+1.5V_VGA

R45 DIS@162/F_4

162_1% ohm
CS11622FB07 RES CHIP 162 1/16W +-1%(0402)
CS11622FB15 RES CHIP 162 1/16W +-1%(0402)

R35 DIS@1.33K/F_4
R34 DIS@1.33K/F_4
C43 DIS@0.1u/16V_4
R390 DIS@1.33K/F_4
R391 DIS@1.33K/F_4
C483 DIS@0.1u/16V_4

[34] FBA_CMD17 — TP1
[34] FBA_CMD1 — TP42
10/14 modify

R46 DIS@162/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R388 DIS@1.33K/F_4
R389 DIS@1.33K/F_4
C477 DIS@0.1u/16V_4
R32 DIS@1.33K/F_4
R33 DIS@1.33K/F_4
C41 DIS@0.1u/16V_4

C484 DIS@1u/10V_4
C476 DIS@1u/10V_4
C45 DIS@1u/10V_4
C491 DIS@1u/10V_4

C478 DIS@10u/6.3V_6
C496 DIS@1u/10V_4
C46 DIS@1u/10V_4
C40 DIS@1u/10V_4
C56 DIS@1u/10V_4
C486 DIS@1u/10V_4

C39 DIS@10u/6.3V_6
C52 DIS@1u/10V_4
C54 DIS@1u/10V_4
C48 DIS@1u/10V_4
C44 DIS@1u/10V_4
C49 DIS@1u/10V_4
C479 DIS@1u/10V_4
C59 DIS@1u/10V_4

C42 DIS@10u/6.3V_6
C485 DIS@10u/6.3V_6
C51 DIS@0.1u/16V_4
C493 DIS@0.1u/16V_4
C492 DIS@0.1u/16V_4
C487 DIS@0.1u/16V_4
C497 DIS@0.1u/16V_4

C47 DIS@10u/6.3V_6
C474 DIS@10u/6.3V_6
C480 DIS@0.1u/16V_4
C490 DIS@0.1u/16V_4
C498 DIS@0.1u/16V_4

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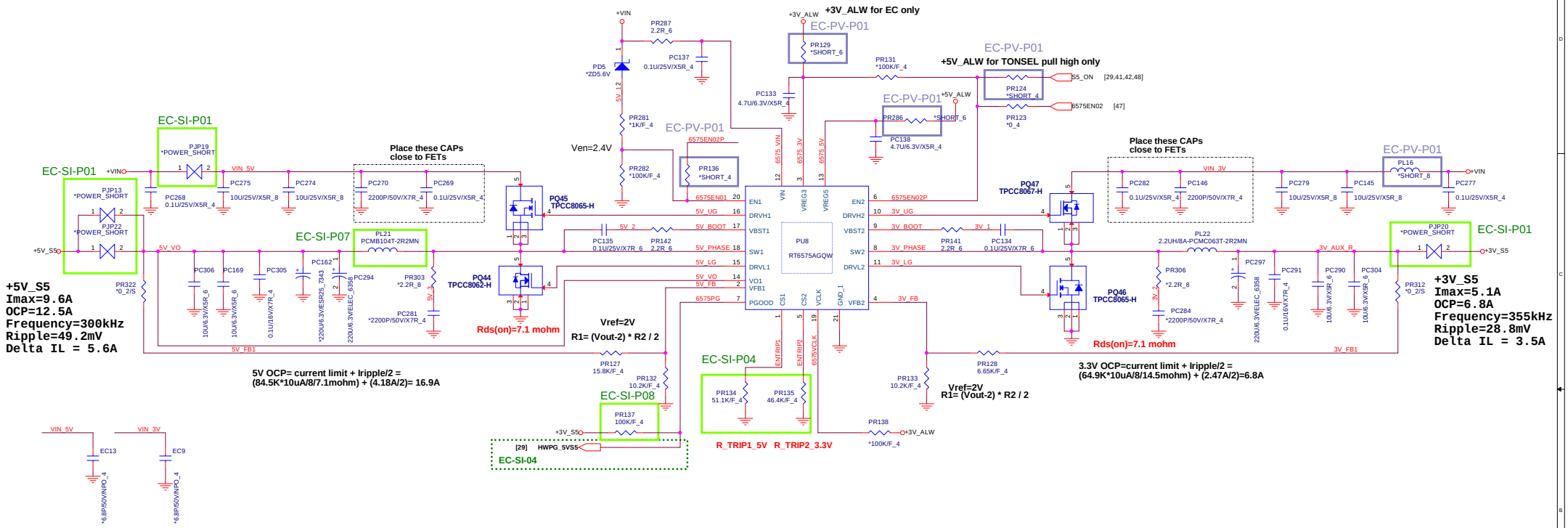
Quanta Computer Inc.
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	N16V-GMR DDR3 VRAM	1A

Date: Wednesday, March 09, 2016 Sheet 38 of 58



L/S Mosfet parameter

MOSFET	Package	ID (Ta=25C)	Rds_on_max
TPCC8067-H	DFN3x3	9A	26m
TPCC8062-H	DFN3x3	27A	7.1m

Power On sequencing

EN0	ENC	REF	VREG3	VREG5	SMPS1	SMPS2
LOW	LOW	OFF	OFF	OFF	OFF	OFF
> 2.4V	LOW	ON	ON	ON	OFF	OFF
> 2.4V	> 2.4V	ON	ON	ON	ON	ON

HP Restricted Secret

Quanta Computer Inc.
PROJECT: HP-Hawaii

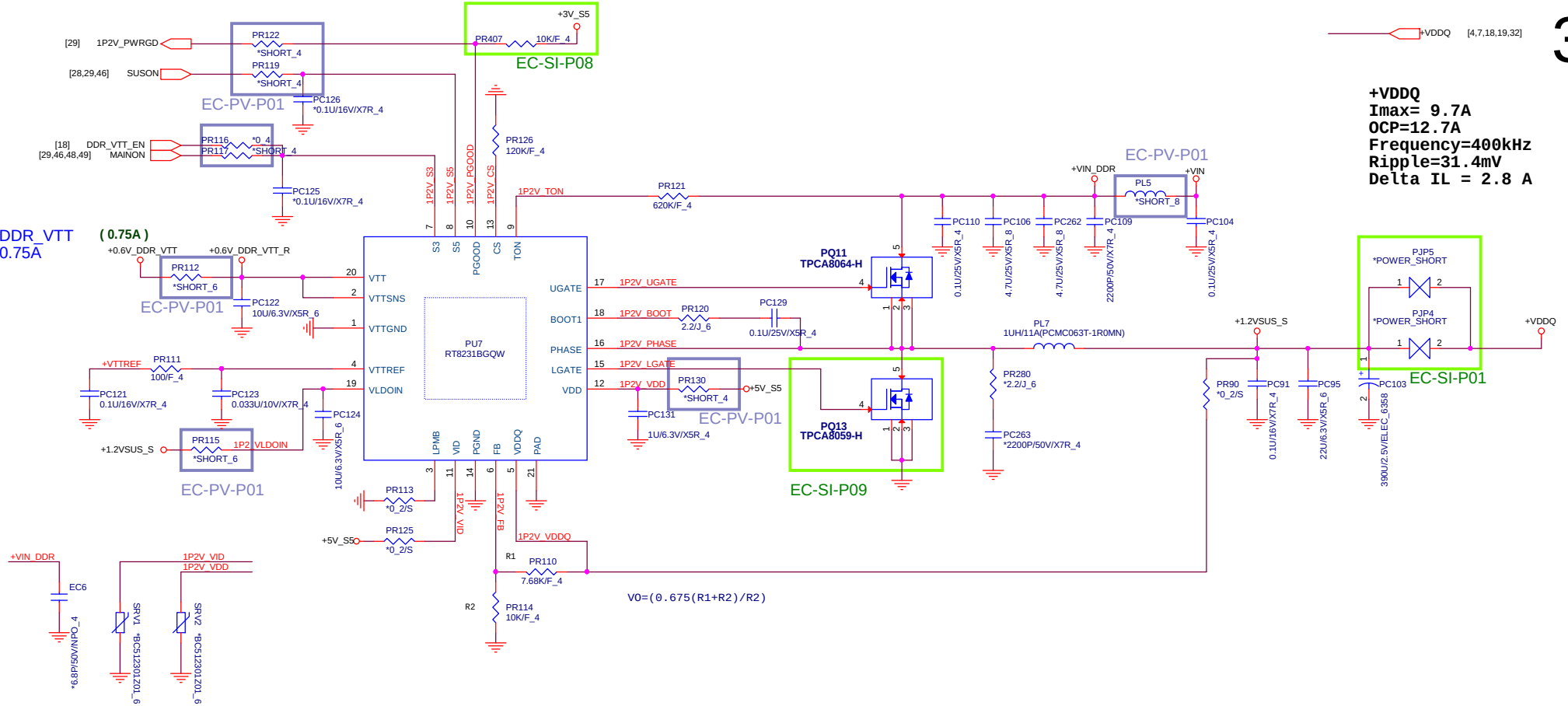
Size	Document Number	Rev
Custom	System +3V_S5/+5V_S5	1A

Date: Wednesday, March 09, 2016 Sheet 39 of 58

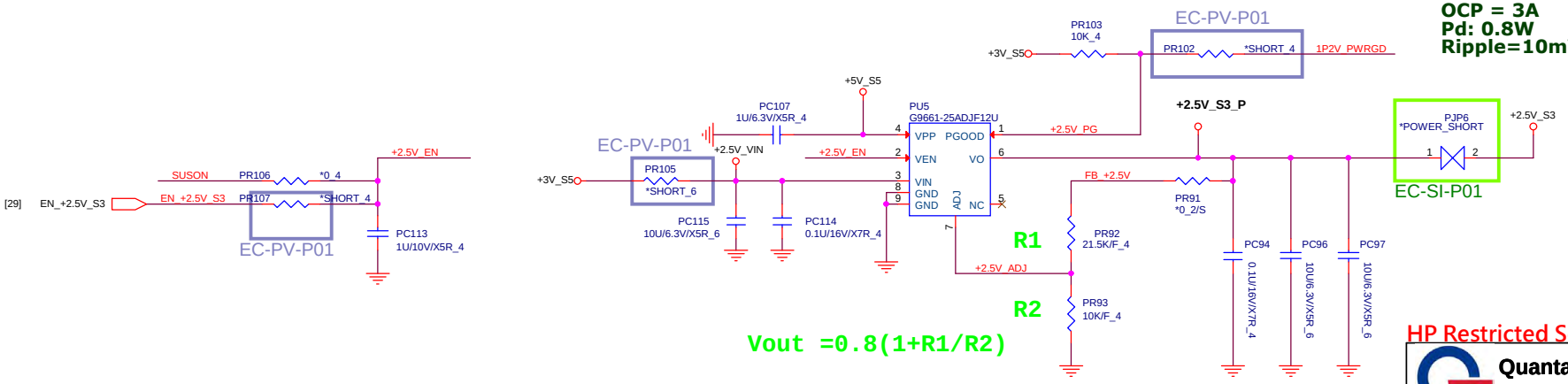
+VDDQ [4,7,18,19,32]

+VDDQ
Imax= 9.7A
OCP=12.7A
Frequency=400kHz
Ripple=31.4mV
Delta IL = 2.8 A

+0.6V_DDR_VTT (0.75A)
PEAK :0.75A



+2.5V_S3 +/- 5%
Imax = 1A
OCP = 3A
Pd: 0.8W
Ripple=10mV



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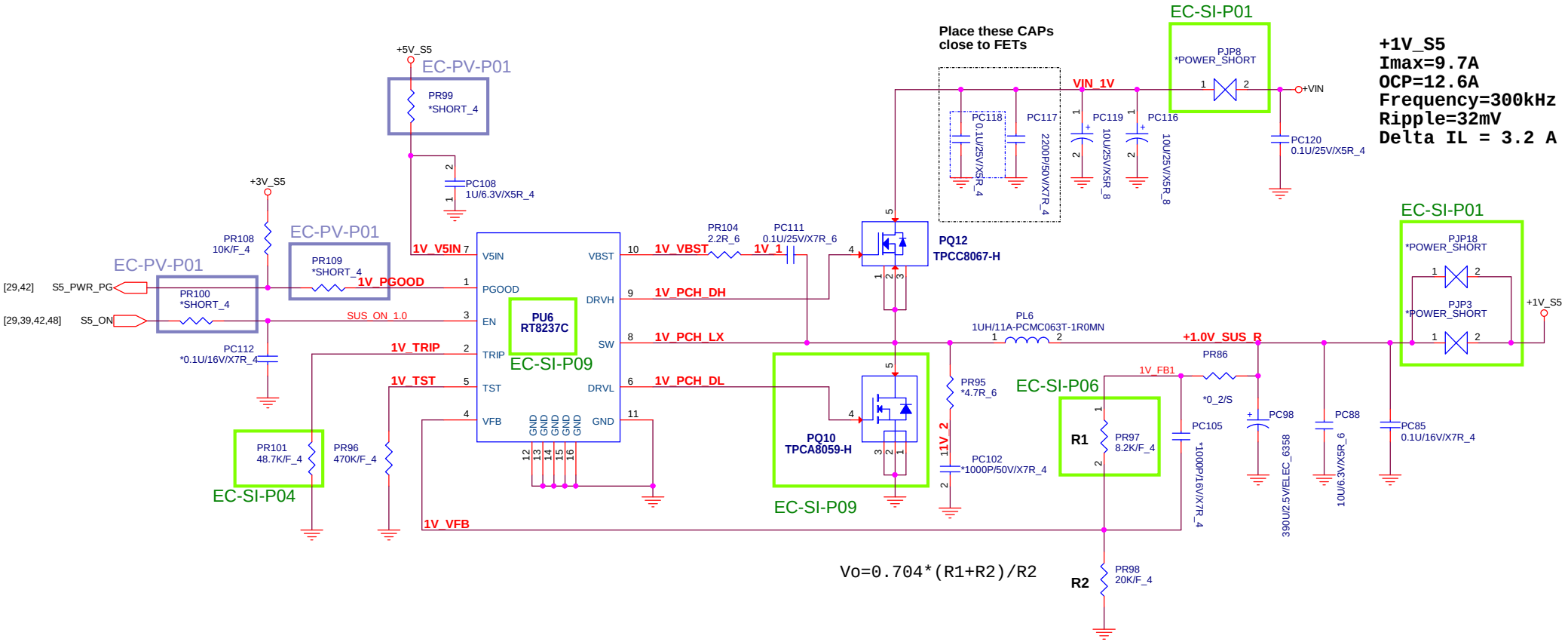
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DDR4 +VDDQ/+2.5V_S3	1A
Date: Wednesday, March 09, 2016	Sheet 40 of 58	



Quanta Computer Inc.

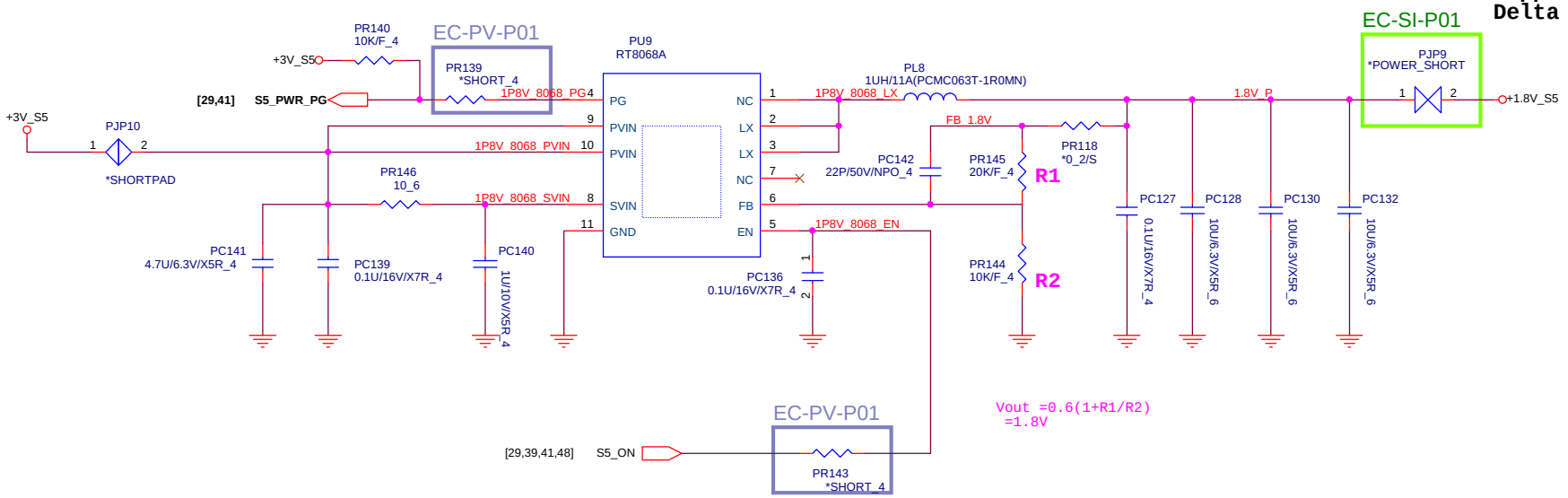
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	+1V_S5	1A

Date: Wednesday, March 09, 2016 Sheet 41 of 58

V1P8A (RT8068A)

+1.8V_S5
Imax=1.2A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A



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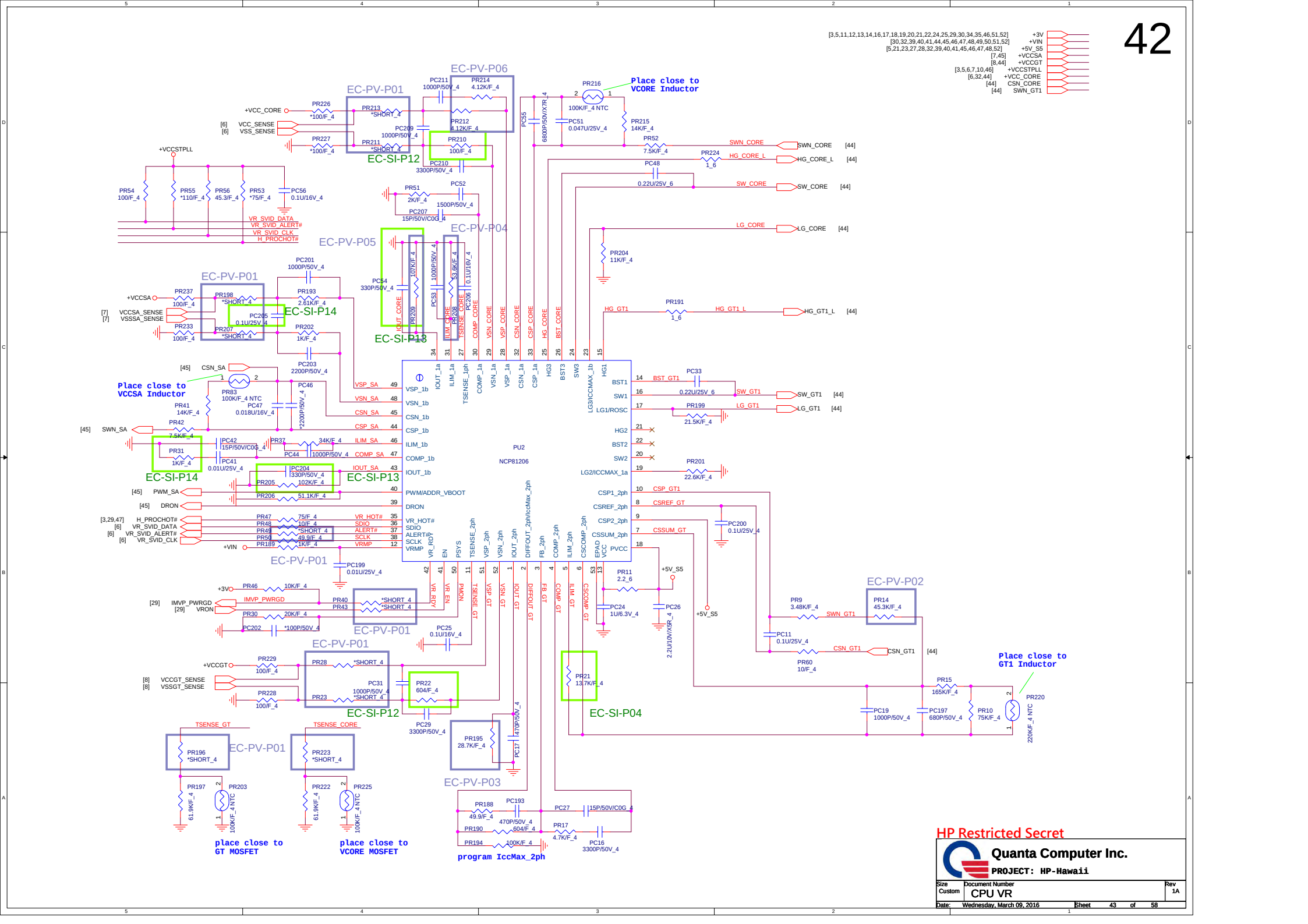
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	+1.8V_S5	1A

Date: Wednesday, March 09, 2016 Sheet 42 of 58



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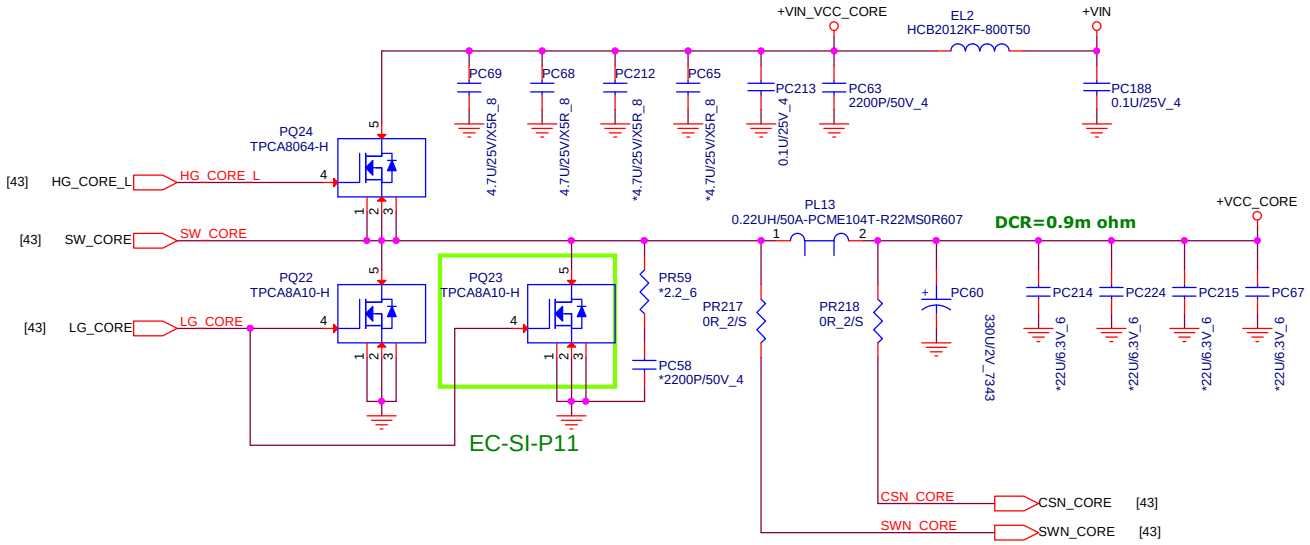
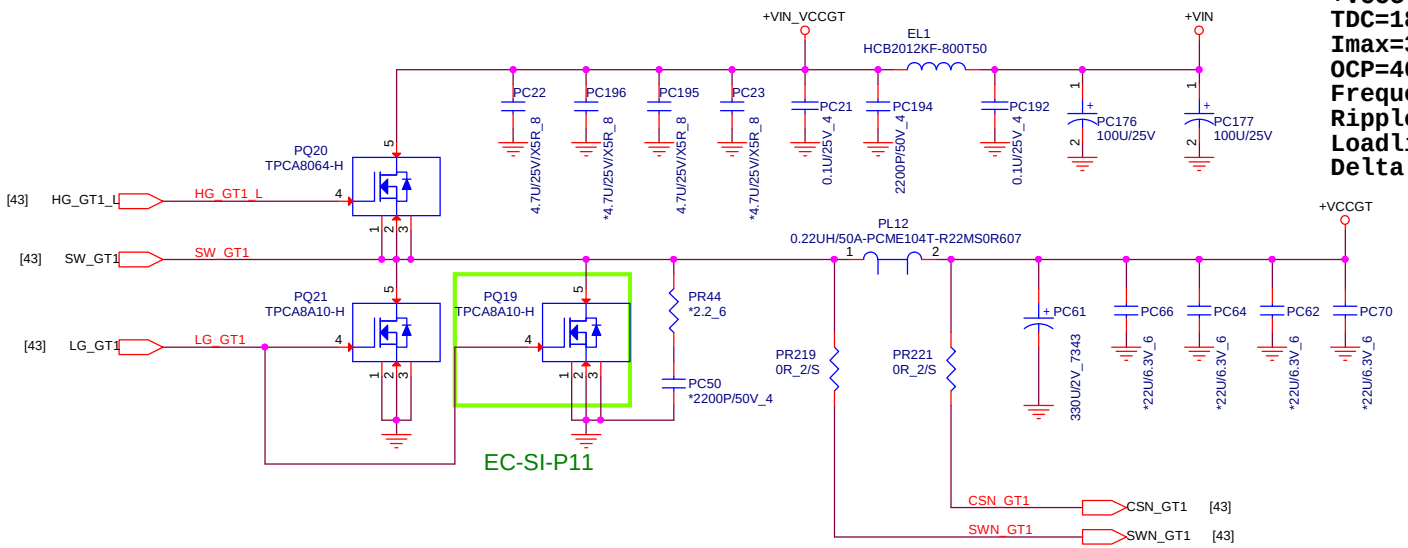
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	CPU VR	1A

Date: Wednesday, March 09, 2016 Sheet 43 of 58



+VCC_CORE
TDC=21A
Imax=29A
OCP=36A
Frequency=450kHz
Ripple=13mV
Loadline: -2.4m ohm
Delta IL = 9.6A



+VCCGT
TDC=18A
Imax=31A
OCP=40A
Frequency=450kHz
Ripple=13mV
Loadline: -3.1m ohm
Delta IL = 9.6A

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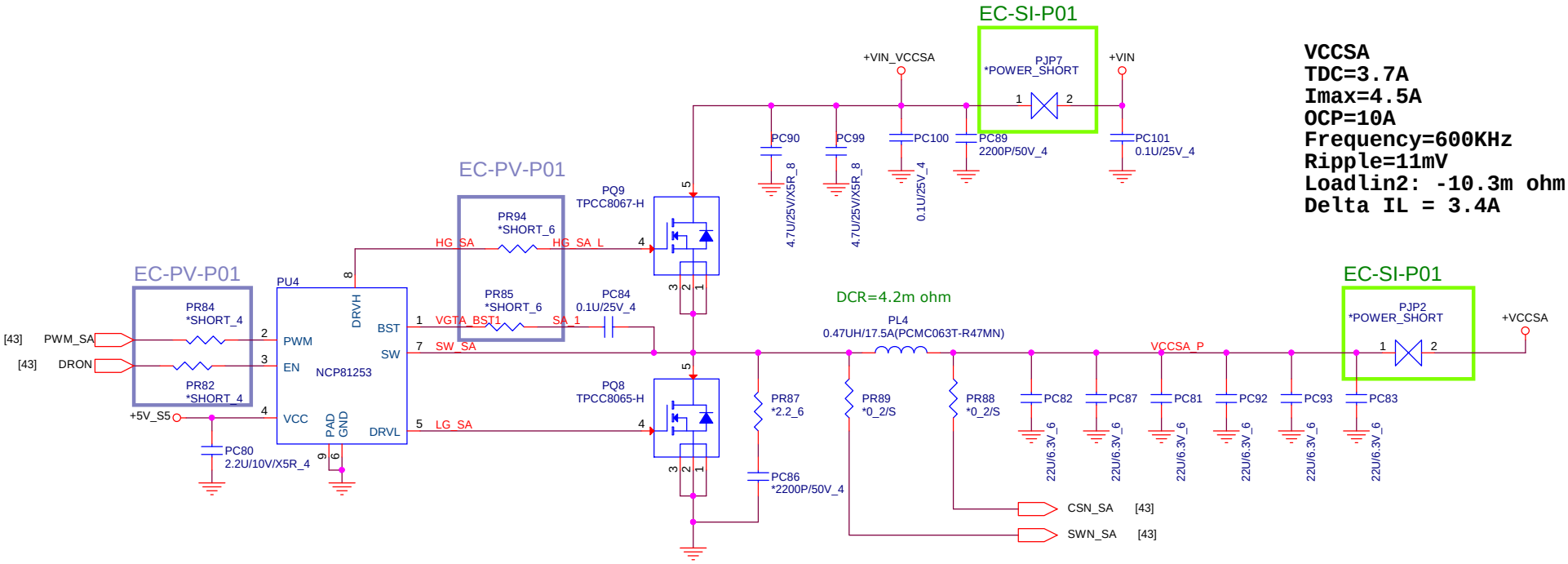
PROJECT: HP-Hawaii

Size	Document Number	Rev
B	CPU +VCC_CORE/+VCCGT	1A

Date: Wednesday, March 09, 2016 Sheet 44 of 58

[30,32,39,40,41,43,44,46,47,48,49,50,51,52] +VIN
[5,21,23,27,28,32,39,40,41,43,46,47,48,52] +5V_S5
[7,43] +VCCSA

VCCSA



VCCSA
TDC=3.7A
Imax=4.5A
OCP=10A
Frequency=600KHz
Ripple=11mV
Loadlin2: -10.3m ohm
Delta IL = 3.4A

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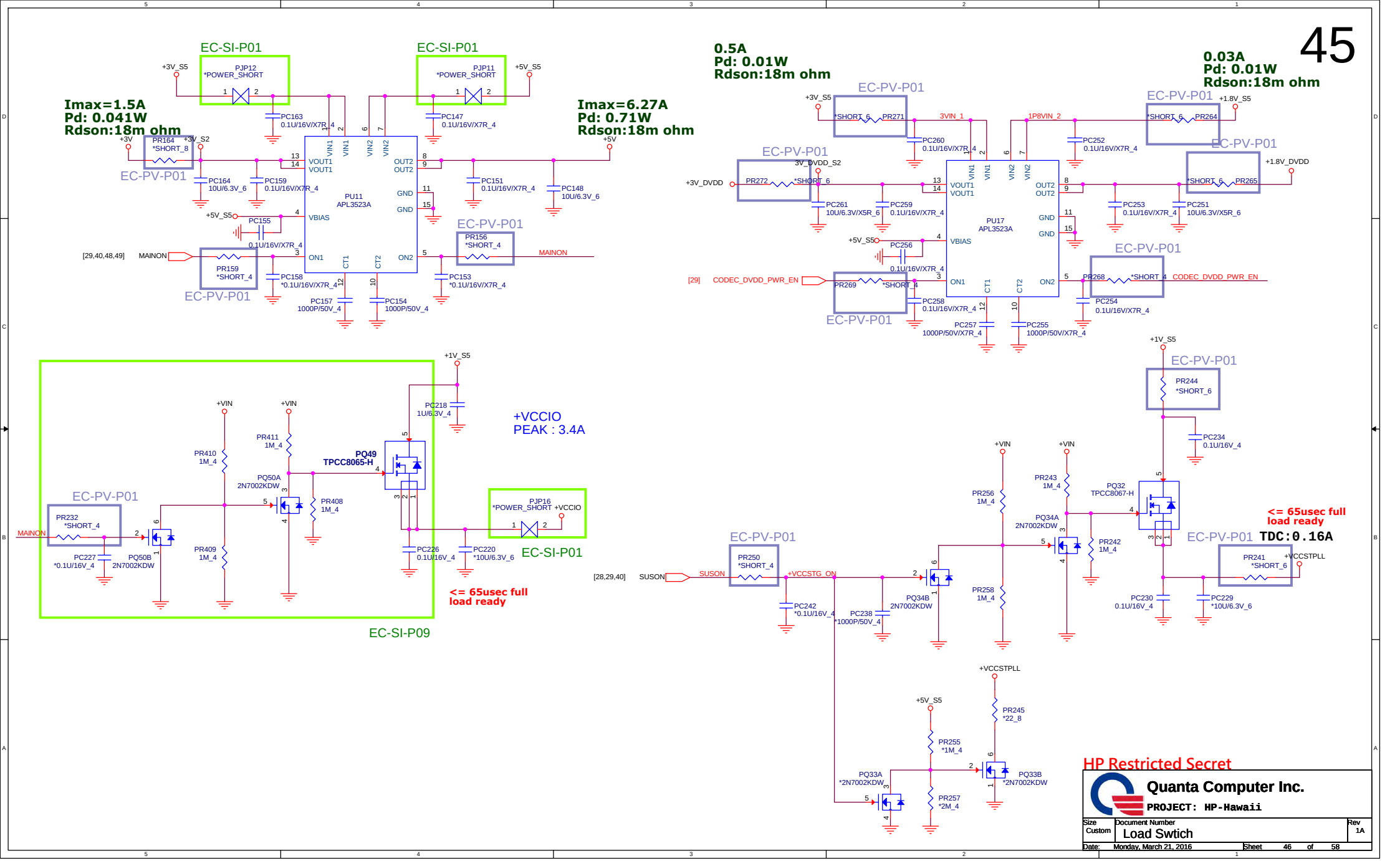
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	CPU +VCCSA	1A
Date: Wednesday, March 09, 2016	Sheet 45 of 58	


EC-SI-P01
EC-SI-P01
Imax=1.5A
Pd: 0.041W
Rdson:18m ohm
Imax=6.27A
Pd: 0.71W
Rdson:18m ohm
0.5A
Pd: 0.01W
Rdson:18m ohm
0.03A
Pd: 0.01W
Rdson:18m ohm
PU11
APL3523A
PU17
APL3523A
EC-PV-P01
+VCCIO
PEAK : 3.4A
PQ49
TPCC8065-H
<= 65usec full
load ready
EC-SI-P09
<= 65usec full
load ready
TDC:0.16A
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PROJECT: HP-Hawaii
Load Swtich
Monday, March 21, 2016
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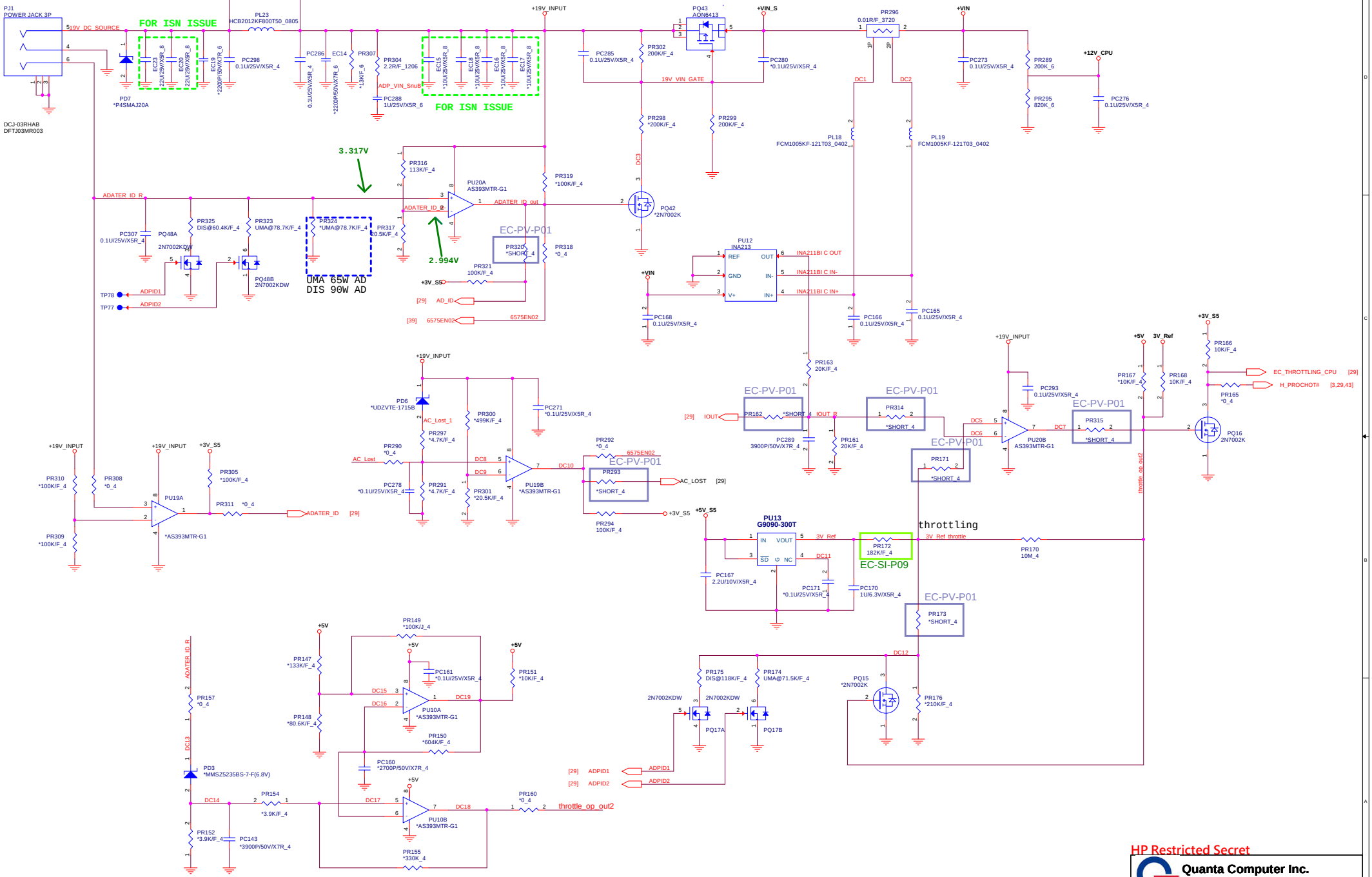
Id=16A
Qg=41~58nC
Rdson=6.9~8.5mOHM



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PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	DC IN	1A
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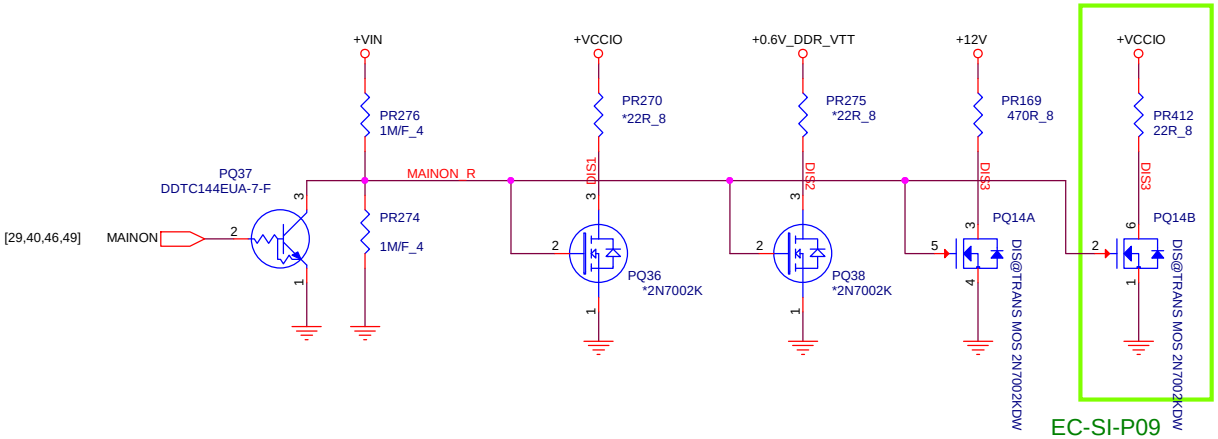
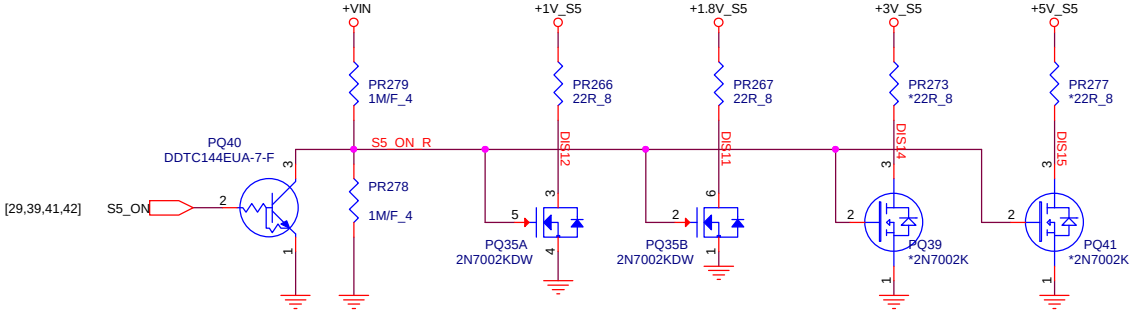
CONFIDENTIAL

DISCHARGE





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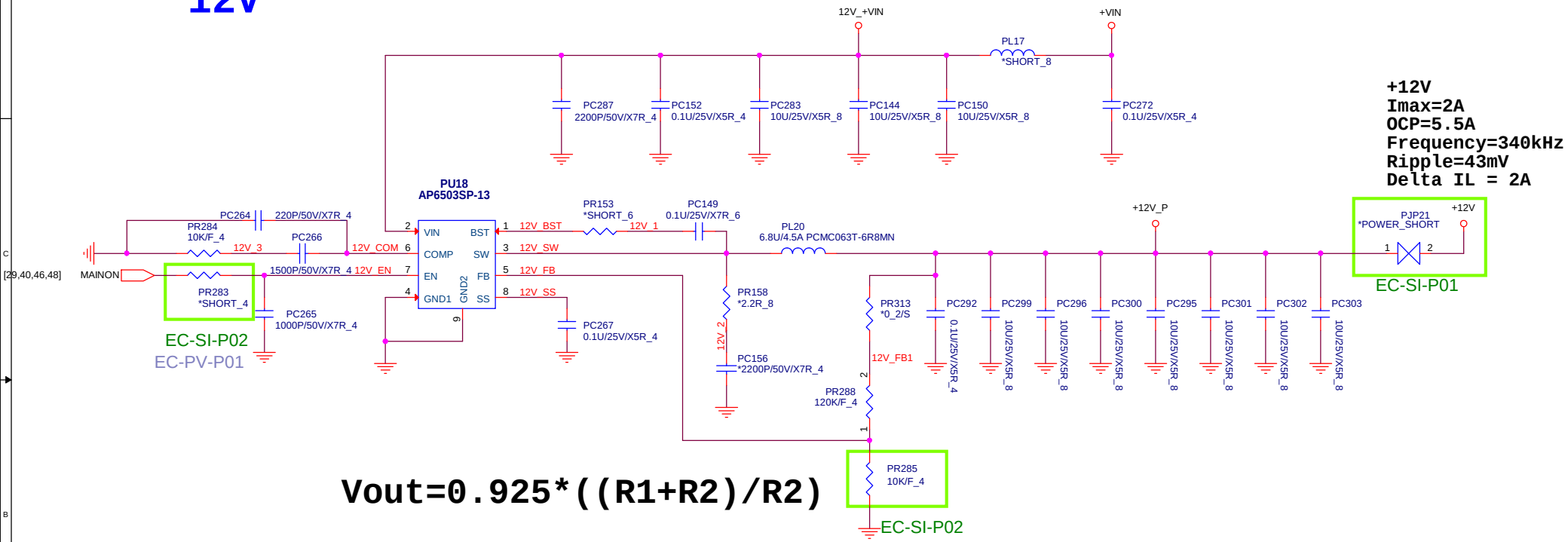
PROJECT: HP-Hawaii		
Size: B	Document Number: Discharge	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 48 of 58	

12V



+12V
Imax=2A
OCP=5.5A
Frequency=340kHz
Ripple=43mV
Delta IL = 2A

Vout=0.925*((R1+R2)/R2)

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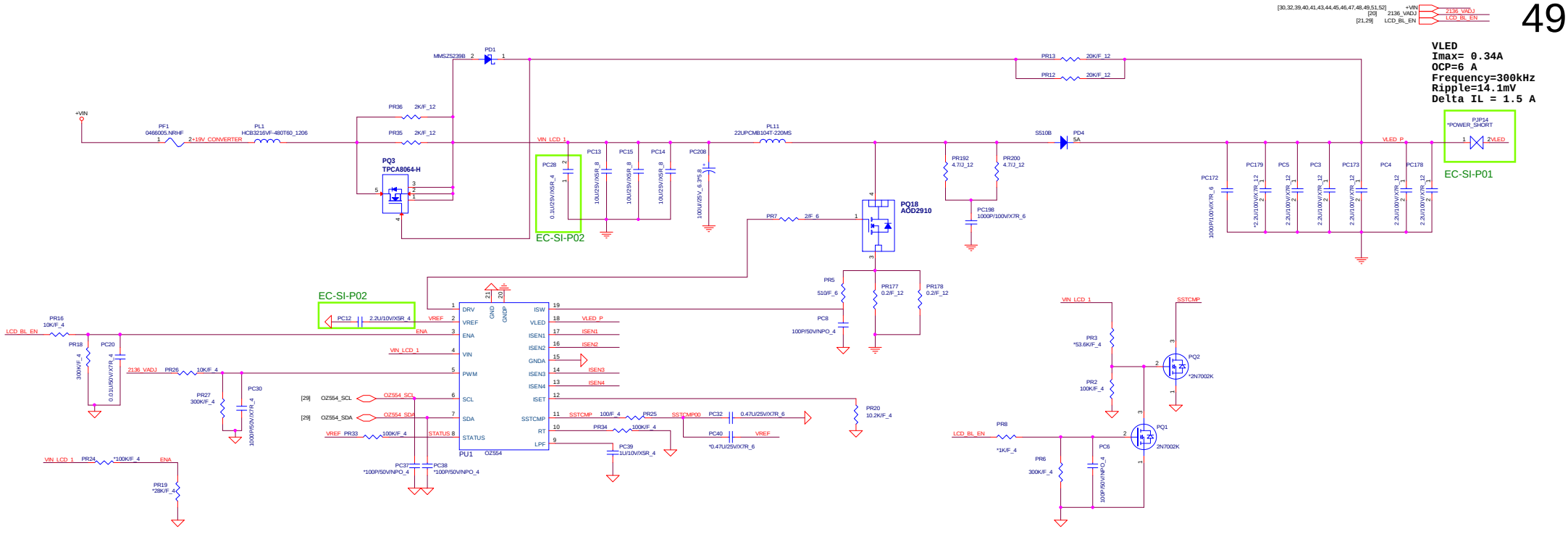
Quanta Computer Inc.		
PROJECT: HP-Hawaii		
Size: B	Document Number: +12V	Rev: 1A
Date: Wednesday, March 09, 2016	Sheet 49 of 58	



PANEL_SIZE Table

PANEL_Size[1:0]	Size
00	19.5/9.53"
01	21.5"
10	23.6"/23.8"
11	Reserve

19.45" /19.53" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M200HJJ-L20 FHD
1101	AUO M195RTN01.0 HD+
1100	LGD LM195WD1-TLA1 HD+
1010	Reserve

21.5" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M215HJK-L3B FHD eDP
1101	SDC LTM215HL01 FHD
1100	LGD LM215WF3-SLN1 FHD
1011	Reserve

23.6" /23.8" PANEL_ID Table

PANEL_ID[3:0]	Panel model
1111	No Connect
1110	INX M236HJK-L5B FHD eDP
1101	AUO M238HAN01.0 FHD
1100	LGD LM238WF1-SLE1 FHD
1011	SDC LTM238HL02 FHD
1010	Reserve

Panel_ID[3:0] = 1111 & Panel_Size[1:0] = 11 is reserved for cabling detection by "No connection".

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Size	Document Number	Rev
Custom	OZ554	1A

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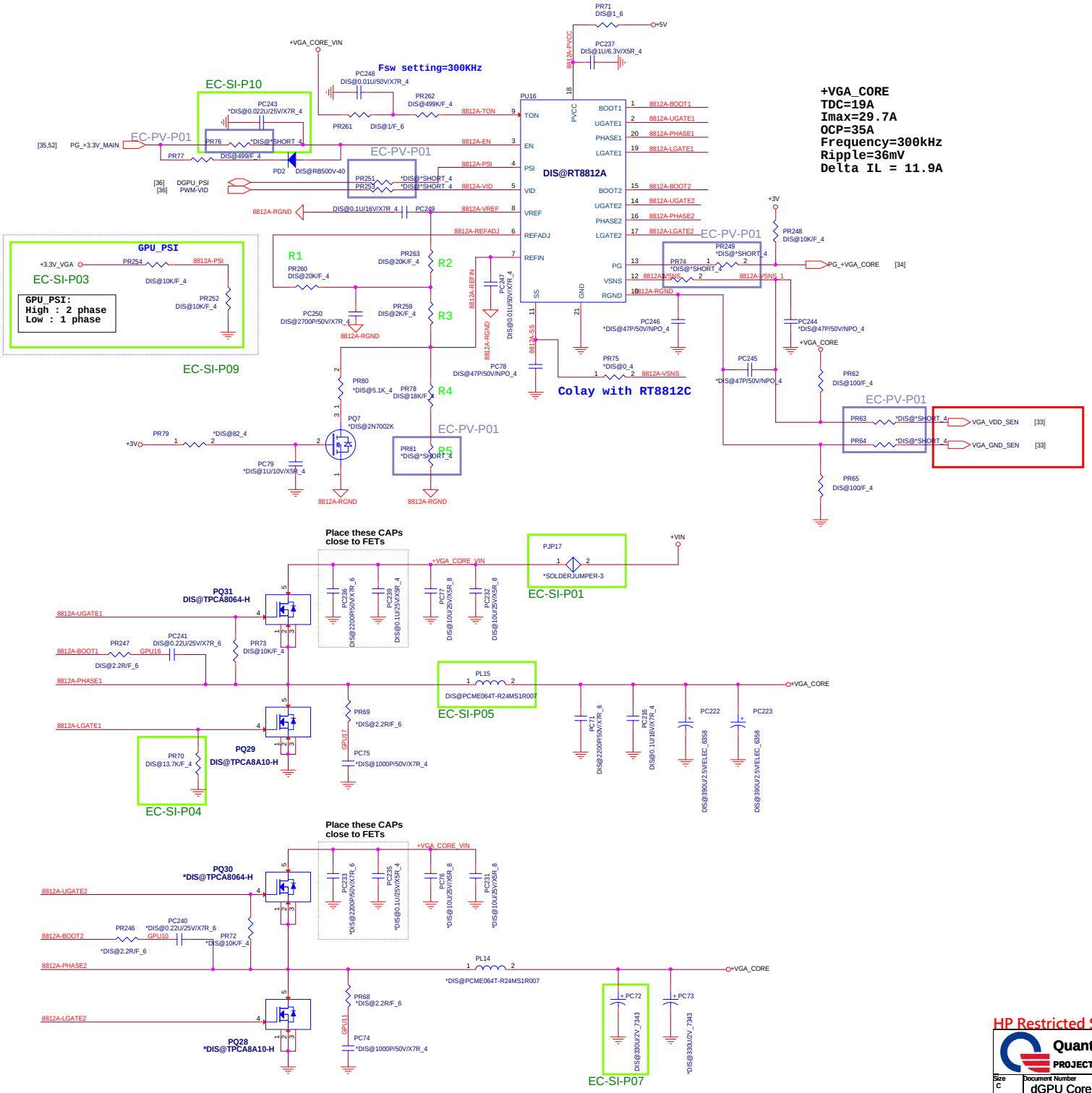

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Size	Document Number	Rev
C	dGPU Core	1A

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VGA POWER

51

AO6402A
Rdson=24m ohm
Imax=0.2A
Pd: 0.01W

+1.05V_VGA
Imax=1.5A
OCP=4A
Frequency=1MHz
Ripple=12mV
Delta IL = 0.8A

+1.5V_VGA
Imax=4.7A
OCP=8A
Frequency=500KHz
Ripple=22mV
Delta IL = 2.8A

+1.05V VGA

40mil

V0=0.6*(R1+R2)/R2

VREF=0.604V

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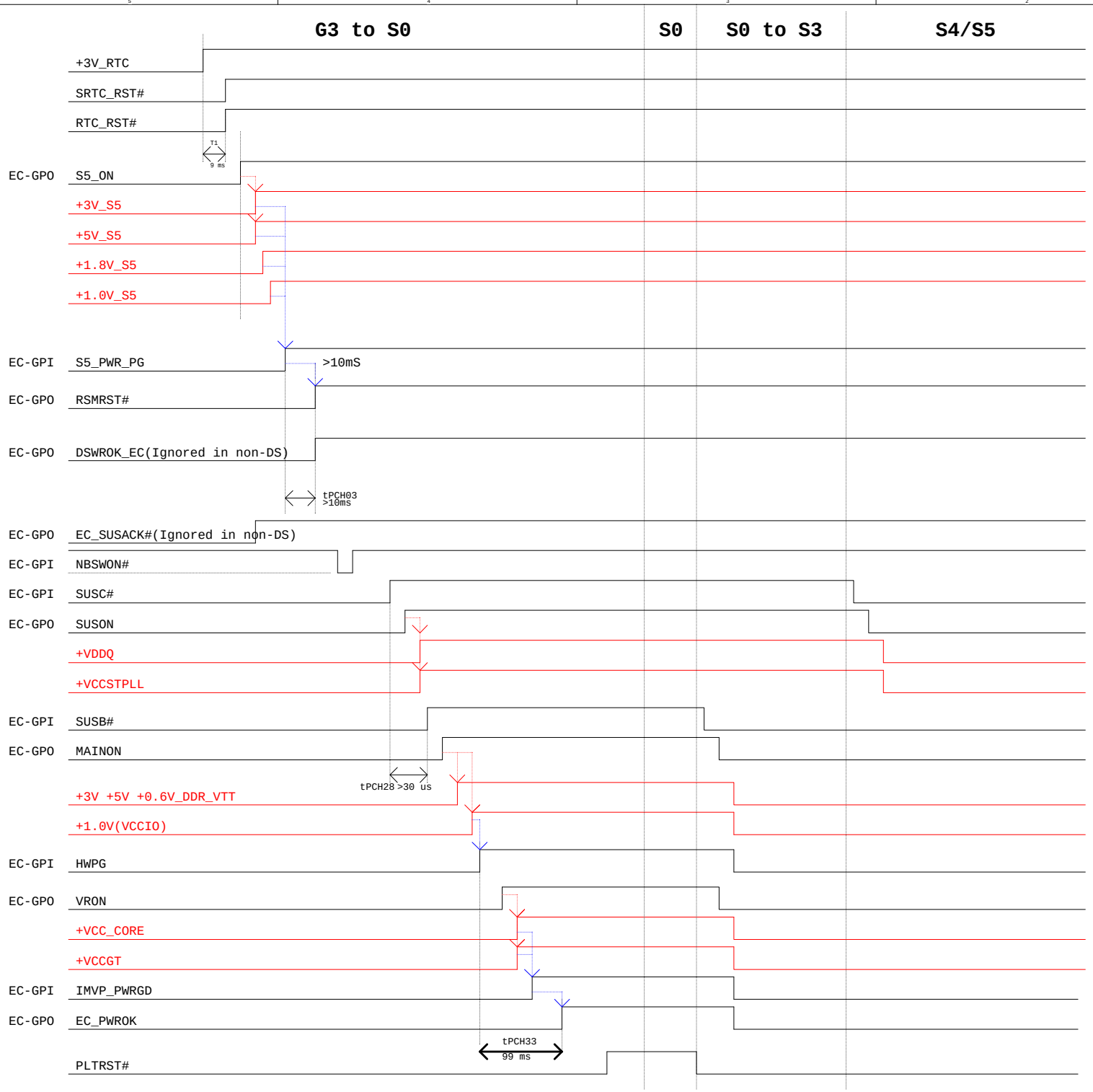
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	dGPU +1.05V/+1.5V	1A
Date: Wednesday, March 09, 2016	Sheet 52 of 58	



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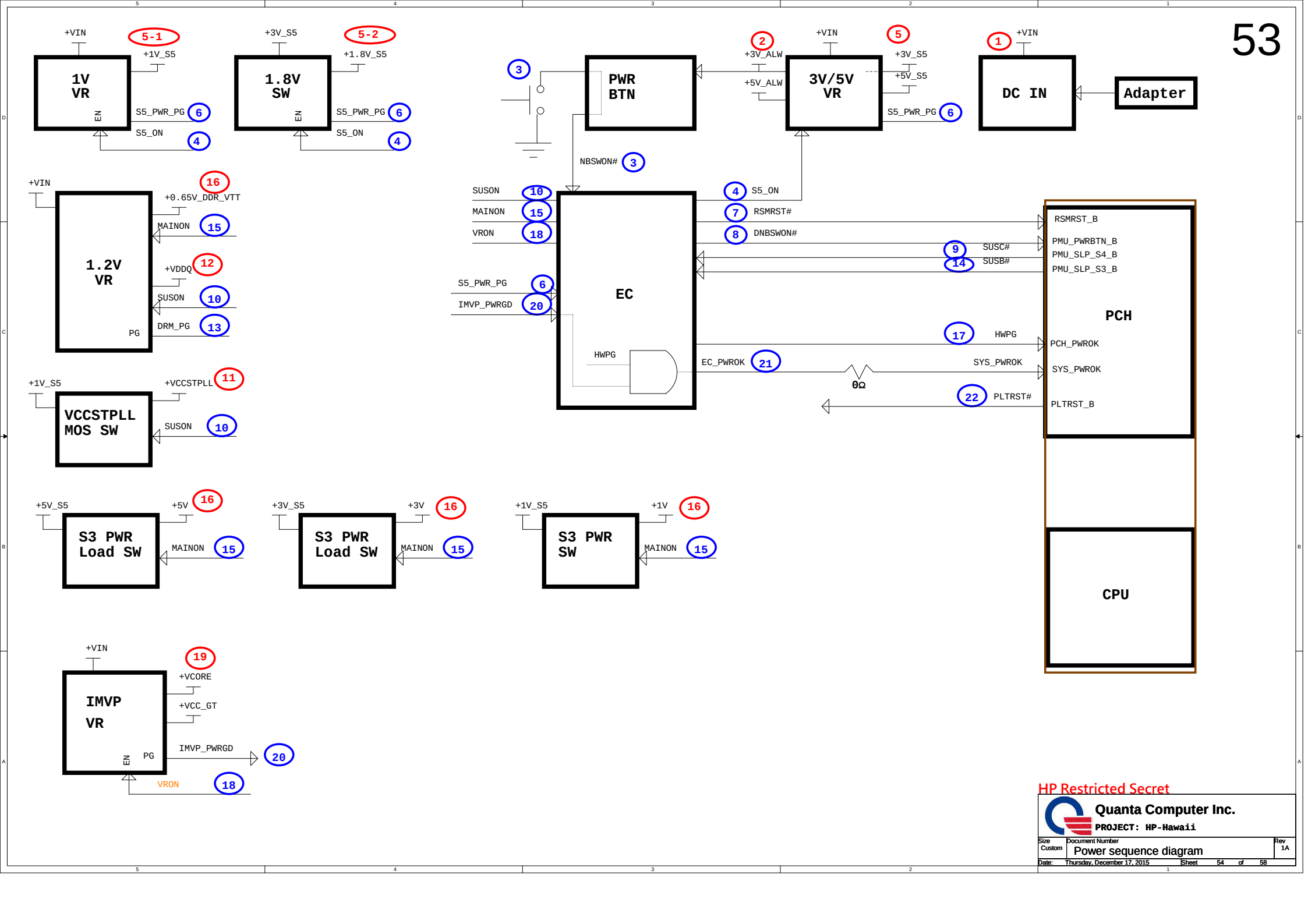
PROJECT: HP-Hawaii

Size	Document Number	Rev
C	Power Sequence	1A

Date: Thursday, December 17, 2015 Sheet 53 of 58



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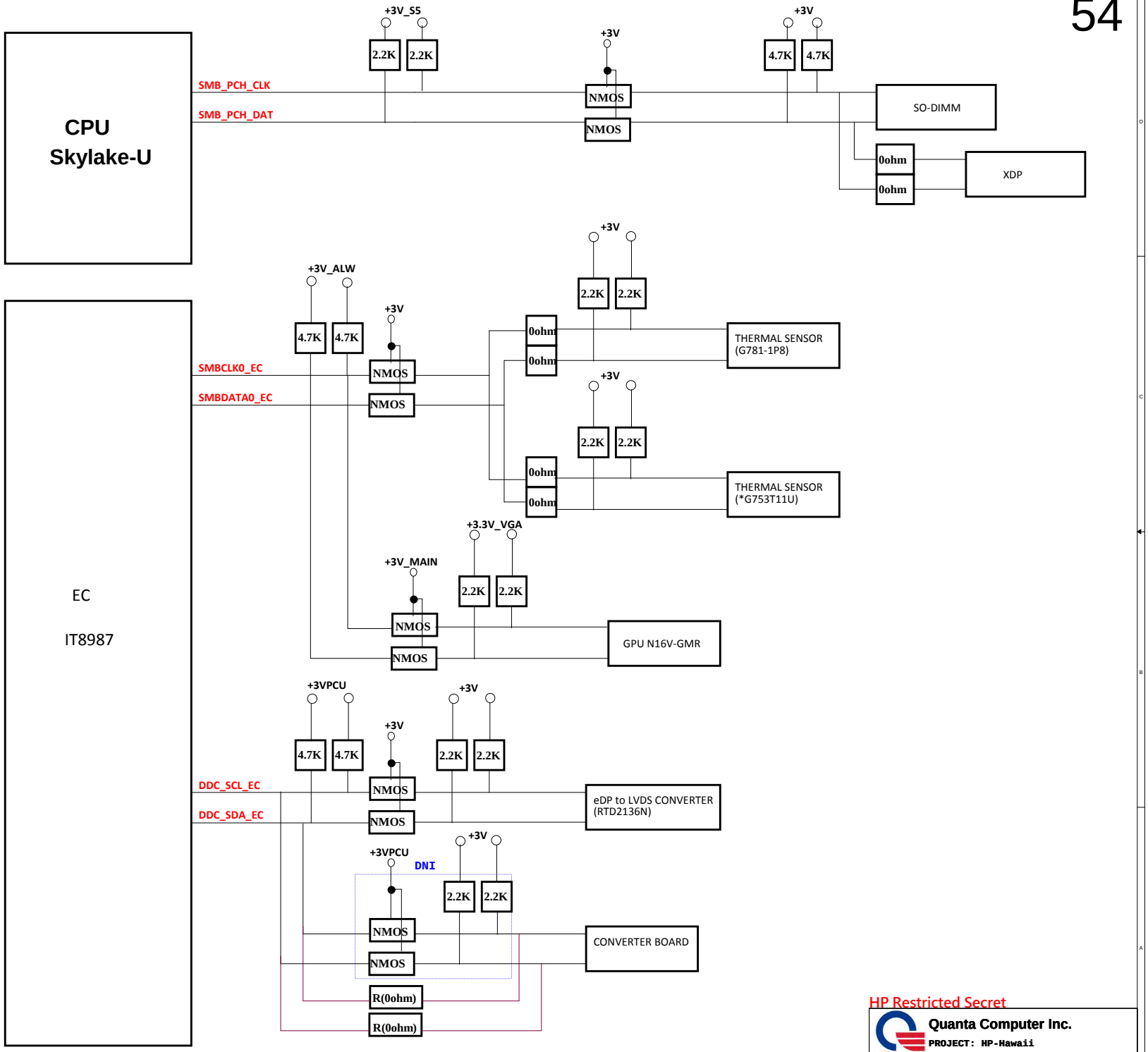
PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	Power sequence diagram	1A

Date: Thursday, December 17, 2015 Sheet 54 of 58



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PROJECT: HP-Hawaii

Size	Document Number	Rev
Custom	SMBUS map	1A

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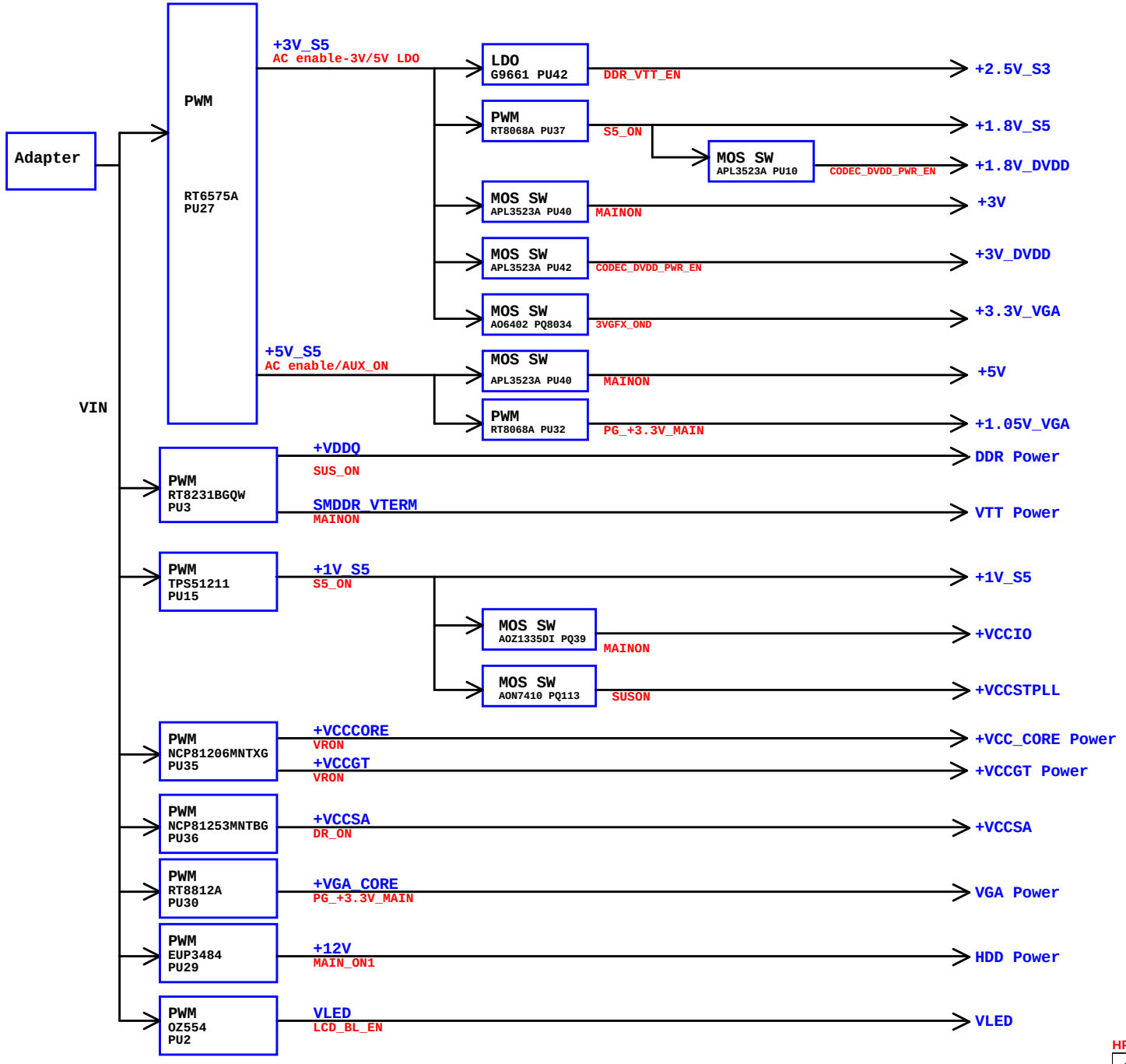
Power Delivery Map



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PROJECT: HP-Hawaii

Size	Document Number	Rev
C	Power Delivery Map	1A

Date: Thursday, January 28, 2016 Sheet 56 of 58

N91 EE Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-01	17,18	Unstuff C205/C213 for DDR4 Issue	C205,C213
EC-SI-02	21	Change HDMI HPD signal from low active to high active	Q38,R638,R639
EC-SI-03	21	Modify Q37 MOSFET gate power source from +5V to +3V	Q37
EC-SI-04	28	Swap EC GPIO for reserving 2nd fan control	
EC-SI-05	22	Separate L/R channels for spkeaker connector	CN26,CN27
EC-SI-06	20	Add ESD protection for CCD	
EC-SI-07	29	Reserve 2nd FAN	
EC-SI-08	49	Reserve 100pF for CN15 (EMI suggestion)	
EC-SI-09	31	Add 2 GND pad for EMI	
EC-SI-10	25	Change ODD connector	CN21
EC-SI-11	26	Change connector of card reader daughter board	CN24
EC-SI-12	13,34	Change load cap for 32.768K/24M/27M due to vendor suggest	
EC-SI-13	All	Stuff EMC/ESD/RF materials	
EC-SI-14	35	Unstuff R437 for correct PSI setting	R437
EC-SI-15	22	Change AL7/AL8/AL9/AL11 as 0ohm from Realtek suggest	AL7,AL8,AL9,AL11

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-01	All	Change 0ohm resistor to be short pad	
EC-PV-02	27	Remove reserved CMC of USB3.0	L28,L29,L30,L33

N91 Power Schematic DB to SI Change List

EC#	Page	Description	Part Affected
EC-SI-P01	38~51	Change default open to default short	PJP1~PJP22
EC-SI-P02	48,49,51	Downsize components	PR283, PR285, PC12, PC28, PC184, PC185, PC174, PL3
EC-SI-P03	50, 51	Correct connection	
EC-SI-P04	38,40,42,50	Fine tune OCP function	PR134, PR135, PR101, PR21, PR70
EC-SI-P05	50	Change choke for transient	PL15
EC-SI-P06	40,51	Fine tune offset voltage	PR97, PR186
EC-SI-P07	38, 50	Change components for ripple voltage	PL21, PC72
EC-SI-P08	38,39	Add components for PG function	PR137, PR122
EC-SI-P09	39,40,45~47,50,51	Change components for common part using	PU6, PQ10, PQ13, PQ14, PQ49, PQ50, PR408~PR412, PR254, PR252, PQ4, PQ5, PQ26, PR172
EC-SI-P10	50	Fine tune soft start	PR76, PC243
EC-SI-P11	43	Add components for Efficiency	PQ19, PQ23
EC-SI-P12	42	Fine tune DVID setting	PR210, PR22
EC-SI-P13	42	Fine tune Iout function	PR205, PR209, PC54, PC204
EC-SI-P14	42	Fine tune compensation	PR31, PC205

N91 EE Schematic SI to PV Change List

EC#	Page	Description	Part Affected
EC-PV-P01	All	Change 0ohm resistor to short pad	
EC-PV-P02	42	Fine tune +VCCGT load line	PR14
EC-PV-P03	42	Fine tune +VCCGT Iout function	PR195
EC-PV-P04	42	Fine tune Vcore OCP	PR208
EC-PV-P05	42	Fine tune Vcore Iout function	PR209
EC-PV-P06	42	Fine tune Vcore Loadline	PR212,PR214