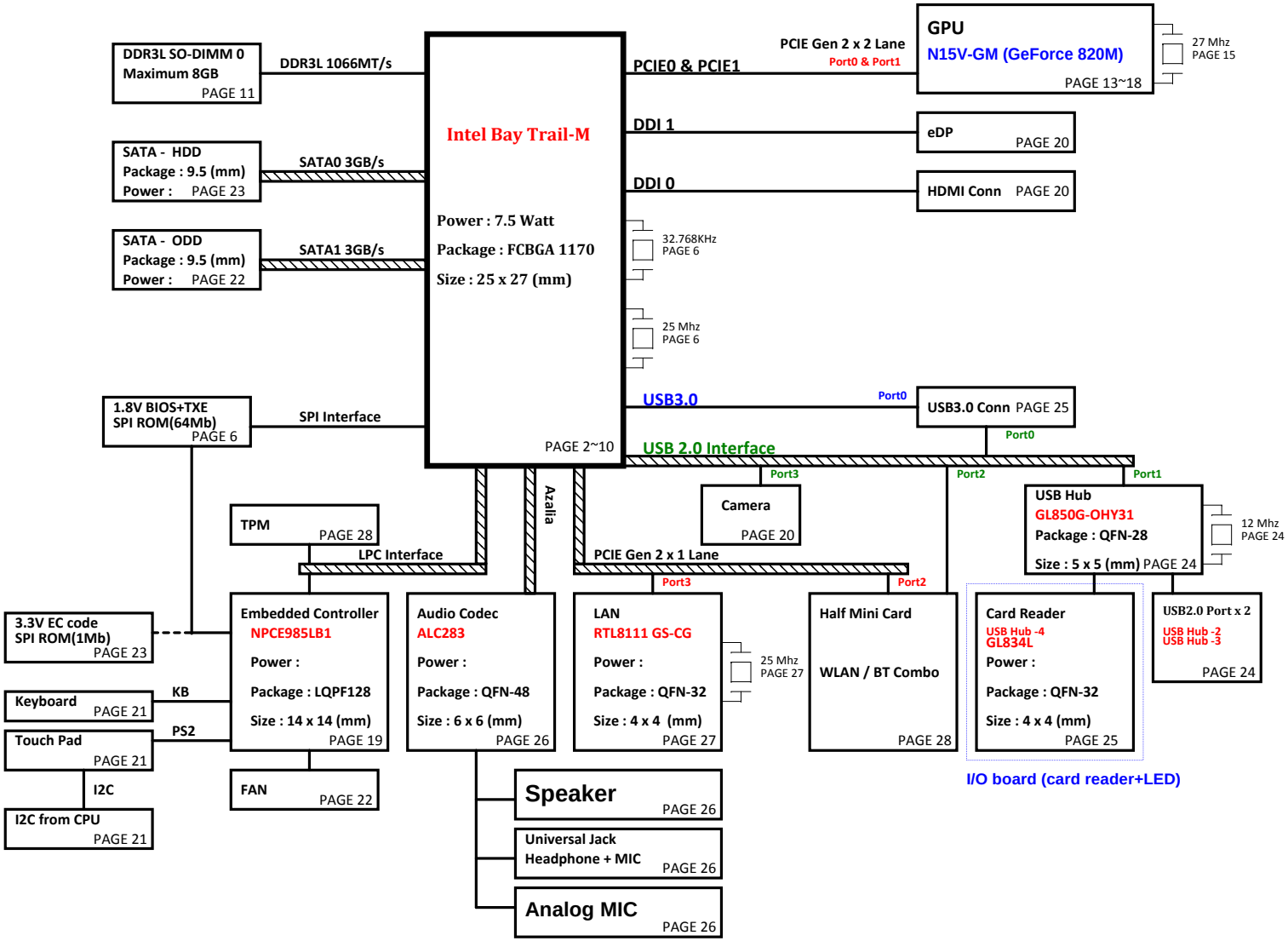
ZYL (17")
Intel Bay Trail-M Platform Block Diagram

PCB 6L STACK UP

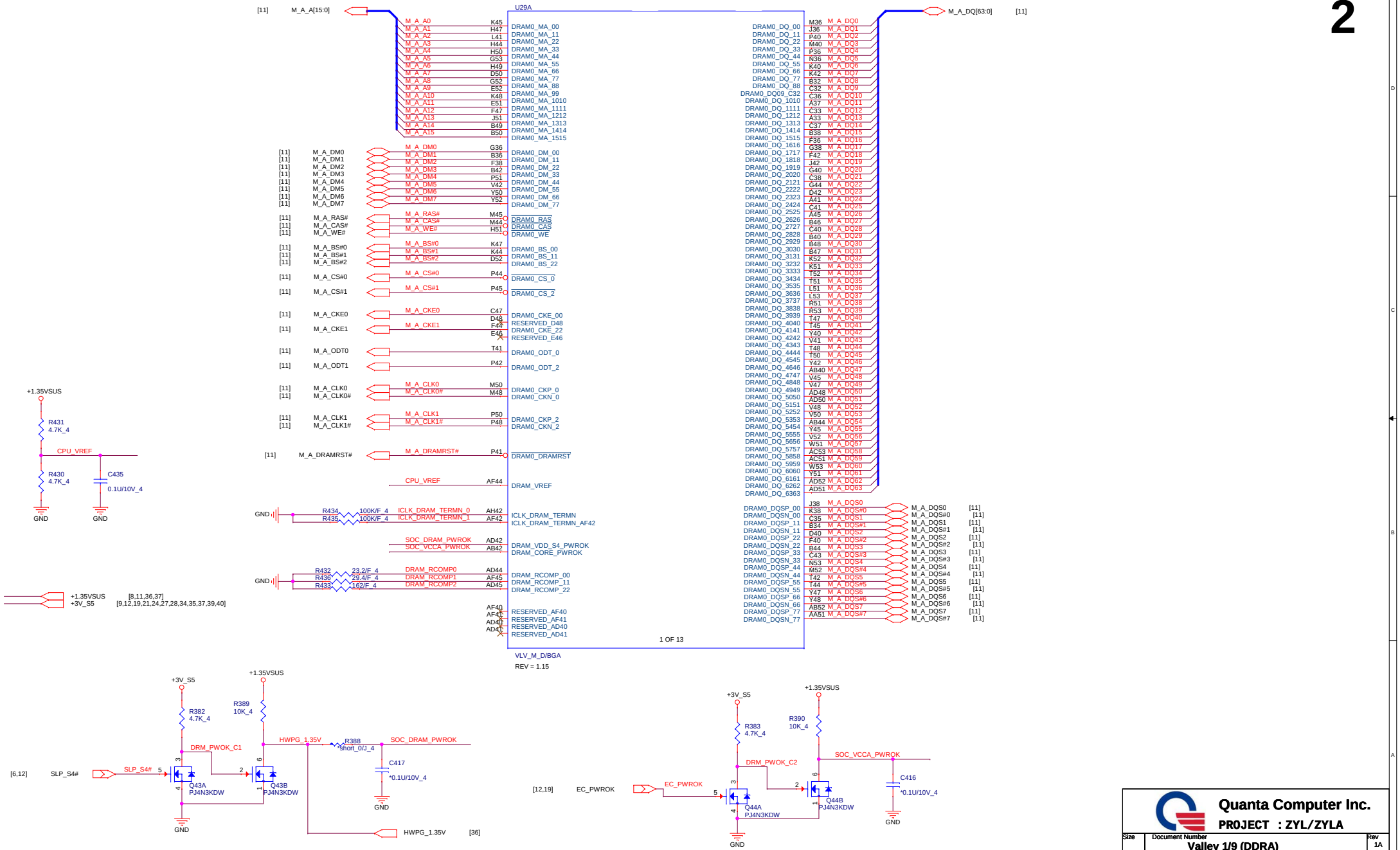
LAYER 1 : TOP
LAYER 2 : SVCC
LAYER 3 : IN1(High)
LAYER 4 : IN2(Low)
LAYER 5 : SGND
LAYER 6 : BOT



Quanta Computer Inc.
PROJECT : ZYL/ZYLA

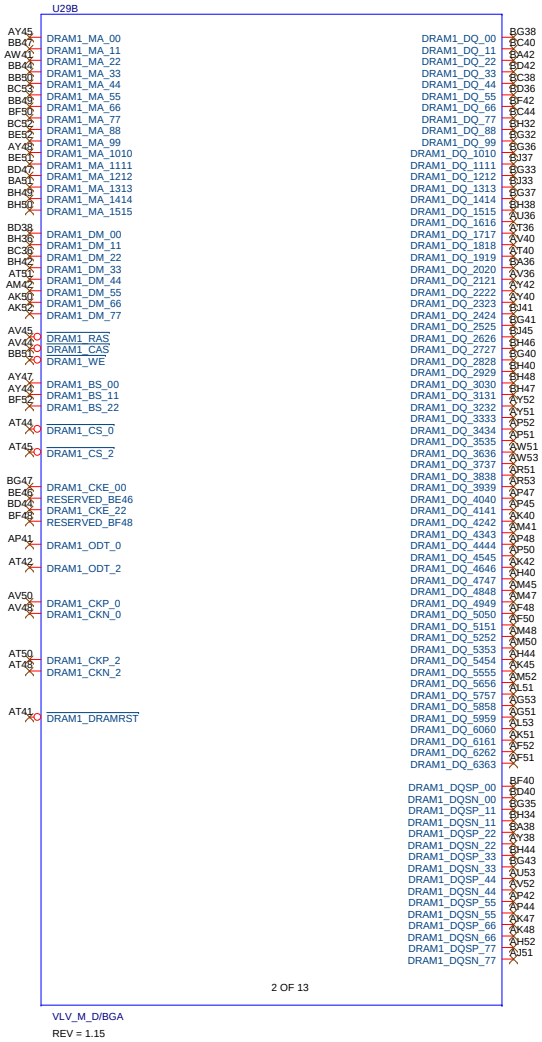
Size	Document Number	Rev
	Intel Block Diagram	1A

Date: Thursday, July 10, 2014 Sheet 1 of 44

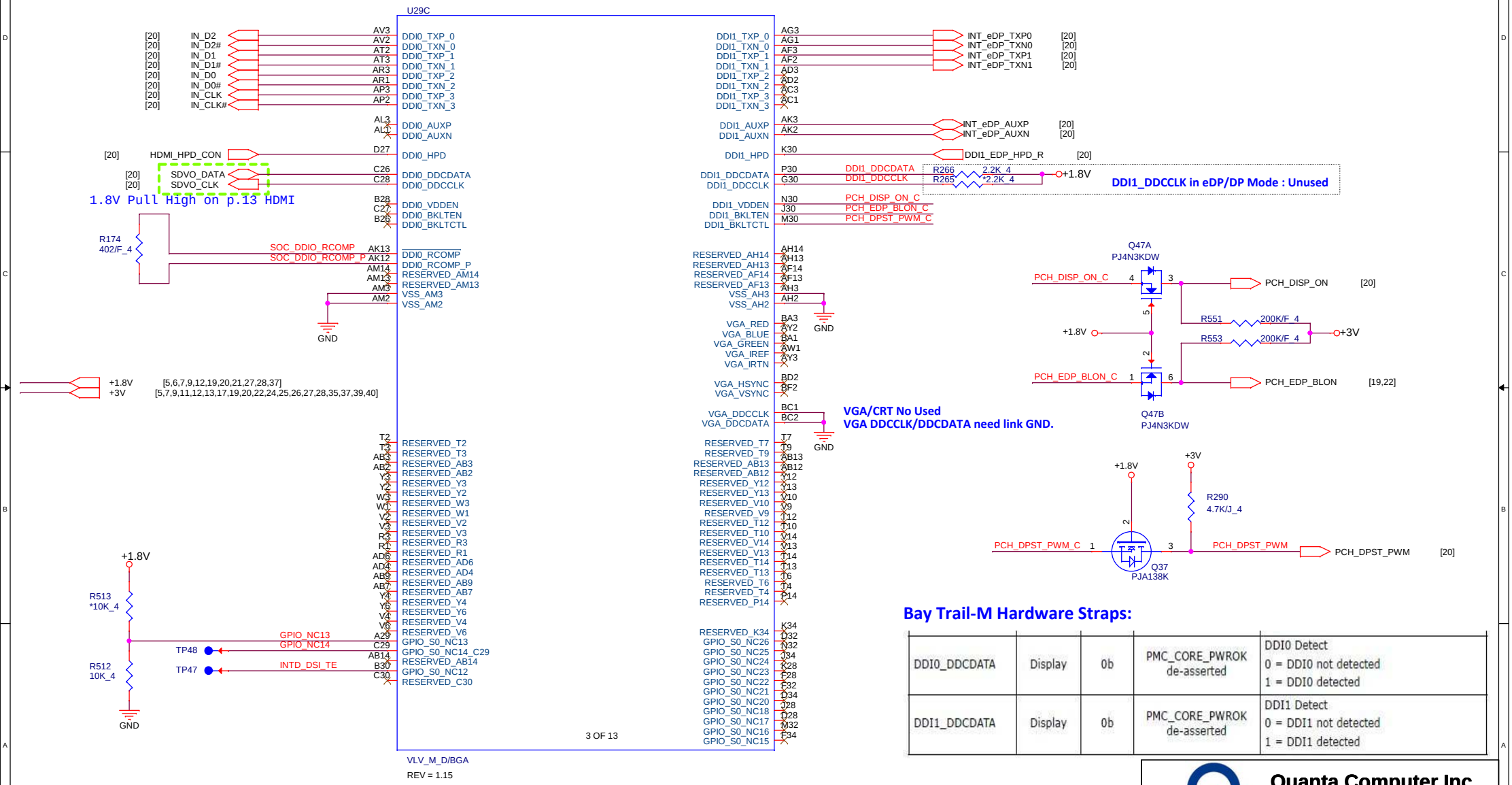


Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 1/9 (DDRA)	1A
Date: Thursday, July 10, 2014	Sheet 2 of 44	



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 2/9 (DDRB)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 3 of 44	



Bay Trail-M Hardware Straps:

DDI0_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI0 Detect 0 = DDI0 not detected 1 = DDI0 detected
DDI1_DDCDATA	Display	0b	PMC_CORE_PWROK de-asserted	DDI1 Detect 0 = DDI1 not detected 1 = DDI1 detected

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	Valley 3/9 (Display)	1A
Date: Thursday, July 10, 2014	Sheet 4 of 44	

SATA HDD

SATA ODD

GPU x2

WLAN x1

LAN x1

201/04/18 : Add GPU Power Control Siganls

201/04/18 : Add GPU Power Control Siganls

Default NC No Pull High / Low

Default Pull High 10K(+3V)

Default NC No Pull High / Low

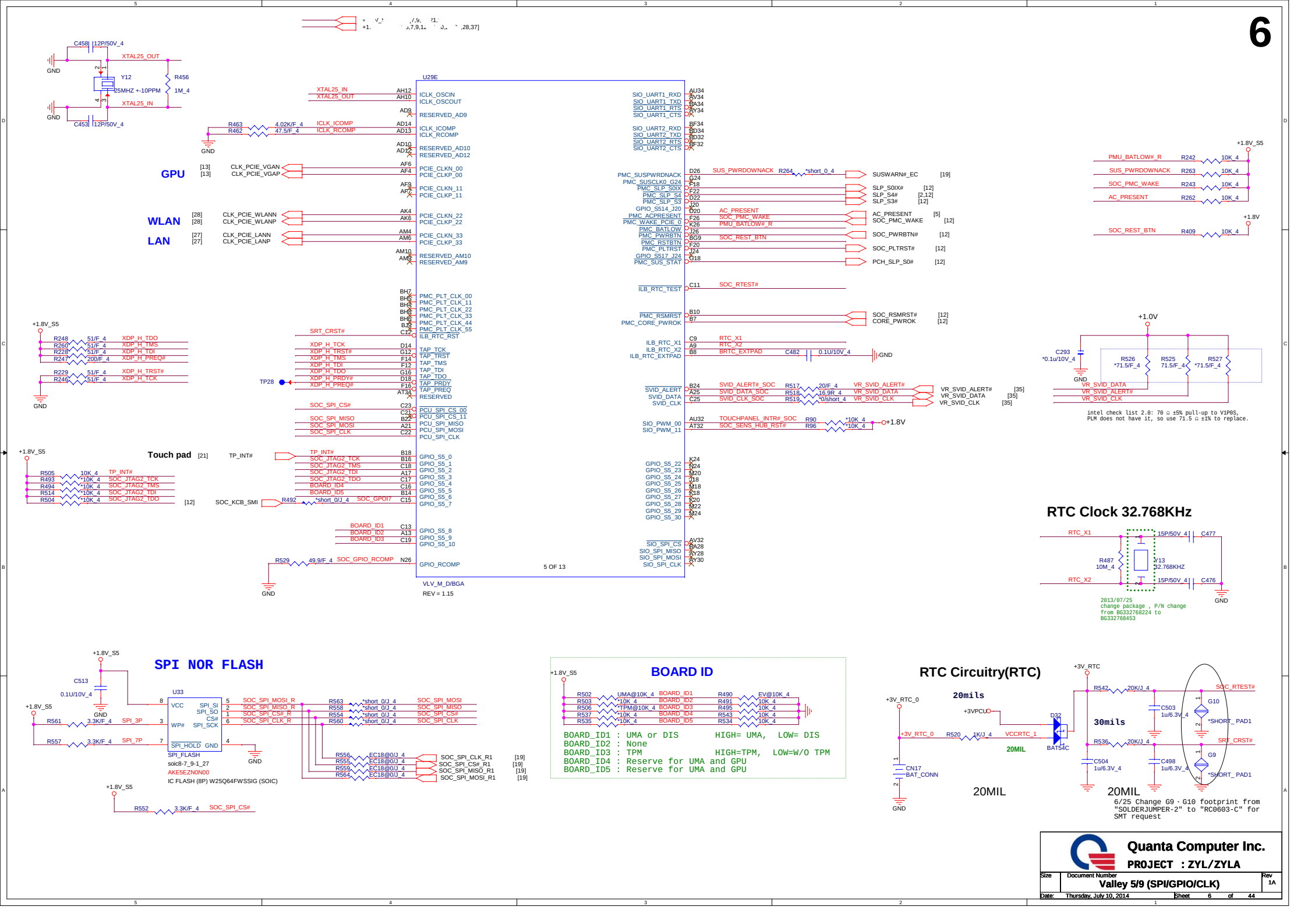
Default Pull Low 10K(GND)

Security Flash Descriptors
0 = Override
1 = Normal Operation

0 = LPC
1 = SPI

AC Present: This input pin indicates when the platform is plugged into AC power.

Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Size | Document Number: Valley 4/9 (SD/PCIE/SATA) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 5 of 44



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 5/9 (SPI/GPIO/CLK)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 6 of 44	

+1.8V_S5 [6,9,12,21,37]
+1.8V [4,5,6,9,12,19,20,21,27,28,37]
+3V [4,5,9,11,12,13,17,19,20,22,24,25,26,27,28,35,37,39,40]

U29F

Port 1 is debug port

USB3.0

USB 2.0 HUB

Bluetooth

CAMERA

Top Swap (A16 Override)
0 = Top address bit is unchanged
1 = Top address bit is inverted

Touch pad

Un-Stuff for Test Only

I2C pull up:
Standard/ Fast Mode --> 560 ohm
Hight speed mode --> CLK- 560 ohm;
DATA- 910 ohm

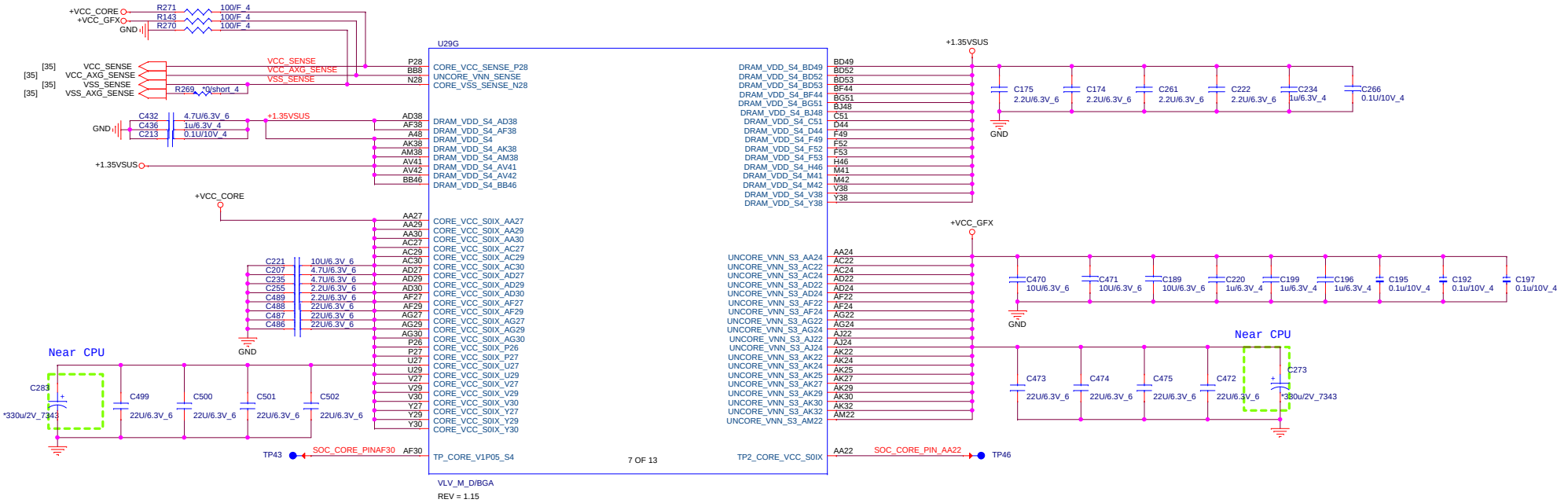
6 OF 13

VLV_M_D/BGA
REV = 1.15

PJ4N3KDW

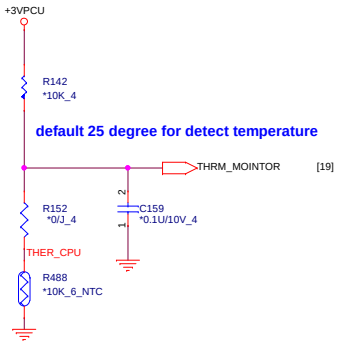
Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size | Document Number: Valley 6/9 (USB/LPC/I2C) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 7 of 44

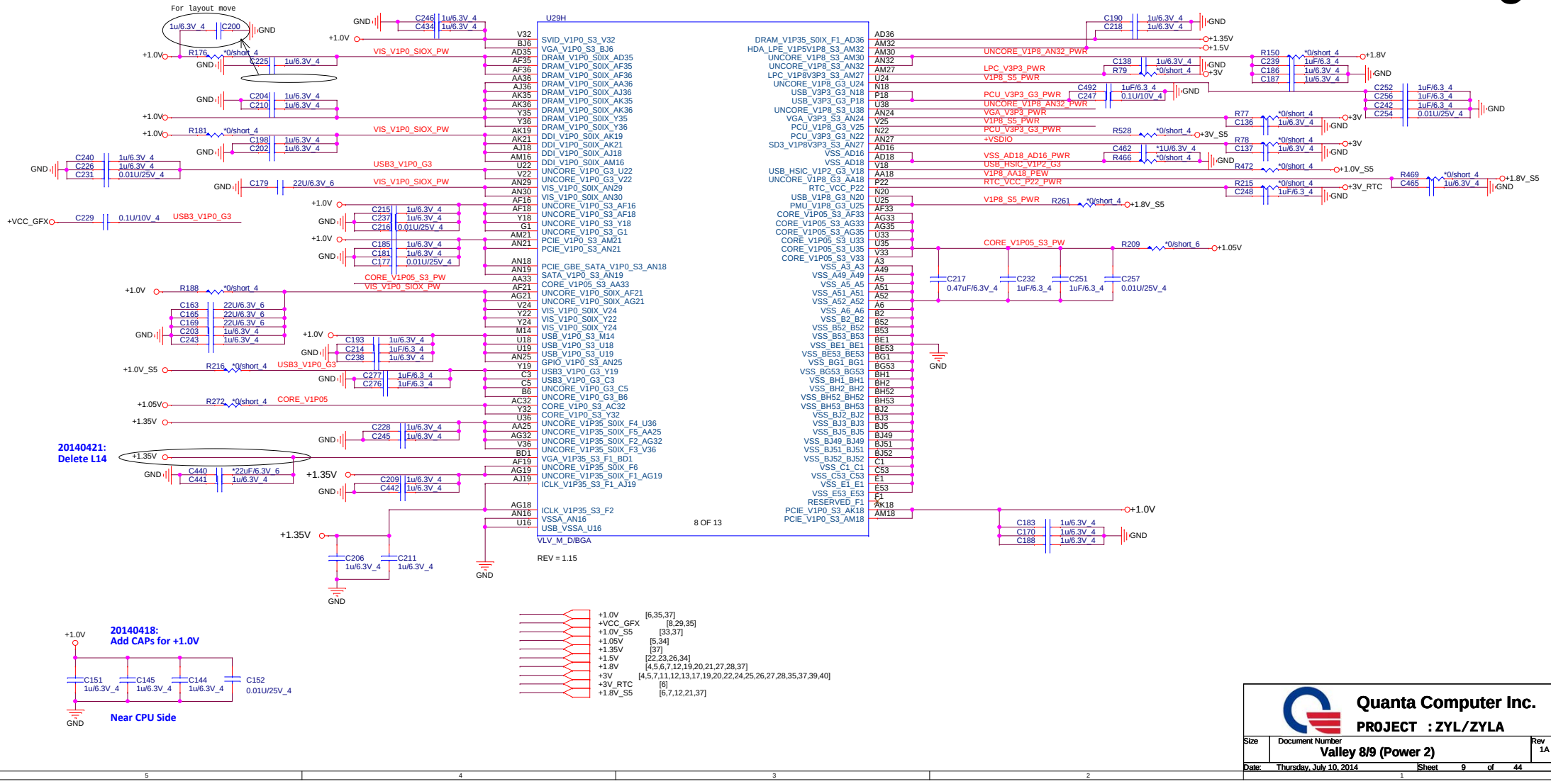


+VCC_CORE [29,35]
+VCC_GFX [9,29,35]
+1.35VSUS [2,11,36,37]
+3VPCU [6,19,21,22,25,26,30,31,32,37,39,40]

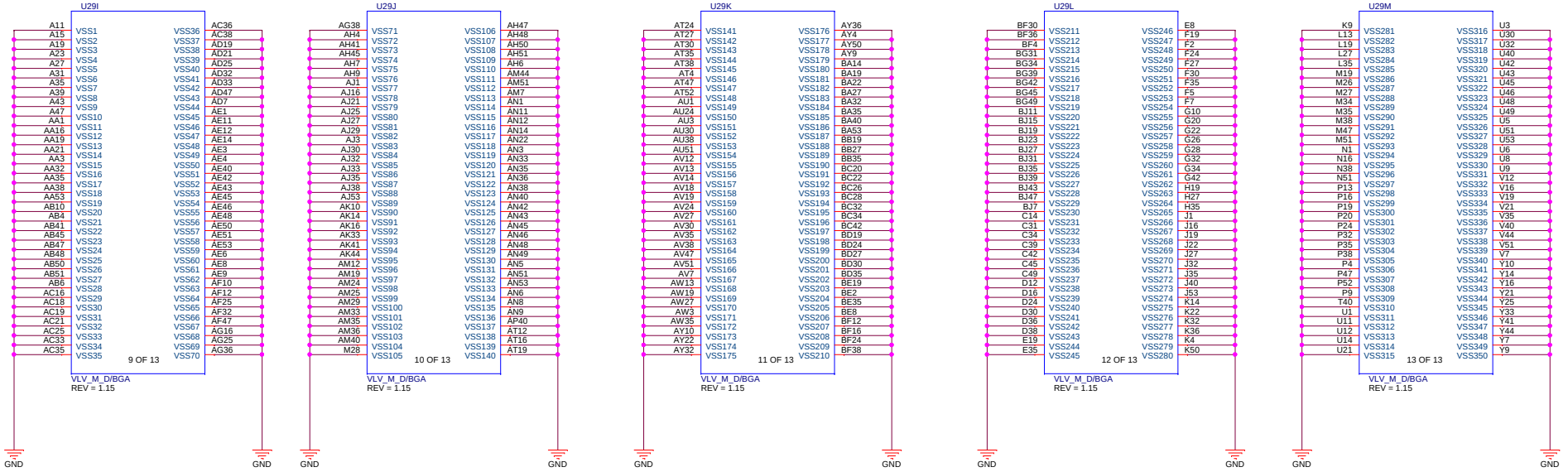
IO Thrm Protect



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Valley 7/9 (Power 1)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 8 of 44	



Quanta Computer Inc.			
PROJECT : ZYL/ZYLA			
Size	Document Number		Rev
	Valley 8/9 (Power 2)		1A
Date: Thursday, July 10, 2014		Sheet 9 of 44	



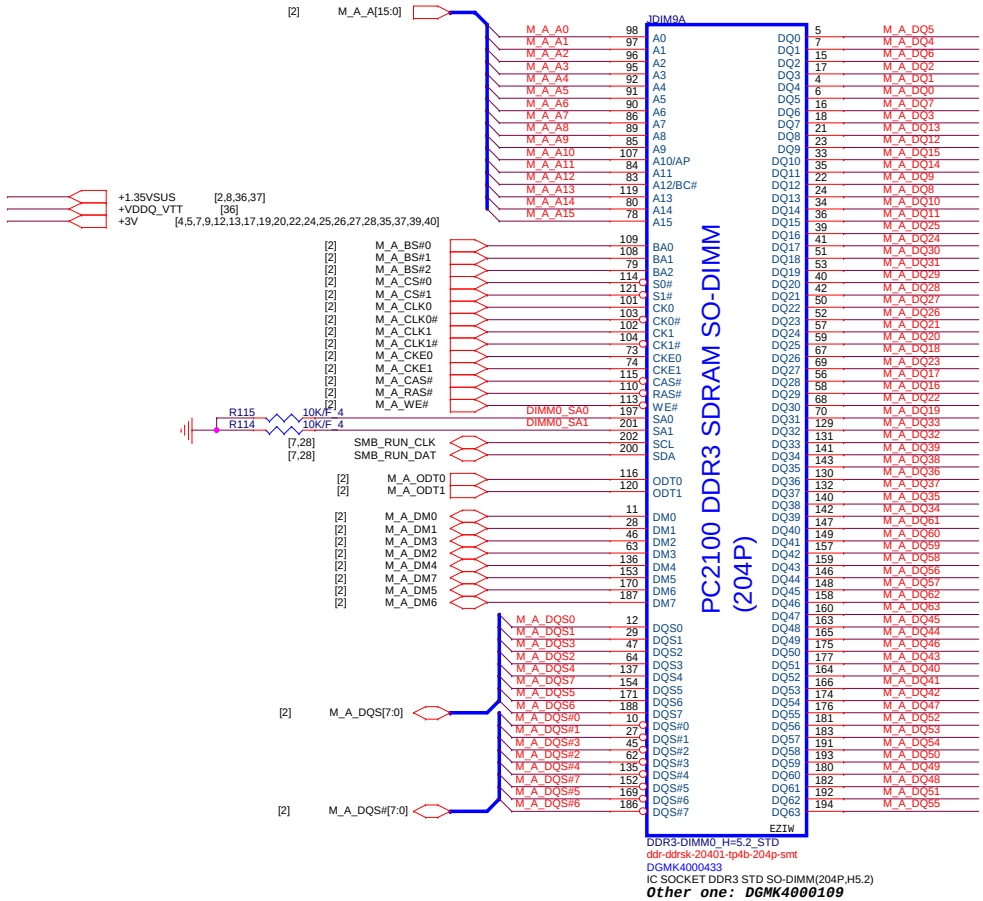
Quanta Computer Inc.

PROJECT : ZYL/ZYLA

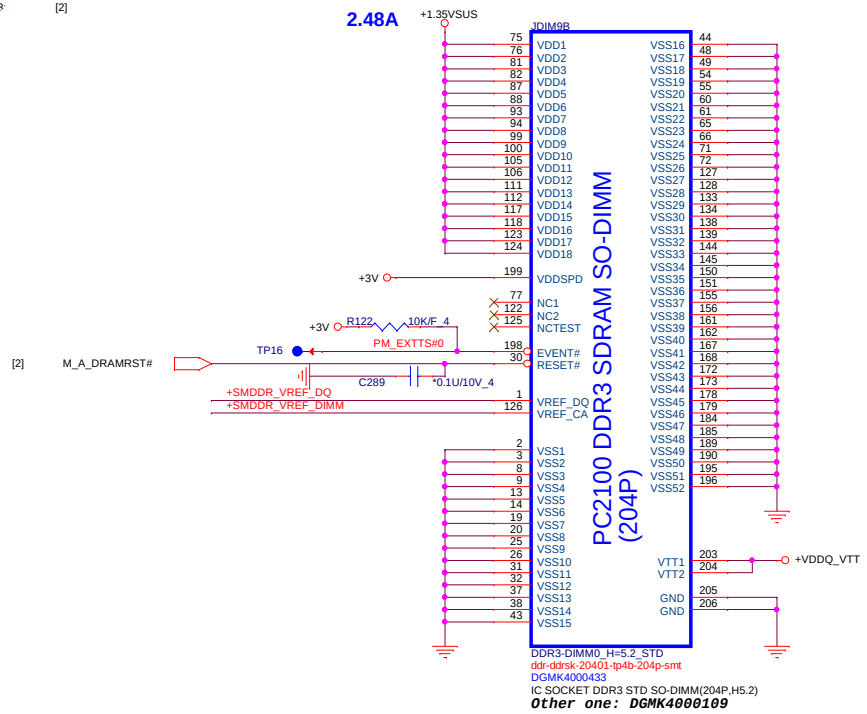
Size	Document Number	Rev
	Valley 9/9 (GND)	1A

Date: Thursday, July 10, 2014 Sheet 10 of 44

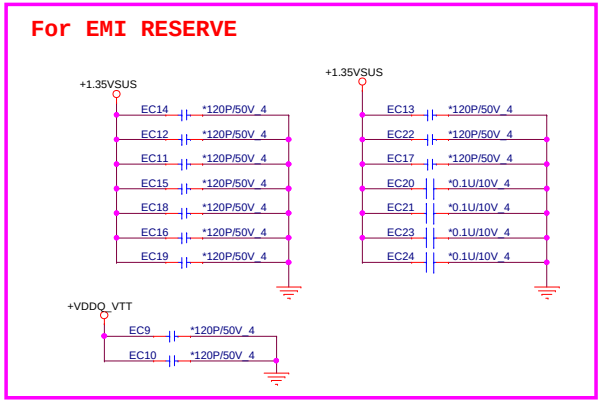
Address A0H



2.48A

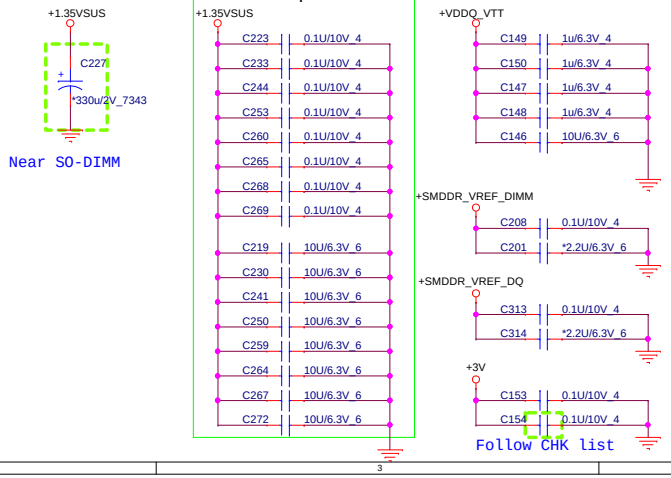


For EMI RESERVE

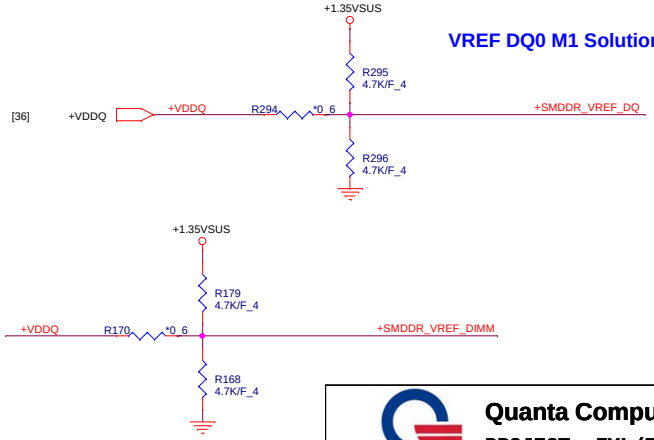


Place these Caps near So-Dimm0.

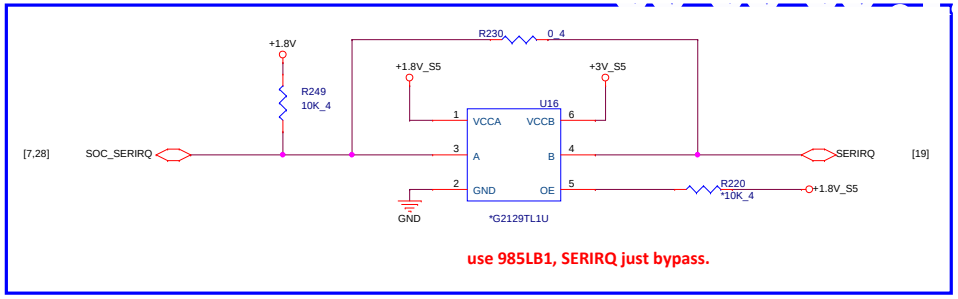
0.1uF/10uF 4pcs on each side of connector

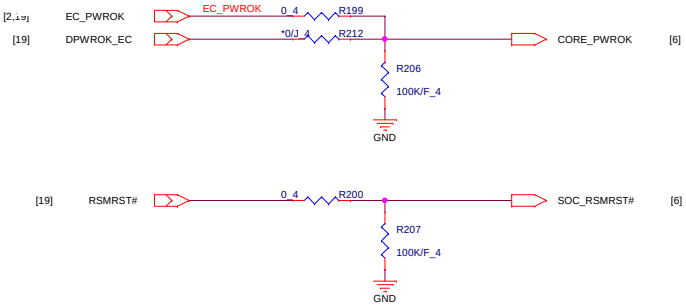


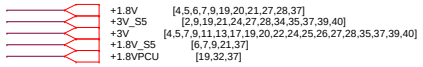
VREF DQ0 M1 Solution

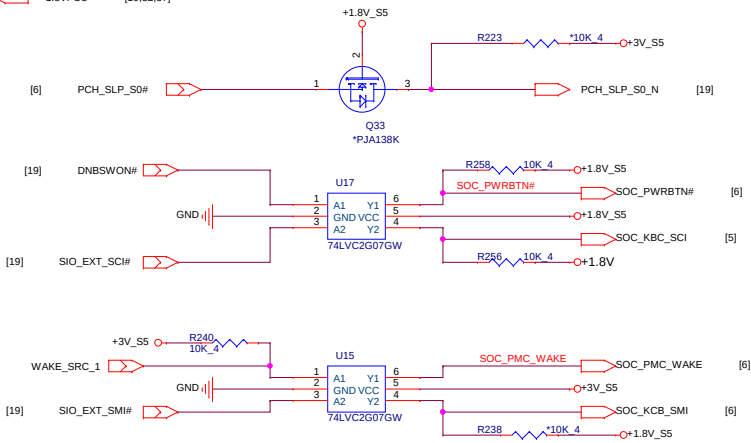


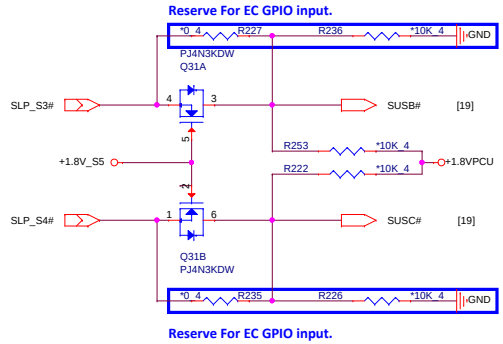
Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: DDR3 DIMM0-STD(5.2H)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 11 of 44	

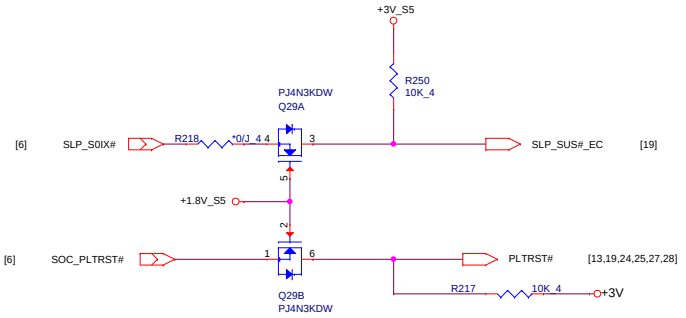


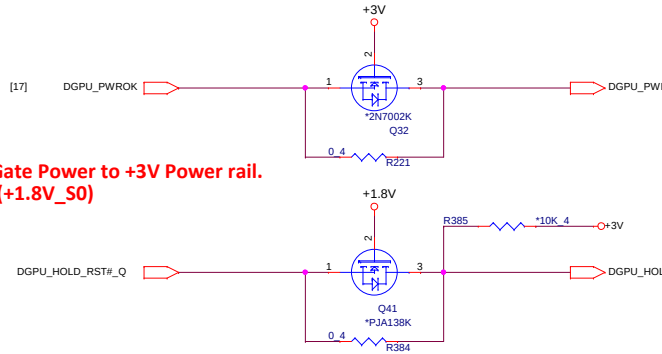


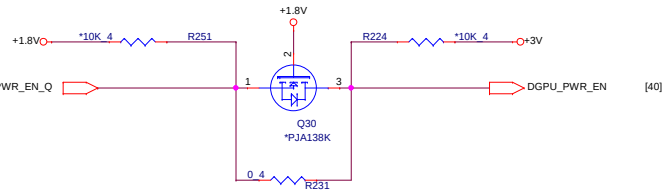












Check Q51 / Q52 Gate Power to +3V Power rail.
Check which GPIO(+1.8V_S0)

Quanta Computer Inc.			
PROJECT : ZYL/ZYLA			
Size	Document Number		Rev
	Level Shfiter		1A
Date: Thursday, July 10, 2014		Sheet 12 of 44	

<VGA>

1000mA

2500mA

210mA of +3V_GFX

PLACE UNDER GPU BALLS

PLACE NEAR GPU

4.7uF x 15 population x10

0.1uF x 8 population x 4

47u x1 | 22u x7 stuff x 1 | 4.7u x6 stuff x 5 | 330u x1 RSVD by DG

0817 RSVD more NVVDD caps by NV DG

Follow Z09 to isolate CLK_REQ#

PU at page 9

not GC6 2.0 unstuff resistor

0.4MM = 16mils

for meet Power down sequence for +3V_GFX

No stuff D8 when GC6 support.

8mils width (0.2MM)

PEX_PLLVDD : 0.3MM = 12mils (150mA)
RSVD R1 and C1 for GV2 co-layout sDDR3 R1

PCH control PEGX_RST#

N15x Power on sequance

PEX_RST timing

Trise >= 1uS

Tfail <=500nS

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size | Document Number: DGPU 1/5 (PEG) | Rev 1A

Date: Thursday, July 10, 2014 | Sheet 13 of 44

<VGA>

N15V-GM no support GC6 function.

For Fermi

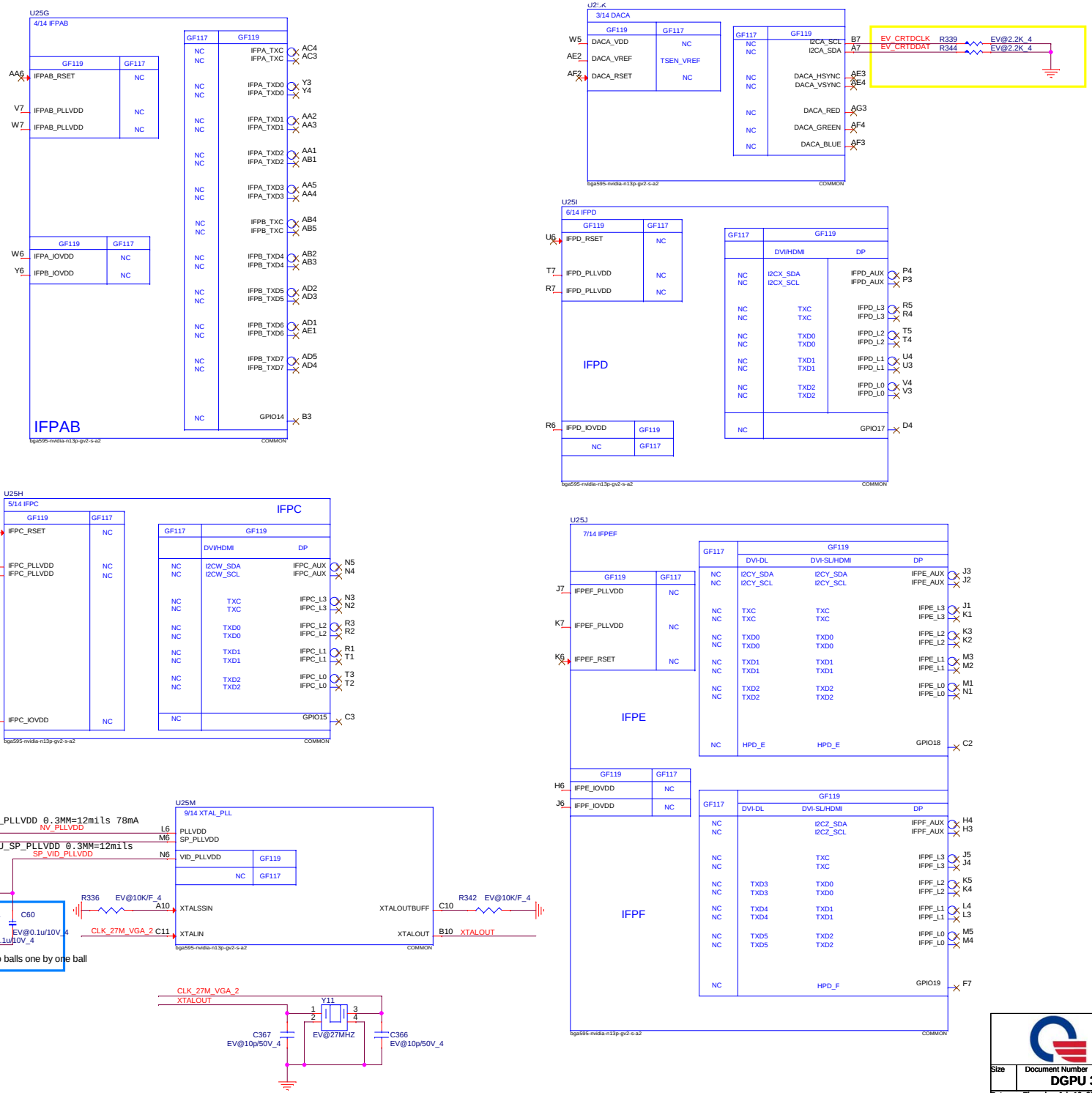
C87 close ball H22 35mA

PLACE CLOSE TO GPU BALLS

PLACE CLOSE TO BGA

sDDR3
R47=42.2/F
R50=51.1/F

Quanta Computer Inc.
PROJECT : ZYL/ZYLA
Size | Document Number: DGPU 2/5 (Memory) | Rev 1A
Date: Thursday, July 10, 2014 | Sheet 14 of 44


U25G
4/14 IFPAB
IFPAB
U25H
5/14 IFPC
IFPC
U25I
6/14 IFPD
IFPD
U25J
7/14 IFPEF
IFPE
IFPF
U25M
9/14 XTAL_PLL
U2?K
3/14 DACA
NV_PLLVDD 0.3MM=12mils 78mA
GPU_SP_PLLVDD 0.3MM=12mils
close to balls one by one ball
Near GPU
Under GPU
EV_CRTDCLK
EV_CRTDDAT
Y11
EV@27MHZ
Quanta Computer Inc.
PROJECT : ZYL/ZYLA
DGPU 3/5 (Display)
Thursday, July 10, 2014
Sheet 15 of 44

<VGA>

U25L

10/14 MISC2

VMON_IN0 E10
VMON_IN1 F10

STRAP0 D1
STRAP1 D2
STRAP2 E2
STRAP3 E3
STRAP4 D3

GF119	GF117
STRAP5_NC	NC

C1
F6

R3
R362 *EV@40.2K/F_4
N15V-GM NC

MULTISTRAP_REF0_GND

GF119	GF117
MULTISTRAP_REF1_GND	NC
MULTISTRAP_REF2_GND	NC

R38 *EV@40.2K F4
R34 *EV@40.2K F5

ROM_CS D12 R37 EV@10K_4 +3V_GFX
ROM_SI B12 ROM_SI
ROM_SO A12 ROM_SO
ROM_SCLK C12 ROM_SCLK

BUFRST D11 R21 *EV@10K_4
PGOOD D10

CEC E9 TP34

bga595-nvidia-n13p-gv2-s-a2 COMMON

+3V_GFX [13,17,40]
+3V_MAIN [13,17]

U25N

8/14 MISC1

I2CS Slave Address= 0x9E (default)

I2CS_SCL D9 GFX_SCL
I2CS_SDA D8 GFX_SDA

I2CC_SCL A9 DGPU_EDIDCLK EV@2.2K_4 R337
I2CC_SDA B9 DGPU_EDIDDATA EV@2.2K_4 R343

THERMDN E12
THERMDP F12

GF117	GF119
NC	I2CB_SCL
NC	I2CB_SDA

I2CB_SCL C9 N13P_SCL EV@2.2K_4 R338
I2CB_SDA C8 N13P_SDA EV@2.2K_4 R30

JTAG_TCK AE5
JTAG_TMS AD6
JTAG_TDI AE6
JTAG_TDO AF6
JTAG_TRST AG4
TP39

GPIO0 C6 TP10
GPIO1 B2
GPIO2 D6
GPIO3 C7
GPIO4 F9
GPIO5 K3 TP9
GPIO6 A4
GPIO7 B6
GPIO8 A6 GPIO8_OVERT#
GPIO9 F8 GPIO9_ALERT
GPIO10 C5
GPIO11 E7
GPIO12 D7 GPIO12_ACIN
GPIO13 B4 DGPU_PSI

PWM-VID [39]
DGPU_PSI [39]

GF117	GF119
NC	GPIO16
NC	GPIO20
NC	GPIO21

GPIO16 D5
GPIO20 E5
GPIO21 C4 GPU_PEX_RST_HOLD#

bga595-nvidia-n13p-gv2-s-a2 COMMON

For N15V-GM-B Sku:
Device ID=0x1140
R3= N.C.
1.ROM_SCLK =10K pull down.
2.ROM_SI= 10k pull down
3.ROM_SO= 10k pull down
4.Strap3~0 = RVL memory binary mode setting.
5.Strap4 =10k pull down

Vendor	Vendor P/N	Strap0	Strap1	Strap2	Strap3	
HYNIX	HT5C4G63AFR-11C	0	0	1	0	
MICRON	MT41J256M16HA-093G:E	1	0	1	1	
SAMSUNG	K4W4G164D-BC1A	1	0	0	1	Default

+3V_MAIN
R335 *EV@4.99K/F_4
R334 *EV@4.99K/F_4
R18 *EV@4.99K/F_4
ROM_SI
ROM_SO
ROM_SCLK
R341 EV@10K/F_4
R340 EV@10K/F_4
R19 EV@10K/F_4

N15V-GM: Stuff 10K pull down

+3V_GFX
R353 EV@10K/F_4
R351 *EV@10K/F_4
R357 *EV@10K/F_4
R355 EV@10K/F_4
R349 *EV@10K/F_4
STRAP0
STRAP1
STRAP2
STRAP3
STRAP4
R352 *EV@10K/F_4
R350 EV@10K/F_4
R356 EV@10K/F_4
R354 *EV@10K/F_4
R348 EV@10K/F_4

STRAP0~3:
N15V-GM Stuff 10K

N15V-GM: Memory strap setting Please follow N15x latest RVL "RVL-06891-001".

N15V-GM VRAM Configuration Table:

	Strap [3:0]	DESCRIPTION	Vendor	Vendor P/N	QCI P/N
4Gb	0100 (0x4) 1101 (0xD) 1001 (0x9)	DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz DDR3 256MBx16,1000MHz	HYNIX MICRON SAMSUNG	H5TC4G63AFR-11C MT41J256M16HA-093G:E K4W4G1646D-BC1A	

STRAP3
Optimus ---> 4.99k PD

Resistor P/N
10K ---> CS31002FB26

+3V_GFX
GPIO9_ALERT R25 EV@10K/F_4
DGPU_PSI R346 *EV@10K/F_4
GPIO8_OVERT# R345 EV@10K/F_4
JTAG_TMS R48 *EV@10K/F_4
JTAG_TDI R49 *EV@10K/F_4
GPIO12_ACIN R11 EV@10K/F_4
GPU_PEX_RST_HOLD# R347 *EV@10K/F_4
JTAG_TCK R57 *EV@10K/F_4
JTAG_TRST# R60 EV@10K/F_4

GPIO8 VGA thrmtrip# => inform EC over temperature protect

GPIO8_OVERT# 1
+3V_GFX
Q13 EV@2N7002K
3
2
R20 *EV@0_4
R22 *0/short_4
dGPU_OTP# = EC control
dGPU_OTP# [19]
PEGX_RST# [13]

+3V_GFX
Q9 EV@2N7002K
2
GPIO12_ACIN 1
3
dGPU_OPP# = EC control
dGPU_OPP# [19]
GPIO12 AC detect
AC high
DC low

SMBus(VGA)

+3V_GFX
+3V_MAIN
R15 EV@10K/F_4
R14 EV@10K/F_4
Q11
GFX_SCL 4
GFX_SDA 1
5
3
2
6
MBCLK2 [19,22]
MBDATA2 [19,22]
EV@2N7002DW
VGA/VGA
EC/S5

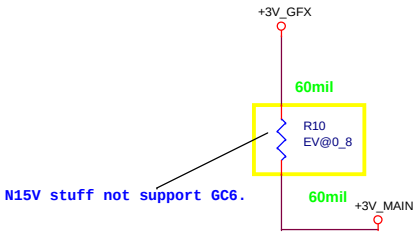
Vendor P/N	820M		QCI P/N
N15V-GM-B-A2	GeForce 820M	0x1140	AJ0N15V0T03

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

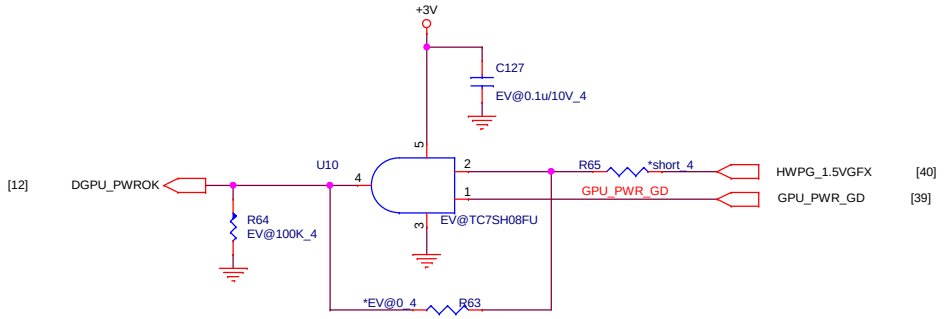
Size	Document Number	Rev
	DGPU 4/5 (MIO/GPIO)	1A

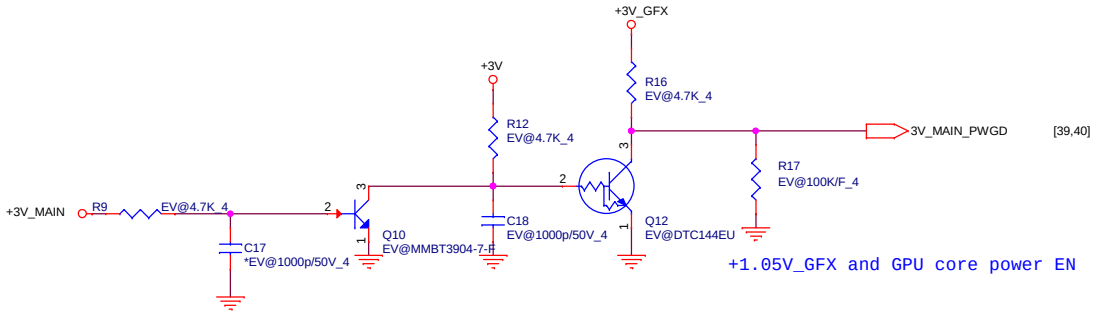
Date: Thursday, July 10, 2014 Sheet 16 of 44

+3V_GFX [13,16,40]
+3V_MAIN [13,16]
+3V [4,5,7,9,11,12,13,19,20,22,24,25,26,27,28,35,37,39,40]



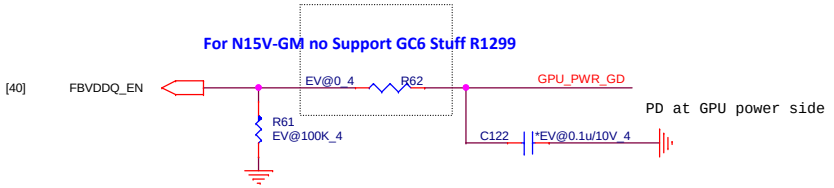
N15V stuff not support GC6.





+1.05V_GFX and GPU core power EN

For N15V-GM no Support GC6 Stuff R1299



PD at GPU power side

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	DGPU 5/5 (Power/Ground)	1A
Date: Thursday, July 10, 2014	Sheet 17 of 44	

CHANNEL A: 2048MiB DDR3X16

+1.05V_GFX [13,14,15,40]

[14] VMA_DQ[63..0]
[14] VMA_DM[7..0]
[14] VMA_WDQS[7..0]
[14] VMA_RDQS[7..0]

VRAM9 / VRAM11 / VRAM10 / VRAM12

96-BALL SDRAM DDR3

EV@VRAM _DDR3_HYNIX_256MX16

Should be 240 Ohms +-1%

R33 EV@243/F_4
R358 EV@243/F_4
R50 EV@243/F_4
R365 EV@243/F_4

Fermi : Change to 160 ohm
1 : CS11602JB00 ,RES CHIP 160 1/16W +-5%(0402)
2 : CS11622FB07 ,RES CHIP 162 1/16W +-1%(0402)

R31 EV@162/F_4 (VMA_CLK0 / VMA_CLK0#)

R58 EV@162/F_4 (VMA_CLK1 / VMA_CLK1#)

[14] FBA_CMD17 → TP11
[14] FBA_CMD1 → TP35
10/14 modify

R360 EV@1.33K/F_4, R361 EV@1.33K/F_4, C372 EV@0.1u/10V_4
R23 EV@1.33K/F_4, R26 EV@1.33K/F_4, C26 EV@0.1u/10V_4
R47 EV@1.33K/F_4, R44 EV@1.33K/F_4, C96 EV@0.1u/10V_4
R371 EV@1.33K/F_4, R370 EV@1.33K/F_4, C386 EV@0.1u/10V_4

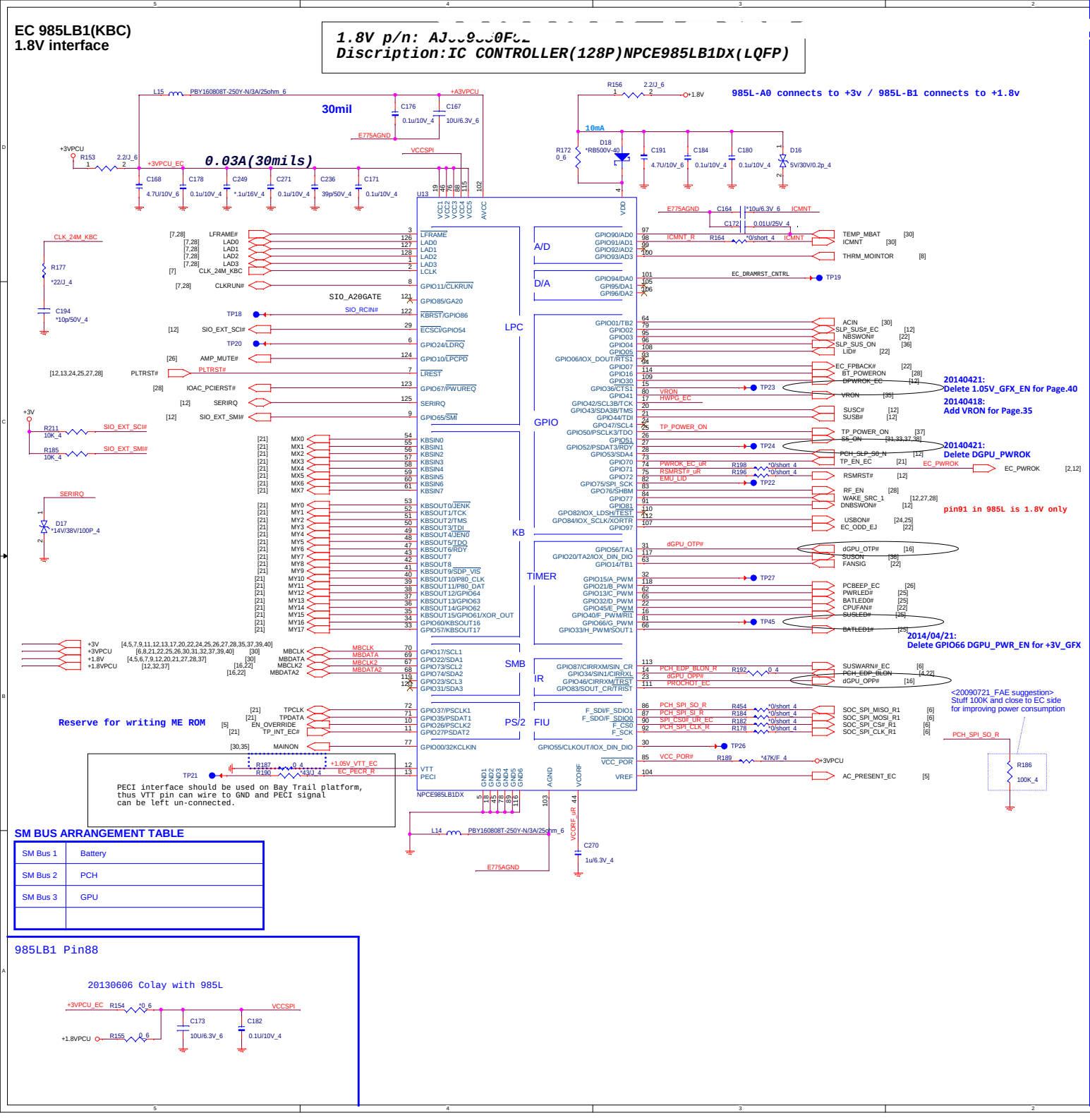
+1.5V_GFX decoupling:
C132 EV@1u/10V_4, C393 EV@1u/10V_4, C121 EV@1u/10V_4, C384 EV@1u/10V_4
C34 EV@10u/6.3V_6, C404 EV@1u/10V_4, C371 EV@1u/10V_4, C381 EV@1u/10V_4, C365 EV@1u/10V_4, C23 EV@1u/10V_4
C362 EV@10u/6.3V_6, C364 EV@1u/10V_4, C390 EV@1u/10V_4, C124 EV@1u/10V_4, C37 EV@1u/10V_4, C113 EV@1u/10V_4, C24 EV@1u/10V_4, C368 EV@1u/10V_4
C400 EV@10u/6.3V_6, C128 EV@10u/6.3V_6, C363 EV@0.1u/10V_4, C370 EV@0.1u/10V_4, C403 EV@0.1u/10V_4, C369 EV@0.1u/10V_4, C114 EV@0.1u/10V_4
C20 EV@10u/6.3V_6, C361 EV@10u/6.3V_6, C383 EV@0.1u/10V_4, C115 EV@0.1u/10V_4, C25 EV@0.1u/10V_4

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	N15P- DDR3 VRAM 1/2	1A
Date: Thursday, July 10, 2014	Sheet 18 of 44	

EC 985LB1(KBC)
1.8V interface

1.8V p/n: AJ[illegible]FC
Discription:IC CONTROLLER(128P)NPCE985LB1DX(LQFP)

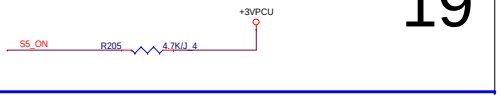


SM BUS ARRANGEMENT TABLE

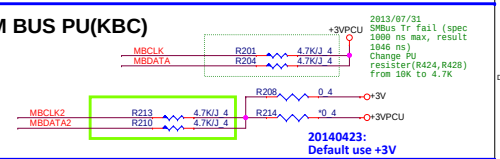
SM Bus 1	Battery
SM Bus 2	PCH
SM Bus 3	GPU

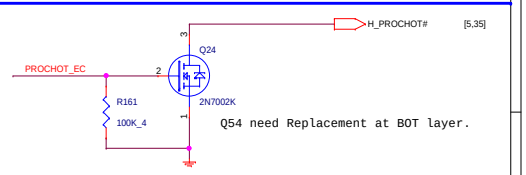
985LB1 Pin88

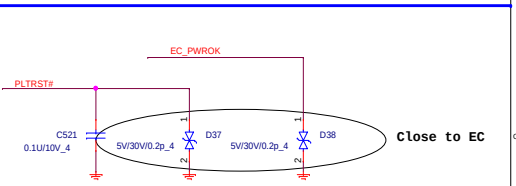
20130606 Colay with 985L



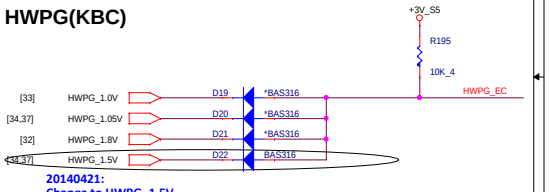
SM BUS PU(KBC)



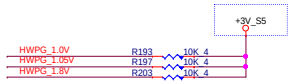


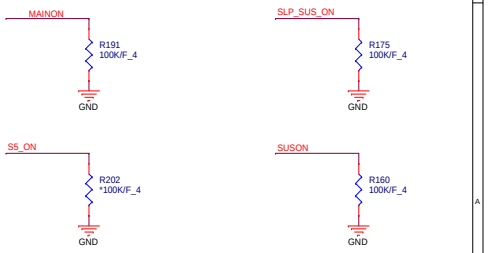


HWPG(KBC)



<20130722>Change power from +3V to +3V_S5 for power sequence issue





Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	NPCE885/FLASH	1A
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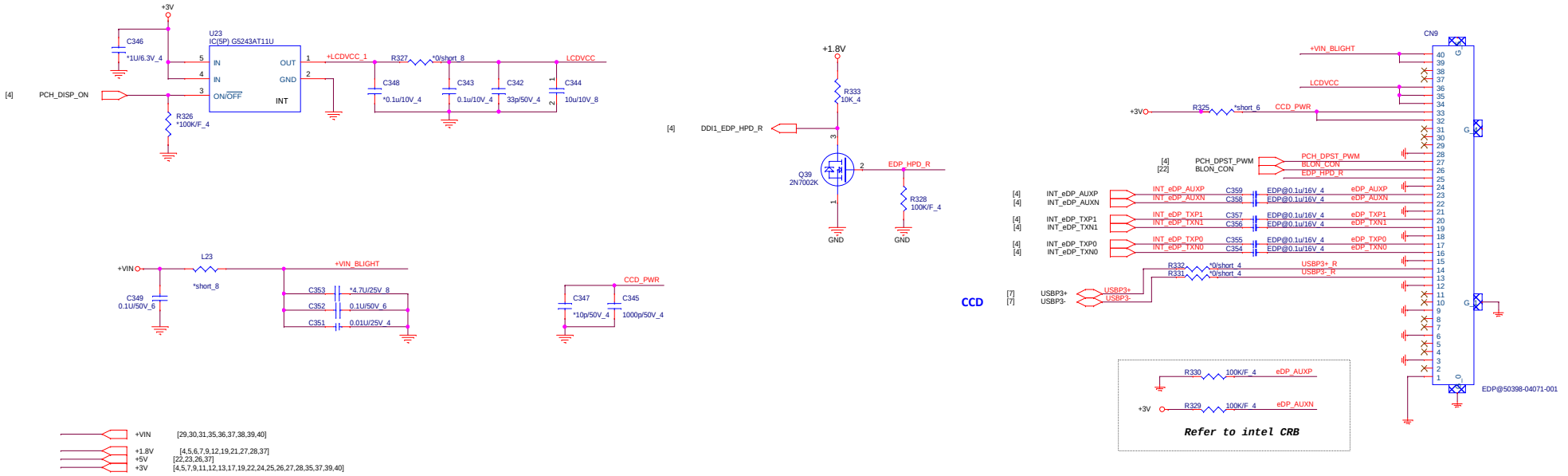
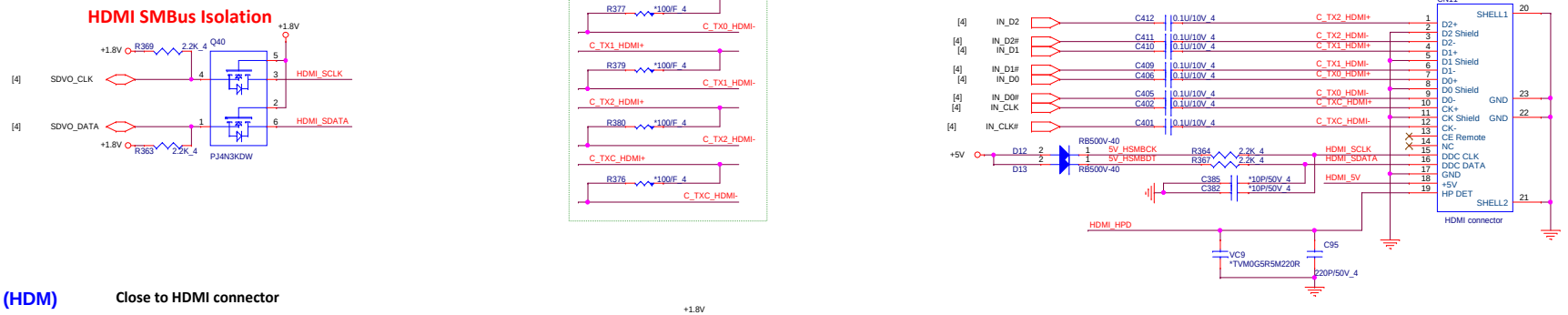
EDP Conn.

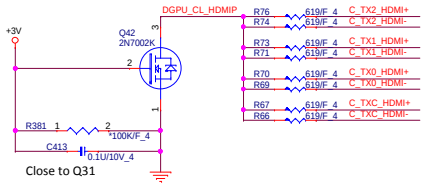


HDMI Conn.

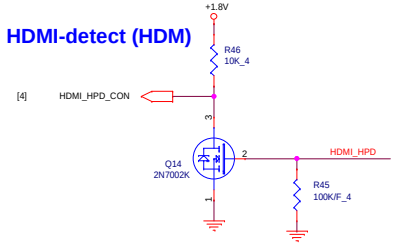


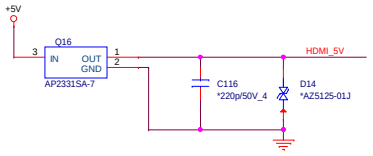
HDMI-Level shift (HDM)

Close to HDMI connector



HDMI-detect (HDM)





Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: LCD/HDMI/Camera	Rev: 1A
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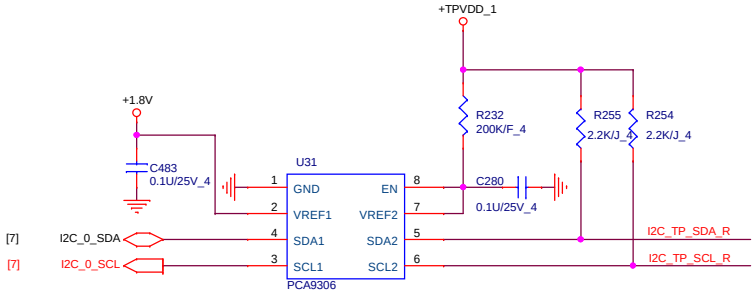
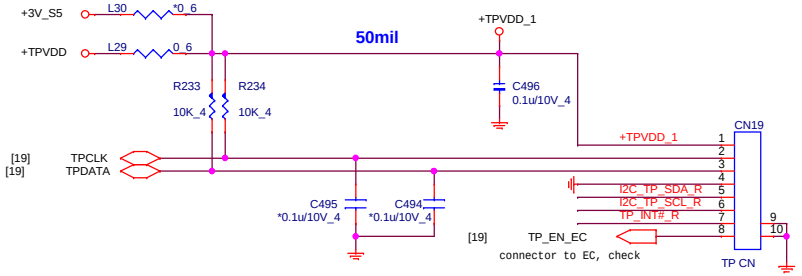
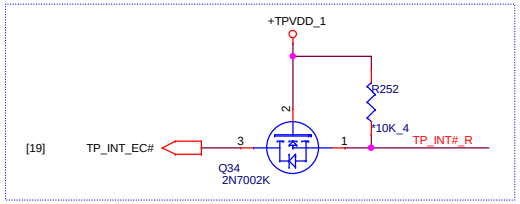
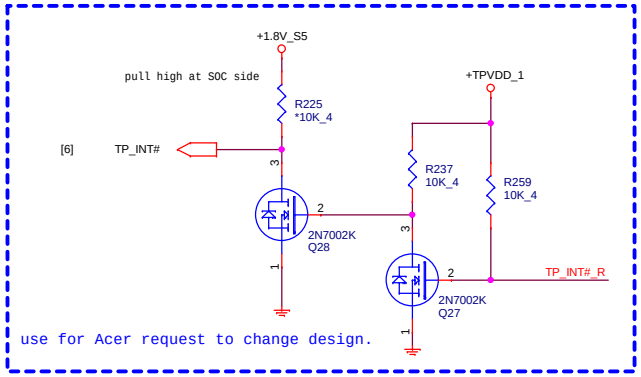
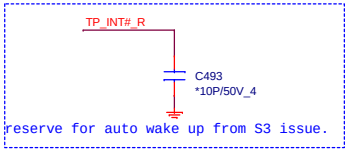
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



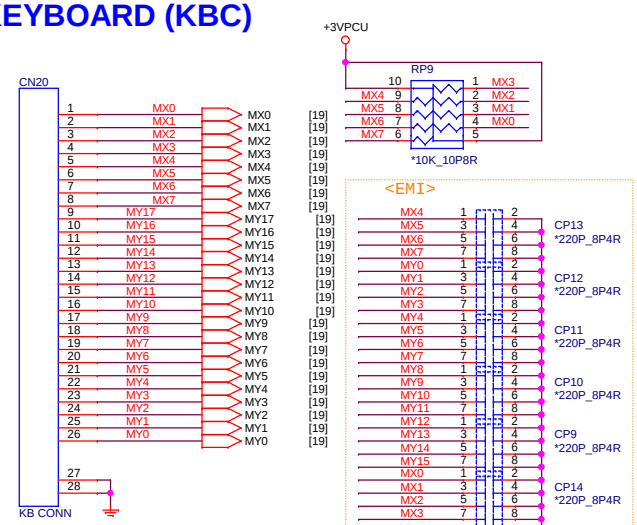


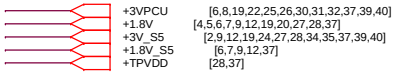






KEYBOARD (KBC)





Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	KB/BT/TP/LED/Power Connector	1A
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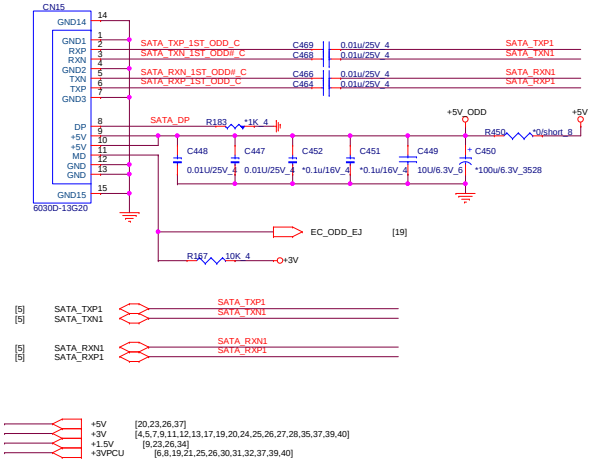
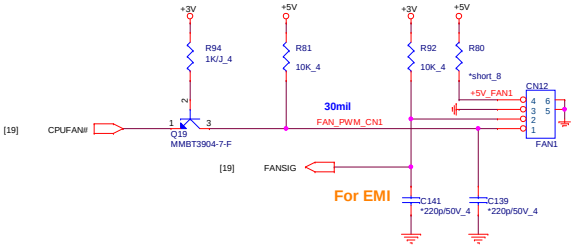
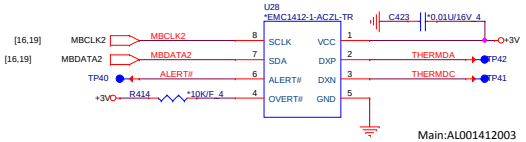
SATA ODD Connector



CPU FAN CTRL(THM)



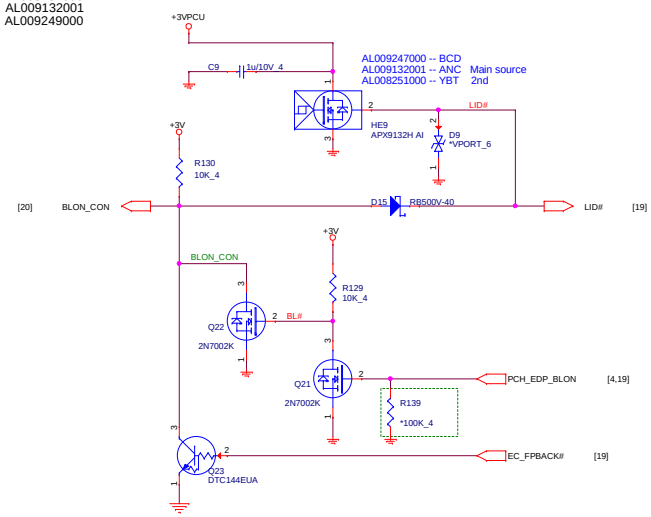
CPU Thermal sensor(THS) / MB Local TEMP



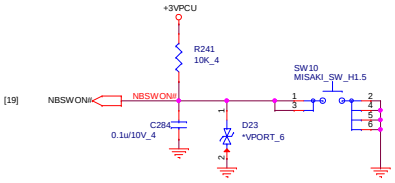
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

HALL IC (HSR)

1st source : EOD
2nd source : AL008251000 -- YBT
3rd source : AL009132001
4th source : AL009249000



Power Switch. (FSW)



Quanta Computer Inc. PROJECT ZYL/ZYLA		
Size	Document Number: ODD/FAN/Hall/PSW	Rev: 1A
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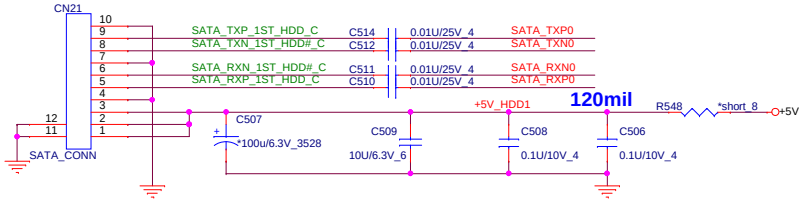
SATA HDD1

HDD1



[5] SATA_TXP0
[5] SATA_TXN0

SATA_TXP0
SATA_TXN0

[5] SATA_RXN0
[5] SATA_RXP0

SATA_RXN0
SATA_RXP0

+5V [20,22,26,37]
+1.5V [9,22,26,34]

Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	SATA HDD/SATA REDRIVER	1A

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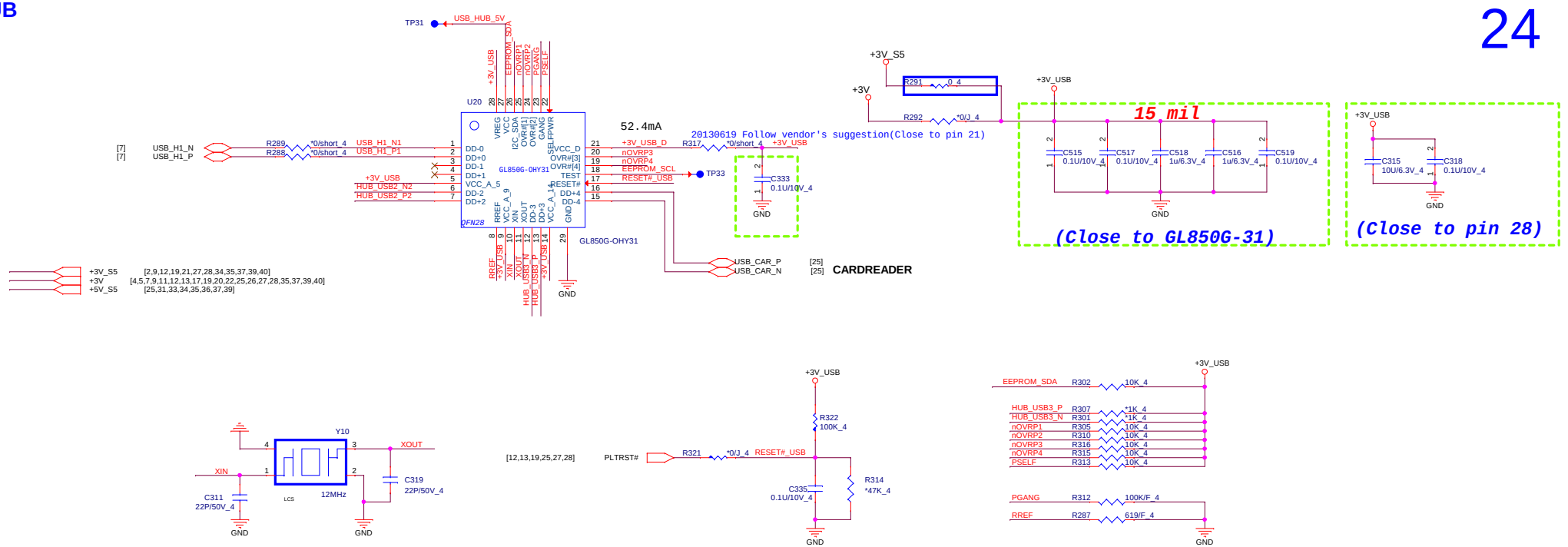
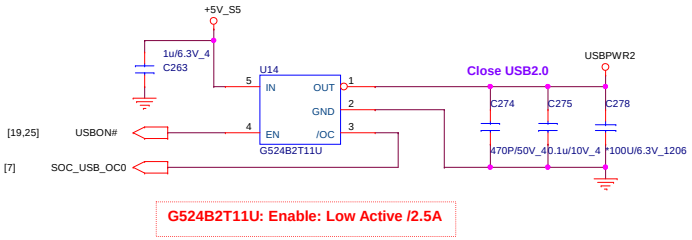
USB HUB

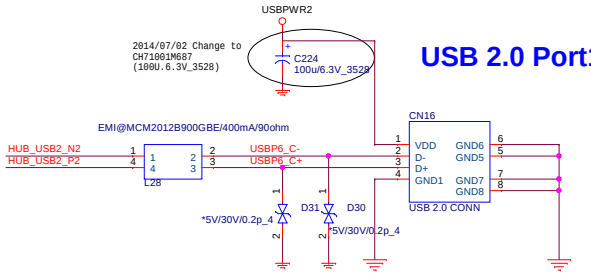


USB 2.0 CONNECTOR X2



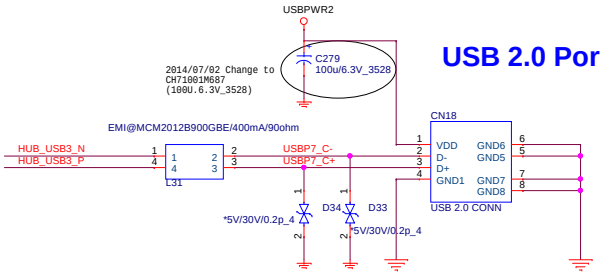
G524B2T11U: Enable: Low Active /2.5A

USB 2.0 Port1



Main: DFHD04MR377
UB2-UARDM-4K1926-4P-R

USB 2.0 Port2



Main: DFHD04MR377
UB2-UARDM-4K1926-4P-R

Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB BOARD CONN	1A
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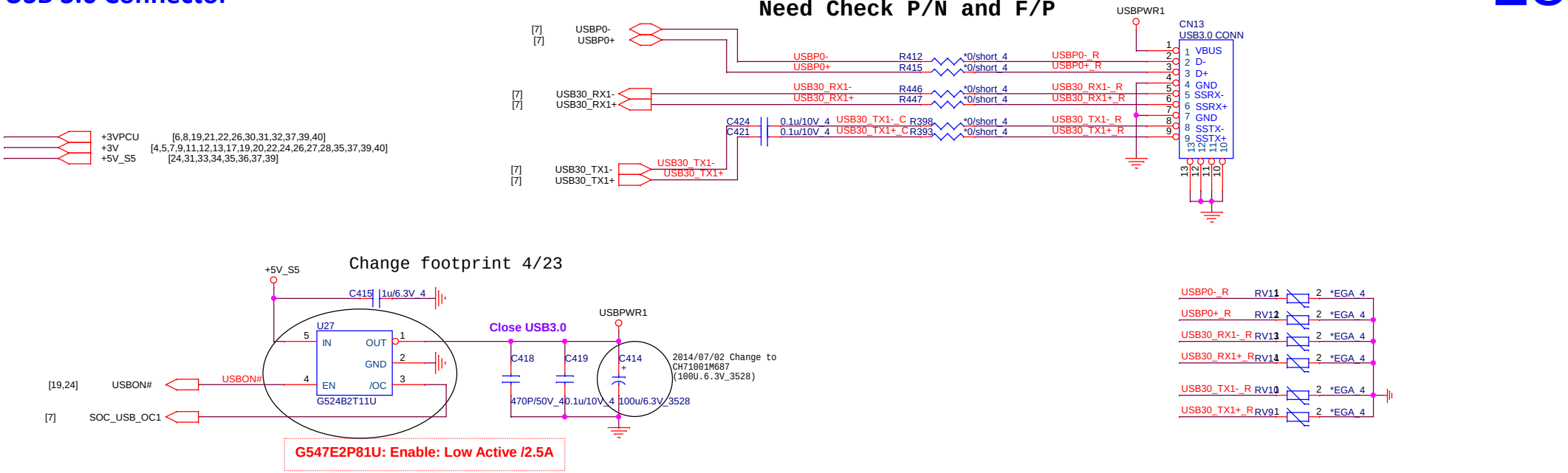
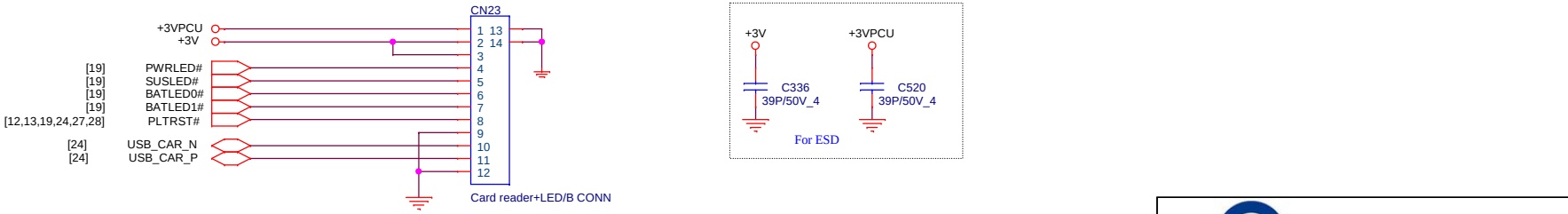
USB 3.0 Connector



Card Reader+ LED/B Connector



Quanta Computer Inc.
PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB 3.0 / Card Reader+LED CONN	1A
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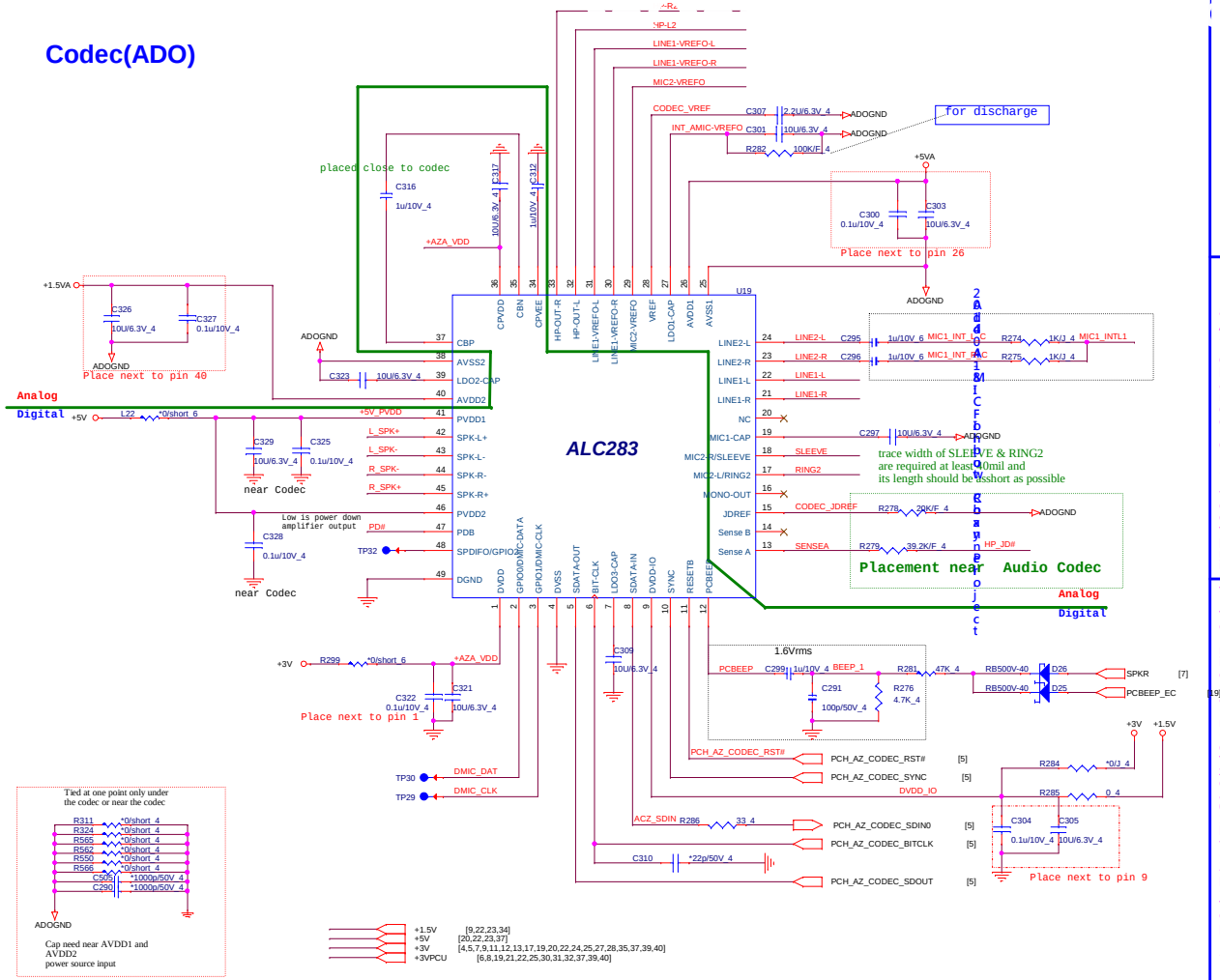
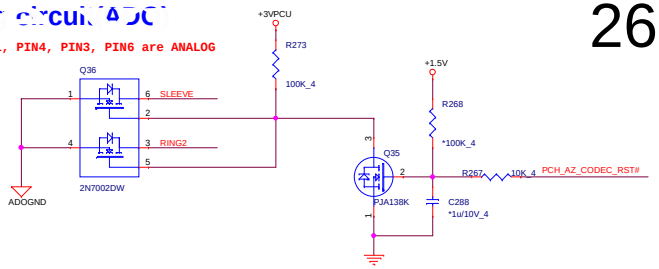
Codec(ADO)

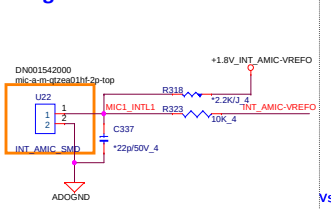


Ground circuit(ADO)

PIN1, PIN4, PIN3, PIN6 are ANALOG

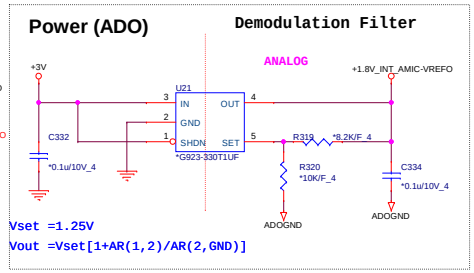


Analog-MIC



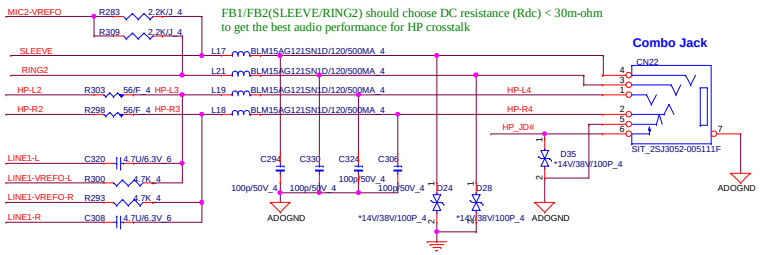
Power (ADO)

Demodulation Filter

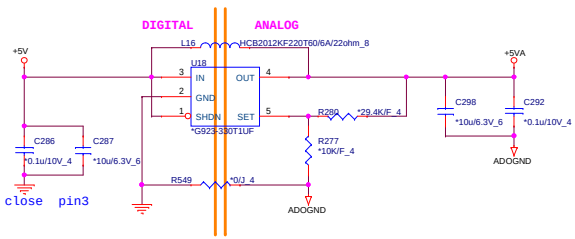


HEADPHONE/MIC/LINE combo (AMP)

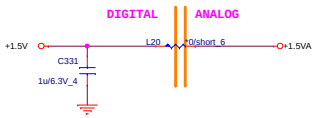
FB1/FB2(SLEEVE/RING2) should choose DC resistance (Rdc) < 30m-ohm to get the best audio performance for HP crosstalk



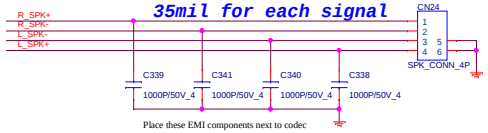
Codec PWR 5V(ADO)



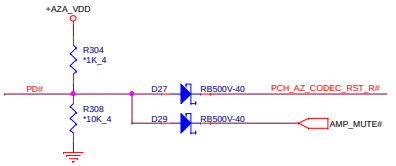
Codec PWR 1.5V(ADO)



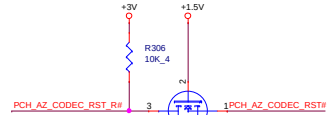
Internal Speaker



Mute(ADO)



Level shift



Quanta Computer Inc.		
PROJECT : ZYL/ZYLA		
Size	Document Number: Codec ALC3225	Rev: 1A
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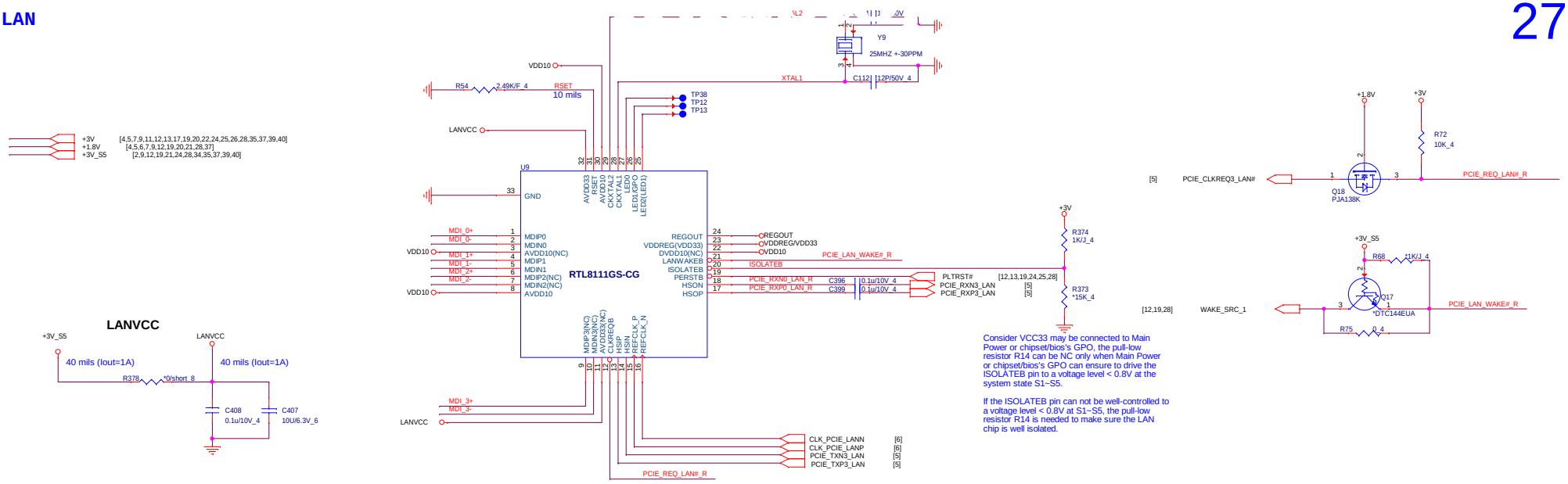
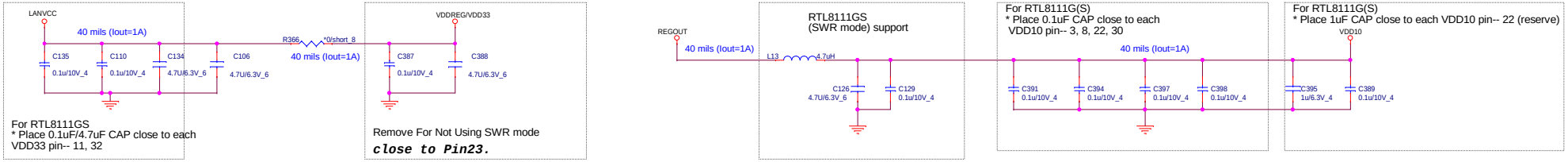
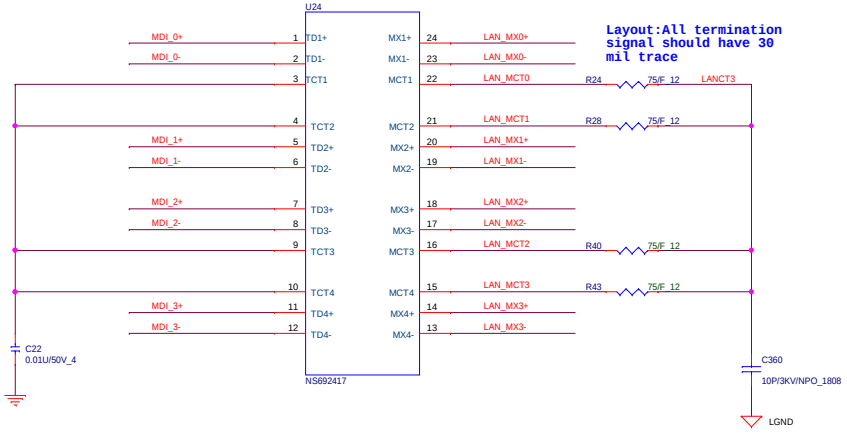
LAN



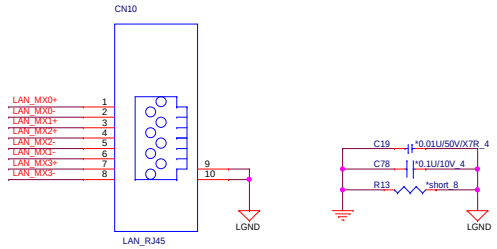


Tramsformer



RJ45 Connector

Need Check P/N and F/P



Quanta Computer Inc. PROJECT : ZYL/ZYLA		
Size	Document Number: LAN	Rev: 1A
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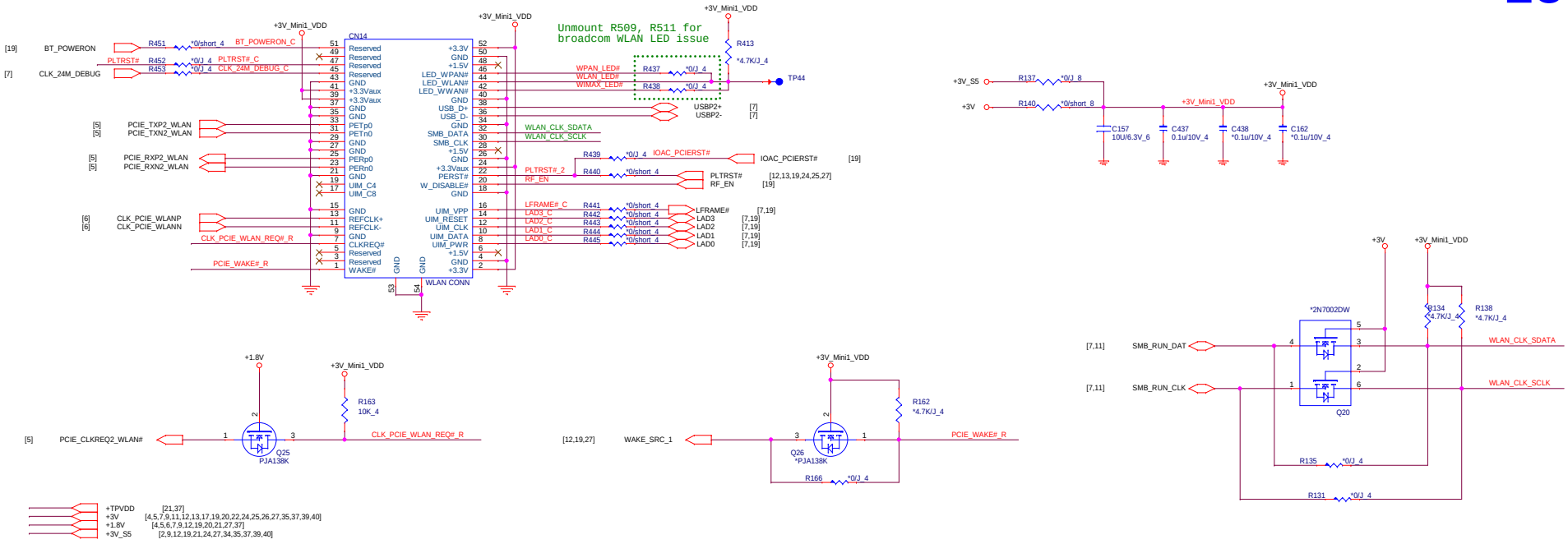
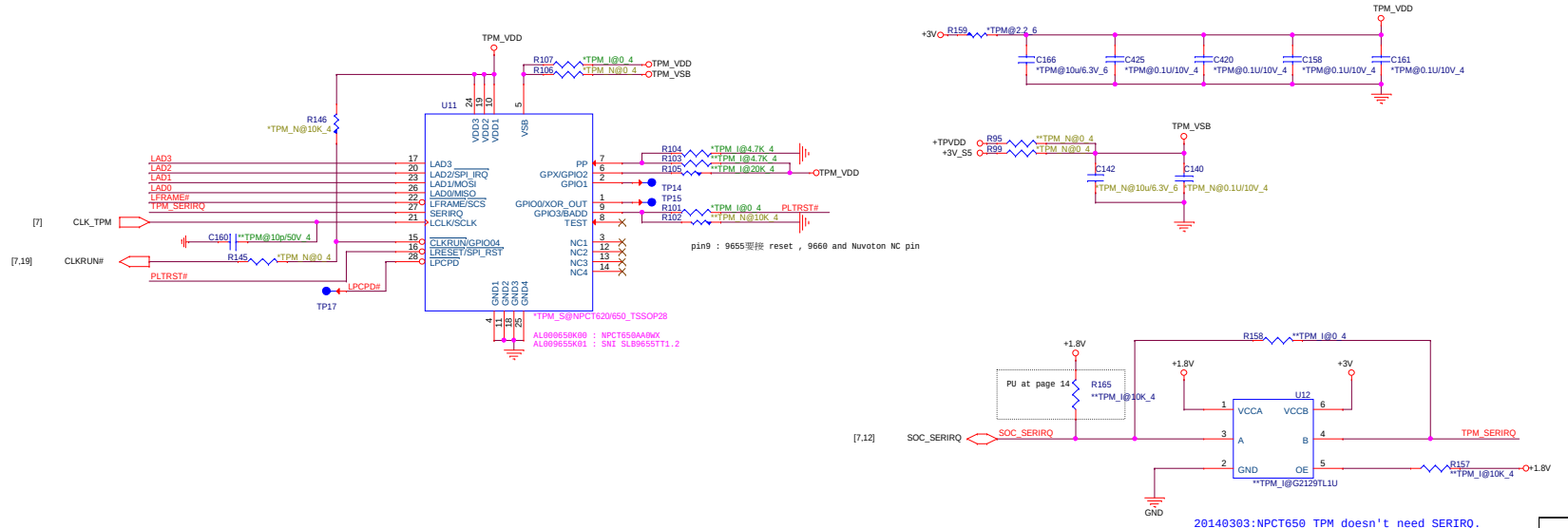
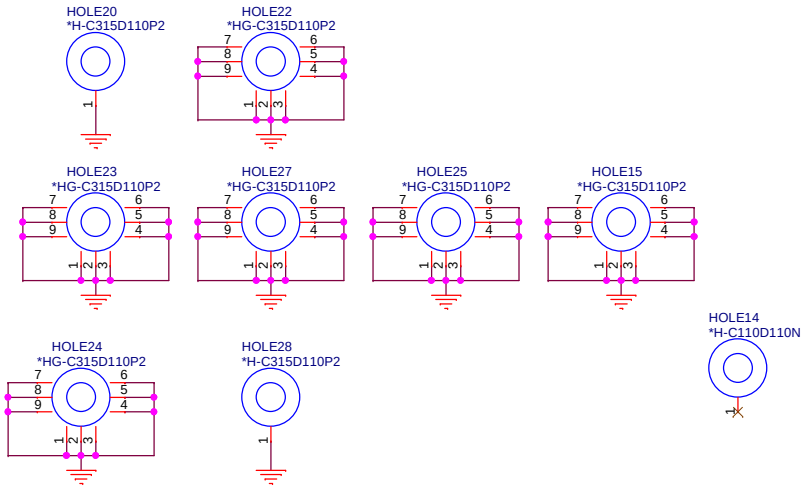
WLAN

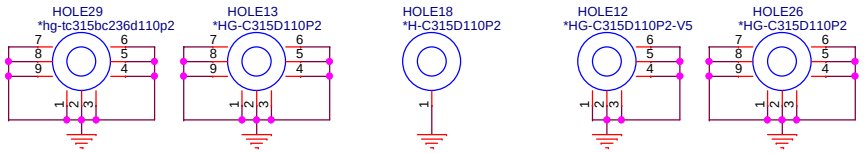

Unmount R509, R511 for broadcom WLAN LED issue
CN14
WLAN CONN
BT_POWERON
PLTRST#
CLK_24M_DEBUG
PCIE_TXP2_WLAN
PCIE_TXN2_WLAN
PCIE_RXP2_WLAN
PCIE_RXN2_WLAN
CLK_PCIE_WLANP
CLK_PCIE_WLANN
CLK_PCIE_WLAN_REQ#_R
PCIE_WAKE#_R
WPAN_LED#
WLAN_LED#
WIMAX_LED#
WLAN_CLK_SDATA
WLAN_CLK_SCLK
IOAC_PCIERST#
PLTRST#_2
RF_EN
LFRAME# C
LAD3_C
LAD2_C
LAD1_C
LAD0_C
LFRAME#
LAD3
LAD2
LAD1
LAD0
USBP2+
USBP2-
TP44
+3V_Mini1_VDD
+3V_S5
+3V
+1.8V
PCIE_CLKREQ2_WLAN#
CLK_PCIE_WLAN_REQ#_R
WAKE_SRC_1
PCIE_WAKE#_R
Q25
PJA138K
Q26
*PJA138K
*2N7002DW
Q20
SMB_RUN_DAT
SMB_RUN_CLK
WLAN_CLK_SDATA
WLAN_CLK_SCLK
+TPVDD
+3V
+1.8V
+3V_S5

TPM (TPM)

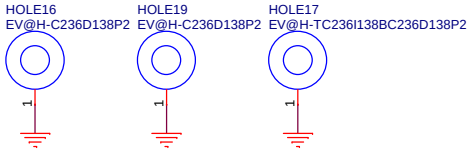

TPM_VDD
TPM_VSB
U11
CLK_TPM
CLKRUN#
PLTRST#
LPCPD#
TP17
TP14
TP15
pin9 : 9655要接 reset , 9660 and Nuvoton NC pin
*TPM_S@NPCT620/650_TSSOP28
AL000650K00 : NPCT650AA0WX
AL009655K01 : SNI SLB9655TT1.2
U12
SOC_SERIRQ
TPM_SERIRQ
**TPM_I@G2129TL1U
20140303:NPCT650 TPM doesn't need SERIRQ.

HOLE(OTH)

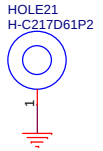




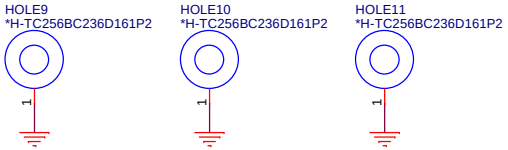
GPU nuts

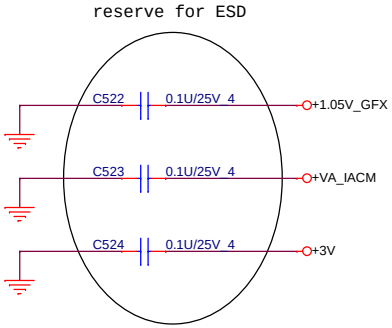


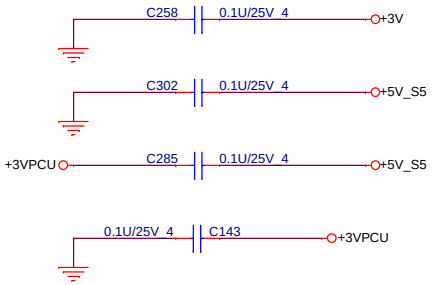
Mini card nuts

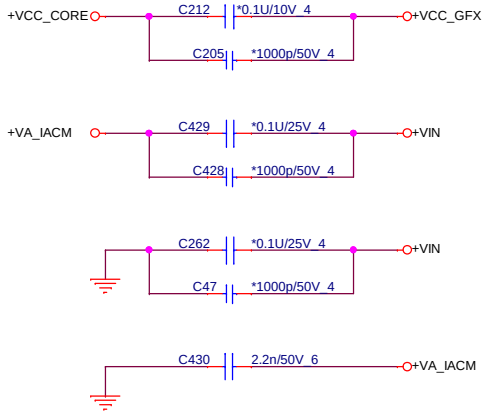


CPU nuts









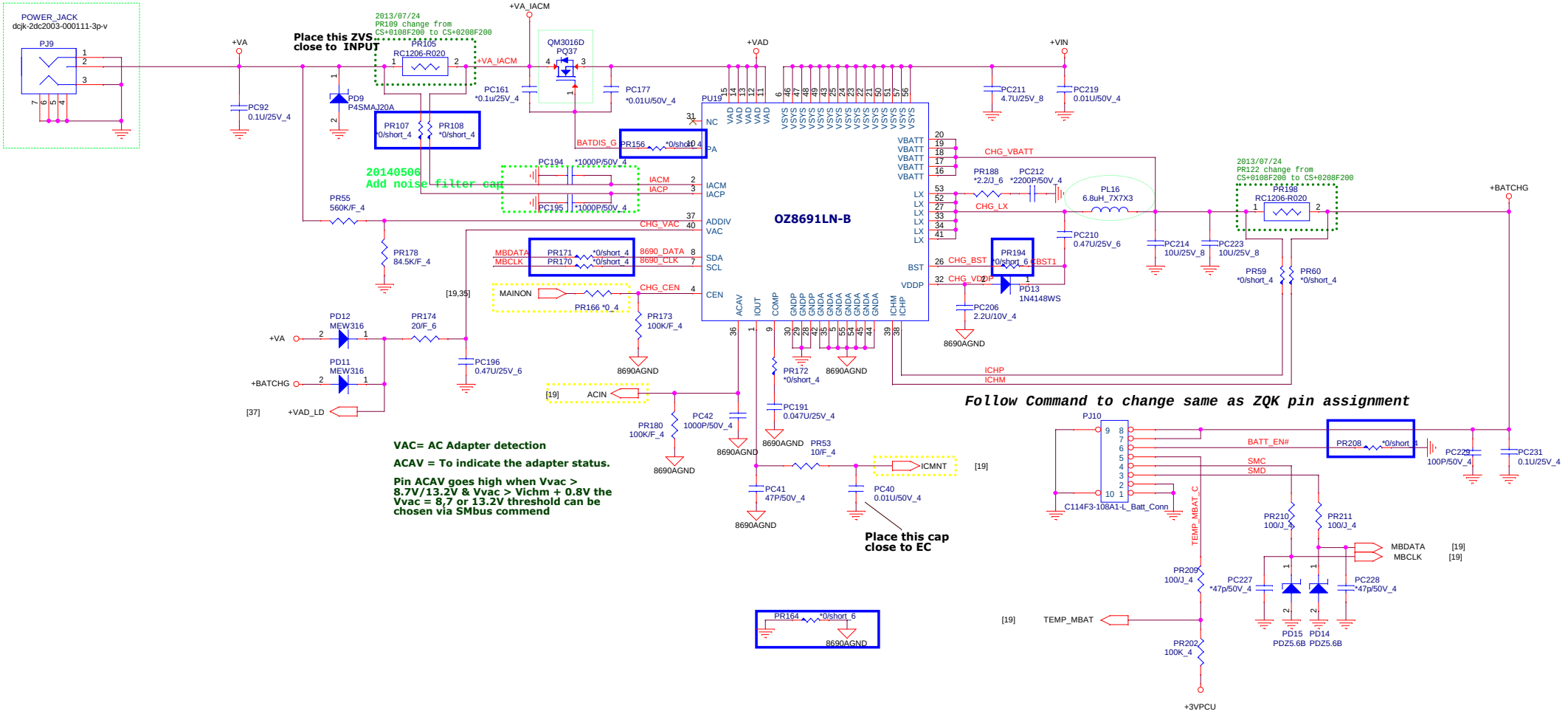
Quanta Computer Inc.

PROJECT : ZYL/ZYLA

Size	Document Number	Rev
	USB BOARD CONN	1A
Date: Thursday, July 10, 2014	Sheet 29 of 44	

DFPJ06MR013-- 95W
DFPJ06MR007--- 45W

ZE7



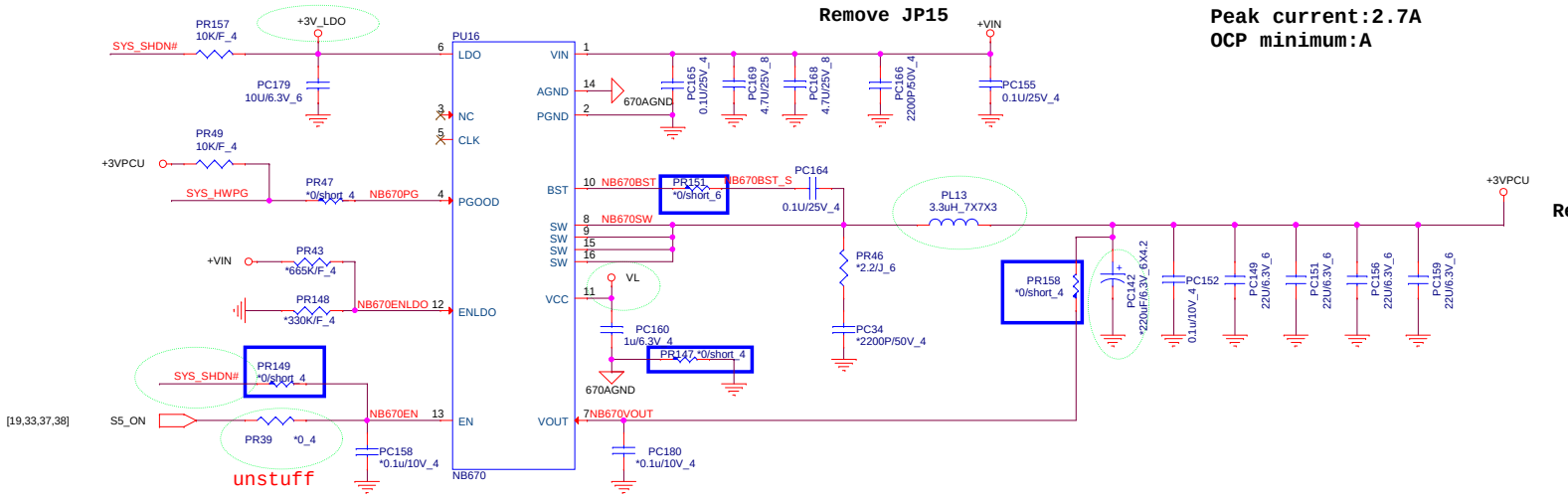
Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: Charger (OZ8690ALN)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 30 of 44	

DC/DC +3VPCU/+5V_S5

LDO(MAX)=100mA

+3.3 Volt +/- 5%
Countinue current:2A
Peak current:2.7A
OCP minimum:A

Remove JP15

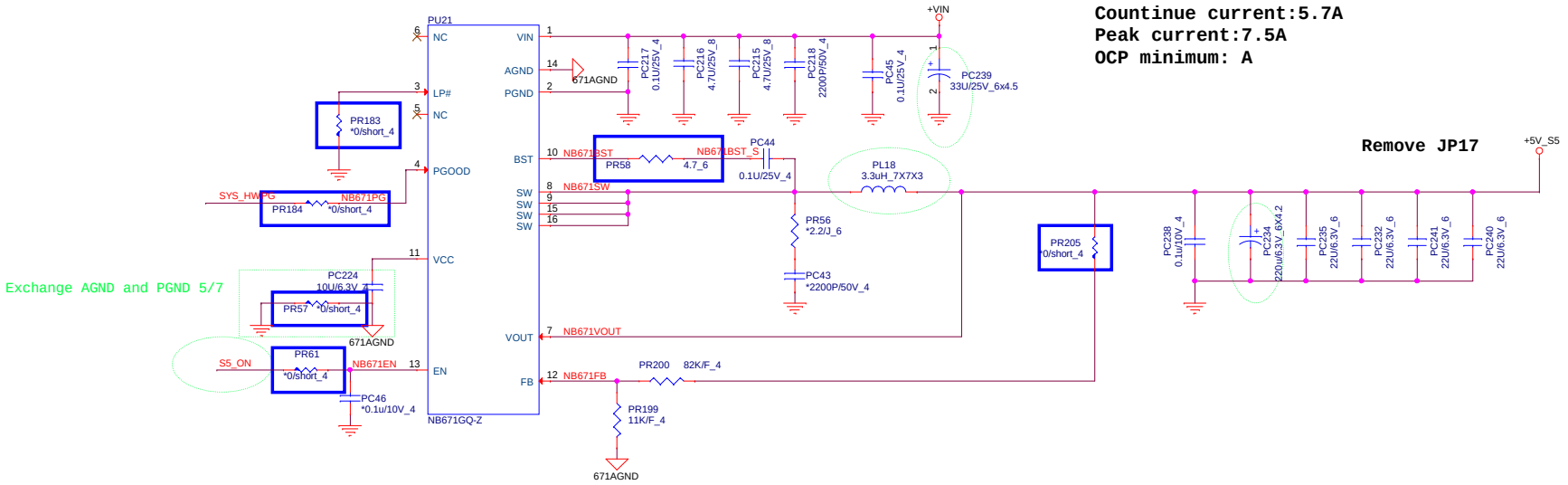


unstuff

Remove JP13

Remove JP18

+5 Volt +/- 5%
Countinue current:5.7A
Peak current:7.5A
OCP minimum: A



Exchange AGND and PGND 5/7

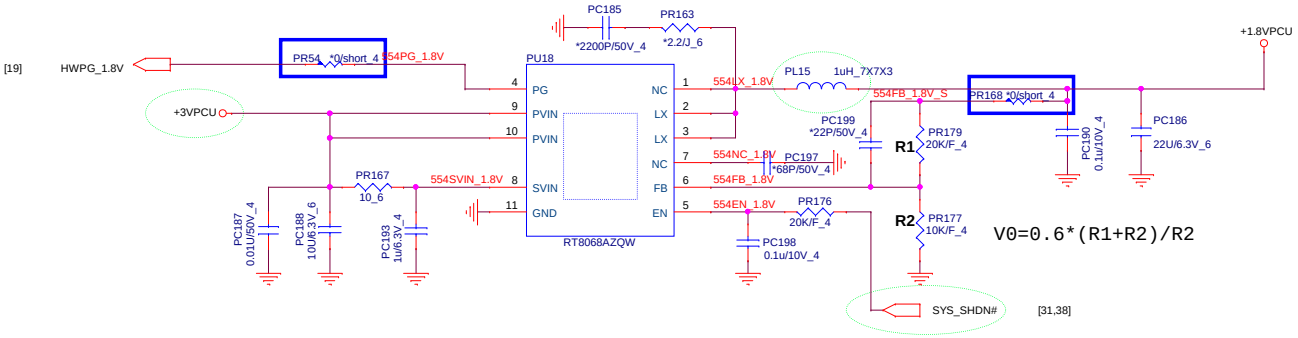
Remove JP17

Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: 3/5VS5 (NB670/NB669)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 31 of 44	

[12,19,37] +1.8VPCU

[6,8,19,21,22,25,26,30,31,37,39,40] +3VPCU

+1.8V Volt +/- 5%
Countinue current:0.08A
Peak current:0.11A
OCP minimum:A

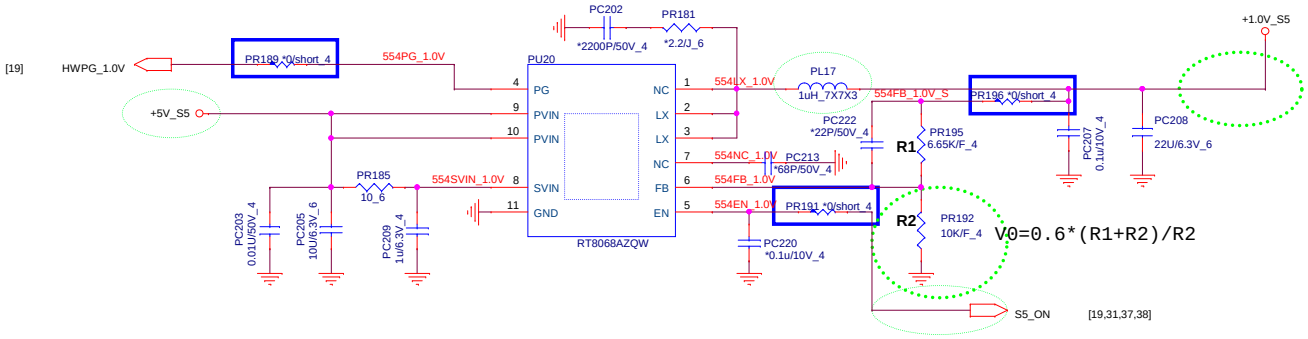


removed PR161 and PR165

Quanta Computer Inc.			
PROJECT : ZHJ			
Size	Document Number +1.8VPCU		Rev 1A
Date: Thursday, July 10, 2014	Sheet 32 of 44		

[9,37] +1.0V_S5
[24,25,31,34,35,36,37,39] +5V_S5
[2,9,12,19,21,24,27,28,34,35,37,39,40] +3V_S5

+1.0V Volt +/- 5%
Countinue current:2.4A
Peak current:3.2A
OCP minimum:A



removed PR169 ,PR175 and PR182

20140609:
Change PR192 from 10K to 9.31K Ohm

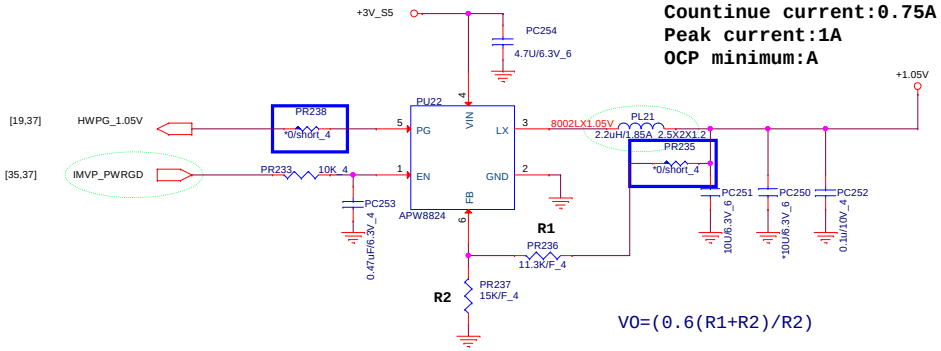
Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: +1.0V	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 33 of 44	

[2,9,12,19,21,24,27,28,35,37,39,40] +3V_S5

[5,9] +1.05V

[9,22,23,26] +1.5V

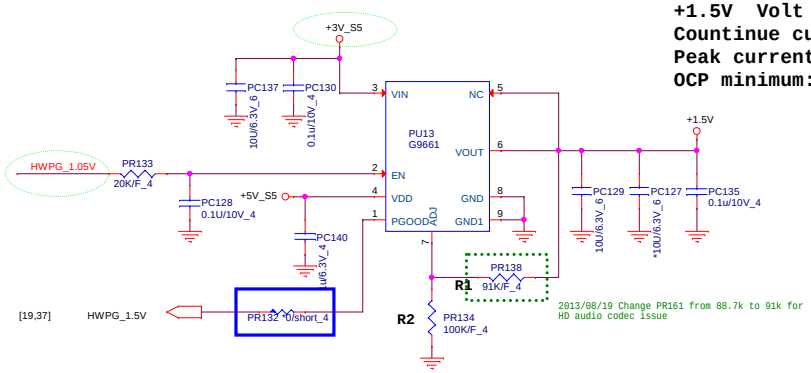
+1.05V Volt +/- 5%
Countinue current:0.75A
Peak current:1A
OCP minimum:A



removed PR232 and PR234

VO=(0.6(R1+R2)/R2)

+1.5V Volt +/- 5%
Countinue current:0.023A
Peak current:0.03A
OCP minimum:A



2013/08/19 Change PR161 from 88.7k to 91k for HD audio codec issue

VO=(0.8(R1+R2)/R2)
R2<120Kohm

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	+1.05V/1.5V	1A

Date: Thursday, July 10, 2014 Sheet 34 of 44

20130617 Change +1.05V to +1.0V

Close to VR

VR_SVID_ALERT# close to CPU

VR_SVID_DATA and VR_SVID_CLK close to VR

[6,9,37] +1.0V
[8,9,29] +VCC_GFX
[20,29,30,31,36,37,38,39,40] +VIN
[24,25,31,33,34,36,37,39] +5V_S5

Parallel

Close to the CPU side.

PU9 ISL95833HRTZ-T

AXG

Remove JP19

DCR=4.2mOhm

+VCC_GFX
TDC : A
PEAK : 14A
OCP : A
Width : mil

GFX_CORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with AXG inductor

Core

Remove JP20

DCR=4.2mOhm

+VCC_CORE
TDC : A
PEAK : 12A
OCP : A
Width : mil

VCORE Load Line : -5.9mV/A for 2.xW SDP

Close to the VR side.

Close with phase1 inductor

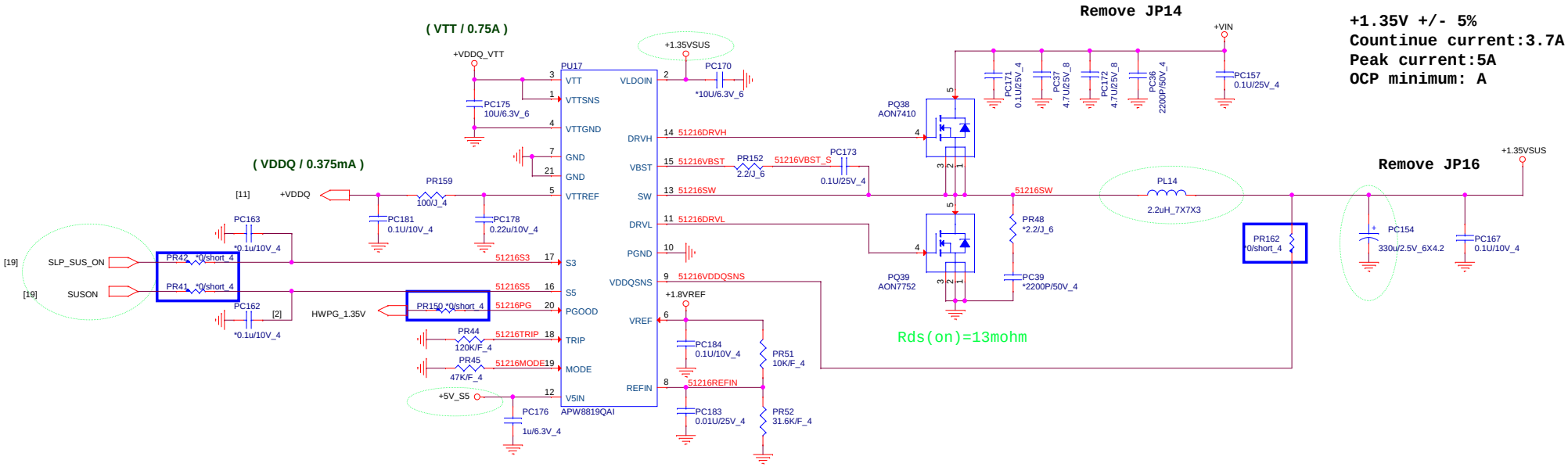
Quanta Computer Inc.
PROJECT : ZHJ

Size | Document Number: +VCC_CORE/+VGFX (ISL95833) | Rev: 1A
Date: Thursday, July 10, 2014 | Sheet 35 of 44

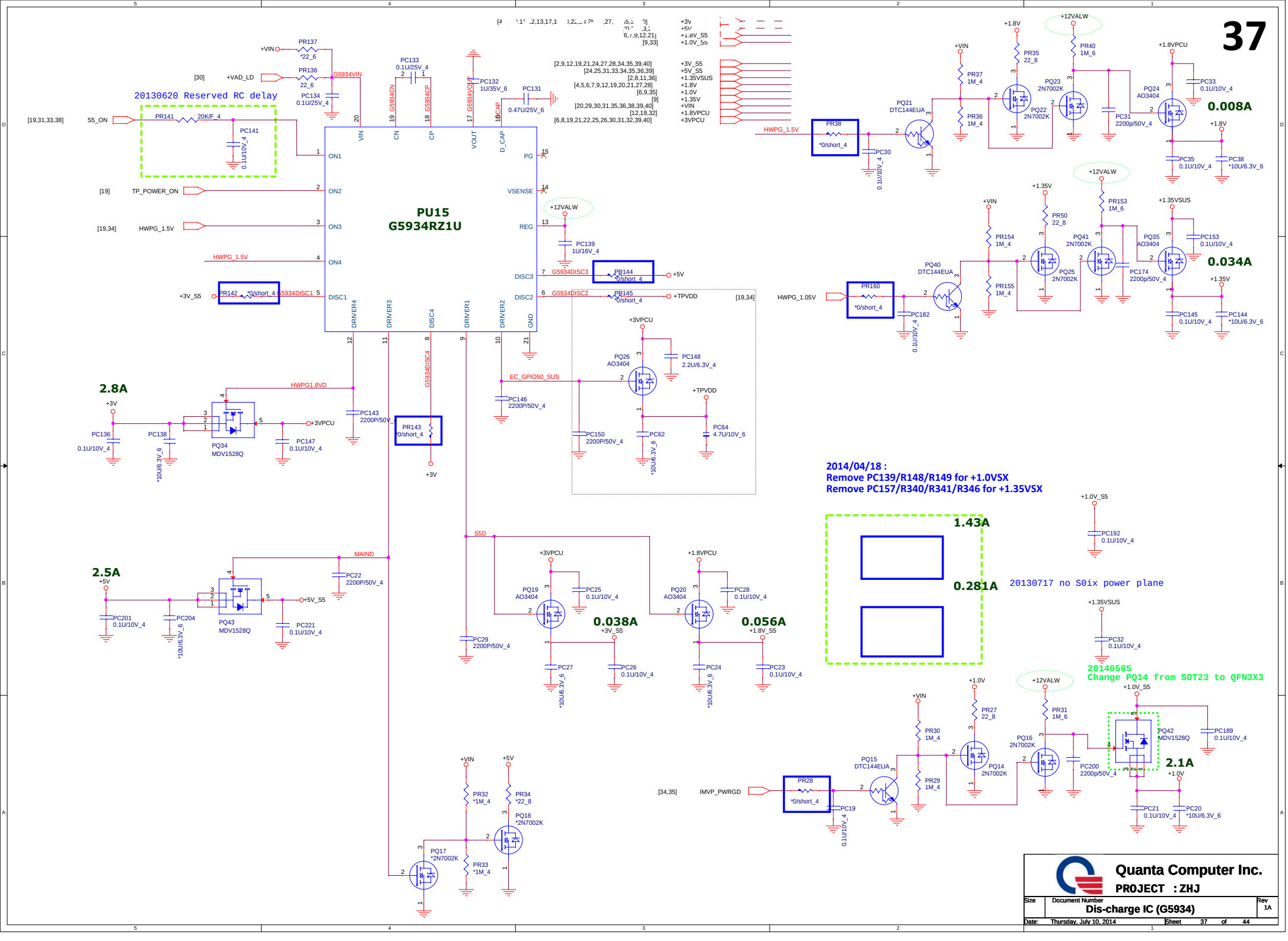
[2,8,11,37] +1.35VSUS

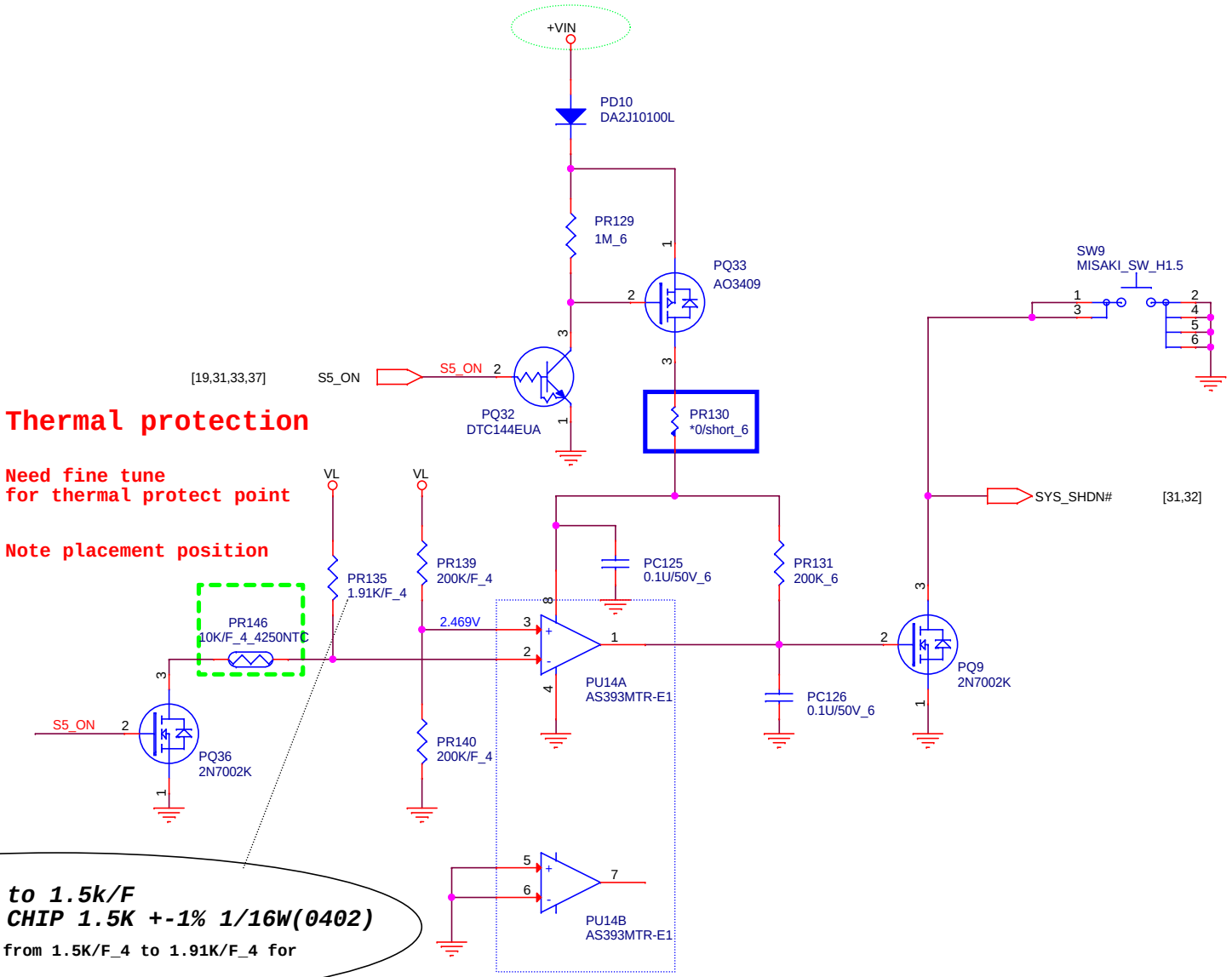
[11] +VDDQ_VTT

[24,25,31,33,34,35,37,39] +5V_S5



Quanta Computer Inc.		
PROJECT : ZHJ		
Size	Document Number: DDR3 (APW8819)	Rev: 1A
Date: Thursday, July 10, 2014	Sheet 36 of 44	


PU15
G5934RZ1U
20130620 Reserved RC delay
2.8A
2.5A
1.43A
0.281A
0.038A
0.056A
0.008A
0.034A
2.1A
2014/04/18 :
Remove PC139/R148/R149 for +1.0VSX
Remove PC157/R340/R341/R346 for +1.35VSX
20130717 no S0ix power plane
20140505
Change PQ14 from SOT23 to QFN3X3
Quanta Computer Inc.
PROJECT : ZHJ
Dis-charge IC (G5934)
Thursday, July 10, 2014
Sheet 37 of 44



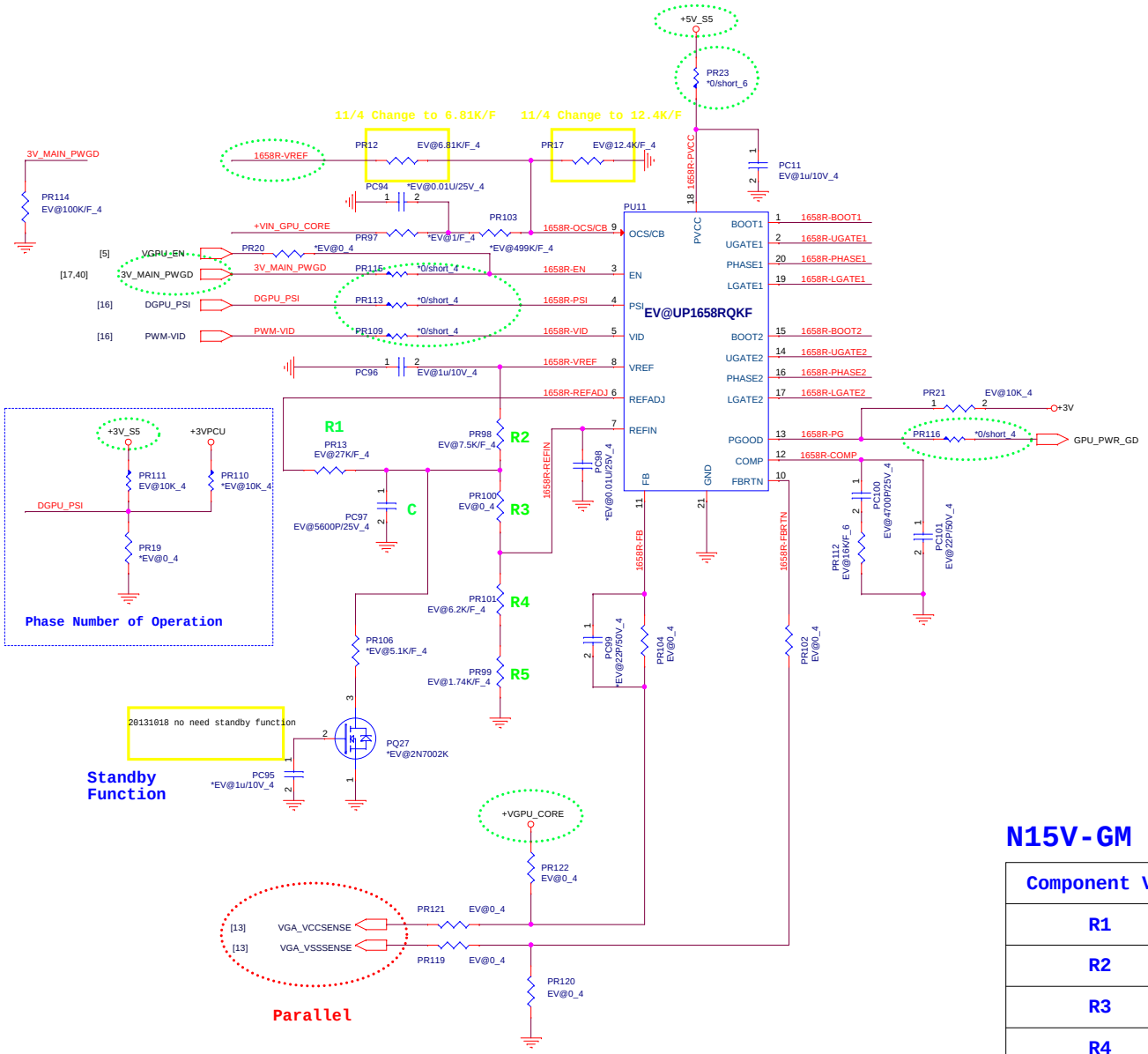
note: PR173 change to 1.5k/F
CS21502FB14 RES CHIP 1.5K +-1% 1/16W(0402)

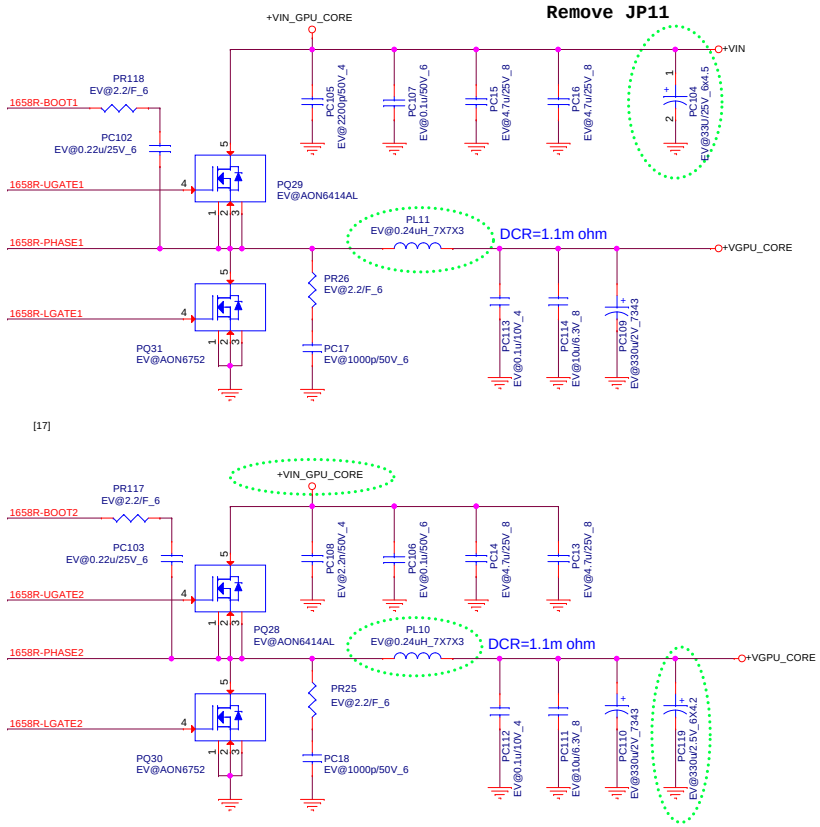
20140702 Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request

For EC control thermal protection (output 3.3V)

Quanta Computer Inc.
PROJECT : ZHJ

Size	Document Number	Rev
	Thermal / Hole	1A
Date: Thursday, July 10, 2014	Sheet 38 of 44	





N15V-GM

Component Value	Config D
R1	27K
R2	7.5K
R3	0
R4	6.2K
R5	1.74K
C	5.6nF

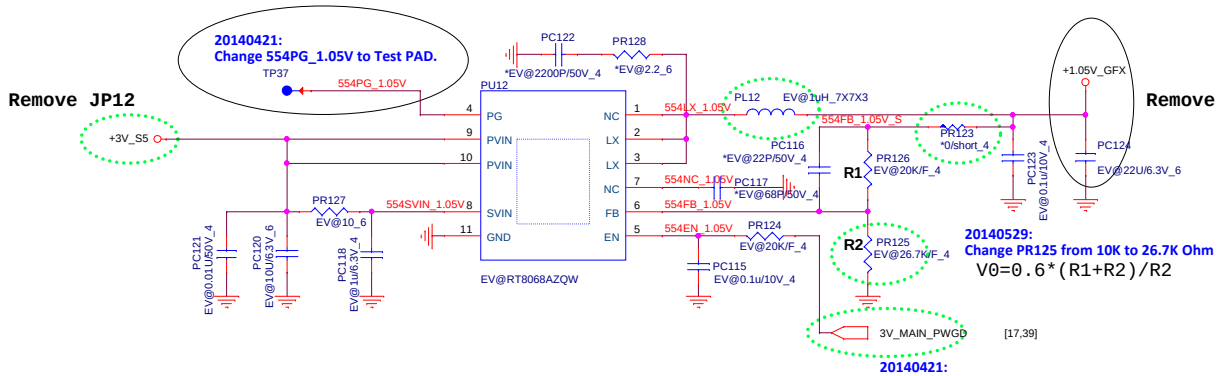
N15V-GM

+VGPU_CORE
Countinue current:33.5A
Peak current:51.5A
OCP:75A
FSW:300KHz
L/L=0mV/A

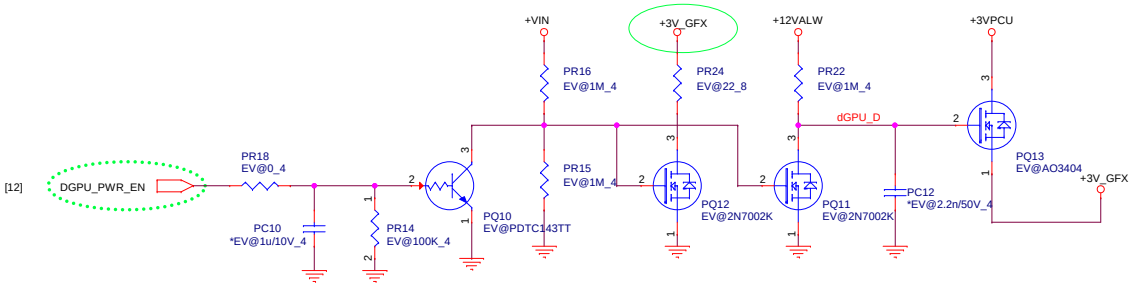
Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+VGPU_CORE (UP1658RQKF)	1A
Date: Thursday, July 10, 2014	Sheet 39 of 44	

[13,14,15] +1.05V_GFX
[13,14,18] +1.5V_GFX
[13,16,17] +3V_GFX

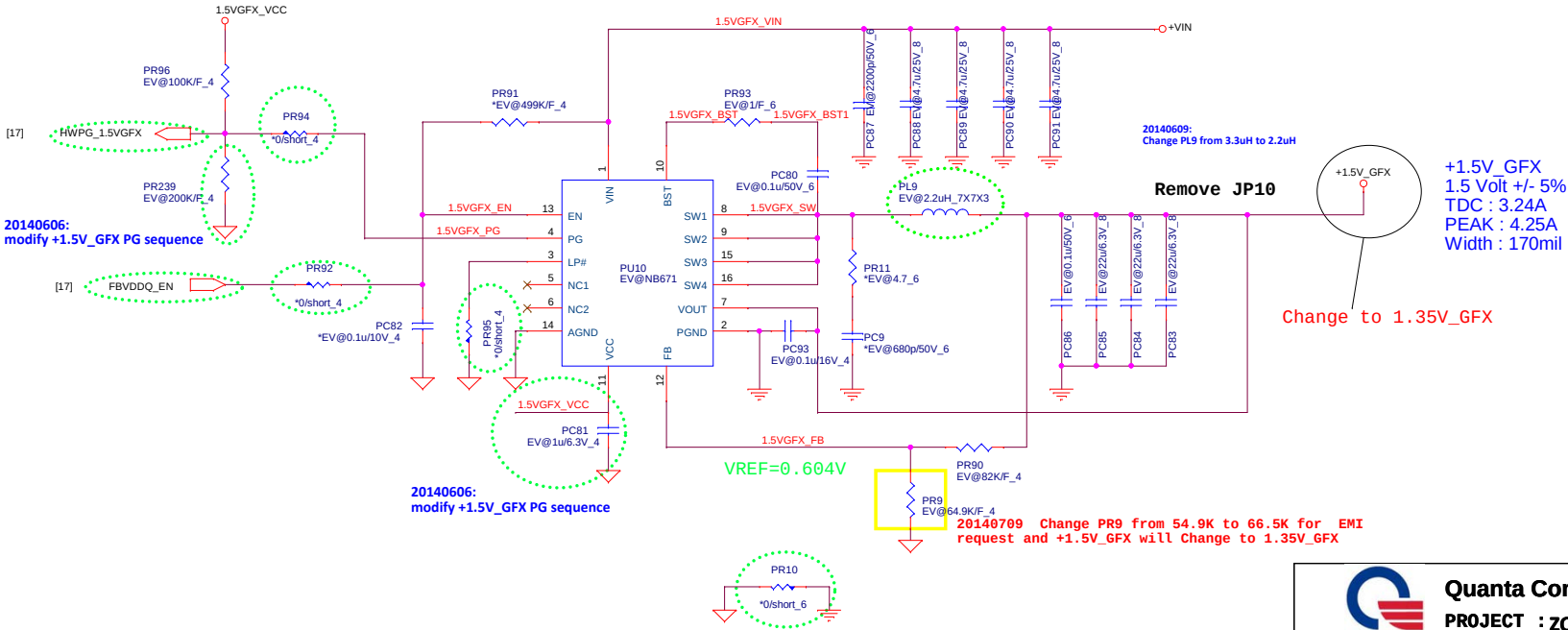


+1.05V_GFX
TDC : 1.553A
PEAK : 2.29A
Width : 90mil



+3V_GFX
TDC : 0.17A
PEAK : 0.342A
Width : 20mil

Remove JP9



+1.5V_GFX
1.5 Volt +/- 5%
TDC : 3.24A
PEAK : 4.25A
Width : 170mil

Quanta Computer Inc.
PROJECT : ZQ0

Size	Document Number	Rev
	+1.5V_GFX/+1.05V_GFX/+3V_GFX	1A

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Bay Trail-M Power On Timing with all Sx (S0 to S5)

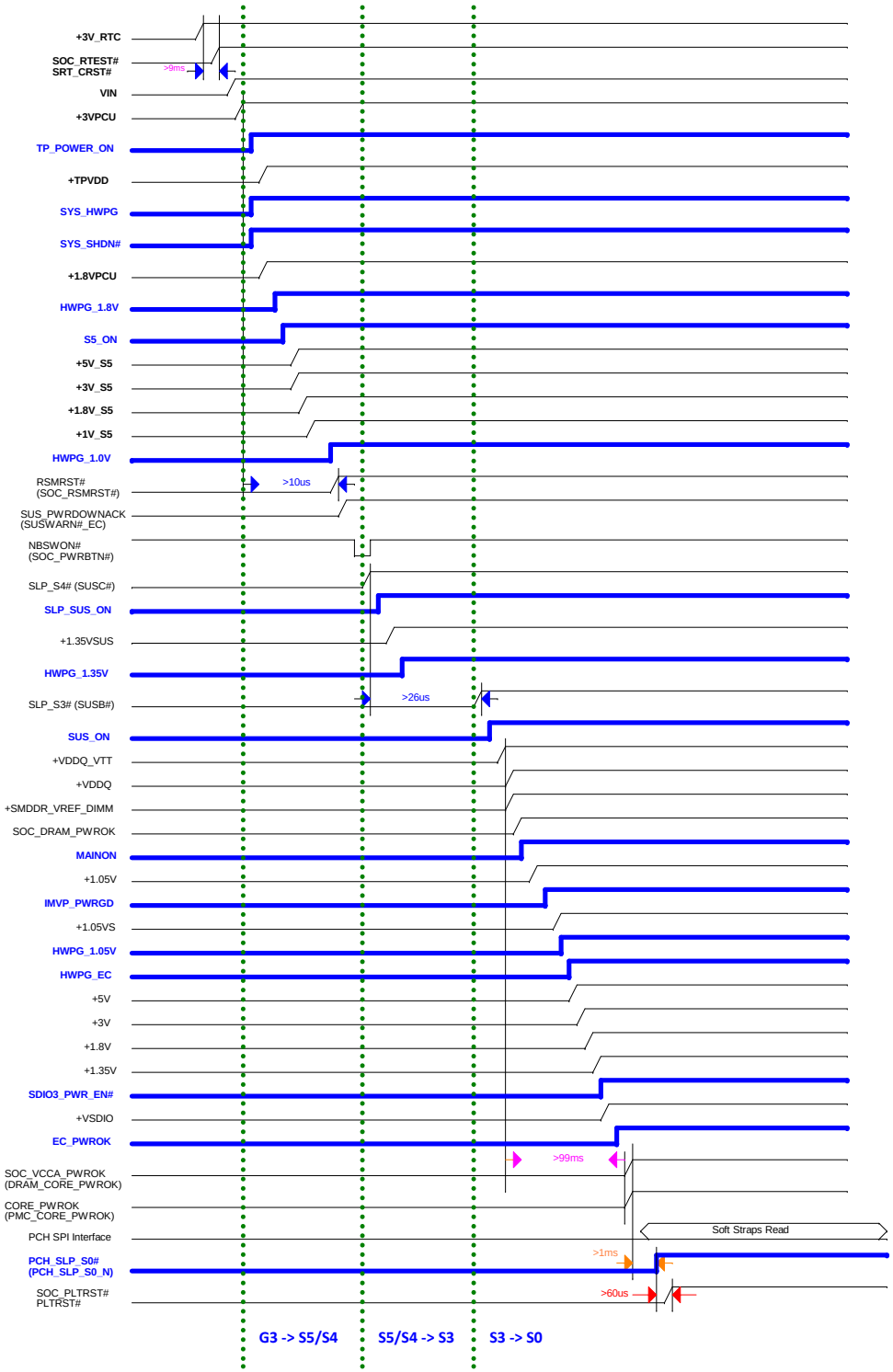
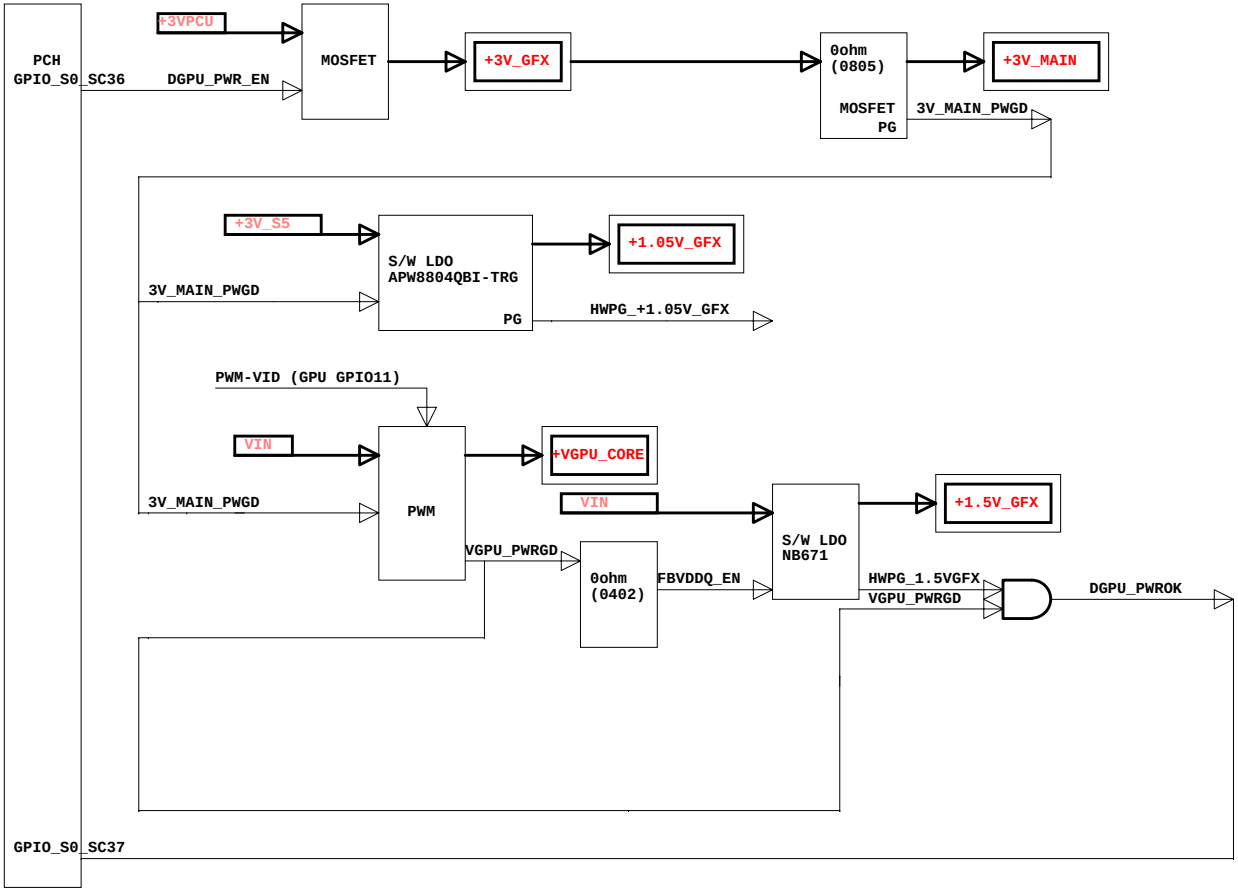


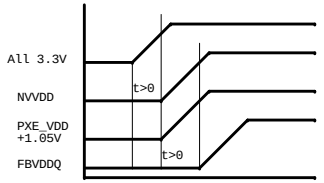
Table 37. SoC Sx-States to SLP_S*#

State	S0	S3	S4	S5	Reset w/o Power Cycle	Reset w/ Power Cycle
CPU Executing	In C0	OFF	OFF	OFF	No	OFF
PMC_SLP_S3#	HIGH	LOW	LOW	LOW	HIGH	LOW
PMC_SLP_S4#	HIGH	HIGH	LOW	LOW	HIGH	LOW
S0 Power Rails	ON	OFF	OFF	OFF	ON	OFF
PMC_PLTRST#	HIGH	LOW	LOW	LOW	LOW	LOW
PMC_SUS_STAT#	HIGH	LOW	LOW	LOW	HIGH	LOW
PCIe Links	L0, L1	L3	L3	L3	L3 Ready	L3

NOTES: The processor treats S4 and S5 requests the same. The processor does not have PMC_SLP_S5#. PMC_SUS_STAT# is required to drive low (asserted) even if core well is left on because PMC_SUS_STAT# also warns of upcoming reset.

VGA power up sequence

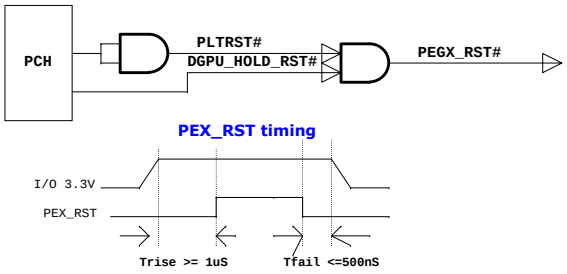




N15x Power on sequance

Notes: -All 3.3V includes all rails powered at 3.3V
-PEX_VDD 1.05V inculdes all rails that are shared

VGA Reset

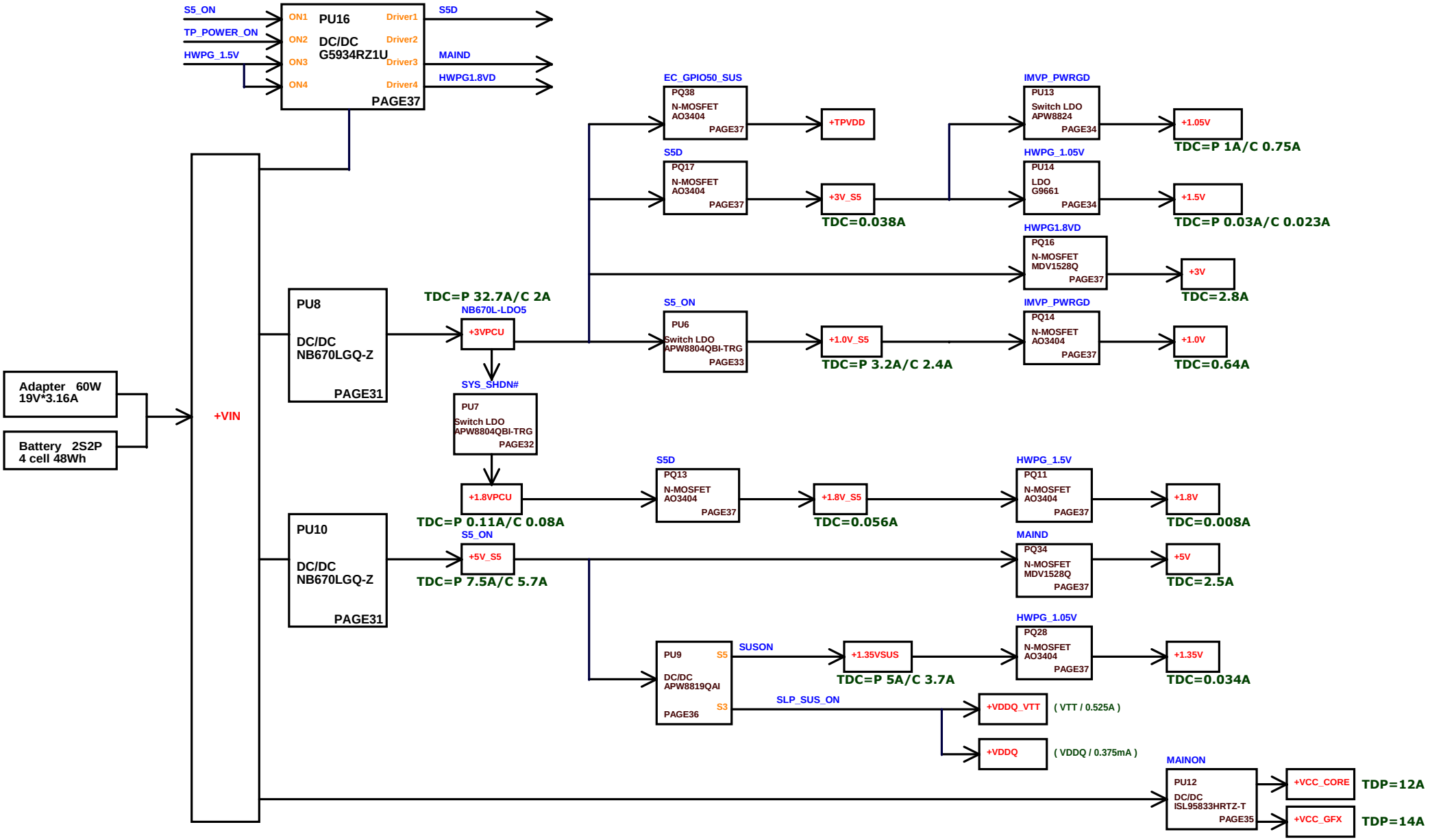


Quanta Computer Inc.
PROJECT : ZYL

Size	Document Number	Rev
	GPU PWR CRL	1A

Date: Thursday, July 10, 2014 Sheet 42 of 44

ZYL POWER BLOCK DIAGRAM



Quanta Computer Inc.
PROJECT : ZYL

Size	Document Number	Rev
	ZYL Power Block Diagram	1A

Date: Thursday, July 10, 2014 Sheet 43 of 44

Model	Date	CHANGE LIST
ZYL REV:A		1. FIRST RELEASED
		Check CPU of P/N. ***Change VRAM of P/N.*** ***Check PJ6 for UMA or Dis- GVA.***
		VGA Chip (Buy and Sell) ***AJ0N15V0T07*** ***VR4GbIII9:*** ***HYNIX Graphic DDRIII 900 4Gb H5TC4G63AFR-11C*** ***AKD5PGWTW13 (B/S)*** ***MICRON Graphic DDRIII 900 4Gb MT41J256M16HA-093G:E*** ***AKD5PZSTL05 (B/S)*** ***SAMSUNG Graphic DDRIII 900 4Gb K4W4G1646D-BC1A*** ***AKD5PGWT504 (B/S)*** CPU (Buy and Sell) Intel Baytrial M cpu n3530 VGA Chip (Buy and Sell) AJ0N15V0T07 VRAM (Buy and Sell) VR2GbIII9 HYNIX Graphic DDRIII 900 2Gb H5TC2G63FFR-11C AKD5MZDTW04 ; AKD5MZDTW05 (B/S) MICRON Graphic DDRIII 900 2Gb MT41J128M16JT-093G:K AKD5MGSTL15 ; AKD5MGSTL25 (B/S) SAMSUNG Graphic DDRIII 900 2Gb K4W2G1646Q-BC1A AKD5MGST511 ; AKD5MGST513 (B/S)
ZYL REV:B	5/27	1.PAGE.22 , modify SW10 pin3 connect to pin1 ,pin2 connect to pin4&pin5&pin6 2.PAGE.24 , modify CN16 & CN18 footprint from "USB-TARA4-9B1323-9P-SMT" to "UB2-UARDM-4K1926-4P-R"
	5/28	1.PAGE.25 , SWAP CN23 USB_CAR_N & USB_CAR_P
	5/29	1.PAGE.40 , Change PR125 from 10K to 26.7K due to 1.05V_GFX output is incorrect
	6/6	1.PAGE.6 , Change C458、C453 from 10P/50V to 12P/50V 2.PAGE.40 , Add PR239 to modify +1.5V_GFX PG sequence
	6/9	1.PAGE.29 , change hole 18、hole20、hole28 footprint from "HG-C315D110P2" to "H-C315D110P2" 2.PAGE.19 , Add D37 D38 C521 3.PAGE.20 , change R66 R67 R69 R70 R71 R73 R74 R76 from 620ohm to 619 ohm 4.PAGE.29 , Change C430 from "CH22206K917" to "CH22206J911" 5.PAGE.22 , Change C464 C466 C468 C469 from "0.01u/16V_4" to "0.01u/25V_4"
	6/10	1.PAGE.29 , reserve & mount C522 C523 C524 for ESD 2.PAGE.40 , Change PL9 from 3.3uH to 2.2uH for modified 1.5V_GFX efficiency.
	6/11	1.PAGE.24 , delete R465 R468 R522 R530 & mount L28,L31 for EMI
	6/13	1.PAGE.7 , PAGE.26,PAGE.28 , unmount R427,C310,R452,R453 2.PAGE.19 , mount D16 and change value form 14V/38V to 5V/30V 3.PAGE.26 , mount C338,C339,C340,C341 for EMI
ZYL REV:C	6/25	1.PAGE.6 , Change G9、G10 footprint from "SOLDERJUMPER-2" to "RC0603-C" 2.PAGE.26 , Change R311、R324、R565、R562、R550、R566 、L23、R13 from "0ohm" to "shortpad"
	6/27	1.PAGE.7 & 28 , Unmount R411 & Delete R147,R148,R149 2.PAGE.9 , Delete R180 for CPU +1.0V voltage
	7/1	1.PAGE.24 & 25 , Change C279,C224,C414 from 100u/6.3V_3216 to 100U/6.3V_3528
	7/2	1.PAGE.38 , Change PR135 from 1.5K/F_4 to 1.91K/F_4 for thermal request
	7/9	1.PAGE.40 , Change PR9 from 54.9K to 64.9K for EMI request and +1.5V_GFX will Change to 1.35V_GFX

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		PART NUMBER:		DRAWING BY:		REVISON: