1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
6	0002265654	ENGINEERING RELEASED	2013-08-22

SCHEM,MLB_KEPLER,J45G

8/22/2013 DVT

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30	30	Thunderbolt Mobile Support	CLEAN_J45	04/26/2013
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35	39	Camera 1 of 2	CLEAN_J45	04/26/2013
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38	48	KEYBOARD/TRACKPAD (1 OF 2)	CLEAN_J45	04/26/2013
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40	50	SMC	CLEAN_J45	04/26/2013
41	51	SMC Shared Support	CLEAN_J45	04/26/2013
42	52	SMC Project Support	CLEAN_J45	04/26/2013
43	53	SMBus Connections	CLEAN_J45	04/26/2013
44	54	High Side Voltage and Current Sensing	CLEAN_J45	04/26/2013
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46	56	Debug Sensors	CLEAN_J45	04/26/2013
47	58	Thermal Sensors	CLEAN_J45	04/26/2013
48	60	Fan Connectors	CLEAN_J45	06/23/2013
49	61	SPI ROM / LPC+SPI Conn.	CLEAN_J45	04/26/2013
50	62	AUDIO:CODEC, ANALOG	CLEAN_J45	04/26/2013
51	63	AUDIO:CODEC, DIGITAL	CLEAN_J45	04/26/2013
52	64	AUDIO: SPEAKER AMP	CLEAN_J45	04/26/2013
53	65	AUDIO: JACK	CLEAN_J45	04/26/2013
54	66	AUDIO: JACK TRANSLATORS	CLEAN_J45	04/26/2013
55	70	DC-In & Battery Connectors	CLEAN_J45	04/26/2013
56	71	PBus Supply & Battery Charger	CLEAN_J45	04/26/2013
57	72	CPU VR12.5 VCC Regulator IC	CLEAN_J45	04/26/2013
58	73	CPU VR12.5 VCC Power Stage	CLEAN_J45	04/26/2013
59	74	1.35V DDR3L SUPPLY	CLEAN_J45	04/26/2013
60	75	5V / 3.3V Power Supply	CLEAN_J45	04/26/2013
61	76	1V05V POWER SUPPLY	CLEAN_J45	04/26/2013
62	77	LCD/KBD Backlight Driver	CLEAN_J45	04/26/2013
63	78	Misc Power Supplies	CLEAN_J45	04/26/2013
64	80	Power FETs	CLEAN_J45	04/26/2013
65	81	Power Control 1/ENABLE	CLEAN_J45	06/23/2013
66	82	Power Sequencing EG/PCH S0	D2_KEPLER	01/13/2012
67	83	eDP Display Connector	CLEAN_J45	04/26/2013
68	84	KEPLER PCI-E	D2_MLB	07/31/2012
69	85	KEPLER CORE/FB POWER	D2_MLB	07/31/2012
70	86	KEPLER FRAME BUFFER I/F	D2_MLB	07/31/2012
71	87	1V05 GPU / 1V35 FB POWER SUPPLY	D2_MLB	07/31/2012
72	88	GDDR5 Frame Buffer A	D2_MLB	07/31/2012
73	89	GDDR5 Frame Buffer B	D2_MLB	07/31/2012
74	90	KEPLER EDP/DP/GPIO	D2_MLB	07/31/2012
75	91	KEPLER GPIOS,CLK & STRAPS	D2_MLB	07/31/2012
76	92	KEPLER PEX PWR/GNDS	D2_MLB	07/31/2012
77	93	GFX IMVP VCore Regulator	D2_MLB	07/31/2012
78	95	RIO Connectors	CLEAN_J45	04/26/2013
79	96	eDP Mux	D2_MLB	07/31/2012
80	97	eDP Muxed Graphics Support	CLEAN_D2	08/14/2012
81	100	Power Aliases	CLEAN_J45	04/26/2013
82	102	Signal Aliases	CLEAN_J45	04/26/2013
83	104	Functional Test Points	CLEAN_J45	04/26/2013
84	105	NC & No Test	CLEAN_J45	04/26/2013
85	110	PCB Rule Definitions	CLEAN_J45	04/26/2013
86	111	CPU Constraints	CLEAN_J45	04/26/2013
87	112	PCH Constraints 1	CLEAN_J45	04/26/2013
88	113	PCH Constraints 2	CLEAN_J45	04/26/2013
89	114	Memory Constraints	CLEAN_J45	04/26/2013
90	115	Thunderbolt Constraints	CLEAN_J45	04/26/2013
91	116	Camera Constraints	CLEAN_J45	04/26/2013
92	117	SMC Constraints	CLEAN_J45	04/26/2013
93	118	Project Specific Constraints	CLEAN_J45	04/26/2013
94	119	GPU (Kepler) Constraints	SIDLE_J15	09/02/2012

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-0675	1	SCHEM,MLB_KEPLER,J45G	SCH	CRITICAL	
820-3787	1	PCBF,MLB_KEPLER,J45G	PCB	CRITICAL	

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TITLE=MLB
ABBREV=ABBREV
LAST_MODIFIED=Thu Aug 22 12:19:14 2013

DRAWING TITLE: SCHEM,MLB,KEPLER,J45G

Apple Inc.

DRAWING NUMBER: 051-0675 | SIZE: D
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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-0177	COMMON PARTS,MLB,KEPLER,J45	J45G_COMMON
985-0181	DEV,MLB,KEPLER,J45	J45G_DEVEL:DVT
639-5245	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5246	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5247	PCBA,MLB,KEPLER,CRW_BSET,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5248	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5249	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5250	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5251	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5252	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5253	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5254	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5255	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5256	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5257	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_HYNIX_A_DIE
639-5258	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_2G_ELPIDA
639-5259	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_HYNIX_A_DIE
639-5260	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_2G_ELPIDA
639-5261	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_HYNIX_A_DIE
639-5262	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_2G_ELPIDA
639-5263	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_HYNIX_A_DIE
639-5264	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_2G_ELPIDA
639-5265	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_HYNIX_A_DIE
639-5266	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_2G_ELPIDA
639-5267	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-HYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_HYNIX_A_DIE
639-5268	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-ELP,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_2G_ELPIDA
-> 639-5478	PCBA,MLB,KEPLER,CRW_BEST,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5479	PCBA,MLB,KEPLER,CRW_BEST,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5480	PCBA,MLB,KEPLER,CRW_BEST,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5481	PCBA,MLB,KEPLER,CRW_BEST,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5482	PCBA,MLB,KEPLER,CRW_BEST,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5483	PCBA,MLB,KEPLER,CRW_BEST,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:BEST,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX
639-5484	PCBA,MLB,KEPLER,CRW_CTO,8G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600_S,FB_4G_HYNIX
639-5485	PCBA,MLB,KEPLER,CRW_CTO,8G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600_S,FB_4G_HYNIX
639-5486	PCBA,MLB,KEPLER,CRW_CTO,8G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600_S,FB_4G_HYNIX
639-5487	PCBA,MLB,KEPLER,CRW_CTO,16G-HYN,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_HYNIX_1600,FB_4G_HYNIX
639-5488	PCBA,MLB,KEPLER,CRW_CTO,16G-MIC,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_MICRON_1600,FB_4G_HYNIX
639-5489	PCBA,MLB,KEPLER,CRW_CTO,16G-ELP,VR-4GHYN,J45G	BASE_BOM,DEVEL_BOM,CPU_CRW:CTO,RAM:4Gb_ELPIDA_1600,FB_4G_HYNIX

J45G BOM Groups

BOM GROUP	BOM OPTIONS
J45G_COMMON	ALTERNATE,COMMON,J45G_COMMON1,J45G_COMMON2,J45G_PROGPARTS,GFX_BM,ACAPS:A2
J45G_COMMON1	CPUMEM:S0,TBTHV:P15V,SKIP_5V3V3:AUDIBLE,CHGR_5V:LDO,CPUPEG:X8X8,S2_PWR:S0
J45G_COMMON2	EDP:YES,LPCPLUS_CONN:YES,LPCPLUS_R:YES,XDP,RIO_PWR:1V5,SPI:DUAL_IO,SSD_PWR_EN:GPIO,CAM_WAKE:NO
J45G_PVT	BKLT:PROD,SENSOR_NONPROD:N
J45G_PROGPARTS	SMC_PROG:PROTO4,BOOTROM_PROG:PROTO4,TBTROM:PROG,TPAD_PSOC:PROG,GFX_PROGPARTS
GFX_PROGPARTS	DPMUXMCU:PROG
J45G_DEVEL:ENG	ALTERNATE,XDP_DEBUG,S0PGOOD_ISL,DDRVREF_DAC,SENSOR_NONPROD:Y,BKLT:ENG,DBGLED,CAM_XTAL:YES,DPMUX_DEBUG
J45G_DEVEL:DVT	ALTERNATE,XDP_DEBUG,BKLT:PROD,SENSOR_NONPROD:N,DBGLED
GFX_BM	GK107:GX,DPMUX:HOCO
XDP_DEBUG	XDP_CONN,XDP_PCH

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S4599	1	IC,CPU,CRW,PRQ,C0,2.0,47W,4+3E,6M,BGA	U0500	CRITICAL	CPU_CRW:BETTER
337S4600	1	IC,CPU,CRW,PRQ,C0,2.3,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:BEST
337S4624	1	IC,CPU,CRW,PRQ,C0,2.6,47W,4+3E,6M,BGA1364	U0500	CRITICAL	CPU_CRW:CTO
337S4542	1	IC,PCH,LPT-M, HM87,C2,SR199,PRQ,20x20mm,FCBGA	U1100	CRITICAL	
338S1247	1	IC,TBT,FR-4C,A0,PRQ,CIO,SR1JC, FCBGA28B	U2800	CRITICAL	
338S1186	1	IC,BCM15700A2,S2 PCIE CMRA,8X8,208FCBGA	U3900	CRITICAL	
333S0700	1	IC,SDRAM,4GBIT,DDR3L-1600,GEMMA,96B FBGA	U4000	CRITICAL	
333S0667	16	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA	.....	CRITICAL	4Gb_HYNIX_1600_S
333S0624	16	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	.....	CRITICAL	4Gb_SAMSUNG_1600_S
333S0703	16	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P	.....	CRITICAL	4Gb_ELPIDA_1600_S
333S0660	16	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA	.....	CRITICAL	4Gb_MICRON_1600_S
333S0667	32	IC,SDRAM,4GBIT,DDR3L-1600,HUMA,78P FBGA	.....	CRITICAL	4Gb_HYNIX_1600
333S0624	32	IC,SDRAM,DDR3-1600,512MX8,78FBGA,C-DIE,SAMSUNG	.....	CRITICAL	4Gb_SAMSUNG_1600
333S0703	32	IC,SDRAM,4GBIT,DDR3L-1600,F DIE,RS,78P	.....	CRITICAL	4Gb_ELPIDA_1600
333S0660	32	IC,SDRAM,4GBIT,DDR3L-1600,V80A,78P,FBGA	.....	CRITICAL	4Gb_MICRON_1600
337S4256	1	IC,GPU,GK107-GT A2,BGA908	U8400	CRITICAL	GK107:GT
337S4427	1	IC,GPU,107GX,926MHZ,1.0375V,1.5V,FBGA908	U8400	CRITICAL	GK107:GX
337S4616	1	IC,GPU,CK107-762,A2,940MHz,5GBPS,1.2V,1.5V908BG	U8400	CRITICAL	GK107:GX2
333S0630	4	IC,SDRAM,GDDR5,64MX32,A-DIE,HYNIX	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_A_DIE
333S0631	4	IC,SDRAM,GDDR5,64MX32,D-DIE,SAMSUNG	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_SAMSUNG
333S0695	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA
333S0701	4	IC,SDRAM,GDDR5,2GBIT,5GBPS,170FBGA,EDW2032BBBG-6A-F	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_ELPIDA_29nm
333S0734	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC2H24BFR-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_2G_HYNIX_29nm
333S0685	4	IC,SDRAM,GDDR5,64MX3,HYNIX,H5GC4H24MFP-T2C	U8800,U8850,U8900,U8950	CRITICAL	FB_4G_HYNIX

DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM:2Gb_HYNIX_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:2Gb_SAMSUNG_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:2Gb_ELPIDA_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:2Gb_MICRON_1600	RAMCFG3:L,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600_S	4Gb_HYNIX_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600_S	4Gb_SAMSUNG_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600_S	4Gb_ELPIDA_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600_S	4Gb_MICRON_1600_S,RAMCFG3:L,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H
RAM:4Gb_HYNIX_1600	4Gb_HYNIX_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L
RAM:4Gb_SAMSUNG_1600	4Gb_SAMSUNG_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:L,RAMCFG0:H
RAM:4Gb_ELPIDA_1600	4Gb_ELPIDA_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:L
RAM:4Gb_MICRON_1600	4Gb_MICRON_1600,RAMCFG3:H,RAMCFG2:L,RAMCFG1:H,RAMCFG0:H

Development/Base BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-0177	1	J45G MLB,KEPLER BASE BOM	BASE	CRITICAL	BASE_BOM
985-0181	1	J45G MLB,KEPLER, DEVEL BOM	DEVEL	CRITICAL	DEVEL_BOM

SYNC_MASTER=J15 REFERENCE SYNC_DATE=07/31/2012

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Programmables - All builds

341S3920	1	IC,EEPROM,FALCON RIDGE (V13.1),J44/J45	U2890	CRITICAL	TBTROM:PROG
335S0915	1	EEPROM,SPI FLASH ROM,4MBit,50MHZ,USON8	U2890	CRITICAL	TBTROM:BLANK
335S0852	1	IC,GPUROM,D2,BLANK	U9101	CRITICAL	GPUROM:BLANK
341S3565	1	IC,EDP MUX-95C,(RENESAS) V3.2.8,DVB,D2	U9600	CRITICAL	DPMUXMCU:PROG
337S4313	1	IC,MCU,H8S/2113,9X9MM,TLP-145V	U9600	CRITICAL	DPMUXMCU:BLANK
341S3856	1	IC,TRKPD/KYBD CNTRLR,CU only,V225,J45	U4801	CRITICAL	TPAD_PSOC:PROG
337S4587	1	IC,TP PSOC,QFN,BLANK	U4801	CRITICAL	TPAD_PSOC:BLANK

SMC

338S1214	1	IC,SMC-A3,40MHZ/50DMIPS,SCPL FW,157BGA	U5000	CRITICAL	SMC_PROG:BASE
341S3901	1	IC,SMC-B1,SCPL,EXT,V2.16Q13,PROTO4,J45G	U5000	CRITICAL	SMC_PROG:PROTO4
341S3741	1	IC,SMC-A3,SCPL,EXT,VXXXX,PVT,J15	U5000	CRITICAL	SMC_PROG:PVT

EFI ROM

335S0807	1	IC,SPI SRL 50MHZ FLASH,64MBIT,8SOP,FUSE,L	U6100	CRITICAL	BOOTROM_PROG:BLANK
335S0812	1	64MBIT SPI SRL DUAL I/O FLSH,SOIC8,Z	U6100	CRITICAL	BOOTROM_PROG:BLANK2
341S3712	1	IC,EFI ROM(V0008)PROTO 0,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO
341S3742	1	IC,EFI ROM(V0013) PROTO 1,J15	U6100	CRITICAL	BOOTROM_PROG:PROTO1
341S3890	1	IC,EFI ROM(V0100) PROTO 3-J45 & EVT-J45	U6100	CRITICAL	BOOTROM_PROG:PROTO3
341S3904	1	IC,EFI ROM(V0106) PROTO 4,J45	U6100	CRITICAL	BOOTROM_PROG:PROTO4

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
128S0311	128S0329		ALL	NEC alt to Sanyo	
138S0739	138S0706		ALL	Samsung alt to Murata	
197S0481	197S0480		ALL	EPSON Alt to NDK	
371S0713	371S0558		ALL	DDS alt to ST	
152S0461	152S1645		ALL	Cyntec alt to Vishay	
376S1080	376S0820		ALL	Diodes alt to On Semi	
155S0667	155S0583		ALL	Panasonic alt to TDK	
376S1032	376S0855		ALL	Toshiba alt to Diodes	
376S1129	376S0855		ALL	NXP alt to Diodes	
376S1089	376S1128		ALL	NXP alt to Diodes	
138S0681	138S0638		ALL	Taiyo Yuden alt to Samsung	
128S0371	128S0376		ALL	Kemet alt to Sanyo	
333S0629	333S0703		ALL	Epida Alt die	
138S0803	138S0639		ALL	Samsung Alt to Murata	
138S0843	138S0674		ALL	Samsung Alt to Murata	
138S0846	138S0811		ALL	Samsung Alt to Murata	
127S0164	127S0162		ALL	Romh Alt to Vishay	
138S0732	138S0715		ALL	Romh Alt to Vishay	
128S0364	128S0264		ALL	Kemet alt to Sanyo	
333S0704	333S0700		ALL	ELPIDA to HYNIX U4000	
353S3527	353S3528		ALL	Pericom eDP MUX	FROM J15
353S3526	353S3528		ALL	TI eDP MUX	
197S0466	197S0464		ALL	Epson alt to NDK	
311S0649	311S0541		ALL	ON alt to Toshiba (U2030,U7001)	
197S0479	197S0478		ALL	Epson alt to NDK	

SYNC_MASTER=J15_REFERENCE SYNC_DATE=07/31/2012

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Frame Holes

ZT0415 2.8R2.3 — GND_BATT_CHGND

ZT0450 TH-NSP — GND_CHASSIS_FAN — SL-2.3X3.9-2.9X4.5

ZT0474 TH-NSP — GND_CHASSIS_MLBCAN5 — SL-1.1X0.45-1.4X0.75

ZT0475 TH-NSP — GND_CHASSIS_MLBCAN6 — SL-1.1X0.45-1.4X0.75

ZT0470 TH-NSP — GND_CHASSIS_MLBCAN1 — SL-1.1X0.45-1.4X0.75

ZT0471 TH-NSP — GND_CHASSIS_MLBCAN2 — SL-1.1X0.45-1.4X0.75

ZT0472 TH-NSP — GND_CHASSIS_MLBCAN3 — SL-1.1X0.45-1.4X0.75

ZT0473 TH-NSP — GND_CHASSIS_MLBCAN4 — SL-1.1X0.45-1.4X0.75

SMT GND TEST PONTS

ZT0490 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0491 2.1SM2.0MM-CIR SMT-PAD-NSP

ZT0492 2.1SM2.0MM-CIR SMT-PAD-NSP

APN 806-2247
BR0401 TH
MLB-MTG_BRKT-J5

J45 THERMAL MODULE STANDOFF

GPU BOSS APN 860-4772

SH0427 4.5OD1.85ID-1.95H

SH0428 4.5OD1.85ID-1.95H

SH0430 4.5OD1.85ID-1.95H

APN 860-1327
SH0425 STDOFF-4.5OD1.8H-SM

SH0423 STDOFF-4.5OD1.8H-SM

APN 817-0688
SH0446 STDOFF-4.9OD2.38H-SM-2

APN 817-0741
SH0445 STDOFF-4.9OD2.38H-SM-SL-2.6X2NP-2

CPU BOSS APN 860-2931

SH0420 5.0OD1.85ID-2.35H

SH0426 5.0OD1.85ID-2.35H

SH0422 5.0OD1.85ID-2.35H

SH0429 5.0OD1.85ID-2.35H

Thermal Module gaskets APN 875-9290

OMIT CG0400 6.0OD3.9H-SM

OMIT CG0402 6.0OD3.9H-SM

OMIT CG0401 6.0OD3.9H-SM

OMIT CG0403 6.0OD3.9H-SM

APN 860-1328
SH0424 STDOFF-4.5OD1.9H-SM

APN 817-4517
SH0421 4.5OD1.85ID-1.95H-1

APN 806-9391
SH0450 SM
SHLD-MLB-USB-J45

APN 806-6192
SH0452 SM
SHLD-J45-CAN-FENCE1-MDP

APN 806-6194
SH0451 SM
SHLD-J45-CAN-FENCE2-MDP

J45 POGO PINS

APN 870-2451

SH0431 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0432 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0433 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0434 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0435 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0436 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

SH0437 POGO-2.3OD-5.5H-SM-LOW-FORCE SM

J45 STANDOFF

APN 860-1448

SH0440 2.9OD1.2ID-1.35H-SM

SH0441 2.9OD1.2ID-1.35H-SM

SH0444 2.9OD1.2ID-1.35H-SM

SH0460 2.9OD1.2ID-1.35H-SM

SH0461 2.9OD1.2ID-1.35H-SM

SH0442 2.9OD1.2ID-1.35H-SM

SH0443 2.9OD1.2ID-1.35H-SM

SH0462 2.9OD1.2ID-1.35H-SM

SH0465 2.9OD1.2ID-1.35H-SM

SH0466 2.9OD1.2ID-1.35H-SM

SH0467 2.9OD1.2ID-1.35H-SM

PD parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
946-3819	1	D2 MLB DYMAX ADHESIVE SEE-CURE 29993-SC	EDGE_BOND	CRITICAL	

SYNC_MASTER=CLEAN_J45 SYNC_DATE=05/03/2013

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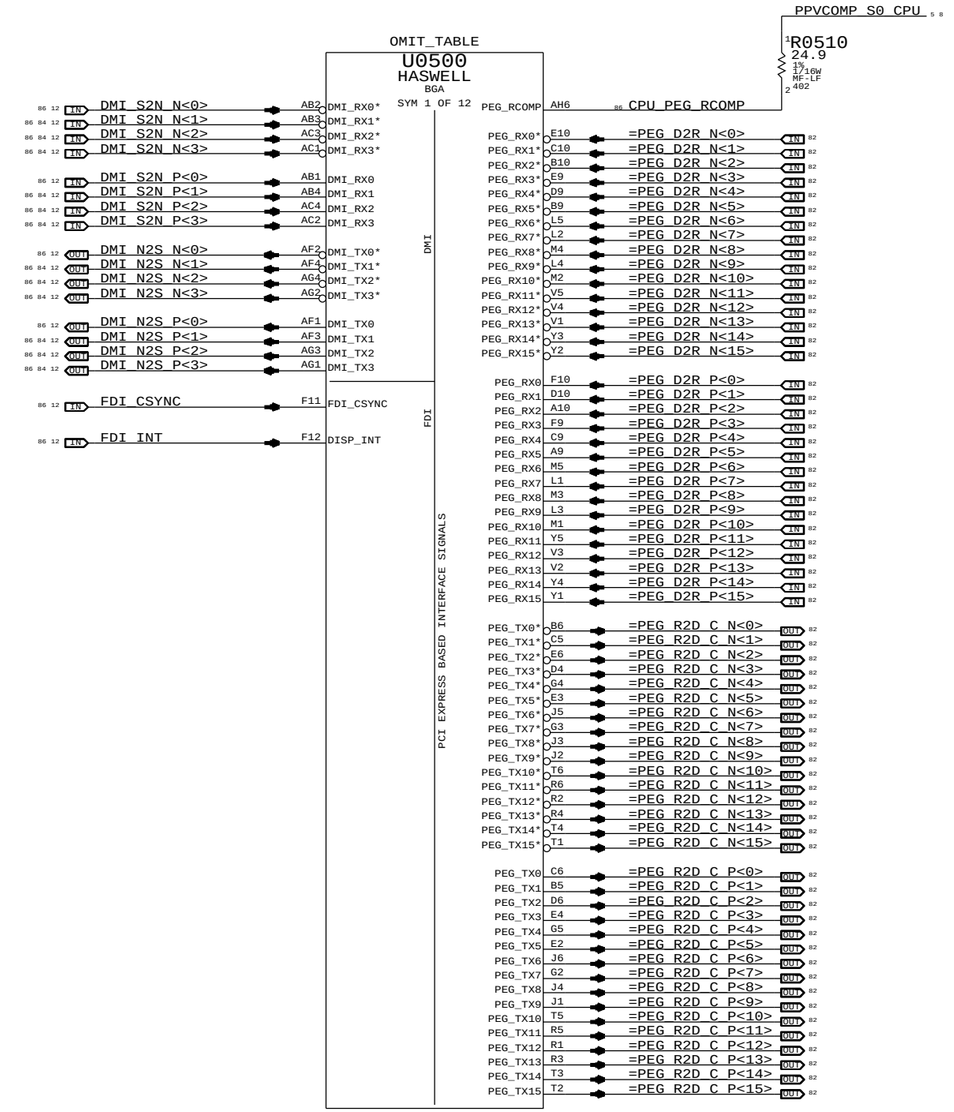

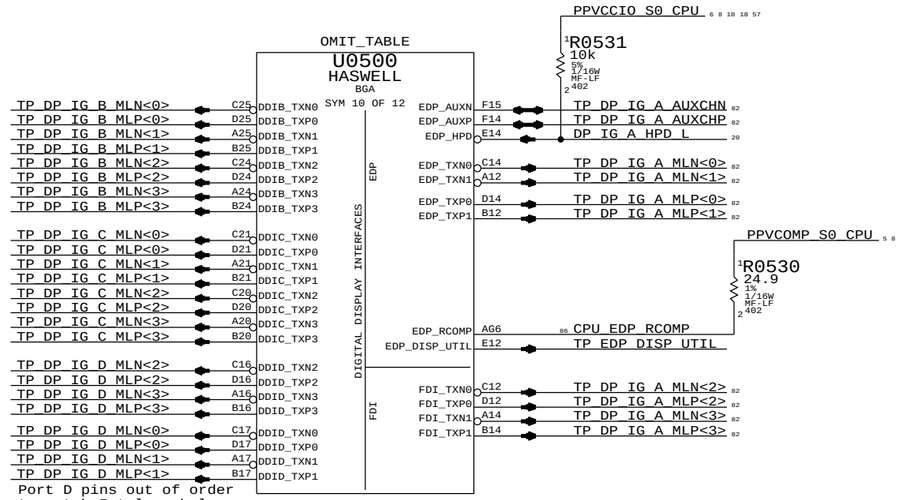

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU DMI/PEG/FDI/RSVD

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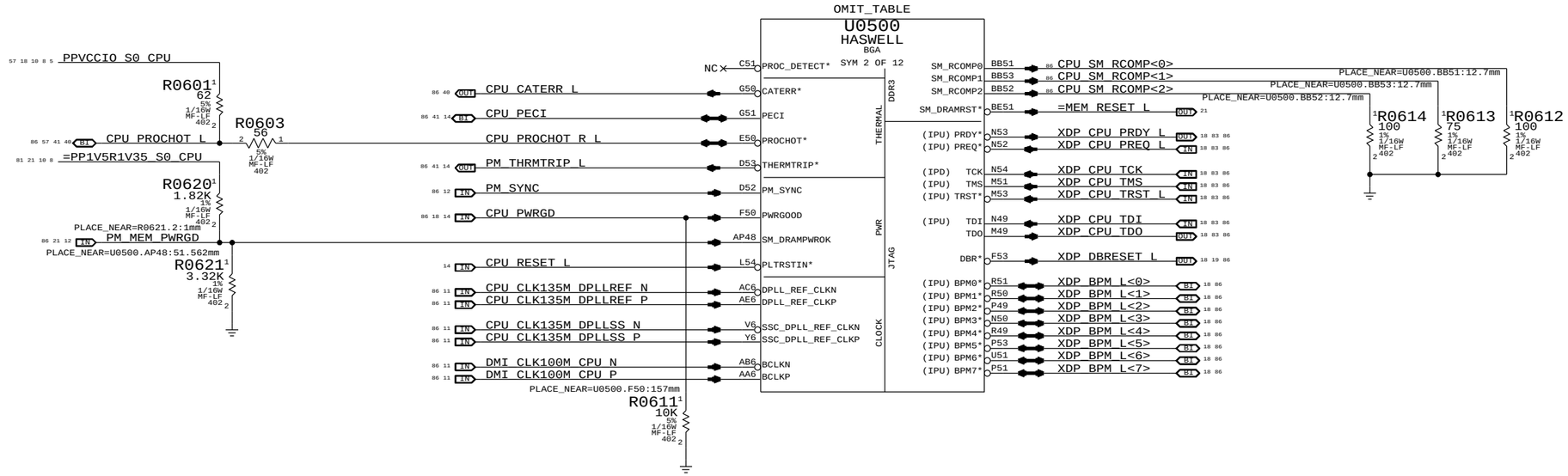
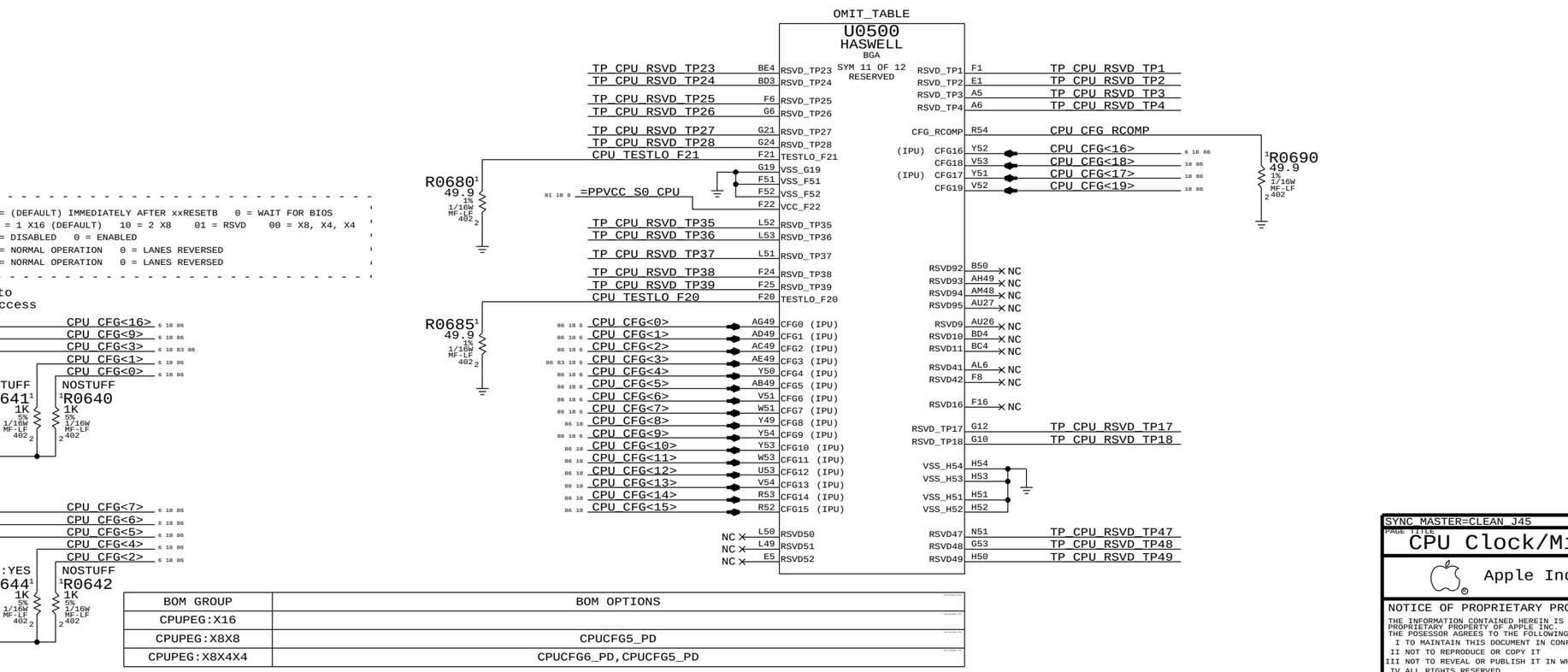
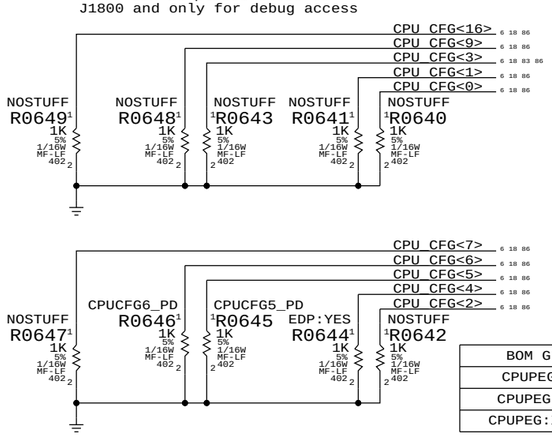




CFG [7] :PEG DEFER TRAINING — 1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB 0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION — 11 = 1 X16 (DEFAULT) 10 = 2 X8 01 = RSVD 00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE — 1 = DISABLED 0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL — 1 = NORMAL OPERATION 0 = LANES REVERSED

These can be placed close to J1800 and only for debug access



BOM GROUP	BOM OPTIONS
CPUPEG:X16	
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU Clock/Misc/JTAG/CFG

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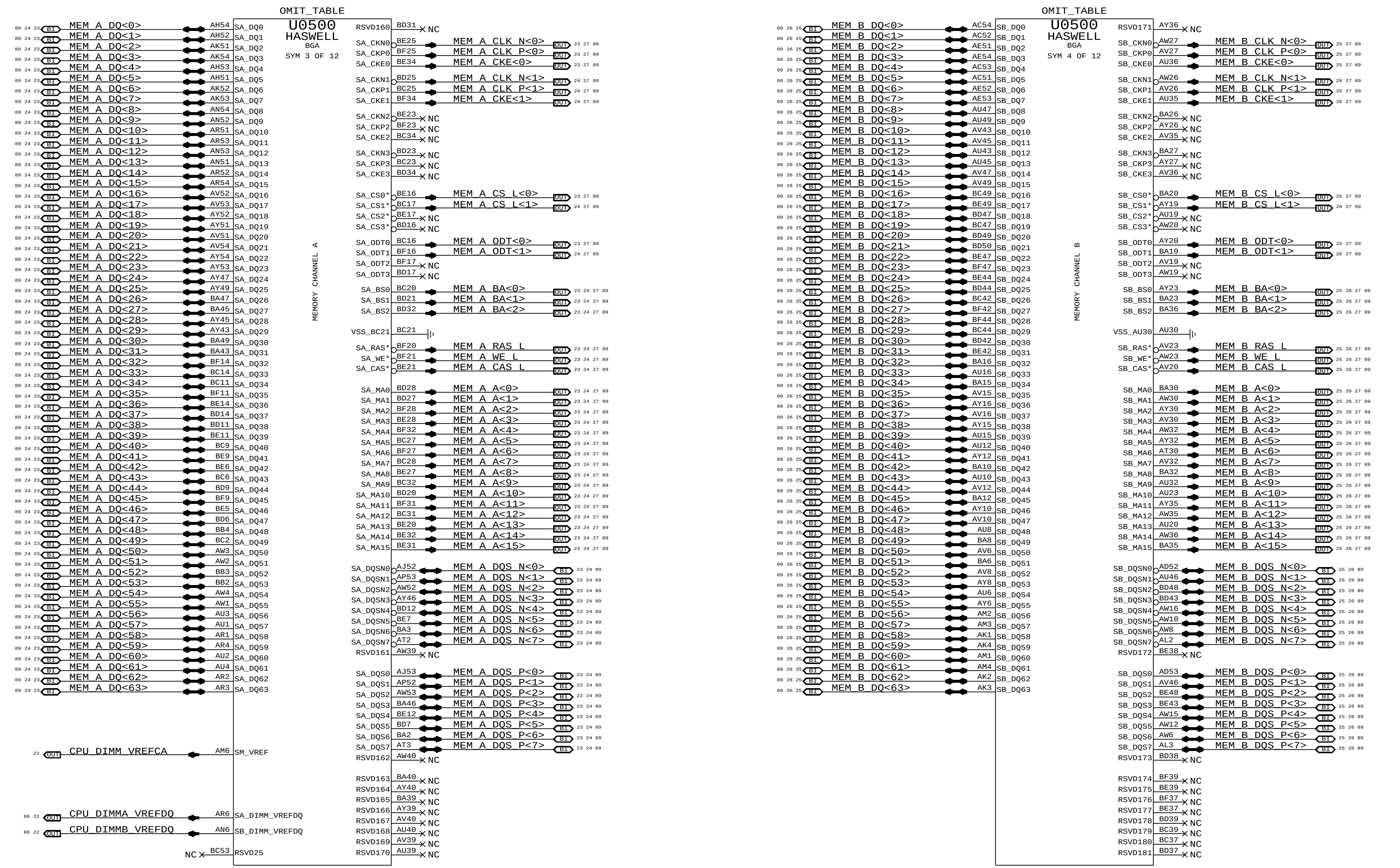

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PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

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NOTE: Aliases not used on CPU supply outputs
to avoid any extraneous connections.

57 18 10 6 5 PPVCCIO_S0_CPU
Max load: 300mA MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

R0800 75 1% 1/10W MF-LF 402
R0802 110 1% 1/16W MF-LF 402
R0810 43 5% 1/16W MF-LF 402
R0811 0 5% 1/16W MF-LF 402
R0812 0 5% 1/16W MF-LF 402

86 57 IN CPU_VIDALERT_L
86 57 OUT CPU_VIDSCLK
86 57 BI CPU_VIDSOUT

R0802.2: PLACE_NEAR=U0500.J50:2.54mm
R0810.2: PLACE_NEAR=U0500.J53:38mm
R0800.2: PLACE_NEAR=R0810.1:2.54mm

81 10 8 6 =PPVCC_S0_CPU
R0860 100 1% 1/10W MF-LF 402
PLACE_NEAR=U0500.C50:50.8mm
PLACE_SIDE=BOTTOM
86 57 OUT CPU_VCCSENSE_P

5 PPVCOMP_S0_CPU
Max load: 300mA MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=1.05V

CPU_VIDALERT_R_L
CPU_VIDSCLK_R
CPU_VIDSOUT_R

18 IN CPU_PWR_DEBUG

TP_CPU_RSVD_TP75
TP_CPU_RSVD_TP76
TP_CPU_IVR_ERROR
TP_CPU_RSVD_TP78

U0500
HASWELL
BGA
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OMIT_TABLE

81 21 10 6 =PP1V5R1V35_S0_CPU

NC J17 RSVD64
NC J21 RSVD65
NC J26 RSVD66
NC J31 RSVD67
AR29
AR31
AR33
AT13
AT19
AT23
AT27
AT32
AT36
AV37
AW22
AW25
AW29
AW33
AY18
BB21
BB22 VDDQ
BB26
BB27
BB30
BB31
BB34
BB36
BD22
BD26
BD30
BD33
BE18
BE22
BE26
BE30
BE33

NC AN31 RSVD68
L6 VCC_L6
M6 VCC_M6
NC AN22 RSVD69
NC AN18 RSVD70
C50 VCC_SENSE
NC AH9 RSVD71
D51 VCCIO_OUT
NC F17 FC_F17
AK6 VCOMP_OUT
NC AN33 RSVD72
NC W9 RSVD73
NC J12 RSVD79(VSS)
NC AR49 RSVD74
J53 VIDALERT*
J52 VIDSCLK
J50 VIDSOUT
B51 VSS_B51
F19 PWR_DEBUG
E52 VSS_E52
V49 RSVD75
U49 RSVD76
AM49 IVR_ERROR
W49 RSVD78
V50 VSS_V50(RSVD)
AN49 VSS_AN49(RSVD)
AJ49 VSS_AJ49(RSVD)
AG50 VSS_AG50(RSVD)
AK49 VSS_AK49(RSVD)
AJ50 VSS_AJ50(RSVD)
AP49 VSS_AP49(RSVD)
AB50 VSS_AB50(RSVD)
AP50 VSS_AP50(RSVD)
AD50 VSS_AD50(RSVD)
AM50 VSS_AM50(RSVD)

A36
A38
A39
A42
A43
A45
A46
A48
AA46
AA47
A8
AA9
VCC

=PPVCC_S0_CPU 6 8 10 81
B43 B45 B46 B48 C27 C28 C31 C32 C34 C36 C38 C39 C42 C43 C45 C46 C48 D27 D28 D31 D32 D34 D36 D38 D39 D42 D43 D45 D46 D48 E27 E28 E31 E32 E34 E36 E38 E39 E42 E43 E45 E46 E48 F27 F28 F31 F32 F34 F36 F38 F39 F42 F43 F45 F46 F48 G27 G29 G31 G32 G34 G36 G38 G39 G42 G43 G45 G46 G48 H11 H12 H13 H14 H16 H17 H18 H19 H20 H21 H23 H24 H25 H26 H27 H29
VCC

Connections would be required
for 2014 CPU support.
FC_D5 D5 TP_CPU_FC_VCCST
FC_D3 D3 TP_CPU_FC_VCCST_PWRGD

OMIT_TABLE
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POWER

H33 H34 H36 H37 H38 H39 H40 H42 H43 H45 H46 H48 H8 H9 J10 J14 J19 J24 J29 J33 J36 J37 J38 J39 J40 J42 J43 J45 J46 J48 J8 J9 K38 K40 K43 K44 K45 K46 K48 K6 K9 L37 L38 L39 L40 L42 L43 L44 L46 L47 L8 M37 M38 M39 M40 M42 M43 M44 M45 M46 M8 M9 N37 N38 N39 N40 N42 N43 N44 N46 N47 N8 N9 P45 P46 P8 R46 R47 R8 R9 T45 T46 U46 U47 U8 U9 V45 V46 V8 W46 W47 W8 Y45 Y46 Y8 A27 A28 A31 A32 A34 B27 B28 B31 B32 B34 B36 B38 B39 B42
VCC

AB45 AB46 AB8 AC46 AC47 AC8 AC9 AD46 AD8 AE46 AE47 AE8 AF8 AG46 AG8 AH46 AH47 AH8 AJ45 AJ46 AK46 AK47 AK8 AL45 AL46 AL8 AL9 AM46 AM47 AM8 AM9 AN10 AN12 AN13 AN14 AN15 AN16 AN17 AN19 AN20 AN21 AN23 AN24 AN25 AN26 AN27 AN29 AN30 AN32 AN34 AN36 AN38 AN39 AN40 AN41 AN42 AN43 AN44 AN45 AN46 AN8 AN9 AP10 AP12 AP13 AP14 AP15 AP16 AP17 AP18 AP19 AP20 AP21 AP22 AP23 AP24 AP25 AP26 AP27 AP29 AP30 AP31 AP32 AP33 AP34 AP35 AP36 AP37 AP38 AP39 AP40 AP41 AP42 AP43 AP44 AP46 AP47 AP8 AP9 AR35 AR37 AR39 AR41 AR43 AR45 AR46 H30 H31 H32
VCC

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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CPU Power

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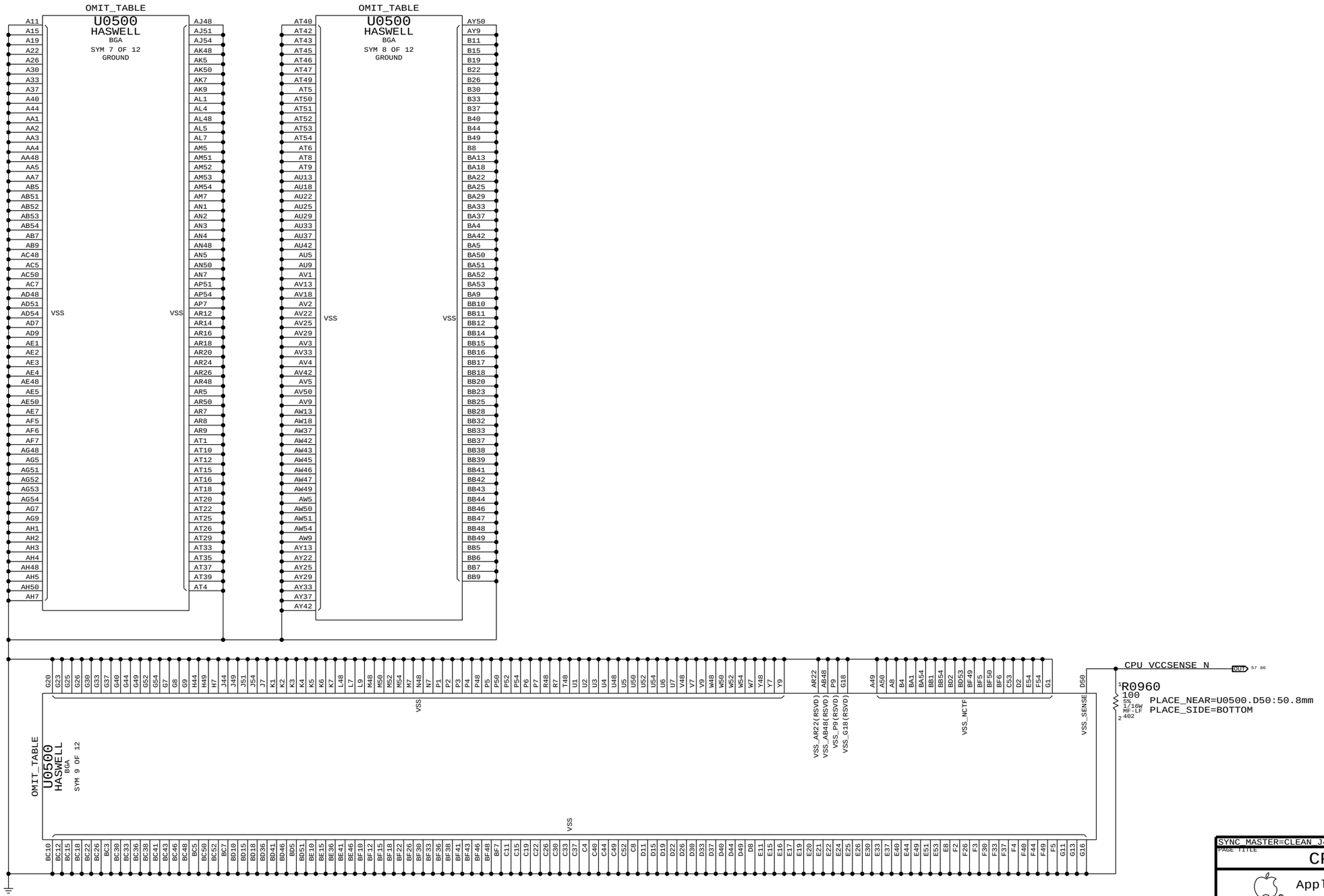

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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CPU Ground

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CPU VCORE Decoupling

Intel recommendation: 4x 470uF 4mOhm (3 CPU-side, 1 opposite), 20x 22uF 0805 (10 CPU-side, 10 opposite near edge, 4x 10uF 0603 (2 CPU-side, 2 opposite), 20x 1uF 0402 (under CPU)
Apple Implementation: 9x 210uF 6mOhm, 44x 10uF 0402, 4x 10uF 0402, 20x 1uF 0402

=PPVCC_S0_CPU

PLACEMENT_NOTE (C1000-C1019):
Place on bottom side of U0500

C1000 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1001 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1002 1UF 10% 10V X6S-CERM 0402 — NO STUFF
C1003 1UF 10% 10V X6S-CERM 0402
C1004 1UF 10% 10V X6S-CERM 0402
C1005 1UF 10% 10V X6S-CERM 0402
C1006 1UF 10% 10V X6S-CERM 0402
C1007 1UF 10% 10V X6S-CERM 0402
C1008 1UF 10% 10V X6S-CERM 0402
C1009 1UF 10% 10V X6S-CERM 0402
C1010 1UF 10% 10V X6S-CERM 0402
C1011 1UF 10% 10V X6S-CERM 0402
C1012 1UF 10% 10V X6S-CERM 0402
C1013 1UF 10% 10V X6S-CERM 0402
C1014 1UF 10% 10V X6S-CERM 0402
C1015 1UF 10% 10V X6S-CERM 0402
C1016 1UF 10% 10V X6S-CERM 0402
C1017 1UF 10% 10V X6S-CERM 0402
C1018 1UF 10% 10V X6S-CERM 0402
C1019 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1020-C1023):
Place near U0500 on bottom side

C1020 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1021 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1022 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
C1023 20UF 20% 4V X5R-CERM 0402-2

CAPS for Acoustic Control (C109A to C102D)

CRITICAL C109A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF, ACAPS:A2
CRITICAL C109B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C109C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C109D 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C109E 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C109F 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C101A 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C101B 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C101C 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C101D 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C101E 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C101F 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C102A 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C102B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C102C 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C102D 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2

PLACEMENT_NOTE (C1024-C1045):
Place near inductors on bottom side.

CRITICAL C1024 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1025 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1026 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1027 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1028 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1029 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1030 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1031 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1032 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1033 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1034 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1035 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1036 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1037 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1038 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1039 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1040 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1041 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1042 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1043 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1044 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1045 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2

PLACEMENT_NOTE (C1046-C1067):
Place near inductors on bottom side.

CRITICAL C1046 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1047 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1048 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1049 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1050 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1051 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1052 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1053 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1054 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1055 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1056 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1057 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C1058 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1059 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1060 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C1061 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1062 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1063 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1064 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1065 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C1066 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A1
CRITICAL C1067 20UF 20% 4V X5R-CERM 0402-2

PLACEMENT_NOTE (C1068-C1076):
Place near inductors on bottom side.

CRITICAL C1068 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1069 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1070 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1071 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1072 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1073 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1074 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1075 210UF 20% 2.5V POLY-TANT CASE-B2S
CRITICAL C1076 210UF 20% 2.5V POLY-TANT CASE-B2S — NO STUFF
CRITICAL C1077 330UF-9MOHM 20% 2.5V POLY-TANT D15T-1 — NO STUFF

CAPS for Acoustic Control (C102E to C103F)

CRITICAL C102E 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C102F 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C103A 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C103B 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C103C 20UF 20% 4V X5R-CERM 0402-2 — NO STUFF
CRITICAL C103D 20UF 20% 4V X5R-CERM 0402-2
CRITICAL C103E 20UF 20% 4V X5R-CERM 0402-2 — ACAPS:A2
CRITICAL C103F 20UF 20% 4V X5R-CERM 0402-2

CPU VDDQ Decoupling

Intel recommendation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402
Apple Implementation: 2x 330uF, 8x 10uF 0603, 10x 1uF 0402

=PP1V5R1V35_S0_CPU

PLACEMENT_NOTE (C1080-C1089):
Place on bottom side of U0500

C1080 1UF 10% 10V X6S-CERM 0402
C1081 1UF 10% 10V X6S-CERM 0402
C1082 1UF 10% 10V X6S-CERM 0402
C1083 1UF 10% 10V X6S-CERM 0402
C1084 1UF 10% 10V X6S-CERM 0402
C1085 1UF 10% 10V X6S-CERM 0402
C1086 1UF 10% 10V X6S-CERM 0402
C1087 1UF 10% 10V X6S-CERM 0402
C1088 1UF 10% 10V X6S-CERM 0402
C1089 1UF 10% 10V X6S-CERM 0402

PLACEMENT_NOTE (C1090-C1097):
Place near U0500 on bottom side

C1090 10UF 20% 4V X6S-CERM 0603
C1091 10UF 20% 4V X6S-CERM 0603
C1092 10UF 20% 4V X6S-CERM 0603
C1093 10UF 20% 4V X6S-CERM 0603
C1094 10UF 20% 4V X6S-CERM 0603
C1095 10UF 20% 4V X6S-CERM 0603
C1096 10UF 20% 4V X6S-CERM 0603
C1097 10UF 20% 4V X6S-CERM 0603

PLACEMENT_NOTE (C1098-C1099):

CRITICAL C1098 330UF-6MOHM 20% 2.5V POLY-TANT D15T-ECGLT-COMBO
CRITICAL C1099 330UF-6MOHM 20% 2.5V POLY-TANT D15T-ECGLT-COMBO
(Z = 1.5mm, place on tall side next to CPU & under heat pipe)

CPU VCCIO Decoupling

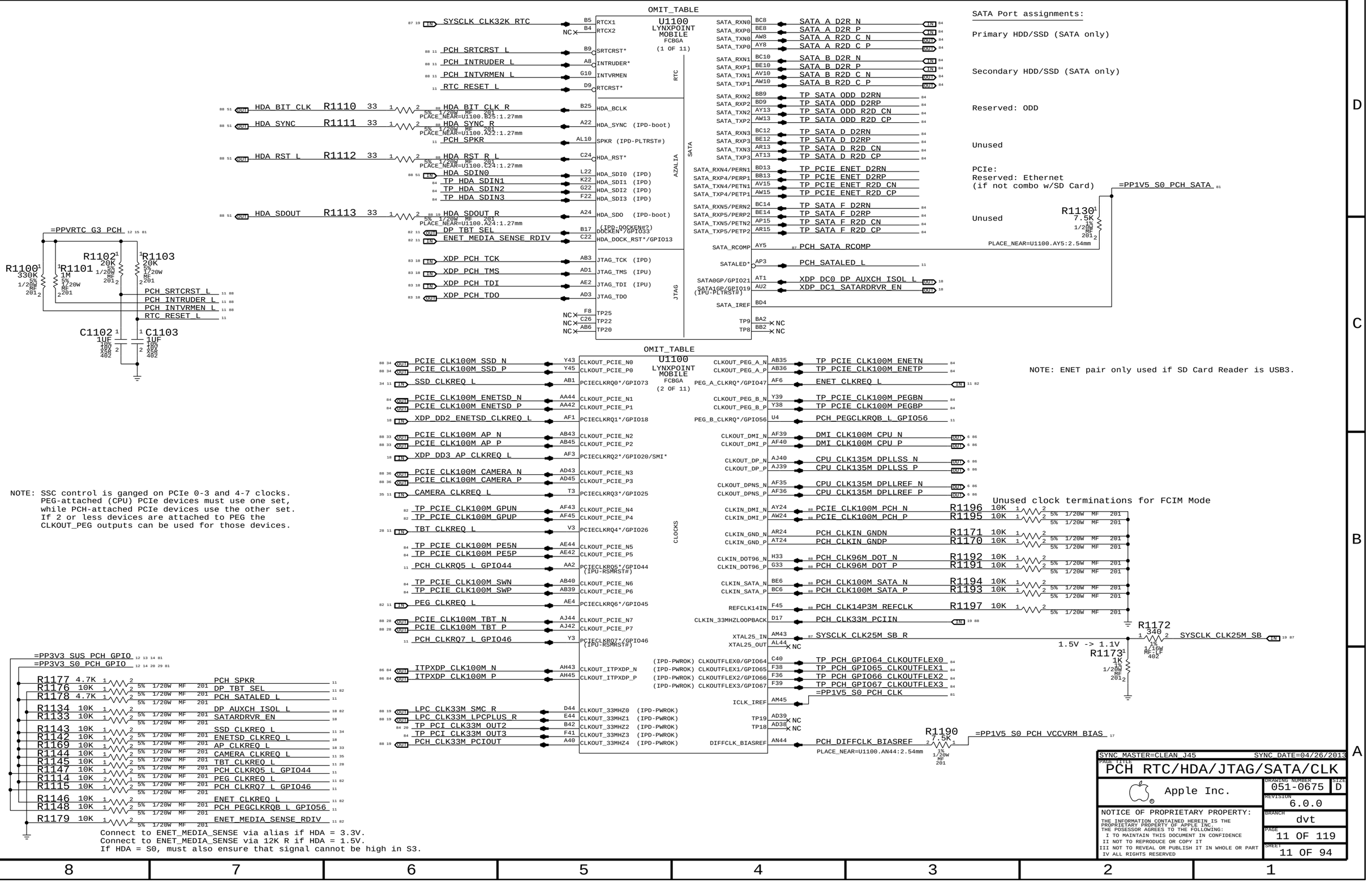
Intel recommendation: 2x 0.01uF 0402 (1 near CPU, 1 near SVID pull-ups)
Apple Implementation: 2x 0.01uF 0402 (second cap is on CPU VR page)

PPVCCIO_S0_CPU

C1079 0.01UF 10% 10V X7R-CERM 0402

NOTE: Intel decoupling recommendations from Shark Bay Mobile Platform Power Delivery Design Guide (doc #487822, Rev 0.8 dated January 2012), Section 5.

SYNC_MASTER=CLEAN_J15 SYNC_DATE=05/02/2013
PAGE TITLE: CPU Decoupling
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 10 OF 119
SHEET: 10 OF 94


OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(1 OF 11)
SYSCLK_CLK32K_RTC
NC
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
HDA_BIT_CLK
HDA_SYNC
HDA_RST_L
HDA_SDOUT
R1110 33
R1111 33
R1112 33
R1113 33
HDA_BIT_CLK_R
HDA_SYNC_R
HDA_RST_R_L
PLACE_NEAR=U1100.B25:1.27mm
PLACE_NEAR=U1100.A22:1.27mm
PLACE_NEAR=U1100.C24:1.27mm
PCH_SPKR
HDA_SDIN0
TP_HDA_SDIN1
TP_HDA_SDIN2
TP_HDA_SDIN3
HDA_SDOUT_R
PLACE_NEAR=U1100.A24:1.27mm
DP_TBT_SEL
ENET_MEDIA_SENSE_RDIV
XDP_PCH_TCK
XDP_PCH_TMS
XDP_PCH_TDI
XDP_PCH_TDO
TP25
TP22
TP20
RTC
AZALIA
JTAG
SATA
SATA_RXN0
SATA_RXP0
SATA_TXN0
SATA_TXP0
SATA_RXN1
SATA_RXP1
SATA_TXN1
SATA_TXP1
SATA_RXN2
SATA_RXP2
SATA_TXN2
SATA_TXP2
SATA_RXN3
SATA_RXP3
SATA_TXN3
SATA_TXP3
SATA_RXN4/PERN1
SATA_RXP4/PERP1
SATA_TXN4/PETN1
SATA_TXP4/PETP1
SATA_RXN5/PERN2
SATA_RXP5/PERP2
SATA_TXN5/PETN2
SATA_TXP5/PETP2
SATA_RCOMP
SATALED*
SATA0GP/GPIO21
SATA1GP/GPIO19 (IPU-PLTRST#)
SATA_IREF
TP9
TP8
SATA A D2R N
SATA A D2R P
SATA A R2D C N
SATA A R2D C P
SATA B D2R N
SATA B D2R P
SATA B R2D C N
SATA B R2D C P
TP SATA ODD D2RN
TP SATA ODD D2RP
TP SATA ODD R2D CN
TP SATA ODD R2D CP
TP SATA D D2RN
TP SATA D D2RP
TP SATA D R2D CN
TP SATA D R2D CP
TP PCIE ENET D2RN
TP PCIE ENET D2RP
TP PCIE ENET R2D CN
TP PCIE ENET R2D CP
TP SATA F D2RN
TP SATA F D2RP
TP SATA F R2D CN
TP SATA F R2D CP
PCH_SATA_RCOMP
PCH_SATALED_L
XDP_DC0_DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN
SATA Port assignments:
Primary HDD/SSD (SATA only)
Secondary HDD/SSD (SATA only)
Reserved: ODD
Unused
PCIe:
Reserved: Ethernet
(if not combo w/SD Card)
Unused
=PP1V5_S0_PCH_SATA
R1130 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AY5:2.54mm
=PPVRTC_G3_PCH
R1100 330K 5% 1/20W MF 201
R1101 1M 5% 1/20W MF 201
R1102 20K 5% 1/20W MF 201
R1103 20K 5% 1/20W MF 201
C1102 1UF 10% 10V X5R 402
C1103 1UF 10% 10V X5R 402
PCH_SRTCRST_L
PCH_INTRUDER_L
PCH_INTVRMEN_L
RTC_RESET_L
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(2 OF 11)
PCIE_CLK100M_SSD_N
PCIE_CLK100M_SSD_P
SSD_CLKREQ_L
PCIE_CLK100M_ENETSD_N
PCIE_CLK100M_ENETSD_P
XDP_DD2_ENETSD_CLKREQ_L
PCIE_CLK100M_AP_N
PCIE_CLK100M_AP_P
XDP_DD3_AP_CLKREQ_L
PCIE_CLK100M_CAMERA_N
PCIE_CLK100M_CAMERA_P
CAMERA_CLKREQ_L
TP_PCIE_CLK100M_GPUN
TP_PCIE_CLK100M_GPUP
TBT_CLKREQ_L
TP_PCIE_CLK100M_PE5N
TP_PCIE_CLK100M_PE5P
PCH_CLKRQ5_L_GPIO44
TP_PCIE_CLK100M_SWN
TP_PCIE_CLK100M_SWP
PEG_CLKREQ_L
PCIE_CLK100M_TBT_N
PCIE_CLK100M_TBT_P
PCH_CLKRQ7_L_GPIO46
ITPXDP_CLK100M_N
ITPXDP_CLK100M_P
LPC_CLK33M_SMC_R
LPC_CLK33M_LPCPLUS_R
TP_PCI_CLK33M_OUT2
TP_PCI_CLK33M_OUT3
PCH_CLK33M_PCIOUT
CLOCKS
CLKOUT_PCIE_N0
CLKOUT_PCIE_P0
PCIECLKRQ0*/GPIO73
CLKOUT_PCIE_N1
CLKOUT_PCIE_P1
PCIECLKRQ1*/GPIO18
CLKOUT_PCIE_N2
CLKOUT_PCIE_P2
PCIECLKRQ2*/GPIO20/SMI*
CLKOUT_PCIE_N3
CLKOUT_PCIE_P3
PCIECLKRQ3*/GPIO25
CLKOUT_PCIE_N4
CLKOUT_PCIE_P4
PCIECLKRQ4*/GPIO26
CLKOUT_PCIE_N5
CLKOUT_PCIE_P5
PCIECLKRQ5*/GPIO44 (IPU-RSMRST#)
CLKOUT_PCIE_N6
CLKOUT_PCIE_P6
PCIECLKRQ6*/GPIO45
CLKOUT_PCIE_N7
CLKOUT_PCIE_P7
PCIECLKRQ7*/GPIO46 (IPU-RSMRST#)
CLKOUT_ITPXDP_N
CLKOUT_ITPXDP_P
CLKOUT_33MHZ0 (IPD-PWROK)
CLKOUT_33MHZ1 (IPD-PWROK)
CLKOUT_33MHZ2 (IPD-PWROK)
CLKOUT_33MHZ3 (IPD-PWROK)
CLKOUT_33MHZ4 (IPD-PWROK)
CLKOUT_PEG_A_N
CLKOUT_PEG_A_P
PEG_A_CLKRQ*/GPIO47
CLKOUT_PEG_B_N
CLKOUT_PEG_B_P
PEG_B_CLKRQ*/GPIO56
CLKOUT_DMI_N
CLKOUT_DMI_P
CLKOUT_DP_N
CLKOUT_DP_P
CLKOUT_DPNS_N
CLKOUT_DPNS_P
CLKIN_DMI_N
CLKIN_DMI_P
CLKIN_GND_N
CLKIN_GND_P
CLKIN_DOT96_N
CLKIN_DOT96_P
CLKIN_SATA_N
CLKIN_SATA_P
REFCLK14IN
CLKIN_33MHZLOOPBACK
XTAL25_IN
XTAL25_OUT
(IPD-PWROK) CLKOUTFLEX0/GPIO64
(IPD-PWROK) CLKOUTFLEX1/GPIO65
(IPD-PWROK) CLKOUTFLEX2/GPIO66
(IPD-PWROK) CLKOUTFLEX3/GPIO67
ICLK_IREF
TP19
TP18
DIFFCLK_BIASREF
TP_PCIE_CLK100M_ENETN
TP_PCIE_CLK100M_ENETP
ENET_CLKREQ_L
TP_PCIE_CLK100M_PEGBN
TP_PCIE_CLK100M_PEGBP
PCH_PEGCLKRQB_L_GPIO56
DMI_CLK100M_CPU_N
DMI_CLK100M_CPU_P
CPU_CLK135M_DPLLSS_N
CPU_CLK135M_DPLLSS_P
CPU_CLK135M_DPLLREF_N
CPU_CLK135M_DPLLREF_P
PCIE_CLK100M_PCH_N
PCIE_CLK100M_PCH_P
PCH_CLKIN_GNDN
PCH_CLKIN_GNDP
PCH_CLK96M_DOT_N
PCH_CLK96M_DOT_P
PCH_CLK100M_SATA_N
PCH_CLK100M_SATA_P
PCH_CLK14P3M_REFCLK
PCH_CLK33M_PCIIN
SYSCLK_CLK25M_SB_R
TP_PCH_GPIO64_CLKOUTFLEX0
TP_PCH_GPIO65_CLKOUTFLEX1
TP_PCH_GPIO66_CLKOUTFLEX2
TP_PCH_GPIO67_CLKOUTFLEX3
=PP1V5_S0_PCH_CLK
PCH_DIFFCLK_BIASREF
PLACE_NEAR=U1100.AN44:2.54mm
R1190 7.5K 1% 1/20W MF 201
=PP1V5_S0_PCH_VCCVRM_BIAS
Unused clock terminations for FCIM Mode
R1196 10K
R1195 10K
R1171 10K
R1170 10K
R1192 10K
R1191 10K
R1194 10K
R1193 10K
R1197 10K
R1172 340 1% 1/16W MF-LF 402
R1173 1K 1% 1/20W MF 201
1.5V -> 1.1V
SYSCLK_CLK25M_SB
NOTE: ENET pair only used if SD Card Reader is USB3.
NOTE: SSC control is ganged on PCIe 0-3 and 4-7 clocks.
PEG-attached (CPU) PCIe devices must use one set,
while PCH-attached PCIe devices use the other set.
If 2 or less devices are attached to PEG the
CLKOUT_PEG outputs can be used for those devices.
=PP3V3_SUS_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1177 4.7K
R1176 10K
R1178 4.7K
R1134 10K
R1133 10K
R1143 10K
R1142 10K
R1169 10K
R1144 10K
R1145 10K
R1147 10K
R1114 10K
R1115 10K
R1146 10K
R1148 10K
R1179 10K
PCH_SPKR
DP_TBT_SEL
PCH_SATALED_L
DP_AUXCH_ISOL_L
SATARDRVR_EN
SSD_CLKREQ_L
ENETSD_CLKREQ_L
AP_CLKREQ_L
CAMERA_CLKREQ_L
TBT_CLKREQ_L
PCH_CLKRQ5_L_GPIO44
PEG_CLKREQ_L
PCH_CLKRQ7_L_GPIO46
ENET_CLKREQ_L
PCH_PEGCLKRQB_L_GPIO56
ENET_MEDIA_SENSE_RDIV
Connect to ENET_MEDIA_SENSE via alias if HDA = 3.3V.
Connect to ENET_MEDIA_SENSE via 12K R if HDA = 1.5V.
If HDA = S0, must also ensure that signal cannot be high in S3.
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
11 OF 119
SHEET
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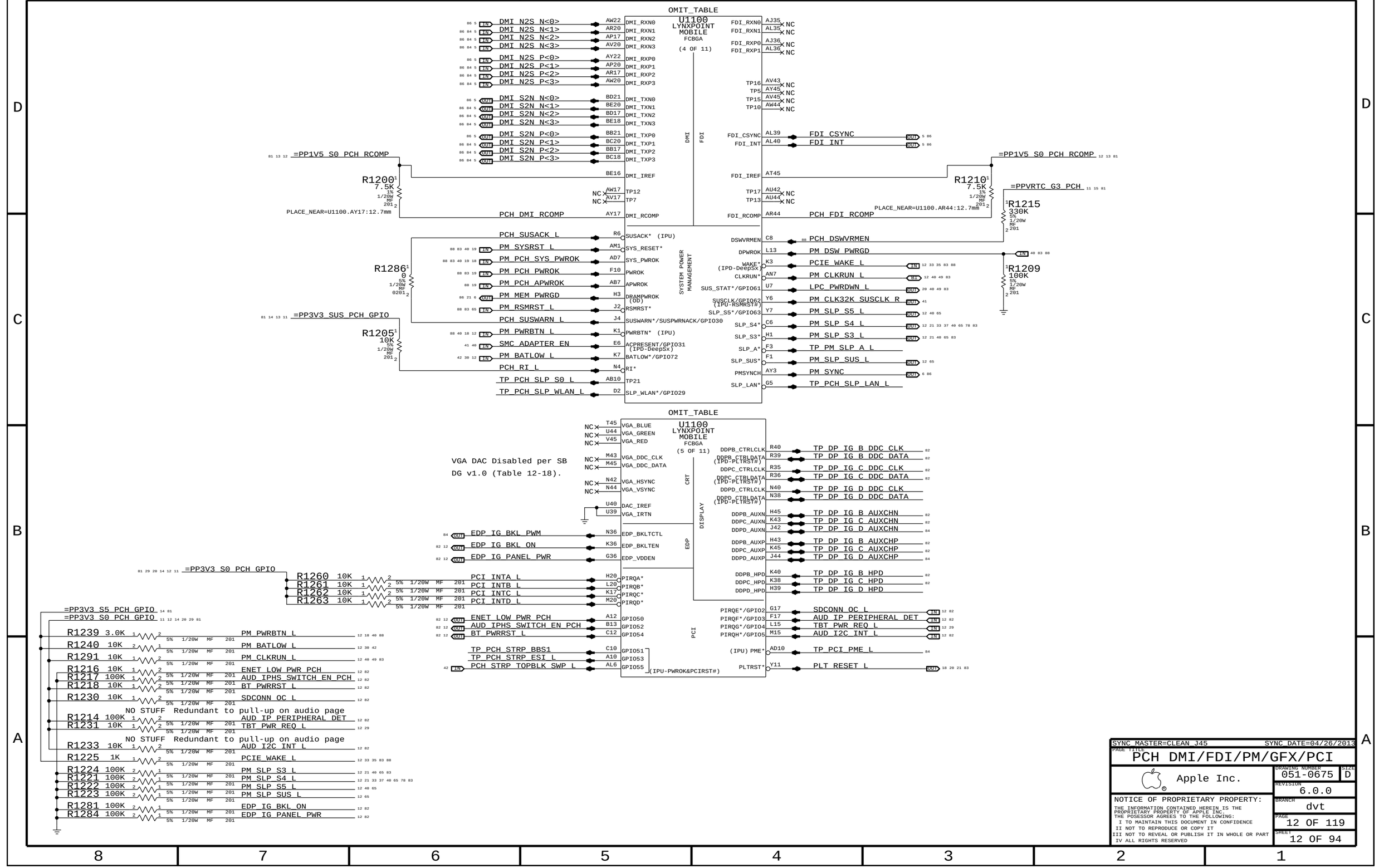
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(4 OF 11)
DMI_RXN0 AW22
DMI_RXN1 AR20
DMI_RXN2 AP17
DMI_RXN3 AV20
DMI_RXP0 AY22
DMI_RXP1 AP20
DMI_RXP2 AR17
DMI_RXP3 AW20
DMI_TXN0 BD21
DMI_TXN1 BE20
DMI_TXN2 BD17
DMI_TXN3 BE18
DMI_TXP0 BB21
DMI_TXP1 BC20
DMI_TXP2 BB17
DMI_TXP3 BC18
DMI_IREF BE16
TP12 AW17
TP7 AV17
DMI_RCOMP AY17
DMI
FDI
FDI_RXN0 AJ35
FDI_RXN1 AL35
FDI_RXP0 AJ36
FDI_RXP1 AL36
TP16 AV43
TP5 AY45
TP15 AV45
TP10 AW44
FDI_CSYNC AL39
FDI_INT AL40
FDI_IREF AT45
TP17 AU42
TP13 AU44
FDI_RCOMP AR44
DMI_N2S_N<0>
DMI_N2S_N<1>
DMI_N2S_N<2>
DMI_N2S_N<3>
DMI_N2S_P<0>
DMI_N2S_P<1>
DMI_N2S_P<2>
DMI_N2S_P<3>
DMI_S2N_N<0>
DMI_S2N_N<1>
DMI_S2N_N<2>
DMI_S2N_N<3>
DMI_S2N_P<0>
DMI_S2N_P<1>
DMI_S2N_P<2>
DMI_S2N_P<3>
FDI_CSYNC
FDI_INT
=PP1V5_S0_PCH_RCOMP
R1200 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AY17:12.7mm
PCH_DMI_RCOMP
R1210 7.5K 1% 1/20W MF 201
PLACE_NEAR=U1100.AR44:12.7mm
PCH_FDI_RCOMP
=PPVRTC_G3_PCH
R1215 330K 5% 1/20W MF 201
SYSTEM POWER MANAGEMENT
PCH_SUSACK_L
PM_SYSRST_L
PM_PCH_SYS_PWROK
PM_PCH_PWROK
PM_PCH_APWROK
PM_MEM_PWRGD
PM_RSMRST_L
PCH_SUSWARN_L
PM_PWRBTN_L
SMC_ADAPTER_EN
PM_BATLOW_L
PCH_RI_L
TP_PCH_SLP_S0_L
TP_PCH_SLP_WLAN_L
SUSACK* (IPU) R6
SYS_RESET* AM1
SYS_PWROK AD7
PWROK F10
APWROK AB7
DRAMPWROK (OD) H3
RSMRST* J2
SUSWARN*/SUSPWRNACK/GPIO30 J4
PWRBTN* (IPU) K1
ACPRESENT/GPIO31 (IPD-DeepSx) E6
BATLOW*/GPIO72 K7
RI* N4
TP21 AB10
SLP_WLAN*/GPIO29 D2
R1286 0 5% 1/20W MF 0201
=PP3V3_SUS_PCH_GPIO
R1205 10K 5% 1/20W MF 201
DSWVRMEN C8
DPWROK L13
WAKE* (IPD-DeepSx) K3
CLKRUN* AN7
SUS_STAT*/GPIO61 U7
SUSCLK/GPIO62 Y6
SLP_S5*/GPIO63 Y7
SLP_S4* C6
SLP_S3* H1
SLP_A* F3
SLP_SUS* F1
PMSYNCH AY3
SLP_LAN* G5
PCH_DSWVRMEN
PM_DSW_PWRGD
PCIE_WAKE_L
PM_CLKRUN_L
LPC_PWRDWN_L
PM_CLK32K_SUSCLK_R
PM_SLP_S5_L
PM_SLP_S4_L
PM_SLP_S3_L
TP_PM_SLP_A_L
PM_SLP_SUS_L
PM_SYNC
TP_PCH_SLP_LAN_L
R1209 100K 5% 1/20W MF 201
OMIT_TABLE
U1100
LYNXPOINT MOBILE
FCBGA
(5 OF 11)
VGA_BLUE T45
VGA_GREEN U44
VGA_RED V45
VGA_DDC_CLK M43
VGA_DDC_DATA M45
VGA_HSYNC N42
VGA_VSYNC N44
DAC_IREF U40
VGA_IRTN U39
VGA DAC Disabled per SB DG v1.0 (Table 12-18).
CRT
DISPLAY
EDP
EDP_BKLTCTL N36
EDP_BKLTEN K36
EDP_VDDEN G36
EDP_IG_BKL_PWM
EDP_IG_BKL_ON
EDP_IG_PANEL_PWR
DDPB_CTRLCLK R40
DDPB_CTRLDATA R39
DDPC_CTRLCLK R35
DDPC_CTRLDATA R36
DDPD_CTRLCLK N40
DDPD_CTRLDATA N38
DDPB_AUXN H45
DDPC_AUXN K43
DDPD_AUXN J42
DDPB_AUXP H43
DDPC_AUXP K45
DDPD_AUXP J44
DDPB_HPD K40
DDPC_HPD K38
DDPD_HPD H39
TP_DP_IG_B_DDC_CLK
TP_DP_IG_B_DDC_DATA
TP_DP_IG_C_DDC_CLK
TP_DP_IG_C_DDC_DATA
TP_DP_IG_D_DDC_CLK
TP_DP_IG_D_DDC_DATA
TP_DP_IG_B_AUXCHN
TP_DP_IG_C_AUXCHN
TP_DP_IG_D_AUXCHN
TP_DP_IG_B_AUXCHP
TP_DP_IG_C_AUXCHP
TP_DP_IG_D_AUXCHP
TP_DP_IG_B_HPD
TP_DP_IG_C_HPD
TP_DP_IG_D_HPD
=PP3V3_S0_PCH_GPIO
R1260 10K 5% 1/20W MF 201
R1261 10K 5% 1/20W MF 201
R1262 10K 5% 1/20W MF 201
R1263 10K 5% 1/20W MF 201
PCI_INTA_L H20
PCI_INTB_L L20
PCI_INTC_L K17
PCI_INTD_L M20
PIRQA*
PIRQB*
PIRQC*
PIRQD*
PCI
ENET_LOW_PWR_PCH A12
AUD_IPHS_SWITCH_EN_PCH B13
BT_PWRRST_L C12
GPIO50
GPIO52
GPIO54
TP_PCH_STRP_BBS1 C10
TP_PCH_STRP_ESI_L A10
PCH_STRP_TOPBLK_SWP_L AL6
GPIO51
GPIO53
GPIO55
(IPU-PWROK&PCIRST#)
PIRQE*/GPIO2 G17
PIRQF*/GPIO3 F17
PIRQG*/GPIO4 L15
PIRQH*/GPIO5 M15
(IPU) PME* AD10
PLTRST* Y11
SDCONN_OC_L
AUD_IP_PERIPHERAL_DET
TBT_PWR_REQ_L
AUD_I2C_INT_L
TP_PCI_PME_L
PLT_RESET_L
=PP3V3_S5_PCH_GPIO
=PP3V3_S0_PCH_GPIO
R1239 3.0K 5% 1/20W MF 201 PM_PWRBTN_L
R1240 10K 5% 1/20W MF 201 PM_BATLOW_L
R1291 10K 5% 1/20W MF 201 PM_CLKRUN_L
R1216 10K 5% 1/20W MF 201 ENET_LOW_PWR_PCH
R1217 100K 5% 1/20W MF 201 AUD_IPHS_SWITCH_EN_PCH
R1218 10K 5% 1/20W MF 201 BT_PWRRST_L
R1230 10K 5% 1/20W MF 201 SDCONN_OC_L
NO STUFF Redundant to pull-up on audio page
R1214 100K 5% 1/20W MF 201 AUD_IP_PERIPHERAL_DET
R1231 10K 5% 1/20W MF 201 TBT_PWR_REQ_L
NO STUFF Redundant to pull-up on audio page
R1233 10K 5% 1/20W MF 201 AUD_I2C_INT_L
R1225 1K 5% 1/20W MF 201 PCIE_WAKE_L
R1224 100K 5% 1/20W MF 201 PM_SLP_S3_L
R1221 100K 5% 1/20W MF 201 PM_SLP_S4_L
R1222 100K 5% 1/20W MF 201 PM_SLP_S5_L
R1223 100K 5% 1/20W MF 201 PM_SLP_SUS_L
R1281 100K 5% 1/20W MF 201 EDP_IG_BKL_ON
R1284 100K 5% 1/20W MF 201 EDP_IG_PANEL_PWR
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
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USB3 Port Assignments:

Unused

PCIe/USB3 Port Assignments:

SD Card Reader
(& Ethernet if combo)

PCIe Port Assignments:

AirPort

Camera

SSD (Gumstick)
Lane 0
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 1
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 2
(PCIe-only)
Or PCIe switch if TBT/SSD

SSD (Gumstick)
Lane 3
(PCIe-only)
Or PCIe switch if TBT/SSD

OMIT_TABLE

U1100
LYNXPOINT MOBILE
FCBGA
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PCI-E | USB

84 TP_USB3_SPARE_D2RN — AW31 PERN1_USB3RN3
84 TP_USB3_SPARE_D2RP — AY31 PERP1_USB3RP3
84 TP_USB3_SPARE_R2D_CN — BE32 PETN1_USB3TN3
84 TP_USB3_SPARE_R2D_CP — BC32 PETP1_USB3TP3

20 IN USB3RPCIE_SD_D2R_N — AT31 PERN2_USB3RN4
20 IN USB3RPCIE_SD_D2R_P — AR31 PERP2_USB3RP4
20 OUT USB3RPCIE_SD_R2D_C_N — BD33 PETN2_USB3TN4
20 OUT USB3RPCIE_SD_R2D_C_P — BB33 PETP2_USB3TP4

88 33 IN PCIE_AP_D2R_N — AW33 PERN3
88 33 IN PCIE_AP_D2R_P — AY33 PERP3
88 33 OUT PCIE_AP_R2D_C_N — BE34 PETN3
88 33 OUT PCIE_AP_R2D_C_P — BC34 PETP3

88 36 IN PCIE_CAMERA_D2R_N — AT33 PERN4
88 36 IN PCIE_CAMERA_D2R_P — AR33 PERP4
88 36 OUT PCIE_CAMERA_R2D_C_N — BE36 PETN4
88 36 OUT PCIE_CAMERA_R2D_C_P — BC36 PETP4

88 34 IN PCIE_SSD_D2R_N<0> — AW36 PERN5
88 34 IN PCIE_SSD_D2R_P<0> — AV36 PERP5
88 34 OUT PCIE_SSD_R2D_C_N<0> — BD37 PETN5
88 34 OUT PCIE_SSD_R2D_C_P<0> — BB37 PETP5

88 34 IN PCIE_SSD_D2R_N<1> — AY38 PERN6
88 34 IN PCIE_SSD_D2R_P<1> — AW38 PERP6
88 34 OUT PCIE_SSD_R2D_C_N<1> — BC38 PETN6
88 34 OUT PCIE_SSD_R2D_C_P<1> — BE38 PETP6

88 34 IN PCIE_SSD_D2R_N<2> — AT40 PERN7
88 34 IN PCIE_SSD_D2R_P<2> — AT39 PERP7
88 34 OUT PCIE_SSD_R2D_C_N<2> — BE40 PETN7
88 34 OUT PCIE_SSD_R2D_C_P<2> — BC40 PETP7

88 34 IN PCIE_SSD_D2R_N<3> — AN38 PERN8
88 34 IN PCIE_SSD_D2R_P<3> — AN39 PERP8
88 34 OUT PCIE_SSD_R2D_C_N<3> — BD42 PETN8
88 34 OUT PCIE_SSD_R2D_C_P<3> — BD41 PETP8

81 12 =PP1V5_S0_PCH_RCOMP
R1300 7.5K 1% 1/20W MF 201 — PLACE_NEAR=U1100.BD29:12.7mm
BE30 PCIE_IREF
NC BC30 TP11
NC BB29 TP6
BD29 PCIE_RCOMP
PCH_PCIE_RCOMP

USB2N0 B37 USB_EXTA_N — B1 37 87
USB2P0 D37 USB_EXTA_P — B1 37 87
USB2N1 A38 USB_EXTC_N — B1 84
USB2P1 C38 USB_EXTC_P — B1 84
USB2N2 A36 TP_USB_SDN — 84
USB2P2 C36 TP_USB_SDP — 84
USB2N3 A34 TP_USB_WLANN — 84
USB2P3 C34 TP_USB_WLANP — 84
USB2N4 B33 TP_USB_4N — 84
USB2P4 D33 TP_USB_4P — 84
USB2N5 F31 TP_USB_PSOCN — 84
USB2P5 G31 TP_USB_PSOCP — 84
USB2N6 K31 TP_USB_6N — 84
USB2P6 L31 TP_USB_6P — 84
USB2N7 G29 TP_USB_7N — 84
USB2P7 H29 TP_USB_7P — 84
USB2N8 A32 USB_EXTB_N — B1 78 83 87
USB2P8 C32 USB_EXTB_P — B1 78 83 87
USB2N9 A30 USB_EXTD_N — B1 84
USB2P9 C30 USB_EXTD_P — B1 84
USB2N10 B29 TP_USB_CAMERAN
USB2P10 D29 TP_USB_CAMERAP
USB2N11 A28 USB_BT_N — B1 33 87
USB2P11 C28 USB_BT_P — B1 33 87
USB2N12 G26 USB_IR_N — B1 84
USB2P12 F26 USB_IR_P — B1 84
USB2N13 F24 USB_TPAD_N — B1 38 87
USB2P13 G24 USB_TPAD_P — B1 38 87
(IPD)

USB3RN1 AR26 USB3_EXTA_D2R_N — IN 37 87
USB3RP1 AP26 USB3_EXTA_D2R_P — IN 37 87
USB3TN1 BE24 USB3_EXTA_R2D_C_N — OUT 37 87
USB3TP1 BD23 USB3_EXTA_R2D_C_P — OUT 37 87
USB3RN2 AW26 USB3_EXTB_D2R_N — IN 78 83 87
USB3RP2 AV26 USB3_EXTB_D2R_P — IN 78 83 87
USB3TN2 BD25 USB3_EXTB_R2D_C_N — OUT 78 87
USB3TP2 BC24 USB3_EXTB_R2D_C_P — OUT 78 87
USB3RN5 AW29 USB3_EXTC_D2R_N — IN 84
USB3RP5 AV29 USB3_EXTC_D2R_P — IN 84
USB3TN5 BE26 USB3_EXTC_R2D_C_N — OUT 84
USB3TP5 BC26 USB3_EXTC_R2D_C_P — OUT 84
USB3RN6 AR29 USB3_EXTD_D2R_N — IN 84
USB3RP6 AP29 USB3_EXTD_D2R_P — IN 84
USB3TN6 BD27 USB3_EXTD_R2D_C_N — OUT 84
USB3TP6 BE28 USB3_EXTD_R2D_C_P — OUT 84

USBRBIAS* K24
USBRBIAS K26
87 PCH_USB_RBIAS
R1370 22.6 1% 1/20W MF 201 — PLACE_NEAR=U1100.K24:11.4mm

TP24 M33 NC
TP23 L33 NC

OC0*/GPIO59 P3 XDP_DA0_USB_EXTA_OC_L — IN 13 18
OC1*/GPIO40 V1 XDP_DA1_USB_EXTC_OC_L — IN 13 18
OC2*/GPIO41 U2 XDP_DA2_SSD_PWR_EN — OUT 18
OC3*/GPIO42 P1 XDP_DA3_CAMERA_PWR_EN — OUT 18
OC4*/GPIO43 M3 XDP_DB0_USB_EXTB_OC_L — IN 13 18
OC5*/GPIO9 T1 XDP_DB1_USB_EXTD_OC_L — IN 13 18
OC6*/GPIO10 N2 XDP_DB2_SD_PWR_EN — OUT 18
OC7*/GPIO14 M1 XDP_DB3_SDCONN_STATE_CHANGE_L — IN 13 18

USB Port Assignments:

Ext A (LS/FS/HS)

Ext C (LS/FS/HS)

Reserved: SD (HS)

Reserved: WiFi (HS)

Unused

Reserved: PSOC (Legacy Trackpad)

Unused

Unused

Ext B (LS/FS/HS)

Ext D (LS/FS/HS)

Reserved: Camera

BT

IR

Trackpad

USB3 Port Assignments:

Ext A (SS)

Ext B (SS)

Ext C (SS)

Ext D (SS)

OMIT_TABLE

U1100
LYNXPOINT MOBILE
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LPC | SMBUS | C-LINK | SPI

88 83 79 49 40 B1 LPC_AD<0> — R1340 33 — LPC_AD_R<0> — A20 LAD0 (IPU)
88 83 79 49 40 B1 LPC_AD<1> — R1341 33 — LPC_AD_R<1> — C20 LAD1 (IPU)
88 83 79 49 40 B1 LPC_AD<2> — R1342 33 — LPC_AD_R<2> — A18 LAD2 (IPU)
88 83 79 49 40 B1 LPC_AD<3> — R1343 33 — LPC_AD_R<3> — C18 LAD3 (IPU)
88 83 79 49 40 OUT LPC_FRAME_L — R1344 33 — LPC_FRAME_R_L — B21 LFRAME*
84 TP_LPC_DREQ0_L — D21 LDRQ0* (IPU)
20 13 OUT TBT_PWR_EN_PCH — G20 LDRQ1*/(GPIO23 (IPU-LDRQ1#?)
83 49 40 13 B1 LPC_SERIRQ — AL11 SERIRQ

88 49 OUT SPI_CLK_R — AJ11 SPI_CLK
88 49 OUT SPI_CS0_R_L — AJ7 SPI_CS0* (IPU)
TP_SPI_CS1_L — AL7 SPI_CS1* (IPU)
TP_SPI_CS2_L — AJ10 SPI_CS2* (IPU)
88 49 B1 SPI_MOSI_R — AH1 SPI_MOSI (IPD)
88 49 B1 SPI_MISO — AH3 SPI_MISO (IPU)
49 13 B1 SPI_IO<2> — AJ4 SPI_IO2 (IPU)
49 13 B1 SPI_IO<3> — AJ2 SPI_IO3 (IPU)

SMBALERT*/GPIO11 N7 PCH_SMBALERT_L — 13
SMBCLK R10 SMBUS_PCH_CLK — OUT 43 83 88
SMBDATA U11 SMBUS_PCH_DATA — B1 43 83 88
SML0ALERT*/GPIO60 N8 PCH_SML0ALERT_L — 13
SML0CLK U8 SML_PCH_0_CLK — OUT 43 88
SML0DATA R7 SML_PCH_0_DATA — B1 43 88
SML1ALERT*/PCHHOT*/GPIO74 H6 PCH_SML1ALERT_L — 13
SML1CLK/GPIO58 K6 SML_PCH_1_CLK — IN 43 88
SML1DATA/GPIO75 N11 SML_PCH_1_DATA — B1 43 88

(IPU/IPD) CL_CLK AF11 TP_CLINK_CLK — 84
(IPU/IPD) CL_DATA AF10 TP_CLINK_DATA — 84
CL_RST* AF7 TP_CLINK_RESET_L — 84

TP1 BA45 NC
TP2 BC45 NC
TP4 BE43 NC
TP3 BE44 NC
TD_IREF AY43 PCH_TD_IREF
R1380 8.2K 1% 1/20W MF 201

=PP3V3_SUS_PCH_GPIO — 11 12 14 81
=PP3V3_SUS_PCH_VCC_SPI — 15 17 81
=PP3V3_S3RS4_PCH_GPIO — 81
=PP3V3_S3RS0_CAMPWREN — 81
=PP3V3_S0_PCH — 81

R1350 10K 5% 1/20W MF 201 — LPC_SERIRQ — 13 40 49 83
R1351 10K 5% 1/20W MF 201 — TBT_PWR_EN_PCH — 13 20
R1360 10K 5% 1/20W MF 201 — XDP_DA0_USB_EXTA_OC_L — 13 18
R1361 10K 5% 1/20W MF 201 — XDP_DA1_USB_EXTC_OC_L — 13 18
R1362 10K 5% 1/20W MF 201 — SSD_PWR_EN — 18 64
R1368 10K 5% 1/20W MF 201 — CAMERA_PWR_EN — 18 35
R1320 10K 5% 1/20W MF 201 — XDP_DB0_USB_EXTB_OC_L — 13 18
R1321 10K 5% 1/20W MF 201 — XDP_DB1_USB_EXTD_OC_L — 13 18
R1367 10K 5% 1/20W MF 201 — SD_PWR_EN — 18 78 83
R1369 10K 5% 1/20W MF 201 — XDP_DB3_SDCONN_STATE_CHANGE_L — 13 18
R1392 1K 5% 1/20W MF 201 — SPI_IO<2> — 13 49
R1393 1K 5% 1/20W MF 201 — SPI_IO<3> — 13 49
R1353 10K 5% 1/20W MF 201 — PCH_SMBALERT_L — 13
R1354 10K 5% 1/20W MF 201 — PCH_SML0ALERT_L — 13
R1355 10K 5% 1/20W MF 201 — PCH_SML1ALERT_L — 13

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Pull-up/down on chipset support page (depends on TBT controller)
Redwood Ridge: TBT_CIO_PLUG_EVENT_L, requires pull-up (S0), no isolation necessary.
Cactus Ridge: TBT_CIO_PLUG_EVENT, requires pull-down & isolation.

OMIT_TABLE

U1100
LYNXPOINT MOBILE
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20 IN	=TBT_CIO_PLUG_EVENT_ISOL	AT8	BMBUSY*/GPIO0
82 14 IN	FW_PME_L	F13	TACH1/GPIO1
82 79 14 IN	DPMUX_UC_IRQ	A14	TACH2/GPIO6
40 14 IN	SMC_RUNTIME_SCI_L	G15	TACH3/GPIO7
18 OUT	XDP_FC0_HDD_PWR_EN	Y1	GPIO8 (IPU-RSMRST#)
82 14 OUT	WOL_EN	K13	LAN_PHY_PWR_CTRL/GPIO12
82 14 OUT	MEM_VDD_SEL_1V5_L	AB11	GPIO15
18 14 IN	XDP_DD0_SSD_PCIE_SEL_L	AN2	SATA4GP/GPIO16 (IPU-BOOT/SATA4GP?)
83 49 14 BI	LPCPLUS_GPIO	C14	TACH0/GPIO17
20 14 OUT	JTAG_TBT_TMS_PCH	BB4	SCLOCK/GPIO22
82 14 BI	TBT_GO2SX_BIDIR	Y10	GPIO24
40 14 IN	SMC_WAKE_SCI_L	R11	GPIO27 (IPU-DeepSx)
21 OUT	ISOLATE_CPU_MEM_L	AD11	GPIO28
20 OUT	TBT_POC_RESET_L	AN6	GPIO34
18 OUT	XDP_FC1_GPU_GOOD	AP1	GPIO35/NMI*
18 OUT	XDP_DC2_ODD_PWR_EN_L	AT3	SATA2GP/GPIO36 (IPD-PLTRST#)
18 OUT	XDP_DC3_JTAG_ISP_TCK	AK1	SATA3GP/GPIO37 (IPD-PLTRST#)
20 14 IN	JTAG_ISP_TDO	AT7	SLOAD/GPIO38
20 14 OUT	JTAG_ISP_TDI	AM3	SDATAOUT0/GPIO39
82 14 OUT	FW_PWR_EN_PCH	AN4	SDATAOUT1/GPIO48
	XDP_DD1_MLB_RAMCFG1	AK3	SATA5GP/GPIO49 (IPD-BOOT/SATA5GP?)
83 49 14 BI	SPIROM_USE_MLB	U12	GPIO57
20	MLB_RAMCFG3	C16	TACH4/GPIO68
20	MLB_RAMCFG2	D13	TACH5/GPIO69
20 IN	SD_SEL_PCIE_L_USB_H	G13	TACH6/GPIO70 (IPU-BOOT?)
20	MLB_RAMCFG0	H15	TACH7/GPIO71 (IPU-BOOT?)

CPU/MISC

TP14	AN10	PCH_A20GATE	14
(IPD) PECI	AY1	PCH_PECI	
RCIN*	AT6	PCH_RCIN_L	14 88
PROCPWRGD	AV3	PCH_PROCPWRGD	
THRMTRIP*	AV1	PM_THRMTRIP_L_R	18 41
PLTRST_PROC*	AU4	CPU_RESET_L	OUT 6
VSS	N10		
	A2		
	A41		
	A43		
	A44		
	B1		
	B2		
	B44		
	B45		
	BA1		
	BC1		
	BD1		
VSS	BD2		
	BD44		
	BD45		
	BE2		
	BE3		
	D1		
	E1		
	E45		
	A4		

GPIO

BE41		
BE5		
C45	VSS	
A5		

=PP1V05_S0_PCH_V_PROC_IO 15 17 81

NO STUFF
R1457 1K 5% 1/16W MF-LF 402

NO STUFF
R1470 43 5% 1/20W MF 201 — CPU_PECI BI 6 41 86
R1440 0 5% 1/20W MF 0201 — CPU_PWRGD OUT 6 18 86
R1456 390 5% 1/20W MF 201 — PM_THRMTRIP_L IN 6 41 86

=PP3V3_S0_PCH_GPIO 81 29 20 14 12 11

RAMCFG0:H	R1475 1	10K 5% 1/20W MF 201 2
RAMCFG1:H	1 R1474	10K 5% 1/20W MF 201 2
RAMCFG2:H	R1473 1	10K 5% 1/20W MF 201 2
RAMCFG3:H	1 R1472	10K 5% 1/20W MF 201 2

18 IN

BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG3:H,RAMCFG2:H,RAMCFG1:H,RAMCFG0:H

Systems with no chip-down memory should pull all 4 RAMCFG GPIOs high.
Systems with chip-down memory should add pull-downs on another page and set straps per software.

=PP3V3_S5_PCH_GPIO 12 81
=PP3V3_SUS_PCH_GPIO 11 12 13 81
=PP3V3_S0_PCH_GPIO 11 12 14 20 29 81

NOTE: GPIO0 pull-up/down on project-specific page

R1485	10K	FW_PME_L	14 82
R1411	20K	DPMUX_UC_IRQ	14 79 82
R1496	10K	SMC_RUNTIME_SCI_L	14 40
R1494	10K	WOL_EN	14 82
R1489	10K	MEM_VDD_SEL_1V5_L	14 82
R1495	100K	XDP_DD0_SSD_PCIE_SEL_L	14 18
R1490	100K	LPCPLUS_GPIO	14 49 83
R1412	10K	JTAG_TBT_TMS_PCH	14 20
R1492	10K	TBT_GO2SX_BIDIR	14 82
R1491	10K	SMC_WAKE_SCI_L	14 40
R1498	10K	ODD_PWR_EN_L	18
R1413	10K	JTAG_ISP_TCK	18 20
R1486	10K	JTAG_ISP_TDO	14 20
R1499	10K	JTAG_ISP_TDI	14 20
R1484	10K	FW_PWR_EN_PCH	14 82
R1493	100K	SPIROM_USE_MLB	14 49 83

NOTE: GPIO70 pull-up/down on project-specific page

R1450	10K	PCH_A20GATE	14
R1455	10K	PCH_RCIN_L	14 88

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PCH GPIO/MISC/NCTF

Apple Inc.

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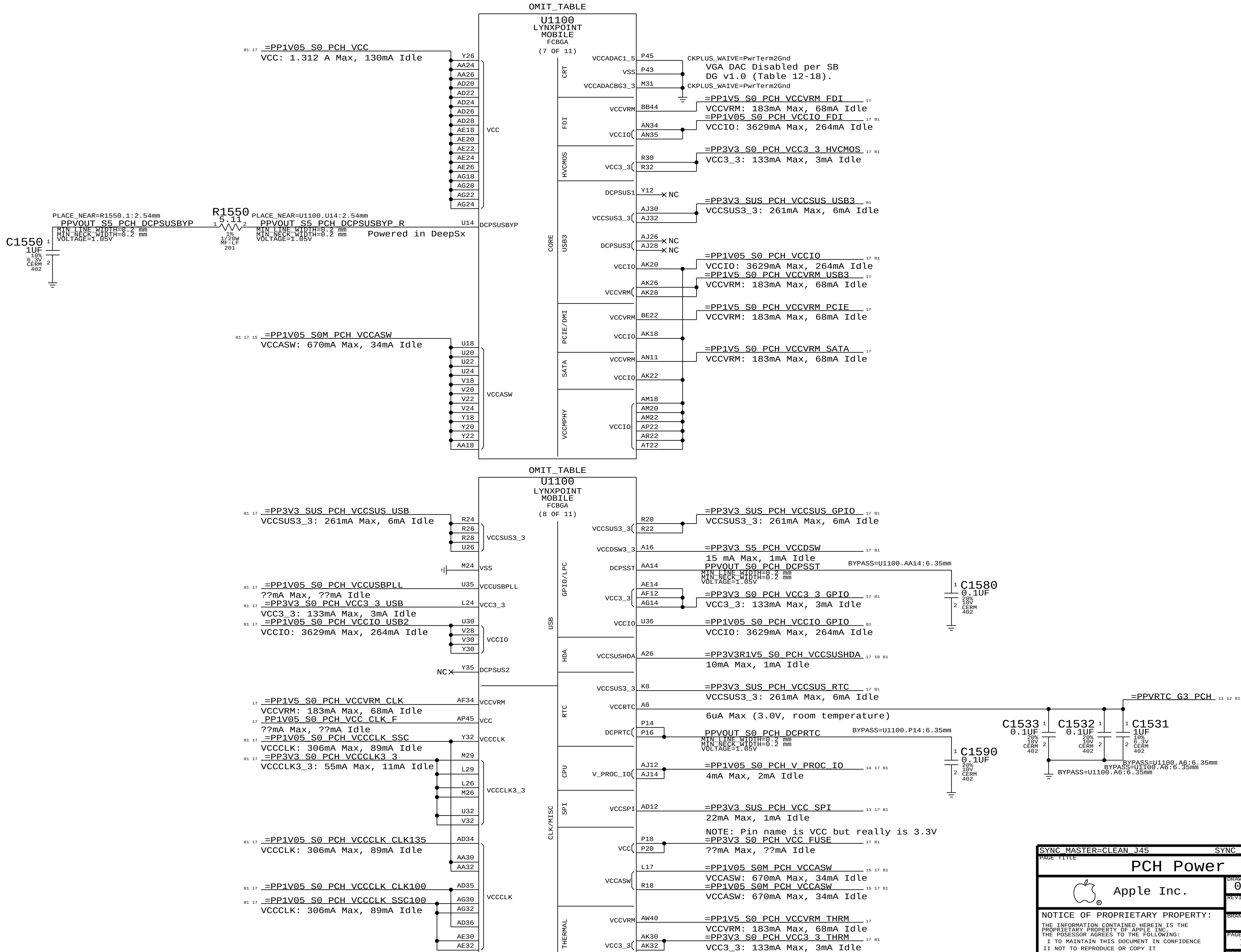

Current data from LPT EDS (doc #486708, Rev 1.0).

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: PCH Power

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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BRANCH: dvt

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U1100
LYNXPOINT
MOBILE
FCBGA
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VSS

AL34			K39
AL38			L2
AL8			L44
AM14			M17
AM24			M22
AM26			N12
AM28			N35
AM30			N39
AM32			N6
AM16			P22
AN36			P24
AN40			P26
AN42			P28
AN8			P30
AP13			P32
AP24			R12
AP31			R14
AP43			R16
AR2			R2
AK16			R34
AT10			R38
AT15			R44
AT17	VSS	VSS	R8
AT20			T43
AT26			U10
AT29			U16
AT36			U28
AT38			U34
D42			U38
AV13			U42
AV22			U6
AV24			V14
AV31			V16
AV33			V26
BB25			V43
AV40			W2
AV6			W44
AW2			Y14
F43			Y16
AY10			Y24
AY15			Y28
AY20			Y34
AY26			Y36
AY29			Y40
AY7			Y8
B11			
B15			

OMIT_TABLE

U1100
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VSS

AA16			B19
AA20			B23
AA22			B27
AA28			B31
AA4			B35
AB12			B39
AB34			B7
AB38			BA40
AB8			BD11
AC2			BD15
AC44			BD19
AD14			AY36
AD16			AT43
AD18			BD31
AD30			BD35
AD32			BD39
AD40			BD7
AD6			D25
AD8			AV7
AE16			F15
AE28			F20
AF38			F29
AF8	VSS	VSS	F33
AG16			BC16
AG2			D4
AG26			G2
AG28			G38
AG44			G44
AJ16			G8
AJ18			H10
AJ20			H13
AJ22			H17
AJ24			H22
AJ34			H24
AJ38			H26
AJ6			H31
AJ8			H36
AK14			H40
AK24			H7
AK43			K10
AK45			K15
AL12			K20
AL2			K29
BC22			K33
BB42			BC28

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PCH Grounds

Apple Inc.

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PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	1	RES,FF,0 OHM,(020OHM MAX),2A,0603	L1790		

Current data from LPT EDS (doc #486708, Rev 1.0).

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PAGE TITLE: PCH DECOUPLING

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Extra BPM Testpoints

XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
XDP_BPM_L<4> → TP1804
XDP_BPM_L<5> → TP1805
XDP_BPM_L<6> → TP1806
XDP_BPM_L<7> → TP1807

(TP-P6)

Merged (CPU/PCH) Micro2-XDP

PPVCCIO_S0_CPU

=PP1V05_S0_CPU_JTAG → R1830 150 5% 1/16W MF-LF 402

CRITICAL
XDP_CONN
J1800
DF40RC-60DP-0.4V
M-ST-SM1
518S0847

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_CPU_PREQ_L	OBSEN_A0	OBSEN_C0	CPU_CFG<17>
XDP_CPU_PRDY_L	OBSEN_A1	OBSEN_C1	CPU_CFG<16>
CPU_CFG<0>	OBSDATA_A0	OBSDATA_C0	CPU_CFG<8>
CPU_CFG<1>	OBSDATA_A1	OBSDATA_C1	CPU_CFG<9>
CPU_CFG<2>	OBSDATA_A2	OBSDATA_C2	CPU_CFG<10>
CPU_CFG<3>	OBSDATA_A3	OBSDATA_C3	CPU_CFG<11>
XDP_BPM_L<0>	OBSEN_B0	OBSEN_D0	CPU_CFG<19>
XDP_BPM_L<1>	OBSEN_B1	OBSEN_D1	CPU_CFG<18>
CPU_CFG<4>	OBSDATA_B0	OBSDATA_D0	CPU_CFG<12>
CPU_CFG<5>	OBSDATA_B1	OBSDATA_D1	CPU_CFG<13>
CPU_CFG<6>	OBSDATA_B2	OBSDATA_D2	CPU_CFG<14>
CPU_CFG<7>	OBSDATA_B3	OBSDATA_D3	CPU_CFG<15>

XDP_CPU_VCCST_PWRGD	PWRGD/HOOK0	ITPCLK/HOOK4	NC
XDP_CPU_PWRBTN_L	HOOK1	ITPCLK#/HOOK5	NC
	VCC_OBS_AB	VCC_OBS_CD	
CPU_PWR_DEBUG	HOOK2	RESET#/HOOK6	XDP_CPURST_L
XDP_SYS_PWROK	HOOK3	DBR#/HOOK7	XDP_DBRESET_L
=SMBUS_XDP_SDA	SDA	TDO	XDP_PCH_TDO
=SMBUS_XDP_SCL	SCL	TRSTn	XDP_TRST_L
XDP_PCH_TCK	TCK1	TDI	XDP_PCH_TDI
	TCK0	TMS	XDP_PCH_TMS
		XDP_PRESENT#	

XDP_CPU_PRESENT_L

CPU_PWRGD → R1800 1K 5% 1/20W MF 201 (PLACE_NEAR=U0500.F50:2.54mm) → XDP
PM_PWRBTN_L → R1802 0 5% 1/20W MF 0201 (PLACE_NEAR=U5000.J3:2.54mm) → XDP
PM_PCH_SYS_PWROK → R1804 0 5% 1/16W MF-LF 402 → XDP
XDP_CPU_TCK

C1804 0.1UF 10% 6.3V CERM-X5R 0201
R1831 1K 5% 1/16W MF-LF 402
C1800 0.1UF 10% 6.3V CERM-X5R 0201
C1801 0.1UF 10% 6.3V CERM-X5R 0201
C1806 0.1UF 10% 6.3V CERM-X5R 0201

R1805 1K 5% 1/20W MF 201 → PLT_RESET_L (PLACE_NEAR=U0500.A67:2.54mm)

NOTE: XDP_DBRESET_L pulled-up to 3.3V on PCH Support Page

CRITICAL
XDP
Q1840
DMN5L06VK-7
SOT-563
→ XDP_CPU_TDO (PLACE_NEAR=J1800.51:28mm)

CRITICAL
XDP
Q1840
DMN5L06VK-7
SOT-563
→ XDP_CPUPCH_TRST_L (MAKE_BASE=TRUE)
→ XDP_CPU_TRST_L (PLACE_NEAR=J1800.53:28mm)

CRITICAL
XDP
Q1842
DMN5L06VK-7
SOT-563
→ XDP_CPU_TDI (PLACE_NEAR=J1800.55:28mm)

CRITICAL
XDP
Q1842
DMN5L06VK-7
SOT-563
→ XDP_CPU_TMS (PLACE_NEAR=J1800.57:28mm)

=PP1V05_S0_CPU_JTAG

XDP_CPU_TDO → R1820 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.M49:28mm) → XDP
XDP_CPU_TCK → R1823 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.N54:28mm) → XDP
XDP_CPU_TRST_L → R1824 51 5% 1/20W MF 201 (PLACE_NEAR=U0500.M53:28mm) → XDP

TDI and TMS are terminated in CPU.

CPU JTAG Isolation

=PP5V_S0_XDPJTAGISOL
=PP3V3_S5_XDPJTAGISOL
C1845 0.1UF 10% 10V X5R-CERM 0201
U1845 74LVC1G07GF SOT891 (VCC, GND, NC, NC, NC)
R1845 330K 5% 1/20W MF 201
ALL_SYS_PWRGD
XDP_JTAG_CPU_ISOL_L

=PP1V05_SUS_PCH_JTAG

XDP_PCH_TDO → R1860 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD3:28mm) → XDP
XDP_PCH_TDI → R1861 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AE2:28mm) → XDP
XDP_PCH_TMS → R1862 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AD1:28mm) → XDP
XDP_PCH_TCK → R1866 51 5% 1/20W MF 201 (PLACE_NEAR=U1100.AB3:28mm) → XDP

PCH/XDP Signals

OMIT (All 10 R's)

				Non-XDP Signals
XDP_DA0_USB_EXTA_OC_L	R1890	SHORT	NONE NONE NONE 201	USB_EXTA_OC_L
XDP_DA2_SSD_PWR_EN	R1895	SHORT	NONE NONE NONE 201	SSD_PWR_EN
XDP_DA3_CAMERA_PWR_EN	R1893	SHORT	NONE NONE NONE 201	CAMERA_PWR_EN
XDP_DB0_USB_EXTB_OC_L	R1894	SHORT	NONE NONE NONE 201	USB_EXTB_OC_L
XDP_DB2_SD_PWR_EN	R1896	SHORT	NONE NONE NONE 201	SD_PWR_EN
XDP_DB3_SDCONN_STATE_CHANGE_L	R1897	SHORT	NONE NONE NONE 201	SDCONN_STATE_CHANGE_L
XDP_DC0_DP_AUXCH_ISOL_L	R1872	SHORT	NONE NONE NONE 201	DP_AUXCH_ISOL_L
XDP_DC1_SATARDRVR_EN		MAKE_BASE=TRUE		SATARDRVR_EN
XDP_DC2_ODD_PWR_EN_L		MAKE_BASE=TRUE		ODD_PWR_EN_L
XDP_DC3_JTAG_ISP_TCK	R1875	SHORT	NONE NONE NONE 201	JTAG_ISP_TCK
XDP_DD0_SSD_PCIE_SEL_L	R1876	SHORT	NONE NONE NONE 201	SSD_PCIE_SEL_L
XDP_DD1_MLB_RAMCFG1		MAKE_BASE=TRUE		MLB_RAMCFG1
XDP_DD2_ENETSD_CLKREQ_L		MAKE_BASE=TRUE		ENETSD_CLKREQ_L
XDP_DD3_AP_CLKREQ_L	R1879	SHORT	NONE NONE NONE 201	AP_CLKREQ_L

PCH/XDP Signal Isolation Notes:

'Output' non-XDP signals require pulls.
'Output' PCH/XDP signals require pulls.

R187x and R189x should be placed where signal path needs to split between route from PCH to J1850 and path to non-XDP signal destination (to minimize stub).

Unused PCH/XDP Signals

XDP_DA1_USB_EXTC_OC_L → TP1810
XDP_DB1_USB_EXTD_OC_L → TP1811
XDP_FC0_HDD_PWR_EN → TP1812
XDP_FC1_GPU_GOOD → TP1813

(TP-P6)

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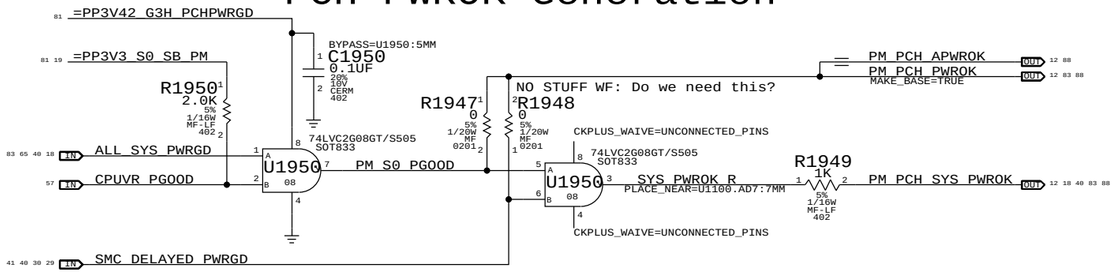
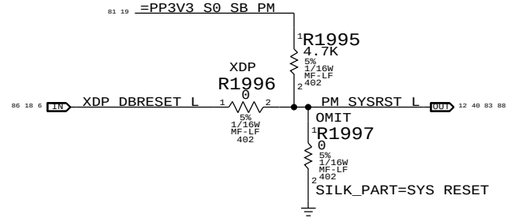
PCH PWROK Generation

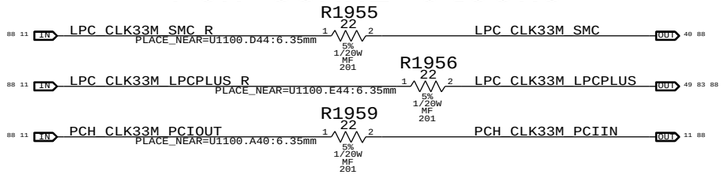


NOTE: ALL_SYS_PWRGD must remain low until at least 5ms after all rails are valid.

PCH Reset Button

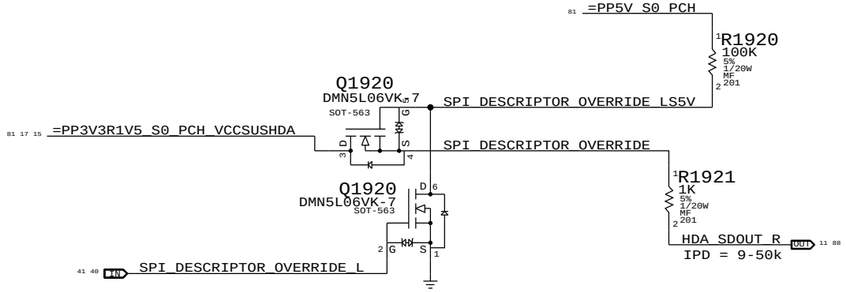


PCH 33MHz Clocks



PCH ME Disable Strap

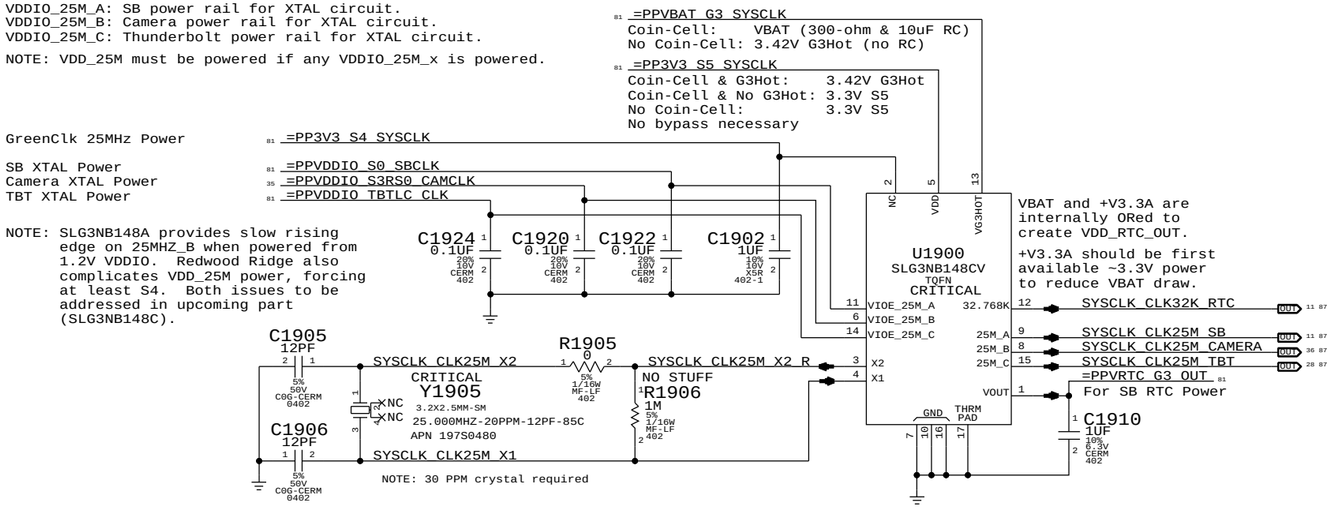
PCH uses HDA_SDO as a power-up strap. If low, ME functions normally. If high, ME is disabled. This allows for full re-flashing of SPI ROM. SMC controls strap enable to allow in-field control of strap setting. Q1920 & 5V pull-up allows circuit to work regardless of HDA voltage.



System RTC Power Source & 32kHz / 25MHz Clock Generator

VDDIO_25M_A: SB power rail for XTAL circuit.
VDDIO_25M_B: Camera power rail for XTAL circuit.
VDDIO_25M_C: Thunderbolt power rail for XTAL circuit.

NOTE: VDD_25M must be powered if any VDDIO_25M_x is powered.



NOTE: SLG3NB148A provides slow rising edge on 25MHZ_B when powered from 1.2V VDDIO. Redwood Ridge also complicates VDD_25M power, forcing at least S4. Both issues to be addressed in upcoming part (SLG3NB148C).

VBAT and +V3.3A are internally ORed to create VDD_RTC_OUT.

+V3.3A should be first available ~3.3V power to reduce VBAT draw.

NOTE: 30 PPM crystal required

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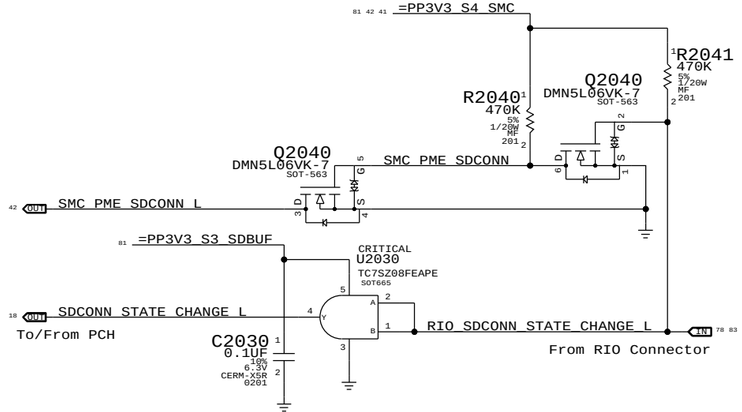
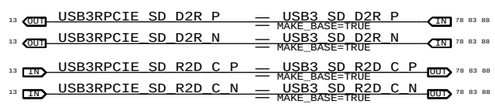
RIO SD Card Reader Support



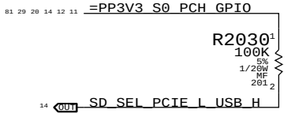
Flexible I/O Aliases

SD Card Reader is always USB3 in this implementaton.



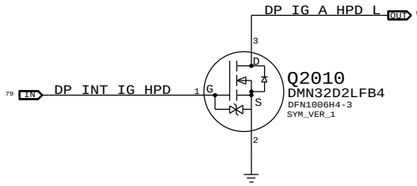
Flexible I/O Configuration Strap

Must pull signal correctly even if always USB or PCIe

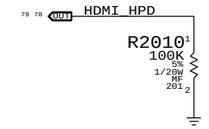


LCD HPD Inverter

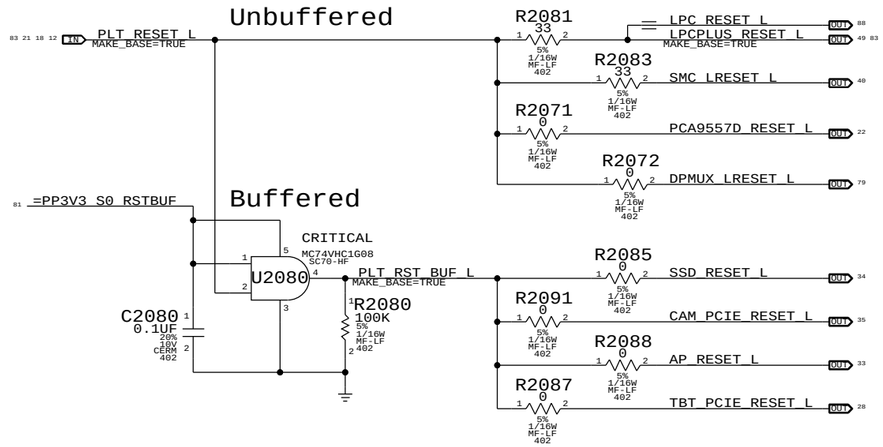
(Pull-Up on CPU Page)



HDMI HPD pull-down

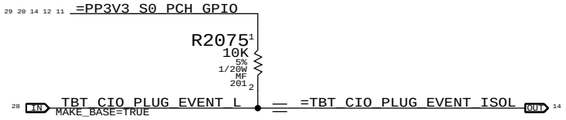


Platform Reset Connections

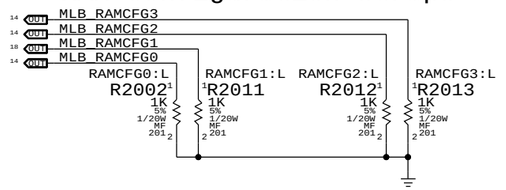


Redwood Ridge Support

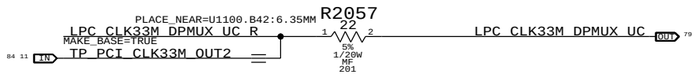
RR output is open-drain, no isolation necessary



RAM Configuration Straps

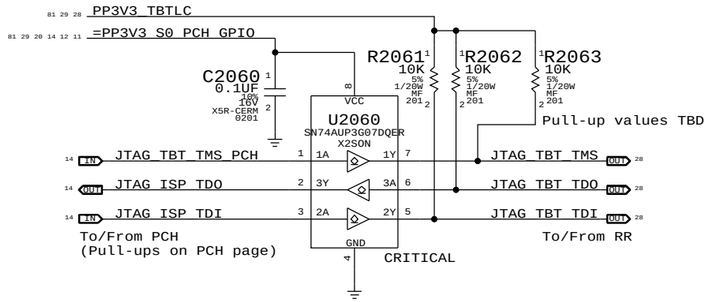


PCH 33MHz Clock for DPMUX

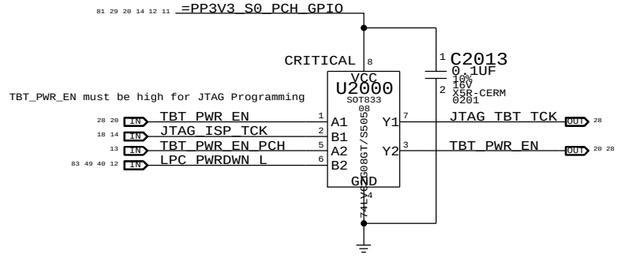


Redwood Ridge JTAG Isolation

TBTLC can be on when S0 is off, and vice-versa
Isolation ensures no leakage to RR or PCH
U2060 supports I/O's powered when VCC=0V

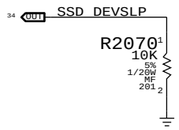


GPIO Glitch Prevention



GS3 Connector Support

DEVSLP not supported on LPT-H



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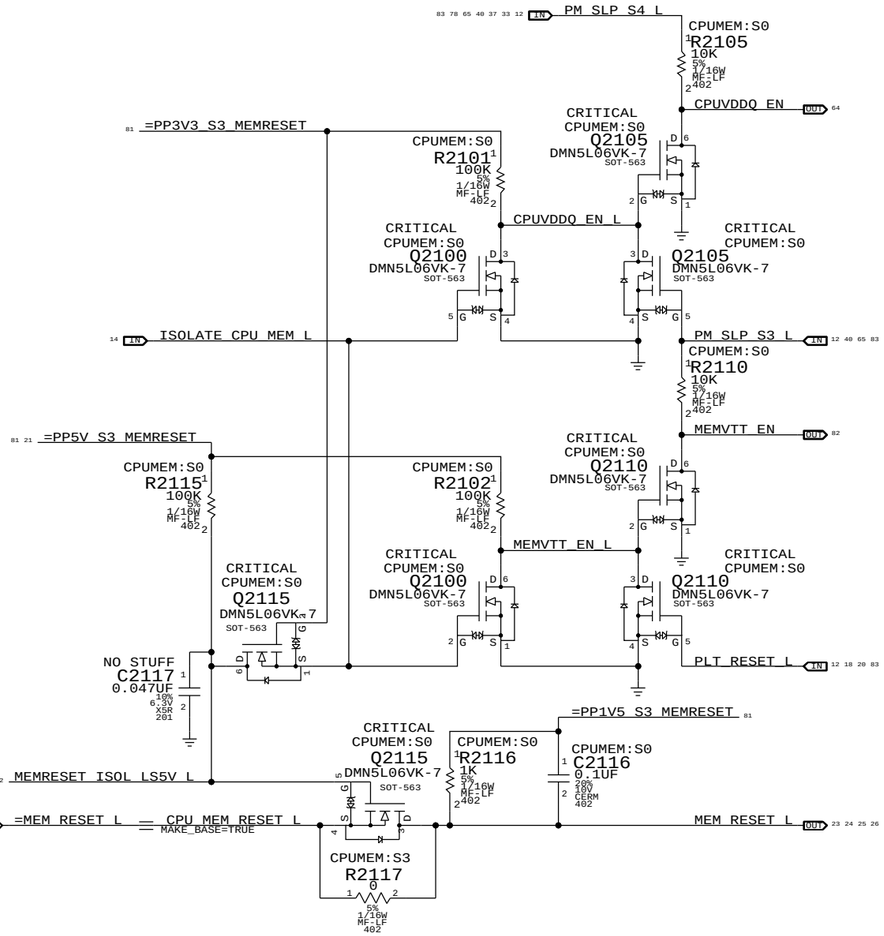
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

CPUVDDQ_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L



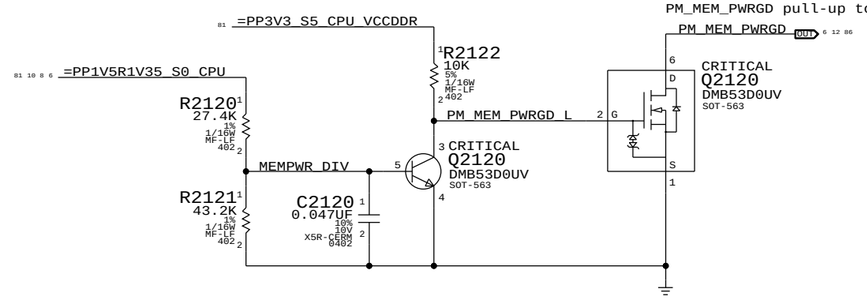
	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	CPUVDDQ_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
to	1	0	1	1	1	1	1	1	1
S3	2	0	0	1	1	1	1	0	1
	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
S0	6	0	1	1	1	1	1	1	1
	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

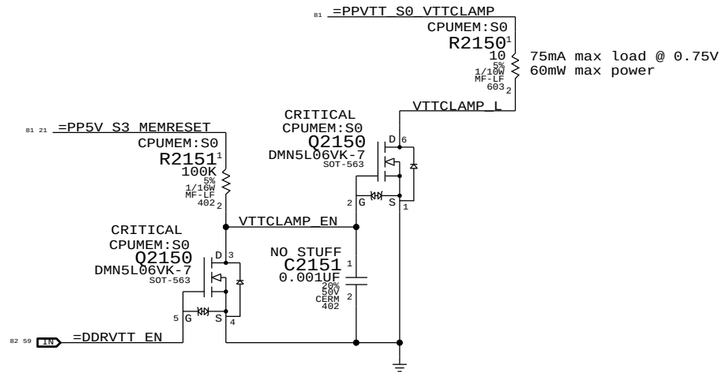
MEM S0 "PGOOD" for CPU

PM_MEM_PWRGD pull-up to CPU VTT rail is on CPU page



MEMVTT Clamp

Ensures CKE signals are held low in S3



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
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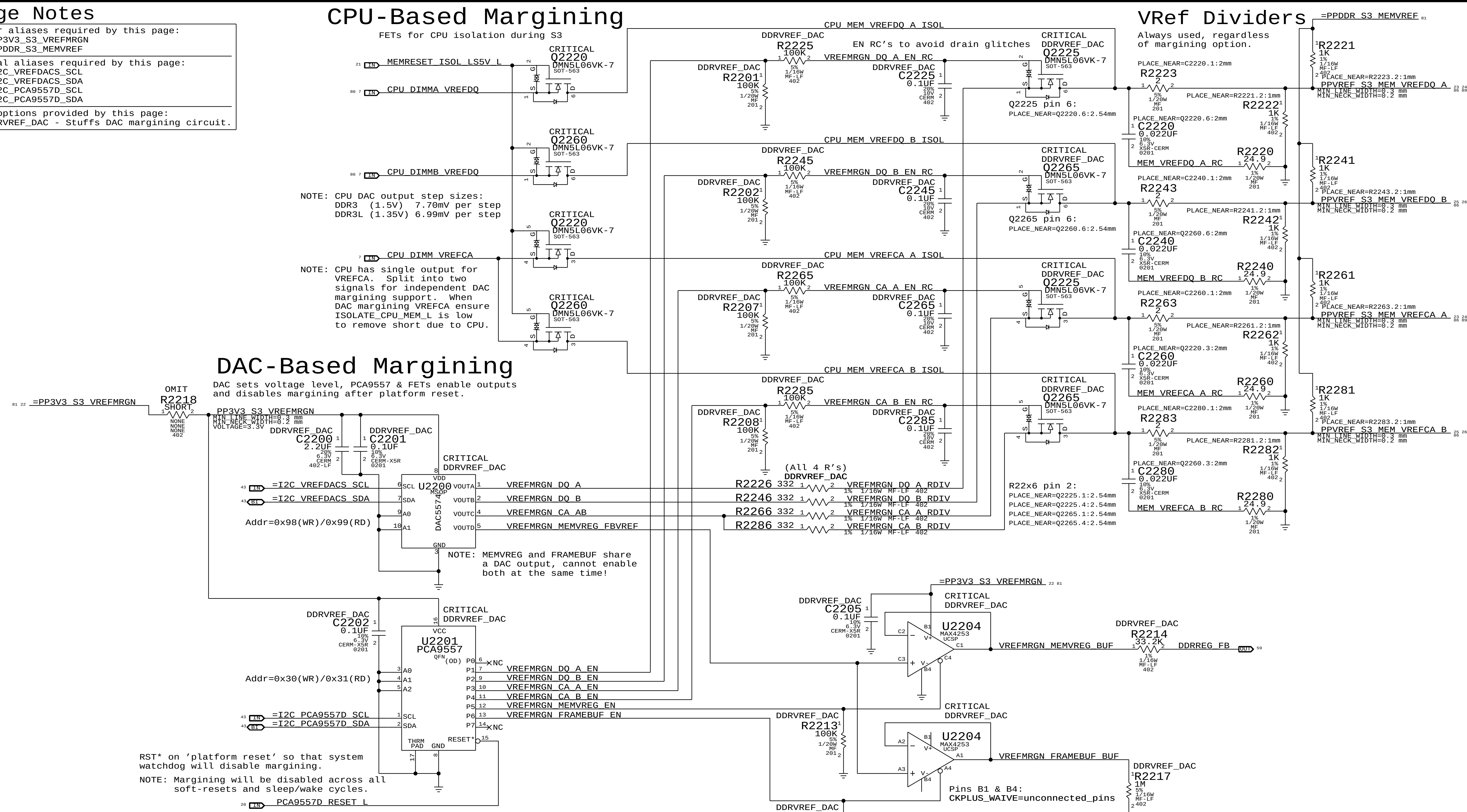
Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPDDR_S3_MEMVREF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
- DDRVREF_DAC - Stuffs DAC margining circuit.



	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	
DAC Channel:	A	B	C	C	D	
PCA9557D Pin:	1	2	3	4	5	
	DDR3 (1.5V)		DDR3L (1.35V)		DDR3 (1.5V)	DDR3L (1.35V)
Nominal value:	0.750V (DAC: 0x3A = 0.747mV)		0.675V (DAC: 0x34 = 0.670mV)		1.500V (DAC: 0x74 = 1.495V)	1.343V (DAC: 0x68 = 1.341V)
Margined target:	0.300V - 1.200V (+/- 450mV)		0.275V - 1.075V (+/- 400mV)		1.200V - 1.800V (+/- 300mV)	0.950V - 1.750V (+/- 400mV)
DAC range:	0.000V - 1.508V (0x00 - 0x75)		0.000V - 1.354V (0x00 - 0x69)		0.000V - 3.004V (0x00 - 0xE9)	0.000V - 2.707V (0x00 - 0xD2)
Margined range:	0.299V - 1.206V (+/- 453mV)		0.269V - 1.083V (+/- 406mV)		1.199V - 1.801V (+/- 301mV)	0.932V - 1.760V (+/- 414mV)
VRef current:	+901uA - -911uA (- = sourced)		+811uA - -816uA (- = sourced)		+36uA - -36uA (- = sourced)	+28uA - -29uA (- = sourced)
DAC step size:	7.68mV / step @ output		7.67mV / step @ output		2.575mV / step @ output	3.923mV / step @ output

NOTE: DDR3 assumes TPS51916 supply with 10.0k/49.9k divider
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

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PAGE TITLE: DDR3 VREF MARGINING

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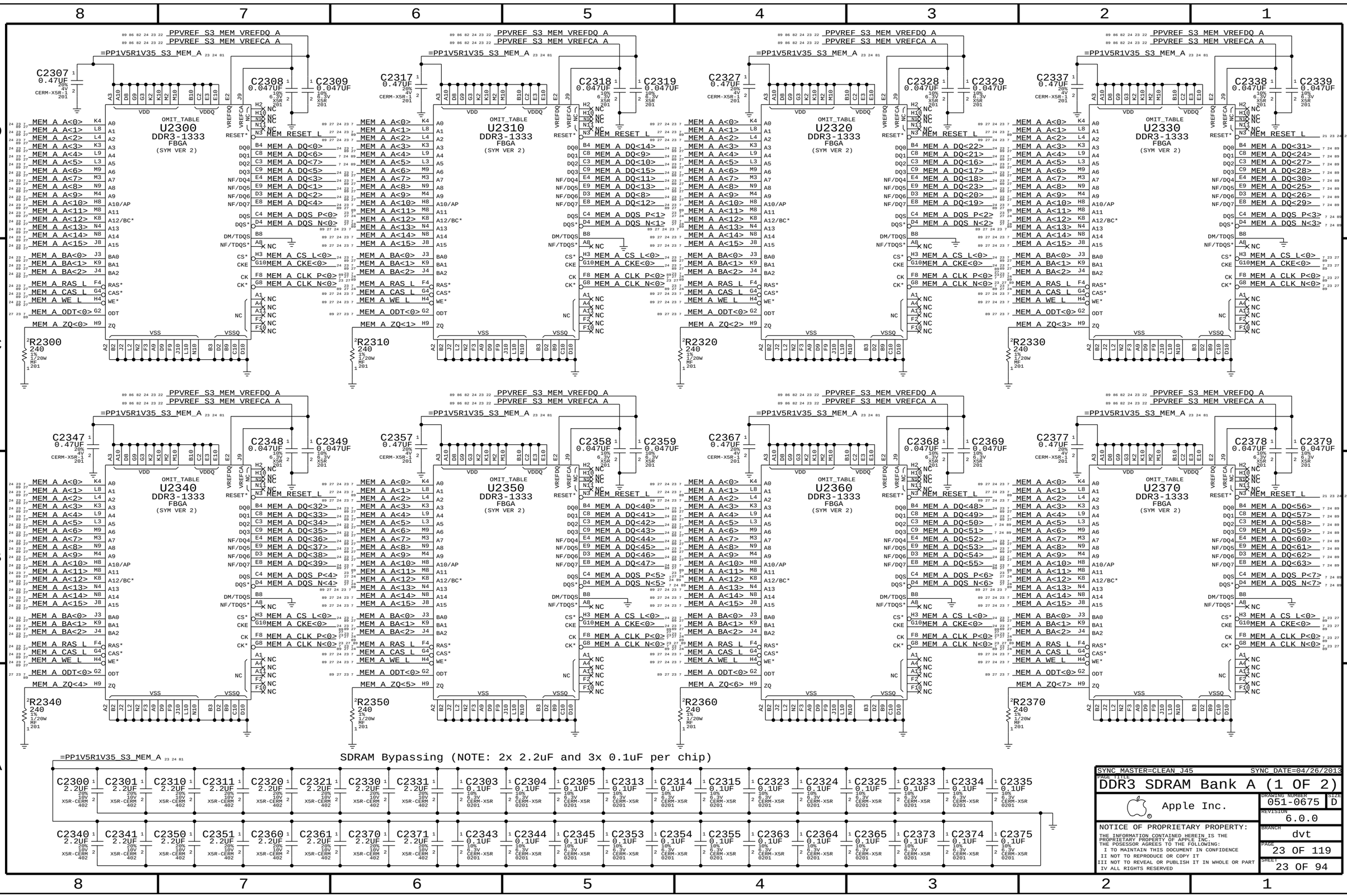
BRANCH: dvt



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
DDR3 SDRAM Bank A (1 OF 2)

Apple Inc.

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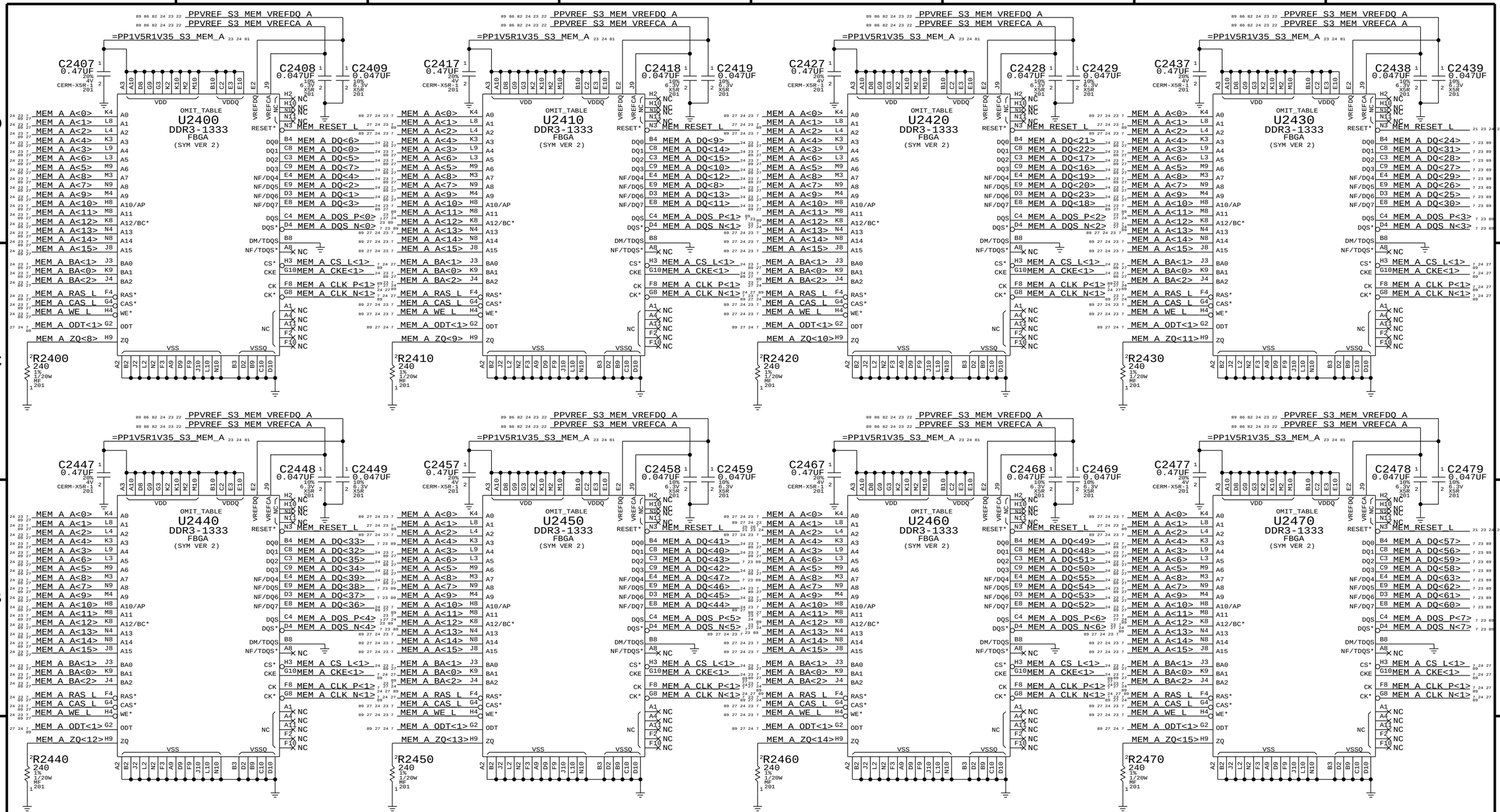

SDRAM Bypassing (NOTE: 2x 2.2uF and 3x 0.1uF per chip)

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: DDR3 SDRAM Bank A (2 OF 2)

Apple Inc.

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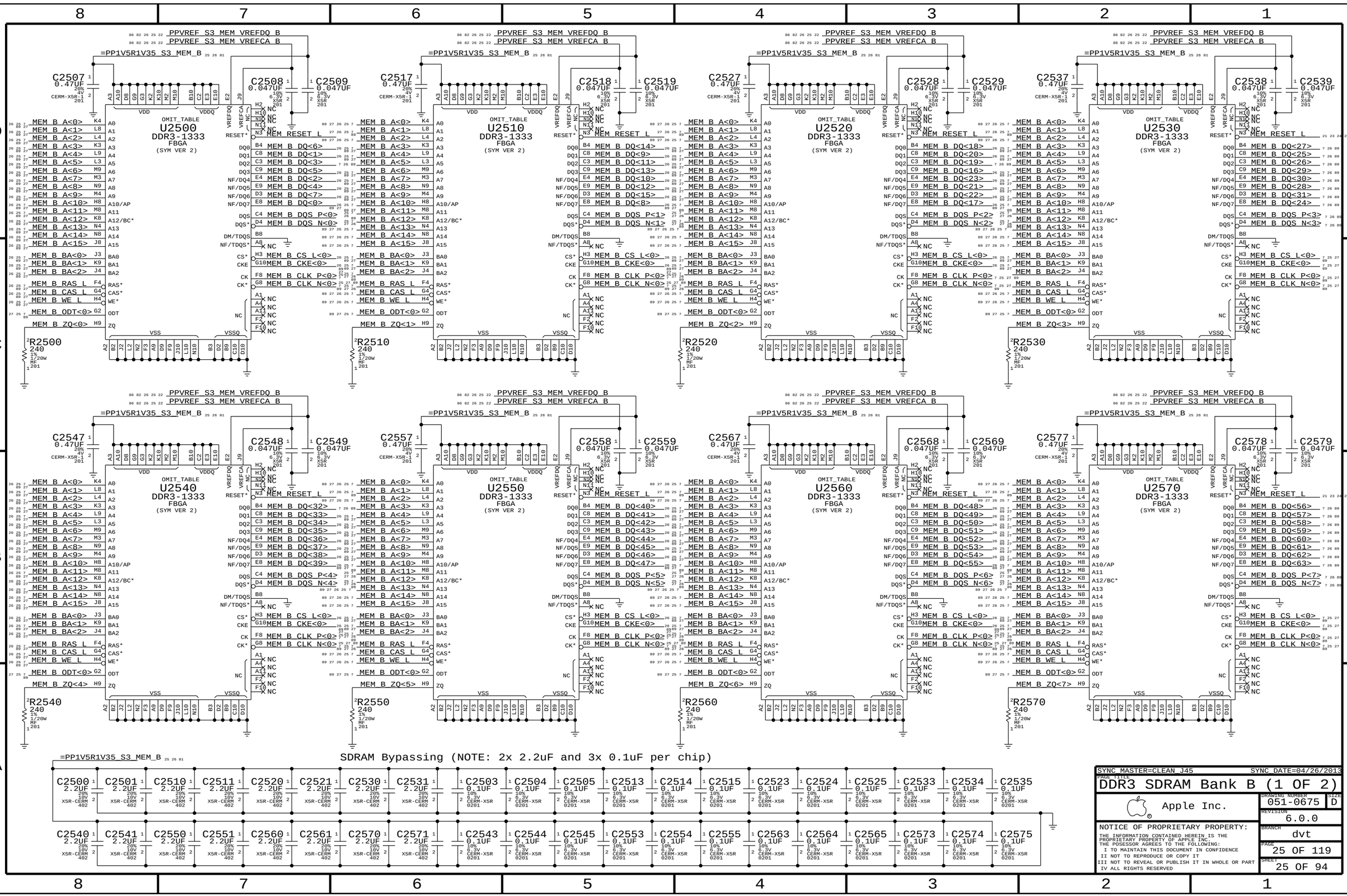

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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DDR3 SDRAM Bank B (1 OF 2)

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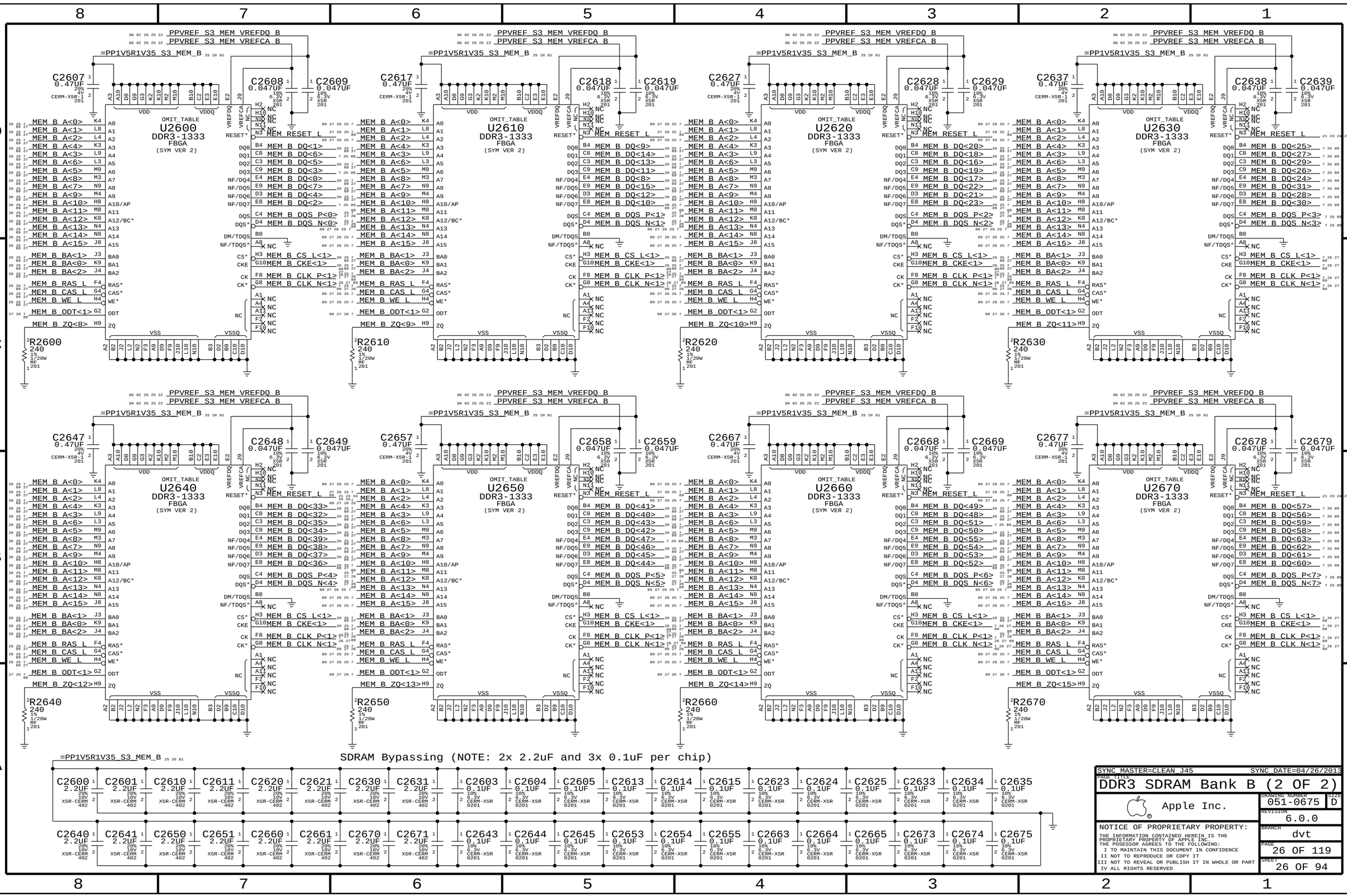

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
DDR3 SDRAM Bank B (2 OF 2)

Apple Inc.

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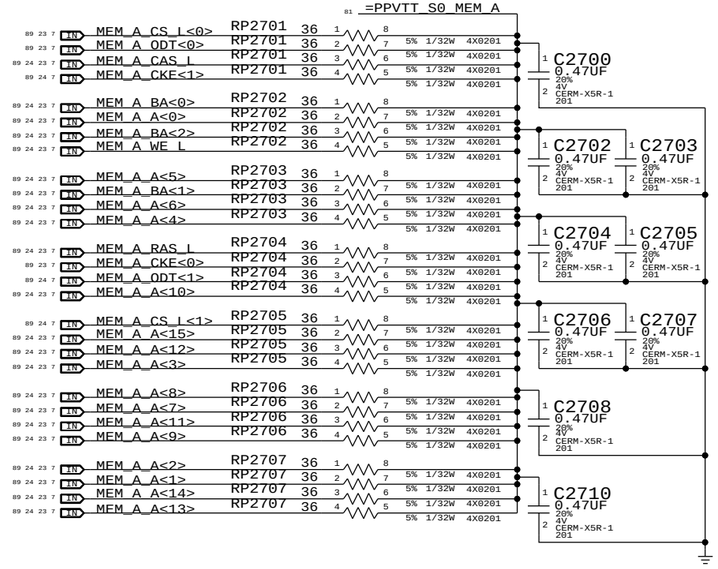
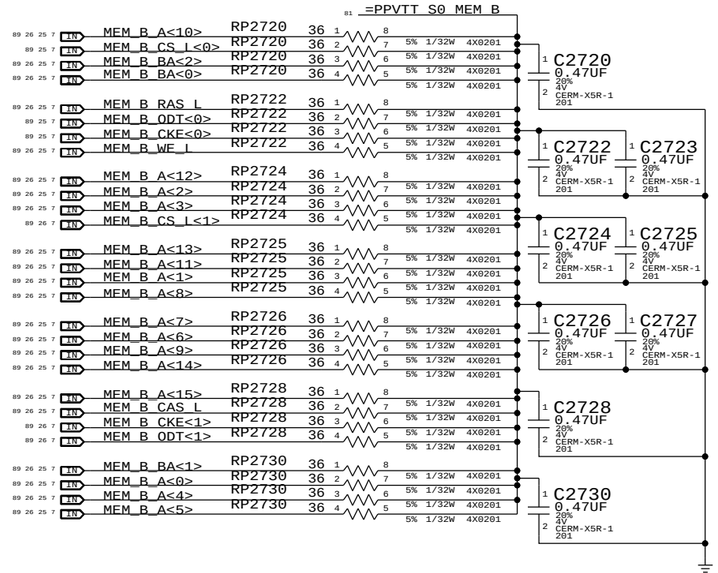
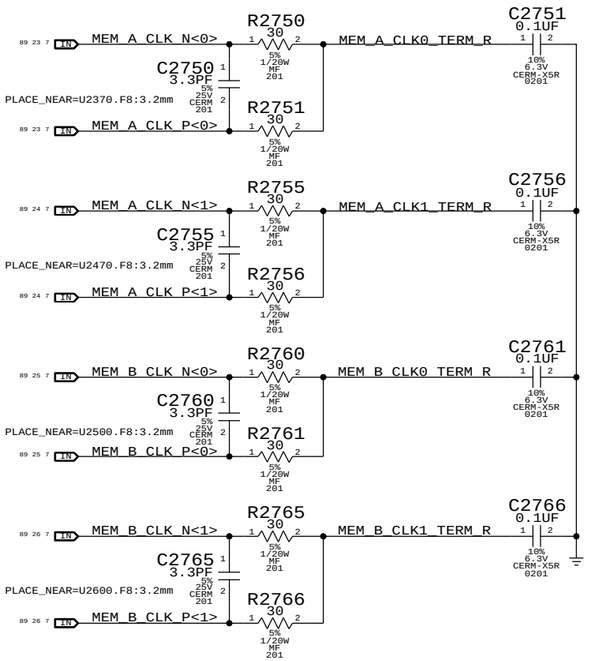
JEDEC 4.20.18 Unbuffered SODIMM Raw Card F spec recommends 36 Ohm term to VTT for CS,CKE,ODT and 36 Ohm for BA,A,RAS,CAS,WE





MEM Clock Termination

Place RC end termination after last DRAM
Place Source Cterm at neckdown at first DRAM



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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DDR3 Termination

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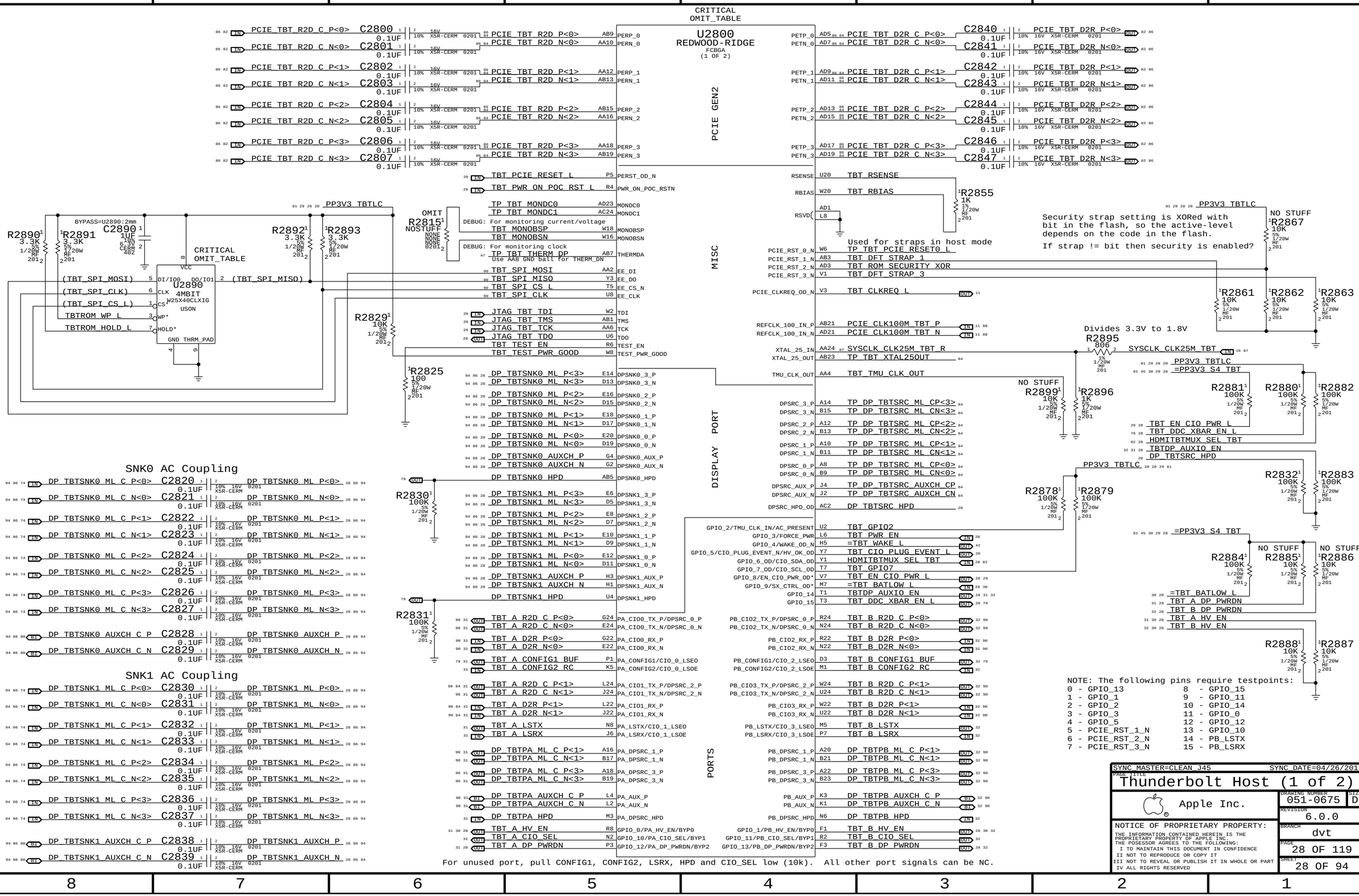
CRITICAL
OMIT_TABLE
U2800
REDWOOD-RIDGE
FCBGA
(1 OF 2)
PCIE GEN2
MISC
DISPLAY PORT
PORTS
PCIE_TBT_R2D_C_P<0>
PCIE_TBT_R2D_C_N<0>
PCIE_TBT_R2D_C_P<1>
PCIE_TBT_R2D_C_N<1>
PCIE_TBT_R2D_C_P<2>
PCIE_TBT_R2D_C_N<2>
PCIE_TBT_R2D_C_P<3>
PCIE_TBT_R2D_C_N<3>
PCIE_TBT_R2D_P<0>
PCIE_TBT_R2D_N<0>
PCIE_TBT_R2D_P<1>
PCIE_TBT_R2D_N<1>
PCIE_TBT_R2D_P<2>
PCIE_TBT_R2D_N<2>
PCIE_TBT_R2D_P<3>
PCIE_TBT_R2D_N<3>
PCIE_TBT_D2R_P<0>
PCIE_TBT_D2R_C_P<0>
PCIE_TBT_D2R_N<0>
PCIE_TBT_D2R_C_N<0>
PCIE_TBT_D2R_P<1>
PCIE_TBT_D2R_C_P<1>
PCIE_TBT_D2R_N<1>
PCIE_TBT_D2R_C_N<1>
PCIE_TBT_D2R_P<2>
PCIE_TBT_D2R_C_P<2>
PCIE_TBT_D2R_N<2>
PCIE_TBT_D2R_C_N<2>
PCIE_TBT_D2R_P<3>
PCIE_TBT_D2R_C_P<3>
PCIE_TBT_D2R_N<3>
PCIE_TBT_D2R_C_N<3>
TBT_PCIE_RESET_L
TBT_PWR_ON_POC_RST_L
TP_TBT_MONDC0
TP_TBT_MONDC1
TBT_MONOBSP
TBT_MONOBSN
TP_TBT_THERM_DP
TBT_SPI_MOSI
TBT_SPI_MISO
TBT_SPI_CS_L
TBT_SPI_CLK
JTAG_TBT_TDI
JTAG_TBT_TMS
JTAG_TBT_TCK
JTAG_TBT_TDO
TBT_TEST_EN
TBT_TEST_PWR_GOOD
TBT_RSENSE
TBT_RBIAS
TP_TBT_PCIE_RESET0_L
TBT_DFT_STRAP_1
TBT_ROM_SECURITY_XOR
TBT_DFT_STRAP_3
TBT_CLKREQ_L
PCIE_CLK100M_TBT_P
PCIE_CLK100M_TBT_N
SYSCLK_CLK25M_TBT_R
TP_TBT_XTAL25OUT
TBT_TMU_CLK_OUT
TP_DP_TBTSRC_ML_CP<3>
TP_DP_TBTSRC_ML_CN<3>
TP_DP_TBTSRC_ML_CP<2>
TP_DP_TBTSRC_ML_CN<2>
TP_DP_TBTSRC_ML_CP<1>
TP_DP_TBTSRC_ML_CN<1>
TP_DP_TBTSRC_ML_CP<0>
TP_DP_TBTSRC_ML_CN<0>
TP_DP_TBTSRC_AUXCH_CP
TP_DP_TBTSRC_AUXCH_CN
DP_TBTSRC_HPD
TBT_GPIO2
TBT_PWR_EN
=TBT_WAKE_L
TBT_CIO_PLUG_EVENT_L
HDMITBTMUX_SEL_TBT
TBT_GPIO7
TBT_EN_CIO_PWR_L
=TBT_BATLOW_L
TBTDP_AUXIO_EN
TBT_DDC_XBAR_EN_L
TBT_A_R2D_C_P<0>
TBT_A_R2D_C_N<0>
TBT_A_D2R_P<0>
TBT_A_D2R_N<0>
TBT_A_CONFIG1_BUF
TBT_A_CONFIG2_RC
TBT_A_R2D_C_P<1>
TBT_A_R2D_C_N<1>
TBT_A_D2R_P<1>
TBT_A_D2R_N<1>
TBT_A_LSTX
TBT_A_LSRX
TBT_B_R2D_C_P<0>
TBT_B_R2D_C_N<0>
TBT_B_D2R_P<0>
TBT_B_D2R_N<0>
TBT_B_CONFIG1_BUF
TBT_B_CONFIG2_RC
TBT_B_R2D_C_P<1>
TBT_B_R2D_C_N<1>
TBT_B_D2R_P<1>
TBT_B_D2R_N<1>
TBT_B_LSTX
TBT_B_LSRX
DP_TBTPA_ML_C_P<1>
DP_TBTPA_ML_C_N<1>
DP_TBTPA_ML_C_P<3>
DP_TBTPA_ML_C_N<3>
DP_TBTPA_AUXCH_C_P
DP_TBTPA_AUXCH_C_N
DP_TBTPA_HPD
TBT_A_HV_EN
TBT_A_CIO_SEL
TBT_A_DP_PWRDN
DP_TBTPB_ML_C_P<1>
DP_TBTPB_ML_C_N<1>
DP_TBTPB_ML_C_P<3>
DP_TBTPB_ML_C_N<3>
DP_TBTPB_AUXCH_C_P
DP_TBTPB_AUXCH_C_N
DP_TBTPB_HPD
TBT_B_HV_EN
TBT_B_CIO_SEL
TBT_B_DP_PWRDN
PP3V3_TBTLC
BYPASS=U2890:2mm
CRITICAL
OMIT_TABLE
U2890
4MBIT
W25X40CLXIG
USON
(TBT_SPI_MOSI)
(TBT_SPI_CLK)
(TBT_SPI_CS_L)
TBTROM_WP_L
TBTROM_HOLD_L
(TBT_SPI_MISO)
OMIT
NOSTUFF
DEBUG: For monitoring current/voltage
DEBUG: For monitoring clock
Use AA8 GND ball for THERM_DN
Used for straps in host mode
Security strap setting is XORed with
bit in the flash, so the active-level
depends on the code in the flash.
If strap != bit then security is enabled?
NO STUFF
Divides 3.3V to 1.8V
=PP3V3_S4_TBT
SNK0 AC Coupling
SNK1 AC Coupling
NOTE: The following pins require testpoints:
0 - GPIO_13
1 - GPIO_1
2 - GPIO_2
3 - GPIO_3
4 - GPIO_5
5 - PCIE_RST_1_N
6 - PCIE_RST_2_N
7 - PCIE_RST_3_N
8 - GPIO_15
9 - GPIO_11
10 - GPIO_14
11 - GPIO_0
12 - GPIO_12
13 - GPIO_10
14 - PB_LSTX
15 - PB_LSRX
For unused port, pull CONFIG1, CONFIG2, LSRX, HPD and CIO_SEL low (10k). All other port signals can be NC.
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
Thunderbolt Host (1 of 2)
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
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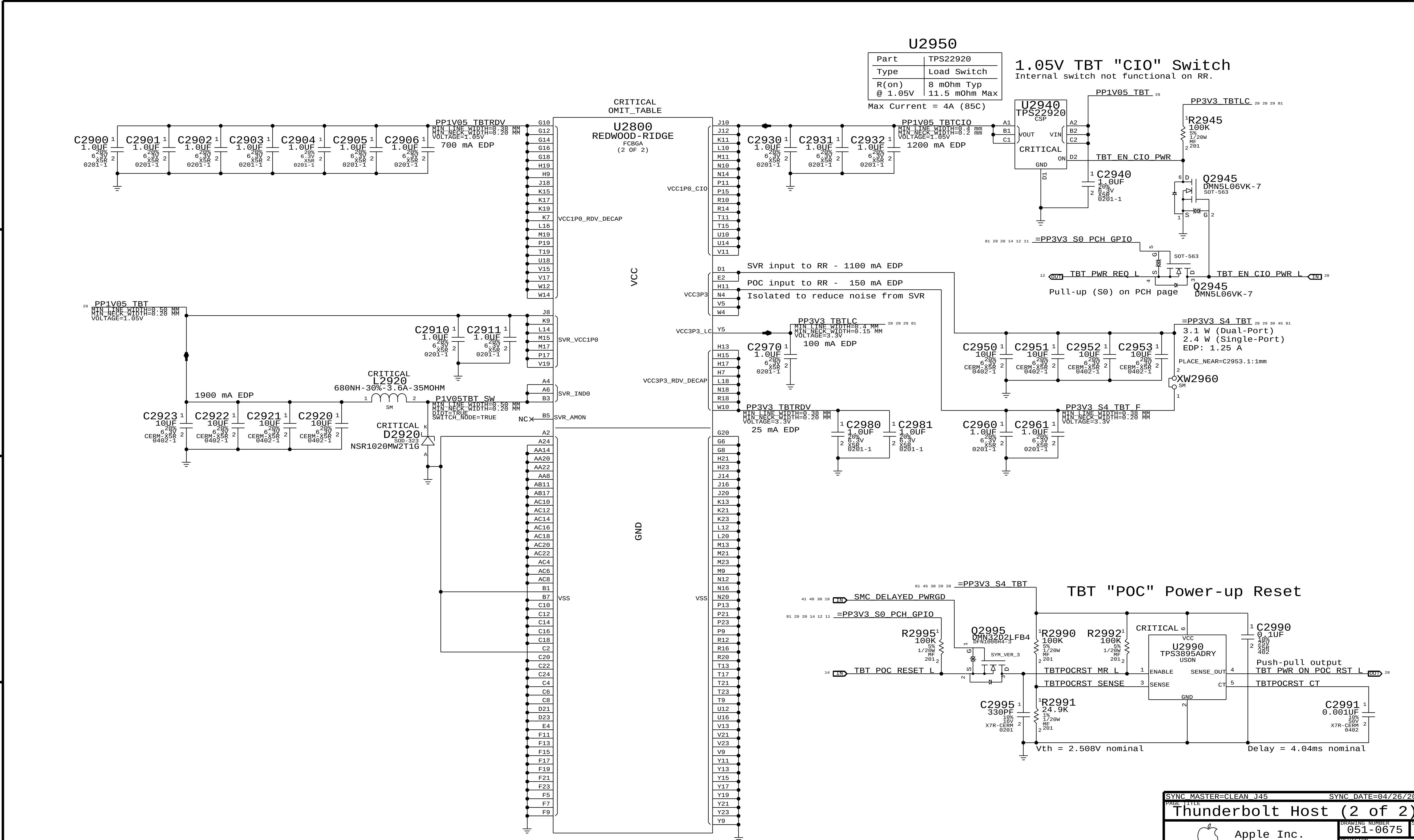

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Thunderbolt Host (2 of 2)

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EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

Page Notes

Power aliases required by this page:
- =PPVIN_SW_TBTBST (8-13V Boost Input)
- =PP15V_TBT_REG (15V Boost Output)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Thunderbolt 15V Boost Regulator

=PPVIN_SW_TBTBST
8-13V Input
Changes required
for 2S.

R3080 470K 5% 1/16W MF-LF 402
C3080 0.1UF 10% 25V X5R 402
TBTBST_PWREN_DIV_L
R3081 330K 5% 1/16W MF-LF 402
TBTBST_PWREN_L

Q3005 DMN5L06VK-7 SOT-563
Q3005 DMN5L06VK-7 SOT-563
TBT_A_HV_EN
TBT_B_HV_EN

CRITICAL
Q3080 SI8409DB BGA

SI8409DB:
Vds(max): -30V
Vgs(max): +/-12V
Vgs(th): -1.4V
Rds(on): 46mOhm @ 4.5V Vgs
Id(max): 3.7A @ 70C

PPVIN_SW_TBTBST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
Voltage not specified here,
add property on another page.

R3091 200K 1% 1/16W MF-LF 402 <R1>
R3092 73.2K 1% 1/16W MF-LF 402 <R2>

UVLO(falling) = 1.22 * (R1 + R2) / R2
UVLO(rising) = UVLO(falling) + (2uA * R1)
UVLO = 4.55V (falling), 4.95 (rising)

C3090 10UF 20% 25V X5R-CERM 0603
C3091 10UF 20% 25V X5R-CERM 0603

CRITICAL
L3095 3.3UH-6.5A PIMB063T-SM
TBTBST_BOOST
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

CRITICAL
U3090 LT3957 QFN

TBTBST_EN_UVLO
TBTBST_INTVCC
TBTBST_VC
TBTBST_RT
TBTBST_SS
TBTBST_VC_RC
GND_TBTBST_SGND
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V

C3085 2.2UF 20% 10V X5R-CERM 402
C3086 2.2UF 20% 10V X5R-CERM 402
C3087 68PF 5% 50V C0G-CERM 0402
R3093 49.9K 1% 1/16W MF-LF 402
C3092 2.2UF 20% 10V X5R-CERM 402
C3093 0.0033UF 10% 50V X7R-CERM 0402
R3094 26.7K 1% 1/16W MF-LF 402
C3094 0.33UF 10% 6.3V CERM-X5R 402

SGND
GND

SGND shorted to
GND inside package,
no XW necessary.

R3089 0 5% 1/20W MF 0201
CRITICAL
D3095 PDS540XF PWRDI5
TBTBST_SNS1
TBTBST_SNS2
XW3095 SM
PLACE_NEAR=C3095.1:2 mm
TBTBST_VSNS
C3088 10PF 5% 50V C0G-CERM 0402
R3095 137K 1% 1/16W MF-LF 402 <Ra>
NO STUFF
C3089 100PF 5% 50V CERM 402
R3096 15.8K 1% 1/16W MF-LF 402 <Rb>
TBTBST_FBX

Vout = 1.6V * (1 + Ra / Rb)

=PP15V_TBT_REG
Vout = 15.47V
Max Current = 2A?
Freq = 480KHz

C3095 33UF-0.060HM 20% 25V POLY-TANT CASE-D3L
C3096 10UF 10% 25V X5R 1206-2
NO STUFF
C3097 10UF 10% 25V X5R 805
C3099 0.001UF 10% 50V X7R-CERM 0402

Q3088 DMN5L06VK-7 SOT-563
Max Vgs: 10V
R3088 330K 5% 1/10W MF-LF 402
TBTBST_SHDN_DIV
R3087 330K 5% 1/10W MF-LF 402
Q3088 DMN5L06VK-7 SOT-563
SMC_DELAYED_PWRGD

BATLOW# Isolation

Q3000 DMN3202LFB4 DFN1006H4-3 SYM_VER_3
=PP3V3_S4_TBT
Pull-up on RR page
PM_BATLOW_L
=TBT_BATLOW_L
TBT_BATLOW_L
MAKE_BASE=TRUE

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Thunderbolt Mobile Support

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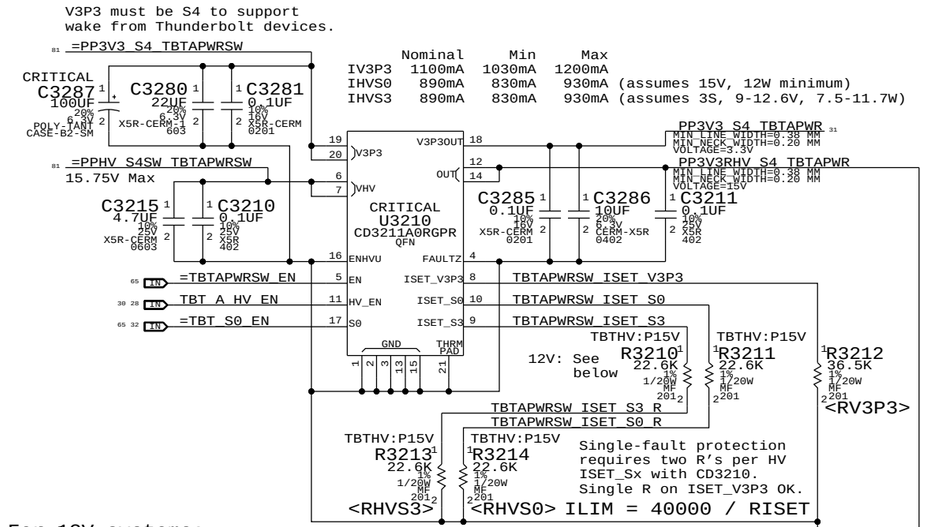
3.3V/HV Power MUX

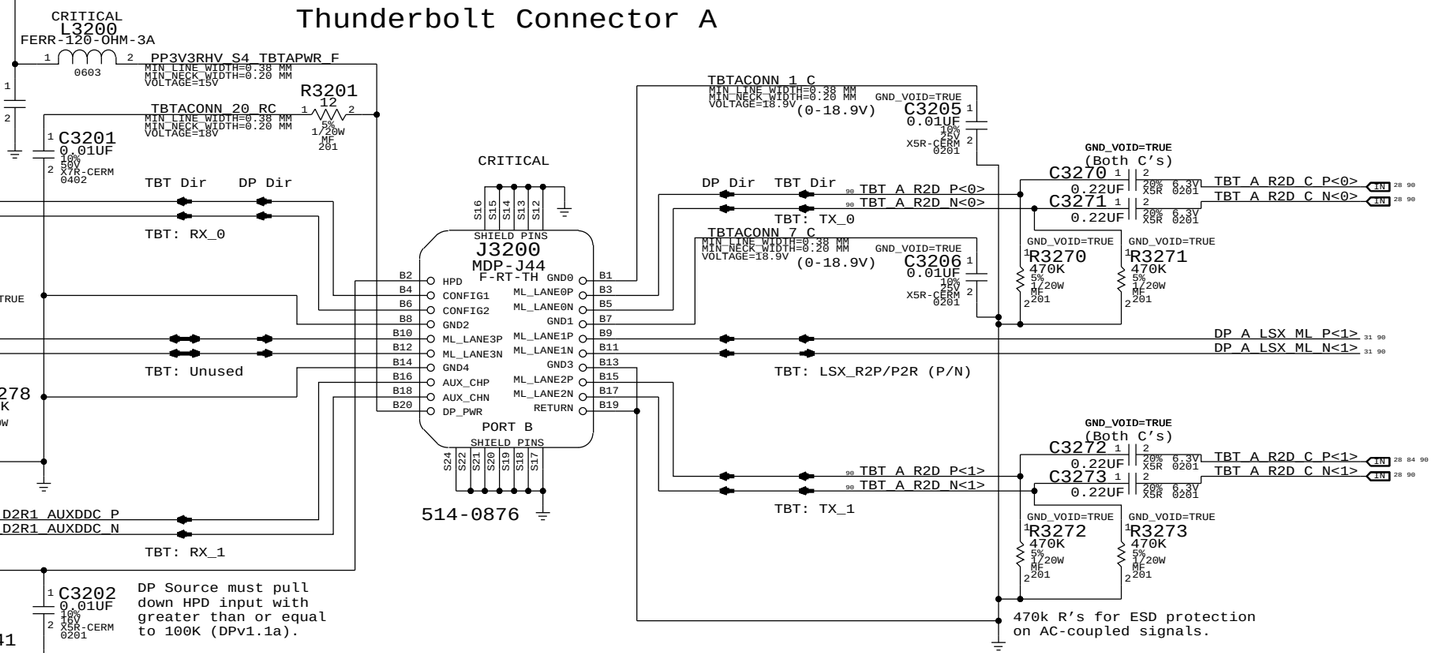


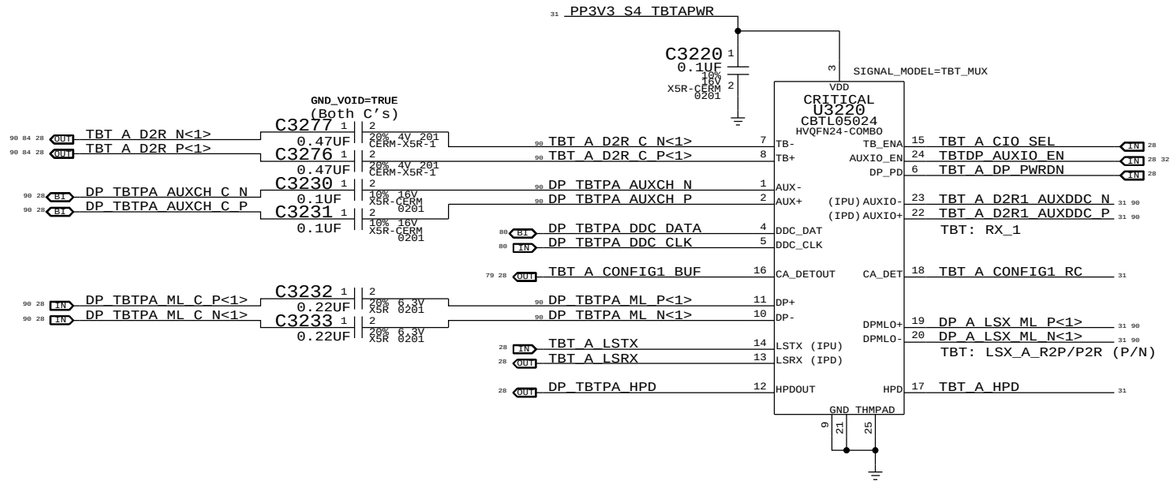
For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3210,R3213		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3211,R3214		TBTHV:P12V

	Nominal	Min	Max
IHVS0/S3	1120mA	1090mA	1170mA (12W minimum)

Thunderbolt Connector A





SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
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3.3V/HV Power MUX

V3P3 must be S4 to support
wake from Thunderbolt devices.

	Nominal	Min	Max	
IV3P3	1100mA	1030mA	1200mA	
IHVS0	890mA	830mA	930mA	(assumes 15V, 12W minimum)
IHVS3	890mA	830mA	930mA	(assumes 3S, 9-12.6V, 7.5-11.7W)

81 =PP3V3_S4_TBTBPWRSW
81 =PPHV_S4SW_TBTBPWRSW
15.75V Max
CRITICAL
C3387 100UF 20% 6.3V POLY-TANT CASE-B2-SM
C3380 22UF 20% 6.3V X5R-CERM 603
C3381 0.1UF 10% 16V X5R-CERM 0201
C3315 4.7UF 10% 25V X5R-CERM 0603
C3310 0.1UF 10% 25V X5R 402
CRITICAL U3310 CD3211A0RGPR QFN
V3P3 (19,20) VHV (6,7) ENHVU (16) EN (5) HV_EN (11) S0 (17) V3P3OUT (18) OUT (12,14) FAULTZ (4) ISET_V3P3 (8) ISET_S0 (10) ISET_S3 (9) GND (1,2,3,13,15) THRM PAD (21)
C3385 0.1UF 10% 16V X5R-CERM 0201
C3386 10UF 20% 6.3V CERM-X5R 0402
C3311 0.1UF 10% 25V 402
PP3V3_S4_TBTBPWR 32 MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=3.3V
PP3V3RHV_S4_TBTBPWR MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
65 IN =TBTBPWRSW_EN
30 28 IN TBT_B_HV_EN
65 31 IN =TBT_S0_EN
TBTBPWRSW_ISET_V3P3
TBTBPWRSW_ISET_S0
TBTBPWRSW_ISET_S3
TBTHV:P15V R3310 22.6K 1% 1/20W MF 201 2
TBTHV:P15V R3311 22.6K 1% 1/20W MF 201 2
R3312 36.5K 1% 1/20W MF 201 2 <RV3P3>
12V: See below
TBTBPWRSW_ISET_S3_R
TBTBPWRSW_ISET_S0_R
TBTHV:P15V R3313 22.6K 1% 1/20W MF 201 2 <RHVS3>
TBTHV:P15V R3314 22.6K 1% 1/20W MF 201 2 <RHVS0>
Single-fault protection requires two R's per HV ISET_Sx with CD3210. Single R on ISET_V3P3 OK.
ILIM = 40000 / RISET

For 12V systems:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3310,R3313		TBTHV:P12V
118S0145	2	RES,MTL FILM,1/20W,17.8K,1,0201,SMD,LF	R3311,R3314		TBTHV:P12V

	Nominal	Min	Max	
IHVS0/S3	1120mA	1090mA	1170mA	(12W minimum)

Thunderbolt Connector B

CRITICAL L3300 FERR-120-OHM-3A 0603
PP3V3RHV_S4_TBTBPWR_F MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=15V
C3300 0.01UF 10% 50V X7R-CERM 0402
C3301 0.01UF 10% 50V X7R-CERM 0402
R3301 12 5% 1/20W MF 201
TBTBCONN_20_RC MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18V

TBT Dir DP Dir
TBT: RX_0
TBT: Unused
TBT: RX_1

GND_VOID=TRUE (Both C's)
C3374 0.47UF 20% 4V 201 CERM-X5R-1
C3375 0.47UF 20% 4V 201 CERM-X5R-1
90 28 OUT TBT_B_D2R_P<0>
90 28 OUT TBT_B_D2R_N<0>
90 TBT_B_D2R_C_P<0>
90 TBT_B_D2R_C_N<0>
R3394 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE
R3395 1K 5% 1/20W MF 201 NO_XNET_CONNECTION=TRUE

C3378 0.22UF 20% 6.3V X5R 0201
C3379 0.22UF 20% 6.3V X5R 0201
90 28 IN DP_TBTPB_ML_C_P<3>
90 28 IN DP_TBTPB_ML_C_N<3>
90 DP_TBTPB_ML_P<3>
90 DP_TBTPB_ML_N<3>
R3379 470K 5% 1/20W MF 201
R3378 470K 5% 1/20W MF 201

90 32 TBT_B_D2R1_AUXDDC_P
90 32 TBT_B_D2R1_AUXDDC_N

32 TBT_B_HPD
32 TBT_B_CONFIG1_RC
28 OUT TBT_B_CONFIG2_RC
R3352 1M 5% 1/20W MF 201
R3351 1M 5% 1/20W MF 201
C3394 330PF 10% 16V X7R-CERM 0201
C3395 330PF 10% 16V X7R-CERM 0201
R3341 100K 5% 1/20W MF 201
C3302 0.01UF 10% 16V X5R-CERM 0201
DP Source must pull down HPD input with greater than or equal to 100K (DPv1.1a).
Sink HPD range:
High: 2.0 - 5.0V
Low: 0 - 0.8V

CRITICAL J3200 MDP-J44 F-RT-TH SHIELD PINS S1 S2 S3 S4 S5 PORT A SHIELD PINS S6 S7 S8 S9 S10 S11 S23
A2 HPD
A4 CONFIG1
A6 CONFIG2
A8 GND2
A10 ML_LANE3P
A12 ML_LANE3N
A14 GND4
A16 AUX_CHP
A18 AUX_CHN
A20 DP_PWR
A1 ML_LANE0P
A3 ML_LANE0N
A5 GND1
A7 ML_LANE1P
A9 ML_LANE1N
A11 GND3
A13 ML_LANE2P
A15 ML_LANE2N
A17 RETURN
A19
514-0876

32 PP3V3_S4_TBTBPWR
C3320 0.1UF 10% 16V X5R-CERM 0201
CRITICAL U3320 CBTL05024 HVQFN24-COMBO
VDD (3) SIGNAL_MODEL=TBT_MUX
GND_THMPAD (9,21,25)

90 28 OUT TBT_B_D2R_N<1>
90 28 OUT TBT_B_D2R_P<1>
C3377 0.47UF 20% 4V 201 CERM-X5R-1
C3376 0.47UF 20% 4V 201 CERM-X5R-1
90 TBT_B_D2R_C_N<1>
90 TBT_B_D2R_C_P<1>
90 28 DP_TBTPB_AUXCH_C_N
90 28 DP_TBTPB_AUXCH_C_P
C3330 0.1UF 10% 16V X5R-CERM 0201
C3331 0.1UF 10% 16V X5R-CERM 0201
90 DP_TBTPB_AUXCH_N
90 DP_TBTPB_AUXCH_P
90 28 DP_TBTPB_ML_C_P<1>
90 28 DP_TBTPB_ML_C_N<1>
C3332 0.22UF 20% 6.3V X5R 0201
C3333 0.22UF 20% 6.3V X5R 0201
90 DP_TBTPB_ML_P<1>
90 DP_TBTPB_ML_N<1>
28 IN TBT_B_LSTX
28 OUT TBT_B_LSRX
28 OUT DP_TBTPB_HPD
89 IN DP_TBTPB_DDC_DATA
89 IN DP_TBTPB_DDC_CLK
79 28 OUT TBT_B_CONFIG1_BUF

TBT_B_D2R_C_N<1> 7 TB-
TBT_B_D2R_C_P<1> 8 TB+
DP_TBTPB_AUXCH_N 1 AUX-
DP_TBTPB_AUXCH_P 2 AUX+
DP_TBTPB_DDC_DATA 4 DDC_DAT
DP_TBTPB_DDC_CLK 5 DDC_CLK
TBT_B_CONFIG1_BUF 16 CA_DETOUT
DP_TBTPB_ML_P<1> 11 DP+
DP_TBTPB_ML_N<1> 10 DP-
TBT_B_LSTX 14 LSTX (IPU)
TBT_B_LSRX 13 LSRX (IPD)
DP_TBTPB_HPD 12 HPDOUT

TB_ENA 15 TBT_B_CIO_SEL IN 28
AUXIO_EN 24 TBTDP_AUXIO_EN IN 28 31
DP_PD 6 TBT_B_DP_PWRDN IN 28
(IPU) AUXIO- 23 TBT_B_D2R1_AUXDDC_N 32 90
(IPD) AUXIO+ 22 TBT_B_D2R1_AUXDDC_P 32 90
TBT: RX_1
CA_DET 18 TBT_B_CONFIG1_RC 32
DPML0+ 19 DP_B_LSX_ML_P<1> 32 90
DPML0- 20 DP_B_LSX_ML_N<1> 32 90
TBT: LSX_A_R2P/P2R (P/N)
HPD 17 TBT_B_HPD 32

TBTBCONN_1_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
C3305 0.01UF 10% 25V X5R-CERM 0201 GND_VOID=TRUE (0-18.9V)
TBTBCONN_7_C MIN_LINE_WIDTH=0.38 MM MIN_NECK_WIDTH=0.20 MM VOLTAGE=18.9V
C3306 0.01UF 10% 25V X5R-CERM 0201 GND_VOID=TRUE (0-18.9V)

DP Dir TBT Dir
90 TBT_B_R2D_P<0>
90 TBT_B_R2D_N<0>
TBT: TX_0
90 TBT_B_R2D_P<1>
90 TBT_B_R2D_N<1>
TBT: TX_1

GND_VOID=TRUE (Both C's)
C3370 0.22UF 20% 6.3V X5R 0201
C3371 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<0> IN 28 90
TBT_B_R2D_C_N<0> IN 28 90
R3370 470K 5% 1/20W MF 201
R3371 470K 5% 1/20W MF 201
DP_B_LSX_ML_P<1> 32 90
DP_B_LSX_ML_N<1> 32 90
C3372 0.22UF 20% 6.3V X5R 0201
C3373 0.22UF 20% 6.3V X5R 0201
TBT_B_R2D_C_P<1> IN 28 90
TBT_B_R2D_C_N<1> IN 28 90
R3372 470K 5% 1/20W MF 201
R3373 470K 5% 1/20W MF 201
470K R's for ESD protection on AC-coupled signals.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
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Apple Inc.
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BRANCH: dvt
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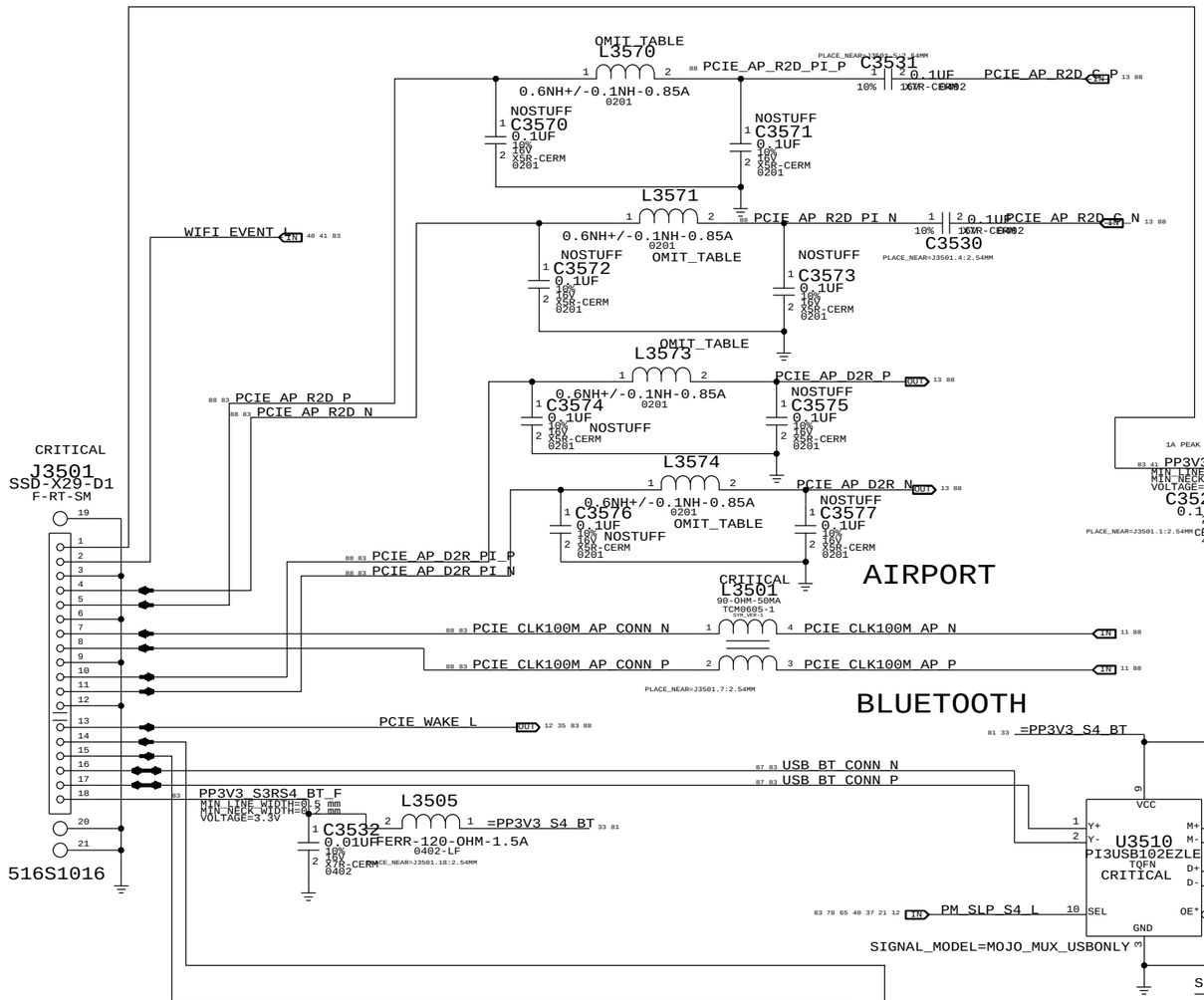
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	4	RES, 0OHM, 0201	L3570,L3571,L3573,L3574		



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

X29C CONNECTOR

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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OOB Isolation

=PP3V3_S0SW_SSD

BYPASS=U3710:5 mm
C3718 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3710 08
SMC_OOB1_R2D_L (IN)
NC

=PP3V3_S0_OOB1_PWRDN

BYPASS=U3711:5 mm
C3719 0.1UF 10% 10V X5R-CERM 0201

CRITICAL
74LVC1G08 SOT891
U3711 08
SMC_OOB1_D2R_L (OUT)
NC

PLACE_NEAR=J3700.1:3mm
CRITICAL
L3700 FERR-26-OHM-6A 0603
=PP3V3_S0SW_SSD
PP3V3_S0SW_SSD_FLT
MIN_LINE_WIDTH=0.6mm
MIN_NECK_WIDTH=0.15mm
VOLTAGE=3.3V
C3701 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=L3700.1:1mm
C3702 0.1UF 10% 10V X5R-CERM 0201 PLACE_NEAR=L3700.1:1mm

514S0449
CRITICAL
J3700 SSD-GS3 F-RT-SM

R3700 100K 1% 1/20W MF 0201

GND_VOID	1	53	GND_VOID		
	2	52	SMC_OOB1_R2D_CONN_L		
	3	51	SMC_OOB1_D2R_CONN_L		
	4				
	5	50	SSD_PCIE_SEL_L	OUT	18
=PP3V3_S0_SSD_AUX	6	49	SSD_DEVSLP	IN	20
SSD_RESET_CONN_L	7	48	SMC_PWRFAIL_WARN_L	IN	40
NC_SSD_MFG_RSVD	8	47	=SSD_CTRL_EN	IN	34
	9				
	10	46			
PCIE_SSD_R2D_C_N<3>	11	45	PCIE_SSD_D2R_N<3>	OUT	13 88
PCIE_SSD_R2D_C_P<3>	12	44	PCIE_SSD_D2R_P<3>	OUT	13 88
	13	43			
PCIE_SSD_R2D_C_N<2>	14	42	PCIE_SSD_D2R_N<2>	OUT	13 88
PCIE_SSD_R2D_C_P<2>	15	41	PCIE_SSD_D2R_P<2>	OUT	13 88
	16	40			
	17	39			
PCIE_SSD_R2D_C_N<1>	18	38	PCIE_SSD_D2R_N<1>	OUT	13 88
PCIE_SSD_R2D_C_P<1>	19	37	PCIE_SSD_D2R_P<1>	OUT	13 88
	20	36			
PCIE_SSD_R2D_C_N<0>	21	35	PCIE_SSD_D2R_N<0>	OUT	13 88
PCIE_SSD_R2D_C_P<0>	22	34	PCIE_SSD_D2R_P<0>	OUT	13 88
	23	33			
SSD_CLKREQ_CONN_L	24				
	25	32			
	26	31	PCIE_CLK100M_SSD_N	IN	11 88
	27	30	PCIE_CLK100M_SSD_P	IN	11 88
	28	29			
	54	59			
	55	60			
	56	61			
	57	62			
	58	63			

PCIE_SSD_R2D_C_N<3> C3710 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_P<3> C3711 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_N<2> C3712 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_P<2> C3713 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_N<1> C3714 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_P<1> C3715 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_N<0> C3716 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201
PCIE_SSD_R2D_C_P<0> C3717 0.1UF 2 GND_VOID=TRUE 10% 16V X5R-CERM 0201

Per Intel PDG, use PCIe style decoupling, when muxing PCIe & SATA

Gumstick3 Connector

Supervisor & CLKREQ# Isolation

Delay = ~55ms

=PP3V3_S0SW_SSD
=PP3V42_G3H_SSDSAK
R3740 100K 5% 1/20W MF 201
R3741 232K 1% 1/20W MF 201
P3V3SSD_VMON
CRITICAL
C3740 0.1UF 10% 6.3V CERM-X5R 0201
U3740 SLG4AP016V TDFN
VDD
SENSE 0.7V
DLY
RESET*
MR*
EN
OUT (OD)
IN
THRM PAD
GND
APN 343S0511
SSD_RESET_L (IN 20)
=SSD_CTRL_EN (IN 34)
SSD_CLKREQ_L (OUT 11)
R3742 100K 1% 1/20W MF 201

34 =SSD_CTRL_EN — SSD_PWR_FET_EN 64
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
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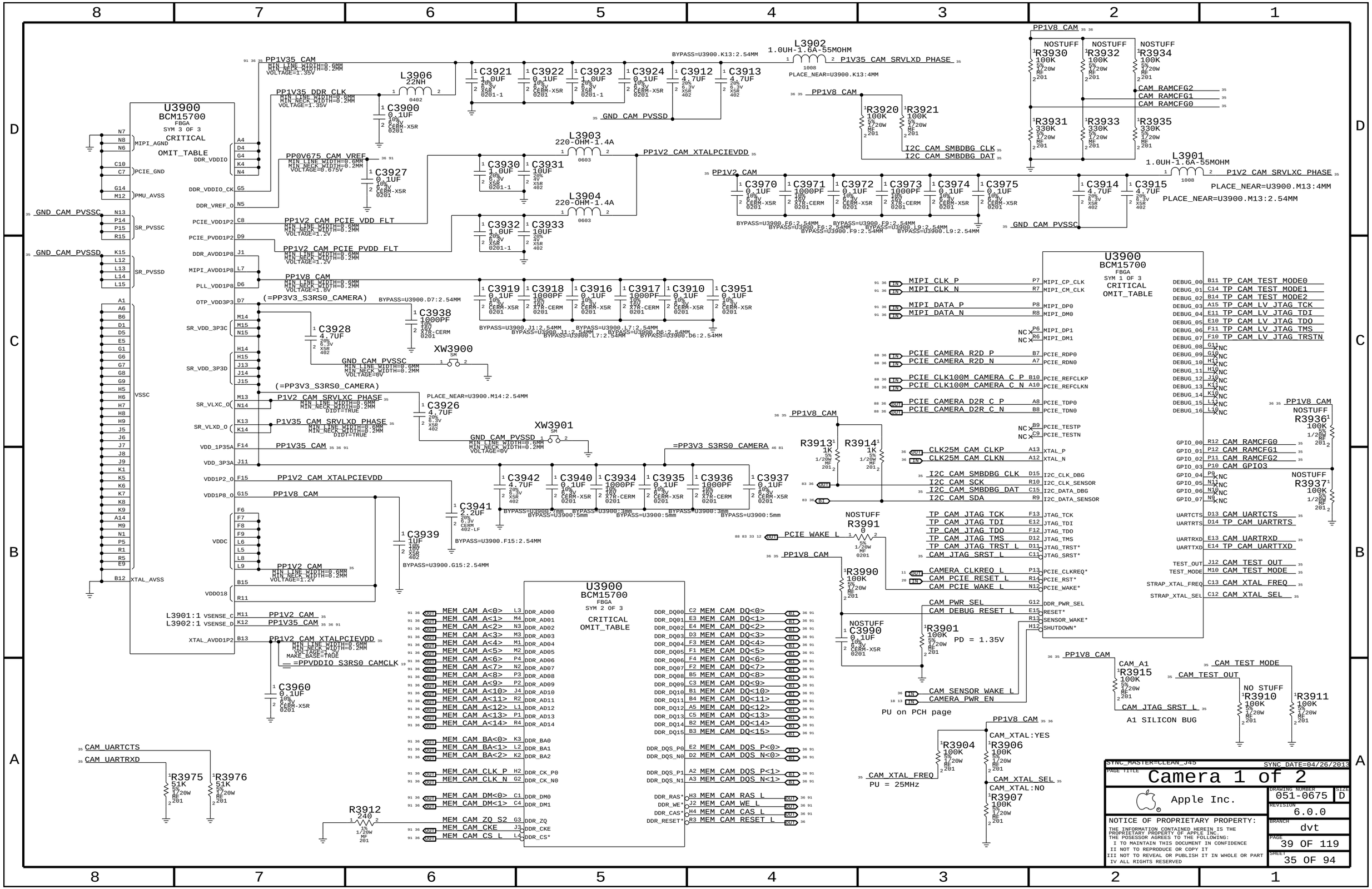
U3900
BCM15700
FBGA
SYM 3 OF 3
CRITICAL
OMIT_TABLE
PP1V35 CAM
PP1V35 DDR CLK
PP0V675 CAM VREF
PP1V2 CAM PCIE VDD FLT
PP1V2 CAM PVDD FLT
PP1V8 CAM
(=PP3V3_S3RS0_CAMERA)
P1V2 CAM SRVLXC PHASE
P1V35 CAM SRVLXD PHASE
PP1V35 CAM
PP1V2 CAM XTALPCIEVDD
PP1V2 CAM
=PP3V3_S3RS0_CAMERA
GND CAM PVSSD
GND CAM PVSSC
XW3900
XW3901
L3902
1.0UH-1.6A-55MOHM
L3903
220-OHM-1.4A
L3904
220-OHM-1.4A
L3901
1.0UH-1.6A-55MOHM
P1V2 CAM SRVLXC PHASE
P1V8 CAM
NOSTUFF
R3930
R3932
R3934
R3931
R3933
R3935
R3920
R3921
CAM RAMCFG2
CAM RAMCFG1
CAM RAMCFG0
I2C CAM SMBDBG CLK
I2C CAM SMBDBG DAT
MIPI CLK P
MIPI CLK N
MIPI DATA P
MIPI DATA N
PCIE CAMERA R2D P
PCIE CAMERA R2D N
PCIE CLK100M CAMERA C P
PCIE CLK100M CAMERA C N
PCIE CAMERA D2R C P
PCIE CAMERA D2R C N
CLK25M CAM CLKP
CLK25M CAM CLKN
I2C CAM SCK
I2C CAM SDA
TP CAM JTAG TCK
TP CAM JTAG TDI
TP CAM JTAG TDO
TP CAM JTAG TMS
TP CAM JTAG TRST L
CAM JTAG SRST L
CAMERA CLKREQ L
CAM PCIE RESET L
CAM PCIE WAKE L
CAM PWR SEL
CAM DEBUG RESET L
CAM SENSOR WAKE L
CAMERA PWR EN
PCIE WAKE L
R3913
R3914
R3990
R3991
R3901
R3936
R3937
R3904
R3906
R3907
R3910
R3911
R3915
R3975
R3976
R3912
CAM UARTCTS
CAM UARTRXD
CAM TEST MODE
CAM TEST OUT
CAM XTAL FREQ
PU = 25MHz
PU on PCH page
A1 SILICON BUG
CAM_XTAL:YES
CAM_XTAL:NO
PD = 1.35V
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
Camera 1 of 2
Apple Inc.
DRAWING NUMBER
051-0675
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REVISION
6.0.0
BRANCH
dvt
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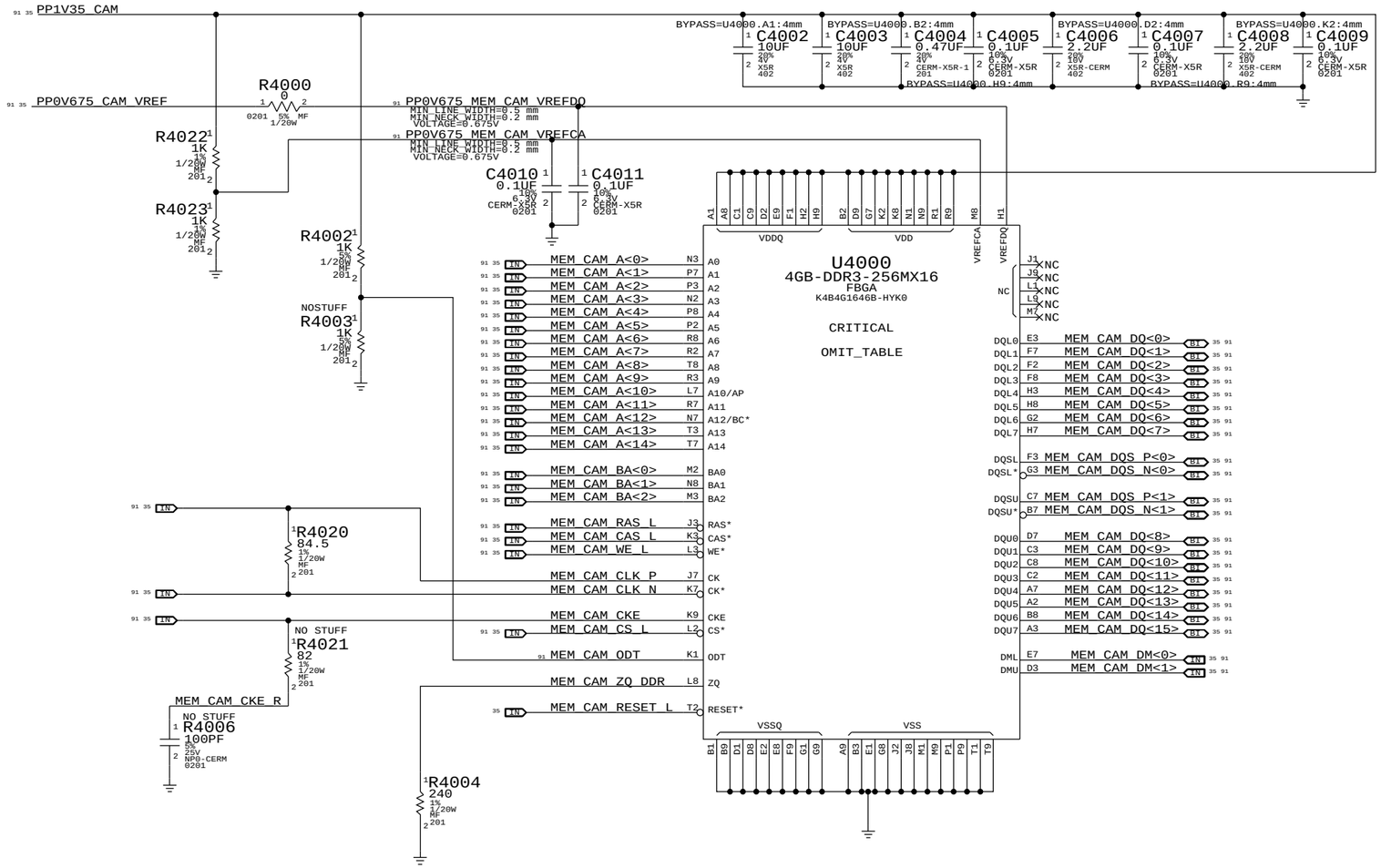


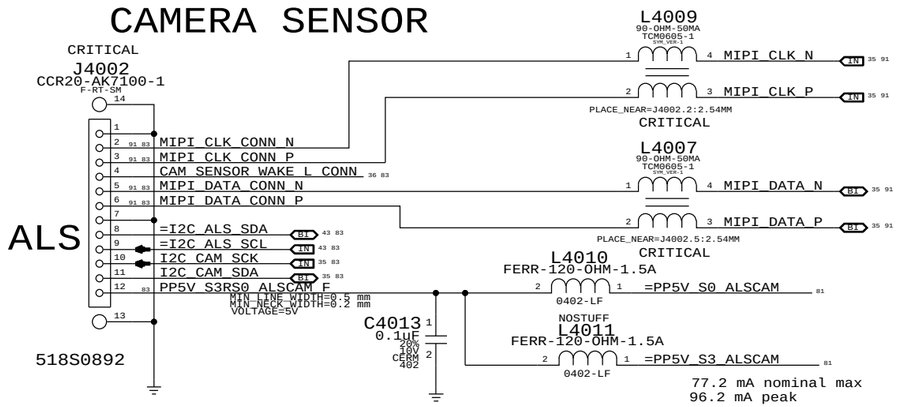
remove DRAM SPD Straps

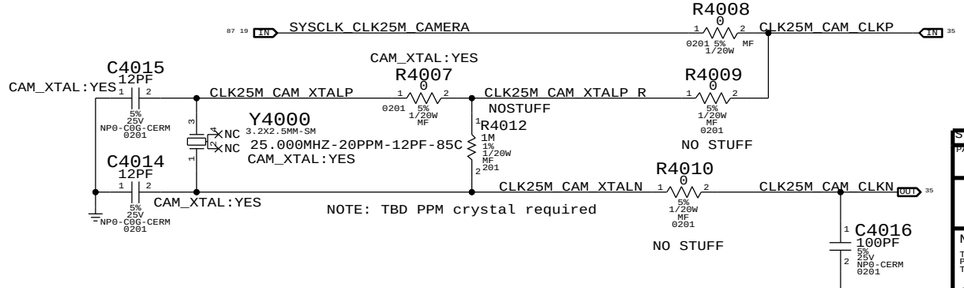
DRAM CFG Chart

VENDOR	CFG 1	CFG 0
HYNIX	0	0
SAMSUNG	1	0
MICRON	0	1
ELPIDA	1	1

DIE REV	CFG 2
A	0
B	1

CAMERA SENSOR





SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Camera 2 of 2

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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BRANCH: dvt
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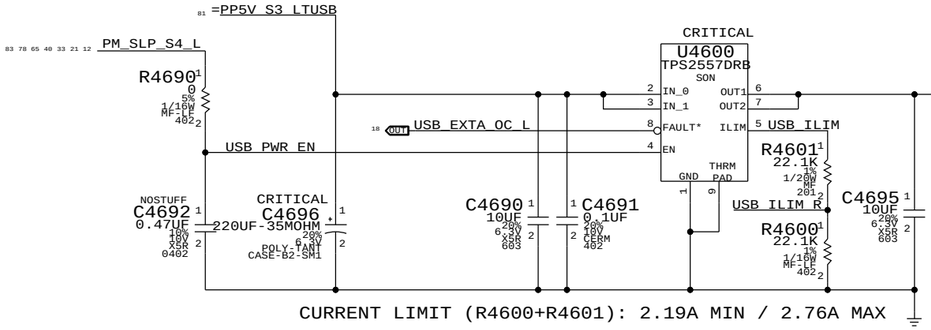
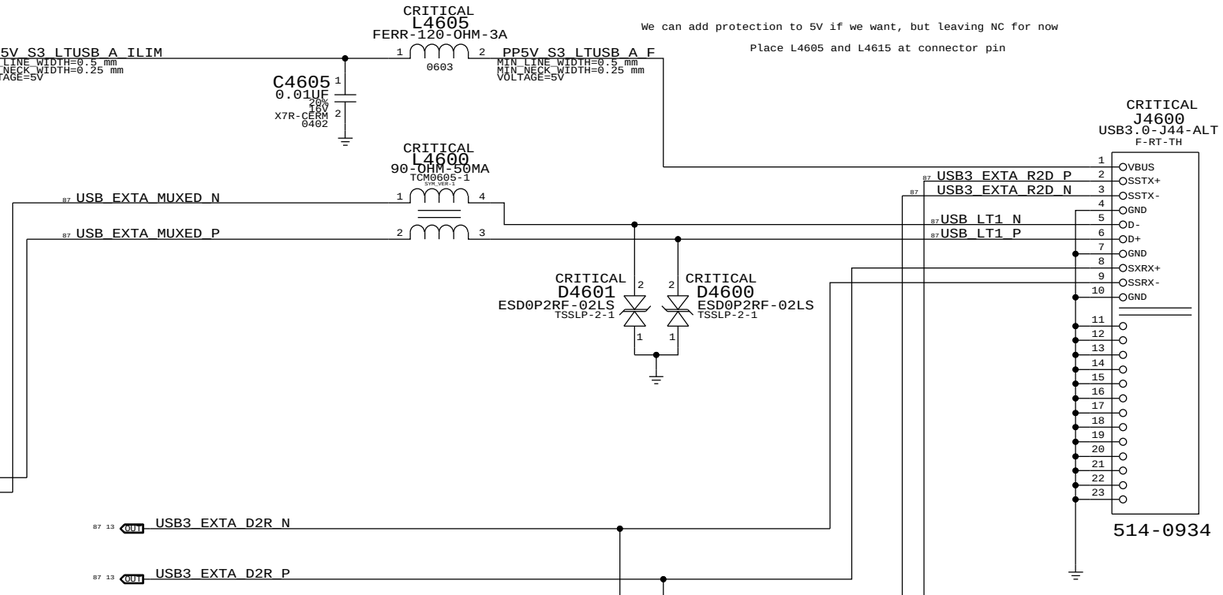
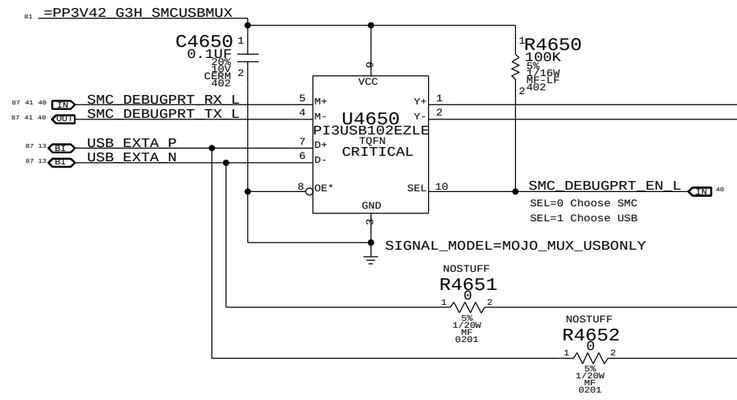
USB Port Power Switch

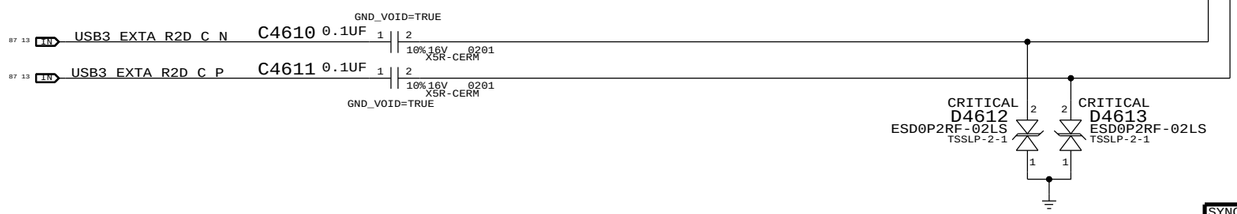


Left USB Port A



USB/SMC Debug Mux





SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: USB 3.0 CONNECTORS

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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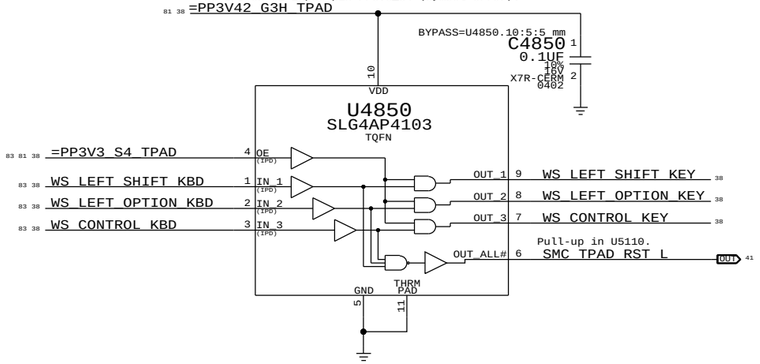
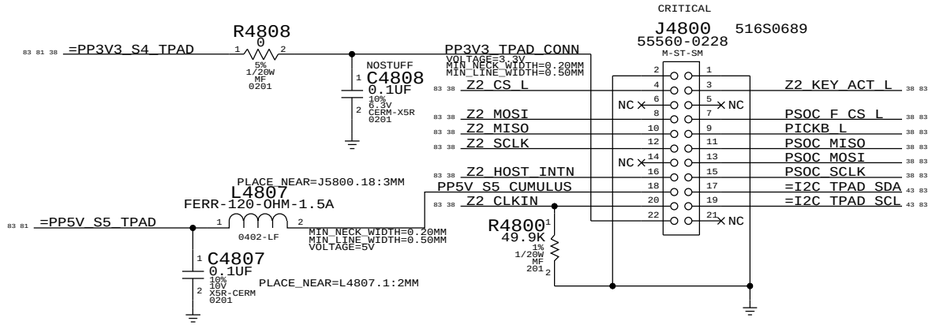
SMC Manual Reset & Isolation

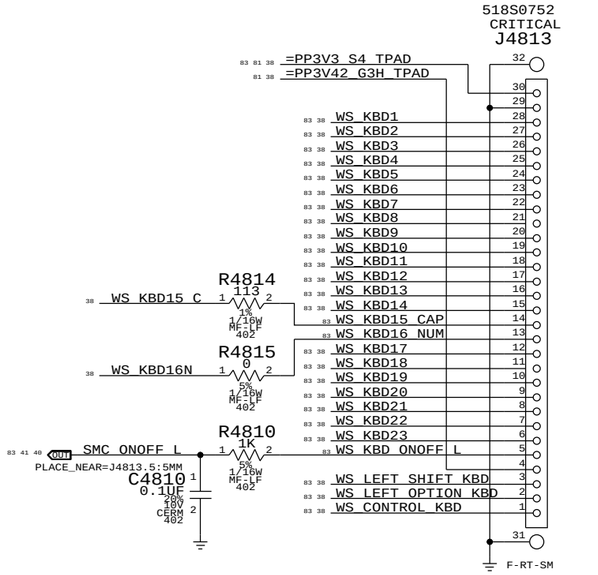
Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSoC power to isolate when PSoC is not powered.
No IPD on OE input pin PP3V3_S4 (symbol error).



IPD Flex Connector

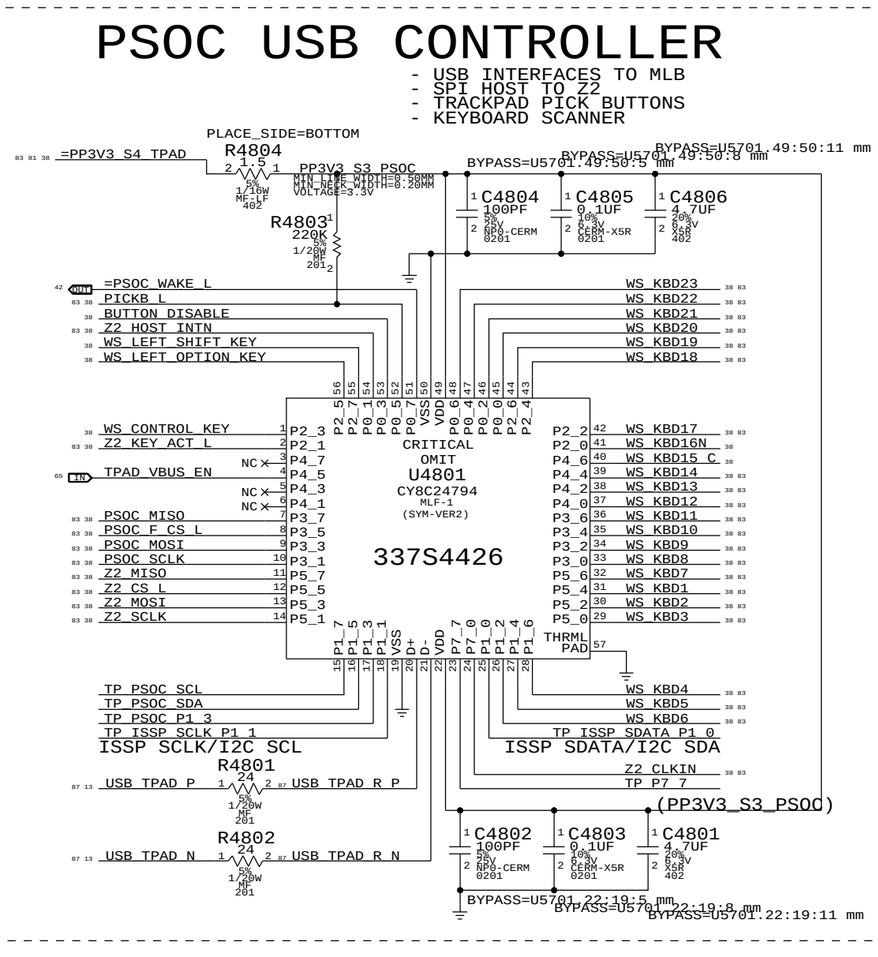


Keyboard Connector

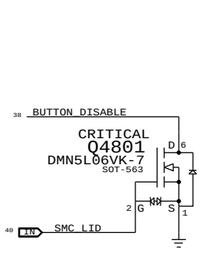


PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA	2.55 KOHM	0.0255 V	0.255E-6 W
		80UA		0.204 V	16.32E-6 W
3V3 LDO	VDD	60MA (MAX)	10 OHM	0.6 V	36E-3 W
	VOUT	60MA (MAX)	0.2 OHM	0.012 V	0.72E-3 W
PSOC	VDD	8MA (TYP)	1.5 OHM	0.012 V	96E-6 W
		14MA (MAX)		0.021 V	294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: KEYBOARD/TRACKPAD (1 OF 2)

Apple Inc.

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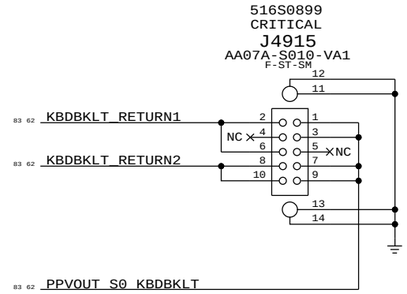
Keyboard Backlight Connector



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
KEYBOARD/TRACKPAD (2 OF 2)

Apple Inc.

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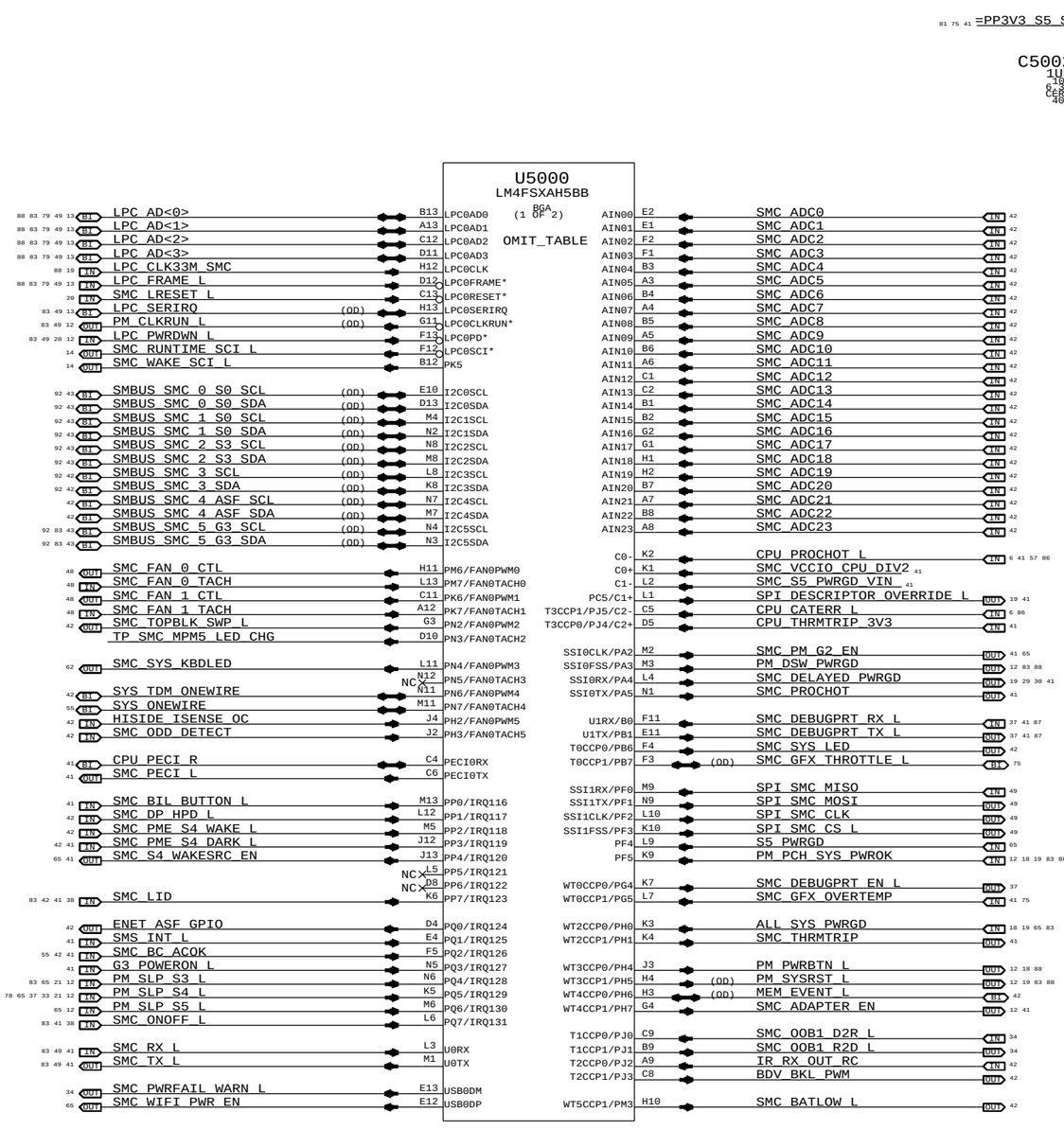
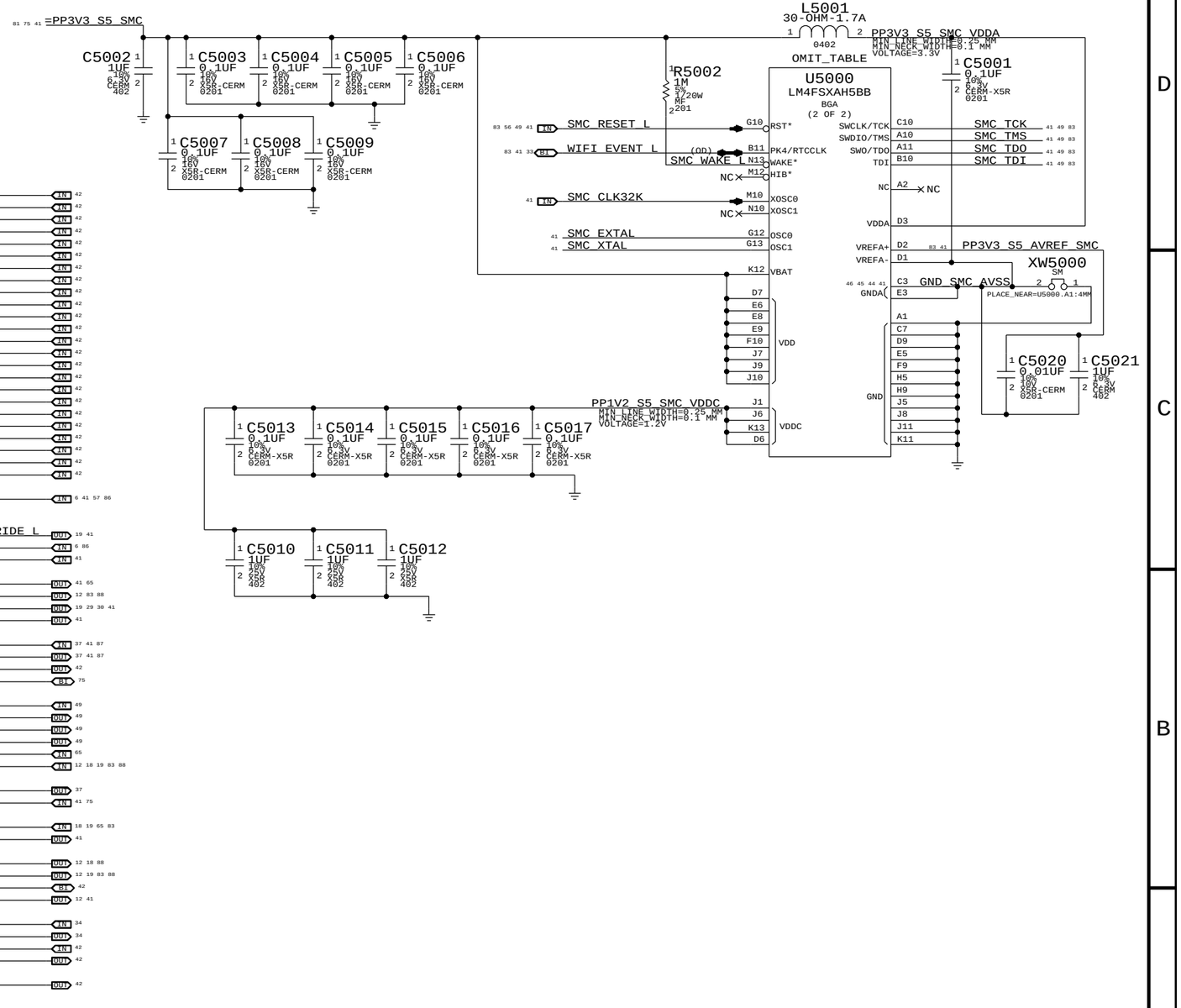
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.





NOTE: SMS Interrupt can be active high or low, rename net accordingly. If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: SMC

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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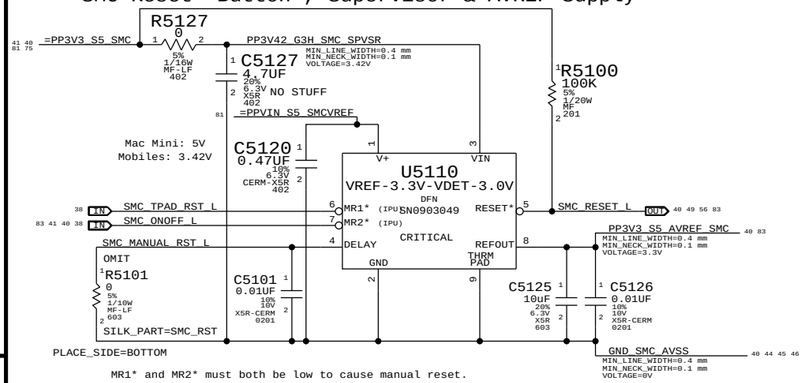
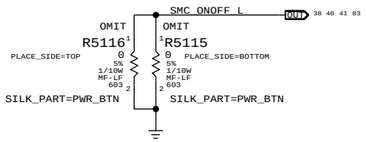
SMC Reset "Button", Supervisor & AVREF Supply



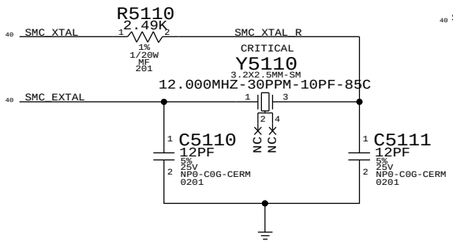
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

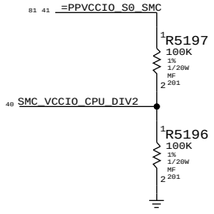
Debug Power "Buttons"



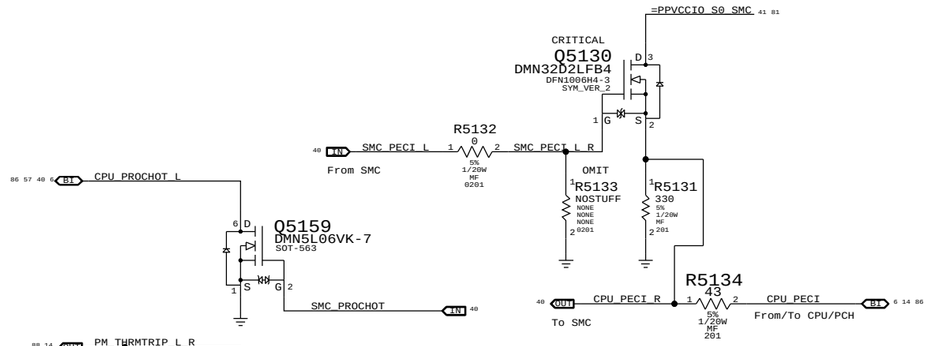
SMC Crystal Circuit

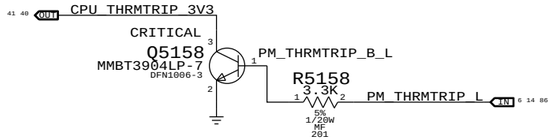


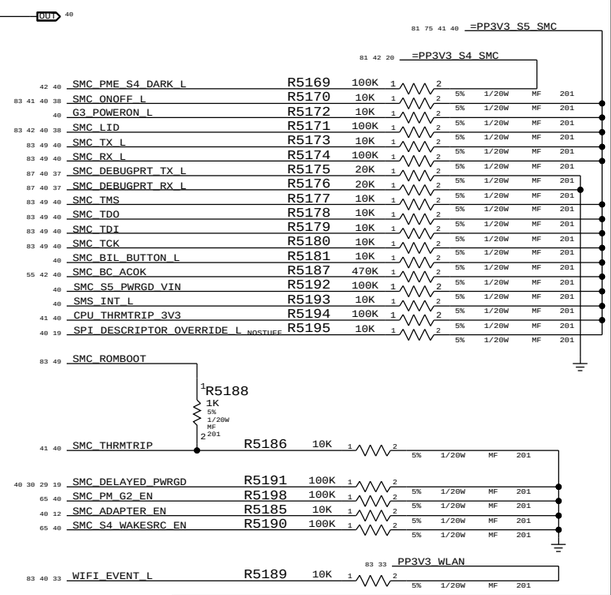
SMC USB CLOCK REQUIRE THESE CRYSTAL VALUES:5,6,8,10,12,16,18,20,24,25 MHZ



SMC12 PECI SUPPORT







SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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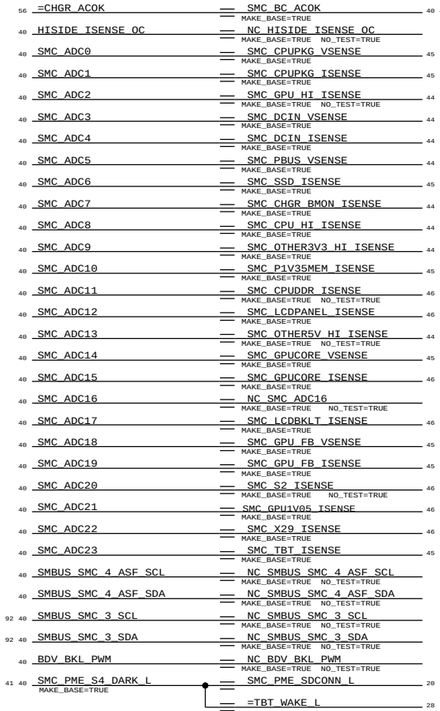
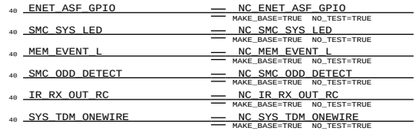
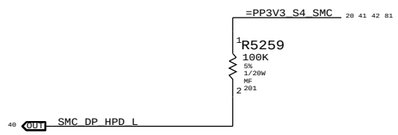


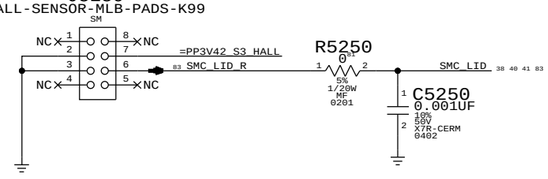


Spare S4 IRQ

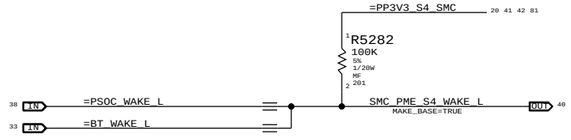


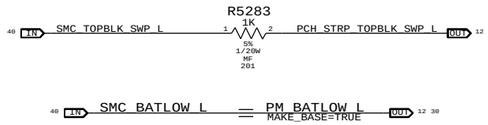
Hall Effect pads

APN: 998-3029
OMIT_TABLE
J5250
HALL-SENSOR-MLB-PADS-K99



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
607-6811	1	SUBASSY,PCBA HALL EFFECT,K99	J5250	CRITICAL	





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SMC Project Support

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PCH SMBus "0" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(MASTER)
SMBUS_PCH_CLK
SMBUS_PCH_DATA

R5300 1K 5% 1/16W MF-LF 402
R5301 1K 5% 1/16W MF-LF 402

VRef DACs
U2200
(Write: 0x98 Read: 0x99)
=I2C_VREFDACS_SCL
=I2C_VREFDACS_SDA

Margin Control
U2201
(Write: 0x30 Read: 0x31)
=I2C_PCA9557D_SCL
=I2C_PCA9557D_SDA

XDP Connectors
J1800 & J1850
(MASTER)
=SMBUS_XDP_SCL
=SMBUS_XDP_SDA

R5390 0 5% 1/16W MF-LF 402
R5391 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

NO STUFF
R5392 0 5% 1/16W MF-LF 402
R5393 0 5% 1/16W MF-LF 402

HDMI Redriver (on RIO)
J9510 -> U9700
(WRITE: 0xCC READ: 0xCD)
I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA
I2C_HDMIRDRV_SCL
I2C_HDMIRDRV_SDA

PCH "SMLink 0" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(MASTER)
SML_PCH_0_CLK
SML_PCH_0_DATA

R5310 8.2K 5% 1/16W MF-LF 402
R5311 8.2K 5% 1/16W MF-LF 402

PCH "SMLink 1" Connections

=PP3V3_S0_SMBUS_PCH

Lynx Point
U1100
(Write: 0x88 Read: 0x89)
SML_PCH_1_CLK
SML_PCH_1_DATA

NO STUFF
R5320 8.2K 5% 1/20W MF 201
NO STUFF
R5321 8.2K 5% 1/20W MF 201

R5323 0 5% 1/20W MF 0201
R5322 0 5% 1/20W MF 0201

SMLink 1 is slave port to access PCH & CPU via PECI.

SMC "0" SMBus Connections

=PP3V3_S0_SMBUS_SMC_0_S0

SMC
U5000
(MASTER)
SMB_0_S0_CLK
SMB_0_S0_DATA

R5350 2.0K 5% 1/16W MF-LF 402
R5351 2.0K 5% 1/16W MF-LF 402

L&R Fin Stack Temp
EMC1414-A: U5850
(Write: 0x98 Read: 0x99)
=SMBUS_GPUTHMSNS_SCL
=SMBUS_GPUTHMSNS_SDA

SMBUS_SMC_0_S0_SCL
SMBUS_SMC_0_S0_SDA

J4002
ALS
(Write: 0x72 Read: 0x73)
=I2C_ALS_SCL
=I2C_ALS_SDA

GPU Temp (Int)
GK107: U8400
(Write: 0x9E Read: 0x9F)
GPU_SMB_CLK_R
GPU_SMB_DAT_R

Need to check with SMC team

SMC "2" SMBUS CONNECTIONS

NOTE: SMC RMT bus remains powered and may be active in S3 state

=PP3V3_S3_SMBUS_SMC_2_S3

SMC
U5000
(MASTER)
SMB_2_S3_CLK
SMB_2_S3_DATA

R5370 1K 5% 1/20W MF 201
R5371 1K 5% 1/20W MF 201

Trackpad
J4801
(Write: 0x90 Read: 0x91)
=I2C_TPAD_SCL
=I2C_TPAD_SDA

SMBUS_SMC_2_S3_SCL
SMBUS_SMC_2_S3_SDA

SMC "1" SMBUS CONNECTIONS

=PP3V3_S0_SMBUS_SMC_1_S0

SMC
U5000
(MASTER)
SMB_1_S0_CLK
SMB_1_S0_DATA

R5360 1K 5% 1/20W MF 201
R5361 1K 5% 1/20W MF 201

CPU/DDR3/PCH/AIRFLOW TEMP
EMC1414-A: U5870
(Write: 0x98 Read: 0x99)
=I2C_CPUTHMSNS_SCL
=I2C_CPUTHMSNS_SDA

SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA

X29 TEMP
TMP105: U5823
(WRITE: 0X92 READ: 0X93)
=I2C_X29THMSNS_SCL
=I2C_X29THMSNS_SDA

SMC "5" SMBUS CONNECTIONS

=PP3V42_G3H_SMBUS_SMC_5

SMC
U5000
(MASTER)
SMB_5_CLK
SMB_5_DATA

R5380 2.0K 5% 1/20W MF 201
R5381 2.0K 5% 1/20W MF 201

Battery Charger
ISL6258 - U7100
(Write: 0x12 Read: 0x13)
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA

Battery
J7050
(Write: 0x16 Read: 0x17)
=SMBUS_BATT_SCL
=SMBUS_BATT_SDA

SMBUS_SMC_5_G3_SCL
SMBUS_SMC_5_G3_SDA

SMC "4" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

SMC "3" SMBUS CONNECTIONS

SMC
U5000
(MASTER)
Unused

=PP3V3_S0_DPMUXI2C

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_A_SCL
=I2C_DPMUX_A_SDA

R5336 4.7K 5% 1/16W MF-LF 402
R5337 4.7K 5% 1/16W MF-LF 402

I2C_DPMUX_A_SCL
I2C_DPMUX_A_SDA

=PP3V3_S0_DPMUXI2C

LED BACKLIGHT SMBUS CONNECTION

DPMUX IC
U9100
(MASTER)
=I2C_DPMUX_UC_SCL
=I2C_DPMUX_UC_SDA

R5334 4.7K 5% 1/20W MF 201
R5335 4.7K 5% 1/20W MF 201

LED BACKLIGHT
U7100
(WRITE: 0x58 READ: 0x59)
=I2C_BKL_1_SCL
=I2C_BKL_1_SDA

I2C_DPMUX_UC_SCL
I2C_DPMUX_UC_SDA

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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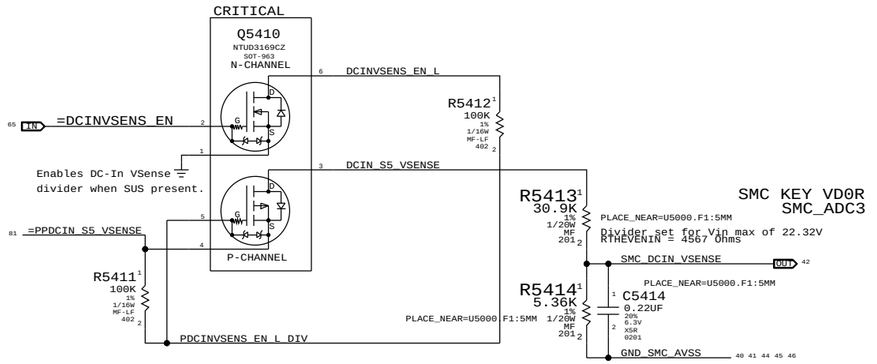
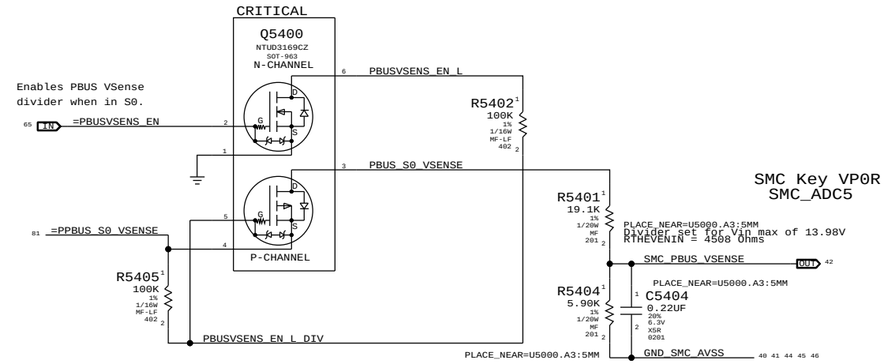
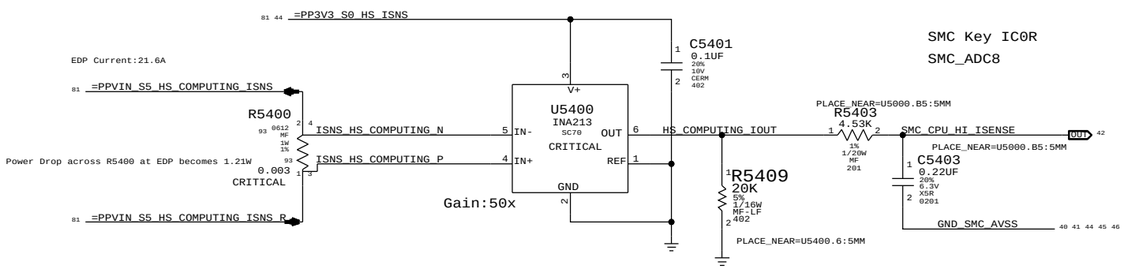
DC-In Voltage Sense Enable & Filter



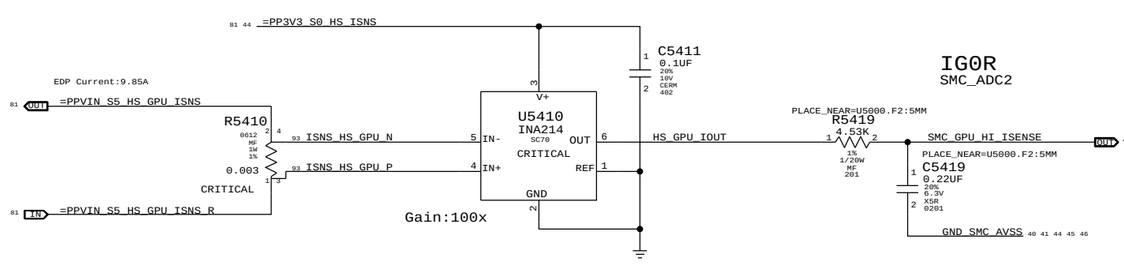
PBUS Voltage Sense Enable & Filter



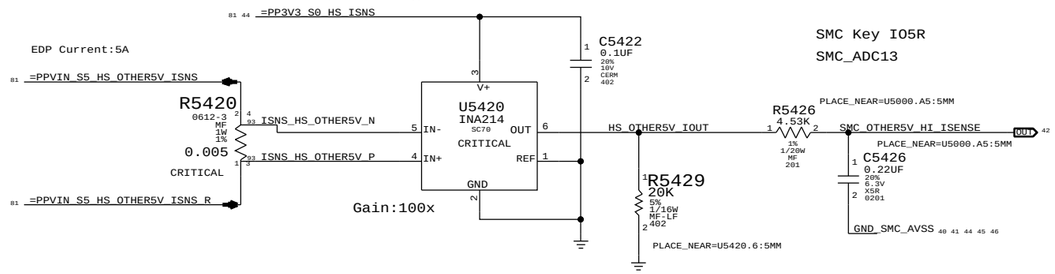
COMPUTING High Side Current Sense / Filter



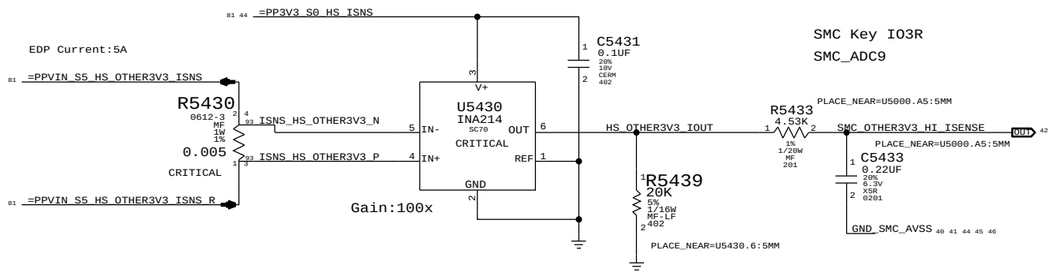
GRAPHICS High Side Current Sense / Filter



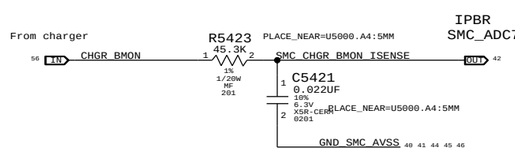
OTHERS (5V) High Side Current Sense / Filter



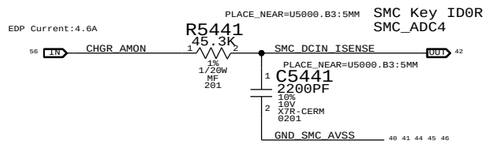
OTHERS (3.3V) High Side Current Sense / Filter



CHARGER BMON HIGH SIDE (BATTERY DISCHARGE) CURRENT SENSE & FILTER



DC-IN (AMON) Current Sense Filter



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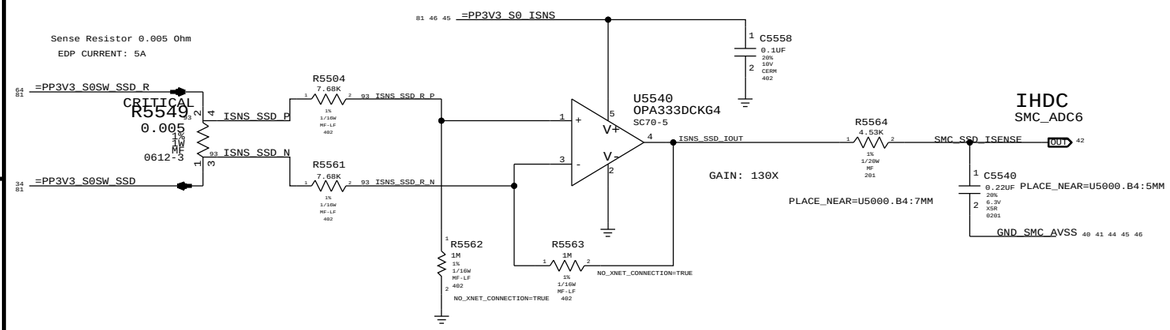
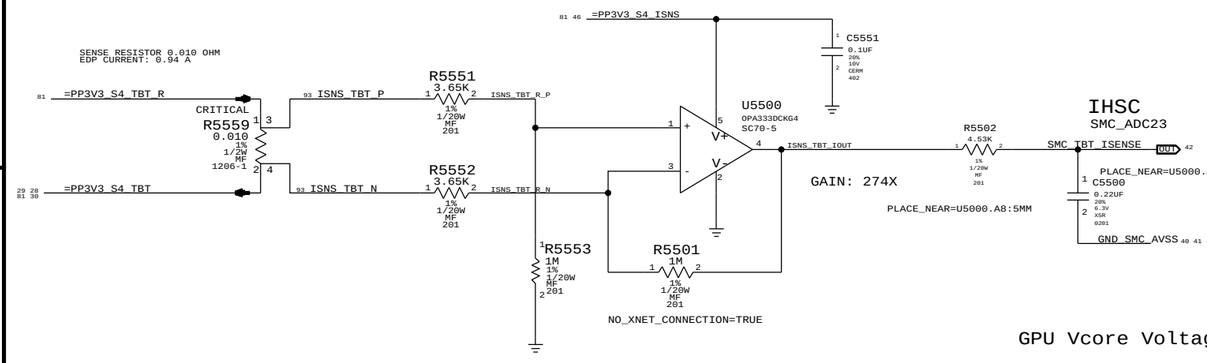
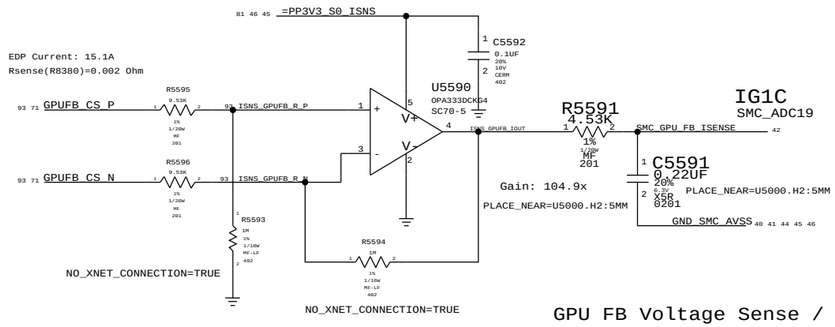
SSD CURRENT SENSE



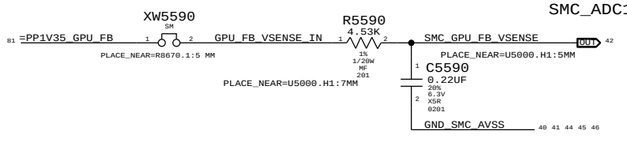
TBT Router CURRENT SENSE



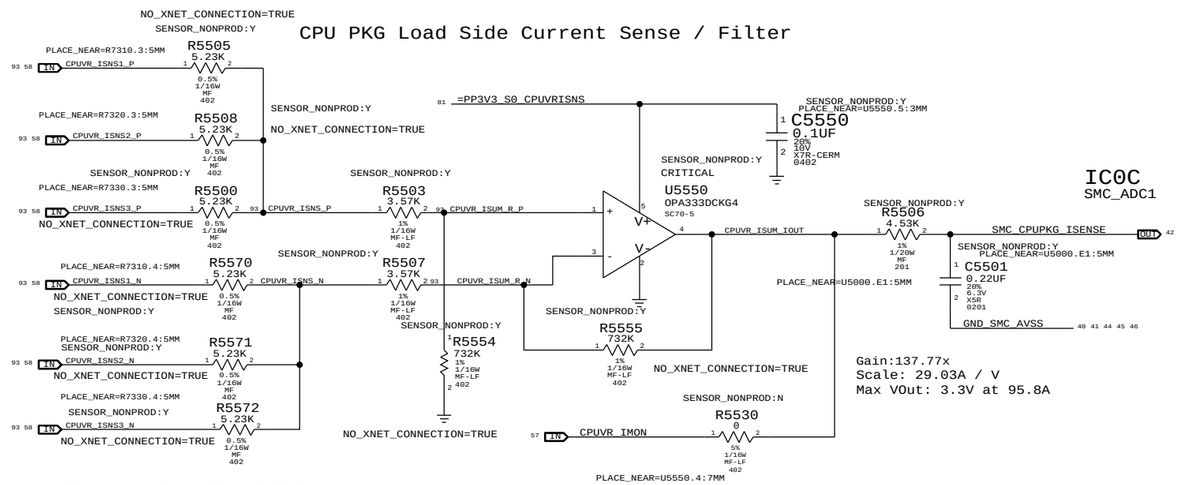
GPU FB (1.35V/1.5V) CURRENT SENSE



GPU FB Voltage Sense / Filter

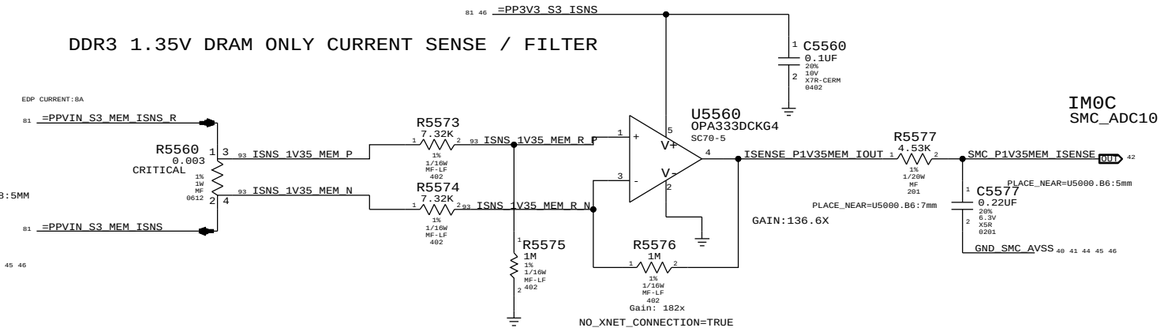


CPU PKG Load Side Current Sense / Filter

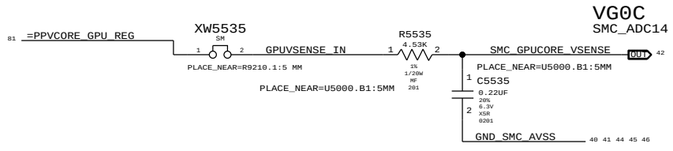


Individual Sense R is 0.75mOhm
EDP: 95A TDP :45A
(Effective Sense R is 0.25mOhm due to summing of the 3 phases)

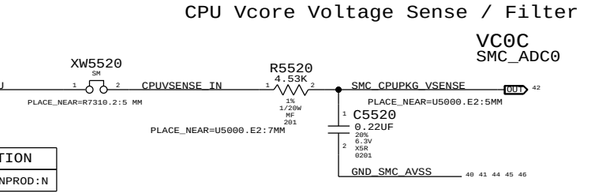
DDR3 1.35V DRAM ONLY CURRENT SENSE / FILTER



GPU Vcore Voltage Sense / Filter



CPU Vcore Voltage Sense / Filter



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0201	1	RES,MTL FILM,0,5,1/20W,0201,SMD,LF	R5506		SENSOR_NONPROD:N

removed LCD BKLT Voltage Sensing

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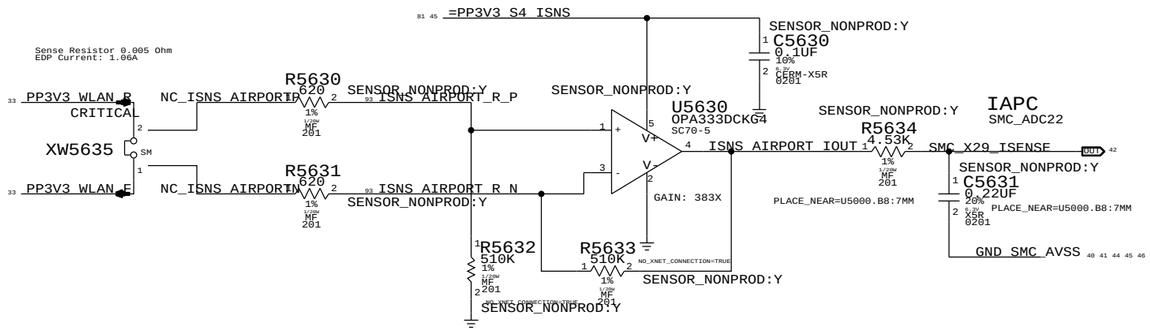
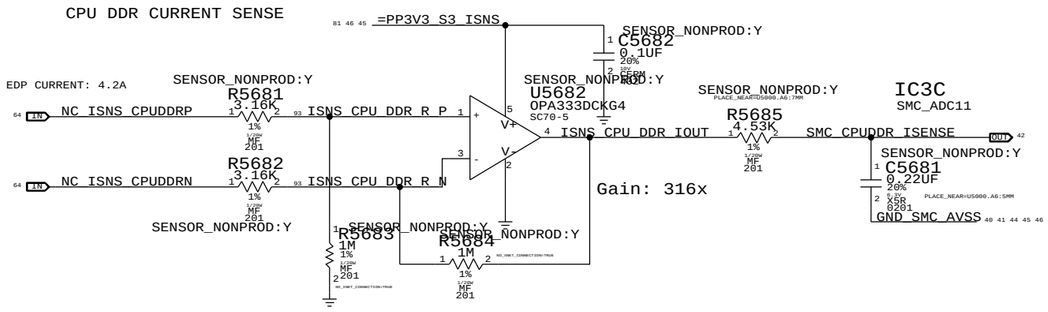
X29 AIRPORT CURRENT SENSE



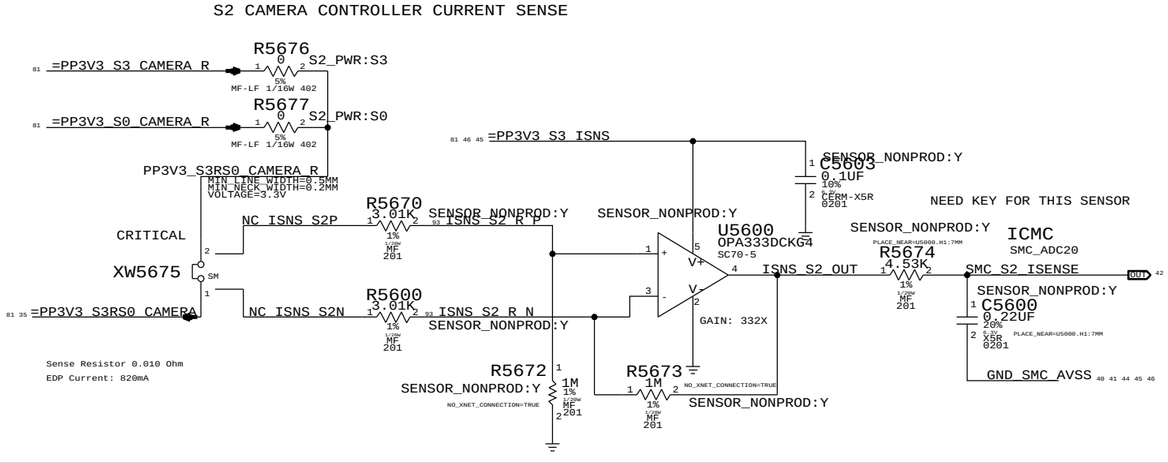
C5601,C5631,C5600,C5681,C5671,C5618,C5642

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	7	RES,MTL FILM,100K,5,1/20W,0201,SMD,LF			SENSOR_NONPROD:N

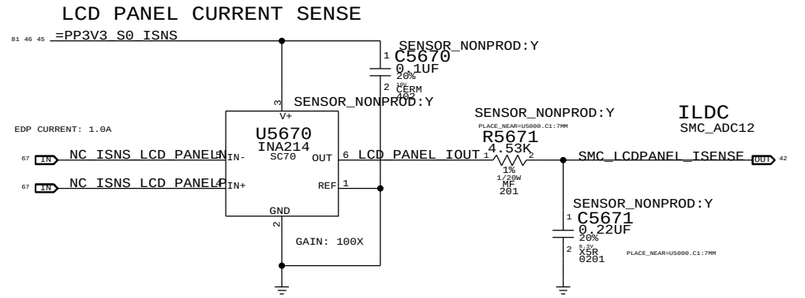
CPU DDR CURRENT SENSE



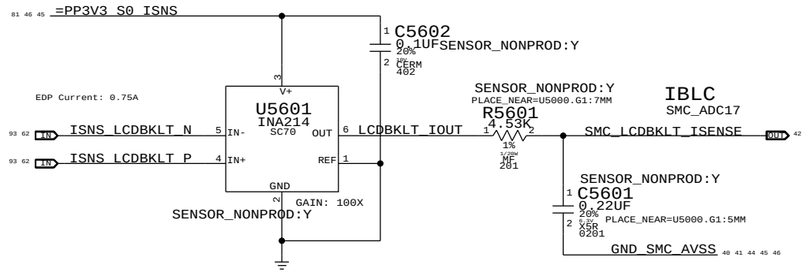
S2 CAMERA CONTROLLER CURRENT SENSE



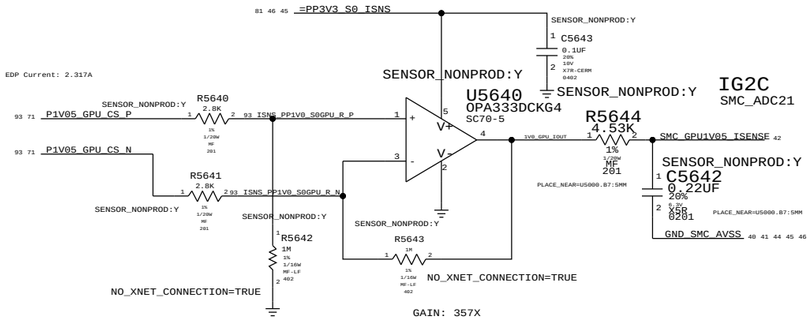
LCD PANEL CURRENT SENSE



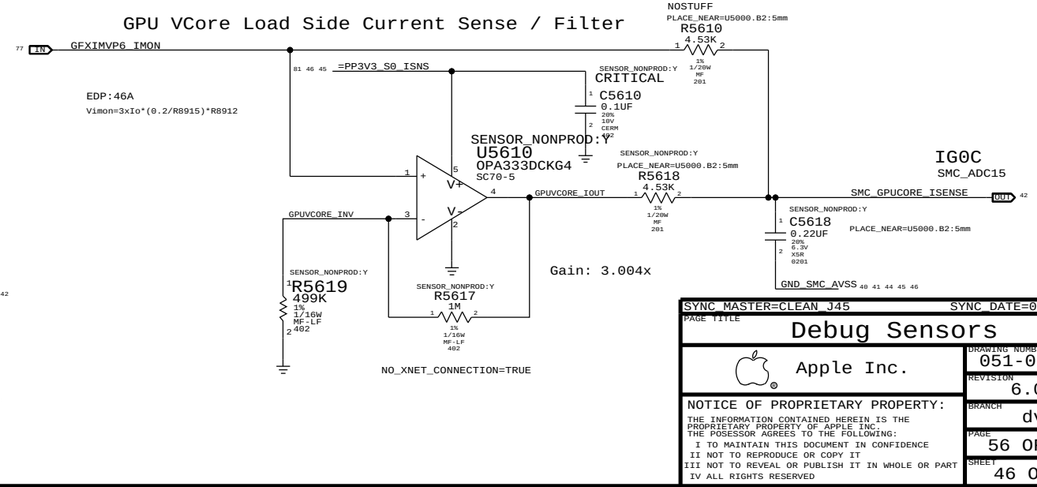
LCD BKLT Current Sense



GPU 1.05V CURRENT SENSE



GPU VCore Load Side Current Sense / Filter



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Debug Sensors

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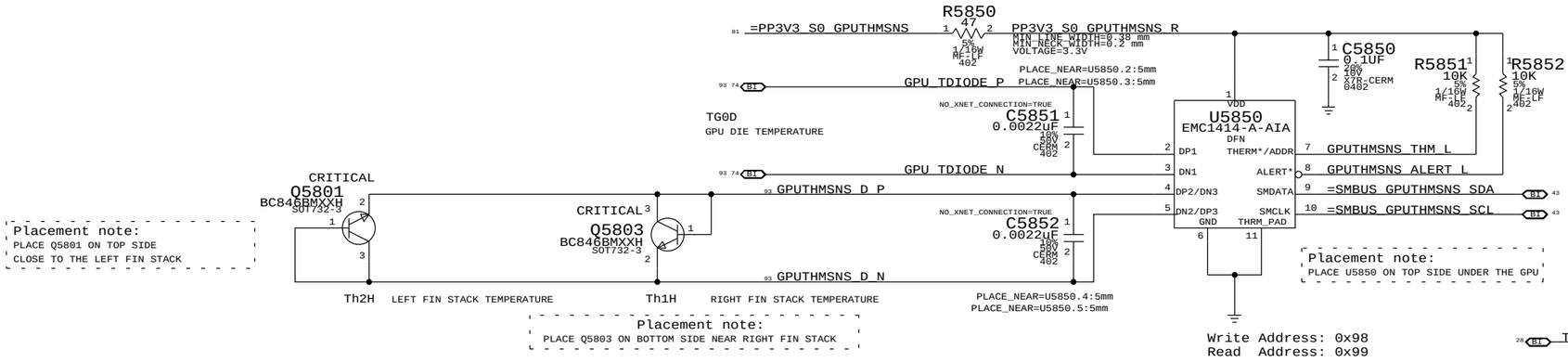
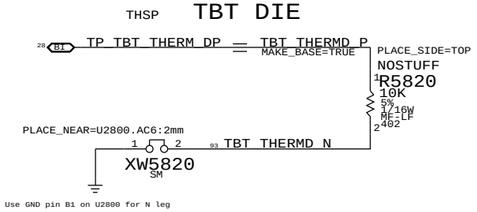
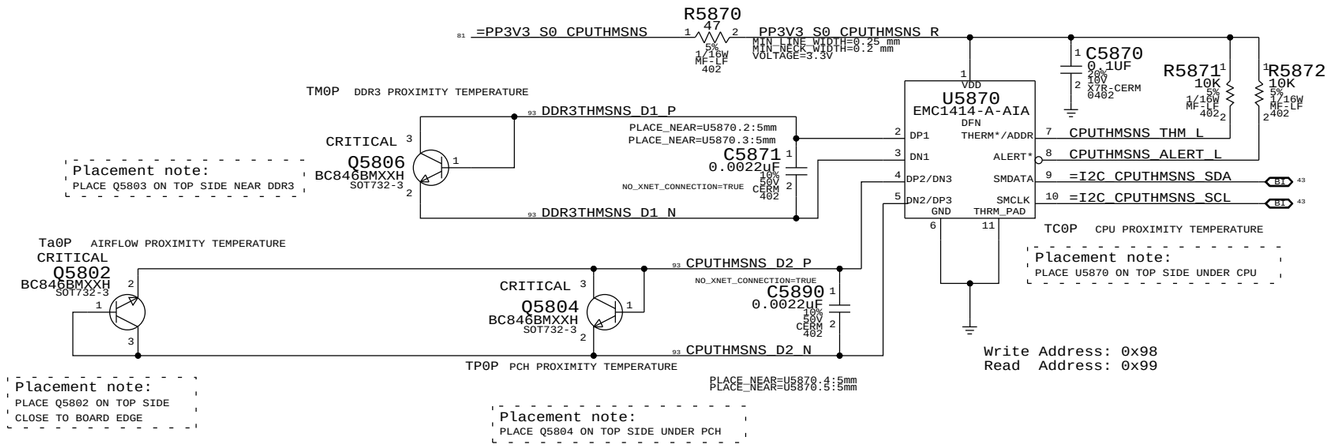
GPU PROXIMITY/GPU DIE/LEFT FIN STACK/RIGHT FIN STACK



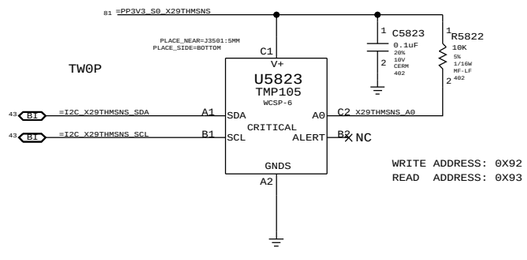
TBT DIE



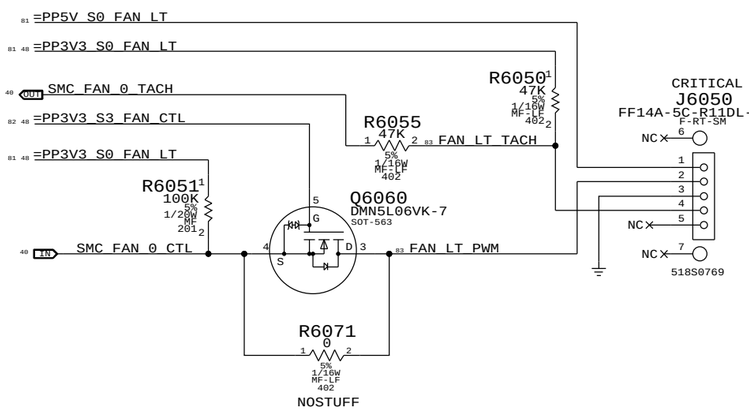
DDR3 PROXIMITY/CPU PROXIMITY/PCH PROXIMITY/AIRFLOW PROXIMITY



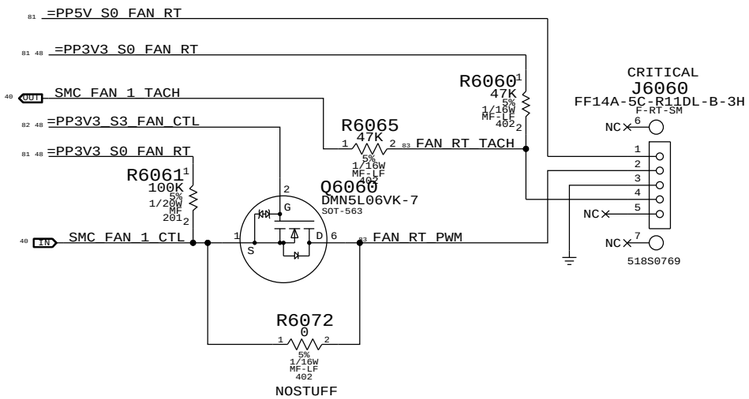
X29 PROXIMITY



Left Fan



Right Fan



SYNC_MASTER=CLEAN_J45 SYNC_DATE=06/23/2013

PAGE TITLE: Fan Connectors

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

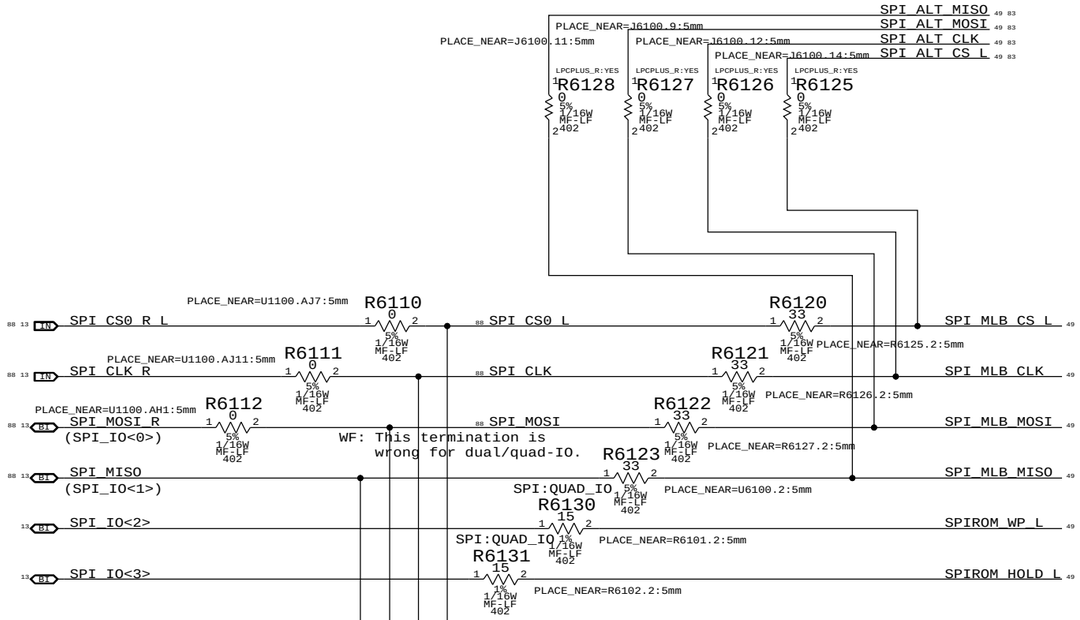
REVISION: 6.0.0

BRANCH: dvt

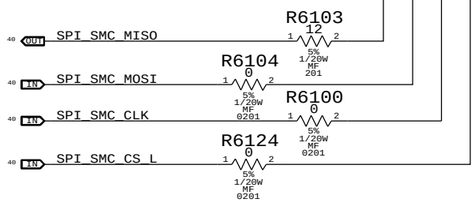
PAGE: 60 OF 119

SHEET: 48 OF 94

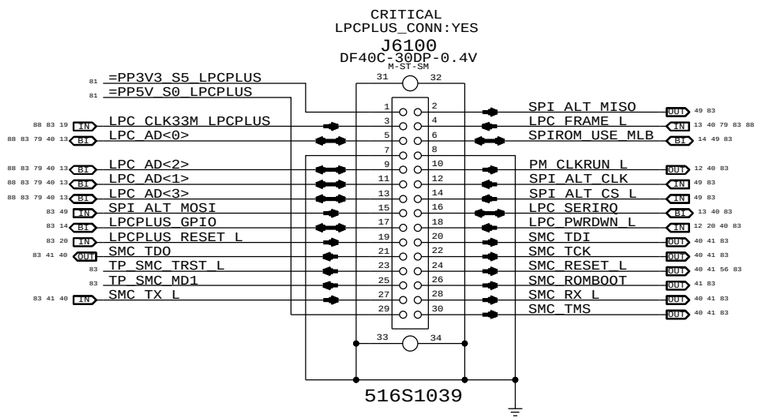
SPI Bus Series Termination



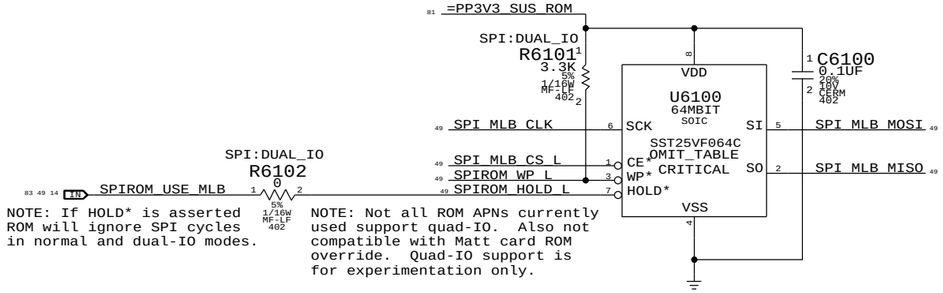
SMC12 SPI SUPPORT



LPC+SPI Connector



SPI ROM



NOTE: If HOLD* is asserted ROM will ignore SPI cycles in normal and dual-IO modes.

NOTE: Not all ROM APNs currently used support quad-IO. Also not compatible with Matt card ROM override. Quad-IO support is for experimentation only.

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: SPI ROM / LPC+SPI Conn.

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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BRANCH: dvt

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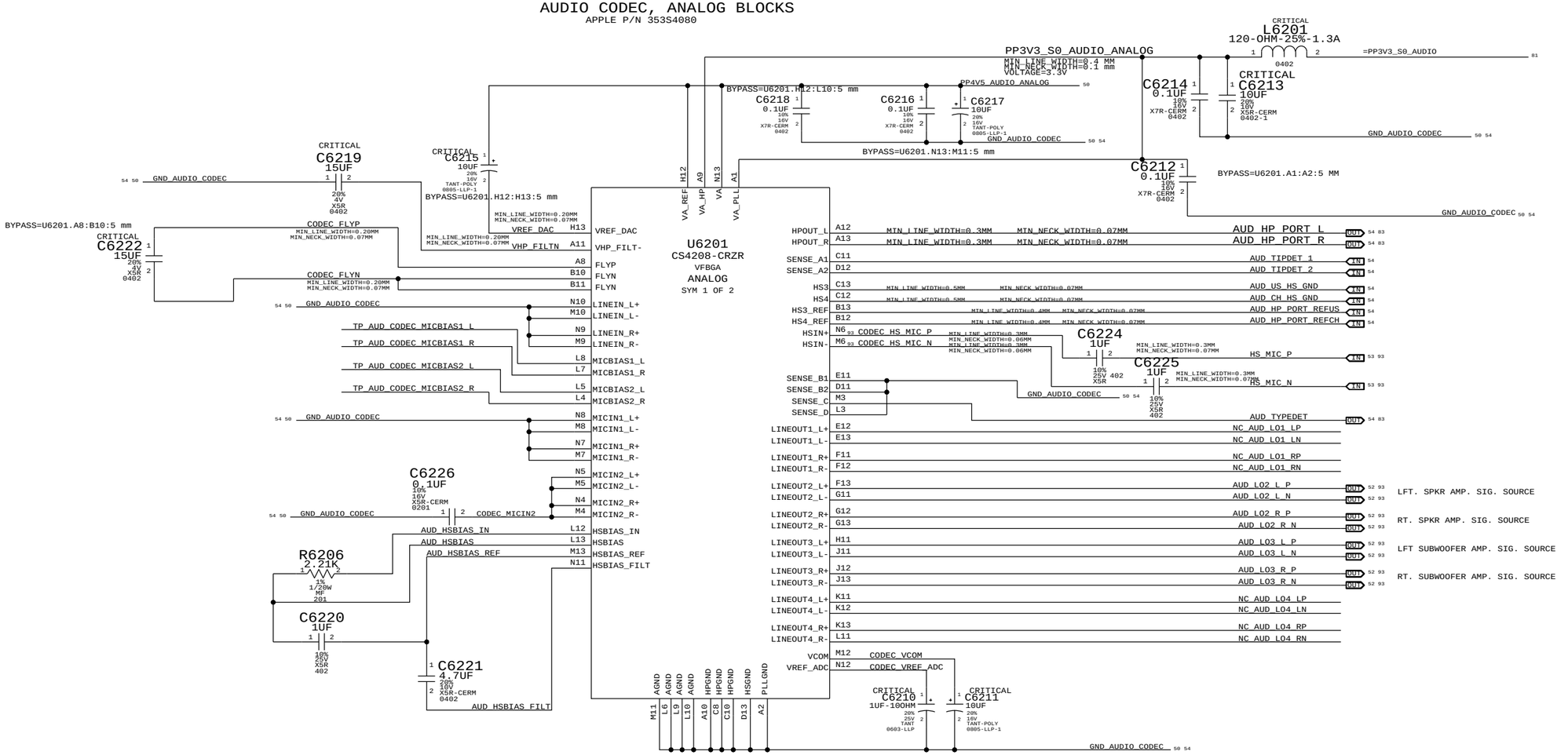
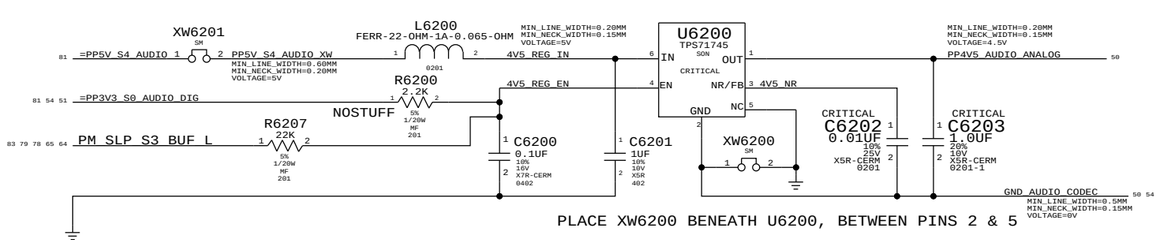
AUDIO CODEC, ANALOG BLOCKS

APPLE P/N 353S4080



4.5V POWER SUPPLY FOR CODEC

APPLE P/N 353S2456



SYNC_MASTER=CLEAN_J45	SYNC_DATE=04/26/2013
PAGE TITLE	AUDIO:CODEC, ANALOG
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
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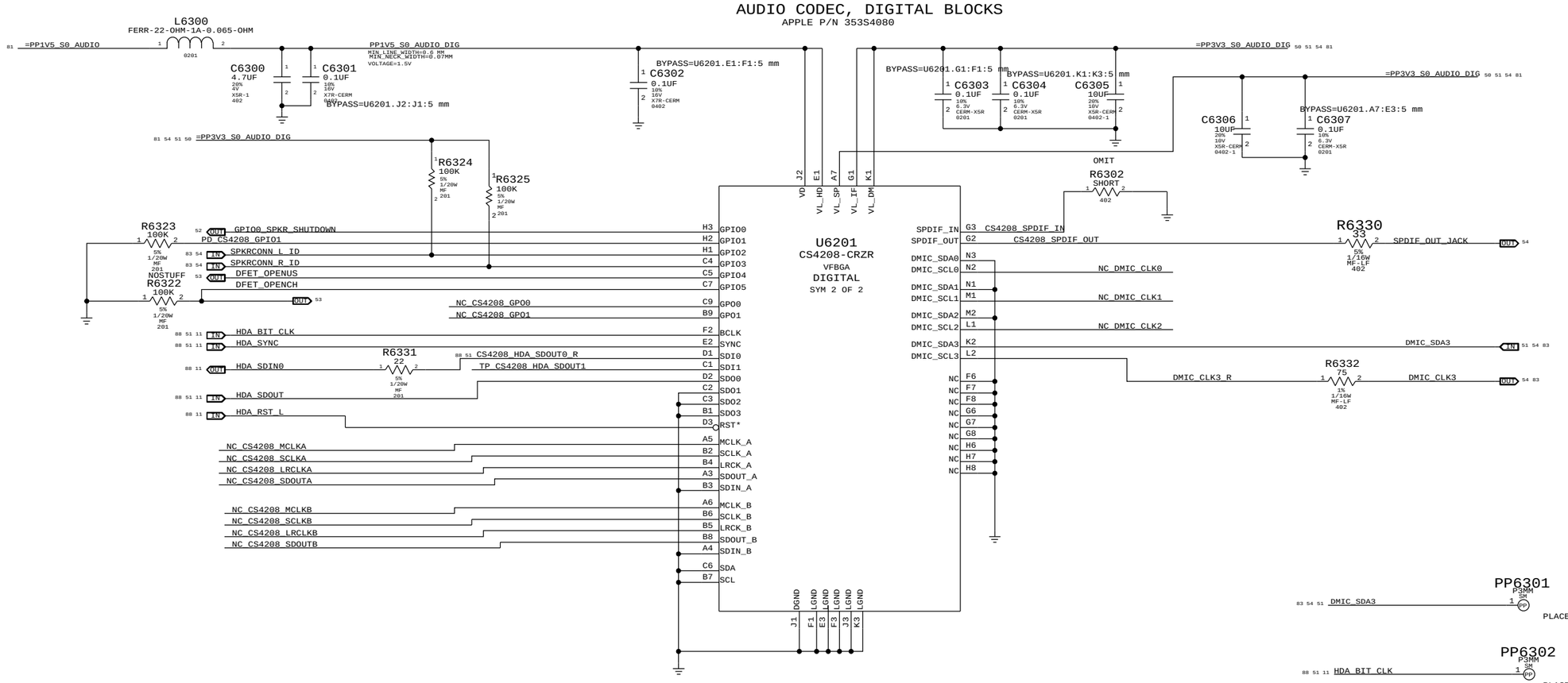
AUDIO CODEC, DIGITAL BLOCKS

APPLE P/N 353S4080



PP6301
P3MMSM
DMIC_SDA3
PLACE_NEAR=U6201.N3:5 mm

PP6302
P3MMSM
HDA_BIT_CLK
PLACE_NEAR=U6201.F2:5 mm

PP6303
P3MMSM
HDA_SYNC
PLACE_NEAR=U6201.E2:5 mm

PP6304
P3MMSM
HDA_SDOUT
PLACE_NEAR=U6201.D2:5 mm

PP6305
P3MMSM
CS4208_HDA_SDOUT0_R
PLACE_NEAR=U6201.D1:5 mm

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
AUDIO:CODEC, DIGITAL

Apple Inc.

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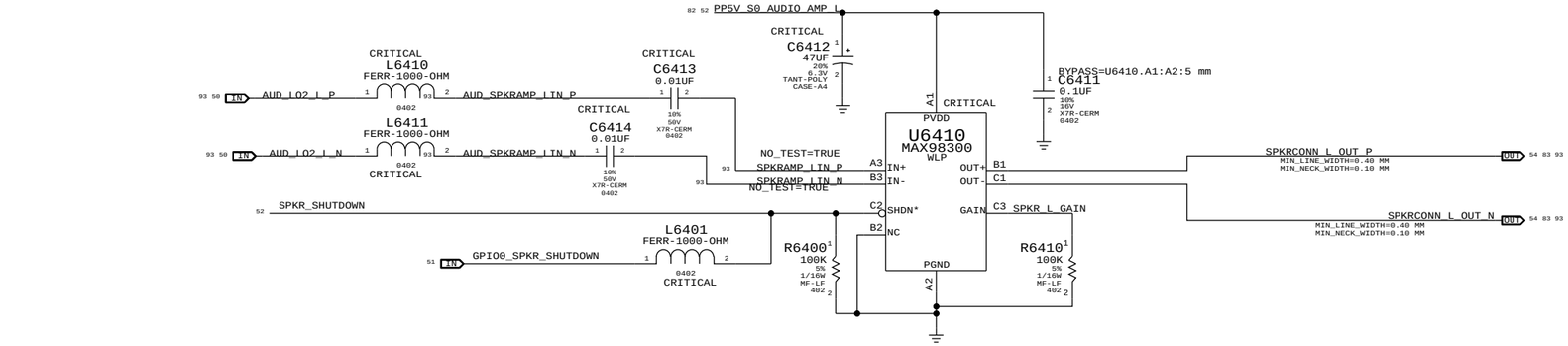
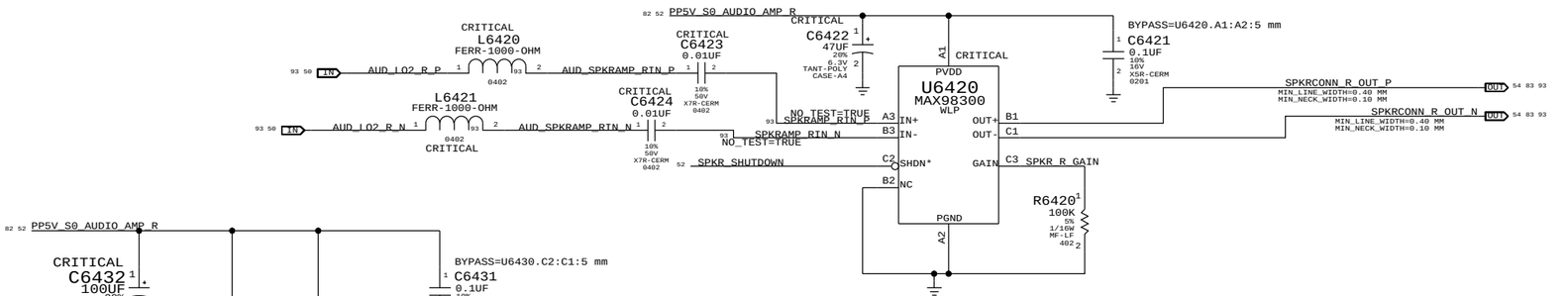
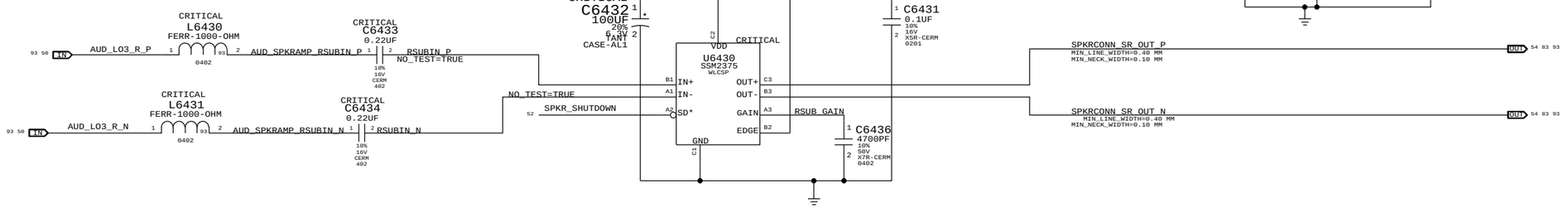
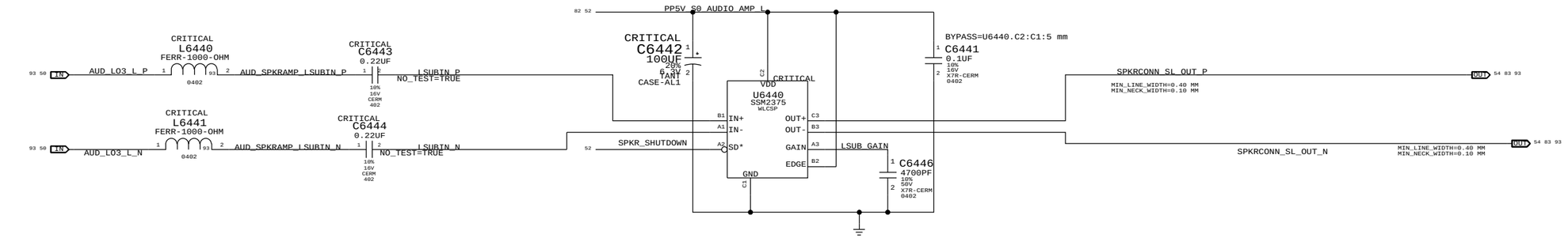
4X MONO SPEAKER AMPLIFIERS (MAX98300 & SSM2375)
APN: 353S2888 & 353S2958
GAIN = +3 DB
1ST ORDER FC (L&R) = NOM 569 HZ
1ST ORDER FC (SUB) = NOM 9 HZ









SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO: SPEAKER AMP

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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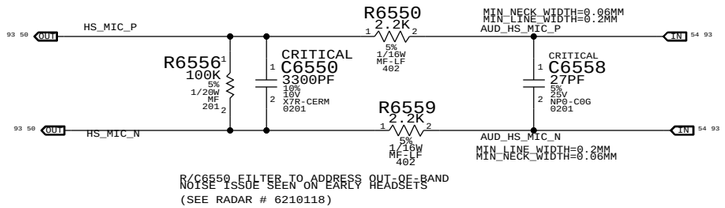

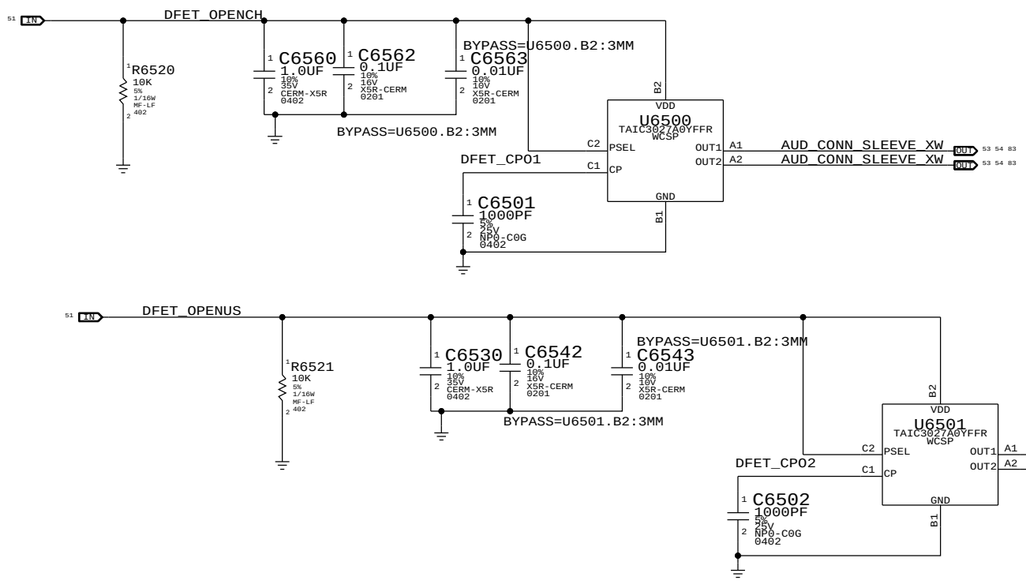

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: AUDIO: JACK

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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CODEC OUTPUT SIGNAL PATHS

FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL
HP/HS OUT	0X02 (2)	0X02 (2)	0X10 (16)	N/A
TWEETERS	0X03 (3)	0X03 (3)	0X12 (18)	CODEC GPIO0
SUB	0X04 (4)	0X04 (4)	0X13 (19)	CODEC GPIO0
SPDIF OUT	N/A	0X0E (14)	0X21 (33)	N/A

CODEC INPUT SIGNAL PATHS

FUNCTION	CONVERTER	PIN COMPLEX	VREF
DMIC 1	0X09 (9)	0X1C (28)	3.3V
DMIC 2	0X09 (9)	0X1C (28)	3.3V
HEADSET MIC	0X07 (7)	0X18 (24)	2.7V

OTHER CODEC GPIO LINES

LEFT SPEAKER ID	GPIO2	INPUT	HIGH = FG, LOW = MERRY
RIGHT SPEAKER ID	GPIO3	INPUT	HIGH = FG, LOW = MERRY
DFET CONTROL	GPIO4	OUTPUT	HIGH = DFETs OPEN

2-MIC CONNECTOR
APN: 518S0769

J6601
FF14A-5C-R11DL-B-3H
F-RT-SM

81 54 51 50 =PP3V3_S0_AUDIO_DIG
83 51 OUT DMIC_SDA3
83 51 OUT DMIC_CLK3
OMIT
R6680
SHORT
402
83 DMIC_SDA2

SPEAKER CONNECTOR HP=80HZ
APN: 518S0672

CRITICAL
J6602
78171-6006
M-RT-SM

93 83 52 IN SPKRCONN_L_OUT_P
93 83 52 IN SPKRCONN_L_OUT_N
83 51 IN SPKRCONN_L_ID
93 83 52 IN SPKRCONN_SL_OUT_P
93 83 52 IN SPKRCONN_SL_OUT_N

CRITICAL
J6603
78171-6006
M-RT-SM

93 83 52 IN SPKRCONN_R_OUT_P
93 83 52 IN SPKRCONN_R_OUT_N
83 51 IN SPKRCONN_R_ID
93 83 52 IN SPKRCONN_SR_OUT_P
93 83 52 IN SPKRCONN_SR_OUT_N

CRITICAL L6611 120-OHM-25%-1.3A 0402
50 OUT AUD_HP_PORT_REFCH
AUD_CONN_SLEEVE
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.3:2.54mm
XW6600 SM
CRITICAL L6612 120-OHM-25%-1.3A 0402
83 53 AUD_CONN_SLEEVE_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
50 OUT AUD_CH_HS_GND
XW6601 SM
93 53 OUT AUD_HS_MIC_P

CRITICAL L6613 120-OHM-25%-1.3A 0402
50 OUT AUD_HP_PORT_REFUS
AUD_CONN_RING2
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.06MM
PLACE_NEAR=J6600.5:2.54mm
XW6602 SM
CRITICAL L6614 120-OHM-25%-1.3A 0402
53 AUD_CONN_RING2_XW
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.1MM
50 OUT AUD_US_HS_GND
XW6603 SM
93 53 OUT AUD_HS_MIC_N

CRITICAL L6604 120-OHM-25%-1.3A 0402
83 50 IN AUD_HP_PORT_L
AUD_CONN_HP_LEFT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
R6602 2.2K 5% 1/20W MF 201
CRITICAL L6608 FERR-470-OHM 0201
50 OUT AUD_TIPDET_2
AUD_CONN_TIPDET_2
50 GND_AUDIO_CODEC
R6603 2.2K 5% 1/20W MF 201
CRITICAL L6607 FERR-470-OHM 0201
50 OUT AUD_TIPDET_1
AUD_CONN_TIPDET_1
CRITICAL L6605 120-OHM-25%-1.3A 0402
83 50 IN AUD_HP_PORT_R
AUD_CONN_HP_RIGHT
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.06MM
CRITICAL L6606 FERR-470-OHM 0201
83 50 OUT AUD_TYPEDET
AUD_CONN_TYPEDET
51 IN SPDIF_OUT_JACK
81 54 51 50 =PP3V3_S0_AUDIO_DIG

APN: 514-0875

J6600
AUDIO-SPDIF-J44
F-RT-TH

5 MIC
6 AUDIO GND
2 2RTN
1 DET2
8 DET1
NC
7 1RTN
3 R.AUDIO
4 AUDIO GND
AUDIO
9 VIN
10 VDD
11 GND
OPERATING VOLTAGE 3.3
POF
12 13 14 15 SHELL PINS

C6600 1UF 10% 10V X5R 402-1
C6601 0.1UF 10% 6.3V CERM-X5R 0201

R6601 10K 5% 1/16W MF-LF 402

CRITICAL DZ6607 ESDALC5-1BM2 SOD882
C6602 100PF 5% 25V NP0-CERM 0201
CRITICAL DZ6601 ESDALC5-1BM2 SOD882
C6603 100PF 5% 25V NP0-CERM 0201
C6604 100PF 5% 25V NP0-CERM 0201
CRITICAL DZ6602 ESDALC5-1BM2 SOD882
C6605 100PF 5% 25V NP0-CERM 0201
CRITICAL DZ6603 ESDALC5-1BM2 SOD882
C6606 100PF 5% 25V NP0-CERM 0201
CRITICAL DZ6606 ESDALC5-1BM2 SOD882
CRITICAL DZ6605 ESDALC5-1BM2 SOD882
C6607 100PF 5% 25V NP0-CERM 0201
C6608 100PF 5% 25V NP0-CERM 0201
CRITICAL DZ6604 ESDALC5-1BM2 SOD882

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE
AUDIO: JACK TRANSLATORS

Apple Inc.

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MagSafe DC Power Jack

CRITICAL
J7000
WTB-PWR-M82
M-RT-SM
518S0508

83 PP20V_DCIN_FUSE
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=20V

CRITICAL
F7005
6AMP-32V-0.00950HM
0603

=PP20V_DCIN_CONN 81

NOSTUFF
C7005
0.01UF
20% 50V CERM 0603

TP_TDM_ONEWIRE_MPM

=PP3V42_G3H_ONEWIREPROT 81

C7008
0.1UF
20% 10V CERM 402
PLACEMENT_NOTE=PLACE NEAR U7100 and U7001

CRITICAL
U7001
TC7SZ08FEAPE
SOT665

SMC_BC_ACOK_VCC

SMC_BC_ACOK
IN 40 41 42

C7000
0.1UF
20% 10V CERM 402

R7029
2.0K
5% 1/16W MF-LF 402

U7000
MAX9940
SC70-5
CRITICAL
VCC
EXT
INT
NC GND
NC

83 ADAPTER_SENSE

SYS_ONEWIRE
B1 40

1-Wire OverVoltage Protection

The chassis ground will otherwise float and can send transients onto ADAPTER_SENSE when AC is connected.

R7012
22.1K
1% 1/20W MF 201

Input impedance of 22.1K meets sparkitecture requirements for D2 design only

Q7010
SI5419DU
POWERPAK

R7010
100K
5% 1/20W MF 201

C7012
0.047UF
10% 25V X5R 0402

R7011
10K
5% 1/20W MF 201

When input voltage is 2V the FET will be off blocking the leakage path and 22.1K can be properly detected.

When input voltage is at 16V+, FET will conduct and power charger and 3.42V reg

DCIN_ISOL_GATE_R

DCIN_ISOL_GATE

81 =PP20V_DCIN_ISOL

D7010
CDZ6.8B
SM
6.8V Zener

R7020
47
5% 1/3W MF 805

PP20V_DCIN_CONN_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V

CRITICAL
D7005
BAT30CWFILM
SOT-323

R7005
10
5% 1/8W MF-LF 805

81 56 =PPBUS_G3H

PPBUS_G3H_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=18.5V

PPVIN_G3H_P3V42G3H
MIN_LINE_WIDTH=0.4 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=20V

APN:353S3733
3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator

C7090 4.7UF 10% 25V X5R-CERM 0603
C7091 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7092 4.7UF 10% 25V X5R-CERM 0603
C7093 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7096 4.7UF 10% 25V X5R-CERM 0603
NOSTUFF C7097 4.7UF 10% 25V X5R-CERM 0603

R7001
0
5% 1/20W MF 0201

P3V42G3H_SHDN_L

U7090
LT3470AED
DFN
VIN BOOST SW BIAS FB GND THRM PAD
SHDN* NC NC

P3V42G3H_BOOST
DIDT=TRUE

C7094
0.22UF
10% 10V CERM 402

CRITICAL
L7095
33UH-20%-0.39A-0.435OHM
DP418C-SM

P3V42G3H_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
DIDT=TRUE

=PP3V42_G3H_REG 81

Vout = 3.425V
300MA MAX OUTPUT
(Switcher limit)

C7095
22PF
5% 50V NPO-C0G-CERM 0201

P3V42G3H_FB

<Ra>
R7095
348K
1% 1/20W MF 201

<Rb>
R7096
200K
1% 1/20W MF 201

C7099
22UF
20% 6.3V X5R-CERM-1 603

Vout = 1.25V * (1 + Ra / Rb)

OMIT
C7001
NOSTUFF
NONE NONE NONE 402

NOSTUFF
R7002
49.9K
1% 1/20W MF 201

BATTERY CONNECTOR

518-0376
CRITICAL
J7050
BAT-J5
F-ST-TH
VER 1

12	POS	1	
13	POS	2	
14	POS	3	
15	POS	4	
NC			
NC			
16	SCL	5	=SMBUS_BATT_SCL
17	SDA	6	=SMBUS_BATT_SDA
18	SYS_DETECT	7	SYS_DETECT_L
19	NEG	8	
20	NEG	9	
21	NEG	10	
22	NEG	11	

83 56 PPVBAT_G3H_CONN

C7050 0.1UF 10% 25V X5R 402
C7060 1UF 10% 25V X5R 603-1

CRITICAL
D7050
RCLAMP2402B
SC-75

R7050
10K
5% 1/10W MF-LF 402

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013
PAGE TITLE
DC-In & Battery Connectors
Apple Inc.
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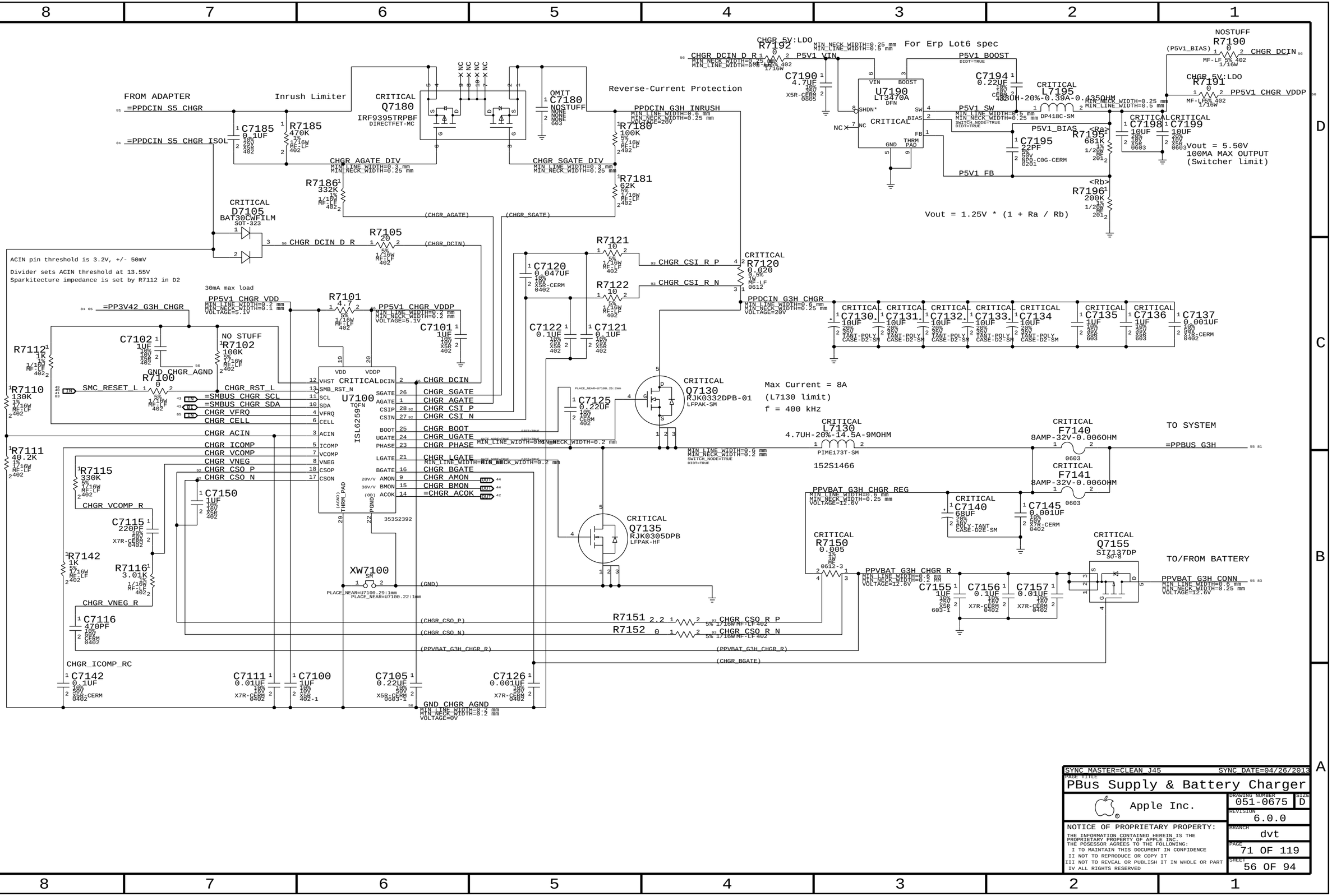
FROM ADAPTER
=PPDCIN_S5_CHGR
=PPDCIN_S5_CHGR_ISOL
Inrush Limiter
CRITICAL
Q7180
IRF9395TRPBF
DIRECTFET-MC
OMIT
C7180
NOSTUFF
Reverse-Current Protection
PPDCIN_G3H_INRUSH
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V
R7180
100K
R7185
470K
C7185
0.1UF
CHGR_AGATE_DIV
CHGR_SGATE_DIV
R7186
332K
R7181
62K
CRITICAL
D7105
BAT30CWFILM
SOT-323
CHGR_DCIN_D_R
R7105
20
(CHGR_DCIN)
(CHGR_AGATE)
(CHGR_SGATE)
ACIN pin threshold is 3.2V, +/- 50mV
Divider sets ACIN threshold at 13.55V
Sparkitecture impedance is set by R7112 in D2
30mA max load
=PP3V42_G3H_CHGR
PP5V1_CHGR_VDD
PP5V1_CHGR_VDDP
R7101
4.7
C7101
1UF
C7102
1UF
NO STUFF
R7102
100K
R7112
1K
GND_CHGR_AGND
R7100
0
R7110
130K
SMC_RESET_L
CHGR_RST_L
=SMBUS_CHGR_SCL
=SMBUS_CHGR_SDA
CHGR_VFRQ
CHGR_CELL
CHGR_ACIN
CHGR_ICOMP
CHGR_VCOMP
CHGR_VNEG
CHGR_CSO_P
CHGR_CSO_N
R7111
40.2K
R7115
330K
C7115
220PF
C7116
470PF
R7116
3.01K
R7142
1K
CHGR_VCOMP_R
CHGR_VNEG_R
CHGR_ICOMP_RC
C7150
1UF
C7142
0.1UF
C7111
0.01UF
C7100
1UF
C7105
0.22UF
C7126
0.001UF
GND_CHGR_AGND
U7100
ISL6259
TQFN
VHST
SMB_RST_N
SCL
SDA
VFRQ
CELL
ACIN
ICOMP
VCOMP
VNEG
CSOP
CSON
DCIN
SGATE
AGATE
CSIP
CSIN
BOOT
UGATE
PHASE
LGATE
BGATE
AMON
BMON
ACOK
VDD
VDDP
(AGND)
THRM_PAD
PGND
353S2392
XW7100
SM
(GND)
PLACE_NEAR=U7100.29:1mm
PLACE_NEAR=U7100.22:1mm
R7121
10
R7122
10
C7120
0.047UF
C7122
0.1UF
C7121
0.1UF
CHGR_CSI_R_P
CHGR_CSI_R_N
CRITICAL
R7120
0.020
PPDCIN_G3H_CHGR
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=20V
CRITICAL
Q7130
RJK0332DPB-01
LFPAK-SM
CRITICAL
Q7135
RJK0305DPB
LFPAK-HF
C7125
0.22UF
Max Current = 8A
(L7130 limit)
f = 400 kHz
CRITICAL
L7130
4.7UH-20%-14.5A-9MOHM
PIME173T-SM
152S1466
CRITICAL
F7140
8AMP-32V-0.006OHM
CRITICAL
F7141
8AMP-32V-0.006OHM
TO SYSTEM
=PPBUS_G3H
PPVBAT_G3H_CHGR_REG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
CRITICAL
C7140
68UF
C7145
0.001UF
CRITICAL
R7150
0.005
1%
1W
MF
0612-3
PPVBAT_G3H_CHGR_R
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=12.6V
C7155
1UF
C7156
0.1UF
C7157
0.01UF
CRITICAL
Q7155
SI7137DP
SO-8
TO/FROM BATTERY
PPVBAT_G3H_CONN
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.6V
R7151
2.2
R7152
0
CHGR_CSO_R_P
CHGR_CSO_R_N
(CHGR_CSO_P)
(CHGR_CSO_N)
(PPVBAT_G3H_CHGR_R)
(CHGR_BGATE)
CHGR_5V:LDO
R7192
0
CHGR_DCIN_D_R
P5V1_VIN
C7190
4.7UF
U7190
LT3470A
DFN
VIN
BOOST
SW
BIAS
FB
THRM
GND
PAD
SHDN*
NC
P5V1_BOOST
DIDT=TRUE
C7194
0.22UF
L7195
2.2UH-20%-0.39A-0.435OHM
P5V1_SW
DP418C-SM
SWITCH_NODE=TRUE
P5V1_BIAS
P5V1_FB
C7195
22PF
R7195
681K
<Ra>
R7196
200K
<Rb>
Vout = 1.25V * (1 + Ra / Rb)
For Erp Lot6 spec
NOSTUFF
R7190
0
(P5V1_BIAS)
CHGR_DCIN
CHGR_5V:LDO
R7191
0
P5V1_CHGR_VDDP
C7198
10UF
C7199
10UF
Vout = 5.50V
100MA MAX OUTPUT
(Switcher limit)
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
PBus Supply & Battery Charger
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
71 OF 119
SHEET
56 OF 94
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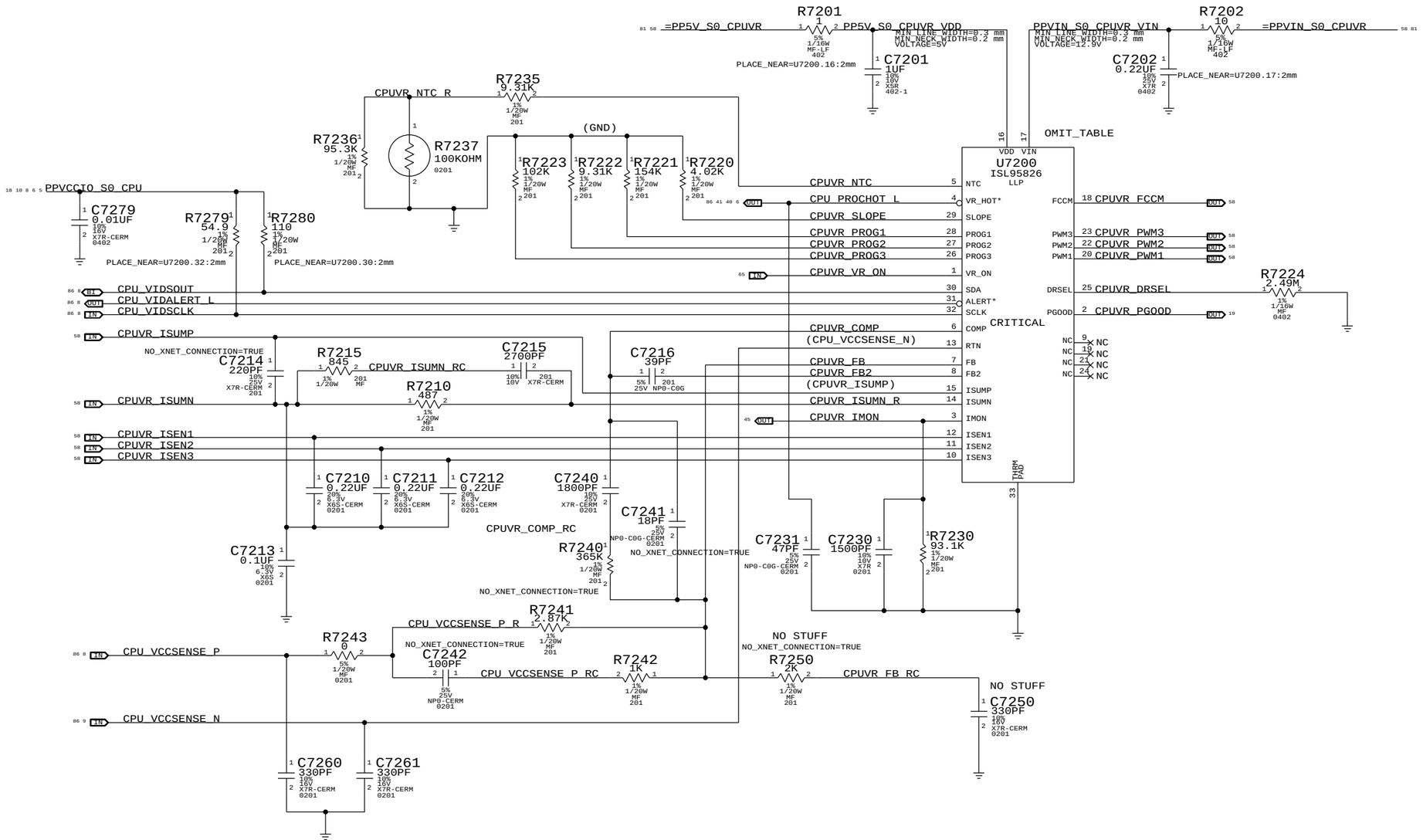
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S4170	1	IC,ISL95826R6200,PWM,PGOOD,SCREEN,32P,QFN	U7200	CRITICAL	



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
CPU VR12.5 VCC Regulator IC

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 72 OF 119
SHEET 57 OF 94

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU VR12.5 VCC Power Stage

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

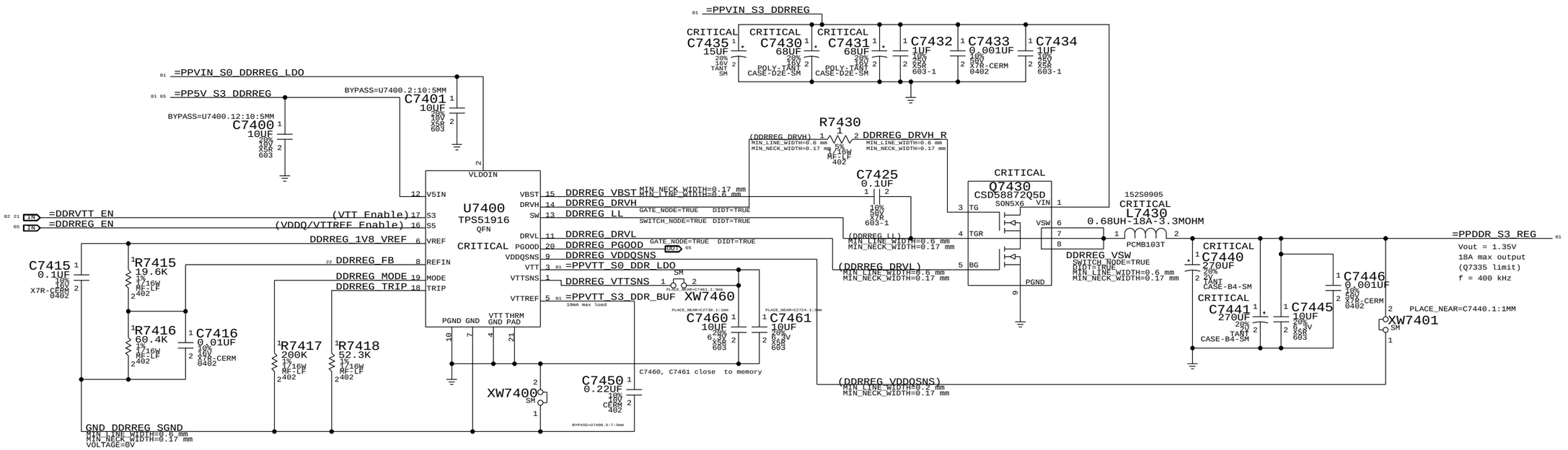
REVISION: 6.0.0

BRANCH: dvt

PAGE: 73 OF 119

SHEET: 58 OF 94

DDR3L (1V35 S3) REGULATOR



SYNC MASTER=CLEAN J45	SYNC DATE=04/26/2013
PAGE TITLE	1.35V DDR3L SUPPLY
Apple Inc.	DRAWING NUMBER 051-0675 · SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 74 OF 119
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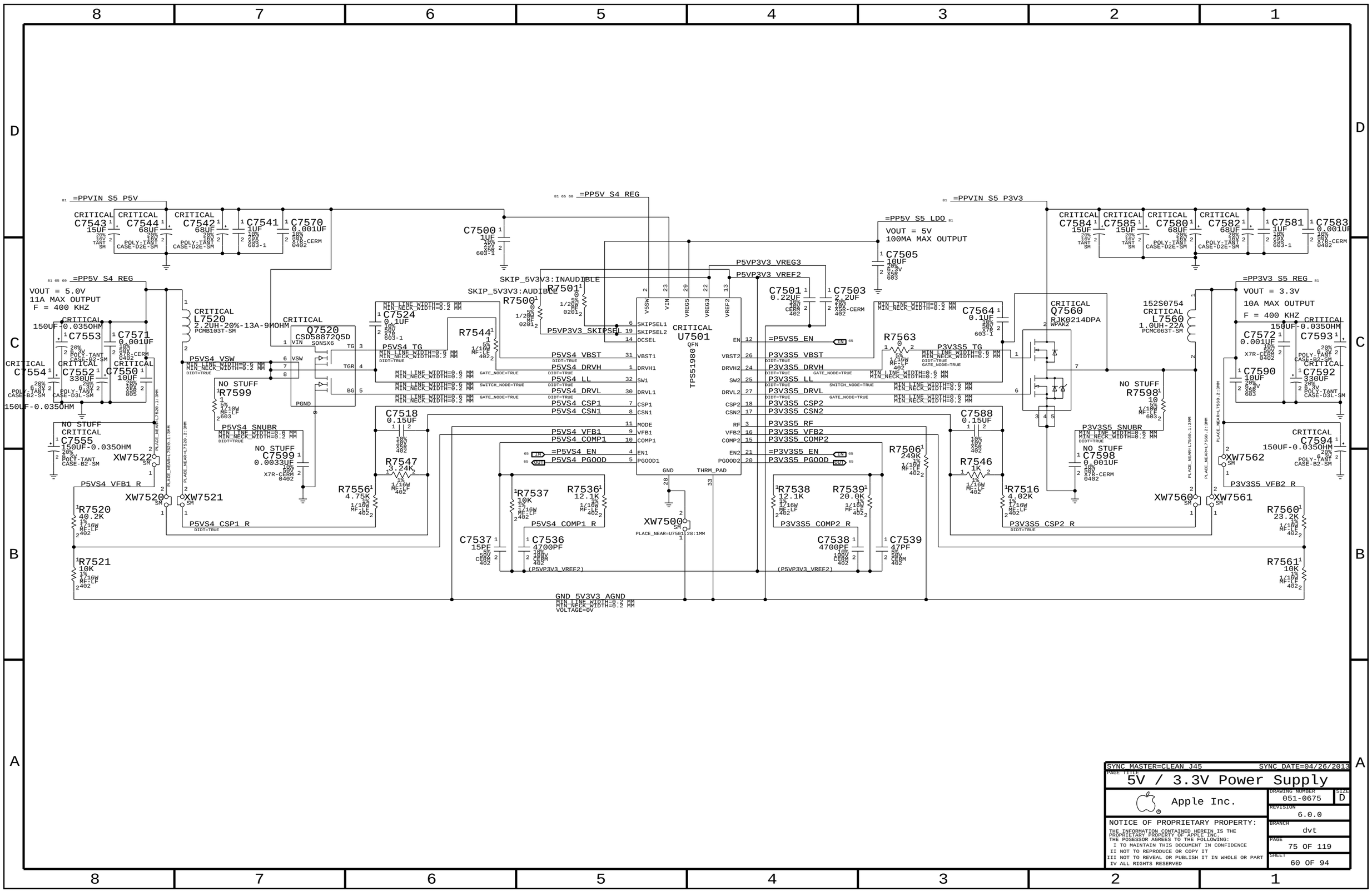
=PPVIN_S5_P5V
=PP5V_S4_REG
VOUT = 5.0V
11A MAX OUTPUT
F = 400 KHZ
=PP5V_S5_LDO
VOUT = 5V
100MA MAX OUTPUT
=PPVIN_S5_P3V3
=PP3V3_S5_REG
VOUT = 3.3V
10A MAX OUTPUT
F = 400 KHZ
SKIP_5V3V3:INAUDIBLE
SKIP_5V3V3:AUDIBLE
P5VP3V3_VREG3
P5VP3V3_VREF2
P5VP3V3_SKIPSEL
TPS51980
QFN
CRITICAL
U7501
Q7520
CSD58872Q5D
L7520
2.2UH-20%-13A-9MOHM
PCMB103T-SM
L7560
1.0UH-22A
PCMC063T-SM
Q7560
RJK0214DPA
WPAK2
P5VS4_VSW
P5VS4_TG
P5VS4_VBST
P5VS4_DRVH
P5VS4_LL
P5VS4_DRVL
P5VS4_CSP1
P5VS4_CSN1
P5VS4_VFB1
P5VS4_COMP1
=P5VS4_EN
P5VS4_PGOOD
=P5VS5_EN
P3V3S5_TG
P3V3S5_VBST
P3V3S5_DRVH
P3V3S5_LL
P3V3S5_DRVL
P3V3S5_CSP2
P3V3S5_CSN2
P3V3S5_RF
P3V3S5_VFB2
P3V3S5_COMP2
=P3V3S5_EN
P3V3S5_PGOOD
P5VS4_VFB1_R
P5VS4_CSP1_R
P5VS4_COMP1_R
P3V3S5_VFB2_R
P3V3S5_CSP2_R
P3V3S5_SNUBR
NO STUFF
GND
GND_5V3V3_AGND
THRM_PAD
SYNC_MASTER=CLEAN_J45
SYNC_DATE=04/26/2013
PAGE TITLE
5V / 3.3V Power Supply
Apple Inc.
DRAWING NUMBER 051-0675
SIZE D
REVISION 6.0.0
BRANCH dvt
PAGE 75 OF 119
SHEET 60 OF 94
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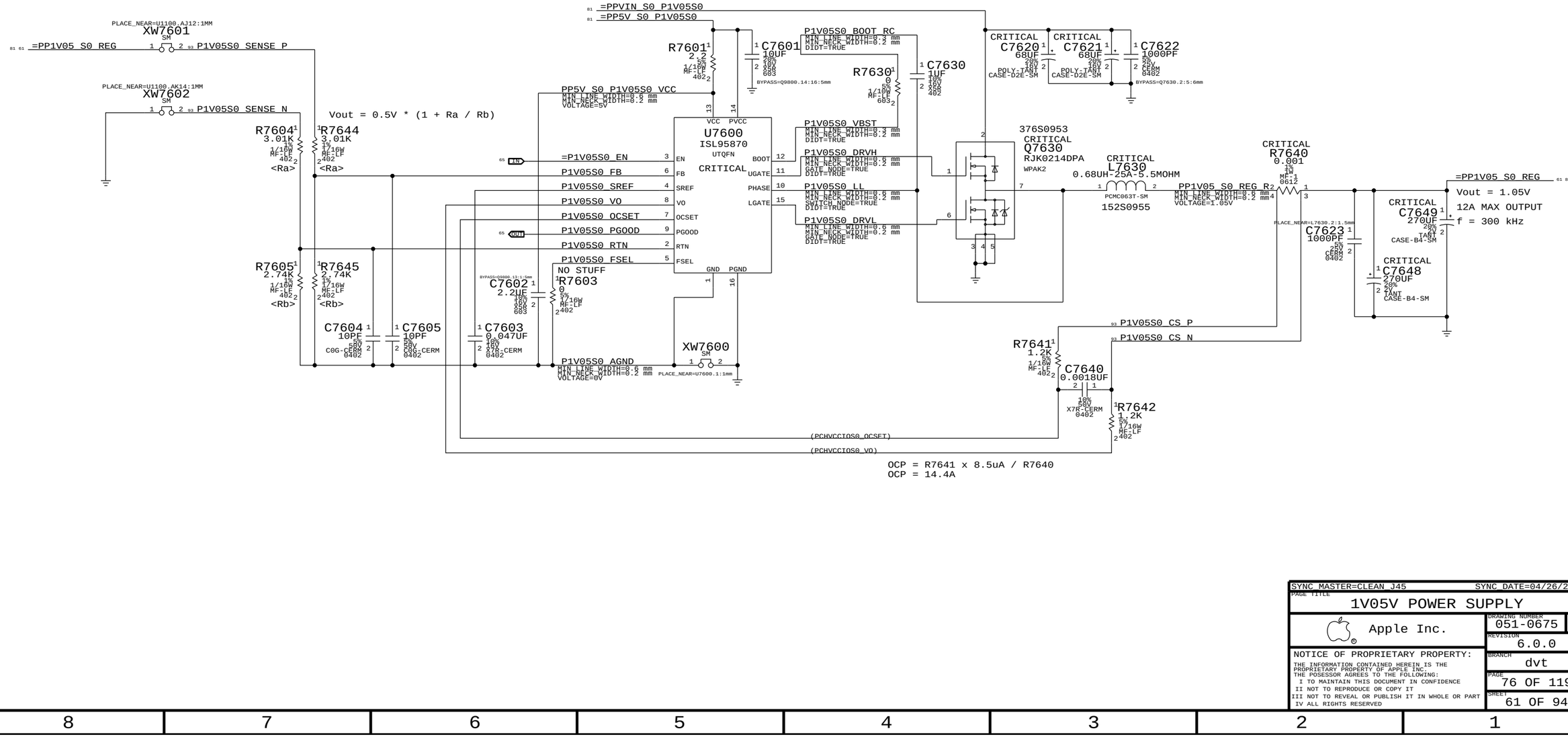
1V05 S0 REGULATOR



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: 1V05V POWER SUPPLY

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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SHEET: 61 OF 94

Page Notes

Power aliases required by this page:
- =PPVIN_S0_LCDBKLT (9-12.6V LCD Backlight Input)
- =PP5V_S0_BKLTCTRL (5V Backlight Driver Input)
- =PP5V_S0_KBDLED (5V Keyboard Backlight Input)

BOM options provided by this page:
BKLT:ENG - Stuffs 10.2 ohm series R for engineering builds
BKLT:PROD - Stuffs 0 ohm series R for production

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	8	RES,MTL FILM,0 OHM,1A MAX,0402,SMD	R7717,R7718,R7719,R7720,R7721,R7722,R7723,R7724		BKLT:PROD

=PPVIN_S0_LCDBKLT
CRITICAL F7700 3AMP-32V-467 603-HF
PPBUS_S0_LCDBKLT_FUSED
R7700 0.025 1% 1W MTL 0612
PPBUS_SW_LCDBKLT_PWR
CRITICAL Q7706 FDC638APZ_SBMS001 SSOT6-HF
PPBUS_SW_BKL
152S1527 CRITICAL L7710 22UH-20%-2.4A-0.105OHM DEM8030C-SM
PPBUS_S0_LCDBKLT_PWR_SW
PLACE_NEAR=L7710.2:3MM
CRITICAL D7701 POWERDI-123 DFLS2100
PPBUS_S0_LCDBKLT_PWR_SW SHOULD BE KEPT AS SHORT AS POSSIBLE
C7715, C7716 SHOULD BE PLACED MIRRORED
C7718, C7719 SHOULD BE PLACED MIRRORED
PPVOUT_S0_LCDBKLT
C7700 1000PF 10% 16V X7R-CERM 0201
R7701 80.6K 1% 1/20W MF 201
NOSTUFF C7701 0.001UF 10% 50V CERM 402
C7710 4.7UF 10% 25V X6S-CERM 0603
C7711 4.7UF 10% 25V X6S-CERM 0603
C7712 0.1UF 10% 25V X7R 402
C7715 2.2UF 10% 100V X7R 1210-1
C7716 2.2UF 10% 100V X7R 1210-1
C7718 2.2UF 10% 100V X7R 1210-1
C7719 2.2UF 10% 100V X7R 1210-1
C7717 1000PF 10% 100V X7R-CERM 0603
PLACE_NEAR=D7701.K:3MM PLACE_NEAR=D7701.K:3MM PLACE_NEAR=R7708.1:5MM
PLACE_NEAR=D7701.K:5MM PLACE_NEAR=D7701.K:5MM
ISNS_LCDBKLT_P
ISNS_LCDBKLT_N
LCDBKLT_EN_L
=PP5V_S0_BKLTCTRL
R7743 0 5% 1/16W MF-LF 402
R7744 0 5% 1/16W MF-LF 402
VOLTAGE=5V MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM
PP5V_S0_BKLT_VDDA
PP5V_S0_BKLT_VDDD
R7702 63.4K 1% 1/16W MF-LF 402
C7740 1UF 10% 16V X5R 402-2
C7741 1UF 10% 16V X5R 402-2
GND_BKLT_SGND
R7740 1M 5% 1/20W MF 201
U7701 QFN LP8548B1SQ_-03
BKL_SW MIN_LINE_WIDTH=2 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
BKL_FB
BKL_FET_CNTL_R MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
CRITICAL Q7701 SI7812DN PWRPK-1212-8
R7703 0 5% 1/16W MF-LF 402
BKL_FET_CNTL MIN_LINE_WIDTH=0.6 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
R7708 18.2K 1% 1/16W MF-LF 402
R7709 150K 1% 1/16W MF-LF 402
=PP5V_S0_BKLTCTRL
NOSTUFF R7760 4.7K 5% 1/20W MF 201
NOSTUFF R7761 4.7K 5% 1/20W MF 201
BKLT_SCL_R
BKLT_SDA_R
BKLT_SD
(PPBUS_S0_BKLT_PWR_R)
(PPBUS_S0_BKLT_PWR_F)
BKLT_SENSE_OUT
BKLT_EN_R
BKLT_PWM_KEYB
BKLT_ISET_KEYB
BKLT_KEYB1
BKLT_KEYB2
BKLT:ENG R7723 10.2 1% 1/16W 402
BKLT:ENG R7724 10.2 1% 1/16W TF 402
KBDBKLT_RETURN1 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
KBDBKLT_RETURN2 MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM
R7741 31.6K 1% 1/20W MF 201
PPVOUT_BKLT_FB2 MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=45V
KBDBKLT_SW MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM DIDT=TRUE
XW7720 SM PLACE_NEAR=D7720.K:2MM
C7726 1.0UF 10% 50V X7R 0805
C7727 1.0UF 10% 50V X7R 0805
=PP5V_S0_KBDLED
R7783 0 5% 1/16W MF-LF 402
MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=5V
PP5V_S0_KBDLED_R
152S1701 CRITICAL L7720 10UH-20%-1.4A-0.17OHM PST041H-CDH46D14-SM
371S0572 CRITICAL D7720 SOD-123 RB160M-60G
PPVOUT_S0_KBDBKLT MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=40V
C7720 2.2UF 10% 25V X5R-CERM 603
C7721 2.2UF 10% 25V X5R-CERM 603
C7722 0.1UF 10% 16V X5R-CERM 0201
C7723 1.0UF 10% 50V X7R 0805
C7724 1.0UF 10% 50V X7R 0805
C7725 0.001UF 10% 50V X7R-CERM 0402
C7720, C7721 SHOULD BE PLACED MIRRORED
C7723, C7724 SHOULD BE PLACED MIRRORED
=PP5V_S0_BKLTCTRL
C7750 1UF 10% 16V X5R 402-2
C7751 1UF 10% 16V X5R 402-2
GND_LCDBKLT_SGND
NOSTUFF C7752 1UF 10% 16V X5R 402-2
NOSTUFF R7752 0 5% 1/20W MF 0201
BKLT_FLT_RC
NOSTUFF C7753 1UF 10% 16V X5R 402-2
BKLT_FLT
NOSTUFF R7753 100K 1% 1/20W MF 201
NOSTUFF R7755 0 5% 1/20W MF 0201
LCD_FSS
BKLT_SYNC
LCD_BKLT_PWM
LCD_BKLT_PWM_R
BKLT_EN_R_JERRY
BKL_1_SDA
=I2C_BKL_1_SDA
BKL_1_SCL
=I2C_BKL_1_SCL
BKLT_ISET_LCD
U7750 LLP LP8549B1SP-03
R7754 27.4K 1% 1/16W MF-LF 402
R7756 10K 5% 1/16W MF-LF 402
XW7701 SM
GND_LCDBKLT_SGND MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25 MM VOLTAGE=0V
LCD_BKLT_EN
R7742 0 5% 1/20W MF 0201
NO STUFF C7742 33PF 5% 25V NPO-C0G 0201
GND_BKLT_SGND
SMC_SYS_KBDLED
R7747 0 5% 1/20W MF 0201
NO STUFF C7747 33PF 5% 25V NPO-C0G 0201
GND_BKLT_SGND
R7757 0 5% 1/20W MF 0201
R7758 0 5% 1/20W MF 0201
BKLT_SDA
BKLT_SCL
CRITICAL 353S4159
XW7700 SM
GND_BKLT_SGND MIN_LINE_WIDTH=0.4 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=0V
BKL_ISEN1
BKL_ISEN2
BKL_ISEN3
BKL_ISEN4
BKL_ISEN5
BKL_ISEN6
R7717 10.2 0.1% 1/16W TF 402
R7718 10.2 0.1% 1/16W TF 402
R7719 10.2 0.1% 1/16W TF 402
R7720 10.2 0.1% 1/16W TF 402
R7721 10.2 0.1% 1/16W TF 402
R7722 10.2 0.1% 1/16W TF 402
BKLT:ENG
LED_RETURN_1
LED_RETURN_2
LED_RETURN_3
LED_RETURN_4
LED_RETURN_5
LED_RETURN_6
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.20 MM
MIN_LINE_WIDTH=0.35 MM MIN_NECK_WIDTH=0.20 MM

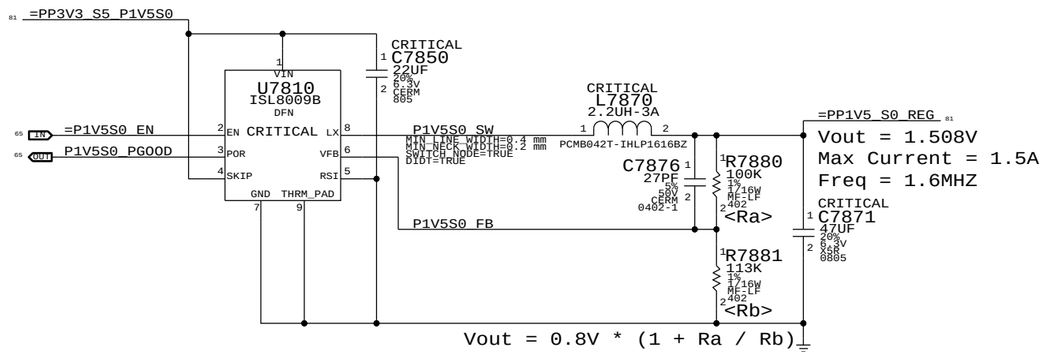
SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: LCD/KBD Backlight Driver

Apple Inc.

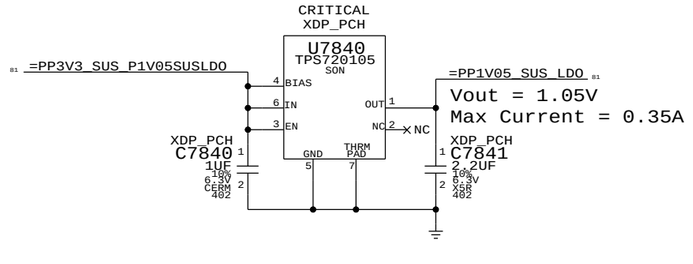
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
PAGE: 77 OF 119
SHEET: 62 OF 94

1.5V S0 Regulator



1.05V SUS LDO

Lynx Point-H requires JTAG pull-ups to be powered at 1.05V in SUS.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage dividers (200/100) to 3.3V SUS, which burns 100mW in all S-states.



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Misc Power Supplies

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

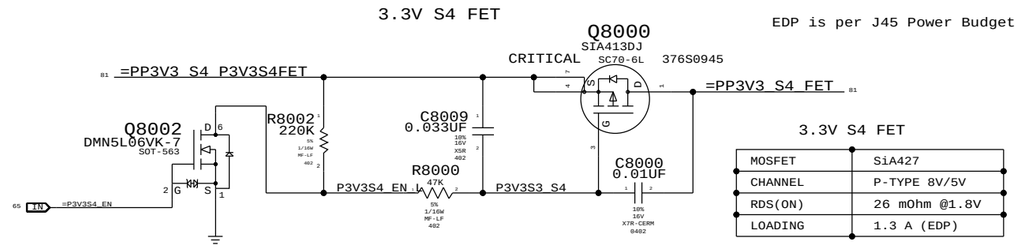
BRANCH: dvt

PAGE: 78 OF 119

SHEET: 63 OF 94

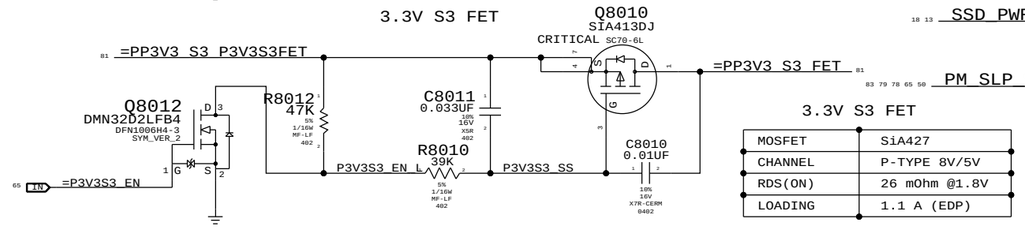
EDP is per J45 Power Budget rev5

3.3V S4 FET



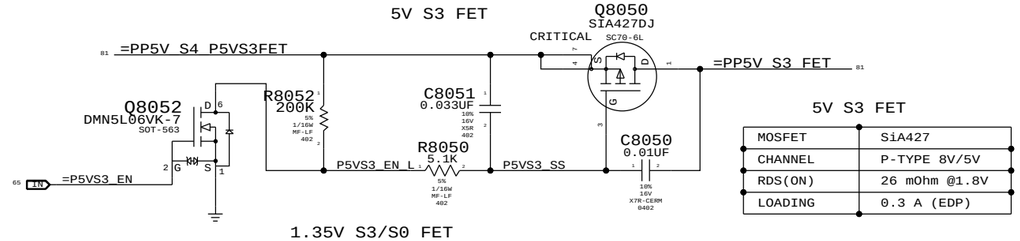
3.3V S4 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.3 A (EDP)

3.3V S3 FET



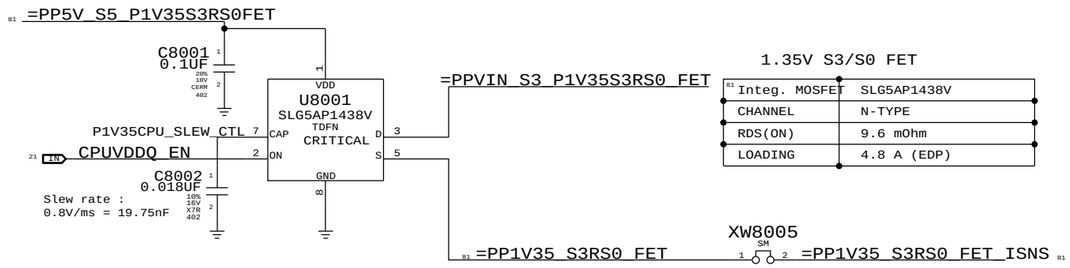
3.3V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.1 A (EDP)

5V S3 FET



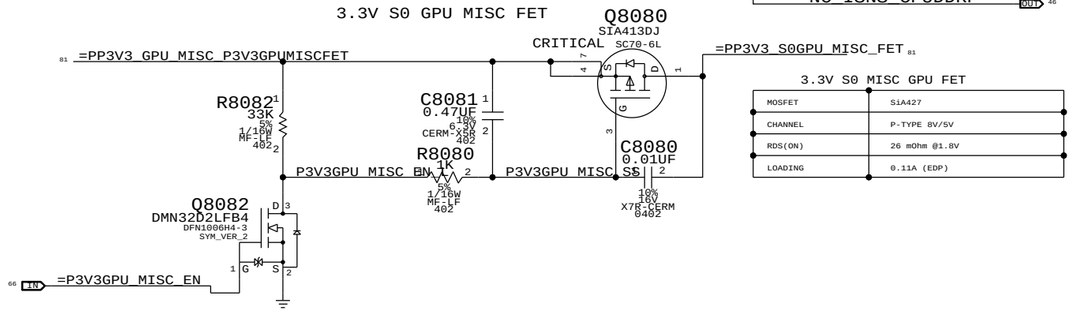
5V S3 FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.3 A (EDP)

1.35V S3/S0 FET



1.35V S3/S0 FET	
Integ. MOSFET	SLG5AP1438V
CHANNEL	N-TYPE
RDS(ON)	9.6 mOhm
LOADING	4.8 A (EDP)

3.3V S0 GPU MISC FET



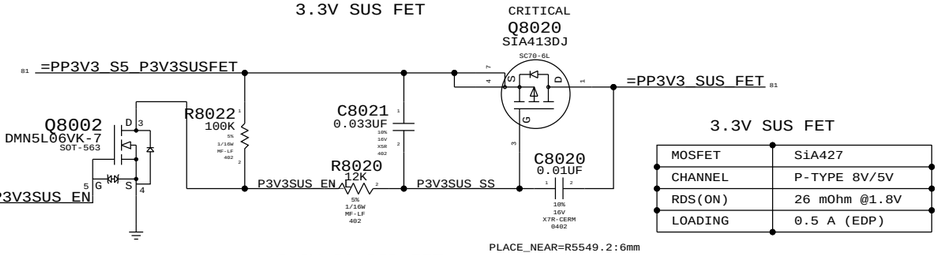
3.3V S0 MISC GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.11A (EDP)

SSD_PWR_EN:GPIO → =P3V3SUS_EN

SSD_PWR_EN → R8073 0 (0201 1/20W 5% MF) → SSD_PWR_EN:S0

PM_SLP_S3_BUF_L → R8074 0 (0201 1/20W 5% MF) → SSD_PWR_FET_EN

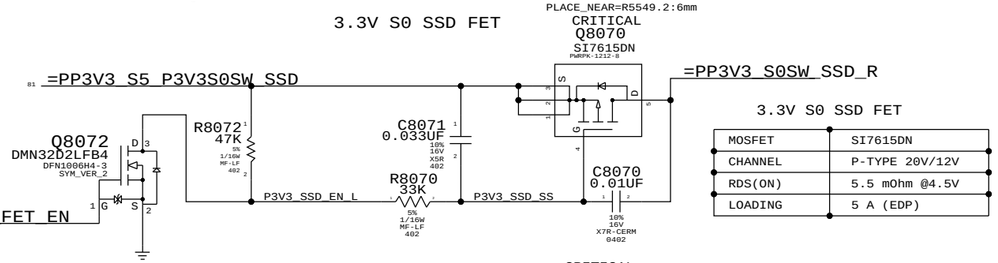
3.3V SUS FET



3.3V SUS FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.5 A (EDP)

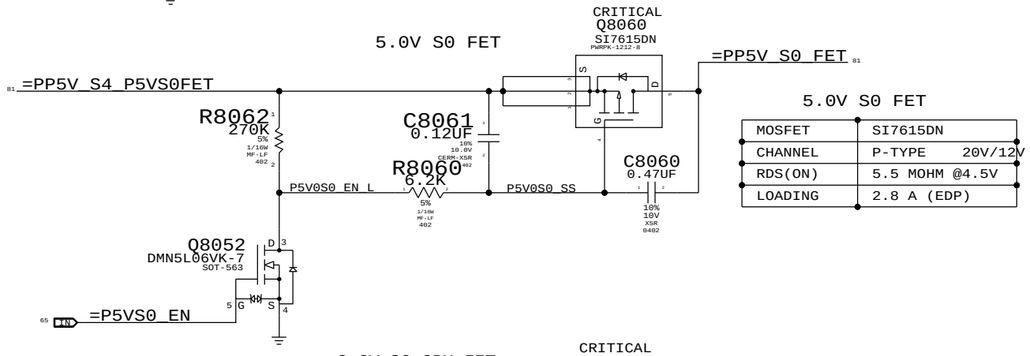
PLACE_NEAR=R5549.2:6mm

3.3V S0 SSD FET



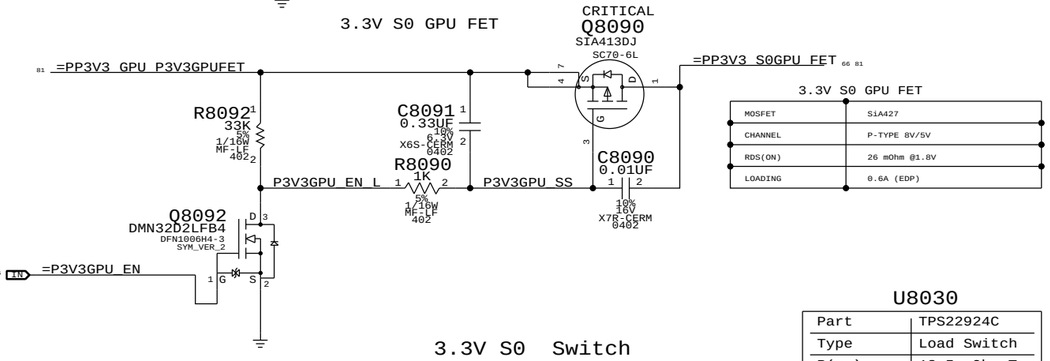
3.3V S0 SSD FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 mOhm @4.5V
LOADING	5 A (EDP)

5.0V S0 FET



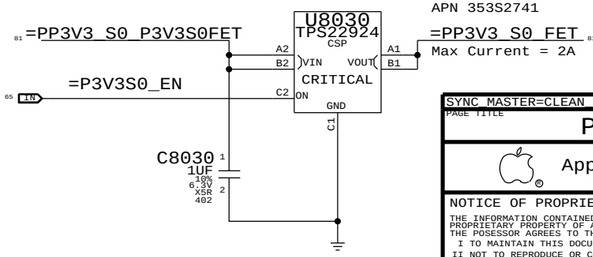
5.0V S0 FET	
MOSFET	SI7615DN
CHANNEL	P-TYPE 20V/12V
RDS(ON)	5.5 MOHM @4.5V
LOADING	2.8 A (EDP)

3.3V S0 GPU FET



3.3V S0 GPU FET	
MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	0.6A (EDP)

3.3V S0 Switch



U8030	
Part	TPS22924C
Type	Load Switch
R(on) @ 2.5V	18.5 mOhm Typ 25.8 mOhm Max

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Power FETs

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

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BRANCH dvt

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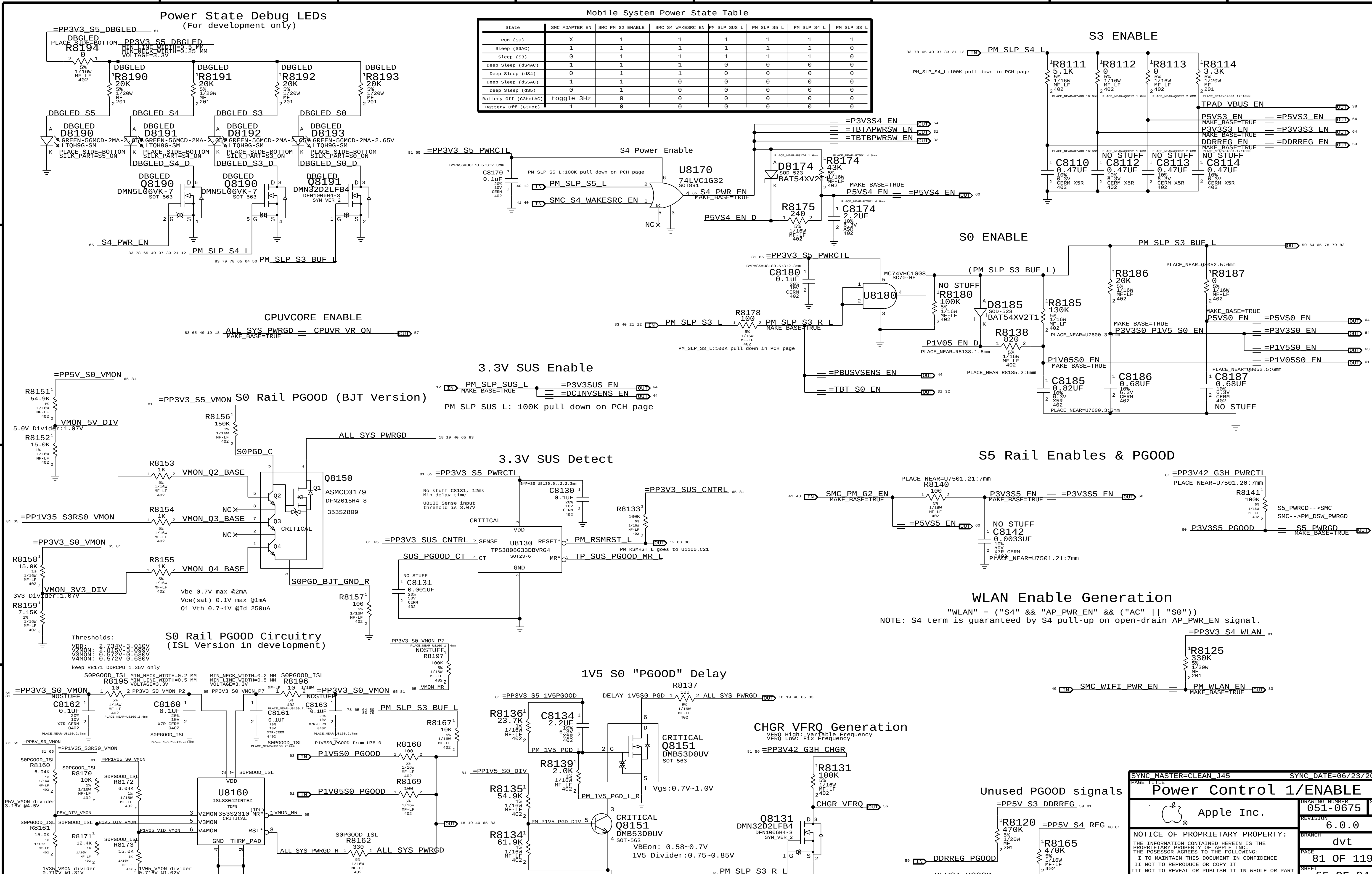

Mobile System Power State Table

State	SMC_ADAPTER_EN	SMC_PM_G2_ENABLE	SMC_S4_WAKESRC_EN	PM_SLP_SUS_L	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	X	1	1	1	1	1	1
Sleep (S3AC)	1	1	1	1	1	1	0
Sleep (S3)	0	1	1	1	1	1	0
Deep Sleep (dS4AC)	1	1	1	0	0	0	0
Deep Sleep (dS4)	0	1	1	0	0	0	0
Deep Sleep (dS5AC)	1	1	0	0	0	0	0
Deep Sleep (dS5)	0	1	0	0	0	0	0
Battery Off (G3HotAC)	toggle 3Hz	0	0	0	0	0	0
Battery Off (G3Hot)	1	0	0	0	0	0	0

SYNC_MASTER=CLEAN_J45 SYNC_DATE=06/23/2013

PAGE TITLE
Power Control 1/ENABLE

Apple Inc.

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GPU Rail Sequencing

KEPLER GPU REQUIRES RAILS TO COME
up in the following order:

1) GPU_3.3V
2) IFPX IOVDD - 1.8V
3) GPUVCORE
4) FBVDDQ/GDDR5 1.35V
5) PEXVDD/Q OR IFPY IOVDD - 1.05V

			=P3V3GPU_MISC_EN	OUT 64
79 EG_RAIL1_EN	P3V3GPU_EN	MAKE_BASE=TRUE	=P3V3GPU_EN	OUT 64
79 EG_RAIL2_EN	P1V8GPU_EN	MAKE_BASE=TRUE	=P1V8GPU_EN	OUT 82
79 EG_RAIL3_EN	GPUVCORE_EN	MAKE_BASE=TRUE	=GPUVCORE_EN	OUT 77
79 EG_RAIL4_EN	P1V35GPUFB_EN	MAKE_BASE=TRUE	=P1V35FB_EN	OUT 71
79 EG_RAIL5_EN	P1V05_S0GPU_EN	MAKE_BASE=TRUE	=P1V05_GPU_EN	OUT 71

NOTE: 1V8 MAY NOT BE REQUIRED FOR KEPLER IF THERE IS NO LVDS

EXT GPU PWRGD Pullup

=PP3V3_S0_PWRCTL (81)

R8200 R8201 R8202
100K 5% 1/20W ME 0201

81 64 IN =PP3V3_S0GPU_FET	GPU_PGOOD1		OUT 79
TP_GPU_PGOOD2	GPU_PGOOD2	MAKE_BASE=TRUE	OUT 79
77 IN GPUVCORE_PGOOD	GPU_PGOOD3	MAKE_BASE=TRUE	OUT 79
71 IN GPUFB_PGOOD	GPU_PGOOD4	MAKE_BASE=TRUE	OUT 79
71 IN P1V05_S0GPU_PGOOD	PM_ALL_GPU_PGOOD	MAKE_BASE=TRUE	OUT 79

NOTE: NO PU ON 3V3 AND 1V8 PGOODS SINCE THEY ARE SYNTHETIC.

NOTE 2: CHECK IF 1V8 IS READ AS LOGIC HIGH BY GMUX

PEG_R2D_P<0> (68 86) — R8210 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<0> (68 86)

PEG_R2D_P<5> (68 86) — R8215 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<5> (68 86)

PEG_R2D_P<3> (68 86) — R8213 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<3> (68 86)

PEG_R2D_P<7> (68 86) — R8217 82 5% 1/20W ME 0201 — NOSTUFF — PEG_R2D_N<7> (68 86)

PLACE R8210 - R8217 CLOSE TO U8000

PCIE TEST STRUCTURES (FOR LAB USE)

PEG_D2R_P<0> (68 82 86) — R8220 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<0> (68 82 86)

PEG_D2R_P<4> (68 82 86) — R8224 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<4> (68 82 86)

PEG_D2R_P<7> (68 82 86) — R8227 82 5% 1/20W ME 0201 — NOSTUFF — PEG_D2R_N<7> (68 82 86)

PLACE R8220 - R8227 CLOSE TO U1000

SYNC_MASTER=D2_KEPLER SYNC_DATE=01/13/2012

PAGE TITLE: Power Sequencing EG/PCH S0

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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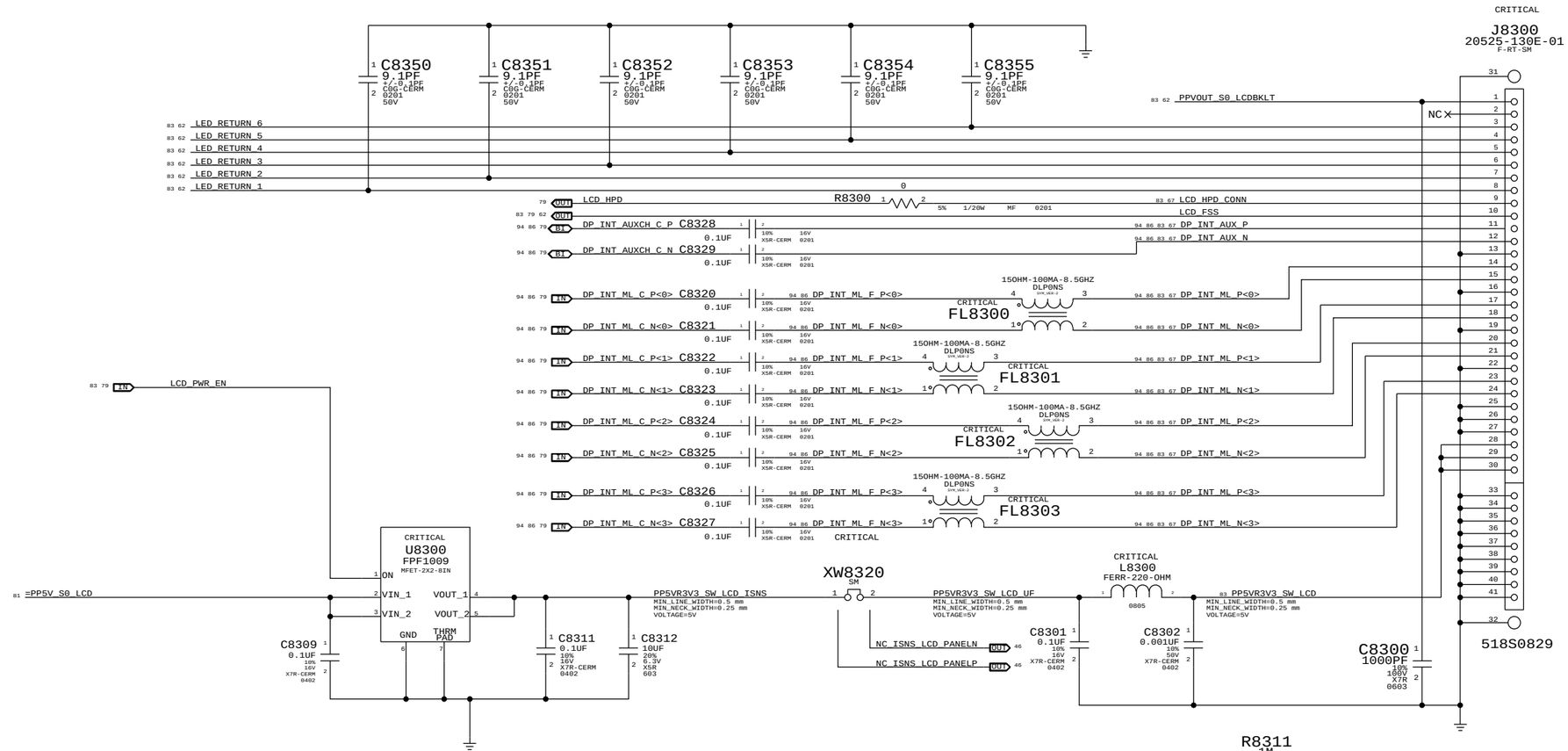
LCD PANEL INTERFACE (eDP)



SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE

eDP Display Connector

Apple Inc.

DRAWING NUMBER 051-0675 SIZE D

REVISION 6.0.0

BRANCH dvt

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Page Notes

Power aliases required by this page:

- +PP3V3_GPU_VDD33

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

C8420 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<0> → PEG_R2D_P<0>
C8421 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<0> → PEG_R2D_N<0>
C8422 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<1> → PEG_R2D_P<1>
C8423 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<1> → PEG_R2D_N<1>
C8424 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<2> → PEG_R2D_P<2>
C8425 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<2> → PEG_R2D_N<2>
C8426 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<3> → PEG_R2D_P<3>
C8427 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<3> → PEG_R2D_N<3>
C8428 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<4> → PEG_R2D_P<4>
C8429 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<4> → PEG_R2D_N<4>
C8430 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<5> → PEG_R2D_P<5>
C8431 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<5> → PEG_R2D_N<5>
C8432 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<6> → PEG_R2D_P<6>
C8433 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<6> → PEG_R2D_N<6>
C8434 0.22UF GND_VOID=TRUE — PEG_R2D_C_P<7> → PEG_R2D_P<7>
C8435 0.22UF GND_VOID=TRUE — PEG_R2D_C_N<7> → PEG_R2D_N<7>

C8455 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<0> → PEG_D2R_P<0>
C8456 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<0> → PEG_D2R_N<0>
C8457 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<1> → PEG_D2R_P<1>
C8458 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<1> → PEG_D2R_N<1>
C8459 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<2> → PEG_D2R_P<2>
C8460 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<2> → PEG_D2R_N<2>
C8461 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<3> → PEG_D2R_P<3>
C8462 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<3> → PEG_D2R_N<3>
C8463 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<4> → PEG_D2R_P<4>
C8464 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<4> → PEG_D2R_N<4>
C8465 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<5> → PEG_D2R_P<5>
C8466 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<5> → PEG_D2R_N<5>
C8467 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<6> → PEG_D2R_P<6>
C8468 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<6> → PEG_D2R_N<6>
C8469 0.22UF GND_VOID=TRUE — PEG_D2R_C_P<7> → PEG_D2R_P<7>
C8470 0.22UF GND_VOID=TRUE — PEG_D2R_C_N<7> → PEG_D2R_N<7>

OMIT_TABLE

U8400
NV-GK107
BGA
(1 OF 10)

PEG_R2D_P<0>	AN12	PEX_RX0	PEX_TX0	AK14	PEG_D2R_C_P<0>
PEG_R2D_N<0>	AM12	PEX_RX0*	PEX_TX0*	AJ14	PEG_D2R_C_N<0>
PEG_R2D_P<1>	AN14	PEX_RX1	PEX_TX1	AH14	PEG_D2R_C_P<1>
PEG_R2D_N<1>	AM14	PEX_RX1*	PEX_TX1*	AG14	PEG_D2R_C_N<1>
PEG_R2D_P<2>	AP14	PEX_RX2	PEX_TX2	AK15	PEG_D2R_C_P<2>
PEG_R2D_N<2>	AP15	PEX_RX2*	PEX_TX2*	AJ15	PEG_D2R_C_N<2>
PEG_R2D_P<3>	AN15	PEX_RX3	PEX_TX3	AL16	PEG_D2R_C_P<3>
PEG_R2D_N<3>	AM15	PEX_RX3*	PEX_TX3*	AK16	PEG_D2R_C_N<3>
PEG_R2D_P<4>	AN17	PEX_RX4	PEX_TX4	AK17	PEG_D2R_C_P<4>
PEG_R2D_N<4>	AM17	PEX_RX4*	PEX_TX4*	AJ17	PEG_D2R_C_N<4>
PEG_R2D_P<5>	AP17	PEX_RX5	PEX_TX5	AH17	PEG_D2R_C_P<5>
PEG_R2D_N<5>	AP18	PEX_RX5*	PEX_TX5*	AG17	PEG_D2R_C_N<5>
PEG_R2D_P<6>	AN18	PEX_RX6	PEX_TX6	AK18	PEG_D2R_C_P<6>
PEG_R2D_N<6>	AM18	PEX_RX6*	PEX_TX6*	AJ18	PEG_D2R_C_N<6>
PEG_R2D_P<7>	AN20	PEX_RX7	PEX_TX7	AL19	PEG_D2R_C_P<7>
PEG_R2D_N<7>	AM20	PEX_RX7*	PEX_TX7*	AK19	PEG_D2R_C_N<7>
NC	AP20	PEX_RX8	PEX_TX8	AK20	NC
NC	AP21	PEX_RX8*	PEX_TX8*	AJ20	NC
NC	AN21	PEX_RX9	PEX_TX9	AH20	NC
NC	AM21	PEX_RX9*	PEX_TX9*	AG20	NC
NC	AN23	PEX_RX10	PEX_TX10	AK21	NC
NC	AM23	PEX_RX10*	PEX_TX10*	AJ21	NC
NC	AP23	PEX_RX11	PEX_TX11	AL22	NC
NC	AP24	PEX_RX11*	PEX_TX11*	AK22	NC
NC	AN24	PEX_RX12	PEX_TX12	AK23	NC
NC	AM24	PEX_RX12*	PEX_TX12*	AJ23	NC
NC	AN26	PEX_RX13	PEX_TX13	AH23	NC
NC	AM26	PEX_RX13*	PEX_TX13*	AG23	NC
NC	AP26	PEX_RX14	PEX_TX14	AK24	NC
NC	AP27	PEX_RX14*	PEX_TX14*	AJ24	NC
NC	AN27	PEX_RX15	PEX_TX15	AL25	NC
NC	AM27	PEX_RX15*	PEX_TX15*	AK25	NC
PEG_CLK100M_P	AL13	PEX_REFCLK	PEX_TSTCLK_OUT	AJ26	PEX_TSTCLK_O_P
PEG_CLK100M_N	AK13	PEX_REFCLK*	PEX_TSTCLK_OUT*	AK26	PEX_TSTCLK_O_N
GPU_RESET_L → R8400 0 MF 5% 1/20W 0201 → GPU_RESET_R_L	AJ12	PEX_RST*	PEX_TERMP	AP29	R8405 2.49K 1% 1/20W MF 201 → GPU_PEX_TERMP
PEX_CLKREQ_L_R	AK12	PEX_CLKREQ*	PEX_SVDD_3V3	AG12	PP3V3_GPU_PEX_PLL_HVDD
NC	AJ11	PEX_WAKE*			

=PP3V3_GPU_VDD33 → R8401 10K 1% 1/20W MF 201 → PEX_CLKREQ_L_R

NOSTUFF R8402 200 1% 1/20W MF 201 — PEX_TSTCLK_O_P ↔ PEX_TSTCLK_O_N

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	KEPLER PCI-E
	Apple Inc.
DRAWING NUMBER	051-0675
SIZE	D
REVISION	6.0.0
BRANCH	dvt
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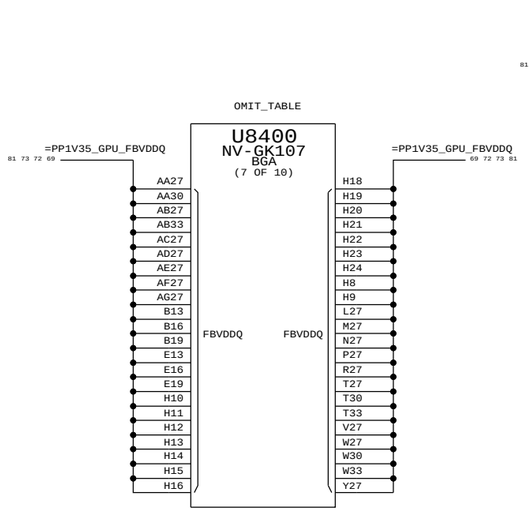

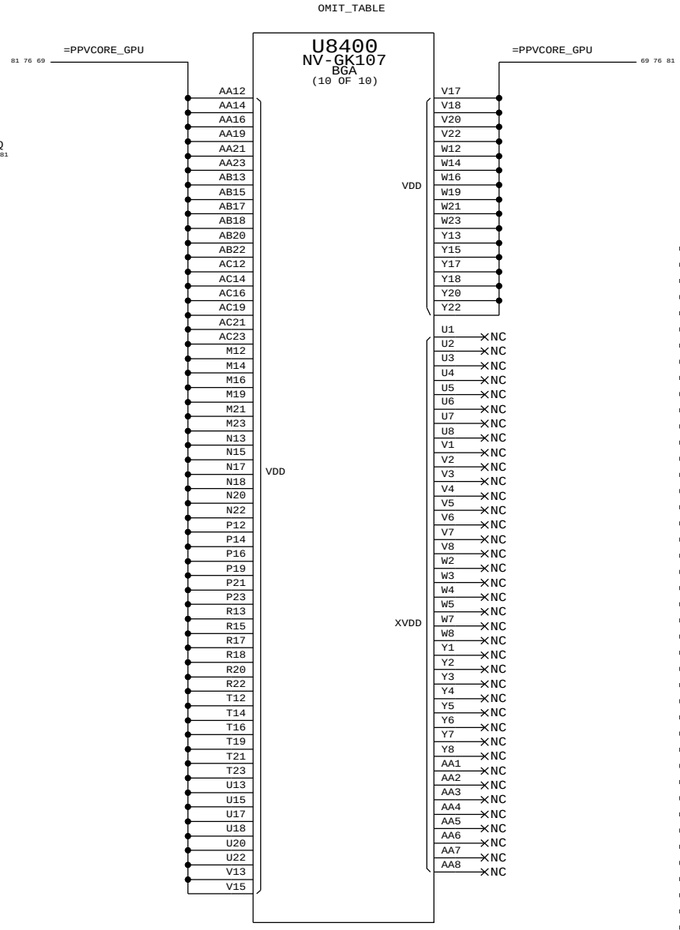

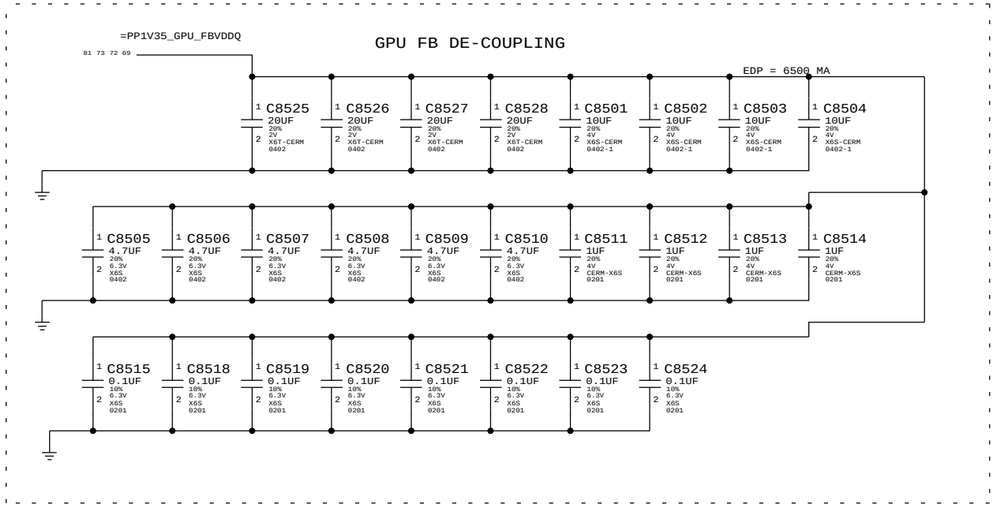

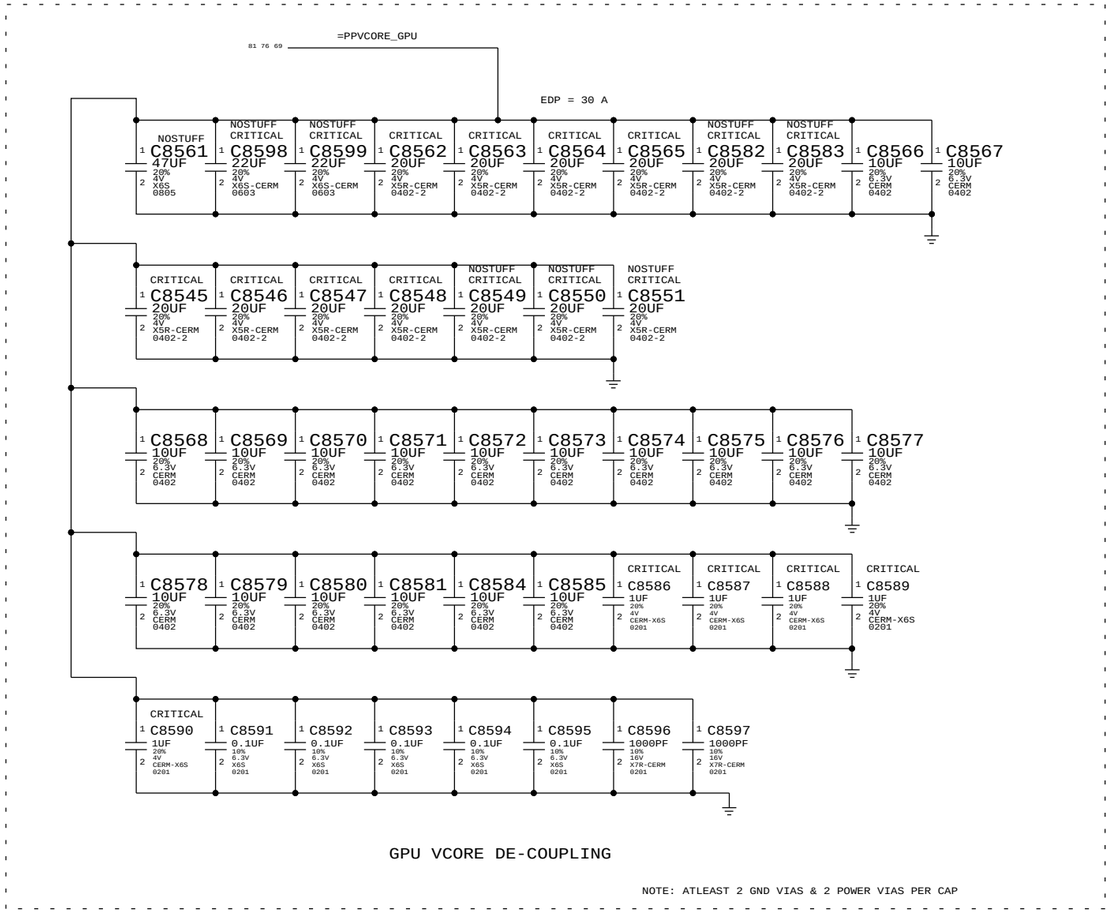

GPU VCORE DE-COUPLING

NOTE: ATLEAST 2 GND VIAS & 2 POWER VIAS PER CAP

Page Notes

Power aliases required by this page:

- =PPVCORE_GPU
- =PP1V35_GPU_FBVDDQ

Signal aliases required by this page:

(NONE)

BOM options provided by this page:

(NONE)

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE: KEPLER CORE/FB POWER

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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NOTE:GDDR5 MODE H MAPPING

OMIT_TABLE

U8400
NV-GK107
BGA
(3 OF 10)
MEM INTERFACE A

FB_A0_DQ<0>	L28	FBA_D0	U30	FBA_CMD0	FB_A0_CS_L	
FB_A0_DQ<1>	M29	FBA_D1	T31	FBA_CMD1	FB_A0_A<3>	
FB_A0_DQ<2>	L29	FBA_D2	U29	FBA_CMD2	FB_A0_A<2>	
FB_A0_DQ<3>	M28	FBA_D3	R34	FBA_CMD3	FB_A0_A<4>	
FB_A0_DQ<4>	N31	FBA_D4	R33	FBA_CMD4	FB_A0_A<5>	
FB_A0_DQ<5>	P29	FBA_D5	U32	FBA_CMD5	FB_A0_WE_L	
FB_A0_DQ<6>	R29	FBA_D6	U33	FBA_CMD6	FB_A0_A<7>	
FB_A0_DQ<7>	P28	FBA_D7	U28	FBA_CMD7	FB_A0_A<6>	
FB_A0_DQ<8>	J28	FBA_D8	V28	FBA_CMD8	FB_A0_ABI_L	
FB_A0_DQ<9>	H29	FBA_D9	V29	FBA_CMD9	FB_A0_A<8>	
FB_A0_DQ<10>	J29	FBA_D10	V30	FBA_CMD10	FB_A0_A<0>	
FB_A0_DQ<11>	H28	FBA_D11	U34	FBA_CMD11	FB_A0_A<1>	
FB_A0_DQ<12>	G29	FBA_D12	U31	FBA_CMD12	FB_A0_RAS_L	
FB_A0_DQ<13>	E31	FBA_D13	V34	FBA_CMD13	FB_A0_RESET_L	70 72 94
FB_A0_DQ<14>	E32	FBA_D14	V33	FBA_CMD14	FB_A0_CKE_L	70 72 94
FB_A0_DQ<15>	F30	FBA_D15	Y32	FBA_CMD15	FB_A0_CAS_L	
FB_A0_DQ<16>	C34	FBA_D16	AA31	FBA_CMD16	FB_A1_CS_L	
FB_A0_DQ<17>	D32	FBA_D17	AA29	FBA_CMD17	FB_A1_A<3>	
FB_A0_DQ<18>	B33	FBA_D18	AA28	FBA_CMD18	FB_A1_A<2>	
FB_A0_DQ<19>	C33	FBA_D19	AC34	FBA_CMD19	FB_A1_A<4>	
FB_A0_DQ<20>	F33	FBA_D20	AC33	FBA_CMD20	FB_A1_A<5>	
FB_A0_DQ<21>	F32	FBA_D21	AA32	FBA_CMD21	FB_A1_WE_L	
FB_A0_DQ<22>	H33	FBA_D22	AA33	FBA_CMD22	FB_A1_A<7>	
FB_A0_DQ<23>	H32	FBA_D23	Y28	FBA_CMD23	FB_A1_A<6>	
FB_A0_DQ<24>	P34	FBA_D24	Y29	FBA_CMD24	FB_A1_ABI_L	
FB_A0_DQ<25>	P32	FBA_D25	W31	FBA_CMD25	FB_A1_A<8>	
FB_A0_DQ<26>	P31	FBA_D26	Y30	FBA_CMD26	FB_A1_A<0>	
FB_A0_DQ<27>	P33	FBA_D27	AA34	FBA_CMD27	FB_A1_A<1>	
FB_A0_DQ<28>	L31	FBA_D28	Y31	FBA_CMD28	FB_A1_RAS_L	
FB_A0_DQ<29>	L34	FBA_D29	Y34	FBA_CMD29	FB_A1_RESET_L	70 72 94
FB_A0_DQ<30>	L32	FBA_D30	Y33	FBA_CMD30	FB_A1_CKE_L	70 72 94
FB_A0_DQ<31>	L33	FBA_D31	V31	FBA_CMD31	FB_A1_CAS_L	
FB_A1_DQ<0>	AG28	FBA_D32				
FB_A1_DQ<1>	AF29	FBA_D33	R30	FBA_CLK0	FB_A0_CLK_P	
FB_A1_DQ<2>	AG29	FBA_D34	R31	FBA_CLK0*	FB_A0_CLK_N	
FB_A1_DQ<3>	AF28	FBA_D35	AB31	FBA_CLK1	FB_A1_CLK_P	
FB_A1_DQ<4>	AD30	FBA_D36	AC31	FBA_CLK1*	FB_A1_CLK_N	
FB_A1_DQ<5>	AD29	FBA_D37	P30	FBA_DQM0	FB_A0_DBI_L<0>	
FB_A1_DQ<6>	AC29	FBA_D38	F31	FBA_DQM1	FB_A0_DBI_L<1>	
FB_A1_DQ<7>	AD28	FBA_D39	F34	FBA_DQM2	FB_A0_DBI_L<2>	
FB_A1_DQ<8>	AJ29	FBA_D40	M32	FBA_DQM3	FB_A0_DBI_L<3>	
FB_A1_DQ<9>	AK29	FBA_D41	AD31	FBA_DQM4	FB_A1_DBI_L<0>	
FB_A1_DQ<10>	AJ30	FBA_D42	AL29	FBA_DQM5	FB_A1_DBI_L<1>	
FB_A1_DQ<11>	AK28	FBA_D43	AM32	FBA_DQM6	FB_A1_DBI_L<2>	
FB_A1_DQ<12>	AM29	FBA_D44	AF34	FBA_DQM7	FB_A1_DBI_L<3>	
FB_A1_DQ<13>	AM31	FBA_D45				
FB_A1_DQ<14>	AN29	FBA_D46	M30	FBA_DQS_RN0	NC	
FB_A1_DQ<15>	AM30	FBA_D47	H30	FBA_DQS_RN1	NC	
FB_A1_DQ<16>	AN31	FBA_D48	E34	FBA_DQS_RN2	NC	
FB_A1_DQ<17>	AN32	FBA_D49	M34	FBA_DQS_RN3	NC	
FB_A1_DQ<18>	AP30	FBA_D50	AF30	FBA_DQS_RN4	NC	
FB_A1_DQ<19>	AP32	FBA_D51	AK31	FBA_DQS_RN5	NC	
FB_A1_DQ<20>	AM33	FBA_D52	AM34	FBA_DQS_RN6	NC	
FB_A1_DQ<21>	AL31	FBA_D53	AF32	FBA_DQS_RN7	NC	
FB_A1_DQ<22>	AK33	FBA_D54				
FB_A1_DQ<23>	AK32	FBA_D55	M31	FBA_DQS_WP0	FB_A0_EDC<0>	
FB_A1_DQ<24>	AD34	FBA_D56	G31	FBA_DQS_WP1	FB_A0_EDC<1>	
FB_A1_DQ<25>	AD32	FBA_D57	E33	FBA_DQS_WP2	FB_A0_EDC<2>	
FB_A1_DQ<26>	AC30	FBA_D58	M33	FBA_DQS_WP3	FB_A0_EDC<3>	
FB_A1_DQ<27>	AD33	FBA_D59	AE31	FBA_DQS_WP4	FB_A1_EDC<0>	
FB_A1_DQ<28>	AF31	FBA_D60	AK30	FBA_DQS_WP5	FB_A1_EDC<1>	
FB_A1_DQ<29>	AG34	FBA_D61	AN33	FBA_DQS_WP6	FB_A1_EDC<2>	
FB_A1_DQ<30>	AG32	FBA_D62	AF33	FBA_DQS_WP7	FB_A1_EDC<3>	
FB_A1_DQ<31>	AG33	FBA_D63				
FB_A0_WCLK_P<0>	K31	FBA_WCK01	K27	FB_DLL_AVDD	PP1V05_GPU_FB_DLL_AVDD	70
FB_A0_WCLK_N<0>	L30	FBA_WCK01*	U27	FBA_PLL_AVDD	PP1V05_GPU_FB_PLL_AVDD	70
FB_A1_WCLK_P<1>	H34	FBA_WCK23	R28	FBA_DEBUG	GPU_FBA_DEBUG0	
FB_A1_WCLK_N<1>	J34	FBA_WCK23*	AC28	FBA_DEBUG	GPU_FBA_DEBUG1	
FB_A1_WCLK_P<0>	AG30	FBA_WCK45	J27	FB_CAL_PD_VDDQ	FB_CAL_PD_VDDQ	70
FB_A1_WCLK_N<0>	AG31	FBA_WCK45*	H27	FB_CAL_PU_GND	FB_CAL_PU_GND	70
FB_A1_WCLK_P<1>	AJ34	FBA_WCK67	H25	FB_CAL_TERM_GND	FB_CAL_TERM_GND	1
FB_A1_WCLK_N<1>	AK34	FBA_WCK67*	E1	70 FB_CLAMP	FB_CLAMP	
	J30	FBA_WCKB01	R32		NC	
	J31	FBA_WCKB01*	AC32		NC	
	J32	FBA_WCKB23	F1		GPU_FBVDDQ_SENSE	
	J33	FBA_WCKB23*	F2		GPU_FBGND_SENSE	
	AH31	FBA_WCKB45				
	AJ31	FBA_WCKB45*				
	AJ32	FBA_WCKB67				
	AJ33	FBA_WCKB67*				

94 72 70 FB_A0_RESET_L — R8650 10K 1% 1/20W MF 201

94 72 70 FB_A1_RESET_L — R8651 10K 1% 1/20W MF 201

FB_A0_CKE_L 70 72 94 — R8652 10K 1% 1/20W MF 201

FB_A1_CKE_L 70 72 94 — R8653 10K 1% 1/20W MF 201

=PP1V35_GPU_S0_FB 70 81

NOSTUFF R8658 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.H26:8.4MM

FB_VREF 70 — PLACE_NEAR=U8400.H26:8.4MM

NOSTUFF R8659 1.33K 1% 1/20W MF 201 — PLACE_NEAR=U8400.H26:8.4MM

NOSTUFF C8660 0.1UF 10% 6.3V X6S 0201

FB VREF GEN (TEST ONLY)

=PP1V35_GPU_S0_FB 70 81

R8603 60.4 1% 1/20W MF 201

R8602 60.4 1% 1/20W MF 201

R8670 100 5% 1/20W MF 201

R8601 60.4 1% 1/20W MF 201 — PLACE_NEAR=U8400.H25:8.4MM

R8661 10K 1% 1/20W MF 201

PLACE CLOSE TO BGA

70 FB_CAL_PU_GND — R8604 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8400.H27:8.4MM

=PP1V35_GPU_S0_FB 70 81 — R8605 40.2 1% 1/20W MF 201 — PLACE_NEAR=U8400.J27:8.4MM — FB_CAL_PD_VDDQ 70

R8671 100 5% 1/20W MF 201

OMIT_TABLE

U8400
NV-GK107
BGA
(4 OF 10)
MEM INTRERFACE B

FB_B0_DQ<0>	G9	FBB_D0	D13	FBB_CMD0	FB_B0_CS_L	
FB_B0_DQ<1>	E9	FBB_D1	E14	FBB_CMD1	FB_B0_A<3>	
FB_B0_DQ<2>	G8	FBB_D2	F14	FBB_CMD2	FB_B0_A<2>	
FB_B0_DQ<3>	F9	FBB_D3	A12	FBB_CMD3	FB_B0_A<4>	
FB_B0_DQ<4>	F11	FBB_D4	B12	FBB_CMD4	FB_B0_A<5>	81 76 70
FB_B0_DQ<5>	G11	FBB_D5	C14	FBB_CMD5	FB_B0_WE_L	
FB_B0_DQ<6>	F12	FBB_D6	B14	FBB_CMD6	FB_B0_A<7>	
FB_B0_DQ<7>	G12	FBB_D7	G15	FBB_CMD7	FB_B0_A<6>	
FB_B0_DQ<8>	G6	FBB_D8	F15	FBB_CMD8	FB_B0_ABI_L	
FB_B0_DQ<9>	F5	FBB_D9	E15	FBB_CMD9	FB_B0_A<8>	
FB_B0_DQ<10>	E6	FBB_D10	D15	FBB_CMD10	FB_B0_A<0>	
FB_B0_DQ<11>	F6	FBB_D11	A14	FBB_CMD11	FB_B0_A<1>	
FB_B0_DQ<12>	F4	FBB_D12	D14	FBB_CMD12	FB_B0_RAS_L	
FB_B0_DQ<13>	G4	FBB_D13	A15	FBB_CMD13	FB_B0_RESET_L	70 73 94
FB_B0_DQ<14>	E2	FBB_D14	B15	FBB_CMD14	FB_B0_CKE_L	70 73 94
FB_B0_DQ<15>	F3	FBB_D15	C17	FBB_CMD15	FB_B0_CAS_L	
FB_B0_DQ<16>	C2	FBB_D16	D18	FBB_CMD16	FB_B1_CS_L	
FB_B0_DQ<17>	D4	FBB_D17	E18	FBB_CMD17	FB_B1_A<3>	76 70 81
FB_B0_DQ<18>	D3	FBB_D18	F18	FBB_CMD18	FB_B1_A<2>	
FB_B0_DQ<19>	C1	FBB_D19	A20	FBB_CMD19	FB_B1_A<4>	
FB_B0_DQ<20>	B3	FBB_D20	B20	FBB_CMD20	FB_B1_A<5>	
FB_B0_DQ<21>	C4	FBB_D21	C18	FBB_CMD21	FB_B1_WE_L	
FB_B0_DQ<22>	B5	FBB_D22	B18	FBB_CMD22	FB_B1_A<7>	
FB_B0_DQ<23>	C5	FBB_D23	G18	FBB_CMD23	FB_B1_A<6>	
FB_B0_DQ<24>	A11	FBB_D24	G17	FBB_CMD24	FB_B1_ABI_L	
FB_B0_DQ<25>	C11	FBB_D25	F17	FBB_CMD25	FB_B1_A<8>	
FB_B0_DQ<26>	D11	FBB_D26	D16	FBB_CMD26	FB_B1_A<0>	
FB_B0_DQ<27>	B11	FBB_D27	A18	FBB_CMD27	FB_B1_A<1>	
FB_B0_DQ<28>	D8	FBB_D28	D17	FBB_CMD28	FB_B1_RAS_L	
FB_B0_DQ<29>	A8	FBB_D29	A17	FBB_CMD29	FB_B1_RESET_L	70 73 94
FB_B0_DQ<30>	C8	FBB_D30	B17	FBB_CMD30	FB_B1_CKE_L	70 73 94
FB_B0_DQ<31>	B8	FBB_D31	E17	FBB_CMD31	FB_B1_CAS_L	
FB_B1_DQ<0>	F24	FBB_D32				
FB_B1_DQ<1>	G23	FBB_D33	D12	FBB_CLK0	FB_B0_CLK_P	
FB_B1_DQ<2>	E24	FBB_D34	E12	FBB_CLK0*	FB_B0_CLK_N	
FB_B1_DQ<3>	G24	FBB_D35	E20	FBB_CLK1	FB_B1_CLK_P	
FB_B1_DQ<4>	D21	FBB_D36	F20	FBB_CLK1*	FB_B1_CLK_N	
FB_B1_DQ<5>	E21	FBB_D37	E11	FBB_DQM0	FB_B0_DBI_L<0>	
FB_B1_DQ<6>	G21	FBB_D38	E3	FBB_DQM1	FB_B0_DBI_L<1>	
FB_B1_DQ<7>	F21	FBB_D39	A3	FBB_DQM2	FB_B0_DBI_L<2>	
FB_B1_DQ<8>	G27	FBB_D40	C9	FBB_DQM3	FB_B0_DBI_L<3>	
FB_B1_DQ<9>	D27	FBB_D41	F23	FBB_DQM4	FB_B1_DBI_L<0>	
FB_B1_DQ<10>	G26	FBB_D42	F27	FBB_DQM5	FB_B1_DBI_L<1>	
FB_B1_DQ<11>	E27	FBB_D43	C30	FBB_DQM6	FB_B1_DBI_L<2>	
FB_B1_DQ<12>	E29	FBB_D44	A24	FBB_DQM7	FB_B1_DBI_L<3>	
FB_B1_DQ<13>	F29	FBB_D45				
FB_B1_DQ<14>	E30	FBB_D46	D9	FBB_DQS_RN0	NC	
FB_B1_DQ<15>	D30	FBB_D47	E4	FBB_DQS_RN1	NC	
FB_B1_DQ<16>	A32	FBB_D48	B2	FBB_DQS_RN2	NC	
FB_B1_DQ<17>	C31	FBB_D49	A9	FBB_DQS_RN3	NC	
FB_B1_DQ<18>	C32	FBB_D50	D22	FBB_DQS_RN4	NC	
FB_B1_DQ<19>	B32	FBB_D51	D28	FBB_DQS_RN5	NC	
FB_B1_DQ<20>	D29	FBB_D52	A30	FBB_DQS_RN6	NC	
FB_B1_DQ<21>	A29	FBB_D53	B23	FBB_DQS_RN7	NC	
FB_B1_DQ<22>	C29	FBB_D54				
FB_B1_DQ<23>	B29	FBB_D55	D10	FBB_DQS_WP0	FB_B0_EDC<0>	
FB_B1_DQ<24>	B21	FBB_D56	D5	FBB_DQS_WP1	FB_B0_EDC<1>	
FB_B1_DQ<25>	C23	FBB_D57	C3	FBB_DQS_WP2	FB_B0_EDC<2>	
FB_B1_DQ<26>	A21	FBB_D58	B9	FBB_DQS_WP3	FB_B0_EDC<3>	
FB_B1_DQ<27>	C21	FBB_D59	E23	FBB_DQS_WP4	FB_B1_EDC<0>	
FB_B1_DQ<28>	B24	FBB_D60	E28	FBB_DQS_WP5	FB_B1_EDC<1>	
FB_B1_DQ<29>	C24	FBB_D61	B30	FBB_DQS_WP6	FB_B1_EDC<2>	
FB_B1_DQ<30>	B26	FBB_D62	A23	FBB_DQS_WP7	FB_B1_EDC<3>	
FB_B1_DQ<31>	C26	FBB_D63				
FB_B0_WCLK_P<0>	F8	FBB_WCK01	H17	70 FBB_PLL_AVDD	PP1V05_GPU_FBB_PLL_AVDD	
FB_B0_WCLK_N<0>	E8	FBB_WCK01*	G14	FBB_DEBUG0	GPU_FBB_DEBUG0	70
FB_B0_WCLK_P<1>	A5	FBB_WCK23	G20	FBB_DEBUG1	GPU_FBB_DEBUG1	70
FB_B0_WCLK_N<1>	A6	FBB_WCK23*	H26	FB_VREF	FB_VREF	70
FB_B1_WCLK_P<0>	D24	FBB_WCK45	C12	FBB_CMD_RFU0	NC	
FB_B1_WCLK_N<0>	D25	FBB_WCK45*	C20	FBB_CMD_RFU1	NC	
FB_B1_WCLK_P<1>	B27	FBB_WCK67				
FB_B1_WCLK_N<1>	C27	FBB_WCK67*				
	D6	FBB_WCKB01				
	D7	FBB_WCKB01*				
	C6	FBB_WCKB23				
	B6	FBB_WCKB23*				
	F26	FBB_WCKB45				
	E26	FBB_WCKB45*				
	A26	FBB_WCKB67				
	A27	FBB_WCKB67*				

C8606 1UF 20% 4V CERM-X6S 0201

C8607 0.1UF 10% 6.3V X6S 0201

=PP1V35_GPU_S0_FB 70 81

R8606 60.4 1% 1/20W MF 201

R8607 60.4 1% 1/20W MF 201

GPU_FBB_DEBUG0 70

GPU_FBB_DEBUG1 70

L8601
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD — 0603 CRITICAL ESR = 0.05OHM — PP1V05_GPU_FB_PLL_AVDD 70

C8601 20UF 20% 2V X6T-CERM 0402

C8602 1UF 20% 4V CERM-X6S 0201

C8603 0.1UF 10% 6.3V X6S 0201

FB PLL & DLL VDD

L8602
FERR-220-OHM-2A
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.05V
=PP1V05_GPU_PEX_IOVDD — 0603 CRITICAL ESR = 0.05OHM — PP1V05_GPU_FB_DLL_AVDD 70

C8608 20UF 20% 2V X6T-CERM 0402

C8604 1UF 20% 4V CERM-X6S 0201

C8605 0.1UF 10% 6.3V X6S 0201

94 73 70 FB_B0_RESET_L — R8654 10K 1% 1/20W MF 201

94 73 70 FB_B1_RESET_L — R8655 10K 1% 1/20W MF 201

70 73 94 FB_B0_CKE_L — R8656 10K 1% 1/20W MF 201

70 73 94 FB_B1_CKE_L — R8657 10K 1% 1/20W MF 201

MEM VREFC & VREFD SWITCH

73 72 FB_SW_LEG

Q8665
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

GPU_ALT_VREF — IN 75

Page Notes

Power aliases required by this page:
- =PP1V35_GPU_S0_FB
- =PP1V05_GPU_PEX_IOVDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	KEPLER FRAME BUFFER I/F
Apple Inc.	DRAWING NUMBER 051-0675 · SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 86 OF 119
	SHEET 70 OF 94

GPU FB SUPPLY

VOUT = 1.5V / 1.35V
13A MAX OUTPUT
F = 500 KHZ

U8750
ISL95870AH
UTQFN
CRITICAL

GPIO(16)	VID1	VID0	FBVDD
	0	0	1.5V
	1	0	1.35V

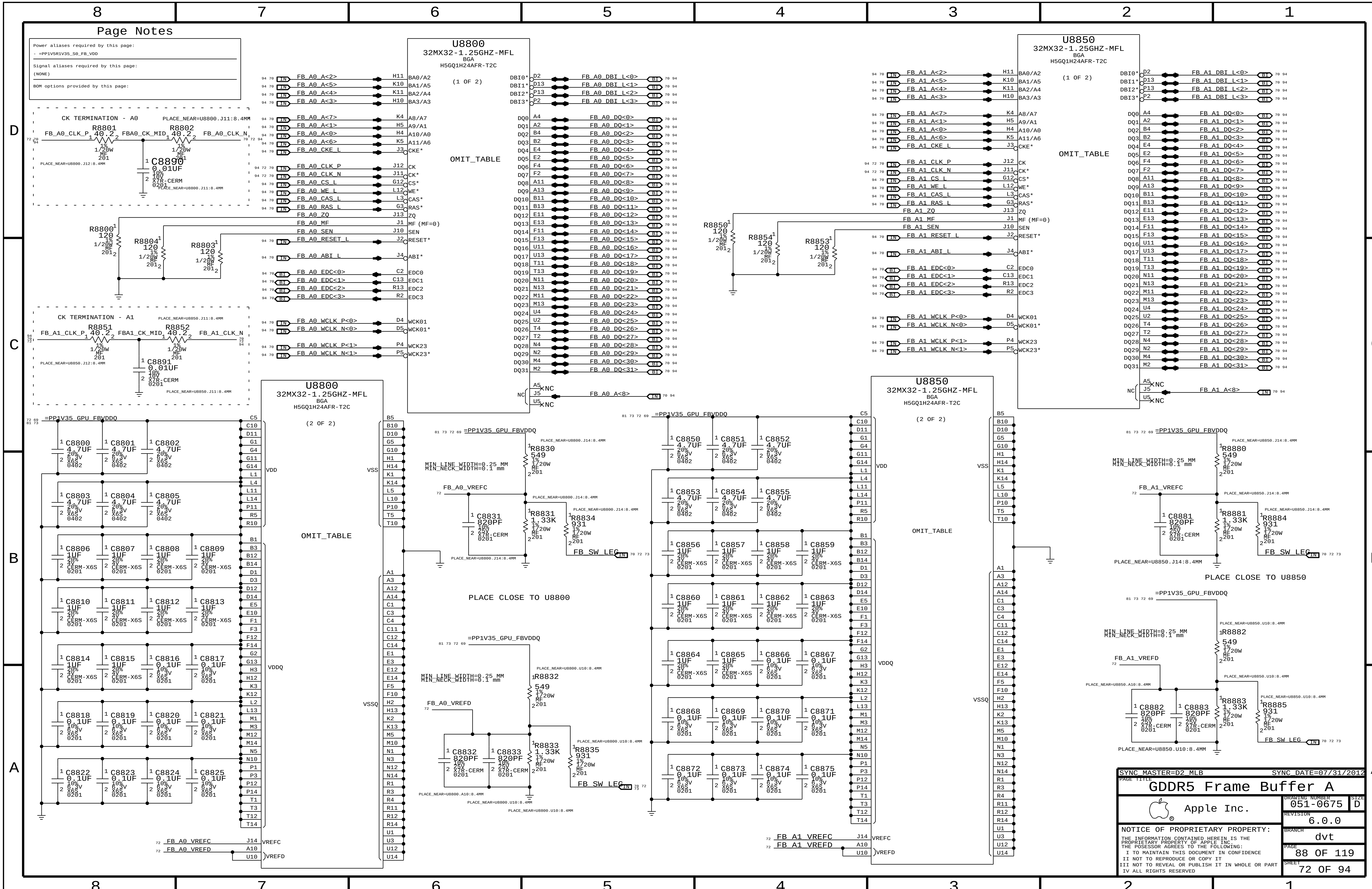
GPU 1V05 SUPPLY

U8710
ISL95870
UTQFN
CRITICAL

VOUT = 1.05V
5.3A MAX OUTPUT
F = 500 KHZ

Vout = 0.5V * (1 + Ra / Rb)

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	1V05 GPU / 1V35 FB POWER SUPPLY
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 87 OF 119
	SHEET 71 OF 94


Page Notes
Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD
Signal aliases required by this page:
(NONE)
BOM options provided by this page:
CK TERMINATION - A0
CK TERMINATION - A1
U8800
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
(2 OF 2)
OMIT_TABLE
U8850
=PP1V35_GPU_FBVDDQ
FB_A0_VREFC
FB_A0_VREFD
FB_A1_VREFC
FB_A1_VREFD
FB_SW_LEG
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 mm
PLACE CLOSE TO U8800
PLACE CLOSE TO U8850
VDD
VSS
VDDQ
VSSQ
SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012
PAGE TITLE
GDDR5 Frame Buffer A
Apple Inc.
DRAWING NUMBER
051-0675
SIZE
D
REVISION
6.0.0
BRANCH
dvt
PAGE
88 OF 119
SHEET
72 OF 94
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Page Notes

Power aliases required by this page:
- =PP1V5R1V35_S0_FB_VDD

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

CK TERMINATION - B0

R8901 40.2 1% 1/20W MF 201 — FB_B0_CLK_P — FBB0_CK_MID — R8902 40.2 1% 1/20W MF 201 — FB_B0_CLK_N
PLACE_NEAR=U8900.J12:8.4MM
PLACE_NEAR=U8900.J11:8.4MM
C8990 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8900.J11:8.4MM

R8900 120 1% 1/20W MF 201
R8904 120 1% 1/20W MF 201
R8903 120 1% 1/20W MF 201

CK TERMINATION - B1

R8951 40.2 1% 1/20W MF 201 — FB_B1_CLK_P — FBB1_CK_MID — R8952 40.2 1% 1/20W MF 201 — FB_B1_CLK_N
PLACE_NEAR=U8950.J12:8.4MM
PLACE_NEAR=U8950.J11:8.4MM
C8991 0.01UF 10% 10V X7R-CERM 0201
PLACE_NEAR=U8950.J11:8.4MM

U8900
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C

(1 OF 2)

FB_B0_A<2>	H11	BA0/A2	
FB_B0_A<5>	K10	BA1/A5	
FB_B0_A<4>	K11	BA2/A4	
FB_B0_A<3>	H10	BA3/A3	
FB_B0_A<7>	K4	A8/A7	
FB_B0_A<1>	H5	A9/A1	
FB_B0_A<0>	H4	A10/A0	
FB_B0_A<6>	K5	A11/A6	
FB_B0_CKE_L	J3	CKE*	
FB_B0_CLK_P	J12	CK	
FB_B0_CLK_N	J11	CK*	
FB_B0_CS_L	G12	CS*	
FB_B0_WE_L	L12	WE*	
FB_B0_CAS_L	L3	CAS*	
FB_B0_RAS_L	G3	RAS*	
FB_B0_ZQ	J13	ZQ	
FB_B0_MF	J1	MF (MF=0)	
FB_B0_SEN	J10	SEN	
FB_B0_RESET_L	J2	RESET*	
FB_B0_ABI_L	J4	ABI*	
FB_B0_EDC<0>	C2	EDC0	
FB_B0_EDC<1>	C13	EDC1	
FB_B0_EDC<2>	R13	EDC2	
FB_B0_EDC<3>	R2	EDC3	
FB_B0_WCLK_P<0>	D4	WCK01	
FB_B0_WCLK_N<0>	D5	WCK01*	
FB_B0_WCLK_P<1>	P4	WCK23	
FB_B0_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_B0_DBI_L<0>	
DBI1*	D13	FB_B0_DBI_L<1>	
DBI2*	P13	FB_B0_DBI_L<2>	
DBI3*	P2	FB_B0_DBI_L<3>	
DQ0	A4	FB_B0_DQ<0>	
DQ1	A2	FB_B0_DQ<1>	
DQ2	B4	FB_B0_DQ<2>	
DQ3	B2	FB_B0_DQ<3>	
DQ4	E4	FB_B0_DQ<4>	
DQ5	E2	FB_B0_DQ<5>	
DQ6	F4	FB_B0_DQ<6>	
DQ7	F2	FB_B0_DQ<7>	
DQ8	A11	FB_B0_DQ<8>	
DQ9	A13	FB_B0_DQ<9>	
DQ10	B11	FB_B0_DQ<10>	
DQ11	B13	FB_B0_DQ<11>	
DQ12	E11	FB_B0_DQ<12>	
DQ13	E13	FB_B0_DQ<13>	
DQ14	F11	FB_B0_DQ<14>	
DQ15	F13	FB_B0_DQ<15>	
DQ16	U11	FB_B0_DQ<16>	
DQ17	U13	FB_B0_DQ<17>	
DQ18	T11	FB_B0_DQ<18>	
DQ19	T13	FB_B0_DQ<19>	
DQ20	N11	FB_B0_DQ<20>	
DQ21	N13	FB_B0_DQ<21>	
DQ22	M11	FB_B0_DQ<22>	
DQ23	M13	FB_B0_DQ<23>	
DQ24	U4	FB_B0_DQ<24>	
DQ25	U2	FB_B0_DQ<25>	
DQ26	T4	FB_B0_DQ<26>	
DQ27	T2	FB_B0_DQ<27>	
DQ28	N4	FB_B0_DQ<28>	
DQ29	N2	FB_B0_DQ<29>	
DQ30	M4	FB_B0_DQ<30>	
DQ31	M2	FB_B0_DQ<31>	
NC	A5	NC	
NC	J5	NC	
NC	U5	NC	

OMIT_TABLE

U8950
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C

(1 OF 2)

FB_B1_A<2>	H11	BA0/A2	
FB_B1_A<5>	K10	BA1/A5	
FB_B1_A<4>	K11	BA2/A4	
FB_B1_A<3>	H10	BA3/A3	
FB_B1_A<7>	K4	A8/A7	
FB_B1_A<1>	H5	A9/A1	
FB_B1_A<0>	H4	A10/A0	
FB_B1_A<6>	K5	A11/A6	
FB_B1_CKE_L	J3	CKE*	
FB_B1_CLK_P	J12	CK	
FB_B1_CLK_N	J11	CK*	
FB_B1_CS_L	G12	CS*	
FB_B1_WE_L	L12	WE*	
FB_B1_CAS_L	L3	CAS*	
FB_B1_RAS_L	G3	RAS*	
FB_B1_ZQ	J13	ZQ	
FB_B1_MF	J1	MF (MF=0)	
FB_B1_SEN	J10	SEN	
FB_B1_RESET_L	J2	RESET*	
FB_B1_ABI_L	J4	ABI*	
FB_B1_EDC<0>	C2	EDC0	
FB_B1_EDC<1>	C13	EDC1	
FB_B1_EDC<2>	R13	EDC2	
FB_B1_EDC<3>	R2	EDC3	
FB_B1_WCLK_P<0>	D4	WCK01	
FB_B1_WCLK_N<0>	D5	WCK01*	
FB_B1_WCLK_P<1>	P4	WCK23	
FB_B1_WCLK_N<1>	P5	WCK23*	

OMIT_TABLE

DBI0*	D2	FB_B1_DBI_L<0>	
DBI1*	D13	FB_B1_DBI_L<1>	
DBI2*	P13	FB_B1_DBI_L<2>	
DBI3*	P2	FB_B1_DBI_L<3>	
DQ0	A4	FB_B1_DQ<0>	
DQ1	A2	FB_B1_DQ<1>	
DQ2	B4	FB_B1_DQ<2>	
DQ3	B2	FB_B1_DQ<3>	
DQ4	E4	FB_B1_DQ<4>	
DQ5	E2	FB_B1_DQ<5>	
DQ6	F4	FB_B1_DQ<6>	
DQ7	F2	FB_B1_DQ<7>	
DQ8	A11	FB_B1_DQ<8>	
DQ9	A13	FB_B1_DQ<9>	
DQ10	B11	FB_B1_DQ<10>	
DQ11	B13	FB_B1_DQ<11>	
DQ12	E11	FB_B1_DQ<12>	
DQ13	E13	FB_B1_DQ<13>	
DQ14	F11	FB_B1_DQ<14>	
DQ15	F13	FB_B1_DQ<15>	
DQ16	U11	FB_B1_DQ<16>	
DQ17	U13	FB_B1_DQ<17>	
DQ18	T11	FB_B1_DQ<18>	
DQ19	T13	FB_B1_DQ<19>	
DQ20	N11	FB_B1_DQ<20>	
DQ21	N13	FB_B1_DQ<21>	
DQ22	M11	FB_B1_DQ<22>	
DQ23	M13	FB_B1_DQ<23>	
DQ24	U4	FB_B1_DQ<24>	
DQ25	U2	FB_B1_DQ<25>	
DQ26	T4	FB_B1_DQ<26>	
DQ27	T2	FB_B1_DQ<27>	
DQ28	N4	FB_B1_DQ<28>	
DQ29	N2	FB_B1_DQ<29>	
DQ30	M4	FB_B1_DQ<30>	
DQ31	M2	FB_B1_DQ<31>	
NC	A5	NC	
NC	J5	NC	
NC	U5	NC	

U8900
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C

(2 OF 2)

OMIT_TABLE

VDD	C5	C10	
	D11	G1	
	G4	G11	
	G14	L1	
	L4	L11	
	L14	P11	
	R5	R10	
VDDQ	B1	B3	
	B12	B14	
	D1	D3	
	D12	D14	
	E5	E10	
	F1	F3	
	F12	F14	
	G2	G13	
	H3	H12	
	K3	K12	
	L2	L13	
	M1	M3	
	M12	M14	
	N5	N10	
	P1	P3	
	P12	P14	
	T1	T3	
	T12	T14	
VSS	B5	B10	
	D10	G5	
	G10	H1	
	H14	K1	
	K14	L5	
	L10	P10	
	T5	T10	
VSSQ	A1	A3	
	A12	A14	
	C1	C3	
	C4	C11	
	C12	C14	
	E1	E3	
	E12	E14	
	F5	F10	
	H2	H13	
	K2	K13	
	M5	M10	
	N1	N3	
	N12	N14	
	R1	R3	
	R4	R11	
	R12	R14	
	U1	U3	
	U12	U14	
VREFC	J14	FB_B0_VREFC	
VREFD	A10	FB_B0_VREFD	
	U10		

U8950
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C

(2 OF 2)

OMIT_TABLE

VDD	C5	C10	
	D11	G1	
	G4	G11	
	G14	L1	
	L4	L11	
	L14	P11	
	R5	R10	
VDDQ	B1	B3	
	B12	B14	
	D1	D3	
	D12	D14	
	E5	E10	
	F1	F3	
	F12	F14	
	G2	G13	
	H3	H12	
	K3	K12	
	L2	L13	
	M1	M3	
	M12	M14	
	N5	N10	
	P1	P3	
	P12	P14	
	T1	T3	
	T12	T14	
VSS	B5	B10	
	D10	G5	
	G10	H1	
	H14	K1	
	K14	L5	
	L10	P10	
	T5	T10	
VSSQ	A1	A3	
	A12	A14	
	C1	C3	
	C4	C11	
	C12	C14	
	E1	E3	
	E12	E14	
	F5	F10	
	H2	H13	
	K2	K13	
	M5	M10	
	N1	N3	
	N12	N14	
	R1	R3	
	R4	R11	
	R12	R14	
	U1	U3	
	U12	U14	
VREFC	J14	FB_B1_VREFC	
VREFD	A10	FB_B1_VREFD	
	U10		

=PP1V35_GPU_FBVDDQ

C8900 4.7UF 20% 6.3V X6S 0402
C8901 4.7UF 20% 6.3V X6S 0402
C8902 4.7UF 20% 6.3V X6S 0402
C8903 4.7UF 20% 6.3V X6S 0402
C8904 4.7UF 20% 6.3V X6S 0402
C8905 4.7UF 20% 6.3V X6S 0402
C8906 1UF 20% 4V CERM-X6S 0201
C8907 1UF 20% 4V CERM-X6S 0201
C8908 1UF 20% 4V CERM-X6S 0201
C8909 1UF 20% 4V CERM-X6S 0201
C8910 1UF 20% 4V CERM-X6S 0201
C8911 1UF 20% 4V CERM-X6S 0201
C8912 1UF 20% 4V CERM-X6S 0201
C8913 1UF 20% 4V CERM-X6S 0201
C8914 1UF 20% 4V CERM-X6S 0201
C8915 1UF 20% 4V CERM-X6S 0201
C8916 0.1UF 10% 6.3V X6S 0201
C8917 0.1UF 10% 6.3V X6S 0201
C8918 0.1UF 10% 6.3V X6S 0201
C8919 0.1UF 10% 6.3V X6S 0201
C8920 0.1UF 10% 6.3V X6S 0201
C8921 0.1UF 10% 6.3V X6S 0201
C8922 0.1UF 10% 6.3V X6S 0201
C8923 0.1UF 10% 6.3V X6S 0201
C8924 0.1UF 10% 6.3V X6S 0201
C8925 0.1UF 10% 6.3V X6S 0201

PLACE CLOSE TO U8900

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8930 549 1% 1/20W MF 201 — PLACE_NEAR=U8900.J14:8.4MM
FB_B0_VREFC
C8931 820PF 10% 25V X7R-CERM 0201
R8931 1.33K 1% 1/20W MF 201
R8934 931 1% 1/20W MF 201 — FB_SW_LEG
PLACE_NEAR=U8900.J14:8.4MM

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8932 549 1% 1/20W MF 201 — PLACE_NEAR=U8900.U10:8.4MM
FB_B0_VREFD
C8932 820PF 10% 25V X7R-CERM 0201
C8933 820PF 10% 25V X7R-CERM 0201
R8933 1.33K 1% 1/20W MF 201
R8935 931 1% 1/20W MF 201 — FB_SW_LEG
PLACE_NEAR=U8900.U10:8.4MM
PLACE_NEAR=U8900.A10:8.4MM

=PP1V35_GPU_FBVDDQ

C8950 4.7UF 20% 6.3V X6S 0402
C8951 4.7UF 20% 6.3V X6S 0402
C8952 4.7UF 20% 6.3V X6S 0402
C8953 4.7UF 20% 6.3V X6S 0402
C8954 4.7UF 20% 6.3V X6S 0402
C8955 4.7UF 20% 6.3V X6S 0402
C8956 1UF 20% 4V CERM-X6S 0201
C8957 1UF 20% 4V CERM-X6S 0201
C8958 1UF 20% 4V CERM-X6S 0201
C8959 1UF 20% 4V CERM-X6S 0201
C8960 1UF 20% 4V CERM-X6S 0201
C8961 1UF 20% 4V CERM-X6S 0201
C8962 1UF 20% 4V CERM-X6S 0201
C8963 1UF 20% 4V CERM-X6S 0201
C8964 1UF 20% 4V CERM-X6S 0201
C8965 1UF 20% 4V CERM-X6S 0201
C8966 0.1UF 10% 6.3V X6S 0201
C8967 0.1UF 10% 6.3V X6S 0201
C8968 0.1UF 10% 6.3V X6S 0201
C8969 0.1UF 10% 6.3V X6S 0201
C8970 0.1UF 10% 6.3V X6S 0201
C8971 0.1UF 10% 6.3V X6S 0201
C8972 0.1UF 10% 6.3V X6S 0201
C8973 0.1UF 10% 6.3V X6S 0201
C8974 0.1UF 10% 6.3V X6S 0201
C8975 0.1UF 10% 6.3V X6S 0201

R8950 120 1% 1/20W MF 201
R8954 120 1% 1/20W MF 201
R8953 120 1% 1/20W MF 201

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8980 549 1% 1/20W MF 201 — PLACE_NEAR=U8950.J14:8.4MM
FB_B1_VREFC
C8981 820PF 10% 25V X7R-CERM 0201
R8981 1.33K 1% 1/20W MF 201
R8984 931 1% 1/20W MF 201 — FB_SW_LEG
PLACE_NEAR=U8950.J14:8.4MM

PLACE CLOSE TO U8950

=PP1V35_GPU_FBVDDQ
MIN_LINE_WIDTH=0.25 MM
MIN_NECK_WIDTH=0.1 MM
R8982 549 1% 1/20W MF 201 — PLACE_NEAR=U8950.U10:8.4MM
FB_B1_VREFD
C8982 820PF 10% 25V X7R-CERM 0201
C8983 820PF 10% 25V X7R-CERM 0201
R8983 1.33K 1% 1/20W MF 201
R8985 931 1% 1/20W MF 201 — FB_SW_LEG
PLACE_NEAR=U8950.A10:8.4MM
PLACE_NEAR=U8950.U10:8.4MM

SYNC_MASTER=D2_MLB	SYNC_DATE=07/31/2012
PAGE TITLE	GDDR5 Frame Buffer B
Apple Inc.	DRAWING NUMBER 051-0675 SIZE D
	REVISION 6.0.0
	BRANCH dvt
	PAGE 89 OF 119
	SHEET 73 OF 94

PD FOR AUX CHANNELS (FOR NVIDIA)

DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_TBTSNK0_EG_AUXCH_P
DP_TBTSNK0_EG_AUXCH_N
DP_TBTSNK1_EG_AUXCH_P
DP_TBTSNK1_EG_AUXCH_N
HDMI_EG_DDC_CLK_Q
HDMI_EG_DDC_DATA_Q

R9001 10K 1% 1/20W MF 201 — DISABLE PHY A & B FOR 15" MBP
R9002 10K 1% 1/20W MF 201
R9003 10K 1% 1/20W MF 201
R9008 10K 1% 1/20W MF 201
R9014 100K 1% 1/20W MF 201
R9013 100K 1% 1/20W MF 201
R9015 100K 1% 1/20W MF 201
R9016 100K 1% 1/20W MF 201
R9017 100K 1% 1/20W MF 201
R9018 100K 1% 1/20W MF 201
R9027 100K 1% 1/20W MF 201 — NO STUFF
R9028 100K 1% 1/20W MF 201 — NO STUFF
R9021 1K 1% 1/20W MF 201 — IFPC_RSET, PLACE_NEAR=U8400.AF8:5MM
R9006 1K 1% 1/20W MF 201 — IFPD_RSET, PLACE_NEAR=U8400.AN2:5MM
R9007 1K 1% 1/20W MF 201 — IFPEF_RSET, PLACE_NEAR=U8400.AD6:5MM
R9023 4.7K 1% 1/20W MF 201
R9024 4.7K 1% 1/20W MF 201
R9025 4.7K 1% 1/20W MF 201
R9026 4.7K 1% 1/20W MF 201
R9011 10K 1% 1/20W MF 201
R9012 10K 1% 1/20W MF 201

PD FOR RSET

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_IFP8_IOVDD
- =PP1V8_GPU_IFPA_IOVDD
- =PP1V8_GPU_DPLL
- =PP1V05_GPU_DPLL
- =PP3V3_GPU_IFPX_PLLVDD
- =PP1V05_GPU_IFPCD_IOVDD
- =PP1V05_GPU_IFPEF_IOVDD
- =PP3V3_GPU_VDD33

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- J31:YES
- D2:YES

PP1V05_GPU_SP_PLLVDD = PP1V05_GPU_VID_PLLVDD (MAKE_BASE=TRUE)

GPU_OSC_27M_XTAL_BUFFOUT_R — PLACE_NEAR=U8400.J4:8.4MM
GPU_OSC_27M_SSIN — PLACE_NEAR=U8400.H1:8.4MM

OMIT_TABLE

U8400
NV-GK107
BGA
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PP1V8_GPU_IFPA_IOVDD	AG8	IFPA_IOVDD	IFPA_TXC / IFPA_TXC* AM6 AN6
PP3V3_GPU_IFPB_IOVDD	AG9	IFPB_IOVDD	IFPA_TXD0 / IFPA_TXD0* AP3 AN3
PP1V05_GPU_IFPCD_IOVDD	AF6	IFPC_IOVDD	IFPA_TXD1 / IFPA_TXD1* AN5 AM5
PP1V05_GPU_IFPCD_IOVDD	AG6	IFPD_IOVDD	IFPA_TXD2 / IFPA_TXD2* AL6 AK6
PP1V05_GPU_IFPEF_IOVDD	AC7	IFPE_IOVDD	IFPA_TXD3 / IFPA_TXD3* AJ6 AH6
PP1V05_GPU_IFPEF_IOVDD	AC8	IFPF_IOVDD	IFPB_TXC / IFPB_TXC* AJ9 AH9
PP1V05_GPU_IFPAB_PLLVDD	AH8	IFPAB_PLLVDD	IFPB_TXD4 / IFPB_TXD4* AP6 AP5
NC	AJ8	IFPAB_RSET	IFPB_TXD5 / IFPB_TXD5* AM7 AL7
PP3V3_GPU_IFPX_PLLVDD	AF7	IFPC_PLLVDD	IFPB_TXD6 / IFPB_TXD6* AN8 AM8
IFPC_RSET	AF8	IFPC_RSET	IFPB_TXD7 / IFPB_TXD7* AK8 AL8
PP3V3_GPU_IFPX_PLLVDD	AG7	IFPD_PLLVDD	
IFPD_RSET	AN2	IFPD_RSET	
PP3V3_GPU_IFPX_PLLVDD	AB8	IFPEF_PLLVDD	
IFPEF_RSET	AD6	IFPEF_RSET	

=PP3V3_GPU_VDD33

DDC 3.3V/5V LEVEL TRANSLATOR

Q9000 DMN5L06VK-7 SOT-563 — HDMI_EG_DDC_CLK
Q9000 DMN5L06VK-7 SOT-563 — HDMI_EG_DDC_DATA

DPA_EG_DDC_CLK	R4	I2CA_SCL
DPA_EG_DDC_DATA	R5	I2CA_SDA
GPU_SSC_SMB_CLK	R2	I2CC_SCL
GPU_SSC_SMB_DAT	R3	I2CC_SDA
GPU_SMB_CLK	T4	I2CS_SCL
GPU_SMB_DAT	T3	I2CS_SDA
DPB_EG_DDC_CLK	R7	I2CB_SCL
DPB_EG_DDC_DATA	R6	I2CB_SDA

DDC MAPPING
I2CA -> IFPE
I2CB -> IFPF
I2CC -> SSC CLK GEN

IFPC_AUX_I2CW_SCL	AG3	HDMI_EG_DDC_CLK_Q
IFPC_AUX_I2CW_SDA*	AG2	HDMI_EG_DDC_DATA_Q
IFPC_L0 / IFPC_L0*	AK1 AJ1	HDMI_EG_DATA_C_P<2> / HDMI_EG_DATA_C_N<2>
IFPC_L1 / IFPC_L1*	AJ3 AJ2	HDMI_EG_DATA_C_P<1> / HDMI_EG_DATA_C_N<1>
IFPC_L2 / IFPC_L2*	AH3 AH4	HDMI_EG_DATA_C_P<0> / HDMI_EG_DATA_C_N<0>
IFPC_L3 / IFPC_L3*	AG5 AG4	HDMI_EG_CLK_C_P / HDMI_EG_CLK_C_N
IFPD_AUX_I2CX_SCL	AK3	DP_INT_EG_AUX_P
IFPD_AUX_I2CX_SDA*	AK2	DP_INT_EG_AUX_N
IFPD_L0 / IFPD_L0*	AM1 AM2	DP_INT_EG_ML_P<0> / DP_INT_EG_ML_N<0>
IFPD_L1 / IFPD_L1*	AM3 AM4	DP_INT_EG_ML_P<1> / DP_INT_EG_ML_N<1>
IFPD_L2 / IFPD_L2*	AL3 AL4	DP_INT_EG_ML_P<2> / DP_INT_EG_ML_N<2>
IFPD_L3 / IFPD_L3*	AK4 AK5	DP_INT_EG_ML_P<3> / DP_INT_EG_ML_N<3>
IFPE_AUX_I2CY_SCL	AB3	DP_TBTSNK0_EG_AUXCH_P
IFPE_AUX_I2CY_SDA*	AB4	DP_TBTSNK0_EG_AUXCH_N
IFPE_L0 / IFPE_L0*	AD2 AD3	DP_TBTSNK0_ML_C_P<0> / DP_TBTSNK0_ML_C_N<0>
IFPE_L1 / IFPE_L1*	AD1 AC1	DP_TBTSNK0_ML_C_P<1> / DP_TBTSNK0_ML_C_N<1>
IFPE_L2 / IFPE_L2*	AC2 AC3	DP_TBTSNK0_ML_C_P<2> / DP_TBTSNK0_ML_C_N<2>
IFPE_L3 / IFPE_L3*	AC4 AC5	DP_TBTSNK0_ML_C_P<3> / DP_TBTSNK0_ML_C_N<3>
IFPF_AUX_I2CZ_SCL	AF3	DP_TBTSNK1_EG_AUXCH_P
IFPF_AUX_I2CZ_SDA*	AF2	DP_TBTSNK1_EG_AUXCH_N
IFPF_L0 / IFPF_L0*	AE3 AE4	DP_TBTSNK1_ML_C_P<0> / DP_TBTSNK1_ML_C_N<0>
IFPF_L1 / IFPF_L1*	AF4 AF5	DP_TBTSNK1_ML_C_P<1> / DP_TBTSNK1_ML_C_N<1>
IFPF_L2 / IFPF_L2*	AD4 AD5	DP_TBTSNK1_ML_C_P<2> / DP_TBTSNK1_ML_C_N<2>
IFPF_L3 / IFPF_L3*	AG1 AF1	DP_TBTSNK1_ML_C_P<3> / DP_TBTSNK1_ML_C_N<3>

DAC_AVDD	AG10	DACA_VDD
	AK9	DACA_RED
	AL10	DACA_GREEN
	AL9	DACA_BLUE
R9000 10K 1% 1/20W MF 201	AP9	DACA_VREF
	AP8	DACA_RSET
	AM9	DACA_HSYNC
	AN9	DACA_VSYNC
	L3	CEC

OMIT_TABLE

U8400
NV-GK107
BGA
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=PP3V3_GPU_MISC	J8	
=PP3V3_GPU_VDD33	K8 L8 M8	VDD33
GPU_ROM_CS_L	H6	ROM_CS*
GPU_ROM_SCLK	H4	ROM_SCLK
GPU_ROM_SI	H5	ROM_SI
GPU_ROM_SO	H7	ROM_SO
R9009 40.2K 0.1% 1/20W MF 0201	J1	MULTI_STRAP_REF0_GND
MULTI_STRAP_REF		
GPU_TESTMODE	AK11	TESTMODE
PP1V05_GPU_SP_PLLVDD	AE8	SP_PLLVDD
PP1V05_GPU_PLLVDD	AD8	PLLVDD
PP1V05_GPU_VID_PLLVDD	AD7	VID_PLLVDD
GPU_OSC_27M_XTALIN	H3	XTAL_IN
GPU_OSC_27M_XTALOUT	H2	XTAL_OUT
GPU_OSC_27M_XTAL_BUFFOUT_R	J4	XTAL_OUTBUFF
GPU_OSC_27M_SSIN	H1	XTAL_SSIN
GPU_MLS_STRAP0	J2	STRAP0
GPU_MLS_STRAP1	J7	STRAP1
GPU_MLS_STRAP2	J6	STRAP2
GPU_MLS_STRAP3	J5	STRAP3
GPU_MLS_STRAP4	J3	STRAP4

GPIO0	P6	GPU_GPIO_0
GPIO1	M3	GPU_GPIO_1
GPIO2	L6	GPU_GPIO_2
GPIO3	P5	GPU_GPIO_3
GPIO4	P7	GPU_GPIO_4
GPIO5	L7	GPU_GPIO_5
GPIO6	M7	GPU_GPIO_6
GPIO7	N8	GPU_GPIO_7
GPIO8	M1	GPU_GPIO_8
GPIO9	M2	GPU_GPIO_9
GPIO10	L1	GPU_GPIO_10
GPIO11	M5	GPU_GPIO_11
GPIO12	N3	GPU_GPIO_12
GPIO13	M4	GPU_GPIO_13
GPIO14	N4	GPU_GPIO_14
GPIO15	P2	GPU_GPIO_15
GPIO16	R8	GPU_GPIO_16
GPIO17	M6	GPU_GPIO_17
GPIO18	R1	GPU_GPIO_18
GPIO19	P3	GPU_GPIO_19
GPIO20	P4	GPU_GPIO_20
GPIO21	P1	GPU_GPIO_21
JTAG_TCK	AM10	GPU_JTAG_TCK
JTAG_TDI	AM11	GPU_JTAG_TDI
JTAG_TDO	AP12	GPU_JTAG_TDO
JTAG_TMS	AP11	GPU_JTAG_TMS
JTAG_TRST*	AN11	GPU_JTAG_TRST_L
THERMDP	K3	GPU_TDIODE_P
THERMDN	K4	GPU_TDIODE_N

CRITICAL
L9004 330-OHM-1.2A 0603 — =PP3V3_GPU_IFPX_PLLVDD → PP3V3_GPU_IFPX_PLLVDD
IFPX PLLVDD
C9010 10UF 20% 10V X6S-CERM 0603
C9011 1UF 10% 25V X6S-CERM 0402
C9012 0.1UF 20% 16V X6S-CERM 0201

PLACE BELOW GPU NEAR DISPLAY SECTION

C9013 10UF 20% 10V X6S-CERM 0603
C9019 4.7UF 10% 6.3V X6S-CERM 0603
C9015 1UF 10% 25V X6S-CERM 0402
C9016 1UF 10% 25V X6S-CERM 0402
C9017 0.1UF 20% 16V X6S-CERM 0201
C9018 0.1UF 20% 16V X6S-CERM 0201

L9005 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM — =PP1V05_GPU_IFPCD_IOVDD → PP1V05_GPU_IFPCD_IOVDD
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
IFP CD IOVDD
C9025 4.7UF 20% 6.3V X6S 0402
C9026 1UF 20% 4V CERM-X6S 0201
C9027 0.1UF 20% 16V X6S-CERM 0201
C9028 0.1UF 20% 16V X6S-CERM 0201
C9055 10UF 20% 4V X6S-CERM 0402-1
C9056 1UF 20% 4V CERM-X6S 0201
C9057 0.1UF 20% 16V X6S-CERM 0201
C9058 0.1UF 20% 16V X6S-CERM 0201

L9006 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM — =PP1V05_GPU_IFPEF_IOVDD → PP1V05_GPU_IFPEF_IOVDD
MIN_LINE_WIDTH=0.5 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
IFP EF IOVDD
C9029 10UF 20% 4V X6S-CERM 0402-1
C9030 1UF 20% 4V CERM-X6S 0201
C9031 0.1UF 20% 16V X6S-CERM 0201
C9032 0.1UF 20% 16V X6S-CERM 0201
C9033 4.7UF 20% 6.3V X6S 0402
C9034 4.7UF 20% 6.3V X6S 0402
C9035 1UF 20% 4V CERM-X6S 0201
C9036 1UF 20% 4V CERM-X6S 0201
C9037 0.1UF 20% 16V X6S-CERM 0201
C9038 0.1UF 20% 16V X6S-CERM 0201

GPU PLL VDD
L9007 FERR-220-OHM-2A 0603 CRITICAL ESR = 0.050OHM — =PP1V05_GPU_PEX_PLLVDD → PP1V05_GPU_PLLVDD
MIN_LINE_WIDTH=0.41 MM MIN_NECK_WIDTH=0.2 MM VOLTAGE=1.05V
C9051 20UF 20% 2V X6T-CERM 0402
C9052 1UF 20% 4V CERM-X6S 0201
C9053 0.1UF 20% 16V X6S-CERM 0201
C9054 0.1UF 20% 16V X6S-CERM 0201

GPU 3V3 VDD
=PP3V3_GPU_VDD33
C9040 10UF 20% 10V X6S-CERM 0603
C9041 1UF 10% 25V X6S-CERM 0402
C9042 1UF 10% 25V X6S-CERM 0402
C9043 0.1UF 20% 16V X6S-CERM 0201
C9044 0.1UF 20% 16V X6S-CERM 0201
=PP3V3_GPU_MISC
C9045 4.7UF 20% 6.3V X6S 0402
C9046 4.7UF 20% 6.3V X6S 0402
C9049 0.1UF 20% 16V X6S-CERM 0201
C9050 0.1UF 20% 16V X6S-CERM 0201

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012
PAGE TITLE: KEPLER EDP/DP/GPIO
Apple Inc.
DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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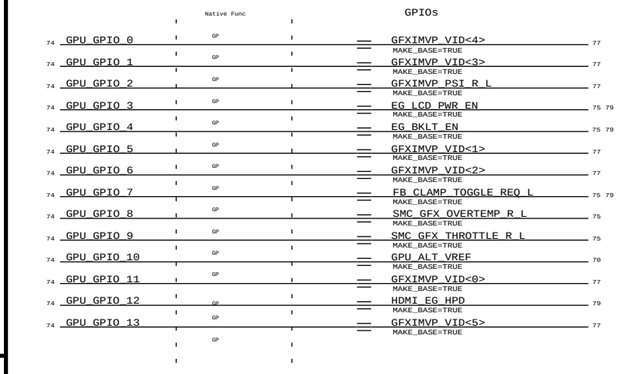
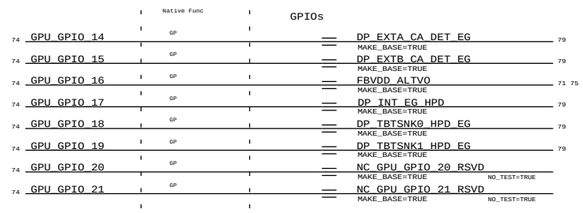
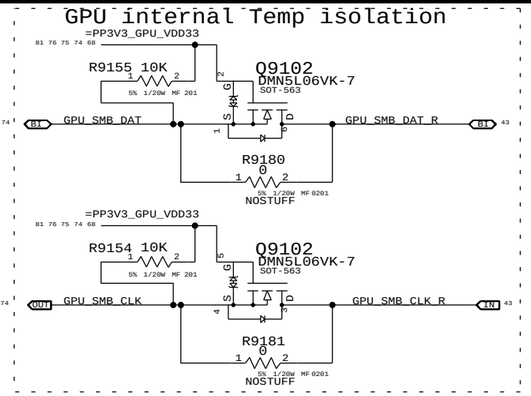
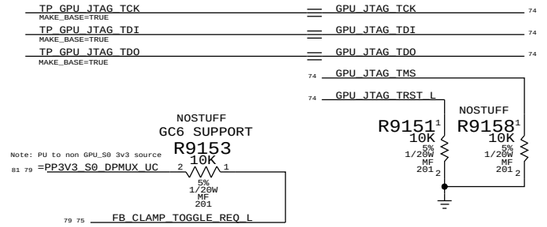
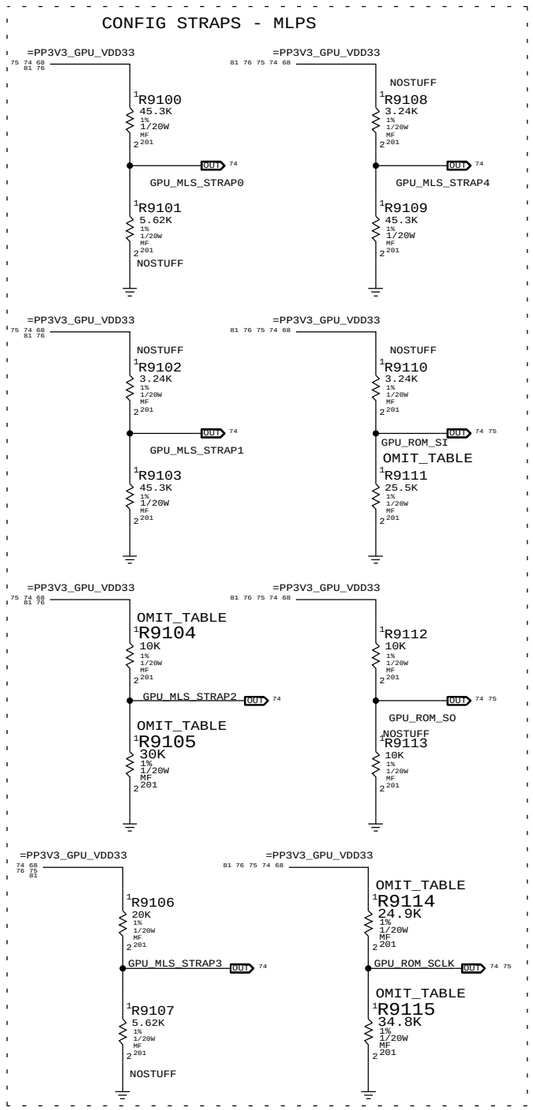


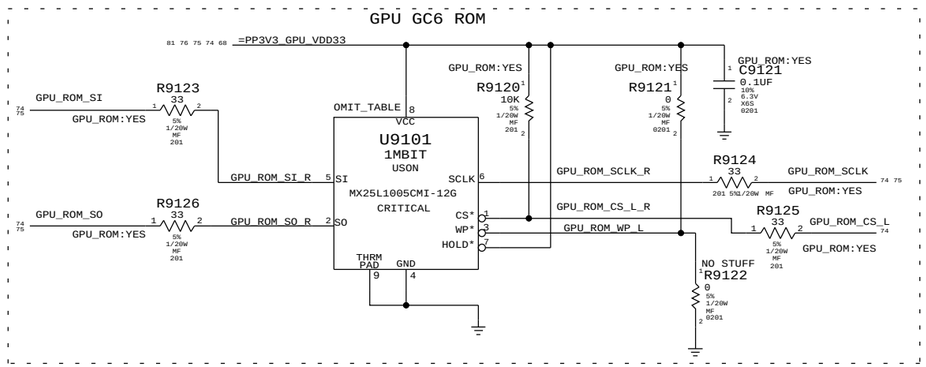






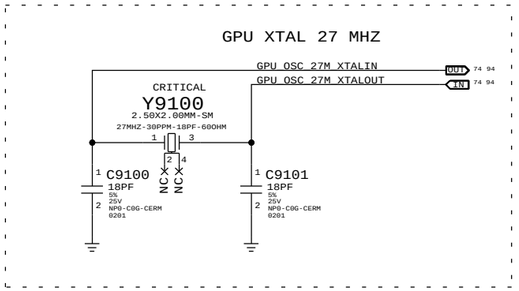


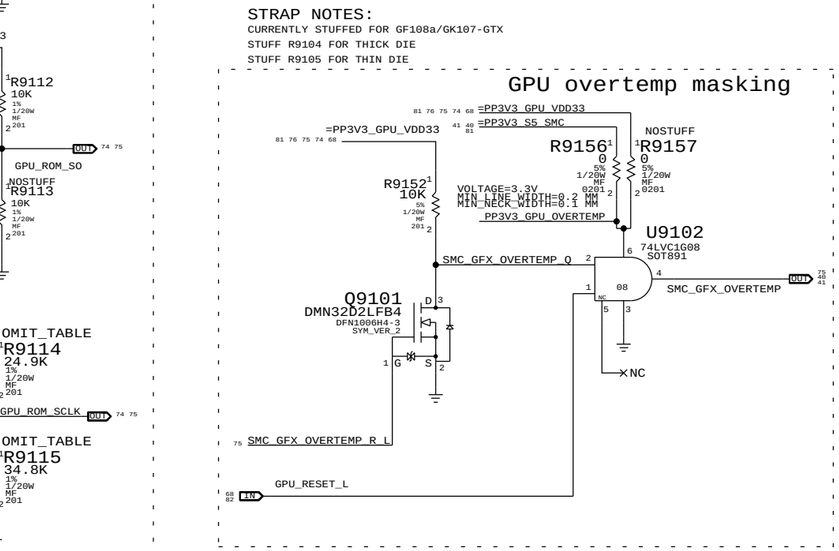
Straps for GK107. GF108 support has been removed.

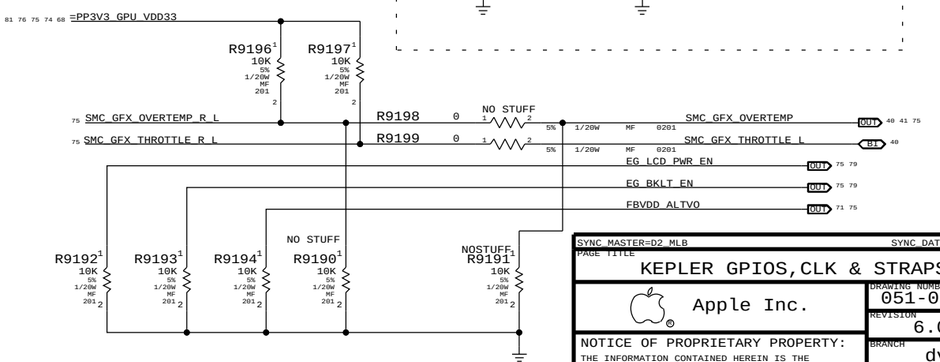


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
118S0230	1	RES,MF,24.9KOHM,1,1/20W,0201,1%	R9111		FB_2G_HYNIX_A_DIE
118S0280	1	RES,MF,30.1KOHM,1,1/20W,0201,1%	R9111		FB_2G_ELPIDA
118S0013	1	RES, 10KOHM, 0201,1%	R9111		FB_2G_HYNIX_29nm
118S0409	1	RES, 4.99 KOHM, 0201,1%	R9111		FB_2G_ELPIDA_29nm
118S0105	1	RES, 15.0 KOHM, 0201,1%	R9111		FB_4G_HYNIX
118S0013	1	RES, 10KOHM, 0201,1%	R9104		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201, 1%	R9115		GK107:GX
118S0315	1	RES, 34.8KOHM, 0201,1%	R9105		GK107:GT
118S0013	1	RES, 10KOHM, 0201,1%	R9114		GK107:GT

Die Rev	Strap
Hynix	0x4
ELPIDA	0x5
Hynix_29nm	0x1
ELPIDA_29nm	0x0







STRAP NOTES:
CURRENTLY STUFFED FOR GF108a/GK107-GTX
STUFF R9104 FOR THICK DIE
STUFF R9105 FOR THIN DIE

SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012
PAGE TITLE
KEPLER GPIOS,CLK & STRAPS
Apple Inc.
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SIZE D
REVISION 6.0.0
BRANCH dvt
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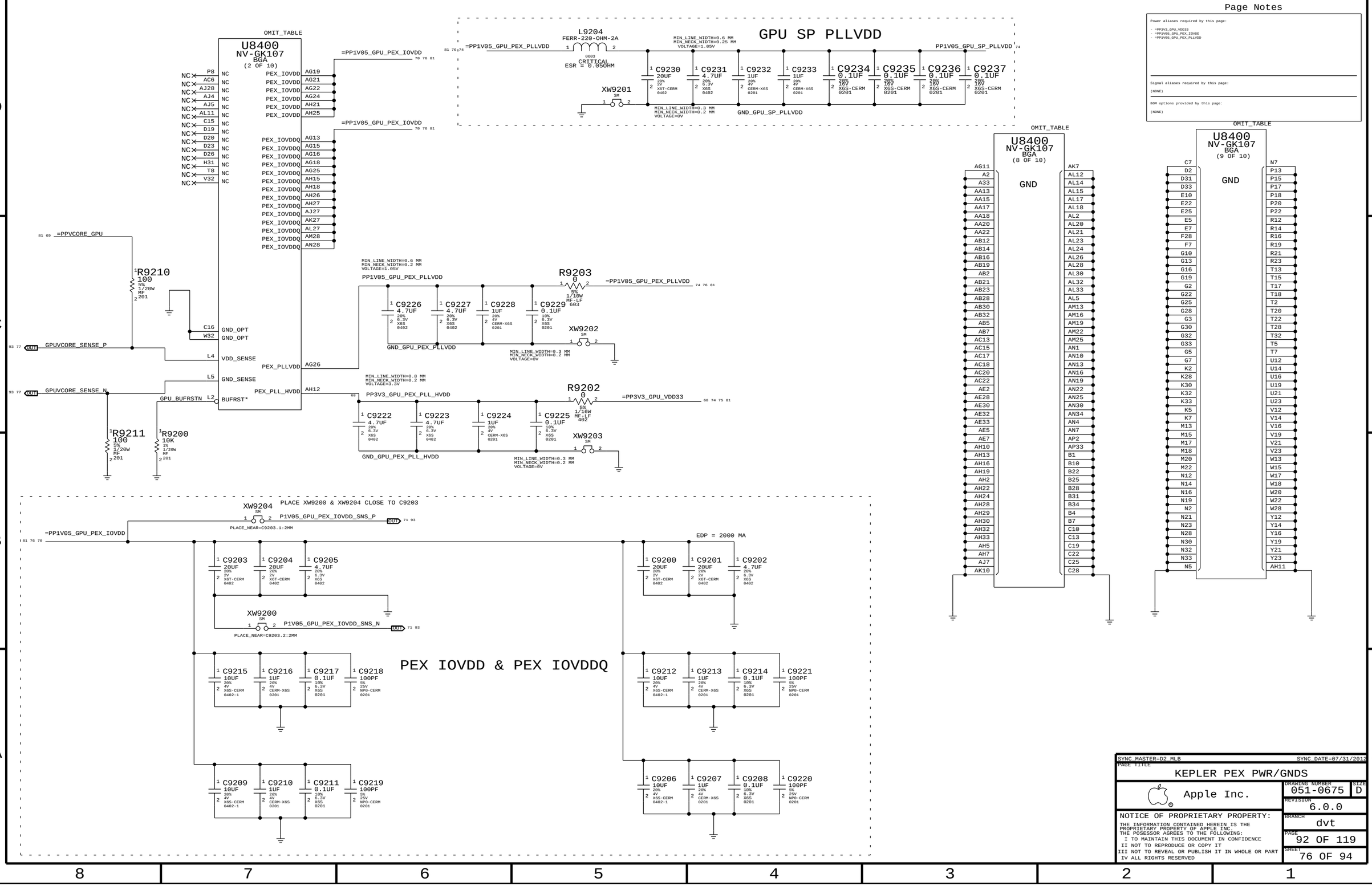

SYNC_MASTER=D2_MLB SYNC_DATE=07/31/2012

PAGE TITLE: KEPLER PEX PWR/GNDS

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

REVISION: 6.0.0

BRANCH: dvt

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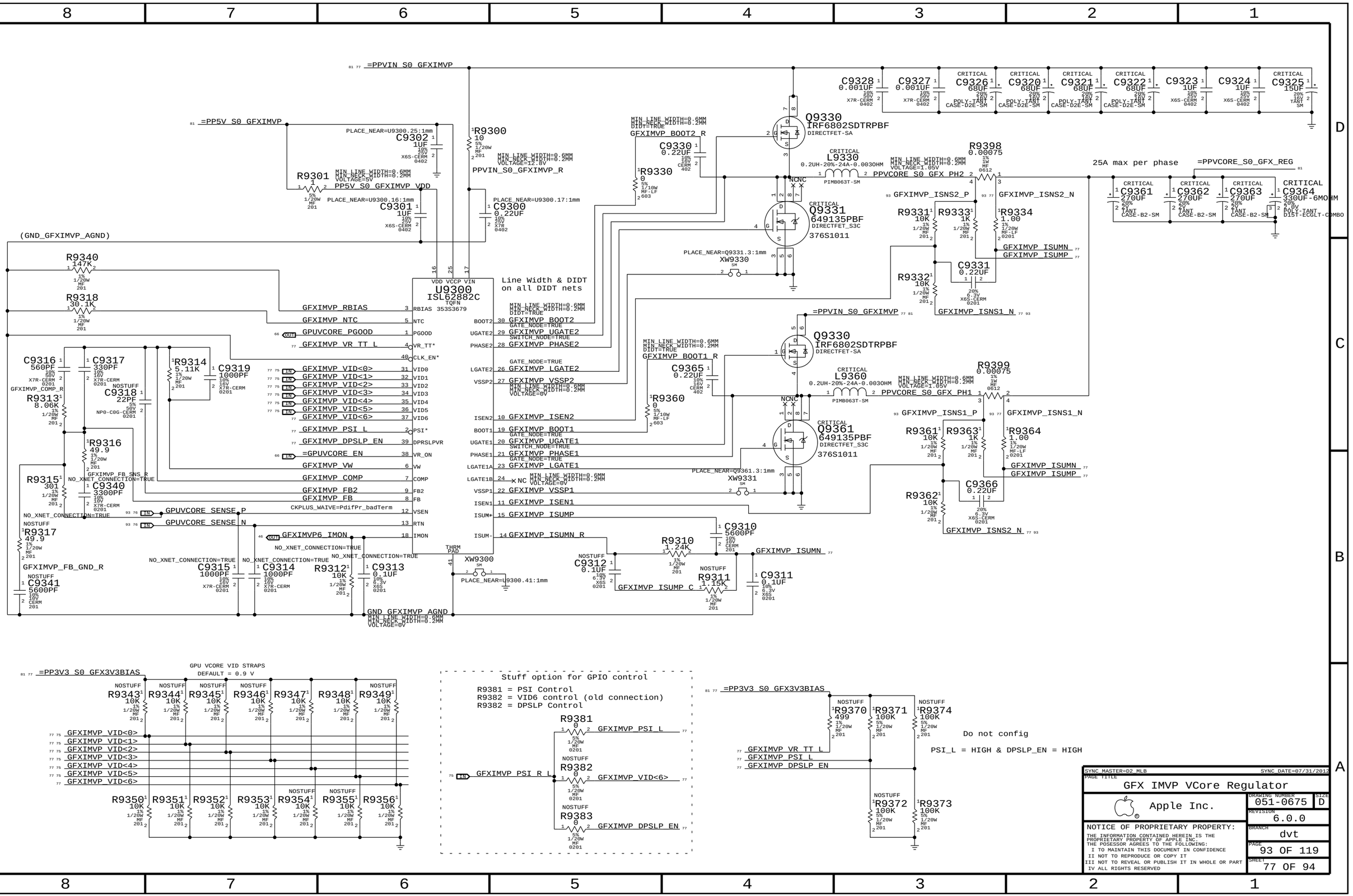
=PPVIN_S0_GFXIMVP
=PP5V_S0_GFXIMVP
PP5V_S0_GFXIMVP_VDD
PPVIN_S0_GFXIMVP_R
(GND_GFXIMVP_AGND)
U9300
ISL62882C
TQFN
Line Width & DIDT on all DIDT nets
GFXIMVP_RBIAS
GFXIMVP_NTC
GPUVCORE_PGOOD
GFXIMVP_VR_TT_L
CLK_EN*
GFXIMVP_VID<0>
GFXIMVP_VID<1>
GFXIMVP_VID<2>
GFXIMVP_VID<3>
GFXIMVP_VID<4>
GFXIMVP_VID<5>
GFXIMVP_VID<6>
GFXIMVP_PSI_L
GFXIMVP_DPSLP_EN
=GPUVCORE_EN
GFXIMVP_VW
GFXIMVP_COMP
GFXIMVP_FB2
GFXIMVP_FB
GPUVCORE_SENSE_P
GPUVCORE_SENSE_N
GFXIMVP6_IMON
GFXIMVP_BOOT2
GFXIMVP_UGATE2
GFXIMVP_PHASE2
GFXIMVP_LGATE2
GFXIMVP_VSSP2
GFXIMVP_ISEN2
GFXIMVP_BOOT1
GFXIMVP_UGATE1
GFXIMVP_PHASE1
GFXIMVP_LGATE1
GFXIMVP_VSSP1
GFXIMVP_ISEN1
GFXIMVP_ISUMP
GFXIMVP_ISUMN_R
GFXIMVP_ISUMN
GFXIMVP_ISUMP_C
GFXIMVP_FB_SNS_R
GFXIMVP_FB_GND_R
GND_GFXIMVP_AGND
Q9330
IRF6802SDTRPBF
DIRECTFET-SA
Q9331
649135PBF
DIRECTFET_S3C
376S1011
Q9361
XW9330
XW9331
XW9300
L9330
L9360
PIMB063T-SM
PPVCORE_S0_GFX_PH2
PPVCORE_S0_GFX_PH1
25A max per phase
=PPVCORE_S0_GFX_REG
GFXIMVP_ISNS2_P
GFXIMVP_ISNS2_N
GFXIMVP_ISNS1_P
GFXIMVP_ISNS1_N
GFXIMVP_ISNS2_N
GPU VCORE VID STRAPS
DEFAULT = 0.9 V
=PP3V3_S0_GFX3V3BIAS
Stuff option for GPIO control
R9381 = PSI Control
R9382 = VID6 control (old connection)
R9382 = DPSLP Control
GFXIMVP_PSI_R_L
Do not config
PSI_L = HIGH & DPSLP_EN = HIGH
GFX IMVP VCore Regulator
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SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012
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Wire-to-Board (Micro-coax) Connector

CRITICAL

J9500
20525-130E-01
F-RT-SM

NO_XNET_CONNECTION=TRUE
BP9501 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9502 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9505 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9506 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9503 SM
BEAD-PROBE TP 1

NO_XNET_CONNECTION=TRUE
BP9504 SM
BEAD-PROBE TP 1

87 13	IN	USB3_EXTB_R2D_C_P	C9501 0.1UF	GND_VOID=TRUE 10% 16V X5R-CERM 0201	
87 13	IN	USB3_EXTB_R2D_C_N	C9502 0.1UF	GND_VOID=TRUE 10% 16V X5R-CERM 0201	
87 83 13	OUT	USB3_EXTB_D2R_P			GND_VOID=TRUE
87 83 13	OUT	USB3_EXTB_D2R_N			GND_VOID=TRUE

87 83 13	BI	USB_EXTB_P	1
87 83 13	BI	USB_EXTB_N	2
			3
87 83		USB3_EXTB_R2D_P	4 GND_VOID=TRUE
87 83		USB3_EXTB_R2D_N	5 GND_VOID=TRUE
			6
			7 GND_VOID=TRUE
			8 GND_VOID=TRUE
			9
94 74	IN	HDMI_EG_DATA_C_P<0>	10 GND_VOID=TRUE
94 74	IN	HDMI_EG_DATA_C_N<0>	11 GND_VOID=TRUE
			12
94 74	IN	HDMI_EG_DATA_C_P<1>	13 GND_VOID=TRUE
94 74	IN	HDMI_EG_DATA_C_N<1>	14 GND_VOID=TRUE
			15
94 74	IN	HDMI_EG_DATA_C_P<2>	16 GND_VOID=TRUE
94 74	IN	HDMI_EG_DATA_C_N<2>	17 GND_VOID=TRUE
			18
94 74	IN	HDMI_EG_CLK_C_P	19
94 74	IN	HDMI_EG_CLK_C_N	20
			21
			22
			23
			24
88 83 20	OUT	USB3_SD_D2R_P	25 GND_VOID=TRUE
88 83 20	OUT	USB3_SD_D2R_N	26 GND_VOID=TRUE
			27
88 83 20	IN	USB3_SD_R2D_C_P	28 GND_VOID=TRUE
88 83 20	IN	USB3_SD_R2D_C_N	29 GND_VOID=TRUE
			30
			33
			34
			35
			36
			37
			38
			39
			40
			41

31 (shield) — 32 (shield) — 518S0829

Board-to-Board (Flex) Connector

CRITICAL

J9510
20590-032E-25
F-ST-SM

Note. Pin1 in symbol is different to 516S0853 in J15.

79 20	OUT	HDMI_HPD	3	PM_SLP_S3_BUF_L	IN 50 64 65 79 83
83 18	OUT	USB_EXTB_OC_L	5	PM_SLP_S4_L	IN 12 21 33 37 40 65 83
83 18 13	IN	SD_PWR_EN	7	HDMI_EG_DDC_CLK	IN 74
83 20	OUT	RIO_SDCONN_STATE_CHANGE_L	9	HDMI_EG_DDC_DATA	BI 74
81		=PP3V3_S3_RIO	15	PP1V5R1V35_S0_RIO	81
			17	=PP5V_S4_RIO	81
81		=PP3V3_S4_RIO			
43	IN	I2C_HDMIRDRV_SCL			
43	BI	I2C_HDMIRDRV_SDA			

GND: 2, 4, 11, 13, 21, 23, 31

C9510 0.1uF 20% 16V CERM 402 (1–2)
C9511 0.1uF 20% 16V CERM 402 (1–2)

34 — 33 — 35 — 36 — 516S1106

RIO_PWR:1V5
R9535 0 5% 1/16W MF-LF 402 (2–1)
MIN_LINE_WIDTH=0.5 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
=PP1V5_S0_RIO 81

RIO_PWR:1V35
R9534 0 5% 1/16W MF-LF 402 (2–1)
=PP1V35_S0_RIO 81

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
RIO Connectors

Apple Inc.

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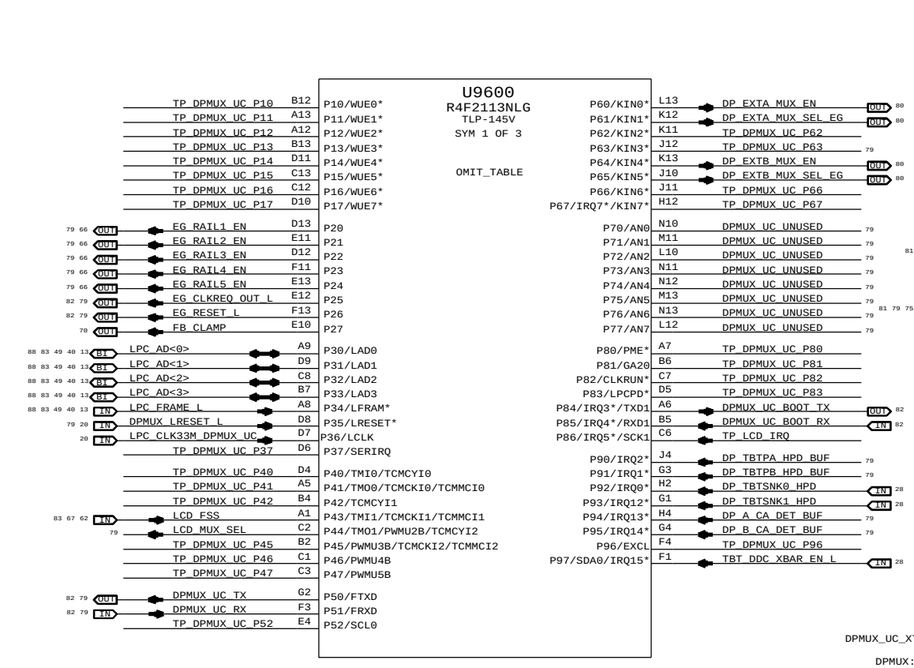
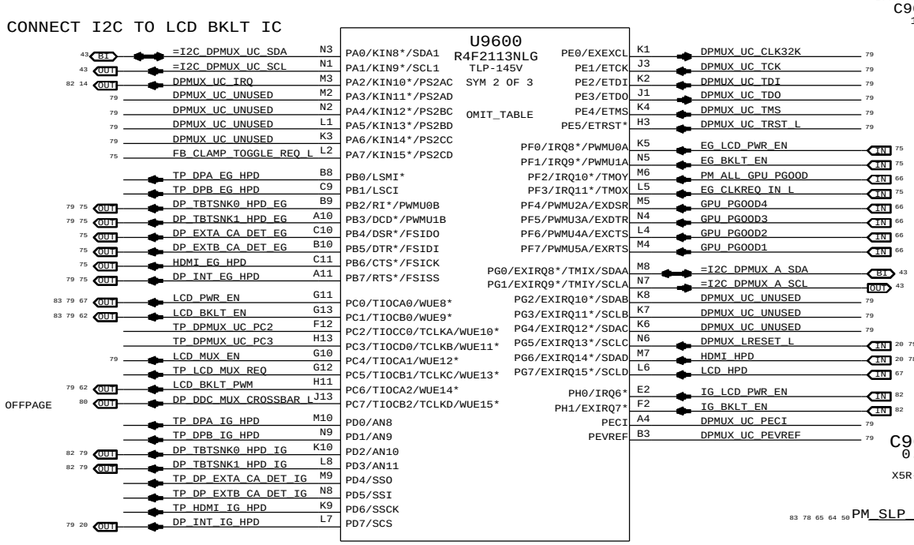
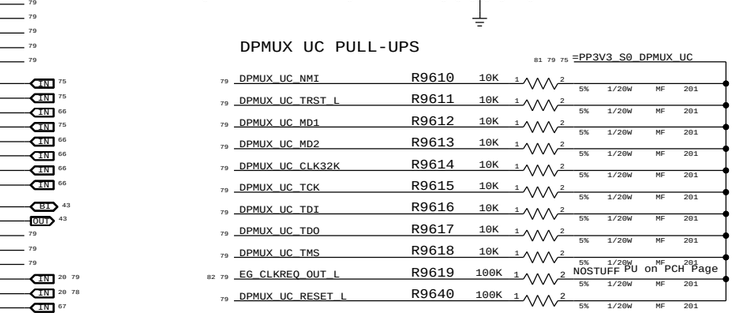


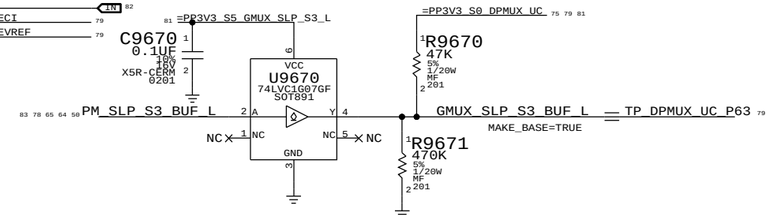


CONNECT I2C TO LCD BKLT IC

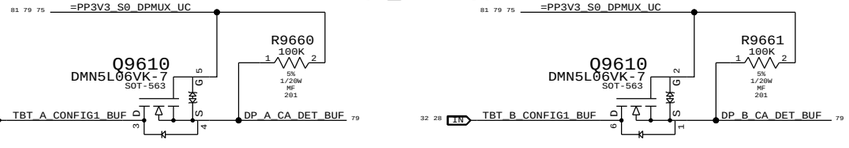
DPMUX UC DEBUG HEADER

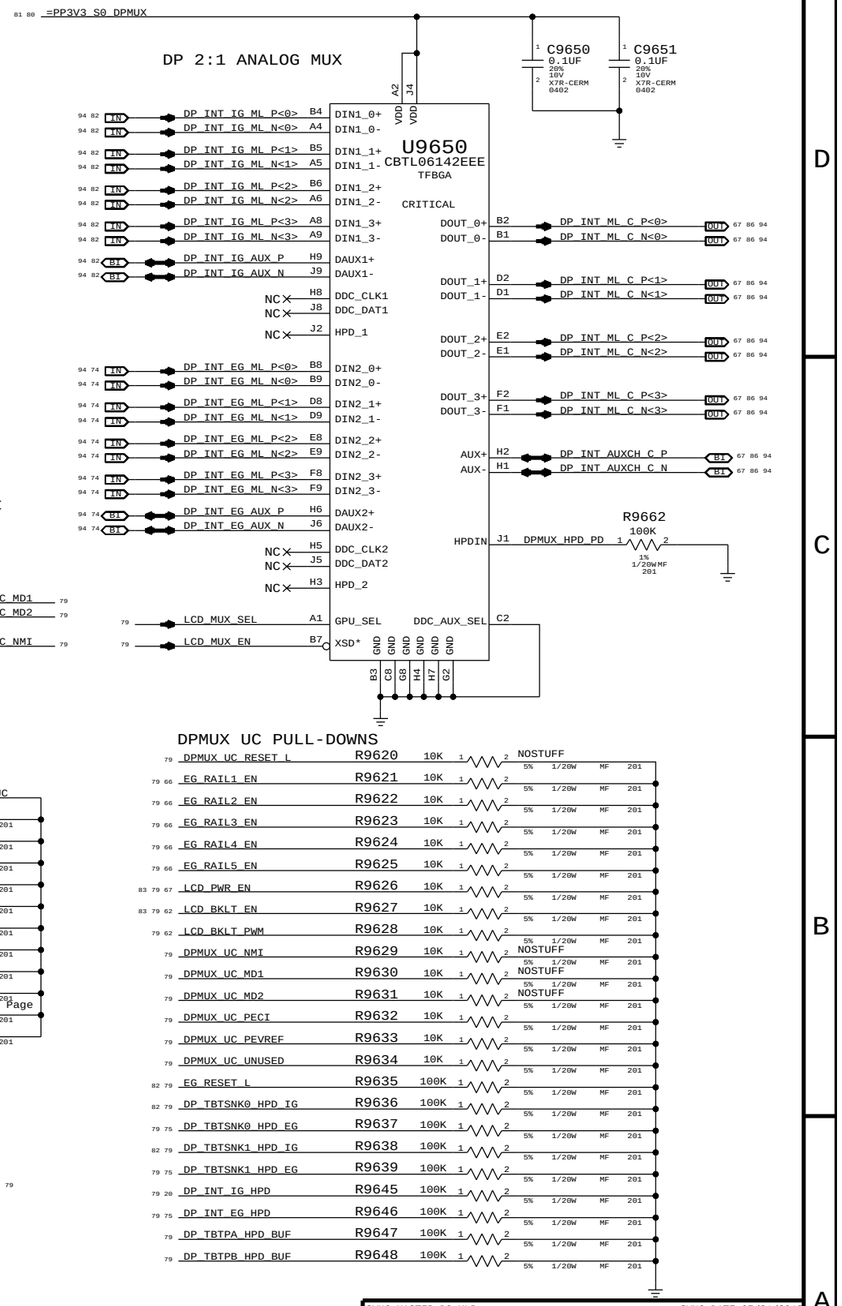


DPMUX UC PULL-UPS



CA_DET ISOLATION





DPMUX UC PULL-DOWNS

SYNC_MASTER=D2_MLB
SYNC_DATE=07/31/2012
PAGE TITLE
eDP Mux
Apple Inc.
DRAWING NUMBER 051-0675
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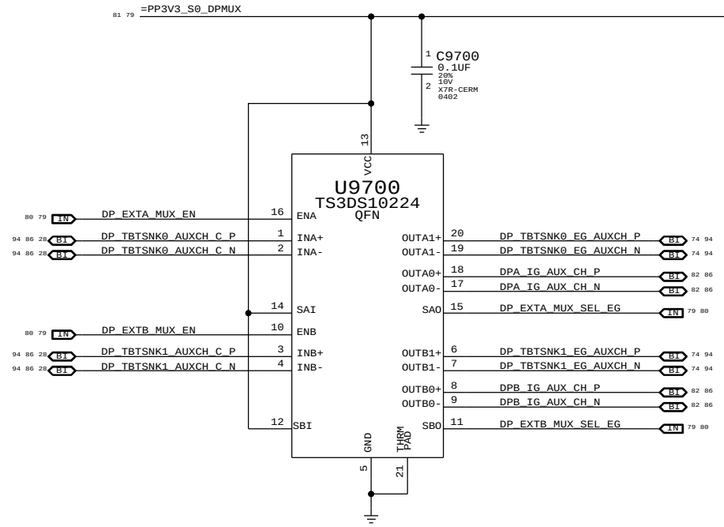
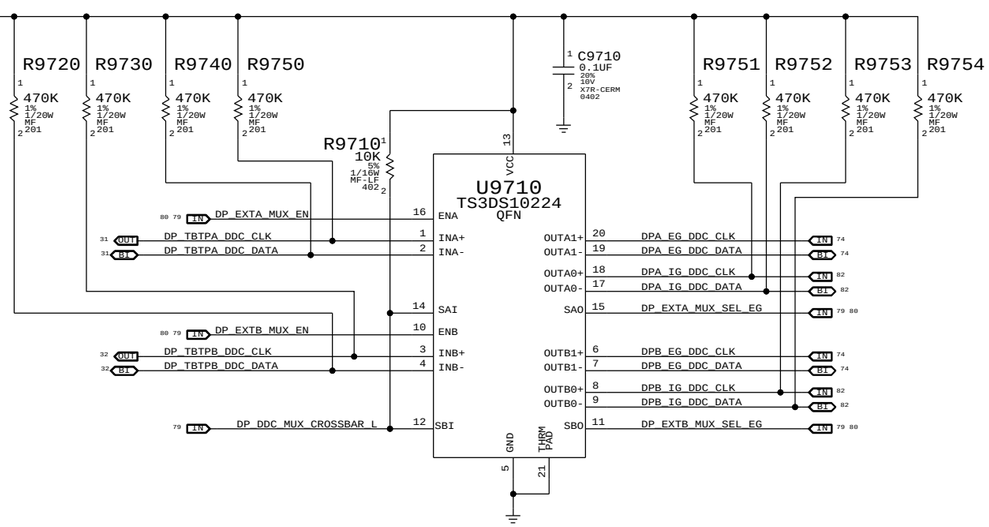
DP A & DP B AUX MUX



DP A & DP B DDC MUX



MUX TRUTH TABLE

SAI/SBI	SAO	SBO	INA	INB
0	0	0	OUTB0	OUTA0
0	0	1	OUTB1	OUTA0
0	1	0	OUTB0	OUTA1
0	1	1	OUTB1	OUTA1
1	0	0	OUTA0	OUTB0
1	0	1	OUTA0	OUTB1
1	1	0	OUTA1	OUTB0
1	1	1	OUTA1	OUTB1

SYNC_MASTER=CLEAN_D2 SYNC_DATE=08/14/2012

PAGE TITLE
eDP Muxed Graphics Support

Apple Inc.

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G3H/5V Rails

=PPBUS_G3H
PPBUS_G3H
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_HS_COMPUTING_ISNS_R
=PPVIN_S5_HS_GPU_ISNS_R
=PPVIN_S5_HS_OTHER3V3_ISNS_R
=PPVIN_S5_HS_OTHER5V_ISNS_R
=PPVIN_S0_LCDBKLT
=PPVIN_SW_TBTBST
=PPBUS_S0_VSENSE

=PPVIN_S5_HS_COMPUTING_ISNS
PPVIN_S5_HS_COMPUTING_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S0_CPUVR
=PPVIN_S3_DDRREG
=PPVIN_S0_P1V05S0

=PPVIN_S5_HS_GPU_ISNS
PPVIN_S5_HS_GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S0_GFXIMVP
=PPVIN_S0GPU_P1V5P1V0

=PPVIN_S5_HS_OTHER3V3_ISNS
PPVIN_S5_HS_OTHER3V3_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_P3V3

=PPVIN_S5_HS_OTHER5V_ISNS
PPVIN_S5_HS_OTHER5V_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S5_P5V

=PPVIN_T101_BOOSTRPBUS_ISNS
PPVIN_S4_TPAD
MIN_LINE_WIDTH=0.6 MM VOLTAGE=28V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVIN_S4_TPAD

=PP20V_DCIN_CONN
PPDCIN_G3H
MIN_LINE_WIDTH=0.6 MM VOLTAGE=20V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR

=PP20V_DCIN_ISOL
PPDCIN_G3H_ISOL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=20V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPDCIN_S5_CHGR_ISOL
=PPDCIN_S5_VSENSE

=PP3V42_G3H_REG
PP3V42_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V42_G3H_CHGR
=PP3V42_S3_HALL
=PP3V3_S5_LPCPLUS
=PP3V42_G3H_ONEWIREPROT
=PP3V42_G3H_PWRCTL
=PP3V42_G3H_SMBUS_SMC_5
=PP3V3_S5_SMC
=PP3V42_G3H_SMCUSBMUX
=PPVIN_S5_SMCVREF
=PPVBAT_G3_SYSCLK
=PP3V42_G3H_TPAD
=PP3V42_G3H_PCHPWRGD
=PP3V42_G3H_SSDSAK

=PPVRTC_G3_OUT
PPVRTC_G3H
MIN_LINE_WIDTH=0.3 MM VOLTAGE=3.42V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVRTC_G3_PCH

=PP5V_S5_LDO
PP5V_S5
MIN_LINE_WIDTH=0.6 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP5V_S5_P1V35S3RS0FET
=PP5V_S5_TPAD

=PP5V_S4_REG
PP5V_S4
MIN_LINE_WIDTH=0.3 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S4_AUDIO
=PP5V_S0_LCD
=PP5V_S3_LTUSB
=PP5V_S4_P5VS0FET
=PP5V_S4_P5VS3FET
=PP5V_S4_RIO

=PP5V_S3_FET
PP5V_S3
MIN_LINE_WIDTH=0.5 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S3_MEMRESET
=PP5V_S3_DDRREG
=PP5V_S3_ALSCAM

=PP5V_S0_FET
PP5V_S0
MIN_LINE_WIDTH=0.2 MM VOLTAGE=5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP5V_S0_AUDIO_XW
=PP5V_S0_CPUVR
=PP5V_S0_FAN_LT
=PP5V_S0_FAN_RT
=PP5V_S0_KBDLED
=PP5V_S0_LPCPLUS
=PP5V_S0_PCH
=PP5V_S0_P1V05S0
=PP5V_S0_VMON
=PP5V_S0_ALSCAM
=PP5V_S0_BKLTCTRL
=PP5V_S0_XDPJTAGISOL
=PP5V_S0_GFXIMVP
=PP5V_S0GPU_P1V0P1V35_GPU

3.3V Rails

=PP3V3_S5_REG
PP3V3_S5
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S4_SYSCLK
=PP3V3_S0_P3V3S0FET
=PP3V3_S3_P3V3S3FET
=PP3V3_S4_P3V3S4FET
=PP3V3_S4_TBTAPWRSW
=PP3V3_S4_TBTBPWRSW
=PP3V3_S5_1V5PGOOD
=PP3V3_S5_CPU_VCCDDR
=PP3V3_S5_DBGLED
=PP3V3_S5_P1V5S0
=PP3V3_S5_P3V3S0SW_SSD
=PP3V3_S5_P3V3SUSFET
=PP3V3_S5_PCH_GPIO
=PP3V3_S5_PCH_VCCDSW
=PP3V3_S5_PWRCTL
=PP3V3_S5_SYSCLK
=PP3V3_S5_VMON
=PP3V3_S5_WLAN
=PP3V3_S5_XDPJTAGISOL
=PP3V3_GPU_MISC_P3V3GPUMISCFET
=PP3V3_GPU_P3V3GPUFET
=PP3V3_S5_GMUX_SLP_S3_L
=PP3V3_S5_FAN_CTL

=PP3V3_S4_FET
PP3V3_S4
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP3V3_S4_BT
=PP3V3_S4_RIO
=PP3V3_S4_SMC
=PP3V3_S4_TBT_R
=PP3V3_S4_TPAD
=PP3V3_S4_ISNS
=PP3V3_S4_WLAN
=PP3V3_S4_FAN_CTL

=PP3V3_SUS_FET
PP3V3_SUS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_SUS_CNTRL
=PP3V3_SUS_P1V05SUSLDO
=PP3V3_SUS_PCH_GPIO
=PP3V3_SUS_PCH_VCCSUS_GPIO
=PP3V3_SUS_PCH_VCCSUS_RTC
=PP3V3_SUS_PCH_VCCSUS_USB
=PP3V3_SUS_PCH_VCCSUS_USB3
=PP3V3_SUS_PCH_VCC_SPI
=PP3V3_SUS_ROM

=PP3V3_S3_FET
PP3V3_S3
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S3RS4_PCH_GPIO
=PP3V3_S3_CAMERA_R
=PP3V3_S3_ISNS
=PP3V3_S3_MEMRESET
=PP3V3_S3_RIO
=PP3V3_S3_SDBUF
=PP3V3_S3_SMBUS_SMC_2_S3
=PP3V3_S3_VREFMRGN
=PP3V3_S3_DPMUX_UC

=PP3V3_S0_FET
PP3V3_S0
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.075 MM MAKE_BASE=TRUE
=PP3V3_S0_AUDIO
=PP3V3_S0_AUDIO_DIG
=PP3V3_S0_CAMERA_R
=PP3V3_S0_CPUTHMSNS
=PP3V3_S0_CPUVRISNS
=PP3V3_S0_FAN_LT
=PP3V3_S0_GPUTHMSNS
=PP3V3_S0_FAN_RT
=PP3V3_S0_HS_ISNS
=PP3V3_S0_ISNS
=PP3V3_S0_LCD
=PP3V3_S0_OOB1_PWRDN
=PP3V3_S0_PCH
=PP3V3_S0_PCH_GPIO
=PP3V3_S0_PCH_VCC3_3_GPIO
=PP3V3_S0_PCH_VCC3_3_HVCMOS
=PP3V3_S0_PCH_VCC3_3_THRM
=PP3V3_S0_PCH_VCC3_3_USB
=PP3V3_S0_PCH_VCCCLK3_3
=PP3V3_S0_PCH_VCC_FUSE
=PP3V3_S0_RSTBUF
=PP3V3_S0_SB_PM
=PP3V3_S0_SMBUS_PCH
=PP3V3_S0_SMBUS_SMC_0_S0
=PP3V3_S0_SMBUS_SMC_1_S0
=PP3V3_S0_SSD_AUX
=PP3V3_S0_VMON
=PP3V3_S0_X29THMSNS
=PP3V3_S0_DPMUX
=PP3V3_S0_DPMUXI2C
=PP3V3_S0_DPMUX_UC
=PP3V3_S0_PWRCTL

=PP3V3_S3RS0_CAMERA
PP3V3_S3RS0_CAMERA
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S3RS0_CAMPWREN

1.5V/1.35V/1.05V/VCORE/BKLT Rails

=PPDDR_S3_REG
PP1V35_S3
MIN_LINE_WIDTH=0.7 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.17 MM MAKE_BASE=TRUE
=PP1V5_S3_MEMRESET
=PPDDR_S3_MEMVREF
=PPVIN_S3_P1V35S3RS0_FET
=PPVIN_S0_DDRREG_LDO
=PPVIN_S3_MEM_ISNS_R

=PPVIN_S3_MEM_ISNS
PP1V35_S3_MEM
MIN_LINE_WIDTH=0.2 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.17 MM MAKE_BASE=TRUE
=PP1V5R1V35_S3_MEM_A
=PP1V5R1V35_S3_MEM_B

=PP1V35_S3RS0_FET_ISNS
PP1V35_S3RS0_CPUDDR
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V35_S3RS0_VMON
=PP1V5R1V35_S0_CPU

=PP1V35_S3RS0_FET
PP1V35_S3RS0_FET
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.35V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V35_S0_RIO

=PP1V5_S0_REG
PP1V5_S0
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.5V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V5_S0_AUDIO
=PP1V5_S0_PCH_CLK
=PP1V5_S0_PCH_SATA
=PP1V5_S0_PCH_RCOMP
=PP1V5_S0_PCH_VCCVRM
=PP3V3R1V5_S0_PCH_VCCSUSHDA
=PPVDDIO_S0_SBCLK
=PP1V5_S0_RIO
=PP1V5_S0_DIV

=PPVTT_S3_DDR_BUF
PPVTTDDR_S3
MIN_LINE_WIDTH=0.3 MM VOLTAGE=0.675V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

=PPVTT_S0_DDR_LDO
PPVTT_S0_DDR
MIN_LINE_WIDTH=0.4 MM VOLTAGE=0.675V
MIN_NECK_WIDTH=0.17 mm MAKE_BASE=TRUE
=PPVTT_S0_MEM_A
=PPVTT_S0_MEM_B
=PPVTT_S0_VTTCLAMP

=PP1V05_SUS_LDO
PP1V05_SUS
MIN_LINE_WIDTH=0.4 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_SUS_PCH_JTAG

=PP1V05_S0_REG
PP1V05_S0
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_S0_PCH_VCC
=PP1V05_S0_PCH_VCCCLK_CLK100
=PP1V05_S0_PCH_VCCCLK_CLK135
=PP1V05_S0_PCH_VCCCLK_SSC
=PP1V05_S0_PCH_VCCCLK_SSC100
=PP1V05_S0_PCH_VCCIO
=PP1V05_S0_PCH_VCCIO_FDI
=PP1V05_S0_PCH_VCCIO_GPIO
=PP1V05_S0_PCH_VCCIO_USB2
=PP1V05_S0_PCH_VCCUSBPLL
=PP1V05_S0_PCH_VCC_CLK
=PP1V05_S0_PCH_V_PROC_IO
=PP1V05_S0M_PCH_VCCASW
=PP1V05_S0_CPU_JTAG
=PPVCCIO_S0_SMC
=PP1V05_S0_VMON

=PPVCC_S0_CPU_REG
PPVCC_S0_CPU
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.8V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE
=PPVCORE_S0_CPU
=PPVCC_S0_CPU

=PPBUS_SW_BKL
PPBUS_SW_BKL
MIN_LINE_WIDTH=0.6 MM VOLTAGE=12.6V
MIN_NECK_WIDTH=0.25 MM MAKE_BASE=TRUE

=PP3V3_S4_TBT
PP3V3_S4_TBT
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.1 MM MAKE_BASE=TRUE
=PP3V3_S0SW_SSD_R
PP3V3_S0SW_SSD_R
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP3V3_S0SW_SSD
PP3V3_S0SW_SSD
MIN_LINE_WIDTH=0.5 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE

TBT RAILS

=PP3V3_TBTLC_FET
PP3V3_TBTLC
MIN_LINE_WIDTH=0.4 MM VOLTAGE=3.3V
MIN_NECK_WIDTH=0.15 MM MAKE_BASE=TRUE
=PPVDDIO_TBTLC_CLK

=PP15V_TBT_REG
PP15V_TBT
MIN_LINE_WIDTH=0.4 MM VOLTAGE=15V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPHV_S4SW_TBTAPWRSW
=PPHV_S4SW_TBTBPWRSW

PPVIN_SW_TBTBST
VOLTAGE=12.6V

"GPU" Rails

=PP3V3_S0GPU_FET
PP3V3_S0GPU
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_IFPX_PLLVDD
=PP3V3_S0_GFX3V3BIAS
=PP3V3_GPU_VDD33

=PP3V3_S0GPU_MISC_FET
PP3V3_S0GPU_MISC
MIN_LINE_WIDTH=0.3 MM
MIN_NECK_WIDTH=0.10MM
VOLTAGE=3.3V
MAKE_BASE=TRUE
=PP3V3_GPU_MISC

=PP1V5R1V35_GPU_REG
PP1V5R1V35_S0GPU
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.2 MM
VOLTAGE=1.5V
MAKE_BASE=TRUE
=PP1V35_GPU_FBVDDQ
=PP1V35_GPU_S0_FB
=PP1V35_GPU_FB

=PP1V05_S0GPU_REG
PP1V0_S0GPU_ISNS
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.05V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PP1V05_GPU_IFPCD_IOVDD
=PP1V05_GPU_IFPEF_IOVDD
=PP1V05_GPU_PEX_IOVDD
=PP1V05_GPU_PEX_PLLVDD

=PPVCORE_GPU_REG
PPVCORE_GPU
MIN_LINE_WIDTH=0.6 MM VOLTAGE=1.0V
MIN_NECK_WIDTH=0.2 MM MAKE_BASE=TRUE
=PPVCORE_GPU
=PPVCORE_S0_GFX_REG

GND
MIN_LINE_WIDTH=0.6 MM
MIN_NECK_WIDTH=0.085 MM
VOLTAGE=0V
MAKE_BASE=TRUE

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE
Power Aliases

Apple Inc.

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Display Aliases

12	EDP_IG_PANEL_PWR	IG_LCD_PWR_EN	79
12	EDP_IG_BKL_ON	IG_BKLT_EN	79
94 79	DP_INT_IG_ML_P<3..0>	TP_DP_IG_A_MLP<3..0>	5
94 79	DP_INT_IG_ML_N<3..0>	TP_DP_IG_A_MLN<3..0>	5
94 79	DP_INT_IG_AUX_P	TP_DP_IG_A_AUXCHP	5
94 79	DP_INT_IG_AUX_N	TP_DP_IG_A_AUXCHN	5
86 80	DPA_IG_AUX_CH_P	TP_DP_IG_B_AUXCHP	12
86 80	DPA_IG_AUX_CH_N	TP_DP_IG_B_AUXCHN	12
86 80	DPB_IG_AUX_CH_P	TP_DP_IG_C_AUXCHP	12
86 80	DPB_IG_AUX_CH_N	TP_DP_IG_C_AUXCHN	12
80	DPA_IG_DDC_CLK	TP_DP_IG_B_DDC_CLK	12
80	DPA_IG_DDC_DATA	TP_DP_IG_B_DDC_DATA	12
80	DPB_IG_DDC_CLK	TP_DP_IG_C_DDC_CLK	12
80	DPB_IG_DDC_DATA	TP_DP_IG_C_DDC_DATA	12
79	DP_TBTSNK0_HPD_IG	TP_DP_IG_B_HPD	12
79	DP_TBTSNK1_HPD_IG	TP_DP_IG_C_HPD	12
79	DPMUX_UC_RX	DPMUX_UC_BOOT_RX	79
79	DPMUX_UC_TX	DPMUX_UC_BOOT_TX	79
79	EG_RESET_L	GPU_RESET_L	68 75
82 11	PEG_CLKREQ_L	EG_CLKREQ_OUT_L	79
18 11	DP_AUXCH_ISOL_L	DP_AUXIO_EN	

MAKE_BASE=TRUE

CPU signals

21	MEMVTT_EN	=DDRVTT_EN	21 59

MAKE_BASE=TRUE

86 68 66	PEG_D2R_P<7..0>	=PEG_D2R_P<7..0>	5
86 68 66	PEG_D2R_N<7..0>	=PEG_D2R_N<7..0>	5
86 68	PEG_R2D_C_P<7..0>	=PEG_R2D_C_P<7..0>	5
86 68	PEG_R2D_C_N<7..0>	=PEG_R2D_C_N<7..0>	5

MAKE_BASE=TRUE

	NC_PCIE_PEG_D2RP<15..12>	=PEG_D2R_P<15..12>	5
	NC_PCIE_PEG_D2RN<15..12>	=PEG_D2R_N<15..12>	5
	NC_PCIE_PEG_R2D_CP<15..12>	=PEG_R2D_C_P<15..12>	5
	NC_PCIE_PEG_R2D_CN<15..12>	=PEG_R2D_C_N<15..12>	5

MAKE_BASE=TRUE; NO_TEST=TRUE

Thunderbolt Signals Through PEG

86 28	PCIE_TBT_D2R_P<3..0>	=PEG_D2R_P<11..8>	5
86 28	PCIE_TBT_D2R_N<3..0>	=PEG_D2R_N<11..8>	5
86 28	PCIE_TBT_R2D_C_P<3..0>	=PEG_R2D_C_P<11..8>	5
86 28	PCIE_TBT_R2D_C_N<3..0>	=PEG_R2D_C_N<11..8>	5

MAKE_BASE=TRUE

88 83 68	PEG_CLK100M_N	TP_PCIE_CLK100M_GPUN	11
88 83 68	PEG_CLK100M_P	TP_PCIE_CLK100M_GPUP	11

MAKE_BASE=TRUE

48 =PP3V3_S3_FAN_CTL

PP3V3_S3_FAN_CTL
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=3.3V
MAKE_BASE=TRUE

RA201
0
1 2
5%
1/20W
MF
0201
0
1 2
5%
1/20W
MF
0201

=PP3V3_S5_FAN_CTL 81

=PP3V3_S4_FAN_CTL 81

RA202
NOSTUFF

TP_P1V8GPU_EN =P1V8GPU_EN 66

Unused signals

12	BT_PWRRST_L
14	MEM_VDD_SEL_1V5_L
14	FW_PWR_EN_PCH
14	WOL_EN
14	FW_PME_L
11	DP_TBT_SEL
11	ENET_MEDIA_SENSE_RDIV
12	AUD_IPHS_SWITCH_EN_PCH
12	AUD_IP_PERIPHERAL_DET
12	AUD_I2C_INT_L
14	TBT_GO2SX_BIDIR
79 14	DPMUX_UC_IRQ
82 11	PEG_CLKREQ_L
11	ENET_CLKREQ_L
12	ENET_LOW_PWR_PCH
28	HDMITBTMUX_SEL_TBT
12	SDCONN_OC_L

		VOLTAGE	MAKE_BASE	
89 86 24 23 22	PPVREF_S3_MEM_VREFDQ_A	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_A
86 26 25 22	PPVREF_S3_MEM_VREFDQ_B	0.675V	TRUE	PP0V75_S3_MEM_VREFDQ_B
89 86 24 23 22	PPVREF_S3_MEM_VREFCA_A	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_A
86 26 25 22	PPVREF_S3_MEM_VREFCA_B	0.675V	TRUE	PP0V75_S3_MEM_VREFCA_B

81 =PP5V_S0_AUDIO_XW

XWA202
SM
1 2
PP5V_S0_AUDIO_AMP_L 52
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

XWA203
SM
1 2
PP5V_S0_AUDIO_AMP_R 52
MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.2MM
VOLTAGE=5V

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Signal Aliases

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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Functional Test Points

J3501 - airport

FUNC_TEST		
TRUE	AP_CLKREQ_Q_L	33
TRUE	AP_RESET_CONN_L	33
TRUE	PCIE_AP_D2R_PI_N	33 88
TRUE	PCIE_AP_D2R_PI_P	33 88
TRUE	PCIE_AP_R2D_N	33 88
TRUE	PCIE_AP_R2D_P	33 88
TRUE	PCIE_CLK100M_AP_CONN_N	33 88
TRUE	PCIE_CLK100M_AP_CONN_P	33 88
TRUE	PCIE_WAKE_L	12 33 35 88
TRUE	PP3V3_S3RS4_BT_F	33
TRUE	PP3V3_WLAN	33 41
TRUE	USB_BT_CONN_N	33 87
TRUE	USB_BT_CONN_P	33 87
TRUE	WIFI_EVENT_L	33 40 41
TRUE	GND	4X

J4002 - Camera

TRUE	MIPI_CLK_CONN_N	36 91
TRUE	MIPI_CLK_CONN_P	36 91
TRUE	CAM_SENSOR_WAKE_L_CONN	36
TRUE	MIPI_DATA_CONN_N	36 91
TRUE	MIPI_DATA_CONN_P	36 91
TRUE	=I2C_ALS_SDA	36 43
TRUE	=I2C_ALS_SCL	36 43
TRUE	I2C_CAM_SCK	35 36
TRUE	I2C_CAM_SDA	35 36
TRUE	PP5V_S3RS0_ALSCAM_F	36
TRUE	GND	

J9500 - rio coax

TRUE	HDMI_CLK_N	86
TRUE	HDMI_CLK_P	86
TRUE	HDMI_DATA_N<0>	86
TRUE	HDMI_DATA_N<1>	86
TRUE	HDMI_DATA_N<2>	86
TRUE	HDMI_DATA_P<0>	86
TRUE	HDMI_DATA_P<1>	86
TRUE	HDMI_DATA_P<2>	86

TRUE	USB3_SD_D2R_N	20 78 88
TRUE	USB3_SD_D2R_P	20 78 88
TRUE	USB3_SD_R2D_C_N	20 78 88
TRUE	USB3_SD_R2D_C_P	20 78 88
TRUE	USB3_EXTB_D2R_N	13 78 87
TRUE	USB3_EXTB_D2R_P	13 78 87
TRUE	USB3_EXTB_R2D_N	78 87
TRUE	USB3_EXTB_R2D_P	78 87
TRUE	USB_EXTB_N	13 78 87
TRUE	USB_EXTB_P	13 78 87
TRUE	GND	19X

J9510 - rio flex

TRUE	SD_PWR_EN	13 18 78
TRUE	PP1V5R1V35_S0_RIO	78
TRUE	HDMI_DDC_CLK	
TRUE	HDMI_DDC_DATA	
TRUE	HDMI_HPD_L	
TRUE	SMBUS_PCH_CLK	13 43 88
TRUE	SMBUS_PCH_DATA	13 43 88
TRUE	PM_SLP_S3_BUF_L	50 64 65 78 79
TRUE	PM_SLP_S4_L	12 21 33 37 40 65 78
TRUE	PP3V3_S3	3X 81 83
TRUE	PP3V3_S4	81 83
TRUE	PP5V_S4	5X 81
TRUE	RIO_SDCONN_STATE_CHANGE_L	20 78
TRUE	USB_EXTB_OC_L	18 78
TRUE	GND	10X

J5150 - hall effect

TRUE	PP3V42_G3H	81 83
TRUE	SMC_LID_R	42
TRUE	GND	

J6050 - left fan

TRUE	FAN_LT_PWM	48
TRUE	FAN_LT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6060 - right fan

TRUE	FAN_RT_PWM	48
TRUE	FAN_RT_TACH	48
TRUE	PP5V_S0	3X 81 83
TRUE	GND	5X

J6100 - lpc + spi

FUNC_TEST		
TRUE	LPCPLUS_GPIO	14 49
TRUE	LPCPLUS_RESET_L	20 49
TRUE	LPC_AD<0>	13 40 49 79 88
TRUE	LPC_AD<1>	13 40 49 79 88
TRUE	LPC_AD<2>	13 40 49 79 88
TRUE	LPC_AD<3>	13 40 49 79 88
TRUE	LPC_CLK33M_LPCPLUS	19 49 88
TRUE	LPC_FRAME_L	13 40 49 79 88
TRUE	LPC_PWRDWN_L	12 20 40 49
TRUE	LPC_SERIRQ	13 40 49
TRUE	PM_CLKRUN_L	12 40 49
TRUE	PP5V_S0	81 83
TRUE	SMC_RESET_L	40 41 49 56
TRUE	SMC_ROMBOOT	41 49
TRUE	SMC_RX_L	40 41 49
TRUE	SMC_TCK	40 41 49
TRUE	SMC_TDI	40 41 49
TRUE	SMC_TDO	40 41 49
TRUE	SMC_TMS	40 41 49
TRUE	SMC_TX_L	40 41 49
TRUE	SPIROM_USE_MLB	14 49
TRUE	SPI_ALT_CLK	49
TRUE	SPI_ALT_CS_L	49
TRUE	SPI_ALT_MISO	49
TRUE	SPI_ALT_MOSI	49
TRUE	TP_SMC_MD1	49
TRUE	TP_SMC_TRST_L	49
TRUE	GND	2X

J4800 - ipd flex

TRUE	Z2_CS_L	38
TRUE	Z2_MOSI	38
TRUE	Z2_MISO	38
TRUE	Z2_SCLK	38
TRUE	Z2_HOST_INTN	38
TRUE	Z2_CLKIN	38
TRUE	Z2_KEY_ACT_L	38
TRUE	PSOC_F_CS_L	38
TRUE	PICKB_L	38
TRUE	PSOC_MOSI	38
TRUE	PSOC_MISO	38
TRUE	PSOC_SCLK	38
TRUE	=I2C_TPAD_SCL	38 43
TRUE	=I2C_TPAD_SDA	38 43
TRUE	SMC_LID	38 40 41 42
TRUE	SMC_T101_COM_1	
TRUE	=PP3V3_S4_TPAD	38 81
TRUE	=PP5V_S5_TPAD	38 81
TRUE	GND	2X

J4813 - keyboard

TRUE	PP3V3_S4	81 83
TRUE	PP3V42_G3H	81 83
TRUE	WS_CONTROL_KBD	38
TRUE	WS_KBD1	38
TRUE	WS_KBD10	38
TRUE	WS_KBD11	38
TRUE	WS_KBD12	38
TRUE	WS_KBD13	38
TRUE	WS_KBD14	38
TRUE	WS_KBD15_CAP	38
TRUE	WS_KBD16_NUM	38
TRUE	WS_KBD17	38
TRUE	WS_KBD18	38
TRUE	WS_KBD19	38
TRUE	WS_KBD2	38
TRUE	WS_KBD20	38
TRUE	WS_KBD21	38
TRUE	WS_KBD22	38
TRUE	WS_KBD23	38
TRUE	WS_KBD3	38
TRUE	WS_KBD4	38
TRUE	WS_KBD5	38
TRUE	WS_KBD6	38
TRUE	WS_KBD7	38
TRUE	WS_KBD8	38
TRUE	WS_KBD9	38
TRUE	WS_KBD_ONOFF_L	38
TRUE	WS_LEFT_OPTION_KBD	38
TRUE	WS_LEFT_SHIFT_KBD	38
TRUE	GND	2X

J4915 - kbd bklt

TRUE	KBDBKLT_RETURN1	2X 39 62
TRUE	KBDBKLT_RETURN2	2X 39 62
TRUE	PPVOUT_S0_KBDBKLT	39 62
TRUE	GND	4X

J6701 - audio flex

FUNC_TEST		
TRUE	AUD_HP_PORT_L	50 54
TRUE	AUD_HP_PORT_R	50 54
TRUE	AUD_SPDIF_OUT_JACK	
TRUE	AUD_TIPDET_INV	
TRUE	AUD_TYPEDET	50 54
TRUE	AUD_CONN_MIC_XW	4X
TRUE	CH_HS_MIC	
TRUE	PP3V3_S0	81 83 93
TRUE	AUD_CONN_SLEEVE_XW	4X 53 54
TRUE	US_HS_MIC	
TRUE	GND	2X GND

J6601 - mic

TRUE	DMIC_CLK3	51 54
TRUE	PP3V3_S0	81 83 93
TRUE	DMIC_SDA2	54
TRUE	DMIC_SDA3	51 54
TRUE	GND	

J6602 - L speaker

TRUE	SPKRCONN_L_ID	51 54
TRUE	SPKRCONN_L_OUT_N	52 54 93
TRUE	SPKRCONN_L_OUT_P	52 54 93
TRUE	SPKRCONN_SL_OUT_N	52 54 93
TRUE	SPKRCONN_SL_OUT_P	52 54 93
TRUE	GND	

J6603 - R speaker

TRUE	SPKRCONN_R_ID	51 54
TRUE	SPKRCONN_R_OUT_N	52 54 93
TRUE	SPKRCONN_R_OUT_P	52 54 93
TRUE	SPKRCONN_SR_OUT_N	52 54 93
TRUE	SPKRCONN_SR_OUT_P	52 54 93
TRUE	GND	

J7000 - DC PWR

TRUE	ADAPTER_SENSE	55
TRUE	PP20V_DCIN_FUSE	2X 55
TRUE	GND	2X

J7050 - battery

TRUE	PPVBAT_G3H_CONN	8X 55 56
TRUE	SMBUS_SMC_5_G3_SCL	40 43 92
TRUE	SMBUS_SMC_5_G3_SDA	40 43 92
TRUE	SYS_DETECT_L	55
TRUE	GND	8X

J8300 - eDP

TRUE	DP_INT_AUX_N	67 86 94
TRUE	DP_INT_AUX_P	67 86 94
TRUE	DP_INT_ML_N<0>	67 86 94
TRUE	DP_INT_ML_N<1>	67 86 94
TRUE	DP_INT_ML_N<2>	67 86 94
TRUE	DP_INT_ML_N<3>	67 86 94
TRUE	DP_INT_ML_P<0>	67 86 94
TRUE	DP_INT_ML_P<1>	67 86 94
TRUE	DP_INT_ML_P<2>	67 86 94
TRUE	DP_INT_ML_P<3>	67 86 94
TRUE	LCD_FSS	62 67 79
TRUE	LCD_HPD_CONN	67
TRUE	LED_RETURN_1	62 67
TRUE	LED_RETURN_2	62 67
TRUE	LED_RETURN_3	62 67
TRUE	LED_RETURN_4	62 67
TRUE	LED_RETURN_5	62 67
TRUE	LED_RETURN_6	62 67
TRUE	PP5VR3V3_SW_LCD	3X 67
TRUE	PPVOUT_S0_LCDBKLT	62 67
TRUE	GND	16X

Power Rails

TRUE	PM_SLP_S3_L	12 21 40 65
TRUE	PPVTT_S0_DDR	81
TRUE	PP3V3_S0	81 83 93
TRUE	PP3V3_S3	81 83
TRUE	PP3V3_S5	81 93
TRUE	PP3V3_S5_AVREF_SMC	40 41
TRUE	PP3V42_G3H	81 83
TRUE	PP5V_S0	81 83
TRUE	PP5V_S3	81
TRUE	PP5V_S5	81
TRUE	PPBUS_G3H	81
TRUE	PPDCIN_G3H	81
TRUE	PPVCC_S0_CPU	81
TRUE	PPVTTDDR_S3	81
TRUE	PP3V3_S0SW_SSD	81
TRUE	PP1V5_S0	81
TRUE	PP1V35_S3	81

XDP

FUNC_TEST		
TRUE	XDP_CPU_TCK	6 18 86
TRUE	XDP_PCH_TCK	11 18
TRUE	XDP_CPU_TDI	6 18 86
TRUE	XDP_CPU_TDO	6 18 86
TRUE	XDP_CPU_TRST_L	6 18 86
TRUE	XDP_CPU_TMS	6 18 86
TRUE	XDP_PCH_TMS	11 18
TRUE	XDP_PCH_TDI	11 18
TRUE	XDP_PCH_TDO	11 18
TRUE	XDP_CPU_PREQ_L	6 18 86
TRUE	XDP_CPU_PRDY_L	6 18 86
TRUE	PM_RSMRST_L	12 65 88
TRUE	PM_PCH_PWROK	12 19 88
TRUE	PM_SYSRST_L	12 19 40 88
TRUE	CPU_CFG<3>	6 18 86
TRUE	PP1V05_S0	81
TRUE	GND	2X GND

Power Sequence

FUNC_TEST		
TRUE	SMC_ONOFF_L	38 40 41
TRUE	PM_DSW_PWRGD	12 40 88
TRUE	ALL_SYS_PWRGD	18 19 40 65
TRUE	PM_PCH_SYS_PWROK	12 18 19 40 88
TRUE	PLT_RESET_L	12 18 20 21
TRUE	LCD_PWR_EN	67 79
TRUE	LCD_BKLT_EN	62 79

TPA401 (A) TP-P6 — TPA402 (A) TP-P6

	PEG_CLK100M_P	68 82 88
	PEG_CLK100M_N	68 82 88

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NC NO_TESTs

PCH

		NO_TEST	MAKE_BASE	
13	TP_USB3_SPARE_D2RN	TRUE	TRUE	NC_USB3_SPARE_D2RN
13	TP_USB3_SPARE_D2RP	TRUE	TRUE	NC_USB3_SPARE_D2RP
13	TP_USB3_SPARE_R2D_CN	TRUE	TRUE	NC_USB3_SPARE_R2D_CN
13	TP_USB3_SPARE_R2D_CP	TRUE	TRUE	NC_USB3_SPARE_R2D_CP
13	USB3_EXTC_D2R_N	TRUE	TRUE	NC_USB3_EXTC_D2RN 87
13	USB3_EXTC_D2R_P	TRUE	TRUE	NC_USB3_EXTC_D2RP 87
13	USB3_EXTC_R2D_C_N	TRUE	TRUE	NC_USB3_EXTC_R2D_CN 87
13	USB3_EXTC_R2D_C_P	TRUE	TRUE	NC_USB3_EXTC_R2D_CP 87
13	USB3_EXTD_D2R_N	TRUE	TRUE	NC_USB3_EXTD_D2RN 87
13	USB3_EXTD_D2R_P	TRUE	TRUE	NC_USB3_EXTD_D2RP 87
13	USB3_EXTD_R2D_C_N	TRUE	TRUE	NC_USB3_EXTD_R2D_CN 87
13	USB3_EXTD_R2D_C_P	TRUE	TRUE	NC_USB3_EXTD_R2D_CP 87
	PCIE_ENET_D2RN	TRUE	TRUE	NC_PCIE_ENET_D2RN
	PCIE_ENET_D2RP	TRUE	TRUE	NC_PCIE_ENET_D2RP
	PCIE_ENET_R2D_CN	TRUE	TRUE	NC_PCIE_ENET_R2D_CN
	PCIE_ENET_R2D_CP	TRUE	TRUE	NC_PCIE_ENET_R2D_CP
11	SATA_A_D2R_N	TRUE	TRUE	NC_SATA_A_D2RN 87
11	SATA_A_D2R_P	TRUE	TRUE	NC_SATA_A_D2RP 87
11	SATA_A_R2D_C_N	TRUE	TRUE	NC_SATA_A_R2D_CN 87
11	SATA_A_R2D_C_P	TRUE	TRUE	NC_SATA_A_R2D_CP 87
11	SATA_B_D2R_N	TRUE	TRUE	NC_SATA_B_D2RN 87
11	SATA_B_D2R_P	TRUE	TRUE	NC_SATA_B_D2RP 87
11	SATA_B_R2D_C_N	TRUE	TRUE	NC_SATA_B_R2D_CN 87
11	SATA_B_R2D_C_P	TRUE	TRUE	NC_SATA_B_R2D_CP 87
11	TP_SATA_ODD_D2RN	TRUE	TRUE	NC_SATA_ODD_D2RN
11	TP_SATA_ODD_D2RP	TRUE	TRUE	NC_SATA_ODD_D2RP
11	TP_SATA_ODD_R2D_CN	TRUE	TRUE	NC_SATA_ODD_R2D_CN
11	TP_SATA_ODD_R2D_CP	TRUE	TRUE	NC_SATA_ODD_R2D_CP
11	TP_SATA_D_D2RN	TRUE	TRUE	NC_SATA_D_D2RN
11	TP_SATA_D_D2RP	TRUE	TRUE	NC_SATA_D_D2RP
11	TP_SATA_D_R2D_CN	TRUE	TRUE	NC_SATA_D_R2D_CN
11	TP_SATA_D_R2D_CP	TRUE	TRUE	NC_SATA_D_R2D_CP
11	TP_SATA_F_D2RN	TRUE	TRUE	NC_SATA_F_D2RN
11	TP_SATA_F_D2RP	TRUE	TRUE	NC_SATA_F_D2RP
11	TP_SATA_F_R2D_CN	TRUE	TRUE	NC_SATA_F_R2D_CN
11	TP_SATA_F_R2D_CP	TRUE	TRUE	NC_SATA_F_R2D_CP
13	USB_EXTC_N	TRUE	TRUE	NC_USB_EXTCN 87
13	USB_EXTC_P	TRUE	TRUE	NC_USB_EXTCP 87
13	TP_USB_SDN	TRUE	TRUE	NC_USB_SDN 87
13	TP_USB_SDP	TRUE	TRUE	NC_USB_SDP 87
13	TP_USB_WLANN	TRUE	TRUE	NC_USB_WLANN
13	TP_USB_WLANP	TRUE	TRUE	NC_USB_WLANP
13	TP_USB_6N	TRUE	TRUE	NC_USB_6N 87
13	TP_USB_6P	TRUE	TRUE	NC_USB_6P 87
13	TP_USB_7N	TRUE	TRUE	NC_USB_7N 87
13	TP_USB_7P	TRUE	TRUE	NC_USB_7P 87
13	USB_EXTD_N	TRUE	TRUE	NC_USB_EXTDN 87
13	USB_EXTD_P	TRUE	TRUE	NC_USB_EXTDP 87
13	TP_USB_PSOCN	TRUE	TRUE	NC_USB_PSOCN
13	TP_USB_PSOCP	TRUE	TRUE	NC_USB_PSOCP
13	USB_IR_N	TRUE	TRUE	NC_USB_IRN 87
13	USB_IR_P	TRUE	TRUE	NC_USB_IRP 87
86 11	ITPXDP_CLK100M_N	TRUE	TRUE	NC_ITPXDP_CLK100MN
86 11	ITPXDP_CLK100M_P	TRUE	TRUE	NC_ITPXDP_CLK100MP
12	TP_PCI_PME_L	TRUE	TRUE	NC_PCI_PME_L
20 11	TP_PCI_CLK33M_OUT2	TRUE	TRUE	NC_PCI_CLK33M_OUT2
11	TP_PCI_CLK33M_OUT3	TRUE	TRUE	NC_PCI_CLK33M_OUT3
11	TP_HDA_SDIN1	TRUE	TRUE	NC_HDA_SDIN1
11	TP_HDA_SDIN2	TRUE	TRUE	NC_HDA_SDIN2
11	TP_HDA_SDIN3	TRUE	TRUE	NC_HDA_SDIN3
13	TP_LPC_DREQ0_L	TRUE	TRUE	NC_LPC_DREQ0_L
13	TP_CLINK_CLK	TRUE	TRUE	NC_CLINK_CLK
13	TP_CLINK_DATA	TRUE	TRUE	NC_CLINK_DATA
13	TP_CLINK_RESET_L	TRUE	TRUE	NC_CLINK_RESET_L
12	EDP_IG_BKL_PWM	TRUE	TRUE	NC_EDP_IG_BKL_PWM
87	USB_SMC_P	TRUE	TRUE	NC_USB_SMCP
87	USB_SMC_N	TRUE	TRUE	NC_USB_SMCN
	SMC_INTERFACE_2	TRUE	TRUE	NC_SMC_INTERFACE_2

Thunderbolt

		NO_TEST	MAKE_BASE	
28	TP_TBT_XTAL25OUT	TRUE	TRUE	NC_TBT_XTAL25OUT
28	TP_DP_TBTSRC_ML_CP<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CP<3..0>
28	TP_DP_TBTSRC_ML_CN<3..0>	TRUE	TRUE	NC_DP_TBTSRC_ML_CN<3..0>
28	TP_DP_TBTSRC_AUXCH_CP	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CP
28	TP_DP_TBTSRC_AUXCH_CN	TRUE	TRUE	NC_DP_TBTSRC_AUXCH_CN
12	TP_DP_IG_D_AUXCHN	TRUE	TRUE	NC_DP_IG_D_AUXCHN
12	TP_DP_IG_D_AUXCHP	TRUE	TRUE	NC_DP_IG_D_AUXCHP
11	TP_PCIE_CLK100M_PE5N	TRUE	TRUE	NC_PCIE_CLK100M_PE5N
11	TP_PCIE_CLK100M_PE5P	TRUE	TRUE	NC_PCIE_CLK100M_PE5P
11	PCIE_CLK100M_ENETSD_N	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDN
11	PCIE_CLK100M_ENETSD_P	TRUE	TRUE	NC_PCIE_CLK100M_ENETSDP
11	TP_PCIE_CLK100M_ENETN	TRUE	TRUE	NC_PCIE_CLK100M_ENETN
11	TP_PCIE_CLK100M_ENETP	TRUE	TRUE	NC_PCIE_CLK100M_ENETP
11	TP_PCIE_CLK100M_PEGBN	TRUE	TRUE	NC_PCIE_CLK100M_PEGBN
11	TP_PCIE_CLK100M_PEGBP	TRUE	TRUE	NC_PCIE_CLK100M_PEGBP
11	TP_PCIE_CLK100M_SWN	TRUE	TRUE	NC_PCIE_CLK100M_SWN
11	TP_PCIE_CLK100M_SWP	TRUE	TRUE	NC_PCIE_CLK100M_SWP
11	TP_PCH_GPIO64_CLKOUTFLEX0	TRUE	TRUE	NC_PCH_GPIO64_CLKOUTFLEX0
11	TP_PCH_GPIO65_CLKOUTFLEX1	TRUE	TRUE	NC_PCH_GPIO65_CLKOUTFLEX1
11	TP_PCH_GPIO66_CLKOUTFLEX2	TRUE	TRUE	NC_PCH_GPIO66_CLKOUTFLEX2
11	TP_PCH_GPIO67_CLKOUTFLEX3	TRUE	TRUE	NC_PCH_GPIO67_CLKOUTFLEX3
13	TP_USB_4N	TRUE	TRUE	NC_USB_4N
13	TP_USB_4P	TRUE	TRUE	NC_USB_4P

	TRUE	PCIE_TBT_R2D_P<3..0>	28 86
	TRUE	PCIE_TBT_R2D_N<3..0>	28 86
	TRUE	PCIE_TBT_D2R_C_P<3..0>	28 86
	TRUE	PCIE_TBT_D2R_C_N<3..0>	28 86
H107	TRUE	DMI_S2N_P<3..1>	5 12 86
H107	TRUE	DMI_S2N_N<3..1>	5 12 86
H107	TRUE	DMI_N2S_P<3..1>	5 12 86
H107	TRUE	DMI_N2S_N<3..1>	5 12 86

PLACEABLE BEAD-PROBES FOR TBT

90 31 28	TBT_A_R2D_C_P<1>	1	TP SM	BEAD-PROBE BPA535 NO_XNET_CONNECTION=TRUE
90 31 28	TBT_A_D2R_P<1>	1	TP SM	BEAD-PROBE BPA531 NO_XNET_CONNECTION=TRUE
90 31 28	TBT_A_D2R_N<1>	1	TP SM	BEAD-PROBE BPA532 NO_XNET_CONNECTION=TRUE

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J15 BOARD-SPECIFIC SPACING & PHYSICAL CONSTRAINTS

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA,P65BGA	MM	16.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=45_OHM_SE	=45_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.095 MM	0.095 MM			
50_OHM_SE	*	Y	0.066 MM	0.066 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE	*	Y	0.083 MM	0.083 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE_ADJ	TOP,BOTTOM	Y	0.116 MM	0.116 MM			
45_OHM_SE_ADJ	*	Y	0.085 MM	0.085 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.145 MM	0.095 MM			
40_OHM_SE	*	Y	0.102 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.095 MM			
37_OHM_SE	*	Y	0.118 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.265 MM	0.095 MM			
27P4_OHM_SE	*	Y	0.186 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	ISL2,ISL11	Y	0.105 MM	0.105 MM		0.120 MM	0.120 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.146 MM	0.146 MM		0.120 MM	0.120 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	ISL2,ISL11	Y	0.096 MM	0.096 MM		0.126 MM	0.126 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.120 MM	0.120 MM		0.160 MM	0.160 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	ISL2,ISL11	Y	0.080 MM	0.080 MM		0.120 MM	0.120 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.105 MM	0.105 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4,ISL9,ISL10	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	ISL2,ISL11	Y	0.078 MM	0.078 MM		0.200 MM	0.200 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.101 MM	0.101 MM		0.180 MM	0.180 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	P072_SPACE
*	*	P65BGA	P075_SPACE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	0.1 MM	?
BGA_P2MM	*	0.2 MM	?
P072_SPACE	*	0.071 MM	?
P075_SPACE	*	0.075 MM	?

Stackup-Defined Spacing Rules

Note: Outer dielectric is 0.058 mm nominal,
Inner dielectric is 0.053 mm nominal.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1:1_SPACING	·	0.1 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1x_DIELECTRIC	TOP,BOTTOM	0.058 MM	?
1x_DIELECTRIC	ISL3,ISL4,ISL9,ISL10	0.053 MM	?
1x_DIELECTRIC	ISL2,ISL5,ISL6,ISL7,ISL8,ISL11	0.101 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
P65_BGA	*	Y	0.071MM	0.071MM		0.075MM	0.126MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
*	P65BGA	P65_BGA

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL
CPU_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?
CPU_VID	*	0.457 MM	?
CPU_VREF	*	12 MIL	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: IVB PLATFORM DG , Tables 205-207

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	*	=3X_DIELECTRIC	?
DMI_TXRX	*	=6X_DIELECTRIC	?
DMICLK2N2S	*	=6X_DIELECTRIC	?
DMICLK2S2N	*	=3X_DIELECTRIC	?
DMICLK2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DMI_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
DMI_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2N2S	TOP,BOTTOM	=10X_DIELECTRIC	?
DMICLK2S2N	TOP,BOTTOM	=6X_DIELECTRIC	?
DMICLK2OTHER	TOP,BOTTOM	=4X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DMI_*	=SAME	*	DMI_2SAME
DMI_N2S	DMI_S2N	*	DMI_TXRX
DMI_S2N	DMI_N2S	*	DMI_TXRX
CLK_DMI	DMI_N2S	*	DMICLK2N2S
CLK_DMI	DMI_S2N	*	DMICLK2S2N
CLK_DMI	*	*	DMICLK2OTHER

PEG - SSD & TBT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PEG_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	*	=3X_DIELECTRIC	?
PEG_TXRX	*	=6X_DIELECTRIC	?
PEG_2OTHER	*	=4X_DIELECTRIC	?
PEG_2CLK	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PEG_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PEG_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PEG_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PEG_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PEG_*	=SAME	*	PEG_2SAME
PEG_R2D	PEG_D2R	*	PEG_TXRX
PEG_*	*	*	PEG_2OTHER
PEG_*	CLK_*	*	PEG_2CLK

DIGITAL VIDEO SIGNAL CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	*	=3x_DIELECTRIC	?
DP_2OTHER	*	=4x_DIELECTRIC	?
HDMICLK_2CLK	*	=7x_DIELECTRIC	?
HDMICLK_2DP	*	=4x_DIELECTRIC	?
HDMICLK_2OTHER	*	=7x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
DP_2OTHER	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2CLK	TOP,BOTTOM	=10x_DIELECTRIC	?
HDMICLK_2DP	TOP,BOTTOM	=6x_DIELECTRIC	?
HDMICLK_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
DISPLAYPORT	=SAME	*	DP_2SAME
DISPLAYPORT	*	*	DP_2OTHER
HDMI_CLK	CLK_*	*	HDMICLK_2CLK
HDMI_CLK	DISPLAYPORT	*	HDMICLK_2DP
HDMI_CLK	*	*	HDMICLK_2OTHER

DisplayPort/TMDS intra-pair matching should be 0.127mm. Inter-pair matching should be within 2.54cm. Max Length 241.3mm.
DIsplayPort AUX CH intra-pair matching should be 0.127mm. Max length 330.2mm.
SOURCE: Calpella SFF DG Rev 1.5 (407364) and Family GPU DG-04202-001-v04.
MAX LENGTH OF DISPLAYPORT/TMDS TRACES: 13 INCHES.

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N P<3:0>	5 12 84
DMI_S2N	CPU_85D	DMI_S2N	DMI_S2N N<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S P<3:0>	5 12 84
DMI_N2S	CPU_85D	DMI_N2S	DMI_N2S N<3:0>	5 12 84
FDI_INT	CPU_50S	CPU_AGTL	FDI_INT	5 12
FDI_CSYNC	CPU_50S	CPU_AGTL	FDI_CSYNC	5 12
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_P	6 11
DMI_CLK	CPU_85D	CLK_DMI	DMI_CLK100M_CPU_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLREF_P	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_N	6 11
CPU_CLK135_PLL	CPU_85D	CLK_PCIE	CPU_CLK135M_DPLLSS_P	6 11
CPU_EDP_COMP	CPU_27P4S	CPU_COMP	CPU_EDP_RCOMP	5
CPU_PEG_COMP	CPU_27P4S	CPU_COMP	CPU_PEG_RCOMP	5
CPU_CFG	CPU_45S	CPU_ITP	CPU_CFG<19..0>	6 18 83
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP_CLK100M_P	11 84
XDP_CLK_PCH	CLK_PCIE_85D	CLK_PCIE	ITPXDP_CLK100M_N	11 84
XDP_TDI	CPU_45S	CPU_ITP	XDP_CPU_TDI	6 18 83
XDP_TDO	CPU_45S	CPU_ITP	XDP_CPU_TDO	6 18 83
XDP_TMS	CPU_45S	CPU_ITP	XDP_CPU_TMS	6 18 83
XDP_TCK	CPU_45S	CPU_ITP	XDP_CPU_TCK	6 18 83
XDP_TRST_L	CPU_45S	CPU_ITP	XDP_CPU_TRST_L	6 18 83
XDP_BPM	CPU_45S	CPU_ITP	XDP_BPM_L<3..0>	6 18
XDP_BPM_L	CPU_45S	CPU_ITP	XDP_BPM_L<7..4>	6 18
XDP_BDRESET_L	CPU_45S	CPU_ITP	XDP_DBRESET_L	6 18 19
XDP_PRDY_L	CPU_45S	CPU_ITP	XDP_CPU_PRDY_L	6 18 83
XDP_PREQ_L	CPU_45S	CPU_ITP	XDP_CPU_PREQ_L	6 18 83
CPU_CATERR_L	CPU_45S	CPU_AGTL	CPU_CATERR_L	6 40
CPU_PECI	CPU_45S	CPU_VID	CPU_PECI	6 14 41
CPU_PROCHOT_L	CPU_45S	CPU_AGTL	CPU_PROCHOT_L	6 40 41 57
CPU_PWRGD	CPU_45S	CPU_AGTL	CPU_PWRGD	6 14 18
PM_THRMTRIP_L	CPU_45S	CPU_8MTI	PM_THRMTRIP_L	6 14 41
PM_MEM_PWRGD	CPU_45S	CPU_AGTL	PM_MEM_PWRGD	6 12 21
PM_SYNC	CPU_45S	CPU_AGTL	PM_SYNC	6 12
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2..0>	6
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSOUT	8 57
CPU_VID	CPU_45S	CPU_VID	CPU_VIDSCLK	8 57
CPU_VID	CPU_45S	CPU_VID	CPU_VIDALERT_L	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 57
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	9 57
CPU_MEM_VREF		CPU_VREF	CPU_DIMMA_VREFDQ	7 22
CPU_MEM_VREF		CPU_VREF	CPU_DIMMB_VREFDQ	7 22
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFDQ_B	22 25 26 82
CPU_MEM_VREF		MEM_PWR	PPVREF_S3_MEM_VREFCA_A	22 23 24 82 89
CPU_MEM_VREF		CPU_VREF	PPVREF_S3_MEM_VREFCA_B	22 25 26 82
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R P<7..0>	66 68 82
PEG_D2R	PEG_80D	PEG_D2R	PEG_D2R N<7..0>	66 68 82
	PEG_80D	PEG_D2R	PEG_D2R_C_P<7..0>	68
	PEG_80D	PEG_D2R	PEG_D2R_C_N<7..0>	68
	PEG_80D	PEG_R2D	PEG_R2D_P<7..0>	66 68
	PEG_80D	PEG_R2D	PEG_R2D_N<7..0>	66 68
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_P<7..0>	68 82
PEG_R2D	PEG_80D	PEG_R2D	PEG_R2D_C_N<7..0>	68 82
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_P<3..0>	28 82
PEG_D2R_TBT	CPU_85D	PEG_D2R	PCIE_TBT_D2R_N<3..0>	28 82
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_P<3..0>	28 84
	CPU_85D	PEG_D2R	PCIE_TBT_D2R_C_N<3..0>	28 84
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_P<3..0>	28 84
PEG_R2D_TBT	CPU_85D	PEG_R2D	PCIE_TBT_R2D_N<3..0>	28 84
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_P<3..0>	28 82
	CPU_85D	PEG_R2D	PCIE_TBT_R2D_C_N<3..0>	28 82

DP AUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	67 79 94
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	67 79 94
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>	67 94
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>	67 94
	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>	67 83 86 94
	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>	67 83 86 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	67 79 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	67 79 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P	67 83 94
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N	67 83 94
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPA_IG_AUX_CH_N	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_P	80 82
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DPB_IG_AUX_CH_N	80 82

DP / HDMI NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_P<2..0>	83
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_DATA_N<2..0>	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_P	83
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_CLK_N	83
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>	28 74 94
DP_TBT_ML0	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>	28 74 94
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>	28 94
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>	28 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>	28 74 94
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>	28 74 94
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>	28 94
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>	28 94
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_P	28 94
TBTSNK0_AUXCH	DP_85D		DP_TBTSNK0_AUXCH_N	28 94
	DP_85D		DP_TBTSNK0_AUXCH_C_P	28 80 94
	DP_85D		DP_TBTSNK0_AUXCH_C_N	28 80 94
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_P	28 94
TBTSNK1_AUXCH1	DP_85D		DP_TBTSNK1_AUXCH_N	28 94
	DP_85D		DP_TBTSNK1_AUXCH_C_P	28 80 94
	DP_85D		DP_TBTSNK1_AUXCH_C_N	28 80 94

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: CPU Constraints

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
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SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
SATA_37SE	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE
SATA_45SE	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	*	=3X_DIELECTRIC	?
SATA_TXRX	*	=6X_DIELECTRIC	?
SATA_2OTHER	*	=4X_DIELECTRIC	?
SATA_RCOMP	*	=6X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
SATA_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
SATA_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
SATA_RCOMP	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
SATA_*	=SAME	*	SATA_2SAME
SATA_R2D	SATA_D2R	*	SATA_TXRX
SATA_*	*	*	SATA_2OTHER

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=4X_DIELECTRIC	?
USB_RBIAS	*	=6X_DIELECTRIC	?
BT_WAKE	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=6X_DIELECTRIC	?
USB_RBIAS	TOP,BOTTOM	=10X_DIELECTRIC	?
BT_WAKE	TOP,BOTTOM	=6X_DIELECTRIC	?

USB 3.0 INTERFACE CONSTRAINTS

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB3_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	*	=3X_DIELECTRIC	?
USB3_TXRX	*	=6X_DIELECTRIC	?
USB3_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB3_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
USB3_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
USB3_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
USB3_*	=SAME	*	USB3_2SAME
USB3_R2D	USB3_D2R	*	USB3_TXRX
USB3_*	*	*	USB3_2OTHER

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_25M_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=4x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.
NOTE: Latest Intel DG calls out 50ohms SE for sys clocks

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CP	84
	SATA_85D	SATA_R2D	NC_SATA_A_R2D_CN	84
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RP	84
T27	SATA_85D	SATA_D2R	NC_SATA_A_D2RN	84
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CP	84
T29	SATA_85D	SATA_R2D	NC_SATA_B_R2D_CN	84
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RP	84
T30	SATA_85D	SATA_D2R	NC_SATA_B_D2RN	84
T21 PCH_SATA_RCOMP	SATA_45SE	SATA_RCOMP	PCH_SATA_RCOMP	11
USB_EXTA	USB_85D	USB	USB_EXTA_P	13 37
USB_EXTA	USB_85D	USB	USB_EXTA_N	13 37
T24 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_P	37
T24 USB_EXTA	USB_85D	USB	USB_EXTA_MUXED_N	37
T23 USB_EXTA	USB_85D	USB	USB_LT1_P	37
T23 USB_EXTA	USB_85D	USB	USB_LT1_N	37
USB_NC	USB_85D	USB	NC_USB_EXTCP	84
USB_NC	USB_85D	USB	NC_USB_EXTCN	84
T23 USB_NC	USB_85D	USB	NC_USB_SDP	84
T23 USB_NC	USB_85D	USB	NC_USB_SDN	84
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_RX_L	37 40 41
T27	CPU_45S	CPU_ITP	SMC_DEBUGPRT_TX_L	37 40 41
USB_SMC	USB_85D	USB	USB_SMC_P	84
USB_SMC	USB_85D	USB	USB_SMC_N	84
T28 USB_NC	USB_85D	USB	NC_USB_6P	84
T28 USB_NC	USB_85D	USB	NC_USB_6N	84
T28 USB_NC	USB_85D	USB	NC_USB_7P	84
T28 USB_NC	USB_85D	USB	NC_USB_7N	84
USB_EXTB	USB_85D	USB	USB_EXTB_P	13 78 83
USB_EXTB	USB_85D	USB	USB_EXTB_N	13 78 83
T26 USB_NC	USB_85D	USB	NC_USB_EXTDP	84
T25 USB_NC	USB_85D	USB	NC_USB_EXTDN	84
USB_BT	USB_85D	USB	USB_BT_P	13 33
USB_BT	USB_85D	USB	USB_BT_N	13 33
	USB_85D	USB	USB_BT_CONN_P	33 83
	USB_85D	USB	USB_BT_CONN_N	33 83
T28 USB_NC	USB_85D	USB	NC_USB_IRP	84
T28 USB_NC	USB_85D	USB	NC_USB_IRN	84
T28 USB_TPAD	USB_85D	USB	USB_TPAD_P	13 38
T28 USB_TPAD	USB_85D	USB	USB_TPAD_N	13 38
T30	USB_85D	USB	USB_TPAD_R_P	38
T30	USB_85D	USB	USB_TPAD_R_N	38
PCH_USB_RBIAS	PCH_USB_RBIAS	USB_RBIAS	PCH_USB_RBIAS	13
T22 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_P	13 37
T23 USB3_EXTA_RX	USB_85D	USB3_D2R	USB3_EXTA_D2R_N	13 37
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTA_D2R_C_N	
T23 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_P	37
T22 USB3_EXTA_TX	USB_85D	USB3_R2D	USB3_EXTA_R2D_N	37
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_P	13 37
T26	USB_85D	USB3_R2D	USB3_EXTA_R2D_C_N	13 37
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_P	13 78 83
T22 USB3_EXTB_RX	USB_85D	USB3_D2R	USB3_EXTB_D2R_N	13 78 83
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_P	
T26	USB_85D	USB3_D2R	USB3_EXTB_D2R_C_N	
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_P	78 83
T22 USB3_EXTB_TX	USB_85D	USB3_R2D	USB3_EXTB_R2D_N	78 83
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_P	13 78
T26	USB_85D	USB3_R2D	USB3_EXTB_R2D_C_N	13 78
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RP	84
T26 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTC_D2RN	84
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CP	84
T26	USB_85D	USB3_R2D	NC_USB3_EXTC_R2D_CN	84
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RP	84
T25 NC_USB3	USB_85D	USB3_D2R	NC_USB3_EXTD_D2RN	84
T25	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CP	84
T25	USB_85D	USB3_R2D	NC_USB3_EXTD_R2D_CN	84

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T25 SYSCLK_CLK32K_RTC	CLK_SLOW_45S	CLK_SLOW	SYSCLK_CLK32K_RTC	11 19
T25 SYSCLK_CLK25M_SB	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB	11 19
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_SB_R	11
T25 SYSCLK_CLK25M_CAM	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_CAMERA	19 36
T25 SYSCLK_CLK25M_TBT	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT	19 28
T25	CLK_25M_45S	CLK_25M	SYSCLK_CLK25M_TBT_R	28

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

PCH Single Net Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCH_SE	TOP,BOTTOM	=3x_DIELECTRIC	?

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	*	=2X_DIELECTRIC	?
PCIE_TXRX	*	=6X_DIELECTRIC	?
PCIE_2OTHER	*	=4X_DIELECTRIC	?
PCIE_2CLK	*	=7X_DIELECTRIC	?
PCIECLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE_2SAME	TOP,BOTTOM	=4X_DIELECTRIC	?
PCIE_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIE_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
PCIE_2CLK	TOP,BOTTOM	=10X_DIELECTRIC	?
PCIECLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
PCIE_*	=SAME	*	PCIE_2SAME
PCIE_R2D	PCIE_D2R	*	PCIE_TXRX
PCIE_*	*	*	PCIE_2OTHER
PCIE_*	CLK_*	*	PCIE_2CLK
CLK_PCIE	*	*	PCIECLK_2OTHER

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
LPC_AD	LPC_45S	LPC	LPC_AD<3..0>	13 40 49 79 83
LPC_FRAME_L	LPC_45S	LPC	LPC_FRAME_L	13 40 49 79 83
LPC_RESET_L	LPC_45S	LPC	LPC_RESET_L	20
SMBUS_PCH_CLK	SMB_45S	SMB	SMBUS_PCH_CLK	13 43 83
SMBUS_PCH_DATA	SMB_45S	SMB	SMBUS_PCH_DATA	13 43 83
SMBUS_PCH_0_CLK	SMB_45S	SMB	SML_PCH_0_CLK	13 43
SMBUS_PCH_0_DATA	SMB_45S	SMB	SML_PCH_0_DATA	13 43
SMBUS_PCH_1_CLK	SMB_45S	SMB	SML_PCH_1_CLK	13 43
SMBUS_PCH_1_DATA	SMB_45S	SMB	SML_PCH_1_DATA	13 43
HDA_BIT_CLK	HDA_45S	HDA	HDA_BIT_CLK	11 51
	HDA_45S	HDA	HDA_BIT_CLK_R	11
HDA_SYNC	HDA_45S	HDA	HDA_SYNC	11 51
	HDA_45S	HDA	HDA_SYNC_R	11
	HDA_45S	HDA	HDA_RST_R_L	11
HDA_RST_L	HDA_45S	HDA	HDA_RST_L	11 51
HDA_SDIN0	HDA_45S	HDA	HDA_SDIN0	11 51
HDA_SDIN0_R	HDA_45S	HDA	CS4208_HDA_SDOUT0_R	51
HDA_SDOUT	HDA_45S	HDA	HDA_SDOUT	11 51
	HDA_45S	HDA	HDA_SDOUT_R	11 19
	SPI_45S	SPI	SPI_CLK_R	13 49
SPI_CLK	SPI_45S	SPI	SPI_CLK	49
	SPI_45S	SPI	SPI_MOSI_R	13 49
SPI_MOSI	SPI_45S	SPI	SPI_MOSI	49
SPI_MISO	SPI_45S	SPI	SPI_MISO	13 49
	SPI_45S	SPI	SPI_CS0_R_L	13 49
SPI_CS0	SPI_45S	SPI	SPI_CS0_L	49
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_P	20 78 83
USB3_SD_R2D	USB3_85D	USB3_R2D	USB3_SD_R2D_C_N	20 78 83
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_P	20 78 83
USB3_SD_D2R	USB3_85D	USB3_D2R	USB3_SD_D2R_N	20 78 83
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_P	33 83
PCIE_AP_R2D	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_N	33 83
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_P	13 33
[184]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_C_N	13 33
	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_P	33
[185]	PCIE_85D	PCIE_R2D	PCIE_AP_R2D_PI_N	33
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_P	13 33
PCIE_AP_D2R	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_N	13 33
[276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_P	33 83
[276]	PCIE_85D	PCIE_D2R	PCIE_AP_D2R_PI_N	33 83
[325] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_P	35 36
[326] PCIE_CAMERA_R2D	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_N	35 36
[327]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_P	13 36
[328]	PCIE_85D	PCIE_R2D	PCIE_CAMERA_R2D_C_N	13 36
[329] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_P	13 36
[330] PCIE_CAMERA_D2R	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_N	13 36
[331]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_P	35 36
[332]	PCIE_85D	PCIE_D2R	PCIE_CAMERA_D2R_C_N	35 36
	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC_R	11 19
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_SMC	19 40
PCH_LPC_CLK0	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS	19 49 83
[240]	CLK_LPC_45S	CLK_LPC	LPC_CLK33M_LPCPLUS_R	11 19
[249] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIIN	11 19
[250] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK14P3M_REFCLK	11
[288] PCIE_CLK100M	CPU_45S	CLK_PCIE	PCH_CLK33M_PCIOUT	11 19
[253] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_P	11
[254] PCIE_CLK100M_PCH	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_PCH_N	11
[255] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_P	11 28
[256] PCIE_CLK100M_TBT	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_TBT_N	11 28
[257] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_P	11
[258] PCIE_CLK100M_DOT	CLK_PCIE_85D	CLK_PCIE	PCH_CLK96M_DOT_N	11
[259] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_P	11
[260] PCIE_CLK100M_SATA	PCIE_85D	CLK_PCIE	PCH_CLK100M_SATA_N	11
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_P	68 82 83
PEG_CLK100M	PEG_80D	CLK_PCIE	PEG_CLK100M_N	68 82 83
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_P	11 33
PCIE_CLK100M_AP	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_N	11 33
[189]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	33 83
[190]	PCIE_85D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	33 83
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_P	11 36
PCIE_CLK100M_S2	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_N	11 36
[333]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_P	35 36
[334]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_CAMERA_C_N	35 36
[285] PCIE_CLK100M_ENET	PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_P	11 34
[286]	CLK_PCIE_85D	CLK_PCIE	PCIE_CLK100M_SSD_N	11 34

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
[313] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTRUDER_L	11
[314] PCH_PM_NET	PCH_45S	PCH_SE	PCH_INTVRMEN_L	11
[315] PCH_PM_NET	PCH_45S	PCH_SE	PCH_DSWVRMEN	12
[316] PCH_PM_NET	PCH_45S	PCH_SE	PCH_SRTCRST_L	11
[308] PCH_PM_NET	PCH_45S	PCH_SE	PM_RSMRST_L	12 65 83
[307] PCH_PM_NET	PCH_45S	PCH_SE	PM_SYSRST_L	12 19 40 83
[318] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_PWROK	12 19 83
[317] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_APWROK	12 19
[320] PCH_PM_NET	PCH_45S	PCH_SE	PM_DSW_PWRGD	12 40 83
[319] PCH_PM_NET	PCH_45S	PCH_SE	PM_PCH_SYS_PWROK	12 18 19 40 83
[309] PCH_PM_NET	PCH_45S	PCH_SE	PM_PWRBTN_L	12 18 40
[306] PCH_PM_NET	PCH_45S	PCH_SE	PM_THRMTRIP_L_R	14 41
[324] PCH_PCIE_WAKE	PCH_45S	PCH_SE	PCIE_WAKE_L	12 33 35 83
[321] PCH_PM_NET	PCH_45S	PCH_SE	PCH_RCIN_L	14
[335] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_P<3..0>	13 34
[336] PCIE_D2R_SSD	PCIE_85D	PCIE_D2R	PCIE_SSD_D2R_N<3..0>	13 34
[338] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_P<3..0>	13 34
[337] PCIE_R2D_SSD	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_C_N<3..0>	13 34
[339]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_P<3..0>	34
[340]	PCIE_85D	PCIE_R2D	PCIE_SSD_R2D_N<3..0>	34

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	*	=2x_DIELECTRIC	?
MEM_DQS2OWNDATA	*	=2x_DIELECTRIC	?
MEM_CMD2CMD	*	=2x_DIELECTRIC	?
MEM_CMD2CTRL	*	=2x_DIELECTRIC	?
MEM_CTRL2CTRL	*	=2x_DIELECTRIC	?
MEM_CLK2CLK	*	=4x_DIELECTRIC	?
MEM_2OTHERMEM	*	=4x_DIELECTRIC	?
MEM_2PWR	*	=2x_DIELECTRIC	?
MEM_2GND	*	=2x_DIELECTRIC	?
MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_DATA2SELF	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_DQS2OWNDATA	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CMD	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CMD2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CTRL2CTRL	TOP,BOTTOM	=5x_DIELECTRIC	?
MEM_CLK2CLK	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2OTHERMEM	TOP,BOTTOM	=8x_DIELECTRIC	?
MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	*	*	MEM_2OTHER
MEM_*_DQS_*	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CLK	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_*_DATA_*	=SAME	*	MEM_DATA2SELF

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_CTRL	*	MEM_CMD2CTRL
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CLK	MEM_CLK	*	MEM_CLK2CLK
MEM_*	MEM_*	*	MEM_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_A_DQS_0	MEM_A_DATA_0	*	MEM_DQS2OWNDATA
MEM_A_DQS_1	MEM_A_DATA_1	*	MEM_DQS2OWNDATA
MEM_A_DQS_2	MEM_A_DATA_2	*	MEM_DQS2OWNDATA
MEM_A_DQS_3	MEM_A_DATA_3	*	MEM_DQS2OWNDATA
MEM_A_DQS_4	MEM_A_DATA_4	*	MEM_DQS2OWNDATA
MEM_A_DQS_5	MEM_A_DATA_5	*	MEM_DQS2OWNDATA
MEM_A_DQS_6	MEM_A_DATA_6	*	MEM_DQS2OWNDATA
MEM_A_DQS_7	MEM_A_DATA_7	*	MEM_DQS2OWNDATA
MEM_B_DQS_0	MEM_B_DATA_0	*	MEM_DQS2OWNDATA
MEM_B_DQS_1	MEM_B_DATA_1	*	MEM_DQS2OWNDATA
MEM_B_DQS_2	MEM_B_DATA_2	*	MEM_DQS2OWNDATA
MEM_B_DQS_3	MEM_B_DATA_3	*	MEM_DQS2OWNDATA
MEM_B_DQS_4	MEM_B_DATA_4	*	MEM_DQS2OWNDATA
MEM_B_DQS_5	MEM_B_DATA_5	*	MEM_DQS2OWNDATA
MEM_B_DQS_6	MEM_B_DATA_6	*	MEM_DQS2OWNDATA
MEM_B_DQS_7	MEM_B_DATA_7	*	MEM_DQS2OWNDATA

DDR3 (Memory Down):

DQ signals should be matched within 0.508mm of associated DQS pair
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQS to clock matching should be within [CLK-139.73mm] and [CLK-30.48mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-2.54mm] to [CLK+2.54mm] of CLK pairs.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to first DRAM device is 139.7mm max, to last DRAM device is 194.31mm max.

SOURCE: Double checked with Doc#486985 Chief River SFF Platform DG: Memory Down
SOURCE: Need to re-confirm CRW DG for memory down (Intel not yet provided)

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_PWR	MEM_*	*	MEM_2PWR
MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	MEM_*	*	MEM_2GND

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_P<0> 7 23 27
MEM_A_CLK0	MEM_72D	MEM_CLK	MEM_A_CLK_N<0> 7 23 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_P<1> 7 24 27
MEM_A_CLK1	MEM_72D	MEM_CLK	MEM_A_CLK_N<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CKE<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CKE<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_CS_L<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_CS_L<1> 7 24 27
MEM_A_CNTL0	MEM_40S	MEM_CTRL	MEM_A_ODT<0> 7 23 27
MEM_A_CNTL1	MEM_40S	MEM_CTRL	MEM_A_ODT<1> 7 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0> 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L 7 23 24 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L 7 23 24 27
MEM_A_DATA_0	MEM_45S	MEM_A_DATA_0	MEM_A_DQ<7..0> 7 23 24
MEM_A_DATA_1	MEM_45S	MEM_A_DATA_1	MEM_A_DQ<15..8> 7 23 24
MEM_A_DATA_2	MEM_45S	MEM_A_DATA_2	MEM_A_DQ<23..16> 7 23 24
MEM_A_DATA_3	MEM_45S	MEM_A_DATA_3	MEM_A_DQ<31..24> 7 23 24
MEM_A_DATA_4	MEM_45S	MEM_A_DATA_4	MEM_A_DQ<39..32> 7 23 24
MEM_A_DATA_5	MEM_45S	MEM_A_DATA_5	MEM_A_DQ<47..40> 7 23 24
MEM_A_DATA_6	MEM_45S	MEM_A_DATA_6	MEM_A_DQ<55..48> 7 23 24
MEM_A_DATA_7	MEM_45S	MEM_A_DATA_7	MEM_A_DQ<63..56> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_P<0> 7 23 24
MEM_A_DQS0	MEM_85D	MEM_A_DQS_0	MEM_A_DQS_N<0> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_P<1> 7 23 24
MEM_A_DQS1	MEM_85D	MEM_A_DQS_1	MEM_A_DQS_N<1> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_P<2> 7 23 24
MEM_A_DQS2	MEM_85D	MEM_A_DQS_2	MEM_A_DQS_N<2> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_P<3> 7 23 24
MEM_A_DQS3	MEM_85D	MEM_A_DQS_3	MEM_A_DQS_N<3> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_P<4> 7 23 24
MEM_A_DQS4	MEM_85D	MEM_A_DQS_4	MEM_A_DQS_N<4> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_P<5> 7 23 24
MEM_A_DQS5	MEM_85D	MEM_A_DQS_5	MEM_A_DQS_N<5> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_P<6> 7 23 24
MEM_A_DQS6	MEM_85D	MEM_A_DQS_6	MEM_A_DQS_N<6> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_P<7> 7 23 24
MEM_A_DQS7	MEM_85D	MEM_A_DQS_7	MEM_A_DQS_N<7> 7 23 24
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_P<0> 7 25 27
MEM_B_CLK0	MEM_72D	MEM_CLK	MEM_B_CLK_N<0> 7 25 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_P<1> 7 26 27
MEM_B_CLK1	MEM_72D	MEM_CLK	MEM_B_CLK_N<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CKE<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CKE<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_CS_L<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_CS_L<1> 7 26 27
MEM_B_CNTL0	MEM_40S	MEM_CTRL	MEM_B_ODT<0> 7 25 27
MEM_B_CNTL1	MEM_40S	MEM_CTRL	MEM_B_ODT<1> 7 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0> 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L 7 25 26 27
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L 7 25 26 27
MEM_B_DATA_0	MEM_45S	MEM_B_DATA_0	MEM_B_DQ<7..0> 7 25 26
MEM_B_DATA_1	MEM_45S	MEM_B_DATA_1	MEM_B_DQ<15..8> 7 25 26
MEM_B_DATA_2	MEM_45S	MEM_B_DATA_2	MEM_B_DQ<23..16> 7 25 26
MEM_B_DATA_3	MEM_45S	MEM_B_DATA_3	MEM_B_DQ<31..24> 7 25 26
MEM_B_DATA_4	MEM_45S	MEM_B_DATA_4	MEM_B_DQ<39..32> 7 25 26
MEM_B_DATA_5	MEM_45S	MEM_B_DATA_5	MEM_B_DQ<47..40> 7 25 26
MEM_B_DATA_6	MEM_45S	MEM_B_DATA_6	MEM_B_DQ<55..48> 7 25 26
MEM_B_DATA_7	MEM_45S	MEM_B_DATA_7	MEM_B_DQ<63..56> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_P<0> 7 25 26
MEM_B_DQS0	MEM_85D	MEM_B_DQS_0	MEM_B_DQS_N<0> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_P<1> 7 25 26
MEM_B_DQS1	MEM_85D	MEM_B_DQS_1	MEM_B_DQS_N<1> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_P<2> 7 25 26
MEM_B_DQS2	MEM_85D	MEM_B_DQS_2	MEM_B_DQS_N<2> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_P<3> 7 25 26
MEM_B_DQS3	MEM_85D	MEM_B_DQS_3	MEM_B_DQS_N<3> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_P<4> 7 25 26
MEM_B_DQS4	MEM_85D	MEM_B_DQS_4	MEM_B_DQS_N<4> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_P<5> 7 25 26
MEM_B_DQS5	MEM_85D	MEM_B_DQS_5	MEM_B_DQS_N<5> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_P<6> 7 25 26
MEM_B_DQS6	MEM_85D	MEM_B_DQS_6	MEM_B_DQS_N<6> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_P<7> 7 25 26
MEM_B_DQS7	MEM_85D	MEM_B_DQS_7	MEM_B_DQS_N<7> 7 25 26
		MEM_PWR	PPVREF_S3_MEM_VREFDQ_A 22 23 24 82 86
		MEM_PWR	PPVREF_S3_MEM_VREFCA_A 22 23 24 82 86
		MEM_PWR	PP1V35_S3_MEM 81

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

PAGE TITLE: Memory Constraints

Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D
REVISION: 6.0.0
BRANCH: dvt
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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

Thunderbolt SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBT_SPI_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBT_SPI	*	=2x_DIELECTRIC	?

Thunderbolt/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SOURCE: Bill Cornelius's Thunderbolt Routing Notes

TBT_DP Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
TBTDP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	*	=3X_DIELECTRIC	?
TBTDP_TXRX	*	=6X_DIELECTRIC	?
TBTDP_2OTHER	*	=4X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
TBTDP_2SAME	TOP,BOTTOM	=4x_DIELECTRIC	?
TBTDP_TXRX	TOP,BOTTOM	=10X_DIELECTRIC	?
TBTDP_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
TBTDP_*	=SAME	*	TBTDP_2SAME
TBTDP_R2D	TBTDP_D2R	*	TBTDP_TXRX
TBTDP_*	*	*	TBTDP_2OTHER

Thunderbolt/DP Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_P<1..0>	28 31 84
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_C_N<1..0>	28 31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_P<1..0>	31
TBT_A_R2D	TBTDP_85D	TBTDP_R2D	TBT_A_R2D_N<1..0>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<1>	28 31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_P<1>	31
DP_A_LSX_ML	DP_85D	DISPLAYPORT	DP_A_LSX_ML_N<1>	31
DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_P<3>	28 31
T802 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_C_N<3>	28 31
T810 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_P<3>	31
T811 DP_TBTPA_ML	DP_85D	DISPLAYPORT	DP_TBTPA_ML_N<3>	31
T807 DP_TBTPA_ML	DP_85D	DISPLAYPORT		
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<0>	31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<0>	28 31
TBT_A_D2R0	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<0>	28 31
T813 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_P<1>	31
T814 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_C_N<1>	31
T815 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_P<1>	28 31 84
T816 TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R_N<1>	28 31 84
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_P	31
TBT_A_D2R1	TBTDP_85D	TBTDP_D2R	TBT_A_D2R1_AUXDDC_N	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_P	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_C_N	28 31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_P	31
TBT_A_AUXCH	DP_85D		DP_TBTPA_AUXCH_N	31
T819 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_P<1..0>	28 32
T817 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_C_N<1..0>	28 32
T818 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_P<1..0>	32
T816 TBT_B_R2D	TBTDP_85D	TBTDP_R2D	TBT_B_R2D_N<1..0>	32
T823 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<1>	28 32
T822 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<1>	28 32
T820 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<1>	32
T824 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<1>	32
T825 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_P<1>	32
T826 DP_B_LSX_ML	DP_85D	DISPLAYPORT	DP_B_LSX_ML_N<1>	32
T832 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_P<3>	28 32
T830 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_C_N<3>	28 32
T828 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_P<3>	32
T826 DP_TBTPB_ML	DP_85D	DISPLAYPORT	DP_TBTPB_ML_N<3>	32
T831 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<0>	32
T829 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<0>	32
T827 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<0>	28 32
T825 TBT_B_D2R0	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<0>	28 32
T833 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_P<1>	32
T830 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_C_N<1>	32
T828 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_P<1>	28 32
T826 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R_N<1>	28 32
T824 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_P	32
T822 TBT_B_D2R1	TBTDP_85D	TBTDP_D2R	TBT_B_D2R1_AUXDDC_N	32
T834 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_P	28 32
T836 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_C_N	28 32
T838 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_P	32
T840 TBT_B_AUXCH	DP_85D		DP_TBTPB_AUXCH_N	32

Only used on dual-port hosts.

Thunderbolt IC Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: PHYSICAL	NET_TYPE: SPACING		
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_P<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_ML_C_N<3..0>	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_P	
	DP_85D	DISPLAYPORT	DP_TBTSRC_AUXCH_C_N	
TBT_SPI_CLK	TBT_SPI_45S	TBT_SPI	TBT_SPI_CLK	28
TBT_SPI_MOSI	TBT_SPI_45S	TBT_SPI	TBT_SPI_MOSI	28
TBT_SPI_MISO	TBT_SPI_45S	TBT_SPI	TBT_SPI_MISO	28
TBT_SPI_CS_L	TBT_SPI_45S	TBT_SPI	TBT_SPI_CS_L	28

Only used on hosts supporting Thunderbolt video-in

SYNC_MASTER=CLEAN_J45 SYNC_DATE=04/26/2013

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Apple Inc.

DRAWING NUMBER: 051-0675 SIZE: D

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MIPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MIPI_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	*	=4X_DIELECTRIC	?
MIPI_2CLK	*	=6X_DIELECTRIC	?
MIPICLK_2OTHER	*	=7X_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MIPI_2OTHER	TOP,BOTTOM	=6X_DIELECTRIC	?
MIPI_2CLK	TOP,BOTTOM	=8X_DIELECTRIC	?
MIPICLK_2OTHER	TOP,BOTTOM	=10X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MIPI_DATA	*	*	MIPI_2OTHER
MIPI_DATA	CLK_MIPI	*	MIPI_2CLK
CLK_MIPI	*	*	MIPICLK_2OTHER

Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
S2_MEM_45S	*	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
S2_MEM_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

Spacing Rule Sets

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	*	=2x_DIELECTRIC	?
S2_DQS2OWNDATA	*	=2x_DIELECTRIC	?
S2_CMD2CMD	*	=2x_DIELECTRIC	?
S2_CMD2CTRL	*	=2x_DIELECTRIC	?
S2_CTRL2CTRL	*	=2x_DIELECTRIC	?
S2_2OTHERMEM	*	=4x_DIELECTRIC	?
S2MEM_2PWR	*	=2x_DIELECTRIC	?
S2MEM_2GND	*	=2x_DIELECTRIC	?
S2MEM_2OTHER	*	=6x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
S2_DATA2SELF	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_DQS2OWNDATA	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CMD2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_CTRL2CTRL	TOP,BOTTOM	=4x_DIELECTRIC	?
S2_2OTHERMEM	TOP,BOTTOM	=6x_DIELECTRIC	?
S2MEM_2PWR	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2GND	TOP,BOTTOM	=4x_DIELECTRIC	?
S2MEM_2OTHER	TOP,BOTTOM	=10x_DIELECTRIC	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DATA*	*	*	S2MEM_2OTHER
S2_MEM_DQS*	*	*	S2MEM_2OTHER
S2_MEM_CMD	*	*	S2MEM_2OTHER
S2_MEM_CTRL	*	*	S2MEM_2OTHER
S2_MEM_CLK	*	*	S2MEM_2OTHER
S2_MEM_DATA*	=SAME	*	S2_DATA2SELF
S2_MEM_CMD	S2_MEM_CMD	*	S2_CMD2CMD
S2_MEM_CMD	S2_MEM_CTRL	*	S2_CMD2CTRL
S2_MEM_CTRL	S2_MEM_CTRL	*	S2_CTRL2CTRL
S2_MEM_*	S2_MEM_*	*	S2_2OTHERMEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_DQS1	S2_MEM_DATA1	*	S2_DQS2OWNDATA
S2_MEM_DQS0	S2_MEM_DATA0	*	S2_DQS2OWNDATA

Memory to Power Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
S2_MEM_PWR	S2_MEM_*	*	S2MEM_2PWR
S2_MEM_PWR	*	*	DEFAULT

Memory to GND Spacing

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
GND	S2_MEM_*	*	S2MEM_2GND

Camera Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING	
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_P 35 36
	S2_MEM_CLK	S2_MEM_85D	S2_MEM_CLK	MEM_CAM_CLK_N 35 36
	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CKE 35 36
161	S2_MEM_CNTL	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CS_L 35 36
162		S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_ODT 36
163	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_CAS_L 35 36
164	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CTRL	MEM_CAM_RAS_L 35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_WE_L 35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<0> 35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<1> 35 36
	S2_MEM_CMD	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_BA<2> 35 36
165	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_P<0> 35 36
	S2_MEM_DQS0	S2_MEM_85D	S2_MEM_DQS0	MEM_CAM_DQS_N<0> 35 36
166	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_P<1> 35 36
167	S2_MEM_DQS1	S2_MEM_85D	S2_MEM_DQS1	MEM_CAM_DQS_N<1> 35 36
168	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DM<0> 35 36
169	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DM<1> 35 36
147	S2_MEM_A	S2_MEM_45S	S2_MEM_CMD	MEM_CAM_A<14..0> 35 36
	S2_MEM_DATA_0	S2_MEM_45S	S2_MEM_DATA0	MEM_CAM_DQ<7..0> 35 36
	S2_MEM_DATA_1	S2_MEM_45S	S2_MEM_DATA1	MEM_CAM_DQ<15..8> 35 36
132	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_P 35 36
133	MIPI_DATA_S2	MIPI_85D	MIPI_DATA	MIPI_DATA_N 35 36
134		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_P 36 83
135		MIPI_85D	MIPI_DATA	MIPI_DATA_CONN_N 36 83
136	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_P 35 36
137	MIPI_CLK_S2	MIPI_85D	CLK_MIPI	MIPI_CLK_N 35 36
138		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_P 36 83
139		MIPI_85D	CLK_MIPI	MIPI_CLK_CONN_N 36 83
140			S2_MEM_PWR	PP1V35_CAM 35 36
140			S2_MEM_PWR	PP0V675_CAM_VREF 35 36
140			S2_MEM_PWR	PP0V675_MEM_CAM_VREFCA 36
140			S2_MEM_PWR	PP0V675_MEM_CAM_VREFDQ 36

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SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
SMBUS_SMC_2_S3_SCL	SMB_45S	SMB	SMBUS_SMC_2_S3_SCL	40 43
SMBUS_SMC_2_S3_SDA	SMB_45S	SMB	SMBUS_SMC_2_S3_SDA	40 43
SMBUS_SMC_1_S0_SCL	SMB_45S	SMB	SMBUS_SMC_1_S0_SCL	40 43
SMBUS_SMC_1_S0_SDA	SMB_45S	SMB	SMBUS_SMC_1_S0_SDA	40 43
SMBUS_SMC_0_S0_SCL	SMB_45S	SMB	SMBUS_SMC_0_S0_SCL	40 43
SMBUS_SMC_0_S0_SDA	SMB_45S	SMB	SMBUS_SMC_0_S0_SDA	40 43
SMBUS_SMC_5_SCL	SMB_45S	SMB	SMBUS_SMC_5_g3_SCL	40 43 83
SMBUS_SMC_5_SDA	SMB_45S	SMB	SMBUS_SMC_5_G3_SDA	40 43 83
SMBUS_SMC_3_SCL	SMB_45S	SMB	SMBUS_SMC_3_SCL	40 42
SMBUS_SMC_3_SDA	SMB_45S	SMB	SMBUS_SMC_3_SDA	40 42

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
CHGR_CSI	1TO1_DIFFPAIR		CHGR_CSI_P	56
	1TO1_DIFFPAIR		CHGR_CSI_N	56
CHGR_CSO	1TO1_DIFFPAIR		CHGR_CSO_P	56
	1TO1_DIFFPAIR		CHGR_CSO_N	56

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_50S	*	=1:1_DIFFPAIR	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR
AUDIODIFF	*	=1:1_DIFFPAIR	0.1 MM	0.1 MM	10 MM	0.1 MM	0.1 MM
THERM_45S_CPUVRISNS1	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	0.2 MM	0.2 MM
THERM_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
SENSE_1TO1_45S	*	=1:1_DIFFPAIR	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2X_DIELECTRIC	?
THERM	*	=2X_DIELECTRIC	?
AUDIO	*	=2X_DIELECTRIC	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
GND	PCIE_*	*	GND_P2MM
GND	SATA_*	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SB_POWER	SATA_*	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D	*			0.09 MM	100 MIL		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D	*			0.09 MM	10 MM		
	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
USB_85D	TOP			0.1 MM	500 MIL		
CPU_27P4S	BOTTOM			0.23 MM	100 MIL		
USB3_85D	TOP			0.1 MM	500 MIL		
USB3_85D	ISL10			0.075 MM			0.090 MM
DP_85D	ISL9			0.075 MM			0.090 MM
PCIE_85D	ISL10			0.075 MM			0.090 MM

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
1TO1_DIFFPAIR	*	1:1_DIFFPAIR

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_CPUDDR_N
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_P 46
	THERM_1TO1_45S	THERM	ISNS_CPU_DDR_R_N 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_P 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUTHMSNS_D2_N 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_P
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_LCD_PANEL_N
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_P 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	DDR3THMSNS_D1_N 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_P 47
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	GPUTHMSNS_D_N 47
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_P 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_N 45
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_P 45
	SENSE_1TO1_45S	SENSE	ISNS_1V35_MEM_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_N
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_P 46
	SENSE_1TO1_45S	SENSE	ISNS_AIRPORT_R_N 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_N 46 62
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_LCDBKLT_P 46 62
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_P 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_GPUFB_R_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_P 45 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	GPUFB_CS_N 45 71
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_P 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER5V_N 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_P 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_OTHER3V3_N 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_P 44
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_HS_COMPUTING_N 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_P 46 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	P1V05_GPU_CS_N 46 71
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_P 44
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_GPU_N 44
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_P 45
	SENSE_1TO1_45S	SENSE	CPUVR_ISNS_N 45
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_P 46
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_PP1V0_S0GPU_R_N 46
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_P 71 76
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05_GPU_PEX_IOVDD_SNS_N 71 76
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_P 45 58
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS1_N 45 58
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_P 45 58
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS2_N 45 58
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_P 45 58
SENSE_DIFFPAIR	THERM_45S_CPUVRISNS1	THERM	CPUVR_ISNS3_N 45 58
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_P 45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	CPUVR_ISUM_R_N 45
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_P 77
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS2_N 77
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_P 77
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GFXIMVP_ISNS1_N 77
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_P 47 74
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	GPU_TDIODE_N 47 74
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_P 76 77
SENSE_DIFFPAIR	40_OHM_SE	THERM	GPUVCORE_SENSE_N 76 77
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_N 45
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	ISNS_TBT_P 45
	AUDIODIFF	AUDIO	ISNS_TBT_R_N 45
	AUDIODIFF	AUDIO	ISNS_TBT_R_P 45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_P 45
	THERM_1TO1_45S	THERM	ISNS_SSD_N 45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	ISNS_SSD_R_P 45
	THERM_1TO1_45S	THERM	ISNS_SSD_R_N 45
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_CS_P 61
	THERM_1TO1_45S	THERM	P1V05S0_CS_N 61
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	P1V05S0_SENSE_P 61
	THERM_1TO1_45S	THERM	P1V05S0_SENSE_N 61
SENSE_DIFFPAIR	THERM_1TO1_45S	THERM	TBT_THERMD_P 47
	THERM_1TO1_45S	THERM	TBT_THERMD_N 47
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSI_R_P 56
	AUDIODIFF	AUDIO	CHGR_CSI_R_N 56
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	CHGR_CSO_R_P 56
	AUDIODIFF	AUDIO	CHGR_CSO_R_N 56
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_P
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_N
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_P 46
SENSE_DIFFPAIR	SENSE_1TO1_45S	SENSE	ISNS_S2_R_N 46

J15 Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_P 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RSUBIN_N 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_P 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LSUBIN_N 52
	AUDIODIFF	AUDIO	RSUBIN_P 52
	AUDIODIFF	AUDIO	RSUBIN_N 52
	AUDIODIFF	AUDIO	LSUBIN_P 52
	AUDIODIFF	AUDIO	LSUBIN_N 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_P 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_R_N 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_P 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO2_L_N 50 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_P 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_RIN_N 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_P 52
	AUDIODIFF	AUDIO	AUD_SPKRAMP_LIN_N 52
	AUDIODIFF	AUDIO	SPKRAMP_RIN_P 52
	AUDIODIFF	AUDIO	SPKRAMP_RIN_N 52
	AUDIODIFF	AUDIO	SPKRAMP_LIN_P 52
	AUDIODIFF	AUDIO	SPKRAMP_LIN_N 52
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_P 52 54 83
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SL_OUT_N 52 54 83
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_P 52 54 83
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	SPKRCONN_SR_OUT_N 52 54 83
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_P 52 54 83
	DIFFPAIR	AUDIO	SPKRCONN_L_OUT_N 52 54 83
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_P 52 54 83
	DIFFPAIR	AUDIO	SPKRCONN_R_OUT_N 52 54 83
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_P
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_R_N
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_P 50
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	CODEC_HS_MIC_N 50
AUDIO_DIFFPAIR	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_P
	DIFFPAIR	AUDIO	AUD_MIC_IN1_L_N
	DIFFPAIR	AUDIO	AUD_HS_MIC_P 53 54
	DIFFPAIR	AUDIO	AUD_HS_MIC_N 53 54
	DIFFPAIR	AUDIO	HS_MIC_P 50 53
	DIFFPAIR	AUDIO	HS_MIC_N 50 53
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_P
	DIFFPAIR	AUDIO	AUD_CONN_HS_MIC_N
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_P 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_R_N 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_P 50 52
AUDIO_DIFFPAIR	AUDIODIFF	AUDIO	AUD_LO3_L_N 50 52
		SB_POWER	PP3V3_S5 81 83
		SB_POWER	PP3V3_S0 81 83
		SB_POWER	PP1V35_S3RS0_CPUDDR 81
		GND	GND

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GDDR5 Frame Buffer Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
GDDR5_45R50SE	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	12.7 MM	=STANDARD	=STANDARD
GDDR5_45SE	*	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=45_OHM_SE_ADJ	=STANDARD	=STANDARD
GDDR5_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	*	=5x_DIELECTRIC	?
GDDR5_CMD	*	=3x_DIELECTRIC	?
GDDR5_DATA	*	=3x_DIELECTRIC	?
GDDR5_EDC	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GDDR5_CLK	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_CMD	TOP,BOTTOM	=4x_DIELECTRIC	?
GDDR5_DATA	TOP,BOTTOM	=5x_DIELECTRIC	?
GDDR5_EDC	TOP,BOTTOM	=5x_DIELECTRIC	?

GDDR5 FB A Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_P
FB_A0_CLK	GDDR5_80D	GDDR5_CLK	FB_A0_CLK_N
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_P
FB_A1_CLK	GDDR5_80D	GDDR5_CLK	FB_A1_CLK_N
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_A<8..0>
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_A<8..0>
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_ABI_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_ABI_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_RAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_RAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CAS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CAS_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_WE_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_WE_L
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_CKE_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_CKE_L
FB_A0_CMD	GDDR5_45SE	GDDR5_CMD	FB_A0_CS_L
FB_A1_CMD	GDDR5_45SE	GDDR5_CMD	FB_A1_CS_L
FB_A0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<0>
FB_A0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<1>
FB_A0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<2>
FB_A0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A0_EDC<3>
FB_A1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<0>
FB_A1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<1>
FB_A1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<2>
FB_A1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_A1_EDC<3>
FB_A0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<0>
FB_A0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<1>
FB_A0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<2>
FB_A0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A0_DBI_L<3>
FB_A1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<0>
FB_A1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<1>
FB_A1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<2>
FB_A1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_A1_DBI_L<3>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<0>
FB_A0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<0>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_P<1>
FB_A0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A0_WCLK_N<1>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<0>
FB_A1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<0>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_P<1>
FB_A1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_A1_WCLK_N<1>
FB_A0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<7..0>
FB_A0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<15..8>
FB_A0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<23..16>
FB_A0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A0_DQ<31..24>
FB_A1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<7..0>
FB_A1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<15..8>
FB_A1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<23..16>
FB_A1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_A1_DQ<31..24>
FB_A0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A0_RESET_L
FB_A1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_A1_RESET_L

GDDR5 FB B Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_P
FB_B0_CLK	GDDR5_80D	GDDR5_CLK	FB_B0_CLK_N
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_P
FB_B1_CLK	GDDR5_80D	GDDR5_CLK	FB_B1_CLK_N
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_A<8..0>
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_A<8..0>
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_ABI_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_ABI_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_RAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_RAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CAS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CAS_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_WE_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_WE_L
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_CKE_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_CKE_L
FB_B0_CMD	GDDR5_45SE	GDDR5_CMD	FB_B0_CS_L
FB_B1_CMD	GDDR5_45SE	GDDR5_CMD	FB_B1_CS_L
FB_B0_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<0>
FB_B0_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<1>
FB_B0_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<2>
FB_B0_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B0_EDC<3>
FB_B1_EDC0	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<0>
FB_B1_EDC1	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<1>
FB_B1_EDC2	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<2>
FB_B1_EDC3	GDDR5_45SE	GDDR5_EDC	FB_B1_EDC<3>
FB_B0_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<0>
FB_B0_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<1>
FB_B0_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<2>
FB_B0_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B0_DBI_L<3>
FB_B1_DBI_L0	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<0>
FB_B1_DBI_L1	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<1>
FB_B1_DBI_L2	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<2>
FB_B1_DBI_L3	GDDR5_45SE	GDDR5_DATA	FB_B1_DBI_L<3>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<0>
FB_B0_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<0>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_P<1>
FB_B0_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B0_WCLK_N<1>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<0>
FB_B1_WCLK0	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<0>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_P<1>
FB_B1_WCLK1	GDDR5_80D	GDDR5_CMD	FB_B1_WCLK_N<1>
FB_B0_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<7..0>
FB_B0_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<15..8>
FB_B0_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<23..16>
FB_B0_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B0_DQ<31..24>
FB_B1_DQ_BYTE0	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<7..0>
FB_B1_DQ_BYTE1	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<15..8>
FB_B1_DQ_BYTE2	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<23..16>
FB_B1_DQ_BYTE3	GDDR5_45SE	GDDR5_DATA	FB_B1_DQ<31..24>
FB_B0_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B0_RESET_L
FB_B1_CMD_R	GDDR5_45SE	GDDR5_CMD	FB_B1_RESET_L

MUXGFX & DP AUX MUX NET PROPERTIES

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_ML_F_N<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_P<3..0>
DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_P
DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUX_N
DP_INT_IG_AUX	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_IG_AUX_N
DP_INT_IG_ML	DP_85D	DISPLAYPORT	DP_INT_IG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_IG_ML_N<3..0>
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_P
	DP_85D	DISPLAYPORT	DP_INT_EG_AUX_N
DP_INT_EG_ML	DP_85D	DISPLAYPORT	DP_INT_EG_ML_P<3..0>
	DP_85D	DISPLAYPORT	DP_INT_EG_ML_N<3..0>
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_P
DP_INT_EG_AUX	DP_85D	DISPLAYPORT	DP_TBTSNK0_EG_AUXCH_N
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_P
DP_INT_EG_AUX1	DP_85D	DISPLAYPORT	DP_TBTSNK1_EG_AUXCH_N
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_P
TBTSNK0_AUXCH	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_N
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK0_AUXCH_C_N
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_P
TBTSNK1_AUXCH1	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_N
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_P
	DP_85D	DISPLAYPORT	DP_TBTSNK1_AUXCH_C_N
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_P<3..0>
DP_TBT_ML	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK0_ML_C_N<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_P<3..0>
DP_TBT_ML1	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_N<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_P<3..0>
	DP_85D	DISPLAYPORT	DP_TBTSNK1_ML_C_N<3..0>

Kepler Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING	
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALIN
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTALOUT
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_XTAL_BUFFOUT_R
GPU_CLK27M	CLK_SLOW_50S	CLK_SLOW	GPU_OSC_27M_SSIN
	1TO1_DIFFPAIR		PEX_TSTCLK_O_P
	1TO1_DIFFPAIR		PEX_TSTCLK_O_N
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_P<2..0>
HDMI_DATA	DP_85D	DISPLAYPORT	HDMI_EG_DATA_C_N<2..0>
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_P
HDMI_CLK	DP_85D	HDMI_CLK	HDMI_EG_CLK_C_N

SYNC_MASTER=SIDLE_J15 SYNC_DATE=09/02/2012

PAGE TITLE: GPU (Kepler) Constraints

Apple Inc.

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