

COMPAL CONFIDENTIAL

MODEL NAME : ZAM81  
PCB NO : LA-A913P  
BOM P/N :  
GPIO MAP: 3.1

Huston 15" DSC  
Broadwell U

2013-08-20  
REV : 0.1 (X00)

@ : Nopop Component  
EMC@ : EMI, ESD and RF Component  
@EMC@ : EMI, ESD and RF Nopop Component  
XDP@ : XDP Component  
CONN@ : Connector Component

| MB PCB      |                                     |
|-------------|-------------------------------------|
| Part Number | Description                         |
| DAA0887Y088 | PCB 13N LA-A913P REV0 MB DSC DOCK 3 |

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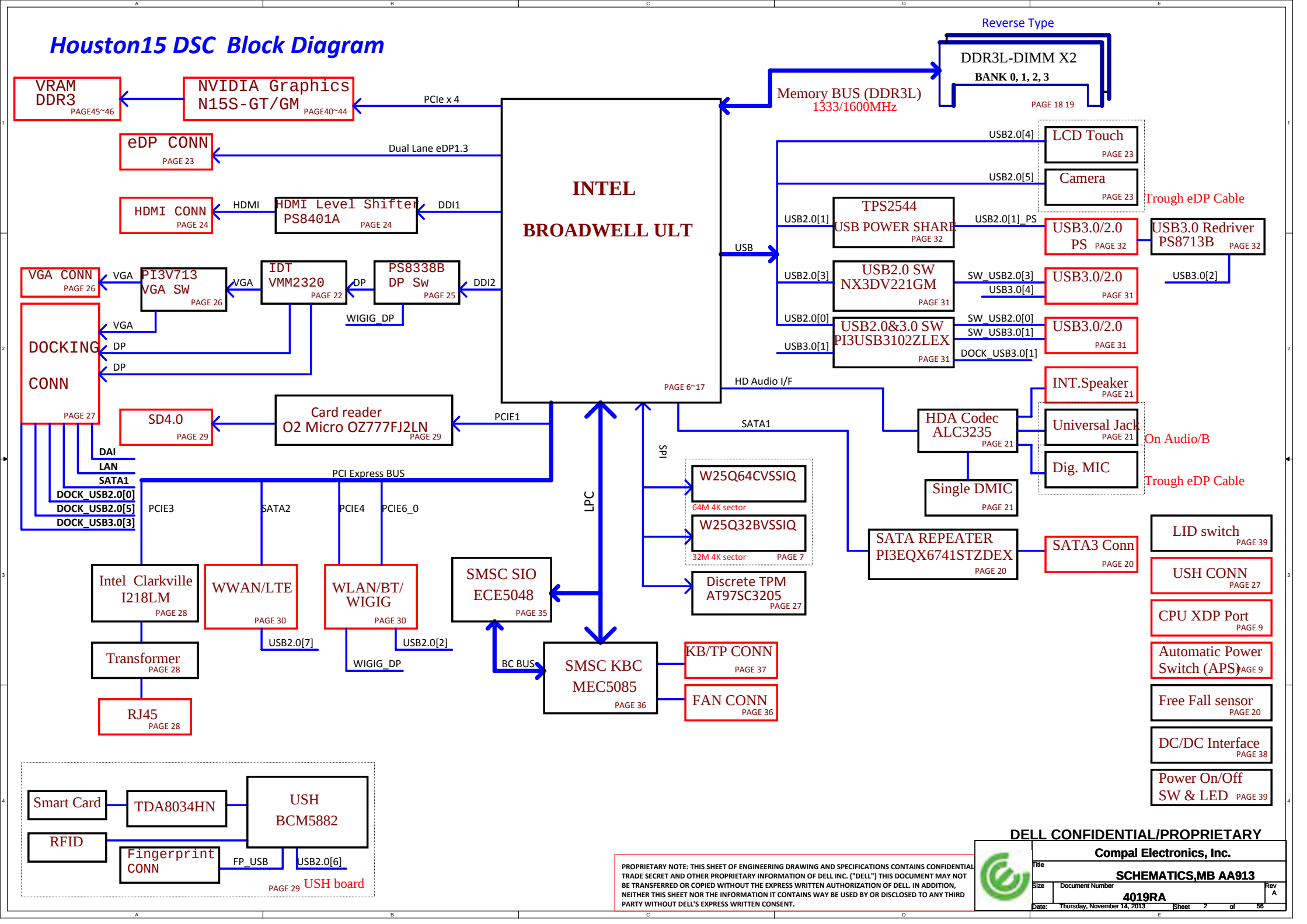
**4019RA**

Thursday, November 14, 2013

Rev **A**

Sheet 1 of 56

# Houston15 DSC Block Diagram



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Date: Thursday, November 14, 2013 Sheet 2 of 56

POWER STATES

| Signal<br>State              | SLP<br>S3# | SLP<br>S4# | SLP<br>S5# | SLP<br>A# | ALWAYS<br>PLANE | M<br>PLANE | SUS<br>PLANE | RUN<br>PLANE | CLOCKS |
|------------------------------|------------|------------|------------|-----------|-----------------|------------|--------------|--------------|--------|
| S0 (Full ON) / M0            | HIGH       | HIGH       | HIGH       | HIGH      | ON              | ON         | ON           | ON           | ON     |
| S3 (Suspend to RAM) / M3     | LOW        | HIGH       | HIGH       | HIGH      | ON              | ON         | ON           | OFF          | OFF    |
| S4 (Suspend to DISK) / M3    | LOW        | LOW        | HIGH       | HIGH      | ON              | ON         | OFF          | OFF          | OFF    |
| S5 (SOFT OFF) / M3           | LOW        | LOW        | LOW        | HIGH      | ON              | ON         | OFF          | OFF          | OFF    |
| S3 (Suspend to RAM) / M-OFF  | LOW        | HIGH       | HIGH       | LOW       | ON              | OFF        | ON           | OFF          | OFF    |
| S4 (Suspend to DISK) / M-OFF | LOW        | LOW        | HIGH       | LOW       | ON              | OFF        | OFF          | OFF          | OFF    |
| S5 (SOFT OFF) / M-OFF        | LOW        | LOW        | LOW        | LOW       | ON              | OFF        | OFF          | OFF          | OFF    |

PM TABLE

| power<br>plane<br>State | +5V_ALW<br>+3.3V_ALW<br>+3.3V_ALW_PCH<br>+3.3V_RTC_LDO | +3.3V_SUS<br>+1.35V_MEM | +5V_RUN<br>+3.3V_RUN<br>+0.675V_DDR_VTT<br>+1.05V_RUN<br>+VCC_CORE | +3.3V_M<br>+1.05V_M | +3.3V_M<br>+1.05V_M<br>(M-OFF) |
|-------------------------|--------------------------------------------------------|-------------------------|--------------------------------------------------------------------|---------------------|--------------------------------|
| S0                      | ON                                                     | ON                      | ON                                                                 | ON                  | ON                             |
| S3                      | ON                                                     | ON                      | OFF                                                                | ON                  | OFF                            |
| S5 S4/AC                | ON                                                     | OFF                     | OFF                                                                | ON                  | OFF                            |
| S5 S4/AC doesn't exist  | OFF                                                    | OFF                     | OFF                                                                | OFF                 | OFF                            |

need to update Power Status and  
PM Table

| PCIE   | USB3.0   | SATA   | DESTINATION        |
|--------|----------|--------|--------------------|
|        | USB3.0 1 |        | JUSB1-->Rear left  |
|        | USB3.0 2 |        | JUSB3-->Right      |
| PCIE 1 | USB3.0 3 |        | MMI (CARD READER)  |
| PCIE 2 | USB3.0 4 |        | JUSB2-->Rear Right |
| PCIE 3 |          |        | LOM                |
| PCIE 4 |          |        | WLAN               |
| PCIE 5 |          |        | GPU/WIGIG          |
| PCIE 6 |          | SATA 3 | WIGI/Express       |
|        |          | SATA 2 | mSATA/PCIE         |
|        |          | SATA 1 | HDD                |
|        |          | SATA 0 | DOCK               |

| BDW<br>ULT | USB PORT# | DESTINATION  |
|------------|-----------|--------------|
|            | 0         | JUSB1        |
|            | 1         | JUSB3        |
|            | 2         | WLAN + BT    |
|            | 3         | JUSB2        |
|            | 4         | Touch Screen |
|            | 5         | CAMERA       |
|            | 6         | USH          |
|            | 7         | WWAN         |

| USH | 0 | BIO |
|-----|---|-----|
|     | 1 | NA  |

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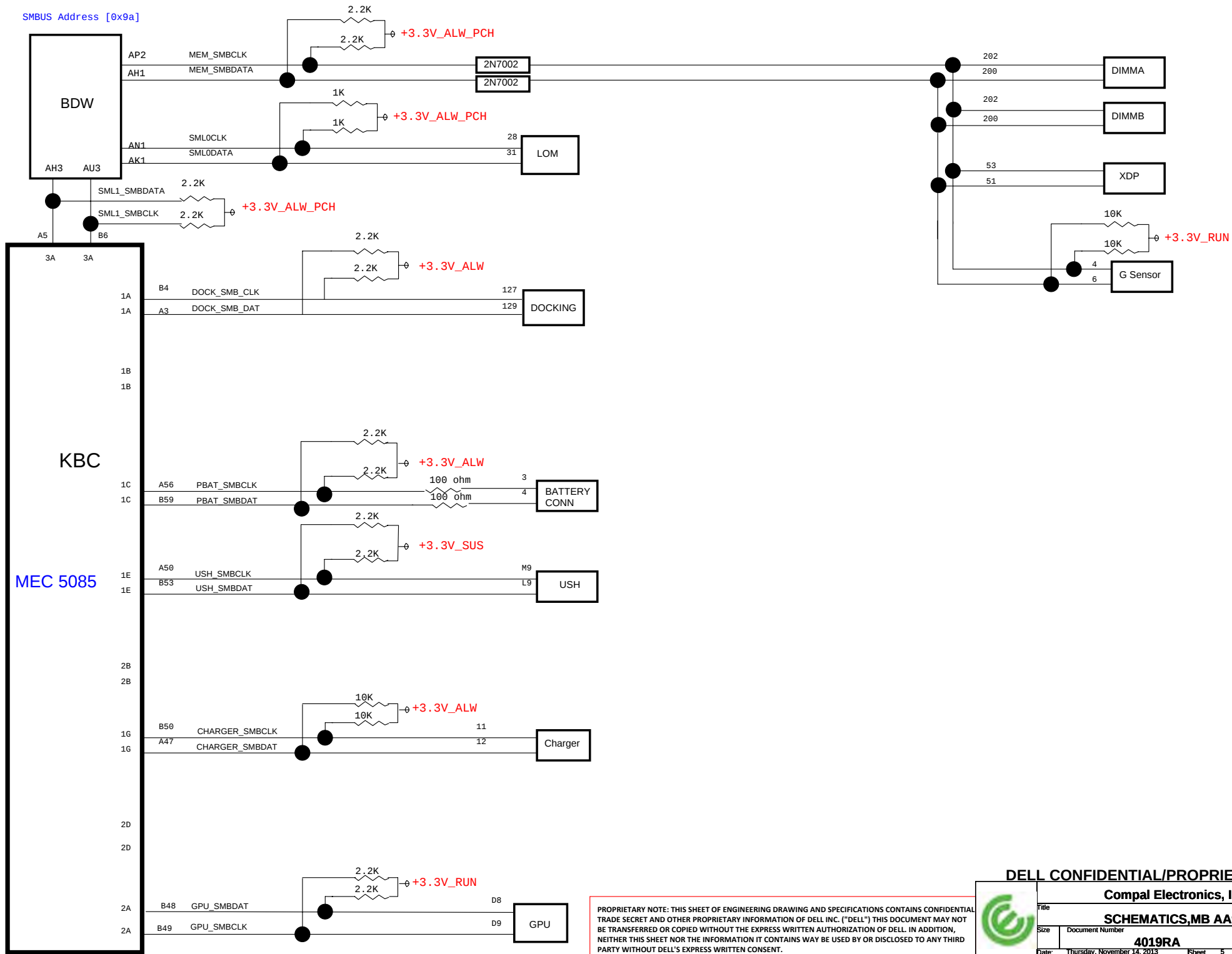


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| Date: | Thursday, November 14, 2013 | Sheet 3             | of 56 |

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SMBUS Address [0x9a]



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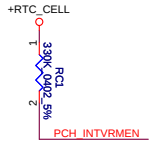
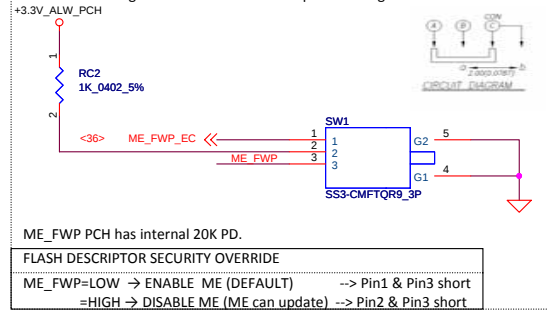
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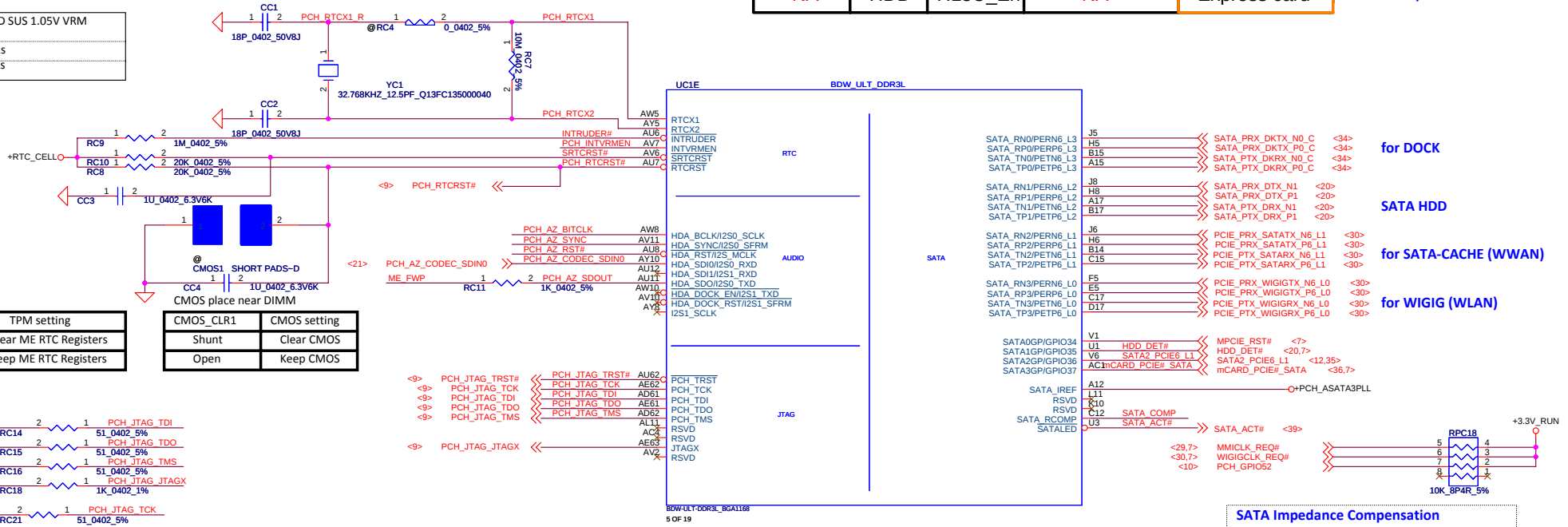
Sheet 5 of 56

## DSC SATA port

Service Mode Switch:  
Add a switch to ME\_FWP signal to unlock the ME region and allow the entire region of the SPI flash to be updated using FPT.

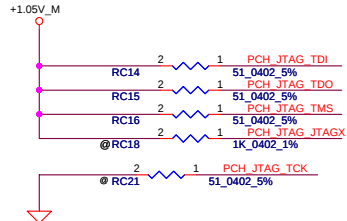


|                                                                                                                        |
|------------------------------------------------------------------------------------------------------------------------|
| <b>INTVRMEN - INTEGRATED SUS 1.05V VRM</b><br><b>ENABLE</b><br>High - Enable Internal VRs<br>Low - Enable External VRs |
|------------------------------------------------------------------------------------------------------------------------|

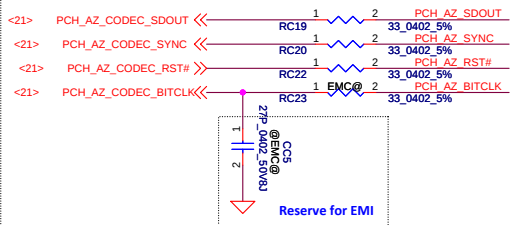


|         |                        |
|---------|------------------------|
| ME_CLR1 | TPM setting            |
| Shunt   | Clear ME RTC Registers |
| Open    | Keep ME RTC Registers  |

|           |              |
|-----------|--------------|
| CMOS_CLR1 | CMOS setting |
| Shunt     | Clear CMOS   |
| Open      | Keep CMOS    |



## HDA for Codec



| SATA0  | SATA1 | PCB       | SATA2/PCIE6 L1                          | SATA3/PCIE6 L0                |
|--------|-------|-----------|-----------------------------------------|-------------------------------|
| E-Dock | HDD   | H12 UMA   | M2 3042<br>2nd PCIe Lane for PCIe Cache | M2 3042<br>(HCA & SATA-Cache) |
| NA     | HDD   | H12 Entry | NA                                      | NA                            |
| E-Dock | HDD   | H14 DSC   | M2 3042<br>SATA-Cache(no HCA)           | M2 3030 WIGIG                 |
| E-Dock | HDD   | H14 UMA   | M2 3042<br>2nd PCIe Lane for PCIe Cache | M2 3042<br>(HCA & SATA-Cache) |
| NA     | HDD   | H14D_En   | NA                                      | M2 3030 WIGIG                 |
| NA     | HDD   | H14U_En   | NA                                      | NA                            |
| E-Dock | HDD   | H15 DSC   | M2 3042<br>SATA-Cache(no HCA)           | M2 3030 WIGIG                 |
| E-Dock | HDD   | H15 UMA   | M2 3042<br>2nd PCIe Lane for PCIe Cache | M2 3042<br>(HCA & SATA-Cache) |
| NA     | HDD   | H15D_En   | NA                                      | M2 3030 WIGIG                 |
| NA     | HDD   | H15U_En   | NA                                      | Express card                  |

contact to WWAN

SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6\_L0 contact to WLAN

contact to WWAN

**contact to WLAN**

SATA2/PCIE6\_L1 contact to WWAN  
SATA3/PCIE6 L0 contact to WLAN

contact to WWAN

## contact to WLAN

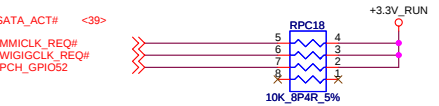
contact to Express card

for DOCK

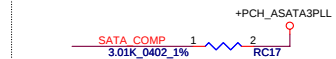
**SATA HDD**

for SATA-CACHE (WWAN)

for WIGIG (WLAN)



## SATA Impedance Compensation



**CAD note:**  
Place the resistor within 500 mils of the PCH. Avoid routing next to clock pins.

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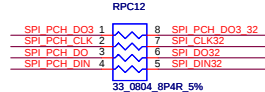
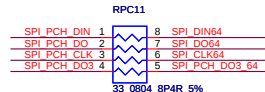
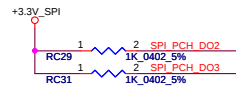
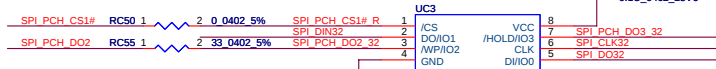
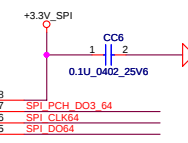
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| Sheet | 6 of 56                     |

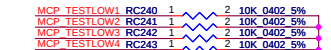
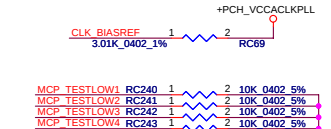
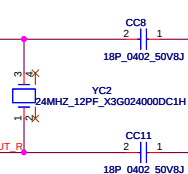
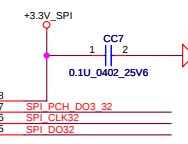
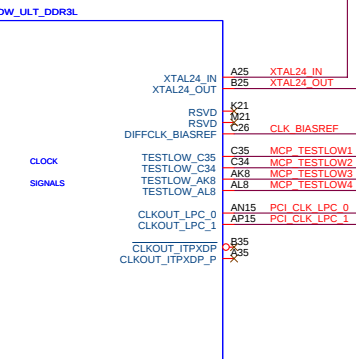
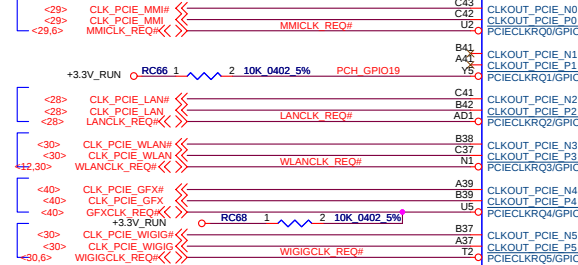
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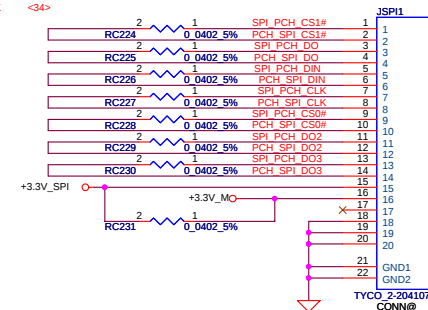
64Mb Flash ROM



|      |              |
|------|--------------|
| UC1F | BDW_ULT_DDR3 |
|------|--------------|



PCI\_CLK\_LPC → EMC@ RC72 1 2 2 0402 5% → CLK\_PCI\_SIO <35>  
EMC@ RC74 1 2 2 0402 5% → CLK\_PCI\_MEC <36>  
PCI\_CLK\_LPC → EMC@ RC67 1 2 2 0402 5% → CLK\_PCI\_LPDEBUG <36>  
EMC@ RC70 1 2 2 0402 5% → CLK\_PCI\_DOCK <34>



|            |               |
|------------|---------------|
| LPC_0      | LPC_1         |
| SIO<br>MEC | DOCK<br>DEBUG |

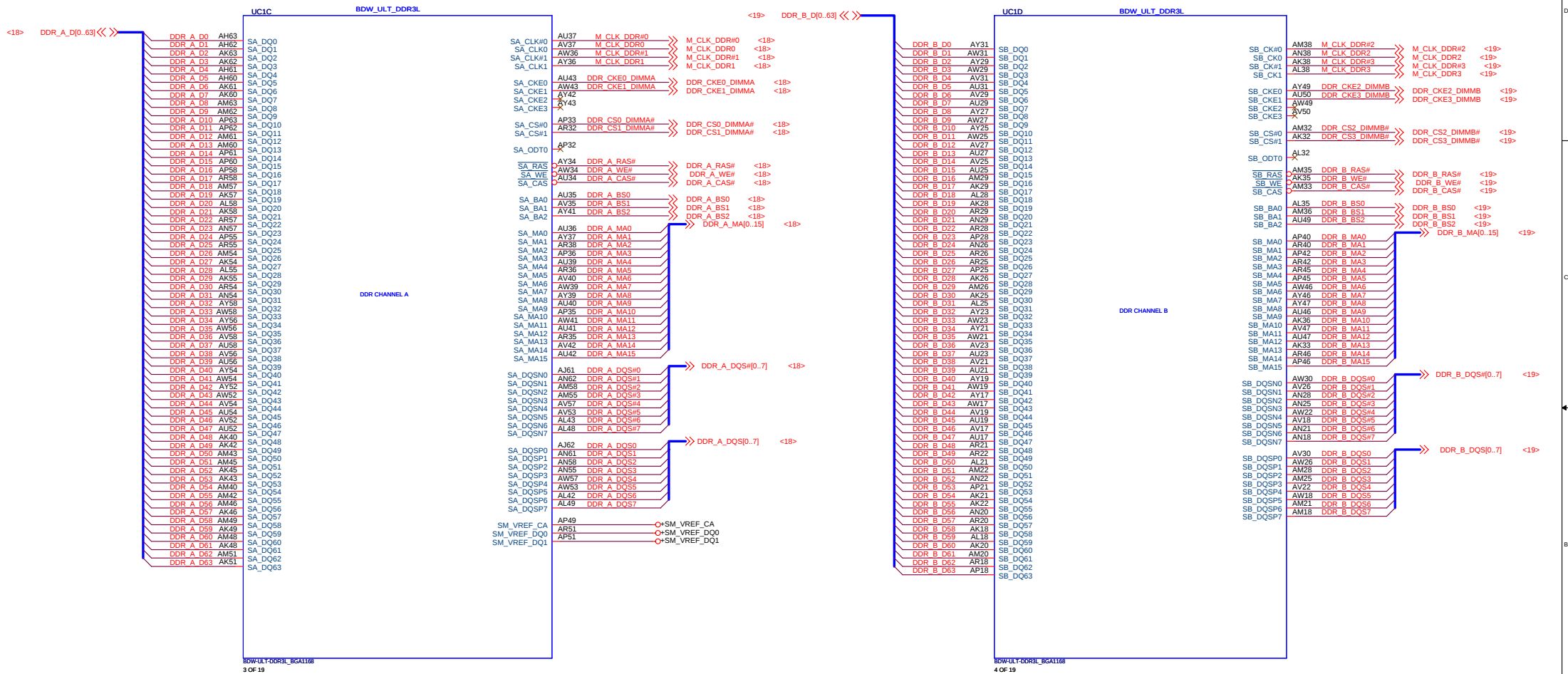
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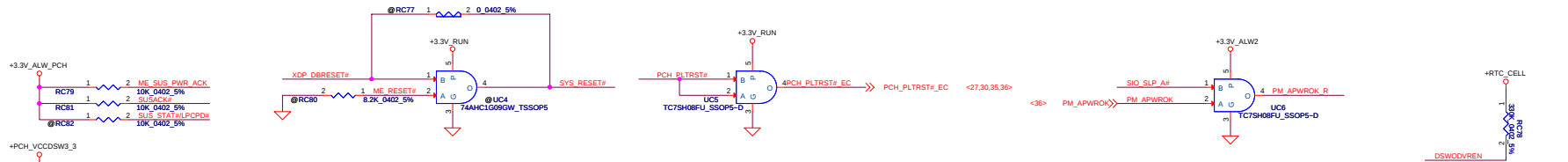


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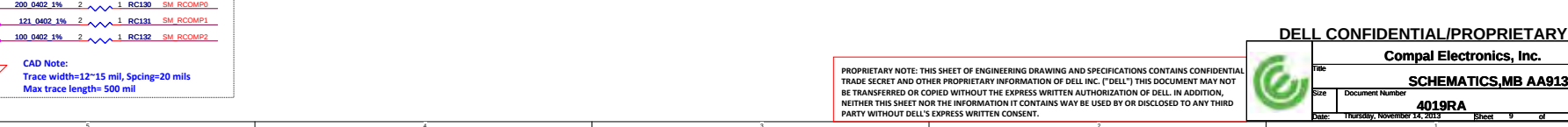
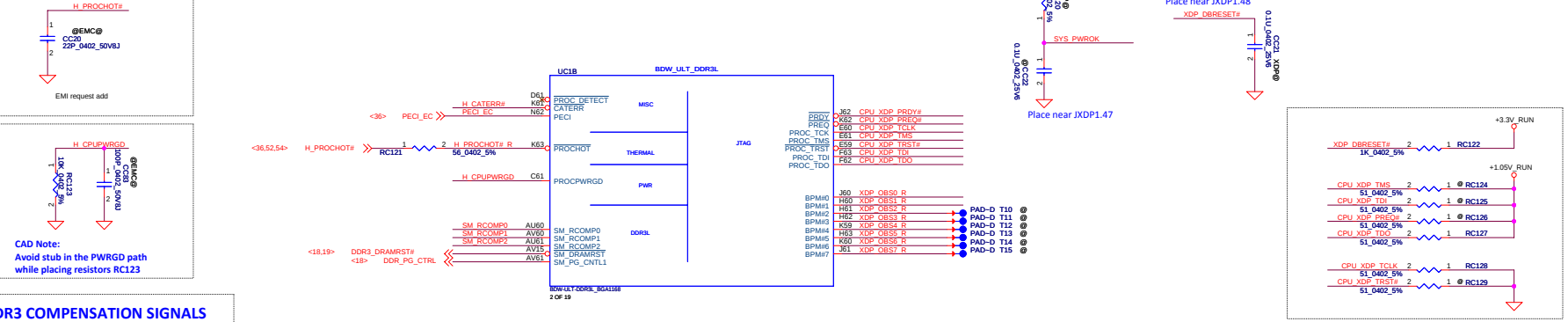
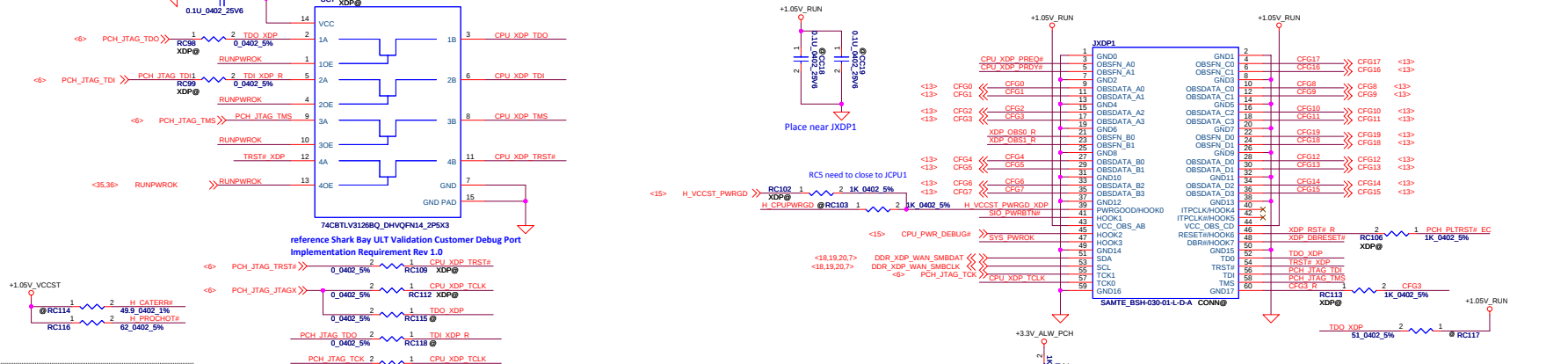
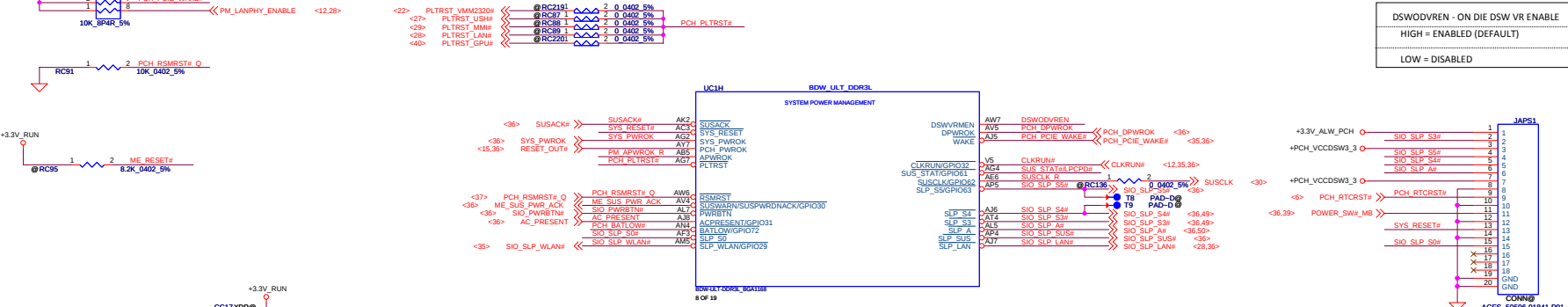
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| Date: | Thursday, November 14, 2013 | Sheet 8             | of 56 |

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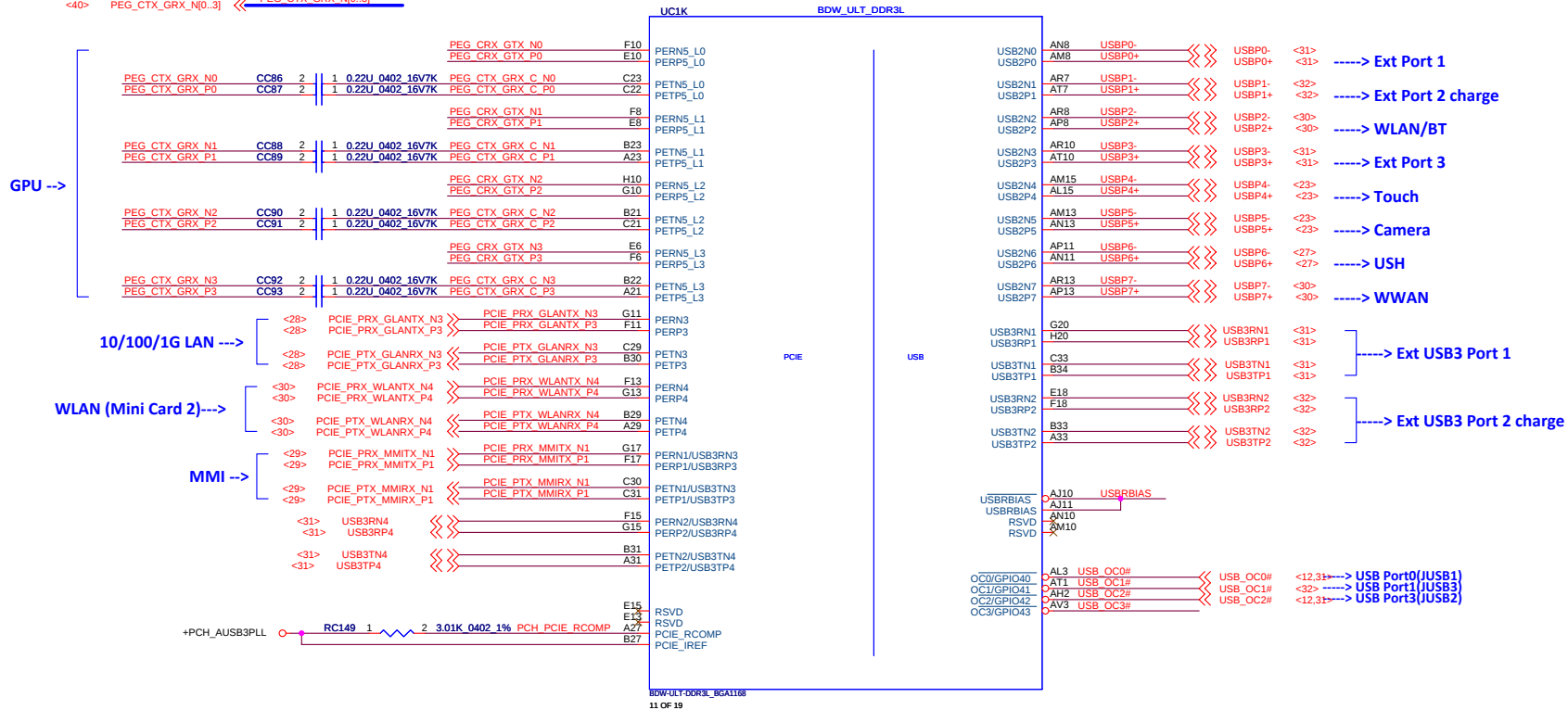
DSWOODREN - ON THE DSW VR ENABLE  
HIGH = ENABLED (DEFAULT)  
LOW = DISABLED





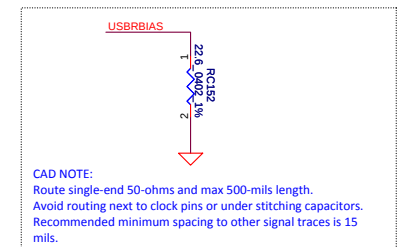
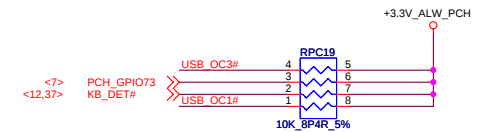
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<40> PEG\_CTX\_GRX\_N[0..3] << PEG\_CTX\_GRX\_N[0..3]

## PCIe for DSC



| PCB       | USB2    | 7 |
|-----------|---------|---|
| H12 UMA   | WWAN    |   |
| H12 Entry | NA      |   |
| H14 DSC   | WWAN    |   |
| H14 UMA   | WWAN    |   |
| H14D_En   | NA      |   |
| H14U_En   | NA      |   |
| H15 DSC   | WWAN    |   |
| H15 UMA   | WWAN    |   |
| H15D_En   | NA      |   |
| H15U_En   | Express |   |

| PCB       | PCIE1   | PCIE2 | PCIE3 | PCIE4 | PCIE5 | PCIE6                         |
|-----------|---------|-------|-------|-------|-------|-------------------------------|
| H12 UMA   | SD card | NA    | LOM   | WLAN  | WIGIG | M2 3042<br>(HCA & SATA-Cache) |
| H12 Entry | SD card | NA    | LOM   | WLAN  | WIGIG | NA                            |
| H14 DSC   | SD card | NA    | LOM   | WLAN  | GPU   | WIGIG                         |
| H14 UMA   | SD card | NA    | LOM   | WLAN  | WIGIG | M2 3042<br>(HCA & SATA-Cache) |
| H14D_En   | SD card | NA    | LOM   | WLAN  | GPU   | WIGIG                         |
| H14U_En   | SD card | NA    | LOM   | WLAN  | WIGIG | NA                            |
| H15 DSC   | SD card | NA    | LOM   | WLAN  | GPU   | WIGIG                         |
| H15 UMA   | SD card | NA    | LOM   | WLAN  | WIGIG | M2 3042<br>(HCA & SATA-Cache) |
| H15D_En   | SD card | NA    | LOM   | WLAN  | GPU   | WIGIG                         |
| H15U_En   | SD card | NA    | LOM   | WLAN  | WIGIG | Express card                  |



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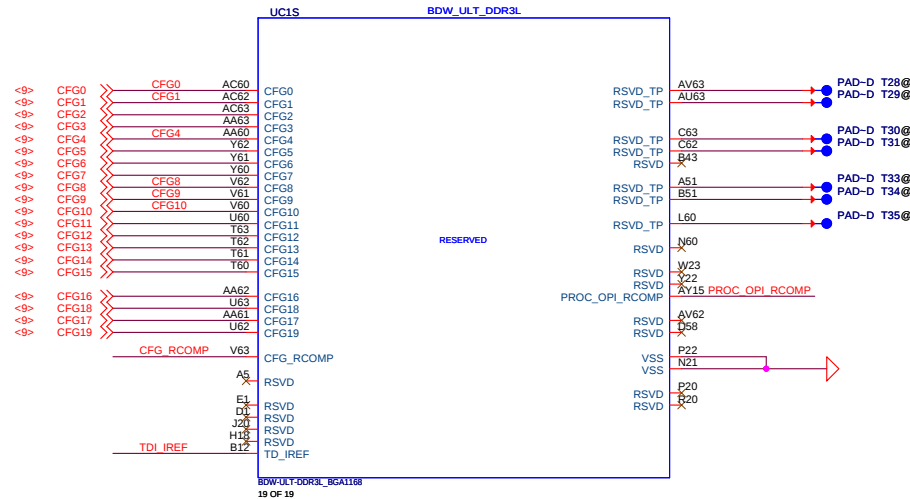


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| Date                     | Thursday, November 14, 2013 | Sheet  | 11 of 56 |

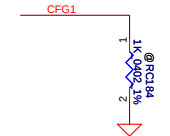
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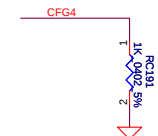
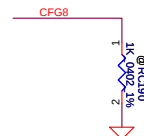
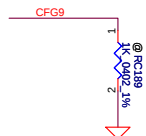
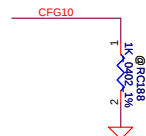
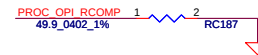
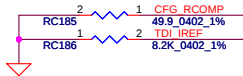
## CFG STRAPS for CPU



| EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKE |                                                           |
|-----------------------------------------------------------|-----------------------------------------------------------|
| CFG0                                                      | 1:(Default) Normal Operation; No stall<br>0:Lane Reversed |



| PCH/PCH LESS MODE SELECTION |                                                 |
|-----------------------------|-------------------------------------------------|
| CFG1                        | 1:(Default) Normal Operation<br>0:Lane Reversed |



| SAFE MODE BOOT |                                                                                                          |
|----------------|----------------------------------------------------------------------------------------------------------|
| CFG10          | 1: POWER FEATURES ACTIVATED DURING RESET<br>0: POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED |

| NO SVID PROTOCOL CAPABLE VR CONNECTED |                                                                                                                                        |
|---------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------|
| CFG9                                  | 1: VRS support SVID protocol are present<br>0:No VR support SVID is present<br>The chip will not generate(OR Respond to) SVID activity |

| ALLOW THE USE OF NOA ON LOCKED UNITS |                                                                                                                                                                 |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG8                                 | 1: Enable(Default): Noa will be disable in locked units and enable in un-locked units<br>0:Disable Noa will be available pegrardless of the locking of the unit |

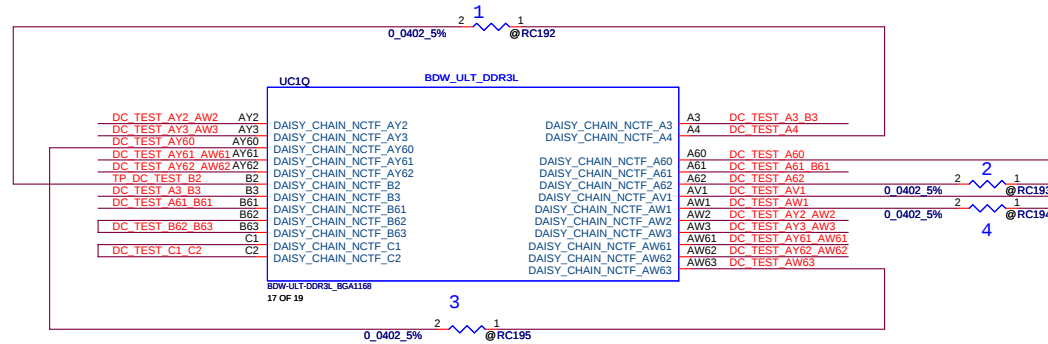
| Display Port Presence Strap |                                                                                                                                                                    |
|-----------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CFG4                        | 1 : Disabled; No Physical Display Port attached to Embedded Display Port<br>0 : Enabled; An external Display Port device is connected to the Embedded Display Port |

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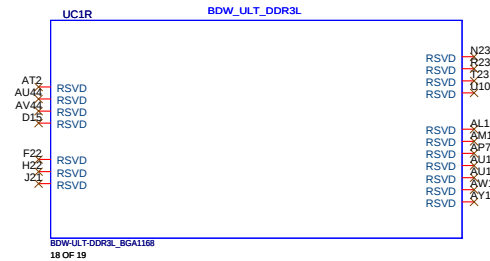
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| Sheet                    | 13 of 56                    |
| Rev                      | A                           |



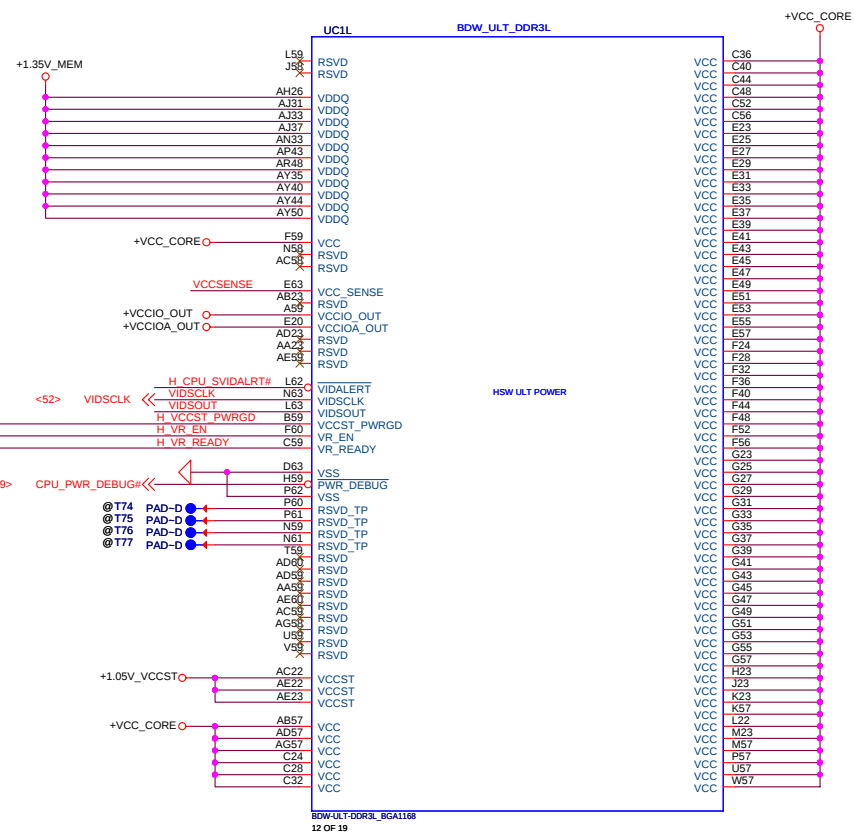
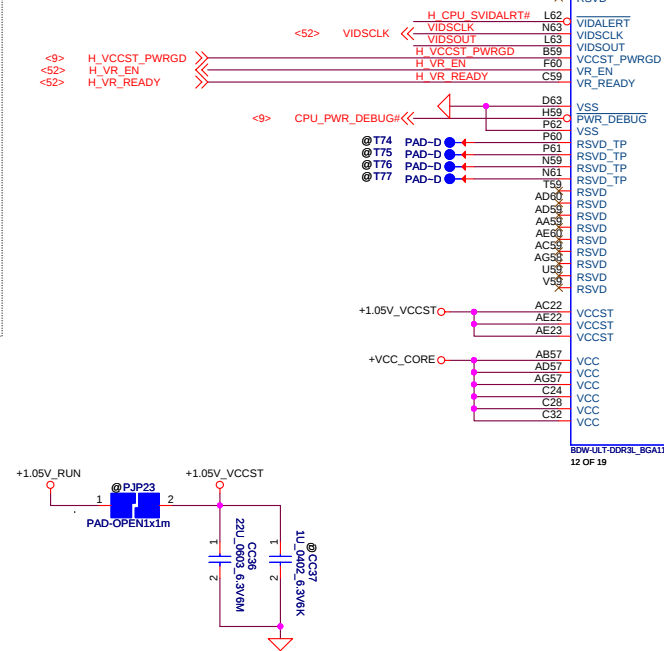
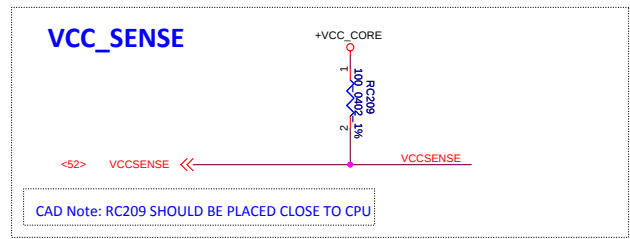
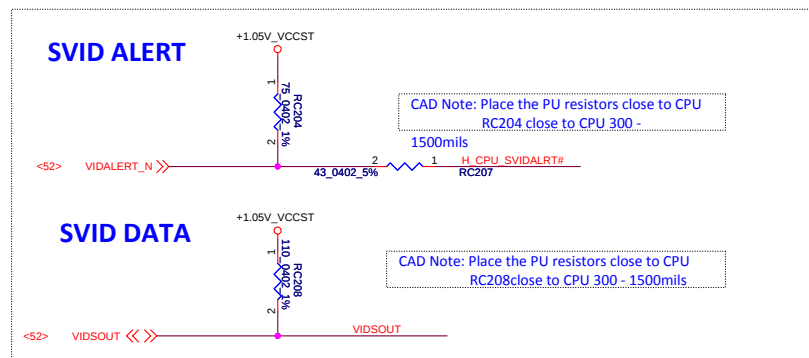
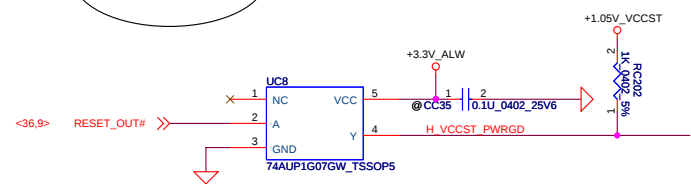
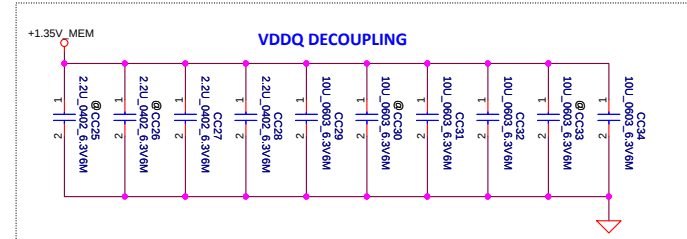
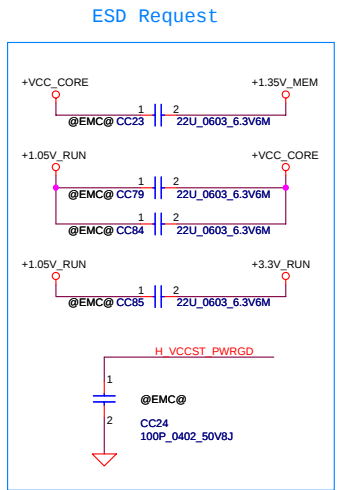
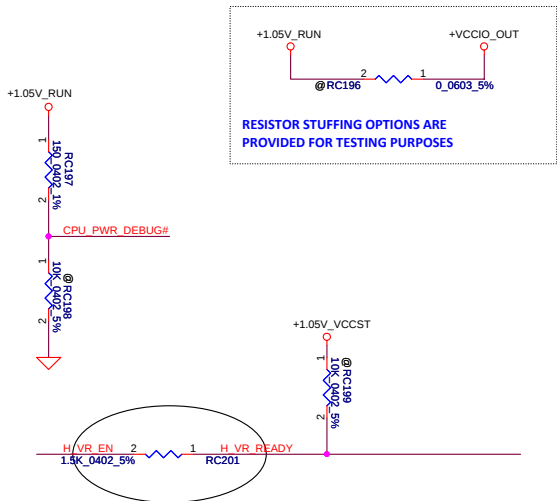
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- 1.B2-PKG-C1-PCB-C2-PKG-B3-PCB-A3-PKG-A4
- 2.A62-PKG-A61-PCB-B61-PKG-B62-PCB-B63-PKG-A60
- 3.AY60-PKG-AW61-PCB-AY61-PKG-AW62-PCB-AY62-PKG-AW63
- 4.AW1-PKG-AW3-PCB-AY3-PKG-AW2-PCB-AY2-PKG-AV1



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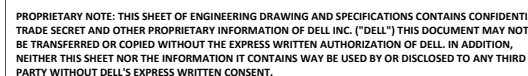
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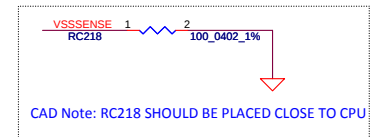
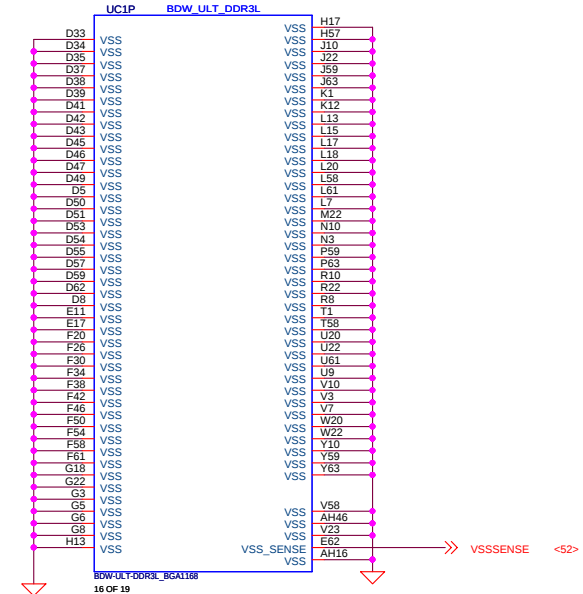
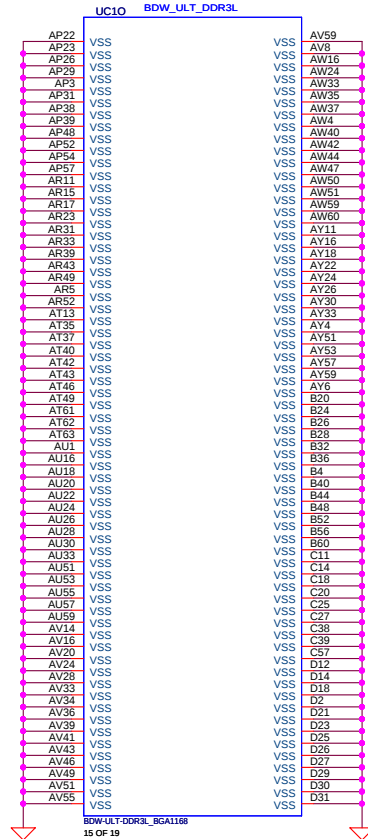
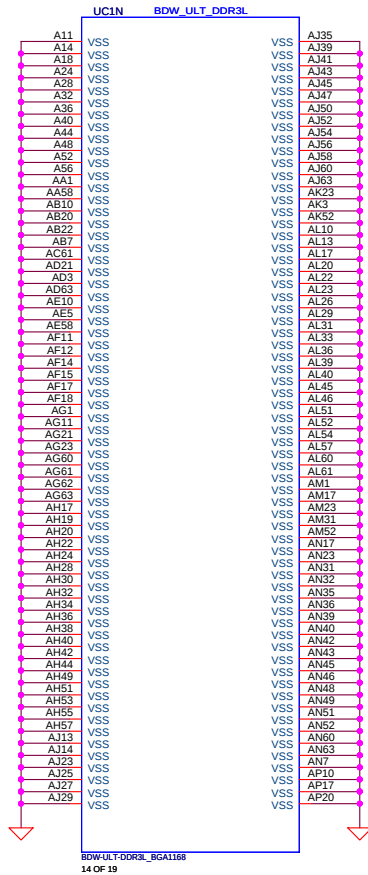
Size: **4019RA**

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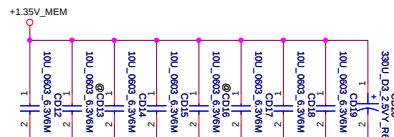
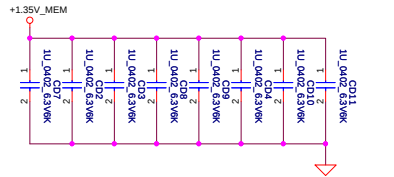


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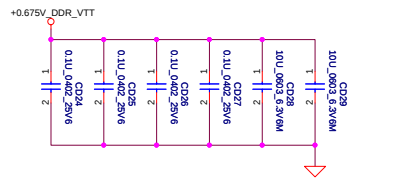
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| Size                          | Document Number             | 4019RA   | Rev A |
| Date:                         | Thursday, November 14, 2013 | Sheet 17 | of 56 |

<B> DDR\_A\_DQS#0..7 <<>>  
 <B> DDR\_A\_DQ0..63 <<>>  
 <B> DDR\_A\_DQS#0..7 <<>>  
 <B> DDR\_A\_MA0..15 <<>>

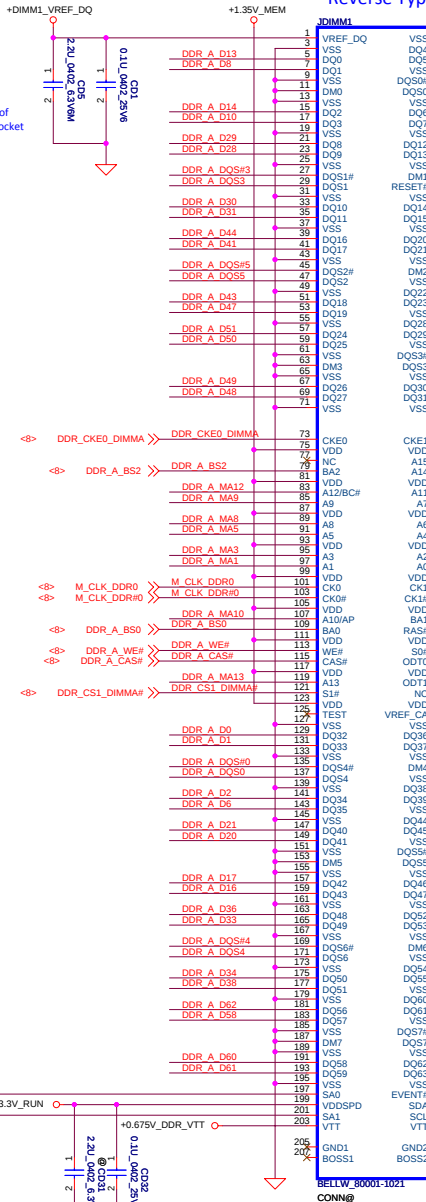
Layout Note:  
Place near JDIMM1



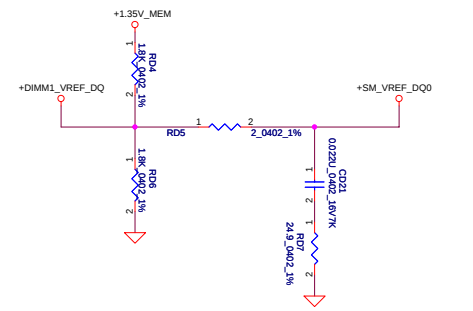
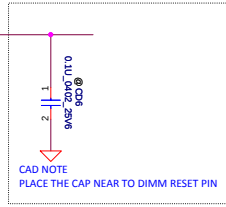
Layout Note:  
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JDIMM1.203,204



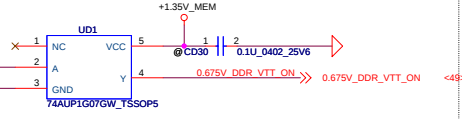
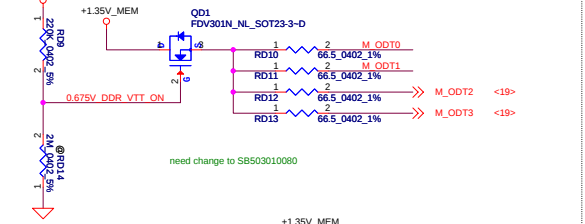
Note:  
Check voltage tolerance of  
VREF\_DQ at the DIMM socket



SP07000P700 LI NK DONE



### DDR3L SODIMM ODT GENERATION



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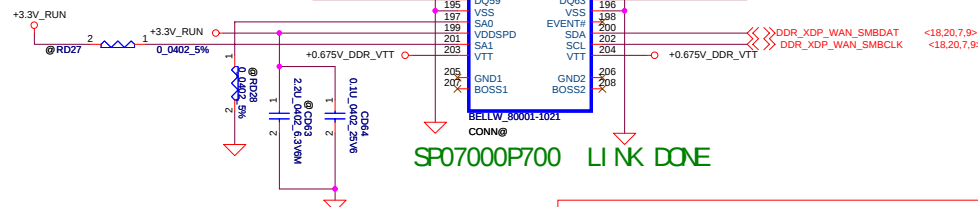
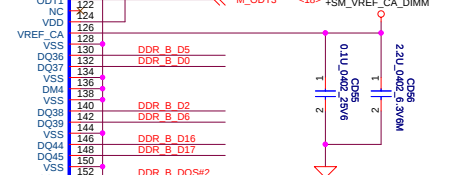
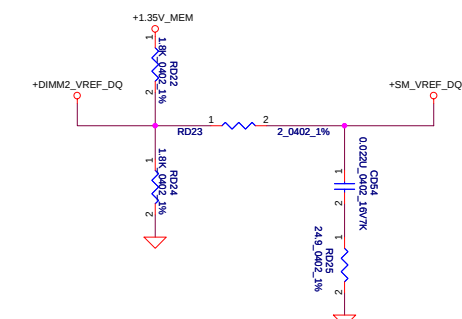
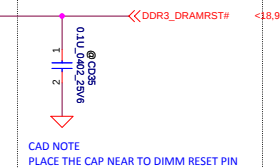
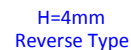
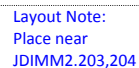
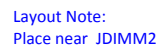
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Thursday, November 14, 2013 Sheet 18 of 56

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SP07000P700 LINK DONE

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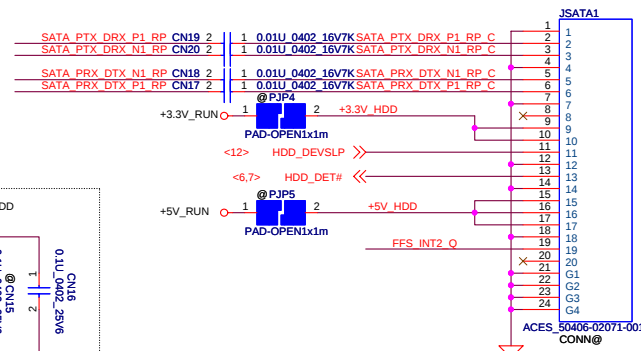
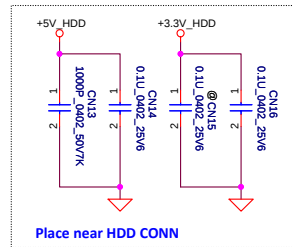
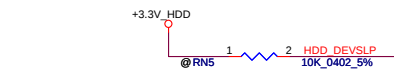
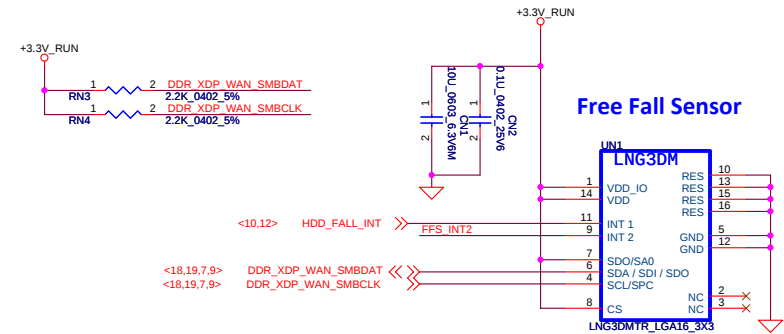
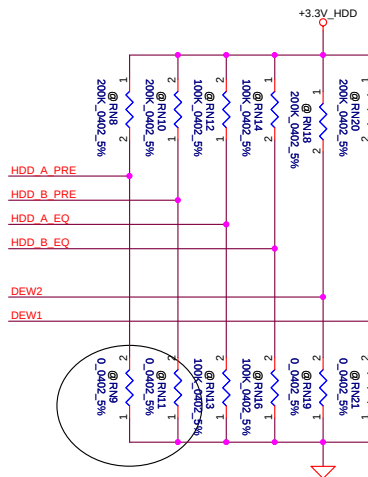
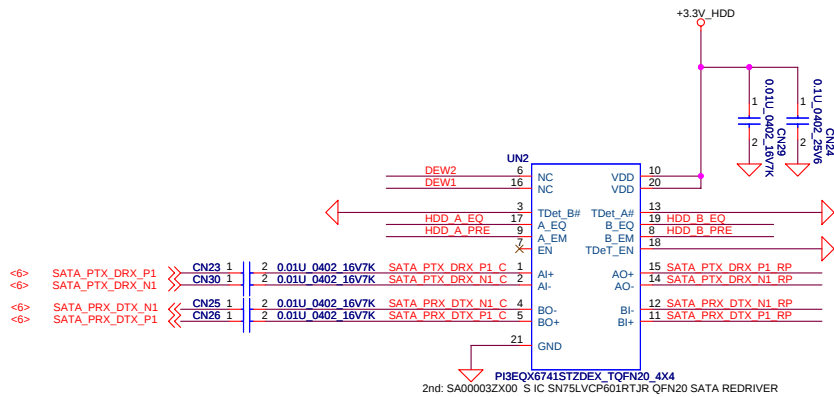
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Date: Thursday, November 14, 2013 Sheet 19 of 56

# SATA Repeater



SP010016L00 LI NK DONE

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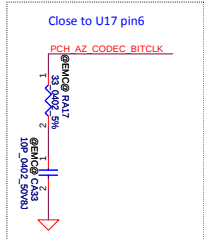
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| Sheet                    | 20 of 56                    |
| Rev                      | A                           |

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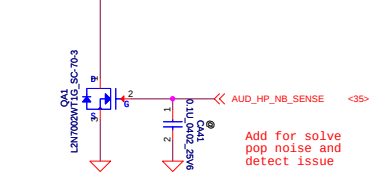
1W x 1ch, 4ohm (Transducer spec is 8Ohm/0.5Watt per unit, there are two transducer units in one speaker box.)

40 mils trace keep 20 mil spacing

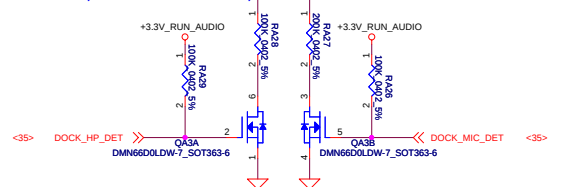
40 mils trace keep 20 mil spacing



Place closely to Pin 13.

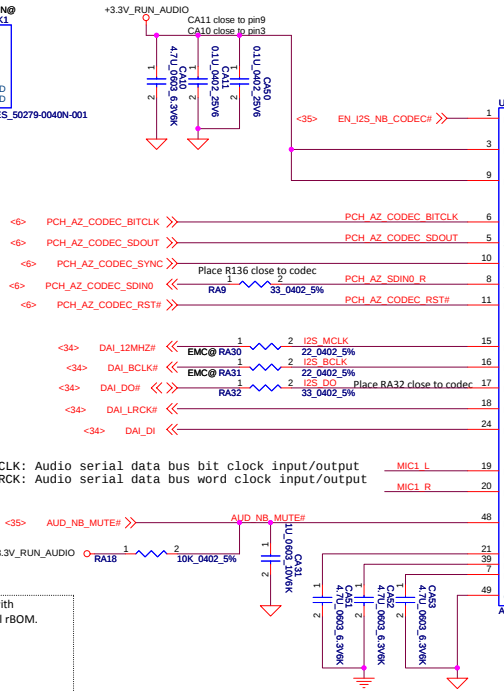


AUD\_SEM  
OCK only

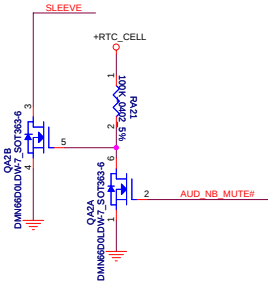
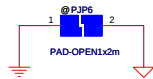
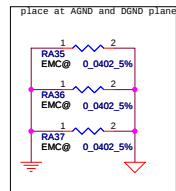


The schematic diagram shows the MIC1 module with the following connections:

- Pin 1: GND
- Pin 2: VCC
- Pin 3: GND
- Pin 4: DMIC1 CLK1
- Pin 5: DMIC1
- Pin 6: +3.3V\_RUN



<35> AUD\_NB\_MUTE#



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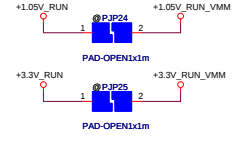
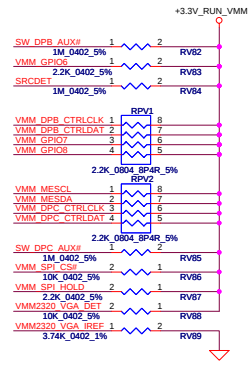
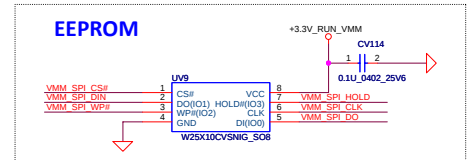
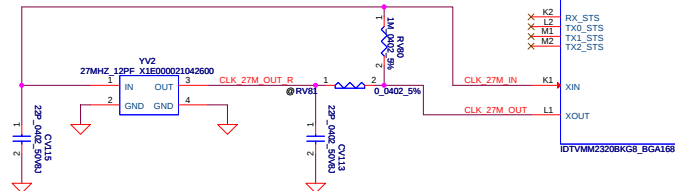
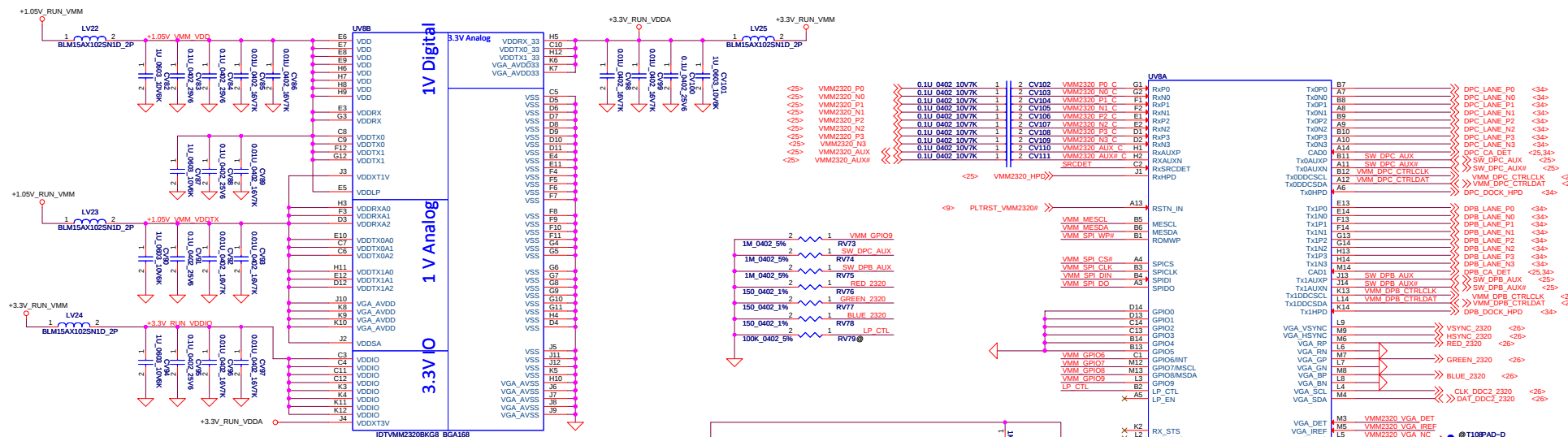


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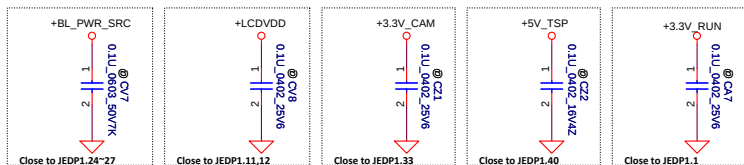
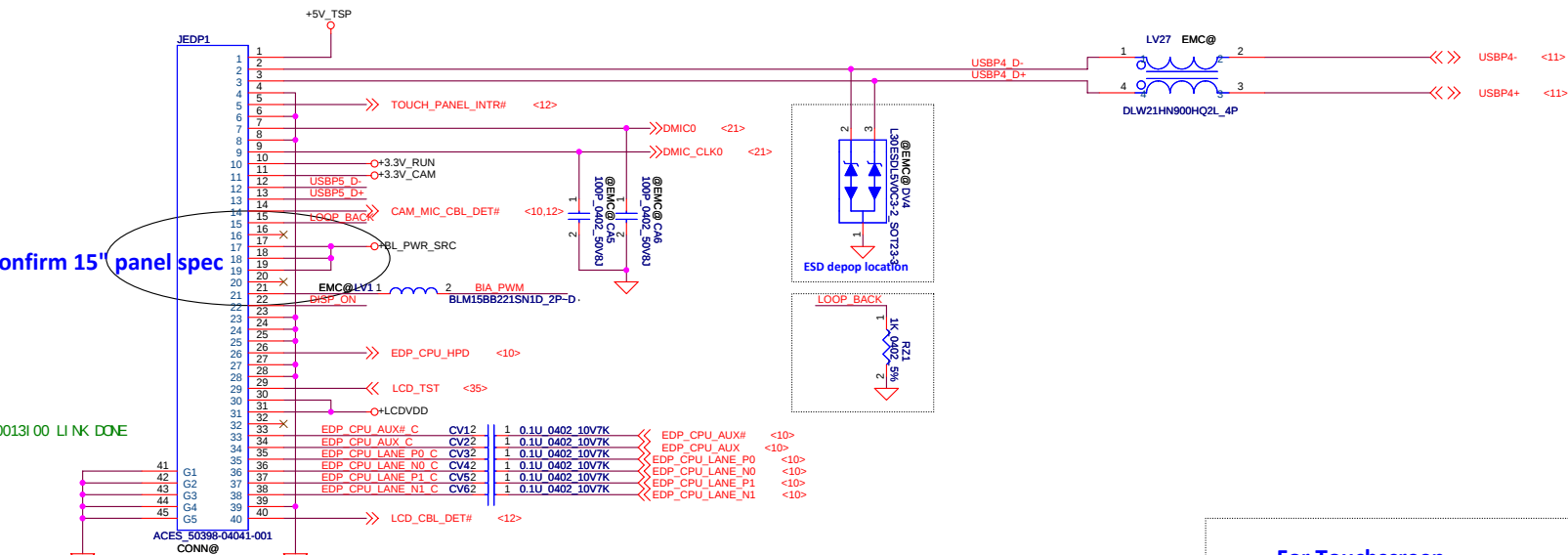
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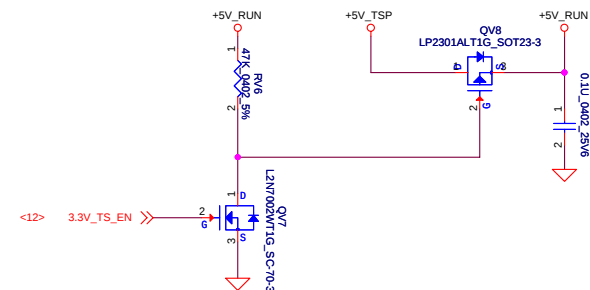
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| Date | Thursday, November 14, 2013 | Sheet  | 22 of 56 |

confirm 15" panel spec

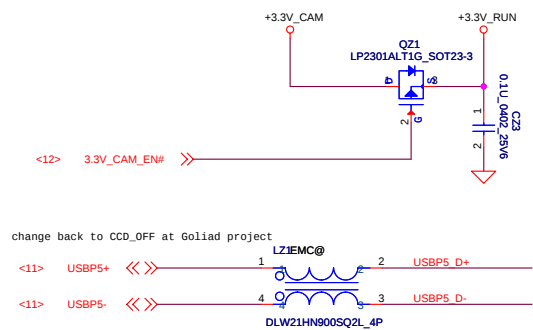
SP010013100 LINK DONE



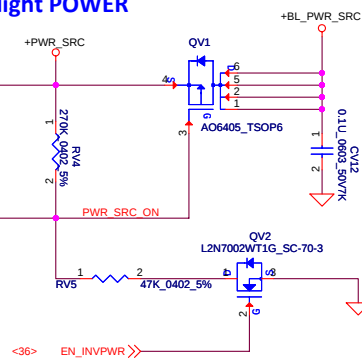
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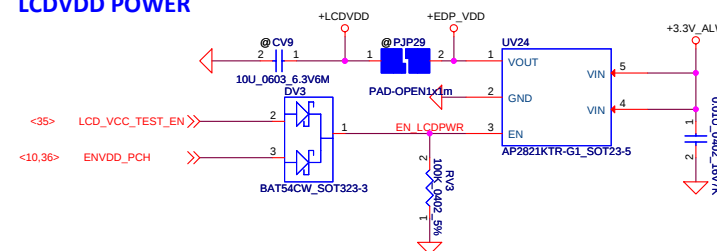
### WebCAM



### Backlight POWER



### LCDVDD POWER



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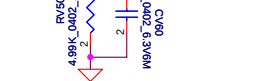
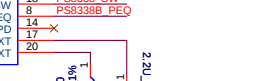
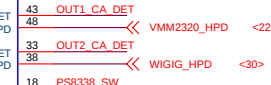
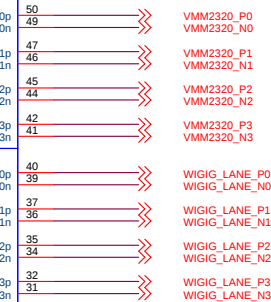
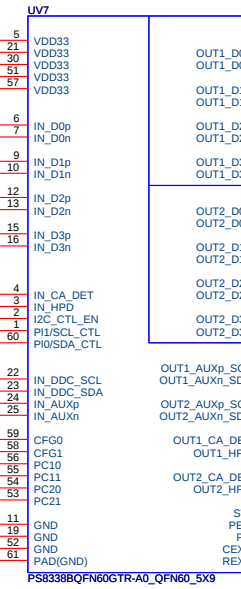
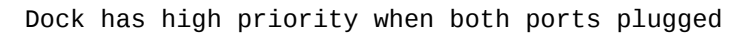
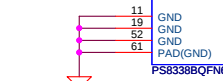
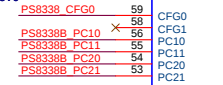
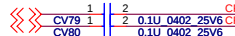
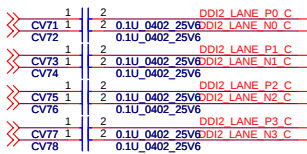
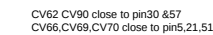
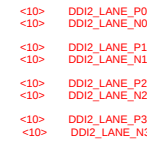
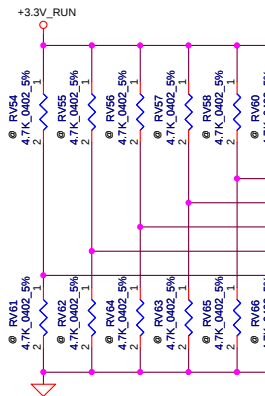
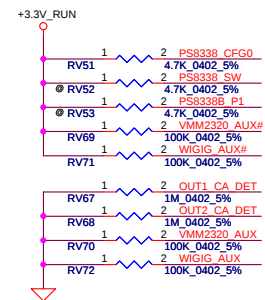
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| Date: Thursday, November 14, 2013 | Sheet 23 of 56  |       |

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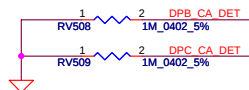
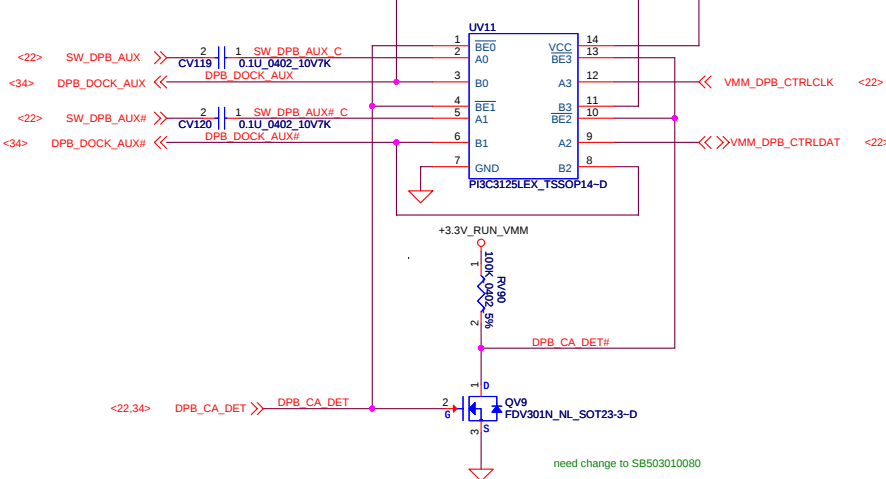


14"/15" use 8338 at DOCK config  
14"/15" use 12412 at Entry config

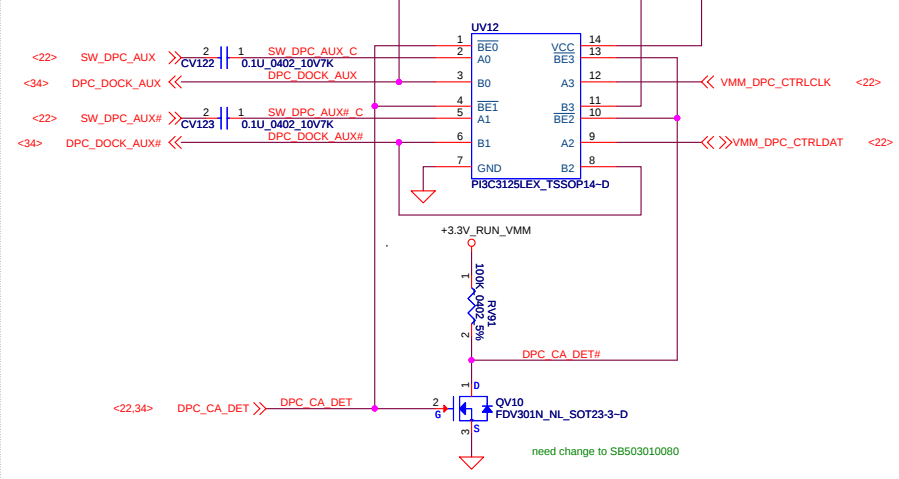
| PCB       | DP SWITCH      |
|-----------|----------------|
| H12 UMA   | PS8339+DP12412 |
| H12 Entry | PS8339         |
| H14 DSC   | PS8338         |
| H14 UMA   | PS8338         |
| H14D_En   | DP12412        |
| H14U_En   | DP12412        |
| H15 DSC   | PS8338         |
| H15 UMA   | PS8338         |
| H15D_En   | DP12412        |
| H15U_En   | DP12412        |



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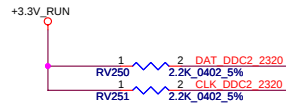


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| Size                 | Document Number | Rev |

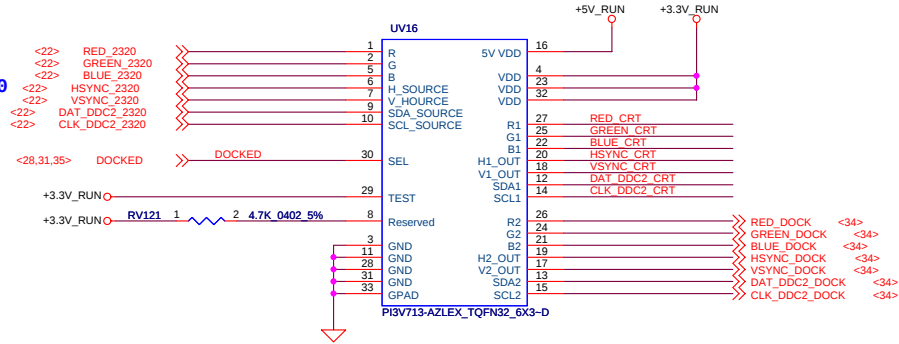
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| Date: | Monday, September 1, 2008 | Sheet | 1 | of | 1 |
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## VGA SW for MB/DOCK

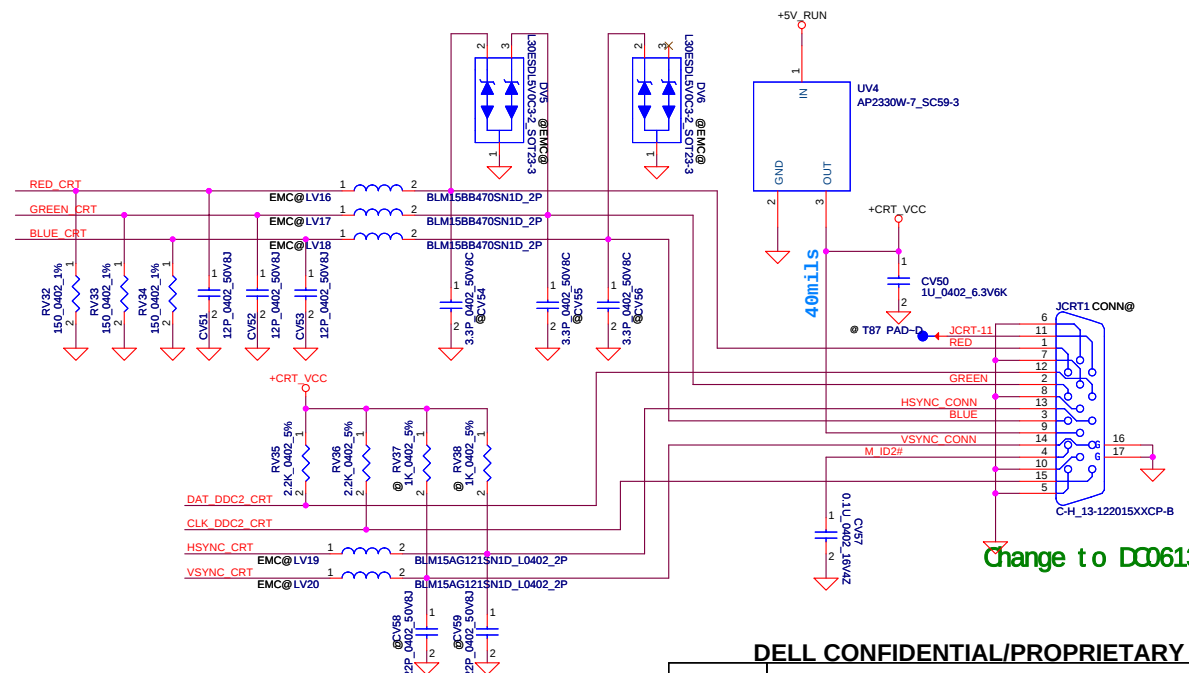
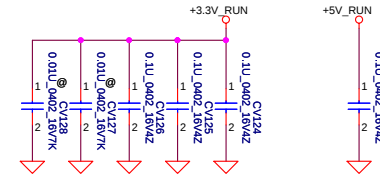
| PCB       | VGA SWITCH |
|-----------|------------|
| H12 UMA   | NA         |
| H12 Entry | NA         |
| H14 DSC   | PI3V713    |
| H14 UMA   | PI3V713    |
| H14D_En   | NA         |
| H14U_En   | NA         |
| H15 DSC   | PI3V713    |
| H15 UMA   | PI3V713    |
| H15D_En   | NA         |
| H15U_En   | NA         |



source from VMM2320



| SEL1/SEL2 | Chanel | Source  |
|-----------|--------|---------|
| 0         | A=B1   | MB      |
| 1         | A=B2   | APR/SP1 |



Change to DC061307290.

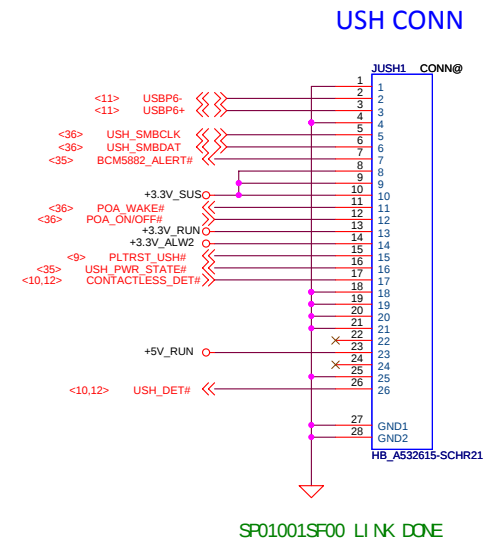
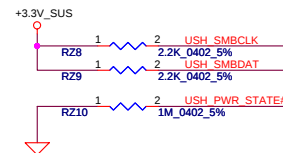
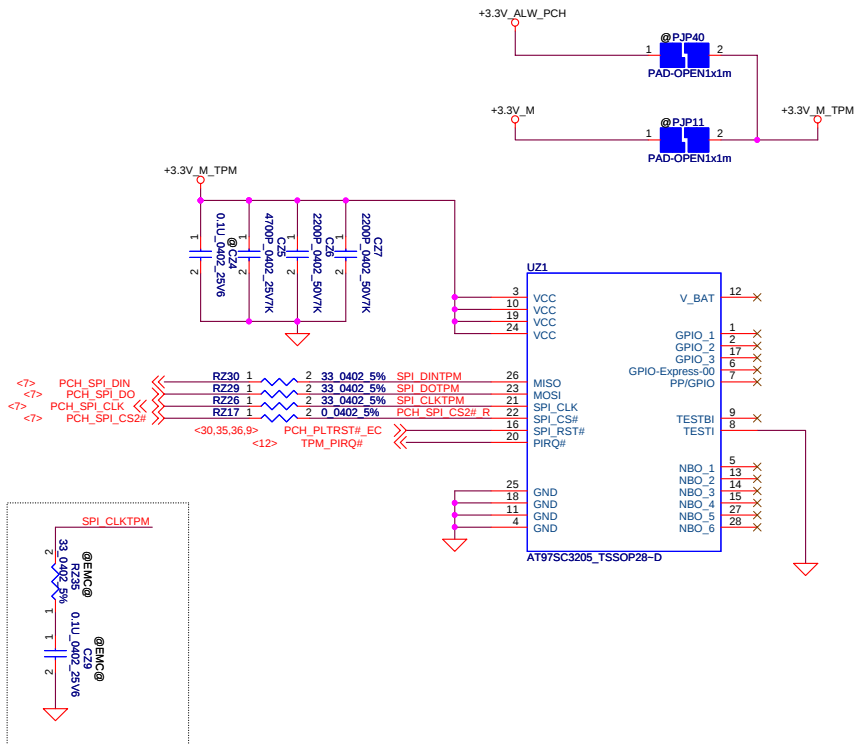


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4019RA

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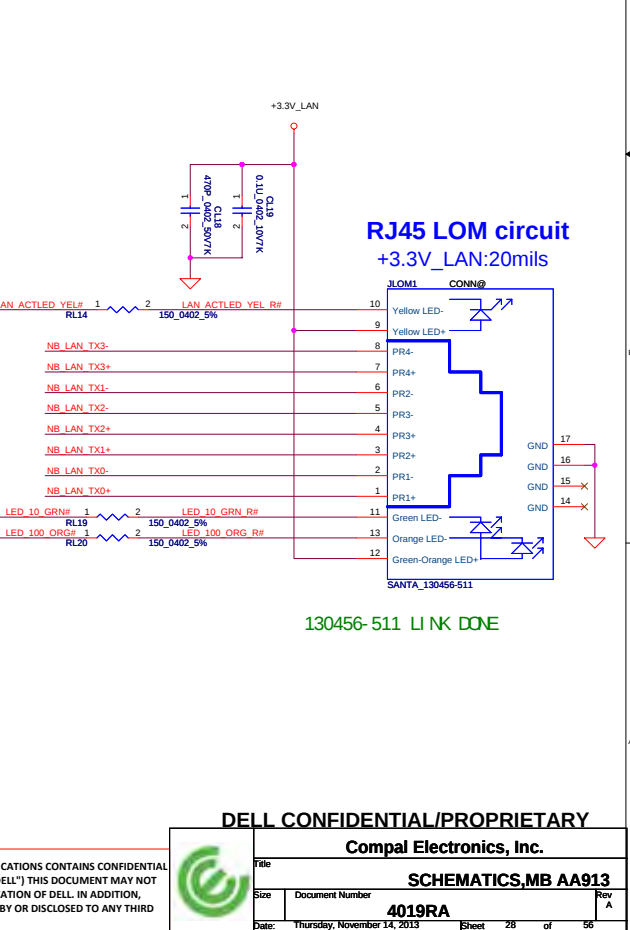
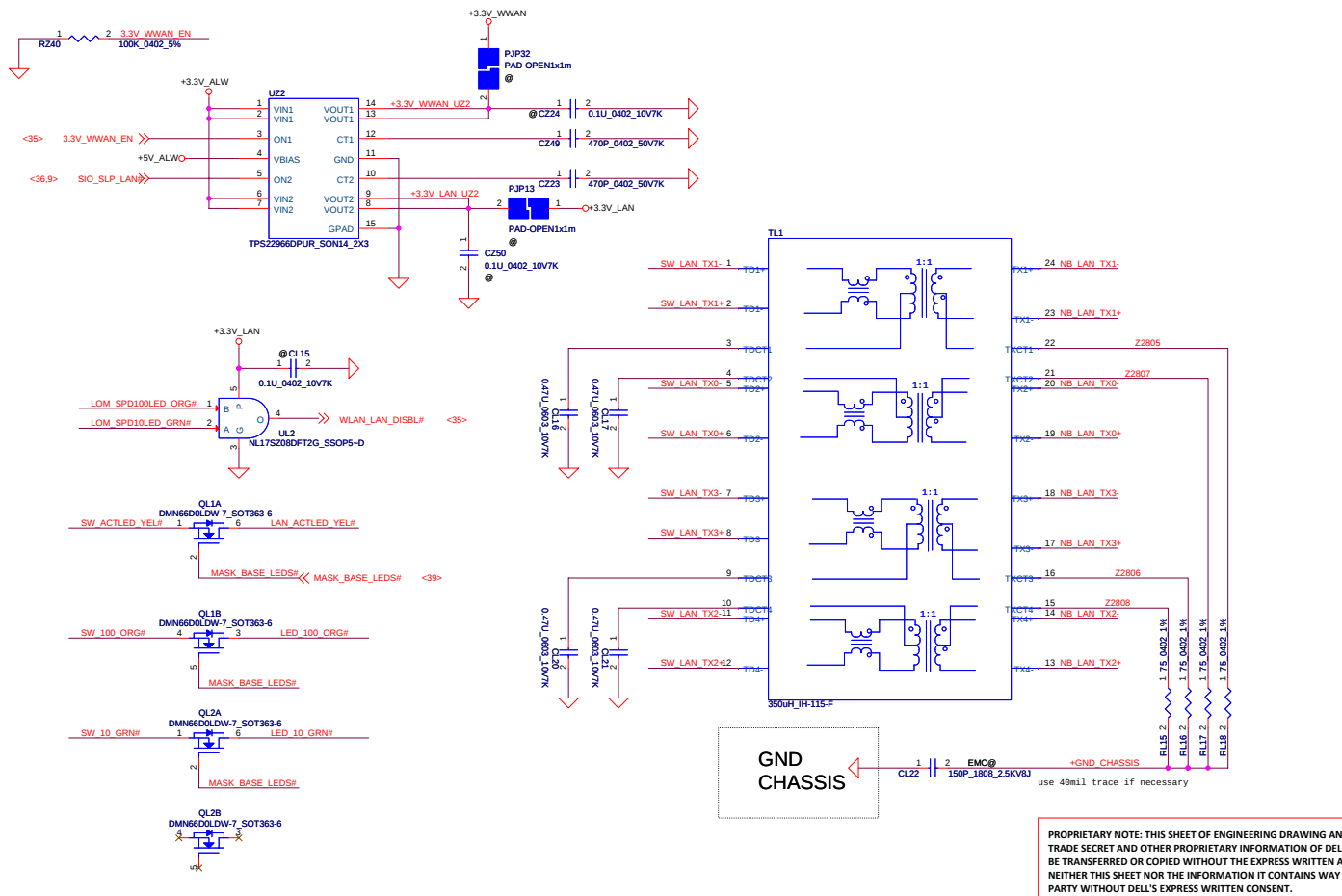
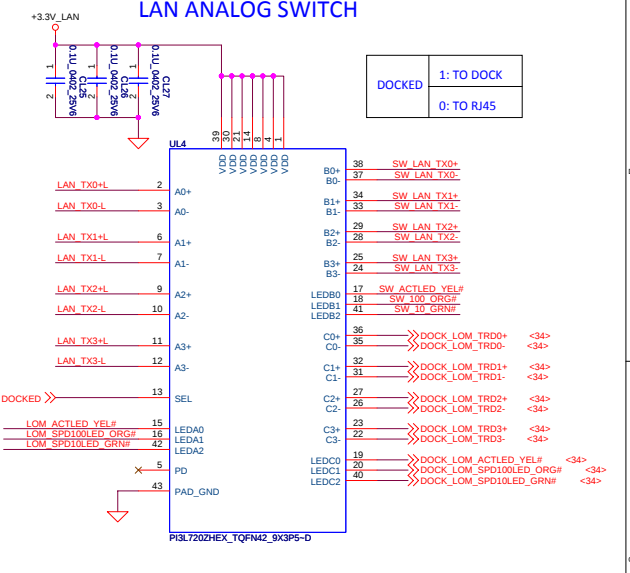
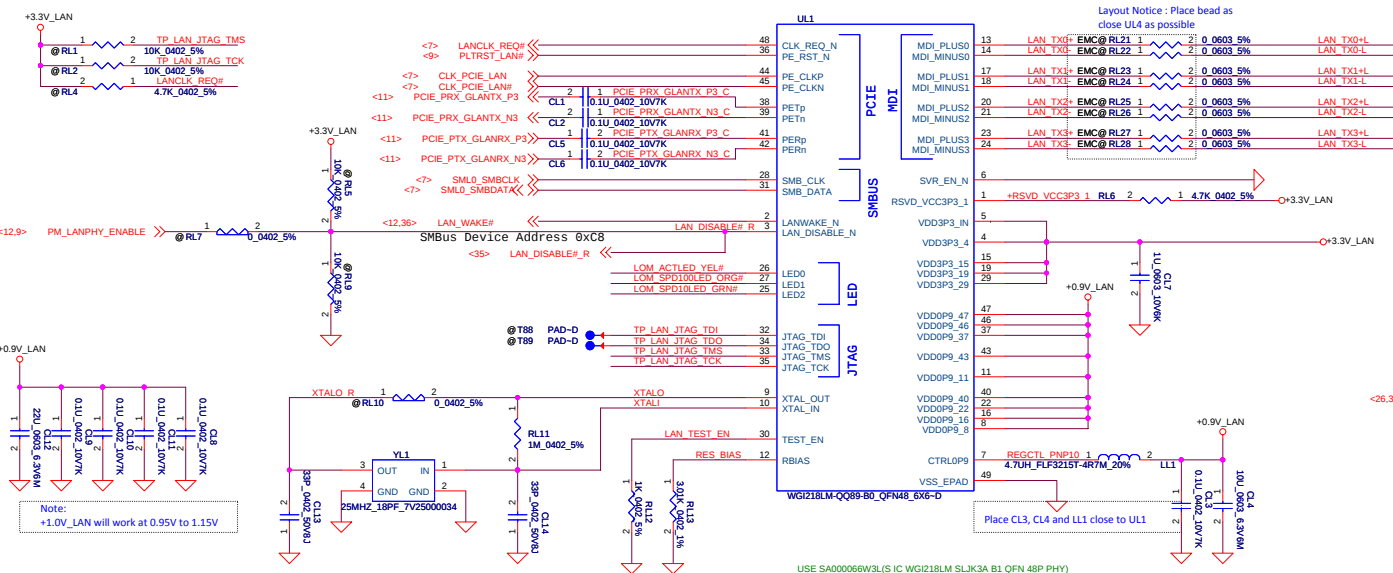
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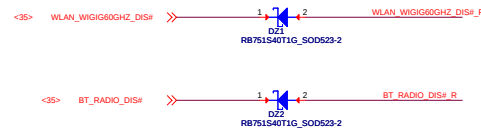
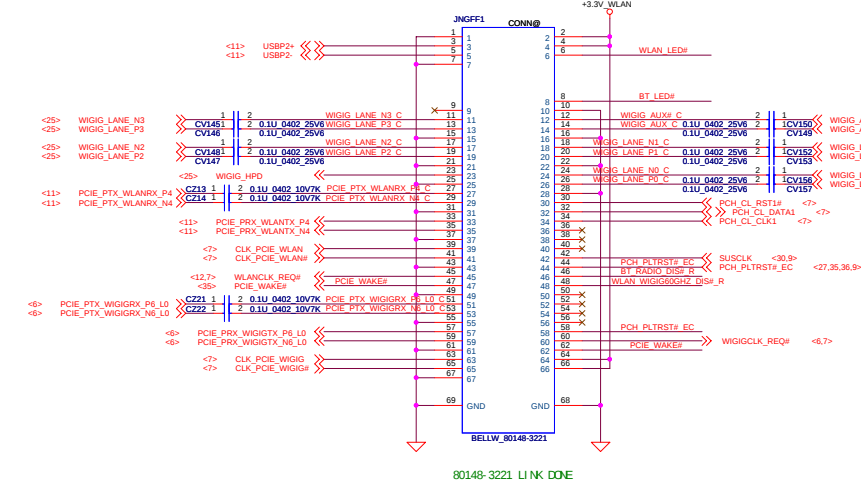
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| Size  | Document Number             | 4019RA |          |
| Date  | Thursday, November 14, 2013 | Sheet  | 27 of 56 |



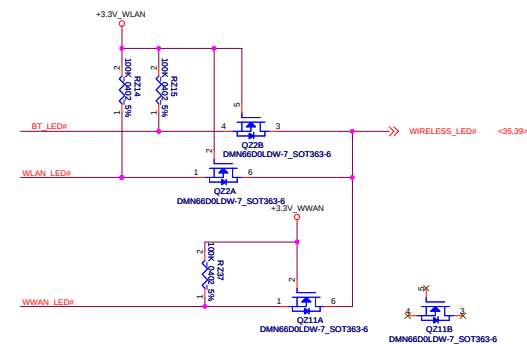
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NGFF slot A Key A

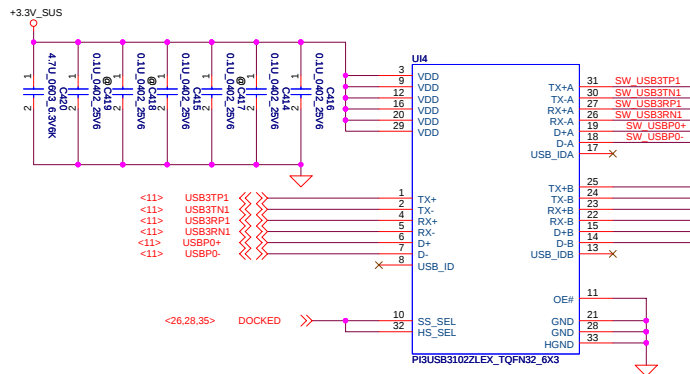
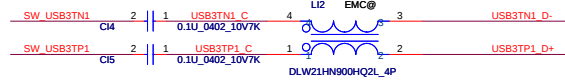
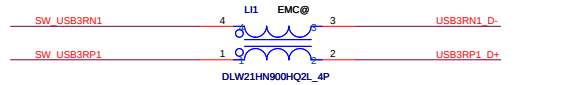


| Power Rating TBD |                   |               |        |           |
|------------------|-------------------|---------------|--------|-----------|
| PWR Rail         | Voltage Tolerance | Primary Power |        | Aux Power |
|                  |                   | Peak          | Normal | Normal    |
| +3.3V            |                   |               |        |           |



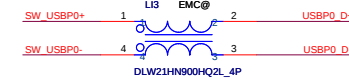
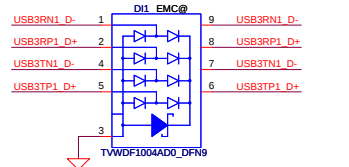
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| Date: |  | Thursday, November 14, 2013 |  | Sheet               |  | 81 of 81 |  |

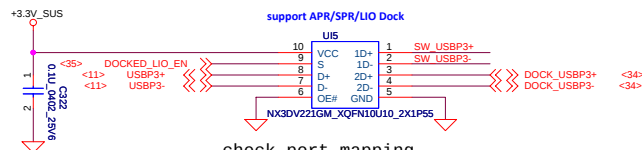
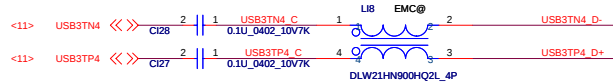
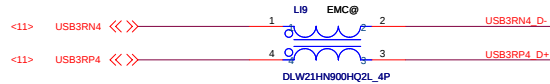
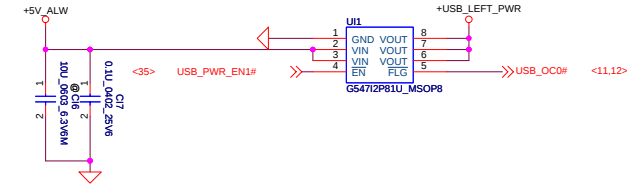
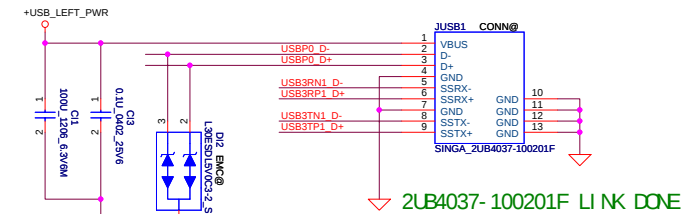


check port mapping

| DOCKED | function |
|--------|----------|
| 1      | Dock     |
| 0      | M/B      |

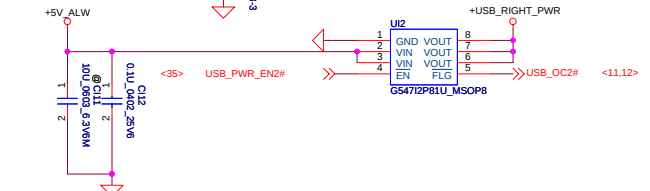
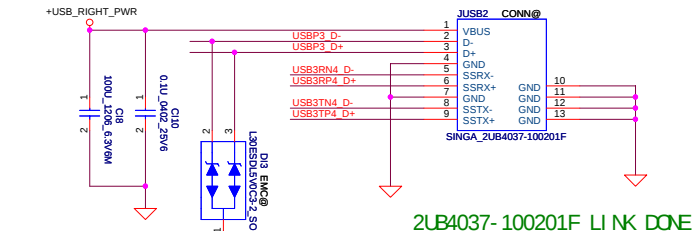
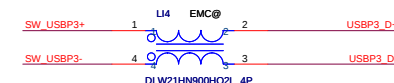
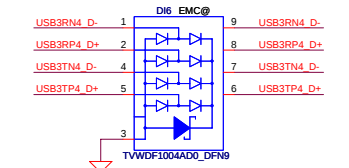


| PCB       | USB2 0  | USB2 3   |
|-----------|---------|----------|
| H12 UMA   | USB3102 | NX3DV221 |
| H12 Entry | NA      | NA       |
| H14 DSC   | USB3102 | NX3DV221 |
| H14 UMA   | USB3102 | NX3DV221 |
| H14D_En   | NA      | NA       |
| H14U_En   | NA      | NA       |
| H15 DSC   | USB3102 | NX3DV221 |
| H15 UMA   | USB3102 | NX3DV221 |
| H15D_En   | NA      | NA       |
| H15U_En   | NA      | NA       |



check port mapping

| DOCKED_LIO_EN | function |
|---------------|----------|
| 1             | Dock     |
| 0             | M/B      |



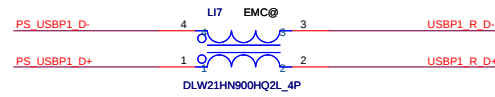
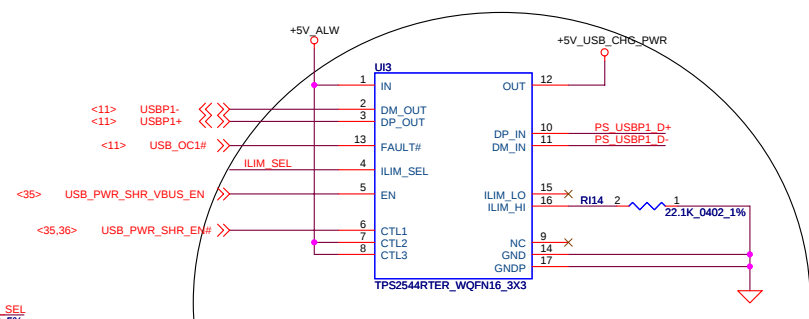
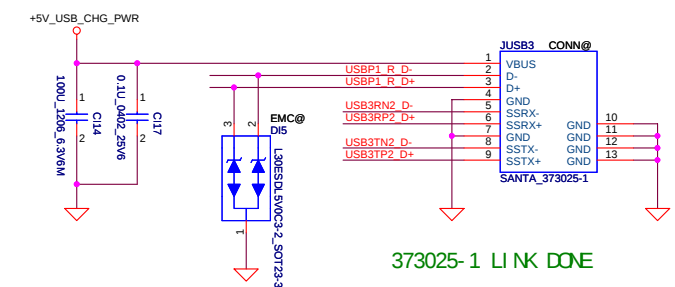
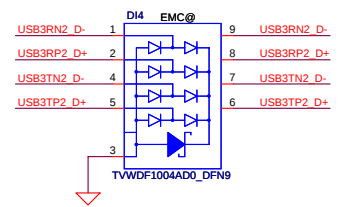
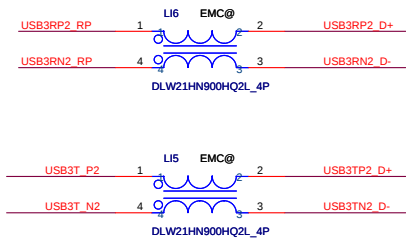
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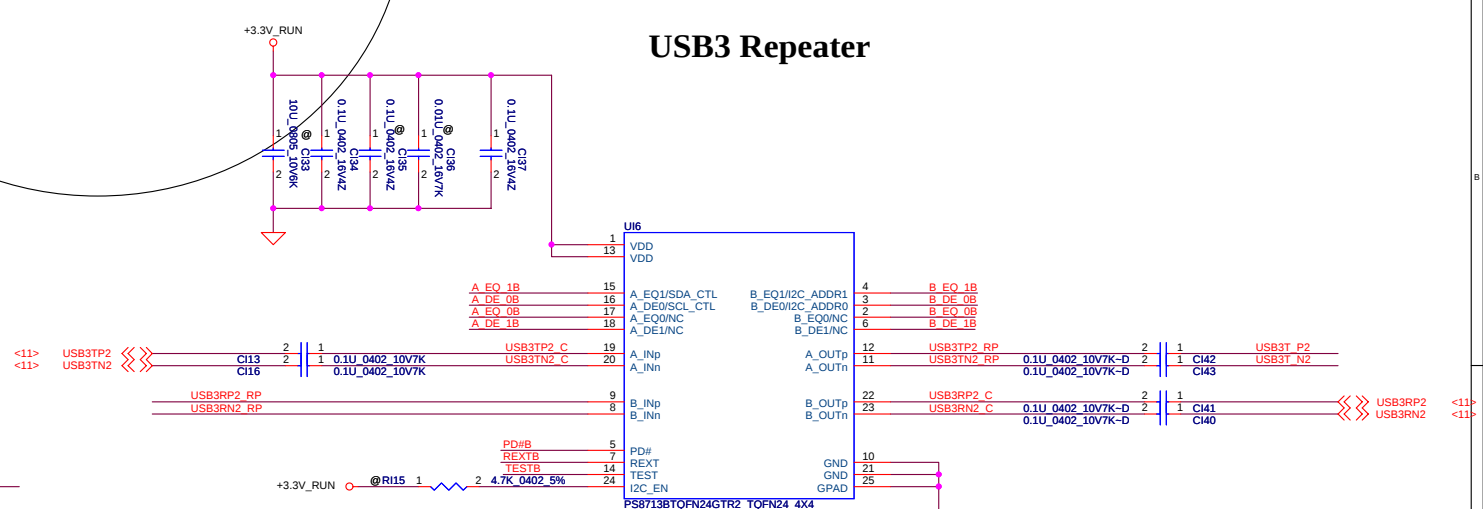
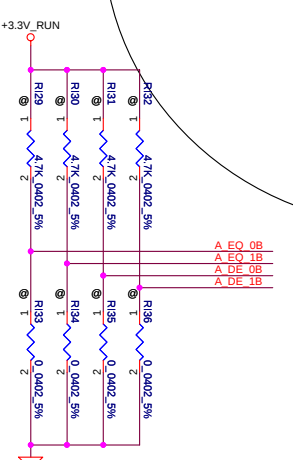
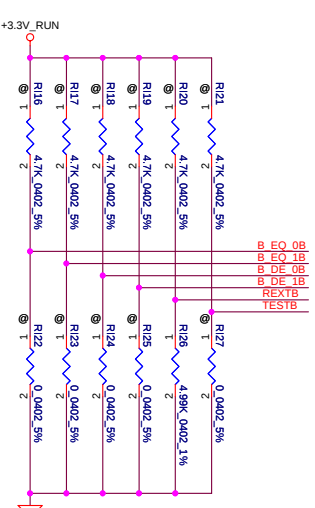


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| Size | Document Number             | 4019RA | Rev A    |
| Date | Thursday, November 14, 2013 | Sheet  | 31 of 56 |

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## USB3 Repeater



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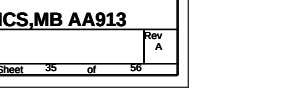
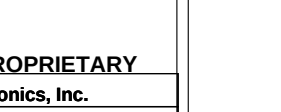
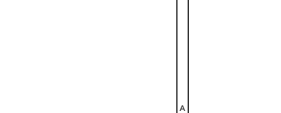
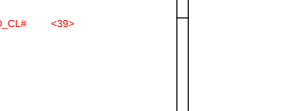
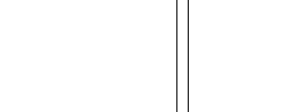
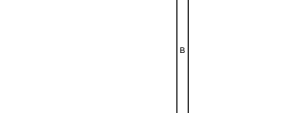
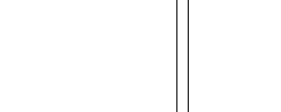
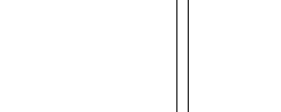
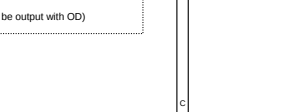
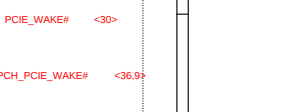
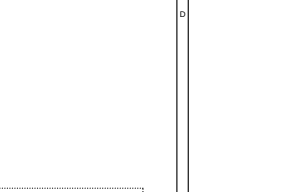
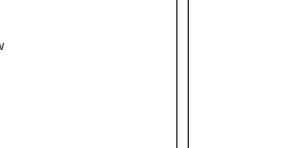
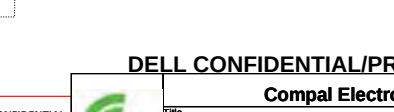
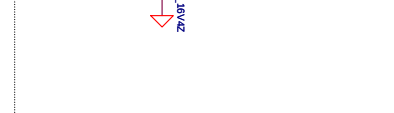
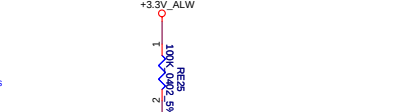
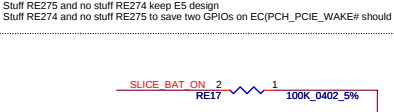
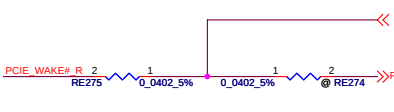
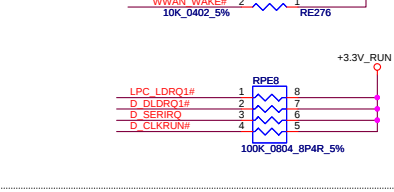
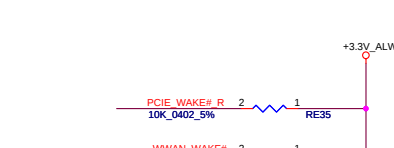
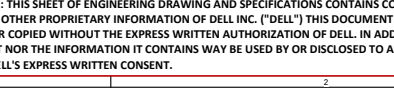
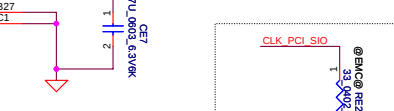
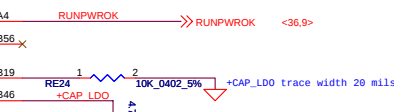
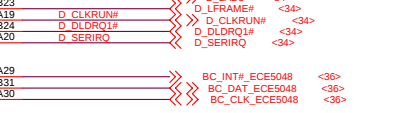
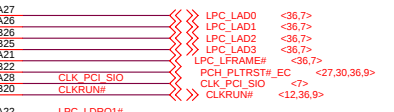
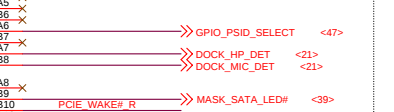
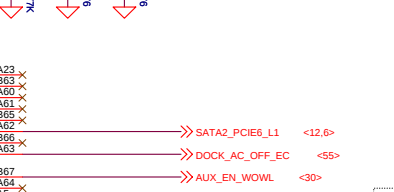
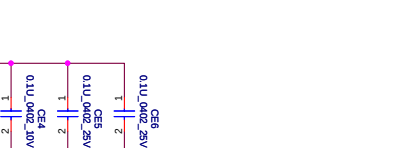
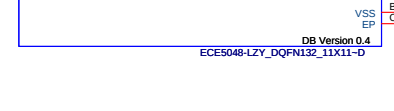
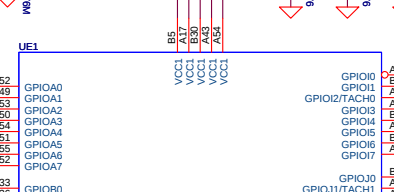
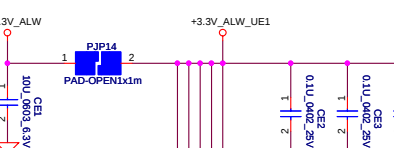
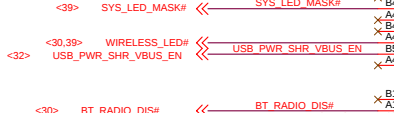
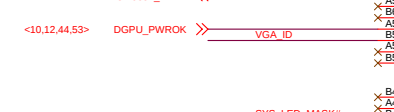
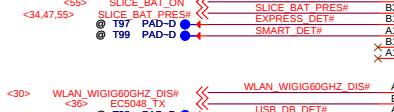
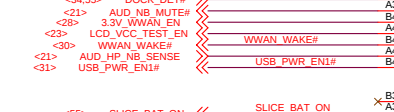
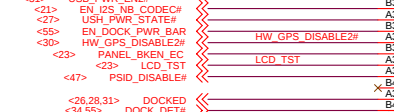
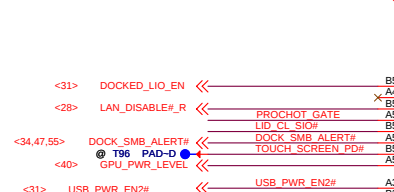
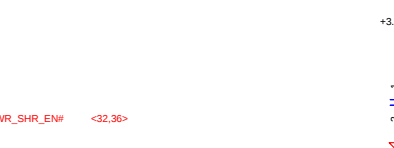
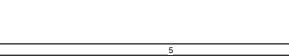
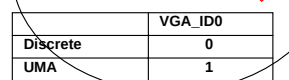
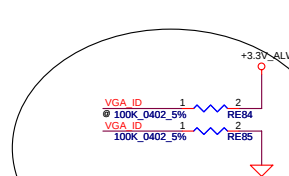
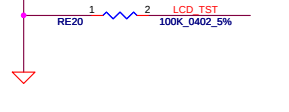
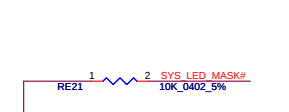
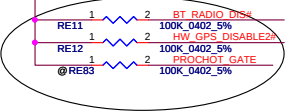
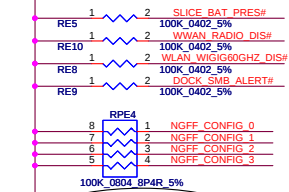
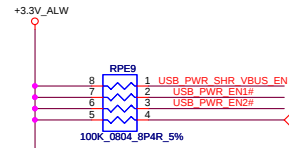


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| Size                | Document Number             | Rev            |
|                     | 4019RA                      | A              |
| Date:               | Thursday, November 14, 2013 | Sheet 33 of 56 |





|          |         |
|----------|---------|
|          | VGA_ID0 |
| Discrete | 0       |
| UMA      | 1       |

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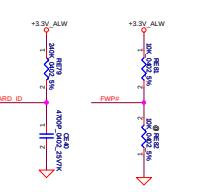
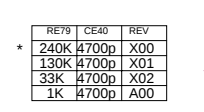
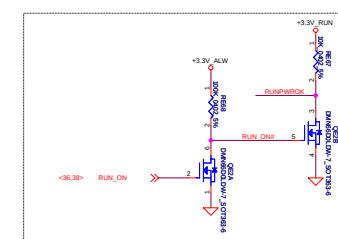
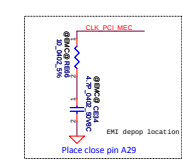
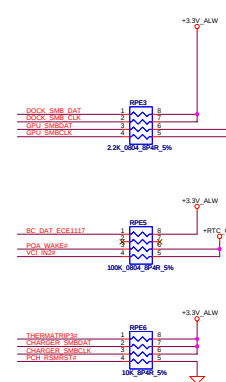
Compal Electronics, Inc.

SCHEMATICS,MB AA913

4019RA

Thursday, November 14, 2013

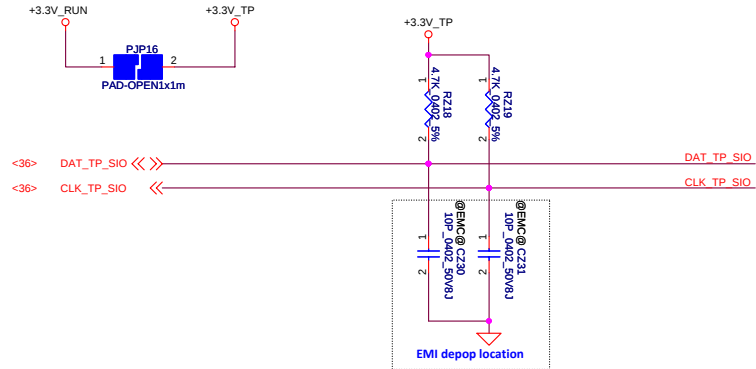
Sheet 35 of 56



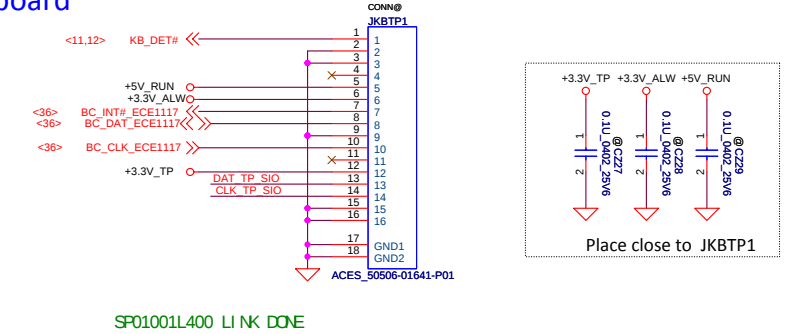
|                                           |                     |
|-------------------------------------------|---------------------|
| Channel 1                                 |                     |
| Thermal Monitoring Interface Strap Option |                     |
| HIGH                                      | Thermistor Readings |
| LOW                                       | Diode Readings      |



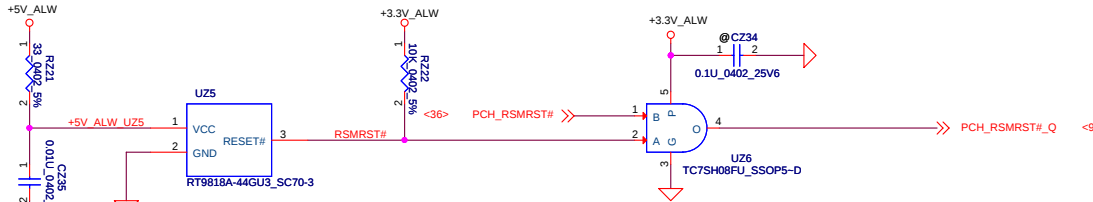
## Touch Pad



## Keyboard



## RSMRST circuit



### @eDP Cable

| Part Number | Description           |
|-------------|-----------------------|
| DC82C087A08 | H-CONN SET 13M MB-EDP |

### @eDP Cable w camera

| Part Number | Description                  |
|-------------|------------------------------|
| DC82C087908 | H-CONN SET 13M MB-EDP-CAMERA |

### @eDP TS Cable w camera

| Part Number | Description                     |
|-------------|---------------------------------|
| DC82C087808 | H-CONN SET 13M MB-EDP-CAMERA-TS |

### @SATA Cable-Spindle HDD

| Part Number | Description                   |
|-------------|-------------------------------|
| DC82C087808 | H-CONN SET 13M MB-SPINDLE HDD |

### @SATA Cable-mSATA

| Part Number | Description                 |
|-------------|-----------------------------|
| DC82C087708 | H-CONN SET 13M MB-mSATA HDD |

### @DC-IN Cable

| Part Number | Description                            |
|-------------|----------------------------------------|
| DC30180MF08 | CONN SET 0VN DCJACK-MB 20W1803-038110F |

### @RTC BATT

| Part Number | Description                            |
|-------------|----------------------------------------|
| DC30180MF08 | CONN SET 0VN DCJACK-MB 20W1803-038110F |

### @FAN

| Part Number | Description                          |
|-------------|--------------------------------------|
| DC28A080808 | FAN SET DAQ26 DC5V AB7405HB-HB3 ADDA |

### @KBTP FFC

| Part Number  | Description                             |
|--------------|-----------------------------------------|
| NBX08081JH08 | FFC 16P G P8.5 PAD=0.3 66.5MM MB-TP 13M |

### @Audio Board FFC

| Part Number  | Description                              |
|--------------|------------------------------------------|
| NBX08081JP08 | FFC 12P F P.5 PAD=.35 26.85MM MB-AUDIO/B |

### @USH Board FFC

| Part Number  | Description                              |
|--------------|------------------------------------------|
| NBX08081JF08 | FFC 26P G P8.5 PAD=0.3 58MM MB-USH/B 13M |

### @LED Board FFC

| Part Number  | Description                              |
|--------------|------------------------------------------|
| NBX08081JM08 | FFC 10P G P.5 PAD.3 192.5MM MB-LED/B 13M |

### @PWR Board FFC

| Part Number  | Description                             |
|--------------|-----------------------------------------|
| NBX08081JL08 | FFC 6P G P8.5 PAD=0.3 31MM MB-PWR/B 13M |

### @FP FFC-Validity

| Part Number  | Description                                   |
|--------------|-----------------------------------------------|
| NBX08081JN08 | FFC 8P F P8.5 PAD=0.3 170MM USH/B-FP VALIDITY |

### @FP FFC-TCS

| Part Number | Description                                |
|-------------|--------------------------------------------|
| NBX08081J08 | FFC 8P F P8.5 PAD=0.3 164.8MM USH/B-FP-TCS |

### @Speak

| Part Number  | Description                |
|--------------|----------------------------|
| PK2308083Q0L | SPK PACK ZJX 2.0W 4 OHM FG |

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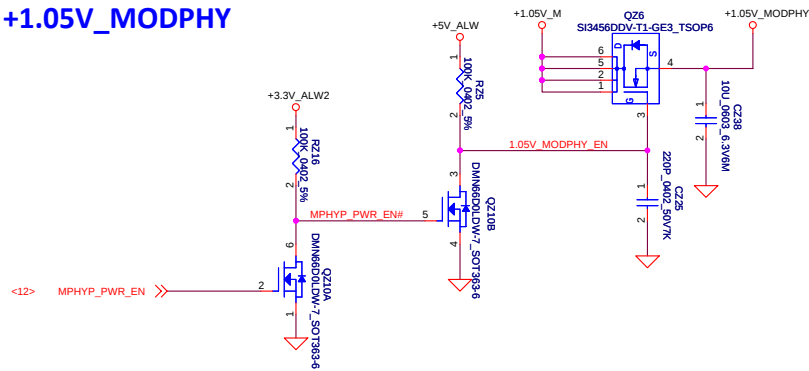
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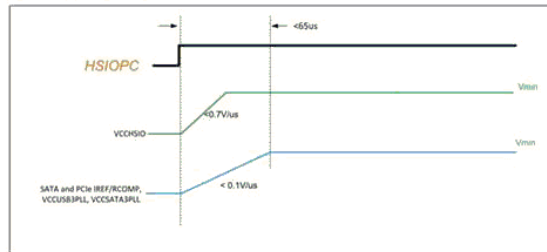
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|-------|-----------------------------|
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| Date  | Thursday, November 14, 2013 |
| Rev   | A                           |
| Sheet | 37 of 56                    |

## +1.05V\_MODPHY

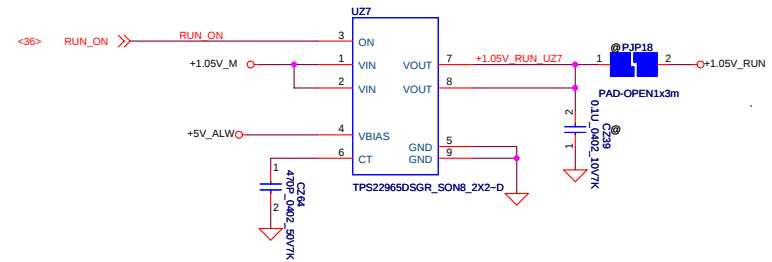


if support MODPHY off keep DSC solution  
MODPHY timing spec 0.7V/us and <65us

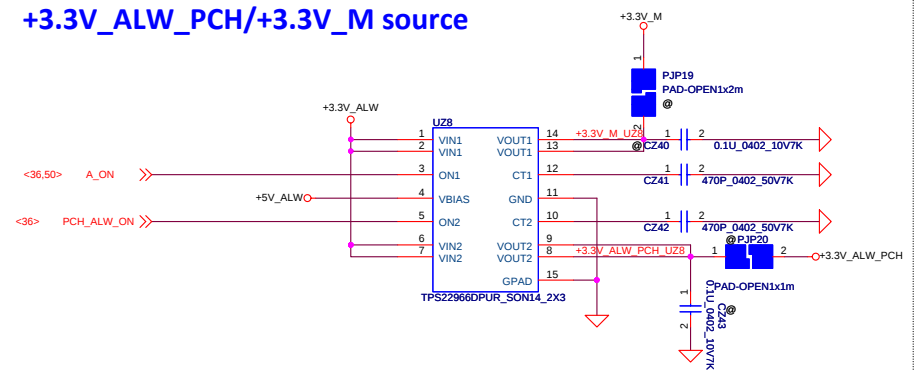
Figure 5-6. Sequencing Requirements between HSIOPC and LPT-LP 1.05V rails and COMP/IREF signals



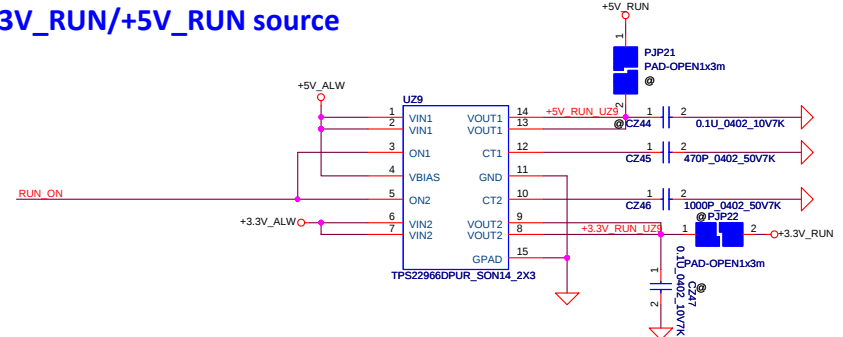
## +1.05V\_RUN source



## +3.3V\_ALW\_PCH/+3.3V\_M source



## +3.3V\_RUN/+5V\_RUN source



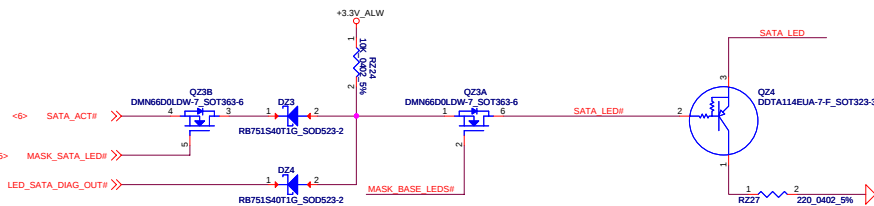
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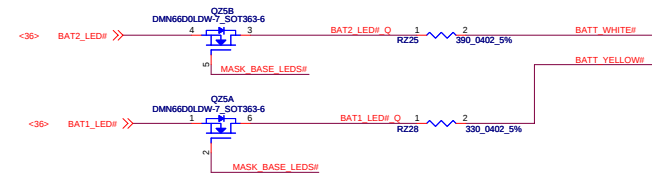
| SCHEMATICS, MB AA913 |                             |       |          |
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| Size                 | 4019RA                      |       |          |
| Date:                | Thursday, November 14, 2013 | Sheet | 38 of 56 |

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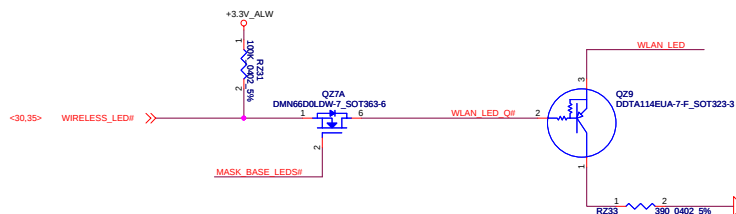
## HDD LED solution for White LED



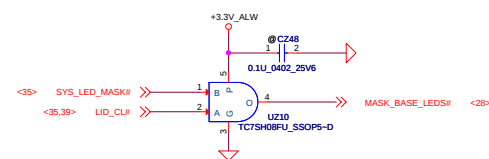
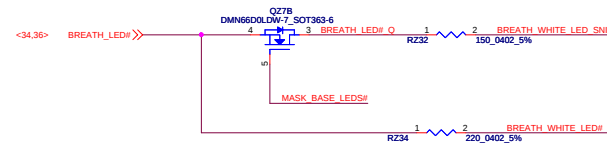
## Battery LED



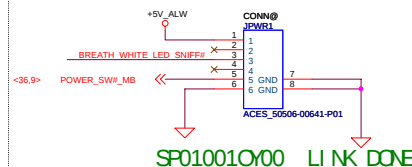
## WLAN LED solution for White LED



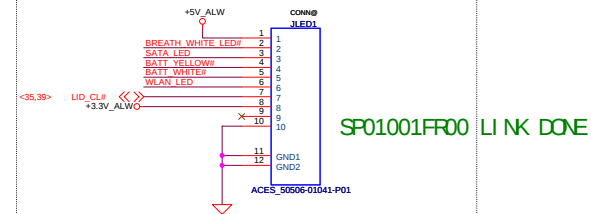
## Breath LED



## POWER board CONN



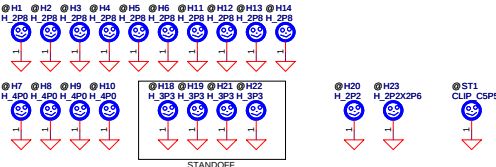
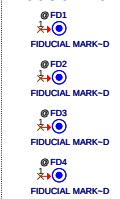
## LED board CONN

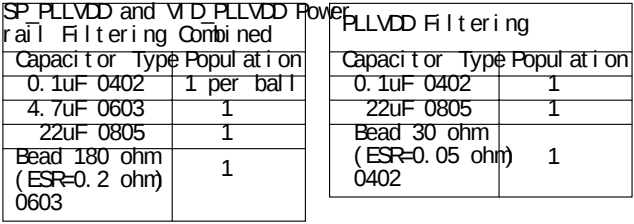


## LED Circuit Control Table

|                                  | SYS_LED_MASK# | LID_CL# |
|----------------------------------|---------------|---------|
| Mask All LEDs (Sniffer Function) | 0             | X       |
| Mask Base MB LEDs (Lid Closed)   | 1             | 0       |
| Do not Mask LEDs (Lid Opened)    | 1             | 1       |

## Fiducial Mark





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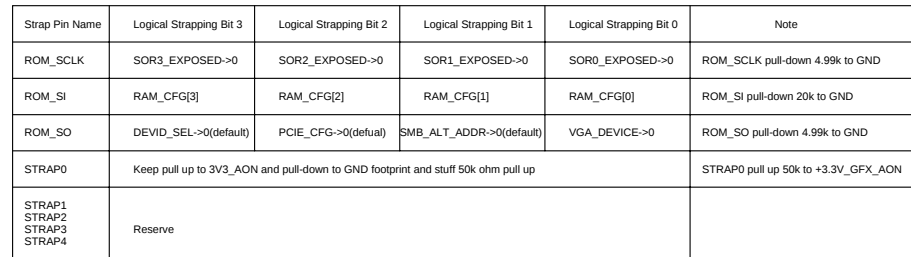
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| Size | Document Number | Rev |
|      | 4212DA          | A   |

Date: Thursday, November 14, 2013 Sheet 40 of 56

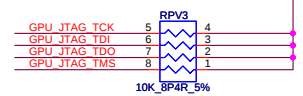
| SMBUS_ALT_ADDR | Description            |
|----------------|------------------------|
| 0              | 0x9E (Default)         |
| 1              | 0x9C (Multi-GPU usage) |

| VGA_DEV | Description                                    |
|---------|------------------------------------------------|
| 0       | Non-Primary 3D Acceleration Device(Class 0300) |
| 1       | Primary Display or VGA Device(Class 0300)      |

| Resistor Value | Full-up to V <sub>DD</sub> | Full-down to GND |
|----------------|----------------------------|------------------|
| 4.99K          | 1000                       | 0000             |
| 10K            | 1001                       | 0001             |
| 15K            | 1010                       | 0010             |
| 20K            | 1011                       | 0011             |
| 24.9K          | 1100                       | 0100             |
| 30.1K          | 1101                       | 0101             |
| 34.8K          | 1110                       | 0110             |
| 45.3K          | 1111                       | 0111             |

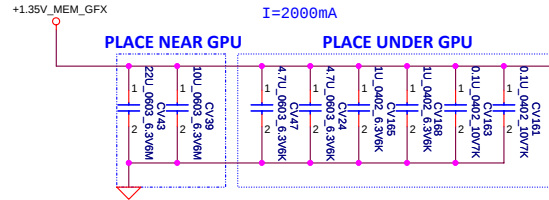


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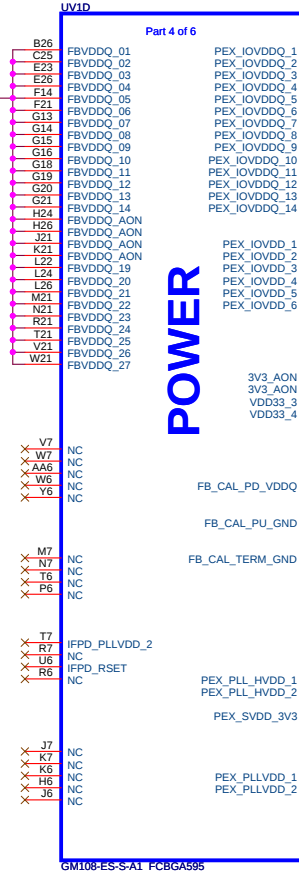
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|                                      | <b>4019RA</b>               |       | <b>A</b> |
| Date:                                | Thursday, November 14, 2013 | Sheet | 41 of 56 |

Date: Thursday, November 14, 2013 Sheet 41 of 56



| DDR3 CPU side FBVDDQ/FBVDDQ2 Combined Decoupling |      |            |
|--------------------------------------------------|------|------------|
| Capacitor                                        | Type | Population |
| 0.1uF                                            | 0402 | 2          |
| 1.0uF                                            | 0603 | 2          |
| 4.7uF                                            | 0603 | 2          |
| 10uF                                             | 0805 | 1          |
| 22uF                                             | 0805 | 1          |

| Power Supply Rail | NLS-GM   | NLS-GT |
|-------------------|----------|--------|
| (V)               | (A)      | (A)    |
| GPU_Core          | -        | 26     |
| GPU_FBI_O         | 1.5/1.35 | TBD    |
| PEX_I_OVDD_Q      | 1.05     | 0.765  |
| PEX_PLLVDD        | 1.05     | 0.130  |
| FBA_PLL_AVDD      | 1.05     | 0.062  |
| FBA_DLL_AVDD      | 1.05     | 0.032  |
| PLL_VDD           | 1.05     | 0.058  |
| SP_PLLVDD         | 1.05     | 0.030  |
| 1.05V Total       | 1.05     | 1.060  |
| VDD83+3V3AON      | 3.3      | 0.036  |
| PEX_SVDD_3V3      | 3.3      | 0.167  |
| PEX_PLL_HVDD      | 3.3      | 0.022  |
| 3.3V Total        | 3.3      | 0.225  |



| PEX_PLLVDD Decoupling |      |            |
|-----------------------|------|------------|
| Capacitor             | Type | Population |
| 0.1uF                 | 0402 | 1          |
| 1uF                   | 0603 | 1          |
| 4.7uF                 | 0805 | 1          |

| PEX_SVDD/PEX_PLL_HVDD Decoupling |      |            |
|----------------------------------|------|------------|
| Capacitor                        | Type | Population |
| 0.1uF                            | 0402 | 1          |
| 4.7uF                            | 0603 | 2          |

| 3V3_MAIN Decoupling |      |            |
|---------------------|------|------------|
| Capacitor           | Type | Population |
| 0.1uF               | 0402 | 2          |
| 1uF                 | 0603 | 1          |
| 4.7uF               | 0603 | 1          |

| 3V3_AON Decoupling |      |            |
|--------------------|------|------------|
| Capacitor          | Type | Population |
| 0.1uF              | 0402 | 1          |
| 1uF                | 0603 | 1          |
| 4.7uF              | 0603 | 1          |

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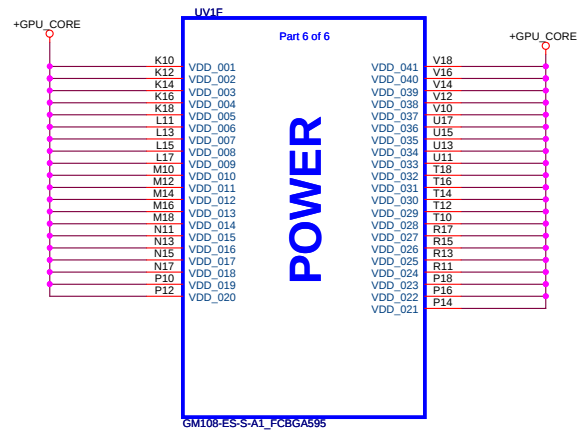
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Thursday, November 14, 2013 Sheet 42 of 56

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Caps on Power Side  
1UX4 4.7UX10 under GPU  
4.7UX5 22UX1 47UX2 330UX2 near GPU



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Date: Thursday, November 14, 2013 Sheet 43 of 56



**256x16 DDR3L**



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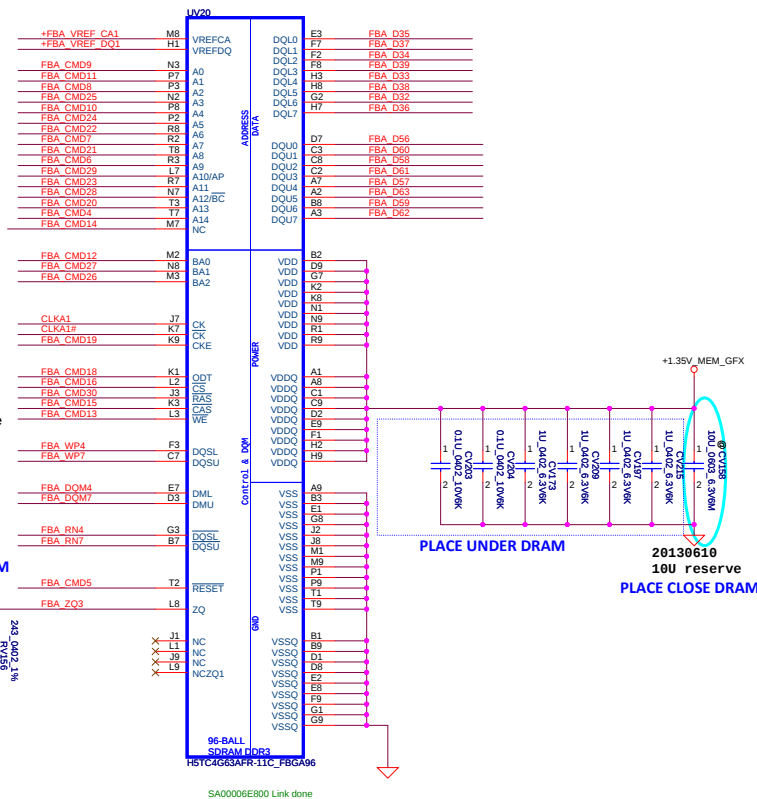
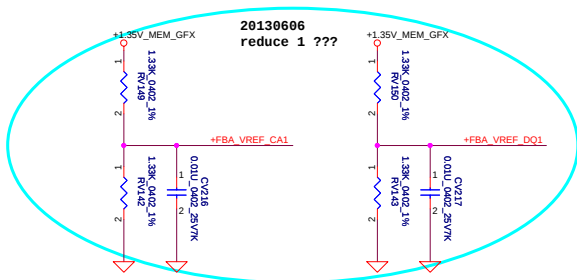
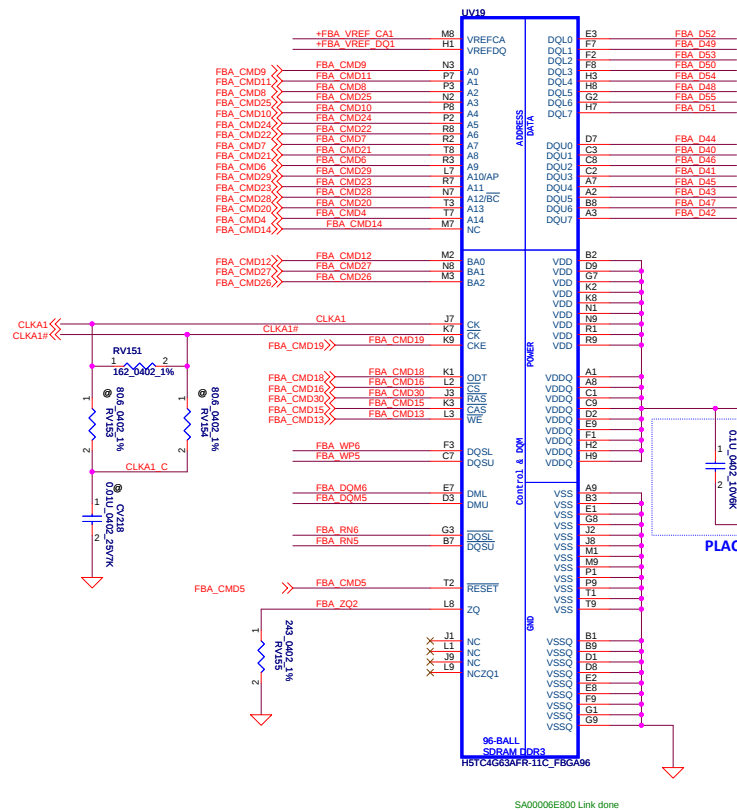
Date: Thursday, November 14, 2013 Sheet 45 of 5



# Memory Partition A - Lower 16 bits

256x16 DDR3L

FBA\_D[32..63] <<>> FBA\_D[32..63]  
FBA\_WP[4..7] <<>> FBA\_WP[4..7]  
FBA\_DQM[4..7] <<>> FBA\_DQM[4..7]  
FBA\_RN[4..7] <<>> FBA\_RN[4..7]

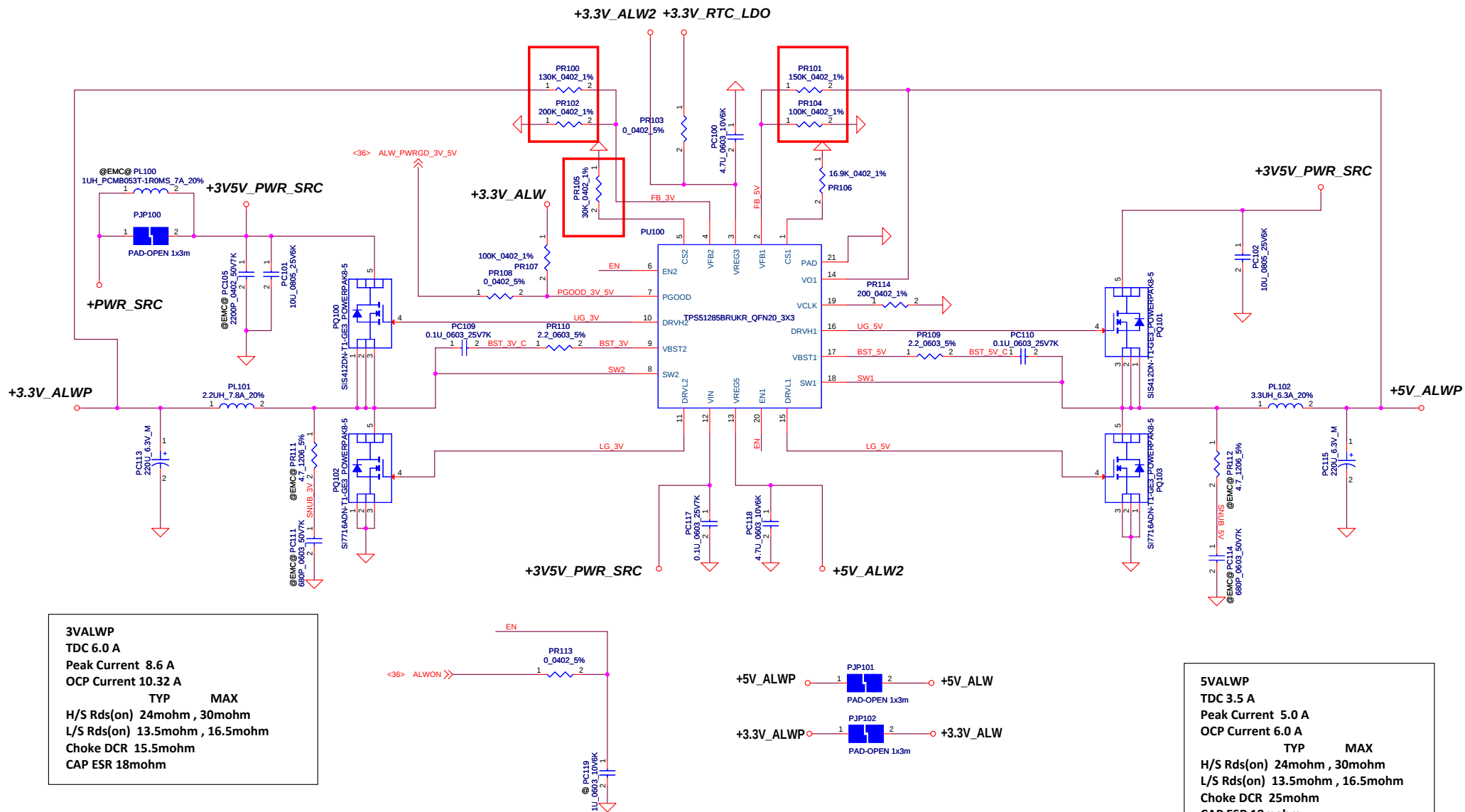


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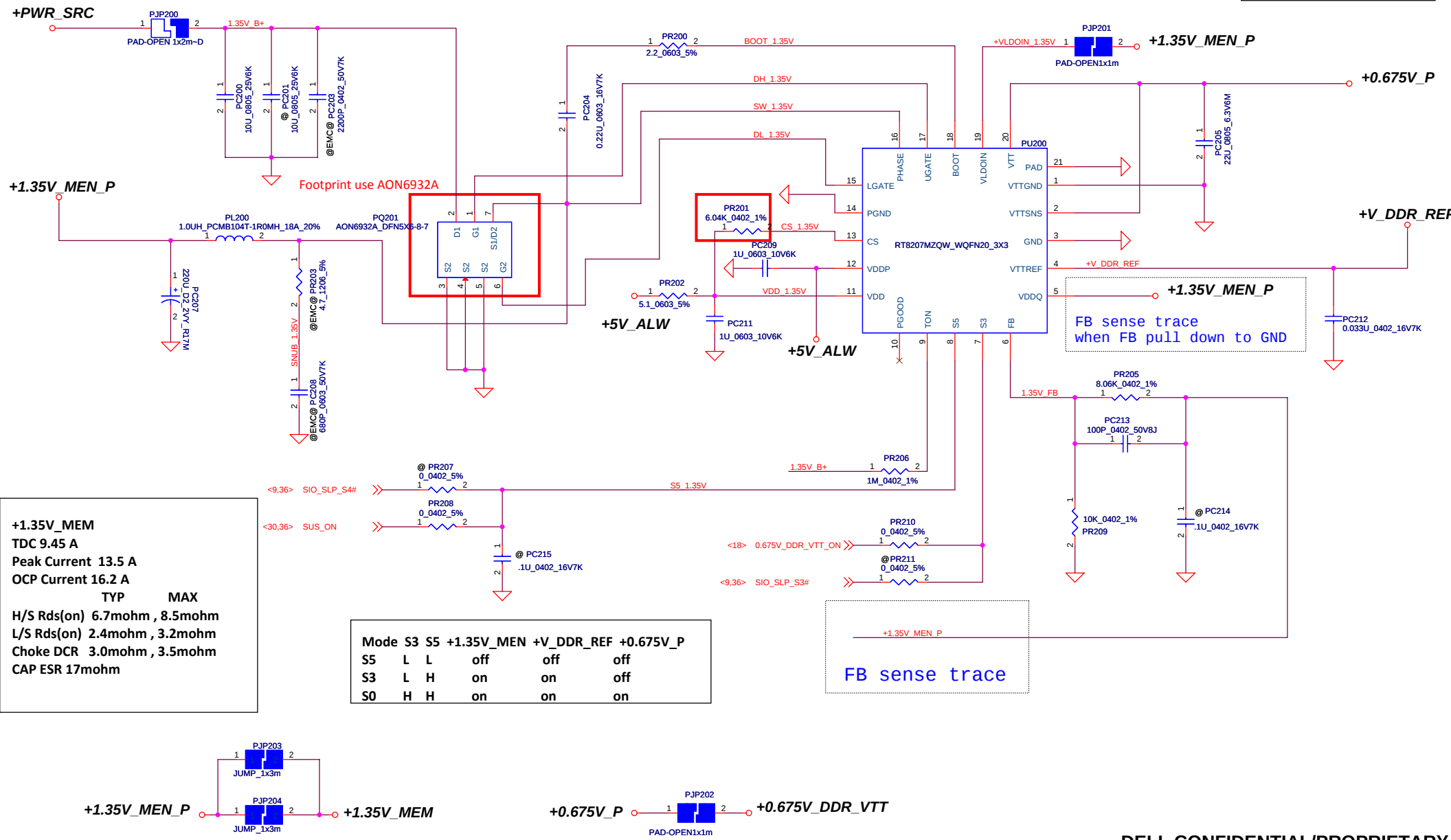
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|                          | 4019RA                      |       | A        |
| Date:                    | Thursday, November 14, 2013 | Sheet | 48 of 56 |

0.675Volt +/- 5%  
TDC 0.7 A  
Peak Current 1.0 A  
OCP Current 1.2 A



**+1.35V\_MEM**  
TDC 9.45 A  
Peak Current 13.5 A  
OCP Current 16.2 A

|             | TYP               | MAX |
|-------------|-------------------|-----|
| H/S Rds(on) | 6.7mohm , 8.5mohm |     |
| L/S Rds(on) | 2.4mohm , 3.2mohm |     |
| Choke DCR   | 3.0mohm , 3.5mohm |     |
| CAP ESR     | 17mohm            |     |

| Mode | S3 | S5 | +1.35V_MEN | +V_DDR_REF | +0.675V_P |
|------|----|----|------------|------------|-----------|
| S5   | L  | L  | off        | off        | off       |
| S3   | L  | H  | on         | on         | off       |
| S0   | H  | H  | on         | on         | on        |

FB sense trace

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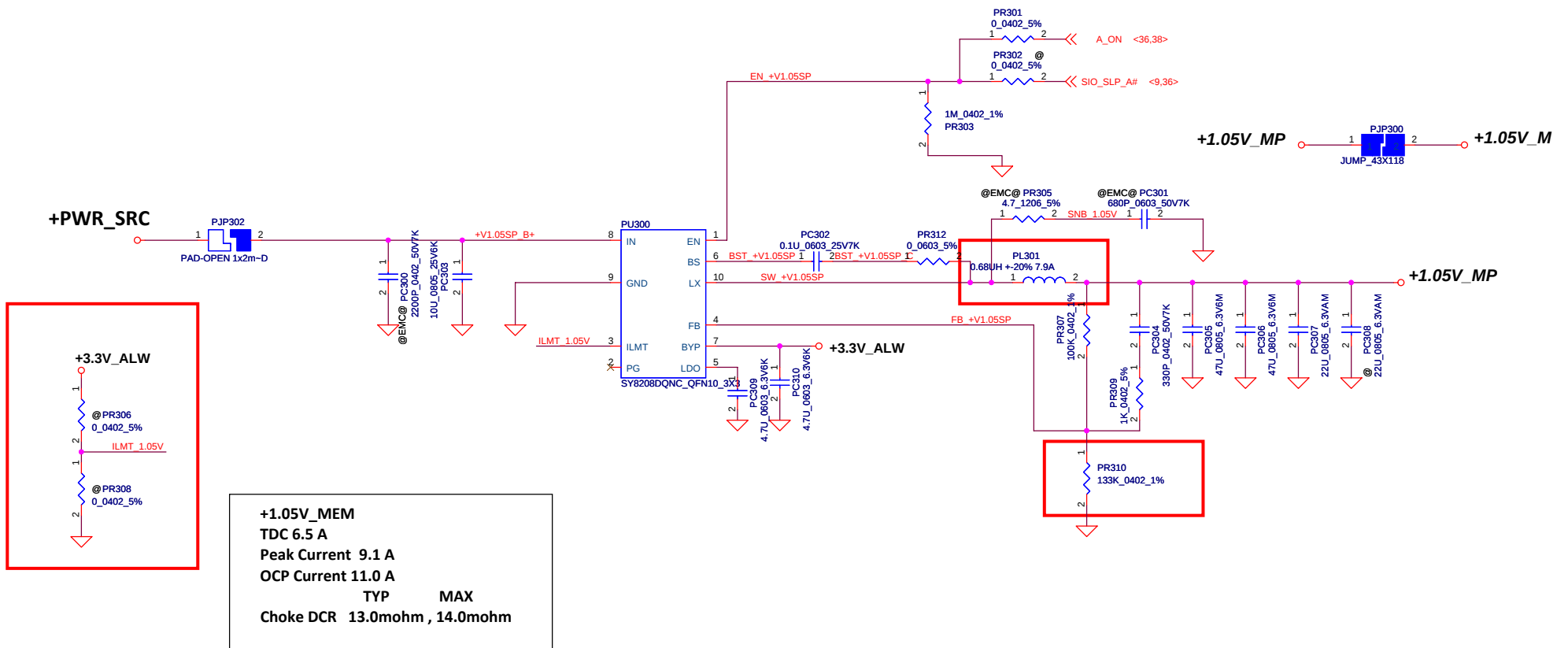
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4019RA

Sheet 49 of 56

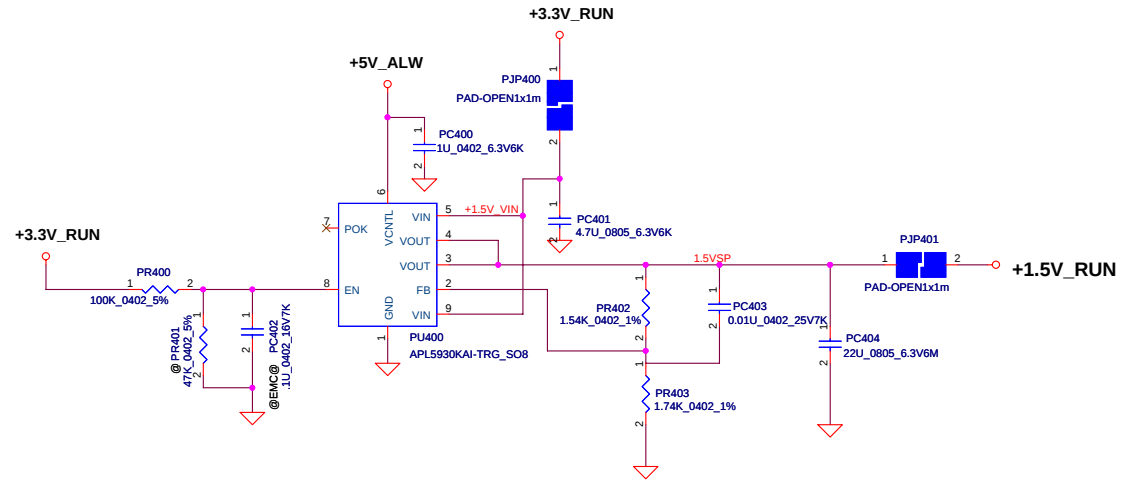
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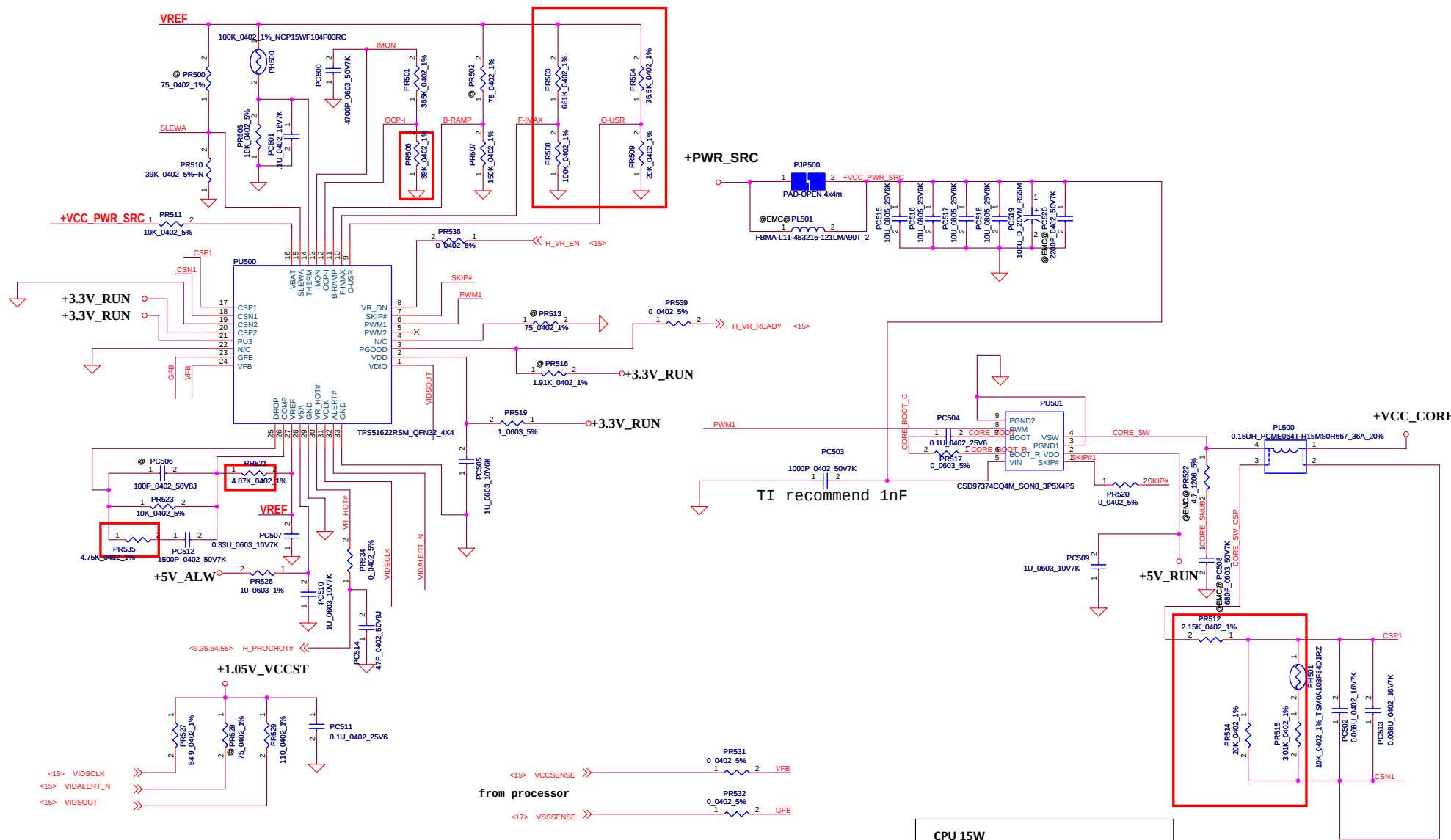


+1.5V\_RUN  
TDC 0.47 A  
Peak Current 0.67 A

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CPU 15W  
 TDC 10 A  
 Peak Current 32 A  
 OCP Current 38.4 A  
 DC Load line -2.0 mV/A  
 Icc\_Dyn\_VID1 27 A  
 Choke DCR: 0.66m +/-7% ohm  
 PH500 B Value : 4250k 1%  
 PH501 B Value : 3370k 1%

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Vboot=Vvref\*(Rref2/(Rref1+Rref2+Rboot))  
 Rt=Rrefadj // (Rboot+Rref2)  
 $V_{min} = V_{vref} * (R_{ref2} / (R_{ref2} + R_{boot})) * (R_t / (R_{ref1} + R_t))$   
 $V_{max} = V_{vref} * R_{ref2} / ((R_{ref1} / R_{refadj}) + R_{boot} + R_{ref2})$   
 $V_{out} = V_{min} + N * V_{step}$   
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

#### PWM-VID Spec and component Values

| PWM-VID Spec       | Config A | Config B | Config C |
|--------------------|----------|----------|----------|
| Vmin               | 0.6V     | 0.6V     | 0.65V    |
| Vmax               | 1.2V     | 1.2V     | 1.15V    |
| Vboot              | 0.875V   | 0.9V     | 0.9V     |
| Voltage step       | 6.25mV   | 6.25mV   | 25mV     |
| N of Voltage level | 96       | 96       | 20       |
| Rrefadj            | PR9      | 39K      | 20K      |
| Rref1              | PR5      | 39K      | 20K      |
| Rboot              | PR8      | 1.5K     | 2K       |
|                    | PR10     | 30K      | 18K      |
| Rref2=PR10+PR12    | PR12     | 1.5K     | 0        |
| C                  | PC8      | 1.5nf    | 2.7nf    |

Module model information:  
 RT8813A\_V1A for IC module  
 RT8813A\_V1B for SW module

Current Limit threshold setting  
 $R_{ocset} = (I_{valley} * R_{ds(on)} + 40 \text{ mV}) / 10 \mu A$   
 $I_{ripple} = (19 - 0.9) * 0.9 / (304.89 \text{ Khz} * 0.36 \mu s * 19) = 7.811 A$   
 $OCP = 54 A / 2 = 27 A$  per phase  
 $I_{valley} = 27 A - 7.811 A / 2 = 23.1 A$

H-side MOS:TPCA8065  
 $R_{ds(on)} = 11.7 \text{ mohm} @ V_{gs} = 10V$   
 $9.4 \text{ mohm} @ V_{gs} = 4.5V$   
 $I_d = 16 A @ T_a = 25 \text{ degC}$   
 L-side MOS:TPCA8057  
 $R_{ds(on)} = 2.0 \text{ mohm} @ V_{gs} = 10V$   
 $2.6 - 3.2 \text{ mohm} @ V_{gs} = 4.5V$   
 $I_d = 42 A @ T_a = 25 \text{ degC}$

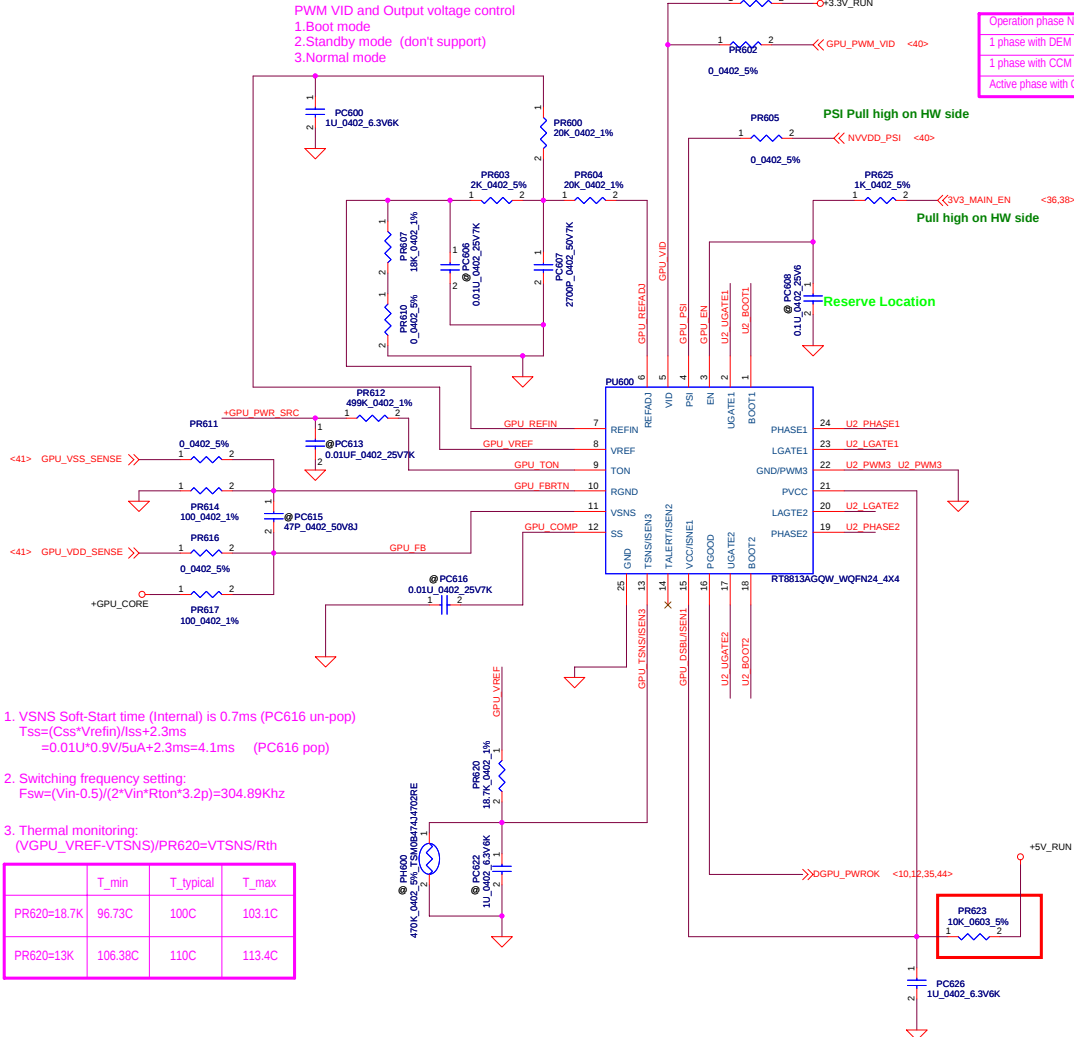
Choke: 0.36uH (Size:10\*10\*4)  
 $R_{dc} = 1.1 \text{ mohm} \pm 5\%$   
 Heat Rating Current=30A  
 Saturation Current=50A

$C = 3 * 330 \mu F (9 \text{ mohm}) = 990 \mu F$   
 $V_{ripple} = \text{ripple} * ESR(\text{min}) = 7.811 A * 3 \text{ mohm} = 23.4 \text{ mV}$

#### Different VGA Chip (different EDP-Peak Current) need select different solution

| VGA Chip                     | N14P-GV     | N14P-GV2    | N14M-GS     | N14M-LP     | N14P-LP     | N14P-GE     | N14P-GS              | N14P-GT                |
|------------------------------|-------------|-------------|-------------|-------------|-------------|-------------|----------------------|------------------------|
| OpenVReg Configurations      | Config B    | Config B    | Config B    | Config B    | Config B    | Config B    | Config B             | Config B               |
| Rated TDP Power at Tj=102C   | 18W         | 25W         | 18W         | 13W         | 18.9W       | 25W         | 25.6W                | 35.5W                  |
| Boosted GPU Total at Tj=102C | 25W         | 32W         | 25W         | 20W         | 23W         | N/A         | 30W                  | 40W                    |
| EDP-Continuous at Tj=102C    | 24A         | 32A         | 26A         | 22A         | 25A         | 27A         | 38A                  | 45A                    |
| EDP-Peak at Tj=102C          | 35A         | 55A         | 45A         | 35A         | 35A         | 40A         | 60A                  | 75A                    |
| Istep max (Evaluation)       | 15A         | 27A         | 25A         | 20A         | 14A         | 12A         | 31.5A                | 35A                    |
| OCP Setting Current          | 42A         | 66A         | 54A         | 42A         | 42A         | 48A         | 72A                  | 90A                    |
| Rocset                       | 8.96K       | 12.45K      | 10.7K       | 8.96K       | 8.96K       | 9.83K       | 8.3K                 | 9.39K                  |
| Recommendation               | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H1L | 2phase 1H2L          | 2phase 1H2L            |
| Polymer Cap (330uF)          | 6mohm * 2   | 9mohm * 3   | 9mohm * 3   | 6mohm * 2   | 6mohm * 2   | 6mohm * 2   | 6mohm * 3 (L=0.22uH) | 4.5mohm * 3 (L=0.15uH) |
| Or OSCON (390uF)             | 10mohm * 3  | 10mohm * 3  | 10mohm * 3  | 10mohm * 3  | 10mohm * 3  | 10mohm * 3  | NULL                 | NULL                   |

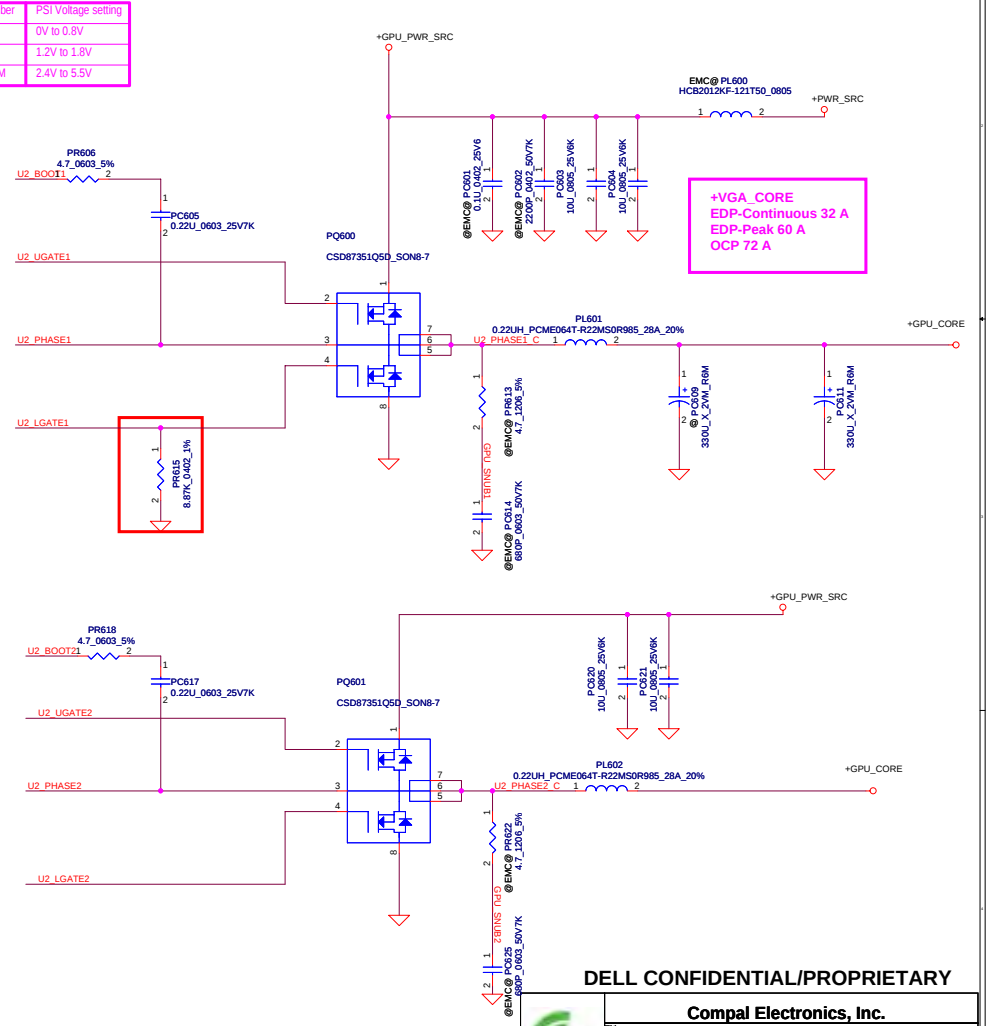
PWM VID and Output voltage control  
 1.Boot mode  
 2.Standby mode (don't support)  
 3.Normal mode



- VSNS Soft-Start time (Internal) is 0.7ms (PC616 un-pop)  
 $T_{ss} = (C_{ss} * V_{refin}) / I_{ss} \approx 2.3 \text{ ms}$   
 $= 0.01 \mu F * 0.9V / 5 \mu A + 2.3 \text{ ms} = 4.1 \text{ ms}$  (PC616 pop)
- Switching frequency setting:  
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2 \text{ p}) = 304.89 \text{ Khz}$
- Thermal monitoring:  
 $(V_{GPU\_VREF} - V_{TSNS}) / PR620 = V_{TSNS} / R_{th}$

|             | T_min   | T_typical | T_max  |
|-------------|---------|-----------|--------|
| PR620=18.7K | 96.73C  | 100C      | 103.1C |
| PR620=13K   | 106.38C | 110C      | 113.4C |

| Operation phase Number | PSI Voltage setting |
|------------------------|---------------------|
| 1 phase with DEM       | 0V to 0.8V          |
| 1 phase with CCM       | 1.2V to 1.8V        |
| Active phase with CCM  | 2.4V to 5.5V        |



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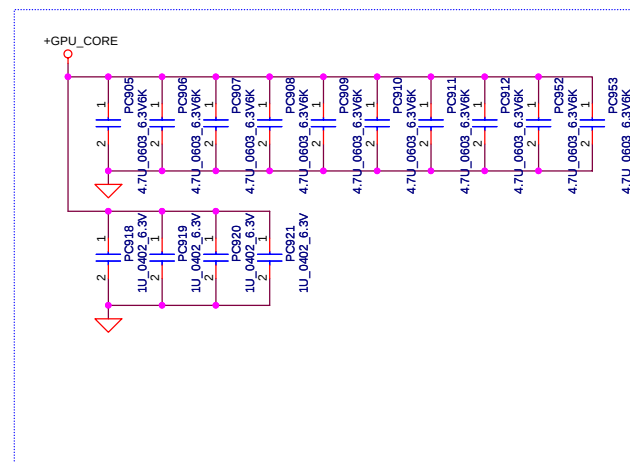
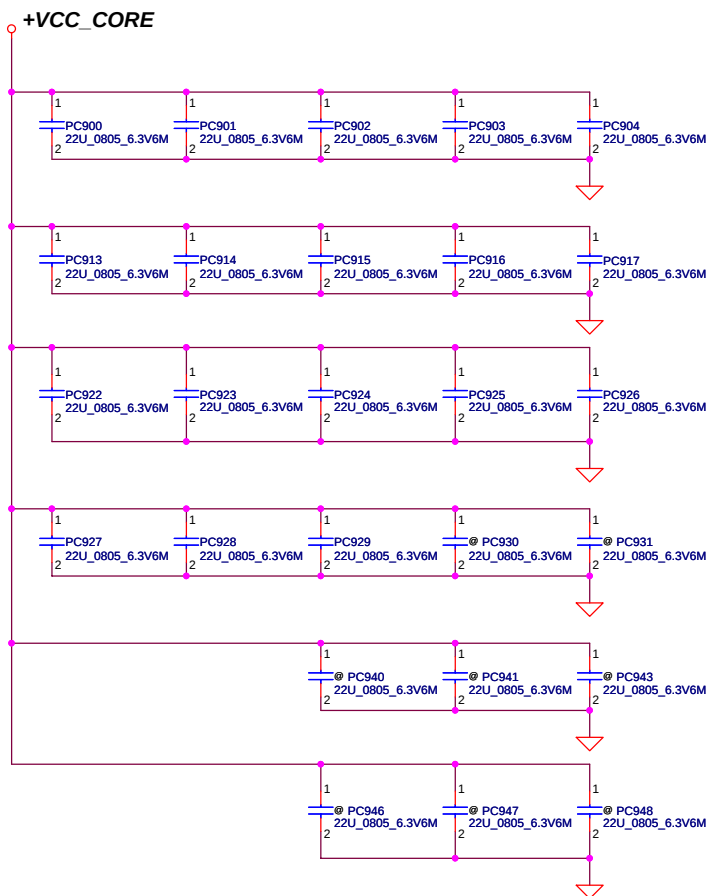
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| 4019RA |                 | A   |

Date: Thursday, November 14, 2013 Sheet 53 of 56

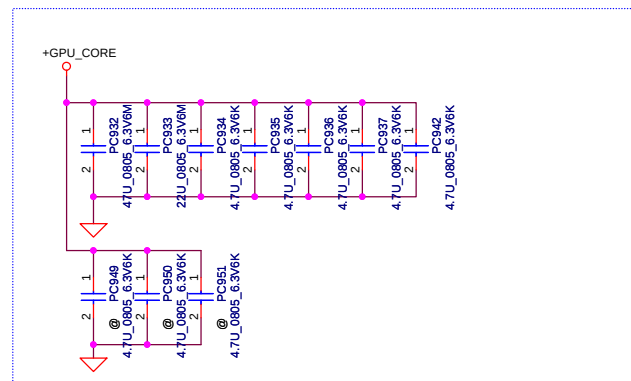
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nVidia GB4-64 package  
Under GPU  
4.7uF 0603 \* 10  
1uF 0402 \* 4



nVidia GB4-64 package  
Near GPU  
47uF 0805 \*1  
22uF 0805 \*1  
4.7uF 0805 \*5

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