



<

## BOM Variants

| BOM NUMBER | BOM NAME                         | BOM OPTIONS                                         |
|------------|----------------------------------|-----------------------------------------------------|
| 639-00613  | PCBA, MLB, BETTER, HY-4GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:HYNIX_4GB, ALTERNATE   |
| 639-00614  | PCBA, MLB, BETTER, HY-8GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:HYNIX_8GB, ALTERNATE   |
| 639-00616  | PCBA, MLB, BETTER, SM-4GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:SAMSUNG_4GB, ALTERNATE |
| 639-00617  | PCBA, MLB, BETTER, SM-8GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:SAMSUNG_8GB, ALTERNATE |
| 639-00621  | PCBA, MLB, BETTER, EL-4GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:ELPIDA_4GB             |
| 639-00622  | PCBA, MLB, BETTER, EL-8GB, X430  | MLB_CMNPTS, CPU:1.6GHZ, DDR3:ELPIDA_8GB             |
| 639-00695  | PCBA, MLB, BETTER, EL-16GB, X430 | MLB_CMNPTS, CPU:1.6GHZ, DDR3:ELPIDA_16GB            |
| 685-00043  | CMN PTS, PCBA, MLB, X430         | MLB_COMMON, J110_MLB                                |
| 685-00044  | VCORE FET, REN, X430             | VCORE_FET:REN                                       |
| 685-00045  | VCORE FET, VSHY, X430            | VCORE_FET:VSHY                                      |

## Alternate Parts

| PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:             |
|-------------|---------------------------|------------|---------|-----------------------|
| 685-00044   | 685-00045                 |            | ALL     | Removes alt to Vishay |

|          |          |  |     |                               |
|----------|----------|--|-----|-------------------------------|
| 333S0704 | 333S0700 |  | ALL | Elpidio CAN DRAM alt to Hynix |
|----------|----------|--|-----|-------------------------------|

## BOM Groups

|               |                                    |
|---------------|------------------------------------|
| BOM GROUP     | BOM OPTIONS                        |
| MLB_PROGPARTS | BOOTROM:PROG, SMC:PROG, TBTRM:PROG |

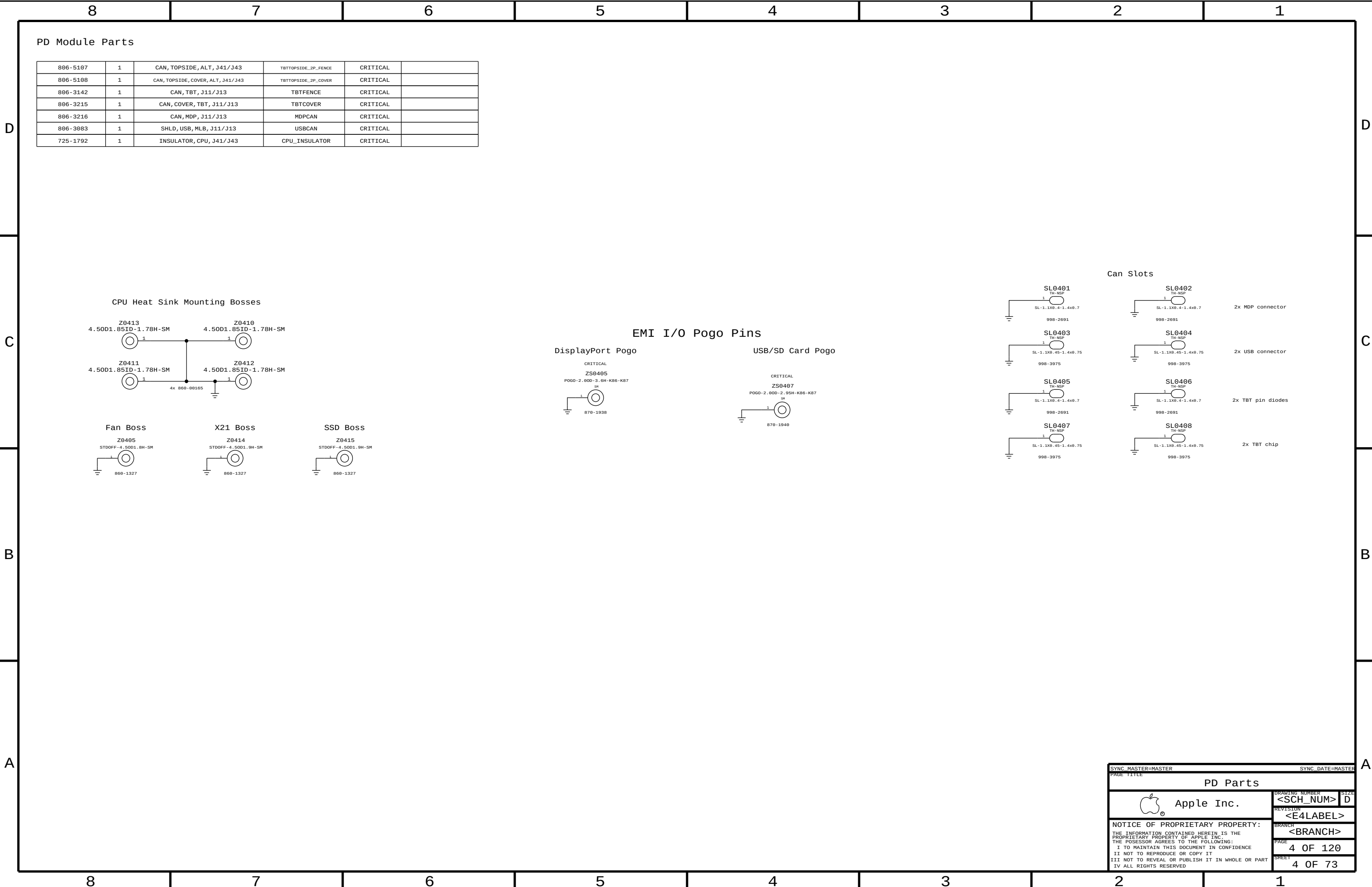
## Programmable Parts

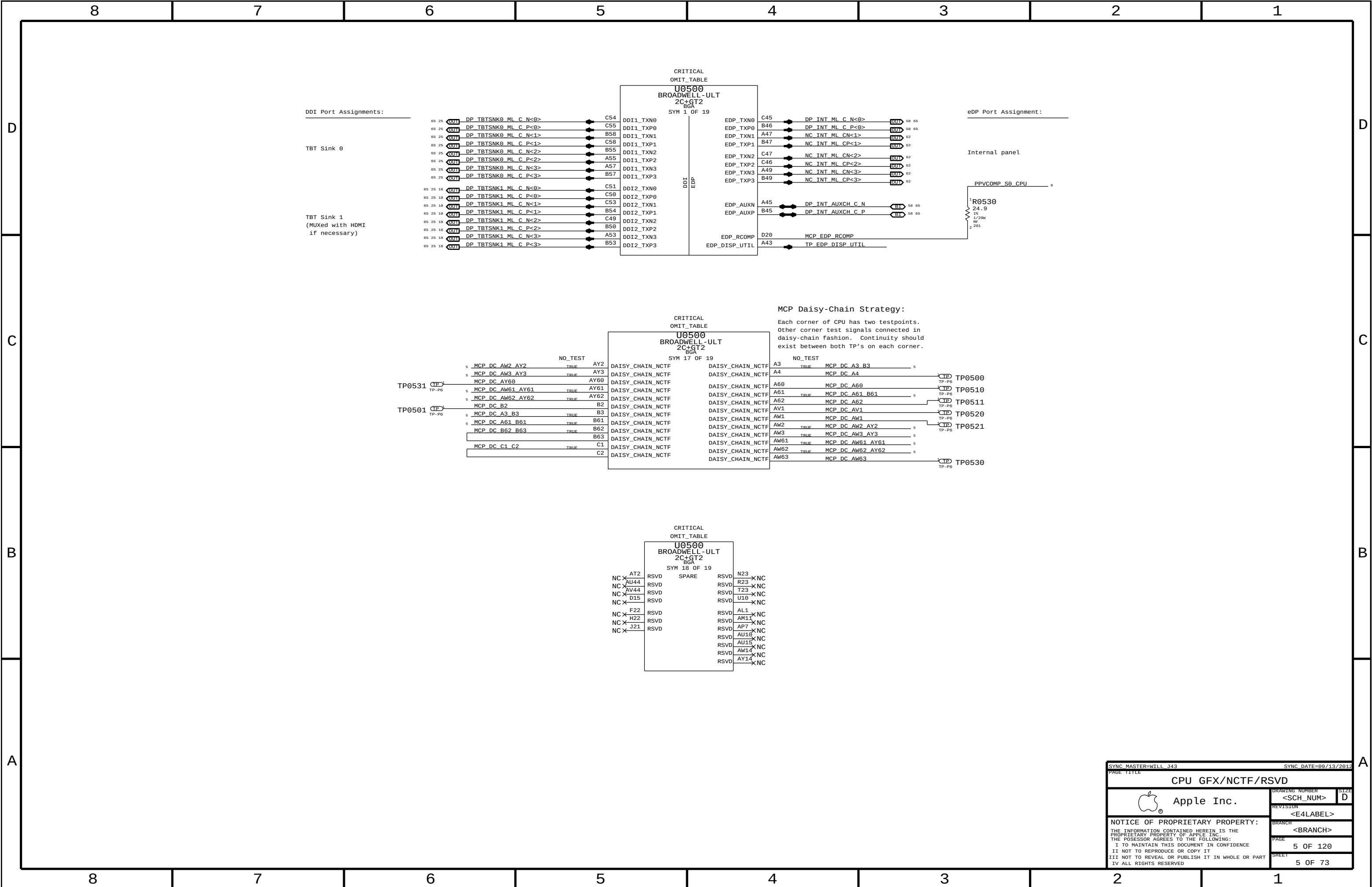
| PART NUMBER | QTY | DESCRIPTION                         | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-------------------------------------|---------------|----------|------------|
| 341S00147   | 1   | IC, SMC-A3,EXT, Vxxx, PROTO 0, 3110 | U5000         | CRITICAL | SMC:PROG   |

### Sub - BOMs

| PART NUMBER | QTY | DESCRIPTION           | REFERENCE DES | CRITICAL | BOM OPTION |
|-------------|-----|-----------------------|---------------|----------|------------|
| 685-00043   | 1   | CMN PTS,PCBA,MLB,J110 | CMNPTS        | CRITICAL | MLB_CMNPTS |
| 685-00045   | 1   | VCORE FET,VSHY,J110   | VCOREFETS     | CRITICAL | VCORE_FETS |

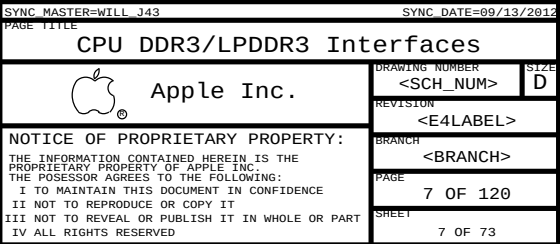
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| PAGE TITLE                                                                                                                                                                                                                                                                                                              |            |                  |                |
| BOM Variants                                                                                                                                                                                                                                                                                                            |            |                  |                |
|                                                                                                                                                                                                                                    | Apple Inc. |                  | DRAWING NUMBER |
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|                                                                                                                                                                                                                                                                                                                         |            |                  | SIZE           |
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|                                                                                                                                                                                                                                                                                                                         |            | PAGE             | 3 OF 120       |
|                                                                                                                                                                                                                                                                                                                         |            | SHEET            | 3 OF 73        |

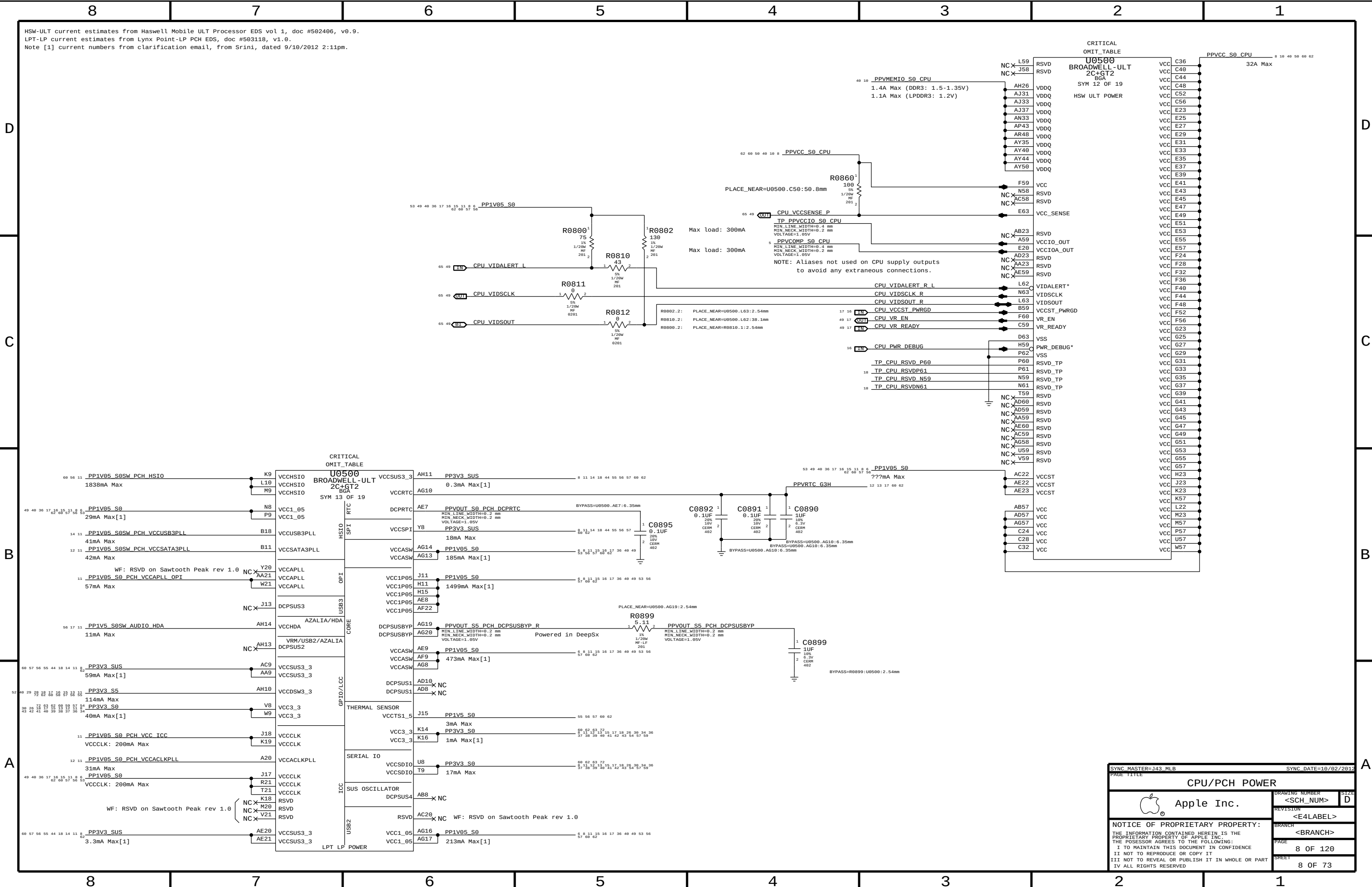






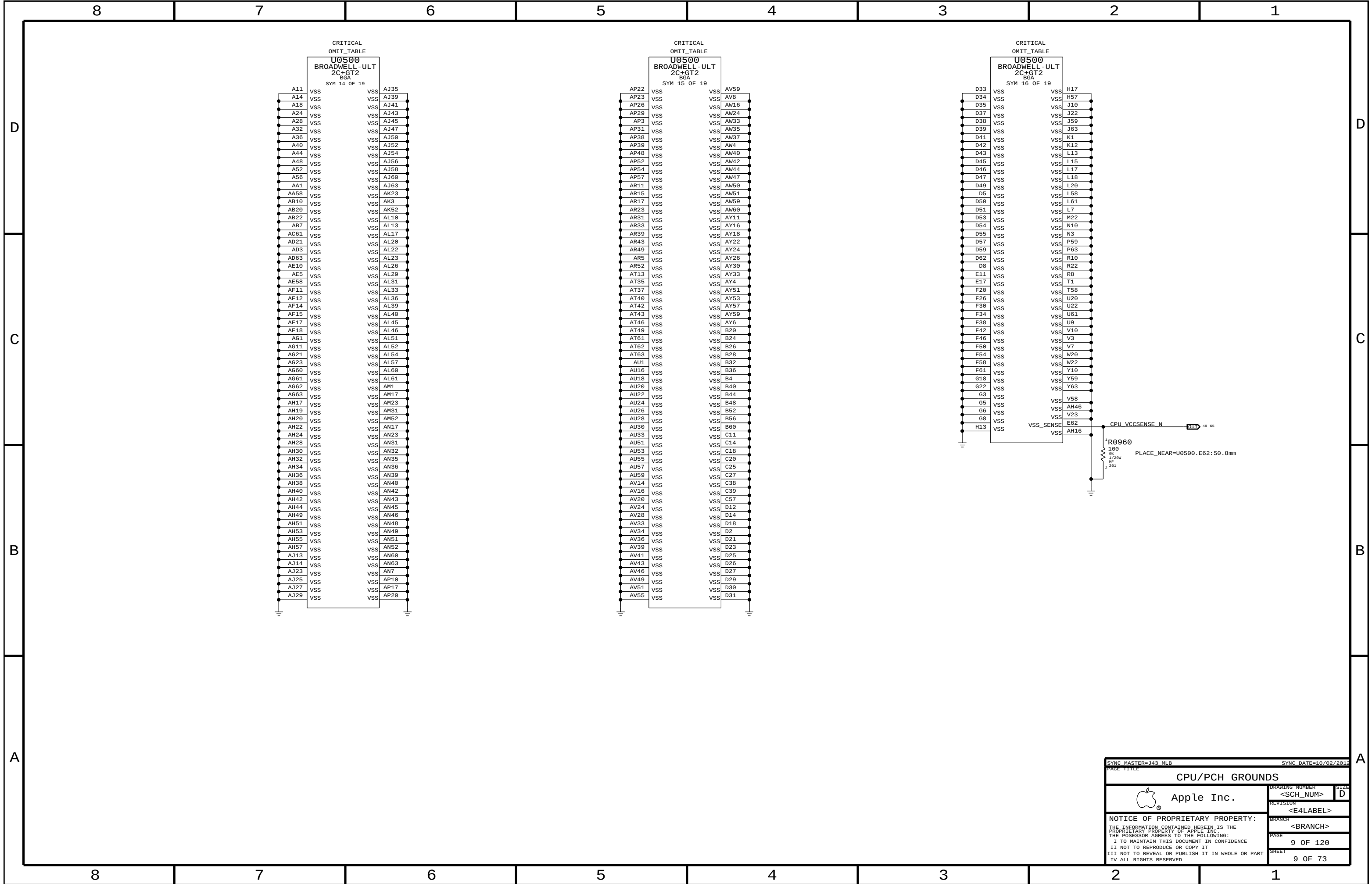


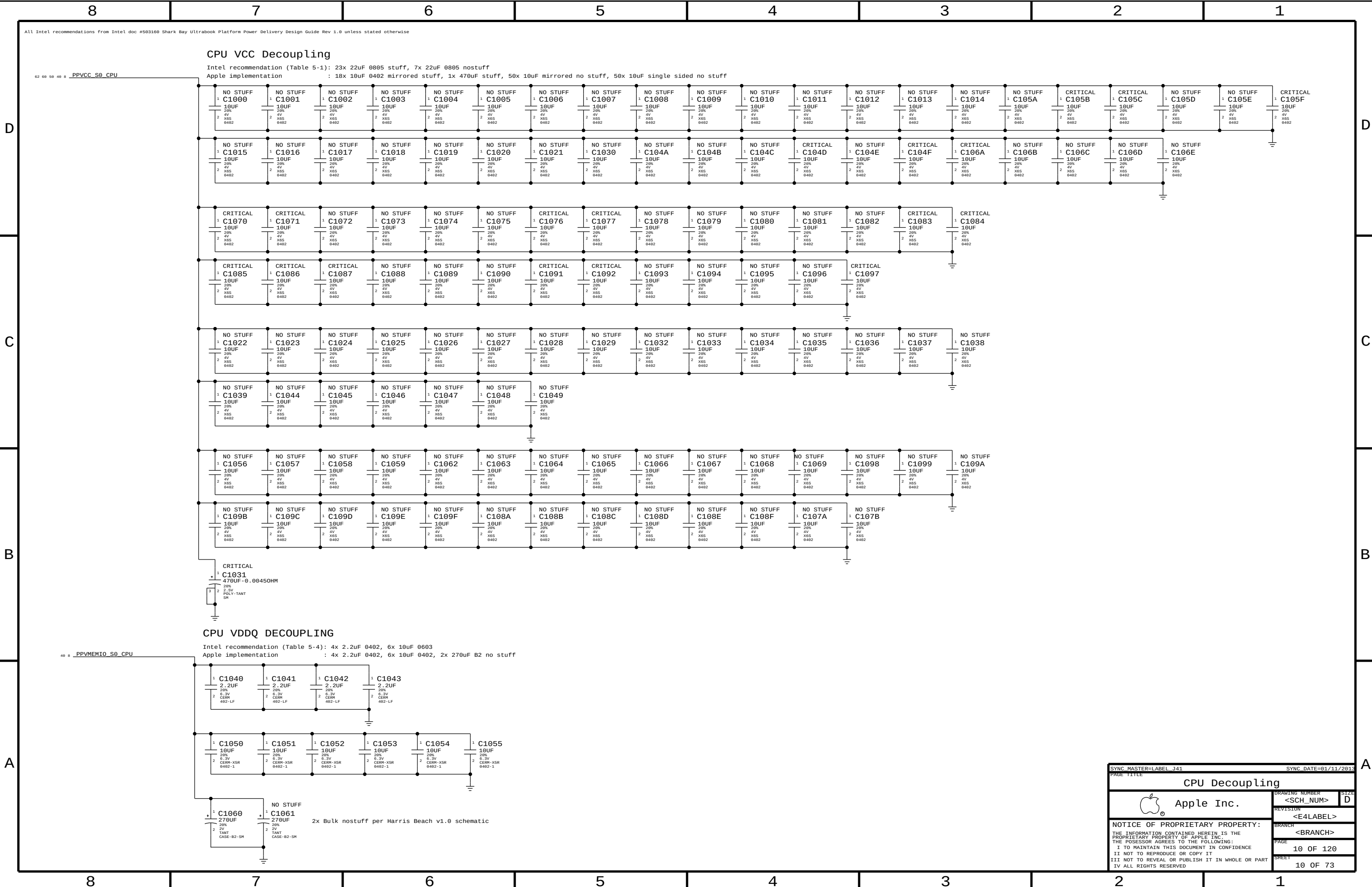




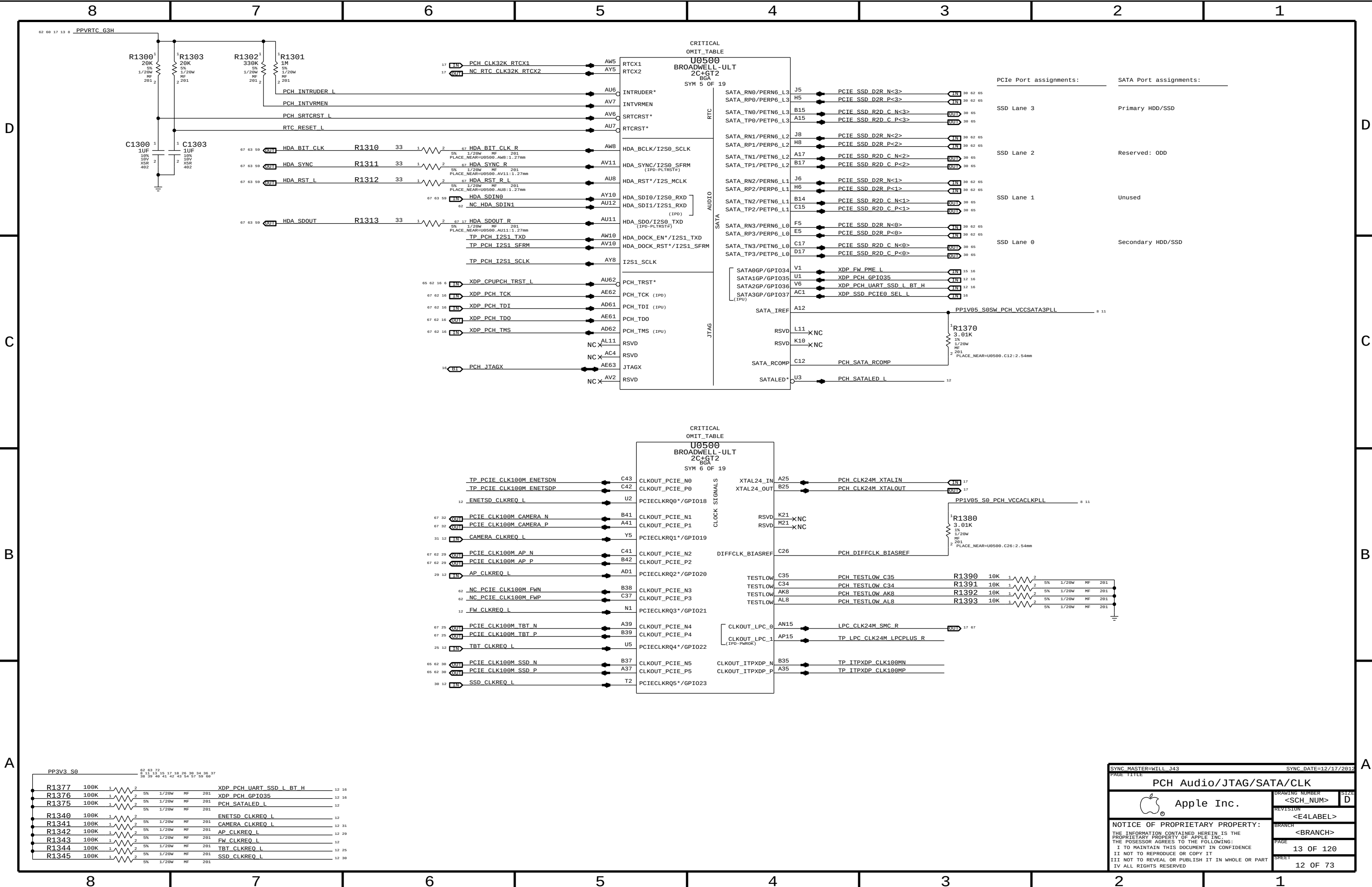
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|---------------------|--|----------------------|----------|
| SYNC MASTER=143 MLB |  | SYNC DATE=10/02/2012 |          |
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| Apple Inc.          |  | DRAWING NUMBER       | SIZE     |
|                     |  | <SCH_NUM>            | D        |
|                     |  | REVISION             |          |
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|                     |  | PAGE                 | 8 OF 120 |
|                     |  | SHEET                | 8 OF 73  |











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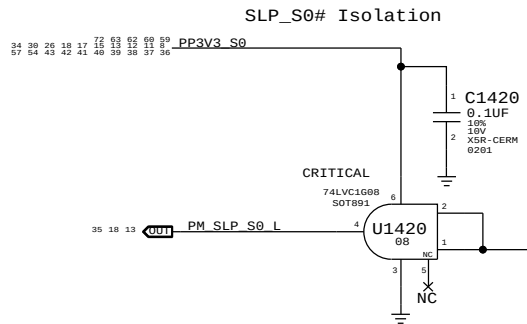
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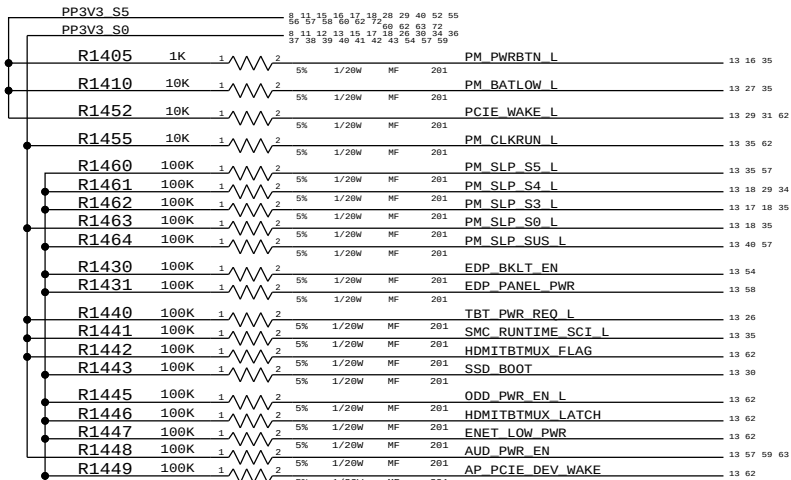
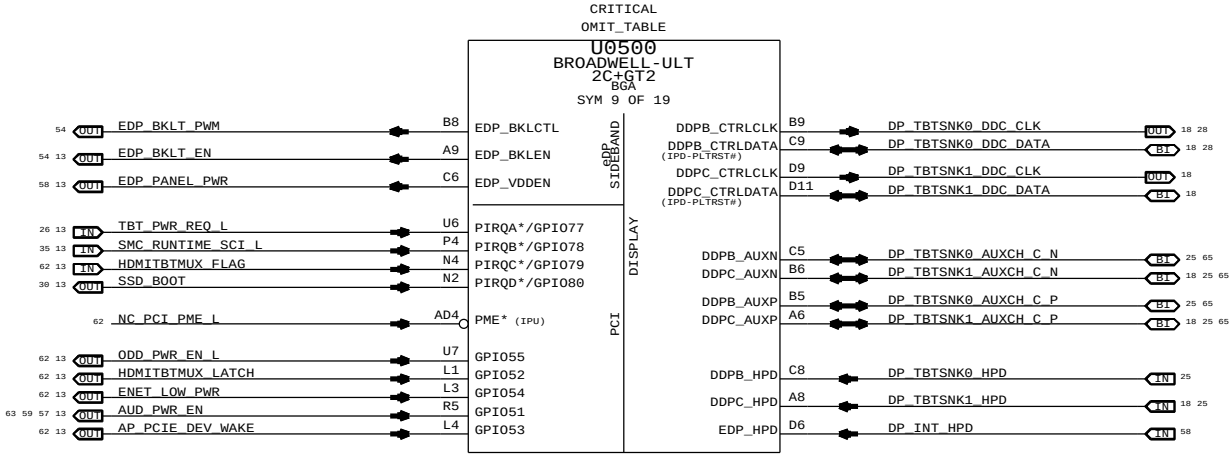
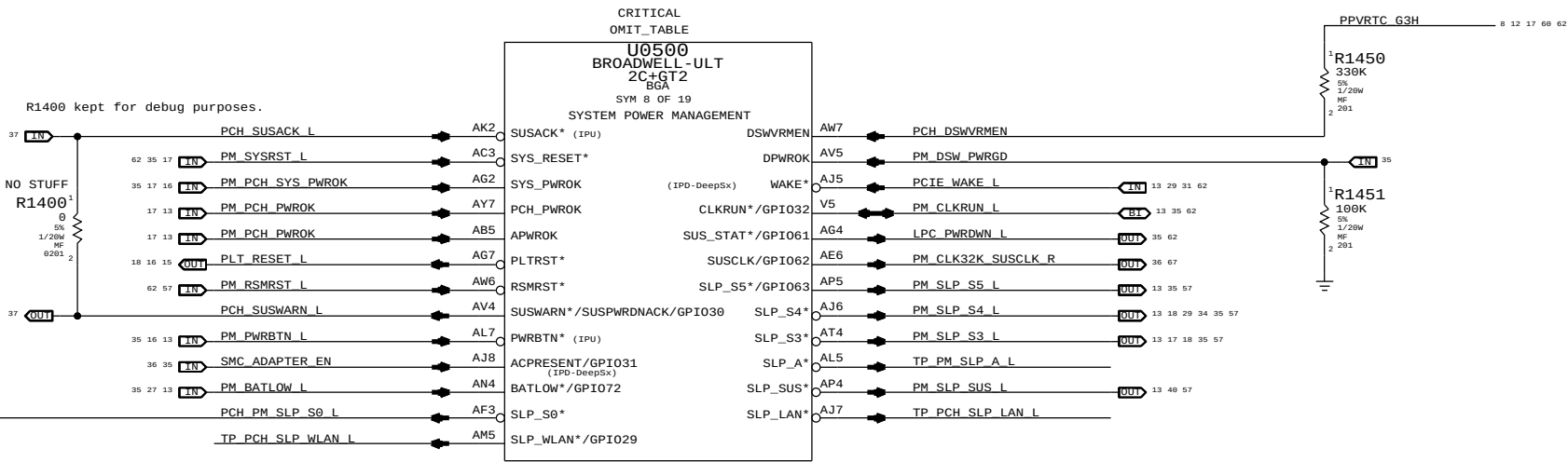
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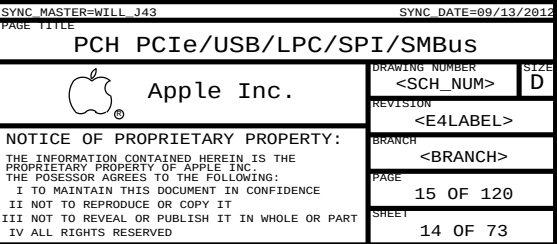
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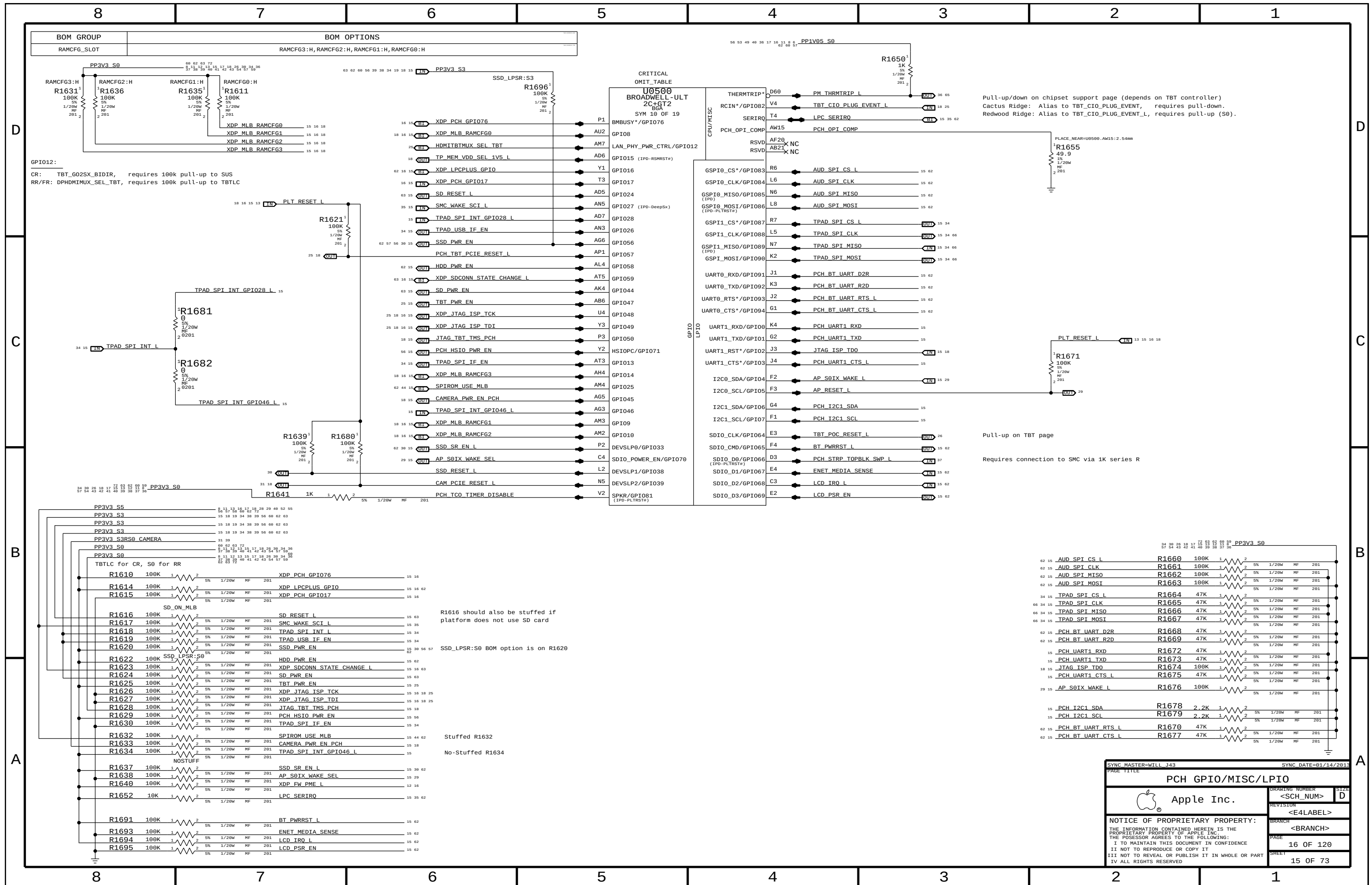
SLP\_S0# can be driven high outside of S0.  
U1420 ensures signal will only be high in S0.

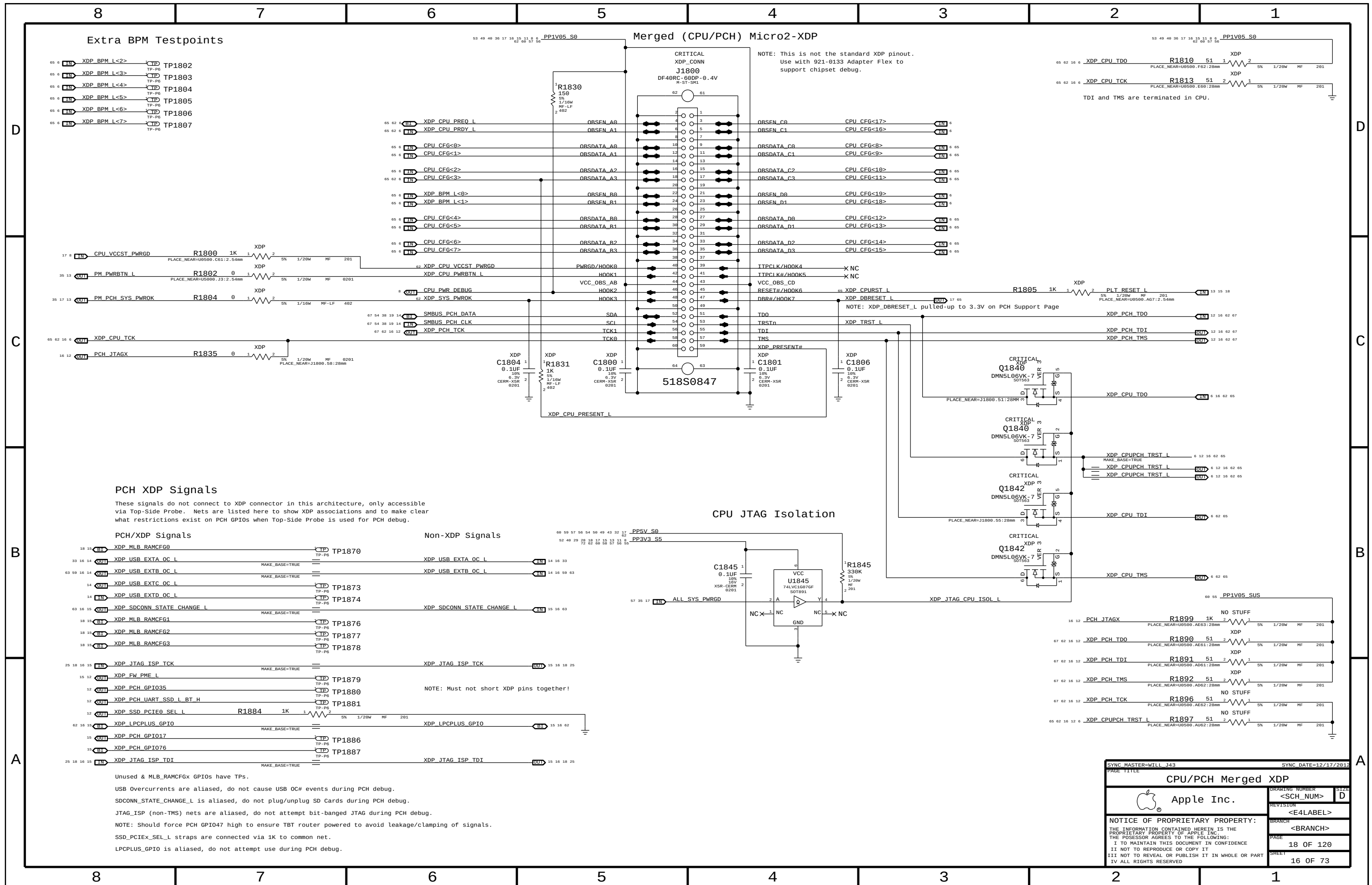


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| PCH PM/PCI/GFX                                                                                                    |  |                      |           |
| Apple Inc.                                                                                                        |  | DRAWING NUMBER       | SIZE      |
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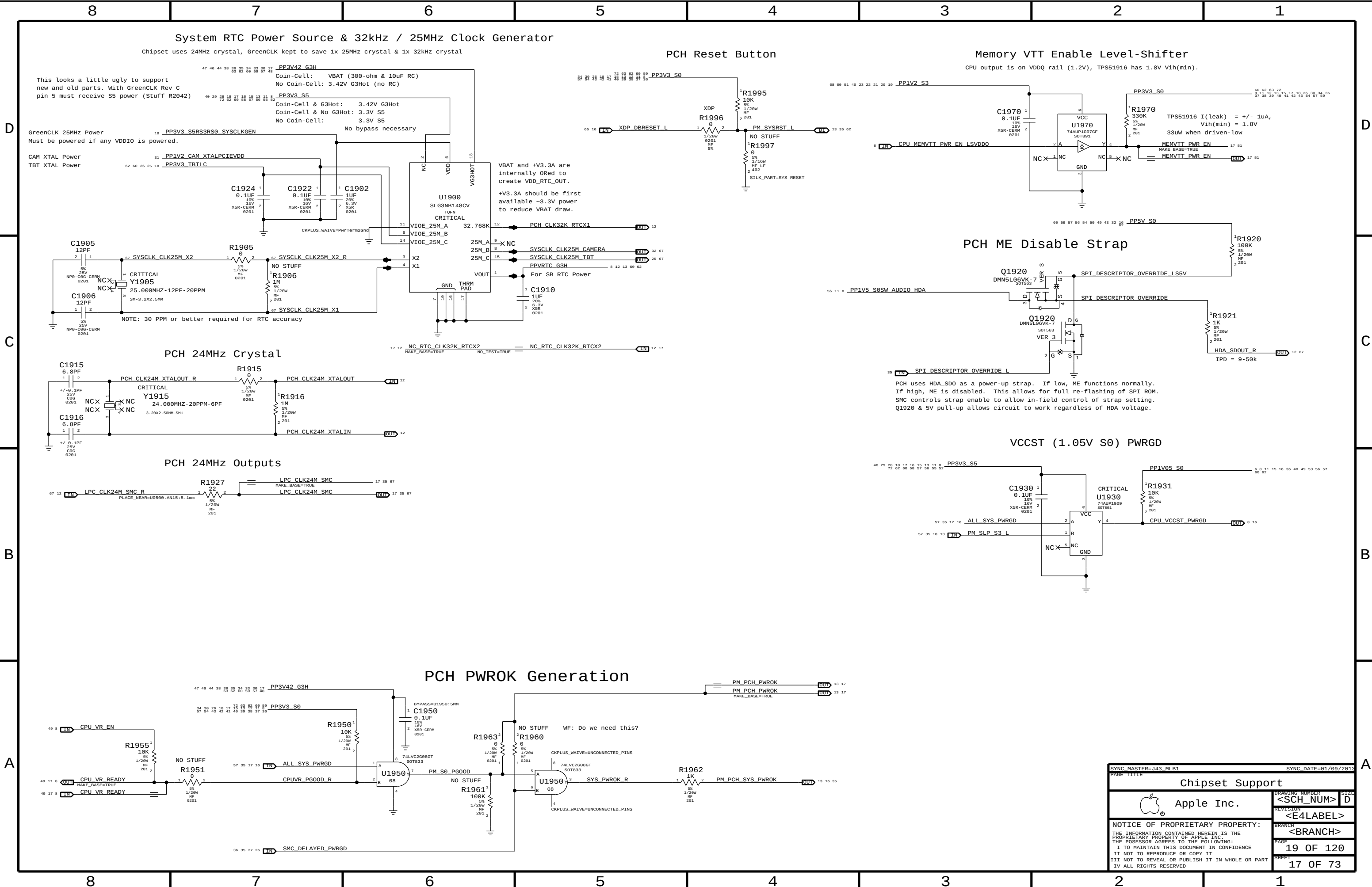




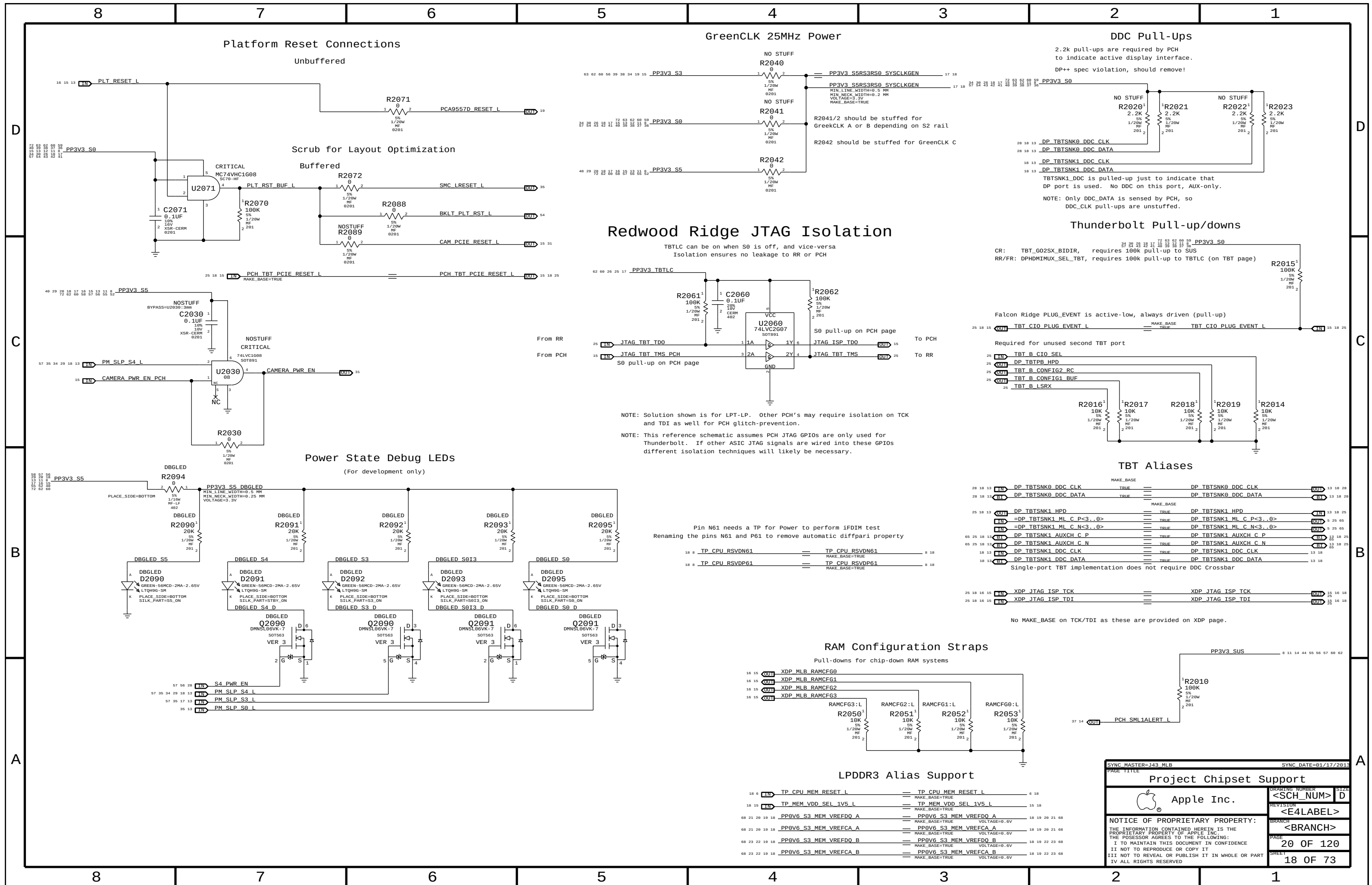








|                                                                                                                                                                                                                                                                                                                         |            |                      |           |
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| PAGE TITLE                                                                                                                                                                                                                                                                                                              |            |                      |           |
| Chipset Support                                                                                                                                                                                                                                                                                                         |            |                      |           |
|                                                                                                                                                                                                                                    | Apple Inc. | DRAWING NUMBER       | SIZE      |
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|                                                                                                                                                                                                                                                                                                                         |            | PAGE                 | 19 OF 120 |
|                                                                                                                                                                                                                                                                                                                         |            | SHEET                | 17 OF 73  |



Page Notes

Power aliases required by this page:

- =PP3V3\_S3\_VREFMRGN
- =PPDDR\_S3\_MEMVREF

Signal aliases required by this page:

- =I2C\_VREFDACS\_SCL
- =I2C\_VREFDACS\_SDA
- =I2C\_PCA9557D\_SCL
- =I2C\_PCA9557D\_SDA

BOM options provided by this page:

- DDRVREF\_DAC - Stuffs DAC margining circuit.

CPU-Based Margining

FETs for CPU isolation during DAC margining

NOTE: CPU DAC output step sizes:  
DDR3 (1.5V) 7.70mV per step  
DDR3L (1.35V) 6.99mV per step  
LPDDR3 (1.2V) 7.77mV per step

NOTE: CPU has single output for VREFCA. Split into two signals for independent DAC margining support. When DAC margining VREFCA ensure VREFMRGN\_CPU\_EN is low to remove short due to CPU.

DAC-Based Margining

DAC sets voltage level, PCA9557 & FETs enable outputs and disables margining after platform reset.

OMIT

PP3V3\_S3

R2218 SHORT

PP3V3\_S3\_VREFMRGN\_DAC

DDRREF\_DAC C2200 2.2UF

DDRREF\_DAC C2201 0.1UF

SMBUS\_PCH\_CLK

SMBUS\_PCH\_DATA

Addr=0x98(WR)/0x99(RD)

VDD

VOUTA

VOUTB

VOUTC

VOUTD

GND

NOTE: MEMVREG and SPARE share a DAC output, cannot enable both at the same time!

DDRREF\_DAC C2202 0.1UF

CRITICAL DDRREF\_DAC

U2201 PCA9557

Addr=0x30(WR)/0x31(RD)

SMBUS\_PCH\_CLK

SMBUS\_PCH\_DATA

PCA9557D\_RESET\_L

RST\* on 'platform reset' so that system watchdog will disable margining.

NOTE: Margining will be disabled across all soft-resets and sleep/wake cycles.

VRef Dividers

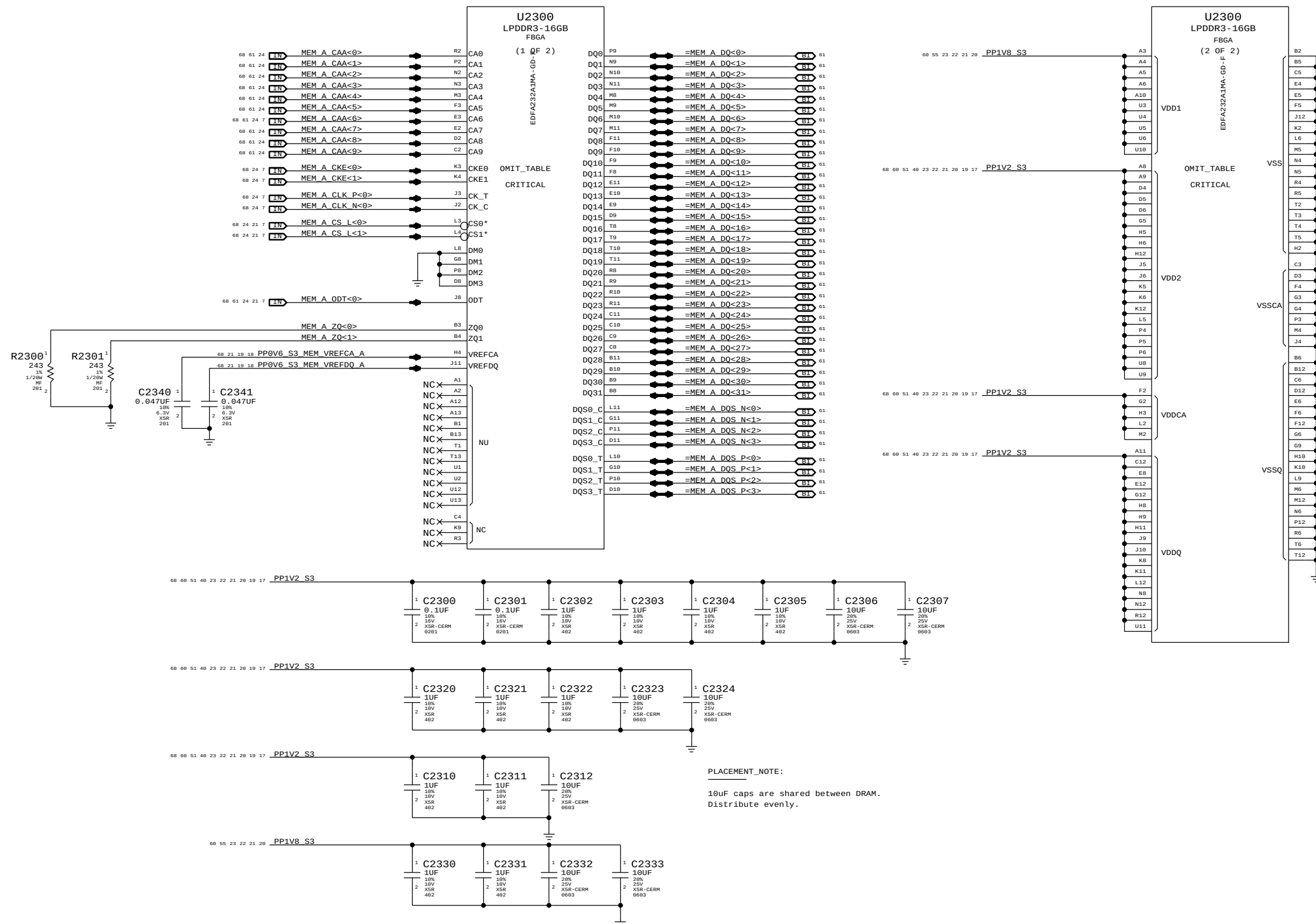
Always used, regardless of margining option.

|                  | MEM A VREF DQ                         | MEM B VREF DQ | MEM A VREF CA                       | MEM B VREF CA | MEM VREG                            |
|------------------|---------------------------------------|---------------|-------------------------------------|---------------|-------------------------------------|
| DAC Channel:     | A                                     | B             | C                                   | C             | D                                   |
| PCA9557D Pin:    | 1                                     | 2             | 3                                   | 4             | 5                                   |
| Nominal value    | LPDDR3 (1.2V)<br>0.600V (DAC: 0x2E.5) |               | DDR3L (1.35V)<br>0.675V (DAC: 0x34) |               | LPDDR3 (1.2V)<br>1.200V (DAC: 0x5D) |
| Margined target: | 0.300V - 0.900V (+/- 300mV)           |               | 0.337V - 1.013V (+/- 337.5mV)       |               | 0.800V - 1.600V (+/- 400mV)         |
| DAC range:       | 0.000V - 1.199V (0x00 - 0x5D)         |               | 0.000V - 1.354V (0x00 - 0x69)       |               | 0.000V - 2.397V (0x00 - 0xBA)       |
| VRef current:    | +73uA - -73uA (- = sourced)           |               | +82uA - -82uA (- = sourced)         |               | +25uA - -25uA (- = sourced)         |
| DAC step size:   | 6.36mV / step @ output                |               | 6.36mV / step @ output              |               | 4.28mV / step @ output              |

NOTE: LPDDR3 assumes TPS51916 supply with 28.7k/57.6k divider  
DDR3L assumes TPS51916 supply with 19.6k/57.6k divider

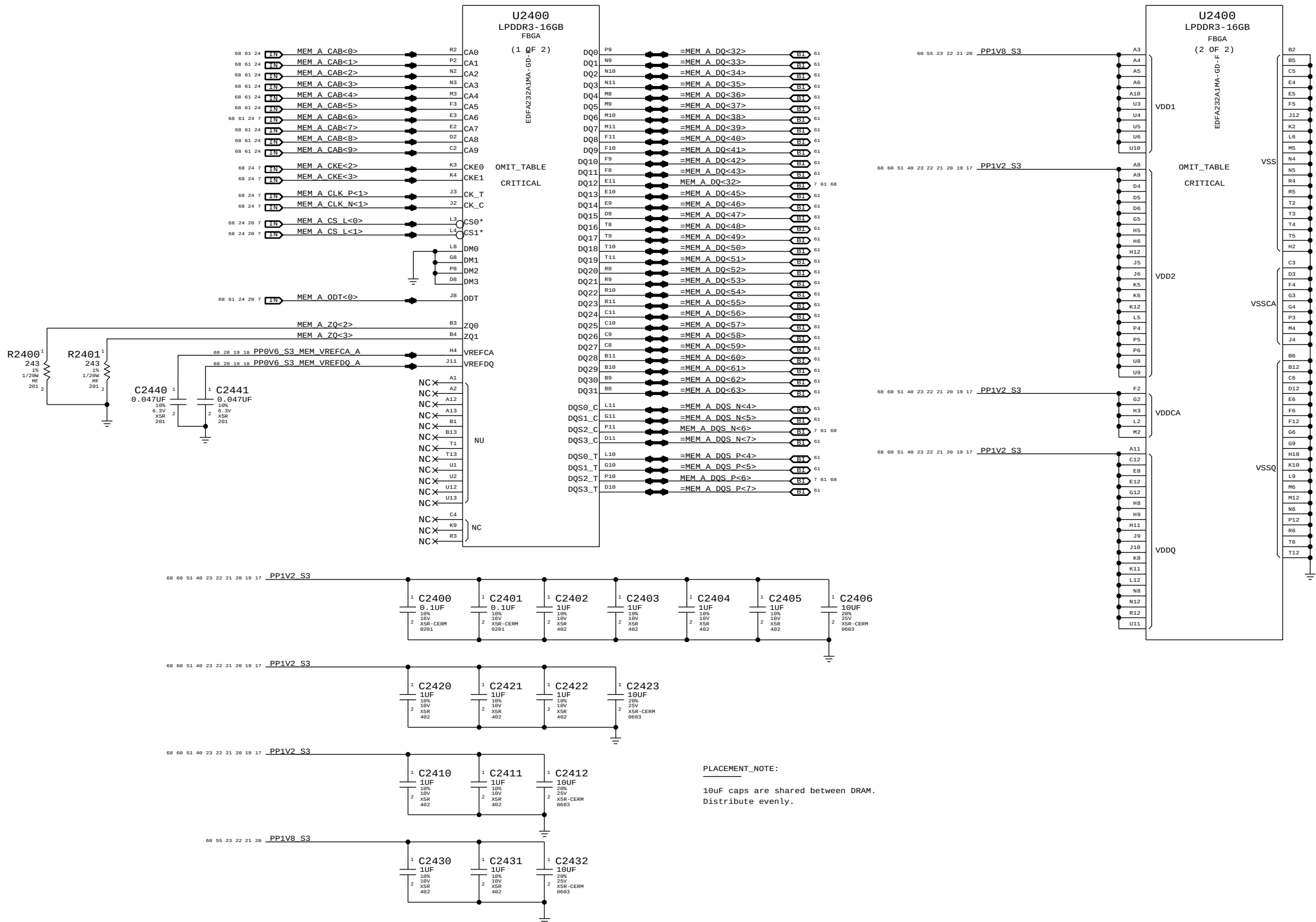
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| PAGE TITLE                                                                                                                                                                                                                                                                                                        |  | DDR3 VREF MARGINING  |           |
| Apple Inc.                                                                                                                                                                                                                                                                                                        |  | DRAWING NUMBER       | SIZE      |
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|                                                                                                                                                                                                                                                                                                                   |  | PAGE                 | 22 OF 120 |
|                                                                                                                                                                                                                                                                                                                   |  | SHEET                | 19 OF 73  |
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## LPDDR3 CHANNEL A (0-31)

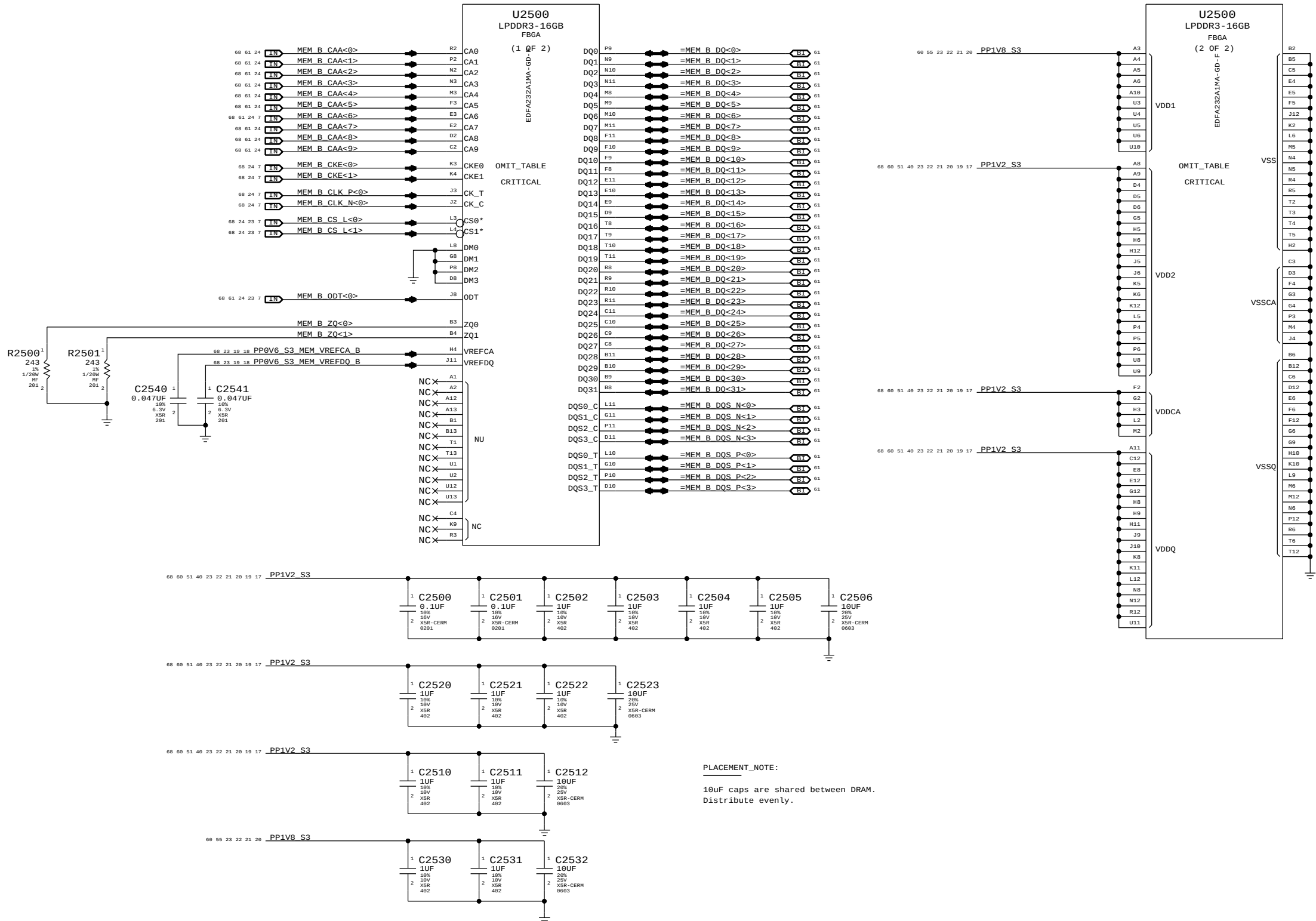


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| SYMC MASTER=MASTER                                                                                                                                                                                                                                                                   |                | SYMC DATE=MASTER                  |                                   |
| PAGE TITLE                                                                                                                                                                                                                                                                           |                |                                   |                                   |
| LPDDR3 DRAM Channel A (0-31)                                                                                                                                                                                                                                                         |                |                                   |                                   |
| <br>Apple Inc.                                                                                                                                                                                  | DRAWING NUMBER | SIZE                              |                                   |
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# LPDDR3 CHANNEL A (32-63)

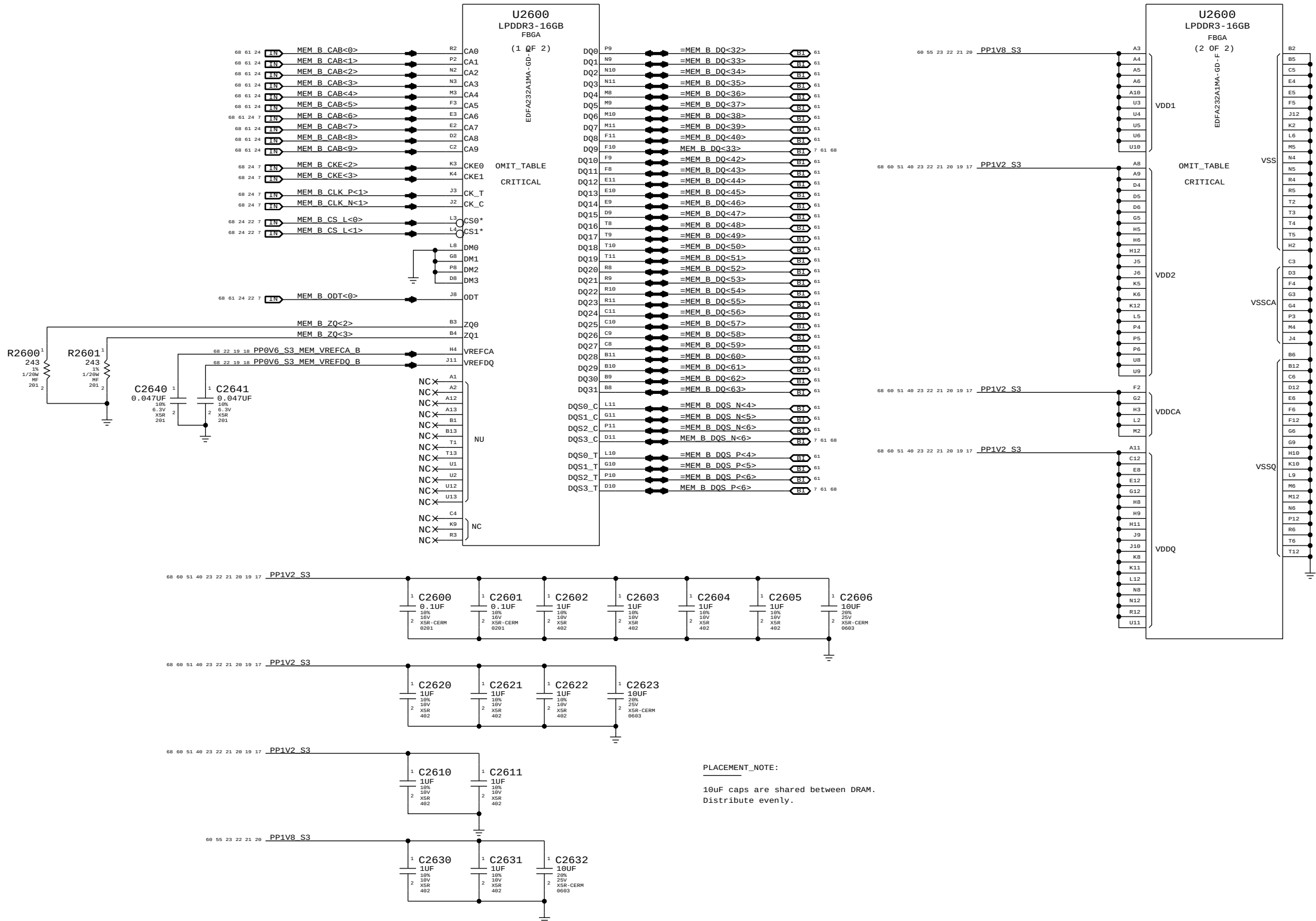


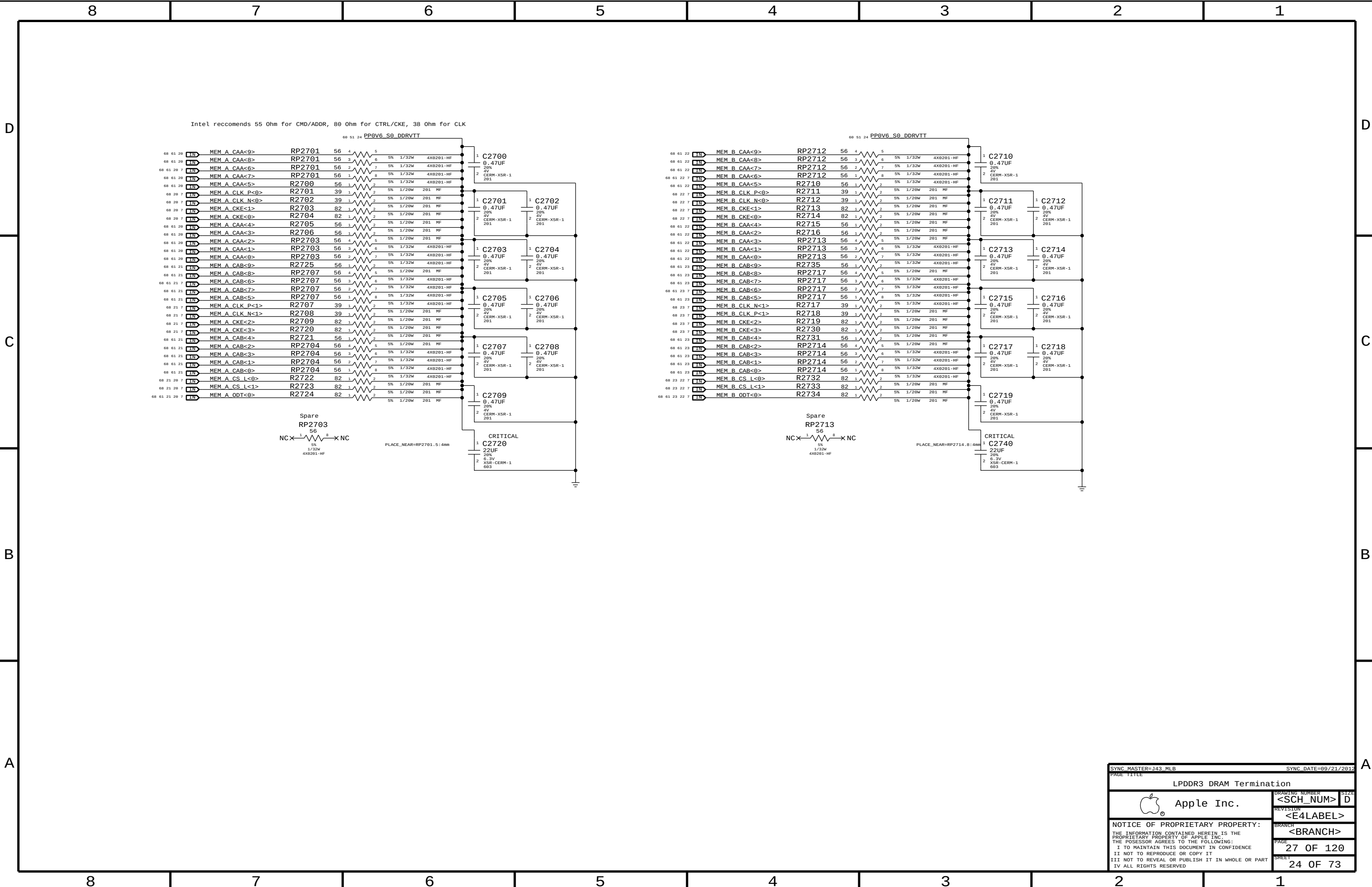
# LPDDR3 CHANNEL B (0-31)



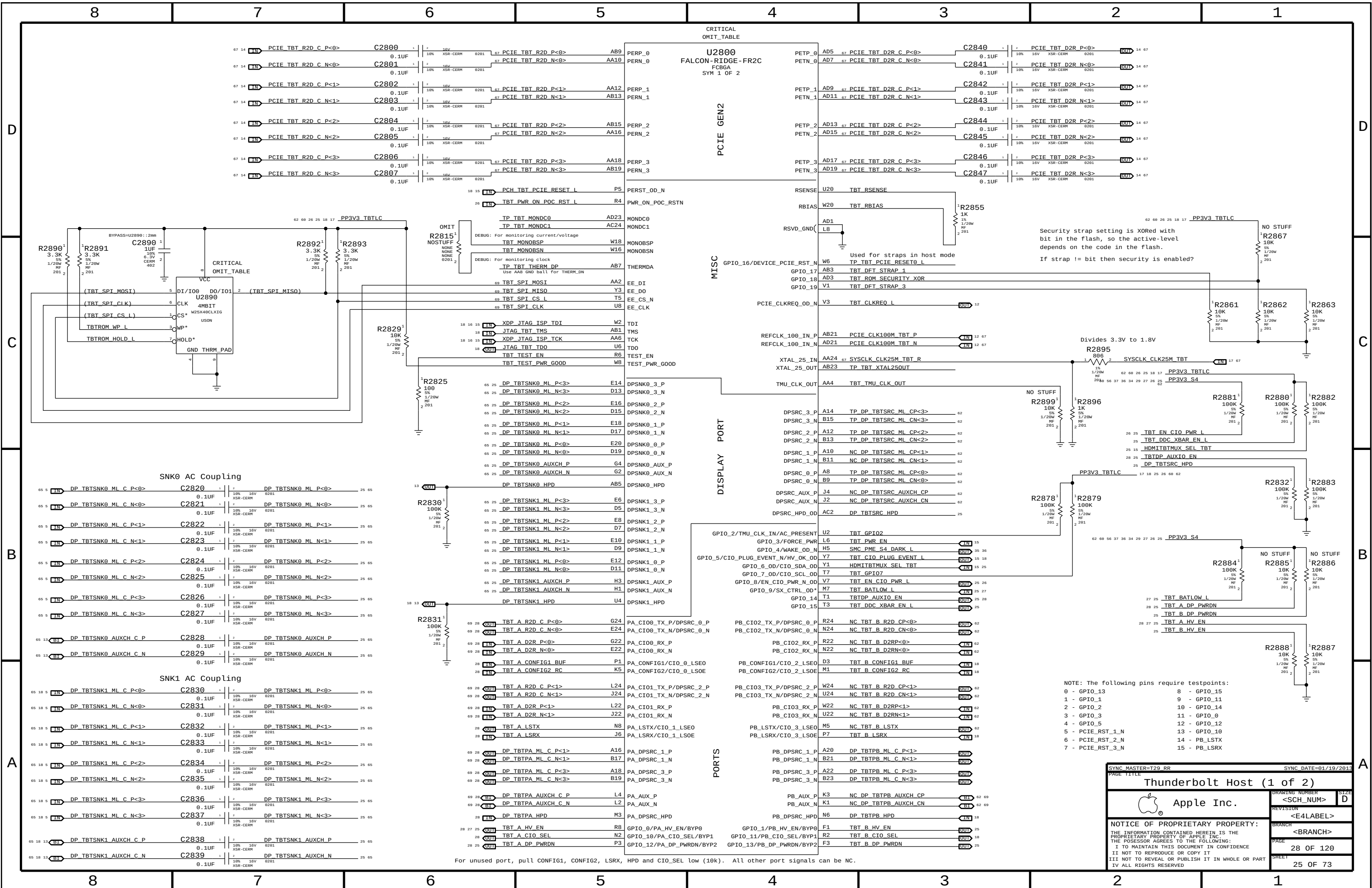


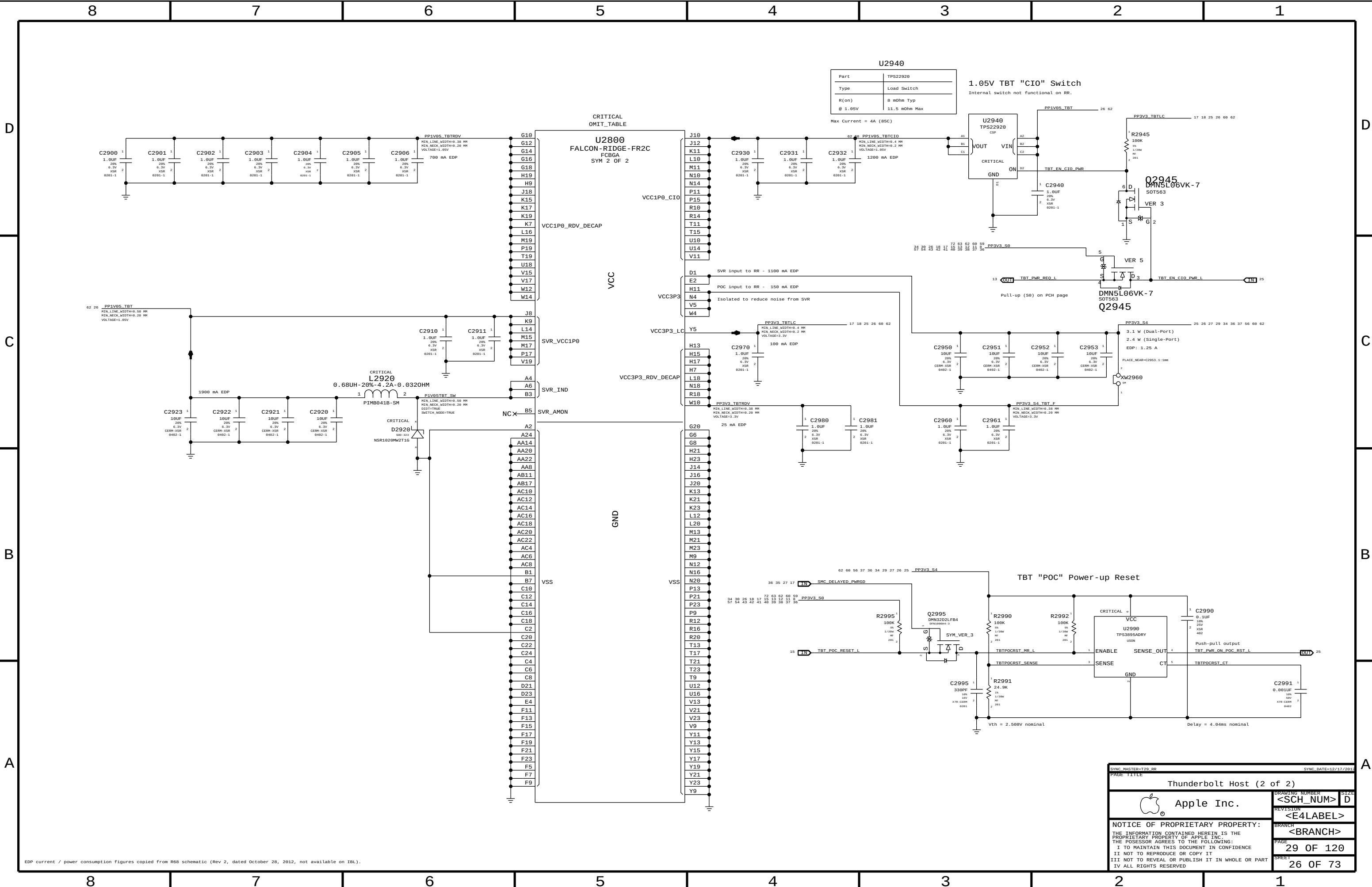
LPDDR3 CHANNEL B (32-63)











EDP current / power consumption figures copied from R68 schematic (Rev 2, dated October 28, 2012, not available on IBL).

SYNC MASTER=T20\_RR

SYNC DATE=12/17/2015

Thunderbolt Host (2 of 2)

Apple Inc.

DRAWING NUMBER

<SCH\_NUM>

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REVISION

<E4LABEL>

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BRANCH

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PAGE

29 OF 120

SHEET

26 OF 73

D

C

B

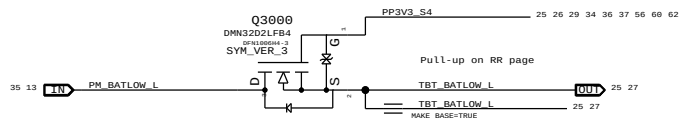
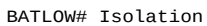
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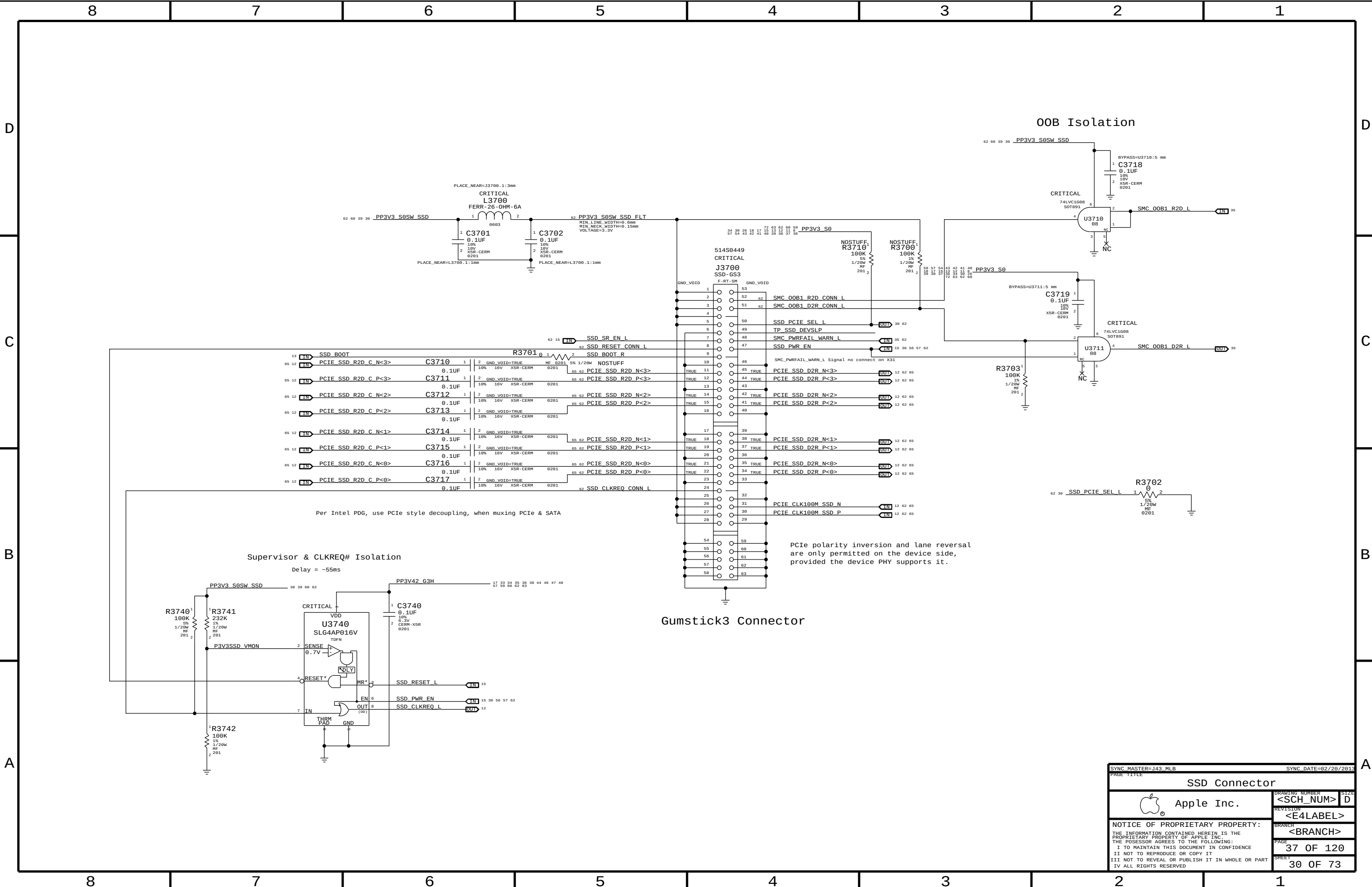
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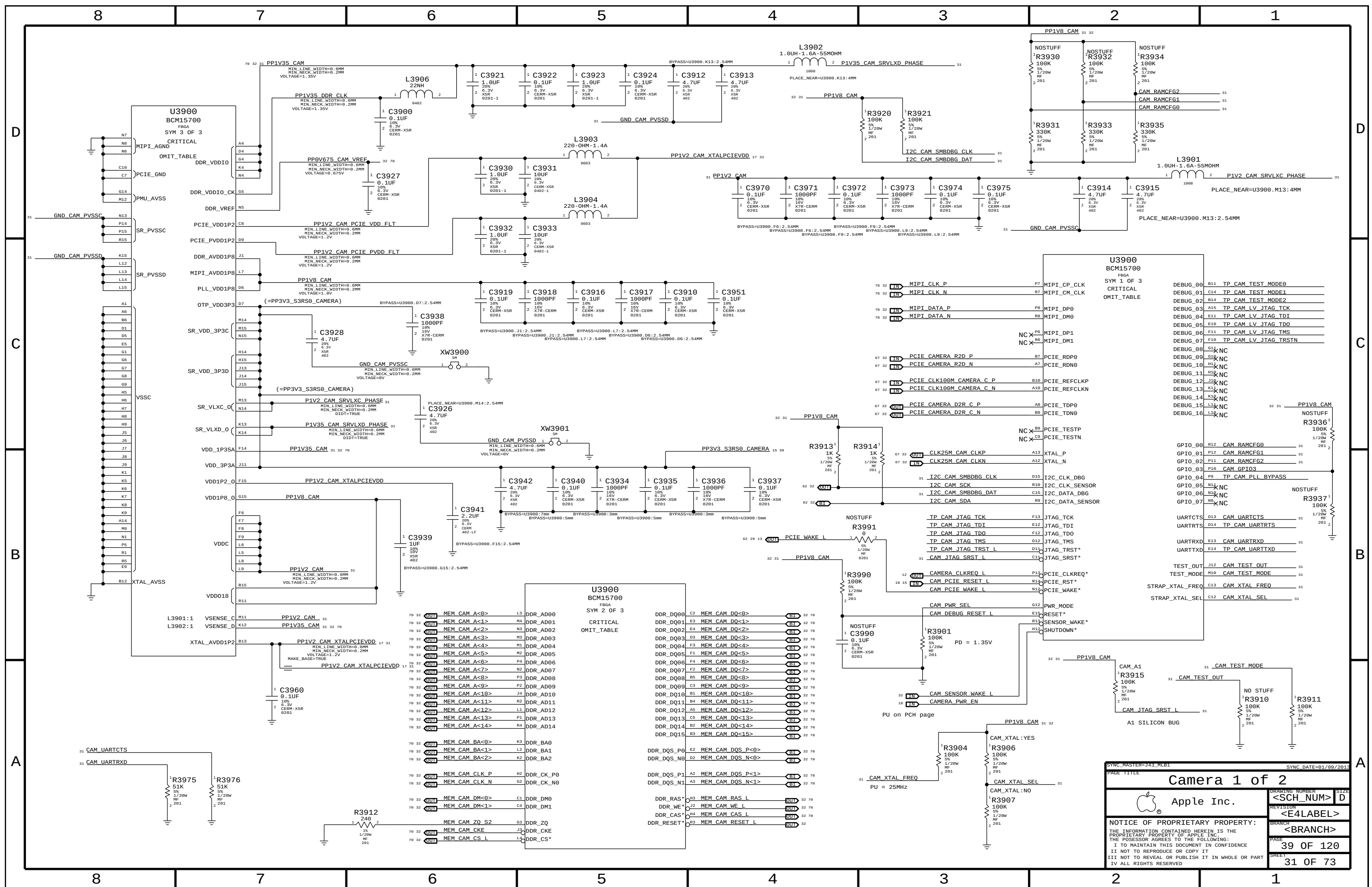


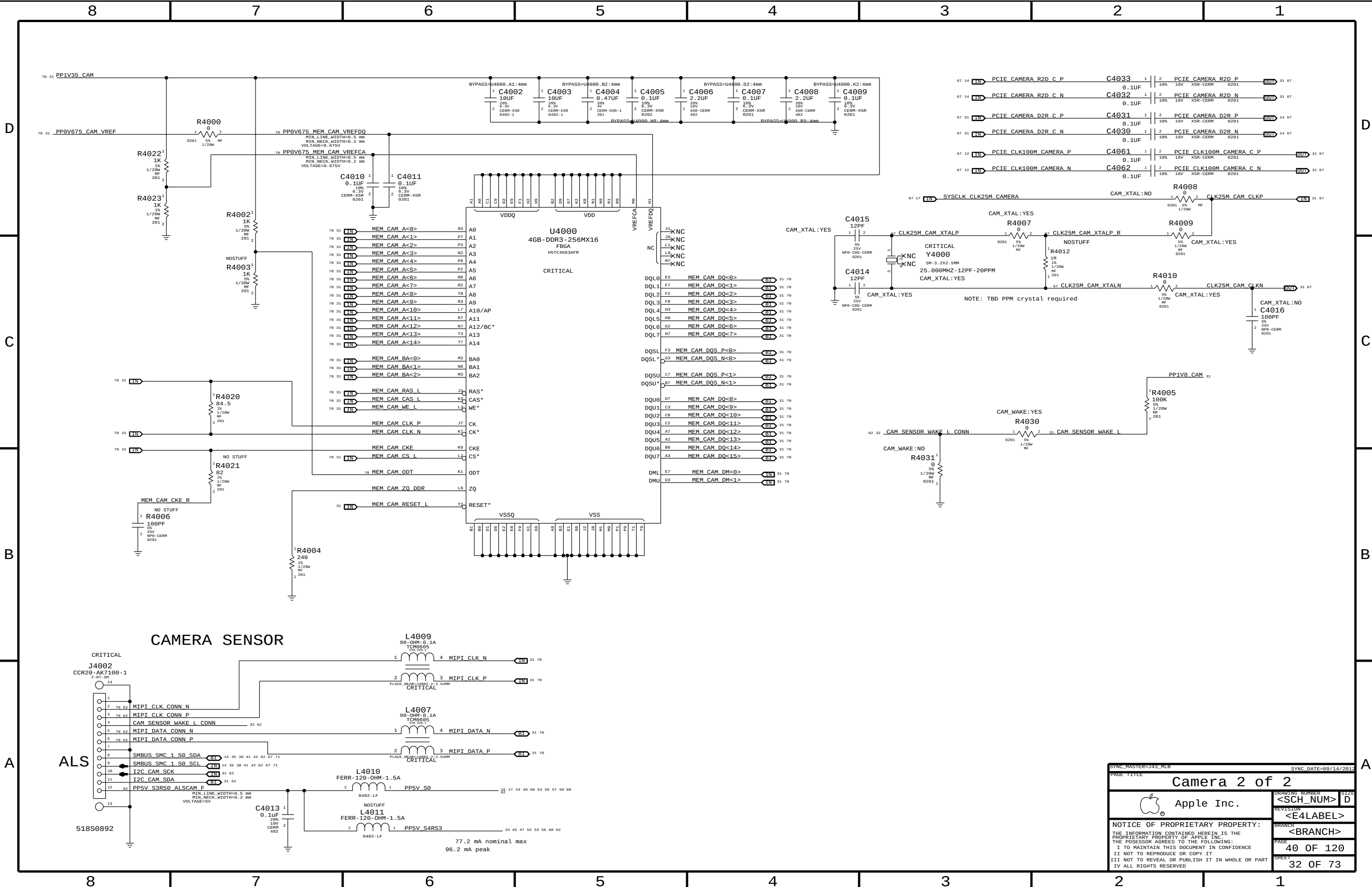




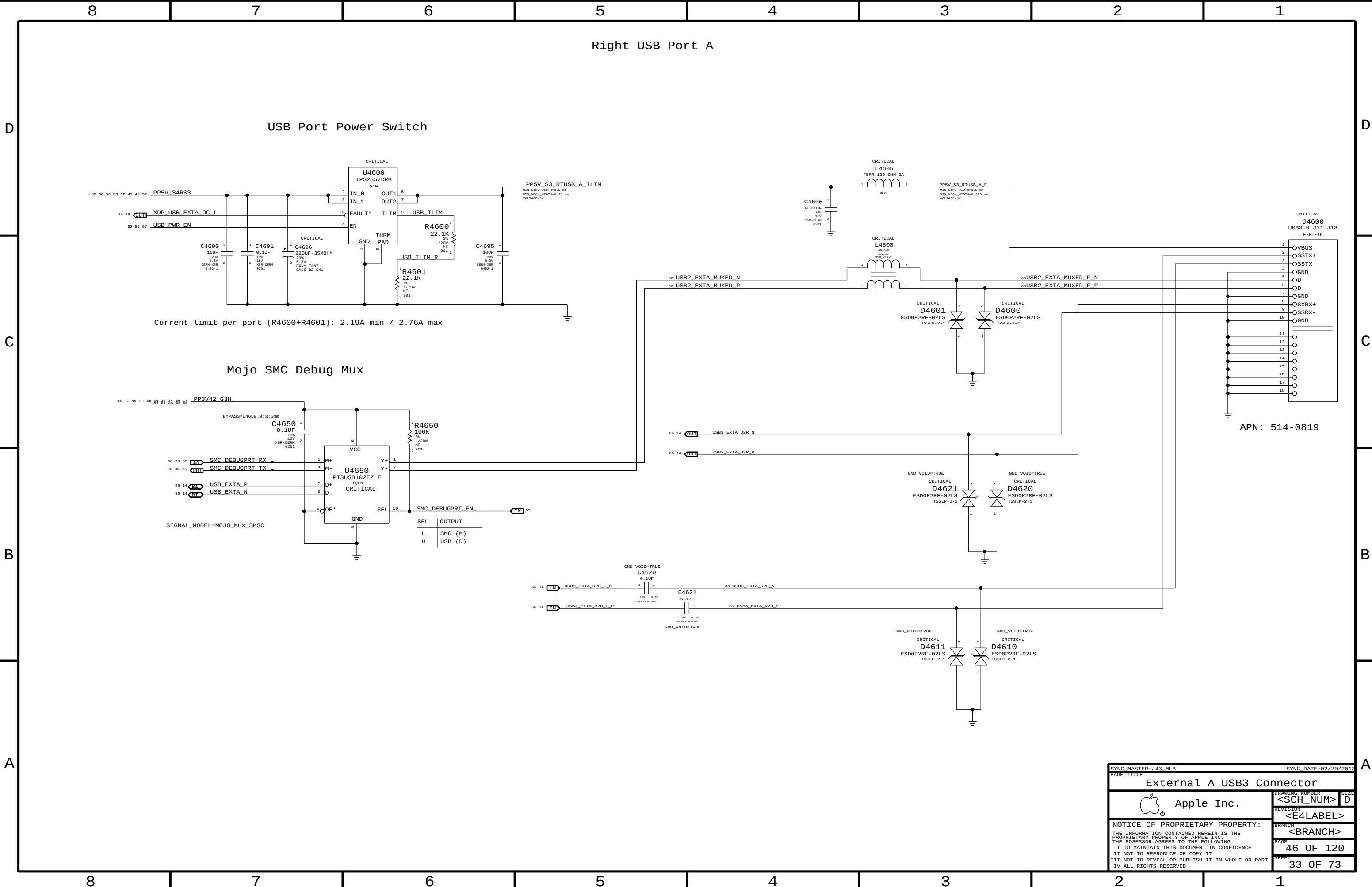


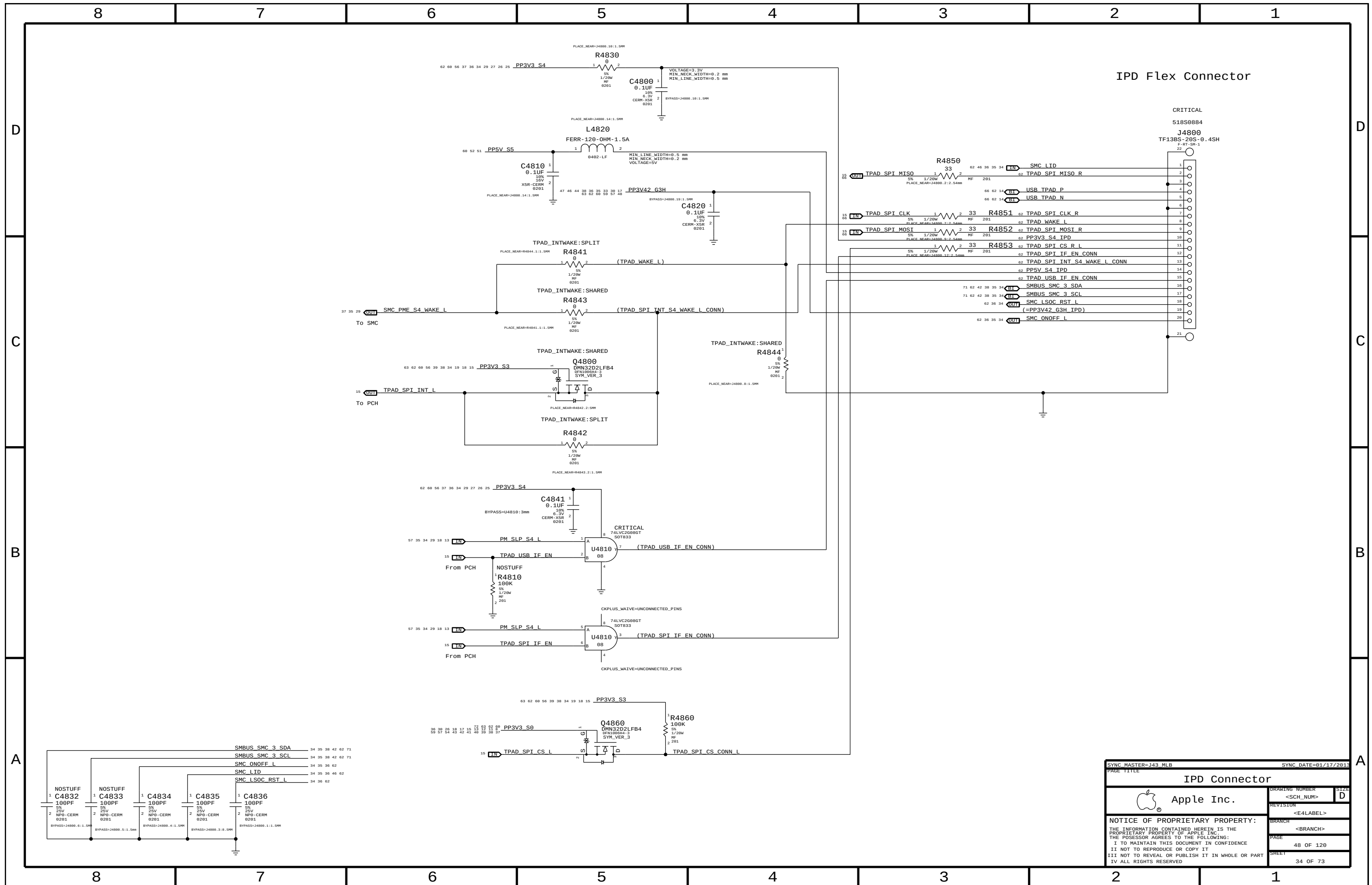


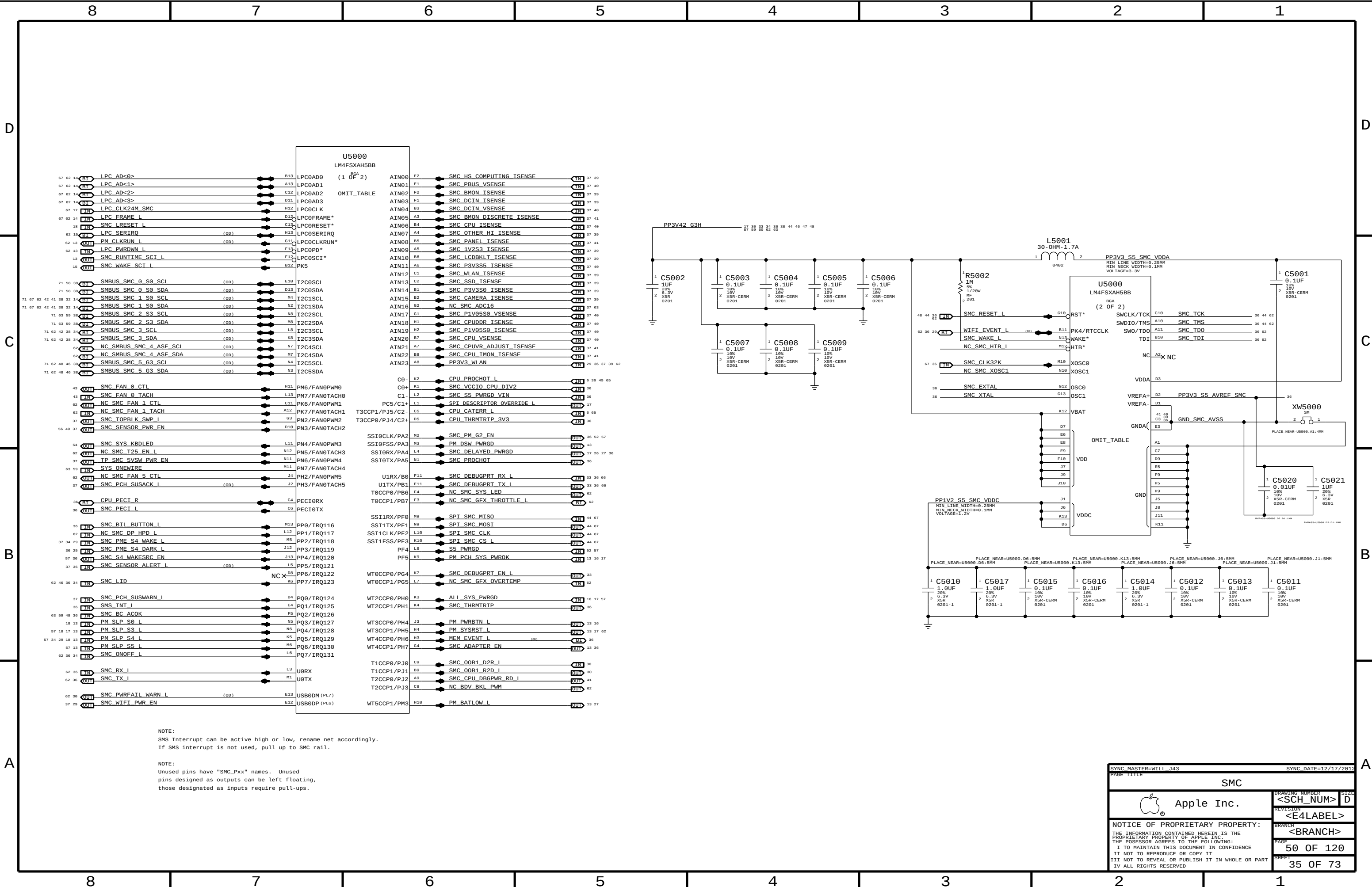












NOTE:  
SMS Interrupt can be active high or low, rename net accordingly.  
If SMS interrupt is not used, pull up to SMC rail.

NOTE:  
Unused pins have "SMC\_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.

SYNC MASTER=WILL\_343

SYNC DATE=12/17/2012

PAGE TITLE

SMC

 Apple Inc.

DRAWING NUMBER

<SCH\_NUM>

SIZE

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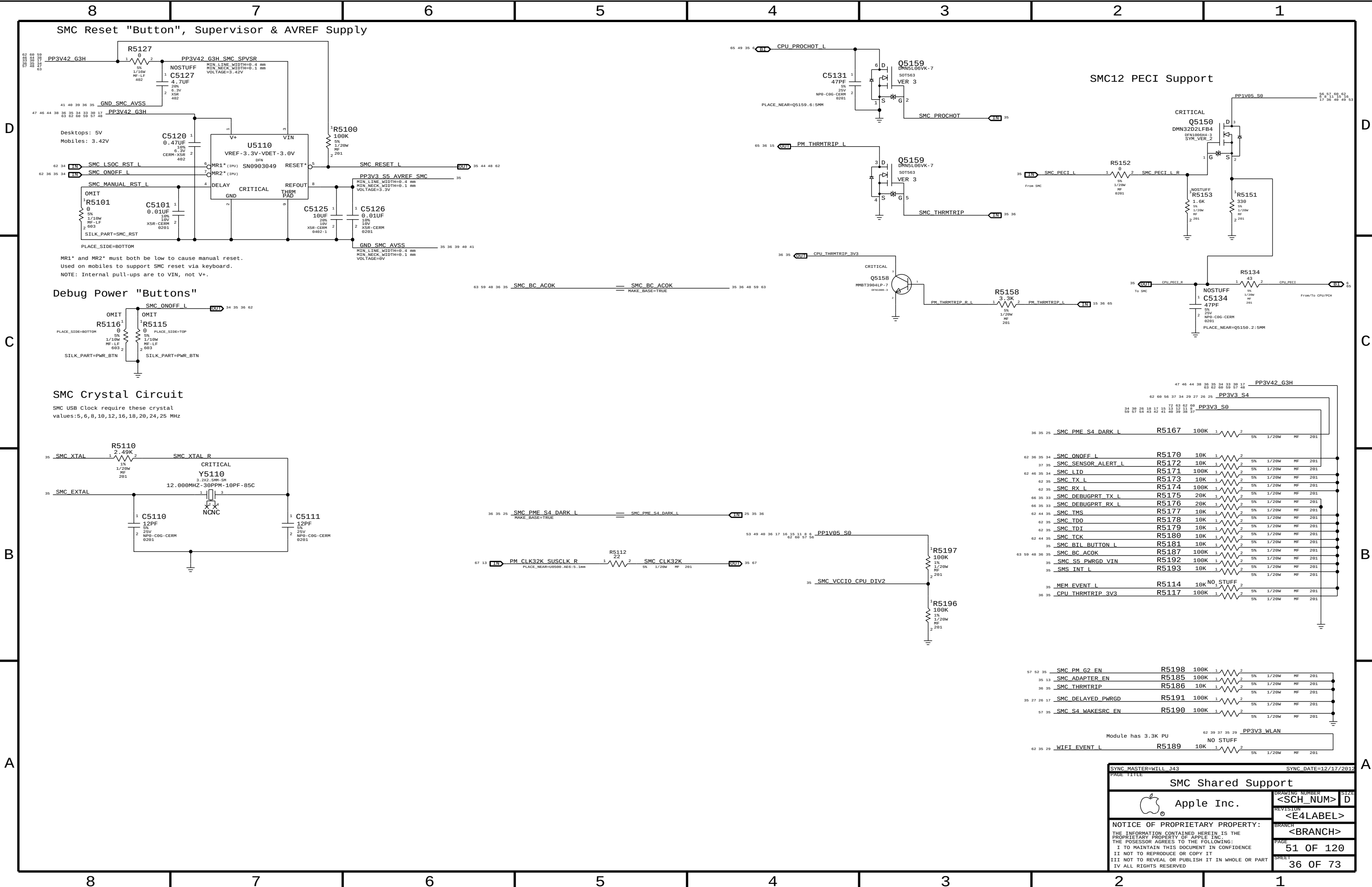
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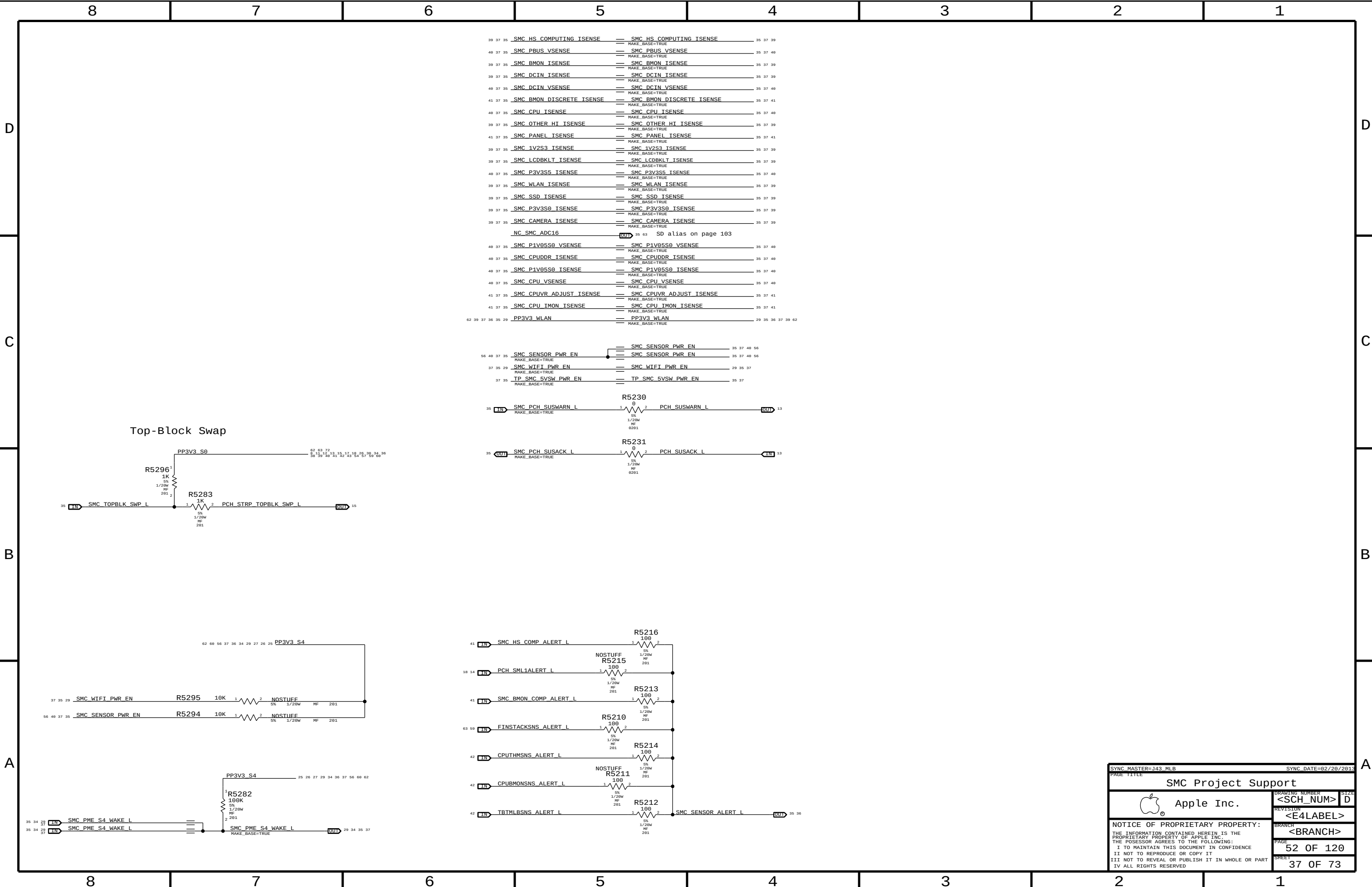
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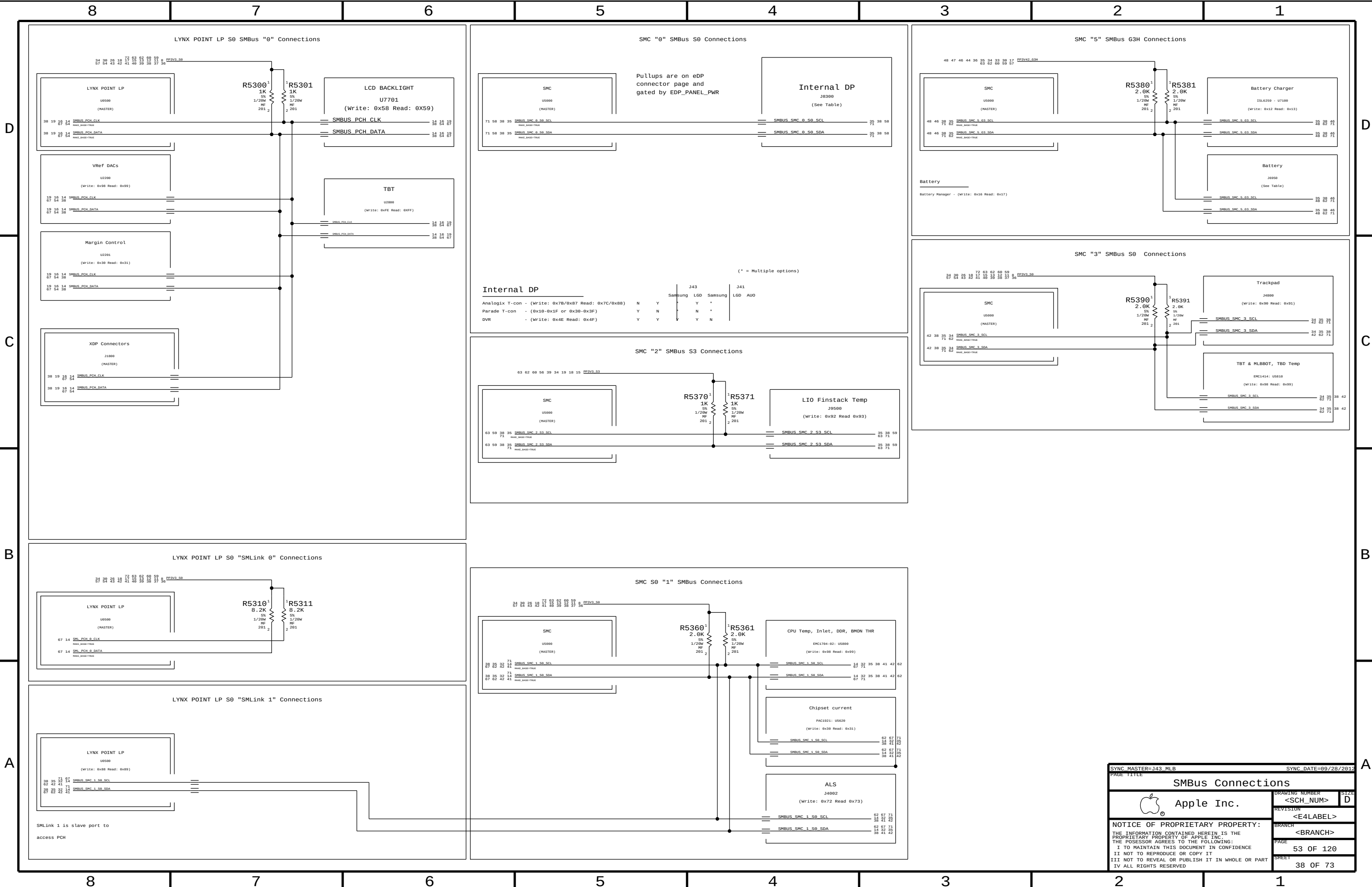
50 OF 120

SHEET

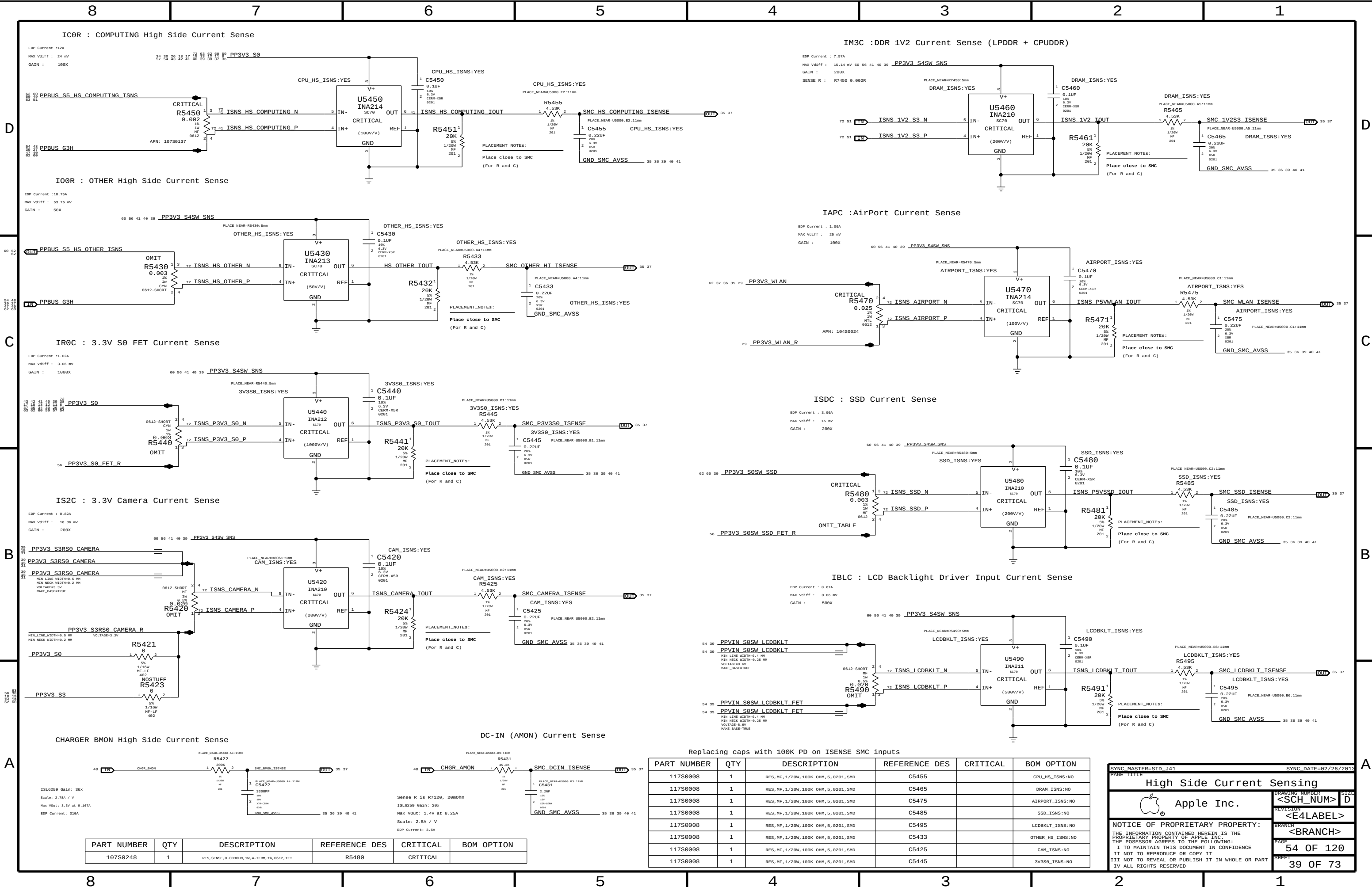
35 OF 73







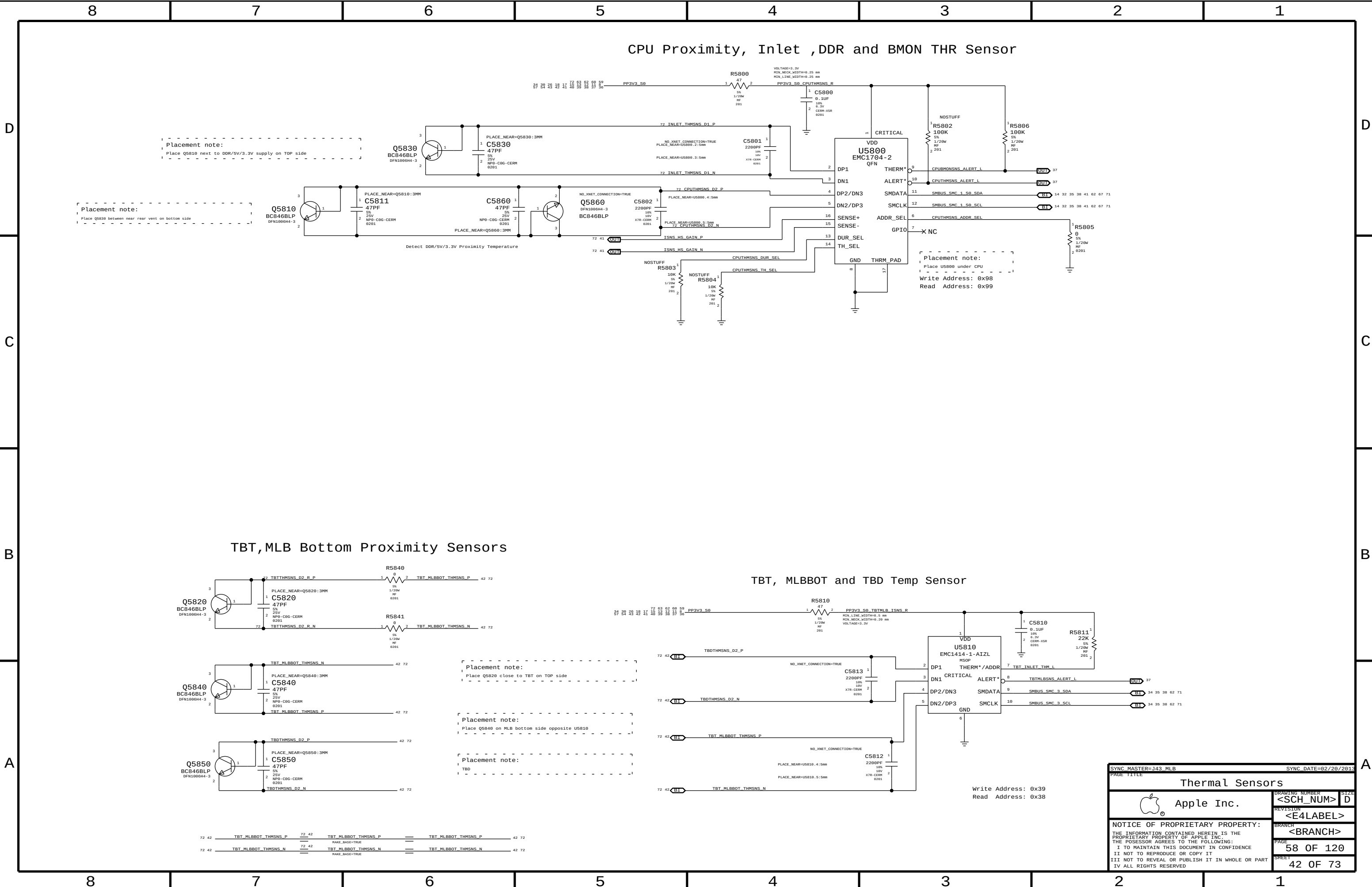












SYNC MASTER=143 MLB

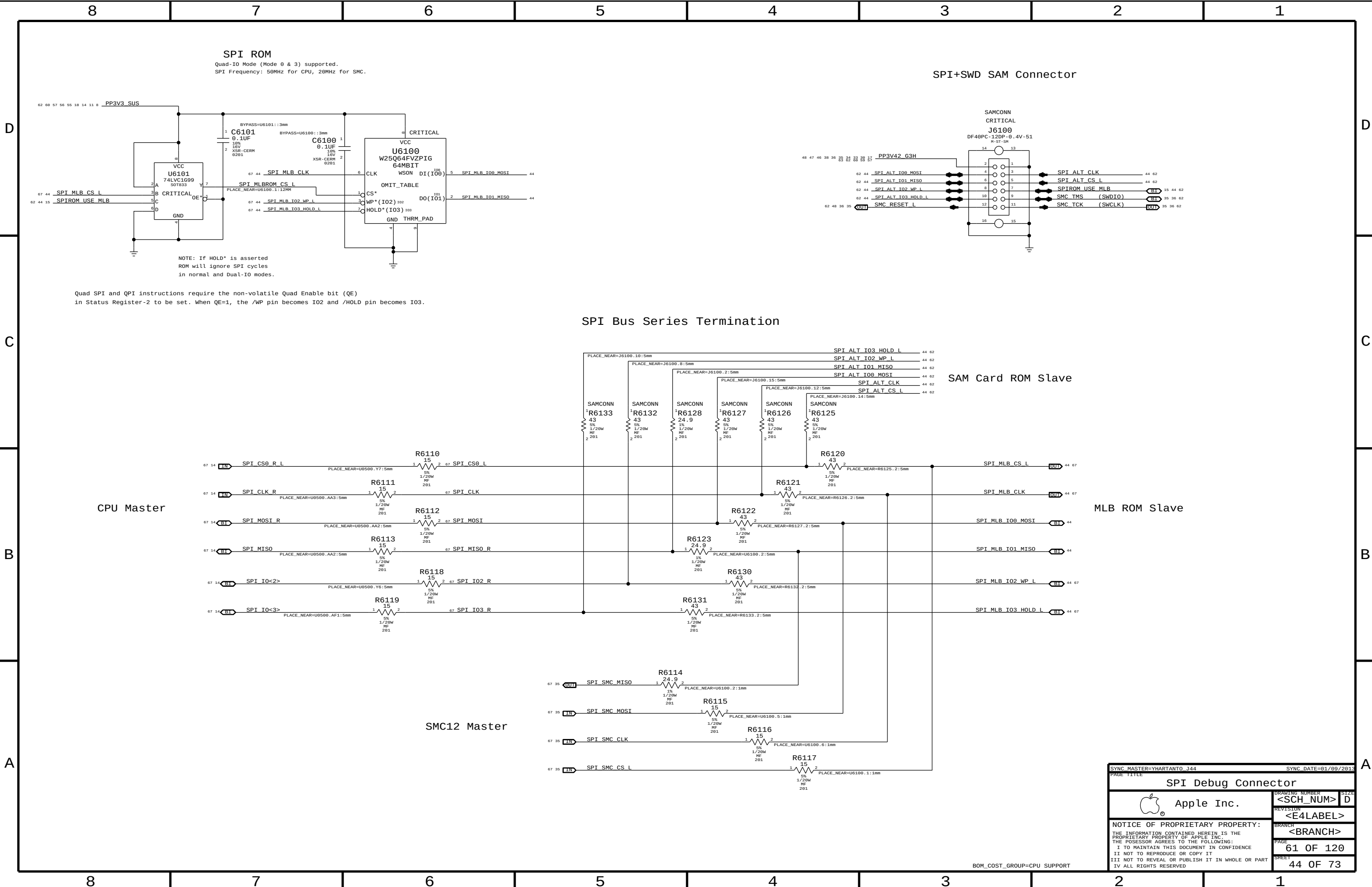
SYNC DATE=02/28/2013

|                                                                                                                                                                                                                                                                                                                         |                                                                                       |
|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------|
| Thermal Sensors                                                                                                                                                                                                                                                                                                         |                                                                                       |
| Apple Inc.                                                                                                                                                                                                                                                                                                              | DRAWING NUMBER<br><SCH_NUM> D                                                         |
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## D

DCB

A



SPI ROM  
Quad-I/O Mode (Mode 0 & 3) supported.  
SPI Frequency: 50MHz for CPU, 20MHz for SMC.

SPI+SWD SAM Connector

SPI Bus Series Termination

SAM Card ROM Slave

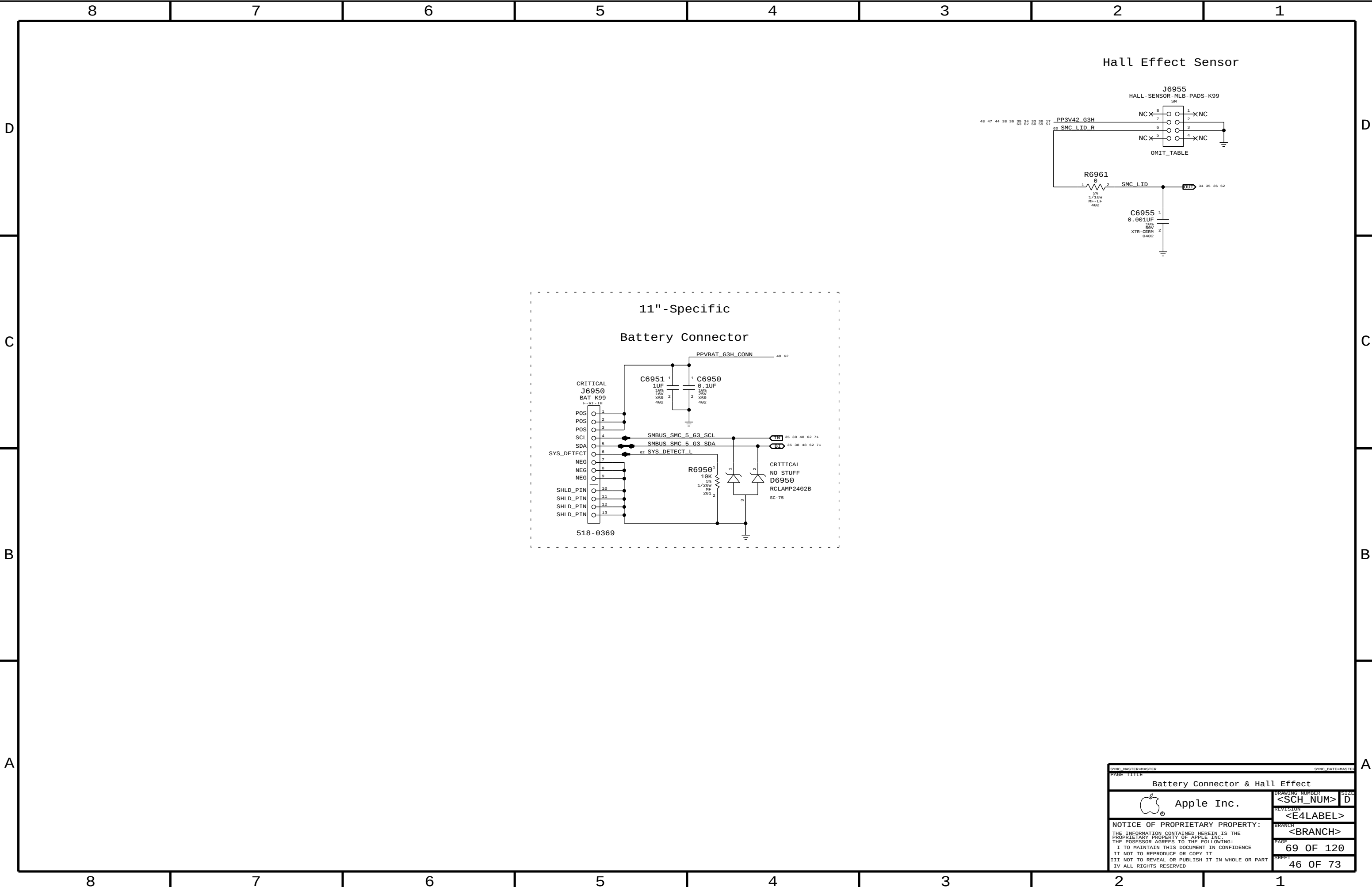
MLB ROM Slave

SMC12 Master

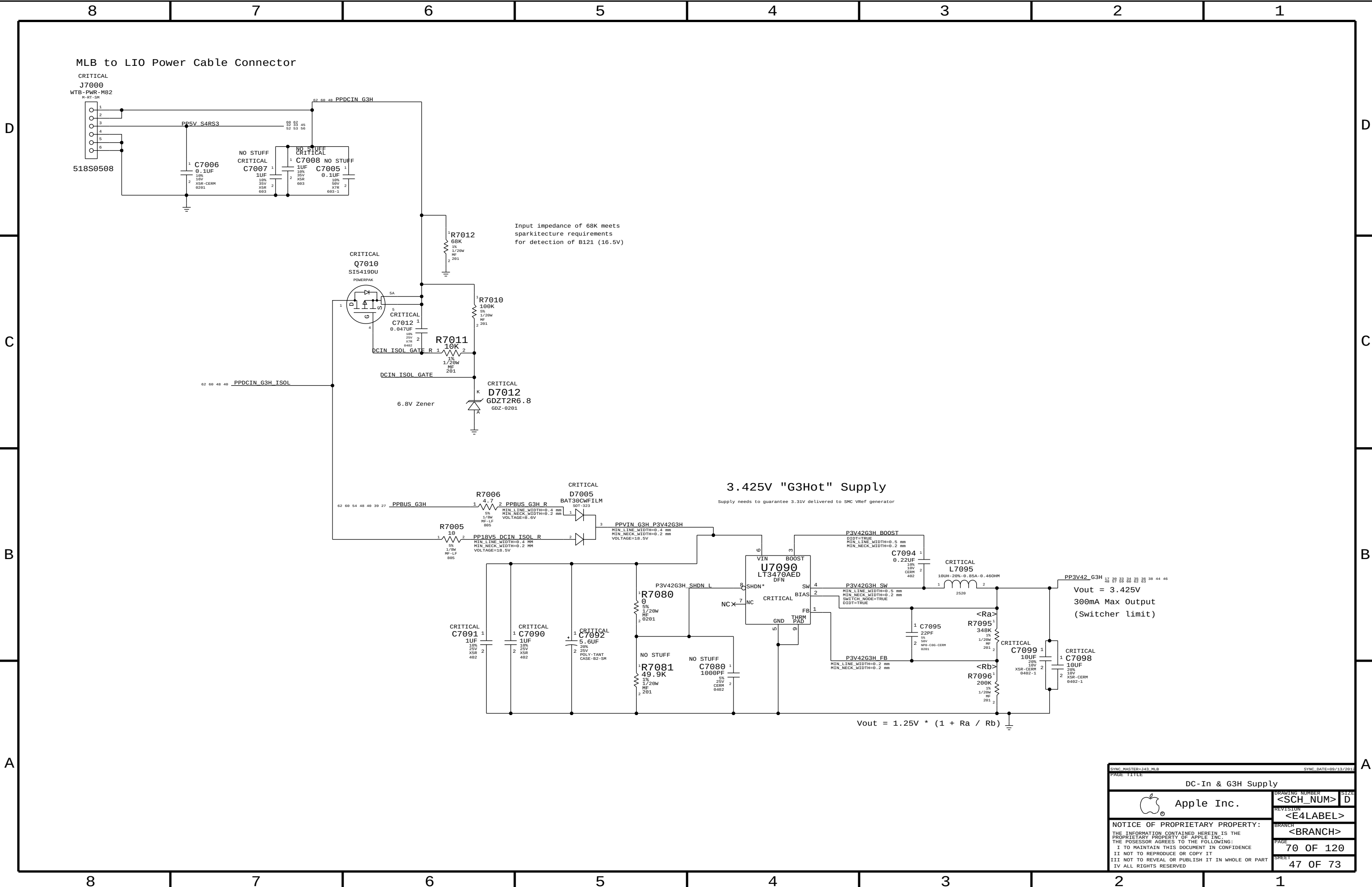
|                                                                                                                                                                                                                                                                                                                             |  |                      |           |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--|----------------------|-----------|
| SYNC MASTER=YHARTANTO J44                                                                                                                                                                                                                                                                                                   |  | SYNC DATE=01/09/2013 |           |
| PAGE TITLE                                                                                                                                                                                                                                                                                                                  |  |                      |           |
| SPI Debug Connector                                                                                                                                                                                                                                                                                                         |  |                      |           |
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|                                                                                                                                                                                                                                                                                                                             |  | PAGE                 | 61 OF 120 |
|                                                                                                                                                                                                                                                                                                                             |  | SHEET                | 44 OF 73  |

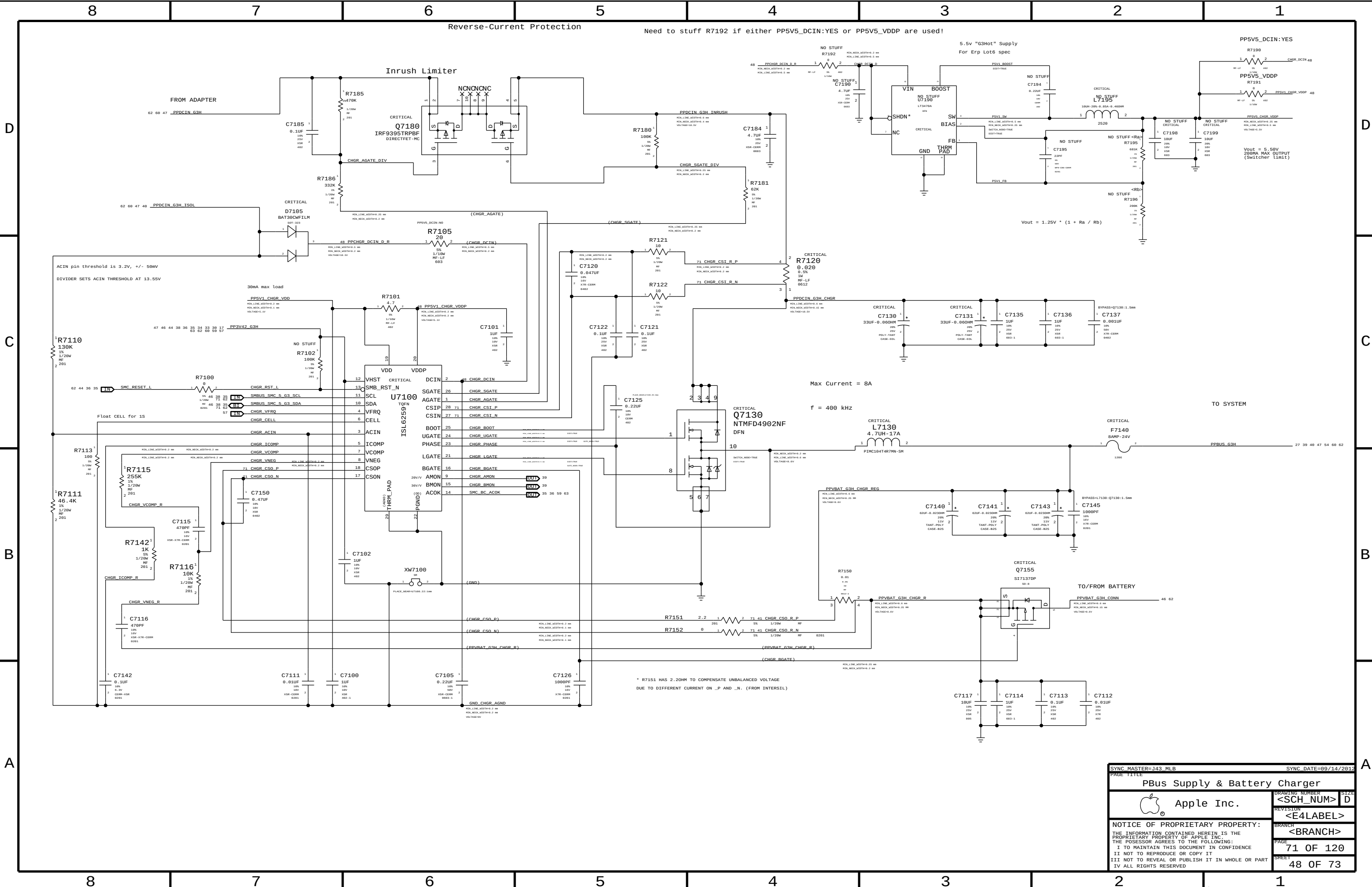
BOM\_COST\_GROUP=CPU\_SUPPORT







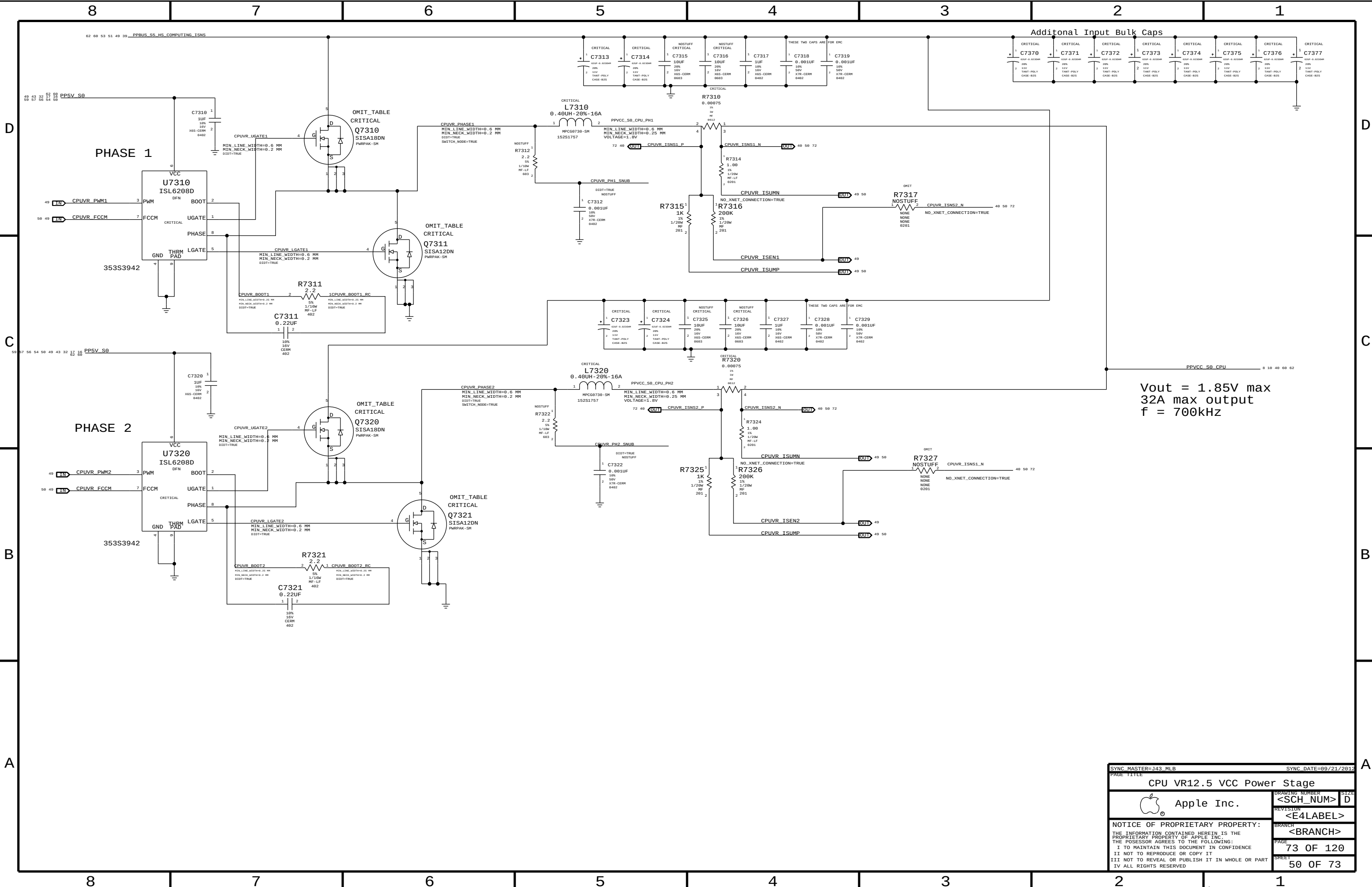


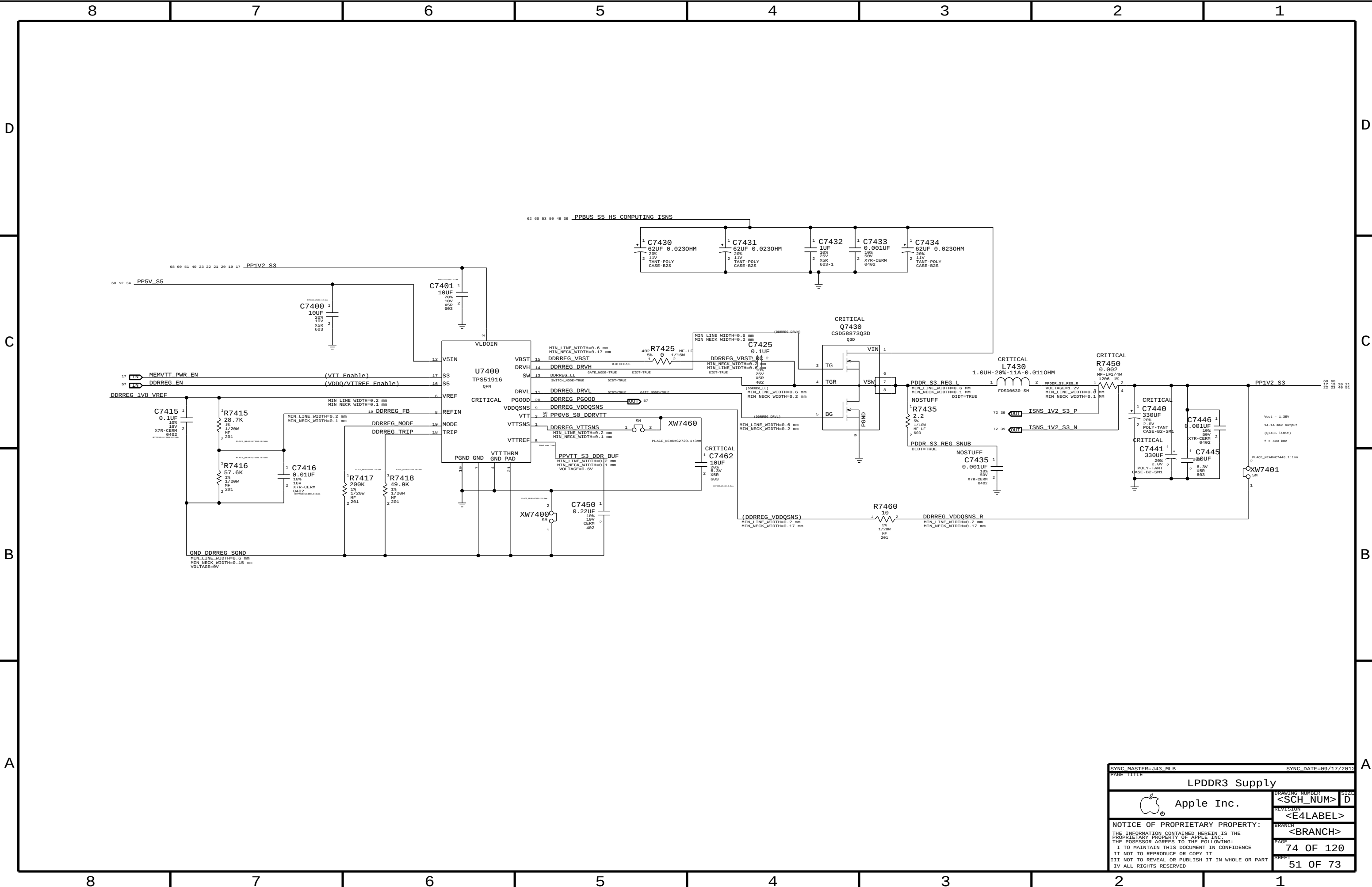


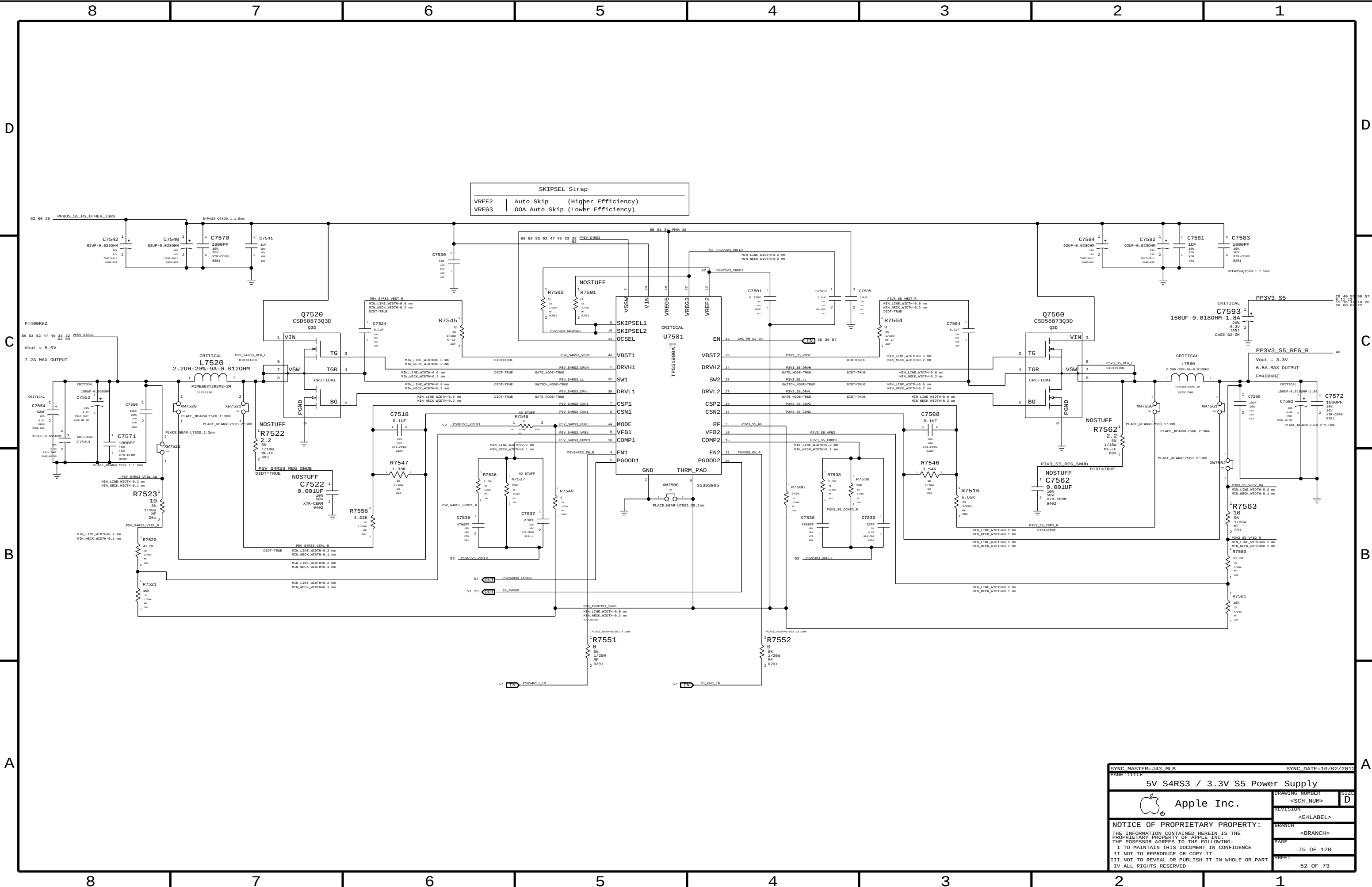
|                                                                                                                                                                                                                                                                                                                         |  |                      |           |
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| SYNC MASTER=143 MLB                                                                                                                                                                                                                                                                                                     |  | SYNC DATE=89/14/2012 |           |
| PAGE TITLE                                                                                                                                                                                                                                                                                                              |  |                      |           |
| PBus Supply & Battery Charger                                                                                                                                                                                                                                                                                           |  |                      |           |
|  Apple Inc.                                                                                                                                                                                                                        |  | DRAWING NUMBER       | SIZE      |
|                                                                                                                                                                                                                                                                                                                         |  | <SCH_NUM>            | D         |
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|                                                                                                                                                                                                                                                                                                                         |  | <E4LABEL>            |           |
|                                                                                                                                                                                                                                                                                                                         |  | BRANCH               |           |
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|                                                                                                                                                                                                                                                                                                                         |  | PAGE                 | 71 OF 120 |
|                                                                                                                                                                                                                                                                                                                         |  | SHEET                | 48 OF 73  |
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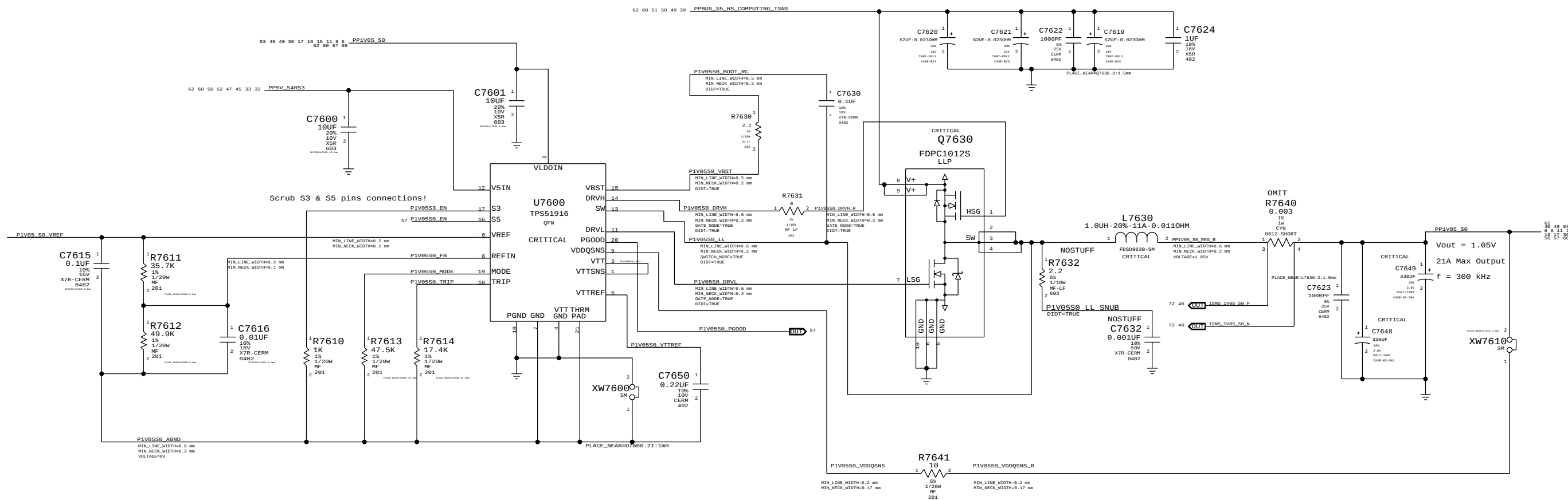




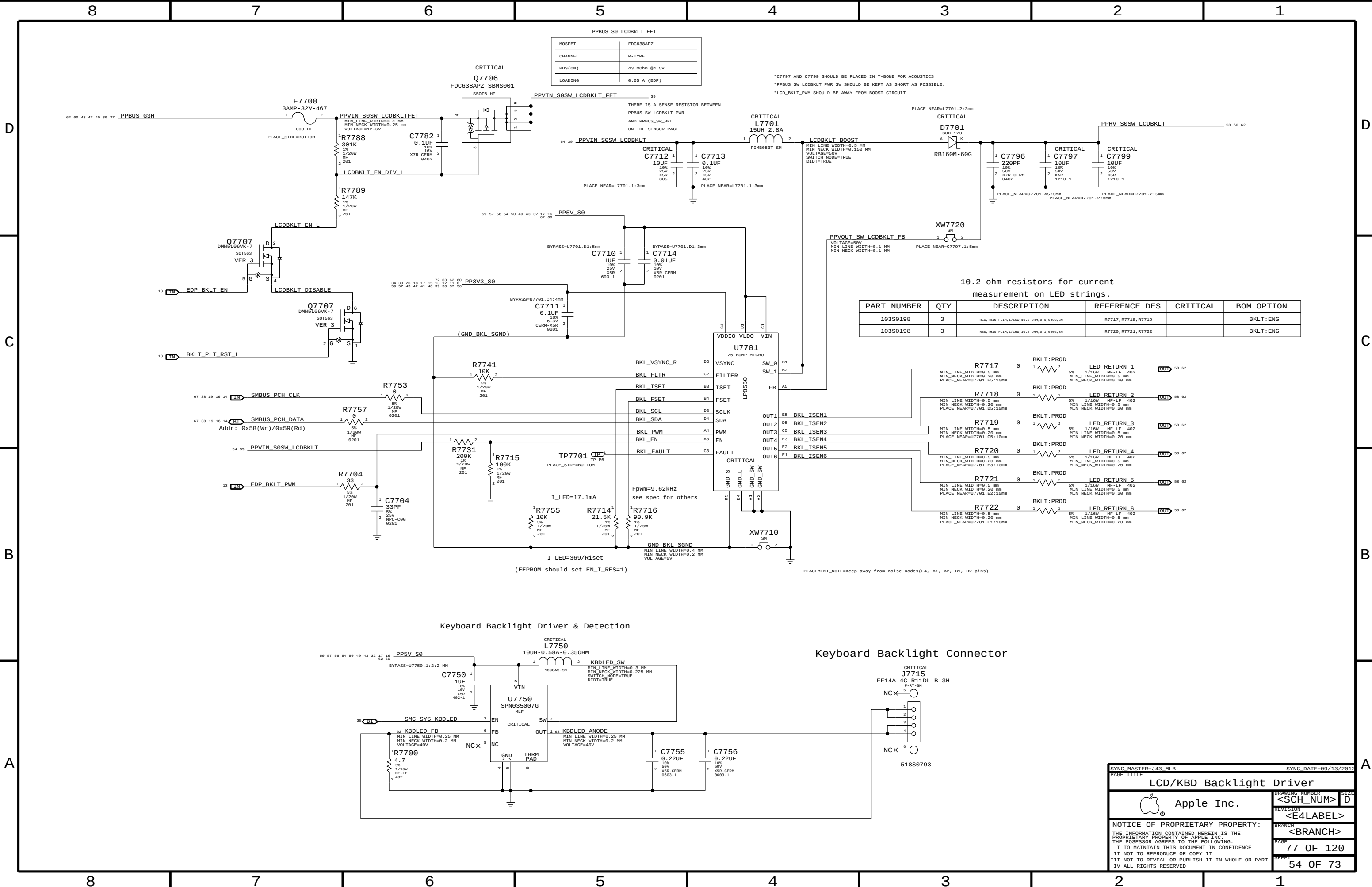




1.05V S0 Regulator



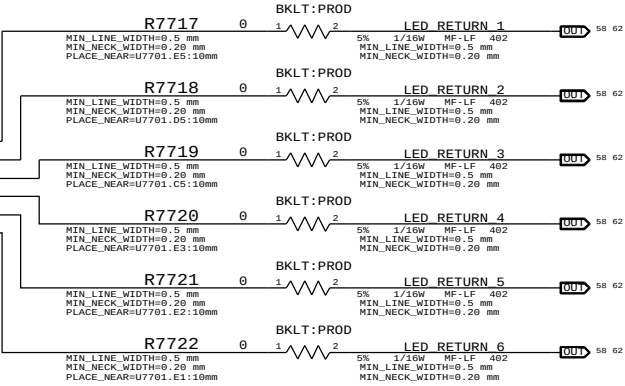
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| SYNC_MASTER=143_MLB                                                                                               |  | SYNC_DATE=89/10/2012  |           |
| PAGE TITLE                                                                                                        |  | 1.05V S0 Power Supply |           |
| DRAWING NUMBER                                                                                                    |  | <SCH_NUM>             | SIZE      |
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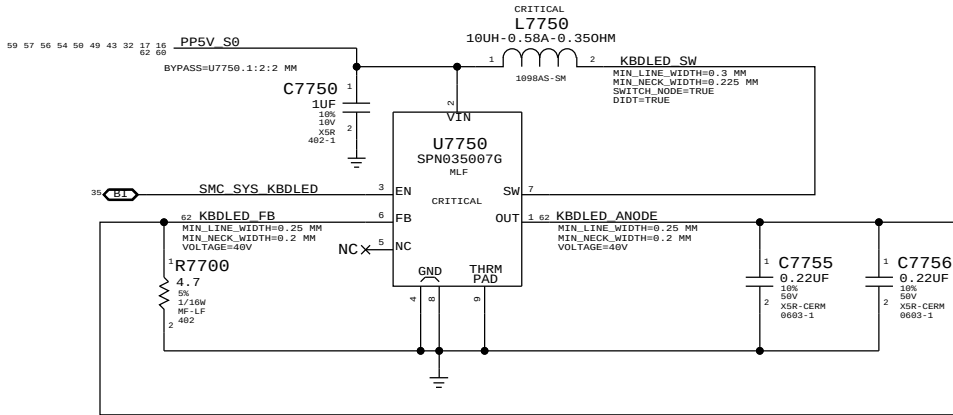
| PPBUS S0 LCDBKLT FET |               |
|----------------------|---------------|
| MOSFET               | FDC638APZ     |
| CHANNEL              | P-TYPE        |
| RDS(ON)              | 43 mOhm @4.5V |
| LOADING              | 0.65 A (EDP)  |

\*C7797 AND C7799 SHOULD BE PLACED IN T-BONE FOR ACOUSTICS  
\*PPBUS\_SW\_LCDBKLT\_PWR\_SW SHOULD BE KEPT AS SHORT AS POSSIBLE.  
\*LCD\_BKLT\_PWM SHOULD BE AWAY FROM BOOST CIRCUIT

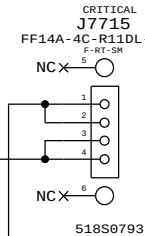
| PART NUMBER | QTY | DESCRIPTION                              | REFERENCE DES     | CRITICAL | BOM OPTION |
|-------------|-----|------------------------------------------|-------------------|----------|------------|
| 103S0198    | 3   | RES,THIN FLTM,1/16W,10.2 OHM,0.1,0402,SM | R7717,R7718,R7719 |          | BKLT:ENG   |
| 103S0198    | 3   | RES,THIN FLTM,1/16W,10.2 OHM,0.1,0402,SM | R7720,R7721,R7722 |          | BKLT:ENG   |



Keyboard Backlight Driver & Detection



Keyboard Backlight Connector



SYNC MASTER=143 MLB

SYNC DATE=09/13/2012

LCD/KBD Backlight Driver

Apple Inc.

<SCH\_NUM> D

<E4LABEL>

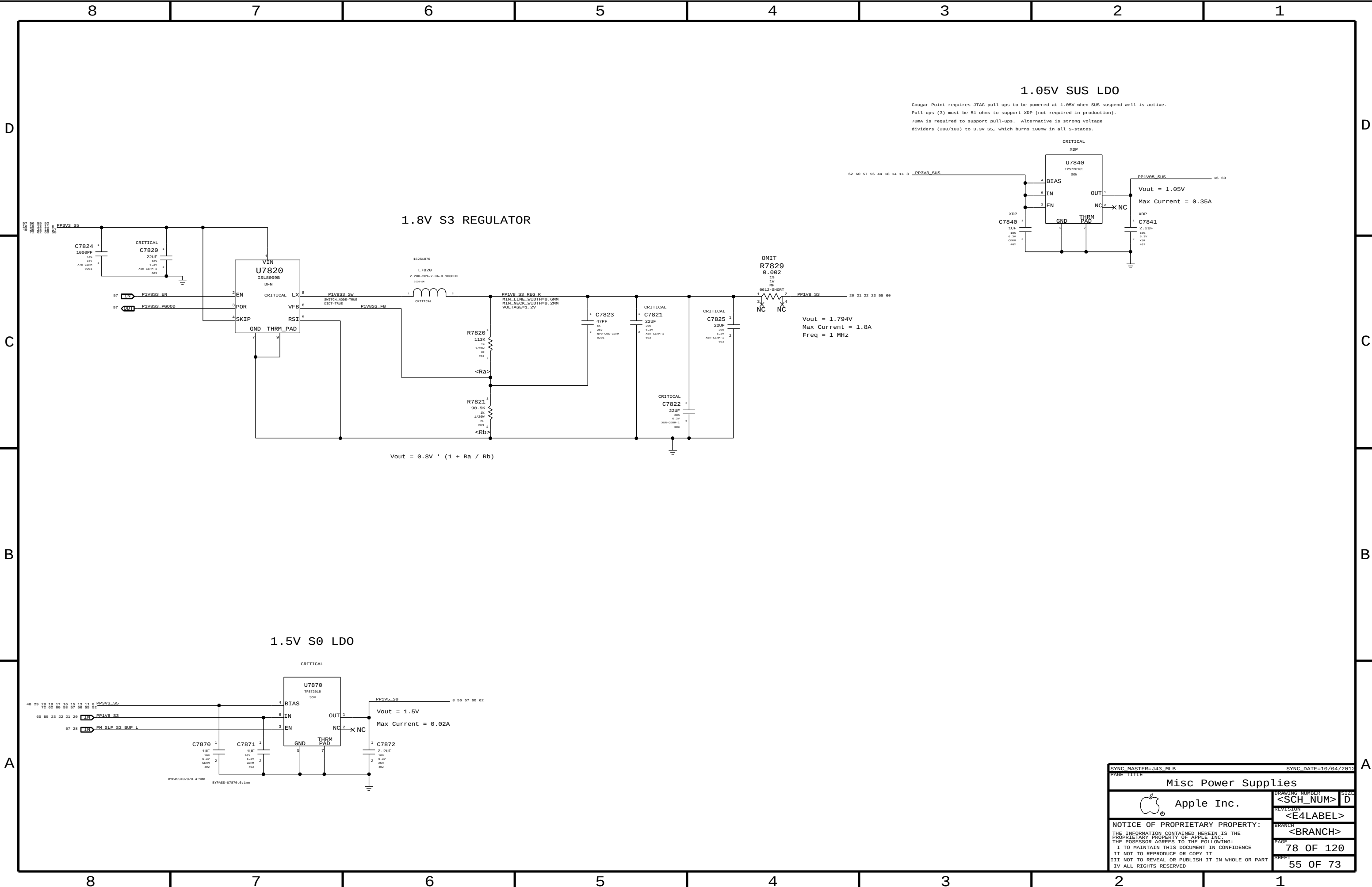
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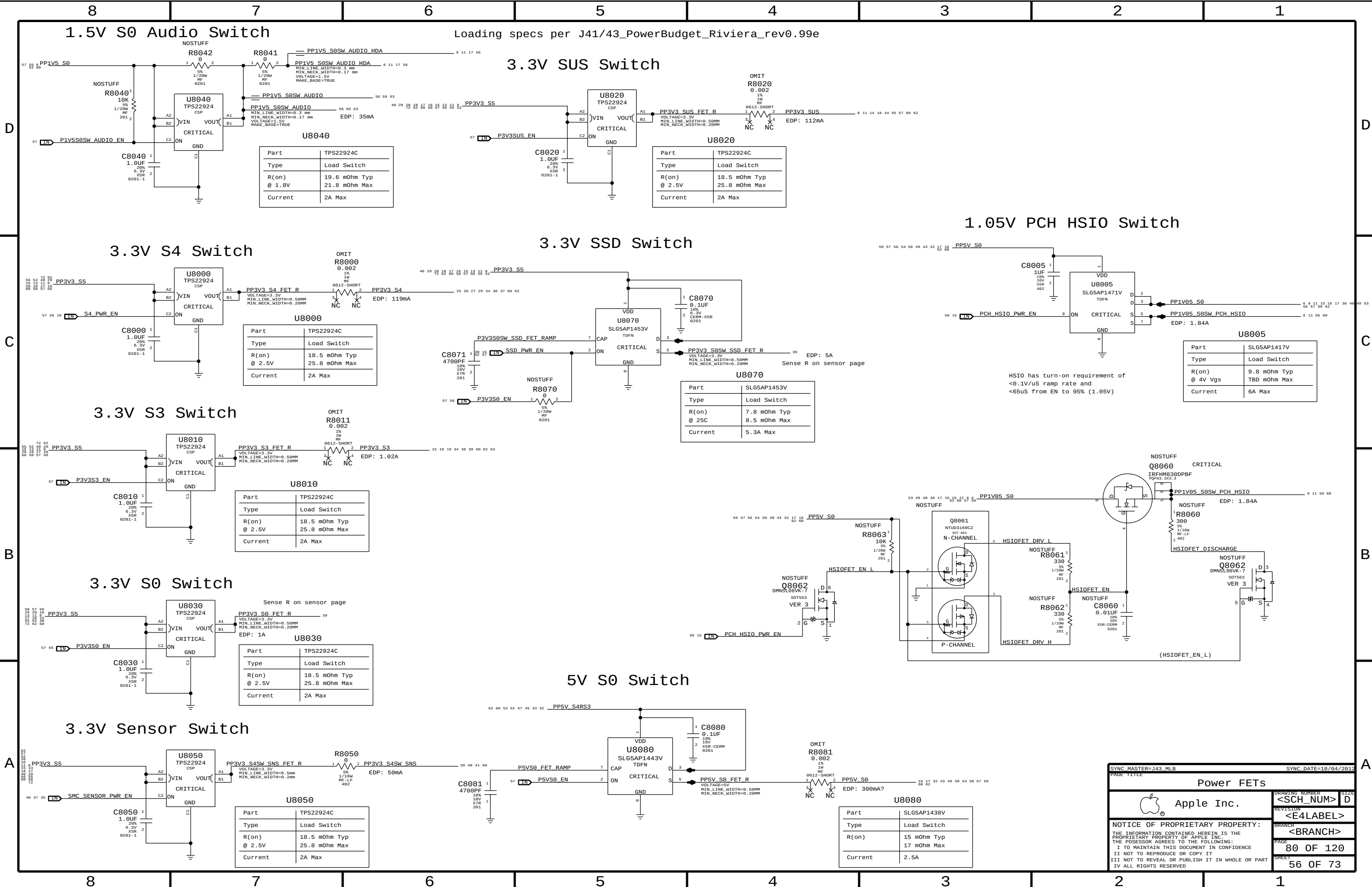
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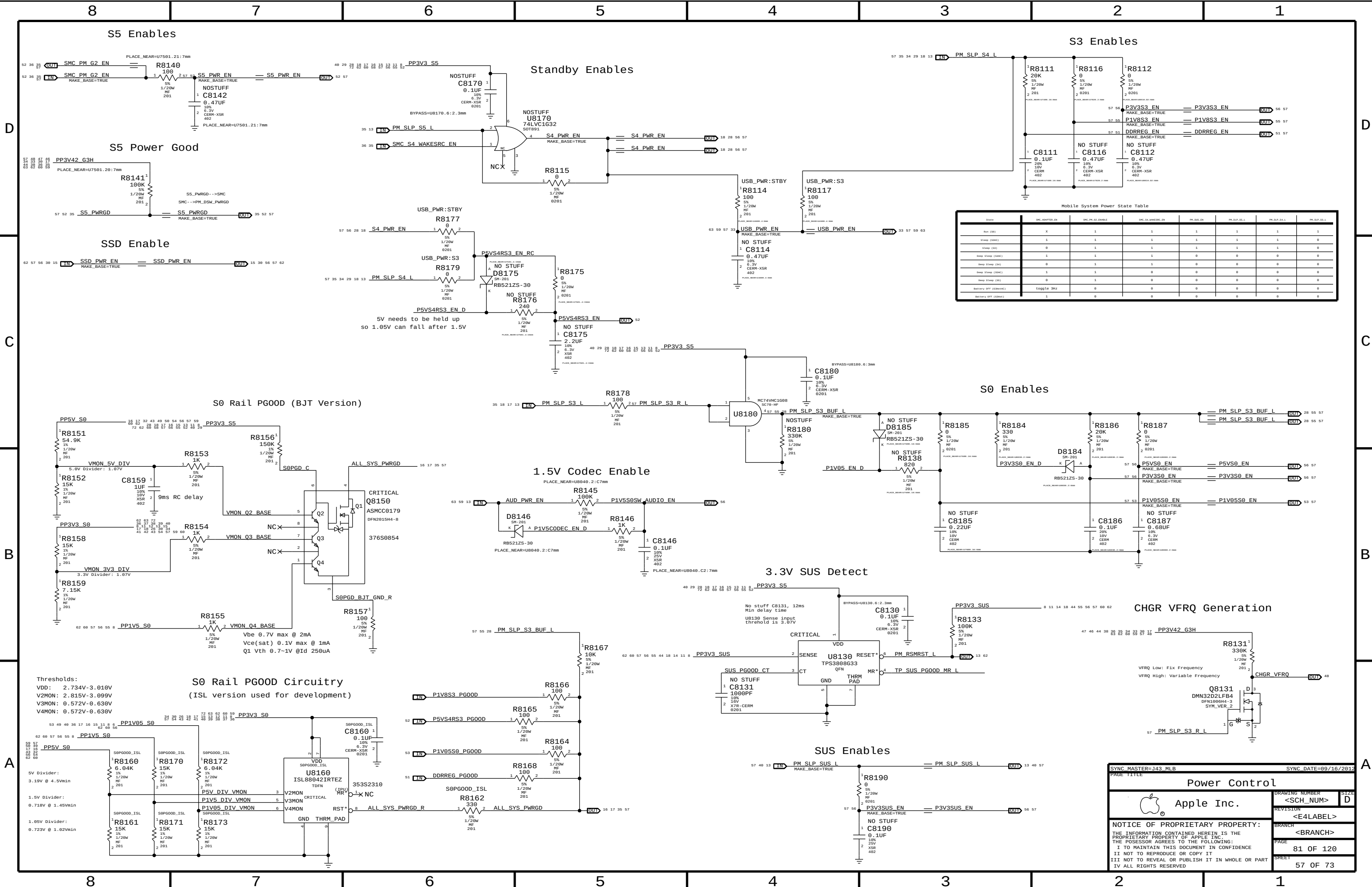
SHEET 54 OF 73



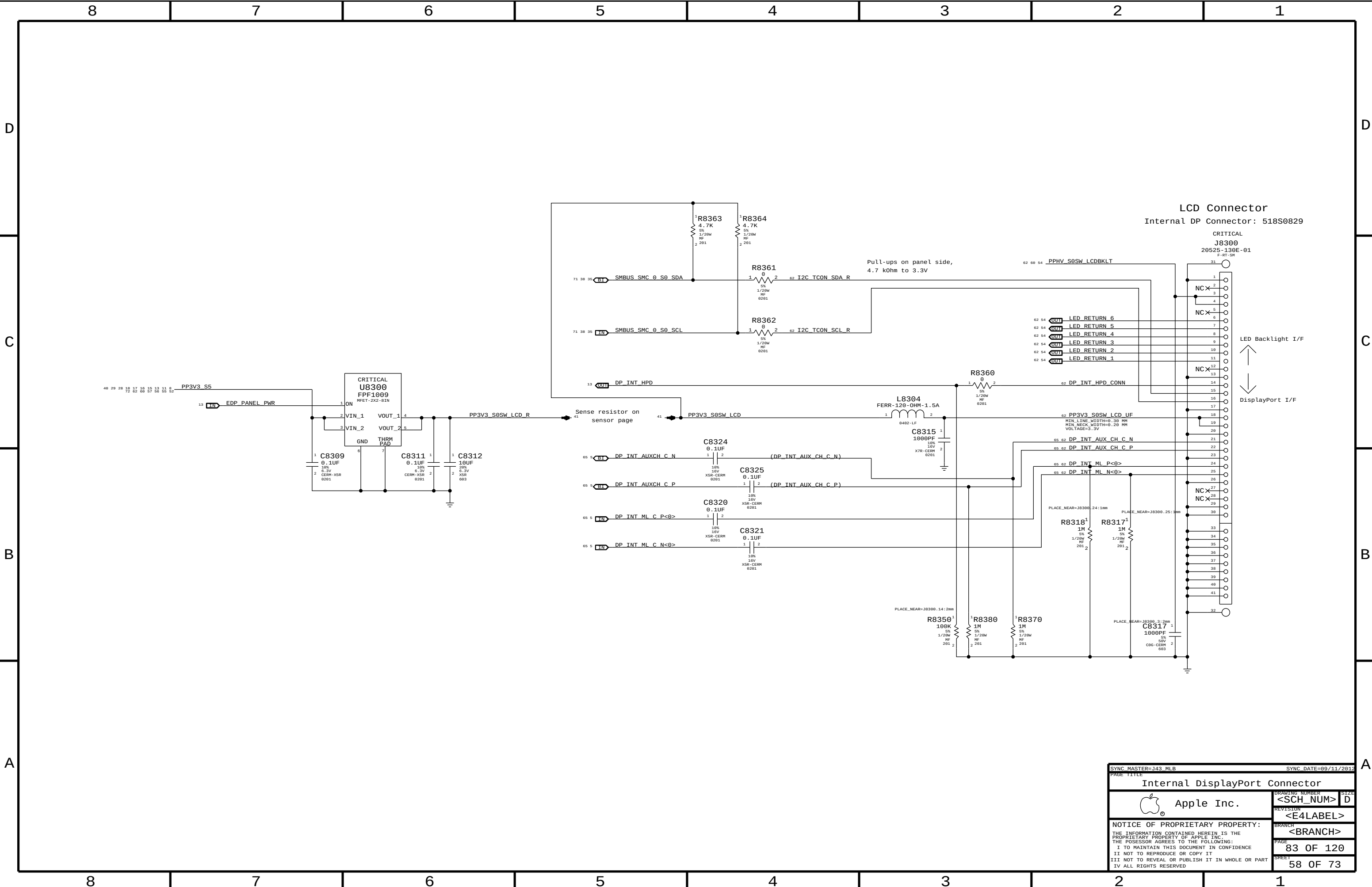


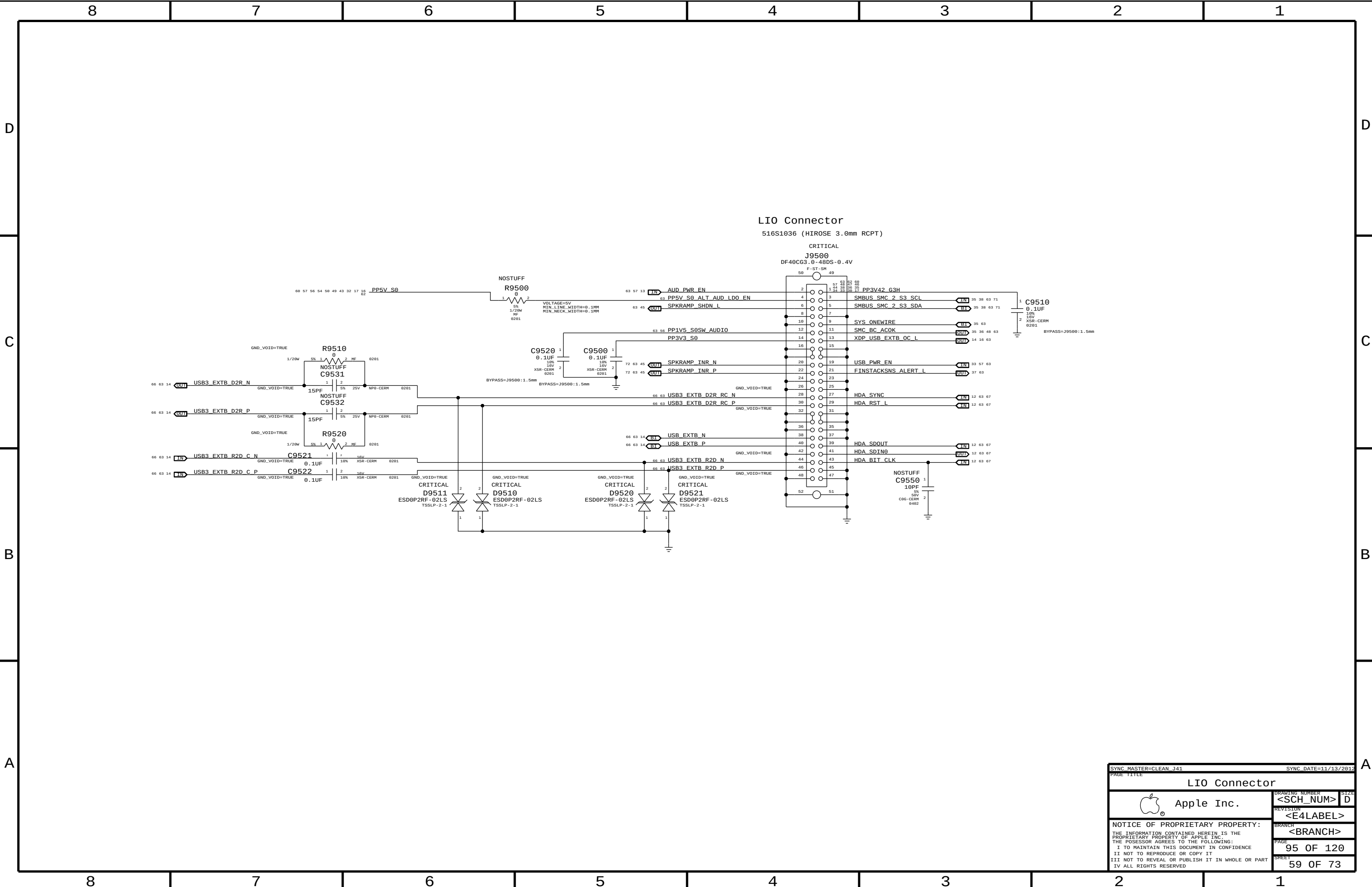


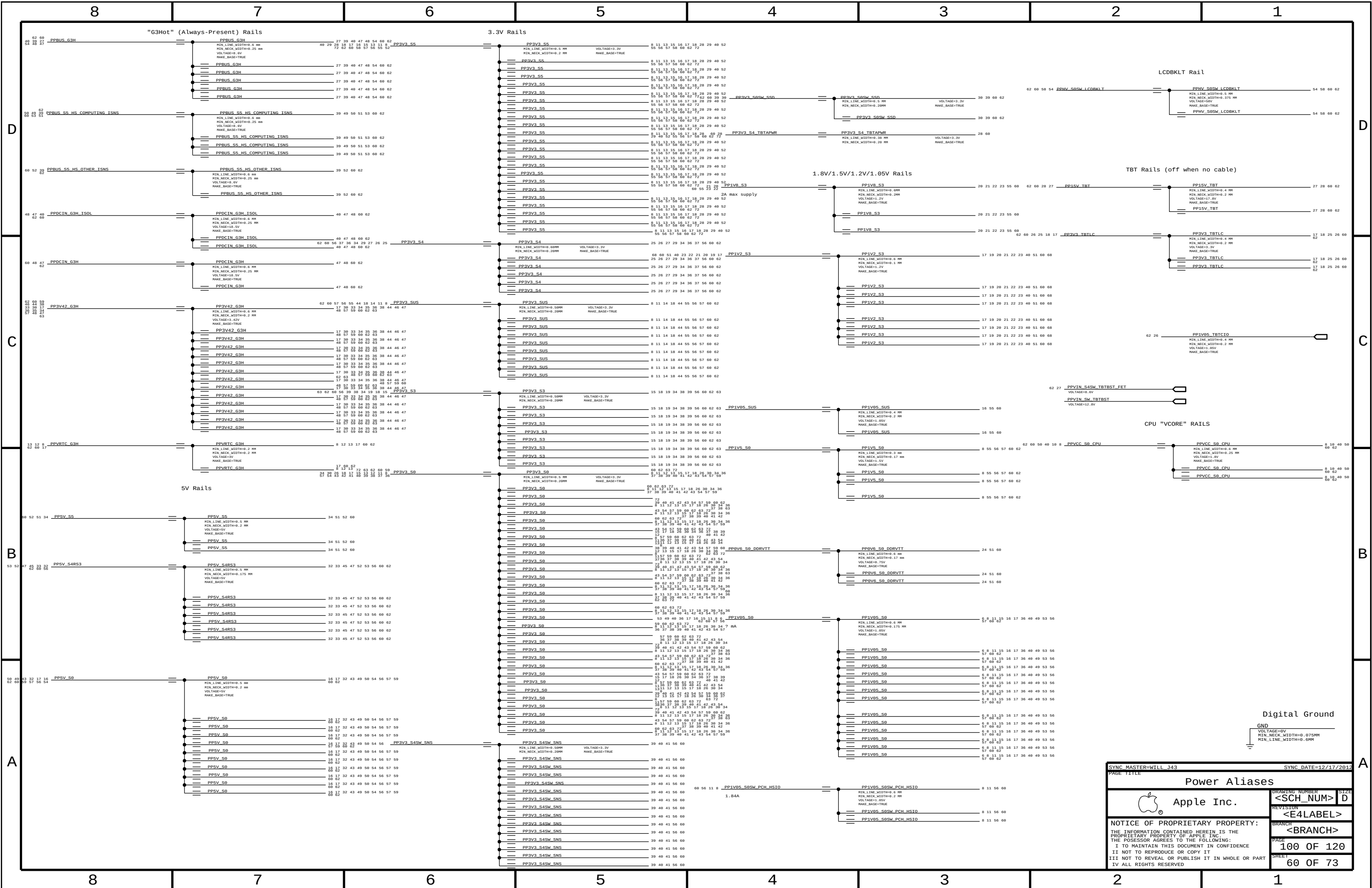




|                                                                                                                   |  |                      |           |
|-------------------------------------------------------------------------------------------------------------------|--|----------------------|-----------|
| SYNC MASTER=143 MLB                                                                                               |  | SYNC DATE=89/16/2012 |           |
| PAGE TITLE                                                                                                        |  | PAGE 1               |           |
| Power Control                                                                                                     |  | DRAWING NUMBER       | <SCH_NUM> |
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|   | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 6                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 5                                    | 4 | 3 | 2 | 1 |  |
|---|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------|---|---|---|---|--|
|   | Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                      |   |   |   |   |  |
|   | J3501: AirPort / BT Connector                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | J6000: Fan Connector                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | Misc Voltages & Control Signals                                                                                                                                                                                                                                                                                                                                                                                                                                                      | NO_TEST Nets                         |   |   |   |   |  |
| D | <p>FUNC_TEST</p> <p>PP3V3 WLAN (Need 6 Tps)</p> <p>WIFI EVENT L</p> <p>PCIE AP R2D N</p> <p>PCIE AP R2D P</p> <p>PCIE CLK100M AP N</p> <p>PCIE CLK100M AP P</p> <p>PCIE AP D2R P</p> <p>PCIE AP D2R N</p> <p>PCIE_WAKE L</p> <p>AP RESET_CONN L</p> <p>AP_CLKREQ_O_L</p> <p>USB_BT_CONN_P</p> <p>USB_BT_CONN_N</p> <p>PP3V3_S4</p> <p>(Need to add 8 GND TPs)</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                          | <p>FUNC_TEST</p> <p>PP5V_S0</p> <p>FAN_RT_TACH</p> <p>FAN_RT_PWM</p> <p>(Need to add 1 GND TP)</p> <p>J4800: IPD Flex Connector</p> <p>S_M_C_L_I_D</p> <p>T_P_A_D_S_P_I_M_I_S_O_R</p> <p>U_S_B_T_P_A_D_P</p> <p>U_S_B_T_P_A_D_N</p> <p>T_P_A_D_S_P_I_C_L_K_R</p> <p>T_P_A_D_W_A_K_E_L</p> <p>T_P_A_D_S_P_I_M_O_S_I_R</p> <p>P_P_3_V_3_S_4_I_P_D</p> <p>T_P_A_D_S_P_I_C_S_R_L</p> <p>T_P_A_D_S_P_I_I_F_EN_CONN</p> <p>T_P_A_D_S_P_I_I_N_T_S_4_W_A_K_E_L_CONN</p> <p>P_P_5_V_4_I_P_D</p> <p>T_P_A_D_U_S_B_I_F_EN_CONN</p> <p>S_M_B_U_S_S_M_C_3_S_D_A</p> <p>S_M_B_U_S_S_M_C_3_S_C_L</p> <p>S_M_C_L_S_O_C_R_S_T_L</p> <p>P_P_3_V_4_2_G_3_H</p> <p>S_M_C_O_N_O_F_F_L</p> <p>(Need to add 5 GND TPs)</p> <p>J7000: DC-In Connector</p> <p>P_P_D_C_I_N_G_3_H</p> <p>P_P_5_V_4_R_S_3</p> <p>(Need to add 5 GND TPs)</p> <p>J6404: Speaker Connector</p> <p>S_P_K_R_A_M_P_R_O_U_T_P</p> <p>S_P_K_R_A_M_P_R_O_U_T_N</p> <p>(Need to add 3 GND TPs)</p> <p>J6950: Battery Connector</p> <p>P_P_V_B_A_T_G_3_H_C_O_N_N</p> <p>S_M_B_U_S_S_M_C_5_G_3_S_C_L</p> <p>S_M_B_U_S_S_M_C_5_G_3_S_D_A</p> <p>S_Y_S_DETECT_L</p> <p>(Need to add 4 GND TPs near J7050 and 1 for shield)</p> <p>J8300: Internal DP Connector</p> <p>P_P_H_V_S_0_S_W_L_C_D_B_K_L_T</p> <p>L_E_D_RETURN_6</p> <p>L_E_D_RETURN_5</p> <p>L_E_D_RETURN_4</p> <p>L_E_D_RETURN_3</p> <p>L_E_D_RETURN_2</p> <p>L_E_D_RETURN_1</p> <p>D_P_I_N_T_H_P_D_C_O_N_N</p> <p>I_2_C_T_C_O_N_S_D_A_R</p> <p>I_2_C_T_C_O_N_S_C_L_R</p> <p>P_P_3_V_3_S_0_S_W_L_C_D_U_F</p> <p>D_P_I_N_T_A_U_X_C_H_C_N</p> <p>D_P_I_N_T_A_U_X_C_H_C_P</p> <p>D_P_I_N_T_M_L_P&lt;0&gt;</p> <p>D_P_I_N_T_M_L_N&lt;0&gt;</p> <p>(Need to add 5 GND TPs)</p> <p>J7715: KB BKLT Connector</p> <p>K_B_D_L_E_D_A_N_O_D_E</p> <p>K_B_D_L_E_D_F_B</p> <p>(Need to add 2 GND TPs)</p> <p>J1800: XDP Connector (Only a subset are needed for FCT HVM test fixture)</p> <p>X_D_P_CPU_T_C_K</p> <p>X_D_P_P_C_H_T_C_K</p> <p>X_D_P_CPU_T_D_I</p> <p>X_D_P_CPU_T_D_O</p> <p>X_D_P_C_P_U_P_C_H_T_R_S_T_L</p> <p>X_D_P_CPU_T_M_S</p> <p>X_D_P_P_C_H_T_M_S</p> <p>X_D_P_P_C_H_T_D_I</p> <p>X_D_P_P_C_H_T_D_O</p> <p>X_D_P_CPU_P_R_E_Q_L</p> <p>X_D_P_CPU_P_R_D_Y_L</p> <p>X_D_P_CPU_V_C_C_S_T_P_W_R_G_D</p> <p>P_M_R_S_M_R_S_T_L</p> <p>X_D_P_S_Y_S_P_W_R_O_K</p> <p>P_M_S_Y_S_R_S_T_L</p> <p>C_P_U_C_F_G&lt;3&gt;</p> <p>P_P_1_V_0_5_S_0</p> <p>(Need to add 2 GND TPs)</p> | <p>FUNC_TEST</p> <p>PPBUS_G3H</p> <p>PPVIN_S4SW_TBTTST_FET</p> <p>PPBUS_SS_HS_COMPUTING_ISNS</p> <p>PPDCIN_G3H</p> <p>PP3V42_G3H</p> <p>PPVRTC_G3H</p> <p>PP3V3_S5</p> <p>PP3V3_SUS</p> <p>PP3V3_S3</p> <p>PP3V3_S0</p> <p>PP3V3_S0SW SSD</p> <p>PP1V5_S0</p> <p>PP1V05_S0</p> <p>PP15V_TBT</p> <p>PP3V3_TBTLIC</p> <p>PP1V05_TBT</p> <p>PPVCSC_S0_CPU</p> <p>PP1V05_TBTCIO</p> <p>PPBUS_SS_HS_OTHER_ISNS</p> <p>PPDCIN_G3H_ISOL</p> <p>PP3V3_S4</p> <p>(Need to add 27 GND TPs)</p> | <p>CPU/PCH</p> <p>SMC</p> <p>TBT</p> |   |   |   |   |  |
| C | <p>J3700: SSD Connector</p> <p>PP3V3_S0SW SSD_FLT (Need 5 TPs)</p> <p>PCIE SSD_R2D_N&lt;3..0&gt;</p> <p>PCIE SSD_R2D_P&lt;3..0&gt;</p> <p>PP3V3_S0</p> <p>SSD_RESET_CONN_L</p> <p>SSD_CLKREQ_CONN_L</p> <p>SMC_00B1_R2D_CONN_L</p> <p>SMC_00B1_D2R_CONN_L</p> <p>SSD_PCIE_SEL_L</p> <p>SSD_SR_EN_L</p> <p>SMC_PWRFAIL_WARN_L</p> <p>SSD_PWR_EN</p> <p>PCIE SSD_D2R_N&lt;3..0&gt;</p> <p>PCIE SSD_D2R_P&lt;3..0&gt;</p> <p>PCIE_CLK100M SSD_N</p> <p>PCIE_CLK100M SSD_P</p> <p>(Need to add 6 GND TPs)</p> <p>J4902: Camera Connector</p> <p>MIPI_CLK_CONN_N</p> <p>MIPI_CLK_CONN_P</p> <p>CAM_SENSOR_WAKE_L_CONN</p> <p>MIPI_DATA_CONN_N</p> <p>MIPI_DATA_CONN_P</p> <p>SMBUS_SMC_1_S0_SDA</p> <p>SMBUS_SMC_1_S0_SCL</p> <p>I2C_CAM_SCK</p> <p>I2C_CAM_SDA</p> <p>PP5V_S3RS0_ALSCAM_F</p> <p>(Need to add TBD GND TPs)</p> |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                      |   |   |   |   |  |
| B | <p>J6100: LPC+SPI Connector</p> <p>SPI_ALT_IO3_HOLD_L</p> <p>SPI_ALT_IO2_WP_L</p> <p>LPC_AD&lt;3..0&gt;</p> <p>SPI_ALT_IO0_MOSI</p> <p>XDP_LPCPLUS_GPIO</p> <p>LPCPLUS_RESET_L</p> <p>SMC_TDO</p> <p>TP_SMC_TRST_L</p> <p>TP_SMC_MD1</p> <p>SMC_TX_L</p> <p>SPI_ALT_IO1_MISO</p> <p>LPC_FRAME_L</p> <p>SPIROM_USE_MLB</p> <p>PM_CLKRUN_L</p> <p>SPI_ALT_CLK</p> <p>SPI_ALT_CS_L</p> <p>LPC_SERIRQ</p> <p>LPC_PWRODN_L</p> <p>SMC_TDI</p> <p>SMC_TCK</p> <p>SMC_RESET_L</p> <p>SMC_ROMBOOT</p> <p>SMC_RX_L</p> <p>SMC_TMS</p> <p>(Need to add 6 GND TPs)</p>                                                                                                                                                                                                                                                                |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                      |   |   |   |   |  |
| A |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |                                      |   |   |   |   |  |
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| Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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| <div> <div> <div>J3501: AirPort / BT Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 WLAN (Need 6 Tps)</div> <div>29 35 36 37 39</div> <div>TRUE</div> <div>WIFI EVENT L</div> <div>29 35 36</div> <div>TRUE</div> <div>PCIE AP R2D N</div> <div>29 67</div> <div>TRUE</div> <div>PCIE AP R2D P</div> <div>29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP N</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP P</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE AP D2R P</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE AP D2R N</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE_WAKE L</div> <div>13 29 31</div> <div>TRUE</div> <div>AP RESET_CONN L</div> <div>29</div> <div>TRUE</div> <div>AP_CLKREQ_0 L</div> <div>29</div> <div>TRUE</div> <div>USB_BT_CONN P</div> <div>29 66</div> <div>TRUE</div> <div>USB_BT_CONN N</div> <div>29 66</div> <div>TRUE</div> <div>PP3V3 S4</div> <div>28 29 34 36 37</div> <div>TRUE</div> <div>(Need to add 8 GND Tps)</div> </div> <div> <div>J3700: SSD Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 S0SW SSD FLT (Need 5 Tps)</div> <div>30</div> <div>TRUE</div> <div>PCIE SSD R2D N&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PCIE SSD R2D P&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PP3V3 S0</div> <div>40 41 42 43 54 57 59</div> <div>TRUE</div> <div>SSD RESET_CONN L</div> <div>26 30 34 35 37 38 39</div> <div>TRUE</div> <div>SSD_CLKREQ_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_R2D_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_D2R_CONN L</div> <div>30</div> <div>TRUE</div> <div>SSD_PCIE_SEL L</div> <div>30</div> <div>TRUE</div> <div>SSD_SR_EN L</div> <div>15 30</div> <div>TRUE</div> <div>SMC_PWRFAIL_WARN L</div> <div>30 35</div> <div>TRUE</div> <div>SSD_PWR_EN</div> <div>15 30 56 57</div> <div>TRUE</div> <div>PCIE SSD D2R N&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE SSD D2R P&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE_CLK100M SSD N</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE_CLK100M SSD P</div> <div>12 30 65</div> <div>TRUE</div> <div>(Need to add 6 GND Tps)</div> </div> <div> <div>J4902: Camera Connector</div> <div> <div>FUNC_TEST</div> <div>MIPI_CLK_CONN N</div> <div>32 70</div> <div>TRUE</div> <div>MIPI_CLK_CONN P</div> <div>32 70</div> <div>TRUE</div> <div>CAM_SENSOR_WAKE_L_CONN</div> <div>32</div> <div>TRUE</div> <div>MIPI_DATA_CONN N</div> <div>32 70</div> <div>TRUE</div> <div>MIPI_DATA_CONN P</div> <div>32 70</div> <div>TRUE</div> <div>SMBUS_SMC_1_S0_SDA</div> <div>14 32 35 38 41 42 67</div> <div>TRUE</div> <div>SMBUS_SMC_1_S0_SCL</div> <div>71</div> <div>TRUE</div> <div>I2C_CAM_SCK</div> <div>31 32</div> <div>TRUE</div> <div>I2C_CAM_SDA</div> <div>31 32</div> <div>TRUE</div> <div>PP5V_S3RS0_ALSCAM_F (Need 2 Tps)</div> <div>32</div> <div>TRUE</div> <div>(Need to add 2 GND Tps)</div> </div> </div> <div> <div>J6100: LPC+SPI Connector</div> <div> <div>FUNC_TEST</div> <div>SPI_ALT_I03_HOLD_L</div> <div>44</div> <div>TRUE</div> <div>SPI_ALT_I02_WP_L</div> <div>44</div> <div>TRUE</div> <div>LPC_AD&lt;3..0&gt;</div> <div>14 35 67</div> <div>TRUE</div> <div>SPI_ALT_I00_M0SI</div> <div>44</div> <div>TRUE</div> <div>XPDI_LPCPLUS_GPI0</div> <div>15 16</div> <div>TRUE</div> <div>LPCPLUS_RESET_L</div> <div>67</div> <div>TRUE</div> <div>SMC_TDO</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_TRST_L</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_MD1</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TX_L</div> <div>35 36</div> <div>TRUE</div> <div>SPI_ALT_I01_MISO</div> <div>44</div> <div>TRUE</div> <div>LPC_FRAME_L</div> <div>14 35 67</div> <div>TRUE</div> <div>SPIROM_USE_MLB</div> <div>15 44</div> <div>TRUE</div> <div>PM_CLKRUN_L</div> <div>13 35</div> <div>TRUE</div> <div>SPI_ALT_CLK</div> <div>44</div> <div>TRUE</div> <div>SPI_ALT_CS_L</div> <div>44</div> <div>TRUE</div> <div>LPC_SERIRQ</div> <div>15 35</div> <div>TRUE</div> <div>LPC_PWRDWN_L</div> <div>13 35</div> <div>TRUE</div> <div>SMC_TDI</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TCK</div> <div>35 36 44</div> <div>TRUE</div> <div>SMC_RESET_L</div> <div>35 36 44 48</div> <div>TRUE</div> <div>SMC_ROMBOOT</div> <div>35 36</div> <div>TRUE</div> <div>SMC_RX_L</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TMS</div> <div>35 36 44</div> <div>TRUE</div> <div>(Need to add 6 GND Tps)</div> </div> </div> <div> <div>J6900: Fan Connector</div> <div> <div>FUNC_TEST</div> <div>PP5V_S0</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_TACH</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_PWM</div> <div>43</div> <div>TRUE</div> <div>(Need to add 1 GND TP)</div> </div> <div> <div>J4800: IPD Flex Connector</div> <div> <div>FUNC_TEST</div> <div>SMC_LID</div> <div>34 35 36 46</div> <div>TRUE</div> <div>TPAD_SPI_MISO_R</div> <div>34</div> <div>TRUE</div> <div>USB_TPAD_P</div> <div>14 34 66</div> <div>TRUE</div> <div>USB_TPAD_N</div> <div>14 34 66</div> <div>TRUE</div> <div>TPAD_SPI_CLK_R</div> <div>34</div> <div>TRUE</div> <div>TPAD_WAKE_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_M0SI_R</div> <div>34</div> <div>TRUE</div> <div>PP3V3_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_CS_R_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_INT_S4_WAKE_L_CONN</div> <div>34</div> <div>TRUE</div> <div>PP5V_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_USB_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>SMBUS_SMC_3_SDA</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMBUS_SMC_3_SCL</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMC_LS0C_RST_L</div> <div>34 36</div> <div>TRUE</div> <div>PP3V42_G3H</div> <div>17 39 33 34 35 36 38 44 46 47</div> <div>TRUE</div> <div>SMC_ONOFF_L</div> <div>48 57 59 60 62 63</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J7000: DC-In Connector</div> <div> <div>FUNC_TEST</div> <div>PPDCIN_G3H (Need 4 Tps)</div> <div>47 48 60 62</div> <div>TRUE</div> <div>PP5V_S4RS3 (Need 3 Tps)</div> <div>32 33 45 47 52 53 56 60</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J6404: Speaker Connector</div> <div> <div>FUNC_TEST</div> <div>SPKRAMP_ROUT_P</div> <div>45 72</div> <div>TRUE</div> <div>SPKRAMP_ROUT_N</div> <div>45 72</div> <div>TRUE</div> <div>(Need to add 3 GND Tps)</div> </div> <div> <div>J6950: Battery Connector</div> <div> <div>FUNC_TEST</div> <div>PPVBAT_G3H_CONN (Need 4 Tps)</div> <div>46 48</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SCL</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SDA</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SYS_DETECT_L</div> <div>46</div> <div>TRUE</div> <div>(Need to add 4 GND Tps near J7050 and 1 for shield)</div> </div> <div> <div>J8300: Internal DP Connector</div> <div> <div>FUNC_TEST</div> <div>PPHV_S0SW_LCDBKLT (Need 2 Tps)</div> <div>54 58 60</div> <div>TRUE</div> <div>LED_RETURN_6</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_5</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_4</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_3</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_2</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_1</div> <div>54 58</div> <div>TRUE</div> <div>DP_INT_HPD_CONN</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SDA_R</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SCL_R</div> <div>58</div> <div>TRUE</div> <div>PP3V3_S0SW_LCD_UF (Need 2 Tps)</div> <div>58</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_N</div> <div>58 65</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_P</div> <div>58 65</div></div></div></div></div></div></div></div></div></div></div> |   |   |   |   |   |   |   |

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| Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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| NO_TEST Nets                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| <div> <div> <div>J3501: AirPort / BT Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 WLAN (Need 6 Tps)</div> <div>29 35 36 37 39</div> <div>TRUE</div> <div>WIFI EVENT L</div> <div>29 35 36</div> <div>TRUE</div> <div>PCIE AP R2D N</div> <div>29 67</div> <div>TRUE</div> <div>PCIE AP R2D P</div> <div>29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP N</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP P</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE AP D2R P</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE AP D2R N</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE_WAKE L</div> <div>13 29 31</div> <div>TRUE</div> <div>AP RESET_CONN L</div> <div>29</div> <div>TRUE</div> <div>AP_CLKREQ_0 L</div> <div>29</div> <div>TRUE</div> <div>USB_BT_CONN P</div> <div>29 66</div> <div>TRUE</div> <div>USB_BT_CONN N</div> <div>29 66</div> <div>TRUE</div> <div>PP3V3 S4</div> <div>28 29 34 36 37</div> <div>TRUE</div> <div>(Need to add 8 GND Tps)</div> </div> <div> <div>J3700: SSD Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 S0SW SSD FLT (Need 5 Tps)</div> <div>30</div> <div>TRUE</div> <div>PCIE SSD R2D N&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PCIE SSD R2D P&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PP3V3 S0</div> <div>40 41 42 43 54 57 59</div> <div>TRUE</div> <div>SSD RESET_CONN L</div> <div>26 30 34 35 37 38 39</div> <div>TRUE</div> <div>SSD_CLKREQ_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_R2D_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_D2R_CONN L</div> <div>30</div> <div>TRUE</div> <div>SSD_PCIE_SEL L</div> <div>30</div> <div>TRUE</div> <div>SSD_SR_EN L</div> <div>15 30</div> <div>TRUE</div> <div>SMC_PWRFAIL_WARN L</div> <div>30 35</div> <div>TRUE</div> <div>SSD_PWR_EN</div> <div>15 30 56 57</div> <div>TRUE</div> <div>PCIE SSD D2R N&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE SSD D2R P&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE_CLK100M SSD N</div> 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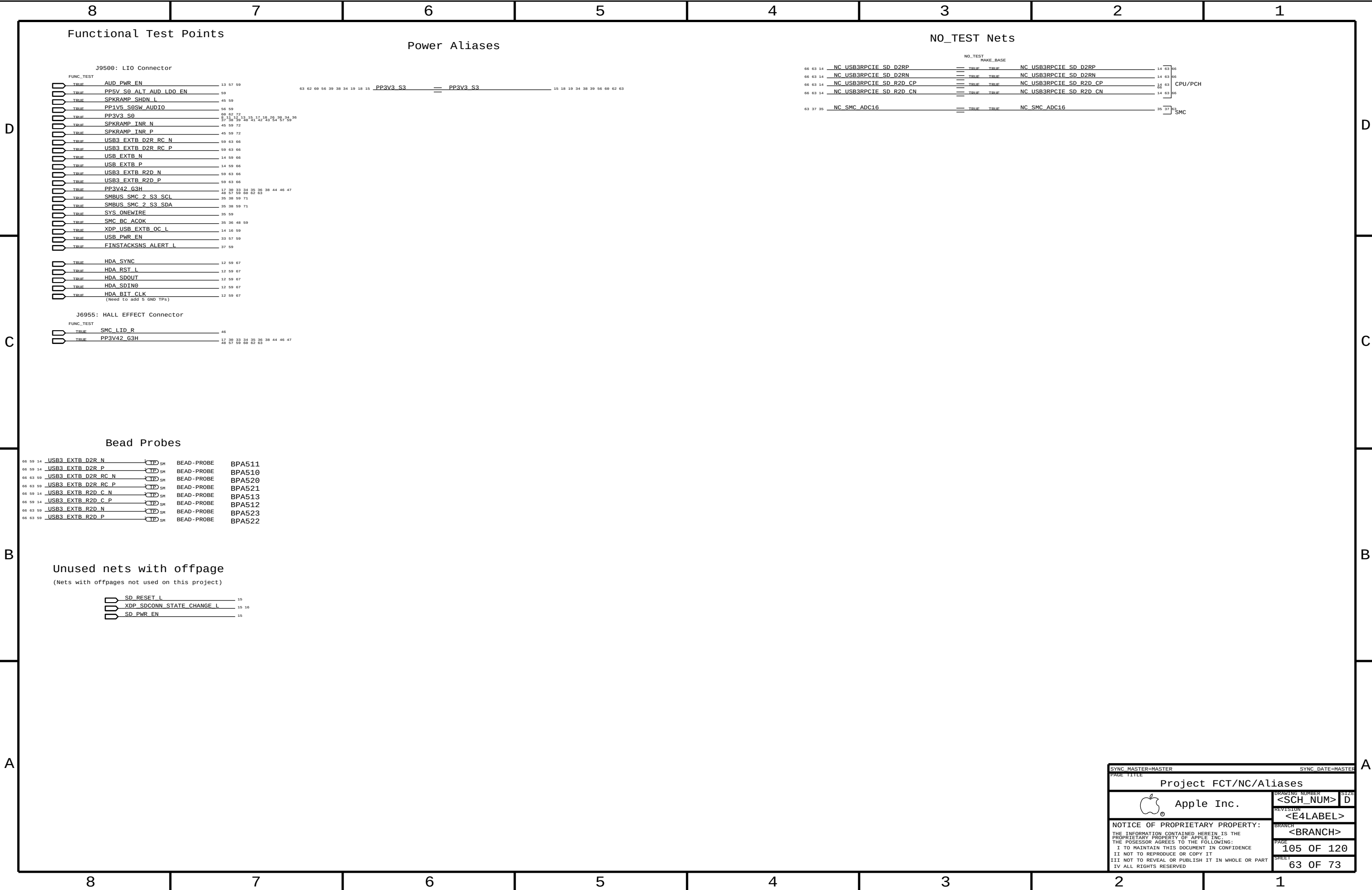
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| Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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| NO_TEST Nets                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| <div> <div> <div>J3501: AirPort / BT Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 WLAN (Need 6 Tps)</div> <div>29 35 36 37 39</div> <div>TRUE</div> <div>WIFI EVENT L</div> <div>29 35 36</div> <div>TRUE</div> <div>PCIE AP R2D N</div> <div>29 67</div> <div>TRUE</div> <div>PCIE AP R2D P</div> <div>29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP N</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP P</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE AP D2R P</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE AP D2R N</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE_WAKE L</div> <div>13 29 31</div> <div>TRUE</div> <div>AP RESET_CONN L</div> <div>29</div> <div>TRUE</div> <div>AP_CLKREQ_0 L</div> <div>29</div> <div>TRUE</div> <div>USB_BT_CONN P</div> <div>29 66</div> <div>TRUE</div> <div>USB_BT_CONN N</div> <div>29 66</div> <div>TRUE</div> <div>PP3V3 S4</div> <div>28 29 34 36 37</div> <div>TRUE</div> <div>(Need to add 8 GND Tps)</div> </div> <div> <div>J3700: SSD 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<div>44</div> <div>TRUE</div> <div>SPI_ALT_I02_WP_L</div> <div>44</div> <div>TRUE</div> <div>LPC_AD&lt;3..0&gt;</div> <div>14 35 67</div> <div>TRUE</div> <div>SPI_ALT_I00_M0SI</div> <div>44</div> <div>TRUE</div> <div>XPDI_LPCPLUS_GPI0</div> <div>15 16</div> <div>TRUE</div> <div>LPCPLUS_RESET_L</div> <div>67</div> <div>TRUE</div> <div>SMC_TDO</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_TRST_L</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_MD1</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TX_L</div> <div>35 36</div> <div>TRUE</div> <div>SPI_ALT_I01_MISO</div> <div>44</div> <div>TRUE</div> <div>LPC_FRAME_L</div> <div>14 35 67</div> <div>TRUE</div> <div>SPIROM_USE_MLB</div> <div>15 44</div> <div>TRUE</div> <div>PM_CLKRUN_L</div> <div>13 35</div> <div>TRUE</div> <div>SPI_ALT_CLK</div> <div>44</div> <div>TRUE</div> <div>SPI_ALT_CS_L</div> <div>44</div> <div>TRUE</div> <div>LPC_SERIRQ</div> <div>15 35</div> <div>TRUE</div> <div>LPC_PWRDWN_L</div> <div>13 35</div> <div>TRUE</div> <div>SMC_TDI</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TCK</div> <div>35 36 44</div> <div>TRUE</div> <div>SMC_RESET_L</div> <div>35 36 44 48</div> <div>TRUE</div> <div>SMC_ROMBOOT</div> <div>35 36</div> <div>TRUE</div> <div>SMC_RX_L</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TMS</div> <div>35 36 44</div> <div>TRUE</div> <div>(Need to add 6 GND Tps)</div> </div> </div> <div> <div>J6900: Fan Connector</div> <div> <div>FUNC_TEST</div> <div>PP5V_S0</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_TACH</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_PWM</div> <div>43</div> <div>TRUE</div> <div>(Need to add 1 GND TP)</div> </div> <div> <div>J4800: IPD Flex Connector</div> <div> <div>FUNC_TEST</div> <div>SMC_LID</div> <div>34 35 36 46</div> <div>TRUE</div> <div>TPAD_SPI_MISO_R</div> <div>34</div> <div>TRUE</div> <div>USB_TPAD_P</div> <div>14 34 66</div> <div>TRUE</div> <div>USB_TPAD_N</div> <div>14 34 66</div> <div>TRUE</div> <div>TPAD_SPI_CLK_R</div> <div>34</div> <div>TRUE</div> <div>TPAD_WAKE_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_M0SI_R</div> <div>34</div> <div>TRUE</div> <div>PP3V3_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_CS_R_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_INT_S4_WAKE_L_CONN</div> <div>34</div> <div>TRUE</div> <div>PP5V_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_USB_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>SMBUS_SMC_3_SDA</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMBUS_SMC_3_SCL</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMC_LS0C_RST_L</div> <div>34 36</div> <div>TRUE</div> <div>PP3V42_G3H</div> <div>17 39 33 34 35 36 38 44 46 47</div> <div>TRUE</div> <div>SMC_ONOFF_L</div> <div>48 57 59 60 62 63</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J7000: DC-In Connector</div> <div> <div>FUNC_TEST</div> <div>PPDCIN_G3H (Need 4 Tps)</div> <div>47 48 60 62</div> <div>TRUE</div> <div>PP5V_S4RS3 (Need 3 Tps)</div> <div>32 33 45 47 52 53 56 60</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J6404: Speaker Connector</div> <div> <div>FUNC_TEST</div> <div>SPKRAMP_ROUT_P</div> <div>45 72</div> <div>TRUE</div> <div>SPKRAMP_ROUT_N</div> <div>45 72</div> <div>TRUE</div> <div>(Need to add 3 GND Tps)</div> </div> <div> <div>J6950: Battery Connector</div> <div> <div>FUNC_TEST</div> <div>PPVBAT_G3H_CONN (Need 4 Tps)</div> <div>46 48</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SCL</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SDA</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SYS_DETECT_L</div> <div>46</div> <div>TRUE</div> <div>(Need to add 4 GND Tps near J7050 and 1 for shield)</div> </div> <div> <div>J8300: Internal DP Connector</div> <div> <div>FUNC_TEST</div> <div>PPHV_S0SW_LCDBKLT (Need 2 Tps)</div> <div>54 58 60</div> <div>TRUE</div> <div>LED_RETURN_6</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_5</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_4</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_3</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_2</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_1</div> <div>54 58</div> <div>TRUE</div> <div>DP_INT_HPD_CONN</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SDA_R</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SCL_R</div> <div>58</div> <div>TRUE</div> <div>PP3V3_S0SW_LCD_UF (Need 2 Tps)</div> <div>58</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_N</div> <div>58 65</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_P</div> <div>58 65</div></div></div></div></div></div></div></div></div></div></div> |   |   |   |   |   |   |   |

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| Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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| NO_TEST Nets                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           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| <div> <div> <div>J3501: AirPort / BT Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 WLAN (Need 6 Tps)</div> <div>29 35 36 37 39</div> <div>TRUE</div> <div>WIFI EVENT L</div> <div>29 35 36</div> <div>TRUE</div> <div>PCIE AP R2D N</div> <div>29 67</div> <div>TRUE</div> <div>PCIE AP R2D P</div> <div>29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP N</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE CLK100M AP P</div> <div>12 29 67</div> <div>TRUE</div> <div>PCIE AP D2R P</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE AP D2R N</div> <div>14 29 67</div> <div>TRUE</div> <div>PCIE_WAKE L</div> <div>13 29 31</div> <div>TRUE</div> <div>AP RESET_CONN L</div> <div>29</div> <div>TRUE</div> <div>AP_CLKREQ_0 L</div> <div>29</div> <div>TRUE</div> <div>USB_BT_CONN P</div> <div>29 66</div> <div>TRUE</div> <div>USB_BT_CONN N</div> <div>29 66</div> <div>TRUE</div> <div>PP3V3 S4</div> <div>28 29 34 36 37</div> <div>TRUE</div> <div>(Need to add 8 GND Tps)</div> </div> <div> <div>J3700: SSD Connector</div> <div> <div>FUNC_TEST</div> <div>PP3V3 S0SW SSD FLT (Need 5 Tps)</div> <div>30</div> <div>TRUE</div> <div>PCIE SSD R2D N&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PCIE SSD R2D P&lt;3..0&gt;</div> <div>39 65</div> <div>TRUE</div> <div>PP3V3 S0</div> <div>40 41 42 43 54 57 59</div> <div>TRUE</div> <div>SSD RESET_CONN L</div> <div>26 30 34 35 37 38 39</div> <div>TRUE</div> <div>SSD_CLKREQ_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_R2D_CONN L</div> <div>30</div> <div>TRUE</div> <div>SMC_00B1_D2R_CONN L</div> <div>30</div> <div>TRUE</div> <div>SSD_PCIE_SEL L</div> <div>30</div> <div>TRUE</div> <div>SSD_SR_EN L</div> <div>15 30</div> <div>TRUE</div> <div>SMC_PWRFAIL_WARN L</div> <div>30 35</div> <div>TRUE</div> <div>SSD_PWR_EN</div> <div>15 30 56 57</div> <div>TRUE</div> <div>PCIE SSD D2R N&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE SSD D2R P&lt;3..0&gt;</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE_CLK100M SSD N</div> <div>12 30 65</div> <div>TRUE</div> <div>PCIE_CLK100M SSD P</div> <div>12 30 65</div> <div>TRUE</div> <div>(Need to add 6 GND Tps)</div> </div> <div> <div>J4902: Camera Connector</div> <div> <div>FUNC_TEST</div> <div>MIPI_CLK_CONN N</div> <div>32 70</div> <div>TRUE</div> <div>MIPI_CLK_CONN P</div> <div>32 70</div> <div>TRUE</div> <div>CAM_SENSOR_WAKE_L_CONN</div> <div>32</div> <div>TRUE</div> <div>MIPI_DATA_CONN N</div> <div>32 70</div> <div>TRUE</div> <div>MIPI_DATA_CONN P</div> <div>32 70</div> <div>TRUE</div> <div>SMBUS_SMC_1_S0_SDA</div> <div>14 32 35 38 41 42 67</div> <div>TRUE</div> <div>SMBUS_SMC_1_S0_SCL</div> <div>71</div> <div>TRUE</div> <div>I2C_CAM_SCK</div> <div>31 32</div> <div>TRUE</div> <div>I2C_CAM_SDA</div> <div>31 32</div> <div>TRUE</div> <div>PP5V_S3RS0_ALSCAM_F (Need 2 Tps)</div> <div>32</div> <div>TRUE</div> <div>(Need to add 2 GND Tps)</div> </div> </div> <div> <div>J6100: LPC+SPI Connector</div> <div> <div>FUNC_TEST</div> <div>SPI_ALT_I03_HOLD_L</div> <div>44</div> <div>TRUE</div> <div>SPI_ALT_I02_WP_L</div> <div>44</div> <div>TRUE</div> <div>LPC_AD&lt;3..0&gt;</div> <div>14 35 67</div> <div>TRUE</div> <div>SPI_ALT_I00_M0SI</div> <div>44</div> <div>TRUE</div> <div>XPDI_LPCPLUS_GPI0</div> <div>15 16</div> <div>TRUE</div> <div>LPCPLUS_RESET_L</div> <div>67</div> <div>TRUE</div> <div>SMC_TDO</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_TRST_L</div> <div>35 36</div> <div>TRUE</div> <div>TP_SMC_MD1</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TX_L</div> <div>35 36</div> <div>TRUE</div> <div>SPI_ALT_I01_MISO</div> <div>44</div> <div>TRUE</div> <div>LPC_FRAME_L</div> <div>14 35 67</div> <div>TRUE</div> <div>SPIROM_USE_MLB</div> <div>15 44</div> <div>TRUE</div> <div>PM_CLKRUN_L</div> <div>13 35</div> <div>TRUE</div> <div>SPI_ALT_CLK</div> <div>44</div> <div>TRUE</div> <div>SPI_ALT_CS_L</div> <div>44</div> <div>TRUE</div> <div>LPC_SERIRQ</div> <div>15 35</div> <div>TRUE</div> <div>LPC_PWRDWN_L</div> <div>13 35</div> <div>TRUE</div> <div>SMC_TDI</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TCK</div> <div>35 36 44</div> <div>TRUE</div> <div>SMC_RESET_L</div> <div>35 36 44 48</div> <div>TRUE</div> <div>SMC_ROMBOOT</div> <div>35 36</div> <div>TRUE</div> <div>SMC_RX_L</div> <div>35 36</div> <div>TRUE</div> <div>SMC_TMS</div> <div>35 36 44</div> <div>TRUE</div> <div>(Need to add 6 GND Tps)</div> </div> </div> <div> <div>J6900: Fan Connector</div> <div> <div>FUNC_TEST</div> <div>PP5V_S0</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_TACH</div> <div>43</div> <div>TRUE</div> <div>FAN_RT_PWM</div> <div>43</div> <div>TRUE</div> <div>(Need to add 1 GND TP)</div> </div> <div> <div>J4800: IPD Flex Connector</div> <div> <div>FUNC_TEST</div> <div>SMC_LID</div> <div>34 35 36 46</div> <div>TRUE</div> <div>TPAD_SPI_MISO_R</div> <div>34</div> <div>TRUE</div> <div>USB_TPAD_P</div> <div>14 34 66</div> <div>TRUE</div> <div>USB_TPAD_N</div> <div>14 34 66</div> <div>TRUE</div> <div>TPAD_SPI_CLK_R</div> <div>34</div> <div>TRUE</div> <div>TPAD_WAKE_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_M0SI_R</div> <div>34</div> <div>TRUE</div> <div>PP3V3_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_CS_R_L</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>TPAD_SPI_INT_S4_WAKE_L_CONN</div> <div>34</div> <div>TRUE</div> <div>PP5V_S4_IPD</div> <div>34</div> <div>TRUE</div> <div>TPAD_USB_IF_EN_CONN</div> <div>34</div> <div>TRUE</div> <div>SMBUS_SMC_3_SDA</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMBUS_SMC_3_SCL</div> <div>34 35 38 42 71</div> <div>TRUE</div> <div>SMC_LS0C_RST_L</div> <div>34 36</div> <div>TRUE</div> <div>PP3V42_G3H</div> <div>17 39 33 34 35 36 38 44 46 47</div> <div>TRUE</div> <div>SMC_ONOFF_L</div> <div>48 57 59 60 62 63</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J7000: DC-In Connector</div> <div> <div>FUNC_TEST</div> <div>PPDCIN_G3H (Need 4 Tps)</div> <div>47 48 60 62</div> <div>TRUE</div> <div>PP5V_S4RS3 (Need 3 Tps)</div> <div>32 33 45 47 52 53 56 60</div> <div>TRUE</div> <div>(Need to add 5 GND Tps)</div> </div> <div> <div>J6404: Speaker Connector</div> <div> <div>FUNC_TEST</div> <div>SPKRAMP_ROUT_P</div> <div>45 72</div> <div>TRUE</div> <div>SPKRAMP_ROUT_N</div> <div>45 72</div> <div>TRUE</div> <div>(Need to add 3 GND Tps)</div> </div> <div> <div>J6950: Battery Connector</div> <div> <div>FUNC_TEST</div> <div>PPVBAT_G3H_CONN (Need 4 Tps)</div> <div>46 48</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SCL</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SMBUS_SMC_5_G3_SDA</div> <div>35 38 46 48 71</div> <div>TRUE</div> <div>SYS_DETECT_L</div> <div>46</div> <div>TRUE</div> <div>(Need to add 4 GND Tps near J7050 and 1 for shield)</div> </div> <div> <div>J8300: Internal DP Connector</div> <div> <div>FUNC_TEST</div> <div>PPHV_S0SW_LCDBKLT (Need 2 Tps)</div> <div>54 58 60</div> <div>TRUE</div> <div>LED_RETURN_6</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_5</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_4</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_3</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_2</div> <div>54 58</div> <div>TRUE</div> <div>LED_RETURN_1</div> <div>54 58</div> <div>TRUE</div> <div>DP_INT_HPD_CONN</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SDA_R</div> <div>58</div> <div>TRUE</div> <div>I2C_TCON_SCL_R</div> <div>58</div> <div>TRUE</div> <div>PP3V3_S0SW_LCD_UF (Need 2 Tps)</div> <div>58</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_N</div> <div>58 65</div> <div>TRUE</div> <div>DP_INT_AUX_CH_C_P</div> <div>58 65</div></div></div></div></div></div></div></div></div></div></div> |   |   |   |   |   |   |   |

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|   | Functional Test Points                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 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|   | J3501: AirPort / BT Connector                                                                                                                                                                                                                                                                                                                                                                                                                                                    | J6000: Fan Connector                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | Misc Voltages & Control Signals                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | NO_TEST Nets                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |   |   |   |   |         |
| D | <p>FUNC_TEST</p> <p>PP3V3 WLAN (Need 6 Tps) 29 35 36 37 39</p> <p>WIFI EVENT L 29 35 36</p> <p>PCIE AP R2D N 29 67</p> <p>PCIE AP R2D P 29 67</p> <p>PCIE CLK100M AP N 12 29 67</p> <p>PCIE CLK100M AP P 12 29 67</p> <p>PCIE AP D2R P 14 29 67</p> <p>PCIE AP D2R N 14 29 67</p> <p>PCIE_WAKE L 13 29 31</p> <p>AP_RESET_CONN L 29</p> <p>AP_CLKREQ_O_L 29</p> <p>USB_BT_CONN_P 29 66</p> <p>USB_BT_CONN_N 29 66</p> <p>PP3V3_S4 29 34 36 37</p> <p>(Need to add 8 GND TPs)</p> | <p>FUNC_TEST</p> <p>PP5V_S0 29 35 36 37 39</p> <p>FAN_RT_TACH 43</p> <p>FAN_RT_PWM 43</p> <p>(Need to add 1 GND TP)</p> <p>J4800: IPD Flex Connector</p> <p>SMT_LID 34 35 36 46</p> <p>TPAD_SPI_MISO_R 34</p> <p>USB_TPAD_P 14 34 66</p> <p>USB_TPAD_N 14 34 66</p> <p>TPAD_SPI_CLK_R 34</p> <p>TPAD_WAKE_L 34</p> <p>TPAD_SPI_MOSI_R 34</p> <p>PP3V3_S4_IPD 34</p> <p>TPAD_SPI_CS_R_L 34</p> <p>TPAD_SPI_IF_EN_CONN 34</p> <p>TPAD_SPI_INT_S4_WAKE_L_CONN 34</p> <p>PP5V_S4_IPD 34</p> <p>TPAD_USB_IF_EN_CONN 34</p> <p>SMBUS_SMC_3_SDA 34 35 38 42 71</p> <p>SMBUS_SMC_3_SCL 34 35 38 42 71</p> <p>PP3V42_G3H 17 39 33 34 35 36 38 44 46 47</p> <p>SMC_ONOFF_L 34 35 36</p> <p>(Need to add 5 GND TPs)</p> <p>J7000: DC-In Connector</p> <p>PPDCIN_G3H (Need 4 Tps) 47 48 60 62</p> <p>PP5V_S4RS3 (Need 3 Tps) 32 33 45 47 52 53 56 60</p> <p>(Need to add 5 GND TPs)</p> <p>J6404: Speaker Connector</p> <p>SPKRAMP_ROUT_P 45 72</p> <p>SPKRAMP_ROUT_N 45 72</p> <p>(Need to add 3 GND TPs)</p> <p>J6950: Battery Connector</p> <p>PPVBAT_G3H_CONN (Need 4 Tps) 46 48</p> <p>SMBUS_SMC_5_G3_SCL 35 38 46 48 71</p> <p>SMBUS_SMC_5_G3_SDA 35 38 46 48 71</p> <p>SYS_DETECT_L 46</p> <p>(Need to add 4 GND TPs near J7050 and 1 for shield)</p> <p>J8300: Internal DP Connector</p> <p>PPHV_S0SW_LCDBKLT (Need 2 Tps) 54 58 60</p> <p>LED_RETURN_6 54 58</p> <p>LED_RETURN_5 54 58</p> <p>LED_RETURN_4 54 58</p> <p>LED_RETURN_3 54 58</p> <p>LED_RETURN_2 54 58</p> <p>LED_RETURN_1 54 58</p> <p>DP_INT_HPD_CONN 58</p> <p>I2C_TCON_SDA_R 58</p> <p>I2C_TCON_SCL_R 58</p> <p>PP3V3_S0SW_LCD_UF (Need 2 Tps) 58</p> <p>DP_INT_AUX_CH_C_N 58 65</p> <p>DP_INT_AUX_CH_C_P 58 65</p> <p>DP_INT_ML_P&lt;0&gt; 58 65</p> <p>DP_INT_ML_N&lt;0&gt; 58 65</p> <p>(Need to add 5 GND TPs)</p> <p>J7715: KB BKLT Connector</p> <p>KBDLED_ANODE 54</p> <p>KBDLED_FB 54</p> <p>(Need to add 2 GND TPs)</p> <p>J1800: XDP Connector (Only a subset are needed for FCT HVM test fixture)</p> <p>XDP_CPU_TCK 6 16 65</p> <p>XDP_PCH_TCK 12 16 67</p> <p>XDP_CPU_TDI 6 16 65</p> <p>XDP_CPU_TDO 6 16 65</p> <p>XDP_CPUPCH_TRST_L 6 12 16 65</p> <p>XDP_CPU_TMS 6 16 65</p> <p>XDP_PCH_TMS 12 16 67</p> <p>XDP_PCH_TDI 12 16 67</p> <p>XDP_PCH_TDO 12 16 67</p> <p>XDP_CPU_PREQ_L 6 16 65</p> <p>XDP_CPU_PRDY_L 6 16 65</p> <p>XDP_CPU_VCCST_PWRGD 16</p> <p>PM_RSMRST_L 13 57</p> <p>XDP_SYS_PWROK 16</p> <p>PM_SYSRST_L 13 17 35</p> <p>CPU_CFG&lt;3&gt; 6 16 65</p> <p>PP1V05_S0 6 8 11 15 16 17 36 40 49 53 56 57 60 62</p> <p>(Need to add 2 GND TPs)</p> | <p>FUNC_TEST</p> <p>PPBUS_G3H 27 39 40 47 48 54 60</p> <p>PPVIN_S4SW_TBFBST_FET 27 60</p> <p>PPBUS_SS_HS_COMPUTING_ISNS 39 49 50 51 53 60</p> <p>PPDCIN_G3H 47 48 60 62</p> <p>PP3V42_G3H 17 39 33 34 35 36 38 44 46 47</p> <p>PPVRTC_G3H 48 57 59 60 62 63</p> <p>PP3V3_S5 8 11 12 15 16 17 18 20 29 40 52</p> <p>PP3V3_SUS 8 11 14 18 44 50 56 57 60</p> <p>PP3V3_S3 15 18 19 34 38 39 56 60 63</p> <p>PP3V3_S0 60 62 63 72</p> <p>PP3V3_S0SW SSD 57 13 34 38 40 51 52 53 54 55 56 57 60</p> <p>PP1V5_S0 8 55 56 57 60</p> <p>PP1V05_S0 8 9 10 11 15 16 17 36 40 49 53 56</p> <p>PP15V_TBT 27 28 60</p> <p>PP3V3_TBTLIC 17 18 25 26 60</p> <p>PP1V05_TBT 26</p> <p>PPVCSC_S0_CPU 8 10 40 50 60</p> <p>PP1V05_TBTCIO 26 60</p> <p>PPBUS_SS_HS_OTHER_ISNS 39 52 60</p> <p>PPDCIN_G3H_ISOL 40 47 48 60</p> <p>PP3V3_S4 25 26 27 29 34 36 37 56 60 62</p> <p>(Need to add 27 GND TPs)</p> | <p>NO_TEST MAKE_BASE</p> <p>NC_PCIE_CLK100M_SDP 62</p> <p>NC_PCIE_CLK100M_SDN 62</p> <p>NC_PCIE_CLK100M_FWP 12 62</p> <p>NC_PCIE_CLK100M_FWN 12 62</p> <p>NC_PCIE_FW_D2RP 14 62</p> <p>NC_PCIE_FW_D2RN 14 62</p> <p>NC_PCIE_FW_R2D_CP 14 62</p> <p>NC_PCIE_FW_R2D_CN 14 62</p> <p>NC_USB_IRP 14 62</p> <p>NC_USB_IRN 14 62</p> <p>NC_USB_CAMERAP 14 62</p> <p>NC_USB_CAMERAN 14 62</p> <p>NC_USB_SDP 14 62</p> <p>NC_USB_SDN 14 62</p> <p>DP_INT_ML_C_P&lt;3...1&gt; 5</p> <p>DP_INT_ML_C_N&lt;3...1&gt; 5</p> <p>NC_HDA_SDIN1 12 62</p> <p>NC_PCI_PME_L 13 62</p> <p>NC_CLINK_CLK 14 62</p> <p>NC_CLINK_DATA 14 62</p> <p>NC_CLINK_RESET_L 14 62</p> <p>NC_SMC_SYS_LED 35 62</p> <p>NC_IR_RX_OUT_RC 62</p> <p>NC_USB_SMCP 62</p> <p>NC_USB_SMCN 62</p> <p>NC_SMC_GFX_OVERTEMP 35 62</p> <p>NC_SMC_GFX_THROTTLE_L 35 62</p> <p>NC_SMC_FAN_1_CTL 35 62</p> <p>NC_SMC_FAN_1_TACH 35 62</p> <p>NC_SMC_FAN_5_CTL 35 62</p> <p>NC_ENET_ASF_GPIO 62</p> <p>NC_SMC_MPMS_LED_PWR 62</p> <p>NC_SMC_MPMS_LED_CHG 62</p> <p>NC_SMC_T25_EN_L 35 62</p> <p>NC_SMC_DP_HPD_L 35 62</p> <p>NC_SMBUS_SMC_4_ASF_SCL 35 62</p> <p>NC_SMBUS_SMC_4_ASF_SDA 35 62</p> <p>NC_BDV_BKL_PWM 35 62</p> <p>TBT_B_R2D_C_P&lt;1..0&gt; 25</p> <p>TBT_B_R2D_C_N&lt;1..0&gt; 25</p> <p>TBT_B_D2R_P&lt;1..0&gt; 25</p> <p>TBT_B_D2R_N&lt;1..0&gt; 25</p> <p>NC_TBT_B_LSTX 25 62</p> <p>NC_DP_TBTPB_ML_CP&lt;3...1:2&gt; 25 62</p> <p>NC_DP_TBTPB_ML_CN&lt;3...1:2&gt; 25 62</p> <p>NC_DP_TBTPB_AUXCH_CP 25 62</p> <p>NC_DP_TBTPB_AUXCH_CN 25 62</p> <p>TP_DP_TBTSRC_ML_CP&lt;3&gt; 25</p> <p>TP_DP_TBTSRC_ML_CN&lt;3&gt; 25</p> <p>TP_DP_TBTSRC_ML_CP&lt;2&gt; 25</p> <p>TP_DP_TBTSRC_ML_CN&lt;2&gt; 25</p> <p>NC_DP_TBTSRC_ML_CP&lt;1&gt; 25 62</p> <p>NC_DP_TBTSRC_ML_CN&lt;1&gt; 25 62</p> <p>TP_DP_TBTSRC_ML_CP&lt;0&gt; 25</p> <p>TP_DP_TBTSRC_ML_CN&lt;0&gt; 25</p> <p>NC_DP_TBTSRC_AUXCH_CP 25 62</p> <p>NC_DP_TBTSRC_AUXCH_CN 25 62</p> |   |   |   |   | CPU/PCH |
| C | <p>J3700: SSD Connector</p> <p>PP3V3_S0SW SSD FLT (Need 5 Tps) 30</p> <p>PCIE SSD_R2D_N&lt;3..0&gt; 30 65</p> <p>PCIE SSD_R2D_P&lt;3..0&gt; 30 65</p> <p>PP3V3_S0 40 41 </p>                                                                                                                                                                                                                                                                                                     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          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|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
|---------------------------------------------------------------------------|--|-------------|-----------------------|--------------------|--|--------------------|--|------------------------|--|----------------------|--|-------------------------|--|-----------------|--|
| 8                                                                         |  | 7           |                       | 6                  |  | 5                  |  | 4                      |  | 3                    |  | 2                       |  | 1               |  |
| J41/J43 Board-Specific Spacing & Physical Constraints                     |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| BOARD LAYERS                                                              |  |             |                       |                    |  |                    |  | BOARD AREAS            |  |                      |  | BOARD UNITS (MIL OR MM) |  | ALLEGRO VERSION |  |
| TOP, ISL2, ISL3, ISL4, ISL5, ISL6, ISL7, ISL8, ISL9, ISL10, ISL11, BOTTOM |  |             |                       |                    |  |                    |  | NO_TYPE, BGA, MEM_TERM |  |                      |  | MM                      |  | 16.2            |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| DEFAULT                                                                   |  | TOP, BOTTOM | Y                     | =50_OHM_SE         |  | =50_OHM_SE         |  |                        |  |                      |  |                         |  |                 |  |
| DEFAULT                                                                   |  | ISL2, ISL11 | Y                     | =45_OHM_SE         |  | =45_OHM_SE         |  |                        |  |                      |  |                         |  |                 |  |
| DEFAULT                                                                   |  | ISL3, ISL10 | Y                     | =45_OHM_SE         |  | =45_OHM_SE         |  |                        |  |                      |  |                         |  |                 |  |
| DEFAULT                                                                   |  | ISL4, ISL9  | Y                     | =45_OHM_SE         |  | =45_OHM_SE         |  |                        |  |                      |  |                         |  |                 |  |
| DEFAULT                                                                   |  | *           | N                     | 100 MM             |  | 100 MM             |  | 10 MM                  |  | 0 MM                 |  | 0 MM                    |  |                 |  |
| STANDARD                                                                  |  | *           | =DEFAULT              | =DEFAULT           |  | =DEFAULT           |  | =DEFAULT               |  | =DEFAULT             |  | =DEFAULT                |  |                 |  |
| Single-ended Physical Constraints                                         |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 27P4_OHM_SE                                                               |  | TOP, BOTTOM | Y                     | 0.310 MM           |  | 0.310 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL2, ISL11 | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL3, ISL10 | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL4, ISL9  | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 35_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.195 MM           |  | 0.195 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 40_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.170 MM           |  | 0.170 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.096 MM           |  | 0.096 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.096 MM           |  | 0.096 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.099 MM           |  | 0.099 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 45_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.135 MM           |  | 0.135 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.075 MM           |  | 0.075 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.075 MM           |  | 0.075 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.080 MM           |  | 0.080 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 50_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.110 MM           |  | 0.110 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 50_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 55_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.090 MM           |  | 0.090 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 55_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| Differential Pair Physical Constraints                                    |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 70_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.165 MM           |  | 0.165 MM           |  |                        |  | 0.110 MM             |  | 0.110 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.100 MM             |  | 0.100 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.100 MM             |  | 0.100 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.110 MM           |  | 0.110MM            |  |                        |  | 0.095 MM             |  | 0.095 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 80_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.132 MM           |  | 0.132 MM           |  |                        |  | 0.130 MM             |  | 0.130 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.081 MM           |  | 0.081 MM           |  |                        |  | 0.115 MM             |  | 0.115 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.081 MM           |  | 0.081 MM           |  |                        |  | 0.115 MM             |  | 0.115 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.088 MM           |  | 0.088 MM           |  |                        |  | 0.110 MM             |  | 0.110 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 90_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.115 MM           |  | 0.115 MM           |  |                        |  | 0.200 MM             |  | 0.200 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.076 MM           |  | 0.076 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 73_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.150 MM             |  | 0.150 MM                |  |                 |  |
| 73_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.100 MM           |  | 0.100 MM           |  |                        |  | 0.150 MM             |  | 0.150 MM                |  |                 |  |
| 73_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.100 MM           |  | 0.100 MM           |  |                        |  | 0.150 MM             |  | 0.150 MM                |  |                 |  |
| 73_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.110 MM           |  | 0.110 MM           |  |                        |  | 0.150 MM             |  | 0.150 MM                |  |                 |  |
| 73_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 85_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.120 MM           |  | 0.120 MM           |  |                        |  | 0.150 MM             |  | 0.150 MM                |  |                 |  |
| 85_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.078 MM           |  | 0.078 MM           |  |                        |  | 0.160 MM             |  | 0.160 MM                |  |                 |  |
| 85_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.078 MM           |  | 0.078 MM           |  |                        |  | 0.160 MM             |  | 0.160 MM                |  |                 |  |
| 85_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.082 MM           |  | 0.082 MM           |  |                        |  | 0.140 MM             |  | 0.140 MM                |  |                 |  |
| 85_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 90_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.115 MM           |  | 0.115 MM           |  |                        |  | 0.200 MM             |  | 0.200 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.076 MM           |  | 0.076 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 27P4_OHM_SE                                                               |  | TOP, BOTTOM | Y                     | 0.310 MM           |  | 0.310 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL2, ISL11 | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL3, ISL10 | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | ISL4, ISL9  | Y                     | 0.182 MM           |  | 0.182 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 27P4_OHM_SE                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 35_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.195 MM           |  | 0.195 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.125 MM           |  | 0.125 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 35_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 40_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.170 MM           |  | 0.170 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.096 MM           |  | 0.096 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.096 MM           |  | 0.096 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.099 MM           |  | 0.099 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 40_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 45_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.135 MM           |  | 0.135 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL2, ISL11 | Y                     | 0.075 MM           |  | 0.075 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL3, ISL10 | Y                     | 0.075 MM           |  | 0.075 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | ISL4, ISL9  | Y                     | 0.080 MM           |  | 0.080 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 45_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 50_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.110 MM           |  | 0.110 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 50_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 55_OHM_SE                                                                 |  | TOP, BOTTOM | Y                     | 0.090 MM           |  | 0.090 MM           |  |                        |  |                      |  |                         |  |                 |  |
| 55_OHM_SE                                                                 |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| Differential Pair Physical Constraints                                    |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 70_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.165 MM           |  | 0.165 MM           |  |                        |  | 0.110 MM             |  | 0.110 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.100 MM             |  | 0.100 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.100 MM             |  | 0.100 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.110 MM           |  | 0.110MM            |  |                        |  | 0.095 MM             |  | 0.095 MM                |  |                 |  |
| 70_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 80_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.132 MM           |  | 0.132 MM           |  |                        |  | 0.130 MM             |  | 0.130 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.081 MM           |  | 0.081 MM           |  |                        |  | 0.115 MM             |  | 0.115 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.081 MM           |  | 0.081 MM           |  |                        |  | 0.115 MM             |  | 0.115 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.088 MM           |  | 0.088 MM           |  |                        |  | 0.110 MM             |  | 0.110 MM                |  |                 |  |
| 80_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 90_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.115 MM           |  | 0.115 MM           |  |                        |  | 0.200 MM             |  | 0.200 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL2, ISL11 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL3, ISL10 | Y                     | 0.070 MM           |  | 0.070 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | ISL4, ISL9  | Y                     | 0.076 MM           |  | 0.076 MM           |  |                        |  | 0.180 MM             |  | 0.180 MM                |  |                 |  |
| 90_OHM_DIFF                                                               |  | *           | N                     | 100 MM             |  | 100 MM             |  | =STANDARD              |  | =STANDARD            |  | =STANDARD               |  |                 |  |
|                                                                           |  |             |                       |                    |  |                    |  |                        |  |                      |  |                         |  |                 |  |
| PHYSICAL_RULE_SET                                                         |  | LAYER       | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH |  | MINIMUM NECK WIDTH |  | MAXIMUM NECK LENGTH    |  | DIFFPAIR PRIMARY GAP |  | DIFFPAIR NECK GAP       |  |                 |  |
| 73_OHM_DIFF                                                               |  | TOP, BOTTOM | Y                     | 0.105 MM           |  | 0.105 MM           |  |                        |  | 0.150 MM             |  |                         |  |                 |  |



## CPU Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CPU_45S           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |
| CPU_27P4S         | *     | =27P4_OHM_SE          | =27P4_OHM_SE       | =27P4_OHM_SE       | =27P4_OHM_SE        | 0.100 MM             | 0.100 MM          |

| SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------------|----------------------|--------|
| CPU_AGTL         | TOP, BOTTOM | =2x_DIELECTRIC       | ?      |
| CPU_AGTL         | *           | =STANDARD            | ?      |

Note: CPU\_8MIL and CPU\_ITP can be converted  
back to TABLE\_SPACING\_RULE  
once rdar://10308147 is resolved

|                   |                   |           |                  |
|-------------------|-------------------|-----------|------------------|
| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
| CPU_8MIL          | *                 | *         | CPU_8MIL_2ANY    |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_8MIL_2ANY    | *     | 8 MIL                | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CPU_ITP           | *                 | *         | CPU_ITP_ZANY     |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_ITP_2ANY     | *     | =4x_DIELECTRIC       | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SEQUENCE |
|-------------------|-------------------|-----------|-----------------------|
| CPU_COMP          | CPU_COMP          | *         | CPU_COMP_2SELF        |
| CPU_COMP          | *                 | *         | CPU_COMP_20OTHER      |

| SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------------|----------------------|--------|
| CPU_COMP_2SELF   | TOP, BOTTOM | =6x_DIELECTRIC       | ?      |
| CPU_COMP_20THER  | TOP, BOTTOM | =10x_DIELECTRIC      | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CPU_COMP_2SELF   | *     | =4x_DIELECTRIC       | ?      |
| CPU_COMP_20THER  | *     | =6x_DIELECTRIC       | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET     |
|-------------------|-------------------|-----------|----------------------|
| CPU_VCCSENSE      | CPU_VCCSENSE      | *         | CPU_VCCSENSE_2SELF   |
| CPU_VCCSENSE      | *                 | *         | CPU_VCCSENSE_20OTHER |

| SPACING_RULE_SET    | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|---------------------|-------------|----------------------|--------|
| CPU_VCCSENSE_2SELF  | TOP, BOTTOM | =6x_DIELECTRIC       | ?      |
| CPU_VCCSENSE_20THER | TOP, BOTTOM | =10x_DIELECTRIC      | ?      |

| SPACING_RULE_SET    | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|---------------------|-------|----------------------|--------|
| CPU_VCCSENSE_2SELF  | *     | =4x_DIELECTRIC       | ?      |
| CPU_VCCSENSE_20THER | *     | =6x_DIELECTRIC       | ?      |

## PCI-Express Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCIE_800          | *     | =B0_OHM_DIFF          | =B0_OHM_DIFF       | =B0_OHM_DIFF       | =B0_OHM_DIFF        | =B0_OHM_DIFF         | =B0_OHM_DIFF      |
| CLK_PCIE_800      | *     | =B0_OHM_DIFF          | =B0_OHM_DIFF       | =B0_OHM_DIFF       | =B0_OHM_DIFF        | =B0_OHM_DIFF         | =B0_OHM_DIFF      |

## PCIE Clock Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CLK_PCIE          | CLK_PCIE          | *         | CLK_PCIE_2SELF   |
| CLK_PCIE          | *                 | *         | CLK_PCIE_20THER  |

| SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------------|----------------------|--------|
| CLK_PCIE_2SELF   | TOP, BOTTOM | =6x_DIELECTRIC       | ?      |
| CLK_PCIE_20THER  | TOP, BOTTOM | =10x_DIELECTRIC      | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_PCIE_2SELF   | *     | =4x_DIELECTRIC       | ?      |
| CLK_PCIE_20THER  | *     | =6x_DIELECTRIC       | ?      |

## CPU PCIe Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| PCIE_CPU_TX       | PCIE_CPU_TX       | *         | PCIE_TX2TX       |
| PCIE_CPU_RX       | PCIE_CPU_RX       | *         | PCIE_RX2RX       |
| PCIE_CPU_TX       | *_CPU_TX          | *         | PCIE_TX20THERTX  |
| PCIE_CPU_RX       | *_CPU_RX          | *         | PCIE_RX20THERRX  |
| PCIE_CPU_TX       | *_CPU_RX          | *         | PCIE_TX2RX       |
| PCIE_CPU_RX       | *_CPU_TX          | *         | PCIE_RX2TX       |
| PCIE_CPU_TX       | *_TX              | *         | PCIE_20THERHS    |
| PCIE_CPU_RX       | *_TX              | *         | PCIE_20THERHS    |
| PCIE_CPU_TX       | *_RX              | *         | PCIE_20THERHS    |
| PCIE_CPU_RX       | *_RX              | *         | PCIE_20THERHS    |
| PCIE_CPU_TX       | *                 | *         | PCIE_20THER      |
| PCIE_CPU_RX       | *                 | *         | PCIE_20THER      |

| SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|------------|----------------------|--------|
| PCIE_TX2TX       | TOP_BOTTOM | =5x_DIELECTRIC       | ?      |
| PCIE_RX2RX       | TOP_BOTTOM | =5x_DIELECTRIC       | ?      |
| PCIE_TX20THERTX  | TOP_BOTTOM | =5x_DIELECTRIC       | ?      |
| PCIE_RX20THERRX  | TOP_BOTTOM | =5x_DIELECTRIC       | ?      |
| PCIE_TX2RX       | TOP_BOTTOM | =7x_DIELECTRIC       | ?      |
| PCIE_RX2TX       | TOP_BOTTOM | =7x_DIELECTRIC       | ?      |
| PCIE_20THERHS    | TOP_BOTTOM | =6x_DIELECTRIC       | ?      |
| PCIE_20THER      | TOP_BOTTOM | =5x_DIELECTRIC       | ?      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCIE_TX2TX       | "     | =2.5x_DIELECTRIC     | ?      |
| PCIE_RX2RX       | "     | =2.5x_DIELECTRIC     | ?      |
| PCIE_TX20THERTX  | "     | =4x_DIELECTRIC       | ?      |
| PCIE_RX20THERRX  | "     | =4x_DIELECTRIC       | ?      |
| PCIE_TX2RX       | "     | =6x_DIELECTRIC       | ?      |
| PCIE_RX2TX       | "     | =6x_DIELECTRIC       | ?      |
| PCIE_20THERHS    | "     | =4x_DIELECTRIC       | ?      |
| PCIE_20THER      | "     | =3x_DIELECTRIC       | ?      |

PCH PCIE Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| PCIE_PCH_TX       | PCIE_PCH_TX       | *         | PCIE_TX2TX       |
| PCIE_PCH_RX       | PCIE_PCH_RX       | *         | PCIE_RX2RX       |
| PCIE_PCH_TX       | *_PCH_TX          | *         | PCIE_TX20THERTX  |
| PCIE_PCH_RX       | *_PCH_RX          | *         | PCIE_RX20THERRX  |
| PCIE_PCH_TX       | *_PCH_RX          | *         | PCIE_TX2RX       |
| PCIE_PCH_RX       | *_PCH_TX          | *         | PCIE_RX2TX       |
| PCIE_PCH_TX       | *_TX              | *         | PCIE_20THERHS    |
| PCIE_PCH_RX       | *_TX              | *         | PCIE_20THERHS    |
| PCIE_PCH_TX       | *_RX              | *         | PCIE_20THERHS    |
| PCIE_PCH_RX       | *_RX              | *         | PCIE_20THERHS    |
| PCIE_PCH_TX       | *                 | *         | PCIE_20THER      |
| PCIE_PCH_RX       | *                 | *         | PCIE_20THER      |

|                 |   |                |   |
|-----------------|---|----------------|---|
| PCIE_RX20THERRX | * | =4x_DIELECTRIC | ? |
| PCIE_TX2RX      | * | =6x_DIELECTRIC | ? |
| PCIE_RX2TX      | * | =6x_DIELECTRIC | ? |
| PCIE_20THERHS   | * | =4x_DIELECTRIC | ? |
| PCIE_20THER     | * | =3x_DIELECTRIC | ? |

Note: DisplayPort tables are on Page 113

SOURCE: 471984\_Chief\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## CPU Net Properties

| ELECTRICAL_CONSTRAINT_SET                                                             |                  | NET_TYPE        |              |                                 |
|---------------------------------------------------------------------------------------|------------------|-----------------|--------------|---------------------------------|
|                                                                                       |                  | PHYSICAL        | SPACING      |                                 |
|    | CPU_PECT         | CPU_45S         | CPU_COMP     | CPU_PECT 6 36                   |
|    | PM_SYNC          | CPU_45S         | CPU_AGT1     | PM_SYNC                         |
|    | PM_MEM_PWRGD     | CPU_45S         | CPU_AGT1     | PM_MEM_PWRGD                    |
|    |                  | CPU_45S         | CPU_ITP      | XDP_DBRESET_L 16 17             |
|    |                  | CPU_45S         | CPU_ITP      | XDP_CPU_PRODY_L 6 16 62         |
|    |                  | CPU_45S         | CPU_ITP      | XDP_CPU_PREQ_L 6 16 62          |
|    |                  | CPU_27PA5       | CPU_COMP     | EDP_COMP                        |
|    |                  | CPU_27PA5       | CPU_COMP     | CPU_PEG_COMP                    |
|    | CPU_SM_RCOMP     | CPU_27PA5       | CPU_COMP     | CPU_SM_RCOMP<0> 6               |
|    | CPU_SM_RCOMP     | CPU_27PA5       | CPU_COMP     | CPU_SM_RCOMP<1> 6               |
|    | CPU_SM_RCOMP     | CPU_27PA5       | CPU_COMP     | CPU_SM_RCOMP<2> 6               |
|    |                  | CPU_45S         | CPU_ITP      | CPU_CFG<11..0> 6 16 62          |
|    | CPU_CATERR_L     | CPU_45S         | CPU_AGT1     | CPU_CATERR_L 6 35               |
|    |                  | CPU_45S         | CPU_AGT1     | CPU_VCCIO_SEL                   |
|    | CPU_PROCHOT_L    | CPU_45S         | CPU_AGT1     | CPU_PROCHOT_L 6 35 36 49        |
|    | CPU_PWRGD        | CPU_45S         | CPU_AGT1     | CPU_PWRGD 6                     |
|    | PM_THRMTRIP_L    | CPU_45S         | CPU_AGT1     | PM_THRMTRIP_L 15 36             |
|    | DMI_CLK100M      | CLK_PCTE_B0D    | CLK_PCTE     | DMI_CLK100M_CPU_P               |
|    | DMI_CLK100M      | CLK_PCTE_B0D    | CLK_PCTE     | DMI_CLK100M_CPU_N               |
|    | DPLL_REF_CLK120M | CLK_PCTE_B0D    | CLK_PCTE     | DPLL_REF_CLKP                   |
|    | DPLL_REF_CLK120M | CLK_PCTE_B0D    | CLK_PCTE     | DPLL_REF_CLKN                   |
|    | ITPCPU_CLK100M   | CLK_PCTE_B0D    | CLK_PCTE     | ITPCPU_CLK100M_P                |
|    | ITPCPU_CLK100M   | CLK_PCTE_B0D    | CLK_PCTE     | ITPCPU_CLK100M_N                |
|    | ITPXPDP_CLK100M  | CLK_PCTE_B0D    | CLK_PCTE     | ITPXPDP_CLK100M_P               |
|    | ITPXPDP_CLK100M  | CLK_PCTE_B0D    | CLK_PCTE     | ITPXPDP_CLK100M_N               |
|    | ITPCPU_CLK100M   | CLK_PCTE_B0D    | CLK_PCTE     | XDP_CPU_CLK100M_P               |
|    | ITPCPU_CLK100M   | CLK_PCTE_B0D    | CLK_PCTE     | XDP_CPU_CLK100M_N               |
|    | XDP_TDI          | CPU_45S         | CPU_ITP      | XDP_CPU_TDI 6 16 62             |
|    | XDP_TDO          | CPU_45S         | CPU_ITP      | XDP_CPU_TDO 6 16 62             |
|    | XDP_TMS          | CPU_45S         | CPU_ITP      | XDP_CPU_TMS 6 16 62             |
|   | XDP_TCK          | CPU_45S         | CPU_ITP      | XDP_CPU_TCK 6 16 62             |
|  | XDP_TRST_L       | CPU_45S         | CPU_ITP      | XDP_CPU_PCH_TRST_L 6 12 16 62   |
|  | XDP_BPM_L        | CPU_45S         | CPU_ITP      | XDP_BPM_L<1..0> 6 16            |
|  |                  | CPU_45S         | CPU_ITP      | XDP_BPM_L<7..2> 6 16            |
|  |                  | CPU_45S         | CPU_ITP      | XDP_OBSDATA_B<3..0>             |
|  | (ESB_CPUBST_L)   | CPU_45S         | CPU_ITP      | CPU_CFG<15..12> 6 16            |
|  |                  | CPU_45S         | CPU_ITP      | XDP_CPUST_L 16                  |
|  | CPU_VCCSENSE     | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_VCCSENSE_P 8 49             |
|  | CPU_VCCSENSE     | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_VCCSENSE_N 9 49             |
|  | CPU_VCCIOSENSE   | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_VCCIOSENSE_P                |
|  | CPU_VCCIOSENSE   | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_VCCIOSENSE_N                |
|  | CPU_AXG_SENSE    | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_AXG_SENSE_P                 |
|  | CPU_AXG_SENSE    | SENSE_1T01_P2MM | CPU_VCCSENSE | CPU_AXG_SENSE_N                 |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_VDDO_SENSE_P                |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_VDDO_SENSE_N                |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_AXG_VALSENSE_P              |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_AXG_VALSENSE_N              |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_VCC_VALSENSE_P              |
|  | CPU_VALSENSE     | CPU_27PA5       | CPU_VCCSENSE | CPU_VCC_VALSENSE_N              |
|  | CPU_SVIDALERT_L  | CPU_45S         | CPU_COMP     | CPU_VIDALERT_L 8 49             |
|  | CPU_SVIDSCLK     | CPU_45S         | CPU_COMP     | CPU_VIDSCLK 8 49                |
|  | CPU_SVIDSOUT     | CPU_45S         | CPU_COMP     | CPU_VIDSOUT 8 49                |
|  | PCIE_CPU_SSD_R2D | PCIE_B0D        | PCIE_CPU_TX  | PCIE_SSD_R2D_C_P<3..0> 12 38    |
|  | PCIE_CPU_SSD_R2D | PCIE_B0D        | PCIE_CPU_TX  | PCIE_SSD_R2D_C_N<3..0> 12 38    |
|  |                  | PCIE_B0D        | PCIE_CPU_TX  | PCIE_SSD_R2D_P<3..0> 38 62      |
|  |                  | PCIE_B0D        | PCIE_CPU_TX  | PCIE_SSD_R2D_N<3..0> 38 62      |
|  |                  | PCIE_B0D        | PCIE_CPU_RX  | PCIE_SSD_D2R_C_P<3..0> 12 38 62 |
|  |                  | PCIE_B0D        | PCIE_CPU_RX  | PCIE_SSD_D2R_C_N<3..0> 12 38 62 |
|  | PCIE_CPU_SSD_D2R | PCIE_B0D        | PCIE_CPU_RX  | PCIE_SSD_D2R_P<3..0> 12 38 62   |
|  | PCIE_CPU_SSD_D2R | PCIE_B0D        | PCIE_CPU_RX  | PCIE_SSD_D2R_N<3..0> 12 38 62   |
|  | PCIE_CLK100M_SSD | CLK_PCTE_B0D    | CLK_PCTE     | PCIE_CLK100M_SSD_P 12 38 62     |
|  | PCIE_CLK100M_SSD | CLK_PCTE_B0D    | CLK_PCTE     | PCIE_CLK100M_SSD_N 12 38 62     |
|  | DP_TBT_MI        | DP_B0D          | DP_TX        | DP_TBTSNK0_ML_P<3..0> 25        |
|  | DP_TBT_MI        | DP_B0D          | DP_TX        | DP_TBTSNK0_ML_N<3..0> 25        |
|  |                  | DP_B0D          | DP_TX        | DP_TBTSNK0_ML_C_P<3..0> 5 25    |
|  |                  | DP_B0D          | DP_TX        | DP_TBTSNK0_ML_C_N<3..0> 5 25    |
|  | DP_TBT_AUXCH     | DP_B0D          | DP_AUX       | DP_TBTSNK0_AUXCH_P 25           |
|  | DP_TBT_AUXCH     | DP_B0D          | DP_AUX       | DP_TBTSNK0_AUXCH_N 25           |
|  |                  | DP_B0D          | DP_AUX       | DP_TBTSNK0_AUXCH_C_P 13 25      |
|  |                  | DP_B0D          | DP_AUX       | DP_TBTSNK0_AUXCH_C_N 13 25      |
|  | DP_TBT_MI        | DP_B0D          | DP_TX        | DP_TBTSNK1_ML_P<3..0> 25        |
|  | DP_TBT_MI        | DP_B0D          | DP_TX        | DP_TBTSNK1_ML_N<3..0> 25        |
|  |                  | DP_B0D          | DP_TX        | DP_TBTSNK1_ML_C_P<3..0> 5 18    |
|  |                  | DP_B0D          | DP_TX        | DP_TBTSNK1_ML_C_N<3..0> 5 18    |
|  | DP_TBT_AUXCH     | DP_B0D          | DP_AUX       | DP_TBTSNK1_AUXCH_P 25           |
|  | DP_TBT_AUXCH     | DP_B0D          | DP_AUX       | DP_TBTSNK1_AUXCH_N 25           |
|  |                  | DP_B0D          | DP_AUX       | DP_TBTSNK1_AUXCH_C_P 13 18      |
|  |                  | DP_B0D          | DP_AUX       | DP_TBTSNK1_AUXCH_C_N 13 18      |
|  | DP_INT_MI        | DP_B0D          | DP_TX        | DP_INT_ML_P<3..0> 58 62         |
|  | DP_INT_MI        | DP_B0D          | DP_TX        | DP_INT_ML_N<3..0> 58 62         |
|  |                  | DP_B0D          | DP_TX        | DP_INT_ML_C_P<3..0> 5 58 62     |
|  |                  | DP_B0D          | DP_TX        | DP_INT_ML_C_N<3..0> 5 58 62     |
|  | DP_INT_AUXCH     | DP_B0D          | DP_AUX       | DP_INT_AUX_CH_C_P 58 62         |
|  | DP_INT_AUXCH     | DP_B0D          | DP_AUX       | DP_INT_AUX_CH_C_N 58 62         |
|  | DP_INT_AUXCH     | DP_B0D          | DP_AUX       | DP_INT_AUXCH_C_P 5 58           |
|  | DP_INT_AUXCH     | DP_B0D          | DP_AUX       | DP_INT_AUXCH_C_N 5 58           |
|  |                  | DP_B0D          | DP_AUX       | DP_INT_AUXCH_P                  |
|  |                  | DP_B0D          | DP_AUX       | DP_INT_AUXCH_N                  |

PCIe SSD

DP

|                                                                                                                                                                                                                                                                          |            |                      |      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|----------------------|------|
| SYNC MASTER=J43 MLB                                                                                                                                                                                                                                                      |            | SYNC DATE=09/21/2012 |      |
| PAGE TITLE                                                                                                                                                                                                                                                               |            |                      |      |
| CU Constraints                                                                                                                                                                                                                                                           |            |                      |      |
|                                                                                                                                                                                     | Apple Inc. | DRAWING NUMBER       | SIZE |
|                                                                                                                                                                                                                                                                          |            | <SCH_NUM>            | D    |
|                                                                                                                                                                                                                                                                          |            | REVISION             |      |
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|                                                                                                                                                                                                                                                                          |            | PAGE                 |      |
|                                                                                                                                                                                                                                                                          |            | 111 OF 120           |      |
|                                                                                                                                                                                                                                                                          |            | SHEET                |      |
|                                                                                                                                                                                                                                                                          |            | 65 OF 73             |      |

## SATA Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SATA_B0D          | *     | =B0_OHM_DIFF          | =B0_OHM_DIFF       | =B0_OHM_DIFF       | =B0_OHM_DIFF        | =B0_OHM_DIFF         | =B0_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SATA_ICOMP       | *     | =4x_DIELECTRIC       | ?      |

SOURCE: 471984\_Chief\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## UART Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| UART_45S          | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =45_OHM_SE           | =45_OHM_SE        |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| UART             | *     | =2x_DIELECTRIC       | ?      |

## USB 2.0 Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCH_USB_BIAS      | *     | =STANDARD             | 8 MIL              | 8 MIL              | =STANDARD           | =STANDARD            | =STANDARD         |
| USB_80D           | *     | =B0_OHM_DIFF          | =B0_OHM_DIFF       | =B0_OHM_DIFF       | =B0_OHM_DIFF        | =B0_OHM_DIFF         | =B0_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| USB              | *     | =2x_DIELECTRIC       | ?      | USB              | TOP,BOTTOM | =4x_DIELECTRIC       | ?      |

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905\_v1.5), Section 3.8

## USB 3.0 Interface Constraints

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET | SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|-------------------|-------------------|-----------|------------------|------------------|-------------|----------------------|--------|
| USB3_PCH_TX       | USB3_PCH_TX       | *         | USB3_TX2TX       | USB3_TX2TX       | TOP, BOTTOM | =5X_DIELECTRIC       | ?      |
| USB3_PCH_RX       | USB3_PCH_RX       | *         | USB3_RX2RX       | USB3_RX2RX       | TOP, BOTTOM | =5X_DIELECTRIC       | ?      |
| USB3_PCH_TX       | *_PCH_TX          | *         | USB3_TX20THERTX  | USB3_TX20THERTX  | TOP, BOTTOM | =5X_DIELECTRIC       | ?      |
| USB3_PCH_RX       | *_PCH_RX          | *         | USB3_RX20THERRX  | USB3_RX20THERRX  | TOP, BOTTOM | =5X_DIELECTRIC       | ?      |
| USB3_PCH_TX       | *_PCH_RX          | *         | USB3_TX2RX       | USB3_TX2RX       | TOP, BOTTOM | =7X_DIELECTRIC       | ?      |
| USB3_PCH_RX       | *_PCH_TX          | *         | USB3_RX2TX       | USB3_RX2TX       | TOP, BOTTOM | =7X_DIELECTRIC       | ?      |
| USB3_PCH_TX       | *_TX              | *         | USB3_20THERHS    | USB3_20THERHS    | TOP, BOTTOM | =6X_DIELECTRIC       | ?      |
| USB3_PCH_RX       | *_TX              | *         | USB3_20THERHS    | USB3_20THER      | TOP, BOTTOM | =5X_DIELECTRIC       | ?      |
| USB3_PCH_TX       | *_RX              | *         | USB3_20THERHS    |                  |             |                      |        |
| USB3_PCH_RX       | *_RX              | *         | USB3_20THERHS    |                  |             |                      |        |
| USB3_PCH_TX       | *                 | *         | USB3_20THER      |                  |             |                      |        |
| USB3_PCH_RX       | *                 | *         | USB3_20THER      |                  |             |                      |        |

SOURCE: 471984\_Cheif\_River\_MS\_PDG\_1.0 and the spacing rule is adjusted per SI team feedback.

## PCH Net Properties

| ELECTRICAL_CONSTRAINT_SET |                    | NET_TYPE      |             |                        |
|---------------------------|--------------------|---------------|-------------|------------------------|
|                           |                    | PHYSICAL      | SPACING     |                        |
|                           |                    |               |             |                        |
|                           | PCH_SATA_ICOMP     |               | SATA_ICOMP  | PCH_SATAICOMP          |
|                           | USB_HUB1_UP        | USB_800       | USB         | USB_HUB_UP_P           |
|                           | USB_HUB1_UP        | USB_800       | USB         | USB_HUB_UP_N           |
|                           | USB_BT             | USB_800       | USB         | USB_BT_P               |
|                           | USB_BT             | USB_800       | USB         | USB_BT_N               |
|                           |                    | USB_800       | USB         | USB_BT_CONN_P          |
|                           |                    | USB_800       | USB         | USB_BT_CONN_N          |
|                           |                    | USB_800       | USB         | USB_BT_WAKE_P          |
|                           |                    | USB_800       | USB         | USB_BT_WAKE_N          |
|                           | USB_TPAD           | USB_800       | USB         | USB_TPAD_P             |
|                           | USB_TPAD           | USB_800       | USB         | USB_TPAD_N             |
|                           |                    | USB_800       | USB         | USB_TPAD_CONN_P        |
|                           |                    | USB_800       | USB         | USB_TPAD_CONN_N        |
|                           |                    | USB_800       | USB         |                        |
|                           |                    | USB_800       | USB         | TPAD_SPT_M0SI_USB_P    |
|                           |                    | USB_800       | USB         | TPAD_SPT_MISO_USB_N    |
|                           | USB_TPAD_M         | USB_800       | USB         | USB_TPAD_M_P           |
|                           | USB_TPAD_M         | USB_800       | USB         | USB_TPAD_M_N           |
|                           | USB_SDCARD         | USB_800       | USB         | USB_SDCARD_P           |
|                           | USB_SDCARD         | USB_800       | USB         | USB_SDCARD_N           |
|                           |                    | SPT_45S       | SPT         | TPAD_SPT_M0SI          |
|                           |                    | SPT_45S       | SPT         | TPAD_SPT_MISO          |
|                           |                    | SPT_45S       | SPT         | TPAD_SPT_CLK           |
|                           |                    |               |             |                        |
|                           | USB_EXT4           | USB_800       | USB         | USB_EXT4_P             |
|                           | USB_EXT4           | USB_800       | USB         | USB_EXT4_N             |
|                           | UART4_A5S          | UART          |             | SMC_DEBUGPRT_TX_L      |
|                           | UART4_A5S          | UART          |             | SMC_DEBUGPRT_RX_L      |
|                           | USB2_EXT4          | USB_800       | USB         | USB2_EXT4_MUXED_P      |
|                           | USB2_EXT4          | USB_800       | USB         | USB2_EXT4_MUXED_N      |
|                           | USB2_EXT4          | USB_800       | USB         | USB2_EXT4_MUXED_F_P    |
|                           | USB2_EXT4          | USB_800       | USB         | USB2_EXT4_MUXED_F_N    |
|                           | USB3_EXT4_RX       | USB_800       | USB3_PCH_RX | USB3_EXT4_D2R_P        |
|                           | USB3_EXT4_RX       | USB_800       | USB3_PCH_RX | USB3_EXT4_D2R_N        |
|                           | USB3_EXT4_TX       | USB_800       | USB3_PCH_TX | USB3_EXT4_D2R_P        |
|                           | USB3_EXT4_TX       | USB_800       | USB3_PCH_TX | USB3_EXT4_D2R_N        |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_EXT4_D2R_F_P      |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_EXT4_D2R_F_N      |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXT4_R2D_F_P      |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXT4_R2D_F_N      |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXT4_R2D_C_P      |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXT4_R2D_C_N      |
|                           | USB_EXTB           | USB_800       | USB         | USB_EXTB_P             |
|                           | USB_EXTB           | USB_800       | USB         | USB_EXTB_N             |
|                           | USB3_EXTB_RX       | USB_800       | USB3_PCH_RX | USB3_EXTB_D2R_P        |
|                           | USB3_EXTB_RX       | USB_800       | USB3_PCH_RX | USB3_EXTB_D2R_N        |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_EXTB_D2R_RC_P     |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_EXTB_D2R_RC_N     |
|                           | USB3_EXTB_TX       | USB_800       | USB3_PCH_TX | USB3_EXTB_R2D_P        |
|                           | USB3_EXTB_TX       | USB_800       | USB3_PCH_TX | USB3_EXTB_R2D_N        |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXTB_R2D_C_P      |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_EXTB_R2D_C_N      |
|                           | USB3_SD_RX         | USB_800       | USB3_PCH_RX | NC_USB3RPCIE_SD_D2RP   |
|                           | USB3_SD_RX         | USB_800       | USB3_PCH_RX | NC_USB3RPCIE_SD_D2RN   |
|                           | USB3_SD_TX         | USB_800       | USB3_PCH_TX | NC_USB3RPCIE_SD_R2D_CP |
|                           | USB3_SD_TX         | USB_800       | USB3_PCH_TX | NC_USB3RPCIE_SD_R2D_CN |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_SD_D2R_C_P        |
|                           |                    | USB_800       | USB3_PCH_RX | USB3_SD_D2R_C_N        |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_SD_R2D_P          |
|                           |                    | USB_800       | USB3_PCH_TX | USB3_SD_R2D_N          |
|                           | PCH_USB_RBIAS      | PCH_USB_RBIAS |             | PCH_USB_RBIAS          |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCIE_CLK100M_PCH_P     |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCIE_CLK100M_PCH_N     |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCH_CLK96M_DOT_P       |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCH_CLK96M_DOT_N       |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCH_CLK100M_SATA_P     |
|                           | PCH_DTEFCLK_UNUSED | CLK_PCTE_800  | CLK_PCTE    | PCH_CLK100M_SATA_N     |
|                           |                    | CPU_45S       | CLK_PCTE    | PCH_CLK14P3M_REFCLK    |

## USB Hucopyb nets

TP SPI nets

USB EXTA nets (Right USB port)

USB EXTB nets (Left USB port)

|                                                                                                                                                                                                                                                                                                                             |                |                      |            |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|----------------------|------------|
| SYNC MASTER=CLEAN J41                                                                                                                                                                                                                                                                                                       |                | SYNC DATE=11/13/2012 |            |
| PAGE TITLE                                                                                                                                                                                                                                                                                                                  |                |                      |            |
| PCH Constraints 1                                                                                                                                                                                                                                                                                                           |                |                      |            |
| <br>Apple Inc.                                                                                                                                                                                                                         | DRAWING NUMBER |                      | SIZE       |
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|                                                                                                                                                                                                                                                                                                                             |                | BRANCH               |            |
|                                                                                                                                                                                                                                                                                                                             |                | <BRANCH>             |            |
|                                                                                                                                                                                                                                                                                                                             |                | PAGE                 | 112 OF 120 |
|                                                                                                                                                                                                                                                                                                                             |                | SHEET                | 66 OF 73   |

## LPC Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| LPC_45S           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |
| CLK_LPC_45S       | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| LPC              | *     | =3x_DIELECTRIC       | ?      |
| CLK_LPC          | *     | =4x_DIELECTRIC       | ?      |

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SMBus Interface Constraints

| PHYSICAL_RULE_SET | LAYER       | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SMB_45S_R_50S     | TOP, BOTTOM | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          |                      |                   |
| SMB_45S_R_50S     | *           | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SMB              | *     | =2x_DIELECTRIC       | ?      |

## HD Audio Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| HDA_455           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| HDA              | *     | =2x_DIELECTRIC       | ?      |

SOURCE: Calpella Platform Design Guide for Ixex Peak M (DG-398905-398905\_v1.5), Section 3.15

## SIO Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_SLOW_45S      | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_SLOW         | *     | =4x_DIELECTRIC       | ?      |

## SPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SPI_455           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SPI              | *     | =4x_DIELECTRIC       | ?      |

## XDP Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| PCH_455           | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| PCH_ITP          | *     | =2:1_SPACING         | ?      |

## DisplayPort

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| DP_B0D            | *     | =B0_OHM_DIFF          | =B0_OHM_DIFF       | =B0_OHM_DIFF       | =B0_OHM_DIFF        | =B0_OHM_DIFF         | =B0_OHM_DIFF      |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|-------------|----------------------|--------|
| DP_2DP           | *     | =3x_DIELECTRIC       | ?      | DP_2DP           | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| DP_20THERHS      | *     | =4x_DIELECTRIC       | ?      | DP_20THERHS      | TOP, BOTTOM | =6x_DIELECTRIC       | ?      |
| DP_20THER        | *     | =3x_DIELECTRIC       | ?      | DP_20THER        | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| DP_AUX           | *     | =3x_DIELECTRIC       | ?      | DP_AUX           | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| DP_TX             | DP_TX             | *         | DP_2DP           |
| DP_TX             | *_TX              | *         | DP_20THERHS      |
| DP_TX             | *_RX              | *         | DP_20THERHS      |
| DP_TX             | *                 | *         | DP_20THER        |

## System Clock Signal Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW_ROUTE_ON_LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| CLK_SLOW_45S      | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |
| CLK_25M_45S       | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| CLK_SLOW         | *     | =2x_DIELECTRIC       | ?      |
| CLK_25M          | *     | =5x_DIELECTRIC       | ?      |

NOTE: 25MHz system clocks very sensitive to noise.

## PCH Net Properties

| ELECTRICAL_CONSTRAINT_SET |               | NET_TYPE    |                         |
|---------------------------|---------------|-------------|-------------------------|
|                           | PHYSICAL      | SPACING     |                         |
| LPC_AD                    | LPC_45S       | LPC         | LPC_AD<3...0>           |
| LPC_FRAME_L               | LPC_45S       | LPC         | LPC_FRAME_L             |
|                           | LPC_45S       | LPC         | LPCPLUS_RESET_L         |
| LPC_CLK33M                | CLK LPC_45S   | CLK LPC     | LPC_CLK24M_SMC          |
|                           | CLK LPC_45S   | CLK LPC     | LPC_CLK24M_SMC_R        |
| LPC_CLK33M                | CLK LPC_45S   | CLK LPC     | LPC_CLK24M_LPCPLUS      |
|                           | CLK LPC_45S   | CLK LPC     | LPC_CLK24M_LPCPLUS_R    |
| SMBUS_PCH_CLK             | SMB_45S_R_50S | SMB         | SMBUS_PCH_CLK           |
| SMBUS_PCH_DATA            | SMB_45S_R_50S | SMB         | SMBUS_PCH_DATA          |
| SMBUS_PCH_0_CLK           | SMB_45S_R_50S | SMB         | SML_PCH_0_CLK           |
| SMBUS_PCH_0_DATA          | SMB_45S_R_50S | SMB         | SML_PCH_0_DATA          |
| SMBUS_SMC_1_S0_SCL        | SMB_45S_R_50S | SMB         | SMBUS_SMC_1_S0_SCL      |
| SMBUS_SMC_1_S0_SDA        | SMB_45S_R_50S | SMB         | SMBUS_SMC_1_S0_SDA      |
| HDA_BTT_CLK               | HDA_45S       | HDA         | HDA_BIT_CLK             |
|                           | HDA_45S       | HDA         | HDA_BIT_CLK_R           |
| HDA_SYNC                  | HDA_45S       | HDA         | HDA_SYNC                |
|                           | HDA_45S       | HDA         | HDA_SYNC_R              |
| HDA_RST_I                 | HDA_45S       | HDA         | HDA_RST_R_L             |
|                           | HDA_45S       | HDA         | HDA_RST_L               |
| HDA_SDIO#                 | HDA_45S       | HDA         | HDA_SDIO#               |
| HDA_SDOUT                 | HDA_45S       | HDA         | HDA_SDOUT               |
|                           | HDA_45S       | HDA         | HDA_SDOUT_R             |
| PM_SUS_CLK                | CLK SLOW_45S  | CLK SLOW    | PM_CLK32K_SUSCLK_R      |
|                           | CLK SLOW_45S  | CLK SLOW    | SMC_CLK32K              |
| SPT_CLK                   | SPT_45S       | SPT         | SPI_CLK_R               |
|                           | SPT_45S       | SPT         | SPI_CLK                 |
| SPT_MOST                  | SPT_45S       | SPT         | SPI_MOSI_R              |
|                           | SPT_45S       | SPT         | SPI_MOSI                |
| SPT_MISO                  | SPT_45S       | SPT         | SPI_MISO                |
|                           | SPT_45S       | SPT         | SPI_MISO_R              |
| SPT_CS0                   | SPT_45S       | SPT         | SPI_CS0_R_L             |
|                           | SPT_45S       | SPT         | SPI_CS0_L               |
|                           | SPT_45S       | SPT         | SPI_SMC_CLK             |
|                           | SPT_45S       | SPT         | SPI_SMC_MOSI            |
|                           | SPT_45S       | SPT         | SPI_SMC_MISO            |
|                           | SPT_45S       | SPT         | SPI_SMC_CS_L            |
|                           | SPT_45S       | SPT         | SPI_MLB_CLK             |
|                           | SPT_45S       | SPT         | SPI_MLB_IO2_WP_L        |
|                           | SPT_45S       | SPT         | SPI_MLB_IO3_HOLD_L      |
|                           | SPT_45S       | SPT         | SPI_MLB_CS_L            |
|                           | SPT_45S       | SPT         | SPI_IO<2>               |
|                           | SPT_45S       | SPT         | SPI_IO2_R               |
|                           | SPT_45S       | SPT         | SPI_IO<3>               |
|                           | SPT_45S       | SPT         | SPI_IO3_R               |
| PCIe AP R2D               | PCIe_80D      | PCIe_PCH_TX | PCIe AP R2D_P           |
| PCIe AP R2D               | PCIe_80D      | PCIe_PCH_TX | PCIe AP R2D_N           |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe AP R2D_C_P         |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe AP R2D_C_N         |
| PCIe AP D2R               | PCIe_80D      | PCIe_PCH_RX | PCIe AP D2R_P           |
| PCIe AP D2R               | PCIe_80D      | PCIe_PCH_RX | PCIe AP D2R_N           |
| PCIe CLK100M_AP           | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_AP_P       |
| PCIe CLK100M_AP           | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_AP_N       |
| PCIe TBT R2D              | PCIe_80D      | PCIe_PCH_TX | PCIe TBT R2D_P<3...0>   |
| PCIe TBT R2D              | PCIe_80D      | PCIe_PCH_TX | PCIe TBT R2D_N<3...0>   |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe TBT R2D_C_P<3...0> |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe TBT R2D_C_N<3...0> |
| PCIe TBT D2R              | PCIe_80D      | PCIe_PCH_RX | PCIe TBT D2R_P<3...0>   |
| PCIe TBT D2R              | PCIe_80D      | PCIe_PCH_RX | PCIe TBT D2R_N<3...0>   |
|                           | PCIe_80D      | PCIe_PCH_RX | PCIe TBT D2R_C_P<3...0> |
|                           | PCIe_80D      | PCIe_PCH_RX | PCIe TBT D2R_C_N<3...0> |
| PCIe CLK100M_TBT          | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_TBT_P      |
| PCIe CLK100M_TBT          | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_TBT_N      |
|                           | CLK PCIe_80D  | CLK PCIe    | PEG_CLK100M_P           |
|                           | CLK PCIe_80D  | CLK PCIe    | PEG_CLK100M_N           |
| XDP_TDT                   | PCH_45S       | PCH_ITP     | XDP_PCH_TDI             |
| XDP_TDO                   | PCH_45S       | PCH_ITP     | XDP_PCH_TDO             |
| XDP_TMS                   | PCH_45S       | PCH_ITP     | XDP_PCH_TMS             |
| XDP_TCK                   | PCH_45S       | PCH_ITP     | XDP_PCH_TCK             |
| PCIe CAM                  | PCIe_80D      | PCIe_PCH_TX | PCIe CAMERA R2D_P       |
| PCIe CAM                  | PCIe_80D      | PCIe_PCH_TX | PCIe CAMERA R2D_N       |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe CAMERA R2D_C_P     |
|                           | PCIe_80D      | PCIe_PCH_TX | PCIe CAMERA R2D_C_N     |
| PCIe CAM                  | PCIe_80D      | PCIe_PCH_RX | PCIe CAMERA D2R_P       |
| PCIe CAM                  | PCIe_80D      | PCIe_PCH_RX | PCIe CAMERA D2R_N       |
|                           | PCIe_80D      | PCIe_PCH_RX | PCIe CAMERA D2R_C_P     |
|                           | PCIe_80D      | PCIe_PCH_RX | PCIe CAMERA D2R_C_N     |
| PCIe CLK100M_CAM          | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_CAMERA_P   |
| PCIe CLK100M_CAM          | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_CAMERA_N   |
|                           | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_CAMERA_C_P |
|                           | CLK PCIe_80D  | CLK PCIe    | PCIe CLK100M_CAMERA_C_N |

## Clock Net Properties

| ELECTRICAL_CONSTRAINT_SET                                                           |                    | NET_TYPE     |          |                      |
|-------------------------------------------------------------------------------------|--------------------|--------------|----------|----------------------|
|                                                                                     |                    | PHYSICAL     | SPACING  |                      |
|  | SYSCLK CLK32K_RTC  | CLK_SLOW_45S | CLK_SLOW | SYSCLK CLK32K_RTCX1  |
|  | SYSCLK CLK25M_SB   | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_CAMERA |
|  |                    | CLK_25M_45S  | CLK_25M  | CLK25M_CAM_CLKP      |
|  |                    | CLK_25M_45S  | CLK_25M  | CLK25M_CAM_XTALP_R   |
|  |                    | CLK_25M_45S  | CLK_25M  | CLK25M_CAM_XTALP     |
|  |                    | CLK_25M_45S  | CLK_25M  | CLK25M_CAM_XTALN     |
|  |                    | CLK_25M_45S  | CLK_25M  | CLK25M_CAM_CLKN      |
|  | SYSCLK CLK25M_TBT  | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_TBT    |
|  |                    | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_TBT_R  |
|  | SYSCLK CLK25M_XTAL | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_X1     |
|  |                    | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_X2     |
|  |                    | CLK_25M_45S  | CLK_25M  | SYSCLK CLK25M_X2_R   |
|  |                    | CLK_25M_45S  | CLK_25M  | SDCLK CLK25M_X2      |
|  |                    | CLK_25M_45S  | CLK_25M  | SDCLK CLK25M_X2_R    |
|  |                    | CLK_25M_45S  | CLK_25M  | SDCLK CLK25M_X1      |

Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW_ROUTE_ON_LAYER? | MINIMUM_LINE_WIDTH | MINIMUM_NECK_WIDTH | MAXIMUM_NECK_LENGTH | DIFFPAIR_PRIMARY_GAP | DIFFPAIR_NECK_GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| MEM_40S           | *     | =40_OHM_SE            | =40_OHM_SE         | =40_OHM_SE         | =40_OHM_SE          | =40_OHM_SE           | =40_OHM_SE        |
| MEM_50S           | *     | =50_OHM_SE            | =50_OHM_SE         | =50_OHM_SE         | =50_OHM_SE          | =50_OHM_SE           | =50_OHM_SE        |
| MEM_70D           | *     | =70_OHM_DIFF          | =70_OHM_DIFF       | =70_OHM_DIFF       | =70_OHM_DIFF        | =70_OHM_DIFF         | =70_OHM_DIFF      |
| MEM_73D           | *     | =73_OHM_DIFF          | =73_OHM_DIFF       | =73_OHM_DIFF       | =73_OHM_DIFF        | =73_OHM_DIFF         | =73_OHM_DIFF      |

Spacing Rule Sets

| SPACING_RULE_SET  | LAYER | LINE-TO-LINE_SPACING | WEIGHT |
|-------------------|-------|----------------------|--------|
| MEM_DATA2SELF     | *     | =2X_DIELECTRIC       | ?      |
| MEM_DATA2OTHERMEM | *     | =8X_DIELECTRIC       | ?      |
| MEM_DQS2OWNDATA   | *     | =3X_DIELECTRIC       | ?      |
| MEM_CMD2CMD       | *     | =3X_DIELECTRIC       | ?      |
| MEM_CMD2CTRL      | *     | =3X_DIELECTRIC       | ?      |
| MEM_CTRL2CTRL     | *     | =3X_DIELECTRIC       | ?      |
| MEM_CLK2CLK       | *     | =6X_DIELECTRIC       | ?      |
| MEM_20THERMEM     | *     | =4X_DIELECTRIC       | ?      |
| MEM_2PWR          | *     | =2X_DIELECTRIC       | 10000  |
| MEM_2GND          | *     | =2X_DIELECTRIC       | 10000  |
| MEM_2OTHER        | *     | =6X_DIELECTRIC       | ?      |

Memory to Power Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_PWR           | MEM_*             | *         | MEM_2PWR         |
| MEM_PWR           | *                 | *         | DEFAULT          |

| NET_PHYSICAL_TYPE | AREA_TYPE | PHYSICAL_RULE_SET |
|-------------------|-----------|-------------------|
| MEM_70D           | MEM_TERM  | MEM_73D           |
| MEM_40S           | MEM_TERM  | MEM_50S           |

Memory to GND Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| GND               | MEM_*             | *         | MEM_2GND         |

Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_A_DQS_0       | MEM_A_DATA_0      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_1       | MEM_A_DATA_1      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_2       | MEM_A_DATA_2      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_3       | MEM_A_DATA_3      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_4       | MEM_A_DATA_4      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_5       | MEM_A_DATA_5      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_6       | MEM_A_DATA_6      | *         | MEM_DQS2OWNDATA  |
| MEM_A_DQS_7       | MEM_A_DATA_7      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_0       | MEM_B_DATA_0      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_1       | MEM_B_DATA_1      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_2       | MEM_B_DATA_2      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_3       | MEM_B_DATA_3      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_4       | MEM_B_DATA_4      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_5       | MEM_B_DATA_5      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_6       | MEM_B_DATA_6      | *         | MEM_DQS2OWNDATA  |
| MEM_B_DQS_7       | MEM_B_DATA_7      | *         | MEM_DQS2OWNDATA  |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_*_DATA_*      | =SAME             | *         | MEM_DATA2SELF    |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET  |
|-------------------|-------------------|-----------|-------------------|
| MEM_*_DATA_*      | MEM_*             | *         | MEM_DATA2OTHERMEM |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CMD           | MEM_CMD           | *         | MEM_CMD2CMD      |
| MEM_CMD           | MEM_CTRL          | *         | MEM_CMD2CTRL     |
| MEM_CTRL          | MEM_CTRL          | *         | MEM_CTRL2CTRL    |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_CLK           | MEM_CLK           | *         | MEM_CLK2CLK      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_*             | MEM_*             | *         | MEM_20THERMEM    |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_A_DQS_0       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_1       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_2       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_3       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_4       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_5       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_6       | *                 | *         | MEM_20THER       |
| MEM_A_DQS_7       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_0       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_1       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_2       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_3       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_4       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_5       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_6       | *                 | *         | MEM_20THER       |
| MEM_B_DQS_7       | *                 | *         | MEM_20THER       |

|              |   |   |            |
|--------------|---|---|------------|
| MEM_A_DATA_0 | * | * | MEM_20THER |
| MEM_A_DATA_1 | * | * | MEM_20THER |
| MEM_A_DATA_2 | * | * | MEM_20THER |
| MEM_A_DATA_3 | * | * | MEM_20THER |
| MEM_A_DATA_4 | * | * | MEM_20THER |
| MEM_A_DATA_5 | * | * | MEM_20THER |
| MEM_A_DATA_6 | * | * | MEM_20THER |
| MEM_A_DATA_7 | * | * | MEM_20THER |
| MEM_B_DATA_0 | * | * | MEM_20THER |
| MEM_B_DATA_1 | * | * | MEM_20THER |
| MEM_B_DATA_2 | * | * | MEM_20THER |
| MEM_B_DATA_3 | * | * | MEM_20THER |
| MEM_B_DATA_4 | * | * | MEM_20THER |
| MEM_B_DATA_5 | * | * | MEM_20THER |
| MEM_B_DATA_6 | * | * | MEM_20THER |
| MEM_B_DATA_7 | * | * | MEM_20THER |
| MEM_CMD      | * | * | MEM_20THER |
| MEM_CTRL     | * | * | MEM_20THER |
| MEM_CLK      | * | * | MEM_20THER |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MEM_A_DATA_0      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_1      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_2      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_3      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_4      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_5      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_6      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_A_DATA_7      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_0      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_1      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_2      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_3      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_4      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_5      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_6      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |
| MEM_B_DATA_7      | MEM_*_DATA_*      | *         | MEM_20THERMEM    |

Memory Net Properties

| NET_TYPE                  |          |              |                       |
|---------------------------|----------|--------------|-----------------------|
| ELECTRICAL_CONSTRAINT_SET | PHYSICAL | SPACING      |                       |
| MEM_A_CLK0                | MEM_70D  | MEM_CLK      | MEM A CLK P<0>        |
| MEM_A_CLK0                | MEM_70D  | MEM_CLK      | MEM A CLK N<0>        |
| MEM_A_CLK1                | MEM_70D  | MEM_CLK      | MEM A CLK P<1>        |
| MEM_A_CLK1                | MEM_70D  | MEM_CLK      | MEM A CLK N<1>        |
| MEM_A_CTRL                | MEM_40S  | MEM_CTRL     | MEM A CS_L<1..0>      |
| MEM_A_CTRL                | MEM_40S  | MEM_CTRL     | MEM A ODT<0>          |
| MEM_A_CKE0                | MEM_40S  | MEM_CMD      | MEM A CKE<1..0>       |
| MEM_A_CKE1                | MEM_40S  | MEM_CMD      | MEM A CKE<3..2>       |
| MEM_A_CMD0                | MEM_40S  | MEM_CMD      | MEM A CAA<9..0>       |
| MEM_A_CMD1                | MEM_40S  | MEM_CMD      | MEM A CAB<9..0>       |
| MEM_A_DQ_BYTE0            | MEM_40S  | MEM_A_DATA_0 | MEM A DQ<7..0>        |
| MEM_A_DQ_BYTE1            | MEM_40S  | MEM_A_DATA_1 | MEM A DQ<15..8>       |
| MEM_A_DQ_BYTE2            | MEM_40S  | MEM_A_DATA_2 | MEM A DQ<23..16>      |
| MEM_A_DQ_BYTE3            | MEM_40S  | MEM_A_DATA_3 | MEM A DQ<31..24>      |
| MEM_A_DQ_BYTE4            | MEM_40S  | MEM_A_DATA_4 | MEM A DQ<39..32>      |
| MEM_A_DQ_BYTE5            | MEM_40S  | MEM_A_DATA_5 | MEM A DQ<47..40>      |
| MEM_A_DQ_BYTE6            | MEM_40S  | MEM_A_DATA_6 | MEM A DQ<55..48>      |
| MEM_A_DQ_BYTE7            | MEM_40S  | MEM_A_DATA_7 | MEM A DQ<63..56>      |
| MEM_A_DQS0                | MEM_70D  | MEM_A_DQS_0  | MEM A DQS P<0>        |
| MEM_A_DQS0                | MEM_70D  | MEM_A_DQS_0  | MEM A DQS N<0>        |
| MEM_A_DQS1                | MEM_70D  | MEM_A_DQS_1  | MEM A DQS P<1>        |
| MEM_A_DQS1                | MEM_70D  | MEM_A_DQS_1  | MEM A DQS N<1>        |
| MEM_A_DQS2                | MEM_70D  | MEM_A_DQS_2  | MEM A DQS P<2>        |
| MEM_A_DQS2                | MEM_70D  | MEM_A_DQS_2  | MEM A DQS N<2>        |
| MEM_A_DQS3                | MEM_70D  | MEM_A_DQS_3  | MEM A DQS P<3>        |
| MEM_A_DQS3                | MEM_70D  | MEM_A_DQS_3  | MEM A DQS N<3>        |
| MEM_A_DQS4                | MEM_70D  | MEM_A_DQS_4  | MEM A DQS P<4>        |
| MEM_A_DQS4                | MEM_70D  | MEM_A_DQS_4  | MEM A DQS N<4>        |
| MEM_A_DQS5                | MEM_70D  | MEM_A_DQS_5  | MEM A DQS P<5>        |
| MEM_A_DQS5                | MEM_70D  | MEM_A_DQS_5  | MEM A DQS N<5>        |
| MEM_A_DQS6                | MEM_70D  | MEM_A_DQS_6  | MEM A DQS P<6>        |
| MEM_A_DQS6                | MEM_70D  | MEM_A_DQS_6  | MEM A DQS N<6>        |
| MEM_A_DQS7                | MEM_70D  | MEM_A_DQS_7  | MEM A DQS P<7>        |
| MEM_A_DQS7                | MEM_70D  | MEM_A_DQS_7  | MEM A DQS N<7>        |
| MEM_B_CLK0                | MEM_70D  | MEM_CLK      | MEM B CLK P<0>        |
| MEM_B_CLK0                | MEM_70D  | MEM_CLK      | MEM B CLK N<0>        |
| MEM_B_CLK1                | MEM_70D  | MEM_CLK      | MEM B CLK P<1>        |
| MEM_B_CLK1                | MEM_70D  | MEM_CLK      | MEM B CLK N<1>        |
| MEM_B_CTRL                | MEM_40S  | MEM_CTRL     | MEM B CS_L<1..0>      |
| MEM_B_CTRL                | MEM_40S  | MEM_CTRL     | MEM B ODT<0>          |
| MEM_B_CKE0                | MEM_40S  | MEM_CMD      | MEM B CKE<1..0>       |
| MEM_B_CKE1                | MEM_40S  | MEM_CMD      | MEM B CKE<3..2>       |
| MEM_B_CMD0                | MEM_40S  | MEM_CMD      | MEM B CAA<9..0>       |
| MEM_B_CMD1                | MEM_40S  | MEM_CMD      | MEM B CAB<9..0>       |
| MEM_B_DQ_BYTE0            | MEM_40S  | MEM_B_DATA_0 | MEM B DQ<7..0>        |
| MEM_B_DQ_BYTE1            | MEM_40S  | MEM_B_DATA_1 | MEM B DQ<15..8>       |
| MEM_B_DQ_BYTE2            | MEM_40S  | MEM_B_DATA_2 | MEM B DQ<23..16>      |
| MEM_B_DQ_BYTE3            | MEM_40S  | MEM_B_DATA_3 | MEM B DQ<31..24>      |
| MEM_B_DQ_BYTE4            | MEM_40S  | MEM_B_DATA_4 | MEM B DQ<39..32>      |
| MEM_B_DQ_BYTE5            | MEM_40S  | MEM_B_DATA_5 | MEM B DQ<47..40>      |
| MEM_B_DQ_BYTE6            | MEM_40S  | MEM_B_DATA_6 | MEM B DQ<55..48>      |
| MEM_B_DQ_BYTE7            | MEM_40S  | MEM_B_DATA_7 | MEM B DQ<63..56>      |
| MEM_B_DQS0                | MEM_70D  | MEM_B_DQS_0  | MEM B DQS P<0>        |
| MEM_B_DQS0                | MEM_70D  | MEM_B_DQS_0  | MEM B DQS N<0>        |
| MEM_B_DQS1                | MEM_70D  | MEM_B_DQS_1  | MEM B DQS P<1>        |
| MEM_B_DQS1                | MEM_70D  | MEM_B_DQS_1  | MEM B DQS N<1>        |
| MEM_B_DQS2                | MEM_70D  | MEM_B_DQS_2  | MEM B DQS P<2>        |
| MEM_B_DQS2                | MEM_70D  | MEM_B_DQS_2  | MEM B DQS N<2>        |
| MEM_B_DQS3                | MEM_70D  | MEM_B_DQS_3  | MEM B DQS P<3>        |
| MEM_B_DQS3                | MEM_70D  | MEM_B_DQS_3  | MEM B DQS N<3>        |
| MEM_B_DQS4                | MEM_70D  | MEM_B_DQS_4  | MEM B DQS P<4>        |
| MEM_B_DQS4                | MEM_70D  | MEM_B_DQS_4  | MEM B DQS N<4>        |
| MEM_B_DQS5                | MEM_70D  | MEM_B_DQS_5  | MEM B DQS P<5>        |
| MEM_B_DQS5                | MEM_70D  | MEM_B_DQS_5  | MEM B DQS N<5>        |
| MEM_B_DQS6                | MEM_70D  | MEM_B_DQS_6  | MEM B DQS P<6>        |
| MEM_B_DQS6                | MEM_70D  | MEM_B_DQS_6  | MEM B DQS N<6>        |
| MEM_B_DQS7                | MEM_70D  | MEM_B_DQS_7  | MEM B DQS P<7>        |
| MEM_B_DQS7                | MEM_70D  | MEM_B_DQS_7  | MEM B DQS N<7>        |
|                           |          | MEM_PWR      | PP1V2 S3              |
|                           |          | MEM_PWR      | PP0V6 S3 MEM_VREFCA_A |
|                           |          | MEM_PWR      | PP0V6 S3 MEM_VREFDQ_A |
|                           |          | MEM_PWR      | PP0V6 S3 MEM_VREFCA_B |
|                           |          | MEM_PWR      | PP0V6 S3 MEM_VREFDQ_B |

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PAGE TITLE

Memory Constraints

 Apple Inc.

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PAGE

114 OF 120

SHEET

68 OF 73



## MIPI Interface Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| KIP1_850          | *     | =S_OHM_DIFF           | =S_OHM_DIFF        | =S_OHM_DIFF        | =S_OHM_DIFF         | =S_OHM_DIFF          | =S_OHM_DIFF       |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER      | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|------------|----------------------|--------|
| MIPI_20THER      | *     | =4X_DIELECTRIC       | ?      | MIPI_20THER      | TOP_BOTTOM | =6X_DIELECTRIC       | ?      |
| MIPI_2CLK        | *     | =6X_DIELECTRIC       | ?      | MIPI_2CLK        | TOP_BOTTOM | =8X_DIELECTRIC       | ?      |
| MIPICLK_20THER   | *     | =7X_DIELECTRIC       | ?      | MIPICLK_20THER   | TOP_BOTTOM | =18X_DIELECTRIC      | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| MIPI_DATA         | *                 | *         | MIPI_20THER      |
| MIPI_DATA         | CLK_MIPI          | *         | MIPI_2CLK        |
| CLK_MIPI          | *                 | *         | MIPICKL_20THER   |

## Memory Bus Constraints

| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| S2_MEM_45S        | *     | =45_OHM_SE            | =45_OHM_SE         | =45_OHM_SE         | =45_OHM_SE          | =STANDARD            | =STANDARD         |
| S2_MEM_85D        | *     | =85_OHM_DIFF          | =85_OHM_DIFF       | =85_OHM_DIFF       | =85_OHM_DIFF        | =85_OHM_DIFF         | =85_OHM_DIFF      |

## Spacing Rule Sets

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT | SPACING_RULE_SET | LAYER       | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|------------------|-------------|----------------------|--------|
| S2_DATA2SELF     | *     | =2x_DIELECTRIC       | ?      | S2_DATA2SELF     | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2_DQS20WDATA    | *     | =2x_DIELECTRIC       | ?      | S2_DQS20WDATA    | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2_CMD2CMD       | *     | =2x_DIELECTRIC       | ?      | S2_CMD2CMD       | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2_CMD2CTRL      | *     | =2x_DIELECTRIC       | ?      | S2_CMD2CTRL      | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2_CTRL2CTRL     | *     | =2x_DIELECTRIC       | ?      | S2_CTRL2CTRL     | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2_20THERMEM     | *     | =4x_DIELECTRIC       | ?      | S2_20THERMEM     | TOP, BOTTOM | =6x_DIELECTRIC       | ?      |
| S2MEM_2PWR       | *     | =2x_DIELECTRIC       | ?      | S2MEM_2PWR       | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2MEM_2GND       | *     | =2x_DIELECTRIC       | ?      | S2MEM_2GND       | TOP, BOTTOM | =4x_DIELECTRIC       | ?      |
| S2MEM_20THER     | *     | =6x_DIELECTRIC       | ?      | S2MEM_20THER     | TOP, BOTTOM | =10x_DIELECTRIC      | ?      |

## Memory Bus Spacing Group Assignments

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| S2_MEM_DATA*      | *                 | *         | S2MEM_20THER     |
| S2_MEM_DQS*       | *                 | *         | S2MEM_20THER     |
| S2_MEM_CMD        | *                 | *         | S2MEM_20THER     |
| S2_MEM_CTRL       | *                 | *         | S2MEM_20THER     |
| S2_MEM_CLK        | *                 | *         | S2MEM_20THER     |
| S2_MEM_DATA*      | =SAME             | *         | S2_DATA2SELF     |
| S2_MEM_CMD        | S2_MEM_CMD        | *         | S2_CMD2CMD       |
| S2_MEM_CMD        | S2_MEM_CTRL       | *         | S2_CMD2CTRL      |
| S2_MEM_CTRL       | S2_MEM_CTRL       | *         | S2_CTRL2CTRL     |
| S2_MEM_*          | S2_MEM_*          | *         | S2_20THERMEM     |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| S2_MEM_DQS1       | S2_MEM_DATA1      | *         | S2_DQS20WINDATA  |
| S2_MEM_DQS0       | S2_MEM_DATA0      | *         | S2_DQS20WINDATA  |

## Memory to Power Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| S2_MEM_PWR        | S2_MEM_*          | *         | S2MEM_2PWR       |
| S2_MEM_PWR        | *                 | *         | DEFAULT          |

## Memory to GND Spacing

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| GND               | S2_MEM_*          | *         | S2MEM_2GND       |

## Camera Net Properties

| ELECTRICAL_CONSTRAINT_SET                                                           |               | NET_TYPE   |              |                        |       |
|-------------------------------------------------------------------------------------|---------------|------------|--------------|------------------------|-------|
|                                                                                     |               | PHYSICAL   | SPACING      |                        |       |
|  | S2_MEM_CLK    | S2_MEM_BSD | S2_MEM_CLK   | MEM_CAM_CLK_P          | 31 32 |
|  | S2_MEM_CLK    | S2_MEM_BSD | S2_MEM_CLK   | MEM_CAM_CLK_N          | 31 32 |
|  | S2_MEM_CMT1   | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_CKE            | 31 32 |
|  | S2_MEM_CMT1   | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_CS_L           | 31 32 |
|  | S2_MEM_CMT1   | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_ODT            | 32    |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_CAS_L          | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_RAS_L          | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CTR1  | MEM_CAM_WE_L           | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CMD   | MEM_CAM_BA<0>          | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CMD   | MEM_CAM_BA<1>          | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CMD   | MEM_CAM_BA<2>          | 31 32 |
|  | S2_MEM_CMD    | S2_MEM_45S | S2_MEM_CMD   | MEM_CAM_BA<3>          | 31 32 |
|  | S2_MEM_DQS0   | S2_MEM_85D | S2_MEM_DQS0  | MEM_CAM_DQS_P<0>       | 31 32 |
|  | S2_MEM_DQS0   | S2_MEM_85D | S2_MEM_DQS0  | MEM_CAM_DQS_N<0>       | 31 32 |
|  | S2_MEM_DQS1   | S2_MEM_85D | S2_MEM_DQS1  | MEM_CAM_DQS_P<1>       | 31 32 |
|  | S2_MEM_DQS1   | S2_MEM_85D | S2_MEM_DQS1  | MEM_CAM_DQS_N<1>       | 31 32 |
|  | S2_MEM_DATA_0 | S2_MEM_45S | S2_MEM_DATA0 | MEM_CAM_DM<0>          | 31 32 |
|  | S2_MEM_DATA_1 | S2_MEM_45S | S2_MEM_DATA1 | MEM_CAM_DM<1>          | 31 32 |
|  | S2_MEM_A      | S2_MEM_45S | S2_MEM_CMD   | MEM_CAM_A<14...0>      | 31 32 |
|  | S2_MEM_DATA_0 | S2_MEM_45S | S2_MEM_DATA0 | MEM_CAM_DQ<7...0>      | 31 32 |
|  | S2_MEM_DATA_1 | S2_MEM_45S | S2_MEM_DATA1 | MEM_CAM_DQ<15...8>     | 31 32 |
|  | MIPI_DATA_S2  | MIPI_BSD   | MIPI_DATA    | MIPI_DATA_P            | 31 32 |
|  | MIPI_DATA_S2  | MIPI_BSD   | MIPI_DATA    | MIPI_DATA_N            | 31 32 |
|  | MIPI_DATA_S2  | MIPI_BSD   | MIPI_DATA    | MIPI_DATA_CONN_P       | 32 62 |
|  | MIPI_DATA_S2  | MIPI_BSD   | MIPI_DATA    | MIPI_DATA_CONN_N       | 32 62 |
|  | MIPI_CLK_S2   | MIPI_BSD   | CLK_MIPI     | MIPI_CLK_P             | 31 32 |
|  | MIPI_CLK_S2   | MIPI_BSD   | CLK_MIPI     | MIPI_CLK_N             | 31 32 |
|  | MIPI_DATA_S2  | MIPI_BSD   | CLK_MIPI     | MIPI_CLK_CONN_P        | 32 62 |
|  | MIPI_DATA_S2  | MIPI_BSD   | CLK_MIPI     | MIPI_CLK_CONN_N        | 32 62 |
|  |               |            | S2_MEM_PWR   | PP1V35_CAM             | 31 32 |
|  |               |            | S2_MEM_PWR   | PP0V675_CAM_VREF       | 31 32 |
|  |               |            | S2_MEM_PWR   | PP0V675_MEM_CAM_VREFCA | 31 32 |
|  |               |            | S2_MEM_PWR   | PP0V675_MEM_CAM_VREFDQ | 32    |





| PHYSICAL_RULE_SET | LAYER | ALLOW ROUTE ON LAYER? | MINIMUM LINE WIDTH | MINIMUM NECK WIDTH | MAXIMUM NECK LENGTH | DIFFPAIR PRIMARY GAP | DIFFPAIR NECK GAP |
|-------------------|-------|-----------------------|--------------------|--------------------|---------------------|----------------------|-------------------|
| SENSE_1T01_45S    | *     | =1T01_DIFFPAIR        | =45_0HM_SE         | =45_0HM_SE         | =45_0HM_SE          | =1T01_DIFFPAIR       | =1T01_DIFFPAIR    |
| SENSE_1T01_P2MM   | *     | =1T01_DIFFPAIR        | 0.200 MM           | 0.100 MM           | =1T01_DIFFPAIR      | =1T01_DIFFPAIR       | =1T01_DIFFPAIR    |
| THERM_1T01_45S    | *     | =1T01_DIFFPAIR        | =45_0HM_SE         | =45_0HM_SE         | =1T01_DIFFPAIR      | =1T01_DIFFPAIR       | =1T01_DIFFPAIR    |
| SPKR_DIFFPAIR     | *     | =1T01_DIFFPAIR        | 0.300 MM           | 0.100 MM           | =1T01_DIFFPAIR      | =1T01_DIFFPAIR       | =1T01_DIFFPAIR    |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| SENSE            | *     | =2:1_SPACING         | ?      |
| THERM            | *     | =2:1_SPACING         | ?      |
| AUDIO            | *     | =2:1_SPACING         | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| CPU_COMP          | GND               | *         | GND_P2MM         |
| CPU_VCCSENSE      | GND               | *         | GND_P2MM         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND              | *     | =STANDARD            | ?      |

| NET_SPACING_TYPE1 | NET_SPACING_TYPE2 | AREA_TYPE | SPACING_RULE_SET |
|-------------------|-------------------|-----------|------------------|
| GND               | CLK_PCIE          | *         | GND_P2MM         |
| GND               | PCIE*             | *         | GND_P2MM         |
| GND               | SATA*             | *         | GND_P2MM         |
| GND               | USB*              | *         | GND_P2MM         |
| GND               | LVDS*             | *         | GND_P2MM         |
| SB_POWER          | CLK_PCIE          | *         | PWR_P2MM         |
| SB_POWER          | SATA*             | *         | PWR_P2MM         |
| SB_POWER          | SATA*             | *         | PWR_P2MM         |

| SPACING_RULE_SET | LAYER | LINE-TO-LINE SPACING | WEIGHT |
|------------------|-------|----------------------|--------|
| GND_P2MM         | *     | 0.20 MM              | 10000  |
| PWR_P2MM         | *     | 0.20 MM              | 10000  |

## J11/J13 Specific Net Properties

| ELECTRICAL_CONSTRAINT_SET                                                             |               | NET_TYPE        |                                                                        |                           |
|---------------------------------------------------------------------------------------|---------------|-----------------|------------------------------------------------------------------------|---------------------------|
|                                                                                       |               | PHYSICAL        | SPACING                                                                |                           |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | INLET_THMSNS_D1_P 42      |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | INLET_THMSNS_D1_N 42      |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBTTHMSNS_D2_R_P 42       |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBTTHMSNS_D2_R_N 42       |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBTTHMSNS_D2_P            |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBTTHMSNS_D2_N            |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBT_MLBBOT_THMSNS_P 42    |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | TBT_MLBBOT_THMSNS_N 42    |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | MLBBOT_THMSNS_D3_P        |
|    | SENSE_DIEPAIR | THERM_1T01_45S  | THERM                                                                  | MLBBOT_THMSNS_D3_N        |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | TBDTHMSNS_D2_P 42         |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | TBDTHMSNS_D2_N 42         |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | CPUATHMSNS_D2_P 42        |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | CPUATHMSNS_D2_N 42        |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | CPUVCCIO50_CS_N           |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | CPUVCCIO50_CS_P           |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | CPUVR_ISNS1_P 40 50       |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | CPUVR_ISNS1_N 40 50       |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | CPUVR_ISNS2_P 40 50       |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | CPUVR_ISNS2_N 40 50       |
|                                                                                       |               |                 |                                                                        |                           |
|    |               | SENSE_1T01_P2MM | SENSE                                                                  | CPUVR_ISNS1_P_R 40 41     |
|    |               | SENSE_1T01_P2MM | SENSE                                                                  | CPUVR_ISNS1_N_R 40 41     |
|    |               | SENSE_1T01_45S  | SENSE                                                                  | CPUVR_ISUM_R_P 40         |
|    |               | SENSE_1T01_45S  | SENSE                                                                  | CPUVR_ISUM_R_N 40         |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | ISNS_CPUDDR_P 40          |
|    | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | ISNS_CPUDDR_N 40          |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_P3V3S5_N 40          |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_P3V3S5_P 40          |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_3V3_S0_P             |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_3V3_S0_N             |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_CAMERA_P 39          |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_CAMERA_N 39          |
|                                                                                       |               |                 |                                                                        |                           |
|    | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_P3V3_S0_N 39         |
|   | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_P3V3_S0_P 39         |
|   | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | ISNS_1V05_S0_P 40 53      |
|  | SENSE_DIEPAIR | SENSE_1T01_P2MM | SENSE                                                                  | ISNS_1V05_S0_N 40 53      |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_BMON_GAIN_P          |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_BMON_GAIN_N          |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_COMPUTING_N 39 41 |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_COMPUTING_P 39 41 |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_OTHER_N 39        |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_OTHER_P 39        |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_1V2_S3_N 39 51       |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_1V2_S3_P 39 51       |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_AIRPORT_N 39         |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_AIRPORT_P 39         |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_SSD_N 39             |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_SSD_P 39             |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_LCDBKLT_N 39         |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_LCDBKLT_P 39         |
|                                                                                       |               |                 |                                                                        |                           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_PANEL_N 41           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_PANEL_P 41           |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_GAIN_N 41 42      |
|  | SENSE_DIEPAIR | SENSE_1T01_45S  | SENSE                                                                  | ISNS_HS_GAIN_P 41 42      |
|                                                                                       |               |                 |                                                                        |                           |
|  | AUD_DIFF      | 1T01_DIEPAIR    | AUDIO                                                                  | SPKRAMP_INR_P 45 59 63    |
|  | AUD_DIFF      | 1T01_DIEPAIR    | AUDIO                                                                  | SPKRAMP_INR_N 45 59 63    |
|  |               | 1T01_DIEPAIR    | AUDIO                                                                  | MAX98300_R_P 45           |
|  |               | 1T01_DIEPAIR    | AUDIO                                                                  | MAX98300_R_N 45           |
|  | SPKR_OUT      | SPKR_DIEPAIR    | AUDIO                                                                  | SPKRAMP_ROUT_P 45 62      |
|  | SPKR_OUT      | SPKR_DIEPAIR    | AUDIO                                                                  | SPKRAMP_ROUT_N 45 62      |
|                                                                                       |               |                 |                                                                        |                           |
|  |               | SB_POWER        | PP3V3_S5 9 11 13 15 16 17 18 28 29 40 52<br>60 62 63 65 56 57 58 60 62 |                           |
|  |               | SB_POWER        | PP3V3_S0 37 38 39 30 31 32 33 34 35 36 38 39                           |                           |
|                                                                                       |               |                 |                                                                        |                           |
|  |               | GND             | GND                                                                    |                           |

|                                                                                                                                                                                                                                                                                                                         |  |                                          |  |
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| Project Specific Constraints                                                                                                                                                                                                                                                                                            |  |                                          |  |
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|                                                                                                                                                                                                                                                                                                                         |  | PAGE<br><b>118 OF 120</b>                |  |
|                                                                                                                                                                                                                                                                                                                         |  | SHEET<br><b>72 OF 73</b>                 |  |



|   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |   |   |   |   |   |   |   |   |
|---|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|---|---|---|---|---|---|---|
|   | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 |   |
| D | <div>Change List:<br/>&lt;rdar://component/508389&gt; J41 HW EE Schematic   Proto 0<br/>&lt;rdar://component/512995&gt; J41 HW EE Schematic   Pre Proto 1<br/>&lt;rdar://component/508412&gt; J41 HW EE Schematic   Proto 1<br/>&lt;rdar://component/508413&gt; J41 HW EE Schematic   EVT<br/>&lt;rdar://component/508414&gt; J41 HW EE Schematic   DVT</div> <div>Kismet:<br/>afp://kismet.apple.com/Kismet-Projects/J41-J43</div> <div>Useful Wiki Links:<br/>Schematic Conventions - https://hmts.ecs.apple.com/wiki/index.php/User:Wferry/SchConventions<br/>Schematic Design Wiki - https://hmts.ecs.apple.com/wiki/index.php/Schematic_Design</div> <div>MobileMac HW Radar:<br/>&lt;rdar://component/497591&gt; MobileMac HW   Task<br/>&lt;rdar://component/497587&gt; MobileMac HW   Schematic<br/>&lt;rdar://component/497585&gt; MobileMac HW   New Bugs<br/>&lt;rdar://component/497588&gt; MobileMac HW   Layout<br/>&lt;rdar://component/497590&gt; MobileMac HW   Investigation<br/>&lt;rdar://component/497589&gt; MobileMac HW   Architecture</div> <div>Other Info:<br/>Page Allocations - &lt;rdar://problem/11791318&gt; 2012 Schematic Page Allocations</div> |   |   |   |   |   |   |   | D |
| C |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |   |   |   |   |   |   |   | C |
| B |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |   |   |   |   |   |   |   | B |
| A |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |   |   |   |   |   |   |   | A |
|   | 8                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 7 | 6 | 5 | 4 | 3 | 2 | 1 |   |

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|                                                                                                                                                                                                                                                                                                                      |  | PAGE<br>120 OF 120          |           |
|                                                                                                                                                                                                                                                                                                                      |  | SHEET<br>73 OF 73           |           |

|                                                                                                                                                                                                                                                                                                                   |  |                  |      |
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| SYNC MASTER=MASTER                                                                                                                                                                                                                                                                                                |  | SYNC DATE=MASTER |      |
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|                                                                                                                                                                                                                                                                                                                   |  | PAGE             |      |
|                                                                                                                                                                                                                                                                                                                   |  | 120 OF 120       |      |
|                                                                                                                                                                                                                                                                                                                   |  | SHEET            |      |
|                                                                                                                                                                                                                                                                                                                   |  | 73 OF 73         |      |