1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

SCHEM,MLB_BAFFIN,X363G

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
10	0006897289	ENGINEERING RELEASED	2016-08-24

PAGE	CSA	CONTENTS	SYNC	DATE
1	1	MLB_BAFFIN		
2	2	BOM Configuration	J80_MLB	07/07/2015
3	3	BOM Configuration	J80_MLB_BAFFIN_CLEAN	12/02/2015
4	4	PD Parts	J80_MLB	11/16/2015
5	5	CPU DMI/PEG/FDI/RSVD	X363_AGOTETI	01/21/2016
6	6	CPU Clock/Misc/JTAG/CFG	J80_MLB	11/06/2015
7	7	CPU DDR3 Interfaces	J80_MLB	11/06/2015
8	8	CPU Power	J80_MLB	08/16/2015
9	9	CPU Ground	J80_MLB	08/17/2015
10	10	CPU Decoupling 1 [10]	J80_DTUZMAN_MLB_BAFFIN	11/22/2015
11	11	CPU Decoupling 2 [11]	X363_SEAN	02/01/2016
12	12	PCH RTC/HDA/JTAG/SATA/CLK	X363_SAKKOC	04/14/2016
13	13	PCH DMI/FDI/PM/GFX/PCI	J80_MLB	11/06/2015
14	14	PCH PCI-E/USB	X363_SAKKOC	04/14/2016
15	15	PCH GPIO/MISC/NCTF	X363_SAKKOC	04/29/2016
16	16	PCH Power	X363_SAKKOC	01/25/2016
17	17	PCH DECOUPLING	J80_MLB	11/06/2015
18	18	CPU/PCH Merged XDP	X363_SAKKOC	01/25/2016
19	19	Chipset Support 1	X363_SAKKOC	04/29/2016
20	20	Chipset Support 2	X363_SAKKOC	01/14/2016
21	22	LPDDR3 VREF MARGINING	J80_MLB	11/06/2015
22	23	LPDDR3 DRAM Channel A (0-31)	J80_MLB	11/06/2015
23	24	LPDDR3 DRAM Channel A (32-63)	J80_MLB	11/06/2015
24	25	LPDDR3 DRAM Channel B (0-31)	J80_MLB	11/06/2015
25	26	LPDDR3 DRAM Channel B (32-63)	J80_MLB	11/06/2015
26	27	LPDDR3 DRAM Termination	J80_MLB	11/06/2015
27	28	USB-C HIGH SPEED 1	J80_MLB	11/06/2015
28	29	USB-C HIGH SPEED 2	J80_MLB	11/06/2015
29	30	USB-C Support	X363_AGOTETI	08/08/2016
30	31	USB-C PORT CONTROLLER A	X362_GKOO	08/08/2016
31	32	USB-C PORT CONTROLLER B	J80_MLB	11/06/2015
32	33	USB-C CONNECTOR A	X362_MLB	03/30/2016
33	34	USB-C CONNECTOR B	X362_MLB	03/29/2016
34	35	TBT 5V REGULATOR	J80_ZIFENGSHEN_MLB_BAFFIN	12/04/2015
35	37	WIFI/BT: MODULE 1	X363_SAKKOC	04/29/2016
36	38	WIFI/BT: MODULE 2	J80_MLB	11/06/2015
37	39	Camera/DFR 1	X363_SAKKOC	04/29/2016
38	40	Camera/DFR 2	X362_T208	03/22/2016
39	41	Camera/DFR 3	X362_T208	04/25/2016
40	42	Berkelium - 1	X362_T208	01/27/2016
41	43	Berkelium - 2	X362_T208	03/15/2016
42	44	T208 Support	X362_T208	06/30/2016
43	45	Connectors&ESD	X363_SAMANTHA	01/08/2016
44	47	External A USB3 Connector	J80_MLB	08/26/2015
45	49	MESA	X362_P49	01/08/2016
46	50	SMC	X363_ZIFENGSHEN	04/14/2016
47	51	SMC Shared Support	J80_ZIFENGSHEN_MLB_BAFFIN	11/19/2015
48	52	SMC Project Support	X363_ZIFENGSHEN	04/14/2016
49	53	SMBus Connections	X363_ZIFENGSHEN	04/14/2016
50	54	Power Sensors: High Side	X363_ZIFENGSHEN	04/14/2016
51	55	Power Sensors: Load Side	X363_ZIFENGSHEN	04/14/2016
52	56	Power Sensors: Extended	X363_ZIFENGSHEN	04/14/2016
53	57	Power Sensors: Extended 2	X363_ZIFENGSHEN	04/14/2016
54	58	Thermal Sensors	X363_ZIFENGSHEN	04/14/2016
55	59	Sensor Extended 3	X363_ZIFENGSHEN	05/19/2016
56	60	Fans	X363_ZIFENGSHEN	04/14/2016
57	61	SPI Debug Connector	J80_MLB	11/06/2015
58	62	HDA Bridge	X363_AUDIO	01/11/2016
59	63	AUDIO JACK CODEC	X363_AUDIO	01/25/2016
60	64	AUDIO Speaker Amps & Conn	X363_AUDIO	01/25/2016
61	65	AUDIO Speaker Amps & Conn	X363_AUDIO	01/25/2016
62	66	AUDIO JACK CONNECTOR	J80_MLB	11/06/2015
63	69	DC-In & Battery Connectors	J80_MLB	11/06/2015
64	70	PBUS Supply & Battery Charger	J80_MLB	11/06/2015
65	71	CORE & SA IMVP IC	J80_DTUZMAN_MLB_BAFFIN	12/10/2015
66	72	CORE IMVP POWER BLOCK	J80_DTUZMAN_MLB_BAFFIN	09/03/2015
67	73	SA IMVP IC	J80_DTUZMAN_MLB_BAFFIN	11/18/2015
68	74	GT & GTX IMVP POWER BLOCK	J80_DTUZMAN_MLB_BAFFIN	09/03/2015
69	76	Power - 5V 3.3V Supply	J80_DTUZMAN_MLB_BAFFIN	12/09/2015
70	78	PMIC-1 & Power Control	J80_MLB	12/08/2015
71	79	PMIC-1 1.2V 0.6V VCCIO	J80_MLB	11/06/2015
72	80	PMIC-1 1V 1.8V VCCPCH	X363_ZIFENGSHEN	04/14/2016
73	81	PMIC-1 Aliases & TPs	J80_SILUCHEN_MLB_BAFFIN	12/08/2015
74	82	Power FETs	J80_SAKKOC_MLB_BAFFIN	12/11/2015
75	84	LCD Backlight Driver	J80_DTUZMAN_MLB_BAFFIN	12/03/2015
76	85	eDP Display Connector	J80_ZIFENGSHEN_MLB_BAFFIN	12/03/2015
77	86	POLARIS_CONTROLLER	X363_JSAMUELS	04/01/2016
78	87	POLARIS POWER	X363_JSAMUELS	05/18/2016
79	88	POLARIS GND	X363_JSAMUELS	04/01/2016
80	89	Connector	X363_JSAMUELS	04/01/2016
81	90	TEMP SENSORS	J80_MLB	11/06/2015
82	91	NAND 1/2	X363_JSAMUELS	08/09/2016
83	92	NAND 2/2	X363_JSAMUELS	08/09/2016
84	93	POLARIS PMIC	X363_JSAMUELS	08/09/2016
85	94	SSD NAND VR	X363_JSAMUELS	04/01/2016
86	95	SSD SUPPORT	X363_ZIFENGSHEN	04/15/2016
87	96	Lifeboat	X363_BBABADI	01/20/2016
88	97	Constraints	Constraints	05/18/2016
89	98	eDP Mux	dpmux	08/22/2015
90	99	GPU PCC	X363_SEAN	01/27/2016
91	100	BAFFIN PCI-E	X363_SEAN	01/27/2016
92	101	Baffin CORE/FB POWER	X363_SEAN	02/01/2016
93	102	Baffin FRAME BUFFER I/F	J80_SEAN	04/29/2015
94	103	Baffin 1V05 GPU / 1V35 FB Power Supply	J80_DTUZMAN_MLB_BAFFIN	12/08/2015
95	104	GDDR5 Frame Buffer A	J80_SEAN	04/29/2015
96	105	GDDR5 Frame Buffer B	J80_SEAN	04/29/2015
97	106	GFX IMVP VCore Regulator [106]	J80_DTUZMAN_MLB_BAFFIN	12/08/2015
98	107	Baffin GPIOs,CLK & Straps	X363_SEAN	01/28/2016
99	108	Baffin DP/GPIO	X363_SEAN	01/27/2016
100	109	Baffin VSS & MISC	X363_SEAN	01/27/2016
101	110	USB-C HIGH SPEED 1	J80_MLB	11/06/2015
102	111	USB-C HIGH SPEED 2	J80_MLB	11/06/2015
103	112	USB-C Support	J80_AGOTETI_MLB_BAFFIN	12/07/2015
104	113	USB-C PORT CONTROLLER A	J80_MLB	11/06/2015
105	114	USB-C PORT CONTROLLER B	J80_MLB	11/06/2015
106	115	USB-C CONNECTOR A	X362_MLB	03/30/2016
107	116	USB-C CONNECTOR B	X362_MLB	03/29/2016
108	117	TBT 5V REGULATOR	J80_ZIFENGSHEN_MLB_BAFFIN	12/04/2015
109	120	Power Aliases - 1	J80_MLB	08/16/2015
110	121	Power Aliases - 2	X363_SAKKOC	01/14/2016
111	122	Signal Aliases	X363_SAKKOC	01/13/2016
112	123	Memory Bit/Byte Swizzle	J80_MLB	11/06/2015
113	124	ICT & FCT 1	X363_SAKKOC	04/14/2016
114	125	ICT & FCT 2	J80_BBABADI_MLB_BAFFIN	12/10/2015
115	126	NC & No Test	X363_BBABADI	01/26/2016
116	127	Desense Caps	X363_ZIFENGSHEN	04/15/2016
117	128	Desense Caps	DESENSE	05/18/2016
118	130	Project Specific Constraints	X363_ZIFENGSHEN	06/02/2016
119	141	639 BOM Configuration	J80_MLB	07/23/2015
120	142	639 BOM Configuration 2	J80_MLB	07/23/2015

DRAWING
TITLE=MLB_BAFFIN
ABBREV=ABBREV
LAST_MODIFIED=Wed Aug 24 09:57:44 2016

LAST_MODIFICATION=Wed Aug 24 09:57:44 2016

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-00647	1	SCHEM,MLB-BAFFIN,X363G	SCH	CRITICAL	
820-00281	1	PCBF,MLB-BAFFIN,X363G	PCB	CRITICAL	

This is the PVT design

DRAWING TITLE: SCHEM,MLB-BAFFIN,X363

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 1 OF 145
SHEET: 1 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00076	COMMON PARTS,MLB-BAFFIN,X363	X363_COMMON
985-00126	DEV,MLB-BAFFIN,X363	X363_DEVEL:PVT
985-00232	DEV,MLB-BAFFIN,PVT,X363	X363_DEVEL:PVT

639 BOMs have been moved to the end of the schematic

X363 BOM Groups

BOM GROUP	BOM OPTIONS
X363_COMMON	ALTERNATE,COMMON,X363_COMMON1,X363_COMMON2,X363_COMMON3,X363_COMMON4,X363_PROGPARTS
X363_COMMON1	SOC:HYNIX,SE:PROD,SKIP_5V3V3:AUDIBLE,DIPLEXER:MURATA,T208_PROG:REV5,BOARD_ID:17,VCCHDA:S0
X363_COMMON2	XDP:YES,SAMCONN,SOC_BOOT:SPI,DPMUX_XTAL:NO,GPUCLK:OSC,BAFFIN,AP_TEMP,VCCPLLOC:S3,WIFI_SAK:NO
X363_COMMON3	CPUTHRM:ALRT,TBTTHRM:ALRT,LOADRC:NO,OTHERRC:YES,DDRRC:YES,TBTRC:YES,TPADRC:YES,LID_FEATURE_ON
X363_COMMON4	EDP:YES,CPUPEG:X8X4X4,TBTTHRM_SNS,GPUTHRM_SNS,S3_STATE:YES,GPU_ROM:YES,SVID_PU:CORE
X363_PROGPARTS	BOOTROM_PROG:DVT,BT_PROG:DVT,WIFI_PROG:DVT,UPCROM_PROG:DVT,SMC_PROG:PVT,DPMUXMCU:PROG,PCC:NO
X363_DEVEL:ENG	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG,GPUROM:BLANK,PCC:YES
X363_DEVEL:DVT	ALTERNATE,ENGISNS,DBGLED,XDP_CONN,USBC_DBG,DBG_BTN,DBG_FAN,DBG_XTAL,DPMUX_DEBUG,WIFI_DBG,SSD_DEBUG
X363_DEVEL:PVT	ALTERNATE,XDP_CONN,USBC_DBG
ENGISNS	TBTISNS,LOADISNS,TPADISNS,DDRISNS,OTHERISNS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S00227	1	CPU,SKY,SR2FT,R1,PRQ,4/2,2.9,BGA1440	U0500	CRITICAL	CPU_SKL:2.9
337S00228	1	CPU,SKY,SR2FU,R1,PRQ,4/2,2.7,BGA1440	U0500	CRITICAL	CPU_SKL:2.7
337S00229	1	CPU,SKY,SR2FQ,R1,PRQ,4/2,2.6,BGA1440	U0500	CRITICAL	CPU_SKL:2.6
998-04701	1	INTERPOSER,INTEL,BGA1440,MM940989	U0500	CRITICAL	CPU_SKL:SOCKET
337S00258	1	IC,SKL PCH-H,SFF,SR2NH,PRQ,D1,BGA939	U1100	CRITICAL	
353S00961	4	IC,CD3215,ACE,C0,USB PWR SW,BLNK,BGA96	U3100,U3200,UB300,UB400	CRITICAL	
338S00254	2	IC,TBT,ALPINE RIDGE DP,QT5S,QS,C1,BGA337	U2800,UB000	CRITICAL	
353S01016	1	IC,ISL9239HIZ,PMU,TUBA,WCSP40,2.1X3.3MM	U7000	CRITICAL	
338S00221	1	IC,PMU,P650839,7X7MM.BGA168	U7800	CRITICAL	
338S00142	1	IC,CODEC,CLIFDEN,CS42L83A,B0,WLCSP49	U6300	CRITICAL	
337S00330	1	IC,GPU,BAFFIN,ULA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_ULA
337S00331	1	IC,GPU,BAFFIN,PROA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_PROA
337S00332	1	IC,GPU,BAFFIN,LEA,A1,PS,BGA769	UA000	CRITICAL	BAFFIN_LEA
998-04866	1	INTERPOSER,AMD,C989,BGA769,VDDCI/MVDD	UA000	CRITICAL	STARDUST:VDDCI_MVDD
998-04867	1	INTERPOSER,AMD,C988,BGA769,VDDC	UA000	CRITICAL	STARDUST:VDDC
677-04532	2	SUBASSY (T&R) PCBA, AMR, INTERPOSER, X363	J5250,J5260	CRITICAL	

Development/Base BOMs

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
685-00076	1	COMMON PARTS,MLB-BAF,X363	BASE	CRITICAL	BASE_BOM
985-00126	1	DEV,MLB-BAF,X363	DEVEL	CRITICAL	DEVEL_BOM

WIFI/BT Diplexers

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
155S0979	3	FLTR,DIPLEXER,2.45/5.54GHZ,0805	U3810,U3820,U3830	CRITICAL	DIPLEXER:MURATA

Strategic Silicon

PART#	STRATEGIC VALUE	COMMENT
337S00227	08	CPU
337S00228	08	CPU
337S00229	08	CPU
333S00050	07	MAIN MEMORY
333S00070	07	MAIN MEMORY
335S00149	02	SSD NAND
335S00204	02	SSD NAND
335S00205	02	SSD NAND
335S00219	02	SSD NAND
339S00154	02	SSD CONTROLLER
339S00155	02	SSD CONTROLLER
338S00166	02	SSD PMIC
337S00225	08	GPU
337S00285	08	GPU
337S00286	08	GPU
333S00044	07	VIDEO MEMORY
333S00043	07	VIDEO MEMORY
333S00078	07	VIDEO MEMORY
333S00074	07	VIDEO MEMORY
333S00075	07	VIDEO MEMORY
343S00135	10	T208
343S00136	10	T208
343S00137	10	T208
338S00138	10	T208
338S00193	09	BERKELIUM
353S3978	02	MOJAVE
338S00097	02	SECURE ELEMENT
338S00254	08	ALPINE RIDGE
353S00961	09	ACE
338S00142	09	CLIFDEN
353S00604	07	AUDIO AMP
353S4316	08	BAYSIDE
338S00221	08	BANJO
353S00853	09	TUBA
339S00056	05	ICEBOCK
359S00006	08	GREEN CLOCK
353S00795	09	DEBUG MUX

GPU Options

BOM GROUP	BOM OPTIONS
2GB_MC_BAFFIN	FB_2GB_MICRON,VRAM:GRP1
2GB_HY_BAFFIN	FB_2GB_HYNIX,VRAM:GRP1
2GB_SM_BAFFIN	FB_2GB_SAMSUNG,VRAM:GRP2
4GB_SM_BAFFIN	FB_4GB_SAMSUNG,VRAM:GRP1
4GB_MC_BAFFIN	FB_4GB_MICRON,VRAM:GRP1

Main DRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00050	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_SAMSUNG_2133
333S00070	4	IC,SDRAM,LPDDR3-2133,32GBIT,20NM,BGA178	U2300,U2400,U2500,U2600	CRITICAL	16G_MICRON_2133

FB VDRAM Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S00044	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_MICRON
333S00043	4	IC,GDDR5,4Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_HYNIX
333S00078	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_2GB_SAMSUNG
333S00074	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,B,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_SAMSUNG
333S00075	4	IC,GDDR5,8Gb,7Gbps,1.5V,25NM,A,170 BGA	UA400,UA450,UA500,UA550	CRITICAL	FB_4GB_MICRON

Main DRAM SPD Straps

BOM GROUP	BOM OPTIONS
RAM_16G_SAMSUNG_2133	16G_SAMSUNG_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG0:L
RAM_16G_MICRON_2133	16G_MICRON_2133,RAMCFG4:L,RAMCFG3:L,RAMCFG1:L

Sub-BOM DIPLEXER

BOM NUMBER	BOM NAME	BOM OPTIONS
685-00085	DIPLEXERS,MURATA,X363G	DIPLEXER:MURATA

SYNC_MASTER=J80_MLB SYNC_DATE=07/07/2015

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 2 OF 145

SHEET 2 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S1231	1	IC,SMC12,40MHZ/50DMIPS MCU,7X7,168BGA	U5000	CRITICAL	SMC_PROG:BLANK	Blank
341S00701	1	IC,SMC-B1,EXT (v2.37F7) PVT,X363G	U5000	CRITICAL	SMC_PROG:PVT	TI
335S00013	1	IC,SPI SERIAL FLASH,64M BITS,3V,8P SOIC,QE=1	U6100	CRITICAL	BOOTROM_PROG:BLANK	Blank
341S00699	1	IC,EFI ROM (V0193), DVT, X363G	U6100	CRITICAL	BOOTROM_PROG:DVT	Macronix/Winbond
353S00926	2	IC,CD3215,ACE,B03,BLNK,BGA96	U2890,UB090	CRITICAL	UPCROM_PROG:BLANK	Blank
341S00707	1	T29,AR1 (V10.5) PVT, X363G	U2890	CRITICAL	UPCROM_PROG:DVT	Winbond
341S00708	1	T29,AR2 (V10.5) PVT, X363G	UB090	CRITICAL	UPCROM_PROG:DVT	Winbond
335S00024	1	IC,SERIAL-FLASH,2MBIT,4V,8-USON,2x3x,6MM	U3750	CRITICAL	BT_PROG:BLANK	Blank
341S00695	1	IC,BT ROM (V28), DVT, X362/X363	U3750	CRITICAL	BT_PROG:DVT	Macronix/Winbond
341S00709	1	WIFI ROM (P107) DVT,NEW,WW1,X362/X363	U3710	CRITICAL	WIFI_PROG:DVT	Rohm/On Semi
341S3565	1	IC, EDP MUX-95C, (RENESAS) V3.2.8,DVB,D2	U9800	CRITICAL	DPMUXMCU:PROG	
335S0724	1	IC,1Mbit SERIAL FLASH 2X3X0.6MM UFDFPN8 PKG	UA701	CRITICAL	GPUROM:BLANK	Blank

SYNC_MSTR=SB_MLB_BRYTA_C10A SYNC_DATE=11/30/2020

PAGE TITLE

BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 3 OF 145

SHEET 3 OF 121

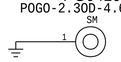
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

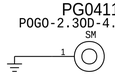
Pogo Pins

APN 870-01771

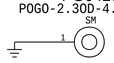
PG0410
POGO-2.30D-4.63H-SM



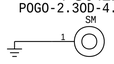
PG0411
POGO-2.30D-4.63H-SM



PG0420
POGO-2.30D-4.63H-SM

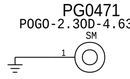


PG0421
POGO-2.30D-4.63H-SM



PG0430
POGO-2.30D-4.63H-SM

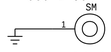
PG0471
POGO-2.30D-4.63H-SM



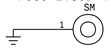
PG0470
POGO-2.30D-4.63H-SM

APN 870-01772

PG0400
POGO-2.30D-4.06H-SM



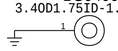
PG0401
POGO-2.30D-4.06H-SM



SMT Bosses

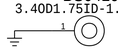
APN 860-00392

BS0400
3.40D1.75ID-1.12H-SM



USB-C Left
BOT side - North

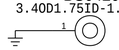
BS0410
3.40D1.75ID-1.12H-SM



USB-C Right
BOT side - North

APN 806-06520

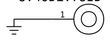
BS0420
3.40D1.75ID-1.45H-SM



DFR Touch
BOT side

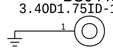
APN 806-06521

BS0430
3.40D1.75ID-1.9H-SM



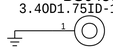
DFR Display
BOT side - Left

BS0440
3.40D1.75ID-1.9H-SM



Keyboard
BOT side - Left

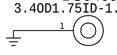
BS0450
3.40D1.75ID-1.9H-SM



Trackpad
BOT side - Left

APN 860-00413

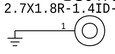
BS0460
3.40D1.75ID-1.57H-SM



Lifeboat
BOT side - North

APN 860-00469

BS0470
2.7X1.8R-1.4ID-0.91H-SM



eDP
TOP side - Left

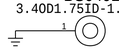
APN 806-07958

TOUCH-COWLING-HOOK-X378

BS0704
SM

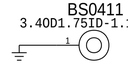
DFR Touch - TOP side

BS0401
3.40D1.75ID-1.12H-SM



USB-C Left
BOT side - South

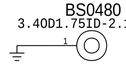
BS0411
3.40D1.75ID-1.12H-SM



USB-C Right
BOT side - South

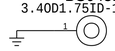
APN 806-06600

BS0480
3.40D1.75ID-2.12H-SM



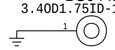
USB-C Right
BOT side - Left

BS0431
3.40D1.75ID-1.9H-SM



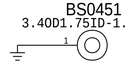
DFR Display
BOT side - Right

BS0441
3.40D1.75ID-1.9H-SM



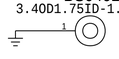
Keyboard
BOT side - Right

BS0451
3.40D1.75ID-1.9H-SM



Trackpad
BOT side - Right

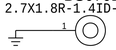
BS0461
3.40D1.75ID-1.57H-SM



Lifeboat
BOT side - South

APN 806-06600

BS0701
2.7X1.8R-1.4ID-0.91H-SM

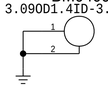


eDP
TOP side - Right

Rubber Mount Standoffs

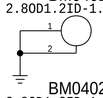
APN 860-00452

BM0400
3.09OD1.4ID-3.25H-SM

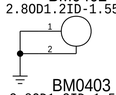


APN 860-00435

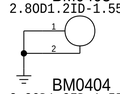
BM0401
2.8OD1.2ID-1.55H-SM



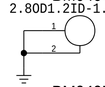
BM0402
2.8OD1.2ID-1.55H-SM



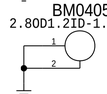
BM0403
2.8OD1.2ID-1.55H-SM



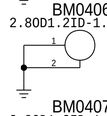
BM0404
2.8OD1.2ID-1.55H-SM



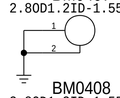
BM0405
2.8OD1.2ID-1.55H-SM



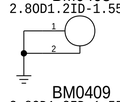
BM0406
2.8OD1.2ID-1.55H-SM



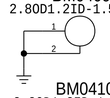
BM0407
2.8OD1.2ID-1.55H-SM



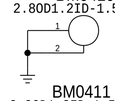
BM0408
2.8OD1.2ID-1.55H-SM



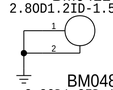
BM0409
2.8OD1.2ID-1.55H-SM



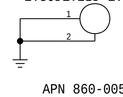
BM0410
2.8OD1.2ID-1.55H-SM



BM0411
2.8OD1.2ID-1.55H-SM

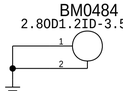


BM0483
2.8OD1.2ID-1.55H-SM



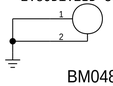
APN 860-00500

BM0484
2.8OD1.2ID-3.5H-SM

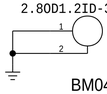


APN 860-00500

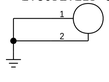
BM0485
2.8OD1.2ID-3.5H-SM



BM0486
2.8OD1.2ID-3.5H-SM



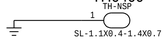
BM0487
2.8OD1.2ID-3.5H-SM



Shield Can TH

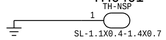
APN 998-2691

TH0400
TH-NSP



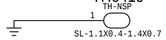
System Memory - BOT side - Left

TH0401
TH-NSP



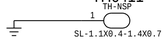
System Memory - BOT side - Right

TH0410
TH-NSP



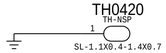
TBT Left - BOT side - North

TH0411
TH-NSP



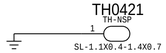
TBT Left - BOT side - South

TH0420
TH-NSP



TBT Right - BOT side - North

TH0421
TH-NSP



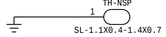
TBT Right - BOT side - South

T208 - TOP side - North

T208 through holes are non-plated... for now

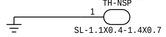
T208 - TOP side - South

TH0440
TH-NSP



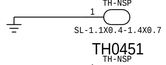
SSD - BOT side - North

TH0441
TH-NSP



SSD - BOT side - South

TH0450
TH-NSP

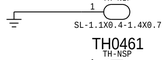


SSD - TOP side - North

TH0451
TH-NSP

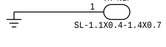
SSD - TOP side - South

TH0460
TH-NSP



Frame Buffer Memory - BOT side - Left

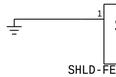
TH0461
TH-NSP



Frame Buffer Memory - BOT side - Right

Shield Can Fence

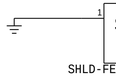
SH0400
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
DRAM - BOT side
APN 806-06590

SH0410
SM



SHLD-FENCE-MLB-M8-X379

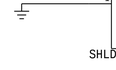
OMIT_TABLE
AR Right - BOT side
APN 806-06586

SH0420
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
AR Left - BOT side
APN 806-06588

SH0430
SM



SHLD-FENCE-M8-X379

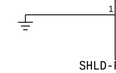
T208 - TOP side
APN 806-07814

SH0440
SM

SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - TOP side
APN 806-06584

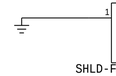
SH0450
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
SSD - BOT side
APN 806-06585

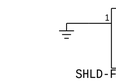
SH0460
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
Diplexer - BOT side
APN 806-06591

SH0470
SM



SHLD-FENCE-MLB-M8-X379

OMIT_TABLE
VRAM - BOT side
APN 806-08026

Shield Can Omit Table

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
806-08023	1	SHIELD,FENCE,DRAM,X378	SH0400	CRITICAL	
806-08019	1	SHIELD,FENCE,ALPINE RIDGE,RIGHT,X378	SH0410	CRITICAL	
806-08021	1	SHIELD,FENCE,ALPINE RIDGE,LEFT,X378	SH0420	CRITICAL	
806-07918	1	SHIELD,NAND,TOP,ALT,X363	SH0440	CRITICAL	
806-07917	1	SHIELD,NAND,BOTTOM,ALT,X363	SH0450	CRITICAL	
806-08024	1	SHIELD,DIPLEX,EG,X378	SH0460	CRITICAL	
806-08026	1	FENCE,VRAM,EG,X378	SH0470	CRITICAL	

BOM_COST_GROUP=MECHANICALS

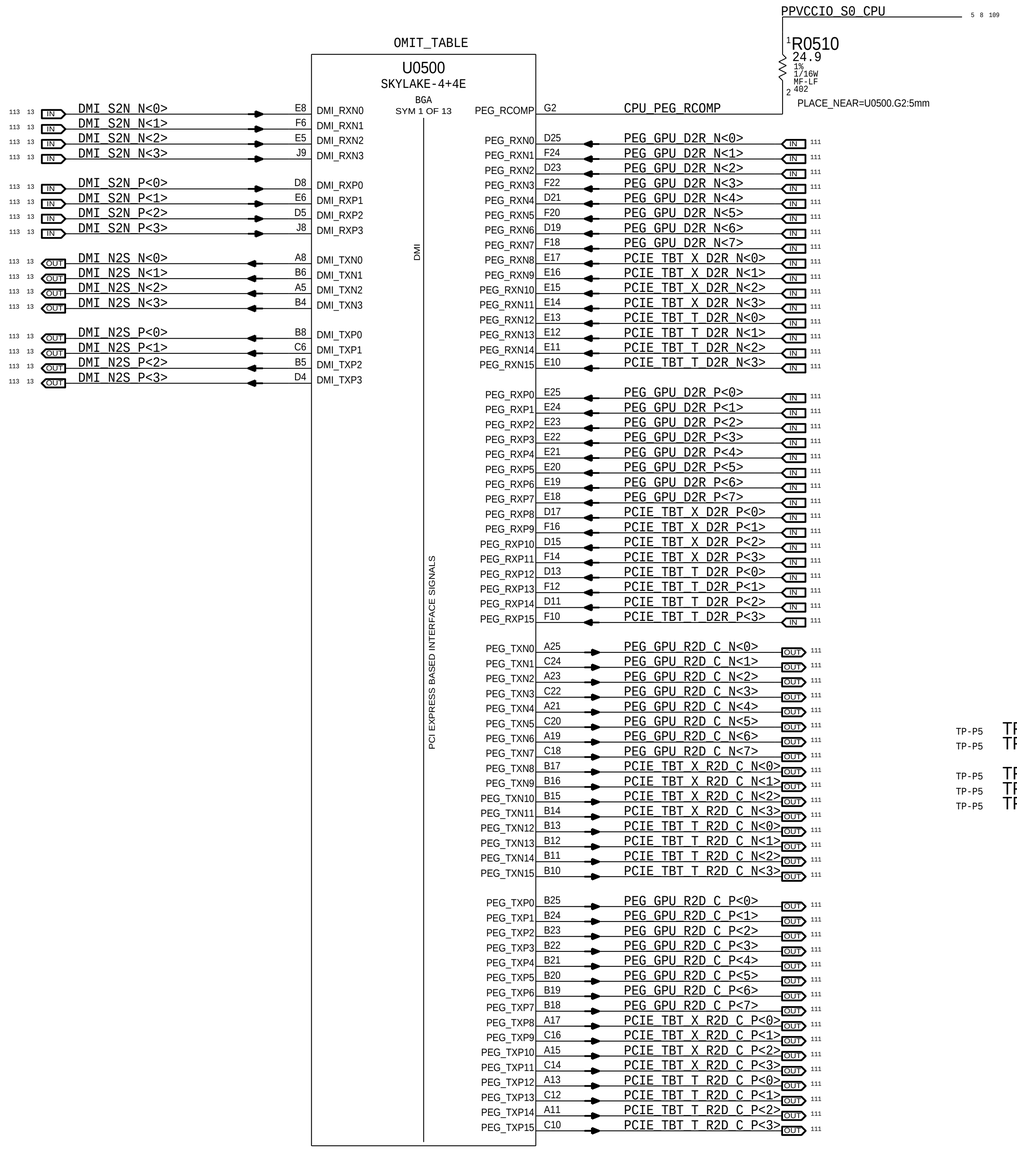
SYNC_MASTER=J80_MLB SYNC_DATE=11/16/2015

PAGE TITLE
PD Parts

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 4 OF 145
SHEET 4 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PAGE TITLE

CPU DMI/PEG/FDI/RSVD

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

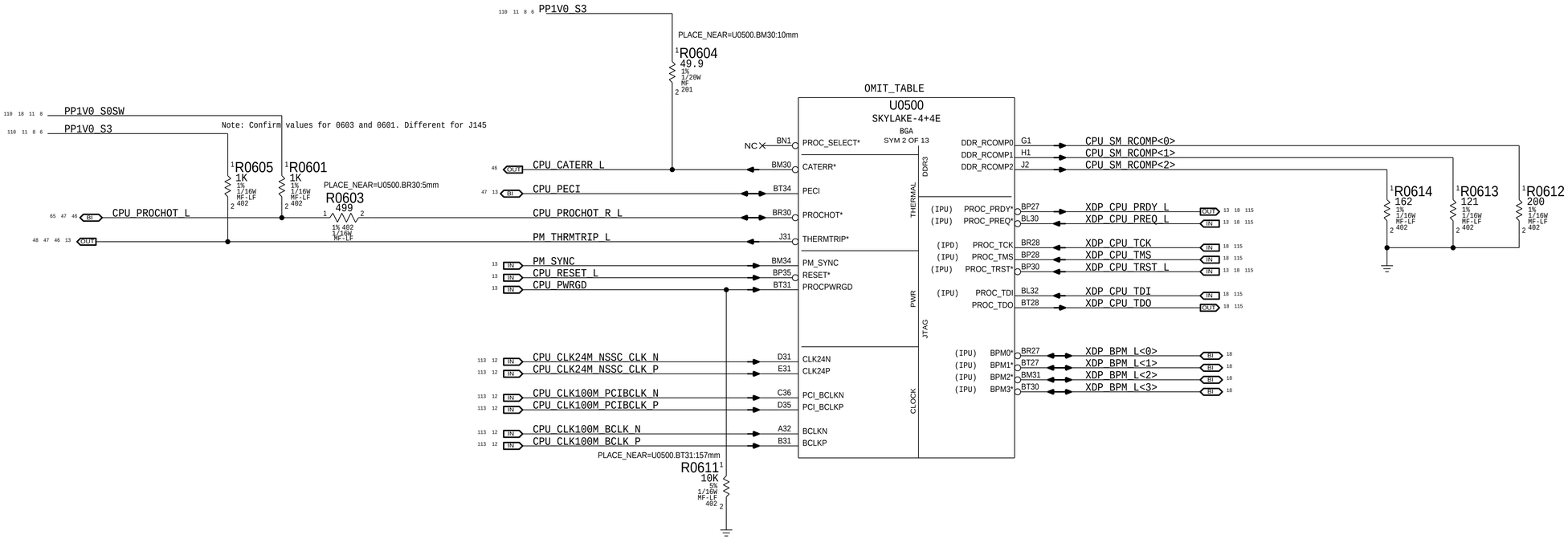
BRANCH dvt-fab10

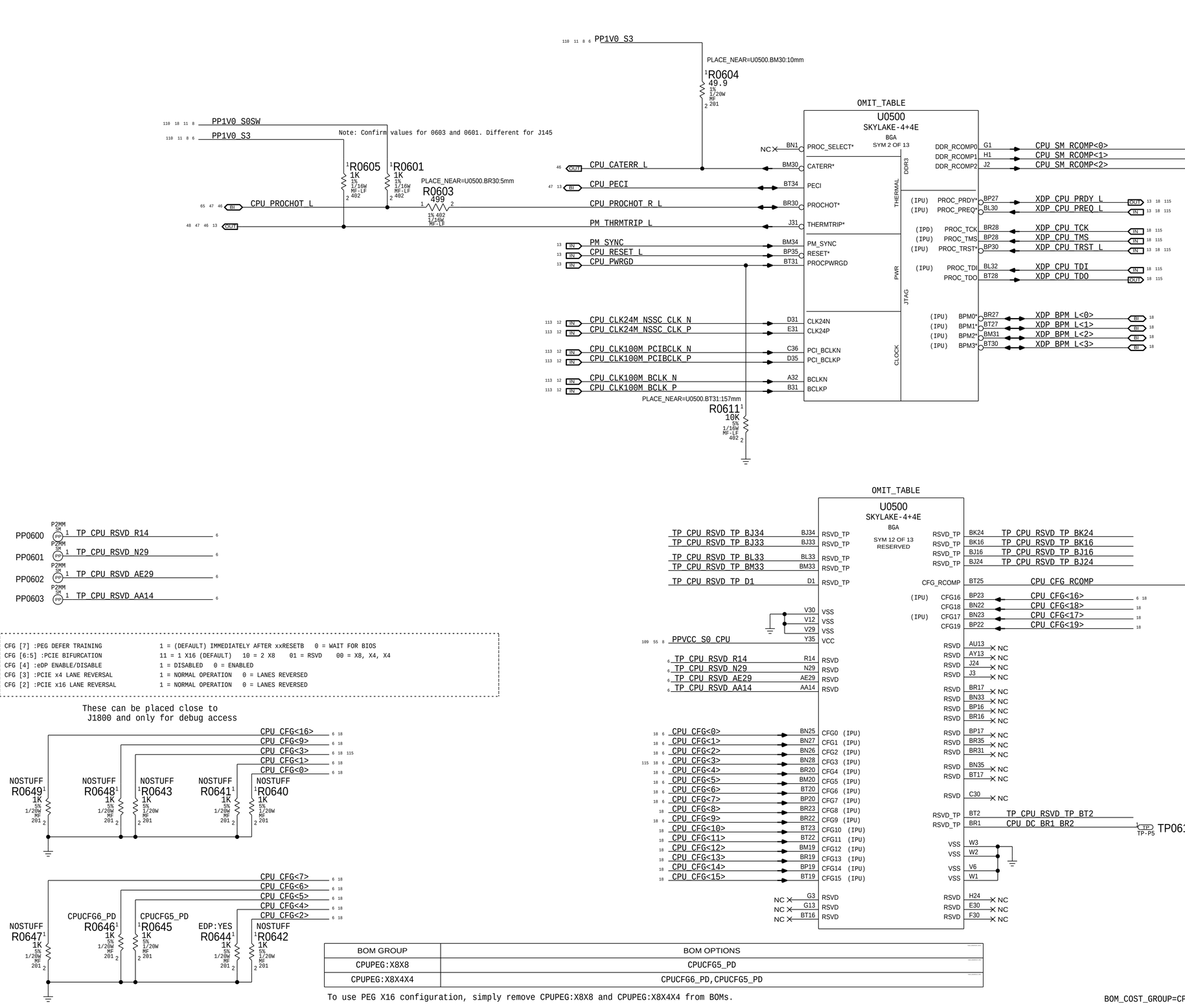
PAGE 5 OF 145

SHEET 5 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED






```
CFG [7] :PEG DEFER TRAINING              1 = (DEFAULT) IMMEDIATELY AFTER xxRESETB   0 = WAIT FOR BIOS
CFG [6:5] :PCIE BIFURCATION              11 = 1 X16 (DEFAULT)   10 = 2 X8    01 = RSVD    00 = X8, X4, X4
CFG [4] :eDP ENABLE/DISABLE              1 = DISABLED   0 = ENABLED
CFG [3] :PCIE x4 LANE REVERSAL           1 = NORMAL OPERATION   0 = LANES REVERSED
CFG [2] :PCIE x16 LANE REVERSAL          1 = NORMAL OPERATION   0 = LANES REVERSED
```

These can be placed close to
J1800 and only for debug access

BOM GROUP	BOM OPTIONS
CPUPEG:X8X8	CPUCFG5_PD
CPUPEG:X8X4X4	CPUCFG6_PD,CPUCFG5_PD

To use PEG X16 configuration, simply remove CPUPEG:X8X8 and CPUPEG:X8X4X4 from BOMs.

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2016

PAGE TITLE

CPU Clock/Misc/JTAG/CFG

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

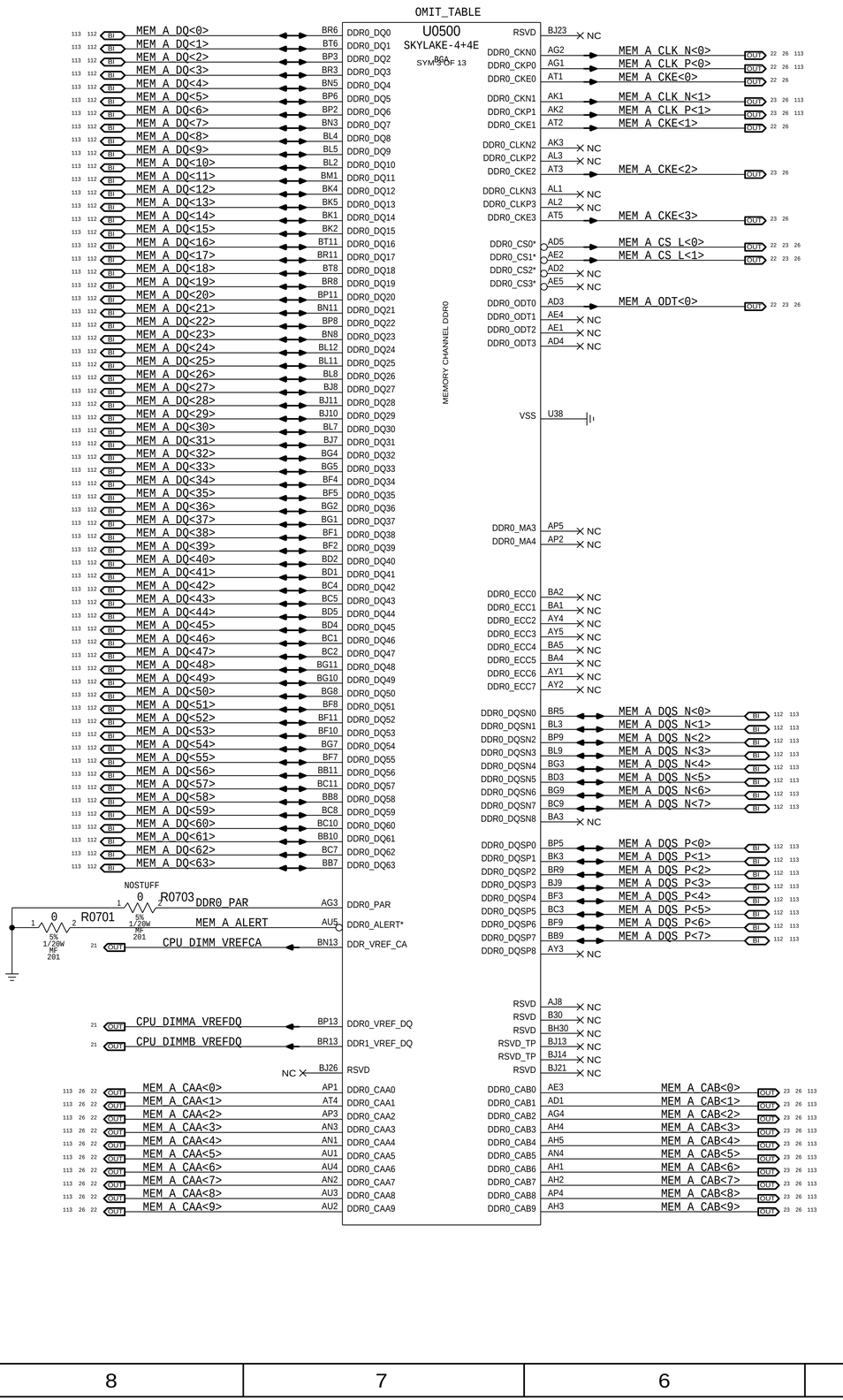
BRANCH dvt-fab10

PAGE 6 OF 145

SHEET 6 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

CPU DDR3 Interfaces

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

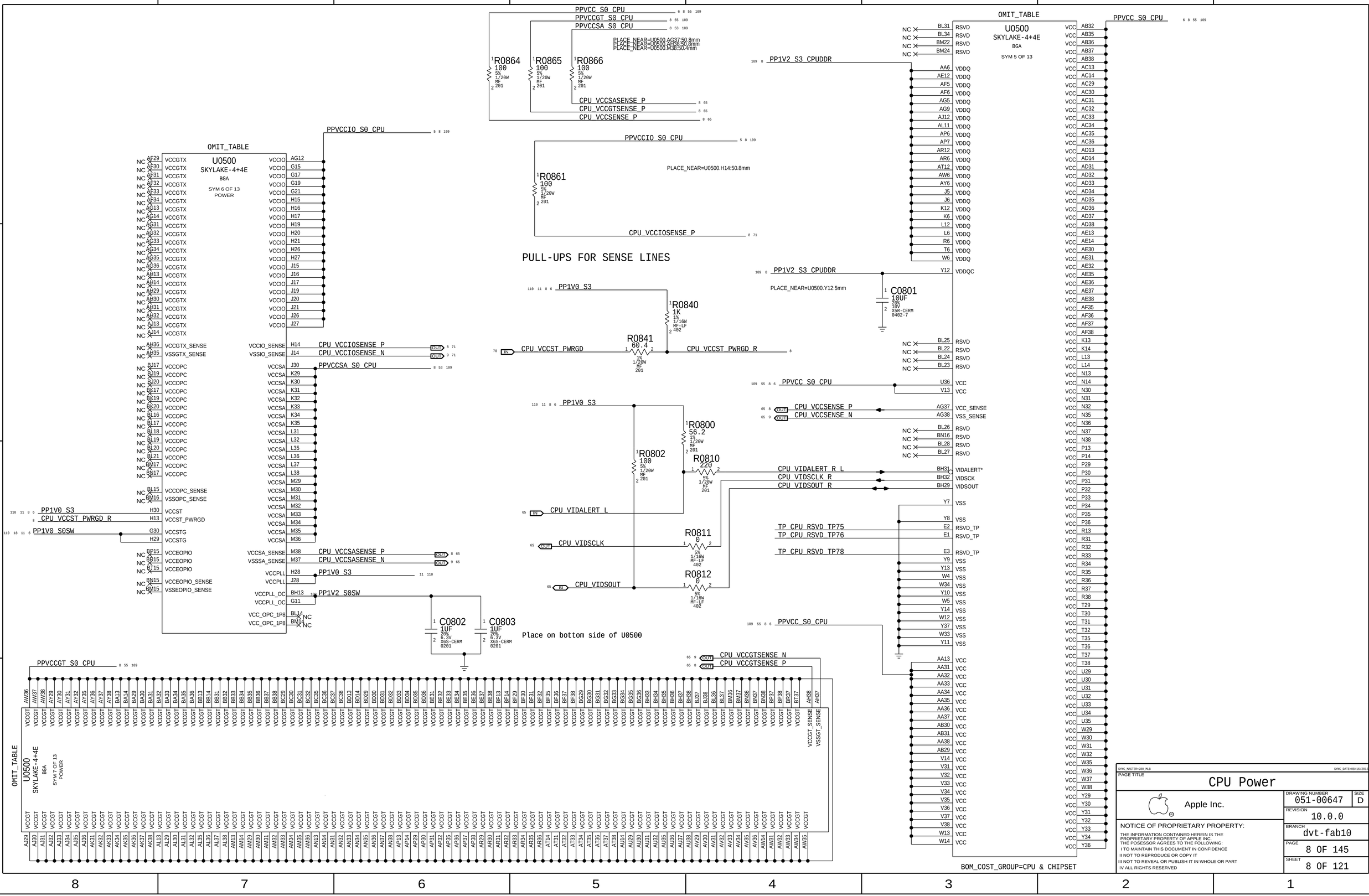
BRANCH dvt-fab10

PAGE 7 OF 145

SHEET 7 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J80_MLB SYNC_DATE=08/16/2016

PAGE TITLE

CPU Power

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

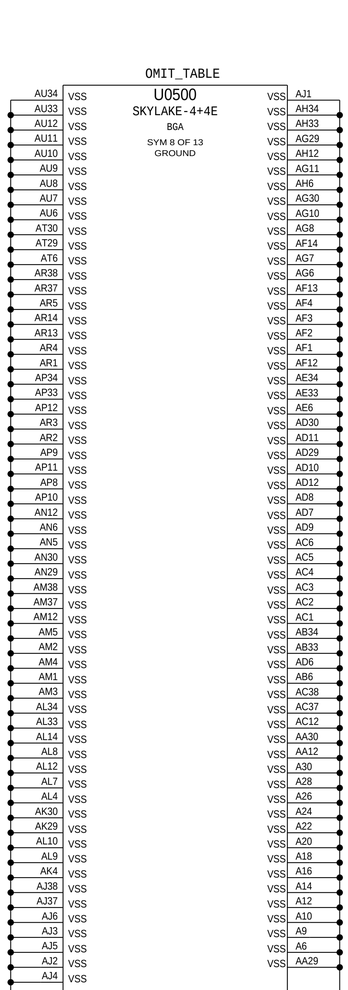
BRANCH dvt-fab10

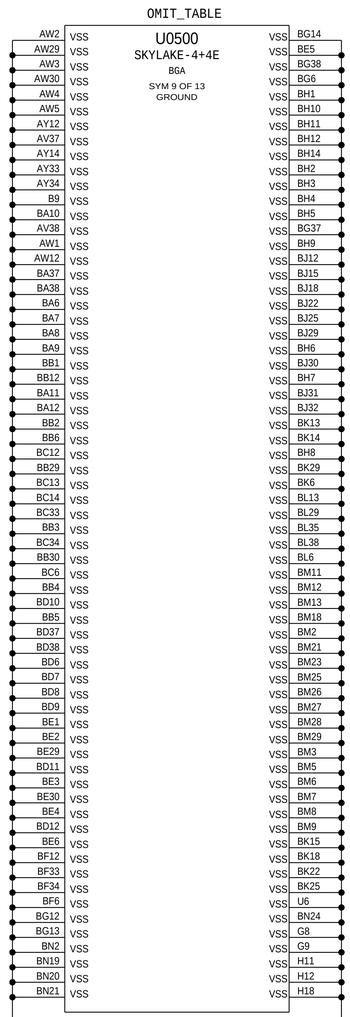
PAGE 8 OF 145

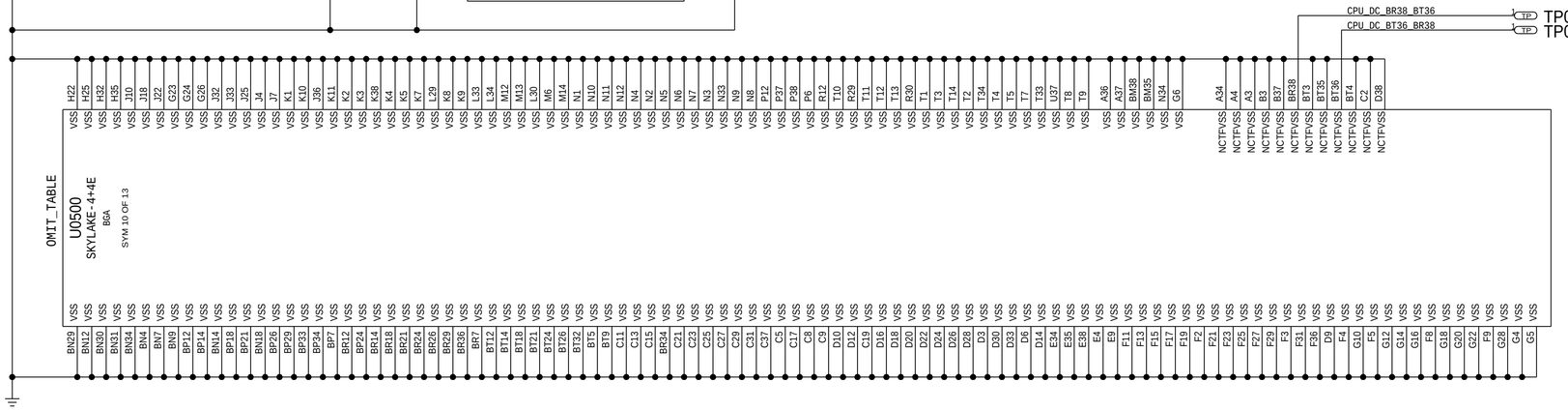
SHEET 8 OF 121

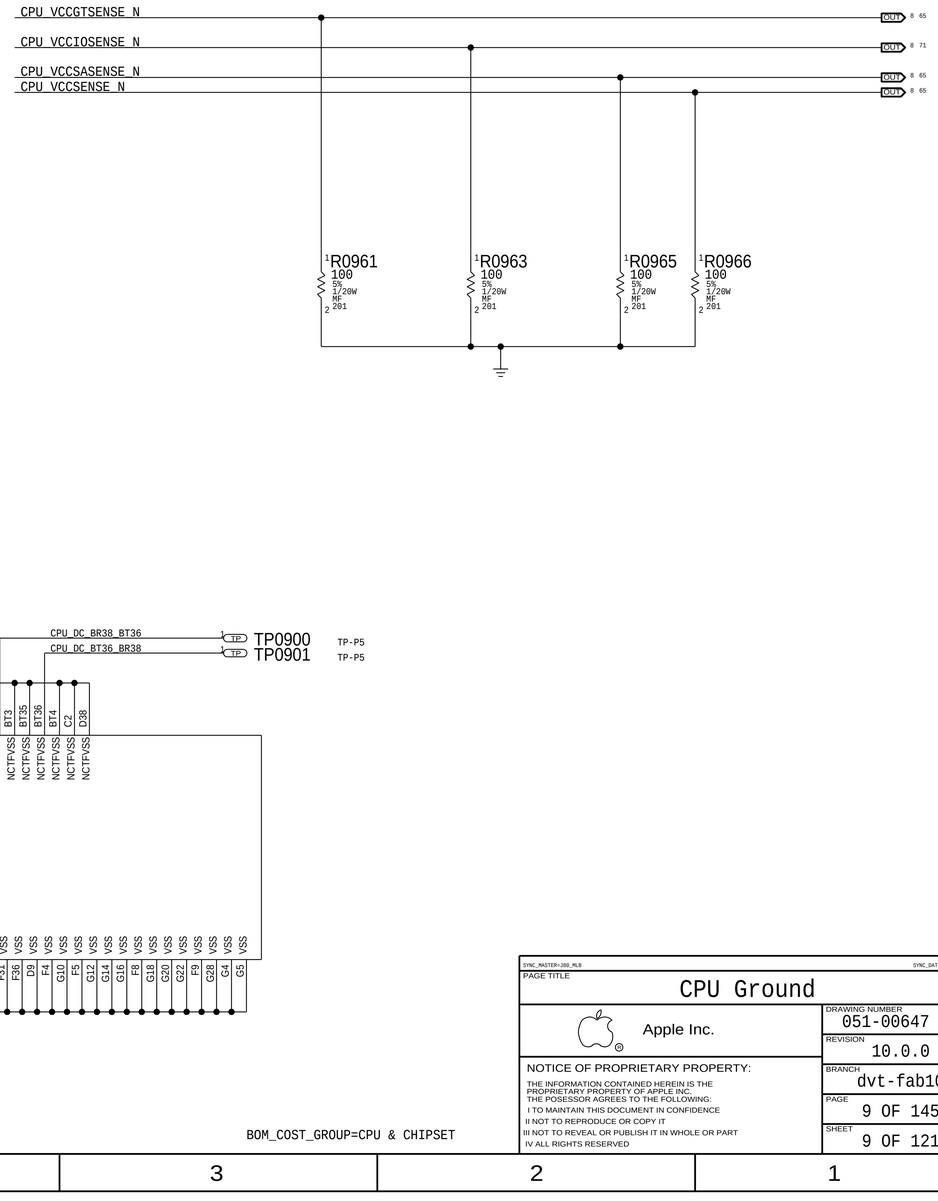
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED









BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=08/17/2015

PAGE TITLE

CPU Ground

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 9 OF 145

SHEET 9 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Vcc CPU Core Decoupling from 20140905 BOM

CPU VCORE Decoupling

Intel recommendation: 5x 220uF ESR 5m ohms ESL 1.9nH each,4x 47uF 0805 8x22uF 0603, 28x 10uF 0402, 3x 10uF 0402, 69x 1uF 0201 Board Edge: 2x 220uF, 4x 47uF rest on the back side
Apple Implementation:

109 PPVCC_S0_CPU

Place on bottom side of U0500

C1000 1UF 20% 4V CERM-X6S 0201
C1001 1UF 20% 4V CERM-X6S 0201
C1002 1UF 20% 4V CERM-X6S 0201
C1003 1UF 20% 4V CERM-X6S 0201
C1004 1UF 20% 4V CERM-X6S 0201
C1005 1UF 20% 4V CERM-X6S 0201
C1006 1UF 20% 4V CERM-X6S 0201
C1007 1UF 20% 4V CERM-X6S 0201
C1008 1UF 20% 4V CERM-X6S 0201
C1009 1UF 20% 4V CERM-X6S 0201
C1010 1UF 20% 4V CERM-X6S 0201
C1011 1UF 20% 4V CERM-X6S 0201
C1012 1UF 20% 4V CERM-X6S 0201
C1013 1UF 20% 4V CERM-X6S 0201
C1014 1UF 20% 4V CERM-X6S 0201
C1015 1UF 20% 4V CERM-X6S 0201
C1016 1UF 20% 4V CERM-X6S 0201
C1017 1UF 20% 4V CERM-X6S 0201
C1018 1UF 20% 4V CERM-X6S 0201
C1019 1UF 20% 4V CERM-X6S 0201
C1020 1UF 20% 4V CERM-X6S 0201
C1021 1UF 20% 4V CERM-X6S 0201
C1022 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1023 1UF 20% 4V CERM-X6S 0201
C1024 1UF 20% 4V CERM-X6S 0201
C1025 1UF 20% 4V CERM-X6S 0201
C1026 1UF 20% 4V CERM-X6S 0201
C1027 1UF 20% 4V CERM-X6S 0201
C1028 1UF 20% 4V CERM-X6S 0201
C1029 1UF 20% 4V CERM-X6S 0201
C1030 1UF 20% 4V CERM-X6S 0201
C1031 1UF 20% 4V CERM-X6S 0201
C1032 1UF 20% 4V CERM-X6S 0201
C1033 1UF 20% 4V CERM-X6S 0201
C1034 1UF 20% 4V CERM-X6S 0201
C1035 1UF 20% 4V CERM-X6S 0201
C1036 1UF 20% 4V CERM-X6S 0201
C1037 1UF 20% 4V CERM-X6S 0201
C1038 1UF 20% 4V CERM-X6S 0201
C1039 1UF 20% 4V CERM-X6S 0201
C1040 1UF 20% 4V CERM-X6S 0201
C1041 1UF 20% 4V CERM-X6S 0201
C1042 1UF 20% 4V CERM-X6S 0201
C1043 1UF 20% 4V CERM-X6S 0201
C1044 1UF 20% 4V CERM-X6S 0201
C1045 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1046 1UF 20% 4V CERM-X6S 0201
C1047 1UF 20% 4V CERM-X6S 0201
C1048 1UF 20% 4V CERM-X6S 0201
C1049 1UF 20% 4V CERM-X6S 0201
C1050 1UF 20% 4V CERM-X6S 0201
C1051 1UF 20% 4V CERM-X6S 0201
C1052 1UF 20% 4V CERM-X6S 0201
C1053 1UF 20% 4V CERM-X6S 0201
C1054 1UF 20% 4V CERM-X6S 0201
C1055 1UF 20% 4V CERM-X6S 0201
C1056 1UF 20% 4V CERM-X6S 0201
C1057 1UF 20% 4V CERM-X6S 0201
C1058 1UF 20% 4V CERM-X6S 0201
C1059 1UF 20% 4V CERM-X6S 0201
C1060 1UF 20% 4V CERM-X6S 0201
C1061 1UF 20% 4V CERM-X6S 0201
C1062 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C10A0 20UF 20% 2.5V X6S-CERM 0402-1
C10A1 20UF 20% 2.5V X6S-CERM 0402-1
C10A2 20UF 20% 2.5V X6S-CERM 0402-1
C10A3 20UF 20% 2.5V X6S-CERM 0402-1
C10A4 20UF 20% 2.5V X6S-CERM 0402-1
C10A5 20UF 20% 2.5V X6S-CERM 0402-1
C10A6 20UF 20% 2.5V X6S-CERM 0402-1
C10A7 20UF 20% 2.5V X6S-CERM 0402-1
C10A8 20UF 20% 2.5V X6S-CERM 0402-1
C10A9 20UF 20% 2.5V X6S-CERM 0402-1
C10B0 20UF 20% 2.5V X6S-CERM 0402-1
C10B1 20UF 20% 2.5V X6S-CERM 0402-1
C10B2 20UF 20% 2.5V X6S-CERM 0402-1
C10B3 20UF 20% 2.5V X6S-CERM 0402-1
C10B4 20UF 20% 2.5V X6S-CERM 0402-1
C10B5 20UF 20% 2.5V X6S-CERM 0402-1
C10B6 20UF 20% 2.5V X6S-CERM 0402-1
C10B7 20UF 20% 2.5V X6S-CERM 0402-1
C10B8 20UF 20% 2.5V X6S-CERM 0402-1
C10B9 20UF 20% 2.5V X6S-CERM 0402-1
C10C0 20UF 20% 2.5V X6S-CERM 0402-1
C10C1 20UF 20% 2.5V X6S-CERM 0402-1
C10C3 20UF 20% 2.5V X6S-CERM 0402-1
C10C4 20UF 20% 2.5V X6S-CERM 0402-1
C10C5 20UF 20% 2.5V X6S-CERM 0402-1
C10C6 20UF 20% 2.5V X6S-CERM 0402-1
C10C7 20UF 20% 2.5V X6S-CERM 0402-1

Noise Floor caps

NOSTUFF
C10D0 20UF 20% 2.5V X6S-CERM 0402-1
C10D1 20UF 20% 2.5V X6S-CERM 0402-1
C10D2 20UF 20% 2.5V X6S-CERM 0402-1
C10D3 20UF 20% 2.5V X6S-CERM 0402-1
C10D4 20UF 20% 2.5V X6S-CERM 0402-1
C10D5 20UF 20% 2.5V X6S-CERM 0402-1
C10D6 20UF 20% 2.5V X6S-CERM 0402-1
C10D7 20UF 20% 2.5V X6S-CERM 0402-1
C10E0 20UF 20% 2.5V X6S-CERM 0402-1
C10E1 20UF 20% 2.5V X6S-CERM 0402-1
C10E2 20UF 20% 2.5V X6S-CERM 0402-1
C10E3 20UF 20% 2.5V X6S-CERM 0402-1

C10N1 12PF 5% 25V NP0-C0G 0201
C10N2 12PF 5% 25V NP0-C0G 0201
C10N3 12PF 5% 25V NP0-C0G 0201
C10N4 12PF 5% 25V NP0-C0G 0201
C10N5 12PF 5% 25V NP0-C0G 0201
C10N6 12PF 5% 25V NP0-C0G 0201
C10N7 12PF 5% 25V NP0-C0G 0201

Place near inductors on bottom side.

NOSTUFF
C10Z1 20UF 20% 2.5V X6S-CERM 0402-1
C10Z2 20UF 20% 2.5V X6S-CERM 0402-1
C10Z3 20UF 20% 2.5V X6S-CERM 0402-1
C10Z4 20UF 20% 2.5V X6S-CERM 0402-1
C10Z5 20UF 20% 2.5V X6S-CERM 0402-1
C10Z6 20UF 20% 2.5V X6S-CERM 0402-1
C10Z7 20UF 20% 2.5V X6S-CERM 0402-1
C10Z8 20UF 20% 2.5V X6S-CERM 0402-1
C10Z9 20UF 20% 2.5V X6S-CERM 0402-1
C10ZA 20UF 20% 2.5V X6S-CERM 0402-1
C10ZB 20UF 20% 2.5V X6S-CERM 0402-1
C10ZC 20UF 20% 2.5V X6S-CERM 0402-1

C1068 220UF 20% 2V ELEC SM-COMBO
C1069 220UF 20% 2V ELEC SM-COMBO
C1070 220UF 20% 2V ELEC SM-COMBO
C1071 220UF 20% 2V ELEC SM-COMBO
C1072 220UF 20% 2V ELEC SM-COMBO
C1073 220UF 20% 2V ELEC SM-COMBO

116 109 PP1V2_S3_CPUDDR

Place on bottom side of U0500.

C1080 20UF 20% 2.5V X6S-CERM 0402-1
C1081 20UF 20% 2.5V X6S-CERM 0402-1
C1082 20UF 20% 2.5V X6S-CERM 0402-1
C1083 20UF 20% 2.5V X6S-CERM 0402-1
C1084 20UF 20% 2.5V X6S-CERM 0402-1
C1085 20UF 20% 2.5V X6S-CERM 0402-1

Place on bottom side of U0500

C1090 20UF 20% 2.5V X6S-CERM 0402-1
C1091 20UF 20% 2.5V X6S-CERM 0402-1
C1092 20UF 20% 2.5V X6S-CERM 0402-1
C1093 20UF 20% 2.5V X6S-CERM 0402-1
C1094 20UF 20% 2.5V X6S-CERM 0402-1
C1095 20UF 20% 2.5V X6S-CERM 0402-1

CPU VDDQ Decoupling

Intel recommendation: 10x 10uF 0402, 4x 22uF 0602
Apple Implementation:

CPU VCCIO Decoupling

Intel recommendation: 3x 10uF 0402 (opposite CPU)
Apple Implementation:

Place near U0500 on bottom side. U0500 on bottom side

109 PPVCCIO_S0_CPU

C1086 20UF 20% 2.5V X6S-CERM 0402-1
C1087 20UF 20% 2.5V X6S-CERM 0402-1
C1088 20UF 20% 2.5V X6S-CERM 0402-1
C1089 20UF 20% 2.5V X6S-CERM 0402-1
C108A 20UF 20% 2.5V X6S-CERM 0402-1

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J30_DT&DMA_RLB_BAFF3X SYNC_DATE=11/22/2013

PAGE TITLE: CPU Decoupling 1 [10]

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 10 OF 145
SHEET: 10 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Vcc GT Slice Core Decoupling from 20140905 BOM

CPU VGTSlice Decoupling

Intel recommendation: 7x 220uF, 6x 47uF 0805, 6x 22uF 0603, 35x 10uF 0402, 68 1uF 0201
Apple Implementation:

Board Edge: 4x220uF, 7x 47uF rest on back side

116 109 PPVCCGT_S0_CPU

Place on bottom side of U0500

C1100 1UF 20% 4V CERM-X6S 0201
C1101 1UF 20% 4V CERM-X6S 0201
C1102 1UF 20% 4V CERM-X6S 0201
C1103 1UF 20% 4V CERM-X6S 0201
C1104 1UF 20% 4V CERM-X6S 0201
C1105 1UF 20% 4V CERM-X6S 0201
C1106 1UF 20% 4V CERM-X6S 0201
C1107 1UF 20% 4V CERM-X6S 0201
C1108 1UF 20% 4V CERM-X6S 0201
C1109 1UF 20% 4V CERM-X6S 0201
C1110 1UF 20% 4V CERM-X6S 0201
C1111 1UF 20% 4V CERM-X6S 0201
C1112 1UF 20% 4V CERM-X6S 0201
C1113 1UF 20% 4V CERM-X6S 0201
C1114 1UF 20% 4V CERM-X6S 0201
C1115 1UF 20% 4V CERM-X6S 0201
C1116 1UF 20% 4V CERM-X6S 0201
C1117 1UF 20% 4V CERM-X6S 0201
C1118 1UF 20% 4V CERM-X6S 0201
C1119 1UF 20% 4V CERM-X6S 0201
C1120 1UF 20% 4V CERM-X6S 0201
C1121 1UF 20% 4V CERM-X6S 0201
C1122 1UF 20% 4V CERM-X6S 0201
C1123 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1124 1UF 20% 4V CERM-X6S 0201
C1125 1UF 20% 4V CERM-X6S 0201
C1126 1UF 20% 4V CERM-X6S 0201
C1127 1UF 20% 4V CERM-X6S 0201
C1128 1UF 20% 4V CERM-X6S 0201
C1129 1UF 20% 4V CERM-X6S 0201
C1130 1UF 20% 4V CERM-X6S 0201
C1131 1UF 20% 4V CERM-X6S 0201
C1132 1UF 20% 4V CERM-X6S 0201
C1133 1UF 20% 4V CERM-X6S 0201
C1134 1UF 20% 4V CERM-X6S 0201
C1135 1UF 20% 4V CERM-X6S 0201
C1136 1UF 20% 4V CERM-X6S 0201
C1137 1UF 20% 4V CERM-X6S 0201
C1138 1UF 20% 4V CERM-X6S 0201
C1139 1UF 20% 4V CERM-X6S 0201
C1140 1UF 20% 4V CERM-X6S 0201
C1141 1UF 20% 4V CERM-X6S 0201
C1142 1UF 20% 4V CERM-X6S 0201
C1143 1UF 20% 4V CERM-X6S 0201
C1144 1UF 20% 4V CERM-X6S 0201
C1145 1UF 20% 4V CERM-X6S 0201
C1146 1UF 20% 4V CERM-X6S 0201
C1147 1UF 20% 4V CERM-X6S 0201

Place on bottom side of U0500

C1148 1UF 20% 4V CERM-X6S 0201
C1149 1UF 20% 4V CERM-X6S 0201
C1150 1UF 20% 4V CERM-X6S 0201
C1151 1UF 20% 4V CERM-X6S 0201
C1152 1UF 20% 4V CERM-X6S 0201
C1153 1UF 20% 4V CERM-X6S 0201
C1154 1UF 20% 4V CERM-X6S 0201
C1155 1UF 20% 4V CERM-X6S 0201
C1156 1UF 20% 4V CERM-X6S 0201
C1157 1UF 20% 4V CERM-X6S 0201
C1158 1UF 20% 4V CERM-X6S 0201
C1159 1UF 20% 4V CERM-X6S 0201
C1160 1UF 20% 4V CERM-X6S 0201
C1161 1UF 20% 4V CERM-X6S 0201
C1162 1UF 20% 4V CERM-X6S 0201
C1163 1UF 20% 4V CERM-X6S 0201
C1164 1UF 20% 4V CERM-X6S 0201
C1165 1UF 20% 4V CERM-X6S 0201
C1166 1UF 20% 4V CERM-X6S 0201
C1167 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11A0 20UF 20% 2.5V X6S-CERM 0402-1
C11A1 20UF 20% 2.5V X6S-CERM 0402-1
C11A2 20UF 20% 2.5V X6S-CERM 0402-1
C11A3 20UF 20% 2.5V X6S-CERM 0402-1
C11A4 20UF 20% 2.5V X6S-CERM 0402-1
C11A5 20UF 20% 2.5V X6S-CERM 0402-1
C11A6 20UF 20% 2.5V X6S-CERM 0402-1
C11A7 20UF 20% 2.5V X6S-CERM 0402-1
C11A8 20UF 20% 2.5V X6S-CERM 0402-1
C11A9 20UF 20% 2.5V X6S-CERM 0402-1
C11B0 20UF 20% 2.5V X6S-CERM 0402-1
C11B1 20UF 20% 2.5V X6S-CERM 0402-1
C11B2 20UF 20% 2.5V X6S-CERM 0402-1
C11B3 20UF 20% 2.5V X6S-CERM 0402-1
C11B4 20UF 20% 2.5V X6S-CERM 0402-1
C11B5 20UF 20% 2.5V X6S-CERM 0402-1
C11B6 20UF 20% 2.5V X6S-CERM 0402-1
C11B7 20UF 20% 2.5V X6S-CERM 0402-1
C11B8 20UF 20% 2.5V X6S-CERM 0402-1
C11B9 20UF 20% 2.5V X6S-CERM 0402-1
C11C0 20UF 20% 2.5V X6S-CERM 0402-1
C11C1 20UF 20% 2.5V X6S-CERM 0402-1
C11C2 20UF 20% 2.5V X6S-CERM 0402-1
C11C3 20UF 20% 2.5V X6S-CERM 0402-1
C11C4 20UF 20% 2.5V X6S-CERM 0402-1
C11C5 20UF 20% 2.5V X6S-CERM 0402-1
C11C6 20UF 20% 2.5V X6S-CERM 0402-1
C11C7 20UF 20% 2.5V X6S-CERM 0402-1
C11C8 20UF 20% 2.5V X6S-CERM 0402-1
C11C9 20UF 20% 2.5V X6S-CERM 0402-1
C11D0 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11F0 20UF 20% 2.5V X6S-CERM 0402-1
C11F1 20UF 20% 2.5V X6S-CERM 0402-1
C11F2 20UF 20% 2.5V X6S-CERM 0402-1
C11F3 20UF 20% 2.5V X6S-CERM 0402-1
C11F4 20UF 20% 2.5V X6S-CERM 0402-1
C11F5 20UF 20% 2.5V X6S-CERM 0402-1
C11F6 20UF 20% 2.5V X6S-CERM 0402-1
C11F7 20UF 20% 2.5V X6S-CERM 0402-1
C11E0 20UF 20% 2.5V X6S-CERM 0402-1
C11E1 20UF 20% 2.5V X6S-CERM 0402-1
C11E2 20UF 20% 2.5V X6S-CERM 0402-1
C11E3 20UF 20% 2.5V X6S-CERM 0402-1
C11E4 20UF 20% 2.5V X6S-CERM 0402-1
C11E5 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11D4 20UF 20% 2.5V X6S-CERM 0402-1
C11D3 20UF 20% 2.5V X6S-CERM 0402-1
C11D2 20UF 20% 2.5V X6S-CERM 0402-1
C11D1 20UF 20% 2.5V X6S-CERM 0402-1

C1168 220UF 20% 2V ELEC SM-COMBO
C1169 220UF 20% 2V ELEC SM-COMBO
C1170 220UF 20% 2V ELEC SM-COMBO
C1171 220UF 20% 2V ELEC SM-COMBO
C1172 220UF 20% 2V ELEC SM-COMBO

CPU VCCSTG Decoupling

110 18 8 6 PP1V0_S0SW

Place near U0500 on bottom side

C11L1 1UF 20% 4V CERM-X6S 0201
C11L2 1UF 20% 4V CERM-X6S 0201

CPU VCCPLL and VCCST Decoupling

110 8 PP1V0_S3

110 8 6 PP1V0_S3

C11M1 1UF 20% 4V CERM-X6S 0201
C11M2 1UF 20% 4V CERM-X6S 0201

Place near U0500 on bottom side

109 PPVCCSA_S0_CPU

Place on bottom side of U0500

C11H0 1UF 20% 4V CERM-X6S 0201
C11H1 1UF 20% 4V CERM-X6S 0201
C11H2 1UF 20% 4V CERM-X6S 0201

NOSTUFF
C11I0 20UF 20% 2.5V X6S-CERM 0402-1
C11I1 20UF 20% 2.5V X6S-CERM 0402-1
C11I2 20UF 20% 2.5V X6S-CERM 0402-1
C11I3 20UF 20% 2.5V X6S-CERM 0402-1
C11I4 20UF 20% 2.5V X6S-CERM 0402-1
C11I5 20UF 20% 2.5V X6S-CERM 0402-1
C11I6 20UF 20% 2.5V X6S-CERM 0402-1
C11I7 20UF 20% 2.5V X6S-CERM 0402-1

NOSTUFF
C11J0 47UF 20% 6.3V POLY-TANT 0805
C11J1 47UF 20% 6.3V POLY-TANT 0805

C11K9 220UF 20% 2V ELEC SM-COMBO

NOTE: Intel decoupling recommendations from CBR schematics for Skylake H doc#557227 and PDG section 48.1 (document# 546884)

CPU VCCSA Decoupling

Intel recommendation: 2x 220uF, 1x 47uF 0805. 1x 22uF. 7x 10uF 0402, 3x 1uF 0201_
2x 220uF, 1x 22uF on board edge, everything else on back side
Apple Implementation:

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: CPU Decoupling 2 [11]

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 11 OF 145
SHEET: 11 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 4 OF 12

SYSTEM POWER MANAGEMENT

48 IN	SMC_PCH_SUSACK_L	AL15	GPP_A15/SUSACK* (IPU)	DRAM_RESET*	AM11	NC_PCH_DRAM_RESET_L 20
115 46 18 12 IN	PM_SYSRST_L	AJ4	SYS_RESET*	(OD) DSW_PWROK	AF8	PM_DSW_PWRGD IN 46
114 73 46 IN	PM_PCH_SYS_PWROK	AK3	SYS_PWROK	(IPD-DeepSx) WAKE*	AG12	PCIE_WAKE_L IN 12 19
115 70 IN	PM_PCH_PWROK	AJ11	PCH_PWROK	GPP_A8/CLKRUN*	AK14	LPC_CLKRUN_L BI 12 46
				GPP_A14/SUS_STAT*/ESPI_RESET*	AM15	LPC_PWRDWN_L OUT 46
114 35 20 OUT	PLT_RST_L	AG23	GPP_B13/PLTRST*	(IPU-RSMRST#) GPD8/SUSCLK	AH12	PM_CLK32K_SUSCLK_R OUT 47
115 73 46 18 IN	PM_RSMRST_L	AF12	RSMRST*	GPD10/SLP_S5*	AG10	PM_SLP_S5_L OUT 12 20 46 73
48 OUT	SMC_PCH_SUSWARN_L	AJ16	GPP_A13/SUSWARN* /SUSPWRDNACK	GPD5/SLP_S4*	AK10	PM_SLP_S4_L OUT 12 20 43 46 70 73
48 12 IN	PM_PWRBTN_L	AM10	GPD3/PWRBTN*	GPD4/SLP_S3*	AK9	PM_SLP_S3_L OUT 12 20 27 46 70 73 76 89 101 114
12	SSD_SR_EN_L	AL12	GPD1/ACPRESENT	GPD6/SLP_A*	AG11	NC_PCH_SLP_A_L 20
103 46 29 12 IN	PM_BATLOW_L (IPU)	AM12	GPD0/BATLOW*	SLP_SUS*	AH13	PM_SLP_SUS_L OUT 12 70 73
70 46 20 12 OUT	PM_SLP_S0_L	AM22	GPP_B12/SLP_S0*	SLP_LAN*	AK11	NC_PCH_SLP_LAN_L 20
111	NC_PCH_SLP_WLAN_L	AH10	GPD9/SLP_WLAN*	GPD2/LAN_WAKE*	AL9	SMC_WAKE_SCI_L IN 12 46
20	NC_PCH_PME_L	AG16	GPP_A11/PME*	GPD11/LANPHYPC	AJ13	NC_PCH_LANPHYPC 20
59 12	AUD_PWR_EN	AG18	GPP_A12/BMBUSY*/ISH_GP6 /SX_EXIT_HOLDOFF*	GPP_B2/VRALERT*	AH20	BT_LOW_PWR_L OUT 12 35

NOSTUFF R1204 0 5% 1/20W MF 0201

R1205 100K 5% 1/20W MF 201

RTC

20 IN	SYSCLK_CLK32K_PCH	AL8	RTCX1	GPP_A0/RCIN*/ESPI_ALERT1*	AM13	PCH_RCIN_L_PU 12
20 OUT	NC_PCH_CLK32K_RTCX2	AM8	RTCX2	GPP_A1/LAD0/ESPI_IO0	AK12	LPC_AD_R<0> R1440 33 1 2 5% 1/20W MF 201 LPC_AD<0> BI 46 89
12	PCH_INTRUDER_L	AJ10	INTRUDER*	GPP_A2/LAD1/ESPI_IO1	AK13	LPC_AD_R<1> R1441 33 1 2 5% 1/20W MF 201 LPC_AD<1> BI 46 89
12	PCH_SRTCRST_L	AJ8	SRTCRST*	GPP_A3/LAD2/ESPI_IO2	AG20	LPC_AD_R<2> R1442 33 1 2 5% 1/20W MF 201 LPC_AD<2> BI 46 89
12	RTC_RESET_L	AH8	RTCRST*	GPP_A4/LAD3/ESPI_IO3	AM14	LPC_AD_R<3> R1443 33 1 2 5% 1/20W MF 201 LPC_AD<3> BI 46 89
				GPP_A5/LFRAME*/ESPI_CS0*	AL14	LPC_FRAME_R_L R1444 33 1 2 5% 1/20W MF 201 LPC_FRAME_L OUT 46 89
				GPP_A6/SERIRQ/ESPI_CS1*	AH14	LPC_SERIRQ BI 12 46
				GPP_A7/PIRQA*/ESPI_ALERT0*	AJ18	SMC_RUNTIME_SCI_L IN 12 46
				GPD7/RSVD	AL11	NC_PCH_GPD7 20

PLACE_NEAR=U1100.AL14:1.25mm

ESPI/LPC

PP3V0_G3H 16 17 109

R1201 1M 5% 1/20W MF 201
R1202 20K 5% 1/20W MF 201
R1203 20K 5% 1/20W MF 201

PCH_SRTCRST_L 12
PCH_INTRUDER_L 12
RTC_RESET_L 12

C1202 1UF 10% 10V X5R 402-1
C1203 1UF 10% 10V X5R 402-1

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 2 OF 12

CLOCK SIGNALS

113 35 OUT	PCIE_CLK100M_AP_N	J5	CLKOUT_PCIE_N0	XTAL24_IN	B4	SYSCLK_CLK24M_PCH IN 20
113 35 OUT	PCIE_CLK100M_AP_P	J6	CLKOUT_PCIE_P0	XTAL24_OUT	B3	NC_PCH_CLK24M_XTALOUT OUT 20 113
111 OUT	NC_CLKOUT_PCIE_1_N	F2	CLKOUT_PCIE_N1			
111 OUT	NC_CLKOUT_PCIE_1_P	F1	CLKOUT_PCIE_P1			
111 OUT	NC_CLKOUT_PCIE_2_N	K6	CLKOUT_PCIE_N2			
111 OUT	NC_CLKOUT_PCIE_2_P	K5	CLKOUT_PCIE_P2			
27 OUT	PCIE_CLK100M_TBT_X_N	F3	CLKOUT_PCIE_N3			
27 OUT	PCIE_CLK100M_TBT_X_P	F4	CLKOUT_PCIE_P3			
101 OUT	PCIE_CLK100M_TBT_T_N	G2	CLKOUT_PCIE_N4			
101 OUT	PCIE_CLK100M_TBT_T_P	G3	CLKOUT_PCIE_P4			
113 87 OUT	PCIE_CLK100M_SSD_N	E2	CLKOUT_PCIE_N5			
113 87 OUT	PCIE_CLK100M_SSD_P	E1	CLKOUT_PCIE_P5			
111 OUT	NC_CLKOUT_PCIE_6_N	K2	CLKOUT_PCIE_N6			
111 OUT	NC_CLKOUT_PCIE_6_P	K3	CLKOUT_PCIE_P6			
111 OUT	EG_PEG_CLK100M_N	L1	CLKOUT_PCIE_N7			
111 OUT	EG_PEG_CLK100M_P	L2	CLKOUT_PCIE_P7			
111 OUT	NC_CLKOUT_PCIE_8_N	M3	CLKOUT_PCIE_N8			
111 OUT	NC_CLKOUT_PCIE_8_P	M4	CLKOUT_PCIE_P8			
111 OUT	NC_CLKOUT_PCIE_9_N	M2	CLKOUT_PCIE_N9			
111 OUT	NC_CLKOUT_PCIE_9_P	M1	CLKOUT_PCIE_P9			
111 OUT	NC_CLKOUT_PCIE_10_N	R6	CLKOUT_PCIE_N10			
111 OUT	NC_CLKOUT_PCIE_10_P	R7	CLKOUT_PCIE_P10			
111 OUT	NC_CLKOUT_PCIE_11_N	T6	CLKOUT_PCIE_N11			
111 OUT	NC_CLKOUT_PCIE_11_P	T5	CLKOUT_PCIE_P11			
111 OUT	NC_CLKOUT_PCIE_12_N	N3	CLKOUT_PCIE_N12			
111 OUT	NC_CLKOUT_PCIE_12_P	N2	CLKOUT_PCIE_P12			
20 OUT	NC_CLKOUT_PCIE_13_N	P5	CLKOUT_PCIE_N13			
20 OUT	NC_CLKOUT_PCIE_13_P	P6	CLKOUT_PCIE_P13			
111 OUT	NC_CLKOUT_PCIE_14_N	N5	CLKOUT_PCIE_N14			
111 OUT	NC_CLKOUT_PCIE_14_P	N6	CLKOUT_PCIE_P14			
111 OUT	NC_CLKOUT_PCIE_15_N	M6	CLKOUT_PCIE_N15			
111 OUT	NC_CLKOUT_PCIE_15_P	M7	CLKOUT_PCIE_P15			

XCLK_BIASREF E4 — PCH_DIFFCLK_BIASREF — R1234 2.7K 1% 1/20W MF 201 — PP1V0_SUS 110
PLACE_NEAR=U1100.E4:1.25mm

GPP_A9/CLKOUT_LPC0 /ESPI_CLK AJ14 — LPC_CLK24M_SMC_R — 22 — LPC_CLK24M_SMC BI 46
PLACE_NEAR=U1100.AJ14:1.4mm
GPP_A10/CLKOUT_LPC1 AH15 — LPC_CLK24M_DPMUX_UC_R 20
GPP_A16/CLKOUT_48 AL16 — CAMERA_PWR_EN 12

CLKOUT_ITPXDP_N L6 — NC_ITPXDP_CLK100MN OUT 18 113 115
CLKOUT_ITPXDP_P L5 — NC_ITPXDP_CLK100MP OUT 18 113 115

CLKOUT_CPUBCLK_N J3 — CPU_CLK100M_BCLK_N OUT 6 113
CLKOUT_CPUBCLK_P J4 — CPU_CLK100M_BCLK_P OUT 6 113

CLKOUT_CPUNSSC_N H1 — CPU_CLK24M_NSSC_CLK_N OUT 6 113
CLKOUT_CPUNSSC_P H2 — CPU_CLK24M_NSSC_CLK_P OUT 6 113

CLKOUT_CPUPCIBCLK_N J1 — CPU_CLK100M_PCIBCLK_N OUT 6 113
CLKOUT_CPUPCIBCLK_P J2 — CPU_CLK100M_PCIBCLK_P OUT 6 113

PCI EXPRESS CLOCKS & CONTROL

GPP_B5/SRCCLKREQ0*	AL20	AP_CLKREQ_L_R	BI	20
GPP_B6/SRCCLKREQ1*	AM19	ENETSD_CLKREQ_L	IN	20
GPP_B7/SRCCLKREQ2*	AK20	CAMERA_CLKREQ_L	IN	20
GPP_B8/SRCCLKREQ3*	AL19	TBT_X_CLKREQ_L_R	IN	20
GPP_B9/SRCCLKREQ4*	AH22	TBT_T_CLKREQ_L_R	IN	20
GPP_B10/SRCCLKREQ5*	AK22	SSD_CLKREQ_L_R	BI	20
GPP_H0/SRCCLKREQ6*	AM25	TBT_W_CLKREQ_L	IN	20
GPP_H1/SRCCLKREQ7*	AH26	EG_CLKREQ_OUT_L		111
GPP_H2/SRCCLKREQ8*	AL25	AP_S0IX_WAKE_SEL	OUT	12 19
GPP_H3/SRCCLKREQ9*	AF26	AP_S0IX_WAKE_L	IN	12 19
GPP_H4/SRCCLKREQ10*	AK26	TBT_X_CIO_PWR_EN	OUT	29
GPP_H5/SRCCLKREQ11*	AL26	TBT_T_CIO_PWR_EN	OUT	103
GPP_H6/SRCCLKREQ12*	AJ27	TBT_W_CIO_PWR_EN	OUT	20
GPP_H7/SRCCLKREQ13*	AH27	TBT_X_USB_PWR_EN	OUT	29
GPP_H8/SRCCLKREQ14*	AM26	TBT_T_USB_PWR_EN	OUT	103
GPP_H9/SRCCLKREQ15*	AK27	TBT_W_USB_PWR_EN	OUT	20

PP3V3_S0 14 20 73 110

R1238 47K 5% 1/20W MF 201
R1239 47K 5% 1/20W MF 201
R1240 47K 5% 1/20W MF 201
R1241 100K 5% 1/20W MF 201
R1242 100K 5% 1/20W MF 201
R1243 100K 5% 1/20W MF 201
R1244 100K 5% 1/20W MF 201
R1245 100K 5% 1/20W MF 201
R1246 100K 5% 1/20W MF 201

BOM_COST_GROUP=CPU & CHIPSET

110 PP3V3_S4
12 SSD_SR_EN_L — R1211 100K 5% 1/20W MF 201

110 17 16 14 PP3V3_SUS
115 46 18 12 PM_SYSRST_L — R1247 3.0K 5% 1/20W MF 201

110 17 16 15 PP3V3_SUS

110 17 16 PP3V3_S5
19 12 PCIE_WAKE_L — R1248 100K 5% 1/20W MF 201
46 12 SMC_WAKE_SCI_L — R1209 100K 5% 1/20W MF 201
48 12 PM_PWRBTN_L — R1210 1K 5% 1/20W MF 201
103 46 29 12 PM_BATLOW_L — R1212 10K 5% 1/20W MF 201

46 12 SMC_RUNTIME_SCI_L — R1207 100K 5% 1/20W MF 201
46 12 LPC_CLKRUN_L — R1208 10K 5% 1/20W MF 201
12 PCH_RCIN_L_PU — R1251 100K 5% 1/20W MF 201

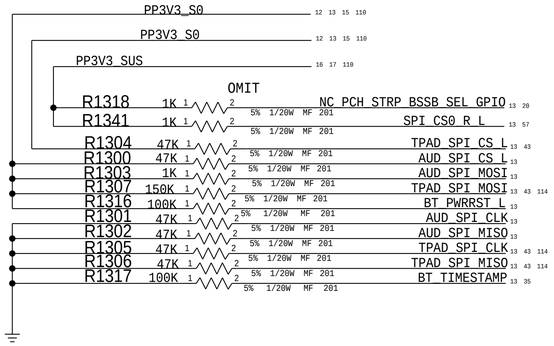
110 15 13 12 PP3V3_S0
46 12 LPC_SERIRQ — R1206 10K 5% 1/20W MF 201
59 12 AUD_PWR_EN — R1214 100K 5% 1/20W MF 201
12 CAMERA_PWR_EN — R1215 100K 5% 1/20W MF 201
19 12 AP_S0IX_WAKE_L — R1216 100K 5% 1/20W MF 201
73 46 20 12 PM_SLP_S5_L — R1230 100K 5% 1/20W MF 201
73 70 46 43 20 12 PM_SLP_S4_L — R1231 100K 5% 1/20W MF 201
114 101 89 76 73 70 46 27 20 12 PM_SLP_S3_L — R1232 100K 5% 1/20W MF 201
70 46 20 12 PM_SLP_S0_L — R1233 100K 5% 1/20W MF 201
19 12 AP_S0IX_WAKE_SEL — R1236 100K 5% 1/20W MF 201
73 70 12 PM_SLP_SUS_L — R1237 100K 5% 1/20W MF 201

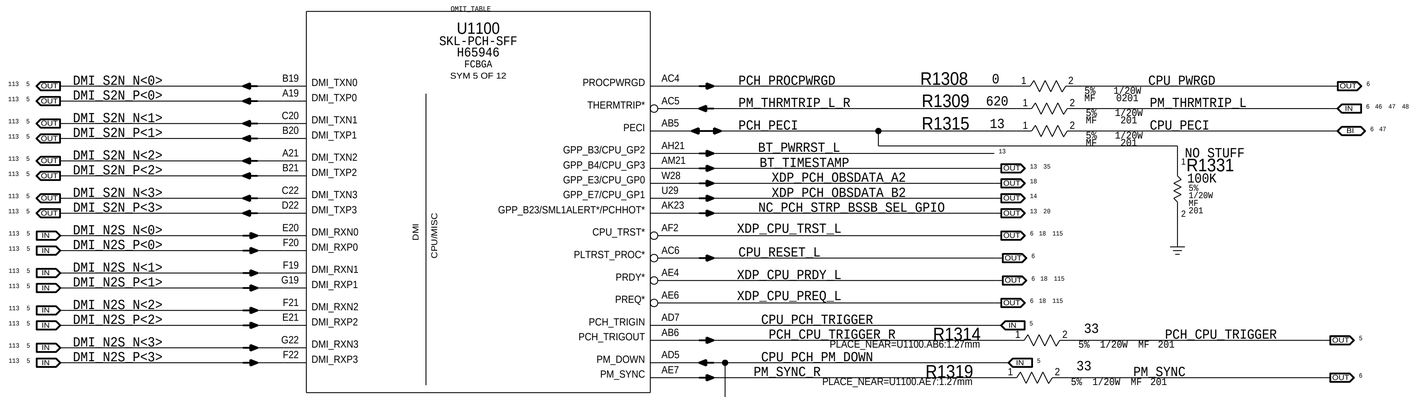
PAGE TITLE
PCH RTC/HDA/JTAG/SATA/CLK

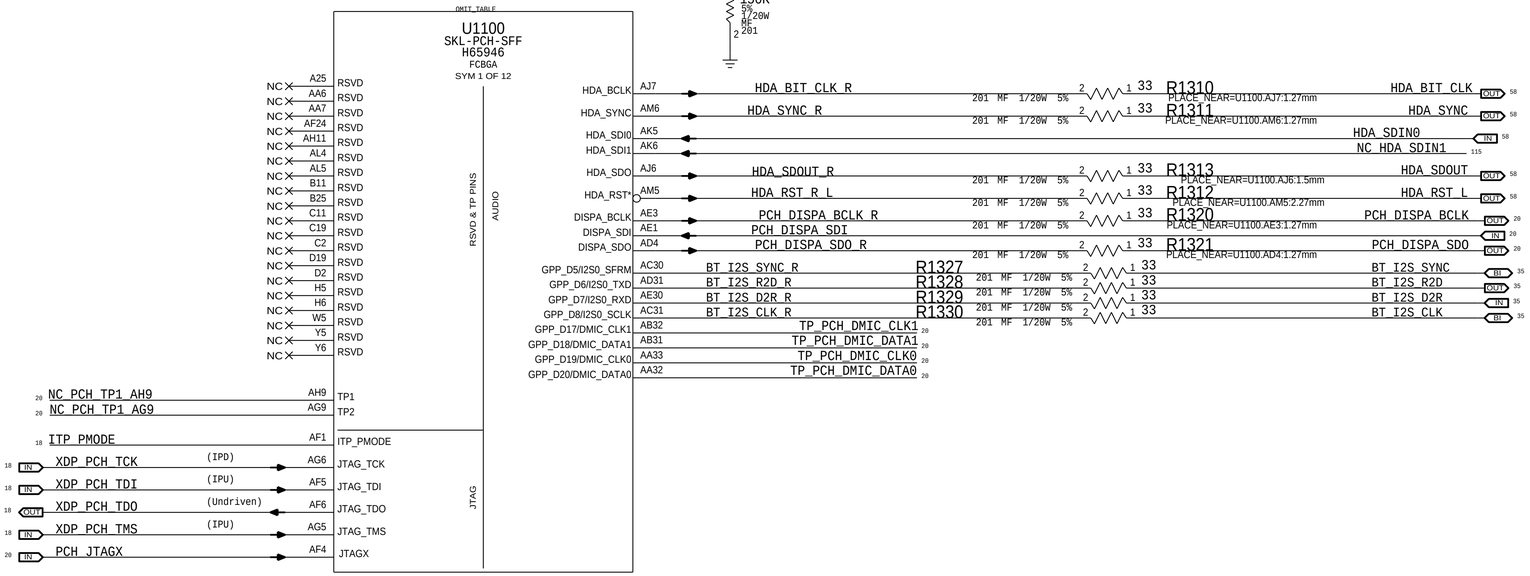
Apple Inc.

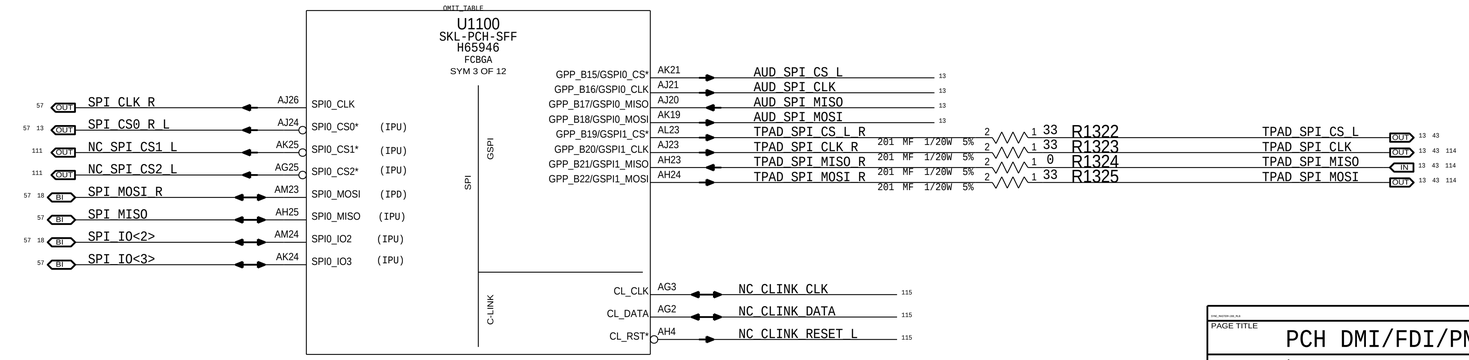
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 12 OF 145
SHEET 12 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED









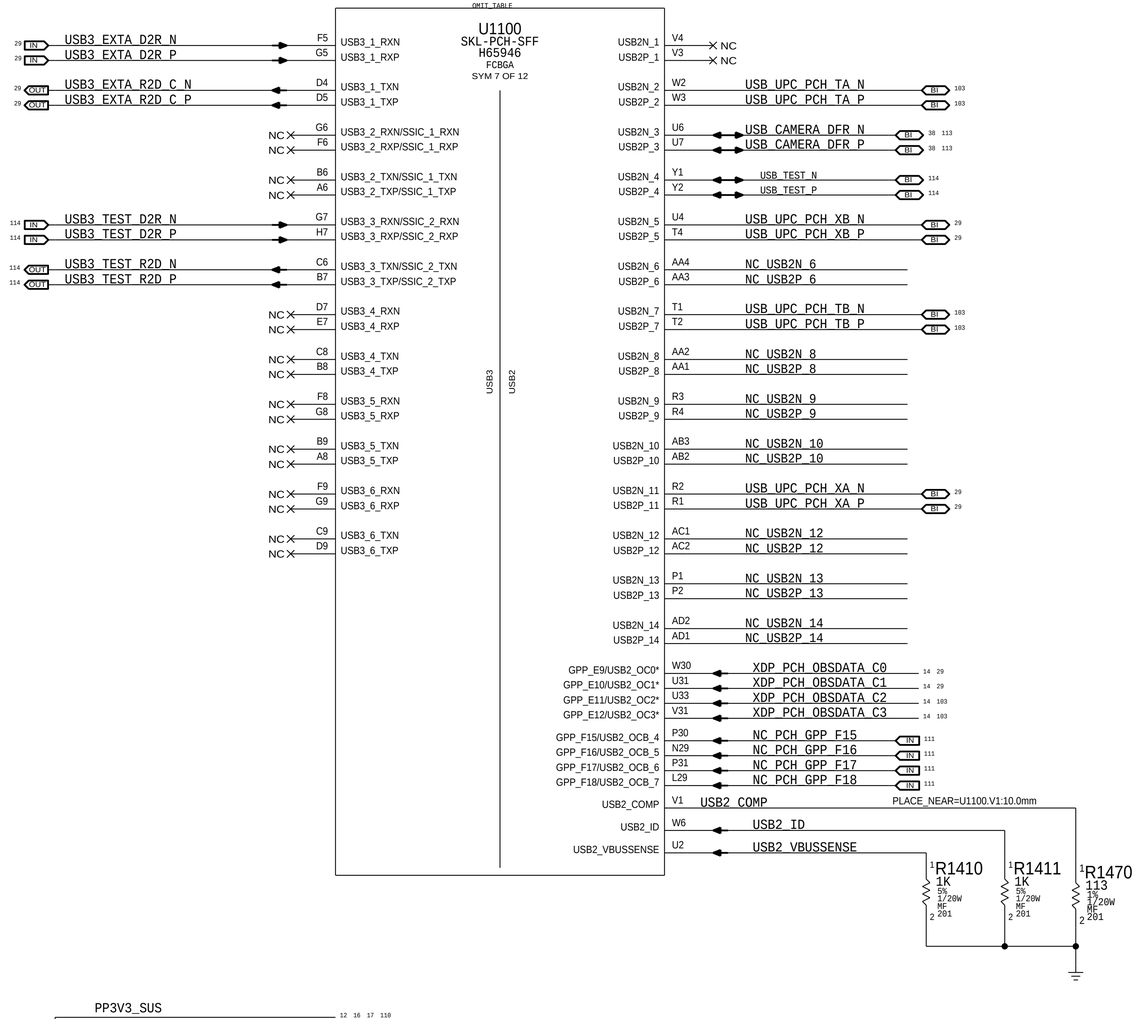
BOM_COST_GROUP=CPU & CHIPSET

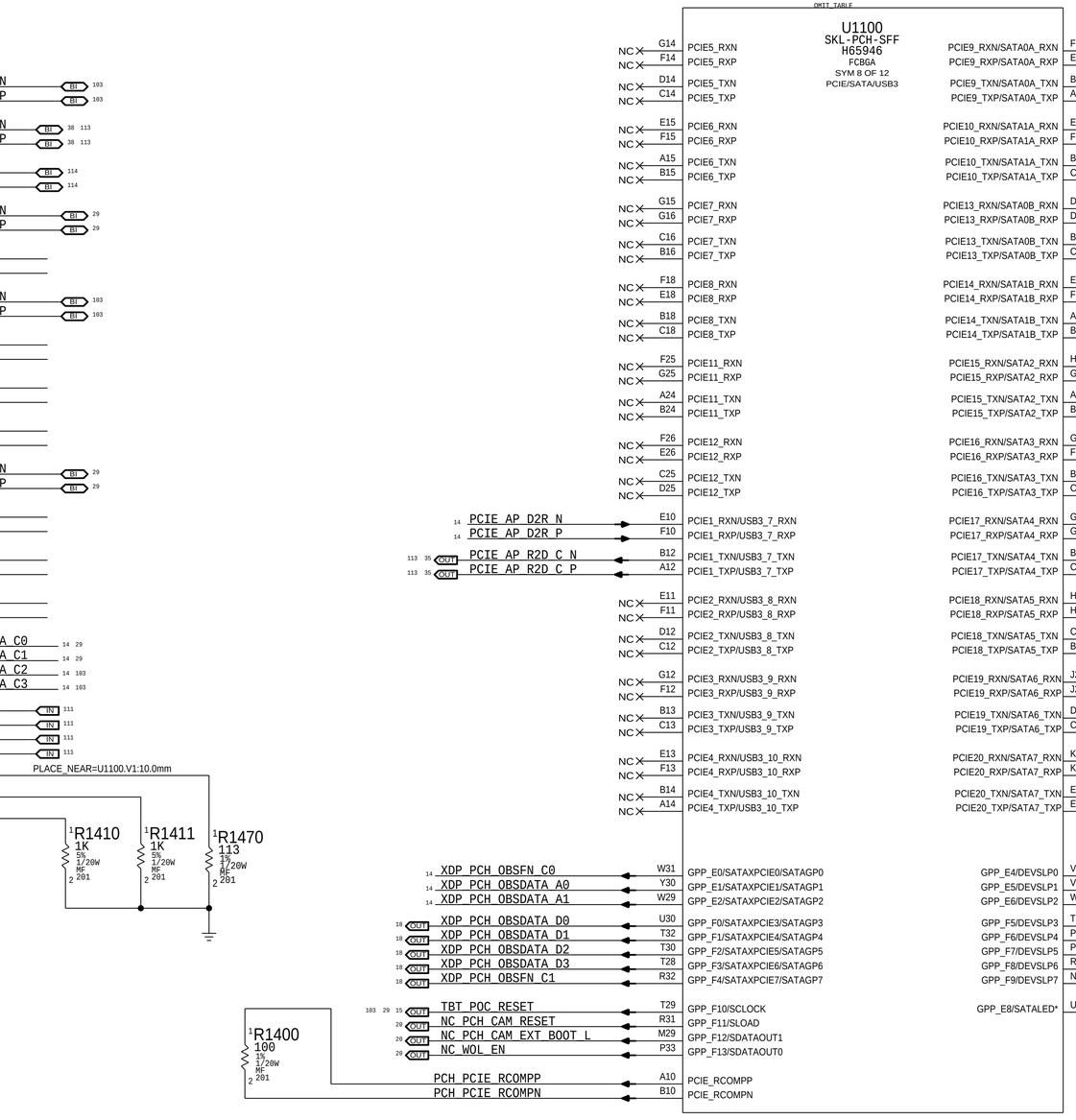
PAGE TITLE
PCH DMI/FDI/PM/GFX/PCI

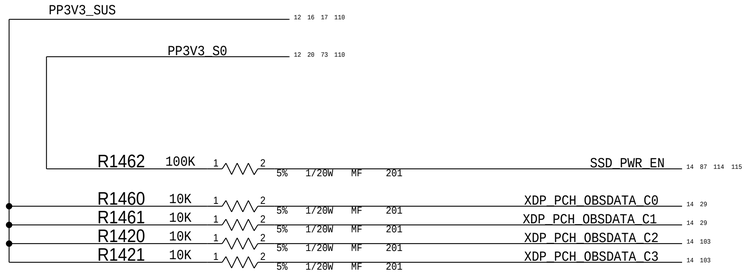
Apple Inc.

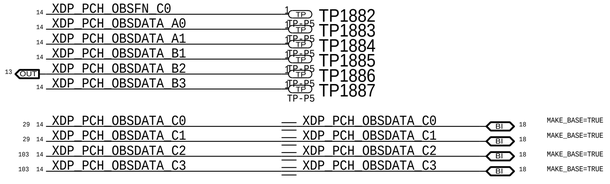
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	13 OF 145
SHEET	13 OF 121

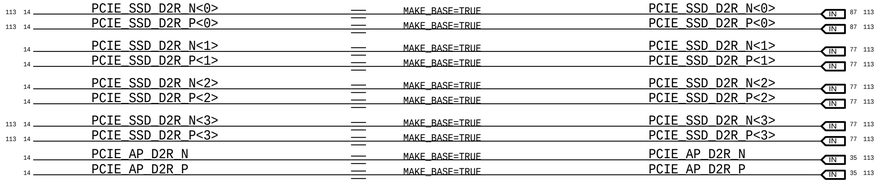
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED











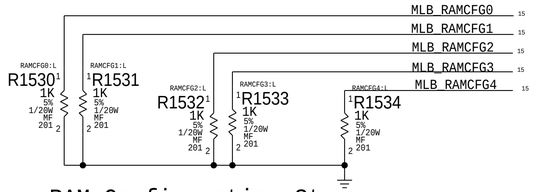
BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
PCH PCI-E/USB

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	14 OF 145
SHEET	14 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

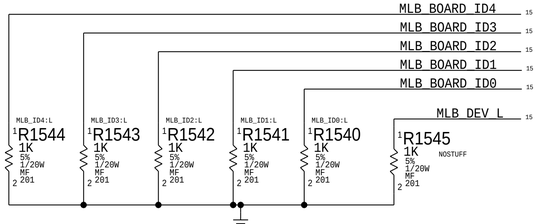


RAM Configuration Straps

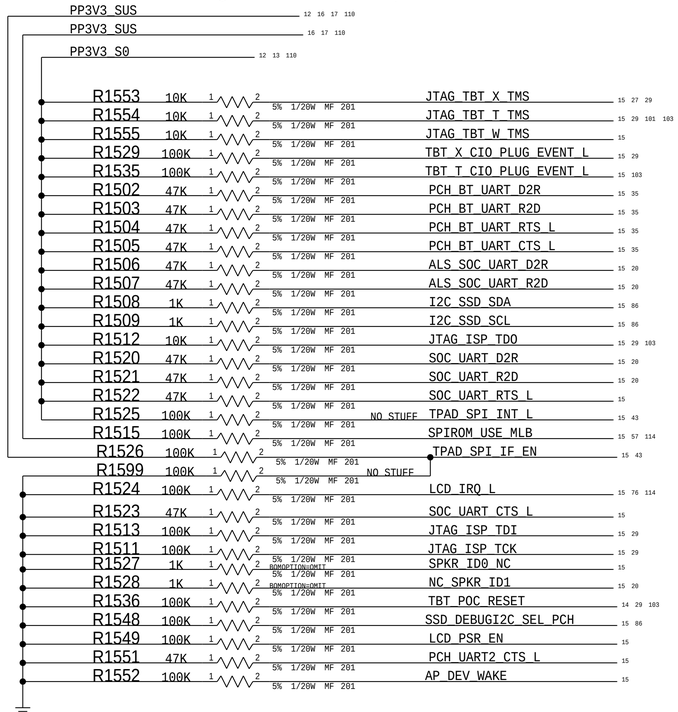
BOM GROUP	BOM OPTIONS
RAMCFG_SLOT	RAMCFG4:L,RAMCFG3:L,RAMCFG2:L,RAMCFG1:L,RAMCFG0:L

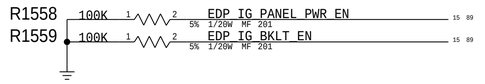
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
117S0006	0	RES,MF,1/20W,1KOHM,5%,0201,SMD		BOARD_ID:1F
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1540	BOARD_ID:1E
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541	BOARD_ID:1D
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1541,R1540	BOARD_ID:1C
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542	BOARD_ID:1B
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1540	BOARD_ID:1A
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541	BOARD_ID:19
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1542,R1541,R1540	BOARD_ID:18
117S0006	1	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543	BOARD_ID:17
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1540	BOARD_ID:16
117S0006	2	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541	BOARD_ID:15
117S0006	3	RES,MF,1/20W,1KOHM,5%,0201,SMD	R1543,R1541,R1540	BOARD_ID:14

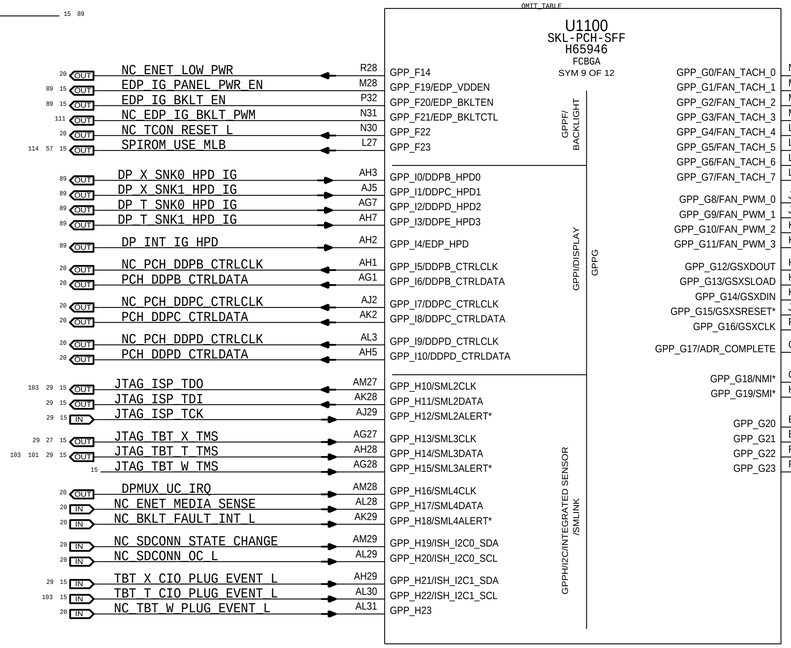
```
PROTO 0 = 0x1F = 1 1 1 1 1 (-01 PCB)
PROTO 0B = 0x1E = 1 1 1 1 0 (-02 PCB)
PROTO 1 = 0x1D = 1 1 1 0 1 (-03 PCB)
PROTO 2 = 0x1C = 1 1 1 0 0 (-04 & -05 PCB)
EVT1 = 0x1B = 1 1 0 1 1 (-06 PCB)
EVT2 = 0x1A = 1 1 0 1 0 (-07 PCB)
DVT = 0x19 = 1 1 0 0 1 (-08 PCB)
DVT1-1 = 0x18 = 1 1 0 0 0 (-09 PCB)
PVT = 0x17 = 1 0 1 1 1 (-10 PCB)
0x16 = 1 0 1 1 0
0x15 = 1 0 1 0 1
0x14 = 1 0 1 0 0
```

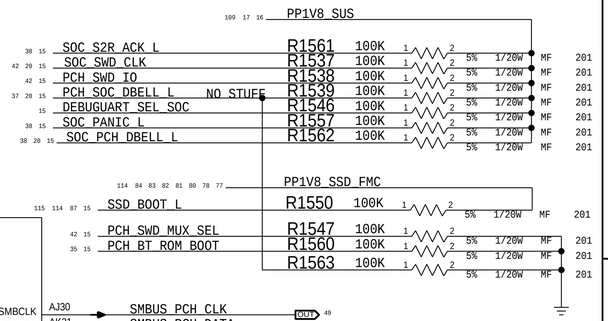


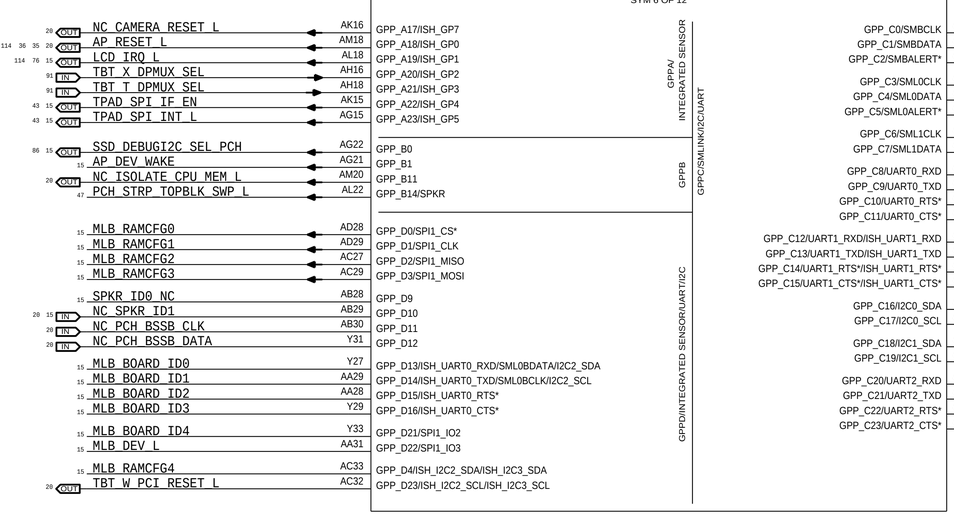
MLB BOARD ID Configuration Straps











BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE	PCH GPIO/MISC/NCTF
Apple Inc.	DRAWING NUMBER 051-00647
	SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 15 OF 145
	SHEET 15 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 10 OF 12
POWER

PRIMARY WELL
AA14 VCCPRIM_1P0
AA15 VCCPRIM_1P0
AA16 VCCPRIM_1P0
AA17 VCCPRIM_1P0
AA18 VCCPRIM_1P0
AA19 VCCPRIM_1P0
AB15 VCCPRIM_1P0
N12 VCCPRIM_1P0
N13 VCCPRIM_1P0
P15 VCCPRIM_1P0
P16 VCCPRIM_1P0
P17 VCCPRIM_1P0
P18 VCCPRIM_1P0
P19 VCCPRIM_1P0
P20 VCCPRIM_1P0
R15 VCCPRIM_1P0
R16 VCCPRIM_1P0
R17 VCCPRIM_1P0
R18 VCCPRIM_1P0
R19 VCCPRIM_1P0
R20 VCCPRIM_1P0
T11 VCCPRIM_1P0
U14 VCCPRIM_1P0
U15 VCCPRIM_1P0
U16 VCCPRIM_1P0
U17 VCCPRIM_1P0
U18 VCCPRIM_1P0
U19 VCCPRIM_1P0
V14 VCCPRIM_1P0
V15 VCCPRIM_1P0
V16 VCCPRIM_1P0
V17 VCCPRIM_1P0
V18 VCCPRIM_1P0
V19 VCCPRIM_1P0
Y14 VCCPRIM_1P0
Y15 VCCPRIM_1P0
Y16 VCCPRIM_1P0
Y17 VCCPRIM_1P0
Y18 VCCPRIM_1P0
Y19 VCCPRIM_1P0

PP1V0_SUS (110 17) → AA14

PRIMARY WELL HVCMOS
AB12 VCCPRIM_3P3
AC14 VCCPRIM_3P3
AD14 VCCPRIM_3P3

PP3V3_SUS (17 14 12 110) → AB12

PP1V_S5_PCH_DCPDSW (17) → AD19 DCPDSW_1P0

PCIE PLL EBB PRIMARY
PP1V0_SUS (110 17) → K22 VCCAPLLEBB_1P0
L22 VCCAPLLEBB_1P0

THERMAL SENSOR PW
PP3V3_S0 (110 17) → T12 VCCATS

PP1V0_SUS (110) → K10 VCCCLK1
PP1V0_SUS (110) → M10 VCCCLK2
M11 VCCCLK2
PP1V0_SUS (110) → K13 VCCCLK3
PP1V0_SUS (110) → L12 VCCCLK4
PP1V_SUS_PCH_VCCCLK5_F (17) → J11 VCCCLK5
J12 VCCCLK5

CLOCK BUFFERS PRIMARY 1.0 V

HD AUDIO POWER
AD13 VCCHDA

AUDIO PLL
VCCHDAPLL_1P0 AC11 ← PP1V_SUS_PCH_VCCHDAPLL_F

L1600
FERR-220-OHM-2A
0603
PP1V_SUS_PCH_VCCUSB2HDAPLL_F (17) 1 2
C1600 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1602 0.1UF 10% 6.3V X5R 0201
VOLTAGE=1.0V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000

MOD PHY PRIMARY
VCCMPHY_1P0 K19 ← PP1V0_SUS (17 110)
VCCMPHY_1P0 L14
VCCMPHY_1P0 L15
VCCMPHY_1P0 L16
VCCMPHY_1P0 L17
VCCMPHY_1P0 L18
VCCMPHY_1P0 L19

VCCDSW_3P3 AC20 ← PP3V3_S5 (12 17 110)
VCCDSW_3P3 AD20
VCCDSW_3P3 P10
VCCDSW_3P3 P11

DEEP SX WELL

ANALOG PLL USB3/ PCIE2/SATA2/PCIE3
VCCAMPHYPLL_1P0 K24 ← PP1V_SUSSW_PCH_VCCAMPHYPLL_F (17)
VCCAMPHYPLL_1P0 L24

MIPI PLL
VCCMIPIPLL_1P0 K21 ← PP1V_SUSSW_PCH_VCCAMPHYPLL_F (17)

GPPA PRIMARY WELL
VCCPGPPA AC19 ← PP3V3_SUS (12 15 17 110)

GPPB/GPPC/GPPH PRIMARY WELL
VCCPGPPBCH AA22 ← PP3V3_SUS (13 17 110)
VCCPGPPBCH AA23
VCCPGPPBCH AB23

GPPD PRIMARY WELL
VCCPGPPD V22 ← PP3V3_SUS (17 110)
VCCPGPPD W22
VCCPGPPD W23

GPPE/GPPEF PRIMARY WELL
VCCPGPPEF T23 ← PP3V3_SUS (15 16 17 110)
VCCPGPPEF U23 ← PP3V3_SUS (15 16 17 110)

GPPG PRIMARY WELL
GPPD 1.8V
VCCPGPPG P23 ← PP1V8_SUS (15 16 17 109)

DCPRTC AD18 ← PPDCPRTC_PCH (17)

RTC WELL SUPPLY
VCCRTC AC17 ← PP3V0_G3H (12 17 109)

RTC LOGIC PW/VRM
VCCRTCPRIM_3P3 AD16 ← PP3V3_SUS (17 110)

SPI
VCCSPI AC22 ← PP3V3_SUS (17 110)
VCCSPI AD22

ANALOG PLL USB2/VRM
VCCUSB2PLL_1P0 AB10 ← PP1V_SUS_PCH_VCCUSB2HDAPLL_F (17)
VCCUSB2PLL_1P0 AC10

L1602
FERR-220-OHM-2A
0603
PP1V8_SUS (17 16 15 109) 1 2
VCCHDA:SUS

L1601
FERR-220-OHM-2A
0603
PP1V8_S0 (109 17) 1 2
VCCHDA:S0
C1601 3.0PF +/-0.1PF 25V NP0-C0G 0201
C1603 0.1UF 10% 6.3V X5R 0201
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.2000
VOLTAGE=1.8V

PP1V8_S0_PCH_VCCHDA_F

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 11 OF 12

A11 A13 A16 A18 A20 A23 A26 A29 A5 A7 A9 AA10 AA11 AA12 AA13 AA20 AA21 AA24 AA27 AA30 AA5 AB1 AB11 AB13 AB14 AB16 AB17 AB18 AB19 AB20 AB21 AB22 AB24 AB27 AB33 AB4 AB7 AC12 AC13 AC15 AC16 AC18 AC21 AC23 AC24 AC28 AC3 AC7 AD10 AD11 AD12 AD15 AD17 AD21 AD23 AD24 AD27 AD3 AD30 AD6 AE2 AE28 AE5 AF10 AF11 AF13 AF14 AF15 AF16 AF18 AF19 AF20 AF21 AF22 AF23 AF25 AF27 AF3 AF32 AF7 AF9 AG13 AG14 AG19 AG24 AG26 AG30 AG4 AG8 AH19 AH6 AJ12 AJ15 AJ19 AJ22 — VSS

AJ25 AJ28 AJ3 AJ31 AJ9 AK18 AK30 AK4 AK7 AK8 AL10 AL13 AL21 AL24 AL27 AL6 AL7 AM16 AM7 AM9 B5 C10 C15 C21 C24 C27 C28 C3 C4 C5 C7 D10 D11 D13 D15 D16 D18 D20 D21 D23 D24 D26 D29 D3 D30 D31 D6 D8 E12 E14 E16 E19 E22 E25 E27 E29 E3 E5 E6 E8 E9 F16 F28 F30 F7 G1 G10 G11 G13 G18 G20 G21 G23 G24 G26 G32 G4 H3 H30 H4 J10 J13 J14 J15 J16 J17 J18 J19 J20 J21 J22 J23 J24 J27 J30 — VSS

OMIT_TABLE

U1100
SKL-PCH-SFF
H65946
FCBGA
SYM 12 OF 12

J7 K1 K11 K12 K14 K15 K16 K17 K18 K20 K23 K27 K32 K4 K7 L10 L11 L13 L20 L21 L23 L28 L3 L4 L7 M12 M13 M14 M15 M16 M17 M18 M19 M20 M21 M22 M23 M24 M27 M30 M5 N1 N10 N11 N14 N15 N16 N17 N18 N19 N20 N21 N22 N23 N24 N27 N32 N4 N7 P12 P13 P14 P21 P22 P24 P28 P3 P4 P7 R10 R11 R12 R13 R14 R21 R22 R23 R24 R27 R30 R33 R5 T10 T13 T14 T15 T16 T17 T18 T19 T20 T21 T22 T24 T27 — VSS

T3 T31 T7 U1 U10 U11 U12 U13 U20 U21 U22 U24 U28 U3 U32 U5 V10 V11 V12 V13 V2 V20 V21 V23 V24 V27 V28 V29 V30 V5 V6 V7 W1 W10 W11 W12 W13 W14 W15 W16 W17 W18 W19 W20 W21 W24 W27 W32 W4 W7 Y10 Y11 Y12 Y13 Y20 Y21 Y22 Y23 Y24 Y28 Y3 Y32 Y4 Y7 — VSS

VSS_NCTF_1 D1
VSS_NCTF_2 C1
VSS_NCTF_3 B1
VSS_NCTF_4 A2
VSS_NCTF_5 A3
VSS_NCTF_6 A4
VSS_NCTF_7 B2
VSS_NCTF_8 A30
VSS_NCTF_9 A31
VSS_NCTF_10 A32
VSS_NCTF_11 A33
VSS_NCTF_12 B33
VSS_NCTF_13 C33
VSS_NCTF_14 D33
VSS_NCTF_15 B32
VSS_NCTF_16 AJ33
VSS_NCTF_17 AK33
VSS_NCTF_18 AL33
VSS_NCTF_19 AM33
VSS_NCTF_20 AM32
VSS_NCTF_21 AM31
VSS_NCTF_22 AM30
VSS_NCTF_23 AL32
VSS_NCTF_24 AM4
VSS_NCTF_25 AM3
VSS_NCTF_26 AM2
VSS_NCTF_27 AM1
VSS_NCTF_28 AL1
VSS_NCTF_29 AK1
VSS_NCTF_30 AJ1
VSS_NCTF_31 AL2

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

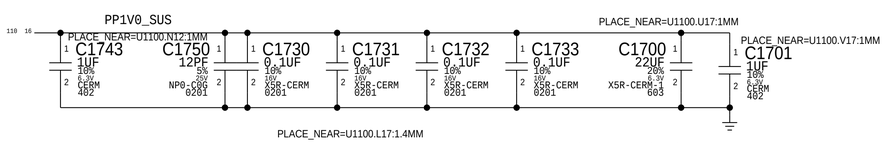
PAGE TITLE
PCH Power

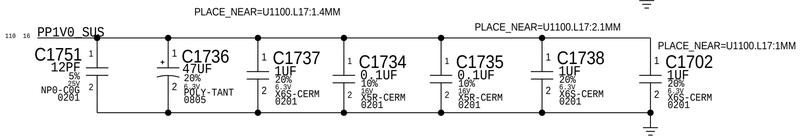
Apple Inc.

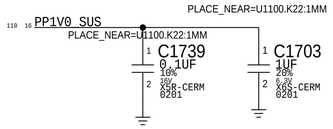
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 16 OF 145
SHEET 16 OF 121

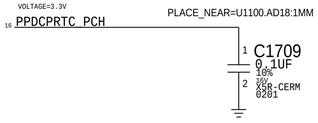
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

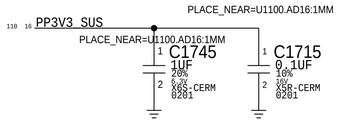
1000PF CAPS ARE INTEL PLACEHOLDERS & ALL PLACENEAR NEED TO BE UPDATED

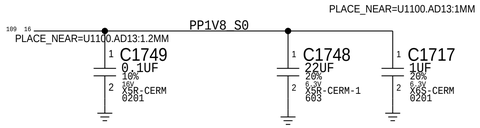


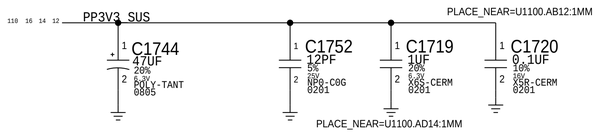


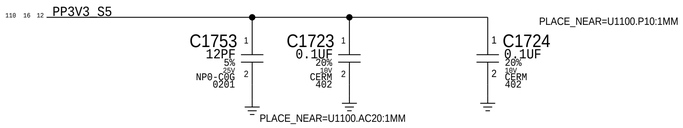


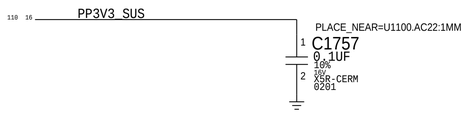


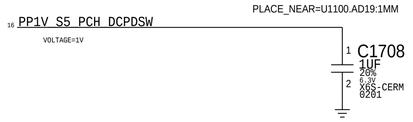


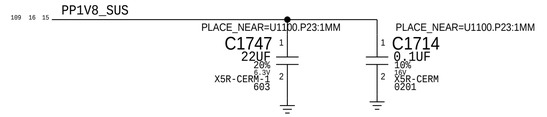


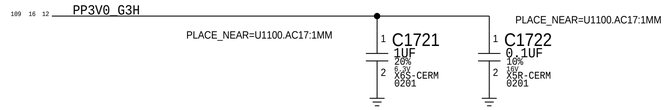






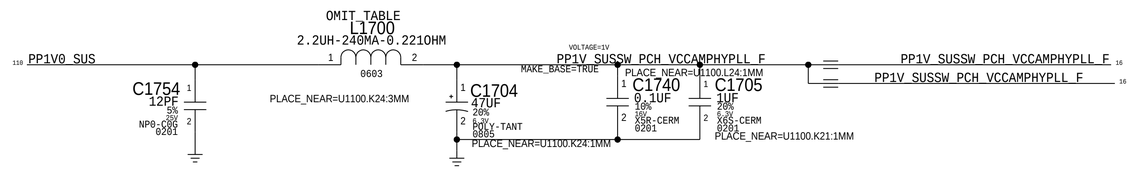


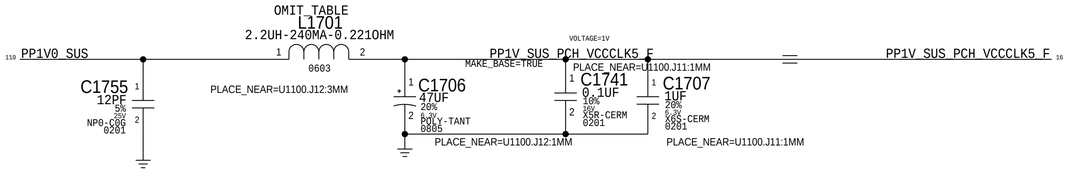


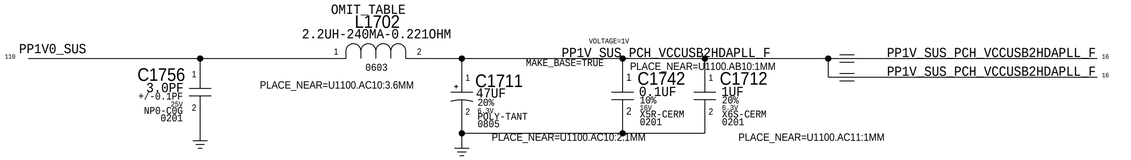


RAIL SIDE

PCH SIDE







PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
113S0022	3	RES,MF,1A MAX,00HM,5%,0603	L1700,L1701,L1702		

Current data from LPT EDS (doc #486708, Rev 1.0).

BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE

PCH DECOUPLING

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 17 OF 145

SHEET 17 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Primary / Merged (CPU/PCH) Micro2-XDP

Extra BPM Testpoints

XDP_BPM_L<0> → TP1800
XDP_BPM_L<1> → TP1801
XDP_BPM_L<2> → TP1802
XDP_BPM_L<3> → TP1803
(TP-P6)

PP1V0_SUS

PULL CFG<3> LOW WHEN XDP PRESENT
PLACE_NEAR=U0500.BN28:2.54MM
XDP:YES R1801 1K 5% 1/20W MF 201 — NO_XNET_CONNECTION

XDP_PRESENT_CPU

XDP_CONN J1800
DF40RC-60DP-0.4V
M-ST-SM1

NOTE: This is not the standard XDP pinout.
Use with 921-0133 Adapter Flex to
support chipset debug.

XDP_PIN_1			
OBSEN_A0	XDP_CPU_PREQ_L	OBSEN_C0	CPU_CFG<17>
OBSEN_A1	XDP_CPU_PRDY_L	OBSEN_C1	CPU_CFG<16>
OBSDATA_A0	CPU_CFG<0>	OBSDATA_C0	CPU_CFG<8>
OBSDATA_A1	CPU_CFG<1>	OBSDATA_C1	CPU_CFG<9>
OBSDATA_A2	CPU_CFG<2>	OBSDATA_C2	CPU_CFG<10>
OBSDATA_A3	CPU_CFG<3>	OBSDATA_C3	CPU_CFG<11>
OBSEN_B0	NC	OBSEN_D0	CPU_CFG<19>
OBSEN_B1	NC	OBSEN_D1	CPU_CFG<18>
OBSDATA_B0	CPU_CFG<4>	OBSDATA_D0	CPU_CFG<12>
OBSDATA_B1	CPU_CFG<5>	OBSDATA_D1	CPU_CFG<13>
OBSDATA_B2	CPU_CFG<6>	OBSDATA_D2	CPU_CFG<14>
OBSDATA_B3	CPU_CFG<7>	OBSDATA_D3	CPU_CFG<15>
HOOK0	XDP_PM_RSMRST_L	ITPCLK/HOOK4	NC_ITPXDP_CLK100MP
HOOK1	XDP_CPU_PWRBTN_L	ITPCLK#/HOOK5	NC_ITPXDP_CLK100MN
VCC_OBS_AB		VCC_OBS_CD	
HOOK2	NC	RESET#/HOOK6	ITP_PMODE
HOOK3	SPI_MOSI_R_CONN	DBR#/HOOK7	XDP_DBRESET_L
SDA	NC	TDO	
SCL	NC	TRSTn	
TCK1	XDP_PCH_TCK	TDI	
TCK0		TMS	
		XDP_PRESENT#	

64 63 — 518S0047

PP3V3_SUS — PLACE_NEAR=J1800.48:2.54MM
XDP:YES R1804 1K 5% 1/20W MF 201

PM_RSMRST_L → R1800 1K XDP:YES 5% 1/20W MF 201 — PLACE_NEAR=U1100.AF12:3.8MM
PM_PWRBTN_L → R1802 10 XDP:YES 5% 1/20W MF 201 — PLACE_NEAR=U1100.AM10:3MM
SPI_MOSI_R → R1803 1K XDP:YES 5% 1/20W MF 201 — PLACE_NEAR=U1100.AM23:2.54MM
XDP_CPU_TCK → R1835 0 XDP:YES 5% 1/20W MF 0201 — PLACE_NEAR=J1800.58:28MM
PCH_JTAGX

XDP_PCH_TCK

C1804 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.42:28MM
C1800 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.44:28MM
C1801 0.1UF 10% 6.3V CERM-X5R 0201 — PLACE_NEAR=J1800.43:28MM, PLACE_NEAR=J1800.47:28MM
C1806 0.1UF 10% 6.3V CERM-X5R 0201

R1830 1K 5% 1/20W MF 201 — PLACE_NEAR=U0500.EB:2.54MM

R1806 0 5% 1/20W MF 0201 — PM_SYSRST_L

PP1V0_S0SW

XDP_PCH_TDO	R1890 51	PLACE_NEAR=U1100.AF6:28MM	XDP:YES
XDP_PCH_TDI	R1891 51	PLACE_NEAR=U1100.AF5:28MM	XDP:YES
XDP_PCH_TMS	R1892 51	PLACE_NEAR=U1100.AG5:28MM	XDP:YES
XDP_CPU_TDO	R1810 51	PLACE_NEAR=U0500.BT28:28MM	XDP:YES
XDP_CPU_TCK	R1813 51	PLACE_NEAR=U0500.BR28:28MM	XDP:YES
XDP_PCH_TCK	R1897 51	PLACE_NEAR=U1100.AG6:28MM	NOSTUFF
XDP_PCH_TRST_L	R1898 51	PROPER WAY TO TERMINATE?	NOSTUFF

ROUTE IN STAR TOPOLOGY FROM XDP CONNECTOR.

R1821 0	PLACE_NEAR=J1800.51:2.54MM	XDP:YES	XDP_CPU_TDO
R1822 0	PLACE_NEAR=J1800.53:2.54MM	XDP:YES	XDP_CPU_TRST_L
R1823 0	PLACE_NEAR=J1800.55:2.54MM	XDP:YES	XDP_CPU_TDI
R1824 0	PLACE_NEAR=J1800.57:2.54MM	XDP:YES	XDP_CPU_TMS

XDP_PCH_TDO
XDP_PCH_TRST_L
XDP_PCH_TDI
XDP_PCH_TMS

PCH XDP Signals

These signals do not connect to the Primary (Merged) XDP connector in this architecture.
The PDG puts them on a secondary XDP connector that is only needed in some PCH debugging situation.
They are listed here to show their secondary XDP functions and to provide test points for signals that are not used elsewhere.

PCH/XDP Signals — Non-XDP Signals

XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_C0	TP1873
XDP_PCH_OBSDATA_C1	TP1874
XDP_PCH_OBSDATA_C2	TP1875
XDP_PCH_OBSDATA_C3	TP1876
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C1	TP1881

PP3V3_SUS
XDP:YES R1850 100K 5% 1/20W MF 201

PP3V3_SUS
XDP:YES C1830 0.1UF 10% 10V X5R-CERM 0201

U1830 74AUP1G07GF SOT891 (VCC, A, NC, GND, Y, (OD), NC, NC)

SPI_IO2_STRAP_L — PLACE_NEAR=U1830.4:7.54MM
R1831 1.5K MF 5% 1/20W 201 — SPI_IO<2> (STRAP TO PCH) — NO_XNET_CONNECTION
PLACE_NEAR=U1830.4:2.54MM
R1832 49.9 1% 1/20W 201 NOSTUFF — NO_XNET_CONNECTION
XDP_PRESENT_L

NEED TO CONNECT TO VCCST, *STG POWER LOGIC

Unused GPIOs have TPs.

USB Overcurrents are aliased, do not cause USB OC# events during PCH debug.

JTAG_ISP (non-TMS) nets are aliased, do not attempt bit-banged JTAG during PCH debug.

BOM_COST_GROUP=DEBUG

DESIGN: X502/MLB
LAST CHANGE: Mon Jun 15 22:04:28 2015

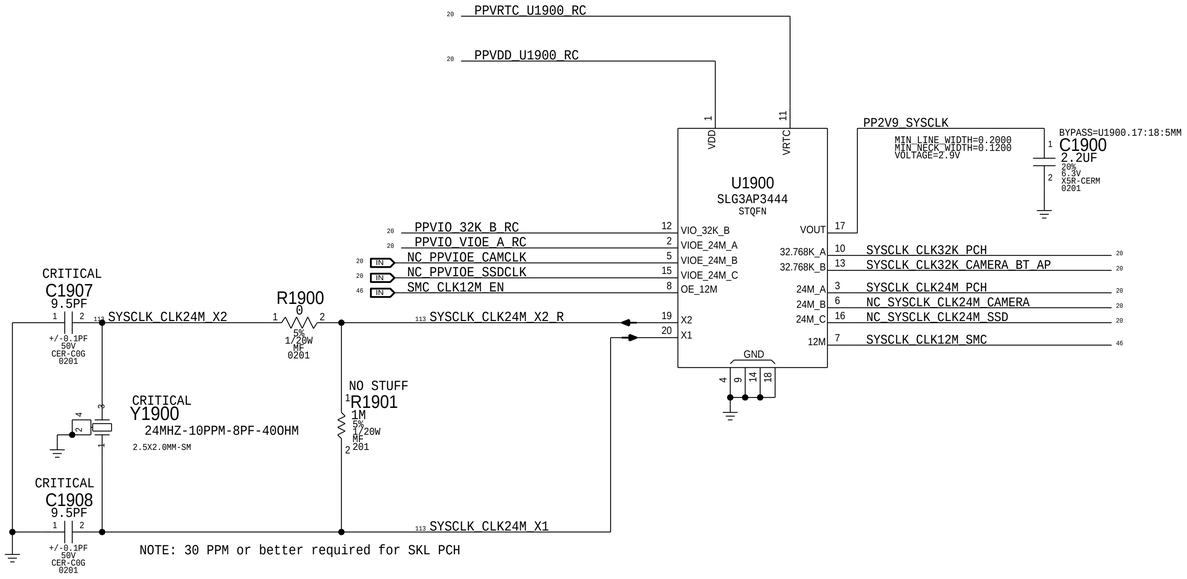
PAGE TITLE: CPU/PCH Merged XDP

Apple Inc.

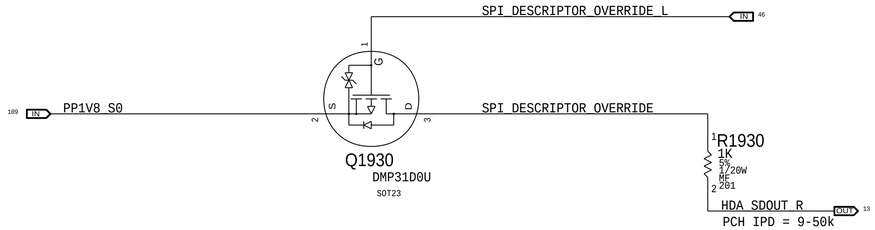
DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 18 OF 145
SHEET: 18 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

System 32kHz / 12MHz / 24MHz Clock Generator

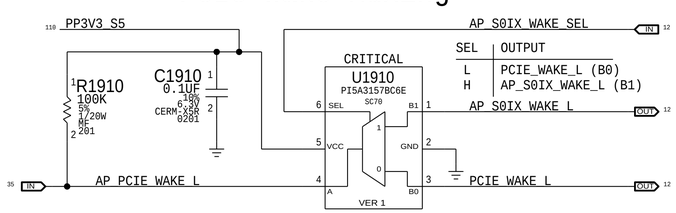


PCH ME Disable Strap



PCH uses HDA_SDO as a power-up strap. If low, ME functions normally.
If high, ME is disabled. This allows for full re-flashing of SPI ROM.
SMC controls strap enable to allow in-field control of strap setting.
***** Circuit does not support HDA voltage >3.3V.

PCIe Wake Muxing



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE
Chipset Support 1

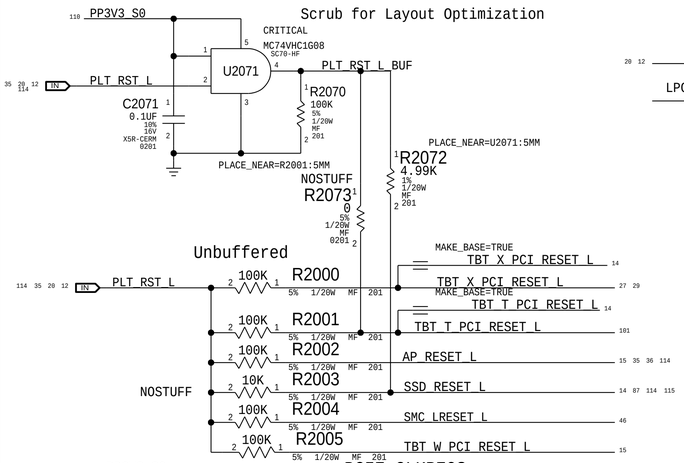
Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 19 OF 145
SHEET 19 OF 121

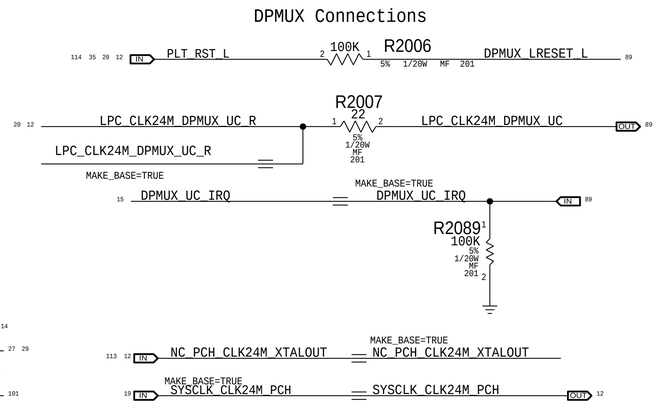
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Platform Reset Connections

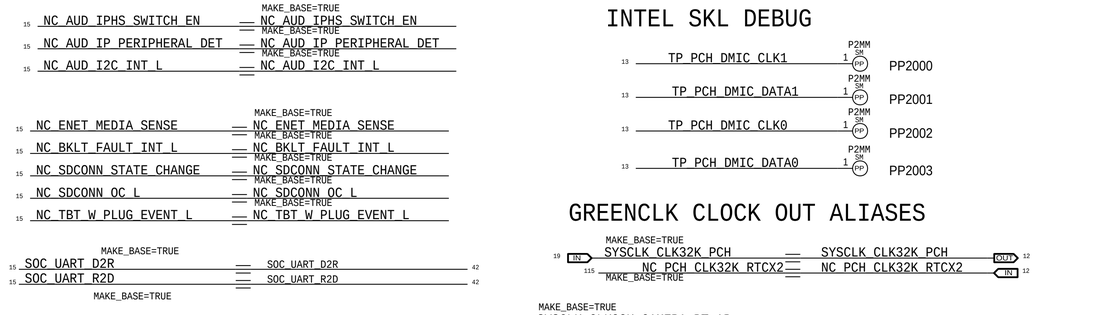
Buffered



DPMUX Connections



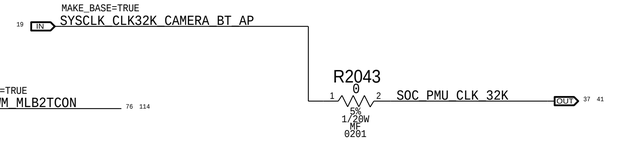
NC ALIASES 3



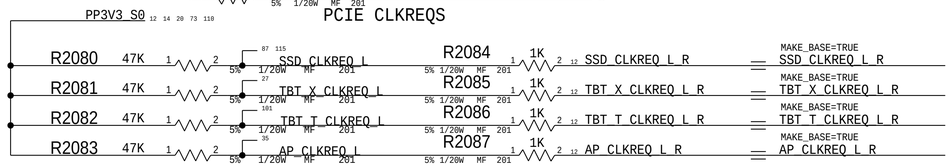
INTEL SKL DEBUG

GREENCLK CLOCK OUT ALIASES

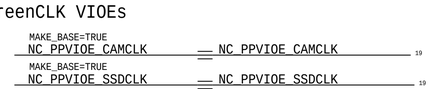
SIGNAL ALIASES



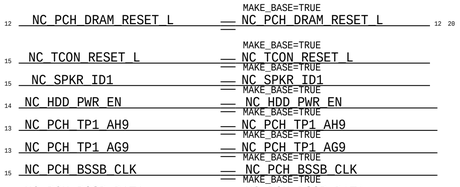
PCIE CLKREQS



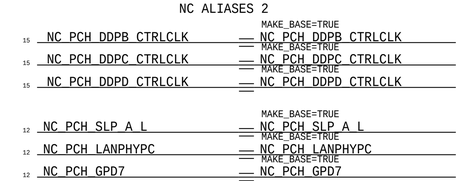
GreenCLK VIOEs

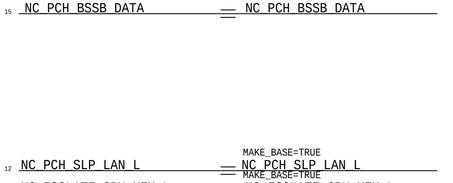


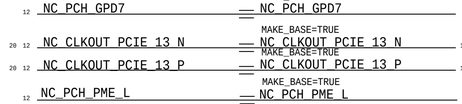
NC ALIASES

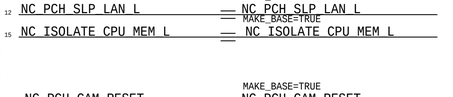


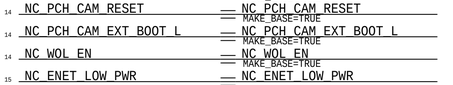
NC ALIASES 2

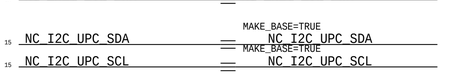


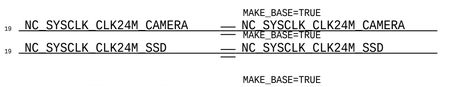


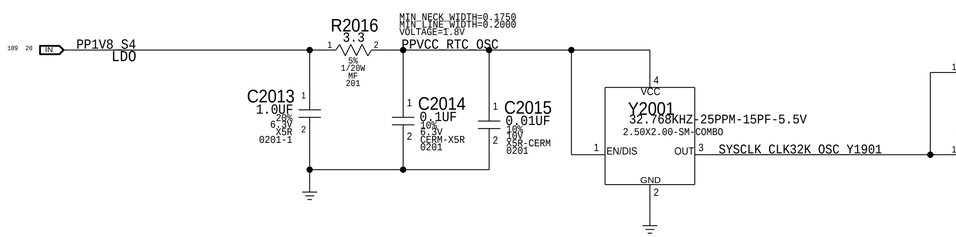




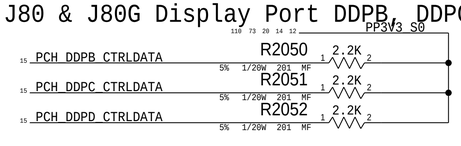


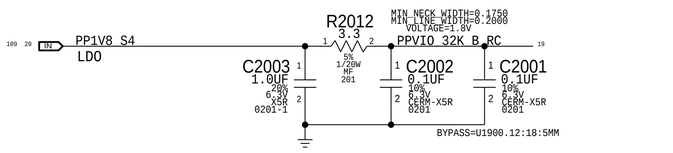






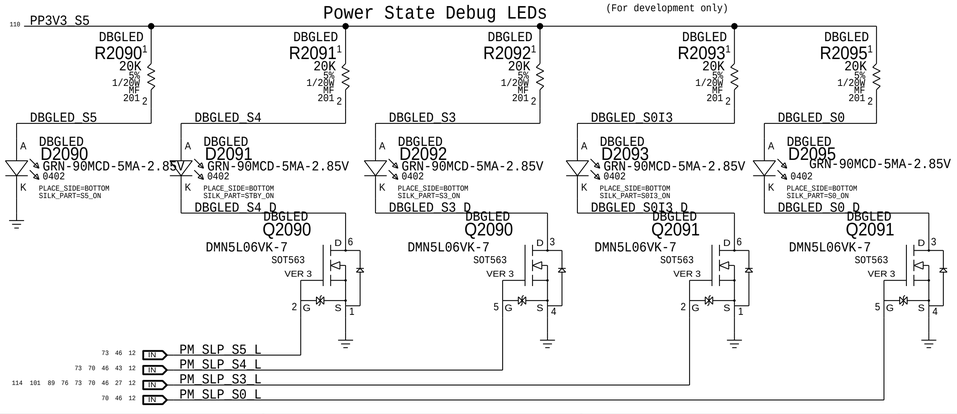
J80 & J80G Display Port DDPB, DDPC,DDPD

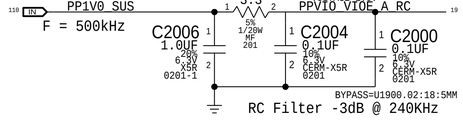


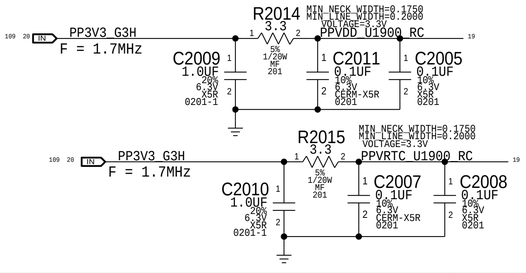


Power State Debug LEDs

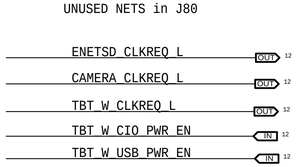
(For development only)







UNUSED NETS in J80



BOM_COST_GROUP=CPU & CHIPSET

PAGE TITLE: Chipset Support 2

Apple Inc.

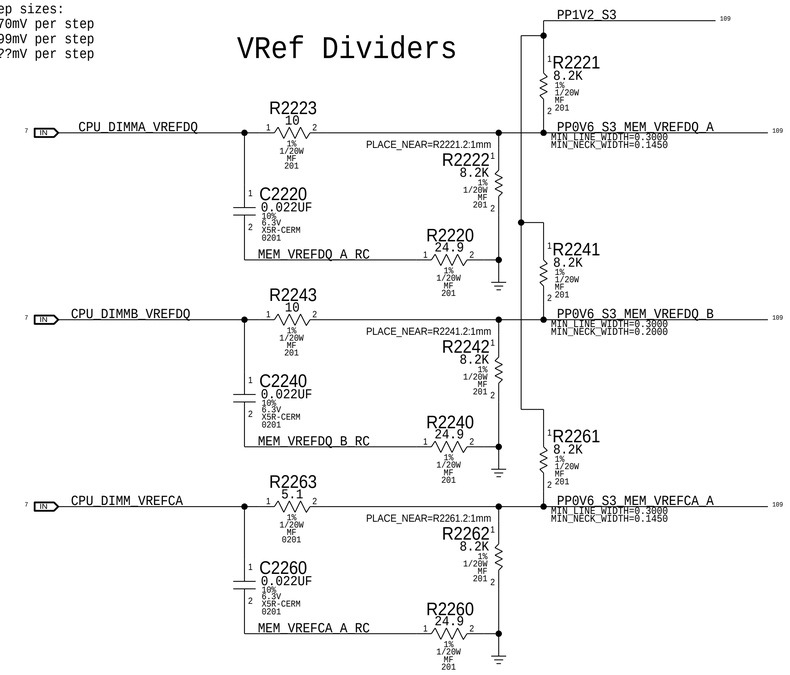
DRAWING NUMBER: 051-00647 | SIZE: D | REVISION: 10.0.0 | BRANCH: dvt-fab10 | PAGE: 20 OF 145 | SHEET: 20 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

CPU-Based Margining

NOTE: CPU DAC output step sizes:
DDR3 (1.5V) 7.70mV per step
DDR3L (1.35V) 6.99mV per step
LPDDR3 (1.2V) ?.??mV per step

VRef Dividers



BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

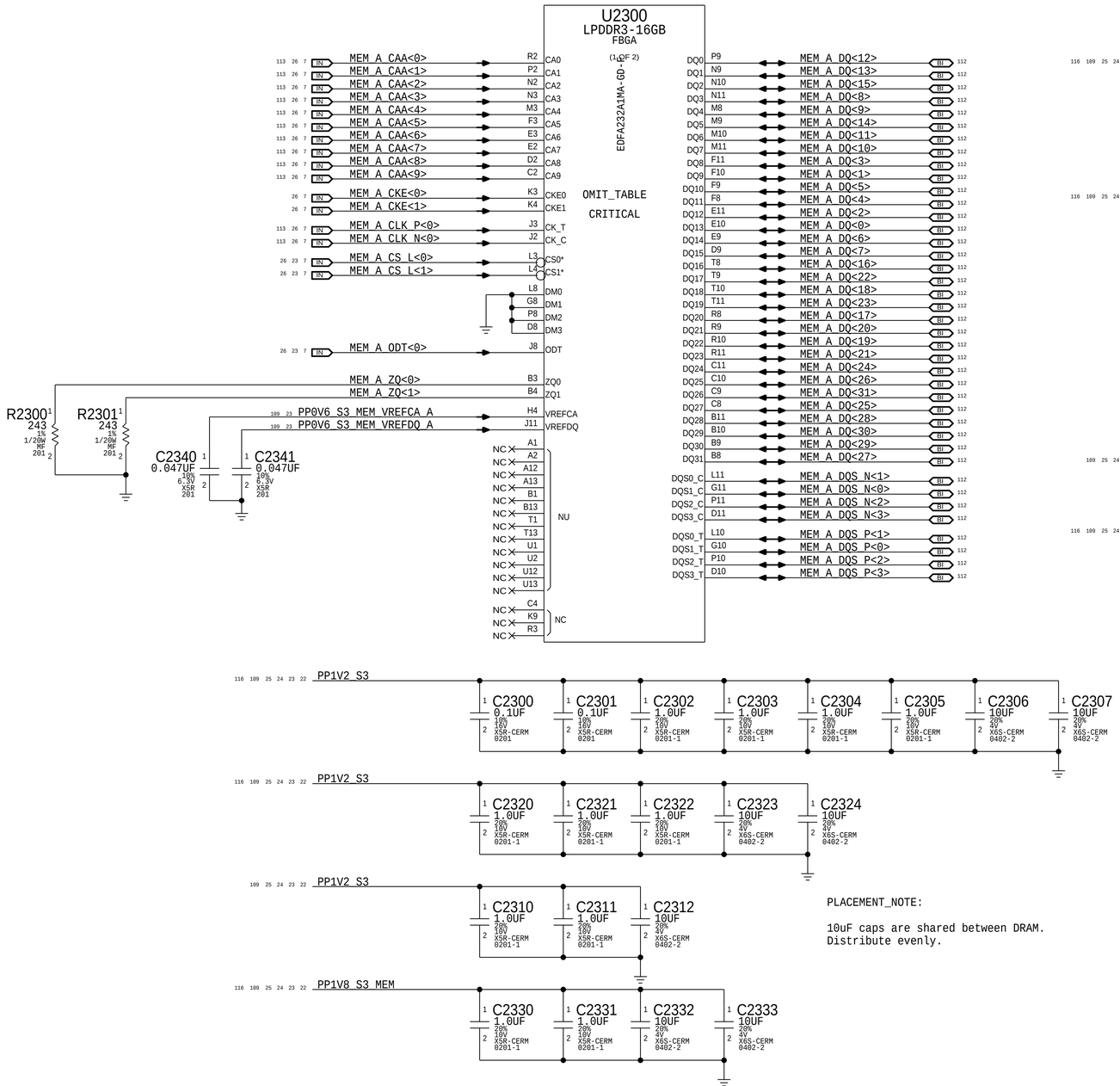
PAGE TITLE: LPDDR3 VREF MARGINING

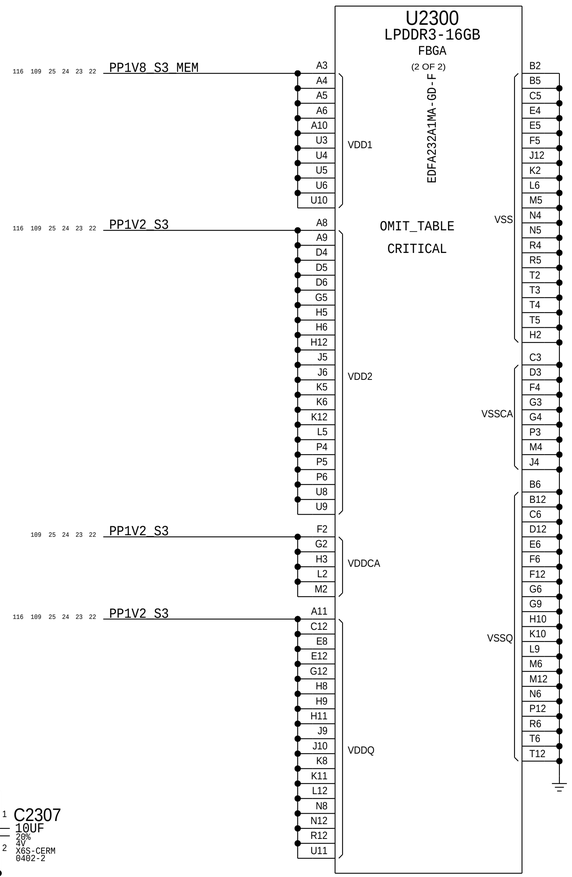
Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 22 OF 145
SHEET: 21 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

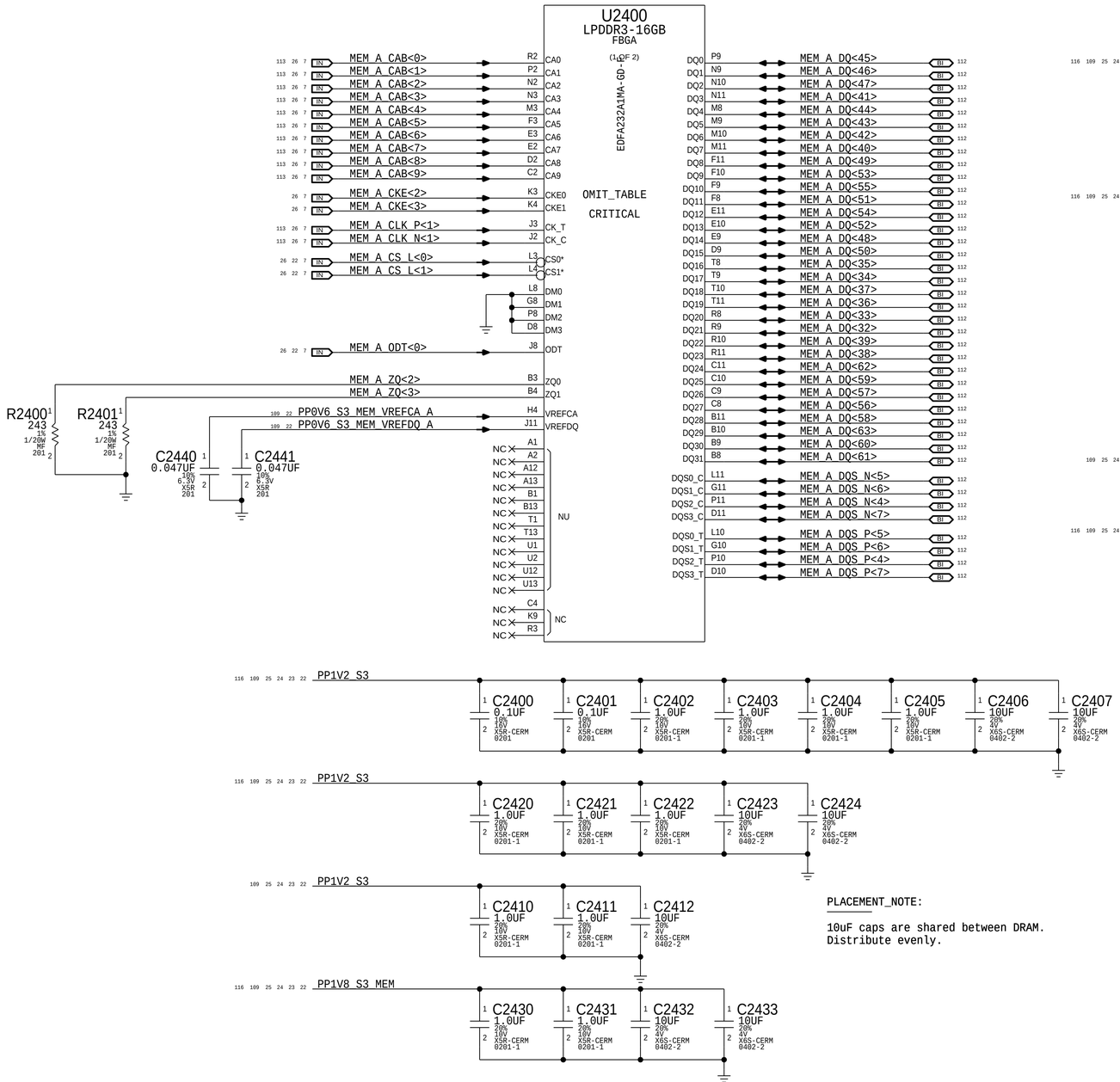
BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	LPDDR3 DRAM Channel A (0-31)
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 23 OF 145
	SHEET 22 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL A (32-63)



PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel A (32-63)

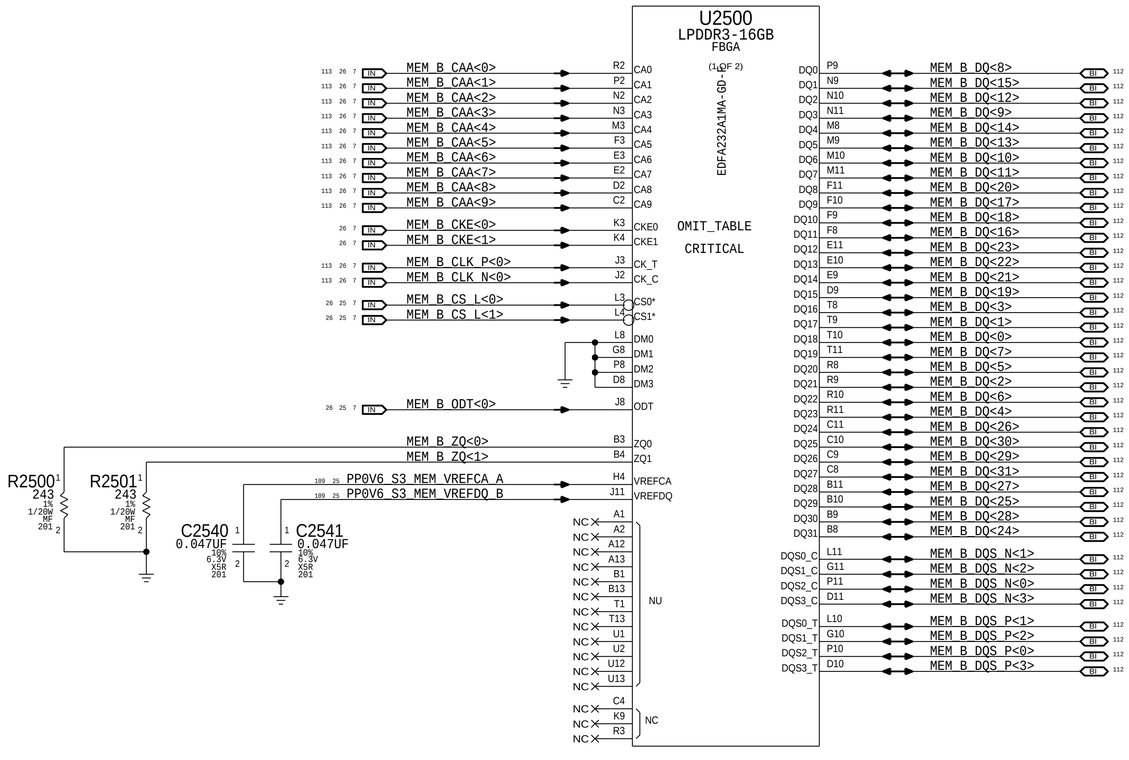
Apple Inc.

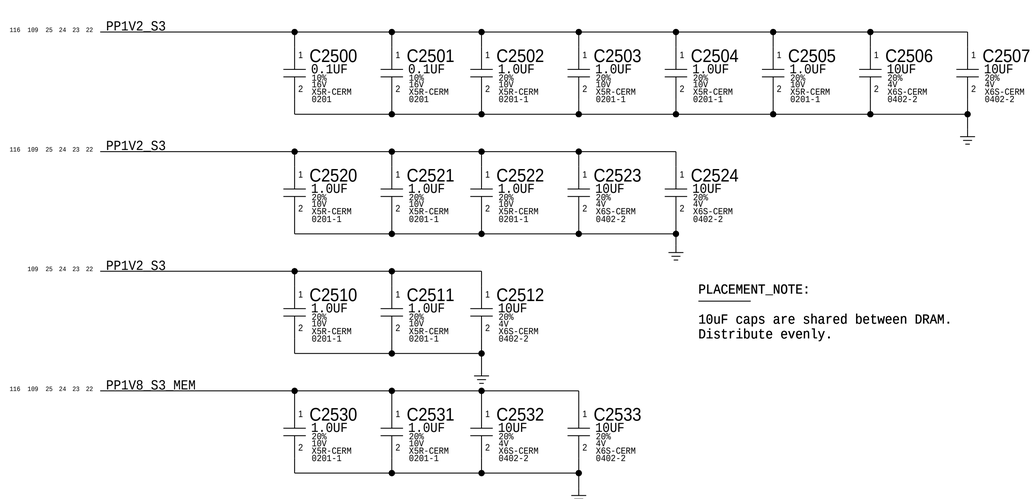
DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 24 OF 145
SHEET: 23 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (0-31)





PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel B (0-31)

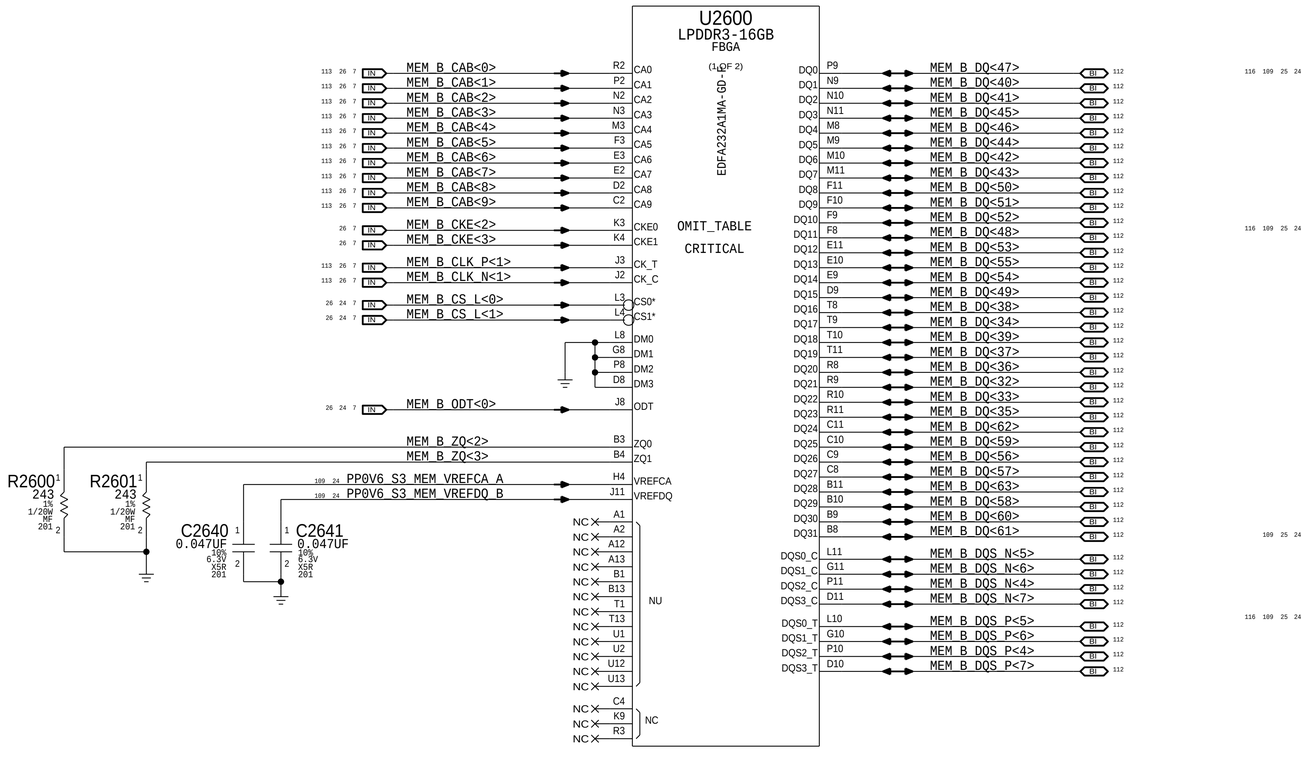
Apple Inc.

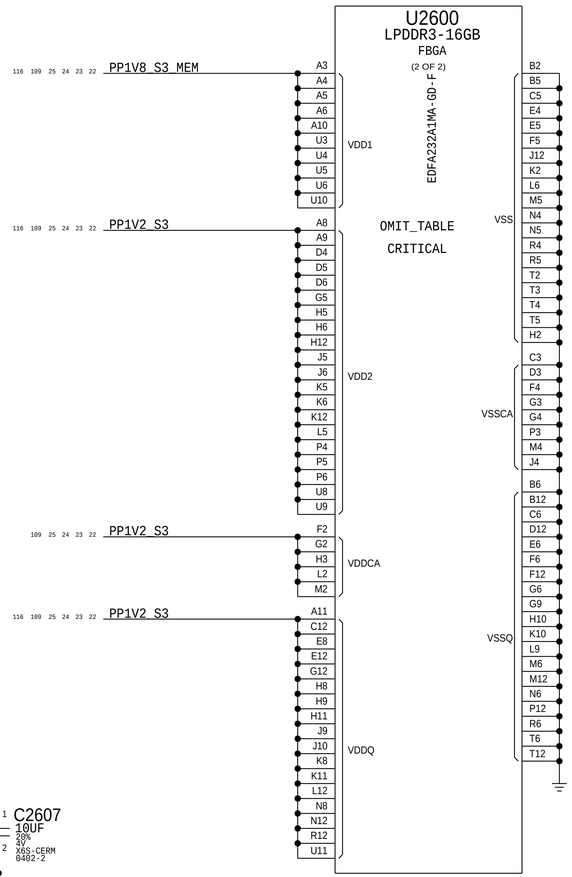
DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 25 OF 145
SHEET: 24 OF 121

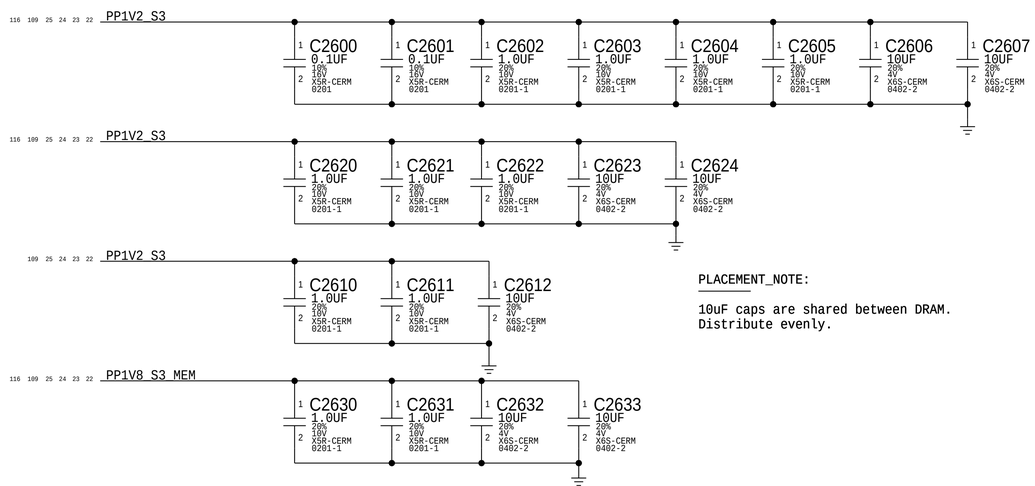
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 CHANNEL B (32-63)







PLACEMENT_NOTE:

10uF caps are shared between DRAM.
Distribute evenly.

BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: LPDDR3 DRAM Channel B (32-63)

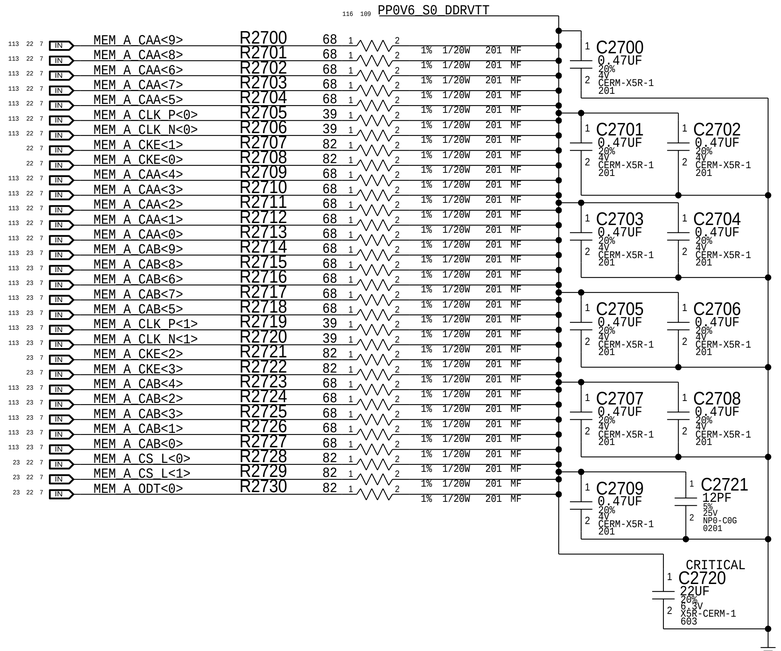
Apple Inc.

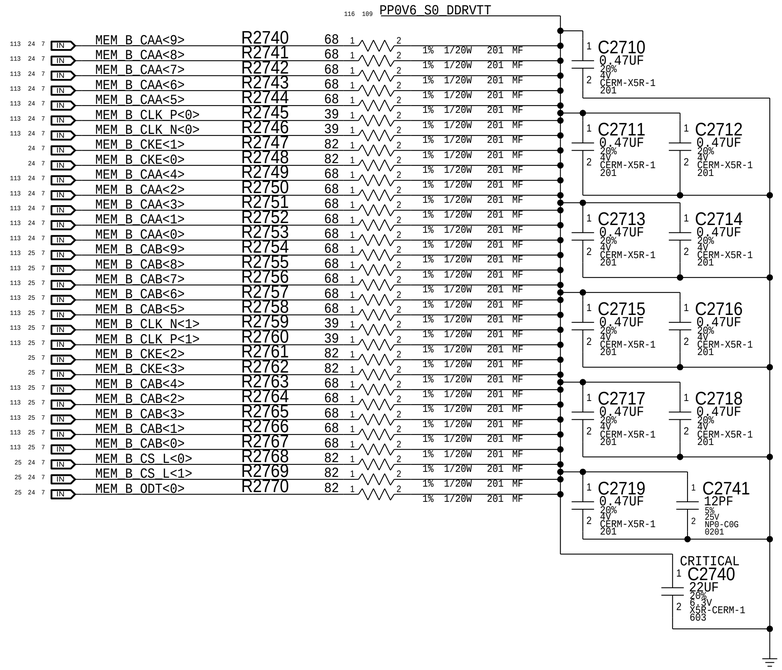
DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 26 OF 145
SHEET: 25 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Intel recommends 68 Ohm for CMD/ADDR, 80 Ohm for CTRL/CKE, 38 Ohm for CLK





BOM_COST_GROUP=DRAM

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

LPDDR3 DRAM Termination

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

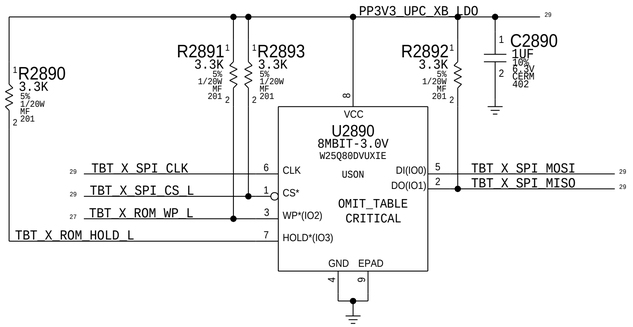
BRANCH dvt-fab10

PAGE 27 OF 145

SHEET 26 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



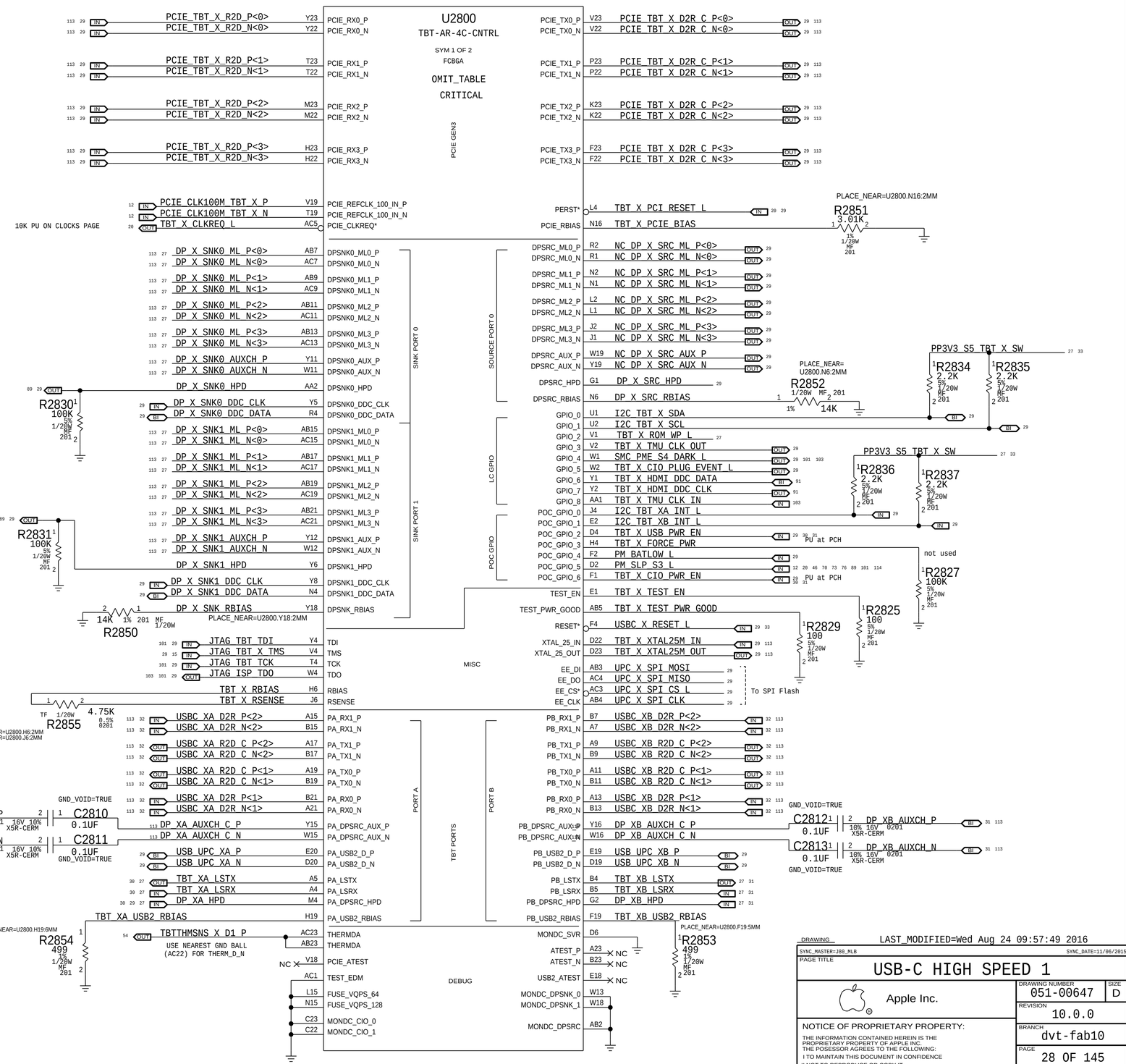
SNK0 AC Coupling

DP_X_SNK0_ML_C_P<0>	C2820	0.1UF	DP_X_SNK0_ML_P<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<0>	C2821	0.1UF	DP_X_SNK0_ML_N<0>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<1>	C2822	0.1UF	DP_X_SNK0_ML_P<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<1>	C2823	0.1UF	DP_X_SNK0_ML_N<1>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<2>	C2824	0.1UF	DP_X_SNK0_ML_P<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<2>	C2825	0.1UF	DP_X_SNK0_ML_N<2>	GND_VOID=TRUE
DP_X_SNK0_ML_C_P<3>	C2826	0.1UF	DP_X_SNK0_ML_P<3>	GND_VOID=TRUE
DP_X_SNK0_ML_C_N<3>	C2827	0.1UF	DP_X_SNK0_ML_N<3>	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_P	C2828	0.1UF	DP_X_SNK0_AUXCH_P	GND_VOID=TRUE
DP_X_SNK0_AUXCH_C_N	C2829	0.1UF	DP_X_SNK0_AUXCH_N	

SNK1 AC Coupling

DP_X_SNK1_ML_C_P<0>	C2830	0.1UF	DP_X_SNK1_ML_P<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<0>	C2831	0.1UF	DP_X_SNK1_ML_N<0>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<1>	C2832	0.1UF	DP_X_SNK1_ML_P<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<1>	C2833	0.1UF	DP_X_SNK1_ML_N<1>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<2>	C2834	0.1UF	DP_X_SNK1_ML_P<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<2>	C2835	0.1UF	DP_X_SNK1_ML_N<2>	GND_VOID=TRUE
DP_X_SNK1_ML_C_P<3>	C2836	0.1UF	DP_X_SNK1_ML_P<3>	GND_VOID=TRUE
DP_X_SNK1_ML_C_N<3>	C2837	0.1UF	DP_X_SNK1_ML_N<3>	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_P	C2838	0.1UF	DP_X_SNK1_AUXCH_P	GND_VOID=TRUE
DP_X_SNK1_AUXCH_C_N	C2839	0.1UF	DP_X_SNK1_AUXCH_N	

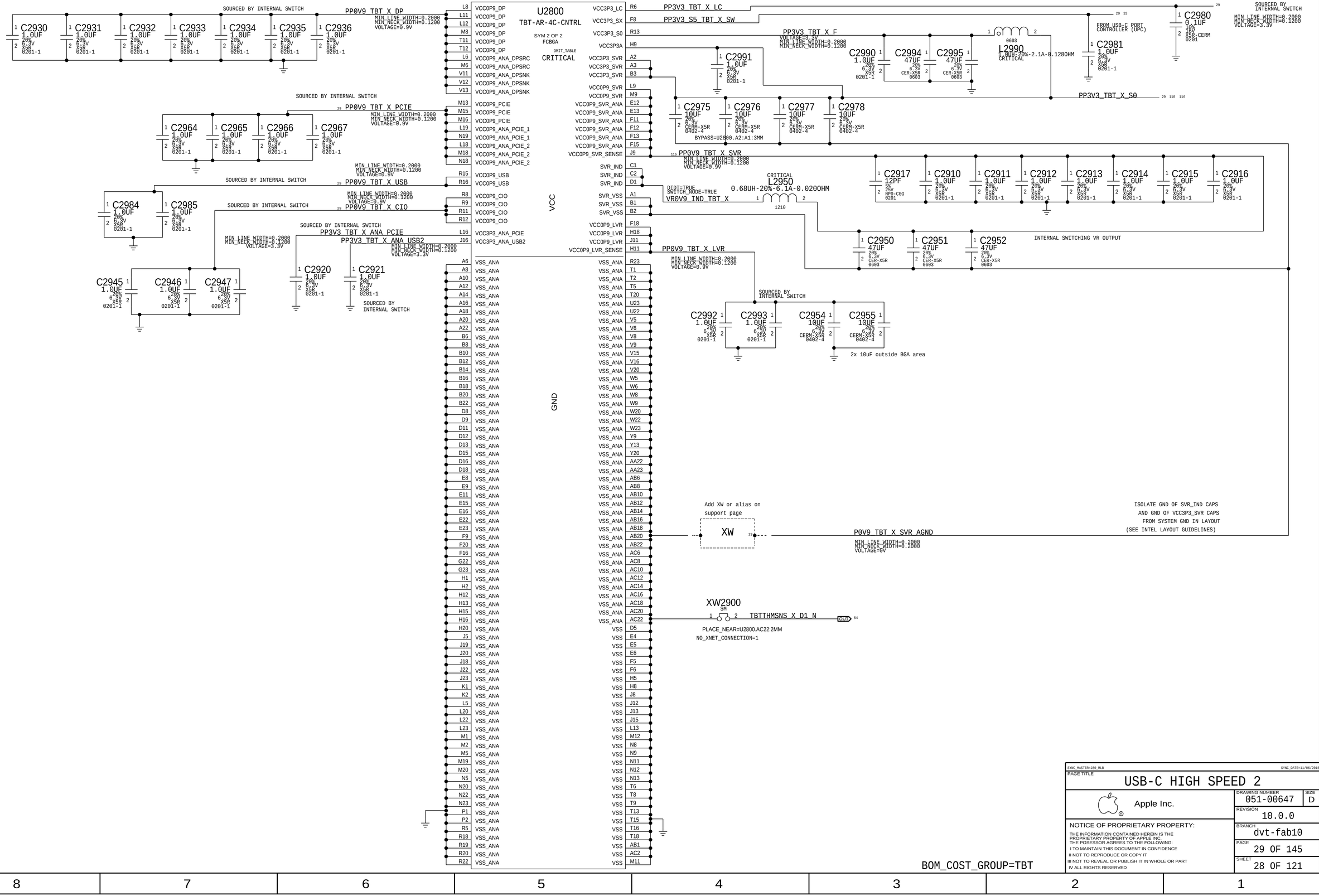
100K	R2862	DP_XA_HPD
100K	R2872	DP_XB_HPD
1M	R2860	TBT_XA_LSTX
1M	R2861	TBT_XA_LSRX
1M	R2870	TBT_XB_LSTX
1M	R2871	TBT_XB_LSRX



BOM_COST_GROUP=TBT

DRAWING	LAST_MODIFIED=Wed Aug 24 09:57:49 2016
SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	USB-C HIGH SPEED 1
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 28 OF 145
	SHEET 27 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

USB-C HIGH SPEED 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 29 OF 145

SHEET 28 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

TMU CLKs

TBT_X_TMU_CLK_OUT → R3025 15 (5% 1/20W MF 201, PLACE_NEAR=U2800.V2:5mm) → TBT_T_TMU_CLK_IN (MAKE_BASE=TRUE)
TBT_X_TMU_CLK_OUT (MAKE_BASE=TRUE)
R3026 100K (5% 1/20W MF 201)

USBC 5V EN PD

UPC_X_5V_EN → R3032 100K (5% 1/20W MF 201)

ACE/SMC I2C PU

PP3V3_G3H
R3038 10K (5% 1/20W MF 201) → SMC_USBC_INT_L

DP SRC OPTIONS

IF DP SRC NOT USED

DP_X_SRC_HPD → R3040 1M (5% 1/20W MF 201)

NC_DP_X_SRC_ML_P<3..0>	NC_DP_X_SRC_ML_P<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_ML_N<3..0>	NC_DP_X_SRC_ML_N<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_X_SRC_AUX_P	NC_DP_X_SRC_AUX_P	MAKE_BASE=TRUE
NC_DP_X_SRC_AUX_N	NC_DP_X_SRC_AUX_N	MAKE_BASE=TRUE

FUSES FOR UPC

PLACE_NEAR=Q3100:5MM
F3000 (CRITICAL, 0603) 6AMP-32V-0.00950HM
PP20V_USBC_XA_VBUS → PP20V_USBC_XA_VBUS_F
PLACE_NEAR=Q3200:5MM
F3001 (CRITICAL, 0603, 740S0135) 6AMP-32V-0.00950HM
PP20V_USBC_XB_VBUS → PP20V_USBC_XB_VBUS_F

25MHz xtal

TBT_X_XTAL25M_OUT → R3007 0 (5% 1/20W MF 201) → TBT_X_XTAL25M_OUT_R
NOSTUFF R3006 1M (5% 1/20W MF 201)
to/from Ridge
Y3000 (CRITICAL) 25MHZ-25PPM-20PF-500HM 2.00X1.60-SM
C3002 20PF (5% 25V C0G 0201)
C3003 20PF (5% 25V C0G 0201)
TBT_X_XTAL25M_IN

AR/ACE SPI BUS SERIES R'S

TBT_X_SPI_CLK	R3094 100	TBT_X_SPI_CLK_DBG	
TBT_X_SPI_CS_L	R3095 15	UPC_XB_SPI_CS_L	Ace
TBT_X_SPI_MOSI	R3096 15	UPC_XB_SPI_MOSI	Ace
TBT_X_SPI_MISO	R3097 15	UPC_XB_SPI_MISO	Ace
	R3098 15	UPC_X_SPI_CLK	AR
ROM	R3090 15	UPC_X_SPI_CS_L	AR
	R3091 15	UPC_X_SPI_MOSI	AR
	R3092 15	UPC_X_SPI_MISO	AR
	R3093 15	PP3V3_TBT_X_S0	

(5% 1/20W MF 201)

USBC DEBUG CONN

TP3001 TP_P5 TP_UPC_XA_SWD_DATA
TP3002 TP_P5 TP_UPC_XA_SWD_CLK
TP3003 TP_P5 TP_UPC_XB_SWD_DATA
TP3004 TP_P5 TP_UPC_XB_SWD_CLK

RIDGE JTAG ISOLATION

PLACE_NEAR=U1100.AJ29:10mm
JTAG_TBT_TCK → R3043 0 → JTAG_ISP_TCK
JTAG_TBT_TDI → R3044 0 → JTAG_ISP_TDI
PLACE_NEAR=U1100.AK28:10mm

POWER ALIASES

PP3V3_UPC_XB_LDO	PP3V3_UPC_XB_LDO	
PP3V3_UPC_XB_LDO		
PP3V3_UPC_XA_LDO	PP3V3_UPC_XA_LDO	
PP3V3_UPC_XA_LDO		
PP20V_USBC_XA_VBUS	PP20V_USBC_XA_VBUS	
PP20V_USBC_XB_VBUS	PP20V_USBC_XB_VBUS	MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=20V
PPDCIN_G3H	PPDCIN_G3H	MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=5V
PP5V_S4_X_USBC	PP5V_S4_X_USBC	
PP5V_S4_X_USBC		
PP5V_S4_X_USBC		MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V
PP3V3_TBT_X_S0	PP3V3_TBT_X_S0	

OMIT

R3089 ACE Debug Support

NOSTUFF R3089 (NONE NONE NONE 402)
UPC_XA_DBG_UART_TX → UPC_XA_DBG_UART_RX
NOSTUFF R3088 (NONE NONE NONE 402) OMIT
TP_UPC_XB_DBG_UART_TX → TP_UPC_XB_DBG_UART_RX

Ridge PDs

DP_X_SNK0_DDC_CLK	R3067 100K	DP_X_SNK0_DDC_CLK
DP_X_SNK0_DDC_DATA	R3068 100K	DP_X_SNK0_DDC_DATA
DP_X_SNK1_DDC_CLK	R3069 100K	DP_X_SNK1_DDC_CLK
DP_X_SNK1_DDC_DATA	R3070 100K	DP_X_SNK1_DDC_DATA

(MAKE_BASE=TRUE, 5% 1/20W MF 201)

ACE DEBUG CONN

Place on bottom
USBC_DBG J3000 505070-1220 M-ST-SM

I2C_TBT_XB_INT_L	1	2	I2C_TBT_XA_INT_L
I2C_UPC_X_SCL2	3	4	I2C_TBT_X_SDA
I2C_UPC_X_SDA2	5	6	I2C_TBT_X_SCL
SMC_USBC_INT_L	7	8	I2C_UPC_XA_DBG_CTL_SDA
TBT_X_SPI_CLK_DBG	9	10	I2C_UPC_XA_DBG_CTL_SCL
UPC_XA_UART_TX	11	12	UPC_XA_UART_RX

ACE A RPD STRAPPING

USBC_XA_CC1 → USBC_XA_CC1 (MAKE_BASE=TRUE)
USBC_XA_CC2 → USBC_XA_CC2 (MAKE_BASE=TRUE)

NC ALIASES / NO TEST

IN NC_UPC_XB_I2C_ADDR

GND ALIASES

GND (MAKE_BASE=TRUE)

RIDGE DEBUG CONN

Place on bottom
USBC_DBG J3001 505070-1220 M-ST-SM

TBT_X_CIO_PLUG_EVENT_L	1	2	TBT_X_PCI_RESET_L
DP_X_SNK0_HPD	3	4	USBC_X_RESET_L
DP_X_SNK1_HPD	5	6	PP3V3_S5_TBT_X_SW
DP_XA_HPD	7	8	PP0V9_TBT_X_PCIE
TBT_POC_RESET	9	10	PP0V9_TBT_X_USB
PP3V3_TBT_X_LC	11	12	PP0V9_TBT_X_CIO

ACE B RPD STRAPPING

USBC_XB_CC1 → USBC_XB_CC1 (MAKE_BASE=TRUE)
USBC_XB_CC2 → USBC_XB_CC2 (MAKE_BASE=TRUE)

ACE PDs

UPC_XA_HPD_RX → R3033 100K (NO STUFF, 5% 1/20W MF 201)
UPC_XB_HPD_RX → R3034 100K (NO STUFF, 5% 1/20W MF 201)
UPC_XA_HPD_RX → R3035 0 (5% 1/20W MF 201)
UPC_XB_HPD_RX → R3036 0 (5% 1/20W MF 201) → SMC_RESET_L
USB_UPC_XA_P → R3081 0 (NOSTUFF, 5% 1/20W MF 0201) → R3084 0 (5% 1/20W MF 0201, NOSTUFF) → USB_UPC_XB_P
USB_UPC_XA_N → R3082 0 (NOSTUFF, 5% 1/20W MF 0201) → R3085 0 (5% 1/20W MF 0201, NOSTUFF) → USB_UPC_XB_N

SIGNAL ALIASES

UPC_X_5V_EN	UPC_X_5V_EN	MAKE_BASE=TRUE
UPC_X_5V_EN		
USB2_UPC_XB_P	R3086 0 (5% 1/20W MF 0201)	USB_UPC_PCH_XB_P
USB2_UPC_XB_P		
USB2_UPC_XB_N	R3087 0 (5% 1/20W MF 0201)	USB_UPC_PCH_XB_N
USB2_UPC_XB_N		
TBT_X_CIO_PWR_EN		TBT_X_CIO_PWR_EN
TBT_X_USB_PWR_EN		TBT_X_USB_PWR_EN
PM_BATLOW_L		PM_BATLOW_L
SMC_PME_S4_DARK_L		SMC_PME_S4_DARK_L
SMC_PME_S4_DARK_L		

UPC_X_SPI_CLK		UPC_X_SPI_CLK
UPC_X_SPI_CS_L		UPC_X_SPI_CS_L
UPC_X_SPI_MOSI		UPC_X_SPI_MOSI
UPC_X_SPI_MISO		UPC_X_SPI_MISO
UPC_T_SPI_CLK		UPC_T_SPI_CLK
UPC_T_SPI_CS_L		UPC_T_SPI_CS_L
UPC_T_SPI_MOSI		UPC_T_SPI_MOSI
UPC_T_SPI_MISO		UPC_T_SPI_MISO
JTAG_ISP_TDO		JTAG_ISP_TDO
SMC_USBC_INT_L		SMC_USBC_INT_L
SMC_USBC_INT_L		
TBT_POC_RESET		TBT_POC_RESET
TBT_X_CIO_PLUG_EVENT_L		TBT_X_CIO_PLUG_EVENT_L

(MAKE_BASE=TRUE)

UPC_XA_FAULT_L → R3078 0 → XDP_PCH_OBSDATA_C0
UPC_XB_FAULT_L → R3079 0 (5% 1/20W MF 0201) → XDP_PCH_OBSDATA_C1

JTAG_TBT_X_TMS		JTAG_TBT_X_TMS
JTAG_TBT_T_TMS		JTAG_TBT_T_TMS
PP3V3_S4		PP3V3_S4
PP3V3_S4		

SMC MOJO

SMC_DEBUGPRT_TX_L		SMC_DEBUGPRT_TX_L
SMC_DEBUGPRT_RX_L		SMC_DEBUGPRT_RX_L

(MAKE_BASE=TRUE)

TP_USBC_XA_RESET_L → TP_USBC_XA_RESET_L (MAKE_BASE=TRUE)

DCI
PCH USB3

USB3_EXTA_D2R_P		USB3_EXTA_D2R_P
USB3_EXTA_D2R_N		USB3_EXTA_D2R_N

USB3_EXTA_R2D_C_P → C3020 0.1UF (X5R-CERM 16V 10% 0201) → USB3_EXTA_R2D_P
USB3_EXTA_R2D_C_N → C3021 0.1UF (X5R-CERM 16V 10% 0201) → USB3_EXTA_R2D_N

USB2_UPC_XA_P → R3076 0 (5% 1/20W MF 0201) → USB_UPC_PCH_XA_P
USB2_UPC_XA_N → R3077 0 (5% 1/20W MF 0201) → USB_UPC_PCH_XA_N

I2C SERIES R'S

I2C_UPC_X_SDA2 → R3041 33 (5% 1/20W MF 201) → SMBUS_SMC_4_G3H_SDA
I2C_UPC_X_SCL2 → R3042 33 (5% 1/20W MF 201) → SMBUS_SMC_4_G3H_SCL
PLACE_NEAR=U5000:5mm

RIDGE 0.9V SVR XW

P0V9_TBT_X_SVR_AGND → XW3000 SM
NO_XNET_CONNECTION=1

TBT to ACE

TBT
Alpine Ridge U2800
(MASTER)

I2C_TBT_X_SCL	I2C_TBT_X_SCL
I2C_TBT_X_SDA	I2C_TBT_X_SDA
I2C_TBT_XA_INT_L	I2C_TBT_XA_INT_L
I2C_TBT_XB_INT_L	I2C_TBT_XB_INT_L

Pri ACE
U3100
(Write: 0x70 Read: 0x71)

Sec ACE
U3200
(Write: 0x7E Read: 0x7F)

Ridge PCIE Caps

PCIE_TBT_X_R2D_C_P<0>	C3040 0.22UF	PCIE_TBT_X_R2D_P<0>
PCIE_TBT_X_R2D_C_N<0>	C3041 0.22UF	PCIE_TBT_X_R2D_N<0>
PCIE_TBT_X_R2D_C_P<1>	C3042 0.22UF	PCIE_TBT_X_R2D_P<1>
PCIE_TBT_X_R2D_C_N<1>	C3043 0.22UF	PCIE_TBT_X_R2D_N<1>
PCIE_TBT_X_R2D_C_P<2>	C3044 0.22UF	PCIE_TBT_X_R2D_P<2>
PCIE_TBT_X_R2D_C_N<2>	C3045 0.22UF	PCIE_TBT_X_R2D_N<2>
PCIE_TBT_X_R2D_C_P<3>	C3046 0.22UF	PCIE_TBT_X_R2D_P<3>
PCIE_TBT_X_R2D_C_N<3>	C3047 0.22UF	PCIE_TBT_X_R2D_N<3>
PCIE_TBT_X_D2R_C_P<0>	C3050 0.22UF	PCIE_TBT_X_D2R_P<0>
PCIE_TBT_X_D2R_C_N<0>	C3051 0.22UF	PCIE_TBT_X_D2R_N<0>
PCIE_TBT_X_D2R_C_P<1>	C3052 0.22UF	PCIE_TBT_X_D2R_P<1>
PCIE_TBT_X_D2R_C_N<1>	C3053 0.22UF	PCIE_TBT_X_D2R_N<1>
PCIE_TBT_X_D2R_C_P<2>	C3054 0.22UF	PCIE_TBT_X_D2R_P<2>
PCIE_TBT_X_D2R_C_N<2>	C3055 0.22UF	PCIE_TBT_X_D2R_N<2>
PCIE_TBT_X_D2R_C_P<3>	C3056 0.22UF	PCIE_TBT_X_D2R_P<3>
PCIE_TBT_X_D2R_C_N<3>	C3057 0.22UF	PCIE_TBT_X_D2R_N<3>

(GND_VOID=TRUE, 0201 X5R 6.3V 20%)

BOM_COST_GROUP=TBT

PAGE TITLE: USB-C Support

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	30 OF 145
SHEET	29 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

CRITICAL
Q3100
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

29 PP20V_USBC_XA_VBUS_F
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=20V

29 PP20V_USBC_XA_VBUS
C3101 1UF 10% 35V X5R 0402

PPDCIN_G3H 29 31 103 104 105
MAX 100uF TOTAL ON RAIL

UPC_XA_GATE1
TP_Q3100_DRAIN
UPC_XA_GATE2

29 PP3V3_UPC_XA_LDO
109 PP3V3_G3H
105 104 103 31 29 GND
CAP FOR PP_5V0 ON VR PAGE
29 PP5V_S4_X_USBC
C3100 10UF 20% 6.3V CERM-X5R 0402-1

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=3.3V
PP3V3_UPC_XA_LDO 29

P3V3_TBT_X_SX_EN_R 33

PP1V8_UPC_XA_LDOA
PP1V8_UPC_XA_LDOD
PP1V1_UPC_XA_LDO_BMC
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.1V

C3104 2.2UF 20% 6.3V X5R-CERM 0201
C3105 1.0UF 20% 6.3V X5R 0201-1
C3106 0.47UF 10% 6.3V CERM-X5R 0201
C3108 10UF 20% 6.3V CERM-X5R 0402-1
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
VOLTAGE=1.8V

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

PP3V3_UPC_XA_LDO 29
R3109 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SCL 29 30
R3108 1M 5% 1/20W MF 201 — I2C_UPC_XA_DBG_CTL_SDA 29 30

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

31 29 IN	TBT_POC_RESET	E11	MRESET	PRIMARY ONLY
29 OUT	TP_USBC_XA_RESET_L	F11	RESET*	PRIMARY ONLY
29 114	UPC_XA_DBG_UART_TX	B2	GPIO0	
29 114	UPC_XA_DBG_UART_RX	C2	GPIO1	
31 29 27 IN	TBT_X_CIO_PWR_EN	D10	GPIO2	
31 29 27 IN	TBT_X_USB_PWR_EN	G11	GPIO3	
29 27 OUT	DP_XA_HPD	C10	GPIO4	
29	UPC_XA_HPD_RX	E10	GPIO5	
29 OUT	UPC_X_5V_EN	G10	GPIO6	
105 104 103 31 29 OUT	SMC_PME_S4_DARK_L	D7	GPIO7	
29 OUT	UPC_XA_FAULT_L	H6	GPIO8	
29 IN	GND	F10	BUSPOWERZ	
GND I2C ADDR PRIMARY ONLY	GND	F1	I2C_ADDR	
	UPC_XA_R_OSC	G2	R_OSC	
30 29	I2C_UPC_XA_DBG_CTL_SCL	E4	DEBUG_CTL1	
30 29	I2C_UPC_XA_DBG_CTL_SDA	D5	DEBUG_CTL2	
29 BI	I2C_TBT_X_SDA	D1	I2C_SDA1	
29 BI	I2C_TBT_X_SCL	D2	I2C_SCL1	
29 OUT	I2C_TBT_XA_INT_L	C1	I2C_IRQ1*	
29 BI	I2C_UPC_X_SDA2	A5	I2C_SDA2	
29 BI	I2C_UPC_X_SCL2	B5	I2C_SCL2	
29 OUT	SMC_USBC_INT_L	B6	I2C_IRQ2*	
29 OUT	GND	A3	SPI_CLK	
29 OUT	GND	B4	SPI_MOSI	
29 IN	GND	A4	SPI_MISO	
29 OUT	GND	B3	SPI_SSZ	
29	TP_UPC_XA_SWD_DATA	F4	SWD_DATA	
29	TP_UPC_XA_SWD_CLK	G4	SWD_CLK	
31 30 29 IN	UPC_XA_UART_RX	F2	UART_RX	
31 29 OUT	UPC_XA_UART_TX	E2	UART_TX	
27 IN	TBT_XA_LSTX	L4	LSX_R2P	
27 OUT	TBT_XA_LSRX	K4	LSX_P2R	
	USB_UPC_XA_F_P	L5	USB_RP_P	
	USB_UPC_XA_F_N	K5	USB_RP_N	
	DP_XA_AUXCH_P	J1	AUX_P	
	DP_XA_AUXCH_N	J2	AUX_N	
29 BI	USB3_EXTA_D2R_P	L2	DEBUG1	
29 BI	USB3_EXTA_D2R_N	K2	DEBUG2	
29 BI	USB3_EXTA_R2D_P	L3	DEBUG3	
29 BI	USB3_EXTA_R2D_N	K3	DEBUG4	

U3100
CD3215A
BGA
CRITICAL
OMIT_TABLE

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

A11	PP_5V0	
B11	PP_5V0	
C11	PP_5V0	
D11	PP_5V0	
A6	PP_HV	
A7	PP_HV	
A8	PP_HV	
B7	PP_HV	
H10	PP_CABLE	
H11	VBUS	
J10	VBUS	
J11	VBUS	
K11	VBUS	
H1	VIN_3V3	
B1	VDDIO	
G1	LDO_3V3	
H2	VOUT_3V3	
K1	LDO_1V8A	
A2	LDO_1V8D	
E1	LDO_BMC	
H7	SS	UPC_XA_SS
B10	SENSEP	
A10	SENSEN	
B9	HV_GATE1	
A9	HV_GATE2	
L9	C_CC1	USBC_XA_CC1
L10	C_CC2	USBC_XA_CC2
K9	RPD_G1	USBC_XA_CC1
K10	RPD_G2	USBC_XA_CC2
K6	C_USB_TP	USBC_XA_USB_DBG_TOP_P
L6	C_USB_TN	USBC_XA_USB_DBG_TOP_N
K7	C_USB_BP	USBC_XA_USB_DBG_BOT_P
L7	C_USB_BN	USBC_XA_USB_DBG_BOT_N
K8	C_SBU1	USBC_XA_SBU1
L8	C_SBU2	USBC_XA_SBU2
L11	NC	

C3109 0.47UF 10% 6.3V CERM-X5R 0201

MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000
C3114 220PF 10% 16V CER-X7R 0201
C3113 220PF 10% 16V CER-X7R 0201
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.2000

GROUND
NC L11
NC or GND to dissipate heat

R3105 1M 5% 1/20W MF 201 — UPC_XA_UART_RX 29 30 31

CRITICAL
R3103 15K 0.1% 1/20W TF-LT 0201

TO SMC

REAR PORT:
CONNECT UPC SPI TO ROM
FRONT PORT:
GROUND UPC SPI

L3000
90-OHM-0.1A
EXC4ACE
SYM_HDR-1

29 BI USB2_UPC_XA_P
29 BI USB2_UPC_XA_N
PLACE_NEAR=U3100:5mm

29 PP3V3_S4
PU to PP3V3_S4 if convenient for layout
Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1
R3110 100K 5% 1/20W MF 201
113 27 BI
113 27 BI
R3111 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

A1	GND
D6	GND
E5	GND
E6	GND
E7	GND
F5	GND
G5	GND
H4	GND
H5	GND
G8	GND
H8	GND
L1	GND
B8	GND
D8	GND
E8	GND
F6	GND
F7	GND
F8	GND
G6	GND
G7	GND

GND 29
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

SYNC_MASTER=1362_0900 SYNC_DATE=08/30/2019

PAGE TITLE
USB-C PORT CONTROLLER A

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 31 OF 145
SHEET 30 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

BOM_COST_GROUP=USB-C

PAGE TITLE

USB-C PORT CONTROLLER B

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

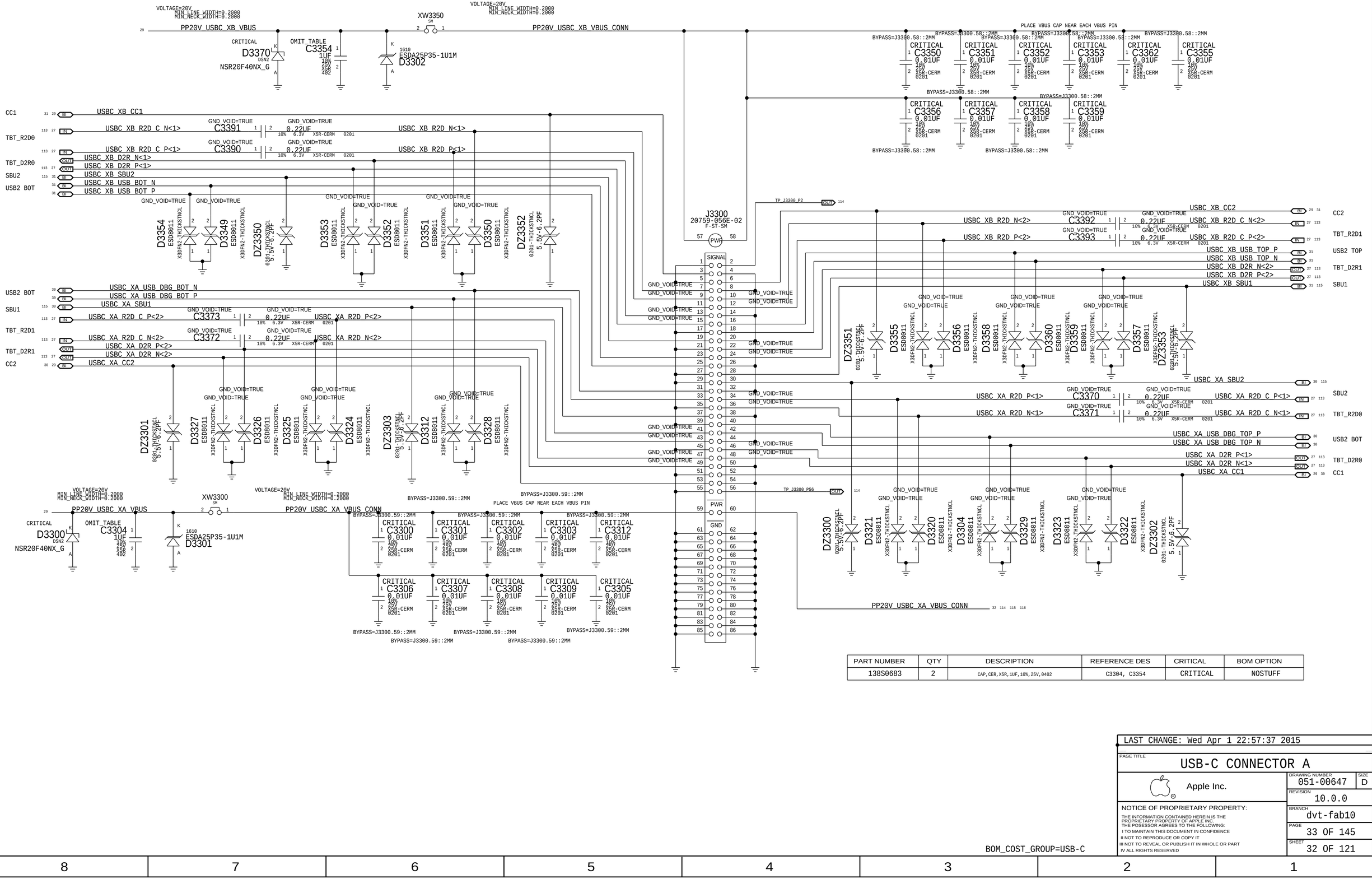
BRANCH: dvt-fab10

PAGE: 32 OF 145

SHEET: 31 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	C3304, C3354	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE

USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

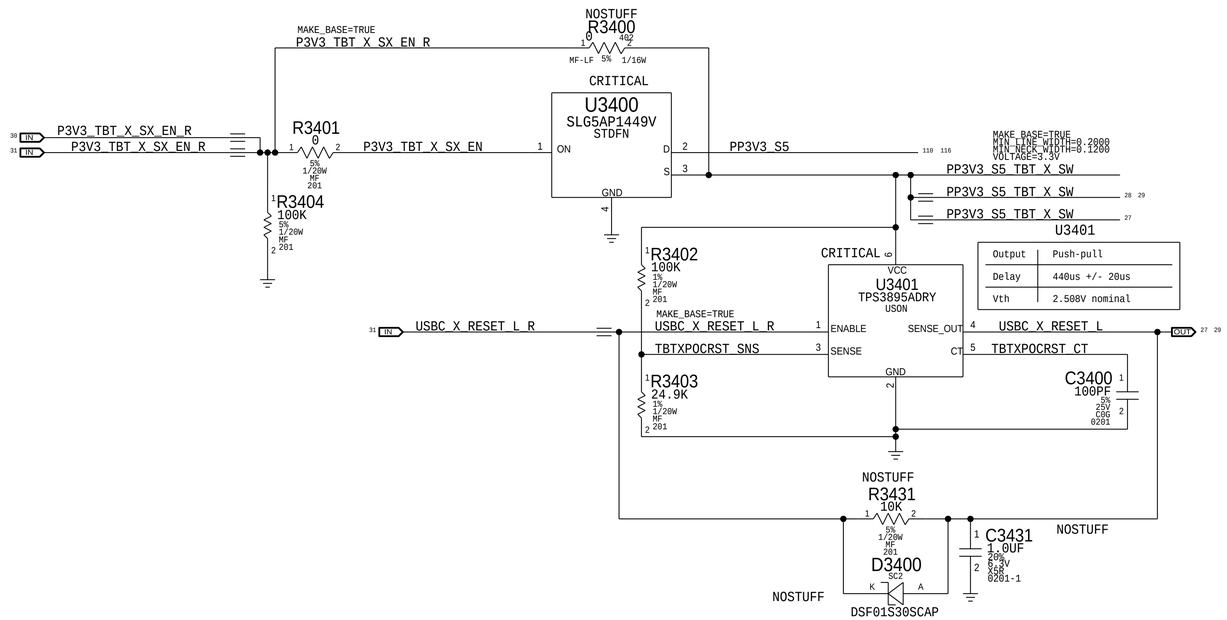
PAGE 33 OF 145

SHEET 32 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

TBT X "POC" Power-up Reset



BOM_COST_GROUP=USB-C

DESIGN: X502/DEV_MLB_U

LAST CHANGE: Wed Feb 18 17:12:24 2015

SYNC_MASTER=X502_MLB SYNC_DATE=03/29/2016

PAGE TITLE

USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

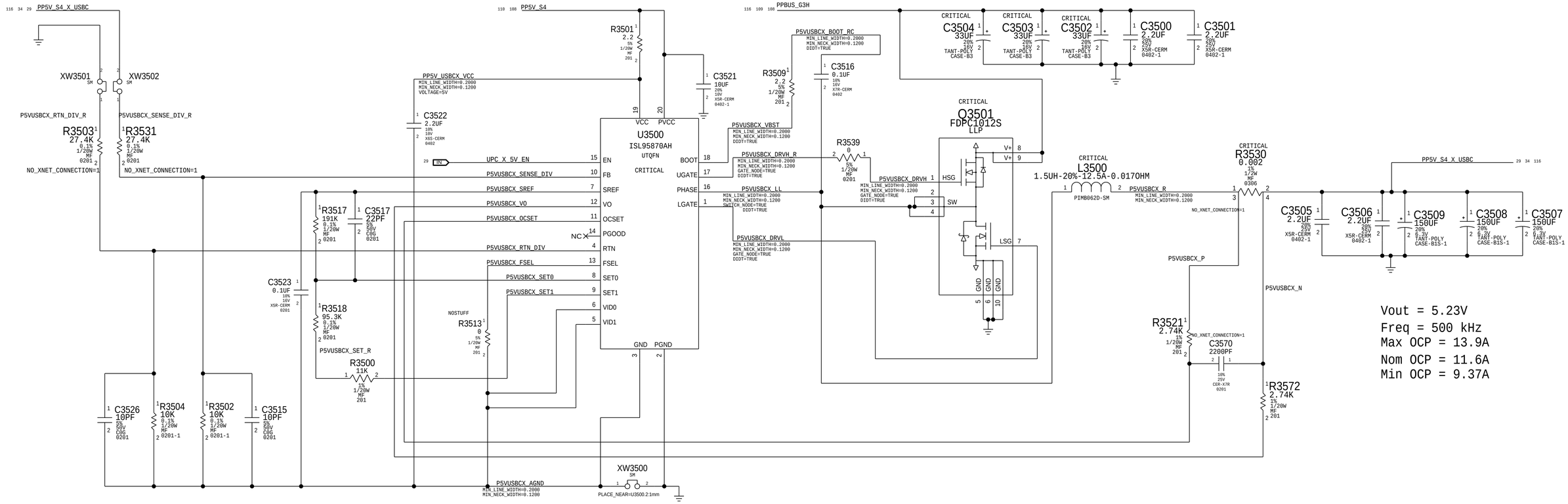
BRANCH dvt-fab10

PAGE 34 OF 145

SHEET 33 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM_COST_GROUP=USB-C

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=12/04/2015

PAGE TITLE: TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

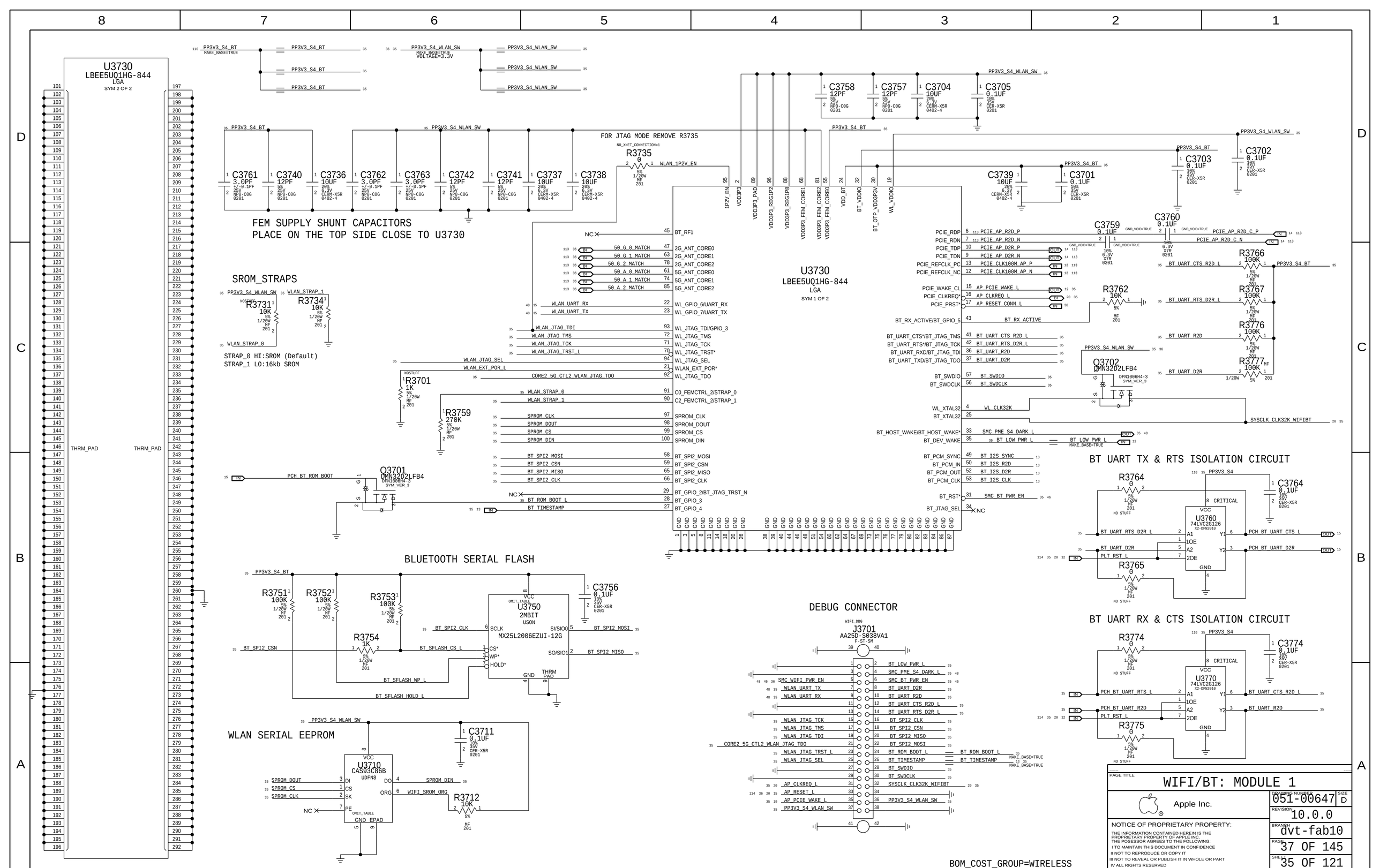
BRANCH: dvt-fab10

PAGE: 35 OF 145

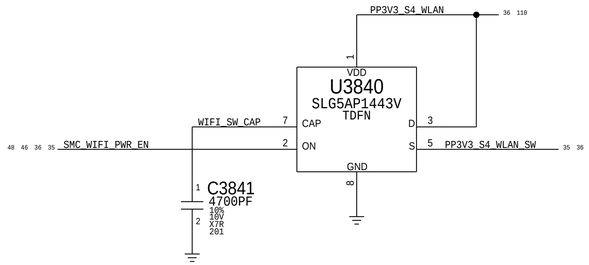
SHEET: 34 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

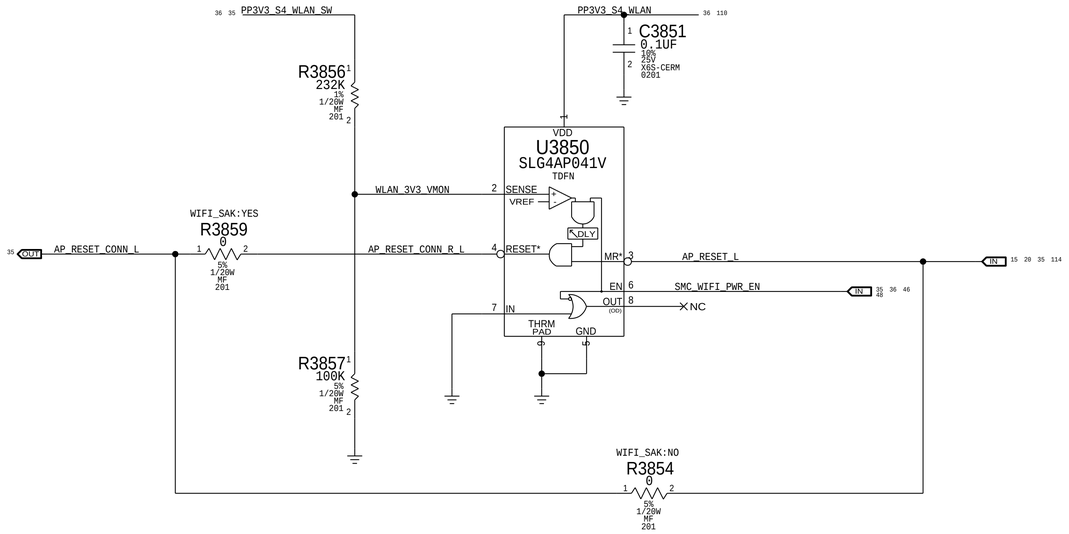

U3730
LBEE5UQ1HG-844
LGA
SYM 2 OF 2
THRM_PAD
THRM_PAD
PP3V3_S4_BT
MAKE_BASE=TRUE
PP3V3_S4_WLAN_SW
MAKE_BASE=TRUE
VOLTAGE=3.3V
FEM SUPPLY SHUNT CAPACITORS
PLACE ON THE TOP SIDE CLOSE TO U3730
C3761 3.0PF
C3740 12PF
C3736 10UF
C3762 3.0PF
C3763 3.0PF
C3742 12PF
C3741 12PF
C3737 10UF
C3738 10UF
FOR JTAG MODE REMOVE R3735
NO_XNET_CONNECTION=1
R3735 0
WLAN_1P2V_EN
C3758 12PF
C3757 12PF
C3704 10UF
C3705 0.1UF
C3739 10UF
C3701 0.1UF
C3703 0.1UF
C3702 0.1UF
C3759 0.1UF
C3760 0.1UF
SROM_STRAPS
R3731 10K
R3734 10K
WLAN_STRAP_1
WLAN_STRAP_0
STRAP_0 HI:SROM (Default)
STRAP_1 LO:16kb SROM
NC
BT_RF1
2G_ANT_CORE0
2G_ANT_CORE1
2G_ANT_CORE2
5G_ANT_CORE0
5G_ANT_CORE1
5G_ANT_CORE2
50_G_0_MATCH
50_G_1_MATCH
50_G_2_MATCH
50_A_0_MATCH
50_A_1_MATCH
50_A_2_MATCH
WL_GPIO_6/UART_RX
WL_GPIO_7/UART_TX
WLAN_UART_RX
WLAN_UART_TX
WL_JTAG_TDI/GPIO_3
WL_JTAG_TMS
WL_JTAG_TCK
WL_JTAG_TRST*
WL_JTAG_SEL
WLAN_EXT_POR*
WL_JTAG_TDO
CORE2_5G_CTL2_WLAN_JTAG_TDO
R3701 1K
R3759 270K
C0_FEMCTRL_2/STRAP_0
C2_FEMCTRL_2/STRAP_1
SPROM_CLK
SPROM_DOUT
SPROM_CS
SPROM_DIN
BT_SPI2_MOSI
BT_SPI2_CSN
BT_SPI2_MISO
BT_SPI2_CLK
BT_GPIO_2/BT_JTAG_TRST_N
BT_GPIO_3
BT_GPIO_4
BT_ROM_BOOT_L
BT_TIMESTAMP
Q3701 DMN32D2LFB4
PCH_BT_ROM_BOOT
BLUETOOTH SERIAL FLASH
R3751 100K
R3752 100K
R3753 100K
R3754 1K
C3756 0.1UF
U3750 2MBIT USON
MX25L2006EZUI-12G
BT_SFLASH_CS_L
BT_SFLASH_WP_L
BT_SFLASH_HOLD_L
WLAN SERIAL EEPROM
C3711 0.1UF
U3710 CAT93C86B UDFN8
WIFI_SROM_ORG
R3712 10K
U3730
LBEE5UQ1HG-844
LGA
SYM 1 OF 2
PCIE_RDP
PCIE_RDN
PCIE_TDP
PCIE_TDN
PCIE_REFCLK_PC
PCIE_REFCLK_NC
PCIE_WAKE_CL
PCIE_CLKREQ*
PCIE_PRST*
PCIE_AP_R2D_P
PCIE_AP_R2D_N
PCIE_AP_D2R_P
PCIE_AP_D2R_N
PCIE_CLK100M_AP_P
PCIE_CLK100M_AP_N
AP_PCIE_WAKE_L
AP_CLKREQ_L
AP_PRST_CONN_L
PCIE_AP_R2D_C_P
PCIE_AP_R2D_C_N
BT_RX_ACTIVE/BT_GPIO_5
BT_RX_ACTIVE
BT_UART_CTS*/BT_JTAG_TMS
BT_UART_RTS*/BT_JTAG_TCK
BT_UART_RXD/BT_JTAG_TDI
BT_UART_TXD/BT_JTAG_TDO
BT_UART_CTS_R2D_L
BT_UART_RTS_D2R_L
BT_UART_R2D
BT_UART_D2R
BT_SWDIO
BT_SWDCLK
WL_XTAL32
BT_XTAL32
SYSCLK_CLK32K_WIFIBT
BT_HOST_WAKE/BT_HOST_WAKE*
BT_DEV_WAKE
SMC_PME_S4_DARK_L
BT_LOW_PWR_L
BT_PCM_SYNC
BT_PCM_IN
BT_PCM_OUT
BT_PCM_CLK
BT_I2S_SYNC
BT_I2S_R2D
BT_I2S_D2R
BT_I2S_CLK
BT_RST*
BT_JTAG_SEL
SMC_BT_PWR_EN
Q3702 DMN32D2LFB4
BT UART TX & RTS ISOLATION CIRCUIT
R3764 0
R3765 0
R3766 100K
R3767 100K
R3776 100K
R3777 100K
U3760 74LVC2G126
BT UART RX & CTS ISOLATION CIRCUIT
R3774 0
R3775 0
U3770 74LVC2G126
DEBUG CONNECTOR
J3701 AA25D-S038VA1
F-ST-SM
BOM_COST_GROUP=WIRELESS
PAGE TITLE
WIFI/BT: MODULE 1
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
37 OF 145
SHEET
35 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

WLAN Power Switch

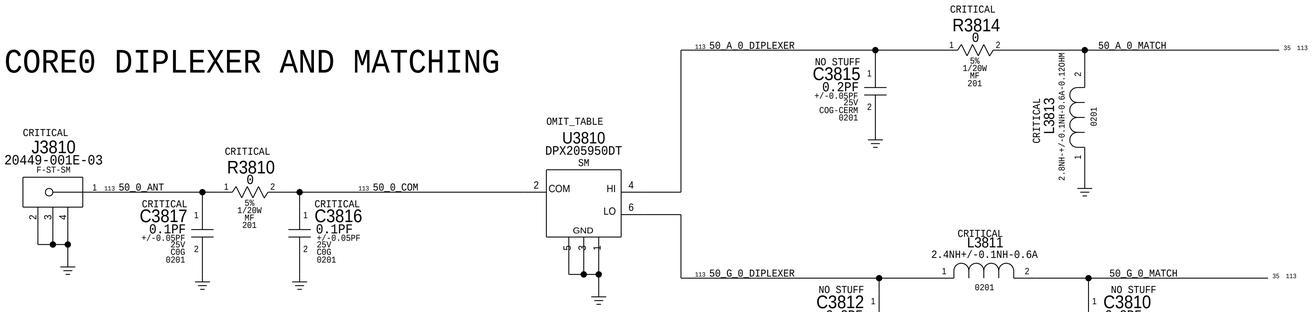


Supervisor & CLKREQ# Isolation

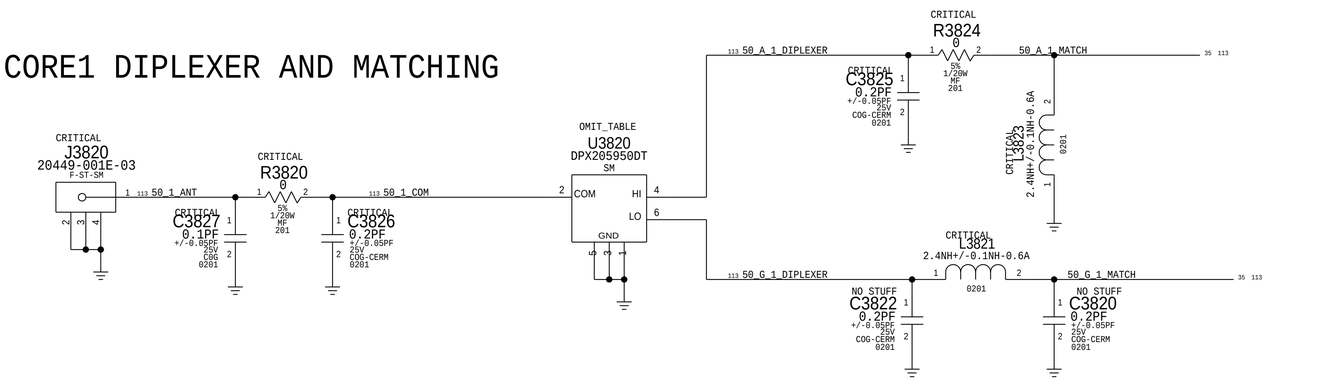
Delay = 130ms +/- 20%



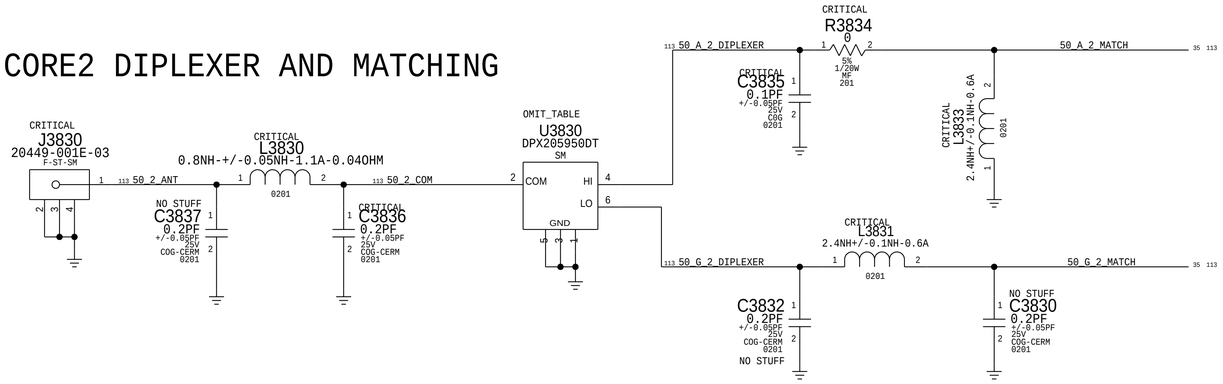
CORE0 DIPLEXER AND MATCHING



CORE1 DIPLEXER AND MATCHING



CORE2 DIPLEXER AND MATCHING



BOM_COST_GROUP=WIRELESS

SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	WIFI/BT: MODULE 2
Apple Inc.	DRAWING NUMBER 051-00647 SIZE D
	REVISION 10.0.0
NOTICE OF PROPRIETARY PROPERTY: THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING: I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART IV ALL RIGHTS RESERVED	BRANCH dvt-fab10
	PAGE 38 OF 145
	SHEET 36 OF 121

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S00136	1	IC,M8+512MB 20NM DDR,A12,S,SCK,BGA780	U3900	CRITICAL	SOC:HYNIX

T208

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
338S00147	1	IC,RTM2,DEV,PN549A1,P61D0	U3905	CRITICAL	SE:DEV
338S00097	1	IC,RTM2,MP,PN549A1,P61D0	U3905	CRITICAL	SE:PROD

SEP ROM

PP1V8_AWAKE_SW3C
C3903 0.1UF 10% 6.3V CERM-X5R 0201
PLACE_NEAR=U3901.8:2mm
U3901 MZ4128 EEPROM MLP
VCC E2 E1 E0 WC* SCL SDA VSS THM_P
SEP_ROM_WC
R3970 10K 5% 1/20W MF 201
SEP_I2C_SCL
SEP_I2C_SDA

L3900

L3900 120-OHM-0.1A-1.5-OHM 0201
PP1V1_SLEEP1_SW2
PP1V1_SLEEP1_PLL_DDR_FILT
VOLTAGE=1.1V
C3900 0.22UF 10% 6.3V X5R-CERM 0201
PP1V1_SLEEP3_BUCK2
VDDIO11_RET_DDR N25
VDDIO11_PLL_DDR U21

unstuff R3951 and stuff R3952 to enable boundary scan
PP1V8_SLEEP2_SW3A
R3952 1K 5% 1/20W MF 201 NOSTUFF
SOC_JTAG_SEL
R3951 10K 5% 1/20W MF 201
M7 needed stronger PU but should be fixed on M8
PP1V8_AWAKE_SW3C
R3953 1K 5% 1/20W MF 201 NOSTUFF
SOC_SWDIO
PP1V8_SLEEP2_SW3A
R3973 10K 5% 1/20W MF 201
PMU_TO_SOC_RESET_L
C3960 100PF 5% 25V C0G 0201

DDR0

NC	L25	DDR0_CA_0
NC	L26	DDR0_CA_1
NC	N26	DDR0_CA_2
NC	N27	DDR0_CA_3
NC	P26	DDR0_CA_4
NC	P25	DDR0_CA_5
NC	M26	DDR0_CK_P
NC	M27	DDR0_CK_N
NC	M25	DDR0_CKE
NC	L27	DDR0_CS
NC	J26	DDR0_DMI_0
NC	V27	DDR0_DMI_1
NC	E26	DDR0_DQ_0
NC	F26	DDR0_DQ_1
NC	G26	DDR0_DQ_2
NC	H26	DDR0_DQ_3
NC	G27	DDR0_DQ_4
NC	K25	DDR0_DQ_5
NC	H27	DDR0_DQ_6
NC	K26	DDR0_DQ_7
NC	AA25	DDR0_DQ_8
NC	Y25	DDR0_DQ_9
NC	W25	DDR0_DQ_10
NC	Y26	DDR0_DQ_11
NC	V26	DDR0_DQ_12
NC	U26	DDR0_DQ_13
NC	T26	DDR0_DQ_14
NC	T27	DDR0_DQ_15
NC	E27	DDR0_DQS_P_0
NC	F27	DDR0_DQS_N_0
NC	W26	DDR0_DQS_P_1
NC	W27	DDR0_DQS_N_1
SOC_PAD_ZQ_A	R26	PAD_ZQ_A
NC	M24	DDR0_RESET_N
SOC_DDR_RREF	N24	DDR0_RREF
PMU_TO_SOC_SLEEP1_PWRGD	L24	DDR0_RET_N
PMU_TO_SOC_SYS_ALIVE	P24	DDR0_SYS_ALIVE

U3900 M8-LPDDR4-H-A-FUSE

OMIT_TABLE
UFBGA
(1 OF 7)

AOP_DETECT_0	AD26	DFR_TOUCH_RESET_L	OUT
AOP_DETECT_1	AD27		NC
AOP_PDM_CLK	AA10		NC
AOP_PDM_DAT	AB10		NC
AOP_PLED_0	AC10		NC
AOP_PLED_1	Y10		NC
AOP_PLED_2	AC14		NC
AOP_PLED_3	AA13		NC
AOP_PLED_4	AD12		NC
AOP_PLED_5	AD13	TP_SOC_CLKOUT	
AOP_PLED_6	AC15		NC
AOP_PLED_7	AB14		NC
AOP_PSENSE_CTRL_4	AA24		NC
AOP_PSENSE_CTRL_5	W24		NC
AOP_PSENSE_CTRL_6	AA21		NC
AOP_PSENSE_CTRL_7	Y24		NC
AOP_PSPI_CS_TRIG_3	AD22	DFR_TOUCH_SPI_CS_L	OUT
AOP_PSPI_CS_TRIG_4	AD23		NC
AOP_PSPI_MISO	AD24	DFR_TOUCH_SPI_MISO	IN
AOP_PSPI_MOSI	Y20	DFR_TOUCH_SPI_MOSI	OUT
AOP_PSPI_SCLK	AB21	DFR_TOUCH_SPI_CLK	OUT
AOP_SPI0_MISO	AC22		NC
AOP_SPI0_MOSI	AC23		NC
AOP_SPI0_SCLK	AD21		NC
AOP_MON_0	AE13	SOC_TO_STOCKHOLM_DWLD_REQ	
AOP_MON_1	AE14		NC
AOP_MON_2	AB15	PCH_SOC_DBELL_L	IN
AOP_MON_3	Y14		NC
AOP_MON_4	AE15	PMU_TO_SOC_IRQ_L	IN
AOP_MON_5	AD15		NC
AOP_MON_6	AA14		NC
AOP_MON_7	AC16		NC
AOP_I2S0_MCK	AA9		NC
AOP_I2S1_MCK	AB9		NC
AOP_SWD_TCK_OUT	AE16		NC
AOP_SWD_TMS0	AD16		NC
AOP_SWD_TMS1	AB16		NC
AOP_I2C0_SCL	AB20	MESA_I2C_SCL	OUT
AOP_I2C0_SDA	AE26	MESA_I2C_SDA	BI
AOP_I2C1_SCL	AE27	ALS_SCL_I2C_1V8	OUT
AOP_I2C1_SDA	AA19	ALS_SDA_I2C_1V8	BI

SOC_JTAG_SEL	AB12	JTAG_SEL	
TP_SOC_JTAG_TRST_L	AB11	JTAG_TRSTN	
SOC_SWDIO	AC13	JTAG_TMS	BI
SOC_SWCLK	AD10	JTAG_TCK	IN
TP_SOC_JTAG_TDI	AD9	JTAG_TDI	
TP_SOC_JTAG_TDO	AA11	JTAG_TDO	
PMU_TO_SOC_RESET_L	AE10	CFSB_AOP	IN
PMU_TO_SOC_SLEEP1_PWRGD	Y12	AOP_DDR_PWRGOOD	IN
SOC_SLEEP1_REQ	AB13	AOP_DDR_REQ	OUT
SOC_WDOG_RST	AE11	WDOG	
SOC_VDD_HI_LO	AE12	SOC_VDD_HI_LO	OUT
	AC11	AOP_DOCK_ATTENTION	NC
	AC12	AOP_DOCK_CONNECT	NC
SOC_CLK_32K	AA22	RT_CLK32768	
PMU_TO_SOC_AWAKE_PWRGD	AB24	AWAKE_PWRGOOD	IN
SOC_AWAKE_REQ	AD11	AWAKE_REQ	OUT
PMU_TO_SOC_RESET_L	AA12	COLD_RESETN	IN

U3900 M8-LPDDR4-H-A-FUSE

OMIT_TABLE
UFBGA
(2 OF 7)

AOP_LSPI_MISO	AA20	NC
AOP_LSPI_MOSI	AB22	NC
AOP_LSPI_SCLK	AD25	NC
AOP_SPI_CS_TRIG_0	AE20	NC
AOP_SPI_CS_TRIG_1	AB17	MESA_PWR_EN
AOP_SPI_CS_TRIG_2	AB18	SOC_TO_STOCKHOLM_DEV_WAKE
AOP_SPI_CS_TRIG_3	AE21	SOC_SPI_BOOT_STATUS
AOP_SPI_CS_TRIG_4	AD19	NC
AOP_SPI_CS_TRIG_5	AA17	NC
AOP_SPI_CS_TRIG_6	AC19	NC
AOP_SPI_CS_TRIG_7	AE22	NC
AOP_SPI_CS_TRIG_8	AE23	NC
AOP_SPI_CS_TRIG_9	AB19	NC
AOP_SPI_CS_TRIG_10	AA18	NC
AOP_SPI_CS_TRIG_11	AE24	NC
AOP_SPI_CS_TRIG_12	AD20	NC
AOP_SPI_CS_TRIG_13	AC21	NC
AOP_SPI_CS_TRIG_14	Y18	NC
AOP_SPI_CS_TRIG_15	AE25	NC
AOP_UART0_CTSN	AC17	NC
AOP_UART0_RTSN	AE18	NC
AOP_UART0_RXD	AE17	NC
AOP_UART0_TXD	AA15	NC
AOP_UART1_CTSN	AA16	NC
AOP_UART1_RTSN	AE19	NC
AOP_UART1_RXD	AD17	NC
AOP_UART1_TXD	AC18	NC
AOP_UART2_RXD	AD18	NC
AOP_UART2_TXD	Y16	NC

R3900 499 1% 1/20W MF 201
PP1V8_SLEEP2_LPLL_FILT
VOLTAGE=1.8V
C3902 0.47UF 10% 6.3V CERM-X5R 0201
PP1V8_SLEEP2_SW3A
VDD18_LPPLL AA23
R3943 78.7K 1% 1/20W MF 201
PPSVDD_STOCKHOLM

STOCKHOLM

PP3V3_S0_LEFT
C3919 4.7UF 20% 6.3V X5R 402
PP_STOCKHOLM_TVDD
C3925 1.0UF 20% 6.3V X5R 0201-1
PPVDD_STOCKHOLM
C3916 0.1UF 10% 6.3V CERM-X5R 0201
C3917 1.0UF 20% 6.3V X5R 0201-1
PP1V8_AWAKE_SW3C
C3918 1.0UF 20% 6.3V X5R 0201-1
PPSVDD_STOCKHOLM
C3915 0.1UF 10% 6.3V CERM-X5R 0201

OMIT_TABLE
U3905
PN66VEU3-A101D004
UFLGA

IRQ	D1	SPIM_IRQ	F1
SVDD_REQ	A5	SIM_SWIO	A4
DWL	B2	GPIO0	A7
CLK_REQ	A2	SPIM_NSS	A6
NFC_CLK_XTAL1	A3	TX_PWR_REQ	D5
RX	C1	ESE_DWPM_DBG	G7
TX	B1	ESE_DWPS_DBG	G6
CTS	D2	RXP	F6
RTS	A1	RXN	F5
VEN	E1	TX1	G3
SMX_RST*	E3	TX2	G5
SMX_CLK	E4	WKUP_REQ	E5
ESE_IO1	F4	VMID	F7
SPIM_MOSI	B3	SE2_PWR_REQ	F2
SPIM_MISO	B4	SE2_SVDD_IN	G1
SPIM_SCK	E6		
XTAL2	C3		

SOC_TO_STOCKHOLM_DWLD_REQ
UART_SOC_TO_STOCKHOLM_TXD
UART_STOCKHOLM_TO_SOC_TXD
UART_SOC_TO_STOCKHOLM_RTS_L
UART_STOCKHOLM_TO_SOC_RTS_L
SOC_TO_STOCKHOLM_EN
PPSVDD_STOCKHOLM
SOC_TO_STOCKHOLM_DEV_WAKE

C3920 0.1UF 10% 6.3V CERM-X5R 0201

4MB SPI ROM

OMIT_TABLE
U3906 4MX8-1.8V UFDFPN N25Q032A11E
R3942 10K 5% 1/20W MF 201
R3941 10K 5% 1/20W MF 201
SOC_ROM_SPI_CLK_R
SOC_ROM_SPI_CS_L
SOC_ROM_SPI_WP_L
SOC_ROM_SPI_RST_L
SOC_ROM_SPI_MOSI_R
SOC_ROM_SPI_MISO_R

I2C Pullups

PP1V8_AWAKE_SW3C
R3904 2.2K 5% 1/20W MF 201
R3905 2.2K 5% 1/20W MF 201
SEP_I2C_SCL
SEP_I2C_SDA
R3911 2.2K 5% 1/20W MF 201
R3912 2.2K 5% 1/20W MF 201
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
PP1V8_S0SW_DFR
R3915 2.2K 5% 1/20W MF 201
R3916 2.2K 5% 1/20W MF 201
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA

32K CLK OPTION

PLACE_NEAR=U3900.AA22:3mm
R3990 0 5% 1/20W MF 0201
SOC_PMU_CLK_32K
GREENCLK
SOC_CLK_32K
SOC
R3925 0 5% 1/20W MF 0201 NOSTUFF
PMU_TO_SOC_CLK_32K
SOC PMU
PLACE_NEAR=U3900.AA22:3mm

PP1V1_SLEEP1_SW2
R3901 240 1% 1/20W MF 201
R3902 240 1% 1/20W MF 201
SOC_PAD_ZQ_A
SOC_DDR_RREF
PMU_TO_SOC_SLEEP1_PWRGD
PMU_TO_SOC_SYS_ALIVE

T208 DFU_STATUS Isolation

DFU_STATUS can be driven high outside of S0
U3910 creates version that is only high in S0
PP1V8_S0
R3981 0 5% 1/20W MF 0201
DFU_STATUS
DFU_SPI_STATUS
U3910 74LVC2G08GT/S505 SOT833
PCH_SOC_DFU_STATUS
R3980 0 5% 1/20W MF 0201 NOSTUFF
SOC_SPI_BOOT_STATUS

T208 WDOG Isolation

SOC_WDOG_RESET can be driven high outside of S0
U3910 creates version that is only high in S0
PP1V8_S0
C3950 0.1UF 10% 6.3V CERM-X5R 0201
U3910 74LVC2G08GT/S505 SOT833
SOC_WDOG_RST
R3972 300K 5% 1/20W MF 201
PCH_SOC_WDOG
R3971 100K 5% 1/20W MF 201

PP1V8_S0
R3960 3.0K 5% 1/20W MF 201
R3961 3.0K 5% 1/20W MF 201
ALS_SCL_I2C_1V8
ALS_SDA_I2C_1V8
R3906 1K 5% 1/20W MF 201
R3907 1K 5% 1/20W MF 201
I2C_CAM_SCL
I2C_CAM_SDA
PP1V8_S0SW_DFR
R3917 4.7K 5% 1/20W MF 201
R3918 4.7K 5% 1/20W MF 201
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA

SOC_TO_STOCKHOLM_DWLD_REQ
R3940 100K 5% 1/20W MF 201 NOSTUFF

BOM_COST_GROUP=T151

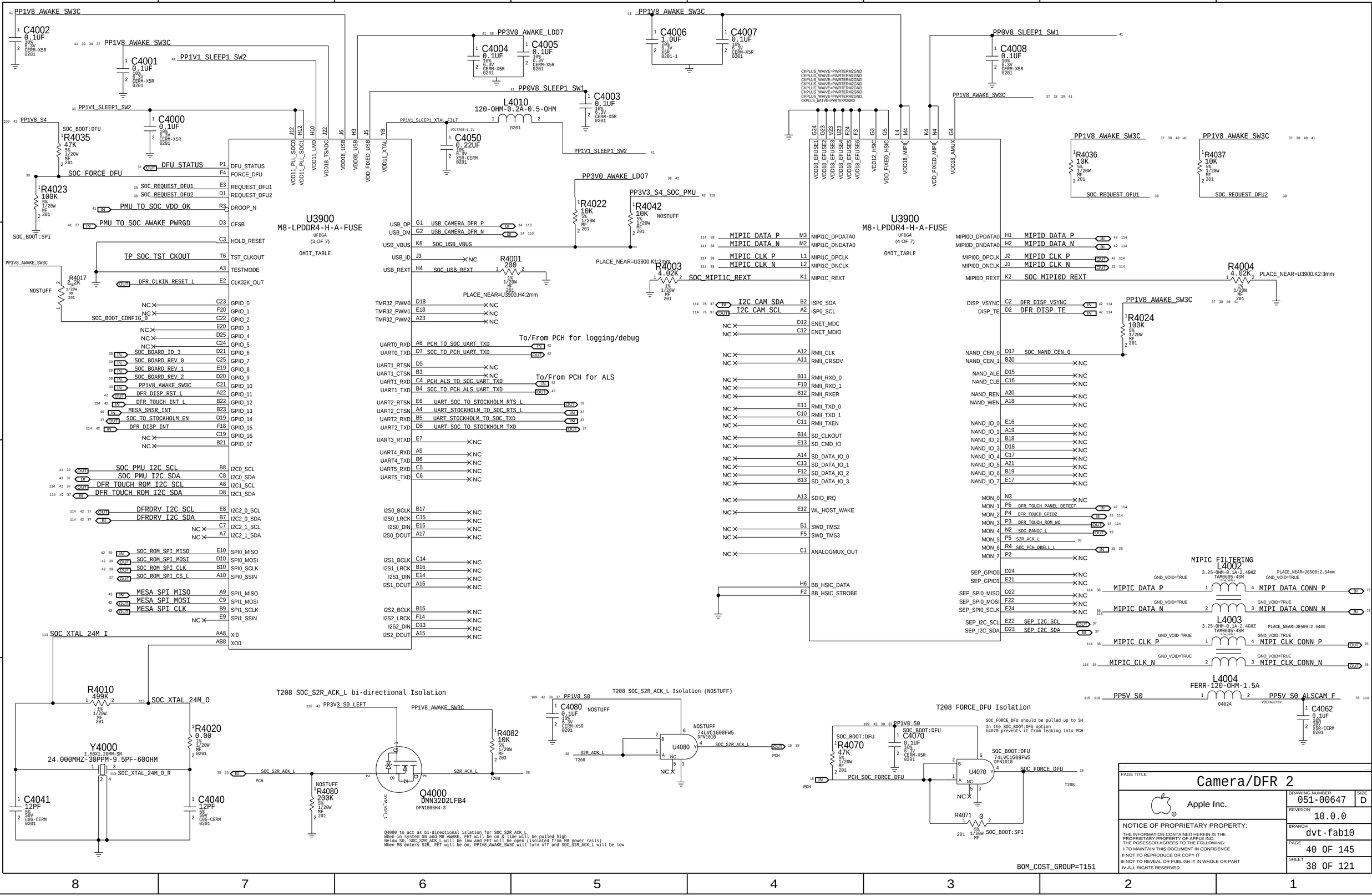
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S00203	1	IC,FLASH,SERIAL,SPI,4MX8,4X3MM,DFN8	U3906		

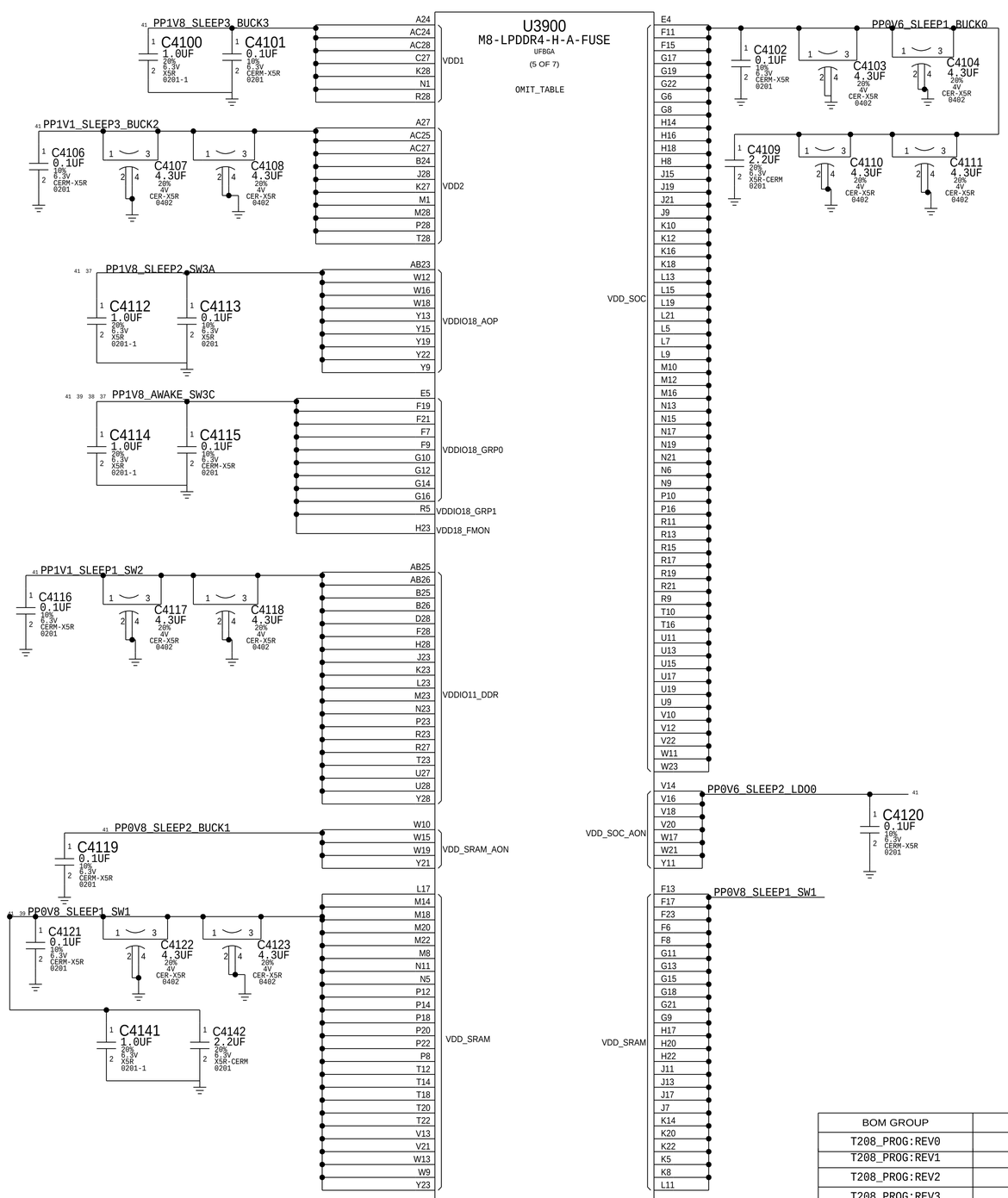
PAGE TITLE: Camera/DFR 1

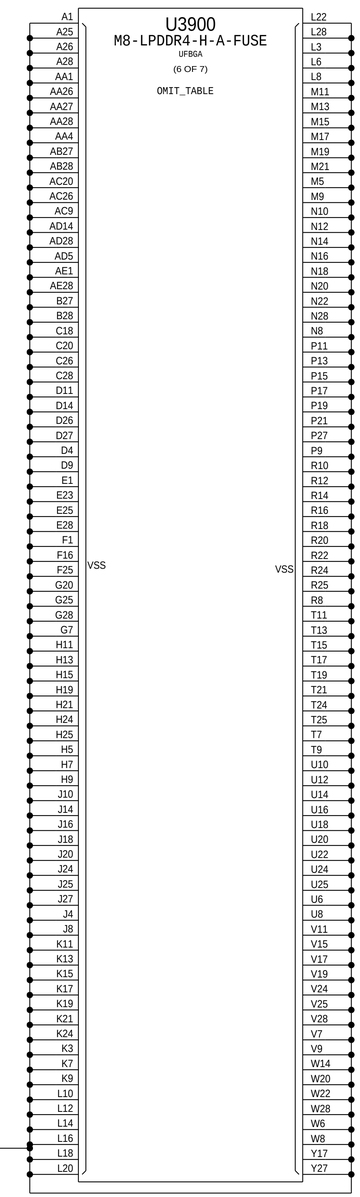
Apple Inc.

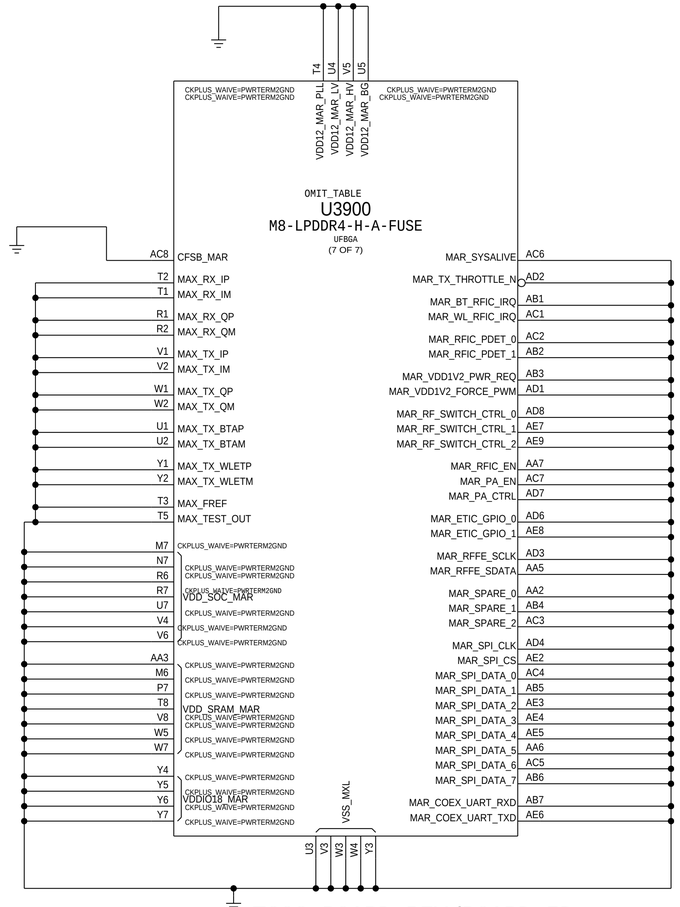
DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 39 OF 145
SHEET: 37 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


PP1V8_AWAKE_SW3C
C4002 0.1UF 10% 6.3V CERM-X5R 0201
C4001 0.1UF 10% 6.3V CERM-X5R 0201
PP1V1_SLEEP1_SW2
C4000 0.1UF 10% 6.3V CERM-X5R 0201
PP1V8_S4
R4035 47K 5% 1/20W MF 201
SOC_BOOT:DFU
SOC_FORCE_DFU
R4023 100K 5% 1/20W MF 201
SOC_BOOT:SPI
PP1V8_AWAKE_SW3C
R4017 2.2K 1/20W MF 201
NOSTUFF
PP3V0_AWAKE_LDO7
C4004 0.1UF 10% 6.3V CERM-X5R 0201
C4005 0.1UF 10% 6.3V CERM-X5R 0201
PP0V8_SLEEP1_SW1
C4003 0.1UF 10% 6.3V CERM-X5R 0201
L4010 120-OHM-0.2A-0.5-OHM 0201
PP1V1_SLEEP1_XTAL_FILT
C4050 0.22UF 10% 6.3V X5R-CERM 0201
VOLTAGE=1.1V
PP1V1_SLEEP1_SW2
PP3V0_AWAKE_LDO7
R4022 10K 5% 1/20W MF 201
PP3V3_S4_SOC_PMU
R4042 10K 5% 1/20W MF 201
NOSTUFF
PLACE_NEAR=U3900.K1:2mm
R4003 4.02K 1% 1/20W MF 201
R4001 200 1% 1/20W MF 201
PLACE_NEAR=U3900.H4:2mm
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(3 OF 7)
OMIT_TABLE
U3900
M8-LPDDR4-H-A-FUSE
UFBGA
(4 OF 7)
OMIT_TABLE
DFU_STATUS
SOC_REQUEST_DFU1
SOC_REQUEST_DFU2
PMU_TO_SOC_VDD_OK
PMU_TO_SOC_AWAKE_PWRGD
TP_SOC_TST_CKOUT
DFR_CLKIN_RESET_L
SOC_BOARD_ID_3
SOC_BOARD_REV_0
SOC_BOARD_REV_1
SOC_BOARD_REV_2
PP1V8_AWAKE_SW3C
DFR_DISP_RST_L
DFR_TOUCH_INT_L
MESA_SNSR_INT
SOC_TO_STOCKHOLM_EN
DFR_DISP_INT
SOC_PMU_I2C_SCL
SOC_PMU_I2C_SDA
DFR_TOUCH_ROM_I2C_SCL
DFR_TOUCH_ROM_I2C_SDA
DFRDRV_I2C_SCL
DFRDRV_I2C_SDA
SOC_ROM_SPI_MISO
SOC_ROM_SPI_MOSI
SOC_ROM_SPI_CLK
SOC_ROM_SPI_CS_L
MESA_SPI_MISO
MESA_SPI_MOSI
MESA_SPI_CLK
SOC_XTAL_24M_I
SOC_XTAL_24M_O
To/From PCH for logging/debug
To/From PCH for ALS
MIPIC_DATA_P
MIPIC_DATA_N
MIPIC_CLK_P
MIPIC_CLK_N
SOC_MIPI1C_REXT
I2C_CAM_SDA
I2C_CAM_SCL
MIPID_DATA_P
MIPID_DATA_N
MIPID_CLK_P
MIPID_CLK_N
SOC_MIPI0D_REXT
DFR_DISP_VSYNC
DFR_DISP_TE
SOC_NAND_CEN_0
MIPIC FILTERING
L4002 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM
L4003 3.25-OHM-0.1A-2.4GHZ TAM0605-4SM
L4004 FERR-120-OHM-1.5A
PP5V_S0
PP5V_S0_ALSCAM_F
R4010 499K 1% 1/20W MF 201
Y4000 1.60X1.20MM-SM 24.000MHZ-30PPM-9.5PF-600HM
R4020 0.00 1% 1/20W MF 0201
C4041 12PF 5% 50V C0G-CERM 0201
C4040 12PF 5% 50V C0G-CERM 0201
T208 SOC_S2R_ACK_L bi-directional Isolation
PP3V3_S0_LEFT
R4082 10K 5% 1/20W MF 201
R4080 200K 5% 1/20W MF 201
NOSTUFF
Q4000 DMN32D2LFB4 DFN1006H4-3
Q4000 to act as bi-directional islation for SOC_S2R_ACK_L
When in system S0 and M8 AWAKE, FET will be on & line will be pulled high
Below S0, SOC_S2R_ACK_L will be low and FET will be open (isolated from M8 power rails)
When M8 enters S2R, FET will be on, PP1V8_AWAKE_SW3C will turn off and SOC_S2R_ACK_L will be low
T208 SOC_S2R_ACK_L Isolation (NOSTUFF)
C4080 0.1UF 10% 6.3V CERM-X5R 0201
NOSTUFF
U4080 74LVC1G08FW5 DFN1010
T208 FORCE_DFU Isolation
SOC_FORCE_DFU should be pulled up to S4
In the SOC_BOOT:DFU option
U4070 prevents it from leaking into PCH
R4070 47K 5% 1/20W MF 201
C4070 0.1UF 10% 6.3V CERM-X5R 0201
U4070 74LVC1G08FW5 DFN1010
PCH_SOC_FORCE_DFU
R4071 0 5% 1/20W MF 201
SOC_BOOT:SPI
BOM_COST_GROUP=T151
PAGE TITLE
Camera/DFR 2
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 40 OF 145
SHEET 38 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



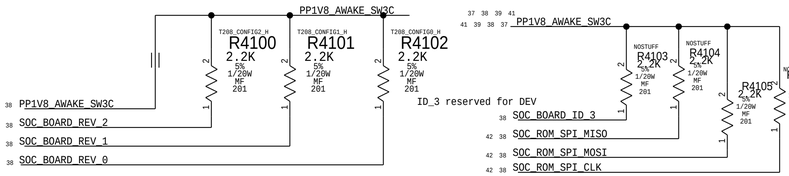




T208 BOARD REV/BOARD ID

S/W READ FLOW

1. SET GPIO AS INPUT
2. DISABLE PU AND ENABLE PD
3. READ
4. DISABLE PD AND ENABLE PU



BOARD REV[3:0]	MODE
1111	T208_Rev0 (X362 P0)
1110	T208_Rev1 (X363 P0)
1101	T208_Rev2 (X362 P1)
1100	T208_Rev3 (X362 P2)
1011	T208_Rev4 (X363 P2/X362 localEVT)
1010	T208_Rev5 (X363 EVT/X362 EVT1)

BOARD ID[3:0]	MODE
1XXX	T202 DEV
0010	T208

BOM GROUP	BOM OPTIONS
T208_PROG:REV0	T208_CONFIG2_H,T208_CONFIG1_H,T208_CONFIG0_H
T208_PROG:REV1	T208_CONFIG2_H,T208_CONFIG1_H
T208_PROG:REV2	T208_CONFIG2_H,T208_CONFIG0_H
T208_PROG:REV3	T208_CONFIG2_H
T208_PROG:REV4	T208_CONFIG1_H, T208_CONFIG0_H
T208_PROG:REV5	T208_CONFIG1_H

BOM_COST_GROUP=T151

PAGE TITLE
Camera/DFR 3

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 41 OF 145
SHEET 39 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Berkelium

FB for Bucks

R4200 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK0_FB — PP0V6_SLEEP1_BUCK0

R4201 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK1_FB — PP0V8_SLEEP1_SW1

R4202 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK2_FB — PP1V1_SLEEP3_BUCK2

R4203 0 5% 1/16W MF-LF 402
SOC_PMU_BUCK3_FB — PP1V8_SLEEP3_BUCK3

Q4201

CSD58892Q2
SON2X2
PP0V8_SLEEP2_BUCK1
SW1_EXT_ON
PP0V8_SLEEP1_SW1

U4200

D2346A1-OTP-CE
WLCSP
SYM 1 OF 2

PP3V3_S4_SOC_PMU
PLACE_NEAR=U4200.K11:2mm
C4203 15UF 20% 6.3V CERM 0402

PLACE_NEAR=U4200.F12:2mm
PLACE_NEAR=U4200.A7:2mm
PLACE_NEAR=U4200.A2:2mm
C4204 15UF 20% 6.3V CERM 0402
C4205 15UF 20% 6.3V CERM 0402
C4206 15UF 20% 6.3V CERM 0402

PLACE_NEAR=U4200.D1:2mm
C4202 15UF 20% 6.3V CERM 0402

VDD_MAIN_BUCK0 A7
VDD_MAIN_BUCK1 A8
VDD_MAIN_BUCK2 A2
VDD_MAIN_BUCK3 F12
VDD_MAIN_BUCK4 G12
VDD_MAIN_BB D1
VDD_MAIN_CHG K11
VDD_MAIN_CHG L11
VDD_MAIN_CHG M11
VDD_MAIN_BBCORE J1
ACT_DIODE K3
VDD_MAIN_SW4 L2
VBAT K12
VBAT L12
VBAT M12
VBAT_S K10
NC C6
SW0_EXT
SW1_EXT_ON D7
SW1_EXT
BB_LX1 E1
BB_LX2 G1
BB_FB J3
BB_OUT H1
VDD_HVLDO_237 M4
VDD_HVLDO_45 N2
VDD_HVLDO_RTC L8
VDD_HVLDO_SW6 L3
LDO2_OUT M5
LDO3_OUT N4
LDO4_OUT M1
LDO5_OUT N3
LDO7_OUT N5
SW4_OUT M2
VDD_MAIN_LDO_16 M10
VDD_MAIN_LDO_8 M6
VDD_MAIN_LDO_9 M9
VDD_MAIN_LDO_AUX N7
LDO1_OUT N10
LDO6_OUT N9
LDO8_OUT N6
LDO9_OUT M8
AUX_PWR_OUT N8
SW1_IN B10
SW1_OUT A11
LDO0_OUT C10
SW2_IN B1
SW2_OUT C1
SW3_IN B12
SW3A_OUT B11
SW3B_OUT C11
SW3C_OUT C12
SW5_IN K1
SW5_OUT L1
SW6_OUT K2

PP3V3_S4_SOC_PMU
PLACE_NEAR=U4200.E1:3mm
C4207 15UF 20% 6.3V CERM 0402

PP3V3_S4_SOC_PMU
C4219 2.2UF 20% 6.3V X5R-CERM 0201
C4218 2.2UF 20% 6.3V X5R-CERM 0201
PLACE_NEAR=U4200.M4:2mm
PLACE_NEAR=U4200.L8:2mm

PP3V3_S4_SOC_PMU
C4220 2.2UF 20% 6.3V X5R-CERM 0201

PP3V3_S4_SOC_PMU
PP3V3_S4_AWAKE_PWRTERM2GND

VOLTAGE=1.8V
PP1V8_ALWAYS_LDO9
C4227 0.22UF 10% 6.3V CERM-X5R 0201
C4226 0.022UF 10% 6.3V X5R-CERM 0201

VOLTAGE=0.6V
C4228 2.2UF 20% 6.3V X5R-CERM 0201

PP0V8_SLEEP2_BUCK1
PP0V8_SLEEP1_SW1
PP0V6_SLEEP2_LDO0
PP1V1_SLEEP3_BUCK2
PP1V1_SLEEP1_SW2
PP1V8_SLEEP3_BUCK3
PP1V8_SLEEP2_SW3A
PP1V8_AWAKE_SW3C
PP3V0_AWAKE_LDO7

VSS1 B2
VSS2 B9
VSS3 C4
VSS3 C5
VSS4 E5
VSS4 E6
VSS4 H5
VSS4 H6
VSS4 F5
VSS4 F6
VSS4 G5
VSS4 G6
VSS6 M3
VSS7 M7
VSS8 G8
VSS8 H7
VSS8 H8
VSS8 E7
VSS8 F7
VSS8 F8
VSS8 G7
VSS8 A1
VSS9 A12
VSS9 N1
VSS9 N12

VDD_SOC

501MA MAX

BUCK0_LX A6 — SOC_PMU_BUCK0_LX
BUCK0_FB C9 — SOC_PMU_BUCK0_FB
CRITICAL Place same side as PMU
L4202 1.0UH-1.82A-0.203OHM MCFK2012-SM
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
C4208 15UF 20% 6.3V CERM 0402
C4209 15UF 20% 6.3V CERM 0402
C4210 2.2UF 20% 6.3V X5R-CERM 0201
C4230 2.2UF 20% 6.3V X5R-CERM 0201
PP0V6_SLEEP1_BUCK0
Mirror Capacitors in Layout

VDD_SRAM_AON VDD_SRAM VDD_SOC_AON

VDD_FIXED_MIPI
VDD_FIXED_USB
300MA MAX

BUCK1_LX A9 — SOC_PMU_BUCK1_LX
BUCK1_FB D9 — SOC_PMU_BUCK1_FB
CRITICAL Place same side as PMU
L4203 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
C4211 4.2UF 10% 10V X5R-CERM 0402-1
C4231 4.2UF 10% 10V X5R-CERM 0402-1
C4233 4.7UF 20% 6.3V CER-X5R 0402
C4232 4.7UF 20% 6.3V CER-X5R 0402
PP0V8_SLEEP2_BUCK1
Mirror Capacitors in Layout

VDD2 VDDQ VDD11_XTAL

460MA MAX

BUCK2_LX A3 — SOC_PMU_BUCK2_LX
BUCK2_FB C2 — SOC_PMU_BUCK2_FB
CRITICAL Place same side as PMU
L4204 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
C4238 10UF 20% 6.3V CERM-X5R 0402
C4239 10UF 20% 6.3V CERM-X5R 0402
C4240 4.7UF 20% 6.3V CER-X5R 0402
C4241 4.7UF 20% 6.3V CER-X5R 0402
PP1V1_SLEEP3_BUCK2
Mirror Capacitors in Layout

VDD1 VDD18_USB VDDIO18_GRP0

100MA MAX

BUCK3_LX E12 — SOC_PMU_BUCK3_LX
BUCK3_FB D10 — SOC_PMU_BUCK3_FB
CRITICAL Place same side as PMU
L4205 1.0UH-1.3A-0.326OHM MCFK1608T1R0M NA
MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 DIDT=TRUE SWITCH_NODE=TRUE
C4234 4.7UF 20% 6.3V CER-X5R 0402
C4235 4.7UF 20% 6.3V CER-X5R 0402
C4236 4.7UF 20% 6.3V CER-X5R 0402
C4237 4.7UF 20% 6.3V CER-X5R 0402
PP1V8_SLEEP3_BUCK3
Mirror Capacitors in Layout

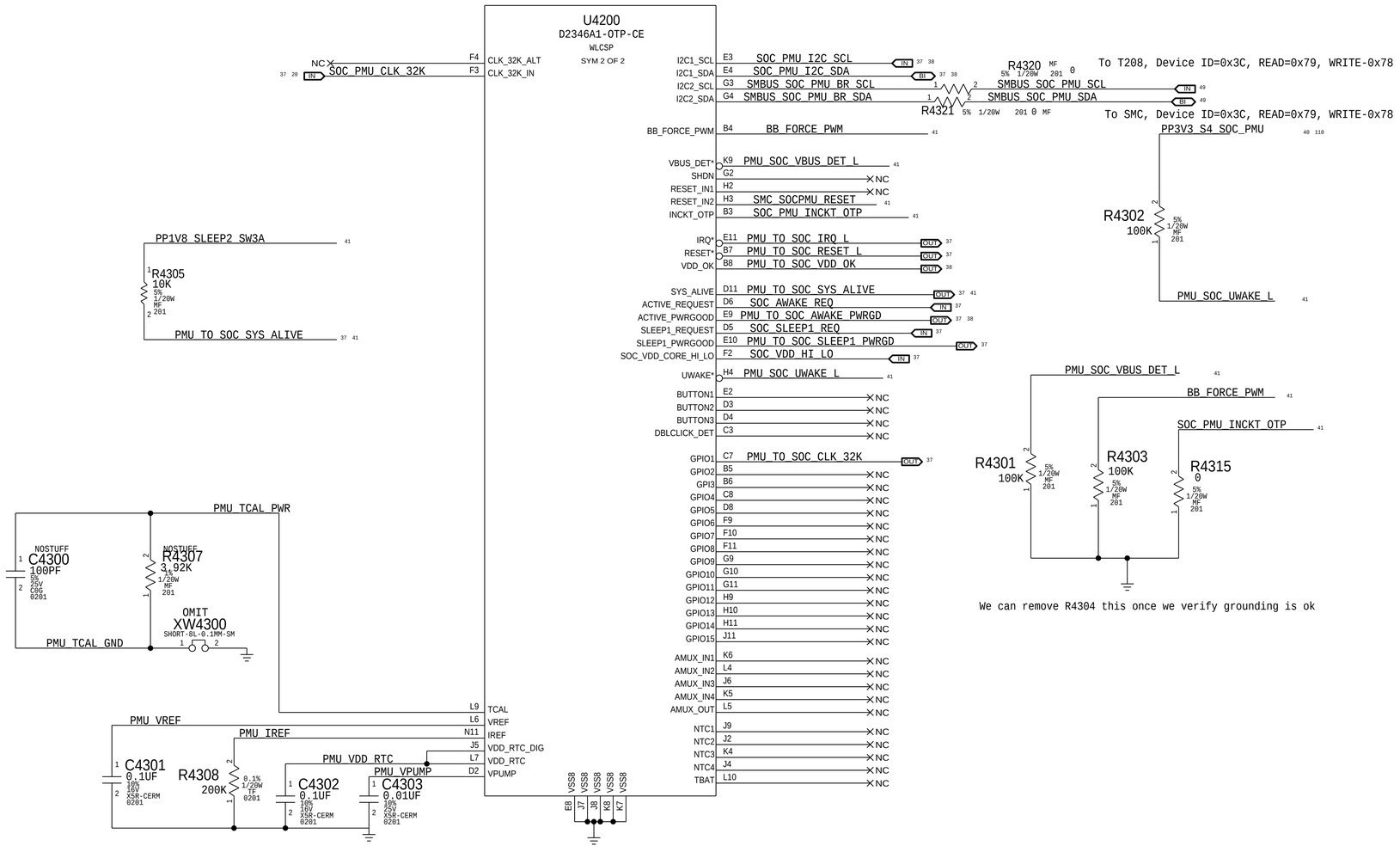
Not using Buck4
BUCK4_LX H12 — NC
BUCK4_FB J10 — NC

BOM_COST_GROUP=T151

PAGE TITLE: Berkelium - 1
Apple Inc.
DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 42 OF 145
SHEET: 40 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Berkelium - 2



T208 POWER ALIASES

BUCK0
PP0V6_SLEEP1_BUCK0 = PP0V6_SLEEP1_BUCK0
VOLTAGE=0.6V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE

BUCK1
LDO0
PP0V6_SLEEP2_LDO0 = PP0V6_SLEEP2_LDO0
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=0.6V

SW1
PP0V8_SLEEP2_BUCK1 = PP0V8_SLEEP2_BUCK1
VOLTAGE=0.8V
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
PP0V8_SLEEP1_SW1 = PP0V8_SLEEP1_SW1
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=0.8V

BUCK2
PP1V1_SLEEP3_BUCK2 = PP1V1_SLEEP3_BUCK2
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=1.1V

SW2
PP1V1_SLEEP1_SW2 = PP1V1_SLEEP1_SW2
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=1.1V

BUCK3
PP1V8_SLEEP3_BUCK3 = PP1V8_SLEEP3_BUCK3
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=1.8V

SW3A
PP1V8_SLEEP2_SW3A = PP1V8_SLEEP2_SW3A
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=1.8V

SW3C
PP1V8_AWAKE_SW3C = PP1V8_AWAKE_SW3C
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=1.8V

LDO7
PP3V0_AWAKE_LDO7 = PP3V0_AWAKE_LDO7
MIN_LINE_WIDTH=0.0900
MIN_NECK_WIDTH=0.0520
MAKE_BASE=TRUE
VOLTAGE=3.0V

Signal Aliases

SMC_SOCPMU_RESET = SMC_SOCPMU_RESET
MAKE_BASE=TRUE

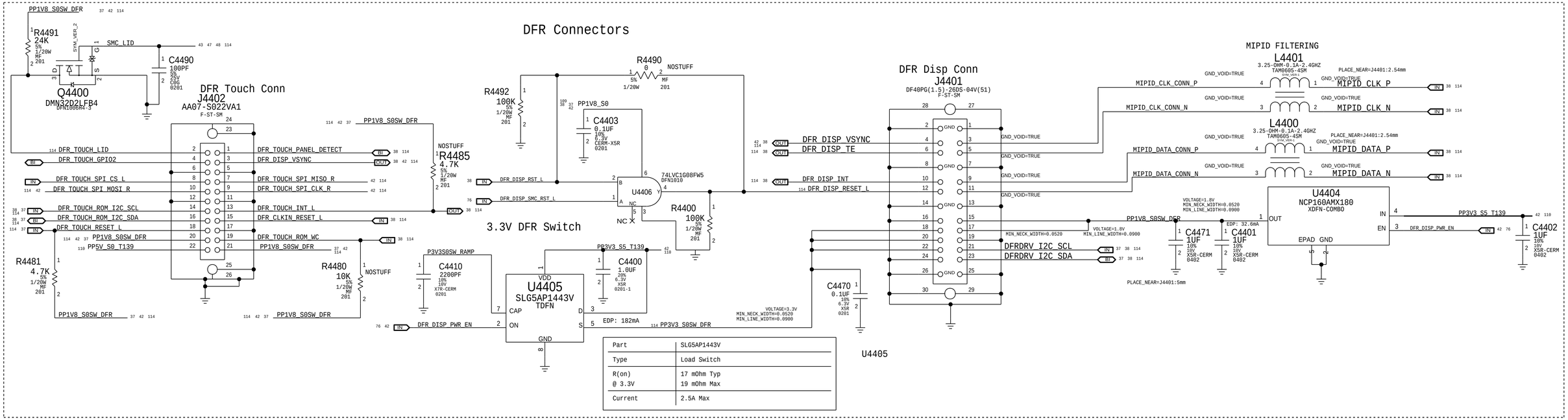
BOM_COST_GROUP=T151

PAGE TITLE	Berkelium - 2
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 43 OF 145
	SHEET 41 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

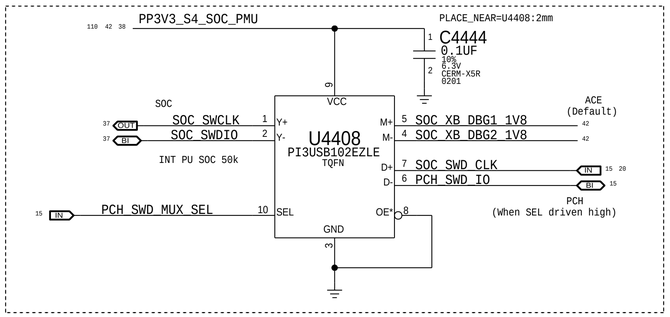
T208 Support

DFR Connectors



Part	SLG5AP1443V
Type	Load Switch
R(on) @ 3.3V	17 mOhm Typ 19 mOhm Max
Current	2.5A Max

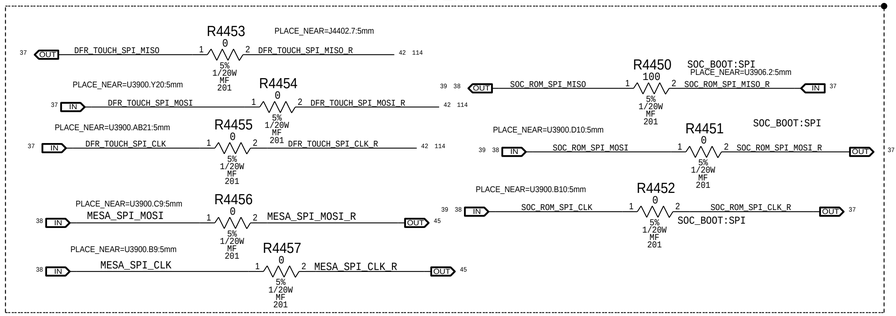
SWD DEBUG MUX



T208 I2C Mapping

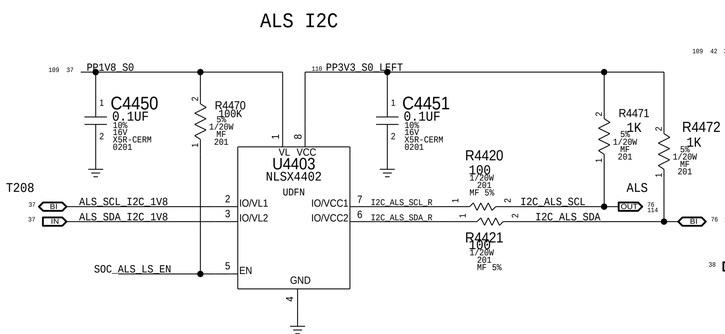
Bus	Device	7-bit Address	8-bit Address Read	8-bit Address Write
AP0	PMU	0011110 (0x3C)	0x79	0x78
AP1	Touch EEPROM	1010000 (0x50)	0xA1	0xA0
AP2_0	Tesla	1010100 (0x4C)	0x99	0x98
AOP0	Mesa EEPROM	101000x (0x50/0x51)	0xA1/A3	0xA0/A2
AOP1	ALS	0111001 (0x39)	0x73	0x72
SEP	M34128 EEPROM	1010001 (0x51)	0xA3	0xA2

SPI TERM

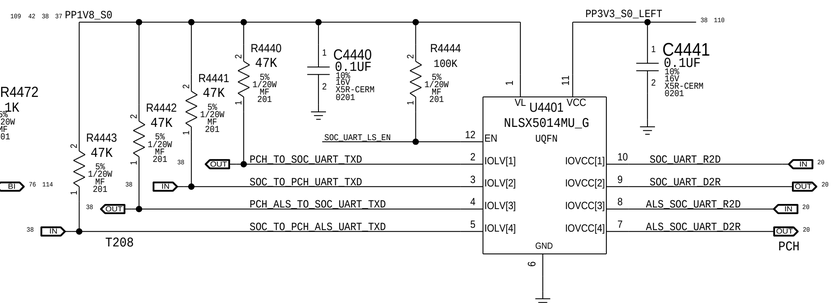


T208 LEVEL SHIFTING

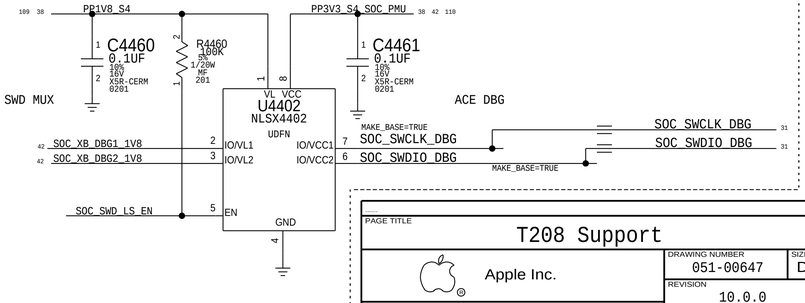
ALS I2C



ALS/DEBUG UART



ACE SWD DBG



PAGE TITLE: T208 Support

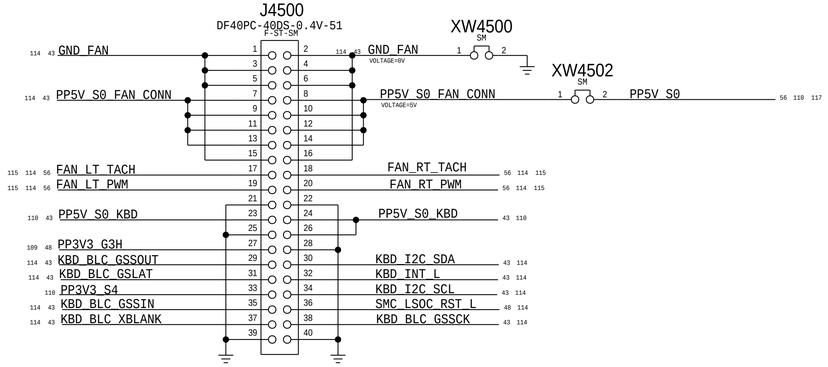
Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 44 OF 145
SHEET: 42 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

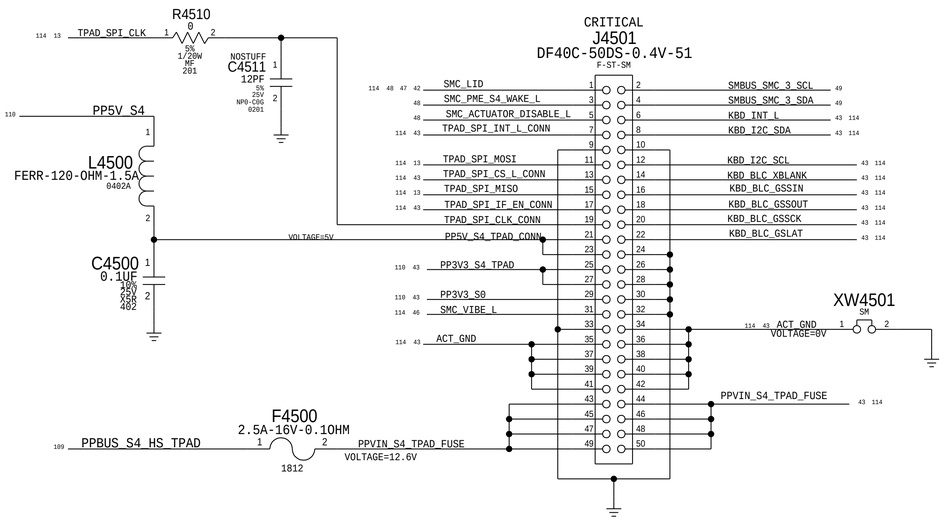
BOM_COST_GROUP=T151

KBD CONNECTOR



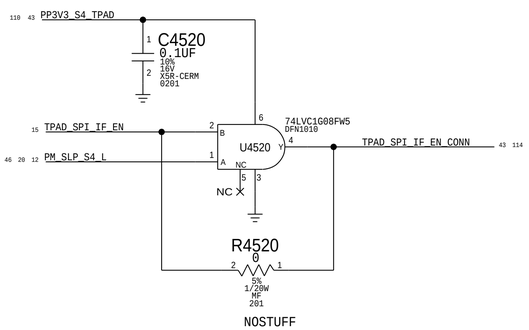
518S00177 (RCPT, 0.3A per pin)
MATE WITH PLUG 516S00054

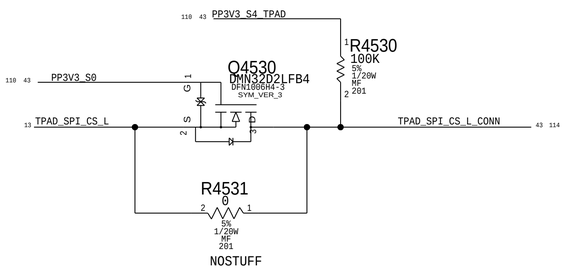
TPAD CONNECTOR

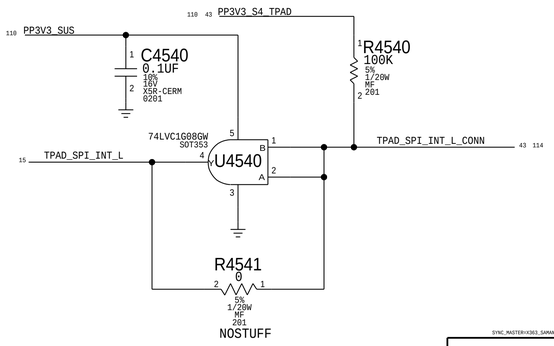


516S00187, MATE WITH 516S00188

TRACKPAD ISOLATION GATES/FET







BOM_COST_GROUP=KEYBOARD

SYNC_MASTER=X383_SAMANTHA
SYNC_DATE=01/08/2018

PAGE TITLE
Connectors&ESD

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 45 OF 145
SHEET 43 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Debug Stuff Was Here

BOM_COST_GROUP=DEBUG

SYNC_MASTER=J68_MLB SYNC_DATE=08/26/2015

PAGE TITLE

External A USB3 Connector

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 47 OF 145

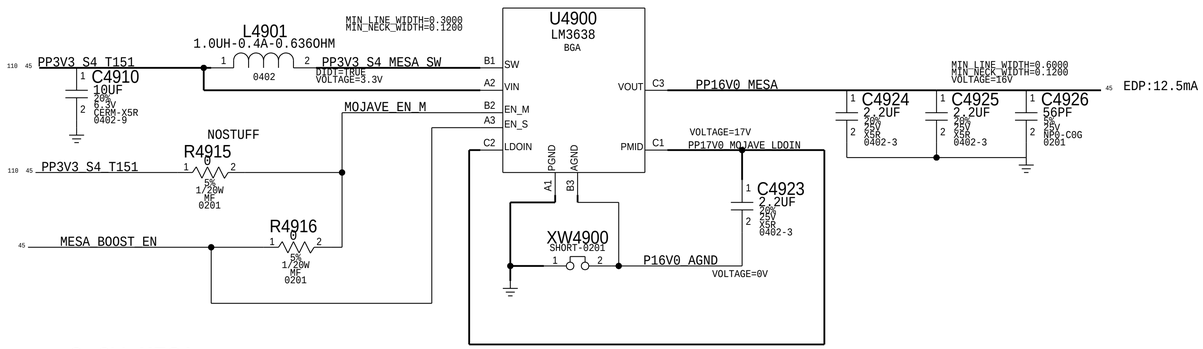
SHEET 44 OF 121

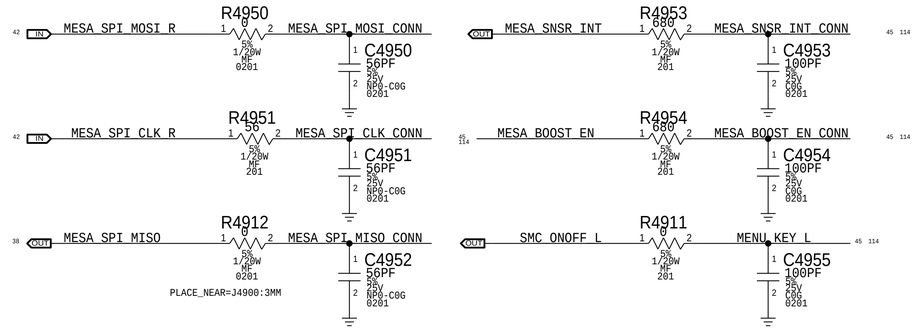
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

ISOLATE FROM OTHER COMPONENTS/NETS AS MUCH AS POSSIBLE

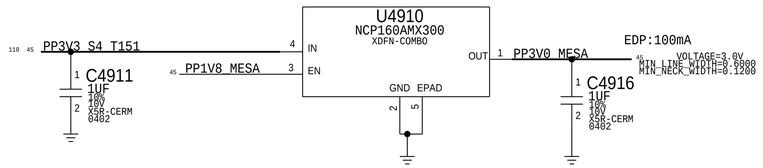
MOJAVE 16V BOOST

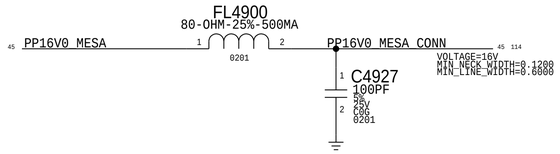




3.0V MESA

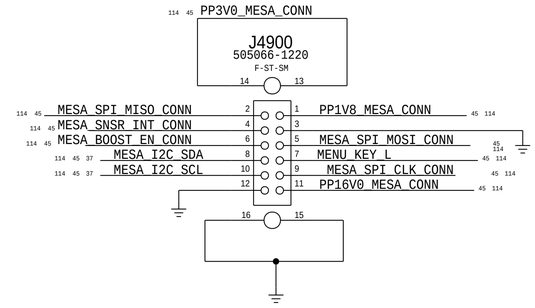
Option to feed LDO from 5V in case of dropout issue

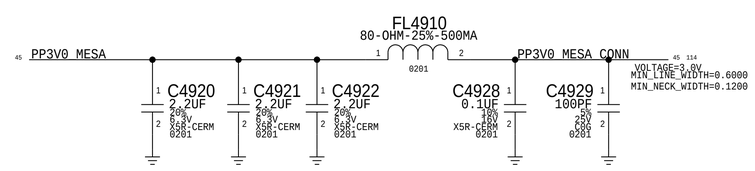




MESA FLEX CONNECTOR

Proto1 Connector for X434/X435 Support
PLUG (516S00115) - X434/ X435 Jumper
Recptacle (516S00203) - X362/X363 MLB

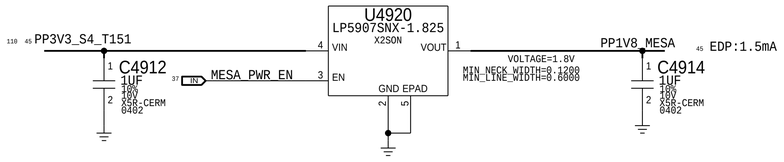


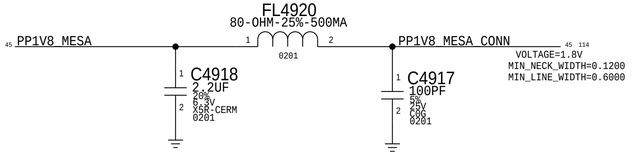


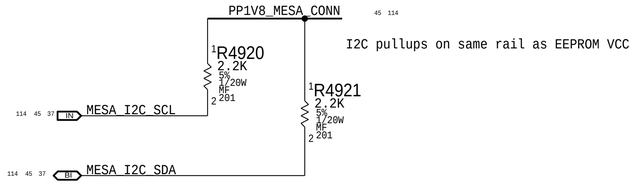
Mesa Power Sequencing Requirements

Power On: 1V8 -> 3V3 -> 16V0

1.8V MESA







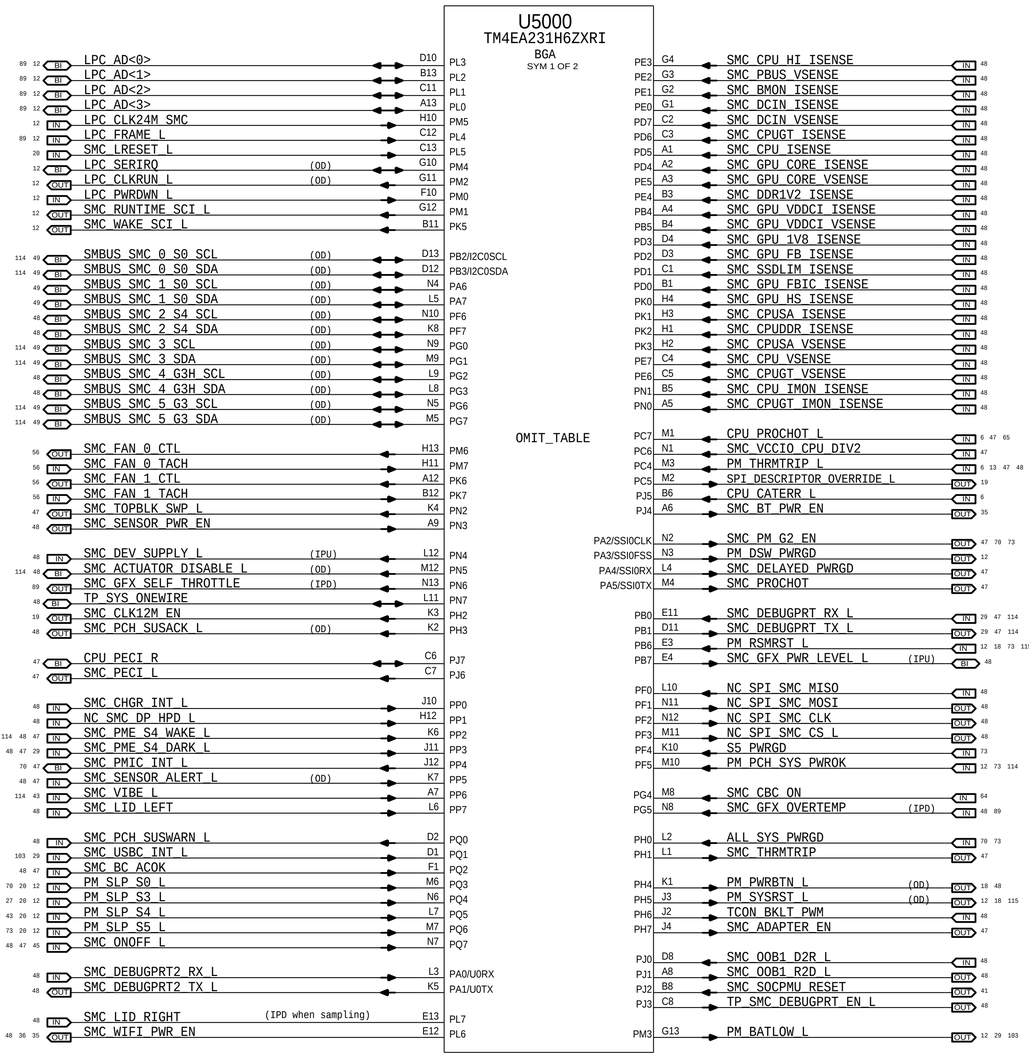
BOM_COST_GROUP=T151

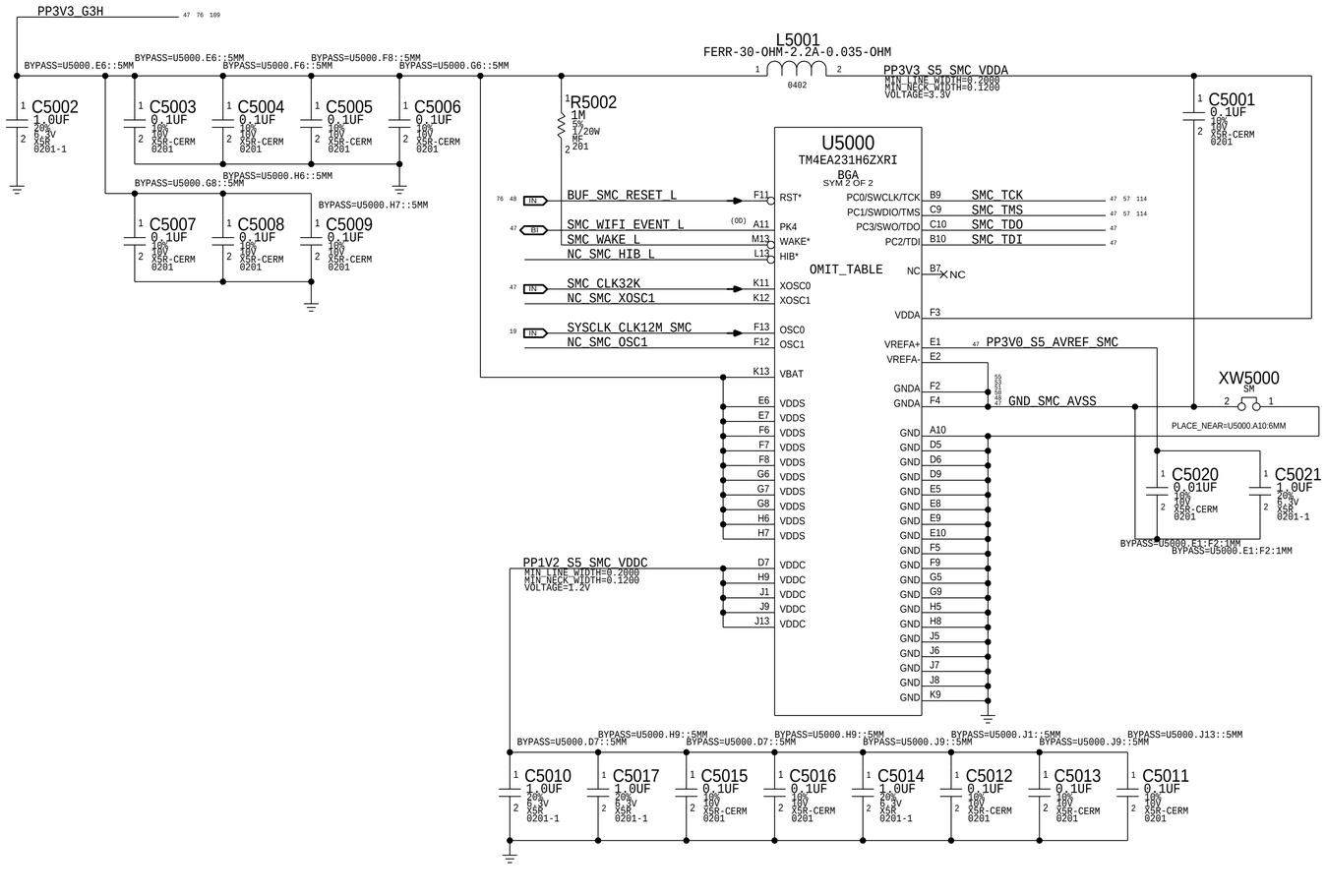
PAGE TITLE
MESA

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 49 OF 145
SHEET 45 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED





NOTE:
SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

NOTE:
Unused pins have "SMC_Pxx" names. Unused
pins designed as outputs can be left floating,
those designated as inputs require pull-ups.

BOM_COST_GROUP=SMC

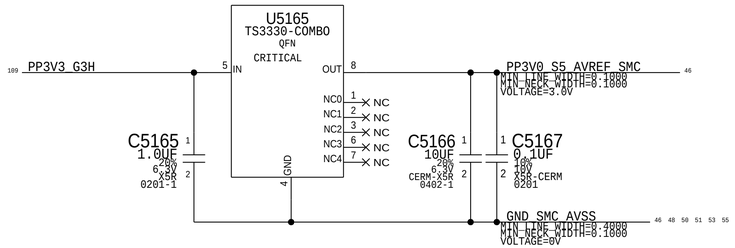
PAGE TITLE: SMC

Apple Inc.

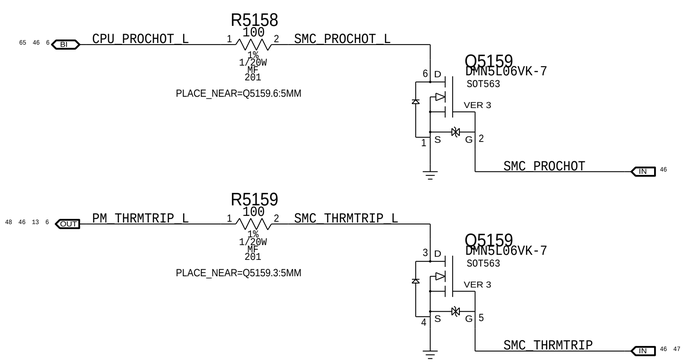
DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 50 OF 145
SHEET: 46 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

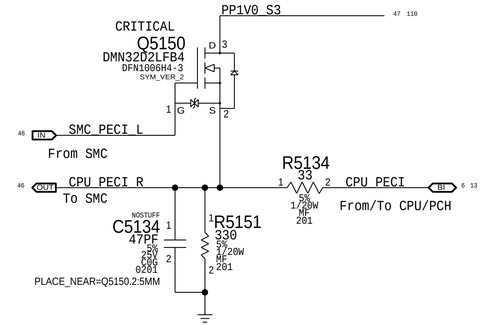
SMC AVREF Supply



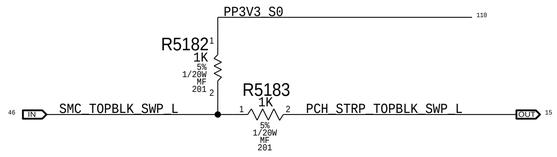
PROCHOT/THRMTRIP Support

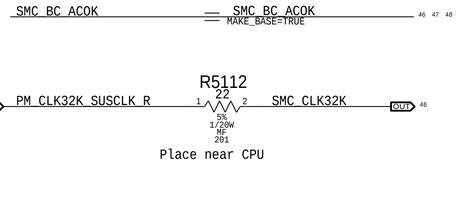


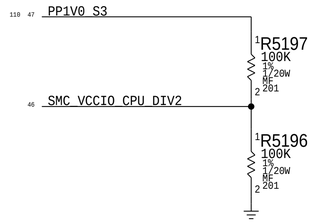
PECI Support

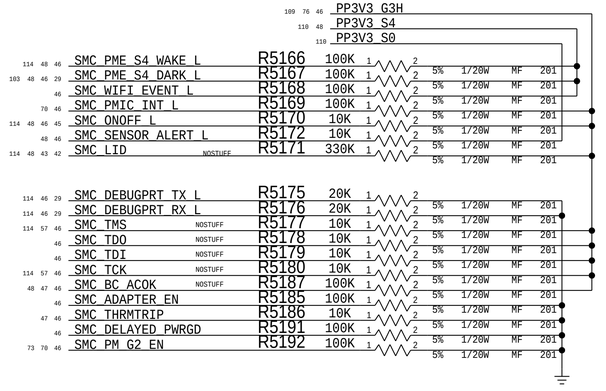


Top-Block Swap









BOM_COST_GROUP=SMC

SYNC_MASTER=J80_ZIFENGSHEN_MLB_BAFFIN SYNC_DATE=11/19/2015

PAGE TITLE: SMC Shared Support

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 51 OF 145
SHEET: 47 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SMC12 ADC Assignments

SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_ISENSE	SMC_CPUGT_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_ISENSE	SMC_GPU_CORE_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_CORE_VSENSE	SMC_GPU_CORE_VSENSE	MAKE_BASE=TRUE	
SMC_DDR1V2_ISENSE	SMC_DDR1V2_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_ISENSE	SMC_GPU_VDDCI_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_VDDCI_VSENSE	SMC_GPU_VDDCI_VSENSE	MAKE_BASE=TRUE	
SMC_GPU_1V8_ISENSE	SMC_GPU_1V8_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FB_ISENSE	SMC_GPU_FB_ISENSE	MAKE_BASE=TRUE	
SMC_SSDLIM_ISENSE	SMC_SSDLIM_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_FBIC_ISENSE	SMC_GPU_FBIC_ISENSE	MAKE_BASE=TRUE	
SMC_GPU_HS_ISENSE	SMC_GPU_HS_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_ISENSE	SMC_CPUSA_ISENSE	MAKE_BASE=TRUE	
SMC_CPUDDR_ISENSE	SMC_CPUDDR_ISENSE	MAKE_BASE=TRUE	
SMC_CPUSA_VSENSE	SMC_CPUSA_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPUGT_VSENSE	SMC_CPUGT_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_IMON_ISENSE	SMC_CPU_IMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPUGT_IMON_ISENSE	SMC_CPUGT_IMON_ISENSE	MAKE_BASE=TRUE	

SMC12 Pin Assignments

SMC_GFX_PWR_LEVEL_L	SMC_GFX_PWR_LEVEL_L	MAKE_BASE=TRUE
TP_SYS_ONEWIRE	TP_SYS_ONEWIRE	MAKE_BASE=TRUE
TP_SMC_DEBUGPRT_EN_L	TP_SMC_DEBUGPRT_EN_L	MAKE_BASE=TRUE
NC_SMC_DP_HPD_L	NC_SMC_DP_HPD_L	MAKE_BASE=TRUE

PM_THRMTRIP_L

CRITICAL
O5290
DMN32D2LFB4
DFN1006H4-3
SYM_VER_2

SMC_GFX_OVERTEMP

NC_SPI_SMC_MISO	NC_SPI_SMC_MISO	TRUE
NC_SPI_SMC_MOSI	NC_SPI_SMC_MOSI	TRUE
NC_SPI_SMC_CLK	NC_SPI_SMC_CLK	TRUE
NC_SPI_SMC_CS_L	NC_SPI_SMC_CS_L	TRUE

SMC_PCH_SUSWARN_L	SMC_PCH_SUSWARN_L	MAKE_BASE=TRUE
SMC_PCH_SUSACK_L	SMC_PCH_SUSACK_L	MAKE_BASE=TRUE
SMC_SENSOR_PWR_EN	SMC_SENSOR_PWR_EN	MAKE_BASE=TRUE
PM_PWRBTN_L	PM_PWRBTN_L	MAKE_BASE=TRUE
SMC_BC_ACOK	SMC_BC_ACOK	
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SCL	SMBUS_SMC_4_G3H_SCL	MAKE_BASE=TRUE
SMBUS_SMC_4_G3H_SDA	SMBUS_SMC_4_G3H_SDA	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SCL	SMBUS_SMC_2_S4_SCL	MAKE_BASE=TRUE
SMBUS_SMC_2_S4_SDA	SMBUS_SMC_2_S4_SDA	MAKE_BASE=TRUE
SMC_OOB1_D2R_L	SMC_OOB1_D2R_L	MAKE_BASE=TRUE
SMC_OOB1_R2D_L	SMC_OOB1_R2D_L	MAKE_BASE=TRUE
SMC_ACTUATOR_DISABLE_L	SMC_ACTUATOR_DISABLE_L	MAKE_BASE=TRUE
SMC_CHGR_INT_L	SMC_CHGR_INT_L	MAKE_BASE=TRUE

Debug Power "Buttons"

PLACE_SIDE=TOP
SILK_PART=PWR_BTN
R5226
RES
0603-NSP
BOMOPTION=OMIT

SMC_ONOFF_L

SW5200
EVQPUA02K

BOMOPTION=DBG_BTN
SILK_PART=PWR_BTN
PLACE_SIDE=BOTTOM

Debug RESET "Buttons"

BOMOPTION=DBG_BTN
PLACE_SIDE=BOTTOM
SILK_PART=RESET_BTN
CRITICAL
SW5227
SOX-152HNT
SM

SMC_RESET_L

Thermal Alerts

NOSTUFF

SMC_CPUHI_COMP_ALERT_L	R5217 100	
CPUTHMSNS_THM_L	R5216 100	CPUTHRM_THRM:SMC
CPUTHMSNS_ALERT_L	R5214 100	CPUTHRM_ALRT:SMC
TBTTHMSNS_X_THM_L	R5220 100	TBTTHRM_THRM:SMC
TBTTHMSNS_T_THM_L	R5221 100	TBTTHRM_THRM:SMC
TBTTHMSNS_X_ALERT_L	R5210 100	TBTTHRM_ALRT:SMC
TBTTHMSNS_T_ALERT_L	R5211 100	TBTTHRM_ALRT:SMC

All: 5% 1/20W MF 201

SMC_SENSOR_ALERT_L

BYPASS=U5256.5::5MM
PP3V3_G3H

R5256 100K 5% 1/20W MF 201
C5256 0.1UF 10% 10V X5R-CERM 0201

SMC_LSOC_RST_L
SMC_ONOFF_L

U5256
SN74LVC1G02
SOT553-5
CRITICAL

SMC_4FINGERS_RST

S4 SMC Wake Sources

SMC_PME_S4_WAKE_L
SMC_PME_S4_DARK_L

R5258 0 5% 1/20W MF 201
LID_FEATURE_ON

PP3V3_G3H
BYPASS=U5255.6::5MM
C5255 0.1UF 10% 10V X5R-CERM 0201

U5255
74LVC1G32
SOT891
CRITICAL

SMC_LID_LEFT_R
SMC_LID_RIGHT

R5255 10K 5% 1/20W MF 201

R5257 0 5% 1/20W MF 201
LID_FEATURE_OFF

SMC_LID_LEFT
SMC_LID

R5259 0 5% 1/20W MF 201
SMC_DEV_SUPPLY_L
SMC_DEV_SUPPLY_R_L

R5260 10 5% 1/20W MF 201
TCON_BKLT_PWM
BKLT_PWM_TCON2MLB

C5257 3300PF 10% 16V X7R-CERM 0201
NOSTUFF

BUF_SMC_RESET_L

NOSTUFF
C5270 1000PF 10% 16V X7R-CERM 0201

GND_SMC_AVSS

BOM_COST_GROUP=SMC

Hall Effect Pads - Left

J5250
AMR-MLB-X502
SM
OMIT_TABLE

HALL_SENSOR_LEFT
PP3V3_G3H

C5250 1000PF 10% 16V X7R-1 0201
NOSTUFF

R5252 10K 5% 1/20W MF 201
SMC_LID_LEFT_R

Hall Effect Pads - Right

J5260
AMR-MLB-X502
SM
OMIT_TABLE

HALL_SENSOR_RIGHT
PP3V3_G3H

C5260 1000PF 10% 16V X7R-1 0201
NOSTUFF

R5253 10K 5% 1/20W MF 201
SMC_LID_RIGHT

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
CPUTHRM:BOTH	CPUTHRM_THRM:SMC,CPUTHRM_ALRT:SMC
CPUTHRM:THRM	CPUTHRM_THRM:SMC
CPUTHRM:ALRT	CPUTHRM_ALRT:SMC

Specify one of these BOM GROUPS.

BOM GROUP	BOM OPTIONS
TBTTHRM:BOTH	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:SMC
TBTTHRM:THRM	TBTTHRM_THRM:SMC,TBTTHRM_ALRT:PU
TBTTHRM:ALRT	TBTTHRM_THRM:PU,TBTTHRM_ALRT:SMC
TBTTHRM:NONE	TBTTHRM_THRM:PU,TBTTHRM_ALRT:PU

PP3V3_S4

R5274 100K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM
NOSTUFF

R5273 10K 5% 1/20W MF 201

R5275 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_TX_L
WLAN_UART_RX

PLACE_SIDE=BOTTOM
NOSTUFF
R5276 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_RX_L
WLAN_UART_TX

PP3V3_G3H

R5280 100K 5% 1/20W MF 201
PLACE_SIDE=BOTTOM

R5281 10K 5% 1/20W MF 201

R5277 0 5% 1/20W MF 0201
SMC_DEBUGPRT2_R_TX

R5278 0 5% 1/20W MF 0201
PLACE_SIDE=BOTTOM
SMC_DEBUGPRT2_R_RX

TP-P6 TP5200
TP-P6 TP5201

SMC_WIFI_PWR_EN
SMC_SENSOR_PWR_EN

R5295 10K 5% 1/20W MF 201
NOSTUFF

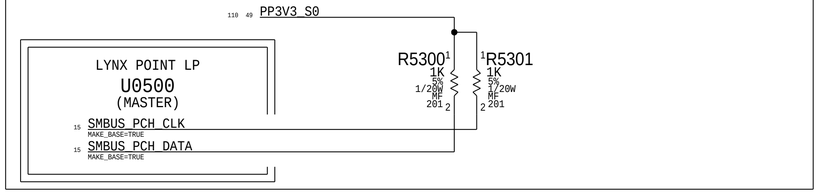
R5294 10K 5% 1/20W MF 201
NOSTUFF

PAGE TITLE	SMC Project Support
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	52 OF 145
SHEET	48 OF 121

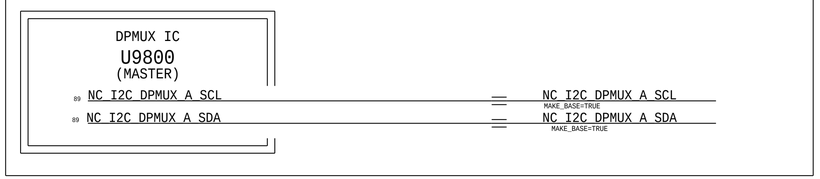
Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

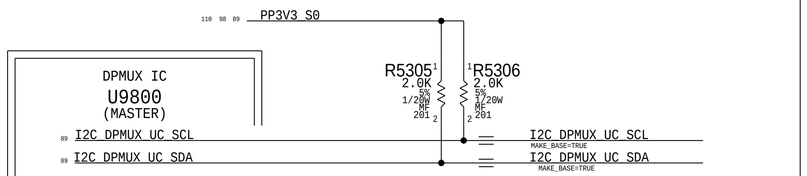
LYNX POINT LP S0 "SMBus 0" Connections



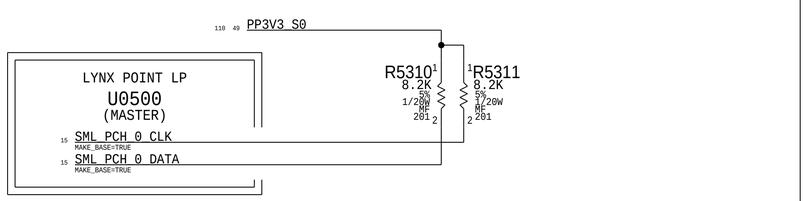
DPMUX Connections



DPMUX Connections



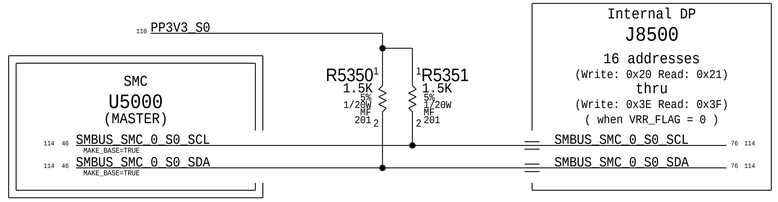
LYNX POINT LP S0 "SMLink 0" Connections



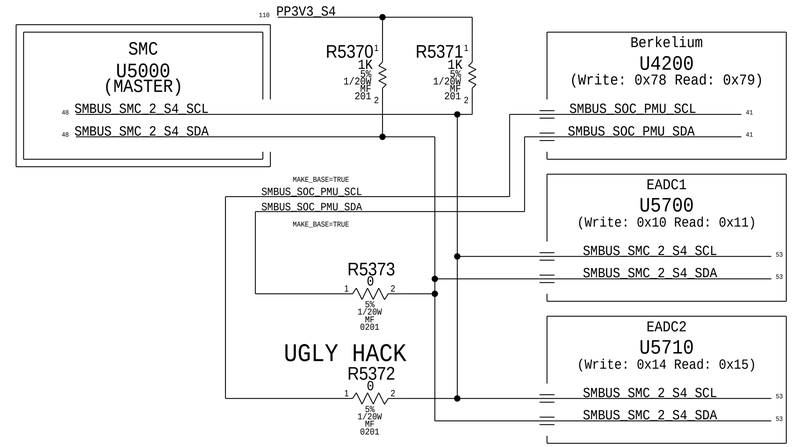
LYNX POINT LP S0 "SMLink 1" Connections

SMLink 1 is slave port to
access PCH.

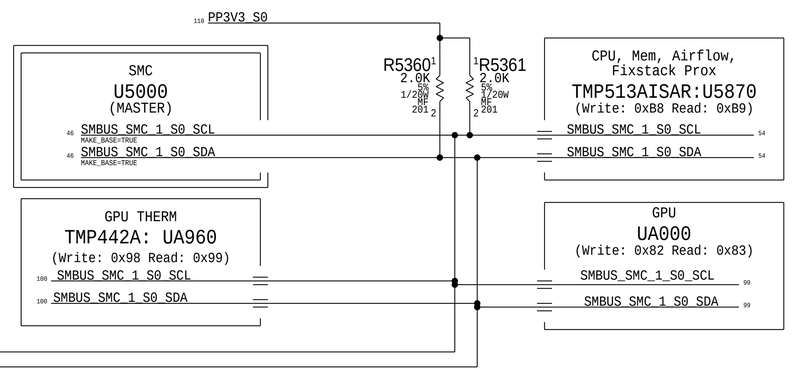
SMC SMBus "0" S0 Connections



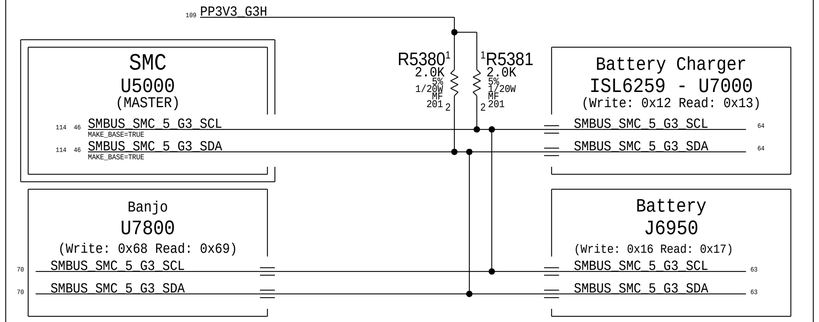
SMC SMBus "2" S4 Connections



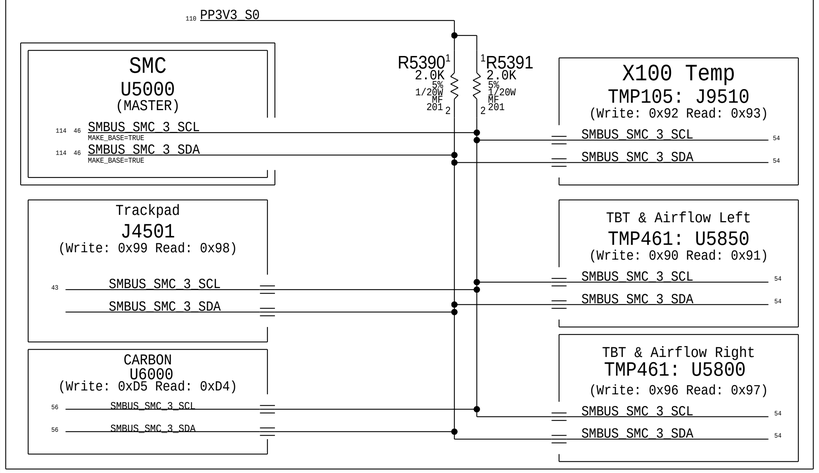
SMC SMBus "1" S0 Connections



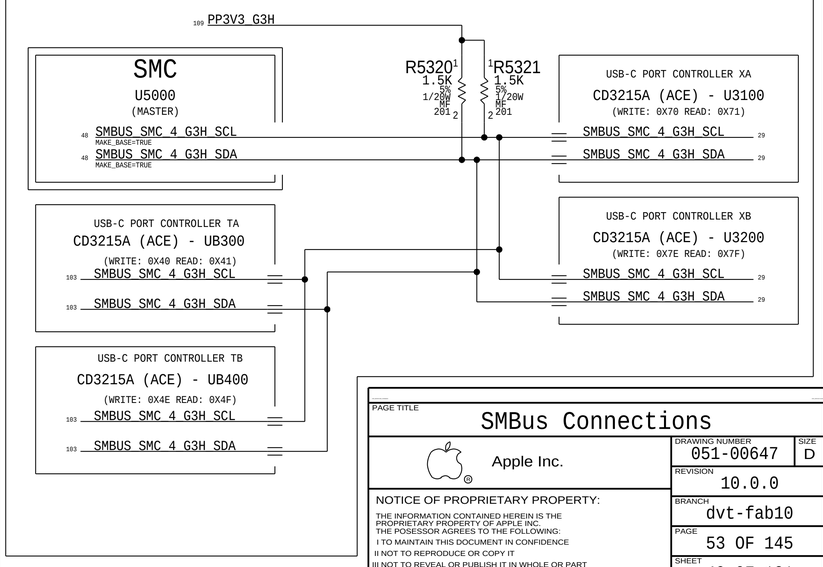
SMC SMBus "5" G3H Connections



SMC SMBus "3" S0 Connections



SMC SMBUS "4" G3H CONNECTIONS



BOM_COST_GROUP=SMC

PAGE TITLE

SMBus Connections

Apple Inc.

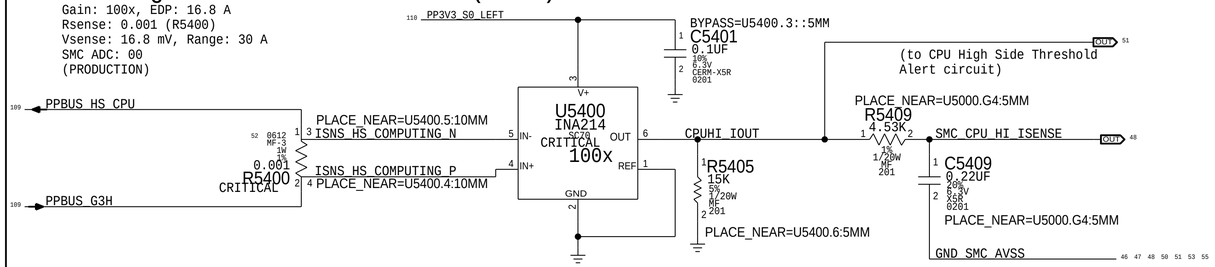
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 53 OF 145
SHEET 49 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

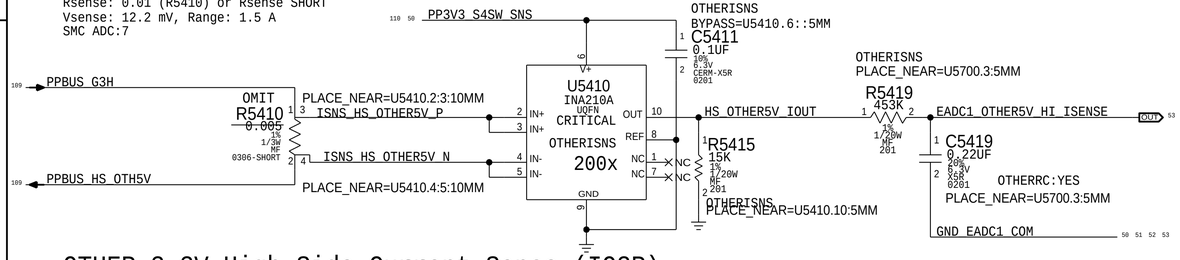
CPU High Side Current Sense (IC0R)

Gain: 100x, EDP: 16.8 A
Rsense: 0.001 (R5400)
Vsense: 16.8 mV, Range: 30 A
SMC ADC: 00
(PRODUCTION)



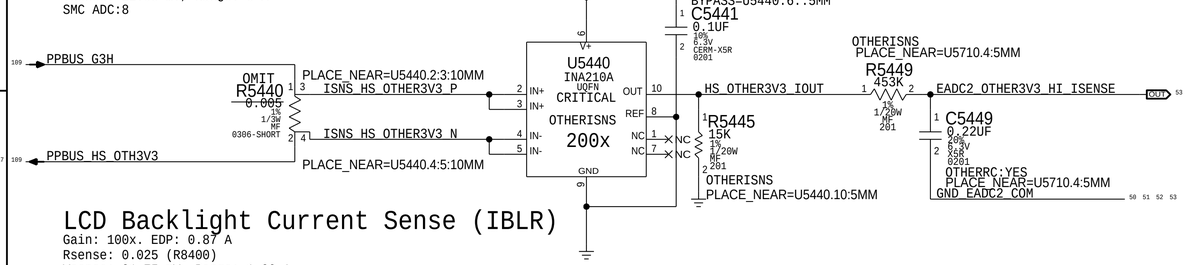
OTHER 5V High Side Current Sense (IO5R)

Gain: 200x, EDP: 1.22 A
Rsense: 0.01 (R5410) or Rsense SHORT
Vsense: 12.2 mV, Range: 1.5 A
SMC ADC:7



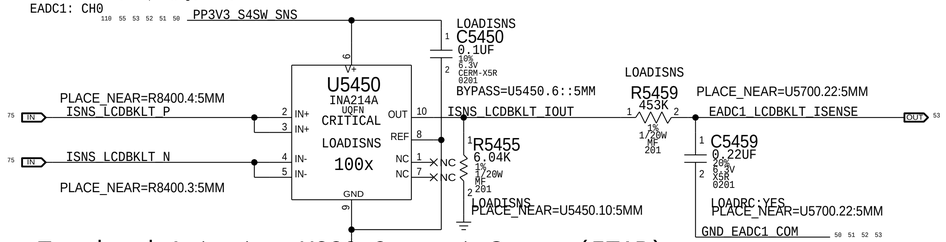
OTHER 3.3V High Side Current Sense (IO3R)

Gain: 200x, EDP: 4.31 A
Rsense: 0.003 (R5440) or Rsense SHORT
Vsense: 12.93 mV, Range: 5 A
SMC ADC:8



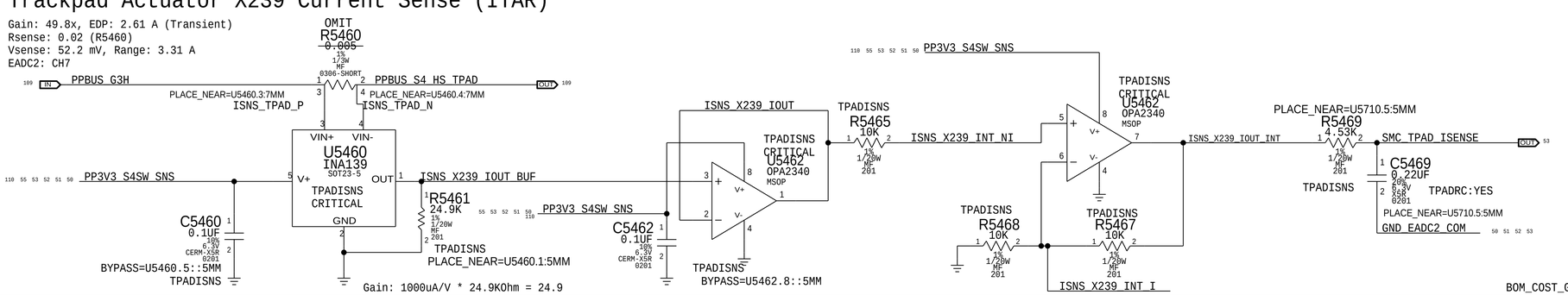
LCD Backlight Current Sense (IBLR)

Gain: 100x. EDP: 0.87 A
Rsense: 0.025 (R8400)
Vsense: 21.75 mV, Range: 1.32 A
EADC1: CH0



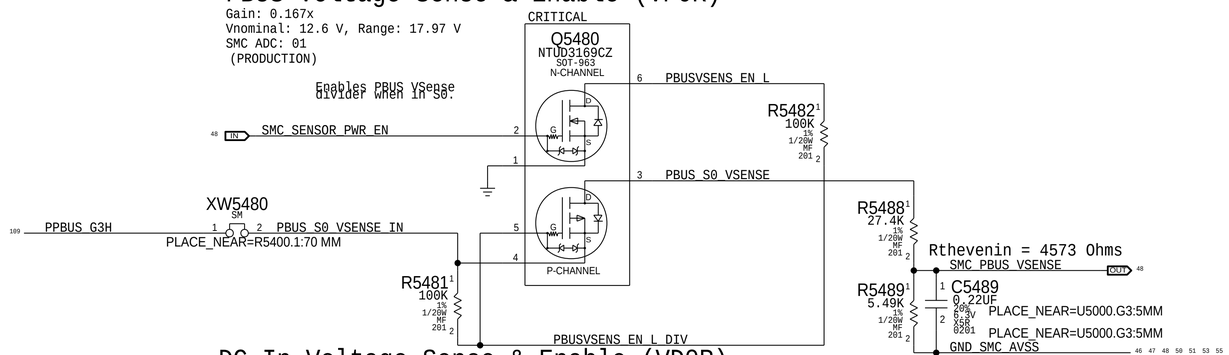
Trackpad Actuator X239 Current Sense (ITAR)

Gain: 49.8x, EDP: 2.61 A (Transient)
Rsense: 0.02 (R5460)
Vsense: 52.2 mV, Range: 3.31 A
EADC2: CH7



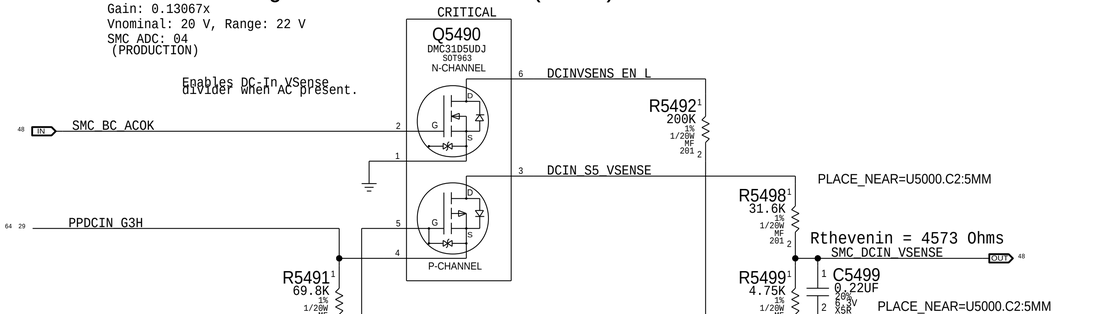
PBUS Voltage Sense & Enable (VP0R)

Gain: 0.167x
Vnominal: 12.6 V, Range: 17.97 V
SMC ADC: 01
(PRODUCTION)



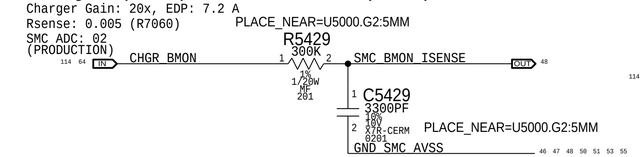
DC In Voltage Sense & Enable (VD0R)

Gain: 0.13067x
Vnominal: 20 V, Range: 22 V
SMC ADC: 04
(PRODUCTION)



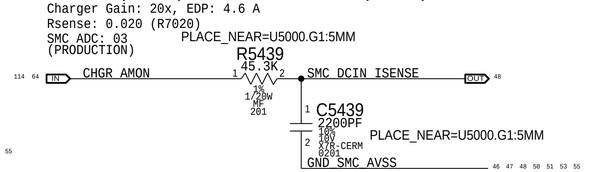
Charger (BMON) Current Sense (IPBR)

Charger Gain: 20x, EDP: 7.2 A
Rsense: 0.005 (R7060)
SMC ADC: 02
(PRODUCTION)



DC-IN (AMON) Current Sense (ID0R)

Charger Gain: 20x, EDP: 4.6 A
Rsense: 0.020 (R7020)
SMC ADC: 03
(PRODUCTION)



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	2	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5419,C5449		OTHERRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5459		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5469		TPADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: High Side

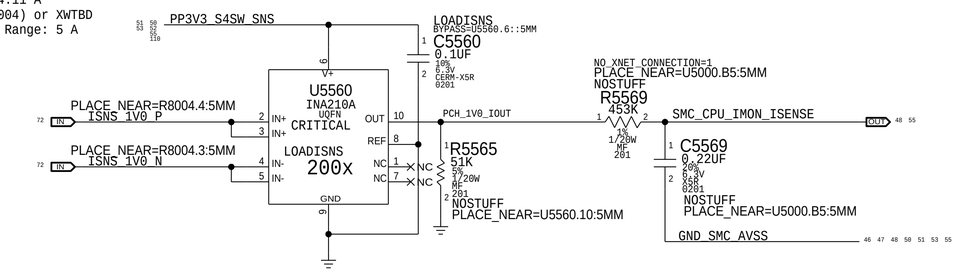
Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 54 OF 145
SHEET: 50 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

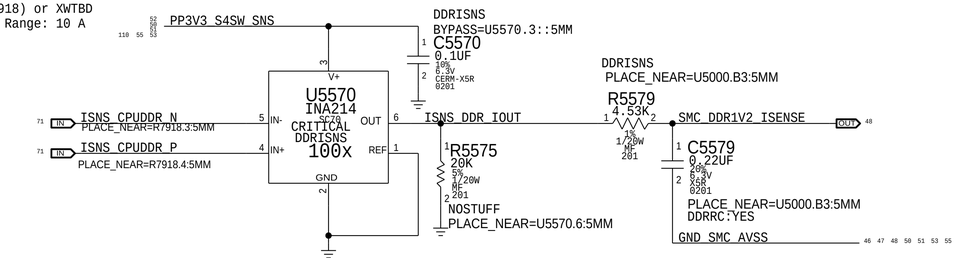
PCH 1.0V Current Sense (ISCC)

Gain: 200x, EDP: 4.11 A
Rsense: 0.003 (R8004) or XWTBD
Vsense: 11.33 mV, Range: 5 A
SMC ADC: 22



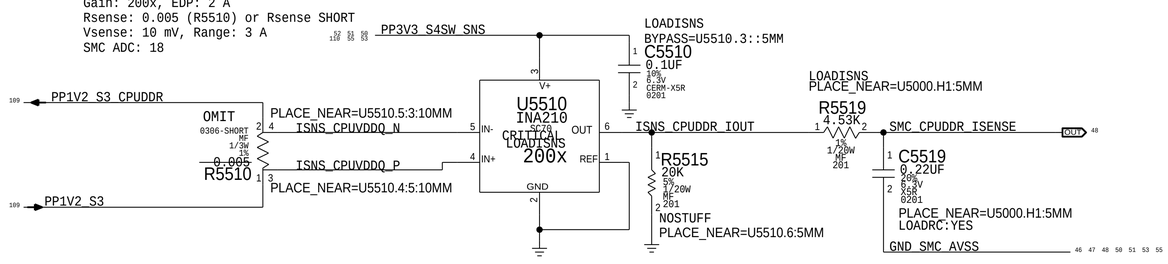
DDR 1.2V S3 (CPU & Memory) Current Sense (IM0C)

Gain: 100x, EDP: 9.01 A
Rsense: 0.003 (R7918) or XWTBD
Vsense: 27.03 mV, Range: 10 A
SMC ADC: 09



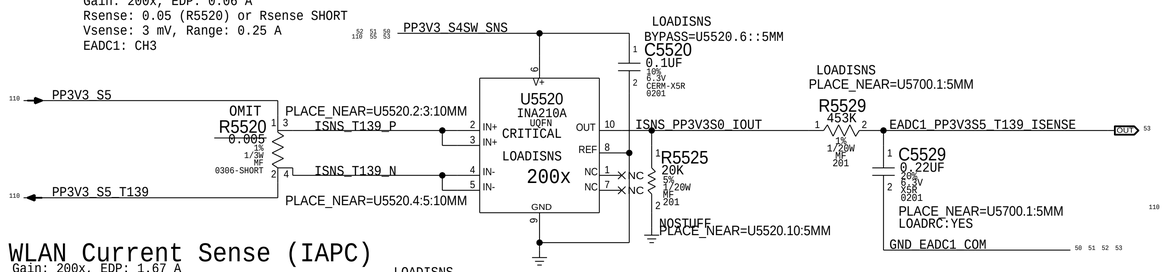
CPU DDR 1.2V S3 (CPU Only) Current Sense (IMCC)

Gain: 200x, EDP: 2 A
Rsense: 0.005 (R5510) or Rsense SHORT
Vsense: 10 mV, Range: 3 A
SMC ADC: 18



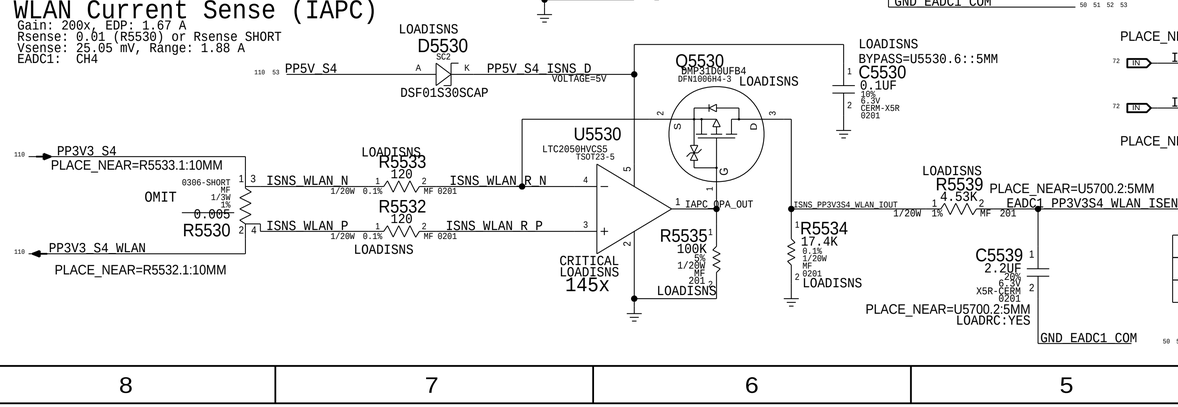
T139 Current Sense (IF3C)

Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5520) or Rsense SHORT
Vsense: 3 mV, Range: 0.25 A
EADC1: CH3



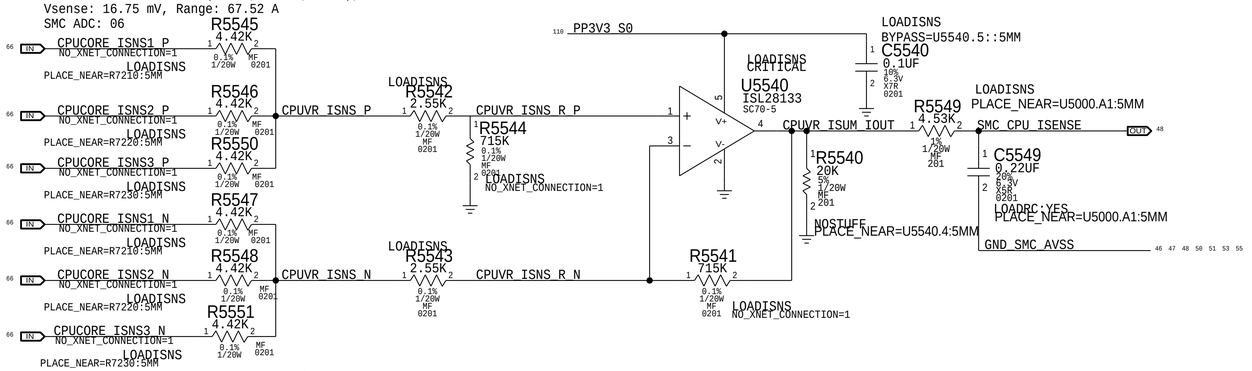
WLAN Current Sense (IAPC)

Gain: 200x, EDP: 1.67 A
Rsense: 0.01 (R5530) or Rsense SHORT
Vsense: 25.05 mV, Range: 1.88 A
EADC1: CH4



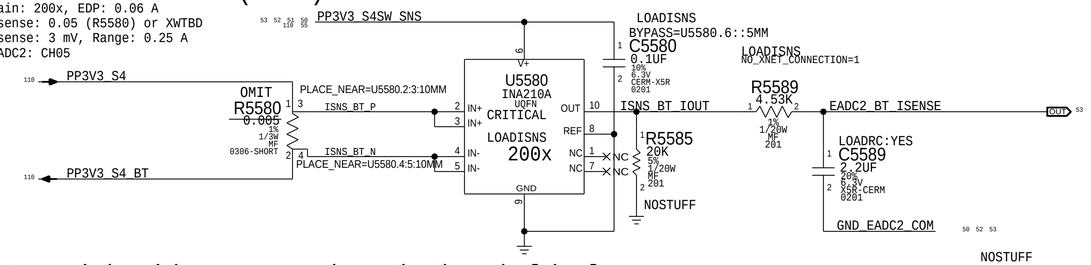
CPU Fixed Current Sense (ICAC)

Gain: 177.71x, EDP: 67 A
Rsense: 3x of 0.00075 (R7210, R7220,R7230), Rsum: 0.00025
Vsense: 16.75 mV, Range: 67.52 A
SMC ADC: 06



BT Current Sense (IBTC)

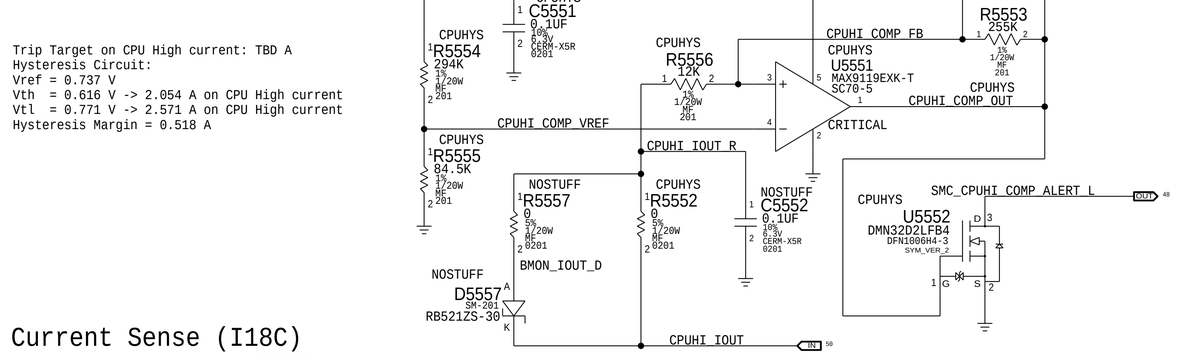
Gain: 200x, EDP: 0.06 A
Rsense: 0.05 (R5580) or XWTBD
Vsense: 3 mV, Range: 0.25 A
EADC2: CH05



CPU High Side Current (IC0R) Threshold Alert

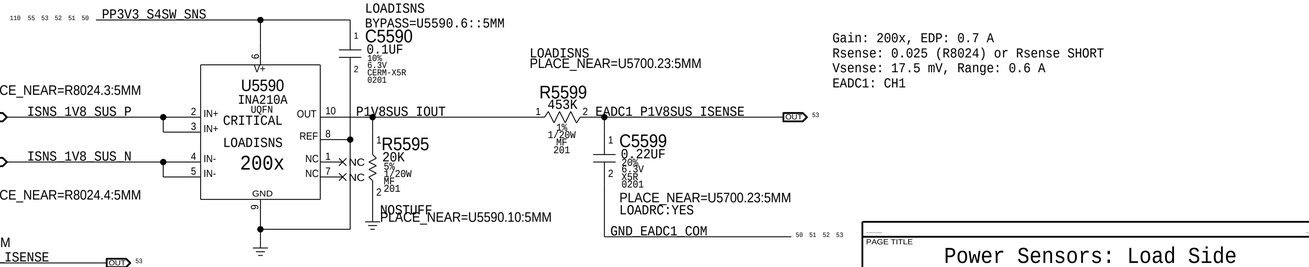
Gain: 100x
Rsense: 0.001 (R5400)

Trip Target on CPU High current: TBD A
Hysteresis Circuit:
Vref = 0.737 V
Vth = 0.616 V -> 2.054 A on CPU High current
Vtl = 0.771 V -> 2.571 A on CPU High current
Hysteresis Margin = 0.518 A



1.8V Current Sense (I18C)

Gain: 200x, EDP: 0.7 A
Rsense: 0.025 (R8024) or Rsense SHORT
Vsense: 17.5 mV, Range: 0.6 A
EADC1: CH1



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	6	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5519,C5529,C5539,C5549,C5589,C5599		LOADRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5579		DDRRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Load Side

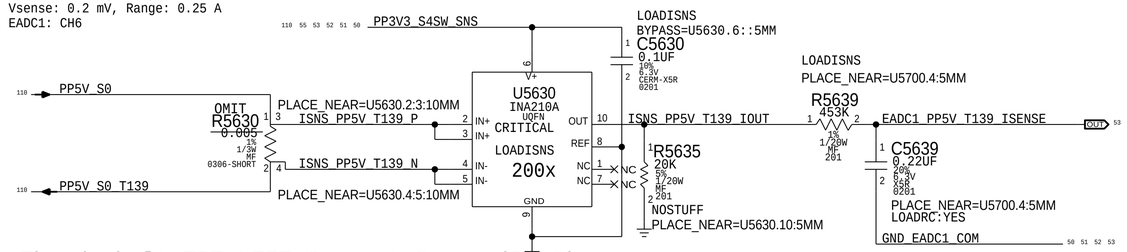
Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 55 OF 145
SHEET: 51 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

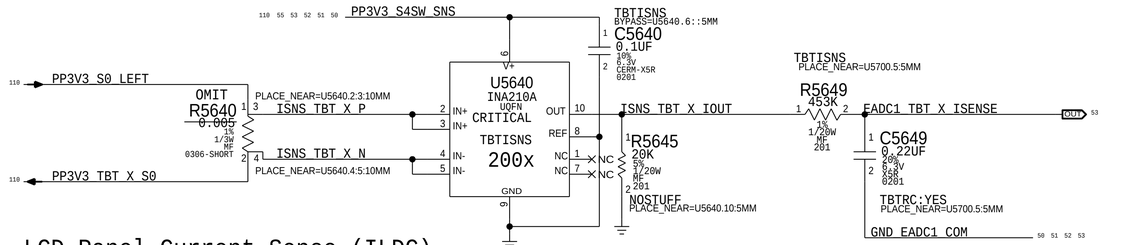
T139 5V Current Sense (IF5C)

Gain: 200x, EDP: 0.004 A
Rsense: 0.05 (R5630) or Rsense SHORT
Vsense: 0.2 mV, Range: 0.25 A
EADC1: CH6



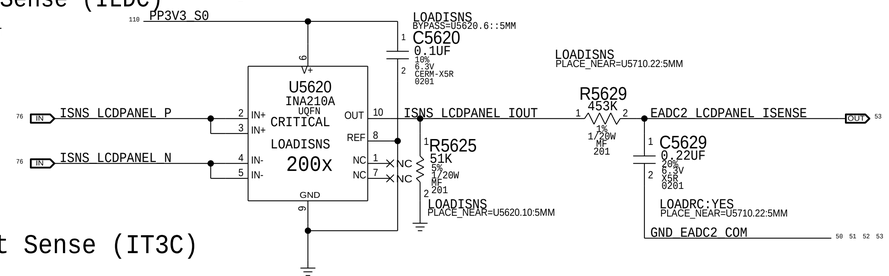
Thunderbolt TBT LEFT Current Sense (IULC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5640) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH7



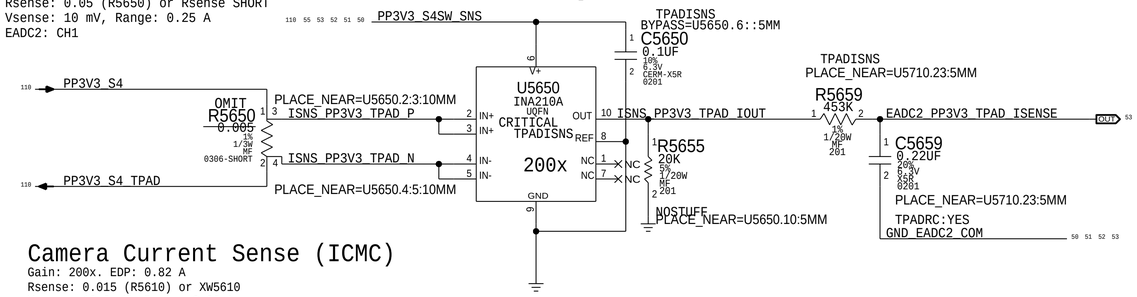
LCD Panel Current Sense (ILDC)

Gain: 200x. EDP: 1 A
RSENSE: 0.01 (R8520) or Rsense SHORT
Vsense: 5 mV, Range: 1.25 A
EADC2: CH0



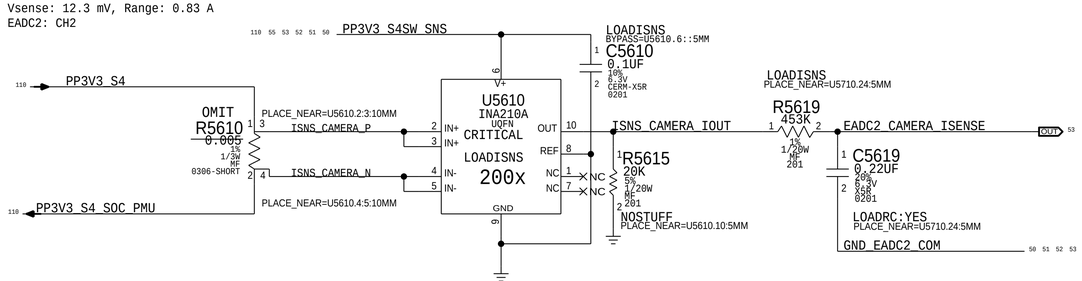
Trackpad 3V Current Sense (IT3C)

Gain: 200x, EDP: 0.2 A
Rsense: 0.05 (R5650) or Rsense SHORT
Vsense: 10 mV, Range: 0.25 A
EADC2: CH1

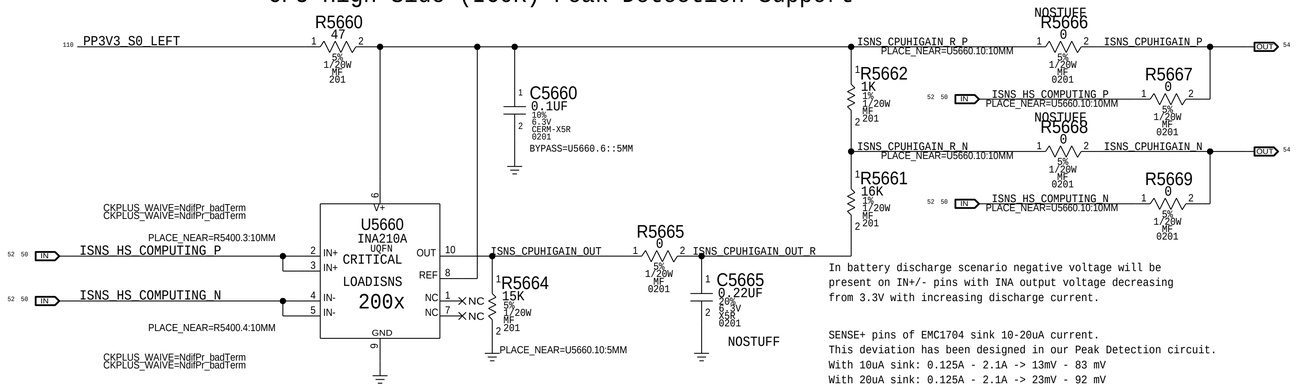


Camera Current Sense (ICMC)

Gain: 200x. EDP: 0.82 A
Rsense: 0.015 (R5610) or XW5610
Vsense: 12.3 mV, Range: 0.83 A
EADC2: CH2



CPU High Side (IC0R) Peak Detection Support

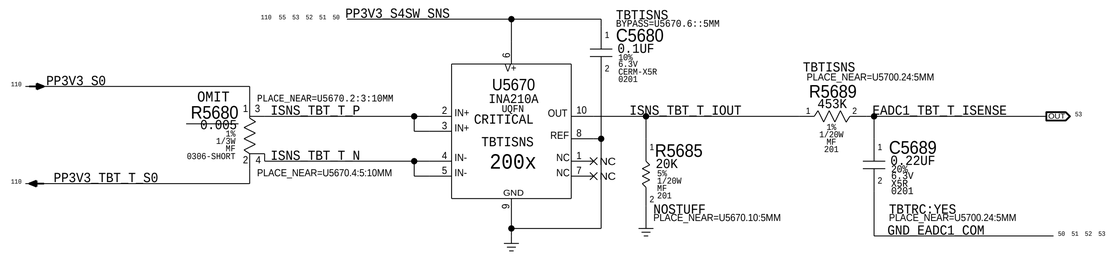


In battery discharge scenario negative voltage will be present on IN+/- pins with INA output voltage decreasing from 3.3V with increasing discharge current.

SENSE+ pins of EMC1704 sink 10-20uA current.
This deviation has been designed in our Peak Detection circuit.
With 10uA sink: 0.125A - 2.1A -> 13mV - 83 mV
With 20uA sink: 0.125A - 2.1A -> 23mV - 92 mV

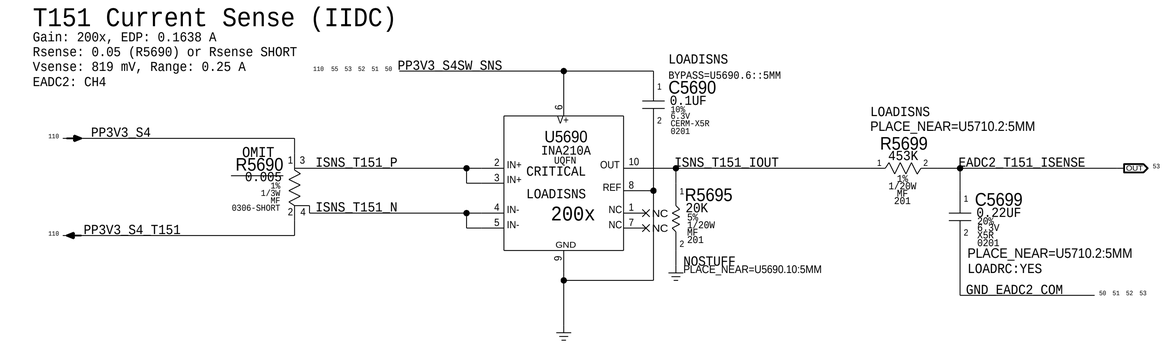
Thunderbolt TBT RIGHT Current Sense (IURC)

Gain: 200x. EDP: 0.5 A
Rsense: 0.025 (R5680) or Rsense SHORT
Vsense: 12.5 mV, Range: 0.5 A
EADC1: CH2



T151 Current Sense (IIDC)

Gain: 200x, EDP: 0.1638 A
Rsense: 0.05 (R5690) or Rsense SHORT
Vsense: 819 mV, Range: 0.25 A
EADC2: CH4



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5619,C5629,C5639,C5699		LOADRC:NO
117S0008	2	RES,MTL FILM,100K,1/16W,0201,SMD,LF	C5649,C5689		TBTRC:NO
117S0008	1	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5659		TPADRC:NO

BOM_COST_GROUP=SENSORS

PAGE TITLE: Power Sensors: Extended

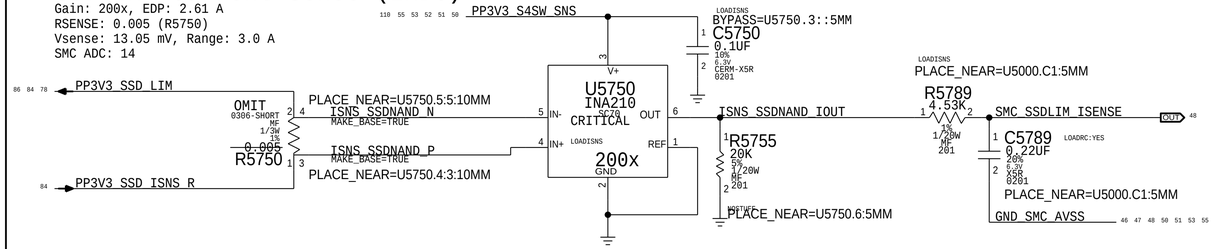
Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 56 OF 145
SHEET: 52 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

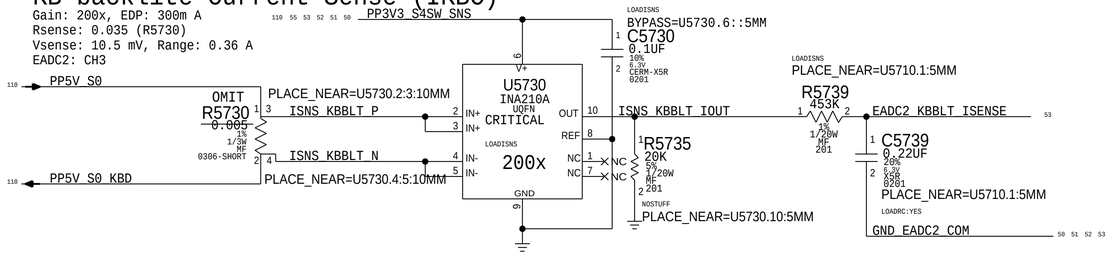
SSDLIM Current Sense (IHDC)

Gain: 200x, EDP: 2.61 A
RSENSE: 0.005 (R5750)
Vsense: 13.05 mV, Range: 3.0 A
SMC ADC: 14



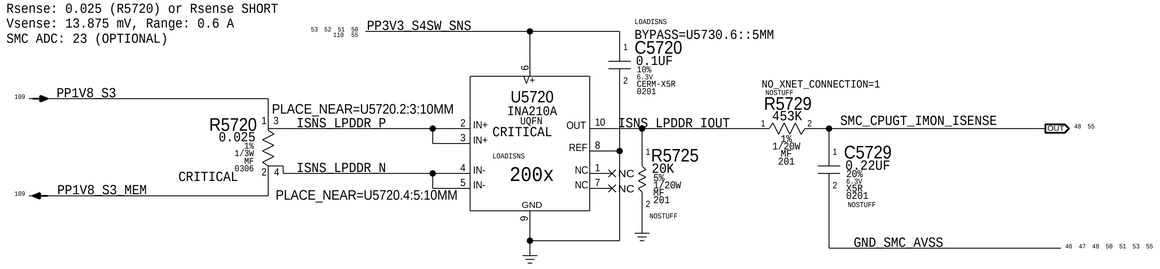
KB backlite Current Sense (IKBC)

Gain: 200x, EDP: 300m A
Rsense: 0.035 (R5730)
Vsense: 10.5 mV, Range: 0.36 A
EADC2: CH3



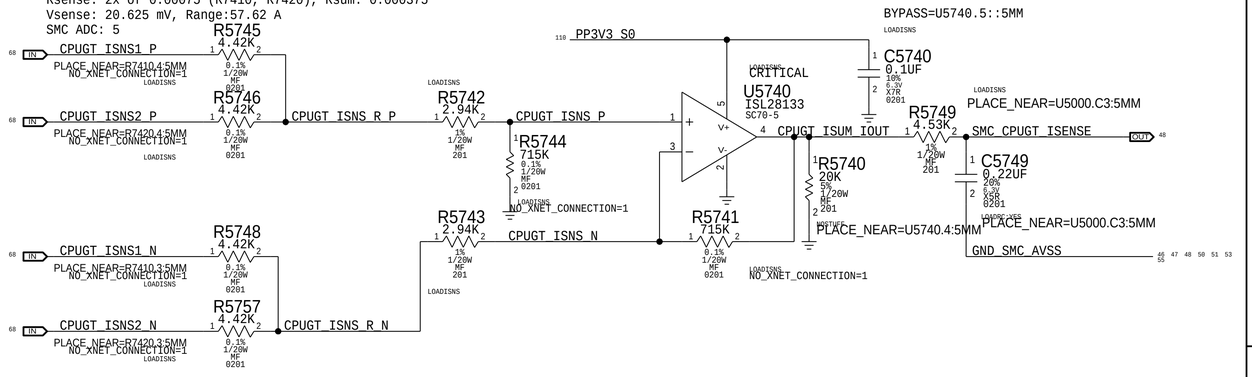
LPDDR 1.8V Current Sense (IM1C)

Gain: 200x, EDP: 0.555 A
Rsense: 0.025 (R5720) or Rsense SHORT
Vsense: 13.875 mV, Range: 0.6 A
SMC ADC: 23 (OPTIONAL)



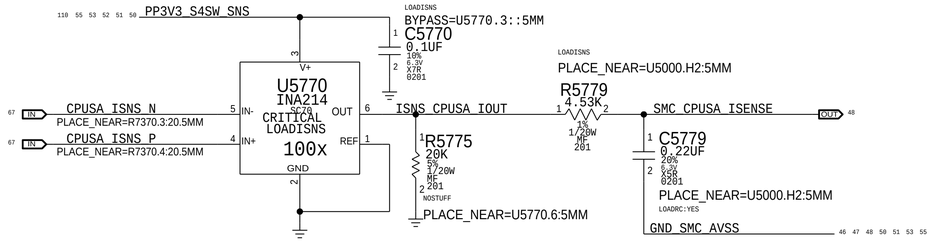
CPU GT Current Sense (ICTC)

Gain: 202.93x, EDP: 55 A
Rsense: 2x of 0.00075 (R7410, R7420), Rsum: 0.000375
Vsense: 20.625 mV, Range:57.62 A
SMC ADC: 5



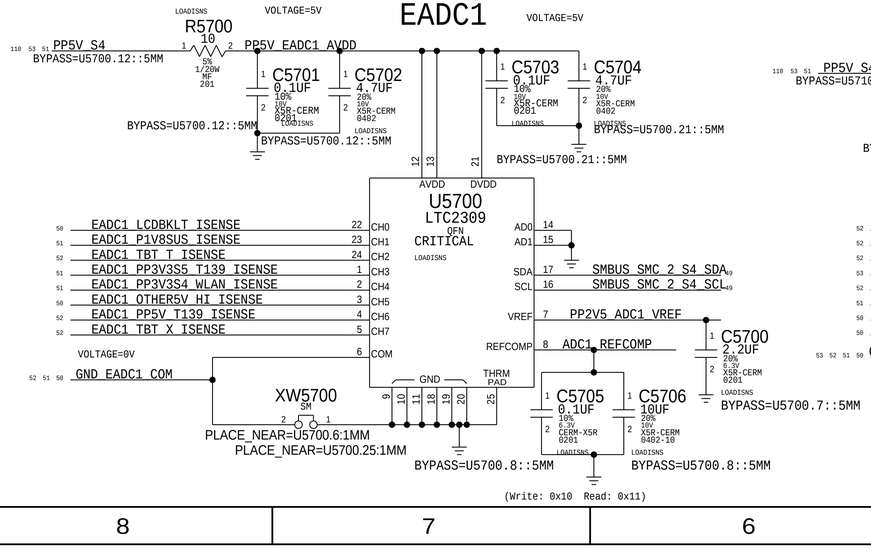
CPU SA Current Sense (ICSC)

Gain: 200x, EDP: 8 A
Rsense: 0.002 (R7570)
Vsense: 16 mV, Range: 7.5 A
SMC ADC: 17



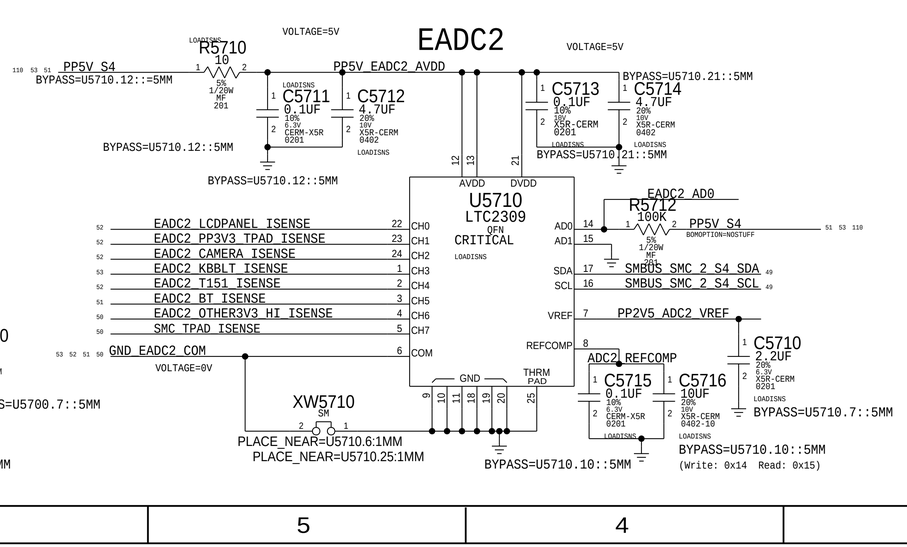
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	4	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5739,C5749,C5779,C5789		LOADRC:NO

EADC1



(Write: 0x10 Read: 0x11)

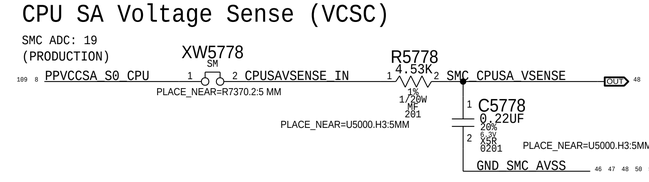
EADC2



(Write: 0x14 Read: 0x15)

CPU SA Voltage Sense (VCSC)

SMC ADC: 19
(PRODUCTION)



PAGE TITLE
Power Sensors: Extended 2

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 57 OF 145
SHEET 53 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

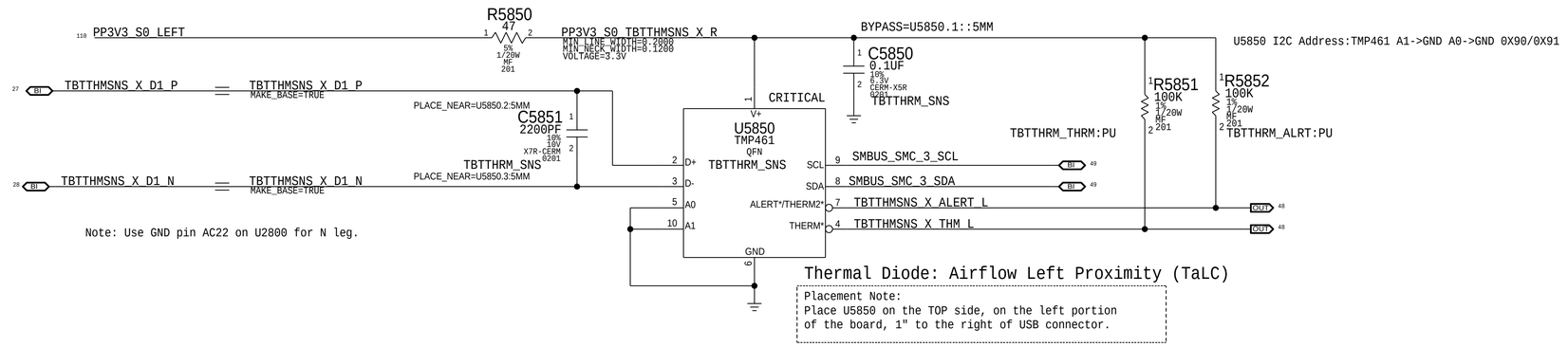
BOM_COST_GROUP=SENSORS

Thermal Sensor A:
Thunderbolt Die, Airflow Left

I2C Write: 0xD8, I2C Read: 0xD9

Thermal Diode: TBT Die (TTLD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.



Thermal Diode: Airflow Left Proximity (TaLC)

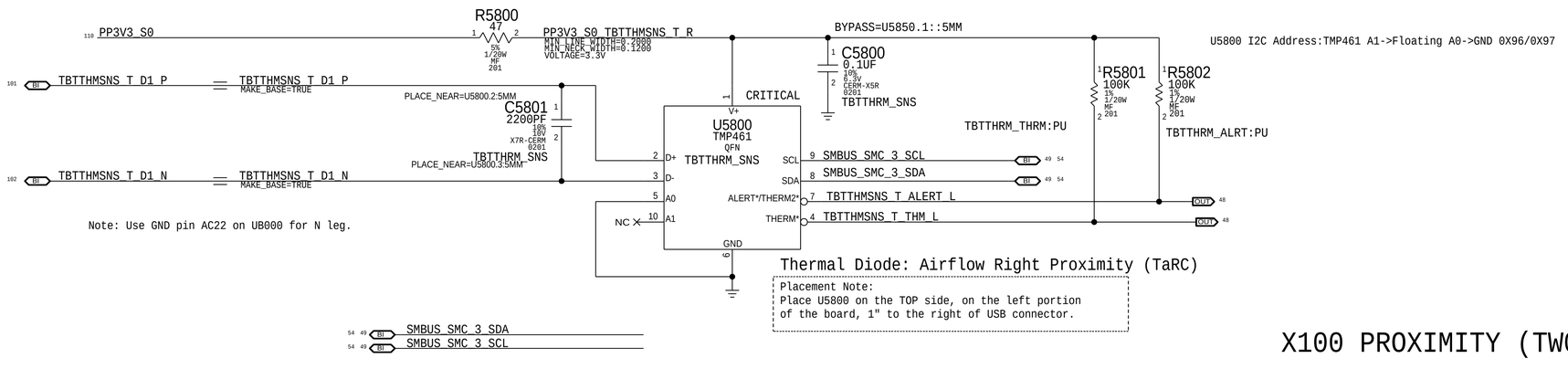
Placement Note:
Place U5850 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor C:
Thunderbolt Die, Air Flow Right

I2C Write: 0x98, I2C Read: 0x99

Thermal Diode: TBT Die (TTRD)

Placement Note:
The P leg connects to THERMDA pin of the TBT chip, the N leg connect to pin AC22.

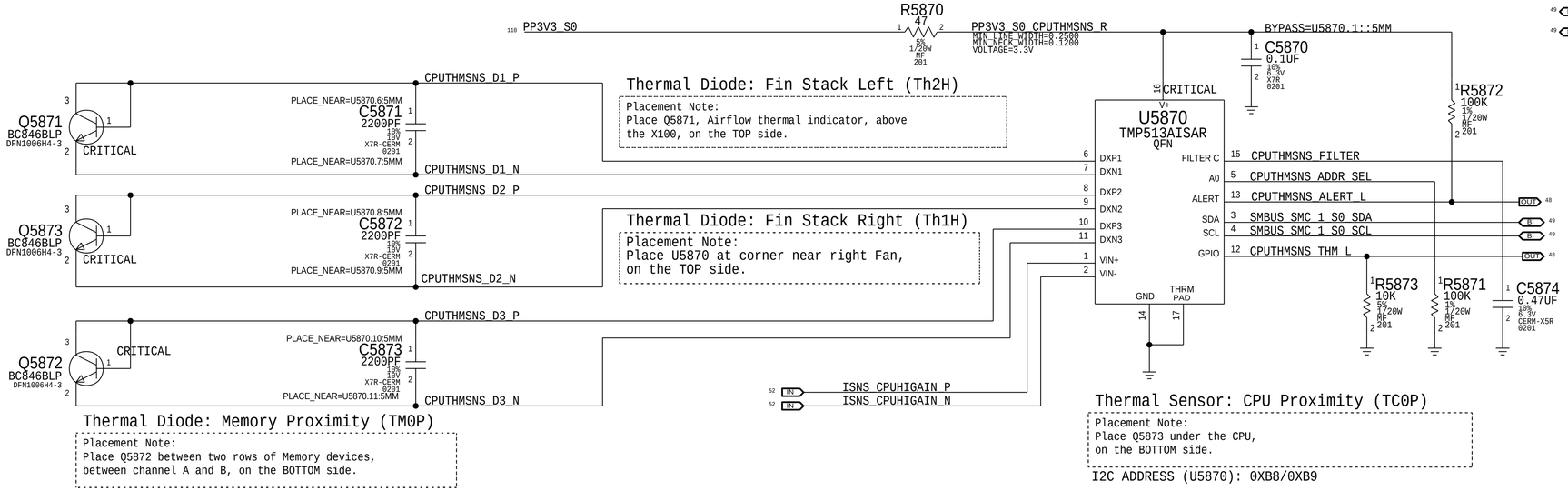


Thermal Diode: Airflow Right Proximity (TaRC)

Placement Note:
Place U5800 on the TOP side, on the left portion of the board, 1" to the right of USB connector.

Thermal Sensor B & CPU High Peak Detection:
CPU Proximity, Memory Proximity, Fin Stack Left, Fin Stack Right

I2C Write: 0x98, I2C Read: 0x99



Thermal Diode: Fin Stack Left (Th2H)

Placement Note:
Place Q5871, Airflow thermal indicator, above the X100, on the TOP side.

Thermal Diode: Fin Stack Right (Th1H)

Placement Note:
Place U5870 at corner near right Fan, on the TOP side.

Thermal Diode: Memory Proximity (TM0P)

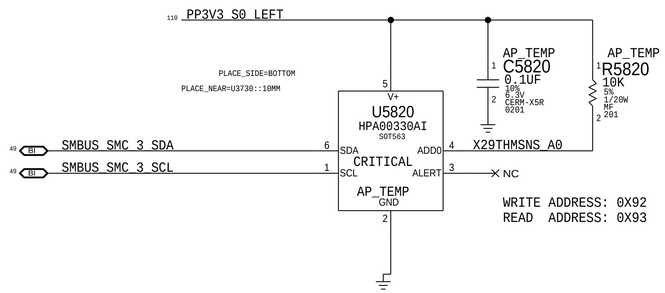
Placement Note:
Place Q5872 between two rows of Memory devices, between channel A and B, on the BOTTOM side.

Thermal Sensor: CPU Proximity (TC0P)

Placement Note:
Place Q5873 under the CPU, on the BOTTOM side.

I2C ADDRESS (U5870): 0XB8/0XB9

X100 PROXIMITY (TW0P)



Placement note:
PLACE U5820 ON BOTTOM NEAR X100

BOM_COST_GROUP=SENSORS

PAGE TITLE
Thermal Sensors

Apple Inc.

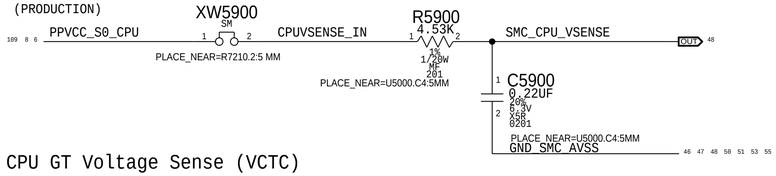
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 58 OF 145
SHEET 54 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SENSORS: EXTENDER 3

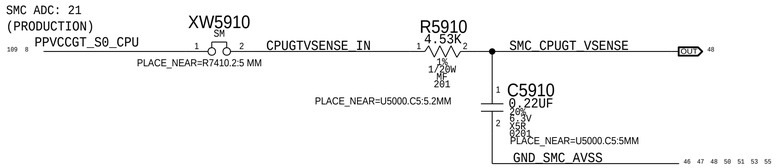
CPU Core Voltage Sense (VCAC)

SMC ADC: 20
(PRODUCTION)



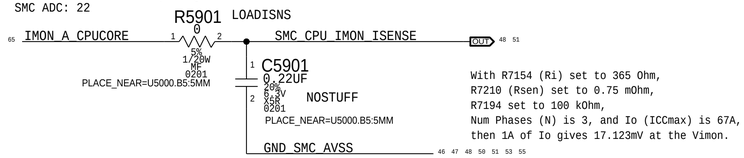
CPU GT Voltage Sense (VCTC)

SMC ADC: 21
(PRODUCTION)



CPU Core IMON Current Sense (ICAM)

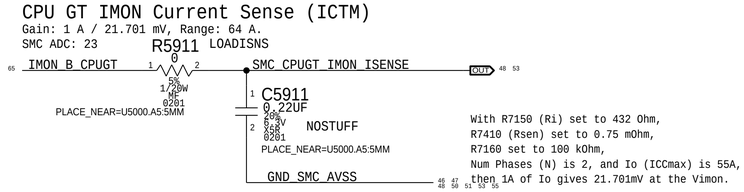
Gain: 1 A / 17.123 mV, Range: 67 A.
SMC ADC: 22



With R7154 (Ri) set to 365 Ohm,
R7210 (Rsen) set to 0.75 mOhm,
R7194 set to 100 kOhm,
Num Phases (N) is 3, and Io (ICCmax) is 67A,
then 1A of Io gives 17.123mV at the Vimon.

CPU GT IMON Current Sense (ICTM)

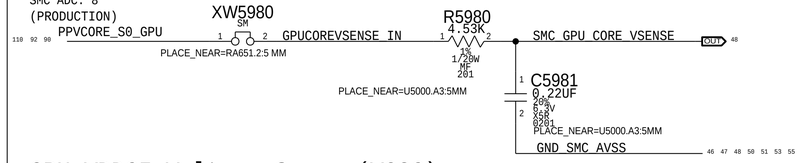
Gain: 1 A / 21.701 mV, Range: 64 A.
SMC ADC: 23



With R7150 (Ri) set to 432 Ohm,
R7410 (Rsen) set to 0.75 mOhm,
R7160 set to 100 kOhm,
Num Phases (N) is 2, and Io (ICCmax) is 55A,
then 1A of Io gives 21.701mV at the Vimon.

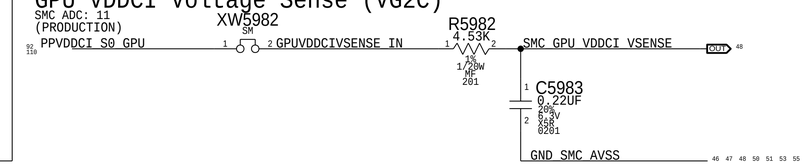
GPU CORE Voltage Sense (VG0C)

SMC ADC: 8
(PRODUCTION)



GPU VDDCI Voltage Sense (VG2C)

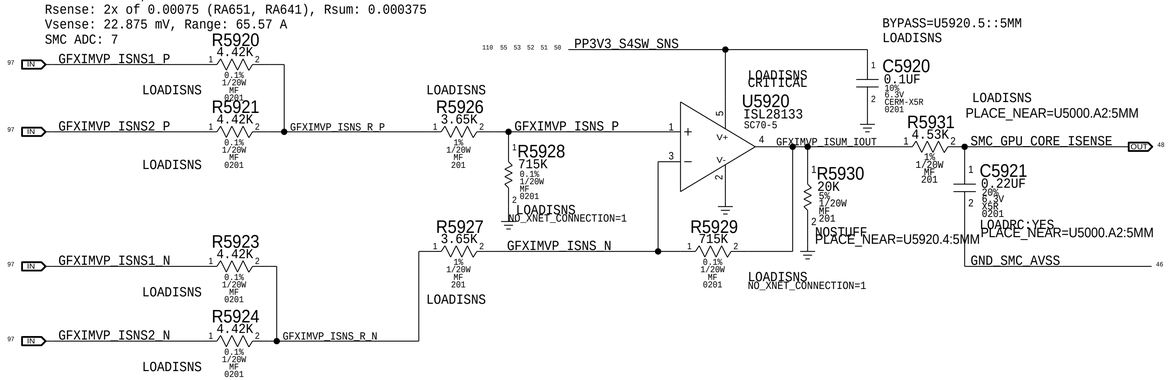
SMC ADC: 11
(PRODUCTION)



GPU SENSORS

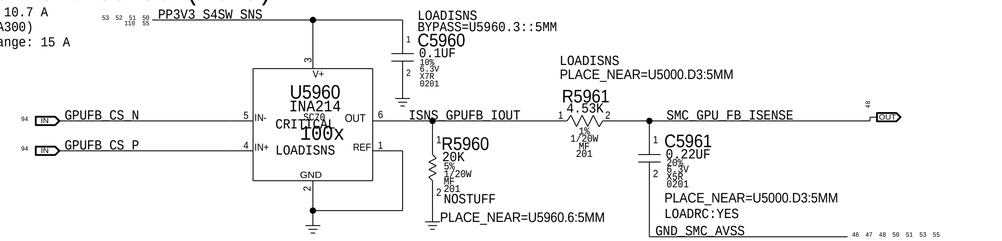
GPU CORE Current Sense (IG0C)

Gain: 122.01x, EDP: 64.2 A
Rsense: 2x of 0.00075 (RA651, RA641), Rsum: 0.000375
Vsense: 22.875 mV, Range: 65.57 A
SMC ADC: 7



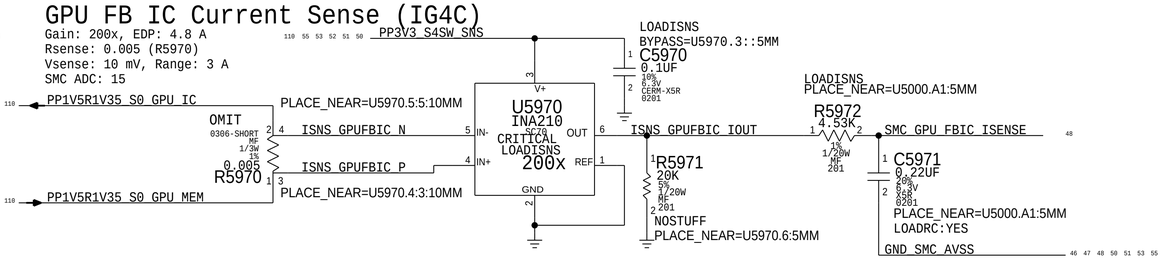
GPU FB Current Sense (IG1C)

Gain: 100x, EDP: 10.7 A
Rsense: 0.002 (RA300)
Vsense: 16 mV, Range: 15 A
SMC ADC: 13



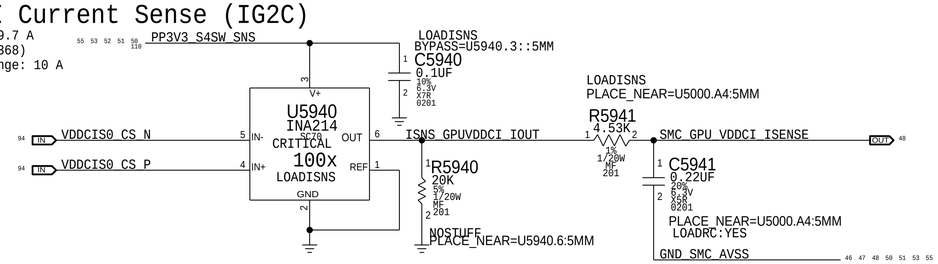
GPU FB IC Current Sense (IG4C)

Gain: 200x, EDP: 4.8 A
Rsense: 0.005 (R5970)
Vsense: 10 mV, Range: 3 A
SMC ADC: 15



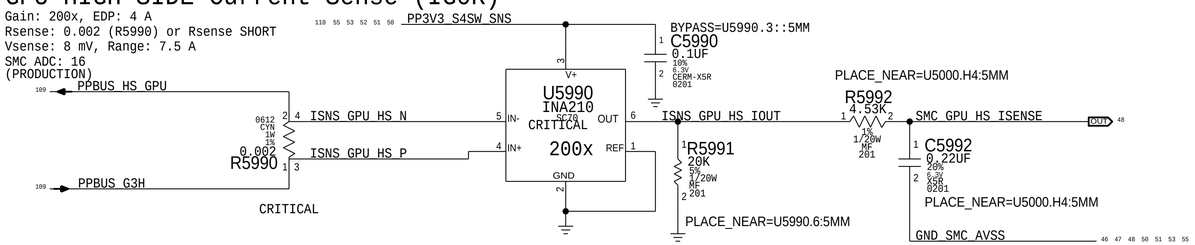
GPU VDDCI Current Sense (IG2C)

Gain: 100x, EDP: 9.7 A
Rsense: 0.003 (RA368)
Vsense: 24 mV, Range: 10 A
SMC ADC: 10



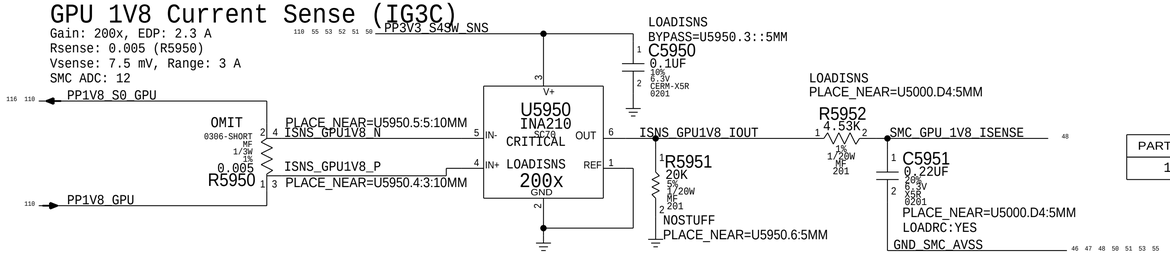
GPU HIGH SIDE Current Sense (IG0R)

Gain: 200x, EDP: 4 A
Rsense: 0.002 (R5990) or Rsense SHORT
Vsense: 8 mV, Range: 7.5 A
SMC ADC: 16
(PRODUCTION)



GPU 1V8 Current Sense (IG3C)

Gain: 200x, EDP: 2.3 A
Rsense: 0.005 (R5950)
Vsense: 7.5 mV, Range: 3 A
SMC ADC: 12



BOM_COST_GROUP=SENSORS

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0008	5	RES,MTL FLIM,100K,1/16W,0201,SMD,LF	C5921,C5941,C5951,C5961,C5971		LOADRC:NO

PAGE TITLE
Sensor Extended 3

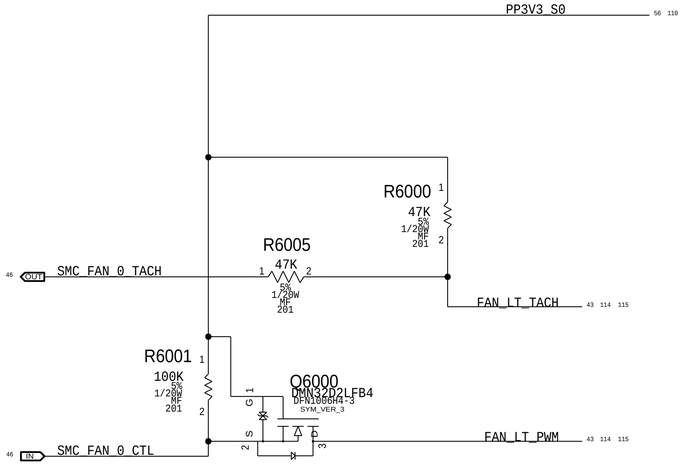
Apple Inc.

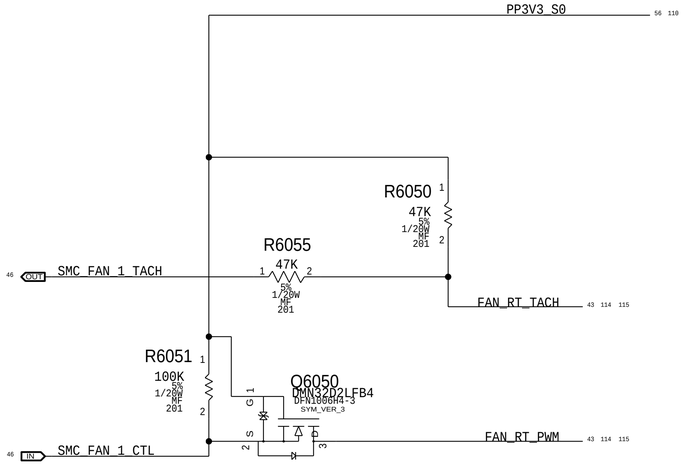
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 59 OF 145
SHEET 55 OF 121

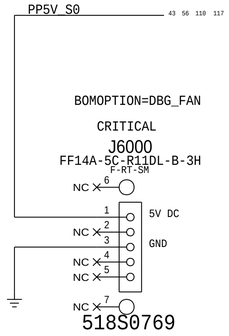
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

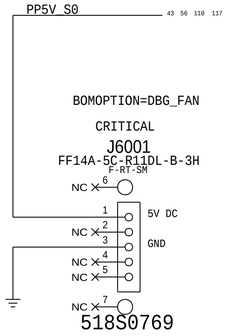
FAN CONNECTOR

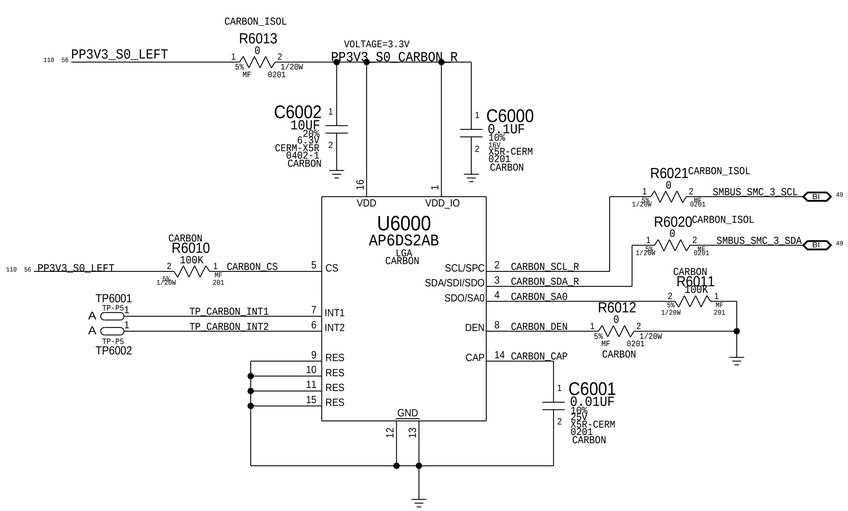
KEEP THE 5 PIN CONNECTOR FROM D1









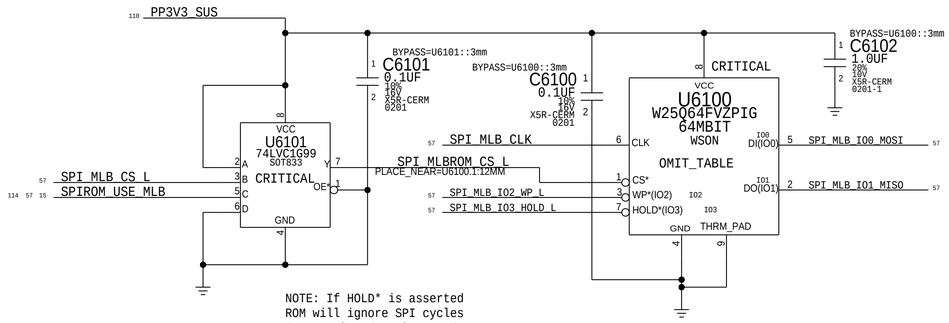


BOM_COST_GROUP=FAN

PAGE TITLE
Fans
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 60 OF 145
SHEET 56 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SPI ROM

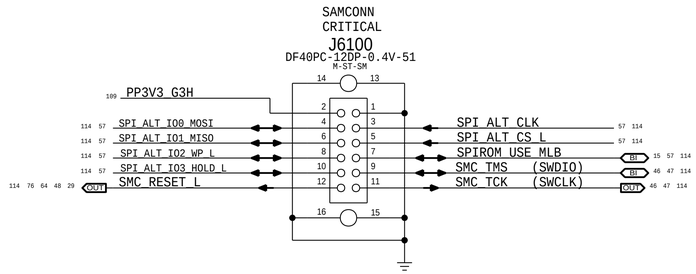
Quad-IO Mode (Mode 0 & 3) supported.
SPI Frequency: 50MHz for CPU, 20MHz for SMC.



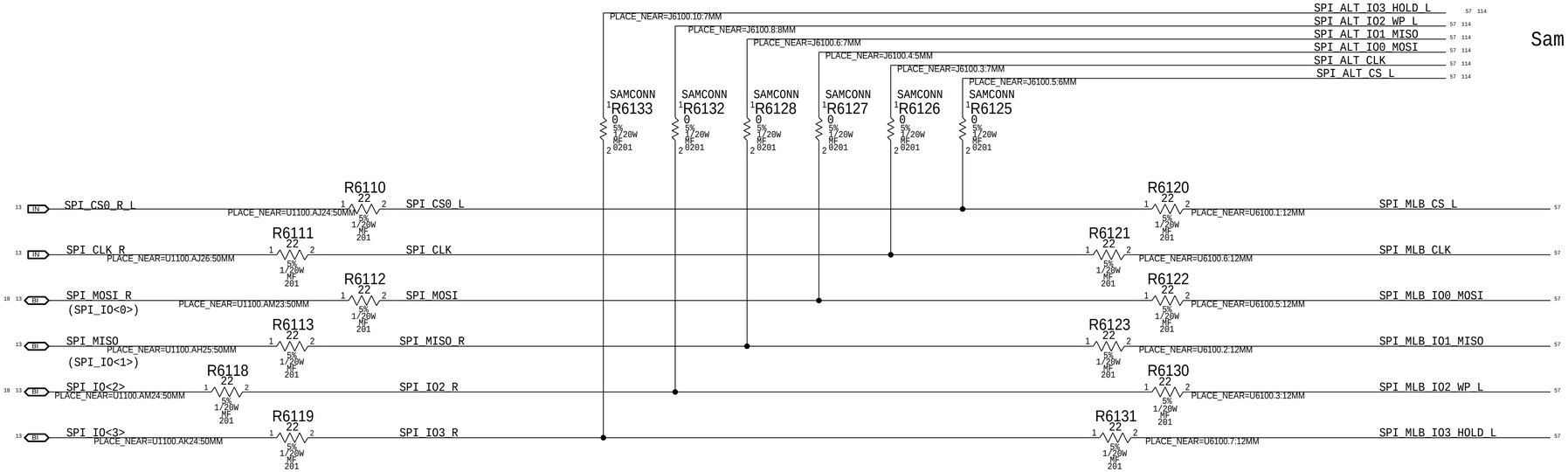
NOTE: If HOLD* is asserted
ROM will ignore SPI cycles
in normal and Dual-IO modes.

Quad SPI and QPI instructions require the non-volatile Quad Enable bit (QE)
in Status Register-2 to be set. When QE=1, the /WP pin becomes IO2 and /HOLD pin becomes IO3.

SPI+SWD SAM Connector



SPI Bus Series Termination (Modified per PDG)



BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE: SPI Debug Connector

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 61 OF 145
SHEET: 57 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PCH AUDIO

AUDIO JACK CODEC

RIGHT SPEAKER AMPS

LEFT SPEAKER AMPS

3-MIC CONNECTOR
APN: 518S0818

BOM_COST_GROUP=AUDIO

PAGE TITLE	HDA Bridge
	Apple Inc.
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	62 OF 145
SHEET	58 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

AUDIO JACK CODEC I2C ADDRESS

AD1	AD0	ADDRESS
GND	GND	0x48 <--
GND	1.8V	0x49
1.8V	GND	0x4A
1.8V	1.8V	0x4B

L6361 FERR-470-OHM 0201
12 AUD_PWR_EN → L83_LDO_EN

L6360 FERR-22-OHM-1A-0.055OHM 0201
110 59 PP3V3_S0 → PP3V3_S0_AUD_F

U6360 NCP160AMX180 XDFN-COMBO
PP3V3_S0_AUD_F → IN (4); EN (3); GND EPAD (2, 5); OUT (1) → PP1V8_S0_LDO_AUD 59
VOLTAGE=1.8V

C6360 1.0UF 20% 10V X5R-CERM 0201-1 CRITICAL
BYPASS=U6360.A1:B2:3 MM

R6360 100K 5% 1/20W MF 201 NOSTUFF

XW6300 SHORT-8L-0.25MM-SM

C6361 1.0UF 20% 10V X5R-CERM 0201-1 CRITICAL
BYPASS=U6360.A2:B2:3 MM

GND_AUDIO_CODEC 59 117

59 PP1V8_S0_LDO_AUD
C6301 2.2UF 10% 10V X5R-CERM 0402 CRITICAL
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200
BYPASS=U6300.B1:C2:5 MM
117 59 GND_AUDIO_CODEC

L6300 FERR-22-OHM-1A-0.055OHM 0201
L83_VCP MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.0850

L6301 FERR-22-OHM-1A-0.055OHM 0201
59 PP1V8_S0_LDO_AUD → L83_VL MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
C6303 0.1UF 10% 50V X7R 603-1 CRITICAL
BYPASS=U6300.A3:B3:5 MM

L6302 FERR-22-OHM-1A-0.055OHM 0201
110 59 PP3V3_S0 → L83_VP MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1000
C6304 10UF 20% 10V X5R-CERM 0402-7 CRITICAL
BYPASS=U6300.D7:C7:5 MM

C6302 2.2UF 10% 10V X5R-CERM 0402 CRITICAL
BYPASS=U6300.D6:F6:5 MM
XW6301 SHORT-8L-0.25MM-SM
GND_VCP

OMIT_TABLE C6305 4.7UF 10% 10V X5R 0402
L83_VCP_FILTP MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
BYPASS=U6300.E6:F6:5 MM

OMIT_TABLE C6306 4.7UF 10% 10V X5R 0402
L83_VCP_FILTN MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
BYPASS=U6300.G6:F6:5 MM

62 OUT AUD_HP_PORT_L → R6300 1K 5% 1/20W MF 201 → 117 59 GND_AUDIO_CODEC
NO_XNET_CONNECTION=1

NO_XNET_CONNECTION=1 R6301 1K 5% 1/20W MF 201

62 IN AUD_HP_SENSE_L
62 IN AUD_HP_SENSE_R
62 OUT AUD_HP_PORT_R
62 BI AUD_HP_PORT_CH_GND
62 BI AUD_HP_PORT_US_GND

C6321 470PF 10% 16V X5R-X7R 201 NOSTUFF PLACE_NEAR=U6300:10mm
C6322 470PF 10% 16V X5R-X7R 201 NOSTUFF PLACE_NEAR=U6300:10mm
C6320 560PF 5% 25V C0G 0201 NOSTUFF PLACE_NEAR=U6300:10mm

R6351 2.2K 1% 1/20W MF 201
R6352 2.2K 1% 1/20W MF 201
C6352 27PF 5% 25V C0G 0201 CRITICAL
C6351 3300PF 10% 16V X7R-CERM 0201 CRITICAL
R6350 100K 5% 1/20W MF 201
62 IN AUD_HS_MIC_P
62 IN AUD_HS_MIC_N
R/C6550 FILTER TO ADDRESS OUT-OF-BAND NOISE ISSUE SEEN ON EARLY HEADSETS (SEE RADAR # 6210118)
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

HS_MIC_P
HS_MIC_N
AUD_RING_SENSE
62 IN AUD_TIP_SENSE

R6310 0 5% 1/20W MF 201
PLACE_NEAR=U6300:10mm

C6309 4.7UF 20% 6.3V X5R 402 CRITICAL
BYPASS=U6300.F3:E3:5 MM
L83_HSBIAS_FILT MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000
L83_HSBIAS_FILT_REF MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

CRITICAL U6300 CS42L83A WLCSP-SKT
APN:338S00142

D7	VP	+VCP_FILT	E6
A3	VL	-VCP_FILT	G6
A7	VD_FILT	GNDCP	F6
XNC		VL_SEL	C4
B1	VA	DIGLDO_PDN*	D4
D6	VCP	INT*	B7
D5	HPSENSA	WAKE*	C6
E5	HPOUTA	RESET*	C5
F5	HPSENSB	SPDIF_TX	A6
G5	HPOUTB	SWIRE_SEL	D3
F1	HS4	ASP_LRCK/FSYNC	B5
E2	HS_CLAMP2	SWIRE_SD/ASP_SDIN	A5
E1	HSIN+	ASP_SDOUT	A4
G2	HS3	SWIRE_CLK/ASP_SCLK	B4
F2	HS_CLAMP1	AD0	C3
D1	HSIN-	AD1	B2
F4	HS4_REF	SDA	A1
G4	HS3_REF	SCL	A2
G3	RING_SENSE	FLYP	E7
E4	TIP_SENSE	FLYC	F7
F3	HSBIAS_FILT	FLYN	G7
E3	HSBIAS_FILT_REF	FILT_P	C1
B3	GNDL		
B6	GNDD		
C7			
G1	GNDHS		
C2	GNDA		
D2			

AUD_CODEC_INT_L OUT 58
AUD_CODEC_WAKE_L <RDAR://PROBLEM/22033298>
AUD_CODEC_RESET_L IN 58
AUD_ASP2_LRCLK IN 58
AUD_ASP2_SDOUT IN 58
AUD_ASP2_SDIN OUT 58
AUD_ASP2_SCLK IN 58
L83_SDOUT_R
L83_SDOUT

R6304 0 5% 1/20W MF 201 PLACE_NEAR=U6300:5mm
R6306 33 5% 1/20W MF 201 PLACE_NEAR=U6300:10MM

C6307 2.2UF 10% 10V X5R-CERM 0402 CRITICAL
BYPASS=U6300.E7:F7:5 MM
C6308 2.2UF 10% 10V X5R-CERM 0402 CRITICAL
BYPASS=U6300.G7:F7:5 MM
C6380 47PF 5% 25V C0G 0201 NOSTUFF

62 BI AUD_I2C_1B_SDA
62 IN AUD_I2C_1B_SCL
L83_FLYP
L83_FLYC
L83_FLYN
L83_FILTP MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1000

C6310 10UF 20% 10V X5R 0603 CRITICAL
BYPASS=U6300.C1:C2:5 MM

PP3V3_S0 59 110
R6302 47K 5% 1/20W MF 201
R6303 100K 1% 1/20W MF 201

GND_AUDIO_CODEC
MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 59 117

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0719	2	CAP,CER,4.7UF,20%,10V,X5R,0402,MURATA	C6305,C6306	CRITICAL	

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO JACK CODEC

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 63 OF 145
SHEET 59 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK

VREF_AMP_WL
BYPASS=U6400.E4:C4:5 MM
C6400 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6400.A2:C2:10 MM
BYPASS=U6400.E2:C2:10 MM
BYPASS=U6400.A3:B3:5 MM
BYPASS=U6400.E3:D3:5 MM
PPBUS_G3H 60 61 109
C6401 0.1UF 10% 16V X7R-CERM 0402
C6402 0.1UF 10% 16V X7R-CERM 0402
C6403 10UF 20% 35V X5R-CERM 0603
C6404 10UF 20% 35V X5R-CERM 0603
C6480 100UF 20% 20V POLY SM-1
C6481 100UF 20% 20V POLY SM-1
PP1V8_S0 109 61 60 58
BYPASS=U6400.A4:B4:5 MM
C6405 1.0UF 20% 10V X5R-CERM 0201-1

U6400 MAX98706 WLP CRITICAL
A4 E4 A2 E2 A3 E3
DVDD VREFC PVDD
IRQ* D5
SCL A6
SDA B6
RESET* E5
BCLK E6
LRCLK C6
DIN D6
DOUT C5
NC
OUTPSNS E1
OUTP D1 D2
OUTN B1 B2
OUTNSNS A1
ADDR0 B5
ADDR1 A5
AGND DGND PGND
C4 D4 B4 B3 C1 C2 C3 D3

61 58 OUT AUD_SPKRAMP_INT_L
61 58 IN AUD_SPKRAMP_RESET_L
R6401 100K 5% 1/20W MF 201
60 58 IN AUD_I2C_1A_SCL
60 58 BI AUD_I2C_1A_SDA
I2C ADDRESS = 0x31
PP1V8_S0 58 60 61 109

PLACE_NEAR=U6400:5MM
60 58 IN AUD_ASP1A_SCLK
R6402 0 5% 1/20W MF 201
SPKRAMP_WL_SCLK
PLACE_NEAR=U6400:5MM
60 58 IN AUD_ASP1A_LRCLK
R6403 0 5% 1/20W MF 201
SPKRAMP_WL_LRCLK
PLACE_NEAR=U6400:5MM
60 58 IN AUD_ASP1A_SDOUT
R6405 0 5% 1/20W MF 201
SPKRAMP_WL_SDIN

L6400 180OHM-3.4A 0806
SPKRAMP_WL_OUT_POS
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
114 SPKRCONN_WL_OUT_POS
L6401 180OHM-3.4A 0806
SPKRAMP_WL_OUT_NEG
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1000
114 SPKRCONN_WL_OUT_NEG
C6406 220PF 5% 25V C0G-CERM 0402
C6407 220PF 5% 25V C0G-CERM 0402

APN: 518S00521
J6410 78171-0004 M-RT-SM
5 1 2 3 4 6

LEFT SPEAKER CONNECTOR

VREF_AMP_TL
BYPASS=U6450.E4:C4:5 MM
C6450 1.0UF 20% 10V X5R-CERM 0201-1
BYPASS=U6450.A2:C2:10 MM
BYPASS=U6450.E2:C2:10 MM
BYPASS=U6450.A3:B3:5 MM
BYPASS=U6450.E3:D3:5 MM
PPBUS_G3H 60 61 109
C6451 0.1UF 10% 16V X7R-CERM 0402
C6452 0.1UF 10% 16V X7R-CERM 0402
C6453 10UF 20% 35V X5R-CERM 0603
C6454 10UF 20% 35V X5R-CERM 0603
PP1V8_S0 109 61 60 58
BYPASS=U6450.A4:B4:5 MM
C6455 1.0UF 20% 10V X5R-CERM 0201-1

U6450 MAX98706 WLP CRITICAL
A4 E4 A2 E2 A3 E3
DVDD VREFC PVDD
IRQ* D5
SCL A6
SDA B6
RESET* E5
BCLK E6
LRCLK C6
DIN D6
DOUT C5
NC
OUTPSNS E1
OUTP D1 D2
OUTN B1 B2
OUTNSNS A1
ADDR0 B5
ADDR1 A5
AGND DGND PGND
C4 D4 B4 B3 C1 C2 C3 D3

60 58 IN AUD_I2C_1A_SCL
60 58 BI AUD_I2C_1A_SDA
I2C ADDRESS = 0x32

PLACE_NEAR=U6450:5MM
60 58 IN AUD_ASP1A_SCLK
R6452 0 5% 1/20W MF 201
SPKRAMP_TL_SCLK
PLACE_NEAR=U6450:5MM
60 58 IN AUD_ASP1A_LRCLK
R6453 0 5% 1/20W MF 201
SPKRAMP_TL_LRCLK
PLACE_NEAR=U6450:5MM
60 58 IN AUD_ASP1A_SDOUT
R6455 0 5% 1/20W MF 201
SPKRAMP_TL_SDIN

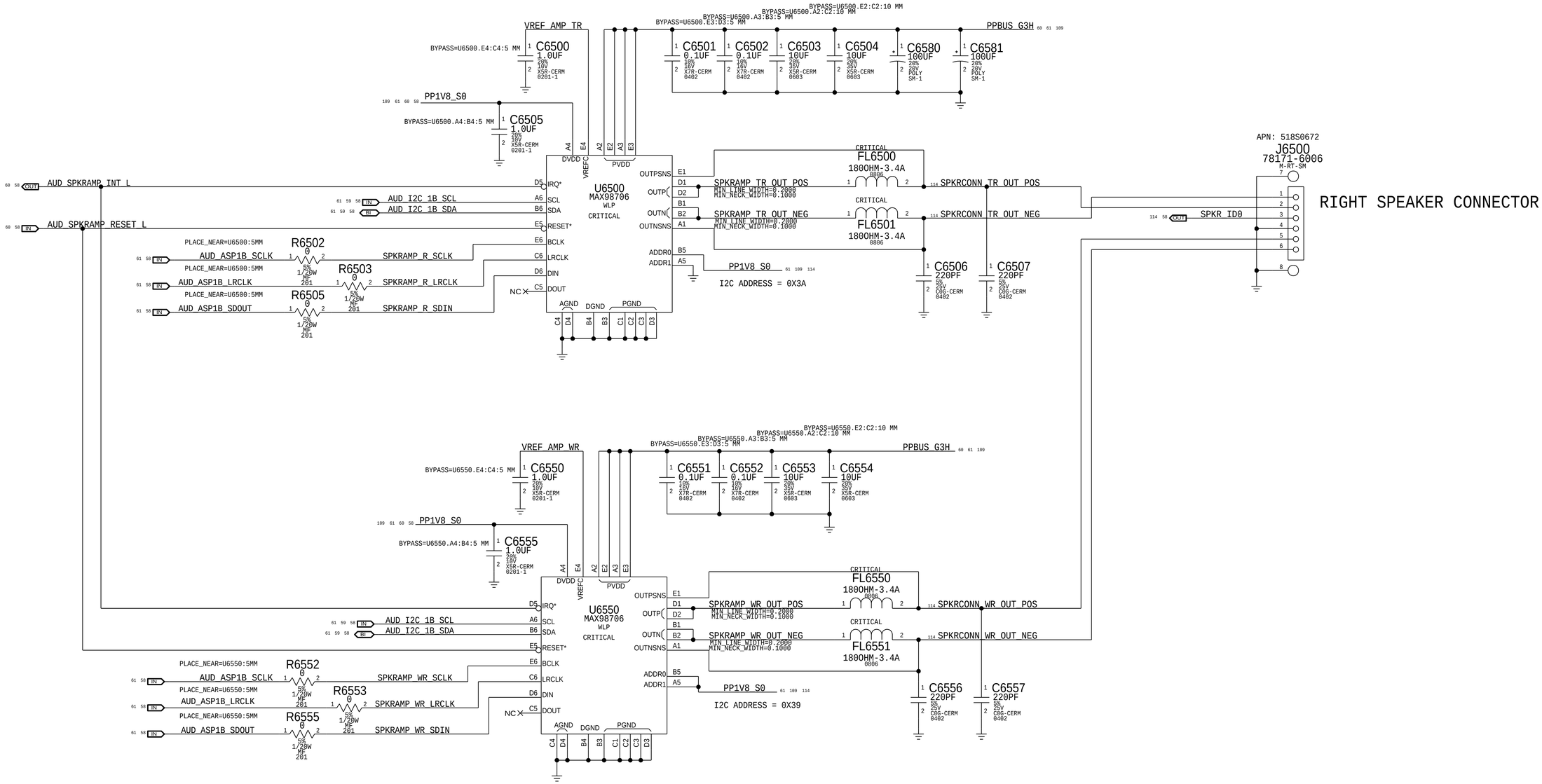
L6450 180OHM-3.4A 0806
SPKRAMP_TL_OUT_POS
114 SPKRCONN_TL_OUT_POS
L6451 180OHM-3.4A 0806
SPKRAMP_TL_OUT_NEG
114 SPKRCONN_TL_OUT_NEG
C6456 220PF 5% 25V C0G-CERM 0402
C6457 220PF 5% 25V C0G-CERM 0402

BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 64 OF 145
SHEET 60 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

2X MONO SPEAKER AMPLIFIER
APN: 353S00604
0dBFS = 9VPK



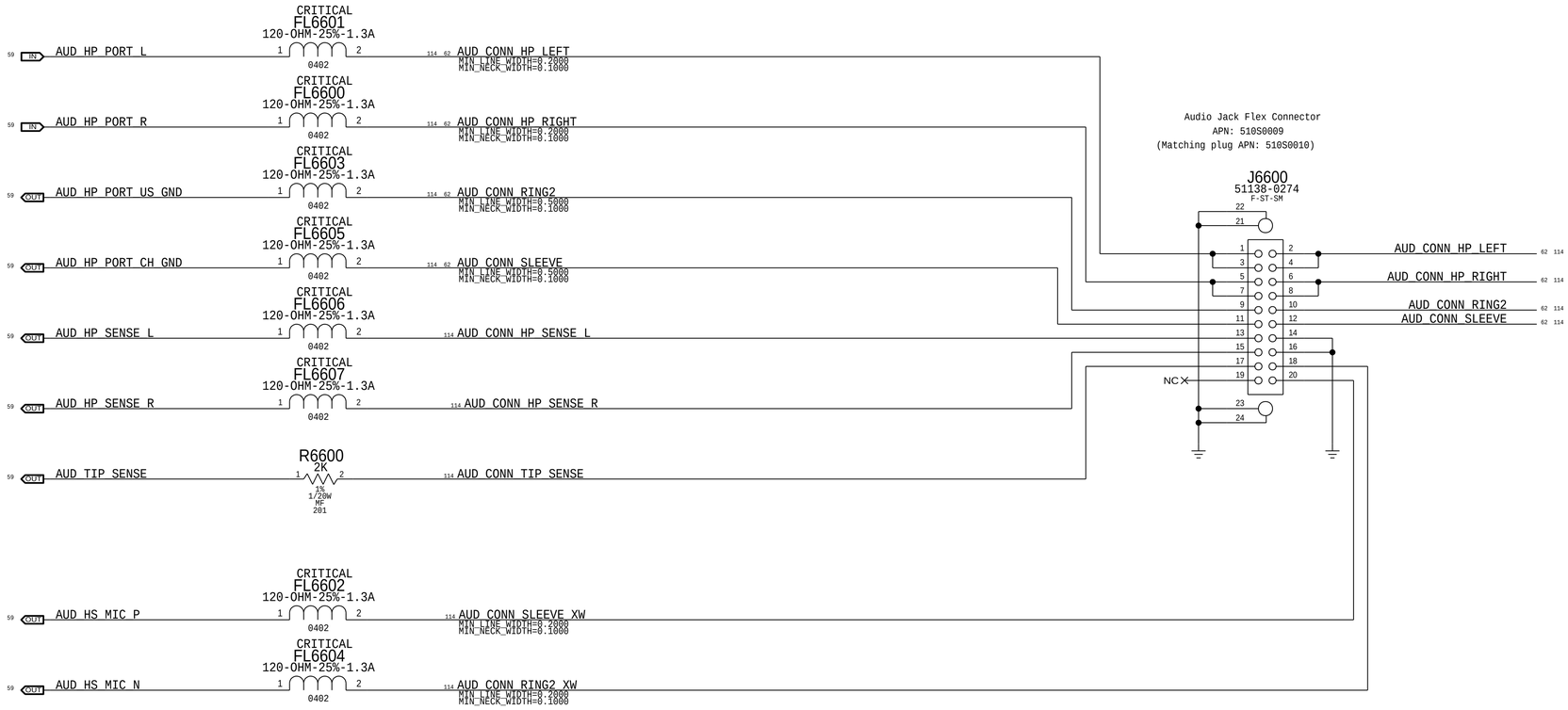
BOM_COST_GROUP=AUDIO

PAGE TITLE
AUDIO Speaker Amps & Conn

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 65 OF 145
SHEET 61 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM_COST_GROUP=AUDIO

PAGE TITLE

AUDIO JACK CONNECTOR

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 66 OF 145

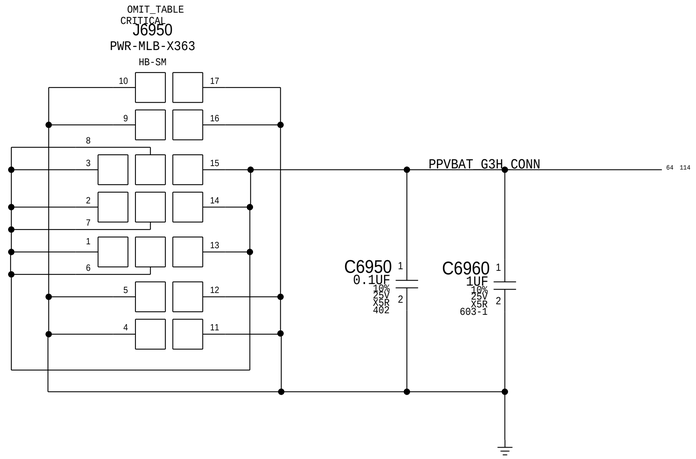
SHEET 62 OF 121

NOTICE OF PROPRIETARY PROPERTY:

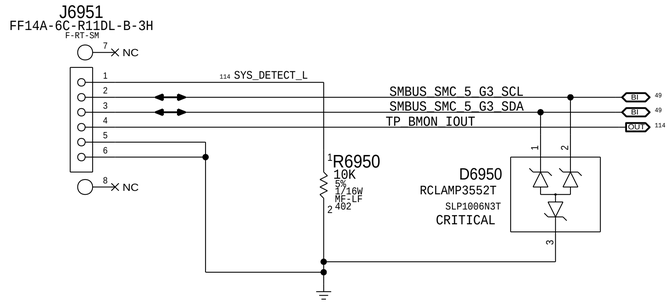
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

J80 Battery Hotbar Flex Pads 998-03902

Flex Pad TO MLB 998-03780.

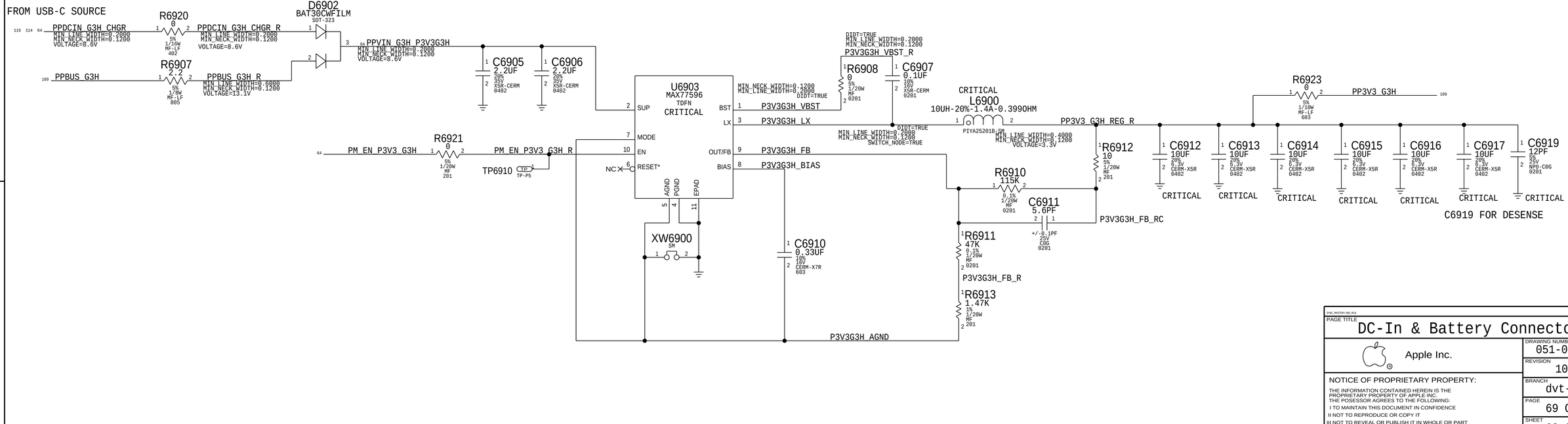


APN:518S0818



BMU POWER FLEX HOTBAR'd TO THE MLB:

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
632-00862	1	PCBA,FLEX,BMU PWR,X363	J6950	CRITICAL	



PAGE TITLE

DC-In & Battery Connectors

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 69 OF 145

SHEET 63 OF 121

NOTICE OF PROPRIETARY PROPERTY:

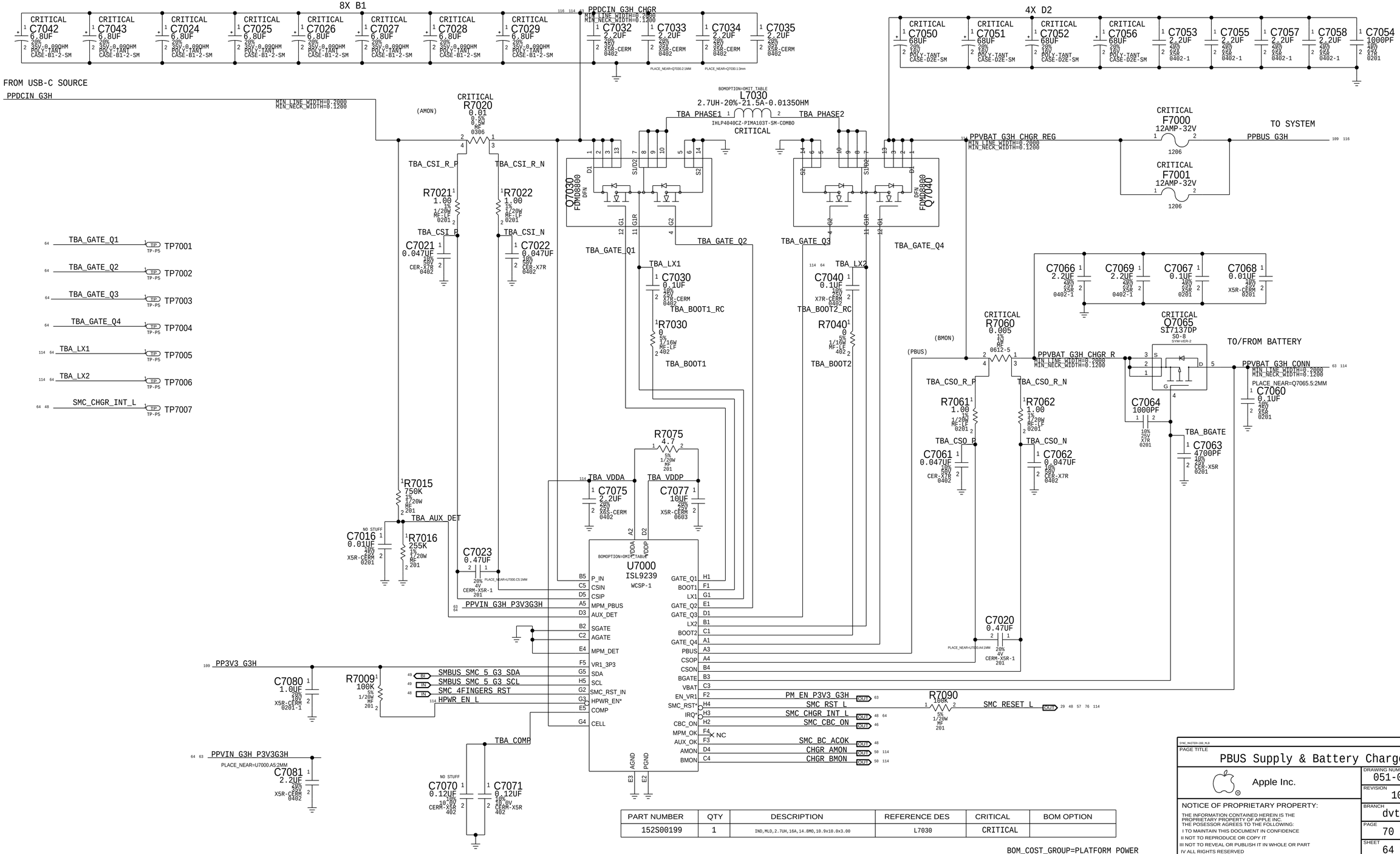
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00199	1	IND,MLD,2.7UH,16A,14.8MO,10.9x10.0x3.00	L7030	CRITICAL	

BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J09_MLB
SYNC_DATE=11/06/2015

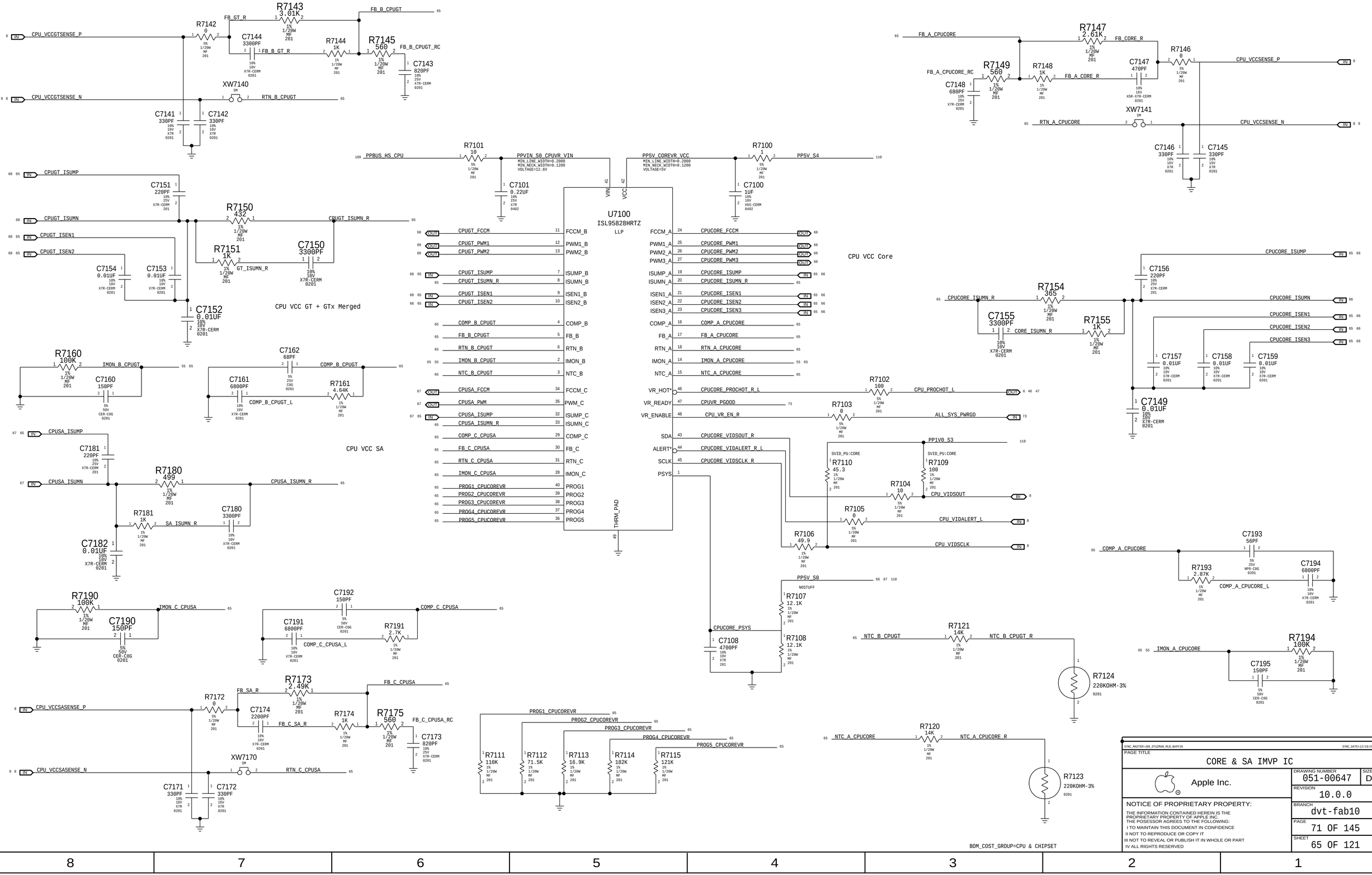
PAGE TITLE

PBUS Supply & Battery Charger

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 70 OF 145
SHEET 64 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


CPU_VCCGTSENSE_P
CPU_VCCGTSENSE_N
R7142 0
R7143 3.01K
R7144 1K
R7145 560
C7144 3300PF
C7143 820PF
FB_GT_R
FB_B_CPUGT
FB_B_CPUGT_RC
XW7140
RTN_B_CPUGT
C7141 330PF
C7142 330PF
CPUGT_ISUMP
CPUGT_ISUMN
CPUGT_ISEN1
CPUGT_ISEN2
C7151 220PF
R7150 432
R7151 1K
C7150 3300PF
C7154 0.01UF
C7153 0.01UF
C7152 0.01UF
CPUGT_ISUMN_R
GT_ISUMN_R
CPU VCC GT + GTx Merged
R7160 100K
C7160 150PF
IMON_B_CPUGT
C7162 68PF
C7161 6800PF
R7161 4.64K
COMP_B_CPUGT
COMP_B_CPUGT_L
CPUSA_ISUMP
CPUSA_ISUMN
C7181 220PF
R7180 499
R7181 1K
C7180 3300PF
C7182 0.01UF
SA_ISUMN_R
CPUSA_ISUMN_R
CPU VCC SA
R7190 100K
C7190 150PF
IMON_C_CPUSA
C7192 150PF
C7191 6800PF
R7191 2.7K
COMP_C_CPUSA
COMP_C_CPUSA_L
CPU_VCCSASENSE_P
CPU_VCCSASENSE_N
R7172 0
R7173 2.49K
R7174 1K
R7175 560
C7174 2200PF
C7173 820PF
FB_SA_R
FB_C_CPUSA
FB_C_CPUSA_RC
XW7170
RTN_C_CPUSA
C7171 330PF
C7172 330PF
PPBUS_HS_CPU
R7101 10
C7101 0.22UF
PPVIN_S0_CPUVR_VIN
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=12.6V
PP5V_COREVR_VCC
R7100 1
C7100 1UF
PP5V_S4
U7100
ISL95828HRTZ
LLP
VIN
VCC
THRM_PAD
CPUGT_FCCM
CPUGT_PWM1
CPUGT_PWM2
CPUGT_ISUMP
CPUGT_ISUMN_R
CPUGT_ISEN1
CPUGT_ISEN2
COMP_B_CPUGT
FB_B_CPUGT
RTN_B_CPUGT
IMON_B_CPUGT
NTC_B_CPUGT
CPUSA_FCCM
CPUSA_PWM
CPUSA_ISUMP
CPUSA_ISUMN_R
COMP_C_CPUSA
FB_C_CPUSA
RTN_C_CPUSA
IMON_C_CPUSA
PROG1_CPUCOREVR
PROG2_CPUCOREVR
PROG3_CPUCOREVR
PROG4_CPUCOREVR
PROG5_CPUCOREVR
FCCM_B
PWM1_B
PWM2_B
ISUMP_B
ISUMN_B
ISEN1_B
ISEN2_B
COMP_B
FB_B
RTN_B
IMON_B
NTC_B
FCCM_C
PWM_C
ISUMP_C
ISUMN_C
COMP_C
FB_C
RTN_C
IMON_C
PROG1
PROG2
PROG3
PROG4
PROG5
FCCM_A
PWM1_A
PWM2_A
PWM3_A
ISUMP_A
ISUMN_A
ISEN1_A
ISEN2_A
ISEN3_A
COMP_A
FB_A
RTN_A
IMON_A
NTC_A
VR_HOT*
VR_READY
VR_ENABLE
SDA
ALERT*
SCLK
PSYS
CPUCORE_FCCM
CPUCORE_PWM1
CPUCORE_PWM2
CPUCORE_PWM3
CPUCORE_ISUMP
CPUCORE_ISUMN_R
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
COMP_A_CPUCORE
FB_A_CPUCORE
RTN_A_CPUCORE
IMON_A_CPUCORE
NTC_A_CPUCORE
CPUCORE_PROCHOT_R_L
CPUVR_PGOOD
CPU_VR_EN_R
CPUCORE_VIDSOUT_R
CPUCORE_VIDALERT_R_L
CPUCORE_VIDSCLK_R
PP5V_S0
NOSTUFF
CPUCORE_PSYS
R7107 12.1K
R7108 12.1K
C7108 4700PF
R7102 100
R7103 0
CPU_PROCHOT_L
ALL_SYS_PWRGD
PP1V0_S3
SVID_PU:CORE
R7110 45.3
R7109 100
R7104 10
R7105 0
CPU_VIDSOUT
CPU_VIDALERT_L
CPU_VIDSCLK
R7106 49.9
R7111 110K
R7112 71.5K
R7113 16.9K
R7114 182K
R7115 121K
R7120 14K
R7123 220KOHM-3%
R7121 14K
R7124 220KOHM-3%
NTC_B_CPUGT_R
NTC_A_CPUCORE_R
FB_A_CPUCORE
FB_A_CPUCORE_RC
R7147 2.61K
R7149 560
R7148 1K
C7147 470PF
C7148 680PF
FB_CORE_R
FB_A_CORE_R
R7146 0
CPU_VCCSENSE_P
CPU_VCCSENSE_N
XW7141
RTN_A_CPUCORE
C7146 330PF
C7145 330PF
CPU VCC Core
CPUCORE_ISUMP
CPUCORE_ISUMN
CPUCORE_ISEN1
CPUCORE_ISEN2
CPUCORE_ISEN3
CORE_ISUMN_R
R7154 365
R7155 1K
C7155 3300PF
C7156 220PF
C7157 0.01UF
C7158 0.01UF
C7159 0.01UF
C7149 0.01UF
C7193 56PF
R7193 2.87K
C7194 6800PF
COMP_A_CPUCORE_L
R7194 100K
C7195 150PF
SYNC_MASTER=J80_DTU2MAR_MLB_BAFFIN
SYNC_DATE=12/10/2012
PAGE TITLE
CORE & SA IMVP IC
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 71 OF 145
SHEET 65 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED
BOM_COST_GROUP=CPU & CHIPSET

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	3	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7210,U7220,U7230	CRITICAL	

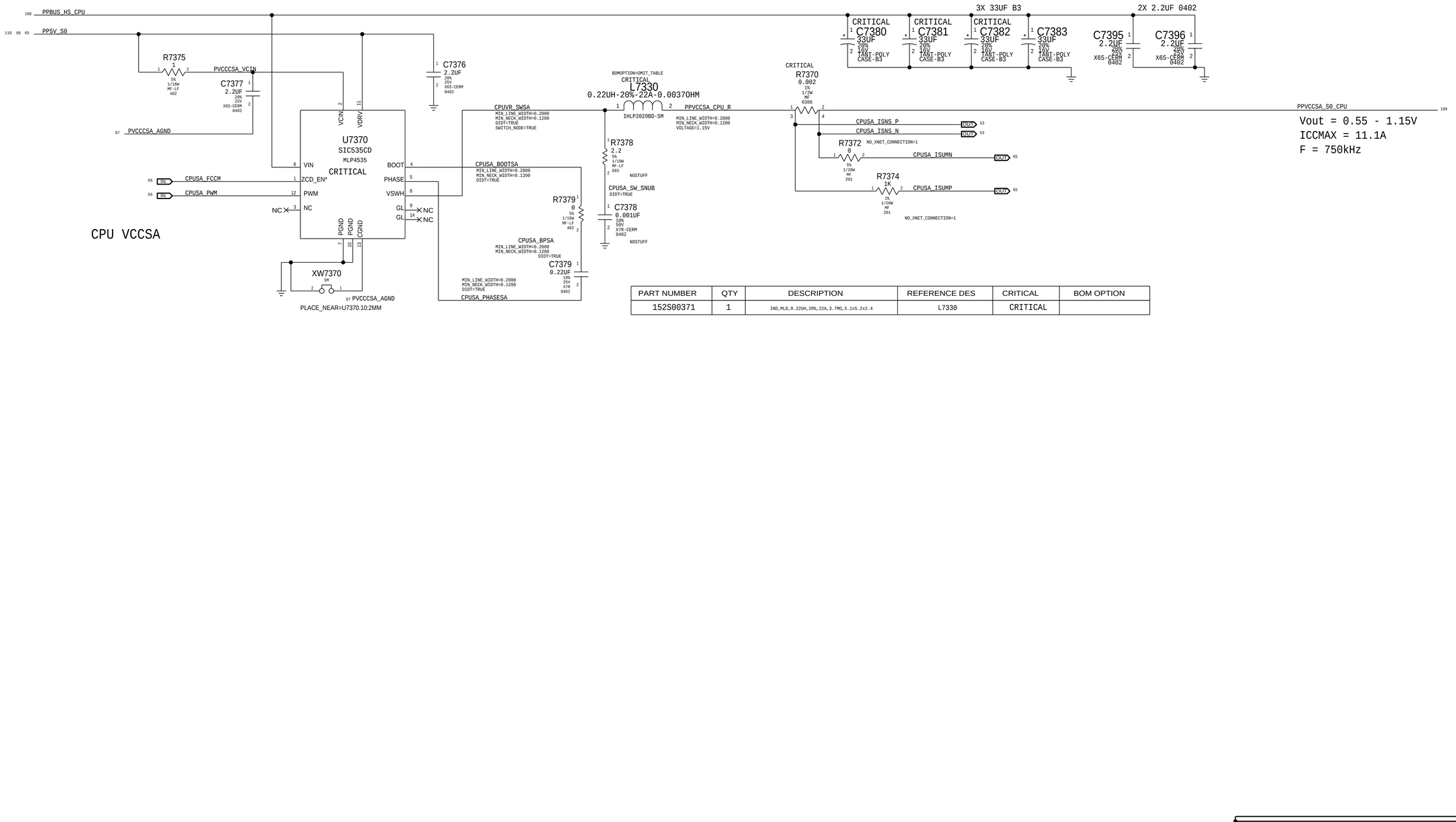
SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN
SYNC_DATE=09/03/2015

PAGE TITLE
CORE IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 72 OF 145
SHEET 66 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



CPU VCCSA

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
152S00371	1	IND,MLD,0.22UH,20%,22A,3.7MO,5.1x5.2x2.4	L7330	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

SYNC_MASTER=J80_DTUZMAN_MLB_BAFFIN SYNC_DATE=11/18/2015

PAGE TITLE

SA IMVP IC

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

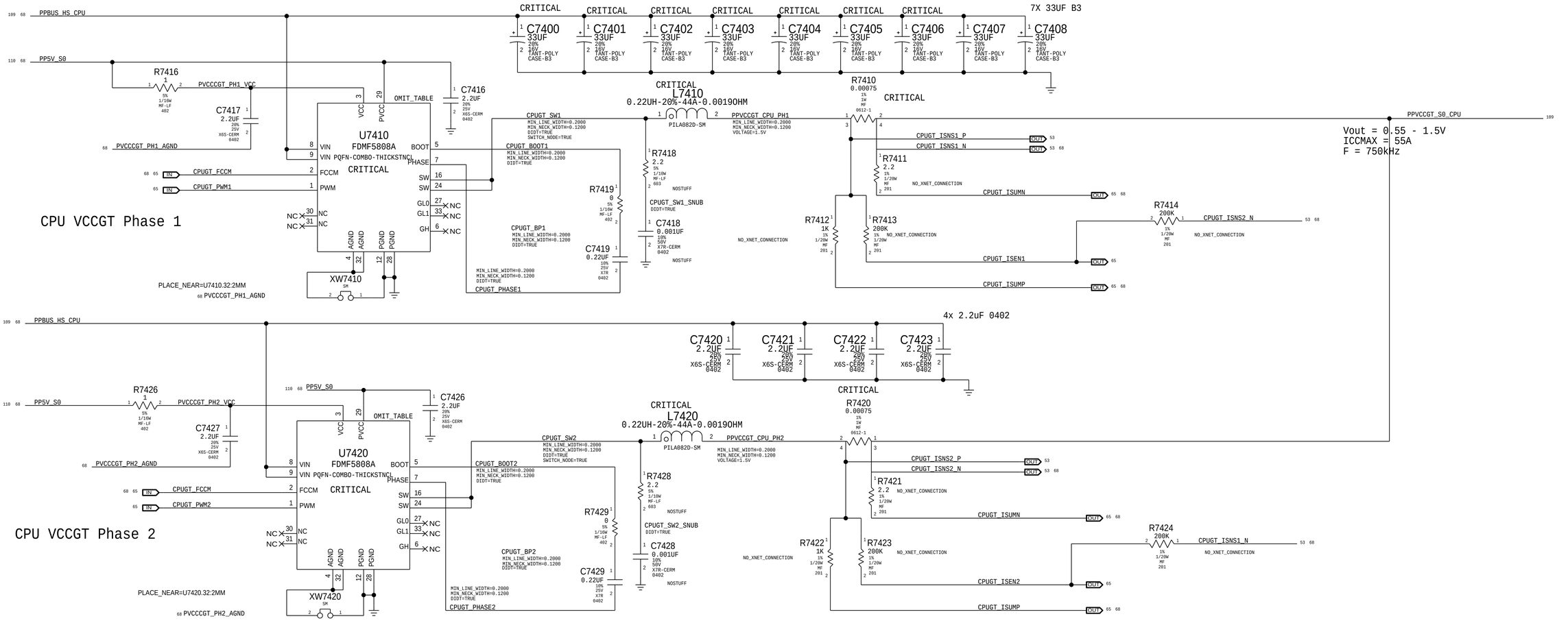
BRANCH dvt-fab10

PAGE 73 OF 145

SHEET 67 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00497	2	IC,SIC635,DRMOS,IMVP-8,40A,PQFN31,5X5	U7410,U7420	CRITICAL	

BOM_COST_GROUP=CPU & CHIPSET

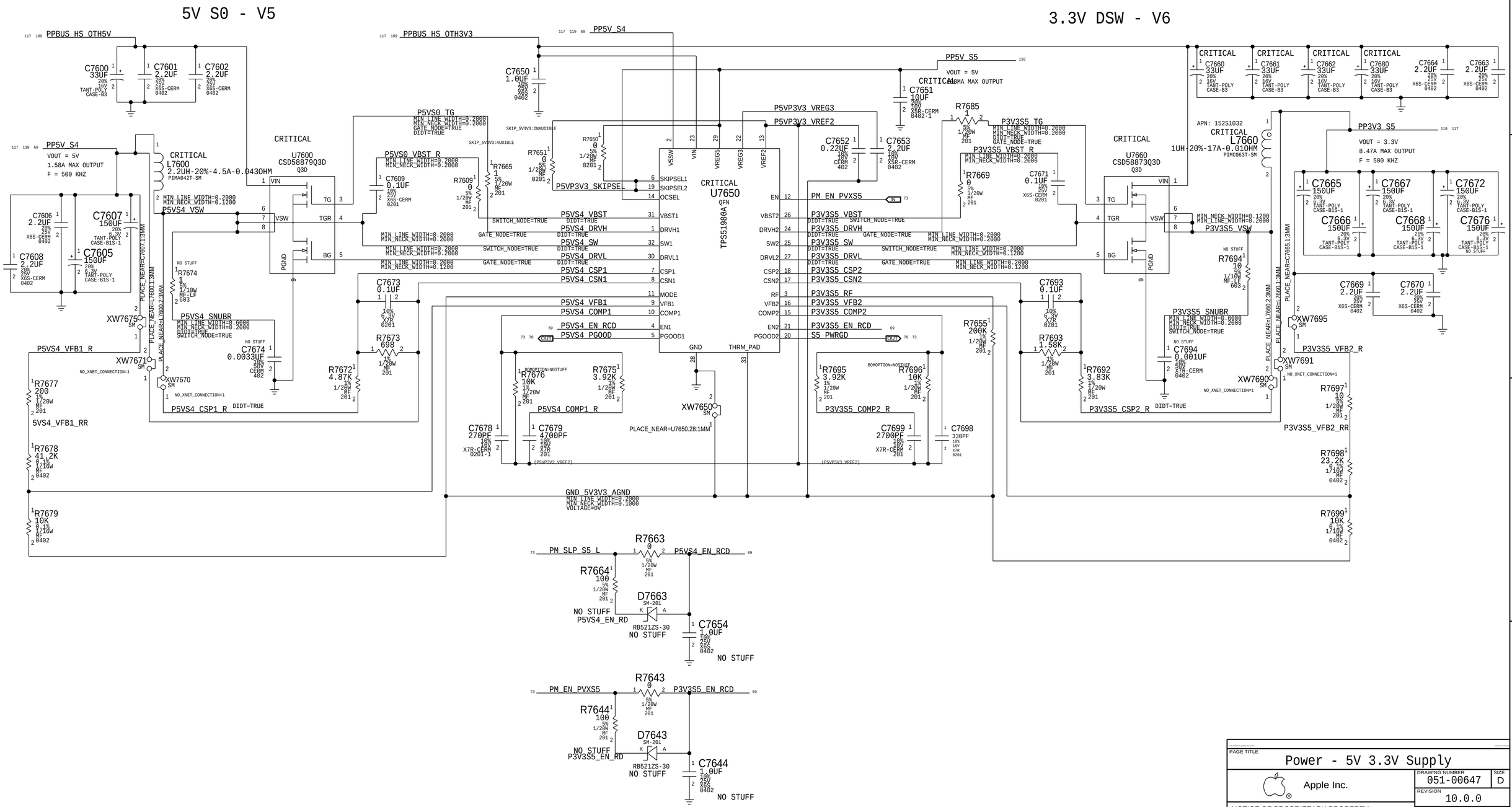
SYNC_MASTER=J80_DTU2MAR_MLB_BAFFIN
SYNC_DATE=09/03/2015

PAGE TITLE
GT & GTX IMVP POWER BLOCK

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 74 OF 145
SHEET 68 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



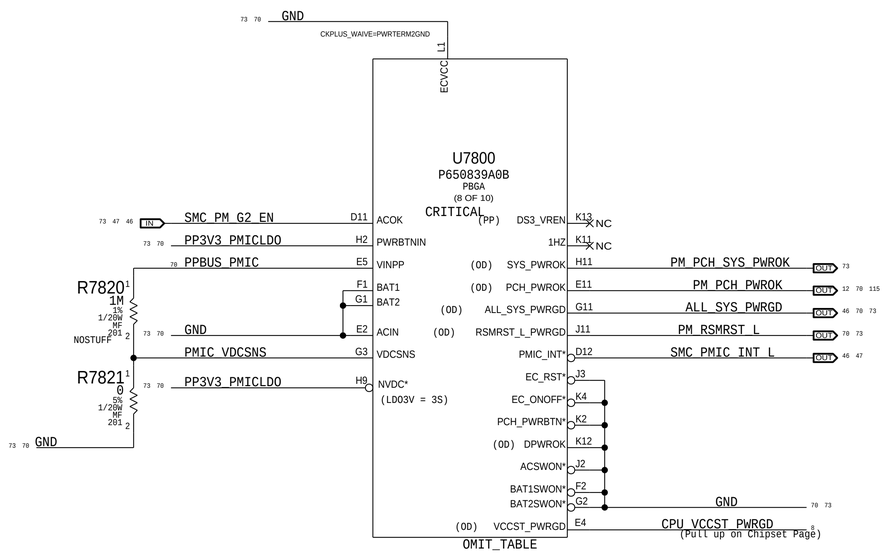
PAGE TITLE
Power - 5V 3.3V Supply

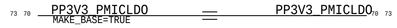
Apple Inc.

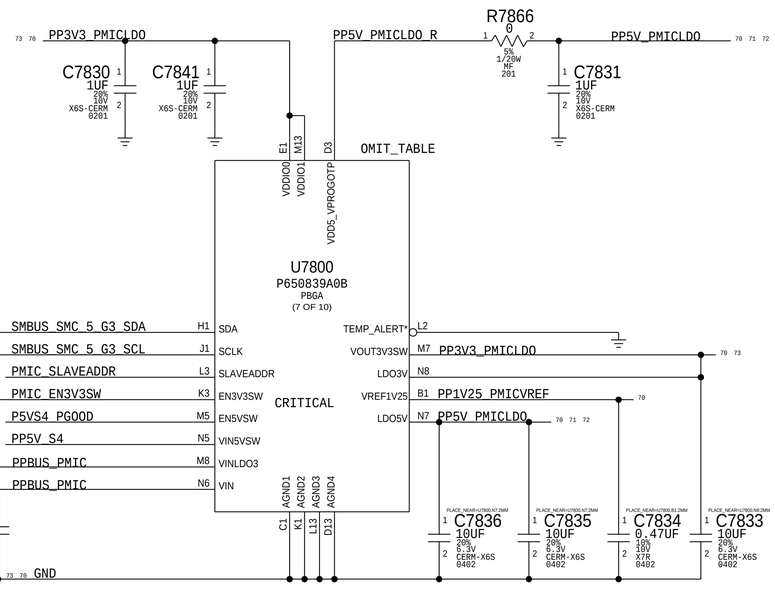
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 76 OF 145
SHEET 69 OF 121

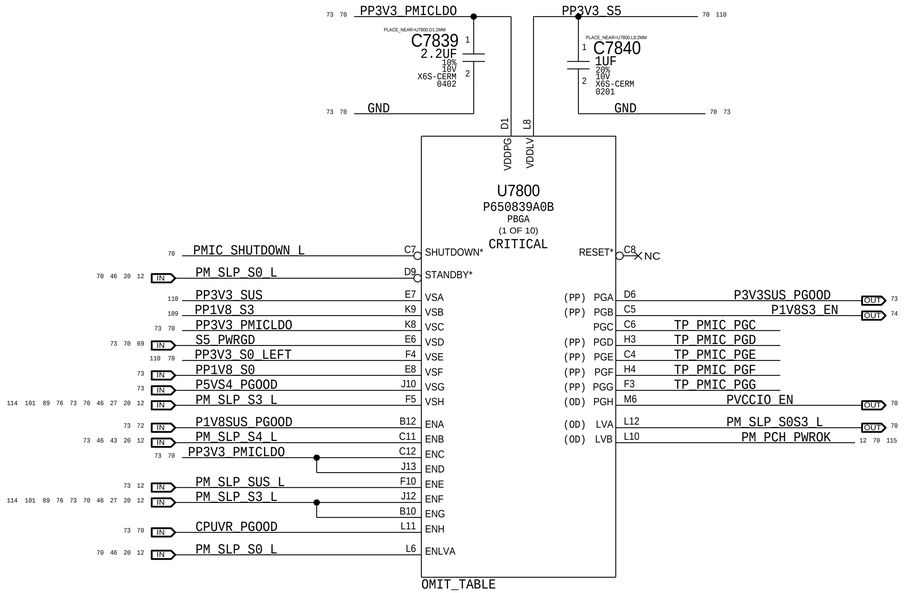
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

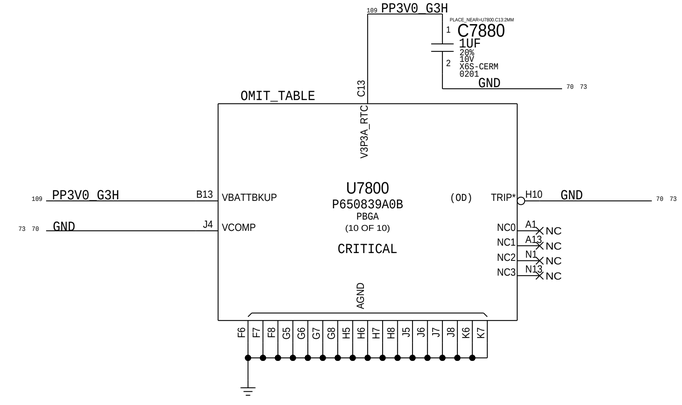
BANJO - PMIC Control

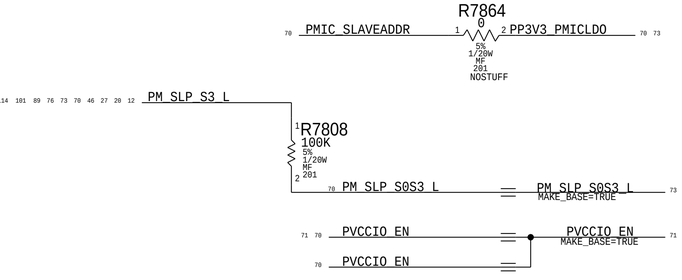


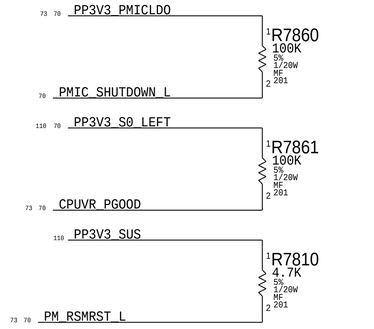


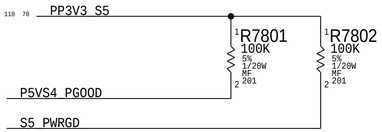


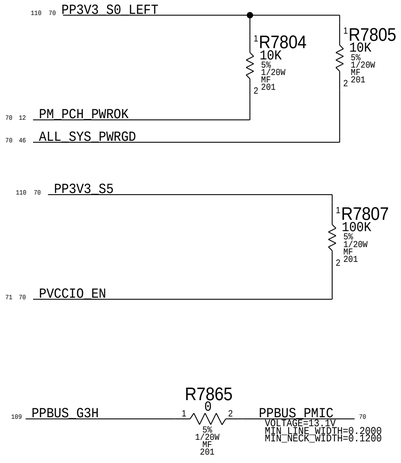












BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J08_MLB
SYNC_DATE=12/08/2016

PAGE TITLE

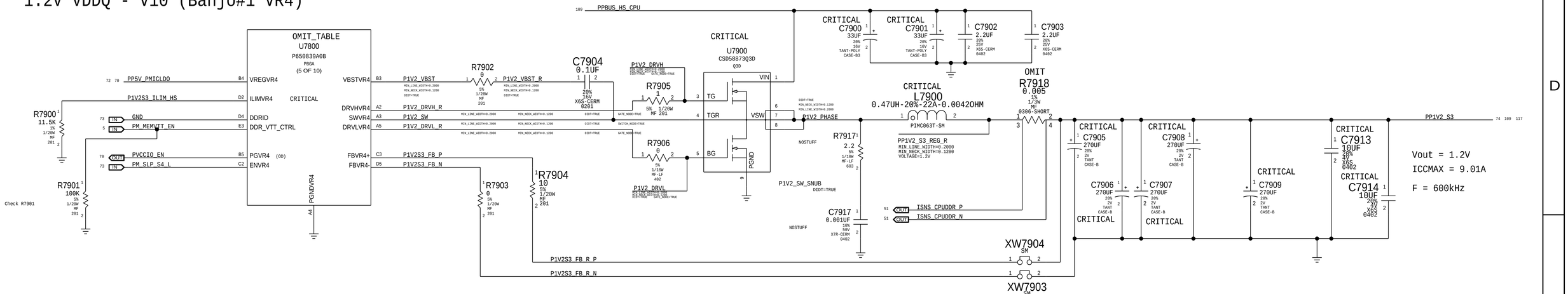
PMIC-1 & Power Control

Apple Inc.

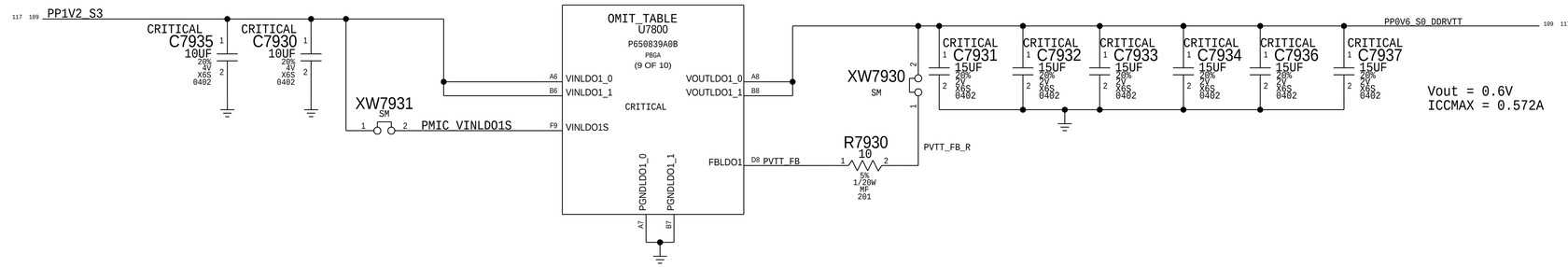
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 78 OF 145
SHEET 70 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

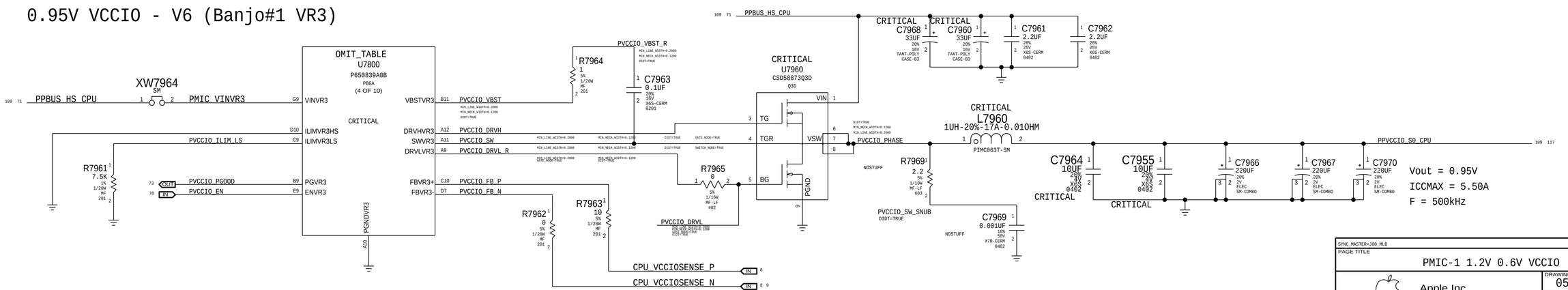
1.2V VDDQ - V10 (Banjo#1 VR4)



0.6V VTT - V13 (Banjo#1 LDO1)



0.95V VCCIO - V6 (Banjo#1 VR3)



BOM_COST_GROUP=PLATFORM POWER

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

PMIC-1 1.2V 0.6V VCCIO

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER 051-00647

SIZE D

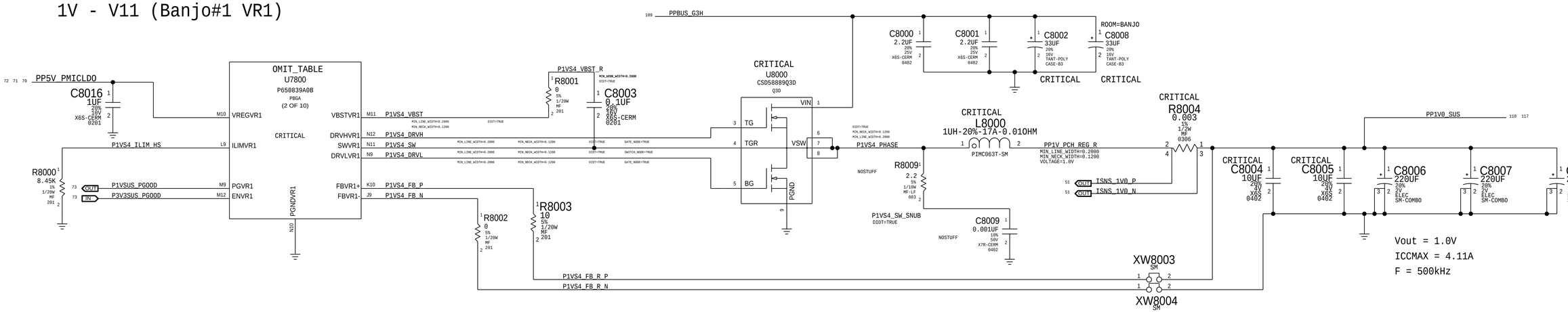
REVISION 10.0.0

BRANCH dvt-fab10

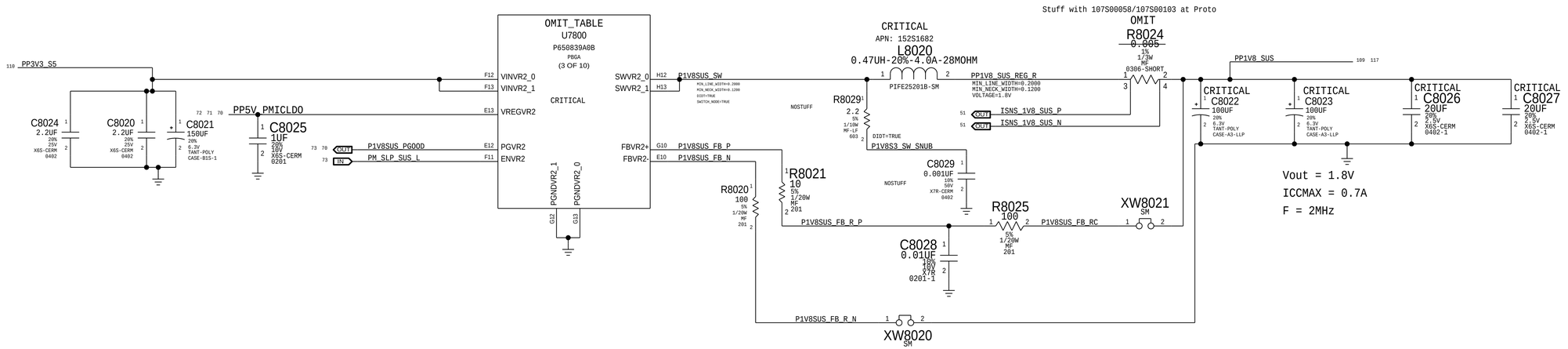
PAGE 79 OF 145

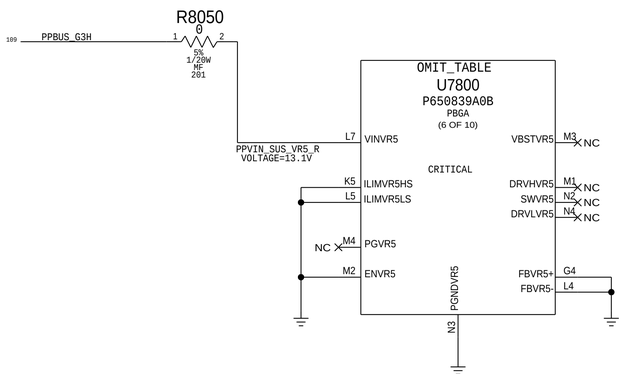
SHEET 71 OF 121

1V - V11 (Banjo#1 VR1)



1.8V - V8 (Banjo#1 VR2)





BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMIC-1 1V 1.8V VCCPCH

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

PAGE: 80 OF 145

SHEET: 72 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

S5 Enables

70 47 46 SMC_PM_G2_EN — MAKE_BASE=TRUE — R8110 0 5% 1/20W MF 201 — MAKE_BASE=TRUE — PM_EN_PVXS5 → PM_EN_PVXS5 (OUT 69), PM_EN_PVXS5 (OUT 69)

SUS Enables

70 12 PM_SLP_SUS_L — MAKE_BASE=TRUE — PM_SLP_SUS_L → PM_SLP_SUS_L (OUT 72), PM_SLP_SUS_L (OUT 74)

S4 Enables

46 20 12 PM_SLP_S5_L — MAKE_BASE=TRUE — PM_SLP_S5_L → PM_SLP_S5_L (OUT 74), PM_SLP_S5_L (OUT 74), PM_SLP_S5_L (OUT 69)

S3 Enables

73 70 46 43 20 12 PM_SLP_S4_L — MAKE_BASE=TRUE — PM_SLP_S4_L (OUT 71)

S0 Enables

114 101 89 76 70 46 27 20 12 PM_SLP_S3_L — MAKE_BASE=TRUE — PM_SLP_S3_L → PM_SLP_S3_L (73), PM_SLP_S3_L (OUT 74), PM_SLP_S3_L (OUT 74)

S0i Enables

73 P1VS0SW_EN_RC — MAKE_BASE=TRUE — P1VS0SW_EN_RC (OUT 74)

73 70 IN PM_SLP_S0S3_L — MAKE_BASE=TRUE — PM_SLP_S0S3_L (OUT 74)

70 PP3V3_PMICLDO — MAKE_BASE=TRUE — PP3V3_PMICLDO 70

110 PP5V_S4 — PP5V_S4 70

70 69 P5VS4_PGOOD — MAKE_BASE=TRUE — P5VS4_PGOOD → P5VS4_PGOOD (OUT 70)

73 70 GND — MAKE_BASE=TRUE — GND 71

70 P3V3SUS_PGOOD — MAKE_BASE=TRUE — P3V3SUS_PGOOD 72

70 46 ALL_SYS_PWRGD — MAKE_BASE=TRUE — ALL_SYS_PWRGD 65

70 69 S5_PWRGD — S5_PWRGD MAKE_BASE=TRUE 46

115 46 18 12 PM_RSMRST_L — MAKE_BASE=TRUE — PM_RSMRST_L 70

73 70 GND — MAKE_BASE=TRUE

73 70 CPUVR_PGOOD — MAKE_BASE=TRUE — CPUVR_PGOOD 65, CPUVR_PGOOD

109 PP1V8_S0 — PP1V8_S0 (OUT 70)

73 70 IN CPUVR_PGOOD — P2MM SM PP → PP8100

71 IN PVCCIO_PGOOD — P2MM SM PP → PP8101

72 IN P1VSUS_PGOOD — P2MM SM PP → PP8102

72 70 IN P1V8SUS_PGOOD — P2MM SM PP → PP8106

J80G specific

114 73 46 12 PM_PCH_SYS_PWROK — MAKE_BASE=TRUE — PM_PCH_SYS_PWROK 70

110 20 14 12 PP3V3_S0 — R8199 10K 1% 1/20W MF 201 — 114 73 46 12 PM_PCH_SYS_PWROK

KEEP THESE RAILS ON WHEN USING XDP

110 73 18 PP3V3_SUS — XDP:YES C8192 0.1UF 10% 10V X5R-CERM 0201 — XDP:YES U8192 74AUP1T97GM SOT886 (S4# OR XDP)

73 18 IN XDP_PRESENT_L (INV)

73 70 46 43 20 12 IN PM_SLP_S4_L

XDP:NO R8193 0 5% 1/20W MF 201

P1V0S3_EN (OUT 74)

XDP:YES R8192 100K 5% 1/20W MF 201

110 73 18 PP3V3_SUS — XDP:YES C8194 0.1UF 10% 10V X5R-CERM 0201 — XDP:YES U8194 74AUP1T97GM SOT886 (S3# AND S0# OR XDP)

73 18 IN XDP_PRESENT_L (INV)

73 70 IN PM_SLP_S0S3_L

XDP:NO R8195 0 5% 1/20W MF 201

P1VS0SW_EN_RC (73)

XDP:YES R8194 100K 5% 1/20W MF 201

73 PM_SLP_S3_L — R8163 0 5% 1/20W MF 201 — P5VS0_EN (OUT 74)

R8164 100 5% 1/20W MF 201

D8163 SM-201 RB521ZS-30 NO STUFF

NO STUFF P5VS0_EN_RD

C8154 1.0UF 10% 25V X5S 0402 NO STUFF

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE: PMIC-1 Aliases & TPs

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

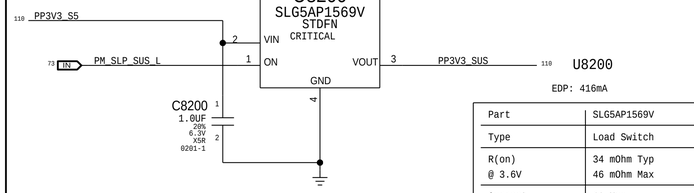
BRANCH dvt-fab10

PAGE 81 OF 145

SHEET 73 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

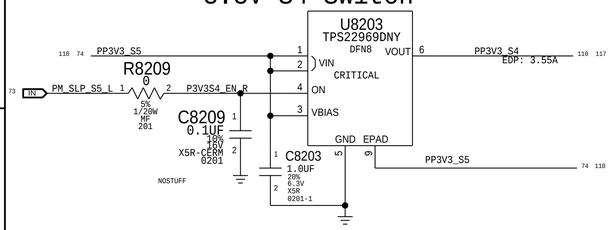
3.3V SUS Switch



U8200
EDP: 416mA

Part	SLG5AP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

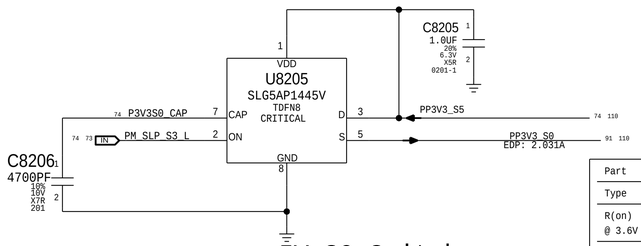
3.3V S4 Switch



U8203

Part	TPS22969
Type	Load Switch
R(on) @ 3.6V	4.4 MOHM TYP 6.6 MOHM MAX
Current	6A MAX

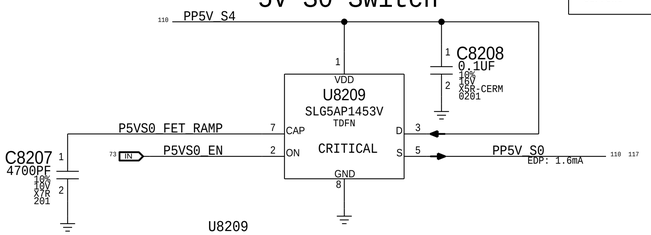
3.3V S0 Switch



U8205

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

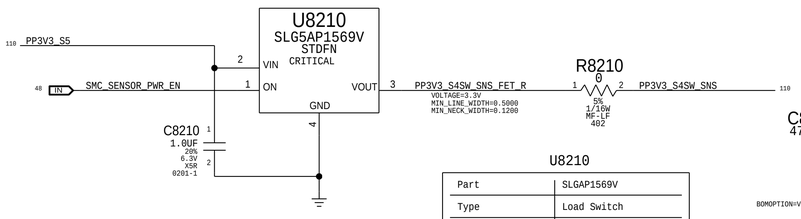
5V S0 Switch



U8209

Part	SLG5AP1453V
Type	Load Switch
R(on)	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A

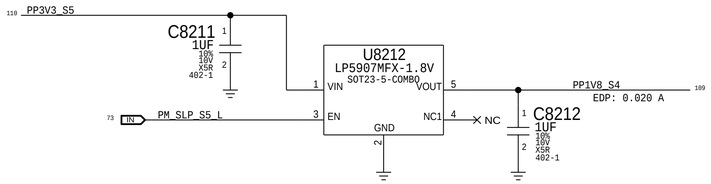
3.3V Sensor Switch



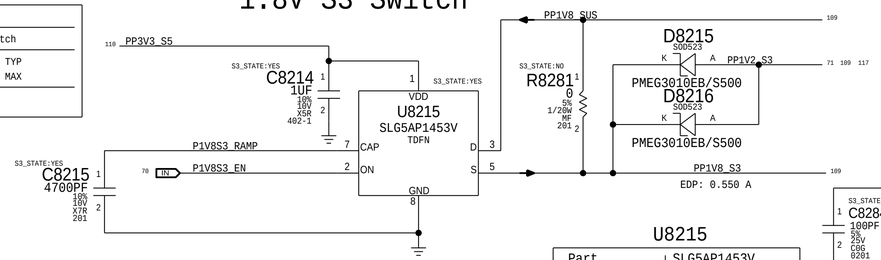
U8210

Part	SLGAP1569V
Type	Load Switch
R(on) @ 3.6V	34 mOhm Typ 46 mOhm Max
Current	1A Max

1.8V S4 LDO



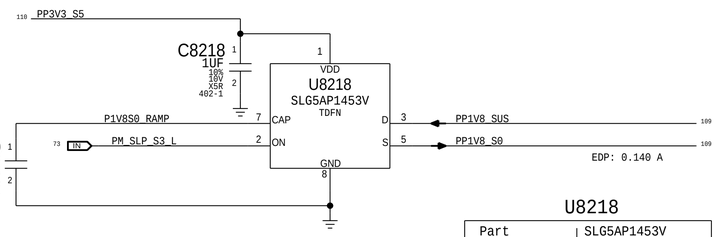
1.8V S3 Switch



U8215

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

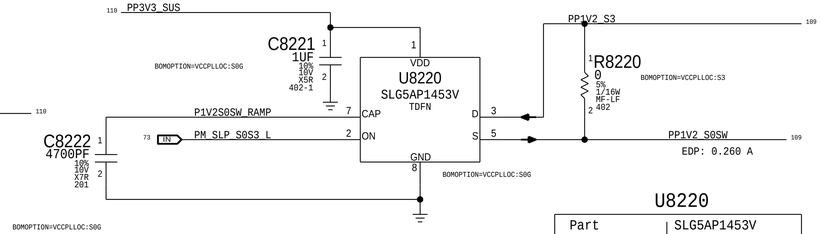
1.8V S0 Switch



U8218

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

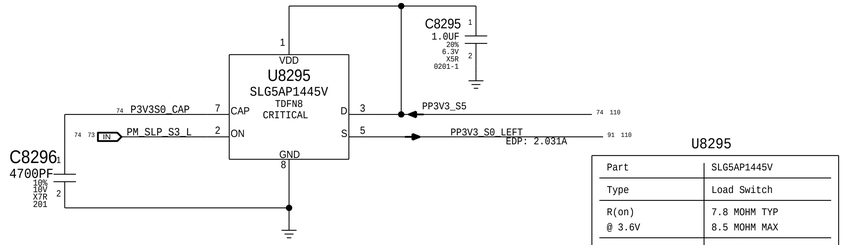
1.2V S0 SW Switch



U8220

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

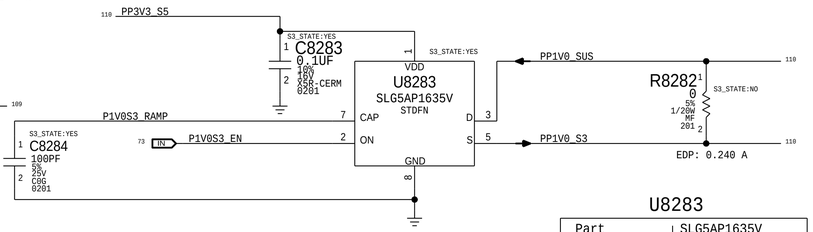
3.3V S0 Switch LEFT



U8295

Part	SLG5AP1445V
Type	Load Switch
R(on) @ 3.6V	7.8 MOHM TYP 8.5 MOHM MAX
Current	4A MAX

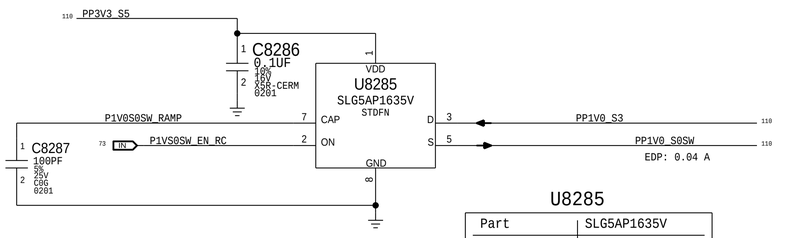
1.0V S3 Switch



U8283

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

1.0V S0 SW Switch



U8285

Part	SLG5AP1635V
Type	Load Switch
R(on) @ 25C	20 mOhm Typ 28 mOhm Max
Current	2.5A Max
Ton Total	39us max @ 1V

BOM_COST_GROUP=PLATFORM POWER

PAGE TITLE
Power FETs

Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	82 OF 145
SHEET	74 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Page Notes

Power aliases required by this page:

- =PPVIN_S0SW_LCDBKLTFET (9-12.6V LCD BACKLIGHT INPUT)
- =PP5V_S0_BKLT (5V BACKLIGHT DRIVER INPUT)

PLATFORM_RESET NO LONGER GATES THE BKLT_EN AS BOTH COME FROM PCH NOW

I2C ID DEDICATED.ONLY CONNECTS TO JERRY

VOUT = 52V TYP, 59V MAX
IOUT = 0.135A TYP, 0.15A MAX
FS = 625KHZ TYP (+/- 7%)

PBUS LINE WIDTHS

LCD BKLT LINE WIDTHS

BOM_COST_GROUP=DISPLAY

PAGE TITLE	LCD Backlight Driver
	Apple Inc.
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	84 OF 145
SHEET	75 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LCD PANEL INTERFACE (eDP) + Camera (MIPI)

U8510 BYPASS

NO STUFF
R8590 0 5% 1/20W MF 0201
EDP_PANEL_PWR_EN (89 76) — PANEL_FET_EN_DLY (76)

NO STUFF
R8591 0 5% 1/20W MF 0201
EDP_PANEL_PWR_EN — BUF_EDP_PANEL_PWR_EN (76 114)

NO STUFF
R8592 0 5% 1/20W MF 0201
(76 64 57 48 29 114) IN SMC_RESET_L — BUF_SMC_RESET_L OUT (46 48 76)

LCD Panel HPD, FSS & AUX strapping

PP3V3_S0
NO_XNET_CONNECTION=1
NO_STUFF
R8503 1M 5% 1/20W MF 201 — EDP_AUXCH_C_N (114 76)

R8505 0 5% 1/20W MF 0201
(114 89) OUT DP_INT_HPD — DP_INT_HPD_R (76)

EDP_AUXCH_C_P (114 76)
NO_XNET_CONNECTION=1
NO_STUFF
R8502 1M 5% 1/20W MF 201

(114 76 89) LCD_FSS
R8504 100K 5% 1/20W MF 201
R8501 100K 5% 1/20W MF 201

PP5V_S0 (110)
CRITICAL
U8500 SLG5AP1443V TDFN
R8515 150K 5% 1/20W MF 201
LCD_PWR_SLEW — CAP (7); ON (2); VDD (1); D (3); S (5); GND (8)
PANEL_P5V_EN
VOLTAGE=5V
PP5V_S0SW_LCD (76 114)
C8515 0.1UF 10% 16V X5R-CERM 0201
C8509 2200PF 10% 10V X7R-CERM 0201
C8511 0.1UF 10% 16V X5R-CERM 0201
C8512 10UF 20% 6.3V X5R-CERM 0402-7

R8517 330 5% 1/20W MF 201
PANEL_P5V_EN_D — D8517 SC2 DSF01S30SCAP

PP3V3_S5 (110)
CRITICAL
U8501 SLG5AP1443V TDFN
LCD_PWR_SLEW_3V3 — CAP (7); ON (2); VDD (1); D (3); S (5); GND (8)
VOLTAGE=3.3V
PP3V3_S0SW_LCD_R
C8513 2200PF 10% 10V X7R-CERM 0201
C8510 1.0UF 20% 6.3V X5R 0201-1

Stuff with 107S0276/107S0020 at Proto
0MIT
R8520 0.005 1% 1/2W MF 0306-SHORT
NO_XNET_CONNECTION=1
PP3V3_S0SW_LCD (76 114)
MIN_NECK_WIDTH=0.2000
MIN_LINE_WIDTH=0.2000
VOLTAGE=3.3V
52 ISNS_LCDPANEL_P
52 ISNS_LCDPANEL_N

R8516 200K 1% 1/20W MF 201
PANEL_P3V3_EN
C8516 0.47UF 10% 6.3V CERM-X5R 0201

R8518 330 5% 1/20W MF 201
PANEL_P3V3_EN_D — D8518 SC2 DSF01S30SCAP

PPVOUT_S0_LCDBKLT (75 76 114 116)
C8500 1000PF 10% 100V X7R-CERM 0603

76 PANEL_FET_EN_DLY
PP3V3_G3H (109 47 46)
CRITICAL
U8510 SLG4AP4998 STQFN
VDD (1)
EDP_PANEL_PWR_EN (89 76) IN — EDP_PANEL_PWR_EN (2)
PM_SLP_S3_L (114 101 89 73 70 46 27 20 12) IN — PM_SLP_S3_L (4)
SMC_RESET_L (114 76 64 57 48 29) IN — SMC_RESET_INPUT_L (12)
PANEL_FET_EN_DLY (3)
PANEL_PWR_EN_CONN (8)
SMC_RESET_OUTPUT_L (9)
X604_DISP_PWR_EN (6)
X604_DISP_SMC_RST_L (10)
NC0 (5) NC_U8510_5
NC1 (11) NC_U8510_11
GND (7)

BUF_SMC_RESET_L — OUT (46 48 76)
DFR_DISP_PWR_EN — OUT (42)
DFR_DISP_SMC_RST_L — OUT (42)
BUF_EDP_PANEL_PWR_EN (76 114)

NO_XNET_CONNECTION=1
J8500 20759-042E-02 F-ST-SM
PPVOUT_S0_LCDBKLT (116 114 76 75) — PWR 43
PP3V3_S0SW_LCD (76 114) — PWR 44

	SIGNAL		
EDP_AUXCH_C_N (114 76)	1	2	
EDP_AUXCH_C_P (114 76)	3	4	BUF_EDP_PANEL_PWR_EN (76 114)
	5	6	DP_INT_HPD_R (76)
EDP_INT_ML_N<0> (76)	7	8	LCD_FSS (76 89 114)
EDP_INT_ML_P<0> (76)	9	10	LCD_IRQ_L OUT (15 114)
	11	12	
EDP_INT_ML_N<1> (76)	13	14	BKLT_PWM_TCON2MLB OUT (48 114)
EDP_INT_ML_P<1> (76)	15	16	BKLT_PWM_MLB2TCON IN (20 114)
	17	18	
EDP_INT_ML_N<2> (76)	19	20	
EDP_INT_ML_P<2> (76)	21	22	
	23	24	I2C_BKLT_SDA BI (111 114)
EDP_INT_ML_N<3> (76)	25	26	I2C_BKLT_SCL IN (111 114)
EDP_INT_ML_P<3> (76)	27	28	SMBUS_SMC_0_S0_SDA BI (49 114)
	29	30	SMBUS_SMC_0_S0_SCL IN (49 114)
MIPI_DATA_CONN_N (38) BI	31	32	
MIPI_DATA_CONN_P (38) BI	33	34	I2C_ALS_SDA BI (42 114)
	35	36	I2C_ALS_SCL IN (42 114)
MIPI_CLK_CONN_N (38) IN	37	38	I2C_CAM_SCL IN (37 38 114)
MIPI_CLK_CONN_P (38) IN	39	40	I2C_CAM_SDA BI (37 38 114)
	41	42	
PWR			
PP5V_S0SW_LCD (114 76)	45	46	PP5V_S0_ALSCAM_F (30 114)
GND			
	47	48	
	49	50	
	51	52	
	53	54	
	55	56	
	57	58	
	59	60	
	61	62	
	63	64	
	65	66	
	67	68	

EDP_INT_ML_P<0> (114 111 IN) = EDP_INT_ML_P<0> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<0> (114 111 IN) = EDP_INT_ML_N<0> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<1> (114 111 IN) = EDP_INT_ML_P<1> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<1> (114 111 IN) = EDP_INT_ML_N<1> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<2> (114 111 IN) = EDP_INT_ML_P<2> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<2> (114 111 IN) = EDP_INT_ML_N<2> (76) MAKE_BASE=TRUE
EDP_INT_ML_P<3> (114 111 IN) = EDP_INT_ML_P<3> (76) MAKE_BASE=TRUE
EDP_INT_ML_N<3> (114 111 IN) = EDP_INT_ML_N<3> (76) MAKE_BASE=TRUE
EDP_AUXCH_C_P (113 111 BI) = EDP_AUXCH_C_P (76 114) MAKE_BASE=TRUE
EDP_AUXCH_C_N (113 111 BI) = EDP_AUXCH_C_N (76 114) MAKE_BASE=TRUE

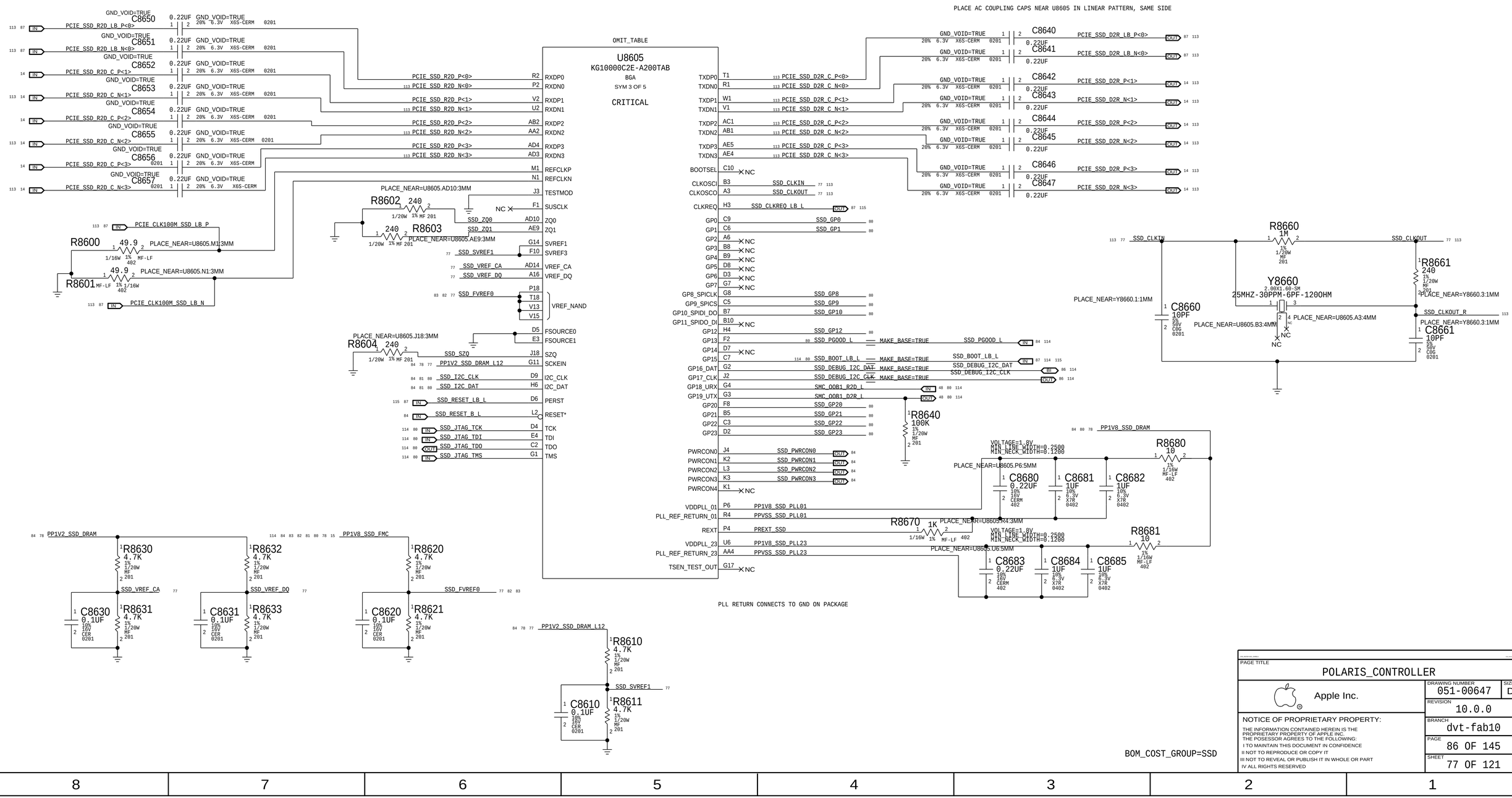
BOM_COST_GROUP=DISPLAY

PAGE TITLE: eDP Display Connector

Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 85 OF 145
SHEET: 76 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


PLACE AC COUPLING CAPS NEAR U8605 IN LINEAR PATTERN, SAME SIDE
U8605
KG10000C2E-A200TAB
BGA
SYM 3 OF 5
CRITICAL
OMIT_TABLE
PLL RETURN CONNECTS TO GND ON PACKAGE
BOM_COST_GROUP=SSD
PAGE TITLE
POLARIS_CONTROLLER
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
86 OF 145
SHEET
77 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U8605
KG10000C2E-A200TAB
BGA
SYM 4 OF 5
CRITICAL

VDD1: B4, B23, AD8, AD21 ← PP1V8_SSD_DRAM (84 80 78 77)
VDD2: A4, A8, A15, A23, C1, J1, AE8, AE14, AE18, AE21 ← PP1V2_SSD_DRAM (84 78 77)
VDD33_ALV33: E2 ← PP3V3_SSD_LIM (86 84 53)
VDD33_UART: E1
C8796 12PF 5% 25V NP0-C0G 0201
C8797 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8795 0.22UF 20% 6.3V X5R 0201

VDD10_ALV: M9, N10, P9, R10, T9 ← PP1V0_SSD_CORE (114 84)
VDD10_SRAM: U10
C8746 12PF 5% 25V NP0-C0G 0201
C8745 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8744 1UF 10% 6.3V X7R 0402
C8743 1UF 10% 6.3V X7R 0402
C8742 0.1UF 10% 16V CER 0201
C8741 0.1UF 10% 16V CER 0201
C8740 0.1UF 10% 16V CER 0201

VDD10_LOG: H17, K9, K11, K13, K15, K17, M11, M15, M17, P11, P15, P17, T11, T13, T15, T17 ← PP1V0_SSD_CORE_L12 (84 78)
C8758 12PF 5% 25V NP0-C0G 0201
C8757 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8756 1UF 10% 6.3V X7R 0402
C8755 1UF 10% 6.3V X7R 0402
C8754 1UF 10% 6.3V X7R 0402
NOSTUFF C8753 0.1UF 10% 16V CER 0201
NOSTUFF C8752 0.1UF 10% 16V CER 0201
C8751 0.1UF 10% 16V CER 0201
C8750 0.1UF 10% 16V CER 0201

L8760 FERR-30-OHM-2.2A-0.035-OHM 0402
VOLTAGE=1.0V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
PP1V0_SSD_CORE_L12 (84 78)
C8761 1UF 10% 6.3V X7R 0402
C8760 0.1UF 10% 16V CER 0201

VDD10_PLL: K8 ← PP1V0_SSD_PLL
VDD11_LVDS: R7 ← PP1V1_SSD_LVDS (78)
VDD12_CKE: F11 ← PP1V2_SSD_DRAM (84 78 77)

VDD12_DDR: G9, G13, H7, H8, H9, H10, H11, H12, H13, H14, H15, H16 ← PP1V2_SSD_DRAM_L12 (84 78 77)
C8774 12PF 5% 25V NP0-C0G 0201
C8773 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8772 1UF 10% 6.3V X7R 0402
C8771 0.22UF 10% 16V CERM 402
C8770 0.1UF 10% 16V CER 0201

VDD18_ALV18: K4, L4, M4 ← PP1V8_SSD_DRAM (77 78 80 84)
VDD18_GPIO: F6, G6 ← PP1V8_SSD_DRAM_L12 (78 84)
VDD18_LVDS: T7 ← PP1V8_SSD_LVDS (78)

VDD18_NAND: F17, F20, J20, K18, L18, N18, N20, R18, U18, V10, V12, V14, V16, V18, Y12, Y18, Y20 ← PP1V8_SSD_FMC (15 77 78 80 81 82 83 84 114)

VDD18_OSC: F4 ← PP1V8_SSD_OSC (78)
VDD18_PLL0: M6 ← PP1V8_SSD_PLL0 (78)
VDD18_PLL1: M7 ← PP1V8_SSD_PLL1 (78)
VDD18_PLL2: K6 ← PP1V8_SSD_PLL2 (78)
VDD18_PLL3: K7 ← PP1V8_SSD_PLL3 (78)
VDD18_TS: G16 ← PP1V8_SSD_FMC (15 77 78 80 81 82 83 84 114)

VDDCA: AE10, AE13, AE15, AE19 ← PP1V2_SSD_DRAM (77 78 84)

VDDIO_01: P8, R8
VDDIO_23_0: U8
VDDIO_23_1: V8
PP1V1_SSD_PCIE (78 84)
C8702 0.1UF 10% 16V CER 0201
C8703 0.1UF 10% 16V CER 0201
C8704 1UF 10% 6.3V X7R 0402
C8705 1UF 10% 6.3V X7R 0402

VDDIO_SENSE_01: T4 ×NC
VDDIO_SENSE_23: AB4 ×NC

VDDQ: A5, A7, A9, A11, A14, A17, A19, A22, C25, D1, D25, H1, H25 ← PP1V2_SSD_DRAM (77 78 84)

PP1V1_SSD_PCIE (84 78)
L8700 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V1_SSD_LVDS (78)
VOLTAGE=1.1V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8700 1UF 10% 6.3V X7R 0402
C8701 0.1UF 10% 16V CER 0201

PP1V8_SSD_DRAM (84 80 78 77)
L8710 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_LVDS (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8710 1UF 10% 6.3V X7R 0402
C8711 0.1UF 10% 16V CER 0201

L8715 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_OSC (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8716 1UF 10% 6.3V X7R 0402
C8715 0.1UF 10% 16V CER 0201

PP1V8_SSD_DRAM_L12 (84 78)
C870C 12PF 5% 25V NP0-C0G 0201
C870D 3.0PF +/-0.1PF 25V NP0-C0G 0201

L8720 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_PLL0 (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8721 1UF 10% 6.3V X7R 0402
C8720 0.1UF 10% 16V CER 0201

L8725 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_PLL1 (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8726 1UF 10% 6.3V X7R 0402
C8725 0.1UF 10% 16V CER 0201

L8730 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_PLL2 (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8731 1UF 10% 6.3V X7R 0402
C8730 0.1UF 10% 16V CER 0201

L8735 FERR-30-OHM-2.2A-0.035-OHM 0402
PP1V8_SSD_PLL3 (78)
VOLTAGE=1.8V MIN_NECK_WIDTH=0.1200 MIN_LINE_WIDTH=0.2000
C8736 1UF 10% 6.3V X7R 0402
C8735 0.1UF 10% 16V CER 0201

PP1V2_SSD_DRAM (84 78 77)
C877B 12PF 5% 25V NP0-C0G 0201
C877A 3.0PF +/-0.1PF 25V NP0-C0G 0201
C8779 1UF 10% 6.3V X7R 0402
C8778 1UF 10% 6.3V X7R 0402
C8777 1UF 10% 6.3V X7R 0402
C8776 0.1UF 10% 16V CER 0201
C8775 0.1UF 10% 16V CER 0201

PP1V8_SSD_DRAM (84 80 78 77)
C8791 1UF 10% 6.3V X7R 0402
C8790 1UF 10% 6.3V X7R 0402

PP1V8_SSD_FMC (114 84 83 82 81 80 78 77 15)
C8784 1UF 10% 6.3V X7R 0402
C8783 1UF 10% 6.3V X7R 0402
C8782 1UF 10% 6.3V X7R 0402
C8781 0.22UF 10% 16V CERM 402
C8780 0.1UF 10% 16V CER 0201

PP3V3_SSD_NAND (84 83 82)
C870A 12PF 5% 25V NP0-C0G 0201
C870B 3.0PF +/-0.1PF 25V NP0-C0G 0201

BOM_COST_GROUP=SSD

PAGE TITLE
POLARIS POWER

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 87 OF 145
SHEET 78 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OMIT_TABLE

U8605

KG10000C2E-A200TAB

BGA

SYM 5 OF 5

CRITICAL

A1	
A2	
A10	
A24	
A25	
B1	
B2	
B6	
B12	
B14	
B21	
B24	
B25	
C4	
C8	
C14	
C16	
C18	
C20	
D10	
D12	
D15	
D23	
E25	
F7	
F9	
F14	
G10	
G15	
G19	
G22	
G24	
H2	
J6	
J7	
J8	
J10	
J12	
J14	
J16	
K19	
K23	
K25	
L6	
L7	
L8	VSSI
L10	
L12	
L14	
L16	
M3	
M8	
M18	
N16	
N23	
N25	
R12	
R14	
R16	
R19	
R24	
U12	
U14	
U16	
U23	
V9	
V11	
V19	
V25	
W10	
W14	
W17	
Y23	
AA25	
AB16	
AB20	
AB23	
AC9	
AC13	
AD11	
AD17	
AD22	
AD24	
AD25	
AE24	
AE25	

L1	
M2	
N2	
N3	
N4	
N6	
N7	
N8	
P1	
P3	
R3	
R6	
T2	
T3	
T6	
T8	
U1	
U3	
U4	
U7	
V3	
V4	VSSIO
V6	
W2	
W3	
W4	
W8	
Y1	
Y2	
Y3	
Y4	
AA1	
AA3	
AB3	
AB5	
AC2	
AC3	
AC4	
AC5	
AD1	
AD2	
AD5	
AD6	
AE1	
AE2	
AE3	
AE6	
AE7	
F3	VSS18_OSC
P7	
V7	VSS_LVDS

BOM_COST_GROUP=SSD

PAGE TITLE

PAGE_TITLE=POLARIS GND

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

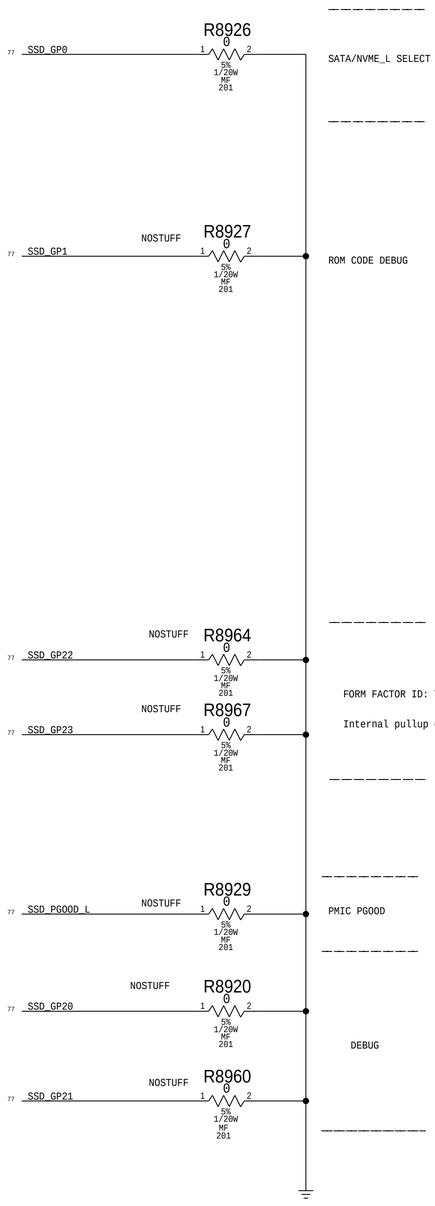
BRANCH dvt-fab10

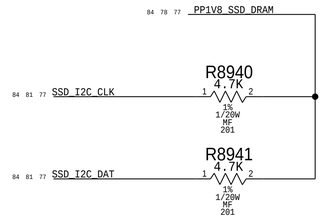
PAGE 88 OF 145

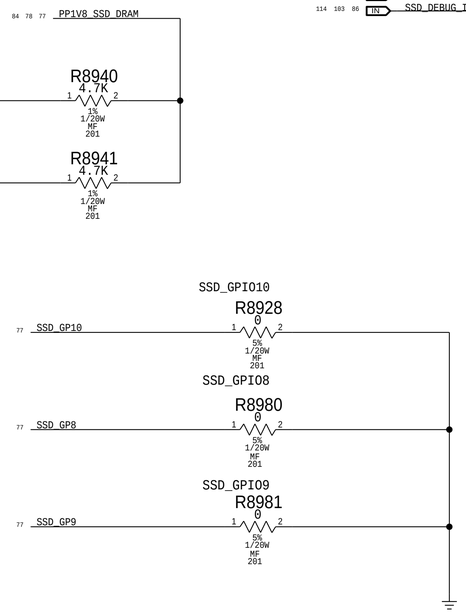
SHEET 79 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED







SSD DENSITY

SSD RELATED BOM Groups

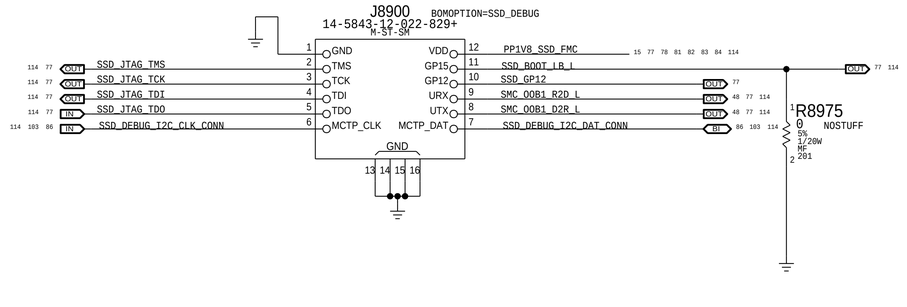
BOM GROUP	BOM OPTIONS
SSD_CONFIG:256GB	SSD_GPIO9,NAND_TYPE:256GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:512GB	SSD_GPIO8,NAND_TYPE:512GB,SSD_CTRL_TYPE:4GBIT
SSD_CONFIG:1TB	NAND_TYPE:1TB,SSD_CTRL_TYPE:8GBIT
SSD_CONFIG:2TB	SSD_GPIO10,NAND_TYPE:2TB,SSD_CTRL_TYPE:8GBIT

NAND Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S00149	4	NAND,1Z,64GBM,TOGG DDR2,64G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:256GB
335S00204	4	NAND,V3,128GBM,TOGG DDR2,256G,SSBGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:512GB
335S00205	4	NAND,V3,256GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:1TB
335S00219	4	NAND,V3,512GBM,TOGG DDR2,256G,SS,BGA 168	U9100,U9110,U9200,U9210	CRITICAL	NAND_TYPE:2TB

SSD Controller Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
339S00154	1	POP,POLARIS+4GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:4GBIT
339S00155	1	POP,POLARIS+8GBIT,SSD CTRL,A2,BGA516	U8605	CRITICAL	SSD_CTRL_TYPE:8GBIT



SSD CONFIGURATIONS

CAPACITY	NAND APN	CONTROLLER APN	R8980/GPIO8	R8981/GPIO9	R8928/GPIO10
128 GB	-	-	STUFF-0	STUFF-0	STUFF-0
256 GB	335S00149	339S00154 (A2 4GB DRAM)	NOSTUFF-1	STUFF-0	NOSTUFF-1
512 GB	335S00204	339S00154 (A2 4GB DRAM)	STUFF-0	NOSTUFF-1	NOSTUFF-1
1 TB	335S00205	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	NOSTUFF-1
2 TB	335S00219	339S00155 (A2 8GB DRAM)	NOSTUFF-1	NOSTUFF-1	STUFF-0

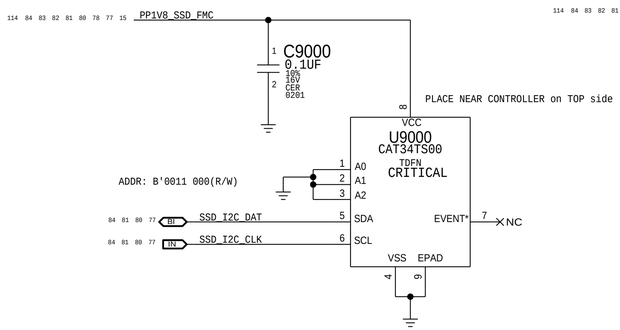
BOM_COST_GROUP=SSD

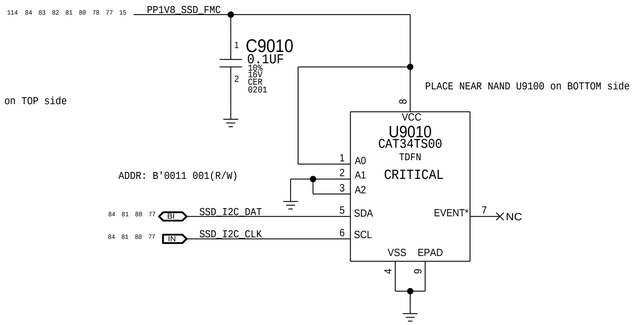
PAGE TITLE: Connector

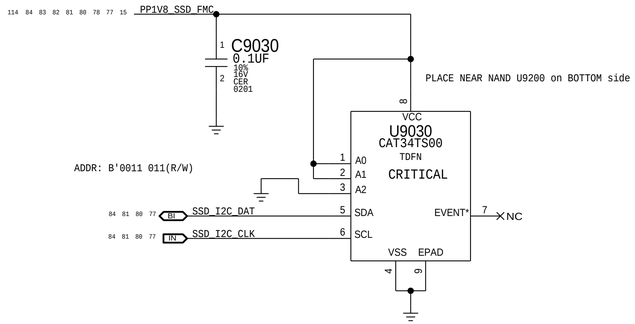
Apple Inc.

DRAWING NUMBER: 051-00647
SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 89 OF 145
SHEET: 80 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED







BOM_COST_GROUP=SSD

PAGE TITLE

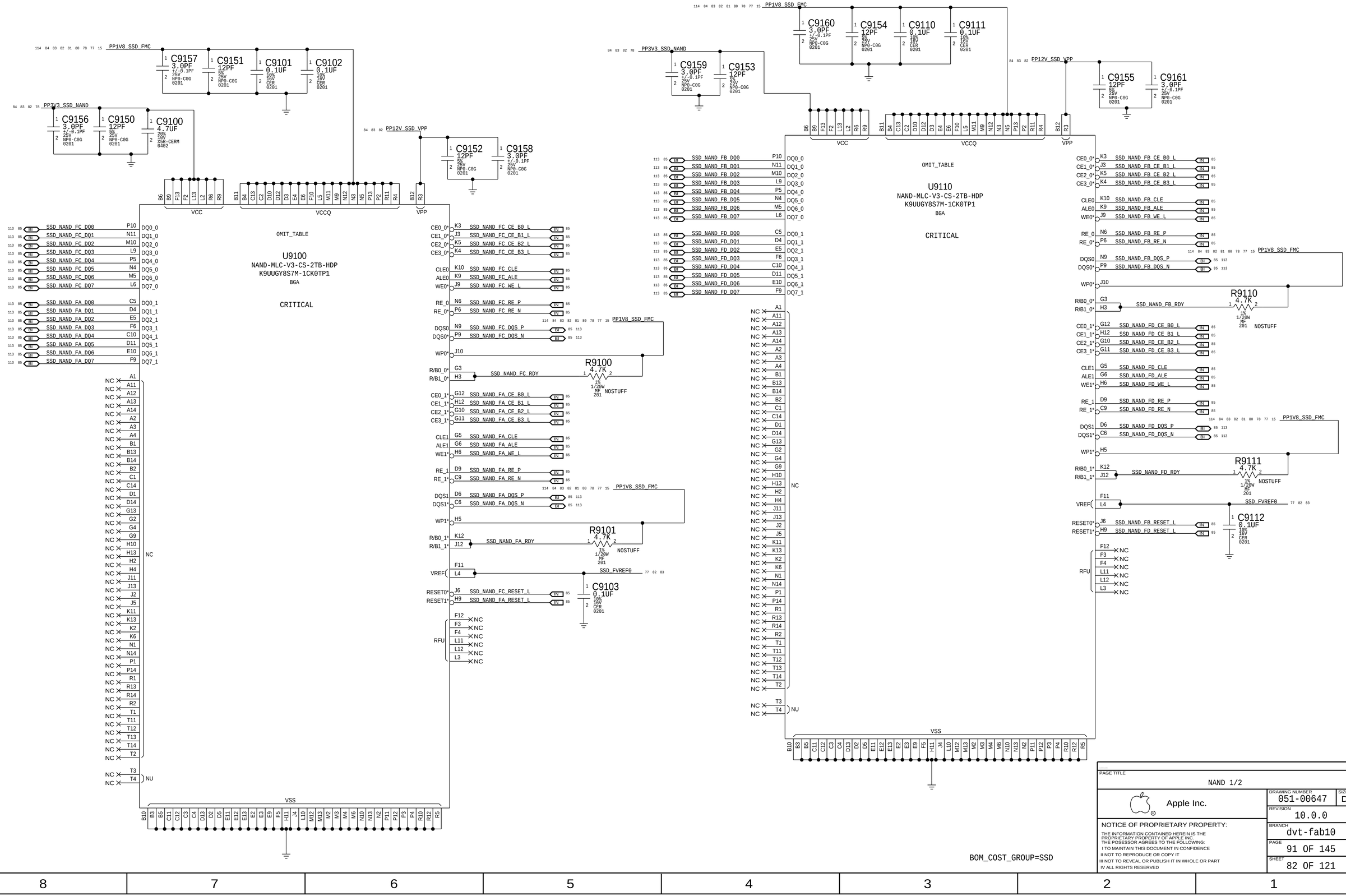
PAGE_TITLE=TEMP SENSORS

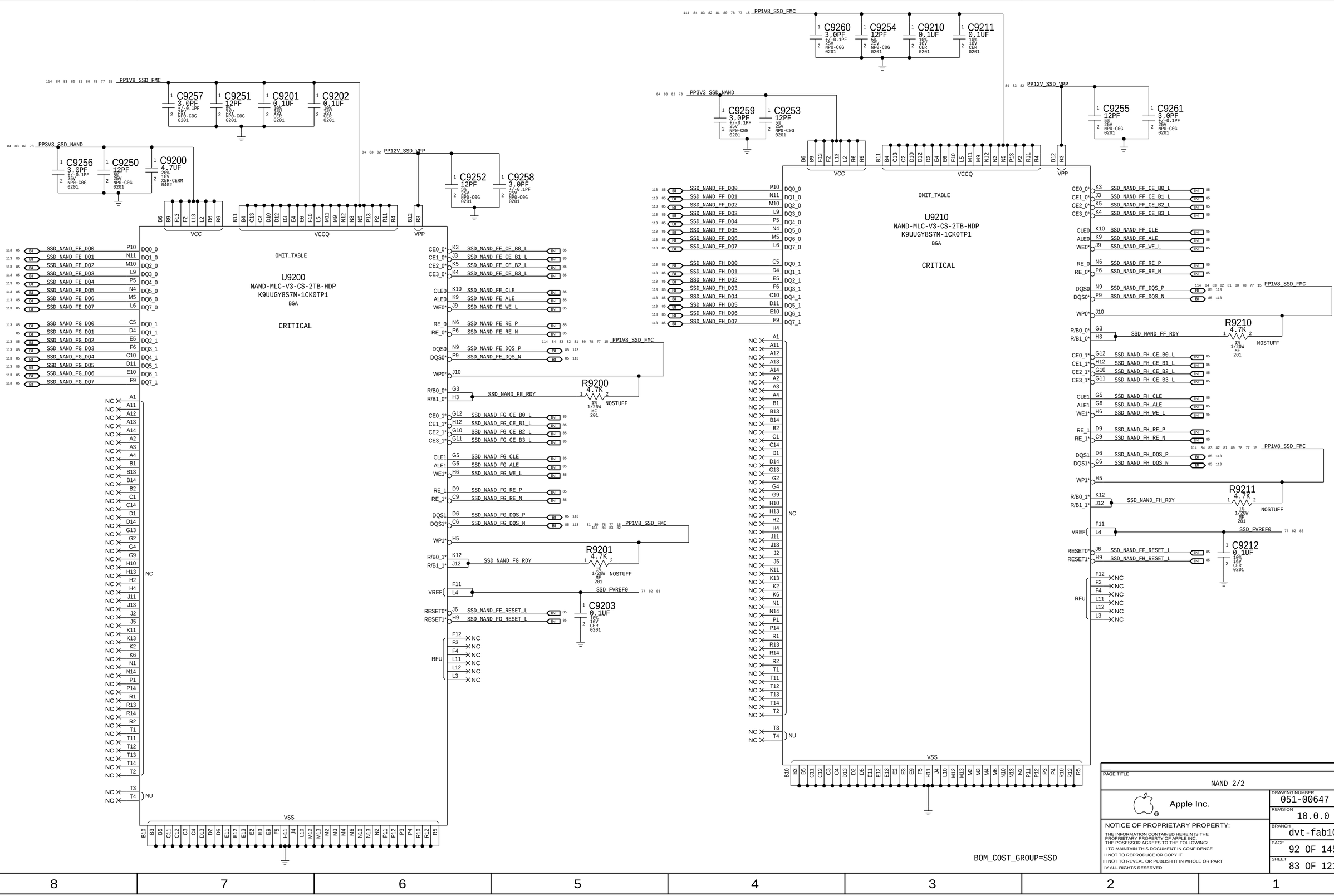
Apple Inc.

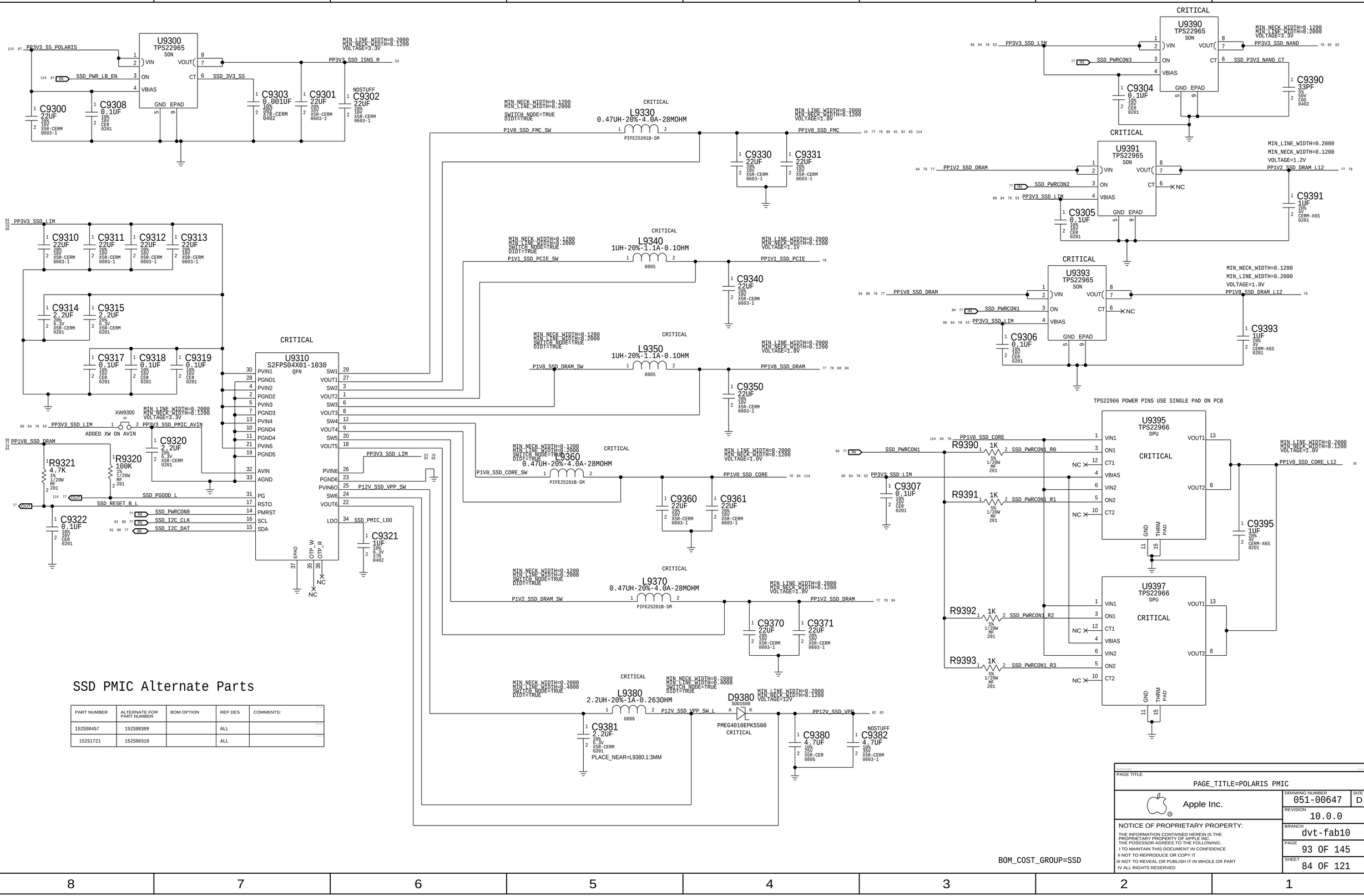
NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 90 OF 145
SHEET 81 OF 121


PP1V8_SSD_FMC
C9157 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9151 12PF 5% 25V NP0-C0G 0201
C9101 0.1UF 10% 16V CER 0201
C9102 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9156 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9150 12PF 5% 25V NP0-C0G 0201
C9100 4.7UF 20% 10V X5R-CERM 0402
PP12V_SSD_VPP
C9152 12PF 5% 25V NP0-C0G 0201
C9158 3.0PF +/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9100
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FC_DQ0 SSD_NAND_FC_DQ1 SSD_NAND_FC_DQ2 SSD_NAND_FC_DQ3 SSD_NAND_FC_DQ4 SSD_NAND_FC_DQ5 SSD_NAND_FC_DQ6 SSD_NAND_FC_DQ7
SSD_NAND_FA_DQ0 SSD_NAND_FA_DQ1 SSD_NAND_FA_DQ2 SSD_NAND_FA_DQ3 SSD_NAND_FA_DQ4 SSD_NAND_FA_DQ5 SSD_NAND_FA_DQ6 SSD_NAND_FA_DQ7
NC
NU
VSS
SSD_NAND_FC_CE_B0_L SSD_NAND_FC_CE_B1_L SSD_NAND_FC_CE_B2_L SSD_NAND_FC_CE_B3_L
SSD_NAND_FC_CLE SSD_NAND_FC_ALE SSD_NAND_FC_WE_L
SSD_NAND_FC_RE_P SSD_NAND_FC_RE_N
SSD_NAND_FC_DQS_P SSD_NAND_FC_DQS_N
SSD_NAND_FC_RDY
R9100 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FA_CE_B0_L SSD_NAND_FA_CE_B1_L SSD_NAND_FA_CE_B2_L SSD_NAND_FA_CE_B3_L
SSD_NAND_FA_CLE SSD_NAND_FA_ALE SSD_NAND_FA_WE_L
SSD_NAND_FA_RE_P SSD_NAND_FA_RE_N
SSD_NAND_FA_DQS_P SSD_NAND_FA_DQS_N
SSD_NAND_FA_RDY
R9101 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
SSD_NAND_FC_RESET_L SSD_NAND_FA_RESET_L
C9103 0.1UF 10% 16V CER 0201
RFU
PP3V3_SSD_NAND
C9159 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9153 12PF 5% 25V NP0-C0G 0201
PP1V8_SSD_FMC
C9160 3.0PF +/-0.1PF 25V NP0-C0G 0201
C9154 12PF 5% 25V NP0-C0G 0201
C9110 0.1UF 10% 16V CER 0201
C9111 0.1UF 10% 16V CER 0201
PP12V_SSD_VPP
C9155 12PF 5% 25V NP0-C0G 0201
C9161 3.0PF +/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9110
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FB_DQ0 SSD_NAND_FB_DQ1 SSD_NAND_FB_DQ2 SSD_NAND_FB_DQ3 SSD_NAND_FB_DQ4 SSD_NAND_FB_DQ5 SSD_NAND_FB_DQ6 SSD_NAND_FB_DQ7
SSD_NAND_FD_DQ0 SSD_NAND_FD_DQ1 SSD_NAND_FD_DQ2 SSD_NAND_FD_DQ3 SSD_NAND_FD_DQ4 SSD_NAND_FD_DQ5 SSD_NAND_FD_DQ6 SSD_NAND_FD_DQ7
NC
NU
VSS
SSD_NAND_FB_CE_B0_L SSD_NAND_FB_CE_B1_L SSD_NAND_FB_CE_B2_L SSD_NAND_FB_CE_B3_L
SSD_NAND_FB_CLE SSD_NAND_FB_ALE SSD_NAND_FB_WE_L
SSD_NAND_FB_RE_P SSD_NAND_FB_RE_N
SSD_NAND_FB_DQS_P SSD_NAND_FB_DQS_N
SSD_NAND_FB_RDY
R9110 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FD_CE_B0_L SSD_NAND_FD_CE_B1_L SSD_NAND_FD_CE_B2_L SSD_NAND_FD_CE_B3_L
SSD_NAND_FD_CLE SSD_NAND_FD_ALE SSD_NAND_FD_WE_L
SSD_NAND_FD_RE_P SSD_NAND_FD_RE_N
SSD_NAND_FD_DQS_P SSD_NAND_FD_DQS_N
SSD_NAND_FD_RDY
R9111 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
SSD_NAND_FB_RESET_L SSD_NAND_FD_RESET_L
C9112 0.1UF 10% 16V CER 0201
RFU
BOM_COST_GROUP=SSD
PAGE TITLE
NAND 1/2
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 91 OF 145
SHEET 82 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


PP1V8_SSD_FMC
C9257 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9251 12PF 5% 25V NP0-C0G 0201
C9201 0.1UF 10% 16V CER 0201
C9202 0.1UF 10% 16V CER 0201
PP3V3_SSD_NAND
C9256 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9250 12PF 5% 25V NP0-C0G 0201
C9200 4.7UF 20% 10V X5R-CERM 0402
PP12V_SSD_VPP
C9252 12PF 5% 25V NP0-C0G 0201
C9258 3.0PF ±/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9200
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FE_DQ0
SSD_NAND_FE_DQ1
SSD_NAND_FE_DQ2
SSD_NAND_FE_DQ3
SSD_NAND_FE_DQ4
SSD_NAND_FE_DQ5
SSD_NAND_FE_DQ6
SSD_NAND_FE_DQ7
SSD_NAND_FG_DQ0
SSD_NAND_FG_DQ1
SSD_NAND_FG_DQ2
SSD_NAND_FG_DQ3
SSD_NAND_FG_DQ4
SSD_NAND_FG_DQ5
SSD_NAND_FG_DQ6
SSD_NAND_FG_DQ7
SSD_NAND_FE_CE_B0_L
SSD_NAND_FE_CE_B1_L
SSD_NAND_FE_CE_B2_L
SSD_NAND_FE_CE_B3_L
SSD_NAND_FE_CLE
SSD_NAND_FE_ALE
SSD_NAND_FE_WE_L
SSD_NAND_FE_RE_P
SSD_NAND_FE_RE_N
SSD_NAND_FE_DQS_P
SSD_NAND_FE_DQS_N
SSD_NAND_FG_RDY
R9200 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FG_CE_B0_L
SSD_NAND_FG_CE_B1_L
SSD_NAND_FG_CE_B2_L
SSD_NAND_FG_CE_B3_L
SSD_NAND_FG_CLE
SSD_NAND_FG_ALE
SSD_NAND_FG_WE_L
SSD_NAND_FG_RE_P
SSD_NAND_FG_RE_N
SSD_NAND_FG_DQS_P
SSD_NAND_FG_DQS_N
R9201 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
C9203 0.1UF 10% 16V CER 0201
SSD_NAND_FE_RESET_L
SSD_NAND_FG_RESET_L
RFU
NC
NU
VSS
PP3V3_SSD_NAND
C9259 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9253 12PF 5% 25V NP0-C0G 0201
C9260 3.0PF ±/-0.1PF 25V NP0-C0G 0201
C9254 12PF 5% 25V NP0-C0G 0201
C9210 0.1UF 10% 16V CER 0201
C9211 0.1UF 10% 16V CER 0201
PP12V_SSD_VPP
C9255 12PF 5% 25V NP0-C0G 0201
C9261 3.0PF ±/-0.1PF 25V NP0-C0G 0201
VCC
VCCQ
VPP
OMIT_TABLE
U9210
NAND-MLC-V3-CS-2TB-HDP
K9UUGY8S7M-1CK0TP1
BGA
CRITICAL
SSD_NAND_FF_DQ0
SSD_NAND_FF_DQ1
SSD_NAND_FF_DQ2
SSD_NAND_FF_DQ3
SSD_NAND_FF_DQ4
SSD_NAND_FF_DQ5
SSD_NAND_FF_DQ6
SSD_NAND_FF_DQ7
SSD_NAND_FH_DQ0
SSD_NAND_FH_DQ1
SSD_NAND_FH_DQ2
SSD_NAND_FH_DQ3
SSD_NAND_FH_DQ4
SSD_NAND_FH_DQ5
SSD_NAND_FH_DQ6
SSD_NAND_FH_DQ7
SSD_NAND_FF_CE_B0_L
SSD_NAND_FF_CE_B1_L
SSD_NAND_FF_CE_B2_L
SSD_NAND_FF_CE_B3_L
SSD_NAND_FF_CLE
SSD_NAND_FF_ALE
SSD_NAND_FF_WE_L
SSD_NAND_FF_RE_P
SSD_NAND_FF_RE_N
SSD_NAND_FF_DQS_P
SSD_NAND_FF_DQS_N
SSD_NAND_FF_RDY
R9210 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_NAND_FH_CE_B0_L
SSD_NAND_FH_CE_B1_L
SSD_NAND_FH_CE_B2_L
SSD_NAND_FH_CE_B3_L
SSD_NAND_FH_CLE
SSD_NAND_FH_ALE
SSD_NAND_FH_WE_L
SSD_NAND_FH_RE_P
SSD_NAND_FH_RE_N
SSD_NAND_FH_DQS_P
SSD_NAND_FH_DQS_N
R9211 4.7K 1% 1/20W MF 201 NOSTUFF
SSD_FVREF0
C9212 0.1UF 10% 16V CER 0201
SSD_NAND_FF_RESET_L
SSD_NAND_FH_RESET_L
RFU
NC
NU
VSS
BOM_COST_GROUP=SSD
PAGE TITLE
NAND 2/2
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 92 OF 145
SHEET 83 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SSD PMIC Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
152S00457	152S00309		ALL	
152S1721	152S00310		ALL	

BOM_COST_GROUP=SSD

PAGE TITLE

PAGE_TITLE=POLARIS PMIC

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

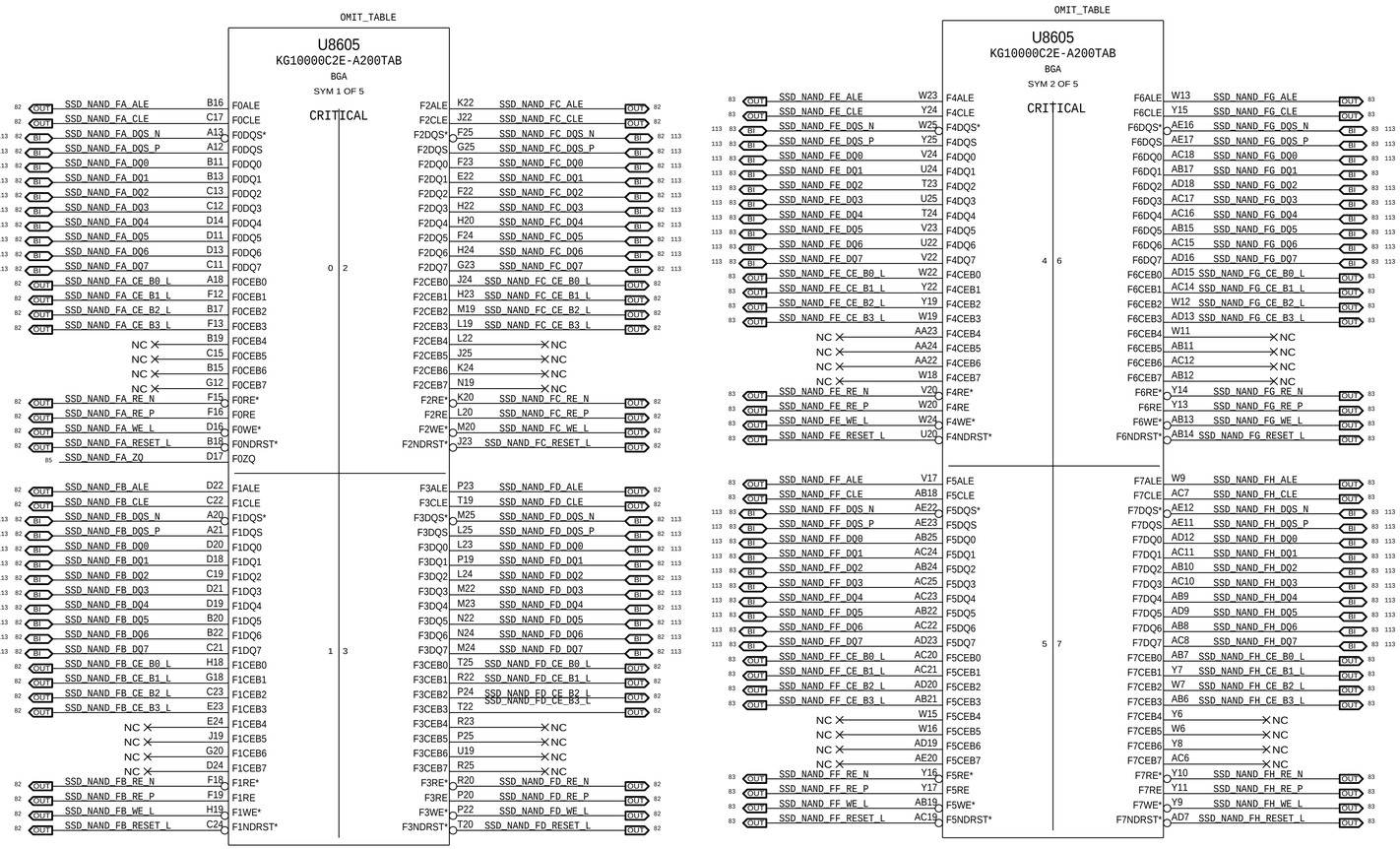
REVISION 10.0.0

BRANCH dvt-fab10

PAGE 93 OF 145

SHEET 84 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



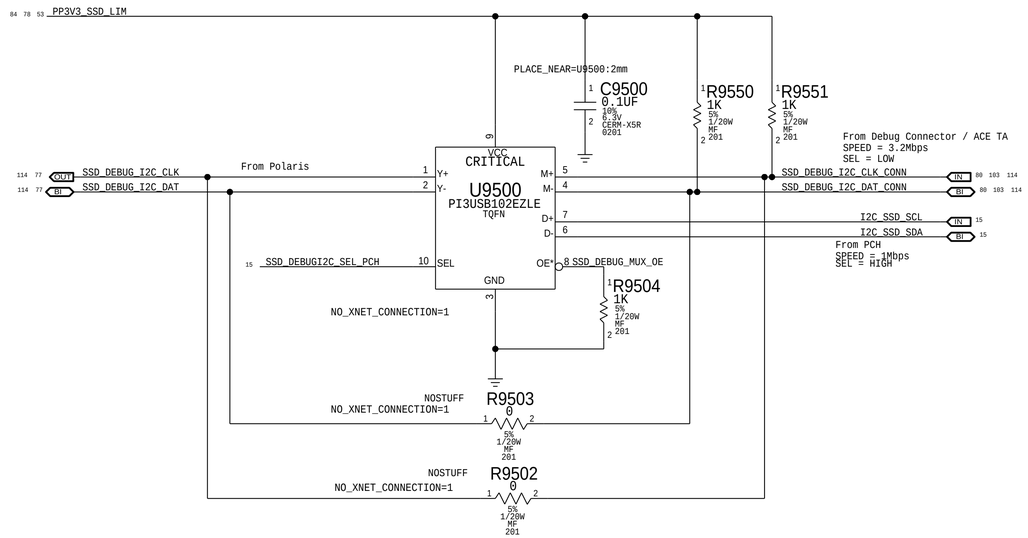
BOM_COST_GROUP=SSD

PAGE TITLE
SSD NAND VR

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 94 OF 145
SHEET 85 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM_COST_GROUP=SSD

PAGE TITLE

SSD SUPPORT

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 95 OF 145

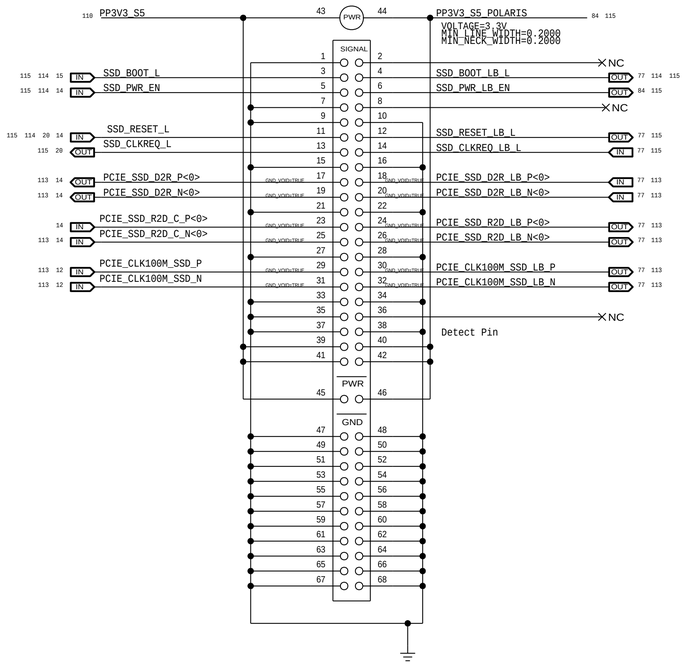
SHEET 86 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LIFEBOAT

J9600
20759-042E-02
F-ST-SM



BOM_COST_GROUP=SSD

SYNC_MASTER=X363_BBABADI
SYNC_DATE=01/20/2016

PAGE TITLE
Lifeboat

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 96 OF 145
SHEET 87 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE TITLE

Constraints

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 97 OF 145

SHEET 88 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

U9800 R4F2113NLG TLP-145V SYM 1 OF 3

OMIT_TABLE

TP_DPMUX_UC_P10	B12	P10/WUE0*	
TP_DPMUX_UC_P11	A13	P11/WUE1*	
TP_DPMUX_UC_P12	A12	P12/WUE2*	
TP_DPMUX_UC_P13	B13	P13/WUE3*	
TP_DPMUX_UC_P14	D11	P14/WUE4*	
TP_DPMUX_UC_P15	C13	P15/WUE5*	
TP_DPMUX_UC_P16	C12	P16/WUE6*	
TP_DPMUX_UC_P17	D10	P17/WUE7*	
EG_RAIL1_EN (91 89 OUT)	D13	P20	
EG_RAIL2_EN (91 89 OUT)	E11	P21	
EG_RAIL3_EN (91 89 OUT)	D12	P22	
EG_RAIL4_EN (91 89 OUT)	F11	P23	
EG_RAIL5_EN (91 89 OUT)	E13	P24	
EG_CLKREQ_SEL_L (98 89 OUT)	E12	P25	
EG_RESET_L (111 89 OUT)	F13	P26	
TP_FB_CLAMP	E10	P27	
LPC_AD<0> (46 12 BI)	A9	P30/LAD0	
LPC_AD<1> (46 12 BI)	D9	P31/LAD1	
LPC_AD<2> (46 12 BI)	C8	P32/LAD2	
LPC_AD<3> (46 12 BI)	B7	P33/LAD3	
LPC_FRAME_L (46 12 IN)	A8	P34/LFRAM*	
DPMUX_LRESET_L (89 20 OUT)	D8	P35/LRESET*	
LPC_CLK24M_DPMUX_UC (20 IN)	D7	P36/LCLK	was 33MHz now 24MHz!!!
TP_DPMUX_UC_P37	D6	P37/SERIRQ	
TP_DPMUX_UC_P40	D4	P40/TMI0/TCMCYI0	
TP_DPMUX_UC_P41	A5	P41/TMO0/TCMCKI0/TCMMCI0	
TP_DPMUX_UC_P42	B4	P42/TCMCYI1	
LCD_FSS (114 76 IN)	A1	P43/TMI1/TCMCKI1/TCMMCI1	
LCD_MUX_SEL (89)	C2	P44/TMO1/PWMU2B/TCMCYI2	
TP_DPMUX_UC_P45	B2	P45/PWMU3B/TCMCKI2/TCMMCI2	
TP_DPMUX_UC_P46	C1	P46/PWMU4B	
TP_DPMUX_UC_P47	C3	P47/PWMU5B	
DPMUX_UC_TX (111 89 OUT)	G2	P50/FTXD	
DPMUX_UC_RX (111 89 IN)	F3	P51/FRXD	
TP_DPMUX_UC_P52	E4	P52/SCL0	

TP_DPMUX_UC_P60	L13	P60/KIN0*	
TP_DPMUX_UC_P61	K12	P61/KIN1*	
TP_DPMUX_UC_P62	K11	P62/KIN2*	
GMUX_SLP_S3_BUF_L (89)	J12	P63/KIN3*	
TP_DPMUX_UC_P64	K13	P64/KIN4*	
TP_DPMUX_UC_P65	J10	P65/KIN5*	
TP_DPMUX_UC_P66	J11	P66/KIN6*	
TP_DPMUX_UC_P67	H12	P67/IRQ7*/KIN7*	
	N10	P70/AN0	NC
	M11	P71/AN1	NC
	L10	P72/AN2	NC
	N11	P73/AN3	NC
	N12	P74/AN4	NC
	M13	P75/AN5	NC
	N13	P76/AN6	NC
	L12	P77/AN7	NC
TP_DPMUX_UC_P80	A7	P80/PME*	
TP_DPMUX_UC_P81	B6	P81/GA20	
TP_DPMUX_UC_P82	C7	P82/CLKRUN*	
TP_DPMUX_UC_P83	D5	P83/LPCPD*	
DPMUX_UC_TX (OUT 111)	A6	P84/IRQ3*/TXD1	
DPMUX_UC_RX (IN 111)	B5	P85/IRQ4*/RXD1	
TP_LCD_IRQ	C6	P86/IRQ5*/SCK1	
GPU_GFX_OVERTEMP (IN 89 99)	J4	P90/IRQ2*	
DP_X_SNK0_HPD (IN 27 29 89)	G3	P91/IRQ1*	
DP_X_SNK1_HPD (IN 27 29)	H2	P92/IRQ0*	
DP_T_SNK0_HPD (IN 101)	G1	P93/IRQ12*	
DP_T_SNK1_HPD (IN 101)	H4	P94/IRQ13*	
SMC_GFX_PWR_LEVEL_L (IN 48 89)	G4	P95/IRQ14*	
GFX_SELF_THROTTLE (IN 89 99)	F4	P96/EXCL	
TP_DPMUX_UC_P97	F1	P97/SDA0/IRQ15*	

U9800 R4F2113NLG TLP-145V SYM 2 OF 3

OMIT_TABLE

I2C_DPMUX_UC_SDA (49 BI)	N3	PA0/KIN8*/SDA1	
I2C_DPMUX_UC_SCL (49 OUT)	N1	PA1/KIN9*/SCL1	
DPMUX_UC_IRQ (20 OUT)	M3	PA2/KIN10*/PS2AC	
	M2	PA3/KIN11*/PS2AD	NC
	N2	PA4/KIN12*/PS2BC	NC
	L1	PA5/KIN13*/PS2BD	NC
SMC_GFX_OVERTEMP (89 48 46 OUT)	K3	PA6/KIN14*/PS2CC	
TP_FB_CLAMP_TOGGLE_REQ_L	L2	PA7/KIN15*/PS2CD	
TP_DPA_EG_HPD	B8	PB0/LSMI*	
DP_X_SNK0_HPD_EG (99 89 OUT)	C9	PB1/LSCI	
DP_X_SNK1_HPD_EG (99 89 OUT)	B9	PB2/RI*/PWMU0B	
DP_T_SNK0_HPD_EG (99 89 OUT)	A10	PB3/DCD*/PWMU1B	
DP_T_SNK1_HPD_EG (99 89 OUT)	C10	PB4/DSR*/FSIDO	
GPU_GFX_PWR_LEVEL_L (99 OUT)	B10	PB5/DTR*/FSIDI	
SMC_GFX_SELF_THROTTLE (89 46 OUT)	C11	PB6/CTS*/FSICK	
DP_INT_EG_HPD (99 89 OUT)	A11	PB7/RTS*/FSISS	
EDP_PANEL_PWR_EN (89 76 OUT)	G11	PC0/TIOCA0/WUE8*	
EDP_BKLT_EN (89 75 OUT)	G13	PC1/TIOCB0/WUE9*	
TP_DPMUX_UC_PC2	F12	PC2/TIOCC0/TCLKA/WUE10*	
TP_DPMUX_UC_PC3	H13	PC3/TIOCD0/TCLKB/WUE11*	
LCD_MUX_EN (89)	G10	PC4/TIOCA1/WUE12*	
TP_LCD_MUX_REQ	G12	PC5/TIOCB1/TCLKC/WUE13*	
BKLT_PWM_MLB2TCON (89 20 OUT)	H11	PC6/TIOCA2/WUE14*	
TP_DPMUX_UC_PC7	J13	PC7/TIOCB2/TCLKD/WUE15*	
TP_DPA_IG_HPD	M10	PD0/AN8	
DP_X_SNK0_HPD_IG (89 15 OUT)	N9	PD1/AN9	
DP_X_SNK1_HPD_IG (89 15 OUT)	K10	PD2/AN10	
DP_T_SNK0_HPD_IG (89 15 OUT)	L8	PD3/AN11	
DP_T_SNK1_HPD_IG (89 15 OUT)	M9	PD4/SSO	
TP_DPMUX_UC_PD5	N8	PD5/SSI	
TP_DPMUX_UC_PD6	K9	PD6/SSCK	
DP_INT_IG_HPD (89 15 OUT)	L7	PD7/SCS	

DPMUX_UC_CLK32K (89)	K1	PE0/EXEXCL	
DPMUX_UC_TCK (89)	J3	PE1/ETCK	
DPMUX_UC_TDI (89)	K2	PE2/ETDI	
DPMUX_UC_TDO (89)	J1	PE3/ETDO	
DPMUX_UC_TMS (89)	K4	PE4/ETMS	
DPMUX_UC_TRST_L (89)	H3	PE5/ETRST*	
EG_LCD_PWR_EN (IN 89)	K5	PF0/IRQ8*/PWMU0A	
EG_BKLT_EN (IN 89)	N5	PF1/IRQ9*/PWMU1A	
PM_ALL_GPU_PGOOD (IN 91)	M6	PF2/IRQ10*/TMOY	
P5_S0GPU_PGOOD (IN 91)	L5	PF3/IRQ11*/TMOX	
GPUVCORE_PGOOD (IN 91)	M5	PF4/PWMU2A/EXDSR	
PVDDCI_PGOOD (IN 91)	N4	PF5/PWMU3A/EXDTR	
P1V8GPU_PGOOD (IN 91)	L4	PF6/PWMU4A/EXCTS	
P3V3_S0GPU_PGOOD (IN 91)	M4	PF7/PWMU5A/EXRTS	
NC_I2C_DPMUX_A_SDA (BI 49)	M8	PG0/EXIRQ8*/TMIX/SDAA	
NC_I2C_DPMUX_A_SCL (OUT 49)	N7	PG1/EXIRQ9*/TMIY/SCLA	
	K8	PG2/EXIRQ10*/SDAB	NC
	K7	PG3/EXIRQ11*/SCLB	NC
	K6	PG4/EXIRQ12*/SDAC	NC
DPMUX_LRESET_L (IN 20 89)	N6	PG5/EXIRQ13*/SCLC	
TP_DPMUX_UC_PG6	M7	PG6/EXIRQ14*/SDAD	
DP_INT_HPD (IN 76 114)	L6	PG7/EXIRQ15*/SCLD	
EDP_IG_PANEL_PWR_EN (IN 15)	E2	PH0/IRQ6*	
EDP_IG_BKLT_EN (IN 15)	F2	PH1/EXIRQ7*	
DPMUX_UC_PECI (89)	A4	PECI	
DPMUX_UC_PEVREF (89)	B3	PEVREF	

R9894 0 5% 1/20W MF 201

DPMUX_UC_MD2_R (1) — (2) DPMUX_UC_MD2 (89)

Q9890 DMN32D2LFB4

DFN1006H4-3 SYM_VER_2

D=3, G=1, S=2

DPMUX_UC_MD1 (89)

R9801 0 5% 1/16W MF-LF 402

PP3V3_S4 (110) — PP3V3_S3_DPMUX_UC_R (89)

MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V

R9800 0 5% 1/16W MF-LF 402

PP3V3_S0 (110 98 89 49) — PP3V3_S0_DPMUX_UC_R (89)

MIN_LINE_WIDTH=0.3000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V

C9800 / C9801 / C9802 / C9803 0.1UF 20% 10V X7R-CERM 0402

C9804 0.1UF 20% 10V X7R-CERM 0402

DPMUX_UC_RESET_L (89)

R9802 NOSTUFF 0 5% 1/16W MF-LF 402

DPMUX_LRESET_L (89 20)

DPMUX_UC_VCL

C9805 0.47UF 10% 6.3V X6S-CERM 0402

U9800 R4F2113NLG TLP-145V SYM 3 OF 3

OMIT_TABLE

	M12	AVCC	
	B1	VCC	
	M1	VCC	
	H10	VCC	
	E1	VCL	
	L11	AVREF	
	J2	VBAT	
	D3	RES*	
DPMUX_UC_XTAL (113 89)	A3	XTAL	
DPMUX_UC_EXTAL (113 89)	A2	EXTAL	
DPMUX_UC_MDCKN (89)	C4	MDCKN	
DPMUX_UC_MD1 (89)	D1	MD1	
DPMUX_UC_MD2 (89)	H1	MD2	
DPMUX_UC_NMI (89)	E3	NMI	
	E5	NC	NC
	D2	VSS	
	L3	VSS	
	F10	VSS	
	C5	VSS	
	B11	VSS	
	L9	AVSS	

R9850 10K 5% 1/20W MF 201

DPMUX_XTAL:NO

DPMUX UC PULL-UPS

DPMUX_UC_NMI (89)	R9810	10K	
DPMUX_UC_TRST_L (89)	R9811	10K	
DPMUX_UC_MD1 (89)	R9812	10K	
DPMUX_UC_MD2 (89)	R9813	10K	
DPMUX_UC_CLK32K (89)	R9814	10K	
DPMUX_UC_TCK (89)	R9815	10K	
DPMUX_UC_TDI (89)	R9816	10K	
DPMUX_UC_TDO (89)	R9817	10K	
DPMUX_UC_TMS (89)	R9818	10K	
EG_CLKREQ_SEL_L (98 89)	R9819	100K	
SMC_GFX_PWR_LEVEL_L (89 48)	R9842	100K	
LCD_MUX_EN (89)	R9855	10K	
LCD_MUX_SEL (89)	R9856	10K	NOSTUFF
DPMUX_UC_RESET_L (89)	R9840	100K	NOSTUFF
	R9841	0	GMUX_SLP_S3_BUF_L (89)

PP3V3_S0 (110 98 89 49) — 5% 1/20W MF 201

C9870 0.1UF 10% 6.3V X7R 0201

PP3V3_S5 (116)

U9870 74LVC1G07GF SOT891

VCC, GND

PM_SLP_S3_L (114 101 76 73 70 46 27 20 12) — A — Y — GMUX_SLP_S3_BUF_L (89)

NC — 1 — NC — 5 — NC

R9870 4.7K 5% 1/20W MF 201

PP3V3_S0 (49 89 98 110)

R9871 NOSTUFF 470K 5% 1/20W MF 201

GMUX_SLP_S3_BUF_L — MAKE_BASE=TRUE — GMUX_SLP_S3_BUF_L (89)

DPMUX UC DEBUG HEADER

J9800 1909782 M-RT-SM

PP3V3_S0_DPMUX_UC_R (89)	1	
DPMUX_UC_TX (111 89)	2	
DPMUX_UC_RX (111 89)	3	
DPMUX_UC_RESET_L (89)	4	
	5	
DPMUX_UC_MD1 (89)	6	
	7	
	8	DPMUX_DEBUG

PP3V3_S0 (49 89 98 110)

R9890 10K 5% 1/20W MF 201

DPMUX_XTAL:YES — DPMUX_UC_MDCKN (89)

R9891 10K 5% 1/20W MF 201

DPMUX_XTAL:NO

DPMUX_XTAL:YES

R9892 0 5% 1/20W MF 201

DBG_XTAL

Y9800 1.60X1.20MM-SM

24.000MHZ-38PPM-9.5PF-600HM

DPMUX_UC_XTAL_R (113) — 1 — 2 — 3 — 4 — DPMUX_UC_EXTAL_R (113)

DPMUX_XTAL:YES

R9893 0 5% 1/20W MF 201

DPMUX_UC_XTAL (89 113)

DPMUX_UC_EXTAL (89 113)

DBG_XTAL

C9890 12PF 5% 50V C0G-CERM 0201

DBG_XTAL

C9891 12PF 5% 50V C0G-CERM 0201

DP 2:1 ANALOG MUX

PP3V3_S0 (110)

C9850 / C9851 0.1UF 20% 10V X7R-CERM 0402

U9850 CBTL06142EEE TFBGA

CRITICAL

DP_INT_IG_ML_P<0> (113 5 IN)	B4	DIN1_0+	
DP_INT_IG_ML_N<0> (113 5 IN)	A4	DIN1_0-	
DP_INT_IG_ML_P<1> (113 5 IN)	B5	DIN1_1+	
DP_INT_IG_ML_N<1> (113 5 IN)	A5	DIN1_1-	
DP_INT_IG_ML_P<2> (113 5 IN)	B6	DIN1_2+	
DP_INT_IG_ML_N<2> (113 5 IN)	A6	DIN1_2-	
DP_INT_IG_ML_P<3> (113 5 IN)	A8	DIN1_3+	
DP_INT_IG_ML_N<3> (113 5 IN)	A9	DIN1_3-	
DP_INT_IG_AUX_P (113 5 BI)	H9	DAUX1+	
DP_INT_IG_AUX_N (113 5 BI)	J9	DAUX1-	
	H8	DDC_CLK1	NC
	J8	DDC_DAT1	NC
	J2	HPD_1	NC
DP_INT_EG_ML_P<0> (113 99 IN)	B8	DIN2_0+	
DP_INT_EG_ML_N<0> (113 99 IN)	B9	DIN2_0-	
DP_INT_EG_ML_P<1> (113 99 IN)	D8	DIN2_1+	
DP_INT_EG_ML_N<1> (113 99 IN)	D9	DIN2_1-	
DP_INT_EG_ML_P<2> (113 99 IN)	E8	DIN2_2+	
DP_INT_EG_ML_N<2> (113 99 IN)	E9	DIN2_2-	
DP_INT_EG_ML_P<3> (113 99 IN)	F8	DIN2_3+	
DP_INT_EG_ML_N<3> (113 99 IN)	F9	DIN2_3-	
DP_INT_EG_AUX_P (113 99 BI)	H6	DAUX2+	
DP_INT_EG_AUX_N (113 99 BI)	J6	DAUX2-	
	H5	DDC_CLK2	NC
	J5	DDC_DAT2	NC
	H3	HPD_2	NC
LCD_MUX_SEL (89)	A1	GPU_SEL	
LCD_MUX_EN (89)	B7	XSD*	
	C2	DDC_AUX_SEL	
	B3 C8 G8 H4 H7 C2	GND GND GND GND GND GND	

EDP_INT_ML_P<0> (OUT 111)	B2	DOUT_0+	
EDP_INT_ML_N<0> (OUT 111)	B1	DOUT_0-	
EDP_INT_ML_P<1> (OUT 111)	D2	DOUT_1+	
EDP_INT_ML_N<1> (OUT 111)	D1	DOUT_1-	
EDP_INT_ML_P<2> (OUT 111)	E2	DOUT_2+	
EDP_INT_ML_N<2> (OUT 111)	E1	DOUT_2-	
EDP_INT_ML_P<3> (OUT 111)	F2	DOUT_3+	
EDP_INT_ML_N<3> (OUT 111)	F1	DOUT_3-	
EDP_AUXCH_C_P (BI 111)	H2	AUX+	
EDP_AUXCH_C_N (BI 111)	H1	AUX-	
DPMUX_HPD_PD	J1	HPDIN	

R9862 100K 1% 1/20W MF 201

DPMUX UC PULL-DOWNS

DPMUX_UC_RESET_L (89)	R9820	10K	NOSTUFF
EG_RAIL1_EN (91 89)	R9821	10K	
EG_RAIL2_EN (91 89)	R9822	10K	
EG_RAIL3_EN (91 89)	R9823	10K	
EG_RAIL4_EN (91 89)	R9824	10K	
EG_RAIL5_EN (91 89)	R9825	10K	
EDP_PANEL_PWR_EN (89 76)	R9826	10K	
EDP_BKLT_EN (89 75)	R9827	10K	
BKLT_PWM_MLB2TCON (89 20)	R9828	10K	
DPMUX_UC_NMI (89)	R9829	10K	NOSTUFF
DPMUX_UC_MD1 (89)	R9830	10K	NOSTUFF
DPMUX_UC_MD2 (89)	R9831	10K	NOSTUFF
DPMUX_UC_PECI (89)	R9832	10K	
DPMUX_UC_PEVREF (89)	R9833	10K	
EG_RESET_L (111 89)	R9835	100K	
DP_X_SNK0_HPD_IG (89 15)	R9836	100K	
DP_X_SNK0_HPD_EG (99 89)	R9837	100K	
DP_X_SNK1_HPD_IG (89 15)	R9838	100K	
DP_X_SNK1_HPD_EG (99 89)	R9839	100K	
DP_INT_IG_HPD (89 15)	R9845	100K	
DP_INT_EG_HPD (99 89)	R9846	100K	
GPU_GFX_OVERTEMP (99 89)	R9847	100K	
GFX_SELF_THROTTLE (99 89)	R9848	100K	
SMC_GFX_OVERTEMP (89 48 46)	R9849	100K	
SMC_GFX_SELF_THROTTLE (89 46)	R9852	100K	
LCD_MUX_SEL (89)	R9853	100K	
LCD_MUX_EN (89)	R9854	100K	NOSTUFF

DP_T_SNK0_HPD_IG (89 15)	R9872	100K
DP_T_SNK0_HPD_EG (99 89)	R9873	100K
DP_T_SNK1_HPD_IG (89 15)	R9874	100K
DP_T_SNK1_HPD_EG (99 89)	R9875	100K

BOM_COST_GROUP=GRAPHICS

SYNC_MASTER=dpmux — SYNC_DATE=08/22/2015

PAGE TITLE: eDP Mux

Apple Inc.

DRAWING NUMBER: 051-00647 — SIZE: D

REVISION: 10.0.0

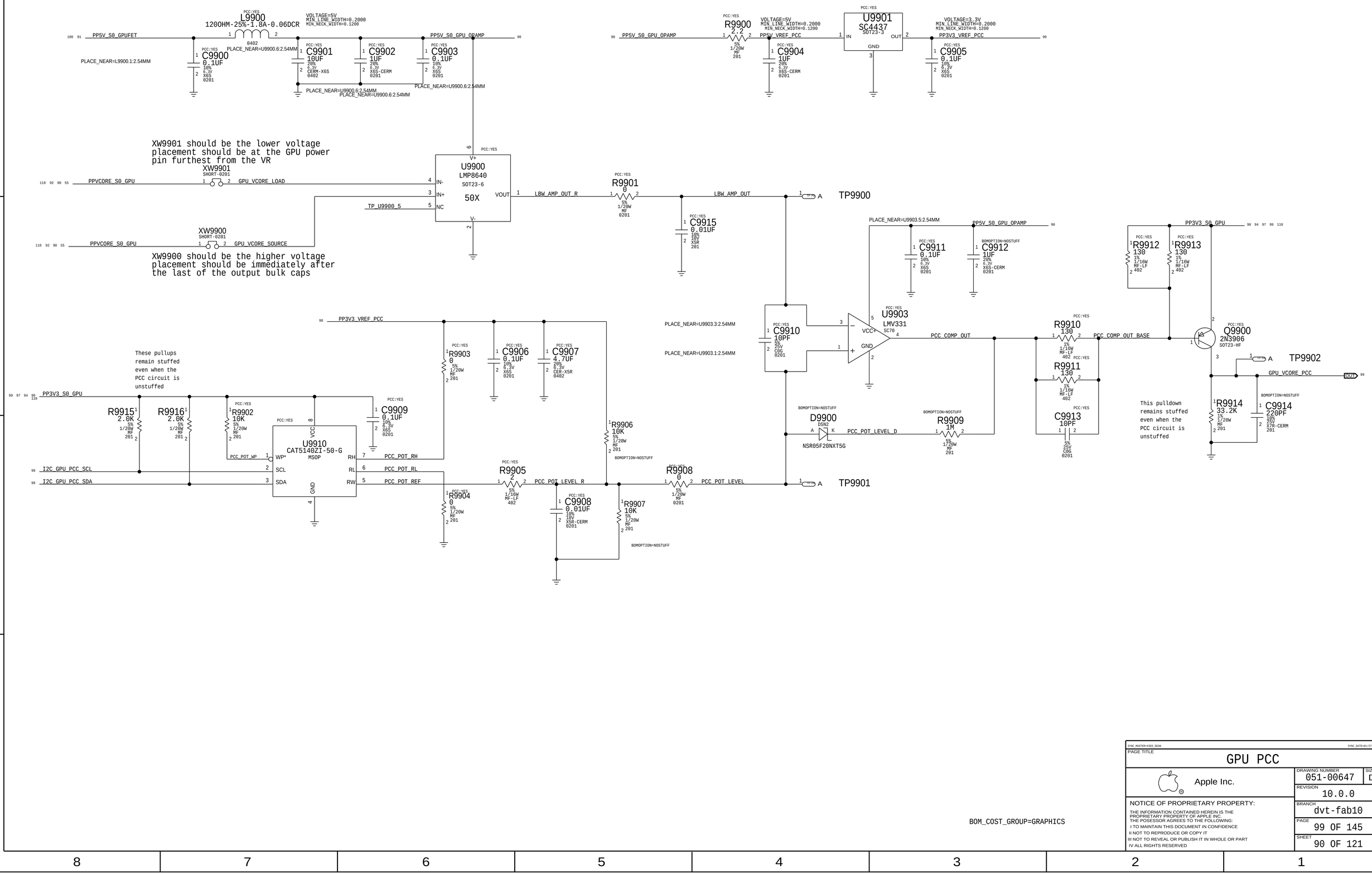
BRANCH: dvt-fab10

PAGE: 98 OF 145

SHEET: 89 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=X363_SEAN SYNC_DATE=01/27/2016

PAGE TITLE

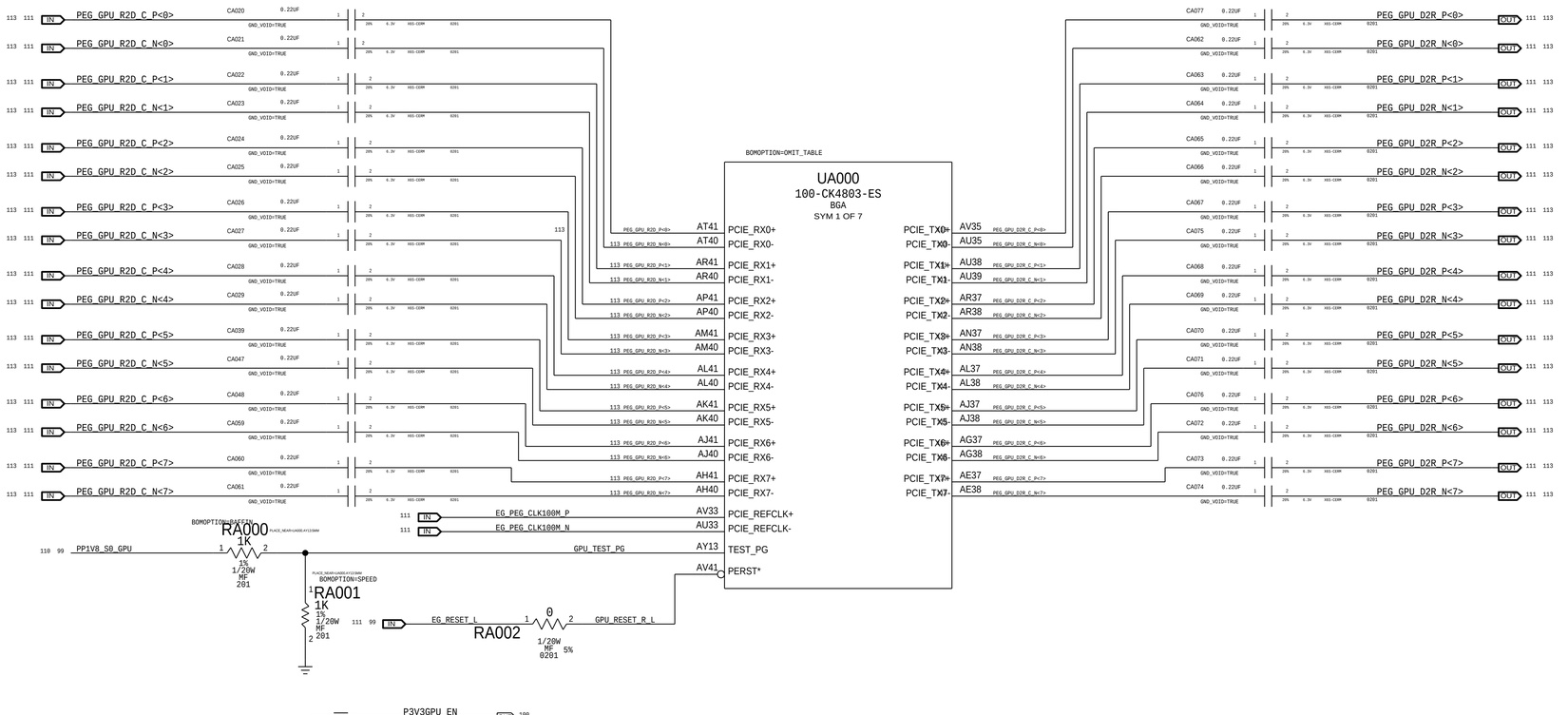
GPU PCC

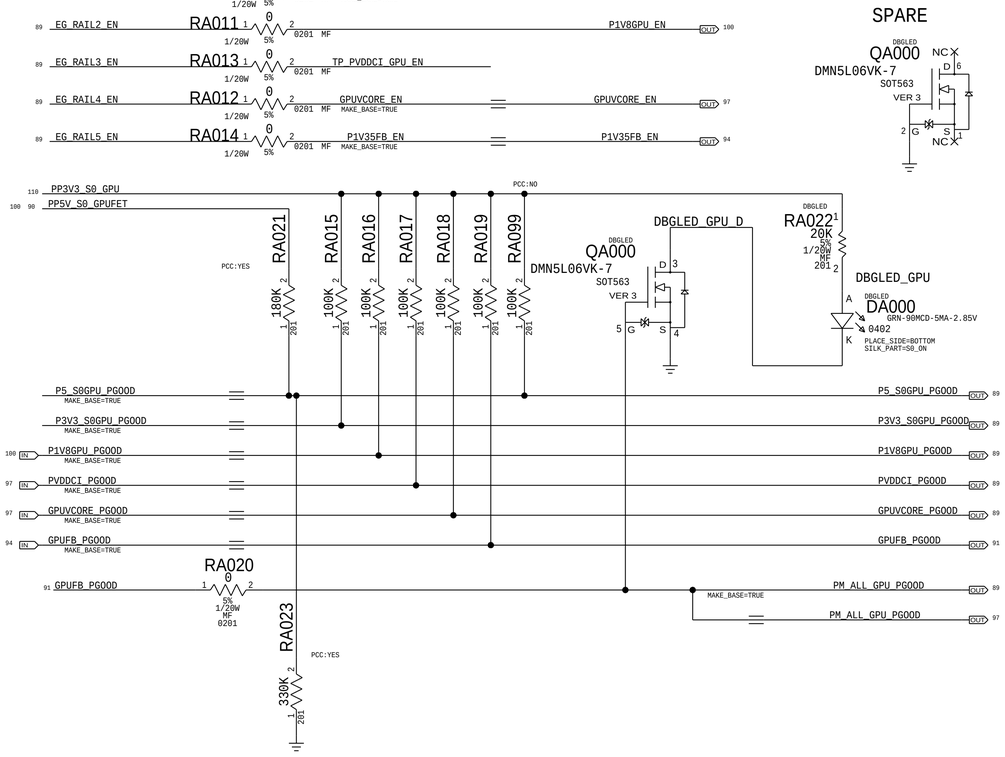
Apple Inc.

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	99 OF 145
SHEET	90 OF 121

NOTICE OF PROPRIETARY PROPERTY:

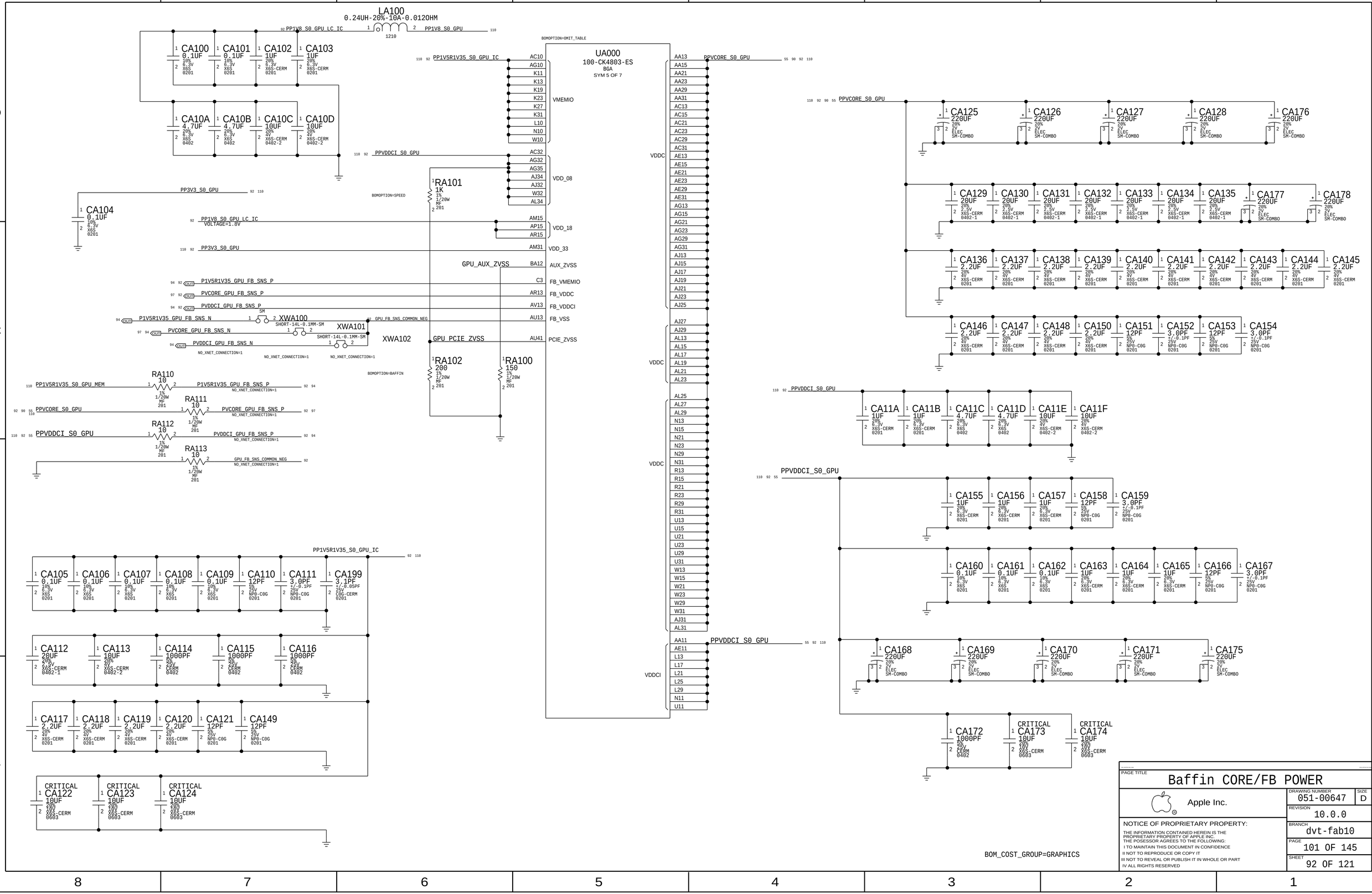
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

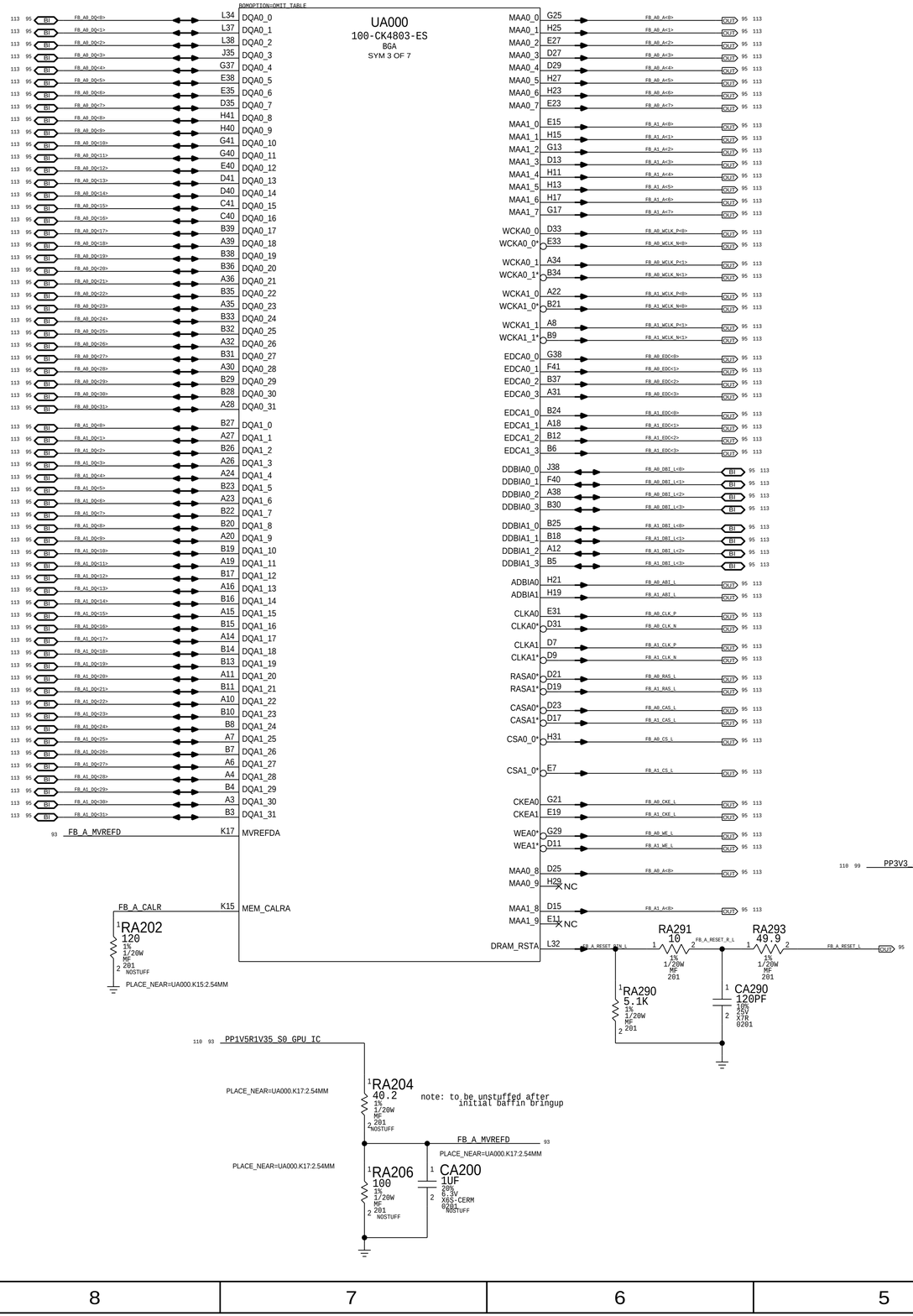


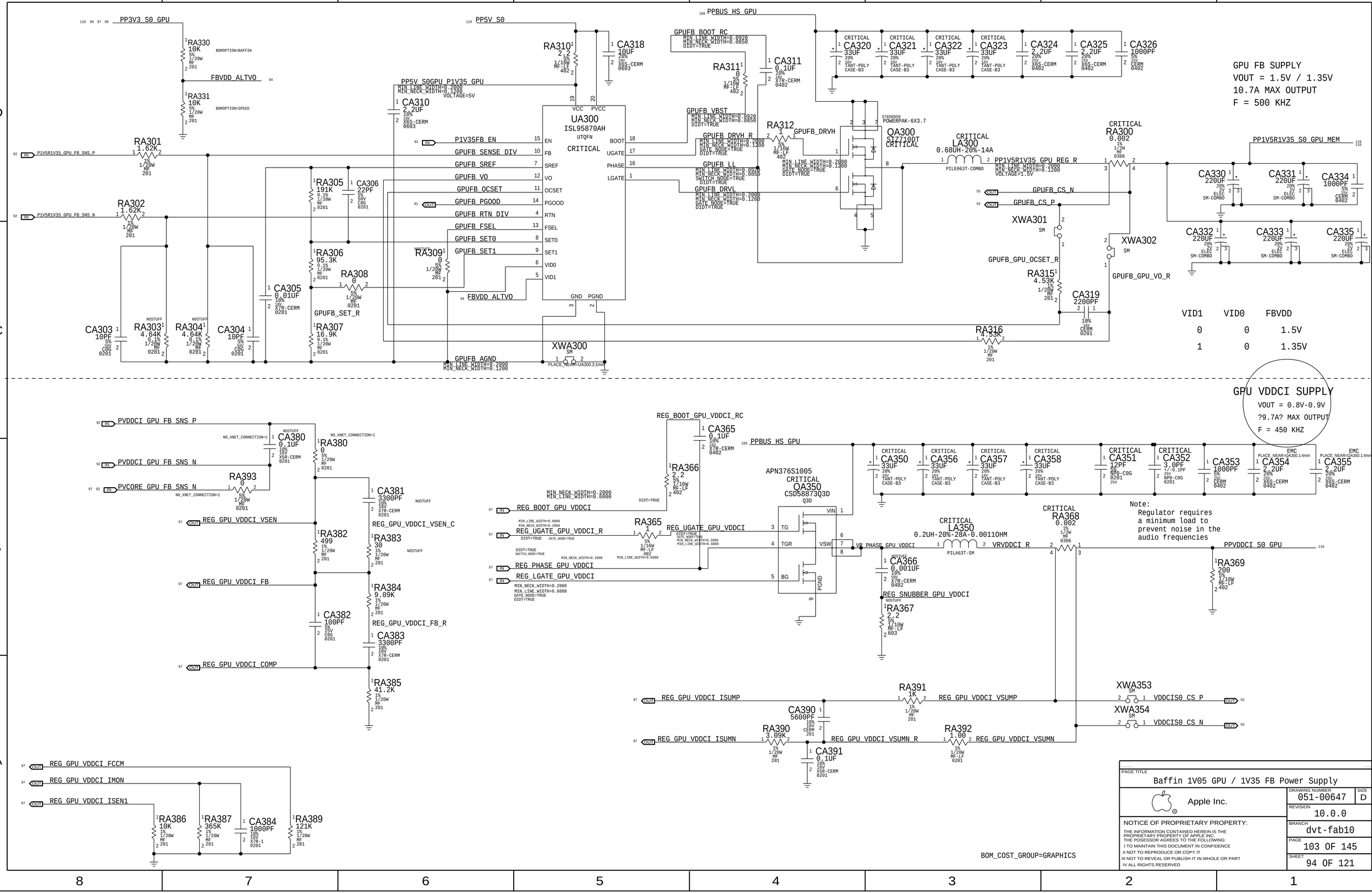


PAGE TITLE	BAFFIN PCI-E
Apple Inc.	DRAWING NUMBER 051-00647
	SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 100 OF 145
	SHEET 91 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


LA100
0.24UH-20%-10A-0.0120HM
1210
PP1V8_S0_GPU_LC_IC
PP1V8_S0_GPU
CA100 0.1UF 10% 6.3V X6S 0201
CA101 0.1UF 10% 6.3V X6S 0201
CA102 1UF 20% 6.3V X6S-CERM 0201
CA103 1UF 20% 6.3V X6S-CERM 0201
CA10A 4.7UF 20% 6.3V X6S 0402
CA10B 4.7UF 20% 6.3V X6S 0402
CA10C 10UF 20% 4V X6S-CERM 0402-2
CA10D 10UF 20% 4V X6S-CERM 0402-2
CA104 0.1UF 10% 6.3V X6S 0201
PP3V3_S0_GPU
BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 5 OF 7
PP1V5R1V35_S0_GPU_IC
PPVDDCI_S0_GPU
RA101 1K 1% 1/20W MF 201
BOMOPTION=SPEED
PP1V8_S0_GPU_LC_IC
VOLTAGE=1.8V
PP3V3_S0_GPU
GPU_AUX_ZVSS
P1V5R1V35_GPU_FB_SNS_P
PVCORE_GPU_FB_SNS_P
PVDDCI_GPU_FB_SNS_P
P1V5R1V35_GPU_FB_SNS_N
PVCORE_GPU_FB_SNS_N
PVDDCI_GPU_FB_SNS_N
XWA100
SHORT-14L-0.1MM-SM
XWA101
XWA102
GPU_FB_SNS_COMMON_NEG
GPU_PCIE_ZVSS
RA102 200 1% 1/20W MF 201
RA100 150 1% 1/20W MF 201
BOMOPTION=BAFFIN
RA110 10 1% 1/20W MF 201
RA111 10 1% 1/20W MF 201
RA112 10 1% 1/20W MF 201
RA113 10 1% 1/20W MF 201
PP1V5R1V35_S0_GPU_MEM
PPVCORE_S0_GPU
PPVDDCI_S0_GPU
NO_XNET_CONNECTION=1
VMEMIO
VDD_08
VDD_18
VDD_33
AUX_ZVSS
FB_VMEMIO
FB_VDDC
FB_VDDCI
FB_VSS
PCIE_ZVSS
VDDC
VDDCI
PPVCORE_S0_GPU
CA125 220UF 20% 2V ELEC SM-COMBO
CA126 220UF 20% 2V ELEC SM-COMBO
CA127 220UF 20% 2V ELEC SM-COMBO
CA128 220UF 20% 2V ELEC SM-COMBO
CA176 220UF 20% 2V ELEC SM-COMBO
CA129 20UF 20% 2.5V X6S-CERM 0402-1
CA130 20UF 20% 2.5V X6S-CERM 0402-1
CA131 20UF 20% 2.5V X6S-CERM 0402-1
CA132 20UF 20% 2.5V X6S-CERM 0402-1
CA133 20UF 20% 2.5V X6S-CERM 0402-1
CA134 20UF 20% 2.5V X6S-CERM 0402-1
CA135 20UF 20% 2.5V X6S-CERM 0402-1
CA177 220UF 20% 2V ELEC SM-COMBO
CA178 220UF 20% 2V ELEC SM-COMBO
CA136 2.2UF 20% 4V X6S-CERM 0201
CA137 2.2UF 20% 4V X6S-CERM 0201
CA138 2.2UF 20% 4V X6S-CERM 0201
CA139 2.2UF 20% 4V X6S-CERM 0201
CA140 2.2UF 20% 4V X6S-CERM 0201
CA141 2.2UF 20% 4V X6S-CERM 0201
CA142 2.2UF 20% 4V X6S-CERM 0201
CA143 2.2UF 20% 4V X6S-CERM 0201
CA144 2.2UF 20% 4V X6S-CERM 0201
CA145 2.2UF 20% 4V X6S-CERM 0201
CA146 2.2UF 20% 4V X6S-CERM 0201
CA147 2.2UF 20% 4V X6S-CERM 0201
CA148 2.2UF 20% 4V X6S-CERM 0201
CA150 2.2UF 20% 4V X6S-CERM 0201
CA151 12PF 5% 25V NP0-C0G 0201
CA152 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA153 12PF 5% 25V NP0-C0G 0201
CA154 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA11A 1UF 20% 6.3V X6S-CERM 0201
CA11B 1UF 20% 6.3V X6S-CERM 0201
CA11C 4.7UF 20% 6.3V X6S 0402
CA11D 4.7UF 20% 6.3V X6S 0402
CA11E 10UF 20% 4V X6S-CERM 0402-2
CA11F 10UF 20% 4V X6S-CERM 0402-2
PPVDDCI_S0_GPU
CA155 1UF 20% 6.3V X6S-CERM 0201
CA156 1UF 20% 6.3V X6S-CERM 0201
CA157 1UF 20% 6.3V X6S-CERM 0201
CA158 12PF 5% 25V NP0-C0G 0201
CA159 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA160 0.1UF 10% 6.3V X6S 0201
CA161 0.1UF 10% 6.3V X6S 0201
CA162 0.1UF 10% 6.3V X6S 0201
CA163 1UF 20% 6.3V X6S-CERM 0201
CA164 1UF 20% 6.3V X6S-CERM 0201
CA165 1UF 20% 6.3V X6S-CERM 0201
CA166 12PF 5% 25V NP0-C0G 0201
CA167 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA168 220UF 20% 2V ELEC SM-COMBO
CA169 220UF 20% 2V ELEC SM-COMBO
CA170 220UF 20% 2V ELEC SM-COMBO
CA171 220UF 20% 2V ELEC SM-COMBO
CA175 220UF 20% 2V ELEC SM-COMBO
CA172 1000PF 5% 25V C0G-CERM 0402
CRITICAL CA173 10UF 20% 10V X6S-CERM 0603
CRITICAL CA174 10UF 20% 10V X6S-CERM 0603
BOM_COST_GROUP=GRAPHICS
PP1V5R1V35_S0_GPU_IC
CA105 0.1UF 10% 6.3V X6S 0201
CA106 0.1UF 10% 6.3V X6S 0201
CA107 0.1UF 10% 6.3V X6S 0201
CA108 0.1UF 10% 6.3V X6S 0201
CA109 0.1UF 10% 6.3V X6S 0201
CA110 12PF 5% 25V NP0-C0G 0201
CA111 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA199 3.1PF +/-0.05PF 25V C0G-CERM 0201
CA112 20UF 20% 2.5V X6S-CERM 0402-1
CA113 10UF 20% 4V X6S-CERM 0402-2
CA114 1000PF 5% 25V C0G CERM 0402
CA115 1000PF 5% 25V C0G CERM 0402
CA116 1000PF 5% 25V C0G CERM 0402
CA117 2.2UF 20% 4V X6S-CERM 0201
CA118 2.2UF 20% 4V X6S-CERM 0201
CA119 2.2UF 20% 4V X6S-CERM 0201
CA120 2.2UF 20% 4V X6S-CERM 0201
CA121 12PF 5% 25V NP0-C0G 0201
CA149 12PF 5% 25V NP0-C0G 0201
CRITICAL CA122 10UF 20% 10V X6S-CERM 0603
CRITICAL CA123 10UF 20% 10V X6S-CERM 0603
CRITICAL CA124 10UF 20% 10V X6S-CERM 0603
PAGE TITLE
Baffin CORE/FB POWER
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 101 OF 145
SHEET 92 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 3 OF 7
DQA0_0
DQA0_1
DQA0_2
DQA0_3
DQA0_4
DQA0_5
DQA0_6
DQA0_7
DQA0_8
DQA0_9
DQA0_10
DQA0_11
DQA0_12
DQA0_13
DQA0_14
DQA0_15
DQA0_16
DQA0_17
DQA0_18
DQA0_19
DQA0_20
DQA0_21
DQA0_22
DQA0_23
DQA0_24
DQA0_25
DQA0_26
DQA0_27
DQA0_28
DQA0_29
DQA0_30
DQA0_31
DQA1_0
DQA1_1
DQA1_2
DQA1_3
DQA1_4
DQA1_5
DQA1_6
DQA1_7
DQA1_8
DQA1_9
DQA1_10
DQA1_11
DQA1_12
DQA1_13
DQA1_14
DQA1_15
DQA1_16
DQA1_17
DQA1_18
DQA1_19
DQA1_20
DQA1_21
DQA1_22
DQA1_23
DQA1_24
DQA1_25
DQA1_26
DQA1_27
DQA1_28
DQA1_29
DQA1_30
DQA1_31
FB_A_MVREFD
MVREFDA
FB_A_CALR
MEM_CALRA
RA202
120
PLACE_NEAR=UA000.K15:2.54MM
MAA0_0
MAA0_1
MAA0_2
MAA0_3
MAA0_4
MAA0_5
MAA0_6
MAA0_7
MAA1_0
MAA1_1
MAA1_2
MAA1_3
MAA1_4
MAA1_5
MAA1_6
MAA1_7
WCKA0_0
WCKA0_0*
WCKA0_1
WCKA0_1*
WCKA1_0
WCKA1_0*
WCKA1_1
WCKA1_1*
EDCA0_0
EDCA0_1
EDCA0_2
EDCA0_3
EDCA1_0
EDCA1_1
EDCA1_2
EDCA1_3
DDBIA0_0
DDBIA0_1
DDBIA0_2
DDBIA0_3
DDBIA1_0
DDBIA1_1
DDBIA1_2
DDBIA1_3
ADBIA0
ADBIA1
CLKA0
CLKA0*
CLKA1
CLKA1*
RASA0*
RASA1*
CASA0*
CASA1*
CSA0_0*
CSA1_0*
CKEA0
CKEA1
WEA0*
WEA1*
MAA0_8
MAA0_9
MAA1_8
MAA1_9
DRAM_RSTA
RA290
5.1K
CA290
120PF
RA291
10
RA293
49.9
PP1V5R1V35_S0_GPU_IC
RA204
40.2
note: to be unstuffed after initial baffin bringup
RA206
100
CA200
1UF
PLACE_NEAR=UA000.K17:2.54MM
BOMOPTION=OMIT_TABLE
UA000
100-CK4803-ES
BGA
SYM 4 OF 7
DQB0_0
DQB0_1
DQB0_2
DQB0_3
DQB0_4
DQB0_5
DQB0_6
DQB0_7
DQB0_8
DQB0_9
DQB0_10
DQB0_11
DQB0_12
DQB0_13
DQB0_14
DQB0_15
DQB0_16
DQB0_17
DQB0_18
DQB0_19
DQB0_20
DQB0_21
DQB0_22
DQB0_23
DQB0_24
DQB0_25
DQB0_26
DQB0_27
DQB0_28
DQB0_29
DQB0_30
DQB0_31
DQB1_0
DQB1_1
DQB1_2
DQB1_3
DQB1_4
DQB1_5
DQB1_6
DQB1_7
DQB1_8
DQB1_9
DQB1_10
DQB1_11
DQB1_12
DQB1_13
DQB1_14
DQB1_15
DQB1_16
DQB1_17
DQB1_18
DQB1_19
DQB1_20
DQB1_21
DQB1_22
DQB1_23
DQB1_24
DQB1_25
DQB1_26
DQB1_27
DQB1_28
DQB1_29
DQB1_30
DQB1_31
FB_B_MVREFD
MVREFDB
PP3V3_S0_GPU
GPU_TEST_EN
TESTEN
FB_B_CALR
MEM_CALRB
RA200
10K
RA201
10K
RA203
120
PLACE_NEAR=UA000.R10:2.54MM
MAB0_0
MAB0_1
MAB0_2
MAB0_3
MAB0_4
MAB0_5
MAB0_6
MAB0_7
MAB1_0
MAB1_1
MAB1_2
MAB1_3
MAB1_4
MAB1_5
MAB1_6
MAB1_7
WCKB0_0
WCKB0_0*
WCKB0_1
WCKB0_1*
WCKB1_0
WCKB1_0*
WCKB1_1
WCKB1_1*
EDCB0_0
EDCB0_1
EDCB0_2
EDCB0_3
EDCB1_0
EDCB1_1
EDCB1_2
EDCB1_3
DDBIB0_0
DDBIB0_1
DDBIB0_2
DDBIB0_3
DDBIB1_0
DDBIB1_1
DDBIB1_2
DDBIB1_3
ADBIB0
ADBIB1
CLKB0
CLKB0*
CLKB1
CLKB1*
RASB0*
RASB1*
CASB0*
CASB1*
CSB0_0*
CSB1_0*
CKEB0
CKEB1
WEB0*
WEB1*
MAB0_8
MAB0_9
MAB1_8
MAB1_9
DRAM_RSTB
RA296
10
RA297
49.9
RA295
5.1K
CA295
120PF
PP1V5R1V35_S0_GPU_IC
RA205
40.2
note: to be unstuffed after initial baffin bringup
RA207
100
CA201
1UF
PLACE_NEAR=UA000.U10:2.54MM
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin FRAME BUFFER I/F
Apple Inc.
DRAWING NUMBER
051-00647
SIZE
D
REVISION
10.0.0
BRANCH
dvt-fab10
PAGE
102 OF 145
SHEET
93 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED


PP3V3_S0_GPU
RA330 10K 5% 1/20W MF 201 BOMOPTION=BAFFIN
FBVDD_ALTVO
RA331 10K 5% 1/20W MF 201 BOMOPTION=SPEED
PP5V_S0
RA310 2.2 5% 1/16W MF-LF 402
CA318 10UF 20% 10V X6S-CERM 0603
PP5V_S0GPU_P1V35_GPU
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=5V
CA310 2.2UF 10% 10V X6S-CERM 0603
PPBUS_HS_GPU
GPUFB_BOOT_RC
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
DIDT=TRUE
RA311 0 5% 1/16W MF-LF 402
CA311 0.1UF 10% 16V X7R-CERM 0402
GPUFB_VBST
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
DIDT=TRUE
GPUFB_DRVH_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE
GPUFB_LL
MIN_LINE_WIDTH=0.0920
MIN_NECK_WIDTH=0.0850
SWITCH_NODE=TRUE
DIDT=TRUE
GPUFB_DRVL
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE
RA312 1 5% 1/16W MF-LF 402
GPUFB_DRVH
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
GATE_NODE=TRUE
DIDT=TRUE
QA300 SIZ710DT CRITICAL
37680959 POWERPAK-6X3.7
UA300 ISL95870AH UTQFN CRITICAL
VCC PVCC BOOT UGATE PHASE LGATE
EN FB SREF VO OCSET PGOOD RTN FSEL SET0 SET1 VID0 VID1
GND PGND
XWA300 SM PLACE_NEAR=UA300.3:1mm
CRITICAL CA320 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA321 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA322 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA323 33UF 20% 16V TANT-POLY CASE-B3
CA324 2.2UF 20% 25V X6S-CERM 0402
CA325 2.2UF 20% 25V X6S-CERM 0402
CA326 1000PF 5% 25V C0G 0402
GPU FB SUPPLY
VOUT = 1.5V / 1.35V
10.7A MAX OUTPUT
F = 500 KHZ
P1V5R1V35_GPU_FB_SNS_P
RA301 1.62K 1% 1/20W MF 201
P1V5R1V35_GPU_FB_SNS_N
RA302 1.62K 1% 1/20W MF 201
RA305 191K 0.1% 1/20W MF 0201
CA306 22PF 5% 50V C0G 0201
RA306 95.3K 0.1% 1/20W MF 0201
RA307 16.9K 0.1% 1/20W MF 0201
RA308 0 5% 1/20W MF 0201
GPUFB_SET_R
CA305 0.01UF 10% 16V X7R-CERM 0201
CA303 10PF 5% 50V C0G 0201
RA303 4.64K 0.1% 1/20W MF 0201 NOSTUFF
RA304 4.64K 0.1% 1/20W MF 0201 NOSTUFF
CA304 10PF 5% 50V C0G 0201
RA309 0 5% 1/20W MF 201 NOSTUFF
P1V35FB_EN
GPUFB_SENSE_DIV
GPUFB_SREF
GPUFB_VO
GPUFB_OCSET
GPUFB_PGOOD
GPUFB_RTN_DIV
GPUFB_FSEL
GPUFB_SET0
GPUFB_SET1
FBVDD_ALTVO
GPUFB_AGND
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
CRITICAL LA300 0.68UH-20%-14A PILE063T-COMBO
PP1V5R1V35_GPU_REG_R
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.5V
CRITICAL RA300 0.002 1% 1/2W MF 0306
PP1V5R1V35_GPU_MEM
CA330 220UF 20% 2V ELEC SM-COMBO
CA331 220UF 20% 2V ELEC SM-COMBO
CA334 1000PF 5% 25V C0G 0402
GPUFB_CS_N
GPUFB_CS_P
XWA301 SM
XWA302 SM
GPUFB_GPU_OCSET_R
GPUFB_GPU_VO_R
RA315 4.53K 1% 1/20W MF 201
CA319 2200PF 10% 16V CERM 0201
RA316 4.53K 1% 1/20W MF 201
CA332 220UF 20% 2V ELEC SM-COMBO
CA333 220UF 20% 2V ELEC SM-COMBO
CA335 220UF 20% 2V ELEC SM-COMBO
VID1 VID0 FBVDD
0 0 1.5V
1 0 1.35V
GPU VDDCI SUPPLY
VOUT = 0.8V-0.9V
?9.7A? MAX OUTPUT
F = 450 KHZ
PVDDCI_GPU_FB_SNS_P
PVDDCI_GPU_FB_SNS_N
PVCORE_GPU_FB_SNS_N
NO_XNET_CONNECTION=1
CA380 0.1UF 10% 16V X5R-CERM 0201 NOSTUFF
RA380 0 5% 1/20W MF 0201
RA393 0 5% 1/20W MF 0201
CA381 3300PF 10% 10V X7R-CERM 0201 NOSTUFF
REG_GPU_VDDCI_VSEN
REG_GPU_VDDCI_VSEN_C
RA382 499 1% 1/20W MF 201
RA383 30 1% 1/20W MF 201 NOSTUFF
REG_GPU_VDDCI_FB
REG_GPU_VDDCI_FB_R
RA384 9.09K 1% 1/20W MF 201
CA382 100PF 5% 25V C0G 0201
CA383 3300PF 10% 10V X7R-CERM 0201
REG_GPU_VDDCI_COMP
RA385 41.2K 1% 1/20W MF 201
REG_GPU_VDDCI_FCCM
REG_GPU_VDDCI_IMON
REG_GPU_VDDCI_ISEN1
RA386 10K 1% 1/20W MF 201
RA387 365K 1% 1/20W MF 201
CA384 1000PF 10% 16V X7R-1 0201
RA389 121K 1% 1/20W MF 201
REG_BOOT_GPU_VDDCI_RC
CA365 0.1UF 10% 16V X7R-CERM 0402
RA366 2.2 5% 1/16W MF-LF 402
APN376S1005
CRITICAL
QA350 CSD58873Q3D Q3D
REG_BOOT_GPU_VDDCI
REG_UGATE_GPU_VDDCI_R
RA365 1 5% 1/16W MF-LF 402
REG_UGATE_GPU_VDDCI
REG_PHASE_GPU_VDDCI
REG_LGATE_GPU_VDDCI
VIN TG TGR VSW BG PGND
VR_PHASE_GPU_VDDCI
CRITICAL LA350 0.2UH-20%-28A-0.00110HM PILA63T-SM
VRVDDCI_R
CRITICAL RA368 0.002 1% 1/2W MF 0306
PPVDDCI_S0_GPU
RA369 200 5% 1/16W MF-LF 402
Note:
Regulator requires a minimum load to prevent noise in the audio frequencies
CRITICAL CA350 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA356 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA357 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA358 33UF 20% 16V TANT-POLY CASE-B3
CRITICAL CA351 12PF 5% NP0-C0G 0201 25V
CRITICAL CA352 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA353 1000PF 5% 25V C0G 0402
EMC CA354 2.2UF 20% 25V X6S-CERM 0402 PLACE_NEAR=QA350.1:4mm
EMC CA355 2.2UF 20% 25V X6S-CERM 0402 PLACE_NEAR=QA350.1:4mm
CA366 0.001UF 10% 50V X7R-CERM 0402 NOSTUFF
REG_SNUBBER_GPU_VDDCI
RA367 2.2 5% 1/10W MF-LF 603 NOSTUFF
REG_GPU_VDDCI_ISUMP
REG_GPU_VDDCI_ISUMN
RA391 1K 1% 1/20W MF 201
CA390 5600PF 10% 16V CERM 201
RA390 3.09K 1% 1/20W MF 201
CA391 0.1UF 10% 16V X5R-CERM 0201
REG_GPU_VDDCI_VSUMP
REG_GPU_VDDCI_VSUMN_R
RA392 1.00 1% 1/20W MF-LF 0201
REG_GPU_VDDCI_VSUMN
XWA353 SM VDDCIS0_CS_P
XWA354 SM VDDCIS0_CS_N
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin 1V05 GPU / 1V35 FB Power Supply
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 103 OF 145
SHEET 94 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

8 7 6 5 4 3 2 1

D C B A

UA400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(1 OF 2)
OMIT_TABLE

UA400
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

UA450
32MX32-1.25GHZ-MFL
BGA
H5GQ1H24AFR-T2C
(2 OF 2)
OMIT_TABLE

PP1V5R1V35_S0_GPU_MEM
CK TERMINATION - A0
CK TERMINATION - A1
RA401 60.4 1% 1/20W MF 201
RA402 60.4 1% 1/20W MF 201
RA451 60.4 1% 1/20W MF 201
RA452 60.4 1% 1/20W MF 201
PLACE_NEAR=UA400.211:8.4MM
PLACE_NEAR=UA400.212:8.4MM
PLACE_NEAR=UA400.213:8.4MM
FB_A0_CLK_P
FB_A0_CLK_N
FB_A1_CLK_P
FB_A1_CLK_N

RA400 120 1% 1/20W MF 201
RA403 120 1% 1/20W MF 201
RA404 120 1% 1/20W MF 201
RA450 120 1% 1/20W MF 201
RA453 120 1% 1/20W MF 201
RA454 120 1% 1/20W MF 201

FB_A0_A<2>
FB_A0_A<5>
FB_A0_A<4>
FB_A0_A<3>
FB_A0_A<7>
FB_A0_A<1>
FB_A0_A<0>
FB_A0_A<6>
FB_A0_CKE_L
FB_A0_CLK_P
FB_A0_CLK_N
FB_A0_CS_L
FB_A0_WE_L
FB_A0_CAS_L
FB_A0_RAS_L
FB_A0_ZQ
FB_A0_MF
FB_A0_SEN
FB_A_RESET_L
FB_A0_ABI_L
FB_A0_EDC<0>
FB_A0_EDC<1>
FB_A0_EDC<2>
FB_A0_EDC<3>
FB_A0_WCLK_P<0>
FB_A0_WCLK_N<0>
FB_A0_WCLK_P<1>
FB_A0_WCLK_N<1>
FB_A0_A<8>

FB_A1_A<2>
FB_A1_A<5>
FB_A1_A<4>
FB_A1_A<3>
FB_A1_A<7>
FB_A1_A<1>
FB_A1_A<0>
FB_A1_A<6>
FB_A1_CKE_L
FB_A1_CLK_P
FB_A1_CLK_N
FB_A1_CS_L
FB_A1_WE_L
FB_A1_CAS_L
FB_A1_RAS_L
FB_A1_ZQ
FB_A1_MF
FB_A1_SEN
FB_A_RESET_L
FB_A1_ABI_L
FB_A1_EDC<0>
FB_A1_EDC<1>
FB_A1_EDC<2>
FB_A1_EDC<3>
FB_A1_WCLK_P<0>
FB_A1_WCLK_N<0>
FB_A1_WCLK_P<1>
FB_A1_WCLK_N<1>
FB_A1_A<8>

BA0/A2
BA1/A5
BA2/A4
BA3/A3
A8/A7
A9/A1
A10/A0
A11/A6
CKE*
CK
CK*
CS*
WE*
CAS*
RAS*
ZQ
MF (MF=0)
SEN
RESET*
ABI*
EDC0
EDC1
EDC2
EDC3
WCK01
WCK01*
WCK23
WCK23*
NC

DBI0*
DBI1*
DBI2*
DBI3*
DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31

FB_A0_DBI_L<0>
FB_A0_DBI_L<1>
FB_A0_DBI_L<2>
FB_A0_DBI_L<3>
FB_A0_DQ<0>
FB_A0_DQ<1>
FB_A0_DQ<2>
FB_A0_DQ<3>
FB_A0_DQ<4>
FB_A0_DQ<5>
FB_A0_DQ<6>
FB_A0_DQ<7>
FB_A0_DQ<8>
FB_A0_DQ<9>
FB_A0_DQ<10>
FB_A0_DQ<11>
FB_A0_DQ<12>
FB_A0_DQ<13>
FB_A0_DQ<14>
FB_A0_DQ<15>
FB_A0_DQ<16>
FB_A0_DQ<17>
FB_A0_DQ<18>
FB_A0_DQ<19>
FB_A0_DQ<20>
FB_A0_DQ<21>
FB_A0_DQ<22>
FB_A0_DQ<23>
FB_A0_DQ<24>
FB_A0_DQ<25>
FB_A0_DQ<26>
FB_A0_DQ<27>
FB_A0_DQ<28>
FB_A0_DQ<29>
FB_A0_DQ<30>
FB_A0_DQ<31>

FB_A1_DBI_L<0>
FB_A1_DBI_L<1>
FB_A1_DBI_L<2>
FB_A1_DBI_L<3>
FB_A1_DQ<0>
FB_A1_DQ<1>
FB_A1_DQ<2>
FB_A1_DQ<3>
FB_A1_DQ<4>
FB_A1_DQ<5>
FB_A1_DQ<6>
FB_A1_DQ<7>
FB_A1_DQ<8>
FB_A1_DQ<9>
FB_A1_DQ<10>
FB_A1_DQ<11>
FB_A1_DQ<12>
FB_A1_DQ<13>
FB_A1_DQ<14>
FB_A1_DQ<15>
FB_A1_DQ<16>
FB_A1_DQ<17>
FB_A1_DQ<18>
FB_A1_DQ<19>
FB_A1_DQ<20>
FB_A1_DQ<21>
FB_A1_DQ<22>
FB_A1_DQ<23>
FB_A1_DQ<24>
FB_A1_DQ<25>
FB_A1_DQ<26>
FB_A1_DQ<27>
FB_A1_DQ<28>
FB_A1_DQ<29>
FB_A1_DQ<30>
FB_A1_DQ<31>

CA400 4.7UF 20% 6.3V X6S 0402
CA401 4.7UF 20% 6.3V X6S 0402
CA402 4.7UF 20% 6.3V X6S 0402
NOSTUFF CA496 12PF 5% 25V NP0-C0G 0201
CA403 4.7UF 20% 6.3V X6S 0402
CA404 4.7UF 20% 6.3V X6S 0402
CA405 4.7UF 20% 6.3V X6S 0402
CA497 3.0PF +/-0.1PF 25V NP0-C0G 0201
CA406 1UF 20% 4V CERM-X6S 0201
CA407 1UF 20% 4V CERM-X6S 0201
CA408 1UF 20% 4V CERM-X6S 0201
CA409 1UF 20% 4V CERM-X6S 0201
CA410 1UF 20% 4V CERM-X6S 0201
CA411 1UF 20% 4V CERM-X6S 0201
CA412 1UF 20% 4V CERM-X6S 0201
CA413 1UF 20% 4V CERM-X6S 0201
CA414 1UF 20% 4V CERM-X6S 0201
CA415 1UF 20% 4V CERM-X6S 0201
CA416 0.1UF 10% 6.3V X6S 0201
CA417 0.1UF 10% 6.3V X6S 0201
CA418 0.1UF 10% 6.3V X6S 0201
CA419 0.1UF 10% 6.3V X6S 0201
CA420 0.1UF 10% 6.3V X6S 0201
CA421 0.1UF 10% 6.3V X6S 0201
CA422 0.1UF 10% 6.3V X6S 0201
CA423 0.1UF 10% 6.3V X6S 0201
CA424 0.1UF 10% 6.3V X6S 0201
CA425 0.1UF 10% 6.3V X6S 0201

VDD
VDDQ
VSS
VSSQ
VREFC
VREFD

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.0850
RA430 549 1% 1/20W MF 201
RA431 1.33K 1% 1/20W MF 201
RA432 549 1% 1/20W MF 201
RA433 1.33K 1% 1/20W MF 201
RA434 931 1% 1/20W MF 201
RA435 931 1% 1/20W MF 201
CA431 820PF 10% 25V X7R-CERM 0201
CA432 820PF 10% 25V X7R-CERM 0201
CA433 820PF 10% 25V X7R-CERM 0201
NOSTUFF
FB_A0_VREFC
FB_A0_VREFD
FB_SW_LEG
PLACE CLOSE TO U9000

RA480 549 1% 1/20W MF 201
RA481 1.33K 1% 1/20W MF 201
RA482 549 1% 1/20W MF 201
RA483 1.33K 1% 1/20W MF 201
RA484 931 1% 1/20W MF 201
RA485 931 1% 1/20W MF 201
CA481 820PF 10% 25V X7R-CERM 0201
CA482 820PF 10% 25V X7R-CERM 0201
CA483 820PF 10% 25V X7R-CERM 0201
FB_A1_VREFC
FB_A1_VREFD
PLACE CLOSE TO U9050

CA450 4.7UF 20% 6.3V X6S 0402
CA451 4.7UF 20% 6.3V X6S 0402
CA452 4.7UF 20% 6.3V X6S 0402
CA453 4.7UF 20% 6.3V X6S 0402
CA454 4.7UF 20% 6.3V X6S 0402
CA455 4.7UF 20% 6.3V X6S 0402
CA456 1UF 20% 4V CERM-X6S 0201
CA457 1UF 20% 4V CERM-X6S 0201
CA458 1UF 20% 4V CERM-X6S 0201
CA459 1UF 20% 4V CERM-X6S 0201
CA460 1UF 20% 4V CERM-X6S 0201
CA461 1UF 20% 4V CERM-X6S 0201
CA462 1UF 20% 4V CERM-X6S 0201
CA463 1UF 20% 4V CERM-X6S 0201
CA464 1UF 20% 4V CERM-X6S 0201
CA465 1UF 20% 4V CERM-X6S 0201
CA466 0.1UF 10% 6.3V X6S 0201
CA467 0.1UF 10% 6.3V X6S 0201
CA468 0.1UF 10% 6.3V X6S 0201
CA469 0.1UF 10% 6.3V X6S 0201
CA470 0.1UF 10% 6.3V X6S 0201
CA471 0.1UF 10% 6.3V X6S 0201
CA472 0.1UF 10% 6.3V X6S 0201
CA473 0.1UF 10% 6.3V X6S 0201
CA474 0.1UF 10% 6.3V X6S 0201
CA475 0.1UF 10% 6.3V X6S 0201

BOM_COST_GROUP=GRAPHICS

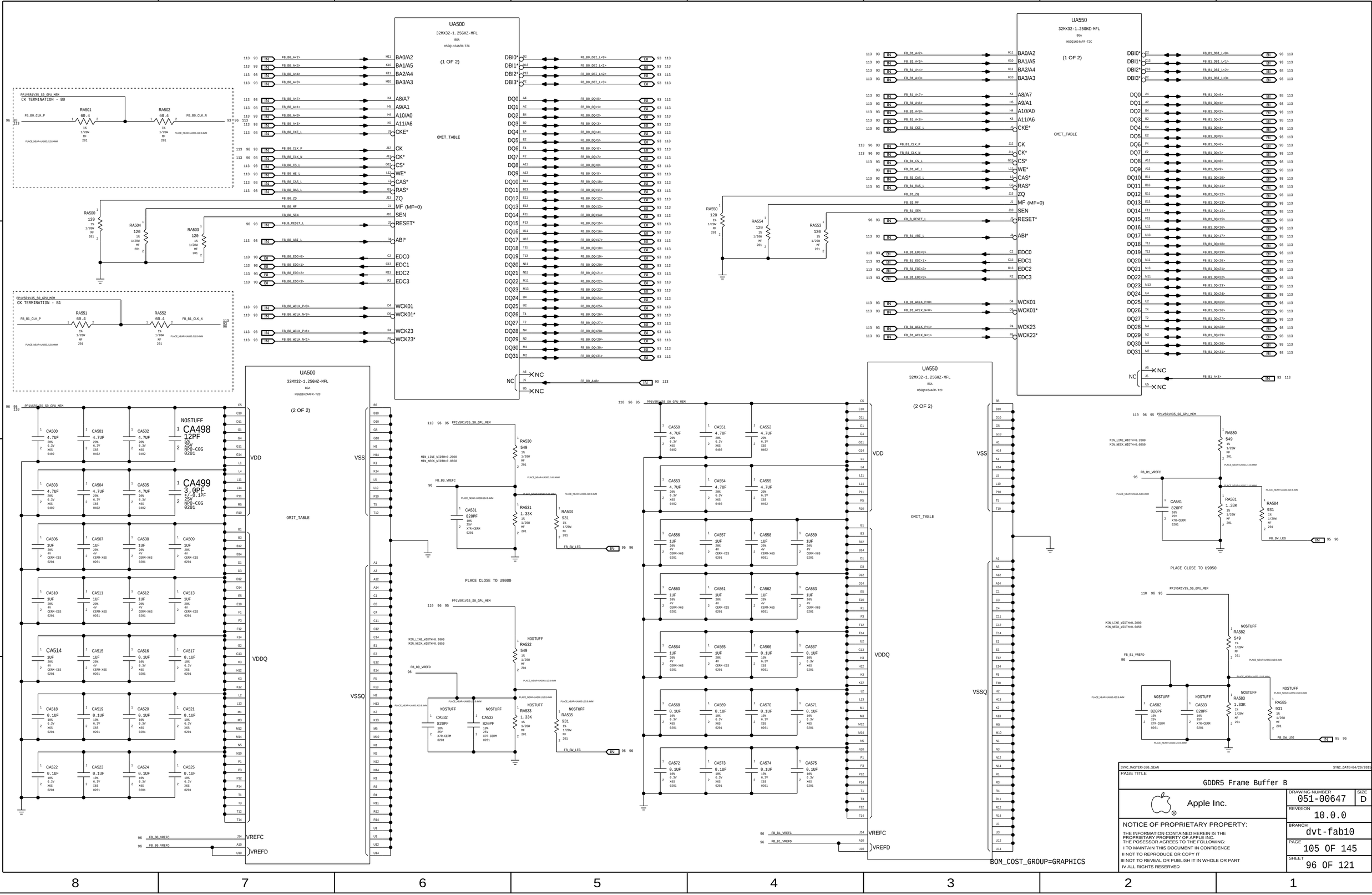
SYNC_MASTER=J80_SEAN
SYNC_DATE=04/29/2015

PAGE TITLE
GDDR5 Frame Buffer A

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 104 OF 145
SHEET 95 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J00_SEAN SYNC_DATE=04/29/2015

PAGE TITLE

GDDR5 Frame Buffer B

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 105 OF 145

SHEET 96 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S00174	2	MOSFET,CTRL+SYNC,25V,4.1/1.4MO,QFN32,6x6	QA640,QA650	CRITICAL	

GPU CORE SUPPLY

VOUT = 0.75-1.00V

64.2A MAX OUTPUT

F = 450 KHZ

UA600 ISL6277AHRZ

QFN, CRITICAL

VDDIO = 1.14V - 1.95V

TABLE 6. PRE-PWROK METAL VID CODES

SVC	SVD	OUTPUT VOLTAGE (V)
0	0	1.1
0	1	1.0
1	0	0.9
1	1	0.8

ISL6277A datasheet (December 19,2012)

BOM_COST_GROUP=GRAPHICS

PAGE TITLE: GFX IMVP VCore Regulator [106]

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER: 051-00647 | SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 106 OF 145
SHEET: 97 OF 121

former site of the SPEED MLPS STRAPS

PCIe Gen3 enabled, Half-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled
All power audio-capable display output
256MB FB Aperture Size

PS_0:	01001	82nF	8.45k	2k
PS_1:	10001	10nF	8.45k	2k
PS_2:	10000	10nF	NC	4.75k
PS_3:	00000	680nF	NC	4.75k

NOTICE THE ANNOYING MIX OF 3.3V AND 1.8V PULL-UPS

110 PP3V3_S0_GPU
110 PP1V8_S0_GPU

RA770 NOSTUFF 5.1K 1% 1/20W MF 201
RA771 NOSTUFF 5.1K 1% 1/20W MF 201
RA772 NOSTUFF 5.1K 1% 1/20W MF 201
RA773 NOSTUFF 5.1K 1% 1/20W MF 201
RA774 5.1K 1% 1/20W MF 201
RA775 NOSTUFF 5.1K 1% 1/20W MF 201
RA776 NOSTUFF 5.1K 1% 1/20W MF 201
RA777 NOSTUFF 5.1K 1% 1/20W MF 201
RA778 NOSTUFF 5.1K 1% 1/20W MF 201
RA779A NOSTUFF 5.1K 1% 1/20W MF 201
RA77A NOSTUFF 5.1K 1% 1/20W MF 201
RA77B NOSTUFF 5.1K 1% 1/20W MF 201
RA77C NOSTUFF 5.1K 1% 1/20W MF 201
RA77D NOSTUFF 5.1K 1% 1/20W MF 201
RA77F NOSTUFF 5.1K 1% 1/20W MF 201
RA780 NOSTUFF 5.1K 1% 1/20W MF 201
RA781 5.1K 1% 1/20W MF 201
RA782 NOSTUFF 5.1K 1% 1/20W MF 201
RA783 NOSTUFF 5.1K 1% 1/20W MF 201
RA784 5.1K 1% 1/20W MF 201
RA79B NOSTUFF 5.1K 1% 1/20W MF 201

99	GPU_ROM_CONFIG<2>	0
99	GPU_ROM_CONFIG<1>	0
99	GPU_ROM_CONFIG<0>	1
99	GPU_AUD_PORT_CONN<2>	0
99	GPU_AUD_PORT_CONN<1>	0
99	GPU_AUD_PORT_CONN<0>	0
99	GPU_BIF_GEN3_EN_A	1
99	GPU_TX_HALF_SWING	0
99	GPU_TX_DEEMPH_EN	1
99 99	GPU_ROM_SO (strap BIF_CLK_PM_EN)	1
99 98	GPU_ROM_CS_L_R (strap BIOS_ROM_EN)	0
99	GPU_VGA_DIS	0
99	GPU_AUD<1>	1
99	GPU_AUD<0>	0
99	GPU_BRD_CFG<2>	0
99	GPU_BRD_CFG<1>	0
99	GPU_BRD_CFG<0>	0
99	GPU_SMBUS_ADDR<1>	0
99	GPU_SMBUS_ADDR<0>	1

RA785 5.1K 1% 1/20W MF 201
RA786 NOSTUFF 5.1K 1% 1/20W MF 201
RA787 5.1K 1% 1/20W MF 201
RA788 NOSTUFF 5.1K 1% 1/20W MF 201
RA789 NOSTUFF 5.1K 1% 1/20W MF 201
RA78A 5.1K 1% 1/20W MF 201
RA78B NOSTUFF 5.1K 1% 1/20W MF 201
RA78C 5.1K 1% 1/20W MF 201
RA78D 5.1K 1% 1/20W MF 201
RA78E NOSTUFF 5.1K 1% 1/20W MF 201
RA78F 5.1K 1% 1/20W MF 201
RA790 5.1K 1% 1/20W MF 201
RA791 5.1K 1% 1/20W MF 201
RA792 5.1K 1% 1/20W MF 201
RA793 NOSTUFF 5.1K 1% 1/20W MF 201
RA794 5.1K 1% 1/20W MF 201
RA795 5.1K 1% 1/20W MF 201
RA796 5.1K 1% 1/20W MF 201
RA797 5.1K 1% 1/20W MF 201
RA798 5.1K 1% 1/20W MF 201
RA799 5.1K 1% 1/20W MF 201

GPU_ROM_SI_R (strap reserved) 98 99
GPU_RESERVED 99

BAFFIN STRAPS

PCIe Gen3 enabled, FULL-Swing, TX De-emp enabled
VBIOS disabled, Boot from EFI
VGA enabled, CLKREQ_L enabled
All power audio-capable display output
Audio for DP or HDMI dongle
256MB FB Aperture Size
SMBUS address 41

Former site of the GPU SVI2 VOLTAGE TRANSLATION SPEED ONLY

99 GPU_GPIO_SVC_R — RA750 22 1/20W 5% MF 201 — GPU_GPIO_SVC — RA757 0 5% 1/20W MF 0201 — GPUVCORE_SVC_R OUT 97

99 GPU_GPIO_SVD_R — RA751 22 1/20W 5% MF 201 — GPU_GPIO_SVD — RA758 0 5% 1/20W MF 0201 — GPUVCORE_SVD_R OUT 97

99 GPUVCORE_SVT — GPUVCORE_SVT IN 97
MAKE_BASE=TRUE

GPU CLKREQ GATING

110 89 49 PP3V3_S0
CA700 0.1UF 10% 6.3V CERM-X5R 0201
RA700 47K 5% 1/20W MF 201
89 EG_CLKREQ_SEL_L
BOMOPTION=SPEED
RA703 0 5% 1/20W MF 0201
111 EG_CLKREQ_OUT_L
BOMOPTION=BAFFIN
CRITICAL
UA702 PI5A3157BC6E SC70
SEL B1 VCC GND A B0
EG_CLKREQ_PU
VER 1
RA701 47K 5% 1/20W MF 201
RA702 47K 5% 1/20W MF 201
PP3V3_S0_GPU 110
GPU_CLKREQ_L 99
RA704 0 NOSTUFF MF 5% 1/20W 0201

SEL = 0 : PCH CLKREQ CONNECTED TO GPU
SEL = 1 : PCH CLKREQ TIED TO PULLUP

GPU XTAL 27 MHZ OR GPU OSC 100 MHZ

110 PP1V8_S0_GPU
OMIT_TABLE
RA740 0 5% 1/20W MF 0201
GPUCLK:OSC
RA741 10K 5% 1/20W MF 201
113 GPU_XTAL_XTAL_OR_CLK
GPUCLK:XTAL
CA740 18PF 5% 25V C0G 0201
OMIT_TABLE
RA743 0 5% 1/20W MF 0201
GPU_XTAL OR CLK_IN 99 113
GPUCLK:XTAL
RA745 1M 5% 1/20W MF 201
OMIT_TABLE
YA740 27MHZ-30PPM-18PF-60OHM 2.50X2.00MM-SM
GPU_XTAL_PWR_OR_GND
OMIT_TABLE
RA742 0 5% 1/20W MF 0201
GPUCLK:XTAL
RA744 0 5% 1/20W MF 0201
GPU_XTAL_OUT 99 113
113 GPU_XTAL_PU_OR_CAP
GPUCLK:XTAL
CA741 18PF 5% 25V C0G 0201

GPU ROM

110 PP3V3_S0_GPU
BOMOPTION=NOSTUFF
GPU_ROM:YES RA721 5.1K
GPU_ROM:YES RA723 33
99 GPU_ROM_SI_R — GPU_ROM_SI
GPU_ROM:YES RA724 33
99 GPU_ROM_SCLK_R — GPU_ROM_SCLK
GPU_ROM:YES RA725 33
98 99 GPU_ROM_CS_L_R — GPU_ROM_CS_L
GPU_ROM_WP_L
NO STUFF RA722 0
RA720 5.1K
UA701 M25P10A UFDFPN8 OMIT_TABLE
8 VCC
5 D
6 C
1 S*
3 W*
7 HOLD*
VSS 4
THRM PAD 9
2 Q
GPU_ROM_SO_R — RA726 33 — GPU_ROM_SO 98 99
GPU_ROM:YES CA721 0.1UF 10% 6.3V X5R 0201

GPU JTAG

110 PP3V3_S0_GPU
RA731 NOSTUFF 10K 5% 1/16W MF-LF 402
RA732 NOSTUFF 10K 5% 1/16W MF-LF 402
RA733 NOSTUFF 10K 5% 1/16W MF-LF 402
RA734 NOSTUFF 10K 5% 1/16W MF-LF 402
GPU_JTAG_TDI 99
GPU_JTAG_TRST_L 99
GPU_JTAG_TMS 99
GPU_JTAG_TDO 99
GPU_JTAG_TCK 99
RA730 NOSTUFF 10K 5% 1/16W MF-LF 402

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
197S0499	1	XTAL,27.000MHZ,30PPM,12PF,2.5x2.0MM	YA740	CRITICAL	GPUCLK:XTAL
197S00056	1	OSC,MEMS,100MHZ,+/-20PPM,1.8V,2520	YA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA743	CRITICAL	GPUCLK:XTAL
117S0080	1	RES,33 OHM,5%,0201	RA743	CRITICAL	GPUCLK:OSC
155S0387	1	FERRITE BEAD, 4700HM,0.1A,1.5MOHM DCR,060	RA740	CRITICAL	GPUCLK:OSC
117S0201	1	RES,0 OHM,5%,0201	RA742	CRITICAL	GPUCLK:XTAL
132S0444	1	CAP,CER,X5R,0.1UF,10%,6.3V,0201	RA742	CRITICAL	GPUCLK:OSC

BOM_COST_GROUP=GRAPHICS

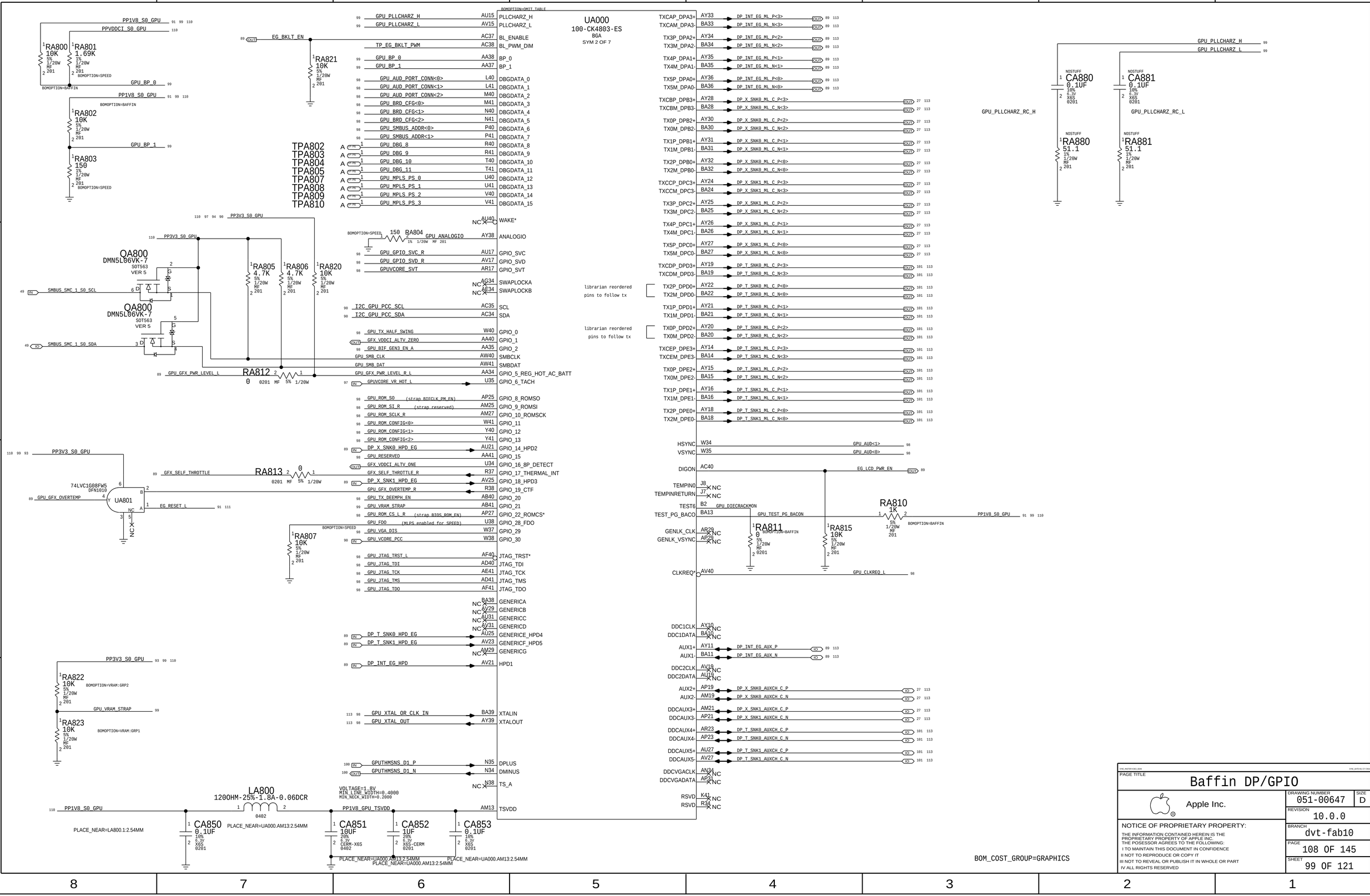
SYNC_MASTER=K18GL_DEAN — SYNC_DATE=01/29/2018

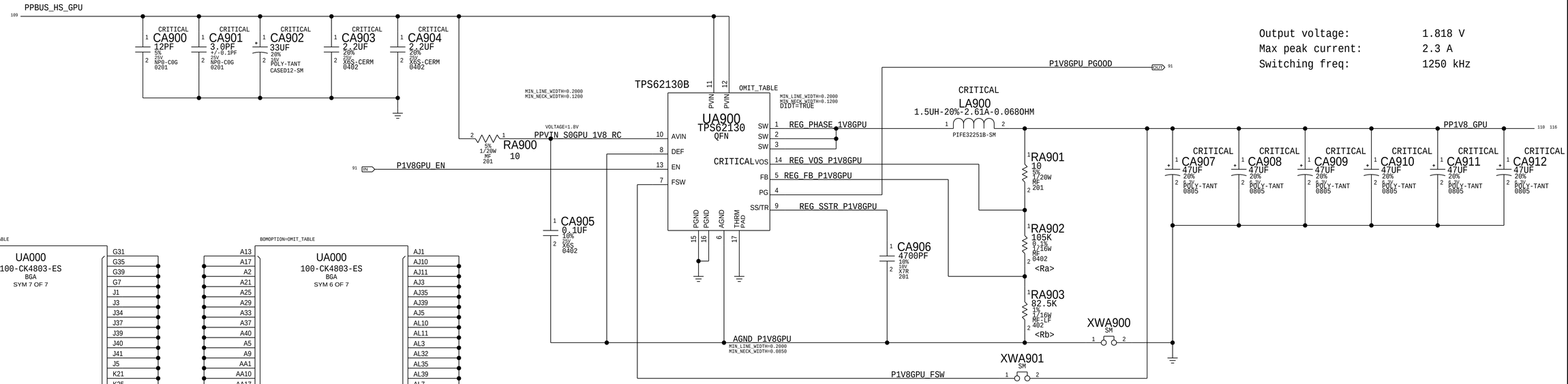
PAGE TITLE: Baffin GPIOs,CLK & Straps

Apple Inc.

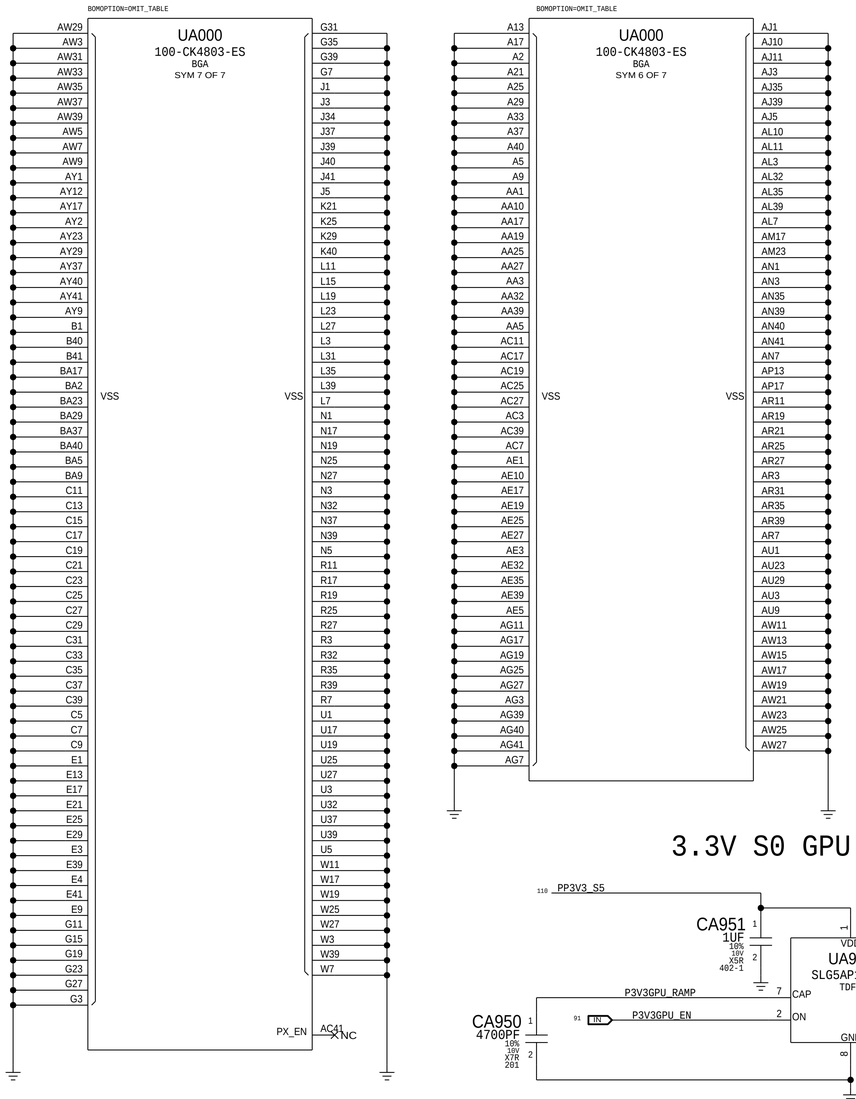
DRAWING NUMBER: 051-00647 — SIZE: D
REVISION: 10.0.0
BRANCH: dvt-fab10
PAGE: 107 OF 145
SHEET: 98 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

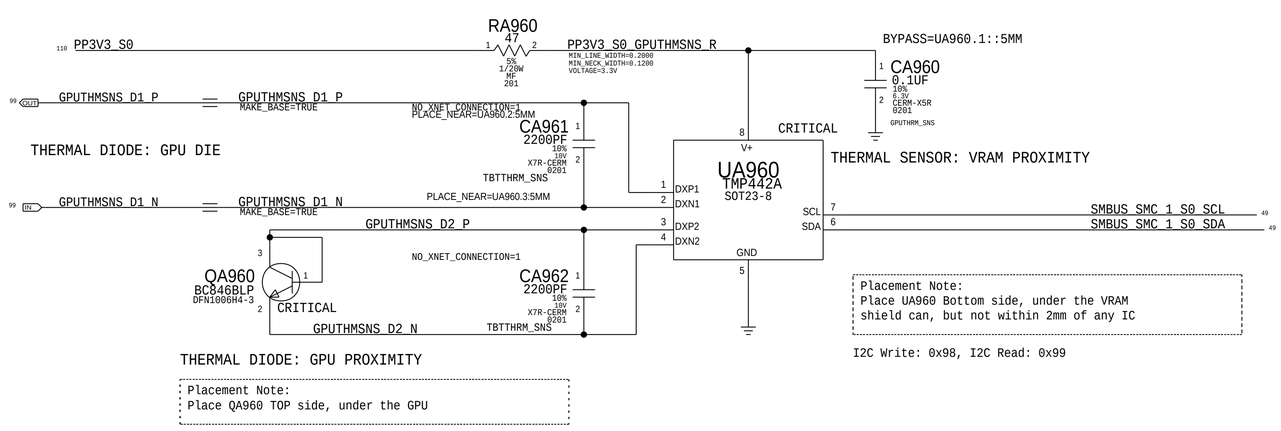

PP1V8_S0_GPU
PPVDDCI_S0_GPU
RA800 10K 5% 1/20W MF 201
RA801 1.69K 1% 1/20W MF 201
BOMOPTION=SPEED
GPU_BP_0
BOMOPTION=BAFFIN
RA802 10K 5% 1/20W MF 201
GPU_BP_1
RA803 150 1% 1/20W MF 201
EG_BKLT_EN
TP_EG_BKLT_PWM
RA821 10K 5% 1/20W MC 201
GPU_BP_0
GPU_BP_1
GPU_AUD_PORT_CONN<0>
GPU_AUD_PORT_CONN<1>
GPU_AUD_PORT_CONN<2>
GPU_BRD_CFG<0>
GPU_BRD_CFG<1>
GPU_BRD_CFG<2>
GPU_SMBUS_ADDR<0>
GPU_SMBUS_ADDR<1>
TPA802 TPA803 TPA804 TPA805 TPA807 TPA808 TPA809 TPA810
GPU_DBG_8
GPU_DBG_9
GPU_DBG_10
GPU_DBG_11
GPU_MPLS_PS_0
GPU_MPLS_PS_1
GPU_MPLS_PS_2
GPU_MPLS_PS_3
PP3V3_S0_GPU
QA800 DMN5L06VK-7 SOT563 VER 5
SMBUS_SMC_1_S0_SCL
SMBUS_SMC_1_S0_SDA
RA805 4.7K 5% 1/20W MF 201
RA806 4.7K 5% 1/20W MF 201
RA820 10K 5% 1/20W MF 201
GPU_GFX_PWR_LEVEL_L
RA812 0 0201 MF 5% 1/20W
GPU_GFX_PWR_LEVEL_R_L
PP3V3_S0_GPU
GFX_SELF_THROTTLE
RA813 0 0201 MF 5% 1/20W
GFX_SELF_THROTTLE_R
74LVC1G08FW5 DFN1010
UA801
GPU_GFX_OVERTEMP
EG_RESET_L
GPU_GFX_OVERTEMP_R
RA807 10K 5% 1/20W MF 201
GPU_VCORE_PCC
GPU_JTAG_TRST_L
GPU_JTAG_TDI
GPU_JTAG_TCK
GPU_JTAG_TMS
GPU_JTAG_TDO
PP3V3_S0_GPU
RA822 10K BOMOPTION=VRAM:GRP2
GPU_VRAM_STRAP
RA823 10K BOMOPTION=VRAM:GRP1
DP_T_SNK0_HPD_EG
DP_T_SNK1_HPD_EG
DP_INT_EG_HPD
GPU_XTAL_OR_CLK_IN
GPU_XTAL_OUT
GPUTHMSNS_D1_P
GPUTHMSNS_D1_N
LA800 120OHM-25%-1.8A-0.06DCR 0402
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.4000
MIN_NECK_WIDTH=0.2000
PP1V8_S0_GPU
PP1V8_GPU_TSVDD
CA850 0.1UF 10% 6.3V X6S 0201
CA851 10UF 20% 6.3V CERM-X6S 0402
CA852 1UF 20% 6.3V X6S-CERM 0201
CA853 0.1UF 10% 6.3V X6S 0201
PLACE_NEAR=LA800.1:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
PLACE_NEAR=UA000.AM13:2.54MM
BOMOPTION=OMIT_TABLE
UA000 100-CK4803-ES BGA SYM 2 OF 7
PLLCHARZ_H
PLLCHARZ_L
BL_ENABLE
BL_PWM_DIM
BP_0
BP_1
DBGDATA_0
DBGDATA_1
DBGDATA_2
DBGDATA_3
DBGDATA_4
DBGDATA_5
DBGDATA_6
DBGDATA_7
DBGDATA_8
DBGDATA_9
DBGDATA_10
DBGDATA_11
DBGDATA_12
DBGDATA_13
DBGDATA_14
DBGDATA_15
WAKE*
RA804 150 1% 1/20W MF 201
GPU_ANALOGIO
ANALOGIO
GPIO_SVC
GPIO_SVD
GPIO_SVT
SWAPLOCKA
SWAPLOCKB
SCL
SDA
GPIO_0
GPIO_1
GPIO_2
SMBCLK
SMBDAT
GPIO_5_REG_HOT_AC_BATT
GPIO_6_TACH
GPIO_8_ROMSO
GPIO_9_ROMSI
GPIO_10_ROMSCK
GPIO_11
GPIO_12
GPIO_13
GPIO_14_HPD2
GPIO_15
GPIO_16_8P_DETECT
GPIO_17_THERMAL_INT
GPIO_18_HPD3
GPIO_19_CTF
GPIO_20
GPIO_21
GPIO_22_ROMCS*
GPIO_28_FDO
GPIO_29
GPIO_30
JTAG_TRST*
JTAG_TDI
JTAG_TCK
JTAG_TMS
JTAG_TDO
GENERICA
GENERICB
GENERICC
GENERICD
GENERICE_HPD4
GENERICF_HPD5
GENERICG
HPD1
XTALIN
XTALOUT
DPLUS
DMINUS
TS_A
TSVDD
TXCAP_DPA3+
TXCAM_DPA3-
TX3P_DPA2+
TX3M_DPA2-
TX4P_DPA1+
TX4M_DPA1-
TX5P_DPA0+
TX5M_DPA0-
TXCBP_DPB3+
TXCBM_DPB3-
TX0P_DPB2+
TX0M_DPB2-
TX1P_DPB1+
TX1M_DPB1-
TX2P_DPB0+
TX2M_DPB0-
TXCCP_DPC3+
TXCCM_DPC3-
TX3P_DPC2+
TX3M_DPC2-
TX4P_DPC1+
TX4M_DPC1-
TX5P_DPC0+
TX5M_DPC0-
TXCDP_DPD3+
TXCDM_DPD3-
librarian reordered pins to follow tx
TX2P_DPD0+
TX2M_DPD0-
TX1P_DPD1+
TX1M_DPD1-
librarian reordered pins to follow tx
TX0P_DPD2+
TX0M_DPD2-
TXCEP_DPE3+
TXCEM_DPE3-
TX0P_DPE2+
TX0M_DPE2-
TX1P_DPE1+
TX1M_DPE1-
TX2P_DPE0+
TX2M_DPE0-
DP_INT_EG_ML_P<3>
DP_INT_EG_ML_N<3>
DP_INT_EG_ML_P<2>
DP_INT_EG_ML_N<2>
DP_INT_EG_ML_P<1>
DP_INT_EG_ML_N<1>
DP_INT_EG_ML_P<0>
DP_INT_EG_ML_N<0>
DP_X_SNK0_ML_C_P<3>
DP_X_SNK0_ML_C_N<3>
DP_X_SNK0_ML_C_P<2>
DP_X_SNK0_ML_C_N<2>
DP_X_SNK0_ML_C_P<1>
DP_X_SNK0_ML_C_N<1>
DP_X_SNK0_ML_C_P<0>
DP_X_SNK0_ML_C_N<0>
DP_X_SNK1_ML_C_P<3>
DP_X_SNK1_ML_C_N<3>
DP_X_SNK1_ML_C_P<2>
DP_X_SNK1_ML_C_N<2>
DP_X_SNK1_ML_C_P<1>
DP_X_SNK1_ML_C_N<1>
DP_X_SNK1_ML_C_P<0>
DP_X_SNK1_ML_C_N<0>
DP_T_SNK0_ML_C_P<3>
DP_T_SNK0_ML_C_N<3>
DP_T_SNK0_ML_C_P<2>
DP_T_SNK0_ML_C_N<2>
DP_T_SNK0_ML_C_P<1>
DP_T_SNK0_ML_C_N<1>
DP_T_SNK0_ML_C_P<0>
DP_T_SNK0_ML_C_N<0>
DP_T_SNK1_ML_C_P<3>
DP_T_SNK1_ML_C_N<3>
DP_T_SNK1_ML_C_P<2>
DP_T_SNK1_ML_C_N<2>
DP_T_SNK1_ML_C_P<1>
DP_T_SNK1_ML_C_N<1>
DP_T_SNK1_ML_C_P<0>
DP_T_SNK1_ML_C_N<0>
HSYNC
VSYNC
DIGON
TEMPIN0
TEMPINRETURN
TEST6
TEST_PG_BACO
GENLK_CLK
GENLK_VSYNC
CLKREQ*
GPU_AUD<1>
GPU_AUD<0>
EG_LCD_PWR_EN
GPU_DIECRACKMON
GPU_TEST_PG_BACON
RA811 0 BOMOPTION=BAFFIN
RA815 10K 5% 1/20W MF 201
RA810 1K 5% 1/20W MF 201
PP1V8_S0_GPU
GPU_CLKREQ_L
DDC1CLK
DDC1DATA
AUX1+
AUX1-
DDC2CLK
DDC2DATA
AUX2+
AUX2-
DDCAUX3+
DDCAUX3-
DDCAUX4+
DDCAUX4-
DDCAUX5+
DDCAUX5-
DDCVGACLK
DDCVGADATA
RSVD
DP_INT_EG_AUX_P
DP_INT_EG_AUX_N
DP_X_SNK0_AUXCH_C_P
DP_X_SNK0_AUXCH_C_N
DP_X_SNK1_AUXCH_C_P
DP_X_SNK1_AUXCH_C_N
DP_T_SNK0_AUXCH_C_P
DP_T_SNK0_AUXCH_C_N
DP_T_SNK1_AUXCH_C_P
DP_T_SNK1_AUXCH_C_N
GPU_PLLCHARZ_H
GPU_PLLCHARZ_L
CA880 0.1UF 10% 6.3V X6S 0201
CA881 0.1UF 10% 6.3V X6S 0201
RA880 51.1 1% 1/20W MF 201
RA881 51.1 1% 1/20W MF 201
GPU_PLLCHARZ_RC_H
GPU_PLLCHARZ_RC_L
BOM_COST_GROUP=GRAPHICS
PAGE TITLE
Baffin DP/GPIO
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 108 OF 145
SHEET 99 OF 121
NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



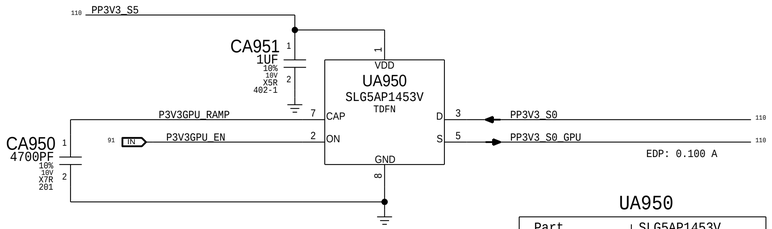
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S00897	1	IC,TPS62130B-S,3A BUCK CNVTRT,QFN16,3X3M	UA900	CRITICAL	



GPU THERMAL



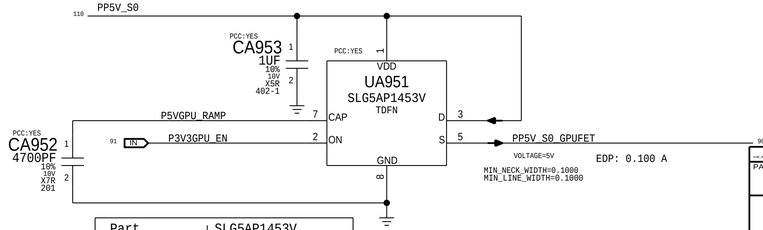
3.3V S0 GPU Switch



UA950

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

5V S0 GPU Switch



UA951

Part	SLG5AP1453V
Type	Load Switch
R(on) @ 5.3A	7.8 mOhm Typ 9.6 mOhm Max
Current	5.3A Max

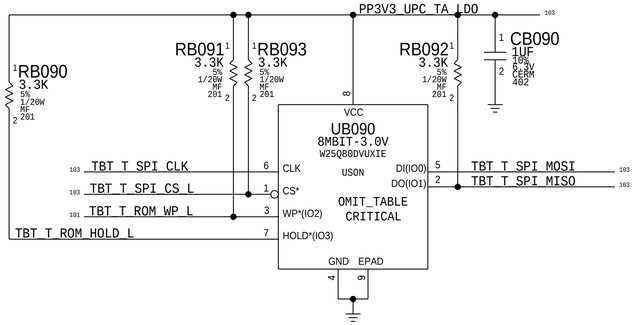
BOM_COST_GROUP=GRAPHICS

PAGE TITLE: Baffin VSS & MISC

Apple Inc.

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	109 OF 145
SHEET	100 OF 121



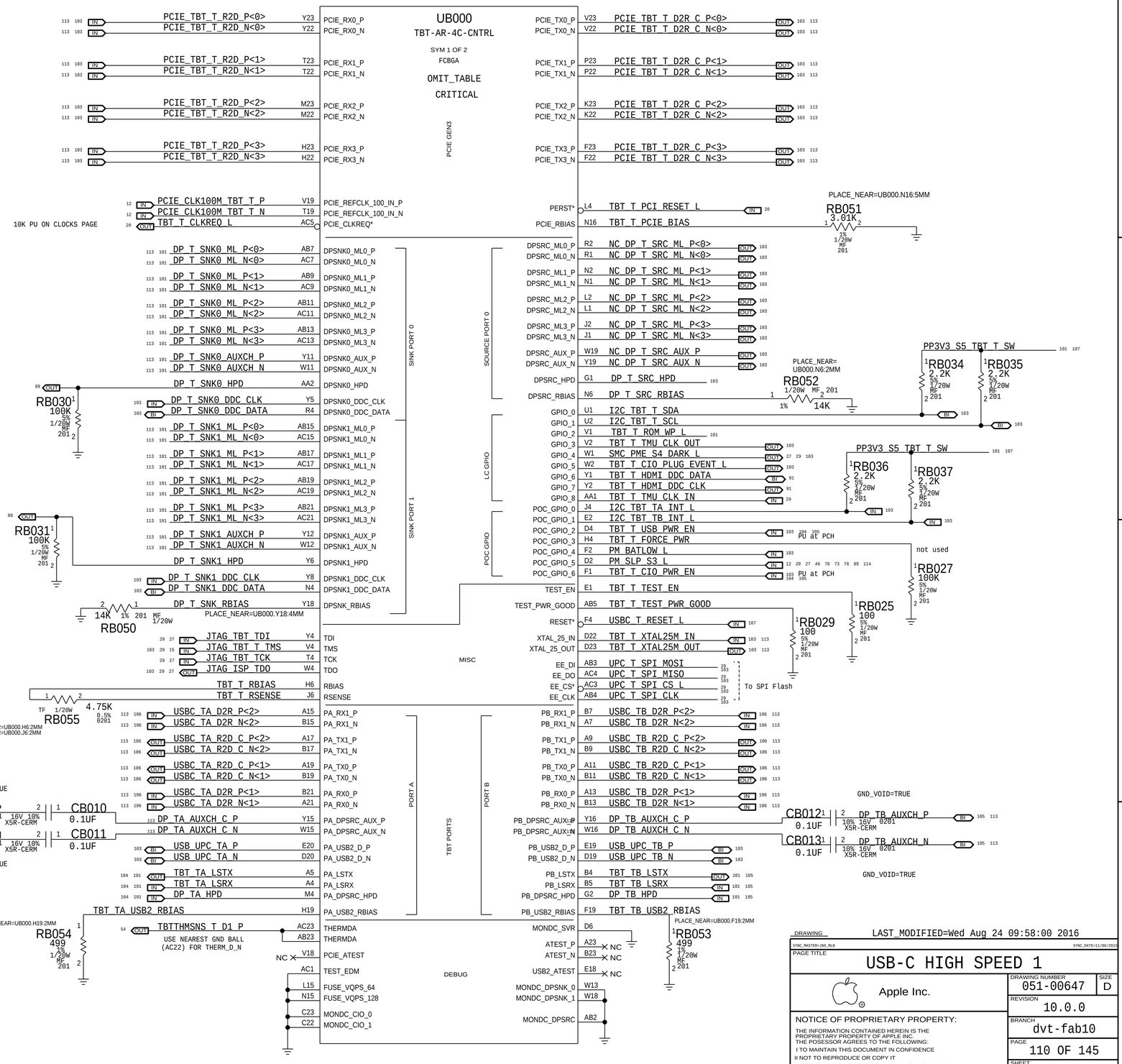
SNK0 AC Coupling

DP_T_SNK0_ML_C_P<0>	CB020 0.1UF	DP_T_SNK0_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<0>	CB021 0.1UF	DP_T_SNK0_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<1>	CB022 0.1UF	DP_T_SNK0_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<1>	CB023 0.1UF	DP_T_SNK0_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<2>	CB024 0.1UF	DP_T_SNK0_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<2>	CB025 0.1UF	DP_T_SNK0_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_P<3>	CB026 0.1UF	DP_T_SNK0_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK0_ML_C_N<3>	CB027 0.1UF	DP_T_SNK0_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_P	CB028 0.1UF	DP_T_SNK0_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK0_AUXCH_C_N	CB029 0.1UF	DP_T_SNK0_AUXCH_N	GND_VOID=TRUE	

SNK1 AC Coupling

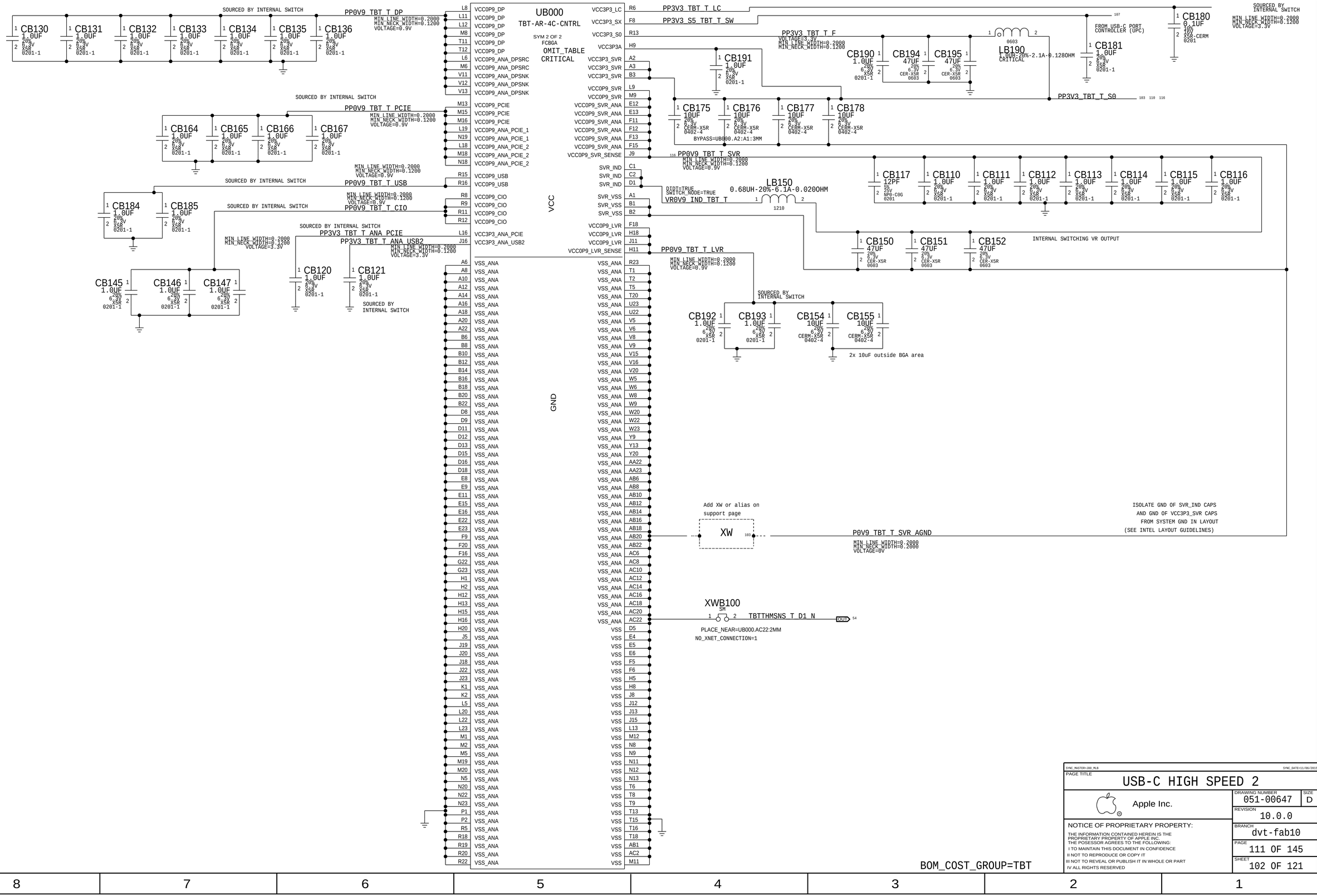
DP_T_SNK1_ML_C_P<0>	CB030 0.1UF	DP_T_SNK1_ML_P<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<0>	CB031 0.1UF	DP_T_SNK1_ML_N<0>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<1>	CB032 0.1UF	DP_T_SNK1_ML_P<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<1>	CB033 0.1UF	DP_T_SNK1_ML_N<1>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<2>	CB034 0.1UF	DP_T_SNK1_ML_P<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<2>	CB035 0.1UF	DP_T_SNK1_ML_N<2>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_P<3>	CB036 0.1UF	DP_T_SNK1_ML_P<3>	GND_VOID=TRUE	
DP_T_SNK1_ML_C_N<3>	CB037 0.1UF	DP_T_SNK1_ML_N<3>	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_P	CB038 0.1UF	DP_T_SNK1_AUXCH_P	GND_VOID=TRUE	
DP_T_SNK1_AUXCH_C_N	CB039 0.1UF	DP_T_SNK1_AUXCH_N	GND_VOID=TRUE	

RB062 100K 5% 1/20W MF 201	DP_TA_HPD	
RB072 100K 5% 1/20W MF 201	DP_TB_HPD	
RB060 1M 5% 1/20W MF 201	TBT_TA_LSTX	
RB061 1M 5% 1/20W MF 201	TBT_TA_LSRX	
RB070 1M 5% 1/20W MF 201	TBT_TB_LSTX	
RB071 1M 5% 1/20W MF 201	TBT_TB_LSRX	



DRAWING
LAST_MODIFIED=Wed Aug 24 09:58:00 2016
SYNC_MASTER=J89_MLB
SYNC_DATE=11/06/2015
PAGE TITLE
USB-C HIGH SPEED 1
Apple Inc.
DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 110 OF 145
SHEET 101 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



SYNC_MASTER=J80_MLB	SYNC_DATE=11/06/2015
PAGE TITLE	USB-C HIGH SPEED 2
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 111 OF 145
	SHEET 102 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

TMU CLKs

TBT_T_TMU_CLK_OUT → RB225 15 (5% 1/20W MF 201, MAKE_BASE=TRUE) → TBT_X_TMU_CLK_IN (MAKE_BASE=TRUE)
TBT_T_TMU_CLK_OUT (MAKE_BASE=TRUE)
PLACE_NEAR=UB000.V2:5mm
TBT_X_TMU_CLK_IN → RB226 100K (5% 1/20W MF 201)

DP SRC OPTIONS

IF DP SRC NOT USED

DP_T_SRC_HPD → RB240 1M (5% 1/20W MF 201)

NC_DP_T_SRC_ML_P<3..0>	NC_DP_T_SRC_ML_P<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_T_SRC_ML_N<3..0>	NC_DP_T_SRC_ML_N<3..0>	MAKE_BASE=TRUE, NO_TEST=1
NC_DP_T_SRC_AUX_P	NC_DP_T_SRC_AUX_P	MAKE_BASE=TRUE
NC_DP_T_SRC_AUX_N	NC_DP_T_SRC_AUX_N	MAKE_BASE=TRUE

FUSES FOR UPC

PP20V_USBC_TA_VBUS → FB200 (PLACE_NEAR=QB300:5MM, CRITICAL, 0603, 6AMP-32V-0.0095OHM) → PP20V_USBC_TA_VBUS_F
PP20V_USBC_TB_VBUS → FB201 (PLACE_NEAR=QB400:5MM, CRITICAL, 0603, 740S0135, 6AMP-32V-0.0095OHM) → PP20V_USBC_TB_VBUS_F

25MHz xtal

TBT_T_XTALIN25M_OUT → RB207 0 (5% 1/20W MF 201) → TBT_T_XTALIN25M_OUT_R
NOSTUFF RB206 1M (5% 1/20W MF 201) to/from Ridge
CRITICAL YB200 25MHZ-25PPM-20PF-50OHM 2.00X1.60-SM
CB202 20PF (5% 25V C0G 0201)
CB203 20PF (5% 25V C0G 0201)
TBT_T_XTALIN25M_IN

AR/ACE SPI BUS SERIES R'S

ROM: TBT_T_SPI_CLK, TBT_T_SPI_CS_L, TBT_T_SPI_MOSI, TBT_T_SPI_MISO
RB290 100 (5% 1/20W MF 201) TBT_T_SPI_CLK_DBG

RB280	UPC_TA_SPI_CLK	IN	Ace
RB281	UPC_TA_SPI_CS_L	IN	Ace
RB282	UPC_TA_SPI_MOSI	IN	Ace
RB283	UPC_TA_SPI_MISO	OUT	Ace
RB284	UPC_T_SPI_CLK	IN	AR
RB285	UPC_T_SPI_CS_L	IN	AR
RB286	UPC_T_SPI_MOSI	IN	AR
RB287	UPC_T_SPI_MISO	OUT	AR

(15 5% 1/20W MF 201)

TP UPC TA SWD DATA / CLK, TP UPC TB SWD DATA / CLK

TP UPC TA SWD DATA → TPB201
TP UPC TA SWD CLK → TPB202
TP UPC TB SWD DATA → TPB203
TP UPC TB SWD CLK → TPB204
(TP-P5)

ACE Debug Support

OMIT RB289 (NOSTUFF NONE 402): TP_UPC_TA_DBG_UART_TX → TP_UPC_TA_DBG_UART_RX
OMIT RB288 (NOSTUFF NONE 402): TP_UPC_TB_DBG_UART_TX → TP_UPC_TB_DBG_UART_RX

USBC 5V EN PD

UPC_T_5V_EN → RB232 100K (5% 1/20W MF 201)

Ridge PDs

DP_T_SNK0_DDC_CLK	RB267	DP_T_SNK0_DDC_CLK
DP_T_SNK0_DDC_DATA	RB268	DP_T_SNK0_DDC_DATA
DP_T_SNK1_DDC_CLK	RB269	DP_T_SNK1_DDC_CLK
DP_T_SNK1_DDC_DATA	RB270	DP_T_SNK1_DDC_DATA

(MAKE_BASE=TRUE; 100K 5% 1/20W MF 201)

ACE FET DCIN Bypass Caps

PPDCIN_G3H → CB211 0.1UF, CB212 0.1UF, CB213 0.1UF, CB214 0.1UF (10% 35V CER-X5R 0201)

ACE A/B RPD STRAPPING

USBC_TA_CC1	USBC_TA_CC1
USBC_TB_CC1	USBC_TB_CC1
USBC_TA_CC2	USBC_TA_CC2
USBC_TB_CC2	USBC_TB_CC2

(MAKE_BASE=TRUE)

ACE PDs

UPC_TA_DBG3	RB260	UPC_TA_DBG3
UPC_TA_DBG4	RB261	UPC_TA_DBG4
UPC_TB_DBG3	RB262	UPC_TB_DBG3
UPC_TB_DBG4	RB263	UPC_TB_DBG4
UPC_TA_DBG1	RB264	UPC_TA_DBG1
UPC_TA_DBG2	RB265	UPC_TA_DBG2
UPC_TA_HPD_RX	RB233	UPC_TA_HPD_RX
UPC_TB_HPD_RX	RB234	UPC_TB_HPD_RX

(100K 5% 1/20W MF 201)

RIDGE 0.9V SVR XW

XWB200 SM: P0V9_TBT_T_SVR_AGND → NO_XNET_CONNECTION=1

I2C SERIES R'S

SMBUS_SMC_4_G3H_SDA → RB241 33 (PLACE_NEAR=U5000:5mm) → I2C_UPC_T_SDA2
SMBUS_SMC_4_G3H_SCL → RB242 33 (PLACE_NEAR=U5000:5mm) → I2C_UPC_T_SCL2
(5% 1/20W MF 201, MAKE_BASE=TRUE)

ACE DEBUG CONN

Place on bottom
USBC_DBG JB200 505070-1220 M-ST-SM

I2C_TBT_TB_INT_L	1	2	I2C_TBT_TA_INT_L
I2C_UPC_T_SCL2	3	4	I2C_TBT_T_SDA
I2C_UPC_T_SDA2	5	6	I2C_TBT_T_SCL
SMC_USBC_INT_L	7	8	TBT_T_CIO_PWR_EN
TBT_T_SPI_CLK_DBG	9	10	TBT_T_USB_PWR_EN
UPC_TA_UART_TX	11	12	UPC_TA_UART_RX
	15	16	

TBT to ACE

TBT (Alpine Ridge U2800, MASTER) ↔ Pri ACE (U3100, Write: 0x70 Read: 0x71)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TA_INT_L	I2C_TBT_TA_INT_L
I2C_TBT_TB_INT_L	

TBT ↔ Sec ACE (U3200, Write: 0x7E Read: 0x7F)

I2C_TBT_T_SCL	I2C_TBT_T_SCL
I2C_TBT_T_SDA	I2C_TBT_T_SDA
I2C_TBT_TB_INT_L	I2C_TBT_TB_INT_L

(MAKE_BASE=TRUE)

SIGNAL ALIASES

USB2_UPC_TB_P	RB252 0	USB_UPC_PCH_TB_P
USB2_UPC_TB_N	RB253 0	USB_UPC_PCH_TB_N
USB2_UPC_TA_P	RB256 0	USB_UPC_PCH_TA_P
USB2_UPC_TA_N	RB257 0	USB_UPC_PCH_TA_N

(5% MF 1/20W 0201)

TBT_T_CIO_PWR_EN	TBT_T_CIO_PWR_EN
TBT_T_USB_PWR_EN	TBT_T_USB_PWR_EN
PM_BATLOW_L	PM_BATLOW_L
SMC_PME_S4_DARK_L	SMC_PME_S4_DARK_L
UPC_T_5V_EN	UPC_T_5V_EN
JTAG_ISP_TDO	JTAG_ISP_TDO
SMC_USBC_INT_L	SMC_USBC_INT_L
SMC_USBC_INT_L	
SSD_DEBUG_I2C_CLK_CONN	SSD_DEBUG_I2C_CLK_CONN
SSD_DEBUG_I2C_DAT_CONN	SSD_DEBUG_I2C_DAT_CONN
TBT_T_CIO_PLUG_EVENT_L	TBT_T_CIO_PLUG_EVENT_L
UPC_TA_FAULT_L	XDP_PCH_OBSDATA_C2 (RB258 0)
UPC_TB_FAULT_L	XDP_PCH_OBSDATA_C3 (RB259 0)
JTAG_TBT_T_TMS	JTAG_TBT_T_TMS
PP3V3_S4	PP3V3_S4
TP_USBC_TB_RESET_L	TP_USBC_TB_RESET_L
TBT_POC_RESET	TBT_POC_RESET

(MAKE_BASE=TRUE)

USB_UPC_TB_P / USB_UPC_TB_N / USB_UPC_TA_P / USB_UPC_TA_N

RB250 0	USB_UPC_TB_P	NOSTUFF
RB251 0	USB_UPC_TB_N	NOSTUFF
RB354 0	USB_UPC_TA_P	NOSTUFF
RB255 0	USB_UPC_TA_N	NOSTUFF

(5% MF 1/20W 0201)

POWER ALIASES

PP3V3_UPC_TA_LDO	PP3V3_UPC_TA_LDO
PP20V_USBC_TA_VBUS	PP20V_USBC_TA_VBUS
PP20V_USBC_TB_VBUS	PP20V_USBC_TB_VBUS
PP3V3_UPC_TB_LDO	PP3V3_UPC_TB_LDO
PP5V_S4_T_USBC	PP5V_S4_T_USBC (MIN_LINE_WIDTH=0.6000 MIN_NECK_WIDTH=0.1200 VOLTAGE=5V)
PP3V3_TBT_T_S0	PP3V3_TBT_T_S0 (MIN_LINE_WIDTH=0.2000 MIN_NECK_WIDTH=0.1200 VOLTAGE=3.3V)

(MAKE_BASE=TRUE)

Ridge PCIE Caps

R2D: PCIE_TBT_T_R2D_C_P<0> → PCIE_TBT_T_R2D_P<0> (CB240) … PCIE_TBT_T_R2D_C_N<3> → PCIE_TBT_T_R2D_N<3> (CB247)
D2R: PCIE_TBT_T_D2R_C_P<0> → PCIE_TBT_T_D2R_P<0> (CB250) … PCIE_TBT_T_D2R_C_N<3> → PCIE_TBT_T_D2R_N<3> (CB257)
(GND_VOID=TRUE; 0201 X5R 6.3V 20% 0.22UF)

NO TEST

NC_UPC_TB_I2C_ADDR

GND ALIASES

GND (MAKE_BASE=TRUE) → BOM_COST_GROUP=TBT

PAGE TITLE	USB-C Support
Apple Inc.	
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	112 OF 145
SHEET	103 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PRIMARY ACE USB-C PORT CONTROLLER (UPC)

QB300
FDPC4044
PWR-CLIP-33

FUSE
Add on support page

PP20V_USBC_TA_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

PP20V_USBC_TA_VBUS
CB301 1UF 10% 35V X5R 0402

PP3V3_UPC_TA_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB300 10UF 20% 6.3V X5R-CERM-X5R 0402-1

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL
UPC_TA_GATE1
TP_QB300_DRAIN
UPC_TA_GATE2

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V

PP3V3_UPC_TA_LDO
P3V3_TBT_T_SX_EN_R
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
PP1V8_UPC_TA_LDOA
PP1V8_UPC_TA_LDOD
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V
CB306 0.47UF 10% 6.3V CERM-X5R 0201

PP1V1_UPC_TA_LDO_BMC
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V
CB305 1.0UF 20% 6.3V X5R 0201-1
CB308 10UF 20% 6.3V X5R-CERM-X5R 0402-1
CB304 2.2UF 20% 6.3V X5R-CERM 0201

PULL R3109 AND R3108 UP TO ACEs LDOs FOR 1ST RIDGE'S ACES
PULL R3109 AND R3108 DOWN TO GND FOR 2ND RIDGE'S ACES

GND
RB309 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SCL
RB308 1M 5% 1/20W MF 201 — I2C_UPC_TA_DBG_CTL_SDA

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

USE GPIO2 FOR USB-C ANALOG AUDIO SUPPORT ON DESIGNS WITHOUT AN AUDIO JACK CONNECTOR

USE GPIO3 FOR POWER_GATE_EN ON BANSURI DESIGNS

UB300
CD3215A
BGA

TBT_POC_RESET	E11	MRESET	PRIMARY ONLY
USBC_T_RESET_L_R	F11	RESET*	PRIMARY ONLY
TP_UPC_TA_DBG_UART_TX	B2	GPIO0	
TP_UPC_TA_DBG_UART_RX	C2	GPIO1	
TBT_T_CIO_PWR_EN	D10	GPIO2	
TBT_T_USB_PWR_EN	G11	GPIO3	
DP_TA_HPD	C10	GPIO4	
UPC_TA_HPD_RX	E10	GPIO5	
UPC_T_5V_EN	G10	GPIO6	
SMC_PME_S4_DARK_L	D7	GPIO7	
UPC_TA_FAULT_L	H6	GPIO8	
GND	F10	BUSPOWERZ	
UPC_TA_I2C_ADDR	F1	I2C_ADDR	
UPC_TA_R_OSC	G2	R_OSC	
I2C_UPC_TA_DBG_CTL_SCL	E4	DEBUG_CTL1	
I2C_UPC_TA_DBG_CTL_SDA	D5	DEBUG_CTL2	
I2C_TBT_T_SDA	D1	I2C_SDA1	
I2C_TBT_T_SCL	D2	I2C_SCL1	
I2C_TBT_TA_INT_L	C1	I2C_IRQ1*	
I2C_UPC_T_SDA2	A5	I2C_SDA2	
I2C_UPC_T_SCL2	B5	I2C_SCL2	
SMC_USBC_INT_L	B6	I2C_IRQ2*	
UPC_TA_SPI_CLK	A3	SPI_CLK	
UPC_TA_SPI_MOSI	B4	SPI_MOSI	
UPC_TA_SPI_MISO	A4	SPI_MISO	
UPC_TA_SPI_CS_L	B3	SPI_SSZ	
TP_UPC_TA_SWD_DATA	F4	SWD_DATA	
TP_UPC_TA_SWD_CLK	G4	SWD_CLK	
UPC_TA_UART_RX	F2	UART_RX	
UPC_TA_UART_TX	E2	UART_TX	
TBT_TA_LSTX	L4	LSX_R2P	
TBT_TA_LSRX	K4	LSX_P2R	
USB_UPC_TA_F_P	L5	USB_RP_P	
USB_UPC_TA_F_N	K5	USB_RP_N	
DP_TA_AUXCH_P	J1	AUX_P	
DP_TA_AUXCH_N	J2	AUX_N	
UPC_TA_DBG1	L2	DEBUG1	
UPC_TA_DBG2	K2	DEBUG2	
UPC_TA_DBG3	L3	DEBUG3	
UPC_TA_DBG4	K3	DEBUG4	

CRITICAL
OMIT_TABLE

DIGITAL CORE I/O AND CONTROL
HV FET/SENSE
TYPE-C
PORT MUX

SS H7 — UPC_TA_SS
SENSEP B10
SENSEN A10
HV_GATE1 B9
HV_GATE2 A9
CB309 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 L9 — USBC_TA_CC1
C_CC2 L10 — USBC_TA_CC2
RPD_G1 K9 — USBC_TA_CC1
RPD_G2 K10 — USBC_TA_CC2
C_USB_TP K6 — USBC_TA_USB_TOP_P
C_USB_TN L6 — USBC_TA_USB_TOP_N
C_USB_BP K7 — USBC_TA_USB_BOT_P
C_USB_BN L7 — USBC_TA_USB_BOT_N
C_SBU1 K8 — USBC_TA_SBU1
C_SBU2 L8 — USBC_TA_SBU2
CB314 220PF 10% 16V CER-X7R 0201
CB313 220PF 10% 16V CER-X7R 0201

MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

NC L11 — GROUND
NC or GND to dissipate heat

GND I2C ADDR PRIMARY ONLY
RB302 0 5% 1/20W MF 201
CRITICAL
RB303 15K 0.1% 1/20W TF-LT 0201
NEED 0.1%

UPC_TA_UART_RX
RB305 1M 5% 1/20W MF 201

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

LB300
90-OHM-0.1A
EXCX4CE

USB2_UPC_TA_P — PLACE_NEAR=UB300.L5:5mm
USB2_UPC_TA_N — PLACE_NEAR=UB300.K5:5mm

PP3V3_S4
PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
RB310 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1
RB311 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

GND (A1, D6, E5, E6, E7, F5, G5, H4, H5, G8, H8, L1, B8, D8, E8, F6, F7, F8, G6, G7)

PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER A
Apple Inc.	
DRAWING NUMBER	051-00647
SIZE	D
REVISION	10.0.0
BRANCH	dvt-fab10
PAGE	113 OF 145
SHEET	104 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SECONDARY ACE USB-C PORT CONTROLLER (UPC)

PULL R3209 AND R3208 UP TO ACE$_1$ LDOs FOR 1ST RIDGE'S ACES
PULL R3209 AND R3208 DOWN TO GND FOR 2ND RIDGE'S ACES

GND
1M RB409 I2C_UPC_TB_DBG_CTL_SCL
1M RB408 I2C_UPC_TB_DBG_CTL_SDA
5% 1/20W MF 201

1M RB405 UPC_TA_UART_TX

CRITICAL
RB403 15K 0.1% 1/20W TF-LF 0201
NEED 0.1%

TO SMC

REAR PORT: CONNECT UPC SPI TO ROM
FRONT PORT: GROUND UPC SPI

TESTPOINTS MUST BE PRESENT FOR GPIO0, GPIO1 (EVEN IN PRODUCTION)

PU to PP3V3_S4 if convenient for layout.
Otherwise PU to PP3V3_UPC_XA_LDO
NO_XNET_CONNECTION=1

RB410 100K 5% 1/20W MF 201
RB411 100K 5% 1/20W MF 201
NO_XNET_CONNECTION=1

LB400 90-OHM-0.1A EXCX4CE

QB400 FDPC4044 PWR-CLIP-33

FUSE Add on support page

PP20V_USBC_TB_VBUS_F
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=20V

NC

PP20V_USBC_TB_VBUS
CB401 1UF 10% 25V X5R 0402

PPDCIN_G3H
MAX 100uF TOTAL ON RAIL

UPC_TB_GATE1
TP_QB400_DRAIN
UPC_TB_GATE2

PP3V3_UPC_TB_LDO
PP3V3_G3H
GND
PP5V_S4_T_USBC
CAP FOR PP_5V0 ON VR PAGE
CB400 10UF 20% 6.3V CERM-X5R 0402-1

PP3V3_UPC_TB_LDO
P3V3_TBT_T_SX_EN_R
PP1V8_UPC_TB_LDOA
PP1V8_UPC_TB_LDOD
PP1V1_UPC_TB_LDO_BMC
CB405 1.0UF 20% 6.3V X5R 0201-1
CB408 10UF 20% 6.3V CERM-X5R 0402-1
CB404 2.2UF 20% 4V X5R-CERM 0201
CB406 0.47UF 10% 6.3V CERM-X5R 0201
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=3.3V
VOUT 3V3 FOR RIDGE, OR FLOAT IF UNUSED
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.1V
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
VOLTAGE=1.8V

UB400 CD3215A BGA
CRITICAL
OMIT_TABLE

TBT_POC_RESET — MRESET
TP_USBC_TB_RESET_L — RESET*
TP_UPC_TB_DBG_UART_TX — GPIO0
TP_UPC_TB_DBG_UART_RX — GPIO1
TBT_T_CIO_PWR_EN — GPIO2
TBT_T_USB_PWR_EN — GPIO3
DP_TB_HPD — GPIO4
UPC_TB_HPD_RX — GPIO5
UPC_T_5V_EN — GPIO6
SMC_PME_S4_DARK_L — GPIO7
UPC_TB_FAULT_L — GPIO8
GND — BUSPOWERZ
NC_UPC_TB_I2C_ADDR — I2C_ADDR
UPC_TB_R_OSC — R_OSC
I2C_UPC_TB_DBG_CTL_SCL — DEBUG_CTL1
I2C_UPC_TB_DBG_CTL_SDA — DEBUG_CTL2
I2C_TBT_T_SDA — I2C_SDA1
I2C_TBT_T_SCL — I2C_SCL1
I2C_TBT_TB_INT_L — I2C_IRQ1*
I2C_UPC_T_SDA2 — I2C_SDA2
I2C_UPC_T_SCL2 — I2C_SCL2
SMC_USBC_INT_L — I2C_IRQ2*
GND — SPI_CLK
GND — SPI_MOSI
GND — SPI_MISO
GND — SPI_SSZ
TP_UPC_TB_SWD_DATA — SWD_DATA
TP_UPC_TB_SWD_CLK — SWD_CLK
UPC_TA_UART_TX — UART_RX
UPC_TA_UART_RX — UART_TX
TBT_TB_LSTX — LSX_R2P
TBT_TB_LSRX — LSX_P2R
USB_UPC_TB_F_P — USB_RP_P
USB_UPC_TB_F_N — USB_RP_N
DP_TB_AUXCH_P — AUX_P
DP_TB_AUXCH_N — AUX_N
SSD_DEBUG_I2C_CLK_CONN — DEBUG1
SSD_DEBUG_I2C_DAT_CONN — DEBUG2
UPC_TB_DBG3 — DEBUG3
UPC_TB_DBG4 — DEBUG4

USB2_UPC_TB_P — PLACE_NEAR=UB400.L5:5mm
USB2_UPC_TB_N — PLACE_NEAR=UB400.K5:5mm

HV FET/SENSE
DIGITAL CORE I/O AND CONTROL
TYPE-C
PORT MUX

SS — UPC_TB_SS
SENSEP
SENSEN
HV_GATE1
HV_GATE2
CB409 0.47UF 10% 6.3V CERM-X5R 0201

C_CC1 — USBC_TB_CC1
C_CC2 — USBC_TB_CC2
RPD_G1 — USBC_TB_CC1
RPD_G2 — USBC_TB_CC2
C_USB_TP — USBC_TB_USB_TOP_P
C_USB_TN — USBC_TB_USB_TOP_N
C_USB_BP — USBC_TB_USB_BOT_P
C_USB_BN — USBC_TB_USB_BOT_N
C_SBU1 — USBC_TB_SBU1
C_SBU2 — USBC_TB_SBU2
CB414 220PF 10% 16V CER-X7R 0201
CB413 220PF 10% 16V CER-X7R 0201
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200
MIN_LINE_WIDTH=0.2000
MIN_NECK_WIDTH=0.1200

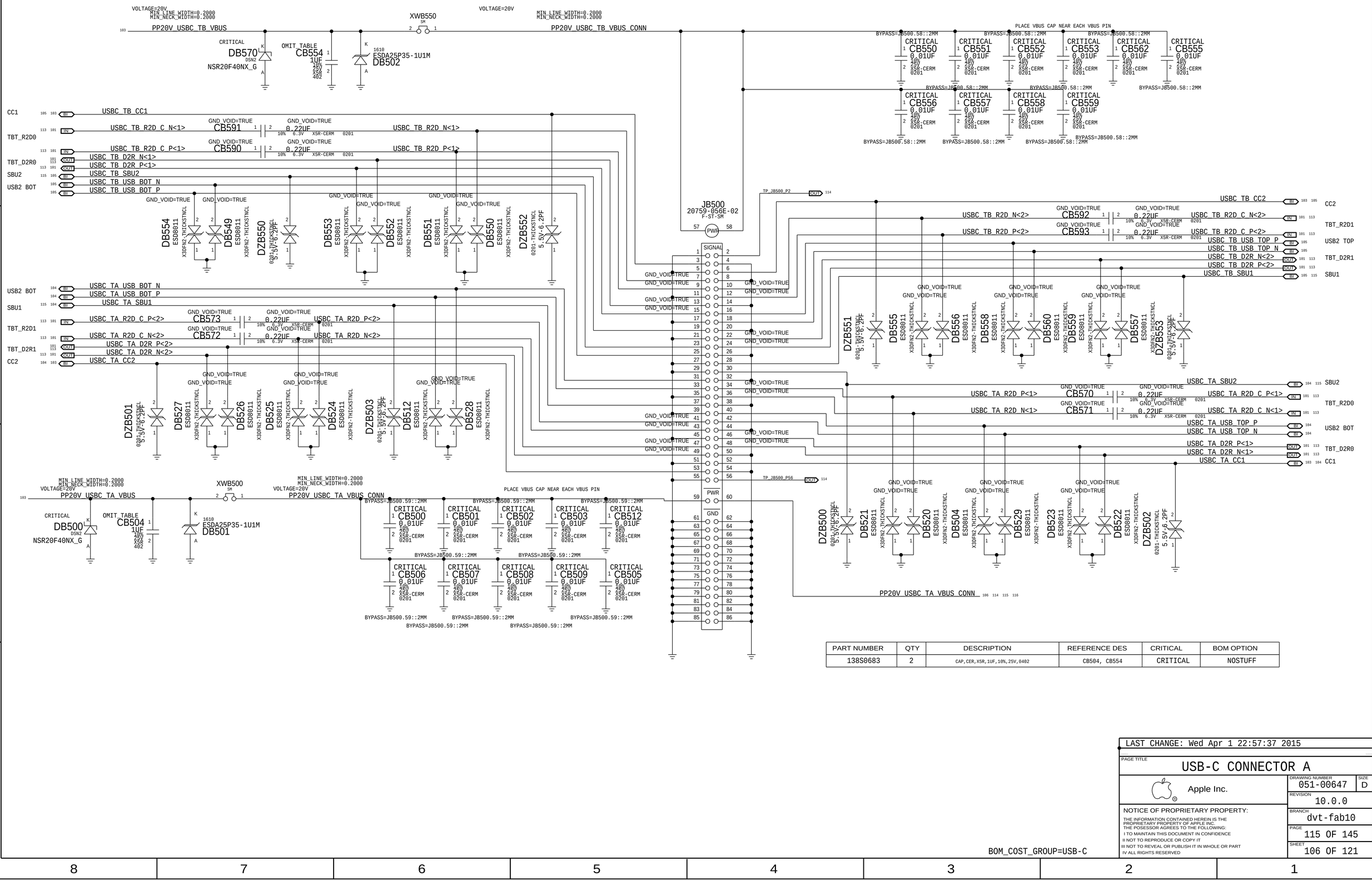
NC — GROUND
NC or GND to dissipate heat

A1 D6 E5 E6 E7 F5 G5 H4 H5 G8 H8 L1 B8 D8 E8 F6 F7 F8 G6 G7 — GND
GND
PIN D6 IS UNDOCUMENTED RESET
CAN GROUND PIN D6 IN PRODUCTION

BOM_COST_GROUP=USB-C

PAGE TITLE	USB-C PORT CONTROLLER B
Apple Inc.	DRAWING NUMBER 051-00647 · SIZE D
	REVISION 10.0.0
	BRANCH dvt-fab10
	PAGE 114 OF 145
	SHEET 105 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0683	2	CAP,CER,X5R,1UF,10%,25V,0402	CB504, CB554	CRITICAL	NOSTUFF

BOM_COST_GROUP=USB-C

LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE: USB-C CONNECTOR A

Apple Inc.

DRAWING NUMBER: 051-00647 SIZE: D

REVISION: 10.0.0

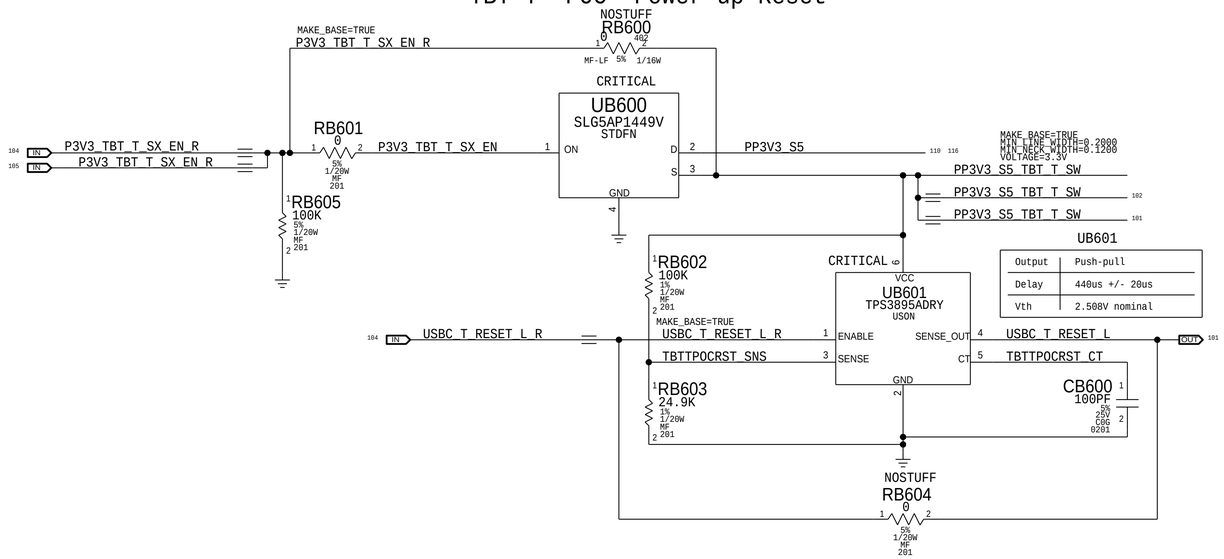
BRANCH: dvt-fab10

PAGE: 115 OF 145

SHEET: 106 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

TBT T "POC" Power-up Reset



BOM_COST_GROUP=USB-C

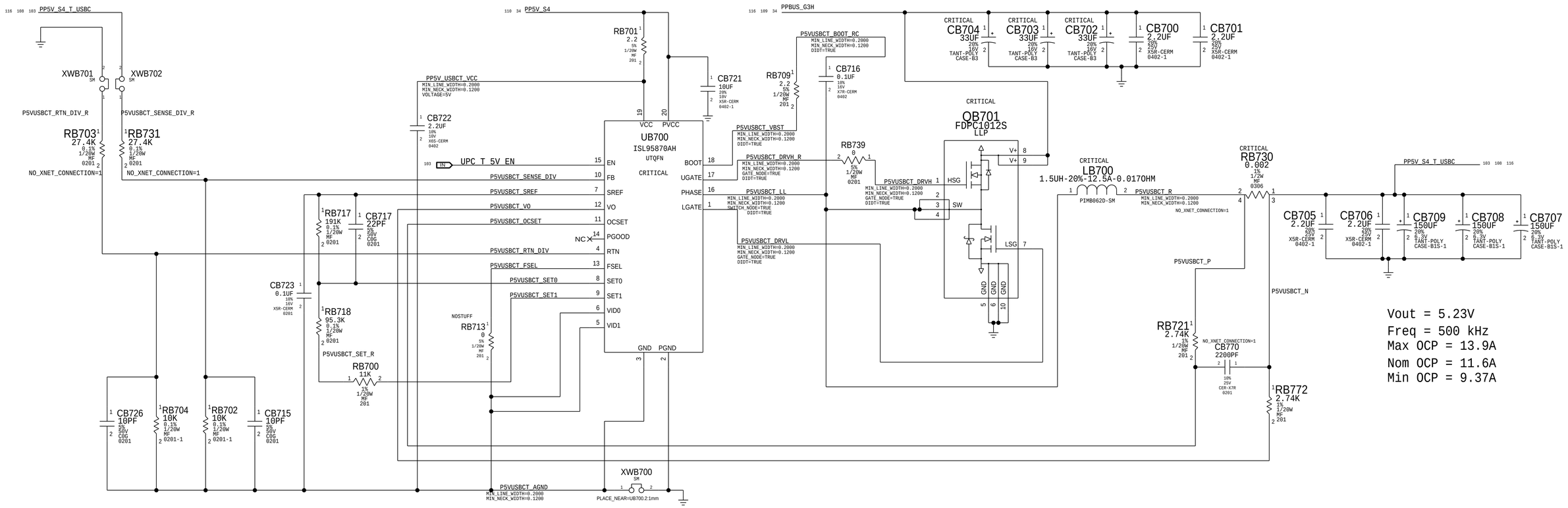
DESIGN: j130/dev_mlb_u
LAST CHANGE: Wed Apr 1 22:57:37 2015

PAGE TITLE
USB-C CONNECTOR B

Apple Inc.

DRAWING NUMBER 051-00647
SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 116 OF 145
SHEET 107 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM_COST_GROUP=USB-C

PAGE TITLE

TBT 5V REGULATOR

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 117 OF 145

SHEET 108 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PBUS Rails

116 64 PPBUS_G3H
- PPBUS_G3H — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 114
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 75
- PPBUS_G3H — 50
- PPBUS_G3H — 50
- PPBUS_G3H — 70
- PPBUS_G3H — 63
- PPBUS_G3H — 72
- PPBUS_G3H — 34 108 116
- PPBUS_G3H — 55
- PPBUS_G3H — 60 61
- PPBUS_G3H — 72

50 PPBUS_HS_CPU
- PPBUS_HS_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.2000, VOLTAGE=13.1V, MAKE_BASE=TRUE — 117
- PPBUS_HS_CPU — 66
- PPBUS_HS_CPU — 67
- PPBUS_HS_CPU — 68
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 71
- PPBUS_HS_CPU — 65

55 PPBUS_HS_GPU
- PPBUS_HS_GPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE — 97
- PPBUS_HS_GPU — 94
- PPBUS_HS_GPU — 97
- PPBUS_HS_GPU — 94
- PPBUS_HS_GPU — 100

50 PPBUS_HS_OTH5V
- PPBUS_HS_OTH5V — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH5V — 69 117

117 50 PPBUS_HS_OTH3V3
- PPBUS_HS_OTH3V3 — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_HS_OTH3V3 — 69 117

50 PPBUS_S4_HS_TPAD
- PPBUS_S4_HS_TPAD — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=13.1V, MAKE_BASE=TRUE
- PPBUS_S4_HS_TPAD — 43

3V3 G3H Rails

63 PP3V3_G3H
- PP3V3_G3H — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.3V, MAKE_BASE=TRUE — 114
- PP3V3_G3H — 57
- PP3V3_G3H — 46 47 76
- PP3V3_G3H — 48
- PP3V3_G3H — 64
- PP3V3_G3H — 43 48
- PP3V3_G3H — 49
- PP3V3_G3H — 48
- PP3V3_G3H — 47
- PP3V3_G3H — 20
- PP3V3_G3H — 49
- PP3V3_G3H — 30
- PP3V3_G3H — 31
- PP3V3_G3H — 29
- PP3V3_G3H — 104
- PP3V3_G3H — 105

RTC Rails

70 PP3V0_G3H
- PP3V0_G3H — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=3.0V, MAKE_BASE=TRUE
- PP3V0_G3H — 12 16 17
- PP3V0_G3H — 70

IMVP Rails

66 PPVCC_S0_CPU
- PPVCC_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 114
- PPVCC_S0_CPU — 6 8 55
- PPVCC_S0_CPU — 10

67 PPVCCSA_S0_CPU
- PPVCCSA_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.15V, MAKE_BASE=TRUE
- PPVCCSA_S0_CPU — 8 53
- PPVCCSA_S0_CPU — 11

68 PPVCCGT_S0_CPU
- PPVCCGT_S0_CPU — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PPVCCGT_S0_CPU — 8 55
- PPVCCGT_S0_CPU — 11 116

CPU VCCIO Rails

117 71 PPVCCIO_S0_CPU
- PPVCCIO_S0_CPU — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.95V, MAKE_BASE=TRUE — 10
- PPVCCIO_S0_CPU — 5 8

1V2 Rails

117 74 71 PP1V2_S3
- PP1V2_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S3 — 22 23 24 25 116
- PP1V2_S3 — 71 117
- PP1V2_S3 — 21
- PP1V2_S3 — 22 23 24 25
- PP1V2_S3 — 22 23 24 25 116
- PP1V2_S3 — 51
- PP1V2_S3 — 74

51 PP1V2_S3_CPUDDR
- PP1V2_S3_CPUDDR — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S3_CPUDDR — 8
- PP1V2_S3_CPUDDR — 10 116

74 PP1V2_S0SW
- PP1V2_S0SW — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.2V, MAKE_BASE=TRUE
- PP1V2_S0SW — 8

0V6 Rails

117 71 PP0V6_S0_DDRVTT
- PP0V6_S0_DDRVTT — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=0.6V, MAKE_BASE=TRUE
- PP0V6_S0_DDRVTT — 26 116
- PP0V6_S0_DDRVTT — 26 116

21 PP0V6_S3_MEM_VREFDQ_A
- PP0V6_S3_MEM_VREFDQ_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

109 21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 22 23

21 PP0V6_S3_MEM_VREFDQ_B
- PP0V6_S3_MEM_VREFDQ_B — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

109 21 PP0V6_S3_MEM_VREFCA_A
- PP0V6_S3_MEM_VREFCA_A — MAKE_BASE=TRUE, VOLTAGE=0.6V — 24 25

1V8 Rails

117 72 PP1V8_SUS
- PP1V8_SUS — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_SUS — 74
- PP1V8_SUS — 74
- PP1V8_SUS — 15 16 17

74 PP1V8_S4
- PP1V8_S4 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S4 — 38 42
- PP1V8_S4 — 20

74 PP1V8_S3
- PP1V8_S3 — MIN_LINE_WIDTH=0.2000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3 — 53
- PP1V8_S3 — 70

53 PP1V8_S3_MEM
- PP1V8_S3_MEM — MIN_LINE_WIDTH=0.6000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE
- PP1V8_S3_MEM — 22 23 24 25 116

74 PP1V8_S0
- PP1V8_S0 — MIN_LINE_WIDTH=0.5000, MIN_NECK_WIDTH=0.1200, VOLTAGE=1.8V, MAKE_BASE=TRUE — 61 114
- PP1V8_S0 — 16 17
- PP1V8_S0 — 58 60 61
- PP1V8_S0 — 37 38 42
- PP1V8_S0 — 73
- PP1V8_S0 — 19
- PP1V8_S0 — 37 42
- PP1V8_S0 — 37

SYNC_MASTER=J08_MLB SYNC_DATE=08/16/2016

PAGE TITLE

Power Aliases - 1

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 120 OF 145
SHEET 109 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PAGE TITLE
Power Aliases - 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 121 OF 145
SHEET 110 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

SIGNAL ALIAS

NC ALIASES 2

111 12	NC_CLKOUT_PCIE_1_N	NC_CLKOUT_PCIE_1_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_1_P	NC_CLKOUT_PCIE_1_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_2_N	NC_CLKOUT_PCIE_2_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_2_P	NC_CLKOUT_PCIE_2_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_6_N	NC_CLKOUT_PCIE_6_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_6_P	NC_CLKOUT_PCIE_6_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_8_N	NC_CLKOUT_PCIE_8_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_8_P	NC_CLKOUT_PCIE_8_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_9_N	NC_CLKOUT_PCIE_9_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_9_P	NC_CLKOUT_PCIE_9_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_10_N	NC_CLKOUT_PCIE_10_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_10_P	NC_CLKOUT_PCIE_10_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_11_N	NC_CLKOUT_PCIE_11_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_11_P	NC_CLKOUT_PCIE_11_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_12_N	NC_CLKOUT_PCIE_12_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_12_P	NC_CLKOUT_PCIE_12_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_14_N	NC_CLKOUT_PCIE_14_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_14_P	NC_CLKOUT_PCIE_14_P	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_15_N	NC_CLKOUT_PCIE_15_N	12 111	MAKE_BASE=TRUE
111 12	NC_CLKOUT_PCIE_15_P	NC_CLKOUT_PCIE_15_P	12 111	MAKE_BASE=TRUE

15	NC_TP_PCH_GPP_G1	NC_TP_PCH_GPP_G1	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G2	NC_TP_PCH_GPP_G2	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G3	NC_TP_PCH_GPP_G3	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G4	NC_TP_PCH_GPP_G4	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G5	NC_TP_PCH_GPP_G5	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G6	NC_TP_PCH_GPP_G6	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G7	NC_TP_PCH_GPP_G7	15	MAKE_BASE=TRUE
15	NC_TP_PCH_GPP_G8	NC_TP_PCH_GPP_G8	15	MAKE_BASE=TRUE

14	NC_PCH_GPP_F15	NC_PCH_GPP_F15	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F16	NC_PCH_GPP_F16	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F17	NC_PCH_GPP_F17	14	MAKE_BASE=TRUE
14	NC_PCH_GPP_F18	NC_PCH_GPP_F18	14	MAKE_BASE=TRUE

GPU PEG Lanes

113 91	IN PEG_GPU_D2R_P<7..0>	=PEG_D2R_P<7..0>	OUT 5	MAKE_BASE=TRUE
113 91	IN PEG_GPU_D2R_N<7..0>	=PEG_D2R_N<7..0>	OUT 5	MAKE_BASE=TRUE
113 91	OUT PEG_GPU_R2D_C_P<7..0>	=PEG_R2D_C_P<7..0>	IN 5	MAKE_BASE=TRUE
113 91	OUT PEG_GPU_R2D_C_N<7..0>	=PEG_R2D_C_N<7..0>	IN 5	MAKE_BASE=TRUE

Thunderbolt Signals Through PEG

113 29	IN PCIE_TBT_X_D2R_P<3..0>	=PEG_D2R_P<11..8>	OUT 5	MAKE_BASE=TRUE
113 29	IN PCIE_TBT_X_D2R_N<3..0>	=PEG_D2R_N<11..8>	OUT 5	MAKE_BASE=TRUE
113 29	OUT PCIE_TBT_X_R2D_C_P<3..0>	=PEG_R2D_C_P<11..8>	IN 5	MAKE_BASE=TRUE
113 29	OUT PCIE_TBT_X_R2D_C_N<3..0>	=PEG_R2D_C_N<11..8>	IN 5	MAKE_BASE=TRUE
113 103	IN PCIE_TBT_T_D2R_P<3..0>	=PEG_D2R_P<15..12>	OUT 5	MAKE_BASE=TRUE
113 103	IN PCIE_TBT_T_D2R_N<3..0>	=PEG_D2R_N<15..12>	OUT 5	MAKE_BASE=TRUE
113 103	OUT PCIE_TBT_T_R2D_C_P<3..0>	=PEG_R2D_C_P<15..12>	IN 5	MAKE_BASE=TRUE
113 103	OUT PCIE_TBT_T_R2D_C_N<3..0>	=PEG_R2D_C_N<15..12>	IN 5	MAKE_BASE=TRUE

GPU ALIAS

12	EG_CLKREQ_OUT_L	EG_CLKREQ_OUT_L	98	MAKE_BASE=TRUE
12	EG_PEG_CLK100M_N	EG_PEG_CLK100M_N	91	MAKE_BASE=TRUE
12	EG_PEG_CLK100M_P	EG_PEG_CLK100M_P	91	MAKE_BASE=TRUE
89	EG_RESET_L	EG_RESET_L	91 99	MAKE_BASE=TRUE

CPU Display Aliases

	eDP conn	DPMUX		
114 76	EDP_INT_ML_P<3..0>	EDP_INT_ML_P<3..0>	89	MAKE_BASE=TRUE
114 76	EDP_INT_ML_N<3..0>	EDP_INT_ML_N<3..0>	89	MAKE_BASE=TRUE
113 76	EDP_AUXCH_C_P	EDP_AUXCH_C_P	89	MAKE_BASE=TRUE
113 76	EDP_AUXCH_C_N	EDP_AUXCH_C_N	89	MAKE_BASE=TRUE

	NC_DDI1_ML_C_P<3..0>	NC_DDI1_ML_C_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI1_ML_C_N<3..0>	NC_DDI1_ML_C_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI1_AUXCH_C_P	NC_DDI1_AUXCH_C_P	5	MAKE_BASE=TRUE
	NC_DDI1_AUXCH_C_N	NC_DDI1_AUXCH_C_N	5	MAKE_BASE=TRUE
	NC_DDI2_ML_C_P<3..0>	NC_DDI2_ML_C_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI2_ML_C_N<3..0>	NC_DDI2_ML_C_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI2_AUXCH_C_P	NC_DDI2_AUXCH_C_P	5	MAKE_BASE=TRUE
	NC_DDI2_AUXCH_C_N	NC_DDI2_AUXCH_C_N	5	MAKE_BASE=TRUE
	NC_DDI3_ML_P<3..0>	NC_DDI3_ML_P<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI3_ML_N<3..0>	NC_DDI3_ML_N<3..0>	5	MAKE_BASE=TRUE NO_TEST=1
	NC_DDI3_AUXCH_P	NC_DDI3_AUXCH_P	5	MAKE_BASE=TRUE
	NC_DDI3_AUXCH_N	NC_DDI3_AUXCH_N	5	MAKE_BASE=TRUE

89	DPMUX_UC_RX	DPMUX_UC_RX	89	MAKE_BASE=TRUE
89	DPMUX_UC_TX	DPMUX_UC_TX	89	MAKE_BASE=TRUE
15	NC_EDP_IG_BKLT_PWM	NC_EDP_IG_BKLT_PWM		MAKE_BASE=TRUE

EPD PANEL

75	I2C_BKLT_SCL	I2C_BKLT_SCL	76 114	MAKE_BASE TRUE
75	I2C_BKLT_SDA	I2C_BKLT_SDA	76 114	MAKE_BASE TRUE

UNUSED SIGNALS

12	NC_PCH_SLP_WLAN_L	NC_PCH_SLP_WLAN_L		MAKE_BASE=TRUE
13	NC_SPI_CS1_L	NC_SPI_CS1_L		MAKE_BASE=TRUE
13	NC_SPI_CS2_L	NC_SPI_CS2_L		MAKE_BASE=TRUE

SYNC_MASTER=X363_SAMXOC SYNC_DATE=01/13/2016

PAGE TITLE

Signal Aliases

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 122 OF 145

SHEET 111 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

LPDDR3 COMMAND/ADDRESS

Memory Bit/Byte Swizzle

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_A_DQ<0>	MEM_A_DQ<0>
MEM_A_DQ<1>	MEM_A_DQ<1>
MEM_A_DQ<2>	MEM_A_DQ<2>
MEM_A_DQ<3>	MEM_A_DQ<3>
MEM_A_DQ<4>	MEM_A_DQ<4>
MEM_A_DQ<5>	MEM_A_DQ<5>
MEM_A_DQ<6>	MEM_A_DQ<6>
MEM_A_DQ<7>	MEM_A_DQ<7>
MEM_A_DQ<8>	MEM_A_DQ<8>
MEM_A_DQ<9>	MEM_A_DQ<9>
MEM_A_DQ<10>	MEM_A_DQ<10>
MEM_A_DQ<11>	MEM_A_DQ<11>
MEM_A_DQ<12>	MEM_A_DQ<12>
MEM_A_DQ<13>	MEM_A_DQ<13>
MEM_A_DQ<14>	MEM_A_DQ<14>
MEM_A_DQ<15>	MEM_A_DQ<15>
MEM_A_DQ<16>	MEM_A_DQ<16>
MEM_A_DQ<17>	MEM_A_DQ<17>
MEM_A_DQ<18>	MEM_A_DQ<18>
MEM_A_DQ<19>	MEM_A_DQ<19>
MEM_A_DQ<20>	MEM_A_DQ<20>
MEM_A_DQ<21>	MEM_A_DQ<21>
MEM_A_DQ<22>	MEM_A_DQ<22>
MEM_A_DQ<23>	MEM_A_DQ<23>
MEM_A_DQ<24>	MEM_A_DQ<24>
MEM_A_DQ<25>	MEM_A_DQ<25>
MEM_A_DQ<26>	MEM_A_DQ<26>
MEM_A_DQ<27>	MEM_A_DQ<27>
MEM_A_DQ<28>	MEM_A_DQ<28>
MEM_A_DQ<29>	MEM_A_DQ<29>
MEM_A_DQ<30>	MEM_A_DQ<30>
MEM_A_DQ<31>	MEM_A_DQ<31>
MEM_A_DQ<32>	MEM_A_DQ<32>
MEM_A_DQ<33>	MEM_A_DQ<33>
MEM_A_DQ<34>	MEM_A_DQ<34>
MEM_A_DQ<35>	MEM_A_DQ<35>
MEM_A_DQ<36>	MEM_A_DQ<36>
MEM_A_DQ<37>	MEM_A_DQ<37>
MEM_A_DQ<38>	MEM_A_DQ<38>
MEM_A_DQ<39>	MEM_A_DQ<39>
MEM_A_DQ<40>	MEM_A_DQ<40>
MEM_A_DQ<41>	MEM_A_DQ<41>
MEM_A_DQ<42>	MEM_A_DQ<42>
MEM_A_DQ<43>	MEM_A_DQ<43>
MEM_A_DQ<44>	MEM_A_DQ<44>
MEM_A_DQ<45>	MEM_A_DQ<45>
MEM_A_DQ<46>	MEM_A_DQ<46>
MEM_A_DQ<47>	MEM_A_DQ<47>
MEM_A_DQ<48>	MEM_A_DQ<48>
MEM_A_DQ<49>	MEM_A_DQ<49>
MEM_A_DQ<50>	MEM_A_DQ<50>
MEM_A_DQ<51>	MEM_A_DQ<51>
MEM_A_DQ<52>	MEM_A_DQ<52>
MEM_A_DQ<53>	MEM_A_DQ<53>
MEM_A_DQ<54>	MEM_A_DQ<54>
MEM_A_DQ<55>	MEM_A_DQ<55>
MEM_A_DQ<56>	MEM_A_DQ<56>
MEM_A_DQ<57>	MEM_A_DQ<57>
MEM_A_DQ<58>	MEM_A_DQ<58>
MEM_A_DQ<59>	MEM_A_DQ<59>
MEM_A_DQ<60>	MEM_A_DQ<60>
MEM_A_DQ<61>	MEM_A_DQ<61>
MEM_A_DQ<62>	MEM_A_DQ<62>
MEM_A_DQ<63>	MEM_A_DQ<63>

BDW-H LPDDR3 NET	BIT SWIZZLE
MAKE_BASE=TRUE	
MEM_B_DQ<0>	MEM_B_DQ<0>
MEM_B_DQ<1>	MEM_B_DQ<1>
MEM_B_DQ<2>	MEM_B_DQ<2>
MEM_B_DQ<3>	MEM_B_DQ<3>
MEM_B_DQ<4>	MEM_B_DQ<4>
MEM_B_DQ<5>	MEM_B_DQ<5>
MEM_B_DQ<6>	MEM_B_DQ<6>
MEM_B_DQ<7>	MEM_B_DQ<7>
MEM_B_DQ<8>	MEM_B_DQ<8>
MEM_B_DQ<9>	MEM_B_DQ<9>
MEM_B_DQ<10>	MEM_B_DQ<10>
MEM_B_DQ<11>	MEM_B_DQ<11>
MEM_B_DQ<12>	MEM_B_DQ<12>
MEM_B_DQ<13>	MEM_B_DQ<13>
MEM_B_DQ<14>	MEM_B_DQ<14>
MEM_B_DQ<15>	MEM_B_DQ<15>
MEM_B_DQ<16>	MEM_B_DQ<16>
MEM_B_DQ<17>	MEM_B_DQ<17>
MEM_B_DQ<18>	MEM_B_DQ<18>
MEM_B_DQ<19>	MEM_B_DQ<19>
MEM_B_DQ<20>	MEM_B_DQ<20>
MEM_B_DQ<21>	MEM_B_DQ<21>
MEM_B_DQ<22>	MEM_B_DQ<22>
MEM_B_DQ<23>	MEM_B_DQ<23>
MEM_B_DQ<24>	MEM_B_DQ<24>
MEM_B_DQ<25>	MEM_B_DQ<25>
MEM_B_DQ<26>	MEM_B_DQ<26>
MEM_B_DQ<27>	MEM_B_DQ<27>
MEM_B_DQ<28>	MEM_B_DQ<28>
MEM_B_DQ<29>	MEM_B_DQ<29>
MEM_B_DQ<30>	MEM_B_DQ<30>
MEM_B_DQ<31>	MEM_B_DQ<31>
MEM_B_DQ<32>	MEM_B_DQ<32>
MEM_B_DQ<33>	MEM_B_DQ<33>
MEM_B_DQ<34>	MEM_B_DQ<34>
MEM_B_DQ<35>	MEM_B_DQ<35>
MEM_B_DQ<36>	MEM_B_DQ<36>
MEM_B_DQ<37>	MEM_B_DQ<37>
MEM_B_DQ<38>	MEM_B_DQ<38>
MEM_B_DQ<39>	MEM_B_DQ<39>
MEM_B_DQ<40>	MEM_B_DQ<40>
MEM_B_DQ<41>	MEM_B_DQ<41>
MEM_B_DQ<42>	MEM_B_DQ<42>
MEM_B_DQ<43>	MEM_B_DQ<43>
MEM_B_DQ<44>	MEM_B_DQ<44>
MEM_B_DQ<45>	MEM_B_DQ<45>
MEM_B_DQ<46>	MEM_B_DQ<46>
MEM_B_DQ<47>	MEM_B_DQ<47>
MEM_B_DQ<48>	MEM_B_DQ<48>
MEM_B_DQ<49>	MEM_B_DQ<49>
MEM_B_DQ<50>	MEM_B_DQ<50>
MEM_B_DQ<51>	MEM_B_DQ<51>
MEM_B_DQ<52>	MEM_B_DQ<52>
MEM_B_DQ<53>	MEM_B_DQ<53>
MEM_B_DQ<54>	MEM_B_DQ<54>
MEM_B_DQ<55>	MEM_B_DQ<55>
MEM_B_DQ<56>	MEM_B_DQ<56>
MEM_B_DQ<57>	MEM_B_DQ<57>
MEM_B_DQ<58>	MEM_B_DQ<58>
MEM_B_DQ<59>	MEM_B_DQ<59>
MEM_B_DQ<60>	MEM_B_DQ<60>
MEM_B_DQ<61>	MEM_B_DQ<61>
MEM_B_DQ<62>	MEM_B_DQ<62>
MEM_B_DQ<63>	MEM_B_DQ<63>

MAKE_BASE		
TRUE	MEM_A_DQS_P<0>	MEM_A_DQS_P<0>
TRUE	MEM_A_DQS_N<0>	MEM_A_DQS_N<0>
TRUE	MEM_A_DQS_P<1>	MEM_A_DQS_P<1>
TRUE	MEM_A_DQS_N<1>	MEM_A_DQS_N<1>
TRUE	MEM_A_DQS_P<2>	MEM_A_DQS_P<2>
TRUE	MEM_A_DQS_N<2>	MEM_A_DQS_N<2>
TRUE	MEM_A_DQS_P<3>	MEM_A_DQS_P<3>
TRUE	MEM_A_DQS_N<3>	MEM_A_DQS_N<3>
TRUE	MEM_A_DQS_P<4>	MEM_A_DQS_P<4>
TRUE	MEM_A_DQS_N<4>	MEM_A_DQS_N<4>
TRUE	MEM_A_DQS_P<5>	MEM_A_DQS_P<5>
TRUE	MEM_A_DQS_N<5>	MEM_A_DQS_N<5>
TRUE	MEM_A_DQS_P<6>	MEM_A_DQS_P<6>
TRUE	MEM_A_DQS_N<6>	MEM_A_DQS_N<6>
TRUE	MEM_A_DQS_P<7>	MEM_A_DQS_P<7>
TRUE	MEM_A_DQS_N<7>	MEM_A_DQS_N<7>

MAKE_BASE		
TRUE	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>
TRUE	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>
TRUE	MEM_B_DQS_P<1>	MEM_B_DQS_P<1>
TRUE	MEM_B_DQS_N<1>	MEM_B_DQS_N<1>
TRUE	MEM_B_DQS_P<2>	MEM_B_DQS_P<2>
TRUE	MEM_B_DQS_N<2>	MEM_B_DQS_N<2>
TRUE	MEM_B_DQS_P<3>	MEM_B_DQS_P<3>
TRUE	MEM_B_DQS_N<3>	MEM_B_DQS_N<3>
TRUE	MEM_B_DQS_P<4>	MEM_B_DQS_P<4>
TRUE	MEM_B_DQS_N<4>	MEM_B_DQS_N<4>
TRUE	MEM_B_DQS_P<5>	MEM_B_DQS_P<5>
TRUE	MEM_B_DQS_N<5>	MEM_B_DQS_N<5>
TRUE	MEM_B_DQS_P<6>	MEM_B_DQS_P<6>
TRUE	MEM_B_DQS_N<6>	MEM_B_DQS_N<6>
TRUE	MEM_B_DQS_P<7>	MEM_B_DQS_P<7>
TRUE	MEM_B_DQS_N<7>	MEM_B_DQS_N<7>

SYNC_MASTER=J80_MLB SYNC_DATE=11/06/2015

PAGE TITLE

Memory Bit/Byte Swizzle

Apple Inc.

DRAWING NUMBER 051-00647

SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 123 OF 145

SHEET 112 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

High Speed NO_TEST

DMI

13	5	IN	DMI_S2N_P<3..0>	NO_TEST=1
13	5	IN	DMI_S2N_N<3..0>	NO_TEST=1
13	5	IN	DMI_N2S_P<3..0>	NO_TEST=1
13	5	IN	DMI_N2S_N<3..0>	NO_TEST=1

DP - CPU/ACE

99	27	IN	DP_X_SNK0_ML_C_N<3..0>	NO_TEST=1
99	27	IN	DP_X_SNK0_ML_C_P<3..0>	NO_TEST=1
	27	IN	DP_X_SNK0_ML_N<3..0>	NO_TEST=1
	27	IN	DP_X_SNK0_ML_P<3..0>	NO_TEST=1
99	27	IN	DP_X_SNK1_ML_C_N<3..0>	NO_TEST=1
99	27	IN	DP_X_SNK1_ML_C_P<3..0>	NO_TEST=1
	27	IN	DP_X_SNK1_ML_N<3..0>	NO_TEST=1
	27	IN	DP_X_SNK1_ML_P<3..0>	NO_TEST=1
101	99	IN	DP_T_SNK0_ML_C_N<3..0>	NO_TEST=1
101	99	IN	DP_T_SNK0_ML_C_P<3..0>	NO_TEST=1
	101	IN	DP_T_SNK0_ML_N<3..0>	NO_TEST=1
	101	IN	DP_T_SNK0_ML_P<3..0>	NO_TEST=1
101	99	IN	DP_T_SNK1_ML_C_N<3..0>	NO_TEST=1
101	99	IN	DP_T_SNK1_ML_C_P<3..0>	NO_TEST=1
	101	IN	DP_T_SNK1_ML_N<3..0>	NO_TEST=1
	101	IN	DP_T_SNK1_ML_P<3..0>	NO_TEST=1
99	27	IN	DP_X_SNK0_AUXCH_C_P	NO_TEST=1
99	27	IN	DP_X_SNK0_AUXCH_C_N	NO_TEST=1
101	99	IN	DP_T_SNK0_AUXCH_C_P	NO_TEST=1
101	99	IN	DP_T_SNK0_AUXCH_C_N	NO_TEST=1
	27	IN	DP_X_SNK0_AUXCH_P	NO_TEST=1
	27	IN	DP_X_SNK0_AUXCH_N	NO_TEST=1
	101	IN	DP_T_SNK0_AUXCH_P	NO_TEST=1
	101	IN	DP_T_SNK0_AUXCH_N	NO_TEST=1
99	27	IN	DP_X_SNK1_AUXCH_C_P	NO_TEST=1
99	27	IN	DP_X_SNK1_AUXCH_C_N	NO_TEST=1
101	99	IN	DP_T_SNK1_AUXCH_C_P	NO_TEST=1
101	99	IN	DP_T_SNK1_AUXCH_C_N	NO_TEST=1
	27	IN	DP_X_SNK1_AUXCH_P	NO_TEST=1
	27	IN	DP_X_SNK1_AUXCH_N	NO_TEST=1
	101	IN	DP_T_SNK1_AUXCH_P	NO_TEST=1
	101	IN	DP_T_SNK1_AUXCH_N	NO_TEST=1

CPU/EDP

111	76	IN	EDP_AUXCH_C_N	
111	76	IN	EDP_AUXCH_C_P	

PCH/AR

35	14	IN	PCIE_AP_D2R_P	NO_TEST=1
35	14	IN	PCIE_AP_D2R_N	NO_TEST=1
	35	IN	PCIE_AP_R2D_P	NO_TEST=1
	35	IN	PCIE_AP_R2D_N	NO_TEST=1
35	14	IN	PCIE_AP_R2D_C_P	NO_TEST=1
35	14	IN	PCIE_AP_R2D_C_N	NO_TEST=1

PCH/SSD

87	77	14	IN	PCIE_SSD_D2R_N<3..0>	NO_TEST=1
87	77	14	IN	PCIE_SSD_D2R_P<3..0>	NO_TEST=1
113	77		IN	PCIE_SSD_R2D_N<3..0>	NO_TEST=1
113	77		IN	PCIE_SSD_R2D_P<3..0>	NO_TEST=1
	77		IN	PCIE_SSD_D2R_C_N<3..0>	NO_TEST=1
113	87	77	14	IN	PCIE_SSD_R2D_C_N<3..0>	NO_TEST=1
	14		IN	PCIE_SSD_D2R_N<0>	NO_TEST=1
	14		IN	PCIE_SSD_D2R_P<0>	NO_TEST=1
	77		IN	PCIE_SSD_D2R_C_P<3..0>	NO_TEST=1
113	87	77	14	IN	PCIE_SSD_R2D_C_N<3..0>	NO_TEST=1
	87	77		IN	PCIE_SSD_D2R_LB_P<0>	
	87	77		IN	PCIE_SSD_R2D_LB_N<0>	
	14		IN	PCIE_SSD_D2R_P<3>	NO_TEST=1
	87	77		IN	PCIE_SSD_D2R_LB_N<0>	
	14		IN	PCIE_SSD_D2R_N<3>	NO_TEST=1
	87	77		IN	PCIE_SSD_R2D_LB_P<0>	

USB-C X

32	27	IN	USBC_XB_D2R_N<2..1>	NO_TEST=1
32	27	IN	USBC_XB_D2R_P<2..1>	NO_TEST=1
32	27	IN	USBC_XA_D2R_P<2..1>	NO_TEST=1
32	27	IN	USBC_XB_R2D_C_P<2..1>	NO_TEST=1
30	27	IN	DP_XA_AUXCH_P	NO_TEST=1
32	27	IN	USBC_XA_D2R_N<2..1>	NO_TEST=1
32	27	IN	USBC_XB_R2D_C_N<2..1>	NO_TEST=1
32	27	IN	USBC_XA_R2D_C_P<2..1>	NO_TEST=1
31	27	IN	DP_XB_AUXCH_P	NO_TEST=1
32	27	IN	USBC_XA_R2D_C_N<2..1>	NO_TEST=1
31	27	IN	DP_XB_AUXCH_N	NO_TEST=1
30	27	IN	DP_XA_AUXCH_N	NO_TEST=1
	27	IN	DP_XA_AUXCH_C_N	NO_TEST=1
	27	IN	DP_XA_AUXCH_C_P	NO_TEST=1
	27	IN	DP_XB_AUXCH_C_P	NO_TEST=1
	27	IN	DP_XB_AUXCH_C_N	NO_TEST=1

PEG

111	91	IN	PEG_GPU_D2R_N<7..0>	NO_TEST=1
111	91	IN	PEG_GPU_D2R_P<7..0>	NO_TEST=1
111	91	IN	PEG_GPU_R2D_C_N<7..0>	NO_TEST=1
111	91	IN	PEG_GPU_R2D_C_P<7..0>	NO_TEST=1
111	29	IN	PCIE_TBT_X_D2R_P<3..0>	NO_TEST=1
111	29	IN	PCIE_TBT_X_D2R_N<3..0>	NO_TEST=1
111	29	IN	PCIE_TBT_X_R2D_C_P<3..0>	NO_TEST=1
111	29	IN	PCIE_TBT_X_R2D_C_N<3..0>	NO_TEST=1
111	103	IN	PCIE_TBT_T_D2R_P<3..0>	NO_TEST=1
111	103	IN	PCIE_TBT_T_D2R_N<3..0>	NO_TEST=1
103	101	IN	PCIE_TBT_T_D2R_C_P<3..0>	NO_TEST=1
103	101	IN	PCIE_TBT_T_D2R_C_N<3..0>	NO_TEST=1
29	27	IN	PCIE_TBT_X_D2R_C_P<3..0>	NO_TEST=1
29	27	IN	PCIE_TBT_X_D2R_C_N<3..0>	NO_TEST=1
29	27	IN	PCIE_TBT_X_R2D_P<3..0>	NO_TEST=1
29	27	IN	PCIE_TBT_X_R2D_N<3..0>	NO_TEST=1
103	101	IN	PCIE_TBT_T_R2D_P<3..0>	NO_TEST=1
103	101	IN	PCIE_TBT_T_R2D_N<3..0>	NO_TEST=1
111	103	IN	PCIE_TBT_T_R2D_C_P<3..0>	NO_TEST=1
111	103	IN	PCIE_TBT_T_R2D_C_N<3..0>	NO_TEST=1
	91	IN	PEG_GPU_D2R_C_N<7..0>	NO_TEST=1
	91	IN	PEG_GPU_D2R_C_P<7..0>	NO_TEST=1
	91	IN	PEG_GPU_R2D_N<7..0>	NO_TEST=1
	91	IN	PEG_GPU_R2D_P<7..0>	NO_TEST=1

PCH/DFR

38	14	IN	USB_CAMERA_DFR_N	
38	14	IN	USB_CAMERA_DFR_P	

BAFFIN FRAME BUFFER

95	93	IN	FB_A1_CS_L	NO_TEST=1
95	93	IN	FB_A0_CKE_L	NO_TEST=1
95	93	IN	FB_A1_CKE_L	NO_TEST=1
95	93	IN	FB_A0_WE_L	NO_TEST=1
95	93	IN	FB_A1_WE_L	NO_TEST=1
96	93	IN	FB_B1_CS_L	NO_TEST=1
96	93	IN	FB_B0_CKE_L	NO_TEST=1
96	93	IN	FB_B1_CKE_L	NO_TEST=1
113	96	93	IN	FB_B0_WE_L	NO_TEST=1
113	96	93	IN	FB_B0_WE_L	NO_TEST=1
96	93	IN	FB_B0_CLK_P	NO_TEST=1
96	93	IN	FB_B1_CLK_N	NO_TEST=1
96	93	IN	FB_B1_CLK_P	NO_TEST=1
96	93	IN	FB_B0_RAS_L	NO_TEST=1
96	93	IN	FB_B1_RAS_L	NO_TEST=1
96	93	IN	FB_B0_CAS_L	NO_TEST=1
96	93	IN	FB_B1_CAS_L	NO_TEST=1
96	93	IN	FB_B0_CS_L	NO_TEST=1
95	93	IN	FB_A0_DQ<31..0>	NO_TEST=1
95	93	IN	FB_A1_DQ<31..0>	NO_TEST=1
95	93	IN	FB_A0_A<8..0>	NO_TEST=1
95	93	IN	FB_A1_A<8..0>	NO_TEST=1
95	93	IN	FB_A0_WCLK_N<1..0>	NO_TEST=1
95	93	IN	FB_A0_WCLK_P<1..0>	NO_TEST=1
95	93	IN	FB_A1_WCLK_N<1..0>	NO_TEST=1
95	93	IN	FB_A1_WCLK_P<1..0>	NO_TEST=1
95	93	IN	FB_A0_EDC<3..0>	NO_TEST=1
95	93	IN	FB_A1_EDC<3..0>	NO_TEST=1
95	93	IN	FB_A0_DBI_L<3..0>	NO_TEST=1
95	93	IN	FB_A1_DBI_L<3..0>	NO_TEST=1
95	93	IN	FB_A0_ABI_L	NO_TEST=1
95	93	IN	FB_A1_ABI_L	NO_TEST=1
95	93	IN	FB_A0_CLK_N	NO_TEST=1
95	93	IN	FB_A0_CLK_P	NO_TEST=1
95	93	IN	FB_A1_CLK_N	NO_TEST=1
95	93	IN	FB_A1_CLK_P	NO_TEST=1
95	93	IN	FB_A0_RAS_L	NO_TEST=1
95	93	IN	FB_A1_RAS_L	NO_TEST=1
95	93	IN	FB_A0_CAS_L	NO_TEST=1
95	93	IN	FB_A1_CAS_L	NO_TEST=1
95	93	IN	FB_A0_CS_L	NO_TEST=1
96	93	IN	FB_B0_CLK_N	NO_TEST=1
96	93	IN	FB_B0_DQ<31..0>	NO_TEST=1
96	93	IN	FB_B1_DQ<31..0>	NO_TEST=1
96	93	IN	FB_B0_A<8..0>	NO_TEST=1
96	93	IN	FB_B1_A<8..0>	NO_TEST=1
96	93	IN	FB_B0_WCLK_N<1..0>	NO_TEST=1
96	93	IN	FB_B0_WCLK_P<1..0>	NO_TEST=1
96	93	IN	FB_B1_WCLK_N<1..0>	NO_TEST=1
96	93	IN	FB_B1_WCLK_P<1..0>	NO_TEST=1
96	93	IN	FB_B0_EDC<3..0>	NO_TEST=1
96	93	IN	FB_B1_EDC<3..0>	NO_TEST=1
96	93	IN	FB_B0_DBI_L<3..0>	NO_TEST=1
96	93	IN	FB_B1_DBI_L<3..0>	NO_TEST=1
96	93	IN	FB_B0_ABI_L	NO_TEST=1
96	93	IN	FB_B1_ABI_L	NO_TEST=1

CPU/PCH CLK

12	6	IN	CPU_CLK24M_NSSC_CLK_N	NO_TEST=1
12	6	IN	CPU_CLK24M_NSSC_CLK_P	NO_TEST=1
12	6	IN	CPU_CLK100M_PCIBCLK_N	NO_TEST=1
12	6	IN	CPU_CLK100M_PCIBCLK_P	NO_TEST=1
12	6	IN	CPU_CLK100M_BCLK_N	NO_TEST=1
12	6	IN	CPU_CLK100M_BCLK_P	NO_TEST=1
87	12	IN	PCIE_CLK100M_SSD_N	NO_TEST=1
87	12	IN	PCIE_CLK100M_SSD_P	NO_TEST=1
87	77	IN	PCIE_CLK100M_SSD_LB_N	NO_TEST=1
87	77	IN	PCIE_CLK100M_SSD_LB_P	NO_TEST=1
115	18	12	IN	NC_ITPXDP_CLK100MN	NO_TEST=1
115	18	12	IN	NC_ITPXDP_CLK100MP	NO_TEST=1
35	12	IN	PCIE_CLK100M_AP_P	NO_TEST=1
35	12	IN	PCIE_CLK100M_AP_N	NO_TEST=1

MUX

89	5	IN	DP_INT_IG_ML_N<3..0>	NO_TEST=1
89	5	IN	DP_INT_IG_ML_P<3..0>	NO_TEST=1
89	5	IN	DP_INT_IG_AUX_N	NO_TEST=1
89	5	IN	DP_INT_IG_AUX_P	NO_TEST=1
99	89	IN	DP_INT_EG_ML_N<3..0>	NO_TEST=1
99	89	IN	DP_INT_EG_ML_P<3..0>	NO_TEST=1
99	89	IN	DP_INT_EG_AUX_N	NO_TEST=1
99	89	IN	DP_INT_EG_AUX_P	NO_TEST=1

DP MUX CRYSTAL

89		IN	DPMUX_UC_XTAL	NO_TEST=1
89		IN	DPMUX_UC_EXTAL	NO_TEST=1
89		IN	DPMUX_UC_EXTAL_R	NO_TEST=1
89		IN	DPMUX_UC_XTAL_R	NO_TEST=1

XTAL

		IN	GPU_XTAL_PU_OR_CAP	NO_TEST=1
		IN	NC_PCH_CLK24M_XTALOUT	NO_TEST=1
19		IN	SYSCLK_CLK24M_X2	NO_TEST=1
19		IN	SYSCLK_CLK24M_X2_R	NO_TEST=1
19		IN	SYSCLK_CLK24M_X1	NO_TEST=1
29	27	IN	TBT_X_XTAL25M_OUT	NO_TEST=1
29		IN	TBT_X_XTAL25M_OUT_R	NO_TEST=1
29	27	IN	TBT_X_XTAL25M_IN	NO_TEST=1
103	101	IN	TBT_T_XTAL25M_OUT	NO_TEST=1
103		IN	TBT_T_XTAL25M_OUT_R	NO_TEST=1
38		IN	SOC_XTAL_24M_O	NO_TEST=1
103	101	IN	TBT_T_XTAL25M_IN	NO_TEST=1
38		IN	SOC_XTAL_24M_I	NO_TEST=1
38		IN	SOC_XTAL_24M_O_R	NO_TEST=1
77		IN	SSD_CLKIN	NO_TEST=1
77		IN	SSD_CLKOUT	NO_TEST=1
77		IN	SSD_CLKOUT_R	NO_TEST=1
99	98	IN	GPU_XTAL_OUT	NO_TEST=1
99	98	IN	GPU_XTAL_OR_CLK_IN	NO_TEST=1
	98	IN	GPU_XTAL_XTAL_OR_CLK	NO_TEST=1

MEM

26	22	7	IN	MEM_A_CAA<9..0>	NO_TEST=1
26	23	7	IN	MEM_A_CLK_P<1..0>	NO_TEST=1
26	23	7	IN	MEM_A_CLK_N<1..0>	NO_TEST=1
112		7	IN	MEM_A_DQ<63..0>	NO_TEST=1
112		7	IN	MEM_B_DQ<63..0>	NO_TEST=1
112		7	IN	MEM_A_DQS_P<7..0>	NO_TEST=1
112		7	IN	MEM_A_DQS_N<7..0>	NO_TEST=1
112		7	IN	MEM_B_DQS_P<7..0>	NO_TEST=1
112		7	IN	MEM_B_DQS_N<7..0>	NO_TEST=1
26	23	7	IN	MEM_A_CAB<9..0>	NO_TEST=1
26	24	7	IN	MEM_B_CAA<9..0>	NO_TEST=1
26	25	7	IN	MEM_B_CAB<9..0>	NO_TEST=1
26	25	24	7	IN	MEM_B_CLK_P<1..0>	NO_TEST=1
26	25	24	7	IN	MEM_B_CLK_N<1..0>	NO_TEST=1

WIFI

	36		IN	50_0_ANT	NO_TEST=1
	36		IN	50_1_ANT	NO_TEST=1
	36		IN	50_2_ANT	NO_TEST=1
	36		IN	50_0_COM	NO_TEST=1
	36		IN	50_1_COM	NO_TEST=1
	36		IN	50_2_COM	NO_TEST=1
	36		IN	50_A_0_DIPLEXER	NO_TEST=1
36	35		IN	50_A_0_MATCH	NO_TEST=1
	36		IN	50_G_0_DIPLEXER	NO_TEST=1
36	35		IN	50_G_0_MATCH	NO_TEST=1
	36		IN	50_A_1_DIPLEXER	NO_TEST=1
36	35		IN	50_A_1_MATCH	NO_TEST=1
	36		IN	50_G_1_DIPLEXER	NO_TEST=1
36	35		IN	50_G_1_MATCH	NO_TEST=1
	36		IN	50_A_2_DIPLEXER	NO_TEST=1
36	35		IN	50_A_2_MATCH	NO_TEST=1
	36		IN	50_G_2_DIPLEXER	NO_TEST=1
36	35		IN	50_G_2_MATCH	NO_TEST=1

USB-C T

106	101		IN	USBC_TA_D2R_P<2..1>	NO_TEST=1
106	101		IN	USBC_TA_D2R_N<2..1>	NO_TEST=1
106	101		IN	USBC_TA_R2D_C_P<2..1>	NO_TEST=1
106	101		IN	USBC_TA_R2D_C_N<2..1>	NO_TEST=1
104	101		IN	DP_TA_AUXCH_P	NO_TEST=1
104	101		IN	DP_TA_AUXCH_N	NO_TEST=1
	101		IN	DP_TA_AUXCH_C_P	NO_TEST=1
	101		IN	DP_TA_AUXCH_C_N	NO_TEST=1
106	101		IN	USBC_TB_D2R_P<2..1>	NO_TEST=1
106	101		IN	USBC_TB_D2R_N<2..1>	NO_TEST=1
106	101		IN	USBC_TB_R2D_C_P<2..1>	NO_TEST=1
106	101		IN	USBC_TB_R2D_C_N<2..1>	NO_TEST=1
105	101		IN	DP_TB_AUXCH_P	NO_TEST=1
105	101		IN	DP_TB_AUXCH_N	NO_TEST=1
	101		IN	DP_TB_AUXCH_C_P	NO_TEST=1
	101		IN	DP_TB_AUXCH_C_N	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQ4	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQ0	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQS_P	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQ5	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQ6	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQ7	NO_TEST=1
85	83		IN	SSD_NAND_FH_DQS_N	NO_TEST=1

NAND

85	82	IN	SSD_NAND_FA_DQ0	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ1	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ2	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ3	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ4	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ5	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ6	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQ7	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQS_N	NO_TEST=1
85	82	IN	SSD_NAND_FA_DQS_P	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ0	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ1	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ2	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ3	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ4	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ5	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ6	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQ7	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQS_N	NO_TEST=1
85	82	IN	SSD_NAND_FB_DQS_P	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ0	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ1	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ2	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ3	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ4	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ5	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ6	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQ7	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQS_N	NO_TEST=1
85	82	IN	SSD_NAND_FC_DQS_P	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ0	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ1	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ2	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ3	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ4	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ5	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ6	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQ7	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQS_N	NO_TEST=1
85	82	IN	SSD_NAND_FD_DQS_P	NO_TEST=1
	85	83	IN	SSD_NAND_FE_DQ0	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ1	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ2	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ3	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ4	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ5	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ6	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQ7	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQS_N	NO_TEST=1
85	83	IN	SSD_NAND_FE_DQS_P	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ0	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ1	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ2	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ3	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ4	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ5	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ6	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQ7	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQS_N	NO_TEST=1
85	83	IN	SSD_NAND_FF_DQS_P	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ0	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ2	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ3	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ4	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ5	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ6	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQ7	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQS_N	NO_TEST=1
85	83	IN	SSD_NAND_FG_DQS_P	NO_TEST=1
85	83	IN	SSD_NAND_FH_DQ1	NO_TEST=1
85	83	IN	SSD_NAND_FH_DQ2	NO_TEST=1
85	83	IN	SSD_NAND_FH_DQ3	NO_TEST=1

SYNC_MASTER=X363_SAKKOC SYNC_DATE=04/14/2016

PAGE TITLE

ICT & FCT 1

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 124 OF 145

SHEET 113 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

MESA CONNECTOR

45	IN	PP3V0_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MISO_CONN	FUNC_TEST=TRUE
45	IN	MESA_SNSR_INT_CONN	FUNC_TEST=TRUE
45	IN	MESA_BOOST_EN_CONN	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SDA	FUNC_TEST=TRUE
45 37	IN	MESA_I2C_SCL	FUNC_TEST=TRUE
45	IN	PP1V8_MESA_CONN	FUNC_TEST=TRUE
45	IN	MESA_SPI_MOSI_CONN	FUNC_TEST=TRUE
45	IN	MENU_KEY_L	FUNC_TEST=TRUE
45	IN	MESA_SPI_CLK_CONN	FUNC_TEST=TRUE
45	IN	PP16V0_MESA_CONN	FUNC_TEST=TRUE
		GND	

SPI ROM

114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO0_MOSI	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO1_MISO	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO2_WP_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_IO3_HOLD_L	FUNC_TEST=TRUE
76 64 57 48 29 114	IN	SMC_RESET_L	FUNC_TEST=TRUE
57	IN	SPI_ALT_CLK	FUNC_TEST=TRUE
57	IN	SPI_ALT_CS_L	FUNC_TEST=TRUE
57 15	IN	SPIROM_USE_MLB	FUNC_TEST=TRUE
57 47 46	IN	SMC_TMS	FUNC_TEST=TRUE
57 47 46	IN	SMC_TCK	FUNC_TEST=TRUE
		GND	

AUDIO AMP

61	IN	SPKRCONN_TR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_TR_OUT_NEG	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_POS	FUNC_TEST=TRUE
61	IN	SPKRCONN_WR_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_TL_OUT_NEG	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_POS	FUNC_TEST=TRUE
60	IN	SPKRCONN_WL_OUT_NEG	FUNC_TEST=TRUE
61 58	IN	SPKR_ID0	FUNC_TEST=TRUE
		GND	FUNC_TEST=

DFR Touch Conn

42	IN	DFR_TOUCH_LID	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_GPIO2	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_SPI_CS_L	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MOSI_R	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFR_TOUCH_ROM_I2C_SDA	FUNC_TEST=TRUE
42 37	IN	DFR_TOUCH_RESET_L	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
110	IN	PP5V_S0_T139	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_PANEL_DETECT	FUNC_TEST=TRUE
114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_MISO_R	FUNC_TEST=TRUE
42	IN	DFR_TOUCH_SPI_CLK_R	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_INT_L	FUNC_TEST=TRUE
42 38	IN	DFR_CLKIN_RESET_L	FUNC_TEST=TRUE
42 38	IN	DFR_TOUCH_ROM_WC	FUNC_TEST=TRUE
		GND	X4

DFR Disp Conn

114 42 38	IN	DFR_DISP_VSYNC	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_TE	FUNC_TEST=TRUE
42 38	IN	DFR_DISP_INT	FUNC_TEST=TRUE
42	IN	DFR_DISP_RESET_L	FUNC_TEST=TRUE
42	IN	PP3V3_S0SW_DFR	X3 FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_P	FUNC_TEST=TRUE
42 38	IN	MIPID_CLK_N	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_P	FUNC_TEST=TRUE
42 38	IN	MIPID_DATA_N	FUNC_TEST=TRUE
114 42 37	IN	PP1V8_S0SW_DFR	X2 FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SCL	FUNC_TEST=TRUE
42 38 37	IN	DFRDRV_I2C_SDA	FUNC_TEST=TRUE
		GND	X6

KBD CONNECTOR

43	IN	GND_FAN	X2 FUNC_TEST=TRUE
43	IN	PP5V_S0_FAN_CONN	X2 FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_LT_PWM	FUNC_TEST=TRUE
110	IN	PP5V_S0_KBD	X2 FUNC_TEST=TRUE
114 109	IN	PP3V3_G3H	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
110 103 29	IN	PP3V3_S4	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
43	IN	KBD_BLC_XBLANK	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_TACH	FUNC_TEST=TRUE
115 56 43	IN	FAN_RT_PWM	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
		GND	X5

TPAD CONNECTOR

114 43	IN	KBD_I2C_SCL	FUNC_TEST=TRUE
114 43	IN	KBD_I2C_SDA	FUNC_TEST=TRUE
114 43	IN	KBD_INT_L	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_3_SCL	FUNC_TEST=TRUE
110	IN	PP3V3_S4_TPAD	FUNC_TEST=TRUE
43	IN	PP5V_S4_TPAD_CONN	FUNC_TEST=TRUE
43	IN	ACT_GND	X4 FUNC_TEST=TRUE
43	IN	PPVIN_S4_TPAD_FUSE	X4 FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_CLK	FUNC_TEST=TRUE
43	IN	TPAD_SPI_IF_EN_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MISO	FUNC_TEST=TRUE
43	IN	TPAD_SPI_CS_L_CONN	FUNC_TEST=TRUE
43 13	IN	TPAD_SPI_MOSI	FUNC_TEST=TRUE
43	IN	TPAD_SPI_INT_L_CONN	FUNC_TEST=TRUE
48 46	IN	SMC_ACTUATOR_DISABLE_L	FUNC_TEST=TRUE
48 47 46	IN	SMC_PME_S4_WAKE_L	FUNC_TEST=TRUE
48 47 43 42	IN	SMC_LID	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSLAT	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSCK	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSOUT	FUNC_TEST=TRUE
46 43	IN	SMC_VIBE_L	FUNC_TEST=TRUE
114 43	IN	KBD_BLC_GSSIN	FUNC_TEST=TRUE
		GND	X3

eDP

116 76 75	IN	PPVOUT_S0_LCDBKLT	FUNC_TEST=TRUE
76	IN	PP3V3_S0SW_LCD	X2 FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_N	FUNC_TEST=TRUE
76	IN	EDP_AUXCH_C_P	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<0>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<1>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<2>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_N<3>	FUNC_TEST=TRUE
111 76	IN	EDP_INT_ML_P<3>	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_N	FUNC_TEST=TRUE
38	IN	MIPIC_CLK_P	FUNC_TEST=TRUE
76	IN	PP5V_S0SW_LCD	FUNC_TEST=TRUE
76 38	IN	PP5V_S0_ALSCAM_F	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SDA	FUNC_TEST=TRUE
76 42	IN	I2C_ALS_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SCL	FUNC_TEST=TRUE
76 38 37	IN	I2C_CAM_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SDA	FUNC_TEST=TRUE
111 76	IN	I2C_BKLT_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 48	IN	BKLT_PWM_TCON2MLB	FUNC_TEST=TRUE
76 20	IN	BKLT_PWM_MLB2TCON	FUNC_TEST=TRUE
89 76	IN	LCD_FSS	FUNC_TEST=TRUE
76 15	IN	LCD_IRQ_L	FUNC_TEST=TRUE
76	IN	BUF_EDP_PANEL_PWR_EN	FUNC_TEST=TRUE
89 76	IN	DP_INT_HPD	FUNC_TEST=TRUE
		GND	X3
76 49	IN	SMBUS_SMC_0_S0_SCL	FUNC_TEST=TRUE
76 49	IN	SMBUS_SMC_0_S0_SDA	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_P	FUNC_TEST=TRUE
38	IN	MIPIC_DATA_N	FUNC_TEST=TRUE

AUDIO JACK

62	IN	AUD_CONN_HP_LEFT	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_RIGHT	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_L	FUNC_TEST=TRUE
62	IN	AUD_CONN_HP_SENSE_R	FUNC_TEST=TRUE
62	IN	AUD_CONN_TIP_SENSE	FUNC_TEST=TRUE
62	IN	AUD_CONN_SLEEVE_XW	FUNC_TEST=TRUE
62	IN	AUD_CONN_RING2_XW	FUNC_TEST=TRUE
		GND	X2

BATTERY TUBA

64 63	IN	PPVBAT_G3H_CONN	X7 FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SCL	FUNC_TEST=TRUE
49 46	IN	SMBUS_SMC_5_G3_SDA	FUNC_TEST=TRUE
63	IN	TP_BMON_IOUT	FUNC_TEST=TRUE
64 50	IN	CHGR_AMON	FUNC_TEST=TRUE
64 50	IN	CHGR_BMON	FUNC_TEST=TRUE
63	IN	SYS_DETECT_L	FUNC_TEST=TRUE
		GND	X5
114 48 43	IN	SMC_LSOC_RST_L	FUNC_TEST=TRUE
64	IN	TBA_COMP	FUNC_TEST=TRUE
64	IN	TBA_VDDA	FUNC_TEST=TRUE
64	IN	TBA_LX1	FUNC_TEST=TRUE
64	IN	TBA_LX2	FUNC_TEST=TRUE
		GND	X2
64	IN	PPVBAT_G3H_CHGR_REG	X5 FUNC_TEST=TRUE
116 64 63	IN	PPDCIN_G3H_CHGR	X5 FUNC_TEST=TRUE

USB_C

TP_UPC_XA_SWD_DATA	---------->	TP3001
TP_UPC_XA_SWD_CLK	---------->	TP3002
TP_UPC_XB_SWD_DATA	---------->	TP3003
TP_UPC_XB_SWD_CLK	---------->	TP3004

104 103	IN	TP_UPC_TA_DBG_UART_TX	FUNC_TEST=TRUE
104 103	IN	TP_UPC_TA_DBG_UART_RX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_TX	FUNC_TEST=TRUE
105 103	IN	TP_UPC_TB_DBG_UART_RX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_TX	FUNC_TEST=TRUE
30 29	IN	UPC_XA_DBG_UART_RX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_TX	FUNC_TEST=TRUE
31 29	IN	TP_UPC_XB_DBG_UART_RX	FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TB_VBUS_CONN	X5 FUNC_TEST=TRUE
116 115 106	IN	PP20V_USBC_TA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5
116 115 32	IN	PP20V_USBC_XB_VBUS_CONN	X4 FUNC_TEST=TRUE
116 115 32	IN	PP20V_USBC_XA_VBUS_CONN	X5 FUNC_TEST=TRUE
		GND	X5

SSD DEBUG CONNECTOR

115 87 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
80 77	IN	SSD_BOOT_LB_L	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_CLK_CONN	FUNC_TEST=TRUE
103 86 80	IN	SSD_DEBUG_I2C_DAT_CONN	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_R2D_L	FUNC_TEST=TRUE
80 77 48	IN	SMC_OOB1_D2R_L	FUNC_TEST=TRUE
83 82 81 80 78 77 85 80	IN	PP1V8_SSD_FMC	
		GND	

MIC

58	IN	DMIC1_CLK	FUNC_TEST=TRUE
58	IN	DMIC1_DATA	FUNC_TEST=TRUE
58	IN	DMIC2_CLK	FUNC_TEST=TRUE
58	IN	DMIC2_DATA	FUNC_TEST=TRUE
109 61	IN	PP1V8_S0	FUNC_TEST=TRUE
		GND	

USB-C PROBE BLOCK TESTING

32	IN	TP_J3300_P2	FUNC_TEST=TRUE	1 TP-P6 A	TPAC580
32	IN	TP_J3300_P56	FUNC_TEST=TRUE	1 TP-P6 A	TPAC581
106	IN	TP_JB500_P2		1 TP-P6 A	TPAC582
106	IN	TP_JB500_P56	FUNC_TEST=TRUE	1 TP-P6 A	TPAC583

ADDITIONAL TPs

110	IN	PP3V3_S5	FUNC_TEST=TRUE	1 TP-P6 A	TPAC584
110	IN	PP3V3_SUS	FUNC_TEST=TRUE	1 TP-P6 A	TPAC585

Wifi & SSD fixture Test Points

(row,col)=(4,2) Diameter=0.6mm Pitch=1mm

Right Side - Top Layer

		1 TP-P6 A	TPAC528
80 77	SSD_JTAG_TMS	1 TP-P6 A	TPAC519
80 77	SSD_JTAG_TCK	1 TP-P6 A	TPAC520
80 77	SSD_JTAG_TDI	1 TP-P6 A	TPAC521
80 77	SSD_JTAG_TDO	1 TP-P6 A	TPAC522
86 77	SSD_DEBUG_I2C_CLK	1 TP-P6 A	TPAC523
86 77	SSD_DEBUG_I2C_DAT	1 TP-P6 A	TPAC524
84 77	SSD_PGOOD_L	1 TP-P6 A	TPAC535

(row,col)=(2,6) Diameter=0.6mm Pitch=1mm

Left Side - Top Layer

50 114	PPDCIN_G3H	1 TP-P6 A	TPAC500
50 114	PPDCIN_G3H	1 TP-P6 A	TPAC501
50 114	PPDCIN_G3H	1 TP-P6 A	TPAC502
50 114	PPDCIN_G3H	1 TP-P6 A	TPAC503
		1 TP-P6 A	TPAC504
		1 TP-P6 A	TPAC505
		1 TP-P6 A	TPAC506
		1 TP-P6 A	TPAC507
	GND TRUE	1 TP-P6 A	TPAC529
64	HPWR_EN_L	1 TP-P6 A	TPAC512
110	PP3V3_S0	1 TP-P6 A	TPAC536
114 109	PP3V3_G3H	1 TP-P6 A	TPAC518

(row,col)=(5,5) Diameter=0.6mm Pitch=1mm

Middle - Top Layer

46 45 48 47	SMC_ONOFF_L	1 TP-P6 A	TPAC517
		1 TP-P6 A	TPAC538
28 20 114	SMC_RESET_L	1 TP-P6 A	TPAC539
		1 TP-P6 A	TPAC527
14	USB3_TEST_D2R_N	1 TP-P6 A	TPAC510
14	USB3_TEST_D2R_P	1 TP-P6 A	TPAC511
		1 TP-P6 A	TPAC595
		1 TP-P6 A	TPAC596
84 78	PP1V0_SSD_CORE	1 TP-P6 A	TPAC598
109	PPVCC_S0_CPU	1 TP-P6 A	TPAC597
109	PPBUS_G3H	1 TP-P6 A	TPAC599
14	USB3_TEST_R2D_N	1 TP-P6 A	TPAC525
14	USB3_TEST_R2D_P	1 TP-P6 A	TPAC526
29 35	AP_RESET_L	1 TP-P6 A	TPAC537
14	USB_TEST_P	1 TP-P6 A	TPAC530
14	USB_TEST_N	1 TP-P6 A	TPAC531
29 115	SSD_RESET_L	1 TP-P6 A	TPAC532
46 12 75	PM_PCH_SYS_PWROK	1 TP-P6 A	TPAC533
87 14 115	SSD_PWR_EN	1 TP-P6 A	TPAC534
46 29 47	SMC_DEBUGPRT_TX_L	1 TP-P6 A	TPAC508
46 29 47	SMC_DEBUGPRT_RX_L	1 TP-P6 A	TPAC509
87 15 115 101	SSD_BOOT_L	1 TP-P6 A	TPAC513
29 27 49 89 76	PM_SLP_S3_L	1 TP-P6 A	TPAC514
48	SMC_DEV_SUPPLY_R_L	1 TP-P6 A	TPAC515
20 32 35	PLT_RST_L	1 TP-P6 A	TPAC516

PAGE TITLE

ICT & FCT 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 125 OF 145

SHEET 114 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

OTHER TEST POINTS / NC

NC with No Testpoint Property

13	NC_CLINK_CLK	1	TRUE		NC_CLINK_CLK
13	NC_CLINK_DATA	1	TRUE		NC_CLINK_DATA
13	NC_CLINK_RESET_L	1	TRUE		NC_CLINK_RESET_L
113 18 12	NC_ITPXDP_CLK100MN	1	TRUE		NC_ITPXDP_CLK100MN
113 18 12	NC_ITPXDP_CLK100MP	1	TRUE		NC_ITPXDP_CLK100MP
13	NC_HDA_SDIN1	1	TRUE		NC_HDA_SDIN1
**	NC_SPI_SMC_MOSI	1			48
12	NC_SPI_SMC_MISO	1			48
14	NC_SPI_SMC_CS_L	1			48
13	NC_SPI_SMC_CLK	1			48
17	NC_PCH_CLK32K_RTCX2				20

FAN Test Points

123	TRUE	FAN_LT_PWM	43 56 114
124	TRUE	FAN_LT_TACH	43 56 114
127	TRUE	PP5V_S0	38 110 115
128	TRUE	FAN_RT_PWM	43 56 114
129	TRUE	FAN_RT_TACH	43 56 114
130	TRUE	PP5V_S0	38 110 115

XDP Test-Points

152	TRUE	XDP_CPU_TCK	6 18
153	TRUE	XDP_PCH_TCK	13 18
167	TRUE	XDP_CPU_TDI	6 18
166	TRUE	XDP_CPU_TDO	6 18
155	TRUE	XDP_CPU_TRST_L	6 13 18
154	TRUE	XDP_CPU_TMS	6 18
158	TRUE	XDP_PCH_TMS	13 18
162	TRUE	XDP_PCH_TDI	13 18
161	TRUE	XDP_PCH_TDO	13 18
168	TRUE	XDP_CPU_PREQ_L	6 13 18
159	TRUE	XDP_CPU_PRDY_L	6 13 18
163	TRUE	PM_RSMRST_L	12 18 46 73
164	TRUE	PM_PCH_PWROK	12 70
165	TRUE	PM_SYSRST_L	12 18 46
156	TRUE	CPU_CFG<3>	6 18

CPU (Refer to CPU pages)

CPU_DC_B2_C1	TP0501
CPU_DC_B38_C38	TP0502
CPU_DC_BR2_BR1	TP0503
CPU_DC_C1_B2	TP0504
CPU_DC_C38_B38	TP0505
CPU_DC_BR1_BR2	TP0610
CPU_DC_BR38_BT36	TP0900
CPU_DC_BT36_BR38	TP0901

PCH (Refer to PCH pages)

XDP_PCH_OBSDATA_A0	TP1883
XDP_PCH_OBSDATA_A1	TP1884
XDP_PCH_OBSDATA_A2	TP1870
XDP_PCH_OBSDATA_A3	TP1871
XDP_PCH_OBSDATA_B0	TP1872
XDP_PCH_OBSDATA_B1	TP1885
XDP_PCH_OBSDATA_B2	TP1886
XDP_PCH_OBSDATA_B3	TP1887
XDP_PCH_OBSDATA_D0	TP1877
XDP_PCH_OBSDATA_D1	TP1878
XDP_PCH_OBSDATA_D2	TP1879
XDP_PCH_OBSDATA_D3	TP1880
XDP_PCH_OBSFN_C0	TP1882
XDP_BPM_L<0>	TP1800
XDP_BPM_L<1>	TP1801
XDP_BPM_L<2>	TP1802
XDP_BPM_L<3>	TP1803
NC_USB_EXTA_OC_L	TP1873
NC_USB_EXTB_OC_L	TP1874
NC_USB_EXTC_OC_L	TP1875
NC_USB_EXTD_OC_L	TP1876

TPs on BOTTOM to check USB-C Instalation

175	USBC_XA_SBU1	FUNC_TEST=TRUE	30 32
176	USBC_XB_SBU1	FUNC_TEST=TRUE	31 32
177	USBC_XA_SBU2	FUNC_TEST=TRUE	30 32
178	USBC_XB_SBU2	FUNC_TEST=TRUE	31 32
179	USBC_TA_SBU1	FUNC_TEST=TRUE	104 106
180	USBC_TB_SBU1	FUNC_TEST=TRUE	105 106
181	USBC_TA_SBU2	FUNC_TEST=TRUE	104 106
182	USBC_TB_SBU2	FUNC_TEST=TRUE	105 106
***	PP20V_USBC_XA_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
183	PP20V_USBC_XB_VBUS_CONN	FUNC_TEST=TRUE	32 114 116
185	PP20V_USBC_TA_VBUS_CONN	FUNC_TEST=TRUE	106 114 116
184	PP20V_USBC_TB_VBUS_CONN	FUNC_TEST=TRUE	106 114 116

TPs to check LifeBoat Instalation

186	PP3V3_S5_POLARIS	FUNC_TEST=TRUE	84 87
187	PP3V3_S5	FUNC_TEST=TRUE	110
192	SSD_PWR_EN	FUNC_TEST=TRUE	14 87 114
189	SSD_PWR_LB_EN	FUNC_TEST=TRUE	84 87
191	SSD_BOOT_L	FUNC_TEST=TRUE	15 87 114
197	SSD_BOOT_LB_L	FUNC_TEST=TRUE	77 87 114
193	SSD_RESET_L	FUNC_TEST=TRUE	14 20 87 114
195	SSD_RESET_LB_L	FUNC_TEST=TRUE	77 87
194	SSD_CLKREQ_L	FUNC_TEST=TRUE	20 87
196	SSD_CLKREQ_LB_L	FUNC_TEST=TRUE	77 87

SYNC_MASTER=K363_BBABADI SYNC_DATE=01/26/2016

PAGE TITLE: NC & No Test

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 126 OF 145

SHEET 115 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
131S00041	6	CAP,CER,12PF,5%,100V,C0G,0402	CC784,CC785,CC786,CC787,CC788	CRITICAL	

PAGE TITLE

Desense Caps

Apple Inc.

DRAWING NUMBER 051-00647 | SIZE D

REVISION 10.0.0

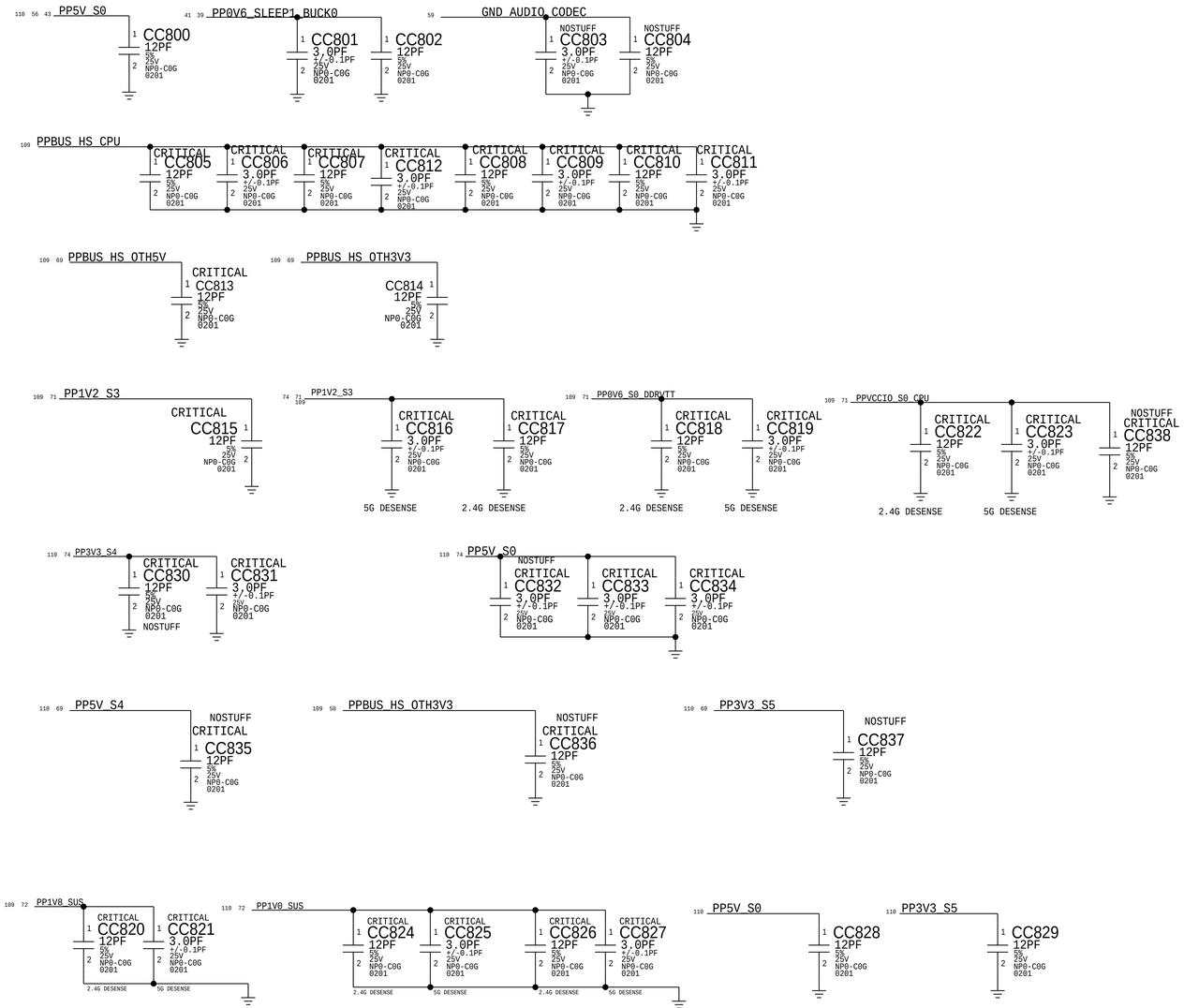
BRANCH dvt-fab10

PAGE 127 OF 145

SHEET 116 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED



BOM_COST_GROUP=WIRELESS

PAGE TITLE: Desense Caps

Apple Inc.

DRAWING NUMBER: 051-00647 | SIZE: D

REVISION: 10.0.0

BRANCH: dvt-fab10

PAGE: 128 OF 145

SHEET: 117 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC. THE POSESSOR AGREES TO THE FOLLOWING:

I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART

IV ALL RIGHTS RESERVED

SYNC_MASTER=X363_ZIFENGSHEN SYNC_DATE=06/02/2016

PAGE TITLE

Project Specific Constraints

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D

REVISION 10.0.0

BRANCH dvt-fab10

PAGE 130 OF 145

SHEET 118 OF 121

NOTICE OF PROPRIETARY PROPERTY:

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

44 ULA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02212	MLB,2.6G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02120	MLB,2.6G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02591	MLB,2.6G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02214	MLB,2.6G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02587	MLB,2.6G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02116	MLB,2.6G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02589	MLB,2.6G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02586	MLB,2.6G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01615	MLB,2.7G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02592	MLB,2.7G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01614	MLB,2.7G,MC-16,ULA-MC,SSD-512,X36G3	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01603	MLB,2.7G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02594	MLB,2.7G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01602	MLB,2.7G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01639	MLB,2.9G,MC-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01637	MLB,2.9G,MC-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02596	MLB,2.9G,MC-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01638	MLB,2.9G,MC-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01627	MLB,2.9G,SM-16,ULA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01625	MLB,2.9G,SM-16,ULA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02598	MLB,2.9G,SM-16,ULA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01626	MLB,2.9G,SM-16,ULA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_MC_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02154	MLB,2.6G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02119	MLB,2.6G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02590	MLB,2.6G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02213	MLB,2.6G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-02211	MLB,2.6G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02115	MLB,2.6G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02588	MLB,2.6G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-02585	MLB,2.6G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01612	MLB,2.7G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02593	MLB,2.7G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01611	MLB,2.7G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01600	MLB,2.7G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-02595	MLB,2.7G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01599	MLB,2.7G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01636	MLB,2.9G,MC-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01634	MLB,2.9G,MC-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02597	MLB,2.9G,MC-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01635	MLB,2.9G,MC-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB
639-01624	MLB,2.9G,SM-16,ULA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:1TB
639-01622	MLB,2.9G,SM-16,ULA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:256GB
639-02599	MLB,2.9G,SM-16,ULA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:2TB
639-01623	MLB,2.9G,SM-16,ULA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,BAFFIN_ULA,SSD_CONFIG:512GB

36 PROA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02655	MLB,2.7G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02656	MLB,2.7G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02654	MLB,2.7G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02664	MLB,2.7G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02665	MLB,2.7G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02663	MLB,2.7G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02673	MLB,2.9G,MC-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02674	MLB,2.9G,MC-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02672	MLB,2.9G,MC-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02682	MLB,2.9G,SM-16,PROA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02683	MLB,2.9G,SM-16,PROA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02681	MLB,2.9G,SM-16,PROA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02652	MLB,2.7G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02653	MLB,2.7G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02651	MLB,2.7G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02661	MLB,2.7G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02662	MLB,2.7G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02660	MLB,2.7G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02670	MLB,2.9G,MC-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02671	MLB,2.9G,MC-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02669	MLB,2.9G,MC-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02679	MLB,2.9G,SM-16,PROA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02680	MLB,2.9G,SM-16,PROA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02678	MLB,2.9G,SM-16,PROA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02649	MLB,2.7G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02650	MLB,2.7G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02648	MLB,2.7G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02658	MLB,2.7G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02659	MLB,2.7G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02657	MLB,2.7G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.7,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02667	MLB,2.9G,MC-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02668	MLB,2.9G,MC-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02666	MLB,2.9G,MC-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB
639-02676	MLB,2.9G,SM-16,PROA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:1TB
639-02677	MLB,2.9G,SM-16,PROA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:2TB
639-02675	MLB,2.9G,SM-16,PROA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_PROA,SSD_CONFIG:512GB

BOM Variants, Power/Socket Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-01966	PCBA,MLB,NONE,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01967	PCBA,MLB,SKT,VDDC,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01968	PCBA,MLB,SKT,MVDD,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,STARDUST:VDDC?_MVDD,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB
639-01969	PCBA,MLB,SKT,CPU,SM-16,FB4-SM,S256,X363	BASE_BOM,DEVEL_BOM,CPU_SKL:SOCKET,RAM_16G_SAMSUNG_2133,4GB_SM_BAFFIN,SSD_CONFIG:256GB

SYNC_MASTER=J80_MLB SYNC_DATE=07/23/2015

PAGE TITLE
639 BOM Configuration

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 141 OF 145
SHEET 119 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

BOM Variants

48 LEA Configs

BOM NUMBER	BOM NAME	BOM OPTIONS
639-02621	MLB,2.6G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02618	MLB,2.6G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02622	MLB,2.6G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02620	MLB,2.6G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02608	MLB,2.6G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02602	MLB,2.6G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02611	MLB,2.6G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02605	MLB,2.6G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02645	MLB,2.9G,MC-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02643	MLB,2.9G,MC-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02646	MLB,2.9G,MC-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02644	MLB,2.9G,MC-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02633	MLB,2.9G,SM-16,LEA-HY,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02631	MLB,2.9G,SM-16,LEA-HY,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02634	MLB,2.9G,SM-16,LEA-HY,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02632	MLB,2.9G,SM-16,LEA-HY,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_HY_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02647	MLB,2.6G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02616	MLB,2.6G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02619	MLB,2.6G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02617	MLB,2.6G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02607	MLB,2.6G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02601	MLB,2.6G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02610	MLB,2.6G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02604	MLB,2.6G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02641	MLB,2.9G,MC-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02639	MLB,2.9G,MC-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02642	MLB,2.9G,MC-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02640	MLB,2.9G,MC-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02629	MLB,2.9G,SM-16,LEA-MC,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02627	MLB,2.9G,SM-16,LEA-MC,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02630	MLB,2.9G,SM-16,LEA-MC,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02628	MLB,2.9G,SM-16,LEA-MC,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_MC_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02614	MLB,2.6G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02612	MLB,2.6G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02615	MLB,2.6G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02613	MLB,2.6G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02606	MLB,2.6G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02600	MLB,2.6G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02609	MLB,2.6G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02603	MLB,2.6G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.6,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02637	MLB,2.9G,MC-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02635	MLB,2.9G,MC-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02638	MLB,2.9G,MC-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02636	MLB,2.9G,MC-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_MICRON_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB
639-02625	MLB,2.9G,SM-16,LEA-SM,SSD-1TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:1TB
639-02623	MLB,2.9G,SM-16,LEA-SM,SSD-256,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:256GB
639-02626	MLB,2.9G,SM-16,LEA-SM,SSD-2TB,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:2TB
639-02624	MLB,2.9G,SM-16,LEA-SM,SSD-512,X363G	BASE_BOM,DEVEL_BOM,CPU_SKL:2.9,RAM_16G_SAMSUNG_2133,2GB_SM_BAFFIN,BAFFIN_LEA,SSD_CONFIG:512GB

SYNC_MASTER=J80_MLB SYNC_DATE=07/23/2015

PAGE TITLE
639 BOM Configuration 2

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 142 OF 145
SHEET 120 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
740S0144	740S0118		ALL		
740S00003	740S0135		ALL		
376S1089	376S1128		ALL		
376S1080	376S0820		ALL		
376S00086	376S0761		ALL		
376S00074	376S0855		ALL		
376S00014	376S0761		ALL		
372S0186	372S0185		ALL		
371S0713	371S0558		ALL		
311S00060	311S0273		ALL		
311S00004	311S0370		ALL		
155S0914	155S0097		ALL		
155S0694	155S0387		ALL		
155S0660	155S0513		ALL		
155S00154	155S0398		ALL		
155S00007	155S0667		ALL		
138S0863	138S0853		ALL		
138S0775	138S0860		ALL		<rdar://problem/23155097> for IG <rdar://problem/23564467> for EG
138S0703	138S0648		ALL		<rdar://problem/23118804> for IG <rdar://problem/> for EG
132S00064	132S0409		ALL		
128S0325	128S0397		ALL		
128S00029	128S00007		ALL		
128S00026	128S00011		ALL		
128S00070	128S00007		ALL		<rdar://problem/25329164>
128S00009	128S00007		ALL		
107S0249	107S0251		ALL		
107S00071	107S00053		ALL		
107S00070	107S00085		ALL		
107S00033	107S00034		ALL		BLC
107S00015	107S00011		ALL		
376S1106	376S0678		ALL	Fairchild alt to Vishay	BLC
138S0738	138S1101		ALL	Samsung alt to Murata	
138S0846	138S0811		ALL	Samsung alt to Murata	
376S1053	376S0604		ALL	Diodes alt to Fairchild	
152S00359	152S00253		ALL	Chillisin alt to Cyntec	
740S00027	740S0159		ALL	Bourns alt to Little Fuse	
371S0704	371S00077		ALL	NXP alt to Diodes	
138S00032	138S0831		ALL		
138S00049	138S0831		ALL		

220uF 2.0V D-case, 128S00044 DQ

998-04070	998-04071		OFF	Hynix alt to SS	T208
128S00010	128S00011		ALL		
128S00031	128S00011		ALL		
138S00084	138S00060		ALL		<rdar://problem/23118634> for IG <rdar://problem/23527737> for EG
155S00155	155S0441		OFF		(Stale; delete later after page sync)
155S00190	155S0897		ALL		
353S00107	353S3239		ALL		
353S00525	353S4471		ALL		
376S1193	376S00037		OFF		
740S00028	740S0118		ALL		
152S00369	152S00268		ALL	Cyntec w/ NEC	<rdar://problem/23405116> for IG <rdar://problem/23542193> for EG
128S0296	128S0487		ALL	NEC w/ pana	<rdar://problem/23422212> for IG <rdar://problem/23527282> for EG
128S00012	128S0487		ALL	NEC w/ Rohm	
155S00188	155S0275		ALL	Murata w/ Taiyo	<rdar://problem/23446936> for IG <rdar://problem/23542939> for EG
155S00018	155S0664		ALL	Murata w/ Taiyo	<rdar://problem/23447549> for IG <rdar://problem/23543068> for EG
152S00388	152S00182		ALL		<rdar://problem/23542023>
107S0240	107S0255		ALL		<rdar://problem/23520324>
128S00062	128S00067		ALL	NEC for Panasonic	150uF 6.3V B12
138S0660	138S0684		ALL		<rdar://problem/24316249>
155S00204	155S0731		ALL		<rdar://problem/24310837>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S0271	311S00008		ALL	NXP w/ Diodes	(Stale; delete later after page sync) <rdar://problem/23117904> for IG <rdar://problem/24316367> for EG
197S00046	197S00036		ALL	Epson w/ TXC	<rdar://problem/23117749> for IG <rdar://problem/23543146> for EG
197S00047	197S00036		ALL	Kyocera w/ TXC	
197S00048	197S00036		ALL	Murata w/ TXC	
197S00053	197S00050		ALL	Kyocera w/ TXC	<rdar://problem/23117849> for IG <rdar://problem/23543858> for EG
197S00054	197S00050		ALL	NDK w/ TXC	
197S00055	197S00050		ALL	Murata w/ TXC	
311S0596	311S0593		ALL	NXP w/ Diodes	<rdar://problem/23118093> for IG <rdar://problem/23544024> for EG
107S0276	107S00020		ALL	Cyntec w/ TFT	<rdar://problem/23117951> for IG <rdar://problem/23542980> for EG
107S00021	107S0284		ALL	TFT w/ Yageo	<rdar://problem/23129685> for IG <rdar://problem/23519943> for EG
132S00012	132S0401		ALL	Taiyo w/ Murata&TDK	<rdar://problem/23118402> for IG <rdar://problem/23527525> for EG
152S00343	152S1682		ALL	NXP w/ Diodes	<rdar://problem/23541694> for IG <rdar://problem/23541871> for EG
107S00087	107S00029		ALL	TFT w/ Yageo	<rdar://problem/23121290> for IG <rdar://problem/23520039> for EG
128S00057	128S00018		ALL	NEC w/ Vishay	<rdar://problem/23363718> for IG <rdar://problem/23526361> for EG
128S00058	128S00018		ALL	NEC w/ Rohm	
128S0364	128S0264		ALL	Kemet w/ Panasonic	<rdar://problem/23366105> for IG <rdar://problem/23527232> for EG
138S0641	138S0700		ALL	Murata w/ SS&Taiyo	<rdar://problem/23118759> for IG <rdar://problem/23528188> for EG
138S0739	138S0706		ALL	NEC w/ Vishay	<rdar://problem/23118915> for IG <rdar://problem/23528364 for EG
138S0945	138S0706		ALL	NEC w/ Rohm	
152S00358	152S00208		ALL	Murata w/ Chillisin	<rdar://problem/23119390> for IG <rdar://problem/23542069> for EG
152S00389	152S00241		OFF	Cyntec w/ Vishay	<rdar://problem/23342644> for IG <rdar://problem/> for EG
152S00390	152S00265		OFF	Cyntec w/ Vishay	<rdar://problem/23342719> for IG <rdar://problem/> for EG
152S00400	152S1872		ALL	Murata w/ Cyntec	
152S1872	152S00361		ALL	Murata w/ Cyntec	<rdar://problem/23132240> for IG <rdar://problem/23542412> for EG
155S00034	155S0706		ALL	Taiyo w/ Murata	<rdar://problem/23118020> for IG <rdar://problem/23543018> for EG

371S00082	371S00046		ALL	On-Semi w/ Diodes	<rdar://problem/23341512> for IG <rdar://problem/23545301> for EG
376S00146	376S1061		ALL	NXP w/ Diodes	<rdar://problem/23341674> for IG <rdar://problem/23545469> for EG
353S00711	353S2073		ALL	On Semi w/ TI	<rdar://problem/23605939> for IG <rdar://problem/23605957> for EG

740S00019	740S00007		ALL	Bourns w/ Polytronics	<rdar://problem/23137505> for IG <rdar://problem/23545479> for EG
155S00189	155S0342		ALL	Murata w/ Taiyo	<rdar://problem/23117986> for IG <rdar://problem/23543015> for EG
132S0438	132S0428		ALL	Murata w/ Taiyo&TDK	<rdar://problem/23118548> for IG <rdar://problem/23527609> for EG
138S0714	138S0713		ALL	Murata w/ Samsung	<rdar://problem/23118842> for IG <rdar://problem/23528300> for EG
138S0715	138S0732		ALL	Murata w/ Samsung	<rdar://problem/23118873> for IG <rdar://problem/23528349> for EG
107S00086	107S00056		ALL	TFT w/ Cyntec	<rdar://problem/23121312> for IG <rdar://problem/23520074> for EG
138S0875	138S0678		ALL	Taiyo w/ Mur&SS	<rdar://problem/23129763> for IG <rdar://problem/23528106> for EG
138S0786	138S0705		ALL	Murata w/ Samsung	<rdar://problem/23129934> for IG <rdar://problem/23528216> for EG
155S0382	155S0659		ALL	Murata w/ TDK	<rdar://problem/23132624> for IG <rdar://problem/23543045> for EG
152S2052	152S1954		ALL	Taiyo w/ Cyntec	<rdar://problem/23135833> for IG <rdar://problem/23542478> for EG
152S2015	152S1958		ALL	Taiyo w/ Cyntec	<rdar://problem/23137154> for IG <rdar://problem/23542579> for EG
128S00055	128S00002		ALL	Kemet w/ Panasonic	<rdar://problem/23148659> for IG <rdar://problem/23526236> for EG
138S0748	138S0751		ALL	Murata w/ SS	<rdar://problem/23155052> for IG <rdar://problem/23528417> for EG
138S00102	138S0773		ALL	Murata w/ Taiyo	<rdar://problem/23155089> for IG <rdar://problem/23529046> for EG
138S0789	138S0941		ALL	Murata w/ SS	<rdar://problem/23155132> for IG <rdar://problem/23529142> for EG
107S00101	107S00005		ALL	Cyntec w/ Yageo	<rdar://problem/23193801> for IG <rdar://problem/23519872> for EG
107S00102	107S00017		ALL	Cyntec w/ Yageo	<rdar://problem/23194019> for IG <rdar://problem/23519914> for EG
107S00100	107S00057		ALL	Cyntec w/ TFT	<rdar://problem/23224358> for IG <rdar://problem/23520119> for EG
107S00103	107S00058		ALL	Cyntec w/ Yageo	<rdar://problem/23228523> for IG <rdar://problem/23520163> for EG
107S00104	107S00061		ALL	Cyntec w/ Yageo	<rdar://problem/23229217> for IG <rdar://problem/23520193> for EG
107S00105	107S00062		ALL	Cyntec w/ Yageo	<rdar://problem/23230371> for IG <rdar://problem/23520241> for EG
152S00403	152S00322		ALL	Murata w/ Chillisin	<rdar://problem/23341061> for IG <rdar://problem/23542282> for EG
353S00852	353S4262		ALL	TI w/ OnSemi	<rdar://problem/23341158> for IG <rdar://problem/23542282> for EG

138S00104	138S0978		ALL		<rdar://problem/23583487>
128S00069	128S00067		ALL	Rohm for Panasonic	150uF 6.3V B12 <rdar://problem/23527054>
138S0759	138S0762		ALL		<rdar://problem/23582324>
377S0077	377S0183		ALL		<rdar://problem/23640745>
152S00363	152S00048		ALL		<rdar://problem/23541533>
138S00111	138S00036		ALL		<rdar://problem/23546425>
138S00097	138S0750		ALL		<rdar://problem/23581953>
155S00203	155S0894		ALL		<rdar://problem/24285018>
116S00006	116S0175		ALL		<rdar://problem/23524119>
311S00104	311S00091		ALL		<rdar://problem/23640575>

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
311S00013	311S0508		ALL	Part will be stuffed in production	<rdar://problem/24316400>
311S00118	311S0489		ALL		<rdar://problem/27623384>
311S00072	311S0657		ALL		<rdar://problem/23595055>
311S00090	311S00028		ALL		<rdar://problem/23602138>
353S00750	353S00877		ALL		<rdar://problem/23545068>
353S00878	353S00599		ALL		<rdar://problem/23545040>
311S00105	311S0233		ALL		<rdar://problem/24316381>
353S00880	353S3452		ALL		<rdar://problem/23545099>
311S00007	311S0426		ALL		<rdar://problem/23597412>
128S0445	128S0392		ALL		<rdar://problem/23566873>
152S00415	152S00140		ALL		<rdar://problem/23766197>
128S0436	128S0392		ALL		<rdar://problem/23566873>
343S00135	343S00136		ALL	T208	
343S00137	343S00136		ALL	T208	
343S00138	343S00136		ALL	T208	
138S00105	138S00037		ALL		<rdar://problem/23640133>
152S00434	152S1829		ALL		<rdar://problem/23825631>
353S3527	353S3528		ALL		<rdar://problem/24492801>
353S3526	353S3528		ALL		<rdar://problem/24492801>
353S00135	353S00034		ALL		<rdar://problem/24534121>
353S2220	353S00034		ALL		<rdar://problem/24534121>
353S00769	353S4398		ALL		<rdar://problem/24534714>
353S00879	353S00754		ALL		<rdar://problem/23545080>
104S00012	155S0398		ALL		<rdar://problem/25180014>
353S4342	353S00854		ALL		<rdar://problem/23621422>
152S00543	152S00484		ALL		<rdar://problem/24780681>
371S00089	371S00085		ALL		<rdar://problem/24806090>
107S00111	107S00110		ALL		<rdar://problem/24968171>
335S00213	335S0888		ALL		<rdar://problem/24985900>
311S0437	311S00112		ALL		<rdar://problem/24747570>
377S0178	377S00031		ALL		<rdar://problem/25118595>
371S00091	371S00083		ALL		<rdar://problem/24827333>
197S00069	197S00068		ALL		<rdar://problem/24473517>
138S0698	138S00113		ALL		<rdar://problem/23528153>
152S00461	152S00112		ALL		<rdar://problem/24417973>
371S00074	371S0602		ALL		<rdar://problem/25919460>
197S00082	197S00081		ALL		
353S00991	353S00920		ALL		
131S00134	131S00041		ALL		<rdar://problem/24316117>

PAGE TITLE
Alternates BOM Table

Apple Inc.

DRAWING NUMBER 051-00647 SIZE D
REVISION 10.0.0
BRANCH dvt-fab10
PAGE 145 OF 145
SHEET 121 OF 121

NOTICE OF PROPRIETARY PROPERTY:
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE INC.
THE POSESSOR AGREES TO THE FOLLOWING:
I TO MAINTAIN THIS DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IT IN WHOLE OR PART
IV ALL RIGHTS RESERVED