CR-1

1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
		?		?	?

Page	Circuits	ENG	Block
1	Table of Contents	KG	
2	Block Diagram	KG	
3	Microprocessor	KG	Processor
4	L3 CACHE & BYPASS	KG	
5	PANGEA PROCESSOR IF	KG	
6	PANGEA SDRAM IF & SDRAM DIMMS	KG	Sys Memory
7	SYSTEM CLOCKS, TERMS, CKE LATCH	KG	Clocks
8	PANGEA AGP INTERFACE, SYSTEM ROM	KG,LL	AGP, Graphics & ROM
9	VIDEO ASIC SEC 1 (AGP & VIDEO OUT)	LL	
10	VIDEO ASIC SEC 2 (FRAME BUFFER IF)	LL	
11	GRAPHICS SDRAMS	LL	
12	VIDEO ASIC SEC 3 (UNUSED CRUD!)	LL	
13	PANGEA ETHERNET, FIREWIRE, PWR/GNDS	RM	Enet, FW
14	PANGEA BYPASS	KG	
15	Ethernet PHY	RM	
16	Firewire PHY, Termination	LL	
17	PANGEA ATA, & PCMCIA BUSSES	RM	HD,Cdbus Modem,USB
18	PANGEA SER/AUD/USB, BOOTSTRAP PINS	RM	
19	USB CONN & PWR	RM	
20	MLB Pull-ups	ALL	PUs
21	L3 VOLTAGE REGULATORS, BOOTBANGER	KK	Power
22	Voltage Regulators	KK	
23	Power Manager Unit	KK	
24	ESP, LA CONNECTORS, AND CPU BYPASS	KG	CONNECTORS
25	Internal & External Video Conns	LL	
26	HD/CD/MODEM/PCMCIA/KITCHENSINK CONN'S	RM	
27	DC/DC CONVERTER (5V AND 3.3V)	KK	POWER STUFF
28	MORE POWER SUPPLY STUFF	KK	
29	TUMBLER AUDIO, CONTROL & D/A	LH	Audio
30	TUMBLER AUDIO, HEADPHONE DRIVER	LH	
31	TUMBLER AUDIO, INTERNAL MIC AND CALL PROGRESS	LH	
32	TUMBLER AUDIO, POWER AMPLIFIER	LH	
33	HOLES AND SLOTS, AND EMC TABLES	KG	
34-40	CONSTRAINT TABLES	ALL	
41-44	Part Tables	RM	

PVT

OCT 13, 2001

POWER RAIL DEFINITIONS

	RUN	SLEEP	SHUTDOWN
+5V	ON	ON	OFF
+5VSD	ON	OFF	OFF
+12V_MAIN	ON	ON	ON
+12VSD	ON	OFF	OFF
+3.3V	ON	ON	OFF

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER / DESIGN CK / ENG APPD / MFG APPD / QA APPD / DESIGNER / RELEASE / SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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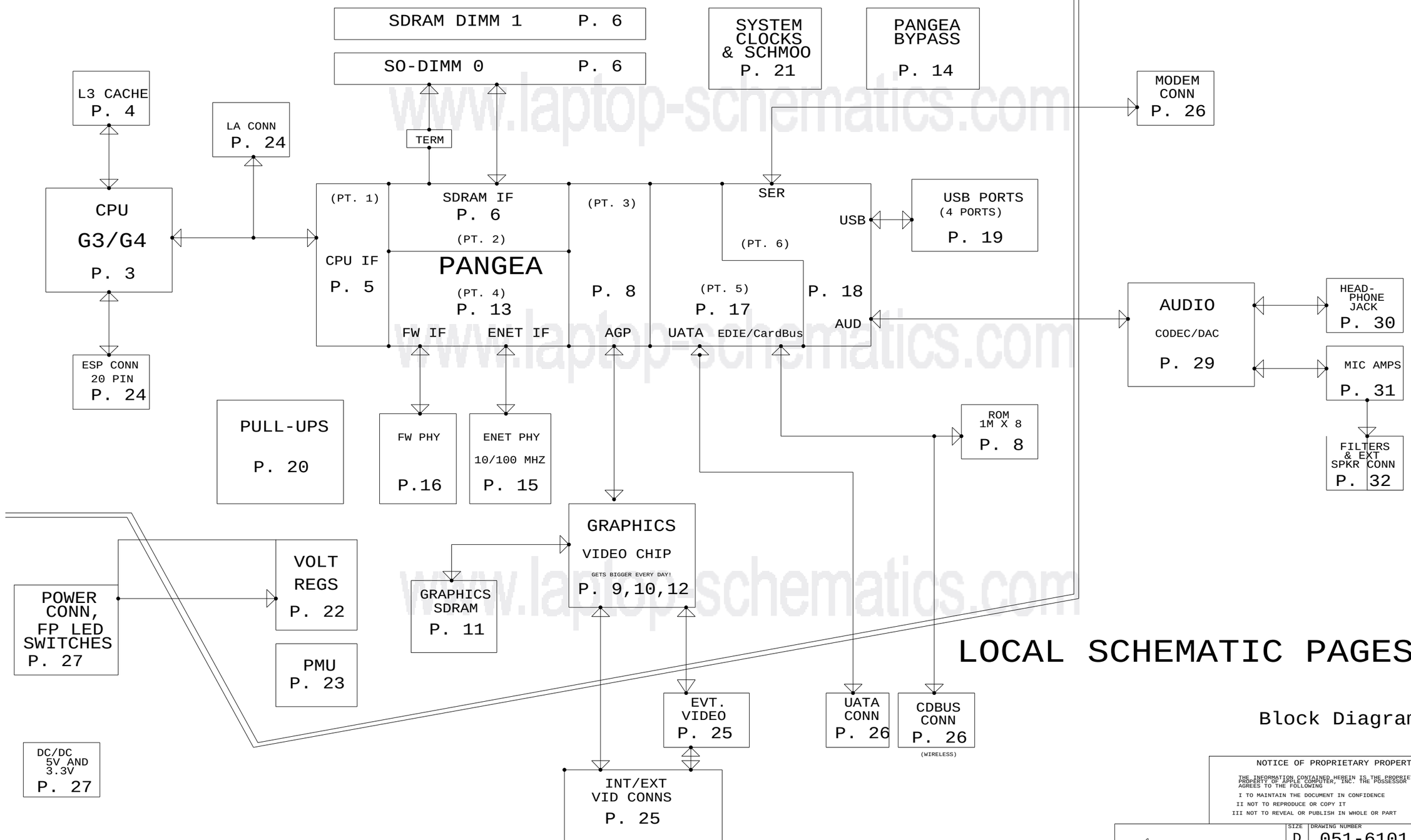
TITLE
SCHEM,PCBA,"Clior"

DRAWING NUMBER 051-6101 REV. 12

SHT 1 OF 44

CORE SCHEMATIC PAGES



LOCAL SCHEMATIC PAGES

Block Diagram

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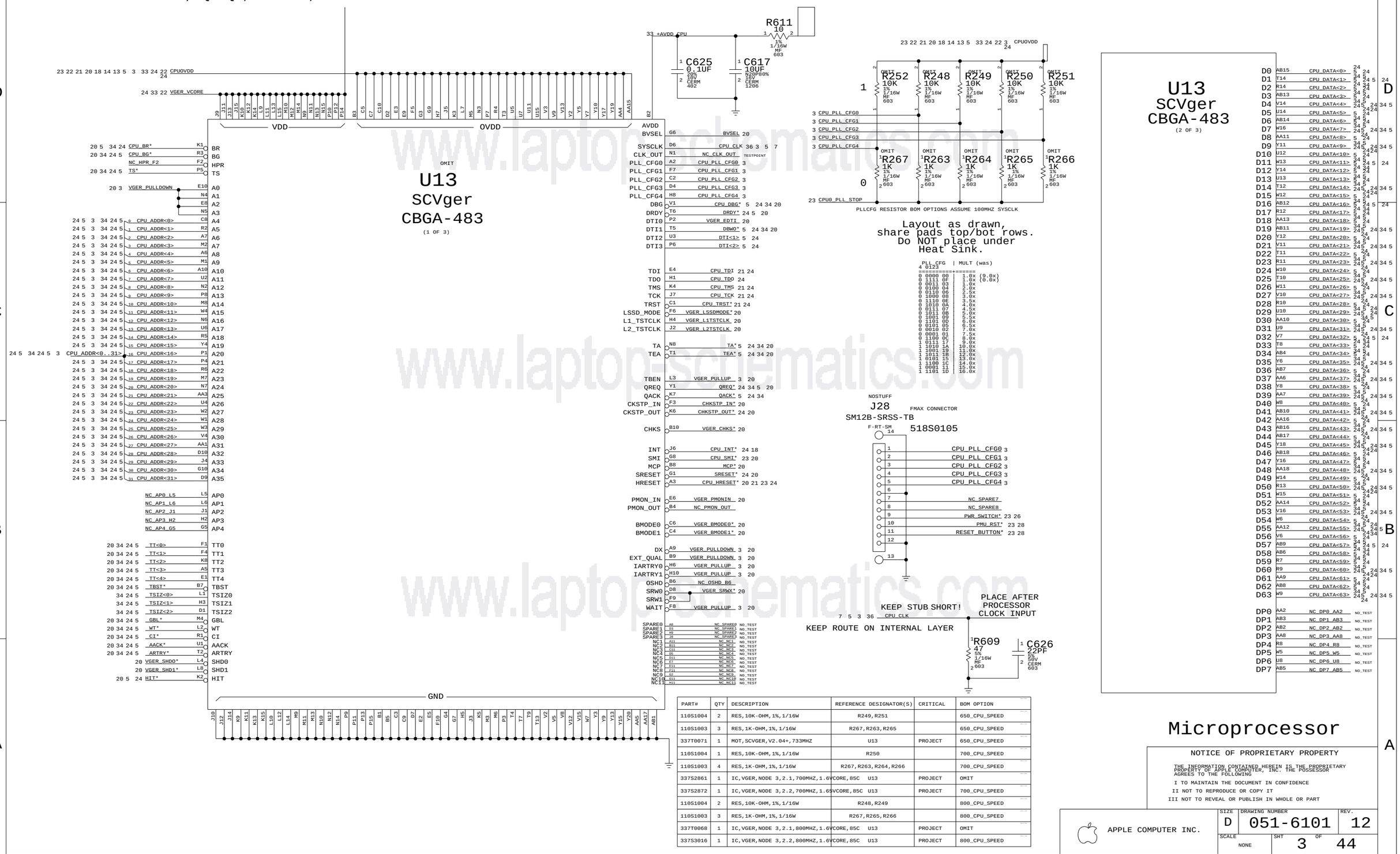
PRIORITY NETS ARE TS*, QREQ*, ARTRY*, BR*



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
110S1004	2	RES,10K-OHM,1%,1/16W	R249,R251		650_CPU_SPEED
110S1003	3	RES,1K-OHM,1%,1/16W	R267,R263,R265		650_CPU_SPEED
337T0071	1	MOT,SCVGER,V2.04+,733MHZ	U13	PROJECT	650_CPU_SPEED
110S1004	1	RES,10K-OHM,1%,1/16W	R250		700_CPU_SPEED
110S1003	4	RES,1K-OHM,1%,1/16W	R267,R263,R264,R266		700_CPU_SPEED
337S2861	1	IC,VGER,NODE 3,2.1,700MHZ,1.6VCORE,85C	U13	PROJECT	OMIT
337S2872	1	IC,VGER,NODE 3,2.2,700MHZ,1.65VCORE,85C	U13	PROJECT	700_CPU_SPEED
110S1004	2	RES,10K-OHM,1%,1/16W	R248,R249		800_CPU_SPEED
110S1003	3	RES,1K-OHM,1%,1/16W	R267,R265,R266		800_CPU_SPEED
337T0068	1	IC,VGER,NODE 3,2.1,800MHZ,1.6VCORE,85C	U13	PROJECT	OMIT
337S3016	1	IC,VGER,NODE 3,2.2,800MHZ,1.6VCORE,85C	U13	PROJECT	800_CPU_SPEED

Microprocessor

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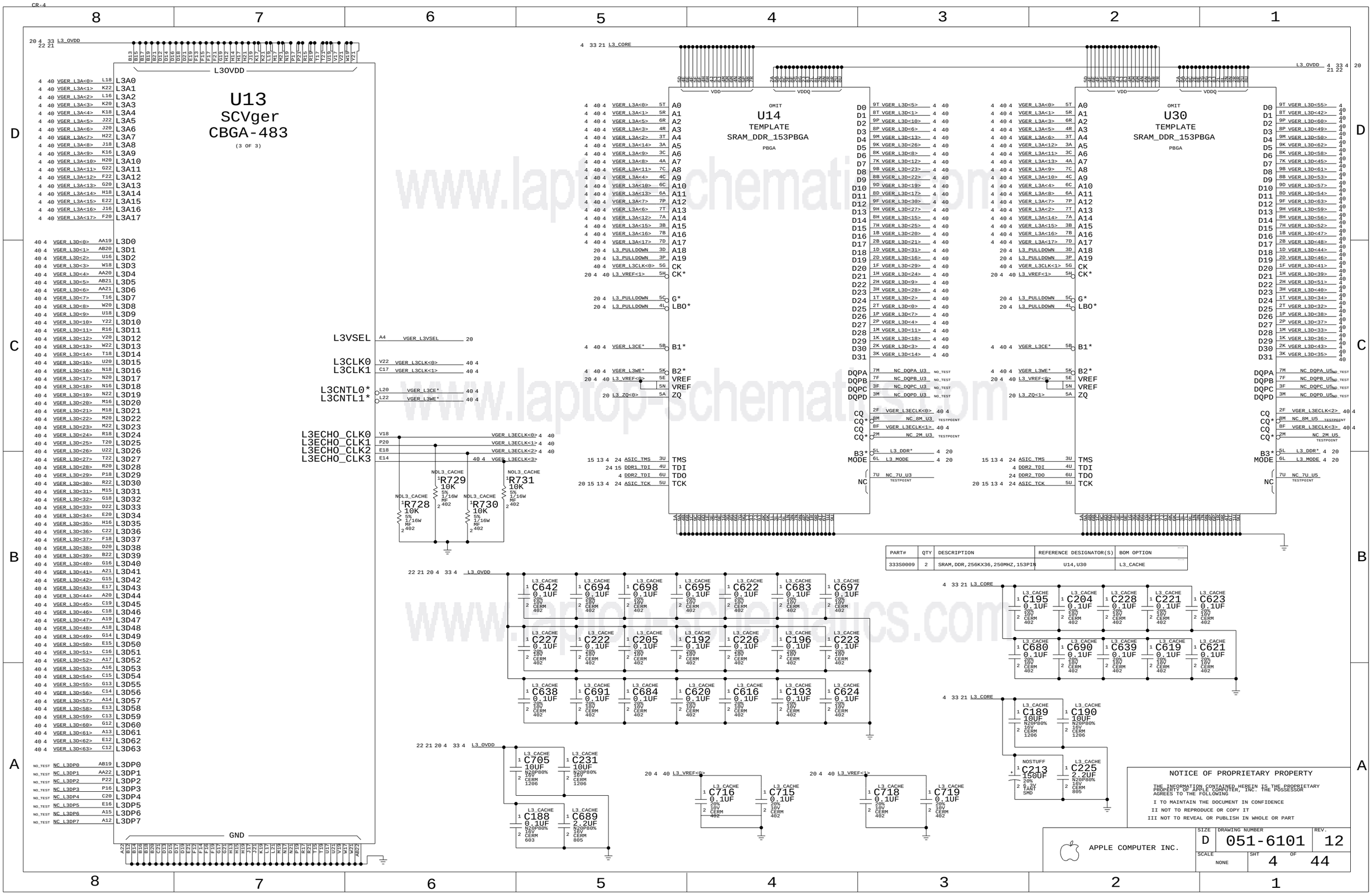

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
333S0009	2	SRAM,DDR,256KX36,250MHZ,153PIN	U14,U30	L3_CACHE

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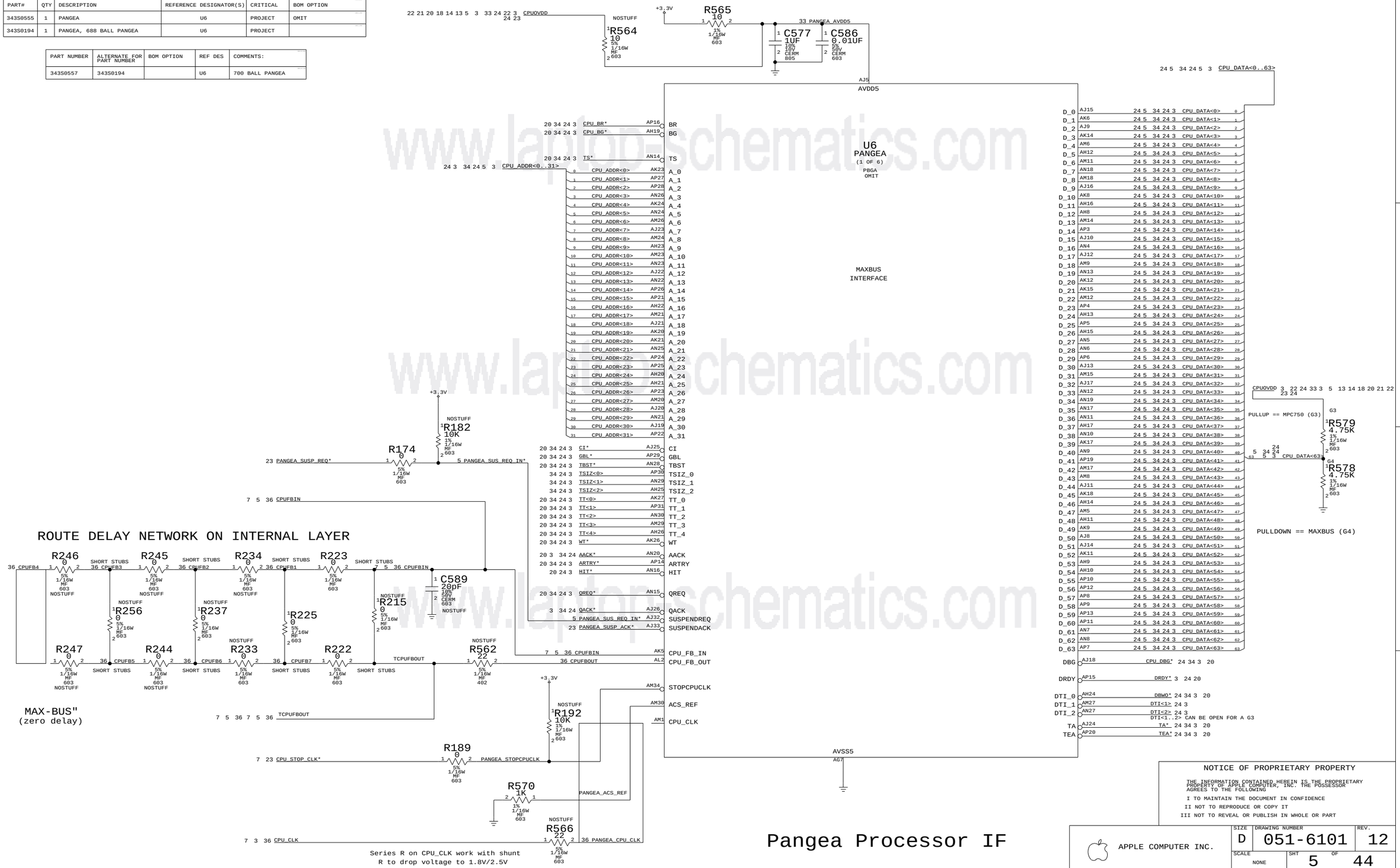
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0555	1	PANGEA	U6	PROJECT	OMIT
343S0194	1	PANGEA, 688 BALL PANGEA	U6	PROJECT	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0557	343S0194		U6	700 BALL PANGEA



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Pangea Processor IF

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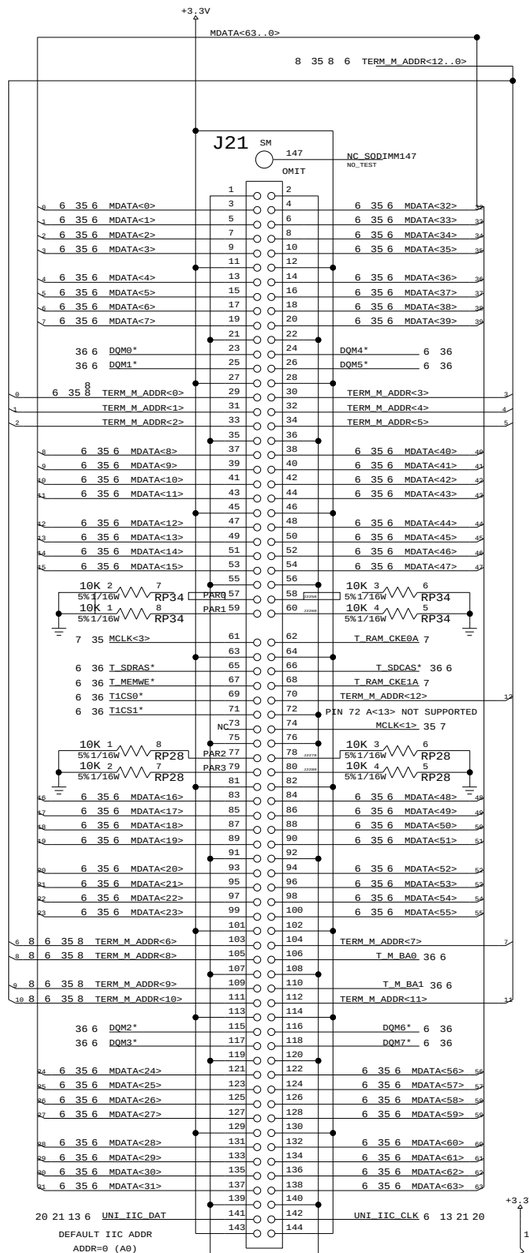
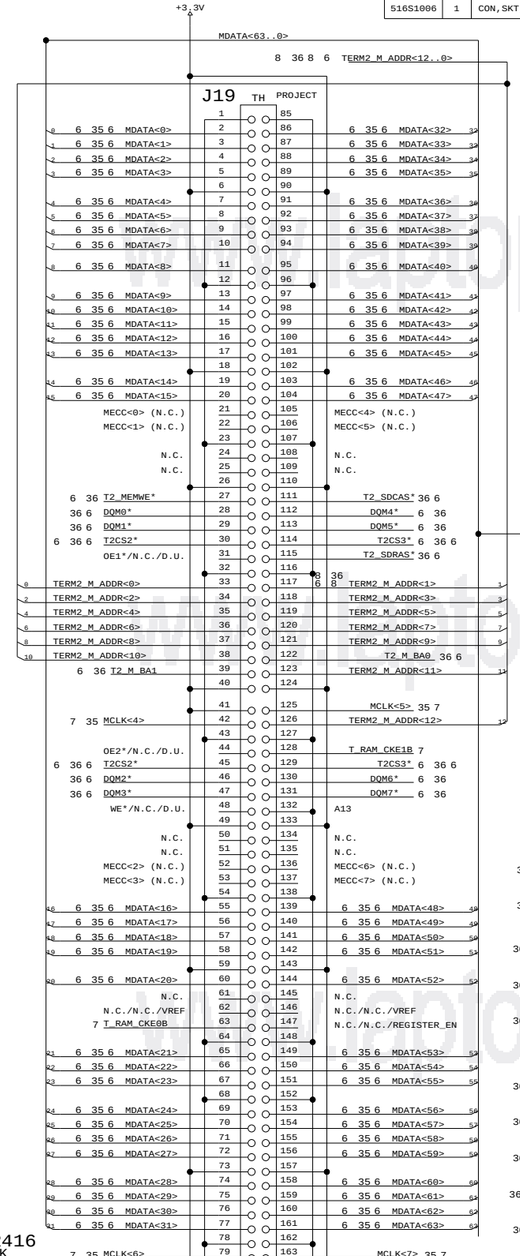
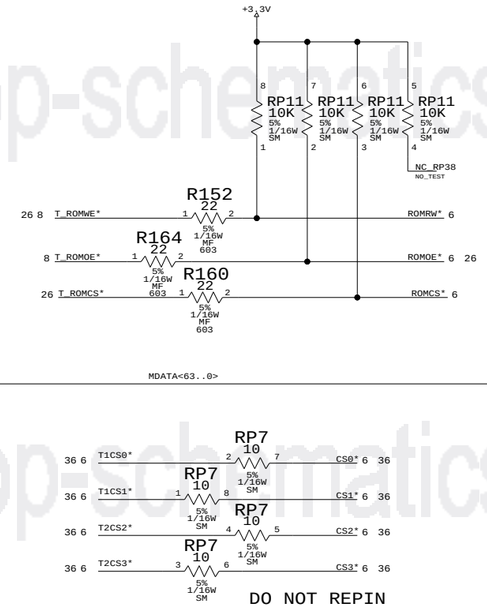
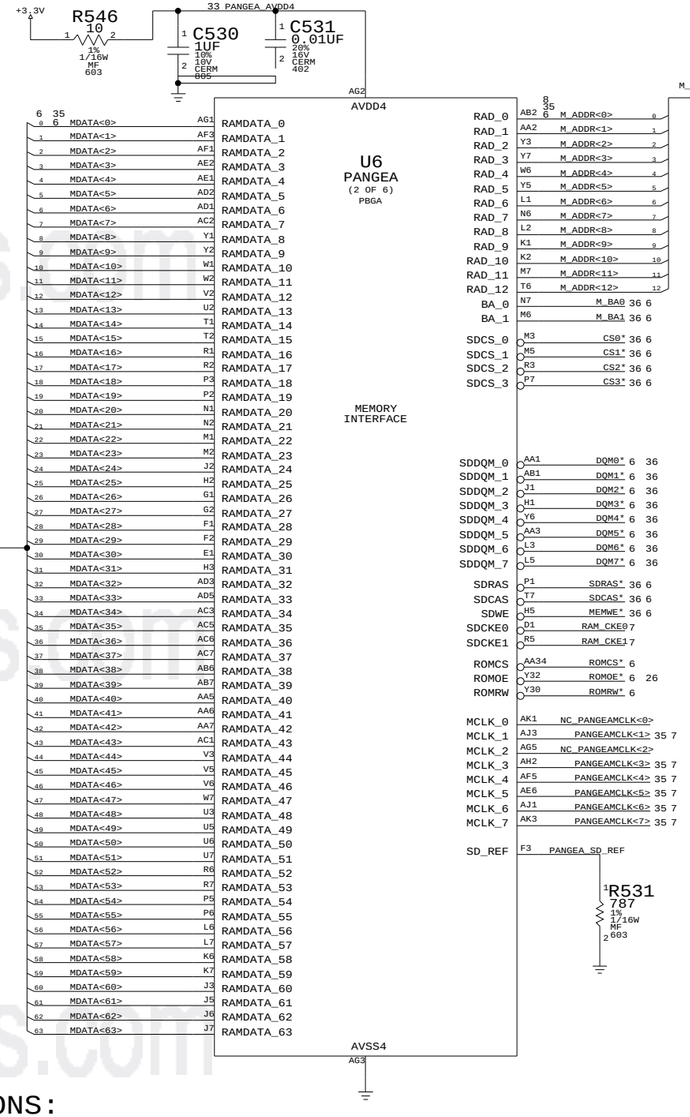
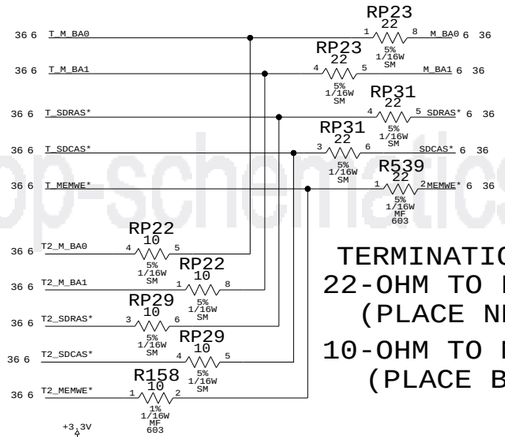
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S1006	1	CON,SKT,SODIMM,SDRAM,3.3V,144P,BLK	J21	PROJECT	







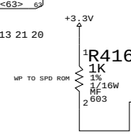


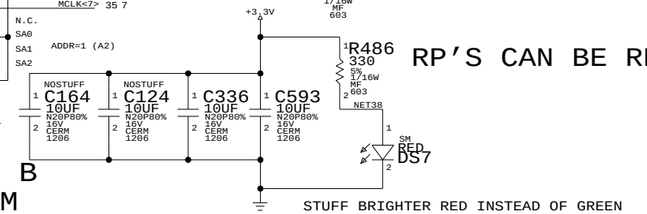


TERMINATIONS:
22-OHM TO FIRST DIMM
(PLACE NEAR FIRST DIMM)
10-OHM TO NEXT DIMM
(PLACE BETWEEN DIMMS)

CS0-3 ARE CRITICAL TIMING NETS
MAKE AS SHORT AS POSSIBLE
SPLIT NETS AT BGA, 10-OHM
SERIES TERM.

Pangea SDRAM IF & SDRAM DIMMs





RP'S CAN BE RE-PINNED WITHIN GROUP

STUFF BRIGHTER RED INSTEAD OF GREEN

516S1006

SO-DIMM A
FIRST DIMM

TERMINATIONS:
22-OHM TO FIRST DIMM
10-OHM TO NEXT DIMM

517-0782

PC100 DIMM B
SECOND DIMM

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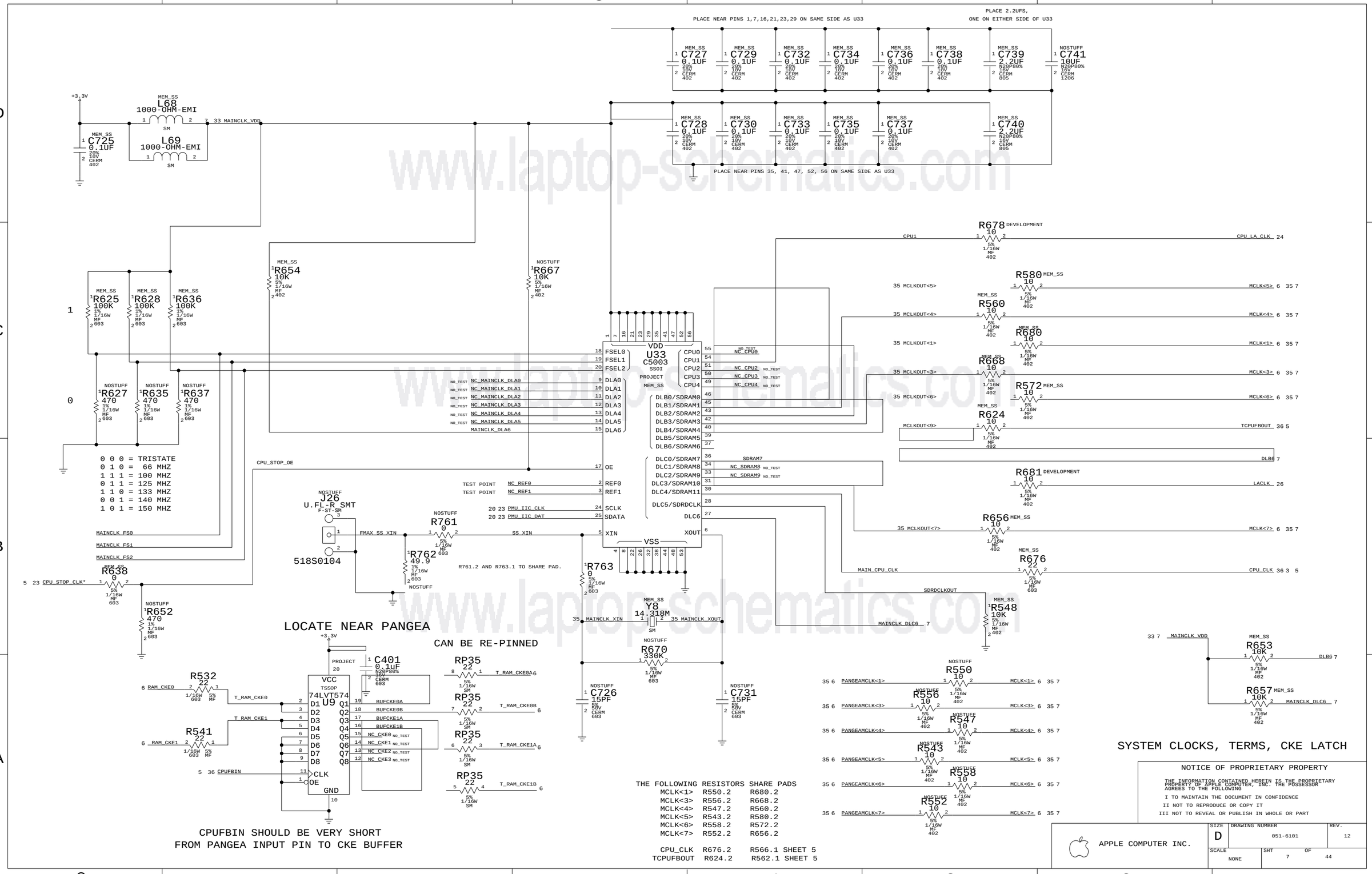

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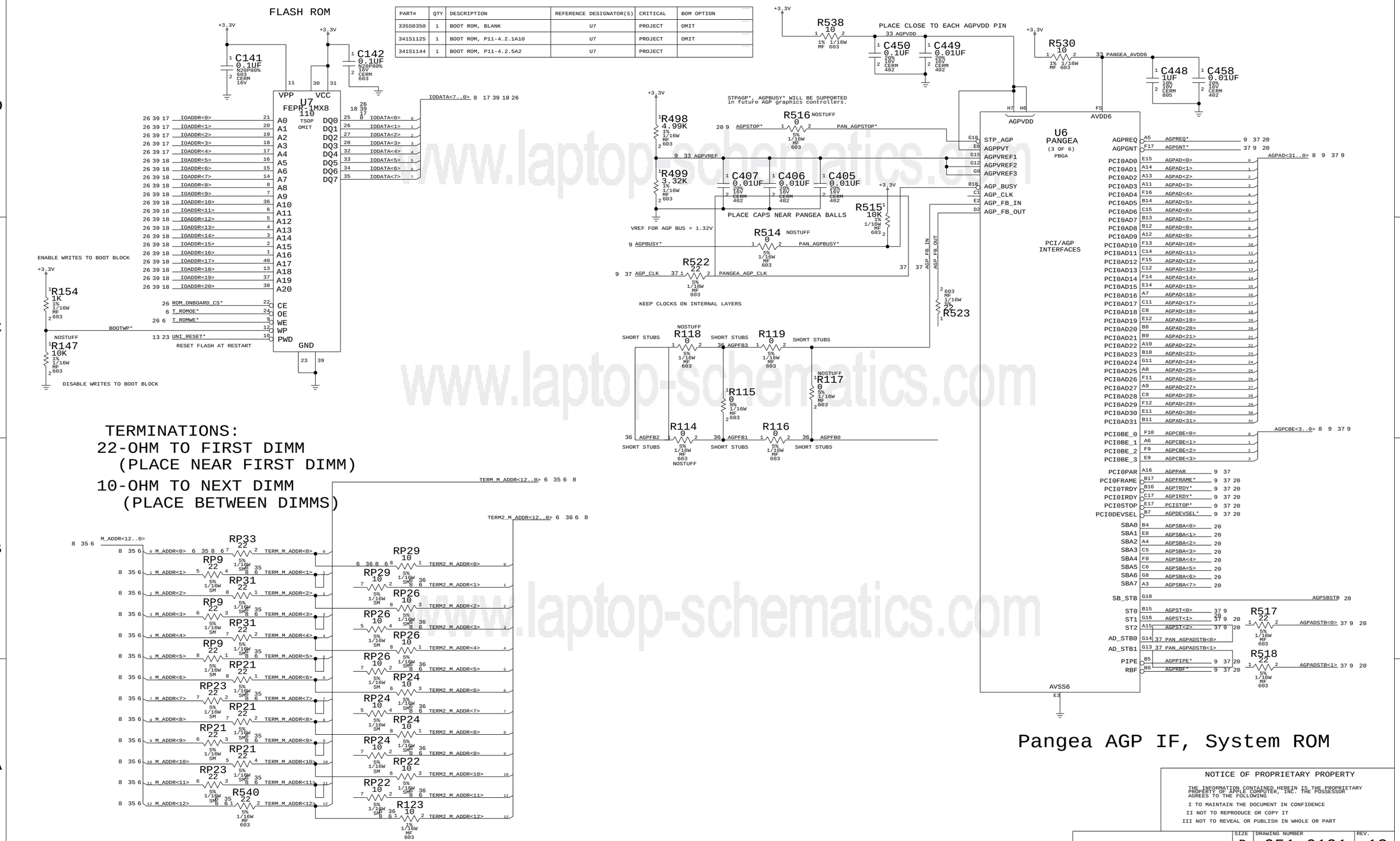
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
335S0350	1	BOOT ROM, BLANK	U7	PROJECT	OMIT
341S1125	1	BOOT ROM, P11-4.2.1A10	U7	PROJECT	OMIT
341S1144	1	BOOT ROM, P11-4.2.5A2	U7	PROJECT	



TERMINATIONS:
22-OHM TO FIRST DIMM
(PLACE NEAR FIRST DIMM)
10-OHM TO NEXT DIMM
(PLACE BETWEEN DIMMS)

Pangea AGP IF, System ROM

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GRAPHICS CONTROLLER - AGP AND VIDEO INTERFACES

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S0208	1	IC,MONICA GRAPHICS CTLR (A02)	U22	PROJECT	OMIT
338S0010	1	IC,MONICA GRAPHICS CTLR (B01)	U22	PROJECT	OMIT
338S0021	1	IC,MONICA GRAPHICS CTLR (B02)	U22	PROJECT	OMIT
338S0021	1	IC,MONICA GRAPHICS CTLR (B03)	U22	PROJECT	

The resistor to the left may be used instead of the regulator if there is a problem with resetting the TMDS xmtr in Monica.

Match lengths and route on internal layers: Nets INT_TMDS_XXX

<---- GPIODx initial conditions

ROUTE THE RGB LINES AS 75 OHM TRACES.

R404 AND R386 MUST be placed close to each other and pin AK7 of Monica.

All of the components to the right must be placed very close to the respective pins on the chip!

GRAPHICS CORE BYPASS (VDD)

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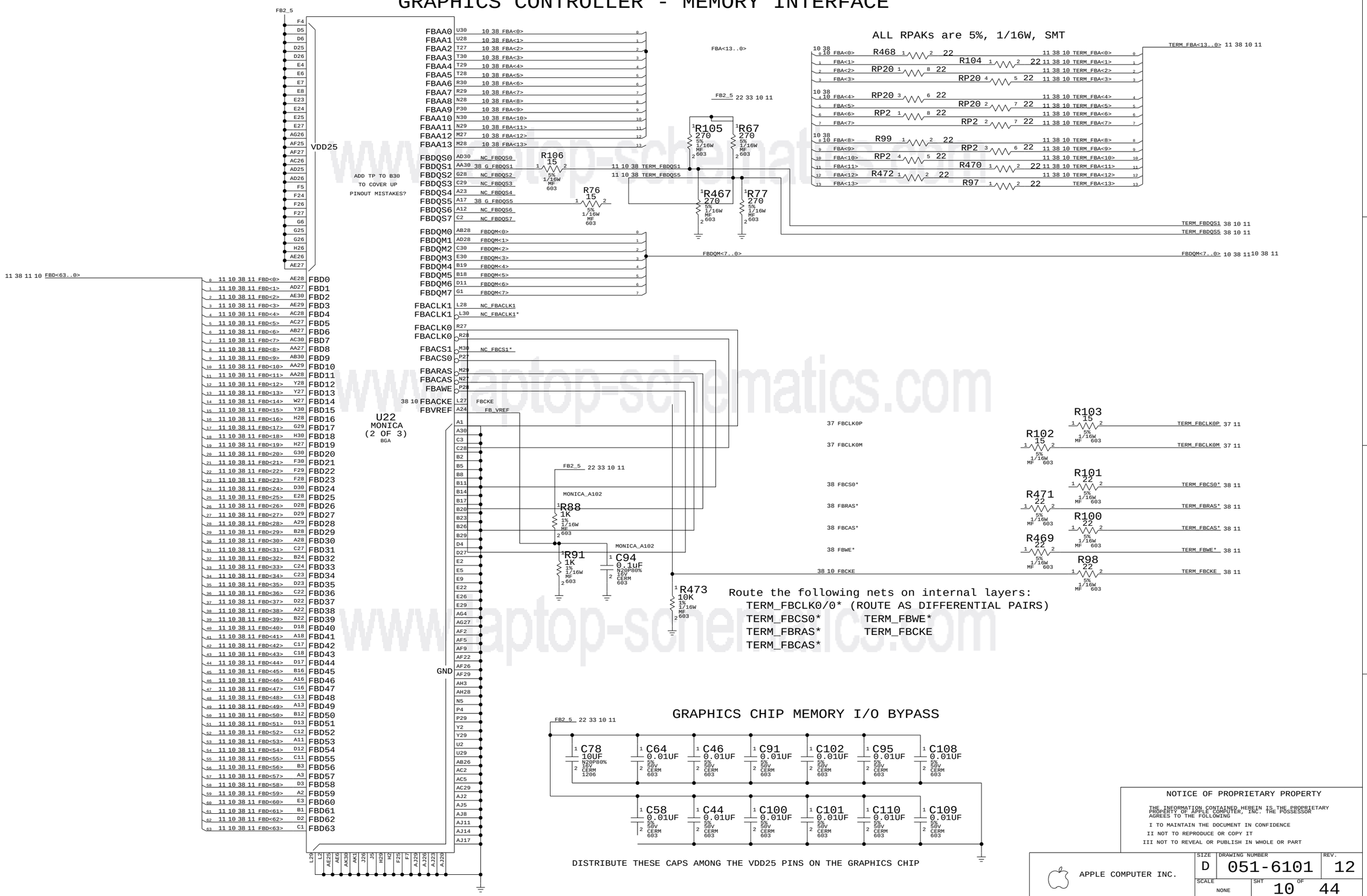
GRAPHICS CONTROLLER - MEMORY INTERFACE



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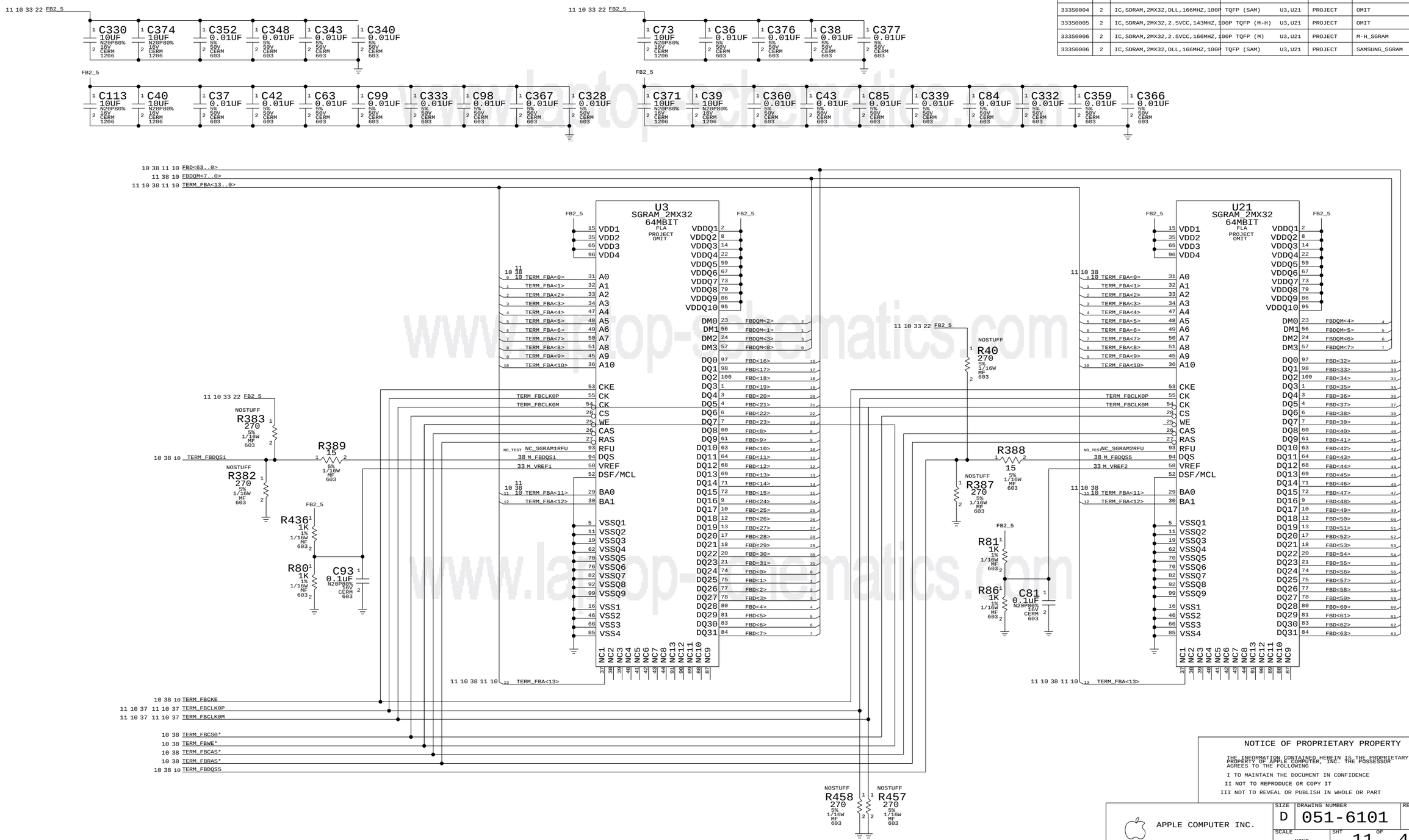
CR-11

GRAPHICS SDRAMS - 16/32 MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
333S0055	333S0006	SAMSUNG_SGRAM	U3,U21	2MX32,2.5VCC,183MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333S0075	2	IC,SGRAM,DDR,2MX32,125MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0076	2	IC,SGRAM,DDR,2MX32,143MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0077	2	IC,SGRAM,DDR,2MX32,166MHZ,100P TQFP, NO DLL	U3,U21	PROJECT	OMIT
333S0003	2	IC,SDRAM,2MX32,DLL,143MHZ,100P TQFP (SAM)	U3,U21	PROJECT	OMIT
333S0004	2	IC,SDRAM,2MX32,DLL,166MHZ,100P TQFP (SAM)	U3,U21	PROJECT	OMIT
333S0005	2	IC,SDRAM,2MX32,2.5VCC,143MHZ,100P TQFP (M-H)	U3,U21	PROJECT	OMIT
333S0006	2	IC,SDRAM,2MX32,2.5VCC,166MHZ,100P TQFP (M)	U3,U21	PROJECT	M-H_SGRAM
333S0006	2	IC,SDRAM,2MX32,DLL,166MHZ,100P TQFP (SAM)	U3,U21	PROJECT	SAMSUNG_SGRAM



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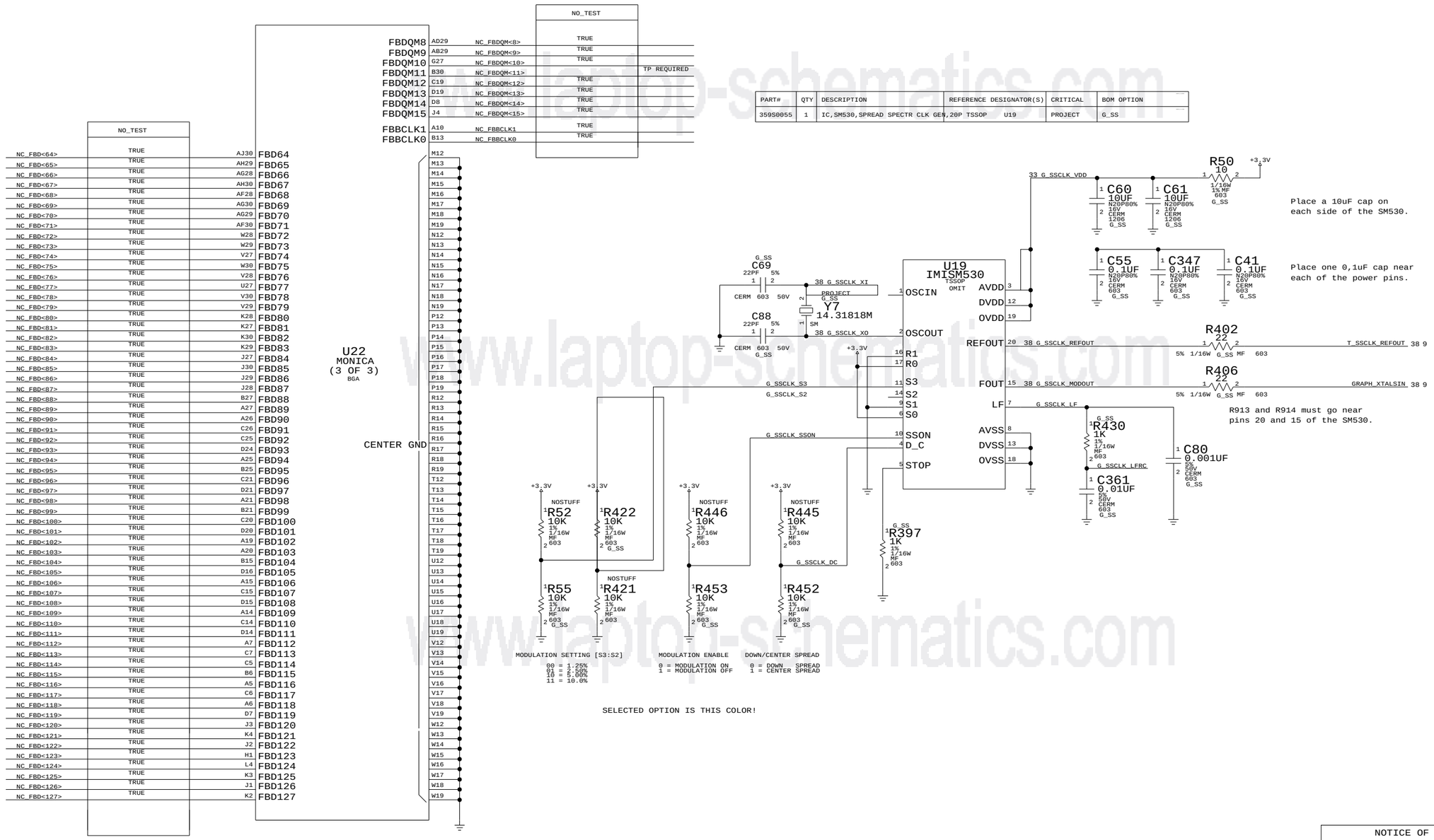
CR-12

GRAPHICS CHIP - UPPER 64-BIT DATA BUS & SUPPORT AND CENTER GROUND BALLS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0055	1	IC,SM530,SPREAD SPECTR CLK GEN,20P TSSOP	U19	PROJECT	G_SS

Place a 10uF cap on each side of the SM530.

Place one 0,1uF cap near each of the power pins.

R913 and R914 must go near pins 20 and 15 of the SM530.

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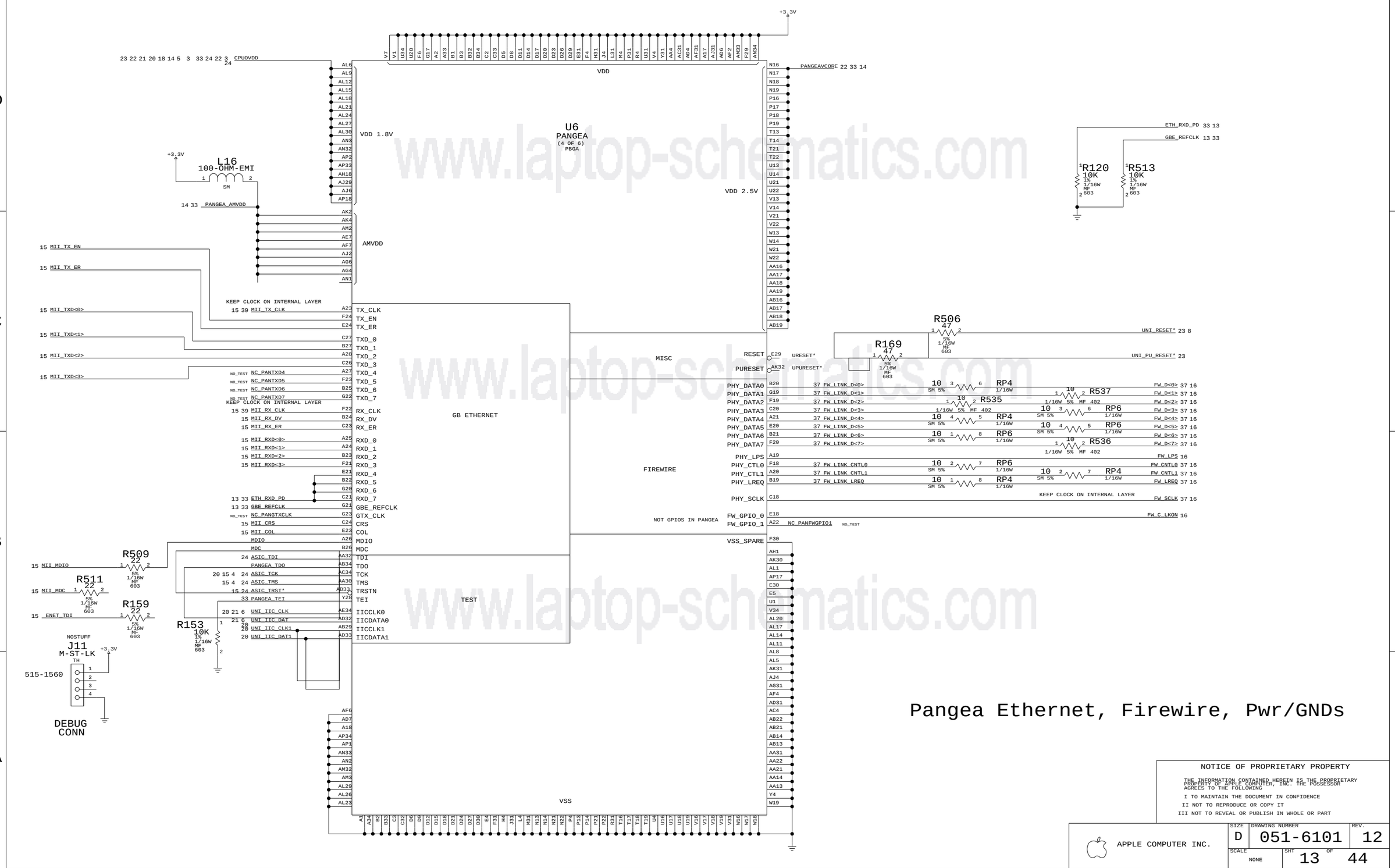

Pangea Ethernet, Firewire, Pwr/GNDs

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CR-14

PANGEA CORE BYPASS

13 33 22 PANGEAVCORE

C492 0.1UF, C478 0.1UF, C515 0.1UF, C485 0.1UF, C468 0.1UF, C506 0.1UF, C480 0.1UF, C517 0.1UF, C493 0.1UF, C486 0.1UF, C469 0.1UF, C505 0.01UF, C514 0.01UF, C499 0.01UF, C479 0.01UF, C472 0.01UF, C507 0.01UF, C481 0.01UF, C516 0.01UF, C500 0.01UF, C482 0.01UF, C473 0.01UF, C508 0.1UF, C483 0.01UF

C528 4.7UF, C465 4.7UF, C463 4.7UF, C462 4.7UF

C504 2.2UF, C474 2.2UF

PLACE AS NEAR AS CORE CENTER AS POSSIBLE

Pangea Processor I/F Bypass -- two per power/ground pair

18 13 5 3 33 24 22 3 24 23 22 21 20 CPUOVDD

C581 0.1UF, C557 0.1UF, C558 0.1UF, C559 0.1UF, C560 0.1UF, C561 0.1UF, C562 0.1UF, C563 0.1UF, C564 0.1UF, C565 0.1UF, C585 0.1UF, C580 0.01UF, C556 0.01UF, C546 0.01UF, C547 0.01UF, C548 0.01UF, C549 0.01UF, C550 0.01UF, C551 0.01UF, C552 0.01UF, C553 0.01UF, C583 0.01UF

C477 0.1UF, C509 0.01UF, C464 0.1UF, C520 0.01UF

Pangea I/O Ring Bypass -- two per power/ground pair

+3.3V

C484 0.1UF, C453 0.1UF, C567 0.1UF, C487 0.1UF, C415 0.1UF, C409 0.1UF, C410 0.1UF, C411 0.1UF, C421 0.1UF, C498 0.1UF, C436 0.1UF, C532 0.1UF, C518 0.1UF, C502 0.1UF, C489 0.1UF, C470 0.1UF, C460 0.1UF, C451 0.1UF, C541 0.1UF

C570 0.01UF, C584 0.1UF, C526 0.1UF, C578 0.01UF

+3.3V

C426 0.1UF, C427 0.1UF, C428 0.1UF, C429 0.1UF, C430 0.1UF, C431 0.1UF, C432 0.1UF, C433 0.1UF, C422 0.1UF, C447 0.1UF, C523 0.1UF, C511 0.1UF, C496 0.1UF, C476 0.1UF, C467 0.1UF, C456 0.1UF, C494 0.1UF, C424 0.1UF, C420 0.01UF

C527 0.01UF, C538 0.01UF, C566 0.01UF, C571 0.1UF

C573 2.2UF, C574 2.2UF, C575 2.2UF, C576 2.2UF

PLACE AT EDGES OF PROC I/F PLANE

+3.3V

C488 0.01UF, C416 0.01UF, C412 0.01UF, C425 0.01UF, C417 0.01UF, C569 0.01UF, C437 0.01UF, C533 0.01UF, C519 0.01UF, C503 0.01UF, C490 0.01UF, C471 0.01UF, C461 0.01UF, C452 0.01UF, C438 0.01UF, C439 0.01UF, C440 0.01UF, C441 0.01UF, C442 0.01UF

+3.3V

C443 0.01UF, C444 0.01UF, C445 0.01UF, C434 0.01UF, C446 0.01UF, C522 0.01UF, C510 0.01UF, C495 0.01UF, C475 0.01UF, C466 0.01UF, C455 0.01UF, C454 0.01UF, C501 0.01UF, C497 0.01UF, C542 0.01UF, C413 0.01UF, C568 0.01UF, C423 0.01UF, C414 0.01UF, C491 0.01UF

Pangea AMVDD Bypass (one pair per pin)

13 33 PANGEA_AMVDD

C535 0.1UF, C525 0.1UF, C537 0.1UF, C544 0.1UF, C545 0.01UF, C572 0.01UF

C529 0.01UF, C521 0.01UF, C536 0.01UF, C543 0.01UF, C554 0.1UF, C539 0.1UF, C579 0.1UF

+3.3V

C513 2.2UF, C459 2.2UF, C419 2.2UF, C418 2.2UF, C457 2.2UF, C512 2.2UF

PLACE ALONG OUTSIDE OF BALL GRID ALONG 3 NON-MAXBUS MAXBUS SIDES (2 PER)

Pangea Bypass

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D	051-6101	12
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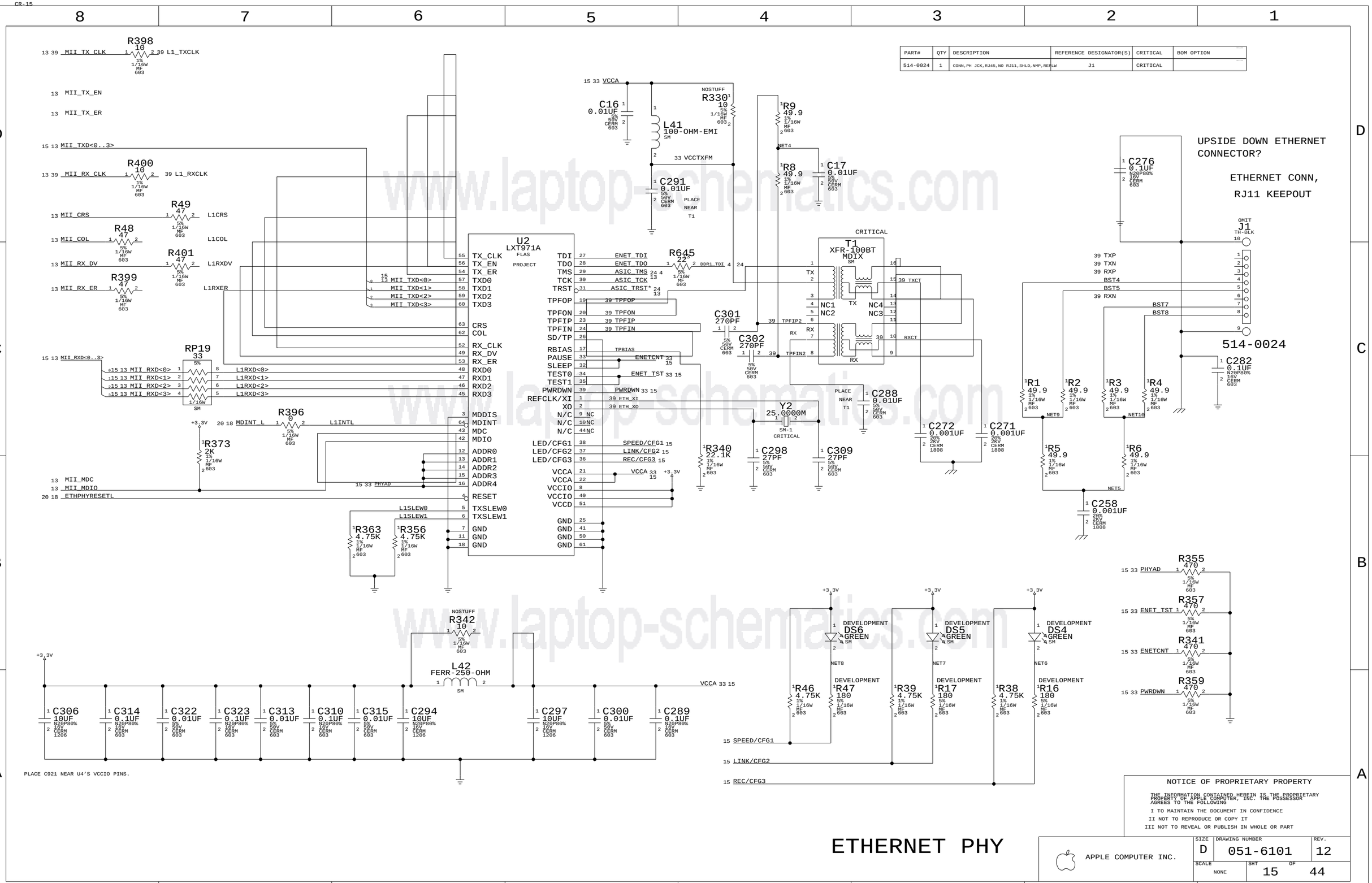

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0024	1	CONN,PH JCK,RJ45,NO RJ11,SHLD,NMP,REFLW	J1	CRITICAL	

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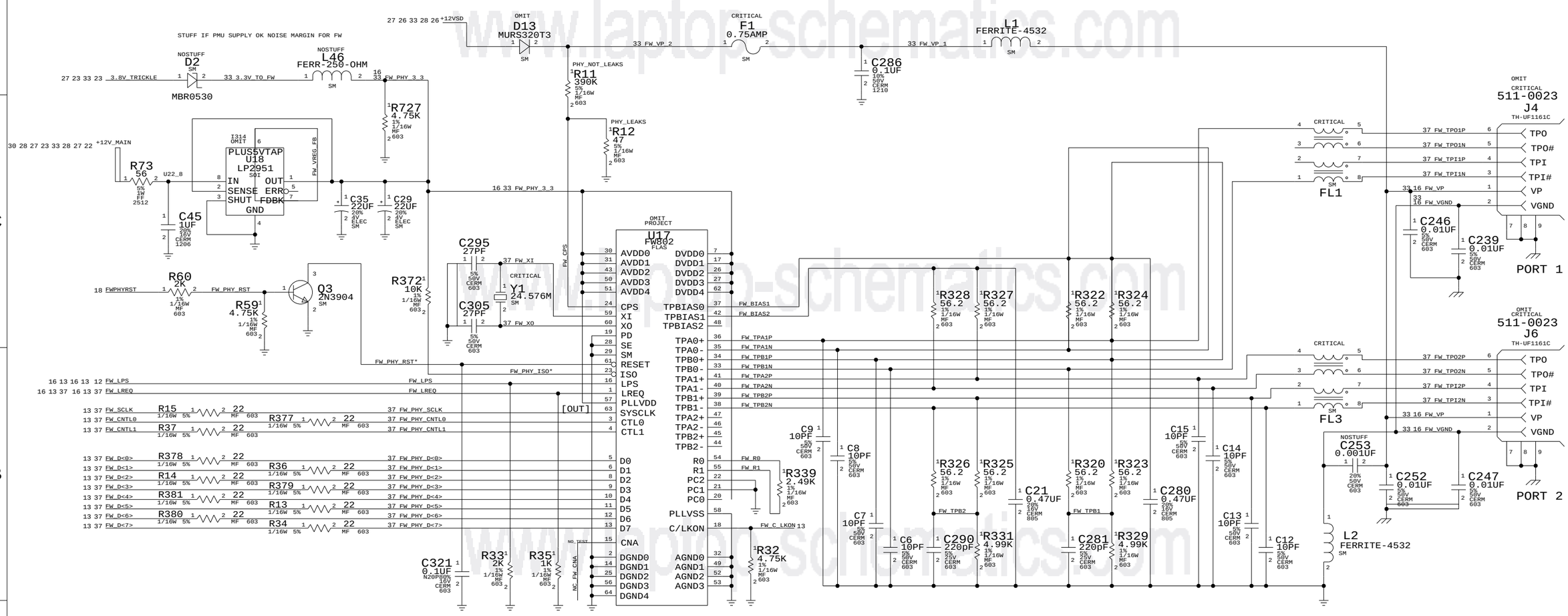
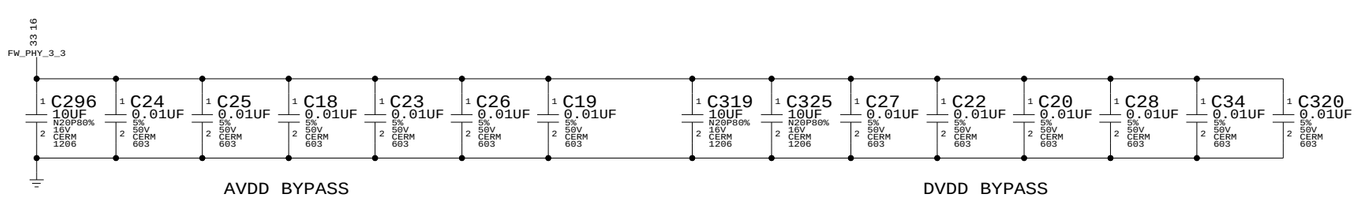
CR-16

Firewire PHY and Termination

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0018	1	FLAS-64W431-H63,2PORT FW PHY,FW802A	REV A U17	PROJECT	
337S0509	1	FLAS-64W431-H63,2PORT FW PHY,FW802	REV 9 U17	PROJECT	OMIT
371S0058	1	DIODE,FAST RECOVERY,200V,3A,SMD	D13		
353S0094	1	5V FIXED/ADJ VREG, SOI-8	U18	PROJECT	OMIT
353S0275	1	3.3V FIXED/ADJ VREG, SOI-8	U18	PROJECT	
514-0023	2	CONN,RCPT,R/A,1394,NOFLANGES,NMP,6P	J4,J6	CRITICAL	



Firewire PHY



AVDD BYPASS

DVDD BYPASS

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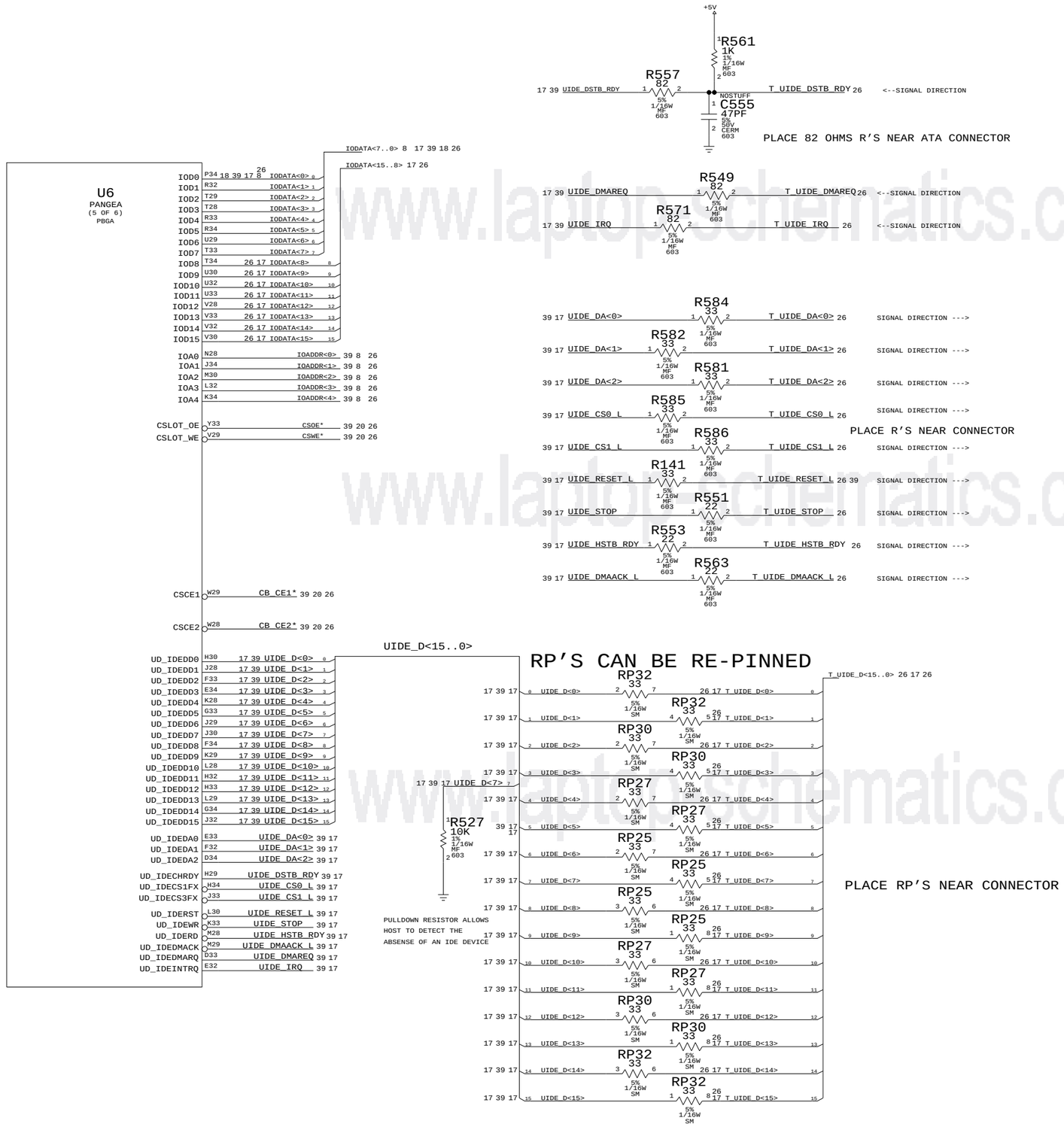

PANGEA ATA, & PCMCIA BUS

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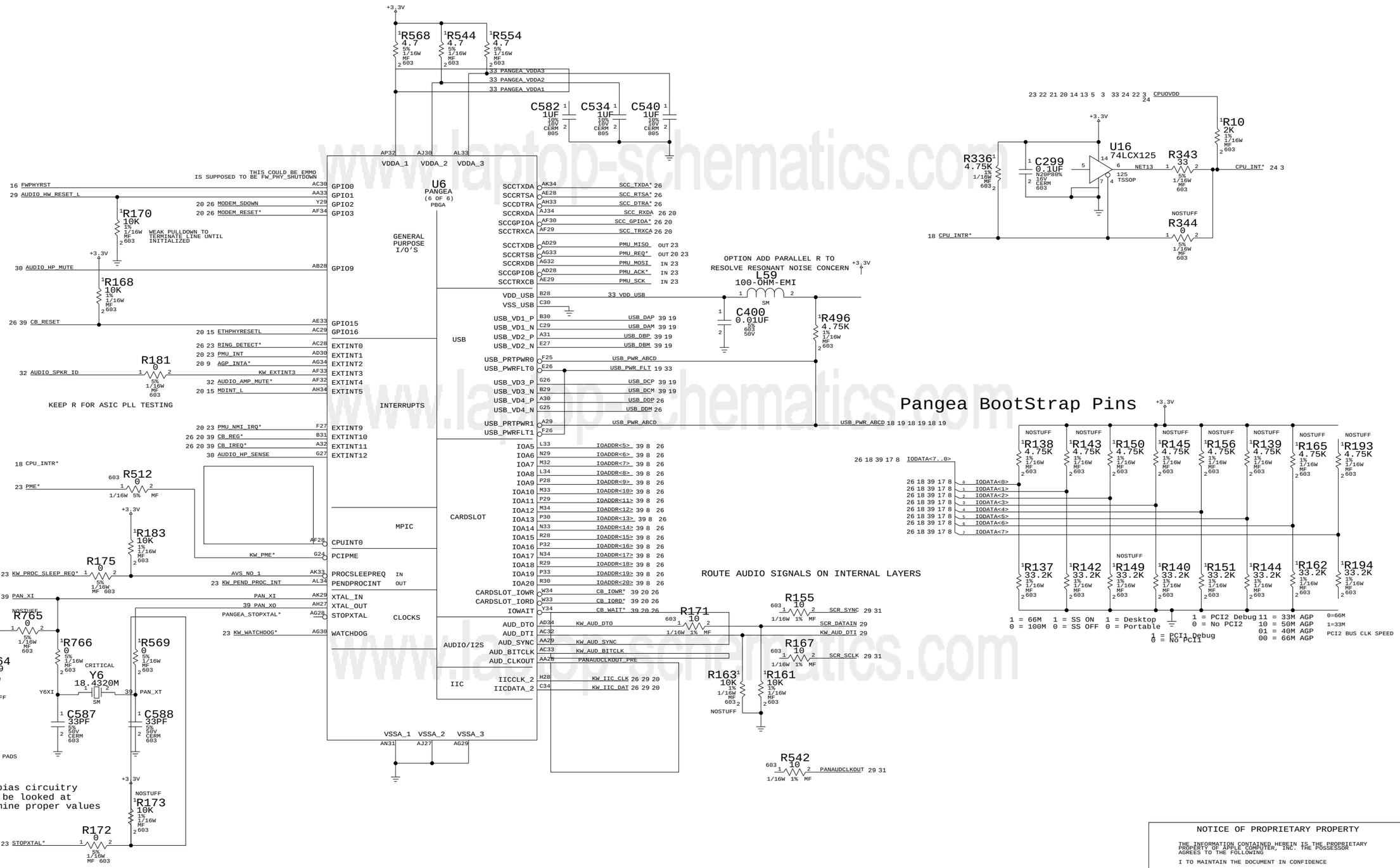

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PANGEA SER/AUD/USB, BOOTSTRAPS

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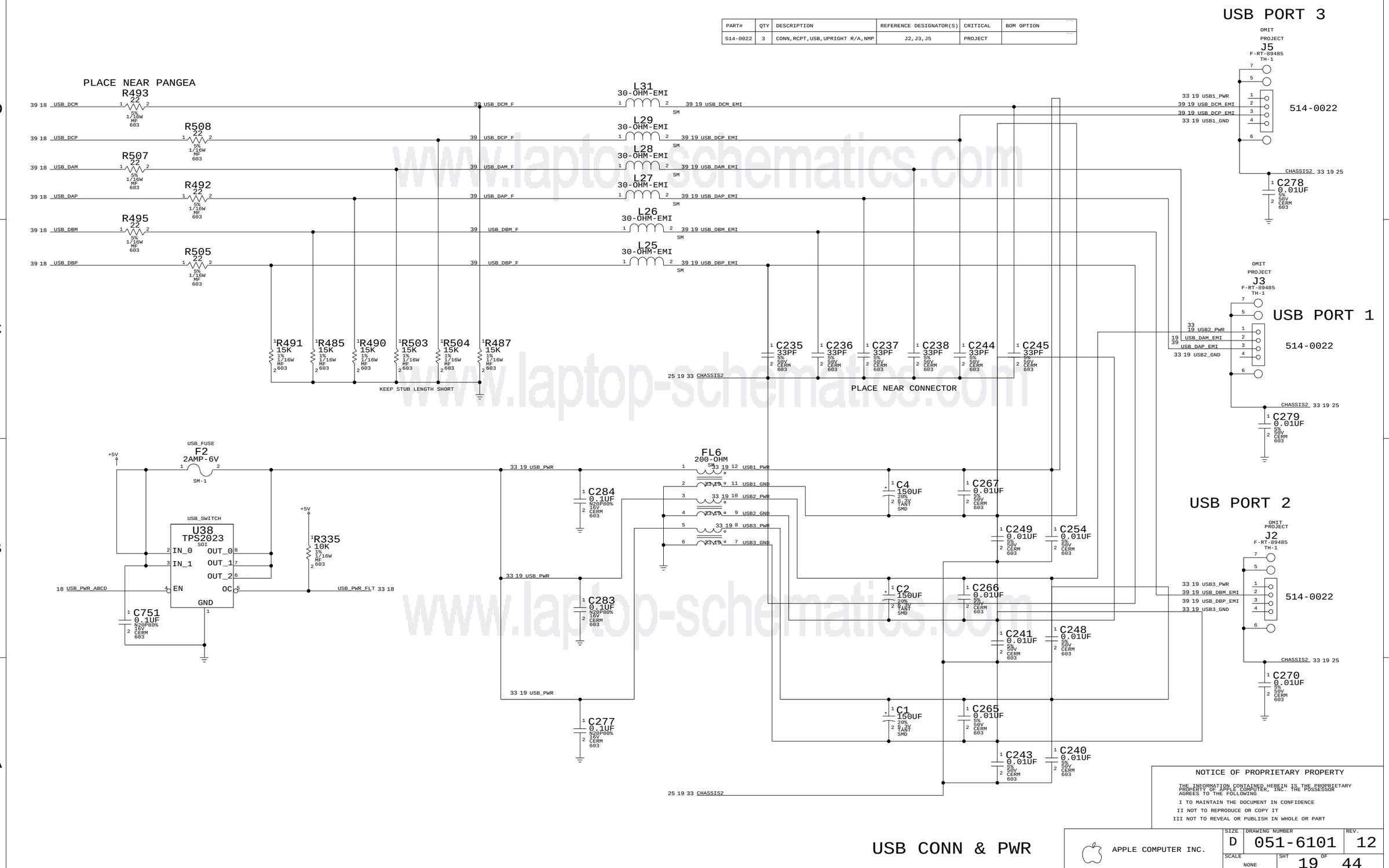
CR-19

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0022	3	CONN,RCPT,USB,UPRIGHT R/A,NMP	J2,J3,J5	PROJECT	



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USB CONN & PWR

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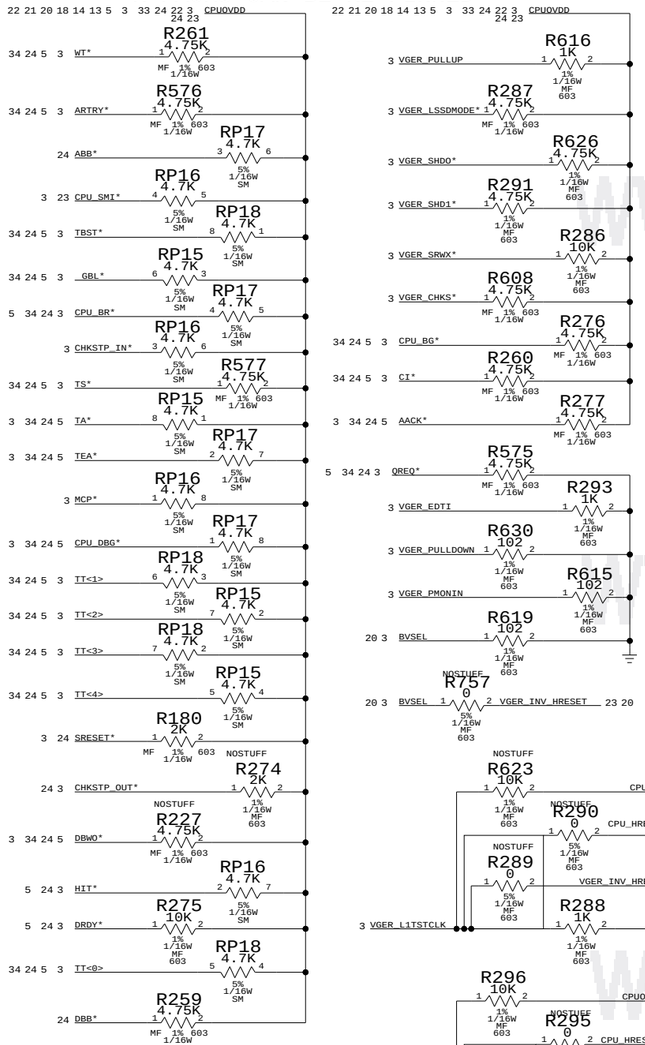
CR-20

PROCESSOR PULLUP/PULLDOWN

R-PACKS CAN BE RE-PINNED



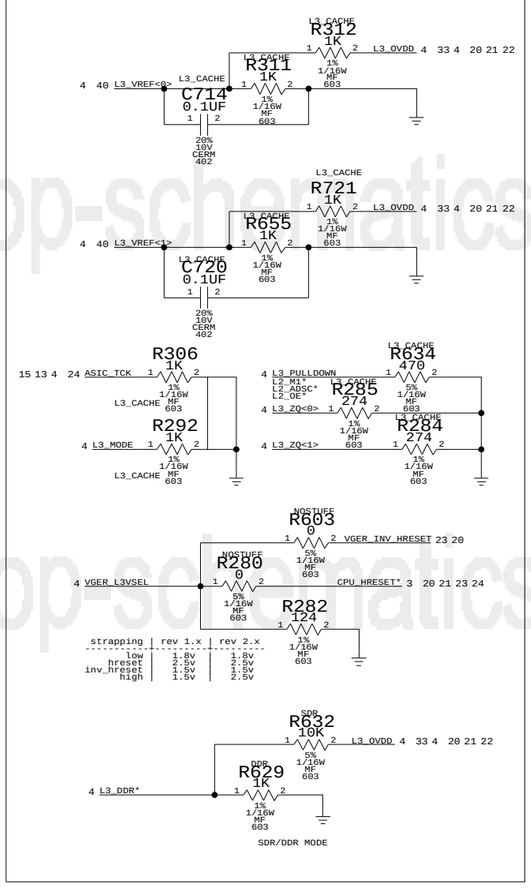
BUS MODE
R619 STUFFED 1.8V BUS MODE
R757 STUFFED 1.5V BUS MODE

RP14 NEEDS TO BE STUFFED ALL THE TIME

NO NOBUSKEEPER PROPERTY ON RP14

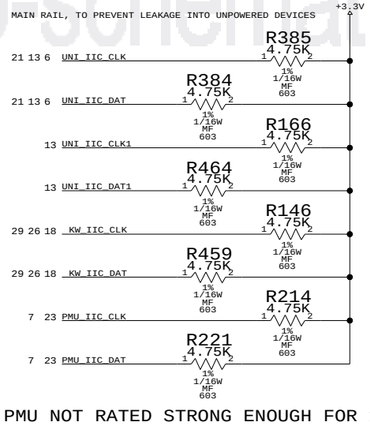
BMODE <0>	BMODE <1>	MSSCR0 <16:17>	Sys Bus	Vger ID	Addr Drve
L	L	1 1	???	01	yes unavail
L	!hr	1 0	Max	01	yes unavail
L	hr	1 1	???	00	yes unavail
L	H	1 0	Max	00	yes unavail
!hr	L	0 1	MB+	01	yes unavail
!hr	!hr	0 0	60x	01	yes unavail
!hr	hr	0 1	MB+	00	yes unavail
!hr	H	0 0	60x	00	yes unavail
hr	L	1 1	???	01	norm unavail
hr	!hr	1 0	Max	01	norm
hr	hr	1 1	???	00	norm unavail
hr	H	1 0	Max	00	norm <----STUFF FOR THIS LINE
H	L	0 1	MB+	01	norm unavail
H	!hr	0 0	60x	01	norm
H	hr	0 1	MB+	00	norm unavail
H	H	0 0	60x	00	norm

L3 CACHE PULLUP/PULLDOWN



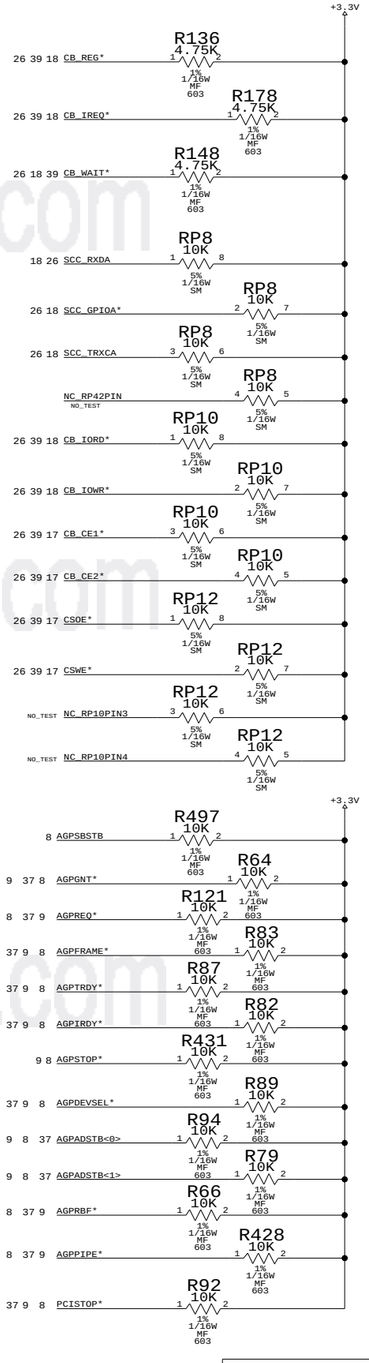
strapping	rev 1.x	rev 2.x
low	1.8v	1.8v
hreset	2.5v	2.5v
inv_hreset	1.5v	1.5v
high	1.5v	2.5v

IIC BUS PULLUPS



PMU NOT RATED STRONG ENOUGH FOR 1K

PANGEA PULLUPS



MLB Pull-ups

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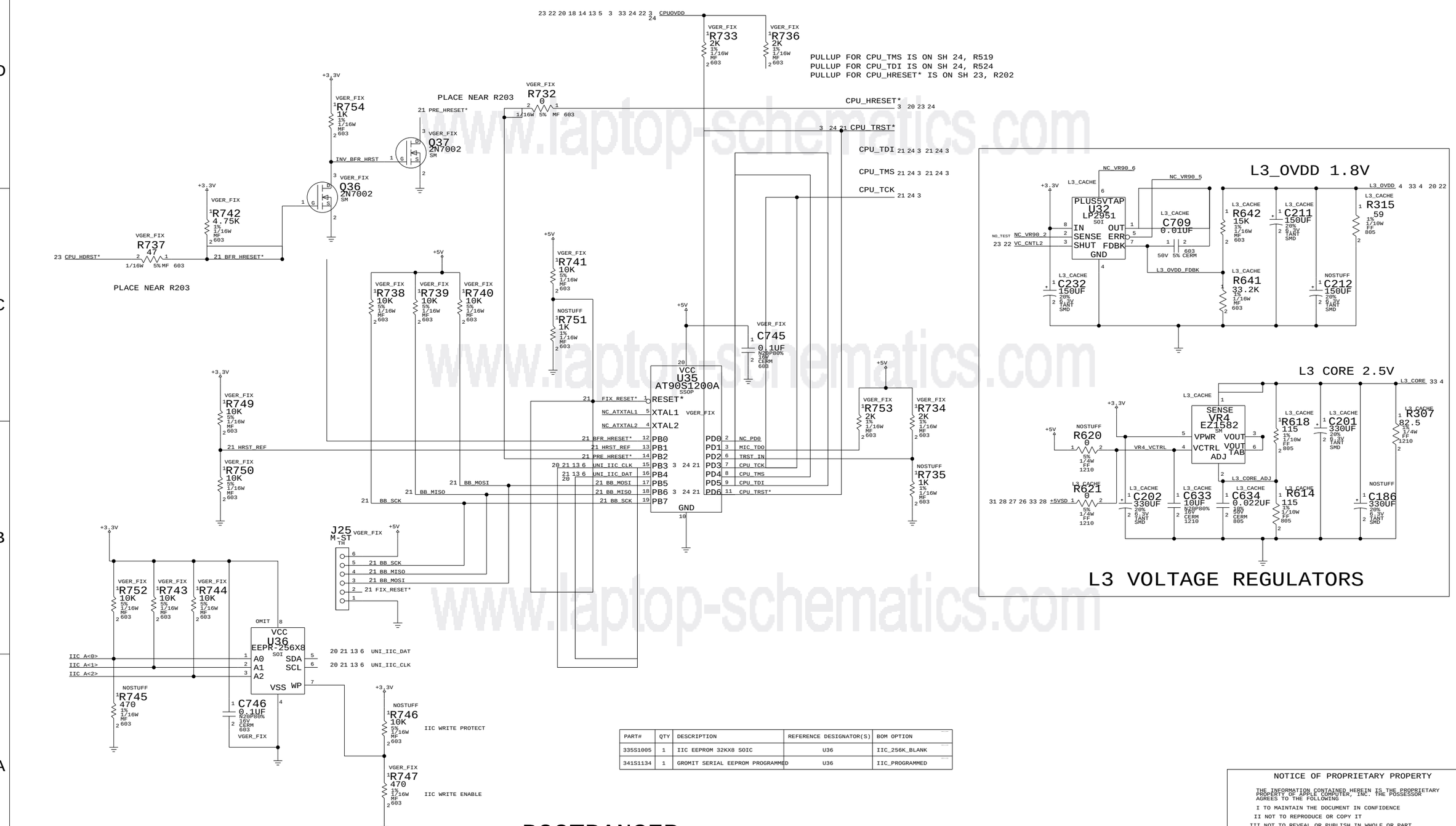

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
335S1005	1	IIC EEPROM 32KX8 SOIC	U36	IIC_256K_BLANK
341S1134	1	GROMIT SERIAL EEPROM PROGRAMMED	U36	IIC_PROGRAMMED

BOOTBANGER

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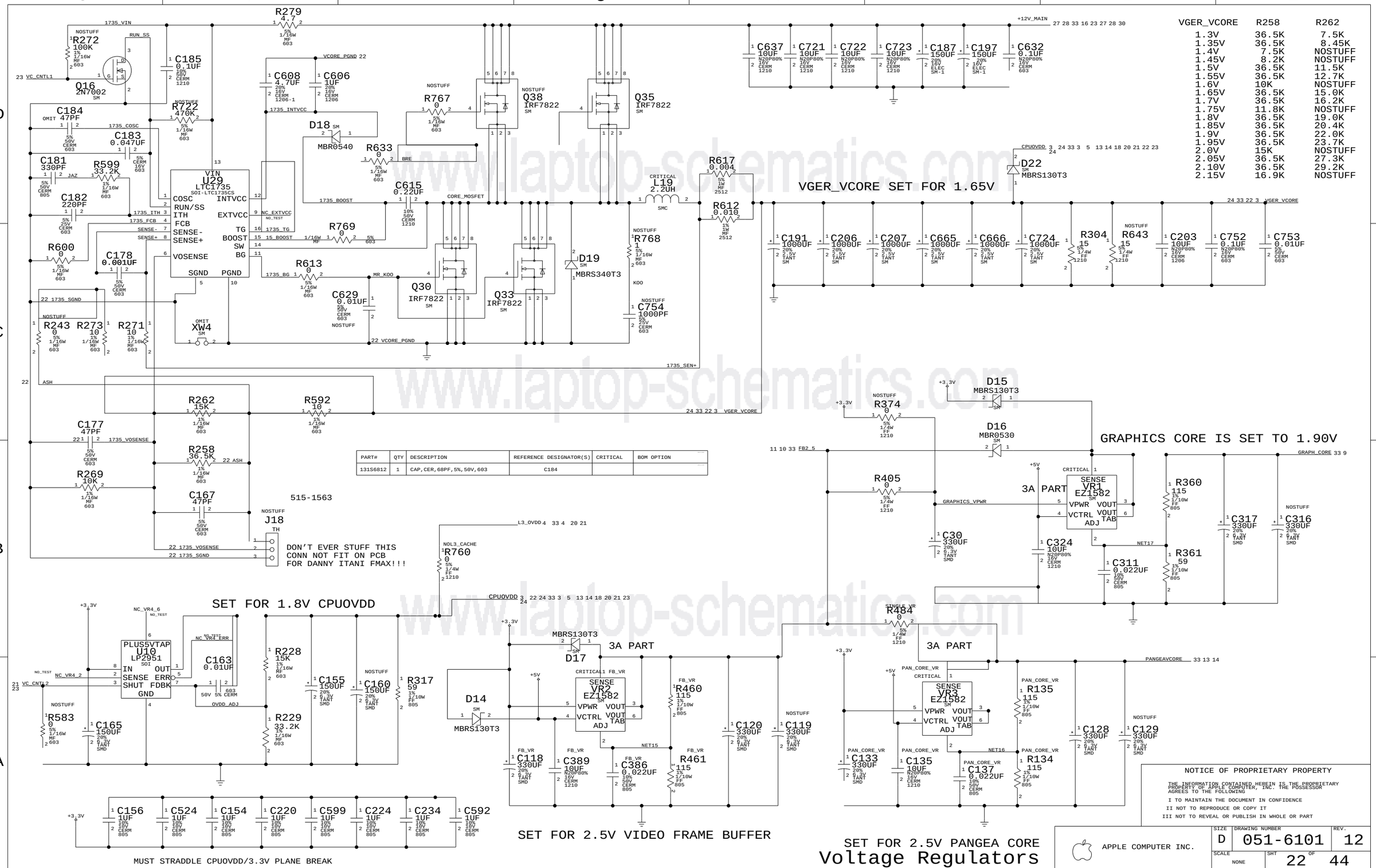

VGER_VCORE	R258	R262
1.3V	36.5K	7.5K
1.35V	36.5K	8.45K
1.4V	7.5K	NOSTUFF
1.45V	8.2K	NOSTUFF
1.5V	36.5K	11.5K
1.55V	36.5K	12.7K
1.6V	10K	NOSTUFF
1.65V	36.5K	15.0K
1.7V	36.5K	16.2K
1.75V	11.8K	NOSTUFF
1.8V	36.5K	19.0K
1.85V	36.5K	20.4K
1.9V	36.5K	22.0K
1.95V	36.5K	23.7K
2.0V	15K	NOSTUFF
2.05V	36.5K	27.3K
2.10V	36.5K	29.2K
2.15V	16.9K	NOSTUFF

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
131S6812	1	CAP,CER,68PF,5%,50V,603	C184		

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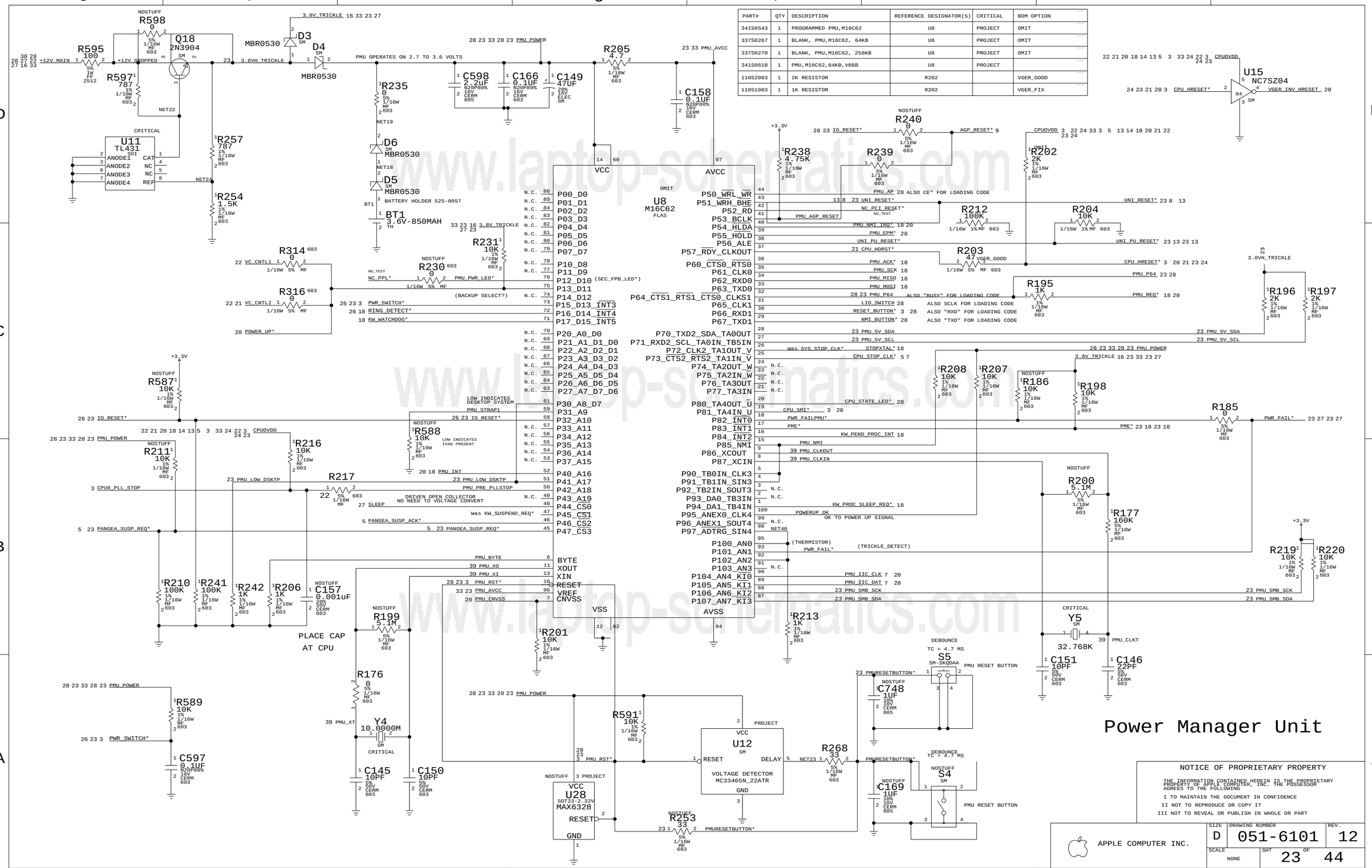
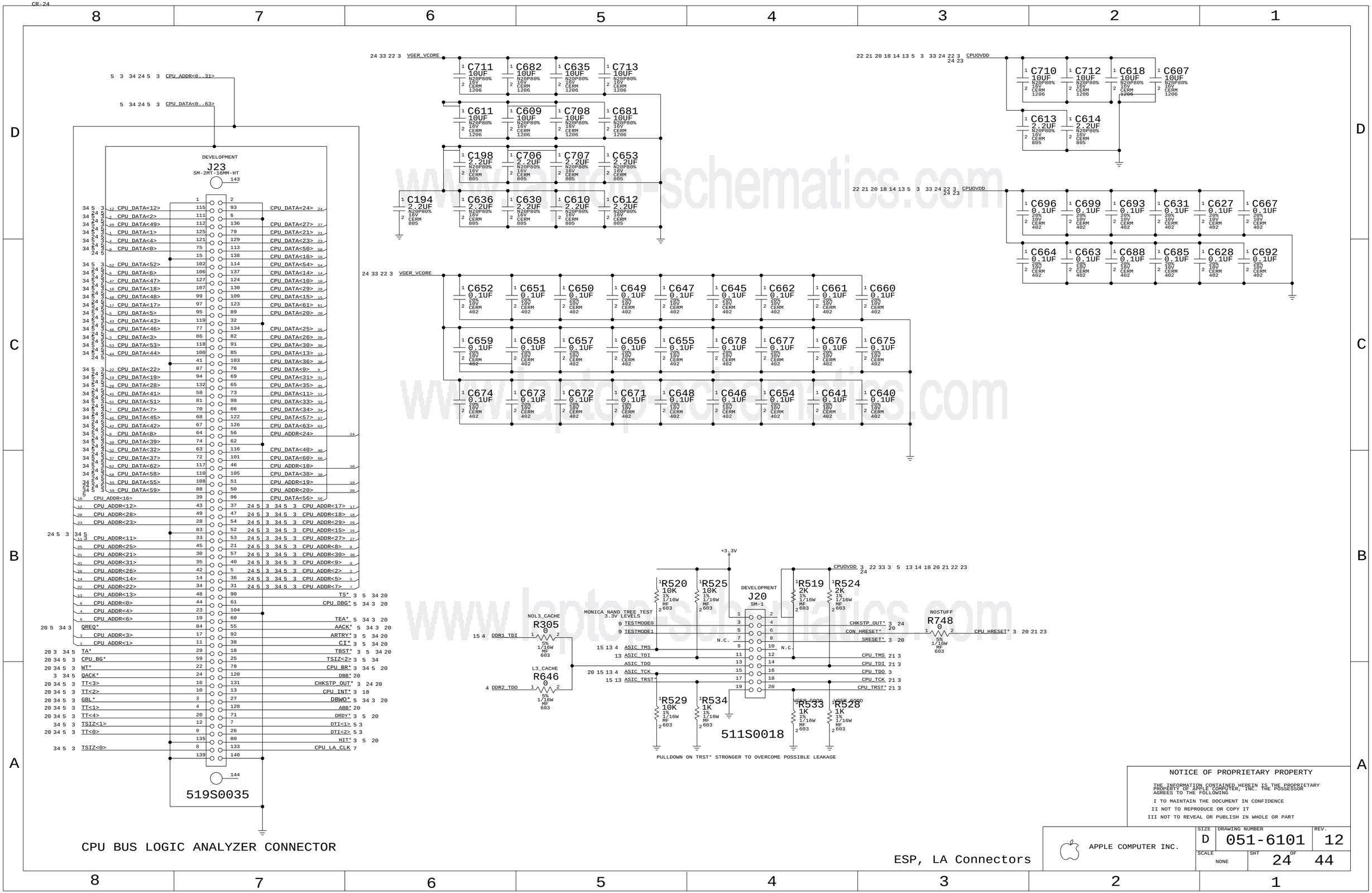
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S0543	1	PROGRAMMED PMU,M16C62	U8	PROJECT	OMIT
337S0267	1	BLANK, PMU,M16C62, 64KB	U8	PROJECT	OMIT
337S0270	1	BLANK, PMU,M16C62, 256KB	U8	PROJECT	OMIT
341S0618	1	PMU,M16C62,64KB,V66B	U8	PROJECT	
110S2003	1	2K RESISTOR	R202		VGER_GOOD
110S1003	1	1K RESISTOR	R202		VGER_FIX





CPU BUS LOGIC ANALYZER CONNECTOR

ESP, LA Connectors

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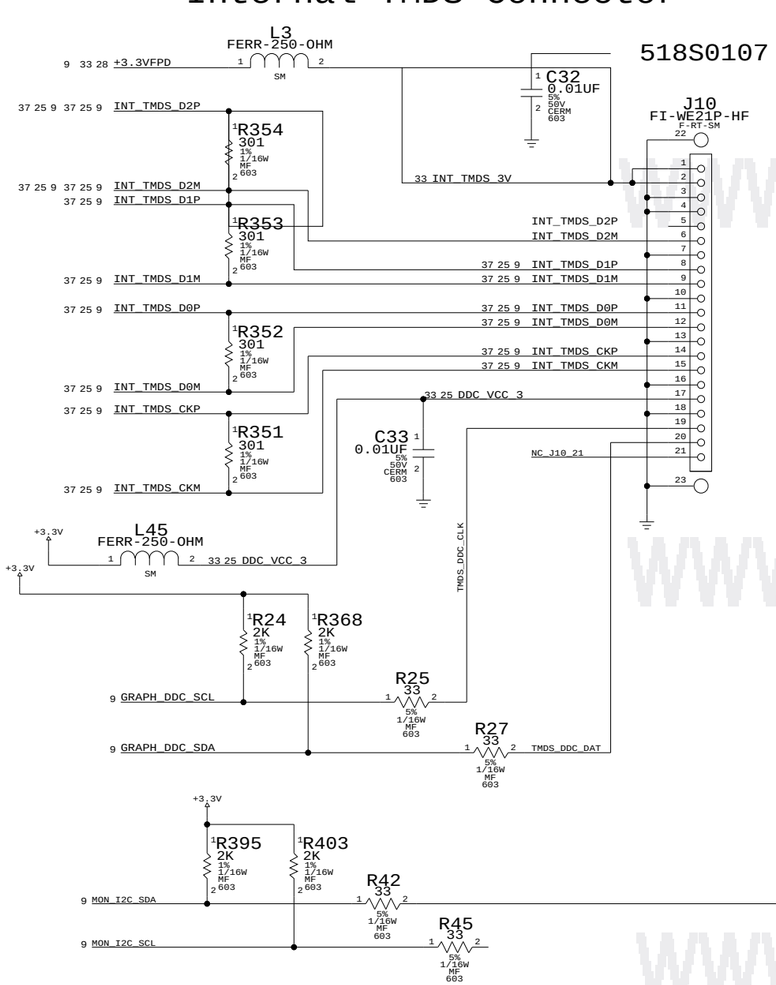
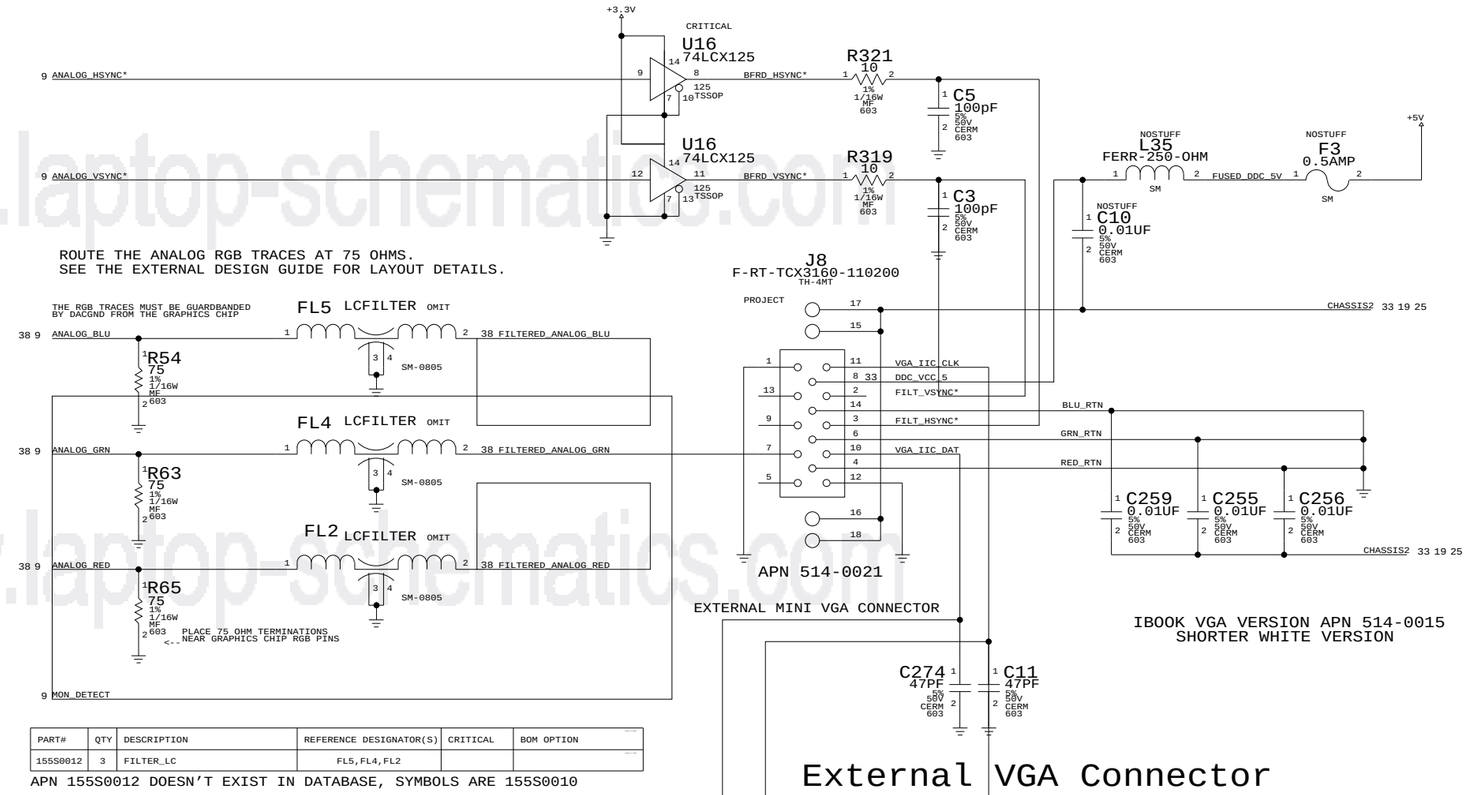
INTERNAL TMDS CONNECTOR, EXTERNAL VGA CONNECTOR AND GRAPHICS CHIP STRAP OPTIONS

Internal TMDS Connector





PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
155S0012	3	FILTER_LC	FL5,FL4,FL2		

APN 155S0012 DOESN'T EXIST IN DATABASE, SYMBOLS ARE 155S0010

External VGA Connector

SELECTED OPTION IS THIS COLOR!

TVD[10]
0 = SBA ENABLED
1 = PIPELINED XFERS ONLY

TVD[9]
0 = AGP 4X ENABLED
1 = AGP 2X ONLY

TVD[5:2]
0010 = 1M X 32 SDR SGRAM
1001 = 2M X 32 DDR SGRAM
1011 = 1M X 32 DDR SGRAM

DFPD[2:1]
00 = PCI_DEV_ID 0X0110

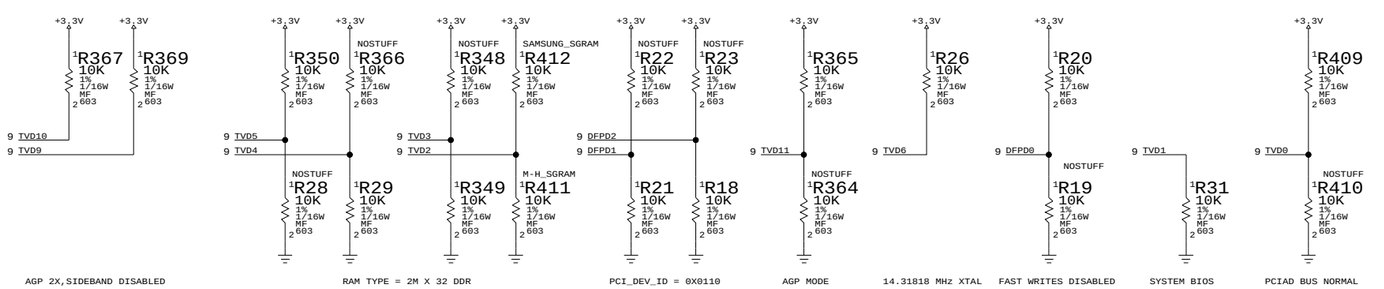
TVD[11]
0 = PCI MODE
1 = AGP MODE

TVD[6]
0 = 13.50000 MHZ
1 = 14.31818 MHZ

DFPD[0]
0 = FW ENABLED
1 = FW DISABLED

TVD[1]
0 = SYSTEM BIOS
1 = ADAPTOR BIOS

TVD[0]
0 = PCIAD BUS SWAPPED
1 = PCIAD BUS NORMAL



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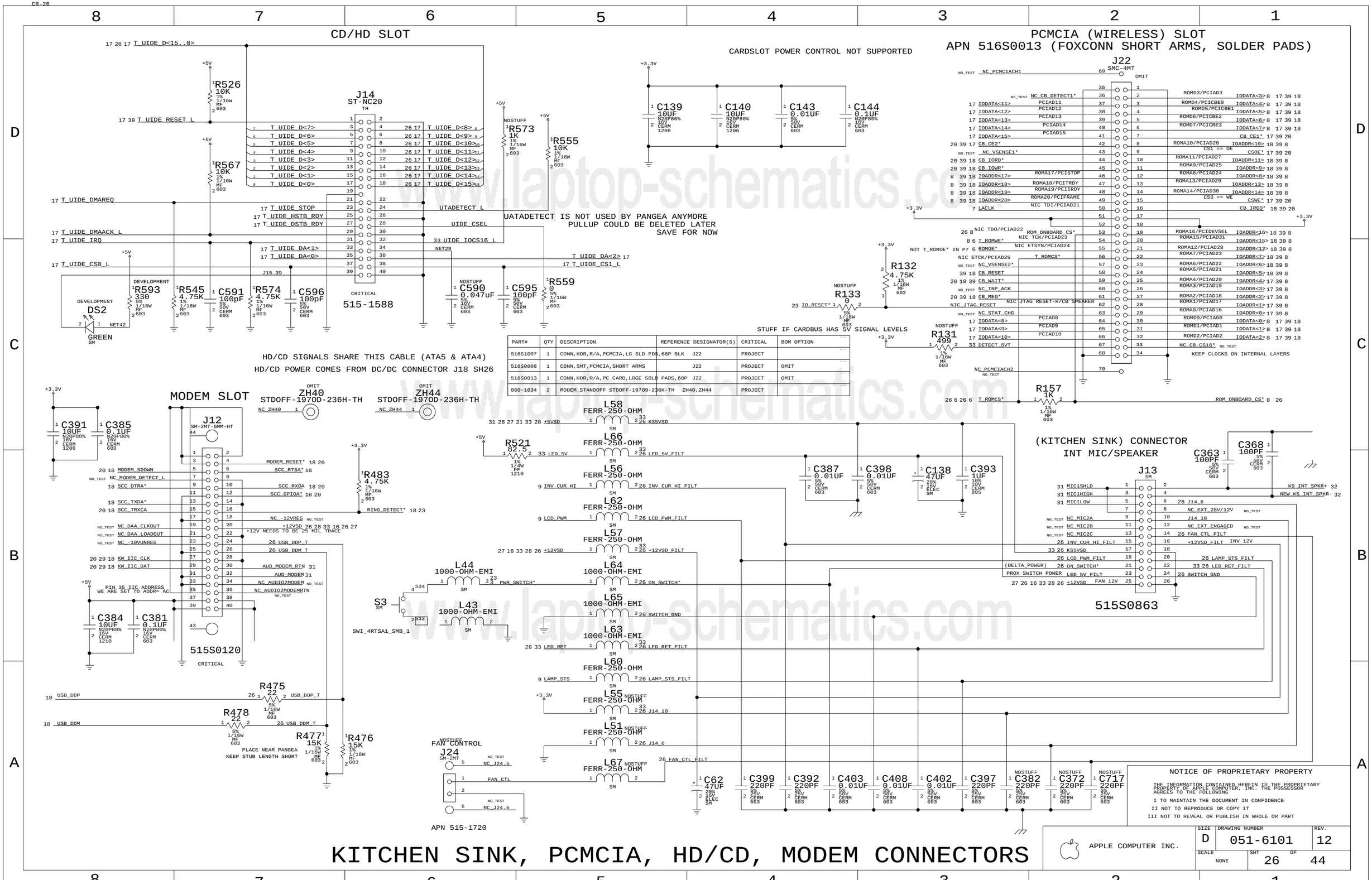

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
516S1007	1	CONN,HDR,R/A,PCMCIA,LG SLD PDS,68P BLK	J22	PROJECT	
516S0008	1	CONN,SMT,PCMCIA,SHORT ARMS	J22	PROJECT	OMIT
516S0013	1	CONN,HDR,R/A,PC CARD,LRGE SOLD PADS,68P	J22	PROJECT	OMIT
860-1034	2	MODEM_STANDOFF STDOFF-19709-236H-TH	ZH40,ZH44	PROJECT	

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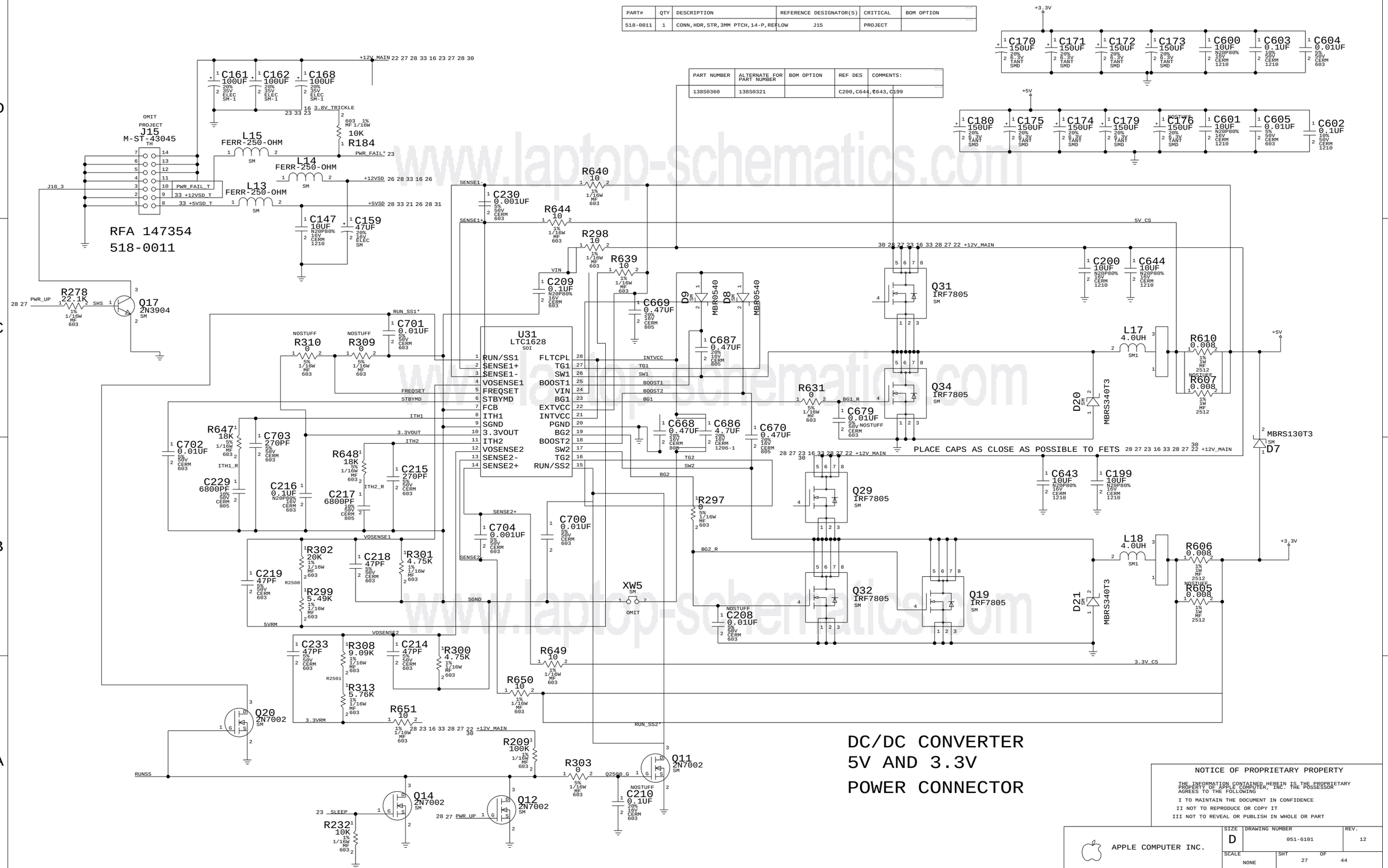
CR-27

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
518-0011	1	CONN,HDR,STR,3MM PTCH,14-P,REFLOW	J15	PROJECT	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0360	138S0321		C200,C644,C643,C199	



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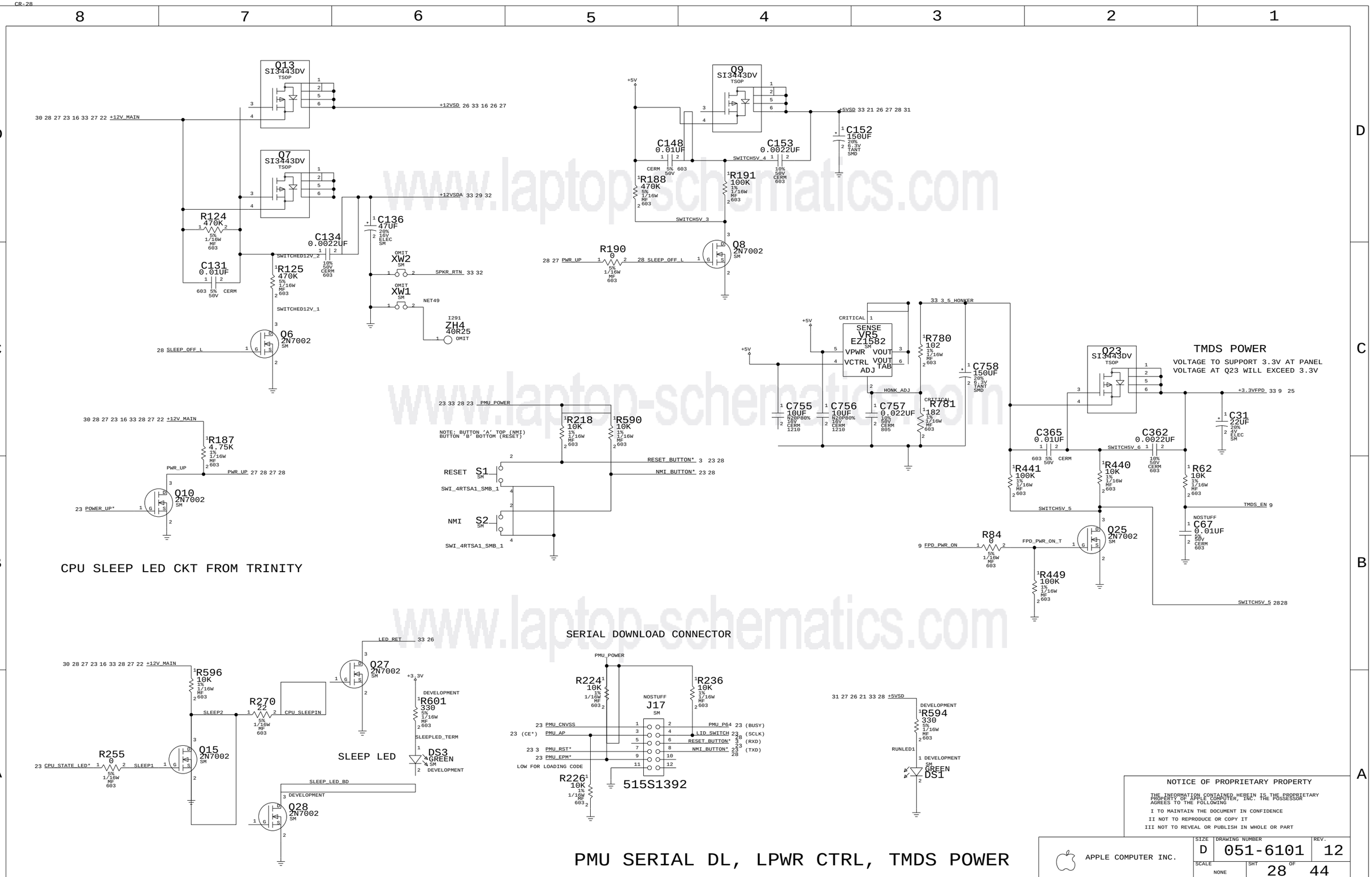

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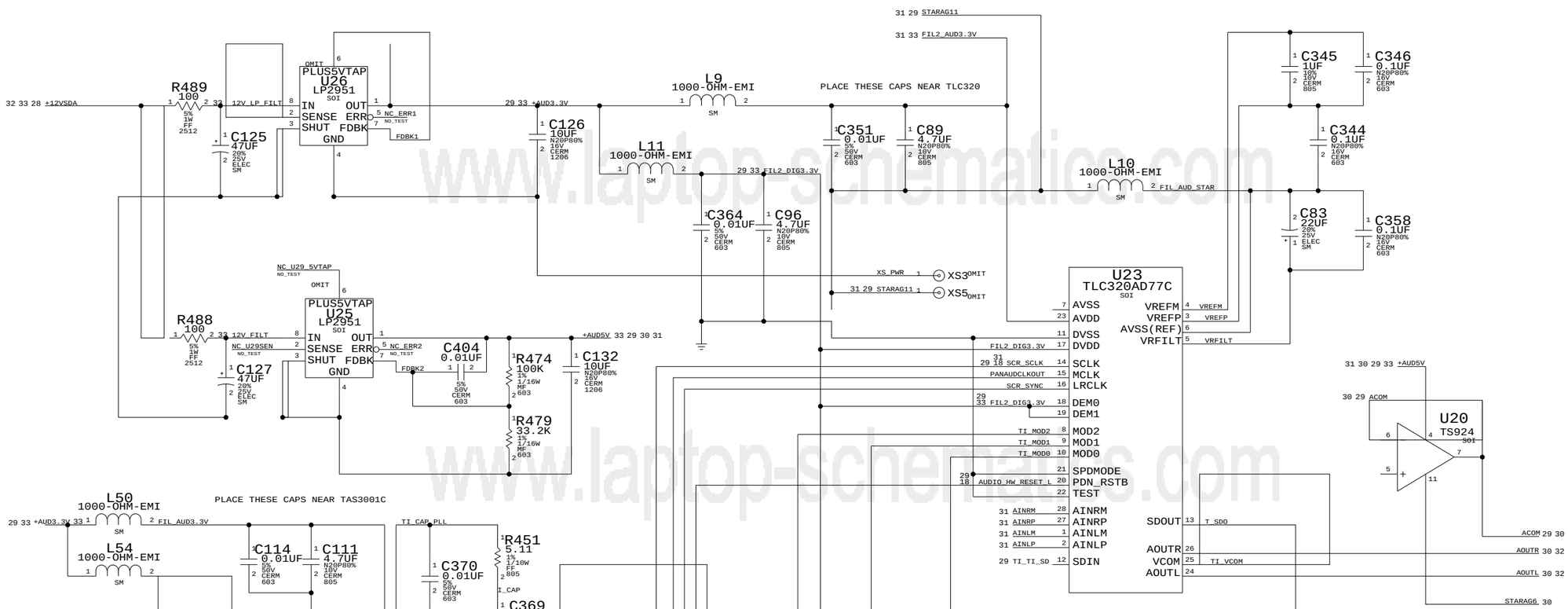
CR-29

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
353S0275	2	IC,2951,ADJ,UPWR,REG,8P,SOP	U25,U26		



CS2/1 I2C ADDRESS SELECTION

CS2	CS1	I2C ADDRESS
0	0	0X68
0	1	0X6A
1	0	0X6C
1	1	0X6E

NEED TO ADD STUFFING OPTIONS

MODE SELECTION

MOD2	MOD1	MOD0	
0	0	0	16-BIT SERIAL
0	0	1	20-BIT SERIAL
0	1	0	24-BIT SERIAL
0	1	1	16-BIT IIS
1	0	0	20-BIT IIS
1	0	1	24-BIT IIS
1	1	0	16-BIT SERIAL LEFT JUSTIFIED
1	1	1	16-BIT DSP FRAME

TUMBLER, CONTROL & D/A

SHEETS 28-32 CONTAIN THE TUMBLER AUDIO SOLUTION
THE FOLLOWING EXTERNAL SIGNALS ARE REQUIRED:

SIGNAL_NAME - DESC

SCR_SYNC - I2S LRCLK
PANAUDCLKOUT - I2S MCLK
KW_IIC_CLK - I2C SCLK
SCR_SCLK - I2S SCLK
KW_IIC_DAT - I2C DATA
SCR_DATAIN - I2S DATA IN (OUT FROM KEYWEST)
TO RESET - A RESET SIGNAL
KW_AUD_DTI - I2S DATA OUT (TO KEYWEST)
AUDIO_SPKR_ID - DETECTS AN EXTERNAL SPKR & READS SPKR II2 ROM
AUDIO_HP_MUTE - MUTE THE HEADPHONE
AUDIO_HP_SENSE - DETECTS HEADPHONES PLUGGED IN
AUDIO_AMP_MUTE - MUTES AUDIO SPEAKER AMP
GPIO_DALLAS - INPUT/OUTPUT TO THE DALLAS ROM
FWPHYRST - POWERS DOWN THE TRIPATH AMP (BACKUP PLAN)

THE FOLLOWING POWER RAILS ARE REQUIRED:

+12VSD -> 12 VOLTS ON ONLY IN RUN MODE (OFF IN SLEEP/SHUTDOWN)

+3,3V -> 3.3 VOLTS ON IN SLEEP/RUN (OFF IN SHUTDOWN)

+5VSD -> 5.0 VOLTS (FOR CALL PROGRESS) ON IN RUN ONLY.

TRICKLE_5V -> 5.0 VOLTS ALWAYS ON.

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12

SCALE NONE — SHT 29 OF 44

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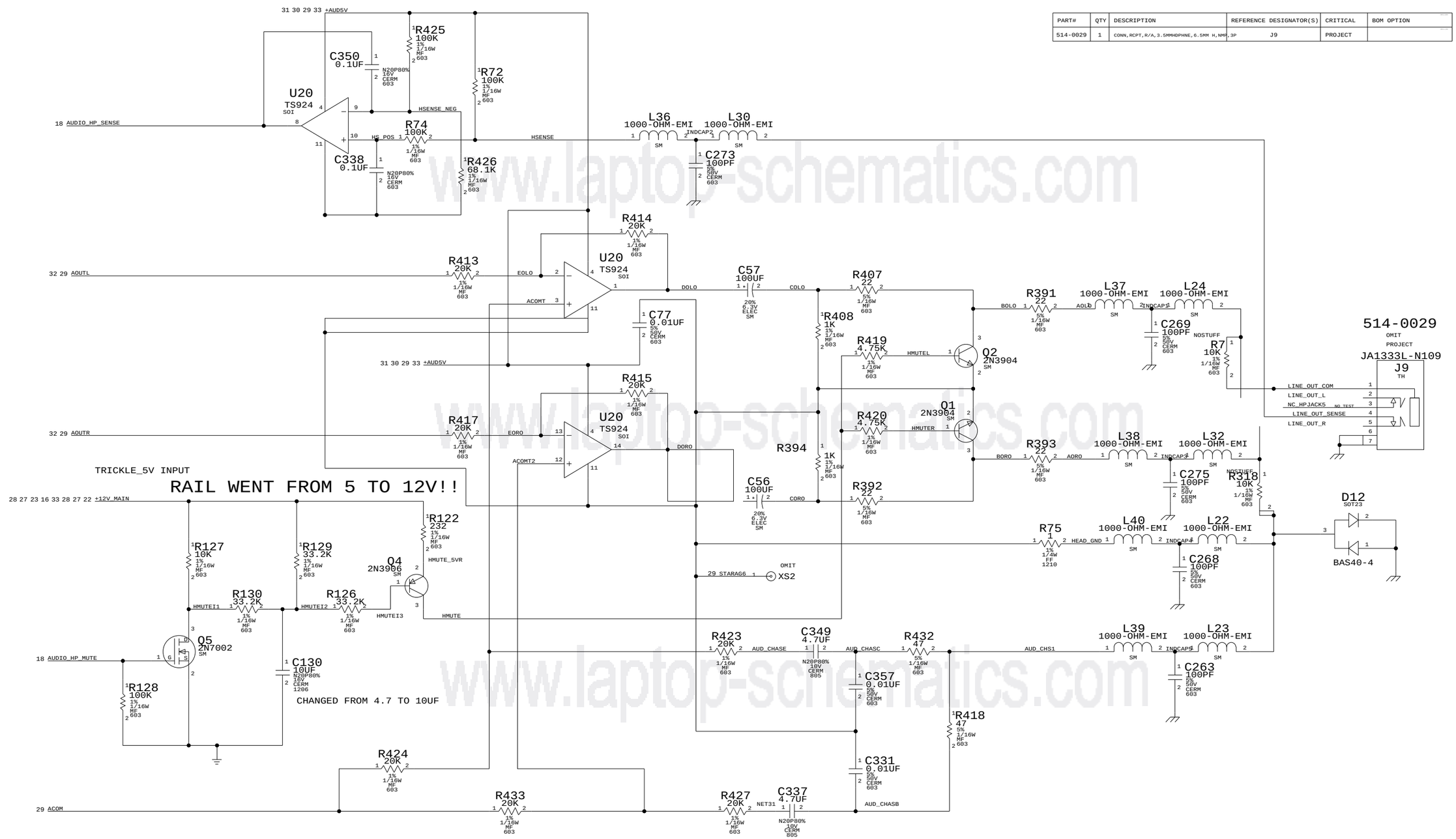
CR-30

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0029	1	CONN,RCPT,R/A,3.5MMHDPHNE,6.5MM H,NMH,3P	J9	PROJECT	



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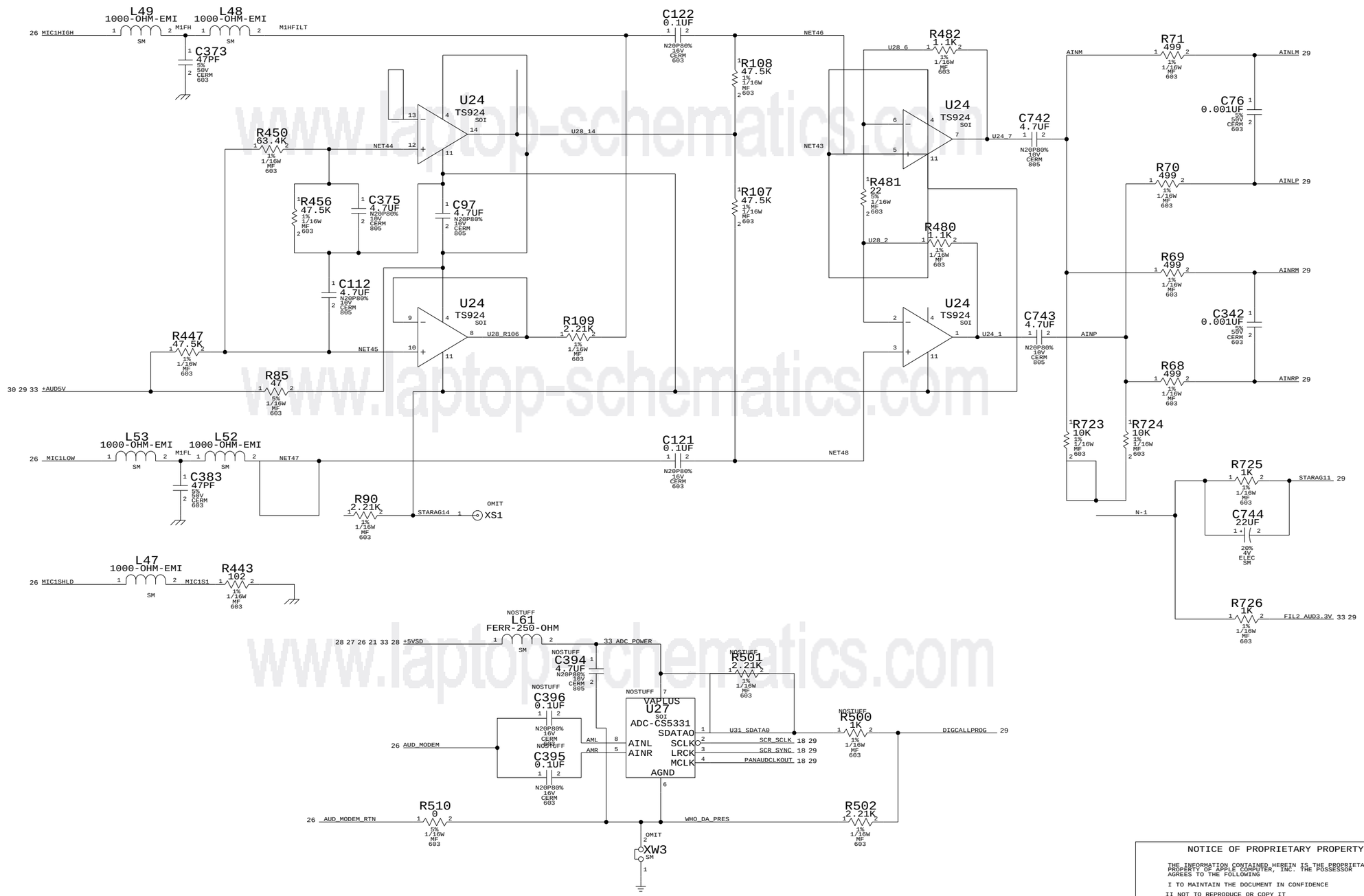
TUMBLER AUDIO, HEADPHONE DRIVER

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE NONE	SHT 30 OF 44	



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TUMBLER AUDIO, MICROPHONE PREAMP AND MODEM CALL PROGRESS

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SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE NONE	SHT 31 OF 44	

CR-32

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0020	1	CONN,2.5MM PH JACK,RT ANG,6-P,NMP	J7	PROJECT	

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
OUTP1	25		10
OUTP2	25		10
OUTM1	25		10
OUTM2	25		10
OUTP1FILT	25		10
OUTP2FILT	25		10
OUTM1FILT	25		10
OUTM2FILT	25		10
SPKR_L+	25		10
SPKR_L-	25		10
SPKR_R+	25		10
SPKR_R-	25		10

ID ROM V(IL) = 0.5V
RISETIME SENSITIVE; SW PROVIDES 4US INTERBIT GAP

514-0020

TUMBLER AUDIO, POWER AMP.

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE NONE	SHT 32 OF 44	

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CR-33

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6101	1	SCHEM,PCBA,P11	PCB1	
056-0862	1	DESIGN GUIDE	PCB1	
DESIGN IF SPECIAL G3 NEEDED> 056-0928	1	DWG,DSGN GD,MLB,P11	PCB1	OMIT
613-3302	1	GEN DWG, PCBA MECH SUBASSY	PCB1	
820-1257	1	PCBF,MLB,P11	PCB1	

HARDWARE

410-1105	2	WIRELESS CONENCTOR SCREW	J22,J22	
835-0101	2	WIRELESS CONNECTOR NUT	J22,J22	
600-9413	1	HEATSINK,MONICA,REAL	U22	OMIT
730-0231	1	HEATSINK,MONICA,STEALTH	U22	OMIT
730-0214	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0202	1	HEATSINK,MICROPROCESSOR	U13	OMIT
730-0217	1	HEATSINK,PANGEA	U6	STEALTH
730-0217	1	HEATSINK,PANGEA	U6	REAL
600-9414	1	HEATSINK,TRIPATH,REAL	U4	OMIT
730-0230	1	HEATSINK,TRIPATH,STEALTH	U4	OMIT
875-0498	1	GAP FILLER VGER CPU	U13	REAL

MODEM/MISC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
525-0057	1	BATTERY HOLDER	BT1		
825-2029	1	LABEL,SERIAL NUMBER BARCODE	PCB1		
617-0186	1	MODEM, SPRING, W/RJ11	J12	PROJECT	OMIT
617-0201	1	MODEM, DASH, W/RJ11	J12	PROJECT	OMIT
617-0205	1	MODEM, DASH, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,DASH,W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, B4, W/NO RJ11	J12	PROJECT	OMIT
617-0196	1	MODEM, AU5, W/NO RJ11	J12	PROJECT	OMIT

617-0196 ALSO REQUIRES DONGLE 611-0138, BUT THAT IS INCLUDED IN ACCESSORY KIT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
617-0213	1	MODEM, SPRING2, W/NO RJ11	J12	PROJECT	OMIT
617-0212	1	EMI FILTER PCB,SPRING2,W/NO RJ11	J12	PROJECT	OMIT

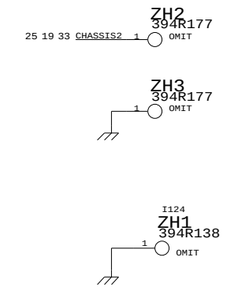
SODIMMS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333-0336	1	IC,SDRAM,64MB ,PC100,SODIMM	J21	PROJECT	OMIT
333-0360	1	IC,SDRAM,128MB,PC100,SODIMM	J21	PROJECT	OMIT
MICRON> 333-0362	1	IC,SDRAM,256MB,PC100,MICRON,SODIMM	J21	PROJECT	OMIT
SAMSUNG/HUNDAI> 333-0363	1	IC,SDRAM,256MB,PC100,SAM/HYUN,SODIMM	J21	PROJECT	OMIT
333-0364	1	IC,SDRAM,512MB,PC100,SODIMM	J21	PROJECT	OMIT

168 PIN DIMMS

333-0112	1	IC,SDRAM,64MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0346	1	IC,SDRAM,128MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0347	1	IC,SDRAM,256MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT
333-0349	1	IC,SDRAM,512MB,PC100,4BK,168P DIMM	J19	PROJECT	OMIT

HOLES AND SLOTS



SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
+5V	200	5	10
+3.3V	25	3.3	10
+12V	100	12	10
	25	0	10
	25	0	10
CPU0VDD	25	1.8	10
VGER_VCORE	15	2.0	10
+AVDD_CPU	25	2.0	10
L3_0VDD	15	1.5	10
L3_CORE	15	2.5	10
PANGEA_AVDD5	10	1.8	10
PANGEA_AVDD4	10	3.3	10
+12VSD_FILT	100	12	10
AGPVDD	10	3.3	10
PANGEA_AVDD6	10	3.3	7
AGPVREF	10	1.32	10
GRAPH_CORE	25	1.9	10
+5VSD	100	5	10
+12VSD	100	12	10
IFP_AVCC	10	3.3	10
MAINCLK_VDD	25	3.3	10
IFP0AVCC	10	3.3	7
DACVDD	10	3.3	10
FB2_5	25	2.5	10
M_VREF1	10	1.25	10
M_VREF2	10	1.25	10
PANGEA_AMVDD	10	3.3	10
PANGEA_TEI		0	10
ETH_RXD_PD		0	10
GBE_REFCLK		0	10
PANGEAVCORE	25	2.5	10
VCCA	10	3.3	10
VCCTXFM	10	3.3	10
PHYAD		0	10
ENET_TST		0	10
ENETCNT		0	10
PWRDWN		0	10
FW_PHY_3_3	10	3.3	10
3.8V_TRICKLE	10	3.8	10
3.3V_TO_FW	10	3.3	10
G_SSCLK_VDD	25	3.3	10
FW_VP_2	40	30	10
FW_VP_1	40	30	10
FW_VP	40	30	10
FW_VGND	40	0	10
AUDAMPPOWER	70	12	10
12V_LP_FILT	25	12	10
12V_FILT	25	12	10
J14_10	25	3.3	10
LED_RET	25	5	10
LED_RET_FILT	25	5	10
XS_SPKR	70	0	10

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	MIN_NECK_WIDTH
CHASSIS2	25	0	10
KS5VSD	15	5	10
LED_5V	25	5	10
LED_5V_FILT	25	5	10
PANGEA_VDDA3	10	3.3	7
PANGEA_VDDA2	10	3.3	10
PANGEA_VDDA1	10	3.3	10
VDD_USB	10	3.3	7
USB_PWR_AB		3.3	10
USB_PWR_CD		3.3	10
USB_PWR_FLT		5	10
AUD_STAR	10	0	10
USB_PWR	200	5	10
USB1_PWR	200	5	10
USB1_GND	200	0	10
USB2_PWR	200	5	10
USB2_GND	200	0	10
USB3_PWR	200	5	10
USB3_GND	200	0	10
PMU_POWER	10	3.3	10
PMU_AVCC	10	3.3	10
+3.3VFPD	25	3.3	10
DDC_VCC_3	10	3.3	10
INT_TMDS_3V	10	3.3	10
3_5_HONKER	50	3.5	25
DETECT_5VT		3.3	10
+12V_MAIN	600	12	25
+12V_DROPPED	50	12	10
UIDE_IOCS16_L		5	10
+12VSDA	100	12	10
+5VSD_T	40	5	10
+12VSD_T	40	12	10
+AUD5V	10	5	10
FIL2_DIG3.3V	10	3.3	10
ADC_POWER	40	5	10
DIG_AUD3.3V	10	3.3	10
FIL_AUD3.3V	10	3.3	10
+AUD3.3V	15	3.3	10
AUD_STAR	15	0	10
FIL2_AUD3.3V	10	3.3	10
AUDAMP5V	10	5	10
SPKR_RTN	100	0	10
DDC_VCC_5	50	0	10
FUSED_DDC_5V	50	0	10

I/O CONNECTORS

USB	SHEET 18	J2, J3, J5
ETHERNET	SHEET 14	J1
FIREWIRE	SHEET 15	J4, J6
VGA	SHEET 24	J8
HEADPHONE	SHEET 29	J9
MODEM	MODEM SCHEM	MODEM SCHEM
DC IN	SHEET 26	J15
SPKR	SHEET 31	J7

Holes and Slots AND EMC INFO

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CR-34

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
CPU_DATA<0>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<1>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<2>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<3>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<4>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<5>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<6>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<7>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<8>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<9>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<10>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<11>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<12>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<13>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<14>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<15>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<16>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<17>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<18>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<19>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<20>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<21>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<22>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<23>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<24>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<25>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<26>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<27>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<28>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<29>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<30>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<31>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<32>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<33>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<34>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<35>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<36>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<37>	100000000::	7		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<38>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<39>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<40>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<41>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<42>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<43>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<44>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<45>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<46>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<47>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<48>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<49>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<50>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<51>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<52>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<53>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<54>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<55>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<56>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<57>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<58>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<59>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<60>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<61>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<62>	100000000::	6		::2000:4500	200		OUT 3 5 24 5 24
CPU_DATA<63>	100000000::	7		::2000:4500	200		OUT 3 5 24 5 24

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
KEY PANGEA TIMING CPU_BR*	100000000::	6		::2000:4500			OUT 3 24 5 20
KEY PANGEA TIMING TS*	100000000::	6		::2000:4500			OUT 3 5 24 20
TBST*	100000000::	6		::2000:4500			OUT 3 5 24 20
AACK*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
KEY PANGEA TIMING ARTRY*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
DBWO*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
KEY PANGEA TIMING QREQ*	100000000::	6		::2000:4500	200		OUT 3 24 5 20
QACK*	100000000::	8		::2000:4500	200		OUT 5 24 3
TA*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
TEA*	100000000::	6		::2000:4500	200		OUT 5 24 3 20
TT<0>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<1>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<2>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<3>	100000000::	6		::2000:4500			OUT 3 5 24 20
TT<4>	100000000::	6		::2000:4500			OUT 3 5 24 20
TSIZ<0>	100000000::	6		::2000:4500	200		OUT 3 5 24
TSIZ<1>	100000000::	6		::2000:4500	200		OUT 3 5 24
TSIZ<2>	100000000::	6		::2000:4500	200		OUT 3 5 24
CPU_ADDR<0>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<1>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<2>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<3>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<4>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<5>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<6>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<7>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<8>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<9>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<10>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<11>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<12>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<13>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<14>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<15>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<16>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<17>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<18>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<19>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<20>	100000000::	6		::2000:4500	220		OUT 3 5 24 3 5 24
CPU_ADDR<21>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<22>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<23>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<24>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<25>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<26>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<27>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<28>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<29>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<30>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
CPU_ADDR<31>	100000000::	6		::2000:4500	200		OUT 3 5 24 3 5 24
GBL*	100000000::	6		::2000:4500			OUT 3 5 24 20
CPU_DBG*	100000000::	6		::2000:4500			OUT 5 24 3 20
CPU_BG*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
WT*	100000000::	6		::2000:4500	200		OUT 3 5 24 20
CI*	100000000::	6		::2000:4500	210		OUT 3 5 24 20

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CONSTRAINTS -- CPU BUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE NONE	SHT 34 OF 44	

CR-35

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NET_SCHED	
MDATA<0>	100000000::	6	::1850:4400	200		U6.AG1 J21.3 J19.2	OUT 6
MDATA<1>	100000000::	6	::1850:4400	200		U6.AF3 J21.5 J19.3	OUT 6
MDATA<2>	100000000::	6	::1850:4400	200		U6.AF1 J21.7 J19.4	OUT 6
MDATA<3>	100000000::	6	::1850:4400	200		U6.AE2 J21.9 J19.5	OUT 6
MDATA<4>	100000000::	6	::1850:4400	200		U6.AE1 J21.13 J19.7	OUT 6
MDATA<5>	100000000::	6	::1850:4400	200		U6.AD2 J21.15 J19.8	OUT 6
MDATA<6>	100000000::	6	::1850:4400	200		U6.AD1 J21.17 J19.9	OUT 6
MDATA<7>	100000000::	6	::1850:4400	200		U6.AC2 J21.19 J19.10	OUT 6
MDATA<8>	100000000::	6	::1850:4400	200		U6.Y1 J21.37 J19.11	OUT 6
MDATA<9>	100000000::	6	::1850:4400	200		U6.Y2 J21.39 J19.13	OUT 6
MDATA<10>	100000000::	6	::1850:4400	200		U6.W1 J21.41 J19.14	OUT 6
MDATA<11>	100000000::	6	::1850:4400	200		U6.W2 J21.43 J19.15	OUT 6
MDATA<12>	100000000::	6	::1850:4400	200		U6.V2 J21.47 J19.16	OUT 6
MDATA<13>	100000000::	6	::1850:4400	200		U6.U2 J21.49 J19.17	OUT 6
MDATA<14>	100000000::	6	::1850:4400	200		U6.T1 J21.51 J19.19	OUT 6
MDATA<15>	100000000::	6	::1850:4400	200		U6.T2 J21.53 J19.20	OUT 6
MDATA<16>	100000000::	6	::1850:4400	200		U6.R1 J21.83 J19.55	OUT 6
MDATA<17>	100000000::	6	::1850:4400	200		U6.R2 J21.85 J19.56	OUT 6
MDATA<18>	100000000::	6	::1850:4400	200		U6.P3 J21.87 J19.57	OUT 6
MDATA<19>	100000000::	6	::1850:4400	200		U6.P2 J21.89 J19.58	OUT 6
MDATA<20>	100000000::	6	::1850:4400	200		U6.N1 J21.93 J19.60	OUT 6
MDATA<21>	100000000::	6	::1850:4400	200		U6.N2 J21.95 J19.65	OUT 6
MDATA<22>	100000000::	6	::1850:4400	200		U6.M1 J21.97 J19.66	OUT 6
MDATA<23>	100000000::	6	::1850:4400	200		U6.M2 J21.99 J19.67	OUT 6
MDATA<24>	100000000::	6	::1850:4400	200		U6.J2 J21.121 J19.69	OUT 6
MDATA<25>	100000000::	6	::1850:4400	200		U6.H2 J21.123 J19.70	OUT 6
MDATA<26>	100000000::	6	::1850:4400	200		U6.G1 J21.125 J19.71	OUT 6
MDATA<27>	100000000::	6	::1850:4400	200		U6.G2 J21.127 J19.72	OUT 6
MDATA<28>	100000000::	6	::1850:4400	200		U6.F1 J21.131 J19.74	OUT 6
MDATA<29>	100000000::	6	::1850:4400	200		U6.F2 J21.133 J19.75	OUT 6
MDATA<30>	100000000::	6	::1850:4400	200		U6.E1 J21.135 J19.76	OUT 6
MDATA<31>	100000000::	6	::1850:4400	200		U6.H3 J21.137 J19.77	OUT 6
MDATA<32>	100000000::	6	::1850:4400	200		U6.AD3 J21.4 J19.86	OUT 6
MDATA<33>	100000000::	6	::1850:4400	200		U6.AD5 J21.6 J19.87	OUT 6
MDATA<34>	100000000::	6	::1850:4400	200		U6.AC3 J21.8 J19.88	OUT 6
MDATA<35>	100000000::	6	::1850:4400	200		U6.AC5 J21.10 J19.89	OUT 6
MDATA<36>	100000000::	6	::1850:4400	200		U6.AC6 J21.14 J19.91	OUT 6
MDATA<37>	100000000::	6	::1850:4400	200		U6.AC7 J21.16 J19.92	OUT 6
MDATA<38>	100000000::	6	::1850:4400	200		U6.AB6 J21.18 J19.93	OUT 6
MDATA<39>	100000000::	6	::1850:4400	200		U6.AB7 J21.20 J19.94	OUT 6
MDATA<40>	100000000::	6	::1850:4400	200		U6.AA5 J21.38 J19.95	OUT 6
MDATA<41>	100000000::	6	::1850:4400	200		U6.AA6 J21.40 J19.97	OUT 6
MDATA<42>	100000000::	6	::1850:4400	200		U6.AA7 J21.42 J19.98	OUT 6
MDATA<43>	100000000::	6	::1850:4400	200		U6.AC1 J21.44 J19.99	OUT 6
MDATA<44>	100000000::	6	::1850:4400	200		U6.V3 J21.48 J19.100	OUT 6
MDATA<45>	100000000::	6	::1850:4400	200		U6.V5 J21.50 J19.101	OUT 6
MDATA<46>	100000000::	6	::1850:4400	200		U6.V6 J21.52 J19.103	OUT 6
MDATA<47>	100000000::	6	::1850:4400	200		U6.W7 J21.54 J19.104	OUT 6
MDATA<48>	100000000::	6	::1850:4400	200		U6.U3 J21.84 J19.139	OUT 6
MDATA<49>	100000000::	6	::1850:4400	200		U6.U5 J21.86 J19.140	OUT 6
MDATA<50>	100000000::	6	::1850:4400	200		U6.U6 J21.88 J19.141	OUT 6
MDATA<51>	100000000::	6	::1850:4400	200		U6.U7 J21.90 J19.142	OUT 6
MDATA<52>	100000000::	6	::1850:4400	200		U6.R6 J21.94 J19.144	OUT 6
MDATA<53>	100000000::	6	::1850:4400	200		U6.R7 J21.96 J19.149	OUT 6
MDATA<54>	100000000::	6	::1850:4400	200		U6.P5 J21.98 J19.150	OUT 6
MDATA<55>	100000000::	6	::1850:4400	200		U6.P6 J21.100 J19.151	OUT 6
MDATA<56>	100000000::	6	::1850:4400	200		U6.L6 J21.122 J19.153	OUT 6
MDATA<57>	100000000::	6	::1850:4400	200		U6.L7 J21.124 J19.154	OUT 6
MDATA<58>	100000000::	6	::1850:4400	200		U6.K6 J21.126 J19.155	OUT 6
MDATA<59>	100000000::	6	::1850:4400	200		U6.K7 J21.128 J19.156	OUT 6
MDATA<60>	100000000::	6	::1850:4400	200		U6.J3 J21.132 J19.158	OUT 6
MDATA<61>	100000000::	6	::1850:4400	200		U6.J5 J21.134 J19.159	OUT 6
MDATA<62>	100000000::	6	::1850:4400	200		U6.J6 J21.136 J19.160	OUT 6
MDATA<63>	100000000::	6	::1850:4400	200		U6.J7 J21.138 J19.161	OUT 6

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
PANGEAMCLK<1>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
PANGEAMCLK<3>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
PANGEAMCLK<4>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
PANGEAMCLK<5>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
PANGEAMCLK<6>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
PANGEAMCLK<7>	100000000::	3	6		::1800:2000		100	10 MIL SPACING	OUT 6 7
MAINCLK_XIN	100000000::				::1800:2000			10 MIL SPACING	OUT 7
MAINCLK_XOUT	100000000::				::1800:2000			10 MIL SPACING	OUT 7
MCLK<1>	100000000::	4	6	J21.74 R550.2 R680.2	::2000:3500	250		10 MIL SPACING	OUT 6 7
MCLK<3>	100000000::	4	6	J21.61 R556.2 R668.2	::2000:3500	250		10 MIL SPACING	OUT 6 7
MCLK<4>	100000000::	4	6	J19.42 R547.2 R560.2	::2000:3500	250		10 MIL SPACING	OUT 6 7
MCLK<5>	100000000::	4	6	J19.125 R543.2 R580.2	::2000:3500	250		10 MIL SPACING	OUT 6 7
MCLK<6>	100000000::	4	6	J19.79 R558.2 R572.2	::2000:4500	250		10 MIL SPACING	OUT 6 7
MCLK<7>	100000000::	4	6	J19.163 R552.2 R656.2	::2000:4500	250		10 MIL SPACING	OUT 6 7
MCLKOUT<1>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
MCLKOUT<3>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
MCLKOUT<4>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
MCLKOUT<5>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
MCLKOUT<6>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
MCLKOUT<7>	100000000::	2	6		:::250			10 MIL SPACING	OUT 7
M_ADDR<0>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<1>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<2>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<3>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<4>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<5>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<6>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<7>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<8>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<9>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<10>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<11>	100000000::	4			::400:1200		200		OUT 6 8
M_ADDR<12>	100000000::	4			::400:1200		200		OUT 6 8
TERM_M_ADDR<0>	100000000::	8		RP33.2 J21.29 RP29.8	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<1>	100000000::	8		RP9.4 J21.31 RP29.7	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<2>	100000000::	8		RP31.1 J21.33 RP26.6	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<3>	100000000::	8		6RP9.3 J21.30 RP26.5	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<4>	100000000::	8		RP31.2 J21.32 RP26.8	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<5>	100000000::	8		RP9.1 J21.34 RP26.7	::1100:3300				OUT 6 8 6 8
TERM_M_ADDR<6>	100000000::	8		RP21.1 J21.103 RP24.6	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<7>	100000000::	8		RP23.2 J21.104 RP24.5	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<8>	100000000::	8		RP21.2 J21.105 RP24.8					OUT 6 8 6 8
TERM_M_ADDR<9>	100000000::	8		RP21.3 J21.109 RP24.7					OUT 6 8 6 8
TERM_M_ADDR<10>	100000000::	8		RP21.4 J21.111 RP22.6	::1050:3200				OUT 6 8 6 8
TERM_M_ADDR<11>	100000000::	8		RP23.3 J21.112 RP22.7	::1100:3200				OUT 6 8 6 8
TERM_M_ADDR<12>	100000000::	8		R540.2 J21.70 R123.1					OUT 6 8 6 8

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CONSTRAINTS -- MEMORY PAGE 1

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6101 | REV. 12

SCALE NONE | SHT 35 OF 44

CR-36

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	NET_SCHED	
T_M_BA0	100MHZ::	5	::1100:2400	200	5 MIL SPACING	RP23.1 J21.106 RP22.5	OUT 6
T_M_BA1	100MHZ::	5	::1100:2400		5 MIL SPACING	RP23.4 J21.110 RP22.8	OUT 6
T_SDRAS*	100MHZ::	5			5 MIL SPACING	RP31.4 J21.65 RP29.6	OUT 6
T_SDCAS*	100MHZ::	5	::1100:2400	200	5 MIL SPACING	RP31.3 J21.66 RP29.5	OUT 6
T_MEMWE*	100MHZ::	5	::1100:2400	200	5 MIL SPACING	R539.1 J21.67 R158.2	OUT 6
T2_M_BA0	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_M_BA1	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_SDRAS*	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6
T2_SDCAS*	100MHZ::	4	::100:840	200	5 MIL SPACING		OUT 6
T2_MEMWE*	100MHZ::	4	::100:500	200	5 MIL SPACING		OUT 6

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
PANGEA_CPU_CLK	100MHZ::	2	6		::300:500		100	10 MIL SPACING	OUT 5
CPU_CLK	100MHZ::	6	6		::2700:4100	1000	200	10 MIL SPACING	OUT 3 5 7
CPUFBOUT	100MHZ::	2	6		::100:600		100	10 MIL SPACING	OUT 5
TCPUFBOUT	100MHZ::	2	6		::475:700		100	10 MIL SPACING	OUT 5 7
CPUFB7	100MHZ::	2	6		::2700:3000		100	10 MIL SPACING	OUT 5
CPUFB6	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB5	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB4	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB3	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB2	100MHZ::	2	6		::1800:2000		100	10 MIL SPACING	OUT 5
CPUFB1	100MHZ::	2	6		::2600:3000		100	10 MIL SPACING	OUT 5
CPUFBIN	100MHZ::	6	6		::475:1300	1000	100	10 MIL SPACING	OUT 5 7
AGPFB0	66MHZ::	2	5		::950:1000	250	100	10 MIL SPACING	OUT 8
AGPFB1	66MHZ::	2	5		::475:700		100	10 MIL SPACING	OUT 8
AGPFB2	66MHZ::	2	5		::950:1100		100	10 MIL SPACING	OUT 8
AGPFB3	66MHZ::	2	5		::475:700		100	10 MIL SPACING	OUT 8
SCHMOO_CPU_CLK	100MHZ::	2	6		::300:500	250	100	10 MIL SPACING	OUT
BANDAID	18.432MHZ::	3			:::2700		100	10 MIL SPACING	OUT

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
TERM2_M_ADDR<0>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<1>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<2>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<3>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<4>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<5>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<6>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<7>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<8>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<9>	100MHZ::	4		::100:500	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<10>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<11>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
TERM2_M_ADDR<12>	100MHZ::	4		::100:700	200	5 MIL SPACING	OUT 6 8 6 8
DQM0*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM1*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM2*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM3*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM4*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM5*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM6*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6
DQM7*	100MHZ::	4		::3000:4000	200	5 MIL SPACING	OUT 6

CS0*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS1*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS2*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
CS3*	100MHZ::	5		::600:1100	200	5 MIL SPACING	OUT 6
T1CS0*	100MHZ::	4		::300:1400	200	5 MIL SPACING	OUT 6
T1CS1*	100MHZ::	4		::300:1400	200	5 MIL SPACING	OUT 6
T2CS2*	100MHZ::	4		::300:2400	200	5 MIL SPACING	OUT 6
T2CS3*	100MHZ::	4		::300:2400	200	5 MIL SPACING	OUT 6
M_BA0	100MHZ::	4		::400:1400	200	5 MIL SPACING	OUT 6
M_BA1	100MHZ::	4		::400:1400	200	5 MIL SPACING	OUT 6
SDRAS*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6
SDCAS*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6
MEMWE*	100MHZ::	4		::400:1000	200	5 MIL SPACING	OUT 6

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CONSTRAINTS -- MEMORY PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6101	12
SCALE NONE	SHT 36 OF 44	

CONSTRAINTS -- AGP, FIREWIRE, PARTIAL GRAPHICS (1 OF 2)

AGP RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	NET_SCHED	NET_SPACING_TYPE	DELAY_RULE	MIN_LINE_WIDTH	
PANGEA_AGP_CLK	66MHZ:: / 3	250 /		10 MIL SPACING	::0225:0275	5	OUT 8
AGP_CLK	66MHZ:: / 12	/		20 MIL SPACING	::3800:3900		OUT 8 9
AGP_FB_IN	66MHZ:: / 3	/		10 MIL SPACING	::1325:1350	5	OUT 8
AGP_FB_OUT	66MHZ:: / 3	/		10 MIL SPACING	::0320:0335	5	OUT 8
AGPCBE<3>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPCBE<2>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPCBE<1>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPCBE<0>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<31>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<30>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<29>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<28>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<27>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<26>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<25>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<24>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<23>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<22>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<21>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<20>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<19>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<18>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<17>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<16>	66MHZ:: / 8	/		5 MIL SPACING	::3750:4000		OUT 8 9
AGPAD<15>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<14>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<13>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<12>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<11>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<10>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<9>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<8>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<7>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<6>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<5>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<4>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<3>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<2>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<1>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
AGPAD<0>	66MHZ:: / 8	/		5 MIL SPACING	::3050:3300		OUT 8 9
PAN_AGPADSTB<1>	66MHZ:: / 4	250 / 200		10 MIL SPACING	::0500:0550		OUT 8
AGPADSTB<1>	66MHZ:: / 8	/ 200		10 MIL SPACING	::3450:3500		OUT 8 9 20
PAN_AGPADSTB<0>	66MHZ:: / 4	250 / 200		10 MIL SPACING	::0600:0650		OUT 8
AGPADSTB<0>	66MHZ:: / 8	/ 200		10 MIL SPACING	::2650:2700		OUT 8 9 20
AGPST<2>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPST<1>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPST<0>	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPREQ*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20
AGPGNT*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPPAR	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9
AGPFRAME*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPTRDY*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPIRDY*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
PCISTOP*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPDEVSEL*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 8 9 20
AGPPIPE*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20
AGPRBF*	66MHZ:: / 8	/		5 MIL SPACING	::3500:4500		OUT 9 8 20

FIREWIRE RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	DELAY_RULE	
FW_XI	24.576MHZ / 2	250	200	10 MIL SPACING		OUT 16
FW_XO	24.576MHZ / 2	250	200	10 MIL SPACING		OUT 16
FW_SCLK	49.152MHZ / 4	250	200	10 MIL SPACING	::5400:6200	OUT 13 16
FW_PHY_SCLK	49.152MHZ / 2	250	200	10 MIL SPACING	::0100:0300	OUT 16
FW_LINK_D<7>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<6>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<5>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<4>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<3>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<2>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<1>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_D<0>	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_CNTL1	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_CNTL0	49.152MHZ / 2		220	5 MIL SPACING	::0500:0800	OUT 13
FW_LINK_LREQ	49.152MHZ / 2		200	5 MIL SPACING	::0500:0800	OUT 13
FW_D<7>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<6>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<5>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<4>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<3>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<2>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<1>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_D<0>	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_CNTL1	49.152MHZ / 4		200	5 MIL SPACING	::4900:5400	OUT 13 16
FW_CNTL0	49.152MHZ / 4		220	5 MIL SPACING	::4900:5400	OUT 13 16
FW_LREQ	49.152MHZ / 4		200	5 MIL SPACING	::5000:5700	OUT 13 16
FW_PHY_D<7>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<6>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<5>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<4>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<3>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<2>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<1>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_D<0>	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_CNTL1	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16
FW_PHY_CNTL0	49.152MHZ / 2		200	5 MIL SPACING	::0100:0300	OUT 16

FIREWIRE DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	DIFFERENTIAL_PAIR	
FW_TPB2P	400MHZ / 3		5 MIL SPACING	TRUE	FW_TPB2X	OUT 16
FW_TPB2N	400MHZ / 3		5 MIL SPACING	TRUE	FW_TPB2X	OUT 16
FW_TPA2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA2X	OUT 16
FW_TPA2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA2X	OUT 16
FW_TPB1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPB1X	OUT 16
FW_TPB1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPB1X	OUT 16
FW_TPA1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA1X	OUT 16
FW_TPA1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPA1X	OUT 16
FW_TPI2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI2	OUT 16
FW_TPI2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI2	OUT 16
FW_TPO2P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO2	OUT 16
FW_TPO2N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO2	OUT 16
FW_TPI1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI1	OUT 16
FW_TPI1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPI1	OUT 16
FW_TPO1P	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO1	OUT 16
FW_TPO1N	400MHZ / 2		5 MIL SPACING	TRUE	FW_TPO1	OUT 16

GRAPHICS DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	DIFFERENTIAL_PAIR	DELAY_RULE	RATSNET_SCHEDULE	
INT_TMDS_D2P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D2	::900:1200		OUT 9 25
INT_TMDS_D2M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D2	::900:1200		OUT 9 25
INT_TMDS_D1P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D1	::900:1200		OUT 9 25
INT_TMDS_D1M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D1	::900:1200		OUT 9 25
INT_TMDS_D0P	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D0	::900:1200		OUT 9 25
INT_TMDS_D0M	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_D0	::900:1200		OUT 9 25
INT_TMDS_CKP	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_CK	::900:1200		OUT 9 25
INT_TMDS_CKM	300MHZ:: / 2		10 MIL SPACING		INT_TMDS_CK	::900:1200		OUT 9 25
FBCLK0P	143MHZ:: / 2		5 MIL SPACING		FBCLK0	::0470:0500		OUT 10
FBCLK0M	143MHZ:: / 2		5 MIL SPACING		FBCLK0	::0470:0500		OUT 10
TERM_FBCLK0P	143MHZ:: / 4		5 MIL SPACING		TERM_FBCLK0			OUT 10 11
TERM_FBCLK0M	143MHZ:: / 4		5 MIL SPACING		TERM_FBCLK0			OUT 10 11

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D	051-6101	12
SCALE NONE	SHT 37 OF 44	

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CONSTRAINTS -- GRAPHICS (2 OF 2)

GRAPHICS RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	RATSNET_SCHEDULE		NET_SPACING_TYPE	DELAY_RULE	
GRAPH_XTALIN	14MHZ / 4	200 / 250			10 MIL SPACING		OUT 9
GRAPH_XTALOUT	14MHZ / 3	200 / 250			10 MIL SPACING		OUT 9
FBD<63>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<62>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<61>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<60>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<59>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<58>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<57>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<56>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<55>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<54>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<53>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<52>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<51>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<50>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<49>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<48>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<47>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<46>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<45>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<44>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<43>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<42>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<41>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<40>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<39>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<38>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<37>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<36>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<35>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<34>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<33>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<32>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<31>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<30>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<29>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<28>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<27>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<26>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<25>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<24>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<23>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<22>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<21>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<20>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<19>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<18>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<17>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<16>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<15>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<14>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<13>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<12>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<11>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<10>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<9>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<8>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<7>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<6>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<5>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<4>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<3>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<2>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<1>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBD<0>	143MHZ / 6	200 /			7.5 MIL SPACING	::1600:2900	OUT 10 11 10 11
FBCS0*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCS0*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBRAS*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBRAS*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBCAS*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCAS*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBWE*	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBWE*	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
FBCKE	143MHZ / 2	200 /			7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBCKE	143MHZ / 4	200 /	FAR_END_CLUSTER		7.5 MIL SPACING		OUT 10 11
G_FBDQS1	143MHZ / 2	200 /			7.5 MIL SPACING	::0500:0600	OUT 10
TERM_FBDQS1	143MHZ / 4	200 /			7.5 MIL SPACING	::5800:6200	OUT 10 11
M_FBDQS1	143MHZ / 2	200 /			7.5 MIL SPACING	::0150:0250	OUT 11
G_FBDQS5	143MHZ / 3	200 /			7.5 MIL SPACING	::0500:0600	OUT 10
TERM_FBDQS5	143MHZ / 4	200 /			7.5 MIL SPACING	::5800:6200	OUT 10 11
M_FBDQS5	143MHZ / 2	200 /			7.5 MIL SPACING	::0150:0250	OUT 11
G_SSCLK_REFOUT	14MHZ 4	200 250			10 MIL SPACING	:::500	OUT 12
G_SSCLK_MODOUT	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12
T_SSCLK_REFOUT	14MHZ 3	200 250			10 MIL SPACING	:::1500	OUT 9 12
GRAPH_XTALSIN	14MHZ 3	200 250			10 MIL SPACING	:::1500	OUT 9 12
G_SSCLK_XI	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12
G_SSCLK_XO	14MHZ 3	200 250			10 MIL SPACING	:::500	OUT 12

MORE GRAPHICS RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	RATSNET_SCHEDULE	STUB_LENGTH	NET_SPACING_TYPE	DELAY_RULE	
FBA<13>	143MHZ 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<12>	143MHZ / 3		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<11>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<10>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<9>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<8>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<7>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<6>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<5>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<4>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<3>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<2>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<1>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
FBA<0>	143MHZ / 2		200	7.5 MIL SPACING	::0400:0700	OUT 10
TERM_FBA<13>	143MHZ 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11 10 11
TERM_FBA<12>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<11>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<10>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<9>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<8>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<7>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<6>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<5>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<4>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<3>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<2>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<1>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
TERM_FBA<0>	143MHZ / 5	FAR_END_CLUSTER	200	7.5 MIL SPACING		OUT 10 11
FBDQM<7>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<6>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<5>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<4>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<3>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<2>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<1>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
FBDQM<0>	143MHZ / 4		200	7.5 MIL SPACING	::1600:2700	OUT 10 11
ANALOG_BLU	66MHZ / 3			15 MIL SPACING		OUT 9 25
ANALOG_GRN	66MHZ / 3			15 MIL SPACING		OUT 9 25
ANALOG_RED	66MHZ / 3			15 MIL SPACING		OUT 9 25
FILTERED_ANALOG_BLU	66MHZ / 2		20			OUT 25
FILTERED_ANALOG_GRN	66MHZ / 2		20			OUT 25
FILTERED_ANALOG_RED	66MHZ / 2		20			OUT 25

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SIG_NAME	PULSE_PARAM	MAX_EXPOSED_LENGTH	ECL	DIFFERENTIAL_PAIR	MAX_VIA_COUNT	STUB_LENGTH	DELAY_RULE	NET_SPACING_TYPE	
UIDE_DA<0>	66MHZ				6		::5170:6000	10 MIL SPACING	OUT 17
UIDE_DA<1>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_DA<2>	66MHZ				6		::5170:6100	10 MIL SPACING	OUT 17
UIDE_DSTB_RDY	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_CS0_L	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_CS1_L	66MHZ				6		::5000:6700	10 MIL SPACING	OUT 17
UIDE_RESET_L	66MHZ				6		::1600:2000	10 MIL SPACING	OUT 17
UIDE_STOP	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_HSTB_RDY	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_DMAACK_L	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_DMAREQ	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_IRQ	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<0>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<1>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<2>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<3>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<4>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<5>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<6>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<7>	66MHZ				6		U6.J30:RP25.4:5170:5920	10 MIL SPACING	OUT 17
UIDE_D<8>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<9>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<10>	66MHZ				6		::5000:5920	10 MIL SPACING	OUT 17
UIDE_D<11>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<12>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<13>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
UIDE_D<14>	66MHZ				6		::5130:5920	10 MIL SPACING	OUT 17
UIDE_D<15>	66MHZ				6		::5170:5920	10 MIL SPACING	OUT 17
T_UIDE_RESET_L	66MHZ				6	100	R141.2:J14.1:3508:3858	10 MIL SPACING	OUT 26 17
L1_TXCLK	2.5MHZ,25MHZ				4	100	::300:500	10 MIL SPACING	OUT 15
L1_RXCLK	2.5MHZ,25MHZ				4		::300:500	10 MIL SPACING	OUT 15
MII_TX_CLK	2.5MHZ,25MHZ				4	100	:::6000	10 MIL SPACING	OUT 13 15
MII_RX_CLK	2.5MHZ,25MHZ	250			4	100	:::6000	10 MIL SPACING	OUT 13 15
TPFOP	10MHZ,100MHZ	200			2	100		10 MIL SPACING	OUT 15
TPFON	10MHZ,100MHZ	202			2	100		10 MIL SPACING	OUT 15
TPFIP	10MHZ,100MHZ	200			2	100		10 MIL SPACING	OUT 15
TPFIN	10MHZ,100MHZ	225			2	100		10 MIL SPACING	OUT 15
TPFIP2	10MHZ,100MHZ	900			2	100		10 MIL SPACING	OUT 15
TPFIN2	10MHZ,100MHZ	400			2	100		10 MIL SPACING	OUT 15
TXP	10MHZ,100MHZ				2	100			OUT 15
TXN	10MHZ,100MHZ				2	100			OUT 15
RXP	10MHZ,100MHZ				2	100			OUT 15
RXN	10MHZ,100MHZ				2	100			OUT 15
TXCT	10MHZ,100MHZ				2	100			OUT 15
RXCT	10MHZ,100MHZ				2	100			OUT 15
ETH_XI	25MHZ	250			3	100	:::1500	10 MIL SPACING	OUT 15
ETH_XO	25MHZ	250			3	100	:::1500	10 MIL SPACING	OUT 15
PAN_XI	18.432MHZ				3		:::1100	10 MIL SPACING	OUT 18
PAN_XO	18.432MHZ	250			2	100	:::1000	10 MIL SPACING	OUT 18
PAN_XT	18.432MHZ				2		:::500	10 MIL SPACING	OUT 18
PMU_XO	10MHZ	250			2	100	:::1000	10 MIL SPACING	OUT 23
PMU_XI	10MHZ				2	100	:::1000	10 MIL SPACING	OUT 23
PMU_XT	10MHZ				2	100	:::1000	10 MIL SPACING	OUT 23
PMU_CLKOUT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING	OUT 23
PMU_CLKIN	0.032768MHZ				2	100	:::1000	10 MIL SPACING	OUT 23
PMU_CLKT	0.032768MHZ	250			2	100	:::1000	10 MIL SPACING	OUT 23

2KV_ISO === 100MIL SPACING

SIG_NAME	ECL			
USB_DCM	TRUE			OUT 18 19
USB_DCP	TRUE			OUT 18 19
USB_DAM	TRUE			OUT 18 19
USB_DAP	TRUE			OUT 18 19
USB_DBM	TRUE			OUT 18 19
USB_DBP	TRUE			OUT 18 19
USB_DCM_F	TRUE			OUT 19
USB_DCP_F	TRUE			OUT 19
USB_DAM_F	TRUE			OUT 19
USB_DAP_F	TRUE			OUT 19
USB_DBM_F	TRUE			OUT 19
USB_DBP_F	TRUE			OUT 19
USB_DCM_EMI	TRUE			OUT 19
USB_DCP_EMI	TRUE			OUT 19
USB_DAM_EMI	TRUE			OUT 19
USB_DAP_EMI	TRUE			OUT 19
USB_DBM_EMI	TRUE			OUT 19
USB_DBP_EMI	TRUE			OUT 19

SIG_NAME	NET_SCHED	
IODATA<0>	U6.P34 R138.2 R137.1 U7.25 J22.30	OUT 8 17 18 26
IODATA<1>	U6.R32 R143.2 R142.1 U7.26 J22.31	OUT 8 17 18 26
IODATA<2>	U6.T29 R150.2 R149.1 U7.27 J22.32	OUT 8 17 18 26
IODATA<3>	U6.T28 R145.2 R140.1 U7.28 J22.2	OUT 8 17 18 26
IODATA<4>	U6.R33 R156.2 R151.1 U7.32 J22.3	OUT 8 17 18 26
IODATA<5>	U6.R34 R139.2 R144.1 U7.33 J22.4	OUT 8 17 18 26
IODATA<6>	U6.U29 R165.2 R162.1 U7.34 J22.5	OUT 8 17 18 26
IODATA<7>	U6.T33 U7.35 J22.6	OUT 8 17 18 26
IOADDR<0>	U6.N28 U7.21 J22.29	OUT 17 8 26
IOADDR<1>	U6.J34 U7.20 J22.28	OUT 17 8 26
IOADDR<2>	U6.M30 U7.19 J22.27	OUT 17 8 26
IOADDR<3>	U6.L32 U7.18 J22.26	OUT 17 8 26
IOADDR<4>	U6.K34 U7.17 J22.25	OUT 17 8 26
IOADDR<5>	U6.L33 U7.16 J22.24	OUT 18 8 26
IOADDR<6>	U6.N29 U7.15 J22.23	OUT 18 8 26
IOADDR<7>	U6.M32 U7.14 J22.22	OUT 18 8 26
IOADDR<8>	U6.L34 U7.8 J22.12	OUT 18 8 26
IOADDR<9>	U6.P28 U7.7 J22.11	OUT 18 8 26
IOADDR<10>	U6.M33 U7.36 J22.8	OUT 18 8 26
IOADDR<11>	U6.P29 U7.6 J22.10	OUT 18 8 26
IOADDR<12>	U6.M34 U7.5 J22.21	OUT 18 8 26
IOADDR<13>	U6.P30 U7.4 J22.13	OUT 18 8 26
IOADDR<14>	U6.N33 U7.3 J22.14	OUT 18 8 26
IOADDR<15>	U6.R28 U7.2 J22.20	OUT 18 8 26
IOADDR<16>	U6.P32 U7.1 J22.19	OUT 18 8 26
IOADDR<17>	U6.N34 U7.40 J22.46	OUT 18 8 26
IOADDR<18>	U6.R29 U7.13 J22.47	OUT 18 8 26
IOADDR<19>	U6.P33 U7.37 J22.48	OUT 18 8 26
IOADDR<20>	U6.R30 U7.38 J22.49	OUT 18 8 26

SIG_NAME	NET_SCHED	
CB_CE2*	U6.W28 RP10.4 J22.42	OUT 17 20 26
CB_CE1*	U6.W29 RP10.3 J22.7	OUT 17 20 26
CB_IORD*	U6.W33 RP10.1 J22.44	OUT 18 20 26
CB_IOWR*	U6.W34 RP10.2 J22.45	OUT 18 20 26
CB_IREQ*	U6.A32 R178.1 J22.16	OUT 18 20 26
CB_REG*	U6.B31 R136.1 J22.61	OUT 18 20 26
CB_RESET	U6.AE33 R168.2 J22.58	OUT 18 26
CB_WAIT*	U6.Y34 R148.1 J22.59	OUT 18 20 26
CSWE*	U6.V29 RP12.2 J22.15	OUT 17 20 26
CSOE*	U6.Y33 RP12.1 J22.9	OUT 17 20 26

CONSTRAINTS -- MISCELLANEOUS

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D	051-6101	12
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SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
VGER_L3D<0>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<1>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<2>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<3>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<4>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<5>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<6>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<7>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<8>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<9>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<10>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<11>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<12>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<13>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<14>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<15>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<16>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<17>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<18>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<19>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<20>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<21>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<22>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<23>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<24>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<25>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<26>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<27>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<28>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<29>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<30>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<31>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<32>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<33>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<34>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<35>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<36>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<37>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<38>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<39>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<40>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<41>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<42>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<43>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<44>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<45>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<46>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<47>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<48>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<49>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<50>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<51>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<52>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<53>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<54>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<55>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<56>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<57>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<58>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<59>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<60>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<61>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<62>	200MHZ	4		::1200:2500	100		OUT 4
VGER_L3D<63>	200MHZ	4		::1200:2500	100		OUT 4

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LIN_WIDTH	DELAY_RULE	STUB_LENGTH	NET_SPACING_TYPE	
VGER_L3A<0>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<1>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<2>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<3>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<4>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<5>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<6>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<7>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<8>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<9>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<10>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<11>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<12>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<13>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<14>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<15>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<16>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3A<17>	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3CLK<0>	200MHZ	4		::2345:2355	100		OUT 4
VGER_L3CLK<1>	200MHZ	4		::2345:2355	100		OUT 4
VGER_L3CE*	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3WE*	200MHZ	4		::2500:2800	100		OUT 4
VGER_L3ECLK<0>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<1>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<2>	200MHZ	4		::2545:2555	100		OUT 4
VGER_L3ECLK<3>	200MHZ	4		::2545:2555	100		OUT 4
L3_VREF<0>			10				OUT 4 20
L3_VREF<1>			10				OUT 4 20

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BT1	23	BATTERY
C1	19	CAP_P
C2	19	CAP_P
C3	25	CAP
C4	19	CAP_P
C5	25	CAP
C6	16	CAP
C7	16	CAP
C8	16	CAP
C9	16	CAP
C10	25	CAP
C11	25	CAP
C12	16	CAP
C13	16	CAP
C14	16	CAP
C15	16	CAP
C16	15	CAP
C17	15	CAP
C18	16	CAP
C19	16	CAP
C20	16	CAP
C21	16	CAP
C22	16	CAP
C23	16	CAP
C24	16	CAP
C25	16	CAP
C26	16	CAP
C27	16	CAP
C28	16	CAP
C29	16	CAP_P
C30	22	CAP_P
C31	28	CAP_P
C32	25	CAP
C33	25	CAP
C34	16	CAP
C35	16	CAP_P
C36	11	CAP
C37	11	CAP
C38	11	CAP
C39	11	CAP
C40	11	CAP
C41	12	CAP
C42	11	CAP
C43	11	CAP
C44	10	CAP
C45	16	CAP
C46	10	CAP
C47	9	CAP
C48	9	CAP
C49	9	CAP
C50	9	CAP
C51	9	CAP
C52	9	CAP
C53	9	CAP
C54	9	CAP
C55	12	CAP
C56	30	CAP_P
C57	30	CAP_P
C58	10	CAP
C59	9	CAP
C60	12	CAP
C61	12	CAP
C62	26	CAP_P
C63	11	CAP
C64	10	CAP
C65	9	CAP
C66	9	CAP
C67	28	CAP
C68	9	CAP
C69	12	CAP
C70	9	CAP
C71	9	CAP
C72	9	CAP
C73	11	CAP
C74	9	CAP
C75	9	CAP
C76	31	CAP
C77	30	CAP
C78	10	CAP
C79	9	CAP
C80	12	CAP
C81	11	CAP
C82	9	CAP
C83	29	CAP_P
C84	11	CAP
C85	11	CAP
C86	9	CAP
C87	9	CAP
C88	12	CAP
C89	29	CAP
C90	9	CAP
C91	10	CAP
C92	9	CAP
C93	11	CAP
C94	10	CAP

C95	10	CAP
C96	29	CAP
C97	31	CAP
C98	11	CAP
C99	11	CAP
C100	10	CAP
C101	10	CAP
C102	10	CAP
C103	9	CAP
C104	9	CAP
C105	9	CAP
C106	9	CAP
C107	9	CAP
C108	10	CAP
C109	10	CAP
C110	10	CAP
C111	29	CAP
C112	31	CAP
C113	11	CAP
C114	29	CAP
C115	29	CAP
C116	29	CAP
C117	32	CAP_P
C118	22	CAP_P
C119	22	CAP_P
C120	22	CAP_P
C121	31	CAP
C122	31	CAP
C123	32	CAP_P
C124	6	CAP
C125	29	CAP_P
C126	29	CAP
C127	29	CAP_P
C128	22	CAP_P
C129	22	CAP_P
C130	30	CAP
C131	28	CAP
C132	29	CAP
C133	22	CAP_P
C134	28	CAP
C135	22	CAP
C136	28	CAP_P
C137	22	CAP
C138	26	CAP_P
C139	26	CAP
C140	26	CAP
C141	8	CAP
C142	8	CAP
C143	26	CAP
C144	26	CAP
C145	23	CAP
C146	23	CAP
C147	27	CAP
C148	28	CAP
C149	23	CAP_P
C150	23	CAP
C151	23	CAP
C152	28	CAP_P
C153	28	CAP
C154	22	CAP
C155	22	CAP_P
C156	22	CAP
C157	23	CAP
C158	23	CAP
C159	27	CAP_P
C160	22	CAP_P
C161	27	CAP_P
C162	27	CAP_P
C163	22	CAP
C164	6	CAP
C165	22	CAP_P
C166	23	CAP
C167	22	CAP
C168	27	CAP_P
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D	?	?
SCALE NONE	SHT ? OF ?	

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D4	23	DIODE_SCHOT
D5	23	DIODE_SCHOT
D6	23	DIODE_SCHOT

D7	27	DIODE_SCHOT
D8	27	DIODE_SCHOT
D9	27	DIODE_SCHOT
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D12	30	DIODE_SCHOT_3P
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FL2	25	FILTER_LC
FL3	16	FILTER_CHOKE_DUAL
FL4	25	FILTER_LC
FL5	25	FILTER_LC
FL6	19	FILTER_12P
FL7	32	FILTER_12P
J1	15	CON_RJ45
J2	19	CON_F4RT_USB_UPRIGHT
J3	19	CON_F4RT_USB_UPRIGHT
J4	16	CON_FWVERT_SKT
J5	19	CON_F4RT_USB_UPRIGHT
J6	16	CON_FWVERT_SKT
J7	32	CON_F8RT_S_TH1
J8	25	CON_F14RT_D4MT_TH1
J9	30	CON_F5RT_S_2MT_TH1
J10	25	CON_F21RT_S2MT_SM
J11	13	CON_M4ST_LCK
J12	26	CON_M40SM_635
J13	26	CON_M26ST_SMBM
J14	26	CON_M40ST_NC20
J15	27	CON_M14ST_D_TH
J17	28	CON_M12ST_SM
J18	22	CON_M3ST_LCK
J19	6	CON_168ST_UDRM
J20	24	CON_F20SM_KX
J21	6	CON_144_33SM72
J22	26	CON_68_PCMCIA_FOXCN
J23	24	CON_F140SM_BTB
J24	26	CON_M2SM_DF13
J25	21	CON_M6ST_BTRY
J26	7	CON_F1ST_S2MT_SM
J27	18	CON_F1ST_S2MT_SM
J28	3	CON_F12RT_S2MT_SM
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R19	25	RES
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R22	25	RES
R23	25	RES

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT ? OF ?	

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R499	8	RES

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D	?	?
SCALE NONE	SHT ? OF ?	

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RP7	6	RPAK4P
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RP24	8	RPAK4P
RP25	17	RPAK4P
RP26	8	RPAK4P
RP27	17	RPAK4P
RP28	6	RPAK4P
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RP30	17	RPAK4P
RP31	6,8	RPAK4P
RP32	17	RPAK4P
RP33	8	RPAK4P
RP34	6	RPAK4P
RP35	7	RPAK4P
S1	28	SWI_4RTSA1_SMB
S2	28	SWI_4RTSA1_SMB
S3	26	SWI_4RTSA1_SMB
S4	23	SWI_TACT_4SM
S5	23	SWI_TACT
T1	15	XFR_100BT_MDIX
U1	9	VREG_TL431
U2	15	TRANSCEIVER_ENET_LXT971A
U3	11	SGRAM_2MX32
U4	32	AMP_TA2024
U5	29	TAS3001C
U6	5,6,8,13	PANGEA
U7	8	FEPR_1MX8
U8	23	M16C62
U9	7	74574
U10	22	VREG_LP2951
U11	23	VREG_TL431
U12	23	VDET_MC33465N_22ATR
U13	3,4	SCVGER483
U14	4	SRAM_DDR_153PBGA
U15	23	NC7SZ04
U16	18,25	74125
U17	16	FW802
U18	16	VREG_LP2951
U19	12	CLK_GEN_IMISM530
U20	29,30	OPAMP_TS924
U21	11	SGRAM_2MX32
U22	9,10,12	MONICA
U23	29	ADDAC_TLC320AD77C
U24	31	OPAMP_TS924
U25	29	VREG_LP2951
U26	29	VREG_LP2951
U27	31	ADC_CS5331
U28	23	MAX6328
U29	22	SWREG_LTC1735
U30	4	SRAM_DDR_153PBGA
U31	27	LTC1628
U32	21	VREG_LP2951
U33	7	CLK_GEN_IMIC5003
U35	21	AT90S1200
U36	21	EEPR_256X8
U38	19	SWI_TPS2023
VR1	22	VREG_EZ1582
VR2	22	VREG_EZ1582
VR3	22	VREG_EZ1582
VR4	21	VREG_EZ1582
VR5	28	VREG_EZ1582
XS1	31	STAR
XS2	30	STAR
XS3	29	STAR
XS4	32	STAR
XS5	29	STAR
XW1	28	SHORT
XW2	28	SHORT
XW3	31	SHORT
XW4	22	SHORT
XW5	27	SHORT
Y1	16	CRYSTAL
Y2	15	CRYSTAL
Y3	9	CRYSTAL
Y4	23	CRYSTAL
Y5	23	CRYSTAL_4PIN
Y6	18	CRYSTAL
Y7	12	CRYSTAL
Y8	7	CRYSTAL
ZH1	33	MTGHOLE
ZH2	33	MTGHOLE
ZH3	33	MTGHOLE
ZH4	28	MTGHOLE
ZH40	26	PCB_STANDOFF
ZH44	26	PCB_STANDOFF

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