CR-1

P72/73 (JUN 04 /2002)

BOMOPTION	P72 OASIS GOOD	P72 OASIS BETTER	P73 OASIS BEST	P72 MIRAGE GOOD	P72 MIRAGE BETTER	P73 MIRAGE BEST
DD1X	X	X	X	X	X	X
DD2X						
600MHZ	X			X		
700MHZ		X	X		X	X
OASIS	X	X	X			
MIRAGE				X	X	X
MID OR HIGH RANGE NO PWRSTEP	X	X	X	X	X	X
HIGH_PLL_RANGE_NO_PWRSTEP						
MID OR HIGH RANGE PWRSTEP						
HIGH PLL PANGE PWRSTEP						
LOW PLL RANGE						
LOW OR MID PLL RANGE	X	X	X	X	X	X
FIREWIRE	X	X	X	X	X	X
NO FIREWIRE						
PWRSTEP						
NO PWRSTEP	X	X	X	X	X	X
100MHZ	X	X	X	X	X	X
66MHZ						
3SBAT	X	X		X	X	
4SBAT			X			X
SWCHG						
HWCHG	X	X	X	X	X	X
OASIS_600	X					
OASIS_700		X	X			
MIRAGE_600				X		
MIRAGE_700					X	X
INTUSB	X	X	X	X	X	X
NON PRODUCTION						
SLOW_CHRG	X	X		X	X	
FAST_CHRG			X			X
128M	X	X	X	X	X	X
256M						
TBEN						

P. LEADER	APPROVED BY	CHECKED BY	PREPARED BY

PAGE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
REV	1.C	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.B	1.B	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	1.0	1.0	1.0
DATE	0604	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0312	0522	0522	0312	0312	0312	0604	0312	0312	0312	0312	0312	0312	0312
27	28	29	30	31	32	33	34	35	36	37	38	39	39	41	42	43	44	45	46	47	48	49	50	51	52	53
1.0	1.B	1.0	1.0	1.0	1.0	1.A	1.0	1.B	1.0	1.0	1.B	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.0	1.C	1.0	1.0	1.0	1.0	1.0
0312	0502	0312	0312	0312	0312	0402	0312	0522	0312	0312	0522	0312	0312	0312	0312	0312	0312	0312	0312	0312	0604	0312	0312	0312	0312	0312

P/N:820-1320
RFA # 222273
ATC P/N:KK0U22701110U02
ATC DRAWING NO.: U227-1-3-08

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DESCRIPTION:
iBook MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI:C ECS:1.C

SCALE: NONE | SHT 1 OF 53

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BLOCK DIAGRAM

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI:C ECS:1.0
SCALE: NONE	SHT 2 OF 53	

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U100 SAHARA 600MHZ BGA

CRITICAL
R800 4.7K 1% 1/16W MF 603

BVSEL
TDI
TDO
TMS
TCK
TRST*
LSSD_MODE*
L1_TSTCLK
L2_TSTCLK
ABB*
AP0
AP1
AP2
AP3
DBB*
DP0
DP1
DP2
DP3
DP4
DP5
DP6
DP7
DBDIS*
QREQ*
QACK*
CKSTP_IN*
CKSTP_OUT*
CLKOUT
TBEN
RSRV*
SMI*
TLBISYNC*
TA*
TEA*
INT*
MCP*
SRESET*
HRESET*
PLL_RANGE0
PLL_RANGE1
BLANK0
BLANK1
AGND
A1VDD
A2VDD
GND0 GND1 GND2 GND3 GND4 GND5 GND6 GND7 GND8 GND9 GND10 GND11 GND12 GND13 GND14 GND15 GND16 GND17 GND18 GND19 GND20 GND21 GND22 GND23 GND24 GND25
GND26 GND27 GND28 GND29 GND30 GND31 GND32 GND33 GND34 GND35 GND36 GND37 GND38 GND39 GND40 GND41 GND42 GND43 GND44 GND45 GND46 GND47 GND48 GND49 GND50 GND51 GND52 GND53 GND54 GND55 GND56 GND57 GND58 GND59
OVDD0 OVDD1 OVDD2 OVDD3 OVDD4 OVDD5 OVDD6 OVDD7 OVDD8 OVDD9 OVDD10 OVDD11 OVDD12 OVDD13 OVDD14 OVDD15 OVDD16 OVDD17 OVDD18 OVDD19 OVDD20 OVDD21 OVDD22 OVDD23 OVDD24 OVDD25 OVDD26 OVDD27 OVDD28 OVDD29 OVDD30 OVDD31
VDD0 VDD1 VDD2 VDD3 VDD4 VDD5 VDD6 VDD7 VDD8 VDD9 VDD10 VDD11 VDD12 VDD13 VDD14 VDD15 VDD16 VDD17 VDD18 VDD19 VDD20 VDD21 VDD22 VDD23 VDD24 VDD25 VDD26 VDD27 VDD28 VDD29 VDD30 VDD31
CPU_ADDR<0..31>
CPU_DATA<0..63>
TT0 TT1 TT2 TT3 TT4
TBST* TSIZ0 TSIZ1 TSIZ2 GBL* WT* CI* AACK* ARTRY* DRTRY* DBG* DBWO*
SYSCLK
PLL_CFG0 PLL_CFG1 PLL_CFG2 PLL_CFG3 PLL_CFG4

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2514	1	IC,SAHARA,1.2,700MHZ,1.5V CORE,85C,292 CBGA	U2	OASIS_700MHZ
337S2509	1	IC,SAHARA,1.2,600MHZ,1.5V CORE,85C,292 CBGA	U2	OASIS_600MHZ
337S2589	1	IC,SAHARA,1.2,700MHZ,1.5V CORE,85C,SFTO	U2	MIRAGE_700MHZ
337S2588	1	IC,SAHARA,1.2,600MHZ,1.5V CORE,85C,SFTO	U2	MIRAGE_600MHZ

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
113S1102	1	RES,FF,100 OHM 5%,1/16W,0603,SMD	R803	DD1X
113S1000	1	RES,FF,0 OHM 5%,1/16W,0603,SMD	R803	DD2X

+VIO_CPU_SLEEP
+VCORE_SLEEP
+2_5V_MAIN
+1_8V_MAIN
+3V_MAIN
+A1VDD_CPU_F_SLEEP
+A2VDD_CPU_F_SLEEP
+AVDD_CPU_SLEEP
+A1VDD_CPU_F_SLEEP
+A2VDD_CPU_F_SLEEP
PAN_QACK*
QACK*
POS_HRESET
CPU_HRESET*
CPU_CLK
SLEEP_L_LS

C1544 220UF 20% 4V POSCAP SMD
C1545 220UF 20% 4V POSCAP SMD
C803 10UF 20% 6.3V CERM 805
C804 10UF 20% 6.3V CERM 805
C805 10UF 20% 6.3V CERM 805
C770 0.1UF 20% 10V CERM 402
C806 0.1UF 20% 10V CERM 402
C807 0.1UF 20% 10V CERM 402
C808 0.1UF 20% 10V CERM 402
C809 0.1UF 20% 10V CERM 402
C810 0.1UF 20% 10V CERM 402
C811 0.1UF 20% 10V CERM 402
C812 0.1UF 20% 10V CERM 402
C813 0.1UF 20% 10V CERM 402
C814 0.1UF 20% 10V CERM 402
C815 0.1UF 20% 10V CERM 402
C816 0.1UF 20% 10V CERM 402
C817 0.1UF 20% 10V CERM 402
C818 0.047UF 10% 10V CERM 402
C819 0.047UF 10% 10V CERM 402
C820 0.01UF 20% 50V CERM 402
C821 0.01UF 20% 50V CERM 402
C822 0.01UF 20% 50V CERM 402
C823 0.01UF 20% 50V CERM 402
C824 0.001UF 20% 50V CERM 402
C825 0.001UF 20% 50V CERM 402
C826 0.001UF 20% 50V CERM 402
C827 0.001UF 20% 50V CERM 402
C828 0.001UF 20% 50V CERM 402
C829 0.001UF 20% 50V CERM 402
C830 0.001UF 20% 50V CERM 402
C831 0.001UF 20% 50V CERM 402
C832 220PF 5% 25V CERM 402
C833 220PF 5% 25V CERM 402
C834 220PF 5% 25V CERM 402
C835 220PF 5% 25V CERM 402
C898 0.1UF 20% 10V CERM 402
C899 0.1UF 20% 10V CERM 402
C883 0.1UF 20% 10V CERM 402
C886 0.1UF 20% 10V CERM 402
C897 0.01UF 20% 50V CERM 402
C887 0.01UF 20% 50V CERM 402
C895 0.01UF 20% 50V CERM 402
C771 0.1UF 20% 10V CERM 402
C980 10UF 20% 6.3V CERM 805
C772 0.1UF 20% 10V CERM 402
C776 0.1UF 20% 10V CERM 402
C774 0.01UF 20% 50V CERM 402
C775 0.01UF 20% 50V CERM 402
C777 0.01UF 20% 50V CERM 402
C836 220UF 20% 4V POSCAP SMD
C800 100UF 20% 6.3V CERM 1812 NOSTUFF
C801 100UF 20% 6.3V CERM 1812 NOSTUFF
C981 10UF 20% 6.3V CERM 805
C837 100UF 20% 10V TANT SMD-1
C838 1.0UF N20P80% 16V CERM 805
C839 1.0UF N20P80% 16V CERM 805
C840 0.1UF 20% 10V CERM 402
C841 0.1UF 20% 10V CERM 402
C842 0.1UF 20% 10V CERM 402
C843 0.1UF 20% 10V CERM 402
C844 0.1UF 20% 10V CERM 402
C845 0.1UF 20% 10V CERM 402
C846 0.1UF 20% 10V CERM 402
C847 0.1UF 20% 10V CERM 402
C848 0.1UF 20% 10V CERM 402
C849 0.1UF 20% 10V CERM 402
C850 0.1UF 20% 10V CERM 402
C851 0.1UF 20% 10V CERM 402
C852 0.1UF 20% 10V CERM 402
C853 0.1UF 20% 10V CERM 402
C854 0.1UF 20% 10V CERM 402
C855 0.1UF 20% 10V CERM 402
C856 0.047UF 10% 10V CERM 402
C857 0.047UF 10% 10V CERM 402
C858 0.047UF 10% 10V CERM 402
C859 0.047UF 10% 10V CERM 402
C860 0.01UF 20% 50V CERM 402
C861 0.01UF 20% 50V CERM 402
C862 0.01UF 20% 50V CERM 402
C863 0.01UF 20% 50V CERM 402
C864 0.001UF 20% 50V CERM 402
C865 0.001UF 20% 50V CERM 402
C866 0.001UF 20% 50V CERM 402
C867 0.001UF 20% 50V CERM 402
C868 0.001UF 20% 50V CERM 402
C869 0.001UF 20% 50V CERM 402
C870 0.001UF 20% 50V CERM 402
C871 0.001UF 20% 50V CERM 402
C884 0.1UF 20% 10V CERM 402
C888 0.1UF 20% 10V CERM 402
C890 0.1UF 20% 10V CERM 402
C891 0.1UF 20% 10V CERM 402
C892 0.1UF 20% 10V CERM 402
C894 0.1UF 20% 10V CERM 402
C889 0.01UF 20% 50V CERM 402
C893 0.01UF 20% 50V CERM 402
C885 0.001UF 20% 50V CERM 402
C778 0.1UF 20% 10V CERM 402
C779 0.1UF 20% 10V CERM 402
C780 0.1UF 20% 10V CERM 402
C781 0.1UF 20% 10V CERM 402
C782 0.01UF 20% 50V CERM 402
C783 0.01UF 20% 50V CERM 402
C784 0.1UF 20% 16V CERM 603
C786 0.1UF 20% 16V CERM 603
C872 0.1UF 20% 10V CERM 402
C873 10UF 20% 6.3V TANT SMA
C874 0.1UF 20% 10V CERM 402
C875 0.01UF 20% 50V CERM 402
C876 0.1UF 20% 10V CERM 402
C877 10UF 20% 6.3V TANT SMA
C878 0.1UF 20% 10V CERM 402
C879 0.01UF 20% 50V CERM 402
C880 20PF 10% 16V CERM 603
R801 2 5% 1/16W MF 603
R802 2 5% 1/16W MF 603
R803 100 5% 1/16W MF 603 OMIT
R804 100K 5% 1/16W MF 603 DD1X
R805 4.7K 5% 1/10W MF 603 DD1X
R806 47 1% 1/16W MF 603
R1113 15K 1% 1/16W MF 603
R1114 68.1K 1% 1/16W MF 603
L800 100-OHM-EMI SM
L801 100-OHM-EMI SM
U103 LTC1701ES5-50 SOT-23
Q800 2N7002 SM DD1X
Q801 2N3904 SM DD1X

PLACE CLOSE TO SAHARA
PLACE CLOSE TO PANGEA
PLACE AFTER PROCESSOR CLOCK INPUT
KEEP STUB SHORT!
KEEP ROUTE ON INTERNAL LAYER
QACK* HIGH IS 32-BIT BUS MODE
QACK* LOW IS 64-BIT BUS MODE
SAMPLED AT CPU_HRESET*

PROCESSOR

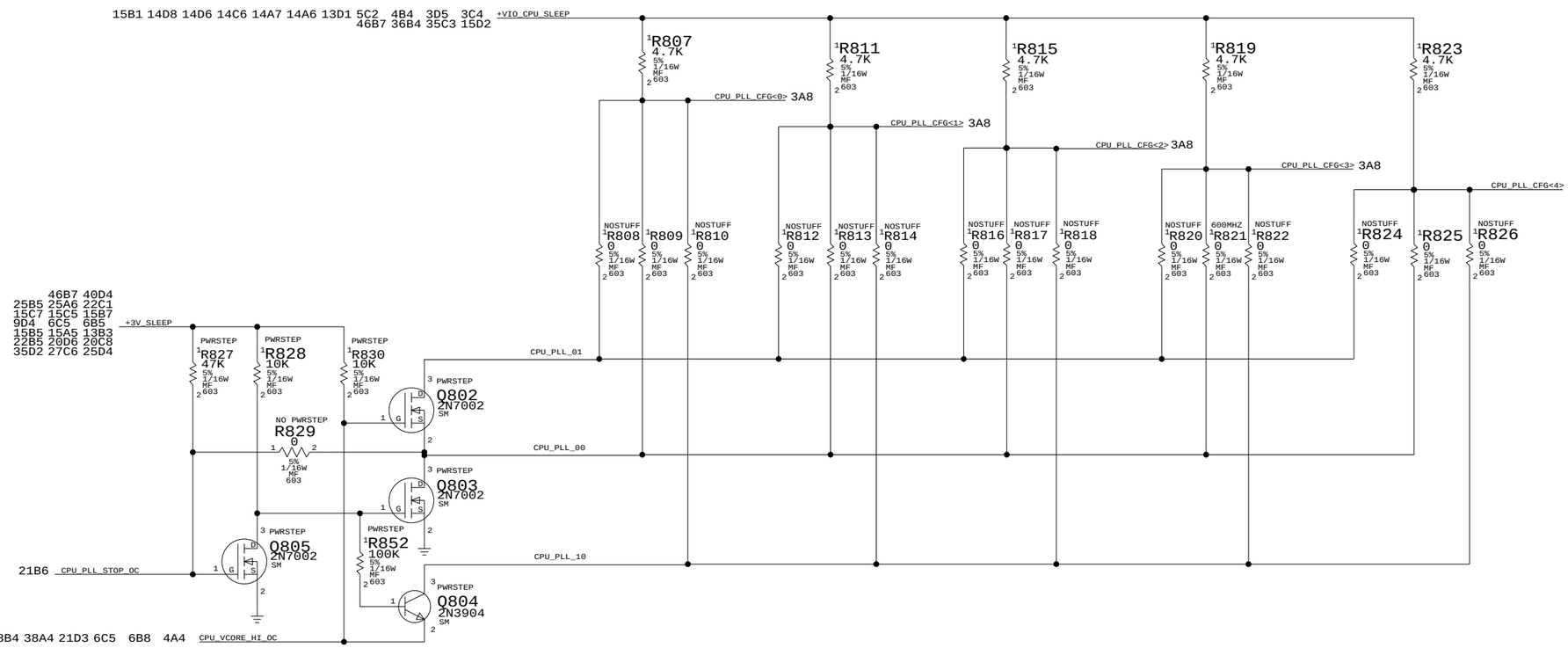
DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.B
SCALE NONE | SHT 3 OF 53

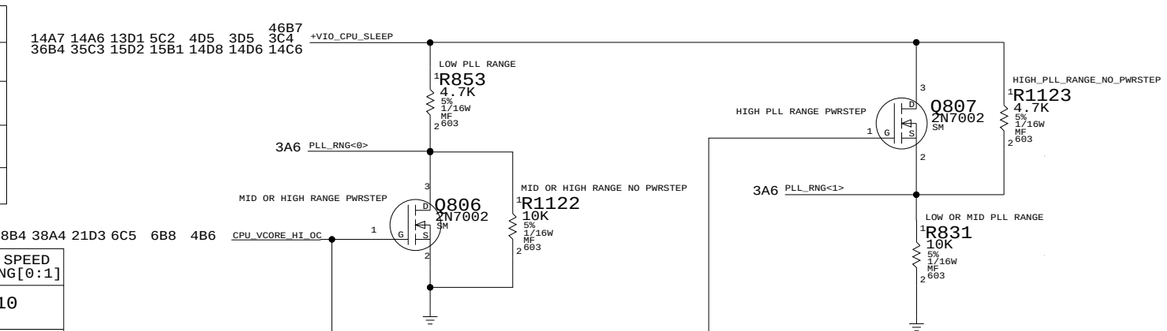
STATE ENCODING	CPU_VCORE_HI_OC	CPU_PLL_STOP_OC
HIGH SPEED	1	0
LOW SPEED	0	0
PLL OFF	X	1

BUS SPEED		66	100
CPU_PLL_CFG[0:4]	CORE:BUS RATIO		
00000	OFF		
00001	OFF		
00010	PLL BYPASS		
00011	PLL BYPASS		
00100	2.0:1	N/A	N/A
00101	2.5:1	N/A	N/A
00110	3.0:1	N/A	N/A
00111	3.5:1	N/A	N/A
01000	4.0:1	N/A	N/A
01001	4.5:1	N/A	N/A
01010	5.0:1	N/A	500
01011	5.5:1	N/A	550
01100	6.0:1	N/A	600
01101	6.5:1	N/A	650
01110	7.0:1	N/A	700
01111	7.5:1	500	750
10000	8.0:1	533	800
10001	8.5:1	567	850
10010	9.0:1	600	900
10011	9.5:1	633	950
10100	10.0:1	667	1000
10101	11.0:1	733	N/A
10110	12.0:1	800	N/A
10111	13.0:1	867	N/A
11000	14.0:1	933	N/A
11001	15.0:1	1000	N/A
11010	16.0:1	N/A	N/A
11011	17.0:1	N/A	N/A
11100	18.0:1	N/A	N/A
11101	19.0:1	N/A	N/A
11110	20.0:1	N/A	N/A
11111	OFF		



PLL_RNG[0:1]	PLL FREQUENCY RANGE
00	500-750 MHZ
01	750-1200 MHZ
10	UP TO 500 MHZ
11	RESERVED

SYSTEM	LOW SPEED PLL_RNG[0:1]	HIGH SPEED PLL_RNG[0:1]
LOW RANGE ONLY	10	10
LOW TO MID RANGE	10	00
LOW TO HIGH RANGE	10	01



CPU PLL CONFIGURATION

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 4 OF 53	

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PANGEA CORE

22B1 16D4 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3
8D6 8D4 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 3A4
13B8 13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7
21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4
46B7 40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4

+3V_MAIN — R296 10 5% 1/16W MF 603 — MA=34MA

40C6 +3V_AVDD5_PANGEA_MAIN
A15 4.7UF N20P80% 10V CERM 805
C308 0.01UF 20% 50V CERM 603

AJ5 AVDD5

CRITICAL PROJECT

U4 PANGEA (1 OF 6) PBGA

MAXBUS INTERFACE

41D1 14C8 3D8	CPU_BR*	AP16	BR		
41A1 14C6 3D8	CPU_BG*	AH19	BG		
41D1 14C8 3D8	TS*	AN14	TS		
41A1 5D7 5C7 3D8 3C8 41C1 41B1	CPU_ADDR<0..31>				
41C1 5D7 3D8	CPU_ADDR<0>	AK23	A_0		
41C1 5D7 3D8	CPU_ADDR<1>	AP27	A_1		
41C1 5D7 3D8	CPU_ADDR<2>	AP28	A_2		
41C1 5D7 3D8	CPU_ADDR<3>	AN26	A_3		
41C1 5D7 3D8	CPU_ADDR<4>	AK24	A_4		
41C1 5D7 3D8	CPU_ADDR<5>	AN24	A_5		
41C1 5D7 3D8	CPU_ADDR<6>	AM26	A_6		
41C1 5D7 3D8	CPU_ADDR<7>	AJ23	A_7		
41C1 5D7 3D8	CPU_ADDR<8>	AM24	A_8		
41C1 5D7 3D8	CPU_ADDR<9>	AH23	A_9		
41C1 5D7 3D8	CPU_ADDR<10>	AM23	A_10		
41C1 5D7 3D8	CPU_ADDR<11>	AN23	A_11		
41B1 5D7 3D8	CPU_ADDR<12>	AJ22	A_12		
41B1 5D7 3D8	CPU_ADDR<13>	AN22	A_13		
41B1 5D7 3D8	CPU_ADDR<14>	AP26	A_14		
41B1 5D7 3D8	CPU_ADDR<15>	AP21	A_15		
41B1 5D7 3D8	CPU_ADDR<16>	AH22	A_16		
41B1 5D7 3D8	CPU_ADDR<17>	AM21	A_17		
41B1 5D7 3D8 3C8	CPU_ADDR<18>	AJ21	A_18		
41B1 5D7 3D8 3C8	CPU_ADDR<19>	AK20	A_19		
41B1 5D7 3D8 3C8	CPU_ADDR<20>	AK21	A_20		
41B1 5D7 3D8 3C8	CPU_ADDR<21>	AN25	A_21		
41B1 5D7 3D8 3C8	CPU_ADDR<22>	AP24	A_22		
41B1 5D7 3D8 3C8	CPU_ADDR<23>	AP25	A_23		
41B1 5D7 3D8 3C8	CPU_ADDR<24>	AH20	A_24		
41B1 5D7 3D8 3C8	CPU_ADDR<25>	AH21	A_25		
41B1 5D7 3D8 3C8	CPU_ADDR<26>	AP23	A_26		
41B1 5D7 3D8 3C8	CPU_ADDR<27>	AM20	A_27		
41B1 5D7 3D8 3C8	CPU_ADDR<28>	AJ20	A_28		
41A1 5D7 3D8 3C8	CPU_ADDR<29>	AN21	A_29		
41A1 5D7 3D8 3C8	CPU_ADDR<30>	AJ19	A_30		
41A1 5D7 3D8 3C8	CPU_ADDR<31>	AP22	A_31		
41A1 14B6 3B8	CI*	AJ25	CI		
41A1 14C8 3C8	GBL*	AP29	GBL		
41D1 14C8 3C8	TBST*	AN28	TBST		
41C1 3C8	TSIZ<0>	AP30	TSIZ_0		
41C1 3C8	TSIZ<1>	AN29	TSIZ_1		
41C1 3C8	TSIZ<2>	AH25	TSIZ_2		
41D1 3C8	TT<0>	AK27	TT_0		
41D1 3C8	TT<1>	AP31	TT_1		
41C1 3C8	TT<2>	AN30	TT_2		
41C1 3C8	TT<3>	AM29	TT_3		
41C1 3C8	TT<4>	AH26	TT_4		
41A1 14B6 3B8	WT*	AK26	WT		
41D1 14B6 3B8	AACK*	AN20	AACK		
41D1 14A8 3B8	ARTRY*	AP14	ARTRY		
14A8	HIT* (NOT USED BY CPU)	AN16	HIT		
41D1 14C8 3A6	QREQ*	AN15	QREQ		
41D1 14B6 3A4	PAN_QACK*	AJ26	QACK		
	PANGEA_SUS_REQ_IN*	AJ32	SUSPENDREQ		
21B5	PANGEA_SUSP_ACK*	AJ33	SUSPENDACK		
		AK5	CPU_FB_IN		
		AL2	CPU_FB_OUT		
		AM34	STOPCPUCLK		
		AM30	ACS_REF		
43C4	PANGEA_CPU_CLK	AM1	CPU_CLK		
		AJ18	DBG*	3B8	14A8 41A1
		AP15	DRDY* (DRDRY NOT USED BY CPU)	14A8	
		AH24	DBWO*	3B8	14D6 41D1
	DTI<1>	AM27	DTI_1		
	DTI<2> (DTI<1..2> CAN BE OPEN FOR A G3)	AN27	DTI_2		
		AJ24	TA*	3A6	14C8 41D1
		AP20	TEA*	3A6	14B8 41D1

DTI<1..2> NOT USED BY CPU

41D5 5D3 3B8 3B6	D_0	AJ15	CPU_DATA<0>	3B8 3B6 41D5	0
	D_1	AK6	CPU_DATA<1>		1
	D_2	AJ9	CPU_DATA<2>		2
41D5 5D3 3B8 3B6	D_3	AK14	CPU_DATA<3>	3B8 3B6 41D5	3
41D5 5D3 3B8 3B6	D_4	AM6	CPU_DATA<4>	41D5	4
41D5 5D3 3B8 3B6	D_5	AH12	CPU_DATA<5>	3B8 3B6 41D5	5
	D_6	AM11	CPU_DATA<6>	41D5	6
	D_7	AN18	CPU_DATA<7>		7
41D5 5D3 3B8 3B6	D_8	AM18	CPU_DATA<8>	3B8 3B6 41D5	8
41D5 5D3 3B8 3B6	D_9	AJ16	CPU_DATA<9>	41D5	9
	D_10	AK8	CPU_DATA<10>	3B8 3B6 41D5	10
41D5 5D3 3B8 3B6	D_11	AH16	CPU_DATA<11>	41D5	11
	D_12	AH8	CPU_DATA<12>		12
	D_13	AM14	CPU_DATA<13>	3B8 3B6 41C5	13
41C5 5D3 3B8 3B6	D_14	AP3	CPU_DATA<14>	41C5	14
	D_15	AJ10	CPU_DATA<15>	3B8 3B6 41C5	15
41C5 5D3 3B8 3B6	D_16	AN4	CPU_DATA<16>	41C5	16
	D_17	AJ12	CPU_DATA<17>		17
	D_18	AM9	CPU_DATA<18>	3B8 3B6 41C5	18
41C5 5D3 3B8 3B6 3A8	D_19	AN13	CPU_DATA<19>	41C5	19
	D_20	AK12	CPU_DATA<20>		20
	D_21	AK15	CPU_DATA<21>		21
	D_22	AM12	CPU_DATA<22>		22
	D_23	AP4	CPU_DATA<23>		23
	D_24	AH13	CPU_DATA<24>		24
	D_25	AP5	CPU_DATA<25>		25
	D_26	AH15	CPU_DATA<26>		26
	D_27	AN5	CPU_DATA<27>		27
	D_28	AN6	CPU_DATA<28>		28
	D_29	AP6	CPU_DATA<29>		29
	D_30	AJ13	CPU_DATA<30>		30
	D_31	AM15	CPU_DATA<31>		31
	D_32	AJ17	CPU_DATA<32>		32
	D_33	AN12	CPU_DATA<33>		33
	D_34	AN19	CPU_DATA<34>		34
	D_35	AN17	CPU_DATA<35>		35
	D_36	AN11	CPU_DATA<36>		36
	D_37	AH17	CPU_DATA<37>		37
	D_38	AN10	CPU_DATA<38>		38
	D_39	AK17	CPU_DATA<39>		39
	D_40	AN9	CPU_DATA<40>		40
	D_41	AP19	CPU_DATA<41>		41
	D_42	AM17	CPU_DATA<42>		42
	D_43	AM8	CPU_DATA<43>		43
	D_44	AJ11	CPU_DATA<44>		44
	D_45	AK18	CPU_DATA<45>		45
	D_46	AH14	CPU_DATA<46>		46
	D_47	AM5	CPU_DATA<47>		47
	D_48	AH11	CPU_DATA<48>		48
	D_49	AK9	CPU_DATA<49>		49
	D_50	AJ8	CPU_DATA<50>		50
	D_51	AJ14	CPU_DATA<51>		51
	D_52	AK11	CPU_DATA<52>		52
	D_53	AH9	CPU_DATA<53>		53
	D_54	AH10	CPU_DATA<54>		54
	D_55	AP10	CPU_DATA<55>		55
	D_56	AP12	CPU_DATA<56>		56
	D_57	AP8	CPU_DATA<57>		57
	D_58	AP9	CPU_DATA<58>		58
	D_59	AP13	CPU_DATA<59>		59
	D_60	AP11	CPU_DATA<60>		60
	D_61	AN7	CPU_DATA<61>		61
	D_62	AN8	CPU_DATA<62>		62
5D3 5B3 3B8	D_63	AP7	CPU_DATA<63>	3B7 3B6 41A5	63

CPU_DATA<0..63> 3A8 3B6 3B7 3B8 3C7 5B3 5B4 5C4 5D4 41A5 41B5 41C5 41D5

5D3 3B8 3B6 3B7 5B4 41A5 CPU_DATA<63>

+VIO_CPU_SLEEP 3C4 3D5 4B4 4D5 13D1 14A6 14A7 14C6 14D6 14D8 15B1 15D2 35C3 36B4 46B7

R75 4.7K 5% 1/16W MF 603
NOSTUFF R293 4.7K 5% 1/16W MF 603

NOTE: USE 10 MILS 40OHM TRACE

43C4	CPUFB4	R65 0	SHORT STUBS	CPUFB3	R287 0
	CPUFB2	R70 0	SHORT STUBS	CPUFB1	R292 0
	CPUFBIN	5B8 43C4			
		NOSTUFF R67 0			NOSTUFF R288 0
		NOSTUFF R76 0			NOSTUFF R290 0
		R66 0	43C4 CPUFB5		R286 0
		R71 0	43C4 CPUFB6		R289 0
			CPUFB7		TCPUFBOUT 6C5 43C4

All 5% 1/16W MF 603 unless noted.

2" longer (0.5 ns longer)	1" longer (0.2 ns longer)	MAX-BUS" (zero delay)	1" shorter (0.2ns faster)	2" shorter (0.5 ns faster)

DELAY LENGTHS:

ROUTE DELAY NETWORK ON INTERNAL LAYER

R302 0 5% 1/16W MF 603
PANGEA_SUSP_REQ* — 1 — 2 — 5B1 43C4 CPUFBIN

R613 33 5% 1/16W MF 603
43B4 6D8 FBOUT_CLK — 1 — 2
NOSTUFF C305 20pF 10% 50V CERM 603

43C4 TP20 A — 1 PANGEA_CPU_CLK

Series R on CPU_CLK work with shunt
R to drop voltage to 1.8V/2.5V

21C3 CPU_STOP_CLK* — R73 0 5% 1/16W MF 603 — PANGEA_STOPCPUCLK

40C4 PANGEA_ACS_REF — R298 1K 1% 1/16W MF 603 (2.4MA)

AVSS5 AG7

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0557	1	RFA-127675,PANGEA,PBGA-34X34-100	U4	PROJECT	

Pangea Processor IF

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE	SHT	OF
NONE	5	53

CR-6

PANGEA CORE

SPREAD SPECTRUM CLOCK GENERATOR

+3V_CLKGEN_AVDD_SLEEP
+3V_CLKGEN_SLEEP

U801 CY28507 TSSOP
VDD VDDL AVDD
XIN CLKA
CLKSEL CLKB
OEDE CLKC
OE CLKD
XOUT CLKE
AVSS VSSL VSS

FBOUT_CLK
CLKSEL
OEDE
STOPXTAL*

28507_CLK5
28507_CLK3
28507_CLK4
28507_CLK2
28507_CLK1

R847 0 MCLK<1> 42D1 8B4 TO SODIMM BANKA CLOCK
R848 4.7K
R843 0 MCLK<0> 7A2 7A4 7C2 7C4 42D1 TO ON BOARD SDRAM CLOCK BANK0
R844 4.7K
R845 27 574_CLK 7B8 43B4 TO LVT574 CLOCK
R846 10 LACLK 20B6 TO J9 (LA I/F) CLOCK
R841 0 MCLK<3> 8C5 42D1 TO SODIMM BANKB CLOCK
R842 4.7K

R837 22.1 CPU_CLK 3A4 TO CPU CLOCK
CPU HAS A BUILT IN PULLDOWN.
R838 10 TBENDIVCLK 6B8 43B4 TO TBEN DIVIDE BY 3
R839 10 TCPUFBOUT 5B1 43C4 TO PANGEA FEEDBACK CLOCK
R840 4.7K

R850 22 TBEN
R849 47

PLACE NEAR SAHARA

TBEN DIVIDE 3 CIRCUIT

+3V_CLKGEN_SLEEP
C1100 0.1UF 20% 10V CERM 402
U802 74LVC109 TSSOP (J /K /PR /CLR /Q)
J_TO_Q* TBENDIVCLK CPU_VCORE_HI_OC TBEN GND

R307 4.7K NOSTUFF PMU_IIC_CLK
R204 4.7K NOSTUFF PMU_IIC_DAT
R835 0 TBEN CPU_VCORE_HI_OC
R1118 10K +3V_CLKGEN_SLEEP OEDE
R1119 10K +3V_CLKGEN_SLEEP CLKSEL 6D8
PLACE CLOSE TO U40
PMU NOT RATED STRONG ENOUGH FOR 1K

L80 400-OHM-EMI SM-1
C650 0.1UF 20% 10V CERM 402
C651 2.2UF N20P80% 10V CERM 805
C652 0.001UF 20% 50V CERM 402
C653 0.1UF 20% 10V CERM 402
C654 0.1UF 20% 10V CERM 402
C655 0.1UF 20% 10V CERM 402
C656 0.1UF 20% 10V CERM 402

L81 400-OHM-EMI SM-1
C657 0.1UF 20% 10V CERM 402
C658 0.1UF 20% 10V CERM 402
C660 0.001UF 20% 50V CERM 402
C661 2.2UF N20P80% 10V CERM 805
C662 0.1UF 20% 10V CERM 402

A BYPASS CAPACITOR 0.1UF SHOULD BE PLACED AS CLOSE AS POSSIBLE TO EACH VDD/AVDD PIN.

R308 10 +3V_MAIN MA=TBD
C324 0.01UF 20% 50V CERM 603
A59 1UF 20% 10V CERM 805
40C6 +3V_AVDD4_PANGEA_MAIN

U4 PANGEA (2 OF 6) PBGA
AVDD4 AG2
RAMDATA_0 .. RAMDATA_63 AG1 AF3 AF1 AE2 AE1 AD2 AD1 AC2 Y1 Y2 W1 W2 V2 U2 T1 T2 R1 R2 P3 P2 N1 N2 M1 M2 J2 H2 G1 G2 F1 F2 E1 H3 AD3 AD5 AC3 AC5 AC6 AC7 AB6 AB7 AA5 AA6 AA7 AC1 V3 V5 V6 W7 U3 U5 U6 U7 R6 R7 P5 P6 L6 L7 K6 K7 J3 J5 J6 J7
MDATA<0> .. MDATA<63>
MEMORY INTERFACE
M_ADDR<0> .. M_ADDR<12> AB2 AA2 Y3 Y7 W6 Y5 M6 L1 N6 L2 K1 K2 M7 T6
M_BA0 N7 M_BA1 M6
SDCS_0 M3 SDCS_1 M5 SDCS_2 R3 SDCS_3 P7
SDDQM_0 AA1 SDDQM_1 AB1 SDDQM_2 J1 SDDQM_3 H1 SDDQM_4 Y6 SDDQM_5 AA3 SDDQM_6 L3 SDDQM_7 L5
SDRAS P1 SDCAS T7 SDWE H5 SDCKE0 D1 SDCKE1 R5
ROMCS AA34 ROMOE Y32 ROMRW Y30
MCLK_0 AK1 MCLK_1 AJ3 MCLK_2 AG5 MCLK_3 AH2 MCLK_4 AF5 MCLK_5 AE6 MCLK_6 AJ1 MCLK_7 AK3
PANGEAMCLK<0> PANGEAMCLK<1> PANGEAMCLK<2> PANGEAMCLK<3> PANGEAMCLK<6>
TP21 TP22 TP23 TP24 TP25
KEEP CLOCK ROUTES ON INTERNAL LAYERS
NO TEST POINT ON PANGEAMCLK<4.5.7>
40C4 SD_REF F3 PANGEA_SD_REF
R347 1K 1% (8.1MA)
AVSS4 AG3

RP'S CAN BE RE-PINNED

RP7 RP9 RP20 RP22 RP23 22 (SM)
M_ADDR<0> .. M_ADDR<12>
TERM_M_ADDR<0> .. TERM_M_ADDR<12>
T_ROMWE* T_ROMOE* T_ROMCS* T_M_BA1 T_M_BA0 T_SDRAS* T_SDCAS* T_MEMWE*
ROMRW* ROMOE* ROMCS* M_BA1 M_BA0 SDRAS* SDCAS* MEMWE*
R321 R310 R89 R318 R313 R88 10K
RP22 10 T1CS0* T1CS1* T1CS2* T1CS3* CS0* CS1* CS2* CS3*

RP'S CAN BE RE-PINNED WITHIN GROUP

DO NOT REPIN
CS R-PACKS
CS0-3 ARE CRITICAL TIMING NETS
MAKE AS SHORT AS POSSIBLE

TERMINATIONS:
20-OHM TO FIRST DIMM
(PLACE NEAR PANGEA)

SPLIT NETS AT BGA, 10-OHM SERIES TERM, ROUTE ON SIDE OPPOSITE PANGEA FOR LOWEST IMPEDANCE PATH.

PANGEA SDRAM & SO-DIMMS I/F

DESCRIPTION: ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0
SCALE NONE | SHT 6 OF 53

8A4 7D1 7C3 7C1 7B1 7A3 7A1 6D4 6D3 6C3 42D5 6B3 8A5
42C5 42B5 42A5 8D5 8B5 8C5 8C4
8B5 8B4 7D4 7D2 7C4 7C2 7B4 7B2 7A4 6B7 6A7
42B1 8C5 8C4

MDATA<63..0>

TERM_M_ADDR<12..0>

DISTRIBUTE CAPS EVENLY AMONG THE SDRAM PADS

+3V_MAIN

C270 0.1UF N20P80% 16V CERM 603
C268 0.01UF 20% 50V CERM 603
C300 0.001UF 20% 50V CERM 603
C267 0.1UF N20P80% 16V CERM 603

U16 OMIT SDRAM-2MX16X4 100MHZ TSOP CRITICAL

42B1 8C5 7D5 7D2 7B4 7B2 6B7	A0	23	TERM_M_ADDR<0>		
	A1	24	TERM_M_ADDR<1>		
	A2	25	TERM_M_ADDR<2>		
	A3	26	TERM_M_ADDR<3>		
	A4	29	TERM_M_ADDR<4>		
	A5	30	TERM_M_ADDR<5>		
	A6	31	TERM_M_ADDR<6>		
	A7	32	TERM_M_ADDR<7>		
	A8	33	TERM_M_ADDR<8>		
	A9	34	TERM_M_ADDR<9>		
	A10	22	TERM_M_ADDR<10>		
	A11	35	TERM_M_ADDR<11>		
	A12	36	TERM_M_ADDR<12>		
43D5 8B4 7C2 7B2 7A4 6A6	BA0	21	T_M_BA0		
43D5 8B4 7C2 7A4 7A2 6A6	BA1	20	T_M_BA1		
43C1 7A4 6A5 7A2 7C2 8C5	CS	19	T1CS0*		
	RAS	18	T_SDRAS*		
	CAS	17	T_SDCAS*		
43D1 6C2 8C5	WE	16	T_MEMWE*		
	LDQM	15	DQM0*		
	UDQM	39	DQM1*		
	CLK	38	MCLK<0>		
	CKE	37	T_RAM_CKE0_MLB		
	VSS	28			
	VSSQ	41			
		54			
		6			
		12			
		46			
		52			
42D5 8D5 7D5 6D3 6D4	DQ0	2	MDATA<0>	0	
	DQ1	4	MDATA<1>	1	
	DQ2	5	MDATA<2>	2	
	DQ3	7	MDATA<3>	3	
	DQ4	8	MDATA<4>	4	
	DQ5	10	MDATA<5>	5	
	DQ6	11	MDATA<6>	6	
	DQ7	13	MDATA<7>	7	
	DQ8	42	MDATA<8>	8	
	DQ9	44	MDATA<9>	9	
	DQ10	45	MDATA<10>	10	
	DQ11	47	MDATA<12>	11	
	DQ12	48	MDATA<12>	12	
	DQ13	50	MDATA<13>	13	
	DQ14	51	MDATA<14>	14	
6C3 6D4 7D5 8C5 42C5	DQ15	53	MDATA<15>	15	

+3V_MAIN

C335 0.1UF N20P80% 16V CERM 603
C334 0.01UF 20% 50V CERM 603
C299 0.01UF 20% 50V CERM 603
C224 0.001UF N20P80% 16V CERM 603

U20 OMIT SDRAM-2MX16X4 100MHZ TSOP CRITICAL

42B1 8C5 7D5 7D4 7B4 7B2 6B7	A0	23	TERM_M_ADDR<0>		
	A1	24	TERM_M_ADDR<1>		
	A2	25	TERM_M_ADDR<2>		
	A3	26	TERM_M_ADDR<3>		
	A4	29	TERM_M_ADDR<4>		
	A5	30	TERM_M_ADDR<5>		
	A6	31	TERM_M_ADDR<6>		
	A7	32	TERM_M_ADDR<7>		
	A8	33	TERM_M_ADDR<8>		
	A9	34	TERM_M_ADDR<9>		
	A10	22	TERM_M_ADDR<10>		
	A11	35	TERM_M_ADDR<11>		
8B4 7A4 6A6 7B2 7C4 43D5	A12	36	TERM_M_ADDR<12>		
	BA0	21	T_M_BA0		
	BA1	20	T_M_BA1		
7A2 8C5 6A6 7A4 6C2 43D1 8B5	CS	19	T1CS0*		
	RAS	18	T_SDRAS*		
	CAS	17	T_SDCAS*		
	WE	16	T_MEMWE*		
	LDQM	15	DQM2*		
	UDQM	39	DQM3*		
	CLK	38	MCLK<0>		
	CKE	37	T_RAM_CKE0_MLB		
	VSS	28			
	VSSQ	41			
		54			
		6			
		12			
		46			
		52			
42C5 8B5 7D5 6D4 6C3	DQ0	2	MDATA<16>	16	
	DQ1	4	MDATA<17>	17	
	DQ2	5	MDATA<18>	18	
	DQ3	7	MDATA<19>	19	
	DQ4	8	MDATA<20>	20	
	DQ5	10	MDATA<21>	21	
	DQ6	11	MDATA<22>	22	
	DQ7	13	MDATA<23>	23	
	DQ8	42	MDATA<24>	24	
	DQ9	44	MDATA<25>	25	
	DQ10	45	MDATA<26>	26	
	DQ11	47	MDATA<27>	27	
	DQ12	48	MDATA<28>	28	
	DQ13	50	MDATA<29>	29	
	DQ14	51	MDATA<30>	30	
	DQ15	53	MDATA<31>	31	

ON BOARD MEMORY

66MHZ R575 22 5% 1/16W MF 603
66MHZ R562 22 5% 1/16W MF 603
100MHZ L70 400-OHM-EMI SM-1
100MHZ C604 0.1UF N20P80% 16V CERM 603
100MHZ C618 0.01UF 20% 50V CERM 603
100MHZ C619 1000PF 5% 25V CERM 603
66MHZ R564 0 5% 1/16W MF 603
66MHZ R573 0 5% 1/16W MF 603
100MHZ R355 22 5% 1/16W MF 603
100MHZ R604 100K 5% 1/16W MF 603
100MHZ R560 22 5% 1/16W MF 603
100MHZ R561 22 5% 1/16W MF 603
100MHZ R354 22 5% 1/16W MF 603
100MHZ R334 22 5% 1/16W MF 603
66MHZ R574 0 5% 1/16W MF 603
100MHZ R605 100K 5% 1/16W MF 603
100MHZ R606 100K 5% 1/16W MF 603
66MHZ R563 22 5% 1/16W MF 603

46B7 40D6 36C6 35D4 35B5 35B3 28C5 26D6 25B4 22B1 21D7 21C7 21C3 20C2 20B3 19C3 18C7 18B6 18A4 16D4 15D3 15C2 14D2 14C3 14B3 13D6 13C8 8B6 7D4 7D2 7B4 7B2 6D4 6B5 5D6 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D4 13B8 11C8 13A8 13C3 15D7 20C3 34B2 8D4

+3V_MAIN

6C2 43C1 RAM_CKE0
6C2 43C1 RAM_CKE1
T_RAM_CKE0_L
T_RAM_CKE1_L
T_RAM_CKE0_MLB_R
T_RAM_CKE0_R
T_RAM_CKE1_R
T_RAM_CKE0
T_RAM_CKE1
TO SODIMM 8C4
TO SODIMM 8C4

100MHZ 20 VCC U35 74LVT574 TSSOP
D1 D2 D3 D4 D5 D6 D7 D8 CLK OE GND
Q1 Q2 Q3 Q4 Q5 Q6 Q7 Q8
19 18 17 16 15 14 13 12
11 1 10

43B4 6C6 574_CLK
21B6 SLEEP

+3V_MAIN

C269 0.1UF N20P80% 16V CERM 603
C298 0.001UF 20% 50V CERM 603
C313 0.01UF 20% 50V CERM 603

U17 OMIT SDRAM-2MX16X4 100MHZ TSOP CRITICAL

42B1 8C5 7D5 7D2 7C4 7B2 6B7	A0	23	TERM_M_ADDR<0>		
	A1	24	TERM_M_ADDR<1>		
	A2	25	TERM_M_ADDR<2>		
	A3	26	TERM_M_ADDR<3>		
	A4	29	TERM_M_ADDR<4>		
	A5	30	TERM_M_ADDR<5>		
	A6	31	TERM_M_ADDR<6>		
	A7	32	TERM_M_ADDR<7>		
	A8	33	TERM_M_ADDR<8>		
	A9	34	TERM_M_ADDR<9>		
	A10	22	TERM_M_ADDR<10>		
	A11	35	TERM_M_ADDR<11>		
42B1 8C4 7D5 7C4 7C2 7B2 6A7	A12	36	TERM_M_ADDR<12>		
43D5 8B4 7C4 7C2 7B2 6A6	BA0	21	T_M_BA0		
43D5 8B4 7C4 7C2 7A2 6A6	BA1	20	T_M_BA1		
43C1 7C4 7C2 7A2 6A5	CS	19	T1CS0*		
43D5 8C5 7C4 7C2 7A2 6A6	RAS	18	T_SDRAS*		
43D5 8C4 7C4 7C2 7A2 6A6	CAS	17	T_SDCAS*		
43D5 8C5 7C4 7C2 7A2 6A6	WE	16	T_MEMWE*		
43D1 8C4 6C2	LDQM	15	DQM4*		
43D1 8C4 6C2	UDQM	39	DQM5*		
42D1 7C4 7C2 7A2 6D6	CLK	38	MCLK<0>		
7C5 7C4 7C2 7A2	CKE	37	T_RAM_CKE0_MLB		
	VSS	28			
	VSSQ	41			
		54			
		6			
		12			
		46			
		52			
42B5 8D4 7D5 6C3 6D4	DQ0	2	MDATA<32>	32	
	DQ1	4	MDATA<33>	33	
	DQ2	5	MDATA<34>	34	
	DQ3	7	MDATA<35>	35	
	DQ4	8	MDATA<36>	36	
	DQ5	10	MDATA<37>	37	
	DQ6	11	MDATA<38>	38	
	DQ7	13	MDATA<39>	39	
	DQ8	42	MDATA<40>	40	
	DQ9	44	MDATA<41>	41	
	DQ10	45	MDATA<42>	42	
	DQ11	47	MDATA<43>	43	
	DQ12	48	MDATA<44>	44	
	DQ13	50	MDATA<45>	45	
	DQ14	51	MDATA<46>	46	
6B3 6D4 7D5 8C4 42B5	DQ15	53	MDATA<47>	47	

+3V_MAIN

C315 0.01UF 20% 50V CERM 603
C314 0.01UF 20% 50V CERM 603
C312 0.1UF N20P80% 16V CERM 603

U19 OMIT SDRAM-2MX16X4 100MHZ TSOP CRITICAL

8D7 6D4 6B5 7D2 7D4	A0	23	TERM_M_ADDR<0>		
42B1 8C5 7D5 7D4 7B4	A1	24	TERM_M_ADDR<1>		
	A2	25	TERM_M_ADDR<2>		
	A3	26	TERM_M_ADDR<3>		
	A4	29	TERM_M_ADDR<4>		
	A5	30	TERM_M_ADDR<5>		
	A6	31	TERM_M_ADDR<6>		
	A7	32	TERM_M_ADDR<7>		
	A8	33	TERM_M_ADDR<8>		
	A9	34	TERM_M_ADDR<9>		
	A10	22	TERM_M_ADDR<10>		
	A11	35	TERM_M_ADDR<11>		
7C2 7A4 6A6	A12	36	TERM_M_ADDR<12>		
43D5	BA0	21	T_M_BA0		
	BA1	20	T_M_BA1		
7C2 7A4 6A5 43C1 7C4	CS	19	T1CS0*		
7C2 7A4 6A6 43D5 8C4 7C4	RAS	18	T_SDRAS*		
43D1 8B4 6C2	CAS	17	T_SDCAS*		
43D1 8B4 6C2	WE	16	T_MEMWE*		
	LDQM	15	DQM6*		
	UDQM	39	DQM7*		
7C4 7C2 7A4 7C5	CLK	38	MCLK<0>		
	CKE	37	T_RAM_CKE0_MLB		
	VSS	28			
	VSSQ	41			
		54			
		6			
		12			
		46			
		52			
42A5 8B4 7D5 6B3 6D4 7D5 8A4 42A5	DQ0	2	MDATA<48>	48	
	DQ1	4	MDATA<49>	49	
	DQ2	5	MDATA<50>	50	
	DQ3	7	MDATA<51>	51	
	DQ4	8	MDATA<52>	52	
	DQ5	10	MDATA<53>	53	
	DQ6	11	MDATA<54>	54	
	DQ7	13	MDATA<55>	55	
	DQ8	42	MDATA<56>	56	
	DQ9	44	MDATA<57>	57	
	DQ10	45	MDATA<58>	58	
	DQ11	47	MDATA<59>	59	
	DQ12	48	MDATA<60>	60	
	DQ13	50	MDATA<61>	61	
	DQ14	51	MDATA<62>	62	
6B3	DQ15	53	MDATA<63>	63	

SDRAM ON-BOARD BANKS.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
33S50007(ATC)	4	16MX16-1H PC100/CL2 TSOPII54	U16,U17,U19,U20	128M
33S50210(ATC)	4	32MX16-1H PC100/CL2 TSOPII54	U16,U17,U19,U20	256M

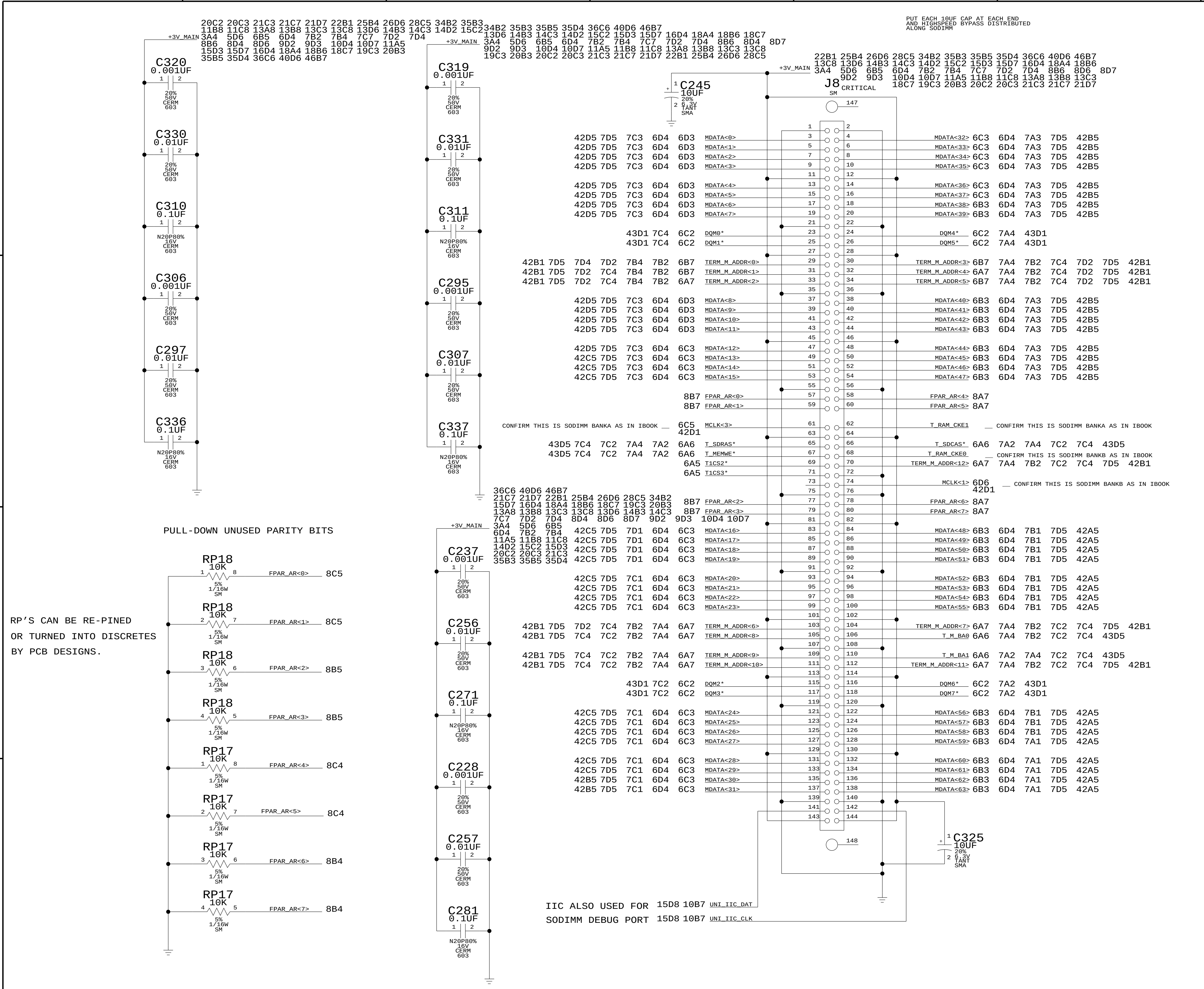
BANK 0

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 7 OF 53	

CR-8



SO-DIMM CONNECTOR

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

NOTICE OF PROPRIETARY PROPERTY

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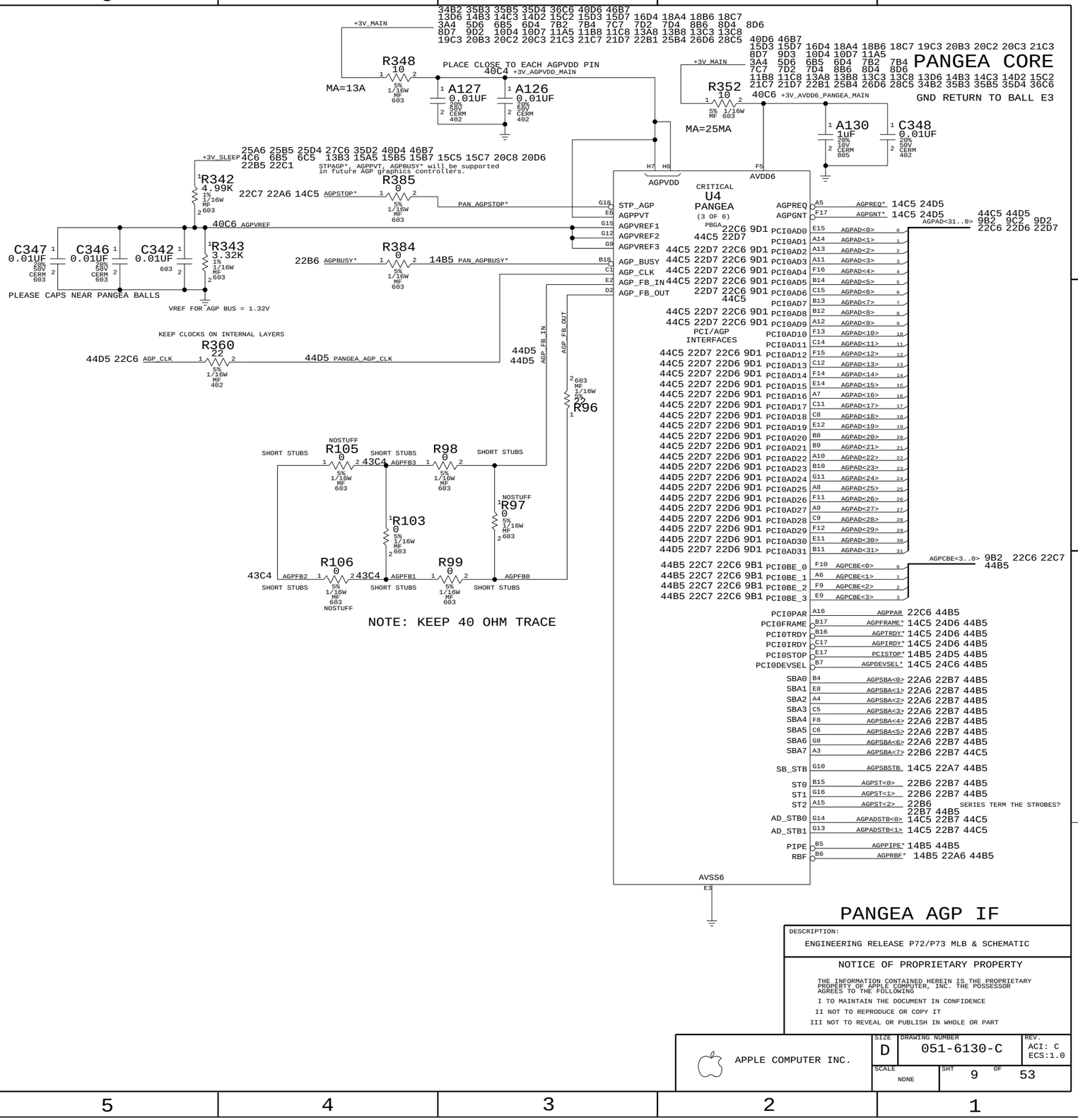
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE NONE	SHT 8	OF 53

PANGEA CORE

PANGEA AGP IF



1. WHAT IS THE PURPOSE OF SINGNAL AGPPVT?
2. CHECK WITH BILL C. FOR AGPVREF DIVIDERS - SCALE FOR LESS LEAKAGE.

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 9 OF 53	

PANGEA CORE

+3V_MAIN 34B2 35B3 35B5 35D4 36C6 40D6 46B7 13D6 14B3 14C3 14D2 15C2 15D3 15D7 16D4 18A4 18B6 18C7 3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D6 8D7 9D2 9D3 10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8 19C3 20B3 20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5

+VIO_CPUBUS_MAIN 36B5 35C4 11D8

+2_5V_MAIN 3B4 11D8 18D7 23A8 23B7 23D1 23D6 23D8 36B7 37C1 40C4

VDD

VDD 1.8V

VDD 2.5V

CRITICAL

U4
PANGEA
(4 OF 6)
PBGA

35D4 35B5 35B3 34B2 28C5 26D6 25B4 19C3 18C7 18B6 18A4 16D4 15D7 15D3 13B8 13A8 11C8 11B8 11A5 10D4 9D3 7C7 7B4 7B2 6D4 6B5 5D6 3A4 9D2 8D7 8D6 8D4 8B6 7D4 7D2 15C2 14D2 14C3 14B3 13D6 13C8 13C3 22B1 21D7 21C7 21C3 20C3 20C2 20B3 46B7 40D6 36C6 40C6 11A8

L25
100-OHM-EMI
SM

+3V_MAIN

+3V_AMVDD_PANGEA_MAIN

AMVDD

ETH_RXD_PD 10B7 40C6

GBE_REFCLK 10B7 40C6

R344 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

18D6 MII_TX_EN

18D6 MII_TX_ER

KEEP CLOCK ON INTERNAL LAYER

18D7 45B4 MII_TX_CLK

18D8 MII_TXD<0>

18C8 MII_TXD<1>

18C8 MII_TXD<2>

18C8 MII_TXD<3>

TX_CLK
TX_EN
TX_ER
TXD_0
TXD_1
TXD_2
TXD_3
TXD_4
TXD_5
TXD_6
TXD_7

KEEP CLOCK ON INTERNAL LAYER

45B4 18C7 MII_RX_CLK

18C6 MII_RX_DV

18C6 MII_RX_ER

18C6 MII_RXD<0>

18C6 MII_RXD<1>

18C6 MII_RXD<2>

18C6 MII_RXD<3>

RX_CLK
RX_DV
RX_ER
RXD_0
RXD_1
RXD_2
RXD_3
RXD_4
RXD_5
RXD_6
RXD_7

40C6 10D2 ETH_RXD_PD

40C6 10D2 GBE_REFCLK

NC

GBE_REFCLK
GTX_CLK

18C6 MII_CRS

18C6 MII_COL

CRS
COL

MDIO
MDC

GB ETHERNET

MISC

R386 47 5% 1/16W MF 603

UNI_RESET* 20B3 21B1 21C3

R303 47 5% 1/16W MF 603

UNI_PU_RESET* 21B1 21C3

RESET E29 URESET*

PURESET AK32 UPURESET*

PHY_DATA0 B20 FW_LINK_D<0> 19A8 44C1
PHY_DATA1 G19 FW_LINK_D<1> 19A8 44C1
PHY_DATA2 F19 FW_LINK_D<2> 19A8 44C1
PHY_DATA3 C20 FW_LINK_D<3> 19A7 44C1
PHY_DATA4 A21 FW_LINK_D<4> 19A7 44C1
PHY_DATA5 E20 FW_LINK_D<5> 19A7 44D1
PHY_DATA6 B21 FW_LINK_D<6> 19A7 44D1
PHY_DATA7 F20 FW_LINK_D<7> 19A7 44D1

PHY_LPS A19 FW_LINK_LPS 19B8
PHY_CTL0 F18 FW_LINK_CNTL0 19A8 44C1
PHY_CTL1 A20 FW_LINK_CNTL1 19A8 44C1
PHY_LREQ B19 FW_LINK_LREQ 19B8 44C1

FIREWIRE

KEEP CLOCK ON INTERNAL LAYER

PHY_SCLK C18 FW_LINK_SCLK 19A8 44D1

FW_GPIO_0 E18 FW_C_LKON 13C8 19B6

FW_GPIO_1 A22 FW_LINK_GPIO1

TP2 THT A

VIEW PLL 5/6

NO FIREWIRE

R358 10K 5% 1/16W MF 402

STUFF ONLY IF FW PHY NOT STUFFED

VSS_SPARE

R125 22 5% 1/16W MF 603

R126 22 5% 1/16W MF 603

18C6 MII_MDIO

18C6 MII_MDC

15D3 15C3 ASIC_TDI

15D3 PANGEA_TDO

15C3 ASIC_TCK

15D3 15C3 ASIC_TMS

15C3 15B3 ASIC_TRST*

40C6 PANGEA_TEI

TDI
TDO
TCK
TMS
TRSTN
TEI

TEST

15D8 8A5 UNI_IIC_CLK

8A5 UNI_IIC_DAT

15D8 UNI_IIC_CLK1

15C8 35B3 UNI_IIC_DAT1

35B3 15C8 R317 10K 5% 1/16W MF 402

IICCLK0
IICDATA0
IICCLK1
IICDATA1

VSS

TEI ASSERTED IF > 2V

Pangea Ethernet, Firewire, Pwr/GNDs

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 10 OF 53	

PANGEA CORE

Pangea Core Bypass -- 16 0.01uF across each pair, 8 0.001uF on corners

+2_5V_MAIN

A85 0.1UF 20% 10V CERM 402 — A105 0.1UF 20% 10V CERM 402 — A68 0.1UF 20% 10V CERM 402 — A97 0.1UF 20% 10V CERM 402 — A112 0.1UF 20% 10V CERM 402 — A79 0.1UF 20% 10V CERM 402 — A104 0.1UF 20% 10V CERM 402 — A67 0.1UF 20% 10V CERM 402 — A84 0.1UF 20% 10V CERM 402 — A96 0.1UF 20% 10V CERM 402 — A113 0.1UF 20% 10V CERM 402 — A80 0.01UF 20% 50V CERM 402 — A70 0.01UF 20% 50V CERM 402 — A82 0.01UF 20% 50V CERM 402 — A100 0.01UF 20% 50V CERM 402 — A110 0.01UF 20% 50V CERM 402 — A78 0.01UF 20% 50V CERM 402 — A103 0.01UF 20% 50V CERM 402 — A69 0.01UF 20% 50V CERM 402 — A81 0.01UF 20% 50V CERM 402 — A99 0.01UF 20% 50V CERM 402 — A111 0.01UF 20% 50V CERM 402 — A77 0.1UF 20% 10V CERM 402 — A102 0.01UF 20% 50V CERM 402

C345 4.7UF N20P80% 16V CERM 805 — C327 4.7UF N20P80% 16V CERM 805 — C341 10UF N20P80% 16V CERM 1210 (CRITICAL)

A76 2.2UF N20P80% 16V CERM 805 — A101 2.2UF N20P80% 16V CERM 805 (CRITICAL)

PLACE AS NEAR AS CORE CENTER AS POSSIBLE

C333 0.1UF 20% 10V CERM 402 — C343 0.01UF 20% 50V CERM 402 — C332 0.1UF 20% 10V CERM 402 — C329 0.01UF 20% 50V CERM 402

Pangea Processor I/F Bypass -- two per power/ground pair

+VIO_CPUBUS_MAIN

A4 0.1UF 20% 10V CERM 402 — A22 0.1UF 20% 10V CERM 402 — A31 0.1UF 20% 10V CERM 402 — A30 0.1UF 20% 10V CERM 402 — A29 0.1UF 20% 10V CERM 402 — A28 0.1UF 20% 10V CERM 402 — A27 0.1UF 20% 10V CERM 402 — A26 0.1UF 20% 10V CERM 402 — A25 0.1UF 20% 10V CERM 402 — A24 0.1UF 20% 10V CERM 402 — A3 0.1UF 20% 10V CERM 402 — A7 0.01UF 20% 50V CERM 402 — A32 0.01UF 20% 50V CERM 402 — A41 0.01UF 20% 50V CERM 402 — A40 0.01UF 20% 50V CERM 402 — A39 0.01UF 20% 50V CERM 402 — A38 0.01UF 20% 50V CERM 402 — A37 0.01UF 20% 50V CERM 402 — A36 0.01UF 20% 50V CERM 402 — A35 0.01UF 20% 50V CERM 402 — A34 0.01UF 20% 50V CERM 402 — A6 0.01UF 20% 50V CERM 402

Pangea I/O Ring Bypass -- two per power/ground pair

+3V_MAIN

A98 0.1UF 20% 10V CERM 402 — A121 0.1UF 20% 10V CERM 402 — A17 0.1UF 20% 10V CERM 402 — A87 0.1UF 20% 10V CERM 402 — A157 0.1UF 20% 10V CERM 402 — A165 0.1UF 20% 10V CERM 402 — A164 0.1UF 20% 10V CERM 402 — A166 0.1UF 20% 10V CERM 402 — A158 0.1UF 20% 10V CERM 402 — A89 0.1UF 20% 10V CERM 402 — A132 0.1UF 20% 10V CERM 402 — A54 0.1UF 20% 10V CERM 402 — A64 0.1UF 20% 10V CERM 402 — A75 0.1UF 20% 10V CERM 402 — A94 0.1UF 20% 10V CERM 402 — A109 0.1UF 20% 10V CERM 402 — A117 0.1UF 20% 10V CERM 402 — A125 0.1UF 20% 10V CERM 402 — A45 0.1UF 20% 10V CERM 402

+3V_MAIN

A149 0.1UF 20% 10V CERM 402 — A148 0.1UF 20% 10V CERM 402 — A147 0.1UF 20% 10V CERM 402 — A146 0.1UF 20% 10V CERM 402 — A145 0.1UF 20% 10V CERM 402 — A144 0.1UF 20% 10V CERM 402 — A143 0.1UF 20% 10V CERM 402 — A142 0.1UF 20% 10V CERM 402 — A151 0.1UF 20% 10V CERM 402 — A128 0.1UF 20% 10V CERM 402 — A61 0.1UF 20% 10V CERM 402 — A72 0.1UF 20% 10V CERM 402 — A91 0.1UF 20% 10V CERM 402 — A106 0.1UF 20% 10V CERM 402 — A114 0.1UF 20% 10V CERM 402 — A122 0.1UF 20% 10V CERM 402 — A95 0.1UF 20% 10V CERM 402 — A152 0.1UF 20% 10V CERM 402 — A159 0.01UF 20% 50V CERM 402

+3V_MAIN

A86 0.01UF 20% 50V CERM 402 — A156 0.01UF 20% 50V CERM 402 — A162 0.01UF 20% 50V CERM 402 — A150 0.01UF 20% 50V CERM 402 — A154 0.01UF 20% 50V CERM 402 — A21 0.01UF 20% 50V CERM 402 — A131 0.01UF 20% 50V CERM 402 — A53 0.01UF 20% 50V CERM 402 — A63 0.01UF 20% 50V CERM 402 — A74 0.01UF 20% 50V CERM 402 — A93 0.01UF 20% 50V CERM 402 — A108 0.01UF 20% 50V CERM 402 — A116 0.01UF 20% 50V CERM 402 — A124 0.01UF 20% 50V CERM 402 — A140 0.01UF 20% 50V CERM 402 — A139 0.01UF 20% 50V CERM 402 — A138 0.01UF 20% 50V CERM 402 — A137 0.01UF 20% 50V CERM 402 — A136 0.01UF 20% 50V CERM 402

+3V_MAIN

A135 0.01UF 20% 50V CERM 402 — A134 0.01UF 20% 50V CERM 402 — A133 0.01UF 20% 50V CERM 402 — A141 0.01UF 20% 50V CERM 402 — A129 0.01UF 20% 50V CERM 402 — A62 0.01UF 20% 50V CERM 402 — A73 0.01UF 20% 50V CERM 402 — A92 0.01UF 20% 50V CERM 402 — A107 0.01UF 20% 50V CERM 402 — A115 0.01UF 20% 50V CERM 402 — A123 0.01UF 20% 50V CERM 402 — A120 0.01UF 20% 50V CERM 402 — A83 0.01UF 20% 50V CERM 402 — A90 0.01UF 20% 50V CERM 402 — A44 0.01UF 20% 50V CERM 402 — A161 0.01UF 20% 50V CERM 402 — A16 0.01UF 20% 50V CERM 402 — A153 0.01UF 20% 50V CERM 402 — A163 0.01UF 20% 50V CERM 402 — A88 0.01UF 20% 50V CERM 402

A20 0.01UF 20% 50V CERM 402 — A5 0.1UF 20% 10V CERM 402 — A57 0.1UF 20% 10V CERM 402 — A9 0.01UF 20% 50V CERM 402

A56 0.01UF 20% 50V CERM 402 — A49 0.01UF 20% 50V CERM 402 — A23 0.01UF 20% 50V CERM 402 — A18 0.1UF 20% 10V CERM 402

A13 2.2UF N20P80% 16V CERM 805 — A10 2.2UF N20P80% 16V CERM 805 — A12 2.2UF N20P80% 16V CERM 805 — A11 2.2UF N20P80% 16V CERM 805

PLACE AT EDGES OF PROC I/F PLANE

Pangea AMVDD Bypass (one pair per pin)

40C6 10C7 +3V_AMVDD_PANGEA_MAIN

A50 0.1UF 20% 10V CERM 402 — A60 0.1UF 20% 10V CERM 402 — A51 0.1UF 20% 10V CERM 402 — A42 0.1UF 20% 10V CERM 402 — A46 0.01UF 20% 50V CERM 402 — A19 0.01UF 20% 50V CERM 402

A58 0.01UF 20% 50V CERM 402 — A65 0.01UF 20% 50V CERM 402 — A52 0.01UF 20% 50V CERM 402 — A43 0.01UF 20% 50V CERM 402 — A200 2.2UF N20P80% 16V CERM 805 — A14 0.1UF 20% 10V CERM 402

36C6 35D4 35B5 35B3 34B2 28C5 26D6
19C3 18C7 18B6 18A4 16D4 15D7 15D3
13B8 13A8 11C8 11B8 10D7 10D4 9D3
7C7 7B4 7B2 6D4 6B5 5D6 3A4
9D2 8D7 8D6 8D4 8B6 7D4 7D2
15C2 14D2 14C3 14B3 13D6 13C8 13C3
25B4 22B1 21D7 21C7 21C3 20C3 20C2 20B3
46B7 40D6

+3V_MAIN

A66 2.2UF N20P80% 16V CERM 805 — A118 2.2UF N20P80% 16V CERM 805 — A160 2.2UF N20P80% 16V CERM 805 — A155 2.2UF N20P80% 16V CERM 805 — A119 2.2UF N20P80% 16V CERM 805 — A71 2.2UF N20P80% 16V CERM 805 (CRITICAL)

PLACE ALONG OUTSIDE OF BALL GRID ALONG 3 NON-MAXBUS MAXBUS SIDES (2 PER)

Pangea Bypass

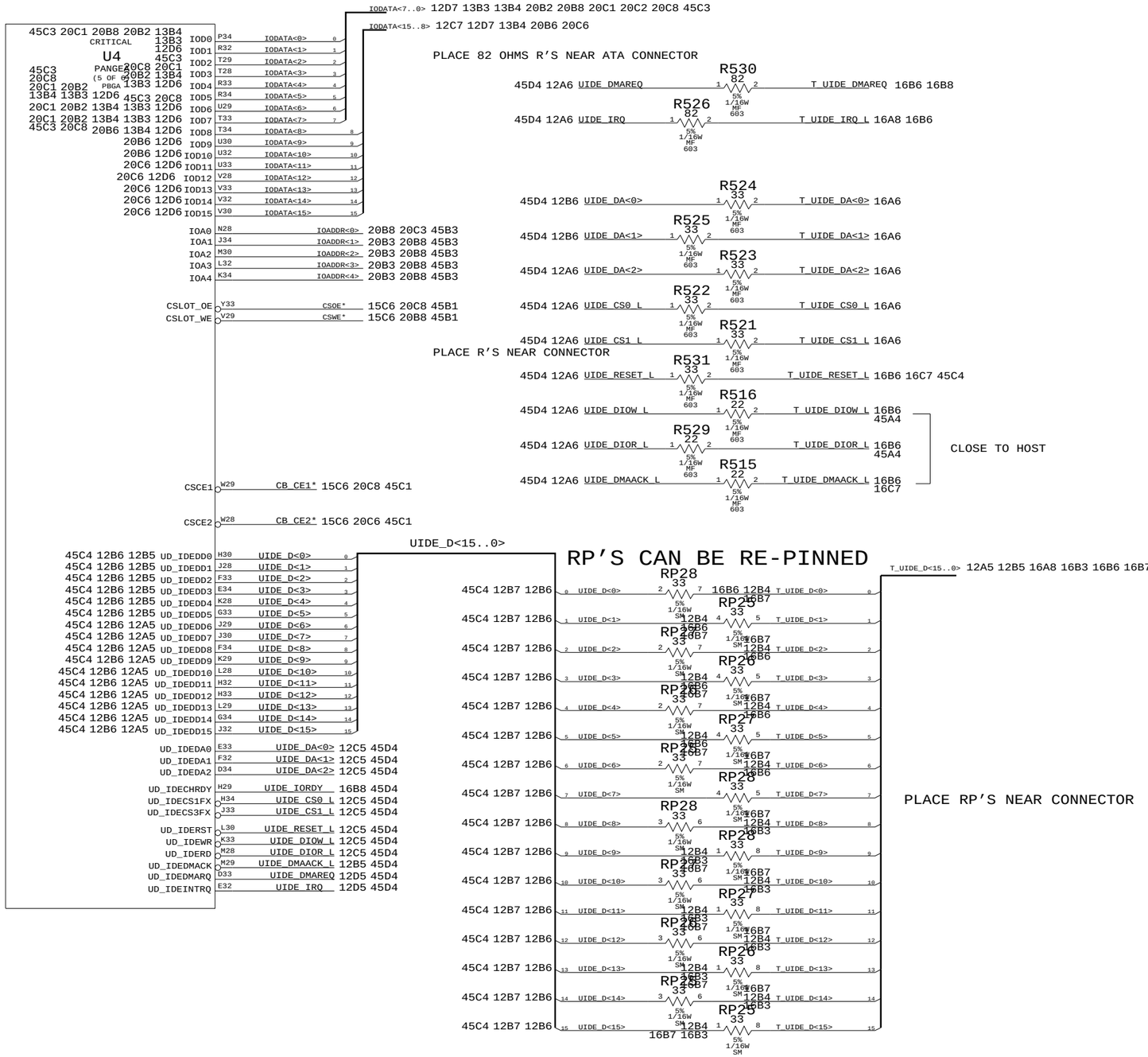
DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 11 OF 53	

CR-12

PANGEA CORE



PANGEA ATA BUS

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 12 OF 53	

CR-13

PANGEA CORE

USBVD1	USBVD2	USBVD3	USBVD4
USB PORT1	IRDA/BT	USB PORT2	INTERAL MODEM

OPTION ADD PARALLEL R TO RESOLVE RESONANT NOISE CONCERN

CRITICAL

CRYSTAL bias circuitry needs to be looked at to determine proper values

Pangea BootStrap Pins

1 = 66M 0 = 100M
1 = SS ON 0 = SS OFF
1 = Desktop 0 = Portable
1 = PCI1 Debug 0 = No PCI1
1 = PCI2 Debug 0 = No PCI2
11 = 33M AGP 10 = 50M AGP 01 = 40M AGP 00 = 66M AGP
1 = 33M 0 = 66M

DEFAULT FOR P72: 00100000
DEFAULT FOR P73: 00100000

PANGEA SER/AUD/USB, BOOTSTRAPS

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 13 OF 53	

CR-14

PANGEA PULLUPS/PULLDOWNS

TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLE ON PAGE 49

MAXBUS PULLS

46B7 36B4 35C3
13D1 5C2 4D5 4B4 3D5 3C4 +VIO_CPU_SLEEP
15D2 15B1 14D6 14C6 14A7 14A6

R553 4.7K 5% 1/16W MF 603

NOSTUFF R38 1K 5% 1/16W MF 603

5B7 3A6 41D1 QREQ*

RP101 4.7K 5% 1/16W SM

RESISTOR 3,6 NOT IN USE

RP4 4.7K 5% 1/16W SM
5B7 3C8 41D1 TBST*

RP14 4.7K 5% 1/16W SM
5D7 3D8 41D1 CPU_BR*

RP14 4.7K 5% 1/16W SM
5B7 3C8 41A1 GBL*

R251 4.7K 5% 1/16W MF 603
5D7 3D8 41D1 TS*

RP4 4.7K 5% 1/16W SM
5A4 3A6 41D1 TA*

RP16 4.7K 5% 1/16W SM
5A4 3A6 41D1 TEA*

R266 10K 5% 1/16W MF 603
3A6 MCP*

RP16 4.7K 5% 1/16W SM
3D6 ABB*

RP101 4.7K 5% 1/16W SM
3D7 DBB*

RP100 4.7K 5% 1/16W SM
3A6 TLBISYNC*

RP101 4.7K 5% 1/16W SM
3A6 SMI*

RP101 4.7K 5% 1/16W SM
6B6 3A6 43B4 TBEN

R39 2K 5% 1/16W MF 603
15D2 3A6 SRESET*

R34 1K 5% 1/16W MF 603
15D2 3A6 CHKSTP_OUT*

R294 10K 5% 1/16W MF 603
5B7 HIT*

R74 10K 5% 1/16W MF 603
5A4 DRDY*

RP16 4.7K 5% 1/16W SM
5A4 3B8 41A1 CPU_DBG*

MIRAGE R268 2.2K 5% 1/16W MF 603
21C3 15B3 CPU_HRST

RP100 4.7K 5% 1/16W SM
3A6 CHKSTP_IN*

R1032 1K 5% 1/16W MF 603
5B7 3B8 41D1 ARTRY*

46B7 36B4 35C3
13D1 5C2 4D5 4B4 3D5 3C4 +VIO_CPU_SLEEP
15D2 15B1 14D8 14C6 14A7 14A6

41D1 5A4 3B8 DBWO* — R262 4.7K 5% 1/16W MF 603

41A1 5D7 3D8 CPU_BG* — R597 4.7K 5% 1/16W MF 603

3D6 LSSD_MODE* — RP100 4.7K 5% 1/16W SM

3D6 L1_TSTCLK — RP100 4.7K 5% 1/16W SM

3D6 L2_TSTCLK — R856 4.7K 5% 1/16W MF 603

R866 4.7K 5% 1/16W MF 603 NOSTUFF

14D8 14D6 14A7 14A6 13D1 5C2 4D5 4B4 3D5 3C4 +VIO_CPU_SLEEP
46B7 36B4 35C3 15D2 15B1

41D1 5B7 3B8 AACK* — RP4 4.7K 5% 1/16W SM

41A1 5B7 3B8 WT* — RP15 4.7K 5% 1/16W SM

41A1 5B7 3B8 CI* — RP15 4.7K 5% 1/16W SM

41D1 5B7 3A4 PAN_QACK* — R260 4.7K 5% 1/16W MF 603

C279 0.001UF 20% 50V CERM 603

(R260) WHY NEED A PULLU[? PANGEA ALWAYS DRIVES EXEPT IN SLEEP.

15D2 15B1 14D8 14D6 46B7 36B4 35C3 15D2 15B1 14D8 14D6
4D5 4B4 3D5 3C4 +VIO_CPU_SLEEP 4D5 4B4 3D5 3C4 +VIO_CPU_SLEEP
14C6 14A6 13D1 5C2 14C6 14A7 13D1 5C2
46B7 36B4 35C3

R862 4.7K 5% 1/16W MF 603
3C6 DBDIS*

NOSTUFF R863 0 5% 1/16W MF 603
3B8 DRTRY*

R864 47 5% 1/16W MF 603
15D2 15B2 3A6 3A4 CPU_HRESET*

SAHARA V2.0		
BVSEL	L1_TSTCLK	I/O VOLTAGE
B'0'	B'0'	N/A
B'0'	B'1'	1.2, 1.5, OR 1.8
B'1'	B'0'	3.3
B'1'	B'1'	2.5

NOTE:
FOR SAHARA V1.1, L1_TSTCLK
MUST BE TIED TO A LOGICAL '1'

AGP PULLS

36C4 25D2 25C2 24C2 23C8 23C1 23B8 22D8 22C5 22A4 14D3 +3V_VGA_MAIN
46C7 46B7

44B5 22A7 9B1 AGPSBSTB — R372 10K 5% 1/16W MF 402

24D5 9D1 AGPGNT* — R371 10K 5% 1/16W MF 603

24D5 9D1 AGPREQ* — R113 10K 5% 1/16W MF 603

24D6 9B1 44B5 AGPFRAME* — R119 10K 5% 1/16W MF 603

44B5 24D6 9B1 AGPTRDY* — R118 10K 5% 1/16W MF 603

44B5 24D6 9B1 AGPIRDY* — R117 10K 5% 1/16W MF 603

22C7 22A6 9D4 AGPSTOP* — R133 10K 5% 1/16W MF 603

44B5 24C6 9B1 AGPDEVSEL* — R111 10K 5% 1/16W MF 603

44C5 22B7 9A1 AGPADSTB<0> — R366 10K 5% 1/16W MF 402

44C5 22B7 9A1 AGPADSTB<1> — R373 10K 5% 1/16W MF 402

44B5 22A6 9A1 AGPRBF* — R453 10K 5% 1/16W MF 603

44B5 9A1 AGPPIPE* — R112 10K 5% 1/16W MF 402

44B5 24D5 9B1 PCISTOP* — R370 10K 5% 1/16W MF 603

9C3 PAN_AGPBUSY* — R104 10K 5% 1/16W MF 402

GPIO PULLS

EMMO* PULLUP HAS BEEN DELETED DUE TO FW NEW INTRPT PINOUT

36C4 25D2 25C2 24C2 23C8 23C1 23B8 22D8 22C5 22A4 14D4 +3V_VGA_MAIN
46C7 46B7

22B6 13C7 AGP_INTA* — R954 10K 5% 1/16W MF 603

38B4 13D7 VCORE_CTL — R1030 10K 5% 1/16W MF 603 — +3V_MAIN

34B2 35B3 35B5 35D4 36C6 40D6 46B7
13C8 13D6 14B3 14C3 15C2 15D3 15D7 16D4 18A4 18B6 18C7
3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D6
8D7 9D2 9D3 10D4 10D7 11A5 11B8 11C8 13A8 13B8 13C3
19C3 20B3 20C2 20C3 21C3 21C7 21D7 22B1 25B4 26D6 28C5

PMU PULLS

46B7 40D6 36C6 35D4
21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6
13C8 13C3 13B8 13A8 11C8 11B8 11A5 10D7
7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4
10D4 9D3 9D2 8D7 8D6 8D4 8B6 7D4
18A4 16D4 15D7 15D3 15C2 14D2 14B3 13D6
35B5 35B3 34B2 28C5 26D6 25B4 22B1 21D7 +3V_MAIN

21C3 13C5 PMU_REQ* — R22 10K 5% 1/16W MF 603

21C3 13C7 PMU_NMI_IRQ* — R389 10K 5% 1/16W MF 603

21B5 13C7 PMU_INT — RP19 10K 5% 1/16W SM

MODEM PULLS

46B7 40D6 36C6 35D4
21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6
13C8 13C3 13B8 13A8 11C8 11B8 11A5 10D7
7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4
10D4 9D3 9D2 8D7 8D6 8D4 8B6 7D4
18A4 16D4 15D7 15D3 15C2 14D2 14C3 13D6
35B5 35B3 34B2 28C5 26D6 25B4 22B1 21D7 +3V_MAIN

16D3 13D7 MODEM_SDOWN — RP19 10K 5% 1/16W MF

21C5 16C3 13C7 RING_DETECT* — RP19 10K 5% 1/16W SM

16D2 13C7 MODEM_RESET* — R955 10K 5% 1/16W MF 603

ENET PULLS

18C4 13C7 ENET_ENRGYDET_IRQ_H — R12 100K 5% 1/16W MF 603

16C3 13C5 SCC_GPIOA* — RP5 100K 5% 1/16W SM

16C2 13C5 SCC_TRXCA — RP5 100K 5% 1/16W SM

NEW 4.7K RESISTORS CAN BE
CHANGED INTO R-PACKS

R-PACKS CAN BE RE-PINNED

PULL-UP/PULL-DOWN(1)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.B
SCALE: NONE	SHT 14 OF 53	

TO LOCATE UNUSED RPAK PINS REFERE TO COMPONENT LOCATIO CREF TABLLE ON PAGE49

IIC BUS PULLUPS

40D6 36C6 35D4 MAIN RAIL, TO PREVENT LEAKAGE INTO UNPOWERED DEVICES
21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6
13C8 13C3 13B8 13A8 11C8 11B8 11A5 10D7
7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4
10D4 9D3 9D2 8D7 8D6 8D4 8B6 7D4
18A4 16D4 15D3 15C2 14D2 14C3 14B3 13D6
35B5 35B3 34B2 28C5 26D6 25B4 22B1 21D7
46B7 10B7 8A5 UNI_IIC_CLK — R1202 1K 5% 1/16W MF 603 — +3V_MAIN
10B7 8A5 UNI_IIC_DAT — R1203 1K 5% 1/16W MF 603
35B3 10B7 UNI_IIC_CLK1 — R312 2.2K 5% 1/16W MF 603
35B3 10A7 UNI_IIC_DAT1 — R82 2.2K 5% 1/16W MF 603

PMU NOT RATED STRONG ENOUGH FOR 1K

46B7 40D4 35D2 27C6
15B7 15B5 15A5 13B3 9D4 6C5 6B5 4C6 +3V_SLEEP
25D4 25B5 25A6 22C1 22B5 20D6 20C8 15C5
21B3 6D5 PMU_IIC_CLK — R1120 10K 5% 1/16W MF 603
21B3 6C5 PMU_IIC_DAT — R1121 10K 5% 1/16W MF 603

PMU PULL UP

CARDSLOT BUS PULLS

20D6 20C8 15C7 15B7 15B5 15A5 13B3 9D4 6C5 6B5 4C6 +3V_SLEEP
46B7 40D4 35D2 27C6 25D4 25B5 25A6 22C1 22B5
45C1 20C6 13B5 CB_IORD* — RP8 10K 5% 1/16W SM
45C1 20B6 13B5 CB_IOWR* — RP8 10K 5% 1/16W SM
45C1 20C8 12B6 CB_CE1* — RP21 10K 5% 1/16W SM
45C1 20C6 12B6 CB_CE2* — RP21 10K 5% 1/16W SM
45B1 20C8 12C6 CSOE* — RP8 10K 5% 1/16W SM
45B1 20B8 12C6 CSWE* — RP21 10K 5% 1/16W SM

20D6 20C8 15C7 15C5 15B7 15A5 13B3 9D4 6C5 6B5 4C6 +3V_SLEEP
46B7 40D4 35D2 27C6 25D4 25B5 25A6 22C1 22B5
45C1 20B6 13C7 CB_REG* — R59 4.7K 5% 1/10W MF 603
45C1 20B8 13C7 CB_IREQ* — R64 4.7K 5% 1/16W MF 603
45C1 20B6 13B5 CB_WAIT* — RP8 10K 5% 1/16W SM
45C1 20B6 13C8 CB_RESET — R83 20K 5% 1/16W MF 603 — +3V_SLEEP
4C6 6B5 6C5 9D4 13B3 15B5 15B7 15C5 15C7 20C8 20D6 22B5
22C1 25A6 25B5 25D4 27C6 35D2 40D4 46B7

46B7 40D4 35D2 27C6
15C5 15B5 15A5 13B3 9D4 6C5 6B5 4C6 +3V_SLEEP
25D4 25B5 25A6 22C1 22B5 20D6 20C8 15C7
27B1 16C3 13B5 KW_IIC_CLK — R339 1K 5% 1/16W MF 603
27B1 16C2 13A5 KW_IIC_DAT — R359 1K 5% 1/16W MF 603

JTAG PULLS

JTAG TEST PORT

CONFIRM PULLUP VOLTAGE

OMIT
I21
J19
SM-1

40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1
16D4 15D7 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8
8D4 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4
13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6
21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4
46B7

+3V_MAIN	1	2	+VIO_CPU_SLEEP	3C4	3D5	4B4 4D5 5C2 13D1 14A6 14A7 14C6	
NC	3	4	CHKSTP_OUT*	3A6	14A8	14D6 14D8 15B1 35C3 36B4 46B7	
NC	5	6	CPU_HRESET*	3A4	3A6	14A6 15B2	
NC	7	8	SRESET*	3A6	14A8		
15C3 10B7 ASIC_TMS	9	10	NC				
15C3 10B7 ASIC_TDI	11	12	CPU_TMS	3D6	15B3		
10B7 PANGEA_TDO	13	14	CPU_TDI	3D6	15B3		
15C3 10B7 ASIC_TCK	15	16	CPU_TDO	3D6			
15B3 10B7 ASIC_TRST*	17	18	CPU_TCK	3D6	15B3		
	19	20	CPU_TRST*	3D6	15A3		

15D3 10B7 ASIC_TDI — R53 10K 5% 1/16W MF 603
15D3 10B7 ASIC_TMS — R52 10K 5% 1/16W MF 603 — +3V_MAIN
35D4 36C6 40D6 46B7
18B6 18C7 19C3 20B3 20C2 20C3 21C3 21C7
10D7 11A5 11B8 11C8 13A8 13B8 13C3 13C8
3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2
7D4 8B6 8D4 8D6 8D7 9D2 9D3 10D4
13D6 14B3 14C3 14D2 15D3 15D7 16D4 18A4
21D7 22B1 25B4 26D6 28C5 34B2 35B3 35B5
15C3 10B7 ASIC_TCK — R58 10K 5% 1/16W MF 603
15C3 10B7 ASIC_TRST* — R60 1K 5% 1/16W MF 603

15D2 3D6 CPU_TDI — RP14 4.7K 5% 1/16W SM — +VIO_CPU_SLEEP
35C3 36B4 46B7
3C4 3D5 4B4 4D5 5C2 13D1
14A6 14A7 14C6 14D6 14D8 15D2
15D2 3D6 CPU_TMS — RP14 4.7K 5% 1/16W SM
15C2 3D6 CPU_TCK — RP15 4.7K 5% 1/16W SM

MIRAGE
21C3 14A8 CPU_HRST — R274 0 5% 1/16W MF 603 — CPU_HRESET* 3A4 3A6 14A6 15D2

15C2 3D6 CPU_TRST* — RP15 4.7K 5% 1/16W SM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
630-3999	1	PCBA,BOOTBANGER,P72	J19	OASIS
511S0018	1	CONN,POPT,STR 20-P .8MM PITCH	J19	NONPRODUCTION

PULL-UP/PULL DOWN(2)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.B

SCALE NONE | SHT 15 OF 53

MICRO DASH AND MINI-SPRING MODEM BOARD CONNECTOR

8D4 40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1
15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8
8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4
13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6
21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4
46B7

+3V_MAIN

C194 10UF N20P80% 16V CERM 1210_1

C39 0.1UF N20P80% 16V CERM 603

J2
F-ST-5047
SM

CLOSE TO PANGEA NOSTUFF
R964 0 5% 1/16W MF 603
28C3 25B4 13C5 SCC_RXDA
14B3 13D7 MODEM_SDOWN
14B3 13C5 SCC_GPIOA*
21C5 14B3 13C7 RING_DETECT*
DAA_OUT_1/MODEM_HOOK_RELAY
27B1 15A8 13B5 KW_IIC_CLK
I2C_ADDR_S0
(COMM_ANALOG_SND_RET)

CLOSE TO PANGEA NOSTUFF
R965 0 5% 1/16W MF 603
MODEM_RESET*
14B3 13C7 SCC_RTSA*
13D5 25B4
NOSTUFF CLOSE TO PANGEA
R963 0 5% 1/16W MF 603
SCC_DTRA
SCC_TXDA* 13D5 25A4
SCC_TRXCA 13C5 14B3
R576 24 5% 1/16W MF 603 CLOSE TO U4
USB_DDM_T
USB_DDM 13C4 13C5
USB_DDP_T
CLOSE TO U4
R577 24 5% 1/16W MF 603
KW_IIC_DAT 13A5 15A8 27B1
I2C_ADDR_S1
USB_DDP 13C4 13C5
+5V_MAIN
34C2 17B7 19D4 24D2 28C4 35D8 36B3 37B4 37D4 38B3 38B8 38C5 40D6 46C7

R227 10K 5% 1/16W MF 603

C196 0.1UF N20P80% 16V CERM 603

C191 10UF N20P80% 16V CERM 1210_1

+5V_HD_SLEEP 16A5 16B8 35C5

R532 100K 5% 1/16W MF 603
T_UIDE_RESET_L 12C4 16B6 45C4

R527 100K 5% 1/16W MF 603
T_UIDE_DMAACK_L 12B4 16B6

RJ-11 SHIELD

16B6 16B3 16A8 12B5 12B4 12A5 T_UIDE_D<15..0>

35C5 16D7 16A5 +5V_HD_SLEEP

R528 1K 5% 1/16W MF 603

45D4 12A6 UIDE_IORDY
R353 82 5% 1/16W MF 603
T_UIDE_IORDY_L 16B6

NOSTUFF
C350 10PF 5% 50V CERM 603

CLOSE TO PANGEA

HDD/CD

J18
SM

45C4 12C4 12C7	T_UIDE_RESET_L	1	RESET	GND	2	
12B4 12A5 16B7 16A8	T_UIDE_D<7>	3	D7	D8	4	16B7 12B4 12A5 T_UIDE_D<8> 8
	T_UIDE_D<6>	5	D6	D9	6	16B7 12B4 12A5 T_UIDE_D<9> 9
	T_UIDE_D<5>	7	D5	D10	8	16B7 12B4 12A5 T_UIDE_D<10> 10
	T_UIDE_D<4>	9	D4	D11	10	16B7 12B4 12A5 T_UIDE_D<11> 11
	T_UIDE_D<3>	11	D3	D12	12	16B7 12B4 12A5 T_UIDE_D<12> 12
	T_UIDE_D<2>	13	D2	D13	14	16B7 12B4 12A5 T_UIDE_D<13> 13
	T_UIDE_D<1>	15	D1	D14	16	16B7 12B4 12A5 T_UIDE_D<14> 14
12B4	T_UIDE_D<0>	17	D0	D15	18	16B7 12B4 12A5 T_UIDE_D<15> 15
16B7 12B5		19	GND	KEY	20	
16B8 12D4	T_UIDE_DMAREQ	21	DMARQ	GND	22	
45A4 12C4	T_UIDE_DIOW_L	23	IOW	GND	24	
45A4 12C4	T_UIDE_DIOR_L	25	IOR	GND	26	
16B7	T_UIDE_IORDY_L	27	IORDY	CSEL	28	
16C7 12B4	T_UIDE_DMAACK_L	29	DMACK	GND	30	
16A8 12D4	T_UIDE_IRQ_L	31	INTRQ	IOCS16	32	
12C4	T_UIDE_DA<1>	33	A1	DIAG	34	
12C4	T_UIDE_DA<0>	35	A0	A2	36	
12C4	T_UIDE_CS0_L	37	CS0	CS1	38	
12C4	T_UIDE_CS1_L	39	DAS	GND	40	
12C4	T_UIDE_DA<2>	41	POWER	POWER	42	
		43	POWER	POWER	44	
		45	N.C.	POWER	46	
		47	GND	POWER	48	
35C5 16B2 16A3	+5V_CD_SLEEP	49	POWER	POWER	50	+5V_CD_SLEEP 16A6 16B2 35C5

C465 0.1UF N20P80% 16V CERM 603

C460 0.1UF N20P80% 16V CERM 603

C470 10UF 20% 10V TANT SMB

C476 10UF 20% 10V TANT SMB

35C5 16D7 16B8 +5V_HD_SLEEP

R586 10K 5% 1/16W MF 603
16B6 12D4 T_UIDE_DMAREQ

R587 10K 5% 1/16W MF 603
16B6 12D4 T_UIDE_IRQ_L

R588 10K 5% 1/16W MF 603
16B7 16B6 12B4 12A5 T_UIDE_D<7>

35C5 16A6 16A3 +5V_CD_SLEEP

C478 10UF 20% 10V TANT SMB

C471 10UF 20% 10V TANT SMB

C466 0.1UF N20P80% 16V CERM 603

NOSTUFF
C462 470PF 10% 50V CERM 603

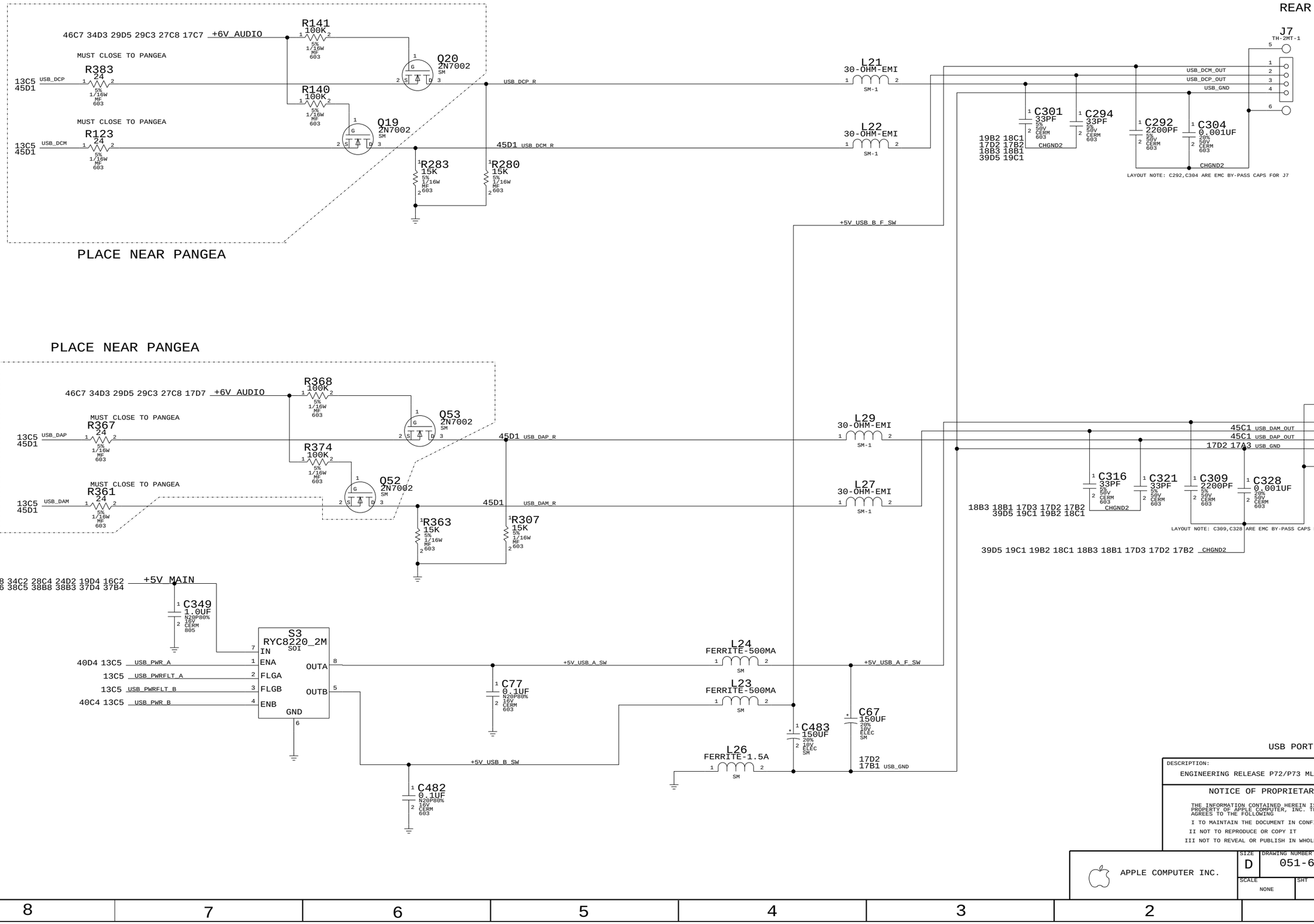
INTERNAL HD AND CD-ROM CONNECTORS

MICRO DASH AND MINI SPRING MODEM BOARD CONNECTOR

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 16 OF 53	

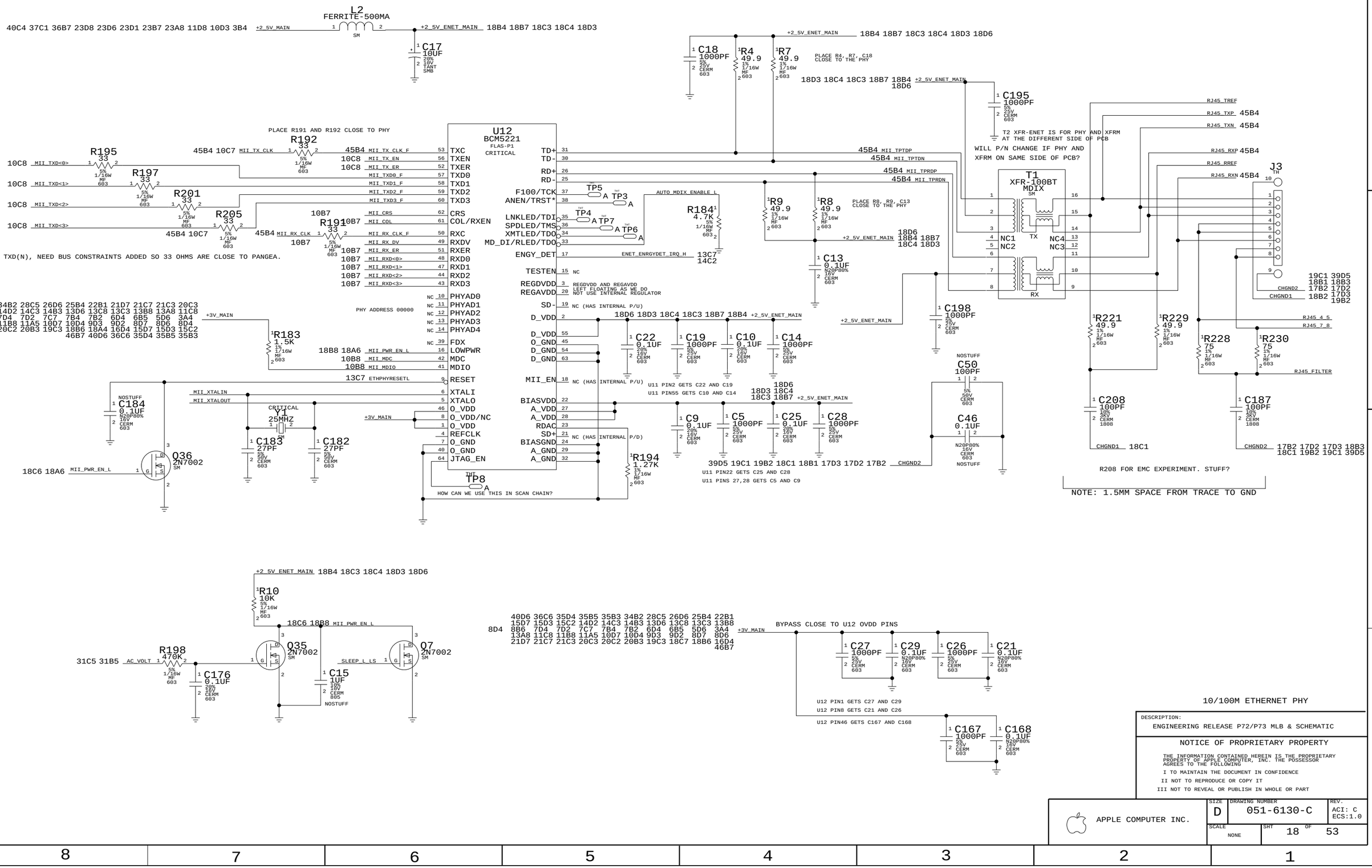


USB PORT

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 17 OF 53	

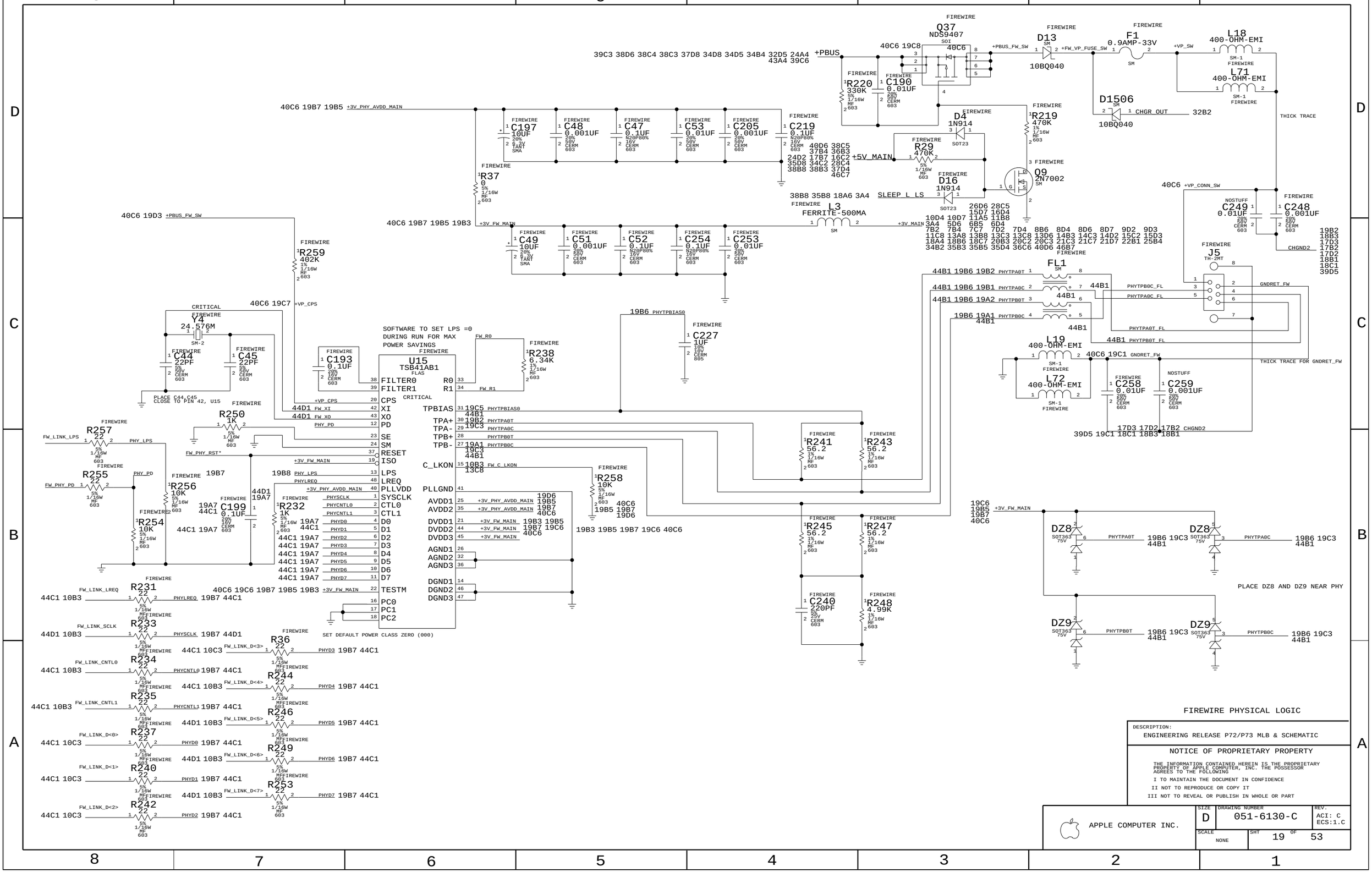


10/100M ETHERNET PHY

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 18 OF 53	


39C3 38D6 38C4 38C3 37D8 34D8 34D5 34B4 32D5 24A4 43A4 39C6 +PBUS
Q37 NDS9407 SOI
40C6 19C8
40C6
FIREWIRE
R220 330K 5% 1/16W MF 603
C190 0.01UF 20% 50V CERM 603
D13 SM 10BQ040
+PBUS_FW_SW
+FW_VP_FUSE_SW
F1 0.9AMP-33V SM
+VP_SW
L18 400-OHM-EMI SM-1
L71 400-OHM-EMI SM-1
D1506 SM 10BQ040
CHGR_OUT
32B2
THICK TRACE
40C6 19B7 19B5 +3V_PHY_AVDD_MAIN
C197 10UF 20% 6.3V TANT SMA
C48 0.001UF 20% 50V CERM 603
C47 0.1UF N20P80% 16V CERM 603
C53 0.01UF 20% 50V CERM 603
C205 0.001UF 20% 50V CERM 603
C219 0.1UF N20P80% 16V CERM 603
40D6 38C5 37B4 36B3 24D2 17B7 16C2 35D8 34C2 28C4 38B8 38B3 37D4 46C7
D4 1N914 SOT23
R219 470K 1% 1/16W MF 603
R29 470K 5% 1/16W MF 603
+5V_MAIN
Q9 2N7002 SM
SLEEP_L_LS
D16 1N914 SOT23
38B8 35B8 18A6 3A4
R37 0 5% 1/16W MF 603
40C6 19B7 19B5 19B3 +3V_FW_MAIN
C49 10UF 20% 6.3V TANT SMA
C51 0.001UF 20% 50V CERM 603
C52 0.1UF N20P80% 16V CERM 603
C254 0.1UF N20P80% 16V CERM 603
C253 0.01UF 20% 50V CERM 603
L3 FERRITE-500MA SM
26D6 28C5 15D7 16D4 10D4 10D7 11A5 11B8 3A4 5D6 6B5 6D4 7B2 7B4 7C7 7D2 7D4 8B6 8D4 8D6 8D7 9D2 9D3 11C8 13A8 13B8 13C3 13C8 13D6 14B3 14C3 14D2 15C2 15D3 18A4 18B6 18C7 20B3 20C2 20C3 21C3 21C7 21D7 22B1 25B4 34B2 35B3 35B5 35D4 36C6 40D6 46B7
+3V_MAIN
40C6 +VP_CONN_SW
NOSTUFF C249 0.01UF 20% 50V CERM 603
C248 0.001UF 20% 50V CERM 603
CHGND2
19B2 18B3 17D3 17B2 17D2 18B1 18C1 39D5
J5 TH-2MT
40C6 19D3 +PBUS_FW_SW
R259 402K 1% 1/16W MF 603
40C6 19C7 +VP_CPS
CRITICAL
Y4 24.576M SM-2
C44 22PF 5% 50V CERM 603
C45 22PF 5% 50V CERM 603
PLACE C44,C45 CLOSE TO PIN 42, U15
SOFTWARE TO SET LPS =0 DURING RUN FOR MAX POWER SAVINGS
C193 0.1UF 20% 16V CERM 603
U15 TSB41AB1 FLAS
FW_R0
FW_R1
R238 6.34K 1% 1/16W MF 603
19B6 PHYTPBIAS0
C227 1UF 10% 10V CERM 805
FILTER0 FILTER1 CPS XI XO PD SE SM RESET ISO LPS LREQ PLLVDD SYSCLK CTL0 CTL1 D0 D1 D2 D3 D4 D5 D6 D7 TESTM PC0 PC1 PC2
R0 R1 TPBIAS TPA+ TPA- TPB+ TPB- C_LKON PLLGND AVDD1 AVDD2 DVDD1 DVDD2 DVDD3 AGND1 AGND2 AGND3 DGND1 DGND2 DGND3
19C5 PHYTPBIAS0
19B2 PHYTPA0T
19C3 PHYTPA0C
PHYTPB0T
19A1 PHYTPB0C
19C3 44B1
FW_C_LKON
10B3 13C8
R258 10K 5% 1/16W MF 603
40C6 19B5 19B7 19D6
+3V_PHY_AVDD_MAIN 19B5 19B7 19D6
+3V_FW_MAIN 19B3 19B5 19B7 19C6 40C6
19B3 19B5 19B7 19C6 40C6
SET DEFAULT POWER CLASS ZERO (000)
FL1 SM
44B1 19B6 19B2 PHYTPA0T
44B1 19B6 19B1 PHYTPA0C
44B1 19B6 19A2 PHYTPB0T
19B6 19A1 PHYTPB0C
44B1
PHYTPB0C_FL
PHYTPA0C_FL
PHYTPA0T_FL
PHYTPB0T_FL
GNDRET_FW
THICK TRACE FOR GNDRET_FW
L19 400-OHM-EMI SM-1
L72 400-OHM-EMI SM-1
40C6 19C1 GNDRET_FW
C258 0.01UF 20% 50V CERM 603
C259 0.001UF 20% 50V CERM 603
17D3 17D2 17B2 CHGND2
39D5 19C1 18C1 18B3 18B1
R250 1K 5% 1/16W MF 603
R257 22 5% 1/16W MF 603
FW_LINK_LPS
PHY_LPS
R255 22 5% 1/16W MF 603
FW_PHY_PD
PHY_PD
R256 10K 5% 1/16W MF 603
R254 10K 5% 1/16W MF 603
FW_PHY_RST*
19B7
19B8 PHY_LPS
PHYLREQ
+3V_PHY_AVDD_MAIN
PHYSCLK PHYCNTL0 PHYCNTL1 PHYD0 PHYD1 PHYD2 PHYD3 PHYD4 PHYD5 PHYD6 PHYD7
C199 0.1UF 20% 16V CERM 603
R232 1K 5% 1/16W MF 603
44D1 19A7
19A7 44C1
R231 22 5% 1/16W MF 603
FW_LINK_LREQ
PHYLREQ
R233 22 5% 1/16W MF 603
FW_LINK_SCLK
R234 22 5% 1/16W MF 603
FW_LINK_CNTL0
R235 22 5% 1/16W MF 603
FW_LINK_CNTL1
R237 22 5% 1/16W MF 603
FW_LINK_D<0>
R240 22 5% 1/16W MF 603
FW_LINK_D<1>
R242 22 5% 1/16W MF 603
FW_LINK_D<2>
R36 22 5% 1/16W MF 603
FW_LINK_D<3>
R224 22 5% 1/16W MF 603
FW_LINK_D<4>
R246 22 5% 1/16W MF 603
FW_LINK_D<5>
R249 22 5% 1/16W MF 603
FW_LINK_D<6>
R253 22 5% 1/16W MF 603
FW_LINK_D<7>
44C1 10B3
44D1 10B3
44C1 10C3
44D1 10C3
R241 56.2 1% 1/16W MF 603
R243 56.2 1% 1/16W MF 603
R245 56.2 1% 1/16W MF 603
R247 56.2 1% 1/16W MF 603
C240 220PF 5% 25V CERM 603
R248 4.99K 1% 1/16W MF 603
19C6 19B5 19B7 40C6
+3V_FW_MAIN
DZ8 SOT363 75V
DZ9 SOT363 75V
PHYTPA0T
PHYTPA0C
PHYTPB0T
PHYTPB0C
19B6 19C3 44B1
PLACE DZ8 AND DZ9 NEAR PHY
FIREWIRE PHYSICAL LOGIC
DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6130-C
REV. ACI: C ECS:1.C
SCALE NONE
SHT 19 OF 53

CARDSLOT (WIRELESS) INTERFACE

20C8 15C7 15C5 15B7 15B5 15A5 13B3 9D4 6C5 6B5 4C6
46B7 40D4 35D2 27C6 25D4 25B5 25A6 22C1 22B5

+3V_SLEEP

C64 10UF 20% 6.3V TANT SMA
C61 0.01UF 20% 50V CERM 603
C60 0.1UF N20P80% 16V CERM 603
C63 0.01UF 20% 50V CERM 603
C65 0.1UF N20P80% 16V CERM 603

C64 AND C61 SHOULD BE PLACED CLOSE TO J9 PIN 24 AND 27
C60 AND C63 SHOULD BE PLACED CLOSE TO J9 PIN 74 AND 77

20B6 6A6 T_ROMCS* — R61 1K 5% 1/16W MF 603 — ROM_ONBOARD_CS* 20B3 20B6

35D2 27C6 25D4 25B5 25A6 22C1
15A5 13B3 9D4 6C5 6B5 4C6
22B5 20D6 15C7 15C5 15B7 15B5
46B7 40D4

+3V_SLEEP

RP24 10K 5% 1/16W 5M

WHY DO WE NEED TO PULLUP IOADDR13-15?

J9 SM I227

20C1 20B2 13B4 13B3 12D7 12D6	IODATA<3>	3	37	NC_CB_DETECT1*
20B2 13B4 13B3 12D7 12D6 45C3	IODATA<4>	4	38	IODATA<11> 12C7 12D6
45C3 20C1 12D6	IODATA<5>	5	39	IODATA<12> 12C7 12D6
45C3 20C1 20B2 13B4 13B3 12D7	IODATA<6>	6	40	IODATA<13> 12C7 12D6
20C1 20B2 13B4 13B3 12D7 12D6	IODATA<7>	7	41	IODATA<14> 12C7 12D6
45C3	CB_CE1*	8	42	IODATA<15> 12C7 12D6
45B3 20B3 13B5	IOADDR<10>	9	43	CB_CE2* 12B6 15C6 45C1
45B1 15C6 12C6	CSOE*	10	44	NC_VSENSE1*
45B3 20B3 13B5	IOADDR<11>	11	45	CB_IORD* 13B5 15C6 45C1
45B3 20B3 13B5	IOADDR<9>	12	46	CB_IOWR* 13B5 15C6 45C1
45B3 20B3 13B5	IOADDR<8>	13	47	IOADDR<17> 13B5 20B3 45B3
45B3 20B3 13B5	IOADDR<13>	14	48	IOADDR<18> 13B5 20B3 45A3
45B3 20B3 13B5	IOADDR<14>	15	49	IOADDR<19> 13B5 20B3 45A3
45B1 15C6 12C6	CSWE*	16	50	IOADDR<20> 13B5 20B3 45A3
45C1 15B6 13C7	CB_IREQ*	17	51	LACLK 6C6
		18	52	
		19	53	
45B3 20B3 13B5	IOADDR<16>	20	54	ROM_ONBOARD_CS* 20B3 20D7
45B3 20B3 13B5	IOADDR<15>	21	55	T_ROMWE* 6A6 20B3
45B3 20B3 13B5	IOADDR<12>	22	56	ROMOE* 6A5 6B2
45B3 20B3 13B5	IOADDR<7>	23	57	T_ROMCS* 6A6 20D7
45B3 20B3 13B5	IOADDR<6>	24	58	NC_VSENSE2*
45B3 20B3 13C5	IOADDR<5>	25	59	CB_RESET 13C8 15A6 45C1
45B3 20B3 12C6	IOADDR<4>	26	60	CB_WAIT* 13B5 15B6 45C1
45B3 20B3 12C6	IOADDR<3>	27	61	NC_INP_ACK
45B3 20B3 12C6	IOADDR<2>	28	62	CB_REG* 13C7 15B6 45C1
45B3 20B3 12C6	IOADDR<1>	29	63	IO_RESET_L 21B1 21B5 22B8
45C3 45B3 20C3 12C6	IOADDR<0>	30	64	NC_STAT_CHG
20C2 20C1 13B4 13B3 12D7 12D6	IODATA<0>	31	65	IODATA<8> 12D6 12D7 13B4
20C1 20B2 13B4 13B3 12D7 12D6	IODATA<1>	32	66	IODATA<9> 12D6 12D7
20B2 13B4 13B3 12D7 12D6 45C3	IODATA<2>	33	67	IODATA<10> 12D6 12D7
45C3 20C1	NC_CB_CS16*	34	68	5V_TOL
		35	69	

NOTE: 5V TOLERENCE LEAVE NC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1036	1	IC,ROM,CORE2001,IBOOK	U18	PROJECT	
335S0350	1	BOOT ROM, BLANK	U18	PROJECT	OMIT

FLASH ROM

46B7
40D6 36C6 35D4 35B5 35B3 34B2 28C5
26D6 25B4 22B1 21D7 21C7 21C3 20C3
20B3 19C3 18C7 18B6 18A4 16D4 15D7 15D3
15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8 13A8 11C8
11B8 11A5 10D7 10D4 9D3 9D2 8D7
40D6 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1 7C7 7B4 7B2 6D4 6B5 5D6 3A4 +3V_MAIN
15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8
8D4 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4 8D6 8D4 8B6 7D4 7D2
13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6
21D7 21C7 21C3 20C2 20B3 19C3 18C7 18B6 18A4 16D4
46B7

+3V_MAIN

C58 0.01UF 20% 50V CERM 603
C66 0.1uF N20P80% 16V CERM 603

U18 FEPR-1MX8 110 TSOP OMIT CRITICAL

45C3 20C1 20B8 13B4 13B3 12D7 12D6					
45B3 20B8 12C6	IOADDR<0>	21	A0	DQ0	25 IODATA<0> 0
45B3 20B8 12C6	IOADDR<1>	20	A1	DQ1	26 IODATA<1> 1
45B3 20B8 12C6	IOADDR<2>	19	A2	DQ2	27 IODATA<2> 2
45B3 20B8 12C6	IOADDR<3>	18	A3	DQ3	28 IODATA<3> 3
45B3 20B8 12C6	IOADDR<4>	17	A4	DQ4	32 IODATA<4> 4
45B3 20B8 13C5	IOADDR<5>	16	A5	DQ5	33 IODATA<5> 5
45B3 20B8 13B5	IOADDR<6>	15	A6	DQ6	34 IODATA<6> 6
45B3 20B8 13B5	IOADDR<7>	14	A7	DQ7	35 IODATA<7> 7
45B3 20B8 13B5	IOADDR<8>	8	A8		
45B3 20B8 13B5	IOADDR<9>	7	A9		
45B3 20C8 13B5	IOADDR<10>	36	A10		
45B3 20C8 13B5	IOADDR<11>	6	A11		
45B3 20B8 13B5	IOADDR<12>	5	A12		
45B3 20B8 13B5	IOADDR<13>	4	A13		
45B3 20B8 13B5	IOADDR<14>	3	A14		
45B3 20B7 13B5 45B3	IOADDR<15>	2	A15		
45B3 20B8 13B5 20B6	IOADDR<16>	1	A16		
ENABLE WRITES TO BOOT BLOCK 13B5	IOADDR<17>	40	A17		
45A3 20B6 13B5	IOADDR<18>	13	A18		
45A3 20B6 13B5	IOADDR<19>	37	A19		
45A3 20B6 13B5	IOADDR<20>	38	A20		
20D7 20B6	ROM_ONBOARD_CS*	22	CE		
6A6	T_ROMOE*	24	OE		
20B6 6A6	T_ROMWE*	9	WE		
BOOTWP*		12	WP		
NOSTUFF 21C3 21B1 10C3	UNI_RESET*	10	PWD		
RESET FLASH AT RESTART			GND		23 39

+3V_MAIN
R68 1K 5% 1/16W MF 603
ENABLE WRITES TO BOOT BLOCK
NOSTUFF
R69 10K 5% 1/16W MF 603
DISABLE WRITES TO BOOT BLOCK

IODATA<7..0> 45C3 12D6 12D7 13B3 13B4 20B2 20B8 20C2 20C8

CARDSLOT(WIRELESS) INTERFACE & BOOTROM

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 20 OF 53	

CR-21

PULL-UPS

40C4 36D2 33C7
33B6 33A4 32D2
31D3 31D2 31C5
21B7 21B1 21A4 +3_3V_PMU
21D6 21C6 21B8

21C5 21B7	KEYBOARD_X2_L	1	RP1 10K 5% 1/16W SM	8
21C5 21B8	KEYBOARD_X1_L	2		7
21C5 21B7	KEYBOARD_X0_L	3		6
21C5 21A8 21A3	DELTA_KEY_L	4		5
21C5 21B8	KEYBOARD_X3_L	1	RP12 10K 5% 1/16W SM	8
21C5 21B7	KEYBOARD_X4_L	2		7
21C5 21B8	KEYBOARD_X5_L	3		6
21C5 21B7	KEYBOARD_X6_L	4		5
21C5 21B8	KEYBOARD_X7_L	5	RP10 10K 5% 1/16W SM	4
21C5 21B7	KEYBOARD_X8_L	6		3
21C6 21B8	KEYBOARD_X9_L	7		2
21B8 21B5	COMMAND_KEY_L	8		1
21B7 21B5 21A8	CONTROL_KEY_L	1	RP11 10K 5% 1/16W SM	8
21B8 21B5 21A8	SHIFT_KEY_L	2		7
21B7 21B5 21A8	OPTION_KEY_L	3		6
21B8 21B5	FN_KEY_L	4		5
21B3	PMU_NMI_L	8	RP3 10K 5% 1/16W SM	1
21C3 21C2	RESET_BUTTON_L	6		3
21C3	DNLOAD_CONFIG_L	5		4
21C3 21C2	NMI_BUTTON_L	7		2

21B7

R222 10K 5% 1/16W MF 603
21B3 RUN_OK

NEED TO CONFIRM THE PMU POWER MANAGEMENT HOOKUP TO PANGEA.
WHAT HAPPENED TO IOCLKSTOP?

33A4 32D2 31D3 31D2 31C5 21D8 21C6 21B8 21B7 21B1 21A4 +3_3V_PMU
40C4 36D2 33C7 33B6

C16 10UF 20% 6.3V TANT SMA
C11 0.1UF N20P80% 16V CERM 603
C32 0.1UF N20P80% 16V CERM 603

R23 10 5% 1/16W MF 603
+3_3V_REF_PMU 21B6 35A5 40C4
R214 10 5% 1/16W MF 603
TEMP 21B3 35A6
C33 1.0UF N20P80% 16V CERM 805
NOSTUFF R212 10K 1% 1/16W MF 603
+3V_PMU_AVCC
C186 0.1UF N20P80% 16V CERM 603

+3V_MAIN
Q4 2N3906 SM
R193 2.2K 5% 1/16W MF 603
R199 200 5% 1/16W MF 603
21B8 NUMLCK_LED
Q2 2N3906 SM
R186 2.2K 5% 1/16W MF 603
R1 200 5% 1/16W MF 603
CAPLCK_LED
21B7 21A4 21B1
33B6 33A4 32D2 31D3 31D2 31C5 21D8 21D6 21B8 40C4 36D2 33C7
+3_3V_PMU
R187 470K 5% 1/16W MF 603
R189 100K 5% 1/16W MF 603
34A8 DC_DC_EN_L
31D7 CHARGE_LED_L
21B2 POWER_UP_L

21B7	KEYBOARD_Y0	86	P00/KEYBRDY0
21B8	KEYBOARD_Y1	85	P01/KEYBRDY1
21B7	KEYBOARD_Y2	84	P02/KEYBRDY2
21B8	KEYBOARD_Y3	83	P03/KEYBRDY3
21B7	KEYBOARD_Y4	82	P04/KEYBRDY4
21B8	KEYBOARD_Y5	81	P05/KEYBRDY5
21B8	KEYBOARD_Y6	80	P06/KEYBRDY6
21B7	KEYBOARD_Y7	79	P07/KEYBRDY7
	NUMLOCK_LED_L	78	P10/NUMBLOCK_LED
	CAPSLOCK_LED_L	77	P11/CAPSLOCK_LED
		76	P12/RUN_LED
		75	P13/SLEEP_LED
		74	P14/BACKUP_SELECT
21D8 21A8 21A3	DELTA_KEY_L	73	P15/DELTAKEY
16C3 14B3 13C7	RING_DETECT*	72	P16
13A7	KW_WATCHDOG*	71	P17/WATCHDOG_KW
21D8 21B7	KEYBOARD_X0_L	70	P20/KEYBOARDX0
21D8 21B8	KEYBOARD_X1_L	69	P21/KEYBOARDX1
21C3 21B7	KEYBOARD_X2_L	68	P22/KEYBOARDX2
21D8 21B8	KEYBOARD_X3_L	67	P23/KEYBOARDX3
21D8 21B7	KEYBOARD_X4_L	66	P24/KEYBOARDX4
21D8 21B8	KEYBOARD_X5_L	65	P25/KEYBOARDX5
21D8 21B7	KEYBOARD_X6_L	64	P26/KEYBOARDX6
	KEYBOARD_X7_L	63	P27/KEYBOARDX7
21D8 21B8	JIS_KBD	61	P30/KEYBOARDX8
21D8 21B7	KEYBOARD_X8_L	61	P31/KEYBOARDX9
21B8	KEYBOARD_X9_L	59	P32/KEYBOARDX10
21D8	IO_RESET_L	58	P33/COMMAND_KEY
21D8 21B8	COMMAND_KEY_L	57	P34/CONTROL_KEY
21D8 21B7 21A8	CONTROL_KEY_L	56	P35/SHIFT_KEY
21D8 21B8 21A8	SHIFT_KEY_L	55	P36/OPTION_KEY
21C8 21B7 21A8	OPTION_KEY_L	54	P37/FN_KEY
21C8 21B8	FN_KEY_L	53	
14C3 13C7	PMU_INT	52	P40/PMU_INT
21B8	KBD_ID	51	P41/KBD_ID
4C6	CPU_PLL_STOP_OC	50	P42/CPU_PLL_0
		49	P43/CPU_PLL_1
38B8 35D4 27C8 7B7 35C4 34A8	SLEEP	48	P44/SLEEP
5B7	IOCLOCKSTOP_L	47	P45/SUSPENDREQ_IOCLOCKSTOP
	PANGEA_SUSP_ACK*	46	P46/SUSPENDACK
	PANGEA_SUSP_REQ*	45	P47/SUSPENDREQ
	BYTE	6	BYTE
45A4	PMU_10MHZ_XOUT	11	XOUT
45A4	PMU_10MHZ_XIN	13	XIN
		10	RESET
40C4 35A5 21D3	+3_3V_REF_PMU	96	VREF
21A2	CNVSS	7	CNVSS
		14 60	VCC
		97	AVCC
		12 62	VSS
		94	AVSS

P50/MONON_10K_PULL_CE_VCC
P51/UNIN_RESET
P52/PCI_RESET
P53/CPU_SRST_0
P54/CPU_SRST_1
P55/PRCSLPREQ_100KEMP_GND
P56/POWERONCLEAR
P57/CPU_HRST
P60/CPU_SMI_0
P61/CPU_SMI_1
P62/TRACKPAD_OUTPUT
P63/TRACKPAD_INPUT
P64/RUN_OK_BUSY
P65/LID_SWITCH_SCLK
P66/RXD
P67/TXD
P70/CC_SDA
P71/CC_SCL
P72/CC_0
P73/CC_1
P74/CHARGEV
P75/CHG_BATT_0
P76/CHARGE1
P77/CHG_BATT_1
P80/DC_DC
P81/ACK
P82/REQ
P83/PME
P84/PENDINGPROCINT
P85/100K_PULL_UP
P86/32KHZ_XTAL
P87/32KHZ_XTAL
P90/SCK
P91/MISO
P92/MOSI
P93/SMB_SEL
P94/SMB_SCK
P95/SMB_SDA
P96/OOPS_RESET
P97/OOPS
P100/TEMP
P101/AC_VOLT
P102/AC_ID
P103
P104/BATT_IN_0
P105/BATT_IN_1
P106/RUN_BATT_0
P107/RUN_BATT_1

U13 M16C62 FLAS CRITICAL

44	CPU_VCORE_HI_OC	4A4 4B6 6B8 6C5 38A4 38B4	
43	UNI_RESET*	10C3 20B3 21B1	
42	EQ_RESET_L		
41	NC		
40	PMU_NMI_IRQ*	13C7 14C3	
39	DNLOAD_CONFIG_L	21C8	
38	UNI_PU_RESET*	10C3 21B1	
37	CPU_HRST	14A8 15B3	
36	T_PMU_ACK*	21C2	
35	PMU_SCK	13C5	
34	PMU_MISO	13C5	
33	PMU_MOSI	13C5	
32	PMU_REQ*	13C5 14C3	
31	LID_CLOSED_L	21B2 24A4	
30	RESET_BUTTON_L	21C2 21C8	
29	NMI_BUTTON_L	21C2 21C8	
28	TRKPAD_RXD		
27	TRKPAD_TXD		
26	STOPXTAL*	6C8 13A8	
25	CPU_STOP_CLK*	5A8	
24	CHARGE_V	32B1	
23	PMU_CHRG_BATT_0	33C7	
22	CHARGE_I	32C1	
20	CPU_STATE_LED_L	21C6	
19			
18	MAIN_GOOD		
17	PME*	13B8 25B2	
16	KW_PEND_PROC_INT	13B7	
15	PMU_NMI_L	21C8	
9	PMU_32KHZ_XOUT		
8	PMU_32KHZ_XIN		
5	BATT_IN_0_L	33A4	
4	BATT_IN_1_L	21B2	
3	NC (RUN_BATT_0)		
2	NC (RUN_BATT_1)		
1	KW_PROC_SLEEP_REQ*	13B7	
100	RUN_OK	21C8	
99	NC		
98	OOPS	21A2	
95	TEMP	21D3 35A6	
93	PMU_AC_IN	31B4	
92	PMU_AC_DET	31B4	
91	NC (SMB_SEL)		
90	PMU_IIC_CLK	6D5 15C8	
89	PMU_IIC_DAT	6C5	
88	SMB_CLK	15B8 21B2	
87	SMB_SDA	21B2 33B4	

R216 4.7K 5% 1/16W MF 603
+5V_IO_SLEEP 21D2 25D8 28D5 35B2 35B5 40C6
R218 10K 5% 1/16W MF 603
R26 100K 5% 1/16W MF 603
+3V_MAIN

R1554 10K 5% 1/16W MF 603
RESET_KEY_L 21A3 21A6

NOSTUFF R223 0 5% 1/16W MF 603
R224 0 5% 1/16W MF 603
CRITICAL Y2 SM 32.768K
C38 10PF 5% 50V CERM 603
C37 10PF 5% 50V CERM 603

TRACKPAD CONN.

+5V_IO_SLEEP
L28 400-OHM-EMI SM-1
C318 0.1UF N20P80% 16V CERM 603
C633 10PF 5% 50V CERM 603
NOSTUFF C322 0.01UF 5% 50V CERM 603
POWER2_CHGND

L30 400-OHM-EMI SM-1
21C4 TRKPAD_TXD
C323 0.001UF 5% 50V CERM 603
C634 10PF 5% 50V CERM 603

L31 400-OHM-EMI SM-1
21C4 TRKPAD_RXD
C326 0.001UF 5% 50V CERM 603
C635 10PF 5% 50V CERM 603

J11 SM

L32 400-OHM-EMI SM-1
39C2 21D1 21C1 POWER2_CHGND
GND_TRACKPAD
C636 10PF 5% 50V CERM 603
C637 470PF 10% 50V CERM 603
39C2 21D2 21D1 21C2 POWER2_CHGND

R206 0 5% 1/16W MF 603
21C3 T_PMU_ACK* PMU_ACK* 13C5

NOSTUFF R213 0 5% 1/16W FF 805
21C8 21C3 RESET_BUTTON_L
NOSTUFF R215 0 5% 1/16W FF 805
21C8 21C3 NMI_BUTTON_L

ADD SILKSCREEN BOX
MUST BE PLACE TOP OF MLB
R213 AND R215 PADS FOR DEVELOPMENT ONLY

RP2 100K 5% SM

21C3 10C3	UNI_PU_RESET*	8
21C3 20B3 10C3	UNI_RESET*	7
21B5 5B8	PANGEA_SUSP_REQ*	6
22B8 21B5 20B6	IO_RESET_L	5

R17 100K 5% 1/16W MF 603
31D7 31B5 AC_ID
R14 7.68K 1% 1/16W MF 603
33B4 21B3 SMB_SDA
R202 7.68K 1% 1/16W MF 603
33B4 21B3 SMB_CLK
+3_3V_PMU
33B6 33C7 36D2 21D8 31C5 31D2 21A4 21B1 21B7 21B8 21C6 21D6 31D3 32D2 33A4 40C4

RP13 100K 5% 1/16W SM

21B3	BATT_IN_1_L	2
24A4 21C3	LID_CLOSED_L	3
21C6	POWER_UP_L	4

+3_3V_PMU
33B6 33C7 36D2 21D8 31C5 31D2 21A4 21B1 21B7 21B8 21C6 21D6 31D3 32D2 33A4 40C4

R20 10K 5% 1/16W MF 603
21B6 CNVSS
R217 10K 5% 1/16W MF 603
21B3 OOPS

KEYBOARD CONN.

40C4 36D2 33C7
31D3 31D2 31C5
21B7 21B1 21A4 +3_3V_PMU
21D8 21D6 21C6
33B6 33A4 32D2

R190 100K 5% 1/16W MF 603
R263 0 5% 1/16W MF 603

J6 SM

21B5	KBD_ID	1	2
21C6	JIS_KBD	3	4
21C8 21B5	FN_KEY_L	5	6
21D8 21B5	COMMAND_KEY_L	7	8
21D8 21B5 21A8	SHIFT_KEY_L	9	10
21D8 21B5 21A8	KEYBOARD_X1_L	11	12
21D8 21C5	KEYBOARD_X3_L	13	14
21D7	NUMLCK_LED	15	16
21D8 21C5	KEYBOARD_X5_L	17	18
21D8 21C5	KEYBOARD_X7_L	19	20
21D8 21C6	KEYBOARD_X9_L	21	22
21C5	KEYBOARD_Y1	23	24
21C5	KEYBOARD_Y3	25	26
21C5	KEYBOARD_Y5	27	28
21C5	KEYBOARD_Y6	29	30

INTL_KBD
CAPLCK_LED 21C7
CONTROL_KEY_L 21A8 21B5 21C8
21D8 KEYBOARD_X0_L 21C5 21D8
KEYBOARD_X2_L 21C5 21D8
KEYBOARD_X4_L 21C5 21D8
KEYBOARD_X6_L 21C5 21D8
KEYBOARD_X8_L 21C5 21D8
KEYBOARD_Y0 21D5
KEYBOARD_Y2 21C5
KEYBOARD_Y4 21C5
KEYBOARD_Y7 21C5

35D4 35B5 35B3 34B2 28C5 26D6 25B4
18C7 18B6 18A4 16D4 15D7 15D3 15C2
13A8 11C8 11B8 11A5 10D7 10D4 9D3
7C7 7B4 7B2 6D4 6B5 5D6 3A4
9D2 8D7 8D6 8D4 8B6 7D4 7D2
14D2 14C3 14B3 13D6 13C8 13C3 13B8
22B1 21D7 21C3 20C3 20C2 20B3 19C3
46B7 40D6 36C6

+3V_MAIN
Q10 2N3906 SM
R27 2.2K 5% 1/16W MF 603
CPU_STATE_LED_L
21A8 SLEEP_LED
R25 10 5% 1/16W MF 603

R3 0 5% 1/16W MF 603
21B8 JIS_KBD

NOSTUFF R550 100K 5% 1/16W MF 603
PLACE_ON_TOP_SIDE REESE RESERVE FOR TEST
NC
21A8 21B5 21C8

R2 100K 5% 1/16W MF 603
21B1 5B8

40C4
31C5 21D8 21D6 21C6 21B8 21B1 21A4 +3_3V_PMU
36D2 33C7 33B6 33A4 32D2 31D3 31D2

U800 74LVC32 TSSOP
21D8 21C5 21A3 DELTA_KEY_L
21D8 21B7 21B5 CONTROL_KEY_L
21D8 21B8 21B5 SHIFT_KEY_L
21C8 21B7 21B5 GND_VCOREOUTPUT
OPTION_KEY_L
RESET_KEY_L 21A3
NC
21A3 38B2 38B5 38B7 38C1 38C4 38C5 38C8 38D3

R226 10M 5% 1/16W MF 603 NOSTUFF
R225 0 5% 1/16W MF 603
Y3 10MHZ SM
C42 12PF 5% 50V CERM 603
C41 12PF 5% 50V CERM 603
PLACE C543, C544 VERY CLOSE TO PIN 12 U39

R21 1K 5% 1/16W MF 603

U14 SOT23-2.63V MAX6326 RESET
NOSTUFF R30 4.7K 5% 1/16W MF 603
NOSTUFF D5 1N914 SOT23
NOSTUFF R19 10K 5% 1/16W MF 603
PMU_RESET_L
CRITICAL Q11 SOT MC33465 INPUT MC33465 RESET* CD GND NC
C192 0.1UF N20P80% 16V CERM 603
NOSTUFF C188 4.7UF 20% 6V CERM 1206

NOSTUFF C1540 470PF 10% 20V CERM 603
NOSTUFF C1541 10PF 5% 50V CERM 603
NOSTUFF C1542 18PF 5% 50V CERM 603
GND_VCOREOUTPUT 21A8 38B2 38B5 38B7 38C1 38C4 38C5 38C8 38D3

DELTA KEY

S1 SM-2MT
R594 1K 5% 1/16W MF 603
21D8 21C5 21A8 DELTA_KEY_L
+3_3V_PMU 32D2 33A4 33B6 33C7 36D2 40C4 21B1 21B7 21B8 21C6 21D6 21D8 31C5 31D2 31D3
NOSTUFF ZD4 1N5233B SOT23

RESET BUTTON

39A7 25B6 25B5 25B3 25A5 21A6 21A3
VGA_CHASSIS_GND
RESET_KEY_L
S4 SM-2MT NOSTUFF

L61 400-OHM-EMI SM-1
21C8 SLEEP_LED
C473 470PF 10% 16V CERM 603
C477 0.01UF 5% 50V CERM 603
S2 SM-2MT

PMU (POWER MANAGEMENT UNIT)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

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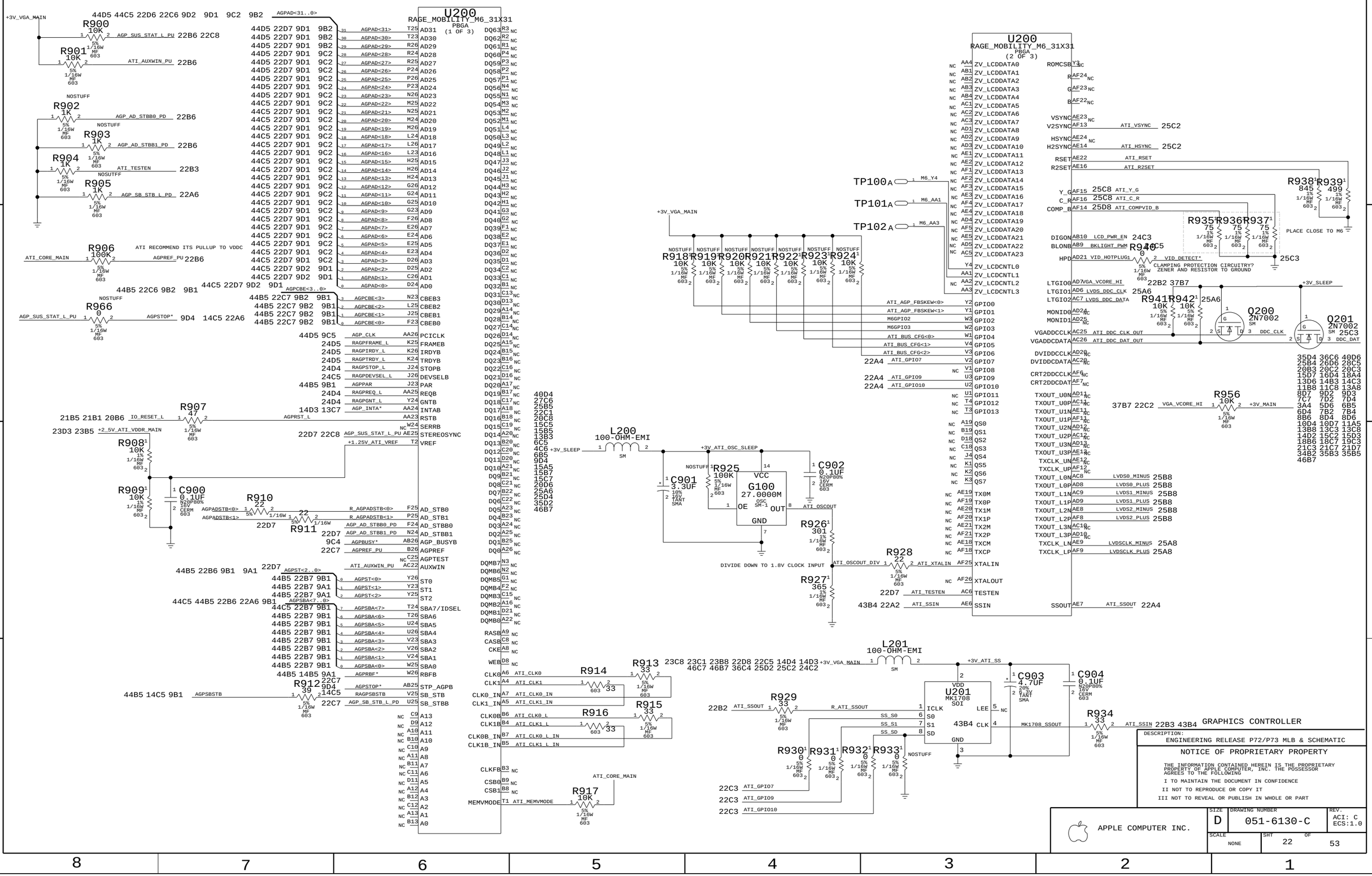
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 21 OF 53	

CR-22


U200
RAGE_MOBILITY_M6_31X31
PBGA
(1 OF 3)
U200
RAGE_MOBILITY_M6_31X31
PBGA
(2 OF 3)
+3V_VGA_MAIN
R900 10K
R901 10K
R902 1K NOSTUFF
R903 1K
R904 1K
R905 1K NOSTUFF
R906 100K
R907 47
R908 10K
R909 10K
C900 0.1UF
R910 22
R911 22
R912 39
R966 0 NOSTUFF
AGP_SUS_STAT_L_PU 22B6 22C8
ATI_AUXWIN_PU 22B6
AGP_AD_STBB0_PD 22B6
AGP_AD_STBB1_PD 22B6
ATI_TESTEN 22B3
AGP_SB_STB_L_PD 22A6
ATI RECOMMEND ITS PULLUP TO VDDC
AGPREF_PU 22B6
IO_RESET_L
+2.5V_ATI_VDDR_MAIN
+1.25V_ATI_VREF
AGPADSTB<0>
AGPADSTB<1>
AGP_AD_STBB0_PD
AGP_AD_STBB1_PD
AGPBUSY*
AGPREF_PU
ATI_AUXWIN_PU
AGPSTOP*
AGPSBSTB
AGP_SB_STB_L_PD
AGP_CLK
RAGPFRAME_L
RAGPIRDY_L
RAGPTRDY_L
RAGPSTOP_L
RAGPDEVSEL_L
AGPPAR
RAGPREQ_L
RAGPGNT_L
AGP_INTA*
AGPRST_L
RAGPSBSTB
AGPAD<31..0>
AGPCBE<3..0>
AGPST<2..0>
AGPSBA<7..0>
AGPRBF*
TP100A M6_Y4
TP101A M6_AA1
TP102A M6_AA3
R918 R919 R920 R921 R922 R923 R924 10K NOSTUFF
ATI_AGP_FBSKEW<0>
ATI_AGP_FBSKEW<1>
M6GPIO2
M6GPIO3
ATI_BUS_CFG<0>
ATI_BUS_CFG<1>
ATI_BUS_CFG<2>
ATI_GPIO7
ATI_GPIO9
ATI_GPIO10
ROMCSB
R
G
B
VSYNC
V2SYNC
HSYNC
H2SYNC
RSET
R2SET
Y_G
C_R
COMP_B
DIGON
BLONB
HPD
LTGIO0
LTGIO1
LTGIO2
MONID0
MONID1
VGADDCCLK
VGADDCDATA
DVIDDCCLK
DVIDDCDATA
CRT2DDCCLK
CRT2DDCDAT
TXOUT_U0N
TXOUT_U0P
TXOUT_U1N
TXOUT_U1P
TXOUT_U2N
TXOUT_U2P
TXOUT_U3N
TXOUT_U3P
TXCLK_UN
TXCLK_UP
TXOUT_L0N
TXOUT_L0P
TXOUT_L1N
TXOUT_L1P
TXOUT_L2N
TXOUT_L2P
TXOUT_L3N
TXOUT_L3P
TXCLK_LN
TXCLK_LP
ATI_VSYNC 25C2
ATI_HSYNC 25C2
ATI_RSET
ATI_R2SET
ATI_Y_G 25C8
ATI_C_R 25C8
ATI_COMPVID_B 25D8
LCD_PWR_EN 24C3
BKLIGHT_PWM 24C5
VID_HOTPLUG1
VID_DETECT*
CLAMPING PROTECTION CIRCUITRY?
ZENER AND RESISTOR TO GROUND
PLACE CLOSE TO M6
VGA_VCORE_HI 22B2 37B7
LVDS_DDC_CLK 25A6
LVDS_DDC_DATA
ATI_DDC_CLK_OUT
ATI_DDC_DAT_OUT
DDC_CLK
DDC_DAT
+3V_SLEEP
+3V_ATI_SS
+3V_MAIN
R956 10K
R938 845
R939 499
R940 0
R941 10K
R942 10K
R935 R936 R937 75
0200 2N7002
0201 2N7002
L200 100-OHM-EMI
L201 100-OHM-EMI
+3V_ATI_OSC_SLEEP
C901 3.3UF
C902 0.1UF
C903 4.7UF
C904 0.1UF
R925 100K NOSTUFF
G100 27.0000M OSC SM-1
R926 301
R927 365
R928 22
ATI_OSCOUT
ATI_OSCOUT_DIV
ATI_XTALIN
DIVIDE DOWN TO 1.8V CLOCK INPUT
U201 MK1708 SOI
ATI_SSOUT
R_ATI_SSOUT
SS_S0
SS_S1
SS_SD
MK1708_SSOUT
ATI_SSIN 22B3 43B4
R929 33
R930 R931 R932 R933 0 NOSTUFF
R934 33
R914 R915 R916 R917 R913 33
ATI_CLK0
ATI_CLK1
ATI_CLK0_IN
ATI_CLK1_IN
ATI_CLK0_L
ATI_CLK1_L
ATI_CLK0_L_IN
ATI_CLK1_L_IN
ATI_CORE_MAIN
ATI_MEMVMODE
GRAPHICS CONTROLLER
DESCRIPTION:
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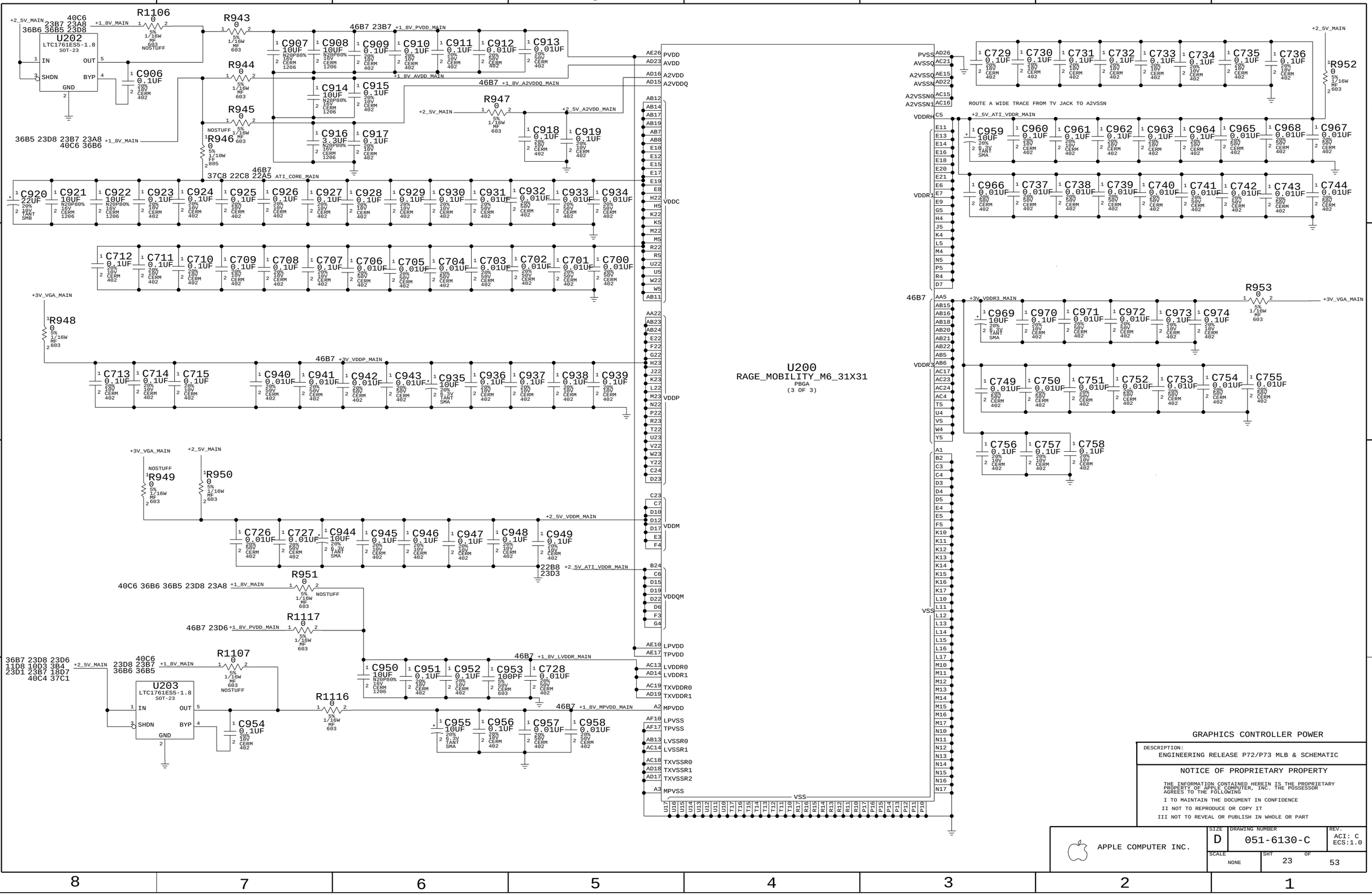
SIZE D
DRAWING NUMBER 051-6130-C
REV. ACI: C ECS:1.0
SCALE NONE
SHT 22 OF 53



GRAPHICS CONTROLLER POWER

DESCRIPTION:
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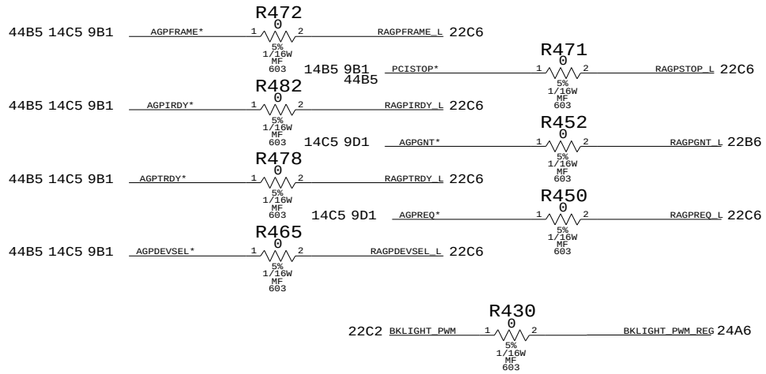
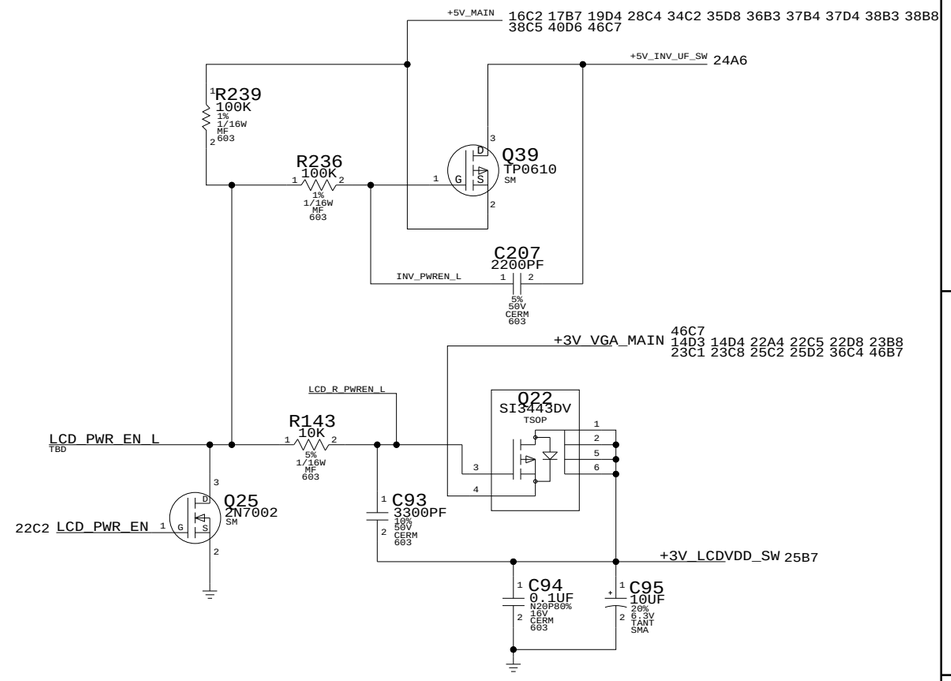
APPLE COMPUTER INC.

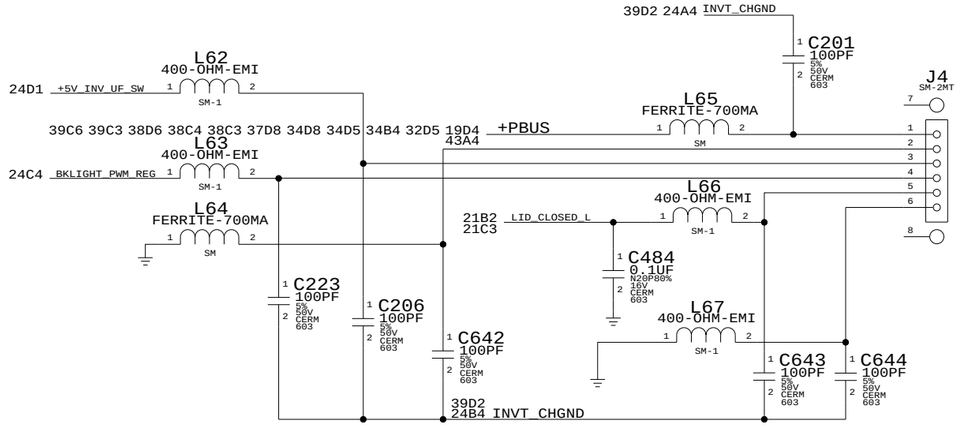
SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 23 OF 53	

AGP BUS SERIES TERM





INVERTER CONNECTOR



EMC_GND DETERMINED BY ATC LAYOUT

LCD I/F

DESCRIPTION:
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 24 OF 53	

Video Connectors

EXTERNAL VIDEO (VGA) INTERFACE

NOTES:

DUE TO EMI CONCERNS,THE FOLLOWING PINS(WHICH ARE LOCATED OVER THE CORRECT PORTION OF THE VGA_CHASS_GND1 PLANE) ARE CONNECTED TO THE VGA_CHASS_GND1 PLANE AS WELL AS DIGITAL GROUND.....
R90-2, C69-2, C70-2, C76-2, FL2-3/4, FL4-3/4, J12-1/4/6/14, C338-2, C339-2, C340-2, C344-2,

35B2 28D5 21D2 21C3 40C6 35B5 +5V_IO_SLEEP — F3 0.5AMP SM — 46C7 40C6 +5V_VGA_FUSE — L33 400-OHM-EMI SM-1 — 46C7 +5V_VGADDCPWR_SLEEP_F

+3V_SLEEP 4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8 20D6 22B5 22C1 25A6 25B5 27C6 35D2 40D4 46B7

FL2 LCFILTER SM-100MHZ NOSTUFF

22C2 ATI_COMPVID_B — L5 0.068UH SM — ATI_B_FILTR — L4 0.068UH SM

FL3 LCFILTER SM-100MHZ NOSTUFF

C69 4.7PF +/-0.25PF 50V CERM 603

C70 3.3PF 5% 50V CERM 603

CLOSE TO VGA CONNECTOR J12

22C2 ATI_Y_G — L6 0.068UH SM — ATI_G_FLTR — L7 0.068UH SM

C72 4.7PF +/-0.25PF 50V CERM 603

C73 3.3PF 5% 50V CERM 603

22C2 ATI_C_R — L8 0.068UH SM — ATI_R_FILTR — L9 0.068UH SM

C78 4.7PF +/-0.25PF 50V CERM 603

FL4 LCFILTER SM-100MHZ NOSTUFF

C76 3.3PF 5% 50V CERM 603

J12 TCX3160 TH-2MT

VGA_B, VGA_G, VGA_R, VGA_CHASS_GND1

R322 4.7K 5% 1/16W MF 603 — VID_DETECT* 22C1

R335 1K 5% 1/16W MF 603 — DDC_CLK 22C1

R338 1K 5% 1/16W MF 603 — DDC_DAT 22C1

VGA_VSYNC 25C1

VGA_HSYNC 25C1

C338 100PF 5% 50V CERM 603

C340 100PF 5% 50V CERM 603

C344 100PF 5% 50V CERM 603

+3V_VGA_MAIN 14D3 14D4 22A4 22C5 22D8 23B8 23C1 23C8 24C2 25C2 36C4 46B7 46C7

22D2 ATI_VSYNC — U21 74AHC1G32 SM — ATI_VSYNC_BUF — R350 33 5% 1/16W MF 603 — VGA_VSYNC 25C4

+3V_VGA_MAIN 14D3 14D4 22A4 22C5 22D8 23B8 23C1 23C8 24C2 25D2 36C4 46B7 46C7

22D2 ATI_HSYNC — U204 74AHC1G32 SM — R346 33 5% 1/16W MF 603 — VGA_HSYNC 25C4

LCD (LVDS) INTERFACE

39A7 25B6 25B5 25A5 21A3 — VGA_CHASS_GND — C975 0.01UF 20% 50V CERM 603 — CHGND3 — 28A4 28A5 28B1 28B2 28C1 28D1 28D3

L11 FERR-250-OHM — 46B7 40D4 35D2 27C6 25D4 25A6 22C1 22B5 46B7 15B5 15A5 13B3 9D4 6C5 6B5 4C6 20D6 20C8 15C7 15C5 — +3V_SLEEP

24C1 +3V_LCDVDD_SW — +3V_LCDVDD_SW_F

C356 0.001UF 20% 50V CERM 603

C357 0.001UF 20% 50V CERM 603

R380 10K 5% 1/16W MF 603

R381 10K 5% 1/16W MF 603

J15 E-RT-20228 SM

VGA_CHASS_GND 21A3 25A5 25B3 25B5 39A7 — 25B3 25A5 21A3 39A7 25B6 VGA_CHASS_GND

C379 10PF 5% 50V CERM 603

C375 10PF 5% 50V CERM 603

C378 10PF 5% 50V CERM 603

C377 10PF 5% 50V CERM 603

22B2 LVDS0_MINUS
22B2 LVDS0_PLUS
22B2 LVDS1_MINUS
22B2 LVDS1_PLUS
22B2 LVDS2_MINUS
22B2 LVDS2_PLUS
22B2 LVDSCLK_MINUS
22B2 LVDSCLK_PLUS

C376 10PF 5% 50V CERM 603

C374 10PF 5% 50V CERM 603

C381 10PF 5% 50V CERM 603

C380 10PF 5% 50V CERM 603

22C2 LVDS_DDC_CLK
22C2 LVDS_DDC_DATA

46B7 40D4 35D2 27C6 25D4 25B5 15B5 15A5 13B3 9D4 6C5 6B5 4C6 22C1 22B5 20D6 20C8 15C7 15C5 15B7 — +3V_SLEEP

(LVDS DDC POWER)

39A7 25B3 21A3 25B6 25B5 — VGA_CHASS_GND

C358 0.001UF 20% 50V CERM 603

C359 0.001UF 20% 50V CERM 603

PME* 13B8 21B3

28C3 13C5 16D4 SCC_RXDA — R959 470K 5% 1/16W MF 603 — Q211 2N7002 SM

R967 1K 5% 1/16W MF 603 — SCC_RTSA* — SLINK_TX_ENABLE_L

C1210 0.01UF 5% 50V CERM 603

+3V_MAIN

13D5 16C1 SCC_TXDA* — U210 74LVC1G125 125 SOT — R960 470 5% 1/16W MF 603 — R961 47K 5% 1/16W MF 603

VIDEO CONNECTOR

DESCRIPTION:
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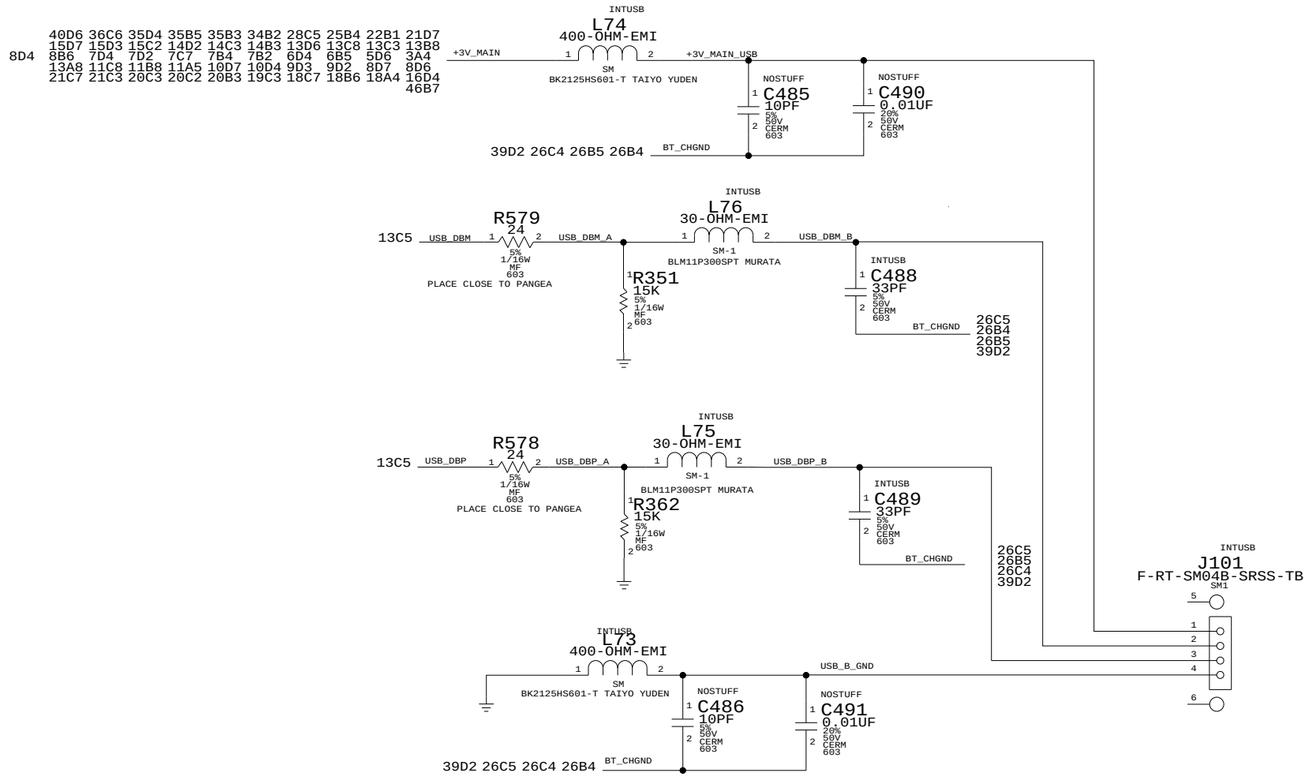
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0

SCALE NONE | SHT 25 OF 53

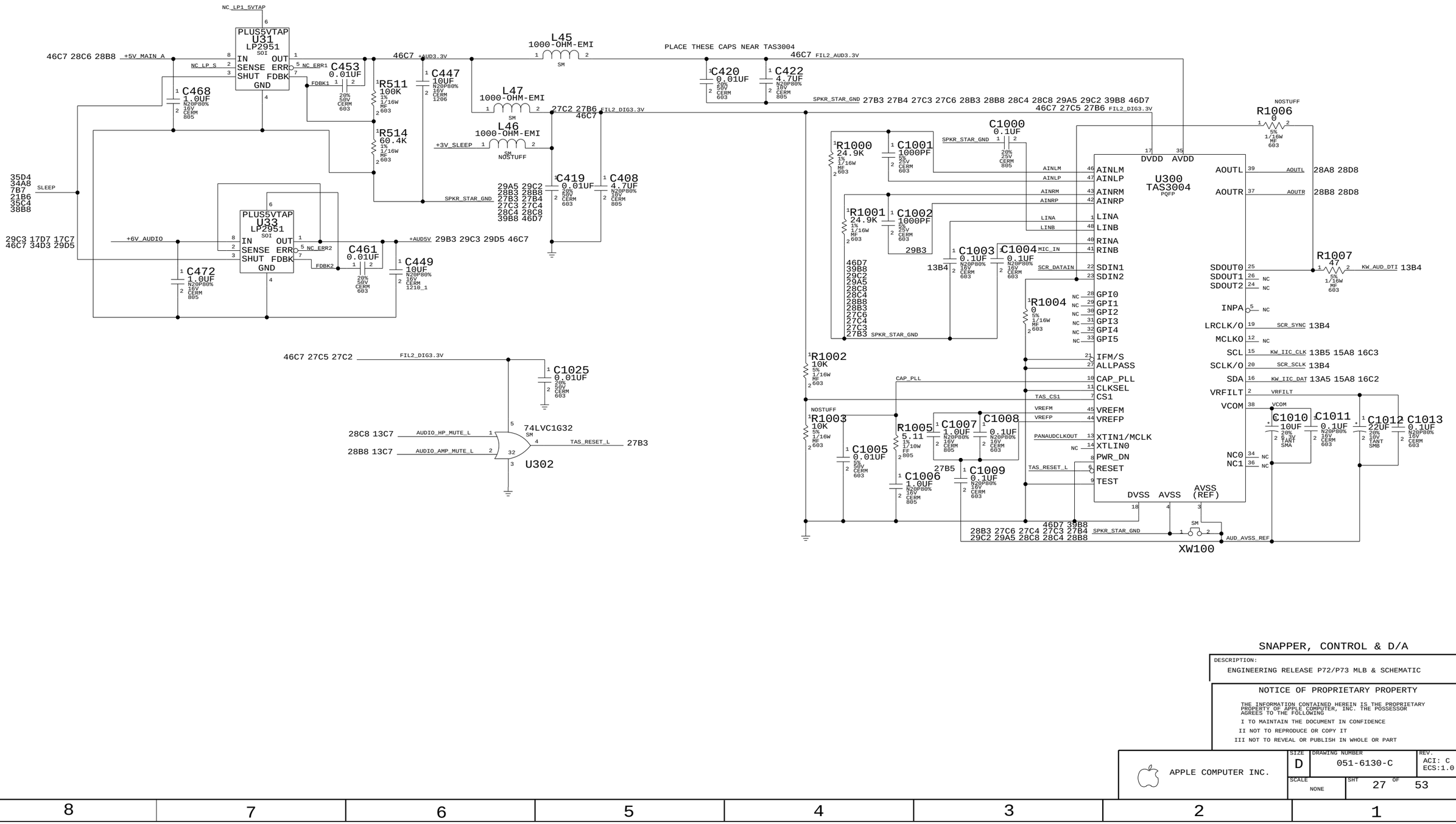


IRDA/BT USB CONNECTOR

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 26 OF 53	



SNAPPER, CONTROL & D/A

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 27 OF 53	

CR-28

SNAPPER AUDIO, SPEAKER & HEADPHONE DRIVER

NOTE: L37 NEAR J13

25MIL TRACE TO C101 PIN1

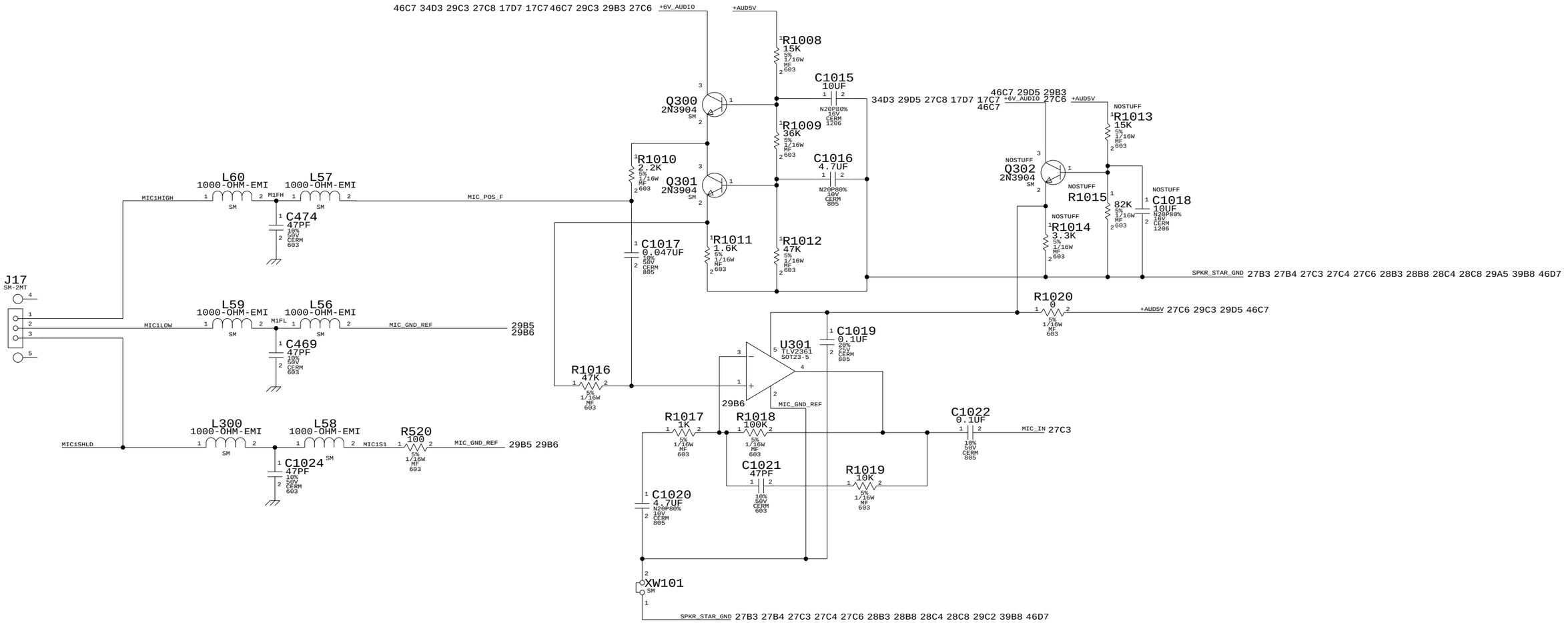
25MILS TRACE

25MIL TRACE TO C101 PIN2

DESCRIPTION:	ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6130-C	REV: ACI: C ECS:1.B
	SCALE: NONE	SHT: 28 OF 53	

CR-29



DESCRIPTION:
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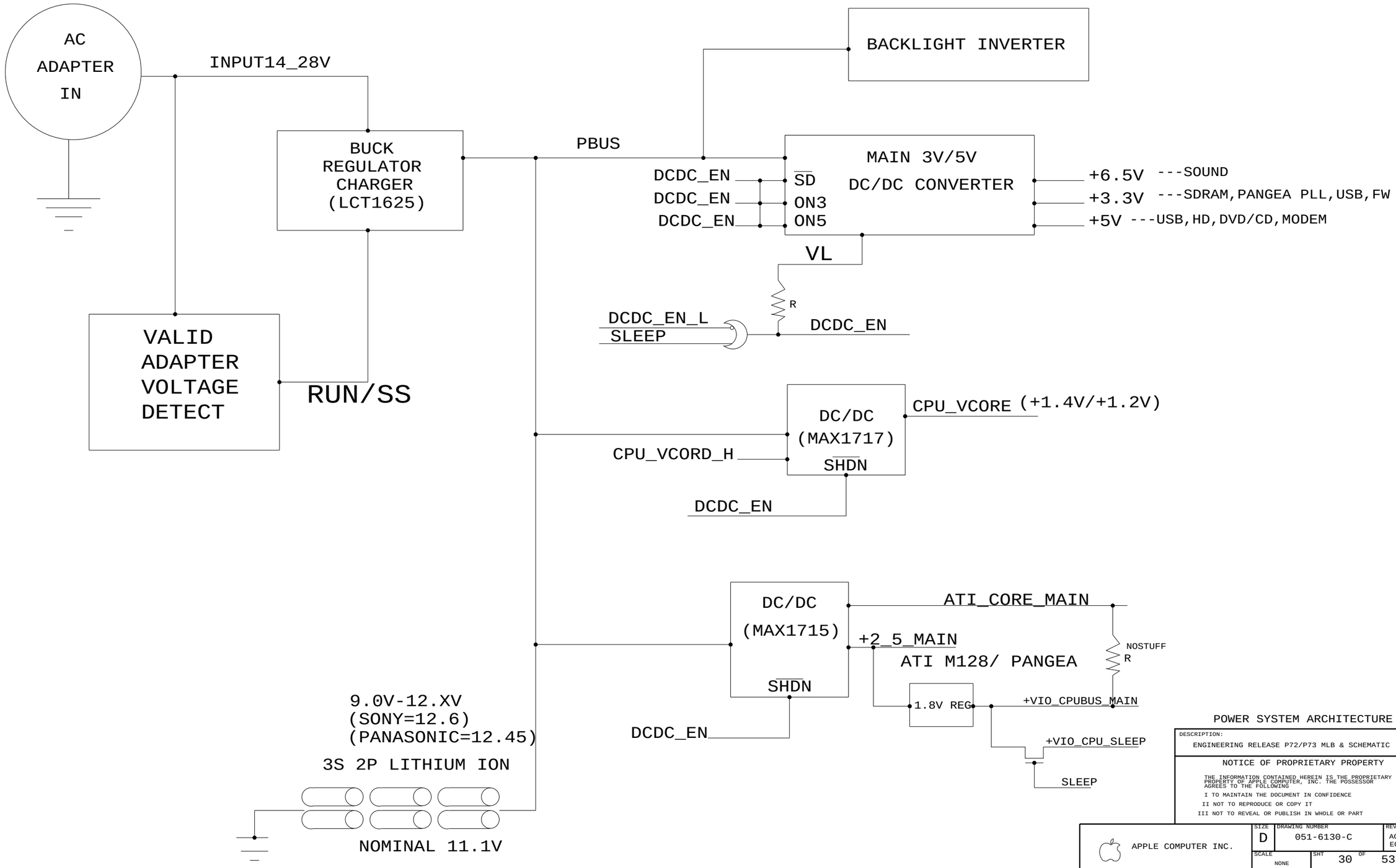
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 29 OF 53	

SNAPPER AUDIO, MICROPHONE PREAMP

POWER SYSTEM ARCHITECTURE



POWER SYSTEM ARCHITECTURE

DESCRIPTION:
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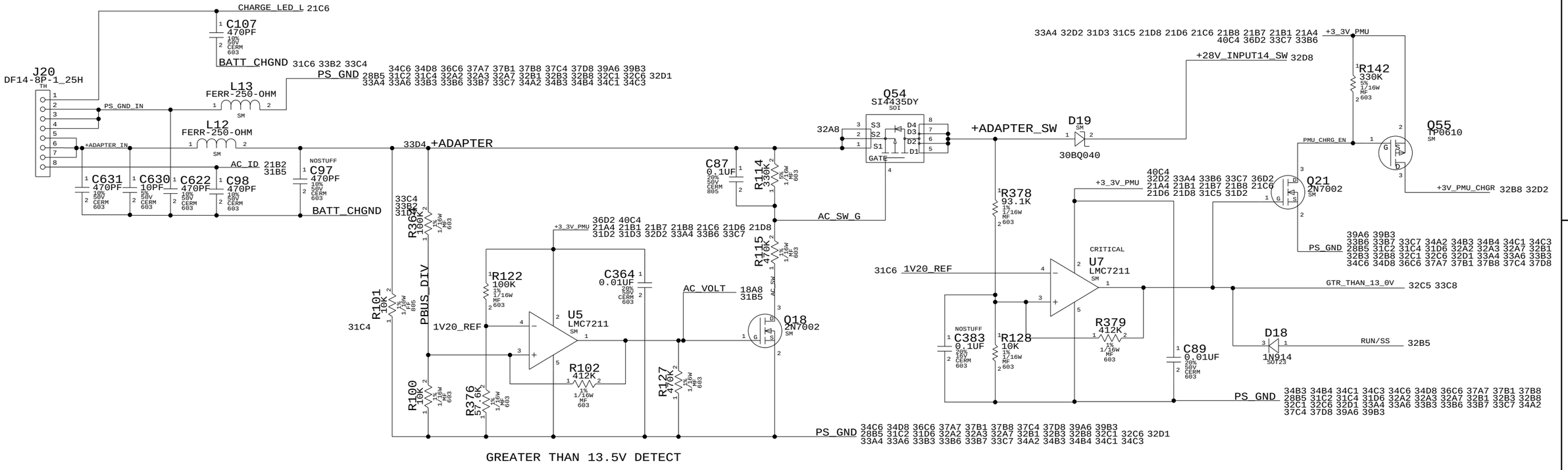
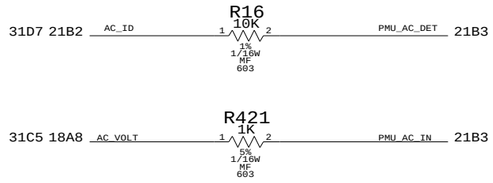
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE	SHT	OF
NONE	30	53





DC-JACK INTERFACE

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 31 OF 53	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S2873	1	CHIP RES 1/16W 1% 2.87K 0603 ACI	R539	SLOW_CHRG
110S2613	1	CHIP RES 1/16W 1% 2.61K 0603 ACI	R539	FAST_CHRG

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
103S0568	1	CHIP RES 1/16W .1% 15.4K 0603 ACI	R495	3SBAT
103S0612	1	CHIP RES 1/16W .1% 11.3K 0603 ACI	R495	4SBAT
110S3012	1	CHIP RES 1/16W 1% 301 0603 ACI	R496	3SBAT
110S1502	1	CHIP EWS 1/16W 1% 150 0603 ACI	R496	4SBAT

ITH_1625

BATTERY CHARGER

DESCRIPTION:
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APPLE COMPUTER INC.

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SCALE: NONE	SHT 32 OF 53	

BATTERY INTERFACE

31D6 +ADAPTER — D20 1N914 — ADAPT_D1 — D21 1N914 — ADAPT_D2 — D22 1N914 (SOT23)

32D1 BATT_LINE

C435 0.01UF, C436 0.01UF, C441 0.01UF (NOSTUFF, 20% 50V CERM 603) — PS_GND

Q67 FDS6975 SM
34A2 34B3 34B4
32D1 33A4 33A6
32A7 32B1 32B3
28B5 31C2 31C4
31D6 32A2 32A3
32B8 32C1 32C6
33B3 33B6 33B7
34C1 34C3 34C6
34D8 36C6 37A7
37B1 37B8 37C4
37D8 39A6 39B3

BATT_RES — R490 56 5% 1W FF 2512 OMIT — R483 56 5% 1W FF 2512 OMIT — R506 56 5% 1W FF 2512 OMIT — D10 SM 30BQ040 — BATT_POS_F

D32 SM MBR0540 — REG2_IN 36D8

L50 60-OHM-EMI SM

STATE	+3_3V_PMU	GTR_THAN_13_0V	PMU_CHRG_BATT_0
ONLY BATTERY	H	L	L
ONLY ADAPTER	H	H	L
CHARHER	H	H	H CHANGE L

PWR_FET_S2 — R169 470K 1% 1/16W MF 603 — AC_OR_BATT_PWR

21C3 PMU_CHRG_BATT_0 — D33 1N914 SOT23

C459 0.01UF 20% 50V CERM 603 — R168 330K 5% 1/16W MF 603 — ADAPTER_PWR_DRAIN

GTR_THAN_13_0V — D29 1N914 SOT23 — R459 470K 5% 1/16W MF 603

33B6 36D2 31D2 31D3 21C6 21D6 21A4 21B1 21B7 21B8 21D8 31C5 32D2 33A4 40C4 — +3_3V_PMU — R163 330K 5% 1/16W MF 603

R162 10K 1% 1/16W MF 603 — BATT_FET_DRAIN — ADAPTER_PWR_SW — Q71 2N7002 SM

Q28 2N7002 SM — BATT_RC — C427 0.047UF 5% 16V CERM 603

PS_GND 34C6 34D8 36C6 37A7 37B1 37B8 37C4 37D8 39A6 39B3 28B5 31C2 31C4 31D6 32A2 32A3 32A7 32B1 32B3 32B8 32C1 32C6 32D1 33A4 33A6 33B3 33B6 33C7 34A2 34B3 34B4 34C1 34C3

PS_GND 34D8 36C6 37A7 37B1 37B8 37C4 32D1 33A4 33A6 33B3 33B7 33C7 34A2 34B3 34B4 34C6 28B5 31C2 31D6 32A2 32A3 32A7 32B1 32B3 32B8 32C1 32C6 34A2 34B3 34B4 34C1 34C3 34C6 37D8 39A6 39B3

Q30 SI4435DY SOI — S3 S2 S1 GATE — D4 D3 D2 D1

R512 39.2K 1% 1/16W MF 603 — BYPASS_R_GATE — R170 35.7K 1% 1/16W MF 603

33B2 31C6 31D7 BATT_CHGND

C626 10PF 5% 50V CERM 603 — C144 47PF 10% 50V CERM 603 — C140 47PF 10% 50V CERM 603 — C625 10PF 5% 50V CERM 603 — C148 1000PF 5% 25V CERM 603 — C623 470PF 10% 50V CERM 603 — C624 10PF 5% 50V CERM 603 — C146 47PF 10% 50V CERM 603 — C629 10PF 5% 50V CERM 603

J16 M-ST TH (OMIT)
BATT_CHGND 7
BATT_POS 1
BATT_IN 2
BATT_CLK 3
BATT_DATA 4
PMU_BATT_DET_L 5
BATT_NEG 6
BATT_CHGND 8

R467 470K 5% 1/16W MF 603 — C136 47PF 10% 50V CERM 603 — C627 10PF 5% 50V CERM 603 — C132 47PF 10% 50V CERM 603 — C628 10PF 5% 50V CERM 603

BATT_CHGND 31C6 31D7 33B2 33C4

C132,C628 STUFF WITH 0 OHM RESISTOR FOR EMC FIX
AND CONSIDER FOR CURRENT LIMIT,CHANGE SIDE TO 0805

L49 100-OHM-EMI SM — 21B2 21B3 SMB_CLK

L48 100-OHM-EMI SM — 21B2 21B3 SMB_SDA

PS_GND

BYPASS_R_DRV

40C4 36D2 33C7 31D2 31C5 21D8 21B7 21B1 21A4 +3_3V_PMU 21D6 21C6 21B8 33A4 32D2 31D3

C475 0.01UF 20% 50V CERM 603

R533 100K 1% 1/16W MF 603 — BATT_OK_REF

39B3 39A6 37D8 37C4 36C6 34D8 34C6 34C3 34A2 33C7 33B7 32C6 32C1 32B8 32B3 31D6 31C4 31C2 28B5 PS_GND 32B1 32A7 32A3 32A2 33B3 33A6 33A4 32D1 34C1 34B4 34B3 37B8 37B1 37A7

Q74 2N7002 SM — BATT_V_GOOD

U10 LMC7211 SM — BATT_OK

R538 93.1K 1% 1/16W MF 603 (OMIT)

40C4 36D2 32D2 31C5 21C6 21B7 21A4 21B1 21B8 21D8 21D6 31D3 31D2 33C7 33B6 — R513 475K 1% 1/16W MF 603 (OMIT) — 21B3 BATT_IN_0_L

R456 470K 5% 1/16W MF 603 — +3_3V_PMU

R454 1K 5% 1/16W MF 603

R518 93.1K 1% 1/16W MF 603 (OMIT) — C1539 0.22UF 20% 25V CERM 805

L44 30-OHM-EMI SM — PS_GND

PS_GND 34C3 34C6 34D8 36C6 37A7 37B1 37B8 37C4 37D8 39A6 39B3 28B5 31C2 31C4 31D6 32A2 32A3 32A7 32B1 32B3 32B8 32C1 32C6 32D1 33A4 33A6 33B3 33B6 33B7 33C7 34A2 34B3 34B4 34C1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
110S4755	1	CHIP RES 1/16W 1% 475K 0603 ACI	R513	3SBAT
110S6655	1	CHIP RES 1/16W 1% 665K 0603 ACI	R513	4SBAT
101S6561	1	CHIP RES 1W 5% 56 2512 ACI	R490	3SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACI	R490	4SBAT
101S6561	1	CHIP RES 1W 5% 56 2512 ACI	R506	3SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACI	R506	4SBAT
101S6102	1	CHIP RES 1W 5% 100 2512 ACI	R483	4SBAT
516-1002	1	CONN FOXCONN BP24067-R1 DIP BATT PLUG ACI	J16	3SBAT
518-0016	1	CONN MOLEX22-05-7065 6P P2.5 TIN DIP	J16	4SBAT
110S9314	2	CHIP RES 1W 1% 93.1K 0603 ACI	R518,R538	3SBAT
110S1005	2	CHIP RES 1W 1% 100K 0603 ACI	R518,R538	4SBAT

BATTERY INTERFACE

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APPLE COMPUTER INC.

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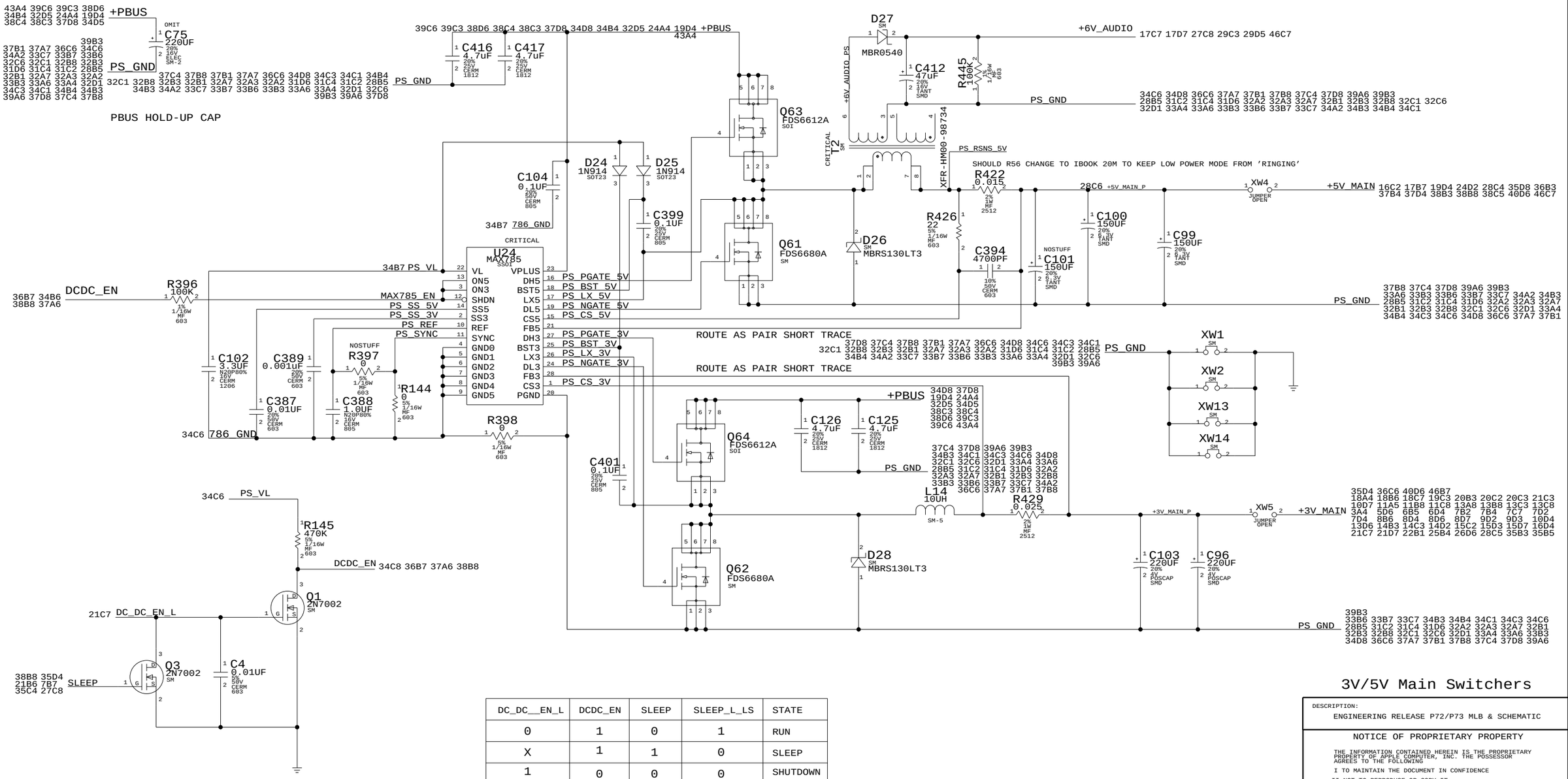
SCALE: NONE	SHT 33 OF 53	

3V/5V Main Switchers

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
126S2228	1	ELEC 220UF/16V 20%	C75	3SBAT
126S1024	1	ELEC 100UF/35V 20%	C75	4SBAT



DC_DC__EN_L	DCDC_EN	SLEEP	SLEEP_L_LS	STATE
0	1	0	1	RUN
X	1	1	0	SLEEP
1	0	0	0	SHUTDOWN

3V/5V Main Switchers

DESCRIPTION:
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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
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SCALE: NONE	SHT 34 OF 53	

LOW CURRENT. CAN WE CHANGE TO CHEAPER FET?

POWER FOR:
TRACKPAD
VGA DDC POWER

38B8 35C4 34A8 27C8 21B6 7B7 SLEEP
8D4 40D6 36C6 35B5 35B3 34B2 28C5 26D6 25B4 22B1 21D7 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4 13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4 16D4 46B7 +3V_MAIN

R62 100K 5% 1/16W MF 603
C59 NOSTUFF 0.01UF 5% 50V CERM 603
C62 2200PF 5% 50V CERM 603
Q14 SI3443DV TSOP
+3V_SLEEP
4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8 20D6 22B5 22C1 25A6 25B5 25D4 27C6 40D4 46B7

38C5 38B8 38B3 37D4 24D2 19D4 17B7 16C2 37B4 36B3 34C2 28C4 46C7 40D6 +5V_MAIN

C456 0.1UF 20% 16V CERM 603
R508 100K 5% 1/16W MF 603
Q70 SI3443DV TSOP
+5V_HD_SLEEP 16A5 16B8 16D7
C457 2200PF 5% 50V CERM 603 NOSTUFF
C452 0.01UF 5% 50V CERM 603
Q66 SI3443DV TSOP
+5V_CD_SLEEP 16A3 16A6 16B2
R504 330K 5% 1/16W MF 603
Q68 SI3443DV TSOP
R299 100K 5% 1/16W MF 603
Q48 SI3443DV TSOP
+5V_IO_SLEEP 21C3 21D2 25D8 28D5 35B2 40C6
C317 NOSTUFF 2200PF 5% 50V CERM 603
28B8 SLEEP_LS
Q47 2N7002 SM
38B8 19D3 18A6 3A4 SLEEP_L_LS

38B8 35D4 34A8 27C8 21B6 7B7 SLEEP
36B5 11D8 10D7 +VIO_CPUBUS_MAIN

C296 0.01UF 5% 50V CERM 603
R281 100K 5% 1/16W MF 603
Q45 SI3447DV TSOP
+VIO_CPU_SLEEP
R598 200 5% 1/16W MF 603
C293 2200PF 5% 50V CERM 603
Q85 2N7002 SM

8D4 25B4 22B1 21D7 21C7 21C3 20C3 20C2 20B3 19C3 18C7 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 13B8 8B6 7D4 7D2 7C7 7B4 7B2 6D4 6B5 5D6 3A4 13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 8D6 46B7 40D6 36C6 35D4 35B3 18B6 18A4 16D4 34B2 28C5 26D6 +3V_MAIN

+3_3V_REF_PMU 21B6 21D3 40C4
R1204 100K 5% 1/16W MF 603
R1206 0 5% 1/16W MF 603
21D3 21B3 TEMP
THERM_OD* 35B4
R1205 NOSTUFF 220K 5% 1/16W MF 603

R1200 10K 5% 1/16W MF 603

13A8 11C8 11B8 11A5 10D7 10D4 9D3 9D2 8D7 15D7 15D3 15C2 14D2 14C3 14B3 13D6 13C8 13C3 21C7 21C3 20C3 20C2 20B3 19C3 18C7 18B6 18A4 36C6 35D4 35B5 35B3 34B2 28C5 26D6 25B4 22B1 46B7

U1200 ADM1030
INT* SCL UNI_IIC_CLK1 10B7 15C8
ADD SDA UNI_IIC_DAT1 10A7 15C8
FAN_FAULT* D+
35A5 THERM_OD* THERM* D- TO_THERMDIODE_2
35B2 TACH_FAN TACH VCC +3V_MAIN
PWM_OUT GND
PLACE ADM1030 CLOSED TO HARD DRIVE

C621 0.1UF 20% 10V CERM 402

PLACE Q1000 CLOSE TO CPU
Q1000 2N3904 SM
+5V_IO_SLEEP
35B4 TACH_FAN
J1 SM-2MT
+3V_MAIN R1201 10K 5% 1/16W MF 603
Q1001 SI2302DS SM

FAN CIRCUIT

POWER SUPPLY LOAD FET SWITCHES

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APPLE COMPUTER INC.

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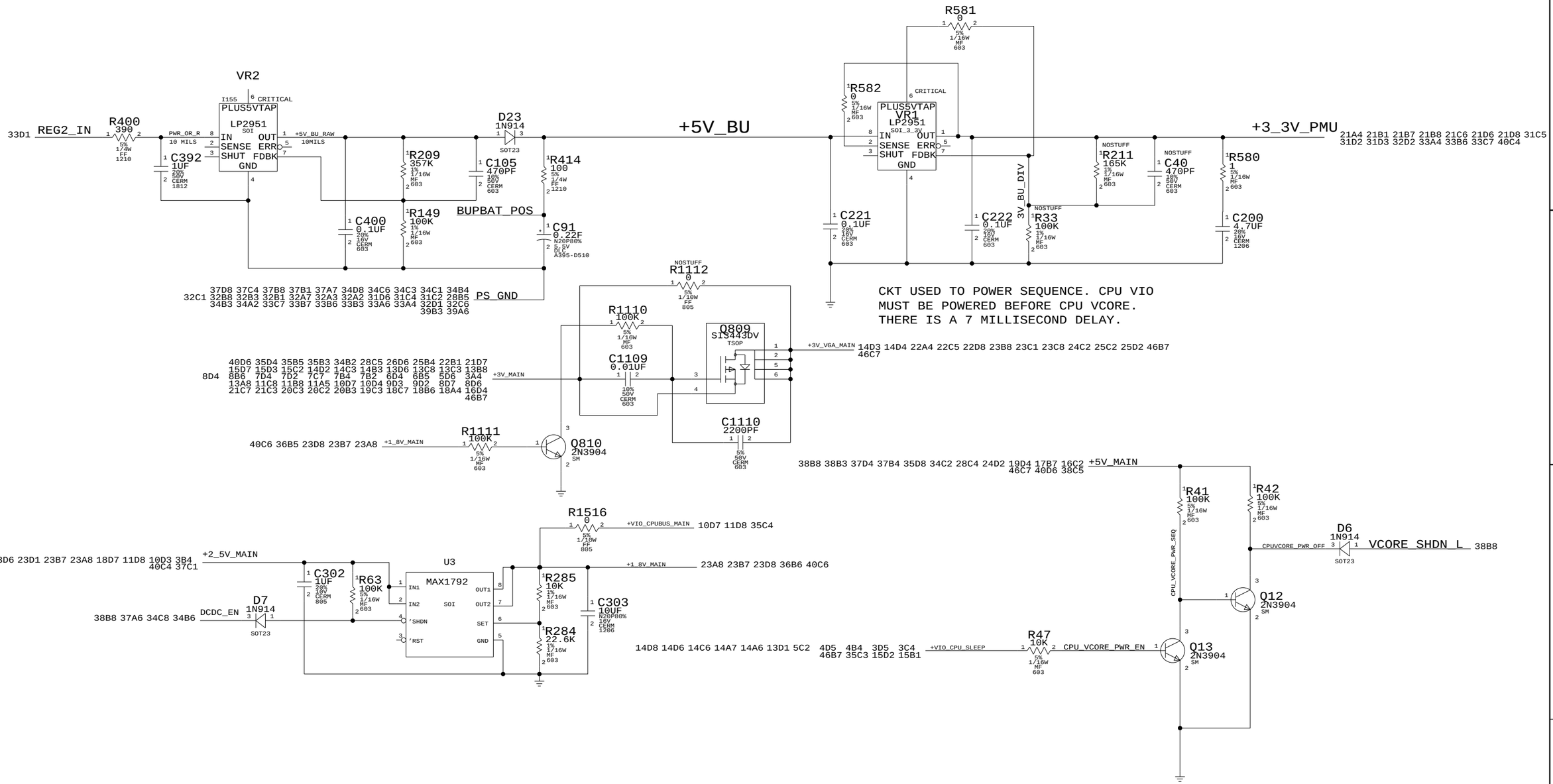
D	051-6130-C	ACI: C ECS:1.B

SCALE	SHT	OF
NONE	35	53



SUPER CAP CIRCUIT

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

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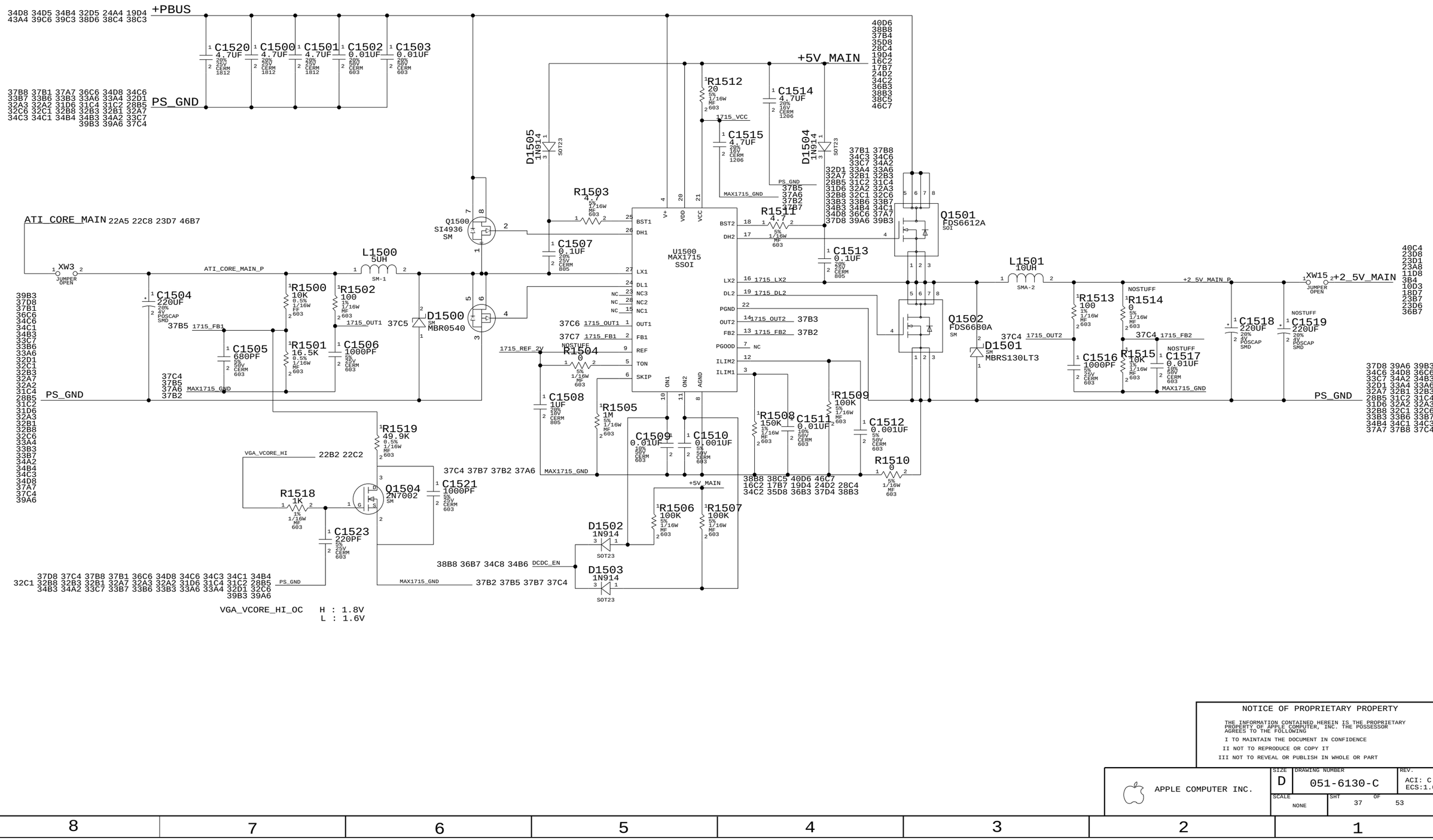
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 36 OF 53	



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APPLE COMPUTER INC.

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SCALE: NONE	SHT 37 OF 53	

CPU_VCORE(1.225/1.5V)

39C6 39C3 38C4 38C3 37D8 34D8 34D5 34B4 32D5 24A4 19D4 43A4 +PBUS

C6 0.01UF 20% 50V CERM 603 NOSTUFF
C31 0.01UF 20% 50V CERM 603 NOSTUFF
C171 4.7uF 20% 25V CERM 1812
C23 4.7uF 20% 25V CERM 1812
C175 4.7uF 20% 25V CERM 1812
C12 4.7uF 20% 25V CERM 1812
GND_VCOREOUTPUT 21A3 21A8 38B2 38B5 38B7 38C1 38C4 38C5 38C8

38C5 38B5 1717_VCC_5V
R1530 1K 5% 1/16W MF 603 NOSTUFF
R1531 100K 5% 1/16W MF 603
R1532 1K 5% 1/16W MF 603 NOSTUFF
R1533 1K 5% 1/16W MF 603
R1534 1K 5% 1/16W MF 603 NOSTUFF
R1535 1K 5% 1/16W MF 603
R1536 1K 5% 1/16W MF 603 NOSTUFF
R1537 1K 5% 1/16W MF 603
R1538 1K 5% 1/16W MF 603 NOSTUFF
R1539 100K 5% 1/16W MF 603
38D3 38C5 38C4 38B2 21A8 21A3 GND_VCOREOUTPUT 38C1 38B7 38B5

1717_VCC_5V 38B5 38D8
C1533 1UF 20% 16V CERM 805
MAX1717_GND 38B6 38B7
R1549 20 5% 1/16W MF 603
C1534 10UF N20P80% 10V CERM 1206
GND_VCOREOUTPUT
+5V MAIN
D1510 1N914 SOT23
R1548 0 5% 1/16W MF 603
C1535 0.1UF 20% 25V CERM 805
Q33 IRF7805 SM

46C7 40D6 38B8 38B3 37D4 37B4 35D8 28C4 19D4 16C2 17B7 24D2 34C2 36B3

SSOI U1 MAX1717
V_PLUS VCC VDD BST DH LX DL GND FBS FB A/B ILIM VGATE GNDS NC
D4 D3 D2 D1 D0 TON REF CC TIME SKP/SDN

38B6 38B5 1717_REF_2V
R1540 0 5% 1/16W MF 603 NOSTUFF
C1532 1UF 20% 16V CERM 805
C1531 470PF 10% 50V CERM 603
R1541 120K 5% 1/16W MF 603
MAX1717_GND
R1542 162K 1% 1/16W MF 603
1717_REF_2V
R1547 0 5% 1/16W MF 603
1717_VCC_5V
R1543 1.62K 1% 1/16W MF 603 NOSTUFF
R1544 115K 1% 1/16W MF 603
R1546 15K 1% 1/16W MF 603 NOSTUFF
1717_REF_2V
R1545 0 5% 1/16W MF 603
GND_VCOREOUTPUT
R1560 0 5% 1/16W MF 603

L1 2.0UH SM
NOSTUFF R1551 2.2 5% 1/4W FF 1210
D12 SM MBRS130LT3
Q32 FDS6672 SM
NOSTUFF C1538 4700PF 10% 50V CERM 603
NOSTUFF C1537 0.0022UF 10% 50V CERM 603
R1555 0 5% 1/16W MF 603 NOSTUFF
R1550 100 1% 1/16W MF 603
C1536 1000PF 5% 25V CERM 603
R1556 0 5% 1/16W MF 603
+VCORE_SLEEP 3D4 38C1 40C6 46B7

39C6 43A4
+PBUS 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C4 38D6 39C3 39C6 43A4
OMIT C1 220UF 20% 16V ELEC SM-2
4SBAT C620 100UF 20% 35V ELEC SM-1
GND_VCOREOUTPUT 38C1 38C5 38C8 21A3 21A8 38B2 38B5 38B7
PBUS HOLD-UP CAP 38D3

XW9 SM
XW7 SM
GND_VCOREOUTPUT 21A3 21A8 38B2 38B5 38B7 38C4 38C5 38C8 38D3
FAT SHORT FAT SHORT
XW8 JUMPER OPEN
+VCORE_SLEEP 3D4 38B3 40C6 46B7
NOSTUFF R28 0.200 5% 1/2W MF 1210
VCORE_DISCHRG
C179 330UF 20% 2.5V POSCAP SMD
C189 330UF 20% 2.5V POSCAP SMD
C185 330UF 20% 2.5V POSCAP SMD
C173 330UF 20% 2.5V POSCAP SMD
C169 330UF 20% 2.5V POSCAP SMD
SHORT FAT SHORT FAT GND_VCOREOUTPUT

46C7 40D6 38C5 38B3 28C4 24D2 19D4 17B7 16C2 +5V MAIN 37D4 37B4 36B3 35D8 34C2
R5 470K 5% 1/16W MF 603
R6 100K 5% 1/16W MF 603
38C5 38B6 MAX1717_GND
D1 1N914 SOT23
38B5 38C7
35B8 19D3 18A6 3A4 SLEEP_L_LS
Q5 2N7002 SM
C172 0.01UF 5% 50V CERM 603
C1530 0.01UF 10% 50V CERM 603
35C4 34A8 27C8 21B6 7B7 35D4 SLEEP
38C8 38C5 38C4 38C1 38B5 38B2 21A8 21A3 38D3 GND_VCOREOUTPUT
MAX1717_GND
37A6 36B7 34C8 34B6 DCDC_EN
D2 1N914 SOT23
36B1 VCORE_SHDN_L

38B2 21A3 21A8 38B7 38C1 38C4 38C5 38C8 38D3
R1552 0 5% 1/16W MF 603 CPU_VCORE_HI_OC 4A4 4B6 6B8 6C5 21D3 38A4
R1553 0 5% 1/16W MF 603 VCORE_CTL 13D7 14D3

38B8 37D4 37B4 36B3 35D8 34C2 28C4 24D2 19D4 17B7 16C2 +5V MAIN 46C7 40D6 38C5
NOSTUFF R15 10K 5% 1/16W MF 603
TP0610T SOT23
NOSTUFF
38B4 21D3 6C5 6B8 4B6 4A4 CPU_VCORE_HI_OC
NOSTUFF C177 4700PF 10% 50V CERM 603

CPU_VCORE_DISCHRG 4
NOSTUFF C20 4700PF 10% 50V CERM 603
NOSTUFF R11 10K 5% 1/16W MF 603
NOSTUFF Q8 FDS6612A SOI

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
126S2226	1	ELEC 220UF/16V 20%	C1	3SBAT
126S2215	1	ELEC 22UF/35V 20% CV-BD	C1	4SBAT

NOTE: SINCE ALL POWER SUPPLIES RESIDE ON THE SYSTEM BOARD JUMPERS HAVE BEEN INCORPORATED TO ALLOW ISOLATION OF THESE CIRCUITS FOR LOAD TESTING W/O THE RISK OF DAMAGE TO THE REST OF THE SYSTEM

CPU_VCORE(1.2/1.4V) & 2.5V SWITCHERS

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APPLE COMPUTER INC.

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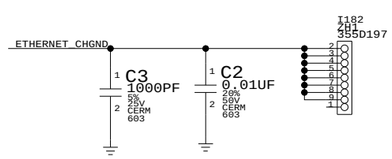
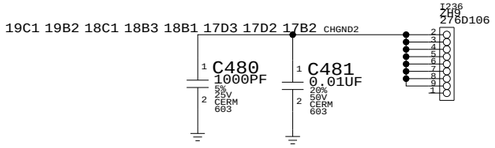
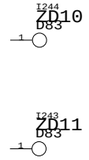
D	051-6130-C	ACI: C ECS:1.B
SCALE: NONE	SHT 38 OF 53	

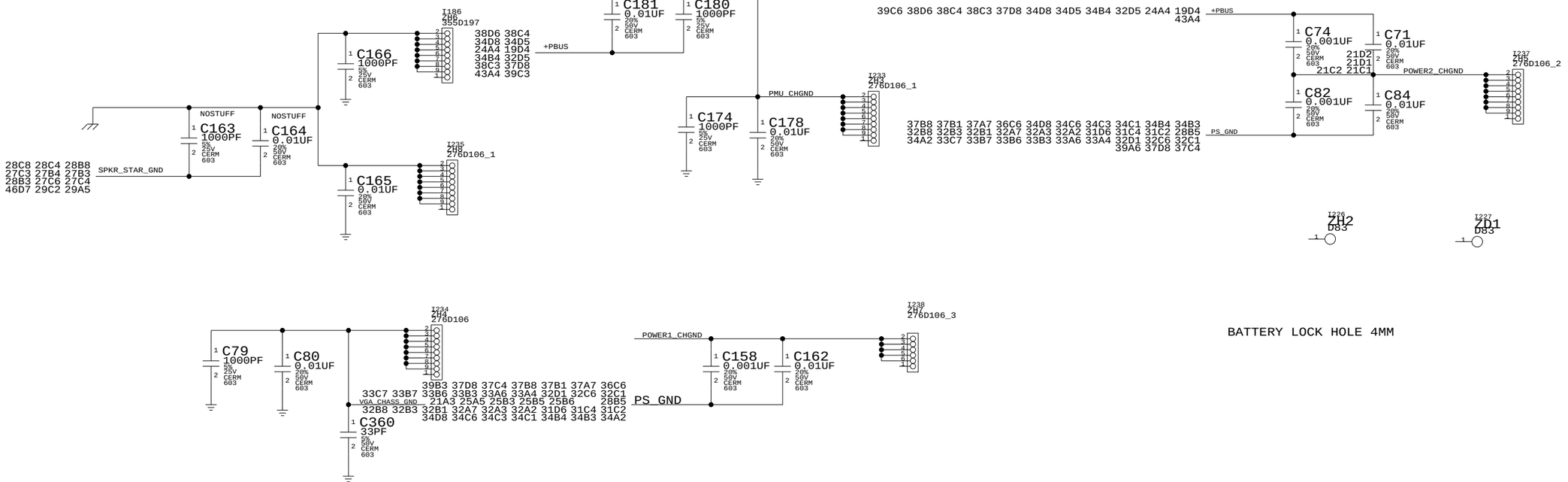






FOR CPU THERMAL MODULE

FOR EMC SMD FINGER



BATTERY LOCK HOLE 4MM

TOOLING HOLES

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 39 OF 53	

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	
+5V_MAIN		5	OUT 38B3 38B8 38C5 46C7
+3V_MAIN		3.3	OUT 16C2 17B7 19D4 24D2 28C4
			OUT 34C2 35D8 36B3 37B4 37D4
		0	OUT
		0	OUT
+2_5V_SLEEP	10	2.5	OUT
+VCORE_SLEEP	10	1.8	OUT 3D4 38B3 38C1 46B7
+3V_AVDD5_PANGEA_MAIN	10	3.3	OUT 5D6
+3V_AVDD4_PANGEA_MAIN	10	3.3	OUT 6D3
+3V_AVDD6_PANGEA_MAIN	10	3.3	OUT 9D2
AGPVREF	10		OUT 9D4
+3V_AMVDD_PANGEA_MAIN	10	3.3	OUT 10C7 11A8
PANGEA_TEI		0	OUT 10B7
ETH_RXD_PD		0	OUT 10B7 10D2
GBE_REFCLK		0	OUT 10B7 10D2
+3V_PHY_AVDD_MAIN		3.3	OUT 19B5 19B7 19D6 40C6
+VP_CPS			OUT 19C7
+3V_FW_MAIN		3.3	OUT 19B3 19B5 19B7 19C6
+3V_PHY_AVDD_MAIN		3.3	OUT 19B5 19B7 19D6 40C6
+PBUS_FW_SW			OUT 19C8 19D3
+FW_VP_FUSE_SW			OUT 19D2
+VP_SW			OUT 19D2
+VP_CONN_SW			OUT 19D2
GNDRET_FW			OUT 19C1 19C2
+5V_IO_SLEEP	20		OUT 21C3 21D2 25D8 28D5 35B2
+5V_VGA_FUSE	20		35B5 OUT 25D6 46C7
+1_8V_MAIN	10	1.8	OUT 23A8 23B7 23D8 36B5 36B6
+1_8V_1644_LX	10		OUT
+1_8V_1644_FB	10		OUT

SIG_NAME	MIN_LINE_WIDTH	VOLTAGE	
+3V_SLEEP	25	3.3	OUT 4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8 20D6 22B5 22C1 25A6 25B5 25D4 27C6 35D2 46B7
+3V_VDDA3_PANGEA_MAIN	10	3.3	OUT 13D6 40D4
+3V_VDDA3_PANGEA_MAIN	10	3.3	OUT 13D6 40D4
+3V_VDDA3_PANGEA_MAIN	10	3.3	OUT 13D6 40D4
VDD_USB	10	3.3	OUT 13C5
USB_PWR_A		3.3	OUT 13C5 17A7
USB_PWR_B		3.3	OUT 13C5 17A7
USB_PWR_FLT_AB		5	OUT
USB_PWR_FLT_CD		5	OUT
+3_3V_PMU	10	3.3	OUT 21A4 21B1 21B7 21B8 21C6 21D6 21D8 31C5 31D2 31D3 32D2
+3_3V_REF_PMU	10	3.3	OUT 21B6 21D3 35A5 33A4 33B6 33C7 36D2
+2_5V_ATILPVDD_MAIN	10	2.5	OUT
+2_5V_F_A2VDDATI_MAIN	10	2.5	OUT
+2_5V_MAIN	10	2.5	OUT 3B4 10D3 11D8 18D7 23A8 23B7 23D1 23D6 23D8 36B7 37C1
+3V_AGPVDD_MAIN	10	3.3	OUT 9D3
+3V_VDDA1_PANGEA_MAIN	10	3.3	OUT 13D6
+3V_VDDA2_PANGEA_MAIN	10	3.3	OUT 13D6
MOBM3G1	10	0	OUT
MOBM3G2	10	0	OUT
MOBM3G3	10	0	OUT
MOBM3V1	10	2.5	OUT
MOBM3V2	10	2.5	OUT
MOBM3V3	10	2.5	OUT
TXVSSR1	10	0	OUT
PANGEA_ACS_REF	10	0	OUT 5A7
PANGEA_SD_REF	10	0	OUT 6B2
VREF_VDDQ	10	3.3	OUT

XWS	SHORT	OPEN
XW1	X	
XW2	X	
XW3	X	
XW4	X	
XW5	X	
XW6	X	
XW7	X	
XW8	X	
XW9	X	
XW10	X	
XW11	X	
XW12	X	
XW13	X	
XW14	X	

I/O CONNECTORS

USB	SHEET 17	J7,J10
ETHERNET	SHEET 18	J3
FIREWIRE	SHEET 19	J5
RGB	SHEET 24	J12
HEADPHONE	SHEET 27	J13
DC IN	SHEET 32	J20

Holes and Slots AND EMC INFO

CONSTRAINTS -- POWER

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0

SCALE NONE | SHT 40 OF 53

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH/ ECL		NET_SPACING_TYPE	
CPU_DATA<0>	100	5	U2.E2 U1.AJ15	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<1>	100	5	U2.D2 U1.AK6	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<2>	100	5	U2.C1 U1.AJ9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<3>	100	5	U2.A3 U1.AK14	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<4>	100	5	U2.B4 U1.AM6	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<5>	100	5	U2.D6 U1.AH12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<6>	100	5	U2.B5 U1.AM11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<7>	100	5	U2.C6 U1.AN18	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<8>	100	5	U2.B6 U1.AM18	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<9>	100	5	U2.A5 U1.AJ16	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<10>	100	5	U2.C7 U1.AK8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<11>	100	5	U2.A6 U1.AH16	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<12>	100	5	U2.B7 U1.AH8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5D3 5D4
CPU_DATA<13>	100	5	U2.A7 U1.AM14	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<14>	100	5	U2.C8 U1.AP3	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<15>	100	5	U2.A8 U1.AJ10	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<16>	100	5	U2.A9 U1.AN4	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<17>	100	5	U2.C9 U1.AJ12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<18>	100	5	U2.B9 U1.AM9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 5C4 5D3
CPU_DATA<19>	100	5	U2.A10 U1.AN13	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<20>	100	5	U2.A11 U1.AK12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<21>	100	5	U2.B12 U1.AK15	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<22>	100	5	U2.C12 U1.AM12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<23>	100	5	U2.A12 U1.AP4	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<24>	100	5	U2.A13 U1.AH13	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<25>	100	5	U2.C13 U1.AP5	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<26>	100	5	U2.A14 U1.AH15	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<27>	100	5	U2.B14 U1.AN5	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<28>	100	5	U2.A15 U1.AN6	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<29>	100	5	U2.C14 U1.AP6	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<30>	100	5	U2.A16 U1.AJ13	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<31>	100	5	U2.B15 U1.AM15	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3A8 3B6 3B8 5C4 5D3
CPU_DATA<32>	100	5	U2.W15 U1.AJ17	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4
CPU_DATA<33>	100	5	U2.Y16 U1.AN12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4 5D3
CPU_DATA<34>	100	5	U2.V14 U1.AN19	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4 5D3
CPU_DATA<35>	100	5	U2.Y15 U1.AN17	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4 5D3
CPU_DATA<36>	100	5	U2.W14 U1.AN11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4 5D3
CPU_DATA<37>	100	5	U2.Y14 U1.AH17	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B8 3C7 5C4 5D3
CPU_DATA<38>	100	5	U2.V13 U1.AN10	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5C4 5D3
CPU_DATA<39>	100	5	U2.Y13 U1.AK17	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<40>	100	5	U2.Y12 U1.AN9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<41>	100	5	U2.V12 U1.AP19	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<42>	100	5	U2.W12 U1.AM17	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<43>	100	5	U2.Y11 U1.AM8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<44>	100	5	U2.Y10 U1.AJ11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<45>	100	5	U2.W9 U1.AK18	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<46>	100	5	U2.V9 U1.AH14	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<47>	100	5	U2.Y9 U1.AM5	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<48>	100	5	U2.Y8 U1.AH11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<49>	100	5	U2.V8 U1.AK9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<50>	100	5	U2.Y7 U1.AJ8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<51>	100	5	U2.W7 U1.AJ14	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<52>	100	5	U2.Y6 U1.AK11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<53>	100	5	U2.V7 U1.AH9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<54>	100	5	U2.Y5 U1.AH10	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<55>	100	5	U2.W6 U1.AP10	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<56>	100	5	U2.V6 U1.AP12	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<57>	100	5	U2.W5 U1.AP8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<58>	100	5	U2.U6 U1.AP9	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<59>	100	5	U2.W4 U1.AP13	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<60>	100	5	U2.Y3 U1.AP11	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<61>	100	5	U2.V1 U1.AN7	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<62>	100	5	U2.U2 U1.AN8	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B4 5D3
CPU_DATA<63>	100	5	U2.T1 R9.2 R10.1 U1.AP7	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3B6 3B7 3B8 5B3 5B4 5D3

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	NET_SCHED	DELAY_RULE	STUB_LENGTH/ ECL		NET_SPACING_TYPE	
KEY PANGEA TIMING CPU_BR*	100	5	U2.N1 RP26.4 U1.AP16			TRUE	5 MIL SPACING	OUT 3D8 5D7 14C8
KEY PANGEA TIMING TS*	100	5	U2.J19 R774.1 U1.AN14	::2300:4400		TRUE	5 MIL SPACING	OUT 3D8 5D7 14C8
TBST*	100	5		::2300:4400		TRUE	5 MIL SPACING	OUT 3C8 5B7 14C8
AACK*	100	5	U2.N18 U1.AN20	::2300:4400	200	TRUE	5 MIL SPACING	OUT 3B8 5B7 14B6
KEY PANGEA TIMING ARTRY*	100	5	U2.M3 R350.1 U1.AP14		200	TRUE	5 MIL SPACING	OUT 3B8 5B7 14A8
DBWO*	100	5		::2300:4400	200	TRUE	5 MIL SPACING	OUT 3B8 5A4 14D6
KEY PANGEA TIMING QREQ*	100	5	U2.L1 R353.1 U1.AN15	:::2900	200	TRUE	5 MIL SPACING	OUT 3A6 5B7 14C8
QACK*	100	5	U2.K2 R174.1	::2300:3500	200	TRUE	5 MIL SPACING	OUT 3A3 3A6
PAN_QACK*	100	4		::450:650	200	TRUE	5 MIL SPACING	OUT 3A4 5B7 14B6
TA*	100	5	U2.M20 RP24.1 U1.AJ24	::2100:4200	200	TRUE	5 MIL SPACING	OUT 3A6 5A4 14C8
TEA*	100	5	U2.M2 RP26.2 U1.AP20		200	TRUE	5 MIL SPACING	OUT 3A6 5A4 14B8
TT<0>	100	5		::2500:3500		TRUE	5 MIL SPACING	OUT 3C8 5B7
TT<1>	100	5		::2500:3500		TRUE	5 MIL SPACING	OUT 3C8 5B7
TT<2>	100	5		::2500:3500		TRUE	5 MIL SPACING	OUT 3C8 5B7
TT<3>	100	5		::2500:3500		TRUE	5 MIL SPACING	OUT 3C8 5B7
TT<4>	100	5	U2.K20 RP24.4 U1.AH26	::2500:3500		TRUE	5 MIL SPACING	OUT 3C8 5B7
TSIZ<0>	100	5	U2.L20 U1.AP30	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 5B7
TSIZ<1>	100	5	U2.M19 U1.AN29	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 5B7
TSIZ<2>	100	5	U2.M18 U1.AH25	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 5B7
CPU_ADDR<0>	100	5	U2.C15 U1.AK23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<1>	100	5	U2.B16 U1.AP27	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<2>	100	5	U2.D15 U1.AP28	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<3>	100	5	U2.B17 U1.AN26	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<4>	100	5	U2.A18 U1.AK24	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<5>	100	5	U2.C20 U1.AN24	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5D7
CPU_ADDR<6>	100	5	U2.D19 U1.AM26	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<7>	100	5	U2.F17 U1.AJ23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<8>	100	5	U2.E19 U1.AM24	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<9>	100	5	U2.F18 U1.AH23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<10>	100	5	U2.F19 U1.AM23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<11>	100	5	U2.E20 U1.AN23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<12>	100	5	U2.G18 U1.AJ22	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<13>	100	5	U2.F20 U1.AN22	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<14>	100	5	U2.G19 U1.AP26	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<15>	100	5	U2.G20 U1.AP21	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<16>	100	5	U2.P20 U1.AH22	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<17>	100	5	U2.P19 U1.AM21	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3D8 5C7 5D7
CPU_ADDR<18>	100	5	U2.R20 U1.AJ21	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<19>	100	5	U2.P18 U1.AK20	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<20>	100	5	U2.T20 U1.AK21	::2500:3500	220	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<21>	100	5	U2.R19 U1.AN25	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<22>	100	5	U2.R18 U1.AP24	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<23>	100	5	U2.T19 U1.AP25	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<24>	100	5	U2.R17 U1.AH20	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<25>	100	5	U2.U19 U1.AH21	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<26>	100	5	U2.V20 U1.AP23	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<27>	100	5	U2.Y18 U1.AM20	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<28>	100	5	U2.W17 U1.AJ20	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<29>	100	5	U2.U15 U1.AN21	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<30>	100	5	U2.W16 U1.AJ19	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
CPU_ADDR<31>	100	5	U2.V15 U1.AP22	::2500:3500	200	TRUE	5 MIL SPACING	OUT 3C8 3D8 5C7 5D7
GBL*	100	5	U2.R2 RP24.3 U1.AP29	::2300:4400		TRUE	5 MIL SPACING	OUT 3C8 5B7 14C8
CPU_DBG*	100	5				TRUE	5 MIL SPACING	OUT 3B8 5A4 14A8
CPU_BG*	100	5	U2.P1 U1.AH19	::2300:4400	200	TRUE	5 MIL SPACING	OUT 3D8 5D7 14C6
WT*	100	5	U2.R1 U1.AK26	::2300:4400	200	TRUE	5 MIL SPACING	OUT 3B8 5B7 14B6
CI*	100	5	U2.T2 U1.AJ25	::2300:4400	210	TRUE	5 MIL SPACING	OUT 3B8 5B7 14B6

CONSTRAINTS -- CPU BUS

CONSTRAINTS -- CPU BUS

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 41 OF 53	

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH	ECL	NET_SPACING_TYPE	NET_SCHED
MDATA<0>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AG1 J1.3 U23.2
MDATA<1>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AF3 J1.5 U23.4
MDATA<2>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AF1 J1.7 U23.5
MDATA<3>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AE2 J1.9 U23.7
MDATA<4>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AE1 J1.13 U23.8
MDATA<5>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AD2 J1.15 U23.10
MDATA<6>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AD1 J1.17 U23.11
MDATA<7>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC2 J1.19 U23.13
MDATA<8>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.Y1 J1.37 U23.42
MDATA<9>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.Y2 J1.39 U23.44
MDATA<10>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.W1 J1.41 U23.45
MDATA<11>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.W2 J1.43 U23.47
MDATA<12>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.V2 J1.47 U23.48
MDATA<13>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.U2 J1.49 U23.50
MDATA<14>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.T1 J1.51 U23.51
MDATA<15>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.T2 J1.53
MDATA<16>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.R1 J1.83 U24.2
MDATA<17>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.R2 J1.85 U24.4
MDATA<18>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.P3 J1.87 U24.5
MDATA<19>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.P2 J1.89 U24.7
MDATA<20>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.N1 J1.93 U24.8
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MDATA<22>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.M1 J1.97 U24.11
MDATA<23>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.M2 J1.99 U24.13
MDATA<24>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.J2 J1.121 U24.42
MDATA<25>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.H2 J1.123 U24.44
MDATA<26>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.G1 J1.125 U24.45
MDATA<27>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.G2 J1.127 U24.47
MDATA<28>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.F1 J1.131 U24.48
MDATA<29>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.F2 J1.133 U24.50
MDATA<30>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.E1 J1.135 U24.51
MDATA<31>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.H3 J1.137 U24.53
MDATA<32>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AD3 J1.4 U22.2
MDATA<33>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AD5 J1.6 U22.4
MDATA<34>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC3 J1.8 U22.5
MDATA<35>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC5 J1.10 U22.7
MDATA<36>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC6 J1.14 U22.8
MDATA<37>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC7 J1.16 U22.10
MDATA<38>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AB6 J1.18 U22.11
MDATA<39>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AB7 J1.20 U22.13
MDATA<40>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AA5 J1.38 U22.42
MDATA<41>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AA6 J1.40 U22.44
MDATA<42>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AA7 J1.42 U22.45
MDATA<43>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.AC1 J1.44 U22.47
MDATA<44>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.V3 J1.48 U22.48
MDATA<45>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.V5 J1.50 U22.50
MDATA<46>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.V6 J1.52 U22.51
MDATA<47>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.W7 J1.54 U22.53
MDATA<48>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.U3 J1.84 U25.2
MDATA<49>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.U5 J1.86 U25.4
MDATA<50>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.U6 J1.88 U25.5
MDATA<51>	100	6	::1930:4400		TRUE	5 MIL SPACING	U1.U7 J1.90 U25.7
MDATA<52>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.R6 J1.94 U25.8
MDATA<53>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.R7 J1.96 U25.10
MDATA<54>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.P5 J1.98 U25.11
MDATA<55>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.P6 J1.100 U25.13
MDATA<56>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.L6 J1.122 U25.42
MDATA<57>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.L7 J1.124 U25.44
MDATA<58>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.K6 J1.126 U25.45
MDATA<59>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.K7 J1.128 U25.47
MDATA<60>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.J3 J1.132 U25.48
MDATA<61>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.J5 J1.134 U25.50
MDATA<62>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.J6 J1.136 U25.51
MDATA<63>	100	6	::1930:4400	200	TRUE	5 MIL SPACING	U1.J7 J1.138 U25.53

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH	ECL	NET_SPACING_TYPE
PANGEAMCLK<0>	100	3	6		::300:500	250	100	TRUE	
PANGEAMCLK<1>	100	3	6		::300:500	250	100	TRUE	
PANGEAMCLK<2>	100	3	6		::300:500	250	100	TRUE	
PANGEAMCLK<3>	100	3	6		::300:500	250	100	TRUE	
MCLK<0>	100	4	6		::1100:3500	250	100	TRUE	
MCLK<1>	100	4	6		::1100:3500	250	100	TRUE	
MCLK<3>	100	4	6		::1100:3500	250	100	TRUE	
M_ADDR<0>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<1>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<2>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<3>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<4>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<5>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<6>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<7>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<8>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<9>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<10>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<11>	100	4			::400:1200		200	TRUE	5 MIL SPACING
M_ADDR<12>	100	4			::400:1200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<0>	100	8		RP23.2 J1.29	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<1>	100	8		RP14.4 J1.31	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<2>	100	8		RP15.1 J1.33	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<3>	100	8		RP14.3 J1.30	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<4>	100	8		RP15.2 J1.32	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<5>	100	8		RP14.1 J1.34	::1100:3300		200	TRUE	5 MIL SPACING
TERM_M_ADDR<6>	100	8		RP21.1 J1.103	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<7>	100	8		RP2.2 J1.104	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<8>	100	8		RP21.2 J1.105	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<9>	100	8		RP21.3 J1.109	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<10>	100	8		RP21.4 J1.111	::1050:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<11>	100	8		RP2.3 J1.112	::1100:3200		200	TRUE	5 MIL SPACING
TERM_M_ADDR<12>	100	8		R208.2 J1.70			200	TRUE	5 MIL SPACING

8D5 7C3 OUT 6D3 8D5 6D4 7C3 OUT 7D5 6D3 6D4 7D5 OUT 8D5 7D5 6D3 6D4 7C3 7D5 8D5 OUT 7C3 6D3 6D4 OUT 8D5 6D3 6D4 7C3 7D5 8D5 OUT 7C3 6D3 6D47C3 OUT 7D5 6D3 6D4 OUT 7D5 8C5 7C3 7D5 8C5 OUT 8C5 6D3 7D5 6D4 OUT 7C3 6D4 7C3 7D5 8C5 OUT 6D4 6C3 8C5 OUT 7D5 6C3 6D4 7C3 7D5 8C5 OUT 7C3 6C3 6D4 OUT 8B5 6C3 6D4 7C3 7D5 8C5 OUT 7D1 6C3 6D47D1 7D5 8B5 OUT 7D5 6C3 6D4 OUT 8B5 7D5 OUT 8B57C1 7D56C3 7C16D4 OUT 6C38B5 6D47C1 8B56C3 7C16D4 OUT 6C37D5 6D4 7D5 8B5 7C1 OUT 8A56C3 7C16D4 OUT 6C37D5 6D48A5 7D57D5 8A57C1 7D56C3 7C16D4 OUT 6C38A5 6D47C1 8A56C3 7C16D4 OUT 6C37D5 6D4 7D5 8D4 7D5 OUT 8D47A3 7D56D4 7A36C3 6D48D4 OUT 6C37D5 7D56C3 7A36D4 OUT 6C38D4 6D47A3 8D46B3 7A36D4 OUT 6B37D5 6D4 7D5 OUT 8C4 7D57A3 7A36B3 6D46D4 OUT 6B37D5 8C4 8C4 OUT 7D56B3 6D4 7A3 7D5 8C4 7A3 6B3 6D4 OUT 8C46B3 6D4 7A3 7D5 8C4 7A3 6B3 6D4 OUT 7D56B3 6D4 7B1 7D5 8B4 OUT 8B4 7D56B3 6D4 7B1 7D5 8B4 7B1 6B3 6D4 6B3 OUT 6D4 7B1 7D5 8B4 OUT 6B3 6D4 7B1 7D5 8B4 OUT 6B3 6D4 7B1 7D5 8B4 OUT 6B3 6D4 7B1 7D5 8B4 OUT 6B3 6D4 7B1 7D5 8B4 OUT 6B3 6D4 7B1 7D5 8A4 OUT 6B3 6D4 7A1 7D5 8A4 OUT 6B3 6D4 7A1 7D5 8A4 OUT 6B3 6D4 7A1 7D5 8A4 OUT 6B3 6D4 7A1 7D5 8A4

OUT 6B2
OUT 6B2
OUT 6B2
OUT 6B2
7C4 OUT 6D6 7A2 7A4 7C2
OUT 6D6 8B4
OUT 6C5 8C5
OUT
OUT
OUT 6B8 6D1 6D2
OUT 6B8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6B8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6B8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6A8 6D1 6D2
OUT 6A8 6C2 6D1 7D4 7C4 7B4 6B7 7B4 7D2 7B2 6A7 7A4 7C4 7D5
OUT 8C5 7D5 7D2 7D5 6A7 7B2 7B4 7C4 8C5
OUT 7D5 8C4 7C4 7D2 6B7 7A4 8B4 7B2 7C4 7D5 7B2 7C2 6A7 7A4 7C4 7D5 6A7 7A4 7B2 7C2 8B5 7C4 7D5 6A7 7A4 7B2 7C2 8B56A7 7B27A4 6A77B2 7A47C2 7C27C4 7C47D5 7D58B4 8C4

CONSTRAINTS -- MEMORY PAGE 1

CONSTRAINTS -- MEMORY PAGE (1)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 42 OF 53	

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	DELAY_RULE	STUB_LENGTH/	ECL	NET_SPACING_TYPE	NET_SCHED	
T_M_BA0	100	5	::1100:2400	200	TRUE	5 MIL SPACING	RP2.1 J1.106	OUT 6A6 7A4 7B2 7C2 7C4 8B4
T_M_BA1	100	5	::1100:2400	200	TRUE	5 MIL SPACING	RP2.4 J1.110	OUT 6A6 7A2 7A4 7C2 7C4 8B4
T_SDRAS*	100	5			TRUE	5 MIL SPACING	RP15.4 J1.65	OUT 6A6 7A2 7A4 7C2 7C4 8C5
T_SDCAS*	100	5	::1100:2400	200	TRUE	5 MIL SPACING	RP15.3 J1.66	OUT 6A6 7A2 7A4 7C2 7C4 8C4
T_MEMWE*	100	5	::1100:2400	200	TRUE	5 MIL SPACING	R202.1 J1.67	OUT 6A6 7A2 7A4 7C2 7C4 8C5

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	MIN_LINE_WIDTH	NET_SCHED	DELAY_RULE	MAX_EXPOSED_LENGTH	STUB_LENGTH/	ECL	NET_SPACING_TYPE	
PANGEA_CPU_CLK	100	2	5		::300:500	250	100	TRUE		OUT 5A7 6C6
CPU_CLK	100	6	5		::2700:5500	250	200	TRUE		OUT 3A4 3A8
CPUFBOUT	100	2	5		::100:600		100	TRUE	10 MIL SPACING	OUT
TCPUFBOUT	100	2	5		::475:700		100	TRUE	10 MIL SPACING	OUT 5B1 6C5
CPUFB7	100	2	5		::900:1000		100	TRUE	10 MIL SPACING	OUT 5B2
CPUFB6	100	2	5		::1800:2000		100	TRUE	10 MIL SPACING	OUT 5B2
CPUFB5	100	2	5		::1800:2000		100	TRUE	10 MIL SPACING	OUT 5B3
CPUFB4	100	2	5		::950:1100		100	TRUE	10 MIL SPACING	OUT 5B3
CPUFB3	100	2	5		::1800:2000		100	TRUE	10 MIL SPACING	OUT 5B3
CPUFB2	100	2	5		::1800:2000		100	TRUE	10 MIL SPACING	OUT 5B2
CPUFB1	100	2	5		::900:1000		100	TRUE	10 MIL SPACING	OUT 5B2
CPUFBIN	100	6	5		::475:1200		100	TRUE	10 MIL SPACING	OUT 5B1 5B8
AGPFB0	66	2	5		::950:1000		100	TRUE	10 MIL SPACING	OUT 9B3
AGPFB1	66	2	5		::475:700		100	TRUE	10 MIL SPACING	OUT 9B4
AGPFB2	66	2	5		::950:1100		100	TRUE	10 MIL SPACING	OUT 9B4
AGPFB3	66	2	5		::475:700		100	TRUE	10 MIL SPACING	OUT 9C4
FBOUT_CLK	100	2	10						10 MIL SPACING	OUT 5A8 6D8
28507_CLK1	100	2	10						10 MIL SPACING	OUT 6C7
28507_CLK2	100	2	10						10 MIL SPACING	OUT 6C7
28507_CLK3	100	2	10						10 MIL SPACING	OUT 6D7
28507_CLK4	100	2	10						10 MIL SPACING	OUT 6D7
28507_CLK5	100	2	10						10 MIL SPACING	OUT 6D7
MK1708_SSOUT		2	5						10 MIL SPACING	OUT 22A3
ATI_SSIN		2	5						10 MIL SPACING	OUT 22A2 22B3
TBENDIVCLK	100	2	5						10 MIL SPACING	OUT 6B8 6C6
TBEN	33	2	4						10 MIL SPACING	OUT 3A6 6B6 14B8
574_CLK	100	2	10						10 MIL SPACING	OUT 6C6 7B8

SIG_NAME	PULSE_PARAM	MAX_VIA_COUNT	ASSIGN_TOPOLOGY	NET_SCHED	DELAY_RULE	STUB_LENGTH/	ECL	NET_SPACING_TYPE	
DQM0*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7C4 8C5
DQM1*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7C4 8C5
DQM2*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7C2 8B5
DQM3*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7C2 8B5
DQM4*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7A4 8C4
DQM5*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7A4 8C4
DQM6*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7A2 8B4
DQM7*	100	4			::3000:4000	200	TRUE	5 MIL SPACING	OUT 6C2 7A2 8B4
CS0*	100	5		U1.M3 RP8.7	::600:1100	200	TRUE	5 MIL SPACING	OUT 6A4 6C2
CS1*	100	5		U1.M5 RP8.8	::600:1100	200	TRUE	5 MIL SPACING	OUT 6A4 6C2
CS2*	100	5		U1.R3 RP8.5	::600:1100	200	TRUE	5 MIL SPACING	OUT 6A4 6C2
CS3*	100	5		U1.P7 RP8.6	::600:1100	200	TRUE	5 MIL SPACING	OUT 6A4 6C2 7C4
T1CS0*	100	4			::300:1400	200	TRUE	5 MIL SPACING	OUT 6A5 7A2
T1CS1*	100	4			::300:1400	200	TRUE	5 MIL SPACING	OUT 7A4 7C2 6A5
RAM_CKE0	100	4			::300:1400	200	TRUE	5 MIL SPACING	OUT 6C2 7B8
RAM_CKE1	100	4			::300:1400	200	TRUE	5 MIL SPACING	OUT 6C2 7B8
M_BA0	100	4			::400:1400	200	TRUE	5 MIL SPACING	OUT 6A5 6C2
M_BA1	100	4			::400:1400	200	TRUE	5 MIL SPACING	OUT 6A5 6C2
SDRAS*	100	4			::400:1000	200	TRUE	5 MIL SPACING	OUT 6A5 6C2
SDCAS*	100	4			::400:1000	200	TRUE	5 MIL SPACING	OUT 6A5 6C2
MEMWE*	100	4			::400:1000	200	TRUE	5 MIL SPACING	OUT 6A5 6C2

VCORE_CSH	U19.1:R354.1::590	VCORE_CS	OUT
VCORE_CSL	U19.2:R354.2::590	VCORE_CS	OUT
2_5V_CSH	U20.1:R355.1::590	2_5V_CS	OUT
2_5V_CSL	U20.2:R355.2::590	2_5V_CS	OUT
VCORE_DH	U19.18:Q53.4::780		OUT
VCORE_DL	U19.15:Q42.4::780		OUT
VCORE_LX	U19.19:L59.1::590		OUT
2_5V_DH	U20.18:Q41.4::780		OUT
2_5V_DL	U20.15:Q10.4::780		OUT
2_5V_LX	U20.19:L38.1::590		OUT
+PBUS	C442.1:Q53.5::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS	C444.1:Q53.6::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS	C446.1:Q53.7::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38C4 38D6 39C3 39C6 43A4
+PBUS	C447.1:Q53.8::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS	C443.1:Q41.5::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
+PBUS	C313.1:Q41.6::390		OUT 19D4 24A4 32D5 34B4 34D5 34D8 37D8 38C3 38C4 38D6 39C3 39C6 43A4
VCORE_BST	U19.17:D31.3::780		OUT
2_5V_BST	U20.17:D30.3::780		OUT

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CONSTRAINTS -- MEMORY PAGE 2

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE	SHT	OF
NONE	43	53

AGP RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH / STUB_LENGTH	NET_SCHED	NET_SPACING_TYPE	DELAY_RULE	DELAY_RULE (THE SEQUEL!)	MIN_LINE_WIDTH
AGP_CLK	66 / 12	250 / 200	R213.1 U5.AG16	10 MIL SPACING	::3800:3900	5	
PANGEA_AGP_CLK	66 / 3	250 / 200		10 MIL SPACING	::0225:0275	5	
AGP_FB_IN	66 / 3	/ 200		10 MIL SPACING	::1325:1350	5	
AGP_FB_OUT	66 / 3	/ 200		10 MIL SPACING	::0320:0335	5	
AGPAD<31>	66 / 8	/ 200	U1.B11 U5.AK14	5 MIL SPACING	::3750:3980		
AGPAD<30>	66 / 8	/ 200	U1.E11 U5.AG14	5 MIL SPACING	::3750:3980		
AGPAD<29>	66 / 8	/ 200	U1.F12 U5.AG15	5 MIL SPACING	::3750:3980		
AGPAD<28>	66 / 8	/ 200	U1.C9 U5.AH14	5 MIL SPACING	::3750:3980		
AGPAD<27>	66 / 8	/ 200	U1.A9 U5.AJ15	5 MIL SPACING	::3750:3980		
AGPAD<26>	66 / 8	/ 200	U1.F11 U5.AH15	5 MIL SPACING	::3750:3980		
AGPAD<25>	66 / 8	/ 200	U1.A8 U5.AK16	5 MIL SPACING	::3750:3980		
AGPAD<24>	66 / 8	/ 200	U1.G11 U5.AK17	5 MIL SPACING	::3750:3980		
AGPAD<23>	66 / 8	/ 200	U1.B10 U5.AJ16	5 MIL SPACING	::3750:3980		
AGPAD<22>	66 / 8	/ 200	U1.A10 U5.AH18	5 MIL SPACING	::3750:3980		
AGPAD<21>	66 / 8	/ 200	U1.B9 U5.AK19	5 MIL SPACING	::3750:3980		
AGPAD<20>	66 / 8	/ 200	U1.B8 U5.AJ18	5 MIL SPACING	::3750:3980		
AGPAD<19>	66 / 8	/ 200	U1.E12 U5.AG18	5 MIL SPACING	::3750:3980		
AGPAD<18>	66 / 8	/ 200	U1.C8 U5.AJ19	5 MIL SPACING	::3750:3980		
AGPAD<17>	66 / 8	/ 200	U1.C11 U5.AH19	5 MIL SPACING	::3750:3980		
AGPAD<16>	66 / 8	/ 200	U1.A7 U5.AG19	5 MIL SPACING	::3750:3980		
AGPAD<15>	66 / 8	/ 200	U1.E14 U5.AJ22	5 MIL SPACING	::3020:3270		
AGPAD<14>	66 / 8	/ 200	U1.F14 U5.AH22	5 MIL SPACING	::3020:3270		
AGPAD<13>	66 / 8	/ 200	U1.C12 U5.AK22	5 MIL SPACING	::3020:3270		
AGPAD<12>	66 / 8	/ 200	U1.F15 U5.AG23	5 MIL SPACING	::3020:3270		
AGPAD<11>	66 / 8	/ 200	U1.C14 U5.AH23	5 MIL SPACING	::3020:3270		
AGPAD<10>	66 / 8	/ 200	U1.F13 U5.AK25	5 MIL SPACING	::3020:3270		
AGPAD<9>	66 / 8	/ 200	U1.A12 U5.AK23	5 MIL SPACING	::3020:3270		
AGPAD<8>	66 / 8	/ 200	U1.B12 U5.AH24	5 MIL SPACING	::3020:3270		
AGPAD<7>	66 / 8	/ 200	U1.B13 U5.AK27	5 MIL SPACING	::3020:3270		
AGPAD<6>	66 / 8	/ 200	U1.C15 U5.AK24	5 MIL SPACING	::3020:3270		
AGPAD<5>	66 / 8	/ 200	U1.B14 U5.AH26	5 MIL SPACING	::3020:3270		
AGPAD<4>	66 / 8	/ 200	U1.F16 U5.AG24	5 MIL SPACING	::3020:3270		
AGPAD<3>	66 / 8	/ 200	U1.A11 U5.AJ27	5 MIL SPACING	::3020:3270		
AGPAD<2>	66 / 8	/ 200	U1.A13 U5.AK26	5 MIL SPACING	::3020:3270		
AGPAD<1>	66 / 8	/ 200	U1.A14 U5.AH27	5 MIL SPACING	::3020:3270		
AGPAD<0>	66 / 8	/ 200	U1.E15 U5.AJ28	5 MIL SPACING	::3020:3270		
AGPADSTB<1>	66 / 8	/ 200	R779.2 U5.AG17	10 MIL SPACING	::0500:0550		
AGPADSTB<0>	66 / 8	/ 200	R778.2 U5.AH25	10 MIL SPACING	::0600:0650		
AGPSBA<7>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<6>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<5>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<4>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<3>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<2>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<1>	66 / 8	/ 200		5 MIL SPACING			
AGPSBA<0>	66 / 8	/ 200		5 MIL SPACING			
AGPSBSTB	66 / 5	/ 200		10 MIL SPACING	::4385:4490		
AGPCBE<3>	66 / 8	/ 200	U1.E9 U5.AK18	5 MIL SPACING	::3750:3980		
AGPCBE<2>	66 / 8	/ 200	U1.F9 U5.AK21	5 MIL SPACING	::3750:3980		
AGPCBE<1>	66 / 8	/ 200	U1.A6 U5.AG22	5 MIL SPACING	::3020:3270		
AGPCBE<0>	66 / 8	/ 200	U1.F10 U5.AJ24	5 MIL SPACING	::3020:3270		
AGPST<2>	66 / 8	/ 200	U1.A15 U5.AK12	5 MIL SPACING	::3500:4500		
AGPST<1>	66 / 8	/ 200	U1.G16 U5.AJ12	5 MIL SPACING	::3500:4500		
AGPST<0>	66 / 8	/ 200	U1.B15 U5.AG12	5 MIL SPACING	::3500:4500		
AGPPAR	66 / 8	/ 200	U1.A16 U5.AJ21	5 MIL SPACING	::3500:4500		
AGPFRAME*	66 / 8	/ 200	U1.B17 U5.AH20	5 MIL SPACING	::3500:4500		
AGPTRDY*	66 / 8	/ 200	U1.B16 U5.AK20	5 MIL SPACING	::3500:4500		
AGPIRDY*	66 / 8	/ 200	U1.C17 U5.AG20	5 MIL SPACING	::3500:4500		
PCISTOP*	66 / 8	/ 200	U1.E17 U5.AH21	5 MIL SPACING	::3500:4500		
AGPDEVSEL*	66 / 8	/ 200	U1.B7 U5.AG21	5 MIL SPACING	::3500:4500		
AGPPIPE*	66 / 8	/ 200	U1.B5 U5.AG13	5 MIL SPACING	::3500:4500		
AGPRBF*	66 / 8	/ 200	U1.B6 U5.AH12	5 MIL SPACING	::3500:4500		

OUT 9C5 22C6
OUT 9C4
OUT 9C3
OUT 9C3
OUT 9B2 9D1 22D6 22D7
OUT 9B2 9D1 22D6 22D7
OUT 9B2 9D1 22D6 22D7
OUT 9C2 9D1 22D6 22D7
OUT 9C2 9D1 22D6 22D7
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OUT 9D1 9D2 22C6 22D7
OUT 9D1 9D2 22C6 22D7
OUT 9A1 14C5 22B7
OUT 9A1 14C5 22B7
OUT 9B1 22B6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 22A6 22B7
OUT 9B1 14C5 22A7
OUT 9B1 9B2 22C6 22C7
OUT 9B1 9B2 22C6 22C7
OUT 9B1 9B2 22C6 22C7
OUT 9B1 9B2 22C6 22C7
OUT 9A1 22B6 22B7
OUT 9A1 22B6 22B7
OUT 9B1 22B6 22B7
OUT 9B1 22C6
OUT 9B1 14C5 24D6
OUT 9B1 14C5 24D6
OUT 9B1 14C5 24D6
OUT 9B1 14B5 24D5
OUT 9B1 14C5 24C6
OUT 9A1 14B5
OUT 9A1 14B5 22A6

CONSTRAINTS -- AGP, FIREWIRE

FIREWIRE RELATED DOO-DAHS

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	
FW_XI	24.576 / 2	250	200	10 MIL SPACING	
FW_XO	24.576 / 2	250	200	10 MIL SPACING	
FW_LINK_SCLK	49.152 / 4	250	200	10 MIL SPACING	
PHYSCLK	49.152 / 4	250	200	10 MIL SPACING	
FW_LINK_D<7>	49.152 / 4		200		
FW_LINK_D<6>	49.152 / 4		200		
FW_LINK_D<5>	49.152 / 4		200		
FW_LINK_D<4>	49.152 / 4		200		
FW_LINK_D<3>	49.152 / 4		200		
FW_LINK_D<2>	49.152 / 4		200		
FW_LINK_D<1>	49.152 / 4		200		
FW_LINK_D<0>	49.152 / 4		200		
FW_LINK_CNTL1	49.152 / 4		200		
FW_LINK_CNTL0	49.152 / 4		220		
FW_LINK_LREQ	49.152 / 4		200		
PHYD7	49.152 / 4		200		
PHYD6	49.152 / 4		200		
PHYD5	49.152 / 4		200		
PHYD4	49.152 / 4		200		
PHYD3	49.152 / 4		200		
PHYD2	49.152 / 4		200		
PHYD1	49.152 / 4		200		
PHYD0	49.152 / 4		200		
PHYCNTL1	49.152 / 4		200	5 MIL SPACING	
PHYCNTL0	49.152 / 4		200	5 MIL SPACING	
PHYLREQ	49.152 / 4		200	5 MIL SPACING	

OUT 19B7
OUT 19B7
OUT 10B3 19A8
OUT 19A7 19B7
OUT 10B3 19A7
OUT 10B3 19A7
OUT 10B3 19A7
OUT 10B3 19A7
OUT 10C3 19A7
OUT 10C3 19A8
OUT 10C3 19A8
OUT 10B3 19A8
OUT 10B3 19A8
OUT 10B3 19B8
OUT 19A7 19B7
OUT 19A7 19B7
OUT 19A7 19B7
OUT 19A7 19B7
OUT 19A7 19B7
OUT 19A7 19B7
OUT 19A7 19B7
OUT 20 19A7 19B7
OUT 20 19A7 19B7
OUT 19B7

FIREWIRE DIFFERENTIAL THINGIES

SIG_NAME	PULSE_PARAM / MAX_VIA_COUNT	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	ECL	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PHYTPA0T	400 / 2	250		TRUE		PHYTPA0
PHYTPA0C	400 / 2	250		TRUE		PHYTPA0
PHYTPB0T	400 / 2	250		TRUE		PHYTPB0
PHYTPB0C	400 / 2	250		TRUE		PHYTPB0
PHYTPA0T_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPA0C_FL	400 / 2	250		TRUE		PHYTPA0_FL
PHYTPB0T_FL	400 / 2	250		TRUE		PHYTPB0_FL
PHYTPB0C_FL	400 / 2	250		TRUE		PHYTPB0_FL

OUT 19C3
OUT 19B1
OUT 19B6
OUT
OUT 19C2
OUT 19C2
OUT 19C2
OUT 19C2

CONSTRAINTS -- AGP, FIREWIRE

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0

SCALE NONE | SHT 44 OF 53

SIG_NAME	PULSE_PARAM	MAX_EXPOSED_LENGTH	ECL	DIFFERENTIAL_PAIR	MAX_VIA_COUNT	STUB_LENGTH	DELAY_RULE	NET_SPACING_TYPE	
UIDE_DA<0>	66				6		::5170:5920	5 MIL SPACING	OUT 12B6 12C5
UIDE_DA<1>	66				6		::5170:5920	5 MIL SPACING	OUT 12B6 12C5
UIDE_DA<2>	66				6		::5170:6100	5 MIL SPACING	OUT 12A6 12C5
UIDE_IORDY	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 16B8
UIDE_CS0_L	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 12C5
UIDE_CS1_L	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 12C5
UIDE_RESET_L	66				6		::1600:2000	5 MIL SPACING	OUT 12A6 12C5
UIDE_DIOW_L	66				6		:::5920	10 MIL SPACING	OUT 12A6 12C5
UIDE_DIOR_L	66				6		:::5920	10 MIL SPACING	OUT 12A6 12C5
UIDE_DMAACK_L	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 12B5
UIDE_DMAREQ	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 12D5
UIDE_IRQ	66				6		::5170:5920	5 MIL SPACING	OUT 12A6 12D5
UIDE_D<0>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<1>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<2>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<3>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<4>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<5>	66				6		::5170:5920	5 MIL SPACING	OUT 12B5 12B6 12B7
UIDE_D<6>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<7>	66				6		U1.J30:RP19.4:5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<8>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<9>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<10>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<11>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<12>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<13>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<14>	66				6		::5130:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
UIDE_D<15>	66				6		::5170:5920	5 MIL SPACING	OUT 12A5 12B6 12B7
T_UIDE_RESET_L	66				6	100	R300.2:710.1:3508:3858	5 MIL SPACING	OUT 12C4 16B6 16C7
MII_TX_CLK_F	2.5,25		TRUE		4	100	::300:500	10 MIL SPACING	OUT 18D6
MII_RX_CLK_F	2.5,25		TRUE		4		::300:500	10 MIL SPACING	OUT 18C6
MII_TX_CLK	2.5,25	250	TRUE		4	100	:::6000	10 MIL SPACING	OUT 10C7 18D7
MII_RX_CLK	2.5,25	250	TRUE		4	100	:::6000	10 MIL SPACING	OUT 10C7 18C7
MII_TPTDP	10,100				2	100		10 MIL SPACING	OUT 18D3
MII_TPTDN	10,100				2	100		10 MIL SPACING	OUT 18D3
MII_TPRDP	10,100				2	100		10 MIL SPACING	OUT 18C3
MII_TPRDN	10,100				2	100		10 MIL SPACING	OUT 18C3
								2KV_ISO===100 MIL SPACING	
RJ45_TXP	10,100			RJ45_TX	2	100		1	OUT 18D1
RJ45_TXN	10,100			RJ45_TX	2	100		1	OUT 18D1
RJ45_RXP	10,100			RJ45_RX	2	100		1	OUT 18D1
RJ45_RXN	10,100			RJ45_RX	2	100		1	OUT 18C1
PAN_XIB	18.432		TRUE		3		:::1000	10 MIL SPACING	OUT 13B7
PAN_XO	18.432		TRUE		2	100	:::1000	10 MIL SPACING	OUT 13B7
PAN_XT	18.432		TRUE		2		:::500	10 MIL SPACING	OUT 13B7
PMU_10MHZ_XOUT	10		TRUE		2	100	:::1000	10 MIL SPACING	OUT 21B5
PMU_10MHZ_XIN	10		TRUE		2	100	:::1000	10 MIL SPACING	OUT 21B5
PMU_32KHZ_XOUT	0.032768		TRUE		2	100	:::1000	10 MIL SPACING	OUT 21B4
PMU_32KHZ_XIN	0.032768		TRUE		2	100	:::1000	10 MIL SPACING	OUT 21B4
T_UIDE_DIOW_L	66				6		::5170:5920	10 MIL SPACING	OUT 12C4 16B6
T_UIDE_DIOR_L	66				6		::5170:5920	10 MIL SPACING	OUT 12C4 16B6

SIG_NAME	ECL	DIFFERENTIAL_PAIR	NET_SPACING_TYPE	
USB_DCM	TRUE	USB_DC		OUT 13C5 17D8
USB_DCP	TRUE	USB_DC		OUT 13C5 17D8
USB_DAM	TRUE	USB_DA		OUT 13C5 17B8
USB_DAP	TRUE	USB_DA		OUT 13C5 17B8
USB_DCM_R	TRUE	USB_DC_R		OUT 17D5
USB_DCP_R	TRUE	USB_DC_R		OUT 17D5
USB_DAM_R	TRUE	USB_DA_R		OUT 17B5
USB_DAP_R	TRUE	USB_DA_R		OUT 17B5
USB_DCM_OUT	TRUE	USB_DC_OUT		OUT 17D2
USB_DCP_OUT	TRUE	USB_DC_OUT		OUT 17D2
USB_DAM_OUT	TRUE	USB_DA_OUT		OUT 17B1
USB_DAP_OUT	TRUE	USB_DA_OUT		OUT 17B1

SIG_NAME	NET_SCHED	
IODATA<0>	U1.P34 R323.2 R324.1 U3.25 J11.30	OUT 20C2 12D6 12D7 13B3 13B4 20B8 20C1
IODATA<1>	U1.R32 R325.2 R326.1 U3.26 J11.31	OUT 12D6 12D7 13B3 13B4 20B2 20B8
IODATA<2>	U1.T29 R327.2 R328.1 U3.27 J11.32	OUT 20C1 12D6 12D7 13B3 20C8 13B4 20B2 20B8 20C1
IODATA<3>	U1.T28 R329.2 R330.1 U3.28 J11.2	OUT 12D6 12D7 13B3 13B4 20B2 20C1
IODATA<4>	U1.R33 R334.2 R335.1 U3.32 J11.3	OUT 12D6 12D7 13B3 13B4 20B2 20C1
IODATA<5>	U1.R34 R336.2 R327.1 U3.33 J11.4	OUT 20C8 12D6 12D7 13B3 20C8 13B4 20B2 20C1 20C8
IODATA<6>	U1.U29 R338.2 R339.1 U3.34 J11.5	OUT 12D6 12D7 13B3 13B4 20B2 20C1
IODATA<7>	U1.T33 U3.35 J11.6	OUT
IOADDR<0>	U1.N28 U3.21 J11.29	OUT 12C6 20B8 20C3
IOADDR<1>	U1.J34 U3.20 J11.28	OUT 12C6 20B3 20B8
IOADDR<2>	U1.M30 U3.19 J11.27	OUT 12C6 20B3 20B8
IOADDR<3>	U1.L32 U3.18 J11.26	OUT 12C6 20B3 20B8
IOADDR<4>	U1.K34 U3.17 J11.25	OUT 12C6 20B3 20B8
IOADDR<5>	U1.L33 U3.16 J11.24	OUT 13C5 20B3 20B8
IOADDR<6>	U1.N29 U3.15 J11.23	OUT 13B5 20B3 20B8
IOADDR<7>	U1.M32 U3.14 J11.22	OUT 13B5 20B3 20B8
IOADDR<8>	U1.L34 U3.8 J11.12	OUT 13B5 20B3 20B8
IOADDR<9>	U1.P28 U3.7 J11.11	OUT 13B5 20B3 20B8
IOADDR<10>	U1.M33 U3.36 J11.8	OUT 13B5 20B3 20C8
IOADDR<11>	U1.P29 U3.6 J11.10	OUT 13B5 20B3 20C8
IOADDR<12>	U1.M34 U3.5 J11.21	OUT 13B5 20B3 20B8
IOADDR<13>	U1.P30 U3.4 J11.13	OUT 13B5 20B3 20B8
IOADDR<14>	U1.N33 U3.3 J11.14	OUT 13B5 20B3 20B8
IOADDR<15>	U1.R28 U3.2 J11.20	OUT 13B5 20B3 20B7
IOADDR<16>	U1.P32 U3.1 J11.19	OUT 13B5 20B3 20B8
IOADDR<17>	U1.N34 U3.40 J11.46	OUT 13B5 20B3 20B6
IOADDR<18>	U1.R29 U3.13 J11.47	OUT 13B5 20B3 20B6
IOADDR<19>	U1.P33 U3.37 J11.48	OUT 13B5 20B3 20B6
IOADDR<20>	U1.R30 U3.38 J11.49	OUT 13B5 20B3 20B6

SIG_NAME	NET_SCHED	
CB_CE2*	U1.W28 RP43.4 J11.42	OUT 12B6 15C6 20C6
CB_CE1*	U1.W29 RP43.3 J11.7	OUT 12B6 15C6 20C8
CB_IORD*	U1.W33 RP43.1 J11.44	OUT 13B5 15C6 20C6
CB_IOWR*	U1.W34 RP43.2 J11.45	OUT 13B5 15C6 20B6
CB_IREQ*	U1.A32 R370.1 J11.16	OUT 13C7 15B6 20B8
CB_REG*	U1.B31 R368.1 J11.61	OUT 13C7 15B6 20B6
CB_RESET	U1.AE33 R306.2 J11.58	OUT 13C8 15A6 20B6
CB_WAIT*	U1.Y34 R369.1 J11.59	OUT 13B5 15B6 20B6
CSWE*	U1.V29 RP44.2 J11.15	OUT 12C6 15C6 20B8
CSOE*	U1.Y33 RP44.1 J11.9	OUT 12C6 15C6 20C8

2KV_ISO === 100MIL SPACING
MANUALLY TAKE CARE OF 2KV FOR ETHERNET

CONSTRAINTS -- MISCELLANEOUS

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0

SCALE NONE | SHT 45 OF 53

NET ATTRIBUTES

I1	F_ACOUT	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I2	ACOM_IN_RL	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I3	A_COM_IN_RC	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I4	A_COM_IN	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I5	SPKR_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	27B3 27B4 27C3 27C4 27C6 28B3 28B8 28C4 28C8 29A5 29C2
I6	MB_IN_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	39B8 46D7
I8	LINE_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I7	LINE_OUT_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	46D7
I10	SPKR_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	27B3 27B4 27C3 27C4 27C6 28B3
I9	DIG_STAR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	28B8 28C4 28C8 29A5 29C2 39B8
I11	SCREAMER_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I12	LINE_OUT_COM_STAR	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I13	ACOUT_RL	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I14	ACOUT_LCL	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I15	ACOUT	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I17	SCREAMER_RET	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I16	SPEAKER_RET	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I18	SCREAMER_DVDD_RET	VOLTAGE=0V	MIN_LINE_WIDTH=10MIL	
I19	+AVCC_SCREAMER	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	
I23	+AVCC_F_SCREAMER	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	
I21	+DVDD_F_SCREAMER	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	
I22	+6V_AUDIO	VOLTAGE=6V	MIN_LINE_WIDTH=10MIL	17C7 17D7 27C8 29C3 29D5 34D3
I20	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	46C7 16C2 17B7 19D4 24D2 28C4
I24	FILT_MIC_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	34C2 35D8 36B3 37B4 37D4 38B3
I25	MIC_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	38B8 38C5 40D6
I27	+24V_EXT	VOLTAGE=24V	MIN_LINE_WIDTH=50MIL	
I26	ADAPTER_+24V	VOLTAGE=24V	MIN_LINE_WIDTH=50MIL	
I28	+24V_EXT_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50MIL	
I29	+5V_VGADDCPWR_SLEEP_F	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	25D5
I30	+5V_VGA_FUSE	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	25D6 40C6
I31	+3V_VGA_MAIN	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	14D3 14D4 22A4 22C5 22D8 23B8 23C1
I32	+AUD3.3V	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	27D6 23C8 24C2 25C2 25D2 36C4 46B7
I33	+5V_MAIN_A	VOLTAGE=5V	MIN_LINE_WIDTH=20MIL	27D8 28B8 28C6
I34	+6V_AUDIO	VOLTAGE=6V	MIN_LINE_WIDTH=20MIL	17C7 17D7 27C8 29C3 29D5 34D3 46C7
I35	+AUD5V	VOLTAGE=5V	MIN_LINE_WIDTH=10MIL	27C6 29B3 29C3 29D5
I36	FIL2_AUD3.3V	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	27D4
I37	FIL2_DIG3.3V	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	27B6 27C2 27C5
I38	+AVDD_CPU_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3B3
I39	+A1VDD_CPU_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3B2
I40	+A2VDD_CPU_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3A2
I41	+A1VDD_CPU_F_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3B1 3D6
I42	+A2VDD_CPU_F_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3A1 3D6
I43	+VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=10MIL	3D4 38B3 38C1 40C6
I44	+VIO_CPU_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	3C4 3D5 4B4 4D5 5C2 13D1 14A6 14A7 14C6 14D6 14D8 15B1
I45	+3V_MAIN	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	15D2 35C3 36B4
I46	+2.5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=10MIL	
I47	+3V_SLEEP	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	4C6 6B5 6C5 9D4 13B3 15A5 15B5 15B7 15C5 15C7 20C8 20D6
I48	+3V_CLKGEN_AVDD_SLEEP	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	22B5 22C1 25A6 25B5 25D4 27C6 35D2 40D4
I49	+3V_CLKGEN_SLEEP	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	6B4 6D8
I50	+1_8V_PVDD_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	6C4 6C8 6D4 6D8
I51	+1_8V_AVDD_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	23B7 23D6
I52	+1_8V_A2VDDQ_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	23D6
I53	ATI_CORE_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	23D6
I54	+1_8V_LVDDR_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	22A5 22C8 23D7 37C8
I55	+1_8V_MPVDD_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=10MIL	23A5
I56	+3V_VDDP_MAIN	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	23A5
I57	+3V_VGA_MAIN	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	23C6
I58	+3V_VDDR3_MAIN	VOLTAGE=3V	MIN_LINE_WIDTH=10MIL	14D3 14D4 22A4 22C5 22D8 23B8 23C1 23C8 24C2 25C2 25D2 36C4
I59	+2.5V_ATI_VDDR_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=10MIL	23C3 46C7

MLB STACKUP

LAYER		THICKNESS (MILS)	TRACE WIDTH (MILS)
L1	SIGNAL(TOP)	1.560	5.0
L1-L2		3.740	
L2	GROUND1(GND)	1.170	---
L2-L3		6.500	
L3	SIGNAL(IN1)	1.170	5.0
L3-L4		6.300	
L4	SIGNAL(IN2)	1.170	5.0
L4-L5		6.500	
L5	POWER(VCC)	1.170	---
L5-L6		6.500	
L6	SIGNAL(IN3)	1.170	5.0
L6-L7		6.500	
L7	GROUND2(GND)	1.170	---
L7-L8		3.540	
L8	SIGNAL(BOTTOM)	1.560	5.0
TOTAL			---

SIGNAL TRACE IMPEDANCE OF ? OHMS

CPU ROUTES ARE ? OHMS?
AGP ROUTES ARE 5 MILS OHMS?
RAM ROUTES ARE ? OHMS?

NET ATTRIBUTES

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 46 OF 53	

REVISION HISTORY (1)

SAHARA QUAL PCB(REV:0.0)

1) CHANGE CPU FROM SIDEWINDER TO SAHARA
2) CHANGE VGA FROM ATI-M3 TO ATI-M6
3) CHANGE AUDIO FROM TUMBLER TO SNAPPER

PROTO (REV:0.1)

1) ACCORDING RADAR#2773492 - UPDATES TO THE P72 SCHEMATICS

2) ACCORDING RADAR#2774277 - P72 M6 SCHEMATICS FIXES FOR PROTO2
   A) UNSTUFF R902,R903,R905
   B) CHANGE R906 TO 100K AND PULL UP TO VDDC
   C) STUFF R914,R916 FOR M6 16MB VERSION
   D) ADD R1116(0OHM) BETWEEN C954 AND C955
   E) UNSTUFF R395 AND Q56

3) ACCORDING RADAR#2775061 - CHANGE P72 TO HARDWARE CHARGING

4) ACCORDING RADAR#2777820 - NEW AVC CABLE CONNECTIONS
   A) ADD U210(74LVC1G125),F100,Q210,Q211,C1210,R957,R958,R959 FOR NEW AVC CONNCETOR.

5) ACCORDING RADAR#2780508 - CHANGE TO THE AUDIO POWER DOWN CIRCUIT
   A) REMOVE R462,R599,R600,R601,R602,R603,C638,Q86,Q87
   B) CONNECT U300/PIN8 TO DGND
   C) CONNECT U300/PIN6 TO IO_RESET_L
   D) CHANGE U4/PIN AA33 NAME FROM AUDIO_HW_RESET_L TO PAN_GPIO1
   E) ADD 10K PULLUP FOR PAN_GPIO1

6) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0

7) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT
   A) ADD U1200(ADM1030) AND Q1000 FOR NEW FAN CONTROL CIRCUIT

8) ACCORDING RADAR#2782007 - DASH MODEM PERFORMANCEIMPACTED BY VCORE SWITCHER
   A) DISCONNECT ZH2 FROM GND

9) ACCORDING RADAR#2782669 - ADD OPTIONAL CONTROL FOR VCORE VLOTAGE
   A) CHANGE U4/PIN AA33 NET NAME FROM PAN_GPIO1 TO VCORE_CTL
   B) REMOVE THE NET NAME "CPU_VCORE_HI_OC" FROM U1/PIN16
   C) ADD R1552 BETWEEN U1/PIN16 AND THE NET "CPU_VCORE_HI_OC"
   D) ADD R1553(NOSTUFF) BETWEEN U1/PIN16 AND NET "VCORE_CTL"

10) ACCORDING RADAR#2782721 - ADDITIONAL M6 CHANGES FOR OK TO FAB
   A) ADD R954 FOR VGA_CORE_HI_OC SIGNAL PULLUP
   B) CHANGE Q1504/PIN2 CONNECTION FROM PS_GND TO MAX1715_GND
   C) CHANGE THE NET NAME FROM VGA_VCORE_HI_OC TO VGA_VCORE_HI

11) ACCORDING RADAR#2782641 - EXTERNAL VIDEO SCHEMATICS CHANGE
   A) REMOVE R394,R393,R395,Q56,R392,C905
   B) CHANGE R935,R936,R937 CONNECTION FROM U200/PIN AF22,AF23,AF24 TO U200/PIN AF14,AF15,AF16
   C) REMOVE COMPVSS SIGNAL AND L36

12) ACCORDING RADAR#2784789 - PROTO BUILD BOM CHANGES
   A) STUFF R803(113S1102),R805(113S1473,R820(113S1000),R1110,R1111, C1109,C1110,Q809,Q810
   B) UNSTUFF R1115,R1112,Q211
   C) CHANGE R539 TO 3.16K,1% (110S3163)

EVT (REV:0.2)

1) ACCORDING RADAR#2798007 - ADD AUDIO/CONTROL CONNECTOR
   A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13
   B) ADD CONTROL CIRCUITS FOR I-POD

2) ACCORDING RADAR#2794270 - SCHEMATICS CHANGE-NEW BLUETOOTH CONN.
   A) USE 4PIN J100 CONN TO REPLACE J100(6PIN)
   B) CHANGE THE USB-D CIRCUITS FOR BLUETOOTH MODULE.

3) ACCORDING RADAR#2805677 - CHANGES FROM EVT LAYOUT REVIEW
   A) ADD R1300 BETWEEN J200-1 AND PAN_XIB
   B) ADD BYPASS CAP C1100 NEAR U802 ON +3V_CLKGEN_SLEEP
   C) MOVE RESISTORS R963,R964 AND R965 NEAR PANGEA
   D) CHANGE C803,C804 AND C805 FORM 1.0U TO 10.0U WITH 0805 PACKAGE
   E) ADD 4 MORE VIAS WHERE +3VCORE_SLEEP OF C800,C801,C836
   F) ADD AN EXTRA VIA ON PIN9 OF U32 TO GROUND
   G) MAKE THE TRACE FROM PIN2 OF D31 GO FIRST TO PIN1 OF C156,THEN TO PIN2 OF R1557
   H) MOVE R1555 CLOSER TO U1 AND L1

4) ACCORDING RADAR#2805288 - CHANGE TO OVERTEMP CIRCUIT
   A) CHANGE R1206 FORM 39K TO 27K

5) ACCORDING RADAR#2805242 - ADD RESISTOR TO SCC RTS SIGNAL FOR TESTING PURPOSES
   A) ADD R967 BETWEEN PIN1 OF U210 AND SCC_RTSA*
   B) NAMED SLINK_TX_ENABLE_L ON U210 PIN1

6) ACCORDING RADAR#2794331 - REMOVE BLEED CIRCUIT FOR VCORE RAIL
   A) NOSTUFF C177,R15,Q6,C20,R11,Q8

7) ACCORDING RADAR#2804787 - SCHEMATIC CHANGE-MOVE FAN TO SLEEP RAIL
   A) USE J900(NEW FOXCONN AUDIO JACK) TO REPLACE J13

8) ACCORDING RADAR#2801304 - RETURN JOLLY ROGER OPTION
   A) CONNECT SCC_RTSA* TO PIN6 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
   B) CONNECT SCC_RXDA TO PIN9 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
   C) CONNECT SCC_TXDA* TO PIN12 OF J2 THROUGH A NOSTUFF 0 OHM RESISTOR
   D) CONNECT SCC_DTRA TO PIN8 OF J2
   E) CONNECT SCC_TRXCA TO PIN14 OF J2

9) ACCORDING RADAR#2804786 - REMOVE CPU_VOCRE_LO_OC CIRCUIT
   A) REMOVE R832 AND Q808

10) ACCORDING RADAR#2803484 - ADD SLOW_CHRG AND FAST_CHRG BOM OPTION
   A) ADD TWO ROW OF BOM OPTION FOR - SLOW_CHRG FOR P72, FAST_CHRG FOR P73
   B) REMOVE THE HWCHG BOM FROM R539 AND ADD THE OMIT LABEL
   C) ADD A BOM OPTION FOR R539 - SLOW_CHRG 3.16K AND FAST_CHRG 2.61K

11) ACCORDING RADAR#2792009 - REMOVE UNUSED SCC LINES FOR MODEM
   A) REMOVE NETS SCC_DTRA* AND SCC_TRXCA
   B) KEEP THE PULLDOWN RESISTORS ON SCC_GPIOA* AND SCC_TRXCA

12) ACCORDING RADAR#2800865 - I CAN'T CHARGE IPOD WHILE IB00K IS SLEEPING
   A) ADD A 10BQ040 ,CATHODE CONNECT TO +FW_VP_FUSE_SW AND ANODE TO +28V_PWRBUS_SW

13) ACCORDING RADAR#2802944 - ATI SUGGESTION FOR AGP SUSPEND
   A) ADD A 0 OHM RESISTOR R966 BETWEEN AGP_SUS_STAT_L_PU AND AGPSTOP*

14) ACCORDING RADAR#2803479 - CHANGE SOME TANTALUM AUDIO CAPS TO CERAMIC
   A) CHANGE C607,C608 AND C391 FROM 1.0U TANT(127S1001) TO 1.0U CERMIC (132S1061)

15) ACCORDING RADAR#2803487 - MODIFICATION TO BATTERY CHARGING CIRCUIT
   A) ADD A 0 OHM RESISTOR SERIES BETWEEN PIN12 OF U32 AND PIN2 OF D31
   B) ADD A NOSTUFF 0.01U 003 CAP BETWEEN PIN4 OF Q73 AND PS_GND

16) ACCORDING RADAR#2794253 - TBEN CIRCUIT-CHANGE D FLIP FLOPS TO JK
   A) REPLACE THE DIVIDEBY THREE CIRCUIT WITH A DUAL J-K FLIP FLOP 74LVC109

17) ACCORDING RADAR#2800233 - CHANGE POWER SUPPLY FOR INTERNAL M6 DDR MEMORY
   A) CHANGE THE VDDM OF M6 TO 2.5V. SO, UNSTUFF R949 AND STUFF R950

18) ACCORDING RADAR#2794264 - AC CONNECTOR WAKE FROM SLEEP CIRCUIT CAHNGE
   A) MOVE F100 FROM PAGE 25 TO PAGE 28
   B) REMOVE TP210 AND TP211

19) ACCORDING RADAR#2794755 - HSYNC AND VSYNC NEED TO BE MOVED TO DAC2
   A) MOVE ATI_VSYNC FROM PIN AE23 TO PIN AF13
   B) MOVE ATI_HSYNC FROM PIN AE24 TO PIN AE14

20) ACCORDING RADAR#2795893 - VGA_VCORE_HI NEEDS TO BE HIGH AT POWERON
   A) CHANGE R956 TO 10K AND CONNECT TO +3V_MAIN

21) ACCORDING RADAR#2795903 - UNSTUFFED COMPONENTS ON SCHEMATICS
   A) UNSTUFF R1112 AND STUFF R1111,R1110,C1109,C1110,Q810 AND Q809

22) ACCORDING RADAR#2797834 - REMOVE PMU RESET BUTTON
   A) NOSTUFF S4

23) ACCORDING RADAR#2754201- LENGTH CONSTRAINTS FOR CPU BUS SIGNALS
   A) CHANGE THE CONSTRAINTS OF CPU BUS TO 2500:3500 AND THE MAX COUT OF VIA TO 5

24) ACCORDING RADAR#2794312 - FAN CIRCUITRY CHANGE
   A) CHANGE THE NAME OF THERM* TO THERM_OD*
   B) CHANGE R1206 TO 39K

25) ACCORDING RADAR#2794262- INVESTIGATE M6 PLL POWER RAIL ARRANGEMENT
   A) UNSTUFF R951 AND CONNECT +1_8V_PVDD_MAIN TO +1_8V_LVDDR_MAIN

26) ACCORDING RADAR#2794249 - NEW SPREAD SPECTRUM PART
   A) CHANGE THE SPREAD SPECTRUM CHIP FROM IMI C9531 TO CYPRESS CY28507
   B) ADD 2 RESISTORS - ONE BETWEEN PMU_IIC_CLK AND +3_3V_PMU ANOTHER IS PMU_IIC_DAT AND +3_3V_PMU

27) ACCORDING RADAR#2779003 - ADD A BOM OPTION TO PREPARE FOR SAHARA DD2.0
   A) SET DD1X BOM OPTION FOR P72/P73 AND CHANGE THE BOM OPTION OF Q800,Q801,R804,R805 TO DD1X

28) ACCORDING RADAR#2780490 - NEW FAN SPEED CONTROL CIRCUIT
   A) ADD A NEW FAN CONTROL CIRCUIT ADM1030 TO REPLACE THE TWO THERMOSTATS

29) ACCORDING RADAR#2791511 - ADD PMU RESET FROM KEYBOARD CIRCUIT
   A) ADD RESET FUNCTION BY PRESSING THE SHIFT-CONTROL-FN-POWER KEY TO REPLACE RESET SWITCH

30) ACCORDING RADAR#2794257 - CHANGE NAME OF AGPREF_PD
   A) CHANGE THE NAME OF AGPREF_PD TO AGPREF_PU

31) ACCORDING RADAR#2794329 - REMOVE BLEED CIRCUIT FOR ATI_CORE_MAIN
   A) REMOVE THE CURRENT BLEED CIRCUIT FOR ATI_CORE_MAIN IN THE BOTTOM LEFT CORNER ON PAGE 37

REVISION HISTORY (1)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE: NONE

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REVISION HISTORY (2)

32) ACCORDING RADAR#2791719 - SCHEMATIC CHANGE - REMOVE R1115
A) REMOVE R1115 BECAUSE SLEEP_L_LS IS ALREADY PULLED UP TO 5V RAIL

33) ACCORDING RADAR#2792071 - REMOVE UNUSED RGB SIGNALS ON PAGE 22
A) REMOVE THE UNUSED RGB SINGALS ON PAGE 22 (PIN AF22,AF23,AF24 ON M6) AND ADD NC FOR THEM

34) ACCORDING RADAR#2792085 - REMOVE OLD HP_DETECT SIGNALS ON PAGE 22
A) REMOVE THE COMPVID_HP_TEST AND COMPVID_HP_DETECT FROM PAGE 22 (AC20 AND AD20 ON M6)

DVT (REV:0.3)

1) ACCORDING RADAR#2843372 - ADD BACK FIREWIRE DIODE
A) STUFF D1506

2) ACCORDING RADAR#2823008 - P72 EVT UNITS PLUG IN A BUS POWERED YANO FW HARD DRIVE - SCREEN GOES DARK. POWER PROBLEM
A) CHANGE THE NET OF D1506 PIN1 FROM +28V_PWRBUS_SW TO CHRG_OUT AND NOSTUFF D1506
B) CHANGE C160 FROM 0.01UF TO 0.1UF

3) ACCORDING RADAR#2838736 - SCHEMATIC CHANGE - 700 MHZ AND 1.5V
A) CHANGE BOM TABLE OF CPU FROM 750MHZ TO 700MHZ
B) REMOVE THE BOM OPTION ON R825
C) CHANGE 600MHZ CPU VCORE TO 1.5V

4) ACCORDING RADAR#2840812 - CHANGE ALL MCLK LINES TO USE 0 OHM SEIES TERMINATION RESISTORS
A) CHANGE R841,R843,R847 TO 0 OHM

5) ACCORDING RADAR#2831933 - P72 PLL RANGE CONFIGURATIONS
A) ALL CONFIGS SHOULD NOW HAVE THE "MID" PLL RANGE OPTIONS (NO POWERSTEP)
B) ADD "MID OR HIGH RANGE NO PWRSTEP" AND LOW OR MID PLL RANGE" ROW FOR P72 GOOD CONFIG
C) REMOVE "LOW PLL RANGE" ROW UNDER THE P72 CONFIGURATION

6) ACCORDING RADAR#2830139 - P72 IMPLEMENT POWERPLAY ON M6 ON P72
A) CHANGE C1505 TO 680P AND ADD C1521 1000P

7) ACCORDING RADAR#2831140 - P72 SCHEMAITC REVIEW ACTION ITEMS

8) ACCORDING RADAR#2824938 - REQUIRED WAKEUP PULSE ON P72 HEADPHONE JACK TAKES TOO LONG (H/W)
A) CHANGE C1210 WITH 0.047UF CAP AND PACKAGE FROM 0805 TO 0603

9) ACCORDING RADAR#2829465 - AUDIO FIX - Q900
A) PIN 2 AND 3 OF Q900 ARE REVERSED. PIN2 SHOULD CONNECT TO GROUND.

10) ACCORDING RADAR#2820867 - TBEN DIVIDE-BY-THREE SCHEMATIC REPAIR
A) CHANGE NET OF U802 PIN1 AND PIN15 FORM +3V_CLKGEN_SLEEP TO CPU_VCORE_HI_OC

11) ACCORDING RADAR#2825538 - KEYBOARD CHORD RESET OF PMU BOOTS
A) CHANGE NET OF U800 PIN5 FROM FN_KEY_L TO OPTION_KEY_L
B) NOSTUFF R19
C) CHANGE R1554 FROM 1K(113S1103) TO 10K(113S1104)

12) ACCORDING RADAR#2828251 - PMU IIC PULLUPS WRONG AT EVT
A) ADD R1120 10K RESISTOR BETWEEN +3V_SLEEP AND THE SIGNAL PMU_IIC_DAT
B) ADD R1121 10K RESISTOR BETWEEN +3V_SLEEP AND THE SIGNAL PMU_IIC_CLK
C) CHANGE THE VOLTAGE ON R1118-2 FROM +3_3V_PMU TO +3V_CLKGEN_SLEEP
D) CHANGE THE VOLTAGE ON R1119-2 FROM +3_3V_PMU TO +3V_CLKGEN_SLEEP

13) ACCORDING RADAR#2829528 - UPDATE NO PWRSTEP BOM OPTION FOR NEW PLL RANGE BITS
A) ADD R1122 10K (BETWEEN Q806 PIN2 AND PIN3) WITH "MID OR HIGH RANGE NO PWRSTEP"
B) ADD R1123 4.7K (BETWEEN Q807 PIN2 AND PIN3) WITH "HIGH PLL RANGE NO PWRSTEP"
C) CHANGE Q806 BOM OPTION TO "MID OR HIGH RANGE PWRSTEP"
D) CHANGE Q807 BOM OPTION TO "HIGH PLL RANGE PWRSTEP"
E) DELETE TWO ROWS ON PAGE 1 "MID RANGE PLL" AND "MID OR HIGH RANGE PLL"
F) ADD 4 ROWS ON PAGE 1 - "MID OR HIGH RANGE NO PWRSTEP" , "HIGH PLL NO PWRSTEP"
"MID OR HIGH RANGE PWRSTEP" , "HIGH PLL RANGE PWRSTEP"

14) ACCORDING RADAR#2830159 - FAST CHARGE FOR ALL SYSTEM CONFIGS
A) CHANGE ALL SYSTEM CONFIGS TO USE THE FAST_CHRG OPTION ON PAGE 1

15) ACCORDING RADAR#2841691 - SERIAL LINE REMAINSAT INTERMEDIATE LEVEL
A) CHANGE R959 FORM 100K(113S1105) TO 470K (113S1475)
B) CHANGE C1210 FROM 0.047UF (132S4743) TO 0.01UF (132S1045)

DVT2 (REV:0.4)

1) ACCORDING RADAR#2855154 - SNAPPER AUDIO CHIP NEEDS SEPARATE RESET
A) ADD Q901,Q902 (2N7002), AND R1031 (100K,5%)
B) CHANGE NET NAME OF U300 PIN6 FROM IO_RESET_L TO TAS_RESET_L

2) ACCORDING RADAR#2856224 - SCHEMATIC CHANGE - ARTRY PULL UP
A) DISCONNECT ARTRY* FROM RP101
B) PULL UP ARTRY* WITH 1K RESISTOR (R1032) TO +VIO_CPU_SLEEP

3) ACCORDING RADAR#2856231 - MORE BYPASS CAPACITORS ON SAHARA
A) ADD C980,C981(10U 0805) FOR +VCORE_SLEEP

4) ACCORDING RADAR#2862722 - INCREASE BANDWIDTH OF MICROPHONE AMPLIFIER
A) CHANGE C1017 FROM 0.022UF TO 0.047UF
B) CHANGE C1021 FROM 150P TO 47P
C) CHANGE C1022 FROM 0.047UF TO 0.1UF
D) CHANGE R1019 FROM 36K TO 10K

5) ACCORDING RADAR#2831587 - P72 EVT : POP HEARD WHEN PLUG HEADPHONES INTO ANALOG LINE OUT
A) CHANGE R139 FROM 100K TO 470K

6) ACCORDING RADAR#2862391 - CHANGE NAME OF BOM OPTION
A) CHANGE R1123 BOM OPTION TO "HIGH_PLL_RANGE_NO_PWRSTEP"
B) CHANGE PAGE 1 BOM TABEL FROM "HIGH PLL RANGE NO PWRSTEP" TO "HIGH_PLL_RANGE_NO_PWRSTEP"

7) ACCORDING RADAR#2865479 - CHANGE CPU VCORE SETTING (LOW SETTING AND VOLTAGE POSITIONING)
A) CHANGE R1531 FROM 1K TO 100K FOR P72 GOOD CONFIGURATION
B) CHANGE R1535 FROM 100K TO 1K
C) DELETE R1542 AND R1543
D) ADD A 0 OHM RESISTOR R1560

PVT (REV: A)

1) ACCORDING RADAR#2868519 - SOUND LEVEL RESETS TO LOW - UPDATE FOR PVT
B) ADD A NAND GATE 74LVC1G32 FOR AUDIO RESET CIRCUIT

2) ACCORDING RADAR#2874422 - FIREWIRE DEAD ON P25 AND P92 DVT
A) ADD TWO QUAD DIODE FOR PHYTPA0T,PHYTPA0C,PHYTPB0T,PHYTPB0C

3) ACCORDING RADAR#2878614 - P72/P73 POPS FROM INTERNAL SPEAKERS POST AUDIO REWORK
A) NOSTUFF D100 AND D101
B) CHANGE C1026 AND C1027 FROM 0.047UF TO 0.1UF

4) ACCORDING RADAR#2882917 - FIREWIRE AND BATTERY CHARGING PROTECTION
A) STUFF DZ8 AND DZ9
B) CHANGE VALUE OF C467 TO 0.1UF

PVT (REV: A)

1) ACCORDING RADAR#2890158 - P72 DEPLETED BATTERY MAY NOT CHARGE IN SYSTEM
A) CHANGE R518 AND R538 FROM 100K TO 93.1K

PVT2 (REV: A)

1) ACCORDING RADAR#2910360 - MATCH P72 SPEAKER AMP TO P92
A) CHANGE C397 AND C402 FROM 0.01UF(132S1045) TO 0.047UF(132S4743)
B) CHANGE R424 AND R431 FROM 27K(113S1274) TO 20.5K(110S2054)
C) CHANGE R428 AND R423 FROM 47K(113S1474) TO 36K(113S1364)

2) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/73
A) ADD OASIS AND MIRAGE OPTIONS TO THE BOM OPTION TABLE AT PAGE 1
B) CHANGE THE BOM OPTION OF J19 FROM NONPRODUCTION TO OMIT AT PAGE 15
C) ADD OMIT BOM OPTION TO R1531 AND R1535 AT PAGE 38.

RAMP (REV: B)

1) ACCORDING RADAR#2917330 - ADD BOOTBANGER BOARD TO P72/P73
A) PAGE 38: CHANGE CPU VCORE SETTING TO 1.2V/1.5V
B) PAGE 14: ADD MIRAGE BOMOPTION TO R268
C) PAGE 15: ADD MIRAGE BOMOPTION TO R274

2) ACCORDING RADAR#2933296 - DIFFERENT CPU ACI P/N AND UPDATE SCH VERSION
A) PAGE 1 : ADD OASIS AND MIRAGE BOMOPTIONS FOR P72/P73
B) PAGE 3 : ADD MIRAGE CPU ACI P/N
C) CHANGE SCHEMATICS VERSION TO B

3) ACCORDING RADAR#2933252 - CHNAGE THE FAN FET TO A STRONGER PART
A) PAGE 35: CHANGE Q1001 FROM 2N7002 TO SI2302DS(372S0027)

RAMP (REV: C)

1) ACCORDING RADAR#2942313 - MORE POST-RAMP SCHEMATIC MODIFICATIONS
A) PAGE 19: STUFF FIREWIRE PROTECTION DIODES DZ8 AND DZ9
B) PAGE 16: CHANGE J2 ACI P/N TO 516S0002
C) UPDATE SCHEMATICS VERSION TO REV.C

2) ACCORDING RADAR#2945017 - F3 BOOTROM
A) PAGE 20: CHANGE BOOTROM ACI P/N TO 341S1036

REVISION HISTORY (2)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.C
SCALE: NONE	SHT 48 OF 53	

*** Signal Cross-Reference ***
--- for the entire design --

+2_5V_ATILPVDD_MAIN	22 38
+2_5V_ENET_MAIN	18
+2_5V_F_A2VDDATI_MAIN	22 38
+2_5V_MAIN	10 11 18 22 35 36 38
+2_5V_SLEEP	38
+2_5V_VCC	35
+3V_AGPVDD_MAIN	9 38
+3V_AMVDD_PANGEA_MAIN	10 11 38
+3V_ATI_OSC_SLEEP	22
+3V_AVDD4_PANGEA_MAIN	6 38
+3V_AVDD5_PANGEA_MAIN	5 38
+3V_AVDD6_PANGEA_MAIN	9 38
+3V_FW_MAIN	19 38
+3V_LCDVDD_SW	22 23 24
+3V_LCDVDD_SW_F	24
+3V_MAIN	3 5 6 7 8 9 10 11 13 14 15 16 18 19 20 21 22 23 24 25 33 34 38
+3V_MAIN_P	33
+3V_PHY_AVDD_MAIN	19 38
+3V_PMU_AVCC	21
+3V_PMU_CHGR	30 31
+3V_SLEEP	4 13 15 20 22 24 26 34 38
+3V_SS_SW_F	22
+3V_VDDA1_PANGEA_MAIN	13 38
+3V_VDDA2_PANGEA_MAIN	13 38
+3V_VDDA3_PANGEA_MAIN	13 38
+3_3V_PMU	21 30 31 32 36 38
+3_3V_REF_PMU	21 38
+5V_BU	36
+5V_BU_RAW	36
+5V_CD_SLEEP	16 34
+5V_HD_SLEEP	16 34
+5V_INV_UF_SW	23
+5V_IO_SLEEP	21 24 27 28 34 38
+5V_MAIN	16 17 19 22 23 25 27 33 34 35 36 38 44
+5V_MAIN_A	26 27
+5V_MAIN_P	27 33
+5V_TP_SLEEP_F	21
+5V_USB_A_F_SW	17
+5V_USB_A_SW	17
+5V_USB_B_F_SW	17
+5V_USB_B_SW	17
+5V_VGADDCPWR_SLEEP_F	24
+5V_VGA_FUSE	24 38
+6V_AUDIO	17 26 28 33 44
+6V_AUDIO_PS	33
+24V_EXT	44
+24V_EXT_GND	44
+28V_INPUT14_SW	30 31
+28V_PWRBUS_SW	31
+ADAPTER	30 32
+ADAPTER_IN	30
+ADAPTER_SW	30 31
+AUD3.3V	26
+AUD5V	26 28
+AVCC_F_SCREAMER	44
+AVCC_SCREAMER	44
+AVDD_CPU_SLEEP	3
+AVDD_CPU_SL_F	3
+DVDD_F_SCREAMER	44
+FW_VP_FUSE_SW	19 38
+PBUS	19 23 31 33 35 37 41
+PBUS_FW_SW	19 38
+VCORE_SLEEP	3 35 38
+VCORE_VCC	35
+VIO_CPUBUS_MAIN	10 11 34 36
+VIO_CPU_SLEEP	3 4 5 13 14 15 34 36
+VP_CONN_SW	19 38
+VP_CPS	19 38
+VP_SW	19 38
1.5V_CPU_VCORE_EN	35
1.5V_CPU_VCORE_PATH	35
1V20_REF	30
1_02V_AUX	31
2_5V_BST	35 41
2_5V_CC	35
2_5V_CSH	35 41
2_5V_CSL	35 41
2_5V_DH	35 41
2_5V_DL	35 41
2_5V_FB	35
2_5V_GND	35
2_5V_LX	35 41
2_5V_REF	35
2_5V_SHDN_L	35
2_5V_SYNC	35
3V_BU_DIV	36
5V_TOL	20
10X_9X_MODE	3 4
786_GND	33
1625_BG	31
1625_BST	31
1625_COMP	31
1625_INTVCC	31
1625_SGND	31
1625_TG	31
1625_VFB	31
1625_VIN	31
AACK*	3 5 14 39
ACOM_IN_RL	44
ACOUT	44
ACOUT_LCL	44
ACOUT_RL	44
AC_ID	21 30
AC_OR_BATT_PWR	32
AC_SW	30

AC_SW_G	30
AC_VOLT	18 30
ADAPTER_+24V	44
ADAPTER_I_REG	31
ADAPTER_PWR_DRAIN	32
ADAPTER_PWR_SW	32
ADAPT_D1	32
ADAPT_D2	32
ADC_POWER	28
AGPAD<31..0>	9 22 42
AGPADSTB<1..0>	9 14 22 42
AGPBUSY*	9 22
AGPCBE<3..0>	9 22 42
AGPDEVSEL*	9 14 23 42
AGPFB0	9 41
AGPFB1	9 41
AGPFB2	9 41
AGPFB3	9 41
AGPFRAME*	9 14 23 42
AGPGNT*	9 14 23
AGPIRDY*	9 14 23 42
AGPPAR	9 22 42
AGPPIPE*	9 14 42
AGPPIPE_IDSEL	22
AGPRBF*	9 14 22 42
AGPREQ*	9 14 23
AGPRST_L	22 23
AGPSBA<7..0>	9 22 42
AGPSBSTB	9 14 22 42
AGPST<2..0>	9 22 42
AGPSTOP*	9 14 22
AGPTRDY*	9 14 23 42
AGPVREF	9 38
AGP_CLK	9 22 42
AGP_FB_IN	9 42
AGP_FB_OUT	9 42
AGP_INTA*	13 14 22
AINLM	26 28
AINLP	26 28
AINRM	26 28
AINRP	26 28
AML	28
AMR	28
AOLO	27
AORO	27
AOUTL	26 27
AOUTR	26 27
ARTRY*	3 5 14 39
ASIC_TCK	10 15
ASIC_TDI	10 15
ASIC_TMS	10 15
ASIC_TRST*	10 15
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ATI_G	22 24
ATI_G_FLTR	24
ATI_HSYNC	22 24
ATI_R	22 24
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ATI_TEST_EN	22
ATI_VSYNC	22 24
ATI_VSYNC_BUF	24
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AUDIO_HP_MUTE_L	13 27
AUDIO_HP_SENSE_L	13 27
AUDIO_HW_RESET_L	13 26
AUD_MODEM	16 28
AUD_MODEM_RET	16 28
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A_COM_IN_RC	44
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BATT_DATA	32
BATT_FET_DRAIN	32
BATT_IN	32
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BATT_IN_1_L	21
BATT_ISNS	31
BATT_LINE	31 32
BATT_NEG	32
BATT_OK	32
BATT_OK_REF	32
BATT_POS	32
BATT_POS_F	32
BATT_RC	32
BATT_RES	32
BATT_V_GOOD	32
BF_FET_G	31
BIASON	22 23
BKLIGHT_PWM	22 23
BKLIGHT_PWM_REG	23
BOOTWP*	20
BUPBAT_POS	36
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BYPASS_R_GATE	32
BYTE	21
CAPLCK_LED	21
CAPSLOCK_LED_L	21
CB_CE1*	12 15 20 43
CB_CE2*	12 15 20 43
CB_IORD*	13 15 20 43
CB_IOWR*	13 15 20 43
CB_IREQ*	13 15 20 43
CB_REG*	13 15 20 43
CB_RESET	13 15 20 43
CB_WAIT*	13 15 20 43
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CHARGE_LED_L	21 30
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CHGND2	17 18 19 37
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CHKSTP_OUT*	3 14 15
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CNVSS	21
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COMMAND_KEY_L	21
COMPVSS	22 24 27
COMP_RC	31
COMP_VID	22 24 27
CONTROL_KEY_L	21
CORO	27
CPUFB1	5 41
CPUFB2	5 41
CPUFB3	5 41
CPUFB4	5 41
CPUFB5	5 41
CPUFB6	5 41
CPUFB7	5 41
CPUFBIN	5 41
CPUFBOUT	5 41
CPUVCORE_PWR_OFF	36
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CPU_BG*	3 5 39
CPU_BR*	3 5 14 39
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CPU_DATA<63..0>	3 5 39
CPU_DBG*	3 5 14 39
CPU_HRESET*	3 15
CPU_HRST	14 15 21
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CPU_INTR*	13
CPU_PLL_00	4
CPU_PLL_01	4
CPU_PLL_10	4
CPU_PLL_CFG<3..0>	3 4
CPU_PLL_STOP_OC	4 21
CPU_STATE_LED_L	21
CPU_STOP_CLK*	5 21
CPU_TCK	3 15
CPU_TDI	3 15
CPU_TDO	3 15
CPU_TMS	3 15
CPU_TRST*	3 15
CPU_VCORE_DISCHRG	35
CPU_VCORE_FB	35
CPU_VCORE_HI_OC	4 21 35
CPU_VCORE_PWR_EN	36
CPU_VCORE_PWR_SEQ	36
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CS1*	6 41
CS2*	6 41
CS3*	6 41
CSOE*	12 15 20 43
CSWE*	12 15 20 43
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DBWO*	3 5 14 39
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DDC_DAT	22 24
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DIG_AUD3.3V	26
DIG_STAR_GND	44
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DQM1*	6 7 8 41
DQM2*	6 7 8 41
DQM3*	6 7 8 41
DQM4*	6 7 8 41
DQM5*	6 7 8 41
DQM6*	6 7 8 41
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ETHPHYRESETL	13 14 18
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FDBK2	26
FET_DRAIN	31
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FIL2_DIG3.3V	26
FILT_MIC_PWR	44
FIL_AUD3.3V	26
FIL_AUD_STAR	26
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FW_C_LKON	10 19
FW_LINK_CNTL0	10 19 42
FW_LINK_CNTL1	10 19 42
FW_LINK_D<7..0>	10 19 42
FW_LINK_GPIO1	10
FW_LINK_LPS	10 19
FW_LINK_LREQ	10 19 42
FW_LINK_SCLK	10 19 42
FW_PHY_PD	13 19
FW_PHY_RST*	19
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FW_R1	19
FW_XI	19 42
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GPIO2	22
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IAC_RC_COMP	31
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IBATT_FB	31
IBATT_RC_COMP	31
IBATT_SERVO	31
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I_CAP	26
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KBD_ID	21
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KEYBOARD_X1_L	21
KEYBOARD_X2_L	21
KEYBOARD_X3_L	21
KEYBOARD_X4_L	21
KEYBOARD_X5_L	21
KEYBOARD_X6_L	21
KEYBOARD_X7_L	21
KEYBOARD_X8_L	21
KEYBOARD_X9_L	21
KEYBOARD_Y0	21
KEYBOARD_Y1	21
KEYBOARD_Y2	21
KEYBOARD_Y3	21
KEYBOARD_Y4	21
KEYBOARD_Y5	21
KEYBOARD_Y6	21
KEYBOARD_Y7	21
KW_AUD_BITCLK	13
KW_AUD_DTI	13 26
KW_AUD_DTO	13
KW_AUD_SYNC	13
KW_EXTINT3	13 14
KW_IIC_CLK	13 15 16 26
KW_IIC_DAT	13 15 16 26
KW_PEND_PROC_INT	13 21
KW_PME*	13
KW_PROC_SLEEP_REQ*	13 21
KW_WATCHDOG*	13 21
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LCD104_ID	22 24
LCD_PWR_EN	22 23
LCD_PWR_EN_L	23
LCD_R_PWREN_L	23
LID_CLOSED_L	21 23
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LVDS0_PLUS	22 24
LVDS1_MINUS	22 24
LVDS1_PLUS	22 24
LVDS2_MINUS	22 24
LVDS2_PLUS	22 24
LVDSCLK_MINUS	22 24
LVDSCLK_PLUS	22 24
LVDS_DDC_CLK	22 24
LVDS_DDC_DATA	22 24
L_SPKR_NEG	27
L_SPKR_NEG_UF	27
L_SPKR_POS	27
M1FH	28
M1FL	28
M1HFILT	28
M2GPIO2	22 24
M2GPIO3	22 24
MA<11..0>	22 23
MAIN_GOOD	21
MAX785_EN	33
MB_IN_STAR_GND	44
MCK	22
MCKIN	22
MCLK<3..0>	7 8 40
MCP*	3 14
MDATA<63..0>	6 7 8 40
MEMWE*	6 41
MIC1HIGH	28
MIC1LOW	28
MIC1S1	28
MIC1SHLD	28
MIC_PWR	44
MII_COL	10 18

MII_CRS	10 18
MII_MDC	10 18
MII_MDIO	10 18
MII_PWR_EN_L	18
MII_RXD<3..0>	10 18
MII_RX_CLK	10 18 43
MII_RX_CLK_F	18 43
MII_RX_DV	10 18
MII_RX_ER	10 18
MII_TPRDN	18 43
MII_TPRDP	18 43
MII_TPTDN	18 43
MII_TPTDP	18 43
MII_TXD0_F	18
MII_TXD1_F	18
MII_TXD2_F	18
MII_TXD3_F	18
MII_TXD<3..0>	10 18
MII_TX_CLK	10 18 43
MII_TX_CLK_F	18 43
MII_TX_EN	10 18
MII_TX_ER	10 18
MII_XTALIN	18
MII_XTALOUT	18
MOBM3G1	22 38
MOBM3G2	22 38
MOBM3G3	22 38
MOBM3V1	22 38
MOBM3V2	22 38
MOBM3V3	22 38
MODEM_RESET*	13 14 16
MODEM_SDOWN	13 14 16 28
M_ADDR<12..0>	6 40
M_BA0	6 41
M_BA1	6 41
NC_ERR1	26
NC_ERR2	26
NC_LP1_5VTAP	26
NC_LP_S	26
NET43	28
NET44	28
NET45	28
NET46	28
NET47	28
NET48	28
NMI_BUTTON_L	21
NUMLCK_LED	21
NUMLOCK_LED_L	21
OOPS	21
OPTION_KEY_L	21
PANAUDCLKOUT	13 26 28
PANGEAMCLK<6..0>	6 7 40
PANGEA_ACLK_REF	5 38
PANGEA_AGP_CLK	9 42
PANGEA_CPU_CLK	5 41
PANGEA_SD_REF	6 38
PANGEA_STOPCPUCLK	5
PANGEA_STOPXTAL*	13
PANGEA_SUSP_ACK*	5 21
PANGEA_SUSP_REQ*	5 21
PANGEA_SUS_REQ_IN*	5
PANGEA_TDO	10 15
PANGEA_TEI	10 38
PAN_AGPBUSY*	9
PAN_AGPSTOP*	9
PAN_QACK*	3 5 14 39
PAN_XIA	13
PAN_XIB	13 43
PAN_XO	13 43
PAN_XT	13 43
PBUS_DIV	30
PBUS_DIV1	31
PBUS_FUSE	31
PCI33EN	22 23
PCISTOP*	9 14 23 42
PHYCNTL0	19 42
PHYCNTL1	19 42
PHYD0	19 42
PHYD1	19 42
PHYD2	19 42
PHYD3	19 42
PHYD4	19 42
PHYD5	19 42
PHYD6	19 42
PHYD7	19 42
PHYLREQ	19 42
PHYSCLK	19 42
PHYTPA0C	19 42
PHYTPA0C_FL	19 42
PHYTPA0T	19 42
PHYTPA0T_FL	19 42
PHYTPB0C	19 42
PHYTPB0C_FL	19 42
PHYTPB0T	19 42
PHYTPB0T_FL	19 42
PHYTPBIAS0	19
PHY_LPS	19
PHY_PD	19
PME*	13 21 25
PMU_10MHZ_XIN	21 43
PMU_10MHZ_XOUT	21 43
PMU_32KHZ_XIN	21 43
PMU_32KHZ_XOUT	21 43
PMU_ACK*	13 21
PMU_AC_DET	21 30
PMU_AC_IN	21 30
PMU_BATT_DET_L	32
PMU_CHGND	37
PMU_CHRG_BATT_0	21 32
PMU_CHRG_EN	30

PMU_IIC_CLK	15 21
PMU_IIC_DAT	15 21
PMU_INT	13 14 21
PMU_MISO	13 21
PMU_MOSI	13 21
PMU_NMI_IRQ*	13 14 21
PMU_NMI_L	21
PMU_REQ*	13 14 21
PMU_RESET_L	21
PMU_SCK	13 21
POS_HRESET	3
POWER1_CHGND	37
POWER2_CHGND	37
POWER_UP_L	21
PS_BST_3V	33
PS_BST_5V	33
PS_CS_3V	33
PS_CS_5V	33
PS_GND	27 30 31 32 33 35 36 37
PS_GND_IN	30
PS_LX_3V	33
PS_LX_5V	33
PS_NGATE_3V	33
PS_NGATE_5V	33
PS_PGATE_3V	33
PS_PGATE_5V	33
PS_REF	33
PS_RSNS_5V	33
PS_SS_3V	33
PS_SS_5V	33
PS_SYNC	33
PS_VL	33
PWR_FET_S2	32
PWR_OR_R	36
PWR_STABLE_DELAY	31
QACK*	3 39
QREQ*	3 5 14 39
R2SET	22
RAGPDEVSEL_L	22 23
RAGPFRAME_L	22 23
RAGPGNT_L	22 23
RAGPIRDY_L	22 23
RAGPREQ_L	22 23
RAGPSTOP_L	22 23
RAGPTRDY_L	22 23
RAM_CKE0	6 7 41
RAM_CKE1	6 7 41
REG2_IN	32 36
RESET_BUTTON_L	21
RESET_KEY_L	21
RING_DETECT*	13 14 16 21
RJ45_4_5	18
RJ45_7_8	18
RJ45_FILTER	18
RJ45_RREF	18
RJ45_RXN	18 43
RJ45_RXP	18 43
RJ45_TREF	18
RJ45_TXN	18 43
RJ45_TXP	18 43
ROMCS*	6
ROMOE*	6 20
ROMRW*	6
ROM_ONBOARD_CS*	20
RSET	22
RUN/SS	30 31
RUN_OK	21
R_SPKR_NEG	27
R_SPKR_NEG_UF	27
R_SPKR_POS	27
SCC_DTRA*	13 16
SCC_GPIOA*	13 14 16
SCC_RTSA*	13 16
SCC_RXDA	13 16
SCC_TRXCA	13 14 16
SCC_TXDA*	13 16
SCREAMER_AGND	44
SCREAMER_DVDD_RET	44
SCREAMER_OUT_CL_F	27
SCREAMER_OUT_CR_F	27
SCREAMER_RET	44
SCR_DATAIN	13 26
SCR_SCLK	13 26 28
SCR_SYNC	13 26 28
SDCAS*	6 41
SDRAS*	6 41
SHIFT_KEY_L	21

REFERENCE DESIGNATOR LOCATION INDEX (1)

DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 49 OF 53	

8	7	6	5	4	3	2	1

TCPUFBOUT	5 41
TEA*	3 5 14 39
TEMP	21
TERM_M_ADDR<12..0>	6 7 8 40
TI_CAP_PLL	26
TI_CS1	26
TI_CS2	26
TI_MOD0	26
TI_MOD1	26
TI_MOD2	26
TI_TI_SD	26
TI_VCOM	26
TRKPAD_RXD	21
TRKPAD_TXD	21
TS*	3 5 14 39
TSIZ<2..0>	3 5 39
TT<4..0>	3 5 39
TXVSSR1	38
T_MEMWE*	6 7 8 41
T_M_BA0	6 7 8 41
T_M_BA1	6 7 8 41
T_PANGEAMCLK<6..6>	7
T_PMU_ACK*	21
T_RAM_CKE0	7 8
T_RAM_CKE0_L	7
T_RAM_CKE0_MLB	7
T_RAM_CKE0_MLB_R	7
T_RAM_CKE0_R	7
T_RAM_CKE1	7 8
T_RAM_CKE1_L	7
T_RAM_CKE1_R	7
T_ROMCS*	6 20
T_ROMOE*	6 20
T_ROMWE*	6 20
T_SDCAS*	6 7 8 41
T_SDO	26
T_SDRAS*	6 7 8 41
T_UIDE_CS0_L	12 16
T_UIDE_CS1_L	12 16
T_UIDE_D<15..0>	12 16
T_UIDE_DA<2..0>	12 16
T_UIDE_DIOR_L	12 16 43
T_UIDE_DIOW_L	12 16 43
T_UIDE_DMAACK_L	12 16
T_UIDE_DMAREQ	12 16
T_UIDE_IORDY_L	16
T_UIDE_IRQ_L	12 16
T_UIDE_RESET_L	12 16 43
UIDE_CS0_L	12 43
UIDE_CS1_L	12 43
UIDE_D<15..0>	12 43
UIDE_DA<2..0>	12 43
UIDE_DIOR_L	12 43
UIDE_DIOW_L	12 43
UIDE_DMAACK_L	12 43
UIDE_DMAREQ	12 43
UIDE_IORDY	12 16 43
UIDE_IRQ	12 43
UIDE_RESET_L	12 43
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UNI_IIC_CLK1	10 15 34
UNI_IIC_DAT	8 10 15 34
UNI_IIC_DAT1	10 15 34
UNI_PU_RESET*	10 21
UNI_RESET*	10 20 21
UPURESET*	10
URESET*	10
USB_DAM	13 17 43
USB_DAM_OUT	17 43
USB_DAM_R	17 43
USB_DAP	13 17 43
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DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6130-C | REV. ACI: C ECS:1.0

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C471	CAP_P	16
C472	CAP	26
C473	CAP	21
C474	CAP	28
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DESCRIPTION:
ENGINEERING RELEASE P72/P73 MLB & SCHEMATIC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE	SHT	OF
NONE	51	53

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C611	CAP_P 27
C612	CAP 21
C613	CAP 21
C614	CAP 19
C615	CAP 19
C616	CAP 19
C617	CAP 19
C618	CAP 7
C619	CAP 7
C620	CAP_P 35
C621	CAP 34
CP1	FINGER_PAD 27
D1	DIODE 35
D2	DIODE 35
D3	DIODE 35
D4	DIODE 19
D5	DIODE 21
D6	DIODE 36
D7	DIODE 36
D8	DIODE 35
D9	DIODE 35
D10	DIODE_SCHOT 32
D11	DIODE 31
D12	DIODE_SCHOT 35
D13	DIODE_SCHOT 19
D16	DIODE 19
D17	DIODE_SCHOT 35
D18	DIODE 30
D19	DIODE_SCHOT 30
D20	DIODE 32
D21	DIODE 32
D22	DIODE 32
D23	DIODE 36
D24	DIODE 33
D25	DIODE 33
D26	DIODE_SCHOT 33
D27	DIODE_SCHOT 33
D28	DIODE_SCHOT 33
D29	DIODE 32
D30	DIODE 31
D31	DIODE_SCHOT 31
D32	DIODE_SCHOT 32
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R433	RES 28
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R435	RES 23
R436	RES 22
R437	RES 22
R438	RES 26
R439	RES 22

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0

SCALE	SHT	OF
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RP27	RPAK4P	12
RP28	RPAK4P	12
S1	DF13_2P_1_25V	21
S2	DF13_2P_1_25H	21
S3	RYC8220_2M	17
S4	DF13_2P_1_25V	21
SH1	SHORT	28
SH2	SHORT	26
T1	XFR_100BT_MDIX	18
T2	XFR_HM00_98734	33
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TP16	TP	22
U1	MAX1636	35
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U3	MAX1792	36
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U12	TRANSCEIVER_BCM5221	18
U13	M16C62_091598	21
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U15	TSB41AB1	19
U16	SDRAM_2MX16X4	7
U17	SDRAM_2MX16X4	7
U18	FEPR_1MX8	20
U19	SDRAM_2MX16X4	7
U20	SDRAM_2MX16X4	7
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U22	MAX1636	35
U23	MK1708	22
U24	MAX785	33
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U27	ADDAC_TLC320AD77C	26
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U30	OPAMP_TS924	28
U31	VREG_LP2951	26
U32	LTC1625	31
U33	VREG_LP2951	26
U34	AMP_LMC7111	31
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U36	MAX4298	27
U37	DS1775	34
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VR2	VREG_LP2951	36
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XW4	JUMPER	33
XW5	JUMPER	33
XW6	JUMPER	31
XW7	SHORT_PAD	35
XW8	JUMPER	35
XW9	SHORT_PAD	35
XW10	JUMPER	27

XW11	SHORT	27
XW12	SHORT_PAD	31
XW13	JUMPER	33
XW14	JUMPER	33
Y1	CRYSTAL	18
Y2	CRYSTAL_4PIN	21
Y3	CRYSTAL	21
Y4	CRYSTAL	19
Y5	CRYSTAL	13
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ZH2	HOLE158	37
ZH3	276D103	37
ZH4	276D103	37
ZH5	276D103	37
ZH6	276D103	37
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ZH8	276D103	37
ZH9	276D103	37
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C609	CAP	27
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R457	RES	23
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REFERENCE DESIGNATOR LOCATION INDEX (5)

DESCRIPTION:
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SIZE	DRAWING NUMBER	REV.
D	051-6130-C	ACI: C ECS:1.0
SCALE: NONE	SHT 53 OF 53	