1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		480849	PRODUCTION RELEASED	01/10/07	?

SCHEM,MLB,PB17"
01/04/2007

PAGE	CONTENTS
1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M10 AGP & CLOCKS
19	M10 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL1162 TMDS TRANSMITTER
21	M10 ANALOG, POWER, GND

PAGE	CONTENTS
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
25	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
26	USB 2.0
27	MARVELL GIGABIT ETHERNET PHY
28	FIREWIRE A/B PHY
29	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
30	PMU (POWER MANAGEMENT UNIT)
31	BATTERY CHARGER AND CONNECTOR
32	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
33	3.3V / 5V SYSTEM POWER SUPPLIES
34	CPU CORE VOLTAGE POWER SUPPLY
35	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
36	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
37	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
38	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
39	FUNCTIONAL TEST POINTS
40	REVISION HISTORY (1 OF 1)
41-42	SIGNAL NAMES
43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		✓
D3_COLD	✓	
GPU_SS	✓	
GPU_SWITCH	✓	
SERIAL_DEBUG		✓
VCORE_OFFSET	✓	
1_8V_MAXBUS	✓	
1_5V_MAXBUS		✓
NEC_USB	✓	
INTREPID_USB		✓
BBANG		✓
NO_BBANG	✓	
ATI_MEMIO_HI	✓	
ATI_MEMIO_LO		✓
SSCG		✓
NO_SSCG	✓	
5V_HD_LOGIC	✓	
3V_HD_LOGIC		✓
EXT_TMDS	✓	
INT_TMDS		✓
NO_4XVCORE	✓	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6582	1	SCHEM,MLB,PB17 INCH	SCH1	
820-1524	1	PCBF,MLB,PB17 INCH	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES °
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

TITLE
SCHEM,MLB,PB17 INCH

DRAWING NUMBER 051-6582 REV. C

SHT 1 OF 44

U44 INTREPID

J18 Ethernet Connector P.28
4 DATA PAIRS
U49 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHz
J22 FW - B Connector P.30
2 DATA PAIRS @ 400MHz
U28 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
100MHZ

J11 OPTICAL DRIVE Connector P.25
EIDE
J13 ULTRA ATA/100 Connector P.25
UIDE

SLEEP LED P.26
LMU
J14 TUBA (SOUND) Connector P.26
I2S
I2C
U48/J2/J4 Fan Circuit P.26
I2C

J25 Battery Connector P.32
SMBUS
3.3V
Power Supply & Charger P.32-36
J19 SUTRO (PWR) Connector P.32

U36 LMU P.24
I2C
U39 PMU P.31
SERIAL
5V

J10 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U26 TI PCI1510 CardBus Controller P.18

J15 TRACKPAD Connector
Keyboard Connector
KB LED LIGHT SENSOR P.24

NOT USED

ETHERNET 10/100/1000 P.14	FIREWIRE 800 MB/S P.14	UATA 100 P.14	EIDE P.14	CARDSLOT P.14	I2S P.15	I2C P.14 P.15

J3 (SHARE WITH BLUETOOTH)
LEFT USB P.25
USB 2.0
J12
RIGHT USB BACKUP BATTERY P.33
NOT USED
USB 2.0
J3 (SHARE WITH LEFT USB)
BlueTooth P.25
NOT USED
J9
Modem Board Connector P.26
INTRPEID
I2C

USB PORT A P.15
USB PORT B P.15
USB PORT C P.15
USB PORT D P.15
USB PORT E P.15
USB PORT F P.15
MAXBUS P.9

SCCA P.15
J5 Serial Debug Connector P.26
VIA/PMU P.15
BOOTROM P.14
U17 BOOT ROM 1M X 8 P.10
PCI 32BITS 33MHZ P.13
U52 USB 2.0 CONTROLLER P.27
PCI BUS
32BITS
33MHZ
3.3V
4X AGP P.13
AGP BUS
1.5V/3.3V
32BITS
66MHZ

U43 ATI M10 64MB P.18-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
J21 AIRPOPT Connector P.25

J8 Inverter Connector P.22
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)
J7 LCD Panel Connector P.22
J17 S-Video Connector P.22
J16 DVI-I Connector P.22

DDR MEMORY P.10
MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14 2:1 DDR MUXES P.11
J20/J23 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.12

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U42 APOLLO CPU (MPC7457) P.5-6
CPU PLL Config P.7
PMU

SYSTEM BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6582 | REV. C
SCALE NONE | SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN
PG 31

INRUSH LIMITER
PG 30

+24V_PBUS

1V20_REF
U21 PG 31
>=13.44V TURNS-ON
<=13.44V SHUTS-OFF

RUN/SS
BUCK REGULATOR (LTC1625)
PG 32
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS (12.8V)

BACKLIGHT INVERTER

+5V_MAIN
VCC
MAIN 2.5V/1.5V DC/DC (MAX1715)
PG 35
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR I/O
MAP31 DDR CORE
DDR POWER
+2.5V_MAIN
1_5V_2_5V_OK
+1.5V_MAIN
INTREPID CORE
AGP I/O

+PBUS

DCDC_EN
SLEEP
MAXBUS SEQUENCING

+5V_MAIN
VCC
SHDN
DC/DC (MAX1717)
PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
CPU_VCORE
(+1.4V/+1.5V)

14V_PBUS

+3V_PMU LDO
PG 32
+BATT
+5V_MAIN
+3V_PMU
+4_6V_BU

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V
MAIN 3V/5V DC/DC (LTC3707)
PG 33
VCC
STBYMD
PGOOD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK
HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND
TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

DCDC_EN_L
AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+5V_MAIN
+PBUS (12.8V)
VCC
EXT_VCC
DC/DC (LTC1778)
PG 20
SHUTDOWN: STOPPED
SLEEP: D3HOT/D3COLD
RUN: RUNNING
TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE
RUN/SS
GPU_VCORE
+1.2V/+1.0V

DCDC_EN
SLEEP
D3_COLD
GPU_VCORE SEQUENCING
1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER
1_5V_2_5V_OK
D3_HOT
DCDC_EN_L
D3_HOT
1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON
HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS
BACKUP BATTERY
CHARGER INPUT & BOOST OUTPUT
PG 32
12.8V CHARGES BACKUP BATTERY
24V IS OUTPUT ONLY FROM BACKUP BATTERY
BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED
+24V_PBUS

DC/DC (LTC3411)
PG 35
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
+1.8V_MAIN
MAXBUS
BROADCOM

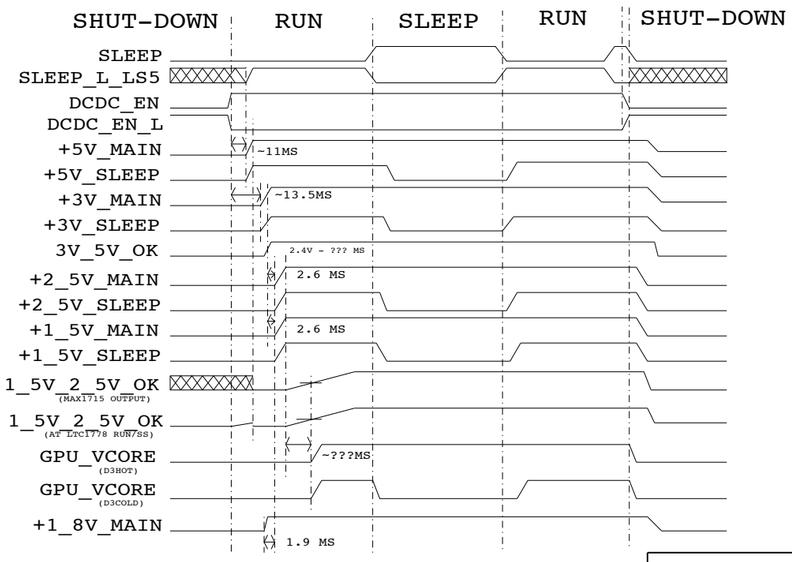
BATTERY CHARGER (MAX1772)
PG 31

+BATT

3S 3P PRISMATIC CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH
PG 31
+PBUS



POWER BLOCK DIAGRAM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE: NONE

SHT 3 OF 44

PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

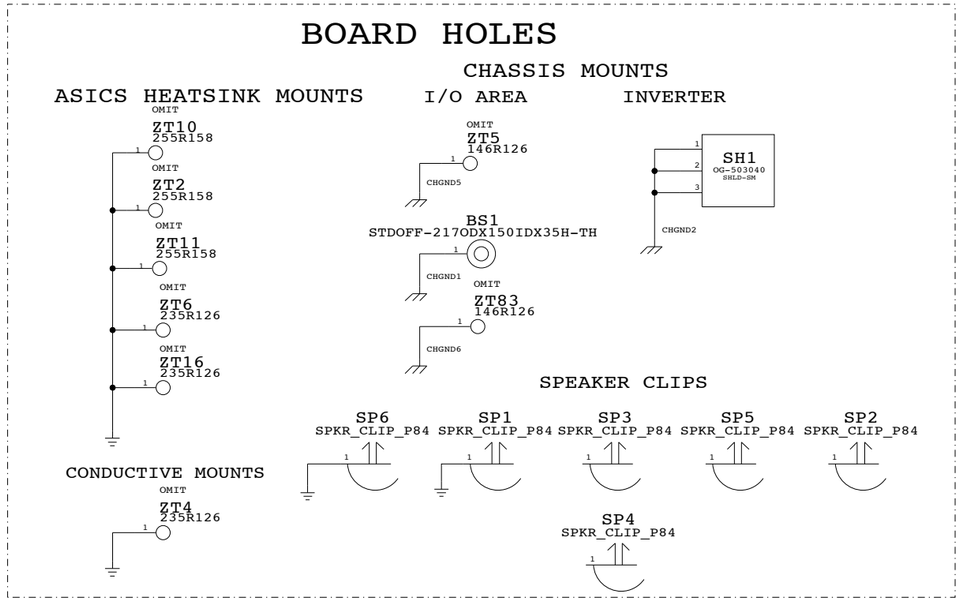
SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

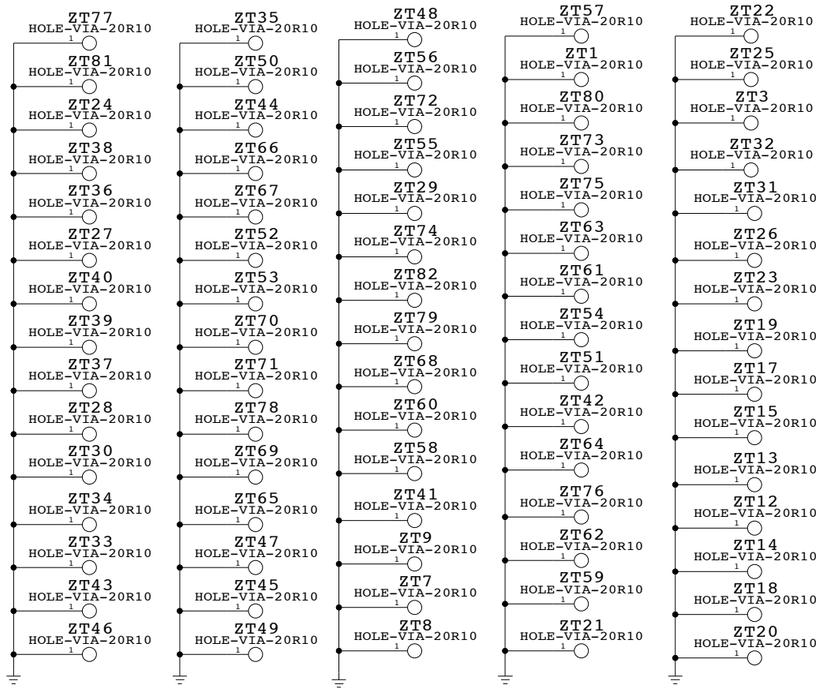
20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



GROUND VIAS



BOARD INFORMATION

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

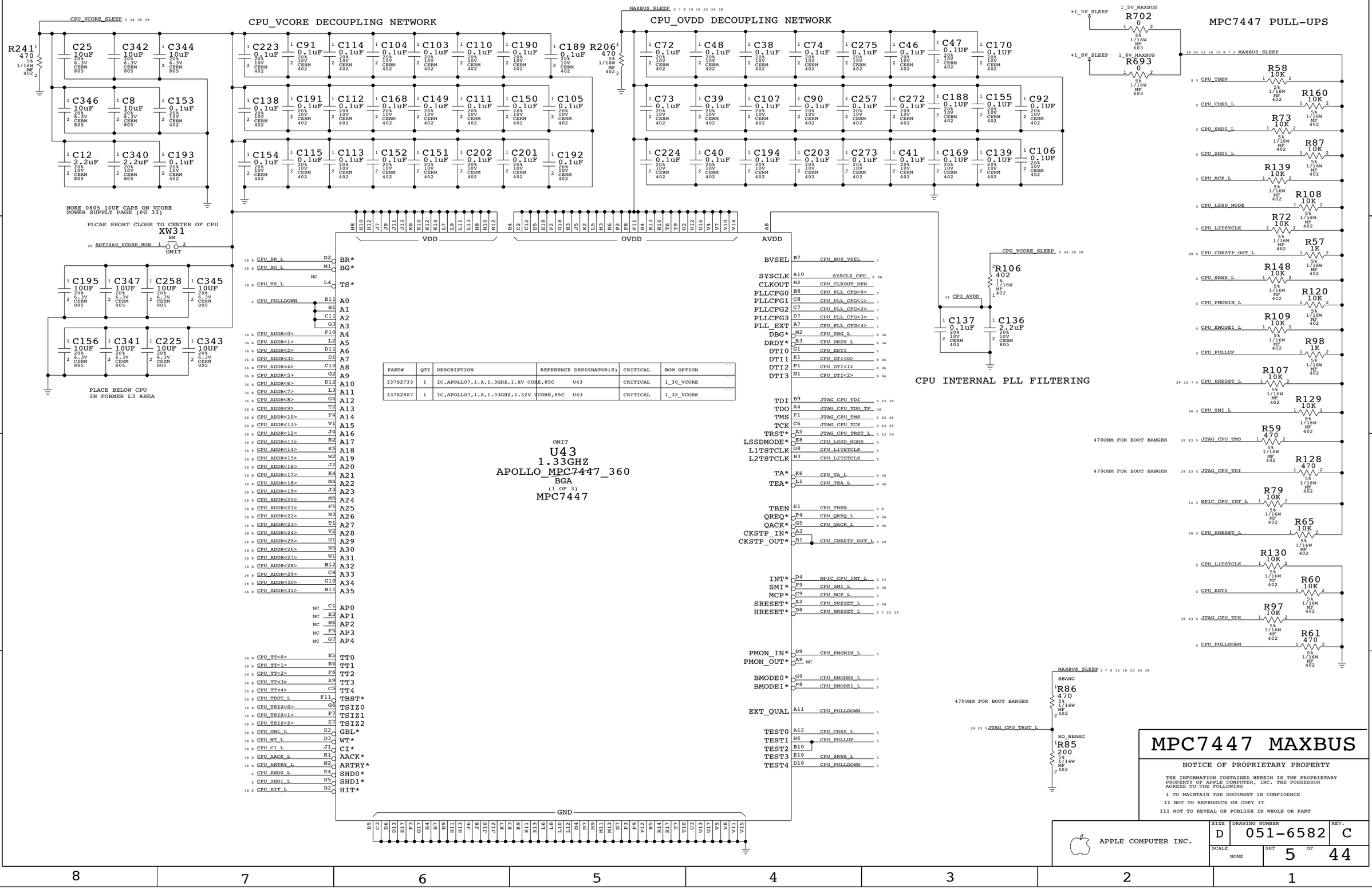
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

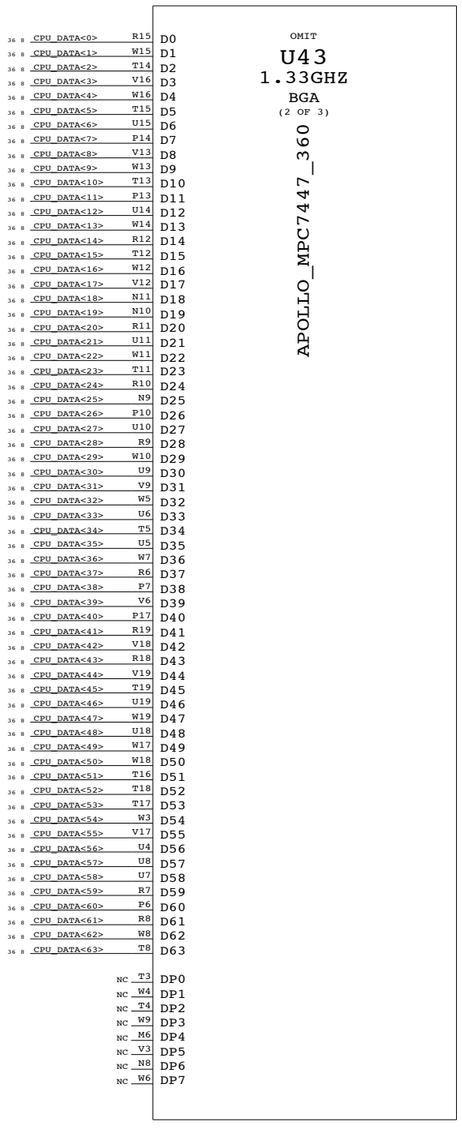
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

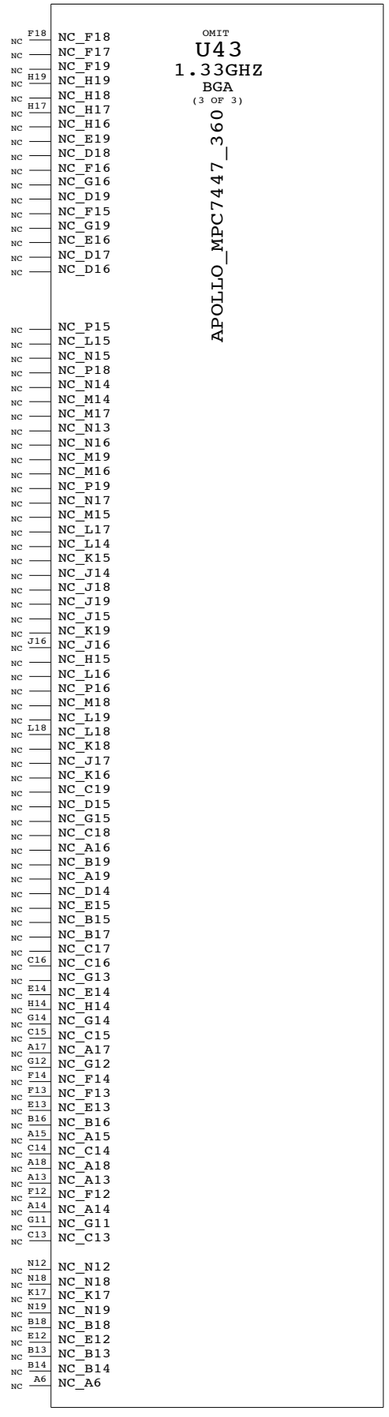
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 4 OF 44	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
33782733	1	IC,APOLLO7,1.X,1.3GHZ,1.XV CORE,85C	U43	CRITICAL	1_30_VCORE
33782807	1	IC,APOLLO7,1.X,1.33GHZ,1.32V VCORE,85C	U43	CRITICAL	1_32_VCORE





BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22

MPC7447/BBANG

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

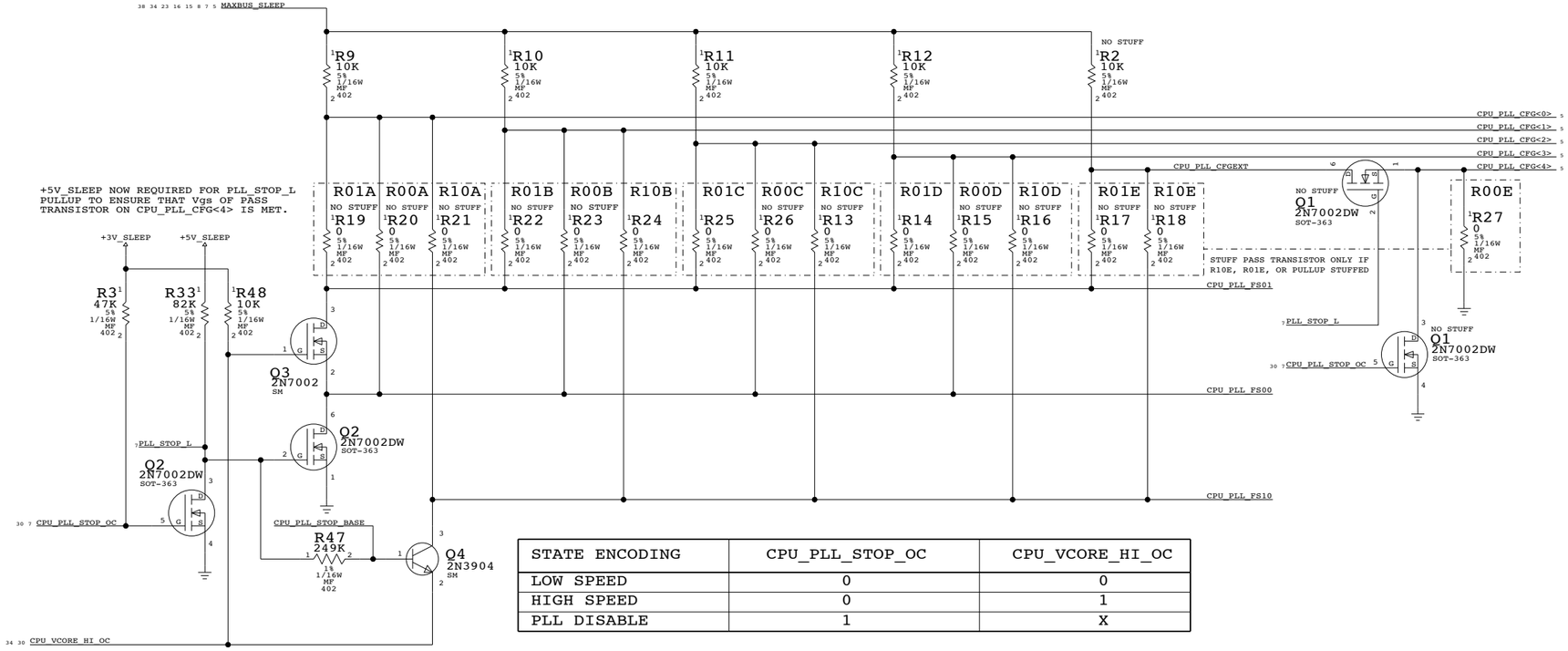
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 6 OF 44	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

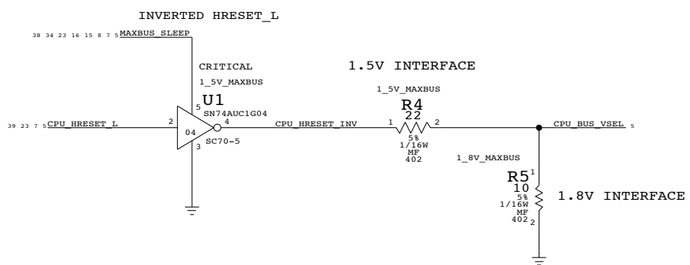
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD	HEX
0.0X	PLL OFF		0 1111	0F
1.0X	PLL BYPASS		0 0011	03
2.0X	333	267	0 0100	04
3.0X	500	400	0 1000	08
4.0X	667	533	0 1010	0A
5.0X	833	667	0 1011	0B
5.5X	917	733	0 1001	09
6.0X	1000	800	0 1101	0D
6.5X	1083	867	0 0101	05
7.0X	1167	933	0 0010	02
7.5X	1250	1000	0 0001	01
8.0X	1333	1067	0 1100	0C
8.5X	1417	1133	0 0110	06
9.0X	1500	1200	1 0111	17
9.5X	1583	1267	0 0111	07
10.0X	1667	1333	1 1010	1A
10.5X	1750	1400	1 1000	18
11.0X	1833	1467	1 1001	19
11.5X	1917	1533	0 0000	00
12.0X	2000	1600	1 1011	1B
12.5X	2083	1667	1 1111	1F
13.0X	2167	1733	1 0101	15
13.5X	2250	1800	0 1110	0E
14.0X	2333	1867	1 1100	1C
15.0X	2500	2000	1 0001	11
16.0X	2667	2133	1 1101	1D
17.0X	2833	2267	1 0000	10
18.0X	3000	2400	1 0010	12
20.0X	3333	2667	1 0011	13
21.0X	3500	2800	1 0100	14
24.0X	4000	3200	1 0110	16
28.0X	4667	3733	1 1110	1E

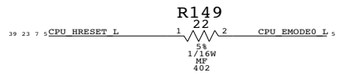
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

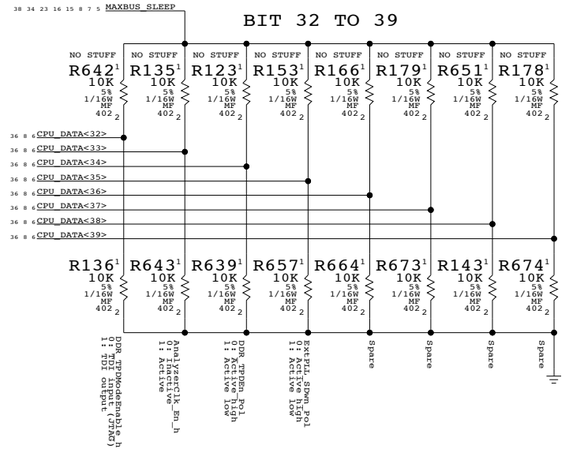
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

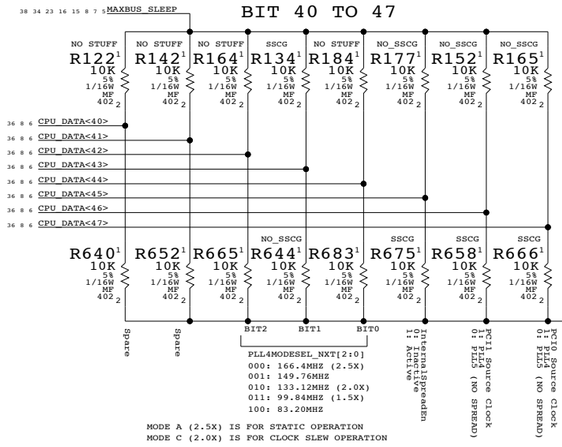
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

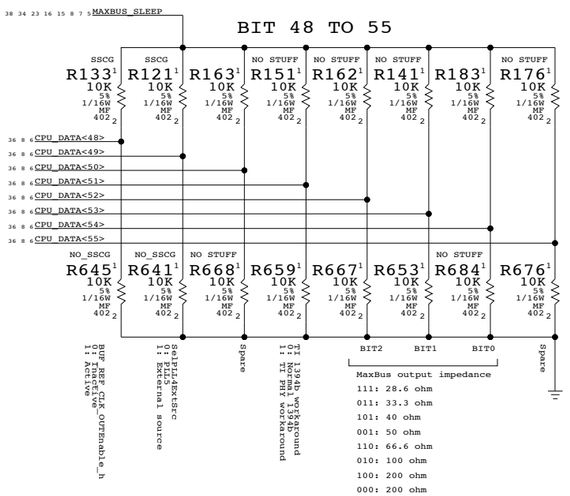
BIT 32 TO 39



BIT 40 TO 47



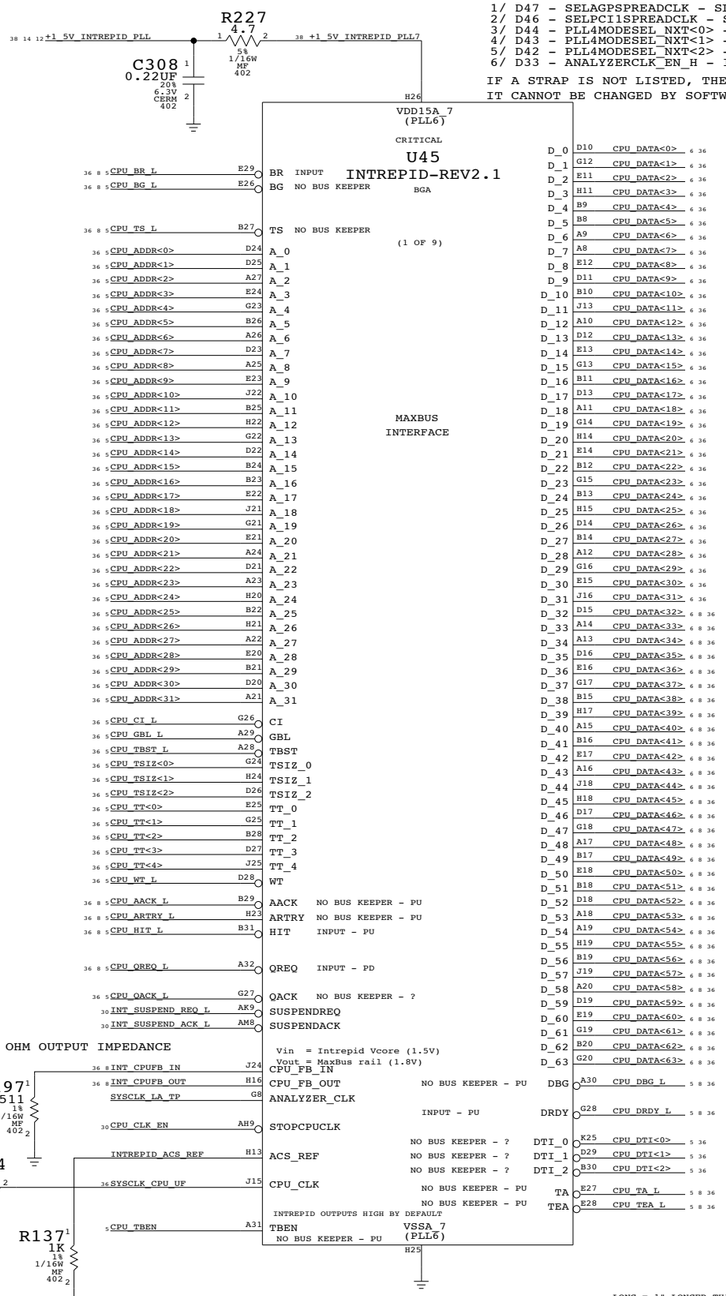
BIT 48 TO 55



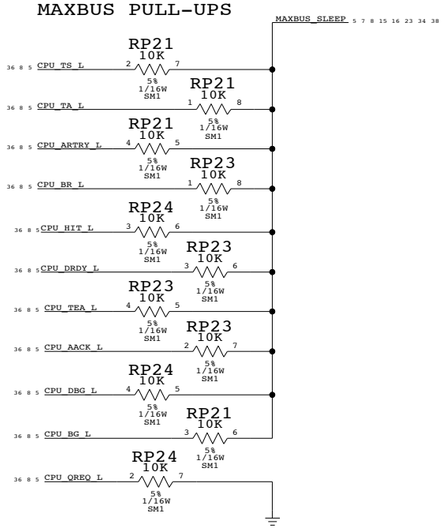
THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

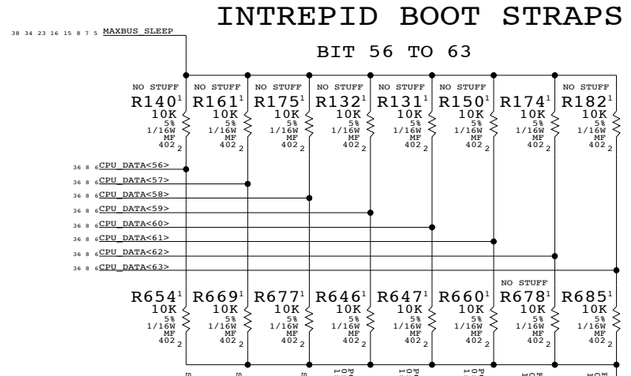


MAXBUS PULL-UPS



INTREPID BOOT STRAPS

BIT 56 TO 63



Intrepid MaxBus

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U45
INTREPID-REV2.1
BGA
(2 OF 9)
CRITICAL

DDR MEMORY INTERFACE

DDR_DATA_0	AK32	MEM_DATA<0>	36 10
DDR_DATA_1	AK33	MEM_DATA<1>	36 10
DDR_DATA_2	AK31	MEM_DATA<2>	36 10
DDR_DATA_3	AK35	MEM_DATA<3>	36 10
DDR_DATA_4	AK36	MEM_DATA<4>	36 10
DDR_DATA_5	AJ32	MEM_DATA<5>	36 10
DDR_DATA_6	AJ35	MEM_DATA<6>	36 10
DDR_DATA_7	AJ36	MEM_DATA<7>	36 10
DDR_DATA_8	AG33	MEM_DATA<8>	36 10
DDR_DATA_9	AG35	MEM_DATA<9>	36 10
DDR_DATA_10	AH35	MEM_DATA<10>	36 10
DDR_DATA_11	AG36	MEM_DATA<11>	36 10
DDR_DATA_12	AH36	MEM_DATA<12>	36 10
DDR_DATA_13	AH32	MEM_DATA<13>	36 10
DDR_DATA_14	AG32	MEM_DATA<14>	36 10
DDR_DATA_15	AG31	MEM_DATA<15>	36 10
DDR_DATA_16	AE32	MEM_DATA<16>	36 10
DDR_DATA_17	AF35	MEM_DATA<17>	36 10
DDR_DATA_18	AF36	MEM_DATA<18>	36 10
DDR_DATA_19	AE36	MEM_DATA<19>	36 10
DDR_DATA_20	AE35	MEM_DATA<20>	36 10
DDR_DATA_21	AE33	MEM_DATA<21>	36 10
DDR_DATA_22	AD36	MEM_DATA<22>	36 10
DDR_DATA_23	AD35	MEM_DATA<23>	36 10
DDR_DATA_24	AA36	MEM_DATA<24>	36 10
DDR_DATA_25	AA35	MEM_DATA<25>	36 10
DDR_DATA_26	AA33	MEM_DATA<26>	36 10
DDR_DATA_27	AB36	MEM_DATA<27>	36 10
DDR_DATA_28	AB35	MEM_DATA<28>	36 10
DDR_DATA_29	AC36	MEM_DATA<29>	36 10
DDR_DATA_30	AA32	MEM_DATA<30>	36 10
DDR_DATA_31	AB33	MEM_DATA<31>	36 10
DDR_DATA_32	V36	MEM_DATA<32>	36 10
DDR_DATA_33	U33	MEM_DATA<33>	36 10
DDR_DATA_34	U32	MEM_DATA<34>	36 10
DDR_DATA_35	V35	MEM_DATA<35>	36 10
DDR_DATA_36	T30	MEM_DATA<36>	36 10
DDR_DATA_37	U36	MEM_DATA<37>	36 10
DDR_DATA_38	U35	MEM_DATA<38>	36 10
DDR_DATA_39	T36	MEM_DATA<39>	36 10
DDR_DATA_40	P33	MEM_DATA<40>	36 10
DDR_DATA_41	R30	MEM_DATA<41>	36 10
DDR_DATA_42	P35	MEM_DATA<42>	36 10
DDR_DATA_43	P36	MEM_DATA<43>	36 10
DDR_DATA_44	R36	MEM_DATA<44>	36 10
DDR_DATA_45	R35	MEM_DATA<45>	36 10
DDR_DATA_46	R33	MEM_DATA<46>	36 10
DDR_DATA_47	R32	MEM_DATA<47>	36 10
DDR_DATA_48	N35	MEM_DATA<48>	36 10
DDR_DATA_49	M36	MEM_DATA<49>	36 10
DDR_DATA_50	L35	MEM_DATA<50>	36 10
DDR_DATA_51	M35	MEM_DATA<51>	36 10
DDR_DATA_52	M33	MEM_DATA<52>	36 10
DDR_DATA_53	L36	MEM_DATA<53>	36 10
DDR_DATA_54	N33	MEM_DATA<54>	36 10
DDR_DATA_55	M30	MEM_DATA<55>	36 10
DDR_DATA_56	J32	MEM_DATA<56>	36 10
DDR_DATA_57	J33	MEM_DATA<57>	36 10
DDR_DATA_58	J35	MEM_DATA<58>	36 10
DDR_DATA_59	K32	MEM_DATA<59>	36 10
DDR_DATA_60	K33	MEM_DATA<60>	36 10
DDR_DATA_61	J36	MEM_DATA<61>	36 10
DDR_DATA_62	K36	MEM_DATA<62>	36 10
DDR_DATA_63	K35	MEM_DATA<63>	36 10

DDR_A_0	H35	MEM_ADDR<0>	9 36
DDR_A_1	G35	MEM_ADDR<1>	9 36
DDR_A_2	G36	MEM_ADDR<2>	9 36
DDR_A_3	F36	MEM_ADDR<3>	9 36
DDR_A_4	F35	MEM_ADDR<4>	9 36
DDR_A_5	E35	MEM_ADDR<5>	9 36
DDR_A_6	E36	MEM_ADDR<6>	9 36
DDR_A_7	G32	MEM_ADDR<7>	9 36
DDR_A_8	D36	MEM_ADDR<8>	9 36
DDR_A_9	H36	MEM_ADDR<9>	9 36
DDR_A_10	G33	MEM_ADDR<10>	9 36
DDR_A_11	H33	MEM_ADDR<11>	9 36
DDR_A_12	D35	MEM_ADDR<12>	9 36
DDR_BA_0	L30	MEM_BA<0>	9 36
DDR_BA_1	M29	MEM_BA<1>	9 36
DDRCS_0	AN34	MEM_CS_L<0>	9 36
DDRCS_1	AN36	MEM_CS_L<1>	9 36
DDRCS_2	AL35	MEM_CS_L<2>	9 36
DDRCS_3	AL33	MEM_CS_L<3>	9 36
DDR_DQS_0	AJ31	MEM_DQS<0>	10 36
DDR_DQS_1	AH31	MEM_DQS<1>	10 36
DDR_DQS_2	AD32	MEM_DQS<2>	10 36
DDR_DQS_3	AB30	MEM_DQS<3>	10 36
DDR_DQS_4	V30	MEM_DQS<4>	10 36
DDR_DQS_5	P32	MEM_DQS<5>	10 36
DDR_DQS_6	N29	MEM_DQS<6>	10 36
DDR_DQS_7	L32	MEM_DQS<7>	10 36
DDR_DM_0	AJ33	MEM_DQM<0>	10 36
DDR_DM_1	AH33	MEM_DQM<1>	10 36
DDR_DM_2	AD33	MEM_DQM<2>	10 36
DDR_DM_3	AC35	MEM_DQM<3>	10 36
DDR_DM_4	T35	MEM_DQM<4>	10 36
DDR_DM_5	T33	MEM_DQM<5>	10 36
DDR_DM_6	N32	MEM_DQM<6>	10 36
DDR_DM_7	L33	MEM_DQM<7>	10 36
DDRRAS	L29	MEM_RAS_L	9 36
DDRCAS	H32	MEM_CAS_L	9 36
DDRWE	E30	MEM_WE_L	9 36
DDRCKE0	AM35	MEM_CKE<0>	9 36
DDRCKE1	AM35	MEM_CKE<1>	9 36
DDRCKE2	AM36	MEM_CKE<2>	9 36
DDRCKE3	AL36	MEM_CKE<3>	9 36
DDR_SELHI_0	AB32	MEM_MUXSEL_H<0>	10 36
DDR_SELHI_1	AE29	MEM_MUXSEL_H<1>	10 36
DDR_SELLO_0	N30	MEM_MUXSEL_L<0>	10 36
DDR_SELLO_1	T32	MEM_MUXSEL_L<1>	10 36
DDR_MCLK_0_P	Y32	SYSCLK_DDRCLK_A0_UF	9 36
DDR_MCLK_0_N	Y33	SYSCLK_DDRCLK_A0_L_UF	9 36
DDR_MCLK_1_P	Y35	SYSCLK_DDRCLK_A1_UF	9 36
DDR_MCLK_1_N	Y36	SYSCLK_DDRCLK_A1_L_UF	9 36
DDR_MCLK_2_P	Y30	INT_DDRCLK2_P_TP	
DDR_MCLK_2_N	W30	INT_DDRCLK2_N_TP	
DDR_MCLK_3_P	W32	SYSCLK_DDRCLK_B0_UF	9 36
DDR_MCLK_3_N	W33	SYSCLK_DDRCLK_B0_L_UF	9 36
DDR_MCLK_4_P	V33	SYSCLK_DDRCLK_B1_UF	9 36
DDR_MCLK_4_N	V32	SYSCLK_DDRCLK_B1_L_UF	9 36
DDR_MCLK_5_P	W35	INT_DDRCLK5_P_TP	
DDR_MCLK_5_N	W36	INT_DDRCLK5_N_TP	
DDR_REF	AA22	INT_MEM_REF_H	38
DDR_VREF_0	Y22	INT_MEM_VREF	9 38
DDR_VREF_1	T22		

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0' & '1' GO TO SLOT A
'2' & '3' GO TO SLOT B

'0'S ARE SAME POLARITY (ACTIVE-LO)
'1'S ARE SAME POLARITY (ACTIVE-HI)

MEM_VREF

38 16 15 10 +2_5V_INTREPID

R198 10K 1% 1/16W MF 402
R191 10K 1% 1/16W MF 402
C245 0.1UF 20% 10V CERM 402
INT_MEM_VREF 9 38

R199 1K 1% 1/16W MF 402

CLOCKS

SYSCLK_DDRCLK_A1_UF	RP33	22	SYSCLK_DDRCLK_A1 11 36
SYSCLK_DDRCLK_A1_L_UF	RP33	22	SYSCLK_DDRCLK_A1_L 11 36
SYSCLK_DDRCLK_A0_UF	RP34	22	SYSCLK_DDRCLK_A0 11 36
SYSCLK_DDRCLK_A0_L_UF	RP34	22	SYSCLK_DDRCLK_A0_L 11 36
SYSCLK_DDRCLK_B1_UF	RP33	22	SYSCLK_DDRCLK_B1 11 36
SYSCLK_DDRCLK_B1_L_UF	RP33	22	SYSCLK_DDRCLK_B1_L 11 36
SYSCLK_DDRCLK_B0_UF	RP34	22	SYSCLK_DDRCLK_B0 11 36
SYSCLK_DDRCLK_B0_L_UF	RP34	22	SYSCLK_DDRCLK_B0_L 11 36

CS

MEM_CS_L<0>	RP36	22	RAM_CS_L<0> 11 36
MEM_CS_L<1>	RP36	22	RAM_CS_L<1> 11 36
MEM_CS_L<2>	RP35	22	RAM_CS_L<2> 11 36
MEM_CS_L<3>	RP35	22	RAM_CS_L<3> 11 36

CKE

MEM_CKE<0>	RP36	22	RAM_CKE<0> 9 11 36
MEM_CKE<1>	RP36	22	RAM_CKE<1> 9 11 36
MEM_CKE<2>	RP35	22	RAM_CKE<2> 9 11 36
MEM_CKE<3>	RP35	22	RAM_CKE<3> 9 11 36

ADDR

MEM_ADDR<0>	RP31	22	RAM_ADDR<0> 11 36
MEM_ADDR<1>	RP25	22	RAM_ADDR<1> 11 36
MEM_ADDR<2>	RP25	22	RAM_ADDR<2> 11 36
MEM_ADDR<3>	RP25	22	RAM_ADDR<3> 11 36
MEM_ADDR<4>	RP30	22	RAM_ADDR<4> 11 36
MEM_ADDR<5>	RP30	22	RAM_ADDR<5> 11 36
MEM_ADDR<6>	RP31	22	RAM_ADDR<6> 11 36
MEM_ADDR<7>	RP30	22	RAM_ADDR<7> 11 36
MEM_ADDR<8>	RP31	22	RAM_ADDR<8> 11 36
MEM_ADDR<9>	RP31	22	RAM_ADDR<9> 11 36
MEM_ADDR<10>	RP26	22	RAM_ADDR<10> 11 36
MEM_ADDR<11>	RP30	22	RAM_ADDR<11> 11 36
MEM_ADDR<12>	RP26	22	RAM_ADDR<12> 11 36

BA

MEM_BA<0>	RP26	22	RAM_BA<0> 11 36
MEM_BA<1>	RP26	22	RAM_BA<1> 11 36

CNTL

MEM_WE_L	RP26	22	RAM_WE_L 11 36
MEM_CAS_L	R250	22	RAM_CAS_L 11 36
MEM_RAS_L	R238	22	RAM_RAS_L 11 36

All RP22 and R250/R238: 5% 1/16W SM1

1MB BOOT ROM

+3V_MAIN

C460 2.2UF 20% 10V CERM 805
C470 0.1UF 20% 10V CERM 402
C479 0.1UF 20% 10V CERM 402

U17
3.3V TSOP
OMIT

VPP 11
VCC 30, 31
GND 23, 39

A0	21	PCI_AD<0>	39 37 26 24 17 12
A1	20	PCI_AD<1>	39 37 26 24 17 12
A2	19	PCI_AD<2>	39 37 26 24 17 12
A3	18	PCI_AD<3>	39 37 26 24 17 12
A4	17	PCI_AD<4>	39 37 26 24 17 12
A5	16	PCI_AD<5>	39 37 26 24 17 12
A6	15	PCI_AD<6>	39 37 26 24 17 12
A7	14	PCI_AD<7>	39 37 26 24 17 12
A8	8	PCI_AD<8>	39 37 26 24 17 12
A9	7	PCI_AD<9>	39 37 26 24 17 12
A10	36	PCI_AD<10>	39 37 26 24 17 12
A11	6	PCI_AD<11>	39 37 26 24 17 12
A12	5	PCI_AD<12>	39 37 26 24 17 12
A13	4	PCI_AD<13>	39 37 26 24 17 12
A14	3	PCI_AD<14>	39 37 26 24 17 12
A15	2	PCI_AD<15>	39 37 26 24 17 12
A16	1	PCI_AD<16>	39 37 26 24 17 12
A17	40	PCI_AD<17>	39 37 26 24 17 12
A18	13	PCI_AD<18>	39 37 26 24 17 12
A19	37	PCI_AD<19>	39 37 26 24 17 12
A20	38	PCI_AD<20>	39 37 26 24 17 12

DQ0	25	PCI_AD<24>	12 17 24 26 37 39
DQ1	26	PCI_AD<25>	12 17 24 26 37 39
DQ2	27	PCI_AD<26>	12 17 24 26 37 39
DQ3	28	PCI_AD<27>	12 17 24 26 37 39
DQ4	32	PCI_AD<28>	12 17 24 26 37 39
DQ5	33	PCI_AD<29>	12 17 24 26 37 39
DQ6	34	PCI_AD<30>	12 17 24 26 37 39
DQ7	35	PCI_AD<31>	12 17 24 26 37 39

CE	22	ROM_ONBOARD_CS_L	39 24 12
OE	24	ROM_OE_L	39 24 12
WE	9	ROM_RW_L	39 24 12
WP	12	ROM_WP_L	
PWD	10	INT_RESET_L	30 13

+3V_MAIN

R338 10K 5% 1/16W MF 402
R386 10K 5% 1/16W MF 402
R357 1K 5% 1/16W MF 402

39 24 12 ROM_CS_L

OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S2103	1	IC, BOOTROM,Q16, SERVICE_BOM	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF

RAM_CKE<0>	R500	10K 5% 1/16W MF 402	36 11 9
RAM_CKE<1>	R439	10K 5% 1/16W MF 402	36 11 9
RAM_CKE<2>	R409	10K 5% 1/16W MF 402	36 11 9
RAM_CKE<3>	R387	10K 5% 1/16W MF 402	36 11 9

INT - DDR/BOOTROM

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

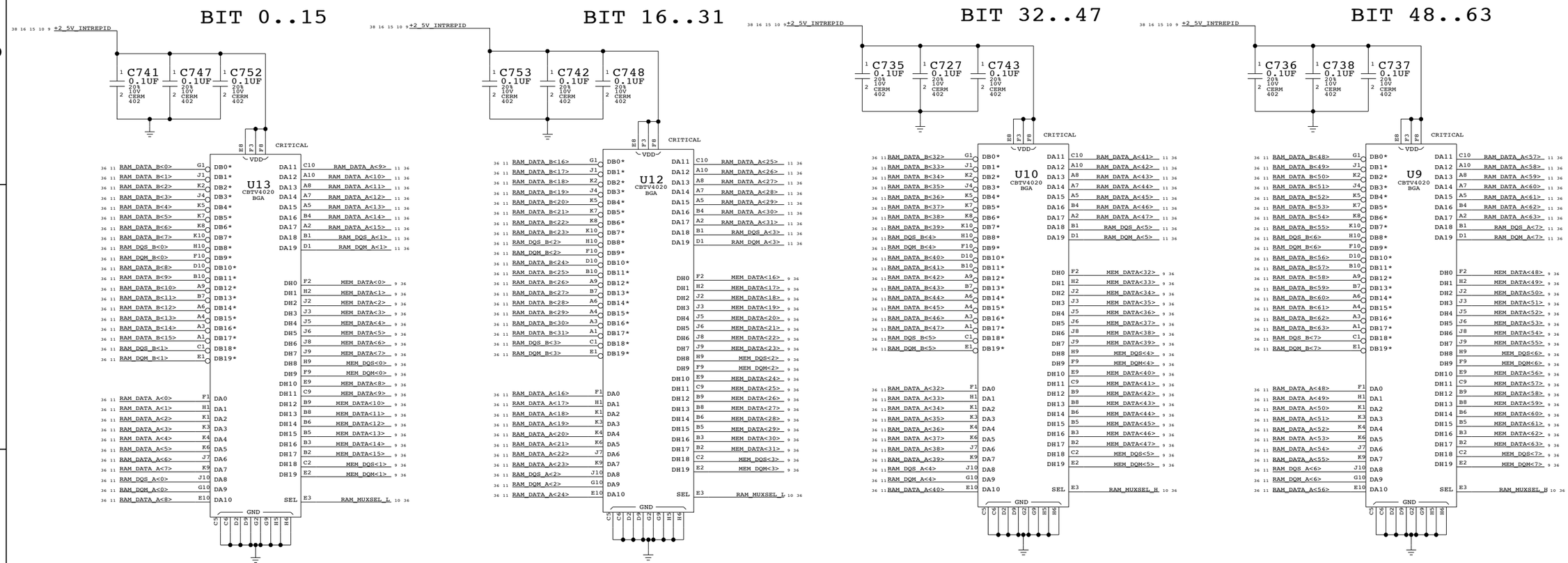
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 9 OF 44	



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

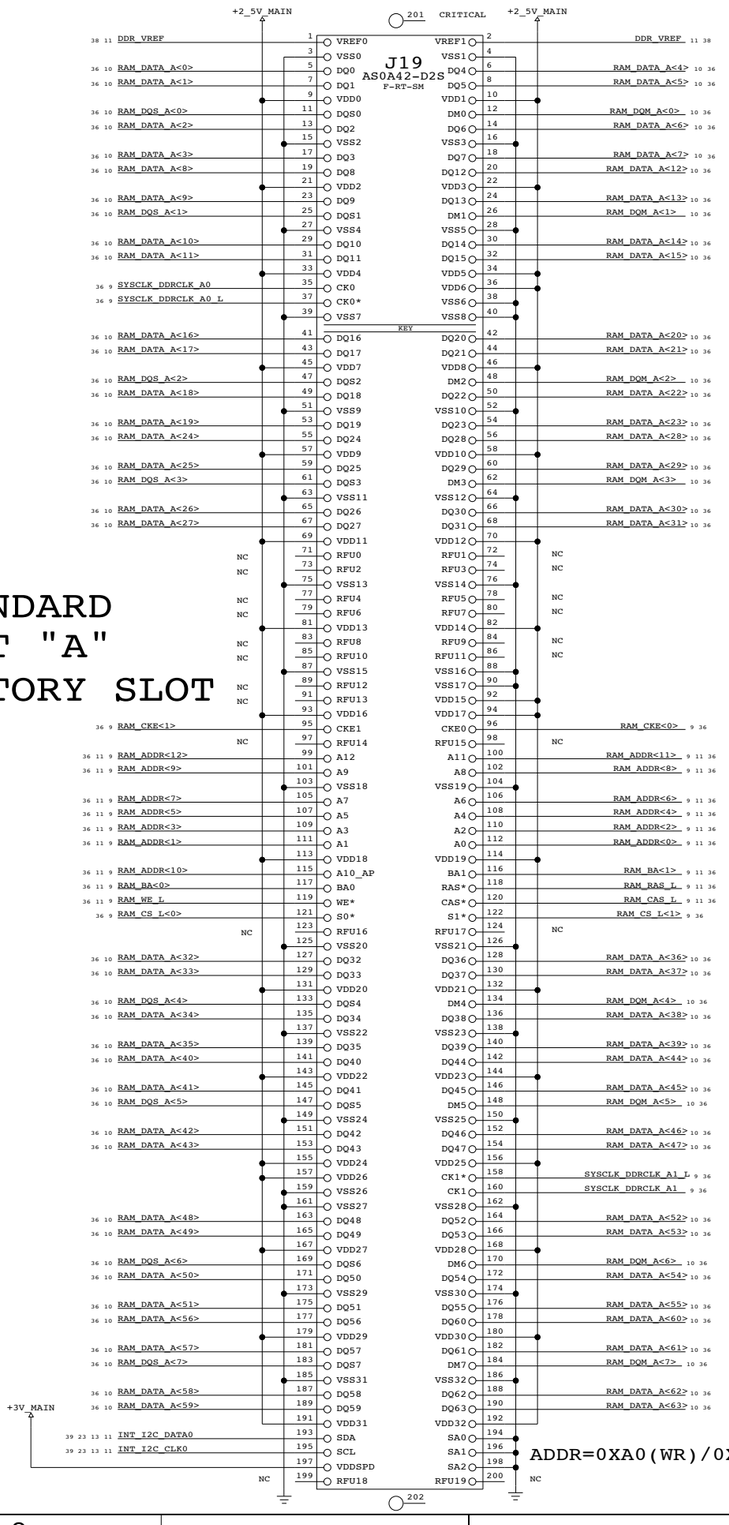
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

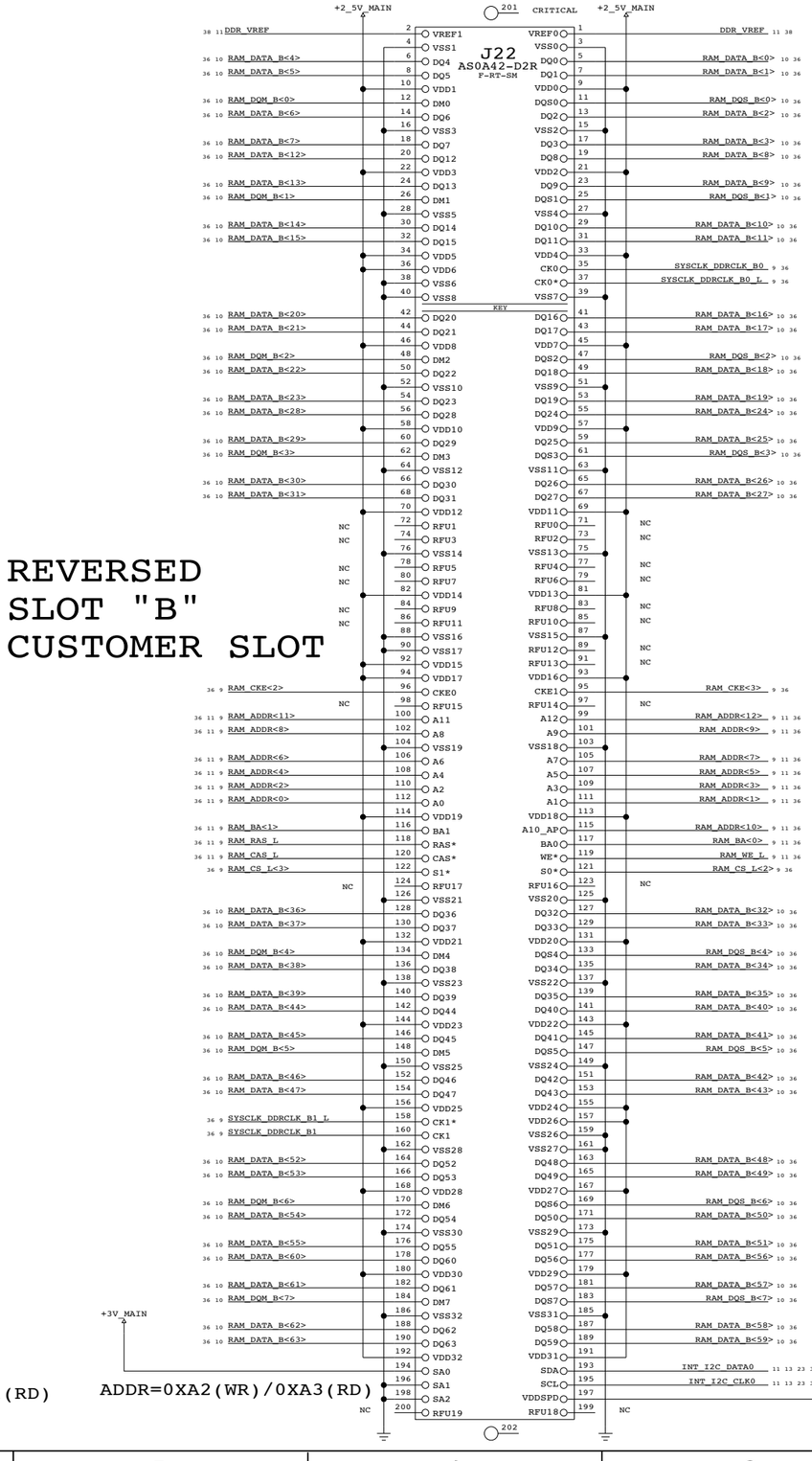
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

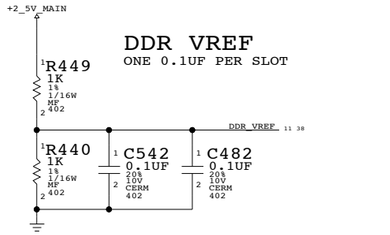
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 10 OF 44	

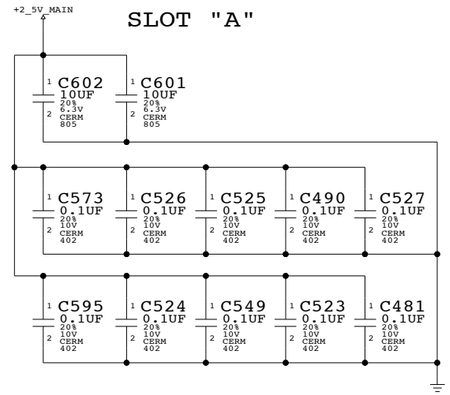


STANDARD
SLOT "A"
FACTORY SLOT



REVERSED
SLOT "B"
CUSTOMER SLOT





DDR SODIMM CONNS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

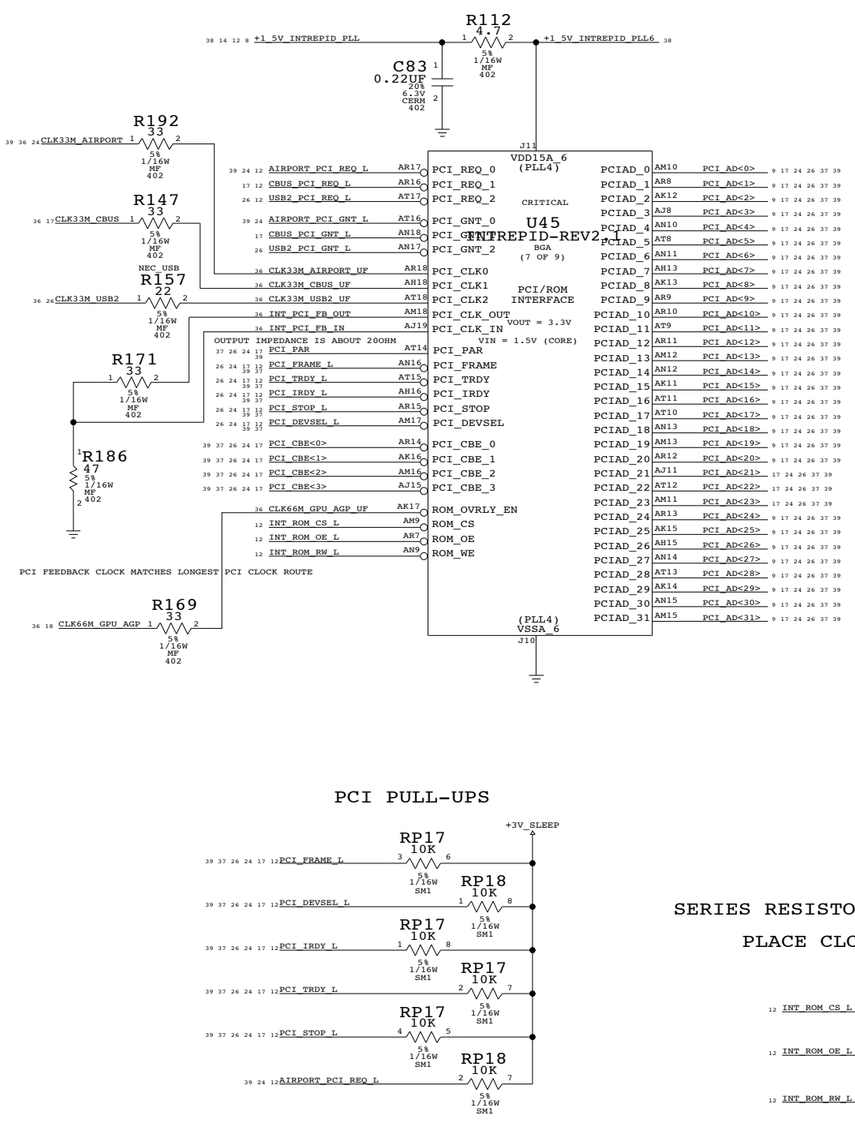
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

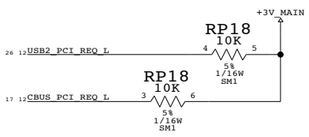
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

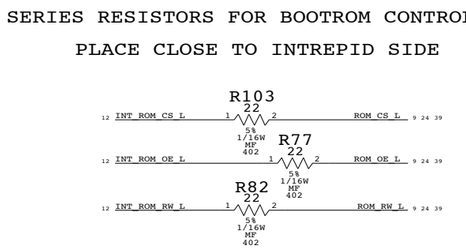
SCALE NONE

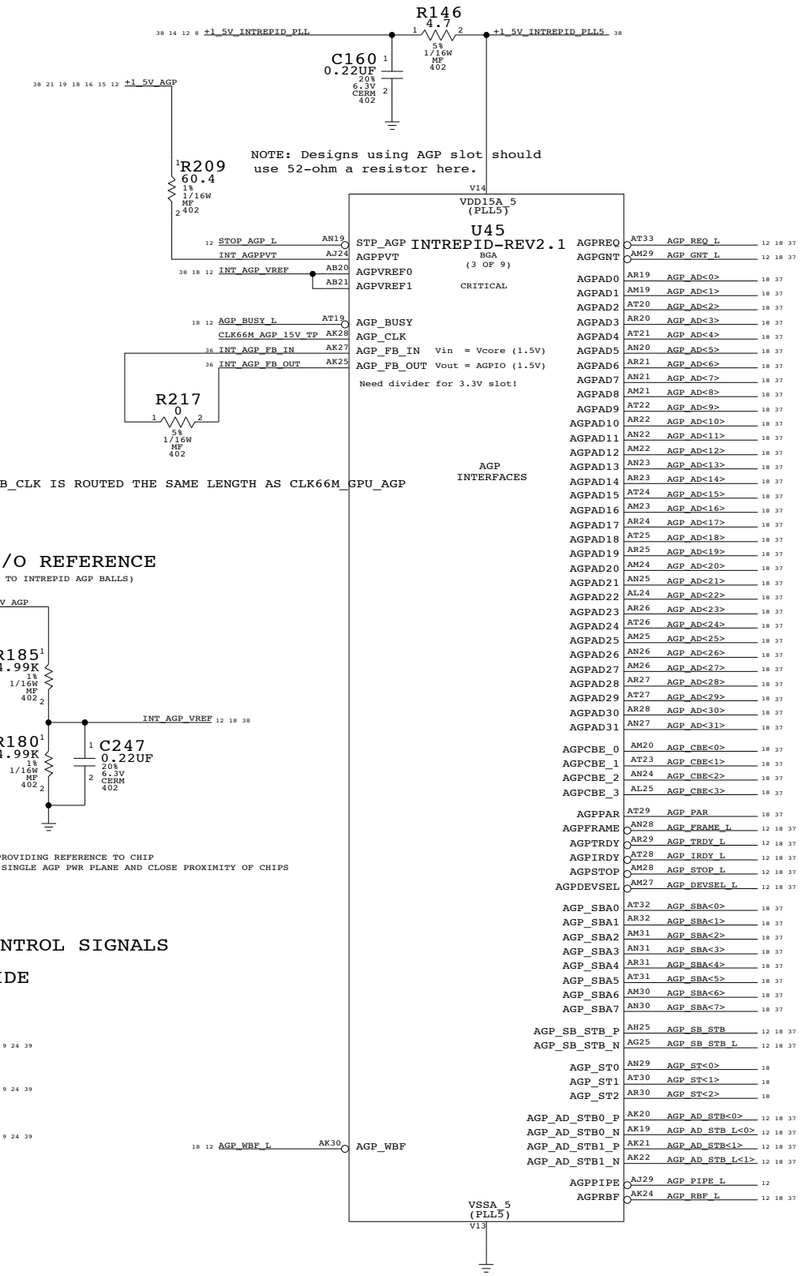
SHT 11 OF 44

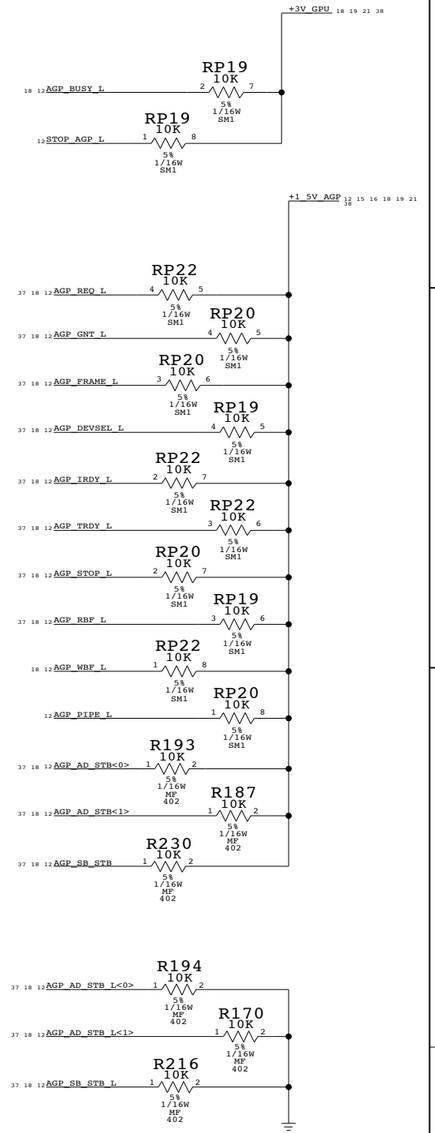




USB2 AND CBUS REQ REMAINS ON
+3V_MAIN BECAUSE THESE CHIPS
ARE POWERED IN SLEEP







NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

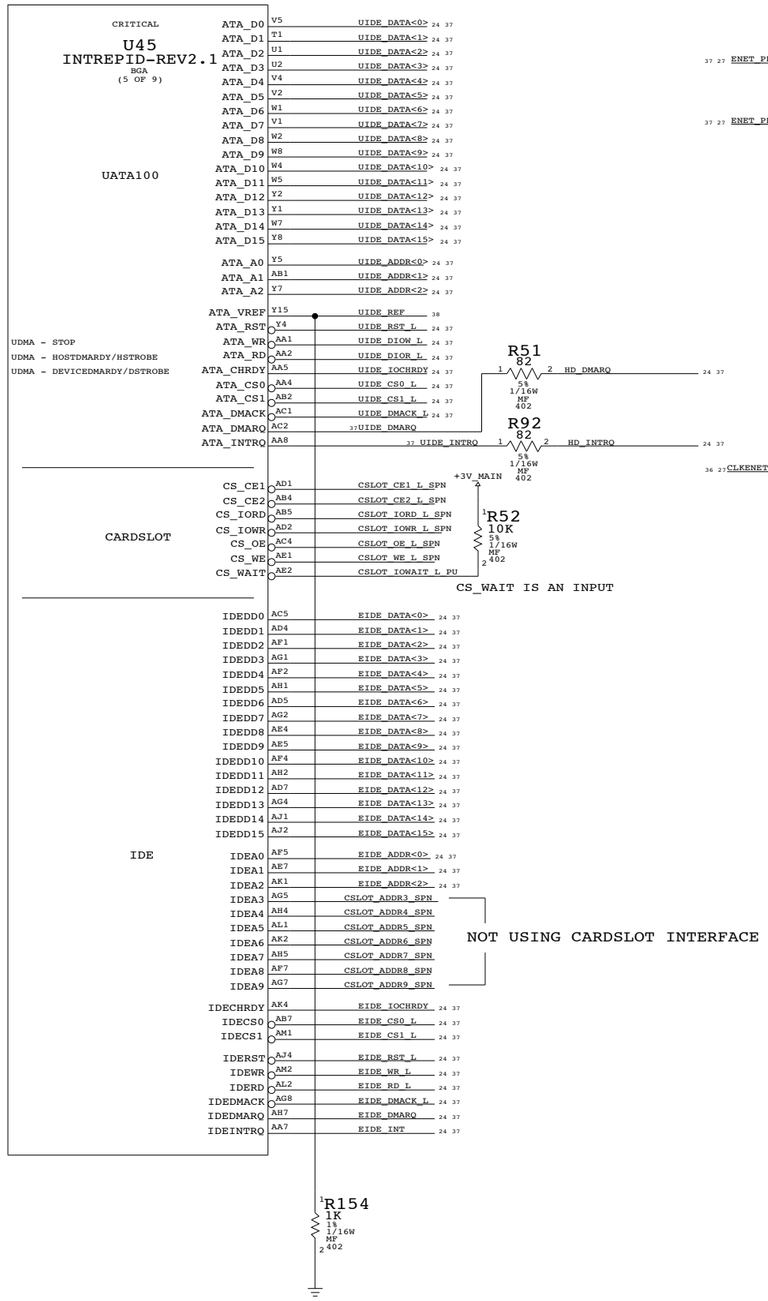
II NOT TO REPRODUCE OR COPY IT

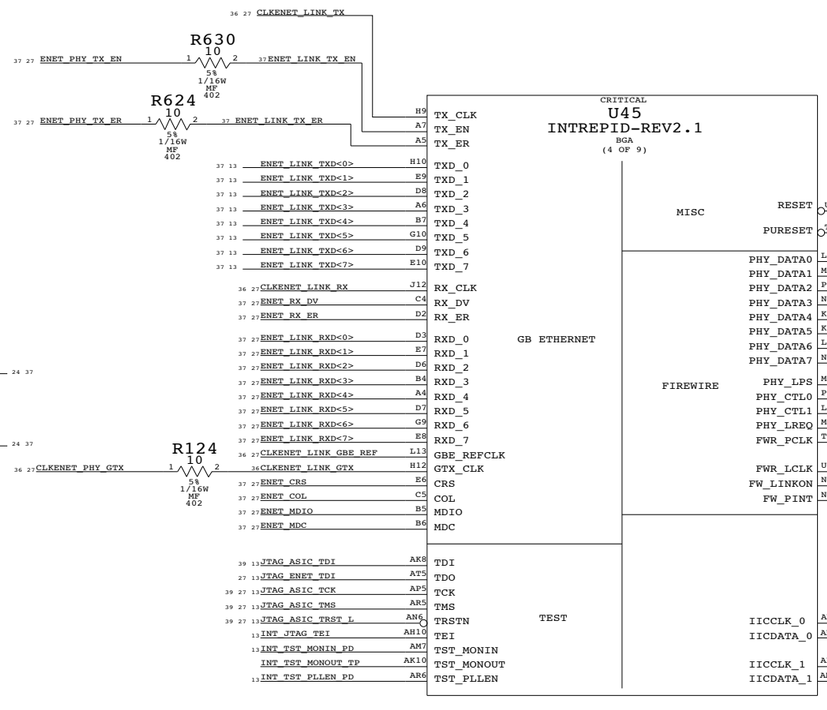
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

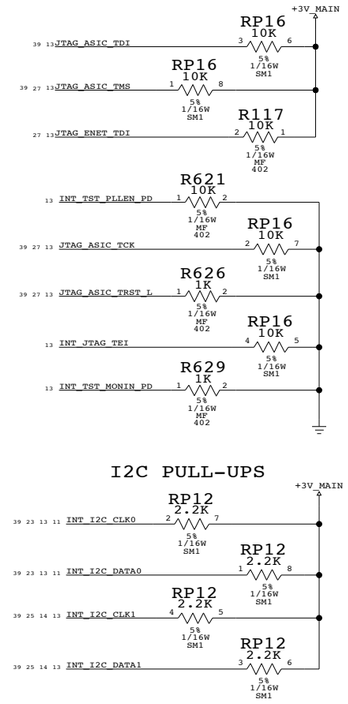
INTREPID AGP/PCI

APPLE COMPUTER INC.

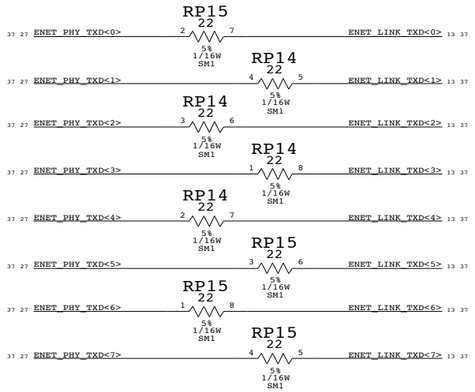
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 12 OF 44	







ENET_TXD SERIES TERMINATION



JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

INT - ENET/FW/UATA EIDE/I2C

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

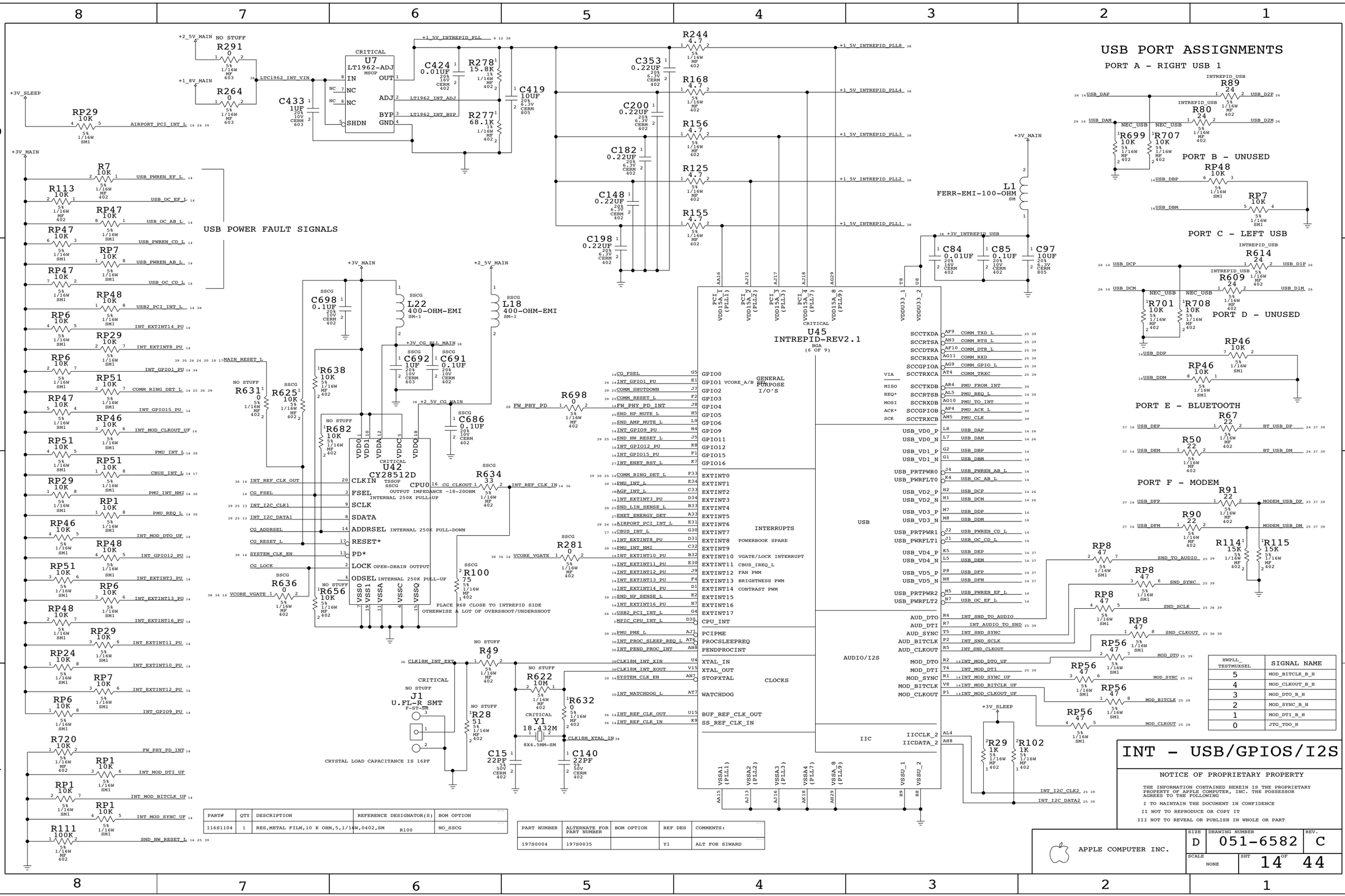
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

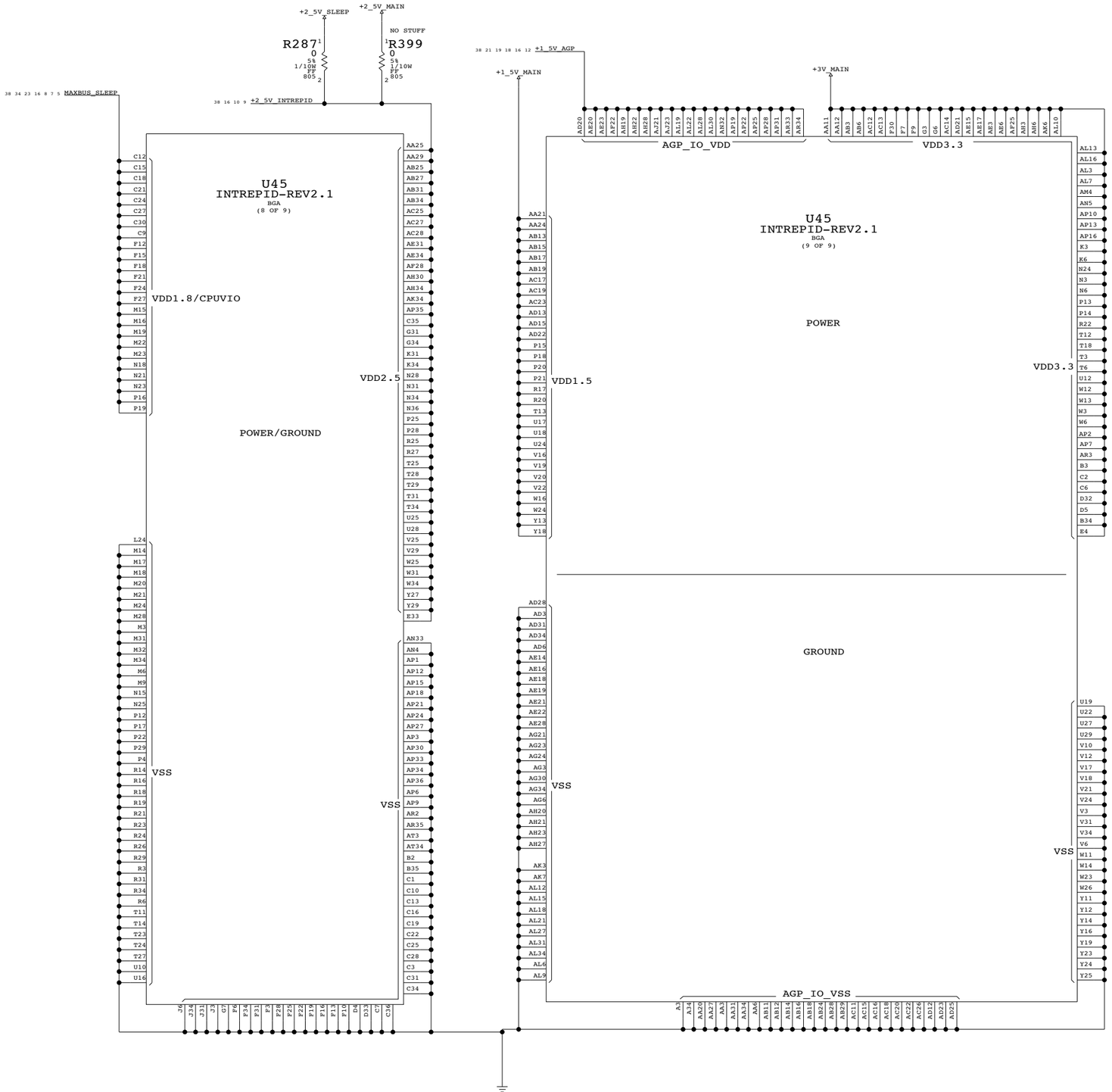
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 13 OF 44	



HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD



Intrepid Power

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 15 OF 44	

38 34 23 15 8 7 5 MAXBUS_SLEEP

INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
32 X 0.22UF (0402)

C204 10uF 20% 6.3V CERM 805 · C348 10uF 20% 6.3V CERM 805 · C236 10uF 20% 6.3V CERM 805 · C196 10uF 20% 6.3V CERM 805

C239 0.22uF 20% 6.3V CERM 402 · C240 0.22uF 20% 6.3V CERM 402 · C350 0.22uF 20% 6.3V CERM 402 · C312 0.22uF 20% 6.3V CERM 402 · C176 0.22uF 20% 6.3V CERM 402 · C288 0.22uF 20% 6.3V CERM 402 · C313 0.22uF 20% 6.3V CERM 402 · C94 0.22uF 20% 6.3V CERM 402 · C286 0.22uF 20% 6.3V CERM 402 · C158 0.22uF 20% 6.3V CERM 402

C174 0.22uF 20% 6.3V CERM 402 · C206 0.22uF 20% 6.3V CERM 402 · C259 0.22uF 20% 6.3V CERM 402 · C237 0.22uF 20% 6.3V CERM 402 · C238 0.22uF 20% 6.3V CERM 402 · C95 0.22uF 20% 6.3V CERM 402 · C117 0.22uF 20% 6.3V CERM 402 · C241 0.22uF 20% 6.3V CERM 402 · C260 0.22uF 20% 6.3V CERM 402 · C314 0.22uF 20% 6.3V CERM 402

C173 0.22uF 20% 6.3V CERM 402 · C171 0.22uF 20% 6.3V CERM 402 · C175 0.22uF 20% 6.3V CERM 402 · C226 0.22uF 20% 6.3V CERM 402 · C172 0.22uF 20% 6.3V CERM 402 · C207 0.22uF 20% 6.3V CERM 402 · C118 0.22uF 20% 6.3V CERM 402 · C287 0.22uF 20% 6.3V CERM 402 · C119 0.22uF 20% 6.3V CERM 402 · C349 0.22uF 20% 6.3V CERM 402

C205 0.22uF 20% 6.3V CERM 402 · C209 0.22uF 20% 6.3V CERM 402

38 21 19 18 15 12 +1_5V_AGP

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
24 X 0.22UF (0402)

C371 10uF 20% 6.3V CERM 805 · C231 10uF 20% 6.3V CERM 805 · C281 10uF 20% 6.3V CERM 805 · C394 10uF 20% 6.3V CERM 805

C356 0.22uF 20% 6.3V CERM 402 · C297 0.22uF 20% 6.3V CERM 402 · C268 0.22uF 20% 6.3V CERM 402 · C217 0.22uF 20% 6.3V CERM 402 · C355 0.22uF 20% 6.3V CERM 402 · C267 0.22uF 20% 6.3V CERM 402 · C250 0.22uF 20% 6.3V CERM 402 · C298 0.22uF 20% 6.3V CERM 402 · C377 0.22uF 20% 6.3V CERM 402 · C216 0.22uF 20% 6.3V CERM 402

C228 0.22uF 20% 6.3V CERM 402 · C230 0.22uF 20% 6.3V CERM 402 · C265 0.22uF 20% 6.3V CERM 402 · C378 0.22uF 20% 6.3V CERM 402 · C357 0.22uF 20% 6.3V CERM 402 · C229 0.22uF 20% 6.3V CERM 402 · C325 0.22uF 20% 6.3V CERM 402 · C393 0.22uF 20% 6.3V CERM 402 · C324 0.22uF 20% 6.3V CERM 402 · C323 0.22uF 20% 6.3V CERM 402

C251 0.22uF 20% 6.3V CERM 402 · C266 0.22uF 20% 6.3V CERM 402 · C249 0.22uF 20% 6.3V CERM 402

38 15 10 9 +2_5V_INTREPID

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
51 X 0.22UF (0402)

C422 10uF 20% 6.3V CERM 805 · C417 10uF 20% 6.3V CERM 805 · C418 10uF 20% 6.3V CERM 805 · C423 10uF 20% 6.3V CERM 805

C407 0.22uF 20% 6.3V CERM 402 · C391 0.22uF 20% 6.3V CERM 402 · C310 0.22uF 20% 6.3V CERM 402 · C317 0.22uF 20% 6.3V CERM 402 · C480 0.22uF 20% 6.3V CERM 402 · C390 0.22uF 20% 6.3V CERM 402 · C370 0.22uF 20% 6.3V CERM 402 · C320 0.22uF 20% 6.3V CERM 402 · C365 0.22uF 20% 6.3V CERM 402 · C366 0.22uF 20% 6.3V CERM 402

C367 0.22uF 20% 6.3V CERM 402 · C292 0.22uF 20% 6.3V CERM 402 · C295 0.22uF 20% 6.3V CERM 402 · C403 0.22uF 20% 6.3V CERM 402 · C291 0.22uF 20% 6.3V CERM 402 · C352 0.22uF 20% 6.3V CERM 402 · C322 0.22uF 20% 6.3V CERM 402 · C392 0.22uF 20% 6.3V CERM 402 · C385 0.22uF 20% 6.3V CERM 402 · C376 0.22uF 20% 6.3V CERM 402

C321 0.22uF 20% 6.3V CERM 402 · C318 0.22uF 20% 6.3V CERM 402 · C399 0.22uF 20% 6.3V CERM 402 · C410 0.22uF 20% 6.3V CERM 402 · C335 0.22uF 20% 6.3V CERM 402 · C369 0.22uF 20% 6.3V CERM 402 · C384 0.22uF 20% 6.3V CERM 402 · C294 0.22uF 20% 6.3V CERM 402 · C406 0.22uF 20% 6.3V CERM 402 · C405 0.22uF 20% 6.3V CERM 402

C404 0.22uF 20% 6.3V CERM 402 · C400 0.22uF 20% 6.3V CERM 402 · C386 0.22uF 20% 6.3V CERM 402 · C289 0.22uF 20% 6.3V CERM 402 · C387 0.22uF 20% 6.3V CERM 402 · C401 0.22uF 20% 6.3V CERM 402 · C354 0.22uF 20% 6.3V CERM 402 · C389 0.22uF 20% 6.3V CERM 402 · C309 0.22uF 20% 6.3V CERM 402 · C398 0.22uF 20% 6.3V CERM 402

C337 0.22uF 20% 6.3V CERM 402 · C290 0.22uF 20% 6.3V CERM 402 · C402 0.22uF 20% 6.3V CERM 402 · C397 0.22uF 20% 6.3V CERM 402 · C368 0.22uF 20% 6.3V CERM 402 · C334 0.22uF 20% 6.3V CERM 402 · C388 0.22uF 20% 6.3V CERM 402 · C293 0.22uF 20% 6.3V CERM 402 · C319 0.22uF 20% 6.3V CERM 402 · C336 0.22uF 20% 6.3V CERM 402

C316 0.22uF 20% 6.3V CERM 402

+1_5V_MAIN

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

C128 10uF 20% 6.3V CERM 805 · C101 10uF 20% 6.3V CERM 805 · C157 10uF 20% 6.3V CERM 805 · C315 10uF 20% 6.3V CERM 805

C147 0.22uF 20% 6.3V CERM 402 · C243 0.22uF 20% 6.3V CERM 402 · C262 0.22uF 20% 6.3V CERM 402 · C242 0.22uF 20% 6.3V CERM 402 · C227 0.22uF 20% 6.3V CERM 402 · C181 0.22uF 20% 6.3V CERM 402 · C142 0.22uF 20% 6.3V CERM 402 · C215 0.22uF 20% 6.3V CERM 402 · C278 0.22uF 20% 6.3V CERM 402 · C264 0.22uF 20% 6.3V CERM 402

C244 0.22uF 20% 6.3V CERM 402 · C212 0.22uF 20% 6.3V CERM 402 · C178 0.22uF 20% 6.3V CERM 402 · C179 0.22uF 20% 6.3V CERM 402 · C177 0.22uF 20% 6.3V CERM 402 · C159 0.22uF 20% 6.3V CERM 402 · C161 0.22uF 20% 6.3V CERM 402 · C162 0.22uF 20% 6.3V CERM 402 · C280 0.22uF 20% 6.3V CERM 402 · C279 0.22uF 20% 6.3V CERM 402

C144 0.22uF 20% 6.3V CERM 402 · C246 0.22uF 20% 6.3V CERM 402 · C211 0.22uF 20% 6.3V CERM 402 · C263 0.22uF 20% 6.3V CERM 402 · C180 0.22uF 20% 6.3V CERM 402 · C213 0.22uF 20% 6.3V CERM 402 · C197 0.22uF 20% 6.3V CERM 402 · C208 0.22uF 20% 6.3V CERM 402 · C214 0.22uF 20% 6.3V CERM 402

+3V_MAIN

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
72 X 0.22UF (0402)

C164 10uF 20% 6.3V CERM 805 · C395 10uF 20% 6.3V CERM 805 · C10 10uF 20% 6.3V CERM 805 · C9 10uF 20% 6.3V CERM 805

C375 0.22uF 20% 6.3V CERM 402 · C351 0.22uF 20% 6.3V CERM 402 · C53 0.22uF 20% 6.3V CERM 402 · C42 0.22uF 20% 6.3V CERM 402 · C21 0.22uF 20% 6.3V CERM 402 · C185 0.22uF 20% 6.3V CERM 402 · C31 0.22uF 20% 6.3V CERM 402 · C143 0.22uF 20% 6.3V CERM 402 · C123 0.22uF 20% 6.3V CERM 402 · C121 0.22uF 20% 6.3V CERM 402

C33 0.22uF 20% 6.3V CERM 402 · C184 0.22uF 20% 6.3V CERM 402 · C43 0.22uF 20% 6.3V CERM 402 · C35 0.22uF 20% 6.3V CERM 402 · C261 0.22uF 20% 6.3V CERM 402 · C60 0.22uF 20% 6.3V CERM 402 · C52 0.22uF 20% 6.3V CERM 402 · C199 0.22uF 20% 6.3V CERM 402 · C57 0.22uF 20% 6.3V CERM 402 · C19 0.22uF 20% 6.3V CERM 402

C16 0.22uF 20% 6.3V CERM 402 · C108 0.22uF 20% 6.3V CERM 402 · C55 0.22uF 20% 6.3V CERM 402 · C32 0.22uF 20% 6.3V CERM 402 · C125 0.22uF 20% 6.3V CERM 402 · C45 0.22uF 20% 6.3V CERM 402 · C76 0.22uF 20% 6.3V CERM 402 · C277 0.22uF 20% 6.3V CERM 402 · C28 0.22uF 20% 6.3V CERM 402 · C26 0.22uF 20% 6.3V CERM 402

C34 0.22uF 20% 6.3V CERM 402 · C23 0.22uF 20% 6.3V CERM 402 · C120 0.22uF 20% 6.3V CERM 402 · C146 0.22uF 20% 6.3V CERM 402 · C141 0.22uF 20% 6.3V CERM 402 · C30 0.22uF 20% 6.3V CERM 402 · C145 0.22uF 20% 6.3V CERM 402 · C96 0.22uF 20% 6.3V CERM 402 · C54 0.22uF 20% 6.3V CERM 402 · C50 0.22uF 20% 6.3V CERM 402

C75 0.22uF 20% 6.3V CERM 402 · C122 0.22uF 20% 6.3V CERM 402 · C51 0.22uF 20% 6.3V CERM 402 · C59 0.22uF 20% 6.3V CERM 402 · C163 0.22uF 20% 6.3V CERM 402 · C126 0.22uF 20% 6.3V CERM 402 · C98 0.22uF 20% 6.3V CERM 402 · C109 0.22uF 20% 6.3V CERM 402 · C56 0.22uF 20% 6.3V CERM 402 · C27 0.22uF 20% 6.3V CERM 402

C296 0.22uF 20% 6.3V CERM 402 · C248 0.22uF 20% 6.3V CERM 402 · C210 0.22uF 20% 6.3V CERM 402 · C58 0.22uF 20% 6.3V CERM 402 · C22 0.22uF 20% 6.3V CERM 402 · C20 0.22uF 20% 6.3V CERM 402 · C61 0.22uF 20% 6.3V CERM 402 · C44 0.22uF 20% 6.3V CERM 402 · C29 0.22uF 20% 6.3V CERM 402 · C24 0.22uF 20% 6.3V CERM 402

C183 0.22uF 20% 6.3V CERM 402 · C18 0.22uF 20% 6.3V CERM 402 · C49 0.22uF 20% 6.3V CERM 402 · C36 0.22uF 20% 6.3V CERM 402 · C17 0.22uF 20% 6.3V CERM 402 · C99 0.22uF 20% 6.3V CERM 402 · C396 0.22uF 20% 6.3V CERM 402 · C124 0.22uF 20% 6.3V CERM 402 · C127 0.22uF 20% 6.3V CERM 402 · C100 0.22uF 20% 6.3V CERM 402

Intrepid Decoupling

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE	SHT	OF
NONE	16	44

PCI1510 PULL-UPS

+3V_MAIN

R757 10K 5% 1/16W MF 402 — CBUS_PCI_PERR_L 17

R756 10K 5% 1/16W MF 402 — CBUS_PCI_SERR_L 17

R753 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU 17

+3V_MAIN

C813 10UF 20% 6.3V CERM 805

C795 0.22UF 20% 6.3V CERM 402

C798 0.22UF 20% 6.3V CERM 402

C790 0.22UF 20% 6.3V CERM 402

C796 0.22UF 20% 6.3V CERM 402

C797 0.22UF 20% 6.3V CERM 402

C791 0.22UF 20% 6.3V CERM 402

R762 10K 5% 1/16W MF 402

+2_5V_MAIN

C789 0.22UF 20% 6.3V CERM 402

A7 C13 D5 E1 M1 N7 N11 — VCC

39 30 26 24 20 18 17 14 MAIN_RESET_L

THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD

R348 47 5% 1/16W MF 402

+3V_MAIN

+5V_MAIN

NO STUFF
R373 10K 5% 1/16W MF 402

U19
TPS2211
SSOI

NC	9		
V_12	5	AVPP	10
V_5_1	6		
V_5_2	3	AVCC0	11
V_3_1	4	AVCC1	12
V_3_2		AVCC2	13
VCCD0	1		
VCCD1	2		
VPPD0	15	CRITICAL	
VPPD1	14		
SHTDWN	16		
GND	7	OC	8 NC

+VPP_CBUS_SW 17 38

+VCC_CBUS_SW 17 38

C773 0.1UF 20% 10V CERM 402

C467 0.1UF 20% 10V CERM 402

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

TPS2211_SHDN_L_PU

CRITICAL
U26
PCI1510GGU
BGA

CLAMP FOR PC-CARD
CLAMP FOR PCI

NC	H10	CLK_48_RSVD/NC	
PCI1510_VR_EN_L	D4	VR_EN*	
	L8	VR_PORT	
39 37 26 24 12 9 PCI_AD<0>	N8	AD0	
39 37 26 24 12 9 PCI_AD<1>	M7	AD1	
39 37 26 24 12 9 PCI_AD<2>	L7	AD2	
39 37 26 24 12 9 PCI_AD<3>	N6	AD3	
39 37 26 24 12 9 PCI_AD<4>	K4	AD4	
39 37 26 24 12 9 PCI_AD<5>	M6	AD5	
39 37 26 24 12 9 PCI_AD<6>	L6	AD6	
39 37 26 24 12 9 PCI_AD<7>	N5	AD7	
39 37 26 24 12 9 PCI_AD<8>	N4	AD8	
39 37 26 24 12 9 PCI_AD<9>	M2	AD9	
39 37 26 24 12 9 PCI_AD<10>	M5	AD10	
39 37 26 24 12 9 PCI_AD<11>	L4	AD11	
39 37 26 24 12 9 PCI_AD<12>	N3	AD12	
39 37 26 24 12 9 PCI_AD<13>	K5	AD13	
39 37 26 24 12 9 PCI_AD<14>	L5	AD14	
39 37 26 24 12 9 PCI_AD<15>	M4	AD15	
39 37 26 24 12 9 PCI_AD<16>	J4	AD16	
39 37 26 24 12 9 PCI_AD<17>	H1	AD17	
39 37 26 24 12 9 PCI_AD<18>	H3	AD18	
PCI_AD<19>	H2	AD19	
39 37 26 24 12 9 PCI_AD<20>	G2	AD20	
39 37 26 24 12 9 PCI_AD<21>	G4	AD21	
39 37 26 24 12 9 PCI_AD<22>	F1	AD22	
39 37 26 24 12 9 PCI_AD<23>	C3	AD23	
39 37 26 24 12 9 PCI_AD<24>	F3	AD24	
39 37 26 24 12 9 PCI_AD<25>	E2	AD25	
39 37 26 24 12 9 PCI_AD<26>	F4	AD26	
39 37 26 24 12 9 PCI_AD<27>	B1	AD27	
39 37 26 24 12 9 PCI_AD<28>	D2	AD28	
39 37 26 24 12 9 PCI_AD<29>	E4	AD29	
39 37 26 24 12 9 PCI_AD<30>	D3	AD30	
39 37 26 24 12 9 PCI_AD<31>	E3	AD31	
39 37 26 24 12 9 PCI_CBE<0>	K6	C/BE0*	
39 37 26 24 12 9 PCI_CBE<1>	M3	C/BE1*	
39 37 26 24 12 9 PCI_CBE<2>	J2	C/BE2*	
39 37 26 24 12 9 PCI_CBE<3>	A1	C/BE3*	
39 37 26 24 12 9 PCI_PAR	N1	PAR	
39 37 26 24 12 9 PCI_IRDY_L	K1	IRDY	
17 CBUS_PCI_SERR_L	L2	SERR	
CBUS_PCI_IDSEL	F2	IDSEL	
17 CBUS_PCI_PERR_L	K3	PERR	
39 37 26 24 12 PCI_FRAME_L	J1	FRAME	
39 37 26 24 12 PCI_STOP_L	L1	STOP	
39 37 26 24 12 PCI_TRDY_L	J3	TRDY	
39 37 26 24 12 PCI_DEVSEL_L	K2	DEVSEL	
CBUS_PCI_RESET_L	G3	PRST	
12 CBUS_PCI_REQ_L	C2	REQ	
12 CBUS_PCI_GNT_L	C1	GNT	
36 12 CLK33M_CBUS	G1	PCLK	
NC	M9	SPKROUT	
NC	M8	RI_OUT/PME	
17 CBUS_SUSPEND_PU	N10	SUSPEND	
14 CBUS_INT_L	K7	MFUNC0	
17 CBUS_MFUNC1_PD	N9	MFUNC1	
17 CBUS_MFUNC2_PD	L9	MFUNC2	
17 CBUS_MFUNC3_PD	K10	MFUNC3	
17 CBUS_MFUNC4_PD	M10	MFUNC4	
17 CBUS_MFUNC5_PD	N12	MFUNC5	
17 CBUS_MFUNC6_PD	L10	MFUNC6	
	L11	GRST	
	B11	VCCCB	
	L3	VCCP	
CBUS_VCCD0_L	N13	VCCD0*	
CBUS_VCCD1_L	L12	VCCD1*	
CBUS_VPPD0	K9	VPPD0	
CBUS_VPPD1	M11	VPPD1	
17 39 CBUS_DET_1_L	L13	CD1*/CCD1*	
17 39 CBUS_DET_2_L	B5	CD2*/CCD2*	
17 CBUS_IORD_L	F12	IORD*/CAD13	
17 CBUS_IOWR_L	C11	IOWR*/CAD15	
17 CBUS_OE_L	G10	OE*/CAD11	
17 CBUS_CE1_L	H13	CE1*/CC/BEO*	
17 CBUS_VS1	B2	VS1*/CVS1	
17 CBUS_VS2	A9	VS2*/CVS2	
17 CBUS_WE_L	D13	WE*/CGNT*	
17 CBUS_READY	A6	RDY/IREQ*/CINT*	
17 CBUS_RESET_L	D8	RESET/CRST*	
17 CBUS_REG_L	A8	REG*/CC/BE3*	
17 CBUS_BVD1_L	C6	BVD1/CSTSCHG/STSCHG*/RI*	
17 CBUS_BVD2_L	D6	BVD2/SPKR*/CAUDIO	
INTEGRATED PULL-UP	A5	WP/IOIS16*/CCLKRUN*	
17 CBUS_CE2_L	G13	CE2/CAD10*	
17 CBUS_INPACK_L	B8	INPACK/CREQ*	
17 CBUS_WAIT_L	B6	WAIT/CSERR*	
17 CBUS_ADDR<0>	C7	A0/CAD26	
17 CBUS_ADDR<1>	D7	A1/CAD25	
17 CBUS_ADDR<2>	B7	A2/CAD24	
17 CBUS_ADDR<3>	D10	A3/CAD23	
17 CBUS_ADDR<4>	B12	A4/CAD22	
17 CBUS_ADDR<5>	C8	A5/CAD21	
17 CBUS_ADDR<6>	C9	A6/CAD20	
17 CBUS_ADDR<7>	A12	A7/CAD18	
17 CBUS_ADDR<8>	E11	A8/CC/BE1*	
17 CBUS_ADDR<9>	F11	A9/CAD14	
17 CBUS_ADDR<10>	G11	A10/CAD9	
17 CBUS_ADDR<11>	G12	A11/CAD12	
17 CBUS_ADDR<12>	D9	A12/CC/BE2*	
17 CBUS_ADDR<13>	E12	A13/CPAR	
17 CBUS_ADDR<14>	D12	A14/CPERR*	
17 CBUS_ADDR<15>	C10	A15/CIRDY*	
17 CBUS_ADDR_16_UF	B13	A16/CCLK	
17 CBUS_ADDR<17>	F10	A17/CAD16	
17 CBUS_ADDR<18>	E13	A18/RSVD	
17 CBUS_ADDR<19>	A13	A19/CBLOCK*	
17 CBUS_ADDR<20>	E10	A20/CSTOP*	
17 CBUS_ADDR<21>	D11	A21/CDEVSEL*	
17 CBUS_ADDR<22>	C12	A22/CTRDY*	
17 CBUS_ADDR<23>	A10	A23/CFRAME*	
17 CBUS_ADDR<24>	B10	A24/CAD17	
17 CBUS_ADDR<25>	B9	A25/CAD19	
17 CBUS_DATA<0>	A4	D0/CAD27	
17 CBUS_DATA<1>	C4	D1/CAD29	
17 CBUS_DATA<2>	A3	D2/RSVD	
17 CBUS_DATA<3>	K11	D3/CAD0	
17 CBUS_DATA<4>	K12	D4/CAD1	
17 CBUS_DATA<5>	J13	D5/CAD3	
17 CBUS_DATA<6>	J10	D6/CAD5	
17 CBUS_DATA<7>	H12	D7/CAD7	
17 CBUS_DATA<8>	C5	D8/CAD28	
17 CBUS_DATA<9>	B4	D9/CAD30	
17 CBUS_DATA<10>	B3	D10/CAD31	
17 CBUS_DATA<11>	M12	D11/CAD2	
17 CBUS_DATA<12>	J11	D12/CAD4	
17 CBUS_DATA<13>	K13	D13/CAD6	
17 CBUS_DATA<14>	J12	D14/RSVD	
17 CBUS_DATA<15>	H11	D15/CAD8	

R750 47 5% 1/16W MF 402 — CBUS_ADDR<16> 17

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C783 2.2UF 20% 10V CERM 805

C776 2.2UF 20% 10V CERM 805

38 17 +VCC_CBUS_SW

R767 22 5% 1/16W MF 402

NO STUFF
R764 47 5% 1/16W MF 402

30 27 26 23 IO_RESET_L

R766 47 5% 1/16W MF 402

39 30 26 24 20 18 17 14 MAIN_RESET_L

RP39 10K 5% 1/32W 25V SM

5	6	CBUS_MFUNC1_PD 17
10	4	CBUS_MFUNC2_PD 17
	7	CBUS_MFUNC3_PD 17
	3	CBUS_MFUNC4_PD 17
	9	CBUS_MFUNC5_PD 17
	8	CBUS_MFUNC6_PD 17
	2	
	1	

GND — A2 A11 D1 F13 H4 K8 M13 N2

PC CARD/CARDBUS CONNECTOR

CRITICAL
J9
QT500806-L111
M-ST-SM1

84 81

	2	1	CBUS_DATA<3> 17
39 17 CBUS_DET_1_L	4	3	CBUS_DATA<4> 17
17 CBUS_DATA<11>	6	5	CBUS_DATA<5> 17
17 CBUS_DATA<12>	8	7	CBUS_DATA<6> 17
17 CBUS_DATA<13>	10	9	
	12	11	CBUS_DATA<7> 17
17 CBUS_DATA<14>	14	13	CBUS_CE1_L 17
17 CBUS_DATA<15>	16	15	CBUS_ADDR<10> 17
17 CBUS_CE2_L	18	17	CBUS_OE_L 17
17 CBUS_VS1	20	19	
	22	21	CBUS_ADDR<11> 17
17 CBUS_IORD_L	24	23	CBUS_ADDR<9> 17
17 CBUS_IOWR_L	26	25	CBUS_ADDR<8> 17
17 CBUS_ADDR<17>	28	27	CBUS_ADDR<13> 17
17 CBUS_ADDR<18>	30	29	
	32	31	CBUS_ADDR<14> 17
17 CBUS_ADDR<19>	34	33	CBUS_WE_L 17
17 CBUS_ADDR<20>	36	35	CBUS_READY 17
17 CBUS_ADDR<21>	38	37	+VCC_CBUS_SW 17 38
38 17 +VCC_CBUS_SW	40	39	
	42	41	+VPP_CBUS_SW 17 38
38 17 +VPP_CBUS_SW	44	43	CBUS_ADDR<16> 17
17 CBUS_ADDR<22>	46	45	CBUS_ADDR<15> 17
17 CBUS_ADDR<23>	48	47	CBUS_ADDR<12> 17
17 CBUS_ADDR<24>	50	49	
	52	51	CBUS_ADDR<7> 17
17 CBUS_ADDR<25>	54	53	CBUS_ADDR<6> 17
17 CBUS_VS2	56	55	CBUS_ADDR<5> 17
17 CBUS_RESET_L	58	57	CBUS_ADDR<4> 17
17 CBUS_WAIT_L	60	59	
	62	61	CBUS_ADDR<3> 17
17 CBUS_INPACK_L	64	63	CBUS_ADDR<2> 17
17 CBUS_REG_L	66	65	CBUS_ADDR<1> 17
17 CBUS_BVD2_L	68	67	CBUS_ADDR<0> 17
17 CBUS_BVD1_L	70	69	
	72	71	CBUS_DATA<0> 17
17 CBUS_DATA<8>	74	73	CBUS_DATA<1> 17
17 CBUS_DATA<9>	76	75	CBUS_DATA<2> 17
17 CBUS_DATA<10>	78	77	CBUS_WP_L 17
39 17 CBUS_DET_2_L	80	79	

83 82

CARDBUS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 17 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0168	1	IC,ATI,M10,NO HEATSPREADER	U44	CRITICAL	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0336	338S0168	?	U44	ALT FOR 338S0168 EOL

OMIT
CRITICAL

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(1 OF 6)

AD31 AD30 AD29 AD28 AD27 AD26 AD25 AD24 AD23 AD22 AD21 AD20 AD19 AD18 AD17 AD16 AD15 AD14 AD13 AD12 AD11 AD10 AD9 AD8 AD7 AD6 AD5 AD4 AD3 AD2 AD1 AD0

CBEB3 CBEB2 CBEB1 CBEB0 PCICLK FRAMEB IRDYB TRDYB STOPB DEVSELB PAR REQB GNTB INTAB RSTB WBF VREFG VREF

AD_STB0 AD_STB1 AD_STBB0 AD_STBB1 AGP_BUSYB AGPREF AGPTEST AGP8X_DETB SUS_STAT ST0 ST1 ST2 SBA7 SBA6 SBA5 SBA4 SBA3 SBA2 SBA1 SBA0 RBFB STP_AGPB SB_STB SB_STBS RSTB_MSK DBI_LO DBI_HI

TEST_YCLK TEST_MLCK MEMTEST PLLTEST MEMVMODE0 MEMVMODE1 D+ D- VSS

R119 47 5% 1/16W MF 402
R127 10K 5% 1/16W MF 402
R159 20K 5% 1/16W MF 402
R172 20K 5% 1/16W MF 402
R158 0 5% 1/16W MF 402
R126 47K 5% 1/16W MF 402
R138 47K 5% 1/16W MF 402
R118 45.3 1% 1/16W MF 402

C62 0.1uF 20% 10V CERM 402
C63 0.01uF 20% 16V CERM 402
(PLACE C1002 CLOSE TO AGPREF PIN)

+3V_GPU +1_5V_AGP +1_8V_GPU +GPU_MEM

AGP_AD_STB<0> AGP_AD_STB<1> AGP_AD_STB_L<0> AGP_AD_STB_L<1> AGP_BUSY_L AGP_ST<0> AGP_ST<1> AGP_ST<2> AGP_SBA<7> AGP_SBA<6> AGP_SBA<5> AGP_SBA<4> AGP_SBA<3> AGP_SBA<2> AGP_SBA<1> AGP_SBA<0> AGP_RBF_L AGP_STP_L AGP_SB_STB AGP_SB_STB_L ATI_RSTB_MSK ATI_DBI_LO_PU ATI_DBI_HI_PU

GPU_AGP_TEST AGP8X_DET_PU INT_AGP_VREF

AGP_ATI_RESET_L AGP_ATI_VREFG AGP_ATI_VREF

GPU_THERM_DP GPU_THERM_DM +GPU_MEM (PULL-UP to GPU_MEM_IO)

ATI_MEMTEST NC

MAIN_RESET_L IS TOGGLED FOR SLEEP
R54 10K 5% 1/16W MF 402
R53 47 5% 1/16W MF 402
MAIN_RESET_L

R43 1K 1% 1/16W MF 402
R44 1K 1% 1/16W MF 402
R45 1K 1% 1/16W MF 402
R46 1K 1% 1/16W MF 402
C11 0.1uF 20% 10V CERM 402
C37 10uF 20% 6.3V CERM 805
PLACE VERF VOLTAGE DIVIDER CLOSE TO ATI M10 VREF PIN

R55 4.7K 5% 1/16W MF 402
R104 4.7K 5% 1/16W MF 402
R70 4.7K 5% 1/16W MF 402
R105 4.7K 5% 1/16W MF 402
ATI_MEMIO_LO ATI_MEMIO_HI

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

OMIT

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(6 OF 6)

M2 P3 A21 B19 M15 N15 P15 R15 T15 T12 T13 T14 W16 V16 U16 T16 R16 R17 R18 R19 U6 AE15 F18 P25

VSS VDDCI

L2
60-OHM-EMI
GPU_VCORE
+GPU_VCORE_VDDCI

C64 0.01uF 20% 16V CERM 402
C67 10uF 20% 6.3V CERM 805
C65 0.01uF 20% 16V CERM 402
C68 0.01uF 20% 16V CERM 402
C66 0.01uF 20% 16V CERM 402
C69 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(2 OF 6)

B26 A26 B25 A25 C22 D21 C21 D20 C20 D22 C23 D23 A27 B27 H2 H1 J2 J1 K4 K3 L4 M3 L3 M4 N2 N1 N4 N3 G30 G28 B30 D26 D16 B15 D11 B10 D5 B3 G3 E1 U1 V3 AB1 AC3 J30 J29 H30 H29 F30 F29 E30 E29 J28 J27 H28 H27 F28 F27 E28 E27 D30 D29 C30 C29 A30 A29 A28 B28 D28 C28 D27 C27 D25 C25 D24 C24 D18 C18 D17 C17 D15 C15 D14 C14 B17

A17 B16 A16 B14 A14 B13 A13 D13 C13 D12 C12 D10 C10 D9 C9 B12 A12 B11 A11 B9 A9 B8 A8 C7 D7 C6 D6 C4 D4 C3 D3 A5 B5 A4 B4 A2 B2 A1 B1 E4 E3 F3 F4 H3 H4 J3 J4 C1 C2 D1 D2 F1 F2 G1 G2 R1 R2 T1 T2 V1 V2 W1 W2 T3 T4 U3 U4 W3 W4 Y3 Y4 V1 Y2 AA1 AA2 AC1 AC2 AD1 AD2 AA3 AA4 AB3 AB4 AD3 AD4 AE3 AE4

OMIT

VSS VSS VSS VSS

27M OSC

(PLACE THE OSCILLATOR AND R189 AND R195 CLOSE TO ATI PIN AJ29)

+3V_SLEEP
L4
FERR-EMI-100-OHM
SM
+3V_ATI_OSC_SLEEP
C77 0.1uF 20% 10V CERM 402
C78 4.7uF 20% 6.3V CERM 805
NO STUFF
R188 100K 5% 1/16W MF 402
CRITICAL
VCC
G2
27.0000M
OSC SM-1
OE OUT GND
ATI_OSC_OE
ATI_CLK27M_OSC
(PLACE R200 CLOSE TO OSC)
GPU_SS
R200 0 1% 1/16W MF 402
ATI_CLK27M_OSC_SS
R189 287 1% 1/16W MF 402
ATI_CLK27M_IN
R195 162 1% 1/16W MF 402

S0=1;S1=M => -1.5% DOWN-SPREAD
SPREAD SPECTRUM SUPPORT

+3V_SLEEP
GPU_SS
L3
FERR-EMI-100-OHM
SM
+3V_ATI_SS
GPU_SS C70 10uF 20% 6.3V CERM 805
GPU_SS C71 0.1uF 20% 10V CERM 402
NO STUFF
R173 0 5% 1/16W MF 402
GPU_SS
R181 0 5% 1/16W MF 402
CRITICAL
VDD
U47
CY25811
SOI
XIN/CLKIN XOUT FRSEL S1 S0 SSCLK VSS
ATI_CLK27M_OSC_SS
ATI_SSCLK_UF
GPU_SS
R201 33 5% 1/16W MF 402
ATI_SSCLK_IN
CY25811_S1
CY25811_S0
NO STUFF
R37 0 5% 1/16W MF 402
NO STUFF
R38 0 5% 1/16W MF 402

M10 AGP INTERFACE

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 18 OF 44	

TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(3 OF 6)

GPU_DVOD<0> AJ5 ZV_LCDDATA0
GPU_DVOD<1> AK5 ZV_LCDDATA1
GPU_DVOD<2> AG6 ZV_LCDDATA2
GPU_DVOD<3> AH6 ZV_LCDDATA3
GPU_DVOD<4> AJ6 ZV_LCDDATA4
GPU_DVOD<5> AK6 ZV_LCDDATA5
GPU_DVOD<6> AG7 ZV_LCDDATA6
GPU_DVOD<7> AH7 ZV_LCDDATA7
GPU_DVOD<8> AJ7 ZV_LCDDATA8
GPU_DVOD<9> AK7 ZV_LCDDATA9
GPU_DVOD<10> AG8 ZV_LCDDATA10
GPU_DVOD<11> AH8 ZV_LCDDATA11
NC AJ8 ZV_LCDDATA12
NC AK8 ZV_LCDDATA13
NC AG9 ZV_LCDDATA14
NC AH9 ZV_LCDDATA15
NC AJ9 ZV_LCDDATA16
NC AK9 ZV_LCDDATA17
NC AG10 ZV_LCDDATA18
NC AH10 ZV_LCDDATA19
ZV_LCDDATA20_PU AJ10 ZV_LCDDATA20
NC AK10 ZV_LCDDATA21
NC AG11 ZV_LCDDATA22
NC AH11 ZV_LCDDATA23

GPU_DVO_VSYNC AJ4 ZV_LCDCNTL0
GPU_DVO_HSYNC AK4 ZV_LCDCNTL1
GPU_DVOD_DE AH5 ZV_LCDCNTL2
GPU_DVO_CLKP AG5 ZV_LCDCNTL3

ATI_AGP_FBSKEW<0> AJ2 GPIO0
ATI_AGP_FBSKEW<1> AK2 GPIO1
ATI_X1CLK_SKEW<0> AK1 GPIO2
ATI_X1CLK_SKEW<1> AH3 GPIO3
ATI_BUS_CFG<0> AH2 GPIO4
ATI_BUS_CFG<1> AJ1 GPIO5
ATI_BUS_CFG<2> AF4 GPIO6
ATI_GPIO7_SPN (NO ICT TEST) AH1 GPIO7
ATI_GPIO8_PD AG3 GPIO8
ATI_GPIO9_SPN (NO ICT TEST) AF3 GPIO9
ATI_GPIO10_SPN (NO ICT TEST) AG2 GPIO10
ATI_GPIO11_SPN (NO ICT TEST) AF2 GPIO11
ATI_GPIO12_SPN (NO ICT TEST) AG1 GPIO12
ATI_GPIO13_SPN (NO ICT TEST) AF1 GPIO13
HPD_PWR_SNS_EN AE2 GPIO14
GPU_VCORE_CNTL_L AE1 GPIO15
ATI_SSCLK_IN M1 GPIO16

ATI_TMDS_DN<0> AJ13 TX0M
ATI_TMDS_DP<0> AK13 TX0P
ATI_TMDS_DN<1> AJ14 TX1M
ATI_TMDS_DP<1> AK14 TX1P
ATI_TMDS_DN<2> AJ15 TX2M
ATI_TMDS_DP<2> AK15 TX2P
ATI_TMDS_CLKN AJ12 TXCM
ATI_TMDS_CLKP AK12 TXCP

ATI_CLK27M_IN AJ29 XTALIN
R229 NC AJ30 XTALOUT
ATI_TESTEN AH24 TESTEN
NC AJ26 SSIN
B24 VSS
B20 VSS
A24 VSS

ROMCSB AE5 NC
R AK28 GPU_R
G AK27 GPU_G
B AK26 GPU_B
VSYNC AG27 ATI_VSYNC
V2SYNC AG25 NC
HSYNC AG26 ATI_HSYNC
H2SYNC AG24 NC
RSET AK25 ATI_RSET
R2SET AJ24 ATI_R2SET
Y_G AK23 GPU_Y
C_R AK24 GPU_C
COMP_B AK22 GPU_COMP
DIGON AE13 FP_PWR_EN
BLON AF13 INV_ON_PWM
HPD1 AF11 GPU_HPD
AUXWIN AJ27 GPU_AUXWIN

DDC1DATA AH28 GPU_DVI_DDC_DATA
DDC1CLK AH27 GPU_DVI_DDC_CLK
DDC2DATA AE12 LVDS_DDC_DATA
DDC2CLK AF12 LVDS_DDC_CLK
DDC3DATA AH26 SI_DDC_DATA
DDC3CLK AH25 SI_DDC_CLK

TXOUT_U0N AH18 LVDS_U0N
TXOUT_U0P AG18 LVDS_U0P
TXOUT_U1N AH19 LVDS_U1N
TXOUT_U1P AG19 LVDS_U1P
TXOUT_U2N AH20 LVDS_U2N
TXOUT_U2P AG20 LVDS_U2P
TXOUT_U3N AH22 LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P AG22 LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN AH21 CLKLVDS_UN
TXCLK_UP AG21 CLKLVDS_UP
TXOUT_L0N AK16 LVDS_L0N
TXOUT_L0P AJ16 LVDS_L0P
TXOUT_L1N AK17 LVDS_L1N
TXOUT_L1P AJ17 LVDS_L1P
TXOUT_L2N AK18 LVDS_L2N
TXOUT_L2P AJ18 LVDS_L2P
TXOUT_L3N AK20 LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P AJ20 LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN AK19 CLKLVDS_LN
TXCLK_LP AJ19 CLKLVDS_LP
SSOUT AJ25 NC
VSS A20
VSS B21

OMIT

EXT_TMDS R228 10K 5% 1/16W MF 402
INT_TMDS R234 10K 5% 1/16W MF 402
R223 NO STUFF 10K 5% 1/16W MF 402
R221 1K 5% 1/16W MF 402
R240 75 1% 1/16W MF 402
R246 75 1% 1/16W MF 402
R249 75 1% 1/16W MF 402
R256 715 1% 1/16W MF 402
R257 499 1% 1/16W MF 402
R245 75 1% 1/16W MF 402
R248 75 1% 1/16W MF 402
R254 75 1% 1/16W MF 402
R711 10K 5% 1/16W MF 402
R247 10K 5% 1/16W MF 402
R253 10K 5% 1/16W MF 402

Q77
SI3446DV
TSOP

L24
FERR-220-OHM
0805

GPU_CORE_OK
+GPU_VDD15_UF
C166 1000pF 10% 25V X7R 402

+1_5V_GPU_VDD15 (500mA)

C222 0.01uF 20% 16V CERM 402
C256 0.01uF 20% 16V CERM 402
C299 0.01uF 20% 16V CERM 402
C305 0.01uF 20% 16V CERM 402
C328 10uF 20% 6.3V CERM 805
C232 0.01uF 20% 16V CERM 402
C269 0.01uF 20% 16V CERM 402
C300 0.01uF 20% 16V CERM 402
C306 0.01uF 20% 16V CERM 402

U44
RAGE_MOBILITY
M10-CSP64
64MB
BGA
(5 OF 6)

F12 L6 T6 AB6 F17 G25 R25 AB25 VDD15
AJ3 AF25 AG4 AH4 AF5 F6 G6 H6 P6 AD26 V6 W6 AC6 AD6 AE6 F7 F10 AE10 F11 AE11 F13 F14 AE14 AF14 W26 AF15 AE17 AC25 AE18 F23 F24 AE24 P25 M25 N25 W25 V25 VDDC
OMIT
G7 G8 G9 G10 G11 G12 G13 G14 G15 G16 G17 G18 G19 G20 G21 G22 G23 G24 H7 H8 H23 H24 J7 J24 K7 K24 L7 L24 M7 M24 N7 N24 P7 P24 R7 R24 T7 T24 U7 U24 V7 V24 W7 W24 Y7 Y24 AA7 AA24 AB7 AB24 AC7 AC8 AC23 AC24 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 VSS

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

C167 10uF 20% 6.3V CERM 805
C219 10uF 20% 6.3V CERM 805
C252 0.22uF 20% 6.3V CERM 402
C270 0.22uF 20% 6.3V CERM 402
C301 0.22uF 20% 6.3V CERM 402
C307 0.22uF 20% 6.3V CERM 402
C329 0.22uF 20% 6.3V CERM 402
C332 0.22uF 20% 6.3V CERM 402
C186 0.22uF 20% 6.3V CERM 402
C220 0.22uF 20% 6.3V CERM 402
C253 0.22uF 20% 6.3V CERM 402
C271 0.22uF 20% 6.3V CERM 402
C302 0.22uF 20% 6.3V CERM 402
C311 0.22uF 20% 6.3V CERM 402
C330 0.22uF 20% 6.3V CERM 402
C333 0.22uF 20% 6.3V CERM 402
C187 0.22uF 20% 6.3V CERM 402
C221 0.22uF 20% 6.3V CERM 402
C254 0.22uF 20% 6.3V CERM 402
C282 0.22uF 20% 6.3V CERM 402
C303 0.22uF 20% 6.3V CERM 402
C326 0.22uF 20% 6.3V CERM 402
C331 0.22uF 20% 6.3V CERM 402
C338 0.22uF 20% 6.3V CERM 402

M10 Power Shut down Sequencing

XW21 SM
XW24 SM
XW20 SM
XW22 SM
XW23 SM
DP6 BAS16TW SOT-363

R258 10K 5% 1/16W MF 402
R260 10K 5% 1/16W MF 402
R262 10K 5% 1/16W MF 402 NO STUFF
R265 10K 5% 1/16W MF 402 NO STUFF
R269 10K 5% 1/16W MF 402 NO STUFF
R271 10K 5% 1/16W MF 402 NO STUFF
R273 10K 5% 1/16W MF 402 NO STUFF
R259 10K 5% 1/16W MF 402 NO STUFF
R261 10K 5% 1/16W MF 402 NO STUFF
R263 10K 5% 1/16W MF 402 NO STUFF
R266 10K 5% 1/16W MF 402 NO STUFF
R270 10K 5% 1/16W MF 402 NO STUFF
R272 10K 5% 1/16W MF 402 NO STUFF
R274 10K 5% 1/16W MF 402 NO STUFF

(GPIO0) ATI_AGP_FBSKEW<0>
(GPIO1) ATI_AGP_FBSKEW<1>
(GPIO2) ATI_X1CLK_SKEW<0>
(GPIO3) ATI_X1CLK_SKEW<1>
(GPIO4) ATI_BUS_CFG<0>
(GPIO5) ATI_BUS_CFG<1>
(GPIO6) ATI_BUS_CFG<2>

GPU VCORE SUPPLY

R389 1M 5% 1/16W MF 402
R430 1 5% 1/16W MF 603
R339 576K 1% 1/16W MF 402

C762 4.7UF 20% 6.3V CERM 1206
C766 4.7UF 20% 6.3V CERM 1206

Q51
SI7860DP
SO-8-PWRPK
CRITICAL

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))

WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)

L30
2.1UH-11A
SM
CRITICAL

D24
SMB
B340LB

R352 4.99K 1% 1/16W MF 402
R451 18.2K 1% 1/16W MF 402
R351 20K 1% 1/16W MF 402
R804 1.82K 1% 1/16W MF 402

C708 22uF 20% 10V CERM 1210
C721 330UF 20% 6.3V POLY SMD
C719 330UF 20% 6.3V POLY SMD
C720 330UF 20% 6.3V POLY SMD
R307 100K 5% 1/16W MF 402
C902 0.1UF 20% 10V CERM 402

Q80
2N7002DW
SOT-363

R410 10K 5% 1/16W MF 402
C515 0.1uF 20% 10V CERM 402

Q48
SI7892DP
SO-8-PWRPK
CRITICAL

D5
SM
MBR0540

R416 2.2 5% 1/16W MF 603
C514 0.1uF 20% 25V CERM 603
C494 0.1uF 20% 25V CERM 603

U16
LTC1778
SSOP
CRITICAL
EXT INT VIN VCC VCC
RUN/SS ITH VRNG FCB PGOOD SGND
ION BOOST TG SW BG VFB PGND

R236 100K 5% 1/16W MF 402
R390 0 5% 1/16W MF 402
R340 20K 1% 1/16W MF 402
C451 220pF 5% 25V CERM 402
C448 470pF 10% 10V CERM 402
R311 0 5% 1/16W MF 402
R332 0 5% 1/16W MF 402
C483 0.1uF 20% 10V CERM 402
C882 0.0022UF 10% 50V CERM 402
NO STUFF

R388 0 5% 1/16W MF 402 NO STUFF
R341 63.4K 1% 1/16W MF 402 NO STUFF
C473 4.7UF 20% 10V CERM 1206

R306 100K 5% 1/16W MF 402
R316 100K 5% 1/16W MF 402
R294 10K 5% 1/16W MF 402
R203 33K 5% 1/16W MF 402
Q6 2N3904 SM
Q5 2N3904 SM
DP1 BAS16TW SOT-363

+5V_MAIN
+1_5V_AGP
+3V_GPU
+2_5V_SLEEP
+PBUS
GPU_VCORE_PWR_SEQ
GPU_VCORE_SEQ_L
GPU_VCORE_SEQ
1778_SHDN_L_D3COLD
SLEEP_L_LS5
DCDC_EN
1778_SHDN_L
1778_ITH
1778_VRNG
1778_FCB
1778_RC
1778_GND
1778_VIN
1778_ION
1778_BST
1778_TG
1778_BST_RC
1778_SW
1778_BG
1778_VFB
1778_VCC
GPU_VCORE_SW
GPU_VCORE_OK
GPU_VCORE
GPU_VCORE_NECK
+GPU_VDD15_NECK
+1_5V_AGP_NECK
+1_8V_PVDD
+1_8V_PVDD_NECK
+2_5V_SLEEP_NECK
HIGH_VCORE_DIV
HIGH_VCORE
VCORE_CNTL_RC
GPU_VCORE_CNTL
GPU_PWRMSR

M10 CORE PWR/LVDS/TMDS

NOTICE OF PROPRIETARY PROPERTY

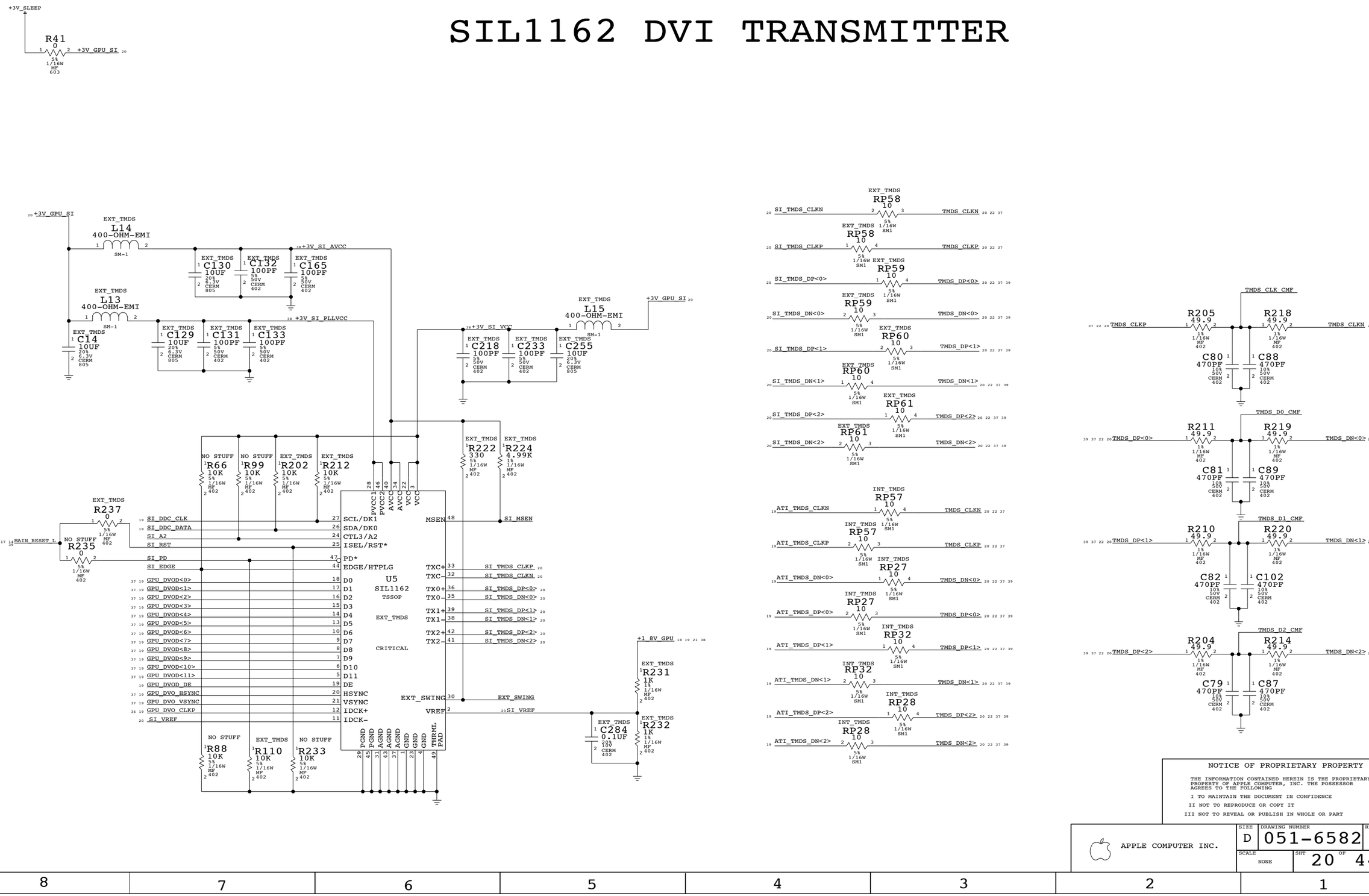
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 19 OF 44	

SIL1162 DVI TRANSMITTER



NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

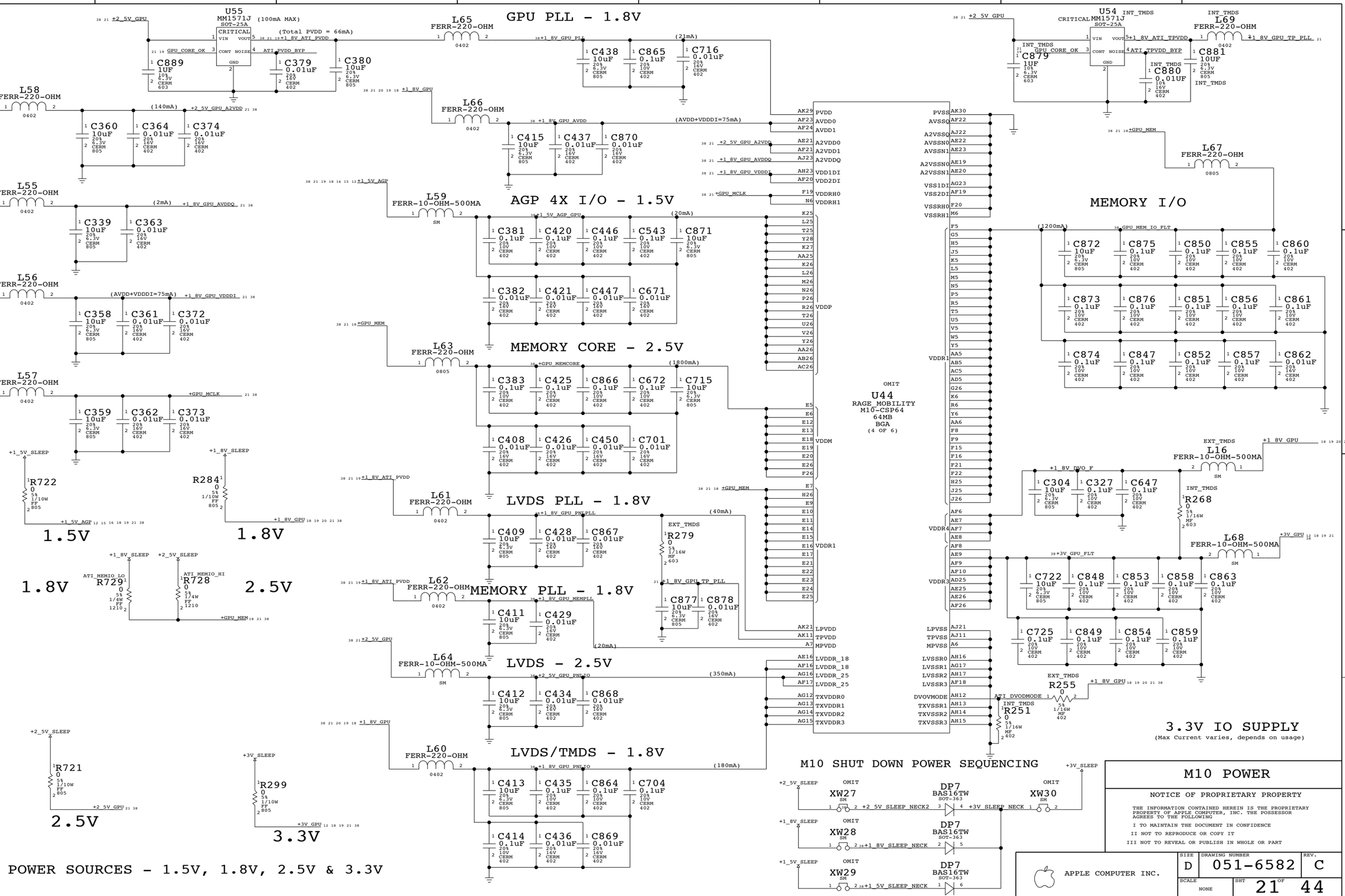
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE	SHT	OF
NONE	20	44


GPU PLL - 1.8V
AGP 4X I/O - 1.5V
MEMORY CORE - 2.5V
LVDS PLL - 1.8V
MEMORY PLL - 1.8V
LVDS - 2.5V
LVDS/TMDS - 1.8V
MEMORY I/O
3.3V IO SUPPLY
(Max Current varies, depends on usage)
1.5V
1.8V
2.5V
3.3V
GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V
M10 SHUT DOWN POWER SEQUENCING
U44 RAGE MOBILITY M10-CSP64 64MB BGA (4 OF 6)
U55 MM1571J (100mA MAX) SOT-25A
U54 MM1571J SOT-25A
L58 FERR-220-OHM
L55 FERR-220-OHM
L56 FERR-220-OHM
L57 FERR-220-OHM
L65 FERR-220-OHM
L66 FERR-220-OHM
L59 FERR-10-OHM-500MA
L63 FERR-220-OHM
L61 FERR-220-OHM
L62 FERR-220-OHM
L64 FERR-10-OHM-500MA
L60 FERR-220-OHM
L69 FERR-220-OHM
L67 FERR-220-OHM
L16 FERR-10-OHM-500MA
L68 FERR-10-OHM-500MA
M10 POWER
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6582
REV. C
SCALE NONE
SHT 21 OF 44

EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 CRITICAL LCFILTER SM-220MHZ — GPU_B → VGA_B
FL1 CRITICAL LCFILTER SM-220MHZ — GPU_G → VGA_G
FL3 CRITICAL LCFILTER SM-220MHZ — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
U56 CRITICAL 74AHC1G32 SM — ATI_HSYNC → R718 33 5% 1/16W MF 402 → VGA_HSYNC_BUF → VGA_HSYNC
U57 CRITICAL 74AHC1G32 SM — ATI_VSYNC → R714 33 5% 1/16W MF 402 → VGA_VSYNC_BUF → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP
Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO
R655 4.7K 5% 1/16W MF 402
R661 4.7K 5% 1/16W MF 402

J14 CRITICAL QH1112 F-RT-TH

TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2>
TMDS_CONN_DP<0>	18	9	TMDS_CONN_DN<1>
(TMDS_DN<5>)	19	2	TMDS_CONN_DP<2>
(TMDS_DP<5>)	20	10	TMDS_CONN_DP<1>
NC	21	3	NC
	22	11	(TMDS_DN<4>)
TMDS_CONN_CLKP	23	4	(TMDS_DP<4>)
TMDS_CONN_CLKN	24	12	NC
VGA_B	C3	5	(TMDS_DN<3>)
VGA_HSYNC	C4	13	(TMDS_DP<3>)
	C5B	C5A	
	34	6	DVI_DDC_CLK_UF
		14	(+5V_DDC_SLEEP)
		7	DVI_DDC_DATA_UF
		15	
		8	VGA_VSYNC
		16	DVI_HPD_UF
		C1	VGA_R
		C2	VGA_G
	35	32	

R670 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402
R650 100 5% 1/16W MF 402
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C1 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND1 CHGND5

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

Q40 SM TP0610 — DVI_DDC_CLK_UF → DVI_TURN_ON
R690 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TRUN_ON_ILIM
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q42 2N3904 SM — SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF
U46 CRITICAL LMC7211 SM — HPD_PWR_SM
R663 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402
+PBUS
Q45 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402 — COMP_DISABLE
R704 100K 5% 1/16W MF 402
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM — HPD_ON_RC
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
Q41 2N7002DW SOT-363 — HPD_PWR_SNS_EN
R213 100K 5% 1/16W MF 402

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<0> → TMDS_CONN_DN<0>; TMDS_DP<0> → TMDS_CONN_DP<0>
L21 CRITICAL 165-OHM SM — TMDS_CLKP → TMDS_CONN_CLKP; TMDS_CLKN → TMDS_CONN_CLKN
L73 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<1> → TMDS_CONN_DN<1>; TMDS_DP<1> → TMDS_CONN_DP<1>
L74 CRITICAL 90-OHM-300MA 2012H — TMDS_DN<2> → TMDS_CONN_DN<2>; TMDS_DP<2> → TMDS_CONN_DP<2>

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

C416 0.001uF 20% 50V CERM 402 — CHGND4
CRITICAL J6 G-501973 F-RT-SM
+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
+3V_LCD
(LVDS DDC POWER)
NC
LVDS_DDC_CLK
LVDS_DDC_DATA
NO STUFF
C449 0.001uF 20% 50V CERM 402
C452 0.001uF 20% 50V CERM 402 — CHGND4

LVDS_L0N	8	9	LVDS_L0P
LVDS_L1N	11	12	LVDS_L1P
LVDS_L2N	14	15	LVDS_L2P
CLKLVDS_LN	17	18	CLKLVDS_LP
LVDS_U0N	20	21	LVDS_U0P
LVDS_U1N	23	24	LVDS_U1P
LVDS_U2N	26	27	LVDS_U2P
CLKLVDS_UN	29	30	CLKLVDS_UP

C500 0.001uF 20% 50V CERM 402 — CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN_L
L32 400-OHM-EMI SM-1 — +5V_INV_SW
C440 10UF 20% 6.3V CERM 805
C746 0.001UF 20% 50V CERM 402
CRITICAL J7 SM-2MT
Q7 FDG6324L SC70-6 — FP_PWR_EN
C749 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C739 0.001UF 20% 50V CERM 402
+3V_PMU
C552 0.1UF 20% 10V CERM 402
74LVC32 TSSOP — U24 — INV_ON_PWM → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603 — CHGND2

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1
L26 FERR-10-OHM-500MA SM — TV_GND1
L25 3.3UH 0603 — GPU_Y
L29 3.3UH 0603 — GPU_C
L27 3.3UH 0603 — GPU_COMP
C712 0.01UF 20% 50V CERM 603
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
CRITICAL J15 MINIDIN RT-TH MH1177 — TV_C, TV_Y, TV_COMP
XW13 SM — GPU_TV_GND2
L28 FERR-10-OHM-500MA SM — TV_GND2
C717 0.01UF 20% 50V CERM 603
Place GND shorts at graphics controller
CHGND1

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603
R391 100K 5% 1/16W MF 402 — LCD_PWREN_L
LCD_DIGON_L
Q11 TSOP SI3443DV — +3V_LCD_SW
L6 FERR-250-OHM SM — C474 0.001uF 20% 50V CERM 402
Q8 2N7002 SM — FP_PWR_EN
CHGND4

VIDEO CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

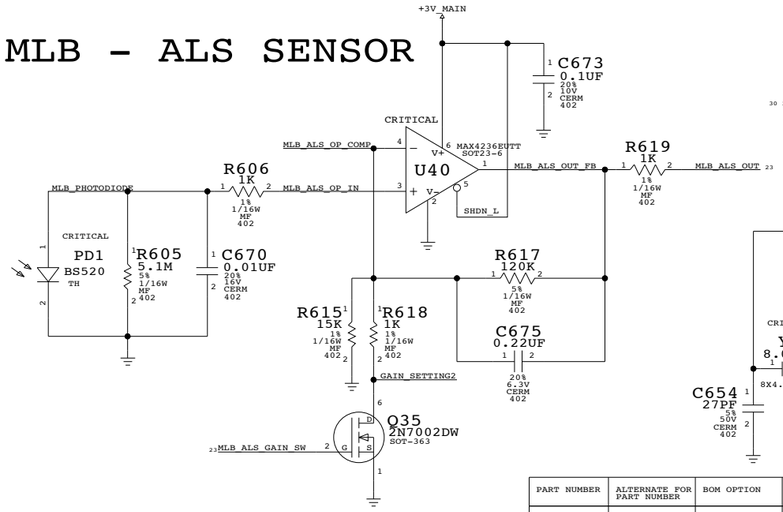
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

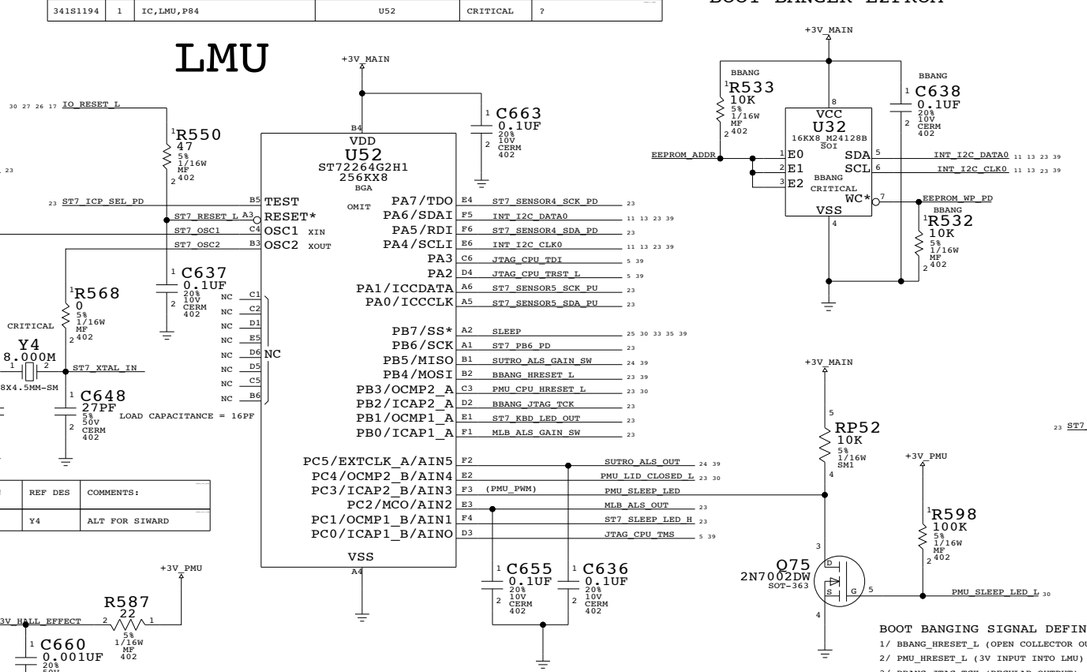
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 22 OF 44	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR



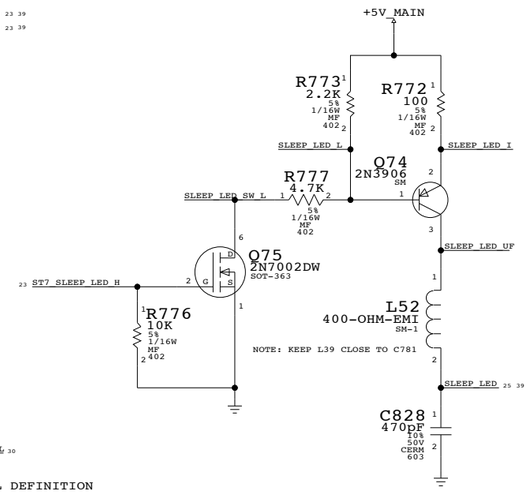
LMU



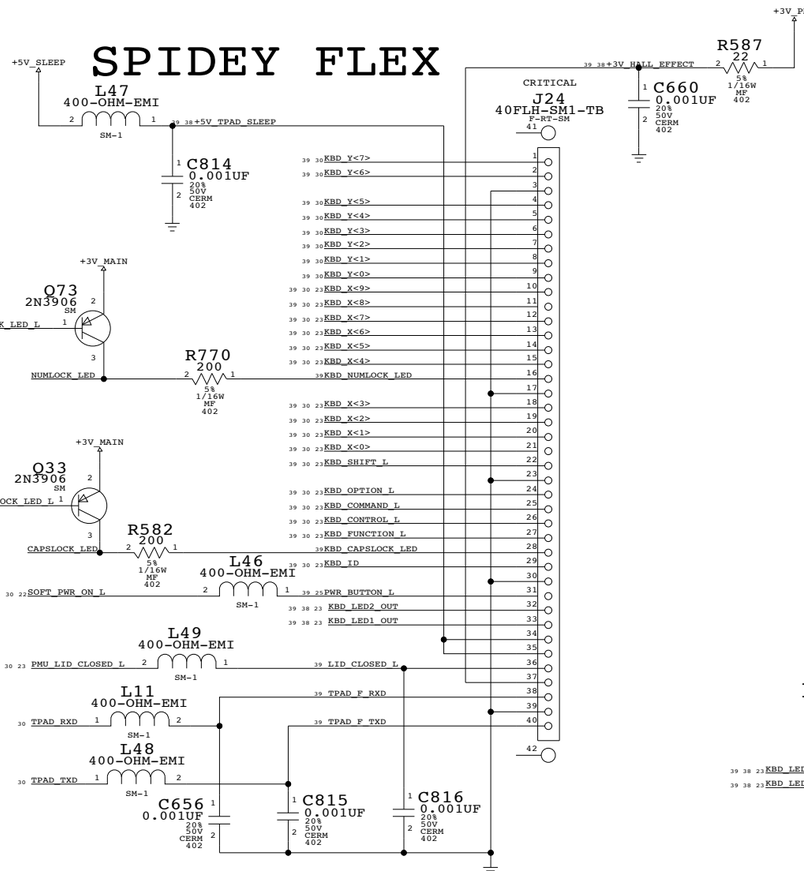
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

BOOT BANGER E2PROM

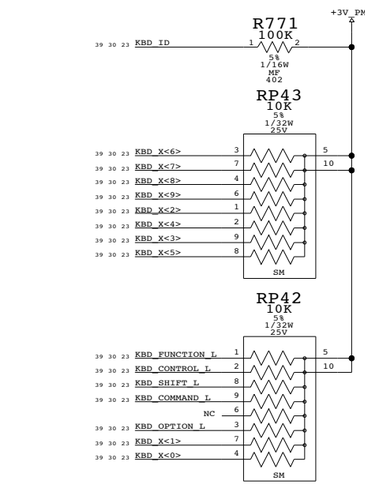
SLEEP LED



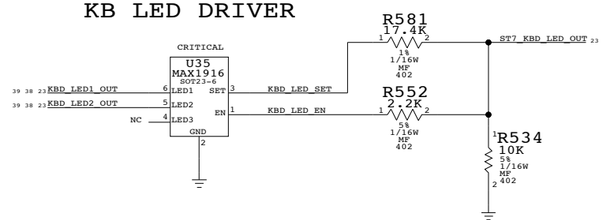
SPIDEY FLEX

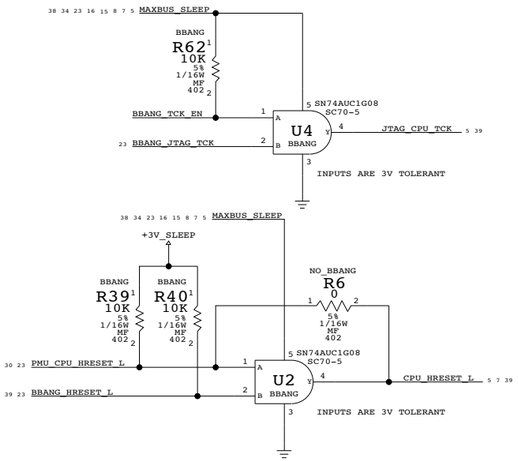


KEYBOARD PULLUPS

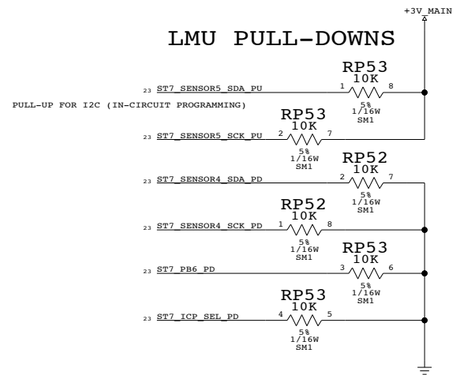


KB LED DRIVER





LMU PULL-DOWNS



BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

LMU/BOOTBANGER/SPIDEY

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

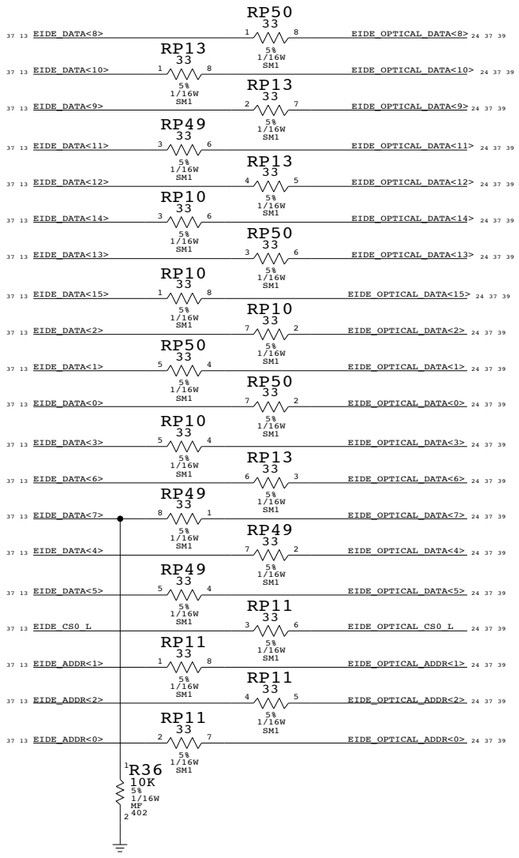
APPLE COMPUTER INC.

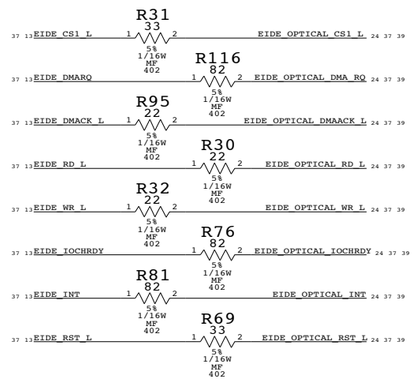
SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 23 OF 44	

HARD DRIVE INTERFACE (UATA100)

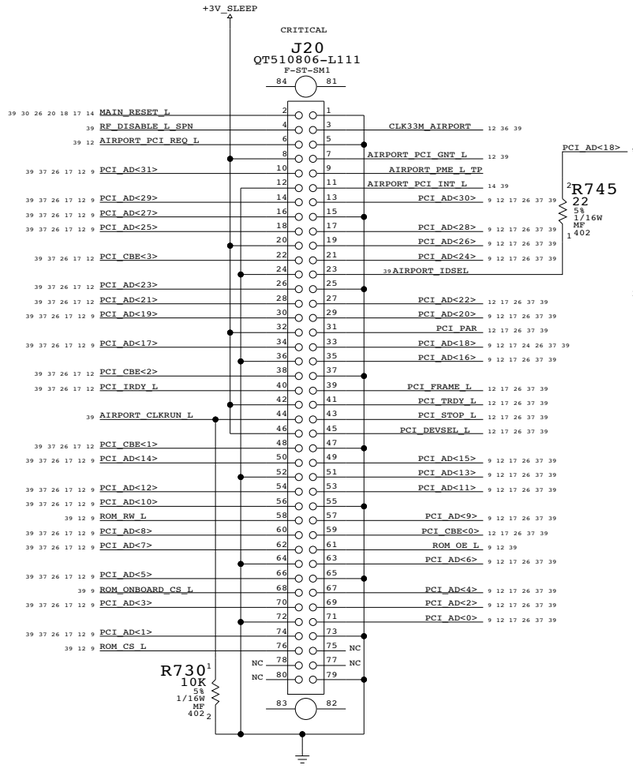
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

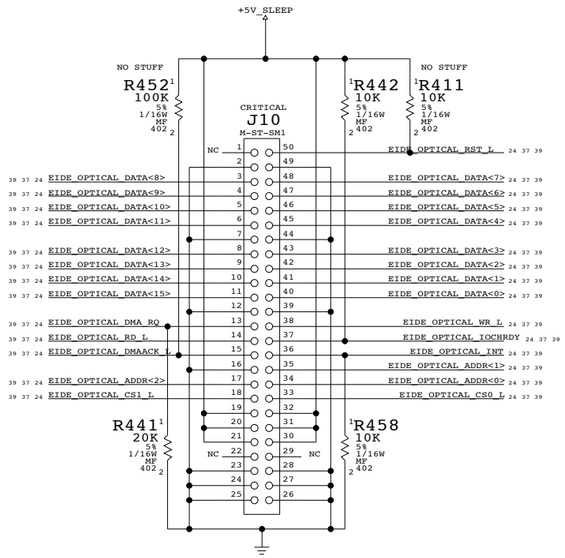




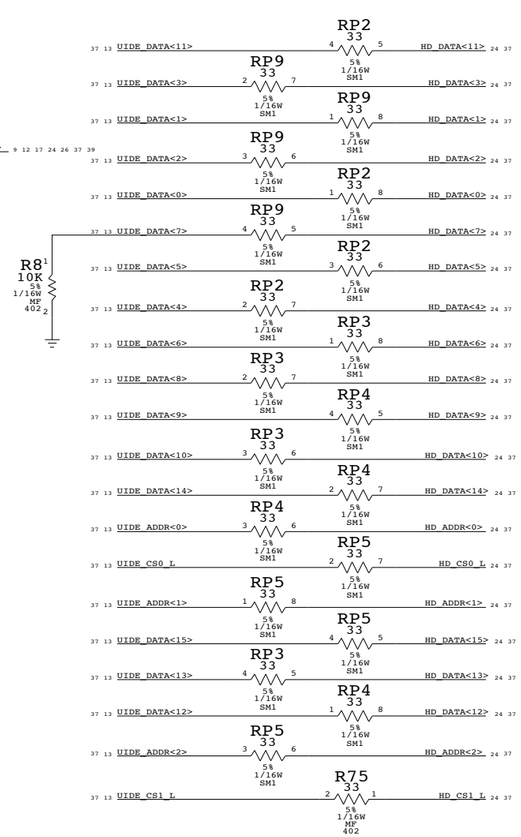
WIRELESS INTERFACE



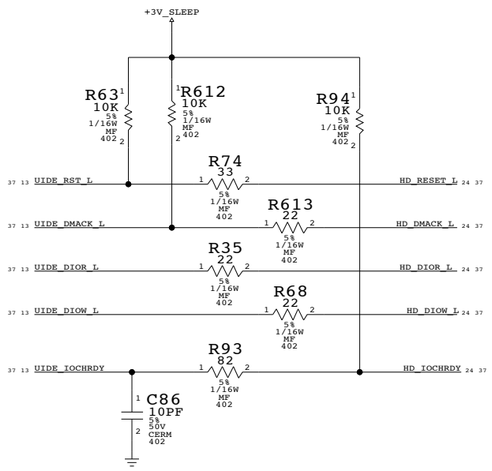
OPTICAL DRIVE INTERFACE (EIDE)



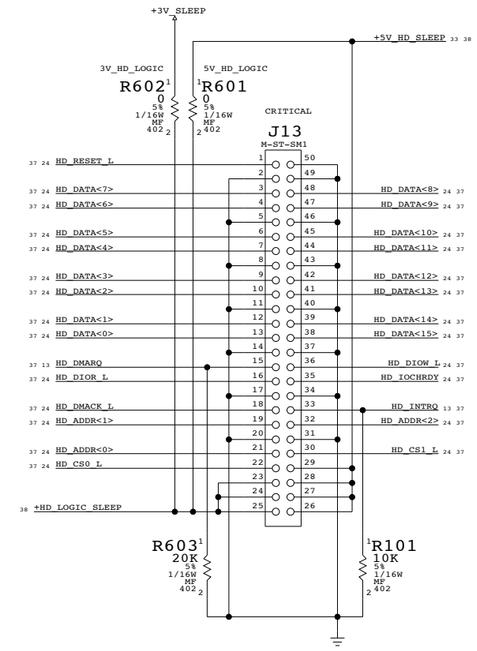
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

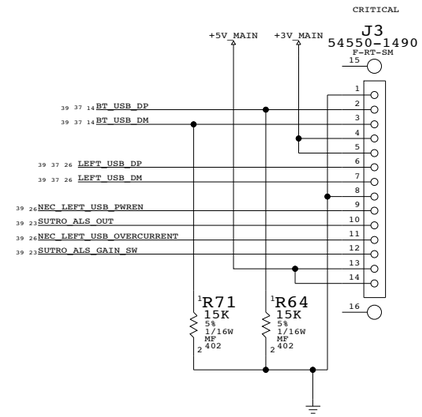


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 24 OF 44	

SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

L77 FERR-220-OHM 0402
L80 FERR-220-OHM 0402
L81 FERR-220-OHM 0402
L82 FERR-220-OHM 0402
L76 FERR-220-OHM 0402
L78 FERR-220-OHM 0402
L79 FERR-220-OHM 0402

SND_SYNC → SND_SYNC_F
SND_CLKOUT → SND_CLKOUT_F
INT_AUDIO_TO_SND → INT_AUDIO_TO_SND_F
SND_TO_AUDIO → SND_TO_AUDIO_F
SND_AMP_MUTE → SND_AMP_MUTE_F
SND_HW_RESET_L → SND_HW_RESET_L_F
SND_SCLK → SND_SCLK_F

C895 0.01UF 20% 16V CERM 402 NO STUFF
C899 0.01UF 20% 16V CERM 402 NO STUFF
C896 0.01UF 20% 16V CERM 402 NO STUFF
C897 0.01UF 20% 16V CERM 402 NO STUFF
C898 0.01UF 20% 16V CERM 402 NO STUFF
C900 0.01UF 20% 16V CERM 402 NO STUFF
C901 0.01UF 20% 16V CERM 402 NO STUFF

+3V_MAIN
+5V_MAIN

CRITICAL
J12
QT510306-L111
F-ST-SM1

INT_AUDIO_TO_SND_F
INT_I2C_CLK2
SND_SCLK_F
SND_CLKOUT_F
SND_SYNC_F
INT_I2C_DATA2
SLEEP_LED

SND_TO_AUDIO_F
SND_HP_SENSE_L
SND_LIN_SENSE_L
SND_AMP_MUTE_F
SLEEP
SND_HW_RESET_L_F
SND_HP_MUTE_INV

XW9 SM SND_AGND

+5V_MAIN
RP44 100K 5% 1/16W SM1
SND_AMP_MUTE
Q26 2N7002DW SOT-363
SND_AMP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1
Q26 2N7002DW SOT-363
INT_PU_RESET_L

+3V_MAIN
RP44 100K 5% 1/16W SM1
1R689 100K 5% 1/16W MF 402
SND_HP_MUTE_INV
Q31 2N7002DW SOT-363
SND_HP_MUTE
Q31 2N7002DW SOT-363
SND_HP_MUTE_L
AMP_CONTROL
RP44 100K 5% 1/16W SM1

MODEM

SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM

+5V_MAIN
C767 10UF 20% 6.3V CERM 805 NO STUFF
C513 0.1UF 20% 10V CERM 402
1R405 10K 5% 1/16W MF 402
+3V_MAIN
C478 0.1UF 20% 10V CERM 402 NO STUFF
C469 10UF 20% 6.3V CERM 805

CRITICAL
J8
QT51066-L010
F-ST-SM1

MOD_DTO
MOD_CLKOUT
COMM_RESET_L
COMM_SHUTDOWN
INT_I2C_CLK2
INT_I2C_DATA2

MOD_SYNC
INT_MOD_DTI
MOD_BITCLK
MODEM_USB_DM
MODEM_USB_DP
COMM_RING_DET_L

FAN CONTROLLER

+3V_MAIN
R814 10 5% 1/16W MF 402
ADT7460_VCC
C904 1UF 20% 10V CERM 603
C711 0.1UF 20% 10V CERM 402

VCC
U3
QSOP
ADT7460

+2.5V/SMBALERT#
SDA
SCL
D1+
D1-
D2+
D2-
GND

PWM1/XTO
TACH1
PWM2/SMBALERT#
TACH2
PWM3/ADR ENABLE#
TACH3
TACH4/ADR SELECT/THERM#

ADT7460_VCORE_MON
INT_I2C_DATA1
INT_I2C_CLK1
THERM1_DP
THERM1_DM
THERM2_DP
THERM2_DM

ADT7460_FAN1_PWM
FANL_TACH
ADT7460_FAN2_PWM
FANR_TACH
ADT7460_ADR_EN_L
NC
ADT7460_THERM

1R42 10K 5% 1/16W MF 402
+5V_SLEEP
1R692 10K 5% 1/16W MF 402
1R695 10K 5% 1/16W MF 402
Q78 2N7002DW SOT-363
Q78 2N7002DW SOT-363

C688 0.001UF 20% 50V CERM 402 NO STUFF
C690 0.001UF 20% 50V CERM 402 NO STUFF
C846 0.001UF 20% 50V CERM 402 NO STUFF
C905 0.001UF 20% 50V CERM 402 NO STUFF

SERIAL DEBUG INTERFACE

+5V_MAIN
SERIAL_DEBUG
CRITICAL
J16
M-ST-5087
SM

COMM_TXD_L
COMM_TRXC
COMM_GPIO_L
COMM_DTR_L
COMM_RTS_L
COMM_RXD

DEBUG POWER BUTTON

NO STUFF
R527 0 5% 1/16W MF 603
PWR_BUTTON_L

DEBUG JUMPERS

+5V_SLEEP
1R293 10K 5% 1/16W MF 402
1R295 10K 5% 1/16W MF 402
FANL_PWM
FANR_PWM
Q78 2N7002DW SOT-363

NO STUFF
R537 0 5% 1/16W MF 603
PMU_NMI_BUTTON_L
NO STUFF
R553 0 5% 1/16W MF 603
PMU_RESET_BUTTON_L

RIGHT FAN (GPU)

+5V_SLEEP
1R623 10K 5% 1/16W MF 402
CRITICAL
J2
SM-2MT
FANR_GND
FANR_TACH
Q36 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C135 4.7UF 20% 10V CERM 1206
FANR_PWM

LEFT FAN (CPU)

+5V_SLEEP
R679 1 10K 5% 1/16W MF 402
CRITICAL
J4
SM-2MT
FANL_TACH
FANL_GND
Q37 SI3446DV TSOP
PLACE CLOSE TO CONNECTOR
C134 4.7UF 20% 10V CERM 1206
FANL_PWM

PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

CAPS FOR EMI EXPERIMENTATION ONLY

FAN INTERFACE

MAIN1
C681 0.0001UF 20% 50V CERM 402
Q66 2N3904 SM
SUPPLY_M_DP
SUPPLY_M_DM

PLACE CLOSE TO CPU
MAIN2
C668 0.001UF 20% 50V CERM 402
Q39 2N3904 SM
CPU_M_DP
CPU_M_DM

PLACE UNDERNEATH UPPER RAM
ALTERNATE1
C678 0.001UF 20% 50V CERM 402 NO STUFF
Q47 2N3904 SM NO STUFF
THERM1_A_DP
THERM1_A_DM

PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2
C651 0.001UF 20% 50V CERM 402 NO STUFF
Q62 2N3904 SM NO STUFF
THERM2_A_DP
THERM2_A_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R719 0 5% 1/16W MF 402
R725 0 5% 1/16W MF 402
R713 0 5% 1/16W MF 402
R716 0 5% 1/16W MF 402

CPU_M_DP → THERM1_DP
CPU_M_DM → THERM1_DM
SUPPLY_M_DP → THERM2_DP
SUPPLY_M_DM → THERM2_DM

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

R723 0 5% 1/16W MF 402 NO STUFF
R726 0 5% 1/16W MF 402 NO STUFF
R710 0 5% 1/16W MF 402 NO STUFF
R717 0 5% 1/16W MF 402 NO STUFF

THERM1_A_DP → THERM1_DP
THERM1_A_DM → THERM1_DM
THERM2_A_DP → THERM2_DP
THERM2_A_DM → THERM2_DM

THERM ISOLATION

+3V_MAIN
1R811 100K 5% 1/16W MF 402
+3V_PMU_AVCC
1R812 100K 5% 1/16W MF 402
THERM_L_OC
1R813 100K 5% 1/16W MF 402
THERM_INV
Q87 2N7002DW SOT-363
Q87 2N7002DW SOT-363
C903 0.1UF 20% 10V CERM 402
ADT7460_THERM

FAN/MODEM/SOUND/SLEEP LED/DEBUG

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6582
REV. C
SCALE NONE
SHT 25 OF 44

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD

+3V_NEC_VDD

C841 0.1uF 20% 10V CERM 402 — C837 0.1uF 20% 10V CERM 402 — C843 0.1uF 20% 10V CERM 402 — C836 0.1uF 20% 10V CERM 402

C840 0.1uF 20% 10V CERM 402 — C829 0.1uF 20% 10V CERM 402 — C834 0.1uF 20% 10V CERM 402 — C838 0.1uF 20% 10V CERM 402

C842 0.1uF 20% 10V CERM 402 — C845 10uF 20% 6.3V CERM 805 — C830 0.1uF 20% 10V CERM 402 — C833 0.1uF 20% 10V CERM 402

+3V_MAIN — L54 FERR-EMI-100-OHM (SM) — NEC_AVDD

C839 0.1uF 20% 10V CERM 402 — C844 0.1uF 20% 10V CERM 402 — C667 10uF 20% 6.3V CERM 805

R796 0 5% 1/16W MF 603 — +3V_NEC_VDD

Y7 LOAD CAPACITANCE IS 16PF

CRITICAL
Y5 30.0000M (8X4.5MM-SM)

C649 27PF 5% 50V CERM 402 — C657 27PF 5% 50V CERM 402 — R590 100 5% 1/16W MF 402

NEC_XT2_R — NEC_XT1 — NEC_XT2

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

+3V_MAIN — RP52 10K 5% 1/16W SM1 — R783 10K 5% 1/16W MF 402

NEC_PCI_SERR_L — NEC_PCI_PERR_L

R784 22 5% 1/16W MF 402

PCI_AD<27>

Series Rpaks required to facilitate NAND-tree testing

RP55 47 5% 1/16W SM1

IO_RESET_L — NEC_IO_RESET_L
PMU_PME_L — NEC_PME_L
MAIN_RESET_L — NEC_MAIN_RESET_L

R551 4.7K 5% 1/16W MF 402

RP54 47 5% 1/16W SM1

USB2_PCI_INT_L — NEC_PCI_INTA_L — NEC_PCI_INTB_L — NEC_PCI_INTC_L — NEC_LEGC

Low/Full/High Speed (External)

CRITICAL
U39
NEC_UPD720101_USB2
FBGA

Low/Full/High Speed (External)

PCI_AD<0>	M5	AD0	
PCI_AD<1>	P5	AD1	
PCI_AD<2>	N5	AD2	
PCI_AD<3>	P4	AD3	
PCI_AD<4>	N4	AD4	
PCI_AD<5>	M3	AD5	
PCI_AD<6>	N3	AD6	
PCI_AD<7>	M1	AD7	
PCI_AD<8>	L2	AD8	
PCI_AD<9>	L1	AD9	
PCI_AD<10>	K2	AD10	
PCI_AD<11>	L3	AD11	
PCI_AD<12>	K1	AD12	
PCI_AD<13>	K3	AD13	
PCI_AD<14>	J2	AD14	
PCI_AD<15>	J1	AD15	
PCI_AD<16>	F2	AD16	
PCI_AD<17>	E3	AD17	
PCI_AD<18>	E1	AD18	
PCI_AD<19>	D3	AD19	
PCI_AD<20>	D1	AD20	
PCI_AD<21>	D2	AD21	
PCI_AD<22>	C2	AD22	
PCI_AD<23>	C1	AD23	
PCI_AD<24>	B4	AD24	
PCI_AD<25>	A4	AD25	
PCI_AD<26>	B5	AD26	
(PCI_AD<27>)	C4	AD27	
PCI_AD<28>	A5	AD28	
PCI_AD<29>	C5	AD29	
PCI_AD<30>	B6	AD30	
PCI_AD<31>	A6	AD31	
PCI_CBE<0>	M2	CBE0	
PCI_CBE<1>	J3	CBE1	
PCI_CBE<2>	F1	CBE2	
PCI_CBE<3>	C3	CBE3	
PCI_PAR	J4	PAR	
PCI_FRAME_L	F3	FRAME	
PCI_IRDY_L	F4	IRDY	
PCI_TRDY_L	G1	TRDY	
PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
PCI_DEVSEL_L	G2	DEVSEL	
USB2_PCI_REQ_L	C6	REQ	
USB2_PCI_GNT_L	D6	GNT	
NEC_PCI_PERR_L	H2	PERR	
NEC_PCI_SERR_L	H1	SERR	OD
NEC_PCI_INTA_L	C7	INTA	OD
NEC_PCI_INTB_L	B7	INTB	OD
NEC_PCI_INTC_L	A7	INTC	OD
CLK33M_USB2	A8	PCLK	
NEC_IO_RESET_L	B8	VBBRST	
NEC_CRUN_L	N6	CRUN	
NEC_PME_L	D9	PME	OD
NEC_MAIN_RESET_L	C9	VCCRST	
NEC_SMI_L_TP	L6	SMI	OD
	L7	LEGC	

VDD_PCI — VDD — AVDD

	L9	XT1/SCLK	
	P8	XT2	
NEC_USB_RSDM1	M14	RSDM1	
(NEC_USB_DAM)	M13	DM1	
(NEC_USB_DAP)	L14	DP1	
NEC_USB_RSDP1	K13	RSDP1	
NEC_USB_RSDM2	K14	RSDM2	
(NEC_USB_DBM)	K12	DM2	
(NEC_USB_DBP)	J14	DP2	
NEC_USB_RSDP2	J12	RSDP2	
RSDM3_TP	H11	RSDM3	
	G11	DM3	
	G13	DP3	
RSDP3_TP	G14	RSDP3	
RSDM4_TP	F12	RSDM4	
	F14	DM4	
	E12	DP4	
RSDP4_TP	E14	RSDP4	
RSDM5_TP	E13	RSDM5	
	D14	DM5	
	C13	DP5	
RSDP5_TP	C14	RSDP5	
NEC_RREF	P11	RREF	
NEC_OCI<1>	B12	OCI1	LEFT PORT
NEC_OCI<2>	B11	OCI2	RIGHT PORT
NEC_OCI<3>	B10	OCI3	
NEC_OCI<4>	A10	OCI4	
NEC_OCI<5>	B9	OCI5	
NEC_LEFT_USB_PWREN	C12	PPON1	OUT
NEC_RIGHT_USB_PWREN	A11	PPON2	OUT
NEC_PPON3_TP	C11	PPON3	OUT
NEC_PPON4_TP	C10	PPON4	OUT
NEC_PPON5_TP	A9	PPON5	OUT
NEC_NC1_TP	P6	NC1	
NEC_NC2_TP	M6	NC2	
NTEST1_TP	M8	NTEST1	IPD
SMC_TP	M7	SMC	IPD
TEB_TP	N7	TEB	IPD
NEC_AMC_TP	P7	AMC	IPD
TEST_TP	L8	TEST	IPD
NEC_NANDTESTEN_TP	M10	NANDTEST	
SRCLK_TP	M9	SRCLK	
NEC_NANDTESTOUT_TP	N9	SRDTA	
SRMOD_TP	P9	TPDSRMOD	
	P13	AVSS	
NEC_AVSS_F	M12	AVSS(R)	

R795 36 1% 1/16W MF 402 — NEC_USB_DAM
R792 36 1% 1/16W MF 402 — NEC_USB_DAP
R791 36 1% 1/16W MF 402 — NEC_USB_DBM
R790 36 1% 1/16W MF 402 — NEC_USB_DBP

Tie to GND at ball N11

R794 9.09K 1% 1/16W MF 402 — NEC_AVSS_F

R286 0 5% 1/16W MF 603

VSS

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING	14
USB_DAP	USB_DA	5 MIL SPACING	14
USB_DCM	USB_DC	5 MIL SPACING	14
USB_DCP	USB_DC	5 MIL SPACING	14
USB_D1M	USB_D1	5 MIL SPACING	14 26
USB_D1P	USB_D1	5 MIL SPACING	14 26
USB_D2M	USB_D2	5 MIL SPACING	14 26
USB_D2P	USB_D2	5 MIL SPACING	14 26

+3V_MAIN

RP45 10K 5% 1/16W SM1 — NEC_LEFT_USB_OVERCURRENT
RP45 10K 5% 1/16W SM1 — NEC_RIGHT_USB_OVERCURRENT

R591 15K 5% 1/16W MF 402 — NEC_OCI<1>
R600 15K 5% 1/16W MF 402 — NEC_OCI<2>

C661 0.1uF 20% 10V CERM 402 — C665 0.1uF 20% 10V CERM 402

+3V_MAIN

R56 10K 5% 1/16W MF 402 — INTREPID_USB
R531 10K 5% 1/16W MF 402 — INTREPID_USB
RP45 10K 5% 1/16W SM1 — NEC_USB
RP45 10K 5% 1/16W SM1 — NEC_USB
R586 10K 5% 1/16W MF 402 — NEC_USB

R789 1.5K 5% 1/16W MF 402 — NEC_USB
R793 1.5K 5% 1/16W MF 402 — NEC_USB

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

R84 0 5% 1/16W MF 402 — NEC_USB_DAM — LEFT_USB_DM
R96 0 5% 1/16W MF 402 — INTREPID_USB — USB_D1M
R83 0 5% 1/16W MF 402 — NEC_USB_DAP — LEFT_USB_DP
R78 0 5% 1/16W MF 402 — INTREPID_USB — USB_D1P
R545 0 5% 1/16W MF 402 — NEC_USB_DBM — RIGHT_USB_DM
R554 0 5% 1/16W MF 402 — INTREPID_USB — USB_D2M
R540 0 5% 1/16W MF 402 — NEC_USB_DBP — RIGHT_USB_DP
R530 0 5% 1/16W MF 402 — INTREPID_USB — USB_D2P

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

USB 2.0

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 26 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0223	338S0079	7	U49	ALT FOR B1

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C442 10uF 20% 6.3V CERM 805

NO STUFF R333 0 5% 1/16W MF 402

3405_MODE

R319 0 5% 1/16W MF 402

U14 LTC3405 SOT23-6 — VIN, RUN, MODE, GND, SW, VFB

LTC3405_SW

CRITICAL L5 3.3uH SM1

+1.0V_MARVELL

R334 665K 1% 1/16W MF 402 R2A

C471 22pF 5% 50V CERM 402

R361 49.9K 1% 1/16W MF 402 R2B

C486 10uF 20% 6.3V CERM 805

3405_VFB

R362 182K 1% 1/16W MF 402 R1

VOUT = 0.8V*(1+R2EQV/R1)

R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R370 0 5% 1/16W MF 402 — CLKENET_LINK_TX / CLKENET_PHY_TX

R353 0 5% 1/16W MF 402 — CLKENET_LINK_RX / CLKENET_PHY_RX

R344 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF / CLKENET_PHY_GBE_REF

CRITICAL U49 88E1111 BCC

TX_CLK, RX_CLK, 125CLK

TXD0–TXD7, TX_EN, TX_ER, GTX_CLK

RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO

CTRL10 — NC

DVDD: C492 0.1UF, C511 0.01UF, C517 0.1UF, C502 0.01UF, C465 0.1UF, C475 0.01UF
PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

VDDO: C464 0.1UF, C472 0.01UF, C453 0.1UF, C503 0.01UF, C501 0.1UF, C496 10uF 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

VDDOH

VDDOX

+2_5V_MARVELL

L34 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

AVDD: C497 0.1UF, C504 0.1UF, C487 0.01UF, C476 0.1UF, C754 10uF 6.3V CERM 805
PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN

R465 0 5% 1/16W 603

PLACE CLOSE TO ETHERNET CONNECTOR

NO STUFF R438 0 5% 1/10W MF 805 — CHGND1

C488 0.1UF, C466 0.1UF, C506 0.1UF, C520 0.1UF
PLACE CAPS AT TRANSFORMER PINS 1, 4, 7 & 10

CRITICAL J17 RJ45 RT-TH

RJ45_DP<0>, RJ45_C0_PD, RJ45_DN<0>, RJ45_DP<1>, RJ45_C1_PD, RJ45_DN<1>, RJ45_DP<2>, RJ45_C2_PD, RJ45_DN<2>, RJ45_DP<3>, RJ45_C3_PD, RJ45_DN<3>

Short shielded RJ-45 — CHGND1

SM XFR-ENET-1000BT T1 CRITICAL

MDI0+, MDI0-, MDI1+, MDI1-, MDI2+, MDI2-, MDI3+, MDI3-

R346 49.9 1% 1/16W MF 402 — MDI0_PD
R372 49.9 1% 1/16W MF 402 — MDI1_PD
R404 49.9 1% 1/16W MF 402 — MDI2_PD
R413 49.9 1% 1/16W MF 402 — MDI3_PD

R355 49.9 1% 1/16W MF 402
R381 49.9 1% 1/16W MF 402
R406 49.9 1% 1/16W MF 402
R428 49.9 1% 1/16W MF 402

C454 0.01UF, C477 0.01UF, C493 0.01UF, C505 0.01UF

PLACE RESISTORS CLOSE TO PHY

R735 75 5% 1/16W MF 402, R733 75 5% 1/16W MF 402, R382 75 5% 1/16W MF 402, R347 75 5% 1/16W MF 402 — ENET_CTAP_CHGND

C457 100pF 10% 3KV CERM 1808 — CHGND1

LED_LINK10, LED_LINK100, LED_LINK1000 (NC), LED_DUPLEX (NC), LED_RX, LED_TX (NC)

CONFIG0 (000), CONFIG1 (000), CONFIG2 (111), CONFIG3 (110), CONFIG4 (111), CONFIG5 (101), CONFIG6 (000)

SEE CONFIG TABLES (BELOW)

TDI, TDO, TCK, TMS, TRST — JTAG_ENET_TDI, JTAG_ASIC_TDO_TP, JTAG_ASIC_TCK, JTAG_ASIC_TMS, JTAG_ASIC_TRST_L

RSET — ENET_RSET

SEL_OSC (NC), SEL_2.5V

GND

+2_5V_MARVELL

R371 10K 5% 1/16W MF 402

R345 10K 5% 1/16W MF 402

R354 1.5K 5% 1/16W MF 402

R343 1K 5% 1/16W MF 402 — INT_ENET_RST_L

D1 1N914 SOT23 — IO_RESET_L / ENET_RST_L

ENET_ENERGY_DET

Q15 2N7002DW SOT-363 — AC_IN

Q15 2N7002DW SOT-363 — SLEEP_L_LS5

C755 2.2uF 20% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

ENET_COMA

ENET_HSDACP, ENET_HSDACM

S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-

CLK25M_ENET_XIN, CLK25M_ENET_XOUT

ENET_VSSC

PUT CRYSTAL CIRCUIT CLOSE TO PHY

NO STUFF R435 20K 5% 1/16W MF 402

R427 0 5% 1/16W MF 402

CRITICAL Y3 25.0000M 8X4.5MM-SM

CLK25M_XTAL_IN

C555 33pF 5% 50V CERM 402

C491 33pF 2% 50V CERM 402

Y3'S LOAD CAPACITANCE IS 20PF

NO STUFF R393 49.9 1% 1/16W MF 402

NO STUFF R403 49.9 1% 1/16W MF 402

R335 10K 5% 1/16W MF 402

R380 4.99K 1% 1/16W MF 402

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

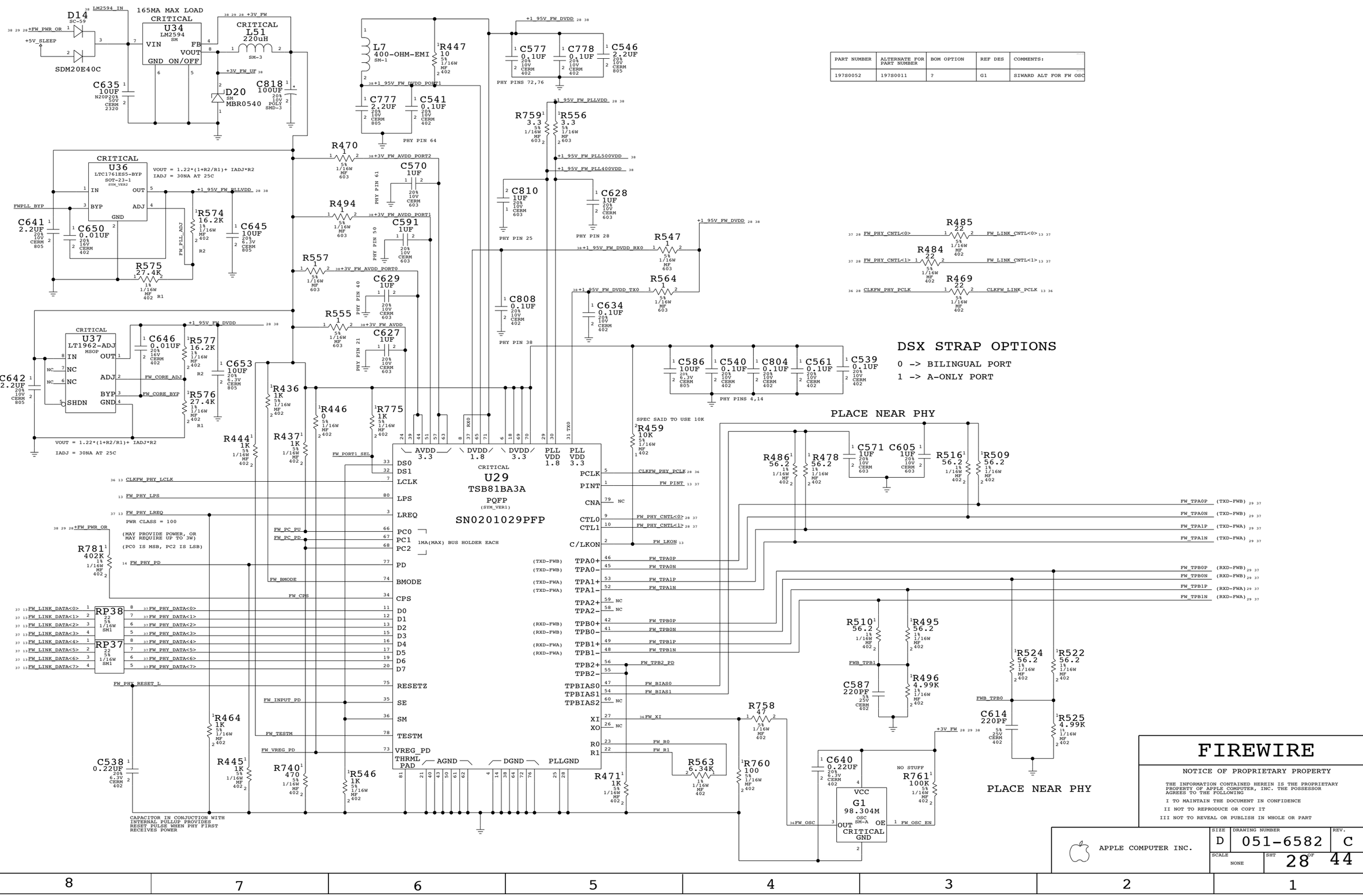
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 27 OF 44	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0052	197S0011	?	G1	SIWARD ALT FOR FW OSC

FIREWIRE

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

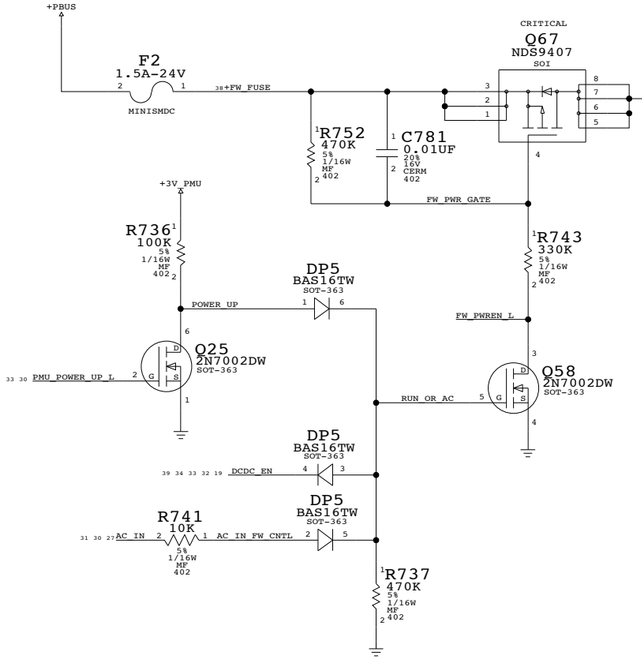
II NOT TO REPRODUCE OR COPY IT

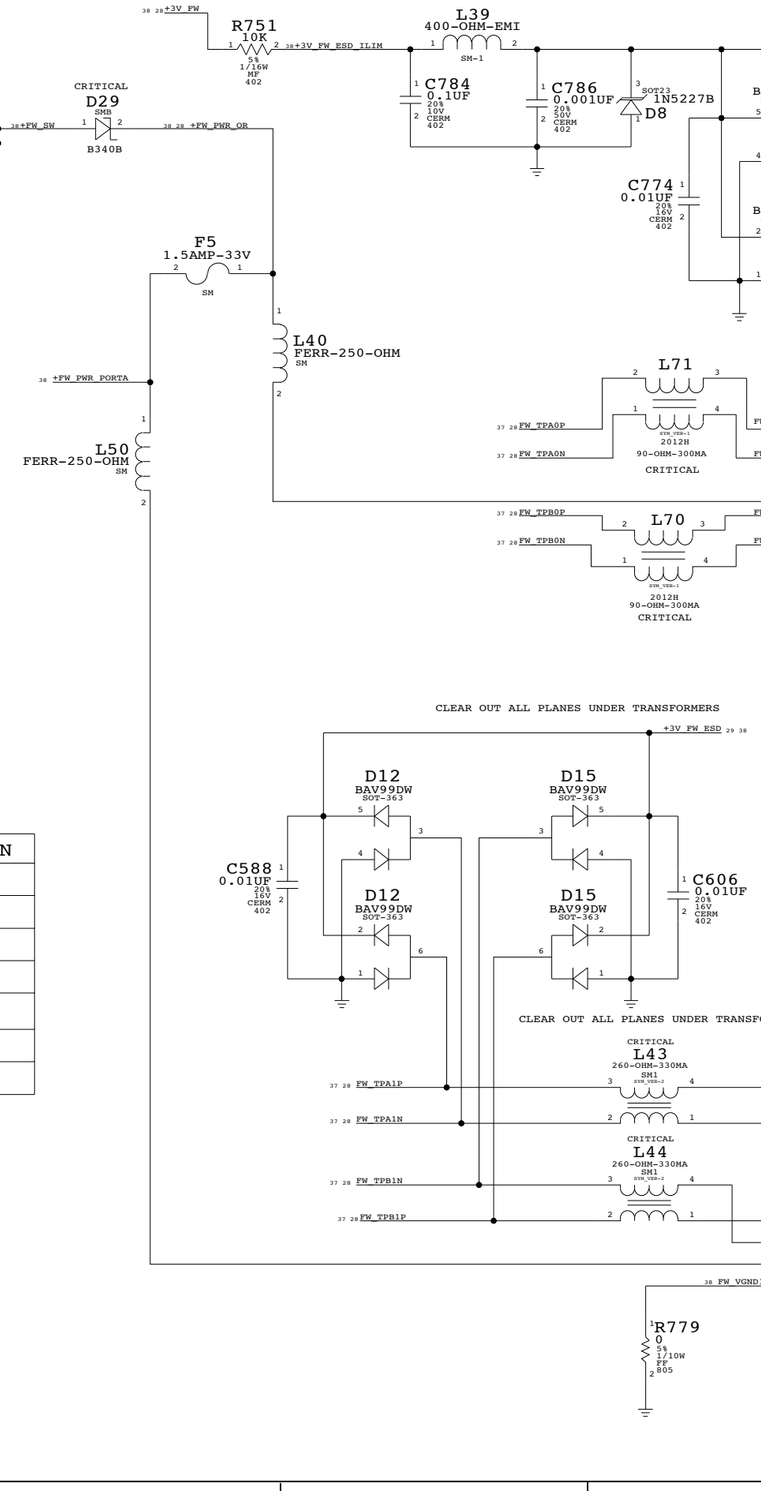
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 28 OF 44	

PORT POWER SWITCH





AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

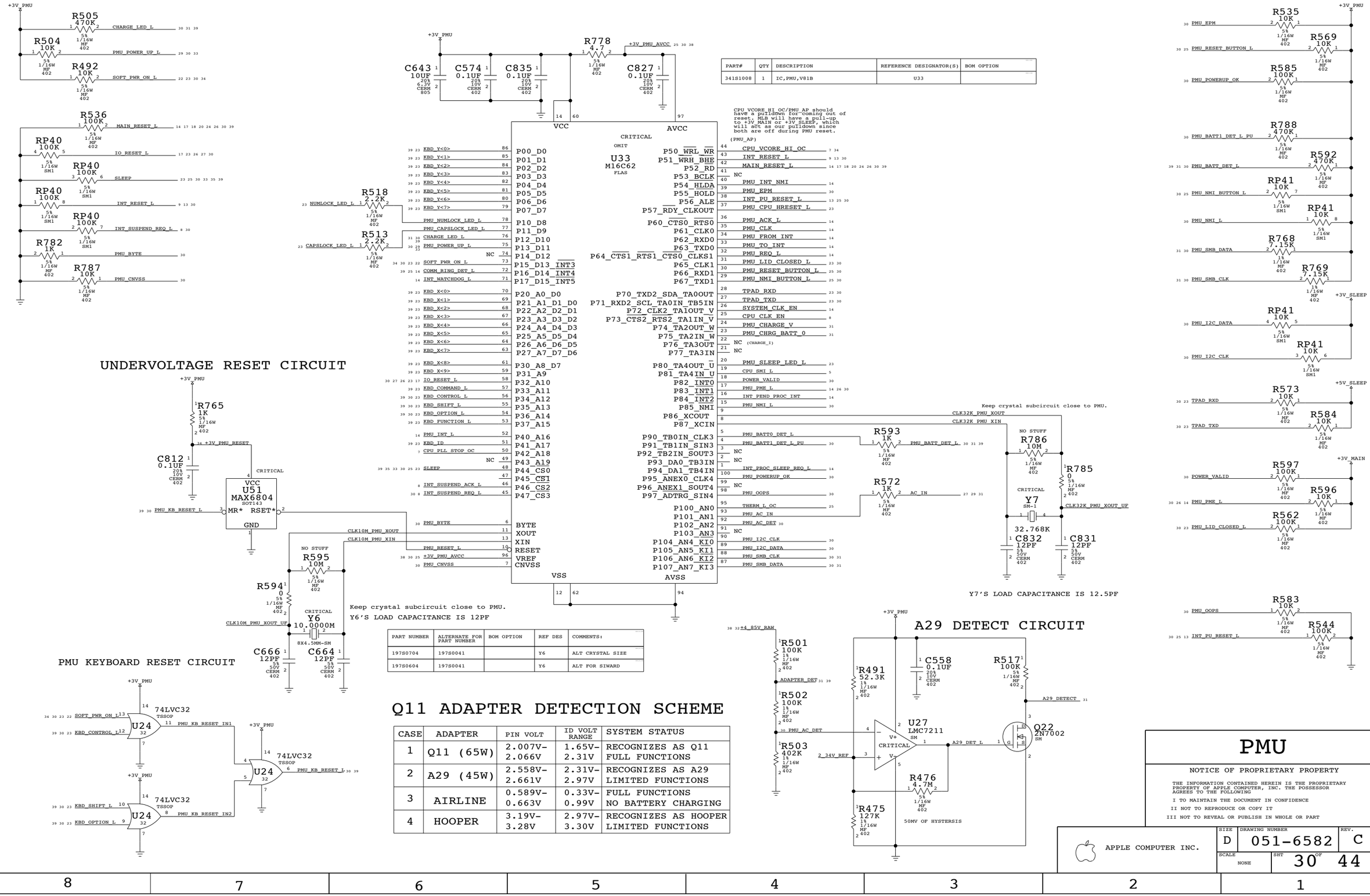
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 29 OF 44	


+3V_PMU
R505 470K CHARGE_LED_L
R504 10K PMU_POWER_UP_L
R492 10K SOFT_PWR_ON_L
R536 100K MAIN_RESET_L
RP40 100K IO_RESET_L
RP40 100K SLEEP
RP40 100K INT_RESET_L
RP40 100K INT_SUSPEND_REQ_L
R782 1K PMU_BYTE
R787 10K PMU_CNVSS
C643 10UF
C574 0.1UF
C835 0.1UF
R778 4.7
+3V_PMU_AVCC
C827 0.1UF
VCC
AVCC
CRITICAL
OMIT
U33
M16C62
FLAS
P00_D0
P01_D1
P02_D2
P03_D3
P04_D4
P05_D5
P06_D6
P07_D7
P10_D8
P11_D9
P12_D10
P13_D11
P14_D12
P15_D13_INT3
P16_D14_INT4
P17_D15_INT5
P20_A0_D0
P21_A1_D1_D0
P22_A2_D2_D1
P23_A3_D3_D2
P24_A4_D4_D3
P25_A5_D5_D4
P26_A6_D6_D5
P27_A7_D7_D6
P30_A8_D7
P31_A9
P32_A10
P33_A11
P34_A12
P35_A13
P36_A14
P37_A15
P40_A16
P41_A17
P42_A18
P43_A19
P44_CS0
P45_CS1
P46_CS2
P47_CS3
BYTE
XOUT
XIN
RESET
VREF
CNVSS
VSS
P50_WRL_WR
P51_WRH_BHE
P52_RD
P53_BCLK
P54_HLDA
P55_HOLD
P56_ALE
P57_RDY_CLKOUT
P60_CTS0_RTS0
P61_CLK0
P62_RXD0
P63_TXD0
P64_CTS1_RTS1_CTS0_CLKS1
P65_CLK1
P66_RXD1
P67_TXD1
P70_TXD2_SDA_TA0OUT
P71_RXD2_SCL_TA0IN_TB5IN
P72_CLK2_TA1OUT_V
P73_CTS2_RTS2_TA1IN_V
P74_TA2OUT_W
P75_TA2IN_W
P76_TA3OUT
P77_TA3IN
P80_TA4OUT_U
P81_TA4IN_U
P82_INT0
P83_INT1
P84_INT2
P85_NMI
P86_XCOUT
P87_XCIN
P90_TB0IN_CLK3
P91_TB1IN_SIN3
P92_TB2IN_SOUT3
P93_DA0_TB3IN
P94_DA1_TB4IN
P95_ANEX0_CLK4
P96_ANEX1_SOUT4
P97_ADTRG_SIN4
P100_AN0
P101_AN1
P102_AN2
P103_AN3
P104_AN4_KI0
P105_AN5_KI1
P106_AN6_KI2
P107_AN7_KI3
AVSS
CPU_VCORE_HI_OC
INT_RESET_L
MAIN_RESET_L
PMU_INT_NMI
PMU_EPM
INT_PU_RESET_L
PMU_CPU_HRESET_L
PMU_ACK_L
PMU_CLK
PMU_FROM_INT
PMU_TO_INT
PMU_REQ_L
PMU_LID_CLOSED_L
PMU_RESET_BUTTON_L
PMU_NMI_BUTTON_L
TPAD_RXD
TPAD_TXD
SYSTEM_CLK_EN
CPU_CLK_EN
PMU_CHARGE_V
PMU_CHRG_BATT_0
PMU_SLEEP_LED_L
CPU_SMI_L
POWER_VALID
PMU_PME_L
INT_PEND_PROC_INT
PMU_NMI_L
INT_PROC_SLEEP_REQ_L
PMU_POWERUP_OK
PMU_OOPS
THERM_L_OC
PMU_AC_IN
PMU_AC_DET
PMU_I2C_CLK
PMU_I2C_DATA
PMU_SMB_CLK
PMU_SMB_DATA
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
PMU_BATT0_DET_L
PMU_BATT1_DET_L_PU
PMU_BATT_DET_L
AC_IN
CPU VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.
(PMU_AP)
NC (CHARGE_I)
Keep crystal subcircuit close to PMU.
Y7'S LOAD CAPACITANCE IS 12.5PF
R535 10K PMU_EPM
R569 10K PMU_RESET_BUTTON_L
R585 100K PMU_POWERUP_OK
R788 470K PMU_BATT1_DET_L_PU
R592 470K PMU_BATT_DET_L
RP41 10K PMU_NMI_BUTTON_L
RP41 10K PMU_NMI_L
R768 7.15K PMU_SMB_DATA
R769 7.15K PMU_SMB_CLK
+3V_SLEEP
RP41 10K PMU_I2C_DATA
RP41 10K PMU_I2C_CLK
+5V_SLEEP
R573 10K TPAD_RXD
R584 10K TPAD_TXD
+3V_MAIN
R597 100K POWER_VALID
R596 10K PMU_PME_L
R562 100K PMU_LID_CLOSED_L
R583 10K PMU_OOPS
R544 100K INT_PU_RESET_L
R518 2.2K NUMLOCK_LED_L
R513 2.2K CAPSLOCK_LED_L
PMU_NUMLOCK_LED_L
PMU_CAPSLOCK_LED_L
CHARGE_LED_L
PMU_POWER_UP_L
SOFT_PWR_ON_L
COMM_RING_DET_L
INT_WATCHDOG_L
KBD_Y<0>
KBD_Y<1>
KBD_Y<2>
KBD_Y<3>
KBD_Y<4>
KBD_Y<5>
KBD_Y<6>
KBD_Y<7>
KBD_X<0>
KBD_X<1>
KBD_X<2>
KBD_X<3>
KBD_X<4>
KBD_X<5>
KBD_X<6>
KBD_X<7>
KBD_X<8>
KBD_X<9>
IO_RESET_L
KBD_COMMAND_L
KBD_CONTROL_L
KBD_SHIFT_L
KBD_OPTION_L
KBD_FUNCTION_L
PMU_INT_L
KBD_ID
CPU_PLL_STOP_OC
SLEEP
INT_SUSPEND_ACK_L
INT_SUSPEND_REQ_L
PMU_BYTE
PMU_RESET_L
+3V_PMU_AVCC
PMU_CNVSS
UNDERVOLTAGE RESET CIRCUIT
R765 1K
C812 0.1UF
+3V_PMU_RESET
U51 MAX6804 SOT143
MR* RSET*
GND
PMU_KB_RESET_L
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
NO STUFF
R595 10M
R594 0
CRITICAL
Y6 10.0000M 8X4.5MM-SM
CLK10M_PMU_XOUT_UF
C666 12PF
C664 12PF
Keep crystal subcircuit close to PMU.
Y6'S LOAD CAPACITANCE IS 12PF
PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:
197S0704 | 197S0041 | | Y6 | ALT CRYSTAL SIZE
197S0604 | 197S0041 | | Y6 | ALT FOR SIWARD
PMU KEYBOARD RESET CIRCUIT
74LVC32 TSSOP U24
SOFT_PWR_ON_L
KBD_CONTROL_L
KBD_SHIFT_L
KBD_OPTION_L
PMU_KB_RESET_IN1
PMU_KB_RESET_IN2
PMU_KB_RESET_L
Q11 ADAPTER DETECTION SCHEME
CASE | ADAPTER | PIN VOLT | ID VOLT RANGE | SYSTEM STATUS
1 | Q11 (65W) | 2.007V-2.066V | 1.65V-2.31V | RECOGNIZES AS Q11 FULL FUNCTIONS
2 | A29 (45W) | 2.558V-2.661V | 2.31V-2.97V | RECOGNIZES AS A29 LIMITED FUNCTIONS
3 | AIRLINE | 0.589V-0.663V | 0.33V-0.99V | FULL FUNCTIONS NO BATTERY CHARGING
4 | HOOPER | 3.19V-3.28V | 2.97V-3.30V | RECOGNIZES AS HOOPER LIMITED FUNCTIONS
A29 DETECT CIRCUIT
+4.85V_RAW
R501 100K
ADAPTER_DET
R502 100K
PMU_AC_DET
R503 402K
2.34V_REF
R491 52.3K
C558 0.1UF
R517 100K
A29_DETECT
U27 LMC7211 SM CRITICAL
A29_DET_L
Q22 2N7002 SM
R476 4.7M
R475 127K
50MV OF HYSTERSIS
PART# | QTY | DESCRIPTION | REFERENCE DESIGNATOR(S) | BOM OPTION
341S1008 | 1 | IC,PMU,V81B | U33 |
PMU
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6582
REV. C
SCALE NONE
SHT 30 OF 44

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL

J18
87438-0833
M-RT-SM

CHARGE_LED_L
+ADAPTER
ADAPTER_DET

NO STUFF
C757 0.1UF 20% 50V CERM 805

PLACE CLOSE TO DC INPUT

R396 20K 1% 1/16W MF 402

DC INRUSH LIMITER

R414 330K 5% 1/16W MF 402
C458 0.1UF 20% 50V CERM 805

Q13 SI4435DY SOI
Q16 SI4435DY SOI

+ADAPTER_SW
+ADAPTER_SENSE
AC_ENABLE_GATE
BCKFD_PROT_GATE
BCKFD_PROT_EN_L

R474 47K 5% 1/16W MF 402
R499 68K 5% 1/16W MF 402
R374 470K 5% 1/16W MF 402
AC_ENABLE_L

Q10 2N7002DW SOT-363
Q21 2N7002DW SOT-363

+3V_PMU
1V20_REF
AC_IN
AC_DIV

R395 102K 1% 1/16W MF 402
R364 102K 1% 1/16W MF 402
C468 0.01UF 20% 16V CERM 402
R363 10K 5% 1/16W MF 402
U15 LMC7211 SM
CRITICAL
R394 1M 5% 1/16W MF 402
AC_IN_L
R375 10K 1% 1/16W MF 402
R365 57.6K 1% 1/16W MF 402
Q10 2N7002DW SOT-363
R383 470K 5% 1/16W MF 402

GREATER THAN 13.5V DETECT

PLACE U23 NEXT TO R460

U23 SENSE VOLTAGE DROP ACROSS R460

C572 0.01UF 20% 50V CERM 603

U23 MAX4172 TSSOP
RS+ RS-
NC1 PG
NC2 OUT
GND
CRITICAL
NC NC MAX4172_OUT

+24V_PBUS
R454 2.21K 0.1% 1/16W MF 603
C883 0.1UF 10% 50V X7R 603-1
CURRENT_THRESHOLD

R460 0.025 1% 1W MF 2512
IF A29 ADAPTER USED, ADJUST CURRENT SETTING

R488 4.7 5% 1/16W MF 402
R498 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN

C578 0.47UF 10% 50V CERM 1206
C579 0.47UF 10% 50V CERM 1206

R754 100K 1% 1/16W MF 402
D9 1N914 SOT23
R755 12.7K 1% 1/16W MF 402
C600 1UF 20% 50V CERM1 1210

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP

U31 MAX1772 QSOP
CRITICAL
CSSP CSSN
DCIN CELLS
ACIN LDO
ACOK DLOV
RFIN BST
VCTL DHI
ICTL LX
ICHG DLO
IINP PGND (GND)
CSIP
CSIN
BATT
REF = 4.096V
REF CLS GND

1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
1772_CSIP
1772_CSIN

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R526 1K 1% 1/16W MF 402
C622 0.01UF 20% 16V CERM 402
C616 0.01UF 20% 16V CERM 402
1772_CCV_RC
R497 1K 1% 1/16W MF 402
C621 0.1UF 20% 10V CERM 402
1772_REF
C630 1UF 20% 10V CERM 603
R487 10K 1% 1/16W MF 402
R473 4.12K 1% 1/16W MF 402
1772_CLS
1772_GND

C652 1UF 20% 10V CERM 603
R559 100K 5% 1/16W MF 402

R542 1K 1% 1/16W MF 402
R566 1K 1% 1/16W MF 402
R565 48.7K 1% 1/16W MF 402
R560 4.12K 1% 1/16W MF 402
R561 100K 5% 1/16W MF 402
R580 5.23K 1% 1/16W MF 402
BATT_LOW_L
BATTV_HIGH
BATTV_LOW
PMU_CHARGE_V
Q27 2N7002DW SOT-363
Q29 2N7002DW SOT-363

1MSEC INTEGRATION TIME

R742 1K 1% 1/16W MF 402
C771 0.1UF 20% 10V CERM 402
IAC_RC_COMP
C772 0.1UF 20% 10V CERM 402
R747 42.2K 0.1% 1/16W FF 603
U50 LMC7111 SOT23-5
CRITICAL
IAC_FB
DP4 BAS16TW SOT-363
R358 150 1% 1/16W MF 402
LTC1625_ITH
PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
ADAPTER_I_REG
R466 10K 1% 1/16W MF 402

R738 42.2K 0.1% 1/16W FF 603
R734 82.5K 0.1% 1/16W FF 603
A29_CURRENT_ADJ
R739 51.1K 0.1% 1/16W FF 603
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
R748 100K 5% 1/16W MF 402
OVER_18V_ADJ
Q20 2N7002DW SOT-363
A29_DETECT
AC_GTR_18V
C775 1UF 20% 10V CERM 603
Q65 2N7002DW SOT-363
1772_ACOK_L

R571 33 5% 1/8W FF 1206
D10 1N914 SOT23
1772_LDO
1772_BST_ESR
R549 100K 5% 1/16W MF 402
C624 0.1UF 20% 25V CERM 603
R774 4.7 5% 1/16W MF 603

C608 0.1UF 20% 50V CERM 805

+24V_PBUS
Q63 IRF7805 SM
CRITICAL
Q64 IRF7811W SO-8
CRITICAL
NO STUFF
C906 0.0022UF 10% 50V CERM 402
XW19 SM

C547 2.2UF 10% 50V CERM 1812
C562 2.2UF 10% 50V CERM 1812
C563 2.2UF 10% 50V CERM 1812
C557 2.2UF 10% 50V CERM 1812
C564 2.2UF 10% 50V CERM 1812

L42 10uH SM1
CRITICAL
D30 SM MBRS140T3
R763 0.05 1% 1W MF 2512
+BATT_RSNS
+BATT_24V_FUSE
R543 1 5% 1/16W MF 603
R511 1 5% 1/16W MF 603
C619 4.7UF 20% 25V CERM 1206
C632 4.7UF 20% 25V CERM 1206
C631 4.7UF 20% 25V CERM 1206
C633 4.7UF 20% 25V CERM 1206
C617 4.7UF 20% 25V CERM 1206
C618 4.7UF 20% 25V CERM 1206
C824 33UF 20% 25V ELEC SM1

BATTERY SWITCH-OVER CIRCUIT

+BATT
F4 5AMP-125V SM-2
F3 5AMP-125V SM-2
+24V_PBUS
+PBUS
+BATT_24V_FUSE
+BATT_14V_FUSE
CRITICAL
Q24 SI4435DY SOI
Q76 SUD45P03 TO-252
R490 47K 5% 1/16W MF 402
R746 47K 5% 1/16W MF 402
BATT_24V_GATE
BATT_14V_GATE
R512 10K 5% 1/16W MF 402
R744 10K 5% 1/16W MF 402
DP4 BAS16TW SOT-363
BATT_24PBUS_EN
BATT_14PBUS_EN
Q21 2N7002DW SOT-363
AC_IN_L
DP4 BAS16TW SOT-363
R489 158K 1% 1/16W MF 402
AC_IN_L_RC
C593 10UF 20% 6.3V CERM 805

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

R567 27.4K 1% 1/16W MF 402
R558 10K 1% 1/16W MF 402
R548 10K 1% 1/16W MF 402
R578 100K 5% 1/16W MF 402
Q30 2N7002DW SOT-363
CHARGE_DISABLE
PMU_CHRG_BATT_0

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

C615 0.1UF 20% 10V CERM 402
U38 LMC7211 SM
CRITICAL
BATT_LOW
R588 100K 1% 1/16W MF 402
R579 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R599 100K 1% 1/16W MF 402
R570 100K 1% 1/16W MF 402
C658 0.047uF 10% 16V CERM 402

R749 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q65 2N7002DW SOT-363
A29_DETECT

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

CRITICAL
J25
87438-0833
M-RT-SM

+BATT_VSNS
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L9 FERR-EMI-100-OHM SM
L53 FERR-50-OHM SM
L10 FERR-EMI-100-OHM SM
L8 FERR-EMI-100-OHM SM
L12 FERR-50-OHM SM
PMU_SMB_CLK
PMU_SMB_DATA

BATTERY CHARGER

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

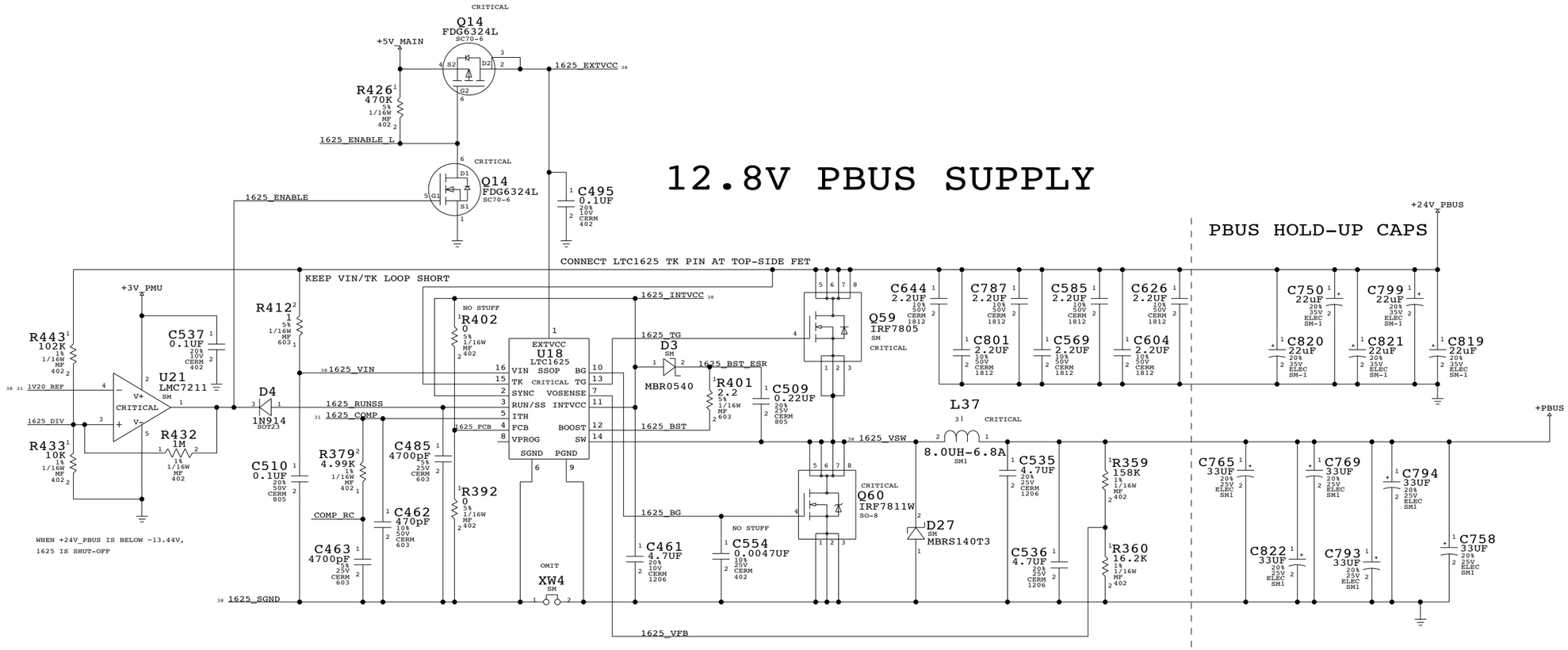
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

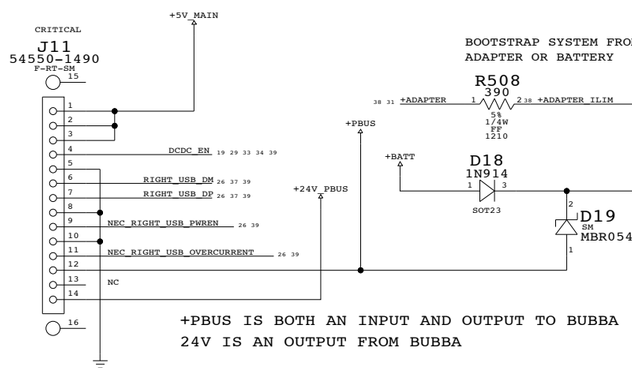
SIZE D | DRAWING NUMBER 051-6582 | REV. C

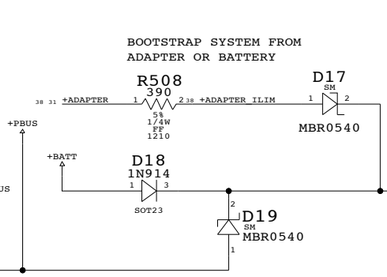
SCALE NONE | SHT 31 OF 44

12.8V PBUS SUPPLY

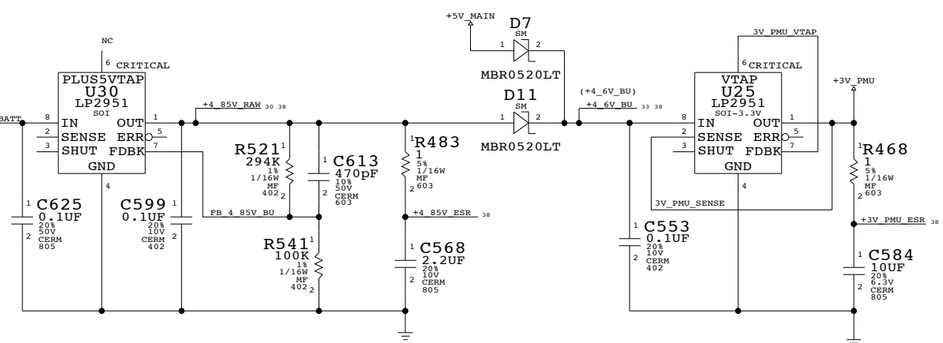


BACKUP BATTERY / USB CONNECTOR





PMU SUPPLY



12.8V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

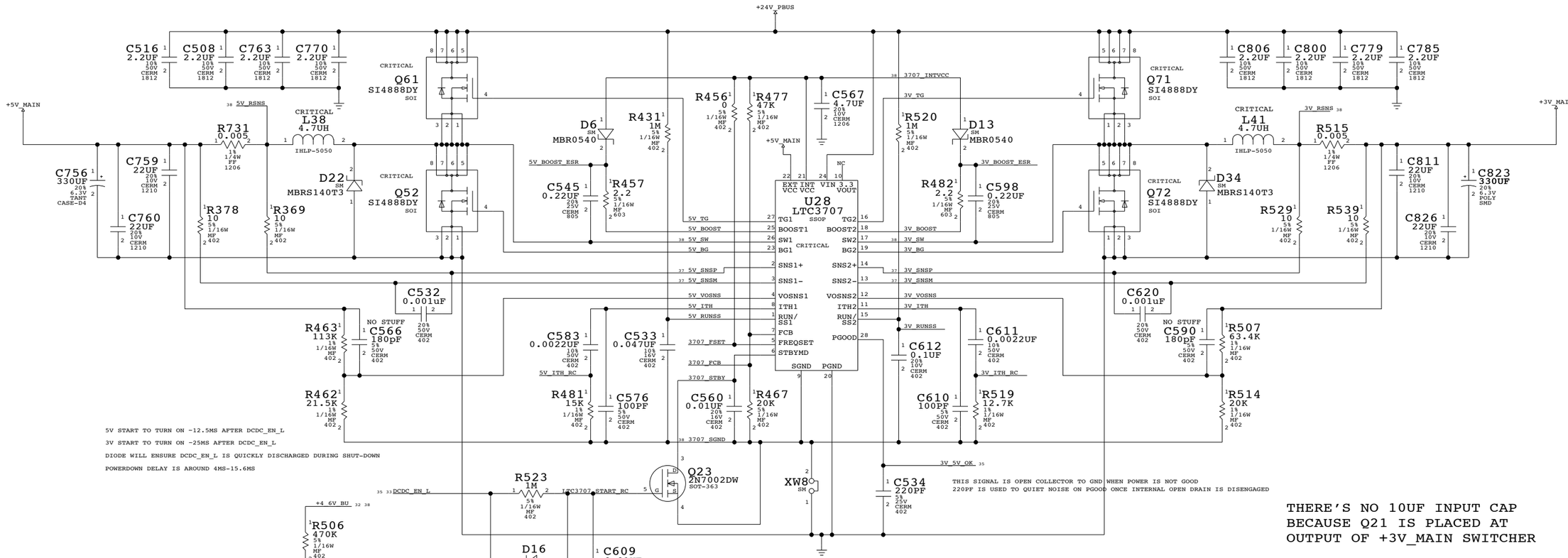
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C

SCALE: NONE

SHT 32 OF 44

3.3V/5V MAIN SUPPLY



5V START TO TURN ON -12.5MS AFTER DCDC_EN_L

3V START TO TURN ON -25MS AFTER DCDC_EN_L

DIODE WILL ENSURE DCDC_EN_L IS QUICKLY DISCHARGED DURING SHUT-DOWN

POWERDOWN DELAY IS AROUND 4MS-15.6MS

3.3V/5V REGULATOR

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 33 OF 44	

VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.175V -> 1.025V 1.30V -> 1.10V

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0022	128S0034	?	C728,C729,C730,C731,C732,C733,C734,C884,C885	

FMAX CONNECTOR

CRITICAL
NO STUFF
J5
M-ST-SM-52465-1217

NC (RFU)

VCORE SUPPLY

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 34 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE
2) AGP I/O IF USING D3HOT

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES
5) CLOCK SLEWING I/O
6) PCI1510 CORE

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD
2) INTREPID MEMORY I/O

THERE'S 100K PULL-UP ON PG 31 ALREADY

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

CHANGE R424 BACK TO 10K, 1%, AND STUFF 5.11K FOR 1.5V OPERATION
CONNECTING 1_5V_FB TO GND, FORCES 1.8V OUTPUT

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7450 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps
4) OPTIONAL VIDEO MEMORY (M10 PRO ONLY)

CONTINUOUS MODE

BURST MODE
NO STUFF

1.5V/1.8V/2.5V SUPPLIES

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 35 OF 44	

DIGITAL SIGNALS

GROUP	SIG_NAME		MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L				250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>		5		250			83 MHZ	5 8
	CPU_ARTRY_L				250.0000	10 MIL SPACING			5 8
	CPU_BG_L				250.0000	10 MIL SPACING			5 8
	CPU_BR_L				250.0000	10 MIL SPACING			5 8
	CPU_CI_L		5		250.0000				5 8
	CPU_DATA<0..31>		5		250			83 MHZ	6 8
	CPU_DATA<32..63>		5		250			83 MHZ	6 8
	CPU_DBG_L		5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>		5		250				5 8
	CPU_DRDY_L_UF					10 MIL SPACING			
	CPU_DRDY_L				250.0000	10 MIL SPACING			5 8
	CPU_GBL_L		5		250.0000				5 8
	CPU_HIT_L				250.0000	10 MIL SPACING			5 8
	CPU_QACK_L		5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L				250.0000	10 MIL SPACING			5 8
	CPU_TA_L				250.0000	10 MIL SPACING			5 8
	CPU_TBST_L		5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L				250.0000				5 8
	CPU_TS_L				250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>		5		250				5 8
	CPU_TT<0...4>		5		250				5 8
	CPU_WT_L		5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>		4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>		4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>		4		200			167 MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET			200				9 10
	RAM_DQS_A<0>		4		200				10 11
	RAM_DQS_B<0>		4		200				10 11
	MEM_DQM<0>		4		200				9 10
	RAM_DQM_A<0>		4		200				10 11
	RAM_DQM_B<0>		4		200				10 11
GROUP 1	MEM_DATA<15..8>		4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>		4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>		4		200			167 MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<1>		4		200				10 11
	RAM_DQS_B<1>		4		200				10 11
	MEM_DQM<1>				200				9 10
	RAM_DQM_A<1>		4		200				10 11
	RAM_DQM_B<1>		4		200				10 11
GROUP 2/3	MEM_DATA<31..16>		4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>		4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>		4		200			167 MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<3..2>		4		200			167 MHZ	10 11
DDR RAM	RAM_DQS_B<3..2>		4		200			167 MHZ	10 11
	MEM_DQM<3..2>		4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>		4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>		4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>		4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>		4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>		4		200			167 MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200			167 MHZ	9 10
	RAM_DQS_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>		4		200			167 MHZ	10 11
	MEM_DQM<5..4>		4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>		4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>		4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>		4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>		4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>		4		200			167 MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<6>				200				10 11
	RAM_DQS_B<6>		4		200				10 11
	MEM_DQM<6>				200				9 10
	RAM_DQM_A<6>		4		200				10 11
	RAM_DQM_B<6>		4		200				10 11
GROUP 7	MEM_DATA<63..56>		4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>		4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>		4		200			167 MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET	4		200				9 10
	RAM_DQS_A<7>				200				10 11
	RAM_DQS_B<7>				200				10 11
	MEM_DQM<7>		4		200				9 10
	RAM_DQM_A<7>		4		200				10 11
	RAM_DQM_B<7>		4		200				10 11
ADDR	MEM_ADDR<12..0>		4					83 MHZ	9
	RAM_ADDR<12..0>		6		200				9 11
	MEM_BA<1..0>		4						9
	RAM_BA<1..0>		6		200				9 11
CONTROL	MEM_CS_L<3..0>		4						9
	RAM_CS_L<3..0>		6		200				9 11
	MEM_CKE<3..0>		4						9
	RAM_CKE<3..0>		6		200				9 11
	MEM_RAS_L		4						9
	RAM_RAS_L				200.0000				9 11
	MEM_CAS_L		4						9
	RAM_CAS_L				200.0000				9 11
	MEM_WE_L		4						9
	RAM_WE_L				200.0000				9 11
	MEM_MUXSEL_H<1..0>		3						9 10
	MEM_MUXSEL_L<1..0>		3						9 10
	RAM_MUXSEL_H		5						10
	RAM_MUXSEL_L		5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10 MIL SPACING		8
	SYSCLK_CPU			4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT			3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM			3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM			3			10 MIL SPACING		8
	INT_CPUFB_LONG			3			10 MIL SPACING		8
	INT_CPUFB_IN					200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN					200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN			4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF					200.0000	10 MIL SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10 MIL SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN			3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT						10 MIL SPACING		
	GPU_CLK27M_UF						10 MIL SPACING		
	GPU_SSCLK_UF						10 MIL SPACING		
	GPU_SSCLK_IN						10 MIL SPACING		
	GPU_FBCLK0						10 MIL SPACING		
	GPU_FBCLK0_L						10 MIL SPACING		
	GPU_FBCLK1						10 MIL SPACING		
	GPU_FBCLK1_L						10 MIL SPACING		
	GPU_DVO_CLKP						10 MIL SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10 MIL SPACING		
	CLK27M_XTAL_IN						10 MIL SPACING		
	CLK27M_GPU_XIN						10 MIL SPACING		
	CLK18M_INT_XIN						10 MIL SPACING		14
	CLK18M_INT_XOUT						10 MIL SPACING		14
	CLK18M_XTAL_IN						10 MIL SPACING		14
	CLK18M_INT_EXT						10 MIL SPACING		14
	CLK25M_ENET_XIN						10 MIL SPACING		27
	CLK25M_ENET_XOUT						10 MIL SPACING		27
	NEC_XT1						10 MIL SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		26
SOUND	SND_SCLK			7		200.0000	10 MIL SPACING		14 25 39
	SND_CLKOUT					200.0000	10 MIL SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10 MIL SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10 MIL SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10 MIL SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10 MIL SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10 MIL SPACING		28
	FW_OSC					200.0000	10 MIL SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 36 OF 44

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHz	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHz	12 18
	AGP_AD_STB<0>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		4	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHz	12 18
	AGP_CBE<3..2>		5	100				66 MHz	12 18
	AGP_AD_STB<1>		4	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHz	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		4	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHz	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHz	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>			NEED TO MATCH DELAY TO 250	200			100 MHz	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHz	13 24
	UIDE_ADDR<2..0>				200			100 MHz	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHz	24
	HD_ADDR<2..0>		5		200			100 MHz	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				27
	MDI_P<0>	ENET_MDI0				27
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2				27
	MDI_M<3>	ENET_MDI3				27
	MDI_P<3>	ENET_MDI3				27
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0		MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0		MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0		MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0		MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0		MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0		MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0		MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0		MIN LINE WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1	500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1	500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1	500.0000	MIN LINE WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1		MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1		MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1		MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1		MIN LINE WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS				31
	1772_CSSP	1772_CSS				31
	1772_CSIN	1772_CSI				31
	1772_CSIP	1772_CSI				31
	3V_SNSM	3V_SNS				33
	3V_SNSP	3V_SNS				33
	5V_SNSM	5V_SNS				33
	5V_SNSP	5V_SNS				33
THERMOSTAT	THERM1_DM	THERM1				25
	THERM1_DP	THERM1				25
	THERM2_DM	THERM2				25
	THERM2_DP	THERM2				25
	THERM1_M_DM	THERM1_MATN				
	THERM1_M_DP	THERM1_MATN				
	THERM2_M_DM	THERM2_MATN				
	THERM2_M_DP	THERM2_MATN				
	THERM1_A_DM	THERM1_ALT				25
	THERM1_A_DP	THERM1_ALT				25
	THERM2_A_DM	THERM2_ALT				25
	THERM2_A_DP	THERM2_ALT				25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.80HM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6582 | REV. C

SCALE NONE | SHT 37 OF 44

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER OR BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND	
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4	39
	CHGND4				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5	
	CHGND5				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6	
	CHGND6				
ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12		27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10 MIN_NECK_WIDTH REDUCED FOR TESTPOINTS	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1331	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1332	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
1333	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1334	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1335	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1336	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
1337	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1338	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1341	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
1340	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1339	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
1342	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
1343	+2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1344	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
1345	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1346	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
1347	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1348	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
1352	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1349	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
1350	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
1351	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	+3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	+3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 13
FUNC_TEST=YES JTAG_ASIC_TDO_TP 27
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36

FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
FUNC_TEST=YES CHGND4 38
FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<10> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<25> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
FUNC_TEST=YES SND_AMP_MUTE 25
FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
FUNC_TEST=YES KBD_X<3> 23 30
FUNC_TEST=YES KBD_X<4> 23 30
FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
FUNC_TEST=YES SRCLK_TP 26
FUNC_TEST=YES SRMOD_TP 26
FUNC_TEST=YES TEB_TP 26
FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
FUNC_TEST=YES KBD_Y<1> 23 30
FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
FUNC_TEST=YES FANR_PWM 25
FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
FUNC_TEST=YES RJ45_DP<3> 27 37
FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TP00R 29 38
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TP01P 29 37
FUNC_TEST=YES FW_TP01N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 32 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
FUNC_TEST=YES INT_MOD_DTI 14 25
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
FUNC_TEST=YES MOD_BITCLK 14 25
FUNC_TEST=YES MOD_CLKOUT 14 25
FUNC_TEST=YES MOD_DTO 14 25
FUNC_TEST=YES MOD_SYNC 14 25
FUNC_TEST=YES SLEEP 23 25 30 33 35
FUNC_TEST=YES 1778_VFB 19 38

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 39 OF 44	

REVISION HISTORY

REV 0.01 - 03/06/2003

3/3
1) Initial check-in of Enterprise schematic after conversion to Concept 14.2

3/10
2) added 8 new 10uF vcore caps
3) added jumpers at 1.5V, 1.8V, 2.5V, 3.3V, 5V, and PBUS supply outputs
4) added 8 more 0.1uF vcore byapass caps

3/11
5) removed dedicated boot banger circuit (U5400,U5200,RP46,U9,U1000)
6) updated firewire to phy to rev A prt number
7) changed cpu PLL config to 1083/833
8) changed reset to U56 (clock slewing chip) to MAIN_RESET_L
9) changed C550 to 138S0536 to limit AVL
10) changed Vcore stuffing options to 1.4V/1.025V using analog mux to support slewing
11) changed stuffing to set Vcore offset to 0mV by default
12) changed comments to eliminate references to L3 in power supply section

3/18
13) changed stuffing options for GPU PCI ID to 0x319
14) changed R164 (DAC1RSET) to 107 ohm pulldown
15) added 10K pulldown to U43 pin A21
16) changed fan controller to ADT7460

3/19
17) added pads for 0.1uF cap from +Adapter to digital gnd for EMC
18) added pads for 0 ohm between chassis and digital gnd near ENET connector for EMC
19) corrected path to correct for last checkin
20) removed BOM table for MAP31
21) REMOVED ALL RELATIVE_PROPAGATION_DELAY AND PROPAGATION_DELAY PROPERTIES TO PRERPARE FOR CONSTRAINT BACK ANNOTATION
22) changed CHGND on R616 to CHGND1
23) ***BOARD RENUMBERED***

3/28
24) integrated M10 pages from Q16 schematic and renumbered them

4/10
25) updated physical constraints for M10 power nets
26) added DP7 for M10 power sequencing
27) added RP27,RP28,RP32, and RP57 for TMDS series termination
28) update PLL CFG high 0010 1.25GHz
low 1011 833MHz
29) update sscg/nosscg stuffing option on intrepid boot straps
30) removed D31 between +Batt and 24V_Pbus
31) add Vcore DAC resistors (R288,R289,R290,R292) for no mux case
32) change intrepid PLL LDO stuffing back to 1.8V main
33) change C640 and C646 to 0.01uF (Apple # 132S1047) for FW check config
34) change I2C pullups (R29 and R102) to 1K
35) changed bootrom part number to 341S1255

4/18
36) changed C756 to 128S0025 (Sanyo only 6.3V 330uF)
37) add pads for 90 ohm chokes to FWB path close to connector (route through the pads)
38) changed Vcore inductor (L36) to molded core part (152S0125)
39) changed Pbus inductor (L37) to molded core part (152S0126)
40) added seperate 1_8V_GPU_TPVDD filter and LDO (U54)

4/21
41) replace disctrete LCL with single chip LCL filters (155S0154) for VGA (L ,L , and L)
42) add 165 ohm chokes on TMDS data pairs at connector (L ,L , and L)
43) move BS1 to bottom side
44) move CPU thermal sensor (Q39) to input 1 on fan controller and power supply sensor (Q66) to input 2
45) added trace from Vcore to fan controller ADC input
46) added FET inverters (Q78) to PWM outputs of fan controller (U3) to prevent spinup at boot
47) added FET (Q79) for +3V_Sleep for M10 power sequencing

4/27
48) changed TMDS data chokes to 90 ohm (155S0128)
49) changed C762 and C766 to 4.7uF 1206 caps
50) changed TMDS data chokes to 90 ohms (155S0128)
51) changed C762 and C766 to 4.7uF 1206
52) changed Q51 to Si7860DP (376S0119)
53) changed Q48 to Si7892DP (376S0120)
54) changed D24 to B340LB (371S0132)
55) changed L30 to 2.2uH Tokin inductor (152S0139)
56) added Q58, R307, and C515 for GPU Vcore control inverter
57) changed R416 to 2.2ohms
58) changed R364 to 102K
59) added 0.1uF 50V C883 to RS- of Max4172 (NO stuff)
60) changed D18 to 1N914
61) changed L38 and L41 to 4.7uH (152S0137)
62) added Q81, R308, R309, and R310 for power sequencing (no stuff)
63) changed Q49 and Q50 to Si7860DP (376S0119)
64) changed L36 to 1.2uH 18.3A (152S0125)
65) added R331 1mohm sense resistor to CPU Vcore
66) added C885 and C884 , 1000uF CPU Vcore outpur caps
67) added Q82, R607, R455, R417, and C886 for 1.5V sleep sequencing
68) added Q83 and 100K R608 for 1.8V sequencing
69) added 15.4K R616 and 10K R672 for 2.5V switcher feedback divider
70) changed pinout of sound connector for sousaphone
71) removed Q44 (5V sound sleep fet)
72) changed Q31 to invert headphone Mute to sousaphone

4/28
73) changed CPU_VCORE_SLEEP location back to across bypass caps to correct after adding reference resistor
74) changed D5 to schottky diode (MBR0540)
75) fixed unnamed net (LTC3411_SHDN_SEQ)
76) changed drain/source polarity of Q76 (FET from +BATT to Pbus)

4/28
77) moved XW15 to connect to CPU_VCORE_SLEEP_UF (before positioning resistor)
78) changed Fan control nets to FanL and FanR from Fan1 and Fan2
79) SWAPPED CONNECTIONS SO THAT OUTPUT 1 FROM FAN CONTROLLER CONNECTS TO LEFT FAN (CPU) AND FAN 2 CONNECTS TO THE RIGHT FAN (GPU)
80) updated power constraints with new fan net names

4/28
81) change Q58 on pg19 to Q80 to consolidate parts
82) CHANGED U55 TO MM1571J FOR COST SAVINGS
83) changed L72,L73,L74 to 90 ohm ferrites
84) added 10K pullup to +5V_MAIN to SND_HP_MUTE
85) repinout Sousaphone connector
86) remore redundant pullups on FANL_TACH and FANR_TACH
87) added TP to all NC on NEC USB2 part for NAND tree testing
88) added NEC_USB bomoption to 0 ohm resistor on NEC_AVSS_F

4/30
89) repinout Sousaphone connector (J12)
90) no stuff R322 to eliminate 3V_sleep pump up
91) updated various text notes with correct reference designators

5/1
92) change L30 to 152S0139 (Tokin CPI-1050-2R2) 11A
93) remove FANR_TACH functional test point
94) add CHGND4 and SLEEP_LED functional test points
95) swap INT_AUDIO_TO_SND and SND_TO_AUDIO on Sousaphone connector (J12)

*** rev 01 released for EVT ***

5/6
96) remove NO STUFF on R477 (set 5V and 3.3V switcher in pulse skipping mode)
97) change R337 to 470K and remove No Stuff and no stuff R336 to change Vcore DAC to 1.35V/1.15V
98) change R321 to 499ohm to set 5mV Vcore offset
99) change L72,L73,L74 to 155S0165 (D part for EVT only)

*** rev 02 released for EVT ***

5/7
100) no stuff Q79 to disable 3V_SLEEP sequencing to work around wake from sleep bug with M10
101) added BOM table to define correct part number for M10 without heatspreader (338S0133)

*** rev 03 released for EVT ***

5/22
102) fixed NO STUFF BOM option for R291
103) add NO STUFF to R223 to correct startup level of GPU_VCORE_CNTL
104) add NO STUFF to R300 to complete 3V sequecing on wake from sleep fix
105) changed R376 to 158K and R321 to 2.74K to set CPU_VCORE offset to 35mV

*** rev 04 released for EVT ***

5/19/03
106) changed both AGP_NV_INT_L and AGP_ATI_INT_L to AGP_INT_L
107) removed redundant 3V_GPU pullup R687 (Intrepid side AGP_INT_L pullup)
108) added R699,R701,R707,R708 as 10k pulldowns to Intrepid USB ports A and C when NEC_USB is stuffed
109) changed SND_HP_MUTE_INV gate/inversion FETS to pullup to +3V_MAIN
110) added R711 as pullup to +3V_GPU on AUXWIN signal from M10 (U44)
111) added R698 as 0 ohm jumper between FW_PHY_PD and Intrepid
112) added U56, U57, R718,R714 for VGA Hsync and VGA Vsync buffering
113) changed L72,L73,L74 to 155S0164 (new high speed part)
114) added NO STUFF BOM option to R223 to correct for sense of GPU_VCORE_CNTL
115) added NO STUFF BOM option to R300 to avoid sleep wake problem

6/3/03
116) Intgrated new 1.8V switcher (LTC3412)(U58)(353S0650) and inductor (L75- 152S0142)
117) changed 2.5V_SLEEP FET (U48) and 1.8V_SLEEP FET (U6) to higher current part (Si6467BDQ - 376S0161)
118) added 10K pulldown (R720) on FW_PHY_PD_INT for when R698 is removed
119) changed R728 and R729 to 1210 0ohm resistors to support switching the entire memory bus between 1.8V and 2.5V
120) added R721 as jumper between +2_5V_SLEEP and +2_5V_GPU

6/4/03
121) NO STUFF R631 to remove MAIN_RESET_L from clock slewing chip
122) changed FWB connector to new part with extra ground tabs (514S0059)

6/5/03
123) changed I2C 0 and 1 pullups (RP12) to 2.2K to improve rise/fall times (sensor check config errors)
124) added CRITICAL flag to new 1.8V switcher (U58), inductor (L75), 1.8V sleep FET (U6), and 2.5V sleep FET (48)
125) removed gnd caps (C651 and C647) on I2S clock at sound connector (J12)
126) added LC filter on SND_SYNC for EMI (L77 and C895)
127) added LC filter on SND_CLKOUT for EMI (80 and C899)
128) added LC filter on INT_AUDIO_TO_SND for EMI (L81 and C896)
129) added LC filter on SND_TO_AUDIO for EMI (L82 and C897)
130) added LC filter on SND_AMP_MUTE for EMI (L76 and C898)
131) added LC filter on SND_HW_RESET_L for EMI (L78 and C900)
132) added LC filter on SND_SCLK for EMI (L79 and C901)
133) added C902 and R804 to prevent latch-up condition in GPU Vcore circuit when using powermiser
134) removed R331 (CPU Vcore positioning resistor)
135) changed C728,C729,C730,C731,C732,C733,C734,C884,C885 to 220uF Rubycon caps (128S0024)
136) add Vcore offset change circuit to modify offset in low (Q86,R805,R806,R807,R808,R809)
137) changed Q83 into dual (2N7002DW) and added R810 to invert 3V_5V_ON before switching RUN/SS

6/6/03
138) rotated J26 (FW B connector)
139) changed D29 to B340B (3A part - 371S0159)

6/9/03
140) modified Vcore offset select circuit with Takashi's changes - changed Gnd reference to VCORE_GND_SNS
141) added double inverter to buffer THERM_L_OC (added Q87,R811,R812)
142) removed redundant pullup on THERM_L_OC (R780)

6/9/03
143) added cap on gate of the second FET in Q87 for possible turn on delay (C903)
144) changed inner shield of FWB connector J26 to connect to chassis gnd
145) changed R336 and R325 to 0 ohm to set Vcore VID to 1.3V/1.15V
146) changed R321 to 2.49K to set Vcore offset to +25mV
147) added 10 ohm resistor (R814) and 1uF cap (C904) to filter power to ADT7460 (Gary Leo)

6/10/03
148) changed R612 to 10K to prevent UIDE DMACK from floating
149) changed C80,C88,C81,C89,C82,C102,C79,C87 to NO STUFF (TMDS common-mode termination)
150) changed R205,R218,R211,R219,R210,R220,R204,R214 to 162 ohm 1% (TMDS common-mode termination)
151) changed RP27,RP32,RP28,RP57 to 10ohm (TMDS series termination)

*** released for EVT2 6/10/03 ***

6/13/03
152) fixed NO STUFF on R291
153) removed NO STUFF from C80,C88,C81,C89,C82,C102,C79,C87 (TMDS common-mode termination
154) removed NO STUFF from R638 (pullup on slewing chip FSEL)
155) removed NO STUFF from C903 (cap on input to second part of THERM_OC_L buffer)
156) CHANGED R321 TO 1K FOR VCORE OFFSET OF 12MV (VCORE = 1.30V -30MV/+100MV)

*** released for EVT2 6/13/03 ***

6/18/03
157) changed R228 to pullup to 1.8V for DVO interface conpatibility
158) added R234 and INT_TMDS option to maintain internal TMDS capability
159) changed L30 to 3 pin symbol
160) added U5 to use as external TMDS transmitter (DVI)
161) added R41 to create +3V_GPU_SI power for SIL1162 (U5)
162) added L14, C130, C132, and C165 for 3V AVCC filtering for SIL1162 (U5)
163) added L13, C14, C129, C131, C133 for 3V PVCC filtering for SIL1162 (U5)
164) added L15, C255, C233, C218 for 3V Vcc filtering for SIL1162 (U5)
165) added R235 and R237 as options for MAIN_RESET_L to U5
166) added R231. R232, and C284 for Vref for U5
167) added R66, R99, R202, R212, R222, R224, R88, R110, R223 as straps for U5
168) added RP58, RP59, RP60, RP61 for series termination of SIL1162 TMDS output
169) added L16, C304, C327, C647 for filtering GPU VDDR4
170) added R255 and R251 to strap GPU_DVODMODE correctly for 1.8V DVO
171) added R268 to connect L16 to +3V_GPU_FLT when not using SIL1162
172) added C681, C668, C678, C651 to filter the thermal sensor diff pairs

6/19/03
173) changed GPU_MEM_IO to +GPU_MEM to connect ATI Vref to correct memory voltage
174) swapped TMDS CLKN and CLKP on RP57 and RP58 for layout
175) swapped DN<0> and DP<0> on RP27 for layout
176) corrected un-named nets in TMDS common-mode filters
177) added physical constriants for new Silicon Image power rails
178) CHANGED C728,C731,C734,C733,C730,C732,C729,C885,C885 TO 128S0022 (124S0024 WILL BE DELETED AS A DUPLICATE IN THE LIBRARY)

6/23/03
179) NO STUFF'ed C895,C899,C896,C897,C898,C900, and C901 to fix no sound problem
180) changed C890 to 100pF for improved transient response (Takashi)
181) Removed bypass traces on FWB chokes and stuffed L70 and L71
182) CHANGED R491 TO 52.3K 1%, R475 TO 127K 1%, AND R476 TO 4.7M 5% IN A29 ADAPTER DETECT CIRCUIT DIVIDERS TO REDUCE SHUTDOWN CURRENT
183) added R331 as CPU Vcore sense resistor (1 mohm 1% 2512)
184) No STUFF'ed C651 and C678
185) added C688,C690,C846,C905 for thermal pair filtering at fan controller
186) added C906 to prevent shoot-thru on Q64 (currently NO STUFF'ed)
187) added C907 to prevent shoot-thru on Q68 (currently NO STUFF'ed)
188) changed R517 to 100K
189) changed GND reference for input side of Q86 to digital GND (the other FET in Q856 remains on VCORE_GNDSNS

6/24/03
190) added C908 to prevent gate shoot-thru on Q56
191) added R279 to power TMDS PLL from LVDS filter when using external TMDS transmitter
192) changed R325 to 470K to set the low Vcore to 1.10V
193) stuffed Vcore offset switch (R807,R805,R809,Q86)
194) changed R809 to 1.5K 1% to set low Vcore offset to 10mV
195) changed R321 to 3.01K 1% to set high Vcore offset to 30mV

6/25/03
196) rotated L70 and L71 for layout (PCB symbol problem)
197) changed Q53,Q54,Q55 to IRF7832 (376S0148) for better thermal performance
198) NO STUFF'ed C908 (Q56 gate shoot-thru cap)

*** released for DVT 6/26/03 ***

7/2/03
199) CHANGED J9 (CARDBUS) TO 516S0141 (NEW PIN PLATING SPEC)
200) CHANGED J20 (AIRPORT) TO 516S0142 (NEW PIN PLATING SPEC)
201) CHANGED J10 (OPTICAL DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
202) CHANGED J13 (HARD DRIVE) TO 516S0140 (NEW PIN PLATING SPEC)
203) CHANGED J12 (SOUND) TO 516S0144 (NEW PIN PLATING SPEC)
204) CHANGED J8 (MODEM) TO 516S0143 (NEW PIN PLATING SPEC)
205) ADDED BOM TABLE TO PUT 0 OHM 402 ON L77,L80,L81,L82,L76,L78,L79

7/9/03
207) CORRECTED C889 TO CONNECT TO INPUT (PIN 1) OF U55
208) REMOVED POWER JUMPERS XW25,XW17,XW16,XW10,XW14,XW18
209) CHANGED 197S0035 TO PRIMARY AND 197S0004 AS ALTERNATE FOR Y1 (INTREPID)
210) CHANGED 197S0037 TO PRIMARY AND 197S0603 AS ALTERNATE FOR Y3 (ETHERNET)
211) CHANGED 197S0038 TO PRIMARY AND 197S0608 AS ALTERNATE FOR Y5 (NEC USB2)
212) CHANGED 197S0040 TO PRIMARY AND 197S0008 AS ALTERNATE FOR Y4 (LMU)
213) CHANGED 197S0041 TO PRIMARY AND 197S0604 AS ALTERNATE FOR Y6 (PMU)

7/22/03
214) ADDED 1_32V_VCORE AND 1_30V_VCORE BOM OPTIONS FOR 2 DIFFERENT CPU VCORE SPECS
215) UPDATED CAP MATERIAL TYPES
216) CHANGED FROM 715 PIN TO 667 PIN SYMBOL FOR U44 (M10)

7/28/03
217) CHANGED TMDS TERMINATION FROM 2X 162 TO 2X 49.9 OHMS PER PAIR
218) CHANGED 126S0036 FROM ALT TO PRIMARY, REPLACING 126S0035 FOR CPU VCORE INPUT CAPS

*** RELEASED FOR PRODUCTION 7/28/03 ***

8/4/03
219) CHANGED R99 TO NO STUFF TO FIX I2C ADDRESS OF SIL1162 TMDS TRANSMITTER
220) CHANGED R321 TO 4.02K 1% FOR 1_30_VCORE (40MV OFFSET) AND TO 6.34K 1% FOR 1_32_VCORE (60MV OFFSET)
221) CHANGED R304 TO 470K AND R329 AND R325 TO 0 OHM TO CHANGE LOW VID TO 1.05V ON VCORE
222) CHANGED C611 TO 2200PF, C610 TO 100PF, AND R519 TO 12.7K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
223) NO STUFF C590 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
224) CHANGED C583 TO 2200PF, C576 TO 100PF, AND R481 TO 15.0K 1% TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT
225) NO STUFF C566 TO INCREASE IMMUNITY TO 3.3V PGOOD SIGNAL DROPOUT

9/4/03
228) ADDED 197S0052 AS ALTERNATE FOR G1 (98 MHZ FW OSCILLATOR)
229) CHANGED C728-C734,C884,C885 TO 128S0022 TO REMOVE DUPLICATE PART NUMBER
230) CHANGED C883 TO 132S0100 TO CORRECT FOR USE OF OEM PART NUMBER

8/29/05
1) ADDED 338S0223 (88E1111, B1) AS OPTION
2) ADDED 128S0034 AS OPTION
3) REPLACED 740S0006 WITH 740S0018

*** PRODUCTION RELEASE FOR 051-6582-B ***

01/04/07
1) PER RADAR #4312710, ADD 338S0336 AS ALTERNATE OF 338S0168.
2) PER RADAR #4312710, REPLACE 341S1336 WITH 341S2103, DUE TO 335SXXXX EOL, WHICH REPORT TO 341S1336.

*** SERVICE BON UPDATE FOR 051-6582-C ***

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

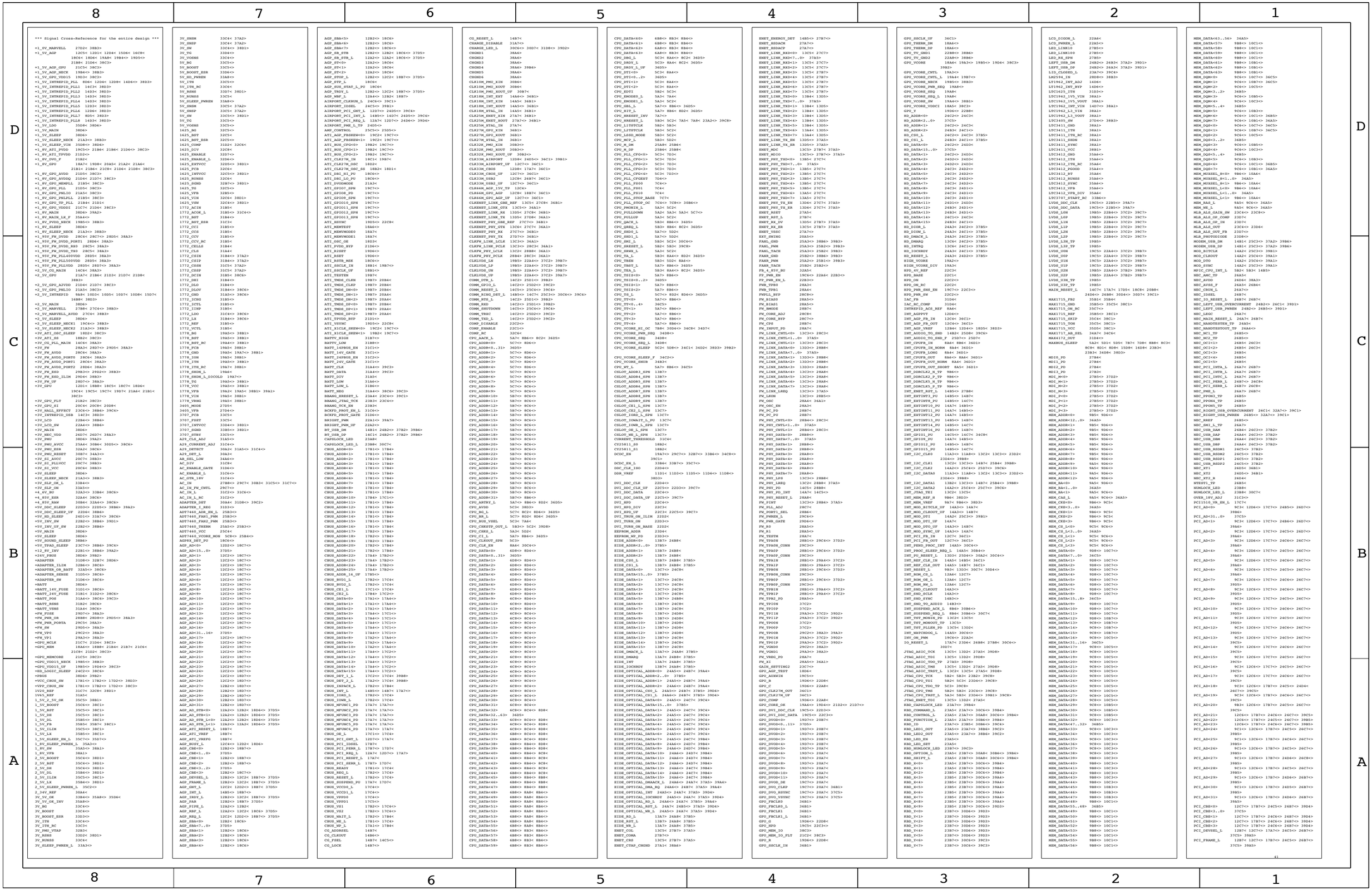
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6582	C
SCALE: NONE	SHT 40 OF 44	


8
7
6
5
4
3
2
1
D
C
B
A
*** Signal Cross-Reference for the entire design ***
+1_0V_MARVELL 27D2< 38B3>
+1_5V_AGP 12C5< 12D1< 12D4< 15D6< 16C8<
18C6< 18D6< 19A8< 19B4< 19D5<
21B8< 21D6< 38C3>
+1_5V_AGP_GPU 21C5< 38C3>
+1_5V_AGP_NECK 19B4< 38B3>
+1_5V_GPU_VDD15 19D3< 38C3>
+1_5V_INTREPID_PLL 8D6< 12D4< 12D8< 14D6< 38D3>
+1_5V_INTREPID_PLL1 14C3< 38D3>
+1_5V_INTREPID_PLL2 14D3< 38D3>
+1_5V_INTREPID_PLL3 14D3< 38D3>
+1_5V_INTREPID_PLL4 14D3< 38D3>
+1_5V_INTREPID_PLL5 12D3< 38D3>
+1_5V_INTREPID_PLL6 12D6< 38D3>
+1_5V_INTREPID_PLL7 8D5< 38D3>
+1_5V_INTREPID_PLL8 14D3< 38D3>
+1_5V_LDO 35D6< 38D6>
+1_5V_MAIN 38D6>
+1_5V_SLEEP 38D6>
+1_5V_SLEEP_NECK 21A3> 38B3>
+1_5V_SLEEP_VIN 35D8> 38D6>
+1_8V_ATI_PVDD 19C5> 21B6< 21B6< 21D6< 38C3>
+1_8V_ATI_TPVDD 21D2<>
+1_8V_DVO_F 21B2<
+1_8V_GPU 18A7> 19D8< 20A5< 21A2< 21A6<
21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1_8V_GPU_AVDD 21D5< 38C3>
+1_8V_GPU_AVDDQ 21D7< 21D7< 38C3>
+1_8V_GPU_MEMPLL 21B5< 38C3>
+1_8V_GPU_PLL 21D5< 38C3>
+1_8V_GPU_PNLIO 21A5< 38C3>
+1_8V_GPU_PNLPLL 21B5< 38C3>
+1_8V_GPU_TX_PLL 21B4< 21D1<
+1_8V_GPU_VDDCI 21C7< 21D4< 38C3>
+1_8V_MAIN 35B4< 39A2>
+1_8V_MAIN_LX_F 35A4<
+1_8V_PVDD_NECK 19B5<> 38B3>
+1_8V_SLEEP 38D6>
+1_8V_SLEEP_NECK 21A3<> 38B3>
+1_95V_FW_DVDD 28C4< 28C7<> 28D5< 38A3>
+1_95V_FW_DVDD_PORT1 28D6< 38A3>
+1_95V_FW_DVDD_RX0 28C5< 38A3>
+1_95V_FW_DVDD_TX0 28D6< 38A3>
+1_95V_FW_PLL400VDD 28D5< 38A3>
+1_95V_FW_PLL500VDD 28D5< 38A3>
+1_95V_FW_PLLVDD 28D3< 28D7<> 38A3>
+2_5V_CQ_MAIN 14C6< 38A3>
+2_5V_GPU 21A7< 21B6< 21D3< 21D7< 21D8<
21D8< 38A3>
+2_5V_GPU_A2VDD 21D4< 21D7< 38C3>
+2_5V_GPU_PNLIO 21A6< 38C3>
+2_5V_INTREPID 9A8< 10D3< 10D6< 10D7< 10D8< 15D7<
16B8< 38D3>
+2_5V_MAIN 38C6>
+2_5V_MARVELL 27B8< 27C4<> 38B3>
+2_5V_MARVELL_AVDD 27C4< 38B3>
+2_5V_SLEEP 38D6>
+2_5V_SLEEP_NECK1 19C4<> 38B3>
+2_5V_SLEEP_NECK2 21A3<> 38B3>
+3V_ATI_OSC_SLEEP 18D2< 38C3>
+3V_ATI_S5 18B2< 38C3>
+3V_CQ_PLL_MAIN 14C4< 38A3>
+3V_FW 28A3> 28D7<> 29D5< 38A3>
+3V_FW_AVDD 28C6< 38A3>
+3V_FW_AVDD_PORT0 28C6< 38A3>
+3V_FW_AVDD_PORT1 28C6< 38A3>
+3V_FW_AVDD_PORT2 28D6< 38A3>
+3V_FW_ESD 29B3<> 29D2<> 38B3>
+3V_FW_RSD_ILIM 29D4< 38B3>
+3V_FW_ST 29D7<> 38A3>
+3V_GPU 12D1< 18B8< 18C5< 18C7< 18D6<
19C3< 19C5< 19C7< 19D7< 21A6< 21B1<
38C3>
+3V_GPU_FLT 21B2< 38C3>
+3V_GPU_SI 20C6< 20C8< 20D8<
+3V_HALL_EFFECT 23C6<> 38B6> 39C4>
+3V_INTREPID_USB 14C2< 38D3>
+3V_LCD 22B4<> 38B6>
+3V_LCD_SW 22A4<> 38B6>
+3V_MAIN 38D6>
+3V_NEC_VDD 26D7< 26D7< 38A3>
+3V_PHU 38D6> 39A2>
+3V_PHU_AVCC 25A4< 30B6< 30D5<> 38C6>
+3V_PHU_ESR 32A2< 38C6>
+3V_PHU_PLLVCC 20C7< 38B3>
+3V_SI_VCC 20C6< 38B3>
+3V_SLEEP 38D6>
+3V_SLEEP_NECK 21A3<> 38B3>
+3V_SLEEP_OR_L 33B4<
+3V_SLP_ENABLE_L 31C6<>
+3V_SLP_OR 33A5<>
+4_0V_BQ 32A2<> 33B6< 38C6>
+4_85V_ESR 32A4< 38C6>
+4_95V_RAW 32B4<> 38C6>
+5V_DDC_SLEEP 22D3<> 22D5<> 38B6> 39A2>
+5V_DDC_SLEEP_UP 22D6< 38B6>
+5V_INTREPID_USB 14C5< 33A7<> 38C6>
+5V_INV_SW 22B2<> 38B6> 39D1>
+5V_INV_UP_SW 22B2<> 38B6>
+5V_MAIN 38D6>
+5V_SLEEP 38D6>
+5V_SOUND_SLEEP 38D6> 38E6>
+5V_TPAD_SLEEP 23C7<> 38B6> 39C4>
+12_8V_INV 22B1<> 38B6> 39A2>
+24V_PBUS 38D6> 39A2>
+ADAPTER 31D8<> 32B7< 38D6>
+ADAPTER_ILIM 32B6<> 38C6>
+ADAPTER_OR_BATT 32A6<> 38C6>
+ADAPTER_SENSE 31D5<> 38C6>
+ADAPTER_SW 31D6<> 38C6>
+BATT 38D6>
+BATT_14V_FUSE 31D1<> 38C6>
+BATT_24V_FUSE 31B5<> 38C6>
+BATT_POS 31A4<> 38C6> 39C3>
+BATT_RSNS 31B2< 38C6>
+BATT_VSNS 31A4< 38C6>
+FW_FUSE 29D7<> 38A3>
+FW_PWR_OR 28D6<> 29D5<> 38A3>
+FW_PWR_PORTA 29C5< 38A3>
+FW_SW 29D5<> 38A3>
+FW_VP0 29C2<> 38A3>
+FW_VP1 29A3<> 38A3>
+GPU_MCLK 21C7< 21D4< 38C3>
+GPU_MEM 18A6<> 18B8< 21B4< 21B7< 21C6<
21C8< 21D2< 38C3>
+GPU_MEMCORE 21C5< 38C3>
+GPU_VDD15_NECK 19B5<> 38B3>
+GPU_VDD15_OF 19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP 23A5<> 38B6>
+PBUS 38D6> 39B2>
+VCC_CBUS_SW 17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW 17B1<> 17B2<> 17D2<> 38C3>
1V20_REF 31C7< 32C8< 38D3>
1V65_REF 31A5<> 38A3>
1_5V_2_5V_OR 35C5> 38B1>
1_5V_BOOST 35C6> 38C1>
1_5V_BST 35C5> 38C1>
1_5V_DH 35C5> 38C1>
1_5V_DL 35B5< 38C1>
1_5V_FB 35B5< 35B7< 38C1>
1_5V_ILIM 35C5> 38C1>
1_5V_LX 35B5< 38C1>
1_5V_SLEEPG_EN_L 35C7<> 35D7<>
1_5V_SLEEP_PWREN_L 35A3<>
1_8V_SW 35A5<> 38A1>
1_8V_VFB 38A1>
2_5V_BOOST 35C4<> 38D1>
2_5V_BST 35C4<> 38D1>
2_5V_DH 35C4<> 38D1>
2_5V_DL 35B4<> 38D1>
2_5V_ILIM 35C5> 38C1>
2_5V_LX 35B4<> 38D1>
2_5V_SLEEP_PWREN_L 35C2<>
2_34V_REF 30A4<
3V_5V_OK 30B4<> 35A8<> 35D6<
3V_5V_OK_INV 35A8<>
3V_BG 33C4<>
3V_BOOST 33C6<>
3V_BOOST_ESR 33D3<>
3V_ITH 33C6<>
3V_ITH_RC 33C3<
3V_PWG_VTAP 32B3<
3V_RSNS 32D4<> 38D1>
3V_RUN8S 33C4<
3V_SLEEP_PWREN_L 33A3<>
3V_SNSM 33C4< 37A2>
3V_SNSP 33C4< 37A2>
3V_SW 33C4<> 38D1>
3V_TG 33D4<>
3V_VOSNS 33C4<>
5V_BG 33C5<>
5V_BOOST 33C5<>
5V_BOOST_ESR 33D4<>
5V_HD_PWREN 33A6<>
5V_ITH 33C5<>
5V_ITH_RC 33C6<
5V_RSNS 33D7< 38D1>
5V_RUN8S 33C5<
5V_SLEEP_PWREN 33A3<>
5V_SW 33C5<> 38D1>
5V_TG 33C5<>
5V_VOSNS 35B4< 38D6>
1625_BG 32C5<>
1625_BST 32C5<
1625_COMP 31D2< 32C6<
1625_DIV 32C8<
1625_ENABLE 32D7<>
1625_ENABLE_L 32D6<>
1625_EXTVCC 32D5<> 38D1>
1625_FCB 32C6<
1625_INTVCC 32C5<> 38D1>
1625_RUN8S 32C6<
1625_SGND 32B7<> 38D1>
1625_TG 32C5<>
1625_VFB 32B5<>
1625_VIN 32C6< 38D1>
1625_VSW 32D5< 38D1>
1772_ACIN 31B5<
1772_ACOK_L 31B5<> 31C4<>
1772_BST 31B4<>
1772_BST_ESR 31C3<
1772_CCI 31B6<>
1772_CCS 31B5<
1772_CCV 31B5<>
1772_CONV_RC 31B5<
1772_CELLS 31B4<
1772_CLS 31A4<>
1772_CSIN 31B4<> 37A2>
1772_CSIP 31B4<> 37A2>
1772_CSIN 31C5< 37A2>
1772_CSSP 31C5< 37A2>
1772_DCIN 31B5< 38C6>
1772_DHI 31B4<>
1772_DLO 31B4<>
1772_DRVCC 31B4<> 38C6>
1772_GND 31A5> 38C6>
1772_ICHG 31B5<>
1772_ICTL 31B6<>
1772_IINP 31B5<
1772_LDO 31C4<> 38C6>
1772_LX 31B4<> 38C6>
1772_REF 31B5<>
1772_VCTL 31B5<
1772_BG 19A5<> 38B1>
1778_BST 19A5<> 38B1>
1778_BST_RC 19A4<> 38B1>
1778_FCB 19A5<> 38B1>
1778_GND 19A5<> 38B1> 38D1>
1778_ION 19A5> 38B1>
1778_ITH 19A5<> 38B1>
1778_ITH_RC 19A7< 38B1>
1778_SHDN_L 19A6<
1778_SHDN_L_D3COLD 19A7<>
1778_TG 19A5<> 38B1>
1778_VCC 19A5<> 38B1>
1778_VFB 19A3< 19A5< 38B1> 39A1>
1778_VIN 19A5< 38B1>
1778_VRNG 19A5< 38B1>
3405_MODE 27D5<
3405_VFB 27D4<>
3405_VSW 27D3<>
3707_FCB 33C5<
3707_ITHYVCC 33D4<> 38D1>
3707_SGND 33B5<> 38D1>
3707_STBY 33C5<>
A29_CLK_ADJ 31A5<>
A29_CURRENT_ADJ 31C4<>
A29_DETECT 30A2< 31A5<> 31C4<>
A29_DET_L 34A4<
AC_DIV 27E4<
AC_ENABLE_GATE 31D6<>
AC_ENABLE_L 31C6<>
AC_GTR_18V 31C4<>
AC_IN 27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL 29C7<>
AC_IN_L 31C2<> 31C6<>
AC_IN_L_RC 31C2<>
ADAPTER_DET 34A4< 31D8<> 39C2>
ADAPTER_I_REG 31D3<>
ADT7460_ADR_EN_L 25B3<>
ADT7460_FAN1_PWM 25B3<>
ADT7460_FAN2_PWM 25B3<>
ADT7460_THERM 25A5<> 25B3<>
ADT7460_VCC 25B3<>
ADT7460_VCORE_MON 5C8<> 25A6<>
AGPBX_DET_PU 18C6<>
AGP_AD<0> 12D2<> 18C7<>
AGP_AD<15..0> 37D5>
AGP_AD<1> 12C2<> 18C7<>
AGP_AD<2> 12C2<> 18C7<>
AGP_AD<3> 12C2<> 18C7<>
AGP_AD<4> 12C2<> 18C7<>
AGP_AD<5> 12C2<> 18C7<>
AGP_AD<6> 12C2<> 18C7<>
AGP_AD<7> 12C2<> 18C7<>
AGP_AD<8> 12C2<> 18C7<>
AGP_AD<9> 12C2<> 18C7<>
AGP_AD<10> 12C2<> 18C7<>
AGP_AD<11> 12C2<> 18C7<>
AGP_AD<12> 12C2<> 18C7<>
AGP_AD<13> 12C2<> 18C7<>
AGP_AD<14> 12C2<> 18C7<>
AGP_AD<15> 12C2<> 18C7<>
AGP_AD<16> 12C2<> 18C7<>
AGP_AD<31..16> 37D5>
AGP_AD<17> 12C2<> 18C7<>
AGP_AD<18> 12C2<> 18C7<>
AGP_AD<19> 12C2<> 18C7<>
AGP_AD<20> 12C2<> 18C7<>
AGP_AD<21> 12C2<> 18C7<>
AGP_AD<22> 12C2<> 18C7<>
AGP_AD<23> 12C2<> 18C7<>
AGP_AD<24> 12C2<> 18C7<>
AGP_AD<25> 12C2<> 18D7<>
AGP_AD<26> 12C2<> 18D7<>
AGP_AD<27> 12B2<> 18D7<>
AGP_AD<28> 12B2<> 18D7<>
AGP_AD<29> 12B2<> 18D7<>
AGP_AD<30> 12B2<> 18D7<>
AGP_AD<31> 12B2<> 18D7<>
AGP_BBA<0> 12B2<> 18C6>
AGP_BBA<1> 12B2<> 18C6>
AGP_BBA<2> 12B2<> 18C6>
AGP_BBA<3> 12B2<> 18C6>
AGP_BBA<4> 12B2<> 18C6>
AGP_BBA<5> 12B2<> 18C6>
AGP_BBA<6> 12B2<> 18C6>
AGP_BBA<7> 12B2<> 18C6>
AGP_BB_STB 12B2<> 12C2< 18C6> 37D5>
AGP_BB_STB_L 12A2<> 12C2< 18C6> 37D5>
AGP_BUSY_L 12A2<> 18C6>
AGP_DBI_HI 12A2<> 18C6>
AGP_DBI_LO 12A2<> 18C6>
AGP_ST0 12A2<> 18C6>
AGP_ST1 12A2<> 18C6>
AGP_ST2 12A2<> 18C6>
AGP_STOP_L 12A2<> 18C6>
AGP_STP_L 18C6<
AGP_SYS_STRAT_L_PU 18C6<>
AGP_TRDY_L 12B2<> 12C2< 18B7<> 37D5>
AGP_WBF_L 12A4<> 12B2< 18B7>
AIRPORT_DISRUN_L 34A3<>
AIRPORT_IDSEL 24C5<> 39B1>
AIRPORT_PCI_GNT_L 24D5<> 39C4>
AIRPORT_PCI_INT_L 14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L 12A7< 12D7<> 24D6<> 39C4>
AIRPORT_PME_L_TP 24D5<> 39C4>
AMP_CONTROL 25C5<> 25D5<>
ATI_AGP_FBEKEN<0> 19C2< 19C7<>
ATI_AGP_FBEKEN<1> 19C2< 19C7<>
ATI_BUS_CFG<0> 19B2< 19C7<>
ATI_BUS_CFG<1> 19B2< 19C7<>
ATI_BUS_CFG<2> 19B2< 19C7<>
ATI_CLK27_IN 18C1< 19B7<
ATI_CLK27M_OSC 18D2<
ATI_CLK27M_OSC_SS 18B2< 18D1<
ATI_DBI_HI_PU 18C6<>
ATI_DBI_LO_PU 18C6<>
ATI_DVODMODE 21A3<
ATI_GPIO7_ESR 19C7<>
ATI_GPIO8_PD 19C7<>
ATI_GPIO9_SPN 19C7<>
ATI_GPIO10_SPN 19C7<>
ATI_GPIO11_SPN 19C7<>
ATI_GPIO12_SPN 19C7<>
ATI_GPIO13_SPN 19C7<>
ATI_HSYNC 19D5<> 22C8<
ATI_MEMTEST 18A7<
ATI_MEMVMODE0 18A7<
ATI_MEMVMODE1 18A7<
ATI_OSC_OE 19A6<
ATI_PVDD_BYP 21D6<>
ATI_R2SET 19D6<>
ATI_RSET 19D6<>
ATI_RSTB_MEK 18C6<>
ATI_SSCLK_IN 18C1< 19B7<>
ATI_SSCLK_UP 18B1<>
ATI_TESTEN 19B7<
ATI_TMDS_CLKN 19B7> 20B4<
ATI_TMDS_CLKP 19B7> 20B4<
ATI_TMDS_DN<0> 19B7> 20B4<
ATI_TMDS_DN<1> 19B7> 20A4<
ATI_TMDS_DN<2> 19B7> 20A4<
ATI_TMDS_DP<0> 19B7> 20B4<
ATI_TMDS_DP<1> 19B7> 20A4<
ATI_TMDS_DP<2> 19B7> 20A4<
ATI_TPVDD_BYP 21D2<>
ATI_VSYNC 19D5<> 22C8<
ATI_X1CLK_SKEW<0> 19B2< 19C7<>
ATI_X1CLK_SKEW<1> 19B2< 19C7<>
BATTV_HIGH 31B7<>
BATTV_OUT 31B6<> 38C6>
BATT_14FBOB_EN 31C1<>
BATT_24FBOB_EN 31C2<>
BATT_24FBOB_EN_GND 31C2<>
BATT_24V_GATE 31C1<>
BATT_CLK 31A4<> 39C3>
BATT_DATA 31A4<> 39C3>
BATT_DIV 31A5<
BATT_LOW 31A6<>
BATT_LOW_L 31B6<>
BATT_NEG 31A4<> 38C6> 39C3>
BBANG_HRESET_L 23A4< 23C4<> 39C1>
BBANG_JTAG_TCK 23B3< 23C4<>
BBANG_TCK_EN 23B3<
BCKFB_PROT_EN_L 31C6<>
BCKFB_PROT_GATE 31D6<>
BRIGHT_PWM 22A1<> 39A7>
BRIGHT_PWM_UF 22A2<>
BT_USB_DN 14B1< 24B2<> 37B2> 39B6>
BT_USB_DP 14C1< 24B2<> 37B2> 39B6>
CAPSLOCK_LED 23A6<
CAPSLOCK_LED_L 23B6< 30C7<
CBUS_ADDR<0> 17B1<> 17B4>
CBUS_ADDR<1> 17B1<> 17B4>
CBUS_ADDR<2> 17B1<> 17B4>
CBUS_ADDR<3> 17B1<> 17B4>
CBUS_ADDR<4> 17B1<> 17B4>
CBUS_ADDR<5> 17B1<> 17B4>
CBUS_ADDR<6> 17B1<> 17B4>
CBUS_ADDR<7> 17B1<> 17B4>
CBUS_ADDR<8> 17B1<> 17B4>
CBUS_ADDR<9> 17B1<> 17B4>
CBUS_ADDR<10> 17B4< 17C1<>
CBUS_ADDR<11> 17B2< 17B4>
CBUS_ADDR<12> 17B1<> 17B4>
CBUS_ADDR<13> 17B1<> 17B4>
CBUS_ADDR<14> 17B1<> 17B4>
CBUS_ADDR<15> 17B1<> 17B4>
CBUS_ADDR<16> 17B1<> 17B4>
CBUS_ADDR<17> 17B1<> 17B4>
CBUS_ADDR<18> 17B2< 17B4>
CBUS_ADDR<19> 17B2< 17B4>
CBUS_ADDR<20> 17B2< 17B4>
CBUS_ADDR<21> 17B2< 17B4>
CBUS_ADDR<22> 17B2< 17B4>
CBUS_ADDR<23> 17A4< 17B2>
CBUS_ADDR<24> 17A4< 17B2>
CBUS_ADDR<25> 17A4< 17B2>
CBUS_ADDR_16_UF 17B5<>
CBUS_BVD1_L 17B2> 17C4<
CBUS_BVD2_L 17B2> 17C4<
CBUS_CE1_L 17C1< 17C4>
CBUS_CE2_L 17B4< 17C2>
CBUS_DATA<0> 17A1<> 17A4>
CBUS_DATA<1> 17A1<> 17A4>
CBUS_DATA<2> 17A1<> 17C1<>
CBUS_DATA<3> 17A4< 17C1<>
CBUS_DATA<4> 17A4< 17C1<>
CBUS_DATA<5> 17A4< 17C1<>
CBUS_DATA<6> 17A4< 17C1<>
CBUS_DATA<7> 17A4< 17C1<>
CBUS_DATA<8> 17A2< 17A4<>
CBUS_DATA<9> 17A2< 17A4<>
CBUS_DATA<10> 17A2< 17A4<>
CBUS_DATA<11> 17A4< 17C2<>
CBUS_DATA<12> 17A4< 17C2<>
CBUS_DATA<13> 17A4< 17C2<>
CBUS_DATA<14> 17A4< 17C2<>
CBUS_DATA<15> 17A4< 17C2<>
CBUS_DET_1_L 17C2> 17C4< 39B8>
CBUS_DET_2_L 17A2> 17C4< 39B8>
CBUS_INPACK_L 17B2> 17B4<
CBUS_INT_L 14B5> 14B7< 17A7<>
CBUS_IOMD_L 17B2> 17C4>
CBUS_IOWR_L 17B2> 17C4>
CBUS_MFUNC1_PD 17A7< 17C7<>
CBUS_MFUNC2_PD 17A7< 17A7<>
CBUS_MFUNC3_PD 17A7< 17A7<>
CBUS_MFUNC4_PD 17A7< 17A7<>
CBUS_MFUNC5_PD 17A7< 17A7<>
CBUS_MFUNC6_PD 17A7< 17A7<>
CBUS_OE_L 17C1< 17C4>
CBUS_PCI_GNT_L 12D7< 17A7<
CBUS_PCI_IDSEL 17B7< 17C4>
CBUS_PCI_PERR_L 17B7> 17D7<
CBUS_PCI_REQ_L 12A7< 12D7<> 17A7>
CBUS_PCI_RESET_L 17A7<
CBUS_PCI_SERR_L 17B7> 17D7<
CBUS_READY 17B1<> 17C4<
CBUS_REG_L 17B2> 17C4>
CBUS_RESET_L 17B2> 17C4>
CBUS_SUSPEND_PD 17A7> 17D7<
CBUS_VCCD0_L 17C4<>
CBUS_VCCD1_L 17C4<>
CBUS_VPPD0 17C4<>
CBUS_VPPD1 17C5<>
CBUS_VS1 17B2<> 17C4<>
CBUS_VS2 17B2> 17C4<>
CBUS_WAIT_L 17B2> 17B4<
CBUS_WE_L 17B1<> 17C4>
CBUS_WP_L 17A1<> 17B4<
CG_ADDRSEL 14B7<
CG_CLKOUT 14B6<>
CG_FBEL 14B7< 14C5<>
CG_LOCK 14B7<>
CO_RESET_L 14B7<
CHARGE_DISABLE 31A7<>
CHARGE_LED_L 30C6<> 30D7< 31D8<> 39D2>
CHGND1 38A6>
CHGND2 38A6>
CHGND3 38A6>
CHGND4 38A6> 39B6>
CHGND5 38A6>
CHGND6 38A6>
CLK10M_PMU_XIN 30B6<
CLK10M_PMU_XOUT 30B6<
CLK10M_PMU_XOUT_UF 30B7<
CLK18M_INT_EXT 14A6<> 36B1>
CLK18M_INT_XIN 14A5< 36B1>
CLK18M_INT_XOUT 14A5<> 36B1>
CLK18M_XTAL_IN 14A5< 36B1>
CLK25M_ENET_XIN 27A7< 36B1>
CLK25M_ENET_XOUT 27A7<> 36B1>
CLK25M_XTAL_IN 27A7<
CLK27M_GPU_XIN 36B1>
CLK27M_GPU_XOUT 36B1>
CLK27M_XTAL_IN 36B1>
CLK32K_PMU_XIN 30B3<>
CLK32K_PMU_XOUT 30B3<>
CLK32K_PMU_XOUT_UF 30B2<>
CLK33M_AIRPORT 12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF 12C7<> 36C1>
CLK33M_CBUS 12D8< 17A7< 36C1>
CLK33M_CBUS_UF 12C7<> 36C1>
CLK33M_USB2 12C8< 26B7< 36C1>
CLK33M_USB2_UF 12C7<> 36C1>
CLK66M_AGP_15V_UF 12C7<>
CLK66M_GPU_AGP 12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF 12C7<> 36C1>
CLKENET_LINK_GPU_REF 13C5< 27C8< 36B1>
CLKENET_LINK_GTX 13C5<> 36B1>
CLKENET_LINK_RX 13D5< 27C8< 36B1>
CLKENET_LINK_TX 13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF 27C7<> 36B1>
CLKENET_PHY_GTX 13C6< 27C7< 36A1>
CLKENET_PHY_RX 27C7<> 36B1>
CLKENET_PHY_TX 27D7<> 36B1>
CLKFW_ILINK_GTX 13C3<> 36A1>
CLKFW_ILINK_PCLK 13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK 28B4< 28B6< 36A1>
CLKFW_PHY_PCLK 28B4> 28C3< 36A1>
CLKLVDS_LN 19B5> 22A4<> 37C2> 39B7>
CLKLVDS_LP 19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UN 19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP 19B5> 22A4<> 37C2> 39A7>
COMM_GPIO_L 14C2<> 25D2<> 39C2>
COMM_INPACK_L 14C2<> 25D1<> 39C2>
COMM_RING_DET_L 14B5> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L 14C2> 25D1<> 39B2>
COMM_TXD 14C2<> 25D1<> 39B2>
COMM_SHUTDOWN 14C5<> 25C4<> 39C4>
COMM_TXRC 14C2<> 25D2<> 39C2>
COMM_TXD_L 14C2<> 25D2<> 39C2>
COMP_DISABLE 22C2<>
COMP_ENABLE 22C1<>
COMP_RC 32C6<
CPU_AACK_L 5A7< 8B6<> 8C2< 36D5>
CPU_ADDRV0 5B7< 8B6<>
CPU_ADDR<0..31> 36D5>
CPU_ADDR<1> 5C7> 8D6<>
CPU_ADDR<2> 5C7<> 8D6<>
CPU_ADDR<3> 5C7<> 8D6<>
CPU_ADDR<4> 5C7<> 8D6<>
CPU_ADDR<5> 5C7<> 8C6<>
CPU_ADDR<6> 5C7<> 8C6<>
CPU_ADDR<7> 5C7<> 8C6<>
CPU_ADDR<8> 5C7<> 8C6<>
CPU_ADDR<9> 5C7<> 8C6<>
CPU_ADDR<10> 5B7<> 8C6<>
CPU_ADDR<11> 5B7<> 8C6<>
CPU_ADDR<12> 5B7<> 8C6<>
CPU_ADDR<13> 5B7<> 8C6<>
CPU_ADDR<14> 5B7<> 8C6<>
CPU_ADDR<15> 5B7<> 8C6<>
CPU_ADDR<16> 5B7<> 8C6<>
CPU_ADDR<17> 5B7<> 8C6<>
CPU_ADDR<18> 5B7<> 8C6<>
CPU_ADDR<19> 5B7<> 8C6<>
CPU_ADDR<20> 5B7<> 8C6<>
CPU_ADDR<21> 5B7<> 8C6<>
CPU_ADDR<22> 5B7<> 8C6<>
CPU_ADDR<23> 5B7<> 8C6<>
CPU_ADDR<24> 5A7<> 8C6<>
CPU_ADDR<25> 5A7<> 8C6<>
CPU_ADDR<26> 5A7<> 8C6<>
CPU_ADDR<27> 5A7<> 8C6<>
CPU_ADDR<28> 5A7<> 8C6<>
CPU_ADDR<29> 5A7<> 8C6<>
CPU_ADDR<30> 5A7<> 8C6<>
CPU_ADDR<31> 5A7<> 8B6<>
CPU_ADSTB_L 5B7<> 8D6<>
CPU_ADSTB_UL 5B7<> 8D6<>
CPU_BG_L 5C7< 8C2< 8D6<> 36D5>
CPU_BR_L 5C7> 8D2< 8D6<> 36D5>
CPU_BUS_VSEL 5C3< 7A6<
CPU_CHRSTP_OUT_L 5B3<> 5C2< 39D8>
CPU_CHSG_L 5A3< 5D2<
CPU_C1_L 5A7> 8B6<> 36D5>
CPU_CLKOUTFLEX_SPN 5C3>
CPU_CLK_EN 8A6< 30C4<>
CPU_DATA<0> 6D8<> 8D4<>
CPU_DATA<0..31> 36D5>
CPU_DATA<1> 6D8<> 8D4<>
CPU_DATA<2> 6D8<> 8D4<>
CPU_DATA<3> 6D8<> 8D4<>
CPU_DATA<4> 6D8<> 8D4<>
CPU_DATA<5> 6D8<> 8D4<>
CPU_DATA<6> 6D8<> 8D4<>
CPU_DATA<7> 6D8<> 8D4<>
CPU_DATA<8> 6D8<> 8D4<>
CPU_DATA<9> 6C8<> 8D4<>
CPU_DATA<10> 6C8<> 8D4<>
CPU_DATA<11> 6C8<> 8D4<>
CPU_DATA<12> 6C8<> 8C4<>
CPU_DATA<13> 6C8<> 8C4<>
CPU_DATA<14> 6C8<> 8C4<>
CPU_DATA<15> 6C8<> 8C4<>
CPU_DATA<16> 6C8<> 8C4<>
CPU_DATA<17> 6C8<> 8C4<>
CPU_DATA<18> 6C8<> 8C4<>
CPU_DATA<19> 6C8<> 8C4<>
CPU_DATA<20> 6C8<> 8C4<>
CPU_DATA<21> 6C8<> 8C4<>
CPU_DATA<22> 6C8<> 8C4<>
CPU_DATA<23> 6C8<> 8C4<>
CPU_DATA<24> 6C8<> 8C4<>
CPU_DATA<25> 6C8<> 8C4<>
CPU_DATA<26> 6C8<> 8C4<>
CPU_DATA<27> 6C8<> 8C4<>
CPU_DATA<28> 6C8<> 8C4<>
CPU_DATA<29> 6C8<> 8C4<>
CPU_DATA<30> 6C8<> 8C4<>
CPU_DATA<31> 6C8<> 8C4<>
CPU_DATA<32>,<63> 36D5>
CPU_DATA<33> 6C8<> 8C4<> 8D8<
CPU_DATA<34> 6C8<> 8C4<> 8D8<
CPU_DATA<35> 6C8<> 8C4<> 8D8<
CPU_DATA<36> 6B8<> 8C4<> 8D8<
CPU_DATA<37> 6B8<> 8C4<> 8D8<
CPU_DATA<38> 6B8<> 8B4<> 8D8<
CPU_DATA<39> 6B8<> 8B4<> 8D8<
CPU_DATA<40> 6B8<> 8B4<> 8C8<
CPU_DATA<41> 6B8<> 8B4<> 8C8<
CPU_DATA<42> 6B8<> 8B4<> 8C8<
CPU_DATA<43> 6B8<> 8B4<> 8C8<
CPU_DATA<44> 6B8<> 8B4<> 8B8<
CPU_DATA<45> 6B8<> 8B4<> 8B8<
CPU_DATA<46> 6B8<> 8B4<> 8B8<
CPU_DATA<47> 6B8<> 8B4<> 8B8<
CPU_DATA<48> 6B8<> 8A8< 8B4<>
CPU_DATA<49> 6B8<> 8A8< 8B4<>
CPU_DATA<50> 6B8<> 8A8< 8B4<>
CPU_DATA<51> 6B8<> 8A8< 8B4<>
CPU_DATA<52> 6B8<> 8A8< 8B4<>
CPU_DATA<53> 6B8<> 8A8< 8B4<>
CPU_DATA<54> 6B8<> 8A8< 8B4<>
CPU_DATA<55> 6B8<> 8A8< 8B4<>
CPU_DATA<56> 6B8<> 8B3< 8B4<>
CPU_DATA<57> 6B8<> 8B3< 8B4<>
CPU_DATA<58> 6B8<> 8B3< 8B4<>
CPU_DATA<59> 6B8<> 8B3< 8B4<>
CPU_DATA<60> 6B8<> 8B3< 8B4<>
CPU_DATA<61> 6B8<> 8B3< 8B4<>
CPU_DATA<62> 6A8<> 8B3< 8B4<>
CPU_DATA<63> 6A8<> 8B3< 8B4<>
CPU_DBG_L 5C3> 8A4<> 8C2< 36D5>
CPU_DRDY_L 5C3> 8A4< 8C2< 36D5>
CPU_DRDY_L_UF 36D5>
CPU_DTI<0> 5C3< 8A4<>
CPU_DTI<2> 5C3< 8A4<>
CPU_EDTI 5B2< 5C3<
CPU_EMODE0_L 5A3< 7A4<
CPU_EMODE1_L 5A5< 5C2<
CPU_GBL_L 5A7> 8B6<> 36D5>
CPU_HIT_L 5A5< 8B6< 8D2< 36D5>
CPU_HRESET_INV 7A7<>
CPU_HRESET_L 5B3< 5C2< 7A5< 7A8< 23A2<> 39C8>
CPU_L1TSTCLK 5B2< 5B3<
CPU_L2TSTCLK 5B3< 5C2<
CPU_LSSD_MODE 5B3< 5D2<
CPU_MCP_TX_EN 13D5<> 37A5>
CPU_M_DM 25A8< 25B6<
CPU_M_DP 25B6< 25B8<
CPU_PLL_CFG<0> 5C3< 7D3<
CPU_PLL_CFG<1> 5C3< 7D3<
CPU_PLL_CFG<2> 5C3< 7D3<
CPU_PLL_CFG<3> 5C3< 7D3<
CPU_PLL_CFG<4> 5C3< 7D3<>
CPU_PLL_DET 12C8< 26B7< 36C1>
CPU_PLL_FS00 7C4<>
CPU_PLL_FS01 7C4<>
CPU_PLL_FS10 7C4<
CPU_PLL_STOP_BASE 7C7<>
CPU_PLL_STOP_OC 7C4<> 7C8<> 30B6<>
CPU_PMONIN_L 5A3< 5C2<
CPU_PULLDOWN 5A< 5A3< 5C7<>
CPU_PULLUP 5A3< 5C2<
CPU_QACK_L 5B3> 8B6<> 36D5>
CPU_QREQ_L 5B3< 8B6< 8C2< 36D5>
CPU_SDID_L 5A7> 5D2<
CPU_SDID_L 5A7> 5D2<
CPU_SMI_L 25A3<> 38B6> 39B3>
CPU_SRESET_L 5B2< 5B3< 39C8>
CPU_SWR_L 5A3< 5D2<
CPU_TA_L 5B3< 8A4<> 8D2< 36D5>
CPU_TBEN 5B3< 5D2< 8A6<>
CPU_TRST_L 5A7< 8B6<> 36D5>
CPU_TEA_L 5B3< 8A4<> 8C2< 36D5>
CPU_TSI2<0> 5A7> 8B6<>
CPU_TSI2<0..2> 36D5>
CPU_TSI1K<1> 5A7> 8B6<>
CPU_TSI2K<1> 5A7> 8B6<>
CPU_TS_L 5C7<> 8D2< 8D4<> 36D5>
CPU_TT<0> 5A7< 8B6<>
CPU_TT<0..4> 36C5>
CPU_TT<1> 5A7< 8B6<>
CPU_TT<2> 5A7< 8B6<>
CPU_TT<3> 5A7< 8B6<>
CPU_TT<4> 5A7< 8B6<>
CPU_VCORE_HI_OC 7C5<> 34C8< 34D7<
CPU_VCORE_PWR_SEQ 34D8<>
CPU_VCORE_SEQ 34D8<
CPU_VCORE_SEQ_L 34D8<
CPU_VCORE_SLEEP 5C2< 5D8<> 34C1< 34D2< 38D3> 39B2>
CPU_VCORE_SL

```
PCI_IRDY_L          12B7< 12C7<> 17B7<> 24C6<> 26B7<>
                  37C5> 39A5>
PCI_PAR             12C7<> 17B7<> 24C5<> 26B7<> 37C5>
                  39D4>
PCI_STOP_L          12A7< 12C7<> 17B7<> 24C5<> 26B7<>
                  37C5> 39A5>
PCI_TRDY_L          12B7< 12C7<> 17A7<> 24C5<> 26B7<>
                  37C5> 39A5>
PLL_STOP_L          7C4<> 7C8<>
PMU_ACK_L           14C2< 30C4<>
PMU_AC_DET          30A4< 30B4<>
PMU_AC_IN           30B4<>
PMU_BATT0_DET_L     30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<
PMU_BATT_DET_L      30B3< 30D2< 31A4<> 39C3>
PMU_BYTE            30B6< 30C7<
PMU_CAPSLOCK_LED_L  30C6<>
PMU_CHARGE_V        30C4<> 31B8<>
PMU_CHRG_BATT_0     30C4<> 31A8<>
PMU_CLK             14C2<> 30C4<>
PMU_CNVSS           30B6< 30C7<
PMU_CPU_HRESET_L    23A4< 23C4<> 30C4<>
PMU_EPM             30D2< 30D4<>
PMU_FROM_INT        14C2<> 30C4<>
PMU_I2C_CLK         30B4<> 30C2<
PMU_I2C_DATA        30B4<> 30C2<
PMU_INT_L           14B5<> 14B7< 30B6<>
PMU_INT_NMI         14B5<> 14B7< 30D4<>
PMU_KB_RESET_IN1    30A7<>
PMU_KB_RESET_IN2    30A7<>
PMU_KB_RESET_L      30A6> 30B7< 39B2>
PMU_LID_CLOSED_L    23A8< 23C4<> 30B2< 30C4<>
PMU_NMI_BUTTON_L    25C1< 30C2< 30C4<>
PMU_NMI_L           30C2< 30C4<>
PMU_NUMLOCK_LED_L   30C6<>
PMU_OOPS            30B2< 30B4<>
PMU_PME_L           14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK      30B4<> 30D2<
PMU_POWER_UP_L      29C7<> 30C6<> 30D7< 33B8<
PMU_REQ_L           14B7< 14C2> 30C4<>
PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L         30B6<>
PMU_SLEEP_LED       23C4<>
PMU_SLEEP_LED_L     23C2<> 30C4<>
PMU_SMB_CLK         30B4<> 30C2< 31A3<
PMU_SMB_DATA        30B4<> 30C2< 31A2<
PMU_TO_INT          14C2<> 30C4<>
POWER_UP            29C7<>
POWER_VALID         30B2< 30C4<>
PWR_BUTTON_L        23A7<> 25C2< 39B2>
RAM_ADDR<0>         9B4< 11B5<> 11B6<>
RAM_ADDR<12..0>     36A5>
RAM_ADDR<1>         9B4< 11B3<> 11B8<>
RAM_ADDR<2>         9B4< 11B5<> 11B6<>
RAM_ADDR<3>         9B4< 11B3<> 11B8<>
RAM_ADDR<4>         9B4< 11B5<> 11B6<>
RAM_ADDR<5>         9B4< 11B3<> 11B8<>
RAM_ADDR<6>         9B4< 11B5<> 11B6<>
RAM_ADDR<7>         9B4< 11B3<> 11B8<>
RAM_ADDR<8>         9B4< 11B5<> 11B6<>
RAM_ADDR<9>         9A4< 11B3<> 11B8<>
RAM_ADDR<10>        9A4< 11B3<> 11B8<>
RAM_ADDR<11>        9A4< 11B5<> 11B6<>
RAM_ADDR<12>        9A4< 11B3<> 11B8<>
RAM_BA<0>           9A4< 11B3<> 11B8<>
RAM_BA<1..0>        36A5>
RAM_BA<1>           9A4< 11B5<> 11B6<>
RAM_CAS_L           9A4< 11B5<> 11B6<> 36A5>
RAM_CKE<0>          9A3< 9C4< 11B6<>
RAM_CKE<3..0>       36A5>
RAM_CKE<1>          9A3< 9C4< 11B8<>
RAM_CKE<2>          9A3< 9C4< 11C5<>
RAM_CKE<3>          9A3< 9C4< 11C3<>
RAM_CS_L<0>         9C4< 11B8<>
RAM_CS_L<3..0>      36A5>
RAM_CS_L<1>         9C4< 11B6<>
RAM_CS_L<2>         9C4< 11B3<>
RAM_CS_L<3>         9C4< 11B5<>
RAM_DATA_A<0>       10C8<> 11D8<>
RAM_DATA_A<7..0>    36C5>
RAM_DATA_A<1>       10C8<> 11D8<>
RAM_DATA_A<2>       10C8<> 11D8<>
RAM_DATA_A<3>       10B8<> 11D8<>
RAM_DATA_A<4>       10B8<> 11D6<>
RAM_DATA_A<5>       10B8<> 11D6<>
RAM_DATA_A<6>       10B8<> 11D6<>
RAM_DATA_A<7>       10B8<> 11D6<>
RAM_DATA_A<8>       10B8<> 11D8<>
RAM_DATA_A<15..8>   36C5>
RAM_DATA_A<9>       10C7<> 11D8<>
RAM_DATA_A<10>      10C7<> 11D8<>
RAM_DATA_A<11>      10C7<> 11D8<>
RAM_DATA_A<12>      10C7<> 11D6<>
RAM_DATA_A<13>      10C7<> 11D6<>
RAM_DATA_A<14>      10C7<> 11D6<>
RAM_DATA_A<15>      10C7<> 11D6<>
RAM_DATA_A<16>      10C6<> 11D8<>
RAM_DATA_A<31..16>  36B5>
RAM_DATA_A<17>      10C6<> 11C8<>
RAM_DATA_A<18>      10C6<> 11C8<>
RAM_DATA_A<19>      10B6<> 11C8<>
RAM_DATA_A<20>      10B6<> 11D6<>
RAM_DATA_A<21>      10B6<> 11C6<>
RAM_DATA_A<22>      10B6<> 11C6<>
RAM_DATA_A<23>      10B6<> 11C6<>
RAM_DATA_A<24>      10B6<> 11C8<>
RAM_DATA_A<25>      10C5<> 11C8<>
RAM_DATA_A<26>      10C5<> 11C8<>
RAM_DATA_A<27>      10C5<> 11C8<>
RAM_DATA_A<28>      10C5<> 11C6<>
RAM_DATA_A<29>      10C5<> 11C6<>
RAM_DATA_A<30>      10C5<> 11C6<>
RAM_DATA_A<31>      10C5<> 11C6<>
RAM_DATA_A<32>      10C4<> 11B8<>
RAM_DATA_A<47..32>  36B5>
RAM_DATA_A<33>      10C4<> 11B8<>
RAM_DATA_A<34>      10C4<> 11B8<>
RAM_DATA_A<35>      10C4<> 11B8<>
RAM_DATA_A<36>      10B4<> 11B6<>
RAM_DATA_A<37>      10B4<> 11B6<>
RAM_DATA_A<38>      10B4<> 11B6<>
RAM_DATA_A<39>      10B4<> 11B6<>
RAM_DATA_A<40>      10B4<> 11B8<>
RAM_DATA_A<41>      10D3<> 11B8<>
RAM_DATA_A<42>      10C3<> 11A8<>
RAM_DATA_A<43>      10C3<> 11A8<>
RAM_DATA_A<44>      10C3<> 11B6<>
RAM_DATA_A<45>      10C3<> 11B6<>
RAM_DATA_A<46>      10C3<> 11A6<>
RAM_DATA_A<47>      10C3<> 11A6<>
RAM_DATA_A<48>      10C2<> 11A8<>
RAM_DATA_A<55..48>  36B5>
RAM_DATA_A<49>      10C2<> 11A8<>
RAM_DATA_A<50>      10C2<> 11A8<>
RAM_DATA_A<51>      10C2<> 11A8<>
RAM_DATA_A<52>      10B2<> 11A6<>
RAM_DATA_A<53>      10B2<> 11A6<>
RAM_DATA_A<54>      10B2<> 11A6<>
RAM_DATA_A<55>      10B2<> 11A6<>
RAM_DATA_A<56>      10B2<> 11A8<>
RAM_DATA_A<63..56>  36A5>
RAM_DATA_A<57>      10D1<> 11A8<>
RAM_DATA_A<58>      10C1<> 11A8<>
RAM_DATA_A<59>      10C1<> 11A8<>
RAM_DATA_A<60>      10C1<> 11A6<>
RAM_DATA_A<61>      10C1<> 11A6<>
RAM_DATA_A<62>      10C1<> 11A6<>
RAM_DATA_A<63>      10C1<> 11A6<>
RAM_DATA_B<0>       10C8<> 11D3<>
RAM_DATA_B<7..0>    36C5>
RAM_DATA_B<1>       10C8<> 11D3<>
RAM_DATA_B<2>       10C8<> 11D3<>
RAM_DATA_B<3>       10C8<> 11D3<>
RAM_DATA_B<4>       10C8<> 11D5<>
RAM_DATA_B<5>       10C8<> 11D5<>
RAM_DATA_B<6>       10C8<> 11D5<>
RAM_DATA_B<7>       10C8<> 11D5<>
RAM_DATA_B<8>       10C8<> 11D3<>
RAM_DATA_B<15..8>   36C5>
RAM_DATA_B<9>       10C8<> 11D3<>
RAM_DATA_B<10>      10C8<> 11D3<>
RAM_DATA_B<11>      10C8<> 11D3<>
RAM_DATA_B<12>      10C8<> 11D5<>
RAM_DATA_B<13>      10C8<> 11D5<>
RAM_DATA_B<14>      10C8<> 11D5<>
RAM_DATA_B<15>      10C8<> 11D5<>
RAM_DATA_B<16>      10C6<> 11D3<>
RAM_DATA_B<31..16>  36B5>
```

```
RAM_DATA_B<17>      10C6<> 11C3<>
RAM_DATA_B<18>      10C6<> 11C3<>
RAM_DATA_B<19>      10C6<> 11C3<>
RAM_DATA_B<20>      10C6<> 11D5<>
RAM_DATA_B<21>      10C6<> 11C5<>
RAM_DATA_B<22>      10C6<> 11C5<>
RAM_DATA_B<23>      10C6<> 11C5<>
RAM_DATA_B<24>      10C6<> 11C3<>
RAM_DATA_B<25>      10C6<> 11C3<>
RAM_DATA_B<26>      10C6<> 11C3<>
RAM_DATA_B<27>      10C6<> 11C3<>
RAM_DATA_B<28>      10C6<> 11C5<>
RAM_DATA_B<29>      10C6<> 11C5<>
RAM_DATA_B<30>      10C6<> 11C5<>
RAM_DATA_B<31>      10C6<> 11C5<>
RAM_DATA_B<32>      10D4<> 11B3<>
RAM_DATA_B<47..32>  36B5>
RAM_DATA_B<33>      10C4<> 11B3<>
RAM_DATA_B<34>      10C4<> 11B3<>
RAM_DATA_B<35>      10C4<> 11B3<>
RAM_DATA_B<36>      10C4<> 11B5<>
RAM_DATA_B<37>      10C4<> 11B5<>
RAM_DATA_B<38>      10C4<> 11B5<>
RAM_DATA_B<39>      10C4<> 11B5<>
RAM_DATA_B<40>      10C4<> 11B3<>
RAM_DATA_B<41>      10C4<> 11B3<>
RAM_DATA_B<42>      10C4<> 11A3<>
RAM_DATA_B<43>      10C4<> 11A3<>
RAM_DATA_B<44>      10C4<> 11B5<>
RAM_DATA_B<45>      10C4<> 11B5<>
RAM_DATA_B<46>      10C4<> 11A5<>
RAM_DATA_B<47>      10C4<> 11A5<>
RAM_DATA_B<48>      10D2<> 11A3<>
RAM_DATA_B<55..48>  36B5>
RAM_DATA_B<49>      10C2<> 11A3<>
RAM_DATA_B<50>      10C2<> 11A3<>
RAM_DATA_B<51>      10C2<> 11A3<>
RAM_DATA_B<52>      10C2<> 11A5<>
RAM_DATA_B<53>      10C2<> 11A5<>
RAM_DATA_B<54>      10C2<> 11A5<>
RAM_DATA_B<55>      10C2<> 11A5<>
RAM_DATA_B<56>      10C2<> 11A3<>
RAM_DATA_B<63..56>  36A5>
RAM_DATA_B<57>      10C2<> 11A3<>
RAM_DATA_B<58>      10C2<> 11A3<>
RAM_DATA_B<59>      10C2<> 11A3<>
RAM_DATA_B<60>      10C2<> 11A5<>
RAM_DATA_B<61>      10C2<> 11A5<>
RAM_DATA_B<62>      10C2<> 11A5<>
RAM_DATA_B<63>      10C2<> 11A5<>
RAM_DQM_A<0>        10B8<> 11D6<> 36C5>
RAM_DQM_A<1>        10C7<> 11D6<> 36C5>
RAM_DQM_A<2>        10B6<> 11C6<>
RAM_DQM_A<3..2>     36B5>
RAM_DQM_A<3>        10C5<> 11C6<>
RAM_DQM_A<4>        10B4<> 11B6<>
RAM_DQM_A<5..4>     36B5>
RAM_DQM_A<5>        10C3<> 11A6<>
RAM_DQM_A<6>        10B2<> 11A6<> 36B5>
RAM_DQM_A<7>        10C1<> 11A6<> 36A5>
RAM_DQM_B<0>        10C8<> 11D5<> 36C5>
RAM_DQM_B<1>        10C8<> 11D5<> 36C5>
RAM_DQM_B<2>        10C6<> 11C5<>
RAM_DQM_B<3..2>     36B5>
RAM_DQM_B<3>        10C6<> 11C5<>
RAM_DQM_B<4>        10C4<> 11B5<>
RAM_DQM_B<5..4>     36B5>
RAM_DQM_B<5>        10C4<> 11B5<>
RAM_DQM_B<6>        10C2<> 11A5<> 36B5>
RAM_DQM_B<7>        10C2<> 11A5<> 36A5>
RAM_DQS_A<0>        10B8<> 11D8<> 36C5>
RAM_DQS_A<1>        10C7<> 11D8<> 36C5>
RAM_DQS_A<2>        10B6<> 11C8<>
RAM_DQS_A<3..2>     36B5>
RAM_DQS_A<3>        10C5<> 11C8<>
RAM_DQS_A<4>        10B4<> 11B8<>
RAM_DQS_A<5..4>     36B5>
RAM_DQS_A<5>        10C3<> 11A8<>
RAM_DQS_A<6>        10B2<> 11A8<> 36B5>
RAM_DQS_A<7>        10C1<> 11A8<> 36A5>
RAM_DQS_B<0>        10C8<> 11D3<> 36C5>
RAM_DQS_B<1>        10C8<> 11D3<> 36C5>
RAM_DQS_B<2>        10C6<> 11C3<>
RAM_DQS_B<3..2>     36B5>
RAM_DQS_B<3>        10C6<> 11C3<>
RAM_DQS_B<4>        10C4<> 11B3<>
RAM_DQS_B<5..4>     36B5>
RAM_DQS_B<5>        10C4<> 11B3<>
RAM_DQS_B<6>        10C2<> 11A3<> 36B5>
RAM_DQS_B<7>        10C2<> 11A3<> 36A5>
RAM_MUXSEL_H        10A3< 10A5< 10B1<> 10B3<> 36A5>
RAM_MUXSEL_L        10A3< 10A5< 10B5<> 10B7<> 36A5>
RAM_RAS_L           9A4< 11B5<> 11B6<> 36A5>
RAM_WE_L            9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN    24D6<> 39C1>
RIGHT_USB_DM        26A3< 32A7<> 37A2> 39D1>
RIGHT_USB_DP        26A3< 32A7<> 37A2> 39D1>
RJ45_C0_PD          27B2<>
RJ45_C1_PD          27B2<>
RJ45_C2_PD          27B2<>
RJ45_C3_PD          27B2<>
RJ45_DN<0>          27B2<> 37D2> 39B3>
RJ45_DN<1>          27B2<> 37D2> 39B3>
RJ45_DN<2>          27B2<> 37D2> 39A3>
RJ45_DN<3>          27B2<> 37D2> 39A3>
RJ45_DP<0>          27B2<> 37D2> 39B3>
RJ45_DP<1>          27B2<> 37D2> 39B3>
RJ45_DP<2>          27B2<> 37D2> 39A3>
RJ45_DP<3>          27B2<> 37D2> 39A3>
ROM_CS_L            9B3< 12A5< 24B6<> 39B1>
ROM_OE_L            9B3< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L    9B3< 24C6<> 39B1>
ROM_RW_L            9B3< 12A5< 24C6<> 39B1>
ROM_WP_L            9B3<
RSDM3_TP            26C5>
RSDM4_TP            26C5>
RSDM5_TP            26C5>
RSDP3_TP            26C5>
RSDP4_TP            26C5>
RSDP5_TP            26C5>
RUN_OR_AC           29C6<>
SI_A2               20B7<
SI_DDC_CLK          19C5<> 20B7<
SI_DDC_DATA         19C5<> 20B7<
SI_EDGE             20B7<
SI_MSEN             20B5<>
SI_PD               20B7<
SI_RST              20B7<
SI_TMDS_CLKN        20B5<> 20C4<
SI_TMDS_CLKP        20B5<> 20C4<
SI_TMDS_DN<0>       20B5<> 20C4<
SI_TMDS_DN<1>       20B5<> 20C4<
SI_TMDS_DN<2>       20A5<> 20B4<
SI_TMDS_DP<0>       20B5<> 20C4<
SI_TMDS_DP<1>       20B5<> 20C4<
SI_TMDS_DP<2>       20A5<> 20B4<
SI_VREF             20A5< 20A7<
SLEEP               23C4<> 25C6<> 30B6<> 30D7< 33A4<
                 33A6< 33B3< 33B8<> 35B3< 35D2< 39A1>

SLEEP_LED           23C1< 25C7<> 39B6>
SLEEP_LED_I         23D1<
SLEEP_LED_L         23D2<
SLEEP_LED_SW_L      23C2<>
SLEEP_LED_UF        23C1<
SLEEP_LS5           33A5<> 33A8<
SLEEP_LS5_EN_L      33A5<>
SLEEP_L_LS5         19A7<> 27A8<> 33A5<> 34C8<> 35C8<
SLEEP_L_LS5_EN_L    33A6<>
SLEEP_L_LS5_INV     35A3< 35C2< 35C8<>
SLEEP_L_LS5_NET     33B3<> 35C8<>
SLEEP_NET           33A3<>
SLEEP_NET_INV       33A3<>
SMC_TP              26B5<
SND_AGND            25C7<> 38B6>
SND_AMP_MUTE        25C8< 25D6<> 39A4>
SND_AMP_MUTE_F      25C7< 25D6<>
SND_AMP_MUTE_L      14C5<> 25D5<>
SND_CLKOUT          14B1< 25D8< 36B1> 39D6>
SND_CLKOUT_F        25C7<> 25D7<
SND_HP_MUTE         25C5<>
SND_HP_MUTE_INV     25C5<> 25C6<> 39A4>
SND_HP_MUTE_L       14C5<> 25C4<>
SND_HP_SENSE_L      14B5<> 25D6<> 39C6>
SND_HW_RESET_L      14A7< 14B5<> 25C8< 39C6>
SND_HW_RESET_L_F    25C6<> 25C7<
SND_LIN_SENSE_L     14B5<> 25D6<> 39C6>
SND_SCLK            14B1< 25C8< 36B1> 39C6>
```

```
SND_SCLK_F          25C7< 25D7<>
SND_SYNC            14B1< 25D8< 39D6>
SND_SYNC_F          25C7<> 25D7<
SND_TO_AUDIO        14B1< 25D8< 39D6>
SND_TO_AUDIO_F      25D6<> 25D7<
SOFT_PWR_ON_L       22D1< 23A8< 30A8< 30C6<> 30D7<
                 34A3<>
SRCLK_TP            26A5> 39A4>
SRMOD_TP            26A5< 39A4>
ST7_ICP_SEL_PD      23A2< 23D6<
ST7_KBD_LED_OUT     23A4< 23C4<>
ST7_OSC1            23D5<
ST7_OSC2            23D5<>
ST7_PB6_PD          23B2< 23C4<>
ST7_RESET_L         23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H     23C2<> 23C4<>
ST7_XTAL_IN         23C5<
STOP_AGP_L          12D2< 12D4<>
SUPPLY_M_DM         25B6< 25B8<
SUPPLY_M_DP         25B6< 25B8<
SUTRO_ALS_GAIN_SW   23C4<> 24B2<> 39C2>
SUTRO_ALS_OUT       23C4<> 24B2<> 39C2>
SYSCLK_CPU          5C3< 8A6< 36D1>
SYSCLK_CPU_UF       8A6<> 36D1>
SYSCLK_DDRCLK_A0    9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1    9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B0    9D4< 11D3<> 36D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1    9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 36D1>
SYSCLK_LA_TP        8A6<>
SYSTEM_CLK_EN       14A5< 14B7< 30C4<>
TEB_TP              26A5< 39A4>
TEST_TP             26A5< 39A4>
THERM1_A_DM         25A6< 25A8< 37A2>
THERM1_A_DP         25A6< 25A8< 37A2>
THERM1_DM           25A5< 25B5< 25B5<> 37A2>
THERM1_DP           25A5< 25B5< 25B5<> 37A2>
THERM1_M_DM         37A2>
THERM1_M_DP         37A2>
THERM2_A_DM         25A6< 25A8< 37A2>
THERM2_A_DP         25A6< 25A8< 37A2>
THERM2_DM           25A5< 25B5< 25B5<> 37A2>
THERM2_DP           25A5< 25B5< 25B5<> 37A2>
THERM2_M_DM         37A2>
THERM2_M_DP         37A2>
THERM_INV           25A5<>
THERM_L_OC          25A4<> 30B4<>
TMDS_CLKN           20B3< 20C1< 20C3< 22B7<> 37B2>
TMDS_CLKP           20B3< 20C2< 20C3< 22C7<> 37B2>
TMDS_CLK_CMF        20C1<
TMDS_CONN_CLKN      22B6<> 22C7<> 37B2> 39A8>
TMDS_CONN_CLKP      22C6<> 22C7<> 37B2> 39D7>
TMDS_CONN_DN<0>     22C7<> 22D6<>
TMDS_CONN_DN<1>     22B7<> 22D5<>
TMDS_CONN_DN<2>     22B6<> 22D5<>
TMDS_CONN_DP<0>     22B7<> 22D6<>
TMDS_CONN_DP<1>     22B7<> 22D5<>
TMDS_CONN_DP<2>     22B6<> 22D5<>
TMDS_D0_CMF         20B1<
TMDS_D1_CMF         20B1<
TMDS_D2_CMF         20A1<
TMDS_DN<0>          20B1< 20B3< 20C3< 22C8<> 37B2>
                 39B8>
TMDS_DN<1>          20A3< 20B1< 20C3< 22B8<> 37B2>
                 39A8>
TMDS_DN<2>          20A1< 20A3< 20B3< 22B7<> 37B2>
                 39A8>
TMDS_DP<0>          20B2< 20B3< 20C3< 22B8<> 37B2>
                 39A8>
TMDS_DP<1>          20A3< 20B2< 20C3< 22B8<> 37B2>
                 39A8>
TMDS_DP<2>          20A2< 20A3< 20B3< 22B7<> 37B2>
                 39A8>
TPAD_F_RXD          23A7<> 39C4>
TPAD_F_TXD          23A7<> 39C4>
TPAD_RXD            23A8< 30C2< 30C4<>
TPAD_TXD            23A8< 30B2< 30C4<>
TPS2211_SHDN_L_PU   17C4<
TV_C                22A6<> 39D6>
TV_COMP             22A6<> 39D6>
TV_GND1             22B6<> 38B6> 39A7>
TV_GND2             22A6<> 38B6> 39A7>
TV_Y                22A6<> 39D6>
UIDE_ADDR<0>        13D7<> 24C4<
UIDE_ADDR<2..0>     37C5>
UIDE_ADDR<1>        13D7<> 24C4<
UIDE_ADDR<2>        13D7<> 24B4<
UIDE_CS0_L          13C7<> 24C4< 37C5>
UIDE_CS1_L          13C7<> 24B4< 37C5>
UIDE_DATA<0>        13D7<> 24D4<
UIDE_DATA<6..0>     37C5>
UIDE_DATA<1>        13D7<> 24D4<
UIDE_DATA<2>        13D7<> 24D4<
UIDE_DATA<3>        13D7<> 24D4<
UIDE_DATA<4>        13D7<> 24C4<
UIDE_DATA<5>        13D7<> 24C4<
UIDE_DATA<6>        13D7<> 24C4<
UIDE_DATA<7>        13D7<> 24C4< 37C5>
UIDE_DATA<8>        13D7<> 24C4<
UIDE_DATA<15..8>    37C5>
UIDE_DATA<9>        13D7<> 24C4<
UIDE_DATA<10>       13D7<> 24C4<
UIDE_DATA<11>       13D7<> 24D4<
UIDE_DATA<12>       13D7<> 24B4<
UIDE_DATA<13>       13D7<> 24B4<
UIDE_DATA<14>       13D7<> 24C4<
UIDE_DATA<15>       13D7<> 24B4<
UIDE_DIOR_L         13C7<> 24A4< 37C5>
UIDE_DIOW_L         13C7<> 24A4< 37C5>
UIDE_DMACK_L        13C7<> 24A4< 37C5>
UIDE_DMARQ          13C7<> 37C5>
UIDE_INTRQ          13C7< 37C5>
UIDE_IOCHRDY        13C7< 24A4< 37C5>
UIDE_REF            13C7<> 38D3>
UIDE_RST_L          13C7<> 24A4< 37C5>
USB2_PCI_GNT_L      12C7<> 26B7<
USB2_PCI_INT_L      14B5<> 14C7< 26A8<
USB2_PCI_REQ_L      12A7< 12D7<> 26B7>
USB_D1M             14C1< 26A5> 26B4<
USB_D1P             14C1< 26A4< 26A5>
USB_D2M             14D1< 26A4< 26A5>
USB_D2P             14D1< 26A4< 26A5>
USB_DAM             14B2<> 14D2< 26A5>
USB_DAP             14B2<> 14D2< 26A5>
USB_DBM             14B2<> 14D2<
USB_DBP             14B2<> 14D2<
USB_DCM             14B2<> 14C2< 26A5>
USB_DCP             14B2<> 14C2< 26A5>
USB_DDM             14B2<> 14C2<
USB_DDP             14B2<> 14C2<
USB_DEM             14B2< 14B2<> 37B2>
USB_DEP             14B2<> 14C2< 37B2>
USB_DFM             14B2< 14B2<> 37B2>
USB_DFP             14B2< 14B2<> 37B2>
USB_OC_AB_L         14B2< 14C7<
USB_OC_CD_L         14B2< 14C7<
USB_OC_EF_L         14B2< 14D7<
USB_PWREN_AB_L      14B2<> 14C7<
USB_PWREN_CD_L      14B2<> 14C7<
USB_PWREN_EF_L      14B2<> 14D7<
VCORE_BOOST         34C4<> 38C1>
VCORE_BST           34C5<> 38C1>
VCORE_CC            34B6<> 38B1>
VCORE_CNTL_RC       19A3<>
VCORE_DH            34B5<> 38C1>
VCORE_DL            34B5<> 38C1>
VCORE_FAST<1>       34D3< 34D5<
VCORE_FAST<2>       34D3< 34D5<
VCORE_FAST<3>       34D3< 34D5<
VCORE_FAST<4>       34D3< 34D5<
VCORE_FB            34B5< 38B1> 39A2>
VCORE_GND           34B5<> 38B1>
VCORE_GNDA          34B6<>
```

```
VCORE_GNDDIV        34A4< 34B5< 38B1>
VCORE_GNDDIV_TEST   34A3<>
VCORE_GNDSNS        34A2<> 34A4< 38B1>
VCORE_GNDSNS_TEST   34A3<>
VCORE_ILIM          34C6<> 38C1>
VCORE_LX            34B5<> 38C1>
VCORE_MUX_EN        34D5<> 39A2>
VCORE_MUX_SEL       34D5<>
VCORE_REF           34B6<> 38C1>
VCORE_SEL_OFF_PU    34B6<>
VCORE_SEL_ON        34B6<>
VCORE_SHDN_L        34C6<>
VCORE_SLOW<1>       34D6<
VCORE_SLOW<2>       34D6<
VCORE_SLOW<3>       34D6<
VCORE_SLOW<4>       34D6<
VCORE_SNS           34A1<> 38B1>
VCORE_TIME          34B4<> 38B1>
VCORE_TON           34B6< 38C1>
VCORE_VCC           34C6< 38C1>
VCORE_VGATE         14B5< 14B7< 34B4> 38B1>
VCORE_VID0          39A3>
VCORE_VID1          39A3>
VCORE_VID2          39A3>
VCORE_VID3          39A3>
VCORE_VID4          39A3>
VCORE_VID<0>        34A2<> 34B8<
VCORE_VID<1>        34A2<> 34B8< 34D4<>
VCORE_VID<2>        34A2<> 34B8< 34D4<>
VCORE_VID<3>        34A2<> 34B8< 34D4<>
VCORE_VID<4>        34A2<> 34B8< 34D4<>
VGA_B               22C6<> 22D7< 39D7>
VGA_G               22C5<> 22D7< 39D7>
VGA_HSYNC           22C6<> 22C7< 39D7>
VGA_HSYNC_BUF       22C8<>
VGA_R               22C5<> 22D7< 39D7>
VGA_VSYNC           22C5<> 22C7< 39D7>
VGA_VSYNC_BUF       22C8<>
ZV_LCDDATA20_PU     19C7<>
```

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6582	REV. C
	SCALE NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

```
BS1   PCB_STANDOFF 4
C1    CAP      22
C2    CAP      34
C3    CAP      34
C4    CAP      34
C5    CAP      34
C6    CAP      34
C7    CAP      34
C8    CAP      5
C9    CAP      16
C10   CAP      16
C11   CAP      18
C12   CAP      5
C13   CAP      34
C14   CAP      20
C15   CAP      14
C16   CAP      16
C17   CAP      16
C18   CAP      16
C19   CAP      16
C20   CAP      16
C21   CAP      16
C22   CAP      16
C23   CAP      16
C24   CAP      16
C25   CAP      5
C26   CAP      16
C27   CAP      16
C28   CAP      16
C29   CAP      16
C30   CAP      16
C31   CAP      16
C32   CAP      16
C33   CAP      16
C34   CAP      16
C35   CAP      16
C36   CAP      16
C37   CAP      18
C38   CAP      5
C39   CAP      5
C40   CAP      5
C41   CAP      5
C42   CAP      16
C43   CAP      16
C44   CAP      16
C45   CAP      16
C46   CAP      5
C47   CAP      5
C48   CAP      5
C49   CAP      16
C50   CAP      16
C51   CAP      16
C52   CAP      16
C53   CAP      16
C54   CAP      16
C55   CAP      16
C56   CAP      16
C57   CAP      16
C58   CAP      16
C59   CAP      16
C60   CAP      16
C61   CAP      16
C62   CAP      18
C63   CAP      18
C64   CAP      18
C65   CAP      18
C66   CAP      18
C67   CAP      18
C68   CAP      18
C69   CAP      18
C70   CAP      18
C71   CAP      18
C72   CAP      5
C73   CAP      5
C74   CAP      5
C75   CAP      16
C76   CAP      16
C77   CAP      18
C78   CAP      18
C79   CAP      20
C80   CAP      20
C81   CAP      20
C82   CAP      20
C83   CAP      12
C84   CAP      14
C85   CAP      14
C86   CAP      24
C87   CAP      20
C88   CAP      20
C89   CAP      20
C90   CAP      5
C91   CAP      5
C92   CAP      5
C93   CAP      35
C94   CAP      16
C95   CAP      16
C96   CAP      16
C97   CAP      14
C98   CAP      16
C99   CAP      16
C100  CAP      16
C101  CAP      16
C102  CAP      20
C103  CAP      5
C104  CAP      5
C105  CAP      5
C106  CAP      5
C107  CAP      5
C108  CAP      16
C109  CAP      16
C110  CAP      5
C111  CAP      5
C112  CAP      5
C113  CAP      5
C114  CAP      5
C115  CAP      5
C116  CAP      34
C117  CAP      16
C118  CAP      16
C119  CAP      16
C120  CAP      16
C121  CAP      16
C122  CAP      16
C123  CAP      16
C124  CAP      16
C125  CAP      16
C126  CAP      16
C127  CAP      16
C128  CAP      16
C129  CAP      20
C130  CAP      20
C131  CAP      20
C132  CAP      20
C133  CAP      20
C134  CAP      25
C135  CAP      25
C136  CAP      5
C137  CAP      5
C138  CAP      5
C139  CAP      5
C140  CAP      14
C141  CAP      16
C142  CAP      16
C143  CAP      16
C144  CAP      16
C145  CAP      16
C146  CAP      16
C147  CAP      16
C148  CAP      14
C149  CAP      5
C150  CAP      5
C151  CAP      5
C152  CAP      5
C153  CAP      5
C154  CAP      5
C155  CAP      5
C156  CAP      5
C157  CAP      16
C158  CAP      16
C159  CAP      16
C160  CAP      12
C161  CAP      16
C162  CAP      16
C163  CAP      16
C164  CAP      16
C165  CAP      20
C166  CAP      19
C167  CAP      19
C168  CAP      5
C169  CAP      5
C170  CAP      5
C171  CAP      16
C172  CAP      16
C173  CAP      16
C174  CAP      16
C175  CAP      16
C176  CAP      16
C177  CAP      16
C178  CAP      16
C179  CAP      16
C180  CAP      16
C181  CAP      16
C182  CAP      14
C183  CAP      16
C184  CAP      16
C185  CAP      16
C186  CAP      19
C187  CAP      19
C188  CAP      5
C189  CAP      5
C190  CAP      5
C191  CAP      5
C192  CAP      5
C193  CAP      5
C194  CAP      5
C195  CAP      5
C196  CAP      16
C197  CAP      16
C198  CAP      14
C199  CAP      16
C200  CAP      14
C201  CAP      5
C202  CAP      5
C203  CAP      5
C204  CAP      16
C205  CAP      16
C206  CAP      16
C207  CAP      16
C208  CAP      16
C209  CAP      16
C210  CAP      16
C211  CAP      16
C212  CAP      16
C213  CAP      16
C214  CAP      16
C215  CAP      16
C216  CAP      16
C217  CAP      16
C218  CAP      20
C219  CAP      19
C220  CAP      19
C221  CAP      19
C222  CAP      19
C223  CAP      5
C224  CAP      5
C225  CAP      5
C226  CAP      16
C227  CAP      16
C228  CAP      16
C229  CAP      16
C230  CAP      16
C231  CAP      16
C232  CAP      19
C233  CAP      20
C234  CAP      34
C235  CAP      35
C236  CAP      16
C237  CAP      16
C238  CAP      16
C239  CAP      16
C240  CAP      16
C241  CAP      16
C242  CAP      16
C243  CAP      16
C244  CAP      16
C245  CAP      9
C246  CAP      16
C247  CAP      12
C248  CAP      16
C249  CAP      16
C250  CAP      16
C251  CAP      16
C252  CAP      19
C253  CAP      19
C254  CAP      19
C255  CAP      20
C256  CAP      19
C257  CAP      5
C258  CAP      5
C259  CAP      16
C260  CAP      16
C261  CAP      16
C262  CAP      16
C263  CAP      16
C264  CAP      16
C265  CAP      16
C266  CAP      16
C267  CAP      16
C268  CAP      16
C269  CAP      19
C270  CAP      19
C271  CAP      19
C272  CAP      5
C273  CAP      5
C274  CAP      34
C275  CAP      5
C276  CAP      35
C277  CAP      16
C278  CAP      16
C279  CAP      16
C280  CAP      16
C281  CAP      16
C282  CAP      19
C284  CAP      20
C285  CAP      34
C286  CAP      16
C287  CAP      16
C288  CAP      16
C289  CAP      16
C290  CAP      16
C291  CAP      16
C292  CAP      16
C293  CAP      16
C294  CAP      16
C295  CAP      16
C296  CAP      16
C297  CAP      16
C298  CAP      16
C299  CAP      19
C300  CAP      19
C301  CAP      19
C302  CAP      19
C303  CAP      19
C304  CAP      21
C305  CAP      19
C306  CAP      19
C307  CAP      19
C308  CAP      8
C309  CAP      16
C310  CAP      16
C311  CAP      19
C312  CAP      16
C313  CAP      16
C314  CAP      16
C315  CAP      16
C316  CAP      16
C317  CAP      16
C318  CAP      16
C319  CAP      16
C320  CAP      16
C321  CAP      16
C322  CAP      16
C323  CAP      16
C324  CAP      16
C325  CAP      16
C326  CAP      19
C327  CAP      21
C328  CAP      19
C329  CAP      19
C330  CAP      19
C331  CAP      19
C332  CAP      19
C333  CAP      19
C334  CAP      16
C335  CAP      16
C336  CAP      16
C337  CAP      16
C338  CAP      19
C339  CAP      21
C340  CAP      5
C341  CAP      5
C342  CAP      5
C343  CAP      5
C344  CAP      5
C345  CAP      5
C346  CAP      5
C347  CAP      5
C348  CAP      16
C349  CAP      16
C350  CAP      16
C351  CAP      16
C352  CAP      16
C353  CAP      14
C354  CAP      16
C355  CAP      16
C356  CAP      16
C357  CAP      16
C358  CAP      21
C359  CAP      21
C360  CAP      21
C361  CAP      21
C362  CAP      21
C363  CAP      21
C364  CAP      21
C365  CAP      16
C366  CAP      16
C367  CAP      16
C368  CAP      16
C369  CAP      16
C370  CAP      16
C371  CAP      16
C372  CAP      21
C373  CAP      21
C374  CAP      21
C375  CAP      16
C376  CAP      16
C377  CAP      16
C378  CAP      16
C379  CAP      21
C380  CAP      21
C381  CAP      21
C382  CAP      21
C383  CAP      21
C384  CAP      16
C385  CAP      16
C386  CAP      16
C387  CAP      16
C388  CAP      16
C389  CAP      16
C390  CAP      16
C391  CAP      16
C392  CAP      16
C393  CAP      16
C394  CAP      16
C395  CAP      16
C396  CAP      16
C397  CAP      16
C398  CAP      16
C399  CAP      16
C400  CAP      16
C401  CAP      16
C402  CAP      16
C403  CAP      16
C404  CAP      16
C405  CAP      16
C406  CAP      16
C407  CAP      16
C408  CAP      21
C409  CAP      21
C410  CAP      16
C411  CAP      21
C412  CAP      21
C413  CAP      21
C414  CAP      21
C415  CAP      21
C416  CAP      22
C417  CAP      16
C418  CAP      16
C419  CAP      14
C420  CAP      21
C421  CAP      21
C422  CAP      16
C423  CAP      16
C424  CAP      14
C425  CAP      21
C426  CAP      21
C427  CAP_P    34
C428  CAP      21
C429  CAP      21
C430  CAP_P    34
C431  CAP_P    34
C432  CAP_P    34
C433  CAP      14
C434  CAP      21
C435  CAP      21
C436  CAP      21
C437  CAP      21
C438  CAP      21
C439  CAP      34
C440  CAP      22
C441  CAP_P    34
C442  CAP      27
C443  CAP_P    34
C444  CAP_P    34
C445  CAP_P    34
C446  CAP      21
C447  CAP      21
C448  CAP      19
C449  CAP      22
C450  CAP      21
C451  CAP      19
C452  CAP      22
C453  CAP      27
C454  CAP      27
C455  CAP      34
C456  CAP      33
C457  CAP      27
C458  CAP      31
C459  CAP      34
C460  CAP      9
C461  CAP      32
C462  CAP      32
C463  CAP      32
C464  CAP      27
C465  CAP      27
C466  CAP      27
C467  CAP      17
C468  CAP      31
C469  CAP      25
C470  CAP      9
C471  CAP      27
C472  CAP      27
C473  CAP      19
C474  CAP      22
C475  CAP      27
C476  CAP      27
C477  CAP      27
C478  CAP      25
C479  CAP      9
C480  CAP      16
C481  CAP      11
C482  CAP      11
C483  CAP      19
C484  CAP      22
C485  CAP      32
C486  CAP      27
C487  CAP      27
C488  CAP      27
C489  CAP      11
C490  CAP      11
C491  CAP      27
C492  CAP      27
C493  CAP      27
C494  CAP      19
C495  CAP      32
C496  CAP      27
C497  CAP      27
C498  CAP      34
C499  CAP      35
C500  CAP      22
C501  CAP      27
C502  CAP      27
C503  CAP      27
C504  CAP      27
C505  CAP      27
C506  CAP      27
C507  CAP      34
C508  CAP      33
C509  CAP      32
C510  CAP      32
C511  CAP      27
C512  CAP      34
C513  CAP      25
C514  CAP      19
C515  CAP      19
C516  CAP      33
C517  CAP      27
C518  CAP      34
C519  CAP      35
C520  CAP      27
C521  CAP      34
C522  CAP      11
C523  CAP      11
C524  CAP      11
C525  CAP      11
C526  CAP      11
C527  CAP      11
C528  CAP      29
C529  CAP      34
C530  CAP      11
C531  CAP      35
C532  CAP      33
C533  CAP      33
C534  CAP      33
C535  CAP      32
C536  CAP      32
C537  CAP      32
C538  CAP      28
C539  CAP      28
C540  CAP      28
C541  CAP      28
C542  CAP      11
C543  CAP      21
C544  CAP      35
C545  CAP      33
C546  CAP      28
C547  CAP      31
C548  CAP      11
C549  CAP      11
C550  CAP      11
C551  CAP      11
C552  CAP      22
C553  CAP      32
C554  CAP      32
C555  CAP      27
C556  CAP      29
C557  CAP      31
C558  CAP      30
C559  CAP      35
C560  CAP      33
C561  CAP      28
C562  CAP      31
C563  CAP      31
C564  CAP      31
C565  CAP      11
C566  CAP      33
C567  CAP      33
C568  CAP      32
C569  CAP      32
C570  CAP      28
C571  CAP      28
C572  CAP      31
C573  CAP      11
C574  CAP      30
C575  CAP      35
C576  CAP      33
C577  CAP      28
C578  CAP      31
C579  CAP      31
C580  CAP      35
C581  CAP      35
C582  CAP      35
C583  CAP      33
C584  CAP      32
C585  CAP      32
C586  CAP      28
C587  CAP      28
C588  CAP      29
C589  CAP      11
C590  CAP      33
C591  CAP      28
C592  CAP      31
C593  CAP      31
C594  CAP      11
C595  CAP      11
C596  CAP      11
C597  CAP      11
C598  CAP      33
C599  CAP      32
C600  CAP      31
C601  CAP      11
C602  CAP      11
C603  CAP      35
C604  CAP      32
C605  CAP      28
C606  CAP      29
C607  CAP      29
C608  CAP      31
C609  CAP      33
C610  CAP      33
C611  CAP      33
C612  CAP      33
C613  CAP      32
C614  CAP      28
C615  CAP      31
C616  CAP      31
C617  CAP      31
C618  CAP      31
C619  CAP      31
C620  CAP      33
C621  CAP      31
C622  CAP      31
C623  CAP      33
C624  CAP      31
C625  CAP      32
C626  CAP      32
C627  CAP      28
C628  CAP      28
C629  CAP      28
C630  CAP      31
C631  CAP      31
C632  CAP      31
C633  CAP      31
C634  CAP      28
C635  CAP      28
C636  CAP      23
C637  CAP      23
C638  CAP      23
C639  CAP      33
C640  CAP      28
C641  CAP      28
C642  CAP      28
C643  CAP      30
C644  CAP      32
C645  CAP      28
C646  CAP      28
C647  CAP      21
C648  CAP      23
C649  CAP      26
C650  CAP      28
C651  CAP      25
C652  CAP      31
C653  CAP      28
C654  CAP      23
C655  CAP      23
C656  CAP      23
C657  CAP      26
C658  CAP      31
C659  CAP      33
C660  CAP      23
C661  CAP      26
C662  CAP      33
C663  CAP      23
C664  CAP      30
C665  CAP      26
C666  CAP      30
C667  CAP      26
C668  CAP      25
C669  CAP      22
C670  CAP      23
C671  CAP      21
C672  CAP      21
C673  CAP      23
C674  CAP      34
C675  CAP      23
C676  CAP      22
C677  CAP      35
C678  CAP      25
C679  CAP      34
C680  CAP      34
C681  CAP      25
C682  CAP      34
C683  CAP      35
C684  CAP      22
C685  CAP      22
C686  CAP      14
C687  CAP      34
C688  CAP      25
C689  CAP      34
C690  CAP      25
C691  CAP      14
C692  CAP      14
C693  CAP      34
C694  CAP_P    33
C695  CAP      34
C696  CAP      22
C697  CAP      33
C698  CAP      14
C699  CAP      34
C700  CAP      33
C701  CAP      21
C702  CAP      22
C703  CAP      22
C704  CAP      21
C705  CAP      35
C706  CAP      22
C707  CAP      22
C708  CAP      19
C709  CAP      35
C710  CAP      22
C711  CAP      25
C712  CAP      22
C713  CAP      22
C714  CAP      22
C715  CAP      21
C716  CAP      21
C717  CAP      22
C718  CAP      22
C719  CAP_P    19
C720  CAP_P    19
C721  CAP_P    19
C722  CAP      21
C723  CAP      35
C724  CAP      22
C725  CAP      21
C726  CAP      35
C727  CAP      10
C728  CAP_P    34
C729  CAP_P    34
C730  CAP_P    34
C731  CAP_P    34
C732  CAP_P    34
C733  CAP_P    34
C734  CAP_P    34
C735  CAP      10
C736  CAP      10
C737  CAP      10
C738  CAP      10
C739  CAP      22
C740  CAP      35
C741  CAP      10
C742  CAP      10
C743  CAP      10
C744  CAP      22
C745  CAP_P    35
C746  CAP      22
C747  CAP      10
C748  CAP      10
C749  CAP      22
C750  CAP_P    32
C751  CAP_P    35
C752  CAP      10
C753  CAP      10
C754  CAP      27
C755  CAP      27
C756  CAP_P    33
C757  CAP      31
C758  CAP_P    32
C759  CAP      33
C760  CAP      33
C761  CAP      11
C762  CAP      19
C763  CAP      33
C764  CAP      34
C765  CAP_P    32
C766  CAP      19
C767  CAP      25
C768  CAP      34
C769  CAP_P    32
C770  CAP      33
C771  CAP      31
C772  CAP      31
C773  CAP      17
C774  CAP      29
C775  CAP      31
C776  CAP      17
C777  CAP      28
C778  CAP      28
C779  CAP      33
C780  CAP_P    35
C781  CAP      29
C782  CAP_P    35
C783  CAP      17
C784  CAP      29
C785  CAP      33
C786  CAP      29
C787  CAP      32
C788  CAP_P    35
C789  CAP      17
C790  CAP      17
C791  CAP      17
C792  CAP      29
C793  CAP_P    32
C794  CAP_P    32
C795  CAP      17
C796  CAP      17
C797  CAP      17
C798  CAP      17
C799  CAP_P    32
C800  CAP      33
C801  CAP      32
C802  CAP      31
C803  CAP      29
C804  CAP      28
C805  CAP      29
C806  CAP      33
C807  CAP      29
C808  CAP      28
C809  CAP      35
C810  CAP      28
C811  CAP      33
C812  CAP      30
C813  CAP      17
C814  CAP      23
C815  CAP      23
C816  CAP      23
C817  CAP      31
C818  CAP_P    28
C819  CAP_P    32
C820  CAP_P    32
C821  CAP_P    32
C822  CAP_P    32
C823  CAP_P    33
C824  CAP_P    31
C825  CAP_P    33
C826  CAP      33
C827  CAP      30
C828  CAP      23
C829  CAP      26
C830  CAP      26
C831  CAP      30
C832  CAP      30
C833  CAP      26
C834  CAP      26
C835  CAP      30
C836  CAP      26
C837  CAP      26
C838  CAP      26
C839  CAP      26
C840  CAP      26
C841  CAP      26
C842  CAP      26
C843  CAP      26
C844  CAP      26
C845  CAP      26
C846  CAP      25
C847  CAP      21
C848  CAP      21
C849  CAP      21
C850  CAP      21
C851  CAP      21
C852  CAP      21
C853  CAP      21
C854  CAP      21
C855  CAP      21
C856  CAP      21
C857  CAP      21
C858  CAP      21
C859  CAP      21
C860  CAP      21
C861  CAP      21
C862  CAP      21
C863  CAP      21
C864  CAP      21
C865  CAP      21
C866  CAP      21
C867  CAP      21
C868  CAP      21
C869  CAP      21
C870  CAP      21
C871  CAP      21
C872  CAP      21
C873  CAP      21
C874  CAP      21
C875  CAP      21
C876  CAP      21
C877  CAP      21
C878  CAP      21
C879  CAP      21
C880  CAP      21
C881  CAP      21
C882  CAP      19
C883  CAP      31
C884  CAP_P    34
C885  CAP_P    34
C886  CAP      35
C887  CAP      35
C888  CAP      35
C889  CAP      21
C890  CAP      35
C891  CAP      35
C892  CAP      35
C893  CAP      35
C894  CAP      35
C895  CAP      25
C896  CAP      25
C897  CAP      25
C898  CAP      25
C899  CAP      25
C900  CAP      25
C901  CAP      25
C902  CAP      19
C903  CAP      25
C904  CAP      25
C905  CAP      25
C906  CAP      31
C907  CAP      35
C908  CAP      35
D1    DIODE      27
D2    DIODE_SCHOT 34
D3    DIODE_SCHOT 32
D4    DIODE      32
D5    DIODE_SCHOT 19
D6    DIODE_SCHOT 33
D7    DIODE_SCHOT 32
D8    ZENER      29
D9    DIODE      31
D10   DIODE      31
D11   DIODE_SCHOT 32
D12   DIODE_DUAL_6P 29
D13   DIODE_SCHOT 33
D14   DIODE_SCHOT_3P2 28
D15   DIODE_DUAL_6P 29
D16   DIODE      33
D17   DIODE_SCHOT 32
D18   DIODE      32
D19   DIODE_SCHOT 32
D20   DIODE_SCHOT 28
D21   DIODE_SCHOT 22
D22   DIODE_SCHOT 33
D23   DIODE_SCHOT 35
D24   DIODE_SCHOT 19
D25   DIODE      34
D26   DIODE_DUAL_6P 29
D27   DIODE_SCHOT 32
D28   DIODE_DUAL_6P 29
D29   DIODE_SCHOT 29
D30   DIODE_SCHOT 31
D33   DIODE_SCHOT 35
D34   DIODE_SCHOT 33
DP1   DPAK3P     19
DP2   DPAK3P     34
DP3   DPAK3P     35
DP4   DPAK3P     31
DP5   DPAK3P     29
DP6   DPAK3P     19
DP7   DPAK3P     21
F1    FUSE       22
F2    FUSE       29
F3    FUSE       31
F4    FUSE       31
F5    FUSE       29
FL1   FILTER_LC 22
FL2   FILTER_LC 22
FL3   FILTER_LC 22
G1    OSC        28
G2    OSC        18
J1    CON_F1ST_S2MT_SM 14
J2    CON_3RTSM_125 25
J3    CON_F14RT_S2MT_SM 24
J4    CON_3RTSM_125 25
J5    CON_12     34
J6    CON_F30RT_S2MT_SM 22
J7    CON_4RT_WRIB 22
J8    CON_F16ST_D_SMA 25
J9    CON_M80ST_D4MT_SM 17
J10   CON_M50SM_5MM 24
J11   CON_F14RT_S2MT_SM 32
J12   CON_F30ST_D_SM 25
J13   CON_M50SM_5MM 24
J14   CON_F30RT_T6MT_TH1 22
J15   CON_F5RT_MINIDIN_TH 22
J16   CON_10STSM_5087 25
J17   CON_RJ45_SHORT_4MT_TH 27
J18   CON_M8RT_S_SM 31
J19   CON_F200RT_DDRDIMM_SM1 11
J20   CON_F80ST_D4MT_SM 24
J22   CON_F200RT_DDRDIMM_SM2 11
J23   CON_F6RT_S4MT_TH1 29
J24   CON_F40RT_S2MT_SM 23
J25   CON_M8RT_S_SM 31
J26   CON_F9RT_1394B_S6MT_SMA 29
L1    IND        14
L2    IND        18
L3    IND        18
L4    IND        18
L5    IND        27
L6    IND        22
L7    IND        28
L8    IND        31
L9    IND        31
L10   IND        31
L11   IND        23
L12   IND        31
L13   IND        20
L14   IND        20
L15   IND        20
L16   IND        21
L18   IND        14
L21   FILTER_4P 22
L22   IND        14
L23   IND        22
L24   IND        19
L25   IND        22
L26   IND        22
L27   IND        22
L28   IND        22
L29   IND        22
L30   IND_3P     19
L31   IND        22
L32   IND        22
L33   IND        22
L34   IND        27
L35   IND        35
L36   IND_3P     34
L37   IND_3P     32
L38   IND        33
L39   IND        29
L40   IND        29
L41   IND        33
L42   IND        31
L43   FILTER_4P 29
L44   FILTER_4P 29
L45   IND        35
L46   IND        23
L47   IND        23
L48   IND        23
L49   IND        23
L50   IND        29
L51   IND        28
L52   IND        23
L53   IND        31
L54   IND        26
L55   IND        21
L56   IND        21
L57   IND        21
L58   IND        21
L59   IND        21
L60   IND        21
L61   IND        21
L62   IND        21
L63   IND        21
L64   IND        21
L65   IND        21
L66   IND        21
L67   IND        21
L68   IND        21
L69   IND        21
L70   FILTER_4P 29
L71   FILTER_4P 29
L72   FILTER_4P 22
L73   FILTER_4P 22
L74   FILTER_4P 22
L75   IND        35
L76   IND        25
L77   IND        25
L78   IND        25
L79   IND        25
L80   IND        25
L81   IND        25
L82   IND        25
PD1   PHOTODIODE_2P 23
Q1    TRA_2N7002DW 7
Q2    TRA_2N7002DW 7
Q3    TRA_2N7002 7
Q4    TRA_2N3904 7
Q5    TRA_2N3904 19
Q6    TRA_2N3904 19
Q7    TRA_FDG6324L 22
Q8    TRA_2N7002 22
Q9    TRA_2N7002DW 33
Q10   TRA_2N7002DW 31
Q11   TRA_SI3443DV 22
Q12   TRA_2N3904 34
Q13   TRA_SI4435DY 31
Q14   TRA_FDG6324L 32
Q15   TRA_2N7002DW 27
Q16   TRA_SI4435DY 31
Q17   TRA_2N3904 34
Q19   TRA_2N7002 35
Q20   TRA_2N7002DW 31
Q21   TRA_2N7002DW 31
Q22   TRA_2N7002 30
Q23   TRA_2N7002DW 33
Q24   TRA_SI4435DY 31
Q25   TRA_2N7002DW 29 33
Q26   TRA_2N7002DW 25
Q27   TRA_2N7002DW 31
Q28   TRA_SI3443DV 33
Q29   TRA_2N7002DW 31
Q30   TRA_2N7002DW 31
Q31   TRA_2N7002DW 25
Q32   TRA_SI3443DV 33
Q33   TRA_2N3906 23
Q35   TRA_2N7002DW 22 23
Q36   TRA_SI3446DV 25
Q37   TRA_SI3446DV 25
Q38   TRA_2N7002DW 22
Q39   TRA_2N3904 25
Q40   TRA_TP0610 22
Q41   TRA_2N7002DW 22
Q42   TRA_2N3904 22
Q43   TRA_SI3443DV 33
Q44   TRA_2N3904 22
Q45   TRA_TP0610 22
Q46   TRA_SI3446DV 35
Q47   TRA_2N3904 25
Q48   TRA_SI7892DP 19
Q49   TRA_SI7860DP 34
Q50   TRA_SI7860DP 34
Q51   TRA_SI7860DP 19
Q52   TRA_SI4888DY 33
Q53   TRA_IRF7832 34
Q54   TRA_IRF7832 34
Q55   TRA_IRF7832 34
Q56   TRA_IRF7811W 35
Q57   TRA_IRF7805 35
Q58   TRA_2N7002DW 29
Q59   TRA_IRF7805 32
Q60   TRA_IRF7811W 32
Q61   TRA_SI4888DY 33
Q62   TRA_2N3904 25
Q63   TRA_IRF7805 31
Q64   TRA_IRF7811W 31
Q65   TRA_2N7002DW 31
Q66   TRA_2N3904 25
Q67   TRA_NDS9407 29
Q68   TRA_IRF7811W 35
Q69   TRA_IRF7805 35
Q71   TRA_SI4888DY 33
Q72   TRA_SI4888DY 33
Q73   TRA_2N3906 23
Q74   TRA_2N3906 23
Q75   TRA_2N7002DW 23
Q76   TRA_SUD45P03 31
Q77   TRA_SI3446DV 19
Q78   TRA_2N7002DW 25
Q79   TRA_2N7002DW 33
Q80   TRA_2N7002DW 19
Q81   TRA_2N7002DW 33
Q82   TRA_2N7002DW 35
Q83   TRA_2N7002DW 35
Q84   TRA_SI6467BDQ 35
Q85   TRA_SI6467BDQ 35
Q86   TRA_2N7002DW 34
Q87   TRA_2N7002DW 25
R1    RES        22
R2    RES        7
R3    RES        7
R4    RES        7
R5    RES        7
R6    RES        23
R7    RES        14
R8    RES        24
R9    RES        7
R10   RES        7
R11   RES        7
R12   RES        7
R13   RES        7
R14   RES        7
R15   RES        7
R16   RES        7
R17   RES        7
R18   RES        7
R19   RES        7
R20   RES        7
R21   RES        7
R22   RES        7
R23   RES        7
R24   RES        7
R25   RES        7
R26   RES        7
R27   RES        7
R28   RES        14
R29   RES        14
R30   RES        24
R31   RES        24
R32   RES        24
R33   RES        7
R34   RES        13
R35   RES        24
R36   RES        24
R37   RES        18
R38   RES        18
R39   RES        23
R40   RES        23
R41   RES        20
R42   RES        25
R43   RES        18
R44   RES        18
R45   RES        18
R46   RES        18
R47   RES        7
R48   RES        7
R49   RES        14
R50   RES        14
R51   RES        13
R52   RES        13
R53   RES        18
R54   RES        18
R55   RES        18
R56   RES        26
R57   RES        5
R58   RES        5
R59   RES        5
R60   RES        5
R61   RES        5
R62   RES        23
R63   RES        24
R64   RES        24
R65   RES        5
R66   RES        20
R67   RES        14
R68   RES        24
R69   RES        24
R70   RES        18
R71   RES        24
R72   RES        5
R73   RES        5
R74   RES        24
R75   RES        24
R76   RES        24
R77   RES        12
R78   RES        26
R79   RES        5
R80   RES        14
R81   RES        24
R82   RES        12
R83   RES        26
R84   RES        26
R85   RES        5
R86   RES        5
R87   RES        5
R88   RES        20
R89   RES        14
R90   RES        14
R91   RES        14
R92   RES        13
R93   RES        24
R94   RES        24
R95   RES        24
R96   RES        26
R97   RES        5
R98   RES        5
R99   RES        20
R100  RES        14
R101  RES        24
R102  RES        14
R103  RES        12
R104  RES        18
R105  RES        18
R106  RES        5
R107  RES        5
R108  RES        5
R109  RES        5
R110  RES        20
R111  RES        14
R112  RES        12
R113  RES        14
R114  RES        14
R115  RES        14
R116  RES        24
R117  RES        13
R118  RES        18
R119  RES        18
R120  RES        5
R121  RES        8
R122  RES        8
R123  RES        8
R124  RES        13
R125  RES        14
R126  RES        18
R127  RES        18
R128  RES        5
R129  RES        5
R130  RES        5
R131  RES        8
R132  RES        8
R133  RES        8
R134  RES        8
R135  RES        8
R136  RES        8
R137  RES        8
R138  RES        18
R139  RES        5
R140  RES        8
R141  RES        8
R142  RES        8
R143  RES        8
R144  RES        8
R145  RES        13
R146  RES        12
R147  RES        12
R148  RES        5
R149  RES        7
R150  RES        8
R151  RES        8
R152  RES        8
R153  RES        8
R154  RES        13
R155  RES        14
R156  RES        14
R157  RES        12
R158  RES        18
R159  RES        18
R160  RES        5
R161  RES        8
R162  RES        8
R163  RES        8
R164  RES        8
R165  RES        8
R166  RES        8
R167  RES        8
R168  RES        14
R169  RES        12
R170  RES        12
R171  RES        12
R172  RES        18
R173  RES        18
R174  RES        8
R175  RES        8
R176  RES        8
R177  RES        8
R178  RES        8
R179  RES        8
R180  RES        12
R181  RES        18
R182  RES        8
R183  RES        8
R184  RES        8
R185  RES        12
R186  RES        12
R187  RES        12
R188  RES        18
R189  RES        18
R190  RES        35
R191  RES        9
R192  RES        12
R193  RES        12
R194  RES        12
R195  RES        18
R196  RES        8
R197  RES        8
R198  RES        9
R199  RES        9
R200  RES        18
R201  RES        18
R202  RES        20
R203  RES        19
R204  RES        20
R205  RES        20
R206  RES        5
R207  RES        8
R208  RES        8
R209  RES        12
R210  RES        20
R211  RES        20
R212  RES        20
R213  RES        22
R214  RES        20
R215  RES        8
R216  RES        12
R217  RES        12
R218  RES        20
R219  RES        20
R220  RES        20
R221  RES        19
R222  RES        20
R223  RES        19
R224  RES        20
R225  RES        8
R226  RES        8
R227  RES        8
R228  RES        19
R229  RES        19
R230  RES        12
R231  RES        20
R232  RES        20
R233  RES        20
R234  RES        19
R235  RES        20
R236  RES        19
R237  RES        20
R238  RES        9
R239  RES        10
R240  RES        19
R241  RES        5
R242  RES        10
R243  RES        10
R244  RES        14
R245  RES        19
R246  RES        19
R247  RES        19
R248  RES        19
R249  RES        19
R250  RES        9
R251  RES        21
R252  RES        10
R253  RES        19
R254  RES        19
R255  RES        21
R256  RES        19
R257  RES        19
R258  RES        19
R259  RES        19
R260  RES        19
R261  RES        19
R262  RES        19
R263  RES        19
R264  RES        14
R265  RES        19
R266  RES        19
R267  RES        34
R268  RES        21
R269  RES        19
R270  RES        19
R271  RES        19
R272  RES        19
R273  RES        19
R274  RES        19
R277  RES        14
R278  RES        14
R279  RES        21
R281  RES        14
R284  RES        21
R286  RES        26
R287  RES        15
R288  RES        34
R289  RES        34
R290  RES        34
R291  RES        14
R292  RES        34
R293  RES        25
R294  RES        19
R295  RES        25
R296  RES        33
R297  RES        34
R298  RES        33
R299  RES        21
R300  RES        33
R301  RES        34
R302  RES        34
R303  RES        34
R304  RES        34
R305  RES        34
R306  RES        19
R307  RES        19
R308  RES        33
R309  RES        33
R310  RES        33
R311  RES        19
R312  RES        34
R313  RES        34
R314  RES        34
R315  RES        34
R316  RES        19
R317  RES        22
R318  RES        34
R319  RES        27
R320  RES        22
R321  RES        34
R322  RES        34
R323  RES        34
R324  RES        34
R325  RES        34
R326  RES        34
R327  RES        34
R328  RES        34
R329  RES        34
R330  RES        34
R331  RES        34
R332  RES        19
R333  RES        27
R334  RES        27
R335  RES        27
R336  RES        34
R337  RES        34
R338  RES        9
R339  RES        19
R340  RES        19
R341  RES        19
R342  RES        22
R343  RES        27
R344  RES        27
R345  RES        27
R346  RES        27
R347  RES        27
R348  RES        17
R349  RES        34
R350  RES        33
R351  RES        19
R352  RES        19
R353  RES        27
R354  RES        27
R355  RES        27
R356  RES        34
R357  RES        9
R358  RES        31
R359  RES        32
R360  RES        32
R361  RES        27
R362  RES        27
R363  RES        31
R364  RES        31
R365  RES        31
R366  RES        34
R367  RES        33
R368  RES        33
R369  RES        33
R370  RES        27
```

R371	RES	27
R372	RES	27
R373	RES	17
R374	RES	31
R375	RES	31
R376	RES	34
R377	RES	33
R378	RES	33
R379	RES	32
R380	RES	27
R381	RES	27
R382	RES	27
R383	RES	31
R384	RES	34
R385	RES	34
R386	RES	9
R387	RES	9
R388	RES	19
R389	RES	19
R390	RES	19
R391	RES	22
R392	RES	32
R393	RES	27
R394	RES	31
R395	RES	31
R396	RES	31
R397	RES	34
R398	RES	34
R399	RES	15
R400	RES	22
R401	RES	32
R402	RES	32
R403	RES	27
R404	RES	27
R405	RES	25
R406	RES	27
R407	RES	34
R408	RES	34
R409	RES	9
R410	RES	19
R411	RES	24
R412	RES	32
R413	RES	27
R414	RES	31
R415	RES	34
R416	RES	19
R417	RES	35
R418	RES	35
R419	RES	35
R420	RES	35
R421	RES	35
R422	RES	35
R423	RES	35
R424	RES	35
R425	RES	35
R426	RES	32
R427	RES	27
R428	RES	27
R429	RES	34
R430	RES	19
R431	RES	33
R432	RES	32
R433	RES	32
R434	RES	34
R435	RES	27
R436	RES	28
R437	RES	28
R438	RES	27
R439	RES	9
R440	RES	11
R441	RES	24
R442	RES	24
R443	RES	32
R444	RES	28
R445	RES	28
R446	RES	28
R447	RES	28
R448	RES	34
R449	RES	11
R450	RES	35
R451	RES	19
R452	RES	24
R453	RES	29
R454	RES	31
R455	RES	35
R456	RES	33
R457	RES	33
R458	RES	24
R459	RES	28
R460	RES	31
R461	RES	35
R462	RES	33
R463	RES	33
R464	RES	28
R465	RES	27
R466	RES	31
R467	RES	33
R468	RES	32
R469	RES	28
R470	RES	28
R471	RES	28
R472	RES	29
R473	RES	31
R474	RES	31
R475	RES	30
R476	RES	30
R477	RES	33
R478	RES	28
R479	RES	35
R480	RES	35
R481	RES	33
R482	RES	33
R483	RES	32
R484	RES	28
R485	RES	28
R486	RES	28
R487	RES	31
R488	RES	31
R489	RES	31
R490	RES	31
R491	RES	30
R492	RES	30
R493	RES	35
R494	RES	28
R495	RES	28
R496	RES	28
R497	RES	31
R498	RES	31
R499	RES	31
R500	RES	9
R501	RES	30
R502	RES	30
R503	RES	30
R504	RES	30
R505	RES	30
R506	RES	33
R507	RES	33
R508	RES	32
R509	RES	28
R510	RES	28
R511	RES	31
R512	RES	31
R513	RES	30
R514	RES	33
R515	RES	33
R516	RES	28
R517	RES	30
R518	RES	30
R519	RES	33
R520	RES	33
R521	RES	32
R522	RES	28
R523	RES	33
R524	RES	28
R525	RES	28
R526	RES	31
R527	RES	25
R528	RES	33
R529	RES	33
R530	RES	26
R531	RES	26
R532	RES	23
R533	RES	23
R534	RES	23
R535	RES	30
R536	RES	30
R537	RES	25
R538	RES	33

R539	RES	33
R540	RES	26
R541	RES	32
R542	RES	31
R543	RES	31
R544	RES	30
R545	RES	26
R546	RES	28
R547	RES	28
R548	RES	31
R549	RES	31
R550	RES	23
R551	RES	26
R552	RES	23
R553	RES	25
R554	RES	26
R555	RES	28
R556	RES	28
R557	RES	28
R558	RES	31
R559	RES	31
R560	RES	31
R561	RES	31
R562	RES	30
R563	RES	28
R564	RES	28
R565	RES	31
R566	RES	31
R567	RES	31
R568	RES	23
R569	RES	30
R570	RES	31
R571	RES	31
R572	RES	30
R573	RES	30
R574	RES	28
R575	RES	28
R576	RES	28
R577	RES	28
R578	RES	31
R579	RES	31
R580	RES	31
R581	RES	23
R582	RES	23
R583	RES	30
R584	RES	30
R585	RES	30
R586	RES	26
R587	RES	23
R588	RES	31
R589	RES	33
R590	RES	26
R591	RES	26
R592	RES	30
R593	RES	30
R594	RES	30
R595	RES	30
R596	RES	30
R597	RES	30
R598	RES	23
R599	RES	31
R600	RES	26
R601	RES	24
R602	RES	24
R603	RES	24
R605	RES	23
R606	RES	23
R607	RES	35
R609	RES	14
R610	RES	35
R611	RES	35
R612	RES	24
R613	RES	24
R614	RES	14
R615	RES	23
R616	RES	35
R617	RES	23
R618	RES	23
R619	RES	23
R621	RES	13
R622	RES	14
R623	RES	25
R624	RES	13
R625	RES	14
R626	RES	13
R627	RES	13
R629	RES	13
R630	RES	13
R631	RES	14
R632	RES	14
R634	RES	14
R636	RES	14
R638	RES	14
R639	RES	8
R640	RES	8
R641	RES	8
R642	RES	8
R643	RES	8
R644	RES	8
R645	RES	8
R646	RES	8
R647	RES	8
R649	RES	22
R650	RES	22
R651	RES	8
R652	RES	8
R653	RES	8
R654	RES	8
R655	RES	22
R656	RES	14
R657	RES	8
R658	RES	8
R659	RES	8
R660	RES	8
R661	RES	22
R662	RES	22
R663	RES	22
R664	RES	8
R665	RES	8
R666	RES	8
R667	RES	8
R668	RES	8
R669	RES	8
R670	RES	22
R671	RES	22
R672	RES	35
R673	RES	8
R674	RES	8
R675	RES	8
R676	RES	8
R677	RES	8
R678	RES	8
R679	RES	25
R680	RES	22
R681	RES	22
R682	RES	14
R683	RES	8
R684	RES	8
R685	RES	8
R686	RES	22
R688	RES	22
R689	RES	25
R690	RES	22
R691	RES	22
R692	RES	25
R693	RES	5
R694	RES	22
R695	RES	25
R696	RES	22
R697	RES	33
R698	RES	14
R699	RES	14
R700	RES	22
R701	RES	14
R702	RES	5
R703	RES	22
R704	RES	22
R705	RES	22
R706	RES	22
R707	RES	14
R708	RES	14
R709	RES	35
R710	RES	25
R711	RES	19
R712	RES	35
R713	RES	25
R714	RES	22
R715	RES	35

R716	RES	25
R717	RES	25
R718	RES	22
R719	RES	25
R720	RES	14
R721	RES	21
R722	RES	21
R723	RES	25
R724	RES	22
R725	RES	25
R726	RES	25
R727	RES	35
R728	RES	21
R729	RES	21
R730	RES	24
R731	RES	33
R732	RES	34
R733	RES	27
R734	RES	31
R735	RES	27
R736	RES	29
R737	RES	29
R738	RES	31
R739	RES	31
R740	RES	28
R741	RES	29
R742	RES	31
R743	RES	29
R744	RES	31
R745	RES	24
R746	RES	31
R747	RES	31
R748	RES	31
R749	RES	31
R750	RES	17
R751	RES	29
R752	RES	29
R753	RES	17
R754	RES	31
R755	RES	31
R756	RES	17
R757	RES	17
R758	RES	28
R759	RES	28
R760	RES	28
R761	RES	28
R762	RES	17
R763	RES	31
R764	RES	17
R765	RES	30
R766	RES	17
R767	RES	17
R768	RES	30
R769	RES	30
R770	RES	23
R771	RES	23
R772	RES	23
R773	RES	23
R774	RES	31
R775	RES	28
R776	RES	23
R777	RES	23
R778	RES	30
R779	RES	29
R781	RES	28
R782	RES	30
R783	RES	26
R784	RES	26
R785	RES	30
R786	RES	30
R787	RES	30
R788	RES	30
R789	RES	26
R790	RES	26
R791	RES	26
R792	RES	26
R793	RES	26
R794	RES	26
R795	RES	26
R796	RES	26
R797	RES	35
R798	RES	35
R799	RES	35
R800	RES	35
R801	RES	35
R802	RES	35
R803	RES	35
R804	RES	19
R805	RES	34
R806	RES	34
R807	RES	34
R808	RES	34
R809	RES	34
R810	RES	35
R811	RES	25
R812	RES	25
R813	RES	25
R814	RES	25
RP1	RPAK4P	14
RP2	RPAK4P	24
RP3	RPAK4P	24
RP4	RPAK4P	24
RP5	RPAK4P	24
RP6	RPAK4P	14
RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	24
RP10	RPAK4P	24
RP11	RPAK4P	24
RP12	RPAK4P	13
RP13	RPAK4P	24
RP14	RPAK4P	13
RP15	RPAK4P	13
RP16	RPAK4P	13
RP17	RPAK4P	12
RP18	RPAK4P	12
RP19	RPAK4P	12
RP20	RPAK4P	12
RP21	RPAK4P	8
RP22	RPAK4P	12
RP23	RPAK4P	8
RP24	RPAK4P	8 14
RP25	RPAK4P	9
RP26	RPAK4P	9
RP27	RPAK2P	20
RP28	RPAK2P	20
RP29	RPAK4P	14
RP30	RPAK4P	9
RP31	RPAK4P	9
RP32	RPAK2P	20
RP33	RPAK4P	9
RP34	RPAK4P	9
RP35	RPAK4P	9
RP36	RPAK4P	9
RP37	RPAK4P	28
RP38	RPAK4P	28
RP39	RPAK10P2C	17
RP40	RPAK4P	30
RP41	RPAK4P	30
RP42	RPAK10P2C	23
RP43	RPAK10P2C	23
RP44	RPAK4P	25
RP45	RPAK4P	26
RP46	RPAK4P	14
RP47	RPAK4P	14
RP48	RPAK4P	14
RP49	RPAK4P	24
RP50	RPAK4P	24
RP51	RPAK4P	14
RP52	RPAK4P	23 26
RP53	RPAK4P	23
RP54	RPAK4P	26
RP55	RPAK4P	26
RP56	RPAK4P	14
RP57	RPAK2P	20
RP58	RPAK2P	20
RP59	RPAK2P	20
RP60	RPAK2P	20
RP61	RPAK2P	20
SH1	SHLD_3P_EMI	4
SP1	SPKR_CLIP_P84	4
SP2	SPKR_CLIP_P84	4
SP3	SPKR_CLIP_P84	4
SP4	SPKR_CLIP_P84	4
SP5	SPKR_CLIP_P84	4
SP6	SPKR_CLIP_P84	4
T1	XFR_ENET_1000BT	27
U1	SN74AUC1G04	7

U2	SN74AUC1G08	23
U3	ADT7460	25
U4	SN74AUC1G08	23
U5	SIL1162	20
U7	VREG_LT1962	14
U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	34
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	27
U15	COMPARATOR_LMC7211	31
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	32
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	34
U21	COMPARATOR_LMC7211	32
U22	MAX1715	35
U23	AMP_MAX4172	31
U24	7432	22 30
U25	VREG_LP2951	32
U26	PC11510GGU	17
U27	COMPARATOR_LMC7211	30
U28	LTC3707	33
U29	TSB81BA3A	28
U30	VREG_LP2951	32
U31	MAX1772	31
U32	EEPROM_16KX8_M2412BB	23
U33	M14C62	30
U34	VREG_LM2594	28
U35	MAX1916	23
U36	LTC1761	28
U37	VREG_LT1962	28
U38	COMPARATOR_LMC7211	31
U39	UPD720101_FBGA	26
U40	OPAMP_MAX4236EUTT	23
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7445_360	5 6
U44	RAGE_MBLTY_M10_CSP64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U49	TRANSCEIVER_88E1111	27
U50	OPAMP_LMC7111	31
U51	MAX6804	30
U52	FEPR_256KX8_ST72264_BGA	23
U54	VREG_NM157lJ	21
U55	VREG_NM157lJ	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	35
XW1	SHORT	35
XW2	SHORT	19
XW3	SHORT	34
XW4	SHORT	32
XW5	SHORT	34
XW6	SHORT	35
XW7	SHORT	34
XW8	SHORT	33
XW9	SHORT	25
XW11	JUMPER	35
XW12	SHORT	22
XW13	SHORT	22
XW15	SHORT	34
XW19	SHORT	31
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	27
Y4	CRYSTAL	23
Y5	CRYSTAL	26
Y6	CRYSTAL	30
Y7	CRYSTAL_4PIN	30
ET1	HOLE_VIA	4
ET2	MTGHOLE	4
ET3	HOLE_VIA	4
ET4	MTGHOLE	4
ET5	MTGHOLE	4
ET6	MTGHOLE	4
ET7	HOLE_VIA	4
ET8	HOLE_VIA	4
ET9	HOLE_VIA	4
ET10	MTGHOLE	4
ET11	MTGHOLE	4
ET12	HOLE_VIA	4
ET13	HOLE_VIA	4
ET14	HOLE_VIA	4
ET15	HOLE_VIA	4
ET16	MTGHOLE	4
ET17	HOLE_VIA	4
ET18	HOLE_VIA	4
ET19	HOLE_VIA	4
ET20	HOLE_VIA	4
ET21	HOLE_VIA	4
ET22	HOLE_VIA	4
ET23	HOLE_VIA	4
ET24	HOLE_VIA	4
ET25	HOLE_VIA	4
ET26	HOLE_VIA	4
ET27	HOLE_VIA	4
ET28	HOLE_VIA	4
ET29	HOLE_VIA	4
ET30	HOLE_VIA	4
ET31	HOLE_VIA	4
ET32	HOLE_VIA	4
ET33	HOLE_VIA	4
ET34	HOLE_VIA	4
ET35	HOLE_VIA	4
ET36	HOLE_VIA	4
ET37	HOLE_VIA	4
ET38	HOLE_VIA	4
ET39	HOLE_VIA	4
ET40	HOLE_VIA	4
ET41	HOLE_VIA	4
ET42	HOLE_VIA	4
ET43	HOLE_VIA	4
ET44	HOLE_VIA	4
ET45	HOLE_VIA	4
ET46	HOLE_VIA	4
ET47	HOLE_VIA	4
ET48	HOLE_VIA	4
ET49	HOLE_VIA	4
ET50	HOLE_VIA	4
ET51	HOLE_VIA	4
ET52	HOLE_VIA	4
ET53	HOLE_VIA	4
ET54	HOLE_VIA	4
ET55	HOLE_VIA	4
ET56	HOLE_VIA	4
ET57	HOLE_VIA	4
ET58	HOLE_VIA	4
ET59	HOLE_VIA	4
ET60	HOLE_VIA	4
ET61	HOLE_VIA	4
ET62	HOLE_VIA	4
ET63	HOLE_VIA	4
ET64	HOLE_VIA	4
ET65	HOLE_VIA	4
ET66	HOLE_VIA	4
ET67	HOLE_VIA	4
ET68	HOLE_VIA	4
ET69	HOLE_VIA	4
ET70	HOLE_VIA	4
ET71	HOLE_VIA	4
ET72	HOLE_VIA	4
ET73	HOLE_VIA	4
ET74	HOLE_VIA	4
ET75	HOLE_VIA	4
ET76	HOLE_VIA	4
ET77	HOLE_VIA	4
ET78	HOLE_VIA	4
ET79	HOLE_VIA	4
ET80	HOLE_VIA	4
ET81	HOLE_VIA	4
ET82	HOLE_VIA	4
ET83	MTGHOLE	4