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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

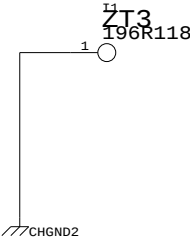
IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD		
1	SIGNAL (1/3 OZ + COPPER PLATING)	
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES



PCB BOARD STANDOFFS

BOARD INFORMATION

NOTICE OF PROPRIETARY PROPERTY

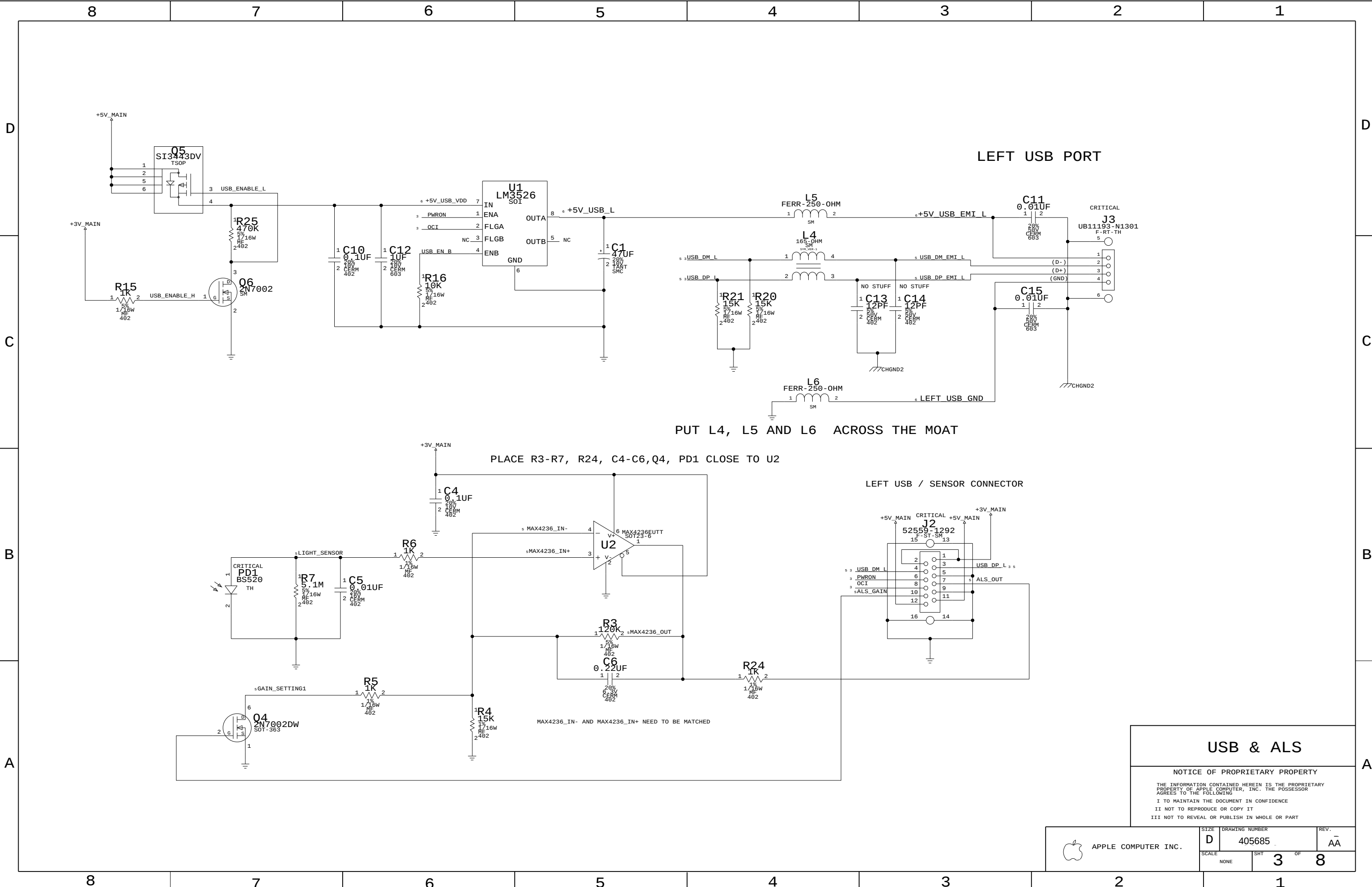
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	SCALE NONE	SHT 2	OF 8



USB & ALS

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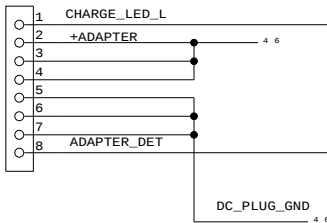
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	SCALE NONE	SHT 3	OF 8

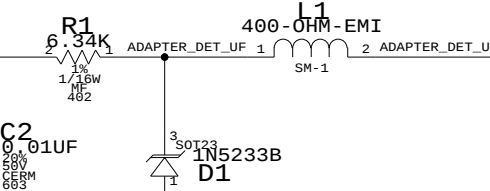
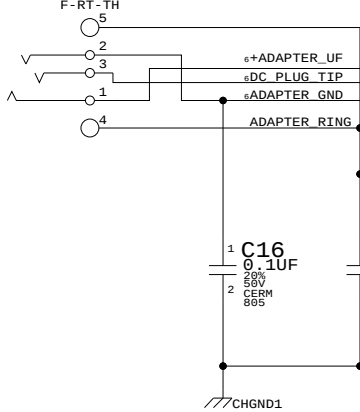
POWER CONNECTOR

CRITICAL
J4
87437-0833
M-ST-SM



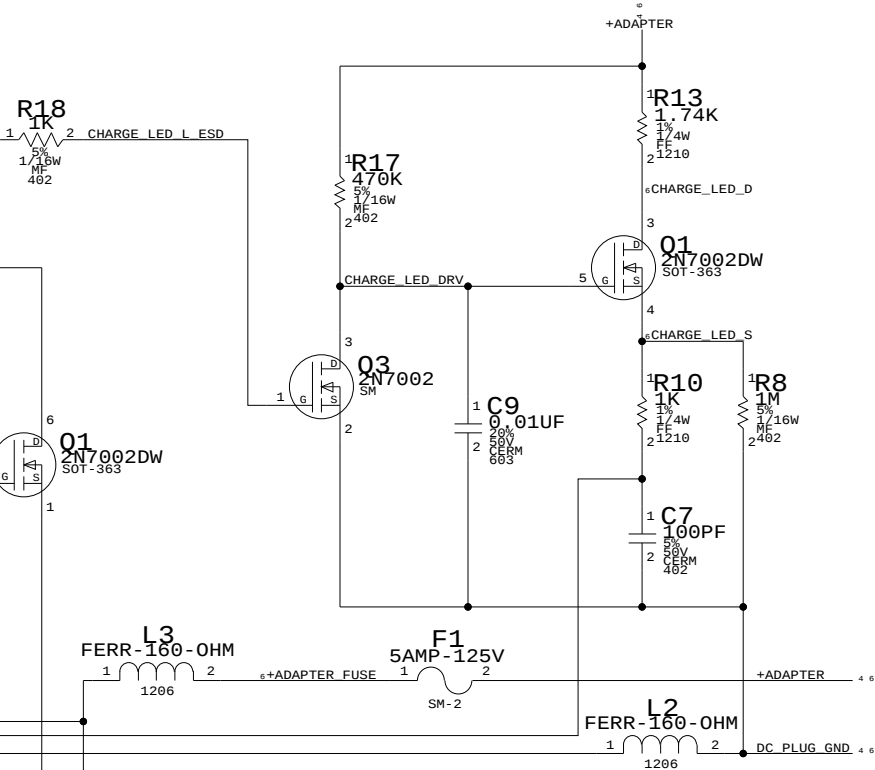
DC POWER JACK

CRITICAL
J1
JPD1133-W01
F-RT-TH



PLACE C2, C3 AND C16 CLOSE TO J1
PLACE L1, L2 AND L3 CLOSE TO J1

CHARGE LED SUPPORT



DC POWER INTERFACE

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 405685	REV. AA
	SCALE NONE	SHT 4	OF 8

REVISION HISTORY

04/22/03 - DESIGN ORIGINATED FROM 051-6282
04/28/03 - PG 3 - REPLACED R19 & R23 WITH 250-OHM 2A FERRITES (TABLE ITEM)
PG 4 - CHANGED C3 TO 0.1UF 0805 (WAS 0.01UF 0603)
EVT 04/29/03 - PG 4 - REPLACED R2 WITH C16 0.1UF 0805 (WAS 0-OHM 0402)
REPLACED R19 & R23 WITH L5 & L6 (PAD CHANGE FOR FERRITES)
CHANGED L2 & L3 FROM 50-OHM FERRITES TO 160-OHM
07/24/03 - PRODUCTION RELEASE

ALS SIGNALS

GROUP	SIG_NAME	DELAY_RULE	MATCHED_DELAY	STUB_LENGTH	MIN_LINE_WIDTH	NET_SPACING_TYPE
ALS						
	LIGHT_SENSOR				MIN_LINE_WIDTH=20	
	GAIN_SETTING1				MIN_LINE_WIDTH=20	
	MAX4236_IN+				MIN_LINE_WIDTH=20	
	MAX4236_IN-				MIN_LINE_WIDTH=20	
	MAX4236_OUT				MIN_LINE_WIDTH=20	
	ALS_GAIN				MIN_LINE_WIDTH=5	
	ALS_OUT				MIN_LINE_WIDTH=10	

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MATCHED_DELAY	MIN_LINE_WIDTH	NET_SPACING_TYPE	MAX_VIAS
USB						
	USB_DM_L	USB_D1	USB_DM:J1.4:L4.1:20	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DP_L	USB_D1	USB_DP:J1.3:L4.2:20	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DM_EMI_L	USB_D1_EMI	USB_D1_EMI:L4.4:J3.2:20	MIN_LINE_WIDTH=5	10 MIL SPACING	
	USB_DP_EMI_L	USB_D1_EMI	USB_D1_EMI:L4.3:J3.3:20	MIN_LINE_WIDTH=5	10 MIL SPACING	

FOR USB DIFFERENTIAL TRACES (ZSINGLE=45 OHM +- 10%, ZDIFF=90 OHM +- 15%)

	MICROSTRIP (OUTER LAYERS)	STRIPLINE (INTERNAL LAYERS)
TRACE WIDTH	4 MIL	5 MIL
SEPARATION OF TRACES	8 MIL	10 MIL

SIGNAL CONSTRAINTS - PAGE 3

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	405685	AA
SCALE	SHT	OF
NONE	5	8

