1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
I		355571	PRODUCTION RELEASED	12/13/04	?

SCHEMATIC,MLB,Q45A ("Rous")

01/21/05

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73	54	PCI SERIES TERMINATION	PCI
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91*	65	USB HOST INTERFACE	USB
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102*	73	AUDIO POWER SUPPLIES	
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* PAGES WHERE MASTER PAGE IS IN A DIFFERENT SCHEMATIC

DIMENSIONS ARE IN MILLIMETERS
XX ± _____
X.XX ± _____
X.XXX ± _____
ANGLES ± _____
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE | SIZE D

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TITLE: SCH,MLB,IMG5

DRAWING NUMBER 051-6482 | REV. I

FREQUENCIES LISTED ARE MAXIMUM DATA TRANSFER RATES SUPPORTED BY U3LITE

U2900
CPU
NEO 10S
PAGE 29

32-BIT
APPLE PI
ELASTIC INTERFACE
1.2V/900MHZ

J5900, J5901
J5902, J5903
17",20" INVERTER
TMDS
EXT VGA
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U1300
SMU
PAGE 13

U1301
RTC
PAGE 13

U5400, U5401
FRAME
BUFFER A
PAGE 54

64-BIT
FRAME BUFFER
2.6V/540MHZ

U4900
GPU
NV18B/NV34
PAGE 49

32-BIT
8X AGP
0.8V/533MHZ
4X = 1.5V
I/O = 1.5V

APPLE PI
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AGP
PAGE 48

U3
U3LITE
CORE
PAGE 22

MAIN MEMORY
PAGE 37

64/128-BIT
MAIN MEMORY
2.6V/400MHZ

SERIES
TERM
PAGE 38

J4000
J4001
DIMMS
PAGE 40

PARALLEL
TERM
PAGES 44&45

64-BIT
FRAME BUFFER
2.6V/540MHZ

U5500, U5501
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BUFFER B
PAGE 55

MISC
PAGE 24

HYPERTRANSPORT
PAGE 60

8-BIT
HYPERTRANSPORT
1.2V/400MHZ
CONTROL = 2.5V

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POWER
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CLOCKS
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J6400
J6401
J6402
HT
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J92107J9220/J9230
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PAGE 92

J9400
MICRODASH MODEM
CONNECTOR
PAGE 94

To Shasta
SCCA

J9240
BLUETOOTH
CONNECTOR
PAGE 92

USB
PAGE 91

U7700
USB 2.0
uPD720101
PCI
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U7500
BOOTROM
PAGE 75

J7600
AIRPORT
EXTREME
CONNECTOR
PAGE 76

EDUCATION: NOT USED
GOOD,BETTER,BEST: HARD DRIVE

JXXXX
SATA
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA1
SATA
PAGE 80

HYPERTRANSPORT
PAGE 62

U2300

PCI
PAGE 74

32-bit PCI (5V-3.3V/33MHz)

FOR DEVELOPMENT ONLY

J8302
SATA DEV
CONNECTOR
PAGE 83

SATA/150
1.2V/1.5GHZ

SATA2

SHASTA

GPIO/PCI64
PAGE 25

EDUCATION: HARD DRIVE
GOOD,BETTER,BEST: OPTICAL

J8301
UATA
CONNECTOR
PAGE 83

UATA/133
3.3V/133MHZ

UATA
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CORE
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NCs
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J9401
CTL-LESS /
SOFT MODEM
CONNECTOR
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ETHERNET
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FIREWIRE
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I2S
PAGE 25
I2S0
SCCA I2S1
SCCB I2S2

GMII (3.3V/125MHz)
8-Bit Tx & 8-Bit Rx

1394 OHCI (3.3V/98MHz)

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AUDIO CODEC
PCM3052
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S/PDIF

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AMP
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LINE OUT

SPEAKER
AMP
PAGE 97

J9801
SPEAKER
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LINE IN
AMP
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U8700
10/100 ETHERNET
BCM5221
PAGE 87

U9000
FIREWIRE A
802A
PAGE 90
0 1

4 Diff pairs

2 Diff pairs

J8700
ETHERNET
CONNECTOR
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J9000, J9001
FIREWIRE A
CONNECTORS
PAGE 90

J9800
LINE IN
CONNECTOR
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J9802
MIC
CONNECTOR
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SYSTEM BLOCK DIAGRAM

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 2 OF 103	

POWER CONNECTOR

J700
PAGE 7

PP24V_RUN
FW CONN
20" LCD INVERTER

PP12V_RUN
20" PANEL POWER
20" LCD INVERTER

PP5V_RUN
HDD & OPTICAL

PP5V_ALL

PP3V3_RUN
PCI BUS
AUDIO CODEC

SYS_POWERUP_L

SMU
POWER SEQUENCE PIN

PULSAR_POWER_DOWN
MAKE_BASE=TRUE
=PULSAR_POWER_DOWN 27
TURN_ON_SHASTA_CORE_L 10
TURN_ON_PP1V2_L 10

SMU_PWRSEQ_P1_4 13
SMU_PWRSEQ_P1_0 13
SMU_PWRSEQ_P1_1 13
SMU_PWRSEQ_P9_5 13 (PWR_GOOD_SB_CORE)
SMU_PWRSEQ_P9_6 13 (PWR_GOOD_PP2V5)
SMU_PWRSEQ_P1_2 13 (TURN_ON_VTT)

PP5V_RUN_AUDIO LINEAR
PAGE 99
5V HP/LINEOUT AMP

PP4V5_RUN_AUDIO LINEAR
PAGE 99
4.5V AUDIO CODEC

CPU CORE SWITCHER
SC2643VX*1
SC1211*4
PAGE 33
0.8~1.2V GPUL

=PP5V_RUN_CPU 6 7 8 31
ALIAS CPU_AVDD_EN 31

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 31
2.8V CPU AVDD

PP5V_PWRON FET SWITCH
PAGE 11
5V USB CONN
UDASH MODEM

PP3V3_ALL LINEAR
PAGE 11
3.3V FW PHY
SMU

PP3V3_PWRON FET SWITCH
PAGE 11
3.3V ENET PHY
USB2 HOST
MODEM & BT

GPU CORE SWITCHER
PAGE 50 IRU3037CS
1.6/1.4V NV18B/NV34

5V

PP1V2_SHASTA_CORE SWITCHER
PAGE 10 IRU3037ACS
1.2V SHASTA CORE

U3LITE CORE SWITCHER
PAGE 22 IRU3037CS
1.53V U3LITE CORE

PP2V5_PWRON SWITCHER
PAGE 9 IRU3037CS
2.62V SHASTA HT
DDR DIMM

PP2V5_PWRON

PP1V2_PWRON FET SWITCH
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PWRON_SD
PWRON_DISK_SB

PP1V2_RUN FET SWITCH
PAGE 10
HT BUS
API BUS

10 6 PPVCORE_PWRON_SB

PP2V5_RUN FET SWITCH
PAGE 9
RAM TERM
GRAPHIC FB

PP1V25_RAM_VTT LINEAR
PAGE 46
1.25V RAM VTT

PP1V5_PWRON LINEAR
PAGE 50
1.5V PULSAR CORE

PP1V5_RUN POWER SW
PAGE 50
AGP BUS

46 TURN_ON_VTT

PP3V3_ALL
R331 10K 5% 1/16W MF 402
PWR_GOOD_SB_CORE

11 RAIL_CTL_NEG
R330 100K 5% 1/16W MF 402
2 COMPARE_SB_CORE 9
C330 0.01UF 20% 16V CERM 402
LM339A SOI
U1100

PP5V_ALL
R342 150K 5% 1/16W MF 402
PS_2V_REF 6

PP3V3_ALL
R341 10K 5% 1/16W MF 402
PWR_GOOD_PP2V5

R340 100K 5% 1/16W MF 402
COMPARE_PP2V5
C340 0.01UF 20% 16V CERM 402
R343 100K 5% 1/16W MF 402

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POWER BLOCK DIAGRAM

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 3 OF 103	

REVISION HISTORY

DATE	DESCRIPTION
02/27/04	EVT3 RELEASE (REV 20)
03/05/04	GPU XTAL - C5700 AND C5719 -> 27PF FROM 22PF I2C A - U1800 MOVED BACK TO PWRON RAIL HEATSINK ASSEMBLY - NEW PART NUMBERS FAN 3 - STUFFING ON ALL CONFIGS FIREWIRE POWER DU JOUR EVT3 - BOM REV 21 RELEASE
03/24/04	MASTER PAGE SYNC EVT3 REWORKS NOSTUFF R807 - SMU_BOOT_SCLK IS ALSO CPU_VID<5> NOSTUFF R3691 & R828 - DIODE CAL RETURN PATH MOVED MARTY SERIAL 0 OHM RESISTORS TO COMMON BOM SMU - ADDED QREQ GPU - ADDED DECOUPLING TO GPU_VTT FOR NV36 INVERTER CONTROL - ADDED AND GATES U5850 & U5851 TO CONTROL LCD_PWM AND FPD_PWR_ON CHECKIN 21001
04/12/04	CPU - CHANGED CPU SYMBOL TO NEO-10S-REV2-76C (OLD IS OBSOLETE) SCHEMATIC REUSE - NETS THAT NEED ALIASES START WITH = (DOES NOT EFFECT NETLIST) 3PHASE CPU POWER SUPPLY - ADDED TABLE FOR R3328 INVERTER - ADDED RESISTORS R5860-1 AND CHANGED R5808-9 TO 47OHM TMDS POWER - ADDED R5960 AND D5914 DIODE CAL - ADDED OPTION TO POWER FROM PP5V_ALL AND PP3V3_ALL RAILS CHECKIN 21002
04/12/04	MASTER PAGE SYNC - IN SYNC ON ALL PAGES EXCEPT PAGE 13 EMI - REMOVED EMI700 & EMI9400 QREQ_L HACK - ADDED U2850, C2850, R2850, R2851 VOLTAGE SENSE FROM 12V - ADDED R3360, R3361 CHECKIN 21003
04/13/04	MAIN MEMORY DQS PARALLEL TERM - CHANGED TO 100 OHM (LIKE EVT3) I/O ALIGNMENT FIXTURE - ADDED 815-8008 TO MLB BOM DIMM CONNECTORS - UPDATED 30 DEGREE SYMBOL GREEN LED - ADDED KINGBRIGHT AS ALTERNATE VTT - NO LONGER POWER SEQUENCED - NO STUFFED R4610 AND R4603 HD TEMP SENSOR - STUFFED ON ALL CONFIGS SMU PULLUPS CHANGES - R1312 -> 2K; R1311 -> 10K SDF804 -> ZH804 CHECKIN 21004
04/14/04	RAM PARALLEL TERM - DQ RPAKS CHANGED TO 68 OHM STROBE RESISTORS CHANGED TO 120 OHM EVT3A RELEASE (REV 22) CHECKIN 22001 - FIXING DIMM SYMBOL CHECKIN 22002 - FIXING DIMM SYMBOL AGAIN
04/21/04	MASTER PAGE SYNC - NOW IN SYNC ON ALL SHAREABLE PAGES MAIN MEMORY - DQ SERIES TERM CHANGED TO 22 OHM MAIN MEMORY - DQ PARALLEL TERM CHANGED TO 82 OHM FIREWIRE POWER - NEW CURRENT LIMITING RESISTOR NOSTUFFING FIREWIRE PORT POWER "CHOICE A" CIRCUIT INPUT VOLTAGE SENSE - CHANGED DIVIDER VALUES INPUT CURRENT SENSE - CHANGED R3343 TO 0.025 OHM 1% RESISTOR CHECKIN 22003
04/21/04	SMU_SUSPENDREQ - STUFFED LEVEL SHIFTER CPU POWER SUPPLY - NOSTUFFED R3305 CHANGED R3304 TO 116S1000 CHANGED C3304-7 TO 132S4733 EVT3A BOM RELEASE REV 23
04/26/04	USB POWER CAPS - NOSTUFFED C9211, C9221, C9231 PULSAR_POWER_DOWN CONNECTED TO SMU_PWRSEQ_P1_4 SW703 CHANGED TO 516S0221 MASTER PAGE SYNC CHECKIN 23001
04/27/04	MASTER PAGE SYNC - AUDIO AND SMU CHANGES SUSPENDACK LEVEL SHIFTER - REPLACED Q2407 AND Q2408 WITH Q2420 SN7002DW I2C_CPU_A - ADDED Q1801 TO LEVEL SHIFTER ADDED POWER SUPPLY TEMP SENSOR Q3000 ADDED TO LEVEL SHIFT / INVERT CPU_BYPASS AND CPU_HRESET CURRENT SENSE - CHANGED R3345 FROM 121K TO 73.2K CHECKIN 23002
04/29/04	QREQ CIRCUITS MOVED TO PWRON RAIL I2C UPDATE NB_SUSPENDACK_L NOW USED U700 TO LEVEL SHIFT - OLD CIRCUIT REMOVED DIMMS - UPDATED TO 25/28 DEGREE CONNECTORS MASTER PAGE SYNC CHECKIN 23003
04/30/04	SOFT MODEM - ADDED DECOUPLING CAPS TO POWER RAIL REMOVED OLD OVERTEMP CIRCUIT ADDED DIAG LED MASTER PAGE SYNC CHECKIN 23004
05/03/04	CPU POWER SUPPLY - ON SEMI FETS ONLY ADDED 1.6GHZ CPU PART NUMBER UPDATED PLATING FOR ZH702 CHECKIN 23005
05/05/04	CPU AVDD - ADDED 2.7V BOM OPTION POWER_FAIL - RESISTOR DIVIDED TO 3.3V ADDED BOMS OPTIONS FOR ON_SEMI AND VISHAY FETS FOR 3PHASE AND 4PHASE CPU PS AVP CHANGES CPU VREG - ADDED BOM OPTION 'EXTRA_C' FOR CAPS WE WOULD LIKE TO NOSTUFF CHECKIN 23006 CPU VREG AVP - C3304, C3305, C3306, C3307 CHANGED TO 8.2NF TMDS TERM - STUFFING CHANGES CHECKIN 23007
05/06/04	DVT RELEASE (REV 24)
05/07/04	TMDS - NEW PARALLEL TERMINATION RESISTORS R5869-R5872 CHECKIN 24001
05/10/04	FRAME BUFFER CLOCKS - ADDED DIFF PAIR PROPERTIES PCI_RESET - UPDATES FOR SCHEMATIC REUSE MASTER PAGE SYNC - ADDED S/PDIF XMITTER AND BITCLK DELAY CHECKIN 24002 AUDIO UPDATES CHECKINS 24003-24005
05/11/04	DVT RELEASE (REV 25)
06/10/04	LAST MINUTE BOM CHANGES FOR DVT: SUSPENDREQ LEVEL SHIFTER - R2419, R2420 CHANGED TO 330 OHM I2C A BUS PULLUPS - R1816,R1817 CHANGED TO 200 OHM USB PULL-DOWNS - R9403,R9404 MOVED TO COMMON BOM SMU CRYSTAL CAPS - C1304,C1305 CHANGED TO 18PF FROM 12PF SMU RESET - CHANGED R1322 TO 150K FROM 100K CPU HEATSINK ASSEMBLIES - NEW PART NUMBERS TMDS POWER - CHANGED D5914 TO SURFACE MOUNT PART FROM THROUGH HOLE MOVED R714 TO R1303 FOR SCHEMATIC REUSE U1600,U1601,U1700 CHANGED TO 353S0890 FOR MORE SOURCES MOVED CPU LOGIC ANALYZER RESISTORS TO DEVELOPMENT BOM CHECKIN 25001
06/11/04 06/21/04	MASTER PAGE SYNC - NOSUFFED EXTERNAL S/PDIF TRANSMITTER ADDED TABLES FOR: NEW 1.5V FET - LOWER RDS(ON) - Q5006 PATA CONN J8301 CHANGED TO 516S0235 (ADDED VENDOR) NEW SATA CONNECTER SOURCES J8300, J8302 NEW TMDS CONNECTOR W/ BOSS J5902 REMOVED COIN CELL BATTERY AND I/O ALIGNMENT FIXTURE FROM MLB BOM (FATP ITEMS) NEW BACKUP SMU_RESET CIRCUIT (SAME AS Q78) CHECKIN 25003
06/22/04	REPLACED Q5006 (FET FOR 1.5V) WITH 376S0254 FAN OPAMPS - REPLACED U1600 W/ SECOND OPAMP IN U1700 TIED INPUTS IN UNUSED OPAMP IN U1601 NOSTUFFED CPU VREG ELECTROLYTIC CAPS C3332, C3427, C3421 NOSTUFFED R2775/6 (UNUSED CLOCKS) CHECKIN 25004
06/22/04 06/23/04	"PROPERLY" TERMINATED UNUSED OPAMP IN U1601 BOM RELEASE REV 26
06/24/04	"PROPERLY" TERMINATED UNUSED OPAMP IN U2100 R5010 REMOVED TO DECREASE DROOP ON 1.5V RAIL ADDED CONNECTOR J1701 TO SUPPORT REMOTE HD TEMP SENSOR CHECKIN 26001
06/28/04	MASTER PAGE SYNC - PICKED UP AUDIO CHANGES RELATED TO BITCLK CHECKIN 26002
06/28/04	SUPPORT FOR 2GB DIMMS - SWAPPED PINS 103 & 167 ON DIMM CONNECTOR CHECKIN 26003
07/01/04	ADDED SECOND SOURCE VTT REGULATOR (PAGE 46) NO STUFF POWER SUPPLY TEMP SENSOR CHANGED HD TEMP SENSOR CONN J1701 TO 4 PIN MASTER PAGE SYNC - AUDIO CHANGES CHECKIN 26004
07/02/04	UPDATED LINE AND NECK WIDTH CONSTRAINTS THROUGHOUT SCHEMATIC NOSTUFFED ON BOARD HD TEMP SENSOR CHANGED U3LITE CORE TO 1.53V FEEDBACK RESISTORS CHANGED TO 603 CHECKIN 26005
07/06/04	REMOVED ON BOARD HARD DRIVE TEMP SENSOR AUDIO DETECT PULLUPS - CHANGED FROM 47K TO 4.7K CHANGED AUDIO I2S_BITCLK SERIES RESISTER TO 0 OHM U3LITE FEEDBACK RESISTORS CHANGED TO 0.5% TOLERANCE CHECKIN 26006
07/08/04	REPLACED MAXIM ANALOG SWITCH U2850 WITH TI ANALOG SWITCH PERICOM ADDED AS AN ALTERNATE ALL I/O CONNECTORS CHANGED POWER CONNECTOR CHANGED POWER SWITCH CHANGED SMU DOWNLOAD CONNECTOR - PRODUCTION P/N CPU PART NUMBERS - UPDATED WITH ACTUAL PART NUMBERS CHECKIN 26007 BOM RELEASE REV 27
07/12/04	CPU VREG DROOP - R3327 CHANGED TO 1.5K; R3326 CHANGED TO 301 PULSAR_POWER_DOWN - R2750 CHANGED TO 47 OHM FOR ICT AUDIO DETECT PULLUPS - CHANGED BACK TO 47K FROM 4.7K AUDIO MUTE PULLDOWNS R9815 & RA012 - CHANGED FROM 47K TO 4.7K MIC BIAS - NOSTUFFED CA210 TO HELP NOISE FLOOR 1.5V_RUN FET - ADDED (N/S) C5060 FOR POSSIBLE SOFT-START 2.5V VREG SOFT START - CHANGED C915 TO 1UF FOR U3L POWER SEQUENCING MLB CARCODE - CHANGED TO 825-6447 I/O CONNECTOR SYMBOL UPDATES CHECKIN 27001
07/13/04	POWER_FAIL_L R DIVIDE - ADJUSTED FOR 2K PULLUP THAT WILL BE IN PVT POWER SUPPLIES ORIGIN HOLE ZH702 - CHANGED TO 4.15MM CHECKIN 27002
07/14/04	FIREWIRE CRYSTAL - ADDED R9060 & R9061 CHECKIN 27003 FIREWIRE CRYSTAL R - FIXED REF DES ANALOG SWITCH U2850 - ADDED PERICOM & AND MAXIM AS ALTERNATES TO TI STUFFED P/S TEMP SENSOR NAMED SOME UNNAMED NETS CHECKIN 27004
07/15/04	U3LITE PWR SEQ - CHANGED C915 TO 0.22UF P/S TEMP SENSOR - NOSTUFF REMOTE HD TEMP SENSOR CONNECTOR - NOSTUFF PVT / PRODUCTION RELEASE 820-1540:A (SCH 051-6482 REV A)
07/28/04	STUFFED TMDS CONNECTOR J5902 (ACCIDENTALLY OMITTED) FIREWIRE CRYSTAL - CHANGED R9061 TO 470 OHM 2.5V VREG - CHANGED SOFT START CAP TO 0.68UF NEW P/N FOR HEATSINK ASSEMBLIES NOSTUFFED OPTICAL TEMP SENSOR STUFFED REMOTE HD TEMP SENSOR CONNECTOR BOM RELEASE (REV B)
08/03/04	2.5V VREG - CHANGED SOFT START CAP TO 0.47UF I/O CONNECTOR SHIELD CHANGE P/N TO 805-5664 NEW CPU P/N AND BINCODES FOR 1.10V VMIN BOM RELEASE (REV C)
08/20/04	TMDS VCC - CHANGED C5918 TO 0.022UF TO LOWER INRUSH CURRENT POWER SWITCH SW703 - MADE FOXCONN 516S0248 AND SUYIN 516S0249 ALTERNATES PATA CONNECTOR J8301 - CHANGED TO 516S0264 TO MATCH REVERSED BOSSES ON FAB BOM RELEASE (REV D)
08/27/04	NOSTUFF SDF700 SW703 - SUYIN WAS REMOVED AS ALTERNATE BOM RELEASE (REV E)
09/14/04	CPU - WAVE5 PROCESSORS ADDED AS ALTERNATES (ARL, BPL, BRL) CPU P/S CAPS - AIR CHANNEL BY STUFFING C3427, C3332 AND NOSTUFFING C3327, C3428 SATABR RESET - STUFFED PULLDOWN R2565 CPU_INT_L - CHANGED R2578 TO 47 OHM TO CURRENT LIMIT BOM RELEASE (REV F)
09/30/04	CPU - 1.6GHZ 1.20V PROCESSORS ADDED AS ALTERNATES (APA, APL) REMOTE HD TEMP SENSOR CONN - CHANGED J1701 TO BLACK 518S0193 KEPT 518S0084 AS ALTERNATE FW SURGE RESISTORS - CHANGED R9056 & R9002 TO 1.3 OHM 107S0060 BOM RELEASE (REV G)
11/15/04	CPU - ADDED HP PROCESSORS AS ALTERNATES (ANA, BNA) AUDIO GROUND - CHANGED R9813 & R9814 TO 0 OHM HD TEMP CONN - REMOVED ALTERNATE CONNECTOR BOM RELEASE (REV H)
12/13/04	CPU DECOUPLING - NOSTUFFED EXTRA_C BOM OPTION U3LITE - ADDED NEW LAMINATE PART AS ALTERNATE BOM RELEASE (REV I)

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SIZE D | DRAWING NUMBER 051-6482 | REV. I

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PROCESSORS

QUALIFIED

	PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
WAVE3	337S2968	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.6G,85C,ARA	1.6GHZ	1.25V	42W	?	U2900	CPU_DD30_1_6GHZ
WAVE3	337S2969	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD3,1.8G,85C,BPA	1.8GHZ	1.20V	42W	?	U2900	CPU_DD30_1_8GHZ

	PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	VOLTAGE
WAVE3	337S2994	337S2968	CPU_DD30_1_6GHZ	U2900	IC,GPUL,DD3,1.6G,APA	1.20V
WAVE5	337S2995	337S2968	CPU_DD30_1_6GHZ	U2900	IC,GPUL,DD3,1.6G,APL	1.20V
WAVE5	337S2980	337S2968	CPU_DD30_1_6GHZ	U2900	IC,GPUL,DD3,1.6G,ARL	1.25V
WAVE5 HP	337S2997	337S2968	CPU_DD30_1_6GHZ	U2900	IC,GPUL,DD3,1.6G,ANA	1.20V
WAVE3	337S2970	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRA	1.25V
WAVE5	337S2981	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BPL	1.20V
WAVE5	337S2982	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BRL	1.25V
WAVE5 HP	337S2998	337S2969	CPU_DD30_1_8GHZ	U2900	IC,GPUL,DD3,1.8G,BNA	1.20V

NOT QUALIFIED

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
337S2865	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,1.8GHZ,85C	1.8GHZ	1.45V	45W	?	U2900	CPU_DD211_1_8GHZ
337S2866	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,DD2.11,2.0GHZ,85C	2.0GHZ	1.45V	45W	?	U2900	CPU_DD211_2_0GHZ
337S2787	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,10S,REV3,2.0G,85C,CJA	2.0GHZ	1.25V	45W	?	U2900	CPU_DD30_2_0GHZ

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0284	1	IC,U3LITE,V1.1,300MM,PBGA	U3	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
343S0282	343S0284		U3	U3L,V1.1,200MM,PBGA
343S0321	343S0284		U3	U3L,NEW LAM,200MM
343S0320	343S0284		U3	U3L,NEW LAM,300MM

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
343S0283	1	IC,ASIC,SHASTA,V1.1,PBGA	U2300	

MISC PARTS

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
	062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1	
	820-1540	1	PCB,FAB,MLB	MLB1	
	825-6447	1	BARCODE LABEL, MLB, Q45	LBL1	
	051-6482	1	PCB,SCHEM,MLB	SCH1	
	341T1366	1	IC,FLASH,1MX8,3.3V,90NS	U7500	
	341T1395	1	PURCH ASSY, SMU BIG	U1300	
CRITICAL	603-6015	1	HEAT SINK ASSEMBLY 17 IN	MECH17	17_INCH_LCD
CRITICAL	603-6016	1	HEAT SINK ASSEMBLY 20 IN	MECH20	20_INCH_LCD

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0119	378S0114	LED700,LED702,LED5900		KINGBRIGHT LED

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TABLE ITEMS

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I

SCALE	SHT	OF
NONE	5	103

NO_TEST=YES TP_BUF_RST 57
NO_TEST=YES TP_DFPCLK 58
NO_TEST=YES TP_DFPCLK_L 58
NO_TEST=YES TP_DFPD0 58
NO_TEST=YES TP_DFPD1 58
NO_TEST=YES TP_DFPD2 58
NO_TEST=YES TP_DFPD3 58
NO_TEST=YES TP_DFPD5 58
NO_TEST=YES TP_DFPD6 58
NO_TEST=YES TP_EXT_TMDS_CKM 58
NO_TEST=YES TP_EXT_TMDS_CKP 58
NO_TEST=YES TP_EXT_TMDS_D0M 58
NO_TEST=YES TP_EXT_TMDS_D0P 58
NO_TEST=YES TP_EXT_TMDS_D1M 58
NO_TEST=YES TP_EXT_TMDS_D1P 58
NO_TEST=YES TP_EXT_TMDS_D2M 58
NO_TEST=YES TP_EXT_TMDS_D2P 58

NO_TEST=YES TP_FBBCS1_L 52
NO_TEST=YES TP_GPU_INTB_L 49
NO_TEST=YES TP_GPU_THERMA 58
NO_TEST=YES TP_GPU_THERMC 58
NO_TEST=YES TP_IFP1VREF 58
NO_TEST=YES TP_NVAGP_TDO 49

NO_TEST=YES TP_TMDS_TXD3M 58
NO_TEST=YES TP_TMDS_TXD3P 58
NO_TEST=YES TP_TMDS_TXD7M 58
NO_TEST=YES TP_TMDS_TXD7P 58
NO_TEST=YES TP_VIPHCLK 57
NO_TEST=YES TP_FRWRLPS 58
NO_TEST=YES TP_AGP_MB_AGP8X_DET_L 48
NO_TEST=YES TP_ATTENTION 29
NO_TEST=YES TP_ENET_CLK125M_GTX 87
NO_TEST=YES TP_ENET_TXD<7> 87
NO_TEST=YES TP_ENET_TXD<4> 87
NO_TEST=YES TP_ENET_TXD<5> 87
NO_TEST=YES TP_FW_CLK98M_LCLK 90
NO_TEST=YES TP_AFN 29
NO_TEST=YES TP_PSRO1 29
NO_TEST=YES TP_PSRO2 29
NO_TEST=YES TP_PSYNCOUT 29
NO_TEST=YES TP_USB2_PWREN<2> 92
NO_TEST=YES TP_USB2_PWREN<3> 92
NO_TEST=YES TP_USB2_PWREN<4> 92

NO_TEST=YES TP_NEC_AMC 77
NO_TEST=YES TP_NEC_NANDTEST 77
NO_TEST=YES TP_NEC_NTEST1 77
NO_TEST=YES TP_NEC_SMC 77
NO_TEST=YES TP_NEC_SMI_L 77
NO_TEST=YES TP_NEC_SRCLK 77
NO_TEST=YES TP_NEC_SRDATA 77
NO_TEST=YES TP_NEC_SRMOD 77
NO_TEST=YES TP_NEC_TEB 77
NO_TEST=YES TP_NEC_TEST 77
NO_TEST=YES TP_PLS_CLK_66M_0 27
NO_TEST=YES TP_PLS_CLK_66M_1 27
NO_TEST=YES TP_PLS_REF_CML 27
NO_TEST=YES TP_PLS_TEST1 27
NO_TEST=YES TP_PLS_TEST2 27
NO_TEST=YES TP_PLS_TEST3 27
NO_TEST=YES TP_SB_FSTEST 25
NO_TEST=YES TP_SB_PLLTEST 25
NO_TEST=YES TP_VREF_CG 48
NO_TEST=YES TP_SB_NC_P7 91
NO_TEST=YES TP_SB_NC_P8 91
NO_TEST=YES TP_SB_NC_R3 91
NO_TEST=YES TP_SB_NC_R4 91
NO_TEST=YES TP_SB_NC_R5 91
NO_TEST=YES TP_SB_NC_R6 91
NO_TEST=YES TP_SB_NC_R7 91
NO_TEST=YES TP_SB_NC_R8 91
NO_TEST=YES TP_SB_NC_T1 91
NO_TEST=YES TP_SB_NC_T2 91
NO_TEST=YES TP_SB_NC_T3 91
NO_TEST=YES TP_SB_NC_T4 91
NO_TEST=YES TP_SB_NC_T5 91
NO_TEST=YES TP_SB_NC_T6 91
NO_TEST=YES TP_SB_NC_T7 91
NO_TEST=YES TP_SB_NC_T8 91
NO_TEST=YES TP_SB_NC_U1 91
NO_TEST=YES TP_SB_NC_U2 91
NO_TEST=YES TP_SB_NC_U3 91
NO_TEST=YES TP_SB_NC_U4 91
NO_TEST=YES TP_SB_NC_U5 91
NO_TEST=YES TP_SB_NC_U6 91
NO_TEST=YES TP_SB_NC_V1 91
NO_TEST=YES TP_SB_NC_V2 91
NO_TEST=YES TP_SB_NC_V3 91
NO_TEST=YES TP_SB_NC_V4 91
NO_TEST=YES TP_SB_NC_W1 91
NO_TEST=YES TP_SB_NC_W3 91
NO_TEST=YES TP_SB_NC_Y1 91
NO_TEST=YES TP_SB_NC_Y3 91
NO_TEST=YES TP_SATA_CLK25M 27
NO_TEST=YES TP_ENET_TCK 87
NO_TEST=YES TP_USB2_PWREN<0> 92
NO_TEST=YES TP_USB2_PWREN<1> 92
NO_TEST=YES TP_DUMMY_A 24
NO_TEST=YES TP_DUMMY_B 24
NO_TEST=YES TP_RAM_CKE_R<2> 8

NO_TEST=YES TP_RAM_CKE_R<3> 8
NO_TEST=YES TP_RAM_CKE_R<6> 8
NO_TEST=YES TP_RAM_CKE_R<7> 8
NO_TEST=YES TP_RAM_CS_L_R<10> 8
NO_TEST=YES TP_RAM_CS_L_R<11> 8
NO_TEST=YES TP_RAM_CS_L_R<2> 8
NO_TEST=YES TP_RAM_CS_L_R<3> 8
NO_TEST=YES TP_RAM_MUXEN0 8
NO_TEST=YES TP_RAM_MUXEN4 8
NO_TEST=YES TP_NB_PM_SLEEP0 24
NO_TEST=YES TP_J4000_SJRESET_L 40
NO_TEST=YES TP_J4001_SJRESET_L 40
NO_TEST=YES TP_CMP_SPARE
NO_TEST=YES TP_ENET_TXD<6> 87
NO_TEST=YES U2100_UNUSED 21
NO_TEST=YES PLS_CLK_66M_0_R 27
NO_TEST=YES PLS_CLK_66M_1_R 27

GENZ SHOULD USE J1400 FOR THE FOLLOWING NETS:

NO_TEST=TRUE EI_CPU_TO_NB_AD<0..43> 14 28 29
NO_TEST=YES EI_CPU_TO_NB_CLK_N 14 28 29
NO_TEST=YES EI_CPU_TO_NB_CLK_P 14 28 29
NO_TEST=TRUE EI_CPU_TO_NB_SR_N<0..1> 14 28 29
NO_TEST=TRUE EI_CPU_TO_NB_SR_P<0..1> 14 28 29
NO_TEST=TRUE EI_NB_TO_CPU_AD<0..43> 14 28 29
NO_TEST=YES EI_NB_TO_CPU_CLK_N 14 28 29
NO_TEST=YES EI_NB_TO_CPU_CLK_P 14 28 29
NO_TEST=TRUE EI_NB_TO_CPU_SR_N<0..1> 14 28 29
NO_TEST=TRUE EI_NB_TO_CPU_SR_P<0..1> 14 28 29
NO_TEST=YES CHKSTOP_L 8 14 29
NO_TEST=YES CPU_HRESET_L 14 29 30
NO_TEST=YES CPU_INT_L 14 25 29 30
NO_TEST=YES CPU1_HTBEN 14
NO_TEST=YES EI_CPU1_CLK_N 14 27
NO_TEST=YES EI_CPU1_CLK_P 14 27
NO_TEST=YES EI_QACK_L 14 28 29
NO_TEST=YES EI_QREQ_L 14 28 29 30
NO_TEST=YES EI_SE 14 28 29 30
NO_TEST=YES I2C_SMU_A_SCL_OUT_L 13 14 18
NO_TEST=YES I2C_SMU_A_SDA_OUT_L 13 14 18
NO_TEST=YES MCP_L 14 29
NO_TEST=YES RI_L 14 29 30
NO_TEST=YES SYNCENABLE 14 29 30
NO_TEST=YES TP_PROC_TRIGGER_OUT 14 29
NO_TEST=YES EI_CPU1_SYNC 14 27

90 IN FW_VP_PORT1 FUNC_TEST=YES
90 IN FW_TPO1P FUNC_TEST=YES
90 IN FW_TPO1N FUNC_TEST=YES
90 IN FW_TPI1P FUNC_TEST=YES
90 IN FW_TPI1N FUNC_TEST=YES
90 IN FW_VP_PORT2 FUNC_TEST=YES
90 IN FW_TPO2P FUNC_TEST=YES
90 IN FW_TPO2N FUNC_TEST=YES
90 IN FW_TPI2P FUNC_TEST=YES
90 IN FW_TPI2N FUNC_TEST=YES
90 IN FW_VGND FUNC_TEST=YES

77 76 75 74 73 IN PCI_AD<31..0> FUNC_TEST=TRUE
77 76 74 73 IN PCI_CBE_L<3..0> FUNC_TEST=TRUE
8 IN PCI_CLK33M_AIRPORT FUNC_TEST=YES
76 74 IN PCI_SLOTA_REQ_L FUNC_TEST=YES
76 74 IN PCI_SLOTA_GNT_L FUNC_TEST=YES
76 25 IN PCI_SLOTA_INT_L FUNC_TEST=YES
74 58 51 8 IN PCI_RESET_L FUNC_TEST=YES
77 76 74 73 IN PCI_FRAME_L FUNC_TEST=YES
77 76 74 73 IN PCI_TRDY_L FUNC_TEST=YES
77 76 74 73 IN PCI_IRDY_L FUNC_TEST=YES
77 76 74 73 IN PCI_STOP_L FUNC_TEST=YES
77 76 74 73 IN PCI_DEVSEL_L FUNC_TEST=YES
77 76 74 73 IN PCI_PAR FUNC_TEST=YES
76 IN PCI_SLOTA_IDSEL FUNC_TEST=YES
76 75 74 IN ROM_CS_L FUNC_TEST=YES
76 75 74 IN ROM_OE_L FUNC_TEST=YES
76 75 74 IN ROM_WE_L FUNC_TEST=YES
76 75 IN ROM_ONBOARD_CS_L FUNC_TEST=YES
76 IN AIRPORT_CLKRUN_L_PD FUNC_TEST=YES

92 IN USB_BT_N FUNC_TEST=YES
92 IN USB_BT_P FUNC_TEST=YES

92 IN USB2_PORT1_N_F FUNC_TEST=YES
92 IN USB2_PORT1_P_F FUNC_TEST=YES
92 IN USB2_PORT2_N_F FUNC_TEST=YES
92 IN USB2_PORT2_P_F FUNC_TEST=YES
92 IN USB2_PORT3_N_F FUNC_TEST=YES
92 IN USB2_PORT3_P_F FUNC_TEST=YES
92 IN PP5V_USB2_PORT1_F FUNC_TEST=YES
92 IN PP5V_USB2_PORT2_F FUNC_TEST=YES
92 IN PP5V_USB2_PORT3_F FUNC_TEST=YES

94 76 25 IN I2S1_DEV_TO_SB_DTI 2 TEST POINTS FUNC_TEST=YES
94 25 IN I2S1_SYNC 2 TEST POINTS FUNC_TEST=YES
94 25 IN I2S1_BITCLK 2 TEST POINTS FUNC_TEST=YES
94 76 25 IN I2S1_MCLK 2 TEST POINTS FUNC_TEST=YES
94 76 25 IN I2S1_SB_TO_DEV_DTO 2 TEST POINTS FUNC_TEST=YES
94 25 IN I2S1_RESET_L 2 TEST POINTS FUNC_TEST=YES
94 25 IN MODEM_RING2SYS_L 2 TEST POINTS FUNC_TEST=YES
94 18 IN I2C_UDASH_SDA FUNC_TEST=YES
94 18 IN I2C_UDASH_SCL FUNC_TEST=YES
94 IN USB_UDASH_N FUNC_TEST=YES
94 IN USB_UDASH_P FUNC_TEST=YES
94 25 IN UDASH_SDOWN FUNC_TEST=YES
94 25 IN UDASH_RESET_L FUNC_TEST=YES
94 IN UDASH_I2C_A1_PU FUNC_TEST=YES

59 IN PPVCC_TMDS FUNC_TEST=YES
59 IN PP3V3_DDC FUNC_TEST=YES
59 IN TD0M FUNC_TEST=YES
59 IN TD0P FUNC_TEST=YES
59 IN TD1M FUNC_TEST=YES
59 IN TD1P FUNC_TEST=YES
59 IN TD2M FUNC_TEST=YES
59 IN TD2P FUNC_TEST=YES
59 IN TCKM FUNC_TEST=YES
59 IN TCKP FUNC_TEST=YES
59 IN TMDS_DDC_DAT FUNC_TEST=YES
59 IN TMDS_DDC_CLK FUNC_TEST=YES
59 7 IN GND_CHASSIS_TMDS FUNC_TEST=YES

59 IN FILT_ANALOG_RED FUNC_TEST=YES
59 IN FILT_ANALOG_GRN FUNC_TEST=YES
59 IN FILT_ANALOG_BLU FUNC_TEST=YES
59 57 56 IN ANALOG_HSYNC_L FUNC_TEST=YES
59 57 56 IN ANALOG_VSYNC_L FUNC_TEST=YES
59 IN VGA_IIC_CLK FUNC_TEST=YES
59 IN VGA_IIC_DAT FUNC_TEST=YES
59 58 IN MON_DETECT FUNC_TEST=YES
59 IN DDC_VCC_5 FUNC_TEST=YES

59 IN PP24V_INV FUNC_TEST=YES
59 IN GND_20_INV FUNC_TEST=YES
59 IN INV_20_LCD_PWM_ FUNC_TEST=YES
59 IN INV_20_CUR_HI_F FUNC_TEST=YES
59 IN PP12V_INV FUNC_TEST=YES
59 IN GND_17_INV FUNC_TEST=YES
59 IN PP5V_AGP_RL FUNC_TEST=YES
59 IN INV_17_LCD_PWM_F FUNC_TEST=YES
59 IN LAMP_STS_F FUNC_TEST=YES
59 IN INV_17_CUR_HI_F FUNC_TEST=YES

33 8 IN CPU_VID_R<5..0> FUNC_TEST=TRUE
36 IN KPVDD2_FMAX FUNC_TEST=YES
36 IN KPGND2_FMAX FUNC_TEST=YES
36 IN TDIODE_POS_FMAX FUNC_TEST=YES
36 IN TDIODE_NEG_FMAX FUNC_TEST=YES
36 33 IN CORE_ISNS_M FUNC_TEST=YES
36 33 IN CORE_ISNS_P FUNC_TEST=YES

PP12V_RUN PP5V_RUN PP24V_RUN PP5V_ALL PP3V3_RUN

IN PP12V_RUN 10 TEST POINTS FUNC_TEST=YES
11 7 IN PP5V_ALL 5 TEST POINTS FUNC_TEST=YES
18 11 IN PP5V_RUN 5 TEST POINTS FUNC_TEST=YES
18 11 IN PP3V3_RUN 5 TEST POINTS FUNC_TEST=YES
IN PP24V_RUN 5 TEST POINTS FUNC_TEST=YES
83 7 IN =PP5V_DISK 5 TEST POINTS FUNC_TEST=YES
83 7 IN =PP12V_DISK 5 TEST POINTS FUNC_TEST=YES
IN GND 12 TEST POINTS FUNC_TEST=YES

PP2V5_RUN PP5V_PWRON PP1V2_PWRON PP1V5_RUN PP3V3_PWRON

IN PP2V5_RUN FUNC_TEST=YES
IN PP1V5_RUN FUNC_TEST=YES
18 13 IN PP5V_PWRON FUNC_TEST=YES
27 18 13 IN PP3V3_PWRON FUNC_TEST=YES
IN PP1V2_PWRON FUNC_TEST=YES
10 2 IN PPVCORE_PWRON_SB FUNC_TEST=YES
13 8 7 IN =PP3V3_ALL_SMU FUNC_TEST=TRUE
31 8 7 7 IN =PP5V_RUN_CPU FUNC_TEST=YES
22 7 IN PPVCORE_NB FUNC_TEST=YES
35 34 33 7 IN PPVCORE_CPU FUNC_TEST=YES
34 33 IN PP12V_CPU FUNC_TEST=YES
33 IN VCORE_SENSE_GND FUNC_TEST=YES
33 IN VCORE_SENSE_VOUT FUNC_TEST=YES
8 7 IN SMU_MANUAL_RESET_L 2 TEST POINTS FUNC_TEST=YES
13 7 IN SYS_POWER_BUTTON_L 2 TEST POINTS FUNC_TEST=YES
7 IN POWER_BUTTON_L FUNC_TEST=YES
7 IN RESET_BUTTON_L FUNC_TEST=YES
13 8 IN SMU_RESET_L FUNC_TEST=YES
33 13 11 10 7 IN SYS_POWERUP_L FUNC_TEST=YES
50 46 11 10 9 8 IN SYS_SLEEP FUNC_TEST=YES
13 8 IN SYS_POWERFAIL_L FUNC_TEST=YES
IN EXT_POWER_BUTTON_L FUNC_TEST=TRUE
9 IN U900_FEEDBACK FUNC_TEST=YES
22 IN U2200_FEEDBACK FUNC_TEST=YES
59 57 IN ANALOG_RED FUNC_TEST=YES
59 57 IN ANALOG_GRN FUNC_TEST=YES
59 57 IN ANALOG_BLU FUNC_TEST=YES
IN AUDIO_LI_DETECT_L FUNC_TEST=TRUE
101 25 IN AUDIO_LO_DET_L FUNC_TEST=YES
75 IN ROM_WP_L FUNC_TEST=YES

83 80 IN UATA_DD<15..0> FUNC_TEST=TRUE
83 80 IN UATA_DA<2..0> FUNC_TEST=TRUE
83 80 IN UATA_CS0_L FUNC_TEST=YES
83 80 IN UATA_CS1_L FUNC_TEST=YES
83 80 IN UATA_RESET_L FUNC_TEST=YES
83 IN UATA_DSTROBE_R FUNC_TEST=YES
83 80 IN UATA_HSTROBE FUNC_TEST=YES
83 8046 83 80 IN UATA_STOP FUNC_TEST=YES
83 IN UATA_DMARQ_R FUNC_TEST=YES
83 80 IN UATA_DMACK_L FUNC_TEST=YES
83 IN UATA_INTRQ_R FUNC_TEST=YES
83 IN UATA_IOCS16_PU FUNC_TEST=YES
83 IN UATA_CSEL_PD FUNC_TEST=YES

36 31 IN TDIODE_NEG FUNC_TEST=YES
76 IN TP_AIRPORT_PME_L FUNC_TEST=YES
76 IN TP_AIRPORT_RF_DISABLE FUNC_TEST=YES

FUNC TEST

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 6 OF 103	

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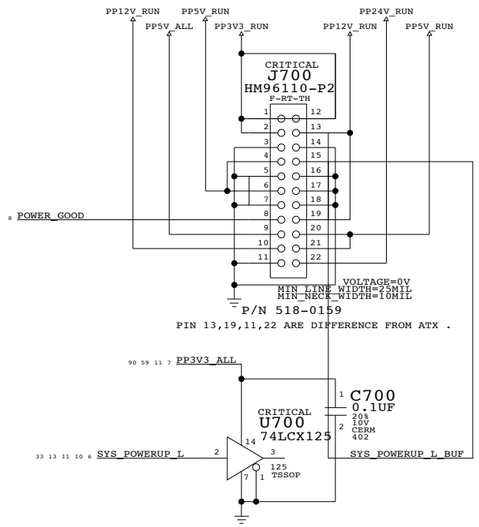
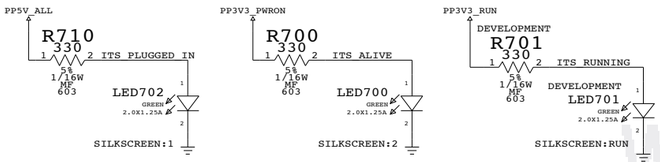
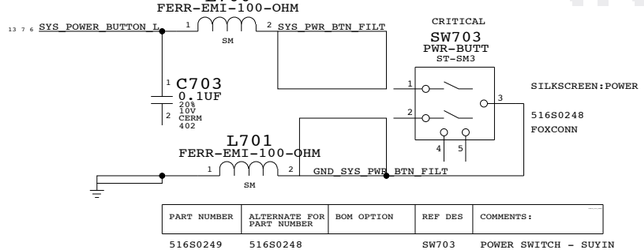
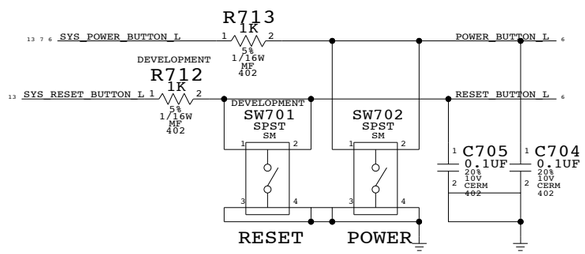


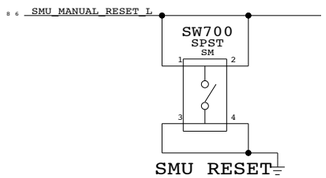




PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
516S0249	516S0248		SW703	POWER SWITCH - SUYIN

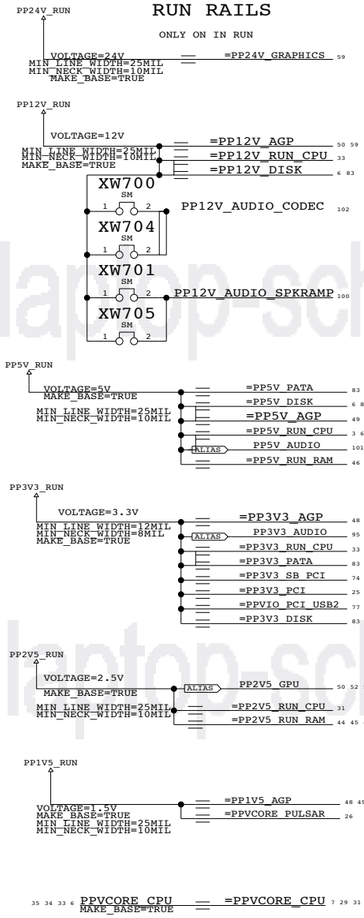
SUYIN WILL NOT BE USED FOR INITIAL RAMP





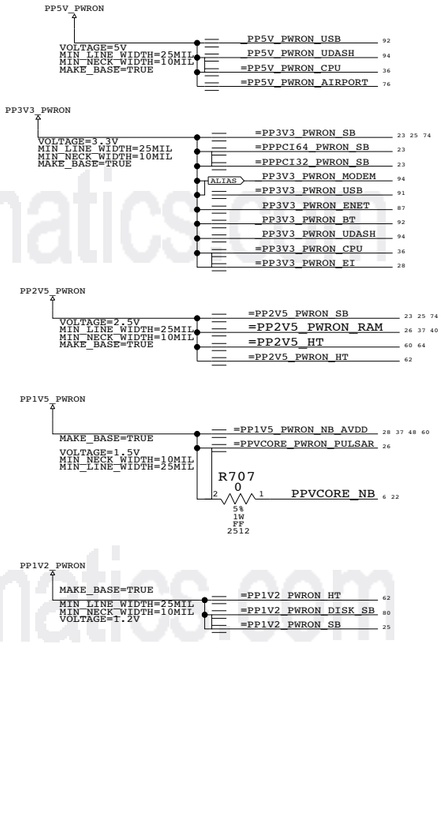
RUN RAILS

ONLY ON IN RUN



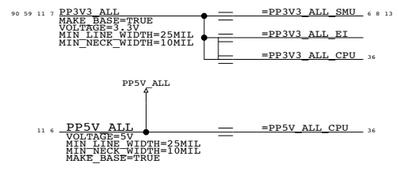
PWRON RAILS

ON IN RUN AND SLEEP

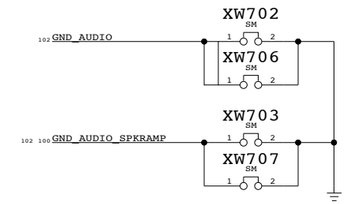


ALL RAILS

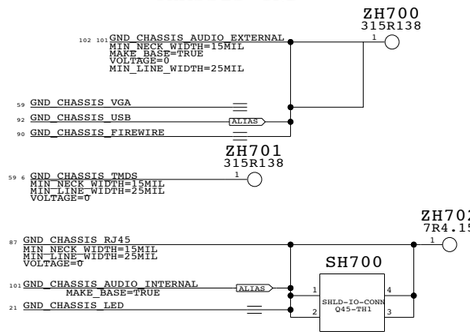
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)



GND RAILS

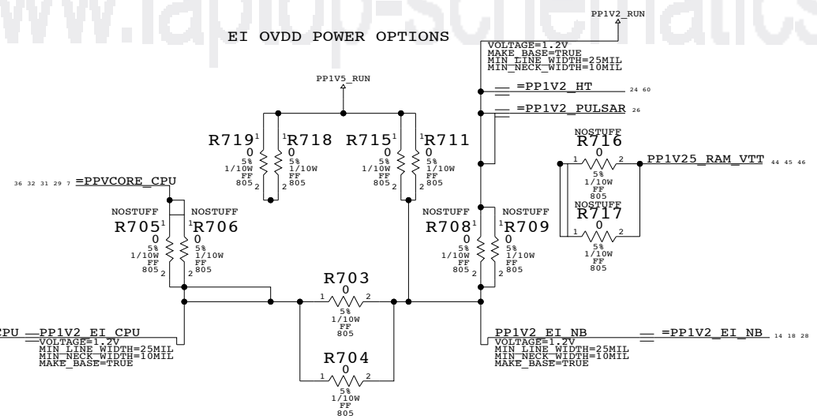


CHASSIS GND



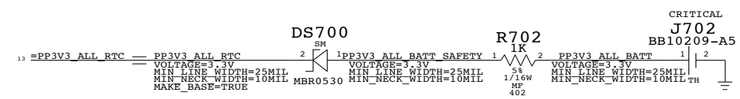
SDF700 IS USED FOR CPU HEATSINK MOUNTING

EI OVDD POWER OPTIONS



RTC BATTERY

ALWAYS ON (TRICKLE)



POWER CONN / ALIAS

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PCI CLOCKS

TP_NB_THMI MAKE_BASE=TRUE ALIAS → NB_THMI (24)
TP_THMO MAKE_BASE=TRUE ALIAS → NB_THMO (24)
TP_RAM_CKE_R<2> MAKE_BASE=TRUE ALIAS → RAM_CKE_R<2> (37)
TP_RAM_CKE_R<3> MAKE_BASE=TRUE ALIAS → RAM_CKE_R<3> (37)
TP_RAM_CKE_R<6> MAKE_BASE=TRUE ALIAS → RAM_CKE_R<6> (37)
TP_RAM_CKE_R<7> MAKE_BASE=TRUE ALIAS → RAM_CKE_R<7> (37)
TP_RAM_MUXEN0 MAKE_BASE=TRUE ALIAS → RAM_MUXEN0 (37)
TP_RAM_MUXEN4 MAKE_BASE=TRUE ALIAS → RAM_MUXEN4 (37)
TP_RAM_CS_L_R<2> MAKE_BASE=TRUE ALIAS → RAM_CS_L_R<2> (37)
TP_RAM_CS_L_R<3> MAKE_BASE=TRUE ALIAS → RAM_CS_L_R<3> (37)
TP_RAM_CS_L_R<10> MAKE_BASE=TRUE ALIAS → RAM_CS_L_R<10> (37)
TP_RAM_CS_L_R<11> MAKE_BASE=TRUE ALIAS → RAM_CS_L_R<11> (37)

PCI_CLK33M_USB2 MAKE_BASE=TRUE → =PCI_CLK33M_USB2 (77)
PCI_CLK_GP0 → (27)
TP_PCI_CLK_GP1 MAKE_BASE=TRUE ALIAS → PCI_CLK_GP1 (27)
PCI_CLK33M_AIRPORT MAKE_BASE=TRUE → PCI_CLK_P3 (27)
PCI_CLK33M_AIRPORT (76)
TP_PCI_CLK_P4 MAKE_BASE=TRUE ALIAS → PCI_CLK_P4 (27)
PCI_CLK33M_SB_EXT MAKE_BASE=TRUE ALIAS → PCI_CLK_P1 (27)

SMU

TP_ALS0_OUT MAKE_BASE=TRUE ALIAS → ALS0_OUT (13)
TP_ALS1_OUT MAKE_BASE=TRUE ALIAS → ALS1_OUT (13)
TP_ALS_GAIN_BOOST MAKE_BASE=TRUE ALIAS → ALS_GAIN_BOOST (13)
TP_SMU_ONEWIRE MAKE_BASE=TRUE ALIAS → SMU_ONEWIRE (13)
TP_SYS_SLOT_PWR MAKE_BASE=TRUE ALIAS → SYS_SLOT_PWR (13)
TP_SMU_PWRSEQ_P1_3 MAKE_BASE=TRUE ALIAS → SMU_PWRSEQ_P1_3 (13)
TP_SYS_DOOR_AJAR_L MAKE_BASE=TRUE ALIAS → SYS_DOOR_AJAR_L (13)
TP_FAN_PWM8 MAKE_BASE=TRUE ALIAS → FAN_PWM8 (13)
TP_SYS_DRIVE_BAY_INT_L MAKE_BASE=TRUE ALIAS → SYS_DRIVE_BAY_INT_L (13)
SMU_WARM_RESET_L MAKE_BASE=TRUE ALIAS → NB_WARM_RESET_L (24)

PCI_RESET_L MAKE_BASE=TRUE → PCI_AIRPORT_RESET_L (76)
GPU_RESET_L (49)
=PCI_ROM_RESET_L (75)
=PCI_USB2_RESET_L (77)

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCB SMU_RESET	10 MIL SPACING		SYS_COLD_RESET_L (13 24)
PCB SMU_RESET	10 MIL SPACING		SYS_WARM_RESET_L (8 25 74 77 87)

DIAG LED

PP5V_ALL
R850 180 5% 1/16W MF 402
LED850P1
LED850 RED SM
LED850P2
Q850 2N3904 SM
R851 1K 5% 1/16W MF 402
DIAG_LED (13) MAKE_BASE=TRUE — DIAG_LED_R

CPU VID<0:5>

VID CONTROLLED BY SMU

PP3V3_RUN
R814 10K, R816 10K, R817 10K, R808 10K, R809 10K, R804 10K (5% 1/16W MF 402)

CPU_VID<0> (13) — R819 0 — CPU_VID_R<0> (6 33)
CPU_VID<1> (13) — R820 0 — CPU_VID_R<1> (6 33)
CPU_VID<2> (13) — R821 0 — CPU_VID_R<2> (6 33)
CPU_VID<3> (13) — R822 0 — CPU_VID_R<3> (6 33)
CPU_VID<4> (13) — R823 0 — CPU_VID_R<4> (6 33)
CPU_VID<5> (13) — R824 0 — CPU_VID_R<5> (6 33)
(5% 1/16W MF 402)

NOSTUFF J803 BM12B-SRSS-TB F-ST-SM (pins 1–13)
NOSTUFF R832 1K, R831 1K, R830 1K, R829 1K, R827 1K, R811 20K (5% 1/16W MF 402)

NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

BACKUP SMU RESET CIRCUIT

=PP3V3_ALL_SMU (13 7 6)
NOSTUFF C800 0.1UF 20% 10V CERM 402
NOSTUFF R890 1K 5% 1/16W MF 402
U890 SM: VCC, DELAY, NOSTUFF_RESET, GND — VOLTAGE DETECTOR MC33465N_30ATR
SMU_MANUAL_RESET_L (8 7 6) — SMU_RESET_L (6 13)
NOSTUFF C890 0.01UF 10% 16V CERM 402
NOSTUFF C891 1UF 10% 6.3V CERM 402
R810 0 5% 1/16W MF 402

PULSAR ERROR_L LED

PP3V3_RUN
DEVELOPMENT R801 4.7K 5% 1/16W MF 402
DEVELOPMENT R800 330 5% 1/16W MF 402
ERROR_LED
DEVELOPMENT D810 RED SM
CLOCK_ERROR_L (27)

DOWNLOAD CONNECTOR

PP3V3_ALL
J802 HCT7051 M-ST-TH (518-0158)
SMU_BOOT_SCLK (13) — SMU_BOOT_CE (13) — SMU_BOOT_CNVSS (13)
R826 100 5% 1/16W MF 402
J802_2 — SMU_BOOT_BUSY (13)
SMU_BOOT_RXD (13)
J802_6 — (SMU_BOOT_EPM)
SMU_MANUAL_RESET_L (6 7 8)
SMU_BOOT_TXD (13)
R806 10K, NOSTUFF R807 10K, R805 0, R803 10K (5% 1/16W MF 402)

J802 & R826 CAN MOVE TO DEVELOPMENT BOM POST RAMP

PLL LOCK LED

=PP5V_RUN_CPU (31 8 7 6 3)
DEVELOPMENT R837 180 5% 1/16W MF 402
DEVELOPMENT Q802 2N3906 SM
Q802_B — Q802_E
DEVELOPMENT R838 1K 5% 1/16W MF 402
DEVELOPMENT R835 180 5% 1/16W MF 402
Q803_C
DEVELOPMENT Q803 2N3904 SM
LED802_1
DEVELOPMENT LED802 GREEN 2.0X1.25A
DEVELOPMENT R839 180 5% 1/16W MF 402
PLLLOCK (29) — Q803_B

CHKSTOP LED

=PP5V_RUN_CPU (31 8 7 6 3)
DEVELOPMENT R833 180 5% 1/16W MF 402
LED801_1
DEVELOPMENT LED801 RED SM
Q800_D
DEVELOPMENT Q800 2N7002 SM
DEVELOPMENT R834 180 5% 1/16W MF 402
Q800_G
DEVELOPMENT R836 180 5% 1/16W MF 402
CHKSTOP_L (29 14 6) — Q801_B
DEVELOPMENT Q801 2N3904 SM

SHASTA JTAG PULL DOWN

JTAG_SB_TRST_L (25)
THESE PINS HAVE INTERNAL PULLUPS
TP_JTAG_SB_TCK MAKE_BASE=TRUE ALIAS → JTAG_SB_TCK (25)
TP_JTAG_SB_TDI MAKE_BASE=TRUE ALIAS → JTAG_SB_TDI (25)
TP_JTAG_SB_TDO MAKE_BASE=TRUE ALIAS → JTAG_SB_TDO (25)
TP_JTAG_SB_TMS MAKE_BASE=TRUE ALIAS → JTAG_SB_TMS (25)
R825 10K 5% 1/16W MF 402

DEVELOPMENT J800 U.FL-R-SMT

F-ST-SM
NB_PMR_OBSV (24) — 518S0104

SMU ANALOG VREF

PP3V3_ALL_SMU_AVCC (13)
NOSTUFF R818 200 1% 1/16W MF 402
PPVREF_SMU MAKE_BASE=TRUE — =PPVREF_SMU (13)
NOSTUFF C801 2.2UF 20% 10V CERM 805
NOSTUFF VR801 2.5V SOT23
R802 0 5% 1/16W MF 402 — PPVREF_SMU_ADC_REF (36)
NOSTUFF C802 0.47UF 20% 10V CERM 603
GND_SMU_AVSS (13 33 36)
NOSTUFF R828 0 5% 1/16W MF 402 — GND_SMU_AVSS_DAGND (36)

POWER_FAIL_L CONNECTION

POWER_GOOD (7)
PP3V3_ALL
NOSTUFF R813 430, NOSTUFF R812 10K (5% 1/16W MF 402)
SYS_POWERFAIL_L (6 13)
R860 4.7K 5% 1/16W MF 402
POWER_GOOD IS A 5V DRIVEN SIGNAL FROM POWER SUPPLY
2K PULLUP INSIDE P/S

AIRPORT CARDGUIDE SMT NUTS

SDF890 STDOFF-6MMOD1MMH-TH
SDF891 STDOFF-6MMOD1MMH-TH

CPU HEATSINK SMT NUTS

NOSTUFF SDF800 HSK-NUT-6.5MM TH — HS_SDF800 — C880 0.01UF 20% 16V CERM 402
NOSTUFF SDF801 HSK-NUT-6.5MM TH — HS_SDF801 — C881 0.01UF 20% 16V CERM 402
NOSTUFF SDF802 HSK-NUT-6.5MM TH — HS_SDF802 — C882 0.01UF 20% 16V CERM 402
NOSTUFF SDF803 HSK-NUT-6.5MM TH — HS_SDF803 — C883 0.01UF 20% 16V CERM 402
QMIT ZH804 6P15R5P4 — HS_SDF804 — C884 0.01UF 20% 16V CERM 402

SDF700 IS ALSO USED FOR HEATSINK MOUNTING

SIGNAL ALIAS

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2.5V VOLTAGE REGULATOR

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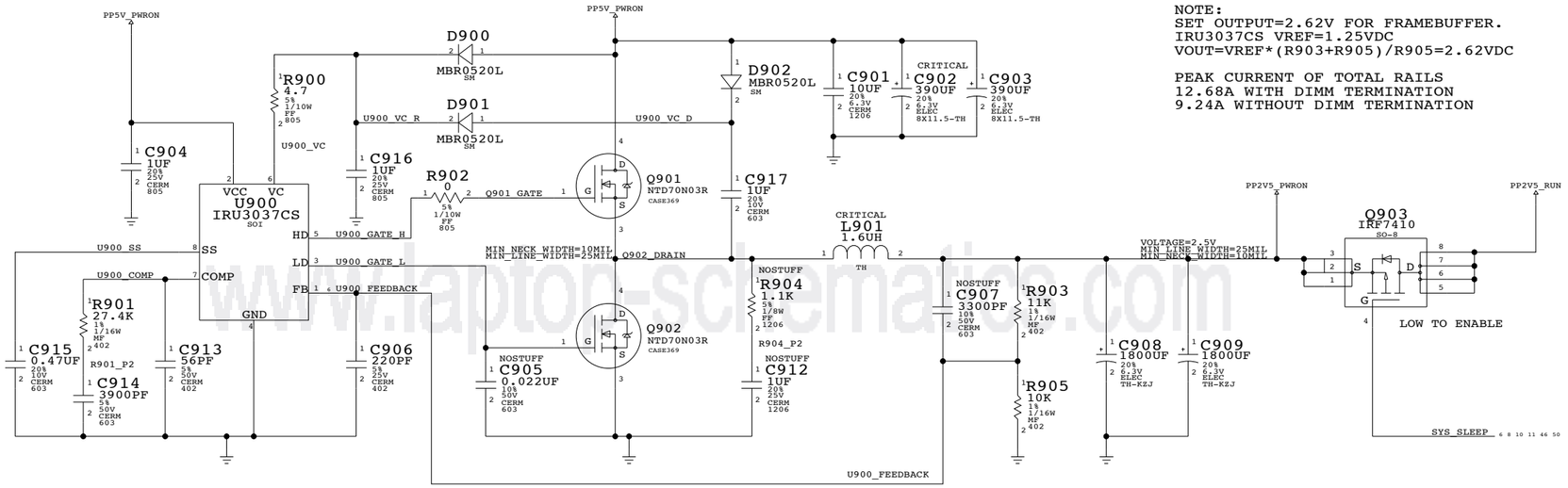

NOTE:
SET OUTPUT=2.62V FOR FRAMEBUFFER.
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R903+R905)/R905=2.62VDC

PEAK CURRENT OF TOTAL RAILS
12.68A WITH DIMM TERMINATION
9.24A WITHOUT DIMM TERMINATION

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2.5V VREG

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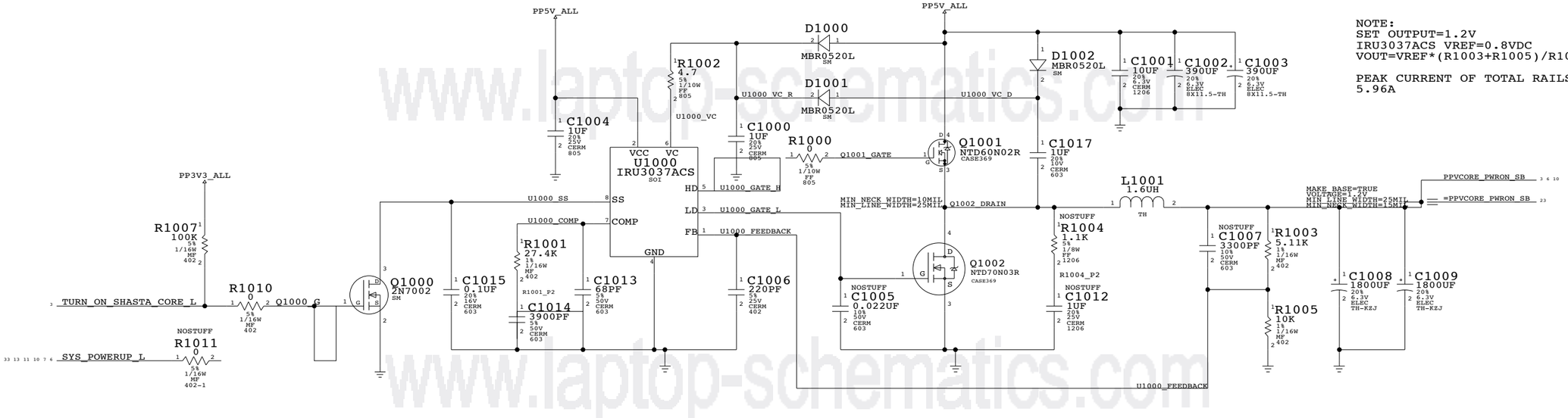
SHASTA CORE VOLTAGE REGULATOR

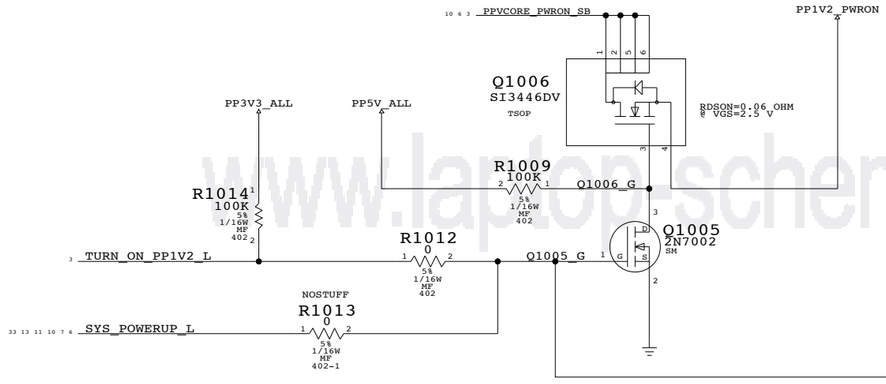


NOTE:
SET OUTPUT=1.2V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.206VDC

PEAK CURRENT OF TOTAL RAILS
5.96A

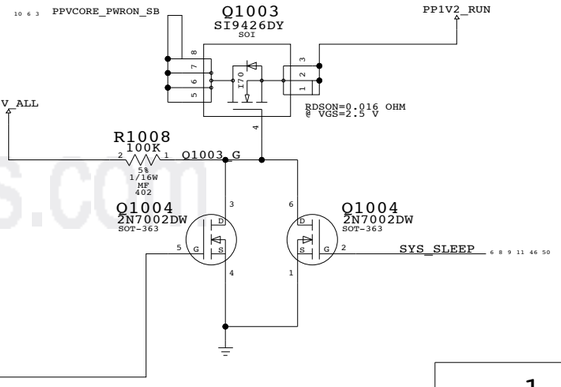
PP1V2_PWRON FET SWITCH

PEAK CURRENT 0.6A



PP1V2_RUN FET SWITCH

PEAK CURRENT 4.43A



1.2V VREG

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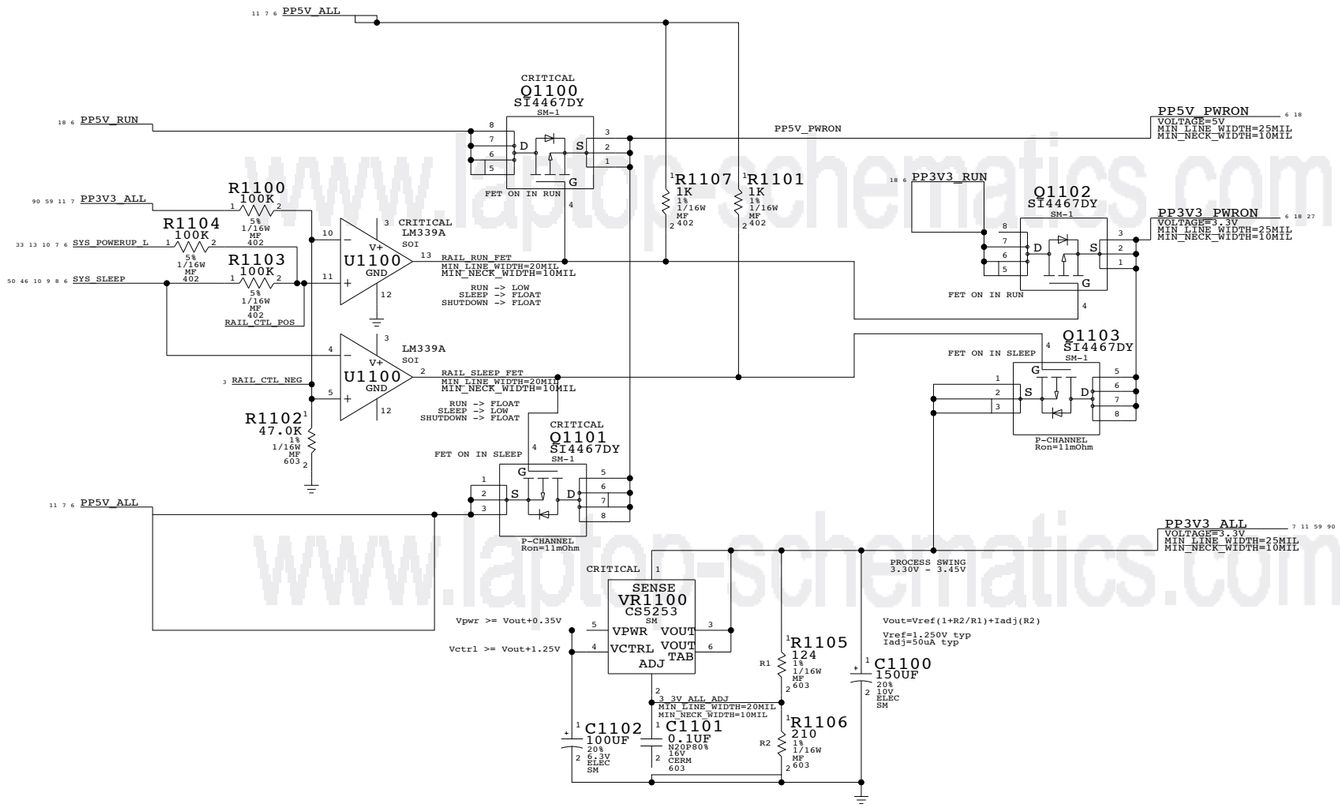

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5V & 3.3V VREGS

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	15 MIL SPACING		SMU_CLK10M_XIN
	15 MIL SPACING		SMU_CLK10M_XOUT
	15 MIL SPACING		SMU_CLK10M_XOUT_R
RTC_CLK32K_XTAL	15 MIL SPACING		RTC_CLK32K_X1
	15 MIL SPACING		RTC_CLK32K_X2

Page Notes

Power aliases required by this page:
- _PP3V3_ALL_SMU
- _PP3V3_ALL_RTC
- _PP3V3_PWRON_SMU
- _PPVREF_SMU (SMU AVCC or 2.5V reference)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

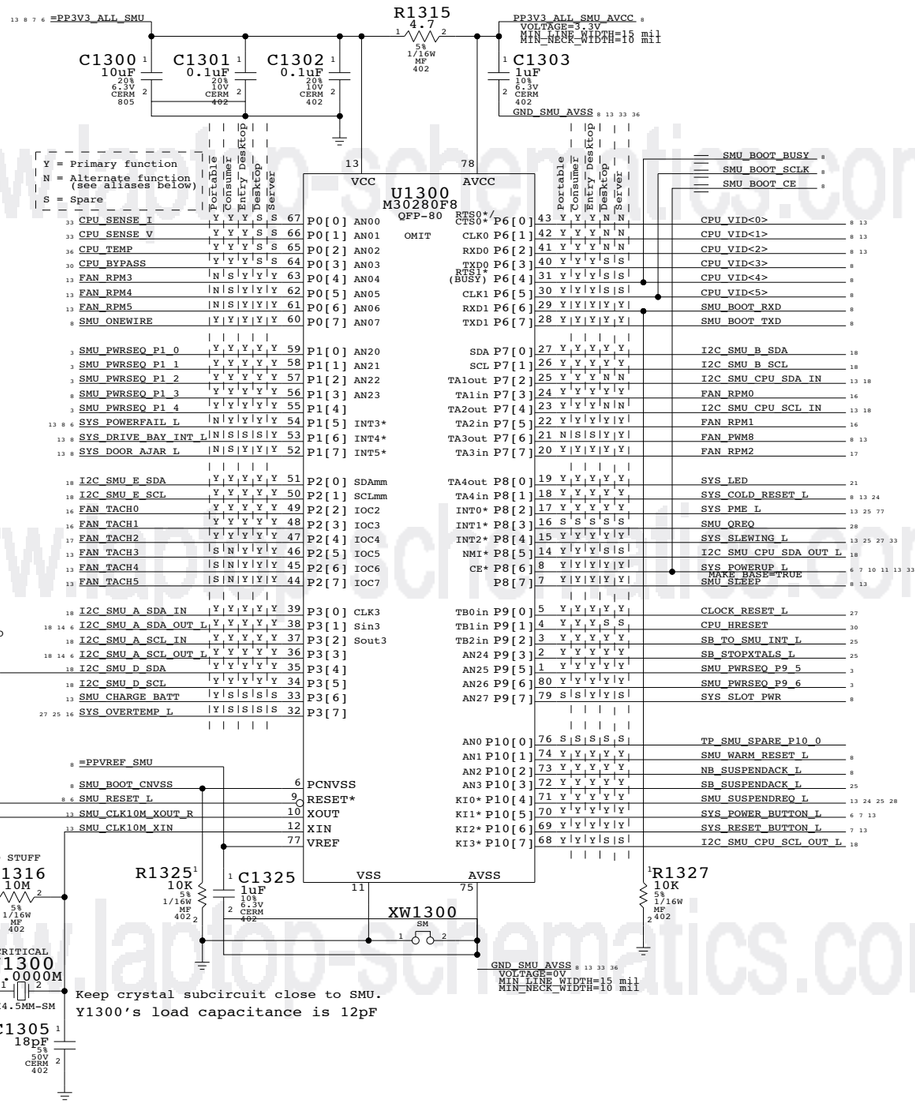
NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

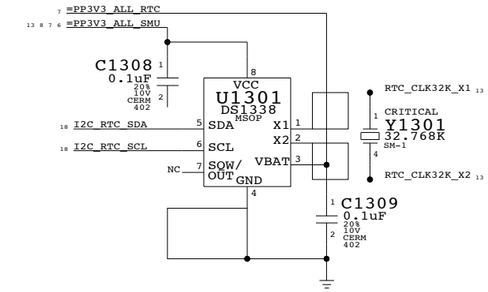
NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

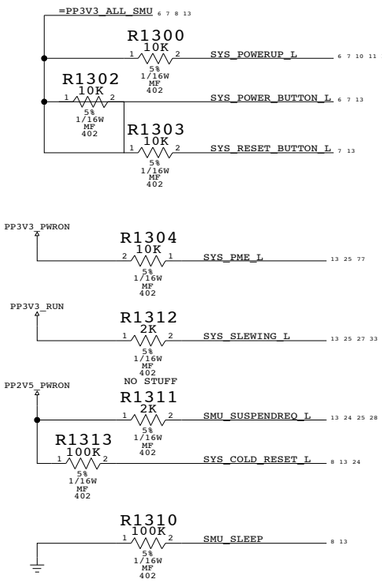
System Management Unit



Real Time Clock



SMU Pull-ups / pull-down



Alternate Functions

Portable

	Port		
FAN_RPM3	0.4		ALS0_OUT
FAN_RPM4	0.5		ALS1_OUT
FAN_RPM5	0.6		ALS_GAIN_BOOST
SYS_POWERFAIL_L	1.5		SMU_ACIN
SYS_DRIVE_BAY_INT_L	1.6		SMU_BATT_DET_L
SYS_DOOR_AJAR_L	1.7		SYS_LID_OPEN
FAN_PWM8	7.6		SYS_KBDLED

Consumer

	Port		
FAN_TACH3	2.5		SYS_LED_RED
FAN_TACH4	2.6		SYS_LED_GREEN
FAN_TACH5	2.7		SYS_LED_BLUE
SMU_CHARGE_BATT	3.6		DIAG_LED

Tower & Server

	Port		
CPU_VID<0>	6.0		FAN_TACH6
CPU_VID<1>	6.1		FAN_TACH7
CPU_VID<2>	6.2		FAN_TACH8
I2C_SMU_CPU_SDA_IN	7.2		FAN_PWM6
I2C_SMU_CPU_SCL_IN	7.4		FAN_PWM7

Master: Link

System Management Unit

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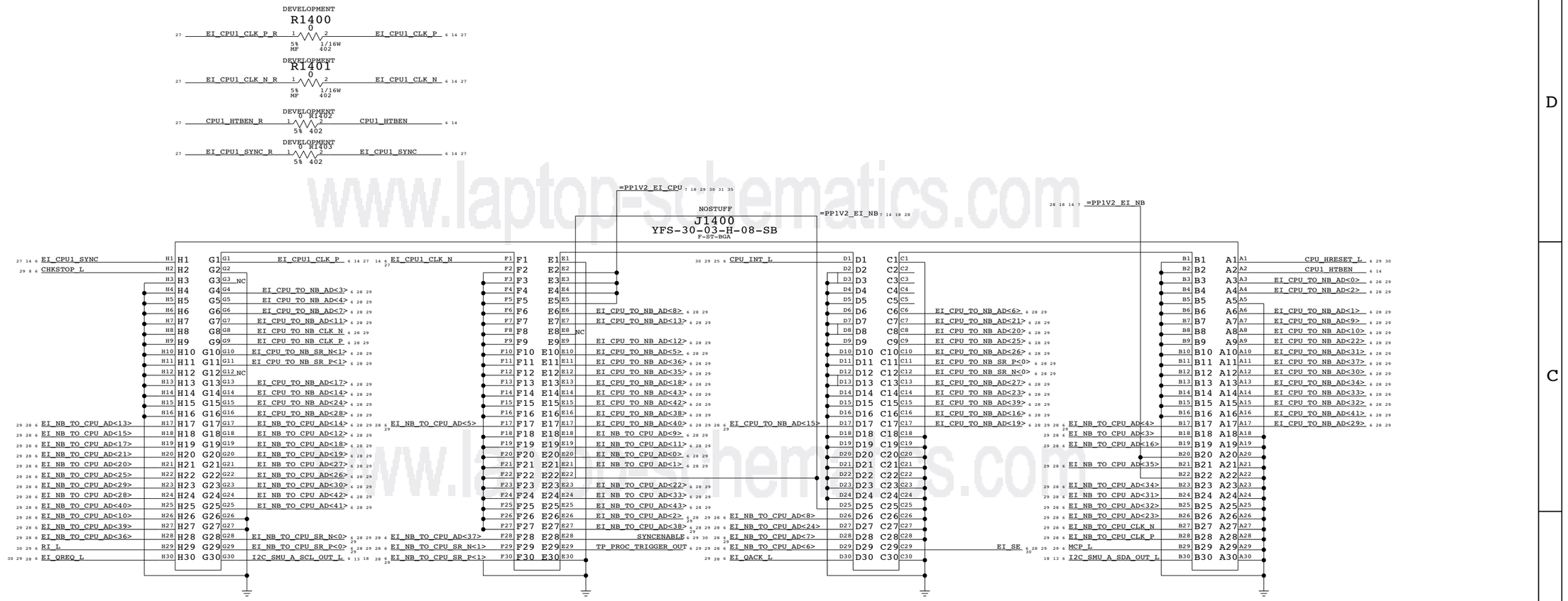

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CPU LOGIC ANALYZER

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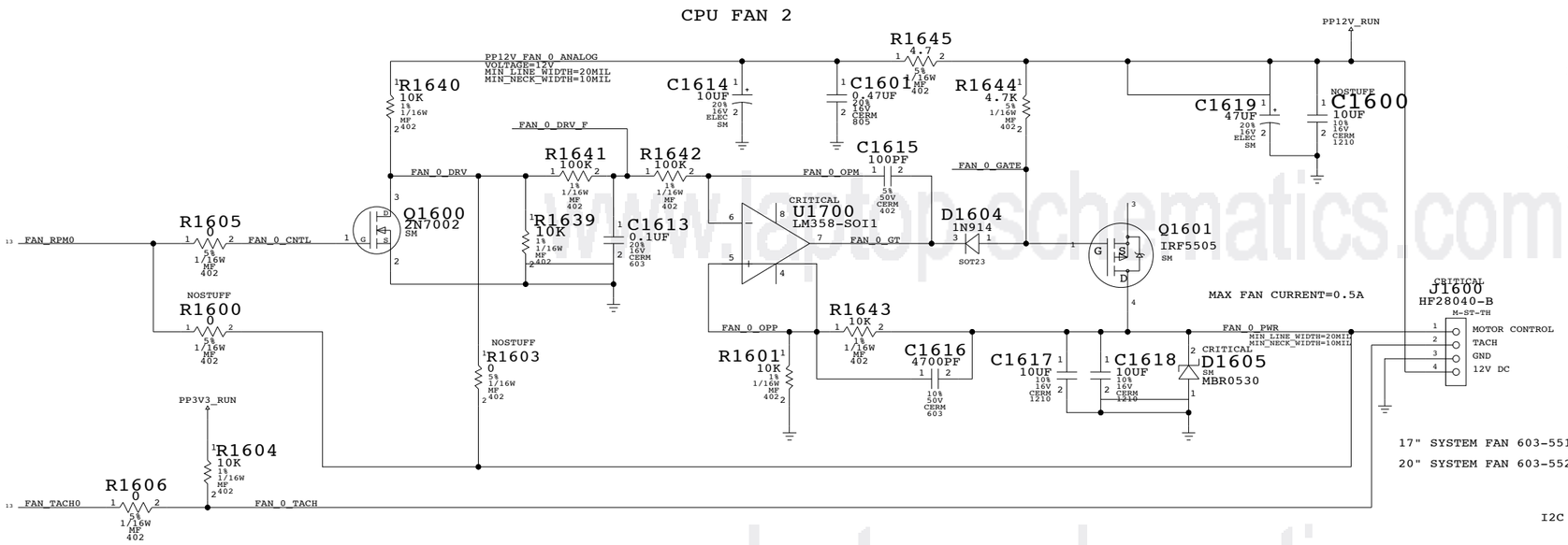
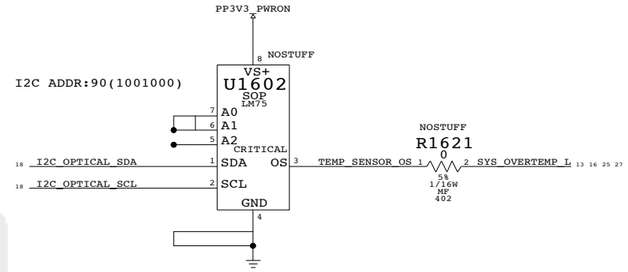
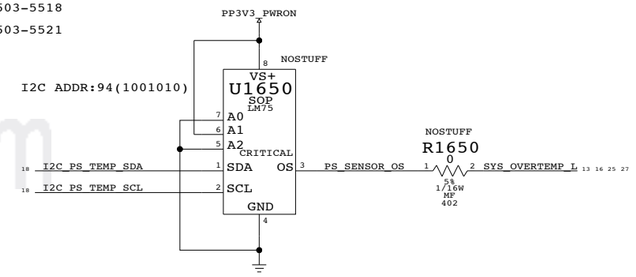
FAN 1 - Q37 STYLE CPU FAN CONTROL CIRCUIT



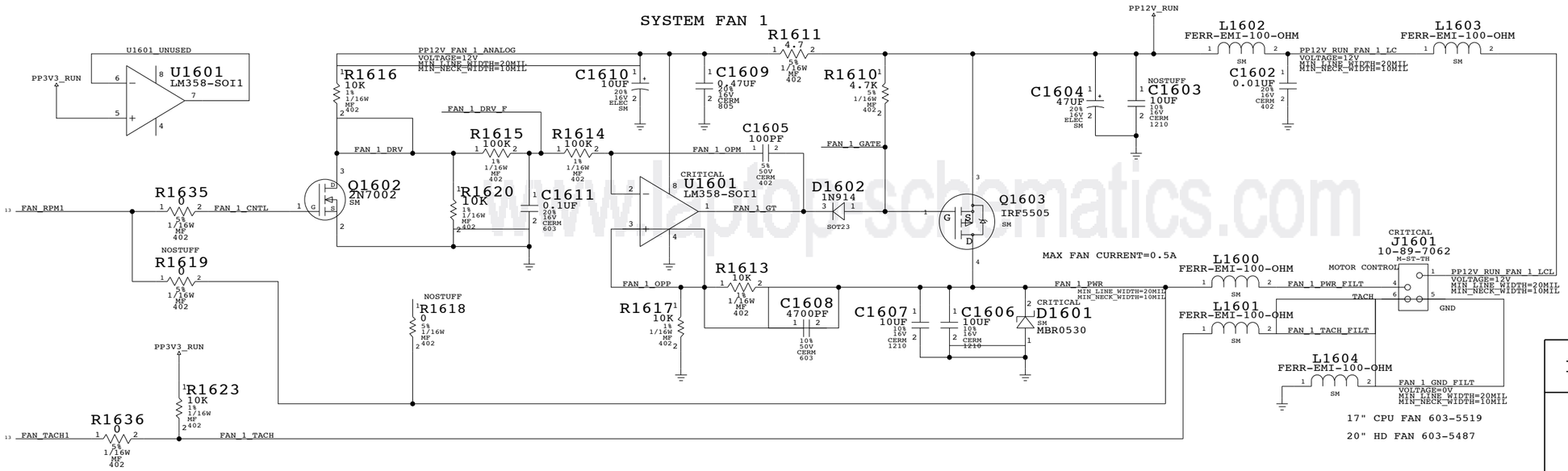
OPTICAL TEMP SENSOR



POWER SUPPLY TEMP SENSOR



FAN 2 - Q37 STYLE CPU FAN CONTROL CIRCUIT



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FAN 1, 2 & SYSTEM TEMP

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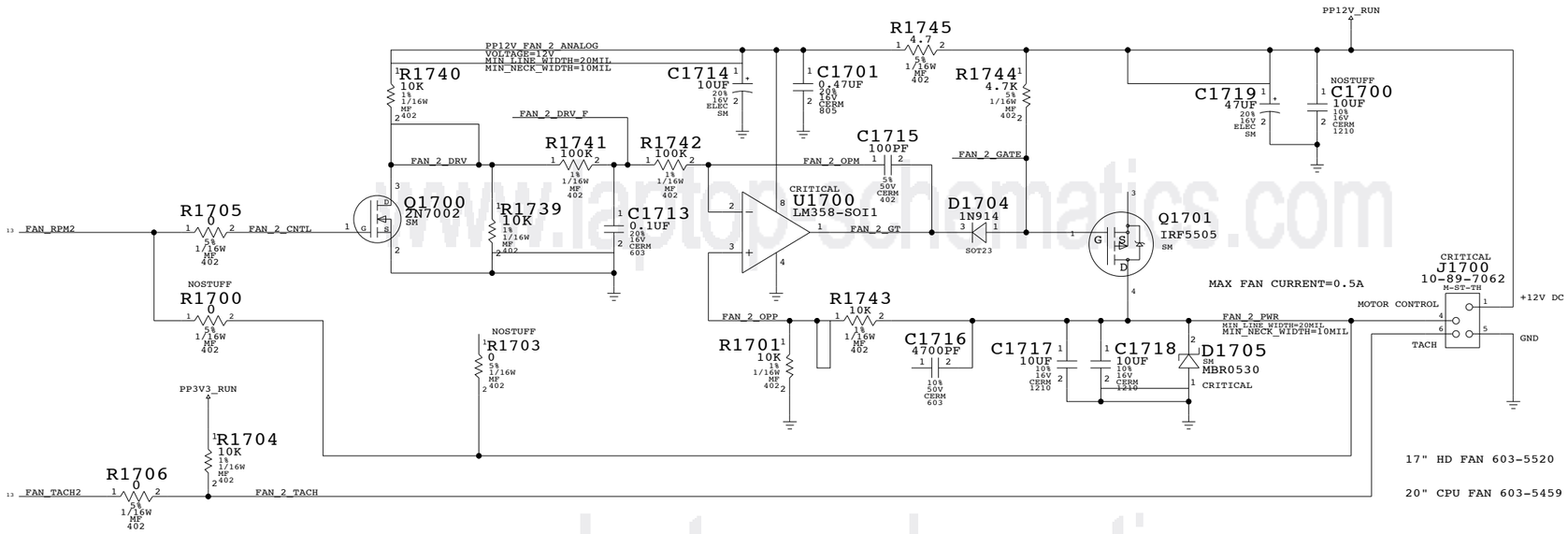
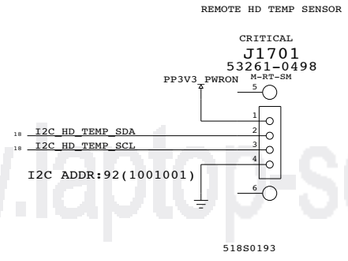
FAN 3 - Q37 STYLE SYSTEM FAN CONTROL CIRCUIT



REMOTE HARD DRIVE TEMP SENSOR



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FAN 3 & HD TEMP

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I2C A BUS

SMU
MASTER
U1300
I2C_SMU_A_SDA_IN — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
I2C_SMU_A_SDA_OUT_L — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
I2C_SMU_A_SCL_IN — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
I2C_SMU_A_SCL_OUT_L — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 36-39

PP5V_PWRON — R1832 0 603 NOSTUFF
PP5V_RUN — R1833 0 603
PP5V_U1800 — MIN_LINE_WIDTH=12MIL, MIN_NECK_WIDTH=8MIL
PP3V3_RUN — R1830 2K 5% 1/16W MF 402 NOSTUFF — R1831 2K 5% 1/16W MF 402 NOSTUFF
PP3V3_PWRON — R1800 2K 5% 1/16W MF 402 — R1801 2K 5% 1/16W MF 402
C1800 0.1UF 20% 10V CERM 402
R1809 4.7K 5% 1/16W MF 402 NOSTUFF — R1828 4.7K 5% 1/16W MF 402 — C1802 0.1UF 20% 10V CERM 402
R1808 200 5% 1/16W MF 402 — R1810 200 5% 1/16W MF 402
=PP1V2_EI_NB

U1800 LM339A SOI — V+ GND
Q1800 2N7002DW SOT-363

U3LITE
U3
I2C_NB_A_SDA — 24
I2C_NB_A_SCL — 24
PINS A20, B20

R1820 0 5% 1/16W MF 402 NOSTUFF — R1821 0 5% 1/16W MF 402 NOSTUFF

PP3V3_PWRON — R1819 2K 5% 1/16W MF 402 — R1818 2K 5% 1/16W MF 402

=PP1V2_EI_CPU
R1816 200 5% 1/16W MF 402 — R1817 200 5% 1/16W MF 402

CPU
U2900
I2C_CPU_A_SCL — 29
I2C_CPU_A_SDA — 29
PINS AA20, Y21

SMU
MASTER
U1300
I2C_SMU_CPU_SCL_IN — MAKE_BASE=TRUE — I2C
I2C_SMU_CPU_SCL_OUT_L — MAKE_BASE=TRUE — I2C
I2C_SMU_CPU_SDA_IN — MAKE_BASE=TRUE — I2C
I2C_SMU_CPU_SDA_OUT_L — MAKE_BASE=TRUE — I2C
PINS 14,25,23,68

RP1800 0K 5% 1/16W SM1
SMU_CPU_JTAG_OR_I2C
I2C_CPU_A_SCL — NET_SPACING_TYPE=I2C
I2C_CPU_A_SDA_TO_SMU — NET_SPACING_TYPE=I2C
I2C_CPU_A_SDA_TO_CPU

Q1801 2N7002DW SOT-363
I2C_CPU_SCL_LS

RP1801 0K 5% 1/16W SM1 NOSTUFF
CPU JTAG
JTAG_CPU_TDO — 29 30
JTAG_CPU_TDI — 29 30
JTAG_CPU_TMS — 29 30
JTAG_CPU_TCK — 29 30

I2C_0V6_REF
C1801 0.1UF 20% 10V CERM 402
R1811 4.7K 5% 1/16W MF 402
USE 576 OHM FOR R1811 IF 5V RAIL IS USED FOR REFERENCE

I2C B BUS

PP3V3_PWRON — R1803 2K 5% 1/16W MF 402 — R1802 2K 5% 1/16W MF 402

SMU
MASTER
U1300
I2C_SMU_B_SDA — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
I2C_SMU_B_SCL — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 26, 27

PULSAR
U2600
I2C_CLOCK_SDA — ALIAS
I2C_CLOCK_SCL — ALIAS
PINS C1, B1

OPTICAL TEMP SENSOR
U1602
I2C_OPTICAL_SDA — ALIAS
I2C_OPTICAL_SCL — ALIAS
PINS 1, 2
I2C ADDR:90

PS TEMP SENSOR
U1650
I2C_PS_TEMP_SDA — ALIAS
I2C_PS_TEMP_SCL — ALIAS
PINS 1, 2
I2C ADDR:94

HD TEMP SENSOR
U1702
I2C_HD_TEMP_SDA — ALIAS
I2C_HD_TEMP_SCL — ALIAS
PINS 1, 2
I2C ADDR:92

I2C C BUS

PP2V5_PWRON — R1805 2K 5% 1/16W MF 402 — R1804 2K 5% 1/16W MF 402
NET_SPACING_TYPE=I2C
NET_SPACING_TYPE=I2C

U3LITE
MASTER
U3
I2C_NB_C_SDA — MAKE_BASE=TRUE — 24
I2C_NB_C_SCL — MAKE_BASE=TRUE — 24
PINS C21, E21

DIMMS
J4000 = A0
J4001 = A2
ALIAS — I2C_DIMM_SDA — 40
ALIAS — I2C_DIMM_SCL — 40
PINS 91, 92
OF EACH DIMM

I2C D & E BUS

PP2V5_PWRON — R1812 2K 5% 1/16W MF 402 — R1813 2K 5% 1/16W MF 402
PP3V3_ALL — R1807 2K 5% 1/16W MF 402 — R1806 2K 5% 1/16W MF 402

U3LITE 'B'
U3
I2C_NB_B_SDA — I2C
I2C_NB_B_SCL — I2C
PINS C20, B21

RTC
U1301
I2C_RTC_SDA — I2C
I2C_RTC_SCL — I2C
PINS 5, 6

R1822 0 5% 1/16W MF 402 NOSTUFF — R1823 0 5% 1/16W MF 402 NOSTUFF

R1824 0 5% 1/16W MF 402
R1826 0 5% 1/16W MF 402 NOSTUFF
R1825 0 5% 1/16W MF 402
R1827 0 5% 1/16W MF 402 NOSTUFF

SMU 'E'
MASTER
U1300
I2C_SMU_E_SDA — I2C
I2C_SMU_E_SCL — I2C
PINS 50, 51

SMU 'D'
MASTER
U1300
I2C_SMU_D_SDA — I2C — 13
I2C_SMU_D_SCL — I2C — 13
PINS 34, 35

I2C SB BUS

PP3V3_RUN — R1815 1K 5% 1/16W MF 402 — R1814 1K 5% 1/16W MF 402

SHASTA
MASTER
U2300
I2C_SB_SDA — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
I2C_SB_SCL — MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS Y9, AB7

MICRODASH
J9400
I2C_UDASH_SDA — ALIAS
I2C_UDASH_SCL — ALIAS
PINS 21, 24

AUDIO
U9500 / AU300
I2C_AUDIO_SDA — ALIAS
I2C_AUDIO_SCL — ALIAS
PINS 18, 19

STANDARD CONFIGURATION: SMU IS MASTER OF BUS E WITH RTC AS SLAVE; U3LITE 'B' AND SMU 'D' ARE NOT USED
TO IMPROVE LATENCY WITH RGB LED - U3LITE 'B' AND SMU 'E' CAN MAKE AN I2C 'E' BUS
SMU 'D' AND RTC CAN MAKE AN I2C 'D' BUS

I2C CONNECTIONS

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TOTAL CURRENT EXCLUDING LEDS CURRENT < 170 MICRO AMPS

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_GREEN
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2101 0 5% 1/16W MF 402
G_PWM_IN_H
R2109 953K 1% 1/16W MF 402
PP5V_PWRON
U2100 LP324 TSSOP
G_BASE_DRV
G_PWM_DC
R2104 953K 1% 1/16W MF 402
C2104 0.022UF 20% 16V CERM 402
C2106 0.47UF 20% 10V CERM 603
R2105 200K 1% 1/16W MF 402
R2112 1K 1% 1/16W MF 402
G_IN_OFFSET
5MV INPUT OFFSET

100% DUTY CYCLE OF 3V-PP PWM = 0.5V

C2105 220PF 5% 25V CERM 402
GND_CHASSIS_LED
G_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2100 400-OHM-EMI SM-1
G_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2102 2N3904 SM
G_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2100 25.5 1% 1/16W MF 402 <-- 17 INCH

CHANGE R2100 VALUE TO SET LED CURRENT
MAX LED CURRENT = 0.5 / R

LED2100 LATBG66B AMB-GRN-BLUE PLCC
AMB
GRN
BLUE
RGB_LED_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2104 400-OHM-EMI SM-1
PP5V_PWRON
C2107 220PF 5% 25V CERM 402
C2108 220PF 5% 25V CERM 402
GND_CHASSIS_LED
C2109 220PF 5% 25V CERM 402

PP3V3_PWRON
PP5V_PWRON
C2103 0.1UF 20% 10V CERM 402
U2100 LP324 TSSOP
U2100_UNUSED

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_RED
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2115 0 5% 1/16W MF 402
R_PWM_IN_H
R2102 953K 1% 1/16W MF 402
PP5V_PWRON
U2100 LP324 TSSOP
R_BASE_DRV
R_PWM_DC
R2110 953K 1% 1/16W MF 402
C2101 0.022UF 20% 16V CERM 402
C2112 0.47UF 20% 10V CERM 603
R2111 200K 1% 1/16W MF 402
R2114 1K 1% 1/16W MF 402
R_IN_OFFSET

R_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2101 400-OHM-EMI SM-1
R_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2108 2N3904 SM
R_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2113 25.5 1% 1/16W MF 402 <-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

SYS_LED_BLUE
MAKE_BASE=TRUE
PWM INPUT FROM SMU

R2130 0 5% 1/16W MF 402
B_PWM_IN_H
R2118 953K 1% 1/16W MF 402
PP5V_PWRON
U2100 LP324 TSSOP
B_BASE_DRV
B_PWM_DC
R2116 953K 1% 1/16W MF 402
C2102 0.022UF 20% 16V CERM 402
C2118 0.47UF 20% 10V CERM 603
R2117 200K 1% 1/16W MF 402
R2127 1K 1% 1/16W MF 402
B_IN_OFFSET

B_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L2102 400-OHM-EMI SM-1
B_DRV MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
Q2114 2N3904 SM
B_DRV_FB MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R2126 25.5 1% 1/16W MF 402 <-- 17 INCH

PLACE THESE PARTS CLOSE TO SMU IC

NOSTUFF
Q2100 FDV302P SOT-23
PP3V3_PWRON
SYS_LED_H
WHITE_LED
R2106 1K 5% 1/16W MF 402
SYS_GATE
NOSTUFF
R2119 953K 1% 1/16W MF 402
WHITE_LED
R2129 4.7K 5% 1/16W MF 402
NOSTUFF
R2132 1K 5% 1/16W MF 402
SYS_LED
PWM INPUT FROM SMU
SYS_LED_IN
WHITE_LED
R2107 0 5% 1/16W MF 402

(STUFF WHEN SYS_LED_L = ACTIVE HIGH)
(AND NO STUFF R2132, R2119 & Q2100)

LED2101
WHITE SM6
SYS_DRV_A MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
PP5V_PWRON
WHITE_LED L2105 400-OHM-EMI SM-1
WHITE_LED C2111 220PF 5% 25V CERM 402
WHITE_LED C2110 220PF 5% 25V CERM 402
GND_CHASSIS_LED
WHITE_LED L2103 400-OHM-EMI SM-1
SYS_LED_DRV_K MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
17_INCH_LCD
R2103 56.2 1% 1/16W MF 402
SYS_LED_DRV_C MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
WHITE_LED Q2101 FDV301N SM

20 INCH -->

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S3921	1	RES, 39.2 OHM, 1%, 402	R2103	20_INCH_LCD
114S1821	3	RES, 18.2 OHM, 1%, 402	R2100,R2113,R2126	NOSTUFF

INDICATOR LED

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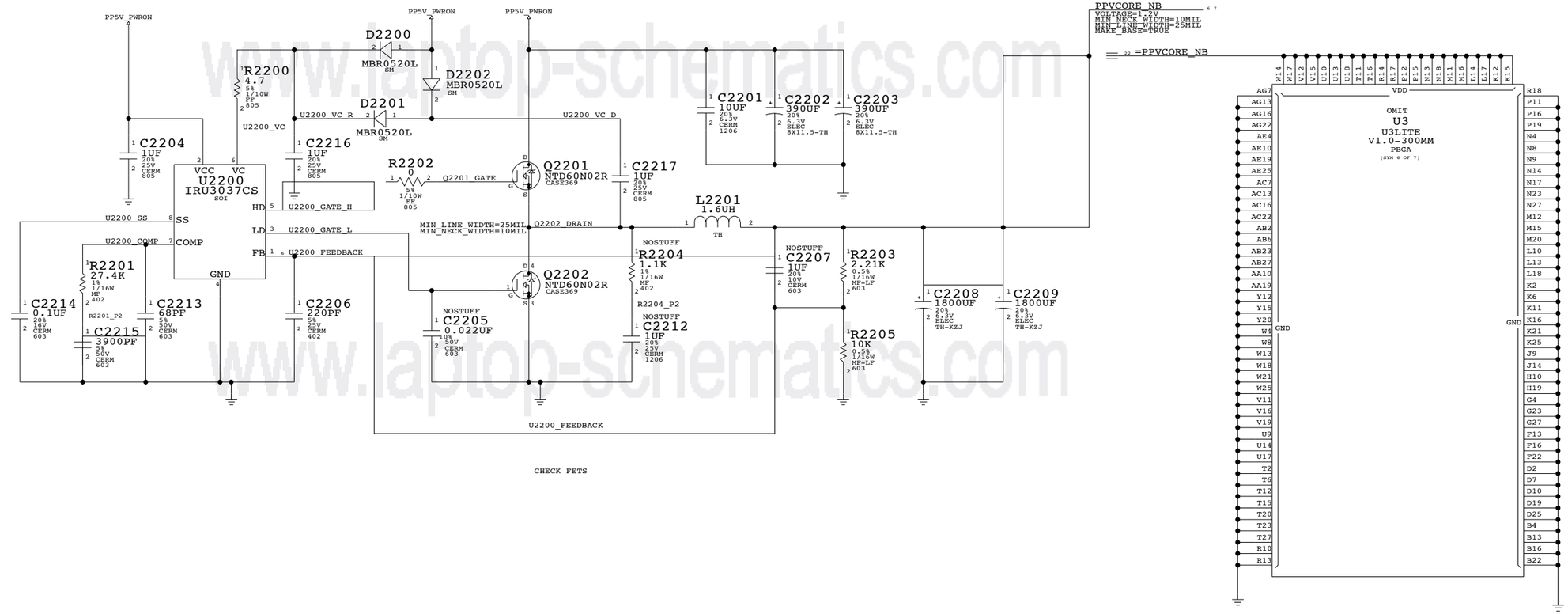
NOTE:
SET OUTPUT=1.5VDC FOR U3LITE CORE
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R2203+R2205)/R2205=1.53VDC

7.73A OF PEAK CURRENT DRAW ON PCORE_NB



CHECK FETS

=PPVCORE_NB

C2222 0.1UF 20% 10V CERM 402
C2223 0.1UF 20% 10V CERM 402
C2225 0.1UF 20% 10V CERM 402
C2227 0.1UF 20% 10V CERM 402
C2228 0.1UF 20% 10V CERM 402
C2229 0.1UF 20% 10V CERM 402
C2230 0.1UF 20% 10V CERM 402
C2231 0.1UF 20% 10V CERM 402
C2232 0.1UF 20% 10V CERM 402
C2233 0.1UF 20% 10V CERM 402
C2234 0.1UF 20% 10V CERM 402
C2235 0.1UF 20% 10V CERM 402
C2236 0.1UF 20% 10V CERM 402
C2237 0.1UF 20% 10V CERM 402
C2238 0.1UF 20% 10V CERM 402
C2239 0.1UF 20% 10V CERM 402
C2240 0.1UF 20% 10V CERM 402
C2242 0.1UF 20% 10V CERM 402
C2243 0.1UF 20% 10V CERM 402
C2244 0.1UF 20% 10V CERM 402
C2245 0.1UF 20% 10V CERM 402
C2246 0.1UF 20% 10V CERM 402
C2247 0.1UF 20% 10V CERM 402

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U3LITE CORE POWER

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Page Notes

Power aliases required by this page:
- _PPPCI64_PWRON_SB (to 5V or 3.3V)
- _PPPCI32_PWRON_SB (to 5V or 3.3V)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PPVCORE_PWRON_SB (1.2V)

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. Connect _PPPCI32_PWRON_SB to appropriate PCI bus voltage and _PPPCI64_PWRON_SB to same if 64-bit PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

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10 =PPVCORE_PWRON_SB

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

74 25 7 =PP3V3_PWRON_SB

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.0
BGA
(1 OF 8)

POWER

OMIT

VDDC: H15 H8 J12 J15 K8 L15 L8 M15 N8 P15 R10 R12 R9 T10 T15

VDDO33: AA1 AA2 AA3 AB10 AB2 AB6 B1 B2 B5 D1 F4 F8 H1 L7 M1 R2 U12 U9 V7 W4

GND: A1 A2 A22 A5 AA10 AA6 AB1 AB22 C19 D2 E22 F3 F7 H2 H9 J10 J11 J13 J14 J16

GND: J22 K10 K11 K12 K13 K7 K9 L10 L11 L12 L13 L14 L16 L9 M10 M11 M12 M13 M14

GND: W5 W19 U22 U13 U10 T12 R19 P9 P4 P14 P13 P12 P10 N9 N22 N13 N12 N11 N10 M2

VDDO25: D19 G15

VIO1: H18 H17 K21

VIO2: L21 W22 Y19

VDDP_KL: V8

Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA (1175 mW)
ANALOG12	1.2V	600 mA (760 mW)
VDDPs	2.5V	100 mA (250 mW)
I/O 2.5	2.5V	20 mA (60 mW)
I/O 3.3	3.3V	220 mA (770 mW)
Total:		3015 mW

=PP2V5_PWRON_SB 7 23 25 74 88

C2350 C2351 C2365
0.1uF 20% 10V CERM 402

=PPPCI64_PWRON_SB 7

C2355 C2356 C2357
0.1uF 20% 10V CERM 402

For PCI_AD<63..32>

=PPPCI32_PWRON_SB 7

C2360 C2361 C2362
0.1uF 20% 10V CERM 402

For PCI_AD<31..0>

=PP2V5_PWRON_SB 7 23 25 74 88

Master: Link

Shasta Core Power

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DRAWING

LAST_MODIFIED=Mon Dec 13 20:01:04 2004

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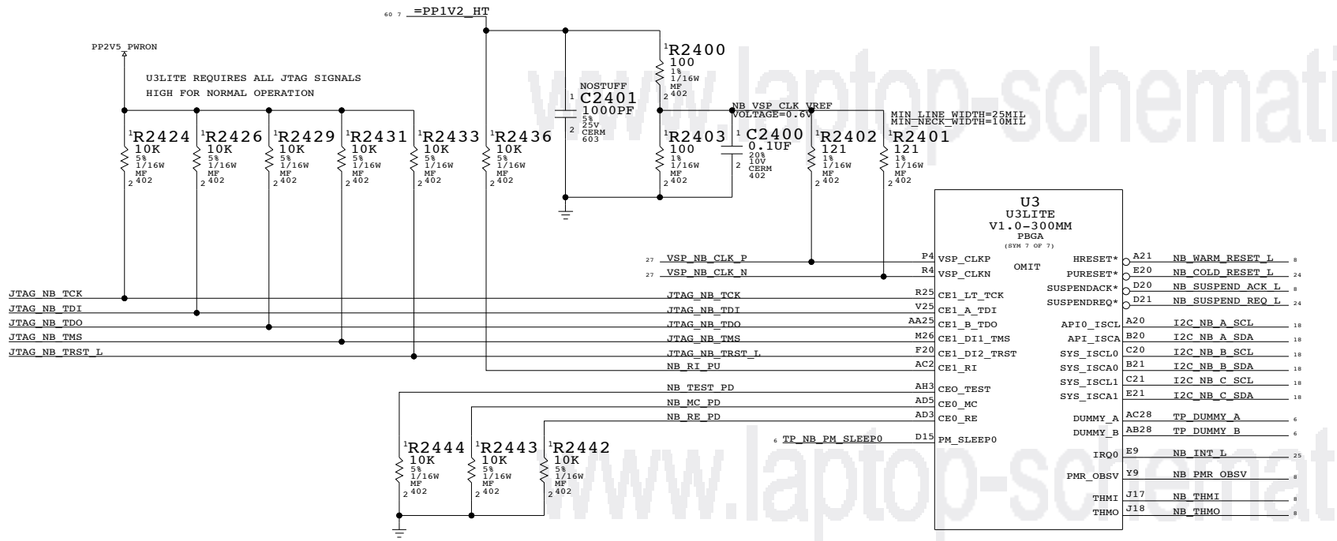

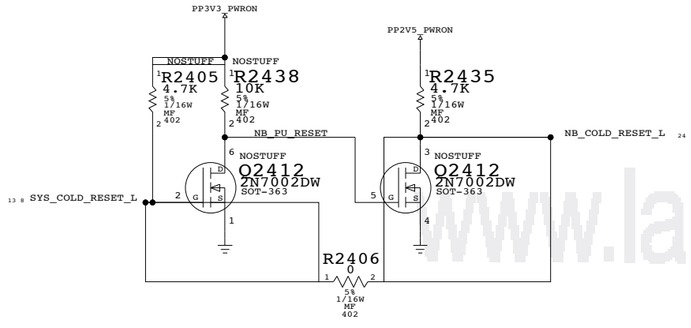

MASTER: GILA
LAST MODIFIED: JUNE 10, 04

U3LITE MISC

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
I2S0_TO_SB			I2S0_DEV_TO_SB_DTI	25 95
I2S0_TO_DEV			I2S0_SB_TO_DEV_DTO	25 95 103
I2S0_TO_DEV	AUDIO		I2S0_MCLK	25 102
I2S0_BIDIR			I2S0_BITCLK	25 102 103
I2S0_BIDIR			I2S0_SYNC	25 95 103
I2S1_TO_SB			I2S1_DEV_TO_SB_DTI	6 25 76 94
I2S1_TO_DEV			I2S1_SB_TO_DEV_DTO	6 25 76 94
I2S1_TO_DEV	10 MIL SPACING		I2S1_MCLK	6 25 76 94
I2S1_BIDIR			I2S1_BITCLK	6 25 94
I2S1_BIDIR			I2S1_SYNC	6 25 94
I2S2_TO_SB			I2S2_DEV_TO_SB_DTI	25 102
I2S2_TO_DEV			I2S2_SB_TO_DEV_DTO	25 102
I2S2_TO_DEV	10 MIL SPACING		I2S2_MCLK	25 102
I2S2_BIDIR			I2S2_BITCLK	25 102
I2S2_BIDIR			I2S2_SYNC	25 102
SB_CLK18M_XTAL	15 MIL SPACING		SB_CLK18M_XTALI	25
	15 MIL SPACING		SB_CLK18M_XTALO	25
	15 MIL SPACING		SB_CLK18M_XTALO_R	25
SB_CLK25M_ATA	15 MIL SPACING		SB_CLK25M_ATA	25 27

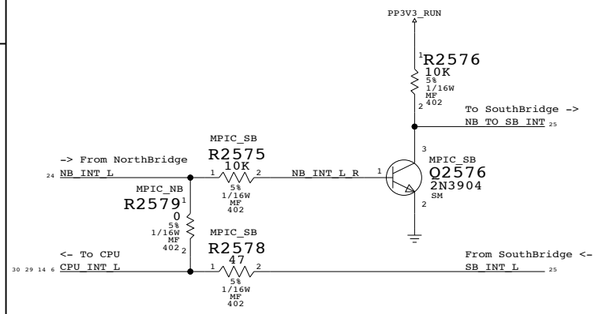
Page Notes

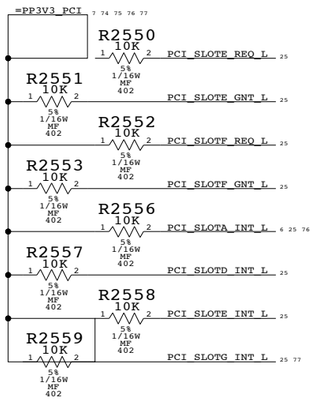
Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- PCI_64BIT
  Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB
  Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

NorthBridge / SouthBridge MPIC Routing



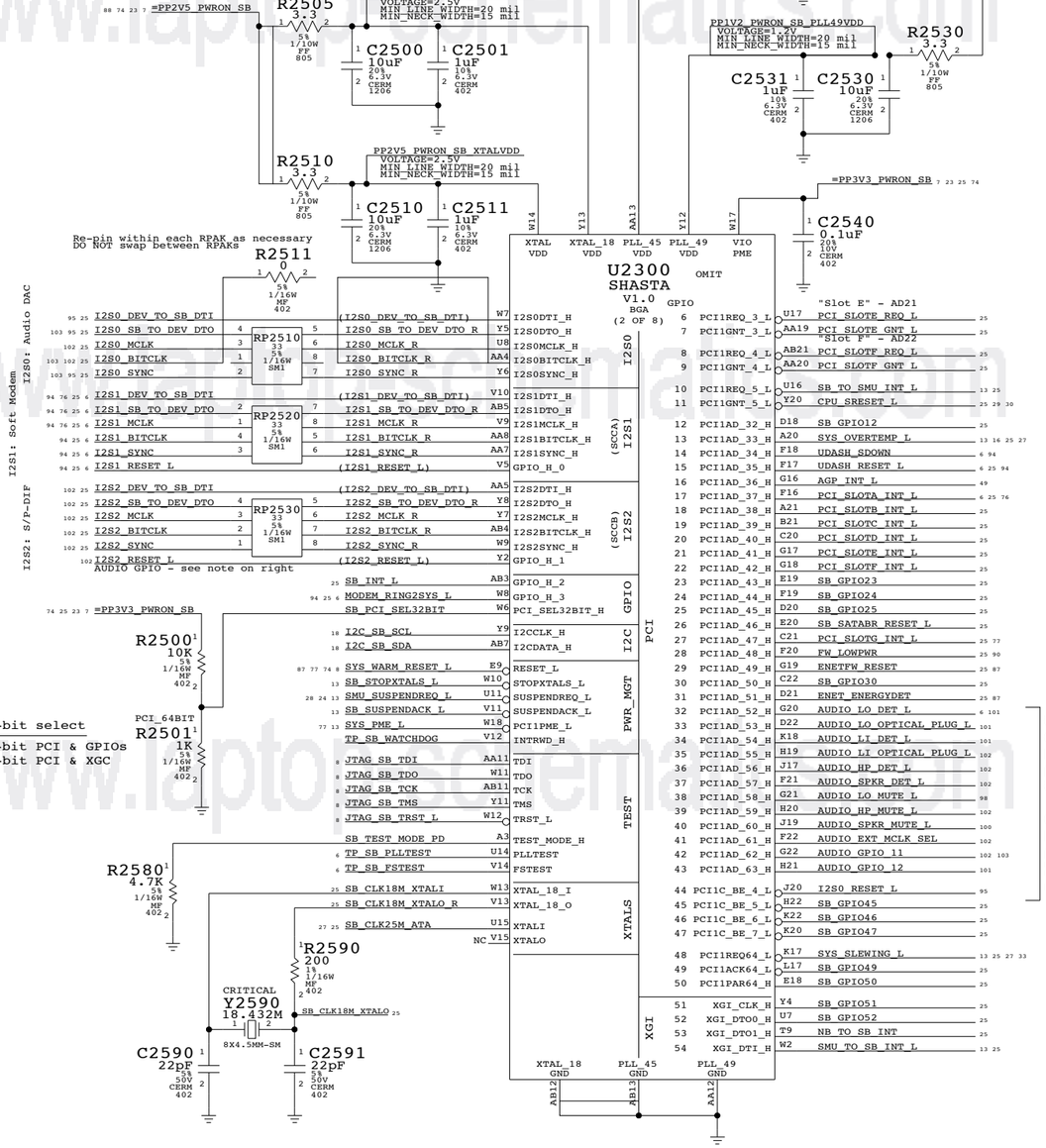


DRAWING

LAST_MODIFIED=Mon Dec 13 20:01:12 2004

PCI 32-bit select

1 = 32-bit PCI & GPIOs
0 = 64-bit PCI & XGC



Shasta Serial / Misc

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D	051-6482	I
SCALE: NONE	SHT 25 OF 103	

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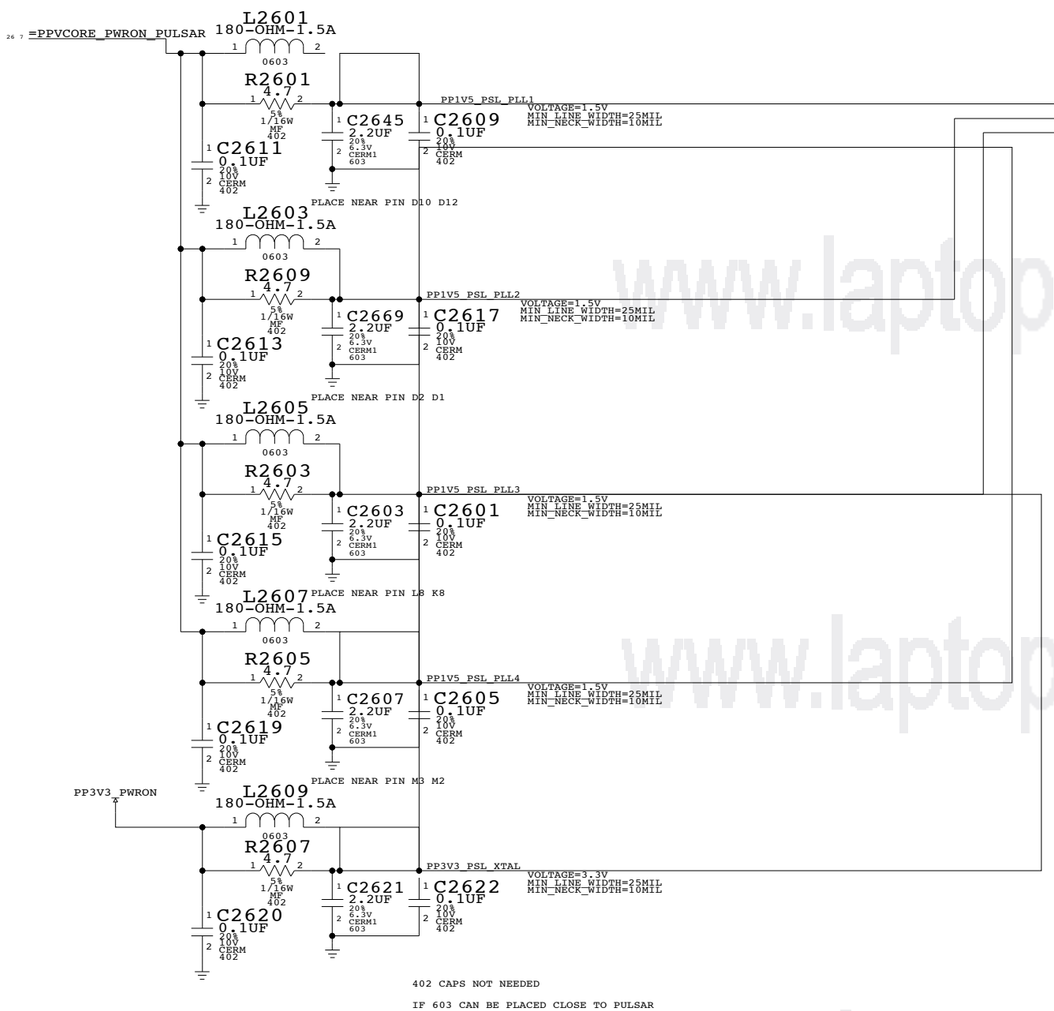
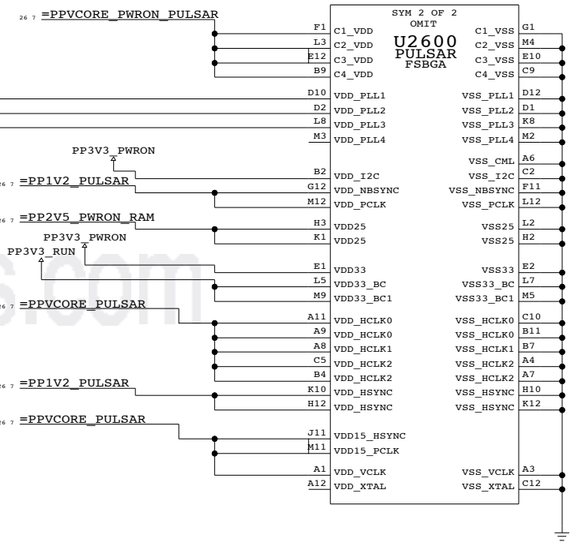
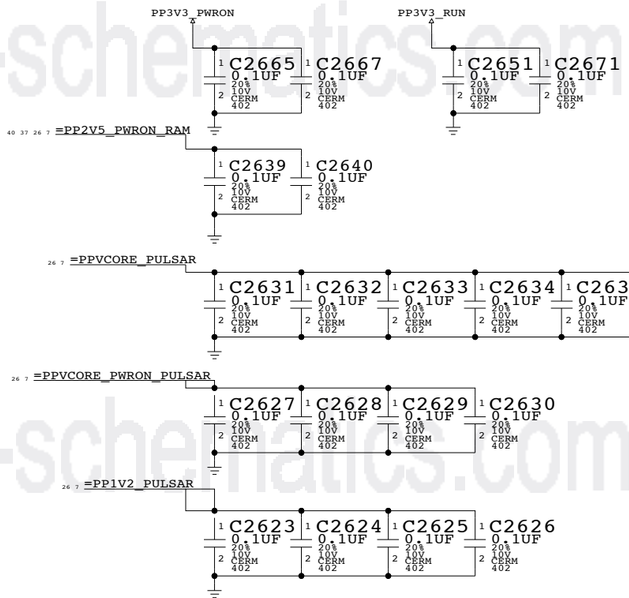




PINS G12, M12, H3, K1, L5, M9, A11, A9
A8, C5, B4, K10, H12 J11, M11, A1
CAN BE TURNED OFF IN SLEEP



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
359S0076	1	PULSAR, PBGA	U2600	

MASTER: GILA
LAST MODIFIED: APR 09, 04

PULSAR POWER

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ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_CLK_P	EI_CPU_CLK	CLOCKS	EI_CPU_CLK	116
EI_CPU_CLK_N	EI_CPU_CLK	CLOCKS	EI_CPU_CLK	117
EI_CPU1_CLK_P	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK	114
EI_CPU1_CLK_N	EI_CPU1_CLK	CLOCKS	EI_CPU1_CLK	115
EI_NB_CLK_P	EI_NB_CLK	CLOCKS	EI_NB_CLK	124
EI_NB_CLK_N	EI_NB_CLK	CLOCKS	EI_NB_CLK	125
EI_CPU_SYNC	EI_SYNC	CLOCKS		120
EI_NB_SYNC		CLOCKS		109
EI_CPU1_SYNC	EI_CPU1_SYNC	CLOCKS		118
VSP_NB_CLK_P	VSP_NB_CLK	CLOCKS	VSP_NB_CLK	134
VSP_NB_CLK_N	VSP_NB_CLK	CLOCKS	VSP_NB_CLK	135
AGP_CLK66M_NB	AGP_NB_CLK	CLOCKS		100
AGP_CLK66M_GPU	AGP_GPU_CLK	CLOCKS		101
HT_CLK66M_NB	HT_NB_CLK	CLOCKS		102
HT_CLK66M_SB	HT_SB_CLK	CLOCKS		103
PCI_CLK66M_SB_INT	CLOCKS_PCI	CLOCKS		106
PCI_CLK33M_SB_EXT	CLOCKS_PCI	CLOCKS		104
PLS_EXTCLK	PLS_XTAL	CLOCKS		119

DIFFERENTIAL SIGNALS SHOULD HAVE 5 MIL SPACING TO EACH OTHER
ALL SPACING GROUPS SHOULD HAVE 15 MIL SPACING TO SIGNALS NOT IN THEIR GROUP

EI_NB_SYNC IS PART OF EI_CPU_SYNC TOPOLOGY

NET SPACING TYPE

SYM 1 OF 2

OMIT
U2600
PULSAR
FSBGA

GPCLK33_0	L4	PCI_CLK_GP0_R	CLOCKS	
GPCLK33_1	K4	PCI_CLK_GP1_R	CLOCKS	
VCLKN	A2	VSP_NB_CLK_N_C	CLOCKS	
VCLKP	B3	VSP_NB_CLK_P_C	CLOCKS	
HCLKN_0	B10	EI_CPU_CLK_N_C	CLOCKS	
HCLKN_1	C8	EI_CPU1_CLK_N_R	CLOCKS	14
HCLKN_2	C4	EI_NB_CLK_N_C	CLOCKS	
HCLKP_0	A10	EI_CPU_CLK_P_C	CLOCKS	
HCLKP_1	B8	EI_CPU1_CLK_P_R	CLOCKS	14
HCLKP_2	B5	EI_NB_CLK_P_C	CLOCKS	
GPCLK25_0	J3	6 PLS_CLK_66M_0_R	CLOCKS	
GPCLK25_1	J1	6 PLS_CLK_66M_1_R	CLOCKS	
PCLK25_0	K2	HT_CLK66M_NB_R	CLOCKS	
PCLK25_1	L1	RAM_CLK66M_NB_R	CLOCKS	
PCLK33_0	K5	PCI_CLK66M_SB_INT_R	CLOCKS	
PCLK33_1	L6	PCI_CLK_P1_R	CLOCKS	
PCLK33_2	M7	AGP_CLK66M_GPU_R	CLOCKS	
PCLK33_3	L9	PCI_CLK_P3_R	CLOCKS	
PCLK33_4	M10	PCI_CLK_P4_R	CLOCKS	
HTBEN_0	K11	CPU_HTBEN_R	CLOCKS	
HTBEN_1	J12	CPU1_HTBEN_R	CLOCKS	14
NBSYNC	F12	EI_NB_SYNC_R	CLOCKS	
HSYNC_0	J10	EI_CPU_SYNC_R	CLOCKS	
HSYNC_1	H11	EI_CPU1_SYNC_R	CLOCKS	14
REFCLK_0	G2	SB_CLK25M_ATA_R	CLOCKS	
REFCLK_1	H1	SATA_CLK25M_R	CLOCKS	
SLEWING*	K9	SLEWING_L_R	CLOCKS	
ERROR*	M8	CLOCK_ERROR_L 8		
PCLK12	L11	HT_CLK66M_SB_R	CLOCKS	
PCLK15	L10	AGP_CLK66M_NB_R	CLOCKS	

SCLK	C1	18 I2C_CLOCK_SCL		
SDATA	B1	18 I2C_CLOCK_SDA		
RESET*	D3	PLS_RESET_L	13 CLOCK_RESET_L	R2704 0 5% 402
XIN	C11	PLS_X_IN		
XOUT	B12	PLS_X_OUT		
ADDRSEL	E3	PLS_X_ADDRSEL		R2738 1K 5% 402 NOSTUFF
TEST1	K3	6 TP_PLS_TEST1		
TEST2	E11	6 TP_PLS_TEST2		
TEST3	D11	6 TP_PLS_TEST3		
SCAN_MODE	M1	PLS_SCAN_MODE	R2706 249 1%	
REF15	G11	PLS_REF15	R2744 681 1%	
REF25	J2	PLS_REF25	R2740 1K 1%	
REF33	M6	PLS_REF33	R2746 1K 1%	
REF_CML	A5	6 TP_PLS_REF_CML		
PRES_CML	B6	PLS_PRES_CML	R2742 806 1%	
FORCESPO*	F2	PLS_FORCE_P0_L_R		
PD	C3			

0=IIC ADDR D2/D3
1=IIC ADDR D4/D5

18 11 6 PP3V3_PWRON
R2722 1K 5% 1/16W MF 402
NOSTUFF R2748 0 5% 1/16W MF 402
25 16 13 SYS_OVERTEMP_L

3 =PULSAR_POWER_DOWN
R2750 47 1 2 402 5% PULSAR_POWER_DOWN_R
NOSTUFF R2724 1K 1 2 402 5%

17 PLS_EXTCLK
NOSTUFF J2700 U.FL-R SMT F-ST-SM
NOSTUFF R2762 24 5% 1/16W MF 402
PLS_INTERM
NOSTUFF R2764 24 5% 1/16W MF 402
NO STUFF R2752 0 5% 1/16W MF 402
R2754 0 5% 1/16W MF 402
NO STUFF R2758 330K 5% 1/16W MF 402
R2756 0 5% 1/16W MF 402
CRITICAL Y2701 25.0000M 8X4.5MM-SM
PLS_X_IN_B
PLS_X_OUT_B
C2707 33PF 5% 50V CERM 402
C2705 33PF 5% 50V CERM 402

R2701 0 5% 3.3V 33MHZ PCI_CLK_GP0 8
R2761 0 5% 402 3.3V 33MHZ PCI_CLK_GP1 8
C2708 0.001UF 50V 10% 2CERM 402
C2710 0.001UF 50V 10% 2CERM 402
VSP_NB_CLK_P 24 27
VSP_NB_CLK_N 24 27
C2713 0.001UF 50V 10% 2CERM 402
C2715 0.001UF 50V 10% 2CERM 402
EI_CPU_CLK_P 27 29
EI_CPU_CLK_N 27 29
C2700 0.001UF 50V 10% 2CERM 402
C2702 0.001UF 50V 10% 2CERM 402
EI_NB_CLK_P 27 28
EI_NB_CLK_N 27 28

R2775 0 5% 402	NOSTUFF	2.5V	66MHZ	TP_PLS_CLK_66M_0 6
R2776 0 5% 402	NOSTUFF	2.5V	66MHZ	TP_PLS_CLK_66M_1 6
R2703 20 5% 402		2.5V	66MHZ	HT_CLK66M_NB 27 40
R2709 20 5% 402		2.5V	66MHZ	RAM_CLK66M_NB 37
R2705 0 5% 402		3.3V	66MHZ	PCI_CLK66M_SB_INT 27 74
R2711 0 5% 402		3.3V	33MHZ	PCI_CLK_P1 8
R2707 0 5% 402		3.3V	66MHZ	AGP_CLK66M_GPU 27 49
R2702 0 5% 402		3.3V	33MHZ	PCI_CLK_P3 8
R2779 0 5% 402				PCI_CLK_P4 8
R2715 0 5% 402		1.2V	33MHZ	CPU_HTBEN 29 30
R2768 0 5% 402		1.2V		EI_NB_SYNC 27 28
R2772 0 5% 402		1.2V		EI_CPU_SYNC 27 29
R2770 22 5% 402	NOSTUFF	2.5V	25MHZ	SB_CLK25M_ATA 25
R2700 0 5% 402		2.5V	25MHZ	TP_SATA_CLK25M 6
R2720 0 5% 402	SYS_SLEWING_L 13 25 33			
R2717 0 5% 402		1.2V	66MHZ	HT_CLK66M_SB 27 62
R2719 0 5% 402		1.5V	66MHZ	AGP_CLK66M_NB 27 48

MASTER: GILA
LAST MODIFIED: JULY 12, 04

PULSAR CLOCKS

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=PP1V2_EI_NB 7 14 18 28

C2800 0.1UF 20% 10V CERM 402
C2801 0.1UF 20% 10V CERM 402
C2802 0.1UF 20% 10V CERM 402
C2803 0.1UF 20% 10V CERM 402
C2804 0.1UF 20% 10V CERM 402
C2805 0.1UF 20% 10V CERM 402
C2806 0.1UF 20% 10V CERM 402
C2807 0.1UF 20% 10V CERM 402
C2808 0.1UF 20% 10V CERM 402
C2809 0.1UF 20% 10V CERM 402
C2810 0.1UF 20% 10V CERM 402
C2811 0.1UF 20% 10V CERM 402
C2812 0.1UF 20% 10V CERM 402
C2813 0.1UF 20% 10V CERM 402
C2814 0.1UF 20% 10V CERM 402
C2815 0.1UF 20% 10V CERM 402
C2816 0.1UF 20% 10V CERM 402
C2817 0.1UF 20% 10V CERM 402

60 48 37 7 =PP1V5_PWRON_NB_AVDD

R2800 2.2 5% 1/16W MF 603

PP1V5_PWRON_EI_NB_AVDD VOLTAGE=1.5V
MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

C2818 1UF 10% 6.3V CERM 402
C2819 0.1UF 20% 10V CERM 402

=PP1V2_EI_NB 7 14 18 28

U3 U3LITE V1.0-300MM PBGA (SYM 1 OF 7) OMIT

APPLE PI INTERFACE

EI_NB_TO_CPU_CLK_P	F15	APIO_BCLKIP	
EI_NB_TO_CPU_CLK_N	E15	APIO_BCLKIN	
EI_NB_TO_CPU_AD<0>	F11	APIO_ADI0	
EI_NB_TO_CPU_AD<1>	F12	APIO_ADI1	
EI_NB_TO_CPU_AD<2>	G11	APIO_ADI2	
EI_NB_TO_CPU_AD<3>	H11	APIO_ADI3	
EI_NB_TO_CPU_AD<4>	G12	APIO_ADI4	
EI_NB_TO_CPU_AD<5>	H12	APIO_ADI5	
EI_NB_TO_CPU_AD<6>	H14	APIO_ADI6	
EI_NB_TO_CPU_AD<7>	G14	APIO_ADI7	
EI_NB_TO_CPU_AD<8>	D9	APIO_ADI8	
EI_NB_TO_CPU_AD<9>	C9	APIO_ADI9	
EI_NB_TO_CPU_AD<10>	D11	APIO_ADI10	
EI_NB_TO_CPU_AD<11>	E11	APIO_ADI11	
EI_NB_TO_CPU_AD<12>	A10	APIO_ADI12	
EI_NB_TO_CPU_AD<13>	A9	APIO_ADI13	
EI_NB_TO_CPU_AD<14>	A8	APIO_ADI14	
EI_NB_TO_CPU_AD<15>	B9	APIO_ADI15	
EI_NB_TO_CPU_AD<16>	C11	APIO_ADI16	
EI_NB_TO_CPU_AD<17>	B11	APIO_ADI17	
EI_NB_TO_CPU_AD<18>	A11	APIO_ADI18	
EI_NB_TO_CPU_AD<19>	A12	APIO_ADI19	
EI_NB_TO_CPU_AD<20>	B12	APIO_ADI20	
EI_NB_TO_CPU_AD<21>	C12	APIO_ADI21	
EI_NB_TO_CPU_AD<22>	D12	APIO_ADI22	
EI_NB_TO_CPU_AD<23>	E12	APIO_ADI23	
EI_NB_TO_CPU_AD<24>	A13	APIO_ADI24	
EI_NB_TO_CPU_AD<25>	A14	APIO_ADI25	
EI_NB_TO_CPU_AD<26>	B14	APIO_ADI26	
EI_NB_TO_CPU_AD<27>	C14	APIO_ADI27	
EI_NB_TO_CPU_AD<28>	A16	APIO_ADI28	
EI_NB_TO_CPU_AD<29>	A15	APIO_ADI29	
EI_NB_TO_CPU_AD<30>	B15	APIO_ADI30	
EI_NB_TO_CPU_AD<31>	C15	APIO_ADI31	
EI_NB_TO_CPU_AD<32>	H15	APIO_ADI32	
EI_NB_TO_CPU_AD<33>	G15	APIO_ADI33	
EI_NB_TO_CPU_AD<34>	F17	APIO_ADI34	
EI_NB_TO_CPU_AD<35>	G17	APIO_ADI35	
EI_NB_TO_CPU_AD<36>	G18	APIO_ADI36	
EI_NB_TO_CPU_AD<37>	H18	APIO_ADI37	
EI_NB_TO_CPU_AD<38>	F18	APIO_ADI38	
EI_NB_TO_CPU_AD<39>	E18	APIO_ADI39	
EI_NB_TO_CPU_AD<40>	A17	APIO_ADI40	
EI_NB_TO_CPU_AD<41>	A18	APIO_ADI41	
EI_NB_TO_CPU_AD<42>	B17	APIO_ADI42	
EI_NB_TO_CPU_AD<43>	C17	APIO_ADI43	
EI_NB_TO_CPU_SR_P<0>	D17	APIO_SRIP0	
EI_NB_TO_CPU_SR_N<0>	A19	APIO_SRIN0	
EI_NB_TO_CPU_SR_P<1>	E17	APIO_SRIP1	
EI_NB_TO_CPU_SR_N<1>	B18	APIO_SRIN1	
EI_QACK_L	D14	API_QACK0	
	E8	APIO_APSYNC	
	H17	APIO_SE	

APIO_BCLKOP	D6	EI_CPU_TO_NB_CLK_P	6 14 28 29
APIO_BCLKON	E6	EI_CPU_TO_NB_CLK_N	6 14 28 29
APIO_ADO0	J2	EI_CPU_TO_NB_AD<0>	6 14 28 29
APIO_ADO1	H1	EI_CPU_TO_NB_AD<1>	6 14 28 29
APIO_ADO2	J1	EI_CPU_TO_NB_AD<2>	6 14 28 29
APIO_ADO3	K1	EI_CPU_TO_NB_AD<3>	6 14 28 29
APIO_ADO4	E1	EI_CPU_TO_NB_AD<4>	6 14 28 29
APIO_ADO5	F2	EI_CPU_TO_NB_AD<5>	6 14 28 29
APIO_ADO6	J4	EI_CPU_TO_NB_AD<6>	6 14 28 29
APIO_ADO7	H4	EI_CPU_TO_NB_AD<7>	6 14 28 29
APIO_ADO8	G1	EI_CPU_TO_NB_AD<8>	6 14 28 29
APIO_ADO9	H2	EI_CPU_TO_NB_AD<9>	6 14 28 29
APIO_ADO10	F1	EI_CPU_TO_NB_AD<10>	6 14 28 29
APIO_ADO11	H5	EI_CPU_TO_NB_AD<11>	6 14 28 29
APIO_ADO12	H3	EI_CPU_TO_NB_AD<12>	6 14 28 29
APIO_ADO13	J3	EI_CPU_TO_NB_AD<13>	6 14 28 29
APIO_ADO14	J5	EI_CPU_TO_NB_AD<14>	6 14 28 29
APIO_ADO15	J6	EI_CPU_TO_NB_AD<15>	6 14 28 29
APIO_ADO16	E3	EI_CPU_TO_NB_AD<16>	6 14 28 29
APIO_ADO17	F4	EI_CPU_TO_NB_AD<17>	6 14 28 29
APIO_ADO18	E2	EI_CPU_TO_NB_AD<18>	6 14 28 29
APIO_ADO19	F5	EI_CPU_TO_NB_AD<19>	6 14 28 29
APIO_ADO20	H6	EI_CPU_TO_NB_AD<20>	6 14 28 29
APIO_ADO21	J7	EI_CPU_TO_NB_AD<21>	6 14 28 29
APIO_ADO22	F3	EI_CPU_TO_NB_AD<22>	6 14 28 29
APIO_ADO23	J8	EI_CPU_TO_NB_AD<23>	6 14 28 29
APIO_ADO24	F6	EI_CPU_TO_NB_AD<24>	6 14 28 29
APIO_ADO25	E5	EI_CPU_TO_NB_AD<25>	6 14 28 29
APIO_ADO26	D5	EI_CPU_TO_NB_AD<26>	6 14 28 29
APIO_ADO27	E4	EI_CPU_TO_NB_AD<27>	6 14 28 29
APIO_ADO28	D8	EI_CPU_TO_NB_AD<28>	6 14 28 29
APIO_ADO29	A5	EI_CPU_TO_NB_AD<29>	6 14 28 29
APIO_ADO30	C2	EI_CPU_TO_NB_AD<30>	6 14 28 29
APIO_ADO31	C3	EI_CPU_TO_NB_AD<31>	6 14 28 29
APIO_ADO32	C5	EI_CPU_TO_NB_AD<32>	6 14 28 29
APIO_ADO33	C6	EI_CPU_TO_NB_AD<33>	6 14 28 29
APIO_ADO34	B2	EI_CPU_TO_NB_AD<34>	6 14 28 29
APIO_ADO35	D1	EI_CPU_TO_NB_AD<35>	6 14 28 29
APIO_ADO36	B1	EI_CPU_TO_NB_AD<36>	6 14 28 29
APIO_ADO37	C1	EI_CPU_TO_NB_AD<37>	6 14 28 29
APIO_ADO38	A6	EI_CPU_TO_NB_AD<38>	6 14 28 29
APIO_ADO39	C8	EI_CPU_TO_NB_AD<39>	6 14 28 29
APIO_ADO40	A2	EI_CPU_TO_NB_AD<40>	6 14 28 29
APIO_ADO41	B3	EI_CPU_TO_NB_AD<41>	6 14 28 29
APIO_ADO42	A7	EI_CPU_TO_NB_AD<42>	6 14 28 29
APIO_ADO43	B8	EI_CPU_TO_NB_AD<43>	6 14 28 29
APIO_SROP0	A3	EI_CPU_TO_NB_SR_P<0>	6 14 28 29
APIO_SRON0	A4	EI_CPU_TO_NB_SR_N<0>	6 14 28 29
APIO_SROP1	B5	EI_CPU_TO_NB_SR_P<1>	6 14 28 29
APIO_SRON1	B6	EI_CPU_TO_NB_SR_N<1>	6 14 28 29
API_QREQ0	E14		
API_APCLKP	D18	EI_NB_CLK_P	
API_APCLKN	C18	EI_NB_CLK_N	
API_CSTP	F14	CPU_CHKSTOP_L	29

PLACE R2805 AND R2806 NEAR U3LITE

R2805 0 5% 1/16W MF 402
27 EI_NB_SYNC — NB_APSYNC

NOSTUFF R2806 0 5% 1/16W MF 402
29 EI_SYNC_FROM_NB
30 29 14 6 EI_SE

API_APCLK_AVSS

C2821 0.001UF 10% 50V CERM 402

=PP1V2_EI_NB 7 14 18 28

NOSTUFF R2802 100 1% 1/16W MF 402

EI_APCLK_VREF VOLTAGE=0.6V

NOSTUFF R2801 100 1% 1/16W MF 402
NOSTUFF C2820 0.1UF 20% 10V CERM 402
NOSTUFF R2803 121 1% 1/16W MF 402
NOSTUFF R2804 121 1% 1/16W MF 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

EI_NB_CLK_P 27
EI_NB_CLK_N 27

QREQ_L HACK

28 7 =PP3V3_PWRON_EI

C2850 0.1UF 20% 10V CERM 402

CRITICAL U2850 74LVC1G66 SOT23-5 TI

30 29 14 6 EI_QREQ_L
EI_NB_QREQ_L
25 24 13 SMU_SUSPENDREQ_L

NOSTUFF R2850 0 5% 1/16W MF 402

NOSTUFF R2899 180 5% 1/16W MF 402
EI_NB_QREQ_L_R

R2851 10K 5% 1/16W MF 402

QREQ TO SMU

28 7 =PP3V3_PWRON_EI

NOSTUFF R2898 10K 5% 1/16W MF 402
SMU_QREQ 13

NOSTUFF Q2899 2N3904 SM

POST-RAMP QUAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:	
353S0920	353S0867		U2850	PERICOM ANALOG SWITCH	CRITICAL
353S0924	353S0867		U2850	MAXIM ANALOG SWITCH	

PLACE QREQ CIRCUITS BETWEEN CPU AND U3LITE

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
EI_CPU_TO_NB_CLK_P	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	2233
EI_CPU_TO_NB_CLK_N	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	2234
EI_NB_TO_CPU_CLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	2235
EI_NB_TO_CPU_CLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	2236
EI_CPU_TO_NB_AD<0..43>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_AD		2216
EI_NB_TO_CPU_AD<0..43>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_AD		2217
EI_CPU_TO_NB_SR_P<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	2218
EI_CPU_TO_NB_SR_N<0>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR0	2219
EI_CPU_TO_NB_SR_P<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	2220
EI_CPU_TO_NB_SR_N<1>	EI_CPU_TO_NB_CAD	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_SR1	2221
EI_NB_TO_CPU_SR_P<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	2222
EI_NB_TO_CPU_SR_N<0>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR0	2223
EI_NB_TO_CPU_SR_P<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	2224
EI_NB_TO_CPU_SR_N<1>	EI_NB_TO_CPU_CAD	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_SR1	2225

OMIT HOLE-VIA-20R10 ZT2847 ZT2857 ZT2867 ZT2807 ZT2817 ZT2827 ZT2837
ZT2848 ZT2858 ZT2868 ZT2808 ZT2818 ZT2828 ZT2838
ZT2849 ZT2859 ZT2869 ZT2809 ZT2819 ZT2829 ZT2839
ZT2850 ZT2860 ZT2800 ZT2810 ZT2820 ZT2830 ZT2840
ZT2851 ZT2861 ZT2801 ZT2811 ZT2821 ZT2831 ZT2841
ZT2852 ZT2862 ZT2802 ZT2812 ZT2822 ZT2832 ZT2842
ZT2853 ZT2863 ZT2803 ZT2813 ZT2823 ZT2833 ZT2843
ZT2854 ZT2864 ZT2804 ZT2814 ZT2824 ZT2834 ZT2844
ZT2855 ZT2865 ZT2805 ZT2815 ZT2825 ZT2835 ZT2845
ZT2806 ZT2816 ZT2826 ZT2836
ZT2846 ZT2856 ZT2866

MASTER: GILA
LAST MODIFIED: JULY 14, 04

U3LITE APPLE PI

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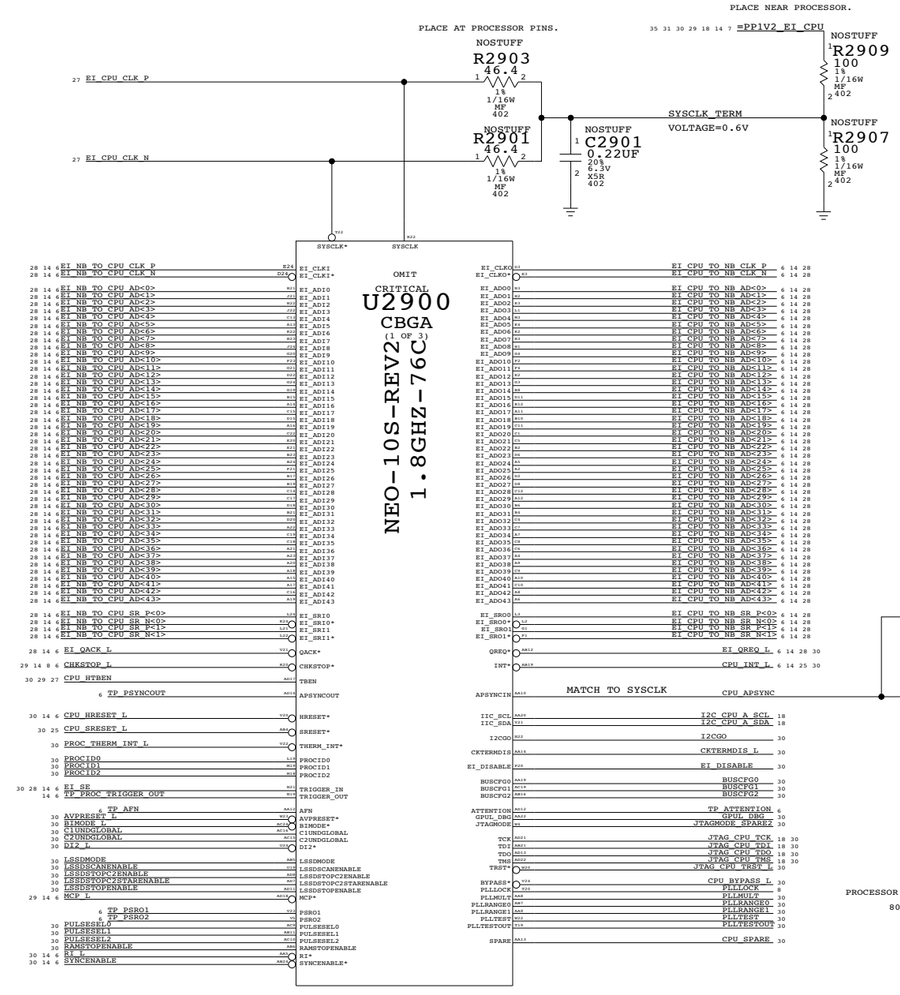
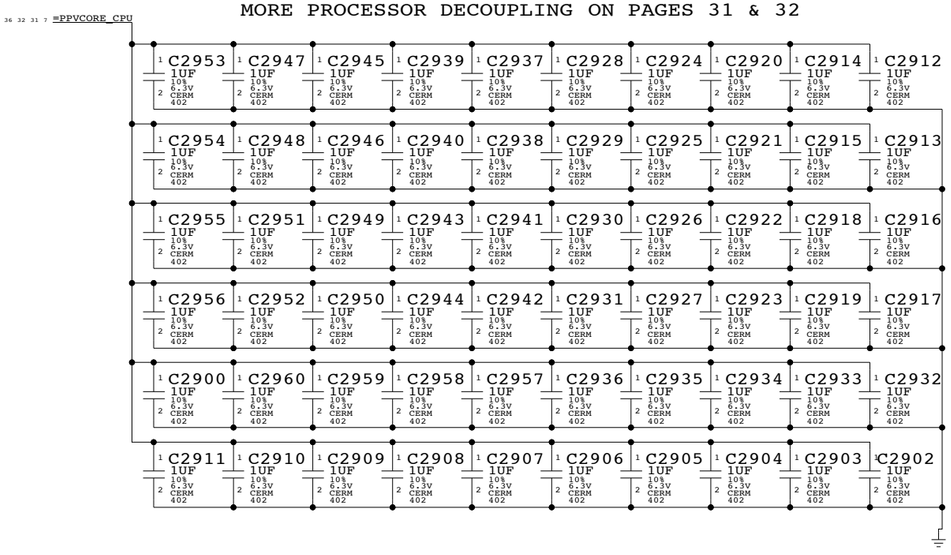
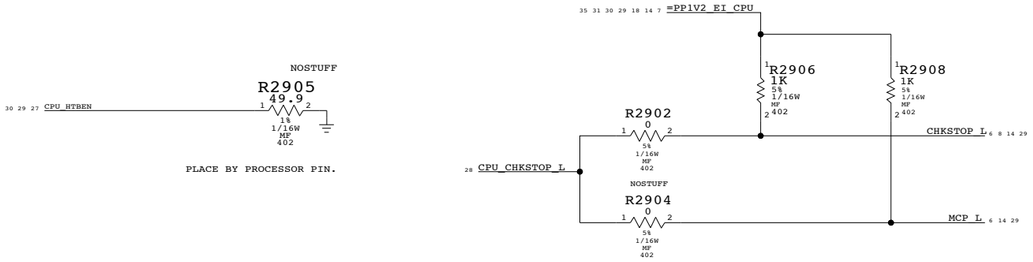
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 28 OF 103	







PROCESSOR LOGIC I/O

MASTER: GILA
LAST MODIFIED: APR 09, 04

NEO APPLE PI

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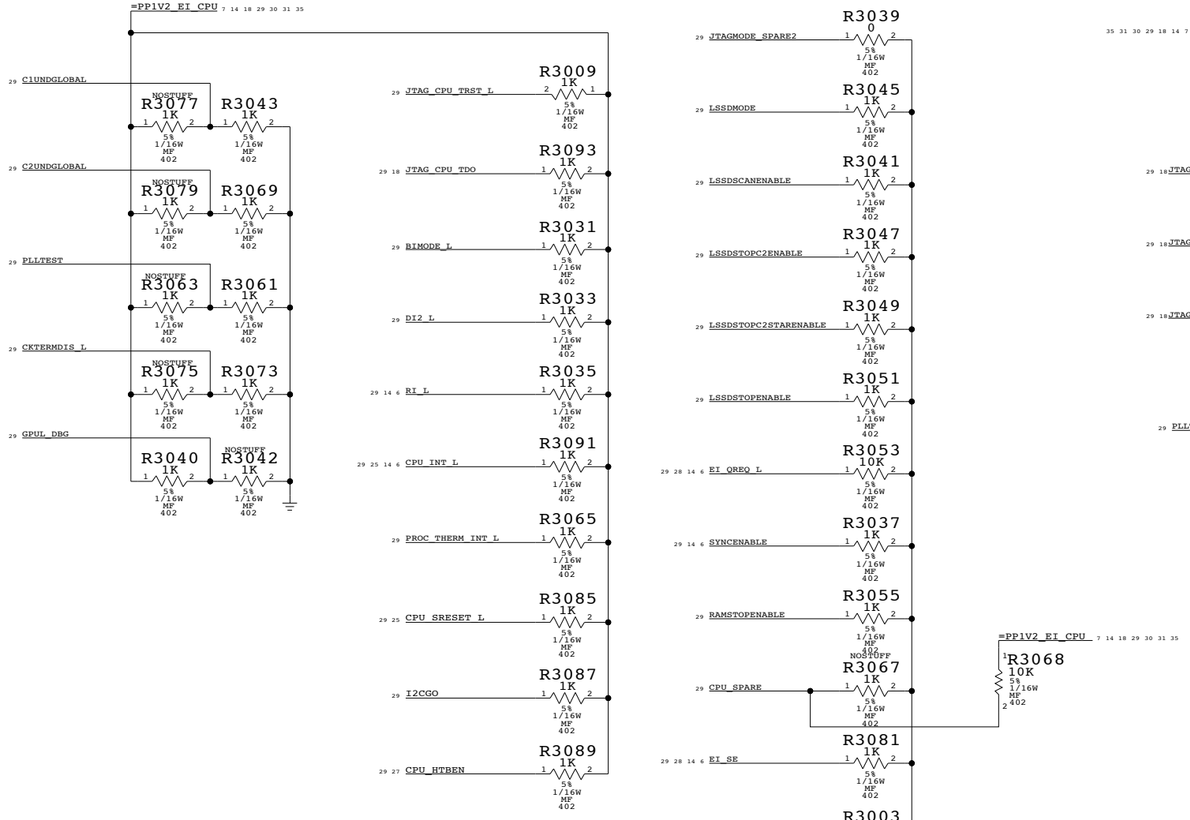

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3034	EI_3TO1	SYSCLK * 12
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3018	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3028	EI_2TO1	PROC / 2
*	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3026,R3012	EI_3TO1	PROC / 3
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3028	NOSTUFF	PROC / 4
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3024,R3010,R3012	NOSTUFF	PROC / 6
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3028	NOSTUFF	PROC / 8
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3026,R3012	NOSTUFF	PROC / 12
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3028	NOSTUFF	PROC / 16
	114S1103	3	RES,1K OHM,1/16W,5%,0402	R3008,R3010,R3012	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3036		
	114S1103	1	RES,1K OHM,1/16W,5%,0402	R3020	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
>= 1.8 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3032	CPU_PLL_LOW	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3030,R3016	CPU_PLL_HIGH	
<= 1.6 GHZ *	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3032	CPU_PLL_MEDIUM	
	114S1103	2	RES,1K OHM,1/16W,5%,0402	R3014,R3016	NOSTUFF	RESERVED

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3022		AVPRESET OFF
114S1103	1	RES,1K OHM,1/16W,5%,0402	R3038	NOSTUFF	AVPRESET ON

* STUFF THESE ON Q45.

SYSTEM CONFIGURATION

MASTER: GILA

LAST MODIFIED: APR 27, 04

CPU STRAPS

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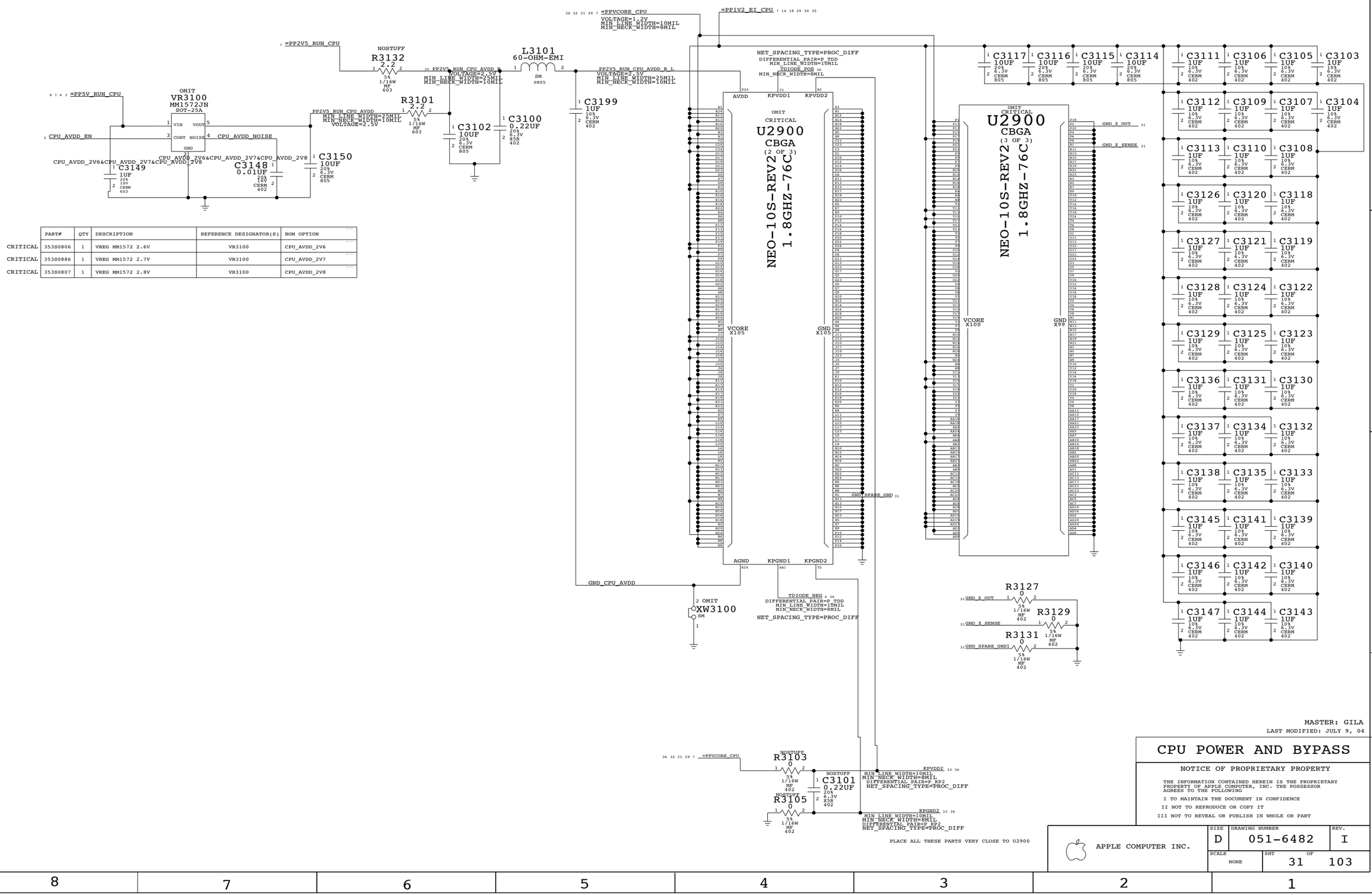
SCALE: NONE	SHT 30 OF 103	



	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	353S0806	1	VREG MM1572 2.6V	VR3100	CPU_AVDD_2V6
CRITICAL	353S0886	1	VREG MM1572 2.7V	VR3100	CPU_AVDD_2V7
CRITICAL	353S0807	1	VREG MM1572 2.8V	VR3100	CPU_AVDD_2V8

MASTER: GILA
LAST MODIFIED: JULY 9, 04

CPU POWER AND BYPASS

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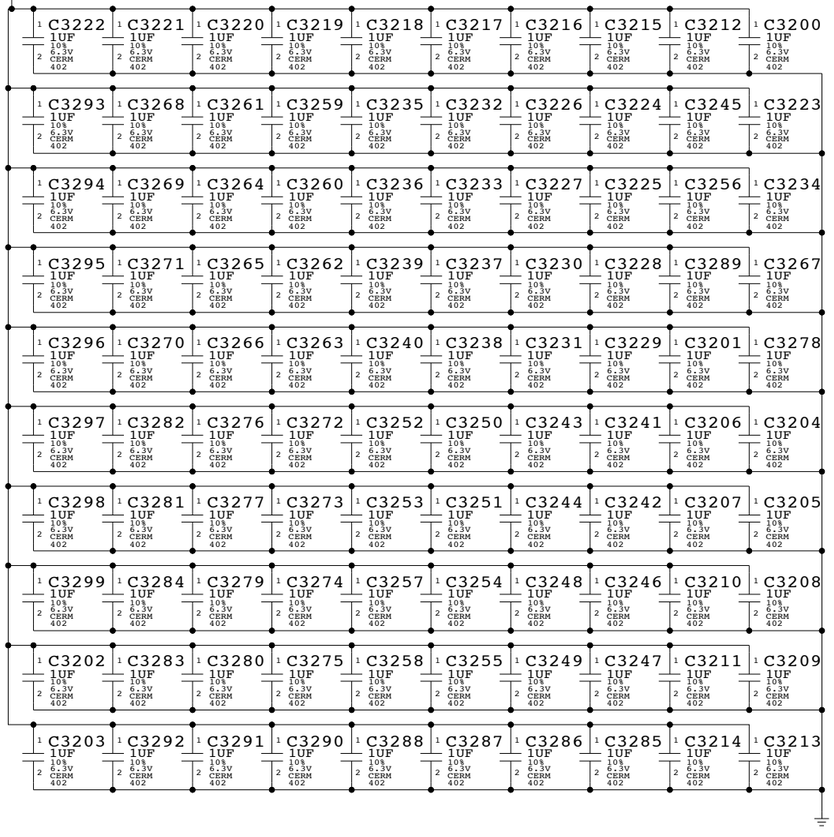
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 31 OF 103	

36 31 29 7 =PPVCORE_CPU



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PROC DECOUPLING

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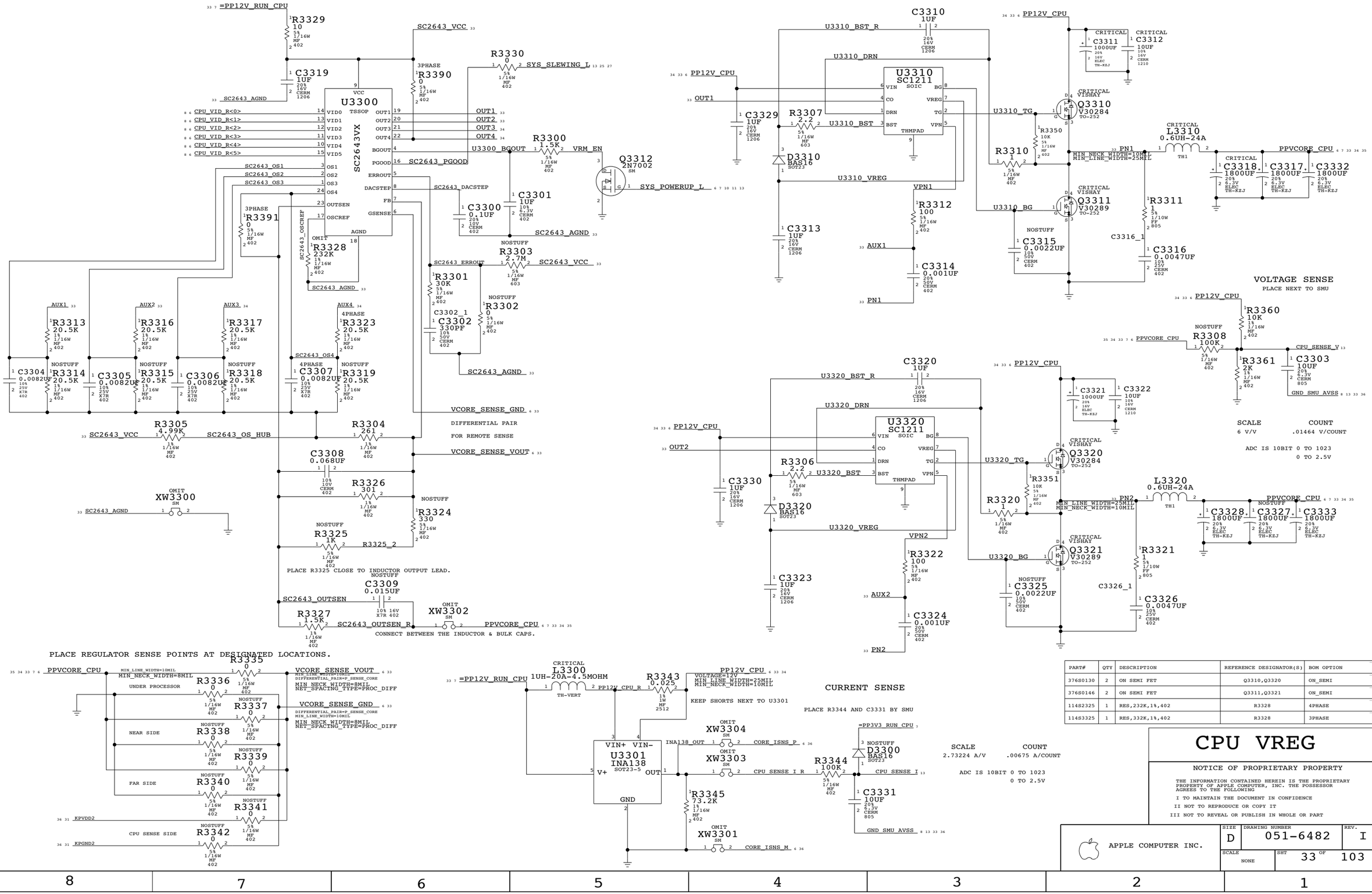
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 32 OF 103	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0130	2	ON SEMI FET	Q3310,Q3320	ON_SEMI
376S0146	2	ON SEMI FET	Q3311,Q3321	ON_SEMI
114S2325	1	RES,232K,1%,402	R3328	4PHASE
114S3325	1	RES,332K,1%,402	R3328	3PHASE

CPU VREG

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SIZE	DRAWING NUMBER	REV.
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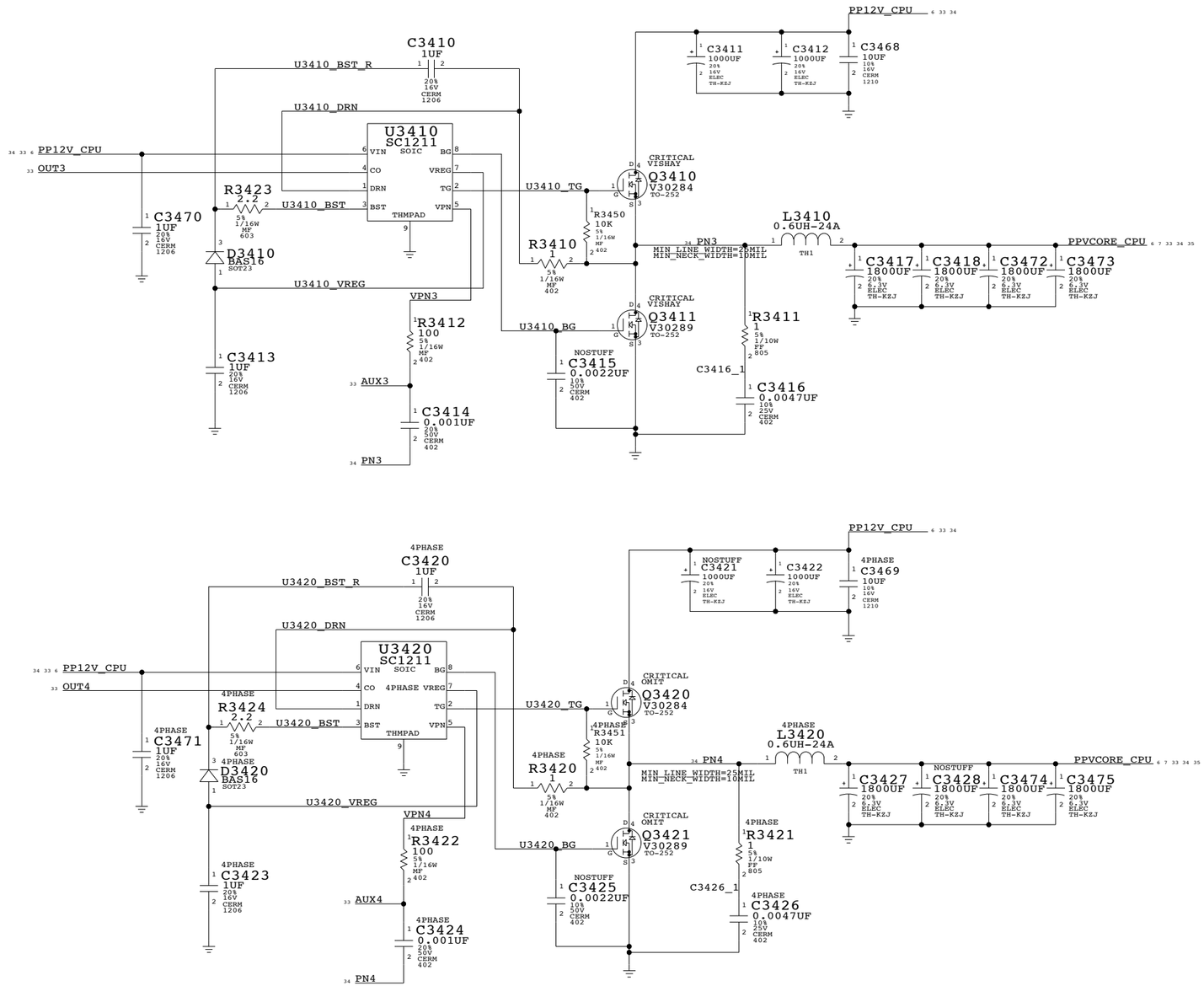
SCALE: NONE	SHT 33 OF 103	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
376S0130	1	ON SEMI FET	Q3410	ON_SEMI
376S0146	1	ON SEMI FET	Q3411	ON_SEMI
376S0130	1	ON SEMI FET	Q3420	4PHASE_ON
376S0146	1	ON SEMI FET	Q3421	4PHASE_ON
376S0204	1	VISHAY FET	Q3420	4PHASE_VISH
376S0207	1	VISHAY FET	Q3421	4PHASE_VISH

CPU VREG

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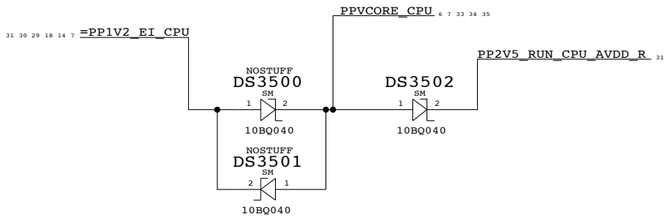
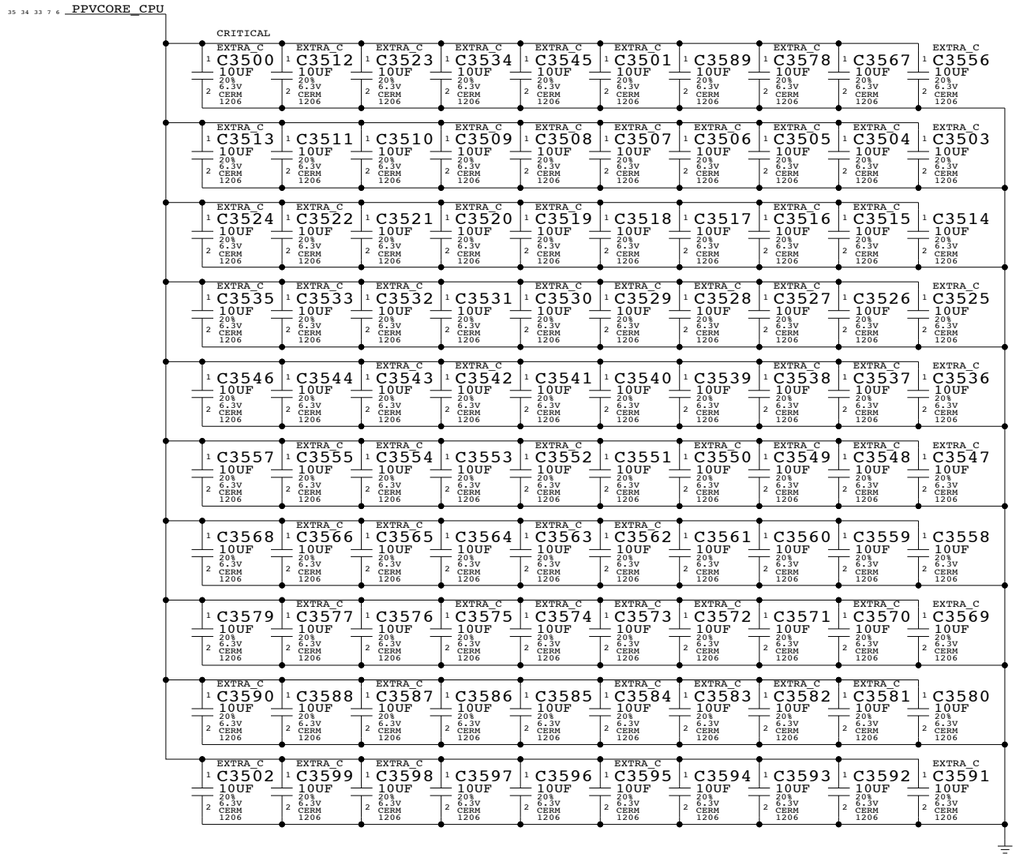
SCALE	SHT
NONE	34 OF 103





CPU VREG OUTPUT CAPS

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 35 OF 103	

NOSTUFF
DS3602
SM
=PP5V_PWRON_CPU
MBR0530
=PP5V_ALL_CPU
R3602
2
5%
1/16W
MF
603
C3603
2.2UF
20%
10V
CERM
805
C3604
2.2UF
C3605
2.2UF
C3600
2.2UF
XW3601
SM
OMIT
MIN_LINE_WIDTH=15MIL
MIN_NECK_WIDTH=10MIL
DAVDD
DAGND
XW3600, R3602, AND DS3602 MUST BE PLACED CLOSE TO SMU

100UA CURRENT SOURCE

THESE SIGNALS HAVE A MIN_LINE_WIDTH=10MIL
AND MIN_NECK_WIDTH=8MIL

R3606
10K
0.1%
1/16W
FF
603
R3603
10K
DAGND
TD1
TD_CURRENT
10MIL
8MIL
U3601
LMV2011
SOT23-5
DAVDD
R3604
20K
ADC_REF
TD2
R3608
12.7K
1%
BUFFER
U3602
R3607
20K
R3605
10K
TD_BUFFERED
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
C3607
10UF
20%
6.3V
CERM
805
R3609
10K
TD3
R3611
100K
R3612
40.2K
U3603
TDIODE_POS
TDIODE_NEG
R3610
10K
R3615
0
R3616
1K
=PPVCORE_CPU
R3613
40.2K
R3614
100K
C3608
10UF
C3610
0.0022UF
10%
50V
CERM
402
C3606
0.0022UF
R3628
100K
CPU_TEMP
CPU_TEMP_R
C3613
10UF
GND_SMU_AVSS
NEED TO CONNECT TO P65 OF 80PIN SMU OR PIN 49 OF 64PIN SMU

POWER MONITOR

=PP3V3_ALL_CPU
R3650
0
=PP3V3_PWRON_CPU
DS3650
MBR0530
PP3V3_CPU_DIODE
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL
R3601
200
C3601
2.2UF
R3690
0
PPVREF_SMU_ADC_REF
D3600
2.5V
SSOT-23
C3602
0.47UF
R3691
0
GND_SMU_AVSS_DAGND
NEEDED FOR FMAX
R3620
51
FMAXT_P
DIFFERENTIAL_PAIR=P_FMAXT
NET_SPACING_TYPE=PROC_DIFF
R3619
0
5%
1/10W
FP
805
R3621
51
FMAXT_M
PLACE AT BOARD EDGE

J3600
BM12B-SRSS-TB
F-ST-SM
PLACE CLOSE
TO U2900
XW3611
XW3612
XW3613
XW3614
KPVDD2_FMAX
KPGND2_FMAX
TDIODE_POS_FMAX
TDIODE_NEG_FMAX
DIFFERENTIAL_PAIR=KP2_FMAX
DIFFERENTIAL_PAIR=TDIODE
MIN_LINE_WIDTH=10MIL
MIN_NECK_WIDTH=8MIL
NET_SPACING_TYPE=PROC_DIFF
CORE_ISNS_M
CORE_ISNS_P
DIFFERENTIAL_PAIR=CORE_ISNS

CPU DIODE CONDITIONER

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SCALE	SHT	OF
NONE	36	103

U3TWINS DO NOT HAVE MASKS

=PP2V5_PWRON_RAM

U3 U3LITE V1.0-300MM PBGA (SYM 2 OF 7) OMIT

MEMORY DATA INTERFACE

RAM_DQ_R<0>	AF20	DDR_DQ0	DDR_DQ64 / AG27 / RAM_DQ_R<64>
RAM_DQ_R<1>	AH22	DDR_DQ1	DDR_DQ65 / AF24 / RAM_DQ_R<65>
RAM_DQ_R<2>	AH21	DDR_DQ2	DDR_DQ66 / AE24 / RAM_DQ_R<66>
RAM_DQ_R<3>	AG21	DDR_DQ3	DDR_DQ67 / AG26 / RAM_DQ_R<67>
RAM_DQ_R<4>	AB20	DDR_DQ4	DDR_DQ68 / AF26 / RAM_DQ_R<68>
RAM_DQ_R<5>	AC21	DDR_DQ5	DDR_DQ69 / AD24 / RAM_DQ_R<69>
RAM_DQ_R<6>	AD23	DDR_DQ6	DDR_DQ70 / AD25 / RAM_DQ_R<70>
RAM_DQ_R<7>	AD21	DDR_DQ7	DDR_DQ71 / AG28 / RAM_DQ_R<71>
RAM_DQ_R<8>	AH26	DDR_DQ8	DDR_DQ72 / AF28 / RAM_DQ_R<72>
RAM_DQ_R<9>	AH25	DDR_DQ9	DDR_DQ73 / AE28 / RAM_DQ_R<73>
RAM_DQ_R<10>	AH24	DDR_DQ10	DDR_DQ74 / AD26 / RAM_DQ_R<74>
RAM_DQ_R<11>	AH23	DDR_DQ11	DDR_DQ75 / AF27 / RAM_DQ_R<75>
RAM_DQ_R<12>	AH27	DDR_DQ12	DDR_DQ76 / AC26 / RAM_DQ_R<76>
RAM_DQ_R<13>	AG24	DDR_DQ13	DDR_DQ77 / AC25 / RAM_DQ_R<77>
RAM_DQ_R<14>	AF23	DDR_DQ14	DDR_DQ78 / AC27 / RAM_DQ_R<78>
RAM_DQ_R<15>	AH28	DDR_DQ15	DDR_DQ79 / AD27 / RAM_DQ_R<79>
RAM_DQ_R<16>	U25	DDR_DQ16	DDR_DQ80 / AA27 / RAM_DQ_R<80>
RAM_DQ_R<17>	AA23	DDR_DQ17	DDR_DQ81 / AA26 / RAM_DQ_R<81>
RAM_DQ_R<18>	Y22	DDR_DQ18	DDR_DQ82 / AA24 / RAM_DQ_R<82>
RAM_DQ_R<19>	AA22	DDR_DQ19	DDR_DQ83 / AA28 / RAM_DQ_R<83>
RAM_DQ_R<20>	U24	DDR_DQ20	DDR_DQ84 / Y26 / RAM_DQ_R<84>
RAM_DQ_R<21>	V23	DDR_DQ21	DDR_DQ85 / Y25 / RAM_DQ_R<85>
RAM_DQ_R<22>	V22	DDR_DQ22	DDR_DQ86 / Y28 / RAM_DQ_R<86>
RAM_DQ_R<23>	U22	DDR_DQ23	DDR_DQ87 / Y24 / RAM_DQ_R<87>
RAM_DQ_R<24>	P25	DDR_DQ24	DDR_DQ88 / V26 / RAM_DQ_R<88>
RAM_DQ_R<25>	R22	DDR_DQ25	DDR_DQ89 / V27 / RAM_DQ_R<89>
RAM_DQ_R<26>	R21	DDR_DQ26	DDR_DQ90 / V24 / RAM_DQ_R<90>
RAM_DQ_R<27>	U23	DDR_DQ27	DDR_DQ91 / W28 / RAM_DQ_R<91>
RAM_DQ_R<28>	P26	DDR_DQ28	DDR_DQ92 / U27 / RAM_DQ_R<92>
RAM_DQ_R<29>	R24	DDR_DQ29	DDR_DQ93 / V28 / RAM_DQ_R<93>
RAM_DQ_R<30>	P24	DDR_DQ30	DDR_DQ94 / T28 / RAM_DQ_R<94>
RAM_DQ_R<31>	P23	DDR_DQ31	DDR_DQ95 / U26 / RAM_DQ_R<95>
RAM_DQ_R<32>	M25	DDR_DQ32	DDR_DQ96 / R27 / RAM_DQ_R<96>
RAM_DQ_R<33>	M23	DDR_DQ33	DDR_DQ97 / R26 / RAM_DQ_R<97>
RAM_DQ_R<34>	P21	DDR_DQ34	DDR_DQ98 / R28 / RAM_DQ_R<98>
RAM_DQ_R<35>	P22	DDR_DQ35	DDR_DQ99 / P27 / RAM_DQ_R<99>
RAM_DQ_R<36>	M24	DDR_DQ36	DDR_DQ100 / M28 / RAM_DQ_R<100>
RAM_DQ_R<37>	L22	DDR_DQ37	DDR_DQ101 / N28 / RAM_DQ_R<101>
RAM_DQ_R<38>	L23	DDR_DQ38	DDR_DQ102 / L28 / RAM_DQ_R<102>
RAM_DQ_R<39>	J23	DDR_DQ39	DDR_DQ103 / P28 / RAM_DQ_R<103>
RAM_DQ_R<40>	D23	DDR_DQ40	DDR_DQ104 / L25 / RAM_DQ_R<104>
RAM_DQ_R<41>	D24	DDR_DQ41	DDR_DQ105 / L26 / RAM_DQ_R<105>
RAM_DQ_R<42>	C26	DDR_DQ42	DDR_DQ106 / L27 / RAM_DQ_R<106>
RAM_DQ_R<43>	C27	DDR_DQ43	DDR_DQ107 / K28 / RAM_DQ_R<107>
RAM_DQ_R<44>	A22	DDR_DQ44	DDR_DQ108 / H27 / RAM_DQ_R<108>
RAM_DQ_R<45>	A25	DDR_DQ45	DDR_DQ109 / H28 / RAM_DQ_R<109>
RAM_DQ_R<46>	C24	DDR_DQ46	DDR_DQ110 / J27 / RAM_DQ_R<110>
RAM_DQ_R<47>	C23	DDR_DQ47	DDR_DQ111 / L24 / RAM_DQ_R<111>
RAM_DQ_R<48>	B24	DDR_DQ48	DDR_DQ112 / J25 / RAM_DQ_R<112>
RAM_DQ_R<49>	B23	DDR_DQ49	DDR_DQ113 / J24 / RAM_DQ_R<113>
RAM_DQ_R<50>	A23	DDR_DQ50	DDR_DQ114 / J26 / RAM_DQ_R<114>
RAM_DQ_R<51>	A24	DDR_DQ51	DDR_DQ115 / G28 / RAM_DQ_R<115>
RAM_DQ_R<52>	A27	DDR_DQ52	DDR_DQ116 / H25 / RAM_DQ_R<116>
RAM_DQ_R<53>	A28	DDR_DQ53	DDR_DQ117 / H24 / RAM_DQ_R<117>
RAM_DQ_R<54>	B28	DDR_DQ54	DDR_DQ118 / F27 / RAM_DQ_R<118>
RAM_DQ_R<55>	A26	DDR_DQ55	DDR_DQ119 / H26 / RAM_DQ_R<119>
RAM_DQ_R<56>	F24	DDR_DQ56	DDR_DQ120 / E28 / RAM_DQ_R<120>
RAM_DQ_R<57>	J22	DDR_DQ57	DDR_DQ121 / E27 / RAM_DQ_R<121>
RAM_DQ_R<58>	E23	DDR_DQ58	DDR_DQ122 / F26 / RAM_DQ_R<122>
RAM_DQ_R<59>	H23	DDR_DQ59	DDR_DQ123 / E26 / RAM_DQ_R<123>
RAM_DQ_R<60>	J21	DDR_DQ60	DDR_DQ124 / D28 / RAM_DQ_R<124>
RAM_DQ_R<61>	H21	DDR_DQ61	DDR_DQ125 / C28 / RAM_DQ_R<125>
RAM_DQ_R<62>	G21	DDR_DQ62	DDR_DQ126 / E25 / RAM_DQ_R<126>
RAM_DQ_R<63>	H22	DDR_DQ63	DDR_DQ127 / E24 / RAM_DQ_R<127>

=PP1V5_PWRON_NB_AVDD

R3702 2.2 5% 1/16W MF 603

PP1V5_PWRON_RAM_NB_AVDD VOLTAGE=1.5V

C3745 1UF 10% 6.3V CERM 402

C3744 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

=PP2V5_PWRON_RAM

DDR CLK_AVDD (AB21)

VDD_DDR (T19, T21, T25, P20, N21, N25, M19, K19, K23, K27, G25, F19, D22, D27, B25)

U3 U3LITE V1.0-300MM PBGA (SYM 3 OF 7) OMIT

MEMORY CONTROL INTERFACE

RAM_CLK66M_NB	AC20	DDR_CLKP	DDR_RAS / AE21 / RAM_RAS_L_R
RAM_CLK_A_P_R	AA12	DDR_CK_A	DDR_CAS / AD20 / RAM_CAS_L_R
RAM_CLK_A_N_R	AB12	DDR_CK_AN	DDR_WE / AC23 / RAM_WE_L_R
RAM_CLK_B_P_R	AB14	DDR_CK_B	DDR_BA0 / AF21 / RAM_BA_R<0>
RAM_CLK_B_N_R	AA14	DDR_CK_BN	DDR_BA1 / AE20 / RAM_BA_R<1>
RAM_CLK_C_P_R	AE15	DDR_CK_C	DDR_MUXEN0 / AH16 / RAM_MUXEN0
RAM_CLK_C_N_R	AE14	DDR_CK_CN	DDR_MUXEN4 / AH18 / RAM_MUXEN4
RAM_CLK_D_P_R	AC14	DDR_CK_D	DDR_MAD0 / AG12 / RAM_A_R<0>
RAM_CLK_D_N_R	AD14	DDR_CK_DN	DDR_MAD1 / AH13 / RAM_A_R<1>
RAM_CLK_E_P_R	AD15	DDR_CK_E	DDR_MAD2 / AE14 / RAM_A_R<2>
RAM_CLK_E_N_R	AC15	DDR_CK_EN	DDR_MAD3 / AH15 / RAM_A_R<3>
RAM_CLK_F_P_R	AA15	DDR_CK_F	DDR_MAD4 / AF12 / RAM_A_R<4>
RAM_CLK_F_N_R	AB15	DDR_CK_FN	DDR_MAD5 / AE12 / RAM_A_R<5>
RAM_CKE_R<0>	AC17	DDR_CKE0	DDR_MAD6 / AD12 / RAM_A_R<6>
RAM_CKE_R<1>	AD17	DDR_CKE1	DDR_MAD7 / AC12 / RAM_A_R<7>
RAM_CKE_R<2>	AE17	DDR_CKE2	DDR_MAD8 / AG15 / RAM_A_R<8>
RAM_CKE_R<3>	AF17	DDR_CKE3	DDR_MAD9 / AF15 / RAM_A_R<9>
RAM_CKE_R<4>	AB17	DDR_CKE4	DDR_MAD10 / AF14 / RAM_A_R<10>
RAM_CKE_R<5>	AA17	DDR_CKE5	DDR_MAD11 / AG14 / RAM_A_R<11>
RAM_CKE_R<6>	AB18	DDR_CKE6	DDR_MAD12 / AH17 / RAM_A_R<12>
RAM_CKE_R<7>	AA18	DDR_CKE7	DDR_MAD13 / AG17 / RAM_A_R<13>
	Y21	DDR_VREF0	DDR_CS0 / AF18 / RAM_CS_L_R<0>
	U21	DDR_VREF1	DDR_CS1 / AE18 / RAM_CS_L_R<1>
	L21	DDR_VREF2	DDR_CS2 / AG20 / RAM_CS_L_R<2>
	H20	DDR_VREF3	DDR_CS3 / AH20 / RAM_CS_L_R<3>
	AA21	DDR_VREF4	DDR_CS8 / AC18 / RAM_CS_L_R<8>
	M21	DDR_VREF5	DDR_CS9 / AD18 / RAM_CS_L_R<9>
	V21	DDR_VREF6	DDR_CS10 / AG18 / RAM_CS_L_R<10>
	J20	DDR_VREF7	DDR_CS11 / AH19 / RAM_CS_L_R<11>
			DDR_DQSP0 / AC24 / RAM_DQS_R<0>
			DDR_DQSP1 / AG23 / RAM_DQS_R<1>
			DDR_DQSP2 / Y23 / RAM_DQS_R<2>
			DDR_DQSP3 / R23 / RAM_DQS_R<3>
			DDR_DQSP4 / M22 / RAM_DQS_R<4>
			DDR_DQSP5 / B26 / RAM_DQS_R<5>
			DDR_DQSP6 / B27 / RAM_DQS_R<6>
			DDR_DQSP7 / F23 / RAM_DQS_R<7>
			DDR_DQSP8 / AE23 / RAM_DQS_R<8>
			DDR_DQSP9 / AD28 / RAM_DQS_R<9>
			DDR_DQSP10 / Y27 / RAM_DQS_R<10>
			DDR_DQSP11 / U28 / RAM_DQS_R<11>
			DDR_DQSP12 / M27 / RAM_DQS_R<12>
			DDR_DQSP13 / J28 / RAM_DQS_R<13>
			DDR_DQSP14 / F28 / RAM_DQS_R<14>
			DDR_DQSP15 / F25 / RAM_DQS_R<15>

DDR_CLK_AVSS (AA20)

=PP2V5_PWRON_RAM

R3700 1K 1% 1/16W MF 402

R3701 1K 1% 1/16W MF 402

PP1V25_PWRON_RAM_VREF_NB VOLTAGE=1.25V

C3730 0.1UF 20% 10V CERM 402

C3746 0.1UF 20% 10V CERM 402

C3747 0.1UF 20% 10V CERM 402

C3748 0.1UF 20% 10V CERM 402

MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

=PP2V5_PWRON_RAM

C3700 C3701 C3702 C3703 C3704 C3705 C3706 C3707 C3708 C3709 C3710 C3711 C3712 C3713 C3714 C3731 C3732 C3733 C3734 C3735 C3736 C3737 — 0.1UF 20% 10V CERM 402

C3715 C3716 C3717 C3718 C3719 C3720 C3721 C3722 C3724 C3725 C3726 C3727 C3728 C3729 C3743 C3742 C3740 C3739 C3738 — 0.1UF 20% 10V CERM 402

MASTER: GILA

LAST MODIFIED: APR 12, 04

U3LITE MEMORY

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6482	I

SCALE	SHT
NONE	37 OF 103

ALL R PACKS ARE 1/16W 5%

38 37	RAM_DQ_R<7>	RP3836	4	5	22	RAM_DQ<7>	38 40 44
38 37	RAM_DQ_R<2>	RP3836	1	8	22	RAM_DQ<2>	38 40 44
38 37	RAM_DQ_R<0>	RP3836	3	6	22	RAM_DQ<0>	38 40 44
38 37	RAM_DQ_R<3>	RP3836	2	7	22	RAM_DQ<3>	38 40 44
38 37	RAM_DQ_R<1>	RP3816	1	8	22	RAM_DQ<1>	38 40 44
38 37	RAM_DQ_R<4>	RP3816	2	7	22	RAM_DQ<4>	38 40 44
38 37	RAM_DQ_R<6>	RP3816	4	5	22	RAM_DQ<6>	38 40 44
38 37	RAM_DQ_R<5>	RP3816	3	6	22	RAM_DQ<5>	38 40 44
38 37	RAM_DQ_R<9>	RP3835	4	5	22	RAM_DQ<9>	38 40 44
38 37	RAM_DQ_R<10>	RP3801	1	8	22	RAM_DQ<10>	38 40 44
38 37	RAM_DQ_R<11>	RP3801	3	6	22	RAM_DQ<11>	38 40 44
38 37	RAM_DQ_R<14>	RP3801	4	5	22	RAM_DQ<14>	38 40 44
38 37	RAM_DQ_R<12>	RP3835	2	7	22	RAM_DQ<12>	38 40 44
38 37	RAM_DQ_R<13>	RP3801	2	7	22	RAM_DQ<13>	38 40 44
38 37	RAM_DQ_R<15>	RP3835	1	8	22	RAM_DQ<15>	38 40 44
38 37	RAM_DQ_R<8>	RP3835	3	6	22	RAM_DQ<8>	38 40 44
38 37	RAM_DQ_R<17>	RP3822	1	8	22	RAM_DQ<17>	38 40 44
38 37	RAM_DQ_R<22>	RP3822	4	5	22	RAM_DQ<22>	38 40 44
38 37	RAM_DQ_R<19>	RP3822	2	7	22	RAM_DQ<19>	38 40 44
38 37	RAM_DQ_R<18>	RP3822	3	6	22	RAM_DQ<18>	38 40 44
38 37	RAM_DQ_R<20>	RP3823	3	6	22	RAM_DQ<20>	38 40 44
38 37	RAM_DQ_R<16>	RP3823	4	5	22	RAM_DQ<16>	38 40 44
38 37	RAM_DQ_R<21>	RP3823	2	7	22	RAM_DQ<21>	38 40 44
38 37	RAM_DQ_R<23>	RP3823	1	8	22	RAM_DQ<23>	38 40 44
38 37	RAM_DQ_R<30>	RP3808	3	6	22	RAM_DQ<30>	38 40 44
38 37	RAM_DQ_R<26>	RP3824	2	7	22	RAM_DQ<26>	38 40 44
38 37	RAM_DQ_R<24>	RP3808	1	8	22	RAM_DQ<24>	38 40 44
38 37	RAM_DQ_R<27>	RP3824	1	8	22	RAM_DQ<27>	38 40 44
38 37	RAM_DQ_R<28>	RP3808	4	5	22	RAM_DQ<28>	38 40 44
38 37	RAM_DQ_R<31>	RP3808	2	7	22	RAM_DQ<31>	38 40 44
38 37	RAM_DQ_R<29>	RP3824	4	5	22	RAM_DQ<29>	38 40 44
38 37	RAM_DQ_R<25>	RP3824	3	6	22	RAM_DQ<25>	38 40 44
38 37	RAM_DQ_R<32>	RP3826	4	5	22	RAM_DQ<32>	38 40 44
38 37	RAM_DQ_R<35>	RP3807	2	7	22	RAM_DQ<35>	38 40 44
38 37	RAM_DQ_R<38>	RP3826	2	7	22	RAM_DQ<38>	38 40 44
38 37	RAM_DQ_R<37>	RP3807	4	5	22	RAM_DQ<37>	38 40 44
38 37	RAM_DQ_R<39>	RP3826	3	6	22	RAM_DQ<39>	38 40 44
38 37	RAM_DQ_R<33>	RP3807	3	6	22	RAM_DQ<33>	38 40 44
38 37	RAM_DQ_R<34>	RP3807	1	8	22	RAM_DQ<34>	38 40 44
38 37	RAM_DQ_R<36>	RP3826	1	8	22	RAM_DQ<36>	38 40 44
38 37	RAM_DQ_R<47>	RP3811	2	7	22	RAM_DQ<47>	38 40 44
38 37	RAM_DQ_R<46>	RP3811	1	8	22	RAM_DQ<46>	38 40 44
38 37	RAM_DQ_R<43>	RP3814	2	7	22	RAM_DQ<43>	38 40 44
38 37	RAM_DQ_R<41>	RP3814	1	8	22	RAM_DQ<41>	38 40 44
38 37	RAM_DQ_R<45>	RP3811	4	5	22	RAM_DQ<45>	38 40 44
38 37	RAM_DQ_R<42>	RP3814	3	6	22	RAM_DQ<42>	38 40 44
38 37	RAM_DQ_R<40>	RP3814	4	5	22	RAM_DQ<40>	38 40 44
38 37	RAM_DQ_R<44>	RP3811	3	6	22	RAM_DQ<44>	38 40 44
38 37	RAM_DQ_R<51>	RP3830	4	5	22	RAM_DQ<51>	38 40 44
38 37	RAM_DQ_R<50>	RP3830	2	7	22	RAM_DQ<50>	38 40 44
38 37	RAM_DQ_R<49>	RP3830	1	8	22	RAM_DQ<49>	38 40 44
38 37	RAM_DQ_R<48>	RP3830	3	6	22	RAM_DQ<48>	38 40 44
38 37	RAM_DQ_R<52>	RP3812	2	7	22	RAM_DQ<52>	38 40 44
38 37	RAM_DQ_R<53>	RP3812	3	6	22	RAM_DQ<53>	38 40 44
38 37	RAM_DQ_R<54>	RP3812	4	5	22	RAM_DQ<54>	38 40 44
38 37	RAM_DQ_R<55>	RP3812	1	8	22	RAM_DQ<55>	38 40 44
38 37	RAM_DQ_R<56>	RP3813	1	8	22	RAM_DQ<56>	38 40 44
38 37	RAM_DQ_R<63>	RP3831	4	5	22	RAM_DQ<63>	38 40 44
38 37	RAM_DQ_R<59>	RP3813	2	7	22	RAM_DQ<59>	38 40 44
38 37	RAM_DQ_R<61>	RP3831	2	7	22	RAM_DQ<61>	38 40 44
38 37	RAM_DQ_R<57>	RP3831	3	6	22	RAM_DQ<57>	38 40 44
38 37	RAM_DQ_R<60>	RP3831	1	8	22	RAM_DQ<60>	38 40 44
38 37	RAM_DQ_R<58>	RP3813	3	6	22	RAM_DQ<58>	38 40 44
38 37	RAM_DQ_R<62>	RP3813	4	5	22	RAM_DQ<62>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_CKE_R<4>	RP3841	3	6	15	RAM_CKE<4>	38 40 45
38 37	RAM_CKE_R<5>	RP3841	4	5	15	RAM_CKE<5>	38 40 45
38 37	RAM_CKE_R<0>	RP3841	2	7	15	RAM_CKE<0>	38 40 44
38 37	RAM_CKE_R<1>	RP3841	1	8	15	RAM_CKE<1>	38 40 44
38 37	RAM_CS_L_R<8>	RP3842	1	8	15	RAM_CS_L<8>	38 40 45
38 37	RAM_CS_L_R<9>	RP3842	2	7	15	RAM_CS_L<9>	38 40 45
38 37	RAM_CS_L_R<1>	RP3842	3	6	15	RAM_CS_L<1>	38 40 44
38 37	RAM_CS_L_R<0>	RP3842	4	5	15	RAM_CS_L<0>	38 40 44

THE FOLLOWING IS A SWAPPABLE GROUP

38 37	RAM_A_R<11>	RP3832	3	6	15	RAM_A<11>	38 40 44
38 37	RAM_A_R<1>	RP3832	4	5	15	RAM_A<1>	38 40 44
38 37	RAM_A_R<10>	RP3832	2	7	15	RAM_A<10>	38 40 45
38 37	RAM_WE_L_R	RP3800	4	5	15	RAM_WE_L	38 40 45
38 37	RAM_A_R<4>	RP3833	3	6	15	RAM_A<4>	38 40 44
38 37	RAM_A_R<6>	RP3833	2	7	15	RAM_A<6>	38 40 44
38 37	RAM_A_R<7>	RP3833	1	8	15	RAM_A<7>	38 40 44
		RP3834	1	8	15		
38 37	RAM_A_R<12>	RP3800	3	6	15	RAM_A<12>	38 40 44
38 37	RAM_A_R<2>	RP3834	2	7	15	RAM_A<2>	38 40 44
38 37	RAM_A_R<0>	RP3833	4	5	15	RAM_A<0>	38 40 44
38 37	RAM_A_R<5>	RP3832	1	8	15	RAM_A<5>	38 40 44
38 37	RAM_A_R<13>	RP3800	2	7	15	RAM_A<13>	38 40 44
38 37	RAM_A_R<3>	RP3800	1	8	15	RAM_A<3>	38 40 44
38 37	RAM_CAS_L_R	RP3804	1	8	15	RAM_CAS_L	38 40 45
38 37	RAM_BA_R<0>	RP3804	4	5	15	RAM_BA<0>	38 40 45
38 37	RAM_BA_R<1>	RP3804	2	7	15	RAM_BA<1>	38 40 45
38 37	RAM_RAS_L_R	RP3804	3	6	15	RAM_RAS_L	38 40 45
38 37	RAM_A_R<9>	RP3834	3	6	15	RAM_A<9>	38 40 44
38 37	RAM_A_R<8>	RP3834	4	5	15	RAM_A<8>	38 40 44

38 37	RAM_DQ_R<68>	RP3818	2	7	22	RAM_DQ<68>	38 40 45
38 37	RAM_DQ_R<65>	RP3805	2	7	22	RAM_DQ<65>	38 40 45
38 37	RAM_DQ_R<70>	RP3818	4	5	22	RAM_DQ<70>	38 40 45
38 37	RAM_DQ_R<66>	RP3805	1	8	22	RAM_DQ<66>	38 40 45
38 37	RAM_DQ_R<71>	RP3818	3	6	22	RAM_DQ<71>	38 40 45
38 37	RAM_DQ_R<64>	RP3805	4	5	22	RAM_DQ<64>	38 40 45
38 37	RAM_DQ_R<67>	RP3805	3	6	22	RAM_DQ<67>	38 40 45
38 37	RAM_DQ_R<69>	RP3818	1	8	22	RAM_DQ<69>	38 40 45
38 37	RAM_DQ_R<74>	RP3817	3	6	22	RAM_DQ<74>	38 40 45
38 37	RAM_DQ_R<73>	RP3802	4	5	22	RAM_DQ<73>	38 40 45
38 37	RAM_DQ_R<72>	RP3817	2	7	22	RAM_DQ<72>	38 40 45
38 37	RAM_DQ_R<75>	RP3817	4	5	22	RAM_DQ<75>	38 40 45
38 37	RAM_DQ_R<78>	RP3802	2	7	22	RAM_DQ<78>	38 40 45
38 37	RAM_DQ_R<79>	RP3817	1	8	22	RAM_DQ<79>	38 40 45
38 37	RAM_DQ_R<77>	RP3802	1	8	22	RAM_DQ<77>	38 40 45
38 37	RAM_DQ_R<76>	RP3802	3	6	22	RAM_DQ<76>	38 40 45
38 37	RAM_DQ_R<87>	RP3806	2	7	22	RAM_DQ<87>	38 40 45
38 37	RAM_DQ_R<86>	RP3821	1	8	22	RAM_DQ<86>	38 40 45
38 37	RAM_DQ_R<81>	RP3821	4	5	22	RAM_DQ<81>	38 40 45
38 37	RAM_DQ_R<80>	RP3821	2	7	22	RAM_DQ<80>	38 40 45
38 37	RAM_DQ_R<84>	RP3806	1	8	22	RAM_DQ<84>	38 40 45
38 37	RAM_DQ_R<85>	RP3806	3	6	22	RAM_DQ<85>	38 40 45
38 37	RAM_DQ_R<83>	RP3821	3	6	22	RAM_DQ<83>	38 40 45
38 37	RAM_DQ_R<82>	RP3806	4	5	22	RAM_DQ<82>	38 40 45
38 37	RAM_DQ_R<91>	RP3819	3	6	22	RAM_DQ<91>	38 40 45
38 37	RAM_DQ_R<93>	RP3819	1	8	22	RAM_DQ<93>	38 40 45
38 37	RAM_DQ_R<94>	RP3803	2	7	22	RAM_DQ<94>	38 40 45
38 37	RAM_DQ_R<90>	RP3819	4	5	22	RAM_DQ<90>	38 40 45
38 37	RAM_DQ_R<88>	RP3803	4	5	22	RAM_DQ<88>	38 40 45
38 37	RAM_DQ_R<89>	RP3819	2	7	22	RAM_DQ<89>	38 40 45
38 37	RAM_DQ_R<92>	RP3803	3	6	22	RAM_DQ<92>	38 40 45
38 37	RAM_DQ_R<95>	RP3803	1	8	22	RAM_DQ<95>	38 40 45
38 37	RAM_DQ_R<98>	RP3820	4	5	22	RAM_DQ<98>	38 40 45
38 37	RAM_DQ_R<96>	RP3820	3	6	22	RAM_DQ<96>	38 40 45
38 37	RAM_DQ_R<103>	RP3820	2	7	22	RAM_DQ<103>	38 40 45
38 37	RAM_DQ_R<97>	RP3820	1	8	22	RAM_DQ<97>	38 40 45
38 37	RAM_DQ_R<100>	RP3825	2	7	22	RAM_DQ<100>	38 40 45
38 37	RAM_DQ_R<99>	RP3825	3	6	22	RAM_DQ<99>	38 40 45
38 37	RAM_DQ_R<102>	RP3825	1	8	22	RAM_DQ<102>	38 40 45
38 37	RAM_DQ_R<101>	RP3825	4	5	22	RAM_DQ<101>	38 40 45
38 37	RAM_DQ_R<111>	RP3809	1	8	22	RAM_DQ<111>	38 40 45
38 37	RAM_DQ_R<106>	RP3809	3	6	22	RAM_DQ<106>	38 40 45
38 37	RAM_DQ_R<105>	RP3809	2	7	22	RAM_DQ<105>	38 40 45
38 37	RAM_DQ_R<108>	RP3829	2	7	22	RAM_DQ<108>	38 40 45
38 37	RAM_DQ_R<107>	RP3829	4	5	22	RAM_DQ<107>	38 40 45
38 37	RAM_DQ_R<110>	RP3829	3	6	22	RAM_DQ<110>	38 40 45
38 37	RAM_DQ_R<104>	RP3809	4	5	22	RAM_DQ<104>	38 40 45
38 37	RAM_DQ_R<109>	RP3829	1	8	22	RAM_DQ<109>	38 40 45
38 37	RAM_DQ_R<119>	RP3828	4	5	22	RAM_DQ<119>	38 40 45
38 37	RAM_DQ_R<112>	RP3815	2	7	22	RAM_DQ<112>	38 40 45
38 37	RAM_DQ_R<117>	RP3815	1	8	22	RAM_DQ<117>	38 40 45
38 37	RAM_DQ_R<118>	RP3828	1	8	22	RAM_DQ<118>	38 40 45
38 37	RAM_DQ_R<113>	RP3815	3	6	22	RAM_DQ<113>	38 40 45
38 37	RAM_DQ_R<115>	RP3828	3	6	22	RAM_DQ<115>	38 40 45
38 37	RAM_DQ_R<116>	RP3828	2	7	22	RAM_DQ<116>	38 40 45
38 37	RAM_DQ_R<114>	RP3815	4	5	22	RAM_DQ<114>	38 40 45
38 37	RAM_DQ_R<121>	RP3827	3	6	22	RAM_DQ<121>	38 40 45
38 37	RAM_DQ_R<124>	RP3827	2	7	22	RAM_DQ<124>	38 40 45
38 37	RAM_DQ_R<120>	RP3827	4	5	22	RAM_DQ<120>	38 40 45
38 37	RAM_DQ_R<123>	RP3810	2	7	22	RAM_DQ<123>	38 40 45
38 37	RAM_DQ_R<125>	RP3827	1	8	22	RAM_DQ<125>	38 40 45
38 37	RAM_DQ_R<122>	RP3810	4	5	22	RAM_DQ<122>	38 40 45
38 37	RAM_DQ_R<126>	RP3810	1	8	22	RAM_DQ<126>	38 40 45
38 37	RAM_DQ_R<127>	RP3810	3	6	22	RAM_DQ<127>	38 40 45

THE FOLLOWING ARE 0402 5% RESISTORS

38 37	RAM_CLK_A_P_R	R3816	1	2	15	RAM_CLK_A_P	38 40
38 37	RAM_CLK_A_N_R	R3817	1	2	15	RAM_CLK_A_N	38 40
38 37	RAM_CLK_B_P_R	R3818	1	2	15	RAM_CLK_B_P	38 40
38 37	RAM_CLK_B_N_R	R3819	1	2	15	RAM_CLK_B_N	38 40
38 37	RAM_CLK_C_P_R	R3820	1	2	15	RAM_CLK_C_P	38 40
38 37	RAM_CLK_C_N_R	R3821	1	2	15	RAM_CLK_C_N	38 40
38 37	RAM_CLK_D_P_R	R3822	1	2	15	RAM_CLK_D_P	38 40
38 37	RAM_CLK_D_N_R	R3823	1	2	15	RAM_CLK_D_N	38 40
38 37	RAM_CLK_E_P_R	R3824	1	2	15	RAM_CLK_E_P	38 40
38 37	RAM_CLK_E_N_R	R3825	1	2	15	RAM_CLK_E_N	38 40
38 37	RAM_CLK_F_P_R	R3826	1	2	15	RAM_CLK_F_P	38 40
38 37	RAM_CLK_F_N_R	R3827	1	2	15	RAM_CLK_F_N	38 40

38 37	RAM_DQS_R<0>	R3800	1	2	15	RAM_DQS<0>	38 40 44
38 37	RAM_DQS_R<1>	R3801	1	2	15	RAM_DQS<1>	38 40 44
38 37	RAM_DQS_R<2>	R3802	1	2	15	RAM_DQS<2>	38 40 44
38 37	RAM_DQS_R<3>	R3803	1	2	15	RAM_DQS<3>	38 40 44
38 37	RAM_DQS_R<4>	R3804	1	2	15	RAM_DQS<4>	38 40 44
38 37	RAM_DQS_R<5>	R3805	1	2	15	RAM_DQS<5>	38 40 44
38 37	RAM_DQS_R<6>	R3806	1	2	15	RAM_DQS<6>	38 40 44
38 37	RAM_DQS_R<7>	R3807	1	2	15	RAM_DQS<7>	38 40 44
38 37	RAM_DQS_R<8>	R3808	1	2	15	RAM_DQS<8>	38 40 45
38 37	RAM_DQS_R<9>	R3809	1	2	15	RAM_DQS<9>	38 40 45
38 37	RAM_DQS_R<10>	R3810	1	2	15	RAM_DQS<10>	38 40 45
38 37	RAM_DQS_R<11>	R3811	1	2	15	RAM_DQS<11>	38 40 45
38 37	RAM_DQS_R<12>	R3812	1	2	15	RAM_DQS<12>	38 40 45
38 37	RAM_DQS_R<13>	R3813	1	2	15	RAM_DQS<13>	38 40 45
38 37	RAM_DQS_R<14>	R3814	1	2	15	RAM_DQS<14>	38 40 45
38 37	RAM_DQS_R<15>	R3815	1	2	15	RAM_DQS<15>	38 40 45

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
38 37 RAM_CLK_A_P_R			RAM_CLK	RAM_CLK_A_R	2006
38 37 RAM_CLK_A_N_R			RAM_CLK	RAM_CLK_A_R	2007
38 37 RAM_CLK_B_P_R			RAM_CLK	RAM_CLK_B_R	2008
38 37 RAM_CLK_B_N_R			RAM_CLK	RAM_CLK_B_R	2009
38 37 RAM_CLK_C_P_R			RAM_CLK	RAM_CLK_C_R	2010
38 37 RAM_CLK_C_N_R			RAM_CLK	RAM_CLK_C_R	2011
38 37 RAM_CLK_D_P_R			RAM_CLK	RAM_CLK_D_R	2012
38 37 RAM_CLK_D_N_R			RAM_CLK	RAM_CLK_D_R	2013
38 37 RAM_CLK_E_P_R			RAM_CLK	RAM_CLK_E_R	2014
38 37 RAM_CLK_E_N_R			RAM_CLK	RAM_CLK_E_R	2015
38 37 RAM_CLK_F_P_R			RAM_CLK	RAM_CLK_F_R	2016
38 37 RAM_CLK_F_N_R			RAM_CLK	RAM_CLK_F_R	2017
40 38 RAM_CLK_A_P	RAM_CLK0		RAM_CLK	RAM_CLK_A	2018
40 38 RAM_CLK_A_N	RAM_CLK0		RAM_CLK	RAM_CLK_A	2019
40 38 RAM_CLK_B_P	RAM_CLK0		RAM_CLK	RAM_CLK_B	2020
40 38 RAM_CLK_B_N	RAM_CLK0		RAM_CLK	RAM_CLK_B	2021
40 38 RAM_CLK_C_P	RAM_CLK0		RAM_CLK	RAM_CLK_C	2022
40 38 RAM_CLK_C_N	RAM_CLK0		RAM_CLK	RAM_CLK_C	2023
40 38 RAM_CLK_D_P	RAM_CLK1		RAM_CLK	RAM_CLK_D	2024
40 38 RAM_CLK_D_N	RAM_CLK1		RAM_CLK	RAM_CLK_D	2025
40 38 RAM_CLK_E_P	RAM_CLK1		RAM_CLK	RAM_CLK_E	2026
40 38 RAM_CLK_E_N	RAM_CLK1		RAM_CLK	RAM_CLK_E	2027
40 38 RAM_CLK_F_P	RAM_CLK1		RAM_CLK	RAM_CLK_F	2028
40 38 RAM_CLK_F_N	RAM_CLK1		RAM_CLK	RAM_CLK_F	2029
38 37 RAM_CKE_R<1..0>			RAM_CAD		2030
38 37 RAM_CKE_R<5..4>			RAM_CAD		2031
44 40 38 RAM_CKE<0>	RAM_CKECS0		RAM_CAD		2032
44 40 38 RAM_CKE<1>	RAM_CKECS0		RAM_CAD		2033
45 40 38 RAM_CKE<4>	RAM_CKECS1		RAM_CAD		2034
45 40 38 RAM_CKE<5>	RAM_CKECS1		RAM_CAD		2035
38 37 RAM_CS_L_R<1..0>			RAM_CAD		2036
38 37 RAM_CS_L_R<9..8>			RAM_CAD		2041
44 40 38 RAM_CS_L<0>	RAM_CKECS0		RAM_CAD		2042
44 40 38 RAM_CS_L<1>	RAM_CKECS0		RAM_CAD		2043
45 40 38 RAM_CS_L<8>	RAM_CKECS1		RAM_CAD		2044
45 40 38 RAM_CS_L<9>	RAM_CKECS1		RAM_CAD		2045
38 37 RAM_DQS_R<15..0>			RAM_CAD		2046
38 37 RAM_DQ_R<127..0>			RAM_CAD		2047
45 44 40 38 RAM_DQ<127..0>			RAM_CAD		2048
44 40 38 RAM_DQS<0>	RAM_DQS0		RAM_CAD		2049
44 40 38 RAM_DQ<7..0>	RAM_DQS0		RAM_CAD		2050
44 40 38 RAM_DQS<1>	RAM_DQS1		RAM_CAD		2051
44 40 38 RAM_DQ<15..8>	RAM_DQS1		RAM_CAD		2052
44 40 38 RAM_DQS<2>	RAM_DQS2		RAM_CAD		2053
44 40 38 RAM_DQ<23..16>	RAM_DQS2		RAM_CAD		2054
44 40 38 RAM_DQS<3>	RAM_DQS3		RAM_CAD		2055
44 40 38 RAM_DQ<31..24>	RAM_DQS3		RAM_CAD		2056
44 40 38 RAM_DQS<4>	RAM_DQS4		RAM_CAD		2057
44 40 38 RAM_DQ<39..32>	RAM_DQS4		RAM_CAD		2058
44 40 38 RAM_DQS<5>	RAM_DQS5		RAM_CAD		2059
44 40 38 RAM_DQ<47..40>	RAM_DQS5		RAM_CAD		2060
44 40 38 RAM_DQS<6>	RAM_DQS6		RAM_CAD		2061
44 40 38 RAM_DQ<55..48>	RAM_DQS6		RAM_CAD		2062
44 40 38 RAM_DQS<7>	RAM_DQS7		RAM_CAD		2063
44 40 38 RAM_DQ<63..56>	RAM_DQS7		RAM_CAD		2064
45 40 38 RAM_DQS<8>	RAM_DQS8		RAM_CAD		2065
45 40 38 RAM_DQ<71..64>	RAM_DQS8		RAM_CAD		2067
45 40 38 RAM_DQS<9>	RAM_DQS9		RAM_CAD		2066
45 40 38 RAM_DQ<79..72>	RAM_DQS9		RAM_CAD		2068
45 40 38 RAM_DQS<10>	RAM_DQS10		RAM_CAD		2070
45 40 38 RAM_DQ<87..80>	RAM_DQS10		RAM_CAD		2069
45 40 38 RAM_DQS<11>	RAM_DQS11		RAM_CAD		2072
45 40 38 RAM_DQ<95..88>	RAM_DQS11		RAM_CAD		2071
45 40 38 RAM_DQS<12>	RAM_DQS12		RAM_CAD		2073
45 40 38 RAM_DQ<103..96>	RAM_DQS12		RAM_CAD		2074
45 40 38 RAM_DQS<13>	RAM_DQS13		RAM_CAD		2075
45 40 38 RAM_DQ<111..104>	RAM_DQS13		RAM_CAD		2077
45 40 38 RAM_DQS<14>	RAM_DQS14		RAM_CAD		2076
45 40 38 RAM_DQ<119..112>	RAM_DQS14		RAM_CAD		2078
45 40 38 RAM_DQS<15>	RAM_DQS15		RAM_CAD		2080
45 40 38 RAM_DQ<127..120>	RAM_DQS15		RAM_CAD		2079
38 37 RAM_A_R<13..0>			RAM_CAD		2033
38 37 RAM_BA_R<1..0>			RAM_CAD		2046
38 37 RAM_RAS_L_R			RAM_CAD		2047
38 37 RAM_CAS_L_R			RAM_CAD		2048
38 37 RAM_WE_L_R			RAM_CAD		2049
45 44 40 38 RAM_A<13..0>	RAM_A_CTL		RAM_CAD		2000
45 40 38 RAM_BA<1..0>	RAM_A_CTL		RAM_CAD		2004
45 40 38 RAM_RAS_L	RAM_A_CTL		RAM_CAD		2001
45 40 38 RAM_CAS_L	RAM_A_CTL		RAM_CAD		2002
45 40 38 RAM_WE_L	RAM_A_CTL		RAM_CAD		2003

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

SERIES TERM

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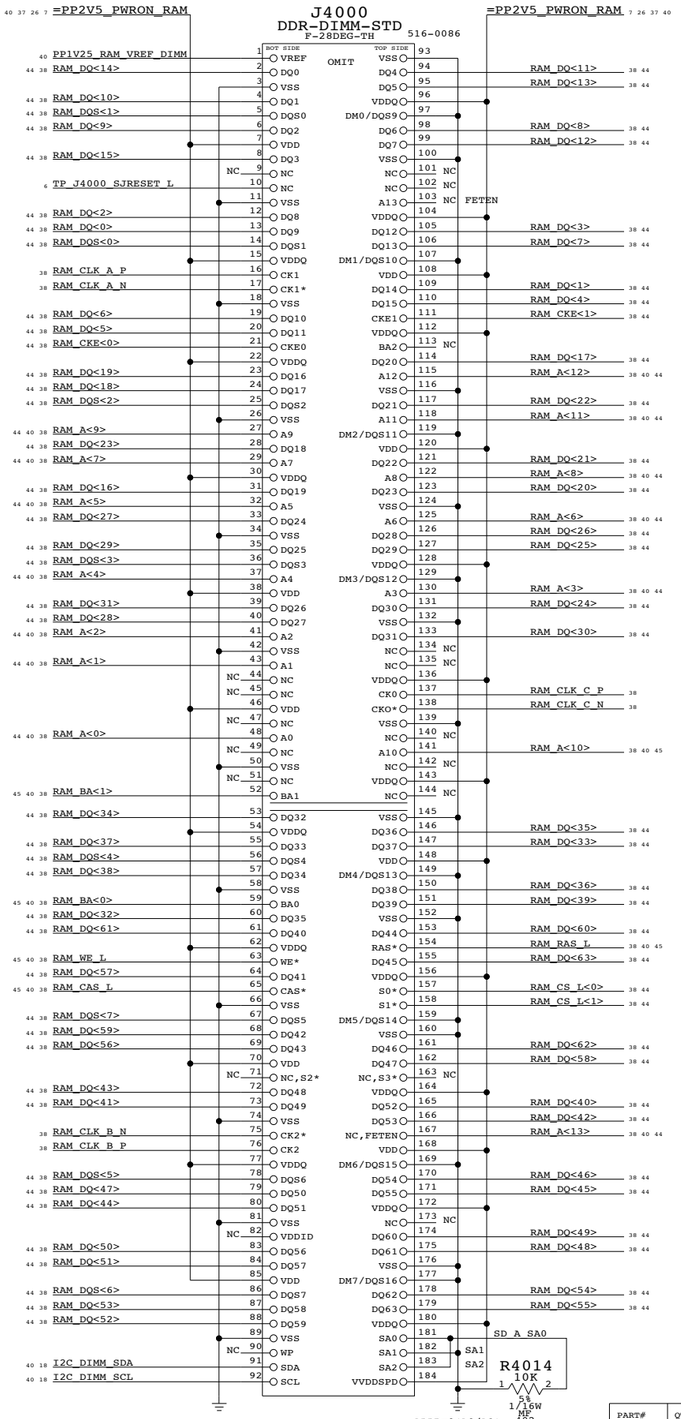
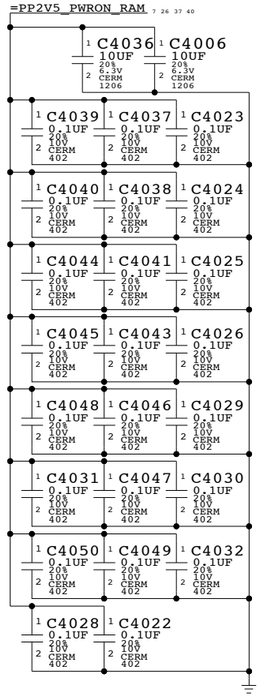
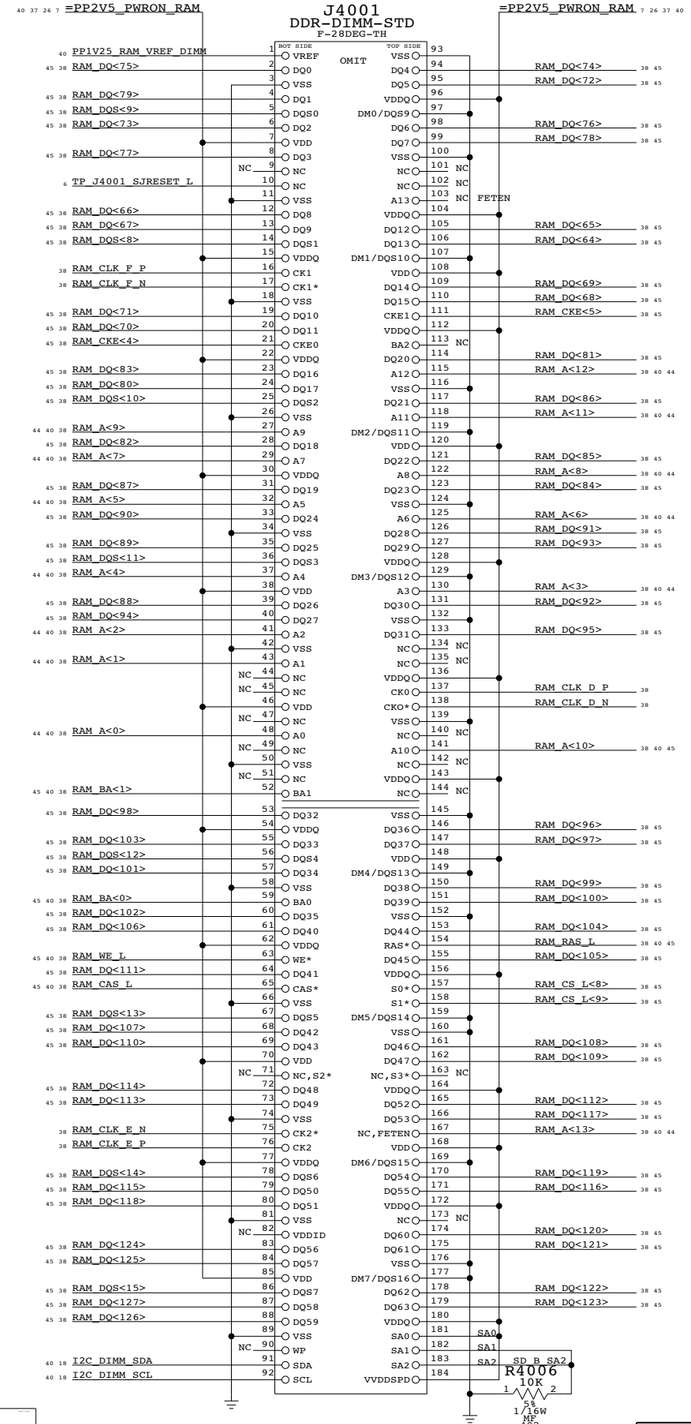
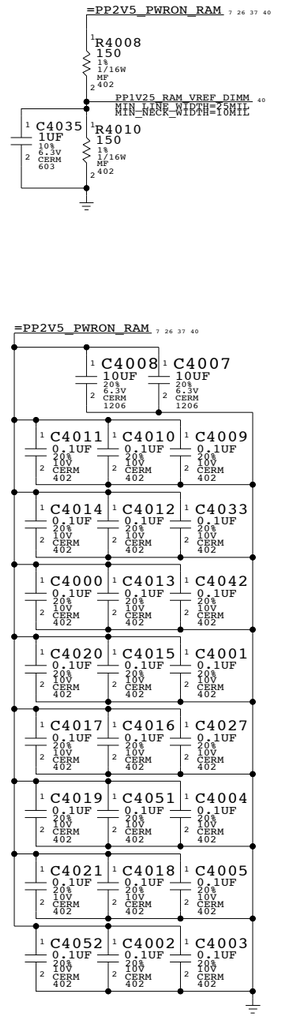
SCALE NONE | SHT 38 OF 103



PIN 82:
NC: VDD & VDDQ ARE THE SAME
GND: VDD & VDDQ ARE DIFFERENT







PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
516-0086	2	CONN,DDR DIMM 30 DEG	J4000,J4001	17_INCH_LCD	CRITICAL
516-0087	2	CONN,DDR DIMM REVERSE 30 DEG	J4000,J4001	20_INCH_LCD	CRITICAL

VVR'S ADJACENT TO V'S OR G'S
VVR'S ADJACENT TO G'S FORBIDDEN

DIMMS

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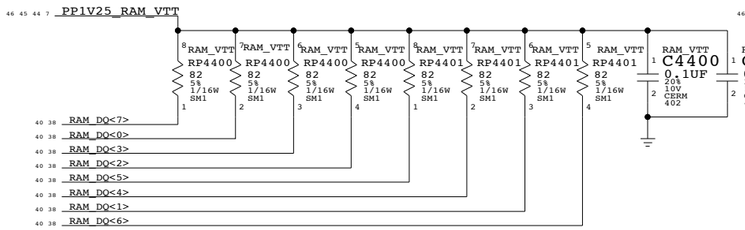
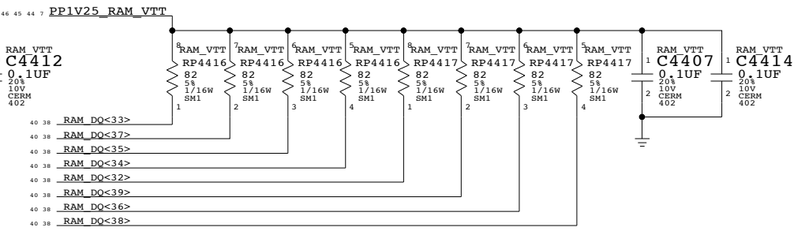
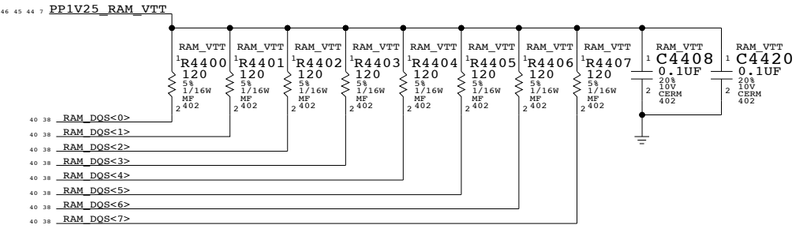
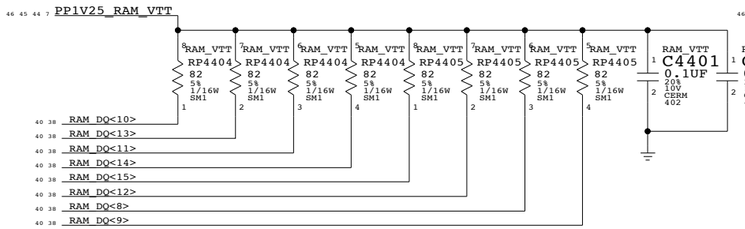
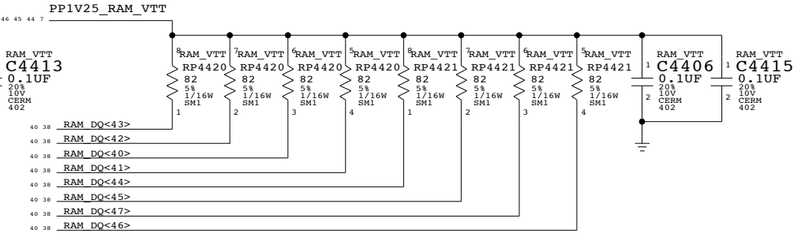
SCALE: NONE	SHT 40 OF 103	

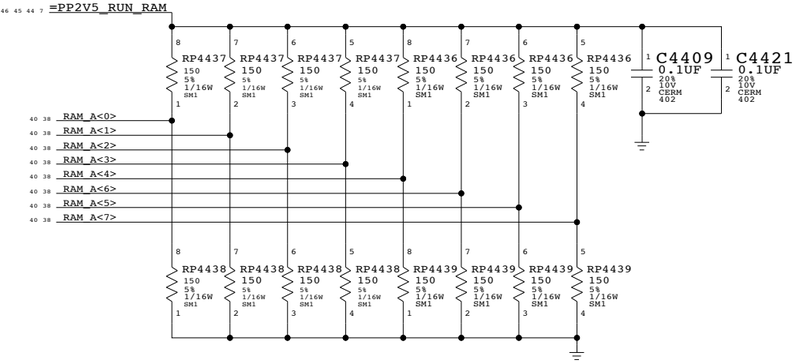


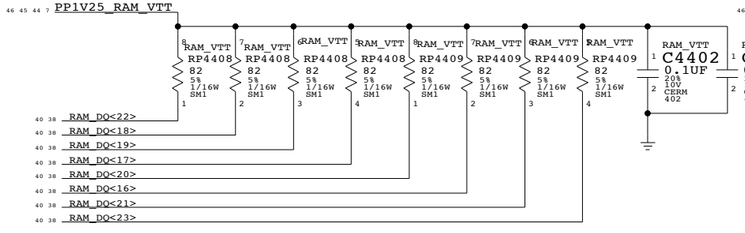


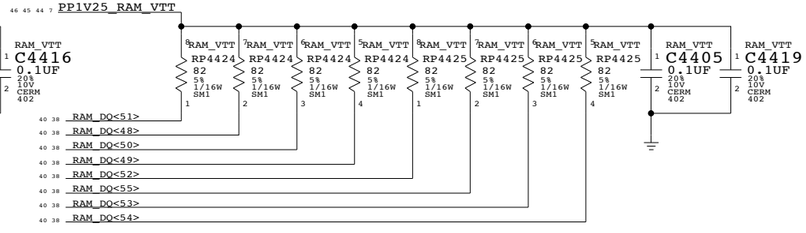


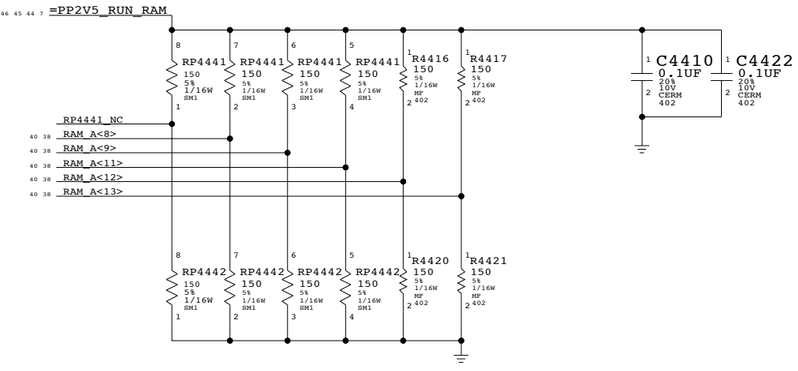


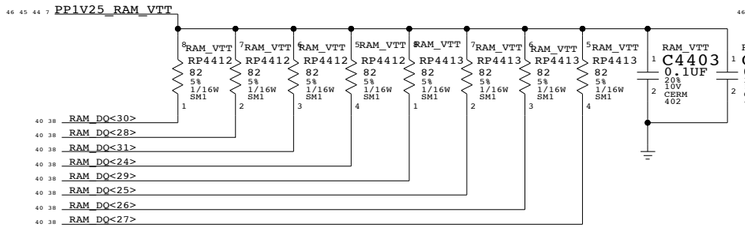


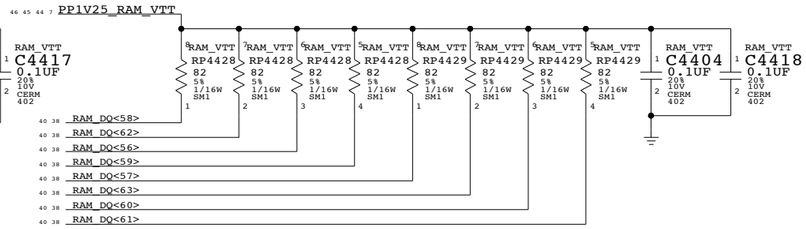


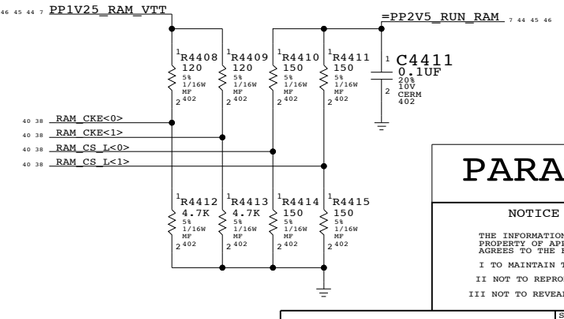












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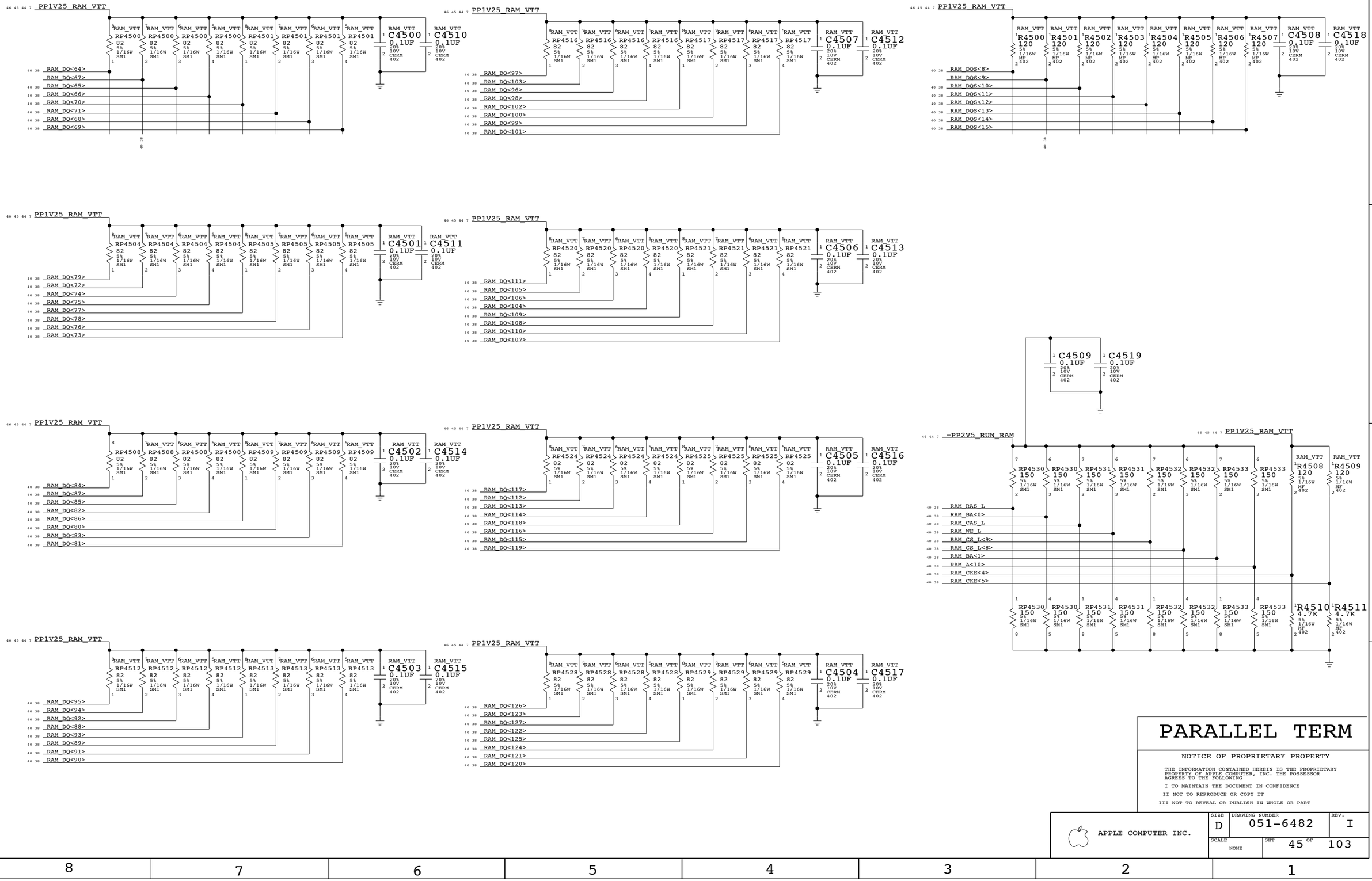
PP1V25_RAM_VTT
RP4500 RP4501 RP4502 RP4503 RP4504 RP4505 RP4506 RP4507 RP4508 RP4509 RP4510 RP4511 RP4512 RP4513 RP4516 RP4517 RP4520 RP4521 RP4524 RP4525 RP4528 RP4529
82 5% 1/16W SM1
120 5% 1/16W MF 402
150 5% 1/16W SM1
4.7K 5% 1/16W MF 402
C4500 C4501 C4502 C4503 C4504 C4505 C4506 C4507 C4508 C4509 C4510 C4511 C4512 C4513 C4514 C4515 C4516 C4517 C4518 C4519
0.1UF 20% 10V CERM 402
RAM_DQ<64> RAM_DQ<67> RAM_DQ<65> RAM_DQ<66> RAM_DQ<70> RAM_DQ<71> RAM_DQ<68> RAM_DQ<69>
RAM_DQ<97> RAM_DQ<103> RAM_DQ<96> RAM_DQ<98> RAM_DQ<102> RAM_DQ<100> RAM_DQ<99> RAM_DQ<101>
RAM_DQS<8> RAM_DQS<9> RAM_DQS<10> RAM_DQS<11> RAM_DQS<12> RAM_DQS<13> RAM_DQS<14> RAM_DQS<15>
RAM_DQ<79> RAM_DQ<72> RAM_DQ<74> RAM_DQ<75> RAM_DQ<77> RAM_DQ<78> RAM_DQ<76> RAM_DQ<73>
RAM_DQ<111> RAM_DQ<105> RAM_DQ<106> RAM_DQ<104> RAM_DQ<109> RAM_DQ<108> RAM_DQ<110> RAM_DQ<107>
=PP2V5_RUN_RAM
RAM_RAS_L RAM_BA<0> RAM_CAS_L RAM_WE_L RAM_CS_L<9> RAM_CS_L<8> RAM_BA<1> RAM_A<10> RAM_CKE<4> RAM_CKE<5>
RAM_DQ<84> RAM_DQ<87> RAM_DQ<85> RAM_DQ<82> RAM_DQ<86> RAM_DQ<80> RAM_DQ<83> RAM_DQ<81>
RAM_DQ<117> RAM_DQ<112> RAM_DQ<113> RAM_DQ<114> RAM_DQ<118> RAM_DQ<116> RAM_DQ<115> RAM_DQ<119>
RAM_DQ<95> RAM_DQ<94> RAM_DQ<92> RAM_DQ<88> RAM_DQ<93> RAM_DQ<89> RAM_DQ<91> RAM_DQ<90>
RAM_DQ<126> RAM_DQ<123> RAM_DQ<127> RAM_DQ<122> RAM_DQ<125> RAM_DQ<124> RAM_DQ<121> RAM_DQ<120>
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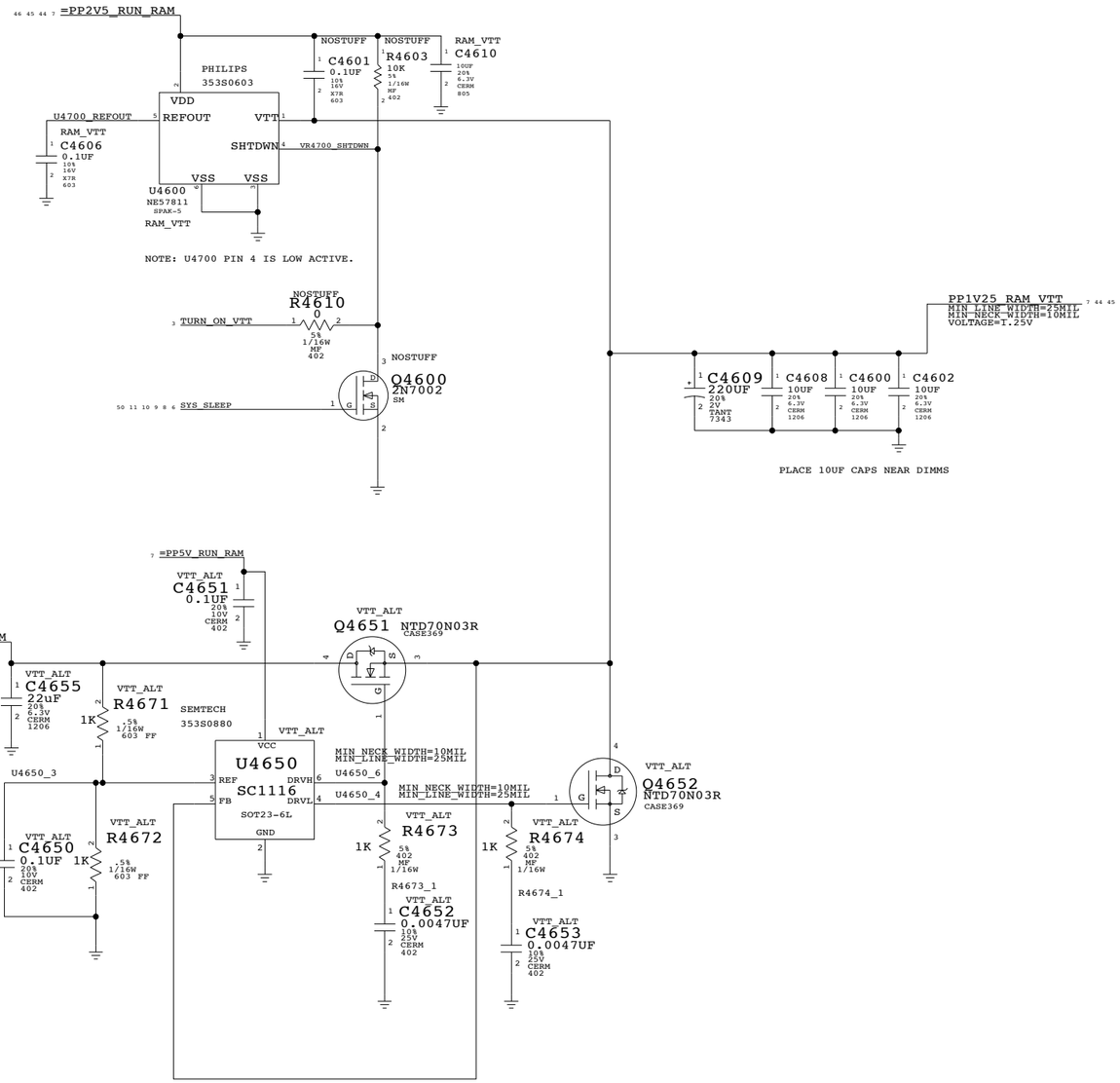

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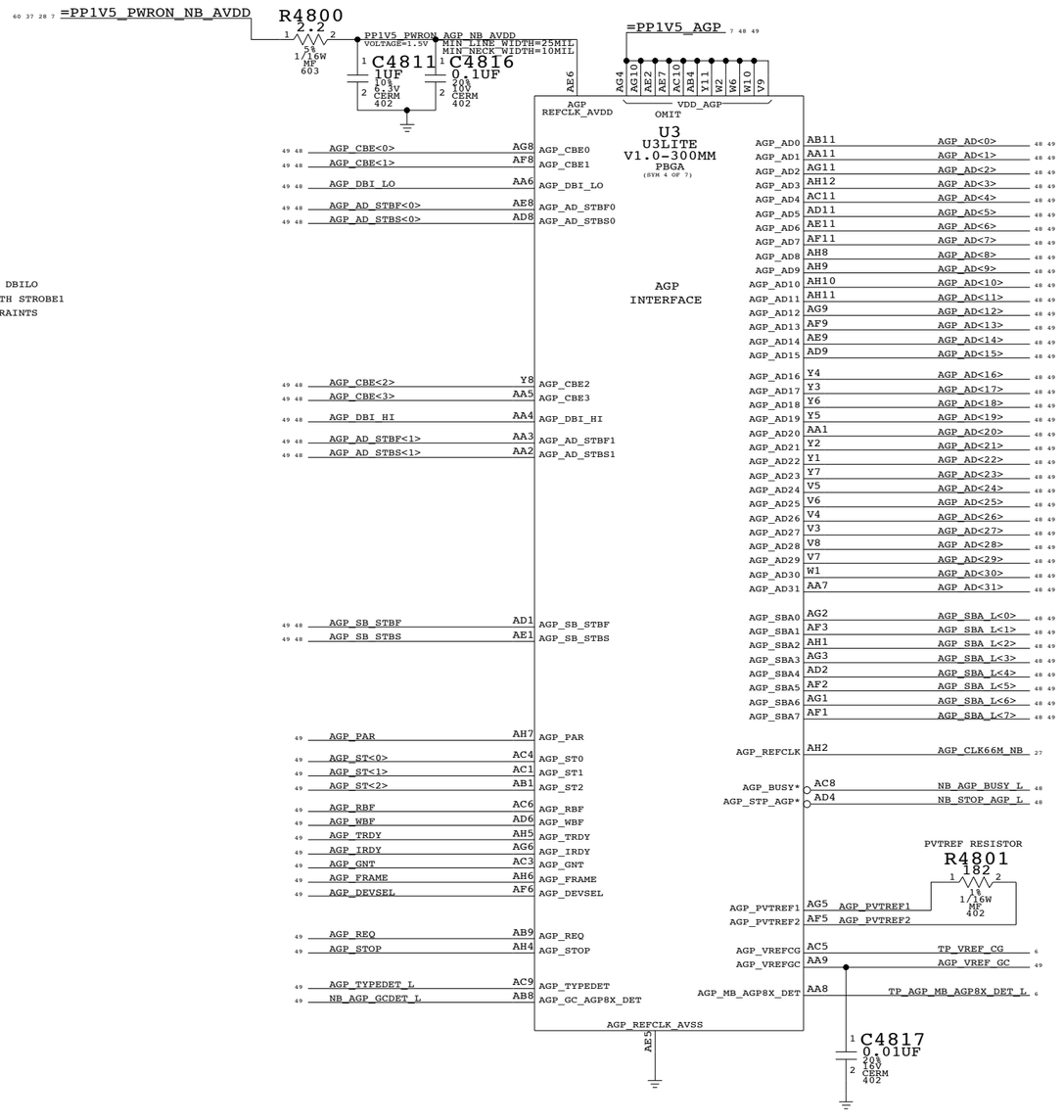
SCALE	SHT
NONE	46 OF 103



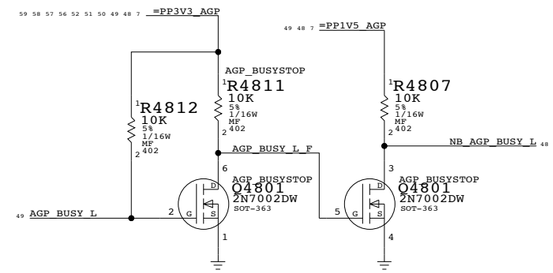
DBIHI AND DBILO
GROUPS WITH STROBE1
FOR CONSTRAINTS

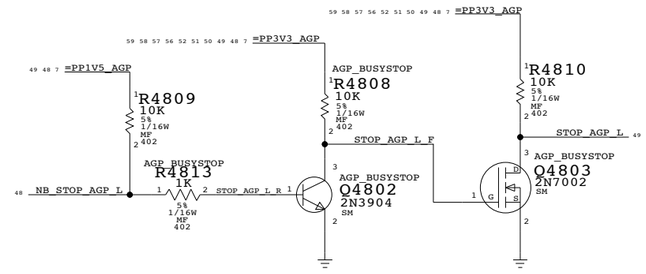
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
AGP_CBE<1..0>	AGP_AD_0	AGP_DATA		146
AGP_CBE<3..2>	AGP_AD_1	AGP_DATA		148
AGP_SB_STBF	AGP_SB_STBS	AGP_STROBE	AGP_SB_STB	149
AGP_SB_STBS	AGP_SB_STBS	AGP_STROBE	AGP_SB_STB	150
AGP_AD_STBF<0>	AGP_AD_STB_0	AGP_STROBE	AGP_AD_STB0	151
AGP_AD_STBS<0>	AGP_AD_STB_0	AGP_STROBE	AGP_AD_STB0	152
AGP_AD_STBF<1>	AGP_AD_STB_1	AGP_STROBE	AGP_AD_STB1	153
AGP_AD_STBS<1>	AGP_AD_STB_1	AGP_STROBE	AGP_AD_STB1	154
AGP_DBI_LO	AGP_AD_1	AGP_DATA		155
AGP_DBI_HI	AGP_AD_1	AGP_DATA		156
AGP_AD<15..0>	AGP_AD_0	AGP_DATA		157
AGP_AD<31..16>	AGP_AD_1	AGP_DATA		158
AGP_SBA_L<7..0>	AGP_SBA	AGP_DATA		159

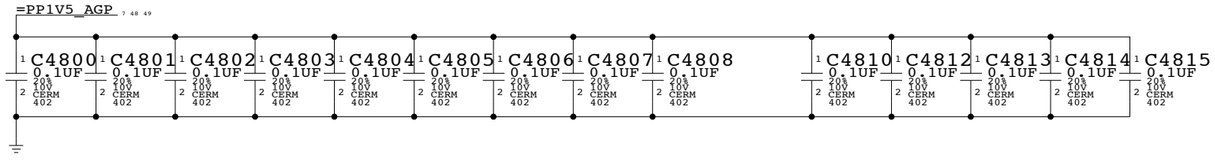
DBI_HI IS NOT A STROBE BUT SHARES THE SAME TOPOLOGY AS A STROBE

LEVEL SHIFTER FOR U3LITE

AGP BUSY AND STOP ARE NOT USED IN ALL DESIGNS







MASTER: GILA
LAST MODIFIED: APR 12, 04

U3LITE AGP

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 48 OF 103	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
338S0176	1	IC,NV18B,GRAPHIC CTRL,C1	U4900	NV18B
338S0175	1	IC,NV34,GRAPHIC CTRL,B1	U4900	NV34

U3LITE AGP I/O REFERENCE
(PLACE CLOSE TO GPU AGP BALL)

=PP1V5_AGP
R4914 3.32K 1% 1/16W MF 402
AGP_VREF_GC
R4940 1.02K 1% 1/16W MF 402
C4940 0.01UF 20% 16V CERM 402

U4900
NV18B
BGA
(1 OF 5)
OMIT

AGP_AD<0>	AJ28	PCIAD0
AGP_AD<1>	AK28	PCIAD1
AGP_AD<2>	AH27	PCIAD2
AGP_AD<3>	AK27	PCIAD3
AGP_AD<4>	AJ27	PCIAD4
AGP_AD<5>	AH26	PCIAD5
AGP_AD<6>	AJ26	PCIAD6
AGP_AD<7>	AH25	PCIAD7
AGP_AD<8>	AH23	PCIAD8
AGP_AD<9>	AJ23	PCIAD9
AGP_AD<10>	AH22	PCIAD10
AGP_AD<11>	AJ22	PCIAD11
AGP_AD<12>	AJ21	PCIAD12
AGP_AD<13>	AK21	PCIAD13
AGP_AD<14>	AH20	PCIAD14
AGP_AD<15>	AJ20	PCIAD15
AGP_AD<16>	AG26	PCIAD16
AGP_AD<17>	AE24	PCIAD17
AGP_AD<18>	AG25	PCIAD18
AGP_AD<19>	AG24	PCIAD19
AGP_AD<20>	AF24	PCIAD20
AGP_AD<21>	AG23	PCIAD21
AGP_AD<22>	AE22	PCIAD22
AGP_AD<23>	AF22	PCIAD23
AGP_AD<24>	AE21	PCIAD24
AGP_AD<25>	AG20	PCIAD25
AGP_AD<26>	AG19	PCIAD26
AGP_AD<27>	AF19	PCIAD27
AGP_AD<28>	AE19	PCIAD28
AGP_AD<29>	AF18	PCIAD29
AGP_AD<30>	AG18	PCIAD30
AGP_AD<31>	AE18	PCIAD31
		AGP 2X,4X : AGP 8X
AGP_CBE<0>	AJ24	PCIC0/BE0* : C0*/BE0
AGP_CBE<1>	AH19	PCIC1/BE1* : C1*/BE1
AGP_CBE<2>	AF25	PCIC2/BE2* : C2*/BE2
AGP_CBE<3>	AG22	PCIC3/BE3* : C3*/BE3
AGP_CLK66M_GPU	AG12	PCICLK : CLK
NV_PCIRST_L	AF15	PCIRST* : RST*
AGP_GNT	AE15	PCIGNT* : GNT
AGP_REQ	AF13	PCIREQ* : REQ
AGP_FRAME	AK16	PCIFRAME* : FRAME
AGP_IRDY	AG16	PCIIRDY* : IRDY
AGP_TRDY	AJ17	PCITRDY* : TRDY
AGP_DEVSEL	AJ16	PCIDEVSEL* : DEVSEL
AGP_STOP	AH17	PCISTOP* : STOP
AGP_PAR	AK18	PCIPAR : PAR
AGP_INT_L	AG15	PCIINTA* : INTA
TP_GPU_INTB_L	AE10	NC_PCIINTB* : INTB
AGP_RBF	AG14	AGPRBF* : RBF
AGP_WBF	AG17	AGPWBF* : WBF
AGP_DBI_HI	AJ18	AGPPIPE* : DBI_HI
AGP_DBI_LO	AJ19	<RESRVD> : DBI_LO
AGP_ST<0>	AG13	AGPST0 : ST0
AGP_ST<1>	AE16	AGPST1 : ST1
AGP_ST<2>	AE13	AGPST2 : ST2
AGP_AD_STBF<0>	AK24	AGPADSTBF0 : ADSTBF0
AGP_AD_STBS<0>	AJ25	AGPADSTBS0* : ADSTBS0
AGP_AD_STBF<1>	AG21	AGPADSTBF1 : ADSTBF1
AGP_AD_STBS<1>	AF21	AGPADSTBS1* : ADSTBS1
AGP_SB_STBF	AK13	AGPSBSTBF : SBSTBF
AGP_SB_STBS	AJ13	AGPSBSTBS* : SBSTBS
AGP_SBA_L<0>	AJ11	AGPSBA0 : SBA0*
AGP_SBA_L<1>	AH11	AGPSBA1 : SBA1*
AGP_SBA_L<2>	AJ12	AGPSBA2 : SBA2*
AGP_SBA_L<3>	AH12	AGPSBA3 : SBA3*
AGP_SBA_L<4>	AJ14	AGPSBA4 : SBA4*
AGP_SBA_L<5>	AH14	AGPSBA5 : SBA5*
AGP_SBA_L<6>	AJ15	AGPSBA6 : SBA6*
AGP_SBA_L<7>	AH15	AGPSBA7 : SBA7*
GPU_MBDET_L	AF16	<RESRVD> : MBDET*
AGP_BUSY_L	AF12	AGPBUSY* : BUSY*
STOP_AGP_L	AG11	AGPSTOP* : STOP*
GPU_AGP_VREF	AK29	AGPVREF : AGPVREF

GPU_RESET_L
R4912 0 1% 1/16W MF 402
NV_PCIRST_L

=PP3V3_AGP
R4908 4.99K 1% 1/16W MF 402
AGP_INT_L

NB_AGP_GCDET_L
AGP_TYPEDET_L
R4913 0 5% 1/16W MF 402
R4909 10K 5% 1/16W MF 402

DOES HOOP UP AGP_BUSY_L &
STOP_AGP_L TO 3.3V OR 1.5V?

AGP VERSION SELECT
(LOW = AGP V3.X)
(HIGH = AGP V2.X)

R4903 0 5% 1/16W MF 402
NOSTUFF
R4950 10K 5% 1/16W MF 402
R4951 10K 5% 1/16W MF 402
GPU_BALLR7
GPU_BALLT7

NC
A1 TP_GPUC0
AK30 TP_GPUC1
G6 TP_GPUC2
R7 NC_TEST
T7 NC_TEST

TCLK C2
TMS C1
TDI D1
TDO E2
TRST* D2

NVAGP_TRST_L
R4905 1K
TP_NVAGP_TDO
TP_NVAGP_TDI
TP_NVAGP_TMS
NVAGP_TCLK
R4904 1K

BOUNDRY SCAN AVAILABLE ONLY ON NV3X SERIES

NVIDIA RECOMMENDS A WIDER RANGE OF CAP VALUES, EMC LIKES ONE VALUE

=PP1V5_AGP

AGPVDDQ: AE14 AE11 AE17 AE20 AE23 AD11 AD14 AD23 AD20 AD17

VDD: AA17 AA18 L20 Y20 L13 Y13 N20 P20 U20 V20 L11 N11 P11 U11 V11 Y11 L14 Y14 L17 Y17 L18 Y18

VDD33: H6 AC6 U7 G14 U6 AD15 H7 AD16 AD19 AD22 AC7 AD12 P24

OUTPUT DRIVER BYPASS

C4912 0.01UF 10% 16V CERM 402
C4911 0.01UF 10% 16V CERM 402
C4904 0.1UF 20% 10V CERM 402
C4905 0.1UF 20% 10V CERM 402
C4906 0.1UF 20% 10V CERM 402
C4913 0.1UF 20% 10V CERM 402
C4907 0.1UF 20% 10V CERM 402
C4908 0.1UF 20% 10V CERM 402
C4909 0.1UF 20% 10V CERM 402
C4910 0.1UF 20% 10V CERM 402

=PPVCORE_GPU

CORE BYPASS

C4914 0.01UF 10% 16V CERM 402
C4915 0.01UF 10% 16V CERM 402
C4916 0.1UF 20% 10V CERM 402
C4917 0.1UF 20% 10V CERM 402
C4918 0.1UF 20% 10V CERM 402
C4919 0.1UF 20% 10V CERM 402
C4920 0.1UF 20% 10V CERM 402
C4921 0.1UF 20% 10V CERM 402
C4922 0.1UF 20% 10V CERM 402
C4923 0.1UF 20% 10V CERM 402
C4924 0.1UF 20% 10V CERM 402

C4925 0.01UF 10% 16V CERM 402
C4926 0.01UF 10% 16V CERM 402
C4927 0.1UF 20% 10V CERM 402
C4928 0.1UF 20% 10V CERM 402
C4929 0.1UF 20% 10V CERM 402
C4930 0.1UF 20% 10V CERM 402
C4931 0.1UF 20% 10V CERM 402
C4932 0.1UF 20% 10V CERM 402

C4961 10UF 20% 6.3V CERM 805
C4960 10UF 20% 6.3V CERM 805
C4902 10UF 20% 6.3V CERM 805
C4900 10UF 20% 6.3V CERM 805
C4903 10UF 20% 6.3V CERM 805
C4901 10UF 20% 6.3V CERM 805
C4933 0.1UF 20% 10V CERM 402
C4934 0.1UF 20% 10V CERM 402
C4935 0.1UF 20% 10V CERM 402

=PP3V3_AGP
NV34 L4901 1000-OHM-EMI SM

AGP_PLLVDD
VOLTAGE=1.3V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL

NV34 C4959 4.7UF 20% 6.3V CERM 805
NV34 C4956 0.1UF 20% 10V CERM 402
NV34 C4955 0.001UF 10% 50V CERM 402

=PP3V3_AGP

I/O BYPASS

C4936 0.01UF 10% 16V CERM 402
C4942 0.01UF 10% 16V CERM 402
C4938 0.1UF 20% 10V CERM 402
C4939 0.1UF 20% 10V CERM 402
C4941 0.1UF 20% 10V CERM 402
C4937 0.1UF 20% 10V CERM 402

C4943 10UF 20% 6.3V CERM 805
C4944 0.01UF 10% 16V CERM 402
C4945 0.01UF 10% 16V CERM 402
C4946 0.1UF 20% 10V CERM 402
C4947 0.1UF 20% 10V CERM 402
C4949 0.1UF 20% 10V CERM 402
C4950 0.1UF 20% 10V CERM 402
C4951 0.1UF 20% 10V CERM 402
C4952 0.1UF 20% 10V CERM 402

=PP5V_AGP
C4953 0.1UF 20% 10V CERM 402
C4954 0.1UF 20% 10V CERM 402

VD50CLAMP0 N4
VD50CLAMP1 AE9
AGP_PLLVDD AE12
50 OHM TO VDDQ AGPCALPD AA13
50 OHM TO GND AGPCALPU AA14
GPU_50PULLUP
GPU_50PULLDWN
10K OHM TO GND TESTMODE AE5
GPU_TMODE
R4901 10K 5% 1/16W MF 402
R4900 49.9 1% 1/16W MF 402

=PP1V5_AGP
R4902 49.9 1% 1/16W MF 402

=PP3V3_AGP
NV34 R4910 10K 5% 1/16W MF 402
NV34 R4911 10K 5% 1/16W MF 402

=PP1V5_AGP
R4906 3.32K 1% 1/16W MF 402
GPU_AGP_VREF
VOLTAGE=0.75V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
R4907 1.02K 1% 1/16W MF 402
C4957 0.01UF 20% 16V CERM 402

GPU AGP I/O REFERENCE
(PLACE CLOSE TO U3LITE AGP BALLS)

FROM Q27 PAGE 24

NVIDIA AGP

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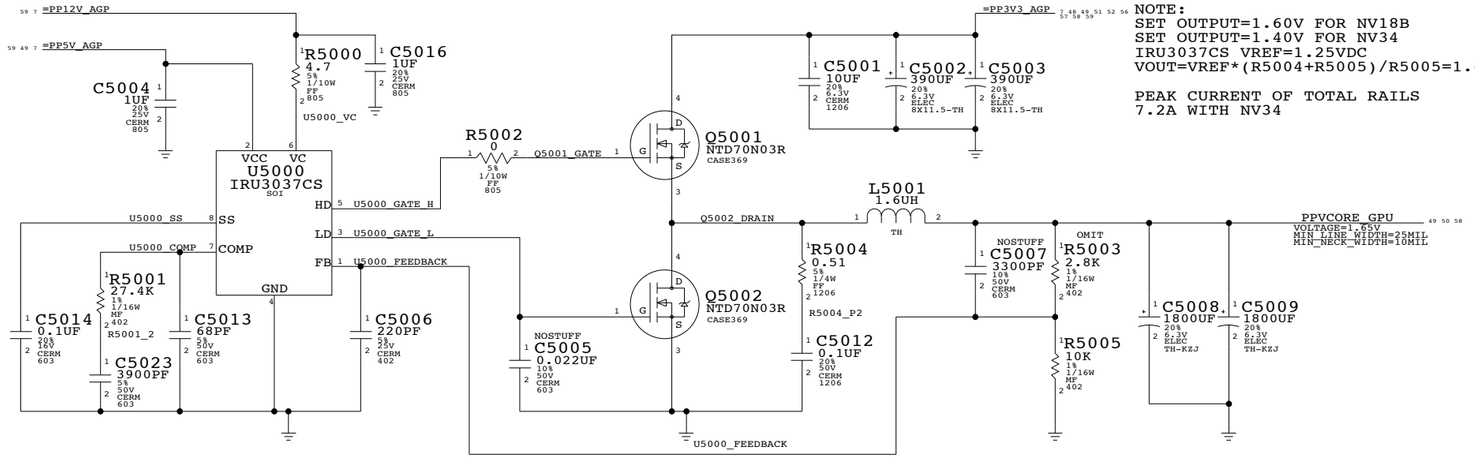
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 49 OF 103	

GPU VCORE VREG

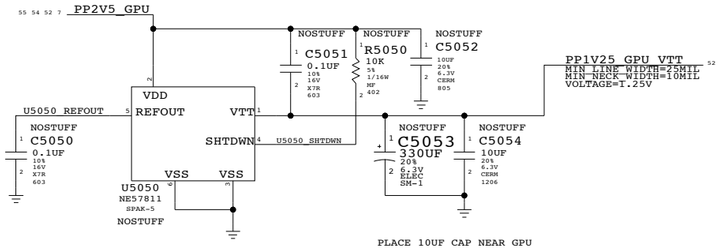
PPVCORE_GPU	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
1.60VDC	114S2803	1	RES,2.8K OHM,1/16W,1%,0402	R5003	NV18B
1.40VDC	114S1213	1	RES,1.21K OHM,1/16W,1%,0402	R5003	NV34



NOTE:
SET OUTPUT=1.60V FOR NV18B
SET OUTPUT=1.40V FOR NV34
IRU3037CS VREF=1.25VDC
VOUT=VREF*(R5004+R5005)/R5005=1.60(OR 1.40) VDC

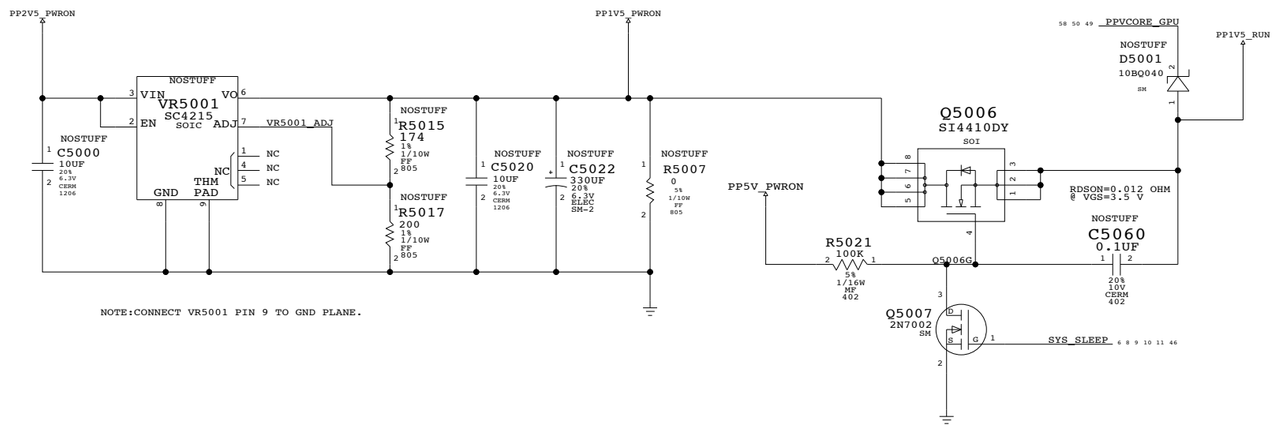
PEAK CURRENT OF TOTAL RAILS
7.2A WITH NV34

GPU VTT VREG



PLACE 10UF CAP NEAR GPU

AGP 1.5V VREG



NOTE:CONNECT VR5001 PIN 9 TO GND PLANE.

NOTE:
SET OUTPUT=1.5V
SC4215 VREF=0.8VDC
VOUT=VREF*(R5015+R5017)/R5017=1.5 VDC

PEAK CURRENT OF TOTAL RAILS
0.95A

GRAPHICS VREGS

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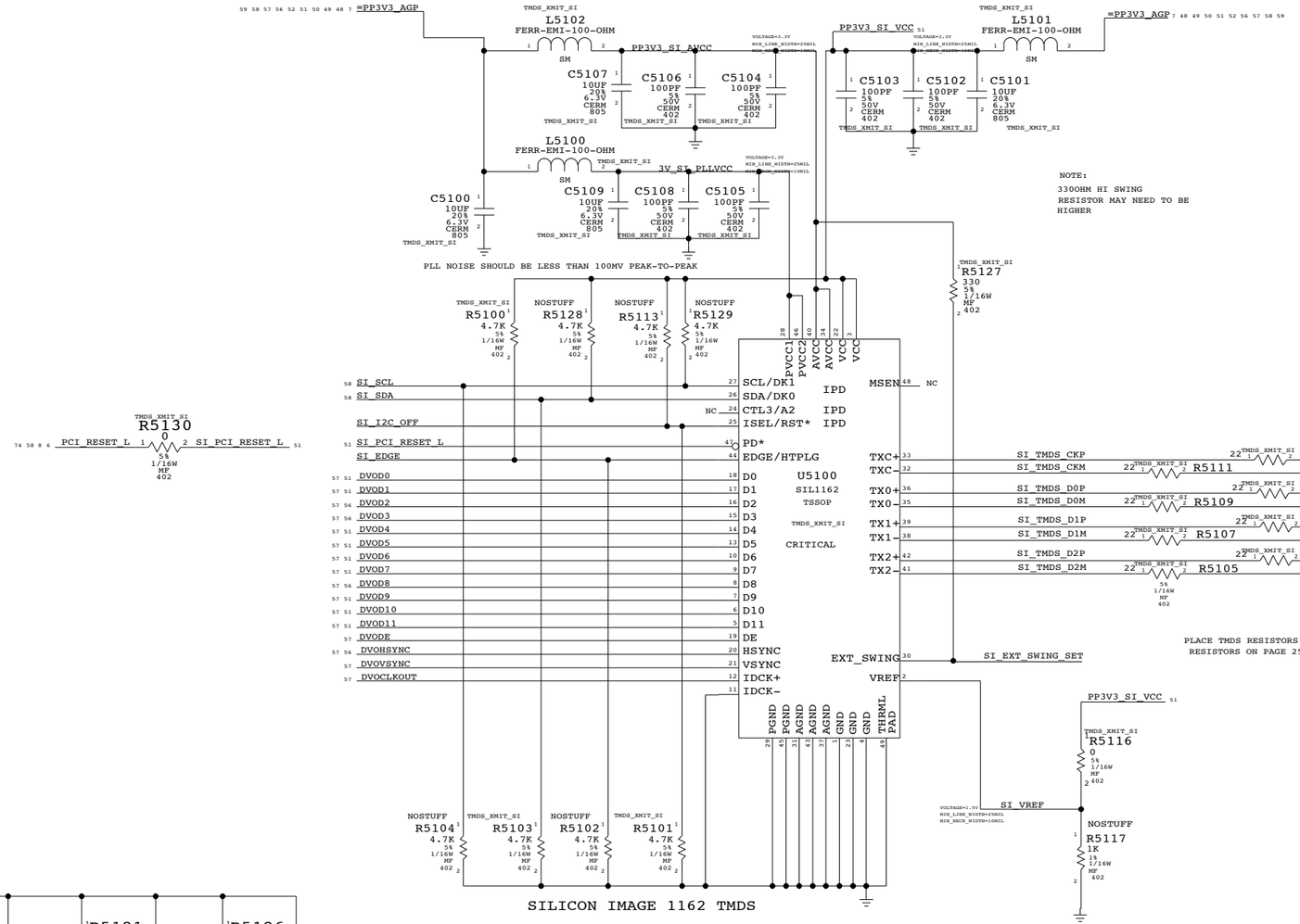
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 50 OF 103	



EXTERNAL TMDS TRANSMITTER

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 51 OF 103	

DRAWING

NVIDIA RECOMMENDS WIDER RANGE OF CAP VALUES, EMC LIKE ONE VALUE

EVENLY DISTRIBUTE 0.01UF & 0.1 UF CAPS

AMONGST FBVDDQ PINS ON NV ASIC

PP2V5_GPU

C5208 0.01UF 10% 16V CERM 402
C5215 0.01UF 10% 16V CERM 402
C5216 0.1UF 10% 10V CERM 402
C5217 0.1UF 10% 10V CERM 402
C5218 0.1UF 10% 10V CERM 402
C5221 0.01UF 10% 16V CERM 402
C5219 0.1UF 10% 10V CERM 402
C5220 0.01UF 10% 16V CERM 402
C5213 0.1UF 10% 10V CERM 402
C5212 0.1UF 10% 10V CERM 402
C5211 0.1UF 10% 10V CERM 402
C5210 0.1UF 10% 10V CERM 402
C5201 1.0UF 20% 6.3V CERM 805
C5222 0.1UF 10% 10V CERM 402
C5224 0.1UF 10% 10V CERM 402
C5225 0.1UF 10% 10V CERM 402
C5226 0.01UF 10% 16V CERM 402
C5227 0.1UF 10% 10V CERM 402
C5228 0.1UF 10% 10V CERM 402
C5229 0.01UF 10% 16V CERM 402
C5200 0.1UF 10% 10V CERM 402
C5223 0.01UF 10% 16V CERM 402
C5214 0.1UF 10% 10V CERM 402
C5209 0.1UF 10% 10V CERM 402
C5202 1.0UF 20% 6.3V CERM 805

U4900
NV18B
BGA
(3 OF 5)

FBVDDQ
NC_VTT
GND

FBAD0 FBAD1 FBAD2 FBAD3 FBAD4 FBAD5 FBAD6 FBAD7 FBAD8 FBAD9 FBAD10 FBAD11 FBAD12 FBAD13 FBAD14 FBAD15 FBAD16 FBAD17 FBAD18 FBAD19 FBAD20 FBAD21 FBAD22 FBAD23 FBAD24 FBAD25 FBAD26 FBAD27 FBAD28 FBAD29 FBAD30 FBAD31 FBAD32 FBAD33 FBAD34 FBAD35 FBAD36 FBAD37 FBAD38 FBAD39 FBAD40 FBAD41 FBAD42 FBAD43 FBAD44 FBAD45 FBAD46 FBAD47 FBAD48 FBAD49 FBAD50 FBAD51 FBAD52 FBAD53 FBAD54 FBAD55 FBAD56 FBAD57 FBAD58 FBAD59 FBAD60 FBAD61 FBAD62 FBAD63

FBADQM0 FBADQM1 FBADQM2 FBADQM3 FBADQM4 FBADQM5 FBADQM6 FBADQM7

FBAA0 FBAA1 FBAA2 FBAA3 FBAA4 FBAA5 FBAA6 FBAA7 FBAA8 FBAA9 FBAA10 FBAA11 FBAA12

FBABA0 FBABA1

FBARAS* FBACAS* FBAWE* FBACSO* FBACS1*

FBVREF

ROMA14 ROMA15 ROMCS*

PP1V25_GPU_VTT

NV36 C5250 0.1UF 10% 10V CERM 402
NV36 C5251 0.1UF 10% 10V CERM 402
NV36 C5252 0.1UF 10% 10V CERM 402
NV36 C5253 0.1UF 10% 10V CERM 402
NV36 C5254 0.1UF 10% 10V CERM 402
NV36 C5255 0.1UF 10% 10V CERM 402
NV36 C5256 0.1UF 10% 10V CERM 402
NV36 C5257 0.1UF 10% 10V CERM 402
NV36 C5258 0.1UF 10% 10V CERM 402
NV36 C5259 0.1UF 10% 10V CERM 402
NV36 C5260 0.1UF 10% 10V CERM 402
NV36 C5261 0.1UF 10% 10V CERM 402

DIFFERENTIAL_PAIR	NET_SPACING_TYPE
FBACLK0	FBCLK
FBACLK0_L	FBCLK
FBACLK1	FBCLK
FBACLK1_L	FBCLK
FBBCLK0	FBCLK
FBBCLK0_L	FBCLK
FBBCLK1	FBCLK
FBBCLK1_L	FBCLK

FBCALPU_GND
FBCAL_TERM_GND
FBCAL_CLK_GND
FB_DLLVDD
FBACKE

NV34 R5202 49.9 1% 1/16W MF 402
NV34 R5203 49.9 1% 1/16W MF 402
R5201 10K 1% 1/16W MF 402
NOSTUFF R5207 549 1% 1/16W MF 402
NOSTUFF R5208 0 1% 1/16W MF 402

WEAK PULL-DOWN RECOMMENDED BY NVIDIA.

FBACLK0 FBACLK0_L FBACLK1 FBACLK1_L
FBADQS0 FBADQS1 FBADQS2 FBADQS3 FBADQS4 FBADQS5 FBADQS6 FBADQS7

NC_FBADQS0 NC_FBADQS1 NC_FBADQS2 NC_FBADQS3 NC_FBADQS4 NC_FBADQS5 NC_FBADQS6 NC_FBADQS7

FB_DLLVDD

NV34 C5205 4.7UF 20% 10V TANT A
NV34 C5206 0.33UF 10% 10V CERM 402
NV34 C5207 0.0010UF 10% 50V CERM 402

NV34 R5206 10 1% 1/16W MF 402

PP2V5_GPU

R5204 1K 1% 1/16W MF 402
R5205 1K 1% 1/16W MF 402
C5203 0.10F 10% 16V CERM 402
C5204 0.10F 10% 16V CERM 402

VOLTAGE=1.25V
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL

U4900
NV18B
BGA
(4 OF 5)

THERMAL GND

FBCD0 FBCD1 FBCD2 FBCD3 FBCD4 FBCD5 FBCD6 FBCD7 FBCD8 FBCD9 FBCD10 FBCD11 FBCD12 FBCD13 FBCD14 FBCD15 FBCD16 FBCD17 FBCD18 FBCD19 FBCD20 FBCD21 FBCD22 FBCD23 FBCD24 FBCD25 FBCD26 FBCD27 FBCD28 FBCD29 FBCD30 FBCD31 FBCD32 FBCD33 FBCD34 FBCD35 FBCD36 FBCD37 FBCD38 FBCD39 FBCD40 FBCD41 FBCD42 FBCD43 FBCD44 FBCD45 FBCD46 FBCD47 FBCD48 FBCD49 FBCD50 FBCD51 FBCD52 FBCD53 FBCD54 FBCD55 FBCD56 FBCD57 FBCD58 FBCD59 FBCD60 FBCD61 FBCD62 FBCD63

FBCDQM0 FBCDQM1 FBCDQM2 FBCDQM3 FBCDQM4 FBCDQM5 FBCDQM6 FBCDQM7

FBCA0 FBCA1 FBCA2 FBCA3 FBCA4 FBCA5 FBCA6 FBCA7 FBCA8 FBCA9 FBCA10 FBCA11 FBCA12

FBCBA0 FBCBA1

FBBCLK0 FBBCLK0* FBBCLK1 FBBCLK1*

FBCLK 0 AND 1 SWAPPED FOR ROUTING REASONS

FBCDQS0 FBCDQS1 FBCDQS2 FBCDQS3 FBCDQS4 FBCDQS5 FBCDQS6 FBCDQS7

NC_FBCDQS0 NC_FBCDQS1 NC_FBCDQS2 NC_FBCDQS3 NC_FBCDQS4 NC_FBCDQS5 NC_FBCDQS6 NC_FBCDQS7

FBCAS* FBCCAS* FBCWE* FBCCS0* FBCCS1* FBCCKE

FBRAS_L FBCAS_L FBWE_L FBCS0_L TP_FBCS1_L FBCKE

R5200 10K 1% 1/16W MF 402

WEAK PULL-DOWN RECOMMENDED BY NVIDIA

ALTERNATE STUFFING FOR 10 OHM R IS FILTER APH 15580052 PER NVIDIA SPEC

NVIDIA FRAME BUFFER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
E	051-6482	??
SCALE: NONE	SHT 52 OF 103	

PLACE R'S CLOSE TO MEMORY

FBD<31>	15	1	8	RP5320	RFBD<31>	
FBD<30>	15	2	7	RP5320	RFBD<30>	
FBD<29>	15	3	6	RP5320	RFBD<29>	
FBD<28>	15	4	5	RP5320	RFBD<28>	
FBD<27>	15	1	8	RP5321	RFBD<27>	
FBD<26>	15	2	7	RP5321	RFBD<26>	
FBD<25>	15	3	6	RP5321	RFBD<25>	
FBD<24>	15	4	5	RP5321	RFBD<24>	
FBD<0>	15	1	8	RP5322	RFBD<0>	
FBD<1>	15	2	7	RP5322	RFBD<1>	
FBD<2>	15	3	6	RP5322	RFBD<2>	
FBD<3>	15	4	5	RP5322	RFBD<3>	
FBD<17>	15	1	8	RP5323	RFBD<17>	
FBD<16>	15	2	7	RP5323	RFBD<16>	
FBD<18>	15	3	6	RP5323	RFBD<18>	
FBD<19>	15	4	5	RP5323	RFBD<19>	
FBD<15>	15	1	8	RP5324	RFBD<15>	
FBD<14>	15	2	7	RP5324	RFBD<14>	
FBD<13>	15	3	6	RP5324	RFBD<13>	
FBD<12>	15	4	5	RP5324	RFBD<12>	
FBD<10>	15	1	8	RP5325	RFBD<10>	
FBD<11>	15	2	7	RP5325	RFBD<11>	
FBD<9>	15	3	6	RP5325	RFBD<9>	
FBD<8>	15	4	5	RP5325	RFBD<8>	
FBD<5>	15	1	8	RP5326	RFBD<5>	
FBD<6>	15	2	7	RP5326	RFBD<6>	
FBD<4>	15	3	6	RP5326	RFBD<4>	
FBD<7>	15	4	5	RP5326	RFBD<7>	
FBD<20>	15	1	8	RP5327	RFBD<20>	
FBD<21>	15	2	7	RP5327	RFBD<21>	
FBD<22>	15	3	6	RP5327	RFBD<22>	
FBD<23>	15	4	5	RP5327	RFBD<23>	

FBD<32>	15	3	6	RP5328	RFBD<32>	
FBD<33>	15	4	5	RP5328	RFBD<33>	
FBD<34>	15	1	8	RP5328	RFBD<34>	
FBD<35>	15	2	7	RP5328	RFBD<35>	
FBD<36>	15	4	5	RP5316	RFBD<36>	
FBD<37>	15	3	6	RP5316	RFBD<37>	
FBD<38>	15	2	7	RP5316	RFBD<38>	
FBD<39>	15	1	8	RP5316	RFBD<39>	
FBD<40>	15	2	7	RP5329	RFBD<40>	
FBD<41>	15	1	8	RP5329	RFBD<41>	
FBD<42>	15	3	6	RP5329	RFBD<42>	
FBD<43>	15	4	5	RP5329	RFBD<43>	
FBD<44>	15	1	8	RP5330	RFBD<44>	
FBD<45>	15	2	7	RP5330	RFBD<45>	
FBD<46>	15	4	5	RP5330	RFBD<46>	
FBD<47>	15	3	6	RP5330	RFBD<47>	
FBD<48>	15	4	5	RP5331	RFBD<48>	
FBD<49>	15	3	6	RP5331	RFBD<49>	
FBD<50>	15	1	8	RP5331	RFBD<50>	
FBD<51>	15	2	7	RP5331	RFBD<51>	
FBD<52>	15	4	5	RP5300	RFBD<52>	
FBD<53>	15	3	6	RP5300	RFBD<53>	
FBD<54>	15	2	7	RP5300	RFBD<54>	
FBD<55>	15	1	8	RP5300	RFBD<55>	
FBD<56>	15	1	8	RP5301	RFBD<56>	
FBD<57>	15	2	7	RP5301	RFBD<57>	
FBD<58>	15	4	5	RP5301	RFBD<58>	
FBD<59>	15	3	6	RP5301	RFBD<59>	
FBD<60>	15	1	8	RP5302	RFBD<60>	
FBD<61>	15	3	6	RP5302	RFBD<61>	
FBD<62>	15	2	7	RP5302	RFBD<62>	
FBD<63>	15	4	5	RP5302	RFBD<63>	

FBD<64>	GPU128BIT	15	1	8	RP5310	RFBD<64>
FBD<65>	GPU128BIT	15	2	7	RP5310	RFBD<65>
FBD<66>	GPU128BIT	15	3	6	RP5310	RFBD<66>
FBD<67>	GPU128BIT	15	4	5	RP5310	RFBD<67>
FBD<84>	GPU128BIT	15	1	8	RP5309	RFBD<84>
FBD<85>	GPU128BIT	15	2	7	RP5309	RFBD<85>
FBD<86>	GPU128BIT	15	3	6	RP5309	RFBD<86>
FBD<87>	GPU128BIT	15	4	5	RP5309	RFBD<87>
FBD<72>	GPU128BIT	15	4	5	RP5319	RFBD<72>
FBD<73>	GPU128BIT	15	3	6	RP5319	RFBD<73>
FBD<75>	GPU128BIT	15	2	7	RP5319	RFBD<75>
FBD<74>	GPU128BIT	15	1	8	RP5319	RFBD<74>
FBD<68>	GPU128BIT	15	1	8	RP5308	RFBD<68>
FBD<70>	GPU128BIT	15	2	7	RP5308	RFBD<70>
FBD<69>	GPU128BIT	15	3	6	RP5308	RFBD<69>
FBD<71>	GPU128BIT	15	4	5	RP5308	RFBD<71>
FBD<80>	GPU128BIT	15	1	8	RP5307	RFBD<80>
FBD<81>	GPU128BIT	15	2	7	RP5307	RFBD<81>
FBD<82>	GPU128BIT	15	3	6	RP5307	RFBD<82>
FBD<83>	GPU128BIT	15	4	5	RP5307	RFBD<83>
FBD<76>	GPU128BIT	15	4	5	RP5317	RFBD<76>
FBD<77>	GPU128BIT	15	3	6	RP5317	RFBD<77>
FBD<78>	GPU128BIT	15	2	7	RP5317	RFBD<78>
FBD<79>	GPU128BIT	15	1	8	RP5317	RFBD<79>
FBD<91>	GPU128BIT	15	1	8	RP5318	RFBD<91>
FBD<90>	GPU128BIT	15	2	7	RP5318	RFBD<90>
FBD<89>	GPU128BIT	15	3	6	RP5318	RFBD<89>
FBD<88>	GPU128BIT	15	4	5	RP5318	RFBD<88>
FBD<95>	GPU128BIT	15	1	8	RP5303	RFBD<95>
FBD<94>	GPU128BIT	15	2	7	RP5303	RFBD<94>
FBD<93>	GPU128BIT	15	3	6	RP5303	RFBD<93>
FBD<92>	GPU128BIT	15	4	5	RP5303	RFBD<92>

FBD<96>	GPU128BIT	15	4	5	RP5315	RFBD<96>
FBD<97>	GPU128BIT	15	3	6	RP5315	RFBD<97>
FBD<98>	GPU128BIT	15	2	7	RP5315	RFBD<98>
FBD<99>	GPU128BIT	15	1	8	RP5315	RFBD<99>
FBD<100>	GPU128BIT	15	4	5	RP5314	RFBD<100>
FBD<101>	GPU128BIT	15	3	6	RP5314	RFBD<101>
FBD<102>	GPU128BIT	15	2	7	RP5314	RFBD<102>
FBD<103>	GPU128BIT	15	1	8	RP5314	RFBD<103>
FBD<104>	GPU128BIT	15	1	8	RP5312	RFBD<104>
FBD<105>	GPU128BIT	15	2	7	RP5312	RFBD<105>
FBD<106>	GPU128BIT	15	3	6	RP5312	RFBD<106>
FBD<107>	GPU128BIT	15	4	5	RP5312	RFBD<107>
FBD<108>	GPU128BIT	15	1	8	RP5313	RFBD<108>
FBD<109>	GPU128BIT	15	2	7	RP5313	RFBD<109>
FBD<110>	GPU128BIT	15	3	6	RP5313	RFBD<110>
FBD<111>	GPU128BIT	15	4	5	RP5313	RFBD<111>
FBD<112>	GPU128BIT	15	4	5	RP5311	RFBD<112>
FBD<113>	GPU128BIT	15	3	6	RP5311	RFBD<113>
FBD<114>	GPU128BIT	15	2	7	RP5311	RFBD<114>
FBD<115>	GPU128BIT	15	1	8	RP5311	RFBD<115>
FBD<116>	GPU128BIT	15	4	5	RP5306	RFBD<116>
FBD<117>	GPU128BIT	15	3	6	RP5306	RFBD<117>
FBD<118>	GPU128BIT	15	2	7	RP5306	RFBD<118>
FBD<119>	GPU128BIT	15	1	8	RP5306	RFBD<119>
FBD<120>	GPU128BIT	15	1	8	RP5304	RFBD<120>
FBD<121>	GPU128BIT	15	2	7	RP5304	RFBD<121>
FBD<122>	GPU128BIT	15	4	5	RP5304	RFBD<122>
FBD<123>	GPU128BIT	15	3	6	RP5304	RFBD<123>
FBD<124>	GPU128BIT	15	1	8	RP5305	RFBD<124>
FBD<125>	GPU128BIT	15	3	6	RP5305	RFBD<125>
FBD<126>	GPU128BIT	15	2	7	RP5305	RFBD<126>
FBD<127>	GPU128BIT	15	4	5	RP5305	RFBD<127>

PLACE R'S CLOSE TO GPU

FBACLK1 — R5316 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBACLK1_L

FBACLK0 — R5317 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBACLK0_L

FBBCLK1 — R5318 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBBCLK1_L

FBBCLK0 — R5319 100 1% 1/16W MF 402 — PLACE 100OHM TERM AT RAM — FBBCLK0_L

PLACE THESE R CLOSE TO SGRAM

FBDQS<0>	R5301 15 1% 1/16W MF 402	RFBDQS<0>
FBDQS<1>	R5302 15 1% 1/16W MF 402	RFBDQS<1>
FBDQS<2>	R5300 15 1% 1/16W MF 402	RFBDQS<2>
FBDQS<3>	R5303 15 1% 1/16W MF 402	RFBDQS<3>
FBDQS<4>	R5307 15 1% 1/16W MF 402	RFBDQS<4>
FBDQS<5>	R5305 15 1% 1/16W MF 402	RFBDQS<5>
FBDQS<6>	R5306 15 1% 1/16W MF 402	RFBDQS<6>
FBDQS<7>	R5304 15 1% 1/16W MF 402	RFBDQS<7>

PLACE THESE R CLOSE TO SGRAM

FBDQS<8>	R5308 15 1% 1/16W MF 402	RFBDQS<8>
FBDQS<9>	R5314 15 1% 1/16W MF 402	RFBDQS<9>
FBDQS<10>	R5309 15 1% 1/16W MF 402	RFBDQS<10>
FBDQS<11>	R5315 15 1% 1/16W MF 402	RFBDQS<11>
FBDQS<12>	R5310 15 1% 1/16W MF 402	RFBDQS<12>
FBDQS<13>	R5313 15 1% 1/16W MF 402	RFBDQS<13>
FBDQS<14>	R5311 15 1% 1/16W MF 402	RFBDQS<14>
FBDQS<15>	R5312 15 1% 1/16W MF 402	RFBDQS<15>

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FB TERMINATION

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 53 OF 103	

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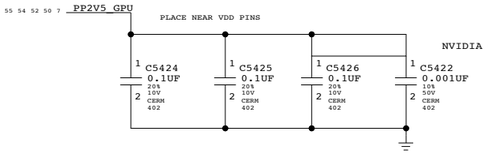
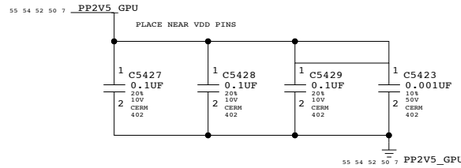
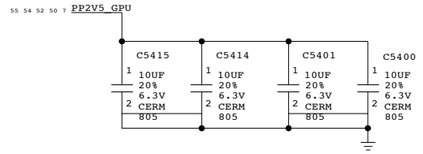
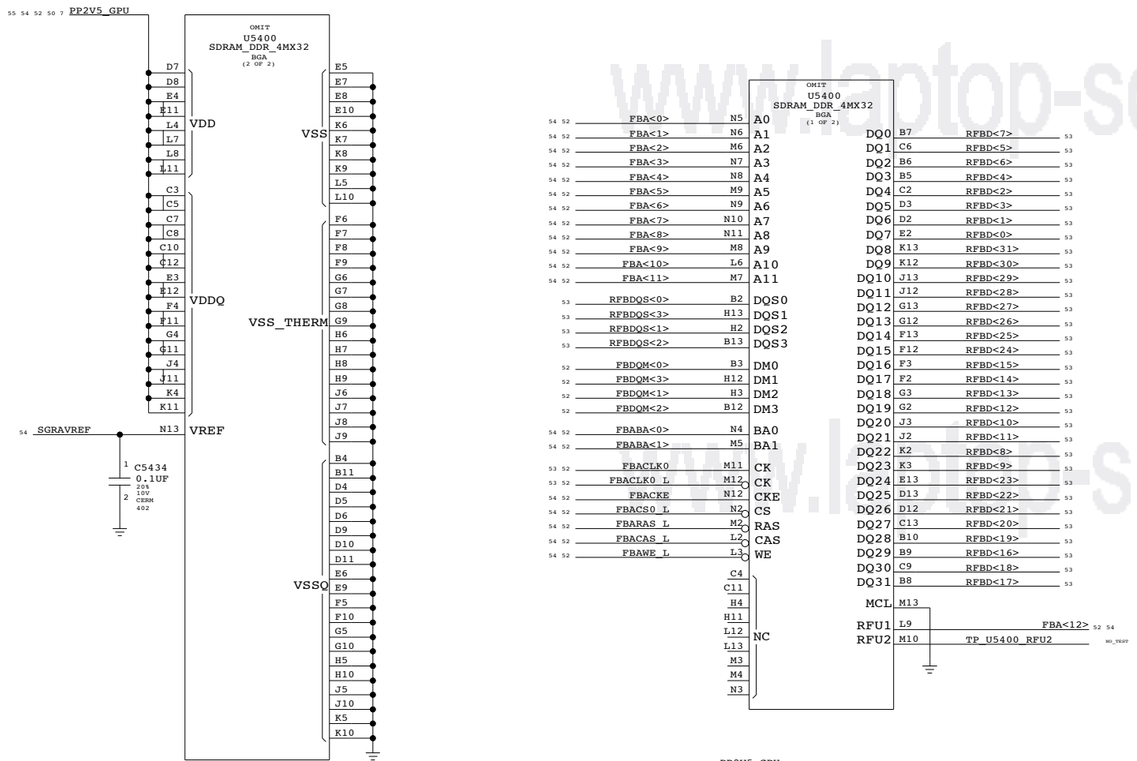
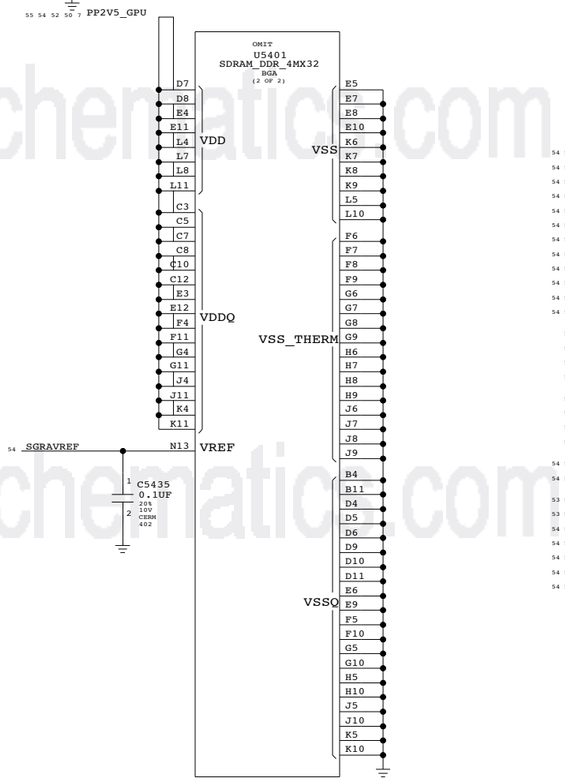


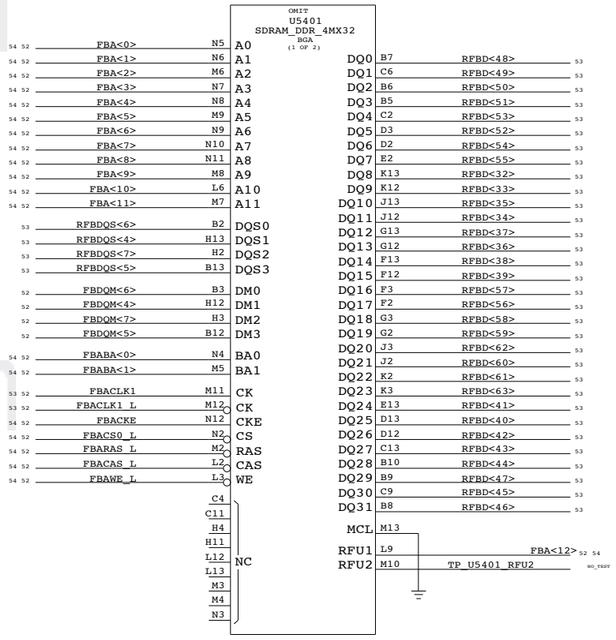
NVIDIA RECOMMENDS WIDER RANGE OF CAP VALUES

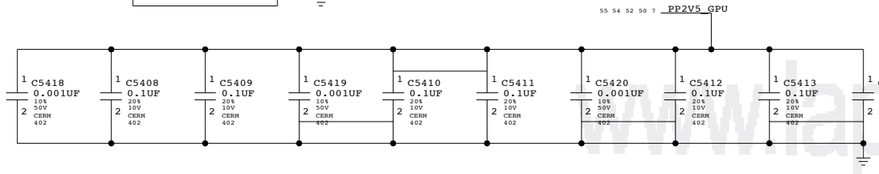


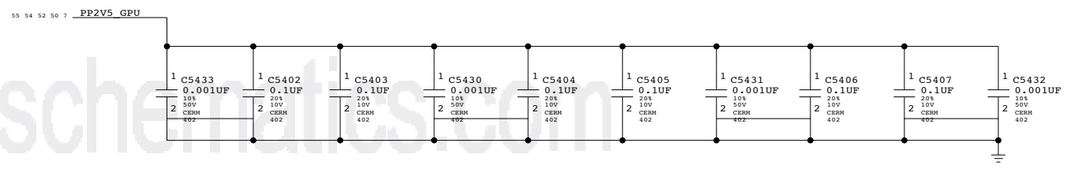






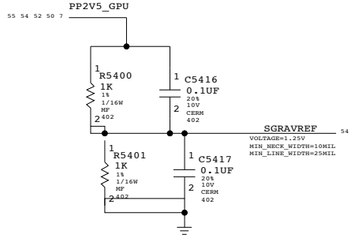






EVENLY PLACE 0.1UF CAP & 0.01UF CAPS

DDR SDRAM A VREF



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	SAMSUNG
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5400,U5401	CRITICAL	HYNIX

GPU DDR SDRAM A

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 54 OF 103	

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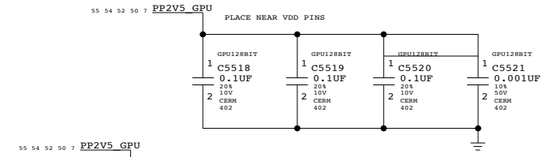
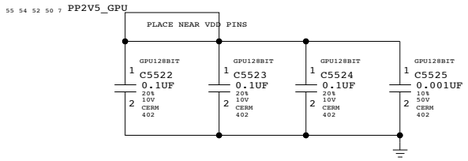
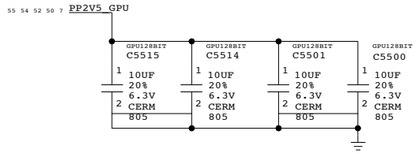
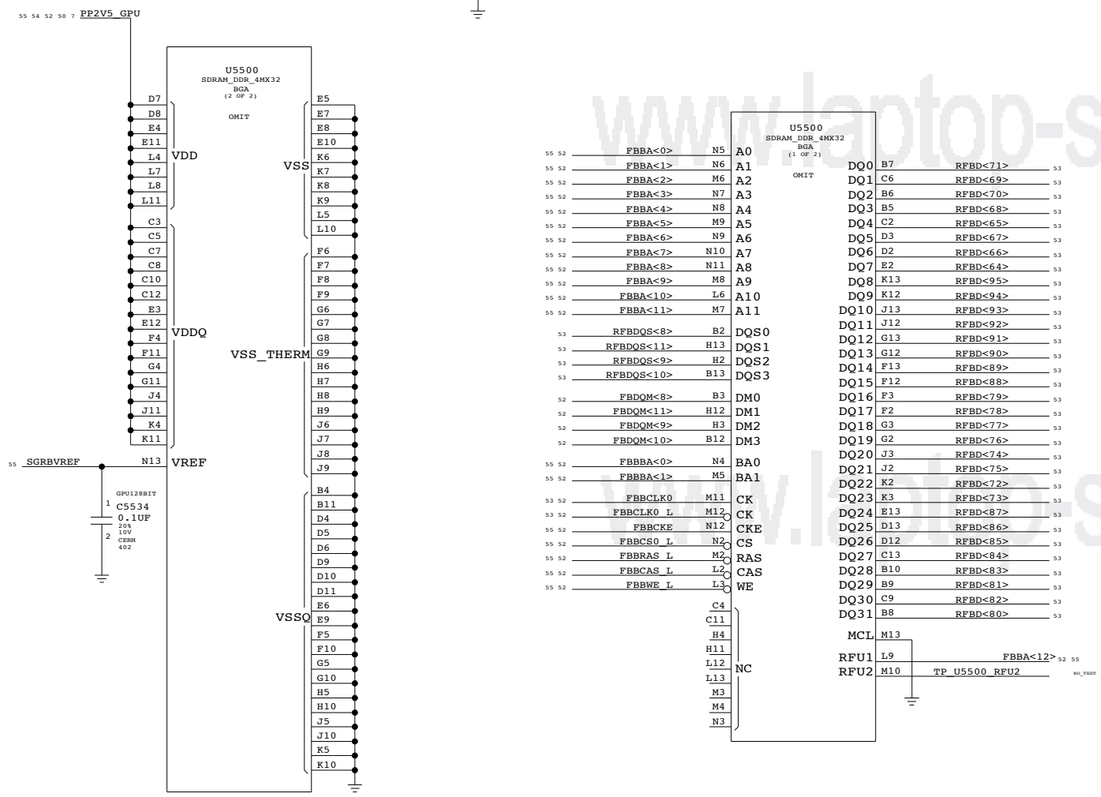
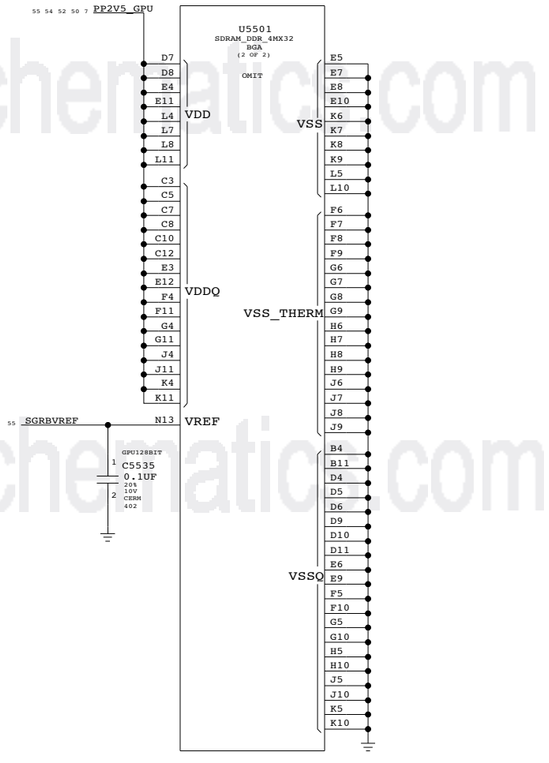
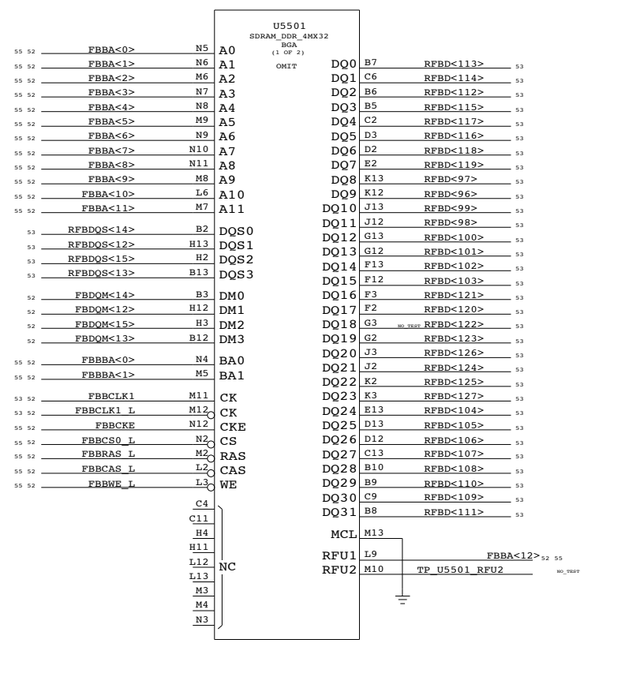


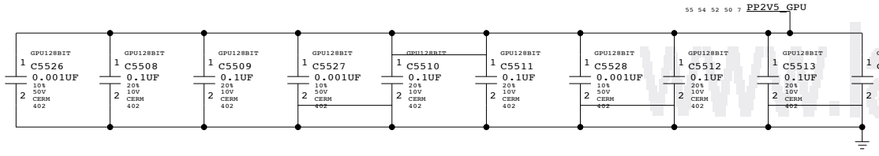


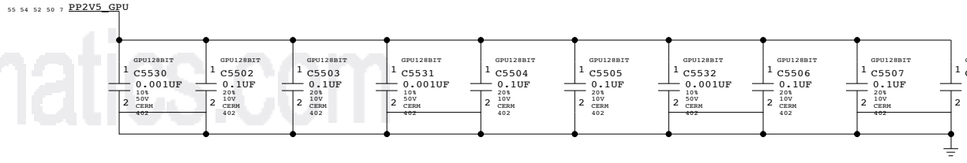






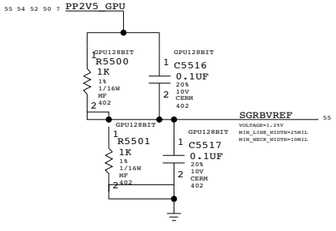






DDR SDRAM B VREF

EVENLY PLACE 0.1UF CAP & 0.01 UF CAPS



SGRAM0 & SGRAM1 MEMORY SUPPORT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0251	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	GPU128BIT_SAMSUNG
333S0252	2	SDRAM,4MX32,DDR,300MHZ	U5500,U5501	CRITICAL	GPU128BIT_HYNIX

GPU DDR SDRAM B

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 55 OF 103	

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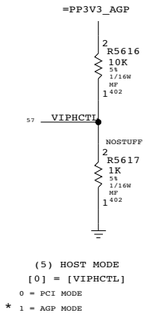
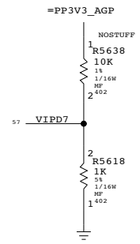
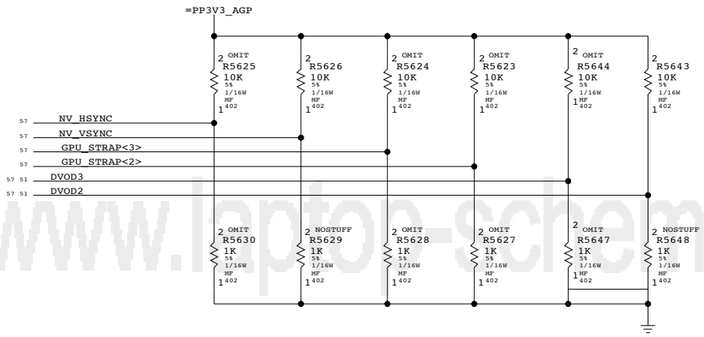


(5) HOST MODE
[0] = [VIPHCTL]
0 = PCI MODE
* 1 = AGP MODE

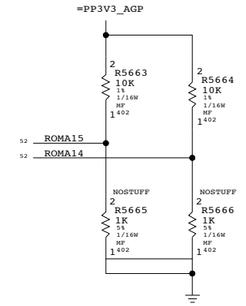


(6) AGP SIDEBAND
[0] = [VIPD7]
* 0 = ENABLE AGP SIDEBAND
1 = DISABLE AGP SIDEBAND

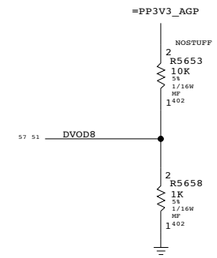


(8) FRAME BUFFER MEMORY SPEED
[5..0] = [NV11_HSYNC,NV11_VSYNC,GPU_STRAP<3>,GPU_STRAP<2>,DVOD3,DVOD2]

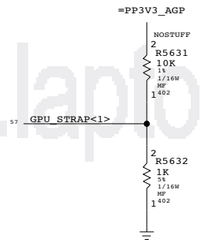
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
110111 = 270MHZ SAMSUNG (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5623		270MHZ_SAM_18
116S1104	1	RES,10K-OHM,1/16W,5%	R5644		270MHZ_SAM_18
116S1103	1	RES,1K-OHM,1/16W,5%	R5628		270MHZ_SAM_18
110011 = 270MHZ HYNIX (NV18B)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5644		270MHZ_HYN_18
116S1103	2	RES,1K-OHM,1/16W,5%	R5628,R5627		270MHZ_HYN_18
111101 = 270MHZ SAMSUNG (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5625,R5624		270MHZ_SAM_34
116S1104	1	RES,10K-OHM,1/16W,5%	R5623		270MHZ_SAM_34
116S1103	1	RES,1K-OHM,1/16W,5%	R5647		270MHZ_SAM_34
111100 = 270MHZ HYNIX (NV34)					
116S1104	2	RES,10K-OHM,1/16W,5%	R5624,R5623		270MHZ_HYN_34
116S1103	2	RES,1K-OHM,1/16W,5%	R5630,R5647		270MHZ_HYN_34



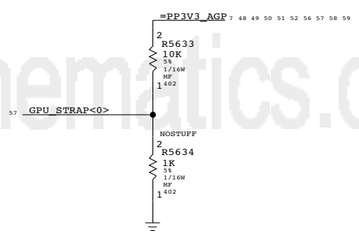
(1) ROM TYPE (OVERRIDDEN IF STRAP1 = 0)
[1..0] = [ROMA15,ROMA14]
00 = PARALLEL
01 = SERIAL AT25F
10 = SERIAL SST45VF
* 11 = SERIAL FUTURE



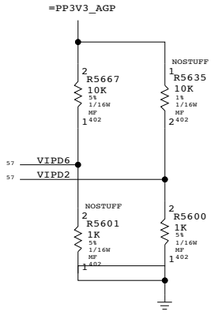
FAST WRITE SUPPORT
0=ENABLE
1=DISABLE



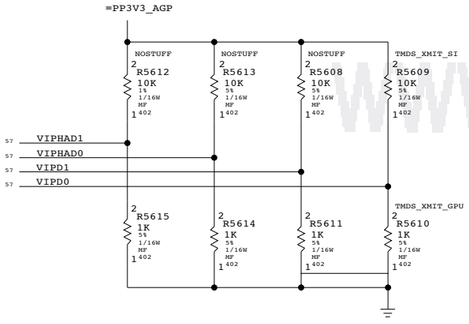
(9) SUB-VENDOR
[0] = [GPU_STRAP<1>]
* 0 = SYSTEM BIOS (VENDOR & SUBSYSTEM ID=0X0000)
1 = ADAPTER CARD VGA BIOS (VENDOR & SUBSYSTEM ID=0X54-0X57)



(10) PCI ADDRESS BUS
[0] = [GPU_STRAP<0>]
0 = REVERSED
* 1 = NORMAL

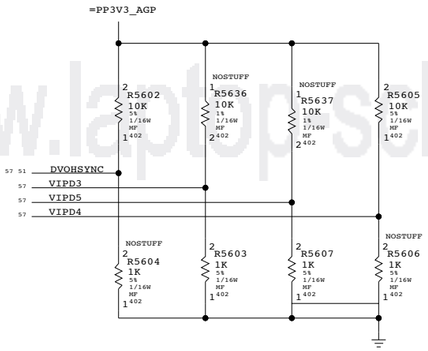


(2) CRYSTAL FREQUENCY SELECT
[1..0] = [VIPD6,VIPD2]
00 = 13.5MHZ
01 = 14.38MHZ
* 10 = 27MHZ
11 = (UNDEFINED)

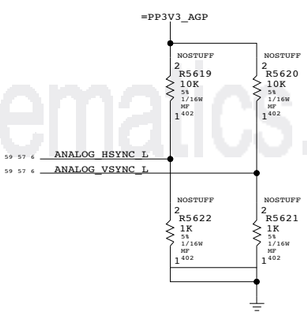


(4) USER DEFINED STRAPS
[3..0] = [VIPHAD1,VIPHAD0,VIPD1,VIPD0]

THESE BITS ARE UNDEFINED BUT THEY
MUST BE KEPT LOW DURING RESET



(3) PCI DEVICE ID
[3..0] = [DVOHSYNC,VIPD3,VIPD5,VIPD4]
0010 = 0X112 GEFORCE2 GO
0011 = 0X113 QUADRO2 GO
0100 = 0X114 NV17M
0000 = 0X110 GEFORCE2GO MX (NV11B)
* 1001 = 0X111 NV18B,NV31,NV34



(7) TV MODE
[1..0] = [ANALOG_HSYNC*,ANALOG_VSYNC*]
00 = SECAM
01 = NTSC
10 = PAL
11 = DISABLED

(THESE RESISTORS ARE ALL NOSTUFF)

NVIDIA STRAPS

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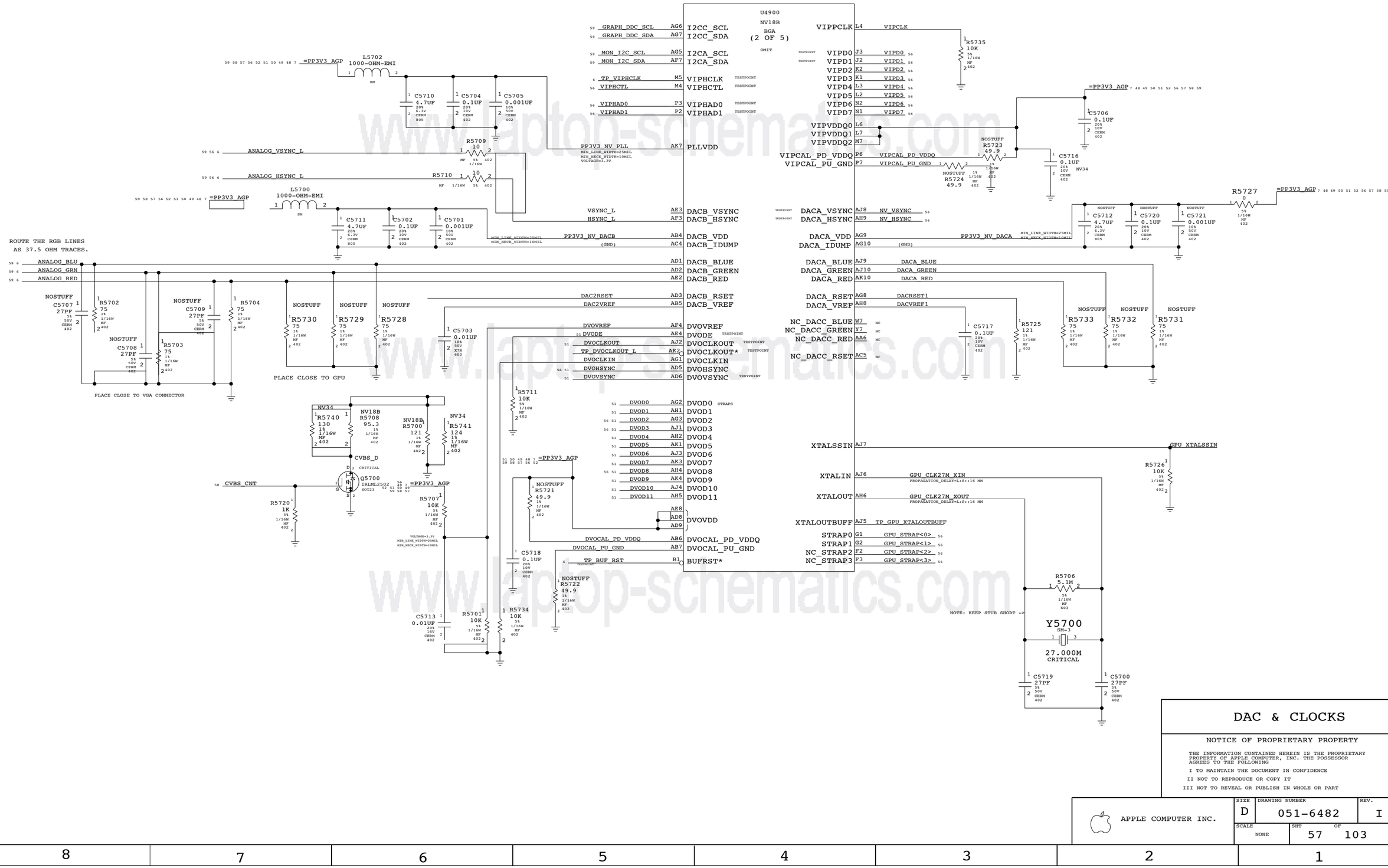
U4900
NV18B
BGA
(2 OF 5)
GMIT
I2CC_SCL
I2CC_SDA
I2CA_SCL
I2CA_SDA
VIPHCLK
VIPHCTL
VIPHAD0
VIPHAD1
PLLVDD
VSYNC_L
HSYNC_L
DACB_VSYNC
DACB_HSYNC
DACB_VDD
DACB_IDUMP
DACB_BLUE
DACB_GREEN
DACB_RED
DACB_RSET
DACB_VREF
DAC2RSET
DAC2VREF
DVOVREF
DVODE
DVOCLKOUT
DVOCLKOUT*
DVOCLKIN
DVOHSYNC
DVOVSYNC
DVOD0
DVOD1
DVOD2
DVOD3
DVOD4
DVOD5
DVOD6
DVOD7
DVOD8
DVOD9
DVOD10
DVOD11
DVOVDD
DVOCAL_PD_VDDQ
DVOCAL_PU_GND
BUFRST*
VIPPCLK
VIPD0
VIPD1
VIPD2
VIPD3
VIPD4
VIPD5
VIPD6
VIPD7
VIPVDDQ0
VIPVDDQ1
VIPVDDQ2
VIPCAL_PD_VDDQ
VIPCAL_PU_GND
DACA_VSYNC
DACA_HSYNC
DACA_VDD
DACA_IDUMP
DACA_BLUE
DACA_GREEN
DACA_RED
DACA_RSET
DACA_VREF
NC_DACC_BLUE
NC_DACC_GREEN
NC_DACC_RED
NC_DACC_RSET
XTALSSIN
XTALIN
XTALOUT
XTALOUTBUFF
STRAP0
STRAP1
NC_STRAP2
NC_STRAP3
GRAPH_DDC_SCL
GRAPH_DDC_SDA
MON_I2C_SCL
MON_I2C_SDA
TP_VIPHCLK
VIPHCTL
VIPHAD0
VIPHAD1
ANALOG_VSYNC_L
ANALOG_HSYNC_L
ANALOG_BLU
ANALOG_GRN
ANALOG_RED
=PP3V3_AGP
PP3V3_NV_PLL
PP3V3_NV_DACB
PP3V3_NV_DACA
L5702 1000-OHM-EMI
L5700 1000-OHM-EMI
R5709 10
R5710 10
C5710 4.7UF
C5704 0.1UF
C5705 0.001UF
C5711 4.7UF
C5702 0.1UF
C5701 0.001UF
C5706 0.1UF
C5716 0.1UF
C5712 4.7UF
C5720 0.1UF
C5721 0.001UF
R5727 0
R5735 10K
R5723 49.9
R5724 49.9
ROUTE THE RGB LINES AS 37.5 OHM TRACES.
R5702 75
R5703 75
R5704 75
C5707 27PF
C5708 27PF
C5709 27PF
PLACE CLOSE TO VGA CONNECTOR
R5730 75
R5729 75
R5728 75
PLACE CLOSE TO GPU
C5703 0.01UF
R5711 10K
C5717 0.1UF
R5725 121
R5733 75
R5732 75
R5731 75
NV34
R5740 130
NV18B R5708 95.3
NV18B R5700 121
NV34 R5741 124
CVBS_D
CVBS_CNT
Q5700 IRLML2502
R5720 1K
R5707 10K
R5721 49.9
R5722 49.9
C5718 0.1UF
C5713 0.01UF
R5701 10K
R5734 10K
R5706 5.1M
Y5700 SM-3 27.000M CRITICAL
C5719 27PF
C5700 27PF
R5726 10K
GPU_XTALSSIN
GPU_CLK27M_XIN
GPU_CLK27M_XOUT
TP_GPU_XTALOUTBUFF
GPU_STRAP<0>
GPU_STRAP<1>
GPU_STRAP<2>
GPU_STRAP<3>
DACRSET1
DACVREF1
NOTE: KEEP STUB SHORT ->
DAC & CLOCKS
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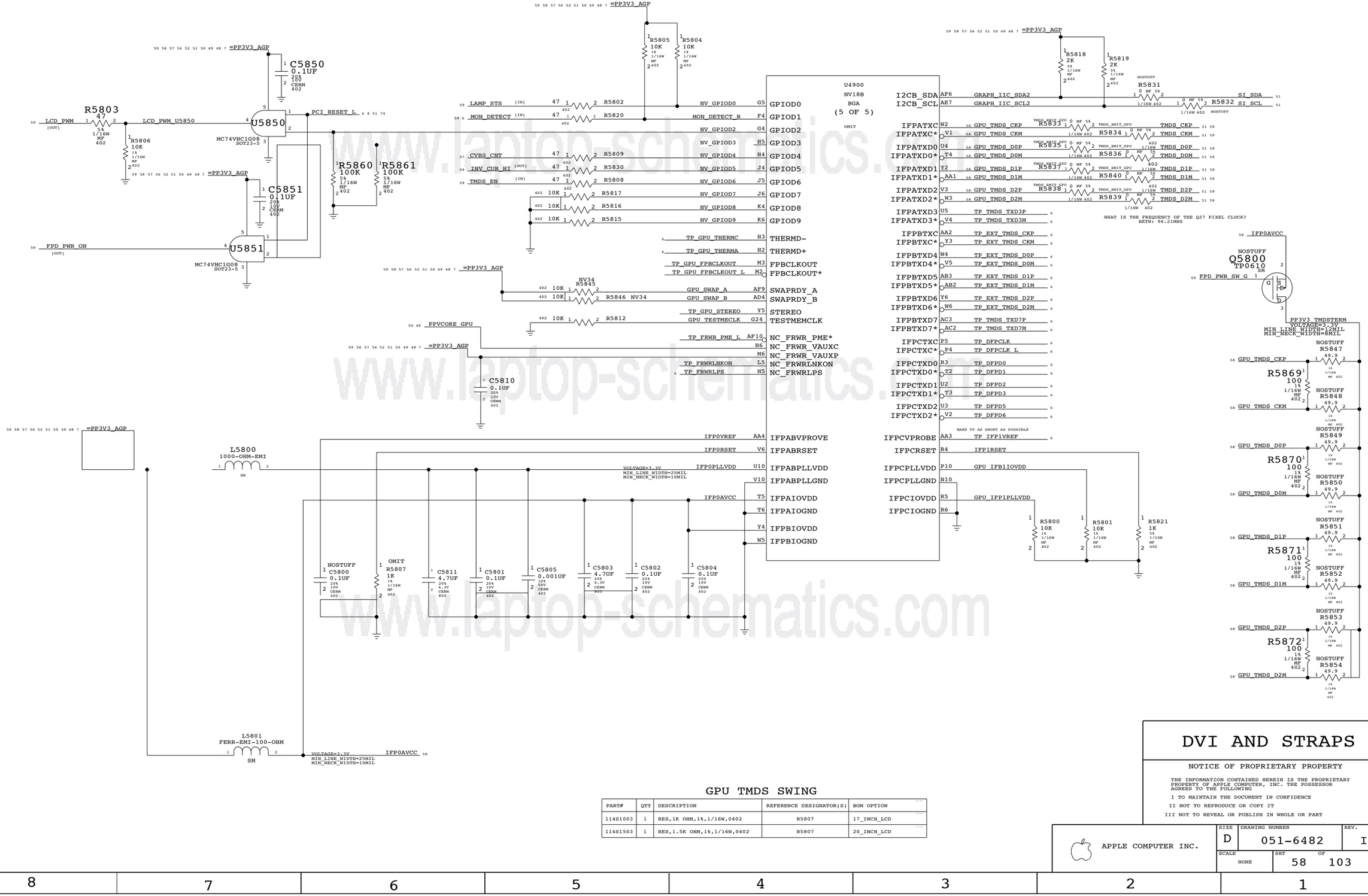
SCALE NONE
SHT 57 OF 103



GPU TMDS SWING

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S1003	1	RES,1K OHM,1%,1/16W,0402	R5807	17_INCH_LCD
114S1503	1	RES,1.5K OHM,1%,1/16W,0402	R5807	20_INCH_LCD

DVI AND STRAPS

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D	051-6482	I
SCALE: NONE	SHT 58 OF 103	

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EXTERNAL VGA CONNECTOR

ANALOG_HSYNC_L
ANALOG_VSYNC_L
C5907 22PF 5% 50V CERM 402
C5908 22PF 5% 50V CERM 402
D5900 BAV99DW SOT-363 NOSTUFF
=PP5V_AGP 7 49 50 59
GND_CHASSIS_VGA 7 59
CRITICAL (514-0201)
J5903 DV01793 F-ST-TH
CHECK RGB RETURN PINS
FL1702 LCFILTER SM-100MHZ — ANALOG_RED
FL1701 LCFILTER SM-100MHZ — ANALOG_GRN
FL1700 LCFILTER SM-100MHZ — ANALOG_BLU
MON_DETECT
FILT_ANALOG_RED
FILT_ANALOG_GRN
FILT_ANALOG_BLU
(RED_RTN)
(GRN_RTN)
(BLU_RTN)
DDC_VCC_5
VGA_IIC_DAT
VGA_IIC_CLK
VOLTAGE=5V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
L5903 FERR-220-OHM 0805
PP5V_USB2 92
C5902 0.01UF 10% 16V CERM 402
C5905 0.01UF 10% 16V CERM 402
C5904 0.01UF 10% 16V CERM 402
C5903 0.01UF 10% 16V CERM 402
ROUTE THE ANALOG RGB TRACES AT 37.5 OHMS.
R5911 2K 5% 1/16W MF 402
R5910 2K 5% 1/16W MF 402
D5902 BAV99DW SOT-363 NOSTUFF
=PP5V_AGP 7 49 50 59
GND_CHASSIS_VGA 7 59
MON_I2C_SDA
MON_I2C_SCL
R5908 33 5% 1/16W MF 402
R5909 33 5% 1/16W MF 402
C5909 47PF 5% 50V CERM 402
C5906 47PF 5% 50V CERM 402

INTERNAL TMDS CONNECTOR

SDF5900 STDOFF-118OD-181H-TH (516S0241)
J5902 53307-3072 F-ST-SM
TD0M
TD0P
TD2M
TD2P
PPVCC_TMDS VOLTAGE=3.3V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
PP3V3_DDC VOLTAGE=3.3V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
TCKM
TCKP
TD1M
TD1P
TMDS_DDC_DAT
TMDS_DDC_CLK
C5916 10UF 10% 16V CERM 1210
C5900 0.01UF 10% 16V CERM 402
GND_CHASSIS_TMDS
SDF5901 STDOFF-118OD-181H-TH
GRAPH_DDC_SDA
GRAPH_DDC_SCL
R5906 33 5% 1/16W MF 402
R5907 2K 5% 1/16W MF 402
R5905 2K 5% 1/16W MF 402
R5900 33 5% 1/16W MF 402
=PP3V3_AGP
L5901 FERR-220-OHM 0805
PP3V3_DDC
C5901 0.01UF 10% 16V CERM 402

INVERTER INTERFACE

20" LCD INVERTER NEED +24V.
17" LCD INVERTER NEED +12V.

Q5903 SI3433DV TSOP
=PP5V_AGP
Q5903_GATE
R5920 100K 5% 1/16W MF 402
R5921 10K 5% 1/16W MF 402
Q5902_DRAIN
R5919 200K 5% 1/16W MF 402
D5901 1N914 SOT23 NOSTUFF
Q5902_GATE
R5916 100K 5% 1/16W MF 402
Q5902 2N7002 SM
=PP12V_AGP
PP5V_AGP_P_SEQ
LCD_PWM
LAMP_STS
INV_CUR_HI
L5904 FERR-220-OHM 0805
L5905 FERR-220-OHM 0805
L5906 FERR-220-OHM 0805
L5907 FERR-220-OHM 0805
L5911 FERR-220-OHM 0805
L5912 FERR-220-OHM 0805
C5921 10UF 20% 16V ELEC SM
C5922 10UF 20% 16V ELEC SM
C5910 0.01UF 20% 50V CERM 603
C5913 0.01UF 20% 50V CERM 603
C5911 0.01UF 20% 50V CERM 603
C5912 220PF 5% 25V CERM 603
C5914 0.01UF 20% 50V CERM 603
C5915 0.01UF 20% 50V CERM 603
GND_CHASSIS_17_INCH_INVERTER
J5900 42375 M-ST-TH 518-0135
PP12V_INV
GND_17_INV
PP5V_AGP_RL
INV_17_LCD_PWM_F
LAMP_STS_F
INV_17_CUR_HI_F

R5926 0 5% 1/16W MF 402 NOSTUFF
L5902 90-OHM-SM SYM_VER-1
R5904 301 1% 1/16W MF 402
R5927 0 5% 1/16W MF 402 NOSTUFF
TMDS_D2M
TMDS_D2P
TD2M
TD2P
R5928 0 5% 1/16W MF 402 NOSTUFF
L5908 90-OHM-SM SYM_VER-1
R5903 301 1% 1/16W MF 402
R5929 0 5% 1/16W MF 402 NOSTUFF
TMDS_D1M
TMDS_D1P
TD1M
TD1P
R5930 0 5% 1/16W MF 402 NOSTUFF
L5909 90-OHM-SM SYM_VER-1
R5902 301 1% 1/16W MF 402
R5931 0 5% 1/16W MF 402 NOSTUFF
TMDS_D0M
TMDS_D0P
TD0M
TD0P
R5932 0 5% 1/16W MF 402 NOSTUFF
L5910 90-OHM-SM SYM_VER-1
R5901 301 1% 1/16W MF 402
R5933 0 5% 1/16W MF 402 NOSTUFF
TMDS_CKM
TMDS_CKP
TCKM
TCKP

PP3V3_ALL
PP3V3_RUN
PP12V_RUN
R5950 0 5% 1/8W FF 1206 17_INCH_LCD
R5923 0 5% 1/8W FF 1206 NOSTUFF
R5922 0 5% 1/8W FF 1206 20_INCH_LCD
PPVCC_FPD
Q5900 IRF7410 SO-8 17_INCH_LCD
376S0082
FPD_PWR_SW_G
FPD_PWR_SW_S
VOLTAGE=3.3V MIN_LINE_WIDTH=25MIL MIN_NECK_WIDTH=10MIL
C5919 0.01UF 20% 16V CERM 402
C5918 0.022UF 20% 16V CERM 402
R5925 100K 5% 1/16W MF 402
R5934 0 5% 1/8W FF 1206 NOSTUFF
R5935 0 5% 1/8W FF 1206 NOSTUFF
L5900 FERR-220-OHM 0805 20_INCH_LCD
PPVCC_TMDS
OMIT R5913 10K 5% 1/16W MF 402
D5914 1N914 SOT23
C5917 10UF 10% 16V CERM 1210
R5960 10K 5% 1/16W MF 402
OMIT R5912 330 5% 1/16W MF 603
LED5900_P1
LED5900 GREEN 2.0X1.25A
SILKSCREEN: 3
FPD_PWR_ON_D
TMDS_EN_R
Q5901 2N7002 SM
FPD_PWR_ON
R5915 100K 5% 1/16W MF 402
R5914 10K 5% 1/16W MF 402
TMDS_EN
DZ5900 1N5227B SOT23 20_INCH_LCD

=PP24V_GRAPHICS
L5913 FERR-220-OHM 0805 20_INCH_LCD
L5914 FERR-220-OHM 0805 20_INCH_LCD
L5915 FERR-220-OHM 0805 20_INCH_LCD
L5916 FERR-220-OHM 0805 20_INCH_LCD
LCD_PWM
INV_CUR_HI
C5947 1UF 20% 50V CERM 1210 NOSTUFF
C5942 1UF 20% 50V CERM 1210 20_INCH_LCD
VOLTAGE=24V MIN_LINE_WIDTH=100MIL MIN_NECK_WIDTH=10MIL
VOLTAGE=5V MIN_LINE_WIDTH=100MIL MIN_NECK_WIDTH=10MIL
PP24V_INV
GND_20_INV
INV_20_LCD_PWM
INV_20_CUR_HI_F
NOTE:REMOVED 2 PINS:LAMP_STATUS & ON/OFF FOR 20" LCD INVETER.
C5943 0.01UF 20% 50V CERM 603 20_INCH_LCD
C5944 0.01UF 20% 50V CERM 603 20_INCH_LCD
C5945 220PF 5% 25V CERM 603 20_INCH_LCD
C5946 0.01UF 20% 50V CERM 603 20_INCH_LCD
GND_CHASSIS_20_INCH_INVERTER
J5901 53048 RT-S-TH 518-0141

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,10K OHM,1/16W,5%,0402	R5913	17_INCH_LCD
116S1105	1	RES,100K OHM,1/16W,5%,0402	R5913	20_INCH_LCD
113S1332	1	RES,330 OHM,1/16W,5%,0603	R5912	17_INCH_LCD
113S1123	1	RES,1.2K OHM,1/16W,5%,0603	R5912	20_INCH_LCD
376S0225	1	XSTR,MOSFET,P-CH,0.02OHM	Q5900	20_INCH_LCD
101S1000	1	RES,0 OHM,1/10W,5%,0805	L5900	17_INCH_LCD

EXT VGA / TMDS AND INVERTER

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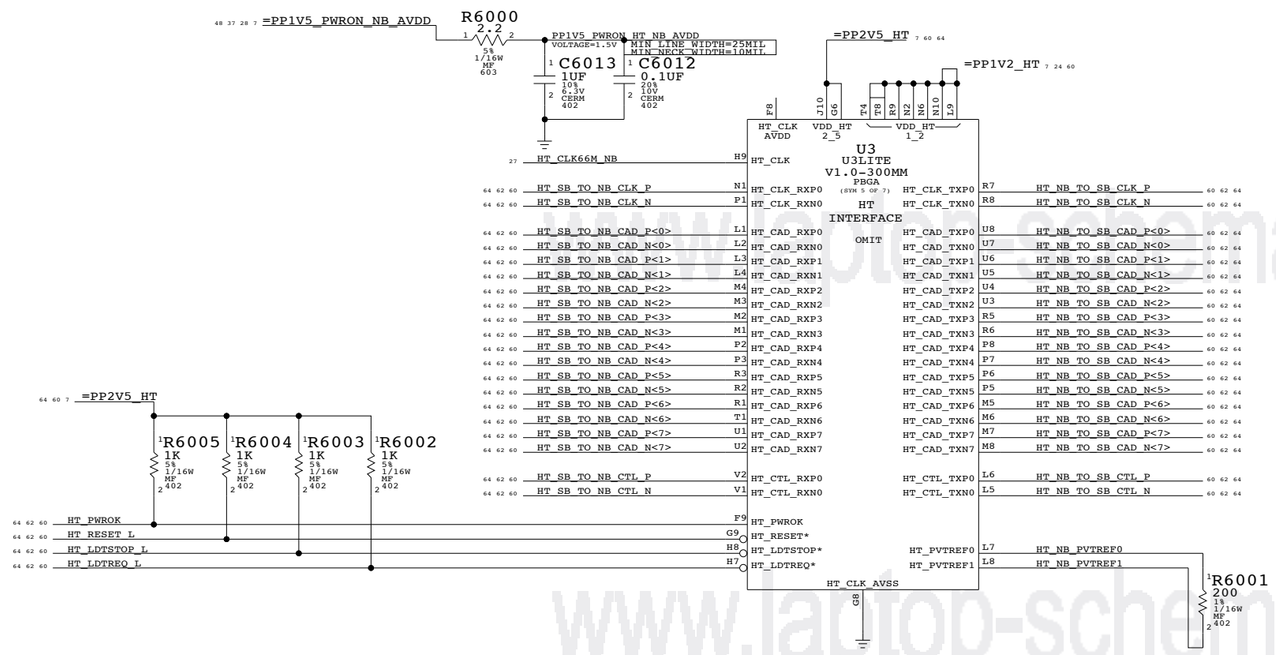
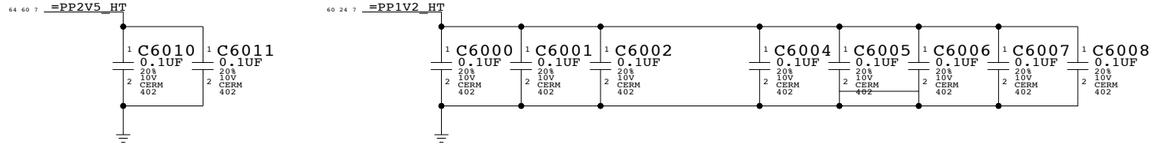
SCALE: NONE	SHT 59 OF 103	





	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
HT_NB_TO_SB_CLK_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	146
HT_NB_TO_SB_CLK_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CLK	147
HT_NB_TO_SB_CTL_P	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	183
HT_NB_TO_SB_CTL_N	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CTL	182
HT_NB_TO_SB_CAD_P<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	151
HT_NB_TO_SB_CAD_N<0>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD0	150
HT_NB_TO_SB_CAD_P<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	152
HT_NB_TO_SB_CAD_N<1>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD1	153
HT_NB_TO_SB_CAD_P<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	154
HT_NB_TO_SB_CAD_N<2>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD2	155
HT_NB_TO_SB_CAD_P<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	156
HT_NB_TO_SB_CAD_N<3>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD3	157
HT_NB_TO_SB_CAD_P<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	158
HT_NB_TO_SB_CAD_N<4>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD4	159
HT_NB_TO_SB_CAD_P<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	160
HT_NB_TO_SB_CAD_N<5>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD5	161
HT_NB_TO_SB_CAD_P<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	162
HT_NB_TO_SB_CAD_N<6>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD6	163
HT_NB_TO_SB_CAD_P<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	164
HT_NB_TO_SB_CAD_N<7>	HT_NB_TO_SB	HT_NB_TO_SB	HT_NB_TO_SB_CAD7	165
HT_SB_TO_NB_CLK_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	148
HT_SB_TO_NB_CLK_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CLK	149
HT_SB_TO_NB_CTL_P	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	184
HT_SB_TO_NB_CTL_N	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CTL	185
HT_SB_TO_NB_CAD_P<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	166
HT_SB_TO_NB_CAD_N<0>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD0	167
HT_SB_TO_NB_CAD_P<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	168
HT_SB_TO_NB_CAD_N<1>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD1	169
HT_SB_TO_NB_CAD_P<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	170
HT_SB_TO_NB_CAD_N<2>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD2	171
HT_SB_TO_NB_CAD_P<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	172
HT_SB_TO_NB_CAD_N<3>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD3	173
HT_SB_TO_NB_CAD_P<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	174
HT_SB_TO_NB_CAD_N<4>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD4	175
HT_SB_TO_NB_CAD_P<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	176
HT_SB_TO_NB_CAD_N<5>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD5	177
HT_SB_TO_NB_CAD_P<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	178
HT_SB_TO_NB_CAD_N<6>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD6	179
HT_SB_TO_NB_CAD_P<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	180
HT_SB_TO_NB_CAD_N<7>	HT_SB_TO_NB	HT_SB_TO_NB	HT_SB_TO_NB_CAD7	181
HT_PWROK	HT_PWROK	HT_2V5		186
HT_RESET_L	HT_CTL	HT_2V5		187
HT_LDTSTOP_L	HT_CTL	HT_2V5		188
HT_LDTREQ_L	HT_CTL	HT_2V5		189

HT_NB_TO_SB HT_SB_TO_NB
5 MIL SPACING FOR DIFF PAIR
10 MIL SPACING TO ANYTHING ELSE

HT_2V5
4 MIL SPACING IN GROUP
8 MIL SPACING TO ANYTHING ELSE

LENGTH TOLERENCE CAN BE LOOSE
MATCHED GROUP CONSTRAINT IS TIGHT ENOUGH

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U3LITE HT

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	15_MIL_SPACING	

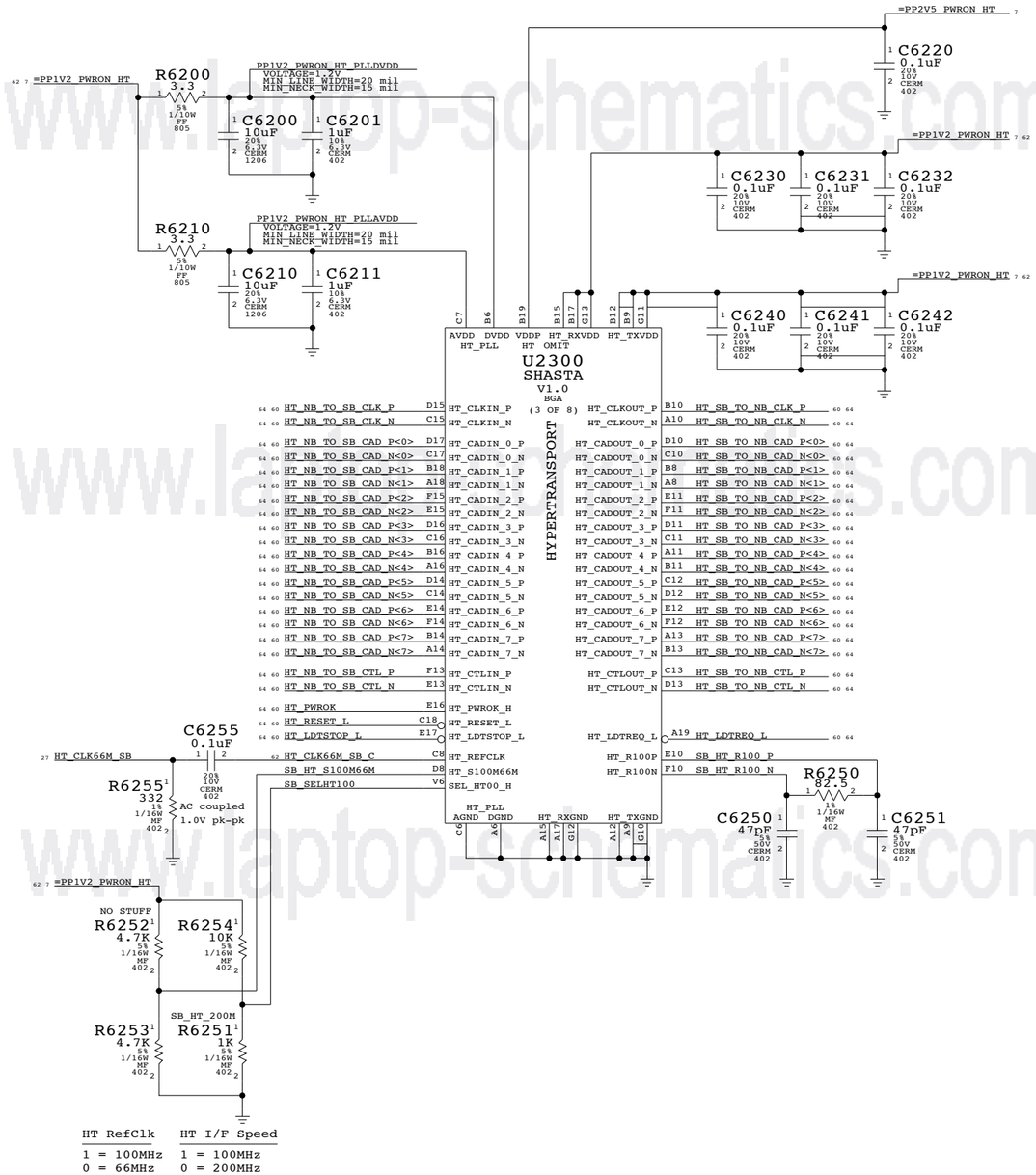
HT_CLK66M_SB_C 62

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_HT
- _PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.



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Master: Link

Shasta HyperTransport

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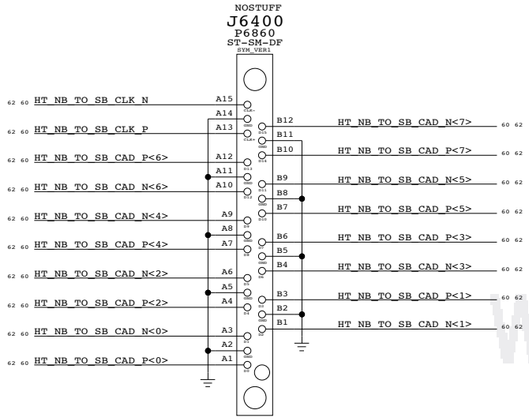
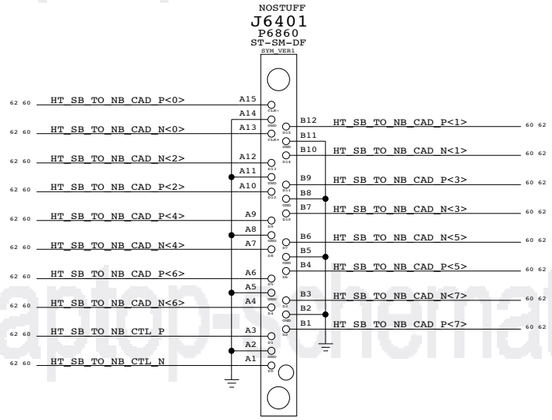
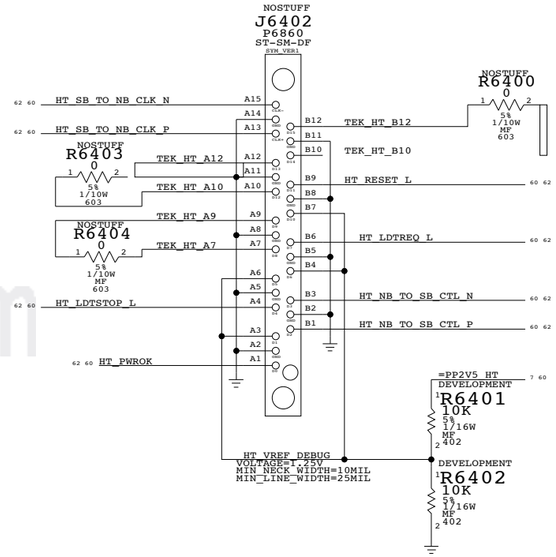
	SCALE	SHT OF	
	NONE	62 103	

SAME CONNECTORS & PINOUT AS

Q37 HYPERTRANSPORT BETWEEN GOLEM AND K2







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HT DEBUG CONN

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ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

74	PCI_SB_AD<0>	RP7300	2	7	47	PCI_AD<0>	6 74 75 76 77
74	PCI_SB_AD<1>	RP7303	1	8	47	PCI_AD<1>	6 74 75 76 77
74	PCI_SB_AD<2>	RP7303	2	7	47	PCI_AD<2>	6 74 75 76 77
74	PCI_SB_AD<3>	RP7303	4	5	47	PCI_AD<3>	6 74 75 76 77
74	PCI_SB_AD<4>	RP7309	2	7	47	PCI_AD<4>	6 74 75 76 77
74	PCI_SB_AD<5>	RP7300	1	8	47	PCI_AD<5>	6 74 75 76 77
74	PCI_SB_AD<6>	RP7300	3	6	47	PCI_AD<6>	6 74 75 76 77
74	PCI_SB_AD<7>	RP7309	4	5	47	PCI_AD<7>	6 74 75 76 77
74	PCI_SB_AD<8>	RP7300	4	5	47	PCI_AD<8>	6 74 75 76 77
74	PCI_SB_AD<9>	RP7301	2	7	47	PCI_AD<9>	6 74 75 76 77
74	PCI_SB_AD<10>	RP7301	1	8	47	PCI_AD<10>	6 74 75 76 77
74	PCI_SB_AD<11>	RP7301	4	5	47	PCI_AD<11>	6 74 75 76 77
74	PCI_SB_AD<12>	RP7309	1	8	47	PCI_AD<12>	6 74 75 76 77
74	PCI_SB_AD<13>	RP7309	3	6	47	PCI_AD<13>	6 74 75 76 77
74	PCI_SB_AD<14>	RP7301	3	6	47	PCI_AD<14>	6 74 75 76 77
74	PCI_SB_AD<15>	RP7307	1	8	47	PCI_AD<15>	6 74 75 76 77
74	PCI_SB_AD<16>	RP7308	1	8	47	PCI_AD<16>	6 74 75 76 77

R7300
47
5%
1/16W
MF
402

76 74	PCI_SB_AD<17>		1	2		PCI_AD<17>	6 74 75 76 77

74	PCI_SB_AD<18>	RP7307	2	7	47	PCI_AD<18>	6 74 75 76 77
74	PCI_SB_AD<19>	RP7306	3	6	47	PCI_AD<19>	6 74 75 76 77
74	PCI_SB_AD<20>	RP7305	1	8	47	PCI_AD<20>	6 74 75 76 77
74	PCI_SB_AD<21>	RP7305	2	7	47	PCI_AD<21>	6 74 76 77
74	PCI_SB_AD<22>	RP7302	1	8	47	PCI_AD<22>	6 74 76 77
74	PCI_SB_AD<23>	RP7302	3	6	47	PCI_AD<23>	6 74 76 77
74	PCI_SB_AD<24>	RP7304	1	8	47	PCI_AD<24>	6 74 75 76 77
74	PCI_SB_AD<25>	RP7306	4	5	47	PCI_AD<25>	6 74 75 76 77
74	PCI_SB_AD<26>	RP7305	3	6	47	PCI_AD<26>	6 74 75 76 77

R7301
47
5%
1/16W
MF
402

77 74	PCI_SB_AD<27>		1	2		PCI_AD<27>	6 74 75 76 77

74	PCI_SB_AD<28>	RP7302	2	7	47	PCI_AD<28>	6 74 75 76 77
74	PCI_SB_AD<29>	RP7304	4	5	47	PCI_AD<29>	6 74 75 76 77
74	PCI_SB_AD<30>	RP7302	4	5	47	PCI_AD<30>	6 74 75 76 77
74	PCI_SB_AD<31>	RP7304	2	7	47	PCI_AD<31>	6 74 75 76 77
74	PCI_SB_CBE_L<0>	RP7303	3	6	47	PCI_CBE_L<0>	6 74 76 77
74	PCI_SB_CBE_L<1>	RP7306	2	7	47	PCI_CBE_L<1>	6 74 76 77
74	PCI_SB_CBE_L<2>	RP7305	4	5	47	PCI_CBE_L<2>	6 74 76 77
74	PCI_SB_CBE_L<3>	RP7304	3	6	47	PCI_CBE_L<3>	6 74 76 77
74	PCI_SB_DEVSEL_L	RP7306	1	8	47	PCI_DEVSEL_L	6 74 76 77
74	PCI_SB_FRAME_L	RP7307	4	5	47	PCI_FRAME_L	6 74 76 77
74	PCI_SB_IRDY_L	RP7307	3	6	47	PCI_IRDY_L	6 74 76 77
74	PCI_SB_TRDY_L	RP7308	3	6	47	PCI_TRDY_L	6 74 76 77
74	PCI_SB_STOP_L	RP7308	4	5	47	PCI_STOP_L	6 74 76 77
74	PCI_SB_PAR	RP7308	2	7	47	PCI_PAR	6 74 76 77

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

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PCI SERIES TERMINATION

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PCI_AD			PCI_AD<31..28> 6 73 75 76 77
PCI_AD27			PCI_AD<27> 6 73 75 76 77
PCI_AD			PCI_AD<26..24> 6 73 75 76 77
PCI_AD23			PCI_AD<23> 6 73 76 77
PCI_AD22			PCI_AD<22> 6 73 76 77
PCI_AD21			PCI_AD<21> 6 73 76 77
PCI_AD20			PCI_AD<20> 6 73 75 76 77
PCI_AD			PCI_AD<19..18> 6 73 75 76 77
PCI_AD17			PCI_AD<17> 6 73 75 76 77
PCI_AD			PCI_AD<16..0> 6 73 75 76 77
PCI			PCI_CBE_L<3..0> 6 73 76 77
PCI			PCI_PAR 6 73 76 77
PCI_CTL			PCI_DEVSEL_L 6 73 74 76 77
PCI_CTL			PCI_FRAME_L 6 73 74 76 77
PCI_CTL			PCI_IRDY_L 6 73 74 76 77
PCI_CTL			PCI_TRDY_L 6 73 74 76 77
PCI_CTL			PCI_STOP_L 6 73 74 76 77

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_SB_PCI (can be _PP3V3_PCI)
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

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7 =PP3V3_SB_PCI

NO STUFF C7410 10uF 20% 6.3V CERM 805
C7400 0.1uF 20% 10V CERM 402
C7401 0.1uF 20% 10V CERM 402
C7402 0.1uF 20% 10V CERM 402
C7403 0.1uF 20% 10V CERM 402
C7404 0.1uF 20% 10V CERM 402

NO STUFF C7411 10uF 20% 6.3V CERM 805
C7405 0.1uF 20% 10V CERM 402
C7406 0.1uF 20% 10V CERM 402
C7407 0.1uF 20% 10V CERM 402
C7408 0.1uF 20% 10V CERM 402
C7409 0.1uF 20% 10V CERM 402

=PP2V5_PWRON_SB 7 23 25 88

C7420 0.1uF 20% 10V CERM 402
C7421 0.1uF 20% 10V CERM 402
C7422 0.1uF 20% 10V CERM 402
C7423 0.1uF 20% 10V CERM 402

VDDOPC: AA22, B22, E21, H16, J21, M16, N21, R20, U21, V19
PCIVDDP: B20, J14, N20, U20

U2300 SHASTA V1.0 BGA (4 OF 8) OMIT

27 PCI_CLK66M_SB_INT	AB9	PCIBR_CLK_H	
27 8 PCI_CLK33M_SB_EXT	U19	PCI1CLK_H	

PCI

PCI1AD_0_H	L18	PCI_SB_AD<0>	73
PCI1AD_1_H	K19	PCI_SB_AD<1>	73
PCI1AD_2_H	L22	PCI_SB_AD<2>	73
PCI1AD_3_H	M22	PCI_SB_AD<3>	73
PCI1AD_4_H	M18	PCI_SB_AD<4>	73
PCI1AD_5_H	L20	PCI_SB_AD<5>	73
PCI1AD_6_H	M21	PCI_SB_AD<6>	73
PCI1AD_7_H	N16	PCI_SB_AD<7>	73
PCI1AD_8_H	M20	PCI_SB_AD<8>	73
PCI1AD_9_H	P22	PCI_SB_AD<9>	73
PCI1AD_10_H	M17	PCI_SB_AD<10>	73
PCI1AD_11_H	N18	PCI_SB_AD<11>	73
PCI1AD_12_H	M19	PCI_SB_AD<12>	73
PCI1AD_13_H	N19	PCI_SB_AD<13>	73
PCI1AD_14_H	P21	PCI_SB_AD<14>	73
PCI1AD_15_H	R22	PCI_SB_AD<15>	73
PCI1AD_16_H	P20	PCI_SB_AD<16>	73
PCI1AD_17_H	V21	PCI_SB_AD<17>	73 76
PCI1AD_18_H	P18	PCI_SB_AD<18>	73
PCI1AD_19_H	T20	PCI_SB_AD<19>	73
PCI1AD_20_H	R16	PCI_SB_AD<20>	73
PCI1AD_21_H	R17	PCI_SB_AD<21>	73
PCI1AD_22_H	W21	PCI_SB_AD<22>	73
PCI1AD_23_H	Y22	PCI_SB_AD<23>	73
PCI1AD_24_H	R18	PCI_SB_AD<24>	73
PCI1AD_25_H	T19	PCI_SB_AD<25>	73
PCI1AD_26_H	T18	PCI_SB_AD<26>	73
PCI1AD_27_H	Y21	PCI_SB_AD<27>	73 77
PCI1AD_28_H	W20	PCI_SB_AD<28>	73
PCI1AD_29_H	T16	PCI_SB_AD<29>	73
PCI1AD_30_H	AA21	PCI_SB_AD<30>	73
PCI1AD_31_H	T17	PCI_SB_AD<31>	73
PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	73
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	73
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	73
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	73
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	73
PCI1FRAME_L	T21	PCI_SB_FRAME_L	73
PCI1IRDY_L	R21	PCI_SB_IRDY_L	73
PCI1TRDY_L	P19	PCI_SB_TRDY_L	73
PCI1STOP_L	P17	PCI_SB_STOP_L	73
PCI1PAR_H	N17	PCI_SB_PAR	73
PCI1RST_L	U18	SB_PCI_RESET_L	

"Slot A" - AD17
76 74 6 PCI_SLOTA_REQ_L AB18 PCI1REQ_0_L
76 74 6 PCI_SLOTA_GNT_L AA18 PCI1GNT_0_L

"Slot G" - AD27
77 74 PCI_SLOTG_REQ_L AB20 PCI1REQ_1_L
77 74 PCI_SLOTG_GNT_L AB19 PCI1GNT_1_L

"Slot D" - AD20
74 PCI_SLOTD_REQ_L V17 PCI1REQ_2_L
74 PCI_SLOTD_GNT_L V18 PCI1GNT_2_L

76 75 6 ROM_CS_L AB8 ROMCS_L
76 75 6 ROM_OE_L AA9 ROMOE_L
76 75 6 ROM_WE_L Y10 ROMRW_L

=PP3V3_PCI 7 25 74 75 76 77

RP7400 4.7K 5% 1/16W SM1 2 7 PCI_SLOTA_REQ_L 6 74 76
RP7400 4.7K 5% 1/16W SM1 1 8 PCI_SLOTA_GNT_L 6 74 76
RP7400 4.7K 5% 1/16W SM1 4 5 PCI_SLOTG_REQ_L 74 77
RP7400 4.7K 5% 1/16W SM1 3 6 PCI_SLOTG_GNT_L 74 77
RP7401 4.7K 5% 1/16W SM1 3 6 PCI_SLOTD_REQ_L 74
RP7401 4.7K 5% 1/16W SM1 4 5 PCI_SLOTD_GNT_L 74

=PP3V3_PWRON_SB 7 23 25

R7455 4.7K 5% 1/16W MF 402
C7450 0.1uF 20% 10V CERM 402
R7450 4.7K 5% 1/16W MF 402

U7450 MC74VHC1G08 SOT23-5

87 77 25 8 SYS_WARM_RESET_L
Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.

PCI_RESET_L 6 8 51 58

77 76 75 74 25 7 =PP3V3_PCI

RP7402 4.7K 5% 1/16W SM1 3 6 77 76 74 73 6 PCI_DEVSEL_L
RP7402 4.7K 5% 1/16W SM1 4 5 77 76 74 73 6 PCI_FRAME_L
RP7402 4.7K 5% 1/16W SM1 2 7 77 76 74 73 6 PCI_IRDY_L
RP7402 4.7K 5% 1/16W SM1 1 8 77 76 74 73 6 PCI_TRDY_L
RP7401 4.7K 5% 1/16W SM1 7 2 77 76 74 73 6 PCI_STOP_L

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Shasta PCI Interface

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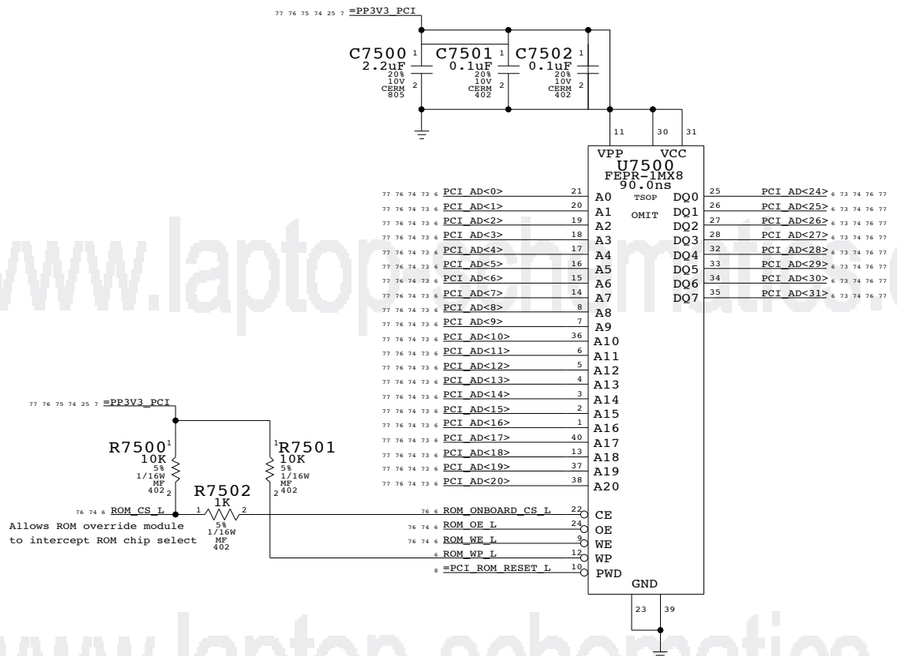
Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



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BootROM

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SCALE: NONE	SHT 75 OF 103	

DRAWING

LAST_MODIFIED=Mon Dec 13 20:02:34 2004

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 8 76

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

77 75 74 25 7 =PP3V3_PCI

C7600 10UF 20% 6.3V CERM 1206 — NO STUFF
C7601 10UF 20% 6.3V CERM 1206 — NO STUFF
C7602 0.1UF 20% 10V CERM 402
C7603 0.1UF 20% 10V CERM 402

CRITICAL
J7600
RCPT-CARD-EDGE
P-ST-TH1

SIDE-A		SIDE-B	
8 PCI_AIRPORT_RESET_L	1	2	
6 TP_AIRPORT_RF_DISABLE	3	4	PCI_CLK33M_AIRPORT 8 76
74 6 PCI_SLOTA_REQ_L	5	6	
	7	8	PCI_SLOTA_GNT_L 6 74
77 75 74 73 6 PCI_AD<31>	9	10	TP_AIRPORT_PME_L 6
	11	12	PCI_SLOTA_INT_L 6 25
77 75 74 73 6 PCI_AD<29>	13	14	PCI_AD<30> 6 73 74 75 77
77 75 74 73 6 PCI_AD<27>	15	16	
77 75 74 73 6 PCI_AD<25>	17	18	PCI_AD<28> 6 73 74 75 77
	19	20	PCI_AD<26> 6 73 74 75 77
77 74 73 6 PCI_CBE_L<3>	21	22	PCI_AD<24> 6 73 74 75 77
	23	24	6 PCI_SLOTA_IDSEL
77 74 73 6 PCI_AD<23>	25	26	
77 74 73 6 PCI_AD<21>	27	28	PCI_AD<22> 6 73 74 77
77 75 74 73 6 PCI_AD<19>	29	30	PCI_AD<20> 6 73 74 75 77
	31	32	PCI_PAR 6 73 74 77
77 75 74 73 6 PCI_AD<17>	33	34	PCI_AD<18> 6 73 74 75 77
	35	36	PCI_AD<16> 6 73 74 75 77
77 74 73 6 PCI_CBE_L<2>	37	38	
77 74 73 6 PCI_IRDY_L	39	40	PCI_FRAME_L 6 73 74 77
	41	42	PCI_TRDY_L 6 73 74 77
6 AIRPORT_CLKRUN_L_PD	43	44	PCI_STOP_L 6 73 74 77
	45	46	PCI_DEVSEL_L 6 73 74 77
77 74 73 6 PCI_CBE_L<1>	47	48	
77 75 74 73 6 PCI_AD<14>	49	50	PCI_AD<15> 6 73 74 75 77
	KEY		
	51	52	PCI_AD<13> 6 73 74 75 77
77 75 74 73 6 PCI_AD<12>	53	54	PCI_AD<11> 6 73 74 75 77
77 75 74 73 6 PCI_AD<10>	55	56	
75 74 6 ROM_WE_L	57	58	PCI_AD<9> 6 73 74 75 77
77 75 74 73 6 PCI_AD<8>	59	60	PCI_CBE_L<0> 6 73 74 77
77 75 74 73 6 PCI_AD<7>	61	62	ROM_OE_L 6 74 75
	63	64	PCI_AD<6> 6 73 74 75 77
77 75 74 73 6 PCI_AD<5>	65	66	
75 6 ROM_ONBOARD_CS_L	67	68	PCI_AD<4> 6 73 74 75 77
77 75 74 73 6 PCI_AD<3>	69	70	PCI_AD<2> 6 73 74 75 77
	71	72	PCI_AD<0> 6 73 74 75 77
77 75 74 73 6 PCI_AD<1>	73	74	
75 74 6 ROM_CS_L	75	76	NC
	NC 77	78	NC — RESERVED FOR USB_DP AND USB_DN
	NC 79	80	
	NC 81	82	NC
	83	84	NC
	85	86	NC
	NC 87	88	NC
	89	90	NC — RESERVED FOR RADIO_IO
	NC 91	92	NC
	NC 93	94	NC
	NC 95	96	NC
	97	98	NC
	NC 99	100	NC

516-0069

R7600 22 5% 1/16W MF 402
1 — 2 PCI_SB_AD<17> 73 74

R7612 0 5% 1/16W MF 402
94 25 6 I2S1_MCLK SCC_RTS_L — I2S1_MCLK_MARTY
I2S1_DEV_TO_SB_DTI_MARTY

R7610 0 5% 1/16W MF 402
94 25 6 I2S1_DEV_TO_SB_DTI SCC_RXDA

I2S1_SB_TO_DEV_DTO_MARTY

R7611 0 5% 1/16W MF 402
94 25 6 I2S1_SB_TO_DEV_DTO SCC_TXDA

PP5V_PWRON_AIRPORT_MARTY
MIN_LINE_WIDTH=25MIL
MIN_NECK_WIDTH=10MIL

R7601 10K 5% 1/16W MF 402 — 1 — 2

7 =PP5V_PWRON_AIRPORT

R7613 0 5% 1/16W MF 402

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AirPort Extreme

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 76 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_USB2	CLOCKS	

=PCI_CLK33M_USB2 8 77

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

7 =PPVIO_PCI_USB2

C7703 0.1uF 20% 10V CERM 402

VDD_PCI

CRITICAL
U7700
NEC_uPD720101_USB2
FBGA

76 75 74 73 6 PCI_AD<0>	M5	AD0	
76 75 74 73 6 PCI_AD<1>	P5	AD1	
76 75 74 73 6 PCI_AD<2>	N5	AD2	
76 75 74 73 6 PCI_AD<3>	P4	AD3	
76 75 74 73 6 PCI_AD<4>	N4	AD4	
76 75 74 73 6 PCI_AD<5>	M3	AD5	
76 75 74 73 6 PCI_AD<6>	N3	AD6	
76 75 74 73 6 PCI_AD<7>	M1	AD7	
76 75 74 73 6 PCI_AD<8>	L2	AD8	
76 75 74 73 6 PCI_AD<9>	L1	AD9	
76 75 74 73 6 PCI_AD<10>	K2	AD10	
76 75 74 73 6 PCI_AD<11>	L3	AD11	
76 75 74 73 6 PCI_AD<12>	K1	AD12	
76 75 74 73 6 PCI_AD<13>	K3	AD13	
76 75 74 73 6 PCI_AD<14>	J2	AD14	
76 75 74 73 6 PCI_AD<15>	J1	AD15	
76 75 74 73 6 PCI_AD<16>	F2	AD16	
76 75 74 73 6 PCI_AD<17>	E3	AD17	
76 75 74 73 6 PCI_AD<18>	E1	AD18	
76 75 74 73 6 PCI_AD<19>	D3	AD19	
76 75 74 73 6 PCI_AD<20>	D1	AD20	
76 74 73 6 PCI_AD<21>	D2	AD21	
76 74 73 6 PCI_AD<22>	C2	AD22	
76 74 73 6 PCI_AD<23>	C1	AD23	
76 75 74 73 6 PCI_AD<24>	B6	AD24	
76 75 74 73 6 PCI_AD<25>	A4	AD25	
76 75 74 73 6 PCI_AD<26>	B5	AD26	
76 75 74 73 6 PCI_AD<27> (PCI_AD<27>)	C4	AD27	
76 75 74 73 6 PCI_AD<28>	A5	AD28	
76 75 74 73 6 PCI_AD<29>	C5	AD29	
76 75 74 73 6 PCI_AD<30>	B6	AD30	
76 75 74 73 6 PCI_AD<31>	A6	AD31	
76 74 73 6 PCI_CBE_L<0>	M2	CBE0	
76 74 73 6 PCI_CBE_L<1>	J3	CBE1	
76 74 73 6 PCI_CBE_L<2>	F1	CBE2	
76 74 73 6 PCI_CBE_L<3>	C3	CBE3	
76 74 73 6 PCI_PAR	J4	PAR	
76 74 73 6 PCI_FRAME_L	F3	FRAME	
76 74 73 6 PCI_IRDY_L	F4	IRDY	
76 74 73 6 PCI_TRDY_L	G1	TRDY	
76 74 73 6 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B3	IDSEL	
76 74 73 6 PCI_DEVSEL_L	G2	DEVSEL	
74 PCI_SLOTG_REQ_L	C6	REQ	
74 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR OD	
NEC_INTA_L	C7	INTA OD	
NEC_INTB_L	B7	INTB OD	
NEC_INTC_L	A7	INTC OD	
77 8 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D9	PME OD	
NEC_VCCRST_L	C9	VCCRST(PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI OD	
NEC_LEGC_PD	L7	LEGC	
IPD NTEST1	M8	TP_NEC_NTEST1	6
IPD SMC	M7	TP_NEC_SMC	6
IPD TEB	N7	TP_NEC_TEB	6
IPD AMC	P7	TP_NEC_AMC	6
IPD TEST	L8	TP_NEC_TEST	6
NANDTEST	M10	TP_NEC_NANDTEST	6
SRCLK	M9	TP_NEC_SRCLK	6
SRDTA	N9	TP_NEC_SRDATA	6
IPD SRMOD	P9	TP_NEC_SRMOD	6

74 73 PCI_SB_AD<27>

R7714 22 5% 1/16W MF 402

76 75 74 25 7 =PP3V3_PCI

R7716 10K 5% 1/16W MF 402

R7713 10K 5% 1/16W MF 402

RP7703 47 5% 1/16W SM1

25 PCI_SLOTG_INT_L

87 74 25 8 SYS_WARM_RESET_L

25 13 SYS_PME_L

8 =PCI_USB2_RESET_L

RP7702 47 5% 1/16W SM1

RP7702 & RP7703 required to facilitate NAND-tree testing

R7715 4.7K 5% 1/16W MF 402

RP7703 47 5% 1/16W SM1

Master: Link

USB 2.0 PCI Interface

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DRAWING

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_P1_C
SATA_RXD1	SATA	SATA_RXD1_C	SATA_RXD_N1_C
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_P1
SATA_TXD1	SATA	SATA_TXD1	SATA_TXD_N1
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_P2_C
SATA_RXD2	SATA	SATA_RXD2_C	SATA_RXD_N2_C
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_P2
SATA_TXD2	SATA	SATA_TXD2	SATA_TXD_N2
UATA_DD			UATA_DD<15..8>
UATA_DD7			UATA_DD<7>
UATA_DD			UATA_DD<6..0>
UATA_HOST			UATA_DA<2..0>
UATA_HOST			UATA_CS0_L
UATA_HOST			UATA_CS1_L
UATA_HOST			UATA_HSTROBE
UATA_HOST			UATA_STOP
UATA_HOST_R			UATA_DMACK_L
UATA_HOST_R			UATA_RESET_L
UATA_DEV_R_C			UATA_DSTROBE
UATA_DEV_R			UATA_DMARQ
UATA_DEV_R			UATA_INTRQ

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	15 mils
Length Tolerance:	50 mils
Primary Max Sep:	10 mils outer
Primary Max Sep:	9 mils inner
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

=PP1V2_PWRON_DISK_SB

SATA_VDD x 5

C8000 0.1uF 20% 10V CERM 402
C8001 0.1uF 20% 10V CERM 402
C8002 0.1uF 20% 10V CERM 402
C8003 0.1uF 20% 10V CERM 402
C8004 0.1uF 20% 10V CERM 402

AB14 AB17 T14 W15 Y18 SATA_VDD

U2300 SHASTA V1.0 BGA (5 OF 8) OMIT

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>	80
UD_IDEDD_1_H	H7	UATA_DD_R<1>	80
UD_IDEDD_2_H	H6	UATA_DD_R<2>	80
UD_IDEDD_3_H	E2	UATA_DD_R<3>	80
UD_IDEDD_4_H	C1	UATA_DD_R<4>	80
UD_IDEDD_5_H	C2	UATA_DD_R<5>	80
UD_IDEDD_6_H	E3	UATA_DD_R<6>	80
UD_IDEDD_7_H	G6	UATA_DD_R<7>	80
UD_IDEDD_8_H	G5	UATA_DD_R<8>	80
UD_IDEDD_9_H	D4	UATA_DD_R<9>	80
UD_IDEDD_10_H	G7	UATA_DD_R<10>	80
UD_IDEDD_11_H	F6	UATA_DD_R<11>	80
UD_IDEDD_12_H	C3	UATA_DD_R<12>	80
UD_IDEDD_13_H	F5	UATA_DD_R<13>	80
UD_IDEDD_14_H	E5	UATA_DD_R<14>	80
UD_IDEDD_15_H	D5	UATA_DD_R<15>	80
UD_IDEDA0_H	E6	UATA_DA_R<0>	80
UD_IDEDA1_H	C4	UATA_DA_R<1>	80
UD_IDEDA2_H	D6	UATA_DA_R<2>	80
UD_IDECS1FX_L	B3	UATA_CS0_L_R	80
UD_IDECS3FX_L	B4	UATA_CS1_L_R	80
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	80
UD_IDERD_L	E4	UATA_HSTROBE_R	80
UD_IDEWR_L	D3	UATA_STOP_R	80
UD_IDERST_L	E7	UATA_RESET_L_R	80

DSTROBE aka: IORDY/HDMARDY*

HSTROBE aka: DIOR*

STOP aka: DIOW*

83 80 UATA_DSTROBE	F9	UD_IDECHRDY_H	
83 80 UATA_DMARQ	D7	UD_IDEDMARQ_H	
83 80 UATA_INTRQ	C5	UD_IDEINTRQ_H	

SATA 0

83 80 SATA_RXD_P1_C	Y17	RXDP1	TXDP1	AA16 SATA_TXD_P1 80 83
83 80 SATA_RXD_N1_C	Y16	RXDN1	TXDN1	AB16 SATA_TXD_N1 80 83

SATA 1

83 80 SATA_RXD_P2_C	AB15	RXDP2	TXDP2	Y15 SATA_TXD_P2 80 83
83 80 SATA_RXD_N2_C	AA15	RXDN2	TXDN2	Y14 SATA_TXD_N2 80 83

SATA_GND

AA14 AA17 T13 W16

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

UATA Termination

R8005 10K 5% 1/16W MF 402

RP8000 33 5% 1/16W SM1
RP8000 33 5% 1/16W SM1
RP8000 33 5% 1/16W SM1
RP8001 33 5% 1/16W SM1
RP8001 33 5% 1/16W SM1
RP8002 33 5% 1/16W SM1
RP8002 33 5% 1/16W SM1
RP8002 33 5% 1/16W SM1
RP8003 33 5% 1/16W SM1
RP8003 33 5% 1/16W SM1
RP8003 33 5% 1/16W SM1
RP8004 33 5% 1/16W SM1
RP8004 33 5% 1/16W SM1
R8000 33 5% 1/16W MF 402
R8001 33 5% 1/16W MF 402
R8002 22 5% 1/16W MF 402
R8003 22 5% 1/16W MF 402
R8004 22 5% 1/16W MF 402

80 UATA_DD_R<0>			UATA_DD<0> 6 80 83
80 UATA_DD_R<1>			UATA_DD<1> 6 80 83
80 UATA_DD_R<2>			UATA_DD<2> 6 80 83
80 UATA_DD_R<3>			UATA_DD<3> 6 80 83
80 UATA_DD_R<4>			UATA_DD<4> 6 80 83
80 UATA_DD_R<5>			UATA_DD<5> 6 80 83
80 UATA_DD_R<6>			UATA_DD<6> 6 80 83
80 UATA_DD_R<7>			UATA_DD<7> 6 80 83
80 UATA_DD_R<8>			UATA_DD<8> 6 80 83
80 UATA_DD_R<9>			UATA_DD<9> 6 80 83
80 UATA_DD_R<10>			UATA_DD<10> 6 80 83
80 UATA_DD_R<11>			UATA_DD<11> 6 80 83
80 UATA_DD_R<12>			UATA_DD<12> 6 80 83
80 UATA_DD_R<13>			UATA_DD<13> 6 80 83
80 UATA_DD_R<14>			UATA_DD<14> 6 80 83
80 UATA_DD_R<15>			UATA_DD<15> 6 80 83
80 UATA_DA_R<0>			UATA_DA<0> 6 80 83
80 UATA_DA_R<1>			UATA_DA<1> 6 80 83
80 UATA_DA_R<2>			UATA_DA<2> 6 80 83
80 UATA_RESET_L_R			UATA_RESET_L 6 80 83
80 UATA_CS0_L_R			UATA_CS0_L 6 80 83
80 UATA_CS1_L_R			UATA_CS1_L 6 80 83
80 UATA_HSTROBE_R			UATA_HSTROBE 6 80 83
80 UATA_STOP_R			UATA_STOP 6 80 83
80 UATA_DMACK_L_R			UATA_DMACK_L 6 80 83

Master: Link

Shasta Disk

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 80 OF 103	

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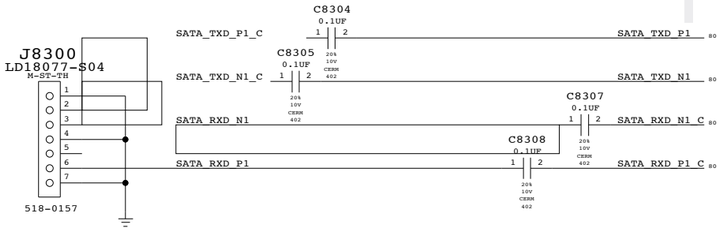
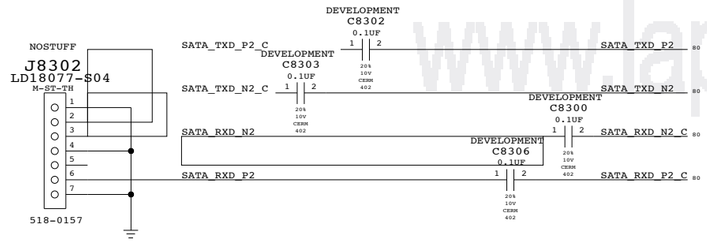
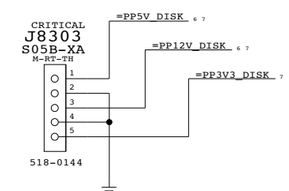
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
UATA_DD			
UATA_DD7			
UATA_DD			
UATA_HOST			
UATA_HOST			
UATA_HOST			
UATA_HOST			
UATA_HOST			
UATA_HOST_R			
UATA_HOST_R			
UATA_DEV_R_C			
UATA_DEV_R			
UATA_DEV_R			

SATA CONNECTORS

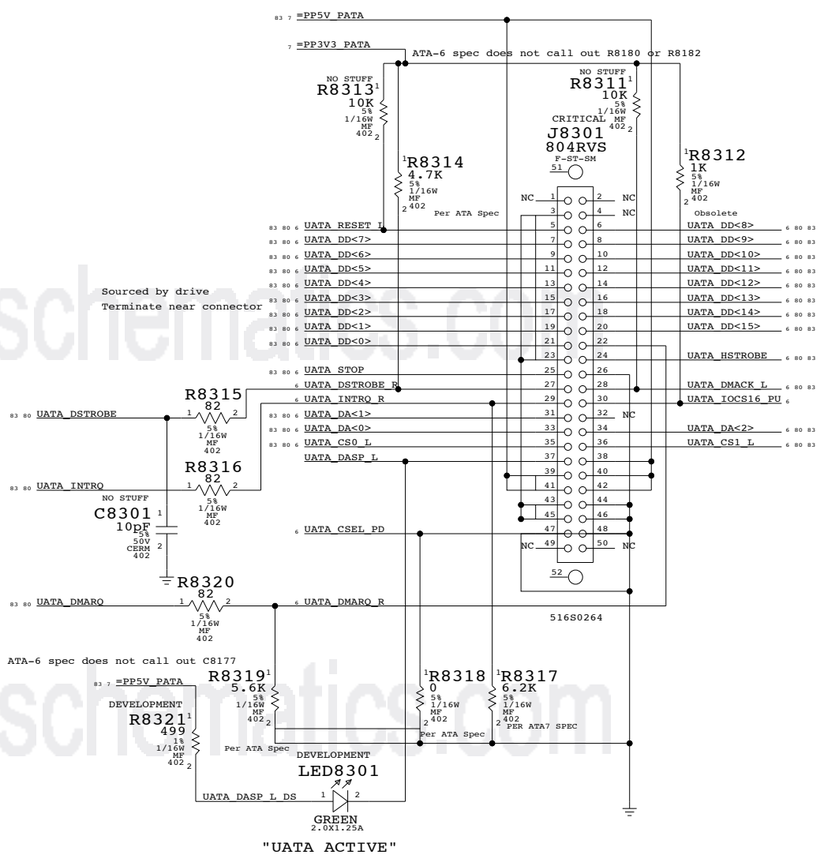




HD POWER



PATA CONNECTOR



"UATA ACTIVE"

DISK CONNECTORS

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 83 OF 103	

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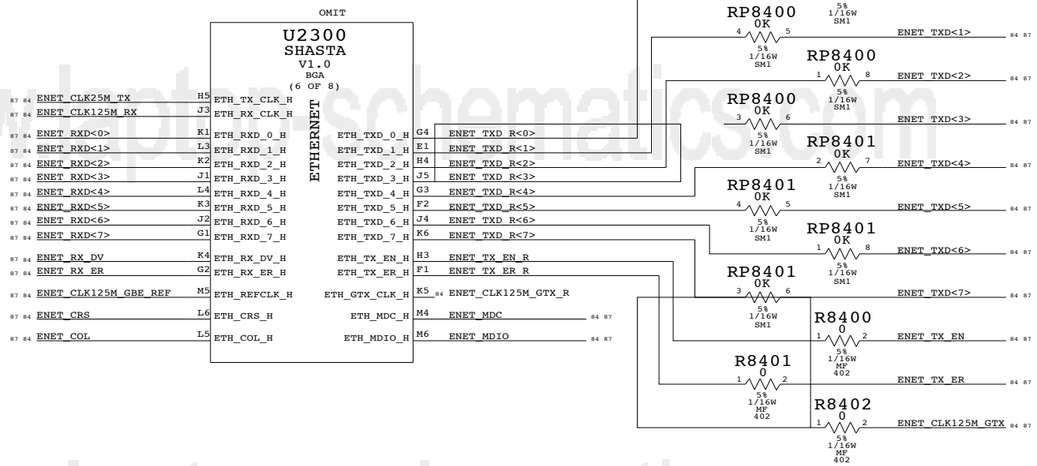
ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_RX_CLK	ENET	10_MIL		ENET_CLK25M_TX 84 87
ENET_RX_CLK	ENET	10_MIL		ENET_CLK125M_RX 84 87
ENET_GBE_REF	ENET	15_MIL_SPACING		ENET_CLK125M_GBE_REF 84 87
ENET_TX_CLK	ENET	15_MIL_SPACING		ENET_CLK125M_GTX 84 87
	ENET	15_MIL_SPACING		ENET_CLK125M_GTX_R 84
ENET_RX	ENET			ENET_RXD<7..0> 84 87
ENET_RX_CTL	ENET			ENET_RX_DV 84 87
ENET_RX_CTL	ENET			ENET_RX_ER 84 87
ENET_TX	ENET			ENET_TXD<7..0> 84 87
ENET_TX_CTL	ENET			ENET_TX_EN 84 87
ENET_TX_CTL	ENET			ENET_TX_ER 84 87
ENET_RX_CTL	ENET			ENET_CRS 84 87
ENET_RX_CTL	ENET			ENET_COL 84 87
ENET_MDC	ENET			ENET_MDC 84 87
ENET_MDIO	ENET			ENET_MDIO 84 87

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



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Shasta Ethernet

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SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 84 OF 103	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDP 87
ENET_MDI_TX	ENET	ENET_MDI_TD	ENET_TDN 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDP 87
ENET_MDI_RX	ENET	ENET_MDI_RD	ENET_RDN 87
ENET_XTAL	15 MIL SPACING		ENET_CLK25M_XIN 87
	15 MIL SPACING		ENET_CLK25M_XOUT 87

ETHERNET ROUTING PRIORITY:
1. DECOUPLING CAPS
2. TX TERMINATION - LOCATE NEAR PHY
3. RX TERMINATION - LOCATE NEAR PHY

ROUTE TD OVER 2.5V PLANE (BOTTOM LAYER) ONLY
ROUTE RD OVER GROUND PLANE (TOP LAYER) ONLY

ALL DIFFERENTIAL SIGNALS SHOULD BE CLOSE, PARALLEL, MATCHED LENGTHS, WITH MINIMUM VIA COUNT, AND SHORT IF POSSIBLE

CLEAR OUT ALL PLANES BETWEEN MIDDLE OF TRANSFORMER AND CONNECTOR

PP2V5_ENET — VOLTAGE=2.5V, MIN_LINE_WIDTH=25MIL, MIN_NECK_WIDTH=10MIL
C8703 0.1UF 20% 10V CERM 402
C8704 0.01UF 20% 16V CERM 402
C8702 0.1UF 20% 10V CERM 402
C8705 0.01UF 20% 16V CERM 402
C8712 10UF 20% 6.3V CERM 805

87 7 PP3V3_PWRON_ENET

ENET_DVDD — VOLTAGE=2.5V, MIN_LINE_WIDTH=25MIL, MIN_NECK_WIDTH=10MIL
C8711 10UF 20% 6.3V CERM 805
C8716 0.1UF 20% 10V CERM 402
C8708 0.01UF 20% 16V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8709 0.01UF 20% 16V CERM 402

NOTE: PLACE R3128, R3100, RP 3101 CLOSE TO PHY

U8700
BCM5231
TQFP
(SYM_VER2)
CRITICAL

REGDVDD	3		
REGAVDD	20		
DVDD1	2		
DVDD2	55		
AVDD1	27		
AVDD2	28		
OVDD1	1		
OVDD2	46		
REFCLK	4		
BIASVDD	22		
OVDD/NC	8		
TXC	53		
TXD0	57		
TXD1	58		
TXD2	59		
TXD3	60		
TXEN	56		
TXER	52		
RXC	50		
RXD0	48		
RXD1	47		
RXD2	44		
RXD3	43		
RXDV	49		
RXER	51		
CRS	62		
COL	61		
RESET*	9		
MDC	42		
MDIO	41		
XTALI	6		
XTALO	5		
PHYAD0	10		
PHYAD1	11		
PHYAD2	12		
PHYAD3	13		
PHYAD4	14		
OGND1	40		
OGND2	45		
OGND3/JTAG_EN	64		
DGND1	54		
DGND2	63		
AGND1	29		
AGND2	32		
XTALGND	7		
BIASGND	24		
TD+	31		
TD-	30		
RD+	26		
RD-	25		
NC	21		
NC	19	NC	
FDX	39	ENET_5221_FDX	87
F100/JTAG_TCK	37	TP_ENET_TCK	6
ANEN/JTAG_TRST	38	ANEN	
TESTEN	15	ENET_5221_TESTEN	87
OVDD/NC	18	MII_EN	
LOW_PWR	16	ENET_5221_LOW_PWR	87
ENERGY_DET	17	ENET_ENERGYDET	25
RDAC	23		
LNKLED/JTAG_TDI*	35	ENET_TDI	87
SPDLED/JTAG_TMS*	36	ENET_TMS	87
XMTLED*	34	XMIT_LED	87
RCVLED/JTAG_TDO*	33	TP_ENET_TDO	

(PLACE R3126, R3127 R3117, R3118 CLOSE TO PHY)
C8710 0.1UF 20% 10V CERM 402
R8701 49.9 1% 1/16W MF 402
R8700 49.9 1% 1/16W MF 402
PP3V3_PWRON_ENET
R8703 49.9 1% 1/16W MF 402
R8702 49.9 1% 1/16W MF 402
R8712 10K 5% 1/16W MF 402
R8713 10K 5% 1/16W MF 402

C8722 0.1UF 20% 10V CERM 402

PRIMARY
SYM_VER-3
ENET_TDP 1
ENET_TDN 3
ENET_RDP 4
ENET_RDN 6
RJ45 CHIP SIDE
GND_CHASSIS_RJ45

(514-0200)
CRITICAL
J8700
RJ45
JFM24V10
F-ST-TH
1CT:1CT TX-SIDE
1CT:1CT RX-SIDE
SECONDARY J1 J2 J3 J4 J5 J6 J7 J8
RJ45 CABLE SIDE
75 OHM 75 OHM 75 OHM 75 OHM
SHIELD 1000PF, 2000V

C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8721 0.1UF 20% 10V CERM 402
TWO OF THESE CAPS SHOULD BE NEAR J8700 PINS 2&5

R8704 10K 5% 1/16W MF 402
R8704 PULLDOWN ENABLES AUTO-MDI/MDIX

R8705 1.27K 1% 1/16W MF 402

RP8702 10K 5% 8M1
87 ENET_5221_FDX
87 ENET_5221_TESTEN
87 ENET_5221_LOW_PWR
87 OGND3_JTAG_EN

PP3V3_PWRON_ENET
R8718 4.7K 5% 1/16W MF 603
R8717 330 5% 1/16W MF 603 — DEVELOPMENT
DS3P1 DEVELOPMENT LED8702 GREEN 2.0X1.25A 10/100
R8716 330 5% 1/16W MF 603 — DEVELOPMENT
DS1P1 DEVELOPMENT LED8701 GREEN 2.0X1.25A XMIT
R8715 330 5% 1/16W MF 603 — DEVELOPMENT
R8714 4.7K 5% 1/16W MF 603
DS2P1 DEVELOPMENT LED8700 GREEN 2.0X1.25A LINK
87 ENET_TMS
87 XMIT_LED
87 ENET_TDI

84 ENET_CLK25M_TX — I237 MAKE_BASE=TRUE — CLK_ENET_LINK_TX (NET_SPACING_TYPE=10 MIL) — R8706 33 5% 1/16W MF 402 — CLKENET_PHY_TX (NET_SPACING_TYPE=10 MIL)
84 ENET_CLK125M_RX — I238 MAKE_BASE=TRUE — CLK_ENET_LINK_RX (NET_SPACING_TYPE=10 MIL)
R8707 33 5% 1/16W MF 402 — CLKENET_PHY_RX (NET_SPACING_TYPE=10 MIL)

RP8700 33 5% 8M1
84 ENET_RXD<0> — ENET_PHY_RXD<0> 48
84 ENET_RXD<1> — ENET_PHY_RXD<1> 47
84 ENET_RXD<2> — ENET_PHY_RXD<2> 44
84 ENET_RXD<3> — ENET_PHY_RXD<3> 43

84 ENET_TX_EN 56
84 ENET_TX_ER 52
R8709 33 5% 1/16W MF 402
84 ENET_RX_DV — ENET_PHY_RX_DV 49
ENET_PHY_RX_ER 51
ENET_PHY_CRS 62
ENET_PHY_COL 61
84 ENET_RX_ER
84 ENET_CRS
84 ENET_COL
RP8701 33 1/16W 5% 8M1

ETHPHYRESET_L — NET_SPACING_TYPE=10 MIL — 9
84 ENET_MDC 42
87 7 PP3V3_PWRON_ENET
C8750 0.1uF 10V CERM 402
77 74 25 8 SYS_WARM_RESET_L
U8750 MC74VHC1G08 SOT23-5
ETHPHYRESET_L_R
R8711 0 5% 1/16W MF 402
R8719 1K 5% 1/16W MF 402
ENETFW_RESET_L 90
Q8700 2N7002 SM
NOSTUFF C8723 10UF 20% 10V CERM 603
25 ENETFW_RESET
SHASTA SIGNAL IS ACTIVE HIGH

87 7 PP3V3_PWRON_ENET
R8708 1.5K 1% 1/16W MF 603
84 ENET_MDIO
(PLACE Y8700 CRYSTAL CLOSE TO PHY)
87 ENET_CLK25M_XIN
CRITICAL
Y8700 25.0000M 8X4.5MM-SM
87 ENET_CLK25M_XOUT
C8701 27PF 5% 50V CERM 603
C8700 27PF 5% 50V CERM 603

PHY ADDRESS 00000

87 OGND3_JTAG_EN

NOTE: LINK SUPPORT FOR GIGABIT ETHERNET PULLED DOWN OR ALIASED TO TEST POINTS HERE.

84 ENET_RXD<4> — I228 ENET_RXD_PD MAKE_BASE=TRUE
84 ENET_RXD<5> — I229
84 ENET_RXD<6> — I230
84 ENET_RXD<7> — I231
R8799 10K 1% 1/16W MF 402

84 ENET_CLK125M_GBE_REF
R8798 10K 1% 1/16W MF 402

84 ENET_TXD<4> — I232 TP_ENET_TXD<4> 6 MAKE_BASE=TRUE
84 ENET_TXD<5> — I233 TP_ENET_TXD<5> 6 MAKE_BASE=TRUE
84 ENET_TXD<6> — I234 TP_ENET_TXD<6> 6 MAKE_BASE=TRUE
84 ENET_TXD<7> — I235 TP_ENET_TXD<7> 6 MAKE_BASE=TRUE
84 ENET_CLK125M_GTX — I236 TP_ENET_CLK125M_GTX 6 MAKE_BASE=TRUE

PP3V3_PWRON_ENET
C8720 4.7UF 20% 10V CERM 1206
C8719 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8713 10UF 20% 6.3V CERM 1206
KEEP ALL CAPS CLOSE TO TRANSCEIVER ON THIS PAGE

ETHERNET PHY

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ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
FW	FW			FW_DATA<7..0> 88 90
FW	FW			FW_CTL<1..0> 88 90
FW_LPS	FW			FW_LPS 88 90
FW_LREQ	FW			FW_LREQ 88 90
FW_PINT	FW			FW_PINT 88 90
FW_LCLK	FW	15_MIL_SPACING		FW_CLK98M_LCLK 88 90
FW_PCLK	FW	15_MIL_SPACING		FW_CLK98M_PCLK 88 90
		15_MIL_SPACING		FW_CLK98M_LCLK_R 88

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

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74 25 23 7 =PP2V5_PWRON_SB

C8800 0.1uF 20% 10V CERM 402
C8801 0.1uF 20% 10V CERM 402
C8802 0.1uF 20% 10V CERM 402

N5 J7 A4 FWVDDP

U2300 OMIT
SHASTA
V1.0
BGA
(7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	88 90
PHY_DATA_1_H	P5	FW_DATA<1>	88 90
PHY_DATA_2_H	N1	FW_DATA<2>	88 90
PHY_DATA_3_H	M7	FW_DATA<3>	88 90
PHY_DATA_4_H	N6	FW_DATA<4>	88 90
PHY_DATA_5_H	L1	FW_DATA<5>	88 90
PHY_DATA_6_H	M3	FW_DATA<6>	88 90
PHY_DATA_7_H	L2	FW_DATA<7>	88 90
PHY_CTL_0_H	N2	FW_CTL<0>	88 90
PHY_CTL_1_H	N3	FW_CTL<1>	88 90
PHY_LPS_H	P6	FW_LPS	88 90
PHY_LREQ_H	P1	FW_LREQ	88 90
PHY_LCLK_H	R1	FW_CLK98M_LCLK_R	88
PHY_LINKON_L	N7	FW_LINKON	90

90 88 FW_CLK98M_PCLK P2 PHY_SCLK_H
90 88 FW_PINT P3 PHY_PINT_L

R8800 22 5% 1/16W MF 402
1 2 FW_CLK98M_LCLK 88 90

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Master: Link

Shasta FireWire

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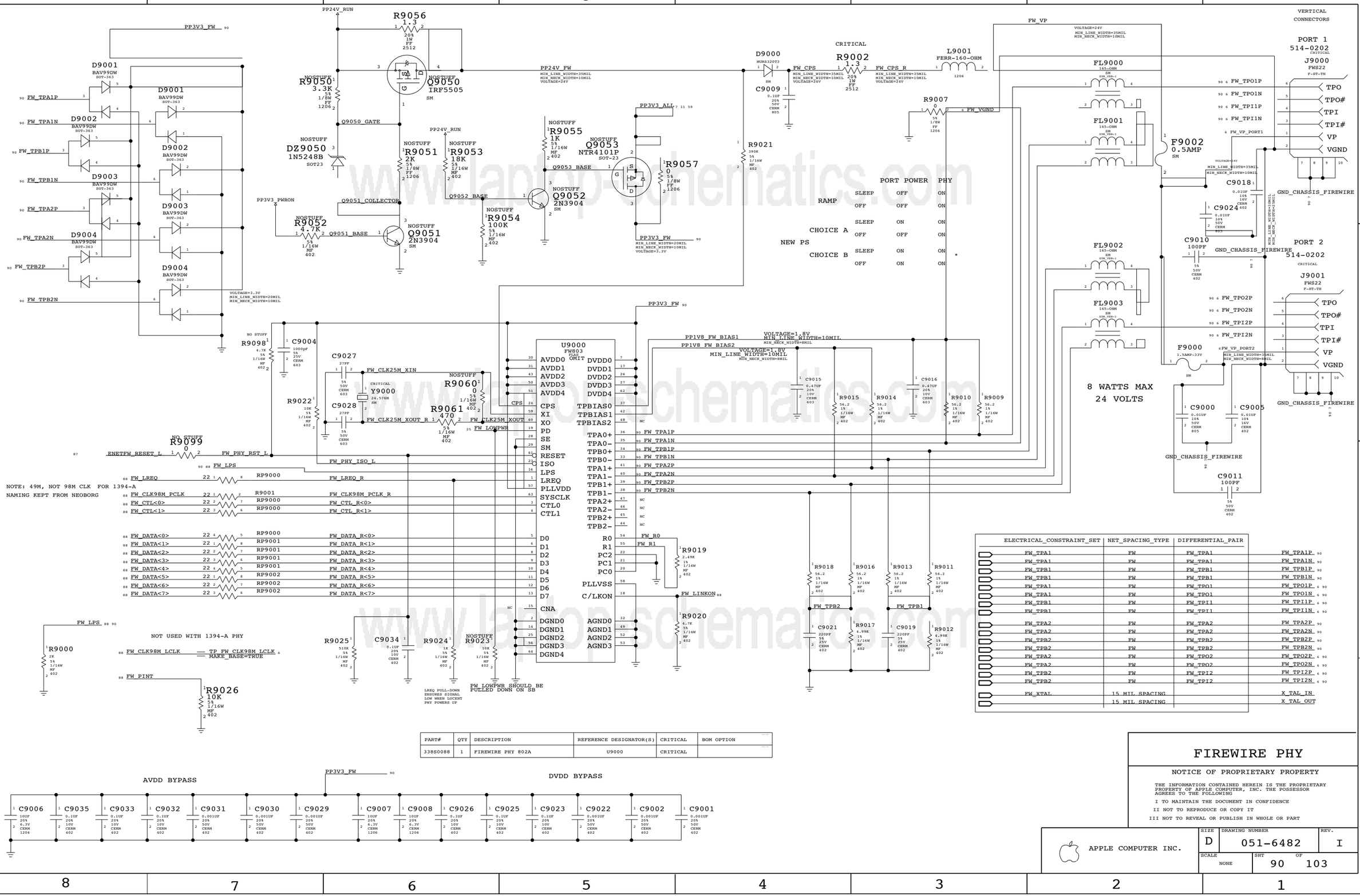

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ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
USB2_0	USB2	USB2	USB2_0	USB2_P<0>
USB2_0	USB2	USB2	USB2_0	USB2_N<0>
USB2_1	USB2	USB2	USB2_1	USB2_P<1>
USB2_1	USB2	USB2	USB2_1	USB2_N<1>
USB2_2	USB2	USB2	USB2_2	USB2_P<2>
USB2_2	USB2	USB2	USB2_2	USB2_N<2>
USB2_3	USB2	USB2	USB2_3	USB2_P<3>
USB2_3	USB2	USB2	USB2_3	USB2_N<3>
USB2_4	USB2	USB2	USB2_4	USB2_P<4>
USB2_4	USB2	USB2	USB2_4	USB2_N<4>
USB2_NEC_XTAL		15_MIL_SPACING		NEC_CLK30M_XT1
		15_MIL_SPACING		NEC_CLK30M_XT2
		15_MIL_SPACING		NEC_CLK30M_XT2_R

Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_USB

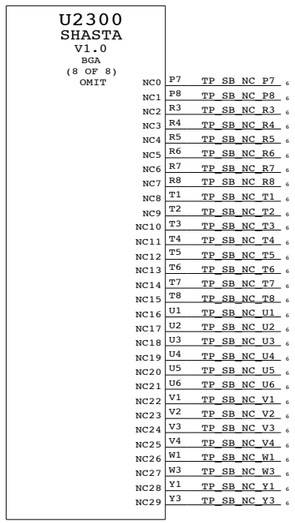
Signal aliases required by this page:
(NONE)

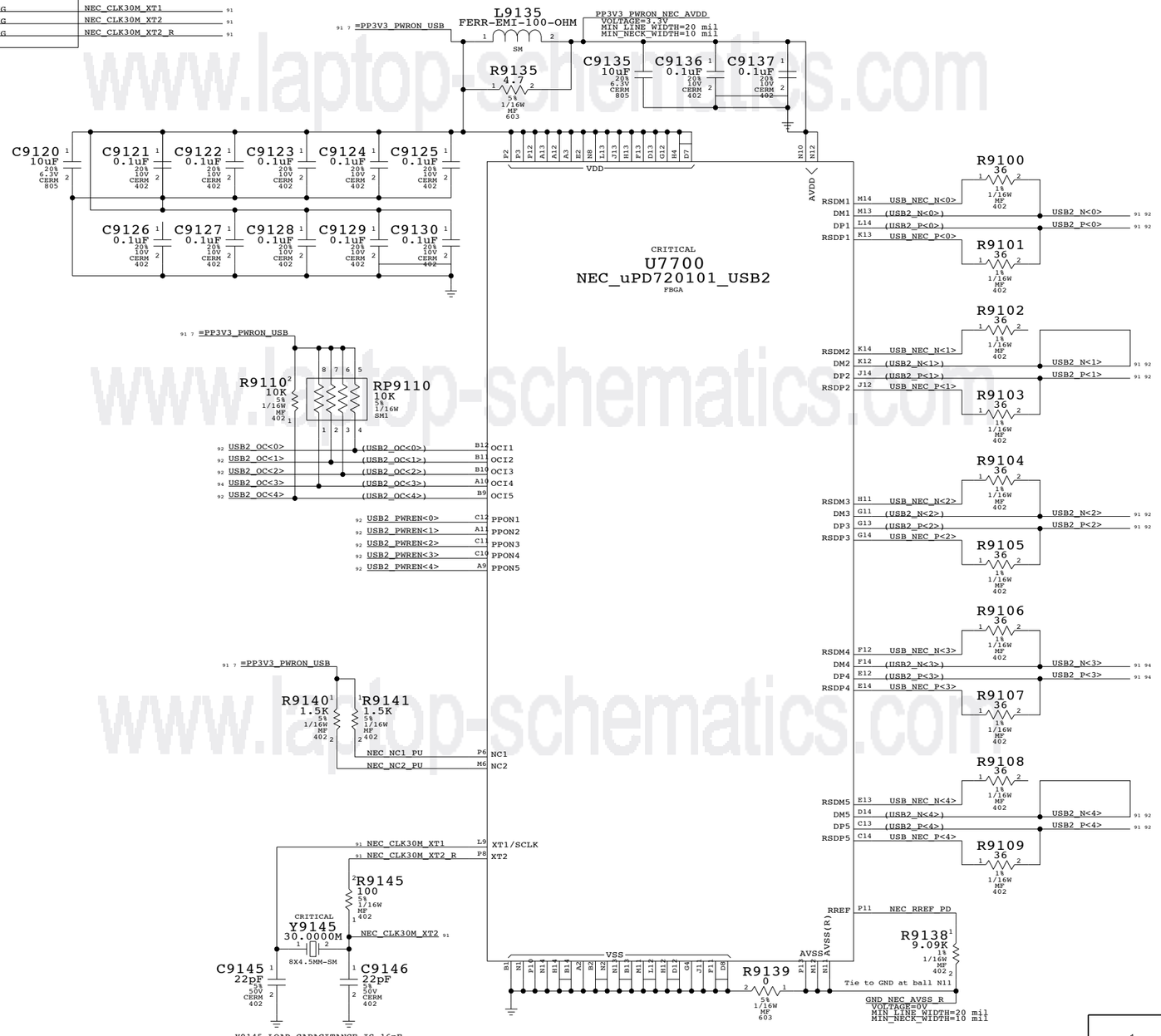
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





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USB Host Interfaces

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
PROVIDED BY	USB2	USB2_PORT1_F	USB2_PORT1_P_F
	USB2	USB2_PORT1_F	USB2_PORT1_N_F
USB CONTROLLER	USB2	USB2_PORT2_F	USB2_PORT2_P_F
	USB2	USB2_PORT2_F	USB2_PORT2_N_F
	USB2	USB2_PORT3_F	USB2_PORT3_P_F
	USB2	USB2_PORT3_F	USB2_PORT3_N_F

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

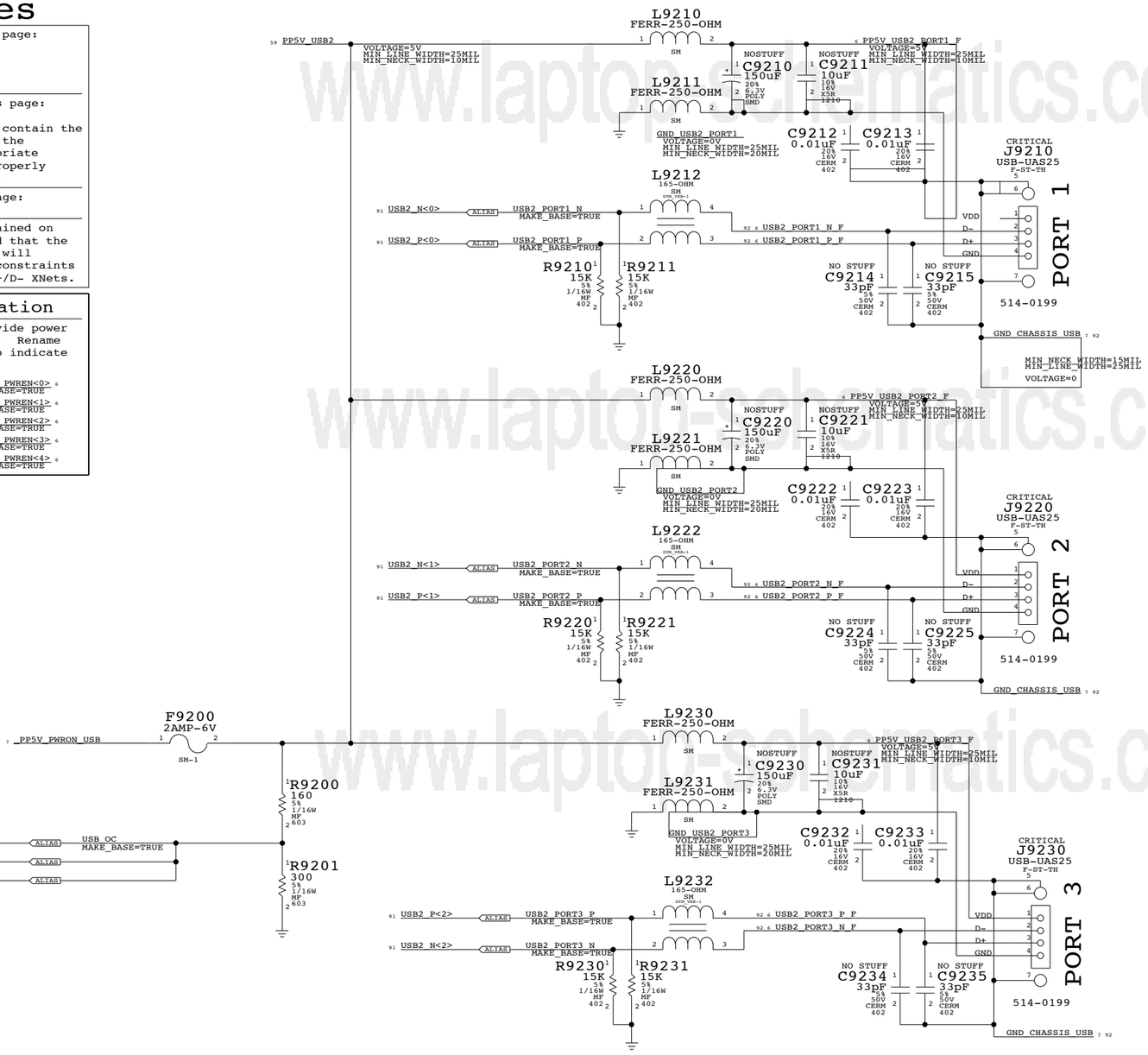
NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

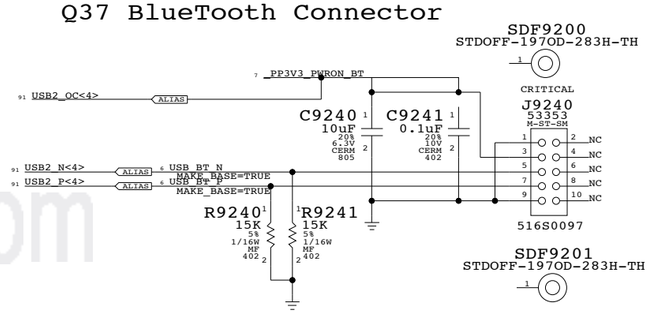
NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

- USB2_PWREN<0> (ALIAS) TP_USB2_PWREN<0> MAKE_BASE=TRUE
- USB2_PWREN<1> (ALIAS) TP_USB2_PWREN<1> MAKE_BASE=TRUE
- USB2_PWREN<2> (ALIAS) TP_USB2_PWREN<2> MAKE_BASE=TRUE
- USB2_PWREN<3> (ALIAS) TP_USB2_PWREN<3> MAKE_BASE=TRUE
- USB2_PWREN<4> (ALIAS) TP_USB2_PWREN<4> MAKE_BASE=TRUE

External USB Ports



Q37 BlueTooth Connector



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USB Device Interfaces

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Page Notes

Power aliases required by this page:
- _PP3V3_PWRON_MODEM
  Spec Load: 0.5 A active, 3 mA auxiliary

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Q52 Modem Connector

SDF9400
STDOFF-4MM-9MMH-TH

CRITICAL
J9401
C104A-H9.0
F-ST-SM

94 7 _PP3V3_PWRON_MODEM

C9450 10UF 20% 6.3V CERM 805
C9451 0.1UF 20% 10V CERM 402

PP3V3_PWRON_MODEM 7 94
R9451 10K 5% 1/16W MF 402

MODEM_RING2SYS_L 6 25 94
MODEM_FC_RGDT
I2S1_SYNC 6 25 94
I2S1_DEV_TO_SB_DTI 6 25 76 94
I2S1_BITCLK 6 25 94

94 76 25 6 I2S1_SB_TO_DEV_DTO
94 25 6 I2S1_RESET_L
94 76 25 6 I2S1_MCLK

516S0116

SDF9401
STDOFF-4MM-9MMH-TH
GND_CHASSIS_MODEM

MicroDash Modem Connector

SOFT MODEM IS PLAN OF RECORD
MICRODASH MODEM CONNECTOR LEFT ON FOR DEVELOPMENT PURPOSES ONLY

NOSTUFF
SDF9402
STDOFF-4MM-9MMH-TH

91 USB2_OC<3> ALIAS
7 PP3V3_PWRON_UDASH

DEVELOPMENT C9400 4.7uF 20% 10V CERM 1206
DEVELOPMENT C9401 0.1uF 20% 10V CERM 402
DEVELOPMENT R9400 10K 5% 1/16W MF 402
NOSTUFF R9401 10K 5% 1/16W MF 402
DEVELOPMENT R9402 10K 5% 1/16W MF 402

DEVELOPMENT
J9400
5047
F-ST-SM

25 6 UDASH_SDOWN
Default to Modem On

94 76 25 6 I2S1_DEV_TO_SB_DTI
94 25 6 I2S1_SYNC
94 25 6 MODEM_RING2SYS_L
MODEM_RING2SYS_L SHOULD BE PULLED UP ON SB
18 6 I2C_UDASH_SCL

(+3.3V)	1	2	(+3.3V)
(GND)	3	4	(RST*) UDASH_RESET_L 6 25
(SDOWN)	5	6	(RTS*) I2S1_MCLK 6 25 76 94
(GND)	7	8	(DTR*) I2S1_RESET_L 6 25 94
(RXD)	9	10	(GND)
(GPIO*)	11	12	(TXD*) I2S1_SB_TO_DEV_DTO 6 25 76 94
(GND)	13	14	(TRXC) I2S1_BITCLK 6 25 94
(RING*)	15	16	(GND)
(HOOK)	NC 17	18	(D-) USB_UDASH_N 6 MAKE_BASE=TRUE
(GND)	19	20	(D+) USB_UDASH_P 6 MAKE_BASE=TRUE
(SCL)	21	22	(GND)
(GND)	23	24	(SDA) I2C_UDASH_SDA 6 18
(A0)	25	26	(A1) UDASH_I2C_A1_PU 6
(SNDIN)	NC 27	28	(+5V)
(SNDOUT)	NC 29	30	(+5V) PP5V_PWRON_UDASH 7

516S0121

ALIAS USB2_N<3> 91
ALIAS USB2_P<3> 91

R9404 15K 5% 1/16W MF 402
R9403 15K 5% 1/16W MF 402

DEVELOPMENT C9402 0.1uF 20% 10V CERM 402
DEVELOPMENT C9403 10uF 20% 6.3V CERM 1206

RJ11 CONNECTOR

STUFFED AT FATP
SYMBOL USED FOR PLACEMENT

OMIT
J9402
RJ11-HGT27.5
ST-TH

514-0205

From Intel Mobile Audio/Modem
Daughter Card Specification
Rev 1.0, February 22, 1999

1 - MONO_OUT/PC_BEEP	2 - AUDIO_PWRON
3 - GND	4 - MONO_PHONE
5 - AUXA_RIGHT	6 - RESERVED
7 - AUXA_LEFT	8 - GND
9 - CD_GND	10 - 5Vmain
11 - CD_RIGHT	12 - RESERVED
13 - CD_LEFT	14 - RESERVED
15 - GND	16 - PRIMARY_DN
17 - 3.3Vaux	18 - 5Vd
19 - GND	20 - GND
21 - 3.3Vmain	22 - AC97_SYNC
23 - AC97_SDATA_OUT	24 - AC97_SDATA_INB
25 - AC97_RESET#	26 - AC97_SDATA_INA
27 - GND	28 - GND
29 - AC97_MSTRCLK	30 - AC97_BITCLK

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Modem Interface

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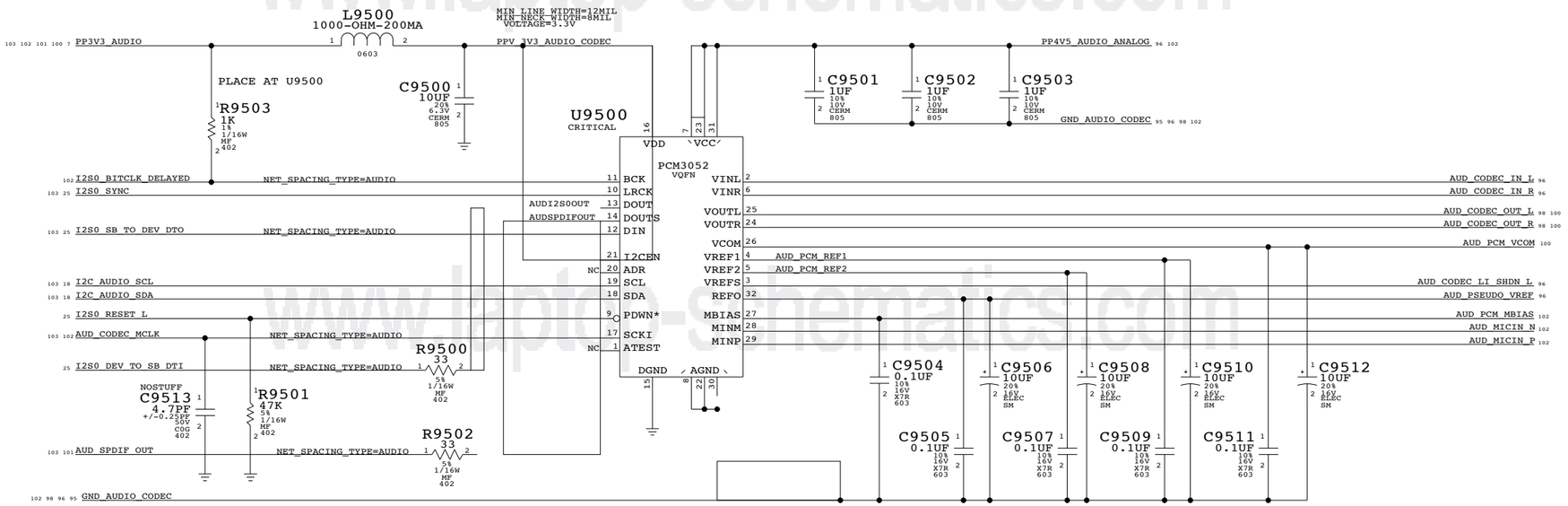
AUDIO CODEC
APPLE P/N 353S0655



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AUDIO: CODEC

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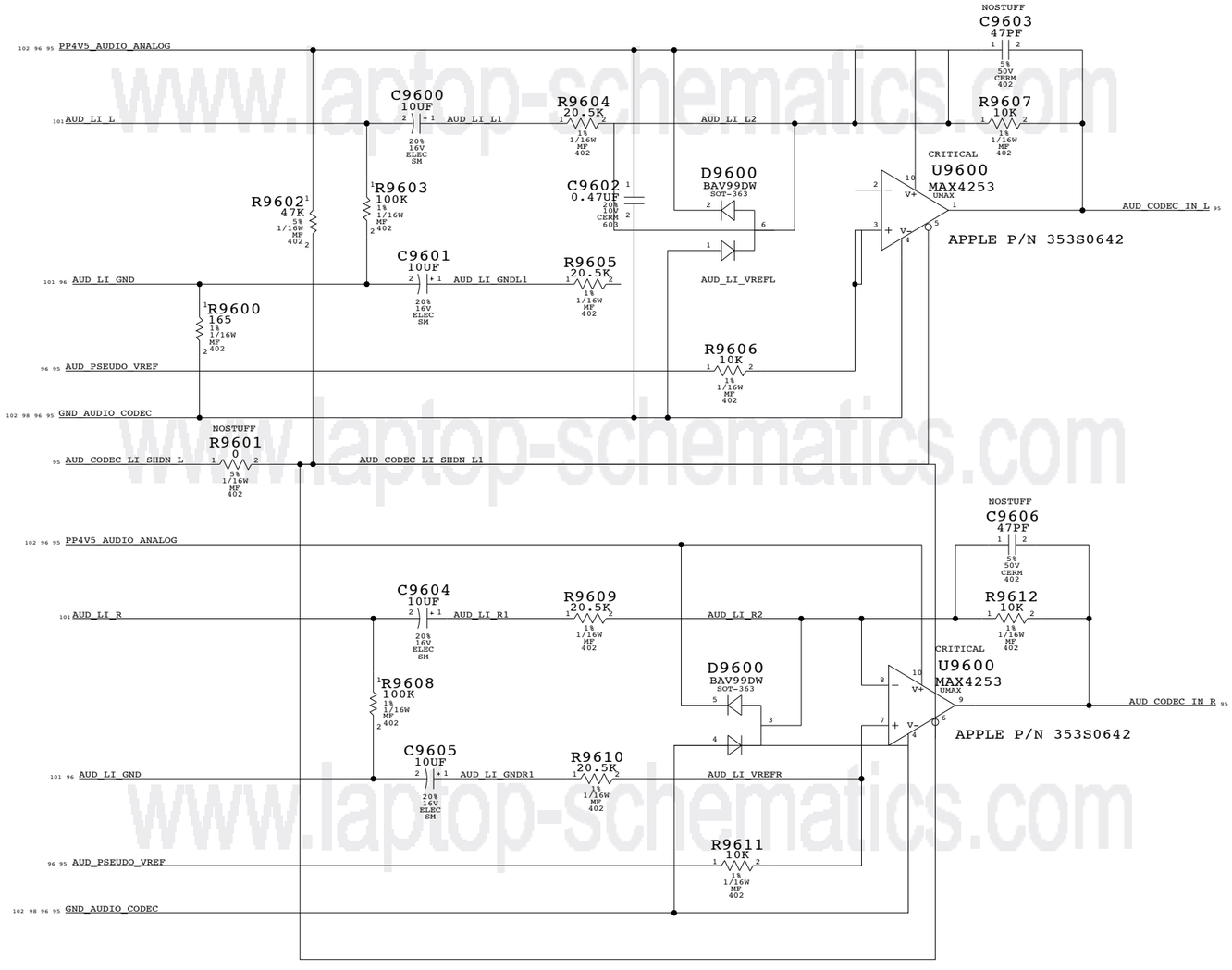
SIZE	DRAWING NUMBER	REV.
D	051-6482	I
SCALE: NONE	SHT 95 OF 103	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



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AUDIO: LINE INPUT AMP

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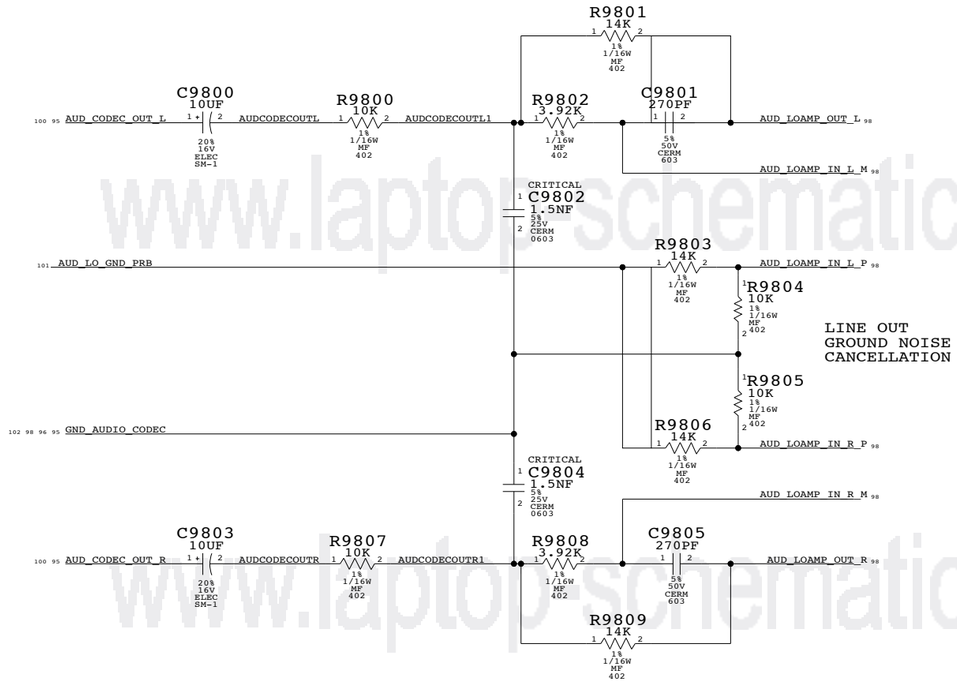
SCALE: NONE	SHT 96 OF 103	

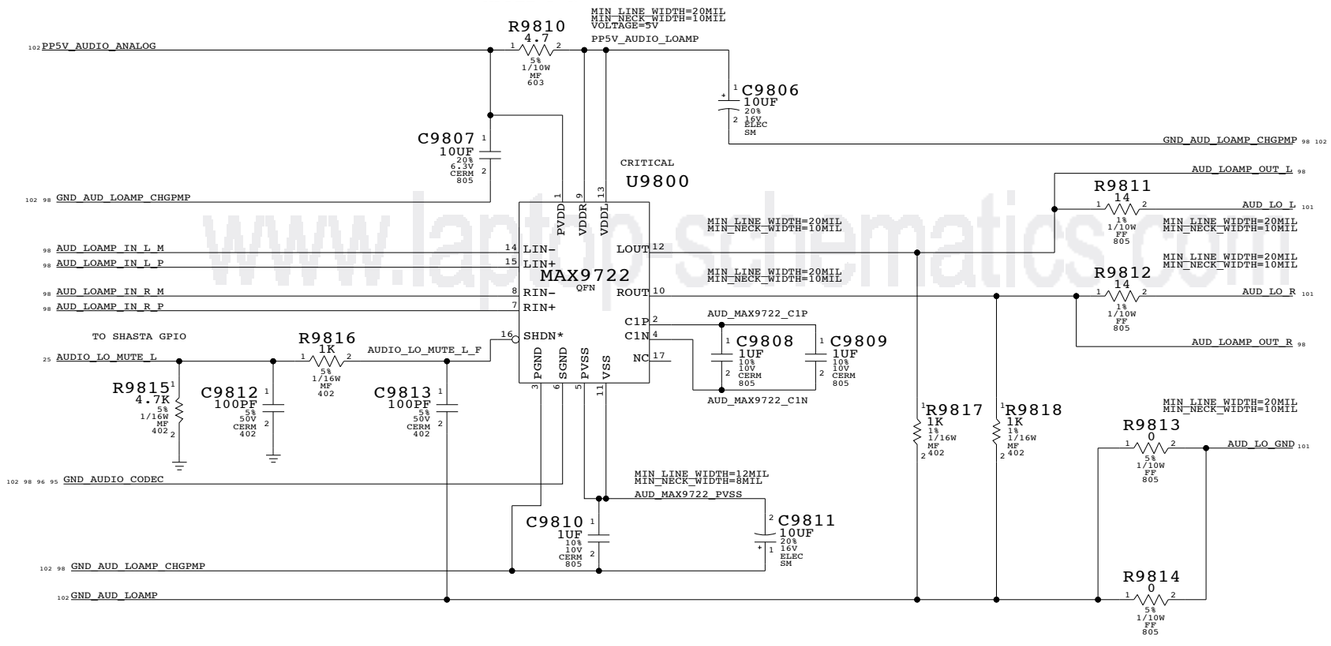
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

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SCALE	SHT	OF
NONE	98	103

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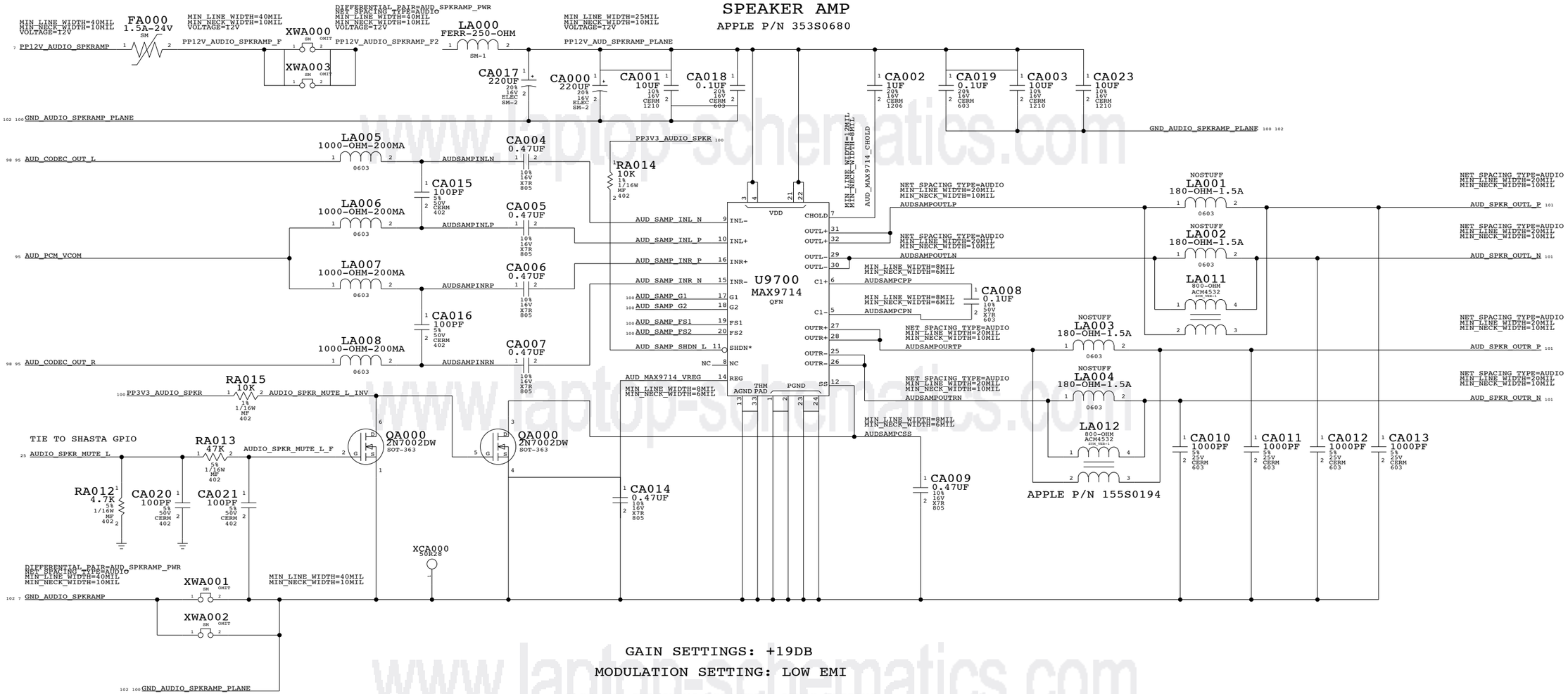
SPEAKER AMP

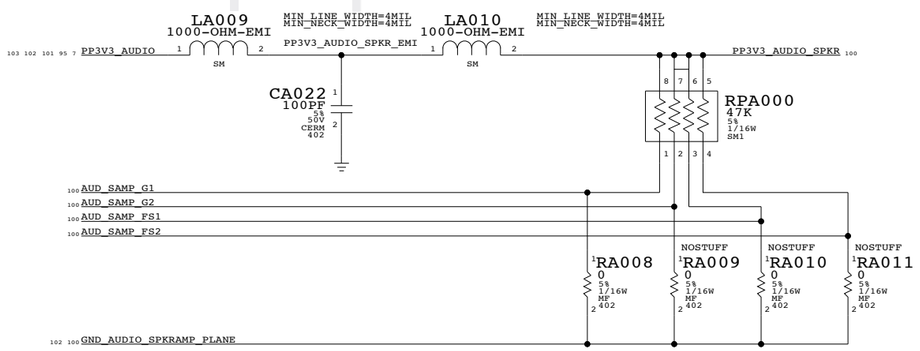
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



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AUDIO: SPEAKER AMP

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SCALE: NONE	SHT: 100 OF 103	

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LINE IN JACK

APPLE P/N 514-0203

JA100 AJR23 F-ST-TH

LA100 FERR-EMI-100-OHM SM — AUD_LI_L_JACK → AUD_LI_L_EMI → AUD_LI_L 96

LA101 FERR-EMI-100-OHM SM — AUD_LI_DET_JACK → AUD_LI_DET_EMI → AUD_LI_DET_H 101

LA102 FERR-EMI-100-OHM SM — AUD_LI_R_JACK → AUD_LI_R_EMI → AUD_LI_R 96

LA103 FERR-EMI-100-OHM SM — AUD_LI_GND_JACK → AUD_LI_GND_EMI 101 → AUD_LI_GND 96

LA104 FERR-EMI-100-OHM SM

LA105 FERR-EMI-100-OHM SM

LA106 FERR-EMI-100-OHM SM

LA107 FERR-EMI-100-OHM SM

All LA parts: MIN_LINE_WIDTH=8MIL MIN_NECK_WIDTH=6MIL

CA100 100PF 5% 50V CERM 402

CA101 100PF 5% 50V CERM 402

CA102 100PF 5% 50V CERM 402

CA103 100PF 5% 50V CERM 402

DZA100 NOSTUFF 14V-15A 0405

102 101 7 GND_CHASSIS_AUDIO_EXTERNAL

102 101 7 GND_CHASSIS_AUDIO_EXTERNAL

SPEAKER CABLE CONNECTOR

APPLE P/N 518-0138

100 AUD_SPKR_OUTR_P → LA130 180-OHM-1.5A 0603 → AUD_SPKR_OUTR_P_CONN → JA101 10-89-7082 M-ST-TH → AUD_SPKR_OUTR_N_CONN → LA133 180-OHM-1.5A 0603 → AUD_SPKR_OUTR_N 100

100 AUD_SPKR_OUTL_N → LA131 180-OHM-1.5A 0603 → AUD_SPKR_OUTL_N_CONN → AUD_SPKR_OUTL_P_CONN → LA134 180-OHM-1.5A 0603 → AUD_SPKR_OUTL_P 100

NET_SPACING_TYPE=AUDIO MIN_LINE_WIDTH=20MIL MIN_NECK_WIDTH=12MIL

AUDIO_GPIO_12_CONN

103 102 101 100 95 7 PP3V3_AUDIO → RA113 47K 5% 1/16W MF 402 → 25 AUDIO_GPIO_12

SPEAKER TYPE DETECT TO SHASTA GPIO

LA132 1000-OHM-200MA 0603

CA119 1000PF 5% 25V CERM 603

CA125 1000PF 5% 25V CERM 603

NOSTUFF CA104 1000PF 5% 25V CERM 603

NOSTUFF CA105 1000PF 5% 25V CERM 603

NOSTUFF CA106 1000PF 5% 25V CERM 603

NOSTUFF CA107 1000PF 5% 25V CERM 603

CA126 1000PF 5% 25V CERM 603

CA127 1000PF 5% 25V CERM 603

101 7 GND_CHASSIS_AUDIO_INTERNAL

LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED

AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED

103 102 101 100 95 7 PP3V3_AUDIO → RA100 100K 5% 1/16W MF 402 → RA102 47K 5% 1/16W MF 402 → 101 AUD_LI_DET_H

RA101 47K 5% 1/16W MF 402 → TO SHASTA GPIO → AUDIO_LI_DET_L 25

QA100 2N7002 SM (AUDLINDETH)

CA108 0.1UF 20% 10V CERM 402

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED

AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED

AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

103 102 101 100 95 7 PP3V3_AUDIO

RA103 100K 5% 1/16W MF 402 → RA104 47K 5% 1/16W MF 402 → TO SHASTA GPIO → AUDIO_LO_DET_L 6 25

QA101 2N7002DW SOT-363

101 AUD_LO_DET1 → RA105 47K 5% 1/16W MF 402 → AUD_LO_DET1_1 → CA109 0.1UF 20% 10V CERM 402

103 102 101 100 95 7 PP3V3_AUDIO

RA106 100K 5% 1/16W MF 402 → RA107 47K 5% 1/16W MF 402 → TO SHASTA GPIO → AUDIO_LO_OPTICAL_PLUG_L 25

QA101 2N7002DW SOT-363

101 AUD_LO_DET2 → RA108 47K 5% 1/16W MF 402 → AUD_LO_DET2_1 → CA110 0.1UF 20% 10V CERM 402

NOSTUFF RA109 100K 5% 1/16W MF 402

LINE OUT JACK

APPLE P/N 514-0204

JA103 JFJ8210 F-ST-TH

AUD_LO_GND_JACK

AUD_LO_DET1_JACK

AUD_LO_R_JACK

AUD_LO_L_JACK

AUD_LO_DET2_JACK

LED: VIN, VDD, GND

MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL AUD_SPDIF_GND

RA112 0 5% 1/16W MF 402

PLACE NEAR J9801 XCA100 50R28

PLACE NEAR J700 XCA101 50R28

101 7 GND_CHASSIS_AUDIO_INTERNAL

MIC CABLE CONNECTOR

APPLE P/N 518-0034

JA102 HF28 M-ST-TH

GND_AUDIO_MIC_CONN

AUD_MIC_IN_P_CONN

AUD_MIC_IN_N_CONN

LA108 FERR-EMI-100-OHM SM — 102 GND_AUDIO_MIC → GND_AUDIO_MIC_EMI

LA109 FERR-EMI-100-OHM SM — 102 AUD_MIC_IN_P → AUD_MIC_IN_P_EMI

LA110 FERR-EMI-100-OHM SM — 102 AUD_MIC_IN_N → AUD_MIC_IN_N_EMI

LA111 FERR-EMI-100-OHM SM

LA112 FERR-EMI-100-OHM SM

LA113 FERR-EMI-100-OHM SM

CA120 1000PF 10% 25V X7R 402

CA121 1000PF 10% 25V X7R 402

CA122 1000PF 10% 25V X7R 402

101 7 GND_CHASSIS_AUDIO_INTERNAL

LA114 FERR-EMI-100-OHM SM — 103 95 AUD_SPDIF_OUT → AUD_SPDIF_OUT_EMI → AUD_SPDIF_OUT_JACK

LA115 FERR-EMI-100-OHM SM — 7 PP5V_AUDIO → PP5V_AUDIO_SPDIF_EMI → PP5V_AUDIO_SPDIF_JACK

LA116 FERR-EMI-100-OHM SM — 101 AUD_LO_DET1 → AUD_LO_DET1_EMI → AUD_LO_DET1_JACK

LA117 FERR-EMI-100-OHM SM — 98 AUD_LO_R → AUD_LO_R_EMI → AUD_LO_R_JACK

LA118 FERR-EMI-100-OHM SM — 98 AUD_LO_L → AUD_LO_L_EMI → AUD_LO_L_JACK

LA119 FERR-EMI-100-OHM SM — 101 AUD_LO_DET2 → AUD_LO_DET2_EMI → AUD_LO_DET2_JACK

LA120 FERR-EMI-100-OHM SM — 98 AUD_LO_GND → AUD_LO_GND_EMI

LA121 FERR-EMI-100-OHM SM — 98 AUD_LO_GND_PRB → AUD_LO_GND_PRB_EMI

LA122 FERR-EMI-100-OHM SM

LA123 FERR-EMI-100-OHM SM

LA124 FERR-EMI-100-OHM SM

LA125 FERR-EMI-100-OHM SM

LA126 FERR-EMI-100-OHM SM

LA127 FERR-EMI-100-OHM SM

LA128 FERR-EMI-100-OHM SM

LA129 FERR-EMI-100-OHM SM

MIN_LINE_WIDTH=12MIL MIN_NECK_WIDTH=8MIL

CA117 0.1UF 20% 10V CERM 402

CA118 1UF 10% 10V CERM 805

CA123 100PF 5% 50V CERM 402

CA124 100PF 5% 50V CERM 402

CA111 100PF 5% 50V CERM 402

CA112 100PF 5% 50V CERM 402

CA113 100PF 5% 50V CERM 402

CA114 100PF 5% 50V CERM 402

CA115 100PF 5% 50V CERM 402

CA116 0.01UF 10% 16V CERM 402

AUD_LI_GND_EMI 101

DZA101 MMBZ15DLT1 15V SOT23

102 101 7 GND_CHASSIS_AUDIO_EXTERNAL

AUDIO: Q45 CONNECTORS

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D	051-6482	I
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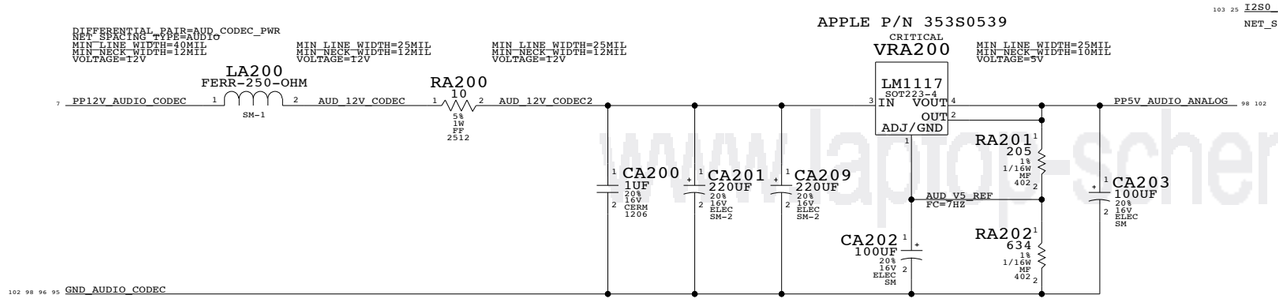
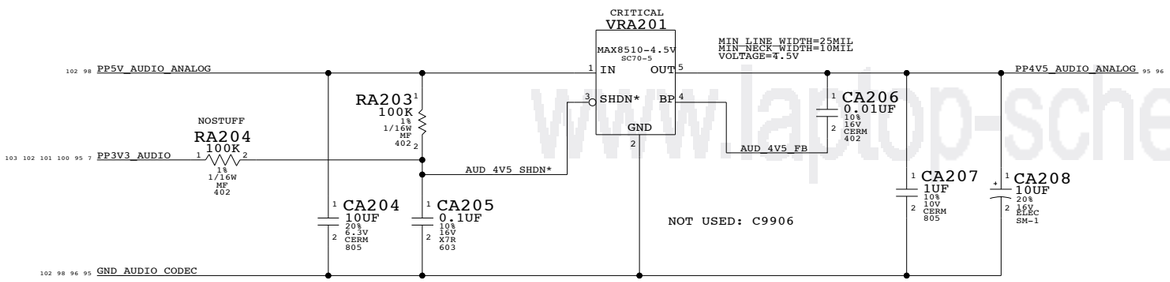
5V POWER SUPPLY FOR THE HEADPHONES/LINE OUT AMP

APPLE P/N 353S0539

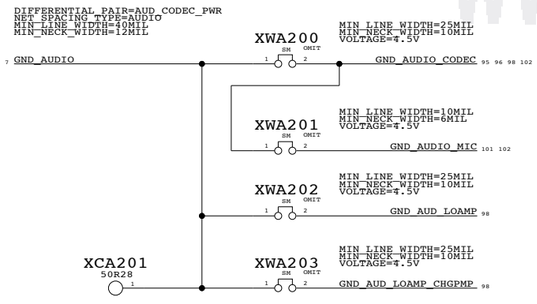


4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

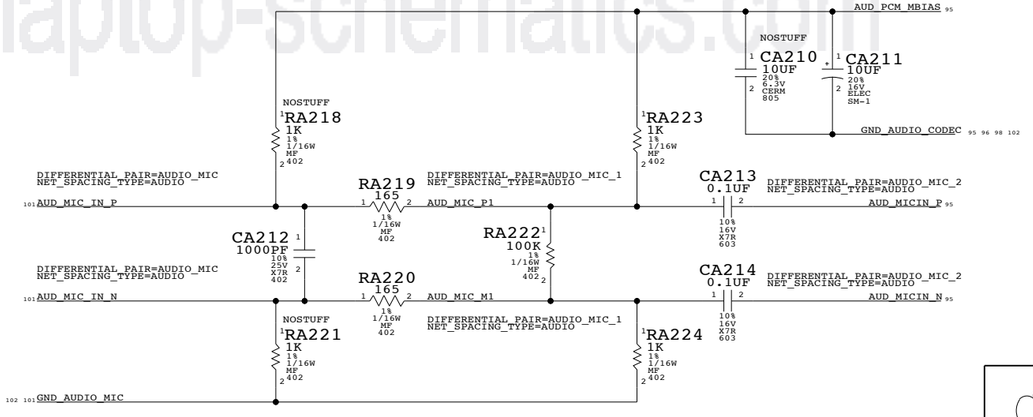
APPLE P/N 353S0733

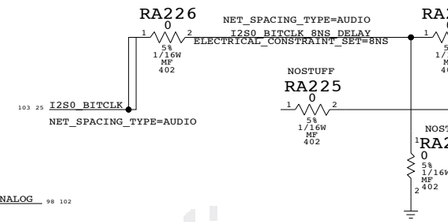


AUDIO GROUND RETURNS

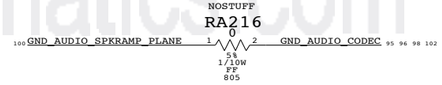


MICROPHONE IMPEDANCE MATCHING CIRCUIT

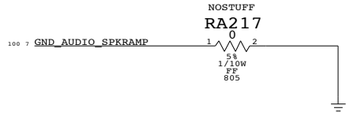




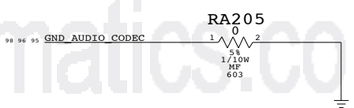
PLACE ACROSS GROUND SPLIT
AT RIGHT SIDE OF CA007



PLACE NEAR ENTRY TO SPEAKER
AMP GROUND PLANE

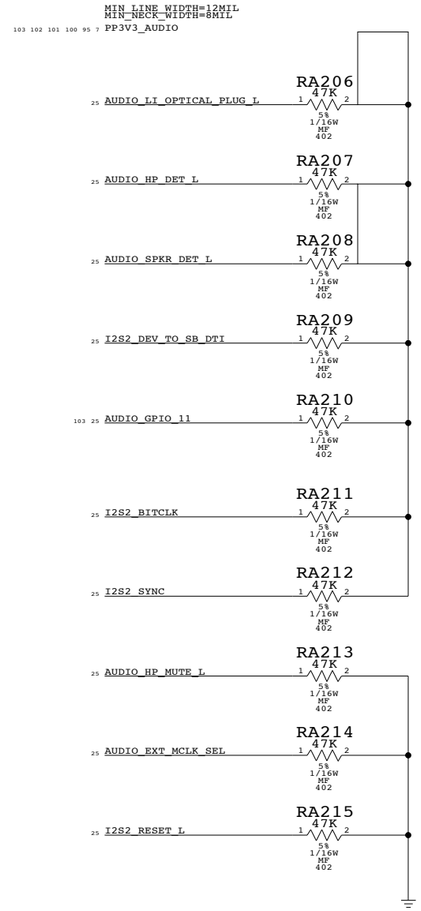


PLACE ACROSS GROUND SPLIT
AT CODEC U9500



PLACE AT J5903

UNUSED GPIO TERMINATIONS



MAKE_BASE=TRUE I88
TP_I2S2_SB_TO_DEV_DTO — I2S2_SB_TO_DEV_DTO

MAKE_BASE=TRUE I89
TP_I2S2_MCLK — I2S2_MCLK

MAKE_BASE=TRUE I116
I2S0_MCLK — AUD_CODEC_MCLK

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AUDIO: Q45 POWER SUPPLIES

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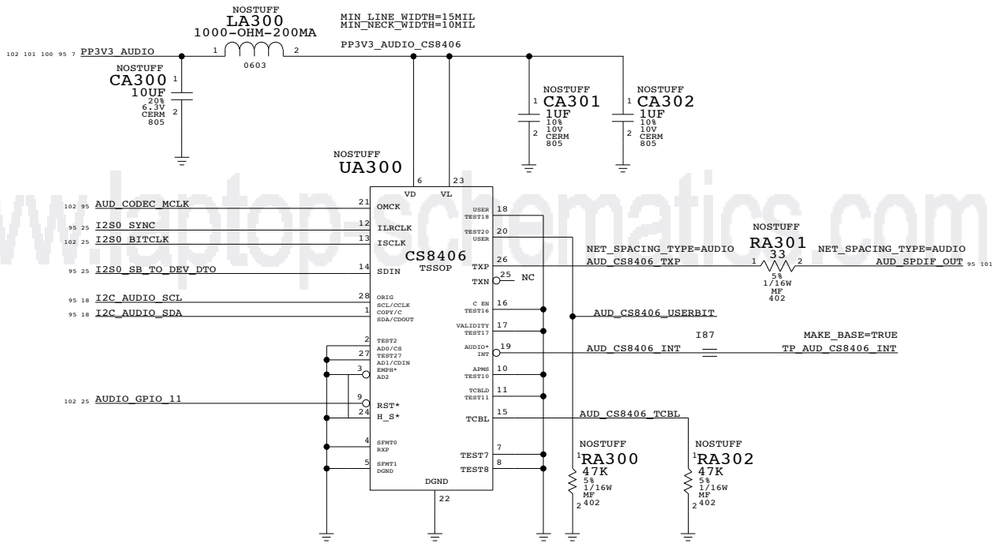
S/PDIF TRANSMITTER
I2C ADDRESS = 0010 000X

APPLE P/N 353S0597



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AUDIO: S/PDIF XMITTER

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D	051-6482	I
SCALE: NONE	SHT 103 OF 103	