1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

DRAWING REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
C		329994	PRODUCTION RELEASED	05/27/04?	

SCHEM,MLB,PB15

Thu May 27 14:58:03 2004

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9	INTREPID MEMORY INTERFACE / BOOT ROM
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11	400PIN STACKED DDR SODIMM CONNECTOR
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16	INTREPID DECOUPLING
17	USB 2.0 INTERFACE (uPD720101)
18	CARDBUS INTERFACE (PCI1510)
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43	COMPONENT LOCATIONS (2 OF 2)

BOM OPTIONS (IN COMMON PARTS)

STUFF	NO STUFF
1_8V_MAXBUS	1_5V_MAXBUS
NO_SSCG	SSCG
5V_HD_LOGIC	3V_HD_LOGIC
NO_BBANG	BBANG
INT_2_5V_COLD	INT_2_5V_HOT
ATI_MEMIO_HI	ATI_MEMIO_LO
SOFT_MODEM	USB_MODEM
GPU_PWRMSR	EXT_TMDS
GPU_SS	
VGA_BUFFER_RES	
INT_TMDS	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6653	1	SCHEM,MLB,PB15	SCH1	
820-1600	1	PCBF,MLB,PB15	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

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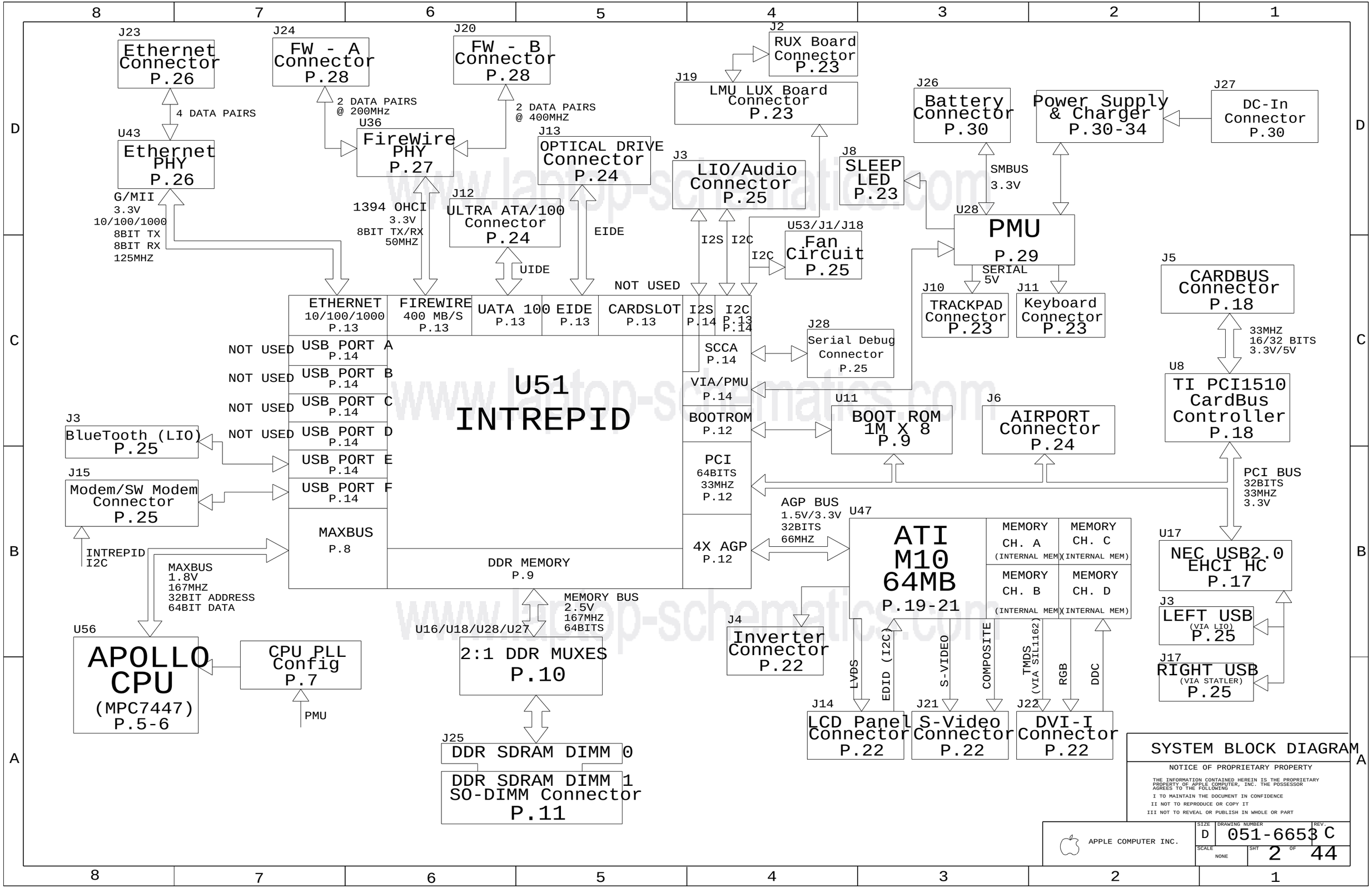
TITLE
SCHEM,MLB,PB15

DRAWING NUMBER 051-6653 REV. C


J23
Ethernet Connector P.26
4 DATA PAIRS
U43
Ethernet PHY P.26
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
J24
FW - A Connector P.28
2 DATA PAIRS @ 200MHz
U36
FireWire PHY P.27
1394 OHCI
3.3V
8BIT TX/RX
50MHZ
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MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
U51
INTREPID
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47
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MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
DDR MEMORY P.9
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27
2:1 DDR MUXES P.10
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EDID (I2C)
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COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC
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PMU
J14
LCD Panel Connector P.22
J21
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DDR SDRAM DIMM 1
SO-DIMM Connector P.11
SYSTEM BLOCK DIAGRAM
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SHT 2 OF 44

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 30

INRUSH LIMITER PG 30

+24V_PBUS

1V20_REF
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF
PG 31

RUN/SS
BUCK REGULATOR (LTC1625) PG 31
VCC
AC: 12.8V
NO AC: BATTERY VOLTAGE 1625 NOT RUNNING
SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 31

+BATT

+5V_MAIN

+3V_PMU

+4_6V_BU

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 32
VCC
PGOOD
STBYMD
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN

3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 31

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS
AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V
(UNTIL DRAINED)

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

DC/DC (LTC3411) PG 34
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

+1.8V_MAIN

MAXBUS

BATTERY CHARGER (MAX1772) PG 30

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 30

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC
MAIN 2.5V/1.5V DC/DC (MAX1715) PG 34
SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING
TURNS ON OUTPUT @ 2.4V
ON1/ON2

PGOOD

1_5V_2_5V_OK

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER
+2.5V_MAIN

+1.5V_MAIN
INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING
DCDC_EN_L WILL PULL ON1/ON2
LOW IN SHUTDOWN

+PBUS

+5V_MAIN

VCC
EXT_VCC
DC/DC (LTC1778)
SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP
D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

DCDC_EN
SLEEP

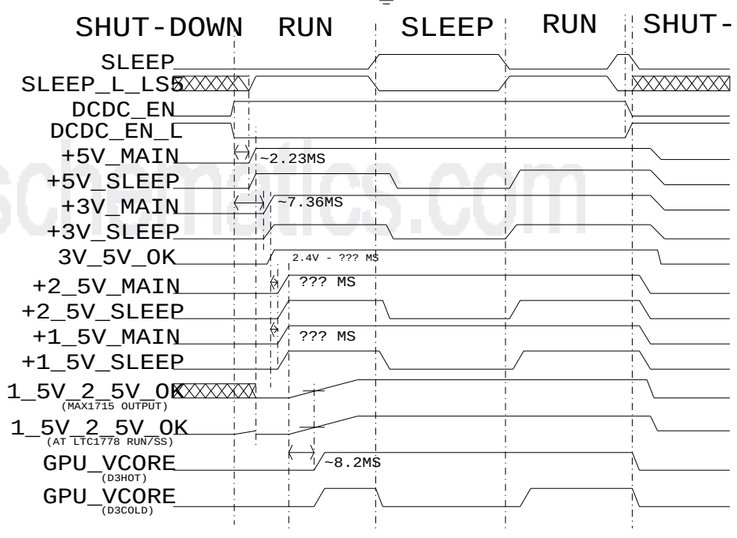
MAXBUS SEQUENCING

+PBUS

+5V_MAIN

VCC
SHDN
DC/DC (MAX1717)
SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING
PG 33

CPU_VCORE (+1.385V)



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POWER BLOCK DIAGRAM

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PCB SPECS

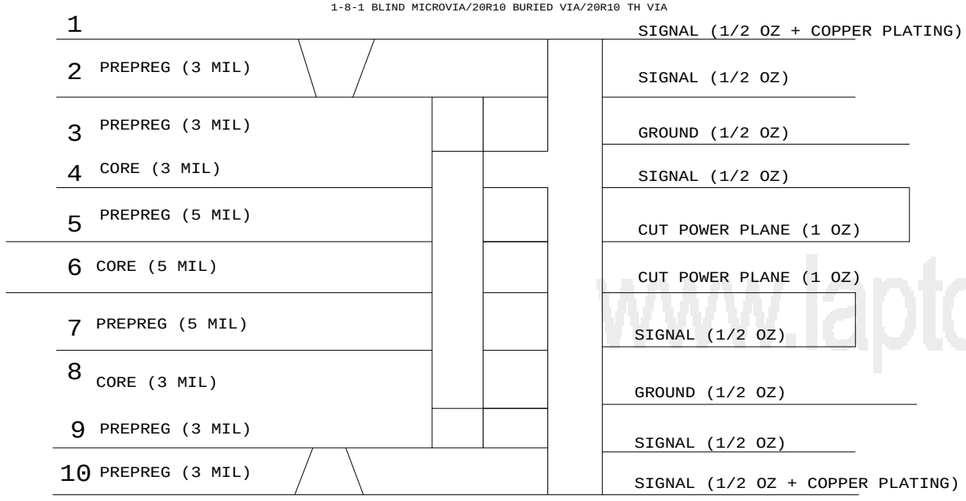
THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA



BOARD HOLES

CHASSIS MOUNTS

ASICS HEATSINK MOUNTS

ZT7 HOLE-VIA-20R10LEFT CPU
ZT21 HOLE-VIA-20R10UPPER RT GPU
ZT58 HOLE-VIA-20R10LWR CPU
ZT59 HOLE-VIA-20R10LWR RT GPU

I/O AREA

ZT85 HOLE-VIA-20R10 DVI CHGND2
ZT86 HOLE-VIA-20R101394 DVI CHGND1
ZT16 HOLE-VIA-20R10 BATT. CHRGR CHGND5

INVERTER

SH1 0G-503040 SHLD-SM CHGND3

MECH. HOLES

ZT74 HOLE-VIA-20R10
ZT36 HOLE-VIA-20R10 ZT301 SPN NO_TEST=TRUE
ZT23 HOLE-VIA-20R10 ZT302 SPN NO_TEST=TRUE
ZT42 HOLE-VIA-20R10 ZT10 SPN NO_TEST=TRUE

GROUND VIAS

ZT76 ZT28 ZT72 ZT69 ZT68 ZT64 ZT61 ZT38 ZT39 ZT40 ZT41 ZT46 ZT71 ZT78 ZT80
ZT50 ZT51 ZT52 ZT53 ZT57 ZT60 ZT82 ZT22 ZT17 ZT35 ZT45 ZT79 ZT81 ZT83 ZT49
ZT48 ZT47 ZT54 ZT55 ZT56 ZT84 ZT5 ZT15 ZT44 ZT4 ZT8 ZT6 ZT32 ZT3 ZT10
ZT11 ZT34 ZT20 ZT43 ZT70 ZT2 ZT9 ZT75 ZT73 ZT63 ZT77 ZT66 ZT62 ZT65 ZT13
ZT25 ZT19 ZT24 ZT67 ZT37 ZT29 ZT31 ZT1 ZT14 ZT12 ZT27 ZT26 ZT30 ZT33 ZT18

(all HOLE-VIA-20R10)

BOARD INFORMATION

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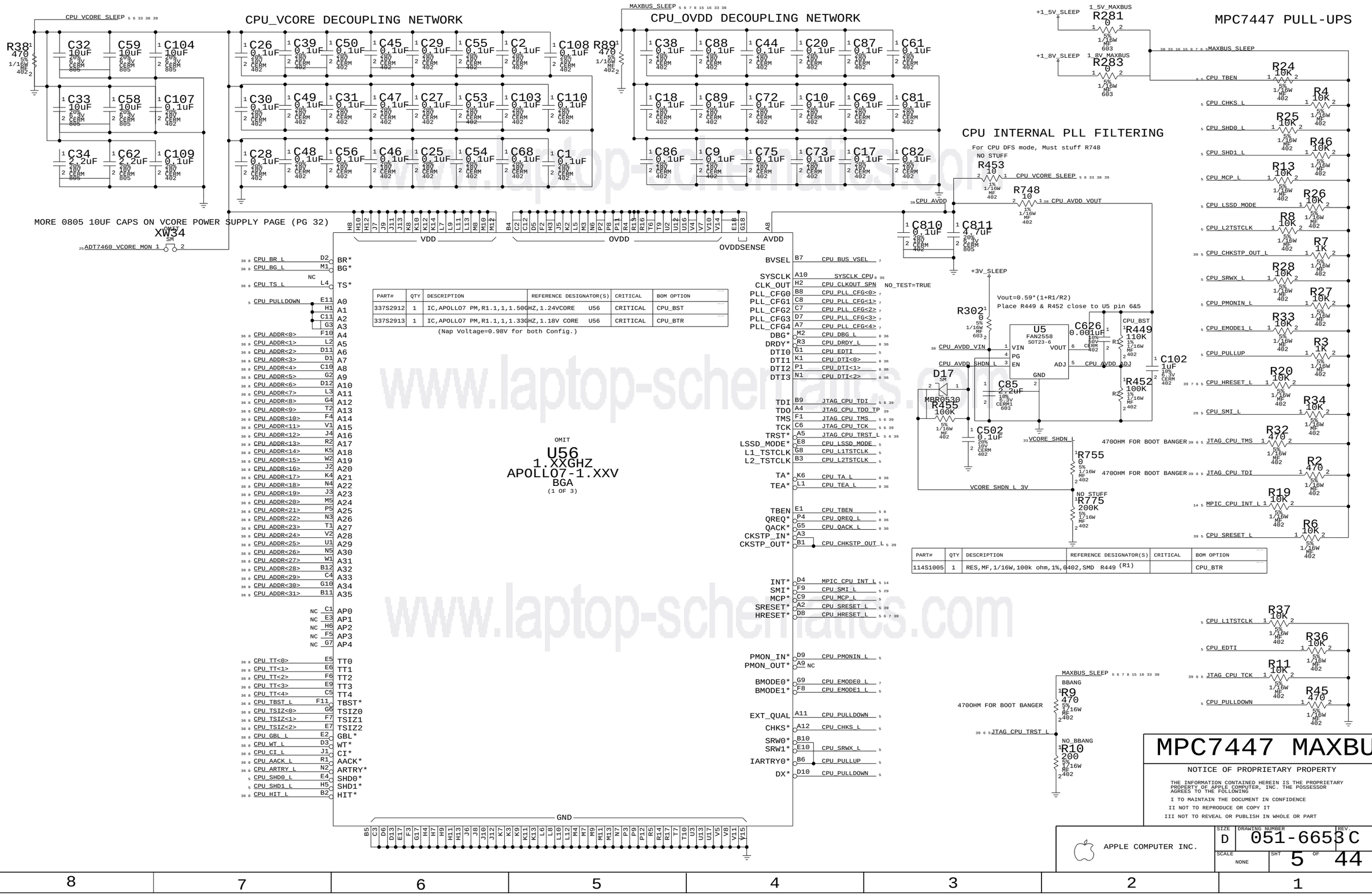
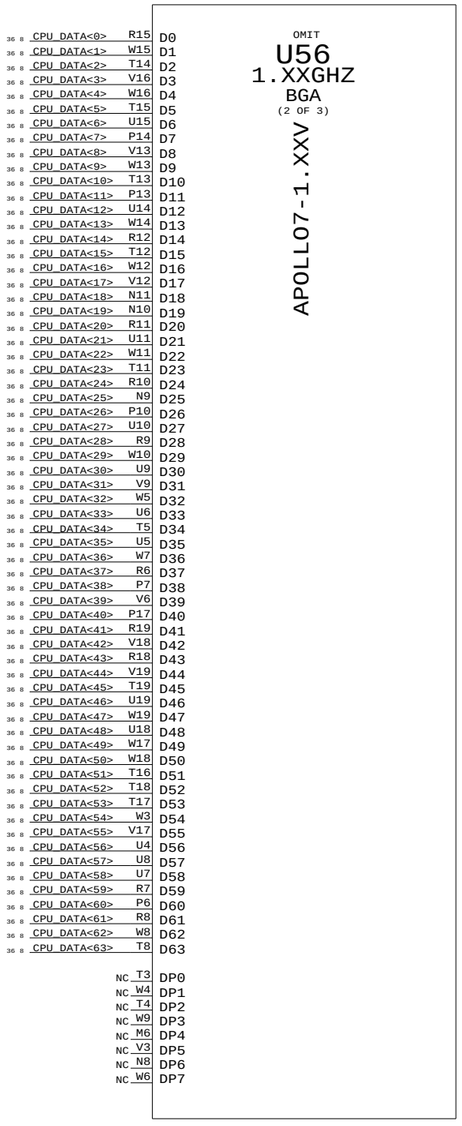


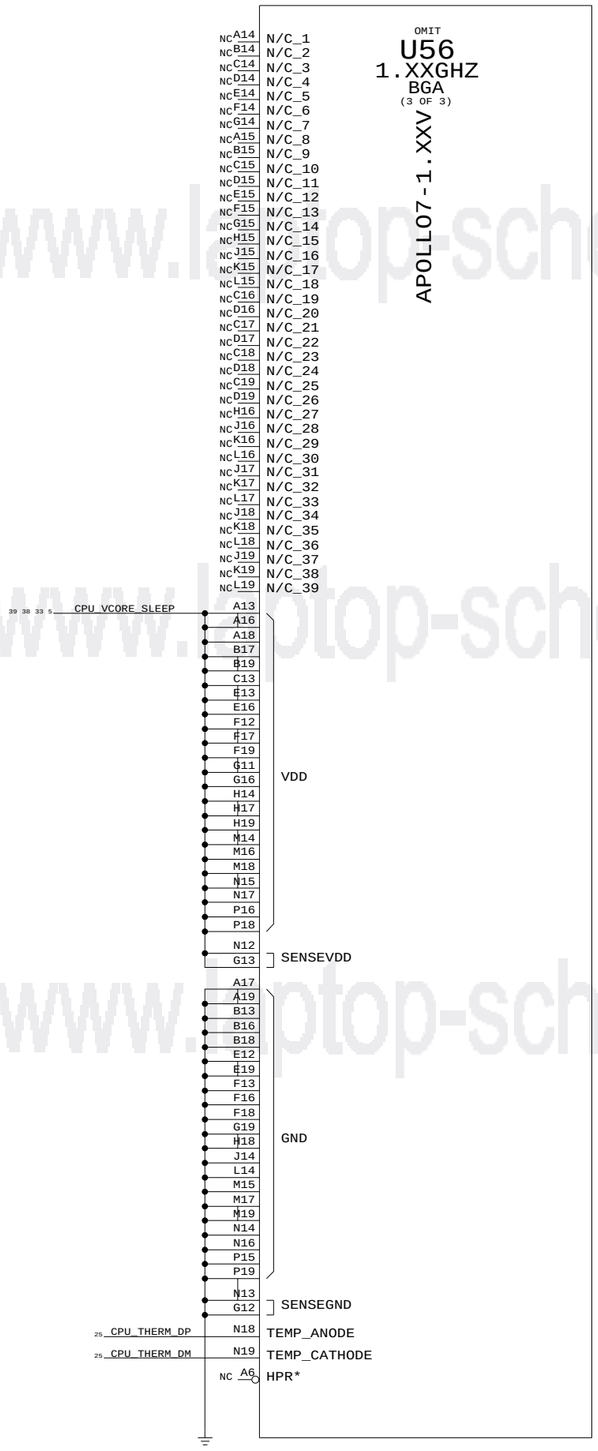
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2912	1	IC,APOLLO7 PM,R1.1,1,1.50GHZ,1.24VCORE	U56	CRITICAL	CPU_BST
337S2913	1	IC,APOLLO7 PM,R1.1,1,1.33GHZ,1.18V CORE	U56	CRITICAL	CPU_BTR

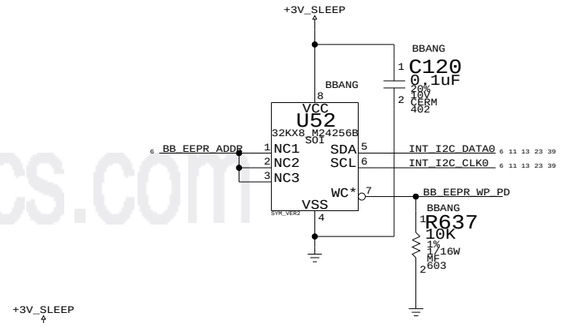
(Nap Voltage=0.98V for both Config.)

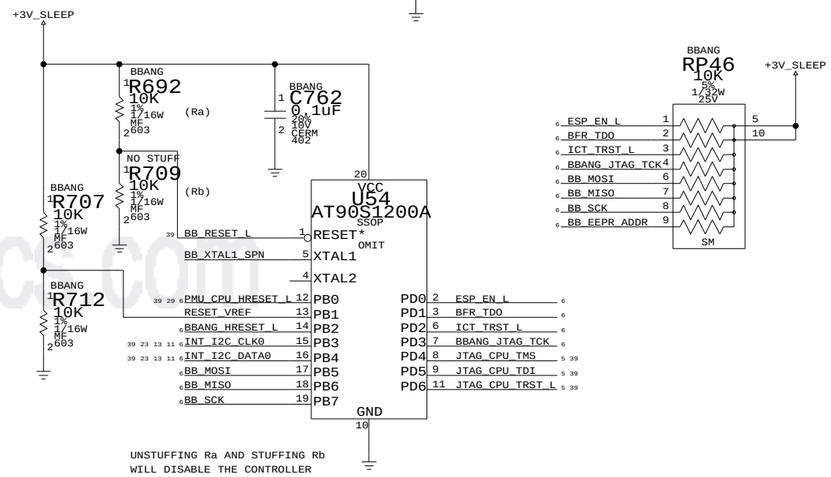
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S1005	1	RES,MF,1/16W,100k ohm,1%,0402,SMD R449 (R1)			CPU_BTR

BOOT BANGER - TWEAK PROCESSOR BITS AFTER POWER-ON

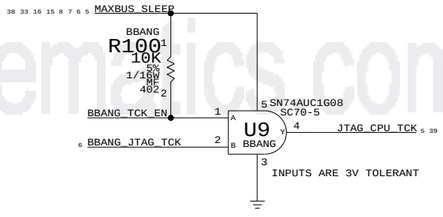


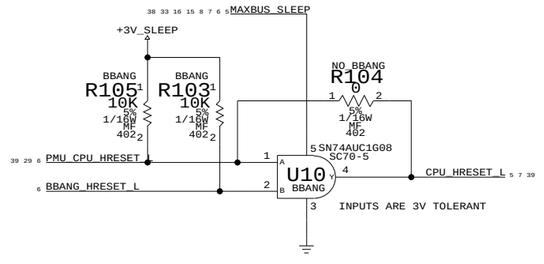






PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1135	1	MCU,PROGRAMMED W/ BBANGER	U54	BBANG





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MPC7447/BBANG

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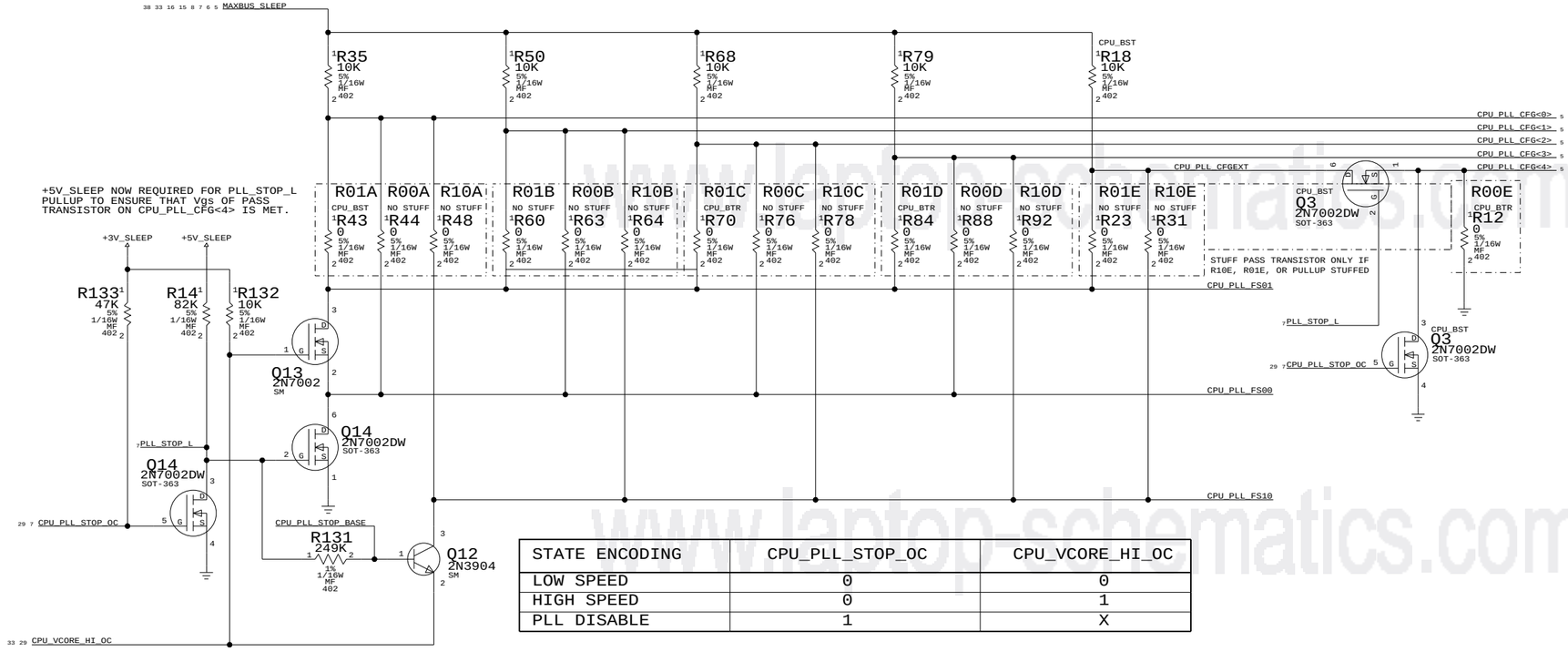
CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

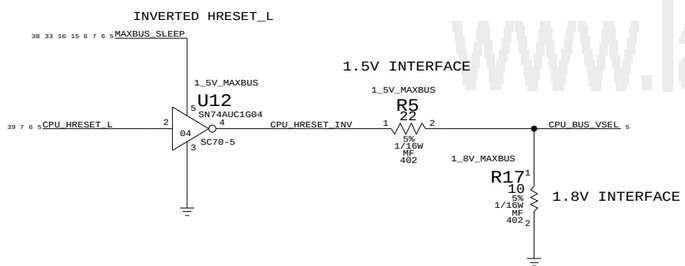
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 0123 E ABCD HEX
0.0X	PLL OFF		0 1111 0F
1.0X	PLL BYPASS		0 0011 03
2.0X	333	267	0 0100 04
3.0X	500	400	0 1000 08
4.0X	667	533	0 1010 0A
5.0X	833	667	0 1011 0B
5.5X	917	733	0 1001 09
6.0X	1000	800	0 1101 0D
6.5X	1083	867	0 0101 05
7.0X	1167	933	0 0010 02
7.5X	1250	1000	0 0001 01
8.0X	1333	1067	0 1100 0C
8.5X	1417	1133	0 0110 06
9.0X	1500	1200	1 0111 17
9.5X	1583	1267	0 0111 07
10.0X	1667	1333	1 1010 1A
10.5X	1750	1400	1 1000 18
11.0X	1833	1467	1 1001 19
11.5X	1917	1533	0 0000 00
12.0X	2000	1600	1 1011 1B
12.5X	2083	1667	1 1111 1F
13.0X	2167	1733	1 0101 15
13.5X	2250	1800	0 1110 0E
14.0X	2333	1867	1 1100 1C
15.0X	2500	2000	1 0001 11
16.0X	2667	2133	1 1101 1D
17.0X	2833	2267	1 0000 10
18.0X	3000	2400	1 0010 12
20.0X	3333	2667	1 0011 13
21.0X	3500	2800	1 0100 14
24.0X	4000	3200	1 0110 16
28.0X	4667	3733	1 1110 1E

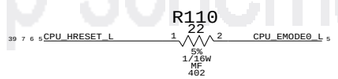
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

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CPU CONFIGURATION

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D	051-6653	C
SCALE: NONE	SHT 7 OF 44	

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS SLEEP

NO STUFF R640 10K 5% 1/16W MF 402
NO STUFF R639 10K 5% 1/16W MF 402
NO STUFF R638 10K 5% 1/16W MF 402
R666 10K 5% 1/16W MF 402

CPU_DATA<32>
CPU_DATA<33>
CPU_DATA<34>
CPU_DATA<35>
CPU_DATA<36>
CPU_DATA<37>
CPU_DATA<38>
CPU_DATA<39>

NO STUFF R622 10K 5% 1/16W MF 402
R619 10K 5% 1/16W MF 402
R618 10K 5% 1/16W MF 402
NO STUFF R653 10K 5% 1/16W MF 402
R621 10K 5% 1/16W MF 402
R620 10K 5% 1/16W MF 402
R652 10K 5% 1/16W MF 402
R650 10K 5% 1/16W MF 402

- BOOT_TPModeEnable_h: 0: TDI output (JTAG); 1: TDI input
- AnalyzerClk_En_h: 0: Active; 1: Active
- BOOT_TPDebug_h: 0: Active low; 1: Active high
- ExtPLL_SDwn_Pol: 0: Active low; 1: Active high
- Spare
- Spare
- Spare
- Spare

BIT 40 TO 47

MAXBUS SLEEP

NO STUFF R641 10K 5% 1/16W MF 402
SSCG R665 10K 5% 1/16W MF 402
NO STUFF R664 10K 5% 1/16W MF 402
NO_SSCG R693 10K 5% 1/16W MF 402
NO STUFF R694 10K 5% 1/16W MF 402
NO STUFF R699 10K 5% 1/16W MF 402

CPU_DATA<40>
CPU_DATA<41>
CPU_DATA<42>
CPU_DATA<43>
CPU_DATA<44>
CPU_DATA<45>
CPU_DATA<46>
CPU_DATA<47>

NO_SSCG R648 10K 5% 1/16W MF 402
R677 10K 5% 1/16W MF 402
R623 10K 5% 1/16W MF 402
NO_SSCG R651 10K 5% 1/16W MF 402
R649 10K 5% 1/16W MF 402
SSCG R678 10K 5% 1/16W MF 402
R679 10K 5% 1/16W MF 402
R684 10K 5% 1/16W MF 402

- Spare
- Spare
- BIT2
- BIT1
- BIT0
- Internal Spread Enable: 0: Active; 1: Active
- PCI Bus Source Clock (no spread): 0: PLL2 (no spread); 1: PLL3 (no spread)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS SLEEP

SSCG R696 10K 5% 1/16W MF 402
SSCG R695 10K 5% 1/16W MF 402
NO STUFF R667 10K 5% 1/16W MF 402
NO STUFF R668 10K 5% 1/16W MF 402
NO STUFF R643 10K 5% 1/16W MF 402
NO STUFF R642 10K 5% 1/16W MF 402
R698 10K 5% 1/16W MF 402

CPU_DATA<48>
CPU_DATA<49>
CPU_DATA<50>
CPU_DATA<51>
CPU_DATA<52>
CPU_DATA<53>
CPU_DATA<54>
CPU_DATA<55>

NO_SSCG R681 10K 5% 1/16W MF 402
NO_SSCG R680 10K 5% 1/16W MF 402
NO STUFF R654 10K 5% 1/16W MF 402
R655 10K 5% 1/16W MF 402
R625 10K 5% 1/16W MF 402
R624 10K 5% 1/16W MF 402
NO STUFF R683 10K 5% 1/16W MF 402
R626 10K 5% 1/16W MF 402

- BUF_REF_CLK_OUTEnable_h: 0: Active; 1: Active
- SelPLL4extsrc: 0: Internal source; 1: External source
- EnPCIROMPullup: 0: Boot ROM on PCI; 1: Boot ROM on PCI
- OBSOLETE (should remain high)
- EnPCIROMPullup: 0: Boot ROM on PCI; 1: Boot ROM on CardSlot
- EnTI1394bWorkaround: 0: TI 1394b workaround; 1: No TI 1394b workaround
- BIT2
- BIT1
- BIT0
- Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

R159 4.7 5% 1/16W MF 402
+1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7
C187 0.22µF 20% 6.3V CERM 402

H26 VDD15A_7 (PLL6) OMIT

U51 INTREPID-REV2.1 BGA

CPU_BR_L	E29	BR	INPUT
CPU_BG_L	E26	BG	NO BUS KEEPER
CPU_TS_L	B27	TS	NO BUS KEEPER
CPU_ADDR<0>	D24	A_0	
CPU_ADDR<1>	D25	A_1	
CPU_ADDR<2>	A27	A_2	
CPU_ADDR<3>	E24	A_3	
CPU_ADDR<4>	G23	A_4	
CPU_ADDR<5>	B26	A_5	
CPU_ADDR<6>	A26	A_6	
CPU_ADDR<7>	D23	A_7	
CPU_ADDR<8>	A25	A_8	
CPU_ADDR<9>	E23	A_9	
CPU_ADDR<10>	J22	A_10	
CPU_ADDR<11>	B25	A_11	
CPU_ADDR<12>	H22	A_12	
CPU_ADDR<13>	G22	A_13	
CPU_ADDR<14>	D22	A_14	
CPU_ADDR<15>	B24	A_15	
CPU_ADDR<16>	B23	A_16	
CPU_ADDR<17>	E22	A_17	
CPU_ADDR<18>	J21	A_18	
CPU_ADDR<19>	G21	A_19	
CPU_ADDR<20>	E21	A_20	
CPU_ADDR<21>	A24	A_21	
CPU_ADDR<22>	D21	A_22	
CPU_ADDR<23>	A23	A_23	
CPU_ADDR<24>	H20	A_24	
CPU_ADDR<25>	B22	A_25	
CPU_ADDR<26>	H21	A_26	
CPU_ADDR<27>	A22	A_27	
CPU_ADDR<28>	E20	A_28	
CPU_ADDR<29>	B21	A_29	
CPU_ADDR<30>	D20	A_30	
CPU_ADDR<31>	A21	A_31	
CPU_CI_L	G26	CI	
CPU_GBL_L	A29	GBL	
CPU_TBST_L	A28	TBST	
CPU_TSIZ<0>	G24	TSIZ_0	
CPU_TSIZ<1>	H24	TSIZ_1	
CPU_TSIZ<2>	D26	TSIZ_2	
CPU_TT<0>	E25	TT_0	
CPU_TT<1>	G25	TT_1	
CPU_TT<2>	B28	TT_2	
CPU_TT<3>	D27	TT_3	
CPU_TT<4>	J25	TT_4	
CPU_WT_L	D28	WT	
CPU_AACK_L	B29	AACK	NO BUS KEEPER - PU
CPU_ARTRY_L	H23	ARTRY	NO BUS KEEPER - PU
CPU_HIT_L	B31	HIT	INPUT - PU
CPU_QREQ_L	A32	QREQ	INPUT - PD
CPU_QACK_L	G27	QACK	NO BUS KEEPER - ?
INT_SUSPEND_REQ_L	AK9	SUSPENDREQ	
INT_SUSPEND_ACK_L	AM8	SUSPENDACK	

(1 OF 9) CRITCAL

MAXBUS INTERFACE

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

INT_CPUFB_IN	J24	CPU_FB_IN	
INT_CPUFB_OUT	H16	CPU_FB_OUT	NO BUS KEEPER - PU
SYSCLK_LA_TP	G8	ANALYZER_CLK	
CPU_CLK_EN	AH9	STOPCPUCLK	INPUT - PU
INTREPID_ACS_REF	H13	ACS_REF	NO BUS KEEPER - ?
SYSCLK_CPU_UF	J15	CPU_CLK	NO BUS KEEPER - ?
CPU_TBEN	A31	TBEN	NO BUS KEEPER - PU

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

DBG	A30	CPU_DBG_L	
DRDY	G28	CPU_DRDY_L	
DTI_0	K25	CPU_DTI<0>	
DTI_1	D29	CPU_DTI<1>	
DTI_2	B30	CPU_DTI<2>	
TA	E27	CPU_TA_L	
TEA	E28	CPU_TEA_L	

D_0	D10	CPU_DATA<0>	
D_1	G12	CPU_DATA<1>	
D_2	E11	CPU_DATA<2>	
D_3	H11	CPU_DATA<3>	
D_4	B9	CPU_DATA<4>	
D_5	B8	CPU_DATA<5>	
D_6	A9	CPU_DATA<6>	
D_7	A8	CPU_DATA<7>	
D_8	E12	CPU_DATA<8>	
D_9	D11	CPU_DATA<9>	
D_10	B10	CPU_DATA<10>	
D_11	J13	CPU_DATA<11>	
D_12	A10	CPU_DATA<12>	
D_13	D12	CPU_DATA<13>	
D_14	E13	CPU_DATA<14>	
D_15	G13	CPU_DATA<15>	
D_16	B11	CPU_DATA<16>	
D_17	D13	CPU_DATA<17>	
D_18	A11	CPU_DATA<18>	
D_19	G14	CPU_DATA<19>	
D_20	H14	CPU_DATA<20>	
D_21	E14	CPU_DATA<21>	
D_22	B12	CPU_DATA<22>	
D_23	G15	CPU_DATA<23>	
D_24	B13	CPU_DATA<24>	
D_25	H15	CPU_DATA<25>	
D_26	D14	CPU_DATA<26>	
D_27	B14	CPU_DATA<27>	
D_28	A12	CPU_DATA<28>	
D_29	G16	CPU_DATA<29>	
D_30	E15	CPU_DATA<30>	
D_31	J16	CPU_DATA<31>	
D_32	D15	CPU_DATA<32>	
D_33	A14	CPU_DATA<33>	
D_34	A13	CPU_DATA<34>	
D_35	D16	CPU_DATA<35>	
D_36	E16	CPU_DATA<36>	
D_37	G17	CPU_DATA<37>	
D_38	B15	CPU_DATA<38>	
D_39	H17	CPU_DATA<39>	
D_40	A15	CPU_DATA<40>	
D_41	B16	CPU_DATA<41>	
D_42	E17	CPU_DATA<42>	
D_43	A16	CPU_DATA<43>	
D_44	J18	CPU_DATA<44>	
D_45	H18	CPU_DATA<45>	
D_46	D17	CPU_DATA<46>	
D_47	G18	CPU_DATA<47>	
D_48	A17	CPU_DATA<48>	
D_49	B17	CPU_DATA<49>	
D_50	E18	CPU_DATA<50>	
D_51	B18	CPU_DATA<51>	
D_52	D18	CPU_DATA<52>	
D_53	A18	CPU_DATA<53>	
D_54	A19	CPU_DATA<54>	
D_55	H19	CPU_DATA<55>	
D_56	B19	CPU_DATA<56>	
D_57	J19	CPU_DATA<57>	
D_58	A20	CPU_DATA<58>	
D_59	D19	CPU_DATA<59>	
D_60	E19	CPU_DATA<60>	
D_61	G19	CPU_DATA<61>	
D_62	B20	CPU_DATA<62>	
D_63	G20	CPU_DATA<63>	

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R169 511 1% 1/16W MF 402
R168 0 5% 1/16W MF 402 (SYSCLK_CPU → SYSCLK_CPU_UF)
R161 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH

R155 0 5% 1/16W MF 402 (INT_CPUFB_OUT2 → INT_CPUFB_OUT_SHORT)
R140 0 5% 1/16W MF 402 (INT_CPUFB_OUT_SHORT → INT_CPUFB_OUT_NORM)
R128 NO STUFF 0 5% 1/16W MF 402 (INT_CPUFB_OUT_NORM → INT_CPUFB_LONG)
R146 NO STUFF 0 5% 1/16W MF 402
R141 0 5% 1/16W MF 402
R147 0 5% 1/16W MF 402 (INT_CPUFB_IN → INT_CPUFB_IN_NORM)
R136 NO STUFF 0 5% 1/16W MF 402

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCIISPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS

MAXBUS SLEEP

RP3 10K 5% 1/16W SM1
- CPU_TS_L
- CPU_TA_L
- CPU_ARTRY_L

RP2 10K 5% 1/16W SM1
- CPU_BR_L
- CPU_HIT_L
- CPU_DRDY_L
- CPU_TEA_L
- CPU_AACK_L

R152 10K 5% 1/16W MF 402 (CPU_HIT_L)
R150 10K 5% 1/16W MF 402 (CPU_DBG_L)
R151 10K 5% 1/16W MF 402 (CPU_QREQ_L)

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS SLEEP

NO STUFF R669 10K 5% 1/16W MF 402
NO STUFF R645 10K 5% 1/16W MF 402
NO STUFF R697 10K 5% 1/16W MF 402
NO STUFF R670 10K 5% 1/16W MF 402
R644 10K 5% 1/16W MF 402
NO STUFF R646 10K 5% 1/16W MF 402

CPU_DATA<56>
CPU_DATA<57>
CPU_DATA<58>
CPU_DATA<59>
CPU_DATA<60>
CPU_DATA<61>
CPU_DATA<62>
CPU_DATA<63>

R656 10K 5% 1/16W MF 402
R685 10K 5% 1/16W MF 402
R657 10K 5% 1/16W MF 402
R628 10K 5% 1/16W MF 402
R682 10K 5% 1/16W MF 402
R658 10K 5% 1/16W MF 402
NO STUFF R627 10K 5% 1/16W MF 402
R629 10K 5% 1/16W MF 402

- Spare
- Spare
- OBSOLETE (should remain high) 0: 0.1 16b / Reg PCI 1: 0.1 16b / 2.3 PCI
- BOOT_PCIGNT_L: 0: GPIO5; 1: PCIGNT_L
- PCI1_REQ1_L: 0: GPIO6; 1: PCIREQ1_L
- PCI1_GNT1_L: 0: GPIO7; 1: PCIGNT1_L
- FireWire Phy interface 0: Legacy interface 1: Enable interface
- Processor Bus Mode 0: 60x bus (G3); 1: 60x bus

Intrepid MaxBus

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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 8 OF 44	

SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

U51 INTREPID-REV2.1 BGA (2 OF 9) CRITICAL — OMIT

DDR_DATA_0 … DDR_DATA_63

MEM_DATA<0> AK32 … MEM_DATA<63> K35

DDR_A_0 H35 MEM_ADDR<0> … DDR_A_12 D35 MEM_ADDR<12>

DDR_BA_0 L30 MEM_BA<0>

DDR_BA_1 M29 MEM_BA<1>

DDRCS_0 AN34 MEM_CS_L<0>

DDRCS_1 AN36 MEM_CS_L<1> ‘0’ & ‘1’ GO TO SLOT A

DDRCS_2 AL35 MEM_CS_L<2> ‘2’ & ‘3’ GO TO SLOT B

DDRCS_3 AL33 MEM_CS_L<3>

DDR_DQS_0 AJ31 MEM_DQS<0> … DDR_DQS_7 L32 MEM_DQS<7>

DDR_DM_0 AJ33 MEM_DQM<0> … DDR_DM_7 L33 MEM_DQM<7>

DDRRAS L29 MEM_RAS_L

DDRCAS H32 MEM_CAS_L

DDRWE K30 MEM_WE_L

DDRCKE0 AN35 MEM_CKE<0>

DDRCKE1 AM35 MEM_CKE<1> ‘0’ & ‘1’ GO TO SLOT A

DDRCKE2 AM36 MEM_CKE<2> ‘2’ & ‘3’ GO TO SLOT B

DDRCKE3 AL36 MEM_CKE<3>

DDR_SELHI_0 AB32 MEM_MUXSEL_MSB_L_TP

DDR_SELHI_1 AE29 MEM_MUXSEL_MSB ‘0’S ARE SAME POLARITY (ACTIVE-LO)

DDR_SELLO_0 N30 MEM_MUXSEL_LSB_L_TP ‘1’S ARE SAME POLARITY (ACTIVE-HI)

DDR_SELLO_1 T32 MEM_MUXSEL_LSB

DDR_MCLK_0_P Y32 SYSCLK_DDRCLK_A0_UF

DDR_MCLK_0_N Y33 SYSCLK_DDRCLK_A0_L_UF

DDR_MCLK_1_P Y35 SYSCLK_DDRCLK_A1_UF

DDR_MCLK_1_N Y36 SYSCLK_DDRCLK_A1_L_UF

DDR_MCLK_2_P Y30 INT_DDRCLK2_P_TP

DDR_MCLK_2_N W30 INT_DDRCLK2_N_TP

DDR_MCLK_3_P W32 SYSCLK_DDRCLK_B0_UF

DDR_MCLK_3_N W33 SYSCLK_DDRCLK_B0_L_UF

DDR_MCLK_4_P V33 SYSCLK_DDRCLK_B1_UF

DDR_MCLK_4_N V32 SYSCLK_DDRCLK_B1_L_UF

DDR_MCLK_5_P W35 INT_DDRCLK5_P_TP

DDR_MCLK_5_N W36 INT_DDRCLK5_N_TP

DDR_REF AA22 INT_MEM_REF_H

DDR_VREF_0 Y22

DDR_VREF_1 T22 INT_MEM_VREF

DDR MEMORY INTERFACE

R209 1K 1% 1/16W MF 402 — MEM_VREF

+2_5V_INTREPID

R208 10K 1% 1/16W MF 402

R202 10K 1% 1/16W MF 402

C249 0.1uF 10% 16V CERM 402

INT_MEM_VREF

CLOCKS

SYSCLK_DDRCLK_A1_UF → SYSCLK_DDRCLK_A1

SYSCLK_DDRCLK_A1_L_UF → SYSCLK_DDRCLK_A1_L

SYSCLK_DDRCLK_A0_UF → SYSCLK_DDRCLK_A0

SYSCLK_DDRCLK_A0_L_UF → SYSCLK_DDRCLK_A0_L

SYSCLK_DDRCLK_B1_UF → SYSCLK_DDRCLK_B1

SYSCLK_DDRCLK_B1_L_UF → SYSCLK_DDRCLK_B1_L

SYSCLK_DDRCLK_B0_UF → SYSCLK_DDRCLK_B0

SYSCLK_DDRCLK_B0_L_UF → SYSCLK_DDRCLK_B0_L

CS

MEM_CS_L<0> → RAM_CS_L<0>

MEM_CS_L<1> → RAM_CS_L<1>

MEM_CS_L<2> → RAM_CS_L<2>

MEM_CS_L<3> → RAM_CS_L<3>

CKE

MEM_CKE<0> → RAM_CKE<0>

MEM_CKE<1> → RAM_CKE<1>

MEM_CKE<2> → RAM_CKE<2>

MEM_CKE<3> → RAM_CKE<3>

ADDR

MEM_ADDR<0> → RAM_ADDR<0>

MEM_ADDR<1> → RAM_ADDR<1>

MEM_ADDR<2> → RAM_ADDR<2>

MEM_ADDR<3> → RAM_ADDR<3>

MEM_ADDR<4> → RAM_ADDR<4>

MEM_ADDR<5> → RAM_ADDR<5>

MEM_ADDR<6> → RAM_ADDR<6>

MEM_ADDR<7> → RAM_ADDR<7>

MEM_ADDR<8> → RAM_ADDR<8>

MEM_ADDR<9> → RAM_ADDR<9>

MEM_ADDR<10> → RAM_ADDR<10>

MEM_ADDR<11> → RAM_ADDR<11>

MEM_ADDR<12> → RAM_ADDR<12>

BA

MEM_BA<0> → RAM_BA<0>

MEM_BA<1> → RAM_BA<1>

CNTL

MEM_WE_L → RAM_WE_L

MEM_CAS_L → RAM_CAS_L

MEM_RAS_L → RAM_RAS_L

1MB BOOT ROM

+3V_MAIN

C125 2.2uF 10% 10V CERM 805

C773 0.1uF 10% 10V CERM 402

C122 0.1uF 10% 10V CERM 402

U11 FEPR-1MX8 1MX8-3.3V TSOP

VPP OMIT VCC

PCI_AD<0> … PCI_AD<31>

A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20

DQ0 DQ1 DQ2 DQ3 DQ4 DQ5 DQ6 DQ7

CE OE WE WP PWD GND

ROM_CS_TP_L

R236 NO STUFF 0 5% 1/16W MF 402

R691 10K 5% 1/16W MF 402

R112 10K 5% 1/16W MF 402

R674 1K 5% 1/16W MF 402

R1 0 NO STUFF 5% 1/16W MF 402

R271 0 NO STUFF 5% 1/16W MF 402

R194 0 NO STUFF 5% 1/16W MF 402

ROM_CS_L

ROM_ONBOARD_CS_TP_L

ROM_OE_TP_L

ROM_RW_TP_L

ROM_ONBOARD_CS_L

ROM_OE_L

ROM_RW_L

ROM_WP_L

INT_RESET_L

OVERRIDE ROM MODULE INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1542	1	IC,BootRom Q16A	U11	CRITICAL	?

Weak pulldowns ensure CKEs stay low after 2.5V I/O to Intrepid shuts off.

RAM_CKE<0> RAM_CKE<1> RAM_CKE<2> RAM_CKE<3>

R247 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R257 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R260 10K 5% 1/16W MF 402 — INT_2_5V_COLD

R265 10K 5% 1/16W MF 402 — INT_2_5V_COLD

INT - DDR/BOOTROM

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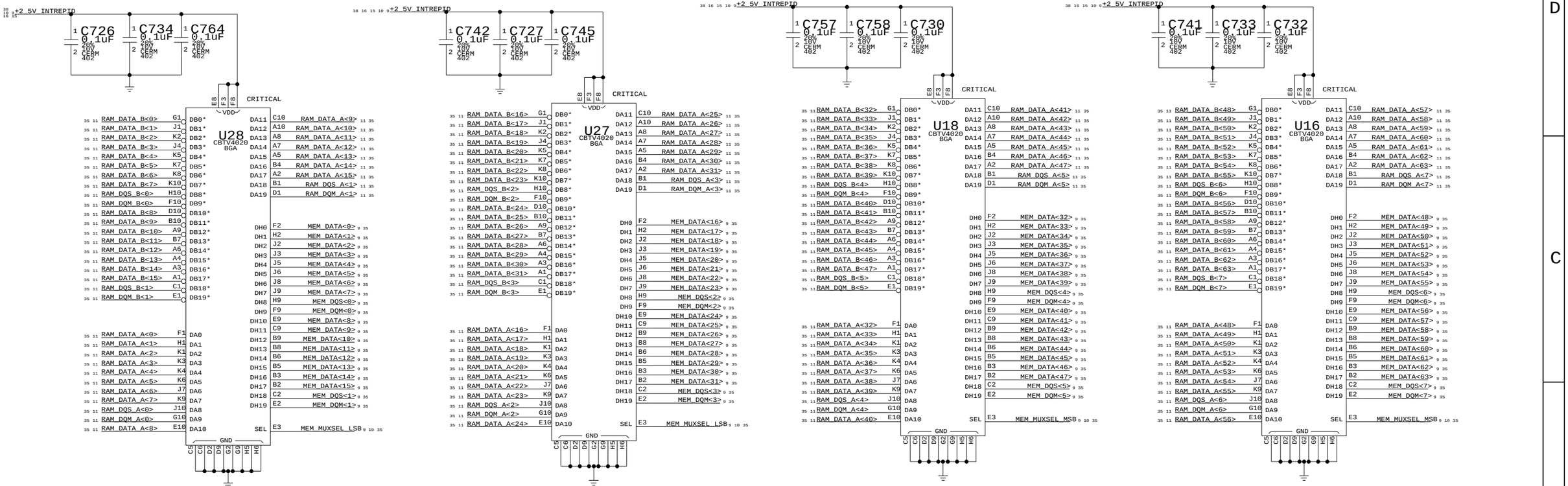
SIZE D | DRAWING NUMBER 051-6653 | REV. C

SCALE NONE | SHT 9 OF 44



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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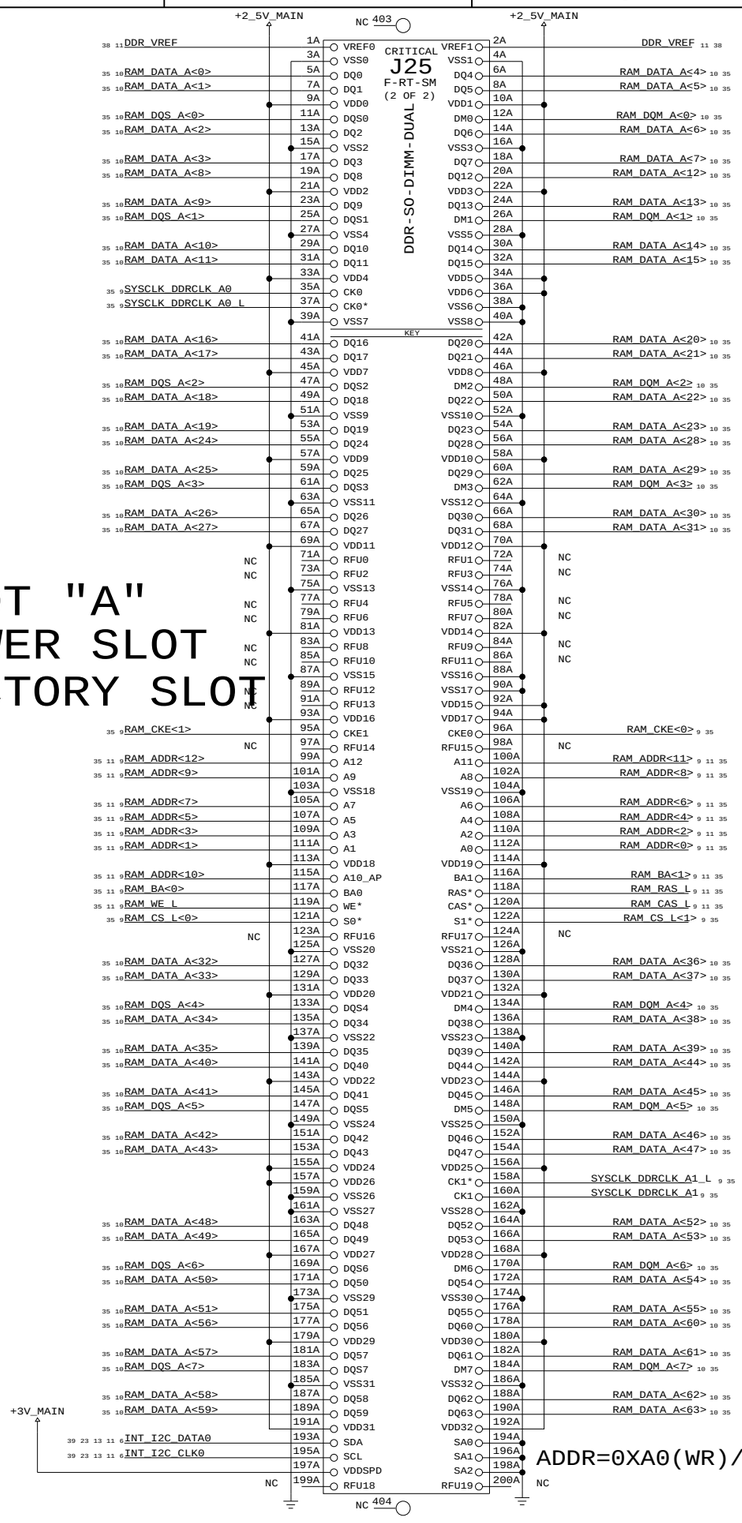
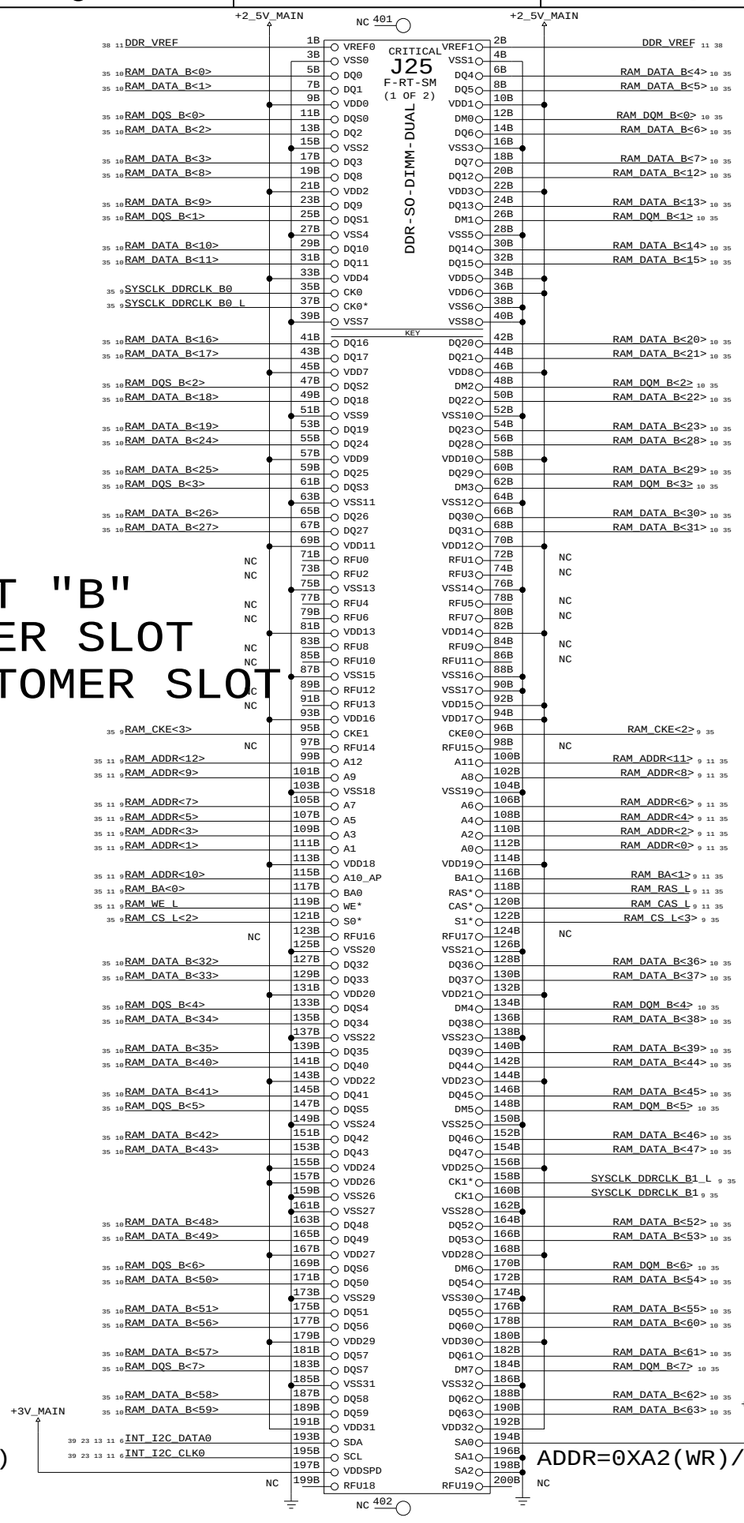
SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 10 OF 44	

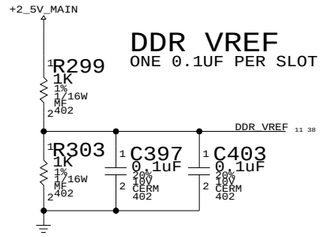


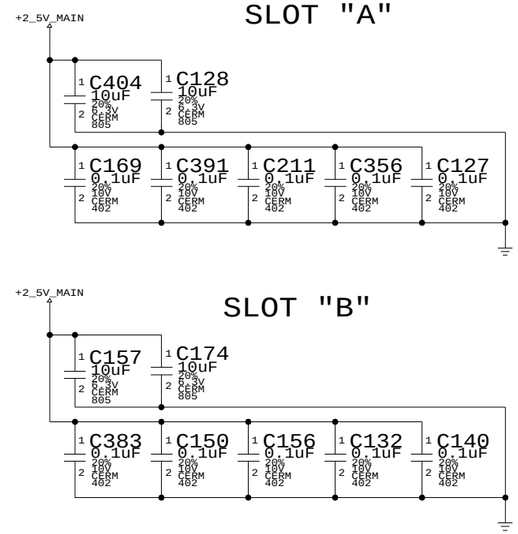
SLOT "A"
LOWER SLOT
FACTORY SLOT



SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting





DDR SODIMM CONNS

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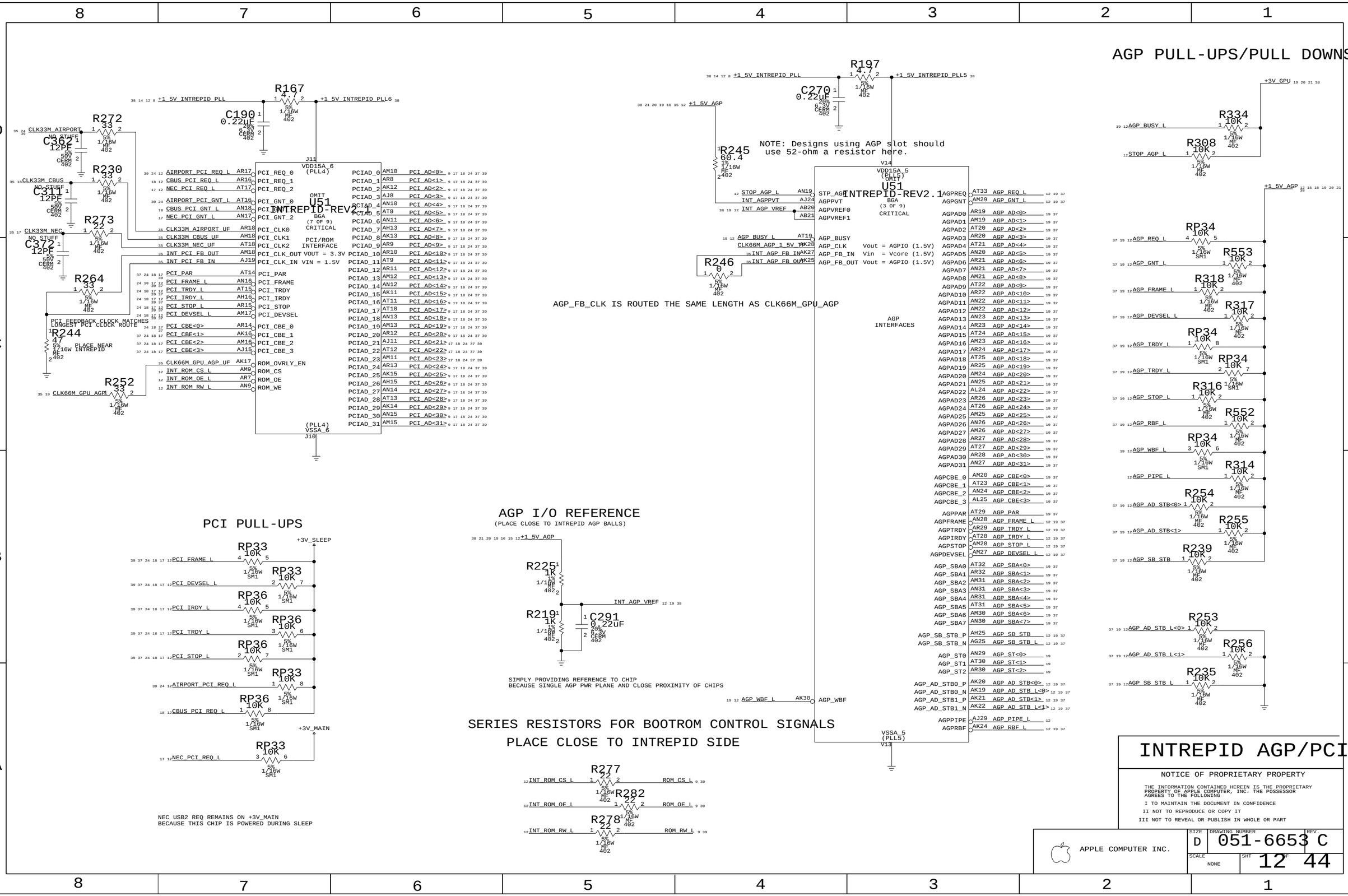
SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 11 OF 44	


R167
4.7
+1 5V INTREPID PLL
+1 5V INTREPID PLL6
C190
0.22UF
R272
33
CLK33M AIRPORT
C302
12PF
R230
33
CLK33M CBUS
C311
12PF
R273
22
CLK33M NEC
C372
12PF
R264
33
PCI FEEDBACK CLOCK MATCHES LONGEST PCI CLOCK ROUTE
R244
47
PLACE NEAR INTREPID
R252
33
CLK66M GPU AGP
J11
VDD15A_6
(PLL4)
U51
INTREPID-REV2.1
BGA
(7 OF 9)
CRITICAL
OMIT
PCI/ROM
INTERFACE
VOUT = 3.3V
VIN = 1.5V
PCI_REQ_0
PCI_REQ_1
PCI_REQ_2
PCI_GNT_0
PCI_GNT_1
PCI_GNT_2
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK_OUT
PCI_CLK_IN
PCI_PAR
PCI_FRAME
PCI_TRDY
PCI_IRDY
PCI_STOP
PCI_DEVSEL
PCI_CBE_0
PCI_CBE_1
PCI_CBE_2
PCI_CBE_3
ROM_OVRLY_EN
ROM_CS
ROM_OE
ROM_WE
PCIAD_0
PCIAD_1
PCIAD_2
PCIAD_3
PCIAD_4
PCIAD_5
PCIAD_6
PCIAD_7
PCIAD_8
PCIAD_9
PCIAD_10
PCIAD_11
PCIAD_12
PCIAD_13
PCIAD_14
PCIAD_15
PCIAD_16
PCIAD_17
PCIAD_18
PCIAD_19
PCIAD_20
PCIAD_21
PCIAD_22
PCIAD_23
PCIAD_24
PCIAD_25
PCIAD_26
PCIAD_27
PCIAD_28
PCIAD_29
PCIAD_30
PCIAD_31
(PLL4)
VSSA_6
J10
R197
4.7
+1 5V INTREPID PLL5
C270
0.22UF
+1 5V AGP
R245
60.4
NOTE: Designs using AGP slot should use 52-ohm a resistor here.
R246
0
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP
V14
VDD15A_5
(PLL5)
U51
INTREPID-REV2.1
BGA
(3 OF 9)
CRITICAL
AGP
INTERFACES
STP_AGP
AGPPVT
AGPVREF0
AGPVREF1
AGP_BUSY
AGP_CLK
AGP_FB_IN
AGP_FB_OUT
Vout = AGPIO (1.5V)
Vin = Vcore (1.5V)
Vout = AGPIO (1.5V)
INT_AGPPVT
INT_AGP_VREF
CLK66M_AGP_1_5V_VM
INT_AGP_FB_IN
INT_AGP_FB_OUT
AGPREQ
AGPGNT
AGPAD0
AGPAD1
AGPAD2
AGPAD3
AGPAD4
AGPAD5
AGPAD6
AGPAD7
AGPAD8
AGPAD9
AGPAD10
AGPAD11
AGPAD12
AGPAD13
AGPAD14
AGPAD15
AGPAD16
AGPAD17
AGPAD18
AGPAD19
AGPAD20
AGPAD21
AGPAD22
AGPAD23
AGPAD24
AGPAD25
AGPAD26
AGPAD27
AGPAD28
AGPAD29
AGPAD30
AGPAD31
AGPCBE_0
AGPCBE_1
AGPCBE_2
AGPCBE_3
AGPPAR
AGPFRAME
AGPTRDY
AGPIRDY
AGPSTOP
AGPDEVSEL
AGP_SBA0
AGP_SBA1
AGP_SBA2
AGP_SBA3
AGP_SBA4
AGP_SBA5
AGP_SBA6
AGP_SBA7
AGP_SB_STB_P
AGP_SB_STB_N
AGP_ST0
AGP_ST1
AGP_ST2
AGP_AD_STB0_P
AGP_AD_STB0_N
AGP_AD_STB1_P
AGP_AD_STB1_N
AGPPIPE
AGPRBF
AGP_WBF
VSSA_5
(PLL5)
V13
AGP PULL-UPS/PULL DOWNS
+3V_GPU
R334
10K
R308
10K
+1 5V AGP
RP34
10K
R553
10K
R318
10K
R317
10K
RP34
10K
RP34
10K
R316
10K
R552
10K
RP34
10K
R314
10K
R254
10K
R255
10K
R239
10K
R253
10K
R256
10K
R235
10K
PCI PULL-UPS
+3V_SLEEP
RP33
10K
RP33
10K
RP36
10K
RP36
10K
RP36
10K
RP33
10K
RP36
10K
+3V_MAIN
RP33
10K
NEC USB2 REQ REMAINS ON +3V_MAIN
BECAUSE THIS CHIP IS POWERED DURING SLEEP
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)
+1 5V AGP
R225
1K
R219
1K
C291
0.22uF
INT_AGP_VREF
SIMPLY PROVIDING REFERENCE TO CHIP
BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE
R277
22
R282
22
R278
22
INT_ROM_CS_L
INT_ROM_OE_L
INT_ROM_RW_L
ROM_CS_L
ROM_OE_L
ROM_RW_L
INTREPID AGP/PCI
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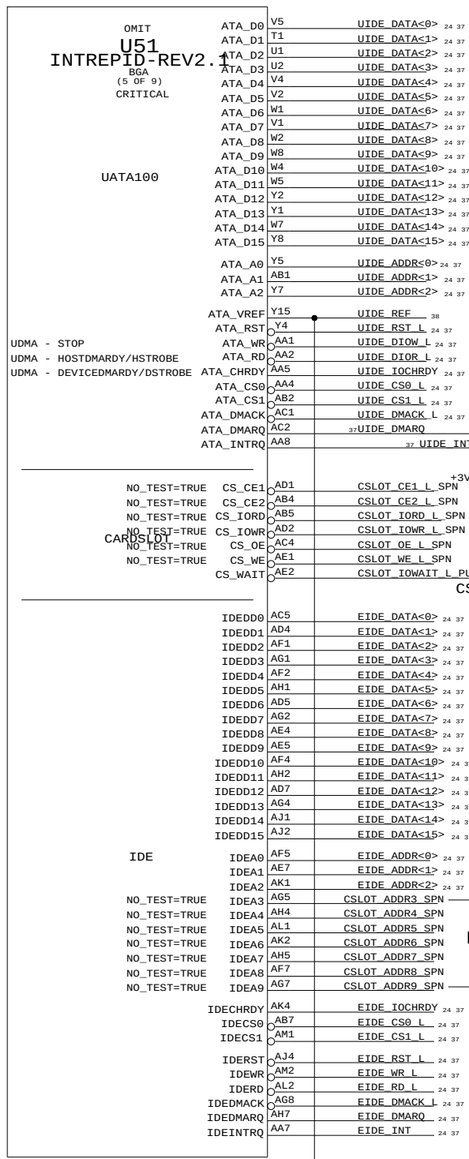
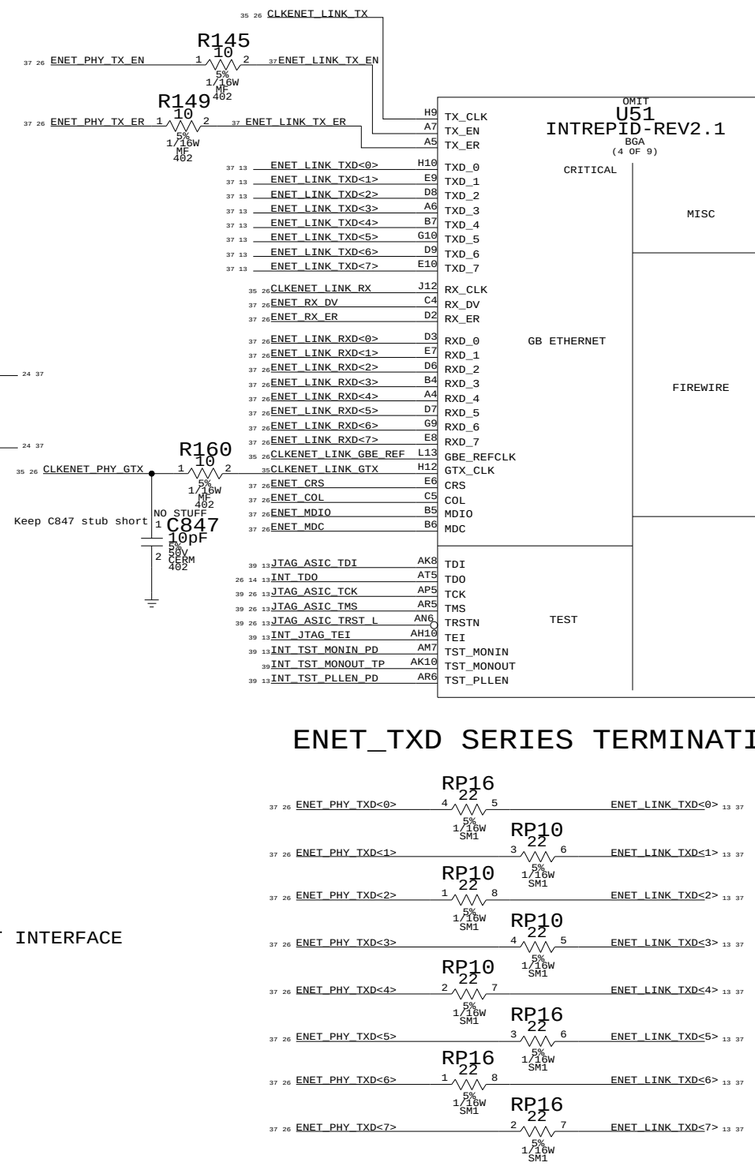
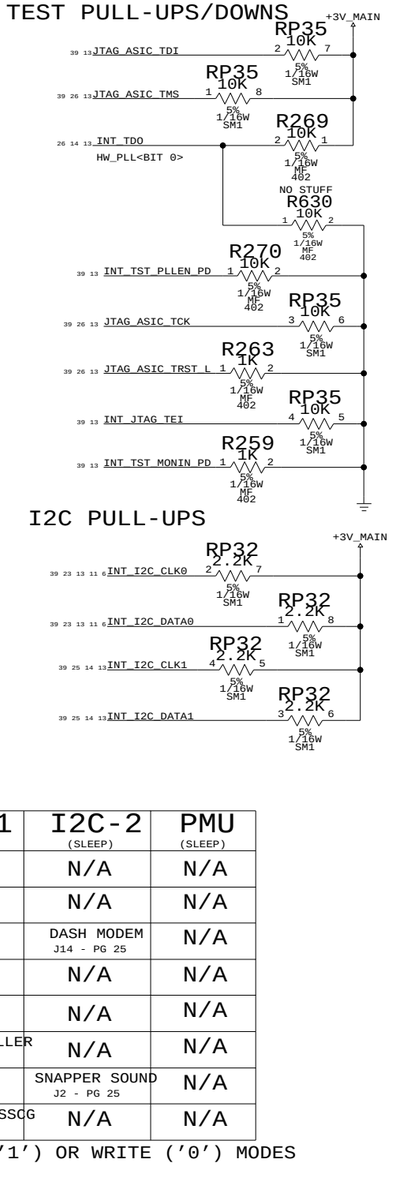
SIZE D
DRAWING NUMBER 051-6653
REV. C
SCALE NONE
SHT 12 OF 44







ENET_TXD SERIES TERMINATION

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - LOWER J25 - PG 11	N/A	N/A	N/A
A2-WR A3-RD	RAM - UPPER J25 - PG 11	N/A	N/A	N/A
AC-WR AD-WR	N/A	N/A	DASH MODEM J14 - PG 25	N/A
AE-WR AF-RD	BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A
84-WR 85-RD	LMU J3000 - PG 23 (LMU on RUX Brd.)	N/A	N/A	N/A
5C-WR 5D-RD	N/A	FAN CONTROLLER U52 - PG 25	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J2 - PG 25	N/A
D2-WR D3-RD	N/A	CLOCK SLEW SSCG U30 - PG 14	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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SCALE: NONE		SHT: 13 44

USB PORT ASSIGNMENTS

PORT A - PORT D/UNUSED

R181 10K — USB_DAM
R183 10K — USB_DAP
R156 10K — USB_DBM
R157 10K — USB_DBP
R164 10K — USB_DCM
R165 10K — USB_DCP
R182 10K — USB_DDM
R180 10K — USB_DDP

PORT E/BLUETOOTH

R174 22 — USB_DEP ↔ BT_USB_DP
R179 22 — USB_DEM ↔ BT_USB_DM
R178 15K
R175 15K

PORT F/MODEM

R192 22 — USB_DFP ↔ MODEM_USB_DP
R188 22 — USB_DFM ↔ MODEM_USB_DM
R189 15K
R193 15K

INT - USB/GPIOS/I2S

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PCI INTERRUPTS

R148 10K — CBUS_INT_L
R746 10K — AIRPORT_PCI_INT_L
R158 10K — NEC_PCI_INT_L

GPIO/EXTINT PULLUPS

R187 10K — USB_PWREN_EF_L
R191 10K — USB_OC_EF_L
RP11 10K — USB_OC_AB_L
RP11 10K — USB_PWREN_CD_L
RP8 10K — USB_PWREN_AB_L
RP11 10K — USB_OC_CD_L
RP8 10K — INT_EXTINT14_PU
RP5 10K — INT_EXTINT8_PU
RP6 10K — COMM_RING_DET_L
RP11 10K — INT_GPIO15_PU
RP6 10K — PMU_INT_NMI
RP6 10K — PMU_INT_L
R250 10K — PMU_REQ_L
RP7 10K — INT_GPIO12_PU
RP7 10K — INT_EXTINT13_PU
RP4 10K — INT_EXTINT16_PU
RP5 10K — INT_EXTINT11_PU
RP6 10K — INT_EXTINT10_PU
RP4 10K — INT_EXTINT12_PU
RP8 10K — INT_GPIO9_PU
RP8 10K — INT_GPIO1_PU
R153 10K — INT_EXTINT3_PU
RP15 10K — INT_MOD_DTO_UF
RP15 10K — INT_MOD_CLKOUT_UF
RP15 10K — INT_MOD_DTI
RP15 10K — INT_MOD_SYNC_UF
R206 10K — INT_MOD_BITCLK_UF
R166 100K — SND_HW_RESET_L

U49 LT1962-ADJ MSOP — IN, NC, NC, SHDN, OUT, ADJ, BYP, GND
C721 1uF — LTC1962_INT_VIN
C392 0.01uF — LT1962_INT_ADJ
R574 18.7K — +1_5V_INTREPID_PLL
C723 10uF — -> 1.55V OUTPUT
R567 68.1K — LT1962_INT_BYP

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
359S0086	1	IC,CY28512-2	U31	CRITICAL	SSCG

U31 CY28512D TSSOP (OMIT) — CRITICAL
INTERNAL 250K PULL-UP
OUTPUT IMPEDANCE ~18-20 OHMS

CLKIN ← CG_FSEL
FSEL ← CG_FSEL
SCLK ← INT_I2C_CLK1
SDATA ← INT_I2C_DATA1
ADDRSEL ← CG_ADDRSEL (INTERNAL 250K PULL-DOWN)
RESET* ← CG_RESET_L
PD* ← CG_SYSCLK_EN
LOCK ← CG_LOCK (OPEN DRAIN OUTPUT)
ODSEL (INTERNAL 250K PULL-UP)
CPU0 → CG_CLKOUT1 → INT_REF_CLK_IN
VDD0 VDD1 VDDA VDDC VDDQ
VSS0 VSS1 VSSA VSSC VSSQ

R284 0 — VCORE_VGATE
R296 10K
R142 0 — VCORE_VGATE
R293 33 — INT_REF_CLK_IN
R292 75 — PLACE NEAR INTREPID TO MINIMIZE OVERSHOOT

R286 0 — NO STUFF
R287 10K — MAIN_RESET_L
R288 10K
R295 10K — NO STUFF

L15 400-OHM-EMI SM-1 — +3V_MAIN
L14 400-OHM-EMI SM-1 — +2_5V_MAIN
C400 0.1uF — +3V_CG_PLL_MAIN
C402 1uF
C399 0.1uF
C394 0.1uF — +2_5V_CG_MAIN

R450 0 — CG_FSEL
R467 0 — NO STUFF — SYSTEM_CLK_EN
R457 0 — INT_TDO
R134 0 — NO STUFF — CLK18M_INT_EXT
R113 51 — NO STUFF
R144 10M — NO STUFF — CLK18M_INT_XOUT
R143 0
Y2 18.432M — 8X4.5MM-SM — CLK18M_XTAL_IN
C152 22pF
C151 22pF
CRYSTAL LOAD CAPACITANCE IS 16PF
R218 0 — INT_REF_CLK_OUT
J9 U.FL-R_SMT F-ST-SM

HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y2	Alt. for Siward Part

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES	RES-0402-V2	RESISTOR	10K		1/16W	5%	R292	NO_SSCG

R240 4 — +1_5V_INTREPID_PLL8
R280 4.7 — +1_5V_INTREPID_PLL4
R279 4.7 — +1_5V_INTREPID_PLL3
R243 4 — +1_5V_INTREPID_PLL2
R201 4.7 — +1_5V_INTREPID_PLL1
C337 0.22uF
C389 0.22uF
C388 0.22uF
C386 0.22uF
C387 0.22uF

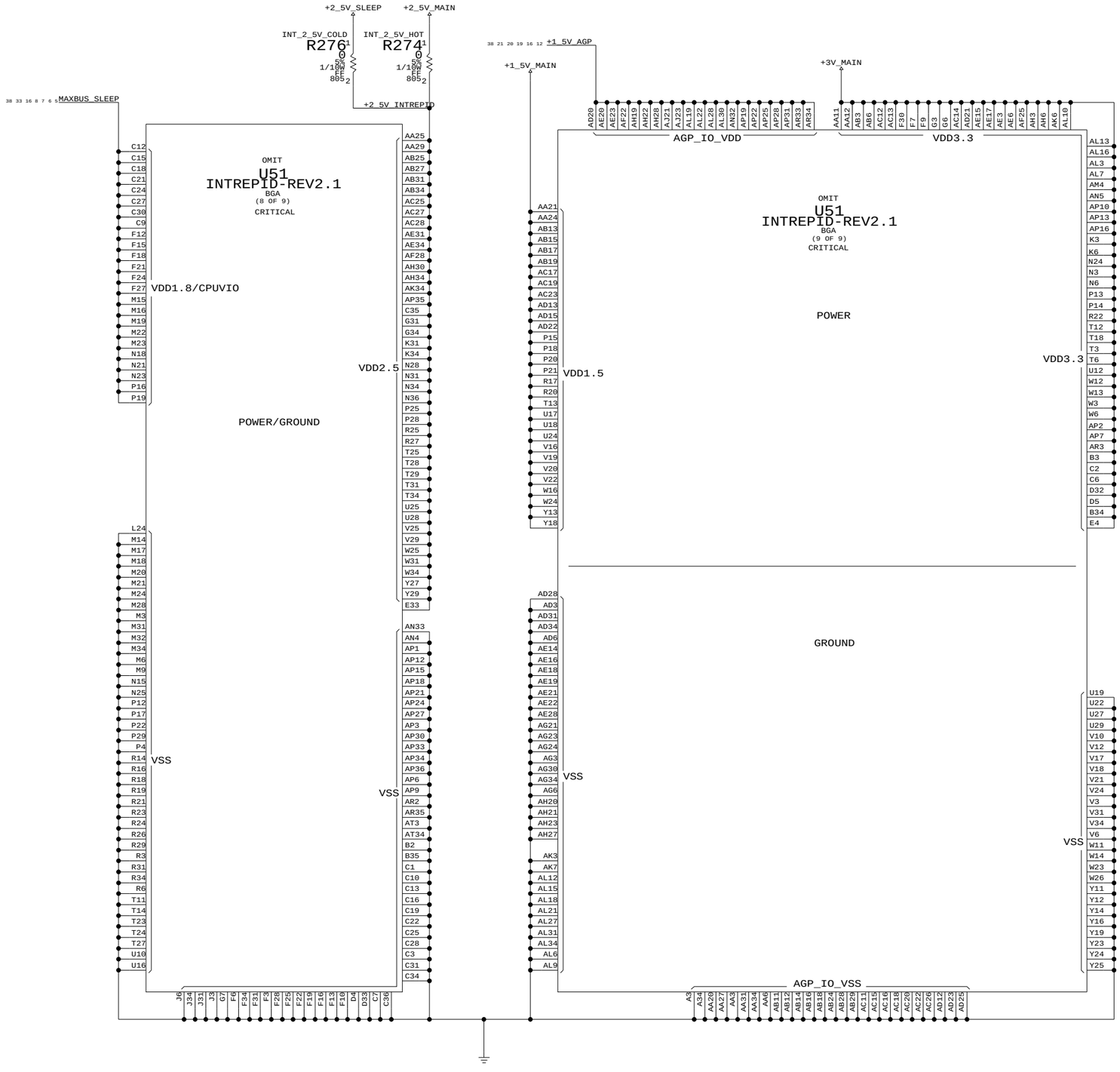
L13 FERR-EMI-100-OHM SM — +3V_MAIN
+3V_INTREPID_USB
C235 0.01uF
C246 0.1uF
C256 10uF

U51 INTREPID-REV2.1 BGA CRITICAL (6 OF 9) — OMIT

GPIO0 GPIO1 GPIO2 GPIO3 GPIO4 GPIO5 GPIO6 GPIO9 GPIO11 GPIO12 GPIO15 GPIO16 — VCORE A/B SEL, GENERAL PURPOSE I/O'S
EXTINT0 EXTINT1 EXTINT2 EXTINT3 EXTINT4 EXTINT5 EXTINT6 EXTINT7 EXTINT8 EXTINT9 EXTINT10 EXTINT11 EXTINT12 EXTINT13 EXTINT14 EXTINT15 EXTINT16 EXTINT17 — INTERRUPTS
POWERBOOK SPARE
CBUS_REG_L
CBUS_IREQ_L
PCIPME PROCSLEEPREQ PENDPROCINT — PCI
XTAL_IN XTAL_OUT STOPXTAL WATCHDOG BUF_REF_CLK_OUT SS_REF_CLK_IN — CLOCKS
SCCTXDA SCCRTSA SCCDTRA SCCRXDA SCCGPIOA SCCTRXCA — VIA
SCCTXDB SCCRTSB SCCRXDB SCCGPIOB SCCTRXCB — MISO REQ* MOSI ACK* SCK
USB_VD0_P USB_VD0_N USB_VD1_P USB_VD1_N USB_PRTPWR0 USB_PWRFLT0 USB_VD2_P USB_VD2_N USB_VD3_P USB_VD3_N USB_PRTPWR1 USB_PWRFLT1 USB_VD4_P USB_VD4_N USB_VD5_P USB_VD5_N USB_PRTPWR2 USB_PWRFLT2 — USB
AUD_DTO AUD_DTI AUD_SYNC AUD_BITCLK AUD_CLKOUT — AUDIO/I2S (SIGNAL FROM MODEM)
MOD_DTO MOD_DTI MOD_SYNC MOD_BITCLK MOD_CLKOUT
IICCLK_2 IICDATA_2 — IIC
VSSA1 VSSA2 VSSA3 VSSA4 VSSA_8 VSSU_1 VSSU_2

RP13 47 — INT_I2S0_SND_TO_DAC
RP13 47 — INT_I2S0_SND_LRCLK
RP13 47 — INT_I2S0_SND_SCLK
RP13 47 — INT_I2S0_SND_MCLK
RP47 0K — SOFT_MODEM — INT_MOD_DTO
RP47 0K — SOFT_MODEM — INT_MOD_SYNC
RP47 0K — SOFT_MODEM — INT_MOD_BITCLK
RP47 0K — SOFT_MODEM — INT_MOD_CLKOUT

+3V_SLEEP
R258 1K
R241 1K
INT_I2C_CLK2
INT_I2C_DATA2



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974 BGA,FAST	U51	CRITICAL	?

Intrepid Power

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INTREPID MAXBUS DECOUPLING

24 Balls
4 X 10UF (0805)
28 X 0.22UF (0402)

MAXBUS_SLEEP

C148 10uF, C142 10uF, C182 0.22uF, C178 0.22uF, C141 0.22uF, C145 0.22uF, C214 0.22uF, C163 0.22uF, C164 0.22uF, C225 0.22uF, C160 0.22uF, C159 0.22uF
C144 10uF, C146 10uF, C204 0.22uF, C166 0.22uF, C205 0.22uF, C223 0.22uF, C229 0.22uF, C181 0.22uF, C207 0.22uF, C208 0.22uF, C183 0.22uF, C180 0.22uF
C165 0.22uF, C206 0.22uF, C147 0.22uF, C149 0.22uF, C179 0.22uF, C162 0.22uF, C161 0.22uF, C213 0.22uF

All 10uF: 20% 6.3V CERM 805. All 0.22uF: 20% 6.3V CERM 402.

INTREPID CORE DECOUPLING

30 Balls
4 X 10UF (0805)
29 X 0.22UF (0402)

+1_5V_MAIN

C324 10uF, C325 10uF, C299 0.22uF, C279 0.22uF, C262 0.22uF, C292 0.22uF, C248 0.22uF, C302 0.22uF, C300 0.22uF, C290 0.22uF, C272 0.22uF, C259 0.22uF
C201 10uF, C200 10uF, C301 0.22uF, C278 0.22uF, C226 0.22uF, C238 0.22uF, C250 0.22uF, C263 0.22uF, C224 0.22uF, C222 0.22uF, C261 0.22uF, C227 0.22uF
C271 0.22uF, C310 0.22uF, C288 0.22uF, C260 0.22uF, C303 0.22uF, C287 0.22uF, C258 0.22uF, C236 0.22uF, C289 0.22uF

All 10uF: 20% 6.3V CERM 805. All 0.22uF: 20% 6.3V CERM 402.

INTREPID AGP I/O DECOUPLING

21 Balls
4 X 10UF (0805)
21 X 0.22UF (0402)

+1_5V_AGP

C381 10uF, C380 10uF, C367 0.22uF, C319 0.22uF, C330 0.22uF, C363 0.22uF, C366 0.22uF, C332 0.22uF, C361 0.22uF, C320 0.22uF, C328 0.22uF, C364 0.22uF
C382 10uF, C379 10uF, C365 0.22uF, C329 0.22uF, C345 0.22uF, C346 0.22uF, C373 0.22uF, C344 0.22uF, C331 0.22uF, C312 0.22uF, C354 0.22uF, C347 0.22uF
C321 0.22uF

All 10uF: 20% 6.3V CERM 805. All 0.22uF: 20% 6.3V CERM 402.

INTREPID 3.3V DECOUPLING

57 Balls
4 X 10UF (0805)
40 X 0.22UF (0402)

+3V_MAIN

C378 10uF, C376 10uF, C170 0.22uF, C358 0.22uF, C268 0.22uF, C327 0.22uF, C342 0.22uF, C215 0.22uF, C352 0.22uF, C171 0.22uF, C158 0.22uF, C309 0.22uF
C377 10uF, C375 10uF, C175 0.22uF, C357 0.22uF, C351 0.22uF, C350 0.22uF, C286 0.22uF, C176 0.22uF, C189 0.22uF, C167 0.22uF, C371 0.22uF, C359 0.22uF
C285 0.22uF, C283 0.22uF, C269 0.22uF, C221 0.22uF, C234 0.22uF, C247 0.22uF, C257 0.22uF, C343 0.22uF, C313 0.22uF, C228 0.22uF
C360 0.22uF, C308 0.22uF, C318 0.22uF, C237 0.22uF, C317 0.22uF, C341 0.22uF, C177 0.22uF, C212 0.22uF, C349 0.22uF, C184 0.22uF

All 10uF: 20% 6.3V CERM 805. All 0.22uF: 20% 6.3V CERM 402.

INTREPID DDR DECOUPLING

44 Balls
4 X 10UF (0805)
46 X 0.22UF (0402)

+2_5V_INTREPID

C314 10uF, C322 10uF, C304 0.22uF, C266 0.22uF, C172 0.22uF, C281 0.22uF, C243 0.22uF, C253 0.22uF, C334 0.22uF, C241 0.22uF, C348 0.22uF, C192 0.22uF
C191 10uF, C202 10uF, C306 0.22uF, C252 0.22uF, C275 0.22uF, C297 0.22uF, C240 0.22uF, C218 0.22uF, C274 0.22uF, C369 0.22uF, C368 0.22uF, C168 0.22uF
C265 0.22uF, C251 0.22uF, C216 0.22uF, C254 0.22uF, C305 0.22uF, C186 0.22uF, C219 0.22uF, C315 0.22uF, C264 0.22uF, C294 0.22uF
C323 0.22uF, C273 0.22uF, C242 0.22uF, C203 0.22uF, C333 0.22uF, C217 0.22uF, C230 0.22uF, C293 0.22uF, C231 0.22uF, C296 0.22uF
C239 0.22uF, C316 0.22uF, C185 0.22uF, C282 0.22uF, C295 0.22uF, C280 0.22uF

All 10uF: 20% 6.3V CERM 805. All 0.22uF: 20% 6.3V CERM 402.

INTREPID/MAIN 2.5V DECOUPLING

10 X 0.22UF (0402)

+2_5V_MAIN

C770 0.22uF, C139 0.22uF, C335 0.22uF, C735 0.22uF, C245 0.22uF, C736 0.22uF, C739 0.22uF, C395 0.22uF, C374 0.22uF, C385 0.22uF

All 0.22uF: 20% 6.3V CERM 402.

Place these 2.5V Decoupling Caps near the Edge of +2.5V_MAIN and +2.5V_INTREPID split

Intrepid Decoupling

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 16 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part

+3V_NEC_VDD 17 38

C749 0.1uF 20% 10V CERM 402
C746 0.1uF 20% 10V CERM 402
C761 0.1uF 20% 10V CERM 402
C750 0.1uF 20% 10V CERM 402
C756 0.1uF 20% 10V CERM 402
C748 0.1uF 20% 10V CERM 402
C769 0.1uF 20% 10V CERM 402
C752 0.1uF 20% 10V CERM 402
C747 0.1uF 20% 10V CERM 402
C197 10uF 20% 6.3V CERM 805
C765 0.1uF 20% 10V CERM 402
C768 0.1uF 20% 10V CERM 402

+3V_MAIN

L7 FERR-EMI-100-OHM SM

R172 0 5% 1/16W MF 603

C760 0.1uF 20% 10V CERM 402
C751 0.1uF 20% 10V CERM 402
C173 10uF 20% 6.3V CERM 805

38 NEC_AVDD

38 17 +3V_NEC_VDD

Y1's LOAD CAPACITANCE = 16 pF

CRITICAL
Y1 30.0000M
8X4.5MM-SM
NEC_XT2_R

C759 27pF 5% 50V CERM 402
C136 27pF 5% 50V CERM 402
R124 100 5% 1/16W MF 402

R613 43.2 1% 1/16W MF 402 — NEC_USB_DAM 25 37 39
R612 43.2 1% 1/16W MF 402 — NEC_USB_DAP 25 37 39

Low/Full/High Speed (External)

R609 43.2 1% 1/16W MF 402 — NEC_USB_DBM 25 37 39
R610 43.2 1% 1/16W MF 402 — NEC_USB_DBP 25 37 39

Low/Full/High Speed (External)

CRITICAL
U17
NEC_uPD720101_USB2
FBGA

H3 M4 C8 P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
VDD_PCI
N10 N12 — AVDD

39 37 24 18 12 9 PCI_AD<0>	M5	AD0	
39 37 24 18 12 9 PCI_AD<1>	P5	AD1	
39 37 24 18 12 9 PCI_AD<2>	N5	AD2	
39 37 24 18 12 9 PCI_AD<3>	P4	AD3	
39 37 24 18 12 9 PCI_AD<4>	N4	AD4	
39 37 24 18 12 9 PCI_AD<5>	M3	AD5	
39 37 24 18 12 9 PCI_AD<6>	N3	AD6	
39 37 24 18 12 9 PCI_AD<7>	M1	AD7	
39 37 24 18 12 9 PCI_AD<8>	L2	AD8	
39 37 24 18 12 9 PCI_AD<9>	L1	AD9	
39 37 24 18 12 9 PCI_AD<10>	K2	AD10	
39 37 24 18 12 9 PCI_AD<11>	L3	AD11	
39 37 24 18 12 9 PCI_AD<12>	K1	AD12	
39 37 24 18 12 9 PCI_AD<13>	K3	AD13	
39 37 24 18 12 9 PCI_AD<14>	J2	AD14	
39 37 24 18 12 9 PCI_AD<15>	J1	AD15	
39 37 24 18 12 9 PCI_AD<16>	F2	AD16	
39 37 24 18 12 9 PCI_AD<17>	E3	AD17	
39 37 24 18 12 9 PCI_AD<18>	E1	AD18	
39 37 24 18 12 9 PCI_AD<19>	D3	AD19	
39 37 24 18 12 9 PCI_AD<20>	D1	AD20	
39 37 24 18 12 PCI_AD<21>	D2	AD21	
39 37 24 18 12 PCI_AD<22>	C2	AD22	
39 37 24 18 12 PCI_AD<23>	C1	AD23	
39 37 24 18 12 9 PCI_AD<24>	B4	AD24	
39 37 24 18 12 9 PCI_AD<25>	A4	AD25	
39 37 24 18 12 9 PCI_AD<26>	B5	AD26	
(PCI_AD<27>)	C4	AD27	
39 37 24 18 12 9 PCI_AD<28>	A5	AD28	
39 37 24 18 12 9 PCI_AD<29>	C5	AD29	
39 37 24 18 12 9 PCI_AD<30>	B6	AD30	
39 37 24 18 12 9 PCI_AD<31>	A6	AD31	
37 24 18 12 PCI_CBE<0>	M2	CBE0	
37 24 18 12 PCI_CBE<1>	J3	CBE1	
37 24 18 12 PCI_CBE<2>	F1	CBE2	
37 24 18 12 PCI_CBE<3>	C3	CBE3	
39 37 24 18 12 PCI_PAR	J4	PAR	
39 37 24 18 12 PCI_FRAME_L	F3	FRAME	
39 37 24 18 12 PCI_IRDY_L	F4	IRDY	
39 37 24 18 12 PCI_TRDY_L	G1	TRDY	
39 37 24 18 12 PCI_STOP_L	G3	STOP	
NEC_IDSEL	B3	IDSEL	
39 37 24 18 12 PCI_DEVSEL_L	G2	DEVSEL	
12 NEC_PCI_REQ_L	C6	REQ	
12 NEC_PCI_GNT_L	D6	GNT	
18 PCI_PERR_L	H2	PERR	
18 PCI_SERR_L	H1	SERR	
NEC_PCI_INTA_L	C7	INTA	
NEC_PCI_INTB_L	B7	INTB	
NEC_PCI_INTC_L	A7	INTC	
35 12 CLK33M_NEC	A8	PCLK	
17 NEC_IO_RESET_L	B8	VBBRST	
NEC_CRUN_L	N6	CRUN	
17 NEC_PME_L	D9	PME	
17 NEC_MAIN_RESET_L	C9	VCCRST	
NEC_SMI_L_TP	L6	SMI	
17 NEC_LEGC	L7	LEGC	

XT1/SCLK	L9	NEC_XT1	
XT2	P8	NEC_XT2	
RSDM1	M14	NEC_USB_RSDM1	
DM1	M13	(NEC_USB_DAM)	
DP1	L14	(NEC_USB_DAP)	
RSDP1	K13	NEC_USB_RSDP1	
RSDM2	K14	NEC_USB_RSDM2	
DM2	K12	(NEC_USB_DBM)	
DP2	J14	(NEC_USB_DBP)	
RSDP2	J12	NEC_USB_RSDP2	
RSDM3	H11	NC	
DM3	G11		
DP3	G13		
RSDP3	G14	NC	
RSDM4	F12	NC	
DM4	F14		
DP4	E12		
RSDP4	E14	NC	
RSDM5	E13	NC	
DM5	D14		
DP5	C13		
RSDP5	C14	NC	
RREF	P11	NEC_RREF	
OCI1	B12	NEC_LUSB_OCI 17	
OCI2	B11	NEC_RUSB_OCI 17	
OCI3	B10	NEC_OCI<3>	
OCI4	A10	NEC_OCI<4>	
OCI5	B9	NEC_OCI<5>	
PPON1	C12 OUT	NEC_LUSB_PPON 25 39	
PPON2	A11 OUT	NEC_RUSB_PPON 25 39	
PPON3	C11 OUT	NEC_PPON3_TP	
PPON4	C10 OUT	NEC_PPON4_TP	
PPON5	A9 OUT	NEC_PPON5_TP	
NC1	P6	NEC_NC<1>	
NC2	M6	NEC_NC<2>	
NTEST1	M8 IPD	NC	
SMC	M7 IPD	NC	
TEB	N7 IPD	NC	
AMC	P7 IPD	NEC_AMC_TP	
TEST	L8 IPD	NC	
NANDTEST	M10	NEC_NANDTESTEN_TP	
SRCLK	M9	NC	
SRDTA	N9	NEC_NANDTESTOUT_TP	
SRMOD	P9 IPD	NC	
AVSS			

R614 9.09K 1% 1/16W MF 402 — Tie to GND (NEC_AVSS_F) at ball N11
NEC_AVSS_F 17

+3V_NEC_VDD 17 38

RP43 10K 5% 1/16W SM1 (3-6)
RP43 10K 5% 1/16W SM1 (4-5)
R606 10K 5% 1/16W MF 402
R615 1K 5% 1/16W MF 402
R632 1K 5% 1/16W MF 402

NEC documentation indicates that NCs must be tied high.

VSS

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8 — AVSS(R)
N11 P13 M12 — AVSS

R798 0 5% 1/16W MF 603 — 17 NEC_AVSS_F

R636 22 5% 1/16W MF 402 — PCI_AD<27>

RP45 47 5% 1/16W SM1
Series Rpaks required to facilitate NAND-tree testing
14 NEC_PCI_INT_L

R617 4.7K 5% 1/16W MF 402

RP44 47 5% 1/16W SM1

29 26 23 IO_RESET_L	1	8	NEC_IO_RESET_L 17
39 29 24 14 PMU_PME_L	2	7	NEC_PME_L 17
39 29 24 19 18 14 MAIN_RESET_L	3	6	NEC_MAIN_RESET_L 17
17 NEC_LEGC	4	5	

+3V_MAIN

RP43 10K 5% 1/16W SM1 (7-2)
RP43 10K 5% 1/16W SM1 (8-1)
R607 0 5% 1/16W MF 402 — 17 NEC_LUSB_OCI — NEC_LUSB_OCI_UF 25 39
R608 0 5% 1/16W MF 402 — 17 NEC_RUSB_OCI — NEC_RUSB_OCI_UF 25 39

NO STUFF C743 0.1uF 20% 10V CERM 402
NO STUFF C744 0.1uF 20% 10V CERM 402

USB 2.0

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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 17 OF 44	

PCI1510 PULL-UPS

+3V_SLEEP_PCCARD

R718 10K 5% 1/16W MF 402 — PCI_PERR_L (17 18)

R714 10K 5% 1/16W MF 402 — PCI_SERR_L (17 18)

R722 10K 5% 1/16W MF 402 — CBUS_SUSPEND_PU (18)

+2_5V_SLEEP

C787 4.7uF 20% 6.3V CERM 805

C786 0.22uF 20% 6.3V CERM 402

+3V_SLEEP

R756 0 5% 1/16W MF 603

+3V_SLEEP_PCCARD (39)

C60 10uF 20% 6.3V CERM 805

C776 10uF 20% 6.3V CERM 805

C789 0.22uF 20% 6.3V CERM 402

C791 0.22uF 20% 6.3V CERM 402

C784 0.22uF 20% 6.3V CERM 402

C782 0.22uF 20% 6.3V CERM 402

C783 0.22uF 20% 6.3V CERM 402

C778 0.22uF 20% 6.3V CERM 402

C775 0.22uF 20% 6.3V CERM 402

R721 10K 5% 1/16W MF 402

A7 C13 D5 E1 M1 N7 N11 — VCC

PCI1510 VR_EN_L (D4 L8)

U8 PCI1510GGU BGA

NC	H10	CLK_48_RSVD/NC
	D4	VR_EN*
	L8	VR_PORT
PCI_AD<0> (39 37 24 17 12 9)	N8	AD0
PCI_AD<1>	M7	AD1
PCI_AD<2>	L7	AD2
PCI_AD<3>	N6	AD3
PCI_AD<4>	K4	AD4
PCI_AD<5>	M6	AD5
PCI_AD<6>	L6	AD6
PCI_AD<7>	N5	AD7
PCI_AD<8>	N4	AD8
PCI_AD<9>	M2	AD9
PCI_AD<10>	M5	AD10
PCI_AD<11>	L4	AD11
PCI_AD<12>	N3	AD12
PCI_AD<13>	K5	AD13
PCI_AD<14>	L5	AD14
PCI_AD<15>	M4	AD15
PCI_AD<16>	J4	AD16
PCI_AD<17>	H1	AD17
PCI_AD<18>	H3	AD18
(PCI_AD<19>)	H2	AD19
PCI_AD<20>	G2	AD20
PCI_AD<21>	G4	AD21
PCI_AD<22>	F1	AD22
PCI_AD<23>	C3	AD23
PCI_AD<24>	F3	AD24
PCI_AD<25>	E2	AD25
PCI_AD<26>	F4	AD26
PCI_AD<27>	B1	AD27
PCI_AD<28>	D2	AD28
PCI_AD<29>	E4	AD29
PCI_AD<30>	D3	AD30
PCI_AD<31>	E3	AD31
PCI_CBE<0>	K6	C/BE0*
PCI_CBE<1>	M3	C/BE1*
PCI_CBE<2>	J2	C/BE2*
PCI_CBE<3>	A1	C/BE3*
PCI_PAR	N1	PAR
PCI_IRDY_L	K1	IRDY
PCI_SERR_L (18)	L2	SERR
CBUS_PCI_IDSEL	F2	IDSEL
PCI_PERR_L (18)	K3	PERR
PCI_FRAME_L	J1	FRAME
PCI_STOP_L	L1	STOP
PCI_TRDY_L	J3	TRDY
PCI_DEVSEL_L	K2	DEVSEL
CBUS_PCI_RESET_L	G3	PRST
CBUS_PCI_REQ_L (12)	C2	REQ
CBUS_PCI_GNT_L (12)	C1	GNT
CLK33M_CBUS (35 12)	G1	PCLK
NC	M9	SPKROUT
NC	M8	RI_OUT/PME
CBUS_SUSPEND_PU (18)	N10	SUSPEND
CBUS_INT_L (14)	K7	MFUNC0
CBUS_MFUNC1_PD (18)	N9	MFUNC1
CBUS_MFUNC2_PD (18)	L9	MFUNC2
CBUS_MFUNC3_PD (18)	K10	MFUNC3
CBUS_MFUNC4_PD (18)	M10	MFUNC4
CBUS_MFUNC5_PD (18)	N12	MFUNC5
CBUS_MFUNC6_PD (18)	L10	MFUNC6
	L11	GRST

CRITICAL — CLAMP FOR PC-CARD, CLAMP FOR PCI

	B11	VCCCB
	L3	VCCP
CBUS_VCCD0_L	N13	VCCD0*
CBUS_VCCD1_L	L12	VCCD1*
CBUS_VPPD0	K9	VPPD0
CBUS_VPPD1	M11	VPPD1
CBUS_DET_1_L (18 39)	L13	CD1*/CCD1*
CBUS_DET_2_L (18 39)	B5	CD2*/CCD2*
CBUS_IORD_L (18)	F12	IORD*/CAD13
CBUS_IOWR_L (18)	C11	IOWR*/CAD15
CBUS_OE_L (18)	G10	OE*/CAD11
CBUS_CE1_L (18)	H13	CE1*/CC/BE0*
CBUS_VS1 (18)	B2	VS1*/CVS1
CBUS_VS2 (18)	A9	VS2*/CVS2
CBUS_WE_L (18)	D13	WE*/CGNT*
CBUS_READY (18)	A6	RDY/IREQ*/CINT*
CBUS_RESET_L (18)	D8	RESET/CRST*
CBUS_REG_L (18)	A8	REG*/CC/BE3*
CBUS_BVD1_L (18)	C6	BVD1/CSTSCHG/STSCHG*/RI*
CBUS_BVD2_L (18)	D6	BVD2/SPKR*/CAUDIO
INTEGRATED PULL-UP	WP/IOIS16*/CCLKRUN*	
CBUS_CE2_L (18)	G13	CE2/CAD10*
CBUS_INPACK_L (18)	B8	INPACK/CREQ*
CBUS_WAIT_L (18)	B6	WAIT/CSERR*
CBUS_ADDR<0> (18)	C7	A0/CAD26
CBUS_ADDR<1> (18)	D7	A1/CAD25
CBUS_ADDR<2> (18)	B7	A2/CAD24
CBUS_ADDR<3> (18)	D10	A3/CAD23
CBUS_ADDR<4> (18)	B12	A4/CAD22
CBUS_ADDR<5> (18)	C8	A5/CAD21
CBUS_ADDR<6> (18)	C9	A6/CAD20
CBUS_ADDR<7> (18)	A12	A7/CAD18
CBUS_ADDR<8> (18)	E11	A8/CC/BE1*
CBUS_ADDR<9> (18)	F11	A9/CAD14
CBUS_ADDR<10> (18)	G11	A10/CAD9
CBUS_ADDR<11> (18)	G12	A11/CAD12
CBUS_ADDR<12> (18)	D9	A12/CC/BE2*
CBUS_ADDR<13> (18)	E12	A13/CPAR
CBUS_ADDR<14> (18)	D12	A14/CPERR*
CBUS_ADDR<15> (18)	C10	A15/CIRDY*
CBUS_ADDR_16_UF	B13	A16/CCLK
CBUS_ADDR<17> (18)	F10	A17/CAD16
CBUS_ADDR<18> (18)	E13	A18/RSVD
CBUS_ADDR<19> (18)	A13	A19/CBLOCK*
CBUS_ADDR<20> (18)	E10	A20/CSTOP*
CBUS_ADDR<21> (18)	D11	A21/CDEVSEL*
CBUS_ADDR<22> (18)	C12	A22/CTRDY*
CBUS_ADDR<23> (18)	A10	A23/CFRAME*
CBUS_ADDR<24> (18)	B10	A24/CAD17
CBUS_ADDR<25> (18)	B9	A25/CAD19
CBUS_DATA<0> (18)	A4	D0/CAD27
CBUS_DATA<1> (18)	C4	D1/CAD29
CBUS_DATA<2> (18)	A3	D2/RSVD
CBUS_DATA<3> (18)	K11	D3/CAD0
CBUS_DATA<4> (18)	K12	D4/CAD1
CBUS_DATA<5> (18)	J13	D5/CAD3
CBUS_DATA<6> (18)	J10	D6/CAD5
CBUS_DATA<7> (18)	H12	D7/CAD7
CBUS_DATA<8> (18)	C5	D8/CAD28
CBUS_DATA<9> (18)	B4	D9/CAD30
CBUS_DATA<10> (18)	B3	D10/CAD31
CBUS_DATA<11> (18)	M12	D11/CAD2
CBUS_DATA<12> (18)	J11	D12/CAD4
CBUS_DATA<13> (18)	K13	D13/CAD6
CBUS_DATA<14> (18)	J12	D14/RSVD
CBUS_DATA<15> (18)	H11	D15/CAD8

A2 A11 D1 F13 H4 K8 M13 N2 — GND

R719 22 5% 1/16W MF 402

R723 47 5% 1/16W MF 402 — MAIN_RESET_L (39 29 24 19 17 14)

RP1 10K 5% 1/32W 25V SM

CBUS_MFUNC1_PD (18)	6
CBUS_MFUNC2_PD (18)	4
CBUS_MFUNC3_PD (18)	7
CBUS_MFUNC4_PD (18)	3
CBUS_MFUNC5_PD (18)	9
CBUS_MFUNC6_PD (18)	8
	2
	1
	5
	10

SLEEP_L_LS5 (34 25 19 32)

R726 0 5% 1/16W MF 402 — TPS2211_SHTDWN

+3V_MAIN

+5V_MAIN

U4 TPS2211 SSOI AVPP

NC	9	
V_12	5	V_5_1
	6	V_5_2
	3	V_3_1
	4	V_3_2
	1	VCCD0
	2	VCCD1
	15	VPPD0
	14	VPPD1
	16	SHTDWN
	7	GND
AVPP	10	
AVCC0	11	
AVCC1	12	
AVCC2	13	
OC	8	NC

+VPP_CBUS_SW (18 38)

+VCC_CBUS_SW (18 38)

C40 0.1uF 20% 16V CERM 402

C37 0.1uF 20% 16V CERM 402

0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV

MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!

TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW

C796 2.2uF 20% 16V CERM 805

C800 2.2uF 20% 16V CERM 805

R724 47 5% 1/16W MF 402 — CBUS_ADDR<16> (18)

PC CARD/CARDBUS CONNECTOR

CRITICAL

J5 QT500806-L111 M-ST-SM1

	84	81	
	2	1	CBUS_DATA<3> (18)
CBUS_DET_1_L (39 18)	4	3	CBUS_DATA<4> (18)
CBUS_DATA<11> (18)	6	5	CBUS_DATA<5> (18)
CBUS_DATA<12> (18)	8	7	CBUS_DATA<6> (18)
CBUS_DATA<13> (18)	10	9	
	12	11	CBUS_DATA<7> (18)
CBUS_DATA<14> (18)	14	13	CBUS_CE1_L (18)
CBUS_DATA<15> (18)	16	15	CBUS_ADDR<10> (18)
CBUS_CE2_L (18)	18	17	CBUS_OE_L (18)
CBUS_VS1 (18)	20	19	
	22	21	CBUS_ADDR<11> (18)
CBUS_IORD_L (18)	24	23	CBUS_ADDR<9> (18)
CBUS_IOWR_L (18)	26	25	CBUS_ADDR<8> (18)
CBUS_ADDR<17> (18)	28	27	CBUS_ADDR<13> (18)
CBUS_ADDR<18> (18)	30	29	
	32	31	CBUS_ADDR<14> (18)
CBUS_ADDR<19> (18)	34	33	CBUS_WE_L (18)
CBUS_ADDR<20> (18)	36	35	CBUS_READY (18)
CBUS_ADDR<21> (18)	38	37	+VCC_CBUS_SW (18 38)
+VCC_CBUS_SW (38 18)	40	39	
	42	41	+VPP_CBUS_SW (18 38)
+VPP_CBUS_SW (38 18)	44	43	CBUS_ADDR<16> (18)
CBUS_ADDR<22> (18)	46	45	CBUS_ADDR<15> (18)
CBUS_ADDR<23> (18)	48	47	CBUS_ADDR<12> (18)
CBUS_ADDR<24> (18)	50	49	
	52	51	CBUS_ADDR<7> (18)
CBUS_ADDR<25> (18)	54	53	CBUS_ADDR<6> (18)
CBUS_VS2 (18)	56	55	CBUS_ADDR<5> (18)
CBUS_RESET_L (18)	58	57	CBUS_ADDR<4> (18)
CBUS_WAIT_L (18)	60	59	
	62	61	CBUS_ADDR<3> (18)
CBUS_INPACK_L (18)	64	63	CBUS_ADDR<2> (18)
CBUS_REG_L (18)	66	65	CBUS_ADDR<1> (18)
CBUS_BVD2_L (18)	68	67	CBUS_ADDR<0> (18)
CBUS_BVD1_L (18)	70	69	
	72	71	CBUS_DATA<0> (18)
CBUS_DATA<8> (18)	74	73	CBUS_DATA<1> (18)
CBUS_DATA<9> (18)	76	75	CBUS_DATA<2> (18)
CBUS_DATA<10> (18)	78	77	CBUS_WP_L (18)
CBUS_DET_2_L (39 18)	80	79	
	83	82	

CARDBUS

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6653 | REV. C

SCALE NONE | SHT 18 OF 44

SIL1162 DVI-Compliant Transmitter

Ext. TMDS source termination

M11 AGP INTERFACE

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

FOR 2.5 VDDR1
MEMVMODE0=1.8V
MEMVMODE1=GND
FOR 1.8 VDDR1
MEMVMODE0=GND
MEMVMODE1=1.8V

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0318	197S0048		G1	Alt. for Siward Part

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 19 OF 44	

Int.TMDS Termination

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU_TMDS_CLK_CMF
R374 49.9 1% 1/16W MF 402 — GPU_TMDS_CLK
R377 49.9 1% 1/16W MF 402 — GPU_TMDS_CLKN
C515 470pF 10% 50V CERM 402
C522 470pF 10% 50V CERM 402

GPU_TMDS_D0_CMF
R367 75 1% 1/16W MF 402 — GPU_TMDS_D0
R369 75 1% 1/16W MF 402 — GPU_TMDS_DN<0>
C511 470pF 10% 50V CERM 402
C507 470pF 10% 50V CERM 402
+1.8V_GPU
+3V_GPU
R389 10K 5% 1/16W MF 402 (INT_TMDS)
R840 10K 5% 1/16W MF 402 (EXT_TMDS) — ZV_LCDDATA20_PU

GPU_TMDS_D1_CMF
R362 75 1% 1/16W MF 402 — GPU_TMDS_DP<1>
R355 75 1% 1/16W MF 402 — GPU_TMDS_DN<1>
C487 470pF 10% 50V CERM 402
C497 470pF 10% 50V CERM 402
R378 1K 5% 1/4W MF 402

GPU_TMDS_D2_CMF
R350 75 1% 1/16W MF 402 — GPU_TMDS_DP<2>
R340 75 1% 1/16W MF 402 — GPU_TMDS_DN<2>
C479 470pF 10% 50V CERM 402
C469 470pF 10% 50V CERM 402
+3V_GPU
NO STUFF R380 10K 5% 1/16W MF 402 — HPD_PWR_SNS_EN
R765 0 5% 1/16W MF 402 — GPU_TMDS_DN<0> — ATI_TMDS_DN<0>
R767 0 5% 1/16W MF 402 — GPU_TMDS_DP<0> — ATI_TMDS_DP<0>
R760 0 5% 1/16W MF 402 — GPU_TMDS_DN<1> — ATI_TMDS_DN<1>
R762 0 5% 1/16W MF 402 — GPU_TMDS_DP<1> — ATI_TMDS_DP<1>
R764 0 5% 1/16W MF 402 — GPU_TMDS_DN<2> — ATI_TMDS_DN<2>
R766 0 5% 1/16W MF 402 — GPU_TMDS_DP<2> — ATI_TMDS_DP<2>
R761 0 5% 1/16W MF 402 — GPU_TMDS_CLKN — ATI_TMDS_CLKN
R763 0 5% 1/16W MF 402 — GPU_TMDS_CLKP — ATI_TMDS_CLKP

Place all TMDS 10 ohms close to GPU

ATI 64MB CRITICAL
U47 RAGE_MOBILITY M11-CSP64 64MB BGA (3 OF 6)

ATI_DVOD<0>	AJ5	ZV_LCDDATA0
ATI_DVOD<1>	AK5	ZV_LCDDATA1
ATI_DVOD<2>	AG6	ZV_LCDDATA2
ATI_DVOD<3>	AH6	ZV_LCDDATA3
ATI_DVOD<4>	AJ6	ZV_LCDDATA4
ATI_DVOD<5>	AK6	ZV_LCDDATA5
ATI_DVOD<6>	AG7	ZV_LCDDATA6
ATI_DVOD<7>	AH7	ZV_LCDDATA7
ATI_DVOD<8>	AJ7	ZV_LCDDATA8
ATI_DVOD<9>	AK7	ZV_LCDDATA9
ATI_DVOD<10>	AG8	ZV_LCDDATA10
ATI_DVOD<11>	AH8	ZV_LCDDATA11
NC	AJ8	ZV_LCDDATA12
NC	AK8	ZV_LCDDATA13
NC	AG9	ZV_LCDDATA14
NC	AH9	ZV_LCDDATA15
NC	AJ9	ZV_LCDDATA16
NC	AK9	ZV_LCDDATA17
NC	AG10	ZV_LCDDATA18
NC	AH10	ZV_LCDDATA19
NC	AJ10	ZV_LCDDATA20
NC	AK10	ZV_LCDDATA21
NC	AG11	ZV_LCDDATA22
NC	AH11	ZV_LCDDATA23
ATI_DVO_VSYNC	AJ4	ZV_LCDCNTL0
ATI_DVO_HSYNC	AK4	ZV_LCDCNTL1
ATI_DVOD_DE	AH5	ZV_LCDCNTL2
ATI_DVO_CLKP	AG5	ZV_LCDCNTL3
ATI_AGP_FBSKEW<0>	AJ2	GPIO0
ATI_AGP_FBSKEW<1>	AK2	GPIO1
ATI_X1CLK_SKEW<0>	AK1	GPIO2
ATI_X1CLK_SKEW<1>	AH3	GPIO3
ATI_BUS_CFG<0>	AH2	GPIO4
ATI_BUS_CFG<1>	AJ1	GPIO5
ATI_BUS_CFG<2>	AF4	GPIO6
ATI_GPIO7_SPN	AH1	GPIO7
ATI_GPIO8_PD	AG3	GPIO8
ATI_GPIO9_SPN	AF3	GPIO9
ATI_GPIO10_SPN	AG2	GPIO10
ATI_GPIO11_SPN	AF2	GPIO11
ATI_GPIO12_SPN	AG1	GPIO12
ATI_GPIO13_SPN	AF1	GPIO13
GPU_VCORE_CNTL_L	AE1	GPIO14
ATI_SSCLK_IN	M1	GPIO15
		GPIO16
ATI_TMDS_DN<0>	AJ13	TX0M
ATI_TMDS_DP<0>	AK13	TX0P
ATI_TMDS_DN<1>	AJ14	TX1M
ATI_TMDS_DP<1>	AK14	TX1P
ATI_TMDS_DN<2>	AJ15	TX2M
ATI_TMDS_DP<2>	AK15	TX2P
ATI_TMDS_CLKN	AJ12	TXCM
ATI_TMDS_CLKP	AK12	TXCP
ATI_CLK27M_IN	AJ29	XTALIN
NC	AJ30	XTALOUT
ATI_TESTEN	AH24	TESTEN
NC	AJ26	SSIN
	B24	VSS
	B20	VSS
	A24	VSS

R351 1K 1% 1/16W MF 402 — ATI_TESTEN

ROMCSB	AE5	NC
R	AK28	GPU_R
G	AK27	GPU_G
B	AK26	GPU_B
VSYNC	AG27	ATI_VSYNC
V2SYNC	AG25	NC
HSYNC	AG26	ATI_HSYNC
H2SYNC	AG24	NC
RSET	AK25	ATI_RSET
R2SET	AJ24	ATI_R2SET
Y_G	AK23	GPU_Y
C_R	AK24	GPU_C
COMP_B	AK22	GPU_COMP
DIGON	AE13	FP_PWR_EN
BLON	AF13	INV_ON_PWM
HPD1	AF11	GPU_HPD
AUXWIN	AJ27	AUXWIN_PU
DDC1DATA	AH28	GPU_DVI_DDC_DATA
DDC1CLK	AH27	GPU_DVI_DDC_CLK
DDC2DATA	AE12	LVDS_DDC_DATA
DDC2CLK	AF12	LVDS_DDC_CLK
DDC3DATA	AH26	SI_I2S_DATA
DDC3CLK	AH25	SI_I2C_CLK
TXOUT_U0N	AH18	LVDS_U0N
TXOUT_U0P	AG18	LVDS_U0P
TXOUT_U1N	AH19	LVDS_U1N
TXOUT_U1P	AG19	LVDS_U1P
TXOUT_U2N	AH20	LVDS_U2N
TXOUT_U2P	AG20	LVDS_U2P
TXOUT_U3N	AH22	LVDS_U3N_TP (NO ICT TEST)
TXOUT_U3P	AG22	LVDS_U3P_TP (NO ICT TEST)
TXCLK_UN	AH21	CLKLVDS_UN
TXCLK_UP	AG21	CLKLVDS_UP
TXOUT_L0N	AK16	LVDS_L0N
TXOUT_L0P	AJ16	LVDS_L0P
TXOUT_L1N	AK17	LVDS_L1N
TXOUT_L1P	AJ17	LVDS_L1P
TXOUT_L2N	AK18	LVDS_L2N
TXOUT_L2P	AJ18	LVDS_L2P
TXOUT_L3N	AK20	LVDS_L3N_TP (NO ICT TEST)
TXOUT_L3P	AJ20	LVDS_L3P_TP (NO ICT TEST)
TXCLK_LN	AK19	CLKLVDS_LN
TXCLK_LP	AJ19	CLKLVDS_LP
SSOUT	AJ25	NC
VSS	A20	
VSS	B21	

NO STUFF R346 75 1% 1/16W MF 402 — ATI_VSYNC
NO STUFF R342 75 1% 1/16W MF 402 — ATI_HSYNC
NO STUFF R341 75 1% 1/16W MF 402

+1.5V_AGP
CRITICAL Q23 SI3446DV TSOP — GPU_CORE_OK — +GPU_VDD15_UF
C407 1000pF 10% 50V X7R 402

L17 FERR-220-OHM 0805 — +1.5V_GPU_VDD15 (500mA)

C448 0.01uF 10% 16V CERM 402
C443 0.01uF 10% 16V CERM 402
C435 0.01uF 10% 16V CERM 402
C482 0.01uF 10% 16V CERM 402
C411 10uF 20% 6.3V CERM 805
C505 0.01uF 10% 16V CERM 402
C532 0.01uF 10% 16V CERM 402
C529 0.01uF 10% 16V CERM 402
C526 0.01uF 10% 16V CERM 402

GPU VCORE - 1.2V

(PUT ALL CAPs BELOW ATI ASIC)

C484 10uF 20% 6.3V CERM 805
C485 10uF 20% 6.3V CERM 805
C440 0.22uF 20% 6.3V CERM 402
C441 0.22uF 20% 6.3V CERM 402
C445 0.22uF 20% 6.3V CERM 402
C446 0.22uF 20% 6.3V CERM 402
C449 0.22uF 20% 6.3V CERM 402
C434 0.22uF 20% 6.3V CERM 402
C452 0.22uF 20% 6.3V CERM 402
C451 0.22uF 20% 6.3V CERM 402
C494 0.22uF 20% 6.3V CERM 402
C498 0.22uF 20% 6.3V CERM 402
C509 0.22uF 20% 6.3V CERM 402
C510 0.22uF 20% 6.3V CERM 402
C512 0.22uF 20% 6.3V CERM 402
C513 0.22uF 20% 6.3V CERM 402
C524 0.22uF 20% 6.3V CERM 402
C525 0.22uF 20% 6.3V CERM 402
C528 0.22uF 20% 6.3V CERM 402
C531 0.22uF 20% 6.3V CERM 402
C533 0.22uF 20% 6.3V CERM 402
C477 0.22uF 20% 6.3V CERM 402
C486 0.22uF 20% 6.3V CERM 402
C495 0.22uF 20% 6.3V CERM 402

R332 715 1% 1/16W MF 402
R333 499 1% 1/16W MF 402
R359 75 1% 1/16W MF 402
R356 75 1% 1/16W MF 402
R360 75 1% 1/16W MF 402
R779 10K 5% 1/16W MF 402 — +3V_GPU
R366 10K 5% 1/16W MF 402
R368 10K 5% 1/16W MF 402

M10 Power Shut down Sequencing

+2.5V_SLEEP
R384 10K 5% 1/16W MF 402
R387 10K 5% 1/16W MF 402
NO STUFF R386 10K 5% 1/16W MF 402
NO STUFF R382 10K 5% 1/16W MF 402
NO STUFF R383 10K 5% 1/16W MF 402
NO STUFF R385 10K 5% 1/16W MF 402
NO STUFF R381 10K 5% 1/16W MF 402

XW11 SM — DP5 BAS16TW SOT-363 — +2.5V_SLEEP_NECK — XW9 SM — +1.8V_ATI_PVDD
XW12 SM — DP5 BAS16TW SOT-363 — +1.5V_AGP_NECK — XW4 SM — +1.5V_AGP — GPU_VCORE
XW5 SM — DP5 BAS16TW SOT-363 — +GPU_VDD15_UF1 — +GPU_VDD15_NECK — +1.8V_PVDD_NECK

(GPIO0)	ATI_AGP_FBSKEW<0>	
(GPIO1)	ATI_AGP_FBSKEW<1>	
(GPIO2)	ATI_X1CLK_SKEW<0>	
(GPIO3)	ATI_X1CLK_SKEW<1>	
(GPIO4)	ATI_BUS_CFG<0>	
(GPIO5)	ATI_BUS_CFG<1>	
(GPIO6)	ATI_BUS_CFG<2>	

NO STUFF R393 10K 5% 1/16W MF 402
NO STUFF R396 10K 5% 1/16W MF 402
NO STUFF R395 10K 5% 1/16W MF 402
NO STUFF R391 10K 5% 1/16W MF 402
NO STUFF R392 10K 5% 1/16W MF 402
NO STUFF R394 10K 5% 1/16W MF 402
NO STUFF R390 10K 5% 1/16W MF 402

GPU VCORE SUPPLY

WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R329 / (R328//R330))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R329 / R330)

+PBUS
R327 1M 5% 1/16W MF 402
R331 1K 1% 1/16W MF 603
R326 576K 1% 1/16W MF 402
C706 4.7uF 20% 6.3V CERM 1206
C708 4.7uF 20% 6.3V CERM 1206

CRITICAL Q48 SI7860DP SO-8-PWRPK — 1778_VCC
CRITICAL Q49 IRF7832 SO-8

R343 0 5% 1/16W MF 402
NO STUFF R352 63.4K 1% 1/16W MF 402
C466 4.7uF 20% 6.3V CERM 1206 — 1778_GND
+5V_MAIN
C431 0.1uF 20% 25V CERM 603 — 1778_VIN
D12 1N914 SOT23
R358 2.2 5% 1/16W MF 603 — 1778_BST_RC
C481 0.1uF 20% 25V CERM 603

R357 100K 5% 1/16W MF 402 — 1778_SHDN_L
U32 LTC1778 SSOP — EXT_INT_VIN, VCC, VCC2, RUN/SS, ITH, VRNG, FCB, PGOOD, SGND, PGND, BOOST, TG, SW, BG, VFB, ION
R339 20K 1% 1/16W MF 402 — 1778_ITH_RC
C465 220pF 5% 50V CERM 402
C455 470pF 10% 50V CERM 402
NO STUFF R344 0 5% 1/16W MF 402
NO STUFF R353 0 5% 1/16W MF 402
C480 0.1uF 10% 16V CERM 402
NO STUFF C838 0.001uF 10% 50V CERM 402
OMIT XW6 SM

CRITICAL L64 2.1uH-11A SM — GPU_VCORE_SW
D29 MBRS130LT3 SM
C704 22uF 20% 6.3V CERM 1210
CRITICAL C705 330uF 20% 6.3V TANT CASE-D4
CRITICAL C707 330uF 20% 6.3V TANT CASE-D4
CRITICAL C711 330uF 20% 6.3V TANT CASE-D4

R329 4.99K 1% 1/16W MF 402 — 1778_VFB
R328 18.2K 1% 1/16W MF 402
R330 20K 1% 1/16W MF 402
R361 1.82K 1% 1/16W MF 402
R786 100K 5% 1/16W MF 402
C846 0.1uF 20% 25V CERM 402
R549 10K 5% 1/16W MF 402 — GPU_VCORE_CNTL1
NO STUFF C712 0.1uF 20% 25V CERM 402
Q25 2N7002DW SOT-363 — GPU_VCORE_CNTL_RC — GPU_VCORE_CNTL
Q25 2N7002DW SOT-363

R558 10K 5% 1/16W MF 402 — GPU_VCORE_PWR_SEQ
R555 33K 5% 1/16W MF 402 — GPU_VCORE_SEQ_L
Q51 2N3904 SM — GPU_VCORE_SEQ
Q52 2N3904 SM
R559 100K 5% 1/16W MF 402 — +1.5V_AGP
R556 100K 5% 1/16W MF 402 — +5V_MAIN
DP7 BAS16TW SOT-363 — SLEEP_L_LS5
DP7 BAS16TW SOT-363 — DCDC_EN

M11 CORE PWR/LVDS/TMDS
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SIZE D | DRAWING NUMBER 051-6653 | REV. C
SCALE NONE | SHT 20 OF 44

GPU PLL - 1.8V

AGP 4X I/O - 1.5V

MEMORY CORE - 2.5V

LVDS PLL - 1.8V

MEMORY PLL - 1.8V

LVDS - 2.5V

LVDS/TMDS - 1.8V

MEMORY I/O

1.8V DVO POWER (EXT.TMDS)

3.3V IO SUPPLY

(Max Current varies, depends on usage)

1.5V

1.8V

2.5V

1.8V

3.3V

GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V

ATI_64MB
CRITICAL
U47
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(4 OF 6)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRAPHICTLR,667BGA	U47	CRITICAL	ATI_128MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0183	338S0154	ATI_64MB	U47	ATI M11 64MB A16
338S0182	338S0158	ATI_128MB	U47	ATI M11 128MB A16

M11 POWER

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 21 OF 44	

EXTERNAL VIDEO (DVI) INTERFACE

VGA SYNC BUFFERS

+3V_MAIN

U40 74AHC1G32 SM

U39 74AHC1G32 SM

L38 OMIT FERR-60-OHM-0.1A 0402

L36 OMIT FERR-60-OHM-0.1A 0402

20 ATI_VSYNC → ATI_VSYNC_BUF → VGA_VSYNC 22 39

20 ATI_HSYNC → ATI_HSYNC_BUF → VGA_HSYNC 22 39

PLACE L1002 & L1003 CLOSE TO DVI CONNECTOR

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

L45 CRITICAL 90-OHM-300mA 2012H SYM_VER-1

L46 CRITICAL 90-OHM-300mA 2012H SYM_VER-1

L47 CRITICAL 90-OHM-300mA 2012H SYM_VER-1

TMDS_DN<0> 37 39 19 → TMDS_CONN_DN<0>

TMDS_DP<0> → TMDS_CONN_DP<0>

TMDS_DN<2> → TMDS_CONN_DN<2>

TMDS_DP<2> → TMDS_CONN_DP<2> 19 37 39

TMDS_DN<1> → TMDS_CONN_DN<1>

TMDS_DP<1> → TMDS_CONN_DP<1>

L37 370-OHM SYM_VER-1

TMDS_CLKP 37 19 → TMDS_CONN_CLKP 22 36 39

TMDS_CLKN 37 19 → TMDS_CONN_CLKN 22 36 39

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

L50 0.068uH SM

L49 0.068uH SM

L44 0.068uH SM

L43 0.068uH SM

L41 0.068uH SM

L40 0.068uH SM

GPU_B 20 → GPU_B_FILTR → VGA_B 22 39

GPU_G 20 → GPU_G_FILTR → VGA_G 22 39

GPU_R 20 → GPU_R_FILTR → VGA_R 22 39

C642 4.7pF 5% 50V CERM 402

C641 3.3pF 0.25% 50V CERM 402

C635 4.7pF 5% 50V CERM 402

C634 3.3pF 0.25% 50V CERM 402

C632 4.7pF 5% 50V CERM 402

C631 3.3pF 0.25% 50V CERM 402

R462 75 1% 1/16W MF 402

R458 75 1% 1/16W MF 402

R456 75 1% 1/16W MF 402

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP

F2 CRITICAL 0.5AMP-13.2V SM

L42 400-OHM-EMI SM-1

+5V_DDC_SLEEP 22 38 39 → +5V_DDC_SLEEP_UF 38

Isolation required for DVI power switch

D19 SM MBR0530 DDC_CLK_ISO

R476 4.7k 5% 1/16W MF 402

R478 4.7k 5% 1/16W MF 402

R479 100 5% 1/16W MF 402

R477 100 5% 1/16W MF 402

R469 100 5% 1/16W MF 402

C654 100pF 5% 25V CERM 201

C655 100pF 5% 25V CERM 201

C667 0.01uF 10% 50V CERM 603

C653 100pF 5% 25V CERM 201

PLACE NEAR C5A & C5B

R464 0 5% 1/16W MF 402

R463 0 5% 1/16W MF 402

PLACE NEAR 3, 11 & 19

CHGND1 CHGND2

J22 CRITICAL QH1112 F-RT-TH

CHGND1

TMDS_CONN_DN<0> 1
TMDS_CONN_DP<0> 18
TMDS_CONN_DN<2> 9
TMDS_CONN_DP<2> 2
TMDS_CONN_DN<1> 38
TMDS_CONN_DP<1> 10
NC 19
NC 20
NC 21
NC 22
(+5V_DDC_SLEEP) 14
DVI_DDC_CLK_UF 3
DVI_DDC_DATA_UF 11
VGA_VSYNC 4
DVI_HPD_UF 12
VGA_R 5
VGA_G 13
VGA_B 6
TMDS_CONN_CLKP 23
TMDS_CONN_CLKN 7
15
24
8
16
C3
C5B
C5A
C4
C2
34
32
35
33
31
36
17

(TMDS_DN<5>) (TMDS_DN<4>) (TMDS_DN<3>) (TMDS_DP<5>) (TMDS_DP<4>) (TMDS_DP<3>)

3V LEVEL SHIFTERS

+3V_SLEEP

Q39 2N7002DW SOT-363

Q39 2N7002DW SOT-363

Q40 2N7002DW SOT-363

DVI_DDC_CLK → GPU_DVI_DDC_CLK 20

DVI_DDC_DATA → GPU_DVI_DDC_DATA 20

DVI_HPD → GPU_HPD 20

R480 10K 5% 1/16W MF 402

R474 10k 5% 1/16W MF 402

R481 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V_will be driven into DDC_CLK. Since P06 fall will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off. Now remote device path is DDC_CLK isolation will be disabled as well.

Q35 TP0610 SM

DVI_DDC_CLK_UF 39 22 → DVI_TURN_ON2

+5V_DDC_SLEEP 39 38 22

R473 680 5% 1/16W MF 402

DVI_TURN_ON_ILIM 1

R459 330 5% 1/16W MF 402

Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

DVI_TURN_ON_BASE

R460 10K 5% 1/16W MF 402

Q35 MMDT3904 SOT-363

SOFT_PWR_ON_L 23 29 33 39

Power key detect path when system is running, HPD normally driven to 3.3V. When power key on remote device pressed,1/16W HPD will be driven to 5V! NV17M COMPARATOR ENABLED BY NV17M GPIO.

+3V_SLEEP

R485 68.1K 1% 1/16W MF 402

C668 0.1uF 10% 16V CERM 402

HPD_4V_REF

U42 LMC7211 SM

DVI_HPD_UF 39 22 → DVI_HPD_DIV

R472 10K 1% 1/16W MF 402

R482 10K 1% 1/16W MF 402

R484 100K 1% 1/16W MF 402

HPD_REF_EN_L

HPD_PWR_SW_BASE

R475 10K 5% 1/16W MF 402

Q35 MMDT3904 SOT-363

HPD_PWR_SW

R470 330 5% 1/16W MF 402

Q40 2N7002DW SOT-363

HPD_PWR_SNS_EN 20

R483 470K 5% 1/16W MF 402

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW15 SM

GPU_TV_GND1 38 → TV_GND1 38 39

L54 FERR-10-OHM-500MA SM

L53 3.3uH 0603

L57 3.3uH 0603

L55 3.3uH 0603

GPU_Y 20

GPU_C 20

GPU_COMP 20

C657 0.01uF 10% 50V CERM 603

C663 560pF 10% 50V CERM 402

C656 560pF 10% 50V CERM 402

C661 560pF 10% 50V CERM 402

C660 560pF 10% 50V CERM 402

C664 560pF 10% 50V CERM 402

C658 560pF 10% 50V CERM 402

C659 0.01uF 10% 50V CERM 603

CRITICAL J21 MINIDIN RT-TH MH11773-WMR8A

TV_C 39

TV_Y 39

TV_COMP 39

CHGND1

XW14 SM

GPU_TV_GND2 38 → TV_GND2 38 39

L56 FERR-10-OHM-500MA SM

Place GND shorts at graphics controller

LCD INTERFACE
LVDS INTERFACE

LCD POWER SWITCH

+3V_MAIN

R347 100K 5% 1/16W MF 402

C474 2200pF 5% 50V CERM 603

R354 100K 5% 1/16W MF 402

LCD_PWREN_L

LCD_DIGON_L

Q28 2N7002 SM

FP_PWR_EN 22 20

TSOP SI3443DV Q29

+3V_LCD_SW 38

L27 FERR-250-OHM SM

+3V_LCD 39 38 (LVDS DDC POWER)

C503 0.001uF 10% 50V CERM 402

+3V_SLEEP

R543 100K 5% 1/16W MF 402

R544 100K 5% 1/16W MF 402

C701 0.001uF 10% 50V CERM 402

LVDS_DDC_CLK 22 39

LVDS_DDC_DATA 20 22 39

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

NO STUFF C702 0.001uF 10% 50V CERM 402

C548 0.001uF 10% 50V CERM 402

CHGND4

J14 CRITICAL G-501973 F-RT-SM

LVDS_DDC_CLK 22 39
LVDS_DDC_DATA 22 39
LVDS_L0N 37 39
LVDS_L0P 37 39
LVDS_L1N 37 39
LVDS_L1P 37 39
LVDS_L2N 39 37 20
LVDS_L2P 39 37 20
CLKLVDS_LN 39 37 20
CLKLVDS_LP 39 37 20
LVDS_U0N 37 20
LVDS_U0P 37 20
LVDS_U1N 37 20
LVDS_U1P 37 20
LVDS_U2N 37 20
LVDS_U2P 37 20
CLKLVDS_UN 37 20
CLKLVDS_UP 37 20
NC

C549 0.001uF 10% 50V CERM 402

R753 0 5% 1/16W MF 402

C819 0.01uF 10% 50V CERM 603

CHGND3

INVERTER INTERFACE

+PBUS

L73 FERR-1K-OHM-EMI SM

+14V_INV 38

+5V_MAIN

Q76 FDG6324L SC70-6

+5V_INV_UF_SW 38

L74 400-OHM-EMI SM-1

R750 100K 5% 1/16W MF 402

FP_PWR_EN

C812 0.001uF 10% 50V CERM 402

C813 10uF 20% 6.3V CERM 805

CRITICAL J4 SM-2MT

+5V_INV_SW 39 38

Q76 FDG6324L SC70-6

FP_PWR_EN 22 20

L72 400-OHM-EMI SM-1

BRIGHT_PWM 39

C815 0.001uF 10% 50V CERM 402

+3V_MAIN

C816 0.001uF 10% 50V CERM 402

C22 0.1uF 10% 16V CERM 402

C19 0.001uF 10% 50V CERM 402

INV_GND

L1 FERR-250-OHM SM

INV_ON_PWM 20

NC7S32 SC70 U2

BRIGHT_PWM_UF

INVERTER EXPECTS ACTIVE HIGH SIGNAL

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
116S1331	2	DISCRETE,RES,33OHM,0402	L36,L38		VGA_BUFFER_RES

VIDEO CONNECTORS

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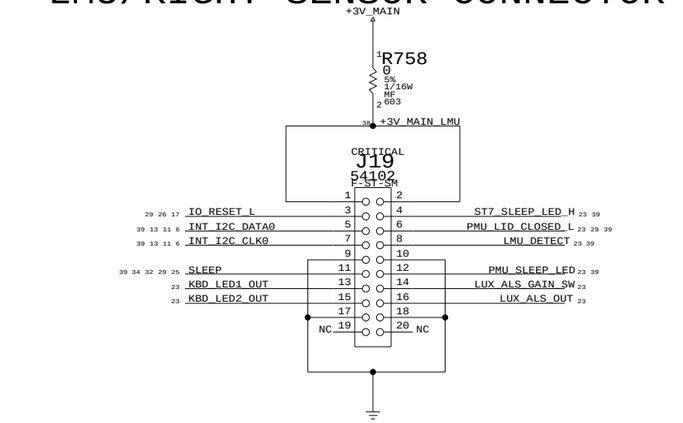
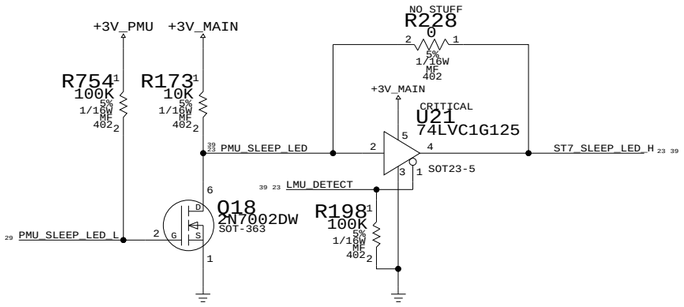
SIZE D | DRAWING NUMBER 051-6653 | REV. C

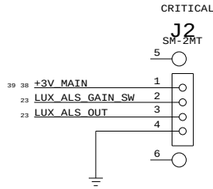
SCALE NONE | SHT 22 44

LMU/RIGHT SENSOR CONNECTOR

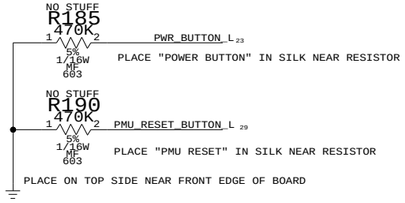




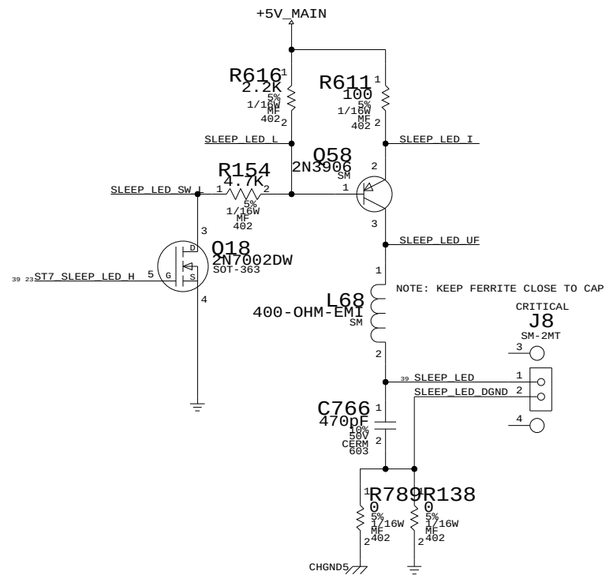
LEFT LIGHT SENSOR CONNECTOR



DEBUG HELPERS

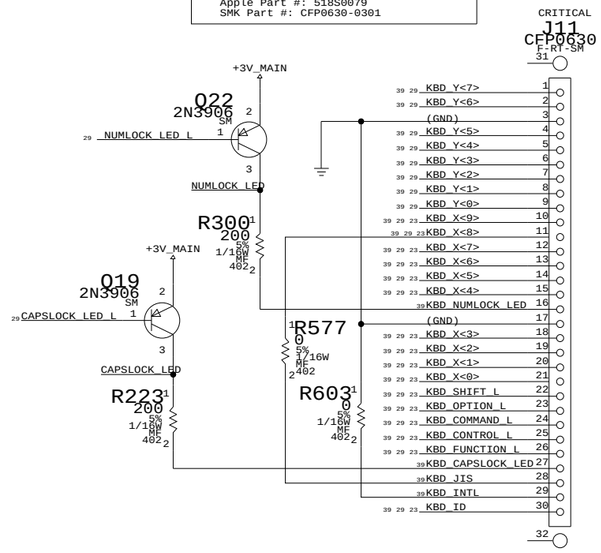


SLEEP LED

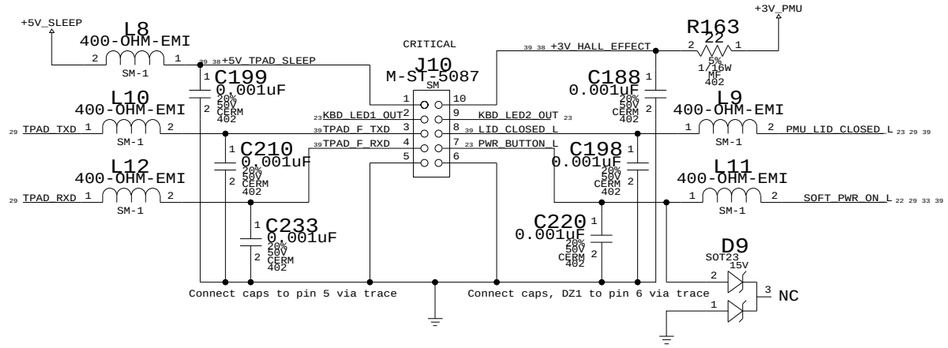


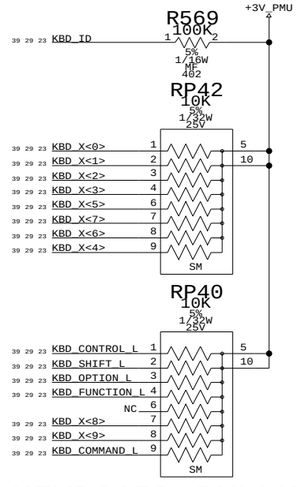
TOP CONTACT ZIF KEYBOARD CONN

CONN,TOP CONTACT ZIF,0.8MM PITCH,30P,SM
Apple Part #: 518S0079
SMK Part #: CFP0630-0301



TRACKPAD/PWR BTN CONN





KEYBOARD PULLUPS

KEYBOARD/TPAD/SLEEP LED

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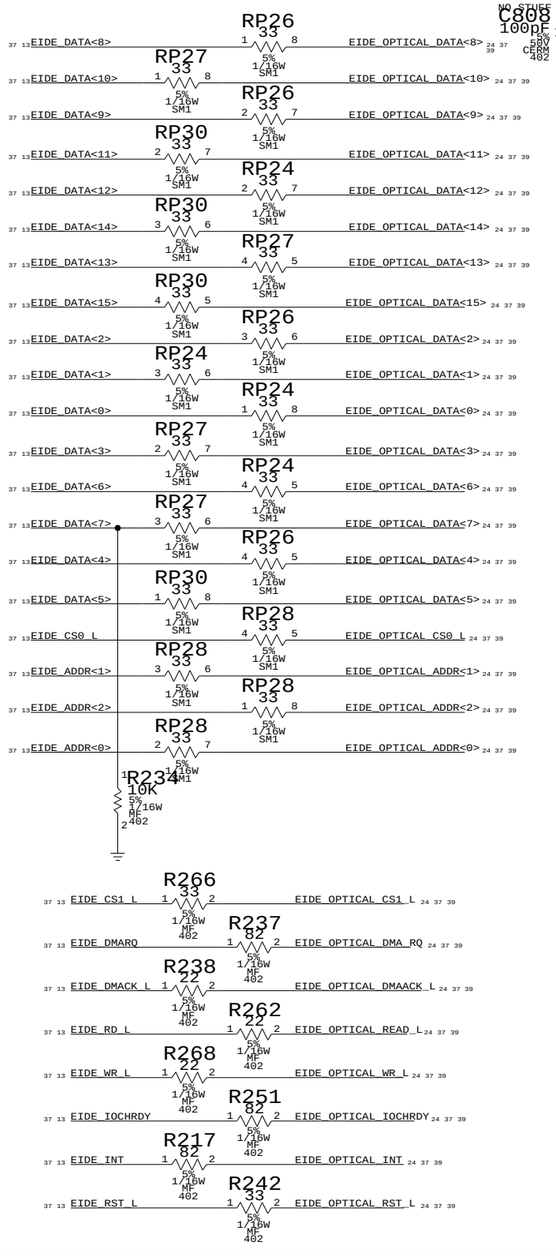
SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 23 OF 44	

WIRELESS INTERFACE

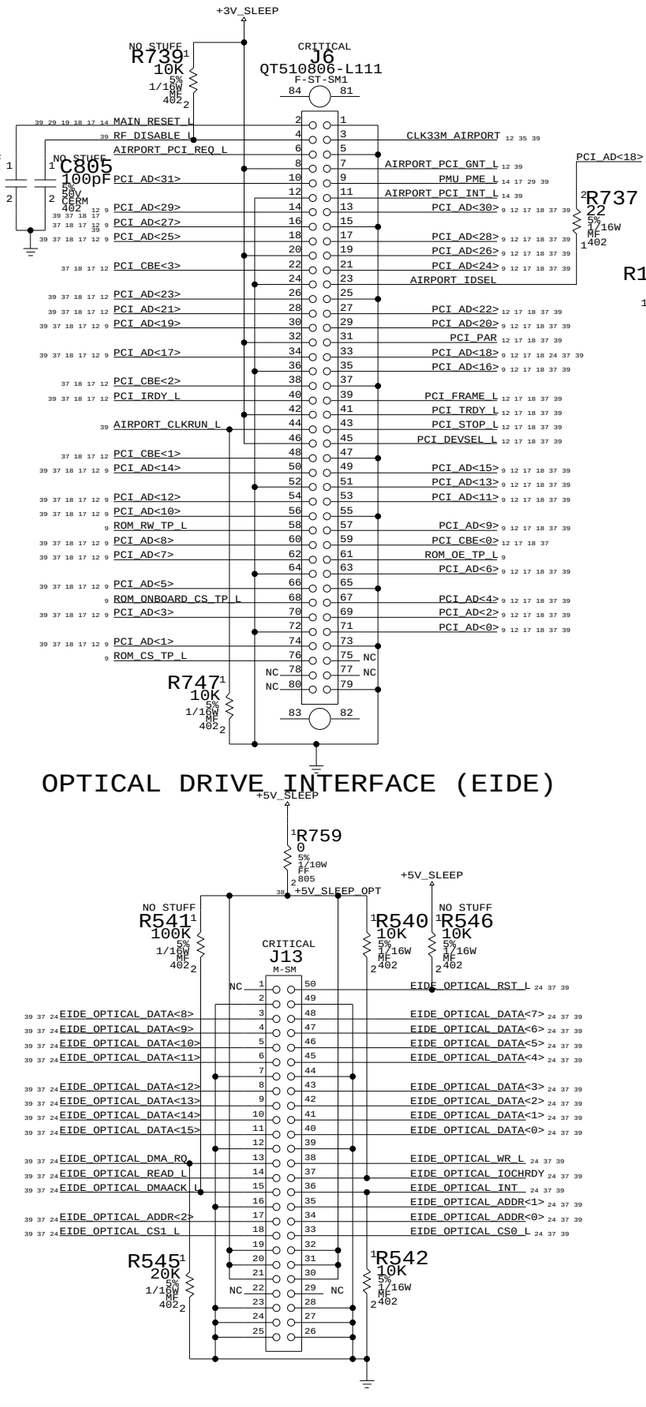
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

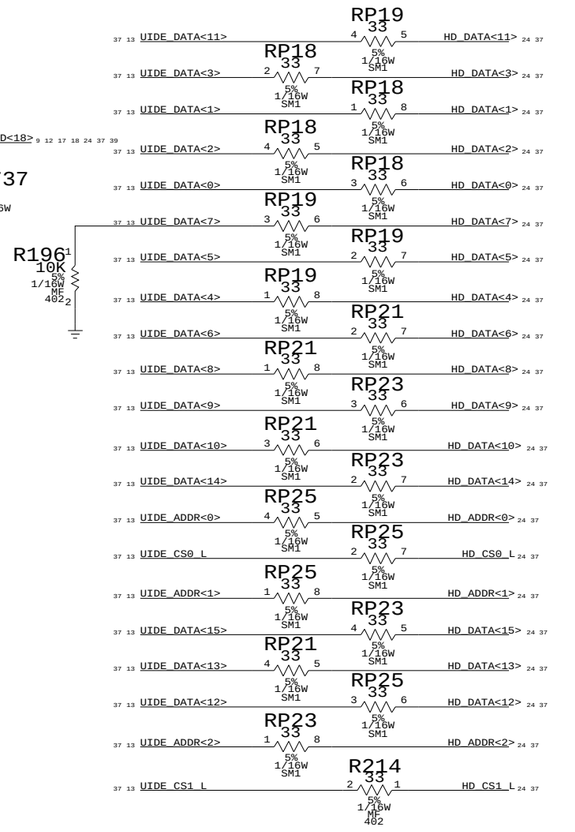
PLACE TERMINATORS NEAR INTREPID



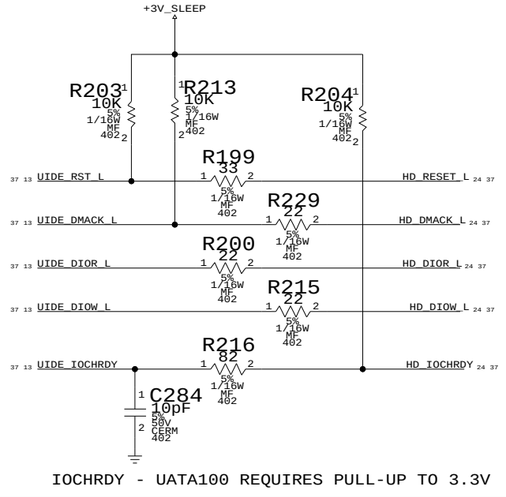
OPTICAL DRIVE INTERFACE (EIDE)



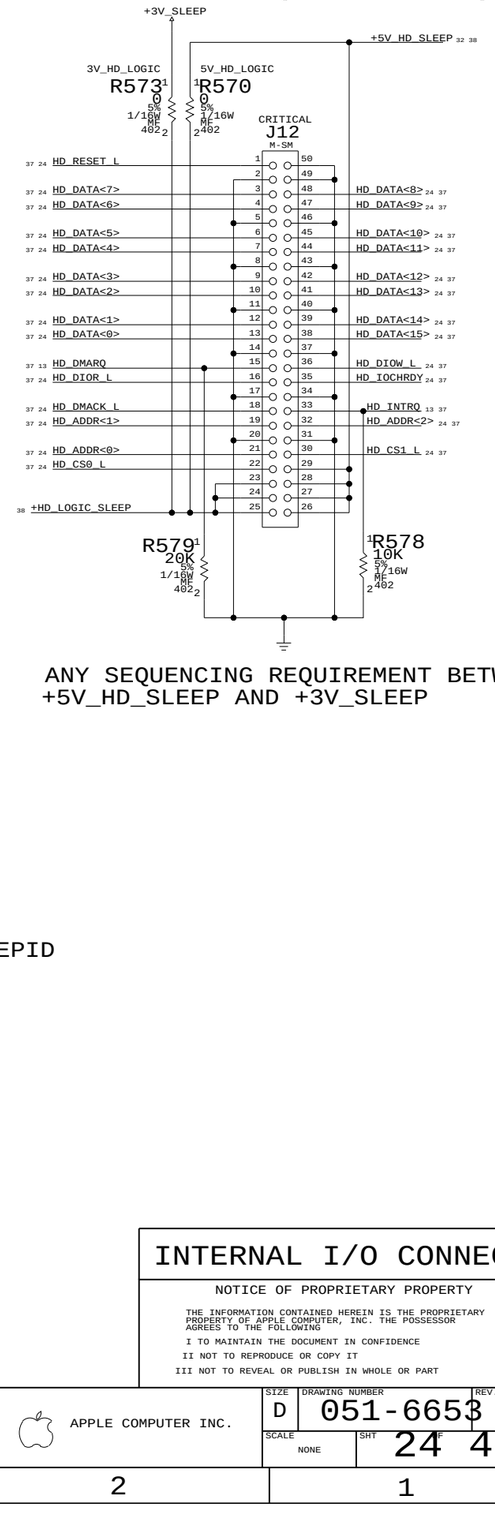
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID



IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN +5V_HD_SLEEP AND +3V_SLEEP

INTERNAL I/O CONNECTORS

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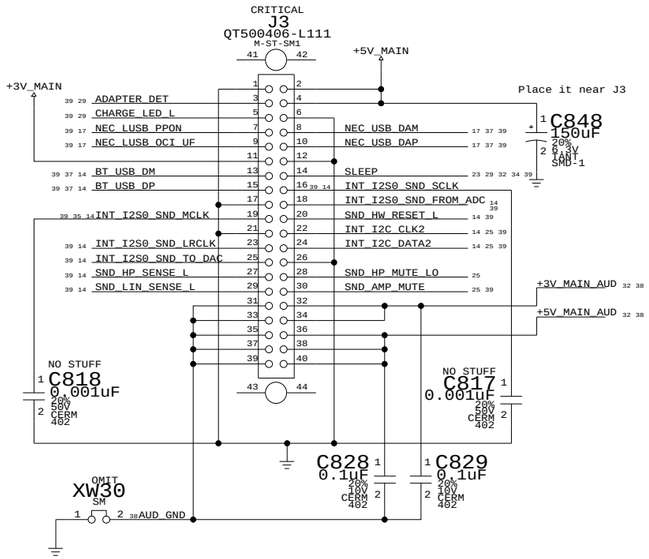
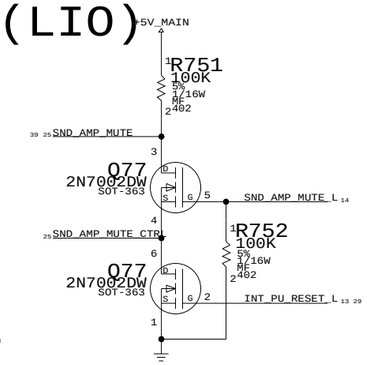
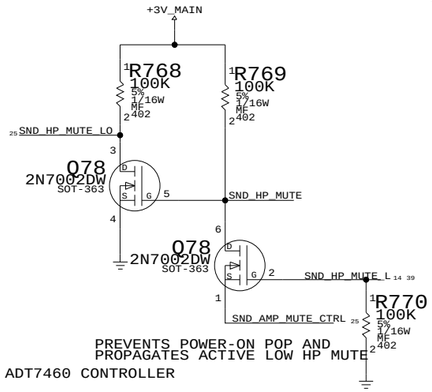
LEFT I/O & AUDIO BOARD (LIO)



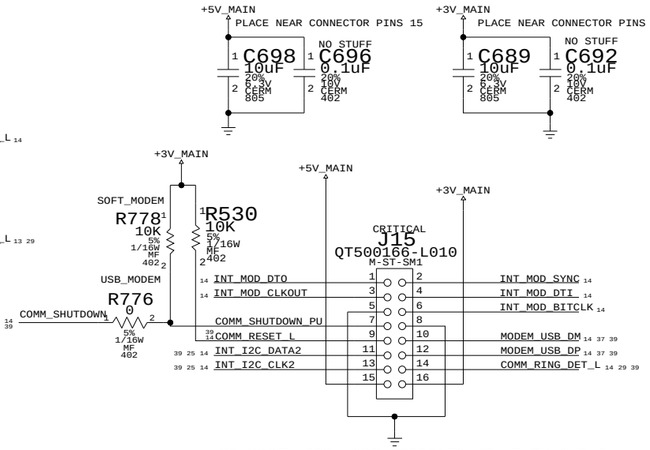


PREVENTS POWER-ON POP AND GENERATES ACTIVE HIGH SPKR MUTE

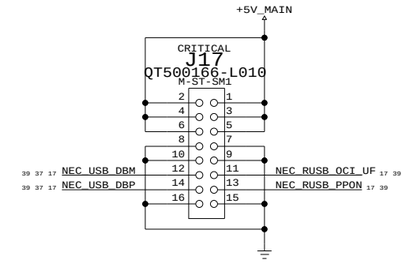


PREVENTS POWER-ON POP AND PROPAGATES ACTIVE LOW HP MUTE

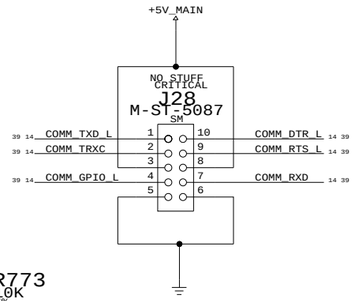
USB MODEM/SOFT MODEM



USB MODEM I2C ADDR ASSIGNED VIA FLEX CABLE

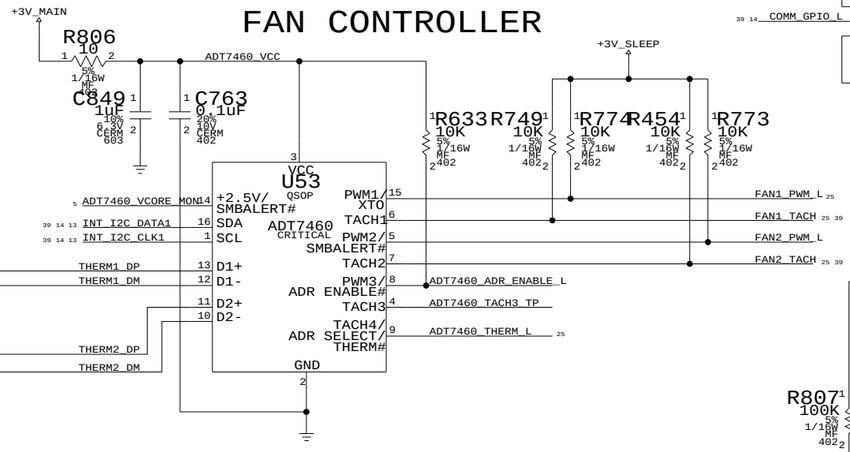


SERIAL DEBUG INTERFACE

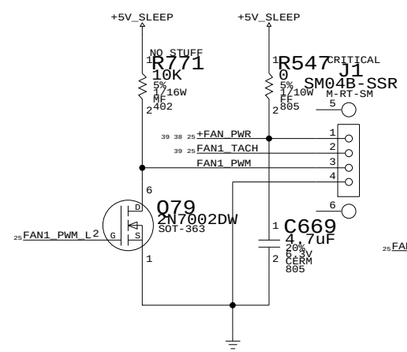


FAN INTERFACE

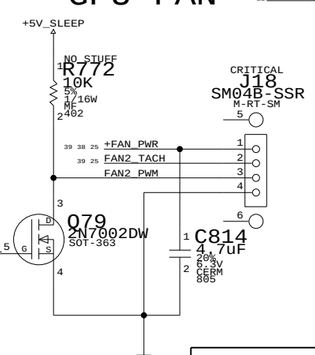
FAN CONTROLLER

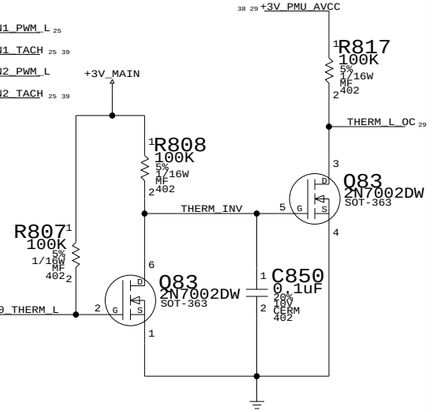


CPU FAN

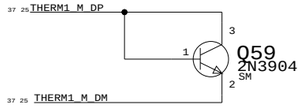


GPU FAN

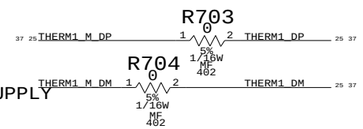




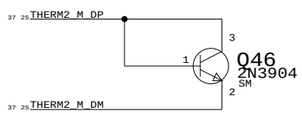
PLACE CLOSE TO CPU
MAIN1

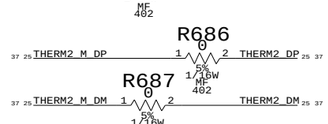


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

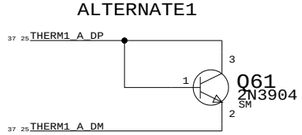


PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2

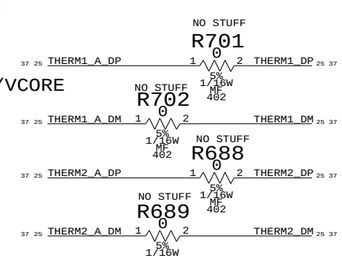


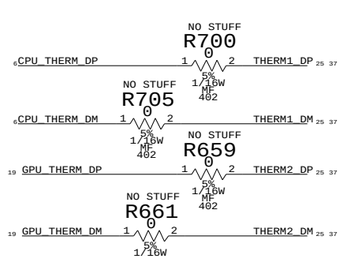


PLACE UNDERNEATH UPPER RAM
ALTERNATE1

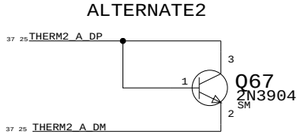


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER





PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



FAN/MODEM/SOUND/BACKUP BATT.

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D	051-6653	C
SCALE: NONE	SHT 25 OF 44	

Ethernet routing priority:
1. Decoupling caps
2. TX SERIES TERMINATION - LOCATE NEAR LINK
3. RX SERIES TERMINATION - LOCATE NEAR PHY

All differential signals should be close, parallel, matched lengths, with minimum via count, and short if possible

Must maintain 50-ohms trace impedance on all MDI pairs and all RJ45 pairs

Sandwich each RJ54 pair between chassis grounds

+3V_MAIN

C680 10uF 20% 6.3V CERM 805

NO STUFF R513 0 5% 1/16W MF 402

3405_MODE

R507 0 5% 1/16W MF 402

U45 LTC3405 SOT23-6 CRITICAL
VIN, RUN, MODE, SW, VFB, GND

LTC3405_SW

CRITICAL L60 3.3uH SM1

R506 665K 1% 1/16W MF 402 R2A

C675 22pF 5% 50V CERM 402

R504 49.9K 1% 1/16W MF 402 R2B

3405_VFB

R503 182K 1% 1/16W MF 402 R1

C674 10uF 20% 6.3V CERM 805

+1_0V_MARVELL

VOUT = 0.8V*(1+R2EQV/R1)
R2EQV = R2A||R2B

PLACE ALL SERIES RES CLOSE TO PHY

R423 0 5% 1/16W MF 402 — CLKENET_LINK_TX — CLKENET_PHY_TX

R421 0 5% 1/16W MF 402 — CLKENET_LINK_RX — CLKENET_PHY_RX

R445 0 5% 1/16W MF 402 — CLKENET_LINK_GBE_REF — CLKENET_PHY_GBE_REF

NO STUFF C851 10pF 5% 50V CERM 402 / C852 10pF 5% 50V CERM 402

Keep C851 & C852 Stubs short

CRITICAL U43 88E1111 BCC

TX_CLK, RX_CLK, 125CLK, TXD0–TXD7, TX_EN, TX_ER, GTX_CLK, RXD0–RXD7, RX_DV, RX_ER, CRS, COL, MDC, MDIO, INT-/INT+, RESET, COMA, S_IN+, S_IN-, S_OUT+, S_OUT-, S_CLK+, S_CLK-, HSDAC+, HSDAC-, XTAL1, XTAL2, VSSC

CTRL10, NC, DVDD, VDDO, VDDOH, VDDOX, AVDD, GND

C594 C601 C608 C619 C603 C599 0.1uF 0.01uF 0.1uF 0.01uF 0.1uF 0.01uF 20% 10V CERM 402

PLACE CAPS (IN ORDER) ON PINS 1, 6, 10/15, 57/62, 67/71, 85

C597 C612 C623 C600 C598 C595 0.1uF 0.01uF 0.1uF 0.01uF 0.1uF 10uF 20% 10V CERM 402 / 6.3V CERM 805

+2_5V_MARVELL

PLACE CAPS (IN ORDER) ON PINS 5, 21/26, 48/52, 66/72, 88, 96

L35 FERR-EMI-600-OHM SM

+2_5V_MARVELL_AVDD

C614 C616 C618 C602 0.1uF 0.01uF 0.1uF 0.01uF 20% 10V CERM 402 / C592 10uF 20% 6.3V CERM 805

PLACE CAPS (IN ORDER) ON PINS 32/35, 36/40, 45 & 78

+2_5V_MAIN

R442 0 5% 1/16W MF 603

C646 C648 C645 C647 0.1uF 0.1uF 0.1uF 0.1uF 20% 10V CERM 402

PLACE CAPS AT CONNECTOR PINS 5 & 6

CRITICAL J23 MJ-R0016 F-RT-TH

PRIMARY: 13, 11, 5 ENET_CTAP, 6 ENET_CTAP, 1 MDI_0+, 2 MDI_0-, 3 MDI_1+, 4 MDI_1-, 7 MDI_2+, 8 MDI_2-, 9 MDI_3+, 10 MDI_3-, 12, 14

1CT:1CT, 75 OHM

SECONDARY: J1 J2 J3 J4 J5 J6 J7 J8

RJ45 CABLE SIDE

RJ45 CHIP SIDE

CHGND1

SHIELD 1000PF, 2000V

MDI_P<0>, MDI_M<0>, MDI_P<1>, MDI_M<1>, MDI_P<2>, MDI_M<2>, MDI_P<3>, MDI_M<3>

R433 R435 R437 R439 49.9 1% 1/16W MF 402

R434 R436 R438 R440 49.9 1% 1/16W MF 402 — MDI0_PD, MDI1_PD, MDI2_PD, MDI3_PD

C622 C613 C615 C617 0.01uF 20% 10V CERM 402

PLACE RESISTORS CLOSE TO PHY

LED_LINK10, LED_LINK100, LED_LINK1000, LED_DUPLEX, LED_RX, LED_TX

SEE CONFIG TABLES (BELOW)

CONFIG0 (000), CONFIG1 (000), CONFIG2 (111), CONFIG3 (110), CONFIG4 (111), CONFIG5 (101), CONFIG6 (000)

TDI, TDO, TCK, TMS, TRST — JTAG_ASIC_TDO_TP, JTAG_ASIC_TCK, JTAG_ASIC_TMS, JTAG_ASIC_TRST_L

RSET — ENET_RSET

SEL_OSC, SEL_2.5V

ENET_RST_L, ENET_COMA, ENET_ENERGY_DET, ENET_HSDACP, ENET_HSDACM, ENET_VSSC

R431 10K 5% 1/16W MF 402 — +2_5V_MARVELL

R430 10K 5% 1/16W MF 402

R432 1.5K 5% 1/16W MF 402

R422 1K 5% 1/16W MF 402 — INT_ENET_RST_L1

D15 1N914 SOT23 — IO_RESET_L

Q32 2N7002DW SOT-363 — AC_IN

Q32 2N7002DW SOT-363 — SLEEP_L_LS5

C611 2.2uF 20% 10V CERM 805

PLACES PHY IN "COMA" MODE WHEN ASLEEP ON BATTERY (SAVES POWER)

NO STUFF R425 20K 5% 1/16W MF 402

PUT CRYSTAL CIRCUIT CLOSE TO PHY

R441 0 5% 1/16W MF 402

CRITICAL Y5 SM-3 25.0000M — CLK25M_XTAL_IN

C604 C624 27pF 5% 50V CERM 402

Y6 LOAD CAPACITANCE IS 16PF

NO STUFF R424 49.9 1% 1/16W MF 402 / NO STUFF R429 49.9 1% 1/16W MF 402

R428 10K 5% 1/16W MF 402

R427 4.99K 1% 1/16W MF 402

CLK25M_ENET_XIN, CLK25M_ENET_XOUT

CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111

10/100/1000 ETHERNET

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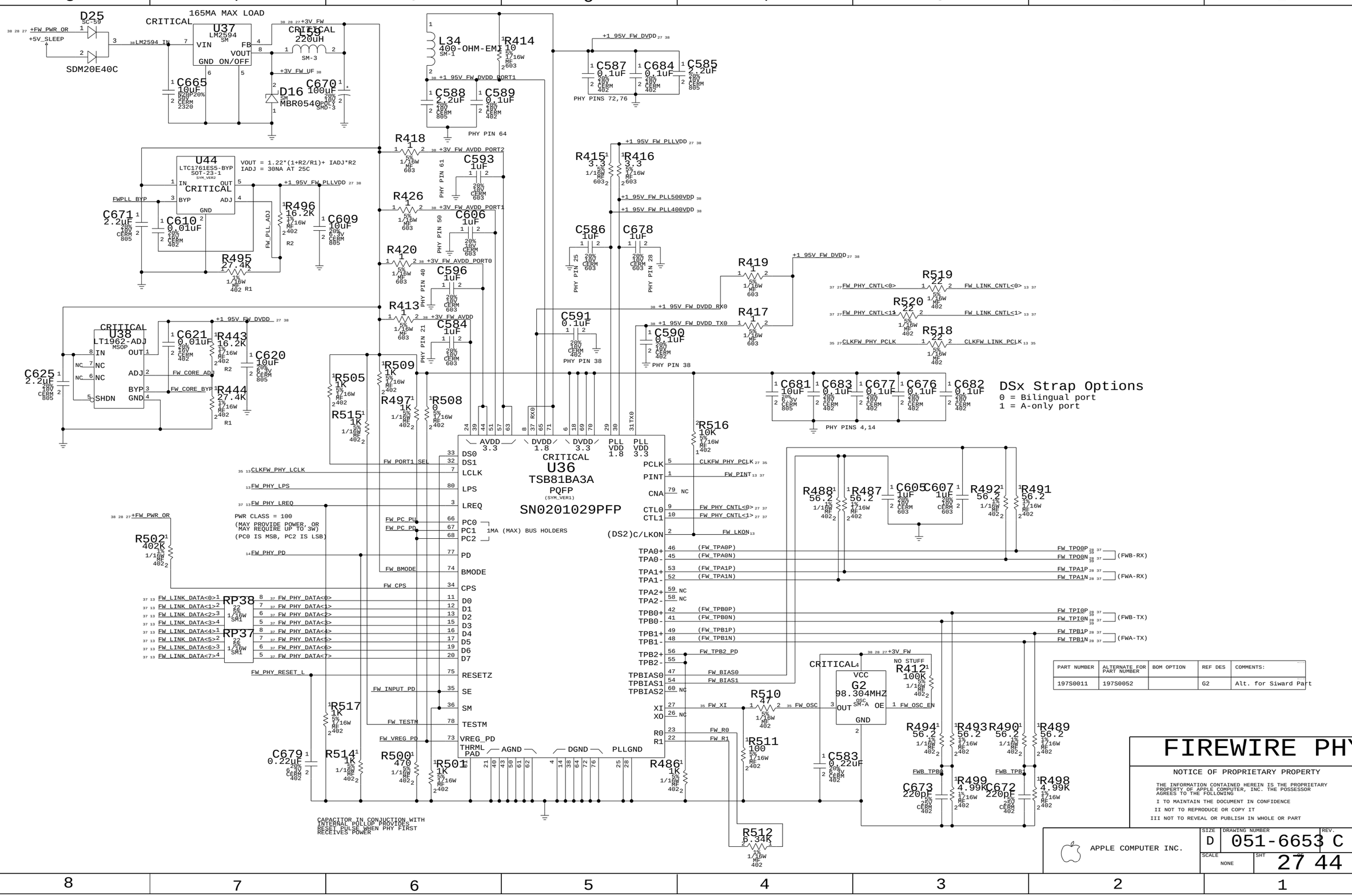
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6653 | REV. C

SCALE NONE | SHT 26 OF 44



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052		G2	Alt. for Siward Part

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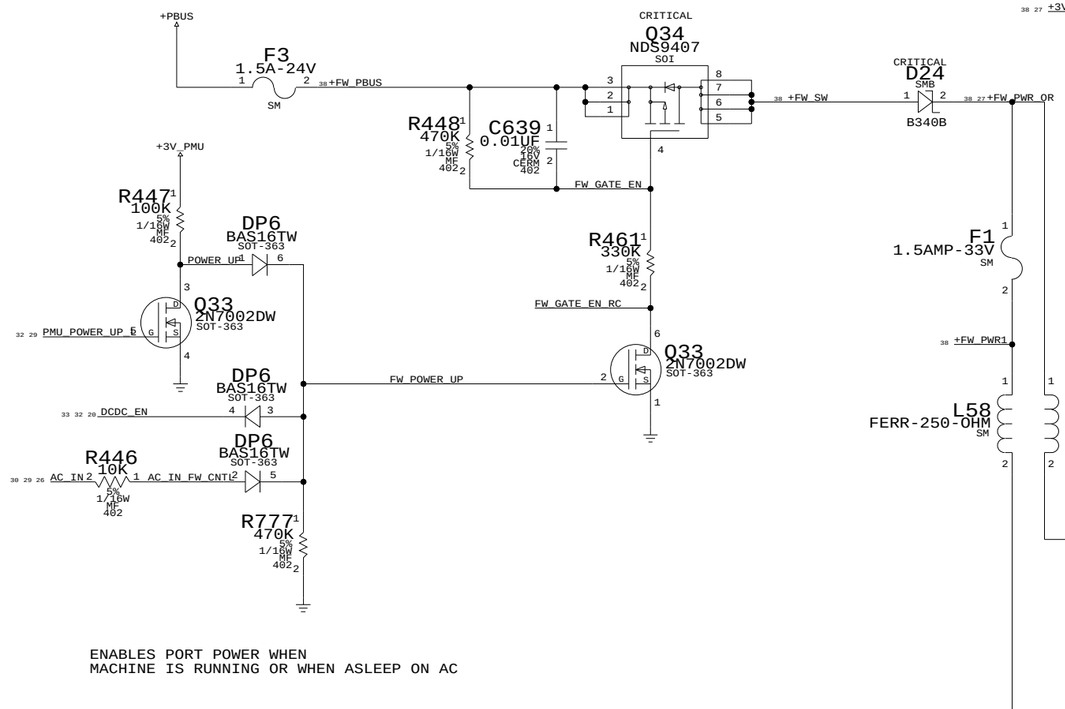
FIREWIRE PHY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 27	44

PORT POWER SWITCH

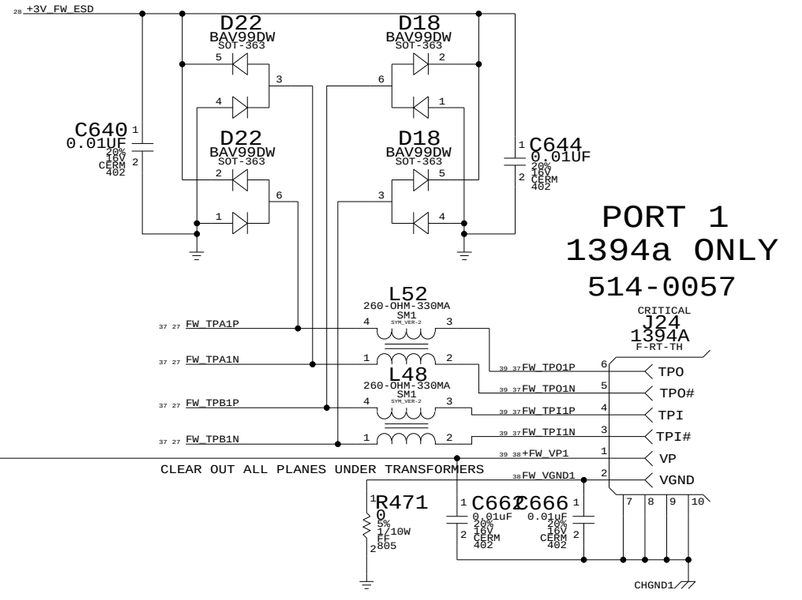


ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

PORT 0
1394a/b
(BILINGUAL)
514S0058

AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO A BETA-ONLY DEVICE THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33



CLEAR OUT ALL PLANES UNDER TRANSFORMERS

PORT 1
1394a ONLY
514-0057

FIREWIRE PORTS

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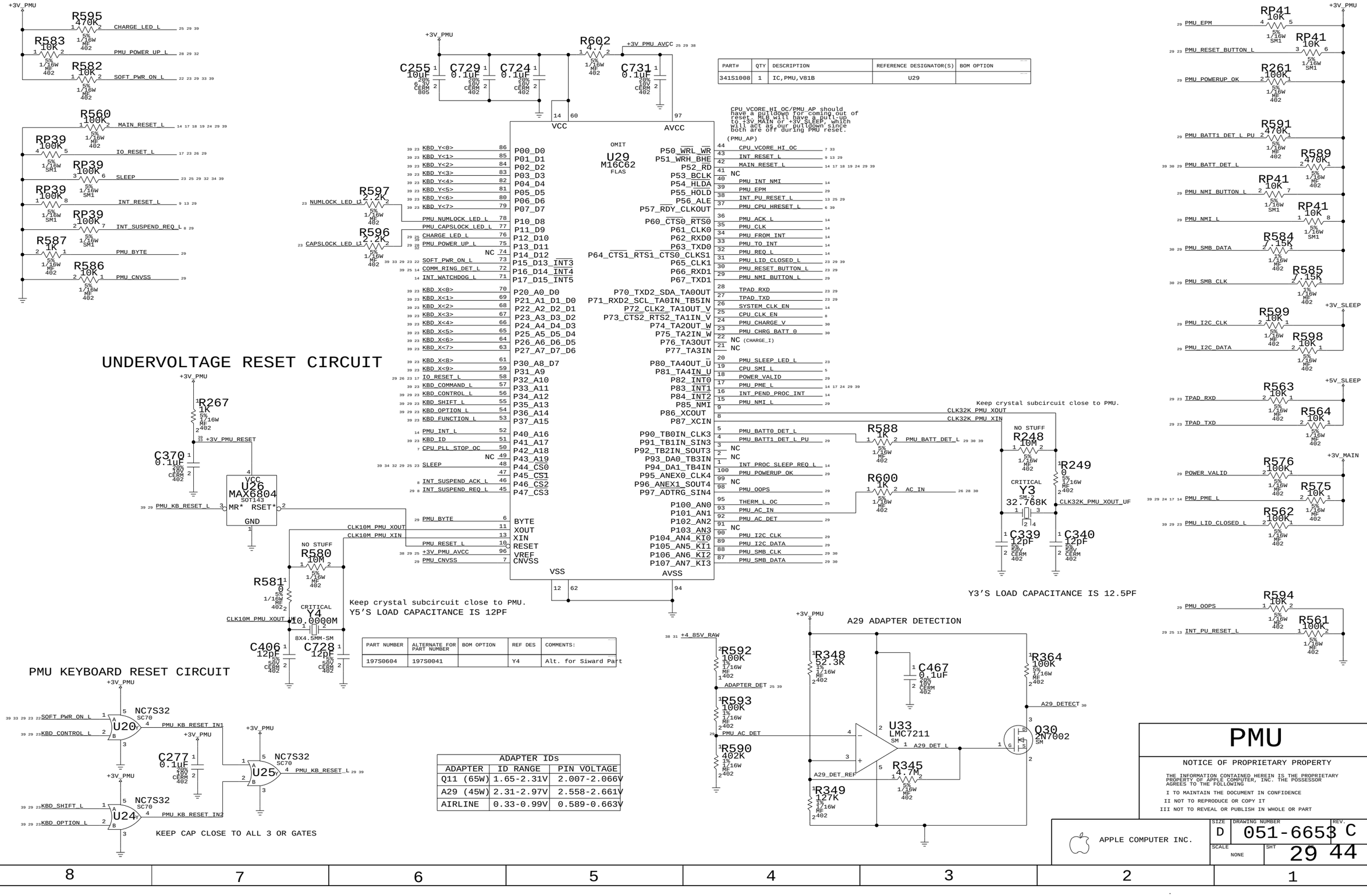
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 28 OF 44	


+3V_PMU
R595 470K CHARGE_LED_L
R583 10K PMU_POWER_UP_L
R582 10K SOFT_PWR_ON_L
R560 100K MAIN_RESET_L
RP39 100K IO_RESET_L
RP39 100K SLEEP
RP39 100K INT_RESET_L
RP39 100K INT_SUSPEND_REQ_L
R587 1K PMU_BYTE
R586 10K PMU_CNVSS
R602 4.7
+3V_PMU_AVCC
C255 10uF
C729 0.1uF
C724 0.1uF
C731 0.1uF
VCC
AVCC
VSS
AVSS
U29
M16C62
FLAS
OMIT
CPU_VCORE_HI_OC/PMU_AP should have a pulldown for coming out of reset. MLB will have a pull-up to +3V_MAIN or +3V_SLEEP, which will act as our pulldown since both are off during PMU reset.
(PMU_AP)
P00_D0 P01_D1 P02_D2 P03_D3 P04_D4 P05_D5 P06_D6 P07_D7
P10_D8 P11_D9 P12_D10 P13_D11 P14_D12 P15_D13_INT3 P16_D14_INT4 P17_D15_INT5
P20_A0_D0 P21_A1_D1_D0 P22_A2_D2_D1 P23_A3_D3_D2 P24_A4_D4_D3 P25_A5_D5_D4 P26_A6_D6_D5 P27_A7_D7_D6
P30_A8_D7 P31_A9 P32_A10 P33_A11 P34_A12 P35_A13 P36_A14 P37_A15
P40_A16 P41_A17 P42_A18 P43_A19 P44_CS0 P45_CS1 P46_CS2 P47_CS3
BYTE XOUT XIN RESET VREF CNVSS
P50_WRL_WR P51_WRH_BHE P52_RD P53_BCLK P54_HLDA P55_HOLD P56_ALE P57_RDY_CLKOUT
P60_CTS0_RTS0 P61_CLK0 P62_RXD0 P63_TXD0 P64_CTS1_RTS1_CTS0_CLKS1 P65_CLK1 P66_RXD1 P67_TXD1
P70_TXD2_SDA_TA0OUT P71_RXD2_SCL_TA0IN_TB5IN P72_CLK2_TA1OUT_V P73_CTS2_RTS2_TA1IN_V P74_TA2OUT_W P75_TA2IN_W P76_TA3OUT P77_TA3IN
P80_TA4OUT_U P81_TA4IN_U P82_INT0 P83_INT1 P84_INT2 P85_NMI P86_XCOUT P87_XCIN
P90_TB0IN_CLK3 P91_TB1IN_SIN3 P92_TB2IN_SOUT3 P93_DA0_TB3IN P94_DA1_TB4IN P95_ANEX0_CLK4 P96_ANEX1_SOUT4 P97_ADTRG_SIN4
P100_AN0 P101_AN1 P102_AN2 P103_AN3 P104_AN4_KI0 P105_AN5_KI1 P106_AN6_KI2 P107_AN7_KI3
R597 2.2K NUMLOCK_LED_L
R596 2.2K CAPSLOCK_LED_L
PMU_NUMLOCK_LED_L
PMU_CAPSLOCK_LED_L
CHARGE_LED_L
PMU_POWER_UP_L
SOFT_PWR_ON_L
COMM_RING_DET_L
INT_WATCHDOG_L
KBD_X<0> KBD_X<1> KBD_X<2> KBD_X<3> KBD_X<4> KBD_X<5> KBD_X<6> KBD_X<7>
KBD_Y<0> KBD_Y<1> KBD_Y<2> KBD_Y<3> KBD_Y<4> KBD_Y<5> KBD_Y<6> KBD_Y<7>
KBD_X<8> KBD_X<9> IO_RESET_L KBD_COMMAND_L KBD_CONTROL_L KBD_SHIFT_L KBD_OPTION_L KBD_FUNCTION_L
PMU_INT_L KBD_ID CPU_PLL_STOP_OC SLEEP INT_SUSPEND_ACK_L INT_SUSPEND_REQ_L +3V_PMU_AVCC PMU_CNVSS PMU_BYTE
PMU_INT_ACK_L
CPU_VCORE_HI_OC
INT_RESET_L
MAIN_RESET_L
PMU_INT_NMI
PMU_EPM
INT_PU_RESET_L
PMU_CPU_HRESET_L
PMU_ACK_L
PMU_CLK
PMU_FROM_INT
PMU_TO_INT
PMU_REQ_L
PMU_LID_CLOSED_L
PMU_RESET_BUTTON_L
PMU_NMI_BUTTON_L
TPAD_RXD
TPAD_TXD
SYSTEM_CLK_EN
CPU_CLK_EN
PMU_CHARGE_V
PMU_CHRG_BATT_0
NC (CHARGE_I)
PMU_SLEEP_LED_L
CPU_SMI_L
POWER_VALID
PMU_PME_L
PMU_INT_PROC_SLEEP_REQ_L
PMU_POWERUP_OK
PMU_OOPS
THERM_L_OC
PMU_AC_IN
PMU_AC_DET
PMU_I2C_CLK
PMU_I2C_DATA
PMU_SMB_CLK
PMU_SMB_DATA
PMU_BATT0_DET_L
PMU_BATT1_DET_L_PU
PMU_BATT_DET_L
AC_IN
CLK32K_PMU_XOUT
CLK32K_PMU_XIN
Keep crystal subcircuit close to PMU.
R588 1K
R600 1K
NO STUFF R248 10M
R249 0
CRITICAL Y3 32.768K SM-2
CLK32K_PMU_XOUT_UF
C339 12pF
C340 12pF
Y3'S LOAD CAPACITANCE IS 12.5PF
RP41 10K PMU_EPM
RP41 10K PMU_RESET_BUTTON_L
R261 100K PMU_POWERUP_OK
R591 470K PMU_BATT1_DET_L_PU
R589 470K PMU_BATT_DET_L
RP41 10K PMU_NMI_BUTTON_L
RP41 10K PMU_NMI_L
R584 2.15K PMU_SMB_DATA
R585 2.15K PMU_SMB_CLK
R599 10K PMU_I2C_CLK
R598 10K PMU_I2C_DATA
+3V_SLEEP
R563 10K TPAD_RXD
R564 10K TPAD_TXD
+5V_SLEEP
R576 100K POWER_VALID
R575 10K PMU_PME_L
R562 100K PMU_LID_CLOSED_L
+3V_MAIN
R594 10K PMU_OOPS
R561 100K INT_PU_RESET_L
UNDERVOLTAGE RESET CIRCUIT
R267 1K
+3V_PMU_RESET
C370 0.1uF
U26 MAX6804 SOT143
VCC MR* RSET* GND
PMU_KB_RESET_L
R580 NO STUFF 10M
R581 0
CRITICAL Y4 10.0000M 8X4.5MM-SM
CLK10M_PMU_XOUT_UF
CLK10M_PMU_XOUT
CLK10M_PMU_XIN
C406 12pF
C728 12pF
Keep crystal subcircuit close to PMU.
Y5'S LOAD CAPACITANCE IS 12PF
PART NUMBER | ALTERNATE FOR PART NUMBER | BOM OPTION | REF DES | COMMENTS:
197S0604 | 197S0041 | | Y4 | Alt. for Siward Part
PMU KEYBOARD RESET CIRCUIT
NC7S32 SC70 U20
SOFT_PWR_ON_L
KBD_CONTROL_L
PMU_KB_RESET_IN1
C277 0.1uF
NC7S32 SC70 U25
PMU_KB_RESET_L
NC7S32 SC70 U24
KBD_SHIFT_L
KBD_OPTION_L
PMU_KB_RESET_IN2
KEEP CAP CLOSE TO ALL 3 OR GATES
ADAPTER IDs
ADAPTER | ID RANGE | PIN VOLTAGE
Q11 (65W) | 1.65-2.31V | 2.007-2.066V
A29 (45W) | 2.31-2.97V | 2.558-2.661V
AIRLINE | 0.33-0.99V | 0.589-0.663V
A29 ADAPTER DETECTION
+4.85V_RAW
R592 100K
ADAPTER_DET
R593 100K
PMU_AC_DET
R590 402K
R348 52.3K
C467 0.1uF
R364 100K
A29_DETECT
U33 LMC7211 SM
A29_DET_L
A29_DET_REF
R345 4.7M
R349 127K
Q30 2N7002 SM
PMU
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SIZE D
DRAWING NUMBER 051-6653
REV. C
SCALE NONE
SHT 29 OF 44

DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

CRITICAL
J27
87438-0433
M-RT-SM

+ADAPTER

C35 0.1uF 10% 10V X7R 603-1

R51 20K 1% 1/16W MF 402

GREATER THAN 13.1V DETECT

R40 97.6K 1% 1/16W MF 402
R16 100K 1% 1/16W MF 402
R42 10K 1% 1/16W MF 402
R30 57.6K 1% 1/16W MF 402
R41 1M 5% 1/16W MF 402
R22 470K 5% 1/16W MF 402
R15 10K 5% 1/16W MF 402
C801 0.01uF 20% 16V CERM 402

U1 LMC7211 SM

1V20_REF
AC_DIV
AC_IN
AC_IN_L

Q1 2N7002DW SOT-363

DC INRUSH LIMITER

Q68 SI4435DY SOI
Q69 SI4435DY SOI

R21 330K 1% 1/16W MF 402
C11 0.1uF 10% 50V CERM 805
R29 470K 5% 1/16W MF 402
AC_ENABLE_GATE
AC_ENABLE_L

BACKFEED PROTECTION

+ADAPTER_SW
+ADAPTER_SENSE
BKFD_PROT_GATE
BKFD_PROT_EN_L

R732 47K 5% 1/16W MF 402
R734 68K 5% 1/16W MF 402
C803 0.1uF 10% 16V CERM 402
R77 2.21K 0.1% 1/16W MF 603
C36 0.01uF 20% 50V CERM 603

Q9 2N7002DW SOT-363

PLACE U24 NEXT TO R382

U3 MAX4172 TSSOP
RS+ RS- PG OUT GND NC1 NC2
MAX4172_OUT

+PBUS CURRENT LIMIT

R728 1K 1% 1/16W MF 402
C798 0.1uF 20% 16V CERM 402
IAC_RC_COMP
+3V_PMU
C794 0.1uF 20% 16V CERM 402
R745 42.2K 0.1% 1/16W PF 603
IAC_FB
U55 MC33111 SOT23-5
PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
LTC1625_ITH
R727 10K 1% 1/16W MF 402
DP1 BAS16TW SOT-363
R119 150 1% 1/16W MF 402
1625_COMP
ADAPTER_I_REG
Place close to RS-
C826 0.01uF 20% 50V CERM 603
CURRENT_THRESHOLD
R736 42.2K 0.1% 1/16W PF 603
R738 82.5K 0.1% 1/16W PF 603
R742 51.1K 0.1% 1/16W PF 603
A29_CURRENT_ADJ
OVER_18V_ADJ
Q2 2N7002DW SOT-363
R744 100K 5% 1/16W MF 402
AC_GTR_18V
Q74 2N7002DW SOT-363
A29_DETECT
1772_ACOK_L
Q74 2N7002DW SOT-363
C809 1uF 20% 25V CERM 603

BATTERY SWITCH-OVER CIRCUIT

+24V_PBUS
F5 5AMP-125V SM-2
+BATT_24V_FUSE
CRITICAL
Q6 SI4435DY SOI
R716 47K 5% 1/16W MF 402
BATT_24V_GATE
R717 10K 5% 1/16W MF 402
BATT_24PBUS_EN
DP1 BAS16TW SOT-363
AC_IN_L
R102 158K 1% 1/16W MF 402
AC_IN_L_RC
C118 10uF 20% 6.3V CERM 805
Q9 2N7002DW SOT-363
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

+PBUS
F4 5AMP-125V SM-2
+BATT_14V_FUSE
CRITICAL
Q7 SUD45P03 TO-252
R710 47K 5% 1/16W MF 402
BATT_14V_GATE
R711 10K 5% 1/16W MF 402
DP1 BAS16TW SOT-363
BATT_14PBUS_EN

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

R73 27.4K 1% 1/16W MF 402
R62 10K 1% 1/16W MF 402
R58 10K 1% 1/16W MF 402
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
R74 4.12K 1% 1/16W MF 402
R59 100K 5% 1/16W MF 402
BATTV_HIGH
BATTV_LOW
R75 5.23K 1% 1/16W MF 402
Q4 2N7002DW SOT-363
PMU_CHARGE_V
R733 20K 1% 1/16W MF 402
R731 1K 1% 1/16W MF 402
BATT_LOW
Q71 2N7002DW SOT-363
Q71 2N7002DW SOT-363
R56 1K 1% 1/16W MF 402
R741 100K 5% 1/16W MF 402
CHARGE_DISABLE
Q72 2N7002DW SOT-363
PMU_CHRG_BATT_0
Q72 2N7002DW SOT-363

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R61 0.025 1% 1W MF 2512
R82 4.7 5% 1/16W MF 402
R87 4.7 5% 1/16W MF 402
1772_CSSP
1772_CSSN
R57 100K 1% 1/16W MF 402
D4 1N914 SOT23
R49 12.7K 1% 1/16W MF 402
C67 1uF 20% 25V CERM 1210
C71 0.47uF 20% 25V CERM 1206
C95 0.47uF 20% 25V CERM 1206

U6 MAX1772 QSOP

1772_DCIN	DCIN	CELLS	1772_CELLS
1772_ACIN	ACIN	LDO	
1772_ACOK_L	ACOK	DLOV	1772_DLOV
(+3V_PMU)	RFIN	BST	1772_BST
1772_VCTL	VCTL	DHI	1772_DHI
1772_ICTL	ICTL	LX	1772_LX
1772_ICHG	ICHG	DLO	1772_DLO
1772_IINP	IINP	PGND	(GND)
		CSIP	1772_CSIP
		CSIN	1772_CSIN
1772_CCV	CCV	BATT	
1772_CCI	CCI		
1772_CCS	CCS		
	REF	CLS	GND

R725 33 1% 1/8W MF 1206
D6 1N914 SOT23
1772_BST_ESR
R52 100K 5% 1/16W MF 402
C97 0.1uF 20% 25V CERM 603
R96 4.7 5% 1/16W MF 603
C96 0.1uF 20% 25V CERM 805
CRITICAL
Q70 IRF7805 SM
C112 2.2uF 20% 25V CERM 1812
C117 2.2uF 20% 25V CERM 1812
C113 2.2uF 20% 25V CERM 1812
C115 2.2uF 20% 25V CERM 1812
C116 2.2uF 20% 25V CERM 1812
CRITICAL
L70 10uH SM1
+BATT_RSNS
R715 0.05 1% 1W MF 2512
+BATT_24V_FUSE
D36 MBRS140T3
CRITICAL
Q64 IRF7811W SO-8
NO_STUFF
C853 1000pf 10% 25V X7R 402
C780 4.7uF 20% 25V CERM 1206
C795 4.7uF 20% 25V CERM 1206
C790 4.7uF 20% 25V CERM 1206
C779 33uF 20% 25V ELEC SM1
R720 1 5% 1/16W MF 603
R713 1 5% 1/16W MF 603
C777 4.7uF 20% 25V CERM 1206
C792 4.7uF 20% 25V CERM 1206
C785 4.7uF 20% 25V CERM 1206
XW1 SM

R94 100K 5% 1/16W MF 402
C41 1uF 20% 25V CERM 603
C98 0.1uF 20% 25V CERM 603
C99 0.1uF 20% 25V CERM 603
+BATT_VSNS

R54 10K 1% 1/16W MF 402
R53 4.12K 1% 1/16W MF 402
1772_CLS
R83 1K 1% 1/16W MF 402
C24 0.1uF 10% 16V CERM 402
1772_CCV_RC
C43 0.01uF 20% 50V CERM 402
C42 0.01uF 20% 50V CERM 402
C23 1uF 20% 25V CERM 603
1772_REF
1772_GND

R47 6.34K 1% 1/16W MF 402
A29_CLS_ADJ
Q2 2N7002DW SOT-363
A29_DETECT

C799 0.1uF 20% 16V CERM 402
U57 LMC7211 SM
BATT_LOW
R729 100K 1% 1/16W MF 402
R740 499K 1% 1/16W MF 402
BATT_DIV
1V65_REF
R730 100K 1% 1/16W MF 402
R735 100K 1% 1/16W MF 402
C807 0.047uF 10% 16V CERM 402

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{Q2}) * (V_{ICTL} / V_{REFIN})$

BATTERY CONNECTOR

CRITICAL
J26
87438-0833
M-RT-SM

+BATT_POS (BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG

L5 FERR-EMI-100-OHM SM
L6 FERR-50-OHM SM
L4 FERR-EMI-100-OHM SM
PMU_SMB_CLK
L3 FERR-EMI-100-OHM SM
PMU_SMB_DATA
L2 FERR-50-OHM SM
+BATT

BATTERY CHARGER

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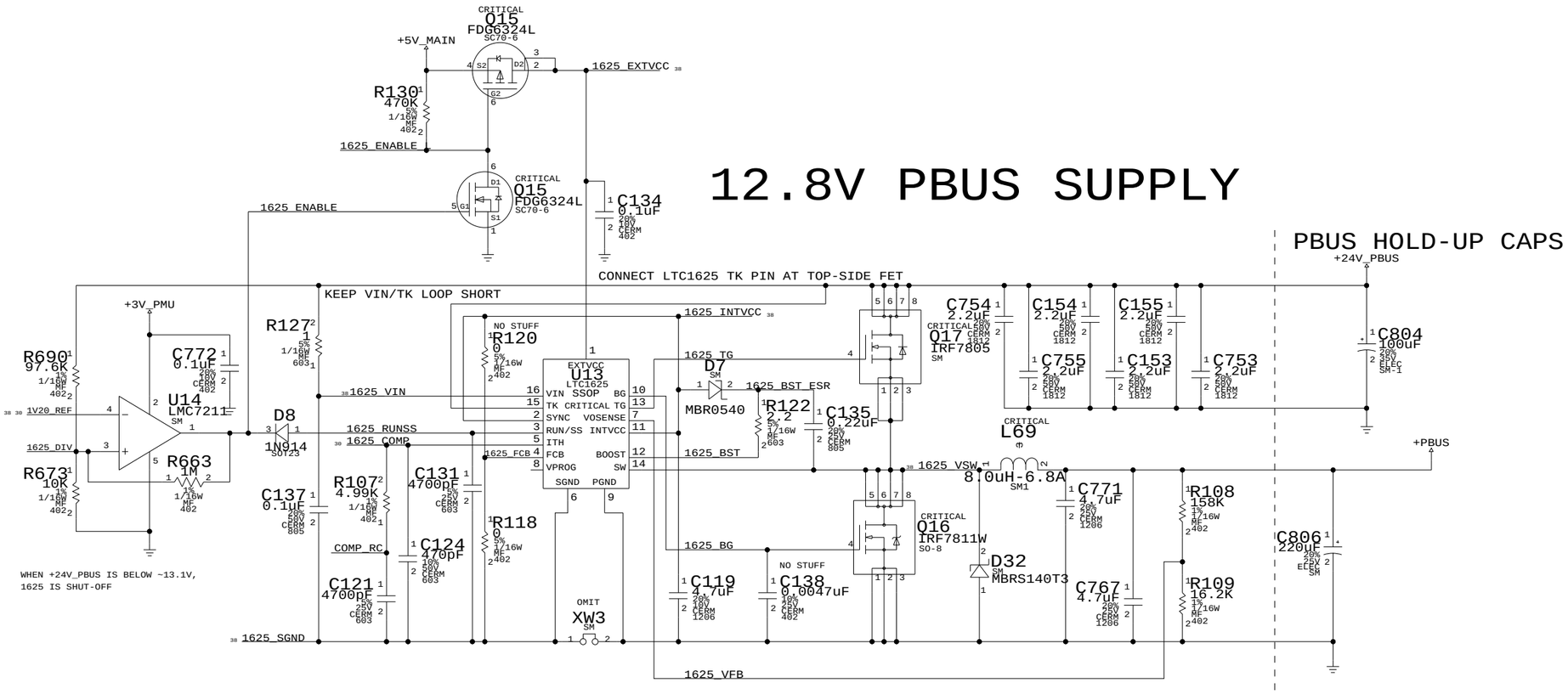
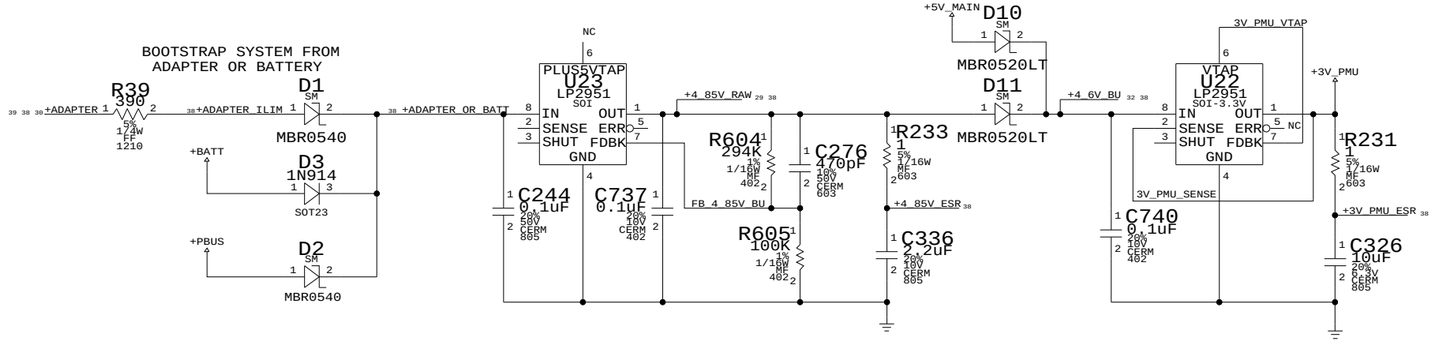
SIZE	DRAWING NUMBER	REV
D	051-6653	C
SCALE: NONE	SHT: 30 OF 44	

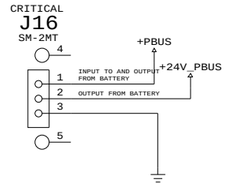
12.8V PBUS SUPPLY



PMU SUPPLY



BACKUP BATTERY



12.8V REGULATOR

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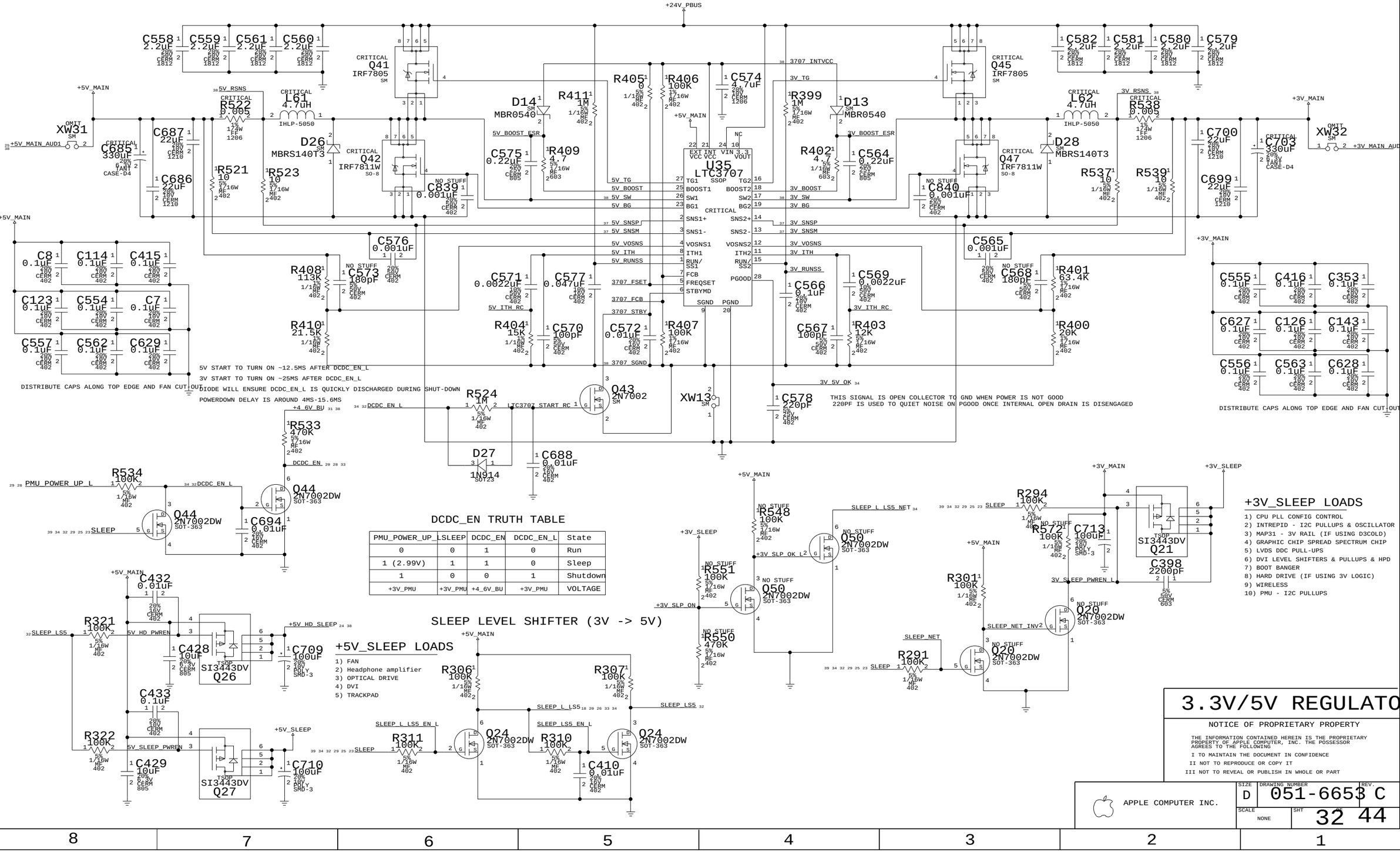
D	051-6653	C
SCALE: NONE	SHT	31 44

3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE

PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

1) FAN
2) Headphone amplifier
3) OPTICAL DRIVE
4) DVI
5) TRACKPAD

+3V_SLEEP LOADS

1) CPU PLL CONFIG CONTROL
2) INTREPID - I2C PULLUPS & OSCILLATOR
3) MAP31 - 3V RAIL (IF USING D3COLD)
4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
5) LVDS DDC PULL-UPS
6) DVI LEVEL SHIFTERS & PULLUPS & HPD
7) BOOT BANGER
8) HARD DRIVE (IF USING 3V LOGIC)
9) WIRELESS
10) PMU - I2C PULLUPS

3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.250V->0.975V 1.50Ghz
1.200V->0.975V 1.33Ghz
(value without offset)

NOTE: When U15 MUX is removed => NO SW Support,
R794,R795,R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S0036	7	CAP,AL,POLY,8.2uF,20%,16V,V CASE,SMD	C51,C52,C77,C78,C91,C92,C111	CRITICAL	

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

Keep trace fat and short!!

Connect MAX1717 GND pin 13
to GND at bottom-side FET

SEL = 0; Y1=A1
SEL = 1; Y1=B1

MAX1717 VID INPUTS ARE 3.3-5V TOLERANT

Note:No stuff R67 to set skip mode of VCore

(R93 CPU_BTR BOM OPTION SEE BOM TABLE)

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * 0.85*(Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)

1.50Ghz 1.280V->0.990V
1.33Ghz 1.220V->0.990V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2003	1	RES,MF,1/16W,2K OHM,1%,0402,SMD	R97	?	CPU_BTR
114S5903	1	RES,MF,1/16W,5.9K OHM,1%,0402,SMD	R93	?	CPU_BTR

ROUTE AS DIFFERENTIAL PAIR

PLACE THIS SHORT AT
PIN OF 100uF CAP
CLOSEST TO CPU

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all
pull-downs are <=1K, A V = B V .

Fmax Test Connections

J7
M-ST-SM-52465-1217

1	VCORE_GNDDIV_TEST	12	VCORE_D0
2	VCORE_GNDSNS_TEST	11	VCORE_D1
3	+3V_PMU_RESET	10	VCORE_D2
4	SOFT_PWR_ON_L	9	VCORE_D3
5	NC (RFU)	8	VCORE_D4
6		7	

VCORE SUPPLY

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SCALE: NONE	SHT 33 OF 44	

1.5V/2.5V SWITCHER

+1_5V_SLEEP LOADS

1) AGP I/O - IF USING D3COLD
2) MAXBUS I/O - IF 1.5V INTERFACE

+1_5V_MAIN LOADS

1) INTREPID CORE

+2_5V_MAIN LOADS

1) MAP31 - FBCORE/FBIO IF USING D3HOT
2) GIGABIT ETHERNET - AVDDL
3) DDR SODIMMS - CORE/IO
4) DDR MUXES

M11 Power Shut down Sequencing

+2_5V_SLEEP LOADS

1) FBCORE/FBIO IF USING D3COLD

DIODE PROVIDE PROVIDE QUICK SHUT-DOWN
POWER DOWN DELAY 1.5MS TO 3.5MS

1.8V SWITCHER

+1_8V_MAIN LOADS

1) INTREPID PLLS

+1_8V_SLEEP LOADS

1) MPC7447 - MAXBUS I/O - IF 1.8V INTERFACE
2) CPU JTAG & MaxBus Pull-ups
3) CPU PLL Config Straps

1.5V/1.8V/2.5V SUPPLIES

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D	051-6653	C
SCALE: NONE	SHT 34 OF 44	

DIGITAL SIGNALS

STUB_LENGTH OF 200 MILS NEEDED WHEN WE CONVERT TO 14.2

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
GROUP 0	I261 MEM_DATA<7..0>	L:S:1602:1700	7	500	(200)			167 MHZ	9 10
	I262 MEM_DQM<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	I263 MEM_DQS<0>	L:S:1602 MIL:1700 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	I264 RAM_DATA_A<7..0>	L:S:1903:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	I265 RAM_DQM_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I266 RAM_DQS_A<0>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I267 RAM_DATA_B<7..0>	L:S:2000:2100	7	500	(200)			167 MHZ	10 11
	I268 RAM_DQM_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I269 RAM_DQS_B<0>	L:S:2000 MIL:2100 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 1	MEM_DATA<15..8>	L:S:1344:1660	7	500	(200)			167 MHZ	9 10
	MEM_DQM<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<1>	L:S:1344 MIL:1660 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<15..8>	L:S:1905:2000	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<1>	L:S:1905 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<15..8>	L:S:2004:2412	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<1>	L:S:2004 MIL:2412 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 2	I270 MEM_DATA<23..16>	L:S:1435:1500	7	500	(200)			167 MHZ	9 10
	I271 MEM_DQM<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	I272 MEM_DQS<2>	L:S:1435 MIL:1500 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	I274 RAM_DATA_A<23..16>	L:S:1707:1800	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	I273 RAM_DQM_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I275 RAM_DQS_A<2>	L:S:1707 MIL:1800 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I277 RAM_DATA_B<23..16>	L:S:1900:2000	7	500	(200)			167 MHZ	10 11
	I276 RAM_DQM_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	I278 RAM_DQS_B<2>	L:S:1900 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 3	MEM_DATA<31..24>	L:S:1233:1485	7	500	(200)			167 MHZ	9 10
	MEM_DQM<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<3>	L:S:1233 MIL:1485 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<31..24>	L:S:1700:2165	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<3>	L:S:1700 MIL:2165 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<25..24>	L:S:1907:2356	7	500	(200)			167 MHZ	10 11
	I279 RAM_DATA_B<26>	L:S:1907 MIL:2356 MIL	7		(200)			167.0 MHz:::	10 11
	I280 RAM_DATA_B<31..27>	L:S:1907:2356	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<3>	L:S:1907 MIL:2356 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 4	MEM_DATA<39..32>	L:S:1915:2000	7	500	(200)			167 MHZ	9 10
	MEM_DQM<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<4>	L:S:1915 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<39..32>	L:S:1205:1387	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
DDR RAM	RAM_DQS_A<4>	L:S:1205 MIL:1387 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<39..32>	L:S:1404:1686	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<4>	L:S:1404 MIL:1686 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 5	MEM_DATA<47..40>	L:S:1719:1893	7	500	(200)			167 MHZ	9 10
	MEM_DQM<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<5>	L:S:1719 MIL:1893 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<47..40>	L:S:1607:1898	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<5>	L:S:1607 MIL:1898 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<47..40>	L:S:1716:2102	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<5>	L:S:1716 MIL:2102 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 6	MEM_DATA<55..48>	L:S:2101:2170	7	500	(200)			167 MHZ	9 10
	MEM_DQM<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<6>	L:S:2101 MIL:2170 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<55..48>	L:S:1204:1357	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<6>	L:S:1204 MIL:1357 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<55..48>	L:S:1400:1546	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<6>	L:S:1400 MIL:1546 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
GROUP 7	MEM_DATA<63..56>	L:S:1903:2000	7	500	(200)			167 MHZ	9 10
	MEM_DQM<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	MEM_DQS<7>	L:S:1903 MIL:2000 MIL	7	500.0000	(200)			167.0 MHz:::	9 10
	RAM_DATA_A<63..56>	L:S:1611:1696	7	500	(200)	TOTAL LENGTH CONTROLLED BY SPREADSHEET		167 MHZ	10 11
	RAM_DQM_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_A<7>	L:S:1611 MIL:1696 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DATA_B<63..56>	L:S:1809:1887	7	500	(200)			167 MHZ	10 11
	RAM_DQM_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
	RAM_DQS_B<7>	L:S:1809 MIL:1887 MIL	7	500.0000	(200)			167.0 MHz:::	10 11
ADDR	MEM_ADDR<12..0>	L:S::500	4					83 MHZ	9
	RAM_ADDR<12..0>	L:S:2000:3000	10		(200)				9 11
	MEM_BA<1..0>	L:S::500	4						9
	RAM_BA<1..0>	L:S:2000:3300	8		(200)				9 11
CONTROL	MEM_CS_L<3..0>	L:S::500	4						9
	RAM_CS_L<3..0>	L:S:2500:3200	7		(200)				9 11
	MEM_CKE<3..0>	L:S::500	4						9
	RAM_CKE<3..0>	L:S:2500:3200	7		(200)				9 11
	MEM_RAS_L	L:S::500 MIL	4						9
	RAM_RAS_L	L:S:2000 MIL:4100 MIL	7		(200)				9 11
	MEM_CAS_L	L:S::500 MIL	4						9
	RAM_CAS_L	L:S:2000 MIL:4100 MIL	7		(200)				9 11
	MEM_WE_L	L:S::500 MIL	4						9
	RAM_WE_L	L:S:2000 MIL:3100 MIL	8		(200)				9 11
	MEM_MUXSEL_MSB	L:S:1700 MIL:3000 MIL	8						9 10
	MEM_MUXSEL_LSB	L:S:1700 MIL:3000 MIL	7						9 10

PRIORITY: 2
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE
EXPOSED ROUTES
MINIMIZE VIAS

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME	PROPAGATION_DELAY	MATCHED_DELAY	MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF	L:S::150 MIL					10 MIL SPACING	167.0 MHz:::	8
	SYSCLK_CPU	L:S:2650 MIL:2750 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	5 8
	INT_CPUFB_OUT	L:S::150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_SHORT	L:S:700 MIL:850 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_OUT_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_IN_NORM	L:S:500 MIL:600 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_LONG	L:S:1050 MIL:1150 MIL		5	250.0000		10 MIL SPACING	167.0 MHz:::	8
	INT_CPUFB_IN	L:S:700 MIL:800 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	8
	SYSCLK_DDRCLK_A0_UF	L:S:300 MIL:350 MIL	DDRCLK_A0_UF SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0_L_UF	L:S:300 MIL:350 MIL	DDRCLK_A0_UF SYSCLK_DDRCLK_A0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_UF	L:S:300 MIL:350 MIL	DDRCLK_A1_UF SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A1_L_UF	L:S:300 MIL:350 MIL	DDRCLK_A1_UF SYSCLK_DDRCLK_A1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_UF	L:S:300 MIL:350 MIL	DDRCLK_B0_UF SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B0_L_UF	L:S:300 MIL:350 MIL	DDRCLK_B0_UF SYSCLK_DDRCLK_B0_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_UF	L:S:300 MIL:350 MIL	DDRCLK_B1_UF SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_B1_L_UF	L:S:300 MIL:350 MIL	DDRCLK_B1_UF SYSCLK_DDRCLK_B1_UF:G:L:S:0 MIL:25 MIL	4		(200)	10 MIL SPACING	167.0 MHz:::	9
	SYSCLK_DDRCLK_A0	L:S:2900 MIL:3000 MIL	DDRCLK_A0 SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A0_L	L:S:2900 MIL:3000 MIL	DDRCLK_A0 SYSCLK_DDRCLK_A0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1	L:S:2900 MIL:3000 MIL	DDRCLK_A1 SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_A1_L	L:S:2900 MIL:3000 MIL	DDRCLK_A1 SYSCLK_DDRCLK_A1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0	L:S:3100 MIL:3200 MIL	DDRCLK_B0 SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B0_L	L:S:3100 MIL:3200 MIL	DDRCLK_B0 SYSCLK_DDRCLK_B0:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1	L:S:3100 MIL:3200 MIL	DDRCLK_B1 SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	SYSCLK_DDRCLK_B1_L	L:S:3100 MIL:3200 MIL	DDRCLK_B1 SYSCLK_DDRCLK_B1:G:L:S:0 MIL:25 MIL	7	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	9 11
	I260 INT_REF_CLK_OUT_UF	L:S::400 MIL				(200)	10 MIL SPACING	49.92 MHz:::	14
	I256 INT_REF_CLK_OUT	L:S:1000 MIL:1150 MIL		5	250.0000	(200)	10 MIL SPACING	49.92 MHz:::	14
	I257 INT_REF_CLK_IN	L:S:1900 MIL:2000 MIL		5	250.0000	(200)	10 MIL SPACING	167.0 MHz:::	14
	CLK66M_GPU_AGP_UF	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::	12
	CLK66M_GPU_AGP	L:S:1800 MIL:1900 MIL		6	400.0000	(200)	10 MIL SPACING	66.00 MHz:::	12 19
	INT_AGP_FB_OUT	L:S::150 MIL				(200)	10 MIL SPACING	66.00 MHz:::	12
	INT_AGP_FB_IN	L:S:1450 MIL:1550 MIL		6	500.0000	(200)	10 MIL SPACING	66.00 MHz:::	12
	CLK33M_CBUS_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	CLK33M_CBUS	L:S:5000 MIL:6000 MIL		9	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 18
	CLK33M_AIRPORT_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	CLK33M_AIRPORT	L:S:9500 MIL:10500 MIL		6	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 24 39
	I259 CLK33M_NEC_UF	L:S::250 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	I258 CLK33M_NEC	L:S:4000 MIL:6000 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12 17
	INT_PCI_FB_OUT	L:S::300 MIL				(200)	10 MIL SPACING	33.00 MHz:::	12
	INT_PCI_FB_IN	L:S:6500 MIL:7500 MIL		7	500.0000	(200)	10 MIL SPACING	33.00 MHz:::	12
M10 & OSC	ATI_CLK27M_OSC	L:S::400 MIL		5		(200)	10 MIL SPACING		19
	ATI_CLK27M_OSC_SS	L:S::400 MIL		5		(200)	10 MIL SPACING		19
	ATI_CLK27M_IN	L:S::200 MIL		5		(200)	10 MIL SPACING		19 20
	ATI_SSCLK_UF	L:S::200 MIL		5		(200)	10 MIL SPACING		19
	ATI_SSCLK_IN	L:S::1800 MIL		5	500.0000	(200)	10 MIL SPACING		19 20
CRYSTALS	CLK18M_INT_XIN	L:S:1400 MIL:1500 MIL					10 MIL SPACING		14
	CLK18M_INT_XOUT	L:S:1250 MIL:1350 MIL					10 MIL SPACING		14
	CLK18M_XTAL_IN	L:S::300 MIL					10 MIL SPACING		14
	CLK18M_INT_EXT	L:S::400 MIL					10 MIL SPACING		14
SOUND	INT_I2S0_SND_MCLK			6	500.0000	(200)	10 MIL SPACING		14 25 39
ETHERNET	CLKENET_PHY_RX	L:S::300 MIL				(200)		125.0 MHz:::	26
	CLKENET_LINK_RX	L:S:8000 MIL:9000 MIL		6	800.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_GBE_REF	L:S::300 MIL				(200)		125.0 MHz:::	26
	CLKENET_LINK_GBE_REF	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
	CLKENET_PHY_TX	L:S::300 MIL				(200)		25.00 MHz:::	26
	CLKENET_LINK_TX	L:S:8000 MIL:9000 MIL		6	500.0000	(200)	10 MIL SPACING	25.00 MHz:::	13 26
	CLKENET_LINK_GTX	L:S::300 MIL				(200)		125.0 MHz:::	13
	CLKENET_PHY_GTX	L:S:8000 MIL:9000 MIL		6	600.0000	(200)	10 MIL SPACING	125.0 MHz:::	13 26
FIREWIRE	CLKFW_PHY_PCLK	L:S::300 MIL				(200)		49.15 MHz:::	27
	CLKFW_LINK_PCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::	13 27
	CLKFW_PHY_LCLK	L:S:7500 MIL:8000 MIL		5	500.0000	(200)	10 MIL SPACING	49.15 MHz:::	13 27
	CLKFW_LINK_LCLK	L:S::300 MIL				(200)		49.15 MHz:::	13
	FW_XI	L:S::500 MIL				(200)	10 MIL SPACING	98.03 MHz:::	27
	FW_OSC	L:S::300 MIL				(200)	10 MIL SPACING	98.03 MHz:::	27

PRIORITY: 1
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9
GOAL: MINIMIZE EXPOSURE ON LONG NETS

SIGNAL CONSTRAINTS - PAGE 1

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APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6653 | REV. C
SCALE NONE | SHT 35 OF 44

DIGITAL SIGNALS

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_ADDR<0..31>	L:S:1500:3100	7		(250)		TRUE	83 MHZ	5 8
	CPU_ARTRY_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_BG_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_BR_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_CI_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_DATA<0..31>	L:S:1100:2700	7		(250)		TRUE	83 MHZ	6 8
	CPU_DATA<32..63>	L:S:1100:2700	8		(250)			83 MHZ	6 8
	CPU_DBG_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_DTI<0..2>	L:S:1500:2950	7		(250)				5 8
	CPU_DRDY_L	L:S:1500 MIL:3200 MIL	7		(250)				5 8
	CPU_GBL_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_HIT_L	L:S:1500 MIL:2800 MIL	7		(250)				5 8
	CPU_QACK_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_QREQ_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TA_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TBST_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TEA_L	L:S:1500 MIL:3000 MIL	7		(250)				5 8
	CPU_TS_L	L:S:1500 MIL:2700 MIL	7		(250)				5 8
	CPU_TSIZ<0..2>	L:S:1500:3500	7		(250)				5 8
	CPU_TT<0..4>	L:S:1500:3400	7		(250)				5 8
	CPU_WT_L	L:S:1500 MIL:3100 MIL	7		(250)				5 8

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

STUB_LENGTH OF 250 MILS NEEDED WHEN DESIGN SWITCHED TO 14.2

Temporary Area for TMDS/DVO signal constraints

ALL TMDS GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND HAVE SAME WIDTH SPACING RULE AS OTHER TMDS SIGNALES

T23	GPU_TMDS_CLKN	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING 5	19 20
T23	GPU_TMDS_CLKP	GPU_CLKTMDS	GPUTMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING 5	19 20
T23	GPU_TMDS_DN<0>	GPU_TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T23	GPU_TMDS_DP<0>	GPU_TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T23	GPU_TMDS_DN<1>	GPU_TMDS_D1		600.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T23	GPU_TMDS_DP<1>	GPU_TMDS_D1		600.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T23	GPU_TMDS_DN<2>	GPU_TMDS_D2		830.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T23	GPU_TMDS_DP<2>	GPU_TMDS_D2		830.0000	100 OHM SPACING 100 OHM SPACING 8	19 20
T24	SI_TMDS_CLKN	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING 5	19
T24	SI_TMDS_CLKP	SI_CLKTMDS	SITMDS:G:L:S:0 MIL:50 MIL		100 OHM SPACING 100 OHM SPACING 5	19
T24	SI_TMDS_DN<0>	SI_TMDS_D0			100 OHM SPACING 100 OHM SPACING 8	19
T24	SI_TMDS_DP<0>	SI_TMDS_D0			100 OHM SPACING 100 OHM SPACING 8	19
T24	SI_TMDS_DN<1>	SI_TMDS_D1			100 OHM SPACING 100 OHM SPACING 8	19
T24	SI_TMDS_DP<1>	SI_TMDS_D1			100 OHM SPACING 100 OHM SPACING 8	19
T24	SI_TMDS_DN<2>	SI_TMDS_D2			100 OHM SPACING 100 OHM SPACING 8	19
T24	SI_TMDS_DP<2>	SI_TMDS_D2			100 OHM SPACING 100 OHM SPACING 8	19

ALL THE DVOD GROUP SIGNALS ROUTE AT LAYER 4 OR 7 AND ROUTE AS STANDARD 50OHM SIGNALS AT 4 MILS

T26	ATI_DVOD<11..0>	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610		19 20
T26	ATI_DVOD_DE	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T26	ATI_DVO_HSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T26	ATI_DVO_VSYNC	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000		19 20
T26	ATI_DVO_CLKP	ATIDVOD:G:L:S:0 MIL:50 MIL	6	610.0000	165.0 MHz:::	19 20
T25	GPU_DVOD<11..0>	GPUDVOD:G:L:S:0 MIL:50 MIL	6	700		19
T25	GPU_DVOD_DE	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T26	GPU_DVO_HSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T26	GPU_DVO_VSYNC	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000		19
T26	GPU_DVO_CLKP	GPUDVOD:G:L:S:0 MIL:50 MIL	6	500.0000	165.0 MHz:::	19

T28	TMDS_CONN_CLKN	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING 4	22 39
T28	TMDS_CONN_CLKP	CLKCONN_TMDS	TMDS_CONN:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 100 OHM SPACING 4	22 39
T27	TMDS_CONN_DN<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING 4	22
T27	TMDS_CONN_DP<0>	CONN_TMDS_D0		500.0000	100 OHM SPACING 100 OHM SPACING 4	22
T27	TMDS_CONN_DN<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING 100 OHM SPACING 4	22
T27	TMDS_CONN_DP<1>	CONN_TMDS_D1		500.0000	100 OHM SPACING 100 OHM SPACING 4	22
T27	TMDS_CONN_DN<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING 4	22
T27	TMDS_CONN_DP<2>	CONN_TMDS_D2		500.0000	100 OHM SPACING 100 OHM SPACING 4	22

SIGNAL CONSTRAINTS - PAGE 1

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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 36 OF 44	

Digital Signals (cont'd)

GROUP	SIG_NAME	PROPAGATION_DELAY	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM
AGP	AGP_AD<15..0>	L:S:1050:1450	7					66 MHZ
AGP BYTES 0-1	AGP_CBE<1..0>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<0>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
AGP BYTES 2-3	AGP_AD<31..16>	L:S:1050:1450	7					66 MHZ
	AGP_CBE<3..2>	L:S:1050:1450	7					66 MHZ
	AGP_AD_STB<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
	AGP_AD_STB_L<1>	L:S:1050 MIL:1450 MIL			(250)	8 MIL SPACING		133.0 MHZ
AGP SIDEBAND	AGP_SBA<7..0>	L:S:1050:1450	7					66 MHZ
	AGP_SB_STB	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ
	AGP_SB_STB_L	L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING		66.00 MHZ
AGP CONTROL	AGP_FRAME_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_IRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_TRDY_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_DEVSEL_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_STOP_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_PAR	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_REQ_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_GNT_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
	AGP_RBF_L	L:S:1250 MIL:1950 MIL						66.00 MHZ
PCI	PCI_AD<31..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_CBE<3..0>	L:S:6000:12500				MIN_DAISY_CHAIN		33 MHZ
	PCI_FRAME_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_IRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_TRDY_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_DEVSEL_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_STOP_L	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
	PCI_PAR	L:S:6000 MIL:12500 MIL				MIN_DAISY_CHAIN		33.00 MHZ
ULTRA ATA-100	UIDE_DATA<15..8>	L:S::710			(200)			100 MHZ
	UIDE_DATA<7>	U51_V1:RP19_3::600 MIL			(200)			100.0 MHZ
	UIDE_DATA<6..0>	L:S::600			(200)			100 MHZ
	UIDE_ADDR<2..0>	L:S::650			(200)			100 MHZ
	UIDE_RST_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOW_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_DIOR_L	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_DMACK_L	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_CS0_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_CS1_L	L:S::500 MIL			(200)			100.0 MHZ
	UIDE_DMARQ	L:S::400 MIL			(200)			100.0 MHZ
	UIDE_IOCHRDY	L:S::600 MIL		10 MIL SPACING	(200)			100.0 MHZ
	UIDE_INTRQ	L:S::400 MIL			(200)			100.0 MHZ
	HD_DATA<15..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_ADDR<2..0>	L:S:5000:6500	7		(200)			100 MHZ
	HD_RESET_L	L:S:4000 MIL:6000 MIL			(200)			100.0 MHZ
	HD_DIOW_L	L:S:3000 MIL:5200 MIL			(200)			100.0 MHZ
	HD_DIOR_L	L:S:6100 MIL:6150 MIL		10 MIL SPACING	(200)			100.0 MHZ
	HD_DMACK_L	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ
	HD_CS0_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ
	HD_CS1_L	L:S:3000 MIL:6000 MIL			(200)			100.0 MHZ
	HD_DMARQ	L:S:4500 MIL:6000 MIL			(200)			100.0 MHZ
	HD_IOCHRDY	L:S:6200 MIL:6300 MIL		10 MIL SPACING	(200)			100.0 MHZ
	HD_INTRQ	L:S:3000 MIL:5000 MIL						100.0 MHZ
EIDE INTREPID	EIDE_DATA<15..0>	L:S::850						33 MHZ
	EIDE_ADDR<2..0>	L:S::850						33 MHZ
	EIDE_CS0_L	L:S::850 MIL						33.00 MHZ
	EIDE_CS1_L	L:S::850 MIL						33.00 MHZ
	EIDE_RD_L	L:S::500 MIL						33.00 MHZ
	EIDE_WR_L	L:S::500 MIL						33.00 MHZ
	EIDE_IOCHRDY	L:S::500 MIL						33.00 MHZ
	EIDE_INT	L:S::500 MIL						33.00 MHZ
	EIDE_RST_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMACK_L	L:S::500 MIL						33.00 MHZ
	EIDE_DMARQ	L:S::500 MIL						33.00 MHZ
OPTICAL	EIDE_OPTICAL_DATA<15..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_ADDR<2..0>	L:S:4000:6000						33 MHZ
	EIDE_OPTICAL_CS0_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_CS1_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_READ_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_WR_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_IOCHRDY	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_INT	L:S:5000 MIL:7000 MIL						33.00 MHZ
	EIDE_OPTICAL_RST_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMAACK_L	L:S:4500 MIL:6500 MIL						33.00 MHZ
	EIDE_OPTICAL_DMA_RQ	L:S:4500 MIL:6500 MIL						33.00 MHZ
ETHERNET MII	ENET_LINK_RXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_RX_DV	L:S:8000 MIL:9000 MIL						
	ENET_RX_ER	L:S:8000 MIL:9000 MIL						
	ENET_PHY_TXD<7..0>	L:S:8000:9000	7	(400)		(400)		
	ENET_LINK_TXD<7..0>	L:S::600						
	ENET_PHY_TX_ER	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_ER	L:S::400 MIL						
	ENET_PHY_TX_EN	L:S:8000 MIL:9000 MIL						
	ENET_LINK_TX_EN	L:S::400 MIL						
	ENET_MDIO	L:S:8000 MIL:9000 MIL						
	ENET_MDC	L:S:8000 MIL:9000 MIL						
	ENET_COL	L:S:8000 MIL:9000 MIL						
	ENET_CRS	L:S:8000 MIL:9000 MIL						
FIREWIRE MII	FW_LINK_DATA<7..0>	L:S:2700:3500	7	(400)		(400)		
	FW_PHY_DATA<7..0>	L:S:4700:5500	7	(400)		(400)		
	FW_LINK_CNTL<1..0>	L:S:9000:10000						
	FW_PHY_CNTL<1..0>	L:S::300						
	FW_LINK_LREQ	L:S::300 MIL						
	FW_PHY_LREQ	L:S:8500 MIL:9500 MIL						
	FW_PINT	L:S:8500 MIL:9500 MIL						

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

PRIORITY: 4
PRIMARY LAYERS: 9
SECONDARY LAYERS: 4,7
GOAL: MINIMIZE TH VIAS

PRIORITY: 7
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 6
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 8
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

PRIORITY: 5
PRIMARY LAYERS: 4,7
SECONDARY LAYERS: 2,9

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	RELATIVE_PROPAGATION_DELAY	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS
FIREWIRE Zo = 110	FW_TPI0N	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPI0P	FW_TPI0	FW_TPI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0N	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPO0P	FW_TPO0	FW_TPO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0N	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPBI0P	FW_TPBI0	FW_TPBI0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0N	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPAO0P	FW_TPAO0	FW_TPAO0:G:L:S:0 MIL:5 MIL	500.0000	110 OHM SPACING	
	FW_TPA1N	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPA1P	FW_TPA1	FW_TPA1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1N	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPB1P	FW_TPB1	FW_TPB1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1N	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPI1P	FW_TPI1	FW_TPI1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1N	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
	FW_TPO1P	FW_TPO1	FW_TPO1:G:L:S:0 MIL:4%	500.0000	110 OHM SPACING	
ETHERNET Zo = 100	MDI_P<0>	ENET_MDI0	ENET_MDI0:G:U43.29:J23.1:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<0>	ENET_MDI0	ENET_MDI0:G:U43.31:J23.2:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<1>	ENET_MDI1	ENET_MDI1:G:U43.33:J23.3:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<1>	ENET_MDI1	ENET_MDI1:G:U43.34:J23.4:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<2>	ENET_MDI2	ENET_MDI2:G:U43.39:J23.7:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<2>	ENET_MDI2	ENET_MDI2:G:U43.41:J23.8:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_P<3>	ENET_MDI3	ENET_MDI3:G:U43.42:J23.9:0 MIL:100 MIL		ENET 11 MIL SPACING	
	MDI_M<3>	ENET_MDI3	ENET_MDI3:G:U43.43:J23.10:0 MIL:100 MIL		ENET 11 MIL SPACING	
LVDS Zo = 100 LOWER	CLKLVDS_LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	
	CLKLVDS_LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	
	LVDS_L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
UPPER	CLKLVDS_UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	
	CLKLVDS_UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING 4	
	LVDS_U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2N	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
	LVDS_U2P	LVDS_U2	LVDS:G:L:S:0 MIL:110 MIL	500.0000	100 OHM SPACING	
TMDS Zo = 100	TMDS_CLKN	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 5	
	TMDS_CLKP	CLKTMDS	TMDS:G:L:S:0 MIL:50 MIL	500.0000	100 OHM SPACING 5	
	TMDS_DN<0>	TMDS_D0		500.0000	100 OHM SPACING 8	
	TMDS_DP<0>	TMDS_D0		500.0000	100 OHM SPACING 8	
	TMDS_DN<1>	TMDS_D1		500.0000	100 OHM SPACING 8	
	TMDS_DP<1>	TMDS_D1		500.0000	100 OHM SPACING 8	
	TMDS_DN<2>	TMDS_D2		500.0000	100 OHM SPACING 8	
	TMDS_DP<2>	TMDS_D2		500.0000	100 OHM SPACING 8	
	ATI_TMDS_CLKN	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 5	
	ATI_TMDS_CLKP	ATI_CLKTMDS	ATITMDS:G:L:S:0 MIL:50 MIL	200.0000	100 OHM SPACING 5	
	ATI_TMDS_DN<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING 8	
	ATI_TMDS_DP<0>	ATI_TMDS_D0		200.0000	100 OHM SPACING 8	
	ATI_TMDS_DN<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING 8	
	ATI_TMDS_DP<1>	ATI_TMDS_D1		200.0000	100 OHM SPACING 8	
	ATI_TMDS_DN<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING 8	
	ATI_TMDS_DP<2>	ATI_TMDS_D2		500.0000	100 OHM SPACING 8	
USB 1.1 Zo = 90	USB_DEM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DEP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFM	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	USB_DFP	USB_DF	USB_DF:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
USB 2.0 Zo = 90	BT_USB_DM	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	BT_USB_DP	BT_USB_D	BT_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DM	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	MODEM_USB_DP	MODEM_USB_D	MODEM_USB:G:L:S:0 MIL:200 MIL		5.6 MIL SPACING	
	NEC_USB_DAM	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DAP	USB_D1	USB_D1:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBM	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
	NEC_USB_DBP	USB_D2	USB_D2:G:L:S:0 MIL:20 MIL	500.0000	90 OHM SPACING	
POWER SUPPLIES	1772_CSSN	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSSP	1772_CSS	1772_CSS:G:L:S:0 MIL:100 MIL			
	1772_CSIN	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	1772_CSIP	1772_CSI	1772_CSI:G:L:S:0 MIL:100 MIL			
	3V_SNSM	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	3V_SNSP	3V_SNS	3V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSM	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
	5V_SNSP	5V_SNS	5V_SNS:G:L:S:0 MIL:100 MIL			
THERMOSTAT	THERM1_DM		THERM1:G:L:S:0 MIL:100 MIL			
	THERM1_DP		THERM1:G:L:S:0 MIL:100 MIL			
	THERM2_DM		THERM2:G:L:S:0 MIL:100 MIL			
	THERM2_DP		THERM2:G:L:S:0 MIL:100 MIL			
	THERM1_M_DM	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_M_DP	THERM1_MAIN	THERM1_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DM	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM2_M_DP	THERM2_MAIN	THERM2_MAIN:G:L:S:0 MIL:100 MIL			
	THERM1_A_DM	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM1_A_DP	THERM1_ALT	THERM1_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DM	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			
	THERM2_A_DP	THERM2_ALT	THERM2_ALT:G:L:S:0 MIL:100 MIL			

PRIORITY: 3
PRIMARY LAYERS: 4,7 FOR CONTROLLED IMPEDANCE DIFF PAIRS
SECONDARY LAYERS: 2,9 FOR UNCONTROLLED IMPEDANCE DIFF PAIRS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3MIL (TRACE WIDTH)
S = 11MIL (TRACE SEPERATION)
H = 16.8MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 106.2 OHMS
Zo(single) = 55.4 OHMS

Clear adjacent power plane!
Zo will be lower due to asymmetric stackup.

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.1MIL (TRACE WIDTH)
S = 4.9MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 94 OHMS
Zo(single) = 50 OHMS

LAYERS 4 OR 7
Er = 4.3 (DIELECTRIC CONSTANT)
W = 3.9MIL (TRACE WIDTH)
S = 5.6MIL (TRACE SEPERATION)
H = 9.6MIL (DIST BETW PLANES)
T = 0.6MIL (TRACE THICKNESS)

Zo(diff) = 89.8 OHMS
Zo(single) = 46.6 OHMS

LAYERS 2 OR 9

SIGNAL CONSTRAINTS - PAGE 2

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SIZE D | DRAWING NUMBER 051-6653 | REV. C

SCALE NONE | SHT 37 OF 44

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23 39
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 31 39
	L631 +ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30 38
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	30
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		30
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	30
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		30
PMU	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		30
	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		29 31
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		31 32
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		31
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		31
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 29
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 32
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+14V_INV	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22 39
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
AUDIO	L335 +5V_MAIN_AUD	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	L336 +3V_MAIN_AUD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 32
	L338 AUD_GND	VOLTAGE=0V	MIN_LINE_WIDTH=50		25
FAN	L339 +FAN_PWR	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FAN1_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	FAN2_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39

I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	IN	
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND1				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND2				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND3				
	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	IN	
	CHGND4				

ENET_CTAP_CHGND VOLTAGE=0V MIN_LINE_WIDTH=25 MIN_NECK_WIDTH=12

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 33 39
	CPU_AVDD	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 33
	L562 CPU_AVDD_VIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	L563 CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	L533 +2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 19
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	VIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
AIRPORT	+3V_AIRPORT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
CARDBUS	L585 +3V_SLEEP_PCCARD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19 20 39
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 19 20 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 21
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	19 20 21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+2_5V_GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	L534 +2_5V_SLEEP_NECK1	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		20
	L534 +3V_SLEEP_NECK	VOLTAGE=3V	MIN_LINE_WIDTH=10		34
	L534 +1_5V_AGP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	L535 +1_8V_PVDD_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		20
	L535 GPU_VCORE_NECK	VOLTAGE=1.2V	MIN_LINE_WIDTH=10		20
	L535 +GPU_VDD15_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		20
	L535 +2_5V_SLEEP_NECK2	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		34
	L535 +1_8V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		34
	L535 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		34
	L536 +1_8V_ATI_TPVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	L536 +1_8V_GPU_TP_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
ETHERNET 88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
NEC USB2.0	L541 +3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	L541 NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	17
FW	L542 LM2594_IN	VOLTAGE=33V	MIN_LINE_WIDTH=40	MIN_NECK_WIDTH=12	27
	L543 +FW_PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	L544 +FW_AMP_SENSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	27 28
	L545 +FW_PWR1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 39
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27 28
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	L541 FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28
	L585 FW_VDD_ON	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1625_VSW	VOLTAGE=14V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+PBUS_JUMPER	VOLTAGE=14V	MIN_LINE_WIDTH=10		
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		31
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	30 31
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+5V_MAIN_JUMPER	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+3V_MAIN_JUMPER	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	2_5V_LX_F	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
1.65V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		34
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	34
	1_5V_LX_F	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		34
	2_5V_ILIM		MIN_LINE_WIDTH=8		34
	MAX1715_TON		MIN_LINE_WIDTH=8		34
	MAX1715_SKIP		MIN_LINE_WIDTH=8		34
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		34
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	33
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	33
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	33
	VCORE_ILIM		MIN_LINE_WIDTH=8		33
	VCORE_REF		MIN_LINE_WIDTH=8		33
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		33
	VCORE_CC		MIN_LINE_WIDTH=8		33
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33 39
	VCORE_TIME		MIN_LINE_WIDTH=8		33
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 33
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		33
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		33
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		33
	L431 VCORE_GNDA	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	20
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	20
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	20
	GPU_VCORE_SW_F	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	
	1778_ION		MIN_LINE_WIDTH=8		20
	1778_ITH		MIN_LINE_WIDTH=8		20
	1778_ITH_RC		MIN_LINE_WIDTH=8		20
	1778_VFB		MIN_LINE_WIDTH=8		20 39
	1778_FCB		MIN_LINE_WIDTH=8		20
	1778_VRNG		MIN_LINE_WIDTH=8		20
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	34
	1_8V_SW_F	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_VFB		MIN_LINE_WIDTH=8		34
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		34
	LTC3411_ITH		MIN_LINE_WIDTH=8		34
	LTC3411_SYNC		MIN_LINE_WIDTH=8		34
	LTC3411_SHDN		MIN_LINE_WIDTH=8		34
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
CY28512D LMU CONN	L368 +3V_MAIN_SSCG	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	L368 +3V_MAIN_LMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
OPT DRIVER	L367 +5V_SLEEP_OPT	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
SCAN/TEST	JTAG_ASIC_TMS	TRUE			13 26
	JTAG_ASIC_TDI	TRUE			13
	JTAG_ASIC_TDO_TP	TRUE			26
	JTAG_ASIC_TCK	TRUE			13 26
	JTAG_ASIC_TRST_L	TRUE			13 26
	CPU_CHKSTP_OUT_L	TRUE			5
	CPU_SRESET_L	TRUE			5
	CPU_HRESET_L	TRUE			5 6 7
	JTAG_CPU_TMS	TRUE			5 6
	JTAG_CPU_TDI	TRUE			5 6
	JTAG_CPU_TDO_TP	TRUE			5
	JTAG_CPU_TCK	TRUE			5 6
	JTAG_CPU_TRST_L	TRUE			5 6
	INT_JTAG_TEI	TRUE			13
	INT_TST_MONIN_PD	TRUE			13
	INT_TST_MONOUT_TP	TRUE			13
	INT_TST_PLLEN_PD	TRUE			13
INT I2C	INT_I2C_CLK0	TRUE			6 11 13 23
	INT_I2C_DATA0	TRUE			6 11 13 23
	INT_I2C_CLK1	TRUE			13 14 25
	INT_I2C_DATA1	TRUE			13 14 25
PWR/GND	+PBUS	TRUE			38
	+24V_PBUS	TRUE			38
	GPU_VCORE	TRUE			19 20 38
	1778_VFB	TRUE			20 38
	CPU_VCORE_SLEEP	TRUE			5 6 33 38
	VCORE_FB	TRUE			33 38
	+1_8V_MAIN	TRUE			38
	+2_5V_MAIN	TRUE			38
	+5V_MAIN	TRUE	2		38 39
	+5V_SLEEP	TRUE	2		38 39
	+3V_MAIN	TRUE	4		23 38
		TRUE		1000	IN
	+3V_PMU	TRUE			38
CARDBUS	CBUS_DET_1_L	TRUE		2000	18
	CBUS_DET_2_L	TRUE		2000	18
DVI	TMDS_DN<0..2>	TRUE		1000	19 22 37
	TMDS_DP<0..2>	TRUE		1000	19 22 37
	TMDS_CONN_CLKN	TRUE		1000	22 36
	TMDS_CONN_CLKP	TRUE		1000	22 36
	VGA_R	TRUE		1000	22
	VGA_G	TRUE		1000	22
	VGA_B	TRUE		1000	22
	VGA_HSYNC	TRUE		1000	22
	VGA_VSYNC	TRUE		1000	22
	DVI_DDC_CLK_UF	TRUE		1000	22
	DVI_DDC_DATA_UF	TRUE		1000	22
	DVI_HPD_UF	TRUE		1000	22
	+5V_DDC_SLEEP	TRUE		2000	22 38
		TRUE	2	2000	IN
CHGND1		TRUE	6	1000	IN
LVDS	LVDS_L0N	TRUE		1000	20 22 37
	LVDS_L0P	TRUE		1000	20 22 37
	LVDS_L1N	TRUE		1000	20 22 37
	LVDS_L1P	TRUE		1000	20 22 37
	LVDS_L2N	TRUE		1000	20 22 37
	LVDS_L2P	TRUE		1000	20 22 37
	CLKLVDS_LN	TRUE		1000	20 22 37
	CLKLVDS_LP	TRUE		1000	20 22 37
	LVDS_DDC_CLK	TRUE		1000	20 22
	LVDS_DDC_DATA	TRUE		1000	20 22
	+3V_LCD	TRUE	2	2000	22 38
	+3V_SLEEP	TRUE		2000	38 39
		TRUE	2	2000	IN
CHGND4		TRUE	6	1000	IN
INVERTER	+14V_INV	TRUE		2000	22 38
	+5V_INV_SW	TRUE		2000	22 38
	BRIGHT_PWM	TRUE		2000	22
	INV_GND	TRUE		2000	22
		TRUE		1000	IN
S-VIDEO	TV_C	TRUE		2000	22
	TV_Y	TRUE		2000	22
	TV_COMP	TRUE		2000	22
	TV_GND1	TRUE		2000	22 38
	TV_GND2	TRUE		2000	22 38
LIO	INT_I2S0_SND_TO_DAC	TRUE		1000	14 25
	INT_I2S0_SND_LRCLK	TRUE		1000	14 25
	INT_I2S0_SND_MCLK	TRUE		1000	14 25 35
	INT_I2S0_SND_SCLK	TRUE		1000	14 25
	INT_I2S0_SND_FROM_ADC	TRUE		1000	14 25
	SND_HP_MUTE_L	TRUE		1000	14 25
	SND_AMP_MUTE	TRUE		1000	25
	SND_HW_RESET_L	TRUE		1000	14 25
	SND_HP_SENSE_L	TRUE		1000	14 25
	SND_LIN_SENSE_L	TRUE		1000	14 25
	INT_I2C_CLK2	TRUE		1000	14 25
	INT_I2C_DATA2	TRUE		1000	14 25
	ADAPTER_DET	TRUE		1000	25 29
	CHARGE_LED_L	TRUE		1000	25 29
	NEC_LUSB_OCI_UF	TRUE		1000	17 25
	NEC_LUSB_PPON	TRUE		1000	17 25
	+5V_MAIN	TRUE	2	2000	38 39
	+5V_SLEEP	TRUE	2	3000	38 39
	+3V_SLEEP	TRUE		2000	38 39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
USB	NEC_USB_DAM	TRUE			17 25 37
	NEC_USB_DAP	TRUE			17 25 37
	NEC_USB_DBM	TRUE			17 25 37
	NEC_USB_DBP	TRUE			17 25 37
	BT_USB_DM	TRUE			14 25 37
	BT_USB_DP	TRUE			14 25 37
	MODEM_USB_DM	TRUE			14 25 37
	MODEM_USB_DP	TRUE			14 25 37
	NEC_RUSB_PPON	TRUE			17 25
	NEC_RUSB_OCI_UF	TRUE			17 25
RT. USB WIRELESS	PCI_AD<0..31>	TRUE		1000	9 12 17 18 24 37
	PCI_FRAME_L	TRUE		1000	12 17 18 24 37
	PCI_TRDY_L	TRUE		1000	12 17 18 24 37
	PCI_IRDY_L	TRUE		1000	12 17 18 24 37
	PCI_DEVSEL_L	TRUE		1000	12 17 18 24 37
	PCI_STOP_L	TRUE		1000	12 17 18 24 37
	PCI_PAR	TRUE		1000	12 17 18 24 37
	AIRPORT_PCI_REQ_L	TRUE		1000	12 24
	AIRPORT_PCI_GNT_L	TRUE		1000	12 24
	AIRPORT_PCI_INT_L	TRUE		1000	14 24
	MAIN_RESET_L	TRUE		1000	14 17 18 19 24 29
	CLK33M_AIRPORT	TRUE		1000	12 24 35
	PMU_PME_L	TRUE		1000	14 17 24 29
	ROM_ONBOARD_CS_L	TRUE		1000	9
	ROM_OE_L	TRUE		1000	9 12
	ROM_CS_L	TRUE		1000	9 12
	ROM_RW_L	TRUE		1000	9 12
	RF_DISABLE_L	TRUE		1000	24
	AIRPORT_CLKRUN_L	TRUE		1000	24
	+3V_AIRPORT	TRUE	4	2000	38
		TRUE	6	1000	IN
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000	24 37
	EIDE_OPTICAL_DMA_RQ	TRUE		2000	24 37
	EIDE_OPTICAL_READ_L	TRUE		2000	24 37
	EIDE_OPTICAL_DMAACK_L	TRUE		2000	24 37
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000	24 37
	EIDE_OPTICAL_CS0_L	TRUE		2000	24 37
	EIDE_OPTICAL_CS1_L	TRUE		2000	24 37
	EIDE_OPTICAL_RST_L	TRUE		2000	24 37
	EIDE_OPTICAL_WR_L	TRUE		2000	24 37
	EIDE_OPTICAL_IOCHRDY	TRUE		2000	24 37
	EIDE_OPTICAL_INT	TRUE		2000	24 37
TRACKPAD	+5V_TPAD_SLEEP	TRUE		3000	23 38
	TPAD_F_TXD	TRUE		3000	23
	TPAD_F_RXD	TRUE		3000	23
	LID_CLOSED_L	TRUE		3000	23
	+3V_HALL_EFFECT	TRUE		3000	23 38
	SOFT_PWR_ON_L	TRUE		3000	22 23 29 33
MODEM/ SERIAL	COMM_RESET_L	TRUE		4000	14 25
	COMM_SHUTDOWN	TRUE		4000	14 25
	COMM_RING_DET_L	TRUE		4000	14 25 29
	COMM_TXD_L	TRUE		4000	14 25
	COMM_TRXC	TRUE		4000	14 25
	COMM_GPIO_L	TRUE		4000	14 25
	COMM_DTR_L	TRUE		4000	14 25
	COMM_RTS_L	TRUE		4000	14 25
	COMM_RXD	TRUE		4000	14 25
KEYBOARD	KBD_ID	TRUE		3000	23 29
	KBD_INTL	TRUE		3000	23
	KBD_JIS	TRUE		3000	23
	KBD_CAPSLOCK_LED	TRUE		3000	23
	KBD_NUMLOCK_LED	TRUE		3000	23
	KBD_FUNCTION_L	TRUE		3000	23 29
	KBD_COMMAND_L	TRUE		3000	23 29
	KBD_OPTION_L	TRUE		3000	23 29
	KBD_CONTROL_L	TRUE		3000	23 29
	KBD_SHIFT_L	TRUE		3000	23 29
	KBD_X<0..9>	TRUE		3000	23 29
	KBD_Y<0..7>	TRUE		3000	23 29
BATTERY	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000	30 38
	BATT_CLK	TRUE		1000	30
	BATT_DATA	TRUE		1000	30
	PMU_BATT_DET_L	TRUE		1000	29 30
FANS	+FAN_PWR	TRUE		3000	25 38
	FAN1_TACH	TRUE		3000	25
	FAN2_TACH	TRUE		3000	25
	FAN1_GND	TRUE		3000	38
	FAN2_GND	TRUE		3000	38
ETHERNET	MDI_P<0..3>	TRUE		1000	26 37
	MDI_M<0..3>	TRUE		1000	26 37
FIREWIRE	FW_TPO0P	TRUE		1000	27 28 37
	FW_TPO0N	TRUE		1000	27 28 37
	FW_TPO0R	TRUE		1000	28
	FW_TPI0P	TRUE		1000	27 28 37
	FW_TPI0N	TRUE		1000	27 28 37
	+FW_VP0	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST	
FIREWIRE (CONT.)	FW_TPO1P	TRUE		1000	28 37
	FW_TPO1N	TRUE		1000	28 37
	FW_TPI1P	TRUE		1000	28 37
	FW_TPI1N	TRUE		1000	28 37
	+FW_VP1	TRUE		1000	28 38
	FW_VGND	TRUE		1000	39
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000	30 31 38
LMU/ALS	ST7_SLEEP_LED_H	TRUE			23
	PMU_SLEEP_LED	TRUE			23
	PMU_LID_CLOSED_L	TRUE			23 29
	LMU_DETECT	TRUE			23
		TRUE	6	1000	IN
MISC.			(100 MIL PROBE PREFERRED)		
	SLEEP_LED	TRUE			23
	PMU_KB_RESET_L	TRUE			29
	SLEEP	TRUE			23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE			6 29
	BB_RESET_L	TRUE			6
	+3V_PMU_RESET	TRUE			29 33

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APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6653 | REV. C
SCALE NONE | SHT 39 OF 44

REVISION HISTORY

Proto/EVT Release

10/27/03 - 1. Schematic originated from Q16 MLB

11/10/03 - 1. Replace U56 symbol
2. Connect OVDDSENSE to MAXBUS_SLEEP
3. Modify SRW0, SRW1 and IARTRY0 connection
4. Connect VDD(Page 6) to CPU_VCORE_SLEEP(PAGE 5)
5. Connect SENSEVDD to CPU_VCORE_SLEEP
6. Connect SENSEGND to GND
7. Add 4 pcs 0 ohm resistor for AMD BootRom issue (R1,R194,R236,R271)
8. Connect TEMP_ANODE and TEMP_CATHODE to ADT7460
9. Modify CPU PLL config
10. Add 0 ohm resistor on CG_FSEL Interpid side(R450)
11. Replace U47 symbol
12. Change R743 from 2m ohm to 1m ohm
13. Change C773,C781,C788,C793,C797,C802 from 220uF to 330uF
14. Change R748 from 410 ohm to 10 ohm

12/01/03 - 1. Modify CPU_VCORE setting.

12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting

12/05/03 - 1. Add CPU AVDD LDO (Page 5)
2. Change Q45 and Q41 to IRF7805 (376S0035)
3. Change Q47 and Q42 to IRF7811W (376S0104)
4. Change R402 and R409 to 4.7ohm resistors
5. Connect INT_TDO from intrepid to Cypress Chip PD* (U31)

12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust
2. Modify CPU_VCORE setting to Motorola new spec
3. Modify LDO power sequence

12/16/03 - 1. Add 10K pull down for INT_TDO on page 13

12/17/03 - 1. Change LDO Vin from +3V_MAIN to +3V_SLEEP
2. Connect INT_TDO from Intrepid to Marvell 88E1111(U43)
3. Add R755,R756,R758,R759 for power rail

DVT Release (Rev. 02)

01/30/04 - 1. Add Soft_Modem(Pin#14) 10K pull-up at J15.7 (Pg 25)
2. Add Bom Table for R97 2.21K ohm VCore Offset (Pg 33)

02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5)
2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9)

DVT Release (Rev. 03)

02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33)
2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5)
3. ATI INT.TMDS termination change to 0 ohm, Qty:8 (Pg 20)
4. AGP I/O VREF voltage divider chagne to both 1K ohm (Pg 12)

DVT Release (Rev. 04)

02/13/04 - 1. INT. TMDS Termination change to 2* 49.9ohm = 100ohm (Pg 20)

PVT Release (Rev. A)

03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20)
2. USB series termination near NEC PHY change to 47 ohm (Pg 17)

PVT Release (Rev. A - 051-6570)

04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17)

Production Release (Rev. A - 051-6653)

04/09/04 - 1. Updated to Apollo 7PM rev 1.1.1 part numbers (Pg 5)
04/09/04 - 2. Updated to production BootROM part number (Pg 9)

Production Release (Rev. B - 051-6653)

04/30/04 - 1. Updated to Fast Intrepid part for 6A ReadMacro Delay value (Pg 8-15)
04/30/04 - 2. Add ATI M11 A16 parts as alternative for A15 parts (Pg 19-21)
04/30/04 - 3. Use new VGA filter to remove ghost image on external VGA display (Pg 22)

Production Release (Rev. C - 051-6653)

05/27/04 - 1. Updated BOM : 113S0006 -> 113S1000
05/27/04 - 2. Updated BOM : 132S0020 -> 132S0100

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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE NONE	SHT 40	44

8 7 6 5 4 3 2 1

D C B A

*** Signal Cross-Reference for the entire design ***

+1.0V_MARVELL 26D2< 38B3<
+1.5V_AGP 12B5< 12D1< 12D4< 15D6< 16C8<
19C6< 19D6< 20A8< 20B4< 20D5<
21B6< 21D6< 38C3<
+1.5V_AGP_GPU 21C5< 38C3<
+1.5V_AGP_NECK 20B4< 38B3<
+1.5V_GPU_VDD15 20D3< 38C3<
+1.5V_INTREPID_PLL 8D6< 12D4< 12D8< 14D6<> 38D3>
+1.5V_INTREPID_PLL1 14C3< 38D3<
+1.5V_INTREPID_PLL2 14D3< 38D3>
+1.5V_INTREPID_PLL3 14D3< 38D3>
+1.5V_INTREPID_PLL4 14D3< 38D3>
+1.5V_INTREPID_PLL5 12D3< 38D3>
+1.5V_INTREPID_PLL6 12D6< 38D3>
+1.5V_INTREPID_PLL7 8D5< 38D3>
+1.5V_INTREPID_PLL8 14D3< 38C3>
+1.5V_LDO 38D6<
+1.5V_MAIN 38D6>
+1.5V_SLEEP 38D6>
+1.5V_SLEEP_NECK 38D2< 38B3>
+1.5V_SLEEP_VIN 38D6>
+1.5V_ATI_PVDD 20C5< 21B6< 21D6<> 38C3>
+1.5V_ATI_TPVDD 21D2<> 38B3>
+1.8V_GPU 19A8< 19C2<> 20D7< 21A2< 21A6<
21B1< 21B6< 21C6< 21D6< 21D8< 38C3>
+1.8V_GPU_AVDD 21D5< 38B3>
+1.8V_GPU_AVDDQ 21D4< 21D7< 38B3>
+1.8V_GPU_DVDD 21C4< 38B3>
+1.8V_GPU_MEMPLL 21B5< 38B3>
+1.8V_GPU_PLL 21D3< 38C3>
+1.8V_GPU_PNLIO 21A5< 38B3>
+1.8V_GPU_PNLPLL 21B5< 38D7>
+1.8V_GPU_TP_PLL 21B5< 21D1< 38B3>
+1.8V_GPU_VDDCI 21C7< 21D4< 38C3>
+1.8V_MAIN 38D6<>
+1.8V_PVDD_NECK 20B5<> 38B3>
+1.8V_SLEEP 38D6>
+1.8V_SLEEP_NECK 34D2<> 38B3>
+1.95V_FW_DVDD 27C4< 27C7<> 27D5< 38A3>
+1.95V_FW_DVDD_PORT1 27D6< 38A3>
+1.95V_FW_DVDD_RX0 27C5< 38A3>
+1.95V_FW_DVDD_TX0 27C5< 38A3>
+1.95V_FW_PLL400DD 27C4< 38A3>
+1.95V_FW_PLL500VDD 27D4< 38A3>
+1.95V_FW_PLLVDD 27D4< 27D6<> 38A3>
+2.5V_CG_MAIN 34C6<
+2.5V_GPU 38C3>
+2.5V_GPU_A2VDD 21D4< 21D7< 38B3>
+2.5V_GPU_MCKC 21C7< 21D4< 38B3>
+2.5V_GPU_MEMCORE 21C5< 38C3>
+2.5V_GPU_VDDC 21D3< 38C3>
+2.5V_INTREPID 9A7< 16D3< 16D6< 18D6< 18D8< 15D6<
16B8< 38D3>
+2.5V_MAIN 38D6< 39C6>
+2.5V_MARVELL 26B6< 26C4<> 38B3>
+2.5V_MARVELL_AVDD 26C4< 38B3>
+2.5V_SLEEP 38D6>
+2.5V_SLEEP_NECK1 20C4<> 38B3>
+2.5V_SLEEP_NECK2 20D5<> 38B3>
+3V_AIRPORT 38C3> 39C3>
+3V_ATI_OSC_SLEEP 19B2< 38B3>
+3V_ATI_SS 12D1< 38B3>
+3V_CG_PLL_MAIN 14C6<
+3V_FW 27A3< 27D7<> 28D5< 38A3>
+3V_FW_AVDD 27C6< 38A3>
+3V_FW_AVDD_PORT0 27C6< 38A3>
+3V_FW_AVDD_PORT1 27C6< 38A3>
+3V_FW_AVDD_PORT2 27D6< 38A3>
+3V_FW_ESD 28B4<> 28D3<>
+3V_FW_ESD_ILIM 28D6<
+3V_FW_UF 27D7<> 38A3>
+3V_GPU 12D1< 18B6< 19C6< 19C8< 19D6<
20C4< 20C5< 20C7< 20D7< 21A6< 21B1<
38C3>
+3V_GPU_FLT 21B2< 38C3>
+3V_HALL_EFFECT 23B4<> 38B6> 39B3>
+3V_INTREPID_USB 13B7<> 38C3>
+3V_LCD 22B4<> 38B6> 39B6>
+3V_LCD_SW 22B4<> 38B6>
+3V_MAIN 22B4<> 38D6> 39C6>
+3V_MAIN_AUD 25C6<> 32C1<> 38B6>
+3V_MAIN_JUMPER 38D1>
+3V_MAIN_LMU 23D7<> 38A1>
+3V_MAIN_SSCG 38A1>
+3V_MIC_VDD 17B3< 17D7< 17D7< 38A3>
+3V_PMU 38D6> 39C6>
+3V_PMU_AVCC 25B4< 25D6<> 38C6>
+3V_PMU_ESR 31A2< 38C6>
+3V_PMU_RESET 29B7< 33A4<> 39C1>
+3V_SI_AVCC 38A5>
+3V_SI_PLLVCC 19D3<
+3V_SI_VCC 19D3<
+3V_SLEEP 38D6< 39A6> 39B6>
+3V_SLEEP_NECK 34D1< 38B3>
+3V_SLEEP_PCARD 18B7< 38C3>
+3V_SLP_OK_L 32B4<>
+3V_SLP_ON 32A5<>
+4.0V_BU 31B5< 32B7< 38C6>
+4.85V_ESR 31A4< 38C6>
+4.85V_RAW 29A5< 31B4<> 38C6>
+5V_DDC_SLEEP 22D5< 22D5<> 38B6> 39B6>
+5V_DDC_SLEEP_UF 22D6< 38B6>
+5V_HD_SLEEP 24D1<> 32A7< 38C6>
+5V_INV_SW 22B2< 38B6> 39A6>
+5V_INV_UF_SW 22B2<> 38B6>
+5V_MAIN 22B4<> 38A6> 39C6>
+5V_MAIN_AUD 25C6<> 32C8<> 38B6>
+5V_MAIN_JUMPER 38D1>
+5V_SLEEP 38A6> 39A6> 39C6>
+5V_SLEEP_OPT 24B5<> 38A1>
+5V_TPAD_SLEEP 24B6<> 38B6> 39B3>
+14V_INV 22B2< 38B6> 39B6>
+24V_PBUS 38D6> 39C6>
+ADAPTER 38D6<> 39A7< 38C6> 39D1>
+ADAPTER_ILIM 31A6< 38C6>
+ADAPTER_OR_BATT 31A5<> 38C6>
+ADAPTER_SENSE 30B4<> 38C6>
+ADAPTER_SW 38D5<> 38C6> 38C6>
+BATT 38A6> 39C6>
+BATT_14V_FUSE 38D1<> 38C6>
+BATT_24V_FUSE 38B1< 38D2<> 38C6>
+BATT_POS 38A4<> 38B6> 39A3>
+BATT_RSNS 38B2< 38C6>
+BATT_VSNS 38A4< 38C6>
+FAN_PWR 25A3< 25A4< 38B6> 39A3>
+FW_AMP_SENSE 38A3>
+FW_PBUS 28D7<> 38A3>
+FW_PWR1 28C5< 38A3>
+FW_PWR_OR 27B4< 27D6<> 28D5<> 38A3>
+FW_SW 28D5<> 38A3>
+FW_VP0 28C1<> 38A3> 39A3>
+FW_VP1 28C1<> 38A3> 39D1>
+GPU_VDD15_NECK 20B5<> 38B3>
+GPU_VDD15_UF 20B5<> 20D4<> 38B3>
+HD_LOGIC_SLEEP 38C6>
+PBUS 38D6> 39C6>
+PBUS_JUMPER 38D1>
+VCC_CBUS_SW 18B1<> 18B2<> 18D2<> 38C3>
+VPP_CBUS_SW 18B1<> 18B2<> 18D2<> 38C3>
1V2B_REF 30C7< 31C6< 38D1>
1V65_REF 30A5<
1_5V_BOOST 34C6<> 38C1>
1_5V_BST 34C5<> 38C1>
1_5V_DH 34C5<> 38C1>
1_5V_DL 34B5<> 38C1>
1_5V_FB 34B5< 34B7< 38C1>
1_5V_ILIM 34C5< 38C1>
1_5V_LX 34B6< 38C1>
1_5V_LX_F 38C1>
1_5V_SLEEP_EN_L 34C7<> 34D7<>
1_8V_PVDD_STD 18D7<
1_8V_SLEEP_PWREN_L 34A3<>
1_8V_SW 34A5<> 38A1>
1_8V_SW_F 38A1>
1_8V_TPVDD_STD 21D1<
1_5V_VFB 34A5<> 38A1>
2_5V_BOOST 34C4<> 38D1>
2_5V_BST 34C4<> 38D1>
2_5V_DH 34C3<> 38D1>
2_5V_DL 34B3<> 38C1>
2_5V_FB 34B4<
2_5V_ILIM 34C5<> 38C1>
2_5V_LX 34B3<> 38D1>
2_5V_LX_F 38D1>
2_5V_SLEEP_PWREN_L 34C2<>
3V_5V_OK 32A6> 34A8< 34D6<

3V_BG 32C4<>
3V_BOOST 32C4<>
3V_BOOST_ESR 32D3<>
3V_ITH 32C4<>
3V_ITH_RC 32C3<
3V_PMU_VTAP 31B3<
3V_RSNS 32D2< 38D1>
3V_RUNSS 32C4<>
3V_SLEEP_PWREN_L 32B3<>
3V_SNSM 32C4< 37A2>
3V_SNSP 32C4< 37A2>
3V_SW 32C4< 38D1>
3V_TG 32C4<>
3V_VOSNS 32C5<>
3V_BOOST_ESR 32D6<>
5V_HD_PWREN 32B3<>
5V_ITH 32C5<>
5V_ITH_RC 32C6<
5V_RSNS 32D7< 38D1>
5V_RUNSS 32C5<>
5V_SLEEP_PWREN 32A8<>
5V_SNSM 32C5< 37A2>
5V_SNSP 32C5< 37A2>
5V_SW 32C5< 38D1>
5V_TG 32C5<>
5V_VOSNS 32C5<>
16Z5_BG 31C5<>
16Z5_BST 31C5<>
16Z5_BST_ESR 31C5<>
16Z5_COMP 38D2< 31C6<
16Z5_DIV 31C8<
16Z5_ENABLE 31D7<>
16Z5_ENABLE_L 31D5<>
16Z5_EXTVCC 31D5<> 38D1>
16Z5_FCB 31C6<>
16Z5_INTVCC 31B5< 38D1>
16Z5_RUNSS 31C6<
16Z5_SGND 31B7<> 38D1>
16Z5_TG 31C5<>
1725_VFB 31B5<>
1725_VIN 31D6< 38D1>
1725_VSW 31C4< 38D1>
1772_ACIN 38B5<
1772_ACOK_L 30B5<> 30C4<>
1772_BST 30B4<>
1772_BST_ESR 30C4<
1772_CCI 30B5<>
1772_CCS 30B5<
1772_CCV 30B5<>
1772_CCV_RC 30B5<
1772_CELLS 30B4<>
1772_CLS 30A4<
1772_CSIN 30B4<> 37A2>
1772_CSIP 30B4<> 37A2>
1772_CSSN 30C5< 37A2>
1772_CSSP 30C5< 37A2>
1772_DCIN 30B6< 38C6>
1772_DHI 30B4<>
1772_DLO 30B4<>
1772_DLOV 30B4<> 38C6>
1772_GND 30A5< 38C6>
1772_ICHG 38B5<
1772_ICTL 30B5<>
1772_HDF 30B5<
1772_LDO 30C4< 38C6>
1772_LX 30B4< 38C6>
1772_REF 30B5<>
1772_VCTL 30B5<
1778_BG 20A5<> 38B1>
1778_BST 20A5< 38B1>
1778_BST_RC 20A5< 38B1>
1778_FCB 20A6< 38B1>
1778_GND 20A6< 20A7<> 38B1>
1778_ION 20A5< 38B1>
1778_ITH 20A6<> 38B1>
1778_ITH_RC 20A7< 38B1>
1778_SHDN_L 20A6<>
1778_TG 20A5<> 38B1>
1778_VCC 20A5< 38B1>
1778_VFB 20A2< 20A5< 38B1> 39C6>
1778_VIN 20A5< 38B1>
1778_VRNG 20A6< 38B1>
3405_MODE 26D5<>
3405_VFB 26D4<>
3707_FCB 32D5<>
3707_FSET 32C5<
3707_INTVCC 32D4<> 38D1>
3707_SGND 32B5<> 38D1>
3707_STBY 32C5<>
A29_CLS_ADJ 38A5<>
A29_CURRENT_ADJ 30C4<>
A29_DETECT 29A2< 38A5<> 30C4<>
A29_DET_L 29A3< 38A5<
A29_DET_REF 29A4<
A2_DIV 30B7<
AC_ENABLE_GATE 30D6<>
AC_ENABLE_L 30C5<>
AC_GTR_18V 30C3<>
AC_IN 26B8<> 28C8< 29B3< 30C5<> 30C6<>
AC_IN_FW_CNTL 28C7<>
AC_IN_L 30C2<> 30C6<>
AC_IN_L_RC 30C2<>
ADAPTER_DET 25B8<> 29A4< 39A6>
ADAPTER_I_REG 36D3<>
ADT7460_ADR_ENABLE_L 25B3<>
ADT7460_TACH1_FB 25B2<>
ADT7460_THERM_L 25B2< 25B3<>
ADT7460_VCORE 25C4<
ADT7460_VCORE_MON 5C8<> 25B4<>
AGP8X_DET_PU 19C6<>
AGP_ADD<0> 12D2<> 19C7<>
AGP_AD<15..0> 37D5>
AGP_AD<1> 12C2<> 19C7<>
AGP_AD<2> 12C2<> 19C7<>
AGP_AD<3> 12C2<> 19C7<>
AGP_AD<4> 12C2<> 19C7<>
AGP_AD<5> 12C2<> 19C7<>
AGP_AD<6> 12C2<> 19C7<>
AGP_AD<7> 12C2<> 19C7<>
AGP_AD<8> 12C2<> 19C7<>
AGP_AD<9> 12D2<> 19C7<>
AGP_AD<10> 12C2<> 19C7<>
AGP_AD<11> 12C2<> 19C7<>
AGP_AD<12> 12C2<> 19C7<>
AGP_AD<13> 12C2<> 19C7<>
AGP_AD<14> 12C2<> 19C7<>
AGP_AD<15> 12C2<> 19C7<>
AGP_AD<16> 12C2<> 19C7<>
AGP_AD<31..16> 37D5>
AGP_AD<17> 12C2<> 19C7<>
AGP_AD<18> 12C2<> 19C7<>
AGP_AD<19> 12C2<> 19C7<>
AGP_AD<20> 12C2<> 19C7<>
AGP_AD<21> 12C2<> 19C7<>
AGP_AD<22> 12C2<> 19C7<>
AGP_AD<23> 12C2<> 19C7<>
AGP_AD<24> 12C2<> 19C7<>
AGP_AD<25> 12C2<> 19C7<>
AGP_AD<26> 12C2<> 19D7<>
AGP_AD<27> 12B2<> 19D7<>
AGP_AD<28> 12B2<> 19D7<>
AGP_AD<29> 12B2<> 19D7<>
AGP_AD<30> 12B2<> 19D7<>
AGP_AD<31> 12B2<> 19D7<>
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AGP_AD_STB<1> 12A2<> 12B2< 19D6<> 37D5>
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CPU_TBST_L 5A7> 8B5<> 36D5>
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PMU_SLEEP_LED_L   23C8<> 29C4<>
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RAM_BA<1>         9A4< 11B3<> 11B6<>
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RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  35C5>
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RAM_DATA_A<23..16>  35C5>
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RAM_DATA_B<23..16>  35C5>
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RAM_DATA_B<47..40>  35B5>
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RAM_DATA_B<47>    10C4<> 11A3<>
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RAM_DATA_B<55..48>  35B5>
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RAM_DATA_B<55>    10C2<> 11A3<>
RAM_DATA_B<56>    10C2<> 11A5<>
RAM_DATA_B<63..56>  35A5>
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RAM_DATA_B<58>    10C2<> 11A5<>
RAM_DATA_B<59>    10C2<> 11A5<>
RAM_DATA_B<60>    10C2<> 11A3<>
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ROM_ONBOARD_CS_TP_L  9B3< 24C6<>
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SI_I2S_DATA       19C4< 20C5<>
SI_MSEN           19D2<>
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SI_RST_L          19C4<
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SI_TMDS_CLKP      19C2<> 19C2< 36D1>
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SND_HP_MUTE_L     14C5<> 25C5<> 39A6>
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SND_HW_RESET_L    14A7< 14B5<> 25D7<> 39A6>
SND_LIN_SENSE_L   14B5<> 25C8<> 39A6>
SOFT_PWR_ON_L     22D1<> 23A5< 29A8< 29C6<> 29D7<
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ST7_SLEEP_LED_H   23C5<> 23C6<> 23D6<> 39D1>
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SYSCLK_CPU_UF     8A5<> 35D1>
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SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 35C1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 35D1>
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SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 35D1>
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SYSCLK_DDRCLK_B0_L  9C4< 11D5<> 35C1>
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SYSCLK_DDRCLK_B1  9D4< 11A3<> 35C1>
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THERM1_DP         25A5< 25A6< 25B5<> 25B6< 37A2>
THERM1_M_DM       25B7< 25B8< 37A2>
THERM1_M_DP       25B7< 25B8< 37A2>
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THERM2_M_DP       25B7< 25B8< 37A2>
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TMDS_CONN_CLKP    22C7<> 22C7<> 36C1> 39C6>
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USB_DFP           14B2<> 14C2< 37B2>
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VCORE_TIME        33B4<> 38B1>
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VGA_G             22C5<> 22C7< 39B6>
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VGA_R             22B7< 22C5<> 39B6>
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ZT10_SPN          4C2<>
ZT301_SPN         4C2<>
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ZV_LCDDATA20_PU  29C7<>
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SIZE	DRAWING NUMBER	REV.
D	051-6653	C
SCALE: NONE	SHT 42 OF 44	

*** Part Cross-Reference for the entire design ***

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J3	CON_M40ST_D4MT_SM	25
J4	CON_4RT_WRIB	22
J5	CON_M80ST_D4MT_SM	18
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J8	CON_2RTSM_125	23
J9	CON_F1ST_S2MT_SM	14
J10	CON_10STSM_5087	23
J11	CON_F30RT_S2MT_SM1	23
J12	CON_M50SM_5MM	24
J13	CON_M50SM_5MM	24
J14	CON_F30RT_S2MT_SM	22
J15	CON_M16ST_D_SMA	25
J16	CON_3RTSM_125	31
J17	CON_M16ST_D_SMA	25
J18	CON_M4RT_S2MT_SM	25
J19	CON_F20ST_D_SM	23
J20	CON_F9RT_1394B_S6MT_SMA	28
J21	CON_F5RT_MINIDIN_TH	22
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R789	RES	23
R790	RES	33
R791	RES	33
R792	RES	33
R794	RES	33
R795	RES	33
R796	RES	33
R797	RES	33
R798	RES	17
R806	RES	25
R807	RES	25
R808	RES	25
R817	RES	25
R818	RES	19
R819	RES	19
R823	RES	19
R824	RES	19
R825	RES	19
R826	RES	19
R827	RES	19
R828	RES	19
R829	RES	19
R830	RES	19
R832	RES	19
R833	RES	19
R835	RES	19
R836	RES	19
R837	RES	19
R838	RES	19
R839	RES	19
R840	RES	20
R841	RES	21
R842	RES	21
R843	RES	21
RP1	RPAK10P2C	18
RP2	RPAK4P	8
RP3	RPAK4P	8
RP4	RPAK4P	14
RP5	RPAK4P	14
RP6	RPAK4P	14
RP7	RPAK4P	14
RP8	RPAK4P	14
RP9	RPAK4P	9
RP10	RPAK4P	13
RP11	RPAK4P	14
RP12	RPAK4P	9
RP13	RPAK4P	14
RP14	RPAK4P	9
RP15	RPAK4P	14
RP16	RPAK4P	13
RP17	RPAK4P	9
RP18	RPAK4P	24
RP19	RPAK4P	24
RP20	RPAK4P	9
RP21	RPAK4P	24
RP22	RPAK4P	9
RP23	RPAK4P	24
RP24	RPAK4P	24
RP25	RPAK4P	24
RP26	RPAK4P	24
RP27	RPAK4P	24
RP28	RPAK4P	24
RP29	RPAK4P	9
RP30	RPAK4P	24
RP31	RPAK4P	9
RP32	RPAK4P	13
RP33	RPAK4P	12
RP34	RPAK4P	12
RP35	RPAK4P	13
RP36	RPAK4P	12
RP37	RPAK4P	27
RP38	RPAK4P	27
RP39	RPAK4P	29
RP40	RPAK10P2C	23
RP41	RPAK4P	29
RP42	RPAK10P2C	23
RP43	RPAK4P	17
RP44	RPAK4P	17
RP45	RPAK4P	17
RP46	RPAK10P2C	6
RP47	RPAK4P	14
RP49	RPAK4P	19
RP50	RPAK4P	19
RP51	RPAK4P	19
RP52	RPAK2P	19
RP53	RPAK2P	19
RP54	RPAK2P	19
RP55	RPAK2P	19
RP56	RPAK2P	19
RP57	RPAK2P	19
RP58	RPAK2P	19
RP59	RPAK2P	19
RP60	RPAK4P	19
SH1	SHLD_3P_EMI	4
U1	COMPARATOR_LMC7211	30
U2	NC7S32	22
U3	AMP_MAX4172	30
U4	PWR_CNTRL_TPS2211	18
U5	FAN2558	5
U6	MAX1772	30
U7	MAX1717	33
U8	PCI1510GGU	18
U9	SN74AUC1G08	6
U10	SN74AUC1G08	6
U11	FEPR_1MX8	9
U12	SN74AUC1G04	7
U13	LTC1625	31
U14	COMPARATOR_LMC7211	31
U15	PI3B3257	33
U16	CBTV4020	10
U17	UPD720101_FBGA	17
U18	CBTV4020	10
U19	MAX1715	34
U20	NC7S32	29
U21	741125	23
U22	VREG_LP2951	31
U23	VREG_LP2951	31
U24	NC7S32	29
U25	NC7S32	29
U26	MAX6804	29
U27	CBTV4020	10
U28	CBTV4020	10
U29	M16C62	29
U30	CLK_GEN_CY25811	19
U31	CLK_GEN_CY28512	14
U32	LTC1778	20
U33	COMPARATOR_LMC7211	29
U34	VREG_MM1571J	21
U35	LTC3707	32

U36	TSB81BA3A	27
U37	VREG_LM2594	27
U38	VREG_LT1962	27
U39	741G32	22
U40	741G32	22
U42	COMPARATOR_LMC7211	22
U43	TRANSCEIVER_88E1111	26
U44	LTC1761	27
U45	LTC3405	26
U46	LTC3411	34
U47	RAGE_MBLTY_M11_CSP64_667	19 20 21
U48	TRA_SI6467BDQ	34
U49	VREG_LT1962	14
U50	TRA_SI3447DV	34
U51	INTREPID 8 9 12 13 14 15	
U52	EEPROM_32KX8_M24256B	6
U53	ADT7460	25
U54	AT90S1200	6
U55	OPAMP_LMC7111	30
U56	APOLLO_MPC7447A_360	5 6
U57	COMPARATOR_LMC7211	30
U58	SIL1162	19
U60	VREG_MM1571J	21
XW1	SHORT	30
XW2	SHORT	33
XW3	SHORT	31
XW4	SHORT	20
XW5	SHORT	20
XW6	SHORT	20
XW8	SHORT	34
XW9	SHORT	20
XW10	SHORT	34
XW11	SHORT	20
XW12	SHORT	20
XW13	SHORT	32
XW14	SHORT	22
XW15	SHORT	22
XW17	SHORT	34
XW21	SHORT	34
XW23	SHORT	34
XW25	SHORT	34
XW27	SHORT	33
XW28	SHORT	33
XW29	SHORT	33
XW30	SHORT	25
XW31	SHORT	32
XW32	SHORT	32
XW34	SHORT	5
Y1	CRYSTAL	17
Y2	CRYSTAL	14
Y3	CRYSTAL_4PIN	29
Y4	CRYSTAL	29
Y5	CRYSTAL_4PIN	26
ZT1	HOLE_VIA	4
ZT2	HOLE_VIA	4
ZT3	HOLE_VIA	4
ZT4	HOLE_VIA	4
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ZT85	HOLE_VIA	4
ZT86	HOLE_VIA	4