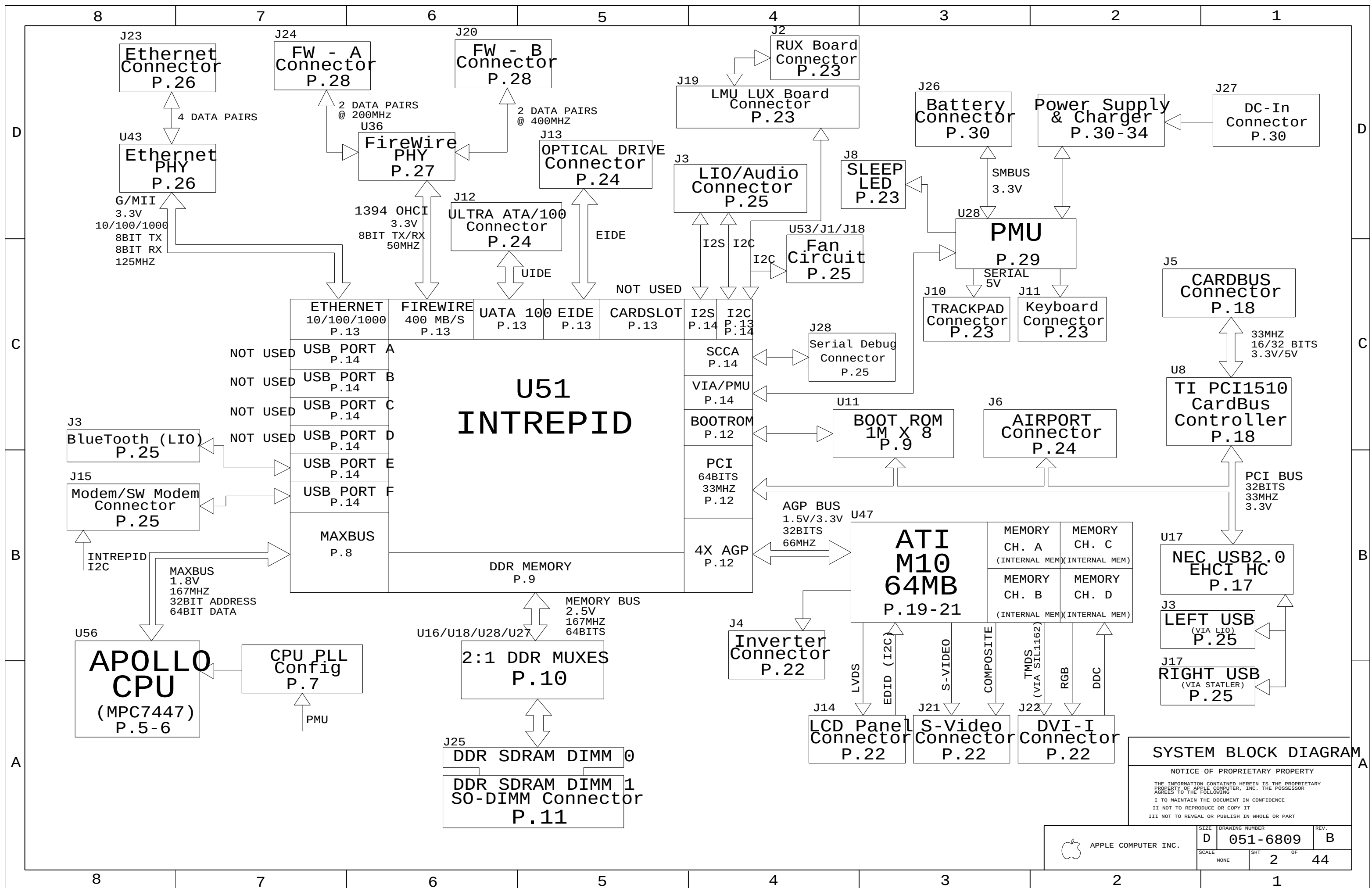
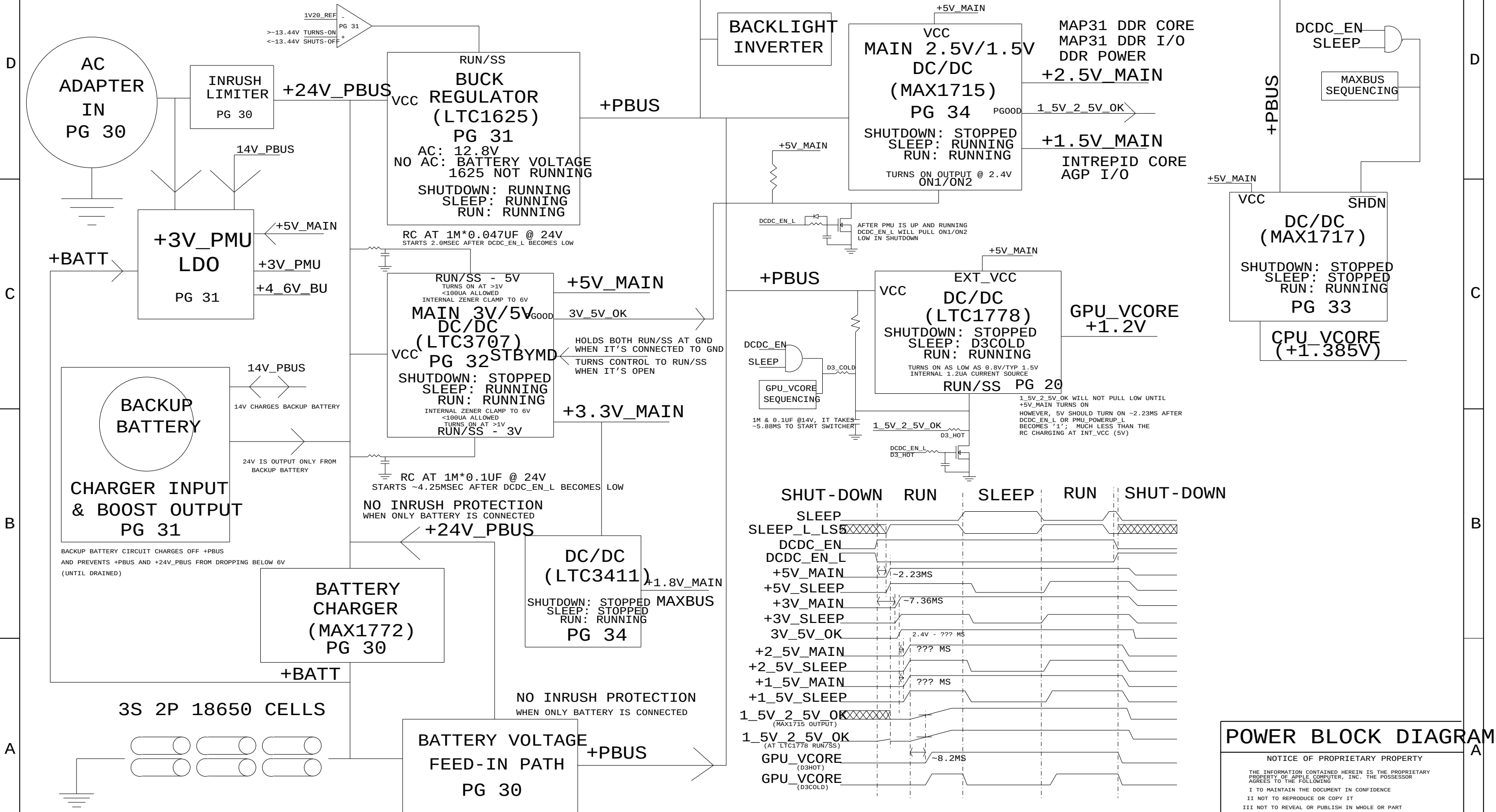




POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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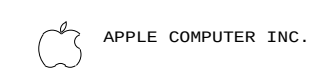
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	D	051-6809	
SCALE		SHT	OF
NONE		3	44



PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 10
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

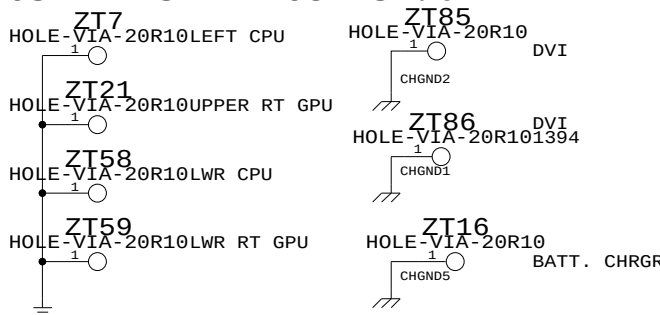
BOARD STACK-UP AND CONSTRUCTION

1-8-1 BLIND MICROVIA/20R10 BURIED VIA/20R10 TH VIA									
1					SIGNAL (1/2 OZ + COPPER PLATING)				
2	PREPREG (3 MIL)				SIGNAL (1/2 OZ)				
3	PREPREG (3 MIL)				GROUND (1/2 OZ)				
4	CORE (3 MIL)				SIGNAL (1/2 OZ)				
5	PREPREG (5 MIL)				CUT POWER PLANE (1 OZ)				
6	CORE (5 MIL)				CUT POWER PLANE (1 OZ)				
7	PREPREG (5 MIL)				SIGNAL (1/2 OZ)				
8	CORE (3 MIL)				GROUND (1/2 OZ)				
9	PREPREG (3 MIL)				SIGNAL (1/2 OZ)				
10	PREPREG (3 MIL)				SIGNAL (1/2 OZ + COPPER PLATING)				

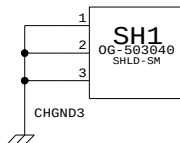
BOARD HOLES

CHASSIS MOUNTS

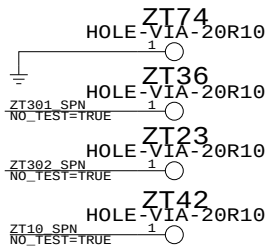
ASICS HEATSINK MOUNTS I/O AREA



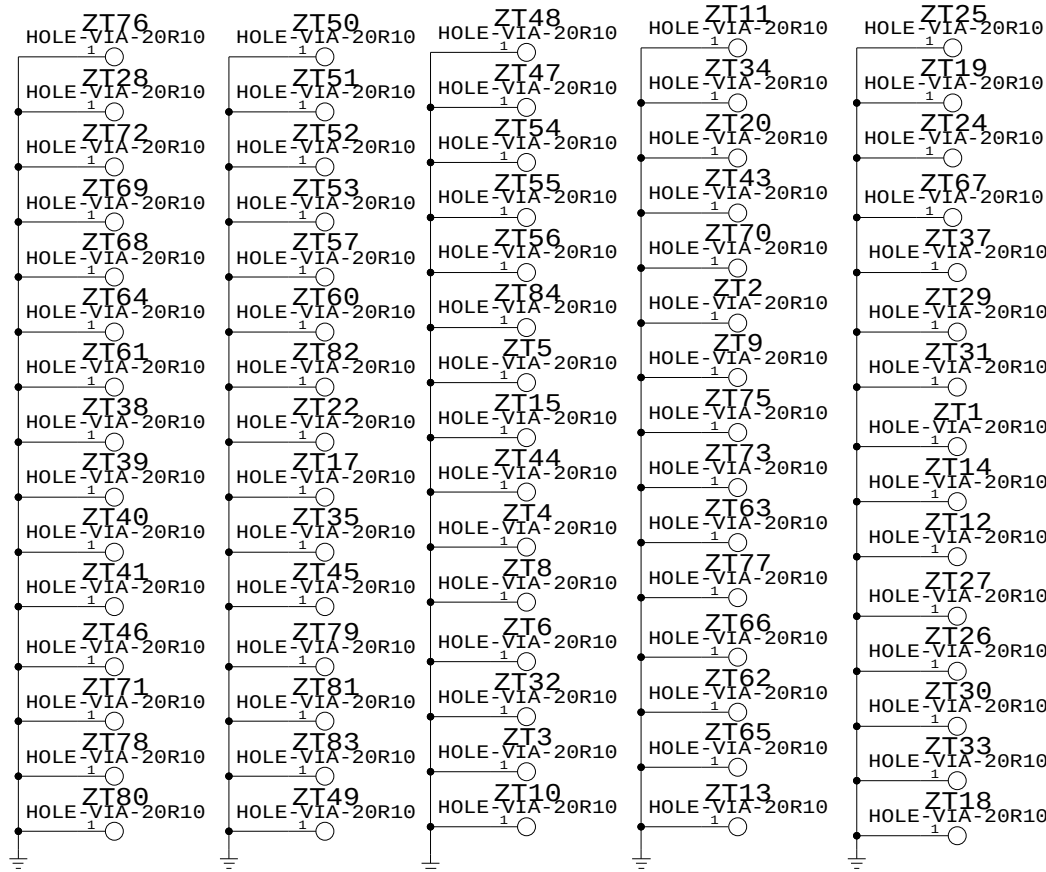
INVERTER



MECH. HOLES



GROUND VIAS



BOARD INFORMATION

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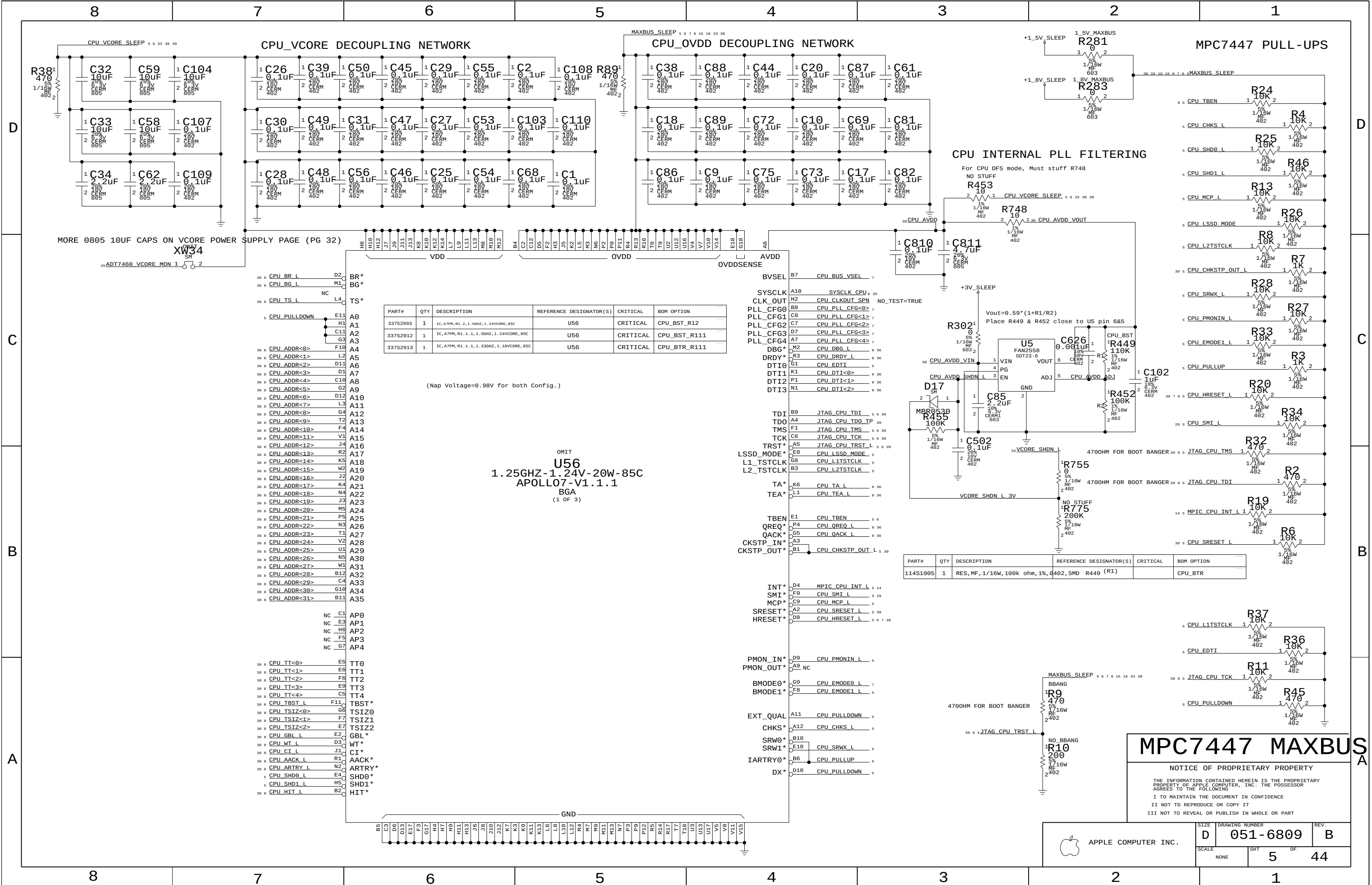
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D	051-6809	B
SCALE	SHT	OF
NONE	4	44



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

APOLLO 7

D

C

B



Schematic diagram of a 22 ohm resistor (R110) connected between CPU_HRESET_L and CPU_EMODE0_L. The resistor is labeled with its value 22, power rating 1/16W, and tolerance MF 482.

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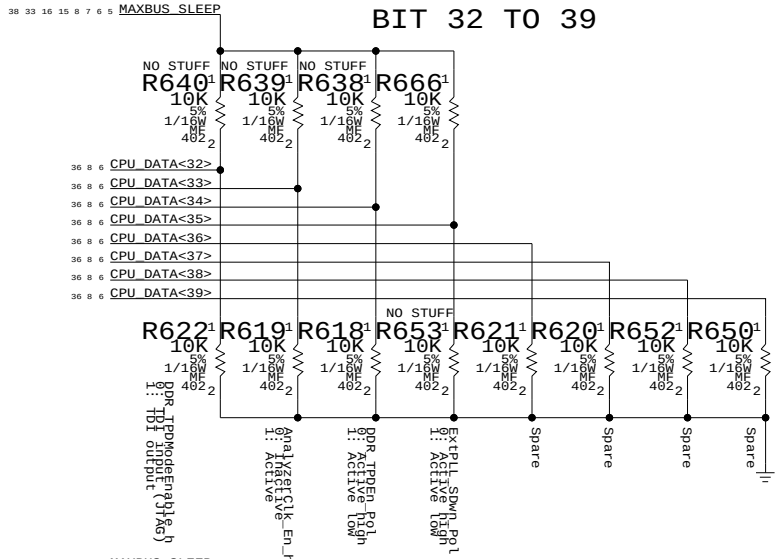
SIZE	DRAWING NUMBER	REV.
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D	051-6809	B
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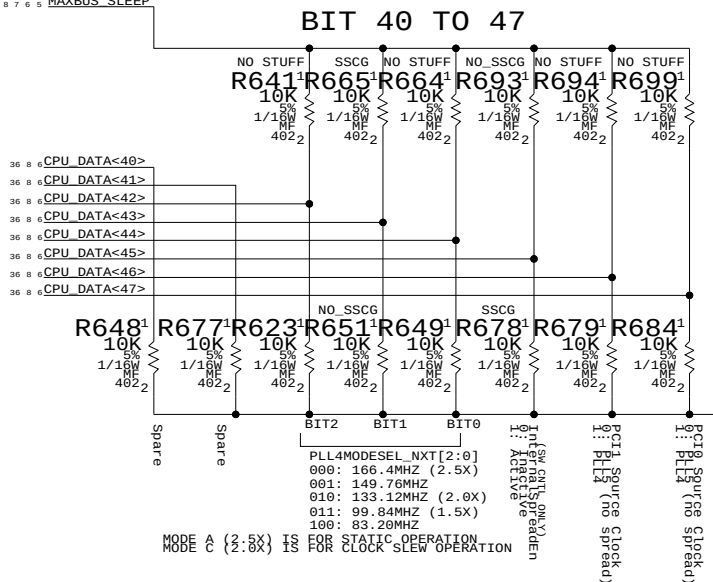
SCALE	SHT	OF
NONE	7	44

INTREPID BOOT STRAPS

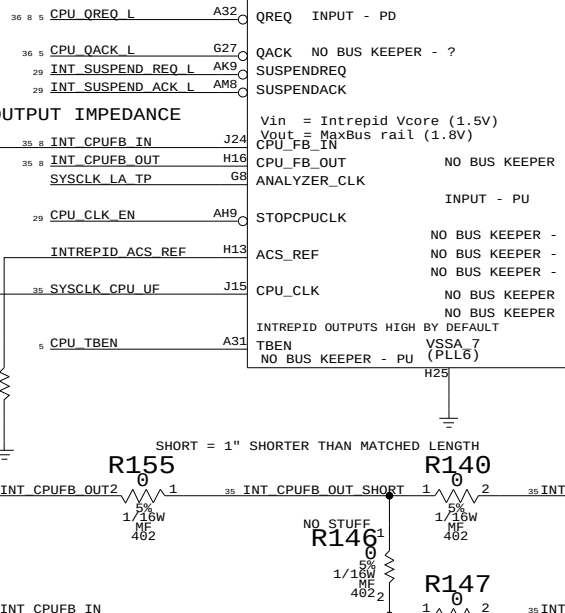
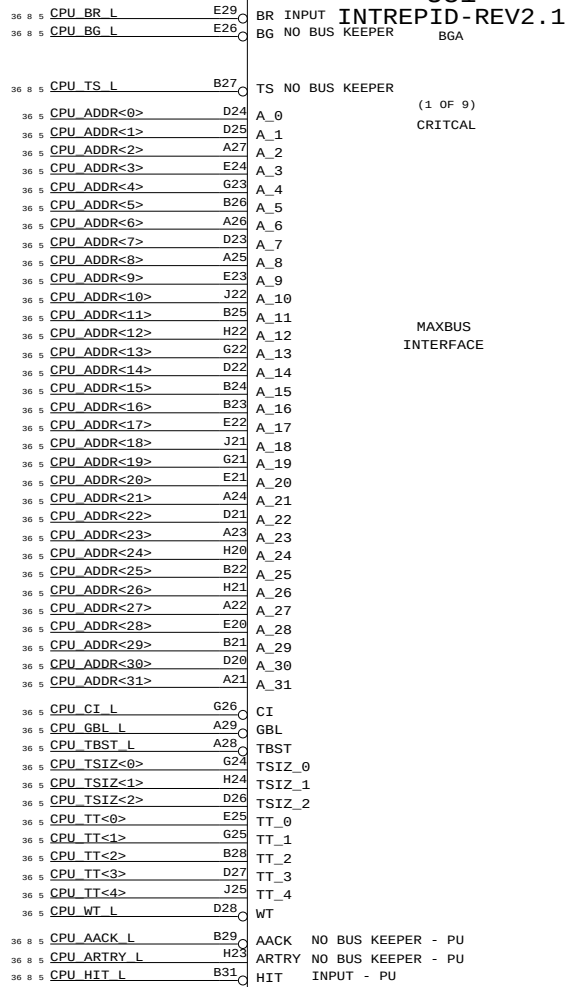
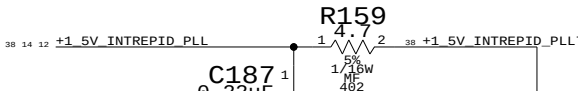
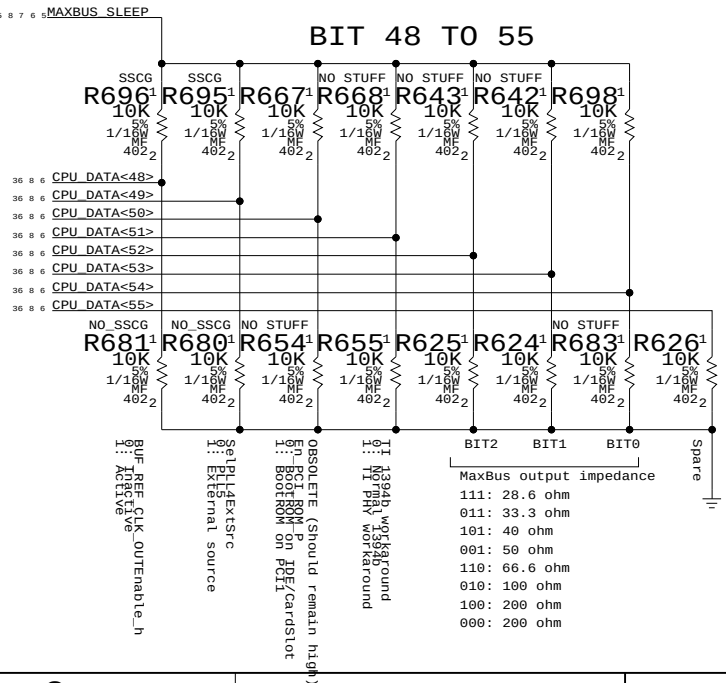
BIT 32 TO 39



BIT 40 TO 47



BIT 48 TO 55

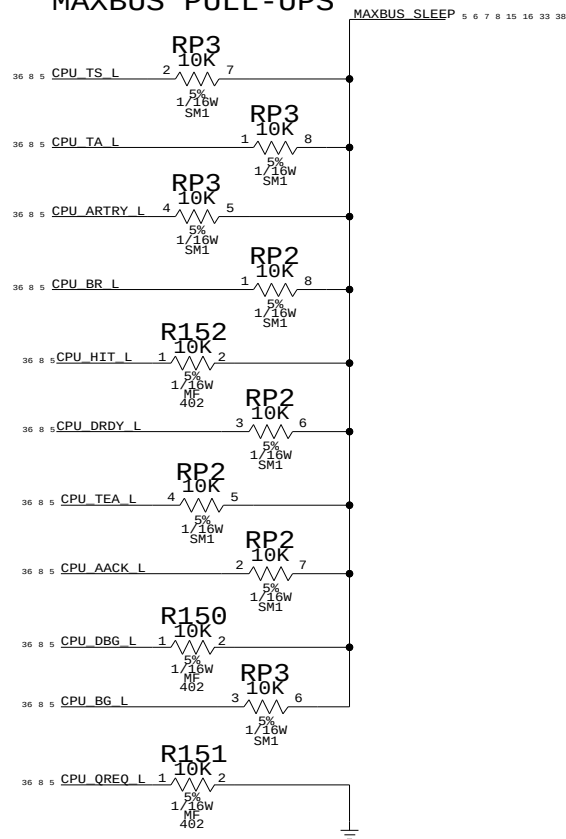


THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:

- 1/ D47 - SELAGSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 2/ D47 - SELAGSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
- 3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
- 4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
- 5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
- 6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

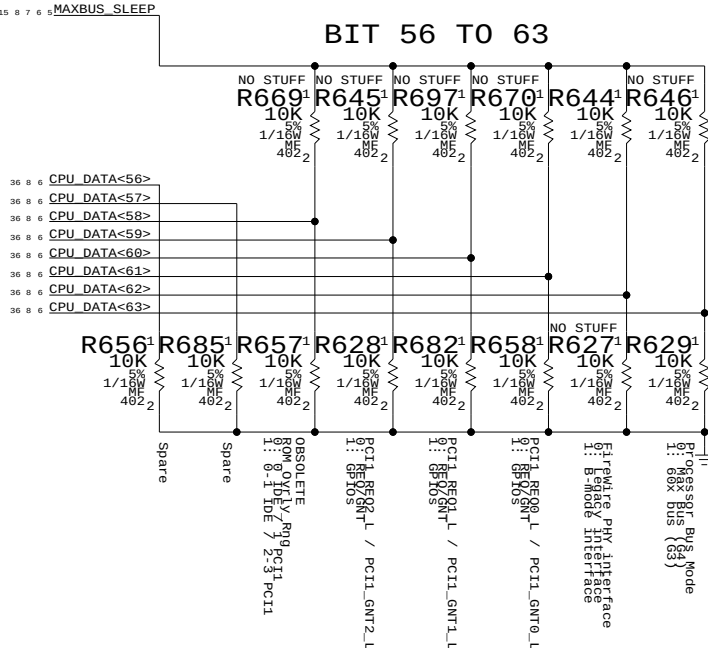
IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

MAXBUS PULL-UPS



INTREPID BOOT STRAPS

BIT 56 TO 63



Intrepid MaxBus

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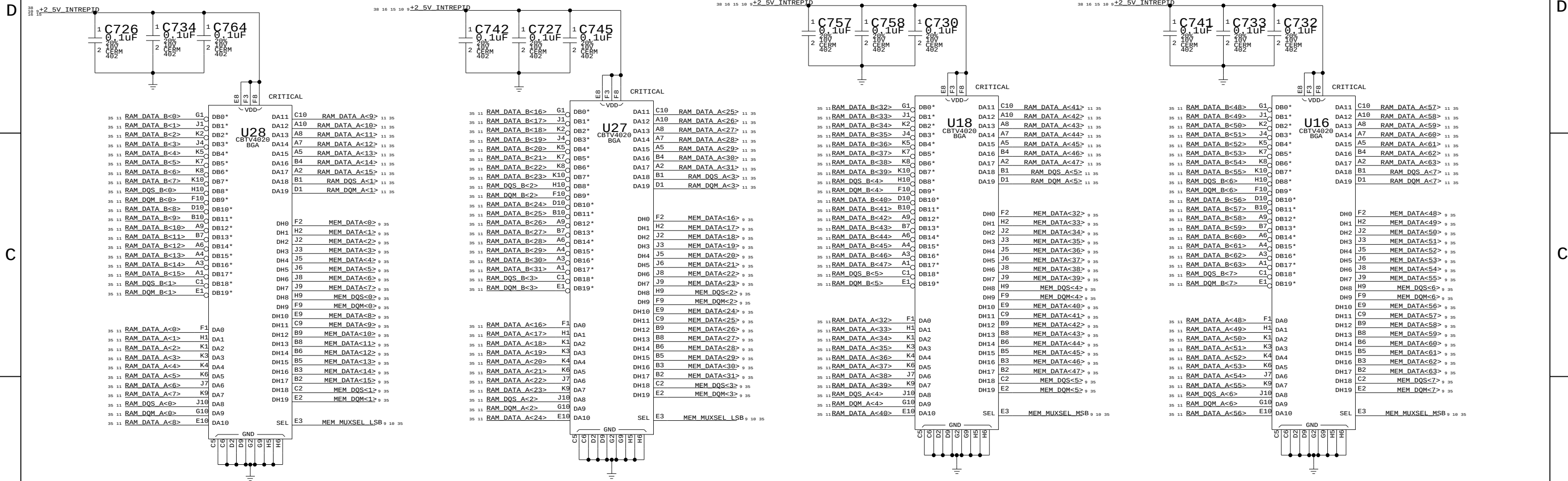
SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	8	44

BIT 0..15

BIT 16..31

BIT 32..47

BIT 48..63



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND

16BIT 2:1 DDR MUXES

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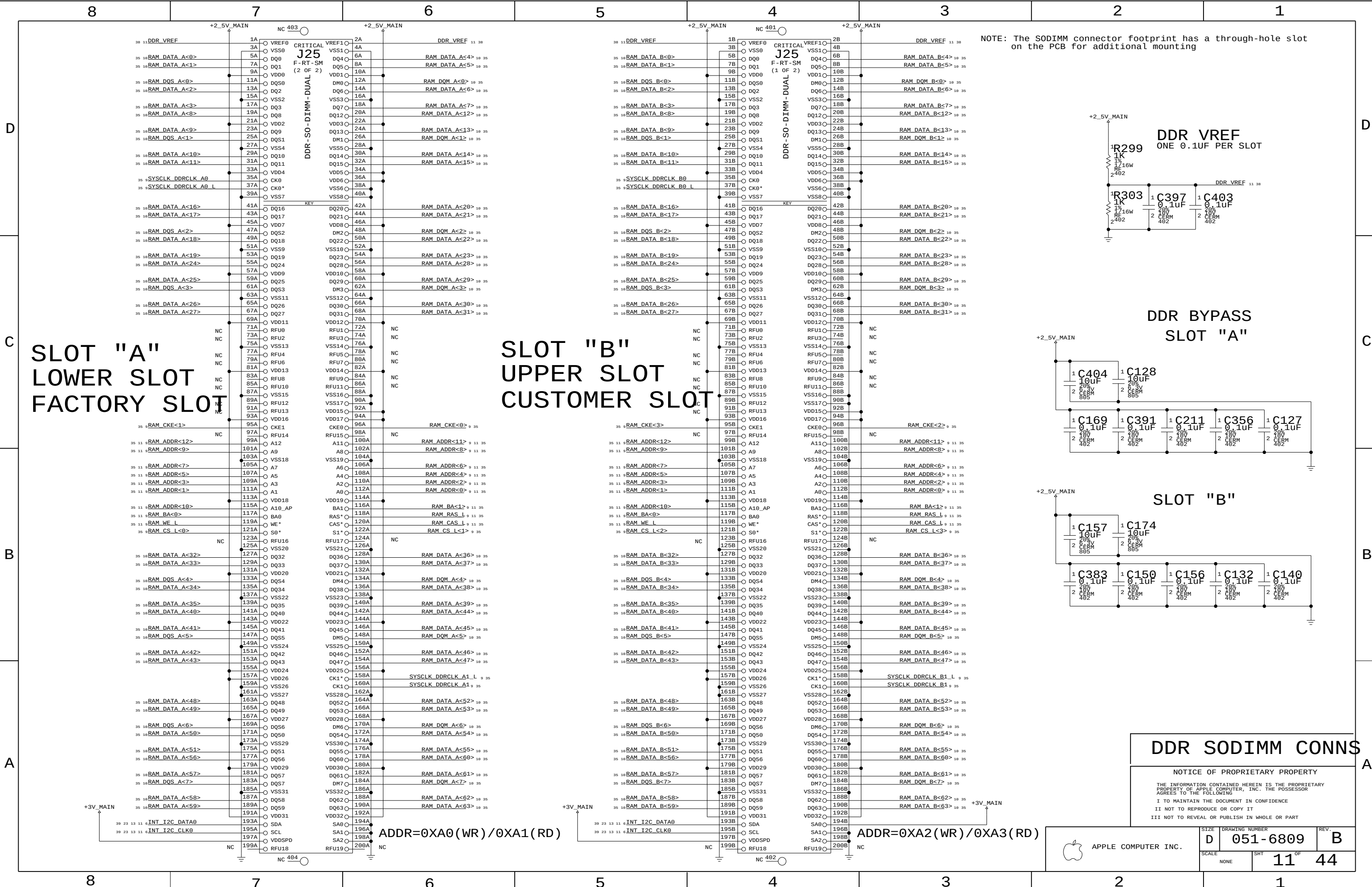
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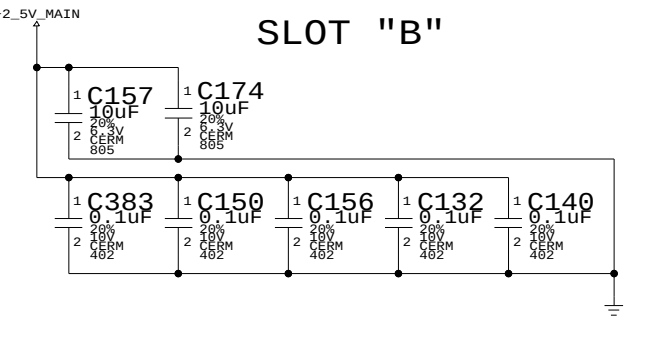
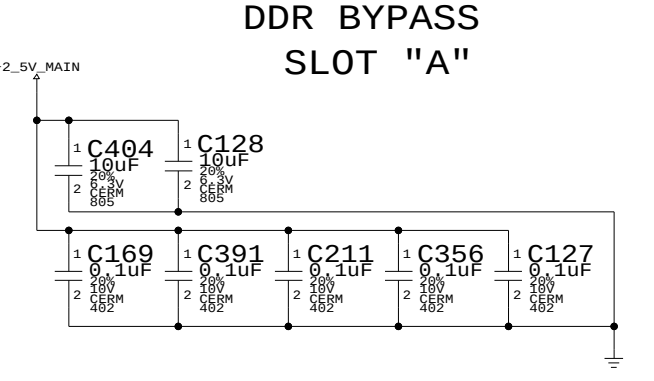
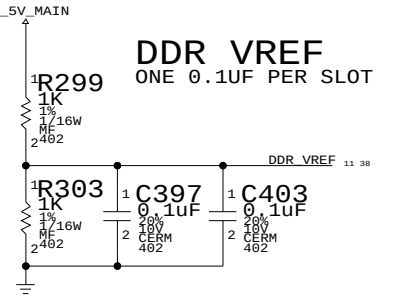
SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	10	44



SLOT "A"
LOWER SLOT
FACTORY SLOT

SLOT "B"
UPPER SLOT
CUSTOMER SLOT

NOTE: The SODIMM connector footprint has a through-hole slot on the PCB for additional mounting



DDR SODIMM CONNS

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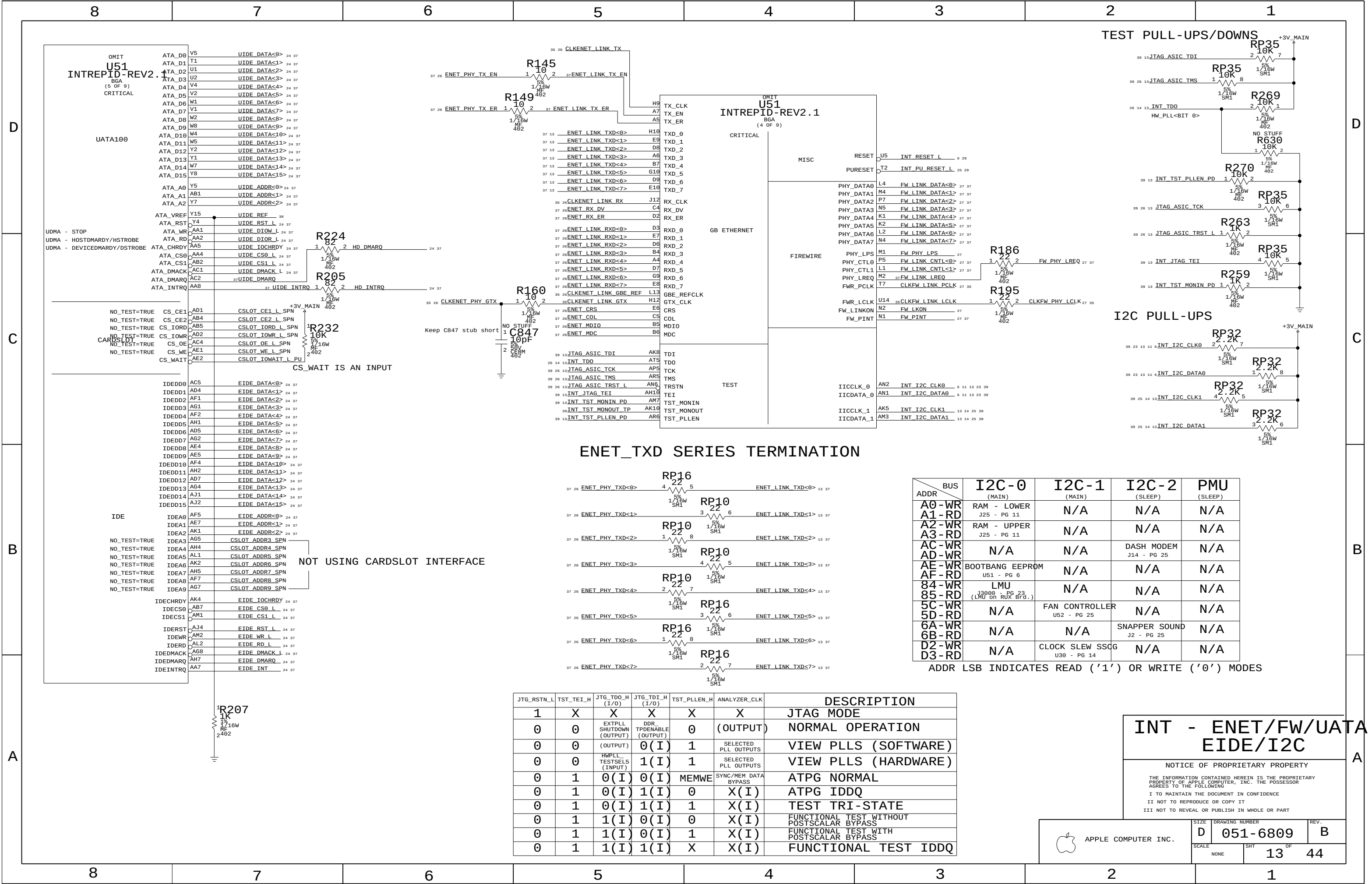
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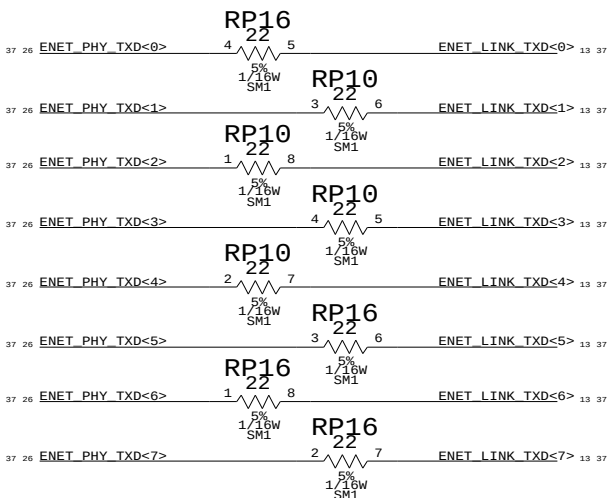
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 APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
	SCALE	SHT 11 ^{OF} 44	
	NONE		



ENET_TXD SERIES TERMINATION



BUS ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
	A0-WR A1-RD	A2-WR A3-RD	A4-WR A5-RD	A6-WR A7-RD
RAM - LOWER J25 - PG 11	N/A	N/A	N/A	N/A
RAM - UPPER J25 - PG 11	N/A	N/A	DASH MODEM J14 - PG 25	N/A
BOOTBANG EEPROM U51 - PG 6	N/A	N/A	N/A	N/A
LMU (LMU on RUX Brd.) J3000 - PG 23	N/A	N/A	N/A	N/A
FAN CONTROLLER U52 - PG 25	N/A	N/A	N/A	N/A
SNAPPER SOUND J2 - PG 25	N/A	N/A	N/A	N/A
CLOCK SLEW SSCG U30 - PG 14	N/A	N/A	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA
EIDE/I2C

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APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6809	REV. B
	SCALE NONE	SHT 13	OF 44



Intrepid Power

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SIZE	DRAWING NUMBER
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D

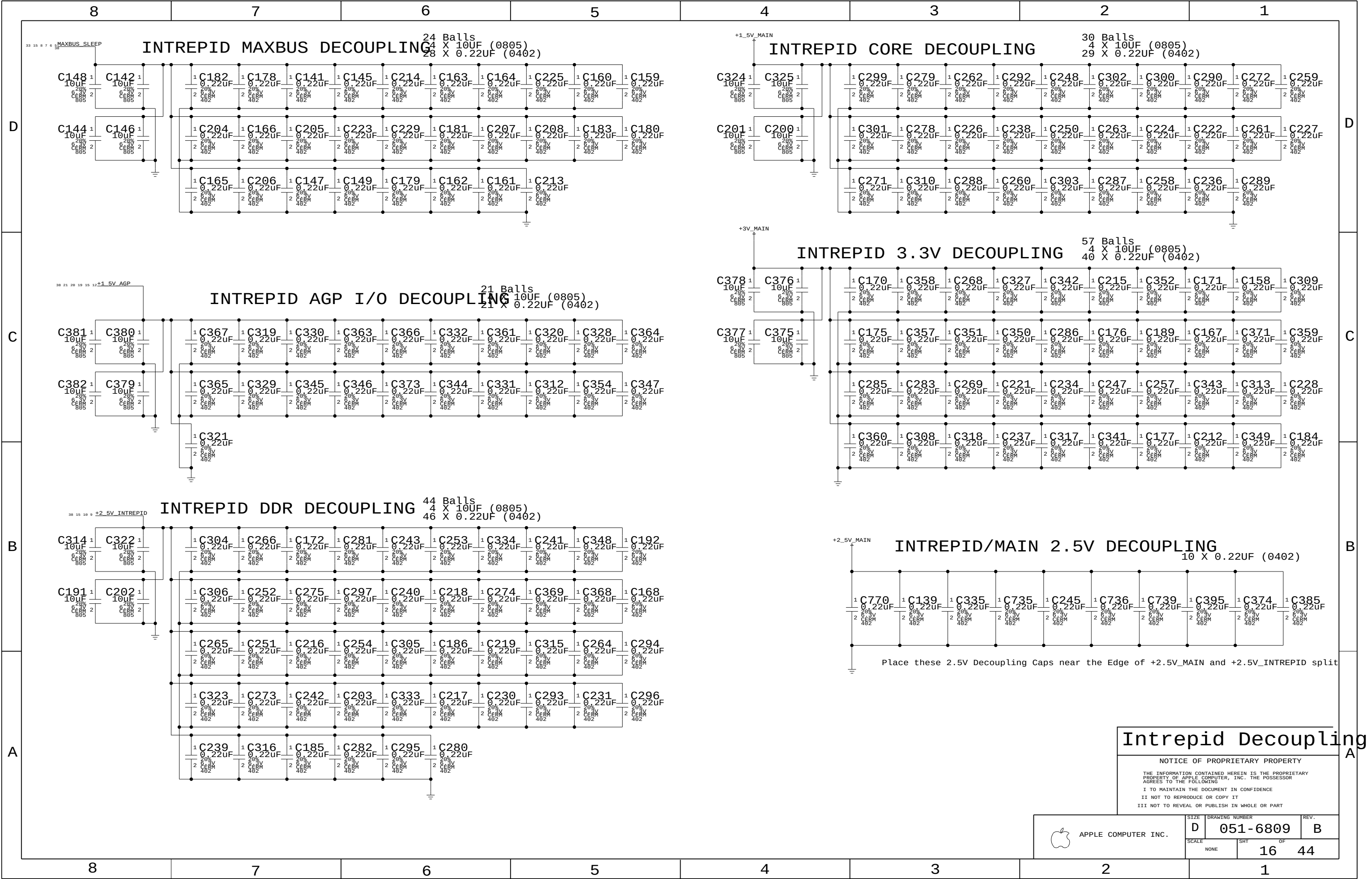
051-6809

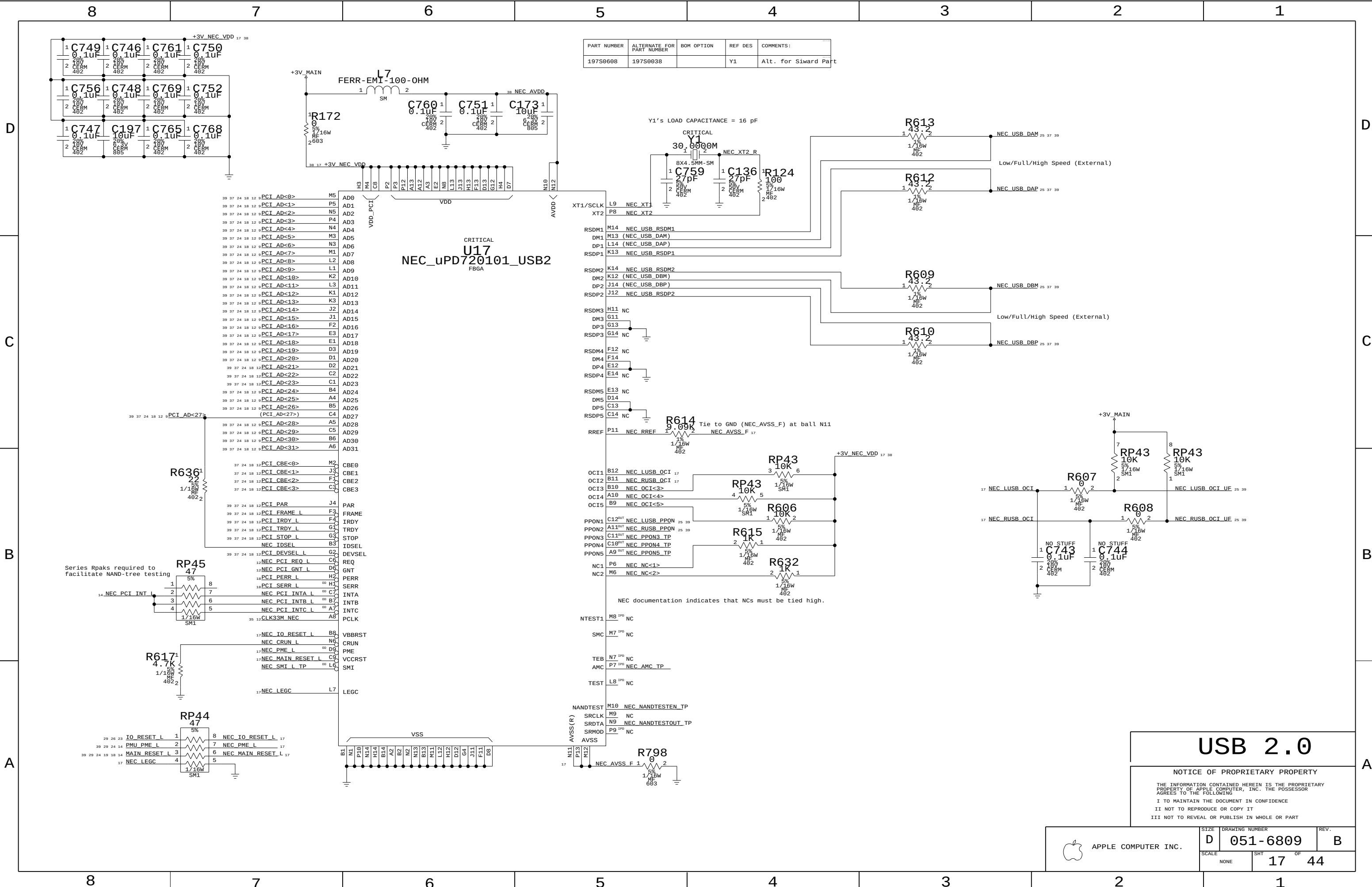
V.

SCALE	
	NON

SHT	
-----	--

44





PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038		Y1	Alt. for Siward Part

Y1's LOAD CAPACITANCE = 16 pF

XT1/SCLK
XT2

RSDM1
DM1
DP1
RSDP1

RSDM2
DM2
DP2
RSDP2

RSDM3
G11
DM3
DP3
RSDP3

RSDM4
F12
DM4
DP4
RSDP4

RSDM5
E13
DM5
DP5
RSDP5

RREF
P11

OC1
B12
OC2
B11
OC3
B10
OC4
B9
OC5
B9

PPON1
C12
PPON2
A11
PPON3
C11
PPON4
C10
PPON5
A9

NC1
P6
NC2
M6

NTST1
M8
SMC
M7
TEB
N7
AMC
P7
TEST
L8

NANDTEST
M10
SRCLK
M9
SRDTA
N9
SRMOD
P9
AVSS
P13

AVSS(R)
N11
N12

R798
17

NEC USB RSDM1
M13 (NEC_USB_DAM)
L14 (NEC_USB_DAP)
K13 NEC_USB_RSDP1

NEC USB RSDM2
K12 (NEC_USB_DBM)
J14 (NEC_USB_DBP)
J12 NEC_USB_RSDP2

NEC USB RSDM3
G11
DM3
DP3
RSDP3

NEC USB RSDM4
F12
DM4
DP4
RSDP4

NEC USB RSDM5
E13
DM5
DP5
RSDP5

NEC USB RSDM6
H11
DM6
DP6
RSDP6

NEC USB RSDM7
I11
DM7
DP7
RSDP7

NEC USB RSDM8
J11
DM8
DP8
RSDP8

NEC USB RSDM9
K11
DM9
DP9
RSDP9

NEC USB RSDM10
L11
DM10
DP10
RSDP10

NEC USB RSDM11
M11
DM11
DP11
RSDP11

NEC USB RSDM12
N11
DM12
DP12
RSDP12

NEC USB RSDM13
O11
DM13
DP13
RSDP13

NEC USB RSDM14
P11
DM14
DP14
RSDP14

NEC USB RSDM15
Q11
DM15
DP15
RSDP15

NEC USB RSDM16
R11
DM16
DP16
RSDP16

NEC USB RSDM17
S11
DM17
DP17
RSDP17

NEC USB RSDM18
T11
DM18
DP18
RSDP18

NEC USB RSDM19
U11
DM19
DP19
RSDP19

NEC USB RSDM20
V11
DM20
DP20
RSDP20

NEC USB RSDM21
W11
DM21
DP21
RSDP21

NEC USB RSDM22
X11
DM22
DP22
RSDP22

NEC USB RSDM23
Y11
DM23
DP23
RSDP23

NEC USB RSDM24
Z11
DM24
DP24
RSDP24

NEC USB RSDM25
AA11
DM25
DP25
RSDP25

NEC USB RSDM26
AB11
DM26
DP26
RSDP26

NEC USB RSDM27
AC11
DM27
DP27
RSDP27

NEC USB RSDM28
AD11
DM28
DP28
RSDP28

NEC USB RSDM29
AE11
DM29
DP29
RSDP29

NEC USB RSDM30
AF11
DM30
DP30
RSDP30

NEC USB RSDM31
AG11
DM31
DP31
RSDP31

NEC USB RSDM32
AH11
DM32
DP32
RSDP32

NEC USB RSDM33
AI11
DM33
DP33
RSDP33

NEC USB RSDM34
AJ11
DM34
DP34
RSDP34

NEC USB RSDM35
AK11
DM35
DP35
RSDP35

NEC USB RSDM36
AL11
DM36
DP36
RSDP36

NEC USB RSDM37
AM11
DM37
DP37
RSDP37

NEC USB RSDM38
AN11
DM38
DP38
RSDP38

NEC USB RSDM39
AO11
DM39
DP39
RSDP39

NEC USB RSDM40
AP11
DM40
DP40
RSDP40

NEC USB RSDM41
AQ11
DM41
DP41
RSDP41

NEC USB RSDM42
AR11
DM42
DP42
RSDP42

NEC USB RSDM43
AS11
DM43
DP43
RSDP43

NEC USB RSDM44
AT11
DM44
DP44
RSDP44

NEC USB RSDM45
AU11
DM45
DP45
RSDP45

NEC USB RSDM46
AV11
DM46
DP46
RSDP46

NEC USB RSDM47
AW11
DM47
DP47
RSDP47

NEC USB RSDM48
AX11
DM48
DP48
RSDP48

NEC USB RSDM49
AY11
DM49
DP49
RSDP49

NEC USB RSDM50
AZ11
DM50
DP50
RSDP50

NEC USB RSDM51
BA11
DM51
DP51
RSDP51

NEC USB RSDM52
BB11
DM52
DP52
RSDP52

NEC USB RSDM53
BC11
DM53
DP53
RSDP53

NEC USB RSDM54
BD11
DM54
DP54
RSDP54

NEC USB RSDM55
BE11
DM55
DP55
RSDP55

NEC USB RSDM56
BF11
DM56
DP56
RSDP56

NEC USB RSDM57
BG11
DM57
DP57
RSDP57

NEC USB RSDM58
BH11
DM58
DP58
RSDP58

NEC USB RSDM59
BG11
DM59
DP59
RSDP59

NEC USB RSDM60
BH11
DM60
DP60
RSDP60

NEC USB RSDM61
BI11
DM61
DP61
RSDP61

NEC USB RSDM62
BJ11
DM62
DP62
RSDP62

NEC USB RSDM63
BK11
DM63
DP63
RSDP63

NEC USB RSDM64
BL11
DM64
DP64
RSDP64

NEC USB RSDM65
BM11
DM65
DP65
RSDP65

NEC USB RSDM66
BN11
DM66
DP66
RSDP66

NEC USB RSDM67
BO11
DM67
DP67
RSDP67

NEC USB RSDM68
BP11
DM68
DP68
RSDP68

NEC USB RSDM69
BQ11
DM69
DP69
RSDP69

NEC USB RSDM70
BR11
DM70
DP70
RSDP70

NEC USB RSDM71
BS11
DM71
DP71
RSDP71

NEC USB RSDM72
BT11
DM72
DP72
RSDP72

NEC USB RSDM73
BU11
DM73
DP73
RSDP73

NEC USB RSDM74
BV11
DM74
DP74
RSDP74

NEC USB RSDM75
BW11
DM75
DP75
RSDP75

NEC USB RSDM76
BX11
DM76
DP76
RSDP76

NEC USB RSDM77
BY11
DM77
DP77
RSDP77

NEC USB RSDM78
BZ11
DM78
DP78
RSDP78

NEC USB RSDM79
CA11
DM79
DP79
RSDP79

NEC USB RSDM80
CB11
DM80
DP80
RSDP80

NEC USB RSDM81
CC11
DM81
DP81
RSDP81

NEC USB RSDM82
CD11
DM82
DP82
RSDP82

NEC USB RSDM83
CE11
DM83
DP83
RSDP83

NEC USB RSDM84
CF11
DM84
DP84
RSDP84

NEC USB RSDM85
CG11
DM85
DP85
RSDP85

NEC USB RSDM86
CH11
DM86
DP86
RSDP86

NEC USB RSDM87
CG11
DM87
DP87
RSDP87

NEC USB RSDM88
CH11
DM88
DP88
RSDP88

NEC USB RSDM89
CI11
DM89
DP89
RSDP89

NEC USB RSDM90
CJ11
DM90
DP90
RSDP90

NEC USB RSDM91
CK11
DM91
DP91
RSDP91

NEC USB RSDM92
CL11
DM92
DP92
RSDP92

NEC USB RSDM93
CM11
DM93
DP93
RSDP93

NEC USB RSDM94
CN11
DM94
DP94
RSDP94

NEC USB RSDM95
CO11
DM95
DP95
RSDP95

NEC USB RSDM96
CP11
DM96
DP96
RSDP96

NEC USB RSDM97
CQ11
DM97
DP97
RSDP97

NEC USB RSDM98
CR11
DM98
DP98
RSDP98

NEC USB RSDM99
CS11
DM99
DP99
RSDP99

NEC USB RSDM100
CT11
DM100
DP100
RSDP100

NEC USB RSDM101
CU11
DM101
DP101
RSDP101

NEC USB RSDM102
CV11
DM102
DP102
RSDP102

NEC USB RSDM103
CW11
DM103
DP103
RSDP103

NEC USB RSDM104
CX11
DM104
DP104
RSDP104

NEC USB RSDM105
CY11
DM105
DP105
RSDP105

NEC USB RSDM106
CZ11
DM106
DP106
RSDP106

NEC USB RSDM107
DA11
DM107
DP107
RSDP107

NEC USB RSDM108
DB11
DM108
DP108
RSDP108

NEC USB RSDM109
DC11
DM109
DP109
RSDP109

NEC USB RSDM110
DD11
DM110
DP110
RSDP110

NEC USB RSDM111
DE11
DM111
DP111
RSDP111

NEC USB RSDM112
DD11
DM112
DP112
RSDP112

NEC USB RSDM113
DE11
DM113
DP113
RSDP113

NEC USB RSDM114
DF11
DM114
DP114
RSDP114

NEC USB RSDM115
DG11
DM115
DP115
RSDP115

NEC USB RSDM116
DH11
DM116
DP116
RSDP116

NEC USB RSDM117
DG11
DM117
DP117
RSDP117

NEC USB RSDM118
DH11
DM118
DP118
RSDP118

NEC USB RSDM119
DI11
DM119
DP119
RSDP119

NEC USB RSDM120
DJ11
DM120
DP120
RSDP120

NEC USB RSDM121
DK11
DM121
DP121
RSDP121

NEC USB RSDM122
DL11
DM122
DP122
RSDP122

NEC USB RSDM123
DM11
DM123
DP123
RSDP123

NEC USB RSDM124
DN11
DM124
DP124
RSDP124

NEC USB RSDM125
DO11
DM125
DP125
RSDP125

NEC USB RSDM126
DP11
DM126
DP126
RSDP126

NEC USB RSDM127
DQ11
DM127
DP127
RSDP127

NEC USB RSDM128
DR11
DM128
DP128
RSDP128

NEC USB RSDM129
DS11
DM129
DP129
RSDP129

NEC USB RSDM130
DT11
DM130
DP130
RSDP130

NEC USB RSDM131
DU11
DM131
DP131
RSDP131

NEC USB RSDM132
DV11
DM132
DP132
RSDP132

NEC USB RSDM133
DW11
DM133
DP133
RSDP133

NEC USB RSDM134
DX11
DM134
DP134
RSDP134

NEC USB RSDM135
DY11
DM135
DP135
RSDP135

NEC USB RSDM136
DZ11
DM136
DP136
RSDP136

NEC USB RSDM137
EA11
DM137
DP137
RSDP137

NEC USB RSDM138
EB11
DM138
DP138
RSDP138

NEC USB RSDM139
EC11
DM139
DP139
RSDP139

NEC USB RSDM140
ED11
DM140
DP140
RSDP140

NEC USB RSDM141
EE11
DM141
DP141
RSDP141

NEC USB RSDM142
EF11
DM142
DP142
RSDP142

NEC USB RSDM143
EG11
DM143
DP143
RSDP143

NEC USB RSDM144
EH11
DM144
DP144
RSDP144

NEC USB RSDM145
EG11
DM145
DP145
RSDP145

NEC USB RSDM146
EH11
DM146
DP146
RSDP146

NEC USB RSDM147
EI11
DM147
DP147
RSDP147

NEC USB RSDM148
EJ11
DM148
DP148
RSDP148

NEC USB RSDM149
EK11
DM149
DP149
RSDP149

NEC USB RSDM150
EL11
DM150
DP150
RSDP150

NEC USB RSDM151
EM11
DM151
DP151
RSDP151

NEC USB RSDM152
EN11
DM152
DP152
RSDP152

NEC USB RSDM153
EO11
DM153
DP153
RSDP153

NEC USB RSDM154
EP11
DM154
DP154
RSDP154

NEC USB RSDM155
EQ11
DM155
DP155
RSDP155

NEC USB RSDM156
ER11
DM156
DP156
RSDP156

NEC USB RSDM157
ES11
DM157
DP157
RSDP157

NEC USB RSDM158
ET11
DM158
DP158
RSDP158

NEC USB RSDM159
EU11
DM159
DP159
RSDP159

NEC USB RSDM160
EV11
DM160
DP160
RSDP160

NEC USB RSDM161
EW11
DM161
DP161
RSDP161

NEC USB RSDM162
EX11
DM162
DP162
RSDP162

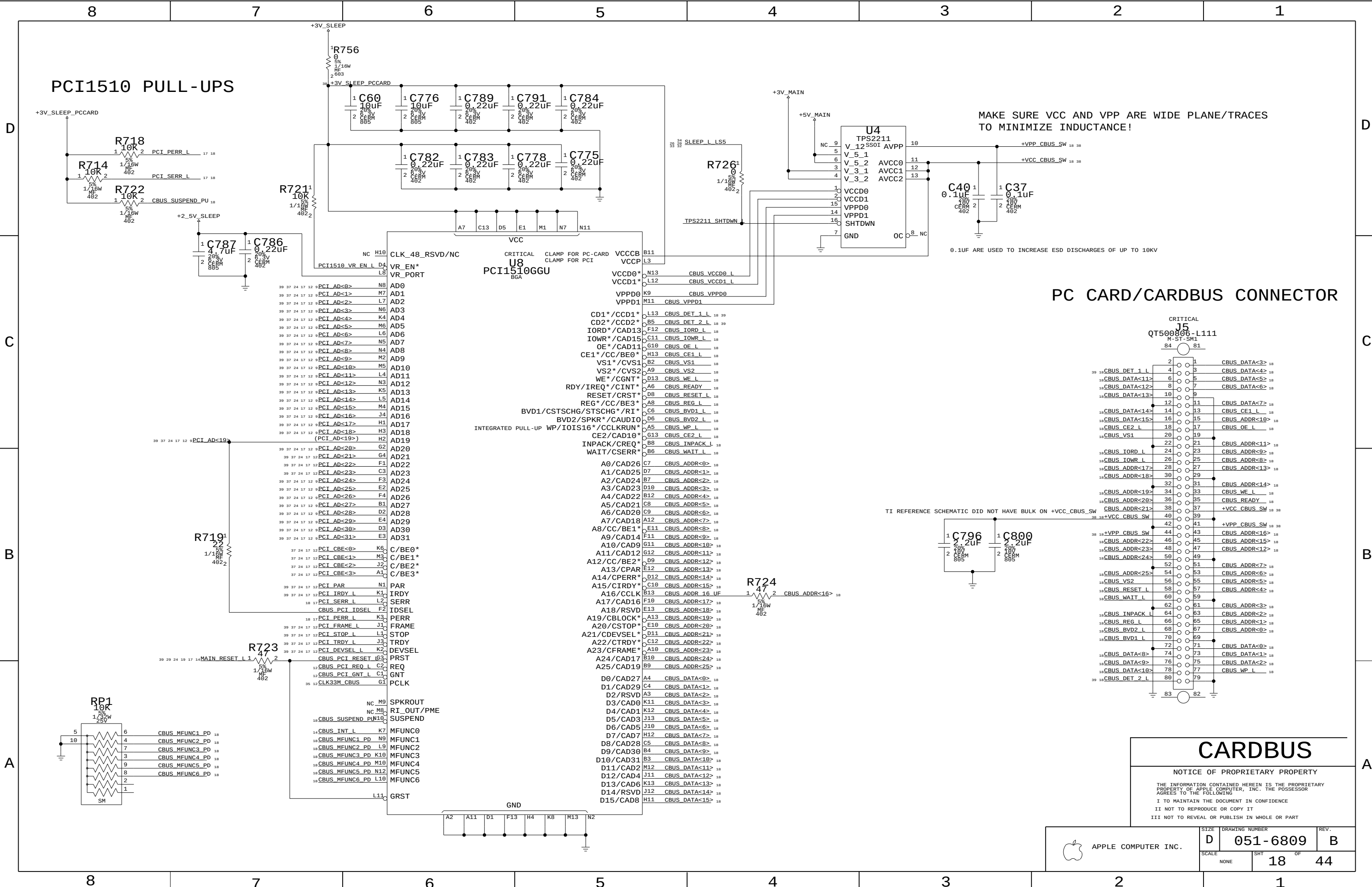
NEC USB RSDM163
EY11
DM163
DP163
RSDP163

NEC USB RSDM164
EZ11
DM164
DP164
RSDP164

NEC USB RSDM165
FA11
DM165
DP165
RSDP165

NEC USB RSDM166
FB11
DM166
DP166
RSDP166

NEC USB RSDM167
FC11
DM167
DP167
RSDP167



PC CARD/CARDBUS CONNECTOR

CARDBUS

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APPLE COMPUTER INC.

SIZE DRAWING NUMBER REV.

D

051-6809

B

SCALE

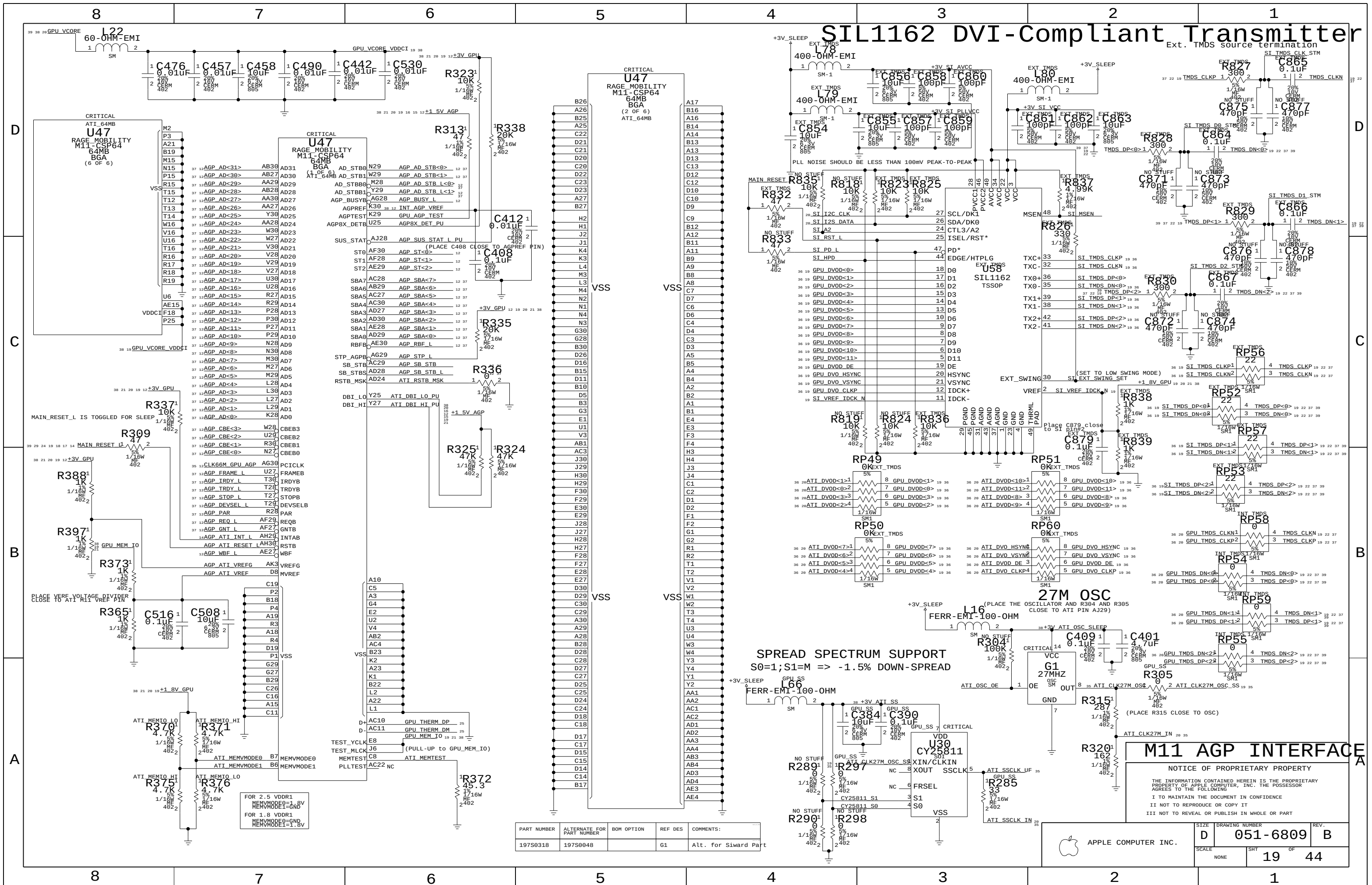
NONE

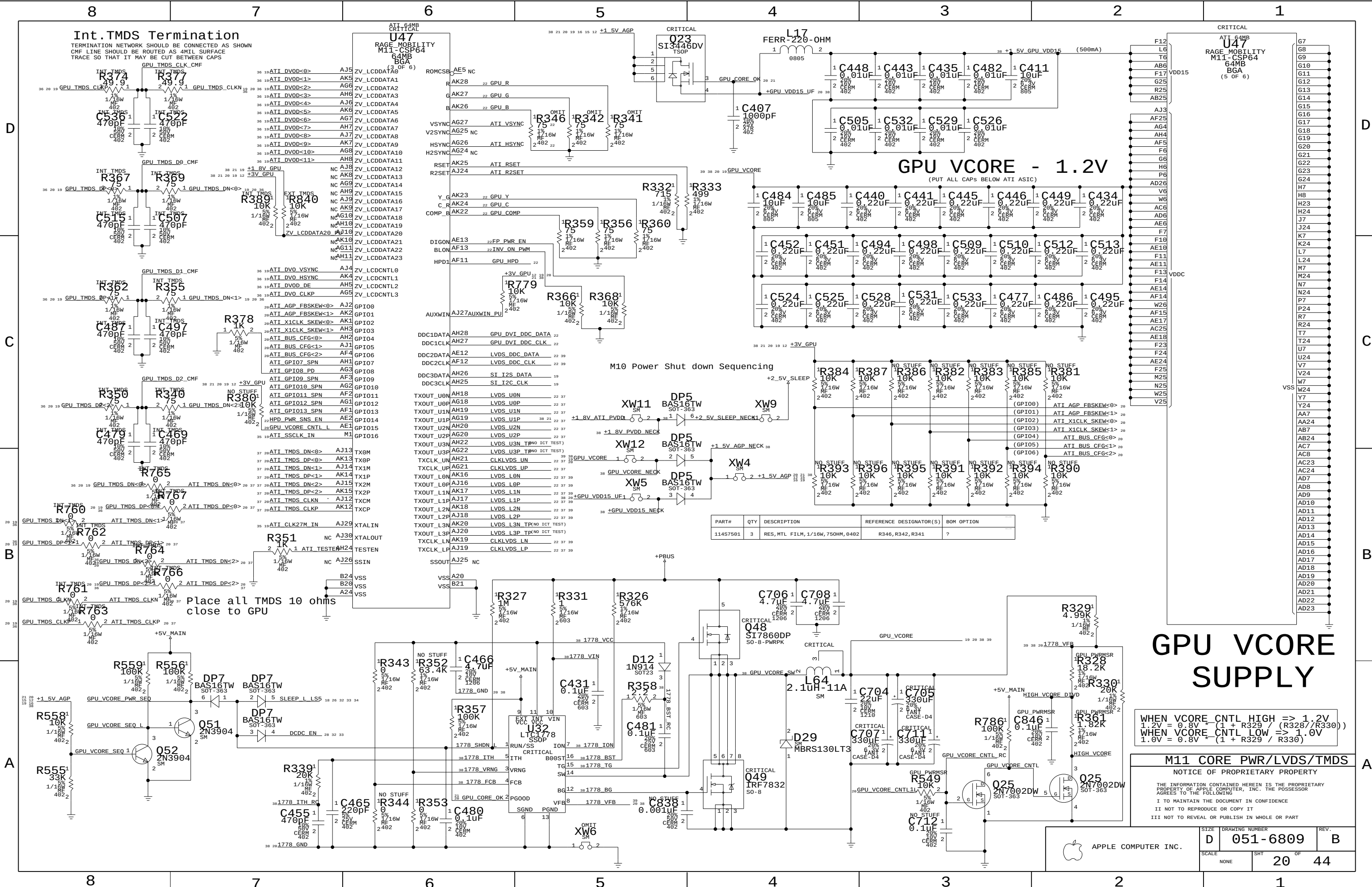
SHT

18

OF

44





Int.TMDS Termination
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS

GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATT ASIC)

**GPU VCORE
SUPPLY**

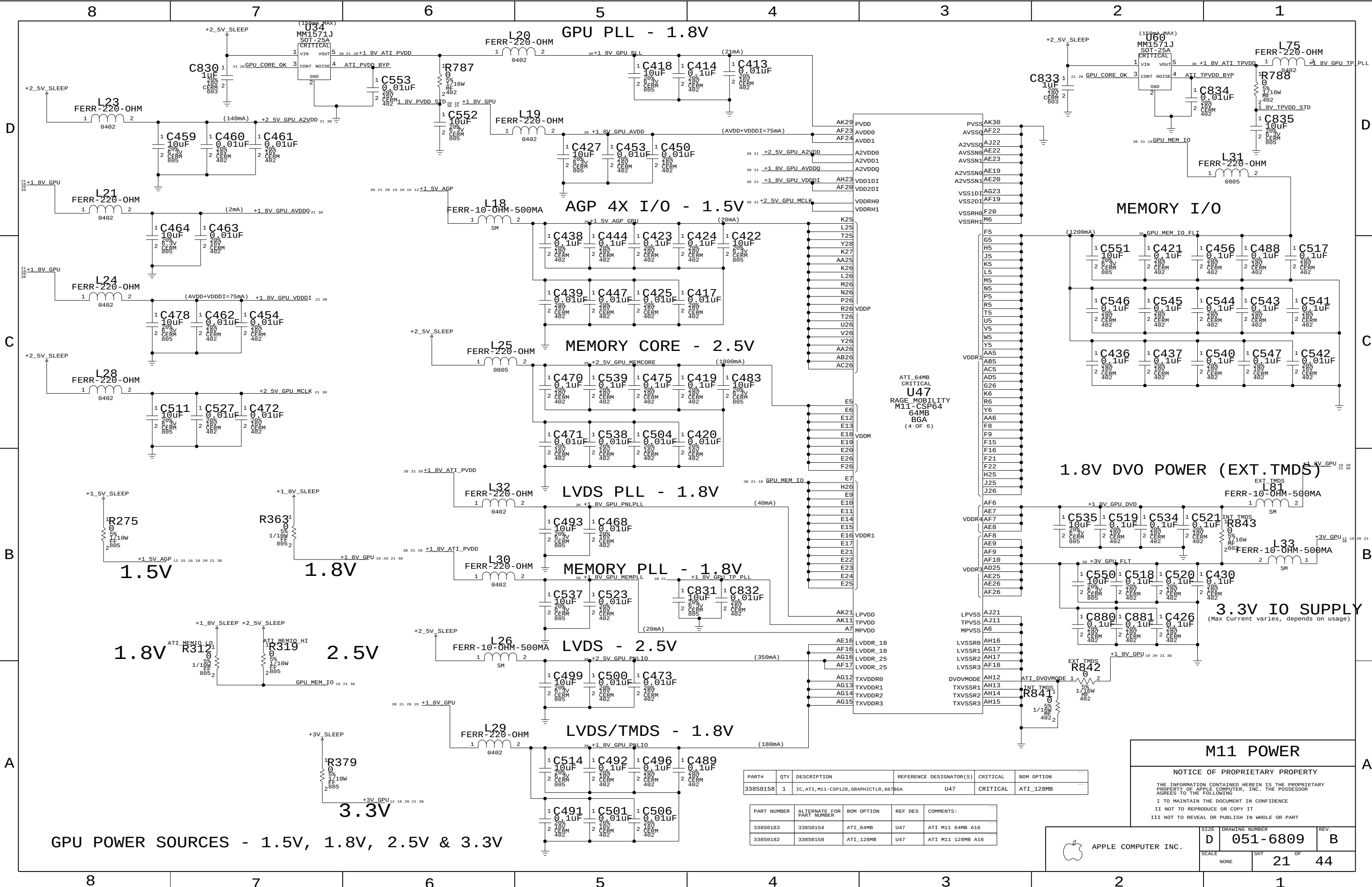
WHEN VCORE_CNTL HIGH => 1.2V
 $1.2V = 0.8V \cdot (1 + R329 / (R328 / R330))$
WHEN VCORE_CNTL LOW => 1.0V
 $1.0V = 0.8V \cdot (1 + R329 / R330)$

M11 CORE PWR/LVDS/TMDS
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE	SHT		OF
	20		44

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
11457501	3	RES,MTL FILM,1/16W,750HM,0402	R346,R342,R341	?



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC, ATI, M11-CSP128, GRAPHIC128, 667BGA	U47	CRITICAL	ATI_128MB

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0183	338S0154	ATI_64MB	U47	ATI M11 64MB A16
338S0182	338S0158	ATI_128MB	U47	ATI M11 128MB A16

M11 POWER

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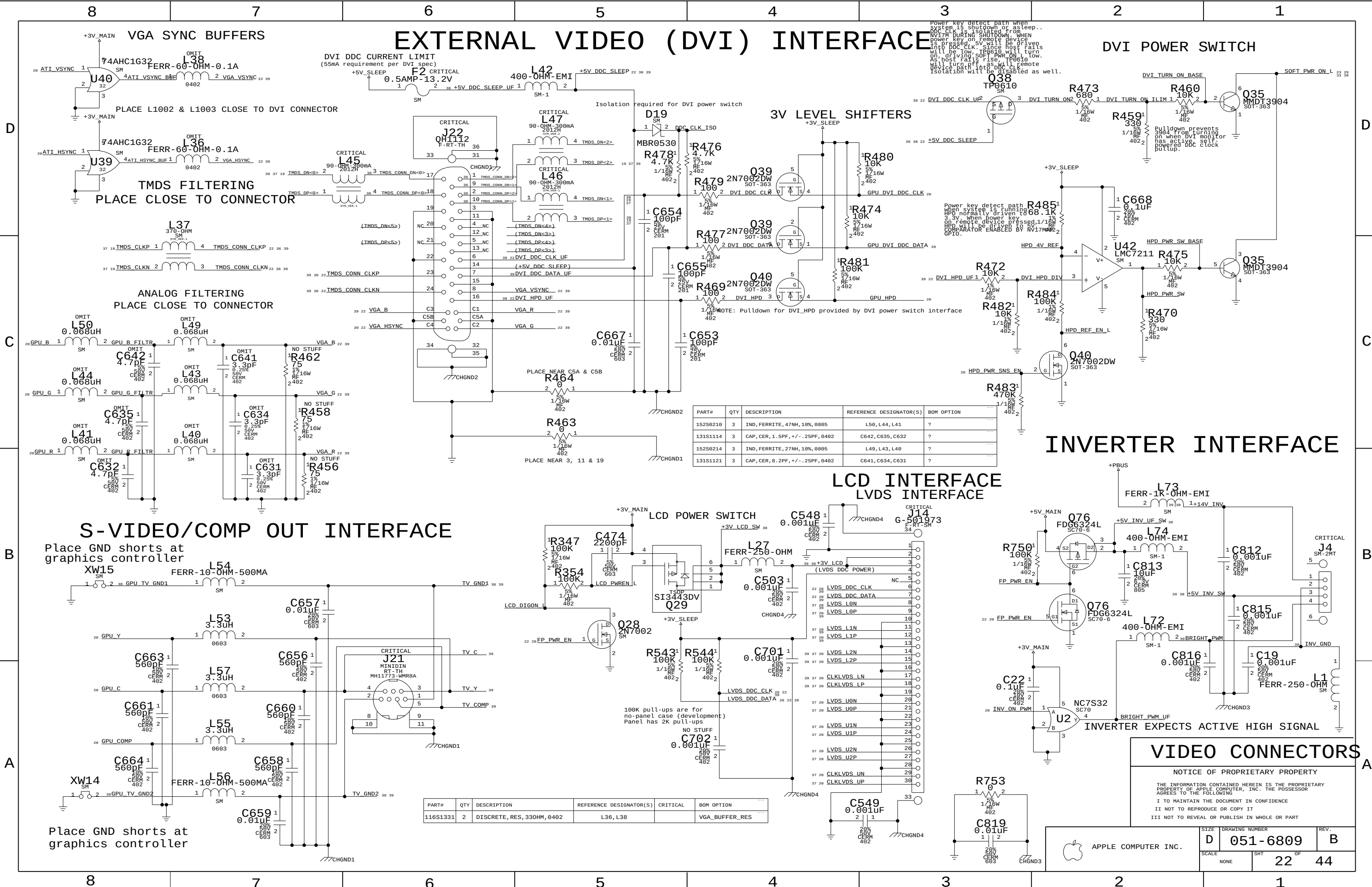
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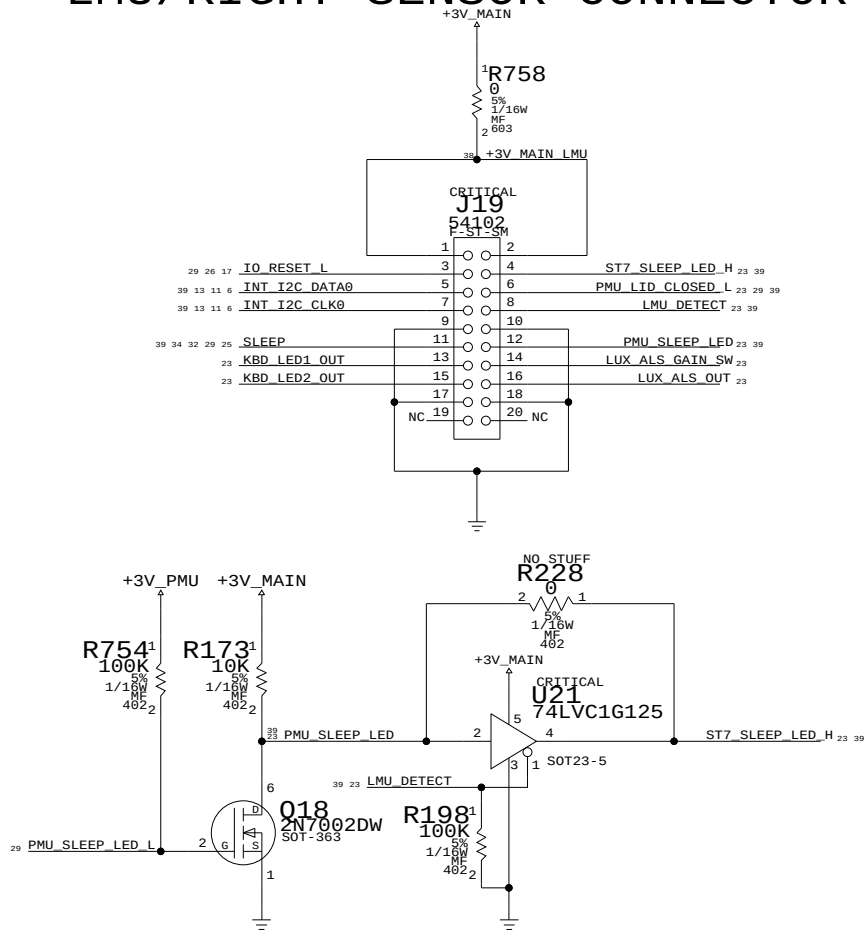
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE	NONE	SHT	21 OF 44

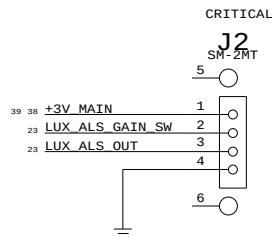
EXTERNAL VIDEO (DVI) INTERFACE



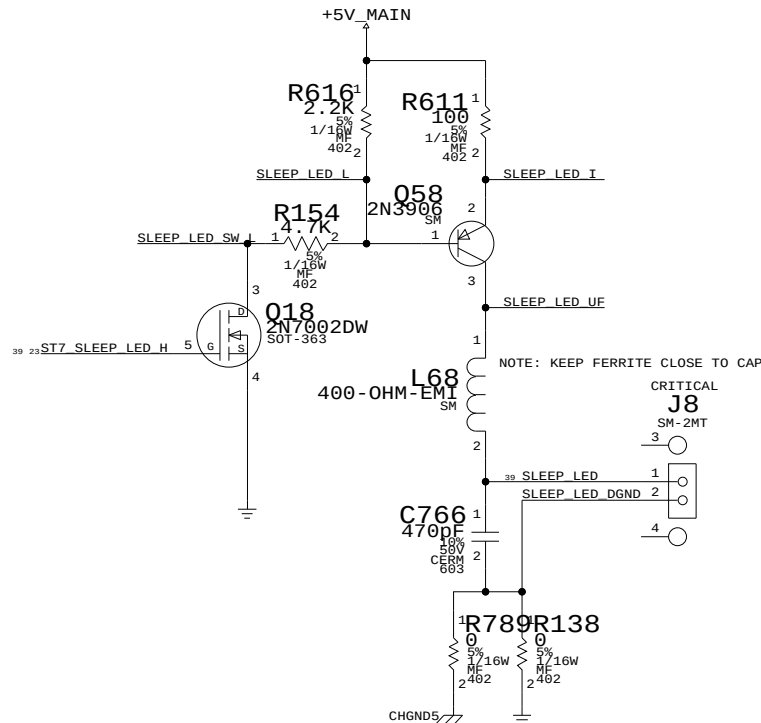
LMU/RIGHT SENSOR CONNECTOR



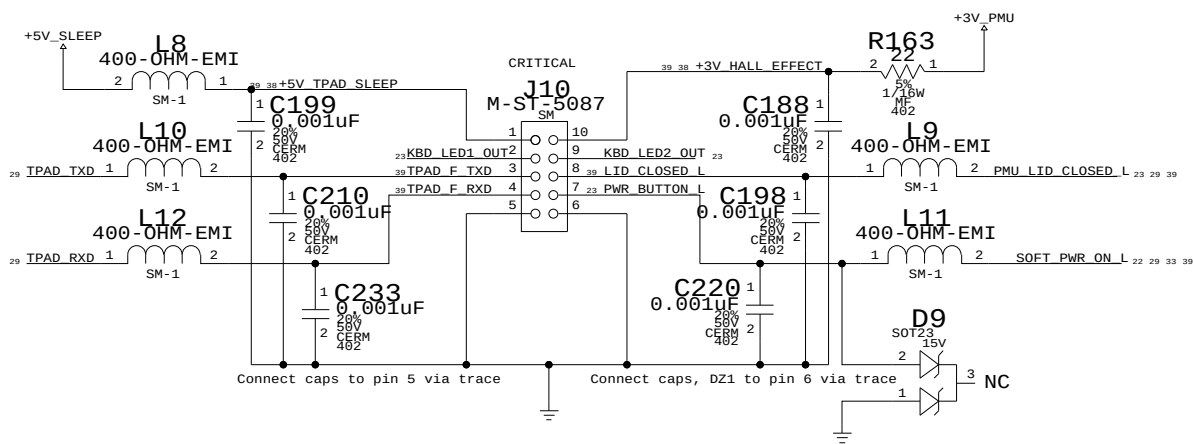
LEFT LIGHT SENSOR CONNECTOR



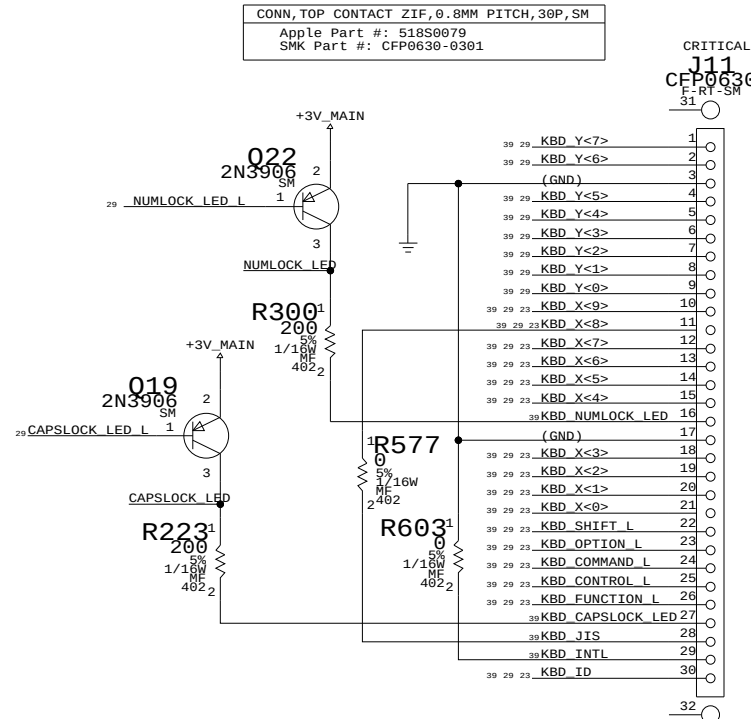
SLEEP LED



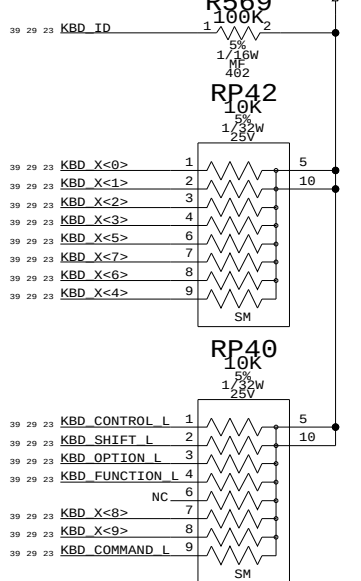
TRACKPAD/PWR BTN CONN



TOP CONTACT ZIF KEYBOARD CONN



KEYBOARD PULLUPS



KEYBOARD/TPAD/SLEEP LED

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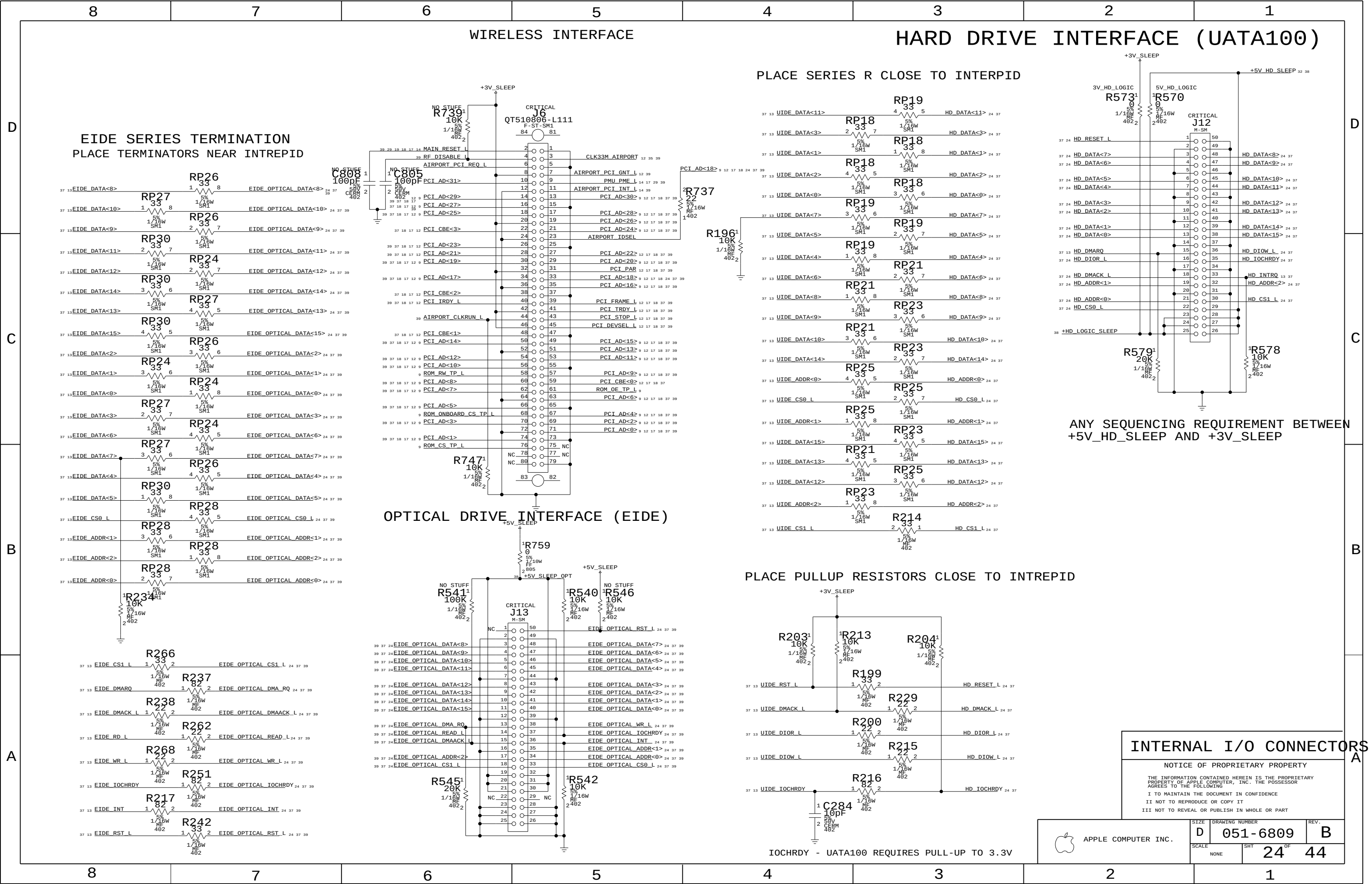
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE		SHT	OF
NONE		23	44





8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---



C



A	PLACE CLOSE TO BATTERY CHARGER/VCORE ALTERNATE2
---	--



8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

D



B



GPU FAN



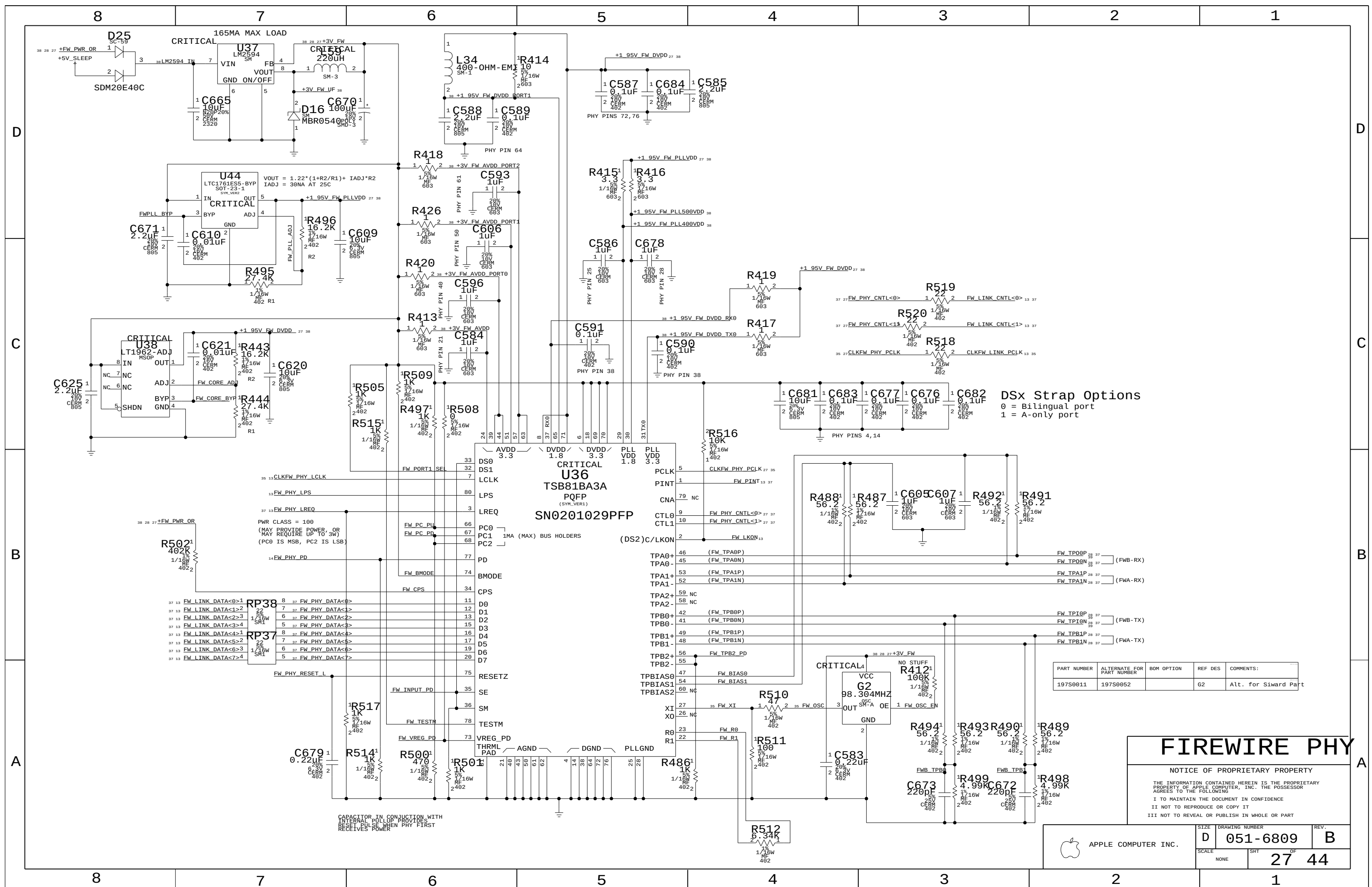
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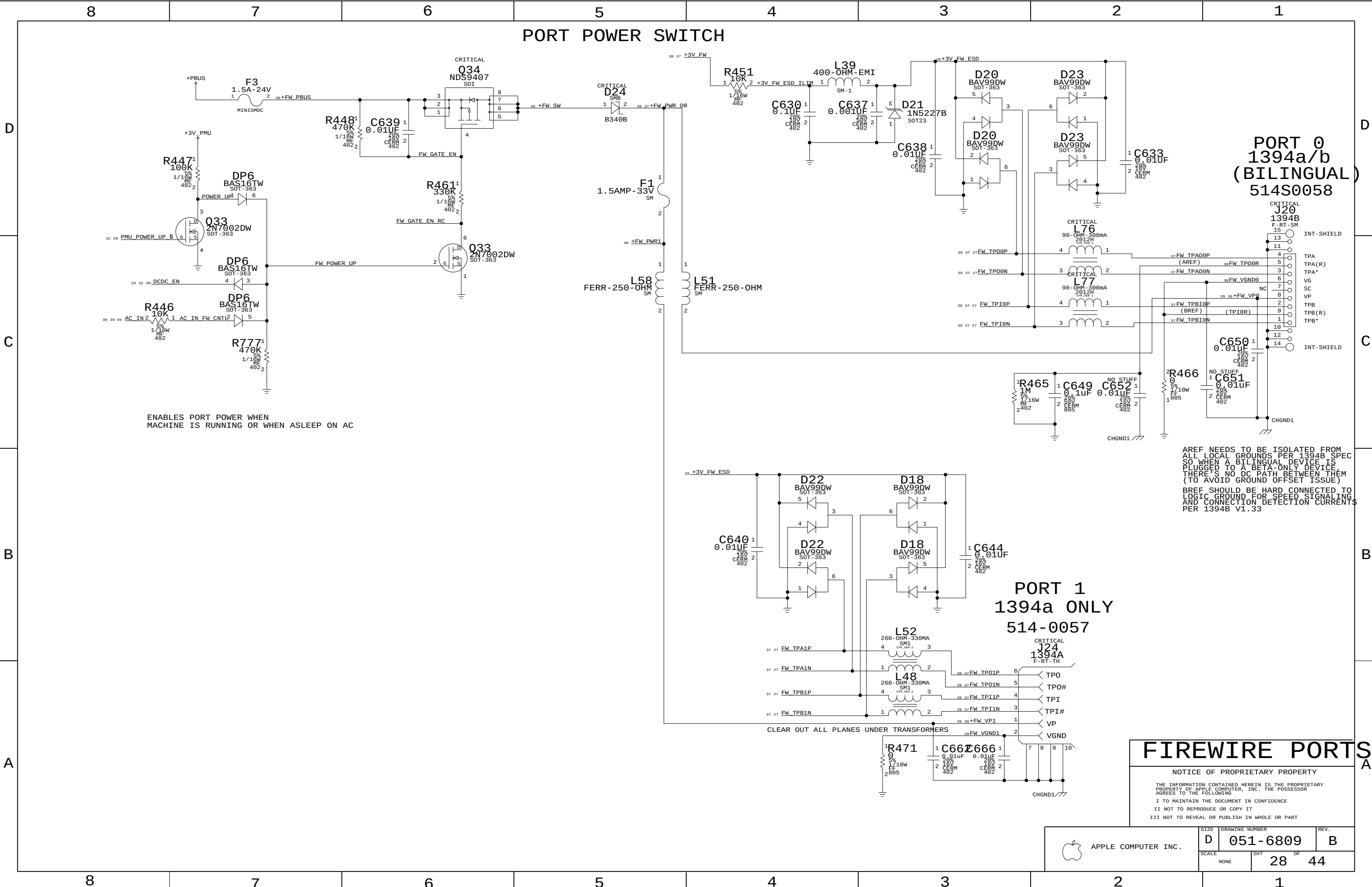
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SIZE D	DRAWING NUMBER 051-6809	REV. B
SCALE NONE	SHT 25 OF 44	





ENABLES PORT POWER WHEN
MACHINE IS RUNNING OR WHEN ASLEEP ON AC

AREF NEEDS TO BE ISOLATED FROM
ALL LOCAL GROUNDS PER 1394B SPEC
SO WHEN A BILINGUAL DEVICE IS
PLUGGED TO A BETA-ONLY DEVICE
THERE'S NO DC PATH BETWEEN THEM
(TO AVOID GROUND OFFSET ISSUE)
BREF SHOULD BE HARD CONNECTED TO
LOGIC GROUND FOR SPEED SIGNALING
AND CONNECTION DETECTION CURRENTS
PER 1394B V1.33

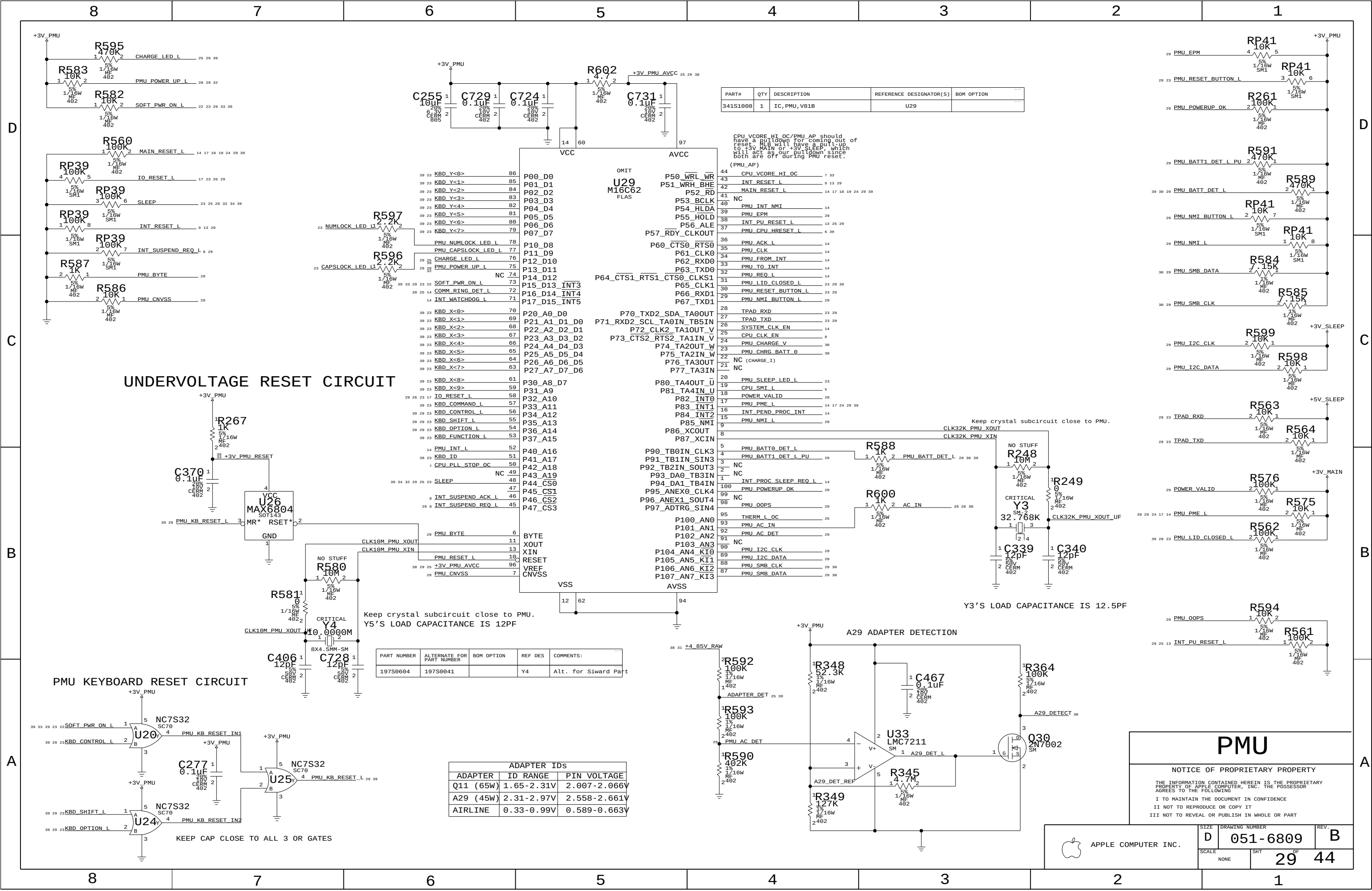
FIREWIRE PORTS

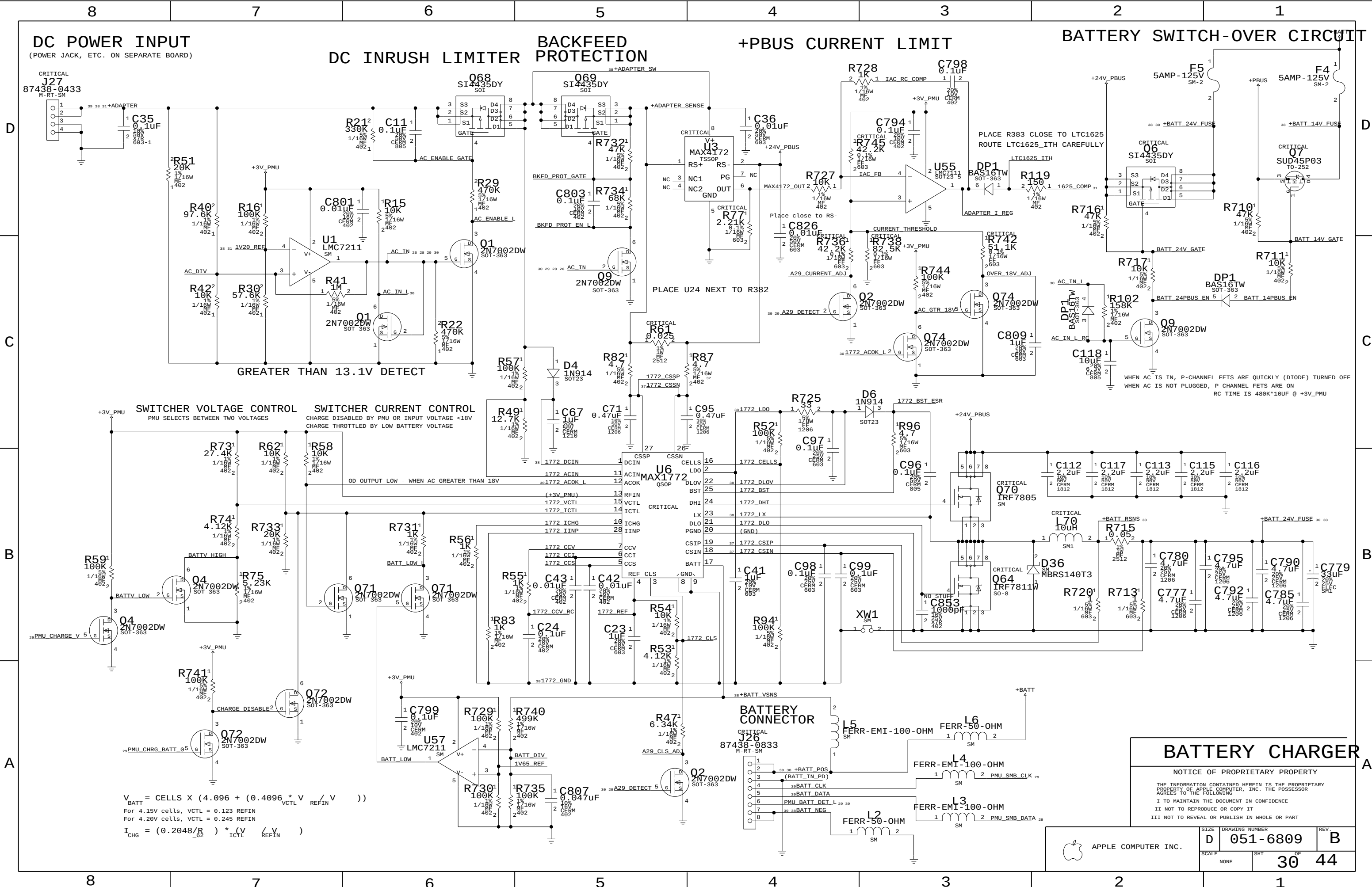
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APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6809	B
SCALE		SHT	OF
NONE		28	44





DC POWER INPUT

(POWER JACK, ETC. ON SEPARATE BOARD)

DC INRUSH LIMITER

BACKFEED PROTECTION

+PBUS CURRENT LIMIT

BATTERY SWITCH-OVER CIRCUIT

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE

BATTERY CONNECTOR

BATTERY CHARGER

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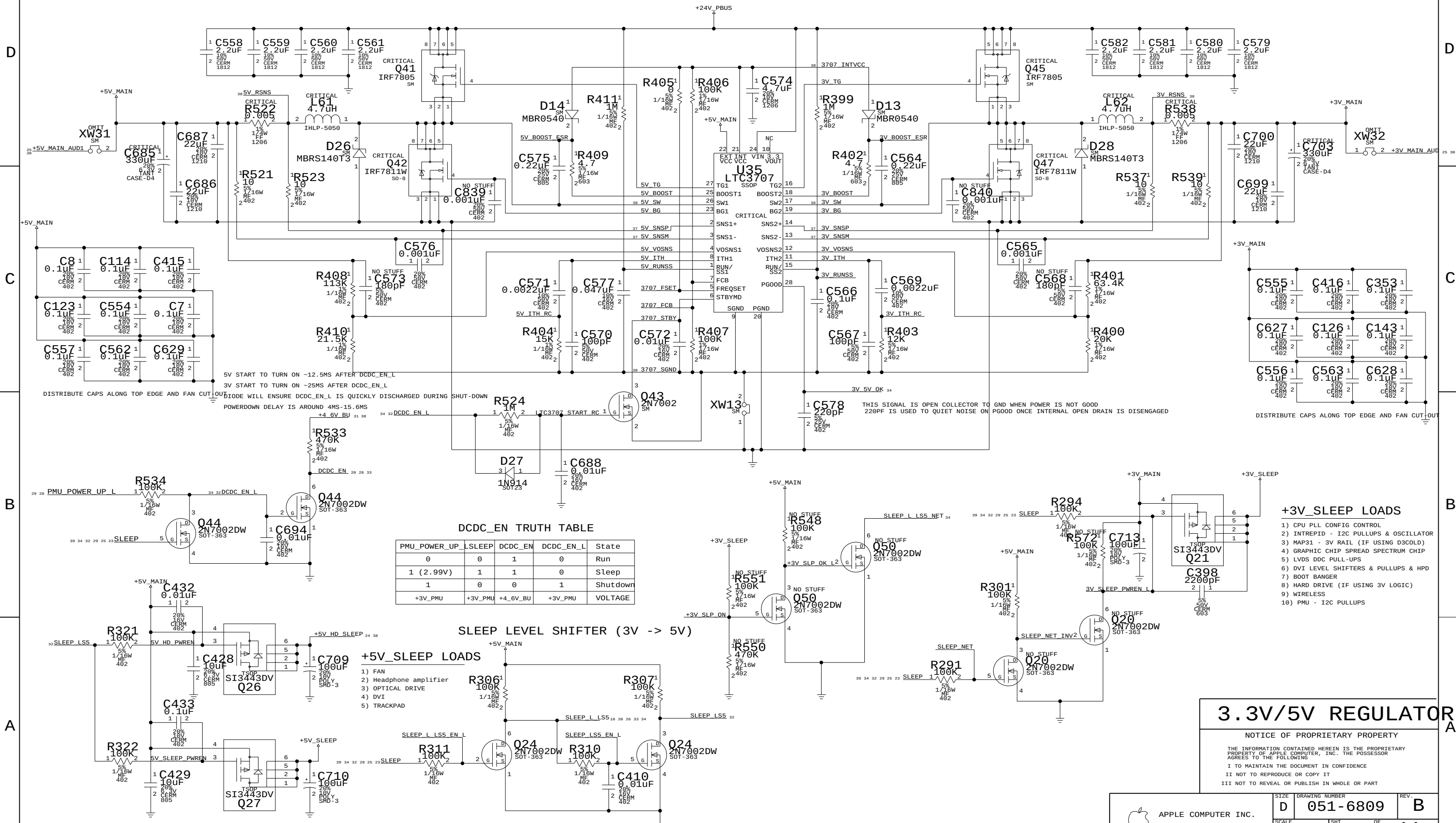
$$V_{BATT} = CELLS \times (4.096 + (0.4096 \times V_{VCTL} / V_{REFIN}))$$

For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN

$$I_{CHG} = (0.2048 / R_{G2}) \times (V_{ICTL} / V_{REFIN})$$

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	30	44

3.3V/5V MAIN SUPPLY



DCDC_EN TRUTH TABLE				
PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

SLEEP LEVEL SHIFTER (3V -> 5V)

+5V_SLEEP LOADS

- 1) FAN
- 2) Headphone amplifier
- 3) OPTICAL DRIVE
- 4) DVI
- 5) TRACKPAD

+3V_SLEEP LOADS

- 1) CPU PLL CONFIG CONTROL
- 2) INTREPID - I2C PULLUPS & OSCILLATOR
- 3) MAP31 - 3V RAIL (IF USING D3COLD)
- 4) GRAPHIC CHIP SPREAD SPECTRUM CHIP
- 5) LVDS DDC PULL-UPS
- 6) DVI LEVEL SHIFTERS & PULLUPS & HPD
- 7) BOOT BANGER
- 8) HARD DRIVE (IF USING 3V LOGIC)
- 9) WIRELESS
- 10) PMU - I2C PULLUPS

3.3V/5V REGULATOR

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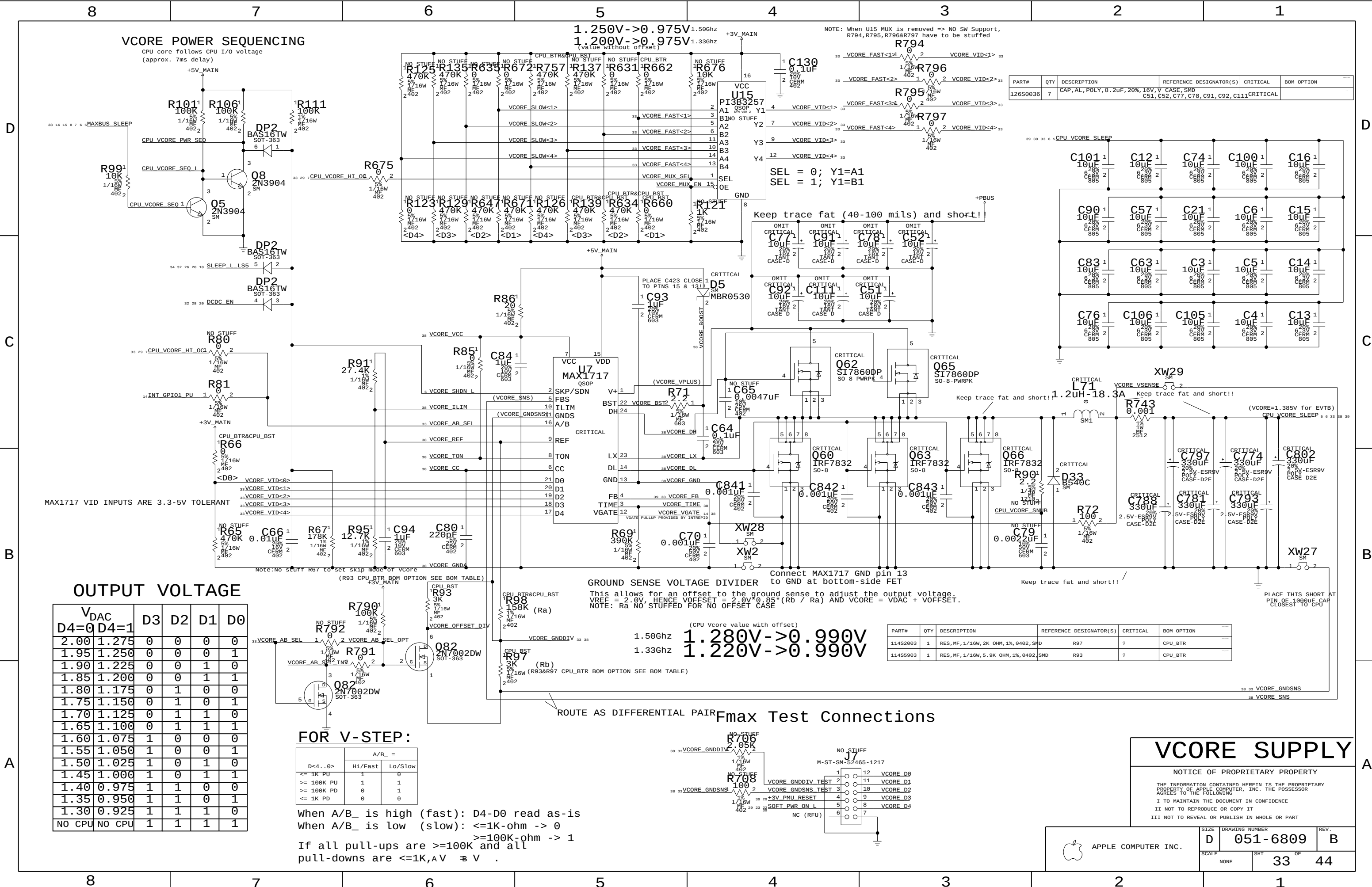
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SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	32	44

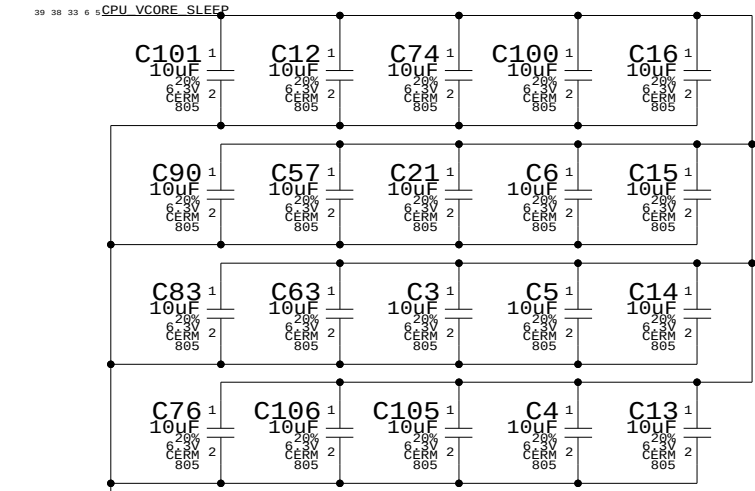


VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage (approx. 7ms delay)

NOTE: When U15 MUX is removed => NO SW Support, R794, R795, R796&R797 have to be stuffed

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
126S9036	7	CAP, AL, POLY, 8.2uF, 20%, 16V, V	C51, C52, C77, C78, C91, C92, C111	CRITICAL	



Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Keep trace fat and short!!

Keep trace fat and short!!

PLACE THIS SHORT AT PIN 10 OF CAP CLOSEST TO CPU

OUTPUT VOLTAGE

V _{DAC}	D4=0	D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0	0
1.95	1.250	0	0	0	0	1
1.90	1.225	0	0	0	1	0
1.85	1.200	0	0	0	1	1
1.80	1.175	0	1	0	0	0
1.75	1.150	0	1	0	0	1
1.70	1.125	0	1	1	0	0
1.65	1.100	0	1	1	1	1
1.60	1.075	1	0	0	0	0
1.55	1.050	1	0	0	1	0
1.45	1.000	1	0	1	1	1
1.40	0.975	1	1	0	0	0
1.35	0.950	1	1	1	0	1
1.30	0.925	1	1	1	1	0
NO CPU	NO CPU	1	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ =	
	Hi/Fast	Lo/Slow
<= 1K PU	1	0
>= 100K PU	0	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0

=>100K-ohm -> 1
If all pull-ups are >=100K and all pull-downs are <=1K, A/V = V

GROUND SENSE VOLTAGE DIVIDER
This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V, HENCE VOFFSET = 2.0V * 0.85 * (Rb / Ra) AND VCORE = VDAC + VOFFSET.
NOTE: Ra NO STUFFED FOR NO OFFSET CASE

(CPU Vcore value with offset)
1.50Ghz 1.280V->0.990V
1.33Ghz 1.220V->0.990V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2093	1	RES, MF, 1/16W, 2K OHM, 1%, 0402, SMD	R97	?	CPU_BTR
114S5993	1	RES, MF, 1/16W, 5.9K OHM, 1%, 0402, SMD	R93	?	CPU_BTR

Fmax Test Connections

VCORE SUPPLY

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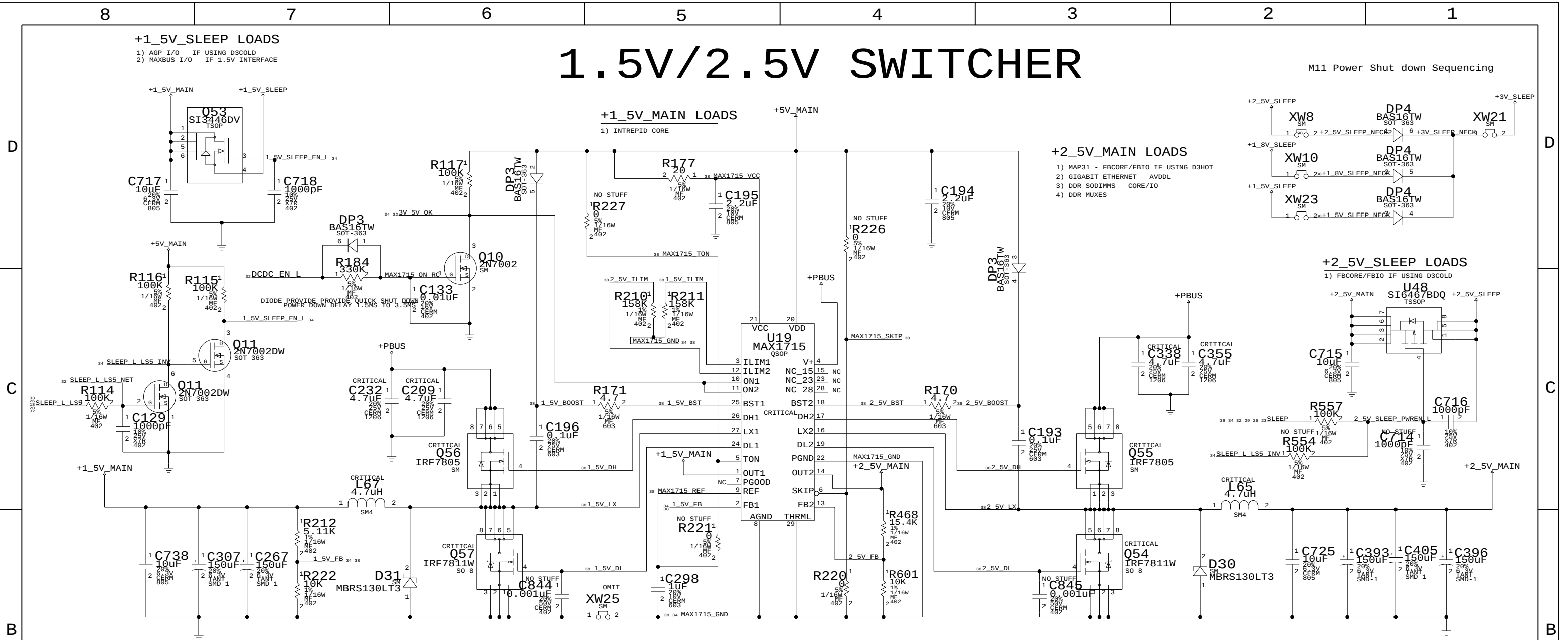
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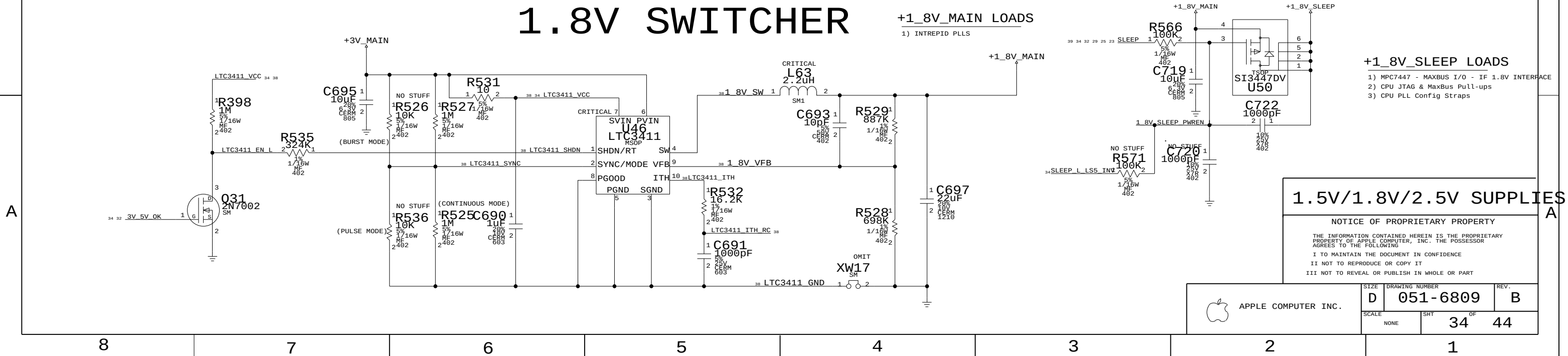
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	33	44

1.5V/2.5V SWITCHER



1.8V SWITCHER



		8		7		6		5		4		3		2		1	

<

8		7		6		5		4		3		2		1																			
Digital Signals (cont'd)																Differential Signals																	
GROUP		SIG_NAME		PROPAGATION_DELAY		MAX_VIAS		MAX_EXPOSED_LENGTH		WIRE_LENGTH		NET_SPACING_TYPE		NO_TEST		PULSE_PARAMS		GROUP		SIG_NAME		DIFFERENTIAL_PAIR		RELATIVE_PROPAGATION_DELAY		MAX_EXPOSED_LENGTH		WIRE_LENGTH		NET_SPACING_TYPE		MAX_VIAS	
D	AGP	AGP AD<15..0>		L:S:1050:1450	7												66 MHZ	12 19	Zo = 110	FIREWIRE	FW_TPIO0N	FW_TPIO0	FW_TPIO0:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39	
		AGP CBE<1..0>		L:S:1050:1450	7												66 MHZ	12 19		FW_TPIO0P	FW_TPIO0P	FW_TPIO0:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP AD_STB<0>		L:S:1050 MIL:1450 MIL				(250)	8 MIL SPACING								133.0 MHZ	12 19		FW_TPO0N	FW_TPO0N	FW_TPO00:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP AD_STB L<0>		L:S:1050 MIL:1450 MIL				(250)	8 MIL SPACING								133.0 MHZ	12 19		FW_TPO0P	FW_TPO0P	FW_TPO00:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP AD<31..16>		L:S:1050:1450	7												66 MHZ	12 19		FW_TPBIO0N	FW_TPBIO0	FW_TPBIO0:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP CBE<3..2>		L:S:1050:1450	7												66 MHZ	12 19		FW_TPBIO0P	FW_TPBIO0P	FW_TPBIO0:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP AD_STB<1>		L:S:1050 MIL:1450 MIL				(250)	8 MIL SPACING								133.0 MHZ	12 19		FW_TPA00N	FW_TPA00N	FW_TPA000:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP AD_STB L<1>		L:S:1050 MIL:1450 MIL				(250)	8 MIL SPACING								133.0 MHZ	12 19		FW_TPA00P	FW_TPA00P	FW_TPA000:G:L:S:0 MIL:5 MIL			500.0000				110 OHM SPACING		27 28 39		
		AGP SBA<7..0>		L:S:1050:1450	7												66 MHZ	12 19		FW_TPA1N	FW_TPA1N	FW_TPA1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39		
		AGP SB_STB		L:S:1050 MIL:1450 MIL				(350)	8 MIL SPACING								66.00 MHZ	12 19		FW_TPA1P	FW_TPA1P	FW_TPA1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39		
C	PCI	AGP SB_STB L		L:S:1050 MIL:1450 MIL			(350)	8 MIL SPACING								66.00 MHZ	12 19	FW_TPB1N	FW_TPB1N	FW_TPB1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP FRAME L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	FW_TPB1P	FW_TPB1P	FW_TPB1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP IRDY L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	FW_TPI1N	FW_TPI1N	FW_TPI1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP TRDY L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	FW_TPI1P	FW_TPI1P	FW_TPI1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP DEVSEL L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	FW_TPO1N	FW_TPO1N	FW_TPO1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP STOP L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	FW_TPO1P	FW_TPO1P	FW_TPO1:G:L:S:0 MIL:4%			500.0000				110 OHM SPACING		27 28 39				
		AGP PAR		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	ENET MDIO	ENET MDIO	ENET MDIO0:G:U43.29:J23.1:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		AGP REQ L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	ENET MDIO<0>	ENET MDIO<0>	ENET MDIO0:G:U43.31:J23.2:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		AGP GNT L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	ENET MDIO<1>	ENET MDIO<1>	ENET MDIO1:G:U43.33:J23.3:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		AGP RBF L		L:S:1250 MIL:1950 MIL												66.00 MHZ	12 19	ENET MDIO<2>	ENET MDIO<2>	ENET MDIO1:G:U43.34:J23.4:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
B	ULTRA ATA-100	PCI AD<31..0>		L:S:6000:12500												33 MHZ	9 12 17 18 24	ENET MDIO<3>	ENET MDIO<3>	ENET MDIO1:G:U43.39:J23.7:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		PCI CBE<3..0>		L:S:6000:12500												33 MHZ	12 17 18 24	ENET MDIO<4>	ENET MDIO<4>	ENET MDIO1:G:U43.41:J23.8:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		PCI FRAME L		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	ENET MDIO<5>	ENET MDIO<5>	ENET MDIO3:G:U43.42:J23.9:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		PCI IRDY L		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	ENET MDIO<6>	ENET MDIO<6>	ENET MDIO3:G:U43.43:J23.10:0 MIL:100 MIL			100 OHM SPACING				11 MIL SPACING		26 39				
		PCI TRDY L		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	CLKLVDS LN	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
		PCI DEVSEL L		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	CLKLVDS LP	CLKLVDS_L	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
		PCI STOP L		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	LVDS L0N	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
		PCI PAR		L:S:6000 MIL:12500 MIL					MIN DAISY CHAIN							33.00 MHZ	12 17 18 24	LVDS L0P	LVDS_L0	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
		UIDE DATA<15..8>		L:S:770				(200)								100 MHZ	13 24	LVDS L1N	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
		UIDE DATA<7>		U43 V1:RP19.3:1:600 MIL				(200)								100.0 MHZ	13 24	LVDS L1P	LVDS_L1	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39				
A	FIREWIRE MII	UIDE DATA<6..0>		L:S:1:600			(200)								100 MHZ	13 24	LVDS L2N	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE ADDR<2..0>		L:S:1:650			(200)		NEED TO MATCH DELAY TO 2500 MHZ						100 MHZ	13 24	LVDS L2P	LVDS_L2	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE RST L		L:S:400 MIL											100.0 MHZ	13 24	CLKLVDS UN	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE DIOW L		L:S:400 MIL											100.0 MHZ	13 24	CLKLVDS UP	CLKLVDS_U	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE DIOR L		L:S:600 MIL					10 MIL SPACING						100.0 MHZ	13 24	LVDS U0N	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE DMACK L		L:S:400 MIL											100.0 MHZ	13 24	LVDS U0P	LVDS_U0	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE CS0 L		L:S:500 MIL											100.0 MHZ	13 24	LVDS U1N	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL			500.0000				100 OHM SPACING		26 22 39					
		UIDE CS1 L		L:S:500 MIL											100.0 MHZ	13 24	LVDS U1P	LVDS_U1	LVDS:G:L:S:0 MIL:110 MIL														

	8	7	6	5	4	3	2	1																																																																																																																																																																																																																																																																																																							
	POWER NET CONSTRAINTS																																																																																																																																																																																																																																																																																																														
	<table><tr><th>GROUP</th><th>SIG_NAME</th><th>VOLTAGE</th><th>MIN_LINE_WIDTH</th><th>MIN_NECK_WIDTH</th></tr><tr><td rowspan="14">MAIN/SLEEP</td><td>+24V PBUS</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+BATT</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+PBUS</td><td>VOLTAGE=12.8V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V MAIN</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V SLEEP</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+3V MAIN</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+3V SLEEP</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=6</td></tr><tr><td>+3V PMU</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+2.5V MAIN</td><td>VOLTAGE=2.5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+2.5V SLEEP</td><td>VOLTAGE=2.5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+1.8V MAIN</td><td>VOLTAGE=1.8V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=6</td></tr><tr><td>+1.8V SLEEP</td><td>VOLTAGE=1.8V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=6</td></tr><tr><td>+1.5V MAIN</td><td>VOLTAGE=1.5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+1.5V SLEEP</td><td>VOLTAGE=1.5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="4">ADAPTER</td><td>+ADAPTER</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=50</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+ADAPTER SW</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=50</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+ADAPTER SW</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=50</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+ADAPTER SENSE</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=50</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="10">BATTERY CHARGER</td><td>+BATT_POS</td><td>VOLTAGE=16.8V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>BATT_NEG</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>I772 DCIN</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>I772 LX</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+BATT_14V_FUSE</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+BATT_24V_FUSE</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+BATT_RSNS</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+BATT_VSNS</td><td>VOLTAGE=12.6V</td><td>MIN LINE WIDTH=10</td><td>MIN NECK WIDTH=10</td></tr><tr><td>I772 LDO</td><td>VOLTAGE=5.4V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>I772 DLOV</td><td>VOLTAGE=5.4V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td rowspan="10">PMU</td><td>I772 GND</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+ADAPTER_ILIM</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+ADAPTER_OR_BATT</td><td>VOLTAGE=24V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+4.85V RAW</td><td>VOLTAGE=4.85V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+4.6V BU</td><td>VOLTAGE=4.6V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+4.85V ESR</td><td>VOLTAGE=4.85V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+3V PMU ESR</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+3V PMU AVCC</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+5V_HD_SLEEP</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+HD_LOGIC_SLEEP</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="2">TRACKPAD</td><td>+5V_TP_AD_SLEEP</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td>+3V_HALL_EFFECT</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td rowspan="10">VIDEO</td><td>+14V_INV</td><td>VOLTAGE=14V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V_INV_UF_SW</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V_INV_SW</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V_ODC_SLEEP</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=15</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+5V_ODC_SLEEP_UF</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=15</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+3V_LCD</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=12</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+3V_LCD_SW</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>GPU_TV_GND1</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td></td></tr><tr><td>GPU_TV_GND2</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td></td></tr><tr><td>TV_GND1</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td></td></tr><tr><td rowspan="2">AUDIO</td><td>+5V_MAIN_AUD</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>+3V_MAIN_AUD</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="2">FAN</td><td>AUD_GND</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=50</td><td></td></tr><tr><td>+FAN_PWR</td><td>VOLTAGE=5V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="4">I/O AREA</td><td>FAN1_GND</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>FAN2_GND</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>CHGND1</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=12</td></tr><tr><td>CHGND2</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=12</td></tr><tr><td rowspan="4">INVERTER TRACKPAD LVDS</td><td>CHGND3</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=12</td></tr><tr><td>CHGND4</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=12</td></tr><tr><td>ENET_CTAP_CHGND</td><td>VOLTAGE=0V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=12</td></tr><tr><td></td><td></td><td></td><td></td></tr></table>	GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	MAIN/SLEEP	+24V PBUS	VOLTAGE=24V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+BATT	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+PBUS	VOLTAGE=12.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+5V MAIN	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+5V SLEEP	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+3V MAIN	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+3V SLEEP	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=6	+3V PMU	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+2.5V MAIN	VOLTAGE=2.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+2.5V SLEEP	VOLTAGE=2.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+1.8V MAIN	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=6	+1.8V SLEEP	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=6	+1.5V MAIN	VOLTAGE=1.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+1.5V SLEEP	VOLTAGE=1.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	ADAPTER	+ADAPTER	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10	+ADAPTER SW	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10	+ADAPTER SW	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10	+ADAPTER SENSE	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10	BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	BATT_NEG	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	I772 DCIN	VOLTAGE=24V	MIN LINE WIDTH=10		I772 LX	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+BATT_RSNS	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+BATT_VSNS	VOLTAGE=12.6V	MIN LINE WIDTH=10	MIN NECK WIDTH=10	I772 LDO	VOLTAGE=5.4V	MIN LINE WIDTH=10		I772 DLOV	VOLTAGE=5.4V	MIN LINE WIDTH=10		PMU	I772 GND	VOLTAGE=0V	MIN LINE WIDTH=10		+ADAPTER_ILIM	VOLTAGE=24V	MIN LINE WIDTH=10		+ADAPTER_OR_BATT	VOLTAGE=24V	MIN LINE WIDTH=10		+4.85V RAW	VOLTAGE=4.85V	MIN LINE WIDTH=10		+4.6V BU	VOLTAGE=4.6V	MIN LINE WIDTH=10		+4.85V ESR	VOLTAGE=4.85V	MIN LINE WIDTH=10		+3V PMU ESR	VOLTAGE=3.3V	MIN LINE WIDTH=10		+3V PMU AVCC	VOLTAGE=3.3V	MIN LINE WIDTH=10		+5V_HD_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	TRACKPAD	+5V_TP_AD_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=10		+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN LINE WIDTH=10		VIDEO	+14V_INV	VOLTAGE=14V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+5V_INV_UF_SW	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+5V_INV_SW	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+5V_ODC_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=15	MIN NECK WIDTH=10	+5V_ODC_SLEEP_UF	VOLTAGE=5V	MIN LINE WIDTH=15	MIN NECK WIDTH=10	+3V_LCD	VOLTAGE=3.3V	MIN LINE WIDTH=12	MIN NECK WIDTH=10	+3V_LCD_SW	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	GPU_TV_GND1	VOLTAGE=0V	MIN LINE WIDTH=25		GPU_TV_GND2	VOLTAGE=0V	MIN LINE WIDTH=25		TV_GND1	VOLTAGE=0V	MIN LINE WIDTH=25		AUDIO	+5V_MAIN_AUD	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	+3V_MAIN_AUD	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	FAN	AUD_GND	VOLTAGE=0V	MIN LINE WIDTH=50		+FAN_PWR	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	I/O AREA	FAN1_GND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	FAN2_GND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	CHGND1	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12	CHGND2	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12	INVERTER TRACKPAD LVDS	CHGND3	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12	CHGND4	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12	ENET_CTAP_CHGND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12					<table><tr><th>GROUP</th><th>SIG_NAME</th><th>VOLTAGE</th><th>MIN_LINE_WIDTH</th><th>MIN_NECK_WIDTH</th></tr><tr><td rowspan="5">CPU</td><td>CPU_VCORE_SLEEP</td><td>VOLTAGE=1.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>CPU_AVDD</td><td>VOLTAGE=1.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>MAXBUS_SLEEP</td><td>VOLTAGE=1.8V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>CPU_AVDD_VIN</td><td>VOLTAGE=3.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td>CPU_AVDD_VOUT</td><td>VOLTAGE=1.3V</td><td>MIN LINE WIDTH=25</td><td>MIN NECK WIDTH=10</td></tr><tr><td rowspan="2">DDR RAM</td><td>DDR_VREF</td><td>VOLTAGE=1.25V</td><td>MIN LINE WIDTH=10</td><td></td></tr><tr><td></td><td></td><td></td><td></td></tr><tr><td>INTREPID PLLS</td><td>+2.5V_INTREPID</td><td>V</td></tr></table>	GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	CPU_AVDD	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	CPU_AVDD_VIN	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10	DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN LINE WIDTH=10						INTREPID PLLS	+2.5V_INTREPID	V
GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH																																																																																																																																																																																																																																																																																																											
MAIN/SLEEP	+24V PBUS	VOLTAGE=24V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+BATT	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+PBUS	VOLTAGE=12.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V MAIN	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V SLEEP	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+3V MAIN	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+3V SLEEP	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=6																																																																																																																																																																																																																																																																																																											
	+3V PMU	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+2.5V MAIN	VOLTAGE=2.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+2.5V SLEEP	VOLTAGE=2.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+1.8V MAIN	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=6																																																																																																																																																																																																																																																																																																											
	+1.8V SLEEP	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=6																																																																																																																																																																																																																																																																																																											
	+1.5V MAIN	VOLTAGE=1.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+1.5V SLEEP	VOLTAGE=1.5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+ADAPTER SW	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+ADAPTER SW	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+ADAPTER SENSE	VOLTAGE=24V	MIN LINE WIDTH=50	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	BATT_NEG	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	I772 DCIN	VOLTAGE=24V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	I772 LX	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+BATT_RSNS	VOLTAGE=12.6V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+BATT_VSNS	VOLTAGE=12.6V	MIN LINE WIDTH=10	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	I772 LDO	VOLTAGE=5.4V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	I772 DLOV	VOLTAGE=5.4V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
PMU	I772 GND	VOLTAGE=0V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+ADAPTER_ILIM	VOLTAGE=24V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+4.85V RAW	VOLTAGE=4.85V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+4.6V BU	VOLTAGE=4.6V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+4.85V ESR	VOLTAGE=4.85V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+3V PMU ESR	VOLTAGE=3.3V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+3V PMU AVCC	VOLTAGE=3.3V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+5V_HD_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
TRACKPAD	+5V_TP_AD_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
VIDEO	+14V_INV	VOLTAGE=14V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V_INV_UF_SW	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V_INV_SW	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V_ODC_SLEEP	VOLTAGE=5V	MIN LINE WIDTH=15	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+5V_ODC_SLEEP_UF	VOLTAGE=5V	MIN LINE WIDTH=15	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+3V_LCD	VOLTAGE=3.3V	MIN LINE WIDTH=12	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+3V_LCD_SW	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	GPU_TV_GND1	VOLTAGE=0V	MIN LINE WIDTH=25																																																																																																																																																																																																																																																																																																												
	GPU_TV_GND2	VOLTAGE=0V	MIN LINE WIDTH=25																																																																																																																																																																																																																																																																																																												
	TV_GND1	VOLTAGE=0V	MIN LINE WIDTH=25																																																																																																																																																																																																																																																																																																												
AUDIO	+5V_MAIN_AUD	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	+3V_MAIN_AUD	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
FAN	AUD_GND	VOLTAGE=0V	MIN LINE WIDTH=50																																																																																																																																																																																																																																																																																																												
	+FAN_PWR	VOLTAGE=5V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
I/O AREA	FAN1_GND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	FAN2_GND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	CHGND1	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12																																																																																																																																																																																																																																																																																																											
	CHGND2	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12																																																																																																																																																																																																																																																																																																											
INVERTER TRACKPAD LVDS	CHGND3	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12																																																																																																																																																																																																																																																																																																											
	CHGND4	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12																																																																																																																																																																																																																																																																																																											
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN LINE WIDTH=25	MIN NECK WIDTH=12																																																																																																																																																																																																																																																																																																											
GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH																																																																																																																																																																																																																																																																																																											
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	CPU_AVDD	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	CPU_AVDD_VIN	VOLTAGE=3.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
	CPU_AVDD_VOUT	VOLTAGE=1.3V	MIN LINE WIDTH=25	MIN NECK WIDTH=10																																																																																																																																																																																																																																																																																																											
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN LINE WIDTH=10																																																																																																																																																																																																																																																																																																												
INTREPID PLLS	+2.5V_INTREPID	V																																																																																																																																																																																																																																																																																																													

FUNCTIONAL TEST POINTS

PROBES ARE ON BOTTOM SIDE. MINIMUM PAD/HOLE SIZE IS 25 MIL.
FUNC_TEST IS ONLY PROPERTY USED BY THE TOOLS. FUNC_QTY IS FOR REFERENCE AND
LISTS THE NUMBER OF TEST POINTS ON THAT NET AND WITHIN THAT GROUP/CONNECTOR.
FUNC_DIST IS SIMILARLY USED TO DEFINE MAXIMUM DISTANCE FROM A CONNECTOR.

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
SCAN/TEST	JTAG_ASIC_TMS	TRUE		13 26
	JTAG_ASIC_TDI	TRUE		13
	JTAG_ASIC_TDO_TP	TRUE		26
	JTAG_ASIC_TCK	TRUE		13 26
	JTAG_ASIC_TRST_L	TRUE		13 26
	CPU_CHKSTP_OUT_L	TRUE		5
	CPU_SRESET_L	TRUE		5
	CPU_HRESET_L	TRUE		5 6 7
	JTAG_CPU_TMS	TRUE		5 6
	JTAG_CPU_TDI	TRUE		5 6
	JTAG_CPU_TDO_TP	TRUE		5
	JTAG_CPU_TCK	TRUE		5 6
	JTAG_CPU_TRST_L	TRUE		5 6
	INT_JTAG_TEI	TRUE		13
	INT_TST_MONIN_PD	TRUE		13
	INT_TST_MONOUT_TP	TRUE		13
	INT_TST_PLLEN_PD	TRUE		13
	INT_I2C_CLK0	TRUE		6 11 13 23
	INT_I2C_DATA0	TRUE		6 11 13 23
	INT_I2C_CLK1	TRUE		13 14 25
INT I2C	INT_I2C_DATA1	TRUE		13 14 25
	+PBUS	TRUE		38
PWR/GND	+24V_PBUS	TRUE		38
	GPU_VCORE	TRUE		10 20 38
	1778_VFB	TRUE		20 38
	CPU_VCORE_SLEEP	TRUE		5 6 33 38
	VCORE_FB	TRUE		33 38
	+1_8V_MAIN	TRUE		38
	+2_5V_MAIN	TRUE		38
	+5V_MAIN	TRUE	2	38 39
	+5V_SLEEP	TRUE	2	38 39
	+3V_MAIN	TRUE	4	23 38
CARDBUS DVI	+3V_PMU	TRUE		38
	CBUS_DET_1_L	TRUE		2000
	CBUS_DET_2_L	TRUE		2000
	TMDS_DM<0..2>	TRUE		1000
	TMDS_DP<0..2>	TRUE		1000
	TMDS_CONN_CLKN	TRUE		1000
	TMDS_CONN_CLKP	TRUE		1000
	VGA_R	TRUE		1000
	VGA_G	TRUE		1000
	VGA_B	TRUE		1000
	VGA_HSYNC	TRUE		1000
	VGA_VSYNC	TRUE		1000
	DVI_DDC_CLK_UF	TRUE		1000
	DVI_DDC_DATA_UF	TRUE		1000
	DVI_HPD_UF	TRUE		1000
	+5V_DDC_SLEEP	TRUE		2000
LVDS	LVDS_L0N	TRUE		1000
	LVDS_L0P	TRUE		1000
	LVDS_L1N	TRUE		1000
	LVDS_L1P	TRUE		1000
	LVDS_L2N	TRUE		1000
	LVDS_L2P	TRUE		1000
	CLKLVDS_LN	TRUE		1000
	CLKLVDS_LP	TRUE		1000
	LVDS_DDC_CLK	TRUE		1000
	LVDS_DDC_DATA	TRUE		1000
	+3V_LCD	TRUE	2	2000
	+3V_SLEEP	TRUE		2000
INVERTER	+14V_INV	TRUE		2000
	+5V_INV_SW	TRUE		2000
	BRIGHT_PWM	TRUE		2000
	INV_GND	TRUE		2000
S-VIDEO	TV_C	TRUE		2000
	TV_Y	TRUE		2000
	TV_COMP	TRUE		2000
	TV_GND1	TRUE		2000
	TV_GND2	TRUE		2000
LIO	INT_I2S0_SND_TO_DAC	TRUE		1000
	INT_I2S0_SND_LRCLK	TRUE		1000
	INT_I2S0_SND_MCLK	TRUE		1000
	INT_I2S0_SND_SCLK	TRUE		1000
	INT_I2S0_SND_FROM_ADC	TRUE		1000
	SND_HP_MUTE_L	TRUE		1000
	SND_HP_MUTE	TRUE		1000
	SND_HW_RESET_L	TRUE		1000
	SND_HP_SENSE_L	TRUE		1000
	SND_LIN_SENSE_L	TRUE		1000
	INT_I2C_CLK2	TRUE		1000
	INT_I2C_DATA2	TRUE		1000
	ADAPTER_DET	TRUE		1000
	CHARGE_LED_L	TRUE		1000
	NEC_LUSB_OCI_UF	TRUE		1000
	NEC_LUSB_PPON	TRUE		1000
	+5V_MAIN	TRUE	2	2000
	+5V_SLEEP	TRUE	2	2000
	+3V_SLEEP	TRUE		2000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
USB	NEC_USB_DAM	TRUE		17 25 37
	NEC_USB_DAP	TRUE		17 25 37
	NEC_USB_DBM	TRUE		17 25 37
	NEC_USB_DBP	TRUE		17 25 37
	BT_USB_DM	TRUE		14 25 37
	BT_USB_DP	TRUE		14 25 37
	MODEM_USB_DM	TRUE		14 25 37
	MODEM_USB_DP	TRUE		14 25 37
	NEC_RUSB_PPON	TRUE		17 25
	NEC_RUSB_OCI_UF	TRUE		17 25
RT. USB WIRELESS	PCI_AD<0..31>	TRUE		1000
	PCI_FRAME_L	TRUE		1000
	PCI_TRDY_L	TRUE		1000
	PCI_IRDY_L	TRUE		1000
	PCI_DEVSEL_L	TRUE		1000
	PCI_STOP_L	TRUE		1000
	PCI_PAR	TRUE		1000
	AIRPORT_PCI_REQ_L	TRUE		1000
	AIRPORT_PCI_GNT_L	TRUE		1000
	AIRPORT_PCI_INT_L	TRUE		1000
	MAIN_RESET_L	TRUE		1000
	CLK33M_AIRPORT	TRUE		1000
	PMU_PME_L	TRUE		1000
	ROM_ONBOARD_CS_L	TRUE		1000
	ROM_OE_L	TRUE		1000
	ROM_CS_L	TRUE		1000
	ROM_RW_L	TRUE		1000
	RF_DISABLE_L	TRUE		1000
	AIRPORT_CLKRUN_L	TRUE		1000
	+3V_AIRPORT	TRUE		1000
OPTICAL	EIDE_OPTICAL_DATA<0..15>	TRUE		2000
	EIDE_OPTICAL_DMA_RD	TRUE		2000
	EIDE_OPTICAL_READ_L	TRUE		2000
	EIDE_OPTICAL_DMAACK_L	TRUE		2000
	EIDE_OPTICAL_ADDR<0..2>	TRUE		2000
	EIDE_OPTICAL_CS0_L	TRUE		2000
	EIDE_OPTICAL_CS1_L	TRUE		2000
	EIDE_OPTICAL_RST_L	TRUE		2000
	EIDE_OPTICAL_WR_L	TRUE		2000
	EIDE_OPTICAL_IOCHRDY	TRUE		2000
	EIDE_OPTICAL_INT	TRUE		2000
TRACKPAD	+5V_TPAP_SLEEP	TRUE		3000
	TPAD_F_TXD	TRUE		3000
	TPAD_F_RXD	TRUE		3000
	LID_CLOSED_L	TRUE		3000
	+3V_HALL_EFFECT	TRUE		3000
	SOFT_PWR_ON_L	TRUE		3000
MODEM/ SERIAL	COMM_RESET_L	TRUE		4000
	COMM_SHUTDOWN	TRUE		4000
	COMM_RING_DET_L	TRUE		4000
	COMM_TXD_L	TRUE		4000
	COMM_TRXC	TRUE		4000
	COMM_GPIO_L	TRUE		4000
	COMM_DTR_L	TRUE		4000
	COMM_RTS_L	TRUE		4000
	COMM_RXD	TRUE		4000
KEYBOARD	KBD_ID	TRUE		3000
	KBD_INTL	TRUE		3000
	KBD_JIS	TRUE		3000
	KBD_CAPSLOCK_LED	TRUE		3000
	KBD_NUMLOCK_LED	TRUE		3000
	KBD_FUNCTION_L	TRUE		3000
	KBD_COMMAND_L	TRUE		3000
	KBD_OPTION_L	TRUE		3000
	KBD_CONTROL_L	TRUE		3000
	KBD_SHIFT_L	TRUE		3000
	KBD_X<0..9>	TRUE		3000
	KBD_Y<0..7>	TRUE		3000
BATTERY	+BATT_POS	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_NEG	TRUE	(100 MIL PROBE PREFERRED)	1000
	BATT_CLK	TRUE		1000
	BATT_DATA	TRUE		1000
	PMU_BATT_DET_L	TRUE		1000
FANS	+FAN_PWR	TRUE		3000
	FAN1_TACH	TRUE		3000
	FAN2_TACH	TRUE		3000
	FAN1_GND	TRUE		3000
	FAN2_GND	TRUE		3000
ETHERNET	MDI_P<0..3>	TRUE		1000
	MDI_M<0..3>	TRUE		1000
FIREWIRE	FW_TP00P	TRUE		1000
	FW_TP00N	TRUE		1000
	FW_TP00R	TRUE		1000
	FW_TPI0P	TRUE		1000
	FW_TPI0N	TRUE		1000
	+FW_VP0	TRUE		1000
	FW_VGND	TRUE		1000

GROUP	SIG_NAME	FUNC_TEST	FUNC_QTY	FUNC_DIST
FIREWIRE (CONT.)	FW_TP01P	TRUE		1000
	FW_TP01N	TRUE		1000
	FW_TPI1P	TRUE		1000
	FW_TPI1N	TRUE		1000
	+FW_VP1	TRUE		1000
	FW_VGND	TRUE		1000
DC PWR IN	+ADAPTER	TRUE	3 (100 MIL PROBE PREFERRED)	1000
LMU/ALS	ST7_SLEEP_LED_H	TRUE		23
	PMU_SLEEP_LED	TRUE		23
	PMU_LID_CLOSED_L	TRUE		23 29
	LMU_DETECT	TRUE		23
MISC.	SLEEP_LED	TRUE		23
	PMU_KB_RESET_L	TRUE		29
	SLEEP	TRUE		23 25 29 32 34
	PMU_CPU_HRESET_L	TRUE		6 29
	BB_RESET_L	TRUE		6
	+3V_PMU_RESET	TRUE		29 33

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6809	B
SCALE	SHT	OF
NONE	39	44

	8	7	6	5	4	3	2	1		
D	REVISION HISTORY Proto/EVT Release 10/27/03 - 1. Schematic originated from Q16 MLB 11/10/03 - 1. Replace U56 symbol 2. Connect OVDDSENSE to MAXBUS_SLEEP 3. Modify SW0 (SRW1 and IABRV8) connection 4. Connect SENSEVDD to CPU_VCORE_SLEEP (PAGE 5) 5. Connect SENSEVDD to CPU_VCORE_SLEEP 6. Connect SENSEGND to GND 7. Add 10K 1% resistor for AMD BootROM issue (R1,R194,R236,R271) 8. Connect TEMP_ANODE and TEMP_CATHODE to AD77460 9. Modify CPU PLL config 10. Add 10 ohm resistor on CG_FSEL Interpid side(R450) 11. Replace U4 symbol 12. Change R743 from 20 ohm to 10 ohm 13. Change R743 from 10 ohm to 10 ohm 14. Change R748 from 418 ohm to 18 ohm 12/01/03 - 1. Modify CPU_VCORE setting. 12/02/03 - 1. Modify CPU_BTR CPU_VCORE VID setting 12/05/03 - 1. Add CPU_AVDD LDO (Page 5) 2. Change Q45 and Q41 to IRF7805 (376S0035) 3. Change Q47 and Q42 to IRF7911W (376S0104) 4. Change R402 and R405 to 470ohm resistors 5. Connect INT_ID0 from Intrepid to Cypress Chip PD* (U31) 12/12/03 - 1. Add R468 and R601 for MAX1715 2.5V adjust 2. Modify CPU_VCORE setting to Motorola new spec 3. Modify LDO power sequence 12/16/03 - 1. Add 10K pull down for INT_TD0 on page 13 12/17/03 - 1. Change LDO Vin from +3V MAIN to +3V SLEEP 2. Connect INT_TD0 from Intrepid to Marvell 88E1111(U43) 3. Add R755,R756,R758,R759 for power rail DVT Release (Rev. 02) 01/30/04 - 1. Add Soft Modem(Pin14) 10K pull-up at J15-7 (Pg 25) 2. Add Bom Table for R97 2.21K ohm VCore Offset (Pg 33) 02/04/04 - 1. C811 change to 4.7uF per MOT A7PM requirement (Pg 5) 2. NO STUFF R236,R1,R271&R194 to remove PCI stub (Pg 9) DVT Release (Rev. 03) 02/12/04 - 1. CPU VCore adjustment for V1.1 A7PM CPU (Pg 33) 2. CPU AVDD adjustment for V1.1 A7PM CPU (Pg 5) 3. Add I/O VREF termination change to 0 ohm, 50% (Pg 20) 4. Add I/O VREF voltage divider change to both 1K ohm (Pg 12) DVT Release (Rev. 04) 02/13/04 - 1. INT. TMDS Termination change to 2* 49.9ohm = 100ohm (Pg 20) PVT Release (Rev. A) 03/11/04 - 1. INT. TMDS Termination change to 2* 75 ohm = 150ohm (except CLK pair) (Pg 20) 2. USB series termination near NEC PHY change to 47 ohm (Pg 17) PVT Release (Rev. A - 051-6570) 04/02/04 - 1. USB series termination near NEC PHY change to 43.2 ohm (Pg 17) Production Release (Rev. A - 051-6653) 04/09/04 - 1. Updated to Apollo 7PM rev 1.1.1 part numbers (Pg 5) 04/09/04 - 2. Updated to production BootROM part number (Pg 9) Production Release (Rev. B - 051-6653) 04/30/04 - 1. Updated to Fast Intrepid part for 6A ReadMacro Delay value (Pg 8-15) 04/30/04 - 2. Add ATI M11 A16 parts as alternative for A15 parts (Pg 19-21) 04/30/04 - 3. Use new VGA filter to remove ghost image on external VGA display (Pg 22) Production Release (Rev. C - 051-6653) 05/27/04 - 1. Updated BOM : 113S0006 -> 113S1000 05/27/04 - 2. Updated BOM : 132S0020 -> 132S0100 Production Release (Rev. B - 051-6809)-- merged with 051-6808 07/07/05 - Added 338S0223 (88E1111 Rev.B1) at U43 and 338S0079 as an alternate 07/08/05 - Added 337S2913 (IC,A7PM,1.33GHZ,1.18VCORE) as an option 07/08/05 - Added label for EEE:SQE 07/08/05 - Replaced 740S0006 with 740S0018 (FUSE,1.5A,24V,SMD,LF) at F3 07/19/05 - Corrected symbols for 337S2838 (MPU),132S0021 (0.47uF,10%) and 138S0511 (2.2uF,10%)									
C										
B										
A										
							A	NOTICE OF PROPRIETARY PROPERTY THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
								APPLE COMPUTER INC. SCALE: NONE	SIZE: D DRAWING NUMBER: 051-6809 REV.: B SHT: 40 OF 44	
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