1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
01		308060	ENGINEERING RELEASED	12/19/03	?

SINCLAIR Q41A

12/18/2003

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43-44	COMPONENT LOCATIONS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		√
D3_COLD	√	
GPU_SS	√	
GPU_SWITCH	√	
SERIAL_DEBUG		√
VCORE_OFFSET	√	
1_8V_MAXBUS	√	
1_5V_MAXBUS		√
NEC_USB	√	
INTREPID_USB		√
BBANG		√
NO_BBANG	√	
ATI_MEMIO_HI	√	
ATI_MEMIO_LO		√
SSCG		√
NO_SSCG	√	
5V_HD_LOGIC	√	
3V_HD_LOGIC		√
EXT_TMDS		√
INT_TMDS	√	
NO_4XVCORE	√	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6598	1	SCHEM,MLB,Q41A	SCH1	
820-1615	1	PCBF,MLB,Q41A	PCB1	

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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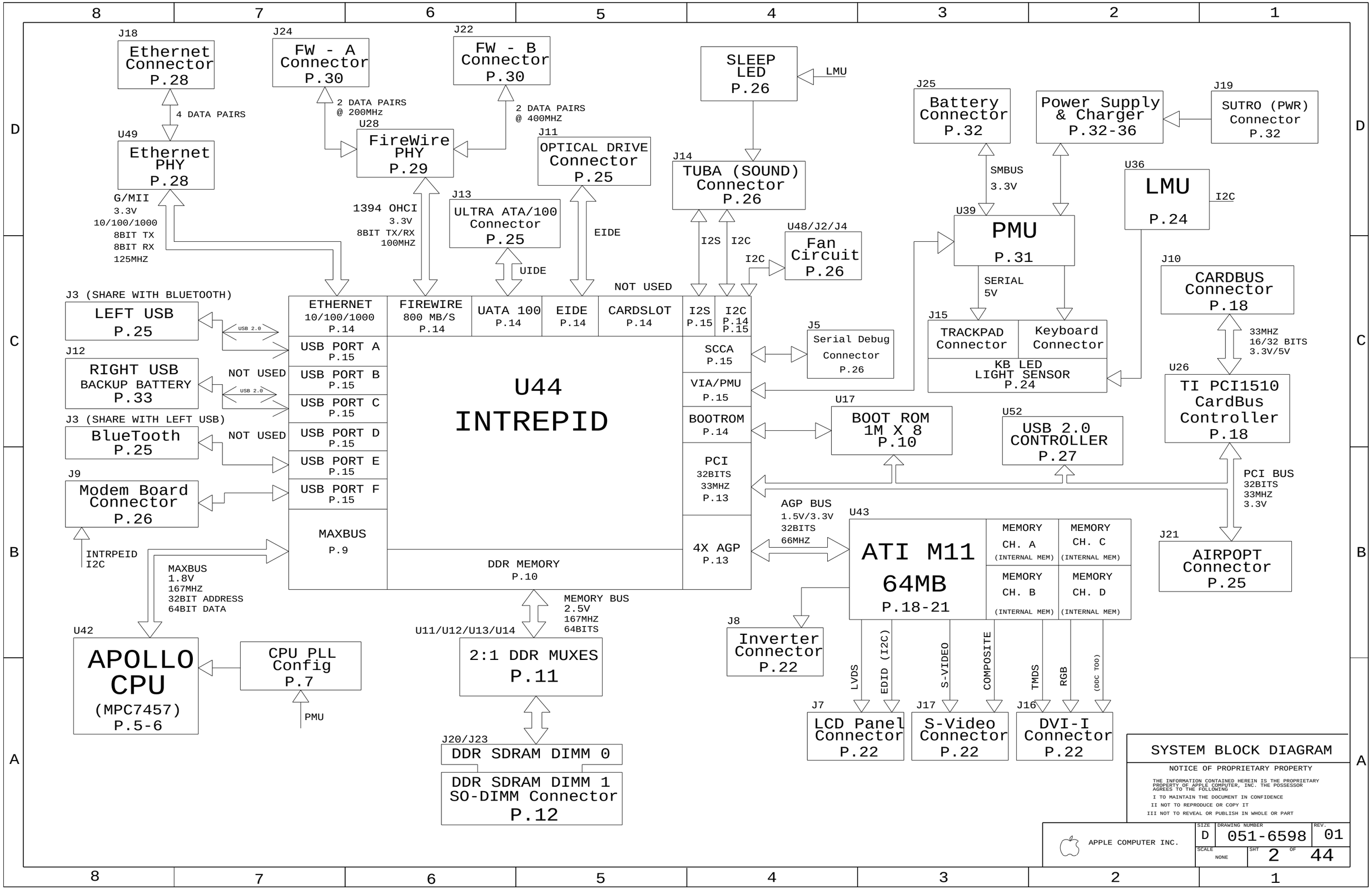
TITLE SCHEM,MLB,Q41A

DRAWING NUMBER 051-6598 REV. 01



SYSTEM BLOCK DIAGRAM

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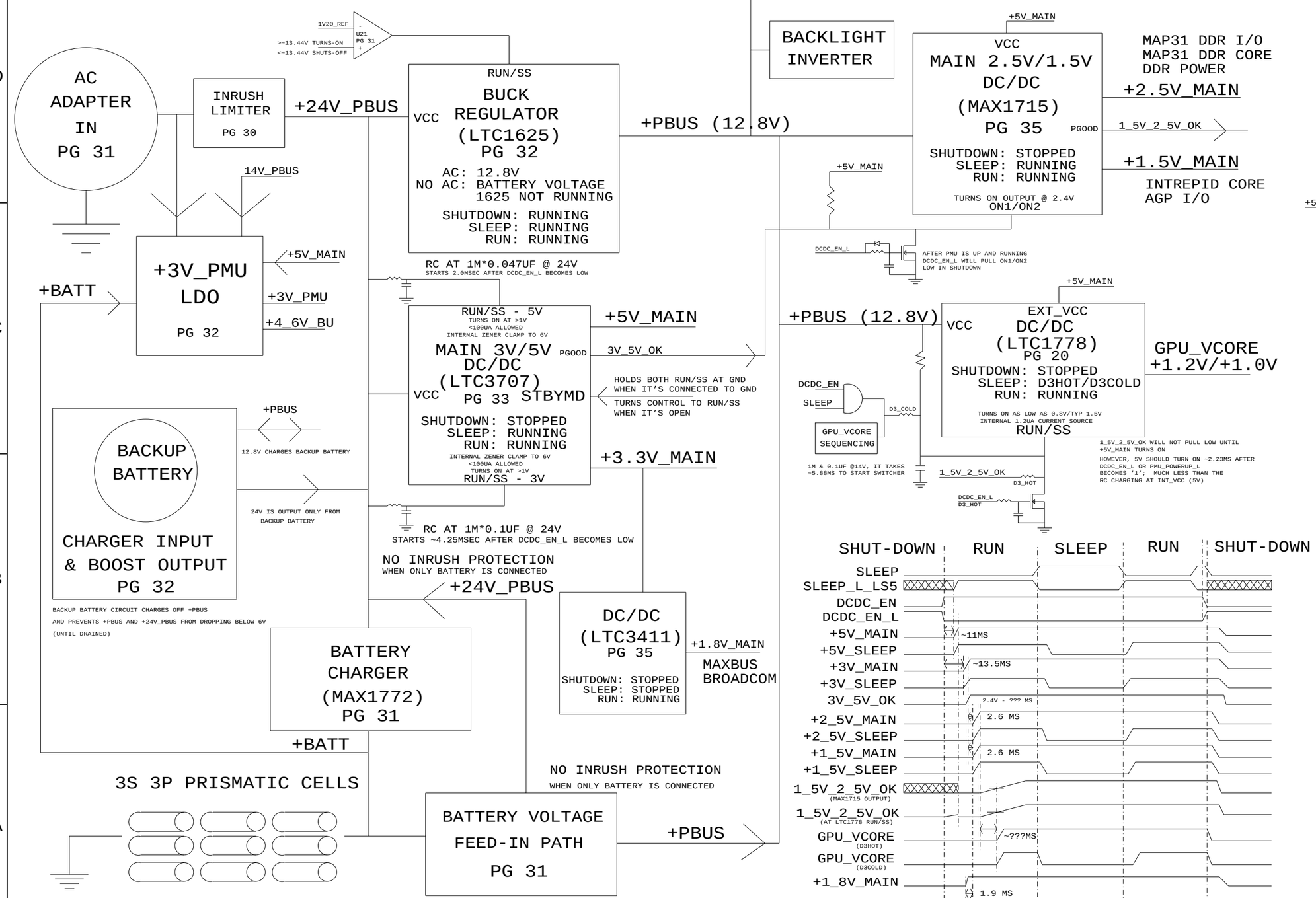
SCALE NONE	SHT 2 OF 44	

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD HOLES

ASICS HEATSINK MOUNTS

OMIT ZT10 255R158
OMIT ZT2 255R158
OMIT ZT11 255R158
OMIT ZT6 235R126
OMIT ZT16 235R126

CHASSIS MOUNTS

I/O AREA

OMIT ZT5 146R126 — CHGND5
BS1 STDOFF-2170DX150IDX35H-TH — CHGND1
OMIT ZT83 146R126 — CHGND6

INVERTER

SH1 OG-503040 SHLD-SM — CHGND2

CONDUCTIVE MOUNTS

OMIT ZT4 235R126

SPEAKER CLIPS

SP6 SPKR_CLIP_P84
SP1 SPKR_CLIP_P84
SP3 SPKR_CLIP_P84
SP5 SPKR_CLIP_P84
SP2 SPKR_CLIP_P84
SP4 SPKR_CLIP_P84

GROUND VIAS

ZT77, ZT81, ZT24, ZT38, ZT36, ZT27, ZT40, ZT39, ZT37, ZT28, ZT30, ZT34, ZT33, ZT43, ZT46 — HOLE-VIA-20R10

ZT35, ZT50, ZT44, ZT66, ZT67, ZT52, ZT53, ZT70, ZT71, ZT78, ZT69, ZT65, ZT47, ZT45, ZT49 — HOLE-VIA-20R10

ZT48, ZT56, ZT72, ZT55, ZT29, ZT74, ZT82, ZT79, ZT68, ZT60, ZT58, ZT41, ZT9, ZT7, ZT8 — HOLE-VIA-20R10

ZT57, ZT1, ZT80, ZT73, ZT75, ZT63, ZT61, ZT54, ZT51, ZT42, ZT64, ZT76, ZT62, ZT59, ZT21 — HOLE-VIA-20R10

ZT22, ZT25, ZT3, ZT32, ZT31, ZT26, ZT23, ZT19, ZT17, ZT15, ZT13, ZT12, ZT14, ZT18, ZT20 — HOLE-VIA-20R10

BOARD INFORMATION

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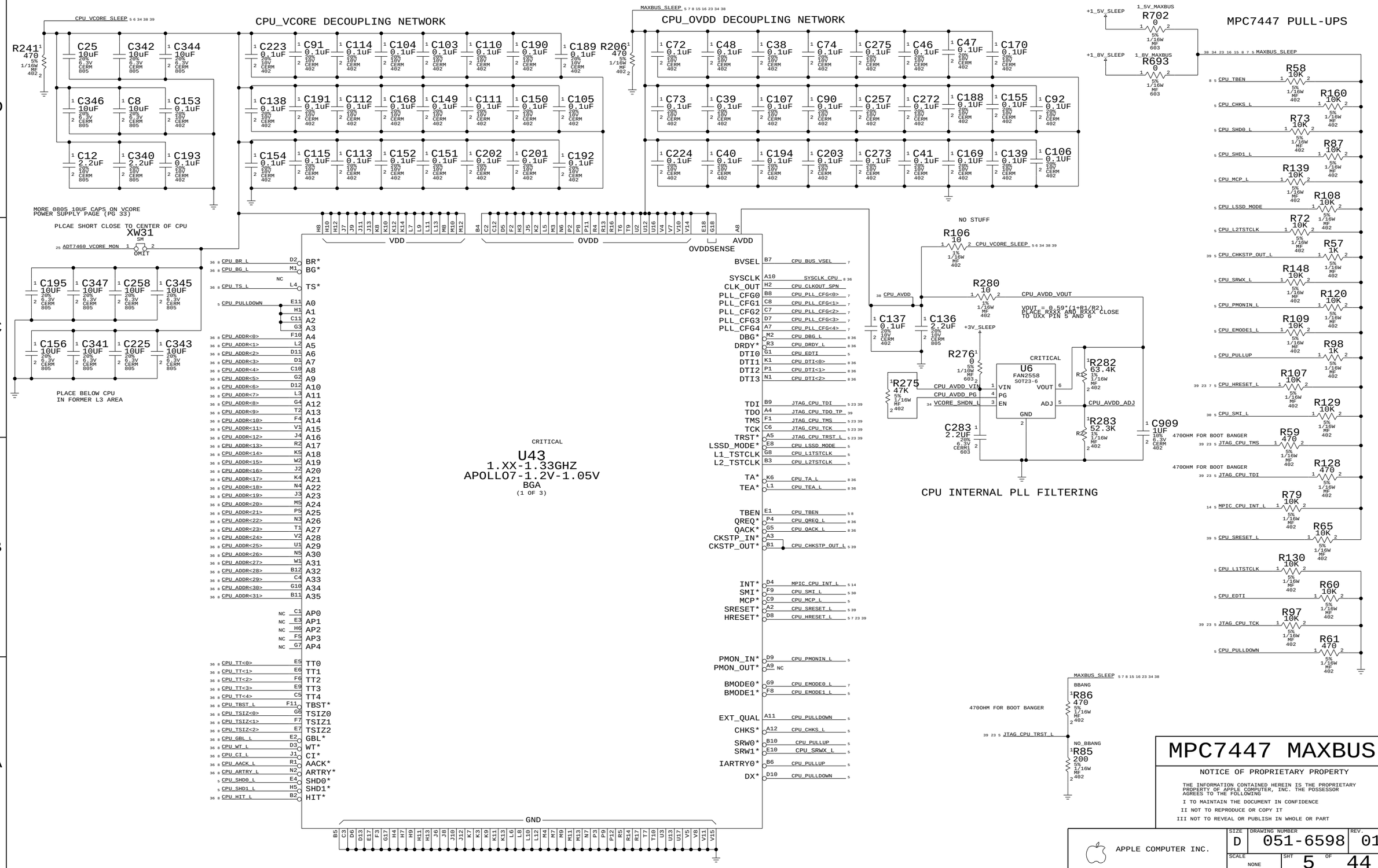
CPU_VCORE DECOUPLING NETWORK
CPU_OVDD DECOUPLING NETWORK
MPC7447 PULL-UPS
CPU_VCORE_SLEEP
MAXBUS_SLEEP
R241 470 5% 1/16W MF 402
R206 470 5% 1/16W MF 402
C25 10uF 20% 6.3V CERM 805
C342 10uF 20% 6.3V CERM 805
C344 10uF 20% 6.3V CERM 805
C346 10uF 20% 6.3V CERM 805
C8 10uF 20% 6.3V CERM 805
C153 0.1uF 20% 10V CERM 402
C12 2.2uF 20% 10V CERM 805
C340 2.2uF 20% 10V CERM 805
C193 0.1uF 20% 10V CERM 402
C223 0.1uF 20% 10V CERM 402
C91 0.1uF 20% 10V CERM 402
C114 0.1uF 20% 10V CERM 402
C104 0.1uF 20% 10V CERM 402
C103 0.1uF 20% 10V CERM 402
C110 0.1uF 20% 10V CERM 402
C190 0.1uF 20% 10V CERM 402
C189 0.1uF 20% 10V CERM 402
C138 0.1uF 20% 10V CERM 402
C191 0.1uF 20% 10V CERM 402
C112 0.1uF 20% 10V CERM 402
C168 0.1uF 20% 10V CERM 402
C149 0.1uF 20% 10V CERM 402
C111 0.1uF 20% 10V CERM 402
C150 0.1uF 20% 10V CERM 402
C105 0.1uF 20% 10V CERM 402
C154 0.1uF 20% 10V CERM 402
C115 0.1uF 20% 10V CERM 402
C113 0.1uF 20% 10V CERM 402
C152 0.1uF 20% 10V CERM 402
C151 0.1uF 20% 10V CERM 402
C202 0.1uF 20% 10V CERM 402
C201 0.1uF 20% 10V CERM 402
C192 0.1uF 20% 10V CERM 402
C72 0.1uF 20% 10V CERM 402
C48 0.1uF 20% 10V CERM 402
C38 0.1uF 20% 10V CERM 402
C74 0.1uF 20% 10V CERM 402
C275 0.1uF 20% 10V CERM 402
C46 0.1uF 20% 10V CERM 402
C47 0.1uF 20% 10V CERM 402
C170 0.1UF 20% 10V CERM 402
C73 0.1uF 20% 10V CERM 402
C39 0.1uF 20% 10V CERM 402
C107 0.1uF 20% 10V CERM 402
C90 0.1uF 20% 10V CERM 402
C257 0.1uF 20% 10V CERM 402
C272 0.1uF 20% 10V CERM 402
C188 0.1uF 20% 10V CERM 402
C155 0.1uF 20% 10V CERM 402
C92 0.1uF 20% 10V CERM 402
C224 0.1uF 20% 10V CERM 402
C40 0.1uF 20% 10V CERM 402
C194 0.1uF 20% 10V CERM 402
C203 0.1uF 20% 10V CERM 402
C273 0.1uF 20% 10V CERM 402
C41 0.1uF 20% 10V CERM 402
C169 0.1uF 20% 10V CERM 402
C139 0.1uF 20% 10V CERM 402
C106 0.1UF 20% 10V CERM 402
+1_5V_SLEEP
1_5V_MAXBUS
R702 0 5% 1/16W MF 603
+1_8V_SLEEP
1_8V_MAXBUS
R693 0 5% 1/16W MF 603
R58 10K 5% 1/16W MF 402 CPU_TBEN
R160 10K 5% 1/16W MF 402 CPU_CHKS_L
R73 10K 5% 1/16W MF 402 CPU_SHD0_L
R87 10K 5% 1/16W MF 402 CPU_SHD1_L
R139 10K 5% 1/16W MF 402 CPU_MCP_L
R108 10K 5% 1/16W MF 402 CPU_LSSD_MODE
R72 10K 5% 1/16W MF 402 CPU_L2TSTCLK
R57 1K 5% 1/16W MF 402 CPU_CHKSTP_OUT_L
R148 10K 5% 1/16W MF 402 CPU_SRWX_L
R120 10K 5% 1/16W MF 402 CPU_PMONIN_L
R109 10K 5% 1/16W MF 402 CPU_EMODE1_L
R98 1K 5% 1/16W MF 402 CPU_PULLUP
R107 10K 5% 1/16W MF 402 CPU_HRESET_L
R129 10K 5% 1/16W MF 402 CPU_SMI_L
470OHM FOR BOOT BANGER
R59 470 5% 1/16W MF 402 JTAG_CPU_TMS
470OHM FOR BOOT BANGER
R128 470 5% 1/16W MF 402 JTAG_CPU_TDI
R79 10K 5% 1/16W MF 402 MPIC_CPU_INT_L
R65 10K 5% 1/16W MF 402 CPU_SRESET_L
R130 10K 5% 1/16W MF 402 CPU_L1TSTCLK
R60 10K 5% 1/16W MF 402 CPU_EDTI
R97 10K 5% 1/16W MF 402 JTAG_CPU_TCK
R61 470 5% 1/16W MF 402 CPU_PULLDOWN
MORE 0805 10UF CAPS ON VCORE POWER SUPPLY PAGE (PG 33)
PLCAE SHORT CLOSE TO CENTER OF CPU
XW31 SM OMIT
ADT7460_VCORE_MON
C195 10UF 20% 6.3V CERM 805
C347 10UF 20% 6.3V CERM 805
C258 10UF 20% 6.3V CERM 805
C345 10UF 20% 6.3V CERM 805
C156 10UF 20% 6.3V CERM 805
C341 10UF 20% 6.3V CERM 805
C225 10UF 20% 6.3V CERM 805
C343 10UF 20% 6.3V CERM 805
PLACE BELOW CPU IN FORMER L3 AREA
VDD
OVDD
AVDD
OVDDSENSE
CPU_BR_L
CPU_BG_L
CPU_TS_L
CPU_PULLDOWN
CPU_ADDR<0>
CPU_ADDR<1>
CPU_ADDR<2>
CPU_ADDR<3>
CPU_ADDR<4>
CPU_ADDR<5>
CPU_ADDR<6>
CPU_ADDR<7>
CPU_ADDR<8>
CPU_ADDR<9>
CPU_ADDR<10>
CPU_ADDR<11>
CPU_ADDR<12>
CPU_ADDR<13>
CPU_ADDR<14>
CPU_ADDR<15>
CPU_ADDR<16>
CPU_ADDR<17>
CPU_ADDR<18>
CPU_ADDR<19>
CPU_ADDR<20>
CPU_ADDR<21>
CPU_ADDR<22>
CPU_ADDR<23>
CPU_ADDR<24>
CPU_ADDR<25>
CPU_ADDR<26>
CPU_ADDR<27>
CPU_ADDR<28>
CPU_ADDR<29>
CPU_ADDR<30>
CPU_ADDR<31>
CPU_TT<0>
CPU_TT<1>
CPU_TT<2>
CPU_TT<3>
CPU_TT<4>
CPU_TBST_L
CPU_TSIZ<0>
CPU_TSIZ<1>
CPU_TSIZ<2>
CPU_GBL_L
CPU_WT_L
CPU_CI_L
CPU_AACK_L
CPU_ARTRY_L
CPU_SHD0_L
CPU_SHD1_L
CPU_HIT_L
BR* BG* TS* A0 A1 A2 A3 A4 A5 A6 A7 A8 A9 A10 A11 A12 A13 A14 A15 A16 A17 A18 A19 A20 A21 A22 A23 A24 A25 A26 A27 A28 A29 A30 A31 A32 A33 A34 A35 AP0 AP1 AP2 AP3 AP4 TT0 TT1 TT2 TT3 TT4 TBST* TSIZ0 TSIZ1 TSIZ2 GBL* WT* CI* AACK* ARTRY* SHD0* SHD1* HIT*
BVSEL CPU_BUS_VSEL
SYSCLK SYSCLK_CPU
CLK_OUT CPU_CLKOUT_SPN
PLL_CFG0 CPU_PLL_CFG<0>
PLL_CFG1 CPU_PLL_CFG<1>
PLL_CFG2 CPU_PLL_CFG<2>
PLL_CFG3 CPU_PLL_CFG<3>
PLL_CFG4 CPU_PLL_CFG<4>
DBG* CPU_DBG_L
DRDY* CPU_DRDY_L
DTI0 CPU_EDTI
DTI1 CPU_DTI<0>
DTI2 CPU_DTI<1>
DTI3 CPU_DTI<2>
TDI JTAG_CPU_TDI
TDO JTAG_CPU_TDO_TP
TMS JTAG_CPU_TMS
TCK JTAG_CPU_TCK
TRST* JTAG_CPU_TRST_L
LSSD_MODE* CPU_LSSD_MODE
L1_TSTCLK CPU_L1TSTCLK
L2_TSTCLK CPU_L2TSTCLK
TA* CPU_TA_L
TEA* CPU_TEA_L
TBEN CPU_TBEN
QREQ* CPU_QREQ_L
QACK* CPU_QACK_L
CKSTP_IN*
CKSTP_OUT* CPU_CHKSTP_OUT_L
INT* MPIC_CPU_INT_L
SMI* CPU_SMI_L
MCP* CPU_MCP_L
SRESET* CPU_SRESET_L
HRESET* CPU_HRESET_L
PMON_IN* CPU_PMONIN_L
PMON_OUT* NC
BMODE0* CPU_EMODE0_L
BMODE1* CPU_EMODE1_L
EXT_QUAL CPU_PULLDOWN
CHKS* CPU_CHKS_L
SRW0* CPU_PULLUP
SRW1* CPU_SRWX_L
IARTRY0* CPU_PULLUP
DX* CPU_PULLDOWN
GND
CRITICAL
U43
1.XX-1.33GHZ
APOLLO7-1.2V-1.05V
BGA
(1 OF 3)
NO STUFF
R106 10 1% 1/16W MF 402 CPU_VCORE_SLEEP
R280 10 1% 1/16W MF 402 CPU_AVDD_VOUT
VOUT = 0.59*(1+R1/R2)
PLACE R2XX AND R3XX CLOSE TO U2X PIN 5 AND 6
CPU_AVDD
C137 0.1uF 20% 10V CERM 402
C136 2.2uF 20% 10V CERM 805
+3V_SLEEP
R276 0 5% 1/16W MF 603
R275 47K 5% 1/16W MF 402
CPU_AVDD_VIN
CPU_AVDD_PG
VCORE_SHDN_L
CRITICAL
U6
FAN2558
SOT23-6
VIN
PG
EN
VOUT
ADJ
GND
CPU_AVDD_ADJ
R282 63.4K 1% 1/16W MF 402
R283 52.3K 1% 1/16W MF 402
C283 2.2UF 20% 6.3V CERM1 603
C909 1UF 10% 6.3V CERM 402
CPU INTERNAL PLL FILTERING
MAXBUS_SLEEP
BBANG
R86 470 5% 1/16W MF 402
470OHM FOR BOOT BANGER
JTAG_CPU_TRST_L
NO_BBANG
R85 200 5% 1/16W MF 402
MPC7447 MAXBUS
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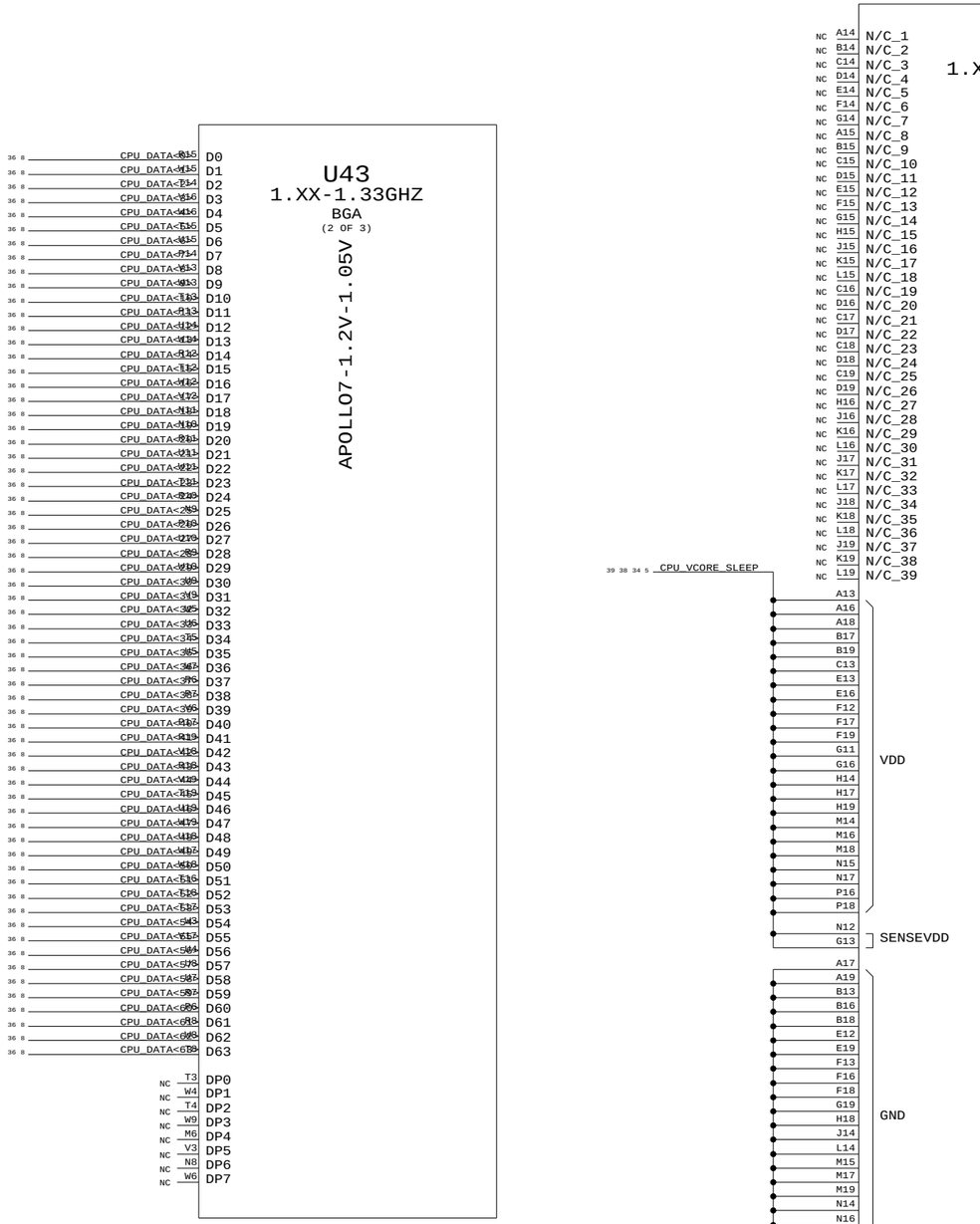
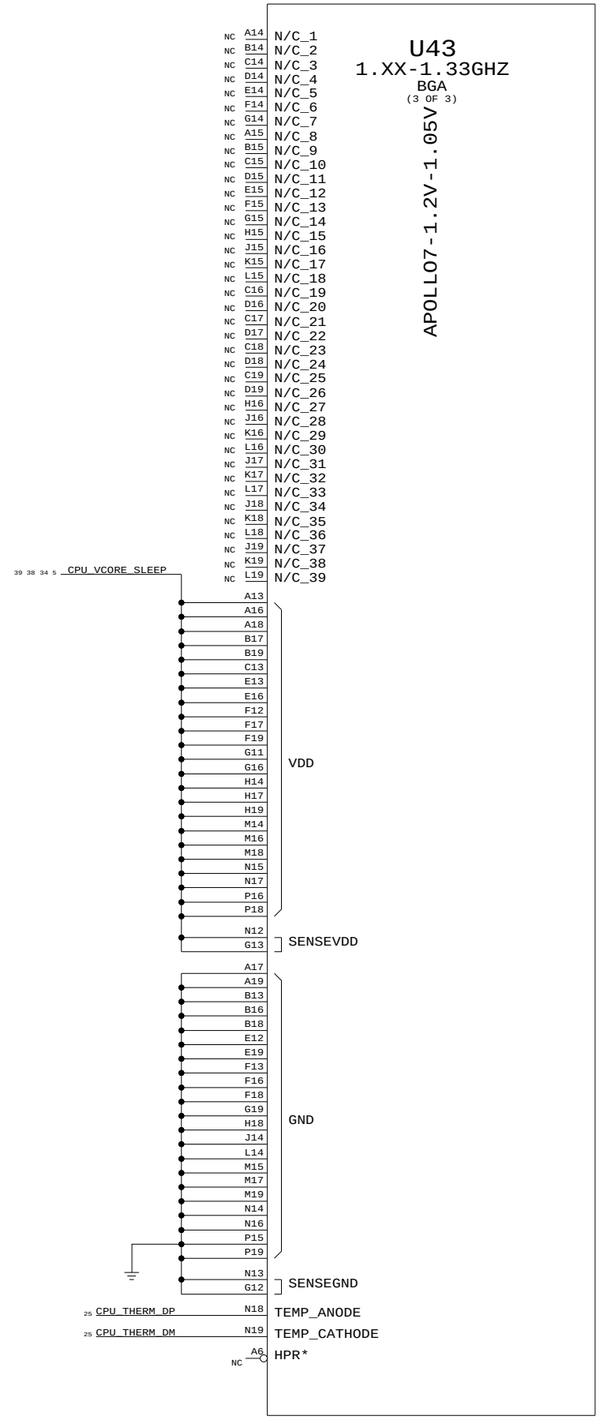
SIZE D
DRAWING NUMBER 051-6598
REV. 01
SCALE NONE
SHT 5 OF 44

BOOT BANGER - LMU PERORMS THIS FUNCTION IF NEEDED
SEE PAGE 22





MPC7447/BBANG

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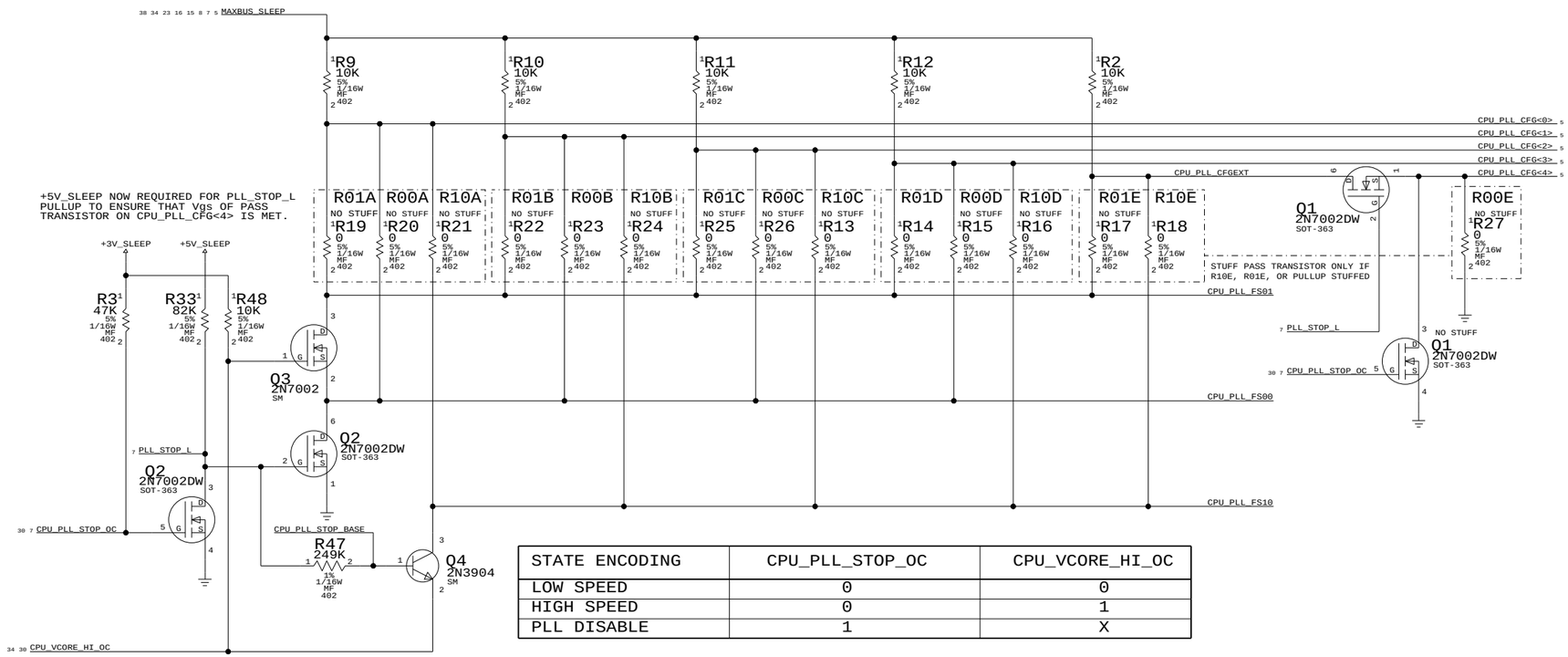
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6598	01

SCALE NONE | SHT 6 OF 44

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

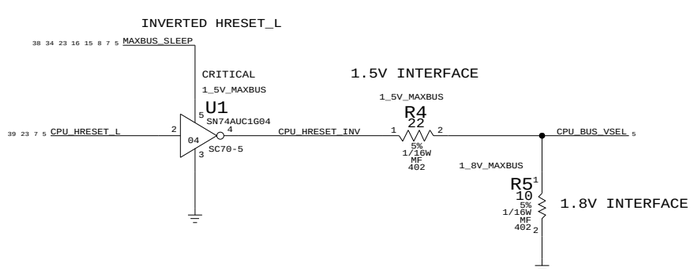
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ (MHZ)	CPU_PLL_CFG 4 E	0123 ABCD	HEX
0.0X	PLL OFF		0	1111	0F
1.0X	PLL BYPASS		0	0011	03
2.0X	333	267	0	0100	04
3.0X	500	400	0	1000	08
4.0X	667	533	0	1010	0A
5.0X	833	667	0	1011	0B
5.5X	917	733	0	1001	09
6.0X	1000	800	0	1101	0D
6.5X	1083	867	0	0101	05
7.0X	1167	933	0	0010	02
7.5X	1250	1000	0	0001	01
8.0X	1333	1067	0	1100	0C
8.5X	1417	1133	0	0110	06
9.0X	1500	1200	1	0111	17
9.5X	1583	1267	0	0111	07
10.0X	1667	1333	1	1010	1A
10.5X	1750	1400	1	1000	18
11.0X	1833	1467	1	1001	19
11.5X	1917	1533	0	0000	00
12.0X	2000	1600	1	1011	1B
12.5X	2083	1667	1	1111	1F
13.0X	2167	1733	1	0101	15
13.5X	2250	1800	0	1110	0E
14.0X	2333	1867	1	1100	1C
15.0X	2500	2000	1	0001	11
16.0X	2667	2133	1	1101	1D
17.0X	2833	2267	1	0000	10
18.0X	3000	2400	1	0010	12
20.0X	3333	2667	1	0011	13
21.0X	3500	2800	1	0100	14
24.0X	4000	3200	1	0110	16
28.0X	4667	3733	1	1110	1E

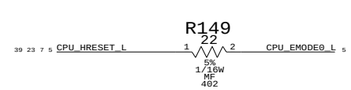
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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SCALE NONE | SHT 7 OF 44

INTREPID BOOT STRAPS

BIT 32 TO 39

MAXBUS_SLEEP

Resistor	Stuffing	Signal	Function
R642	NO STUFF	CPU_DATA<32>	DDR_TPWRDEnable_h 0: Tpd output 1: Tpd input
R135	NO STUFF	CPU_DATA<33>	Analyzerclk_En_h 0: Inactive 1: Active
R123	NO STUFF	CPU_DATA<34>	DDR_TPDDE_Pol 0: Active high 1: Active low
R153	NO STUFF	CPU_DATA<35>	ExtPLL_SDwn_Pol 0: Active high 1: Active low
R166	NO STUFF	CPU_DATA<36>	Spare
R179	NO STUFF	CPU_DATA<37>	Spare
R651	NO STUFF	CPU_DATA<38>	Spare
R178	NO STUFF	CPU_DATA<39>	Spare
R136		CPU_DATA<33>	
R643		CPU_DATA<34>	
R639		CPU_DATA<35>	
R657	NO STUFF	CPU_DATA<36>	
R664		CPU_DATA<37>	
R673		CPU_DATA<38>	
R143		CPU_DATA<39>	
R674			

BIT 40 TO 47

MAXBUS_SLEEP

Resistor	Stuffing	Signal	Function
R122	NO STUFF	CPU_DATA<40>	
R142	NO STUFF	CPU_DATA<41>	
R164	NO STUFF	CPU_DATA<42>	
R134	SSCG	CPU_DATA<43>	
R184	NO STUFF	CPU_DATA<44>	
R177	NO_SSCG	CPU_DATA<45>	
R152	NO_SSCG	CPU_DATA<46>	
R165	NO_SSCG	CPU_DATA<47>	
R640		CPU_DATA<40>	
R652		CPU_DATA<41>	
R665		CPU_DATA<42>	
R644	NO_SSCG	CPU_DATA<43>	
R683		CPU_DATA<44>	
R675	SSCG	CPU_DATA<45>	
R658	SSCG	CPU_DATA<46>	
R666	SSCG	CPU_DATA<47>	

Spare, Spare, BIT2, BIT1, BIT0, InternalspreadEn 1: Active, PCI1_Source Clock 0: PLL4 1: PLL5 (NO SPREAD), PCI0_Source Clock 0: PLL5 1: PLL4 (NO SPREAD)

PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ

MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION

BIT 48 TO 55

MAXBUS_SLEEP

Resistor	Stuffing	Signal	Function
R133	SSCG	CPU_DATA<48>	
R121	SSCG	CPU_DATA<49>	
R163	NO STUFF	CPU_DATA<50>	
R151	NO STUFF	CPU_DATA<51>	
R162	NO STUFF	CPU_DATA<52>	
R141	NO STUFF	CPU_DATA<53>	
R183		CPU_DATA<54>	
R176	NO STUFF	CPU_DATA<55>	
R645	NO_SSCG	CPU_DATA<48>	
R641	NO_SSCG	CPU_DATA<49>	
R668	NO STUFF	CPU_DATA<50>	
R659		CPU_DATA<51>	
R667		CPU_DATA<52>	
R653		CPU_DATA<53>	
R684	NO STUFF	CPU_DATA<54>	
R676		CPU_DATA<55>	

BUF_REF_CLK_OUTEnable_h 1: Active, SetPLL_extSrc 0: External source, Spare, TI 1394b workaround 0: TI PHY workaround 1: Std PHY workaround, BIT2, BIT1, BIT0, Spare

MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm

THE FOLLOWING STRAP BITS CAN BE CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT

IF A STRAP IS NOT LISTED, THEN IT CANNOT BE CHANGED BY SOFTWARE

R227 4.7 5% 1/16W MF 402 — +1_5V_INTREPID_PLL → +1_5V_INTREPID_PLL7

C308 0.22UF 20% 6.3V CERM 402

U45 INTREPID-REV2.1 BGA (1 OF 9) — MAXBUS INTERFACE

VDD15A_7 (PLL6) H26 — CRITICAL

Pin	Signal	Type
E29	CPU_BR_L	BR INPUT
E26	CPU_BG_L	BG NO BUS KEEPER
B27	CPU_TS_L	TS NO BUS KEEPER
D24	CPU_ADDR<0>	A_0
D25	CPU_ADDR<1>	A_1
A27	CPU_ADDR<2>	A_2
E24	CPU_ADDR<3>	A_3
G23	CPU_ADDR<4>	A_4
B26	CPU_ADDR<5>	A_5
A26	CPU_ADDR<6>	A_6
D23	CPU_ADDR<7>	A_7
A25	CPU_ADDR<8>	A_8
E23	CPU_ADDR<9>	A_9
J22	CPU_ADDR<10>	A_10
B25	CPU_ADDR<11>	A_11
H22	CPU_ADDR<12>	A_12
G22	CPU_ADDR<13>	A_13
D22	CPU_ADDR<14>	A_14
B24	CPU_ADDR<15>	A_15
B23	CPU_ADDR<16>	A_16
E22	CPU_ADDR<17>	A_17
J21	CPU_ADDR<18>	A_18
G21	CPU_ADDR<19>	A_19
E21	CPU_ADDR<20>	A_20
A24	CPU_ADDR<21>	A_21
D21	CPU_ADDR<22>	A_22
A23	CPU_ADDR<23>	A_23
H20	CPU_ADDR<24>	A_24
B22	CPU_ADDR<25>	A_25
H21	CPU_ADDR<26>	A_26
A22	CPU_ADDR<27>	A_27
E20	CPU_ADDR<28>	A_28
B21	CPU_ADDR<29>	A_29
D20	CPU_ADDR<30>	A_30
A21	CPU_ADDR<31>	A_31
G26	CPU_CI_L	CI
A29	CPU_GBL_L	GBL
A28	CPU_TBST_L	TBST
G24	CPU_TSIZ<0>	TSIZ_0
H24	CPU_TSIZ<1>	TSIZ_1
D26	CPU_TSIZ<2>	TSIZ_2
E25	CPU_TT<0>	TT_0
G25	CPU_TT<1>	TT_1
B28	CPU_TT<2>	TT_2
D27	CPU_TT<3>	TT_3
J25	CPU_TT<4>	TT_4
D28	CPU_WT_L	WT
B29	CPU_AACK_L	AACK NO BUS KEEPER - PU
H23	CPU_ARTRY_L	ARTRY NO BUS KEEPER - PU
B31	CPU_HIT_L	HIT INPUT - PU
A32	CPU_QREQ_L	QREQ INPUT - PD
G27	CPU_QACK_L	QACK NO BUS KEEPER - ?
AK9	INT_SUSPEND_REQ_L	SUSPENDREQ
AM8	INT_SUSPEND_ACK_L	SUSPENDACK
J24	INT_CPUFB_IN	CPU_FB_IN
H16	INT_CPUFB_OUT	CPU_FB_OUT NO BUS KEEPER - PU
G8	SYSCLK_LA_TP	ANALYZER_CLK
AH9	CPU_CLK_EN	STOPCPUCLK INPUT - PU
H13	INTREPID_ACS_REF	ACS_REF NO BUS KEEPER - ?
J15	SYSCLK_CPU_UF	CPU_CLK NO BUS KEEPER - PU
A31	CPU_TBEN	TBEN NO BUS KEEPER - PU
D10	CPU_DATA<0>	D_0
G12	CPU_DATA<1>	D_1
E11	CPU_DATA<2>	D_2
H11	CPU_DATA<3>	D_3
B9	CPU_DATA<4>	D_4
B8	CPU_DATA<5>	D_5
A9	CPU_DATA<6>	D_6
A8	CPU_DATA<7>	D_7
E12	CPU_DATA<8>	D_8
D11	CPU_DATA<9>	D_9
B10	CPU_DATA<10>	D_10
J13	CPU_DATA<11>	D_11
A10	CPU_DATA<12>	D_12
D12	CPU_DATA<13>	D_13
E13	CPU_DATA<14>	D_14
G13	CPU_DATA<15>	D_15
B11	CPU_DATA<16>	D_16
D13	CPU_DATA<17>	D_17
A11	CPU_DATA<18>	D_18
G14	CPU_DATA<19>	D_19
H14	CPU_DATA<20>	D_20
E14	CPU_DATA<21>	D_21
B12	CPU_DATA<22>	D_22
G15	CPU_DATA<23>	D_23
B13	CPU_DATA<24>	D_24
H15	CPU_DATA<25>	D_25
D14	CPU_DATA<26>	D_26
B14	CPU_DATA<27>	D_27
A12	CPU_DATA<28>	D_28
G16	CPU_DATA<29>	D_29
E15	CPU_DATA<30>	D_30
J16	CPU_DATA<31>	D_31
D15	CPU_DATA<32>	D_32
A14	CPU_DATA<33>	D_33
A13	CPU_DATA<34>	D_34
D16	CPU_DATA<35>	D_35
E16	CPU_DATA<36>	D_36
G17	CPU_DATA<37>	D_37
B15	CPU_DATA<38>	D_38
H17	CPU_DATA<39>	D_39
A15	CPU_DATA<40>	D_40
B16	CPU_DATA<41>	D_41
E17	CPU_DATA<42>	D_42
A16	CPU_DATA<43>	D_43
J18	CPU_DATA<44>	D_44
H18	CPU_DATA<45>	D_45
D17	CPU_DATA<46>	D_46
G18	CPU_DATA<47>	D_47
A17	CPU_DATA<48>	D_48
B17	CPU_DATA<49>	D_49
E18	CPU_DATA<50>	D_50
B18	CPU_DATA<51>	D_51
D18	CPU_DATA<52>	D_52
A18	CPU_DATA<53>	D_53
A19	CPU_DATA<54>	D_54
H19	CPU_DATA<55>	D_55
B19	CPU_DATA<56>	D_56
J19	CPU_DATA<57>	D_57
A20	CPU_DATA<58>	D_58
D19	CPU_DATA<59>	D_59
E19	CPU_DATA<60>	D_60
G19	CPU_DATA<61>	D_61
B20	CPU_DATA<62>	D_62
G20	CPU_DATA<63>	D_63
A30	CPU_DBG_L	DBG
G28	CPU_DRDY_L	DRDY
K25	CPU_DTI<0>	DTI_0
D29	CPU_DTI<1>	DTI_1
B30	CPU_DTI<2>	DTI_2
E27	CPU_TA_L	TA
E28	CPU_TEA_L	TEA

Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)

INTREPID OUTPUTS HIGH BY DEFAULT

VSSA_7 (PLL6) H25

FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE

R197 511 1% 1/16W MF 402

R144 0 5% 1/16W MF 402 — SYSCLK_CPU

R137 1K 1% 1/16W MF 402

SHORT = 1" SHORTER THAN MATCHED LENGTH

R167 0 5% 1/16W MF 402 — INT_CPUFB_OUT → INT_CPUFB_OUT_SHORT

R215 0 5% 1/16W MF 402 — INT_CPUFB_OUT_SHORT → INT_CPUFB_OUT_NORM

R225 0 5% 1/16W MF 402 — NO STUFF

R226 0 5% 1/16W MF 402 — INT_CPUFB_IN

R208 0 5% 1/16W MF 402 — NO STUFF

R196 0 5% 1/16W MF 402 — INT_CPUFB_IN_NORM

LONG = 1" LONGER THAN MATCHED LENGTH

R207 0 5% 1/16W MF 402 — INT_CPUFB_OUT_NORM → INT_CPUFB_LONG

MAXBUS PULL-UPS

MAXBUS_SLEEP

Resistor	Signal
RP21 10K	CPU_TS_L
RP21 10K	CPU_TA_L
RP21 10K	CPU_ARTRY_L
RP23 10K	CPU_BR_L
RP24 10K	CPU_HIT_L
RP23 10K	CPU_DRDY_L
RP23 10K	CPU_TEA_L
RP23 10K	CPU_AACK_L
RP24 10K	CPU_DBG_L
RP21 10K	CPU_BG_L
RP24 10K	CPU_QREQ_L

5% 1/16W SM1

INTREPID BOOT STRAPS

BIT 56 TO 63

MAXBUS_SLEEP

Resistor	Stuffing	Signal	Function
R140	NO STUFF	CPU_DATA<56>	
R161	NO STUFF	CPU_DATA<57>	
R175	NO STUFF	CPU_DATA<58>	
R132	NO STUFF	CPU_DATA<59>	
R131	NO STUFF	CPU_DATA<60>	
R150	NO STUFF	CPU_DATA<61>	
R174		CPU_DATA<62>	
R182	NO STUFF	CPU_DATA<63>	
R654		CPU_DATA<56>	
R669		CPU_DATA<57>	
R677		CPU_DATA<58>	
R646		CPU_DATA<59>	
R647		CPU_DATA<60>	
R660		CPU_DATA<61>	
R678	NO STUFF	CPU_DATA<62>	
R685		CPU_DATA<63>	

Spare, Spare, Spare, PCI1_REQ2_L 0: GPIO 1: PCI1_GNT2_L, PCI1_REQ1_L 0: GPIO 1: PCI1_GNT1_L, PCI1_REQ0_L 0: GPIO 1: PCI1_GNT0_L, Ethernet PHY interface 0: Legacy interface 1: B-Mode interface, Processor Bus Mode 0: 60x bus (32) 1: 60x bus (64)

Intrepid MaxBus

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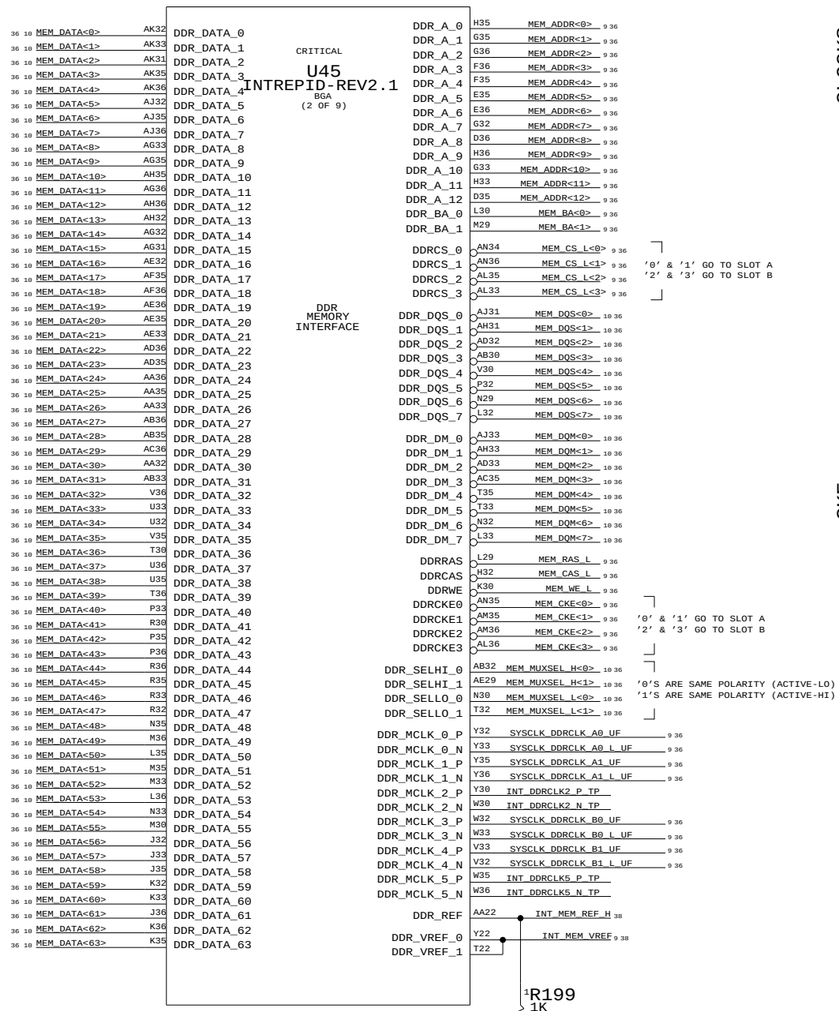
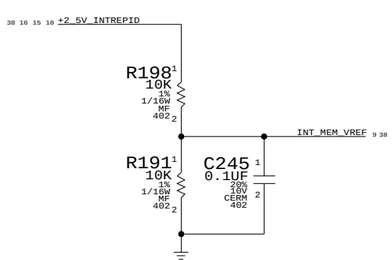
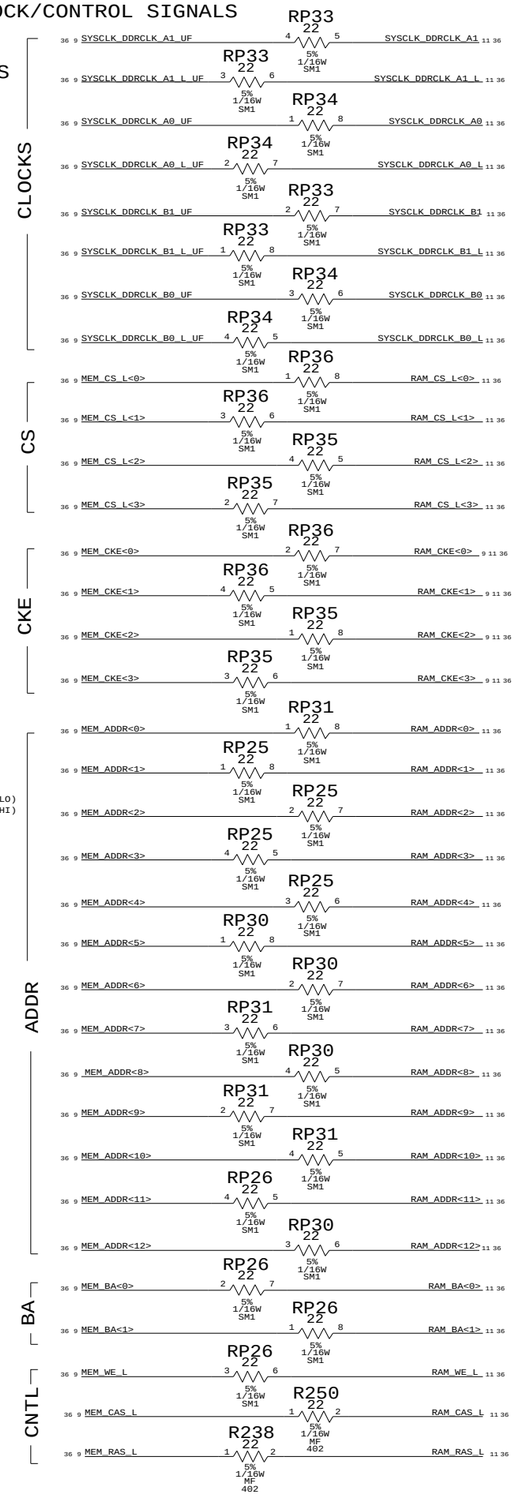
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

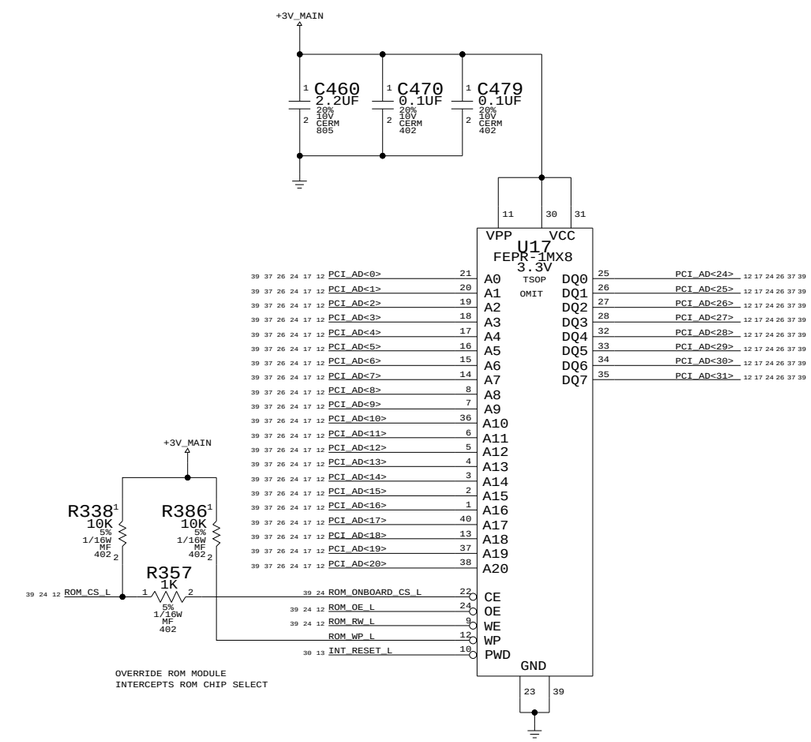


MEM_VREF



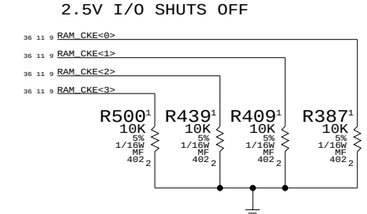


1MB BOOT ROM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1464	1	BOOTROM,PROTO,Q41A	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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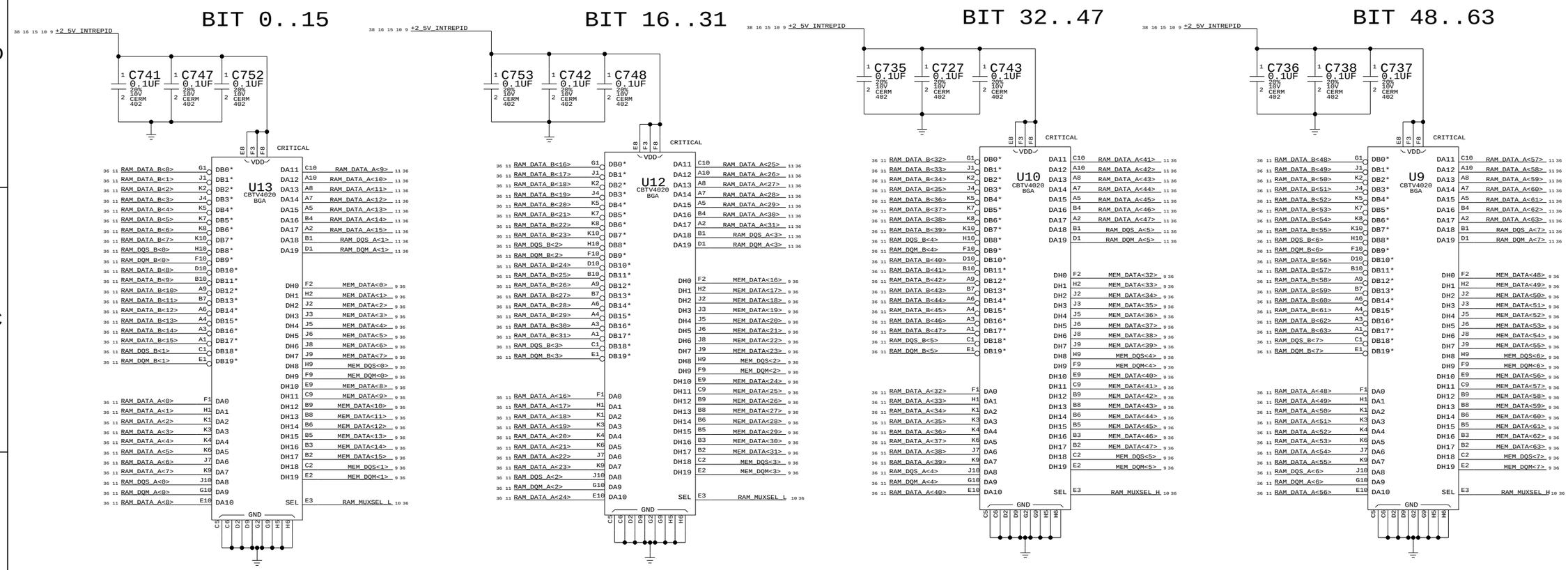
SHT 9 OF 44



SEL = LOW; HOST = B PORT; A PORT = 100OHM TO GND
SEL = HIGH; HOST = A PORT; B PORT = 100OHM TO GND
MEM_MUXSEL_H<0> AND MEM_MUXSEL_L<0> ARE ACTIVE LOW
MEM_MUXSEL_H<1> AND MEM_MUXSEL_L<1> ARE ACTIVE HIGH

ADDED 0 OHM RESISTORS IN CASE POLARITY IS WRONG

16BIT 2:1 DDR MUXES

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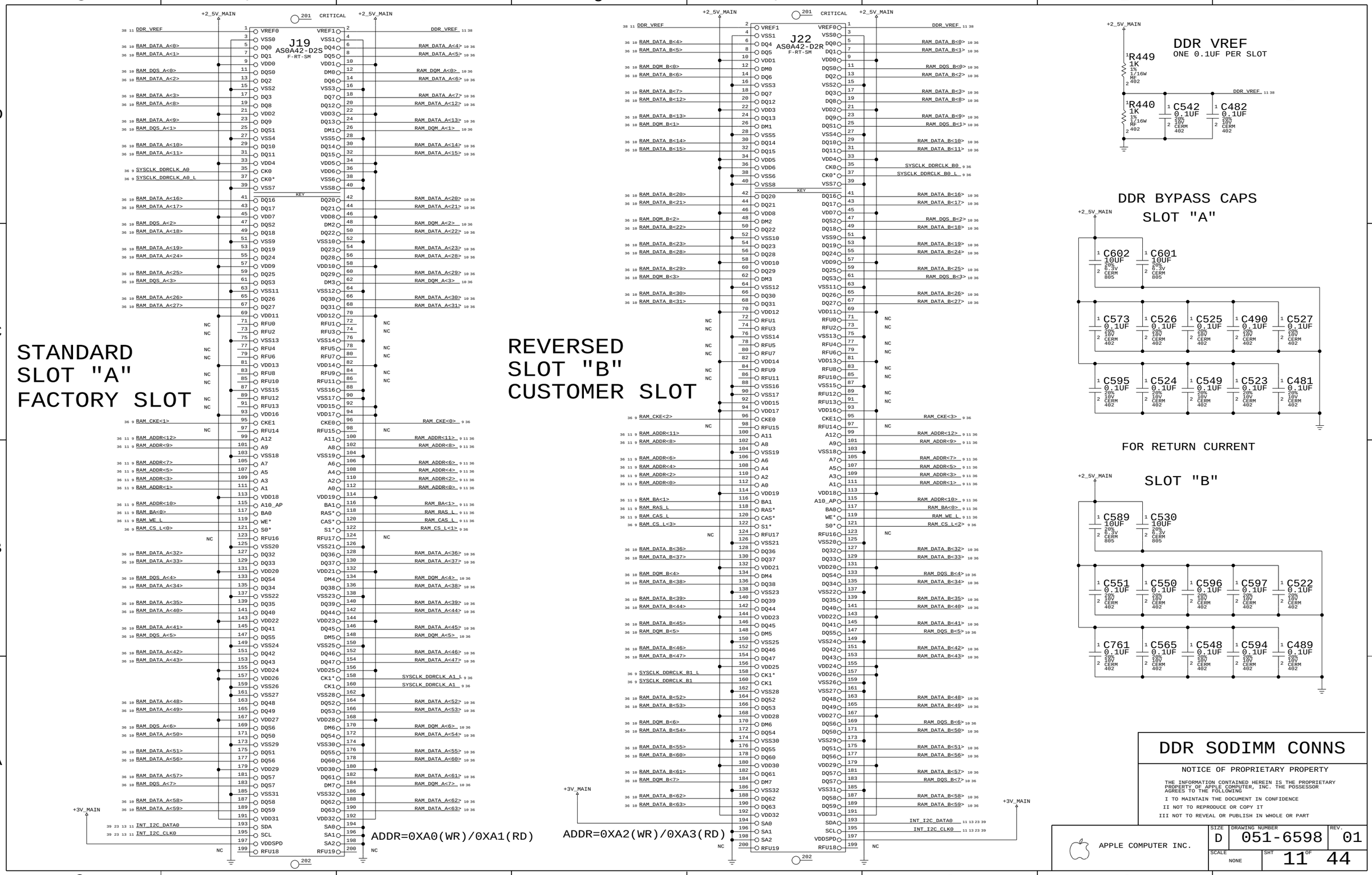
STANDARD
SLOT "A"
FACTORY SLOT
J19
AS0A42-D2S
F-RT-SM
REVERSED
SLOT "B"
CUSTOMER SLOT
J22
AS0A42-D2R
F-RT-SM
ADDR=0XA0(WR)/0XA1(RD)
ADDR=0XA2(WR)/0XA3(RD)
DDR VREF
ONE 0.1UF PER SLOT
DDR BYPASS CAPS
SLOT "A"
FOR RETURN CURRENT
SLOT "B"
DDR SODIMM CONNS
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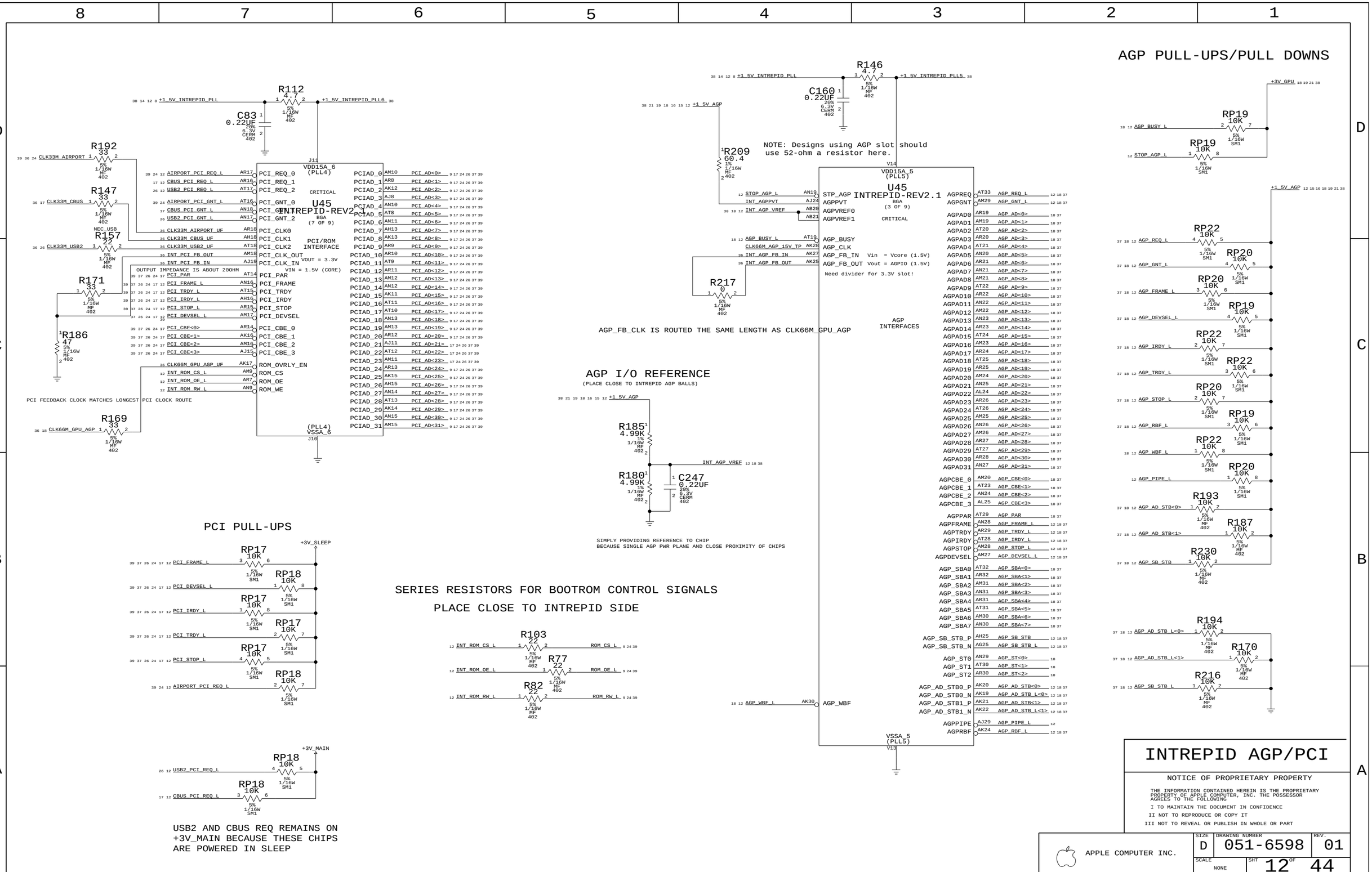
DRAWING NUMBER 051-6598
REV. 01
SCALE NONE
SHT 11 OF 44


AGP PULL-UPS/PULL DOWNS
U45
INTREPID-REV2.1
BGA
(7 OF 9)
CRITICAL
PCI/ROM INTERFACE
VDD15A_6 (PLL4)
VSSA_6 (PLL4)
VOUT = 3.3V
VIN = 1.5V (CORE)
OUTPUT IMPEDANCE IS ABOUT 200HM
PCI FEEDBACK CLOCK MATCHES LONGEST PCI CLOCK ROUTE
NEC_USB
R112 4.7
C83 0.22UF
R192 33
R147 33
R157 22
R171 33
R186 47
R169 33
PCI_REQ_0
PCI_REQ_1
PCI_REQ_2
PCI_GNT_0
PCI_GNT_1
PCI_GNT_2
PCI_CLK0
PCI_CLK1
PCI_CLK2
PCI_CLK_OUT
PCI_CLK_IN
PCI_PAR
PCI_FRAME
PCI_TRDY
PCI_IRDY
PCI_STOP
PCI_DEVSEL
PCI_CBE_0
PCI_CBE_1
PCI_CBE_2
PCI_CBE_3
ROM_OVRLY_EN
ROM_CS
ROM_OE
ROM_WE
PCIAD_0
PCIAD_1
PCIAD_2
PCIAD_3
PCIAD_4
PCIAD_5
PCIAD_6
PCIAD_7
PCIAD_8
PCIAD_9
PCIAD_10
PCIAD_11
PCIAD_12
PCIAD_13
PCIAD_14
PCIAD_15
PCIAD_16
PCIAD_17
PCIAD_18
PCIAD_19
PCIAD_20
PCIAD_21
PCIAD_22
PCIAD_23
PCIAD_24
PCIAD_25
PCIAD_26
PCIAD_27
PCIAD_28
PCIAD_29
PCIAD_30
PCIAD_31
R146 4.7
C160 0.22UF
R209 60.4
NOTE: Designs using AGP slot should use 52-ohm a resistor here.
R217 0
AGP_FB_CLK IS ROUTED THE SAME LENGTH AS CLK66M_GPU_AGP
AGP I/O REFERENCE
(PLACE CLOSE TO INTREPID AGP BALLS)
R185 4.99K
R180 4.99K
C247 0.22UF
SIMPLY PROVIDING REFERENCE TO CHIP BECAUSE SINGLE AGP PWR PLANE AND CLOSE PROXIMITY OF CHIPS
VDD15A_5 (PLL5)
VSSA_5 (PLL5)
STP_AGP
AGPPVT
AGPVREF0
AGPVREF1
AGP_BUSY
AGP_CLK
AGP_FB_IN Vin = Vcore (1.5V)
AGP_FB_OUT Vout = AGPIO (1.5V)
Need divider for 3.3V slot!
AGP_WBF
AGP INTERFACES
PCI PULL-UPS
+3V_SLEEP
RP17 10K
RP18 10K
SERIES RESISTORS FOR BOOTROM CONTROL SIGNALS
PLACE CLOSE TO INTREPID SIDE
R103 22
R77 22
R82 22
+3V_MAIN
USB2 AND CBUS REQ REMAINS ON +3V_MAIN BECAUSE THESE CHIPS ARE POWERED IN SLEEP
RP19 10K
RP22 10K
RP20 10K
R193 10K
R187 10K
R230 10K
R194 10K
R170 10K
R216 10K
INTREPID AGP/PCI
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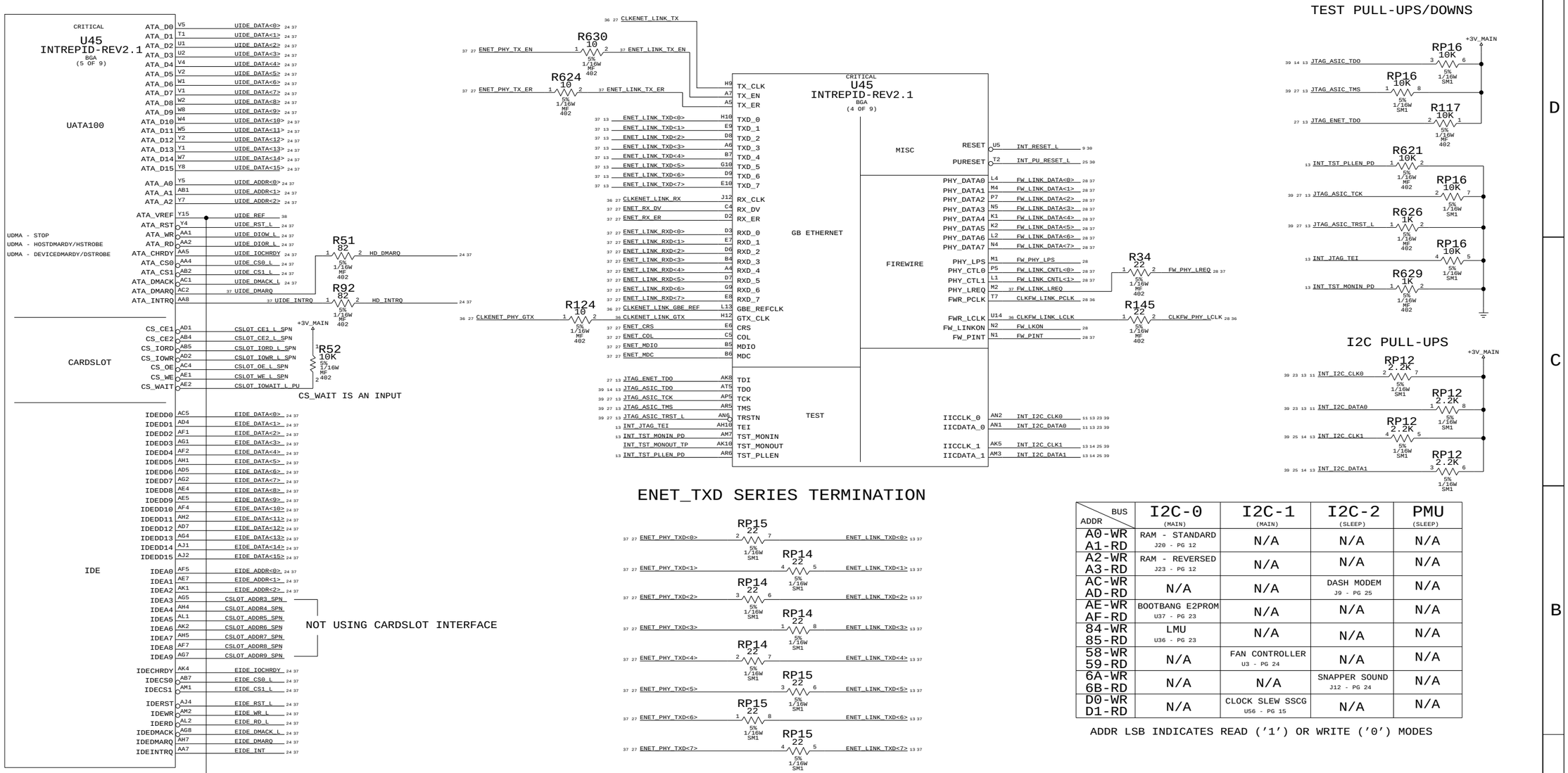
REV. 01
SCALE NONE
SHT 12 OF 44



ADDR \ BUS	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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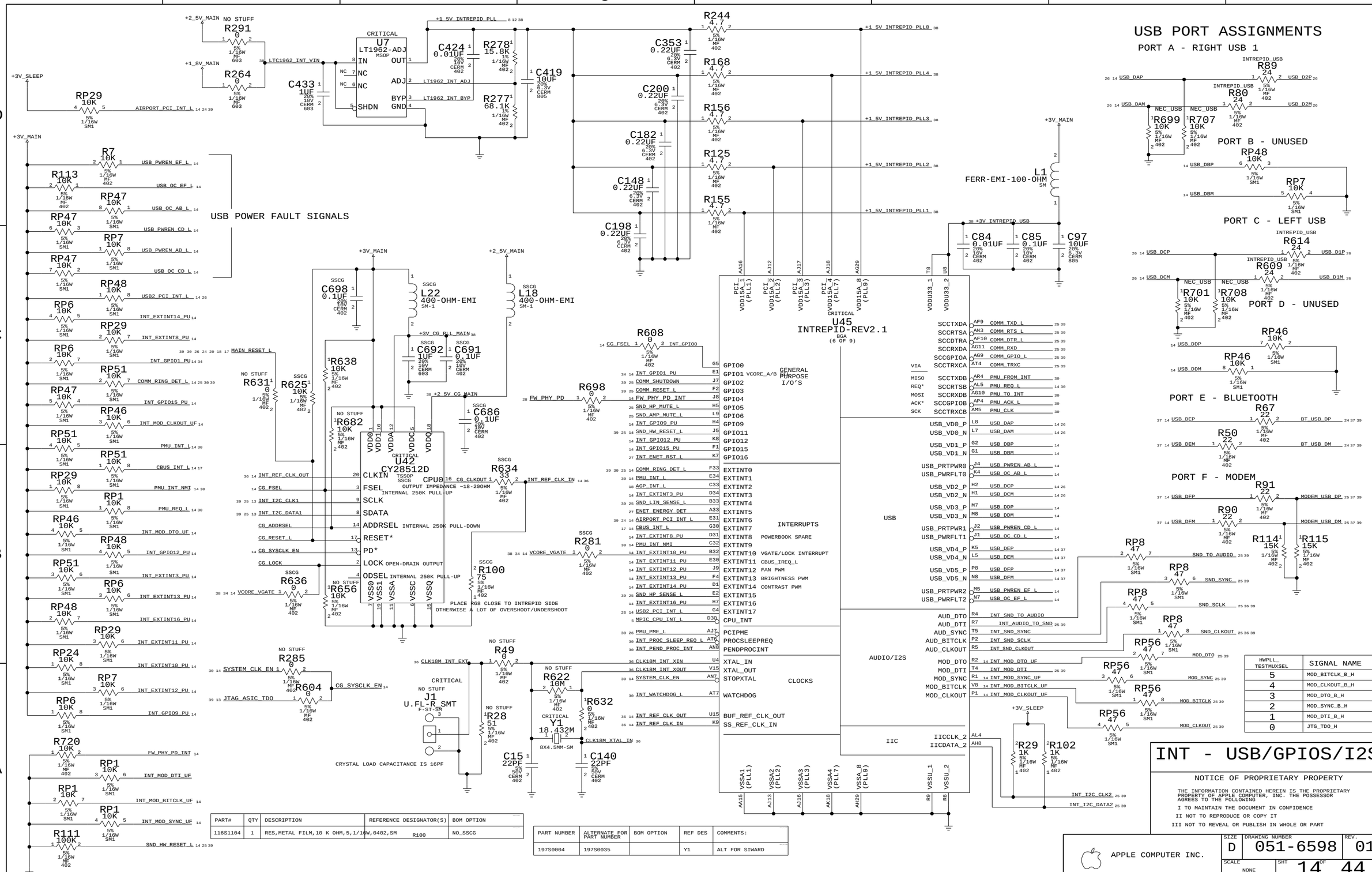

HWPLL_ TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0004	197S0035		Y1	ALT FOR SIWARD

INT - USB/GPIOS/I2S

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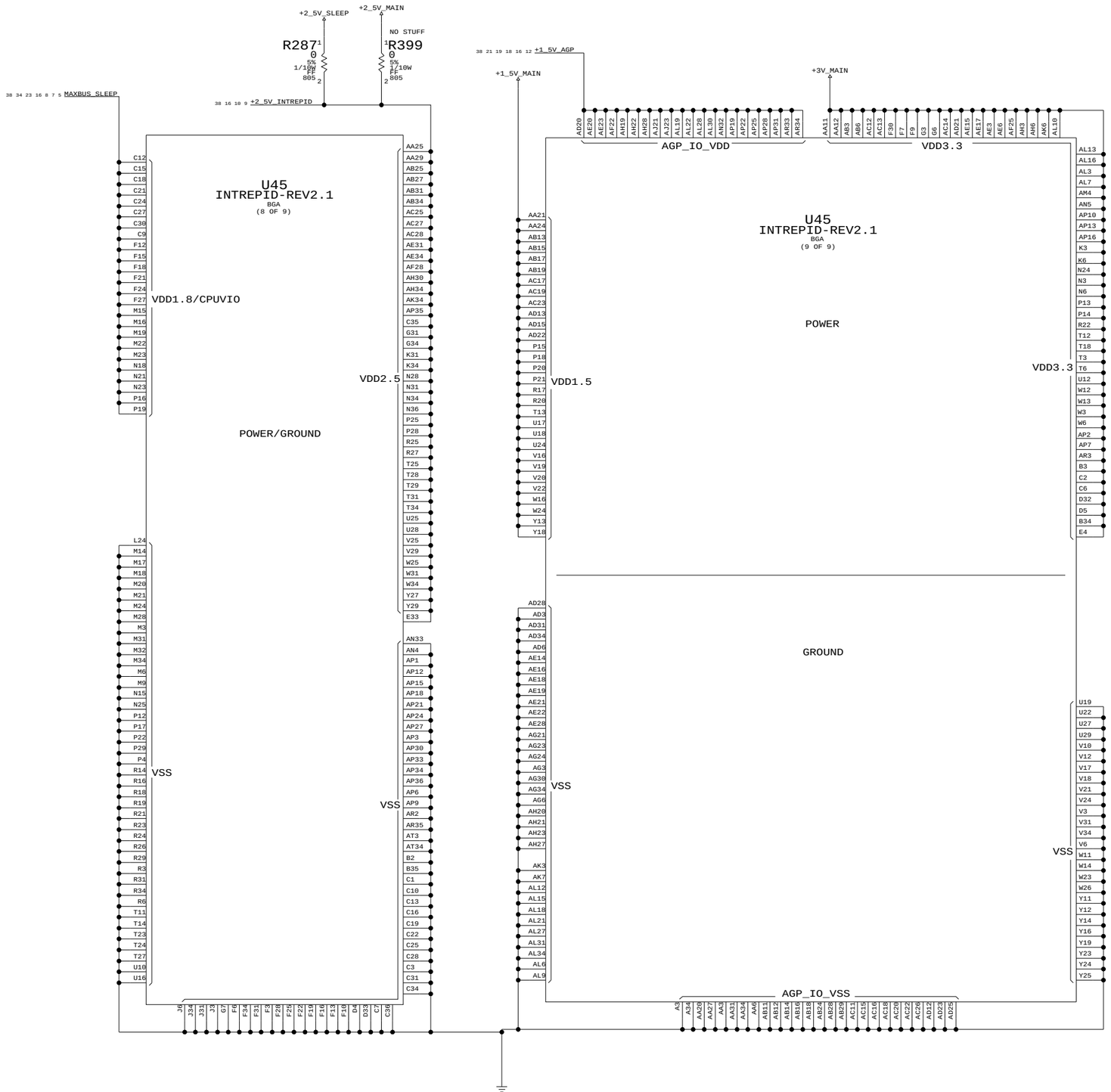

Intrepid Power

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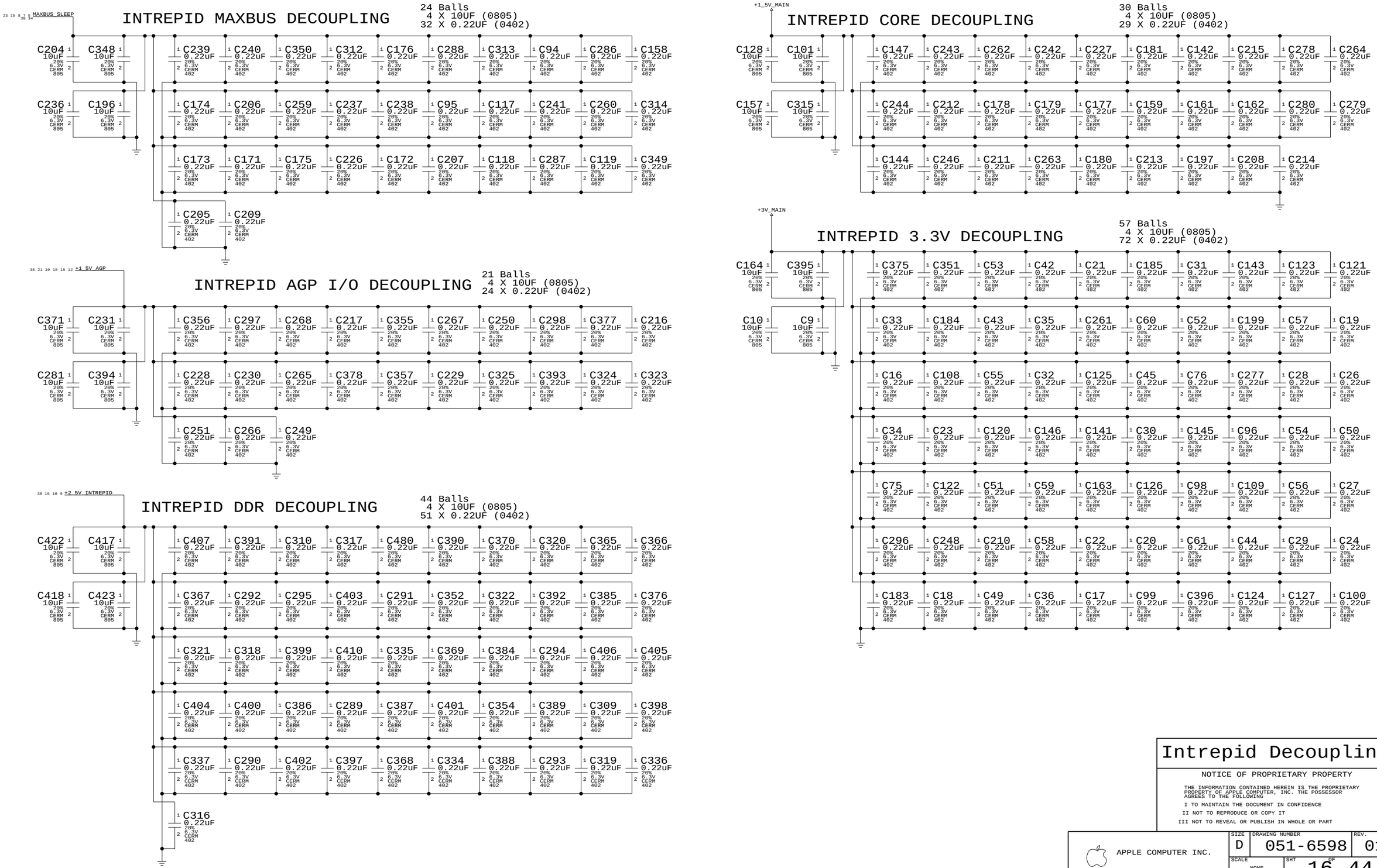

Intrepid Decoupling

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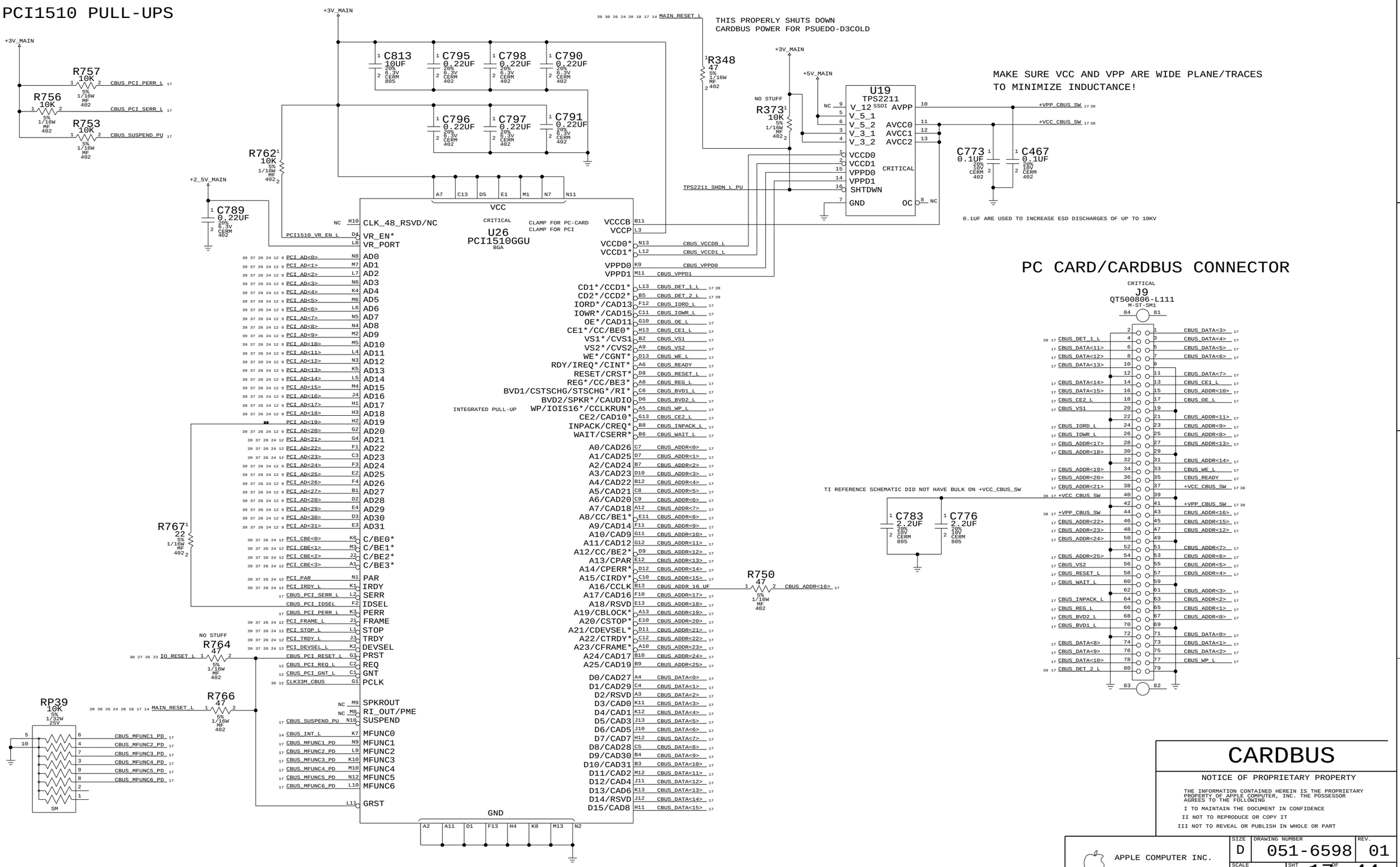
PCI1510 PULL-UPS



CARDBUS

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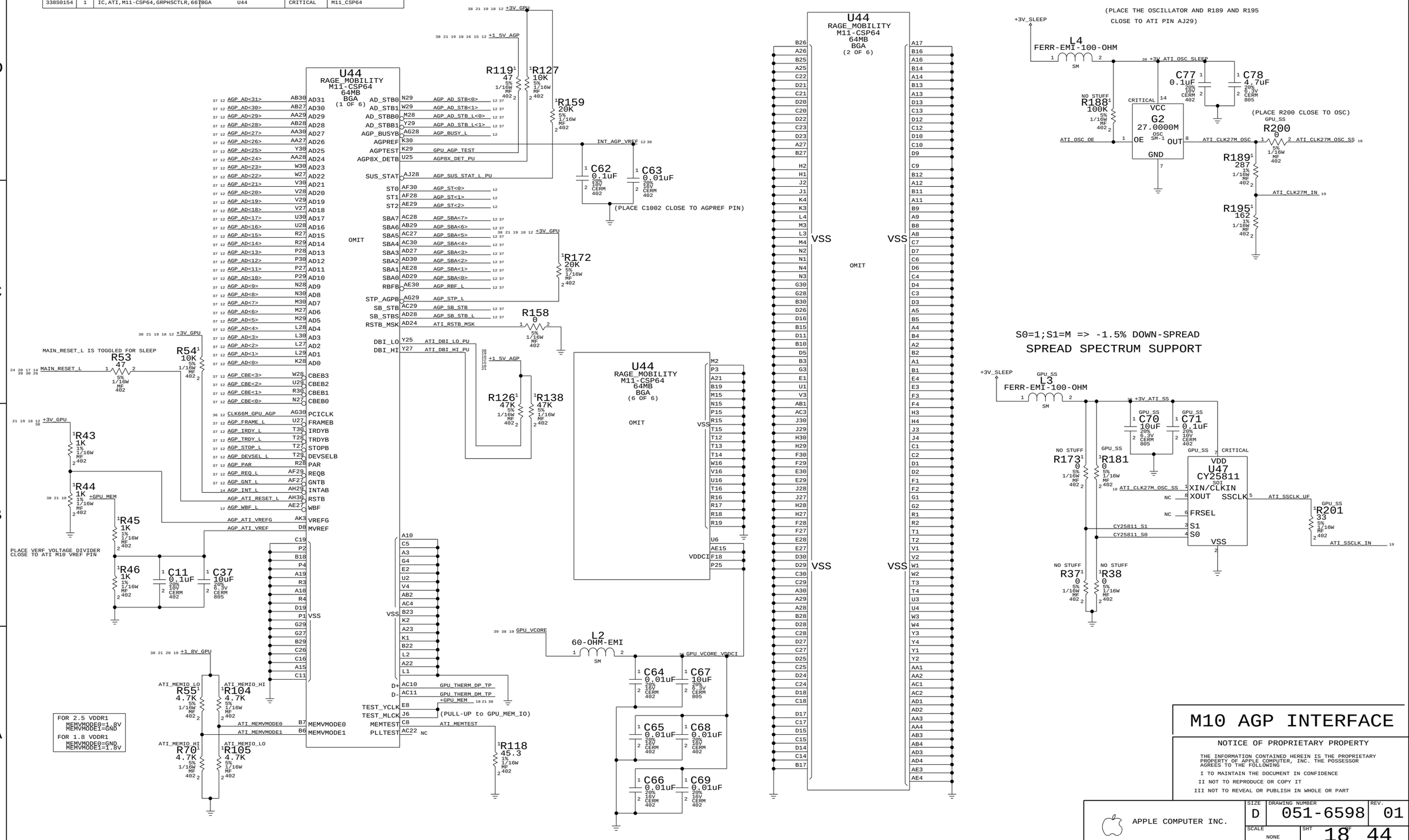
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0158	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA	U44	CRITICAL	M11_CSP128
338S0154	1	IC,ATI,M11-CSP64,GRPHSCTLR,667BGA	U44	CRITICAL	M11_CSP64



M10 AGP INTERFACE

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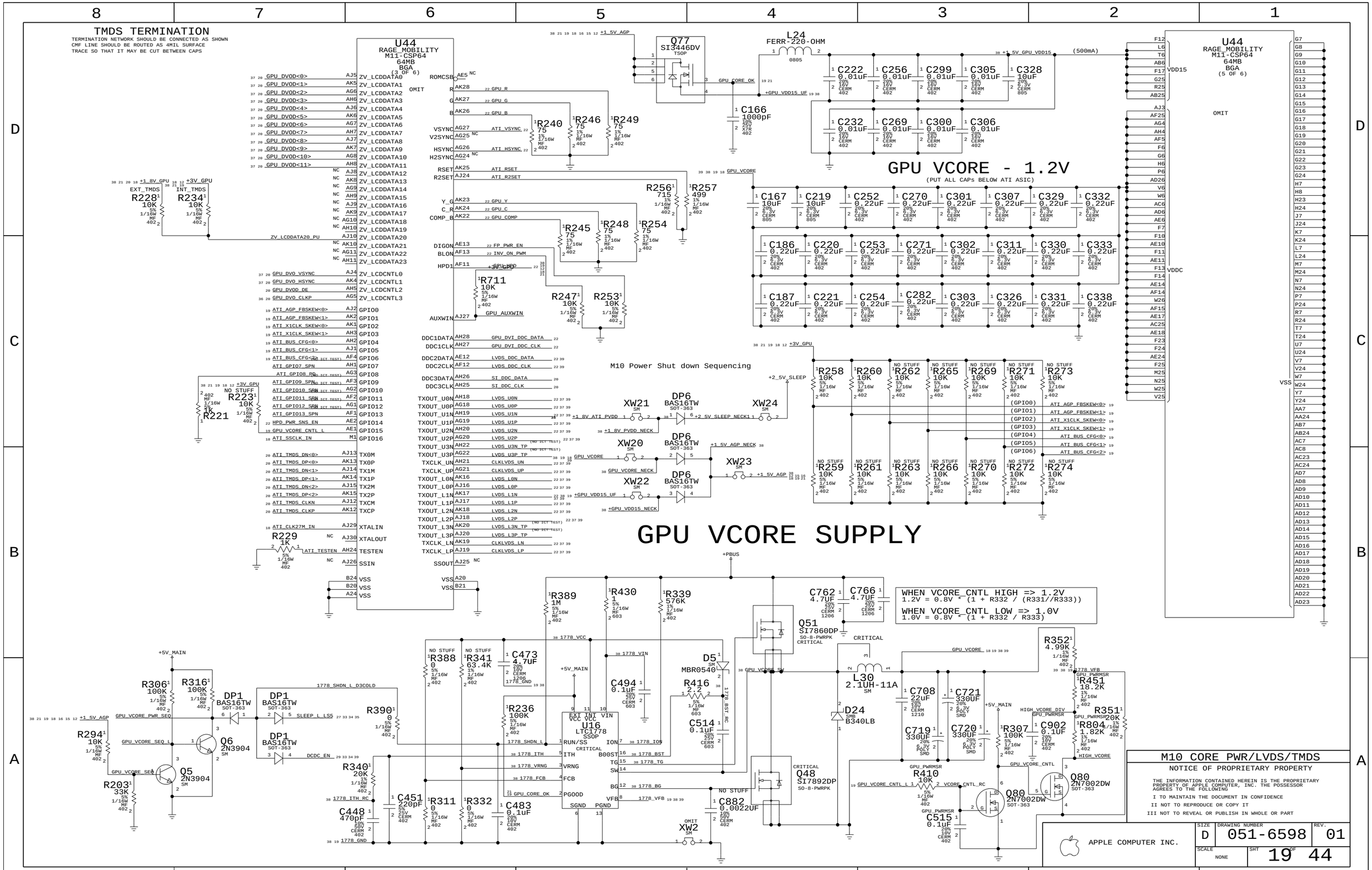
TMDS TERMINATION
TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN
CMF LINE SHOULD BE ROUTED AS 4MIL SURFACE
TRACE SO THAT IT MAY BE CUT BETWEEN CAPS
U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(3 OF 6)
OMIT
Q77
SI3446DV
TSOP
L24
FERR-220-OHM
0805
(500mA)
U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(5 OF 6)
OMIT
GPU VCORE - 1.2V
(PUT ALL CAPs BELOW ATI ASIC)
M10 Power Shut down Sequencing
GPU VCORE SUPPLY
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)
M10 CORE PWR/LVDS/TMDS
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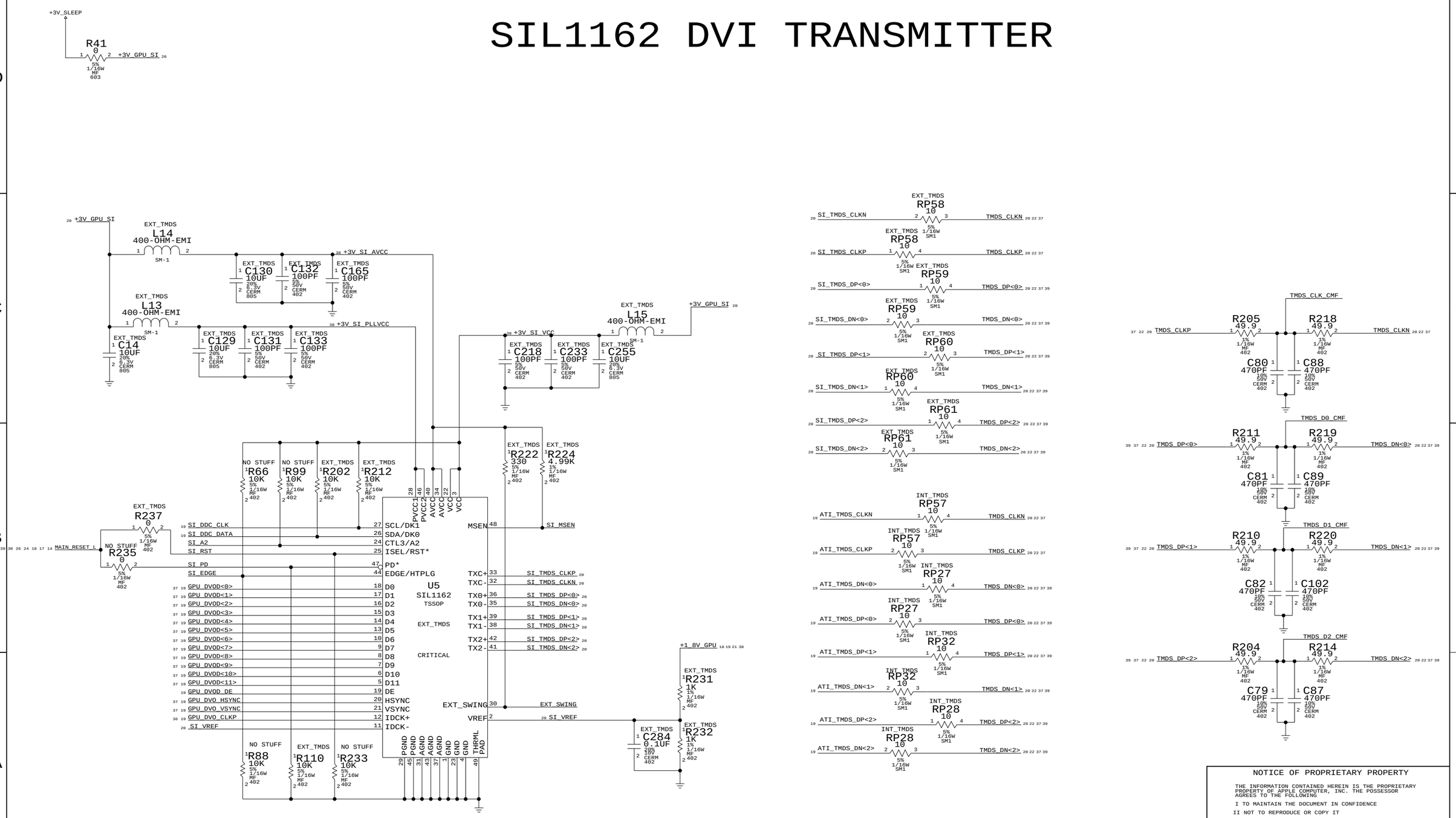
SIL1162 DVI TRANSMITTER



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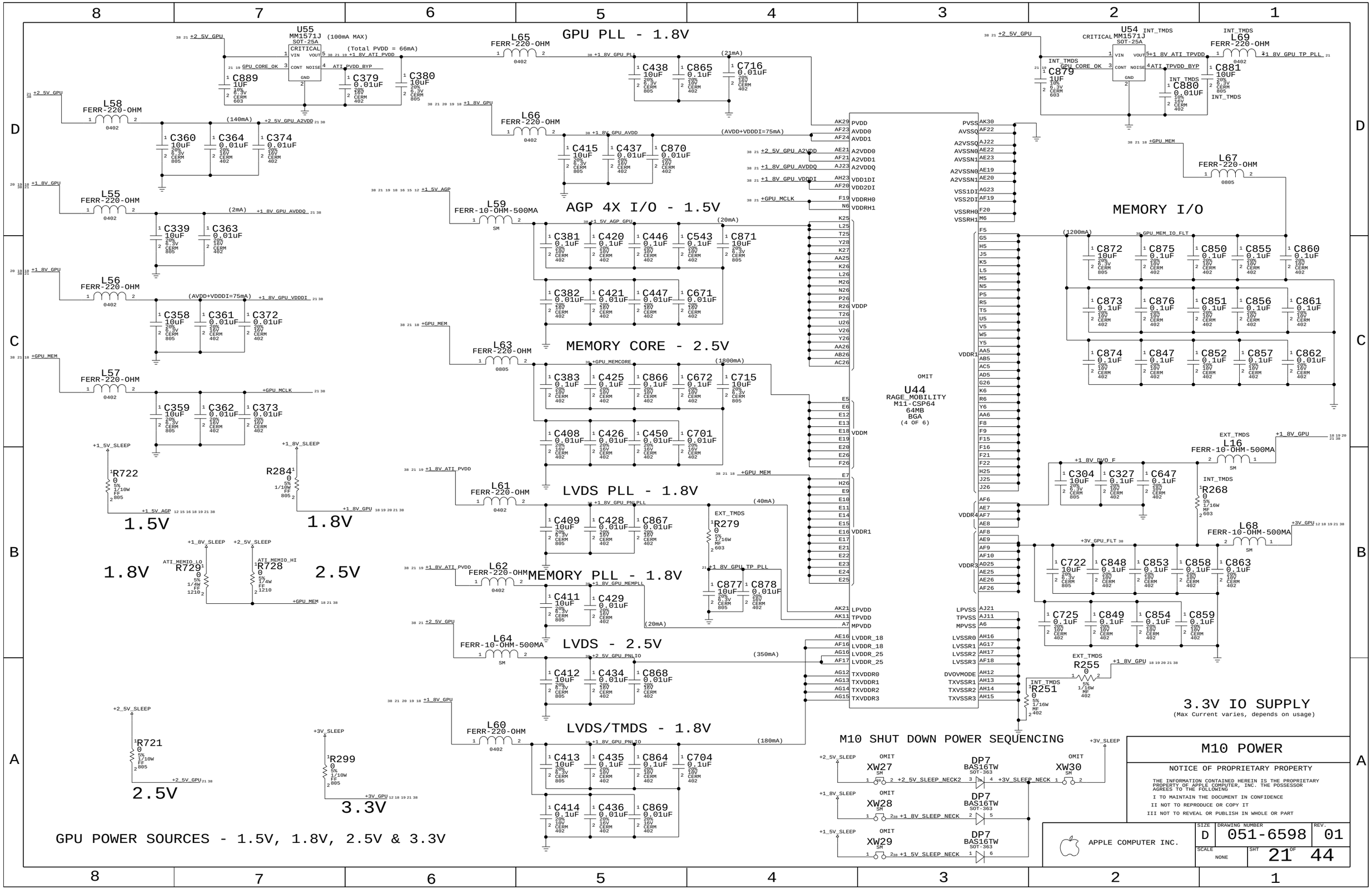
GPU PLL - 1.8V
AGP 4X I/O - 1.5V
MEMORY CORE - 2.5V
LVDS PLL - 1.8V
MEMORY PLL - 1.8V
LVDS - 2.5V
LVDS/TMDS - 1.8V
MEMORY I/O
3.3V IO SUPPLY
(Max Current varies, depends on usage)
M10 SHUT DOWN POWER SEQUENCING
GPU POWER SOURCES - 1.5V, 1.8V, 2.5V & 3.3V
U44
RAGE_MOBILITY
M11-CSP64
64MB
BGA
(4 OF 6)
U55
MM1571J
SOT-25A
U54
MM1571J
SOT-25A
M10 POWER
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EXTERNAL VIDEO (DVI) INTERFACE

ANALOG FILTERING PLACE CLOSE TO CONNECTOR

FL2 LCFILTER SM-220MHZ CRITICAL — GPU_B → VGA_B
FL1 LCFILTER SM-220MHZ CRITICAL — GPU_G → VGA_G
FL3 LCFILTER SM-220MHZ CRITICAL — GPU_R → VGA_R
C685 3.3PF 0.25% 50V CERM 402
C676 3.3PF 0.25% 50V CERM 402
C684 3.3PF 0.25% 50V CERM 402

VGA VSYNC BUFFERS

+3V_MAIN
ATI_HSYNC → U56 74AHC1G32 SM CRITICAL → VGA_HSYNC_BUF → R718 33 5% 1/16W MF 402 → VGA_HSYNC
ATI_VSYNC → U57 74AHC1G32 SM CRITICAL → VGA_VSYNC_BUF → R714 33 5% 1/16W MF 402 → VGA_VSYNC

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

+5V_SLEEP → F1 0.5AMP-13.2V SM → +5V_DDC_SLEEP_UF → L23 400-OHM-EMI SM-1 → +5V_DDC_SLEEP

Isolation required for DVI power switch

D21 SM MBR0530 — DDC_CLK_ISO

J14 QH1112 F-RT-TH CRITICAL

TMDS_CONN_DN<0> → TMDS_CONN_DN<2>
TMDS_CONN_DP<0> → TMDS_CONN_DP<2>
TMDS_CONN_DN<1> → TMDS_CONN_DN<3>
TMDS_CONN_DP<1> → TMDS_CONN_DP<3>
(TMDS_DN<5>) → (TMDS_DN<4>)
(TMDS_DP<5>) → (TMDS_DP<4>)
DVI_DDC_CLK_UF
(+5V_DDC_SLEEP)
TMDS_CONN_CLKP
TMDS_CONN_CLKN
DVI_DDC_DATA_UF
VGA_VSYNC
DVI_HPD_UF
VGA_B → VGA_R
VGA_HSYNC → VGA_G

R661 4.7K 5% 1/16W MF 402
R655 4.7K 5% 1/16W MF 402
R670 100 5% 1/16W MF 402
R649 100 5% 1/16W MF 402
R650 100 5% 1/16W MF 402
C706 100pF 5% 50V CERM 402
C669 100pF 5% 50V CERM 402
C710 0.01UF 20% 50V CERM 603
C1 100pF 5% 50V CERM 402
R706 0 5% 1/16W MF 402 — PLACE NEAR 3, 11 & 19
R1 0 5% 1/16W MF 402 — PLACE NEAR C5A & C5B
CHGND5, CHGND1

3V LEVEL SHIFTERS

+3V_SLEEP
Q38 2N7002DW SOT-363 — DVI_DDC_CLK → GPU_DVI_DDC_CLK
Q38 2N7002DW SOT-363 — DVI_DDC_DATA → GPU_DVI_DDC_DATA
Q35 2N7002DW SOT-363 — DVI_HPD → GPU_HPD
R662 10K 5% 1/16W MF 402
R671 10K 5% 1/16W MF 402
R694 100K 5% 1/16W MF 402

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TP0610 will turn on, driving SOFT_PWR_ON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC CLK. Isolation will be disabled as well.

Q40 TP0610 SM — DVI_DDC_CLK_UF → DVI_TURN_ON
R690 680 5% 1/16W MF 402 — DVI_TURN_ON → DVI_TURN_ON_ILIM
R691 10K 5% 1/16W MF 402 — DVI_TURN_ON_BASE
Q42 2N3904 SM — SOFT_PWR_ON_L
R688 330 5% 1/16W MF 402 — Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.

+3V_SLEEP
R680 68.1K 1% 1/16W MF 402
C696 0.1UF 20% 10V CERM 402
HPD_4V_REF
U46 LMC7211 SM CRITICAL — HPD_PWR_SW
R663 10K 1% 1/16W MF 402 — DVI_HPD_UF → DVI_HPD_DIV
R686 10K 1% 1/16W MF 402
R681 100K 1% 1/16W MF 402
Q41 2N7002DW SOT-363 — HPD_ON
R703 330 5% 1/16W MF 402
+PBUS
Q45 TP0610 SM — COMP_ENABLE
R696 100K 5% 1/16W MF 402 — COMP_DISABLE
R704 100K 5% 1/16W MF 402
HPD_ON_RC
R700 20K 5% 1/16W MF 402 — HPD_BASE
Q44 2N3904 SM
C703 47UF 20% 6.3V CERM 1210
R705 68K 5% 1/16W MF 402
Q41 2N7002DW SOT-363 — NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
HPD_PWR_SNS_EN → R213 100K 5% 1/16W MF 402

LCD INTERFACE

LVDS INTERFACE

100K pull-ups are for no-panel case (development) Panel has 2K pull-ups

+3V_SLEEP
R342 100K 5% 1/16W MF 402
R320 100K 5% 1/16W MF 402
C416 0.001UF 20% 50V CERM 402 — CHGND4
J6 G-501973 F-RT-SM CRITICAL
+3V_LCD — (LVDS DDC POWER) — NC
LVDS_DDC_CLK
LVDS_DDC_DATA
NO STUFF
C449 0.001UF 20% 50V CERM 402
C452 0.001UF 20% 50V CERM 402
LVDS_L0N, LVDS_L0P, LVDS_L1N, LVDS_L1P, LVDS_L2N, LVDS_L2P, CLKLVDS_LN, CLKLVDS_LP, LVDS_U0N, LVDS_U0P, LVDS_U1N, LVDS_U1P, LVDS_U2N, LVDS_U2P, CLKLVDS_UN, CLKLVDS_UP
C500 0.001uF 20% 50V CERM 402 — CHGND4

INVERTER INTERFACE

+PBUS
L33 FERR-1K-OHM-EMI SM — +12_8V_INV
+5V_MAIN
Q7 FDG6324L SC70-6 — +5V_INV_UF_SW
R317 100K 5% 1/16W MF 402 — FP_PWR_EN_L
L32 400-OHM-EMI SM-1
C440 10UF 20% 6.3V CERM 805
Q7 FDG6324L SC70-6 — FP_PWR_EN
+5V_INV_SW
C746 0.001UF 20% 50V CERM 402
J7 SM-2MT CRITICAL
C749 0.001UF 20% 50V CERM 402
L31 400-OHM-EMI SM-1 — BRIGHT_PWM
C739 0.001UF 20% 50V CERM 402
CHGND2
+3V_PMU
C552 0.1UF 20% 10V CERM 402
INV_ON_PWM → U24 74LVC32 TSSOP → BRIGHT_PWM_UF
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
R724 0 5% 1/16W MF 402
C744 0.01uF 20% 50V CERM 603 — CHGND2

TMDS FILTERING PLACE CLOSE TO CONNECTOR

L72 90-OHM-300MA 2012H CRITICAL — TMDS_DN<0> → TMDS_CONN_DN<0>
L73 90-OHM-300MA 2012H CRITICAL — TMDS_DP<0> → TMDS_CONN_DP<0>
L21 165-OHM SM CRITICAL — TMDS_CLKP → TMDS_CONN_CLKP
L74 90-OHM-300MA 2012H CRITICAL — TMDS_CLKN → TMDS_CONN_CLKN
L73 90-OHM-300MA 2012H CRITICAL — TMDS_DN<1> → TMDS_CONN_DN<1>
L74 90-OHM-300MA 2012H CRITICAL — TMDS_DN<2> → TMDS_CONN_DN<2>
TMDS_DP<1> → TMDS_CONN_DP<1>
TMDS_DP<2> → TMDS_CONN_DP<2>

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW12 SM — GPU_TV_GND1 → TV_GND1
L26 FERR-10-OHM-500MA SM
C712 0.01UF 20% 50V CERM 603
L25 3.3UH 0603 — GPU_Y
C702 560PF 10% 50V CERM 402
C707 560PF 10% 50V CERM 402
J15 MINIDIN RT-TH MH1177 CRITICAL — TV_C, TV_Y, TV_COMP
L29 3.3UH 0603 — GPU_C
C718 560PF 10% 50V CERM 402
C724 560PF 10% 50V CERM 402
L27 3.3UH 0603 — GPU_COMP
C714 560PF 10% 50V CERM 402
C713 560PF 10% 50V CERM 402
XW13 SM — GPU_TV_GND2
L28 FERR-10-OHM-500MA SM — TV_GND2
C717 0.01UF 20% 50V CERM 603
CHGND1

Place GND shorts at graphics controller

LCD POWER SWITCHES

+3V_MAIN
R400 100K 5% 1/16W MF 402
C484 2200pF 5% 50V CERM 603 — LCD_PWREN_L
R391 100K 5% 1/16W MF 402 — LCD_DIGON_L
Q11 SI3443DV TSOP
+3V_LCD_SW
L6 FERR-250-OHM SM
C474 0.001uF 20% 50V CERM 402 — CHGND4
Q8 2N7002 SM — FP_PWR_EN

VIDEO CONNECTORS

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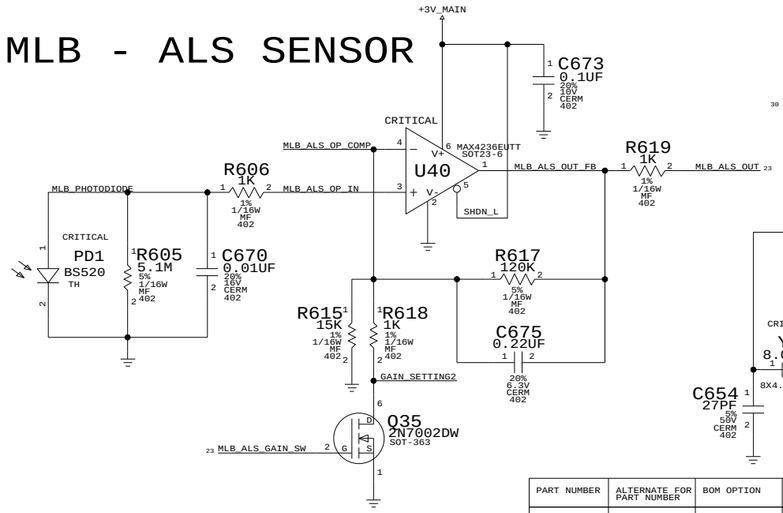
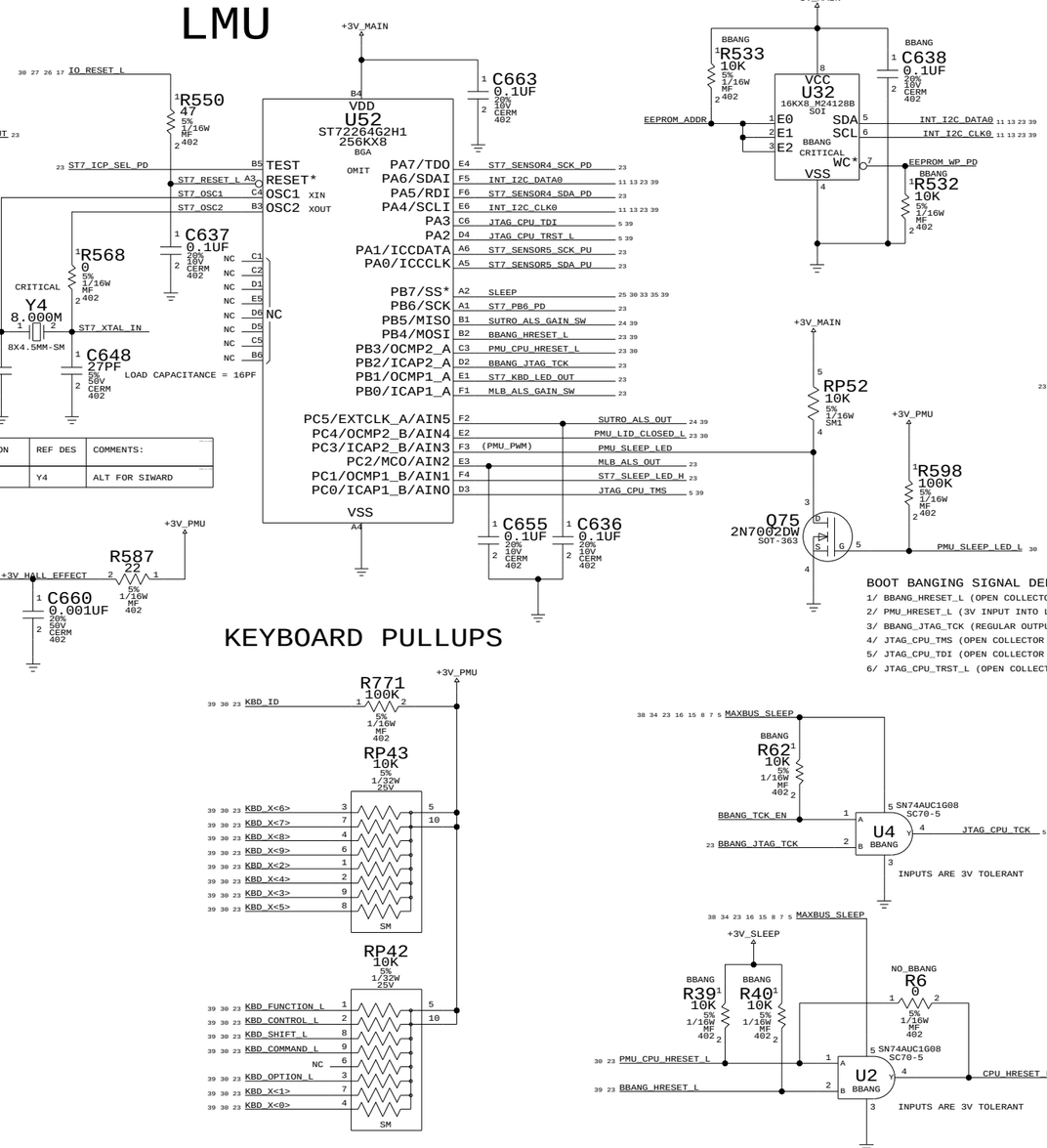
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

MLB - ALS SENSOR



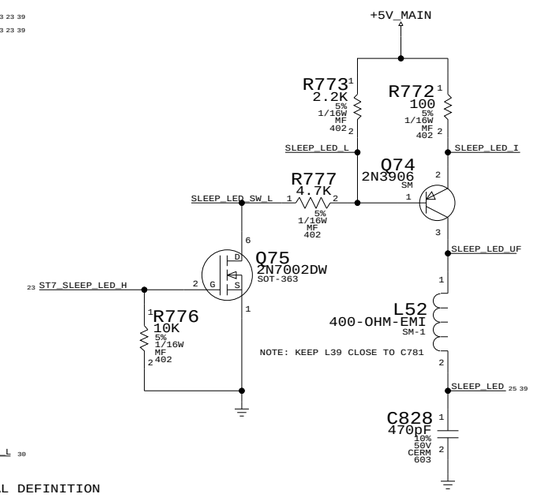
LMU



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0008	197S0040		Y4	ALT FOR SIWARD

BOOT BANGER E2PROM

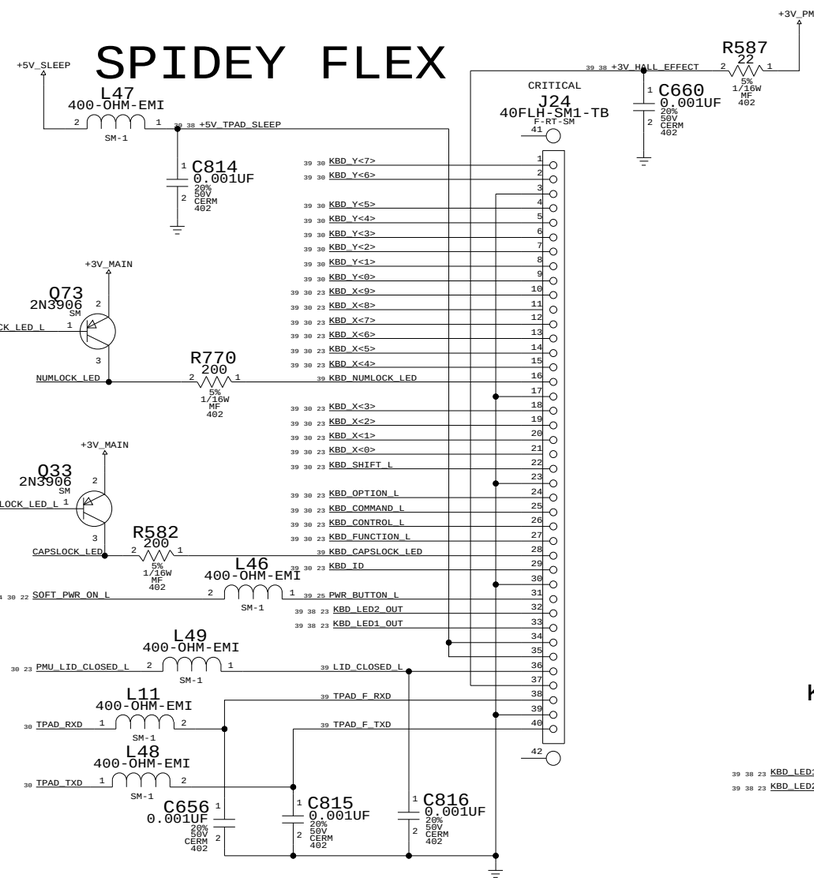
SLEEP LED



BOOT BANGING SIGNAL DEFINITION

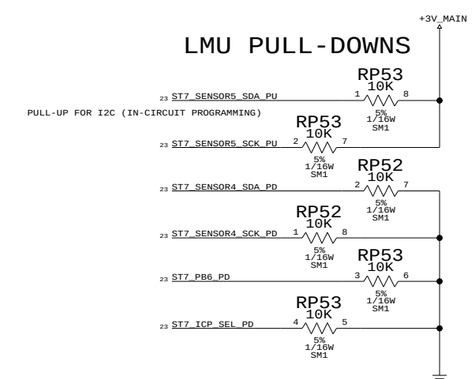
1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

SPIDEY FLEX

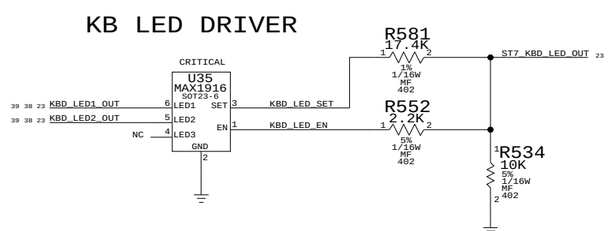


KEYBOARD PULLUPS

LMU PULL-DOWNS



KB LED DRIVER



LMU/BOOTBANGER/SPIDEY

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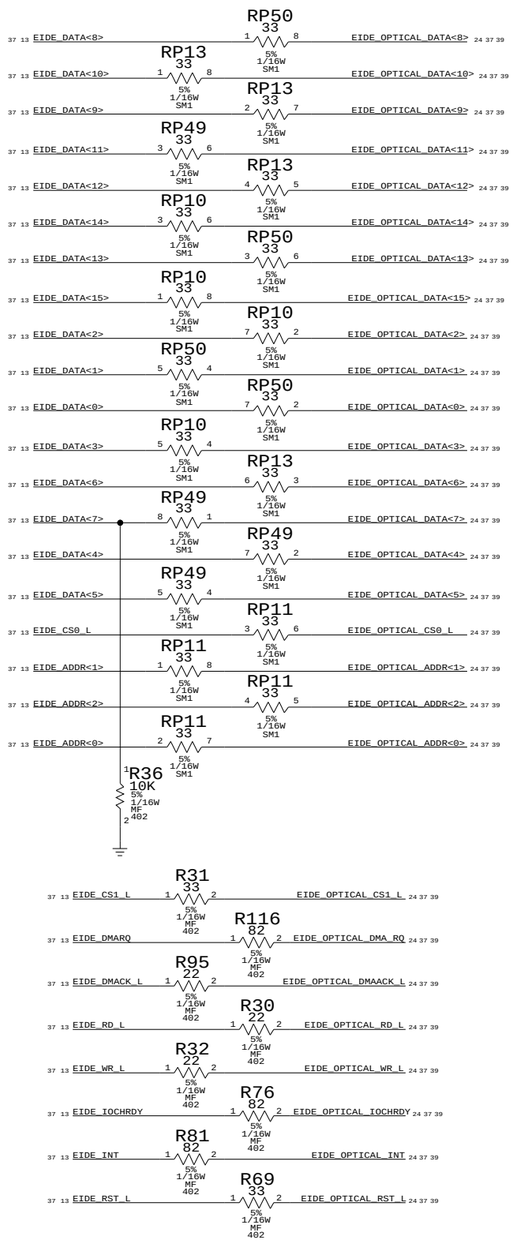
SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE NONE	SHT 23 OF 44	

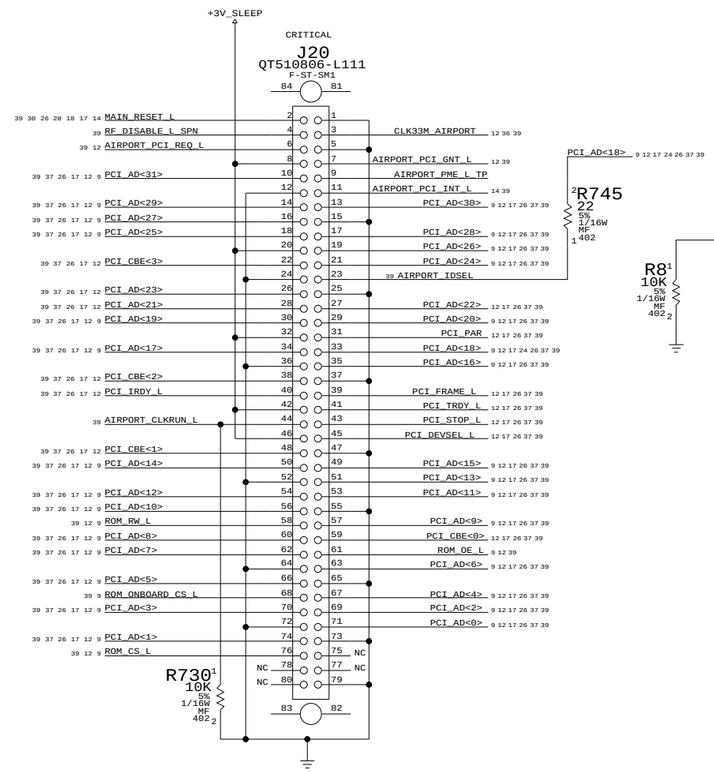
HARD DRIVE INTERFACE (UATA100)

EIDE SERIES TERMINATION

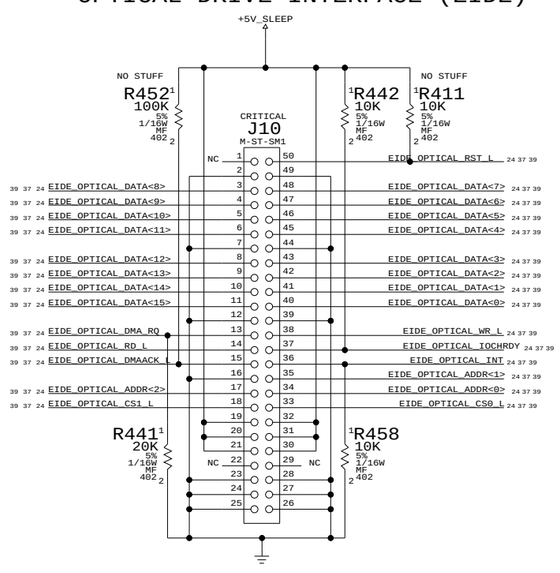
PLACE TERMINATORS NEAR INTREPID



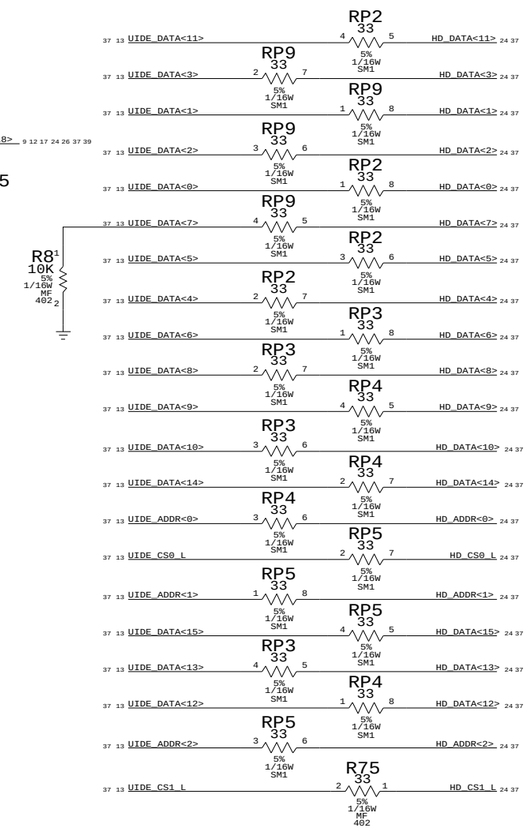
WIRELESS INTERFACE



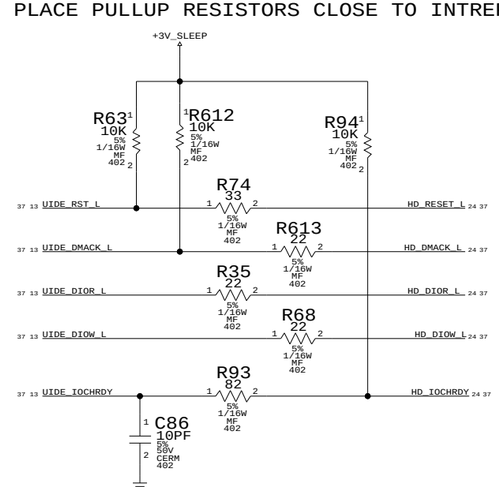
OPTICAL DRIVE INTERFACE (EIDE)



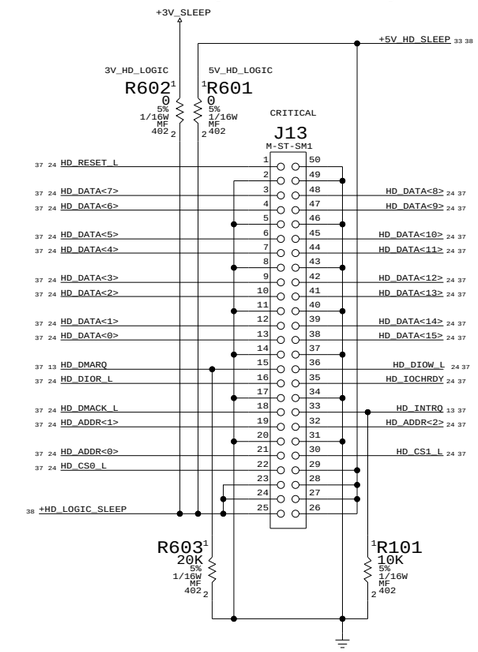
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

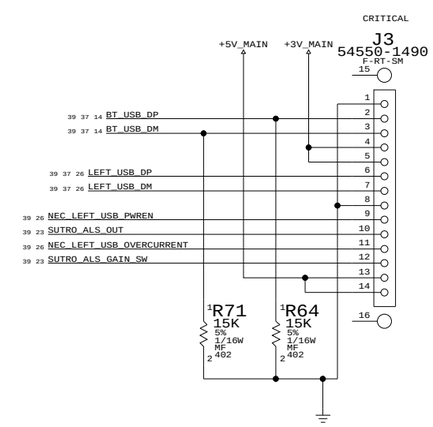


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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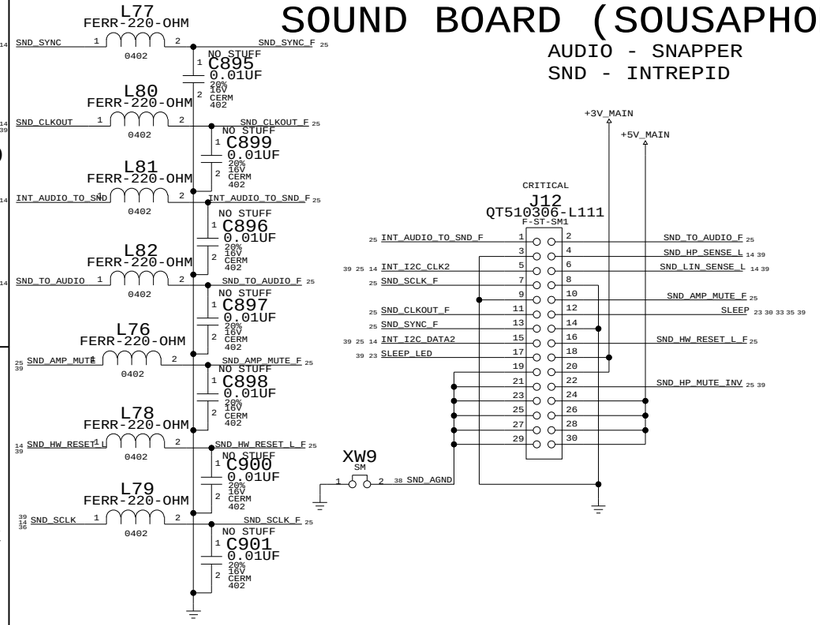
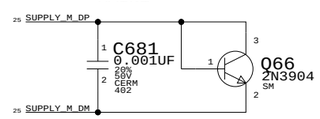
SOUND BOARD (SOUSAPHONE)

AUDIO - SNAPPER
SND - INTREPID

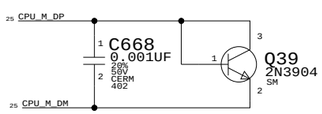


PLACE XW9 CLOSE TO 5V SWITCHER (U27)
PLACE CAPS AS CLOSE TO THERMISTORS AS POSSIBLE
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY

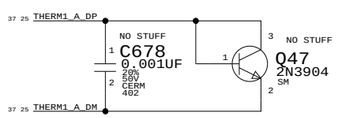
MAIN1



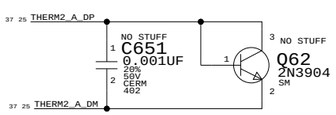
PLACE CLOSE TO CPU
MAIN2



PLACE UNDERNEATH UPPER RAM
ALTERNATE1



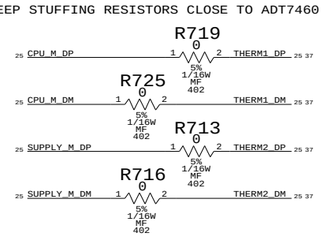
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2



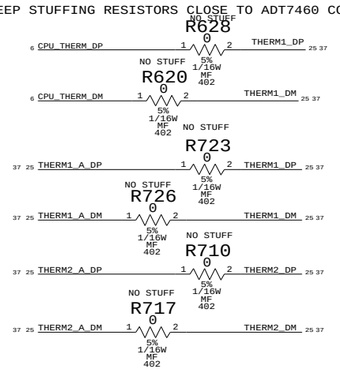
CAPS FOR EMI EXPERIMENTATION ONLY

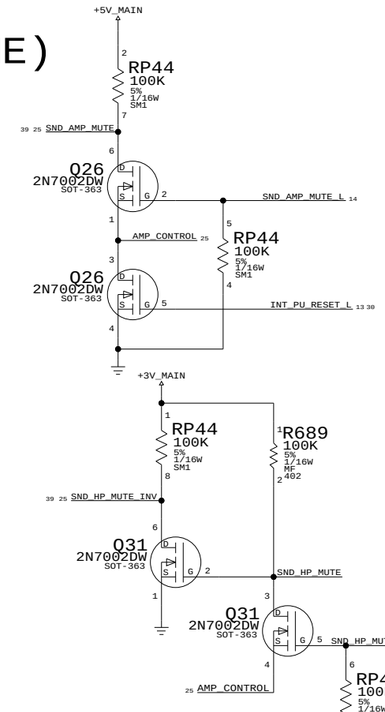
FAN INTERFACE

KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER

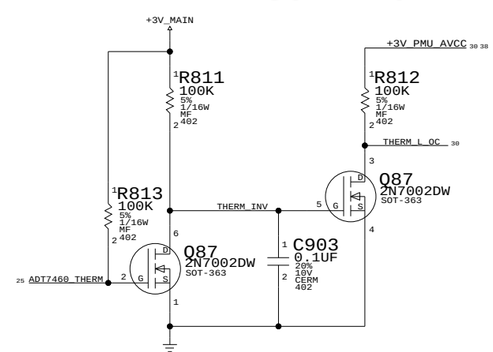


KEEP STUFFING RESISTORS CLOSE TO ADT7460 CONTROLLER



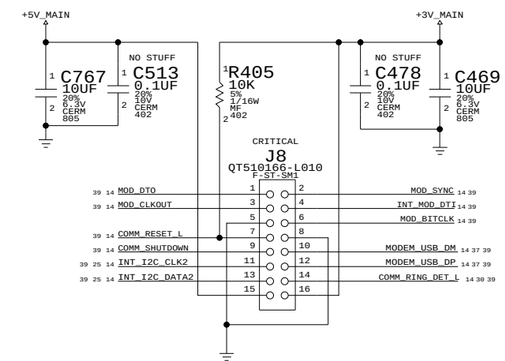


THERM ISOLATION

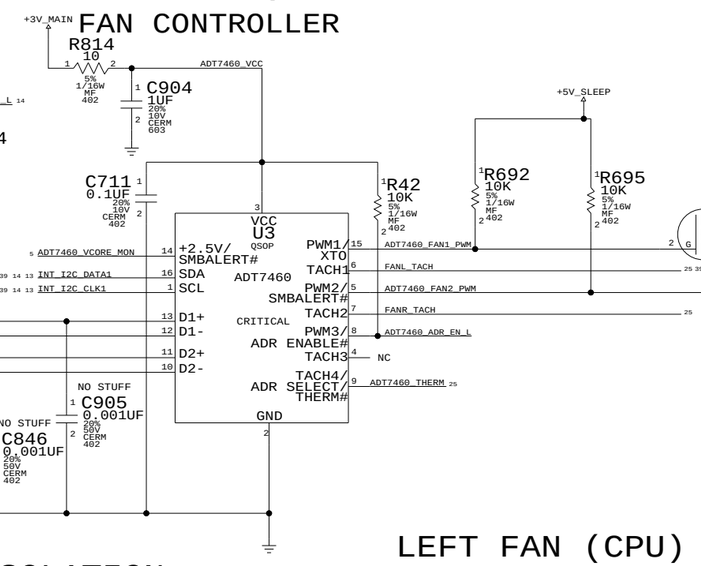


MODEM

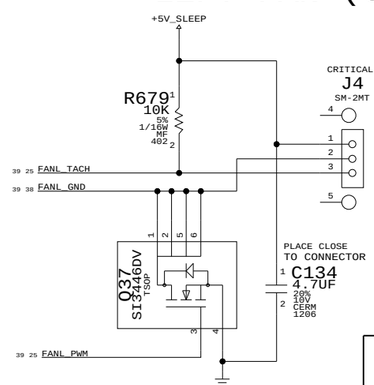
SUPPORTS BOTH THE LAST DASH AND Q52 SOFT MODEM



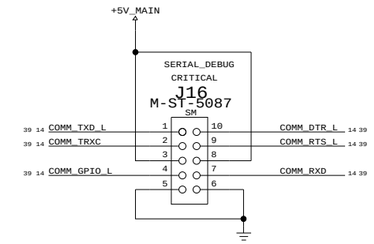
FAN CONTROLLER



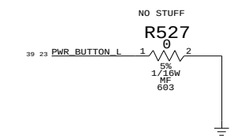
LEFT FAN (CPU)



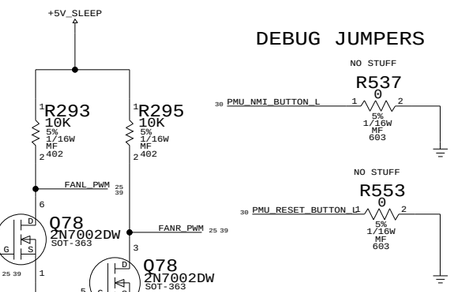
SERIAL DEBUG INTERFACE



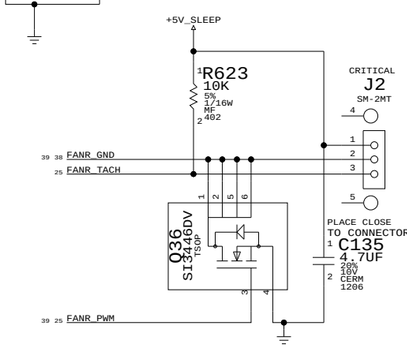
DEBUG POWER BUTTON



DEBUG JUMPERS



RIGHT FAN (GPU)



FAN/MODEM/SOUND/SLEEP LED/DEBUG

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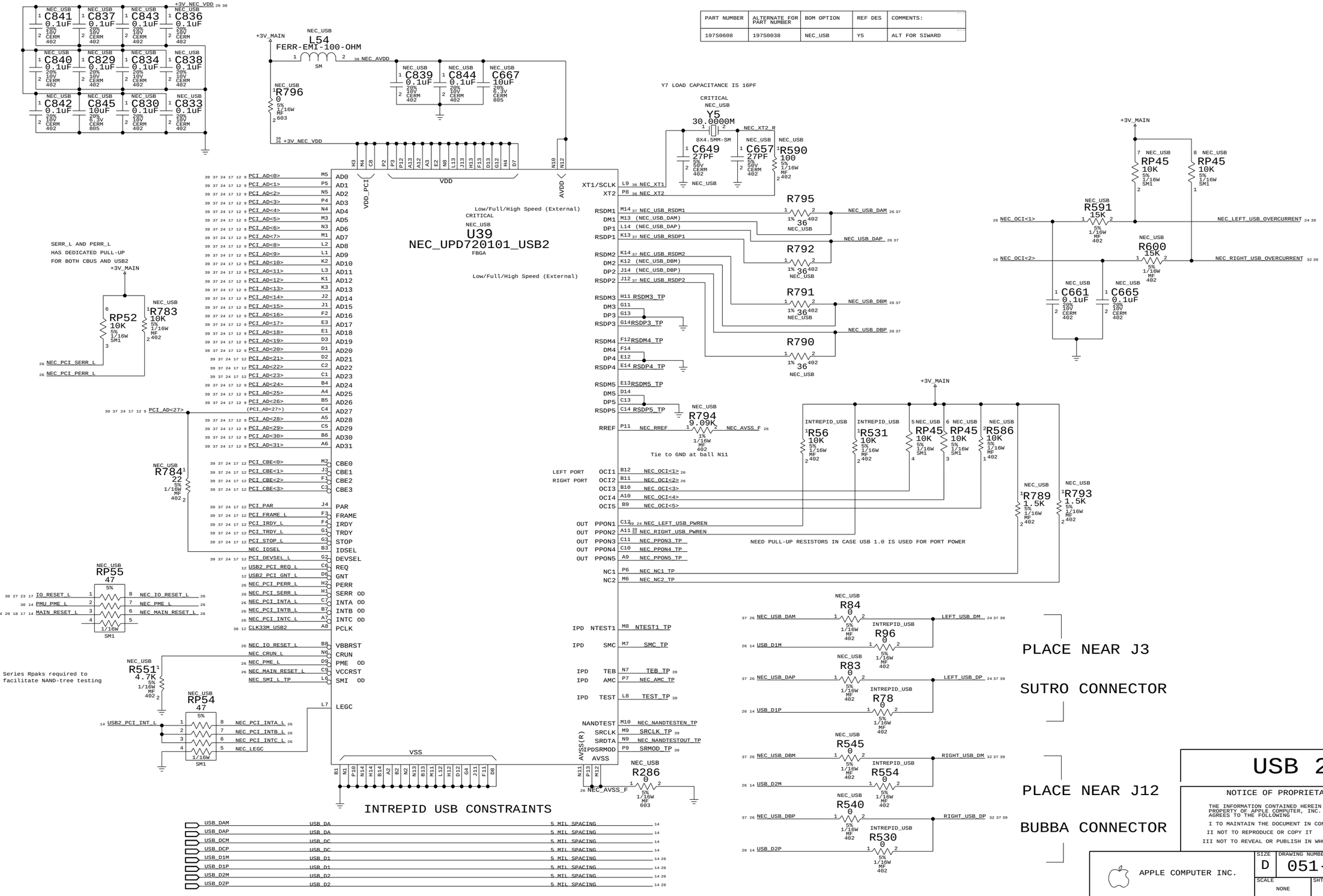
SCALE NONE	SHT 25 OF 44	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0608	197S0038	NEC_USB	Y5	ALT FOR SIWARD



USB 2.0

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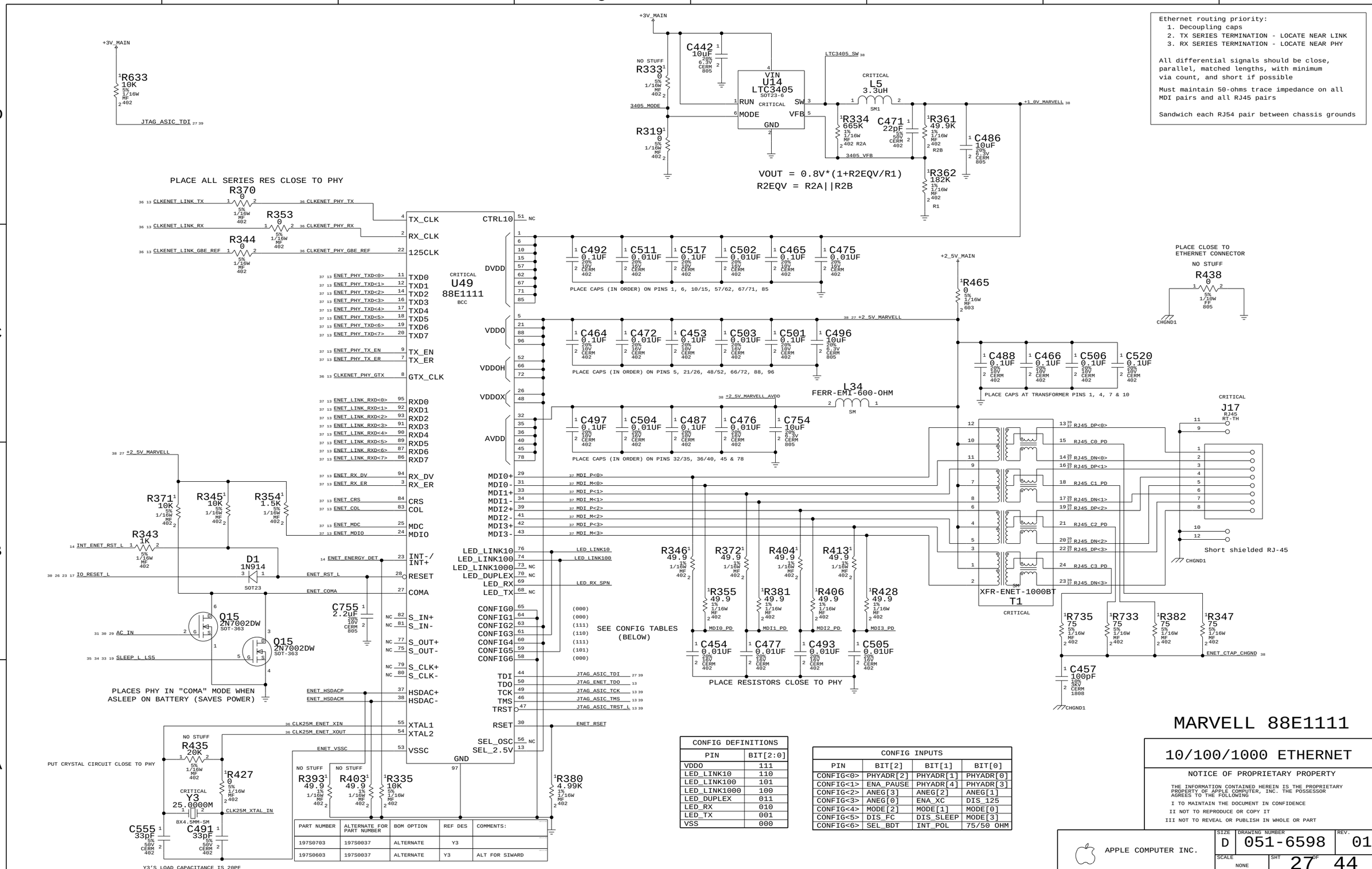
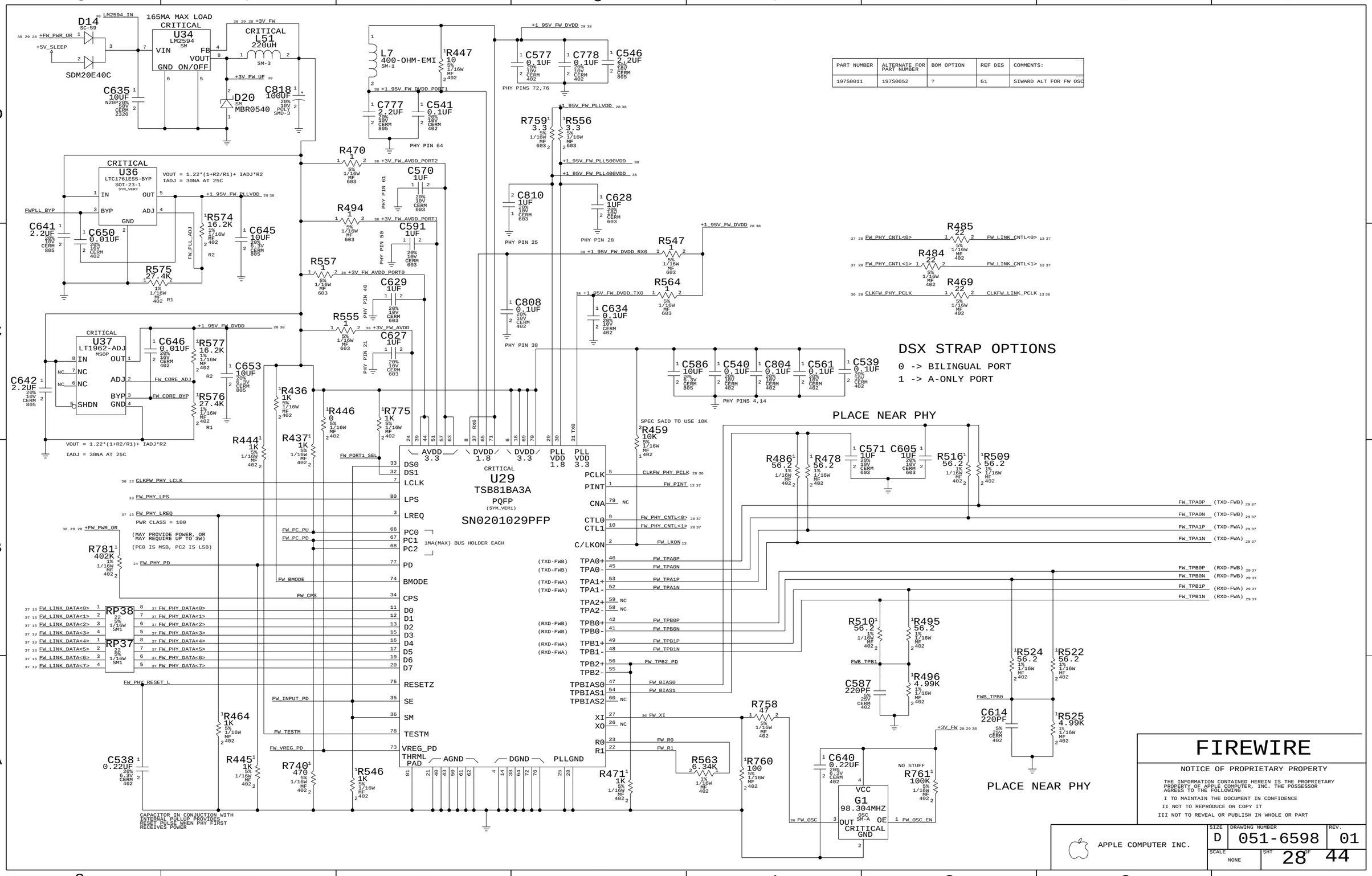


CONFIG DEFINITIONS	
PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS			
PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0703	197S0037	ALTERNATE	Y3	
197S0603	197S0037	ALTERNATE	Y3	ALT FOR SIWARD



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

FIREWIRE

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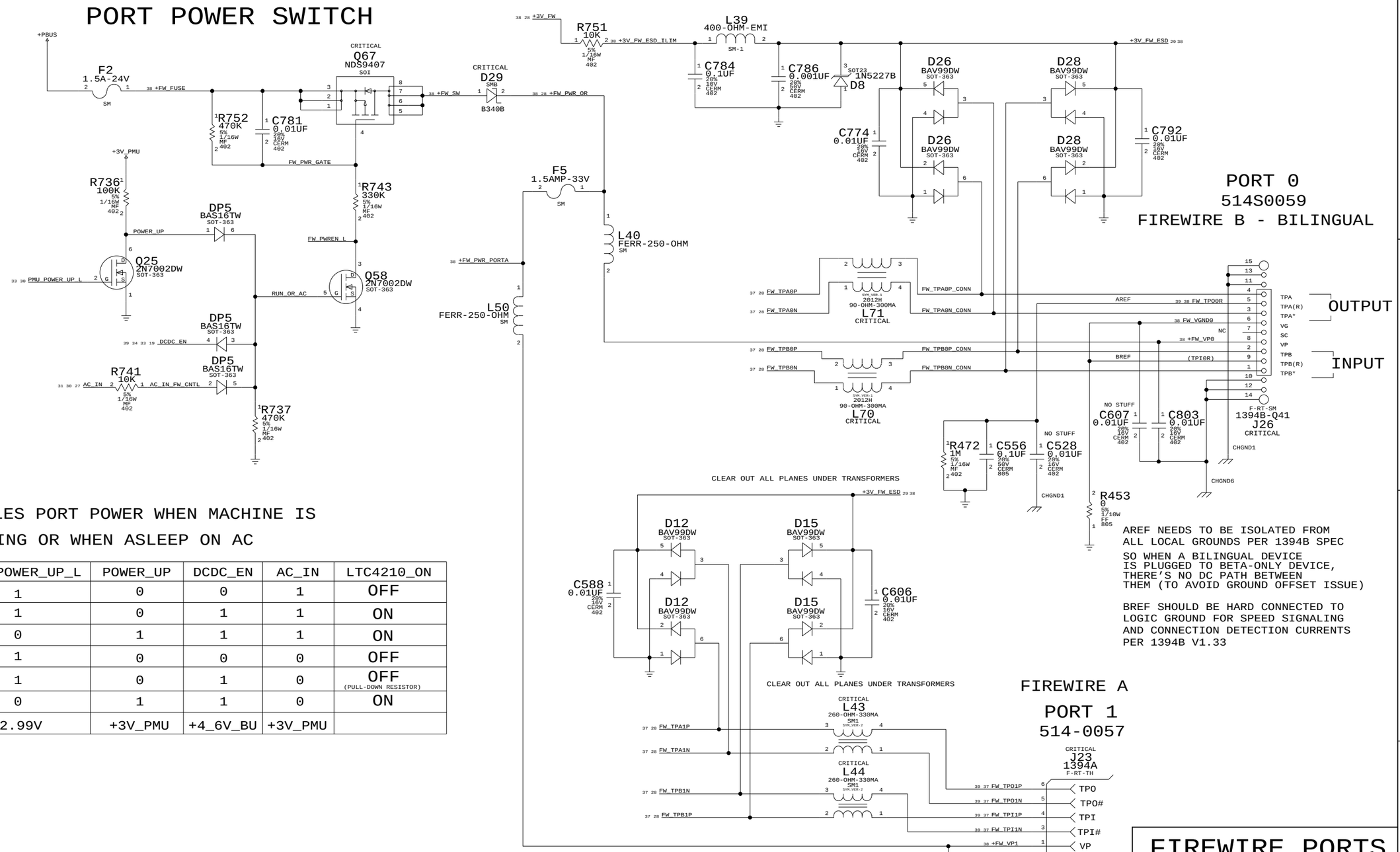
SCALE NONE	SHT 28 OF 44	

PORT POWER SWITCH



AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC

SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

ENABLES PORT POWER WHEN MACHINE IS RUNNING OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	LTC4210_ON
SHUTDOWN (AC)	1	0	0	1	OFF
SLEEP (AC)	1	0	1	1	ON
RUN (AC)	0	1	1	1	ON
SHUTDOWN (BATT)	1	0	0	0	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU	

FIREWIRE PORTS

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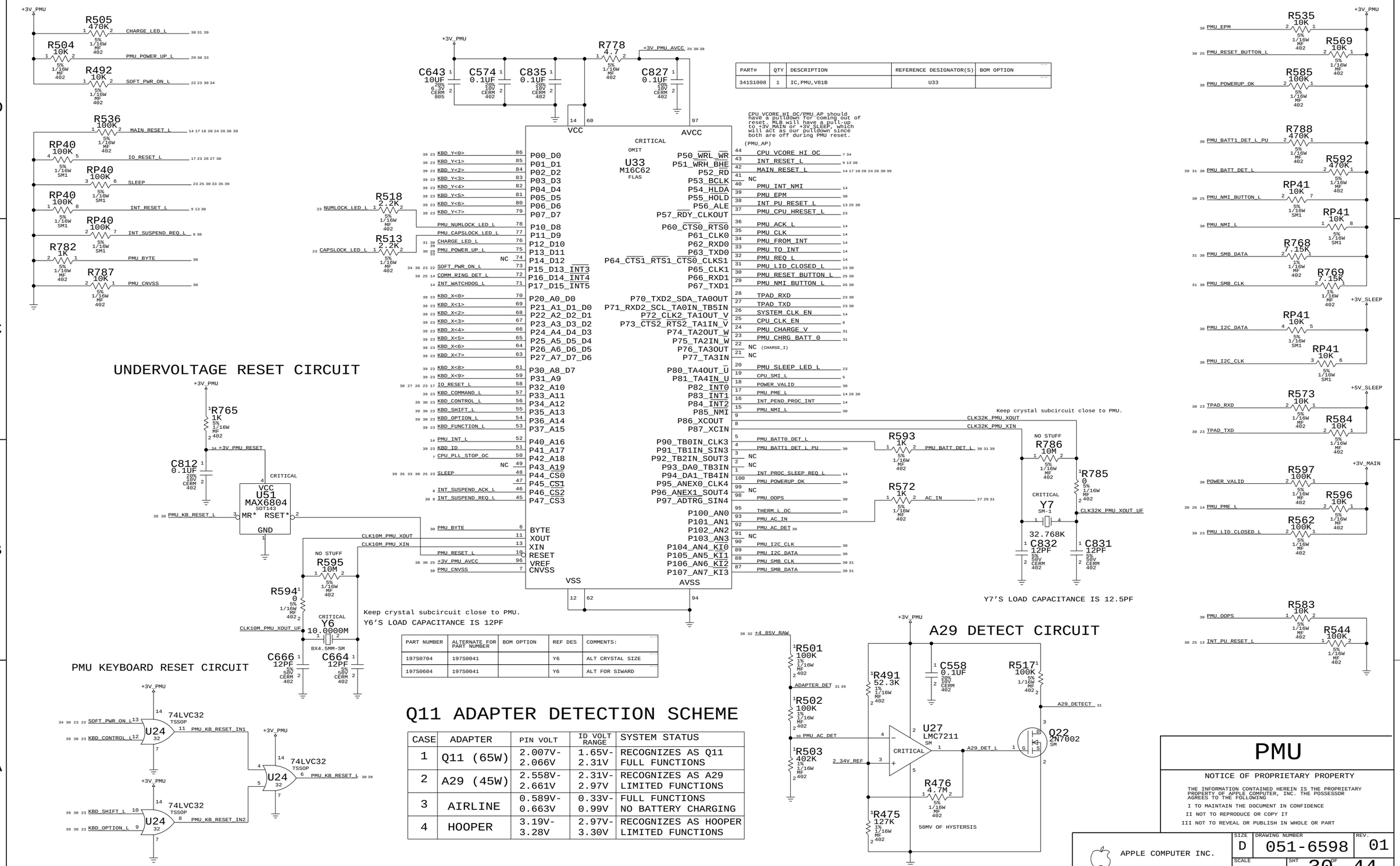

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1008	1	IC,PMU,V81B	U33	

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0704	197S0041		Y6	ALT CRYSTAL SIZE
197S0604	197S0041		Y6	ALT FOR SIWARD

Q11 ADAPTER DETECTION SCHEME

CASE	ADAPTER	PIN VOLT	ID VOLT RANGE	SYSTEM STATUS
1	Q11 (65W)	2.007V- 2.066V	1.65V- 2.31V	RECOGNIZES AS Q11 FULL FUNCTIONS
2	A29 (45W)	2.558V- 2.661V	2.31V- 2.97V	RECOGNIZES AS A29 LIMITED FUNCTIONS
3	AIRLINE	0.589V- 0.663V	0.33V- 0.99V	FULL FUNCTIONS NO BATTERY CHARGING
4	HOOPER	3.19V- 3.28V	2.97V- 3.30V	RECOGNIZES AS HOOPER LIMITED FUNCTIONS

PMU

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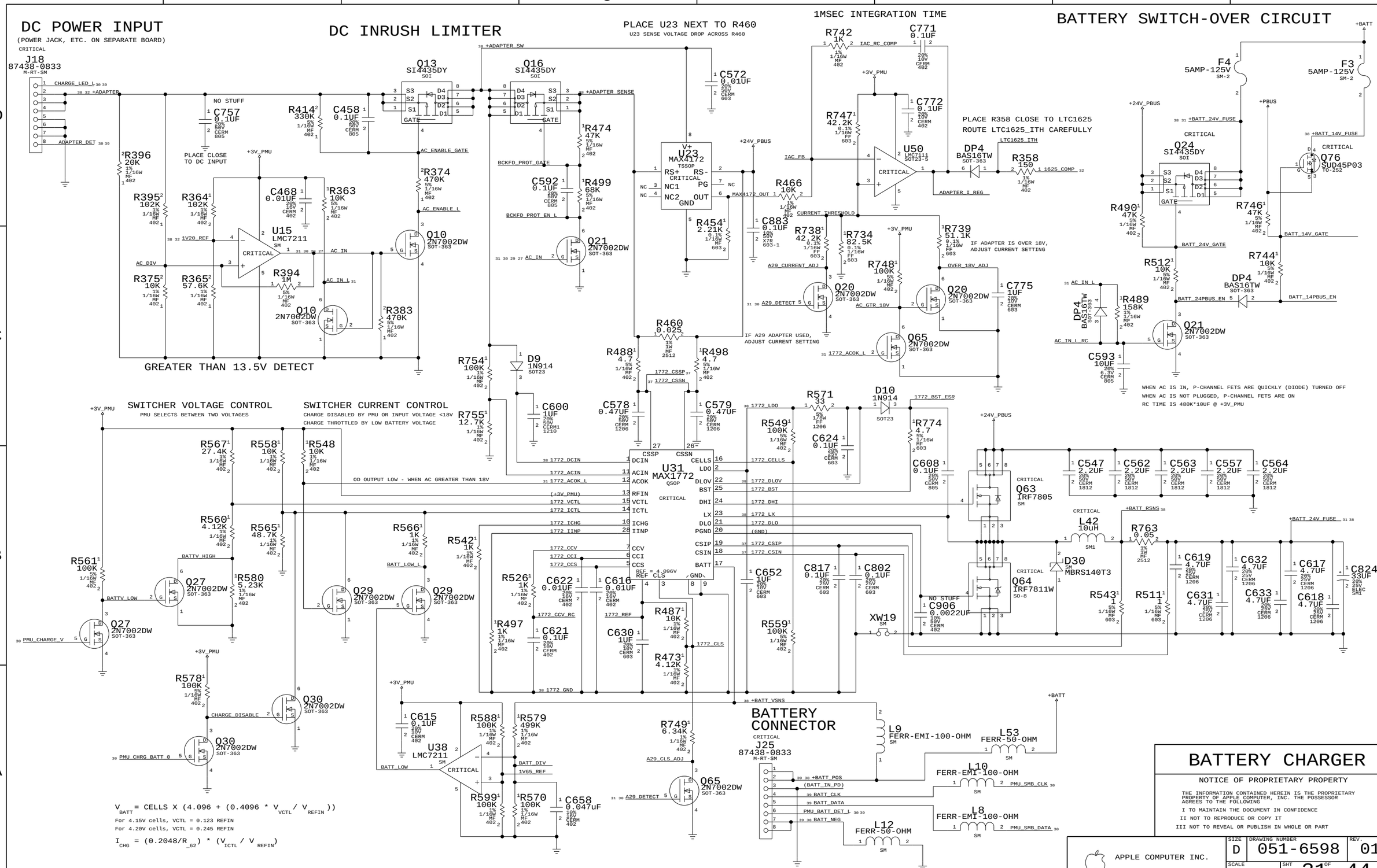
SCALE NONE	SHT 30 OF 44	


DC POWER INPUT
(POWER JACK, ETC. ON SEPARATE BOARD)
DC INRUSH LIMITER
PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460
1MSEC INTEGRATION TIME
BATTERY SWITCH-OVER CIRCUIT
PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
GREATER THAN 13.5V DETECT
SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES
SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
IF A29 ADAPTER USED, ADJUST CURRENT SETTING
IF ADAPTER IS OVER 18V, ADJUST CURRENT SETTING
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU
BATTERY CONNECTOR
J18 87438-0833
J25 87438-0833
U31 MAX1772
U23 MAX4172
U15 LMC7211
U38 LMC7211
U50 LMC7111
Q13 SI4435DY
Q16 SI4435DY
Q24 SI4435DY
Q76 SUD45P03
Q63 IRF7805
Q64 IRF7811W
D9 1N914
D10 1N914
D30 MBRS140T3
F4 5AMP-125V
F3 5AMP-125V
L9 FERR-EMI-100-OHM
L10 FERR-EMI-100-OHM
L8 FERR-EMI-100-OHM
L53 FERR-50-OHM
L12 FERR-50-OHM
L42 10uH
XW19
V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
I_{CHG} = (0.2048/R_{62}) * (V_{ICTL} / V_{REFIN})
BATTERY CHARGER
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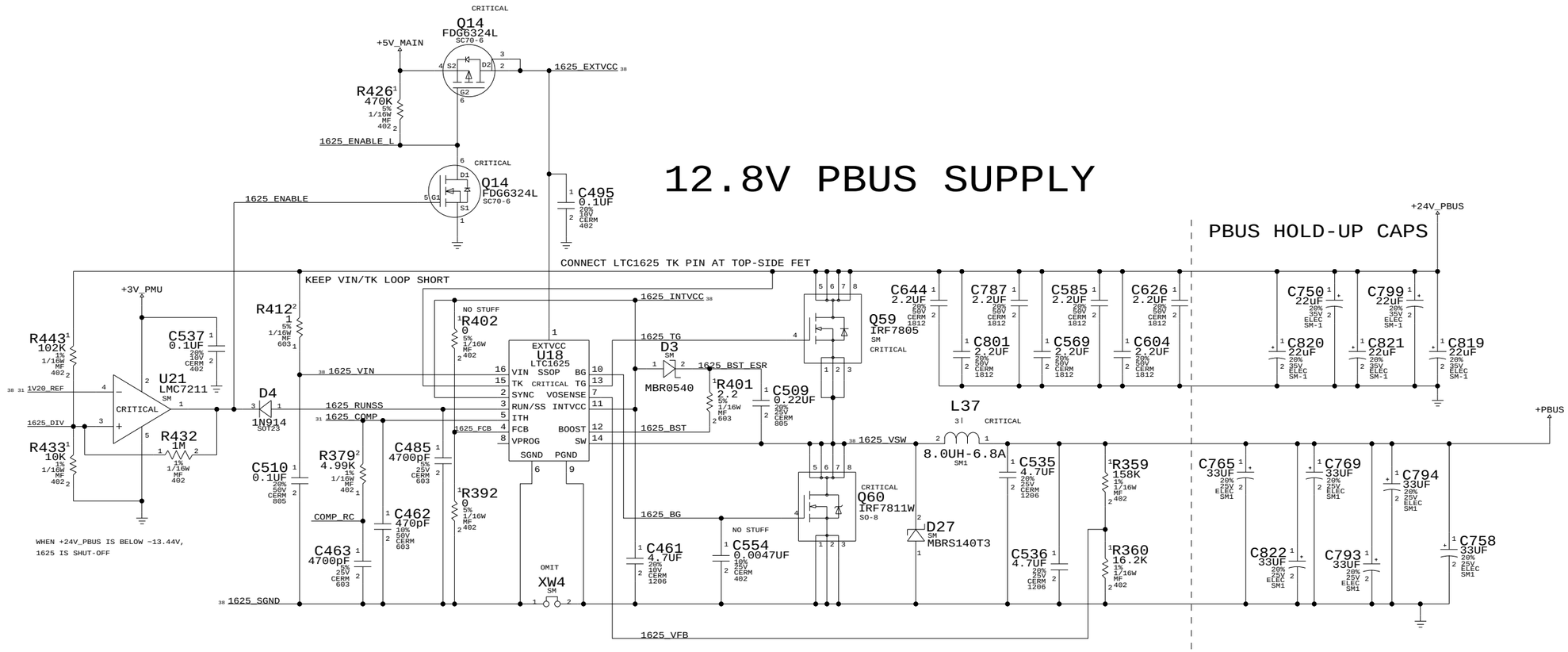
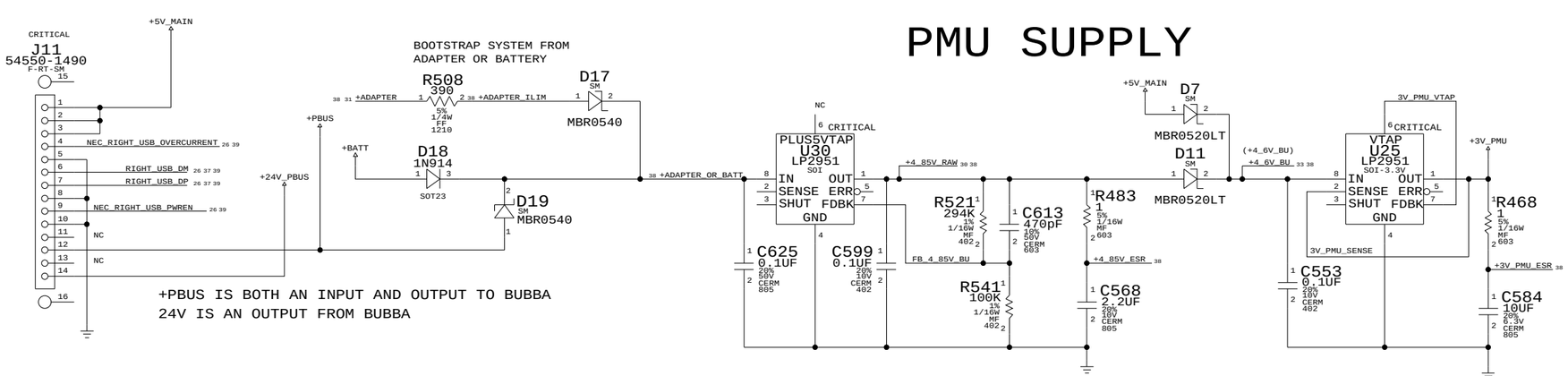
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6598
REV. 01
SCALE NONE
SHT 31 OF 44

12.8V PBUS SUPPLY



BACKUP BATTERY / USB CONNECTOR

PMU SUPPLY



12.8V REGULATOR

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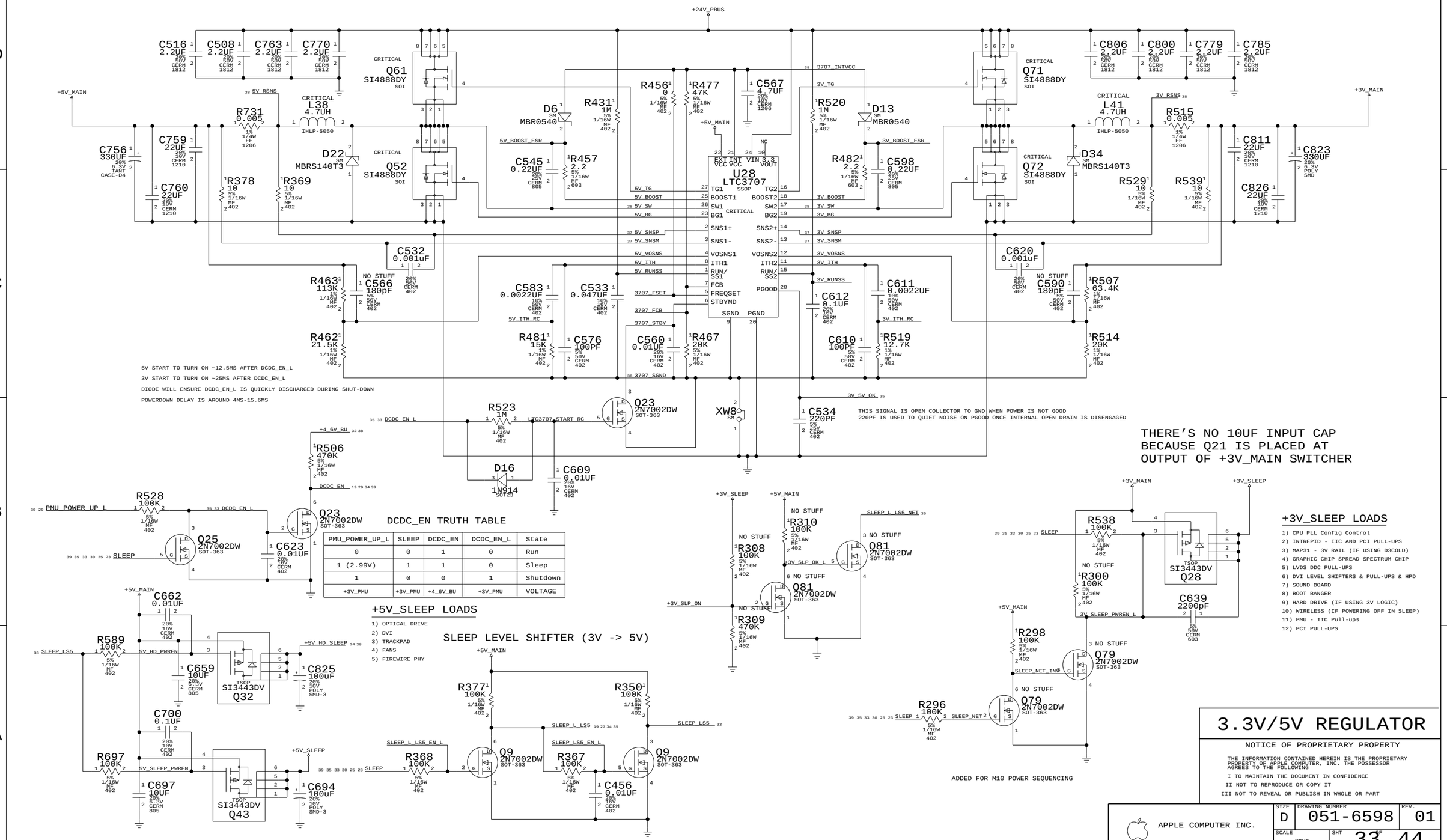
3.3V/5V MAIN SUPPLY



PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

3.3V/5V REGULATOR

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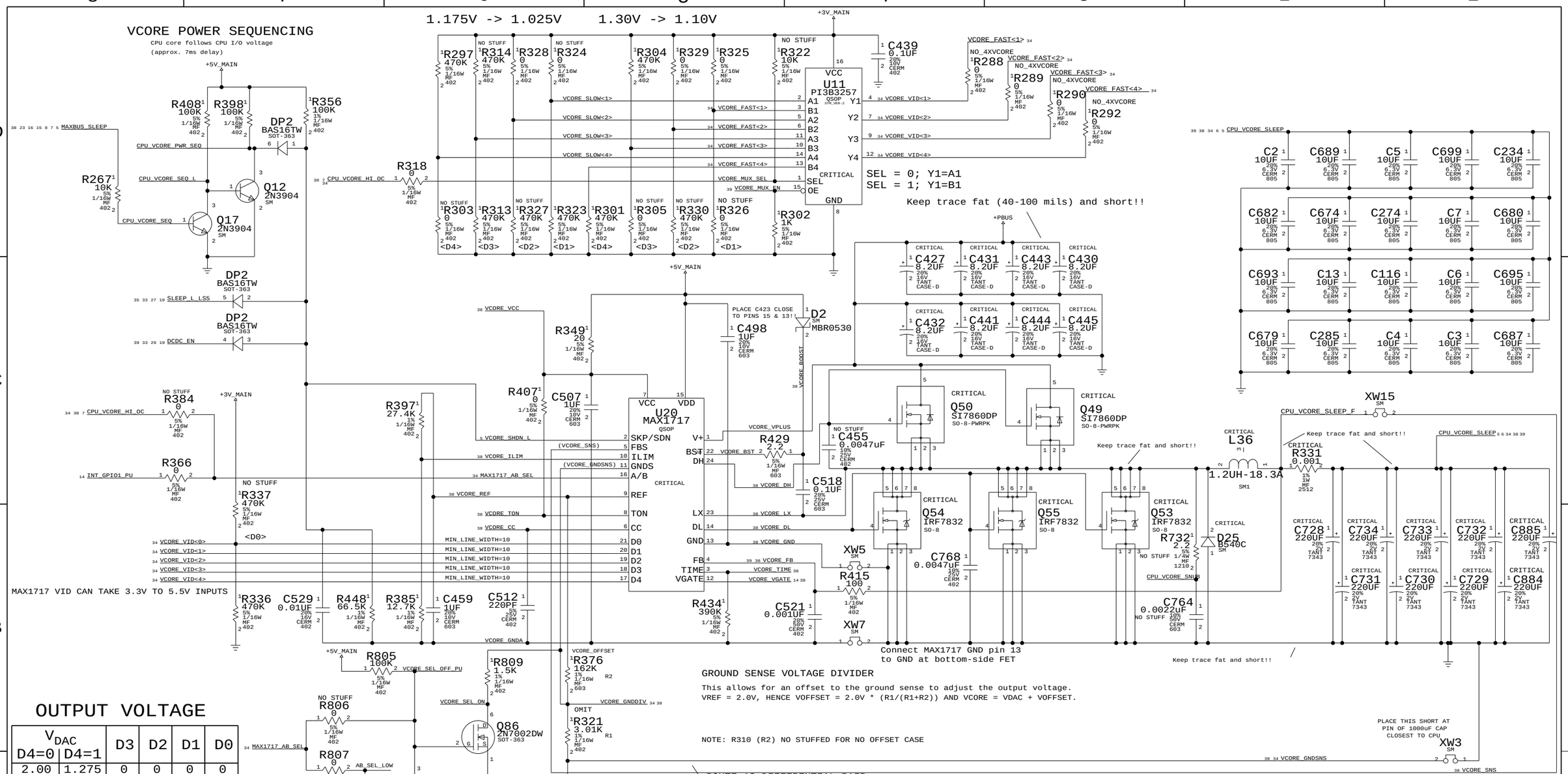

OUTPUT VOLTAGE

V_{DAC} D4=0	V_{DAC} D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S4023	1	RESISTOR	R321	?	1_30_VCORE
114S6343	1	RESISTOR	R321	?	1_32_VCORE

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

VCORE SUPPLY

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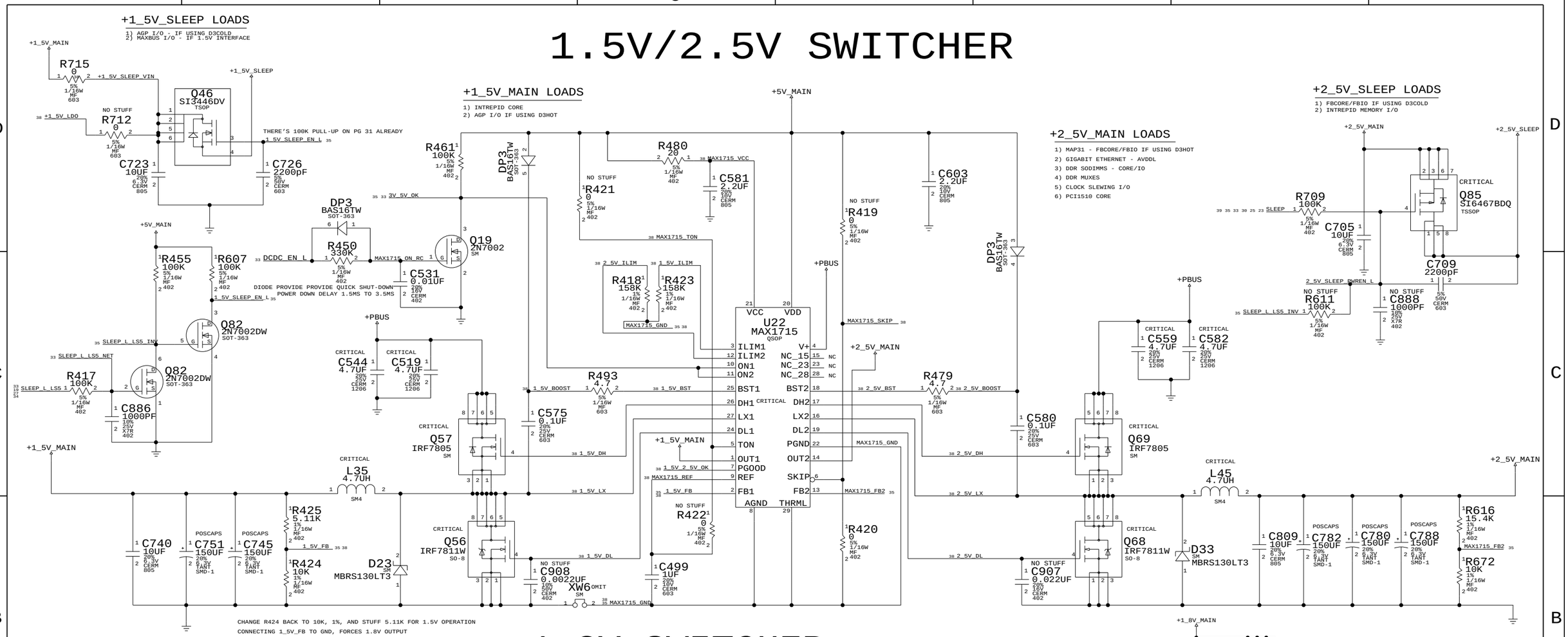
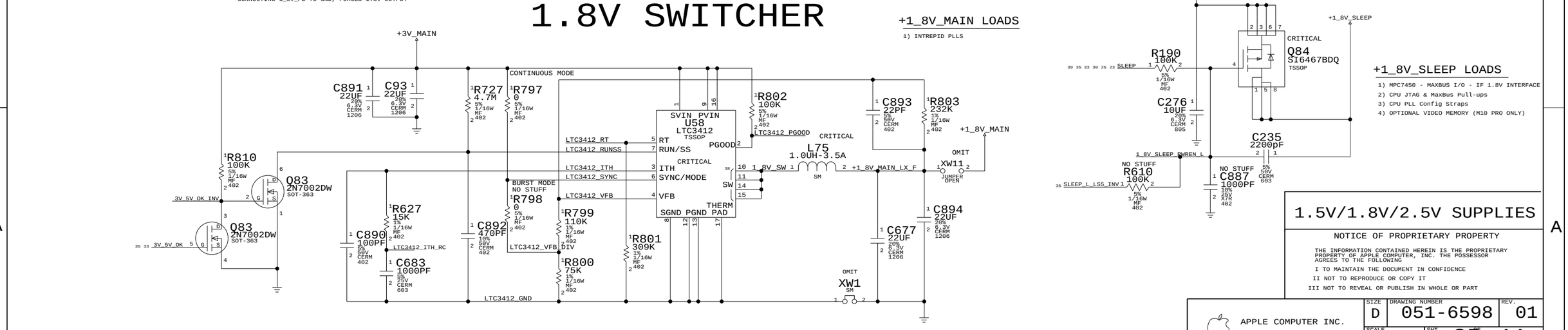
1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L			250.0000	10_MIL_SPACING			5 8
	CPU_ADDR<0..31>	5		250			83_MHZ	5 8
	CPU_ARTRY_L			250.0000	10_MIL_SPACING			5 8
	CPU_BG_L			250.0000	10_MIL_SPACING			5 8
	CPU_BR_L			250.0000	10_MIL_SPACING			5 8
	CPU_CI_L	5		250.0000				5 8
	CPU_DATA<0..31>	5		250			83_MHZ	6 8
	CPU_DATA<32..63>	5		250			83_MHZ	6 8
	CPU_DBG_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_DTI<0..2>	5		250				5 8
	CPU_DRDY_L_UF				10_MIL_SPACING			
	CPU_DRDY_L			250.0000	10_MIL_SPACING			5 8
	CPU_GBL_L	5		250.0000				5 8
	CPU_HIT_L			250.0000	10_MIL_SPACING			5 8
	CPU_QACK_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_QREQ_L			250.0000	10_MIL_SPACING			5 8
	CPU_TA_L			250.0000	10_MIL_SPACING			5 8
	CPU_TBST_L	5		250.0000	10_MIL_SPACING			5 8
	CPU_TEA_L			250.0000				5 8
	CPU_TS_L			250.0000	10_MIL_SPACING			5 8
	CPU_TSIZ<0..2>	5		250				5 8
	CPU_TT<0..4>	5		250				5 8
	CPU_WT_L	5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>	4		200			167_MHZ	9 10
	RAM_DATA_A<7..0>	4		200			167_MHZ	10 11
	RAM_DATA_B<7..0>	4		200			167_MHZ	10 11
	MEM_DQS<0>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200				9 10
	RAM_DQS_A<0>	4		200				10 11
	RAM_DQS_B<0>	4		200				10 11
	MEM_DQM<0>	4		200				9 10
	RAM_DQM_A<0>	4		200				10 11
	RAM_DQM_B<0>	4		200				10 11
GROUP 1	MEM_DATA<15..8>	4		200			167_MHZ	9 10
	RAM_DATA_A<15..8>	4		200			167_MHZ	10 11
	RAM_DATA_B<15..8>	4		200			167_MHZ	10 11
	MEM_DQS<1>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200				9 10
	RAM_DQS_A<1>	4		200				10 11
	RAM_DQS_B<1>	4		200				10 11
	MEM_DQM<1>			200				9 10
	RAM_DQM_A<1>	4		200				10 11
	RAM_DQM_B<1>	4		200				10 11
GROUP 2/3	MEM_DATA<31..16>	4		200			167_MHZ	9 10
	RAM_DATA_A<31..16>	4		200			167_MHZ	10 11
	RAM_DATA_B<31..16>	4		200			167_MHZ	10 11
	MEM_DQS<3..2>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200			167_MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>	4		200			167_MHZ	10 11
	RAM_DQS_B<3..2>	4		200			167_MHZ	10 11
	MEM_DQM<3..2>	4		200			167_MHZ	9 10
	RAM_DQM_A<3..2>	4		200			167_MHZ	10 11
	RAM_DQM_B<3..2>	4		200			167_MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>	4		200			167_MHZ	9 10
	RAM_DATA_A<47..32>	4		200			167_MHZ	10 11
	RAM_DATA_B<47..32>	4		200			167_MHZ	10 11
	MEM_DQS<5..4>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200			167_MHZ	9 10
	RAM_DQS_A<5..4>	4		200			167_MHZ	10 11
	RAM_DQS_B<5..4>	4		200			167_MHZ	10 11
	MEM_DQM<5..4>	4		200			167_MHZ	9 10
	RAM_DQM_A<5..4>	4		200			167_MHZ	10 11
	RAM_DQM_B<5..4>	4		200			167_MHZ	10 11
GROUP 6	MEM_DATA<55..48>	4		200			167_MHZ	9 10
	RAM_DATA_A<55..48>	4		200			167_MHZ	10 11
	RAM_DATA_B<55..48>	4		200			167_MHZ	10 11
	MEM_DQS<6>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200				9 10
	RAM_DQS_A<6>			200				10 11
	RAM_DQS_B<6>	4		200				10 11
	MEM_DQM<6>			200				9 10
	RAM_DQM_A<6>	4		200				10 11
	RAM_DQM_B<6>	4		200				10 11
GROUP 7	MEM_DATA<63..56>	4		200			167_MHZ	9 10
	RAM_DATA_A<63..56>	4		200			167_MHZ	10 11
	RAM_DATA_B<63..56>	4		200			167_MHZ	10 11
	MEM_DQS<7>	TOTAL LENGTH CONTROLLED BY SPREADSHEET		200				9 10
	RAM_DQS_A<7>			200				10 11
	RAM_DQS_B<7>			200				10 11
	MEM_DQM<7>	4		200				9 10
	RAM_DQM_A<7>	4		200				10 11
	RAM_DQM_B<7>	4		200				10 11
ADDR	MEM_ADDR<12..0>	4					83_MHZ	9
	RAM_ADDR<12..0>	6		200				9 11
	MEM_BA<1..0>	4						9
	RAM_BA<1..0>	6		200				9 11
CONTROL	MEM_CS_L<3..0>	4						9
	RAM_CS_L<3..0>	6		200				9 11
	MEM_CKE<3..0>	4						9
	RAM_CKE<3..0>	6		200				9 11
	MEM_RAS_L	4						9
	RAM_RAS_L			200.0000				9 11
	MEM_CAS_L	4						9
	RAM_CAS_L			200.0000				9 11
	MEM_WE_L	4						9
	RAM_WE_L			200.0000				9 11
	MEM_MUXSEL_H<1..0>	3						9 10
	MEM_MUXSEL_L<1..0>	3						9 10
	RAM_MUXSEL_H	5						10
	RAM_MUXSEL_L	5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME			MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF						10_MIL_SPACING		8
	SYSCLK_CPU			4		200.0000	10_MIL_SPACING		5 8
	INT_CPUFB_OUT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_SHORT			3			10_MIL_SPACING		8
	INT_CPUFB_OUT_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_IN_NORM			3			10_MIL_SPACING		8
	INT_CPUFB_LONG			3			10_MIL_SPACING		8
	INT_CPUFB_IN					200.0000	10_MIL_SPACING		8
	SYSCLK_DDRCLK_A0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B0_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_B1_L_UF			3		200.0000	10_MIL_SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1				200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1		3		200.0000	10_MIL_SPACING		9 11
	INT_REF_CLK_OUT			3		200.0000	10_MIL_SPACING		14
	INT_REF_CLK_IN					200.0000	10_MIL_SPACING		14
	CLK66M_GPU_AGP_UF					200.0000	10_MIL_SPACING		12
	CLK66M_GPU_AGP			4		200.0000	10_MIL_SPACING		12 18
	INT_AGP_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_AGP_FB_IN			4		200.0000	10_MIL_SPACING		12
	CLK33M_CBUS_UF					200.0000	10_MIL_SPACING		12
	CLK33M_CBUS		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 17
	CLK33M_AIRPORT_UF					200.0000	10_MIL_SPACING		12
	CLK33M_AIRPORT		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 24 39
	CLK33M_USB2_UF					200.0000	10_MIL_SPACING		12
	CLK33M_USB2		SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10_MIL_SPACING		12 26
	INT_PCI_FB_OUT					200.0000	10_MIL_SPACING		12
	INT_PCI_FB_IN			3		200.0000	10_MIL_SPACING		12
MAP31	GPU_CLK27M_OUT						10_MIL_SPACING		
	GPU_CLK27M_UF						10_MIL_SPACING		
	GPU_SSCLK_UF						10_MIL_SPACING		
	GPU_SSCLK_IN						10_MIL_SPACING		
	GPU_FBCLK0						10_MIL_SPACING		
	GPU_FBCLK0_L						10_MIL_SPACING		
	GPU_FBCLK1						10_MIL_SPACING		
	GPU_FBCLK1_L						10_MIL_SPACING		
	GPU_DVO_CLKP						10_MIL_SPACING		19 20
CRYSTALS	CLK27M_GPU_XOUT						10_MIL_SPACING		
	CLK27M_XTAL_IN						10_MIL_SPACING		
	CLK27M_GPU_XIN						10_MIL_SPACING		
	CLK18M_INT_XIN						10_MIL_SPACING		14
	CLK18M_INT_XOUT						10_MIL_SPACING		14
	CLK18M_XTAL_IN						10_MIL_SPACING		14
	CLK18M_INT_EXT						10_MIL_SPACING		14
	CLK25M_ENET_XIN						10_MIL_SPACING		27
	CLK25M_ENET_XOUT						10_MIL_SPACING		27
	NEC_XT1						10_MIL_SPACING		26
	NEC_XT2		THERE'S ANOTHER 280MIL LEG				10_MIL_SPACING		26
SOUND	SND_SCLK			7		200.0000	10_MIL_SPACING		14 25 39
	SND_CLKOUT					200.0000	10_MIL_SPACING		14 25 39
ETHERNET MARVELL	CLKENET_PHY_RX					200.0000			27
	CLKENET_LINK_RX			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_GBE_REF					200.0000			27
	CLKENET_LINK_GBE_REF			3		200.0000	10_MIL_SPACING		13 27
	CLKENET_PHY_TX					200.0000			27
	CLKENET_LINK_TX			5		200.0000	10_MIL_SPACING		13 27
	CLKENET_LINK_GTX					200.0000			13
	CLKENET_PHY_GTX			3		200.0000	10_MIL_SPACING		13 27
FIREWIRE	CLKFW_PHY_PCLK					200.0000			28
	CLKFW_LINK_PCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_PHY_LCLK			3		200.0000	10_MIL_SPACING		13 28
	CLKFW_LINK_LCLK					200.0000			13
	FW_XI					200.0000	10_MIL_SPACING		28
	FW_OSC					200.0000	10_MIL_SPACING		28

SIGNAL CONSTRAINTS - PAGE 1

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Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ	12 18
	AGP_CBE<3..2>		5	100				66 MHZ	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..11>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ	9 12 17 24 26 39
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ	12 17 24 26 39
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 24 26 39
	PCI_PAR					MIN_DAISY_CHAIN			12 17 24 26 39
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 24
	UIDE_DATA<7>				200				13 24
	UIDE_DATA<6..0>				200			100 MHZ	13 24
	UIDE_ADDR<2..0>				200			100 MHZ	13 24
	UIDE_RST_L				200.0000				13 24
	UIDE_DIOW_L				200.0000				13 24
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 24
	UIDE_DMACK_L				200.0000				13 24
	UIDE_CS0_L				200.0000				13 24
	UIDE_CS1_L				200.0000				13 24
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 24
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5		200			100 MHZ	24
	HD_ADDR<2..0>		5		200			100 MHZ	24
	HD_RESET_L		5		200.0000				24
	HD_DIOW_L		5		200.0000				24
	HD_DIOR_L		5	10 MIL SPACING	200.0000				24
	HD_DMACK_L		5		200.0000				24
	HD_CS0_L		5		200.0000				24
	HD_CS1_L		5		200.0000				24
	HD_DMARQ				200.0000				13 24
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				24
	HD_INTRQ		5						13 24
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 24
	EIDE_ADDR<2..0>							33 MHZ	13 24
	EIDE_CS0_L								13 24
	EIDE_CS1_L								13 24
	EIDE_RD_L								13 24
	EIDE_WR_L								13 24
	EIDE_IOCHRDY								13 24
	EIDE_INT								13 24
	EIDE_RST_L								13 24
	EIDE_DMACK_L								13 24
	EIDE_DMARQ								13 24
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	24 39
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	24 39
	EIDE_OPTICAL_CS0_L								24 39
	EIDE_OPTICAL_CS1_L								24 39
	EIDE_OPTICAL_RD_L								24 39
	EIDE_OPTICAL_WR_L								24 39
	EIDE_OPTICAL_IOCHRDY								24 39
	EIDE_OPTICAL_INT								24 39
	EIDE_OPTICAL_RST_L								24 39
	EIDE_OPTICAL_DMAACK_L								24 39
	EIDE_OPTICAL_DMA_RQ								24 39
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 27
	ENET_RX_DV								13 27
	ENET_RX_ER								13 27
	ENET_PHY_TXD<7..0>		5						13 27
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 27
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 27
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 27
	ENET_MDC								13 27
	ENET_COL								13 27
	ENET_CRS								13 27
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 28
	FW_PHY_DATA<7..0>		5						28
	FW_LINK_CNTL<1..0>								13 28
	FW_PHY_CNTL<1..0>								28
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 28
	FW_PINT								13 28

NEED TO MATCH DELAY TO 250

TOTAL UIDE+HD SKEW <500MIL

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR		MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0					27
	MDI_P<0>	ENET_MDI0					27
	MDI_M<1>	ENET_MDI1		SPACING DELETED BECAUSE			27
	MDI_P<1>	ENET_MDI1		OF PHYSICAL CONSTRAINTS			27
	MDI_M<2>	ENET_MDI2		AROUND MARVELL PHY			27
	MDI_P<2>	ENET_MDI2					27
	MDI_M<3>	ENET_MDI3					27
	MDI_P<3>	ENET_MDI3					27
	RJ45_DN<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DP<0>	RJ45_DP0			10 MIL SPACING		27 39
	RJ45_DN<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DP<1>	RJ45_DP1			10 MIL SPACING		27 39
	RJ45_DN<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DP<2>	RJ45_DP2			10 MIL SPACING		27 39
	RJ45_DN<3>	RJ45_DP3			10 MIL SPACING		27 39
	RJ45_DP<3>	RJ45_DP3			10 MIL SPACING		27 39
FIREWIRE	FW_TPA0N	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA0P	FW_TPA0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0N	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB0P	FW_TPB0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI0N	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0			MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPA1P	FW_TPA1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1N	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPB1P	FW_TPB1		500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		28 29
	FW_TPI1N	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPI1P	FW_TPI1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1N	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
	FW_TPO1P	FW_TPO1			MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 39
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	CLKLVDS_LP	CLKLVDS_L			10 MIL SPACING	4	19 22 39
	LVDS_L0N	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L0P	LVDS_L0			10 MIL SPACING		19 22 39
	LVDS_L1N	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L1P	LVDS_L1			10 MIL SPACING		19 22 39
	LVDS_L2N	LVDS_L2			10 MIL SPACING		19 22 39
	LVDS_L2P	LVDS_L2			10 MIL SPACING		19 22 39
UPPER	CLKLVDS_UN	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	CLKLVDS_UP	CLKLVDS_U			10 MIL SPACING	4	19 22 39
	LVDS_U0N	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U0P	LVDS_U0			10 MIL SPACING		19 22 39
	LVDS_U1N	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U1P	LVDS_U1			10 MIL SPACING		19 22 39
	LVDS_U2N	LVDS_U2			10 MIL SPACING		19 22 39
	LVDS_U2P	LVDS_U2			10 MIL SPACING		19 22 39
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CONN_CLKP	CLKCONN_TMDS			10 MIL SPACING	4	22 39
	TMDS_CLKN	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS			10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DP<0>	TMDS_D0			10 MIL SPACING		20 22 39
	TMDS_DN<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DP<1>	TMDS_D1			10 MIL SPACING		20 22 39
	TMDS_DN<2>	TMDS_D2			10 MIL SPACING		20 22 39
	TMDS_DP<2>	TMDS_D2			10 MIL SPACING		20 22 39
USB	NEC_USB_DAM	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DAP	NEC_USB_DA		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DEM	USB_DE			5 MIL SPACING		14
	USB_DEP	USB_DE			5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_DBP	NEC_USB_DB		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	USB_DFM	USB_DF			5 MIL SPACING		14
	USB_DFP	USB_DF			5 MIL SPACING		14
	BT_USB_DM	BT_USB_D			5 MIL SPACING		14 24 39
	BT_USB_DP	BT_USB_D			5 MIL SPACING		14 24 39
	NEC_USB_RSDM1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP1	NEC_USB_RSD1		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDM2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	NEC_USB_RSDP2	NEC_USB_RSD2		MIN_LINE_WIDTH=5	10 MIL SPACING		26
	MODEM_USB_DM	MODEM_USB_D			5 MIL SPACING		14 25 39
	MODEM_USB_DP	MODEM_USB_D			5 MIL SPACING		14 25 39
	LEFT_USB_DM	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	LEFT_USB_DP	LEFT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		24 26 39
	RIGHT_USB_DM	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
	RIGHT_USB_DP	RIGHT_USB		MIN_LINE_WIDTH=5	10 MIL SPACING		26 32 39
POWER SUPPLIES	1772_CSSN	1772_CSS			DIFF		31
	1772_CSSP	1772_CSS			DIFF		31
	1772_CSIN	1772_CSI			DIFF		31
	1772_CSIP	1772_CSI			DIFF		31
	3V_SNSM	3V_SNS			DIFF		33
	3V_SNSP	3V_SNS			DIFF		33
	5V_SNSM	5V_SNS			DIFF		33
	5V_SNSP	5V_SNS			DIFF		33
THERMOSTAT	THERM1_DM	THERM1			DIFF		25
	THERM1_DP	THERM1			DIFF		25
	THERM2_DM	THERM2			DIFF		25
	THERM2_DP	THERM2			DIFF		25
	THERM1_M_DM	THERM1_MAIN			DIFF		
	THERM1_M_DP	THERM1_MAIN			DIFF		
	THERM2_M_DM	THERM2_MAIN			DIFF		
	THERM2_M_DP	THERM2_MAIN			DIFF		
	THERM1_A_DM	THERM1_ALT			DIFF		25
	THERM1_A_DP	THERM1_ALT			DIFF		25
	THERM2_A_DM	THERM2_ALT			DIFF		25
	THERM2_A_DP	THERM2_ALT			DIFF		25

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

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SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE NONE	SHT 37 OF 44	

POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	39
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	39
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	35
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31 32
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	31
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31 39
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		31
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	31
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	31
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10		31
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10		31
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		30 32
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10		32 33
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10		32
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		32
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		25 30
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24 33
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	24
TRACKPAD	+5V_TPAD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=10		23 39
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		23 39
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 39
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25		22 39
KB LED	KBD_LED1_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
	KBD_LED2_OUT	VOLTAGE=0V	MIN_LINE_WIDTH=10		23 39
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 39
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	25

	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	GND	
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1	
	CHGND1				
INVERTER	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2	
	CHGND2				
TRACKPAD	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3	
	CHGND3				
LVDS	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4	39
	CHGND4				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5	
	CHGND5				
I/O AREA	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6	
	CHGND6				
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	27

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 34 39
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 7 8 15 16 23 34
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10		12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10		9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8		13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M10	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 39
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1838 +1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1839 GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
	1840 +2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1841 +1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1842 +1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1843 +1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	1844 +GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	1845 +1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	1846 +1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	1847 +3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	1848 +3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	1849 +GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20		19
	1850 +2_5V_SLEEP_NECK1	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
	1851 +3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		21
	1852 +1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
	1853 +1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10		19
	1854 GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
	1855 +GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10		19
	1856 +2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
	1857 +1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10		21
	1858 +1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10		21
	1859 +2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	1860 +3V_SI_PLLVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	1861 +3V_SI_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
	1862 +3V_SI_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	27
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	28 29
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28 29
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	28
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 39
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	26
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10		32
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		32
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	31 32
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	33
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	33
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10		33
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8		35
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	35
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	35
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8		35
	2_5V_ILIM		MIN_LINE_WIDTH=8		35
	MAX1715_TON		MIN_LINE_WIDTH=8		35
	MAX1715_SKIP		MIN_LINE_WIDTH=8		35
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8		35
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	35
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=200	MIN_NECK_WIDTH=10	34
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	34
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	34
	VCORE_ILIM		MIN_LINE_WIDTH=8		34
	VCORE_REF		MIN_LINE_WIDTH=8		34
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8		34
	VCORE_CC		MIN_LINE_WIDTH=8		34
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34 39
	VCORE_TIME		MIN_LINE_WIDTH=8		34
	VCORE_VGATE		MIN_LINE_WIDTH=8		14 34
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30		34
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8		34
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8		34
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	19
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	19
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	19
	1778_ION		MIN_LINE_WIDTH=8		19
	1778_ITH		MIN_LINE_WIDTH=8		19
	1778_ITH_RC		MIN_LINE_WIDTH=8		19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8		35
	1778_VFB		MIN_LINE_WIDTH=8		19 39
	1778_FCB		MIN_LINE_WIDTH=8		19
	1778_VRNG		MIN_LINE_WIDTH=8		19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	35
	1_8V_VFB		MIN_LINE_WIDTH=8		
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8		
	LTC3411_ITH		MIN_LINE_WIDTH=8		
	LTC3411_SYNC		MIN_LINE_WIDTH=8		
	LTC3411_SHDN		MIN_LINE_WIDTH=8		
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	14
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
D	051-6598	01
SCALE NONE	SHT 38 OF 44	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 27
FUNC_TEST=YES JTAG_ASIC_TDI 27
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 27
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 27
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 7 23
FUNC_TEST=YES JTAG_CPU_TMS 5 23
FUNC_TEST=YES JTAG_CPU_TDI 5 23
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 23
FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39

FUNC_TEST=YES INT_I2C_CLK0 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 25
FUNC_TEST=YES INT_I2C_DATA1 13 14 25
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 37
FUNC_TEST=YES TMDS_DP<0> 20 22 37
FUNC_TEST=YES TMDS_DN<1> 20 22 37
FUNC_TEST=YES TMDS_DP<1> 20 22 37
FUNC_TEST=YES TMDS_DN<2> 20 22 37
FUNC_TEST=YES TMDS_DP<2> 20 22 37
FUNC_TEST=YES TMDS_CONN_CLKN 22 37

FUNC_TEST=YES TMDS_CONN_CLKP 22 37
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 37
FUNC_TEST=YES LVDS_L0P 19 22 37
FUNC_TEST=YES LVDS_L1N 19 22 37
FUNC_TEST=YES LVDS_L1P 19 22 37
FUNC_TEST=YES LVDS_L2N 19 22 37
FUNC_TEST=YES LVDS_L2P 19 22 37
FUNC_TEST=YES CLKLVDS_LN 19 22 37
FUNC_TEST=YES CLKLVDS_LP 19 22 37
FUNC_TEST=YES LVDS_U0N 19 22 37
FUNC_TEST=YES LVDS_U0P 19 22 37
FUNC_TEST=YES LVDS_U1N 19 22 37
FUNC_TEST=YES LVDS_U1P 19 22 37
FUNC_TEST=YES LVDS_U2N 19 22 37
FUNC_TEST=YES LVDS_U2P 19 22 37
FUNC_TEST=YES CLKLVDS_UN 19 22 37
FUNC_TEST=YES CLKLVDS_UP 19 22 37
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 38
FUNC_TEST=YES TV_GND2 22 38

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 25
FUNC_TEST=YES SND_SYNC 14 25
FUNC_TEST=YES SND_CLKOUT 14 25 36
FUNC_TEST=YES INT_AUDIO_TO_SND 14 25
FUNC_TEST=YES SND_SCLK 14 25 36
FUNC_TEST=YES SND_HW_RESET_L 14 25
FUNC_TEST=YES SND_HP_SENSE_L 14 25
FUNC_TEST=YES SND_LIN_SENSE_L 14 25
FUNC_TEST=YES INT_I2C_DATA2 14 25
FUNC_TEST=YES INT_I2C_CLK2 14 25
T298 FUNC_TEST=YES CHGND4 38
T299 FUNC_TEST=YES SLEEP_LED 23 25

FUNC_TEST=YES BT_USB_DM 14 24 37
FUNC_TEST=YES BT_USB_DP 14 24 37
FUNC_TEST=YES MODEM_USB_DM 14 25 37
FUNC_TEST=YES MODEM_USB_DP 14 25 37
FUNC_TEST=YES PCI_AD<0> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<1> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<2> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<3> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<4> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<5> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<6> 9 12 17 24 26 37

FUNC_TEST=YES PCI_AD<7> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<8> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<9> 9 12 17 24 26 37
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FUNC_TEST=YES PCI_AD<11> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<12> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<13> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<14> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<15> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<16> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<17> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<18> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<19> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<20> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<21> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<22> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<23> 12 17 24 26 37
FUNC_TEST=YES PCI_AD<24> 9 12 17 24 26 37
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FUNC_TEST=YES PCI_AD<26> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<27> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<28> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<29> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<30> 9 12 17 24 26 37
FUNC_TEST=YES PCI_AD<31> 9 12 17 24 26 37
FUNC_TEST=YES PCI_FRAME_L 12 17 24 26 37
FUNC_TEST=YES PCI_TRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_IRDY_L 12 17 24 26 37
FUNC_TEST=YES PCI_DEVSEL_L 12 17 24 26 37
FUNC_TEST=YES PCI_STOP_L 12 17 24 26 37

FUNC_TEST=YES PCI_PAR 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<0> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<1> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<2> 12 17 24 26 37
FUNC_TEST=YES PCI_CBE<3> 12 17 24 26 37
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 24
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 24
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 24
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 24 37
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FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 24 37
FUNC_TEST=YES EIDE_OPTICAL_RD_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 24 37
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 24 37
T291 FUNC_TEST=YES SND_AMP_MUTE 25
T292 FUNC_TEST=YES SND_HP_MUTE_INV 25

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_RST_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_WR_L 24 37
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 24 37
FUNC_TEST=YES EIDE_OPTICAL_INT 24 37
FUNC_TEST=YES TPAD_F_TXD 23
FUNC_TEST=YES TPAD_F_RXD 23
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 25
FUNC_TEST=YES COMM_SHUTDOWN 14 25
FUNC_TEST=YES COMM_RING_DET_L 14 25 30
FUNC_TEST=YES KBD_ID 23 30
FUNC_TEST=YES +5V_TPAD_SLEEP 23 38
FUNC_TEST=YES +3V_HALL_EFFECT 23 38
FUNC_TEST=YES KBD_CAPSLOCK_LED 23
FUNC_TEST=YES KBD_FUNCTION_L 23 30
FUNC_TEST=YES KBD_CONTROL_L 23 30
FUNC_TEST=YES KBD_COMMAND_L 23 30
FUNC_TEST=YES KBD_OPTION_L 23 30
FUNC_TEST=YES KBD_SHIFT_L 23 30
FUNC_TEST=YES KBD_X<0> 23 30
FUNC_TEST=YES KBD_X<1> 23 30
FUNC_TEST=YES KBD_X<2> 23 30
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FUNC_TEST=YES KBD_X<5> 23 30
FUNC_TEST=YES KBD_X<6> 23 30
FUNC_TEST=YES KBD_X<7> 23 30
FUNC_TEST=YES KBD_X<8> 23 30
T287 FUNC_TEST=YES SRCLK_TP 26
T288 FUNC_TEST=YES SRMOD_TP 26
T289 FUNC_TEST=YES TEB_TP 26
T290 FUNC_TEST=YES TEST_TP 26

FUNC_TEST=YES KBD_X<9> 23 30
FUNC_TEST=YES KBD_Y<0> 23 30
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FUNC_TEST=YES KBD_Y<2> 23 30
FUNC_TEST=YES KBD_Y<3> 23 30
FUNC_TEST=YES KBD_Y<4> 23 30
FUNC_TEST=YES KBD_Y<5> 23 30
FUNC_TEST=YES KBD_Y<6> 23 30
FUNC_TEST=YES KBD_Y<7> 23 30
FUNC_TEST=YES KBD_NUMLOCK_LED 23
FUNC_TEST=YES +BATT_POS 31 38
FUNC_TEST=YES BATT_CLK 31
FUNC_TEST=YES BATT_DATA 31
FUNC_TEST=YES BATT_NEG 31 38
FUNC_TEST=YES PMU_BATT_DET_L 30 31
FUNC_TEST=YES FANR_GND 25 38
FUNC_TEST=YES FANL_GND 25 38
FUNC_TEST=YES FANL_TACH 25
T271 FUNC_TEST=YES FANR_PWM 25
T272 FUNC_TEST=YES FANL_PWM 25
FUNC_TEST=YES RJ45_DP<0> 27 37
FUNC_TEST=YES RJ45_DN<0> 27 37
FUNC_TEST=YES RJ45_DP<1> 27 37
FUNC_TEST=YES RJ45_DN<1> 27 37
FUNC_TEST=YES RJ45_DP<2> 27 37
FUNC_TEST=YES RJ45_DN<2> 27 37
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FUNC_TEST=YES RJ45_DN<3> 27 37
FUNC_TEST=YES FW_TPO0R 29 38
T281 FUNC_TEST=YES VCORE_VID0
T282 FUNC_TEST=YES VCORE_VID1
T283 FUNC_TEST=YES VCORE_VID2
T284 FUNC_TEST=YES VCORE_VID3
T285 FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 29 37
FUNC_TEST=YES FW_TPO1N 29 37
FUNC_TEST=YES FW_TPI1P 29 37
FUNC_TEST=YES FW_TPI1N 29 37
FUNC_TEST=YES CHARGE_LED_L 30 31
FUNC_TEST=YES ADAPTER_DET 30 31
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 24
FUNC_TEST=YES SUTRO_ALS_OUT 23 24
FUNC_TEST=YES KBD_LED1_OUT 23 38
FUNC_TEST=YES KBD_LED2_OUT 23 38
FUNC_TEST=YES COMM_TXD_L 14 25
FUNC_TEST=YES COMM_TRXC 14 25
FUNC_TEST=YES COMM_GPIO_L 14 25
FUNC_TEST=YES COMM_DTR_L 14 25
FUNC_TEST=YES COMM_RTS_L 14 25
FUNC_TEST=YES COMM_RXD 14 25
FUNC_TEST=YES PMU_KB_RESET_L 30
FUNC_TEST=YES PWR_BUTTON_L 23 25
FUNC_TEST=YES +PBUS 38
FUNC_TEST=YES +24V_PBUS 38
FUNC_TEST=YES GPU_VCORE 18 19 38
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 34 38
FUNC_TEST=YES VCORE_FB 34 38
FUNC_TEST=YES +1_8V_MAIN 38
FUNC_TEST=YES +3V_PMU 38
FUNC_TEST=YES +5V_DDC_SLEEP 22 38
FUNC_TEST=YES +12_8V_INV 22 38
T286 FUNC_TEST=YES VCORE_MUX_EN 34

FUNC_TEST=YES +5V_INV_SW 22 38
FUNC_TEST=YES LEFT_USB_DM 24 26 37
FUNC_TEST=YES LEFT_USB_DP 24 26 37
FUNC_TEST=YES RIGHT_USB_DM 26 32 37
FUNC_TEST=YES RIGHT_USB_DP 26 32 37
FUNC_TEST=YES NEC_LEFT_USB_PWREN 24 26
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 24 26
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 26 32
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 26 32
FUNC_TEST=YES DCDC_EN 19 29 33 34
FUNC_TEST=YES BBANG_HRESET_L 23
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 24 26 30
FUNC_TEST=YES RF_DISABLE_L_SPN 24
FUNC_TEST=YES AIRPORT_CLKRUN_L 24
FUNC_TEST=YES ROM_RW_L 9 12 24
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 24
FUNC_TEST=YES ROM_CS_L 9 12 24
FUNC_TEST=YES CLK33M_AIRPORT 12 24 36
FUNC_TEST=YES AIRPORT_IDSEL 24
FUNC_TEST=YES ROM_OE_L 9 12 24
T273 FUNC_TEST=YES INT_MOD_DTI 14 25
T274 FUNC_TEST=YES JTAG_CPU_TRST_L 5 23 39
T275 FUNC_TEST=YES MOD_BITCLK 14 25
T276 FUNC_TEST=YES MOD_CLKOUT 14 25
T277 FUNC_TEST=YES MOD_DTO 14 25
T278 FUNC_TEST=YES MOD_SYNC 14 25
T279 FUNC_TEST=YES SLEEP 23 25 30 33 35
T280 FUNC_TEST=YES 1778_VFB 19 38

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SCALE NONE	SHT 39 OF 44	

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U41 TO MIX PSOP64 SYMBOL
5) ADDED CPU AVDD LDO (D6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R608 TO DISCONNECT INT GPIO0 FROM C6 FSEL
8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NET_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL_DIODE_DIFF_PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

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*** Signal Cross-Reference for the entire design ***

+1.0V_MARVELL     27D2< 38B3>
+1.5V_AGP         12C5< 12D1< 12D4< 15D5< 16C8<
                  18C6< 18D6< 19A8< 19B4<> 19D5<>
                  21B8< 21D6< 38C3>
+1.5V_AGP_GPU     21C5< 38C3>
+1.5V_AGP_MEM     19B4<> 38B3>
+1.5V_GPU_VDD15   19D3< 38C3>
+1.5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 38D3>
+1.5V_INTREPID_PLL1  14C3< 38D3>
+1.5V_INTREPID_PLL2  14D3< 38D3>
+1.5V_INTREPID_PLL3  14D3< 38D3>
+1.5V_INTREPID_PLL4  14D3< 38D3>
+1.5V_INTREPID_PLL5  12D3< 38D3>
+1.5V_INTREPID_PLL6  12D6< 38D3>
+1.5V_INTREPID_PLL7  8D5< 38D3>
+1.5V_INTREPID_PLL8  14D3< 38D3>
+1.5V_LDO         35D6< 38D6>
+1.5V_MAIN        38D6>
+1.5V_SLEEP_NECK   21A3<> 38B3>
+1.5V_SLEEP_VIN   35D8< 38D6>
+1.8V_ATI_PVDD    19C5<> 21B6< 21B6< 21D6<> 38C3>
+1.8V_ATI_TPVDD   21D2<>
+1.8V_DVO_P       21B2<
+1.8V_GPU         18A7< 19D8< 20A5< 21A2< 21A6<
                  21B1< 21B6< 21C8< 21D6< 21D8< 38C3>
+1.8V_GPU_AVDD    21D5< 38C3>
+1.8V_GPU_AVDDQ   21A4< 21D7< 38C3>
+1.8V_GPU_MEMPLL  21B5< 38C3>
+1.8V_GPU_PLL     21D5< 38C3>
+1.8V_GPU_PNLI0   21A5< 38C3>
+1.8V_GPU_PNLPLL  21B5< 38C3>
+1.8V_GPU_TP_PLL  21B4< 21D1<
+1.8V_GPU_VDDDI   21C7< 21D4< 38C3>
+1.8V_MAIN        38D6> 39A2>
+1.8V_MAIN_LX_F   35A4>>
+1.8V_PVDD_NECK   19B5<> 38B3>
+1.8V_SLEEP       38D6>
+1.8V_SLEEP_NECK  38D6>
+1.95V_FW_DVDD    28C4< 28C7<> 28D5< 38A3>
+1.95V_FW_DVDD_PORT1  28D6< 38A3>
+1.95V_FW_DVDD_RX0  28C5< 38A3>
+1.95V_FW_DVDD_TX0  28D5< 38A3>
+1.95V_FW_PLL400VDD  28D5< 38A3>
+1.95V_FW_PLL500VDD  28D5< 38A3>
+1.95V_FW_PLLVDD  28D5< 28D7<> 38A3>
+2.5V_CG_MAIN     14C6< 38A3>
+2.5V_GPU         21A7< 21B6< 21D3< 21D7< 21D8<
                  38B3>
+2.5V_GPU_A2VDD   21D4< 21D7< 38C3>
+2.5V_GPU_PNLI0   21A5< 38C3>
+2.5V_INTREPID    9A8< 16D3< 16D5< 16D6< 18D8< 15D7<
                  16B8< 38D3>
+2.5V_MAIN        38D6>
+2.5V_MARVELL     27B8< 27C4<> 38A3>
+2.5V_MARVELL_AVDD  27C4< 38B3>
+2.5V_SLEEP       38D6>
+2.5V_SLEEP_NECK1  19C4<> 38B3>
+2.5V_SLEEP_NECK2  21D3< 38B3>
+3V_ATI_OSC_SLEEP  18D2< 38C3>
+3V_ATI_SS        18B2< 38C3>
+3V_CG_PLL_MAIN   14C6< 38A3>
+3V_FW            28A3< 28D7<> 29D5< 38A3>
+3V_FW_AVDD       28C6< 38A3>
+3V_FW_AVDD_PORT0  28C6< 38A3>
+3V_FW_AVDD_PORT1  28C6< 38A3>
+3V_FW_AVDD_PORT2  28D6< 38A3>
+3V_FW_ESD        29B3<> 29D2< 38A3>
+3V_FW_ESD_ILIM   29D4< 38B3>
+3V_FW_LP         28D7<> 38A3>
+3V_GPU           12D1< 18B8< 18C5< 18C7< 18D6<
                  19C4< 19C6< 19C7< 19D7< 21A6< 21B1<
                  38C3>
+3V_GPU_FLT       21B2< 38C3>
+3V_GPU_SI        20C4< 20C8< 20D8<
+3V_HALL_EFFECT   23C6<> 38B6> 39C4>
+3V_INTREPID_USB  34C3< 38D3>
+3V_LCD           22B4<> 38B6>
+3V_LCD_SW        22A4<> 38B6>
+3V_MAIN          38D6>
+3V_NEC_VDD       26D7< 26D7< 38A3>
+3V_PMU           38D6> 39A2>
+3V_PMU_AVCC      25A4< 30B6< 30D5<> 38C6>
+3V_PMU_ESR       32A2< 38C6>
+3V_PMU_RESET     30B7< 34A3<>
+3V_SI_AVCC       20C7< 38B3>
+3V_SI_PLLVCC     20C7< 38B3>
+3V_SI_VCC        20C6< 38B3>
+3V_SLEEP         38D6>
+3V_SLEEP_NECK    21A5<> 38B3>
+3V_ATI_PLL       8D6< 12D4< 12D8< 14D6<> 38D3>
+3V_INTREPID_PLL1  14C4< 38D3>
+3V_INTREPID_PLL2  14D3< 38D3>
+3V_INTREPID_PLL3  14D3< 38D3>
+3V_INTREPID_PLL4  14D3< 38D3>
+3V_INTREPID_PLL5  12D3< 38D3>
+3V_INTREPID_PLL6  12D6< 38D3>
+3V_INTREPID_PLL7  8D5< 38D3>
+3V_INTREPID_PLL8  14D3< 38D3>
+3V_LDO           35D6< 38D6>
+3V_MAIN           38D6>
+3V_SLEEP_NECK    21A5<> 38B3>
+3V_SLEEP_VIN     35D8< 38D6>
+3V_MAIN           38D6>
+3V_SLEEP          38D6>
+3V_SOUND_SLEEP    38B6>
+5V_TPAD_SLEEP    23C7<> 38B6> 39C4>
+12_8V_INV        22B1< 38B6> 39A2>
+24V_PBUS         38D6> 39B2>
+ADAPTER          31D8<> 32B7< 38D6>
+ADAPTER_ILIM     32B6<> 38C6>
+ADAPTER_OR_BATT  32A5<> 38C6>
+ADAPTER_SENSE    31D5<> 38C6>
+ADAPTER_SW       31D6<> 38C6>
+BATT              38D6>
+BATT_14V_FUSE    31D1<> 38C6>
+BATT_24V_FUSE    31D2<> 38C6>
+BATT_POS         31A4<> 38C6> 39C3>
+BATT_RSNS        31B2> 38C6>
+BATT_VSNS        31A4> 38C6>
+FW_FUSE          29D7<> 38A3>
+FW_PWR_OR        28D6<> 29D5<> 38A3>
+FW_PWR_PORTA     29C5< 38A3>
+FW_SW            29D5<> 38A3>
+FW_VP9           29C2<> 38A3>
+FW_VP1           29A3<> 38A3>
+GPU_MCLK         21C7< 21D4< 38C3>
+GPU_MEM          18A6<> 18B8< 21B4< 21B7< 21C6<
                  21C8< 21D2< 38C3>
+GPU_MEMCORE      21C5< 38C3>
+GPU_VDD15_NECK   19B5<> 38B3>
+GPU_VDD15_UF     19B5<> 19D4<> 38C3>
+HD_LOGIC_SLEEP   24C2<> 38C6>
+PBUS              38D6> 39B2>
+VCC_CBUS_SW      17B1<> 17B2<> 17D2<> 38D3>
+VPP_CBUS_SW      17B1<> 17B2<> 17D2<> 38C3>
1V20_REF          31C7< 32C8< 38D1>
1V65_REF          31A5<>
1.5V_2.5V_OK      35C5> 38B1>
1.5V_BOOST        35C6<> 38C1>
1.5V_BST          35C5> 38C1>
1.5V_DH           35C5<> 38C1>
1.5V_DL           35B5<> 38C1>
1.5V_FB           35B5< 35B7< 38C1>
1.5V_ILIM         35C5<> 38C1>
1.5V_LX           35B6<> 38C1>
1.5V_SLEEP_EN_L   35C7<> 35D7<>
1.5V_SLEEP_PWREN_L  35A3<>
1.8V_SW           35A5<> 38A1>
1.8V_VFB          38A1>
2.5V_BOOST        35C4<> 38D1>
2.5V_BST          35C4<> 38D1>
2.5V_DH           35C4<> 38D1>
2.5V_DL           35B4<> 38D1>
2.5V_ILIM         35C5> 38C1>
2.5V_LX           35B4<> 38D1>
2.5V_SLEEP_PWREN_L  35C2<>
2_34V_REF         30A4<
3V_5V_OK          33B4<> 35A8<> 35D6<
3V_5V_OK_INV      35A8>
3V_B6             33C4>
3V_BOOST          33C4<>
3V_BOOST_ESR      33D3<>
3V_ITH            33C4<>
3V_ITH_RC         33C3<
3V_PMU_VTAP       32B3<
3V_RSNS           33D2< 38D1>
3V_RUNSS          33C4<
3V_SLEEP_PWREN_L  33A3<>

3V_SNSM           33C4< 37A2>
3V_SNSP           33C4< 37A2>
3V_SW             33C4< 38D1>
3V_TG             33D4<>
3V_VOSNS          33C4<>
5V_BG             33C5>>
5V_BOOST          33C5>>
5V_BOOST_ESR      33D5>
5V_HD_PWREN       33A8<>
5V_ITH            33C5>>
5V_ITH_RC         33C6<
5V_RSNS           33D7< 38D1>
5V_RUNSS          33C5<
5V_SLEEP_PWREN    33A8<>>
5V_SNSM           33C5< 37A2>
5V_SNSP           33C6< 37A2>
5V_SW             33C5>> 38D1>
5V_TG             33C5>>
5V_VOSNS          33C5>>
1625_BG           32C5>>
1625_BST          32C5<
1625_BST_ESR      32C5>>
1625_COMP         31D2< 32C6<
1625_DIV          32C8<
1625_ENABLE       32D7<>
1625_ENABLE_L     32D6>>
1625_EXTVCC       31D5> 38D1>
1625_FCB          32C6<
1625_INTVCC       32C5>> 38D1>
1625_RUNSS        32C6<
1625_SGND         32B7<> 38D1>
1625_TG           32C5>>
1625_VFB          32B5>>
1625_VIN          32C6< 38D1>
1625_VSW          32C4>> 38D1>
1772_ACIN         31B5<
1772_ACOK_L       31B5> 31C4<>
1772_BST          31B4>>
1772_BST_ESR      31C3<
1772_CCI          31B5>>
1772_CCS          31B5>>
1772_CCV          31B5>>
1772_CCV_RC       31B5<
1772_CELLS        31B4<
1772_CLS          31A4<
1772_CSIN         31B4<> 37A2>
1772_CSIP         31B4<> 37A2>
1772_CSSN         31C5< 37A2>
1772_CSSP         31C5< 37A2>
1772_DCIN         31B5< 38C6>
1772_DH           31B4>>
1772_DLO          31B4<>
1772_DRV          31B4> 38C6>
1772_GND          31A5> 38C6>
1772_ICHG         31B5<>
1772_ICTL         31B5>>
1772_IINP         31B5<
1772_LDO          31C4<> 38C6>
1772_LX           31B4> 38C6>
1772_REF          31B5>>
1772_VCTL         31B5<
1772_BG           19A5<> 38B1>
1778_BST          19A5> 38B1>
1778_BST_RC       19A4<> 38B1>
1778_FCB          19A5> 38B1>
1778_GND          19A5> 19A6< 38B1>
1778_ION          19A5> 38B1>
1778_ITH          19A5> 38B1>
1778_ITH_RC       19A7< 38B1>
1778_SHDN_L       19A6<
1778_SHDN_L_D3COLD  19A7<>
1778_TG           19A5<> 38B1>
1778_VCC          19A5> 38B1>
1778_VFB          19A2< 19A5< 38B1> 39A1>
1778_VIN          19A5< 38B1>
1778_VRNG         19A5< 38B1>
3485_MODE         27D5<
3485_VFB          27D4<>
3485_FCB          32C5<
3707_FSET         33C5<
3707_INTVCC       33D4< 38D1>
3707_SGND         33B5> 38D1>
3707_STBY         33C5<>
A29_CLS_ADJ       31A5<>
A29_CURRENT_ADJ   31C4<>
A29_DETECT        30A2< 31A5<> 31C4<>
A29_DET_L         30A2<
A29_EN            34A6<>
AB_SEL_LOW        34A6<>
AC_DIV            31C8<
AC_ENABLE_GATE    31D6<>
AC_ENABLE_L       31C6<>
AC_STR_18V        31C4<>
AC_IN             27B8<> 29C7< 30B3< 31C5<> 31C7<>
AC_IN_FW_CNTL     29C7<>
AC_IN_L           32C5<> 31C6<>
AC_IN_L_RC        31C2<>
ADAPTER_DET       30A4< 31D8<> 39C2>
ADAPTER_I_REG     31D3<>
ADT7468_ADR_EN_L  25B3<>
ADT7468_FAN1_PWM  25B3<>
ADT7468_FAN2_PWM  25B3<>
ADT7468_THERM     25A5<> 25B3<>
ADT7468_VCC       25B4<>
ADT7468_VCORE_MON  5C8<> 25B4<>
AGPIX_DET_PU      18C4<>
AGP_AD<0>         12D2<> 18C7<>
AGP_AD<15..0>     37D5>
AGP_AD<1>         12C2<> 18C7<>
AGP_AD<2>         12C2<> 18C7<>
AGP_AD<3>         12C2<> 18C7<>
AGP_AD<4>         12C2<> 18C7<>
AGP_AD<5>         12C2<> 18C7<>
AGP_AD<6>         12C2<> 18C7<>
AGP_AD<7>         12C2<> 18C7<>
AGP_AD<8>         12C2<> 18C7<>
AGP_AD<9>         12C2<> 18C7<>
AGP_AD<10>        12C2<> 18C7<>
AGP_AD<11>        12C2<> 18C7<>
AGP_AD<12>        12C2<> 18C7<>
AGP_AD<13>        12C2<> 18C7<>
AGP_AD<14>        12C2<> 18C7<>
AGP_AD<15>        12C2<> 18C7<>
AGP_AD<16>        12C2<> 18C7<>
AGP_AD<31..16>    37D5>
AGP_AD<17>        12C2<> 18C7<>
AGP_AD<18>        12C2<> 18C7<>
AGP_AD<19>        12C2<> 18C7<>
AGP_AD<20>        12C2<> 18C7<>
AGP_AD<21>        12C2<> 18C7<>
AGP_AD<22>        12C2<> 18C7<>
AGP_AD<23>        12C2<> 18C7<>
AGP_AD<24>        12C2<> 18C7<>
AGP_AD<25>        12C2<> 18C7<>
AGP_AD<26>        12C2<> 18C7<>
AGP_AD<27>        12B2<> 18D7<>
AGP_AD<28>        12B2<> 18D7<>
AGP_AD<29>        12B2<> 18D7<>
AGP_AD<30>        12B2<> 18D7<>
AGP_AD<31>        12B2<> 18D7<>
AGP_AD_STB<0>     12A2<> 12B2<> 18D6<> 37D5>
AGP_AD_STB<1>     12A2<> 12B2<> 18D6<> 37D5>
AGP_AD_STB_L<0>   12A2<> 12B2<> 18D6<> 37D5>
AGP_AD_STB_L<1>   12A2<> 12A2<> 18D6<> 37D5>
AGP_ATI_RESET_L   18B7<
AGP_ATI_VREF      18B7<
AGP_ATI_VREFD     18B7<
AGP_BUSY_L        12A2<> 12D2< 18D6>
AGP_CBE<0>        12B2<> 18B7<>
AGP_CBE<1..0>     37D5>
AGP_CBE<1>        12B2<> 18B7<>
AGP_CBE<2>        12B2<> 18B7<>
AGP_CBE<3..2>     37D5>
AGP_CBE<3>        12B2<> 18B7<>
AGP_DEVSEL_L      12B2<> 12C2< 18B7<> 37D5>
AGP_FRAME_L       12B2<> 12C2< 18B7<> 37D5>
AGP_GNT_L         12C2< 12D2> 18B7< 37D5>
AGP_INT_L         14B5<> 18B7<>
AGP_IRDY_L        12B2<> 12C2< 18B7<> 37D5>
AGP_PAR           12B2> 18B7> 37D5>
AGP_PIPE_L        12A2> 12B2<
AGP_RBF_L         12A2> 12C2< 18C6> 37D5>
AGP_REQ_L         12C2< 12D2> 18B7<> 37D5>
AGP_SBA<0>        12B2< 18C6>
AGP_SBA<7..0>     37D5>
AGP_SBA<1>        12B2> 18C6>
AGP_SBA<2>        12B2> 18C6>
AGP_SBA<3>        12B2> 18C6>
AGP_SBA<4>        12B2> 18C6>

AGP_SBA<5>        12B2<> 18C6>
AGP_SBA<6>        12B2> 18C6>
AGP_SBA<7>        12B2<> 18C6>
AGP_SB_STB        12B2> 12B2< 18C6<> 37D5>
AGP_SB_STB_L      12A2<> 12A2< 18C6<> 37D5>
AGP_ST<0>         12A2> 18C6<
AGP_ST<1>         12A2> 18C6<
AGP_ST<2>         12A2> 18C6<
AGP_STOP_L        12B2<> 12C2< 18B7<> 37D5>
AGP_STP_L         18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L        12B2> 12C2< 18B7<> 37D5>
AGP_WBF_L         12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L  24C6<> 39C1>
AIRPORT_IDSEL     24C5<> 39B1>
AIRPORT_PCI_DAT_L  12D7<> 24D6<> 39C4>
AIRPORT_PCI_INT_L  14B5<> 14D7< 24D5<> 39C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 24D6<> 39D4>
AIRPORT_PME_L_TP  24D6<>
AMP_CONTROL       25C5<> 25D5<>
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ATI_AGP_FBSKEW<1>  19C2< 19C7<>
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ATI_BUS_CFG<1>    19B2< 19C7<>
ATI_BUS_CFG<2>    19B2< 19C7<>
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ATI_CLK27M_OSC    18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU     18C6<>
ATI_DBI_LO_PU     18D6>
ATI_GPIO7_SPN     19C7<>
ATI_GPIO8_PD      19C7<>
ATI_GPIO9_SPN     19C7<>
ATI_GPIO10_SPN    19C7<>
ATI_GPIO11_SPN    19C7<>
ATI_GPIO12_SPN    19C7<>
ATI_GPIO13_SPN    19C7<>
ATI_HSYNC         19D5<> 22C8<
ATI_MEMTEST       18A6<>
ATI_MEMVMODE0     18A7<
ATI_MEMVMODE1     18A7<
ATI_OSC_OE        18D3<
ATI_PCI_BYP       21D6<>
ATI_R2SET         19D6<>
ATI_RSET          19D6<>
ATI_RSTB_MSK      18C6<>
ATI_SSCLK_IN      18B1< 18B7<>
ATI_SSCLK_LP      18B1<>
ATI_TESTEN        19B7<
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ATI_TMDS_CLKP     19B7> 20B4<
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ATI_TMDS_D0-2     19B7> 20A4<
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ATI_VSYNC         19D5<> 22C8<
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ATI_XICLK_SKEW<1>  19C2< 19C7<>
ATI_VREF          31B7<>
BATTV_LOW         31B6>
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BATT_24MBUS_EN    31C2> 38C2>
BATT_24V_GATE     31C1<>
BATT_CLK          31A4<> 39C3>
BATT_DATA         31A4<> 39C3>
BATT_DIV          31A5<
BATT_LOW          31A6<>
BATT_OK_L         31B6<>
BATT_NEG          31A4<> 38C6> 39C3>
BBANG_HRESET_L    23A4< 39C1> 39C1>
BBANG_JTAG_TCK    23B3< 23C4<>
BBANG_TCK_EN      23B3<
BCKFD_PROT_EN_L   31C6<>
BCKFD_PROT_GATE   31D6<>
BRIGHT_PWM        22A5<> 39A7>
BRIGHT_PWM_UF     22A2<>
BT_USB_DM         14B1< 24B2<> 37B2> 39B6>
BT_USB_DP         14B2< 24B2<> 37B2> 39B6>
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CHGND2            38A6>
CHGND3            38A6>
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CHGND5            38A6>
CHGND6            38A6>
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CLK10M_PMU_XOUT   30B6<
CLK10M_PMU_XOUT_UF  30B7<
CLK18M_INT_EXT    14A6<> 36B1>
CLK18M_INT_XIN    14A5< 36B1>
CLK18M_INT_XOUT   14A5<> 36B1>
CLK18M_XTAL_IN    14A5< 36B1>
CLK25M_ENET_XIN   27A7< 36B1>
CLK25M_ENET_XOUT  27A7<> 36B1>
CLK25M_XTAL_IN    27A7<>
CLK27M_GPU_XIN    36B1>
CLK27M_GPU_XOUT   36B1>
CLK27M_XTAL_IN    36B1>
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CLK32K_PMU_XOUT   30B3<>
CLK32K_PMU_XOUT_UF  30B3<>
CLK33M_AIRPORT    12D8< 24D5<> 36C1> 39B1>
CLK33M_AIRPORT_UF  12C7<> 36C1>
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CLK33M_CBUS_UF    12C7<> 36C1>
CLK33M_USB2       12C8< 26B7< 36C1>
CLK33M_USB2_UF    12C7<> 36C1>
CLK66M_AGP_15V_TP  12C4>
CLK66M_GPU_AGP    12C8< 18B7< 36C1>
CLK66M_GPU_AGP_UF  12C7<> 36C1>
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CLKENET_LINK_GTX  13C5<> 36A1>
CLKENET_LINK_RX   13D5< 27C8< 36B1>
CLKENET_LINK_TX   13D5< 27D8< 36A1>
CLKENET_PHY_GBE_REF  27C7<> 36B1>
CLKENET_PHY_GTX   13C6< 27C7< 36A1>
CLKENET_PHY_RX    27C7<> 36B1>
CLKENET_PHY_TX    27D7<> 36B1>
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CLKFW_LINK_PCLK   13C3<> 28C3< 36A1>
CLKFW_PHY_LCLK    13C2 28BB< 36A1>
CLKFW_PHY_PCLK    28B4> 28C3< 36A1>
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CLKLVDS_LP        19B5> 22A4< 37C2> 39B7>
CLKLVDS_UN        19B5> 22A4<> 37C2> 39B7>
CLKLVDS_UP        19B5> 22A4<> 37C2> 39A7>
COMM_DTR_L        14C2> 25D1<> 39B2>
COMM_GPIO_L       14C2<> 25D2<> 39C2>
COMM_RESET_L      14C5<> 25C4<> 39C4>
COMM_RING_DET_L   14B5> 14C7< 25C3<> 30C6<> 39C4>
COMM_RTS_L        14C2> 25D1<> 39B2>
COMM_RXD          14C2<> 25D1<> 39B2>
COMM_SHUTDOWN     14C5<> 25C4<> 39C4>
COMM_TRXC         14C2<> 25D2<> 39C2>
COMM_TXD_L        14C2<> 25D2<> 39C2>
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COMP_ENABLE       22C1<>
COMP_RC           32C6<
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CPU_AVDD_PG       5C3<>
CPU_AVDD_VIN      5C3<
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CPU_DATA<60>      6B8> 8B3< 8B4<>
CPU_DATA<61>      6B8> 8B3< 8B4<>
CPU_DATA<62>      6A8> 8B3< 8B4<>
CPU_DATA<63>      6A8> 8B3< 8B4<>
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CPU_DRDY_L        5C4> 8A4< 8C2< 36D5>
CPU_DRDY_L_UF     36D5>
CPU_DTI<0>        5C4< 8A4<>
CPU_DTI<0..2>     36D5>
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CPU_DTI<2>        5C4< 8A4<>
CPU_EDTI          5C4< 8C4<
CPU_EMODE0_L      5A4< 7A4<
CPU_EMODE1_L      5A4< 5C2<
CPU_GBL_L         5A7< 8B6< 36D5>
CPU_HIT_L         5A7> 8B6< 8D2< 36D5>
CPU_HRESET_INV    7A7<>
CPU_HREQ_L        5B4< 5C2< 7A5< 7A8< 23A2<> 39C8>
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CPU_LZTSTCLK      5B4< 5C2<
CPU_LSSD_MODE     5B4< 5C2<
CPU_MCP_L         5B4< 5D2<
CPU_M_DM          25A5< 25B6<
CPU_M_DP          25B6< 25B8<
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CPU_PLL_CFG<2>    5C4< 7D3<
CPU_PLL_CFG<3>    5C4< 7D3<
CPU_PLL_CFG<4>    5C4< 7D3<>
CPU_PLL_CFGEXT    7D4<>
CPU_PLL_FS00      7C4<
CPU_PLL_FS01      7C4<
CPU_PLL_FS10      7C4<
CPU_PLL_STOP_BASE  7C7<
CPU_PLL_STOP_OC   7C4<> 7C8<> 30B6<>
CPU_PMONIN_L      5A4< 5C2<
CPU_PULLDOWN      5A2< 5A4< 5A4< 5C7<>
CPU_PULLUP        5A4< 5A4< 5C2<
CPU_QACK_L        5A4< 8B6<> 36D5>
CPU_QREQ_L        5B4> 8B6< 8C2< 36D5>
CPU_SHD0_L        5A7<> 5D2<
CPU_SHD1_L        5A7<> 5D2<
CPU_SMI_L         5B4< 5C2< 39C4>>
CPU_SREQ_L        5B2> 5B4< 39C8>
CPU_SRWX_L        5A4< 5C2<
CPU_TA_L          5B4< 8A4<> 8D2< 36D5>
CPU_TBEN          5A4< 5C2< 8A4<>
CPU_TBST_L        5A7> 8B6<> 36D5>
CPU_TEA_L         5B4< 8A4<> 8C2< 36D5>
CPU_THERM_DM      6A6<> 25A6<
CPU_THERM_DP      6A6<> 25A6<
CPU_TSIZ<0>       5A7> 8B6<>
CPU_TSIZ<0..2>    36D5>
CPU_TSIZ<1>       5A7> 8B6<>
CPU_TSIZ<2>       5A7> 8B6<>
CPU_TS_L          5C7> 8D2< 8D6<> 36D5>
CPU_TT<0>         5A7> 8B6<>
CPU_TT<0..4>      36C5>
CPU_TT<1>         5A7> 8B6<>
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CPU_VCORE_HI_DC   7B6< 30D4<> 34C8< 34D7<
CPU_VCORE_PWR_SEQ  34D8<>
CPU_VCORE
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PCI_FRAME_L       12B7< 12C7<> 17B7<> 24C5<> 26B7<>
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PCI_IRDY_L        12B7< 12C7<> 17B7<> 24C6<> 26B7<>
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PCI_PAR           12C7<> 17B7<> 24C5<> 26B7<> 37C5>
                  39D4>
PCI_STOP_L        12A7< 12C7<> 17B7<> 24C5<> 26B7<>
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PCI_TRDY_L        12B7< 12C7<> 17A7<> 24C5<> 26B7<>
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PLL_STOP_L        7C4<> 7C8<>
PMU_ACK_L         14C2> 30C4<>
PMU_AC_DET        38A4< 38B4<>
PMU_AC_IN         30B4<>
PMU_BATT0_DET_L   30B4<>
PMU_BATT1_DET_L_PU  30B4<> 30D2<
PMU_BATT_DET_L    30B3< 30D2< 31A4<> 39C3>
PMU_BYTE          30B6< 30C7<
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PMU_CLK           14C2<> 30C4<>
PMU_CNVSS         30B6< 30C7<
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PMU_EPM           30D2< 30D4<>
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PMU_KB_RESET_L    30A6> 30B7< 39B2>
PMU_LID_CLOSED_L  23A8< 23C4<> 30B2< 30C4<>
PMU_NMI_BUTTON_L  25C1< 30C2< 30C4<>
PMU_NMI_L         30C2< 30C4<>
PMU_NUMLOCK_LED_L 30C6<>
PMU_OOPS          30B2< 30B4<>
PMU_PME_L         14B5<> 26B8< 30B2< 30C4<>
PMU_POWERUP_OK    30B4<> 30D2<
PMU_POWER_UP_L    29C7<> 30C6<> 30D7< 33B8<
PMU_REQ_L         14B7< 14C2> 30C4<>
PMU_RESET_BUTTON_L  25B1< 30C4<> 30D2<
PMU_RESET_L       30B6<>
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PMU_SLEEP_LED_L   23C2<> 30C4<>
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RAM_CKE<3>        9A3< 9C4< 11C3<>
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RAM_CS_L<3..0>    36A5>
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RAM_CS_L<2>       9C4< 11B3<>
RAM_CS_L<3>       9C4< 11B5<>
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RAM_DATA_A<7..0>  36C5>
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RAM_DATA_A<7>     10B8<> 11D6<>
RAM_DATA_A<8>     10B8<> 11D8<>
RAM_DATA_A<15..8>  36C5>
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RAM_DATA_A<10>    10C7<> 11D8<>
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RAM_DATA_A<14>    10C7<> 11D6<>
RAM_DATA_A<15>    10C7<> 11D6<>
RAM_DATA_A<16>    10C6<> 11D8<>
RAM_DATA_A<31..16>  36B5>
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RAM_DATA_A<47..32>  36B5>
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RAM_DATA_B<7..0>  36C5>
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RAM_DATA_B<8>     10C8<> 11D3<>
RAM_DATA_B<15..8>  36C5>
RAM_DATA_B<9>     10C8<> 11D3<>
RAM_DATA_B<10>    10C8<> 11D3<>
RAM_DATA_B<11>    10C8<> 11D3<>
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RAM_DATA_B<31..16>  36B5>
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RAM_DATA_B<18>    10C6<> 11C3<>
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RAM_DATA_B<21>    10C6<> 11C5<>
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RAM_DATA_B<31>    10C6<> 11C5<>
RAM_DATA_B<32>    10C4<> 11B3<>
RAM_DATA_B<47..32>  36B5>
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RAM_DATA_B<34>    10C4<> 11B3<>
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RAM_DATA_B<40>    10C4<> 11B3<>
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RAM_DATA_B<43>    10C4<> 11A3<>
RAM_DATA_B<44>    10C4<> 11A5<>
RAM_DATA_B<45>    10C4<> 11B5<>
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RAM_DATA_B<47>    10C4<> 11A5<>
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RAM_DATA_B<55..48>  36B5>
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RAM_DATA_B<56>    10C2<> 11A3<>
RAM_DATA_B<63..56>  36A5>
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RAM_DATA_B<58>    10C2<> 11A3<>
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RAM_DATA_B<63>    10C2<> 11A5<>
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RAM_DQM_A<2>      10B6<> 11C6<>
RAM_DQM_A<3..2>   36B5>
RAM_DQM_A<4>      10C5<> 11C6<>
RAM_DQM_A<5..4>   36B5>
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RAM_MUXSEL_L      10A3< 10A5< 10B5<> 10B7<> 36A5>
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RAM_WE_L          9A4< 11B3<> 11B8<> 36A5>
RF_DISABLE_L_SPN  24D6<> 39C1>
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RIGHT_USB_DP      26A3< 32A7<> 37A2> 39D1>
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RJ45_DP<0>        27B2<> 37D2> 39B3>
RJ45_DP<1>        27B2<> 37D2> 39B3>
RJ45_DP<2>        27B2<> 37D2> 39A3>
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ROM_OE_L          98A< 12A5< 24C5<> 39B1>
ROM_ONBOARD_CS_L  98A< 24C6<> 39B1>
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ROM_WP_L          9B3<
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RSDM4_TP          26C5>
RSDM5_TP          26C5>
RSDP3_TP          26C5>
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RSDP5_TP          26C5>
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SI_EDGE           20B7<
SI_MSEN           20B5<>
SI_PD             20B7<
SI_RST            20B7<
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SI_TMDS_CLKP      20B5<> 20C4<
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SLEEP_LED_L       23D1<
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SLEEP_LED_UF      23C1<
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SLEEP_L_LS5_INV   35A3< 35C2< 35C8<>
SLEEP_L_LS5_NET   33B3<> 35C8<>
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SLEEP_NET_INV     33A3<>
SMC_TP            26B5<
SND_AGND          25C7<> 38B6>
SND_AMP_MUTE      25C8< 25D6<> 39A4>
SND_AMP_MUTE_F    25C7< 25D6<>
SND_AMP_MUTE_L    14C5<> 25D5<>
SND_CLKOUT        14B1< 25D8< 36B1> 39D6>
SND_CLKOUT_F      25C7<> 25D7<
SND_HP_MUTE       25C5<>
SND_HP_MUTE_INV   25C5<> 25C6<> 39A4>
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SND_HW_RESET_L_F  25C6<> 25C7<
SND_LIN_SENSE_L   14B5<> 25D6<> 39C6>
SND_SCLK          14B1< 25C8< 36B1> 39C6>
SND_SCLK_F        25C7< 25D7<>
SND_SYNC          14B1< 25D8< 39D6>
SND_SYNC_F        25C7<> 25D7<
SND_TO_AUDIO      14B1< 25D8< 39D6>
SND_TO_AUDIO_F    25D6<> 25D7<
SOFT_PWR_ON_L     22D1< 23A8< 30A8< 30C6<> 30D7<
                  34A3<>
SRCLK_TP          26A5> 39A4>
SRMOD_TP          26A5< 39A4>
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ST7_KBD_LED_OUT   23A4< 23C4<>
ST7_OSC1          23D5<
ST7_OSC2          23D5<>
ST7_PB6_PD        23B2< 23C4<>
ST7_RESET_L       23D5<>
ST7_SENSOR4_SCK_PD  23B2< 23D4<>
ST7_SENSOR4_SDA_PD  23B2< 23D4<>
ST7_SENSOR5_SCK_PU  23B2< 23D4<>
ST7_SENSOR5_SDA_PU  23B2< 23D4<>
ST7_SLEEP_LED_H  23C2<> 23C4<>
ST7_XTAL_IN       23C5<
STOP_AGP_L        12D2< 12D4<>
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SUPPLY_M_DP       25B6< 25B8<
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SUTRO_ALS_OUT     23C4<> 24B2<> 39C2>
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SYSCLK_CPU_UF     8A6<> 36D1>
SYSCLK_DDRCLK_A0  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L  9D4< 11D8<> 36D1>
SYSCLK_DDRCLK_A0_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L  9D4< 11A6<> 36D1>
SYSCLK_DDRCLK_A1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_A1_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B0  9D4< 11D3<> 36D1>
SYSCLK_DDRCLK_B0_L  9C4< 11D3<> 36C1>
SYSCLK_DDRCLK_B0_L_UF  9B6<> 9C5< 36D1>
SYSCLK_DDRCLK_B0_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L  9D4< 11A5<> 36C1>
SYSCLK_DDRCLK_B1_L_UF  9B6<> 9D5< 36D1>
SYSCLK_DDRCLK_B1_UF  9B6<> 9D5< 36D1>
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THERM1_DP         25A5< 25A5< 25B5< 25B5<> 37A2>
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THERM1_M_DP       37A2>
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THERM2_A_DP       25A6< 25A8< 37A2>
THERM2_DM         25A5< 25B5< 25B5<> 37A2>
THERM2_DP         25A5< 25B5< 25B5<> 37A2>
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THERM2_M_DP       37A2>
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THERM_L_OC        25A4<> 30B4<>
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TMDS_CLKP         20B3< 20C2< 20C3< 22C7<> 37B2>
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TMDS_CONN_CLKP    22C6<> 22C7<> 37B2> 39D7>
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TMDS_CONN_DP<2>   22B6<> 22D5<>
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TMDS_DN<1>        20A3< 20B1< 20C3< 22B8<> 37B2>
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TMDS_DP<2>        20A2< 20A3< 20B3< 22B7<> 37B2>
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TPS2211_SHDN_L_PU  17C4<
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TV_COMP           22A6<> 39D6>
TV_GND1           22B6<> 38B6> 39A7>
TV_GND2           22A6<> 38B6> 39A7>
TV_Y              22A6<> 39D6>
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UIDE_DATA<15..8>  37C5>
UIDE_DATA<9>      13D7<> 24C4<
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UIDE_DATA<11>     13D7<> 24D4<
UIDE_DATA<12>     13D7<> 24B4<
UIDE_DATA<13>     13D7<> 24B4<
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UIDE_DATA<15>     13D7<> 24B4<
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UIDE_DIOW_L       13C7<> 24A4< 37C5>
UIDE_DMACK_L      13C7<> 24A4< 37C5>
UIDE_DMARQ        13C7<> 37C5>
UIDE_INTRQ        13C7< 37C5>
UIDE_IOCHRDY      13C7< 24A4< 37C5>
UIDE_REF          13C7<> 38D3>
UIDE_RST_L        13C7<> 24A4< 37C5>
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USB2_PCI_INT_L    14B5<> 14C7< 26A8<
USB2_PCI_REQ_L    12A7< 12D7<> 26B7>
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USB_D1P           14C1< 26A4< 26A5>
USB_D2M           14D1< 26A4< 26A5>
USB_D2P           14D1< 26A4< 26A5>
USB_DAM           14B2<> 14D2< 26A5>
USB_DAP           14B2<> 14D2< 26A5>
USB_DBM           14B2<> 14D2<
USB_DBP           14B2<> 14D2<
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USB_DCP           14B2<> 14C2< 26A5>
USB_DDM           14B2<> 14C2<
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USB_DEM           14B2< 14B2<> 37B2>
USB_DEP           14B2<> 14C2< 37B2>
USB_DFM           14B2< 14B2<> 37B2>
USB_DFP           14B2< 14B2<> 37B2>
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USB_OC_CD_L       14B2< 14C7<
USB_OC_EF_L       14B2< 14D7<
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USB_PWREN_CD_L    14B2<> 14C7<
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VCORE_BST         34C5<> 38C1>
VCORE_CC          34B6<> 38B1>
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*** Part Cross-Reference for the entire design ***

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XW3	SHORT	34
XW4	SHORT	32
XW5	SHORT	34
XW6	SHORT	35
XW7	SHORT	34
XW8	SHORT	33
XW9	SHORT	25
XW11	JUMPER	35
XW12	SHORT	22
XW13	SHORT	22
XW15	SHORT	34
XW19	SHORT	31
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	27
Y4	CRYSTAL	23
Y5	CRYSTAL	26
Y6	CRYSTAL	30
Y7	CRYSTAL_4PIN	30
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
ZT55	HOLE_VIA	4
ZT56	HOLE_VIA	4
ZT57	HOLE_VIA	4
ZT58	HOLE_VIA	4
ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4
ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MTGHOLE	4