1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
G		396923	PRODUCTION RELEASED	08/26/05	?

SCHEM,MLB,PB17"

08/25/2005

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1	TITLE PAGE AND CONTENTS
2	SYSTEM BLOCK DIAGRAM
3	POWER BLOCK DIAGRAM
4	PCB NOTES AND HOLES
5	MPC7450 MAXBUS INTERFACE
6	MPC7450 DATA
7	CPU PLL AND CONFIGURATION STRAPS
8	INTREPID MAXBUS AND BOOT STRAPS
9	INTREPID MEMORY INTERFACE / BOOT ROM
10	DDR MEMORY MUXES
11	200PIN DDR MEMORY SODIMM CONNECTORS
12	INTREPID AGP 4X/PCI
13	INTREPID ENET/FW/UATA/EIDE INTERFACES
14	INTREPID GPIOS/SERIAL/USB INTERFACES/SSCG
15	INTREPID POWER RAILS
16	INTREPID DECOUPLING
17	CARDBUS CONTROLLER (PCI1510)
18	M11 AGP & CLOCKS
19	M11 LVDS/TMDS/VGA/GPIO & GPU VCORE
20	SIL178 DUAL TMDS TRANSMITTER
21	M11 ANALOG, POWER, GND
22	VIDEO CONNECTORS - INVERTER, DVI, S-VIDEO DUAL-CHANNEL LVDS
23	LMU, LIGHT SENSOR, BOOTBANGER, SLEEP LED SPIDEY - KBD,TPAD,HALL EFFECT,PWR BUTTON
24	MMM, BATTERY CURRENT SENSE
25	INTERNAL CONNECTORS - DVD, CARDSLOT, HARD DRIVE, LEFT USB/BLUETOOTH
26	FAN CONTROLLER, MODEM, SOUND SERIAL DEBUG (JOLLY ROGER, PWR/NMI/RESET)
27	USB 2.0
28	MARVELL GIGABIT ETHERNET PHY
29	FIREWIRE A/B PHY
30	FIREWIRE A/B CONNECTORS, PORT POWER LIMITER
31	PMU (POWER MANAGEMENT UNIT)
32	BATTERY CHARGER AND CONNECTOR
33	12.8V SYSTEM POWER SUPPLY / PMU POWER SUPPLY
34	3.3V / 5V SYSTEM POWER SUPPLIES
35	CPU CORE VOLTAGE POWER SUPPLY
36	1.5V/ 1.8V / 2.5V SYSTEM POWER SUPPLIES
37	SIGNAL CONSTRAINTS (1 OF 3) - DIGITAL/CLK
38	SIGNAL CONSTRAINTS (2 OF 3) - DIGITAL/DIFF
39	SIGNAL CONSTRAINTS (3 OF 3) - POWER NETS
40	FUNCTIONAL TEST POINTS
41	REVISION HISTORY (1 OF 1)
42-45	SCHEMATIC CREF AND NETLIST REPORTS

BOM OPTIONS	STUFF	NO STUFF
D3_HOT		√
D3_COLD	√	
GPU_SS	√	
GPU_SWITCH	√	
SERIAL_DEBUG		√
VCORE_OFFSET	√	
1_8V_MAXBUS	√	
1_5V_MAXBUS		√
NEC_USB	√	
INTREPID_USB		√
BBANG		√
NO_BBANG		√
ATI_MEMIO_HI	√	
ATI_MEMIO_LO		√
SSCG		√
NO_SSCG	√	
5V_HD_LOGIC	√	
3V_HD_LOGIC		√
EXT_TMDS	√	
INT_TMDS		√
MMM	√	
INT_CLK	√	
EXT_CLK		√

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6694	1	SCHEM,MLB,PB17	SCH1	
820-1688	1	PCBF,MLB,PB17	PCB1	
826-4393	1	LABEL,PCB,28MM X 6MM	EEE:U3Y	LABEL_R15

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE NONE	

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

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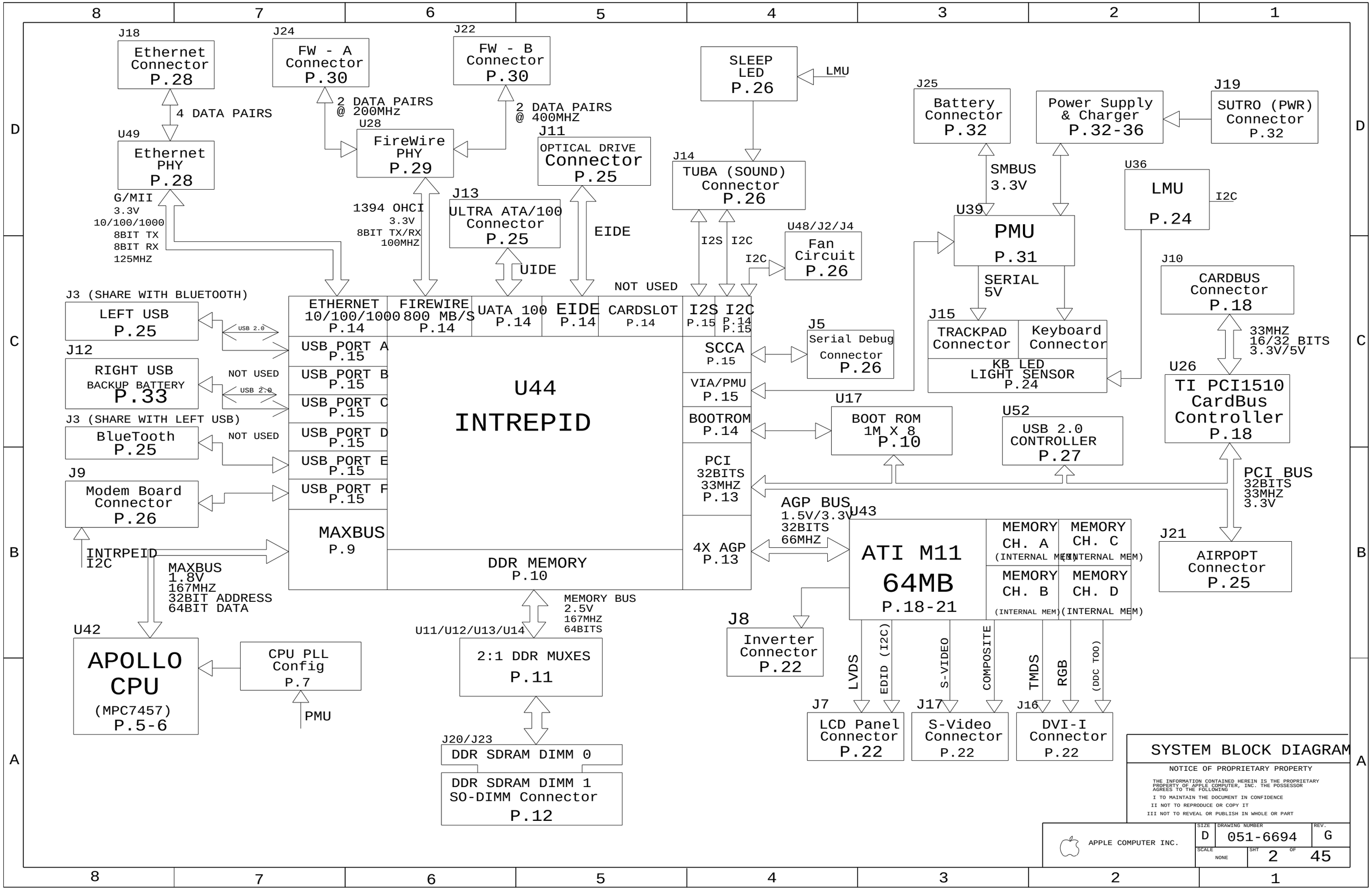
TITLE SCHEM,MLB,PB17"

DRAWING NUMBER 051-6694 REV. G


J18
Ethernet Connector P.28
4 DATA PAIRS
U49
Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ
J24
FW - A Connector P.30
2 DATA PAIRS @ 200MHz
U28
FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
100MHZ
J22
FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
J11
OPTICAL DRIVE Connector P.25
EIDE
J13
ULTRA ATA/100 Connector P.25
UIDE
SLEEP LED P.26
LMU
J14
TUBA (SOUND) Connector P.26
I2S
I2C
I2C
U48/J2/J4
Fan Circuit P.26
J25
Battery Connector P.32
Power Supply & Charger P.32-36
J19
SUTRO (PWR) Connector P.32
SMBUS
3.3V
U36
LMU P.24
I2C
U39
PMU P.31
SERIAL
5V
J10
CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
NOT USED
J3 (SHARE WITH BLUETOOTH)
LEFT USB P.25
USB 2.0
J12
RIGHT USB BACKUP BATTERY P.33
NOT USED
USB 2.0
J3 (SHARE WITH LEFT USB)
BlueTooth P.25
NOT USED
J9
Modem Board Connector P.26
INTRPEID
I2C
MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA
ETHERNET 10/100/1000 P.14
FIREWIRE 800 MB/S P.14
UATA 100 P.14
EIDE P.14
CARDSLOT P.14
I2S P.15
I2C P.14 P.15
USB PORT A P.15
USB PORT B P.15
USB PORT C P.15
USB PORT D P.15
USB PORT E P.15
USB PORT F P.15
MAXBUS P.9
U44
INTREPID
SCCA P.15
VIA/PMU P.15
BOOTROM P.14
PCI 32BITS 33MHZ P.13
4X AGP P.13
DDR MEMORY P.10
J5
Serial Debug Connector P.26
J15
TRACKPAD Connector
Keyboard Connector
KB LED
LIGHT SENSOR P.24
U26
TI PCI1510 CardBus Controller P.18
U17
BOOT ROM 1M X 8 P.10
U52
USB 2.0 CONTROLLER P.27
PCI BUS
32BITS
33MHZ
3.3V
AGP BUS
1.5V/3.3V
32BITS
66MHZ
U43
ATI M11 64MB P.18-21
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)
J21
AIRPOPT Connector P.25
MEMORY BUS
2.5V
167MHZ
64BITS
U11/U12/U13/U14
2:1 DDR MUXES P.11
J8
Inverter Connector P.22
U42
APOLLO CPU (MPC7457) P.5-6
CPU PLL Config P.7
PMU
LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS
RGB
(DDC TOO)
J7
LCD Panel Connector P.22
J17
S-Video Connector P.22
J16
DVI-I Connector P.22
J20/J23
DDR SDRAM DIMM 0
DDR SDRAM DIMM 1
SO-DIMM Connector P.12
SYSTEM BLOCK DIAGRAM
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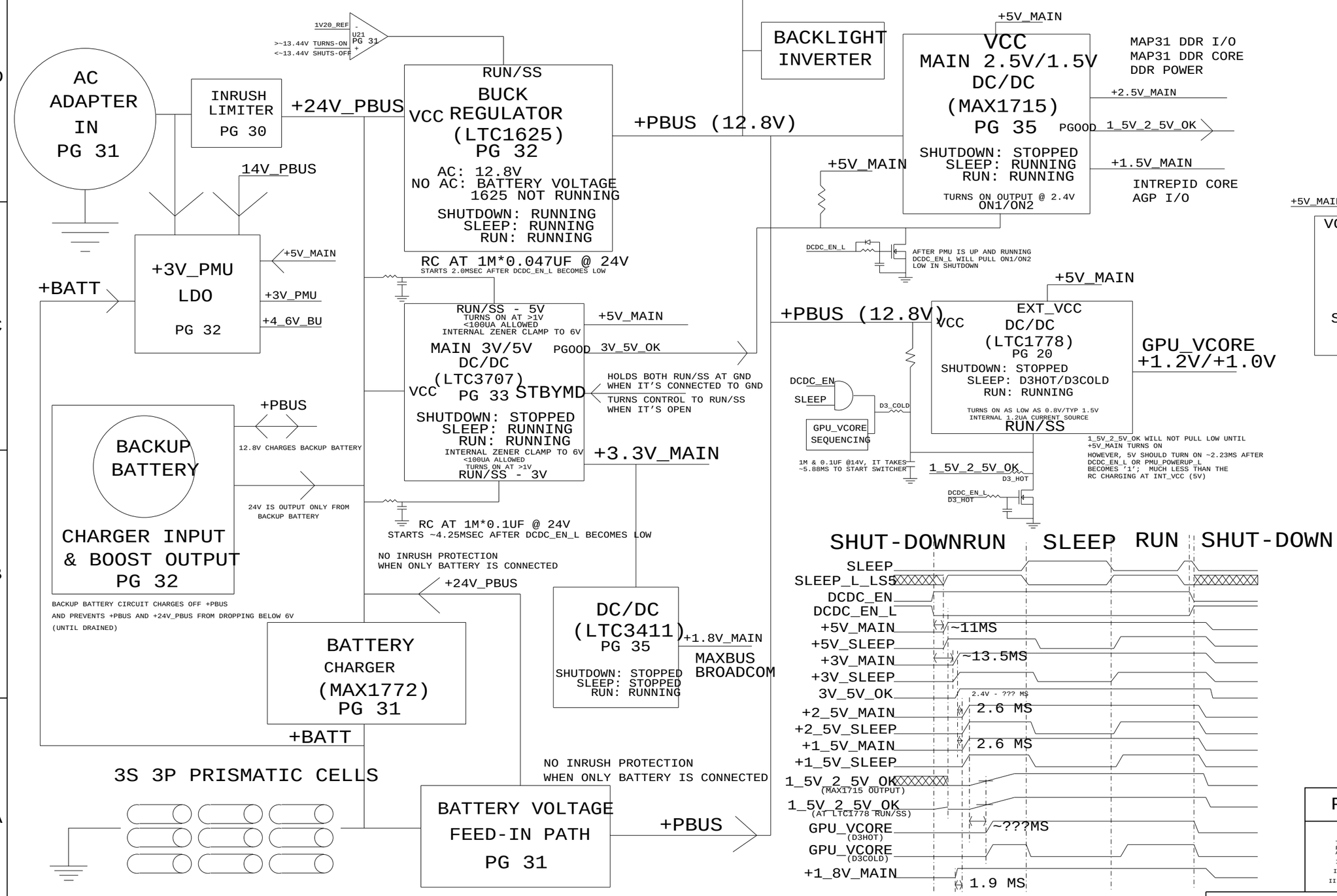
SIZE D
DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 2 OF 45

POWER SYSTEM ARCHITECTURE



POWER BLOCK DIAGRAM

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE NONE | SHT 3 OF 45

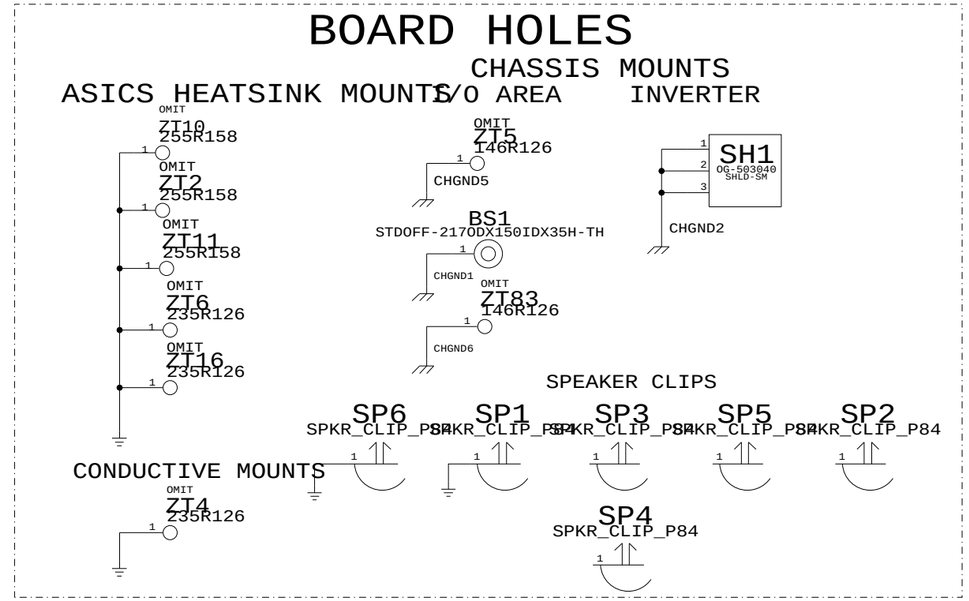
PCB SPECS

THICKNESS : 1.2 MM / 0.047 IN
1/2 OZ CU THICKNESS: 0.7 MILS
1.0 OZ CU THICKNESS: 1.4 MILS

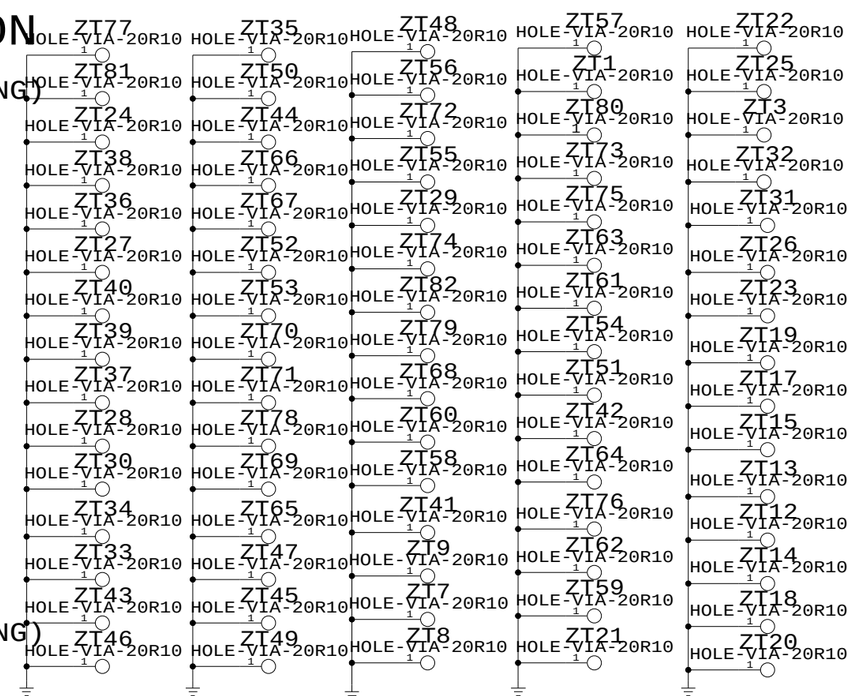
IMPEDANCE : 50 OHMS +/- 10%
DIELECTRIC: FR-4
LAYER COUNT: 12
SIGNAL TRACE WIDTH: 4 MILS
SIGNAL TRACE SPACING: 4 MILS
PREPREG THICKNESS: 2-3 MILS

SEE PCB CAD FILES FOR MORE SPECIFIC INFO.

BOARD HOLES



GROUND VIAS



BOARD STACK-UP AND CONSTRUCTION

20R10 TH VIA OR VIA IN PAD

1		SIGNAL (1/3 OZ + COPPER PLATING)
2	PREPREG (3MIL)	GROUND (1/2 OZ)
3	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
4	PREPREG (3MIL)	SIGNAL (1/2 OZ)
5	LAMINATE (4MIL)	GROUND (1/2 OZ)
6	PREPREG (2MIL)	CUT POWER PLANE(1 OZ)
7	LAMINATE (3MIL)	CUT POWER PLANE(1 OZ)
8	PREPREG (2MIL)	GROUND (1/2 OZ)
9	LAMINATE (4MIL)	SIGNAL (1/2 OZ)
10	PREPREG (3MIL)	SIGNAL (1/2 OZ)
11	LAMINATE (4MIL)	GROUND (1/2 OZ)
12	PREPREG (3MIL)	SIGNAL (1/3 OZ + COPPER PLATING)

BOARD INFORMATION

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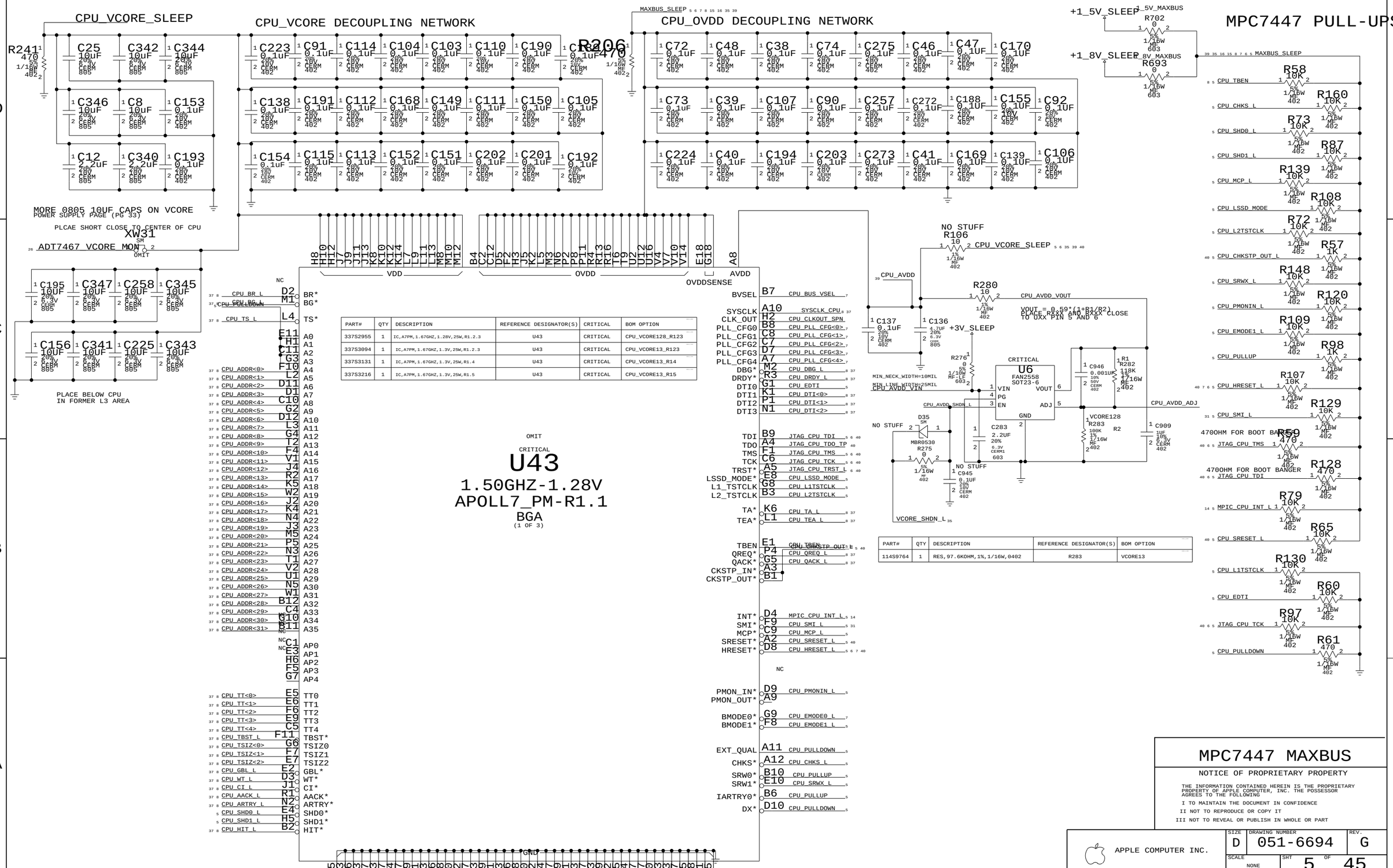
SCALE NONE	SHT 4 OF 45	



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
337S2955	1	IC,A7PM,1.67GHZ,1.28V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE128_R123
337S3094	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.2.3	U43	CRITICAL	CPU_VCORE13_R123
337S3131	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.4	U43	CRITICAL	CPU_VCORE13_R14
337S3216	1	IC,A7PM,1.67GHZ,1.3V,25W,R1.5	U43	CRITICAL	CPU_VCORE13_R15

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S9764	1	RES,97.6KOHM,1%,1/16W,0402	R283	VCORE13

MPC7447 MAXBUS

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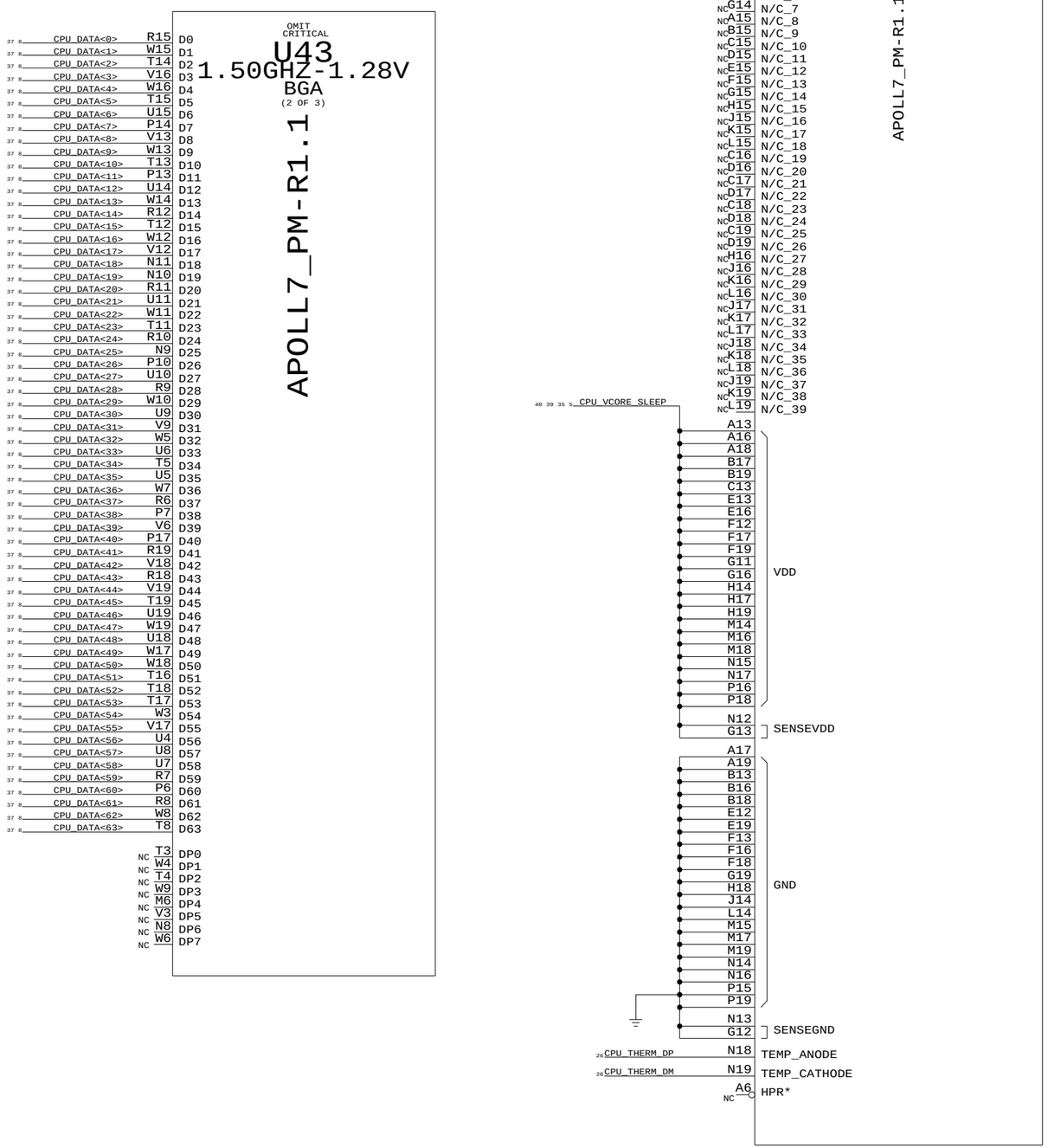
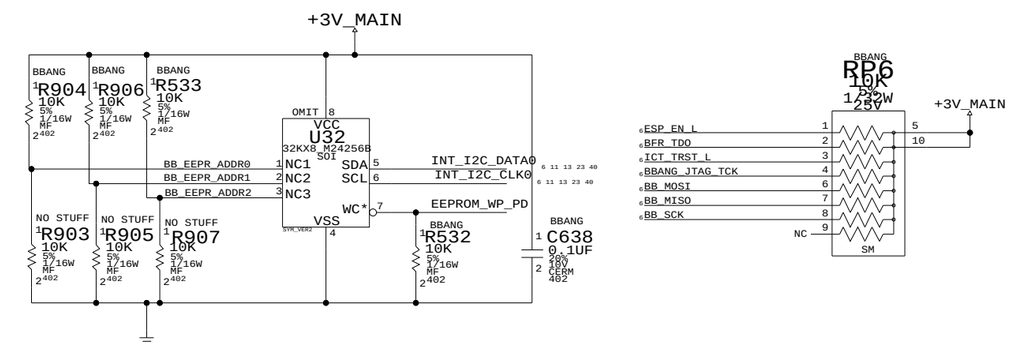
D	051-6694	G

SCALE NONE

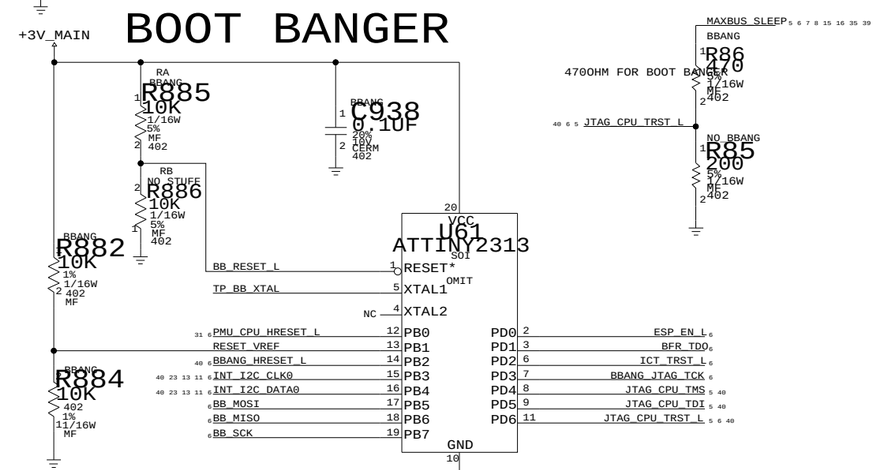
SHT 5 OF 45



BOOT BANGER E2PROM

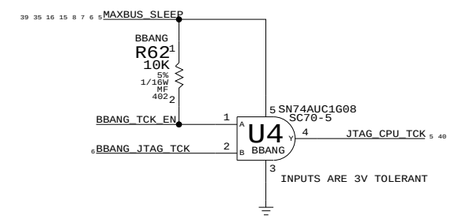


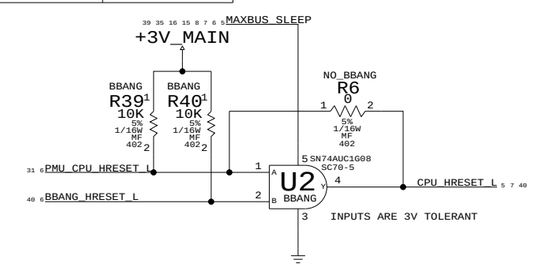
BOOT BANGER



UNSTUFFING RA AND STUFFING RB
WILL DISABLE THE CONTROLLER

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1660	1	MCU,PROGRAMMED W/ BANGER	U61	BBANG
341S1661	1	I2C EEPROM,PROGRAMMED W/ BANGER	U32	BBANG





BOOT BANGING SIGNAL DEFINITION

1/ BBANG_HRESET_L (OPEN COLLECTOR OUTPUT - 10K PULLUP ON MLB)
2/ PMU_HRESET_L (3V INPUT INTO LMU)
3/ BBANG_JTAG_TCK (REGULAR OUTPUT)
4/ JTAG_CPU_TMS (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
5/ JTAG_CPU_TDI (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)
6/ JTAG_CPU_TRST_L (OPEN COLLECTOR OUTPUT - 470OHM PULLUP ON MLB)

MPC7447/BBANG

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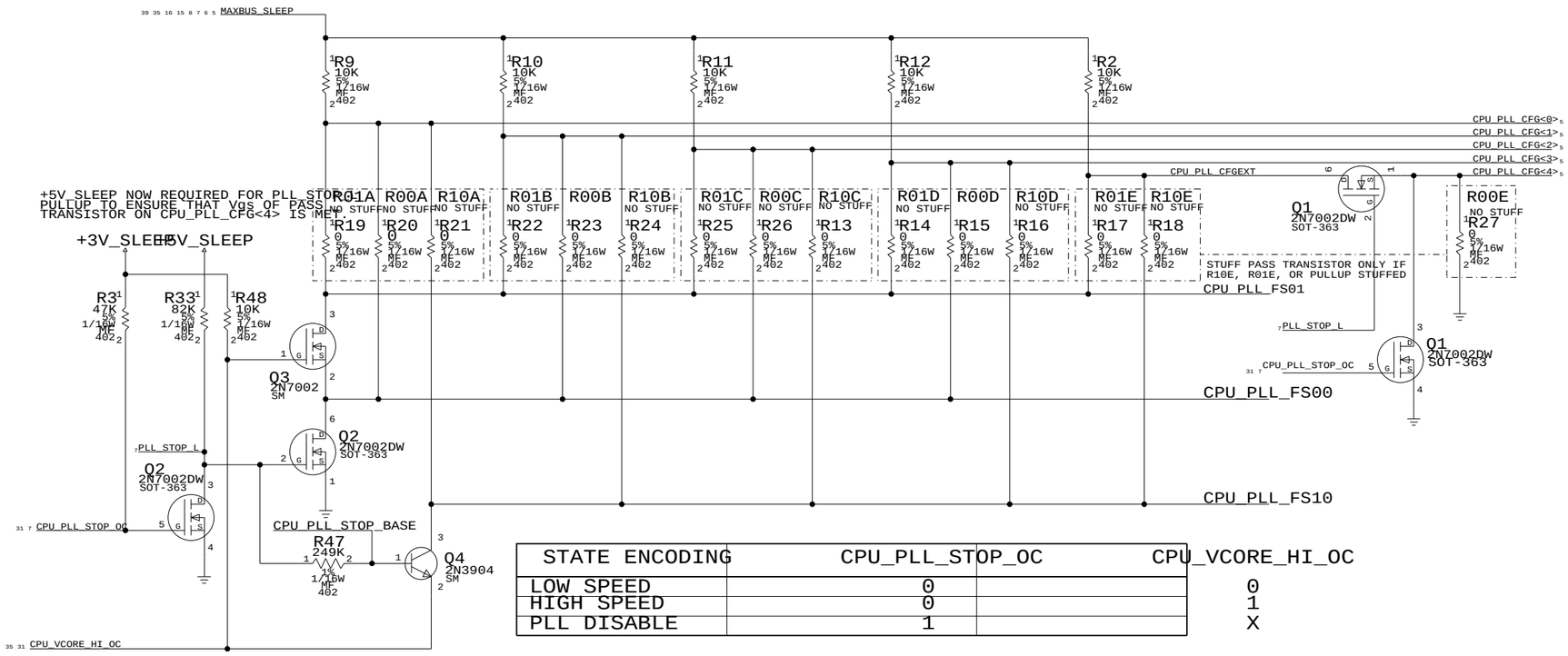
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE NONE	SHT 6 OF 45	

CPU PLL CONFIG CIRCUITRY



STATE ENCODING	CPU_PLL_STOP_OC	CPU_VCORE_HI_OC
LOW SPEED	0	0
HIGH SPEED	0	1
PLL DISABLE	1	X

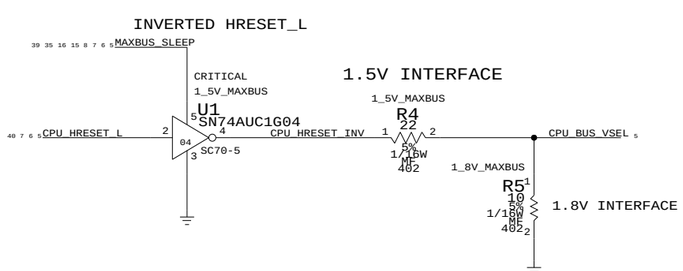
CPU FREQUENCY CONFIGURATION

APOLLO 7

MULTIPLIER (Bus-to-Core)	CORE FREQUENCY (AT BUS FREQUENCY) 167MHZ (MHZ)	133MHZ	CPU_PLL_CFG 4 E	0123 ABCD HEX
0.0X	PLL OFF		0	1111 0F
1.0X	PLL BYPASS		0	0011 03
2.0X	333	267	0	0100 04
3.0X	500	400	0	1000 08
4.0X	667	533	0	1010 0A
5.0X	833	667	0	1011 0B
5.5X	917	733	0	1001 09
6.0X	1000	800	0	1101 0D
6.5X	1083	867	0	0101 05
7.0X	1167	933	0	0010 02
7.5X	1250	1000	0	0001 01
8.0X	1333	1067	0	1100 0C
8.5X	1417	1133	0	0110 06
9.0X	1500	1200	1	0111 17
9.5X	1583	1267	0	0111 07
10.0X	1667	1333	1	1010 1A
10.5X	1750	1400	1	1000 18
11.0X	1833	1467	1	1001 19
11.5X	1917	1533	0	0000 00
12.0X	2000	1600	1	1011 1B
12.5X	2083	1667	1	1111 1F
13.0X	2167	1733	1	0101 15
13.5X	2250	1800	0	1110 0E
14.0X	2333	1867	1	1100 1C
15.0X	2500	2000	1	0001 11
16.0X	2667	2133	1	1101 1D
17.0X	2833	2267	1	0000 10
18.0X	3000	2400	1	0010 12
20.0X	3333	2667	1	0011 13
21.0X	3500	2800	1	0100 14
24.0X	4000	3200	1	0110 16
28.0X	4667	3733	1	1110 1E

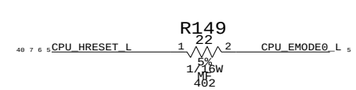
CPU CONFIGURATION

MAXBUS VSEL



DESKTOP HAD PROBLEM USING INVERTER TO INVERT HRESET_L NEED TO CHARACTERIZE

BUSTYPE SELECT



APOLLO ONLY SUPPORTS MAXBUS

SIGNAL	TIED	APPLICATION
CPU_EMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE
CPU_BUS_VSEL (PROCESSOR)	CPU_HRESET_L	2.5V INTERFACE
	LOW	1.8V INTERFACE
	CPU_HRESET_INV	1.5V INTERFACE

CPU CONFIGURATION

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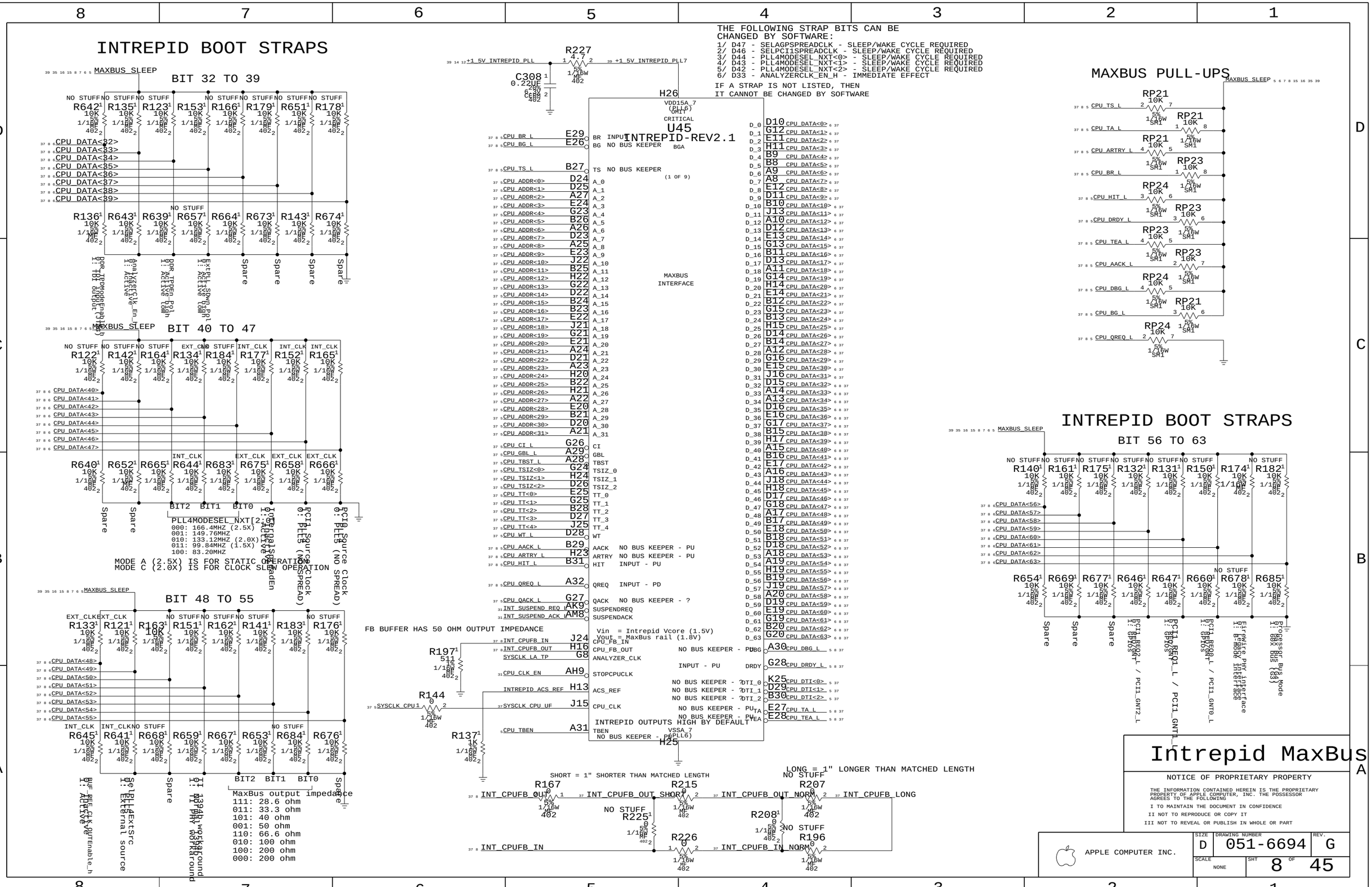
SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE NONE	SHT 7 OF 45	


INTREPID BOOT STRAPS
BIT 32 TO 39
MAXBUS_SLEEP
NO STUFF
R642 R135 R123 R153 R166 R179 R651 R178
CPU_DATA<32>
CPU_DATA<33>
CPU_DATA<34>
CPU_DATA<35>
CPU_DATA<36>
CPU_DATA<37>
CPU_DATA<38>
CPU_DATA<39>
R136 R643 R639 R657 R664 R673 R143 R674
Spare
Spare
Spare
Spare
BIT 40 TO 47
R122 R142 R164 R134 R184 R177 R152 R165
EXT_CLK
INT_CLK
CPU_DATA<40>
CPU_DATA<41>
CPU_DATA<42>
CPU_DATA<43>
CPU_DATA<44>
CPU_DATA<45>
CPU_DATA<46>
CPU_DATA<47>
R640 R652 R665 R644 R683 R675 R658 R666
Spare
Spare
BIT2 BIT1 BIT0
PLL4MODESEL_NXT[2:0]
000: 166.4MHZ (2.5X)
001: 149.76MHZ
010: 133.12MHZ (2.0X)
011: 99.84MHZ (1.5X)
100: 83.20MHZ
MODE A (2.5X) IS FOR STATIC OPERATION
MODE C (2.0X) IS FOR CLOCK SLEW OPERATION
BIT 48 TO 55
R133 R121 R163 R151 R162 R141 R183 R176
CPU_DATA<48>
CPU_DATA<49>
CPU_DATA<50>
CPU_DATA<51>
CPU_DATA<52>
CPU_DATA<53>
CPU_DATA<54>
CPU_DATA<55>
R645 R641 R668 R659 R667 R653 R684 R676
Spare
BIT2 BIT1 BIT0
MaxBus output impedance
111: 28.6 ohm
011: 33.3 ohm
101: 40 ohm
001: 50 ohm
110: 66.6 ohm
010: 100 ohm
100: 200 ohm
000: 200 ohm
THE FOLLOWING STRAP BITS CAN BE
CHANGED BY SOFTWARE:
1/ D47 - SELAGPSPREADCLK - SLEEP/WAKE CYCLE REQUIRED
2/ D46 - SELPCI1SPREADCLK - SLEEP/WAKE CYCLE REQUIRED
3/ D44 - PLL4MODESEL_NXT<0> - SLEEP/WAKE CYCLE REQUIRED
4/ D43 - PLL4MODESEL_NXT<1> - SLEEP/WAKE CYCLE REQUIRED
5/ D42 - PLL4MODESEL_NXT<2> - SLEEP/WAKE CYCLE REQUIRED
6/ D33 - ANALYZERCLK_EN_H - IMMEDIATE EFFECT
IF A STRAP IS NOT LISTED, THEN
IT CANNOT BE CHANGED BY SOFTWARE
R227 4.7
+1.5V_INTREPID_PLL
+1.5V_INTREPID_PLL7
C308 0.22UF
H26
VDD15A_7 (PLL6)
OMIT
CRITICAL
U45
INTREPID-REV2.1
BGA
(1 OF 9)
BR INPUT
BG NO BUS KEEPER
TS NO BUS KEEPER
MAXBUS INTERFACE
CPU_BR_L E29
CPU_BG_L E26
CPU_TS_L B27
CPU_ADDR<0> D24
CPU_ADDR<1> D25
CPU_ADDR<2> A27
CPU_ADDR<3> E24
CPU_ADDR<4> G23
CPU_ADDR<5> B26
CPU_ADDR<6> A26
CPU_ADDR<7> D23
CPU_ADDR<8> A25
CPU_ADDR<9> E23
CPU_ADDR<10> J22
CPU_ADDR<11> B25
CPU_ADDR<12> H22
CPU_ADDR<13> G22
CPU_ADDR<14> D22
CPU_ADDR<15> B24
CPU_ADDR<16> B23
CPU_ADDR<17> E22
CPU_ADDR<18> J21
CPU_ADDR<19> G21
CPU_ADDR<20> E21
CPU_ADDR<21> A24
CPU_ADDR<22> D21
CPU_ADDR<23> A23
CPU_ADDR<24> H20
CPU_ADDR<25> B22
CPU_ADDR<26> H21
CPU_ADDR<27> A22
CPU_ADDR<28> E20
CPU_ADDR<29> B21
CPU_ADDR<30> D20
CPU_ADDR<31> A21
CPU_CI_L G26
CPU_GBL_L A29
CPU_TBST_L A28
CPU_TSIZ<0> G24
CPU_TSIZ<1> H24
CPU_TSIZ<2> D26
CPU_TT<0> E25
CPU_TT<1> G25
CPU_TT<2> B28
CPU_TT<3> D27
CPU_TT<4> J25
CPU_WT_L D28
CPU_AACK_L B29
CPU_ARTRY_L H23
CPU_HIT_L B31
CPU_QREQ_L A32
CPU_QACK_L G27
INT_SUSPEND_REQ_L AK9
INT_SUSPEND_ACK_L AM8
CI
GBL
TBST
TSIZ_0
TSIZ_1
TSIZ_2
TT_0
TT_1
TT_2
TT_3
TT_4
WT
AACK NO BUS KEEPER - PU
ARTRY NO BUS KEEPER - PU
HIT INPUT - PU
QREQ INPUT - PD
QACK NO BUS KEEPER - ?
SUSPENDREQ
SUSPENDACK
Vin = Intrepid Vcore (1.5V)
Vout = MaxBus rail (1.8V)
FB BUFFER HAS 50 OHM OUTPUT IMPEDANCE
INT_CPUFB_IN J24
INT_CPUFB_OUT H16
SYSCLK_LA_TP G8
CPU_CLK_EN AH9
INTREPID_ACS_REF H13
SYSCLK_CPU_UF J15
CPU_TBEN A31
CPU_FB_IN
CPU_FB_OUT NO BUS KEEPER - PU
ANALYZER_CLK
INPUT - PU
STOPCPUCLK
ACS_REF NO BUS KEEPER - ?
CPU_CLK NO BUS KEEPER - PU
NO BUS KEEPER - PU
INTREPID OUTPUTS HIGH BY DEFAULT
TBEN NO BUS KEEPER - PU
VSSA_7 (PLL6)
H25
R197 511
R144 0
R137 1K
D_0 D10 CPU_DATA<0>
D_1 G12 CPU_DATA<1>
D_2 E11 CPU_DATA<2>
D_3 H11 CPU_DATA<3>
D_4 B9 CPU_DATA<4>
D_5 B8 CPU_DATA<5>
D_6 A9 CPU_DATA<6>
D_7 A8 CPU_DATA<7>
D_8 E12 CPU_DATA<8>
D_9 D11 CPU_DATA<9>
D_10 B10 CPU_DATA<10>
D_11 J13 CPU_DATA<11>
D_12 A10 CPU_DATA<12>
D_13 D12 CPU_DATA<13>
D_14 E13 CPU_DATA<14>
D_15 G13 CPU_DATA<15>
D_16 B11 CPU_DATA<16>
D_17 D13 CPU_DATA<17>
D_18 A11 CPU_DATA<18>
D_19 G14 CPU_DATA<19>
D_20 H14 CPU_DATA<20>
D_21 E14 CPU_DATA<21>
D_22 B12 CPU_DATA<22>
D_23 G15 CPU_DATA<23>
D_24 B13 CPU_DATA<24>
D_25 H15 CPU_DATA<25>
D_26 D14 CPU_DATA<26>
D_27 B14 CPU_DATA<27>
D_28 A12 CPU_DATA<28>
D_29 G16 CPU_DATA<29>
D_30 E15 CPU_DATA<30>
D_31 J16 CPU_DATA<31>
D_32 D15 CPU_DATA<32>
D_33 A14 CPU_DATA<33>
D_34 A13 CPU_DATA<34>
D_35 D16 CPU_DATA<35>
D_36 E16 CPU_DATA<36>
D_37 G17 CPU_DATA<37>
D_38 B15 CPU_DATA<38>
D_39 H17 CPU_DATA<39>
D_40 A15 CPU_DATA<40>
D_41 B16 CPU_DATA<41>
D_42 E17 CPU_DATA<42>
D_43 A16 CPU_DATA<43>
D_44 J18 CPU_DATA<44>
D_45 H18 CPU_DATA<45>
D_46 D17 CPU_DATA<46>
D_47 G18 CPU_DATA<47>
D_48 A17 CPU_DATA<48>
D_49 B17 CPU_DATA<49>
D_50 E18 CPU_DATA<50>
D_51 B18 CPU_DATA<51>
D_52 D18 CPU_DATA<52>
D_53 A18 CPU_DATA<53>
D_54 A19 CPU_DATA<54>
D_55 H19 CPU_DATA<55>
D_56 B19 CPU_DATA<56>
D_57 J19 CPU_DATA<57>
D_58 A20 CPU_DATA<58>
D_59 D19 CPU_DATA<59>
D_60 E19 CPU_DATA<60>
D_61 G19 CPU_DATA<61>
D_62 B20 CPU_DATA<62>
D_63 G20 CPU_DATA<63>
DBG A30 CPU_DBG_L
DRDY G28 CPU_DRDY_L
DTI_0 K25 CPU_DTI<0>
DTI_1 D29 CPU_DTI<1>
DTI_2 B30 CPU_DTI<2>
TA E27 CPU_TA_L
TEA E28 CPU_TEA_L
MAXBUS PULL-UPS
RP21 10K CPU_TS_L
RP21 10K CPU_TA_L
RP21 10K CPU_ARTRY_L
RP23 10K CPU_BR_L
RP24 10K CPU_HIT_L
RP23 10K CPU_DRDY_L
RP23 10K CPU_TEA_L
RP23 10K CPU_AACK_L
RP24 10K CPU_DBG_L
RP21 10K CPU_BG_L
RP24 10K CPU_QREQ_L
INTREPID BOOT STRAPS
BIT 56 TO 63
R140 R161 R175 R132 R131 R150 R174 R182
CPU_DATA<56>
CPU_DATA<57>
CPU_DATA<58>
CPU_DATA<59>
CPU_DATA<60>
CPU_DATA<61>
CPU_DATA<62>
CPU_DATA<63>
R654 R669 R677 R646 R647 R660 R678 R685
Spare
Spare
Spare
SHORT = 1" SHORTER THAN MATCHED LENGTH
LONG = 1" LONGER THAN MATCHED LENGTH
R167 0
INT_CPUFB_OUT
INT_CPUFB_OUT_SHORT
R215 0
INT_CPUFB_OUT_NORM
R207 0
INT_CPUFB_LONG
NO STUFF
R225 0
R226 0
INT_CPUFB_IN
R208 0
R196 0
INT_CPUFB_IN_NORM
Intrepid MaxBus
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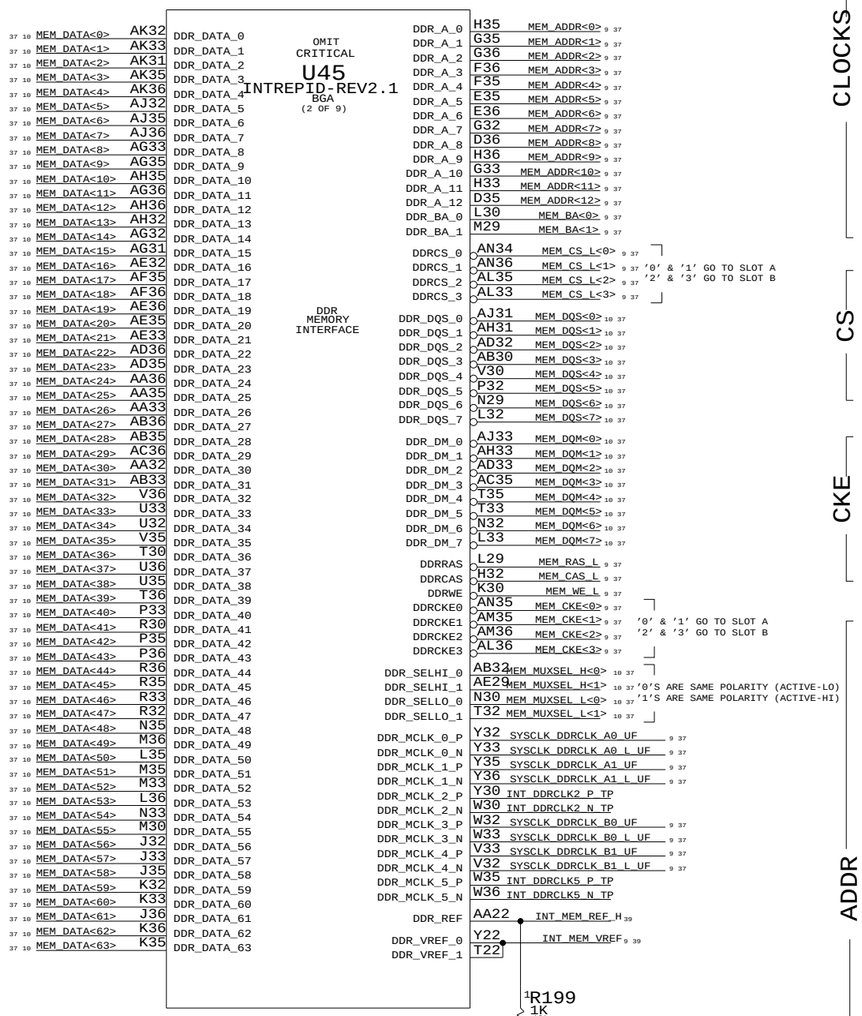
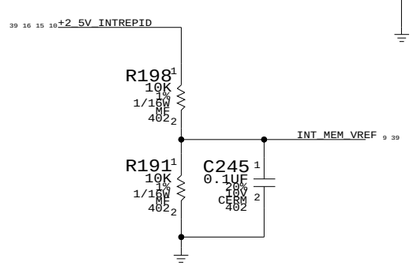
SIZE D
DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 8 OF 45

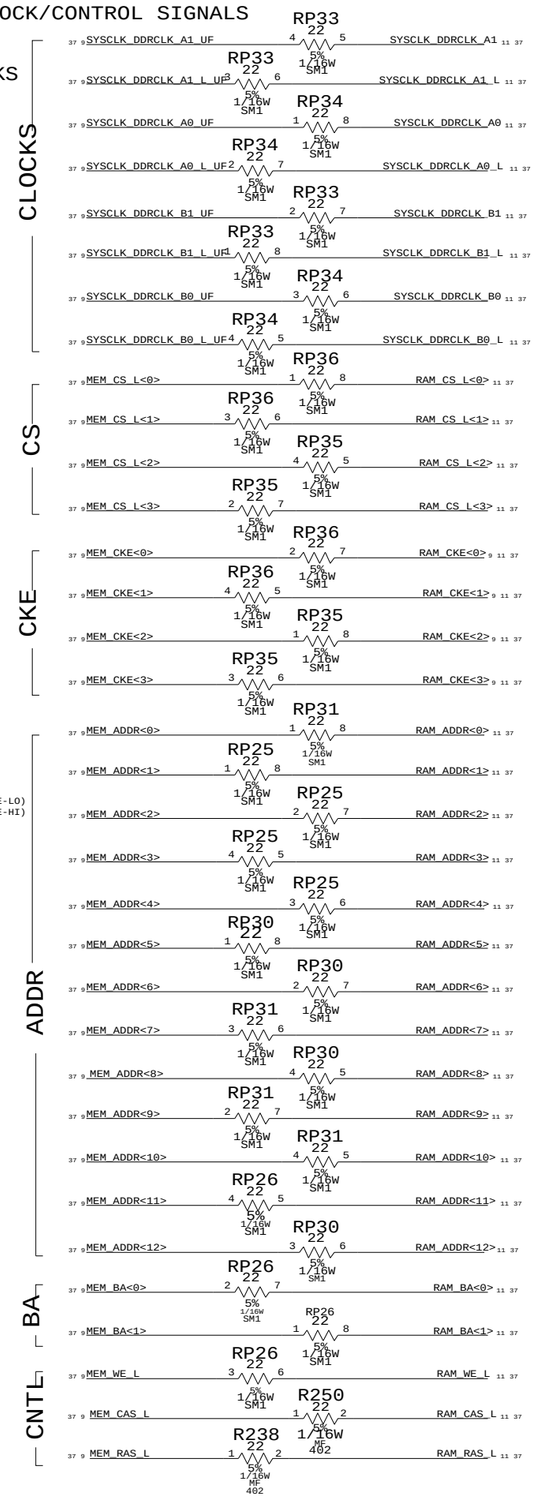
SERIES RESISTORS FOR CLOCK/CONTROL SIGNALS

PINS ARE SWAPABLE FOR RPAKS

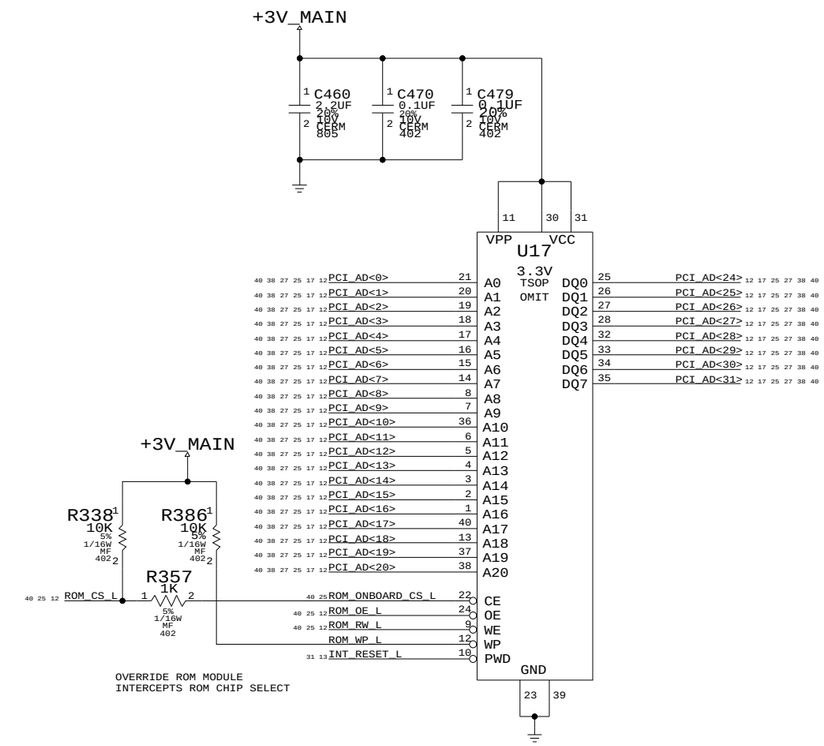


MEM_VREF





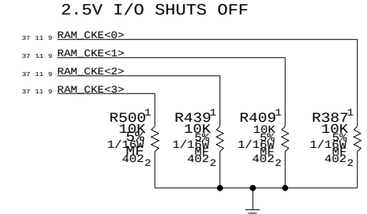
1MB BOOT ROM



OVERRIDE ROM MODULE
INTERCEPTS ROM CHIP SELECT

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1793	1	IC,BOOTROM,4.9.1F3,Q41B	U17	CRITICAL	?

PULL-DOWN RESISTORS TO ENSURE
CKE STAYS LOW AFTER INTREPID
2.5V I/O SHUTS OFF



INT - DDR/BOOTROM

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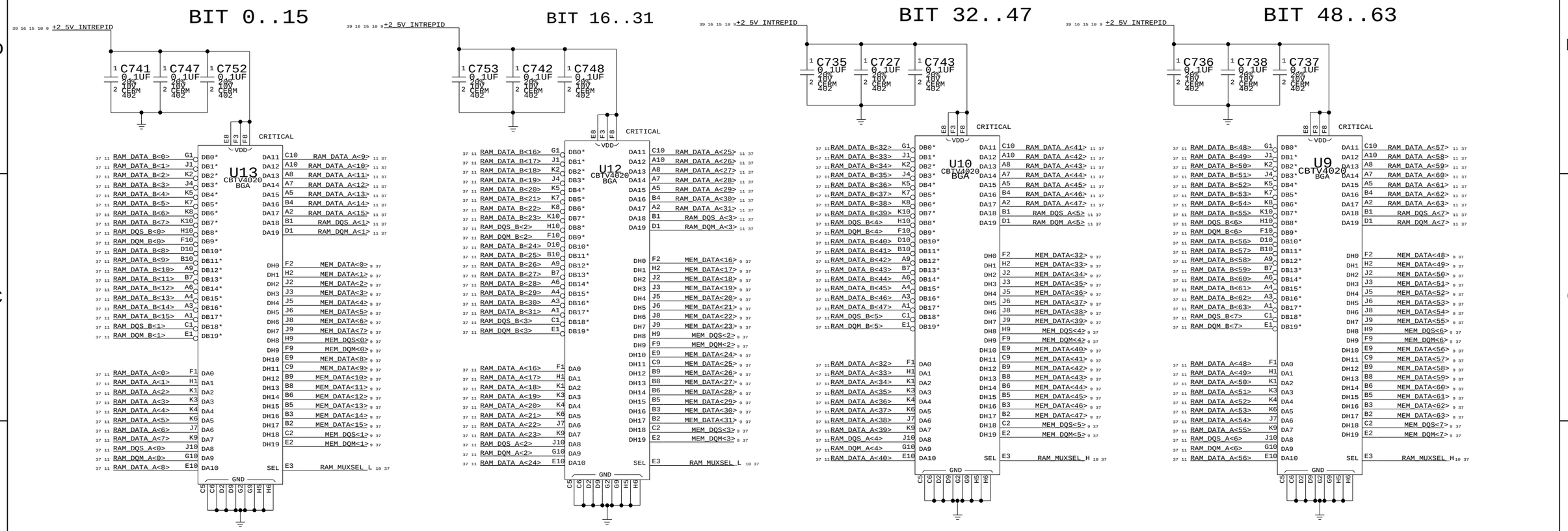
SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE NONE | SHT 9 OF 45



16BIT 2:1 DDR MUXES

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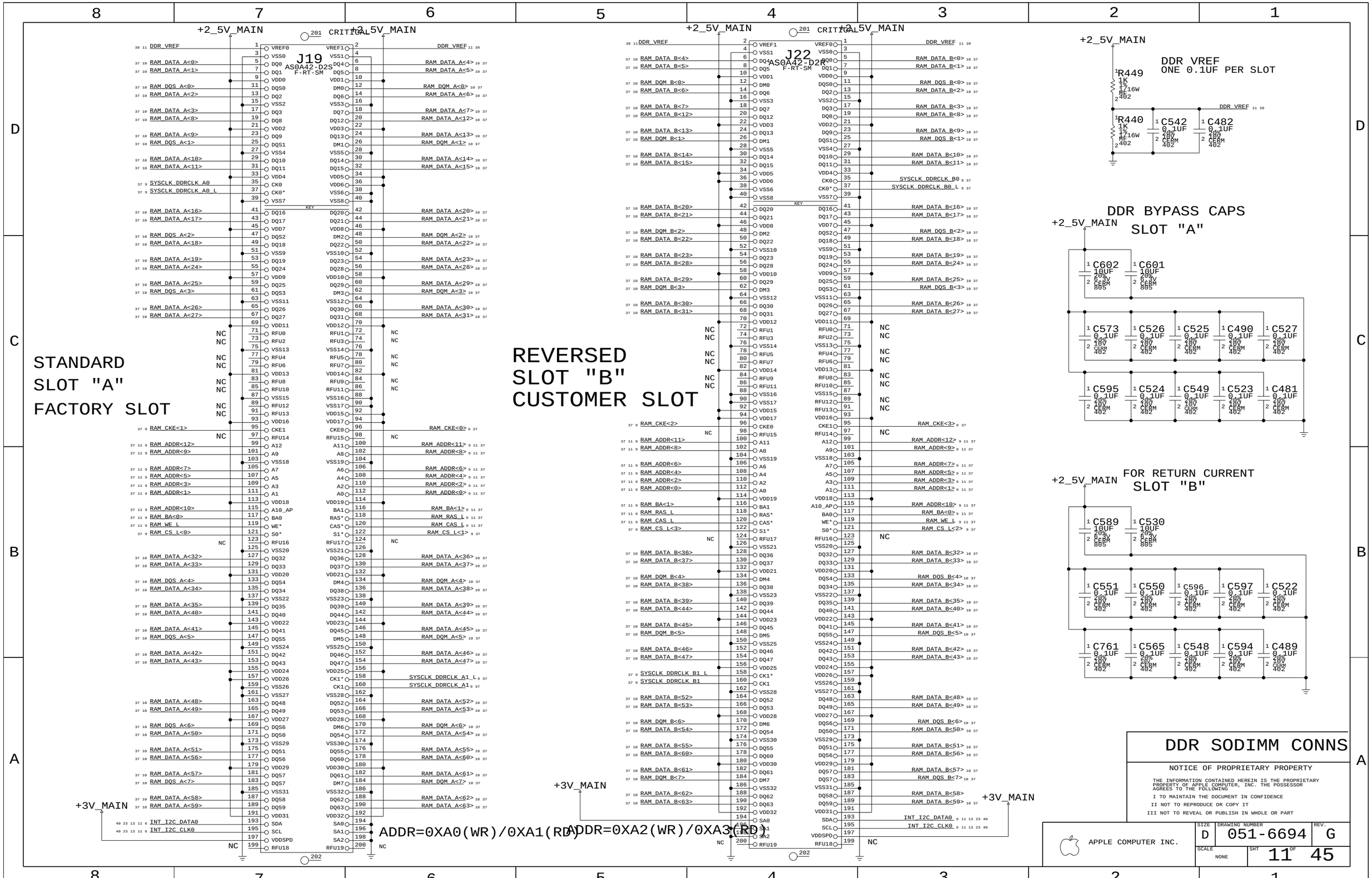
SCALE NONE

SHT 10 OF 45


STANDARD
SLOT "A"
FACTORY SLOT
J19
AS0A42-D2S
F-RT-SM
+2_5V_MAIN
CRITICAL
REVERSED
SLOT "B"
CUSTOMER SLOT
J22
AS0A42-D2R
F-RT-SM
+3V_MAIN
ADDR=0XA0(WR)/0XA1(RD)
ADDR=0XA2(WR)/0XA3(RD)
DDR VREF
ONE 0.1UF PER SLOT
R449
R440
C542
C482
DDR BYPASS CAPS
SLOT "A"
C602
C601
C573
C526
C525
C490
C527
C595
C524
C549
C523
C481
FOR RETURN CURRENT
SLOT "B"
C589
C530
C551
C550
C596
C597
C522
C761
C565
C548
C594
C489
DDR SODIMM CONNS
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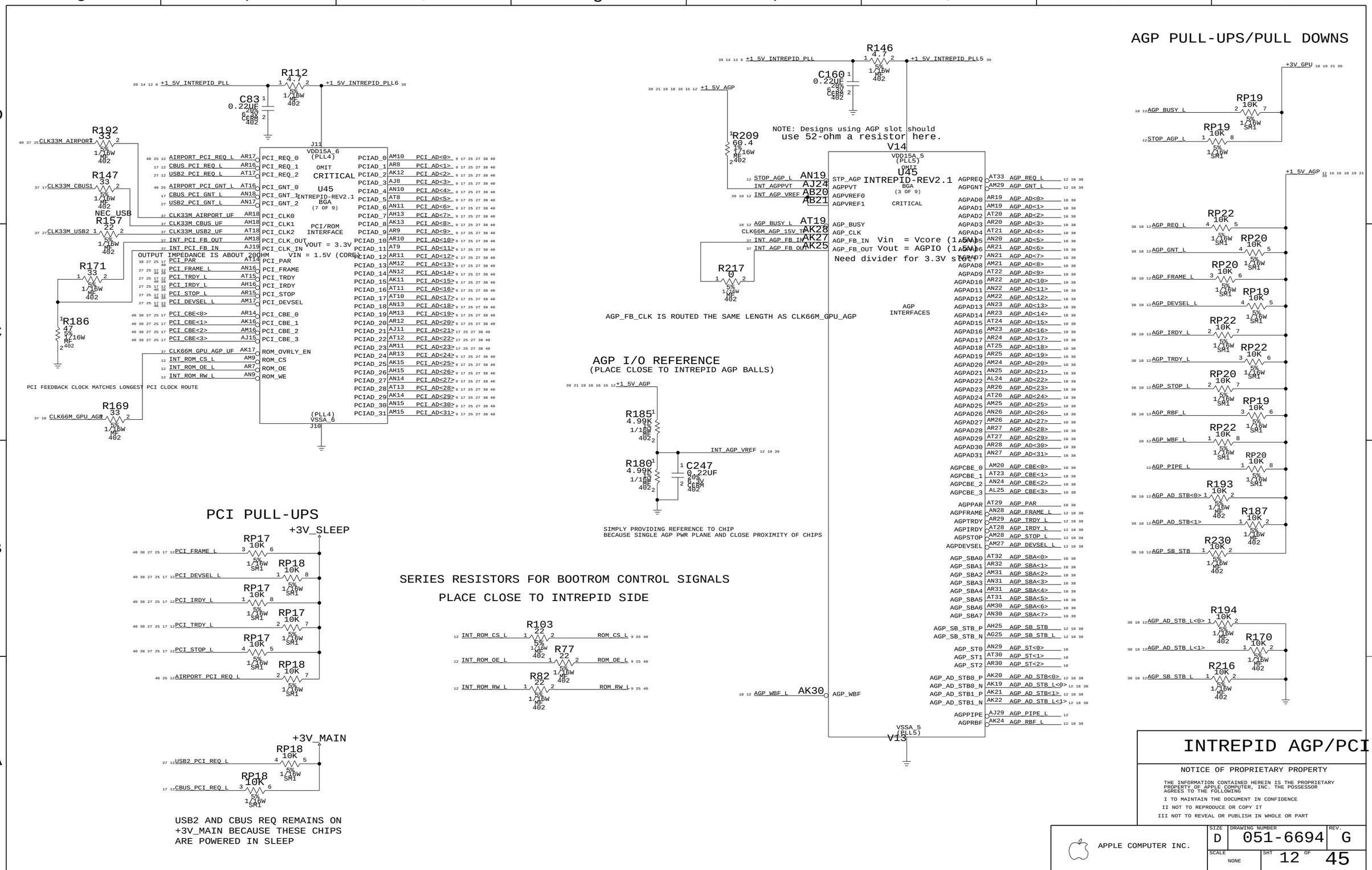
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 11 OF 45



INTREPID AGP/PCI

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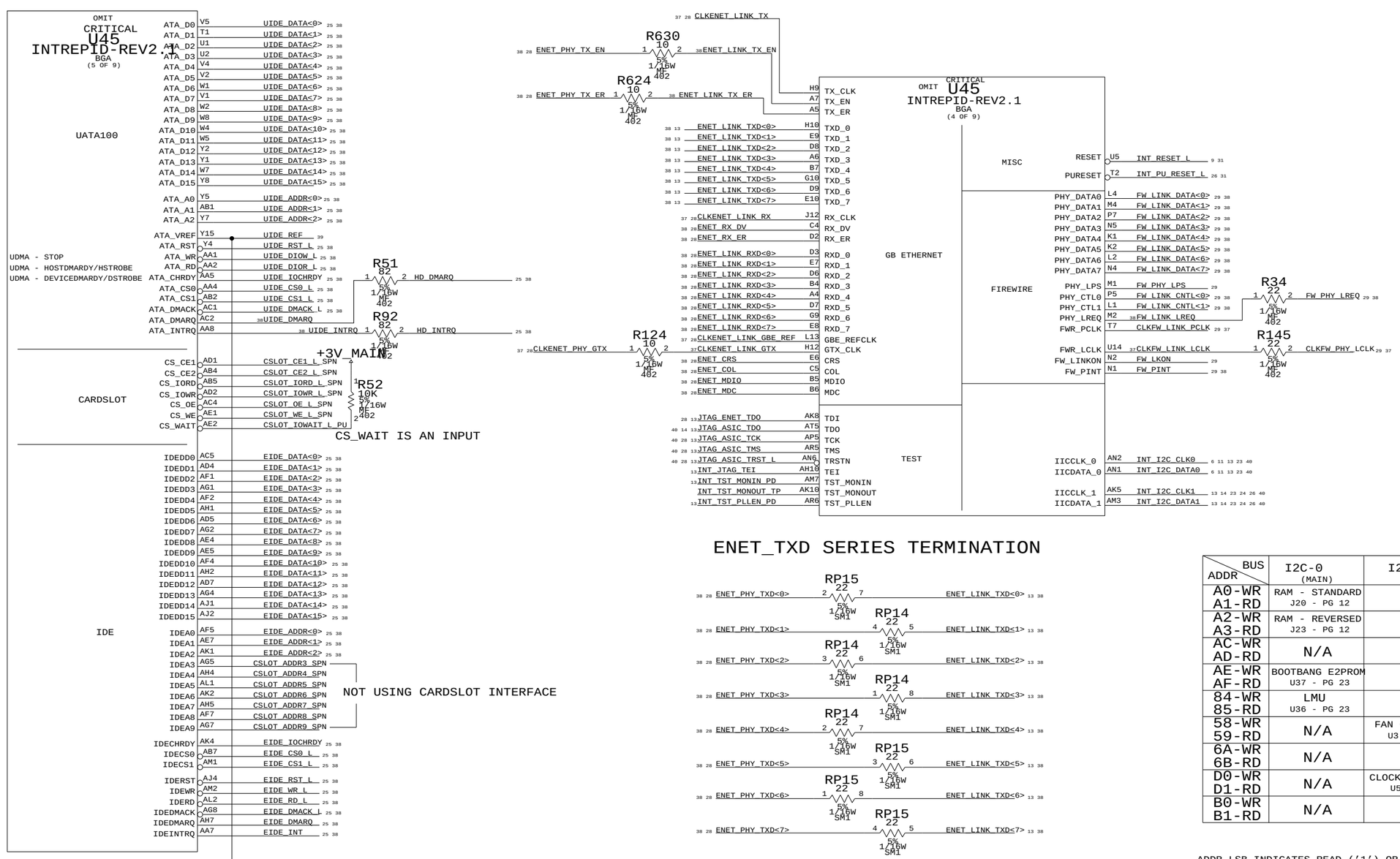
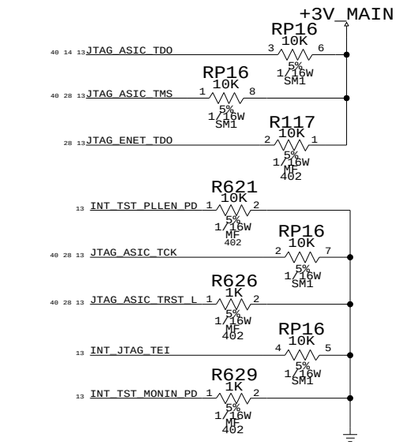
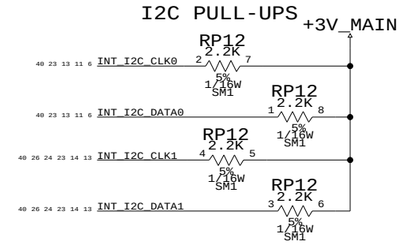
D	051-6694	G
SCALE NONE	SHT 12 OF 45	



TEST PULL-UPS/DOWNS



I2C PULL-UPS



ENET_TXD SERIES TERMINATION

BUS / ADDR	I2C-0 (MAIN)	I2C-1 (MAIN)	I2C-2 (SLEEP)	PMU (SLEEP)
A0-WR A1-RD	RAM - STANDARD J20 - PG 12	N/A	N/A	N/A
A2-WR A3-RD	RAM - REVERSED J23 - PG 12	N/A	N/A	N/A
AC-WR AD-RD	N/A	N/A	DASH MODEM J9 - PG 25	N/A
AE-WR AF-RD	BOOTBANG E2PROM U37 - PG 23	N/A	N/A	N/A
84-WR 85-RD	LMU U36 - PG 23	N/A	N/A	N/A
58-WR 59-RD	N/A	FAN CONTROLLER U3 - PG 24	N/A	N/A
6A-WR 6B-RD	N/A	N/A	SNAPPER SOUND J12 - PG 24	N/A
D0-WR D1-RD	N/A	CLOCK SLEW SSCG U56 - PG 15	N/A	N/A
B0-WR B1-RD	N/A	MMM	N/A	N/A

ADDR LSB INDICATES READ ('1') OR WRITE ('0') MODES

JTG_RSTN_L	TST_TEI_H	JTG_TDO_H (I/O)	JTG_TDI_H (I/O)	TST_PLLEN_H	ANALYZER_CLK	DESCRIPTION
1	X	X	X	X	X	JTAG MODE
0	0	EXTPLL SHUTDOWN (OUTPUT)	DDR_ TPDENABLE (OUTPUT)	0	(OUTPUT)	NORMAL OPERATION
0	0	(OUTPUT)	0(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (SOFTWARE)
0	0	HWPLL_ TESTSEL5 (INPUT)	1(I)	1	SELECTED PLL OUTPUTS	VIEW PLLS (HARDWARE)
0	1	0(I)	0(I)	MEMWE	SYNC/MEM DATA BYPASS	ATPG NORMAL
0	1	0(I)	1(I)	0	X(I)	ATPG IDDQ
0	1	0(I)	1(I)	1	X(I)	TEST TRI-STATE
0	1	1(I)	0(I)	0	X(I)	FUNCTIONAL TEST WITHOUT POSTSCALAR BYPASS
0	1	1(I)	0(I)	1	X(I)	FUNCTIONAL TEST WITH POSTSCALAR BYPASS
0	1	1(I)	1(I)	X	X(I)	FUNCTIONAL TEST IDDQ

INT - ENET/FW/UATA EIDE/I2C

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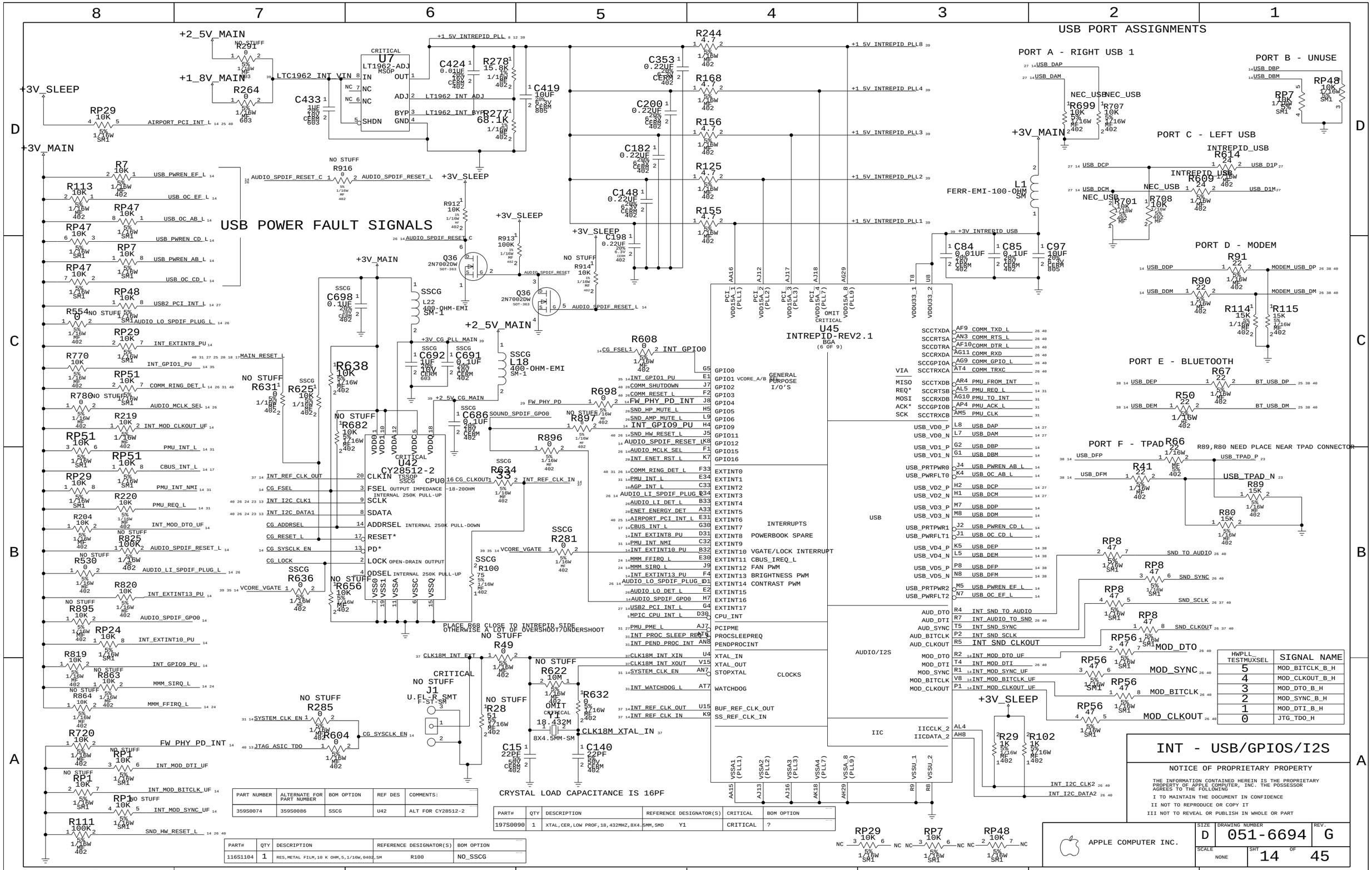
SCALE NONE	SHT 13 OF 45	

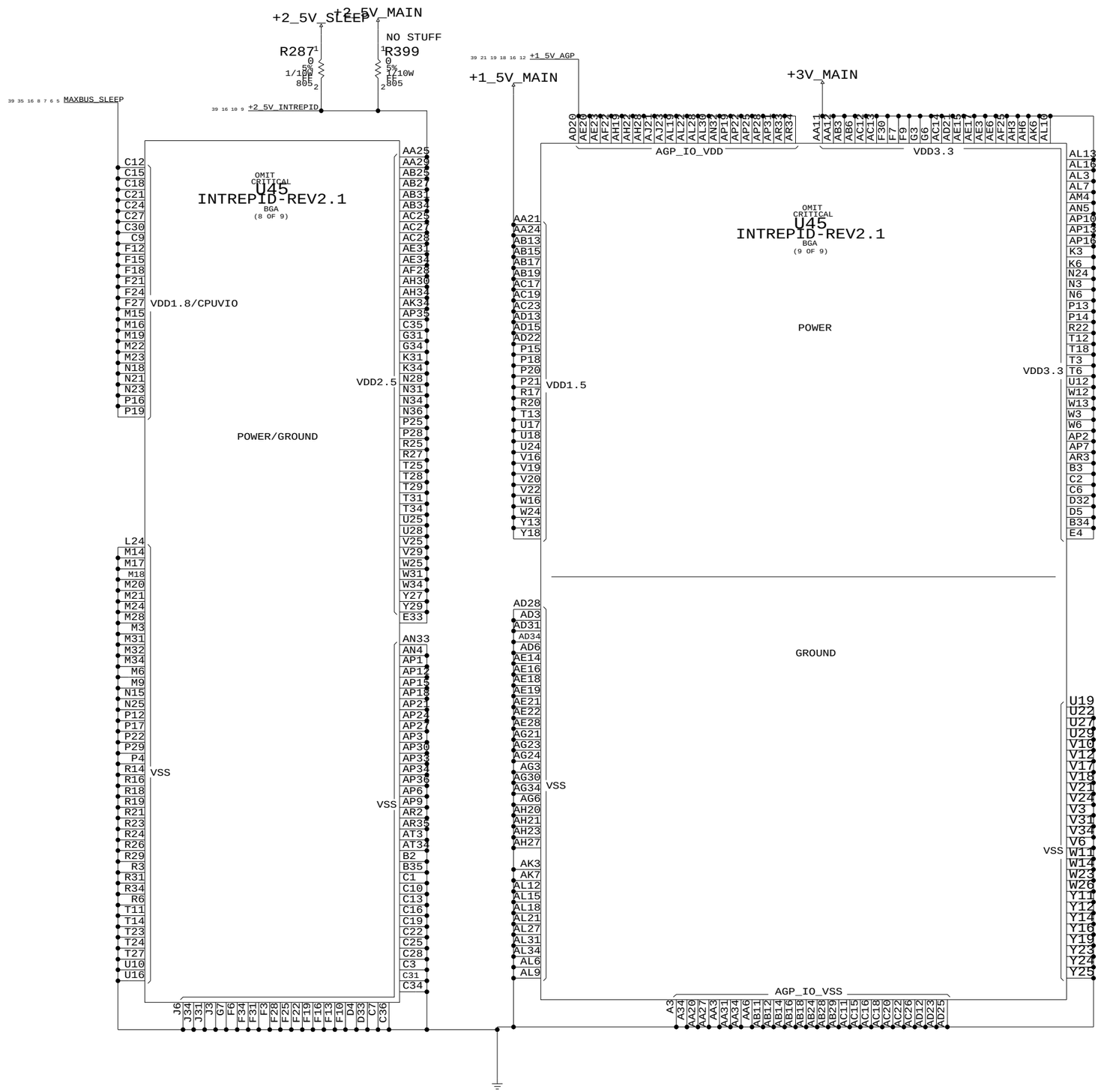


HWPLL_TESTMUXSEL	SIGNAL NAME
5	MOD_BITCLK_B_H
4	MOD_CLKOUT_B_H
3	MOD_DTO_B_H
2	MOD_SYNC_B_H
1	MOD_DTI_B_H
0	JTG_TDO_H

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
359S0074	359S0086	SSCG	U42	ALT FOR CY28512-2

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0090	1	XTAL,CER,LOW PROF,18,432MHZ,8X4.5MM,SMD	Y1	CRITICAL	?

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
116S1104	1	RES,METAL FILM,10 K OHM,5,1/16W,0402,SM	R100	NO_SSCG



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
343S0305	1	IC,ASIC,INTREPID,REV2.1,974BGA,FAST	U45	CRITICAL	?

Intrepid Power

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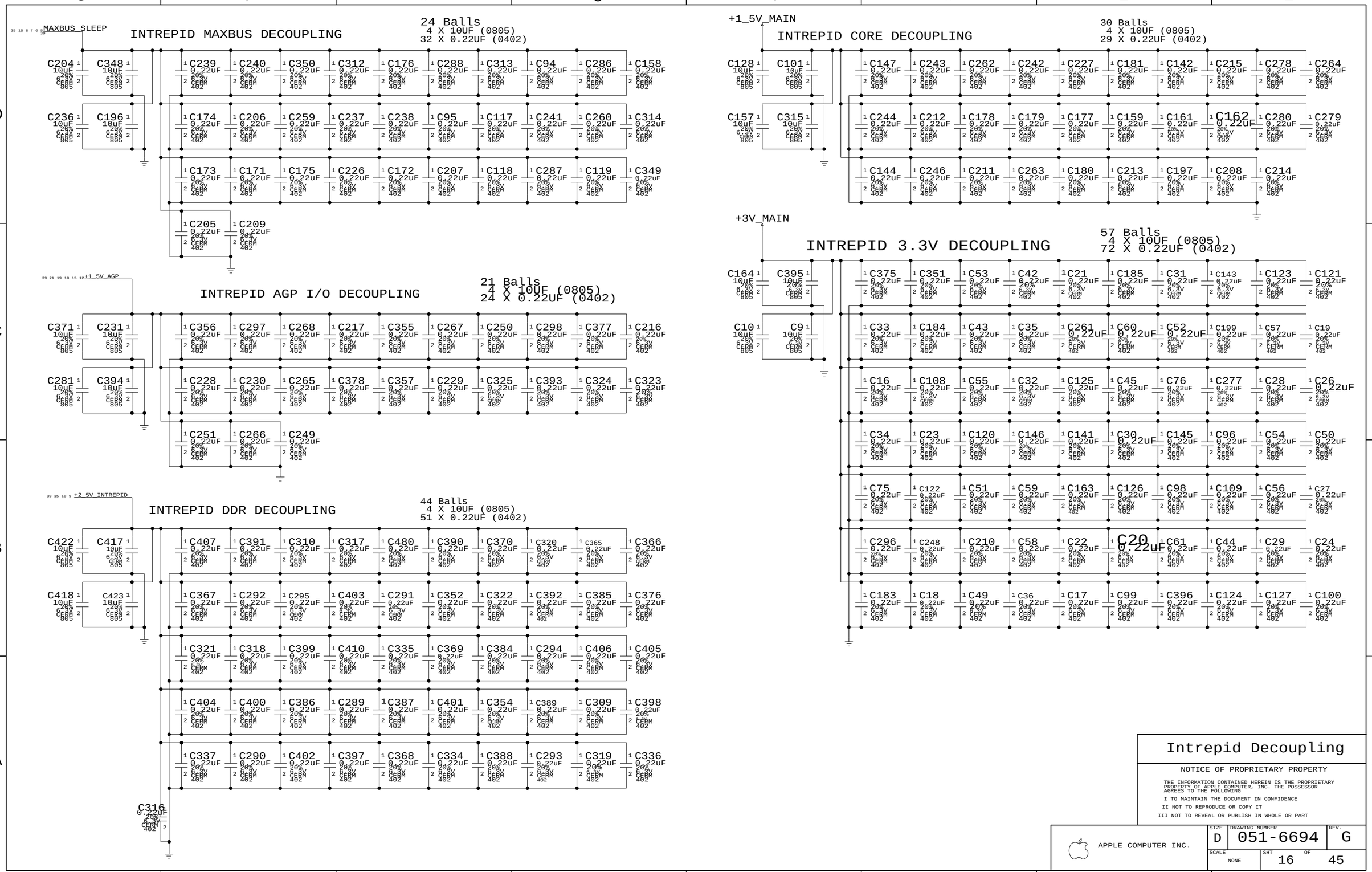
SCALE NONE	SHT 15 OF 45	



Intrepid Decoupling

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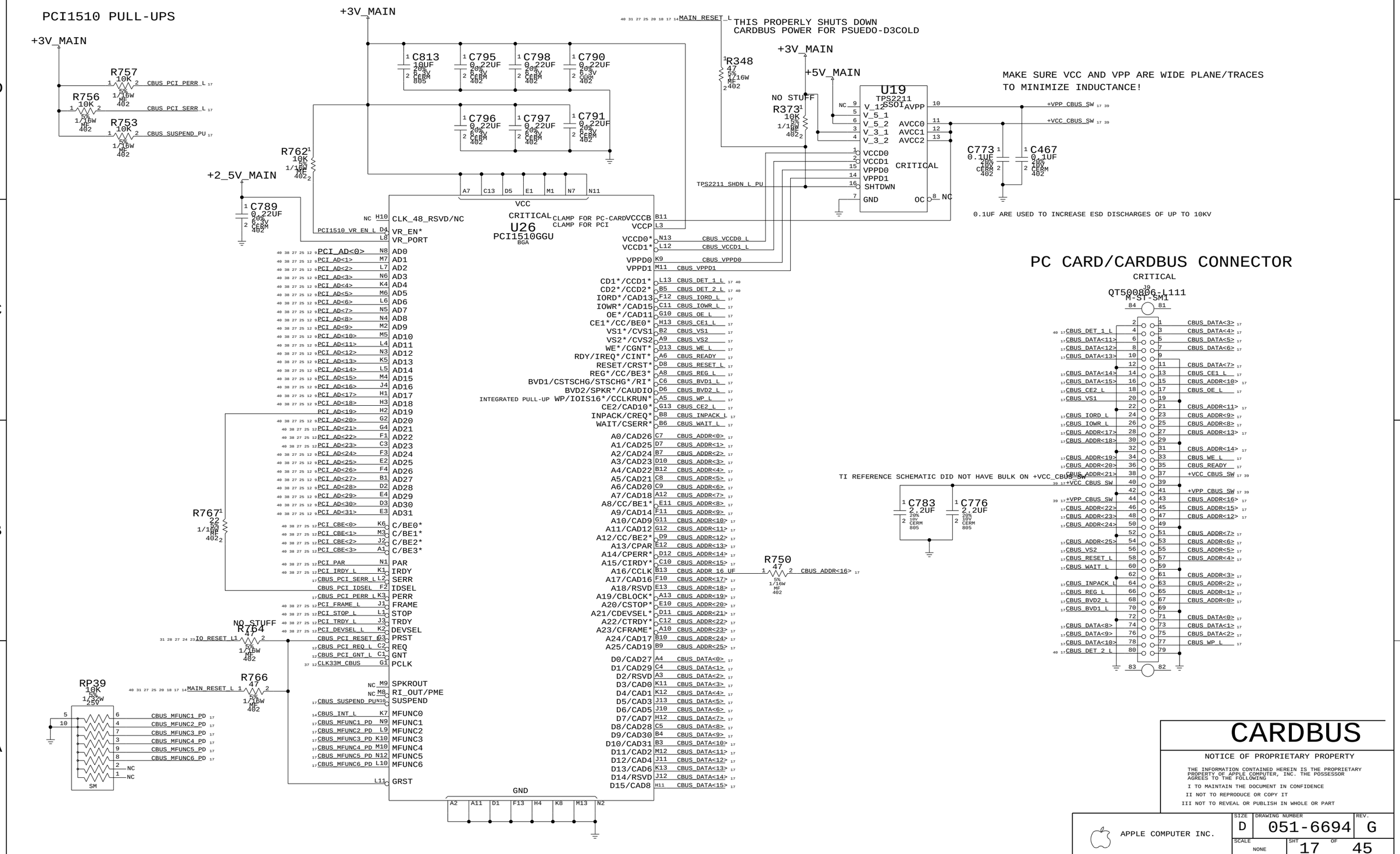
SIZE	DRAWING NUMBER	REV.
D	051-6694	G

SCALE	SHT	OF
NONE	16	45


PCI1510 PULL-UPS
+3V_MAIN
R757 10K 5% 1/16W MF 402
R756 10K 5% 1/16W MF 402
R753 10K 5% 1/16W MF 402
CBUS_PCI_PERR_L
CBUS_PCI_SERR_L
CBUS_SUSPEND_PU
C813 10UF 20% 6.3V CERM 805
C795 0.22UF 20% 6.3V CERM 402
C798 0.22UF 20% 6.3V CERM 402
C790 0.22UF 20% 6.3V CERM 402
C796 0.22UF 20% 6.3V CERM 402
C797 0.22UF 20% 6.3V CERM 402
C791 0.22UF 20% 6.3V CERM 402
R762 10K 5% 1/16W MF 402
+2_5V_MAIN
C789 0.22UF 20% 6.3V CERM 402
MAIN_RESET_L
THIS PROPERLY SHUTS DOWN
CARDBUS POWER FOR PSUEDO-D3COLD
R348 47 5% 1/16W MF 402
+5V_MAIN
NO STUFF
R373 10K 5% 1/16W MF 402
U19
TPS2211
SSOP
V_12
V_5_1
V_5_2
V_3_1
V_3_2
AVPP
AVCC0
AVCC1
AVCC2
VCCD0
VCCD1
VPPD0
VPPD1
SHTDWN
GND
OC
CRITICAL
TPS2211_SHDN_L_PU
+VPP_CBUS_SW
+VCC_CBUS_SW
MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES
TO MINIMIZE INDUCTANCE!
C773 0.1UF 20% 10V CERM 402
C467 0.1UF 20% 10V CERM 402
0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV
VCC
CRITICAL
U26
PCI1510GGU
BGA
CLAMP FOR PC-CARD
CLAMP FOR PCI
CLK_48_RSVD/NC
VR_EN*
VR_PORT
PCI1510_VR_EN_L
VCCCB
VCCP
VCCD0*
VCCD1*
VPPD0
VPPD1
CBUS_VCCD0_L
CBUS_VCCD1_L
CBUS_VPPD0
CBUS_VPPD1
PCI_AD<0>
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
C/BE0*
C/BE1*
C/BE2*
C/BE3*
PAR
IRDY
SERR
IDSEL
PERR
FRAME
STOP
TRDY
DEVSEL
PRST
REQ
GNT
PCLK
SPKROUT
RI_OUT/PME
SUSPEND
MFUNC0
MFUNC1
MFUNC2
MFUNC3
MFUNC4
MFUNC5
MFUNC6
GRST
CD1*/CCD1*
CD2*/CCD2*
IORD*/CAD13
IOWR*/CAD15
OE*/CAD11
CE1*/CC/BE0*
VS1*/CVS1
VS2*/CVS2
WE*/CGNT*
RDY/IREQ*/CINT*
RESET/CRST*
REG*/CC/BE3*
BVD1/CSTSCHG/STSCHG*/RI*
BVD2/SPKR*/CAUDIO
INTEGRATED PULL-UP
WP/IOIS16*/CCLKRUN*
CE2/CAD10*
INPACK/CREQ*
WAIT/CSERR*
A0/CAD26
A1/CAD25
A2/CAD24
A3/CAD23
A4/CAD22
A5/CAD21
A6/CAD20
A7/CAD18
A8/CC/BE1*
A9/CAD14
A10/CAD9
A11/CAD12
A12/CC/BE2*
A13/CPAR
A14/CPERR*
A15/CIRDY*
A16/CCLK
A17/CAD16
A18/RSVD
A19/CBLOCK*
A20/CSTOP*
A21/CDEVSEL*
A22/CTRDY*
A23/CFRAME*
A24/CAD17
A25/CAD19
D0/CAD27
D1/CAD29
D2/RSVD
D3/CAD0
D4/CAD1
D5/CAD3
D6/CAD5
D7/CAD7
D8/CAD28
D9/CAD30
D10/CAD31
D11/CAD2
D12/CAD4
D13/CAD6
D14/RSVD
D15/CAD8
R767 22 5% 1/16W MF 402
R750 47 5% 1/16W MF 402
CBUS_ADDR_16_UF
CBUS_ADDR<16>
NO STUFF
R764 47 5% 1/16W MF 402
IO_RESET_L
R766 47 5% 1/16W MF 402
RP39 10K 5% 1/16W 25V SM
CBUS_MFUNC1_PD
CBUS_MFUNC2_PD
CBUS_MFUNC3_PD
CBUS_MFUNC4_PD
CBUS_MFUNC5_PD
CBUS_MFUNC6_PD
GND
PC CARD/CARDBUS CONNECTOR
CRITICAL
J9
QT500806-L111
M-ST-SM1
TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON +VCC_CBUS_SW
C783 2.2UF 20% 16V CERM 805
C776 2.2UF 20% 10V CERM 805
CARDBUS
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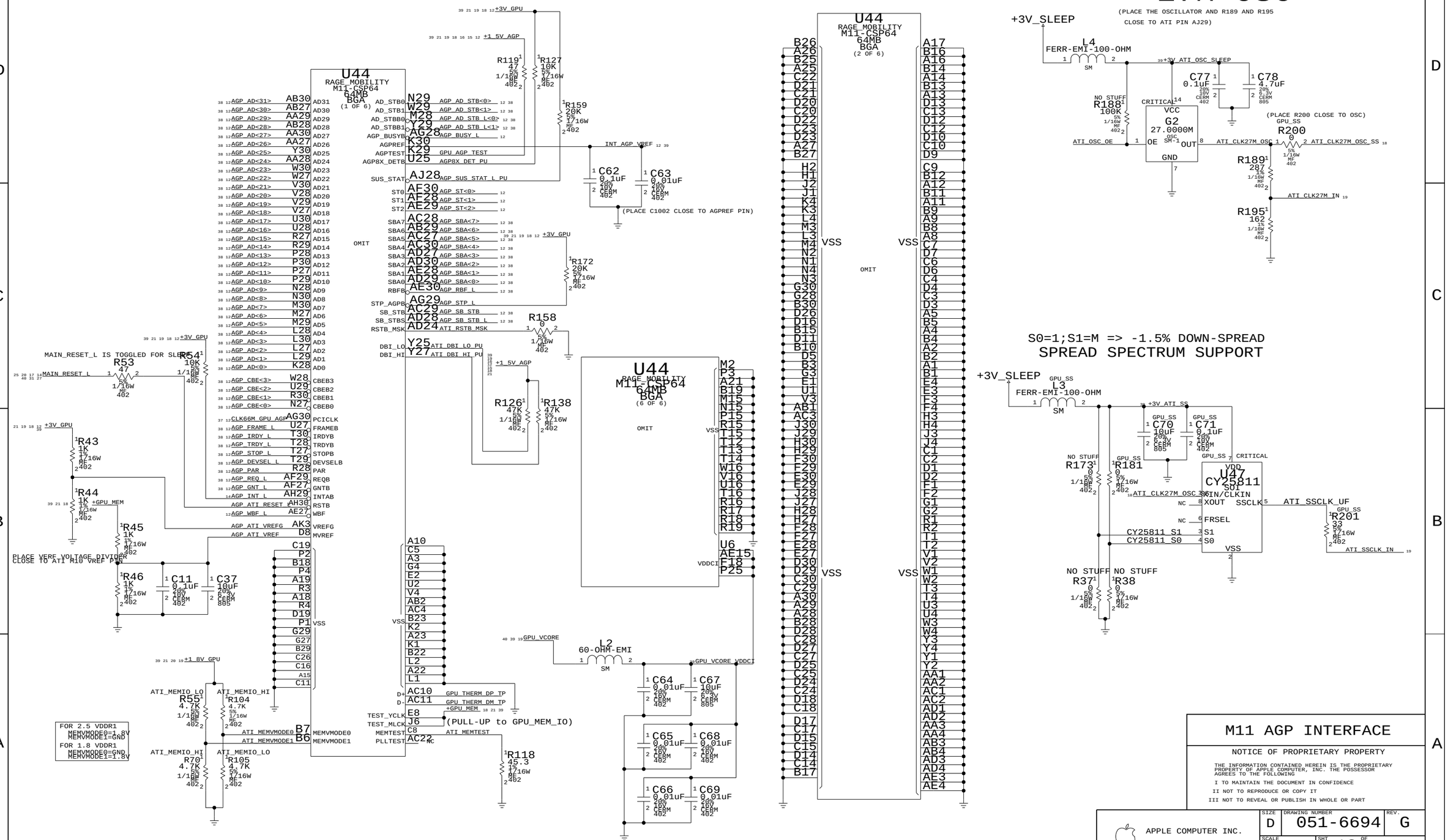
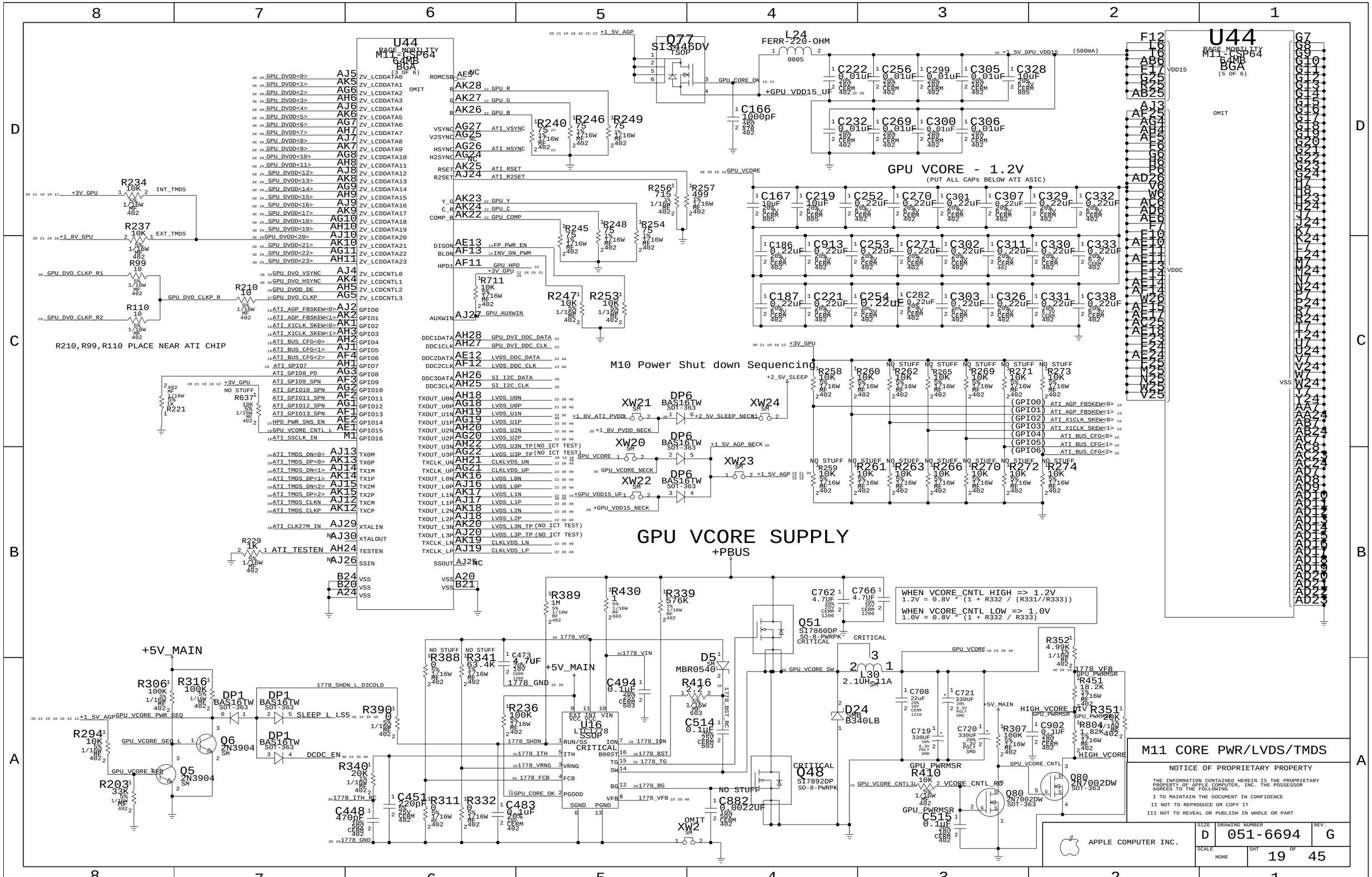
SIZE D
DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 17 OF 45

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0214	1	IC,ATI,M11-CSP128,GRPHCTLR,667BGA,HYNIX U44	U44	CRITICAL	M11_CSP128




U44
RAGE MOBILITY
M11-CSP64
64MB
BGA
(3 OF 6)
(5 OF 6)
OMIT
Q77
SI3446DV
TSOP
L24
FERR-220-OHM
0805
GPU VCORE - 1.2V
(PUT ALL CAPS BELOW ATI ASIC)
M10 Power Shut down Sequencing
GPU VCORE SUPPLY
+PBUS
WHEN VCORE_CNTL HIGH => 1.2V
1.2V = 0.8V * (1 + R332 / (R331//R333))
WHEN VCORE_CNTL LOW => 1.0V
1.0V = 0.8V * (1 + R332 / R333)
R210,R99,R110 PLACE NEAR ATI CHIP
+5V_MAIN
M11 CORE PWR/LVDS/TMDS
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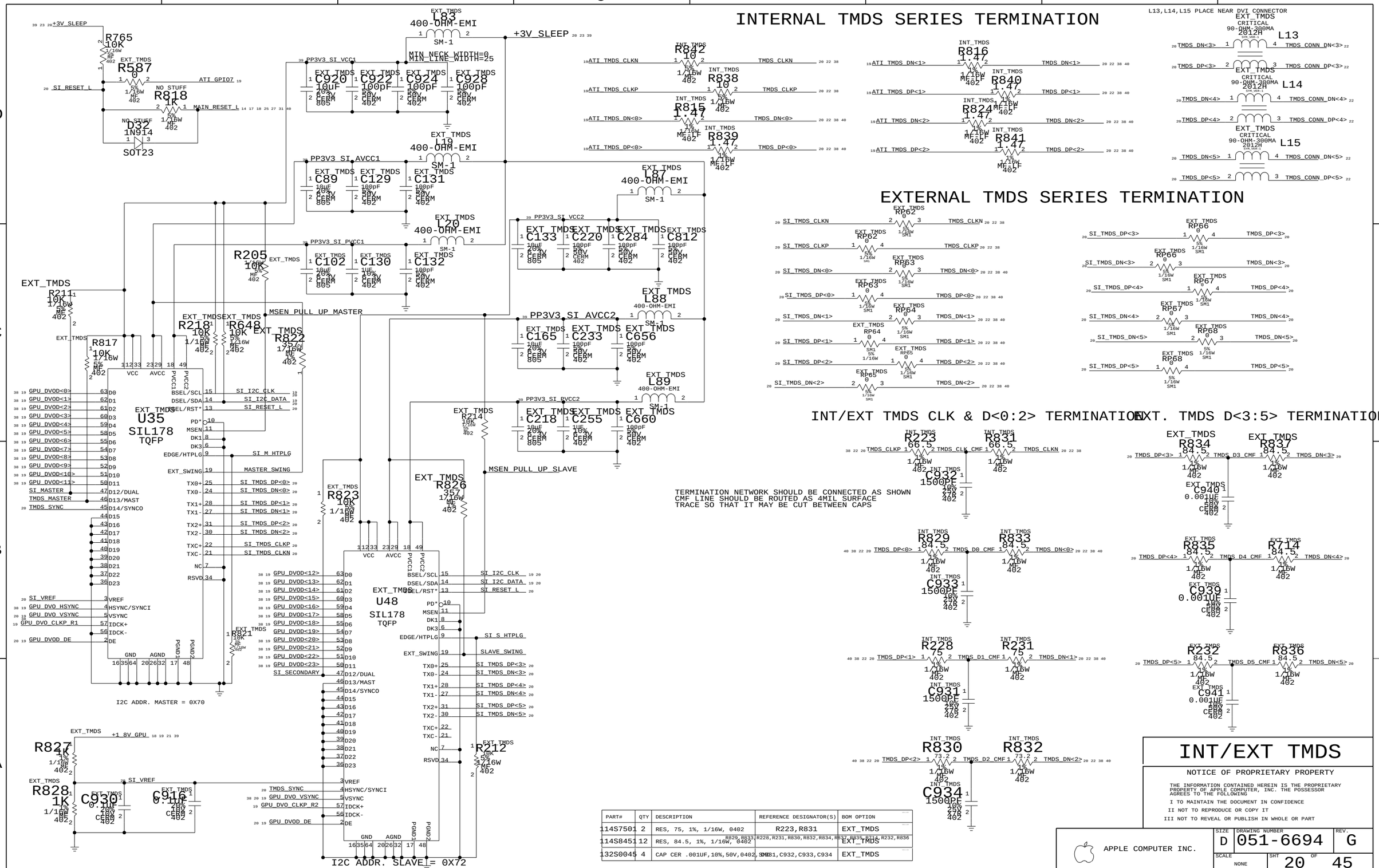

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S7501	2	RES, 75, 1%, 1/16W, 0402	R223,R831	EXT_TMDS
114S8451	12	RES, 84.5, 1%, 1/16W, 0402	R829,R833,R228,R231,R830,R832,R834,R837,R835,R714,R232,R836	EXT_TMDS
132S0045	4	CAP CER .001UF,10%,50V,0402,SMD	C931,C932,C933,C934	EXT_TMDS

INT/EXT TMDS

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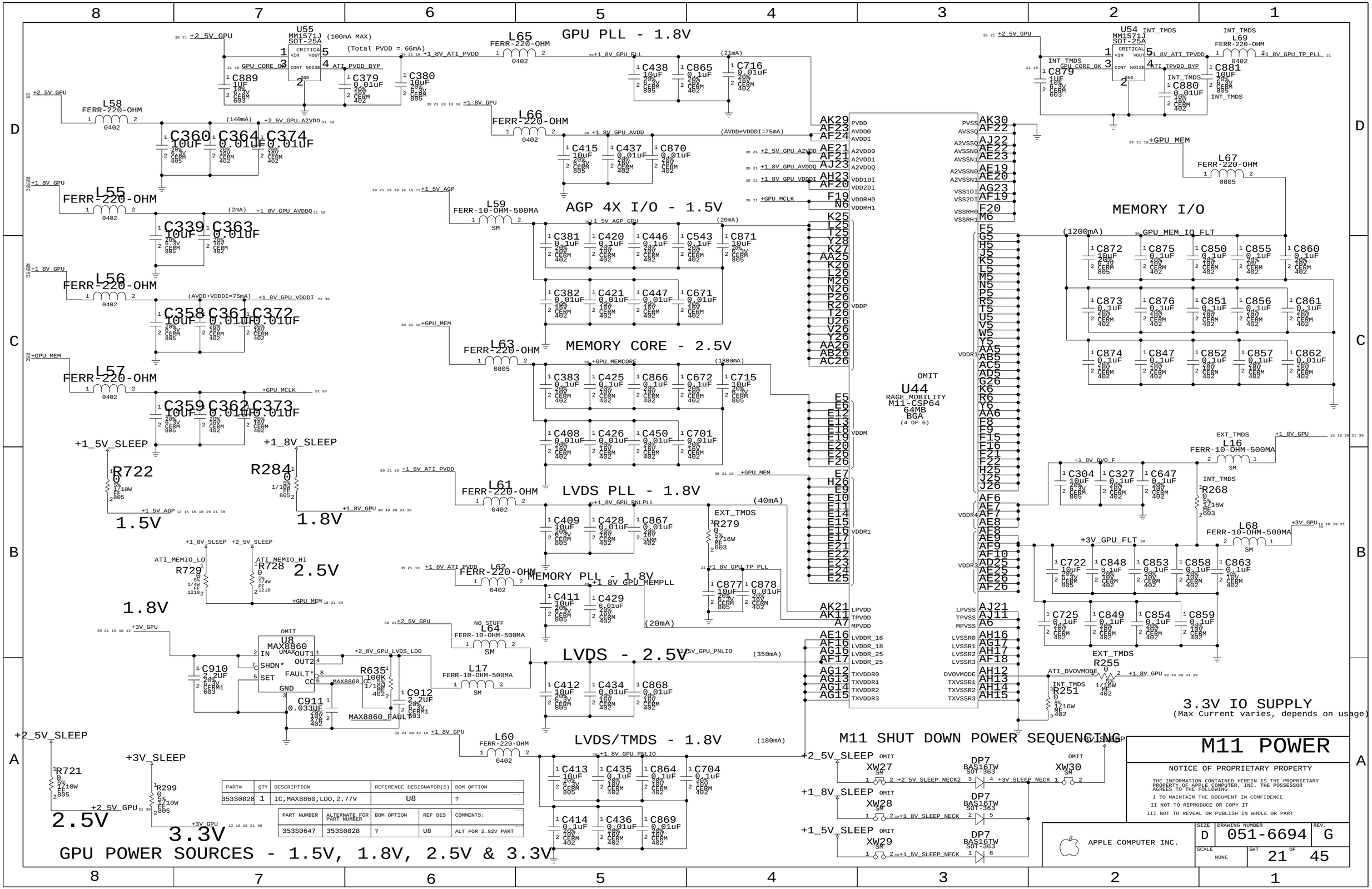
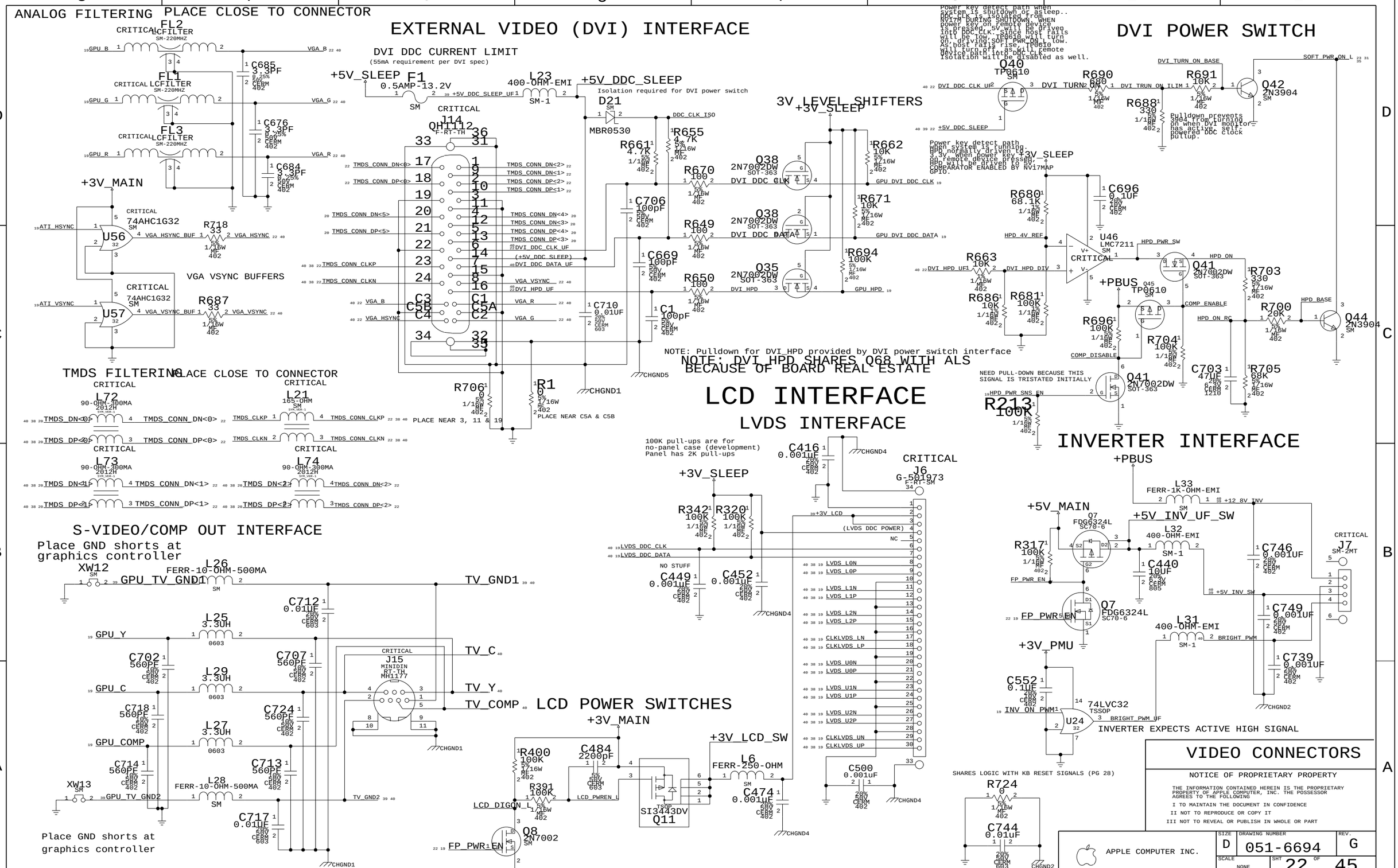


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0828	1	IC,MAX8860,LDO,2.77V	U8	?

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S0828	?	U8	ALT FOR 2.82V PART


ANALOG FILTERING PLACE CLOSE TO CONNECTOR
EXTERNAL VIDEO (DVI) INTERFACE
DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)
DVI POWER SWITCH
Power key detect path when system is shutdown or asleep.. DDC CLK is isolated from NV17M DURING SHUTDOWN. WHEN power key on remote device is pressed, 5V will be driven into DDC CLK. Since host rails will be low, TPD610 will turn on, driving SOFT_PWR_ON L low. As host rails rise, TPD610 will turn off, as will remote device path. DDC CLK Isolation will be disabled as well.
Isolation required for DVI power switch
3V LEVEL SHIFTERS
Power key detect path when system is running. HPD normally driven to 3.3V when power key +3V_SLEEP on remote device pressed. HPD will be driven to 5V. COMPARATOR ENABLED BY NV17MAP GPIO.
Pulldown prevents 3904 from turning on when DVI monitor has active self-powered DDC clock pullup.
VGA VSYNC BUFFERS
TMDS FILTERING PLACE CLOSE TO CONNECTOR
NOTE: Pulldown for DVI_HPD provided by DVI power switch interface
NOTE: DVI_HPD SHARES Q68 WITH ALS BECAUSE OF BOARD REAL ESTATE
LCD INTERFACE
LVDS INTERFACE
INVERTER INTERFACE
100K pull-ups are for no-panel case (development) Panel has 2K pull-ups
S-VIDEO/COMP OUT INTERFACE
Place GND shorts at graphics controller
LCD POWER SWITCHES
NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
INVERTER EXPECTS ACTIVE HIGH SIGNAL
SHARES LOGIC WITH KB RESET SIGNALS (PG 28)
VIDEO CONNECTORS
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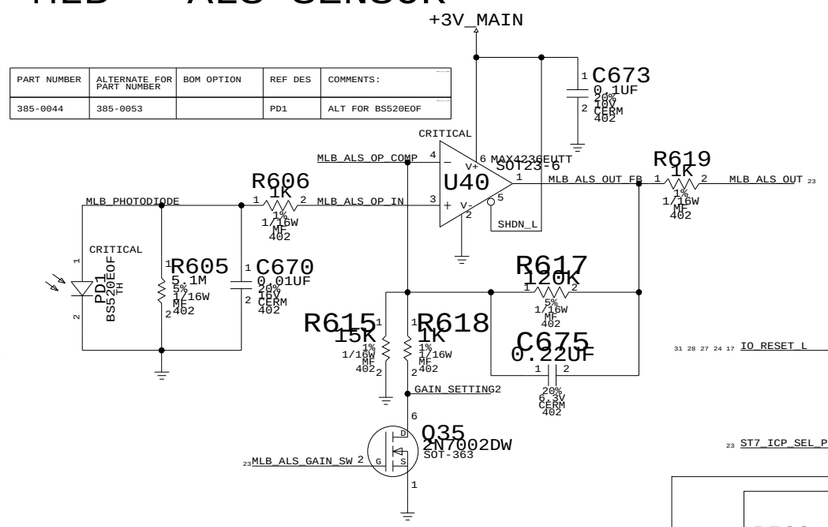
MLB - ALS SENSOR

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
385-0044	385-0053		PD1	ALT FOR BS520EOF

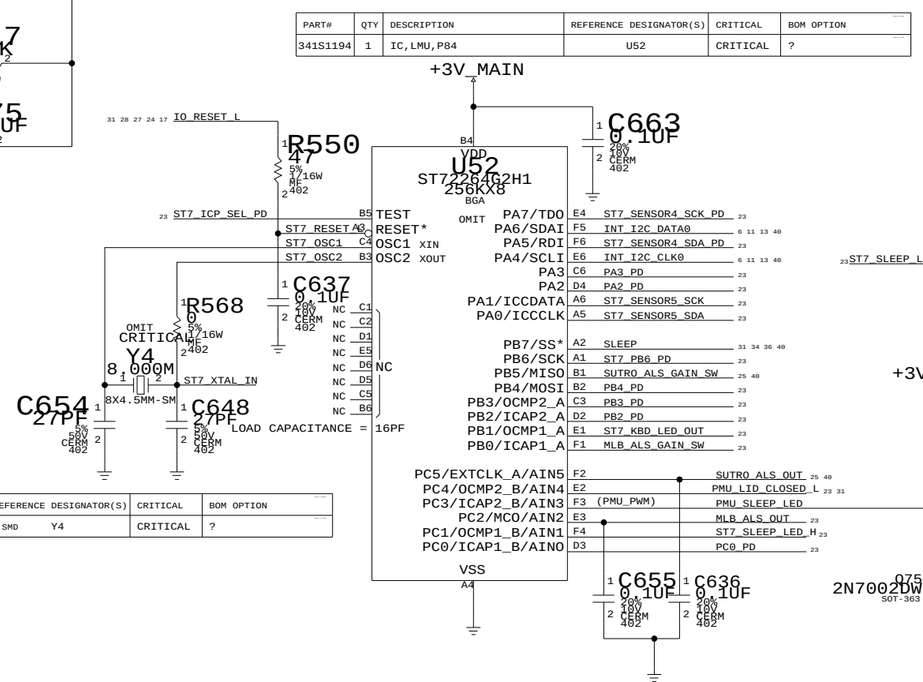
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U40	ALT FOR SUPPLY PROBLEM



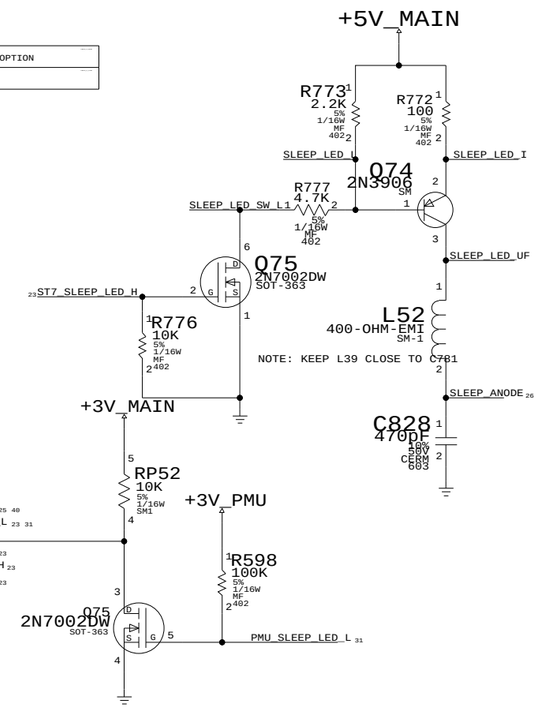
LMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
341S1194	1	IC,LMU,P84	U52	CRITICAL	?

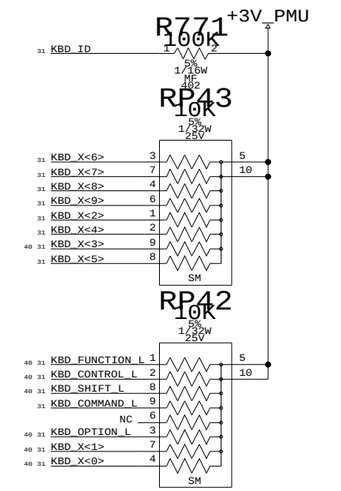
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0091	1	XTAL,CER,LOW PROF,8.000MHZ,8X4.5MM,SMD	Y4	CRITICAL	?



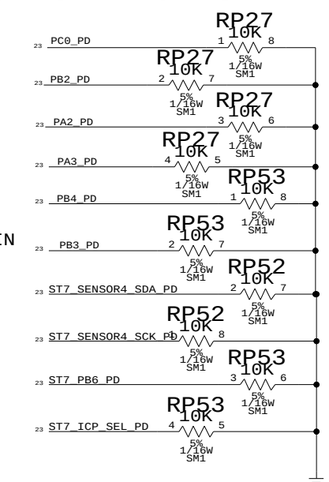
SLEEP LED



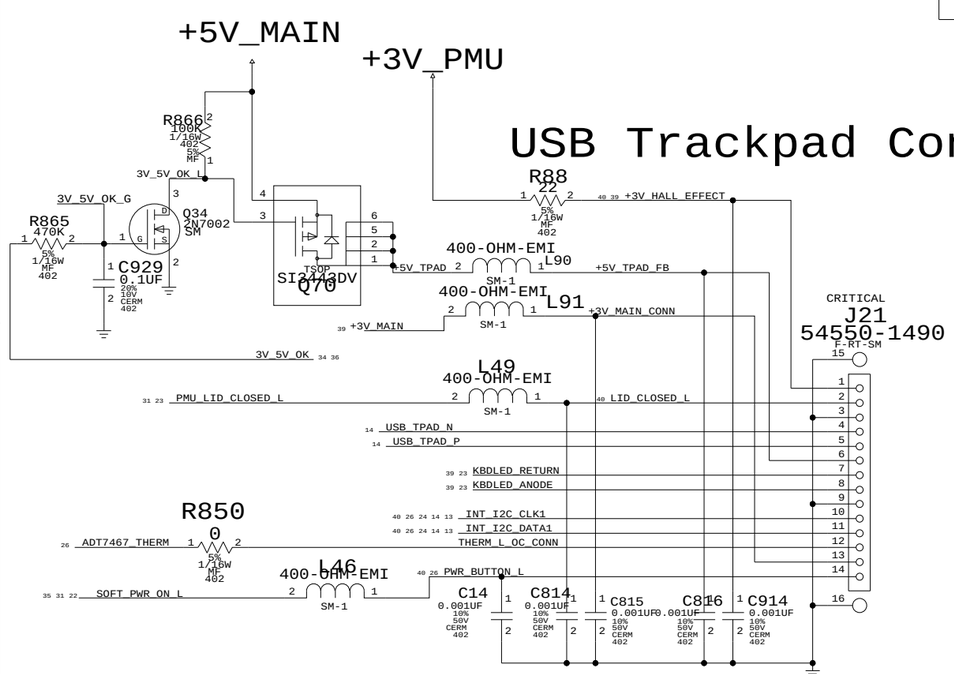
KEYBOARD PULLUPS



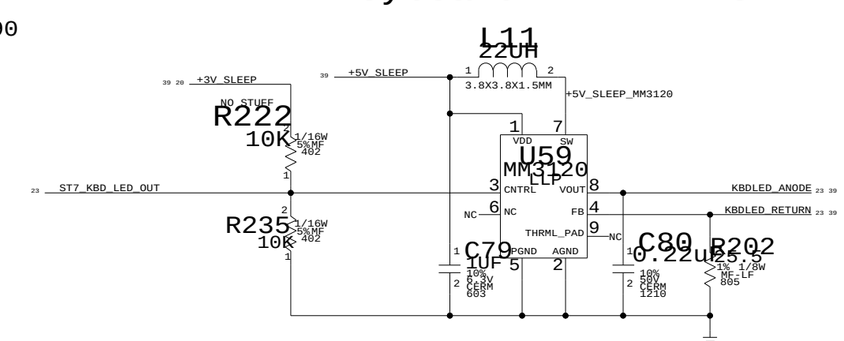
LMU PULL-DOWNS

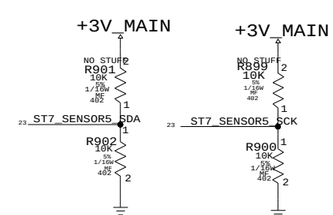


USB Trackpad Connector



Keyboard LED Driver





LMU/BOOTBANGER/SPIDEY

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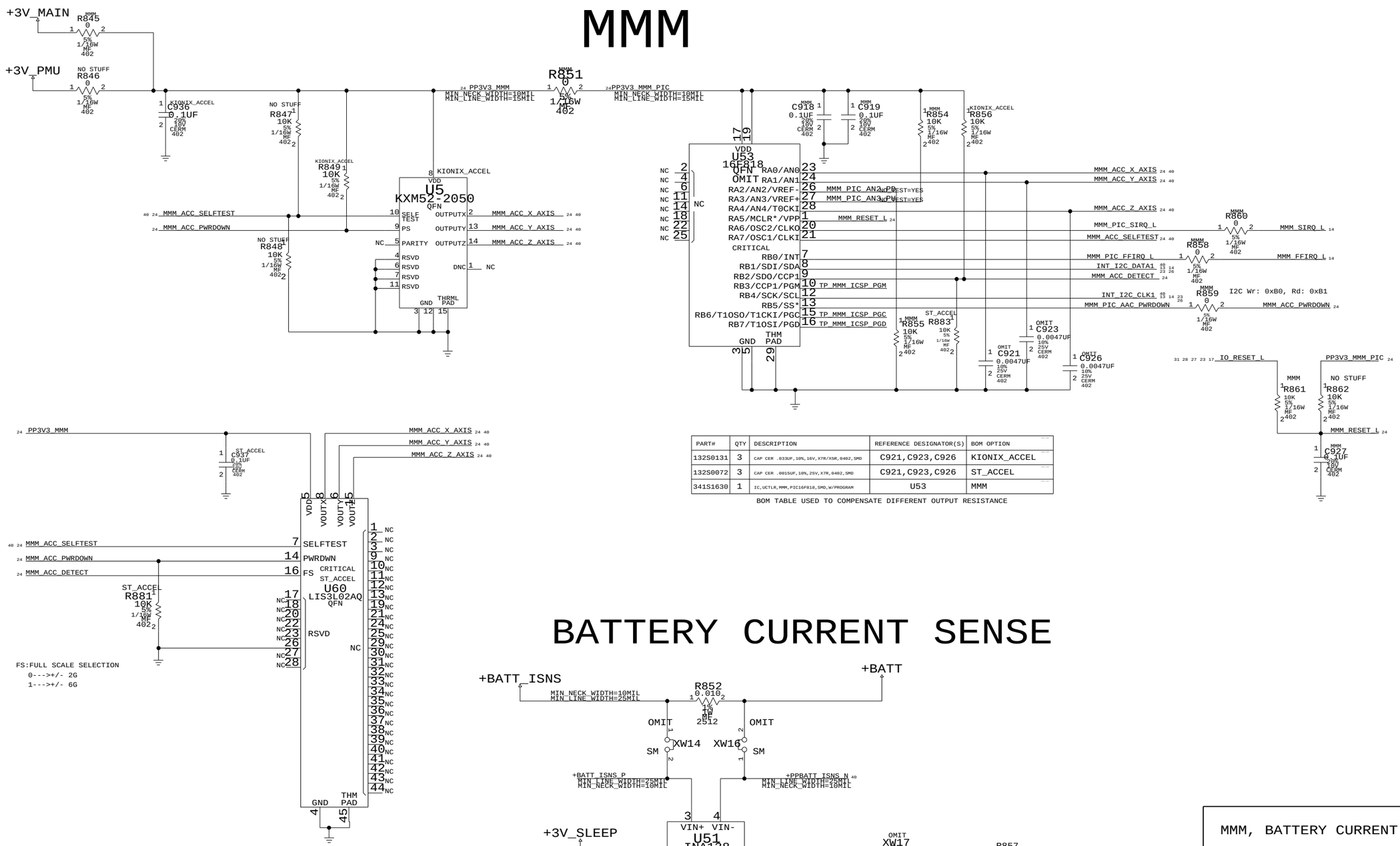
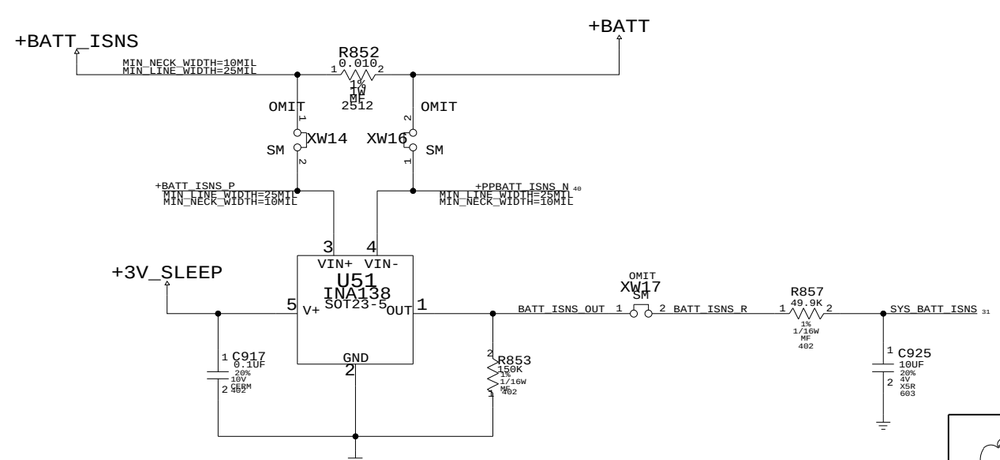
MMM



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S0131	3	CAP CER .033UF,10%,16V,X7R/X5R,0402,SMD	C921,C923,C926	KIONIX_ACCEL
132S0072	3	CAP CER .0015UF,10%,25V,X7R,0402,SMD	C921,C923,C926	ST_ACCEL
341S1630	1	IC,UCTLR,MMM,PIC16F818,SMD,W/PROGRAM	U53	MMM

BOM TABLE USED TO COMPENSATE DIFFERENT OUTPUT RESISTANCE

BATTERY CURRENT SENSE



MMM, BATTERY CURRENT SENSE

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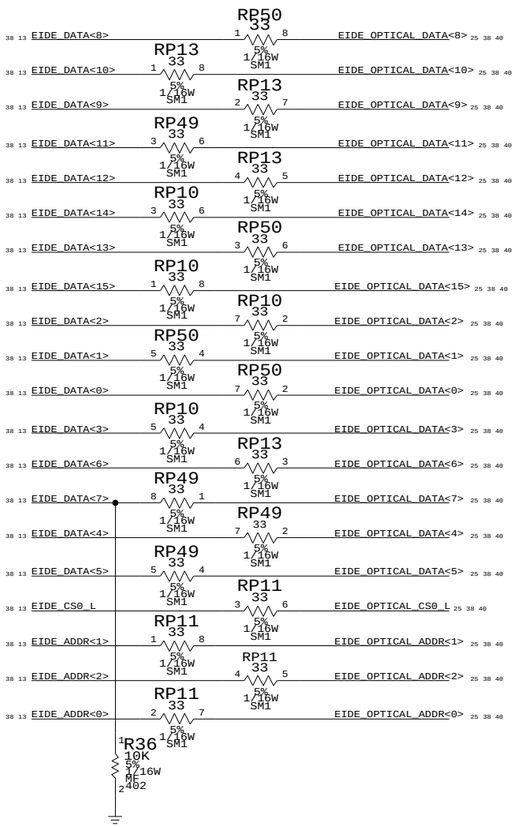
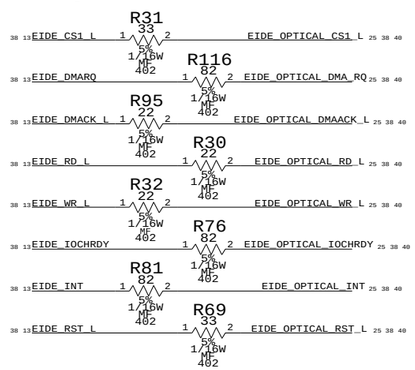
HARD DRIVE INTERFACE (UATA100)

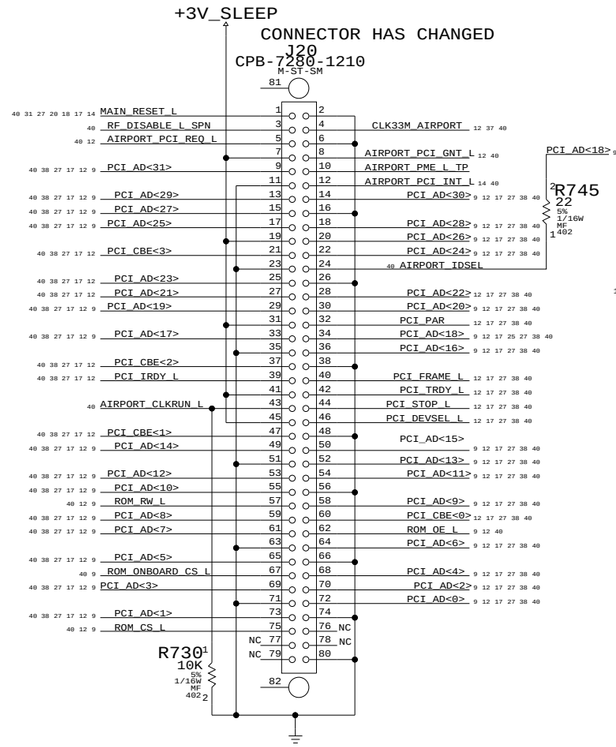
EIDE SERIES TERMINATION

PLACE TERMINATORS NEAR INTREPID

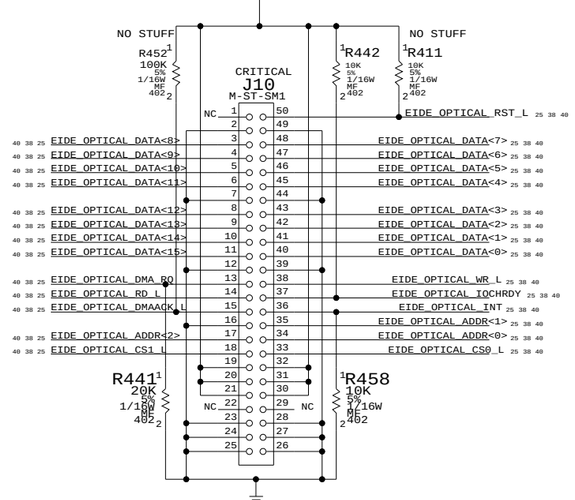




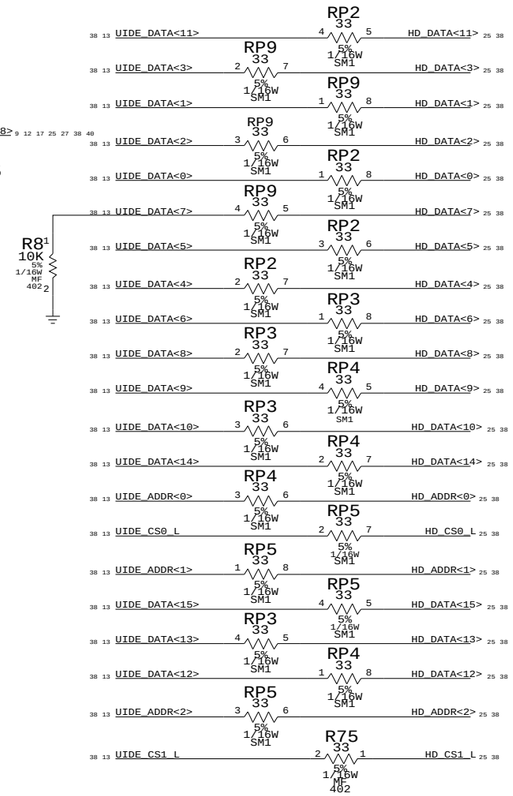
WIRELESS INTERFACE



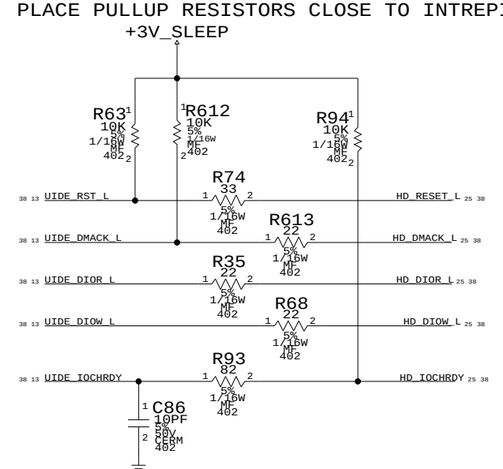
OPTICAL DRIVE INTERFACE (EIDE)



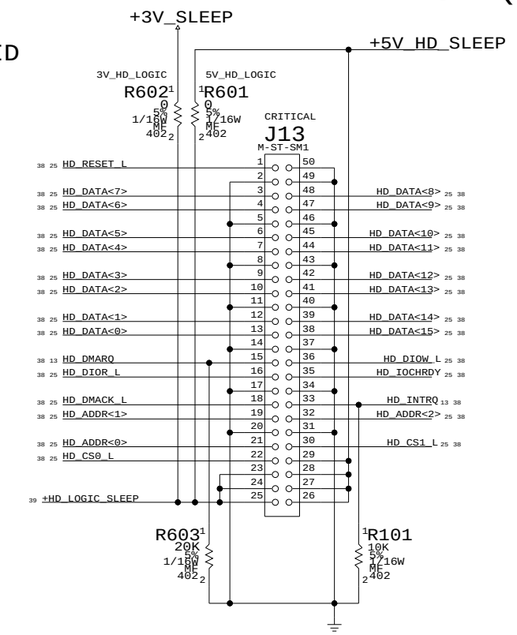
PLACE SERIES R CLOSE TO INTERPID



PLACE PULLUP RESISTORS CLOSE TO INTREPID

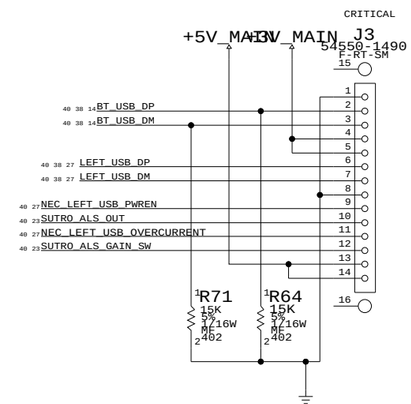


IOCHRDY - UATA100 REQUIRES PULL-UP TO 3.3V



ANY SEQUENCING REQUIREMENT BETWEEN
+5V_HD_SLEEP AND +3V_SLEEP?

BLUETOOTH/LEFT-SIDE USB



INTERNAL I/O CONNECTORS

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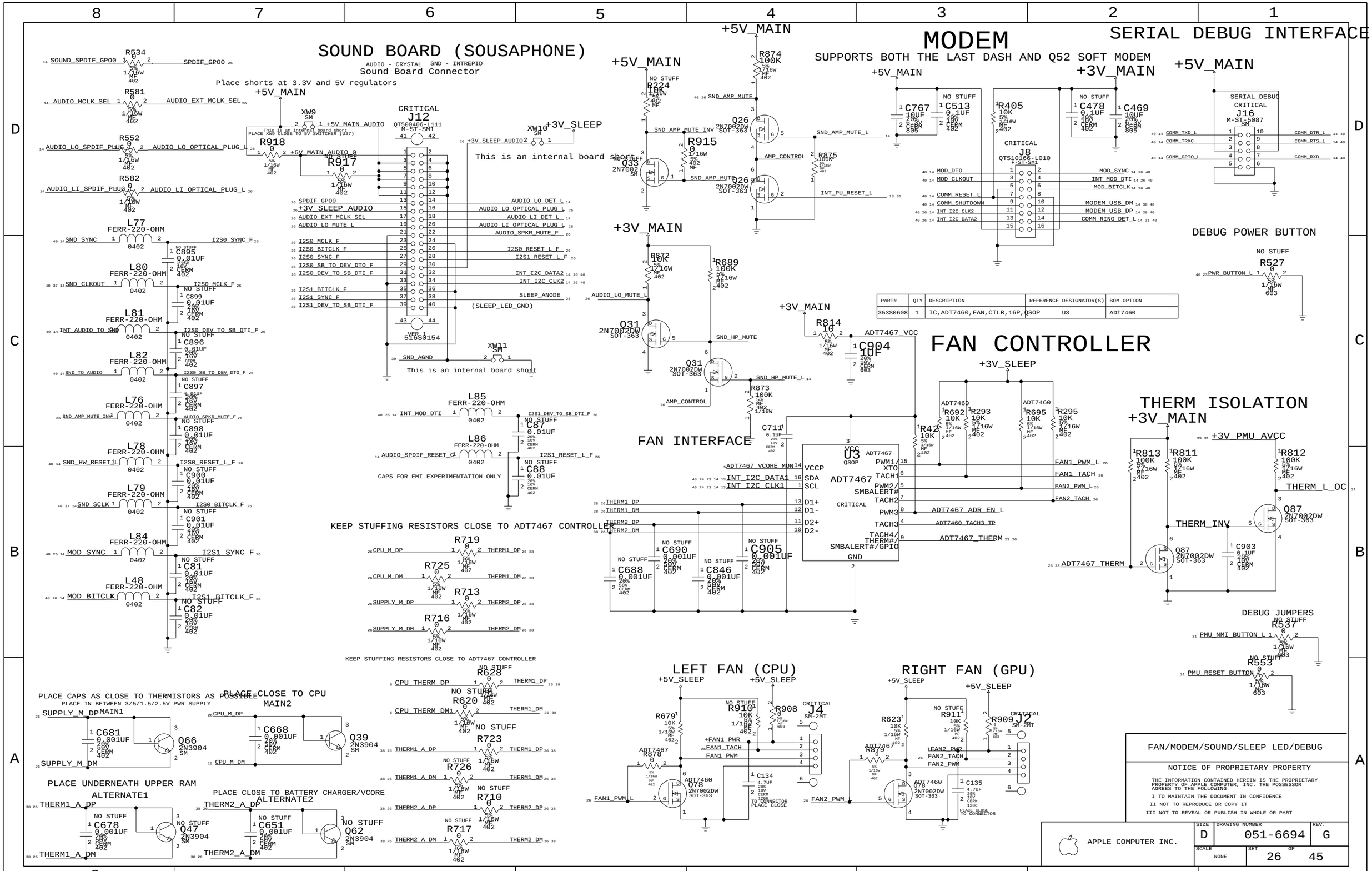

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
353S0608	1	IC,ADT7460,FAN,CTLR,16P,QSOP	U3	ADT7460

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,LW PROF,30.0000MHZ,8X4.5MM,SMD	Y5	CRITICAL	NEC_USB

Y7 LOAD CAPACITANCE IS 16PF

CRITICAL

Low/Full/High Speed (External)

CRITICAL

NEC_USB

U39

NEC_UPD720101_USB2

FBGA

Low/Full/High Speed (External)

SERR_L AND PERR_L
HAS DEDICATED PULL-UP
FOR BOTH CBUS AND USB2

Series Rpaks required to facilitate NAND-tree testing

Tie to GND at ball N11

NEED PULL-UP RESISTORS IN CASE USB 1.0 IS USED FOR PORT POWER

PLACE NEAR J3

SUTRO CONNECTOR

PLACE NEAR J12

BUBBA CONNECTOR

INTREPID USB CONSTRAINTS

USB_DAM	USB_DA	5 MIL SPACING
USB_DAP	USB_DA	5 MIL SPACING
USB_DCM	USB_DC	5 MIL SPACING
USB_DCP	USB_DC	5 MIL SPACING
USB_D1M	USB_D1	5 MIL SPACING
USB_D1P	USB_D1	5 MIL SPACING
USB_D2M	USB_D2	5 MIL SPACING
USB_D2P	USB_D2	5 MIL SPACING

USB 2.0

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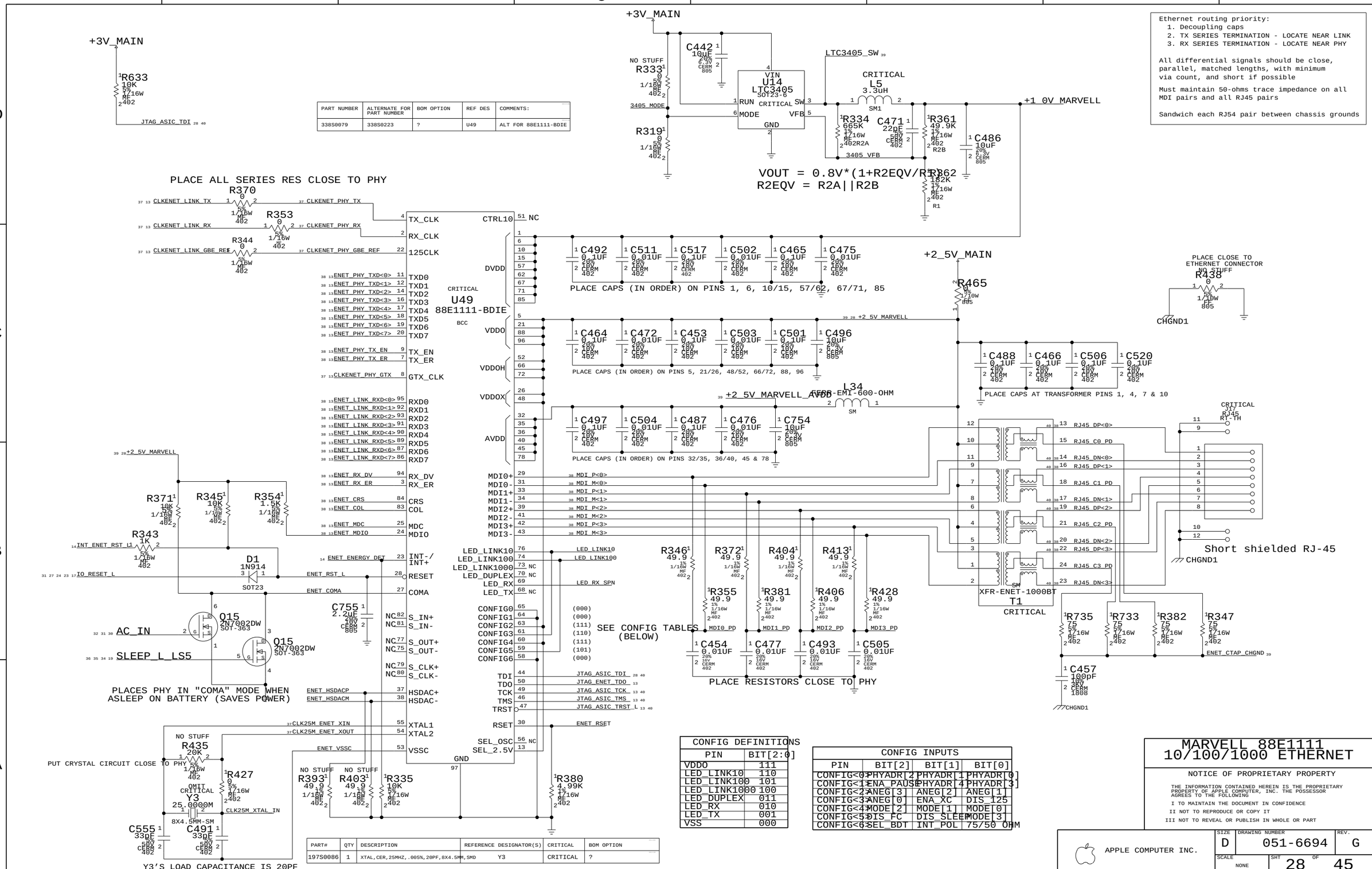

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
338S0079	338S0223	?	U49	ALT FOR 88E1111-BDIE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0086	1	XTAL,CER,25MHZ,.005%,20PF,8X4.5MM,SMD	Y3	CRITICAL	?

CONFIG DEFINITIONS

PIN	BIT[2:0]
VDDO	111
LED_LINK10	110
LED_LINK100	101
LED_LINK1000	100
LED_DUPLEX	011
LED_RX	010
LED_TX	001
VSS	000

CONFIG INPUTS

PIN	BIT[2]	BIT[1]	BIT[0]
CONFIG<0>	PHYADR[2]	PHYADR[1]	PHYADR[0]
CONFIG<1>	ENA_PAUSE	PHYADR[4]	PHYADR[3]
CONFIG<2>	ANEG[3]	ANEG[2]	ANEG[1]
CONFIG<3>	ANEG[0]	ENA_XC	DIS_125
CONFIG<4>	MODE[2]	MODE[1]	MODE[0]
CONFIG<5>	DIS_FC	DIS_SLEEP	MODE[3]
CONFIG<6>	SEL_BDT	INT_POL	75/50 OHM

MARVELL 88E1111 10/100/1000 ETHERNET

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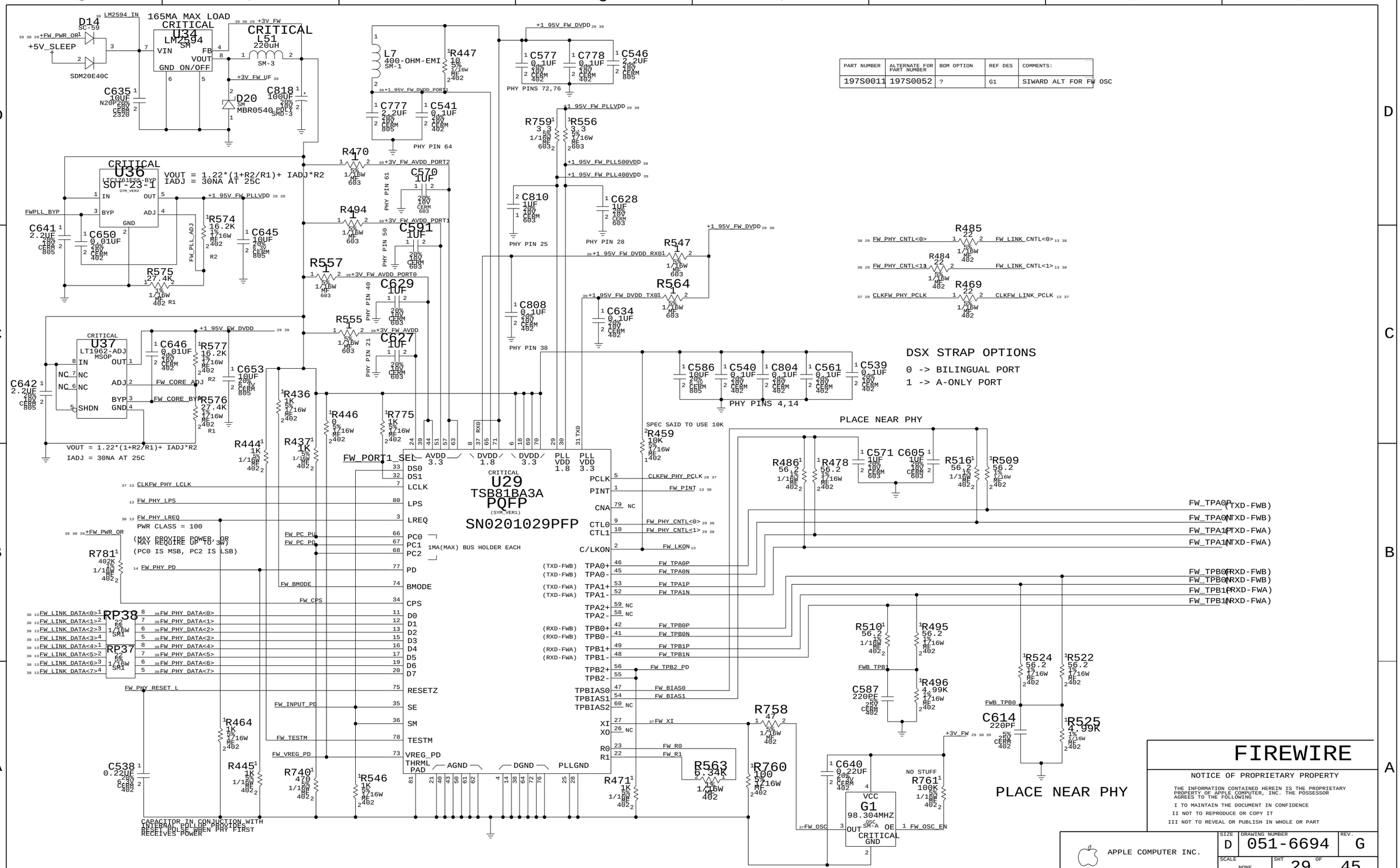
D	051-6694	G
SCALE NONE	SHT 28 OF 45	



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
197S0011	197S0052	?	G1	SIWARD ALT FOR FW OSC

FIREWIRE

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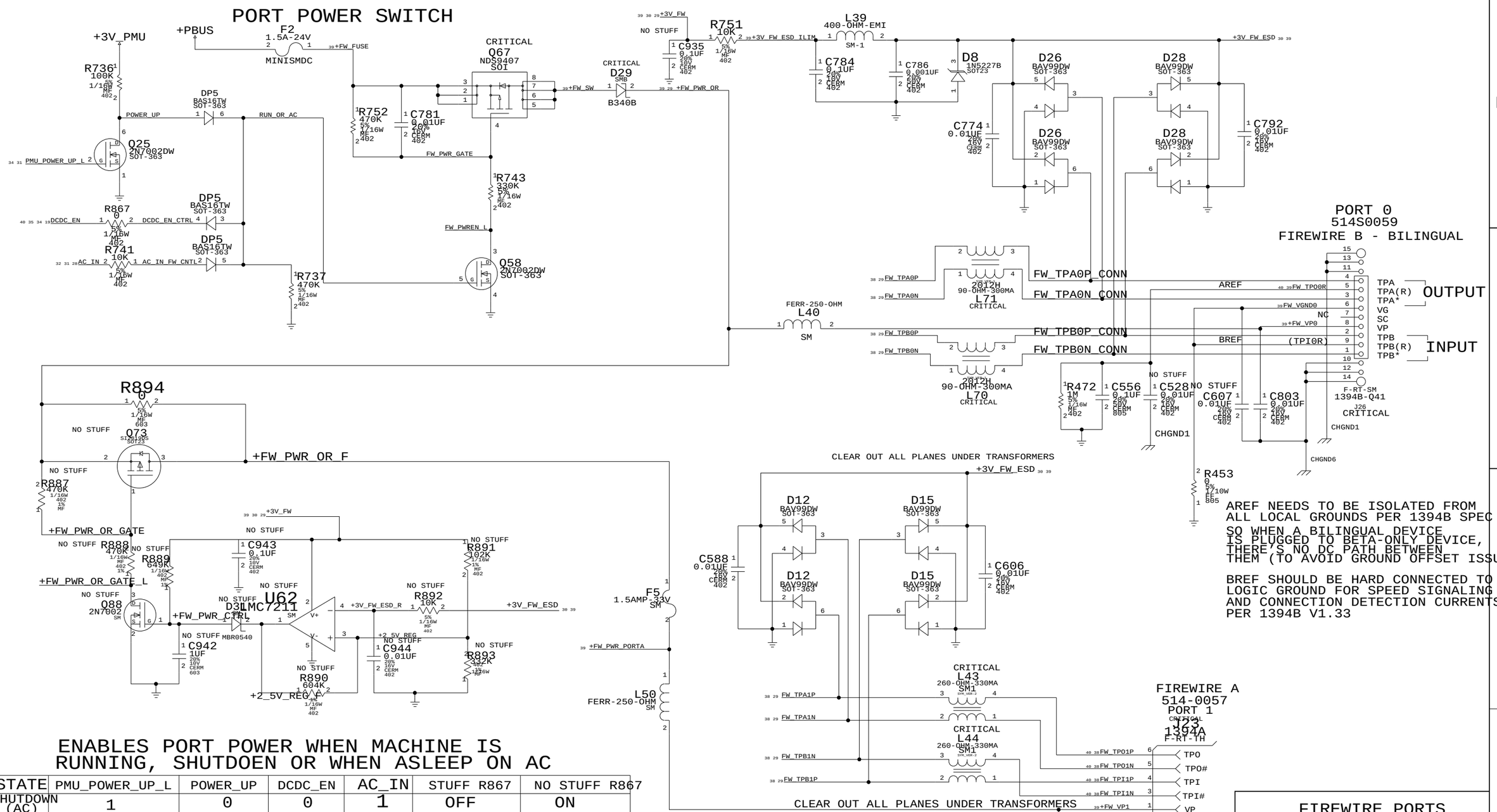
PORT POWER SWITCH



AREF NEEDS TO BE ISOLATED FROM ALL LOCAL GROUNDS PER 1394B SPEC SO WHEN A BILINGUAL DEVICE IS PLUGGED TO BETA-ONLY DEVICE, THERE'S NO DC PATH BETWEEN THEM (TO AVOID GROUND OFFSET ISSUE)

BREF SHOULD BE HARD CONNECTED TO LOGIC GROUND FOR SPEED SIGNALING AND CONNECTION DETECTION CURRENTS PER 1394B V1.33

ENABLES PORT POWER WHEN MACHINE IS RUNNING, SHUTDOEN OR WHEN ASLEEP ON AC

STATE	PMU_POWER_UP_L	POWER_UP	DCDC_EN	AC_IN	STUFF R867	NO STUFF R867
SHUTDOWN (AC)	1	0	0	1	OFF	ON
SLEEP (AC)	1	0	1	1	ON	ON
RUN (AC)	0	1	1	1	ON	ON
SHUTDOWN (BATT)	1	0	0	0	OFF	OFF
SLEEP (BATT)	1	0	1	0	OFF (PULL-DOWN RESISTOR)	OFF (PULL-DOWN RESISTOR)
RUN (BATT)	0	1	1	0	ON	ON
	2.99V	+3V_PMU	+4_6V_BU	+3V_PMU		

FIREWIRE PORTS

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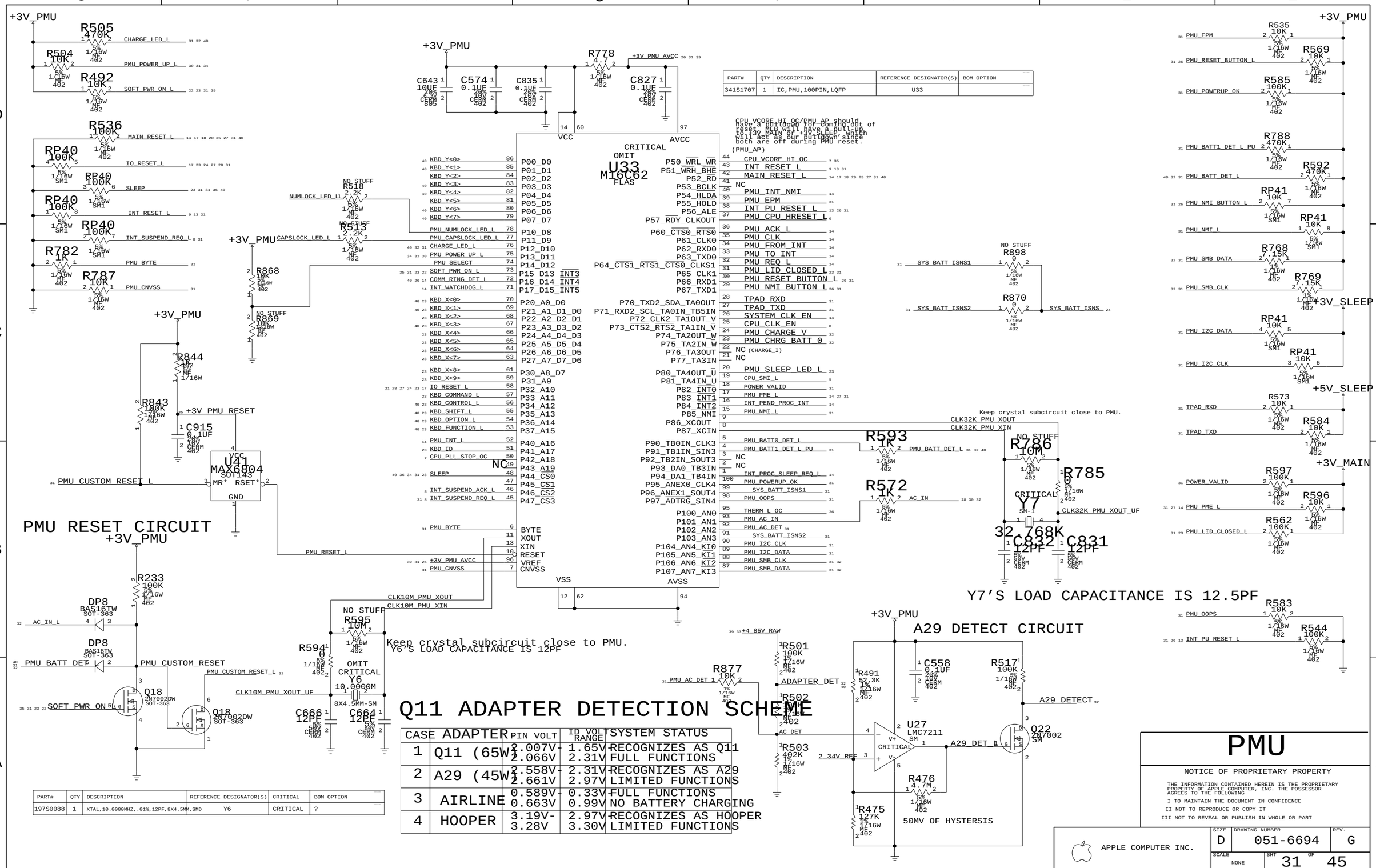
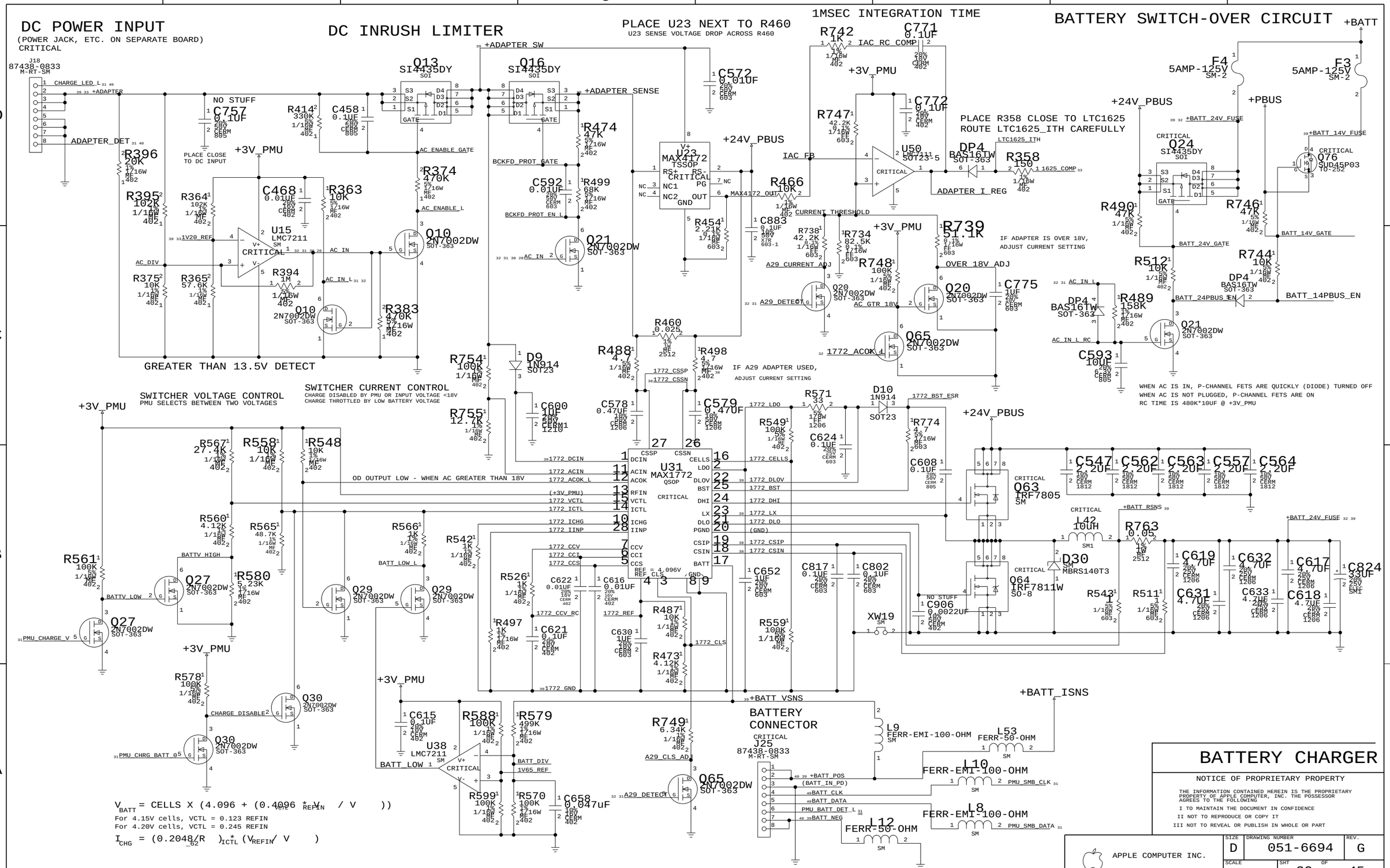


PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
341S1707	1	IC,PMU,100PIN,LQFP	U33	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0088	1	XTAL,10.0000MHZ,.01%,12PF,8X4.5MM,SMD	Y6	CRITICAL	?


DC POWER INPUT
(POWER JACK, ETC. ON SEPARATE BOARD)
CRITICAL
DC INRUSH LIMITER
PLACE U23 NEXT TO R460
U23 SENSE VOLTAGE DROP ACROSS R460
1MSEC INTEGRATION TIME
BATTERY SWITCH-OVER CIRCUIT
PLACE R358 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY
GREATER THAN 13.5V DETECT
SWITCHER VOLTAGE CONTROL
PMU SELECTS BETWEEN TWO VOLTAGES
SWITCHER CURRENT CONTROL
CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V
CHARGE THROTTLED BY LOW BATTERY VOLTAGE
IF A29 ADAPTER USED,
ADJUST CURRENT SETTING
IF ADAPTER IS OVER 18V,
ADJUST CURRENT SETTING
WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU
OD OUTPUT LOW - WHEN AC GREATER THAN 18V
BATTERY CONNECTOR
J25
87438-0833
M-RT-SM
U31
MAX1772
QSOP
U23
MAX4172
TSSOP
U15
LMC7211
U38
LMC7211
Q63
IRF7805
Q64
IRF7811W
D30
MBRS140T3
L42
10UH
R763
0.05
XW19
+BATT_ISNS
+BATT_VSNS
+BATT_POS
(BATT_IN_PD)
BATT_CLK
BATT_DATA
PMU_BATT_DET_L
BATT_NEG
PMU_SMB_CLK
PMU_SMB_DATA
L9
FERR-EMI-100-OHM
L53
FERR-50-OHM
L10
FERR-EMI-100-OHM
L8
FERR-EMI-100-OHM
L12
FERR-50-OHM
V_{BATT} = CELLS X (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))
For 4.15V cells, VCTL = 0.123 REFIN
For 4.20V cells, VCTL = 0.245 REFIN
I_{CHG} = (0.2048/R_{62}) * I_{CTL} (V_{REFIN} / V)
BATTERY CHARGER
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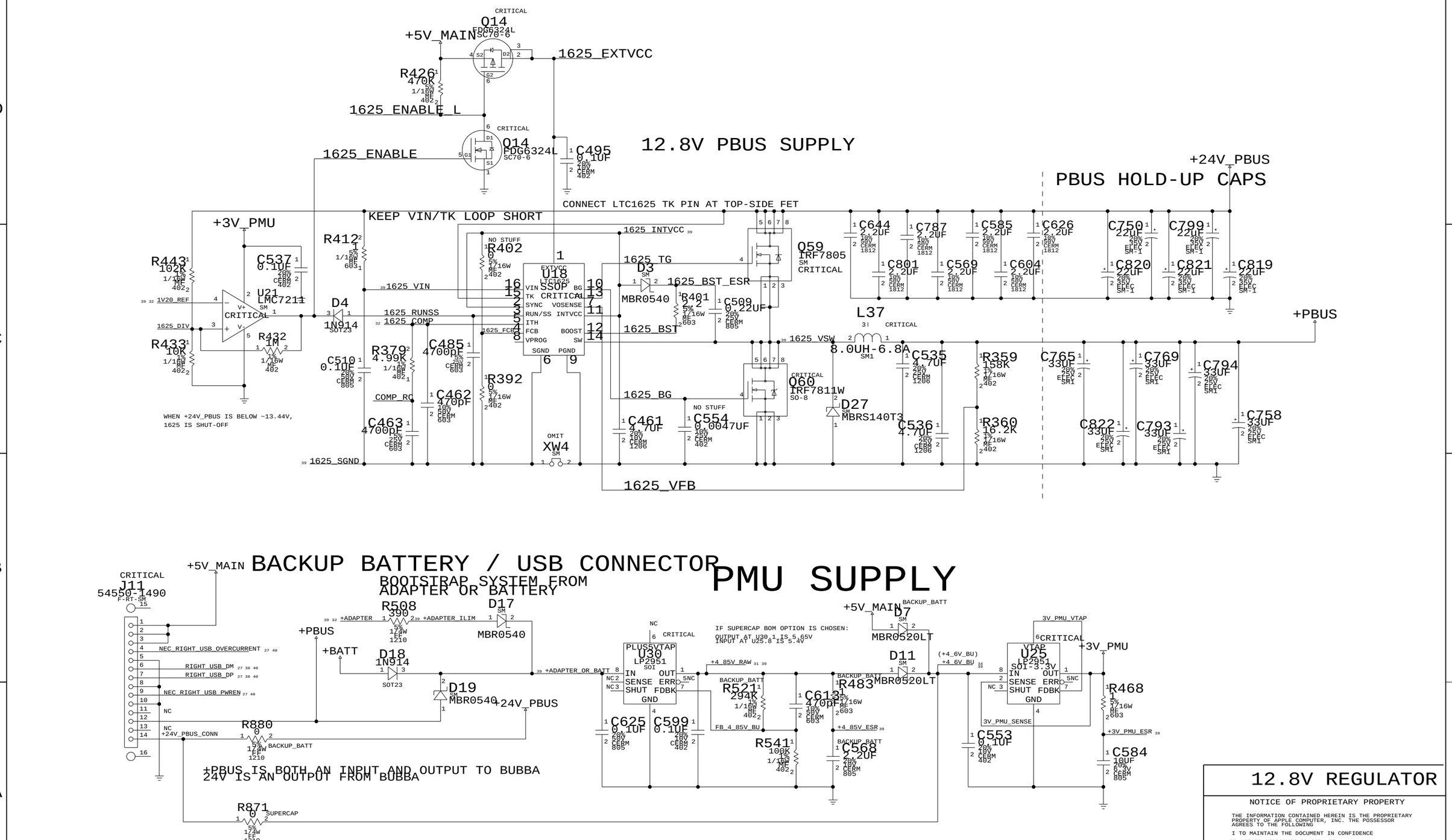
SIZE D
DRAWING NUMBER 051-6694
REV. G
SCALE NONE
SHT 32 OF 45



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S3575	1	RES,MF,1/16W/357K OHM,1%,0402,SMD	R521	?	SUPERCAP

12.8V REGULATOR

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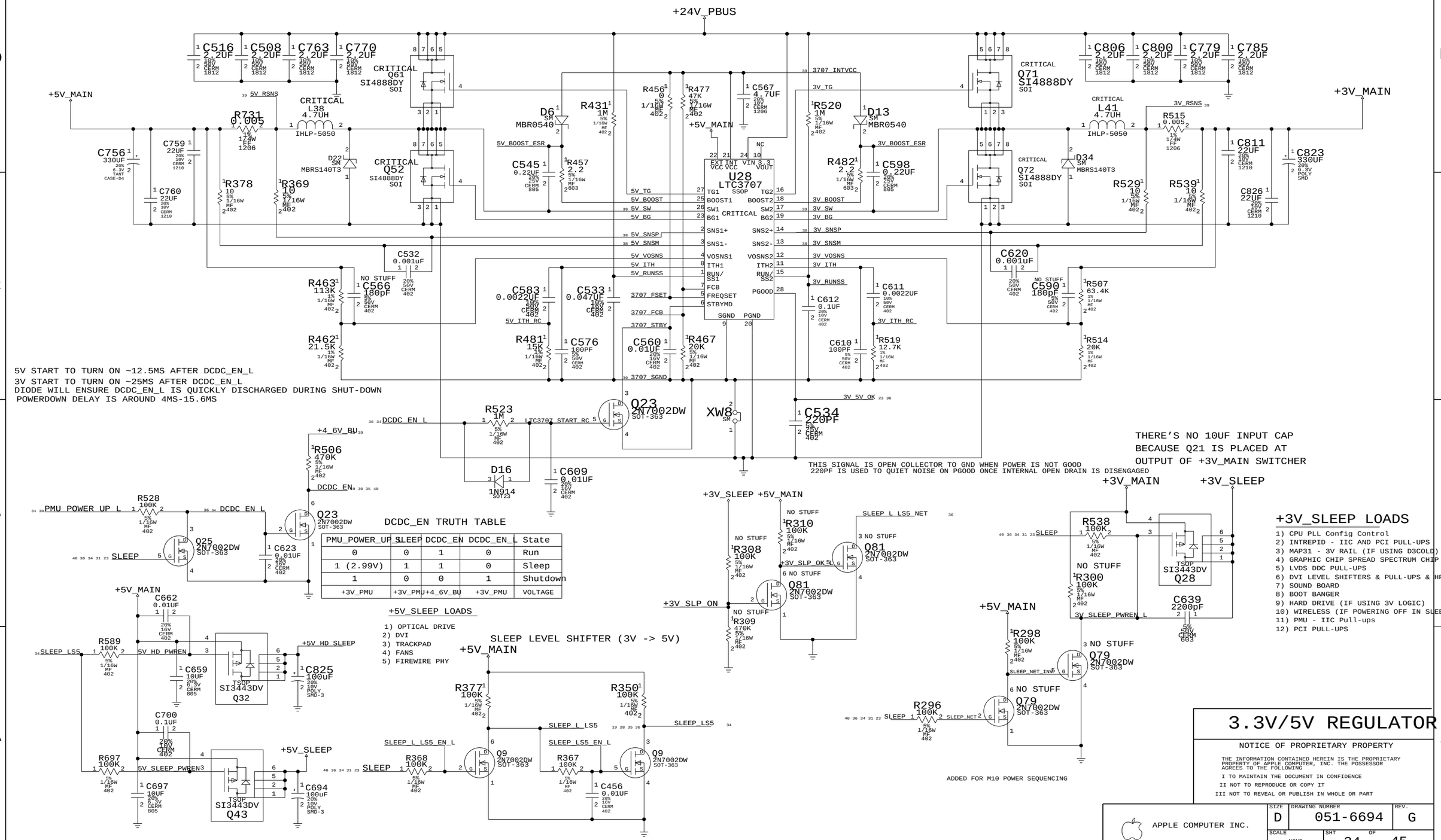
3.3V/5V MAIN SUPPLY



PMU_POWER_UP_L	SLEEP	DCDC_EN	DCDC_EN_L	State
0	0	1	0	Run
1 (2.99V)	1	1	0	Sleep
1	0	0	1	Shutdown
+3V_PMU	+3V_PMU	+4_6V_BU	+3V_PMU	VOLTAGE

3.3V/5V REGULATOR

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VCORE POWER SEQUENCING

CPU core follows CPU I/O voltage
(approx. 7ms delay)

1.67GHZ (WITHOUT VCORE OFFSET) 1.300V -> 0.975V

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
152S0242	1	IND,PWR,1.0UH,20,20.5A,SMD	L36	CRITICAL	

SEL = 0; Y1=A1
SEL = 1; Y1=B1

Keep trace fat (40-100 mils) and short!!

Keep trace fat and short!!

Connect MAX1717 GND pin 13 to GND at bottom-side FET

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

1.67GHZ (WITH VCORE OFFSET) 1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S4023	1	RES,4.02KOHM,1%,1/16W,0402,LF	R321	VCORE13
114S2433	1	RES,2.43KOHM,1%,1/16W,0402,LF	R809	VCORE13

OUTPUT VOLTAGE

VDAC D4=0	VDAC D4=1	D3	D2	D1	D0
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, VB = V .

FMAX CONNECTOR

J5 M-ST-SM-52465-1217

Pin	Signal	Pin	Signal
1		12	VCORE_VID<0>
2		11	VCORE_VID<1>
3	VCORE_GNDDIV_TEST	10	VCORE_VID<2>
4	VCORE_GNDSNS_TEST	9	VCORE_VID<3>
5	+3V_PMU_RESET	8	VCORE_VID<4>
6	SOFT_PWR_ON_L	7	
NC (RFU)			

VCORE SUPPLY

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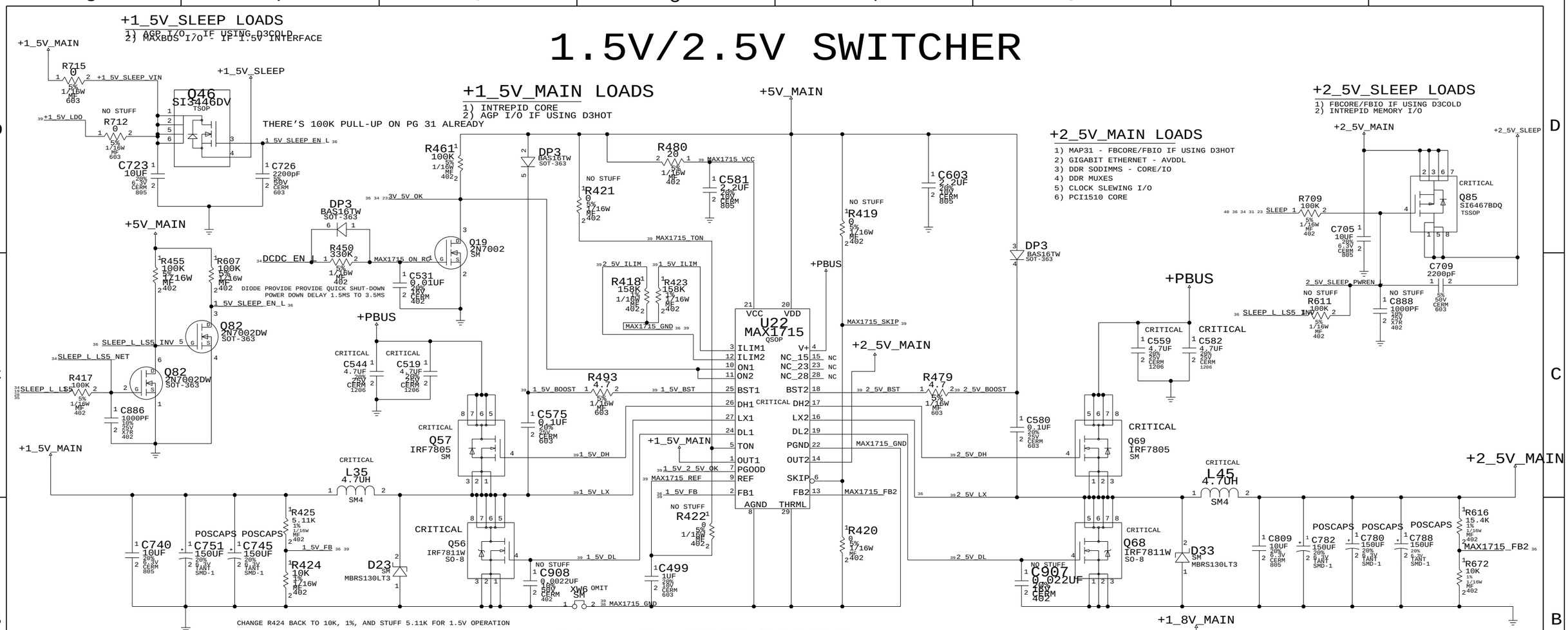
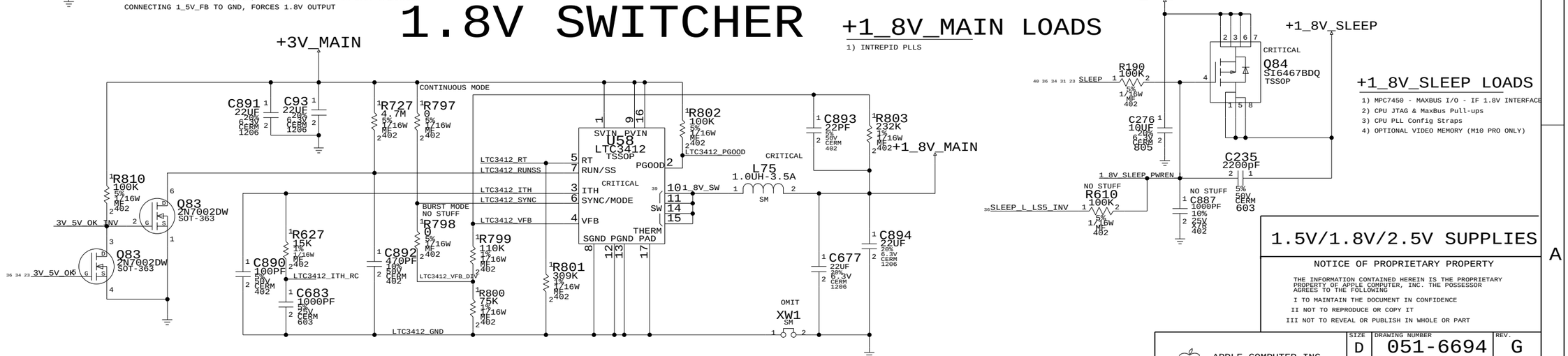
1.5V/2.5V SWITCHER



1.8V SWITCHER



1.5V/1.8V/2.5V SUPPLIES

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DIGITAL SIGNALS

GROUP	SIG_NAME	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
MAXBUS	CPU_AACK_L			250.0000	10 MIL SPACING			5 8
	CPU_ADDR<0..31>	5		250			83 MHZ	5 8
	CPU_ARTRY_L			250.0000	10 MIL SPACING			5 8
	CPU_BG_L			250.0000	10 MIL SPACING			5 8
	CPU_BR_L			250.0000	10 MIL SPACING			5 8
	CPU_CI_L	5		250.0000				5 8
	CPU_DATA<0..31>	5		250			83 MHZ	6 8
	CPU_DATA<32..63>	5		250			83 MHZ	6 8
	CPU_DBG_L	5		250.0000	10 MIL SPACING			5 8
	CPU_DTI<0..2>	5		250				5 8
	CPU_DRDY_L_UF				10 MIL SPACING			
	CPU_DRDY_L			250.0000	10 MIL SPACING			5 8
	CPU_GBL_L	5		250.0000				5 8
	CPU_HIT_L			250.0000	10 MIL SPACING			5 8
	CPU_QACK_L	5		250.0000	10 MIL SPACING			5 8
	CPU_QREQ_L			250.0000	10 MIL SPACING			5 8
	CPU_TA_L			250.0000	10 MIL SPACING			5 8
	CPU_TBST_L	5		250.0000	10 MIL SPACING			5 8
	CPU_TEA_L			250.0000				5 8
	CPU_TS_L			250.0000	10 MIL SPACING			5 8
	CPU_TSIZ<0..2>	5		250				5 8
	CPU_TT<0..4>	5		250				5 8
	CPU_WT_L	5		250.0000				5 8
GROUP 0	MEM_DATA<7..0>	4		200			167 MHZ	9 10
	RAM_DATA_A<7..0>	4		200			167 MHZ	10 11
	RAM_DATA_B<7..0>	4		200			167 MHZ	10 11
	MEM_DQS<0>		TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<0>	4		200				10 11
	RAM_DQS_B<0>	4		200				10 11
	MEM_DQM<0>	4		200				9 10
	RAM_DQM_A<0>	4		200				10 11
	RAM_DQM_B<0>	4		200				10 11
GROUP 1	MEM_DATA<15..8>	4		200			167 MHZ	9 10
	RAM_DATA_A<15..8>	4		200			167 MHZ	10 11
	RAM_DATA_B<15..8>	4		200			167 MHZ	10 11
	MEM_DQS<1>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<1>	4		200				10 11
	RAM_DQS_B<1>	4		200				10 11
	MEM_DQM<1>			200				9 10
	RAM_DQM_A<1>	4		200				10 11
	RAM_DQM_B<1>	4		200				10 11
GROUP 2/3	MEM_DATA<31..16>	4		200			167 MHZ	9 10
	RAM_DATA_A<31..16>	4		200			167 MHZ	10 11
	RAM_DATA_B<31..16>	4		200			167 MHZ	10 11
	MEM_DQS<3..2>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
DDR RAM	RAM_DQS_A<3..2>	4		200			167 MHZ	10 11
	RAM_DQS_B<3..2>	4		200			167 MHZ	10 11
	MEM_DQM<3..2>	4		200			167 MHZ	9 10
	RAM_DQM_A<3..2>	4		200			167 MHZ	10 11
	RAM_DQM_B<3..2>	4		200			167 MHZ	10 11
GROUP 4/5	MEM_DATA<47..32>	4		200			167 MHZ	9 10
	RAM_DATA_A<47..32>	4		200			167 MHZ	10 11
	RAM_DATA_B<47..32>	4		200			167 MHZ	10 11
	MEM_DQS<5..4>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200			167 MHZ	9 10
	RAM_DQS_A<5..4>	4		200			167 MHZ	10 11
	RAM_DQS_B<5..4>	4		200			167 MHZ	10 11
	MEM_DQM<5..4>	4		200			167 MHZ	9 10
	RAM_DQM_A<5..4>	4		200			167 MHZ	10 11
	RAM_DQM_B<5..4>	4		200			167 MHZ	10 11
GROUP 6	MEM_DATA<55..48>	4		200			167 MHZ	9 10
	RAM_DATA_A<55..48>	4		200			167 MHZ	10 11
	RAM_DATA_B<55..48>	4		200			167 MHZ	10 11
	MEM_DQS<6>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<6>			200				10 11
	RAM_DQS_B<6>	4		200				10 11
	MEM_DQM<6>			200				9 10
	RAM_DQM_A<6>	4		200				10 11
	RAM_DQM_B<6>	4		200				10 11
GROUP 7	MEM_DATA<63..56>	4		200			167 MHZ	9 10
	RAM_DATA_A<63..56>	4		200			167 MHZ	10 11
	RAM_DATA_B<63..56>	4		200			167 MHZ	10 11
	MEM_DQS<7>	4	TOTAL LENGTH CONTROLLED BY SPREADSHEET	200				9 10
	RAM_DQS_A<7>			200				10 11
	RAM_DQS_B<7>			200				10 11
	MEM_DQM<7>	4		200				9 10
	RAM_DQM_A<7>	4		200				10 11
	RAM_DQM_B<7>	4		200				10 11
ADDR	MEM_ADDR<12..0>	4					83 MHZ	9
	RAM_ADDR<12..0>	6		200				9 11
	MEM_BA<1..0>	4						9
	RAM_BA<1..0>	6		200				9 11
CONTROL	MEM_CS_L<3..0>	4						9
	RAM_CS_L<3..0>	6		200				9 11
	MEM_CKE<3..0>	4						9
	RAM_CKE<3..0>	6		200				9 11
	MEM_RAS_L	4						9
	RAM_RAS_L			200.0000				9 11
	MEM_CAS_L	4						9
	RAM_CAS_L			200.0000				9 11
	MEM_WE_L	4						9
	RAM_WE_L			200.0000				9 11
	MEM_MUXSEL_H<1..0>	3						9 10
	MEM_MUXSEL_L<1..0>	3						9 10
	RAM_MUXSEL_H	5						10
	RAM_MUXSEL_L	5						10

CLOCK LINE CONSTRAINTS

GROUP	SIG_NAME		MAX VIAS	MAX EXPOSED LENGTH	STUB_LENGTH	NET_SPACING_TYPE	PULSE PARAM	
INTREPID CLOCKS	SYSCLK_CPU_UF					10 MIL SPACING		8
	SYSCLK_CPU		4		200.0000	10 MIL SPACING		5 8
	INT_CPUFB_OUT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_SHORT		3			10 MIL SPACING		8
	INT_CPUFB_OUT_NORM		3			10 MIL SPACING		8
	INT_CPUFB_IN_NORM		3			10 MIL SPACING		8
	INT_CPUFB_LONG		3			10 MIL SPACING		8
	INT_CPUFB_IN				200.0000	10 MIL SPACING		8
	SYSCLK_DDRCLK_A0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B0_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_B1_L_UF		3		200.0000	10 MIL SPACING		9
	SYSCLK_DDRCLK_A0	DDRCLK_A0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A0_L	DDRCLK_A0			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1	DDRCLK_A1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_A1_L	DDRCLK_A1			200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B0_L	DDRCLK_B0	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	SYSCLK_DDRCLK_B1_L	DDRCLK_B1	3		200.0000	10 MIL SPACING		9 11
	INT_REF_CLK_OUT		3		200.0000	10 MIL SPACING		14
	INT_REF_CLK_IN				200.0000	10 MIL SPACING		14
	CLK66M_GPU_AGP_UF				200.0000	10 MIL SPACING		12
	CLK66M_GPU_AGP		4		200.0000	10 MIL SPACING		12 18
	INT_AGP_FB_OUT				200.0000	10 MIL SPACING		12
	INT_AGP_FB_IN		4		200.0000	10 MIL SPACING		12
	CLK33M_CBUS_UF				200.0000	10 MIL SPACING		12
	CLK33M_CBUS	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 17
	CLK33M_AIRPORT_UF				200.0000	10 MIL SPACING		12
	CLK33M_AIRPORT	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 25 40
	CLK33M_USB2_UF				200.0000	10 MIL SPACING		12
	CLK33M_USB2	SHOULD BE AT MOST 4 VIAS FOR CLK	6		200.0000	10 MIL SPACING		12 27
	INT_PCI_FB_OUT				200.0000	10 MIL SPACING		12
	INT_PCI_FB_IN		3		200.0000	10 MIL SPACING		12
MAP31	GPU_CLK27M_OUT					10 MIL SPACING		
	GPU_CLK27M_UF					10 MIL SPACING		
	GPU_SSCLK_UF					10 MIL SPACING		
	GPU_SSCLK_IN					10 MIL SPACING		
	GPU_FBCLK0					10 MIL SPACING		
	GPU_FBCLK0_L					10 MIL SPACING		
	GPU_FBCLK1					10 MIL SPACING		
	GPU_FBCLK1_L					10 MIL SPACING		
	GPU_DVO_CLKP					10 MIL SPACING		19
CRYSTALS	CLK27M_GPU_XOUT					10 MIL SPACING		
	CLK27M_XTAL_IN					10 MIL SPACING		
	CLK27M_GPU_XIN					10 MIL SPACING		
	CLK18M_INT_XIN					10 MIL SPACING		14
	CLK18M_INT_XOUT					10 MIL SPACING		14
	CLK18M_XTAL_IN					10 MIL SPACING		14
	CLK18M_INT_EXT					10 MIL SPACING		14
	CLK25M_ENET_XIN					10 MIL SPACING		28
	CLK25M_ENET_XOUT					10 MIL SPACING		28
	NEC_XT1					10 MIL SPACING		27
	NEC_XT2	THERE'S ANOTHER 280MIL LEG				10 MIL SPACING		27
SOUND	SND_SCLK		7		200.0000	10 MIL SPACING		14 26 40
	SND_CLKOUT				200.0000	10 MIL SPACING		14 26 40
ETHERNET MARVELL	CLKENET_PHY_RX				200.0000			28
	CLKENET_LINK_RX		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_GBE_REF				200.0000			28
	CLKENET_LINK_GBE_REF		3		200.0000	10 MIL SPACING		13 28
	CLKENET_PHY_TX				200.0000			28
	CLKENET_LINK_TX		5		200.0000	10 MIL SPACING		13 28
	CLKENET_LINK_GTX				200.0000			13
	CLKENET_PHY_GTX		3		200.0000	10 MIL SPACING		13 28
FIREWIRE	CLKFW_PHY_PCLK				200.0000			29
	CLKFW_LINK_PCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_PHY_LCLK		3		200.0000	10 MIL SPACING		13 29
	CLKFW_LINK_LCLK				200.0000			13
	FW_XI				200.0000	10 MIL SPACING		29
	FW_OSC				200.0000	10 MIL SPACING		29

SIGNAL CONSTRAINTS - PAGE 1

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SCALE NONE	SHT 37 OF 45	

Digital Signals (cont'd)

GROUP	SIG_NAME	DELAY_RULE	MAX_VIAS	MAX_EXPOSED_LENGTH	STUB_LENGTH	NET_SPACING_TYPE	NO_TEST	PULSE_PARAM	
AGP	AGP_AD<15..0>		5	100				66 MHZ	12 18
AGP BYTES 0-1	AGP_CBE<1..0>		5	100				66 MHZ	12 18
	AGP_AD_STB<0>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<0>		5	100		8 MIL SPACING			12 18
AGP BYTES 2-3	AGP_AD<31..16>		5	100				66 MHZ	12 18
	AGP_CBE<3..2>		5	100				66 MHZ	12 18
	AGP_AD_STB<1>		5	100		8 MIL SPACING			12 18
	AGP_AD_STB_L<1>			100		8 MIL SPACING			12 18
AGP SIDEBAND	AGP_SBA<7..0>		5	100				66 MHZ	12 18
	AGP_SB_STB			100.0000		8 MIL SPACING			12 18
	AGP_SB_STB_L		5	100.0000		8 MIL SPACING			12 18
AGP CONTROL	AGP_FRAME_L			250.0000					12 18
	AGP_IRDY_L			250.0000					12 18
	AGP_TRDY_L		6	250.0000					12 18
	AGP_DEVSEL_L			250.0000					12 18
	AGP_STOP_L		6	250.0000					12 18
	AGP_PAR		6	250.0000					12 18
	AGP_REQ_L			285.0000					12 18
	AGP_GNT_L			250.0000					12 18
	AGP_RBF_L			250.0000					12 18
DVO	GPU_DVOD<0..23>		5	250					19 20
	GPU_DVO_HSYNC								19 20
	GPU_DVO_VSYNC								19 20
PCI	PCI_AD<31..0>					MIN_DAISY_CHAIN		33 MHZ	9 12 17 25 27 40
	PCI_CBE<3..0>					MIN_DAISY_CHAIN		33 MHZ	12 17 25 27 40
	PCI_FRAME_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_IRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_TRDY_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_DEVSEL_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_STOP_L					MIN_DAISY_CHAIN			12 17 25 27 40
	PCI_PAR					MIN_DAISY_CHAIN			12 17 25 27 40
ULTRA ATA-100	UIDE_DATA<15..8>				200			100 MHZ	13 25
	UIDE_DATA<7>			NEED TO MATCH DELAY TO 250	200				13 25
	UIDE_DATA<6..0>				200			100 MHZ	13 25
	UIDE_ADDR<2..0>				200			100 MHZ	13 25
	UIDE_RST_L				200.0000				13 25
	UIDE_DIOW_L				200.0000				13 25
	UIDE_DIOR_L			10 MIL SPACING	200.0000				13 25
	UIDE_DMACK_L				200.0000				13 25
	UIDE_CS0_L				200.0000				13 25
	UIDE_CS1_L				200.0000				13 25
	UIDE_DMARQ				200.0000				13
	UIDE_IOCHRDY			10 MIL SPACING	200.0000				13 25
	UIDE_INTRQ				200.0000				13
	HD_DATA<15..0>		5	TOTAL UIDE+HD SKEW <500MIL	200			100 MHZ	25
	HD_ADDR<2..0>		5		200			100 MHZ	25
	HD_RESET_L		5		200.0000				25
	HD_DIOW_L		5		200.0000				25
	HD_DIOR_L		5	10 MIL SPACING	200.0000				25
	HD_DMACK_L		5		200.0000				25
	HD_CS0_L		5		200.0000				25
	HD_CS1_L		5		200.0000				25
	HD_DMARQ				200.0000				13 25
	HD_IOCHRDY		5	10 MIL SPACING	200.0000				25
	HD_INTRQ		5						13 25
EIDE INTREPID	EIDE_DATA<15..0>							33 MHZ	13 25
	EIDE_ADDR<2..0>							33 MHZ	13 25
	EIDE_CS0_L								13 25
	EIDE_CS1_L								13 25
	EIDE_RD_L								13 25
	EIDE_WR_L								13 25
	EIDE_IOCHRDY								13 25
	EIDE_INT								13 25
	EIDE_RST_L								13 25
	EIDE_DMACK_L								13 25
	EIDE_DMARQ								13 25
OPTICAL	EIDE_OPTICAL_DATA<15..0>							33 MHZ	25 40
	EIDE_OPTICAL_ADDR<2..0>							33 MHZ	25 40
	EIDE_OPTICAL_CS0_L								25 40
	EIDE_OPTICAL_CS1_L								25 40
	EIDE_OPTICAL_RD_L								25 40
	EIDE_OPTICAL_WR_L								25 40
	EIDE_OPTICAL_IOCHRDY								25 40
	EIDE_OPTICAL_INT								25 40
	EIDE_OPTICAL_RST_L								25 40
	EIDE_OPTICAL_DMAACK_L								25 40
	EIDE_OPTICAL_DMA_RQ								25 40
ETHERNET MII	ENET_LINK_RXD<7..0>		5						13 28
	ENET_RX_DV								13 28
	ENET_RX_ER								13 28
	ENET_PHY_TXD<7..0>		5						13 28
	ENET_LINK_TXD<7..0>								13
	ENET_PHY_TX_ER		5						13 28
	ENET_LINK_TX_ER								13
	ENET_PHY_TX_EN		5						13 28
	ENET_LINK_TX_EN								13
	ENET_MDIO								13 28
	ENET_MDC								13 28
	ENET_COL								13 28
	ENET_CRS								13 28
FIREWIRE MII	FW_LINK_DATA<7..0>		5						13 29
	FW_PHY_DATA<7..0>		5						29
	FW_LINK_CNTL<1..0>								13 29
	FW_PHY_CNTL<1..0>								29
	FW_LINK_LREQ								13
	FW_PHY_LREQ								13 29
	FW_PINT								13 29

Differential Signals

GROUP	SIG_NAME	DIFFERENTIAL_PAIR	MAX_EXPOSED_LENGTH	NET_SPACING_TYPE	MAX_VIAS	
ETHERNET	MDI_M<0>	ENET_MDI0				28
	MDI_P<0>	ENET_MDI0				28
	MDI_M<1>	ENET_MDI1	SPACING DELETED BECAUSE			28
	MDI_P<1>	ENET_MDI1	OF PHYSICAL CONSTRAINTS			28
	MDI_M<2>	ENET_MDI2	AROUND MARVELL PHY			28
	MDI_P<2>	ENET_MDI2				28
	MDI_M<3>	ENET_MDI3				28
	MDI_P<3>	ENET_MDI3				28
	RJ45_DN<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DP<0>	RJ45_DP0		10 MIL SPACING		28 40
	RJ45_DN<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DP<1>	RJ45_DP1		10 MIL SPACING		28 40
	RJ45_DN<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DP<2>	RJ45_DP2		10 MIL SPACING		28 40
	RJ45_DN<3>	RJ45_DP3		10 MIL SPACING		28 40
	RJ45_DP<3>	RJ45_DP3		10 MIL SPACING		28 40
FIREWIRE	FW_TPA0N	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPA0P	FW_TPA0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB0N	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB0P	FW_TPB0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPI0N	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPI0P	FW_TPI0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0N	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPO0P	FW_TPO0		MIN_LINE_WIDTH=3.4 10 MIL SPACING		
	FW_TPA1N	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPA1P	FW_TPA1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB1N	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPB1P	FW_TPB1	500.0000	MIN_LINE_WIDTH=3.4 10 MIL SPACING		29 30
	FW_TPI1N	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPI1P	FW_TPI1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPO1N	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
	FW_TPO1P	FW_TPO1		MIN_LINE_WIDTH=3.4 10 MIL SPACING		30 40
LVDS LOWER	CLKLVDS_LN	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	CLKLVDS_LP	CLKLVDS_L		10 MIL SPACING	4	19 22 40
	LVDS_L0N	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L0P	LVDS_L0		10 MIL SPACING		19 22 40
	LVDS_L1N	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L1P	LVDS_L1		10 MIL SPACING		19 22 40
	LVDS_L2N	LVDS_L2		10 MIL SPACING		19 22 40
	LVDS_L2P	LVDS_L2		10 MIL SPACING		19 22 40
UPPER	CLKLVDS_UN	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	CLKLVDS_UP	CLKLVDS_U		10 MIL SPACING	4	19 22 40
	LVDS_U0N	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U0P	LVDS_U0		10 MIL SPACING		19 22 40
	LVDS_U1N	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U1P	LVDS_U1		10 MIL SPACING		19 22 40
	LVDS_U2N	LVDS_U2		10 MIL SPACING		19 22 40
	LVDS_U2P	LVDS_U2		10 MIL SPACING		19 22 40
TMDS	TMDS_CONN_CLKN	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CONN_CLKP	CLKCONN_TMDS		10 MIL SPACING	4	22 40
	TMDS_CLKN	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_CLKP	CLKTMDS		10 MIL SPACING	4	20 22
	TMDS_DN<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DP<0>	TMDS_D0		10 MIL SPACING		20 22 40
	TMDS_DN<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DP<1>	TMDS_D1		10 MIL SPACING		20 22 40
	TMDS_DN<2>	TMDS_D2		10 MIL SPACING		20 22 40
	TMDS_DP<2>	TMDS_D2		10 MIL SPACING		20 22 40
USB	NEC_USB_DAM	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DAP	NEC_USB_DA	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DEM	USB_DE		5 MIL SPACING		14
	USB_DEP	USB_DE		5 MIL SPACING		14
	NEC_USB_DBM	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_DBP	NEC_USB_DB	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	USB_DFM	USB_DF		5 MIL SPACING		14
	USB_DFP	USB_DF		5 MIL SPACING		14
	BT_USB_DM	BT_USB_D		5 MIL SPACING		14 25 40
	BT_USB_DP	BT_USB_D		5 MIL SPACING		14 25 40
	NEC_USB_RSDM1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP1	NEC_USB_RSD1	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDM2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	NEC_USB_RSDP2	NEC_USB_RSD2	MIN_LINE_WIDTH=5	10 MIL SPACING		27
	MODEM_USB_DM	MODEM_USB_D		5 MIL SPACING		14 26 40
	MODEM_USB_DP	MODEM_USB_D		5 MIL SPACING		14 26 40
	LEFT_USB_DM	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	LEFT_USB_DP	LEFT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		25 27 40
	RIGHT_USB_DM	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
	RIGHT_USB_DP	RIGHT_USB	MIN_LINE_WIDTH=5	10 MIL SPACING		27 33 40
POWER SUPPLIES	1772_CSSN	1772_CSS		DIFF		32
	1772_CSSP	1772_CSS		DIFF		32
	1772_CSIN	1772_CSI		DIFF		32
	1772_CSIP	1772_CSI		DIFF		32
	3V_SNSM	3V_SNS		DIFF		34
	3V_SNSP	3V_SNS		DIFF		34
	5V_SNSM	5V_SNS		DIFF		34
	5V_SNSP	5V_SNS		DIFF		34
THERMOSTAT	THERM1_DM	THERM1		DIFF		26
	THERM1_DP	THERM1		DIFF		26
	THERM2_DM	THERM2		DIFF		26
	THERM2_DP	THERM2		DIFF		26
	THERM1_M_DM	THERM1_MAIN		DIFF		
	THERM1_M_DP	THERM1_MAIN		DIFF		
	THERM2_M_DM	THERM2_MAIN		DIFF		
	THERM2_M_DP	THERM2_MAIN		DIFF		
	THERM1_A_DM	THERM1_ALT		DIFF		26
	THERM1_A_DP	THERM1_ALT		DIFF		26
	THERM2_A_DM	THERM2_ALT		DIFF		26
	THERM2_A_DP	THERM2_ALT		DIFF		26

INTERNAL LAYER
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.57OHM
ZDIFF = 99.8OHM

FOR FIREWIRE
ER = 4.3 (DIELECTRIC CONSTANT)
W = 3.4MIL (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 10MIL (SEPERATION OF DIFF TRACES)
ZSINGLE = 53.37OHM
ZDIFF = 107.17OHM

INTERNAL LAYER (USB1.1/USB 2.0)
ER = 4.3 (DIELECTRIC CONSTANT)
W = 4MIL(USB 1.1)/ 5MIL(USB 2.0) (TRACE WIDTH)
B = 12.2MIL (DIST BETW 2 GND PLANES)
T = 0.7MIL (TRACE THICKNESS)
S = 5MIL (USB 1.1) (SEPERATION OF DIFF TRACES)
S = 10MIL (USB 2.0) (SEPERATION OF DIFF TRACES)
ZSINGLE = 51.5OHM (USB 1.1)/ 46.2OHM (USB 2.0)
ZDIFF = 89.3OHM (USB 1.1)/ 89.4OHM (USB 2.0)

SIGNAL CONSTRAINTS - PAGE 2

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POWER NET CONSTRAINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
MAIN/SLEEP	+24V_PBUS	VOLTAGE=24V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+BATT	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+PBUS	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+5V_MAIN	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+5V_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	23
	+3V_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	20 23
	+3V_PMU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	+2_5V_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+2_5V_SLEEP	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_8V_MAIN	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	40
	+1_8V_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_MAIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_SLEEP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	+1_5V_LDO	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
	+1_5V_SLEEP_VIN	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	36
ADAPTER	+ADAPTER	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32 33
	+ADAPTER_SW	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
	+ADAPTER_SENSE	VOLTAGE=24V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	32
BATTERY CHARGER	+BATT_POS	VOLTAGE=16.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	BATT_NEG	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32 40
	1772_DCIN	VOLTAGE=24V	MIN_LINE_WIDTH=10		32
	1772_LX	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_14V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_24V_FUSE	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_RSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	32
	+BATT_VSNS	VOLTAGE=12.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	32
	1772_LDO	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_DLOV	VOLTAGE=5.4V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
	1772_GND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	32
PMU	+ADAPTER_ILIM	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+ADAPTER_OR_BATT	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+4_85V_RAW	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	31 33
	+4_6V_BU	VOLTAGE=4.6V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33 34
	+4_85V_ESR	VOLTAGE=4.85V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_ESR	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	+3V_PMU_AVCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	26 31
MISC HD	+5V_HD_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25 34
	+HD_LOGIC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	25
TRACKPAD	+5V_MAIN_CONN	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	
HALL EFFECT	+3V_HALL_EFFECT	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23 40
VIDEO	+12_8V_INV	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_INV_UF_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	+5V_INV_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22 40
	+5V_DDC_SLEEP_UF	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	22
	+3V_LCD	VOLTAGE=3.3V	MIN_LINE_WIDTH=12	MIN_NECK_WIDTH=10	22
	+3V_LCD_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	GPU_TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22
	TV_GND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
	TV_GND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	22 40
KB LED	KBDLED_ANODE	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
	KBDLED_RETURN	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	23
FAN GND	FANL_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
	FANR_GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	40
SOUND	+5V_SOUND_SLEEP	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	SND_AGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=15	26

	GND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	
I/O AREA	CHGND1	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND1
INVERTER	CHGND2	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND2
TRACKPAD	CHGND3	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND3
LVDS	CHGND4	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND4 40
I/O AREA	CHGND5	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND5
I/O AREA	CHGND6	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	CHGND6
	ENET_CTAP_CHGND	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=12	28

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
CPU	CPU_VCORE_SLEEP	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 35 40
	CPU_AVDD	VOLTAGE=1.4V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5
	MAXBUS_SLEEP	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	5 6 7 8 15 16 35
DDR RAM	DDR_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	11
INTREPID	+2_5V_INTREPID	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	9 10 15 16
	+3V_INTREPID_USB	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	14
PLLS	+1_5V_INTREPID_PLL	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	8 12 14
	+1_5V_INTREPID_PLL1	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL2	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL3	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
	+1_5V_INTREPID_PLL4	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	14
	+1_5V_INTREPID_PLL5	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=5	12
	+1_5V_INTREPID_PLL6	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	12
	+1_5V_INTREPID_PLL7	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	8
	+1_5V_INTREPID_PLL8	VOLTAGE=1.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=6	14
REFERENCE	INT_MEM_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	INT_AGP_VREF	VOLTAGE=1.25V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	12 18
	INT_MEM_REF_H	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	9
	UIDE_REF	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	13
CARDBUS	+VCC_CBUS_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
	+VPP_CBUS_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	17
ATI M11	GPU_VCORE	VOLTAGE=1.2V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 19 40
	+GPU_MEM	VOLTAGE=2.5V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	18 21
	+3V_GPU	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 18 19 21
	+3V_GPU_FLT	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	21
	+1_5V_AGP	VOLTAGE=1.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	12 15 16 18 19 21
	GPU_MEM_IO	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	
	GPU_MEM_IO_FLT	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+GPU_MEMCORE	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	21
	+1_8V_GPU	VOLTAGE=1.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	18 19 20 21
	+2_5V_GPU_PNLIO	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_8V_ATI_PVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19 21
	+1_5V_AGP_GPU	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	21
	+1_5V_GPU_VDD15	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+1_8V_GPU_PLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_VDDDI	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	GPU_VCORE_VDDCI	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	18
	+2_5V_GPU_A2VDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDD	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_PNLIO	VOLTAGE=1.8V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	21
	+GPU_MCLK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_AVDDQ	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_GPU_MEMPLL	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+3V_ATI_OSC_SLEEP	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+3V_ATI_SS	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	18
	+GPU_VDD15_UF	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK2	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+3V_SLEEP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_AGP_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+1_8V_PVDD_NECK	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	GPU_VCORE_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+GPU_VDD15_NECK	VOLTAGE=1.8V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	19
	+2_5V_SLEEP_NECK2	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_8V_SLEEP_NECK	VOLTAGE=3.3V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+1_5V_SLEEP_NECK	VOLTAGE=1.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
	+2_5V_GPU	VOLTAGE=2.5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	21
SILICON IMIAGE	PP3V3_SI_PVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_PVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_AVCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
	PP3V3_SI_VCC2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=0	20
88E1111	+2_5V_MARVELL	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	28
	+2_5V_MARVELL_AVDD	VOLTAGE=2.5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	+1_0V_MARVELL	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	LTC3405_SW	VOLTAGE=1.0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=8	28
	LM2594_IN	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
FW	+3V_FW_ESD_ILIM	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+3V_FW_ESD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30
	+FW_FUSE	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_SW	VOLTAGE=12.8V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_OR	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	29 30
	+FW_VP0	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_PWR_PORTA	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+FW_VP1	VOLTAGE=33V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	+3V_FW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29 30
	+3V_FW_UF	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT2	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD_PORT1	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	29
	+3V_FW_AVDD_PORT0	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+3V_FW_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_RX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_TX0	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_DVDD_PORT1	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLLVDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL400VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	+1_95V_FW_PLL500VDD	VOLTAGE=1.95V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	29
	FW_VGND0	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	FW_VGND1	VOLTAGE=0V	MIN_LINE_WIDTH=100	MIN_NECK_WIDTH=12	30
	FW_TPO0R	VOLTAGE=0V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	30 40
USB 2.0	NEC_AVDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
	+3V_NEC_VDD	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	27
INTREPID SSCG	+3V_CG_PLL_MAIN	VOLTAGE=3.3V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14
	+2_5V_CG_MAIN	VOLTAGE=2.5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=8	14

MIN_NECK_WIDTH REDUCED FOR TESTPOINTS

GROUP	SIG_NAME	VOLTAGE	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
LTC1625 14V SWITCHER	1625_VIN	VOLTAGE=24V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_VSW	VOLTAGE=12.8V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=6	33
	1625_EXTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1625_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	33
	1V20_REF	VOLTAGE=1.2V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	2 33
LTC3707 5V SWITCHER	3707_INTVCC	VOLTAGE=5V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=10	4
	5V_SW	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	4
	5V_RSNS	VOLTAGE=5V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	4
3V SWITCHER	3V_SW	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	4
	3V_RSNS	VOLTAGE=3.3V	MIN_LINE_WIDTH=25	MIN_NECK_WIDTH=10	4
	3707_SGND	VOLTAGE=0V	MIN_LINE_WIDTH=10	MIN_NECK_WIDTH=6	34
MAX1715 2.5V SWITCHER	2_5V_LX	VOLTAGE=2.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	6
	2_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	6
	2_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	6
	2_5V_DH	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	2_5V_DL	VOLTAGE=2.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
1.5V SWITCHER	1_5V_FB	VOLTAGE=1.5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1_5V_LX	VOLTAGE=1.5V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	6
	1_5V_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	6
	1_5V_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	6
	1_5V_DH	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	1_5V_DL	VOLTAGE=1.5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
CONTROL	1_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	2_5V_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_TON		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_SKIP		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_REF	VOLTAGE=2.0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	MAX1715_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	6
	MAX1715_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	6
MAX1717	VCORE_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	5
	VCORE_LX	VOLTAGE=1.4V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	5
	VCORE_DH		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	5
	VCORE_DL		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	5
	VCORE_BOOST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	5
	VCORE_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	5
	VCORE_ILIM		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_REF		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_TON	VOLTAGE=5V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_CC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_FB	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35 40
	VCORE_TIME		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_VGATE		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	14 35
	VCORE_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=15	5
	VCORE_GNDSNS	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_SNS	VOLTAGE=1.4V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
	VCORE_GNDDIV	VOLTAGE=0V	MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	35
LTC1778	1778_VIN	VOLTAGE=14V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	9
	1778_VCC	VOLTAGE=5V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	9
	1778_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	9
	1778_BST	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	9
	1778_BST_RC	VOLTAGE=5V	MIN_LINE_WIDTH=15	MIN_NECK_WIDTH=10	9
	1778_TG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	9
	1778_BG		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	9
	GPU_VCORE_SW	VOLTAGE=1.2V	MIN_LINE_WIDTH=50	MIN_NECK_WIDTH=10	9
	1778_ION		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1_5V_2_5V_OK		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	36
	1778_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19 40
	1778_FCB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
	1778_VRNG		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	19
LTC3411	LTC3411_VCC	VOLTAGE=3.3V	MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC3411_GND	VOLTAGE=0V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	
	1_8V_SW	VOLTAGE=1.8V	MIN_LINE_WIDTH=30	MIN_NECK_WIDTH=10	6
	1_8V_VFB		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH_RC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_ITH		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SYNC		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
	LTC3411_SHDN		MIN_LINE_WIDTH=8	MIN_NECK_WIDTH=6	
LTC1962 INT PLLS	LTC1962_INT_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	4
	LTC1962_L3_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_L3_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VIN		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	
	LTC1962_1V5_VOUT		MIN_LINE_WIDTH=20	MIN_NECK_WIDTH=10	

SIGNAL CONSTRAINTS - PAGE 3

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SIZE	DRAWING NUMBER	REV.
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SCALE NONE	SHT 39 OF 45	

FUNCTIONAL TEST POINTS

FUNC_TEST=YES JTAG_ASIC_TMS 13 28
FUNC_TEST=YES JTAG_ASIC_TDI 28
FUNC_TEST=YES JTAG_ASIC_TDO 13 14
FUNC_TEST=YES JTAG_ASIC_TCK 13 28
FUNC_TEST=YES JTAG_ASIC_TRST_L 13 28
FUNC_TEST=YES CPU_CHKSTP_OUT_L 5
FUNC_TEST=YES CPU_SRESET_L 5
FUNC_TEST=YES CPU_HRESET_L 5 6 7
FUNC_TEST=YES JTAG_CPU_TMS 5 6
FUNC_TEST=YES JTAG_CPU_TDI 5 6
FUNC_TEST=YES JTAG_CPU_TDO_TP 5
FUNC_TEST=YES JTAG_CPU_TCK 5 6
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40

FUNC_TEST=YES INT_I2C_CLK0 6 11 13 23
FUNC_TEST=YES INT_I2C_DATA0 6 11 13 23
FUNC_TEST=YES INT_I2C_CLK1 13 14 23 24 26
FUNC_TEST=YES INT_I2C_DATA1 13 14 23 24 26
FUNC_TEST=YES CBUS_DET_1_L 17
FUNC_TEST=YES CBUS_DET_2_L 17
FUNC_TEST=YES TMDS_DN<0> 20 22 38
FUNC_TEST=YES TMDS_DP<0> 20 22 38
FUNC_TEST=YES TMDS_DN<1> 20 22 38
FUNC_TEST=YES TMDS_DP<1> 20 22 38
FUNC_TEST=YES TMDS_DN<2> 20 22 38
FUNC_TEST=YES TMDS_DP<2> 20 22 38
FUNC_TEST=YES TMDS_CONN_CLKN 22 38

FUNC_TEST=YES TMDS_CONN_CLKP 22 38
FUNC_TEST=YES VGA_R 22
FUNC_TEST=YES VGA_G 22
FUNC_TEST=YES VGA_B 22
FUNC_TEST=YES VGA_VSYNC 22
FUNC_TEST=YES VGA_HSYNC 22
FUNC_TEST=YES DVI_DDC_CLK_UF 22
FUNC_TEST=YES DVI_DDC_DATA_UF 22
FUNC_TEST=YES DVI_HPD_UF 22
FUNC_TEST=YES LVDS_L0N 19 22 38
FUNC_TEST=YES LVDS_L0P 19 22 38
FUNC_TEST=YES LVDS_L1N 19 22 38
FUNC_TEST=YES LVDS_L1P 19 22 38
FUNC_TEST=YES LVDS_L2N 19 22 38
FUNC_TEST=YES LVDS_L2P 19 22 38
FUNC_TEST=YES CLKLVDS_LN 19 22 38
FUNC_TEST=YES CLKLVDS_LP 19 22 38
FUNC_TEST=YES LVDS_U0N 19 22 38
FUNC_TEST=YES LVDS_U0P 19 22 38
FUNC_TEST=YES LVDS_U1N 19 22 38
FUNC_TEST=YES LVDS_U1P 19 22 38
FUNC_TEST=YES LVDS_U2N 19 22 38
FUNC_TEST=YES LVDS_U2P 19 22 38
FUNC_TEST=YES CLKLVDS_UN 19 22 38
FUNC_TEST=YES CLKLVDS_UP 19 22 38
FUNC_TEST=YES LVDS_DDC_CLK 19 22
FUNC_TEST=YES LVDS_DDC_DATA 19 22
FUNC_TEST=YES BRIGHT_PWM 22
FUNC_TEST=YES TV_GND1 22 39
FUNC_TEST=YES TV_GND2 22 39

FUNC_TEST=YES TV_C 22
FUNC_TEST=YES TV_Y 22
FUNC_TEST=YES TV_COMP 22
FUNC_TEST=YES SND_TO_AUDIO 14 26
FUNC_TEST=YES SND_SYNC 14 26
FUNC_TEST=YES SND_CLKOUT 14 26 37
FUNC_TEST=YES INT_AUDIO_TO_SND 14 26
FUNC_TEST=YES SND_SCLK 14 26 37
FUNC_TEST=YES SND_HW_RESET_L 14 26
FUNC_TEST=YES SND_HP_SENSE_L
FUNC_TEST=YES SND_LIN_SENSE_L
FUNC_TEST=YES INT_I2C_DATA2 14 26
FUNC_TEST=YES INT_I2C_CLK2 14 26
FUNC_TEST=YES ~~I393~~ CHGND4 39
FUNC_TEST=YES ~~I394~~ SLEEP_LED

FUNC_TEST=YES BT_USB_DM 14 25 38
FUNC_TEST=YES BT_USB_DP 14 25 38
FUNC_TEST=YES MODEM_USB_DM 14 26 38
FUNC_TEST=YES MODEM_USB_DP 14 26 38
FUNC_TEST=YES PCI_AD<0> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<1> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<2> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<3> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<4> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<5> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<6> 9 12 17 25 27 38

FUNC_TEST=YES PCI_AD<7> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<8> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<9> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<10> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<11> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<12> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<13> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<14> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<15> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<16> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<17> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<18> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<19> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<20> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<21> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<22> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<23> 12 17 25 27 38
FUNC_TEST=YES PCI_AD<24> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<25> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<26> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<27> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<28> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<29> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<30> 9 12 17 25 27 38
FUNC_TEST=YES PCI_AD<31> 9 12 17 25 27 38
FUNC_TEST=YES PCI_FRAME_L 12 17 25 27 38
FUNC_TEST=YES PCI_TRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_IRDY_L 12 17 25 27 38
FUNC_TEST=YES PCI_DEVSEL_L 12 17 25 27 38
FUNC_TEST=YES PCI_STOP_L 12 17 25 27 38

FUNC_TEST=YES PCI_PAR 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<0> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<1> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<2> 12 17 25 27 38
FUNC_TEST=YES PCI_CBE<3> 12 17 25 27 38
FUNC_TEST=YES AIRPORT_PCI_REQ_L 12 25
FUNC_TEST=YES AIRPORT_PCI_GNT_L 12 25
FUNC_TEST=YES AIRPORT_PCI_INT_L 14 25
FUNC_TEST=YES EIDE_OPTICAL_DATA<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<2> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<3> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<4> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<5> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<6> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<7> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<8> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<9> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<10> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<11> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<12> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<13> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<14> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DATA<15> 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMA_RQ 25 38
FUNC_TEST=YES EIDE_OPTICAL_RD_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_DMAACK_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<0> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<1> 25 38
FUNC_TEST=YES EIDE_OPTICAL_ADDR<2> 25 38
FUNC_TEST=YES SND_AMP_MUTE 26
FUNC_TEST=YES SND_HP_MUTE_INV

FUNC_TEST=YES EIDE_OPTICAL_CS0_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_CS1_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_RST_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_WR_L 25 38
FUNC_TEST=YES EIDE_OPTICAL_IOCHRDY 25 38
FUNC_TEST=YES EIDE_OPTICAL_INT 25 38
FUNC_TEST=YES TPAD_F_TXD
FUNC_TEST=YES TPAD_F_RXD
FUNC_TEST=YES LID_CLOSED_L 23
FUNC_TEST=YES COMM_RESET_L 14 26
FUNC_TEST=YES COMM_SHUTDOWN 14 26
FUNC_TEST=YES COMM_RING_DET_L 14 26 31
FUNC_TEST=YES +5V_TPAD_SLEEP
FUNC_TEST=YES +3V_HALL_EFFECT 23 39
FUNC_TEST=YES KBD_CAPSLOCK_LED
FUNC_TEST=YES KBD_FUNCTION_L 23 31
FUNC_TEST=YES KBD_CONTROL_L 23 31
FUNC_TEST=YES +PPBATT_ISNS_N 24
FUNC_TEST=YES KBD_OPTION_L 23 31
FUNC_TEST=YES KBD_SHIFT_L 23 31
FUNC_TEST=YES KBD_X<0> 23 31
FUNC_TEST=YES KBD_X<1> 23 31
FUNC_TEST=YES KBD_X<3> 23 31
FUNC_TEST=YES MMM_ACC_SELFTEST 24
FUNC_TEST=YES MMM_ACC_X_AXIS 24
FUNC_TEST=YES MMM_ACC_Y_AXIS 24
FUNC_TEST=YES MMM_ACC_Z_AXIS 24
FUNC_TEST=YES SRCLK_TP 27
FUNC_TEST=YES SRMOD_TP 27
FUNC_TEST=YES TEB_TP 27
FUNC_TEST=YES TEST_TP 27

FUNC_TEST=YES KBD_Y<0> 31
FUNC_TEST=YES KBD_Y<1> 31
FUNC_TEST=YES KBD_Y<3> 31
FUNC_TEST=YES KBD_Y<4> 31
FUNC_TEST=YES KBD_Y<6> 31
FUNC_TEST=YES KBD_Y<7> 31
FUNC_TEST=YES KBD_NUMLOCK_LED
FUNC_TEST=YES +BATT_POS 32 39
FUNC_TEST=YES BATT_CLK 32
FUNC_TEST=YES BATT_DATA 32
FUNC_TEST=YES BATT_NEG 32 39
FUNC_TEST=YES PMU_BATT_DET_L 31 32
FUNC_TEST=YES FANR_GND 39
FUNC_TEST=YES FANL_GND 39
FUNC_TEST=YES FANL_TACH
FUNC_TEST=YES FANR_PWM
FUNC_TEST=YES FANL_PWM
FUNC_TEST=YES RJ45_DP<0> 28 38
FUNC_TEST=YES RJ45_DN<0> 28 38
FUNC_TEST=YES RJ45_DP<1> 28 38
FUNC_TEST=YES RJ45_DN<1> 28 38
FUNC_TEST=YES RJ45_DP<2> 28 38
FUNC_TEST=YES RJ45_DN<2> 28 38
FUNC_TEST=YES RJ45_DP<3> 28 38
FUNC_TEST=YES RJ45_DN<3> 28 38
FUNC_TEST=YES FW_TPO0R 30 39
FUNC_TEST=YES VCORE_VID0
FUNC_TEST=YES VCORE_VID1
FUNC_TEST=YES VCORE_VID2
FUNC_TEST=YES VCORE_VID3
FUNC_TEST=YES VCORE_VID4

FUNC_TEST=YES FW_TPO1P 30 38
FUNC_TEST=YES FW_TPO1N 30 38
FUNC_TEST=YES FW_TPI1P 30 38
FUNC_TEST=YES FW_TPI1N 30 38
FUNC_TEST=YES CHARGE_LED_L 31 32
FUNC_TEST=YES ADAPTER_DET 31 32
FUNC_TEST=YES SUTRO_ALS_GAIN_SW 23 25
FUNC_TEST=YES SUTRO_ALS_OUT 23 25
FUNC_TEST=YES KBD_LED1_OUT
FUNC_TEST=YES KBD_LED2_OUT
FUNC_TEST=YES COMM_TXD_L 14 26
FUNC_TEST=YES COMM_TRXC 14 26
FUNC_TEST=YES COMM_GPIO_L 14 26
FUNC_TEST=YES COMM_DTR_L 14 26
FUNC_TEST=YES COMM_RTS_L 14 26
FUNC_TEST=YES COMM_RXD 14 26
FUNC_TEST=YES PMU_KB_RESET_L
FUNC_TEST=YES PWR_BUTTON_L 23 26
FUNC_TEST=YES +PBUS 39
FUNC_TEST=YES +24V_PBUS 39
FUNC_TEST=YES GPU_VCORE 18 19 39
FUNC_TEST=YES CPU_VCORE_SLEEP 5 6 35 39
FUNC_TEST=YES VCORE_FB 35 39
FUNC_TEST=YES +1_8V_MAIN 39
FUNC_TEST=YES +3V_PMU 39
FUNC_TEST=YES +5V_DDC_SLEEP 22 39
FUNC_TEST=YES +12_8V_INV 22 39
FUNC_TEST=YES VCORE_MUX_EN 35

FUNC_TEST=YES +5V_INV_SW 22 39
FUNC_TEST=YES LEFT_USB_DM 25 27 38
FUNC_TEST=YES LEFT_USB_DP 25 27 38
FUNC_TEST=YES RIGHT_USB_DM 27 33 38
FUNC_TEST=YES RIGHT_USB_DP 27 33 38
FUNC_TEST=YES NEC_LEFT_USB_PWREN 25 27
FUNC_TEST=YES NEC_LEFT_USB_OVERCURRENT 25 27
FUNC_TEST=YES NEC_RIGHT_USB_PWREN 27 33
FUNC_TEST=YES NEC_RIGHT_USB_OVERCURRENT 27 33
FUNC_TEST=YES DCDC_EN 19 30 34 35
FUNC_TEST=YES BBANG_HRESET_L 6
FUNC_TEST=YES MAIN_RESET_L 14 17 18 20 25 27 31
FUNC_TEST=YES RF_DISABLE_L_SPN 25
FUNC_TEST=YES AIRPORT_CLKRUN_L 25
FUNC_TEST=YES ROM_RW_L 9 12 25
FUNC_TEST=YES ROM_ONBOARD_CS_L 9 25
FUNC_TEST=YES ROM_CS_L 9 12 25
FUNC_TEST=YES CLK33M_AIRPORT 12 25 37
FUNC_TEST=YES AIRPORT_IDSEL 25
FUNC_TEST=YES ROM_OE_L 9 12 25
FUNC_TEST=YES INT_MOD_DTI 14 26
FUNC_TEST=YES JTAG_CPU_TRST_L 5 6 40
FUNC_TEST=YES MOD_BITCLK 14 26
FUNC_TEST=YES MOD_CLKOUT 14 26
FUNC_TEST=YES MOD_DTO 14 26
FUNC_TEST=YES MOD_SYNC 14 26
FUNC_TEST=YES SLEEP 23 31 34 36
FUNC_TEST=YES 1778_VFB 19 39

FUNCTIONAL TEST POINTS

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SIZE	DRAWING NUMBER	REV.
D	051-6694	G
SCALE NONE	SHT 40 OF 45	

REVISION HISTORY

12/11/03

1) IMPORTED Q41 PRODUCTION RELEASE SCHEMATIC
2) CHANGED CPU (U43) TO A7PM
3) CHANGED PLL CONFIG STUFFING FOR NEW CPU
4) CHANGED U41 TO M1X-PSOP4 SYMBOL
5) ADDED CPU AVDD LDO (U6)
6) ADDED R284 AND R604 TO ADD OPTION FOR PD_L OF U42 (CLOCK CHIP) TO BE DRIVEN BY JTAG_ASIC_TDO FROM INTREPID
7) ADDED R698 TO DISCONNECT INT_GPIO0 FROM CC FSEL
8) CHANGED JTAG_ASIC_TDO TP TO JTAG_ASIC_TDO AND MOVED IT TO INTREPID'S TDO
9) CHANGED JTAG_ASIC_TDI TO CONNECT TO ETHERNET PHY'S TDI

12/15/03

10) CHANGED PIN 4 (DCDC_EN) ON J11 TO NEC_RIGHT_USBOVERCURRENT
11) CHANGED PIN 11 OF J11 TO NC

12/16/03

12) ADDED R633 AS PULLUP ON JTAG_ASIC_TDI
13) CHANGED CPU_TEMP_DM TO CPU_THERM_DM
14) CHANGED CPU_TEMP_DP TO CPU_THERM_DP
15) CHANGED GPU_THERM_DP TO GPU_THERM_DP_TP
16) CHANGED GPU_THERM_DM TO GPU_THERM_DM_TP
17) FIXED MISSED CONNECTION WITH MAXBUS_SLEEP TO CPU

12/17/03

18) CHANGED R657 (EXTPLL_SDWN_POL_BOOT_STRAP) TO NO_STUFF AND REMOVED NO_STUFF FROM R153
19) UPDATE DIFF_NE_SPACING_TYPE PROPERTY ON POWER_SUPPLY_SENSE AND THERMAL DIODE DIFF PAIRS
20) CHANGED FIREWIRE OSCILLATOR (G1) TO NEW PREFERRED SUNNY PART

12/18/03

21) CHANGED MAX VIA COUNT ON ALL AGP STB NETS TO 5 TO CLEAR DRCS

** RELEASED FOR EVT **

2/10/04

22) REMOVED XW11 - JUMPER ON 1.8V SWITCHER OUTPUT
23) CHANGED R657 TO STUFFED AND R153 TO NO STUFF
24) CHANGED CPU PLL CONFIG TO 9X HIGH AND 5X LOW

** RELEASED FOR DVT **

3/24/04

25) REMOVED ALTERNATE BOM OPTION FROM ALTERNATE ETHERNET CRYSTALS

3/29/04

26) ADDED ALTERNATE FOR Q41A REV 1.1.1 CPU (U43)
27) ADDED ALTERNATES FOR 128MB AND 64MB A16 MITS
28) CHANGED TMDS SERIES RPARS TO 0 OHMS (RP57,RP27,RP32,RP28)
29) ADDED ALTERNATE FOR ALS OP-AMP (U40)

** RELEASED TO REV A **

30) CHANGED TMDS TERMINATION R,C AND LS TO PRODUCTION VALUES

** RELEASED TO REV A UNDER NEW PART NUMBER **

09/17/2004

1) GPU_DVOD<0..12> NETNAME CHANGE TO GPU_DVOD<0..23>
2) D8 FROM 1N5227B CHANGE TO BZX84C2V7LT1
3) R751 VALUE FROM 10K OHM CHANGE TO 604 OHM
4) ADD C935 (0.1UF)
5) ADD R867 (0 OHM) FOR IPOD ACTION
6) PMU PIN74 NETNAME FROM NC TO PMU_SELECT
7) ADD R868 (10K OHM; NO_STUFF) PULL UP TO +3V_PMU
8) ADD R869 (10K OHM) PULL DOWN TO GND
9) PMU PIN 91 NETNAME FROM NC TO SYS_BATT_ISNS2
10)ADD R870 (0 OHM) SYS_BATT_ISNS2 LINK TO SYS_BATT_ISNS
11)ADD U51 (INA138)
12)ADD R852 (0.010 OHM),R853 (150K OHM) AND R857(49.9 OHM)
13)ADD C917 (0.1UF) AND C925 (10UF)
14)ADD DESCRIPTION FOR MMM I2C BUS
15)MMM I2C BUS LINK TO INTREPID :INT_I2C_CLK1 AND INT_I2C_DATA1
16)CHANGE NETNAME FROM INT_EXTINT11_PU TO MMM_FFIRQ_L
17)CHANGE NETNAME FROM INT_EXTINT12_PU TO MMM_SIRQ_L
18)ADD R863 (10K OHM) AND R864 (10K OHM) FOR MMM_FFIRQ_L&MMM_SIRQ_L PULL UP TO +3V_MAIN
19)ADD U53 (16F818) AND U5 (KXM52)
20)ADD R845 (0 OHM),R846 (0 OHM;NO_STUFF),R847 (10K OHM;NO_STUFF),R848 (10K OHM;NO_STUFF)
21)ADD R849 (10K OHM),R850 (10K OHM;NO_STUFF),R851(0 OHM),R854 (10K OHM),R856 (10K OHM),
22)ADD R860 (0 OHM),R858 (0 OHM),R859 (0 OHM),R855 (10K OHM),R861 (10K OHM),R862(10K OHM;NO_STUFF)
23)ADD C936(0.1UF),C918(0.1UF),C919(0.1UF),C921(0.0047UF),C923(0.0047UF),C926(0.0047UF),C927(0.1UF)
24)DEL RP44 (100K OHM) AND ADD R874 (100K OHM), R875 (100K OHM) AND R873 (100K OHM)
25)ADD R872 (10K OHM) FOR AUDIO_LO_MUTE_L
26)ADD R871 (100 OHM) AND SUPERCAP C937 (N20P80;5.5V;ELEC;0.33F)
27)J21 PIN12 NETNAME FROM NC CHANGE TO THERM_L_OC
28)J21 PIN10 NETNAME FROM NC CHANGE TO INT_I2C_DATA1
29)J21 PIN11 NETNAME FROM NC CHANGE TO INT_I2C_CLK1
30)C592 VALUE FROM 0.001UF CHANGE TO 0.01UF (20%,50V,0603)
31)U59 FROM MP1518DJ CHANGE TO MM3120
32)L11 CHANGE TO 152S0235 (22UH;3.8*3.8*1.5MM)
33)DEL D31
34)R202 VALUE FROM 5.23 OHM CHANGE TO 25.5 OHM
35)C79 VALUE FROM 2.2UF CHANGE TO 1UF
36)ADD Q70 (SI3443), Q34 (2N7002)
37)ADD R866 (100K OHM),R865 (4.7 OHM),C929 (0.022UF)

09/20/2004

1) ADD R877 (10K OHM)
2) ADD R876 (470K OHM;NO_STUFF)

09/21/2004

1) ADD R878 AND R879 (0 OHM;NO_STUFF)[ADD A 0-OHM RESISTOR TO BY-PASS THE N-FET ON EACH FAN]

09/22/2004

1) R822 (680 OHM CHANGE TO 510 OHM) AND R826 (680 OHM CHANGE TO 510 OHM)

09/23/2004

1) ADD NC NETNAME AT U59 PIN6 AND PIN9
2) CHANGE R465 CAP SIZE FROM 0603 TO 0805
3) BOM OPTION FROM NO STUFF CHANGE TO SUPERCAP

09/24/2004

1) CHANGE R465 FROM MF 1/16W TO FF 1/10W
2) ADD R880 AND R871 (0 OHM;BOM_OPTIOM;FOR SUPERCAP AND BACKUP BATTERY SWITCH)
3) ADD U60 (LIS3L02AQ;ST SENSOR)
4) ADD R881 (10K OHM) ,R882 (10K OHM), R883 (10K OHM)
5) ADD C937 (0.1UF,10V,20%,0402)
6) ADD BOM_OPTION (KIONIX_ACCEL AND ST_ACCEL)

10/04/2004

1) CHANGE TEST POINT FUNC_TEST=NO FOR FUNC_TP_WRONG_SIDE.LOG
2) ADD NO_TEST=YES FOR NOTP.LOG(MMM_PIC_AN2_PD,MMM_PIC_AN3_PU)

10/05/2004

1) ADD R850 (0 OHM)

10/15/2004

1) REPLACE BOOT BANGER EEPROM U32 WITH 32KX M24256B FUNC_TP_WRONG_SIDE.LOG

12/16/2004

1) SCHEMATIC RELEASE FOR PRODUCTION

04/27/2005 REV.E

1) ADD LEAD FREE PHOTO SENSOR (385-0053)
2) ADD 337S3094 AND 337S3131

06/20/2005 REV.F

1) ADD LEAD FREE PHOTO SENSOR (385-0053)

08/25/2005 REV.G

1) ADDED 337S3216 (IC,A7PM,R1.5,1.67GHZ,1.3V,25W) AS OPTION
2) REPLACED 341S1561 (BOOTROM 4.91.F1) WITH 341S1793 (BOOTROM 4.9.1.F3)
3) ADDED LABEL WITH EEE:U3Y

REVISION HISTORY(1 OF 1)

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SIZE	DRAWING NUMBER	REV.
D	051-6694	G
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*** Signal Cross-Reference for the entire design ***

+1.8V_MARVELL     28D2< 39D3>
+1.5V_AGP         12C5< 12D1< 12D4< 15D6< 16C8<
                  18C6< 18D6< 19A8< 19B4<> 19D5<>
                  21B8< 21D6< 39C3>
+1.5V_AGP_GPU     21C5< 39C3>
+1.5V_AGP_NECK    19B4<> 39B3>
+1.5V_GPU_VDD15   19D3> 39C3>
+1.5V_INTREPID_PLL  8D6< 12D4< 12D8< 14D6<> 39D3>
+1.5V_INTREPID_PLL1  14C3< 39D3>
+1.5V_INTREPID_PLL2  14D3< 39D3>
+1.5V_INTREPID_PLL3  14D3< 39D3>
+1.5V_INTREPID_PLL4  14D3< 39D3>
+1.5V_INTREPID_PLL5  12D3< 39D3>
+1.5V_INTREPID_PLL6  12D6< 39D3>
+1.5V_INTREPID_PLL7  8D5< 39D3>
+1.5V_INTREPID_PLL8  14D3< 39D3>
+1.5V_LDO         36D8< 39D6>
+1.5V_MAIN        39D6>
+1.5V_SLEEP       39D6>
+1.5V_SLEEP_NECK  21A3< 39B3
+1.5V_SLEEP_VIN   36D8< 39D6>
+1.8V_ATI_PVDD    19C5<> 21B6< 21B6< 21D6<> 39C3>
+1.8V_ATI_TPVDD   21D2<>
+1.8V_DVO_P       21B2<
+1.8V_GPU         18A7< 19C8< 20A8< 21A2< 21A6<
                  21B1< 21B6< 21C8< 21D6< 21D8< 39C3>
+1.8V_GPU_AVDD    21D5< 39C3>
+1.8V_GPU_AVDDQ   21A2< 21D7< 39C3>
+1.8V_GPU_MEMPLL  21B5< 39C3>
+1.8V_GPU_PLL     21D4< 39C3>
+1.8V_GPU_PNLI0   21A5< 39C3>
+1.8V_GPU_PNLPLL  21B5< 39C3>
+1.8V_GPU_TH_PLL  21B4< 21D1<
+1.8V_GPU_VDDDI   21C7< 21D4< 39C3>
+1.8V_MAIN        39D6< 40A2>
+1.8V_PVDD_NECK   19B5<> 39B3>
+1.8V_SLEEP       39D6>
+1.8V_SLEEP_NECK  21A3<> 39B3>
+1.95V_FW_DVDD    29C4< 29C7<> 29D5< 39A3>
+1.95V_FW_DVDD_PORT1  29D6< 39A3>
+1.95V_FW_DVDD_RX1  29C5< 39A3>
+1.95V_FW_DVDD_TX0  29C5< 39A3>
+1.95V_FW_PLL400VDD  29D6< 39A3>
+1.95V_FW_PLL500VDD  29D5< 39A3>
+1.95V_FW_PLLVDD  29D5< 29D7<> 39A3>
+2.5V_CG_MAIN     14C4< 39A3>
+2.5V_GPU         21A8< 21B6< 21D3< 21D7< 21D8<
                  39B3>
+2.5V_GPU_AZVDD   21D4< 21D7< 39C3>
+2.5V_GPU_PNLI0   21A5< 39C3>
+2.5V_INTREPID    9A8< 10D3< 10D5< 10D7< 10D8< 15D7<
                  16B8< 39D3>
+2.5V_MAIN        39D6>
+2.5V_MARVELL     28B8< 28C4<> 39B3>
+2.5V_MARVELL_AVDD  28C4< 39B3>
+2.5V_REG         30B6<
+2.5V_REG_F       30A2<>
+2.5V_SLEEP       39D6>
+2.5V_SLEEP_NECK  19C4<> 39B3>
+2.5V_SLEEP_NECK2  21A3<> 39B3>
+2.8V_GPU_LVDS_LDO  21A6<>
+3V_ATI_OSC_SLEEP  39C3>
+3V_ATI_SS        18B2< 39C3>
+3V_CG_PLL_MAIN   40C6< 39A3>
+3V_FW            29A3> 29D7<> 30B7<> 30D5< 39A3>
+3V_FW_AVDD       29C6< 39A3>
+3V_FW_AVDD_PORT0  29C6< 39A3>
+3V_FW_AVDD_PORT1  29C6< 39A3>
+3V_FW_AVDD_PORT2  29D6< 39A3>
+3V_FW_ESD        30B3<> 30B5< 30D2<> 39B3>
+3V_FW_ESD_ILIM   30D4< 39B3>
+3V_FW_ESD_R      30B6<
+3V_FW_LF         29D7<> 39A3>
+3V_GPU           12D1< 18B8< 18C5< 18C7< 18D6<
                  19C4< 19C5< 19C7< 19D8< 21A7< 21B1<
                  21B8< 39C3>
+3V_GPU_FLT       21B2< 39C3>
+3V_HALL_EFFECT   23B6<> 39B6> 40C4>
+3V_INTREPID_USB  14C3< 39D3>
+3V_LCD           22B4<> 39B6>
+3V_LCD_SW        22A4<> 39B6>
+3V_MAIN          23A7< 39D6>
+3V_MAIN_CONN     23A6<>
+3V_NEC_VDD       27D7< 27D7> 39A3>
+3V_PMU           39D6> 40A2>
+3V_PMU_AVCC      26B1< 31B6< 31D5<> 39C6>
+3V_PMU_ESR       31B4< 39C6>
+3V_PMU_RESET     31C7< 35A3<>
+3V_SLEEP         20D5< 20D8< 23A5< 39D6>
+3V_SLEEP_AUDIO   20D6<> 26D7>
+3V_SLEEP_NECK    21A3<> 39B3>
+3V_SLP_OK_L      34B4<>
+3V_SLP_ON        34A5<>
+4.6V_BU          33A3<> 34B6< 39C6>
+4.85V_ESR        33A4< 39C6>
+4.85V_RAW        31B4< 33A4<> 39C6>
+5V_DDC_SLEEP     22D3<> 22D5<> 39B6> 40A2>
+5V_DDC_SLEEP_UF  22D6< 39B6>
+5V_HD_SLEEP      25D1<> 34A7<> 39C6>
+5V_INV_SW        22B2<> 39B6> 40D1>
+5V_INV_UF_SW     22B2<> 39B6>
+5V_MAIN          39D6>
+5V_MAIN_AUDIO    26D7<>
+5V_MAIN_AUDIO_0  26D7<>
+5V_MAIN_CONN     39B6>
+5V_SLEEP         39D6>
+5V_SLEEP_MK3120  23A4<>
+5V_SLEEP_SDDSP   39B6>
+5V_TPAD          23B7<>
+5V_TPAD_FB       23B6<>
+5V_TPAD_SLEEP    40C4>
+12_9V_INV        22B1<> 39B6> 40A2>
+24V_PBUS         39D6> 40B2>
+24V_PBUS_CONN    33A8<>
+ADAPTER          32D8<> 33B7< 39D6>
+ADAPTER_ILIM     33B6< 39C6>
+ADAPTER_OR_BATT  33A5<> 39C6>
+ADAPTER_SENSE    32D5<> 39C6>
+ADAPTER_SW       32D7<> 39C6>
+BATT             39D6>
+BATT_14V_FUSE    32D1<> 39C6>
+BATT_24V_FUSE    32B1< 32D2<> 39C6>
+BATT_ISNS_P      24A5<>
+BATT_POS         32A4<> 39C6> 40C3>
+BATT_RSNS        32B2< 39C6>
+BATT_VSNS        32A4< 39C6>
+FAN1_PWR         26A4<>
+FAN2_PWR         26A3<>
+FW_FUSE          38D7<> 39A3>
+FW_PWR_CTRL      38B6<>
+FW_PWR_OR        29B8< 29D8<> 38D5<> 39A3>
+FW_PWR_OR_F      38B6<>
+FW_PWR_OR_GATE   38B8<>
+FW_PWR_OR_GATE_L  38B8<
+FW_PWR_PORTA     38B6< 39A3>
+FW_SW            38D5<> 39A3>
+FW_VP9           38C2<> 39A3>
+FW_VP1           38A3<> 39A3>
+GPU_MCLK         21C7< 21D4< 39C3>
+GPU_MEM          18A6<> 18B8< 21B4< 21B7< 21C6<
                  21C8< 21D2< 39C3>
+GPU_MEMCORE      21C5< 39C3>
+GPU_VDD15_NECK   19B5<> 39B3>
+GPU_VDD15_UF     19B5<> 19D4<> 39C3>
+HD_LOGIC_SLEEP   25C2<> 39C6>
+PBUS             39D6> 40B2>
+PPBATT_ISNS_N    24A4< 40B4>
+VCC_CBUS_SW      21B1< 17B2< 17D2<> 39D3>
+VPP_CBUS_SW      17B1< 17B2< 17D2<> 39C3>
1V20_REF          32C7< 33C8< 39D1>
1V65_REF          32A5<
1_5V_2_5V_OK      36C5< 39B1>
1_5V_BOOST        36C6<> 39C1>
1_5V_BST          36C5<> 39C1>
1_5V_DH           36C5<> 39C1>
1_5V_DL           36B5<> 39C1>
1_5V_FB           36B5< 36B7< 39C1>
1_5V_ILIM         36C5<> 39C1>
1_5V_LX           36B5< 39C1>
1_5V_SLEEP_EN_L   36C7<> 36D7<>
1_8V_SLEEP_PWREN_L  36C4<>
1_8V_SW           36A5<> 39A1>
1_8V_VFB          39A1>
2_5V_BOOST        36C4<> 39D1>
2_5V_BST          36C4<> 39D1>
2_5V_DH           36C4<> 39D1>
2_5V_DL           36B4<> 39D1>
2_5V_LX           36B4<> 39D1>
2_5V_SLEEP_PWREN_L  36C2<>
2_34V_REF         31A4<
3V_5V_OK          23A7< 34B4<> 36A8<> 36D6<
3V_5V_OK_G        23B8<
3V_5V_OK_INV      36A8<
3V_5V_OK_L        23B8<>
3V_BG             34C4<>
3V_BOOST          34C4<>
3V_BOOST_ESR      34D3<>
3V_ITH            34C4<>
3V_ITH_RC         34C3<
3V_PMU_VTAB       33B3<
3V_RSNS           34D2< 39D1>
3V_RUNSS          34C4<
3V_SLEEP_PWREN_L  34A3<>
3V_SNDM           34C4< 38A2>
3V_SNSP           34C4< 38A2>
3V_SW             34C4<> 39D1>
3V_TG             34D4<>
3V_VOSNS          34C4<>
5V_BG             34C5<>
5V_BOOST          34C5<>
5V_BOOST_ESR      34D6<>
5V_HG_PWREN       34A6<>
5V_ITH            34C5<>
5V_ITH_RC         34C6<
5V_RSNS           34D7< 39D1>
5V_RUNSS          34C5<
5V_SLEEP          34A6< 39D6>
5V_SLEEP_PWREN    34A8<>
5V_SNSM           34C5< 38A2>
5V_SNSP           34C5< 38A2>
5V_SW             34C5<> 39D1>
5V_TG             34C5<>
5V_VOSNS          34C5<>
16B5_BG           33C5<>
16B5_BST          33C5<
16B5_BST_ESR      33C5<>
16B5_COMP         32D2< 33C6<
16B5_DIV          33C8<
16B5_ENABLE       32D7<>
16B5_ENABLE_L     33D7<>
16B5_EXTVCC       33D5<> 39D1>
16B5_FCB          33C6<
16B5_INTVCC       33C5<> 39D1>
16B5_RUNSS        33C6<
16B5_SGND         33B7<> 39D1>
16B5_TG           33C5<>
16B5_VFB          33B5<>
16B5_VIN          33C6< 39D1>
16B5_VSW          33C4< 39D1>
1772_ACIN         32B5<
1772_ACOK_L       32B5<> 32C4<>
1772_BST          32B4<>
1772_BST_ESR      32C3<
1772_CCI          32B5<>
1772_CCS          32B5<>
1772_CCV          32B5<>
1772_CCV_RC       32B6<
1772_CELLS        32B4<
1772_CLS          32A4<
1772_CSIN         32B4<> 38A2>
1772_CSIP         32B4<> 38A2>
1772_CSSN         32C5< 38A2>
1772_CSSP         32C5< 38A2>
1772_DCIN         32B5< 39C6>
1772_DH           32B4<>
1772_DLO          32B4<>
1772_DLOV         32B4<> 39C6>
1772_GND          32A5<> 39C6>
1772_ICHG         32B5<>
1772_ICTL         32B6<>
1772_ITINP        32B5<
1772_LDO          32C4<> 39C6>
1772_LX           32B4<> 39C6>
1772_REF          32B5<>
1772_VCTL         32B5<>
1778_BG           19A5< 39B1>
1778_BST          19A5< 39B1>
1778_BST_RC       19A4<> 39B1>
1778_FCB          19A5< 39B1>
1778_GND          19A5< 19A7> 39B1>
1778_ION          19A5< 39B1>
1778_ITH          19A5<> 39B1>
1778_ITH_RC       19A7< 39B1>
1778_SHDN         19A5< 39B1>
1778_SHDN_L_D3COLD  19A4<>
1778_TG           19A5< 39B1>
1778_VCC          19A5<> 39B1>
1778_VFB          19A2< 19A5< 39B1> 40A1>
1778_VIN          19A5< 39B1>
1778_VRNG         19A5< 39B1>
3405_MODE         26D5<
3405_VFB          28D4<>
3897_FCB          24C5<
3707_FSET         34C5<
3707_INTVCC       34D4<> 39D1>
3707_SGND         34B5< 39D1>
3707_STBY         34C5>
A29_CLS_ADJ       32A5<>
A29_CURRENT_ADJ   32C4<>
A29_DETECT        31A2< 32A5> 32C4<>
A29_DET_L         31A3<
AB_SEL_LOW        35A6<>
AC_DET            31A4<
AC_DIV            32C6<
AC_ENABLE_GATE    32D6<>
AC_ENABLE_L       32C6<>
AC_STR_18V        32C4<>
AC_IN             28B8<> 30C8< 31B3< 32C5<> 32C7<>
AC_IN_FW_CNTL     30C8<>
AC_IN_L           31B6<> 32C6<>
AC_IN_L_RC        32C2<>
ADAPTER_DET       31A4< 32D8<> 40C2>
ADAPTER_I_REG     32D3<>
ADT7460_TACH3_TP  26B3<>
ADT7467_ADR_EN_L  26B3<>
ADT7467_THERM     23A8< 26B2<> 26B3<
ADT7467_VCC       26B2<>
ADT7467_VCORE_MON  5C8<> 26B4<
AGPBX_DET_PU      18C6<>
AGP_AD<0>         19C7<>
AGP_AD<15..0>     38D5>
AGP_AD<1>         12C2< 18C7<>
AGP_AD<2>         12C2< 18C7<>
AGP_AD<3>         12C2< 18C7<>
AGP_AD<4>         12C2< 18C7<>
AGP_AD<5>         12C2< 18C7<>
AGP_AD<6>         12C2< 18C7<>
AGP_AD<7>         12C2< 18C7<>
AGP_AD<8>         12C2< 18C7<>
AGP_AD<9>         12C2< 18C7<>
AGP_AD<10>        12C2< 18C7<>
AGP_AD<11>        12C2< 18C7<>
AGP_AD<12>        12C2< 18C7<>
AGP_AD<13>        12C2< 18C7<>
AGP_AD<14>        12C2< 18C7<>
AGP_AD<15>        12C2< 18C7<>
AGP_AD<16>        12C2< 18C7<>
AGP_AD<17>        12C2< 18C7<>
AGP_AD<18>        12C2< 18C7<>
AGP_AD<19>        12C2< 18C7<>
AGP_AD<20>        12C2< 18C7<>
AGP_AD<21>        12C2< 18C7<>
AGP_AD<22>        12C2< 18C7<>
AGP_AD<23>        12C2< 18C7<>
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AGP_AD<25>        12C2< 18D7<>
AGP_AD<26>        12C2< 18D7<>
AGP_AD<27>        12C2< 18D7<>
AGP_AD<28>        12B2< 18D7<>
AGP_AD<29>        12B2< 18D7<>
AGP_AD<30>        12B2< 18D7<>
AGP_AD<31>        12B2< 18D7<>
AGP_AD_STB<0>     12A2< 12B2< 18D6<> 38D5>
AGP_AD_STB<1>     12A2< 12B2< 18D6<> 38D5>
AGP_AD_STB_L<0>   12A2< 12B2< 18D6<> 38D5>
AGP_AD_STB_L<1>   12A2< 12A2< 18D6<> 38D5>
AGP_ATI_RESET_L   18B7<
AGP_ATI_VREF      18B7<
AGP_ATI_VREFG     18B7<
AGP_BUSY_L        12C4<> 12D2< 18D6>
AGP_CBE<0>        12B2< 18B7<>
AGP_CBE<1..0>     38D5>
AGP_CBE<1>        12B2< 18B7<>
AGP_CBE<2>        12B2< 18B7<>
AGP_CBE<3..2>     38D5>
AGP_CBE<3>        12B2< 18C7<>
AGP_DEVSEL_L      12B2< 12C2< 18B7< 38D5>
AGP_FRAME_L       12B2< 12C2< 18B7< 38D5>
AGP_GNT_L         12C2< 12D2<> 18B7< 38D5>
AGP_INT_L         14B5< 18B7<>
AGP_IRDY_L        12B2< 12C2< 18B7< 38D5>
AGP_PAR           12B2< 18B7< 38D5>
AGP_PIPE_L        12A2<> 12B2<
AGP_RBF_L         12A2<> 12C2< 18C6> 38D5>
AGP_REQ_L         12C2< 12D2< 18B7< 38D5>
AGP_SBA<0>        12B2< 18C6>
AGP_SBA<7..0>     38D5>
AGP_SBA<1>        12B2< 18C6>
AGP_SBA<2>        12B2< 18C6>
AGP_SBA<3>        12B2< 18C6>
AGP_SBA<4>        12B2< 18C6>
AGP_SBA<5>        12B2< 18C6>
AGP_SBA<6>        12B2< 18C6>
AGP_SBA<7>        12B2< 18C6<>
AGP_SB_STB        12B2< 12B2<> 18C6<> 38D5>
AGP_SB_STB_L      12A2< 12A2<> 18C6<> 38D5>
AGP_ST<0>         12A2<> 18C6<
AGP_ST<1>         12A2<> 18C6<
AGP_ST<2>         12A2<> 18C6<
AGP_STOP_L        12B2< 12C2< 18B7< 38D5>
AGP_STP_L         18C6<
AGP_SUS_STAT_L_PU  18C6<
AGP_TRDY_L        12B2< 12C2< 18B7< 38D5>
AGP_WBF_L         12A4<> 12B2< 18B7>
AIRPORT_CLKRUN_L  25C6< 40C1>
AIRPORT_IDSEL     25C5< 40B1>
AIRPORT_PCI_GNT_L  12C5< 27D5< 40C4>
AIRPORT_PCI_INT_L  14B5< 14D7< 25D5< 40C4>
AIRPORT_PCI_REQ_L  12A7< 12D7<> 25D6<> 40D4>
AIRPORT_PME_L_TP  25D6<>
AMP_CONTROL       26C5<> 26D4<>
ATI_AGP_FBSKEW<0>  19C2< 19C7<>
ATI_AGP_FBSKEW<1>  19C2< 19C7<>
ATI_BUS_CFG<0>    19B2< 19C7<>
ATI_BUS_CFG<1>    19B2< 19C7<>
ATI_BUS_CFG<2>    19B2< 19C7<>
ATI_CLK27M_IN     18C1< 19B7<
ATI_CLK27M_OSC    18D2<
ATI_CLK27M_OSC_SS  18B2< 18D1<
ATI_DBI_HI_PU     18C6<>
ATI_DBI_LO_PU     18C6<>
ATI_DVOVMODE      21A2<
ATI_GPIO7         19C7<> 26D7<
ATI_GPIO8_PD      19C7<>
ATI_GPIO9_SPN     19C7<>
ATI_GPIO10_SPN    19C7<>
ATI_GPIO11_SPN    19C7<>
ATI_GPIO12_SPN    19C7<>
ATI_GPIO13_SPN    19C7<>
ATI_HSYNC         19D5<> 22C8<
ATI_MEMTEST       18A6<>
ATI_MEMVMODE0     19C7<>
ATI_MEMVMODE1     18A7<
ATI_OSC_OE        18D1<
ATI_PVDD_BYP      21D6<>
ATI_R2SET         19D6<>
ATI_RSET          19C2<
ATI_RSTB_MSK      18C6<>
ATI_SSCLK_IN      18B1< 19B7<>
ATI_SSCLK_UF      18B1<>
ATI_TESTEN        19B7<
ATI_TMDS_CLKN     19B7< 20D5<
ATI_TMDS_CLKP     19B7< 20D5<
ATI_TMDS_DN<0>    19B7< 20D5<
ATI_TMDS_DN<1>    19B7< 20D5<
ATI_TMDS_DN<2>    19B7< 20D3<
ATI_TMDS_DP<0>    19B7< 20D5<
ATI_TMDS_DP<1>    19B7< 20D3<
ATI_TMDS_DP<2>    19B7< 20D3<
ATI_TPVDD_BYP     21D1<>
ATI_VSYNC         19D5<> 22C8<
ATI_XICLK_SKEW<0>  19C2< 19C7<>
ATI_XICLK_SKEW<1>  19B2< 19C7<>
AUDIO_EXT_MCLK_SEL  26C7<> 26D7<
AUDIO_LI_DIST_RC  14B5<> 26C5<>
AUDIO_LI_OPTICAL_PLUG_L  26C5<> 26D7<
AUDIO_LI_SPDIF_PLUG_L  14B5<> 14B7< 26D8<
AUDIO_LO_DET_L    14B5< 26C5<
AUDIO_LO_MUTE_L   26C5<> 26C7<>
AUDIO_LO_OPTICAL_PLUG_L  26C5<> 26D7<
AUDIO_LO_SPDIF_PLUG_L  14B5<> 14C7< 26D8<
AUDIO_MCLK_SEL    14B5<> 14C7< 26D8<
AUDIO_SPDIF_GPO0  14B5<> 14B7<
AUDIO_SPDIF_RESET  14C5<>
AUDIO_SPDIF_RESET_C  14B5<> 14D7< 26D6<
AUDIO_SPDIF_RESET_L  14B5<> 14B7< 14C5<> 14D6<
AUDIO_SPKR_MUTE_F  26C5<> 26C7<
BATTERY_HIGH      32B7<>
BATTV_LOW         32B8<>
BATT_14PBUS_EN    32C1<>
BATT_14V_GATE     32C1<>
BATT_24PBUS_EN    32C2<>
BATT_24V_GATE     32C2<>
BATT_CLK          32A4< 40C3>
BATT_DATA         32A4< 40C3>
BATT_DIV          32A5<
BATT_ISNS_OUT     24A4<>
BATT_ISNS_R       24A3<>
BATT_LOW          32A6<>
BATT_LOW_L        32B6<>
BATT_NEG          32A4<> 39C6> 40C3>
BBANG_HRESET_L    6A2< 6B3> 40C1>
BBANG_JTAG_TCK    6A4< 6B1< 6D2<
BBANG_TCK_EN      6A4<
BB_EEPR_ADDR0     6D3>
BB_EEPR_ADDR1     6D3>
BB_EEPR_ADDR2     6D3<
BB_MISO           6B3<> 6D2<
BB_MOSI           6B3<> 6D2<
BB_RESET_L        6C3<
BB_SCK            6B3<> 6D2<
BCKFD_PROT_EN_L   32C6<>
BCKFD_PROT_GATE   32D6<>
BFR_TDO           6C1<> 6D2<
BRIGHT_PWM        22A1< 40A7>
BRIGHT_PWM_UF     22A2<>
BT_USB_DM         14C1< 25B2<> 38B2> 40B6>
BT_USB_DP         14C1< 25B2<> 38B2> 40B6>
CAPSLOCK_LED_L    31C7<
CBUS_ADDR<0>      17B1< 17B4>
CBUS_ADDR<1>      17B1< 17B4>
CBUS_ADDR<2>      17B1< 17B4>
CBUS_ADDR<3>      17B1< 17B4>
CBUS_ADDR<4>      17B1< 17B4>
CBUS_ADDR<5>      17B1< 17B4>
CBUS_ADDR<6>      17B1< 17B4>
CBUS_ADDR<7>      17B1< 17B4>
CBUS_ADDR<8>      17B1< 17B4>
CBUS_ADDR<9>      17B1< 17B4>
CBUS_ADDR<10>     17B4< 17C1>
CBUS_ADDR<11>     17B1< 17B4>
CBUS_ADDR<12>     17B1< 17B4>
CBUS_ADDR<13>     17B1< 17B4>
CBUS_ADDR<14>     17B1< 17B4>
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CBUS_ADDR<17>     17B2< 17B4>
CBUS_ADDR<18>     17B2< 17B4>
CBUS_ADDR<19>     17B2< 17B4>
CBUS_ADDR<20>     17B2< 17B4>
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CBUS_ADDR<22>     17A4> 17B2<
CBUS_ADDR<23>     17A4> 17B2<
CBUS_ADDR<24>     17A4> 17B2<
CBUS_ADDR<25>     17A4> 17B2<
CBUS_ADDR_10_UF   17B5>
CBUS_BVD1_L       17B2< 17C4<
CBUS_BVD2_L       17B2< 17C4<
CBUS_CE1_L        17C4> 17C2<
CBUS_CE2_L        17B4> 17C2<
CBUS_DATA<0>      17A1< 17A4<>
CBUS_DATA<1>      17A1< 17A4<>
CBUS_DATA<2>      17A1< 17A4<>
CBUS_DATA<3>      17A4<> 17C1<
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CBUS_DATA<5>      17A4<> 17C1<
CBUS_DATA<6>      17A4<> 17C1<
CBUS_DATA<7>      17A4<> 17C1<
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CBUS_DATA<9>      17A2< 17A4<>
CBUS_DATA<10>     17A2< 17A4<>
CBUS_DATA<11>     17A4<> 17C2<
CBUS_DATA<12>     17A4<> 17C2<
CBUS_DATA<13>     17A4<> 17C2<
CBUS_DATA<14>     17A4<> 17C2<
CBUS_DATA<15>     17A4<> 17C2<
CBUS_DET_1_L      17C2< 17C4< 40B8>
CBUS_DET_2_L      17A2< 17C4< 40B8>
CBUS_INPACK_L     17B2< 17B4<
CBUS_INT_L        14B5<> 14B7< 17A7<>
CBUS_IORD_L       17B2< 17C4>
CBUS_IOWR_L       17B2< 17C4>
CBUS_MFUNC1_PD    17A7<> 17A7<
CBUS_MFUNC2_PD    17A7<> 17A7<
CBUS_MFUNC3_PD    17A7<> 17A7<
CBUS_MFUNC4_PD    17A7<> 17A7<
CBUS_MFUNC5_PD    17A7<> 17A7<
CBUS_MFUNC6_PD    17A7< 17A7<>
CBUS_OE_L         17C1< 17C4>
CBUS_PCI_GNT_L    12C5> 17A7<
CBUS_PCI_IDSEL    17B7<
CBUS_PCI_PERR_L   17B7<> 17D7<
CBUS_PCI_REQ_L    12A7> 12D7<> 17A7>
CBUS_PCI_RESET_L  17A7<
CBUS_PCI_SERR_L   17B7> 17D7<
CBUS_READY        17B1< 17C4<
CBUS_REG_L        17B2< 17C4>
CBUS_RESET_L      17B2< 17C4>
CBUS_SUSPEND_PU   17A7< 17D7<
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CBUS_VCCD1_L      17C4<>
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CBUS_VS1          17B2< 17C4<>
CBUS_VS2          17B2< 17C4<>
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CBUS_WE_L         17B1< 17C4<>
CEUS_IOP_L        17A1< 17B4<
CO_ADORSEL        14B7<
CG_CLKOUT         14B6<>
CG_PLSEL          14B7< 14C5<
CG_LOCK           14B7<>
CG_RESET_L        14B7<
CG_SYSCLK_EN      14A6< 14B7<
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CHARGE_LED_L      31C6<> 31D7< 32D8<> 40D2>
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CHGND2            39A6>
CHGND3            39A6>
CHGND4            39A6> 40B6>
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CLK33M_AIRPORT_UF  12C7<> 37C1>
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CLK33M_CBUS_UF    12C7<> 37C1>
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CLK33M_USB2_UF    12C7<> 37C1>
CLK66M_AGP_15V_TP  12C4>
CLK66M_GPU_AGP    12C8< 18B7< 37C1>
CLK66M_GPU_AGP_UF  12C7<> 37C1>
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CLKENET_LINK_GTX  13C5<> 37A1>
CLKENET_LINK_RX   13D5< 28D2< 37B1>
CLKENET_LINK_TX   13D5< 28D8< 37A1>
CLKENET_PHY_GBE_REF  28C7<> 37B1>
CLKENET_PHY_GTX   13C6< 28C7< 37A1>
CLKENET_PHY_RX    28C7<> 37B1>
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CLKFW_LINK_PCLK   13C3<> 29C3< 37A1>
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COMM_RESET_L      14C5<> 26D3<> 40C4>
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COMM_RXD          14C2< 26D1<> 40B2>
COMM_SHUTDOWN     14C5<> 26D3<> 40C4>
COMM_TXCC         14C2< 26D2<> 40C2>
COMM_TXD_L        14C2< 26D2<> 40C2>
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CPU_BR_L          5C7> 8D2< 8D6<> 37D5>
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CPU_DBG_L         5C
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NEC_RIGHT_USB_PWREN	27B5<> 33A7<> 40C1>
NEC_RREF	27B5<>
NEC_SMI_L_TP	27A7>
NEC_USB_DAM	27B4< 27C2<> 38B2>
NEC_USB_DAP	27A4< 27C2<> 38B2>
NEC_USB_DBM	27A4< 27C2<> 38B2>
NEC_USB_DBP	27A4< 27C2<> 38B2>
NEC_USB_RSDM1	27C5<> 38B2>
NEC_USB_RSDM2	27C5<> 38B2>
NEC_USB_RSDP1	27C5<> 38B2>
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NEC_XT2	27D5<> 37B1>
NEC_XT2_R	27D4<
NTEST1_TP	27B5<
NUMLOCK_LED_L	31D7<
OVER_18V_ADJ	32C3<>
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PC0_PD	23B2< 23B4<>
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PMU_AC_IN	31B4<>
PMU_BATT0_DET_L	31B4<>
PMU_BATT1_DET_L_PU	31B4<> 31D2<
PMU_BATT_DET_L	31A8<> 31B3< 31D2< 32A4<> 40C3>
PMU_BYTE	31B6< 31C7<
PMU_CAPSLOCK_LED_L	31C6<>
PMU_CHARGE_V	31C4<> 32B8<>
PMU_CHRG_BATT_0	31C4<> 32A8<>
PMU_CLK	14C2<> 31C4<>
PMU_CNVSS	31B6< 31C7<
PMU_CPU_HRESET_L	6A2< 6C3<> 31C4<>
PMU_CUSTOM_RESET	31A8<>
PMU_CUSTOM_RESET_L	31A7<> 31B8<
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PMU_I2C_CLK	31B4<> 31C2<
PMU_I2C_DATA	31B4<> 31C2<
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PMU_INT_NMI	14B5<> 14B7< 31D4<>
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PMU_LID_CLOSED_L	23A8< 23B4<> 31B2< 31C4<>
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PMU_NMI_L	31C2< 31C4<>
PMU_NUMLOCK_LED_L	31C6<>
PMU_OOPS	31B2< 31B4<>
PMU_PME_L	14B5<> 27B8< 31B2< 31C4<>
PMU_POWERUP_OK	31B4<> 31D2<
PMU_POWER_UP_L	30D8<> 31C6<> 31D7< 34B8<
PMU_REQ_L	14B7< 14C2> 31C4<>
PMU_RESET_BUTTON_L	26A2< 31C4<> 31D2<
PMU_RESET_L	31B7<>
PMU_SELECT	31C6<>
PMU_SLEEP_LED	23B4<>
PMU_SLEEP_LED_L	23B3<> 31C4<>
PMU_SMB_CLK	31B4<> 31C2< 32A3<
PMU_SMB_DATA	31B4<> 31C2< 32A2<
PMU_TO_INT	14C2<> 31C4<>
POWER_UP	30D8<>
POWER_VALID	31B2< 31C4<>
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PP3V3_SI_AVCC2	20C5< 39B3>
PP3V3_SI_PVCC1	20C7< 39B3>
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PP3V3_SI_VCC1	20D7< 39B3>
PP3V3_SI_VCC2	20C5< 39B3>
PWR_BUTTON_L	23A7<> 26C1< 40B2>
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RAM_DATA_A<61>	10C1<> 11A6<>
RAM_DATA_A<62>	10C1<> 11A6<>
RAM_DATA_A<63>	10C1<> 11A6<>
RAM_DATA_B<0>	10C8<> 11D3<>
RAM_DATA_B<7..0>	37C5>
RAM_DATA_B<1>	10C8<> 11D3<>
RAM_DATA_B<2>	10C8<> 11D3<>
RAM_DATA_B<3>	10C8<> 11D3<>
RAM_DATA_B<4>	10C8<> 11D5<>
RAM_DATA_B<5>	10C8<> 11D5<>
RAM_DATA_B<6>	10C8<> 11D5<>
RAM_DATA_B<7>	10C8<> 11D5<>
RAM_DATA_B<8>	10C8<> 11D3<>
RAM_DATA_B<15..8>	37C5>
RAM_DATA_B<9>	10C8<> 11D3<>
RAM_DATA_B<10>	10C8<> 11D3<>
RAM_DATA_B<11>	10C8<> 11D3<>
RAM_DATA_B<12>	10C8<> 11D5<>
RAM_DATA_B<13>	10C8<> 11D5<>
RAM_DATA_B<14>	10C8<> 11D5<>
RAM_DATA_B<15>	10C8<> 11D5<>
RAM_DATA_B<16>	10C6<> 11D3<>
RAM_DATA_B<31..16>	37B5>
RAM_DATA_B<17>	10C6<> 11C3<>
RAM_DATA_B<18>	10C6<> 11C3<>
RAM_DATA_B<19>	10C6<> 11C3<>
RAM_DATA_B<20>	10C6<> 11D5<>
RAM_DATA_B<21>	10C6<> 11C5<>
RAM_DATA_B<22>	10C6<> 11C5<>
RAM_DATA_B<23>	10C6<> 11C5<>
RAM_DATA_B<24>	10C6<> 11C3<>
RAM_DATA_B<25>	10C6<> 11C3<>
RAM_DATA_B<26>	10C6<> 11C3<>
RAM_DATA_B<27>	10C6<> 11C3<>
RAM_DATA_B<28>	10C6<> 11C5<>
RAM_DATA_B<29>	10C6<> 11C5<>
RAM_DATA_B<30>	10C6<> 11C5<>
RAM_DATA_B<31>	10C6<> 11C5<>
RAM_DATA_B<32>	10D4<> 11B3<>
RAM_DATA_B<47..32>	37B5>
RAM_DATA_B<33>	10C4<> 11B3<>
RAM_DATA_B<34>	10C4<> 11B3<>
RAM_DATA_B<35>	10C4<> 11B3<>
RAM_DATA_B<36>	10C4<> 11B5<>
RAM_DATA_B<37>	10C4<> 11B5<>
RAM_DATA_B<38>	10C4<> 11B5<>
RAM_DATA_B<39>	10C4<> 11B5<>
RAM_DATA_B<40>	10C4<> 11B3<>
RAM_DATA_B<41>	10C4<> 11B3<>
RAM_DATA_B<42>	10C4<> 11A3<>
RAM_DATA_B<43>	10C4<> 11A3<>
RAM_DATA_B<44>	10C4<> 11B5<>
RAM_DATA_B<45>	10C4<> 11B5<>
RAM_DATA_B<46>	10C4<> 11A5<>
RAM_DATA_B<47>	10C4<> 11A5<>
RAM_DATA_B<48>	10D2<> 11A3<>
RAM_DATA_B<55..48>	37B5>
RAM_DATA_B<49>	10C2<> 11A3<>
RAM_DATA_B<50>	10C2<> 11A3<>
RAM_DATA_B<51>	10C2<> 11A3<>
RAM_DATA_B<52>	10C2<> 11A5<>
RAM_DATA_B<53>	10C2<> 11A5<>
RAM_DATA_B<54>	10C2<> 11A5<>
RAM_DATA_B<55>	10C2<> 11A5<>
RAM_DATA_B<56>	10C2<> 11A3<>
RAM_DATA_B<63..56>	37A5>
RAM_DATA_B<57>	10C2<> 11A3<>
RAM_DATA_B<58>	10C2<> 11A3<>
RAM_DATA_B<59>	10C2<> 11A3<>
RAM_DATA_B<60>	10C2<> 11A5<>
RAM_DATA_B<61>	10C2<> 11A5<>
RAM_DATA_B<62>	10C2<> 11A5<>
RAM_DATA_B<63>	10C2<> 11A5<>
RAM_DQM_A<0>	10B8<> 11D6<> 37C5>
RAM_DQM_A<1>	10C7<> 11D6<> 37C5>
RAM_DQM_A<2>	10B6<> 11C6<>
RAM_DQM_A<3..2>	37B5>
RAM_DQM_A<3>	10C5<> 11C6<>
RAM_DQM_A<4>	10B4<> 11B6<>
RAM_DQM_A<5..4>	37B5>
RAM_DQM_A<5>	10C3<> 11A6<>
RAM_DQM_A<6>	10B2<> 11A6<> 37B5>
RAM_DQM_A<7>	10C1<> 11A6<> 37A5>
RAM_DQM_B<0>	10C8<> 11D5<> 37C5>
RAM_DQM_B<1>	10C8<> 11D5<> 37C5>
RAM_DQM_B<2>	10C6<> 11C5<>
RAM_DQM_B<3..2>	37B5>
RAM_DQM_B<3>	10C6<> 11C5<>
RAM_DQM_B<4>	10C4<> 11B5<>
RAM_DQM_B<5..4>	37B5>
RAM_DQM_B<5>	10C4<> 11B5<>
RAM_DQM_B<6>	10C2<> 11A5<> 37B5>
RAM_DQM_B<7>	10C2<> 11A5<> 37A5>
RAM_DQS_A<0>	10B8<> 11D8<> 37C5>
RAM_DQS_A<1>	10C7<> 11D8<> 37C5>
RAM_DQS_A<2>	10B6<> 11C8<>
RAM_DQS_A<3..2>	37B5>
RAM_DQS_A<3>	10C5<> 11C8<>
RAM_DQS_A<4>	10B4<> 11B8<>
RAM_DQS_A<5..4>	37B5>
RAM_DQS_A<5>	10C3<> 11A8<>
RAM_DQS_A<6>	10B2<> 11A8<> 37B5>
RAM_DQS_A<7>	10C1<> 11A8<> 37A5>
RAM_DQS_B<0>	10C8<> 11D3<> 37C5>
RAM_DQS_B<1>	10C8<> 11D3<> 37C5>
RAM_DQS_B<2>	10C6<> 11C3<>
RAM_DQS_B<3..2>	37B5>
RAM_DQS_B<3>	10C6<> 11C3<>
RAM_DQS_B<4>	10C4<> 11B3<>
RAM_DQS_B<5..4>	37B5>
RAM_DQS_B<5>	10C4<> 11B3<>
RAM_DQS_B<6>	10C2<> 11A3<> 37B5>
RAM_DQS_B<7>	10C2<> 11A3<> 37A5>
RAM_MUXSEL_H	10A3< 10A5< 10B1<> 10B3<> 37A5>
RAM_MUXSEL_L	10A3< 10A5< 10B5<> 10B7<> 37A5>
RAM_RAS_L	9A4< 11B5<> 11B6<> 37A5>
RAM_WE_L	9A4< 11B3<> 11B8<> 37A5>
RESET_VREF	6C3<>
RF_DISABLE_L_SPN	25D6<> 40C1>
RIGHT_USB_DM	27A3< 33A7<> 38A2> 40D1>
RIGHT_USB_DP	27A3< 33A7<> 38A2> 40D1>
RJ45_C0_PD	28B2<>
RJ45_C1_PD	28B2<>
RJ45_C2_PD	28B2<>
RJ45_C3_PD	28B2<>
RJ45_DN<0>	28B2<> 38D2> 40B3>
RJ45_DN<1>	28B2<> 38D2> 40B3>
RJ45_DN<2>	28B2<> 38D2> 40A3>
RJ45_DN<3>	28B2<> 38D2> 40A3>
RJ45_DP<0>	28B2<> 38D2> 40B3>
RJ45_DP<1>	28B2<> 38D2> 40B3>
RJ45_DP<2>	28B2<> 38D2> 40A3>
RJ45_DP<3>	28B2<> 38D2> 40A3>
ROM_CS_L	9B3< 12A5< 25B6<> 40B1>
ROM_OE_L	9B3< 12A5< 25C5<> 40B1>
ROM_ONBOARD_CS_L	9B3< 25C6<> 40B1>
ROM_RW_L	9B3< 12A5< 25C6<> 40B1>
ROM_WP_L	9B3<
RSDM3_TP	27C5>
RSDM4_TP	27C5>
RSDM5_TP	27C5>
RSDP3_TP	27C5>
RSDP4_TP	27C5>
RSDP5_TP	27C5>
RUN_OR_AC	30D7<>
SI_I2C_CLK	19C5<> 20B5< 20C7<
SI_I2C_DATA	19C5<> 20B5<> 20C7<>
SI_MASTER	20B8<
SI_M_HTPLG	20B7<
SI_RESET_L	20B5< 20C7< 20D8<
SI_SECONDARY	20A7<
SI_S_HTPLG	20A5<
SI_TMDS_CLKN	20B7< 20C4<
SI_TMDS_CLKP	20B7< 20C4<
SI_TMDS_DN<0>	20B7< 20C4<
SI_TMDS_DN<1>	20B7< 20C4<
SI_TMDS_DN<2>	20B7< 20C4<
SI_TMDS_DN<3>	20A5< 20C2<
SI_TMDS_DN<4>	20A5< 20C2<
SI_TMDS_DN<5>	20A5< 20C2<
SI_TMDS_DP<0>	20B7< 20C4<
SI_TMDS_DP<1>	20B7< 20C4<
SI_TMDS_DP<2>	20B7< 20C4<
SI_TMDS_DP<3>	20A5< 20C2<
SI_TMDS_DP<4>	20A5< 20C2<
SI_TMDS_DP<5>	20A5< 20C2<
SI_VREF	20A8< 20B8<
SLAVE_SWING	20A5<
SLEEP	23C4<> 31B6<> 31D7< 34A4< 34A6< 34B3< 34B8<> 36B3< 36D2< 40A1>
SLEEP_ANODE	23C2< 26C5<>
SLEEP_LED	40B6>
SLEEP_LED_I	23C2<
SLEEP_LED_L	23C3<
SLEEP_LED_SW_L	23C3<>
SLEEP_LED_UF	23C2<
SLEEP_LS5	34A5<> 34A8<
SLEEP_LS5_EN_L	34A5<>
SLEEP_L_LS5	19A7<> 28A8<> 34A5<> 35C8<> 36C8<
SLEEP_L_LS5_EN_L	34A6<>
SLEEP_L_LS5_INV	36A3< 36C2< 36C8<>
SLEEP_L_LS5_NET	34B3<> 36C8<>
SLEEP_NET	34A3<>
SLEEP_NET_INV	34A3<>
SMC_TP	27B5<
SND_AGND	26C6<> 39B6>
SND_AMP_MUTE	26D4< 26D4<> 40A4>
SND_AMP_MUTE_INV	26C8< 26D4<
SND_AMP_MUTE_L	14C5<> 26D3<>
SND_CLKOUT	14B1< 26C8< 37B1> 40D6>
SND_HP_MUTE	26C4<>
SND_HP_MUTE_INV	40A4>
SND_HP_MUTE_L	14C5<> 26C4<>
SND_HP_SENSE_L	40C6>
SND_HW_RESET_L	14A7< 14B5<> 26B8< 40C6>
SND_LIN_SENSE_L	40C6>
SND_SCLK	14B1< 26B8< 37B1> 40C6>
SND_SYNC	14B1< 26C8< 40D6>
SND_TO_AUDIO	14B1< 26C8< 40D6>
SOFT_PWR_ON_L	22D1< 23A8< 31A8<> 31C6<> 31D7< 35A3<>
SOUND_SPDIF_GPO0	14C5< 26D8<
SPDIF_GPO0	26D7<> 26D7<
SRCLK_TP	27A5> 40A4>
SRMOD_TP	27A5< 40A4>
ST7_ICP_SEL_PD	23A2< 23C6<
ST7_KBD_LED_OUT	23A5<> 23C4<>
ST7_OSC1	23C6<
ST7_OSC2	23C6<>
ST7_PB6_PD	23A2< 23C4<>
ST7_RESET_L	23C6<>
ST7_SENSOR4_SCK_PD	23B2< 23C4<>
ST7_SENSOR4_SDA_PD	23B2< 23C4<>
ST7_SENSOR5_SCK	23B2< 23C4<>
ST7_SENSOR5_SDA	23B3< 23C4<>
ST7_SLEEP_LED_H	23B4<> 23C4<>
ST7_XTAL_IN	23C6<
STOP_AGP_L	12D2< 12D4<>
SUPPLY_M_DM	26A8< 26B6<
SUPPLY_M_DP	26A8< 26B6<
SUTRO_ALS_GAIN_SW	23C4<> 25B2<> 40C2>
SUTRO_ALS_OUT	23B4<> 25B2<> 40C2>
SYSCLK_CPU	5C4< 8A6< 37D1>
SYSCLK_CPU_UF	8A6<> 37D1>
SYSCLK_DDRCLK_A0	9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L	9D4< 11D8<> 37D1>
SYSCLK_DDRCLK_A0_L_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A0_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1	9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L	9D4< 11A6<> 37D1>
SYSCLK_DDRCLK_A1_L_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_A1_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B0	9D4< 11D3<> 37D1>
SYSCLK_DDRCLK_B0_L	9C4< 11D3<> 37C1>
SYSCLK_DDRCLK_B0_L_UF	9B6<> 9C5< 37D1>
SYSCLK_DDRCLK_B0_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1	9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L	9D4< 11A5<> 37C1>
SYSCLK_DDRCLK_B1_L_UF	9B6<> 9D5< 37D1>
SYSCLK_DDRCLK_B1_UF	9B6<> 9D5< 37D1>
SYSCLK_LA_TP	8A6<>
SYSTEM_CLK_EN	14A5< 14A7< 31C4<>
SYS_BATT_ISNS	24A2< 31C2<
SYS_BATT_ISNS1	31B4<> 31C3<
SYS_BATT_ISNS2	31B4<> 31C3<
TEB_TP	27A5< 40A4>
TEST_TP	27A5< 40A4>
THERM1_A_DM	26A6< 26A8< 38A2>
THERM1_A_DP	26A6< 26A8< 38A2>
THERM1_DM	26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_DP	26A5< 26A5< 26B5<> 26B5< 38A2>
THERM1_M_DM	38A2>
THERM1_M_DP	38A2>
THERM2_A_DM	26A6< 26A7< 38A2>
THERM2_A_DP	26A6< 26A7< 38A2>
THERM2_DM	26A5< 26B5<> 26B5< 38A2>
THERM2_DP	26A5< 26B5<> 26B5< 38A2>
THERM2_M_DM	38A2>
THERM2_M_DP	38A2>
THERM_INV	26B2<>
THERM_L_OC	26B1<> 31B4<>
THERM_L_OC_CONN	23A7<>
TMDS_CLKN	20B2< 20C3< 20D4< 22B7<> 38B2>
TMDS_CLKP	20B3< 20C3< 20D4< 22C7<> 38B2>
TMDS_CLK_CMF	20B3<
TMDS_CONN_CLKN	22B6<> 22C7<> 38B2> 40A8>
TMDS_CONN_CLKP	22C6<> 22C7<> 38B2> 40D7>
TMDS_CONN_DN<0>	22C7<> 22D6<>
TMDS_CONN_DN<1>	22B7<> 22D5<>
TMDS_CONN_DN<2>	22B6<> 22D5<>
TMDS_CONN_DN<3>	20D1<> 22C5<>
TMDS_CONN_DN<4>	20D1<> 22C5<>
TMDS_CONN_DN<5>	20D1<> 22C7<>
TMDS_CONN_DP<0>	22B7<> 22D6<>
TMDS_CONN_DP<1>	22B7<> 22D5<>
TMDS_CONN_DP<2>	22B6<> 22D5<>
TMDS_CONN_DP<3>	20D1<> 22C5<>
TMDS_CONN_DP<4>	20D1<> 22C5<>
TMDS_CONN_DP<5>	20D1<> 22C7<>
TMDS_D0_CMF	20B3<
TMDS_D1_CMF	20A3<
TMDS_D2_CMF	20A3<
TMDS_D3_CMF	20B2<
TMDS_D4_CMF	20B1<
TMDS_D5_CMF	20A1<
TMDS_DN<0>	20B2< 20C3< 20D4< 22C8<> 38B2> 40B8>
TMDS_DN<1>	20A2< 20C3< 20D2< 22B8<> 38B2> 40A8>
TMDS_DN<2>	20A2< 20C3< 20D2< 22B7<> 38B2> 40A8>
TMDS_DN<3>	20B1< 20C1< 20D2<>
TMDS_DN<4>	20B1< 20C1< 20D2<>
TMDS_DN<5>	20A1< 20C1< 20D2<>
TMDS_DP<0>	20B3< 20C3< 20D4< 22B8<> 38B2> 40A8>
TMDS_DP<1>	20A3< 20C3< 20D2< 22B8<> 38B2> 40A8>
TMDS_DP<2>	20A3< 20C3< 20D2< 22B7<> 38B2> 40A8>
TMDS_DP<3>	20B2< 20C1< 20D2<>
TMDS_DP<4>	20B2< 20C1< 20D2<>
TMDS_DP<5>	20A2< 20C1< 20D2<>
TMDS_MASTER	20B8<
TMDS_SYNC	20A7< 20B8<
TPAD_F_RXD	40C4>
TPAD_F_TXD	40C4>
TPAD_RXD	31C2< 31C4<>
TPAD_TXD	31B2< 31C4<>
TPS2211_SHDN_L_PU	17C4<
TP_BB_XTAL	6C3<>
TP_MMM_ICSP_PGC	24C3<>
TP_MMM_ICSP_PGD	24C3<>
TP_MMM_ICSP_PGM	24C3<>
TV_C	22A6<> 40D6>
TV_COMP	22A6<> 40D6>
TV_GND1	22B6<> 39B6> 40A7>
TV_GND2	22A6<> 39B6> 40A7>
TV_Y	22A6<> 40D6>
UIDE_ADDR<0>	13D7<> 25C4<
UIDE_ADDR<2..0>	38C5>
UIDE_ADDR<1>	13D7<> 25C4<
UIDE_ADDR<2>	13D7<> 25B4<
UIDE_CS0_L	13C7<> 25C4< 38C5>
UIDE_CS1_L	13C7<> 25B4< 38C5>
UIDE_DATA<0>	13D7<> 25D4<
UIDE_DATA<6..0>	38C5>
UIDE_DATA<1>	13D7<> 25D4<
UIDE_DATA<2>	13D7<> 25D4<
UIDE_DATA<3>	13D7<> 25D4<
UIDE_DATA<4>	13D7<> 25C4<
UIDE_DATA<5>	13D7<> 25C4<
UIDE_DATA<6>	13D7<> 25C4<
UIDE_DATA<7>	13D7<> 25C4< 38C5>
UIDE_DATA<8>	13D7<> 25C4<
UIDE_DATA<15..8>	38C5>
UIDE_DATA<9>	13D7<> 25C4<
UIDE_DATA<10>	13D7<> 25C4<
UIDE_DATA<11>	13D7<> 25D4<
UIDE_DATA<12>	13D7<> 25B4<
UIDE_DATA<13>	13D7<> 25B4<
UIDE_DATA<14>	13D7<> 25C4<
UIDE_DATA<15>	13D7<> 25B4<
UIDE_DIOR_L	13C7<> 25A4< 38C5>
UIDE_DIOW_L	13C7<> 25A4< 38C5>
UIDE_DMACK_L	13C7<> 25A4< 38C5>
UIDE_DMARQ	13C7<> 38C5>
UIDE_INTRQ	13C7< 38C5>
UIDE_IOCHRDY	13C7< 25A4< 38C5>
UIDE_REF	13C7<> 39D3>
UIDE_RST_L	13C7<> 25A4< 38C5>
USB2_PCI_GNT_L	12C7<> 27B7<
USB2_PCI_INT_L	14B5<> 14C7< 27A8<
USB2_PCI_REQ_L	12A7< 12D7<> 27B7>
USB_D1M	14D1< 27A5> 27B4<
USB_D1P	14D1< 27A4< 27A5>
USB_D2M	27A5>
USB_D2P	27A5>
USB_DAM	14B2<> 14D2< 27A5>
USB_DAP	14B2<> 14D2< 27A5>
USB_DBM	14B2<> 14D1<
USB_DBP	14B2<> 14D1<
USB_DCM	14B2<> 14D2< 27A5>
USB_DCP	14B2<> 14D2< 27A5>
USB_DDM	14B2<> 14C2<
USB_DDP	14B2<> 14C2<
USB_DEM	14B2<> 14C2< 38B2>
USB_DEP	14B2<> 14C2< 38B2>
USB_DFM	14B2<> 14B2< 38B2>
USB_DFP	14B2< 14B2<> 38B2>
USB_OC_AB_L	14B2< 14C7<
USB_OC_CD_L	14B2< 14C7<
USB_OC_EF_L	14B2< 14D7<
USB_PWREN_AB_L	14B2<> 14C7<
USB_PWREN_CD_L	14B2<> 14C7<
USB_PWREN_EF_L	14B2<> 14D7<
USB_TPAD_N	14B1< 23A7<>
USB_TPAD_P	14B1< 23A7<>
VCORE_BOOST	35C4<> 39C1>
VCORE_BST	35C5<> 39C1>
VCORE_CC	35B6<> 39B1>
VCORE_CNTL_RC	19A3<>
VCORE_DH	35B5<> 39C1>
VCORE_DL	35B5<> 39C1>
VCORE_FAST<1>	35D3< 35D5<
VCORE_FAST<2>	35D3< 35D5<
VCORE_FAST<3>	35D3< 35D5<
VCORE_FAST<4>	35D3< 35D5<
VCORE_FB	35B5< 39B1> 40A2>
VCORE_GND	35B5<> 39B1>
VCORE_GNDA	35B6<>
VCORE_GNDDIV	35A4< 35B5< 39B1>
VCORE_GNDDIV_TEST	35A3<>
VCORE_GNDSNS	35A2<> 35A4< 39B1>
VCORE_GNDSNS_TEST	35A3<>
VCORE_ILIM	35C6<> 39C1>
VCORE_LX	35B5<> 39C1>
VCORE_MUX_EN	35D5<> 40A2>
VCORE_MUX_SEL	35D5<>
VCORE_REF	35B6<> 39C1>
VCORE_SEL_OFF_PU	35B6<>
VCORE_SEL_ON	35B6<>
VCORE_SHDN_L	5B3<> 35C6<>
VCORE_SLOW<1>	35D6<
VCORE_SLOW<2>	35D6<
VCORE_SLOW<3>	35D6<
VCORE_SLOW<4>	35D6<
VCORE_SNS	35A1<> 39B1>
VCORE_TIME	35B4<> 39B1>
VCORE_TON	35B6< 39C1>
VCORE_VCC	35C6< 39C1>
VCORE_VGATE	14B6< 14B7< 35B4> 39B1>
VCORE_VID0	40A3>
VCORE_VID1	40A3>
VCORE_VID2	40A3>
VCORE_VID3	40A3>
VCORE_VID4	40A3>
VCORE_VID<0>	35A2<> 35B8<
VCORE_VID<1>	35A2<> 35B8< 35D4<>
VCORE_VID<2>	35A2<> 35B8< 35D4<>
VCORE_VID<3>	35A2<> 35B8< 35D4<>
VCORE_VID<4>	35A2<> 35B8< 35D4<>
VGA_B	22C6<> 22D7< 40D7>
VGA_G	22C5<> 22D7< 40D7>
VGA_HSYNC	22C6<> 22C7< 40D7>
VGA_HSYNC_BUF	22C8<>
VGA_R	22C5<> 22D7< 40D7>
VGA_VSYNC	22C5<> 22C7< 40D7>
VGA_VSYNC_BUF	22C8<>

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U9	CBTV4020	10
U10	CBTV4020	10
U11	PI3B3257	35
U12	CBTV4020	10
U13	CBTV4020	10
U14	LTC3405	28
U15	COMPARATOR_LMC7211	32
U16	LTC1778	19
U17	FEPR_1MX8	9
U18	LTC1625	33
U19	PWR_CNTRL_TPS2211	17
U20	MAX1717	35
U21	COMPARATOR_LMC7211	33
U22	MAX1715	36
U23	AMP_MAX4172	32
U24	7432	22
U25	VREG_LP2951	33
U26	PC115106GU	17
U27	COMPARATOR_LMC7211	31
U28	LTC3707	34
U29	TSB810A3A	29
U30	VREG_LP2951	33
U31	MAX1772	32
U32	EEPROM_32KX8_M24256B	6
U33	M16C62	31
U34	VREG_LM2594	29
U35	51L178	20
U36	LTC1761	29
U37	VREG_LT1962	29
U38	COMPARATOR_LMC7211	32
U39	UPD720101_FBGA	27
U40	OPAMP_MAX4236EUTT	23
U41	MAX6804	31
U42	CLK_GEN_CY28512	14
U43	APOLLO_MPC7447A_360	5 6
U44	RAGE_MBLTY_M11_CSP64_667	18 19 21
U45	INTREPID	8 9 12 13 14 15
U46	COMPARATOR_LMC7211	22
U47	CLK_GEN_CY25811	18
U48	51L178	20
U49	TRANSCEIVER_88E1111	28
U50	OPAMP_LMC7111	32
U51	INA138	24
U52	FEPR_256KX8_ST72264_BGA	23
U53	PIC16F818_QFN	24
U54	VREG_MM1571J	21
U55	VREG_MM1571J	21
U56	741G32	22
U57	741G32	22
U58	LTC3412	36
U59	MM3120	23
U60	LIS3L02AQ	24
U61	ATTINY2313	6
U62	COMPARATOR_LMC7211	30
XW1	SHORT	36
XW2	SHORT	19
XW3	SHORT	35
XW4	SHORT	33
XW5	SHORT	35
XW6	SHORT	36
XW7	SHORT	35
XW8	SHORT	34
XW9	SHORT	26
XW10	SHORT	26
XW11	SHORT	26
XW12	SHORT	22
XW13	SHORT	22
XW14	SHORT	24
XW15	SHORT	35
XW16	SHORT	24
XW17	SHORT	24
XW19	SHORT	32
XW20	SHORT	19
XW21	SHORT	19
XW22	SHORT	19
XW23	SHORT	19
XW24	SHORT	19
XW27	SHORT	21
XW28	SHORT	21
XW29	SHORT	21
XW30	SHORT	21
XW31	SHORT	5
Y1	CRYSTAL	14
Y3	CRYSTAL	28
Y4	CRYSTAL	23
Y5	CRYSTAL	27
Y6	CRYSTAL	31
Y7	CRYSTAL_4PIN	31
ZT1	HOLE_VIA	4
ZT2	MTGHOLE	4
ZT3	HOLE_VIA	4
ZT4	MTGHOLE	4
ZT5	MTGHOLE	4
ZT6	MTGHOLE	4
ZT7	HOLE_VIA	4
ZT8	HOLE_VIA	4
ZT9	HOLE_VIA	4
ZT10	MTGHOLE	4
ZT11	MTGHOLE	4
ZT12	HOLE_VIA	4
ZT13	HOLE_VIA	4
ZT14	HOLE_VIA	4
ZT15	HOLE_VIA	4
ZT16	MTGHOLE	4
ZT17	HOLE_VIA	4
ZT18	HOLE_VIA	4
ZT19	HOLE_VIA	4
ZT20	HOLE_VIA	4
ZT21	HOLE_VIA	4
ZT22	HOLE_VIA	4
ZT23	HOLE_VIA	4
ZT24	HOLE_VIA	4
ZT25	HOLE_VIA	4
ZT26	HOLE_VIA	4
ZT27	HOLE_VIA	4
ZT28	HOLE_VIA	4
ZT29	HOLE_VIA	4
ZT30	HOLE_VIA	4
ZT31	HOLE_VIA	4
ZT32	HOLE_VIA	4
ZT33	HOLE_VIA	4
ZT34	HOLE_VIA	4
ZT35	HOLE_VIA	4
ZT36	HOLE_VIA	4
ZT37	HOLE_VIA	4
ZT38	HOLE_VIA	4
ZT39	HOLE_VIA	4
ZT40	HOLE_VIA	4
ZT41	HOLE_VIA	4
ZT42	HOLE_VIA	4
ZT43	HOLE_VIA	4
ZT44	HOLE_VIA	4
ZT45	HOLE_VIA	4
ZT46	HOLE_VIA	4
ZT47	HOLE_VIA	4
ZT48	HOLE_VIA	4
ZT49	HOLE_VIA	4
ZT50	HOLE_VIA	4
ZT51	HOLE_VIA	4
ZT52	HOLE_VIA	4
ZT53	HOLE_VIA	4
ZT54	HOLE_VIA	4
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ZT59	HOLE_VIA	4
ZT60	HOLE_VIA	4
ZT61	HOLE_VIA	4
ZT62	HOLE_VIA	4
ZT63	HOLE_VIA	4
ZT64	HOLE_VIA	4
ZT65	HOLE_VIA	4
ZT66	HOLE_VIA	4

ZT67	HOLE_VIA	4
ZT68	HOLE_VIA	4
ZT69	HOLE_VIA	4
ZT70	HOLE_VIA	4
ZT71	HOLE_VIA	4
ZT72	HOLE_VIA	4
ZT73	HOLE_VIA	4
ZT74	HOLE_VIA	4
ZT75	HOLE_VIA	4
ZT76	HOLE_VIA	4
ZT77	HOLE_VIA	4
ZT78	HOLE_VIA	4
ZT79	HOLE_VIA	4
ZT80	HOLE_VIA	4
ZT81	HOLE_VIA	4
ZT82	HOLE_VIA	4
ZT83	MTGHOLE	4