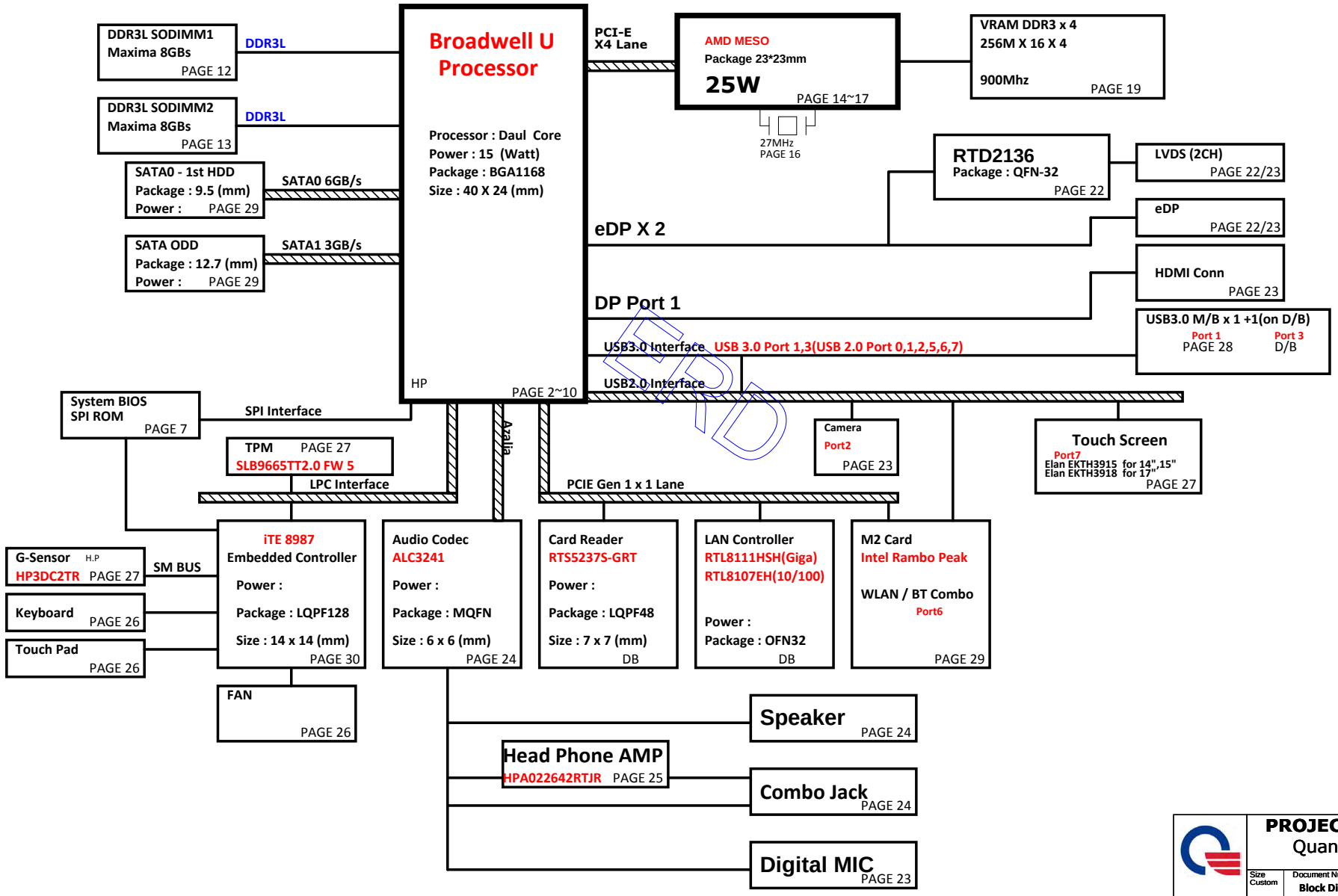
X11 DIS (14" / 15" / 17") Chocolate X11
Intel Cresent Bay ULT Platform Block Diagram



Note

VGA/CPU need check PN

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Block Diagram	1A

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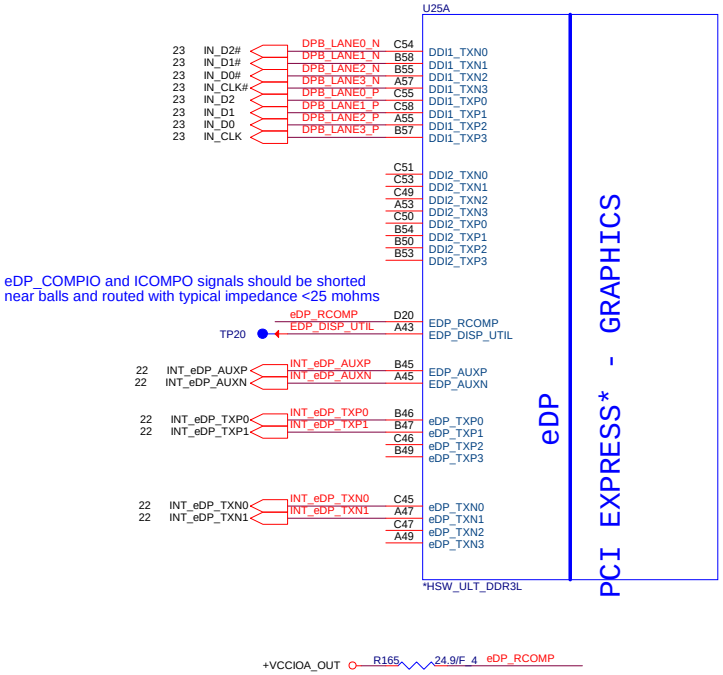
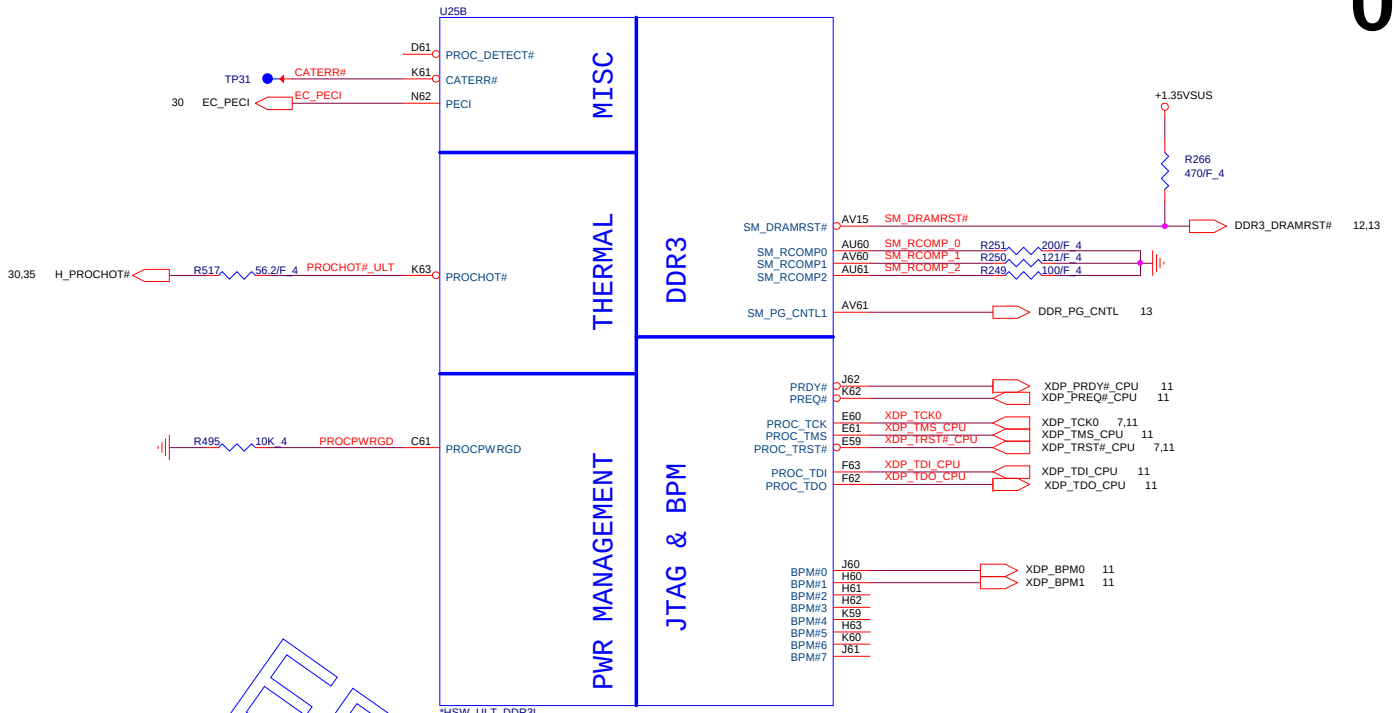
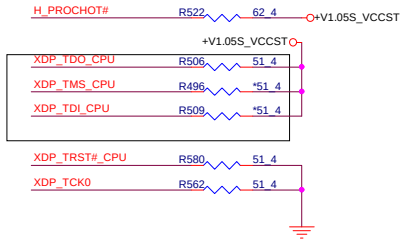


eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms

eDP_COMPIO and ICOMPO signals should be shorted near balls and routed with typical impedance <25 mohms



Processor pull-up (CPU)



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 1/9(eDP/DDI)	1A

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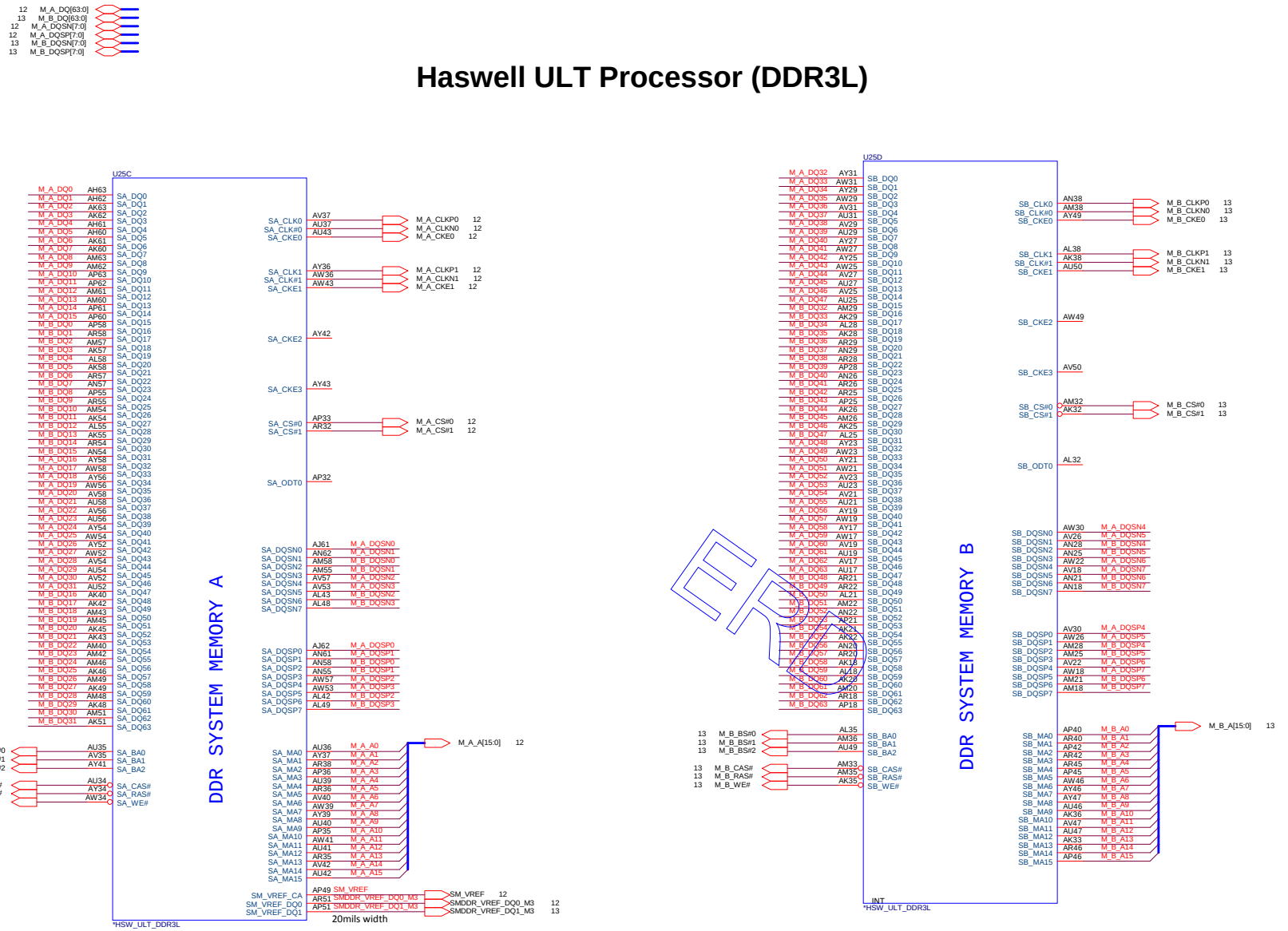
Haswell ULT Processor (DDR3L)



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Quanta Computer Inc.	
Size: Custom	Document Number: ULT 2/9 (DDR3 I/F)
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POWER

32A
+VCC_CORE

U25F
HSW ULT POWER
*HSW_ULT_DDR3L

1.4A
+1.35VSUS
Close to CPU

Direct tie to CPU VCC/VSS-Ball

CFG0-19 need Reserve TP

U25E
RESERVED
*HSW_ULT_DDR3L

Layout note: need routing together and ALERT need between CLK and DATA.

SVID ALERT
SVID CLK
SVID DATA

Place PU resistor close to VR

100- ±1% pull-up to VCC near processor.

IO Thrm Protect
For 65 degree, 1.8v limit, (SW)
For 75 degree, 1.2v limit, (HW)

ERD

Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

	1	0	Circuit
CFG3 (MSR Privacy Bit Feature)	Debug capability is determined by IA32_Debug_Interface_MSR (C80h) bit[0] setting	IA32_Debug_Interface_MSR (C80h) bit[0] default setting overridden	CFG3 R543 *1K_4
CFG4 (eDP enable)	Disabled	Enabled	CFG4 R542 1K_4

+VCCIOA_OUT 2
+VCCIO_OUT 6

+1.35VSUS 2,12,13,33
+1.05V 2,7,9,10,11,27,30,34,35,36
+VCC_CORE 35

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Quanta Computer Inc.

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Custom	04 – ULT 3/9 (POWER-1)	1A
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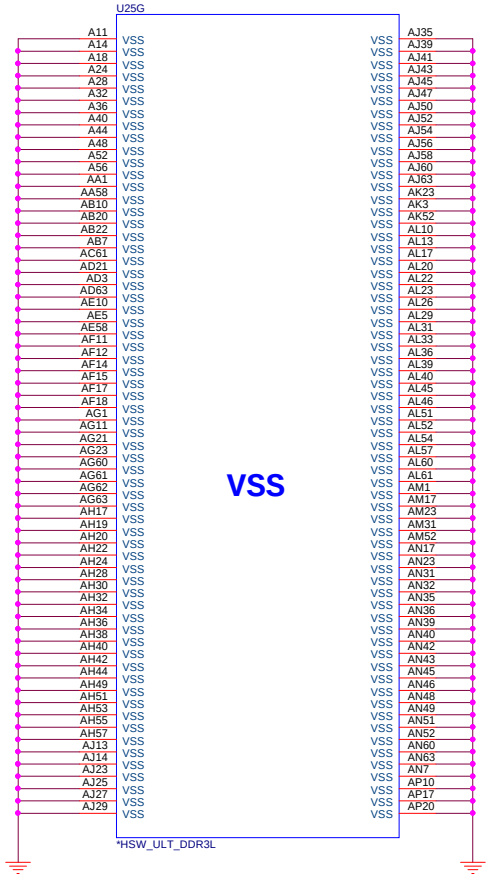

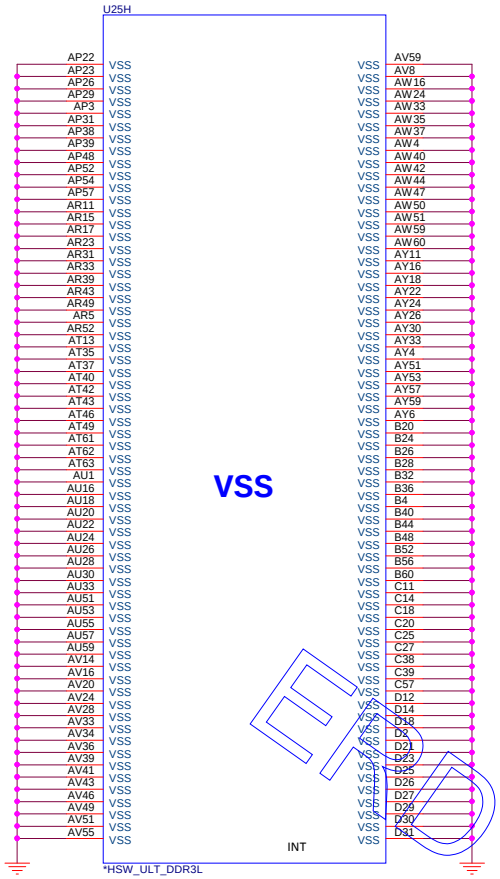

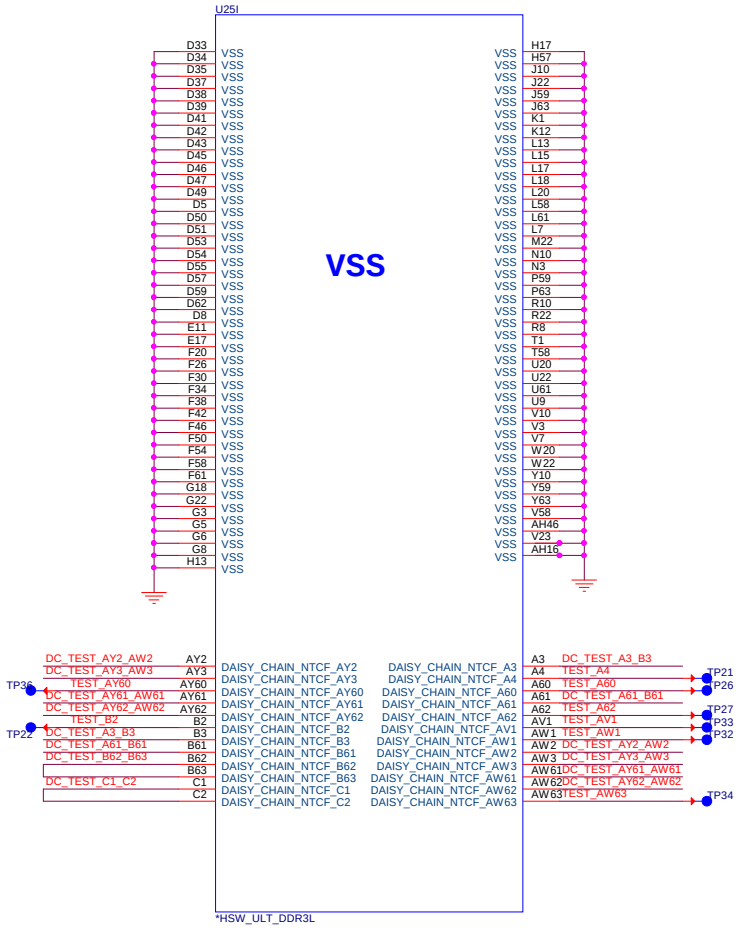

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Size: Custom	Document Number: ULT 4/9 (RSV,GND)	Rev: 1A
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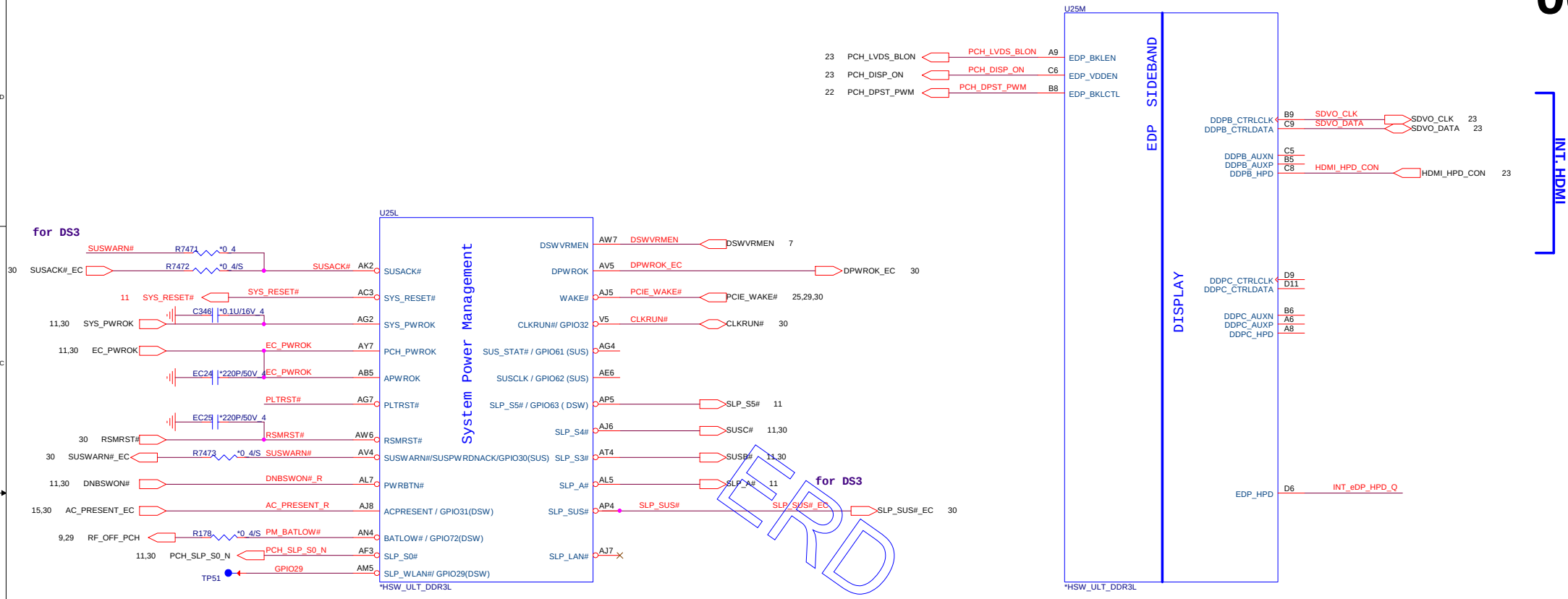
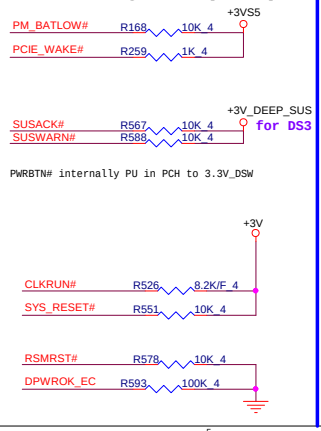
Lynx Point-LP Platform Controller Hub (LVDS,DDI)

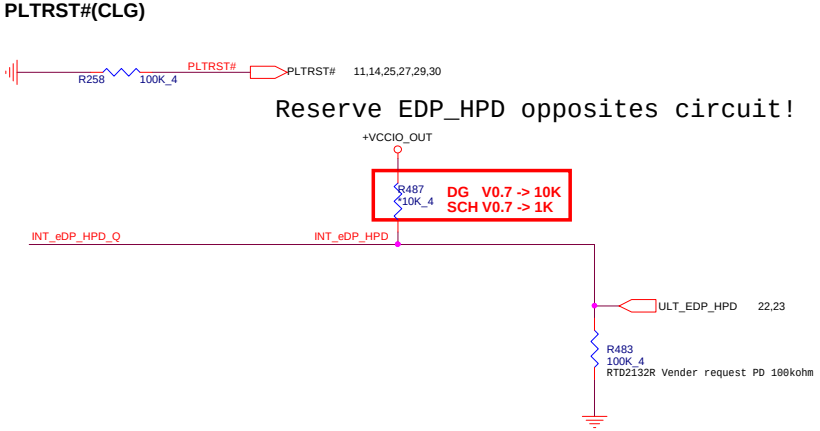
06



PCH Pull-high/low(CLG)



PLTRST#(CLG)



System PWR_OK(CLG)

7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35,36 +3V
9,10,11,27,29,30,32,34,36,37,39 +3VS5

	PROJECT : X11 Quanta Computer Inc.		
Size Custom	Document Number **ULT 5/9(Power Manger)**		Rev 1A
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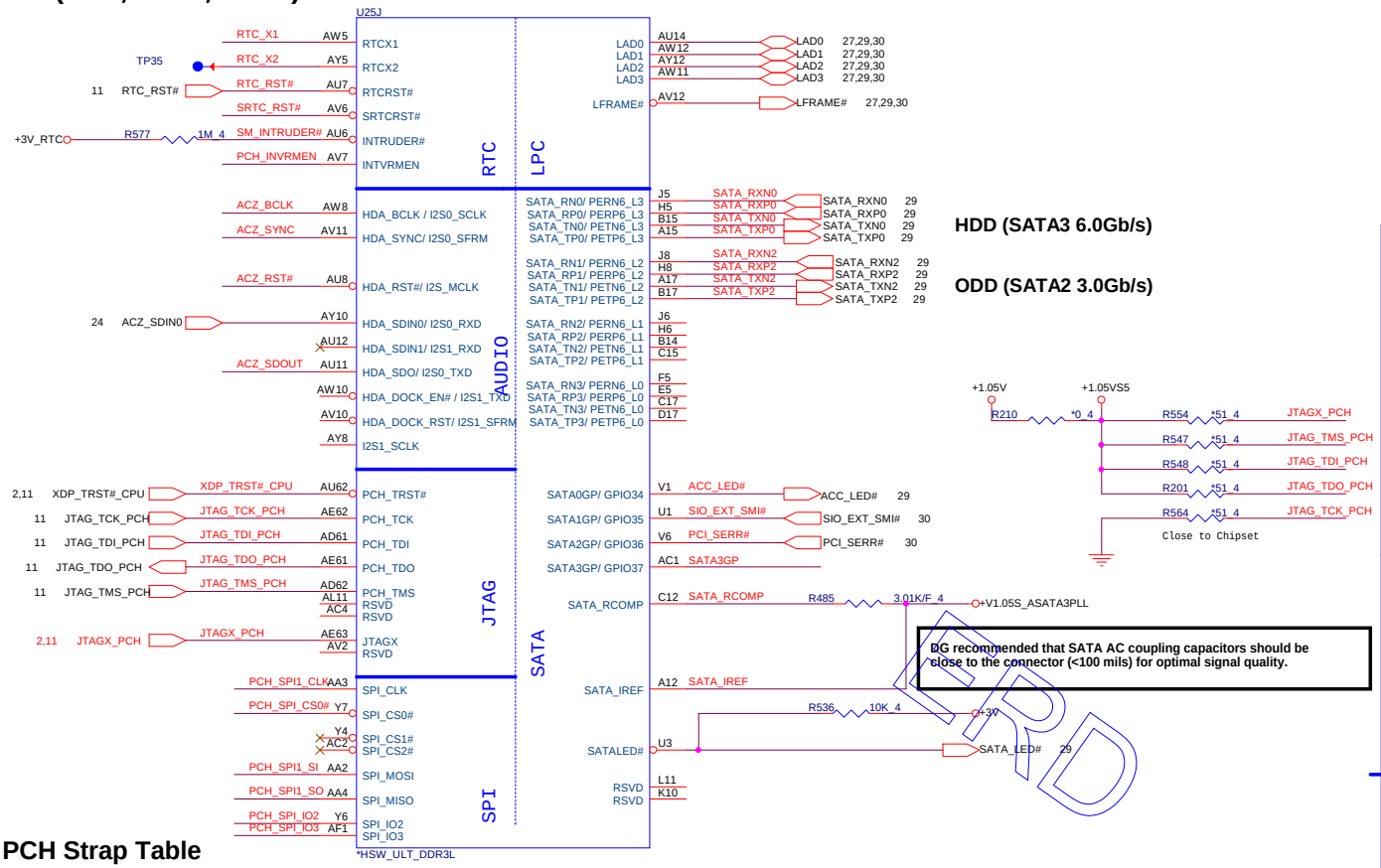
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)



HDD (SATA3 6.0Gb/s)

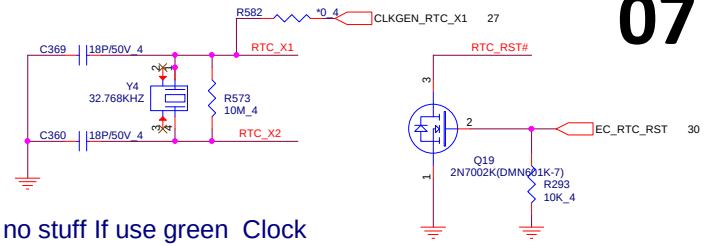
ODD (SATA2 3.0Gb/s)

DG recommended that SATA AC coupling capacitors should be close to the connector (<100 mils) for optimal signal quality.

PCH Strap Table

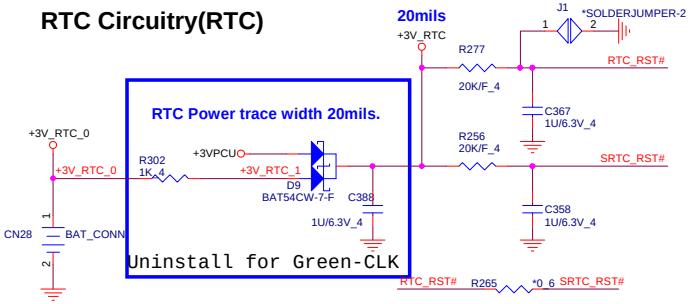
Pin Name	Strap description	Sampled	Configuration	Circuit
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	
SDIO_D0 /GPIO66	Top-Block Swap	PWROK	0 = "top-block swap" mode 1 = Default (weak pull-up 20K)	
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R575 330K_4 PCH_INVRMEN
HDA_SDO /I2S0_TXD	Flash Descriptor Security Only for Interposer	PWROK	0 = Default (weak pull-down 20K) 1 = Can be Overridden	30 GPIO33_EC R581 1K_4 ACZ_SDOUT
GSPI0_MOSI /GPIO86	Boot BIOS Selection	PWROK	GNT0# 1 = LPC; 0 = SPI(Default)	
GPIO15	TLS Confidentiality	PWROK	0 = ME Crypto Transport Layer Security cipher suite with no confidentiality(Default) 1 = Intel ME Crypto TLS cipher suite with confidentiality	
DSWVRMEN	Deep Sx Well On-Die Voltage Regulator Enable	ALWAYS	Should be always pull-up	+3V_RTC R576 330K_4 DSWVRMEN 6
				30 PCH_SPI_CS0#_R → PCH_SPI_CS0#_R 30 PCH_SPI1_CLK_R → PCH_SPI1_CLK_R 30 PCH_SPI1_SI_R → PCH_SPI1_SI_R 30 PCH_SPI1_SO_R → PCH_SPI1_SO_R

RTC Clock 32.768KHz

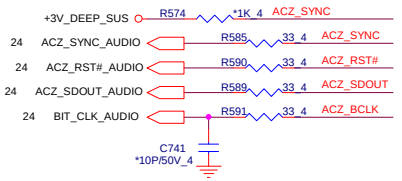


no stuff If use green Clock

RTC Circuitry(RTC)



HDA Bus(CLG)

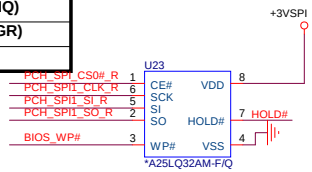


GPIO Pull UP

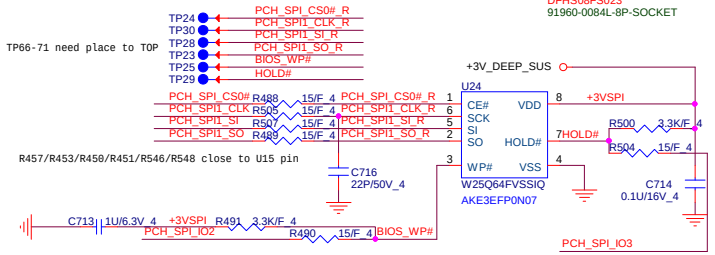
Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

4M SPI ROM Socket

U23&U24 footprint 要重疊



PCH SPI ROM(CLG)



+3V 6,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35,36
+5V 23,24,25,26,29,36

+1.05V 2,4,9,10,11,27,30,34,35,36
+3VS5 6,9,10,11,27,29,30,32,34,36
+3VPCU 4,25,26,27,29,30,31,32
+3V_RTC 10,27
+V1.05S_ASATA3PLL 10

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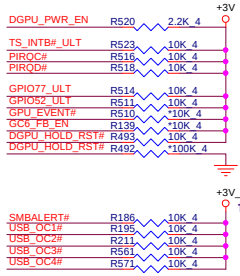
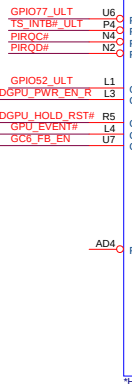
Lynx Point-LP Platform Controller Hub (HDA, JTAG, SATA)

08

PCI/USBOC# Pull-up(CLG)



USB3.0 M/B



15,37,39 DGPU_PWR_EN

14 DGPU_HOLD_RST#

PCI

USB

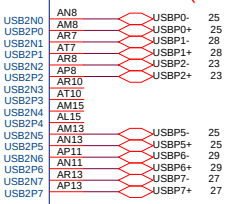
*HSW_ULT_DDR3L

U25N

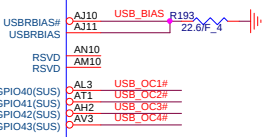
C - Link

CL_CLK AF2
CL_DATA AD2
CL_RST# AF4

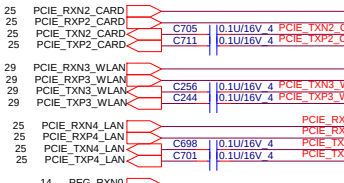
USB2.0(M/B-1) (USBP1)
USB2.0 Small board (USBP5)
USB2.0 Small board (USBP0)
Camera (USBP2)
WLAN (USBP6)
TS (USBP7)



TIE TRACES TOGETHER CLOSE TO PINS WITH LENGTH TO RESISTOR

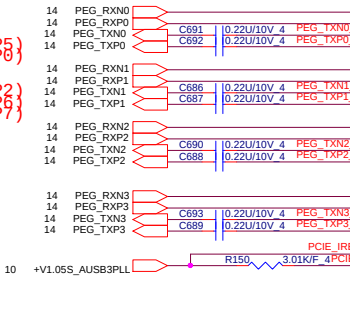


Cardreader

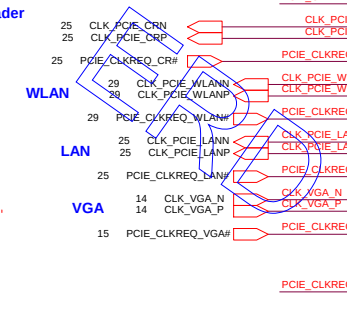


WLAN

LAN



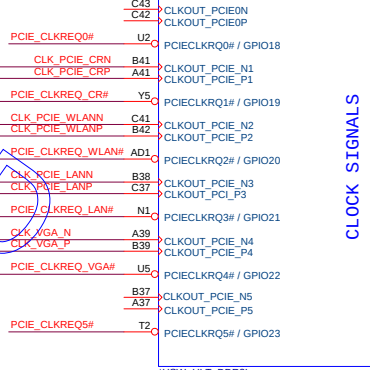
Cardreader

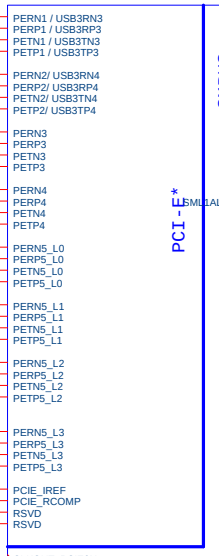


WLAN

LAN

VGA



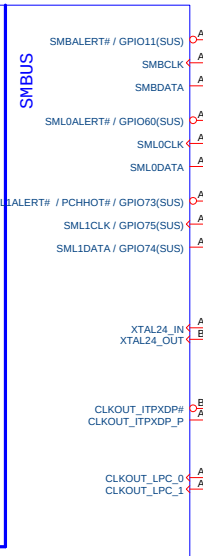


U25K

PCI-E*

*HSW_ULT_DDR3L

CLOCK SIGNALS

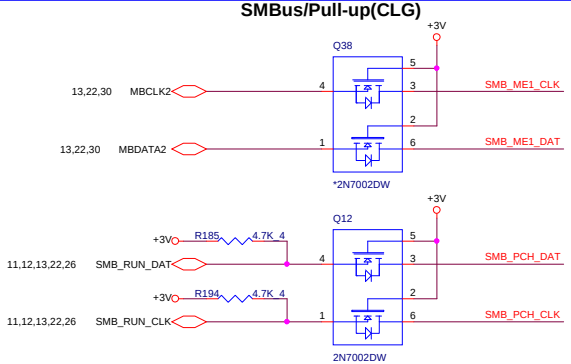


SMBUS

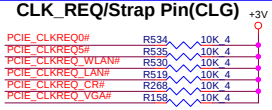
TP10

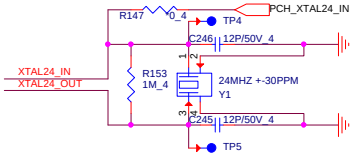
*0_4P2R_4
RP1
CK_XDP_N 11
CK_XDP_P 11
RP1 install for XDP
EC26 18P/50V_4
CLK_24M_KBC 30
CLK_24M_DEBUG 29
R242 22_4
R234 22_4
EMI(near PCH)
EC29 18P/50V_4
R243 22_4
CLK_PCI_TPM 27
EMI(near PCH)
EC27 *18P/50V_4
R149
+V1.05S_AXCK_LCPLL 10
3.01K/F_4
C35 R148 10K_4
C34 R152 10K_4
AK8 R239 10K_4
AL8 R245 10K_4

SMBus/Pull-up(CLG)



CLK_REQ/Strap Pin(CLG)

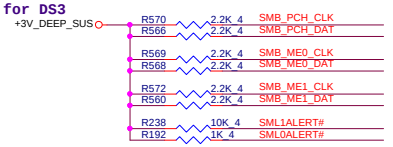




6,7,9,10,11,12,13,22,23,24,25,26,27,29,30,35,36 +3V

6,7,9,10,11 +V_DEEP_SUS

SMBus/Pull-up(CLG)



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Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA) Haswell (GPIO)

09

U25O

GPIO8(SUS)
GPIO9(SUS)
GPIO10(SUS)
LAN_PHY_PWR_CTRL / GPIO12(DSW)
GPIO13(SUS)
GPIO14(SUS)
GPIO15(SUS)
GPIO16
GPIO17
GPIO24 (SUS)
GPIO25(DSW)
GPIO26(SUS)
GPIO27(DSW)
GPIO28(SUS)
DEVSLP0/ GPIO33
DEVSLP1/ GPIO38
DEVSLP2/ GPIO39
GPIO44(SUS)
GPIO45(SUS)
GPIO46(SUS)
GPIO47(SUS)
GPIO48
GPIO49
GPIO50
GPIO56(SUS)
GPIO57(SUS)
GPIO58(SUS)
GPIO59(SUS)
SDIO_POWER_EN/ GPIO70
HSIOPC/ GPIO71
BMBUSY# / GPIO76
SPKR/ GPIO81

GPIO

THRMTRIP#
RCIN# GPIO82
SERIRQ
PCH_OPI_RCOMP
RSVD
RSVD

CPU/MISC

GSPI0_CS/ GPIO83
GSPI0_CLK/ GPIO84
GSPI0_MISO/ GPIO85
GSPI0_MOSI/ GPIO86
GSPI1_CS/ GPIO87
GSPI1_CLK/ GPIO88
GSPI1_MISO/ GPIO89
GSPI1_MOSI/ GPIO90
UART0_RXD/ GPIO91
UART0_TXD/ GPIO92
UART0_RTS/ GPIO93
UART0_CTS/ GPIO94
UART1_RXD/ GPIO0
UART1_TXD/ GPIO1
UART1_RST/ GPIO2
UART1_CTS/ GPIO3
I2C0_SDA/ GPIO4
I2C0_SCL/ GPIO5
I2C1_SDA/ GPIO6
I2C1_SCL/ GPIO7
SDIO_CLK/ GPIO64
SDIO_CMD/ GPIO65
SDIO_D0/ GPIO66
SDIO_D1/ GPIO67
SDIO_D2/ GPIO68
SDIO_D3/ GPIO69

SERIAL IO

*HSW_ULT_DDR3L

30 SIO_EXT_SCI# — SIO_EXT_SCI# AU2
29 BT_OFF — BT_OFF AM3
6,29 RF_OFF_PCH — R177 *0_4 RF_OFF_PCH_R AM2
LAN_DISABLE# AM7
GPIO13_ULT AT3
GPIO14_ULT AH4
AD6
29 ZERO_ODD_DP# — R553 *0_4 ODD_PRSNT#_R Y1
15,30,37,39 DGPU_PWROK T3
BOARD_ID6 AD5
GPIO25_ULT AM4
BOARD_ID7 AN3
GPIO27 AN5
BOARD_ID8 AD7
DEVSLP0 P2
TP11 DEVSLP1 L2
DEVSLP2 N5
GPIO44_ULT AK4
TP for DG
BOARD_ID4 AG5
GPIO46_ULT AG3
BOARD_ID5 AB6
TP12
BT_COMBO_EN# U4
27 ACCEL_INTA# — GPIO49_ULT Y3
GPIO50_ULT P3
BOARD_ID0 AG6
BOARD_ID1 AP1
BOARD_ID2 AL4
BOARD_ID3 AT5
GPIO70_ULT C4
36 MPHY_PWREN — MPHY_PWREN Y2
GPIO76_ULT P1
24 ACZ_SPKR — V2

D60 PCH_THRMTRIP# — PM_THRMTRIP# 30
V4 EC_RCIN# — EC_RCIN# 30
T4 SERIRQ — R529 10K_4 +3V — SERIRQ 27,30
AW15 PCH_OPI_RCOMP — R583 49.9/F_4
AF20
AB21

R6 GSPI0_CS
L6 GSPI0_CLK
N6 GSPI0_MISO
L8
R7 GSPI1_CS
L5 GSPI1_CLK
N7 GSPI1_MISO
K2 GSPI1_MOSI
J1 UART0_RXD
K3 UART0_TXD
J2 UART0_RTS
G1 UART0_CTS
K4 UART1_RXD
G2 UART1_TXD
J3 UART1_RST
J4 UART1_CTS
F2 I2C0_SDA
F3 I2C0_SCL
G4 I2C1_SDA
F1 I2C1_SCL
E3 SDIO_CLK
F4 SDIO_CMD
D3
E4 SDIO_D1
C3 SDIO_D2
E2 SDIO_D3

RP2
GSPI1_CLK 10 — 1 GSPI0_CS
I2C1_SDA 9 — 2 GSPI1_CS
GSPI0_MISO 8 — 3 GSPI1_MISO
SDIO_CMD 7 — 4 UART0_TXD
6 — 5
10K_10P8R_6 +3V

RP6
SDIO_D2 10 — 1 UART0_CTS
SDIO_D1 9 — 2 I2C0_SCL
SDIO_D3 8 — 3 I2C0_SDA
SDIO_CLK 7 — 4 I2C1_SCL
6 — 5
10K_10P8R_6 +3V

RP5
UART1_TXD 10 — 1 GSPI0_CLK
UART0_RTS 9 — 2 UART1_RXD
UART0_RXD 8 — 3 GSPI1_MOSI
UART1_RST 7 — 4 UART1_CTS
6 — 5
10K_10P8R_6 +3V

GPIO Pull-up/Pull-down(CLG)

+3V_DEEP_SUS

SIO_EXT_SCI# R282 10K_4
BT_OFF R180 10K_4
RF_OFF_PCH_R R172 10K_4
GPIO13_ULT R218 10K_4
GPIO14_ULT R183 10K_4
GPIO44_ULT R565 10K_4
GPIO46_ULT R541 10K_4

+3V

GPIO49_ULT R552 10K_4
GPIO50_ULT R524 10K_4
ODD_PRSNT#_R R546 10K_4
DGPU_PWROK R513 10K_4
DEVSLP0 R515 10K_4
DEVSLP2 R499 10K_4
BT_COMBO_EN# R512 *10K_4
GPIO70_ULT R486 10K_4
EC_RCIN# R269 10K_4
GPIO76_ULT R525 10K_4
MPHY_PWREN R544 100K_4
MPHY_PWREN R545 *10K_4

+3VS5

GPIO12 LAN_DISABLE# SUS -->Check list +3V -->Datasheet
GPIO25_ULT R173 10K_4
LAN_DISABLE# R169 10K_4
GPIO27 R626 10K_4

Close to EC

+V1.05S_VCCST
PM_THRMTRIP# R184 1K_4

Model	BOARD_ID[8:7]	BOARD_ID[6:5]	Board ID [4:3]	BOARD_ID[2:1]	BOARD_ID0
Definition	Reserve (Default = 00)	Reserve (Default = 00)	00 Single Rank (X12) 01 Dual Rank (X12) 10 Meso-AMD (X11) 11 Reserve	00 14" 01 15" 10 17"	0 : UMA 1 : DIS

R174 *10K_4 BOARD_ID0 R539 10K_4 +3V_DEEP_SUS
R205 10K_4 BOARD_ID1 R199 *10K_4
R558 10K_4 BOARD_ID2 R559 *10K_4
R248 10K_4 BOARD_ID3 R255 *10K_4
R175 *10K_4 BOARD_ID4 R540 10K_4
R167 10K_4 BOARD_ID5 R549 *10K_4
R161 10K_4 BOARD_ID6 R164 *10K_4
R204 10K_4 BOARD_ID7 R198 *10K_4
R160 10K_4 BOARD_ID8 R163 *10K_4

6,7,8,10,11,12,13,22,23,24,25,26,27,29,30,35,36 +3V
6,10,11,27,29,30,32,34,36,37,39 +3VS5

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	ULT 8/9 (GPIO/MISC)	1A
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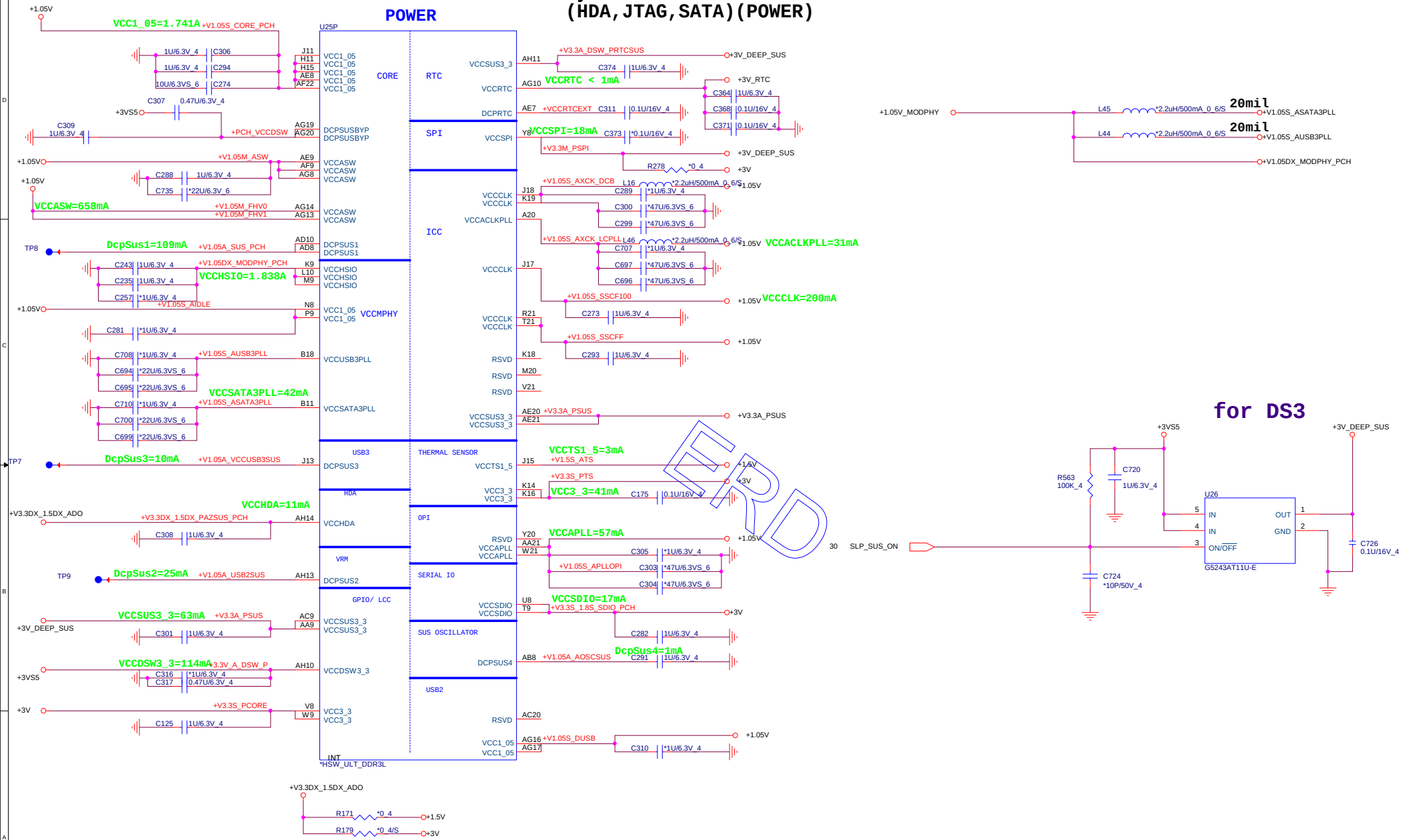
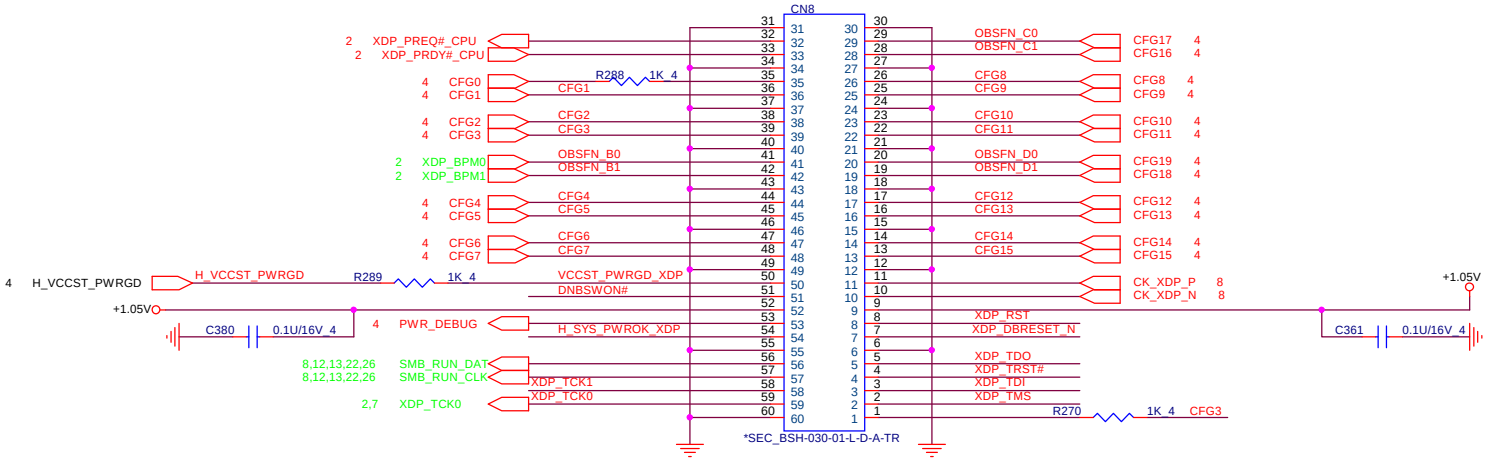
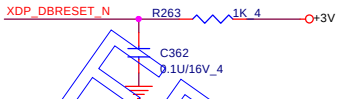
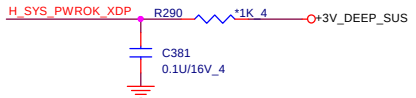
Lynx Point-LP Platform Controller Hub (HDA,JTAG,SATA)(POWER)

POWER

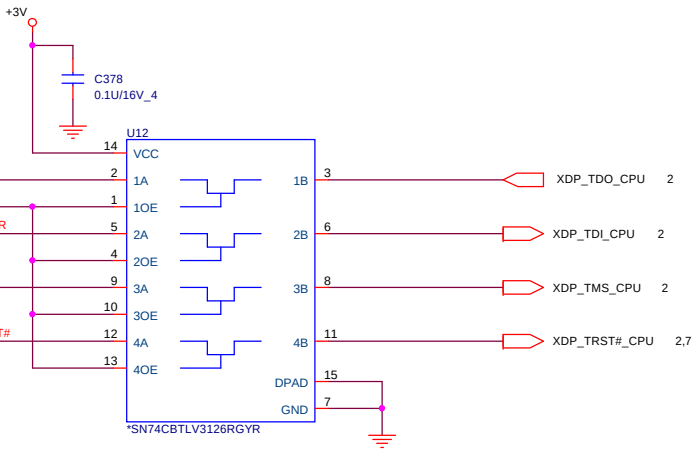




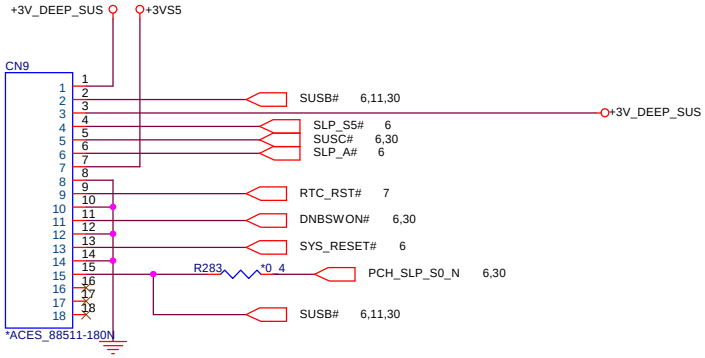


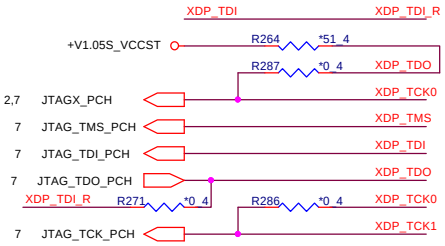


ERD



APS





PROJECT : X11

Quanta Computer Inc.

ULT

Size	Document Number	Rev
	HSW XDP & APS	1A

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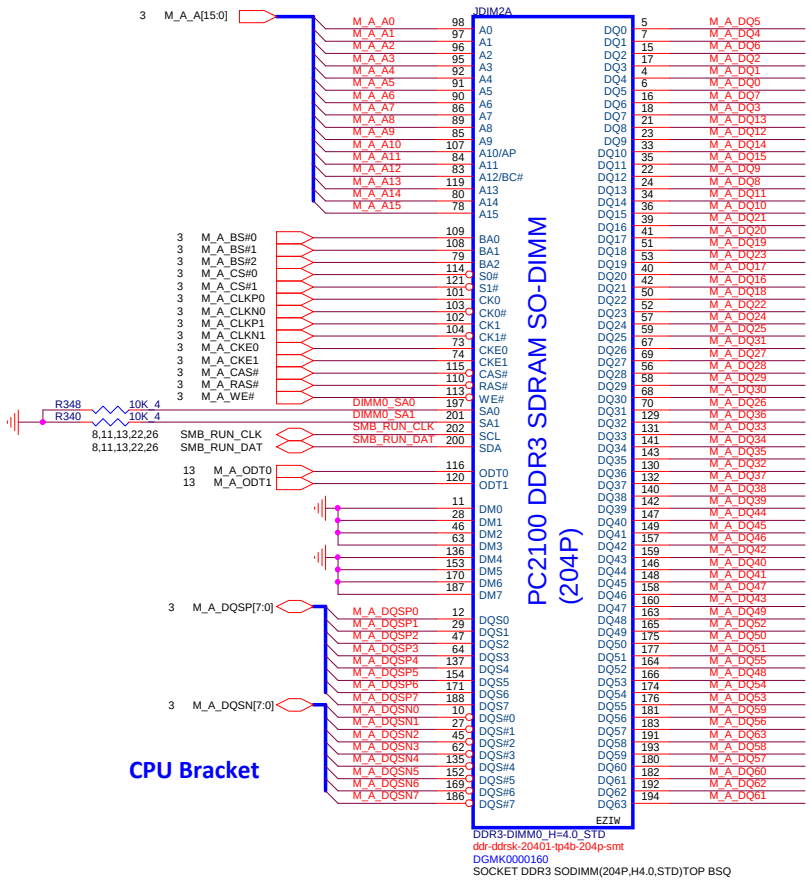
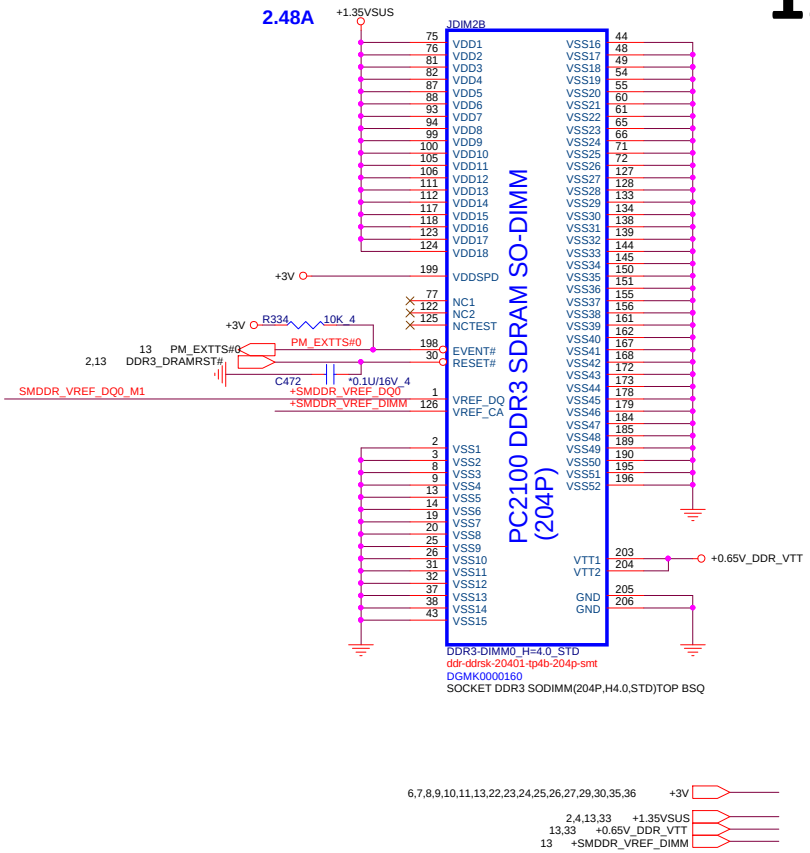
DIMM & Footprint 同Joshua提供



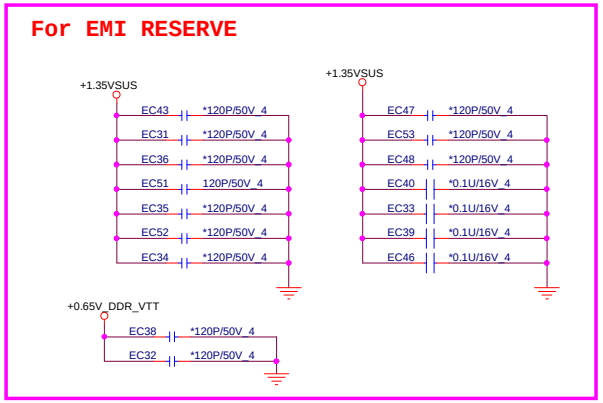
CPU Bracket

ERD

2.48A

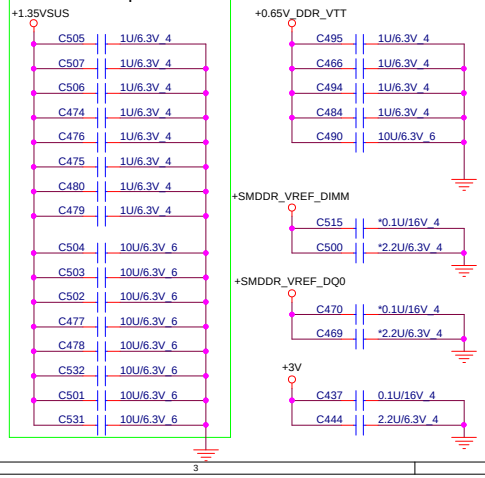


For EMI RESERVE

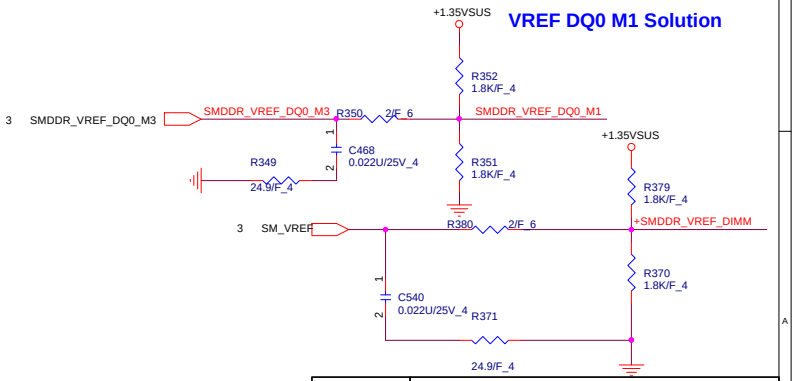


Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector



VREF DQ0 M1 Solution

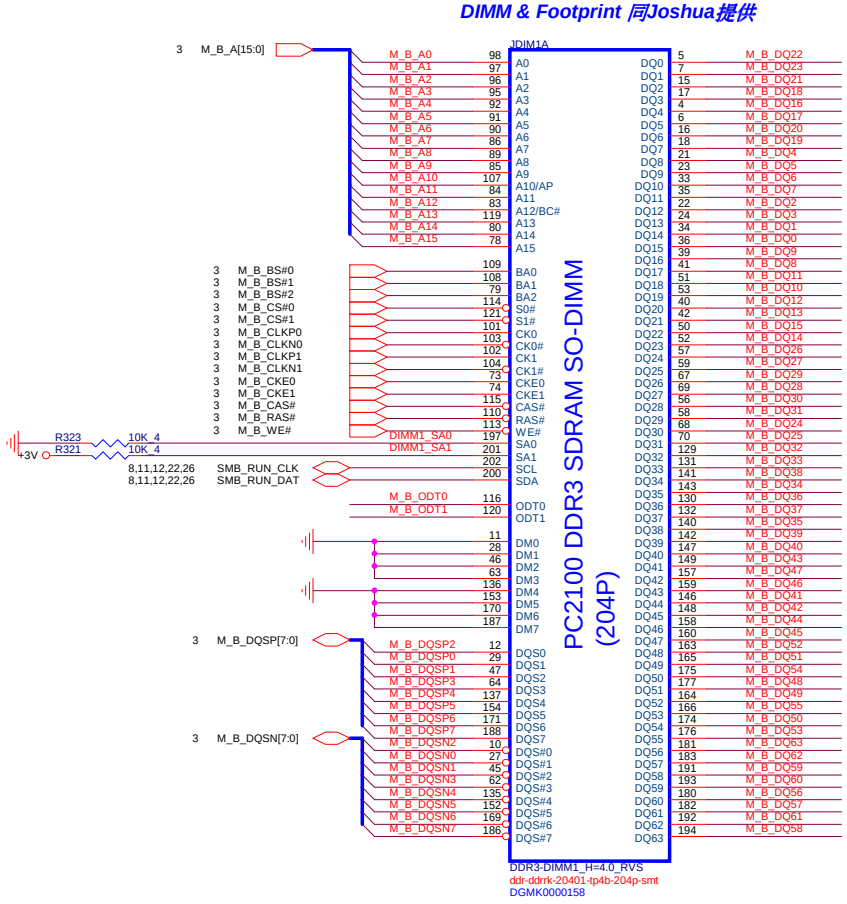


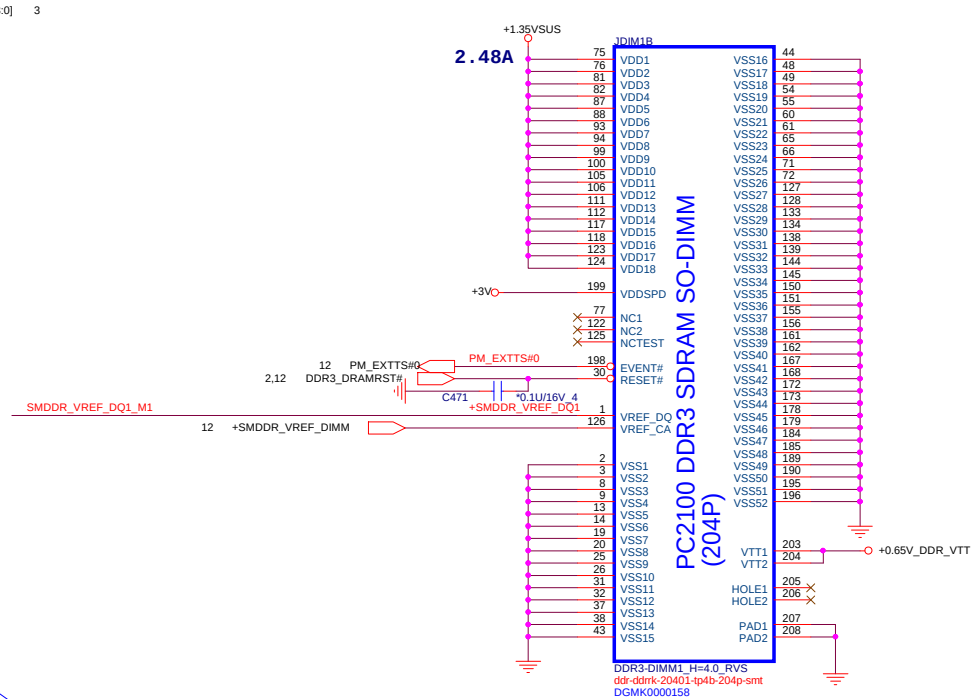
PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	DDR3 DIMM0-STD(4.0H)	1A
Date: Monday, January 05, 2015	Sheet 12of 40	

DIMM & Footprint 同Joshua提供

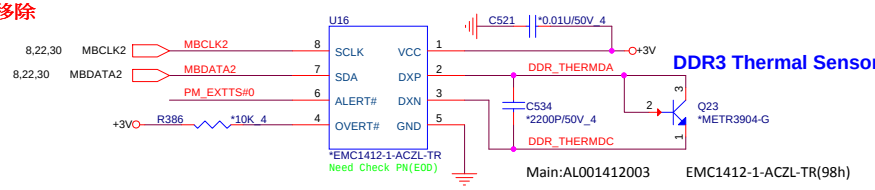




ERD

Local Thermal Sensor

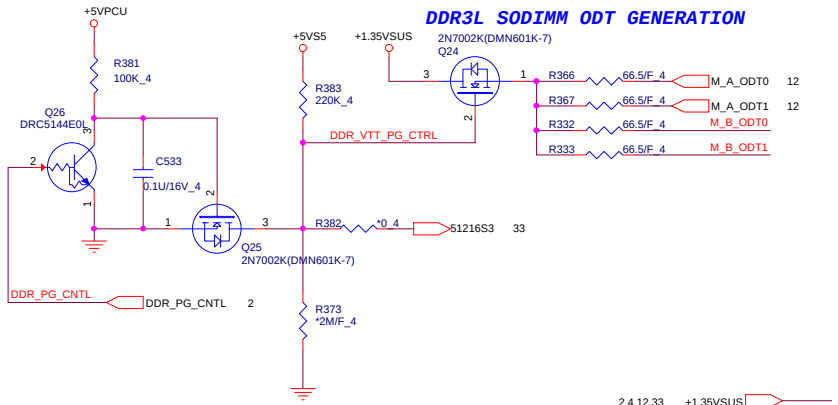
MV可移除



Main:AL001412003 EMC1412-1-ACZL-TR(98h)

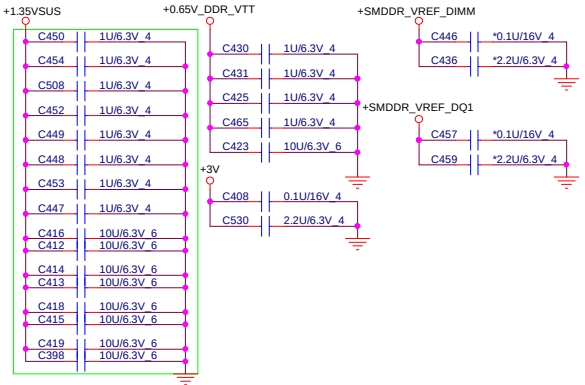
2nd:AL000431014 TMP431ADGKR(98h)

DDR3L SODIMM ODT GENERATION

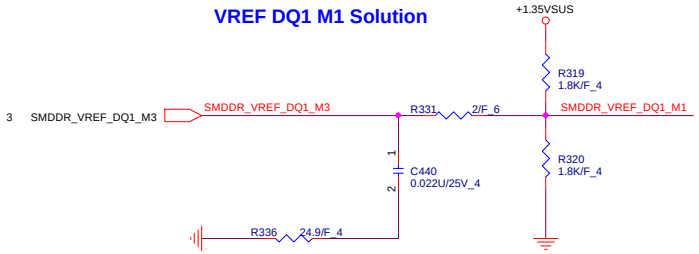


Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector



VREF DQ1 M1 Solution



PROJECT : X11	
Quanta Computer Inc.	
Size: Custom	Document Number: DDR3 DIMM1-RVS(4.0H)
Rev: 1A	
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Platform	Type HP	P/N
Carrizo$_{hp}$	Gen 3	CH4222K9B04 RD
Carrizo-L	Gen 1/Gen 2	CH4102K1B03

9/2: CZ use 0.22u(Gen 3) ; CZ-L use 0.1u(Gen 2)

U4000A

PCI EXPRESS INTERFACE

8	PEG_TXP0	PEG_TXP0	AF30	PCIE_RX0P	PCIE_TX0P	AH30	PEG_RXP0_C	C4000	0.22U/10V_4	PEG_RXP0 8
8	PEG_TXN0	PEG_TXN0	AE31	PCIE_RX0N	PCIE_TX0N	AG31	PEG_RXN0_C	C4001	0.22U/10V_4	PEG_RXN0 8
8	PEG_TXP1	PEG_TXP1	AE29	PCIE_RX1P	PCIE_TX1P	AG29	PEG_RXP1_C	C4002	0.22U/10V_4	PEG_RXP1 8
8	PEG_TXN1	PEG_TXN1	AD28	PCIE_RX1N	PCIE_TX1N	AF28	PEG_RXN1_C	C4003	0.22U/10V_4	PEG_RXN1 8
8	PEG_TXP2	PEG_TXP2	AD30	PCIE_RX2P	PCIE_TX2P	AF27	PEG_RXP2_C	C4004	0.22U/10V_4	PEG_RXP2 8
8	PEG_TXN2	PEG_TXN2	AC31	PCIE_RX2N	PCIE_TX2N	AF26	PEG_RXN2_C	C4005	0.22U/10V_4	PEG_RXN2 8
8	PEG_TXP3	PEG_TXP3	AC29	PCIE_RX3P	PCIE_TX3P	AD27	PEG_RXP3_C	C4006	0.22U/10V_4	PEG_RXP3 8
8	PEG_TXN3	PEG_TXN3	AB28	PCIE_RX3N	PCIE_TX3N	AD26	PEG_RXN3_C	C4007	0.22U/10V_4	PEG_RXN3 8

		AB30	PCIE_RX4P	PCIE_TX4P	AC25	
		AA31	PCIE_RX4N	PCIE_TX4N	AB25	
		AA29	PCIE_RX5P	PCIE_TX5P	Y23	
		Y28	PCIE_RX5N	PCIE_TX5N	Y24	
		Y30	PCIE_RX6P	PCIE_TX6P	AB27	
		W31	PCIE_RX6N	PCIE_TX6N	AB26	
		W29	PCIE_RX7P	PCIE_TX7P	Y27	
		V28	PCIE_RX7N	PCIE_TX7N	Y26	
		V30	NC#V30	NC#W24	W24	
		U31	NC#U31	NC#W23	W23	
		U29	NC#U29	NC#V27	V27	
		T28	NC#T28	NC#U26	U26	
		T30	NC#T30	NC#U24	U24	
		R31	NC#R31	NC#U23	U23	
		R29	NC#R29	NC#T26	T26	
		P28	NC#P28	NC#T27	T27	
		P30	NC#P30	NC#T24	T24	
		N31	NC#N31	NC#T23	T23	
		N29	NC#N29	NC#P27	P27	
		M28	NC#M28	NC#P26	P26	
		M30	NC#M30	NC#P24	P24	
		L31	NC#L31	NC#P23	P23	
		L29	NC#L29	NC#M27	M27	
		K30	NC#K30	NC#N26	N26	

CLOCK

8	CLK_VGA_P	CLK_VGA_P	AK30	PCIE_REFCLKP
8	CLK_VGA_N	CLK_VGA_N	AK32	PCIE_REFCLKN

CALIBRATION

				PCIE_CALR_TX	Y22	SUN_PCIE_CALRP
				PCIE_CALR_RX	AA22	SUN_PCIE_CALRN

R4000 1.69K/F_4 +1.0V_VGA

R4002 1K/F_4

R4001	1K_4	TEST_PG	N10	TEST_PG	
		PEGX_RST#	AL27	PERSTB	

Meso_S3

ERD

U4000G

DP POWER		NC/DP POWER	
AG15	NC_DP_VDDR#1	NC#AE11	AE11
AG16	NC_DP_VDDR#2	NC#AF11	AF11
AF16	NC_DP_VDDR#3	NC#AE13	AE13
AG17	NC_DP_VDDR#4	NC#AF13	AF13
AG18	NC_DP_VDDR#5	NC#AG8	AG8
AG19	NC_DP_VDDR#6	NC#AG10	AG10
AF14	DP_VDDR		
AG20	NC_DP_VDDC#1	NC#AF6	AF6
AG21	NC_DP_VDDC#2	NC#AF7	AF7
AF22	NC_DP_VDDC#3	NC#AF8	AF8
AG22	NC_DP_VDDC#4	NC#AF9	AF9
AD14	DP_VDDC		
AG14	NC_DP_VSSR#1	NC#AE1	AE1
AH14	NC_DP_VSSR#2	NC#AE3	AE3
AM14	NC_DP_VSSR#3	NC#AG1	AG1
AM16	NC_DP_VSSR#4	NC#AG6	AG6
AM18	NC_DP_VSSR#5	NC#AH5	AH5
AF23	NC_DP_VSSR#6	NC#AF10	AF10
AG23	NC_DP_VSSR#7	NC#AG9	AG9
AM20	NC_DP_VSSR#8	NC#AH8	AH8
AM22	NC_DP_VSSR#9	NC#AM6	AM6
AM24	NC_DP_VSSR#10	NC#AM8	AM8
AF19	NC_DP_VSSR#11	NC#AG7	AG7
AF20	NC_DP_VSSR#12	NC#AG11	AG11
AE14	DP_VSSR		
AF17	NC_UPHYAB_DP_CALR	NC#AE10	AE10

Meso_S3

1.8V (40mA)

+1.8V_VGA C4008 10U/6.3VS_6 C4009 1U/10V_4

1.0V (32mA)

+1.0V_VGA C4014 *10U/6.3VS_6 C4015 1U/10V_4 C4016 0.1U/16V_4

12/10:reserve for verify

+3V_VGA R4003 1K/F_4

PLTRST# 2 3 PEGX_RST#

DGPU_HIN_RST# 1 D4000 BAT54AW-L

+3V_VGA C4021 *0.1U/16V_4

C4022 *0.1U/16V_4

U4001 *MC74VHC1G08DFT2G

6,11,25,27,29,30 PLTRST# 2

8 DGPU_HOLD_RST# R4004 *0_4/S DGPU_HIN_RST# 1

4 PEGX_RST# PEGX_RST# 15

R4005 100K/F_4

15,17,39 +3V_VGA

15,17,27,37,39 +1.8V_VGA

17,39 +1.0V_VGA

L

PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ S3 PCIE/DP power	1A

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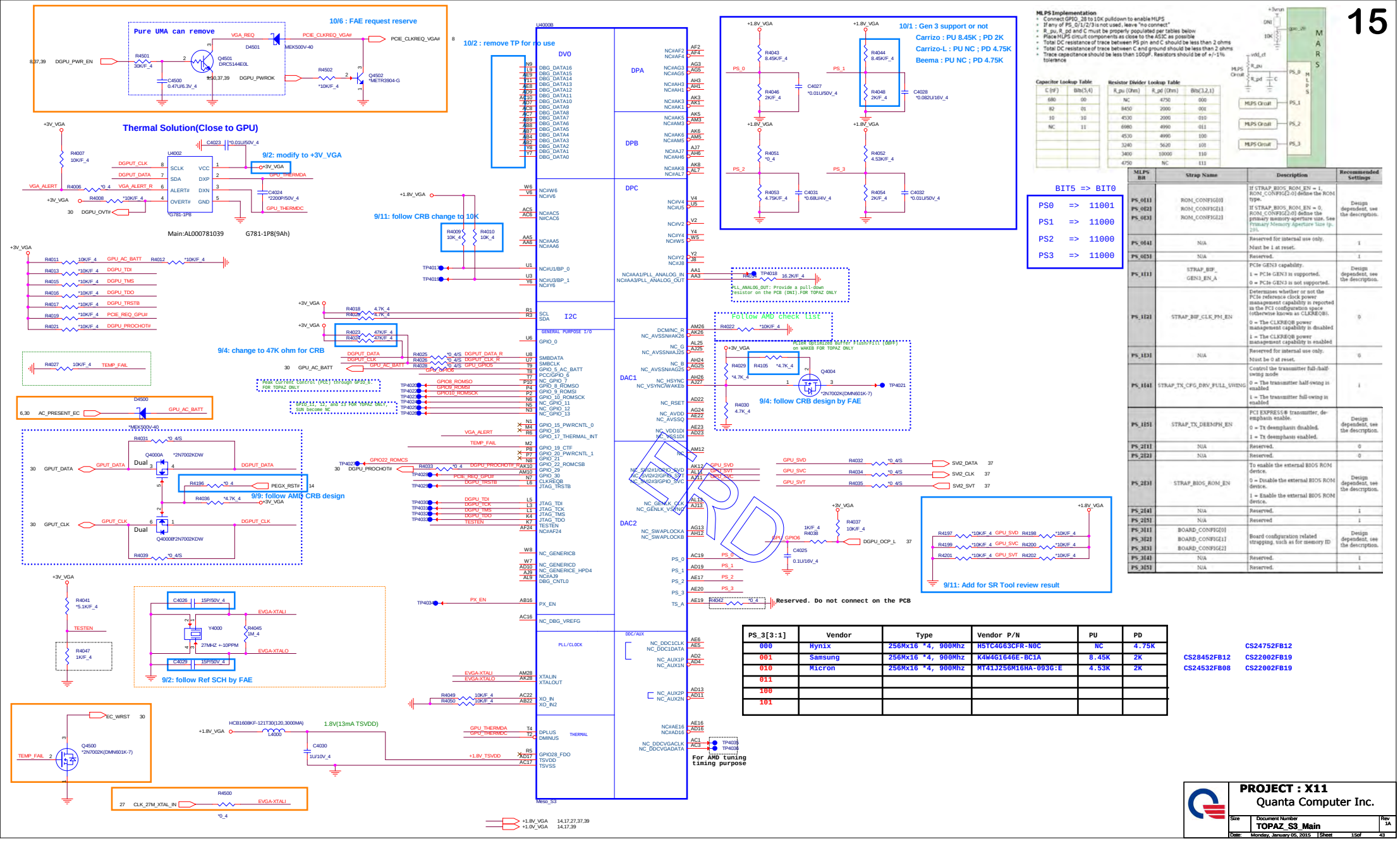
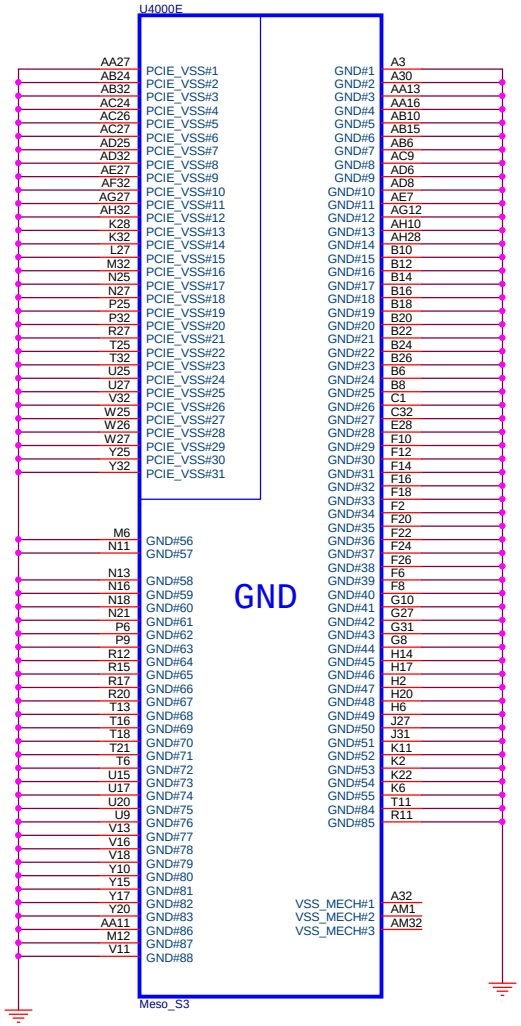
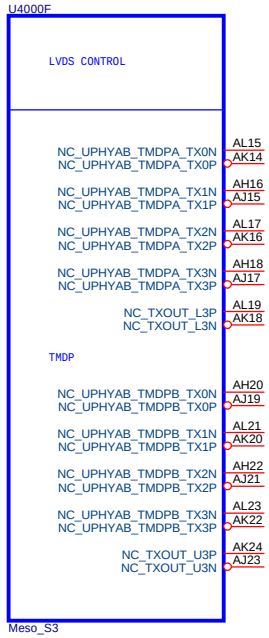


MLPS Bit	Strap Name	Description	Recommended Settings
PS_0[1]	ROM_CONFIG[0] ROM_CONFIG[1] ROM_CONFIG[2]	If STRAP_BIOS_ROM_EN = 1, ROM_CONFIG[2:0] define the ROM type. If STRAP_BIOS_ROM_EN = 0, ROM_CONFIG[2:0] define the primary memory-aperture size. See Primary Memory Aperture Size (p. 29).	Design dependent, see the description.
PS_0[4]	N/A	Reserved for internal use only. Must be 1 at reset.	1
PS_0[5]	N/A	Reserved.	1
PS_1[1]	STRAP_BIF_ GEN3_EN_A	PCIe GEN3 capability. 1 = PCIe GEN3 is supported. 0 = PCIe GEN3 is not supported.	Design dependent, see the description.
PS_1[2]	STRAP_BIF_CLK_PM_EN	Determines whether or not the PCIe reference clock power management capability is reported in the PCI configuration space (otherwise known as CLKREQB). 0 = The CLKREQB power management capability is disabled 1 = The CLKREQB power management capability is enabled	0
PS_1[3]	N/A	Reserved for internal use only. Must be 0 at reset.	0
PS_1[4]	STRAP_TX_CFG_DRV_FULL_SWING	Control the transmitter full-/half-swing mode 0 = The transmitter half-swing is enabled 1 = The transmitter full-swing is enabled	1
PS_1[5]	STRAP_TX_DEEMPH_EN	PCI EXPRESS® transmitter, de-emphasis enable. 0 = Tx deemphasis disabled. 1 = Tx deemphasis enabled.	Design dependent, see the description.
PS_2[1]	N/A	Reserved.	0
PS_2[2]	N/A	Reserved.	0
PS_2[3]	STRAP_BIOS_ROM_EN	To enable the external BIOS ROM device. 0 = Disable the external BIOS ROM device. 1 = Enable the external BIOS ROM device.	Design dependent, see the description.
PS_2[4]	N/A	Reserved.	1
PS_2[5]	N/A	Reserved	1
PS_3[1]	BOARD_CONFIG[0]	Board configuration related strapping, such as for memory ID	Design dependent, see the description.
PS_3[2]	BOARD_CONFIG[1]		
PS_3[3]	BOARD_CONFIG[2]		
PS_3[4]	N/A	Reserved.	1
PS_3[5]	N/A	Reserved.	1

PS_3[3:1]	Vendor	Type	Vendor P/N	PU	PD		
000	Hynix	256Mx16 *4, 900Mhz	H5TC4G63CFR-N0C	NC	4.75K		CS24752FB12
001	Samsung	256Mx16 *4, 900Mhz	K4W4G1646E-BC1A	8.45K	2K	CS28452FB12	CS22002FB19
010	Micron	256Mx16 *4, 900Mhz	MT41J256M16HA-093G:E	4.53K	2K	CS24532FB08	CS22002FB19
011							
100							
101							

PROJECT : X11
Quanta Computer Inc.
Size | Document Number: TOPAZ_S3_Main | Rev: 1A
Date: Monday, January 05, 2015 | Sheet 150f 43





CONFIGURATION STRAPS-- SEE EACH DATABOOK FOR STRAP DETAILS

ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET

RECOMMENDED SETTINGS
0= DO NOT INSTALL RESISTOR
1 = INSTALL 3K RESISTOR
X = DESIGN DEPENDANT
NA = NOT APPLICABLE

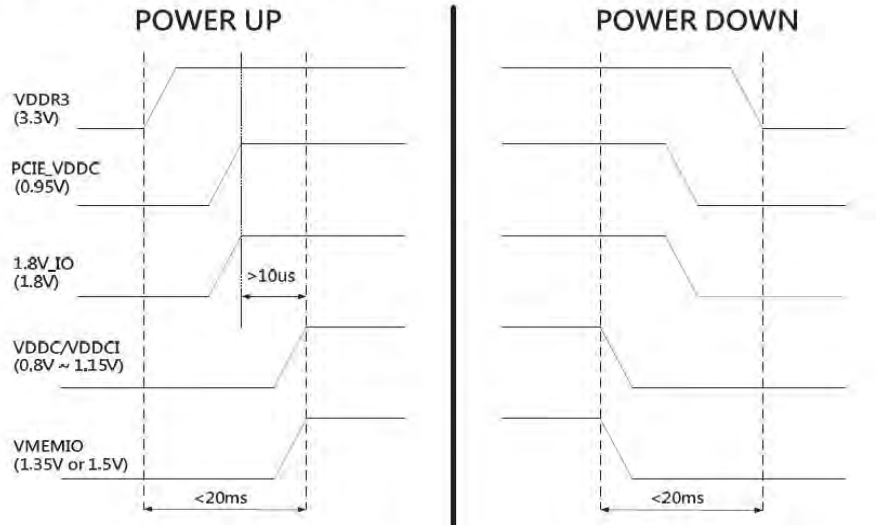
STRAPS	PIN	DESCRIPTION OF DEFAULT SETTINGS	
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLED	X
RSVD	GPIO2	RESERVED	0
RSVD	GPIO8	RESERVED	0
BIF_VGA DIS	GPIO9	VGA ENABLED	0
RSVD	GPIO21	RESERVED	0
BIOS_ROM_EN	GPIO_22_ROMCSB	ENABLE EXTERNAL BIOS ROM	0
ROMIDCFG(2:0)	GPIO[13:11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 0 1
VIP_DEVICE_STRAP_ENA	V2SYNC	IGNORE VIP DEVICE STRAPS (Removed on Seymour/Whistler)	0
RSVD	H2SYNC	RESERVED	0
AUD[1]	HSYNC	SEE DATABOOK FOR DETAIL	0
AUD[0]	VSYNC	SEE DATABOOK FOR DETAIL	0
RSVD	GENERICC	RESERVED	0

NOTE1: AMD RESERVED CONFIGURATION STRAPS

ALLOW FOR PULLUP PADS FOR THESE STRAPS BUT DO NOT INSTALL RESISTOR. IF THESE GPIOS ARE USED, THEY MUST KEEP "LOW" AND NOT CONFLICT DURING RESET.

GPIO21 H2SYNC GENERICC GPIO8 GPIO2

POWER UP / POWER DOWN SEQUENCE



PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
	TOPAZ_S3_GND/LVDS/Strap	1A

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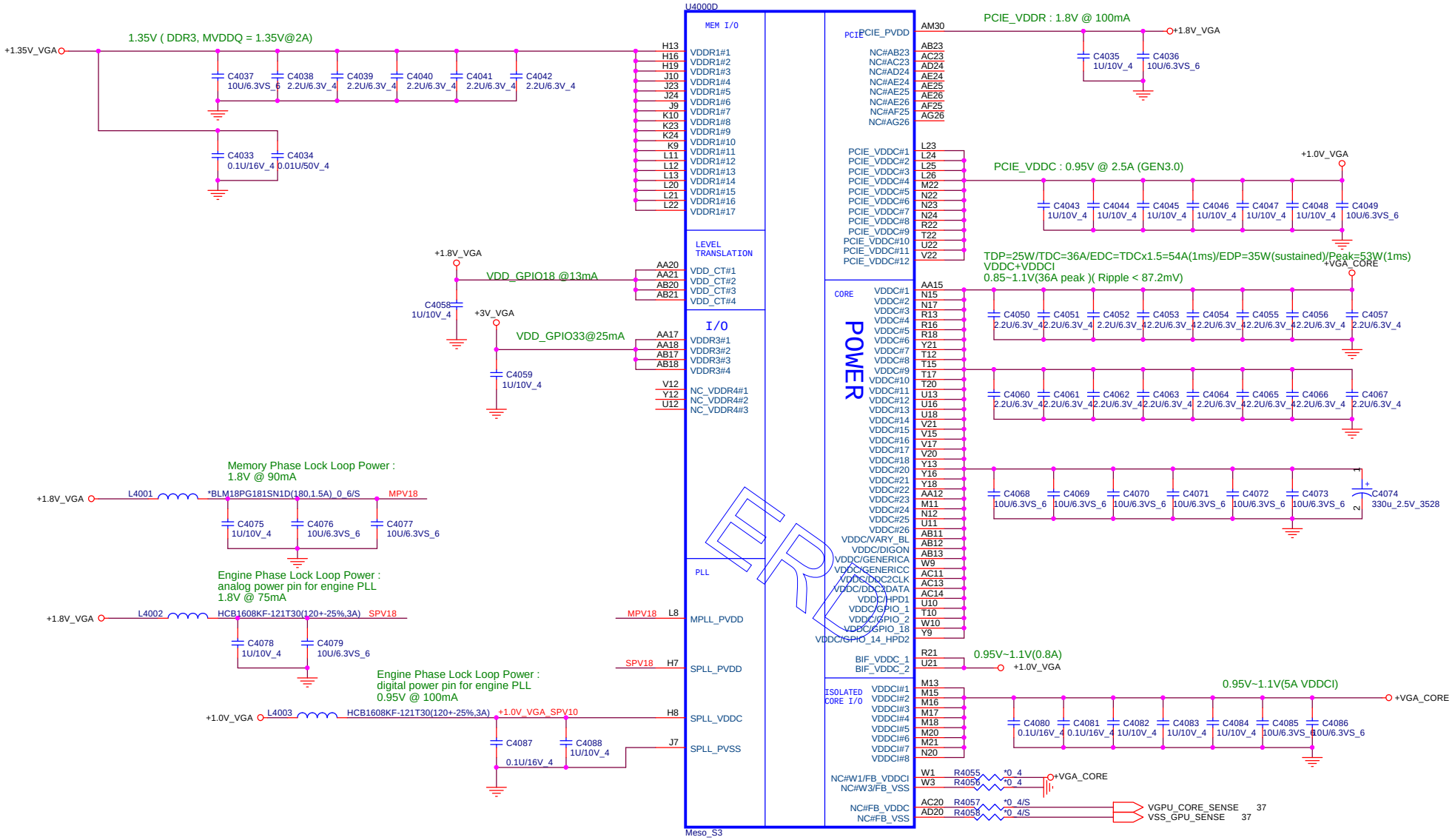
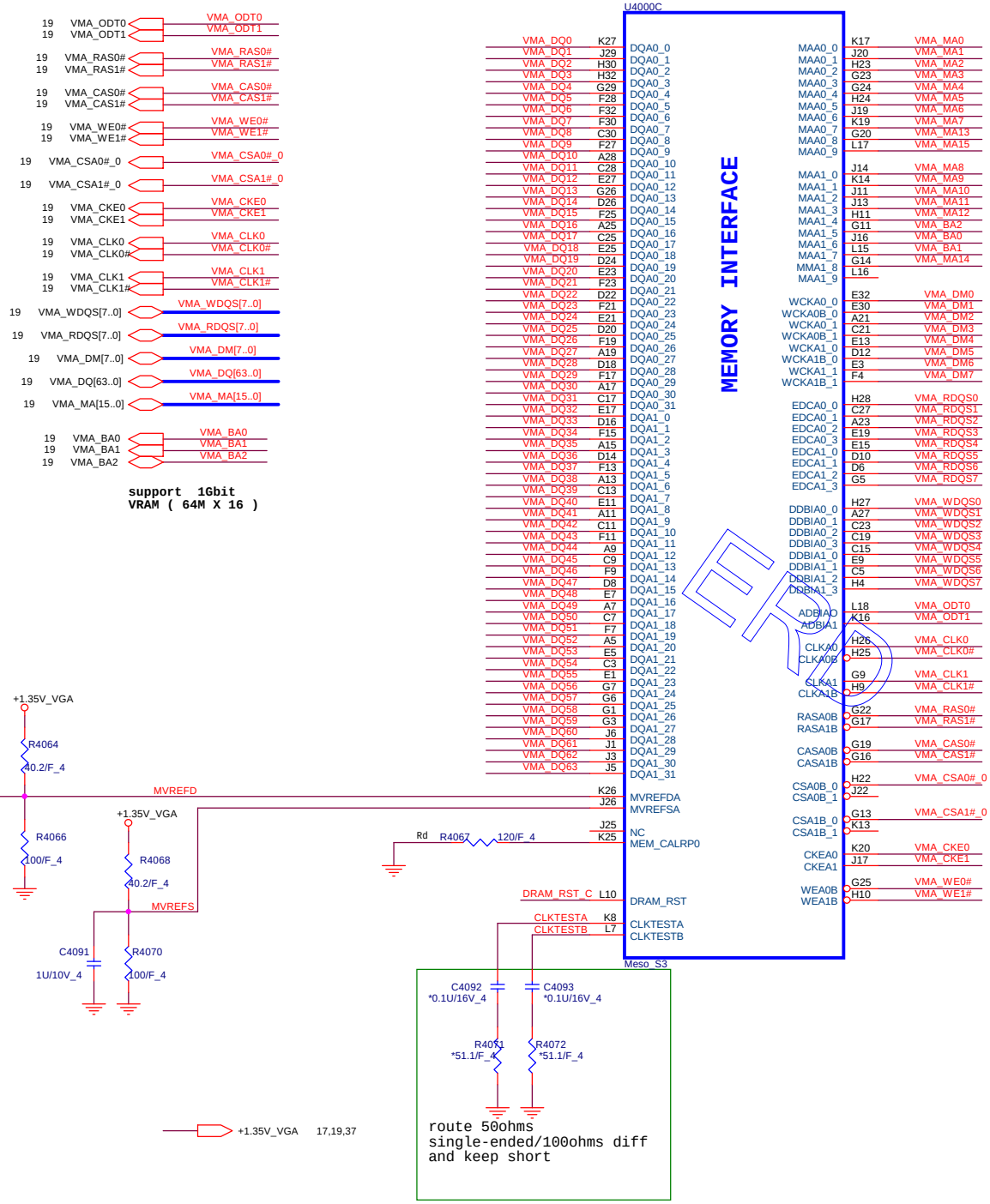
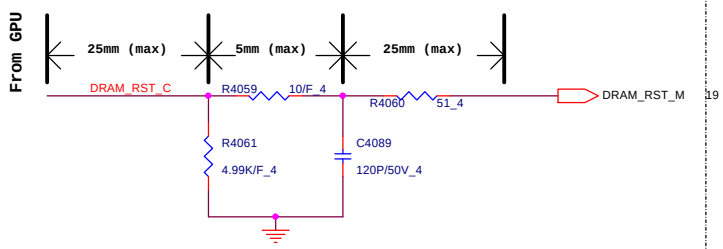


+1.35V_VGA 18,19,37
+1.8V_VGA 14,15,27,37,39
+1.0V_VGA 14,39
+VGA_CORE 37,38

PROJECT : X11		
Quanta Computer Inc.		
Size	Document Number: TOPAZ S3 Power	Rev: 1A
Date: Monday, January 05, 2015	Sheet 17 of 43	





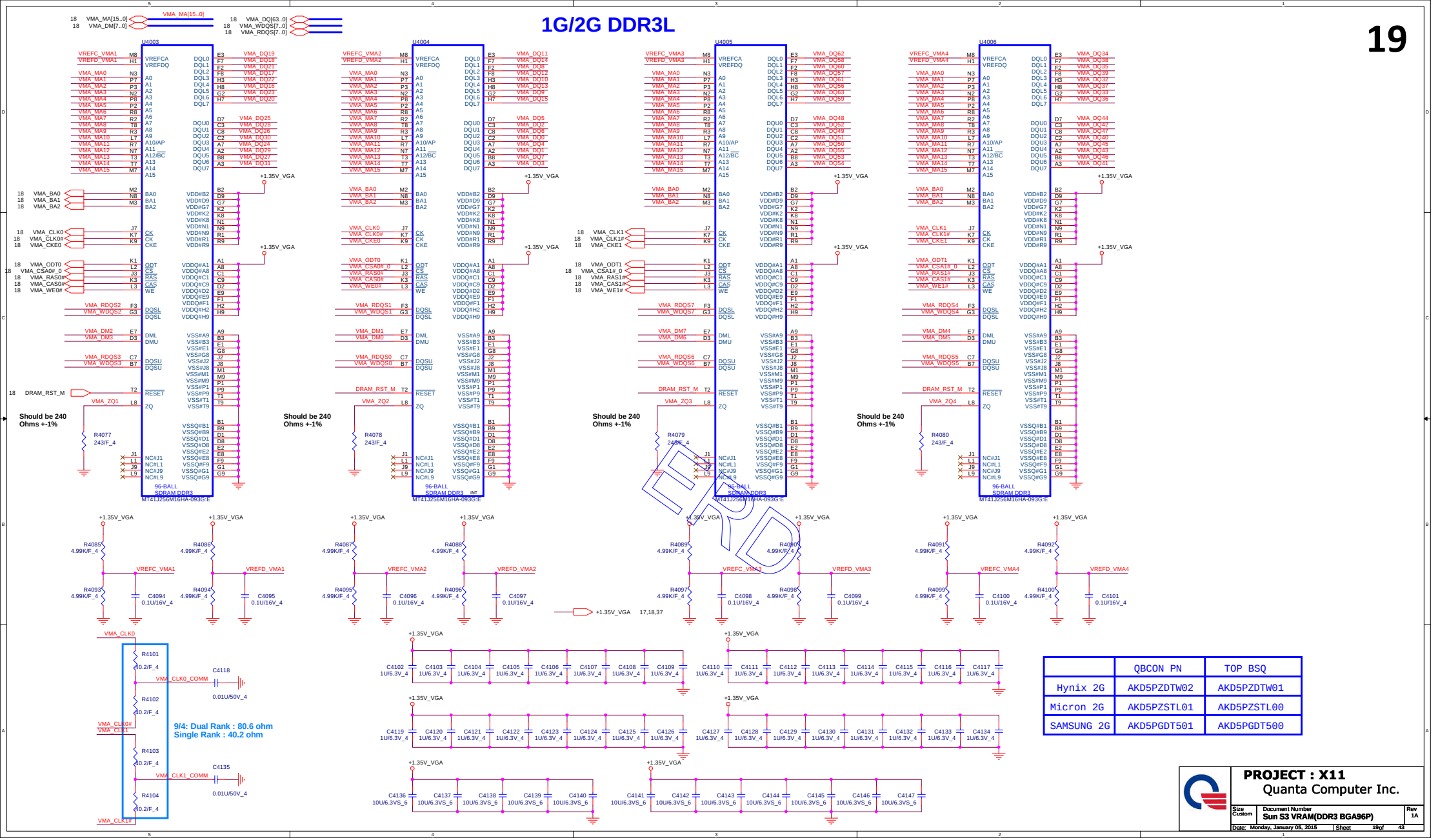
Place all these components very close to GPU (Within 25mm) and keep all component close to each Other (within 5mm) except Rser2

This basic topology should be used for DRAM_RST for DDR3/GDDR5.These Capacitors and Resistor values are an example only. The Series R and || Cap values will depend on the DRAM load and will have to be calculated for different Memory ,DRAM Load and board to pass Reset Signal Spec.

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
	TPOAZ_S3_MEM_Interface	1A
Date: Monday, January 05, 2015	Sheet 18 of 43	

1G/2G DDR3L



	QBCON PN	TOP BSQ
Hynix 2G	AKD5PZDTW02	AKD5PZDTW01
Micron 2G	AKD5PZSTL01	AKD5PZSTL00
SAMSUNG 2G	AKD5PGDT501	AKD5PGDT500

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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ERD

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

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ERD

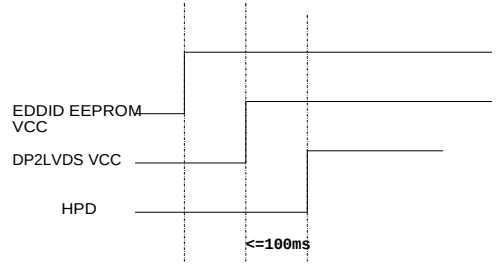
PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	Sun S3 VRAM(DDR3 BGA96P)	1A

Date: Monday, January 05, 2015 | Sheet 21 of 43

RTD2136 Dual Channel only

RTD2136S Power Up Sequence 22



Reserve for co layout EDP CON, EDP only please stuff

Pin 18: keep 80mil Trace

RTD2136R

IC底部需接GND

Reserve

Default(LVDS Only)

For eDP, close to U3

Use 1% Res on R32

LVDS Only

keep 80 mil

USING 60R 2A

CLOSE TO Pin22

Close to Pin18

USING 60R 1A

Close to Pin5

L10: need use CV-4709MN00 for Vendor suggestion

Close to Pin17

Close to Pin11

Close to Pin43

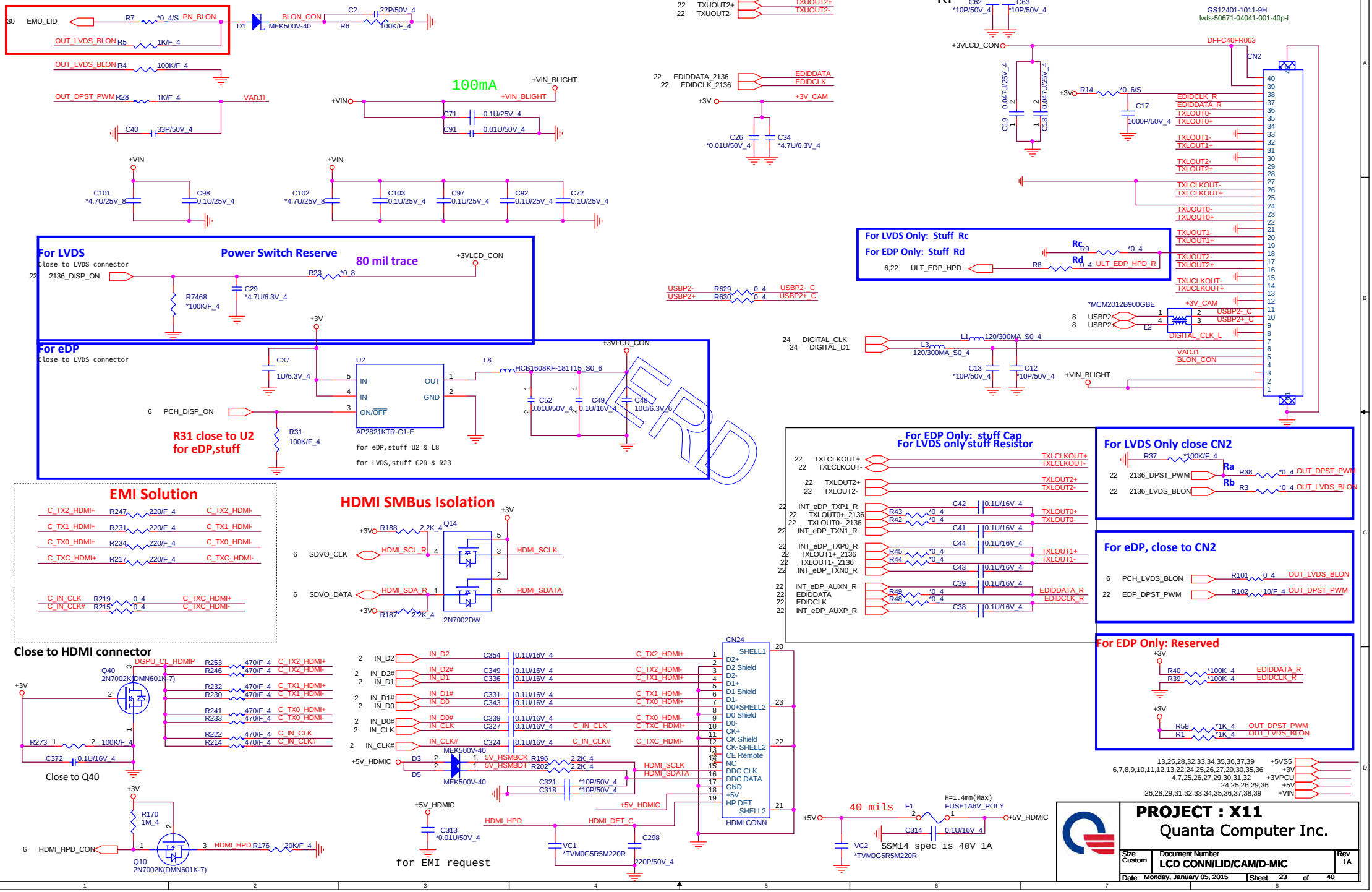
SWR MODE	LDO MODE
Stuff L10	Stuff R59

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	RTD2136	1A

Date: Monday, January 05, 2015 Sheet 22 of 40

LID Switch

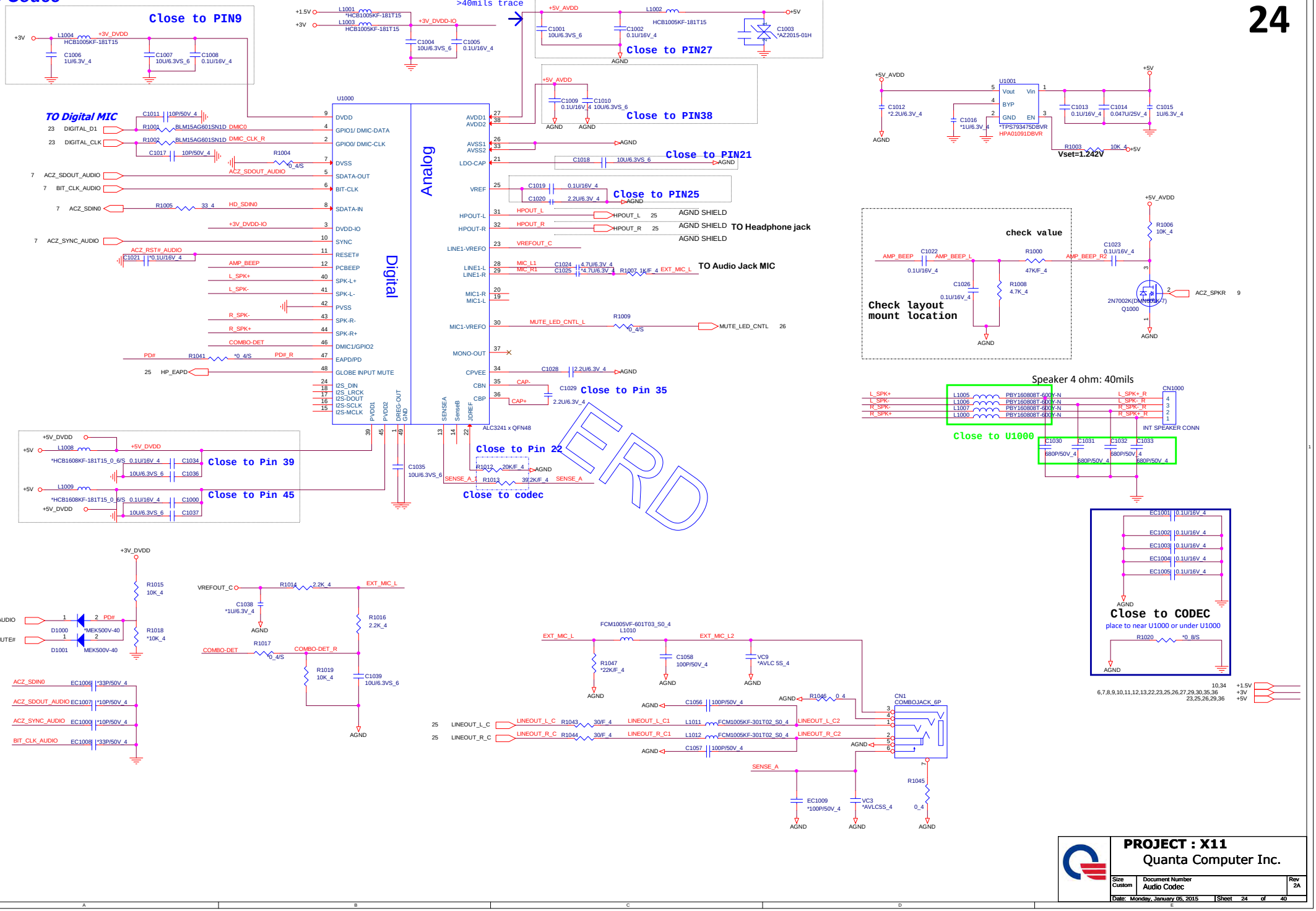


PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM/D-MIC	1A

Date: Monday, January 05, 2015 Sheet 23 of 40

Audio Codec


Close to PIN9
>40mils trace
Close to PIN27
Close to PIN38
Close to PIN21
Close to PIN25
TO Digital MIC
TO Headphone jack
TO Audio Jack MIC
Close to Pin 35
Close to Pin 22
Close to Pin 39
Close to Pin 45
Close to codec
Analog
Digital
U1000
ALC3241 x QFN48
Vset=1.242V
check value
Check layout
mount location
Speaker 4 ohm: 40mils
Close to U1000
INT SPEAKER CONN
Close to CODEC
place to near U1000 or under U1000
COMBOJACK_6P
PROJECT : X11
Quanta Computer Inc.
Audio Codec
Date: Monday, January 05, 2015
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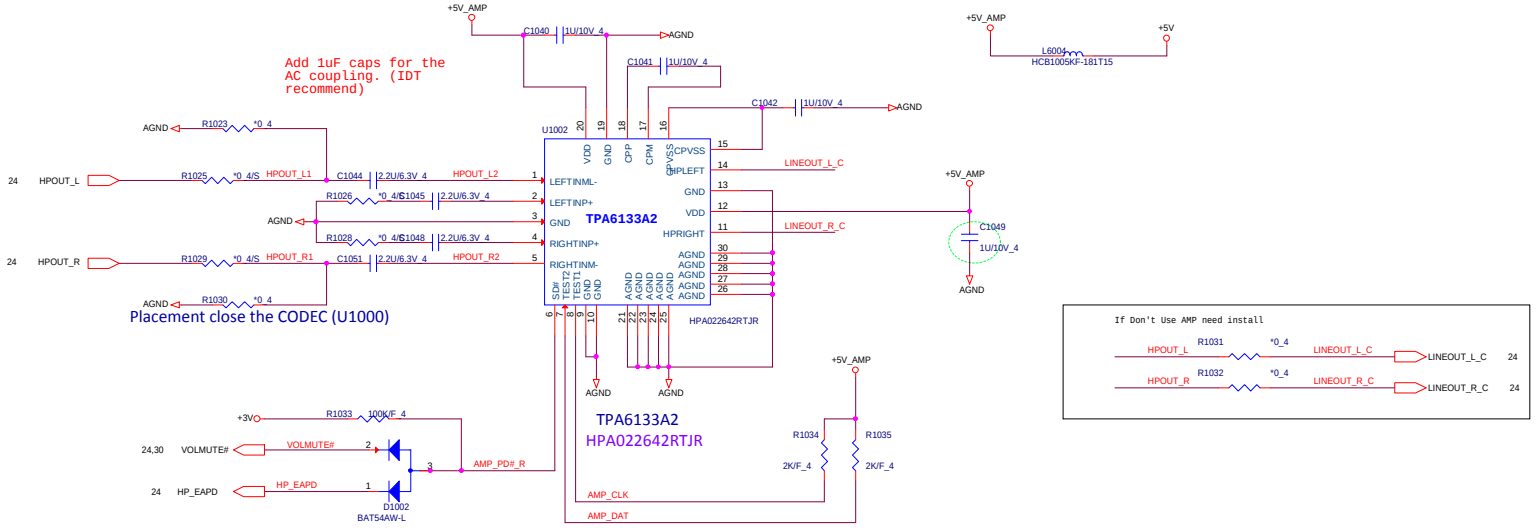
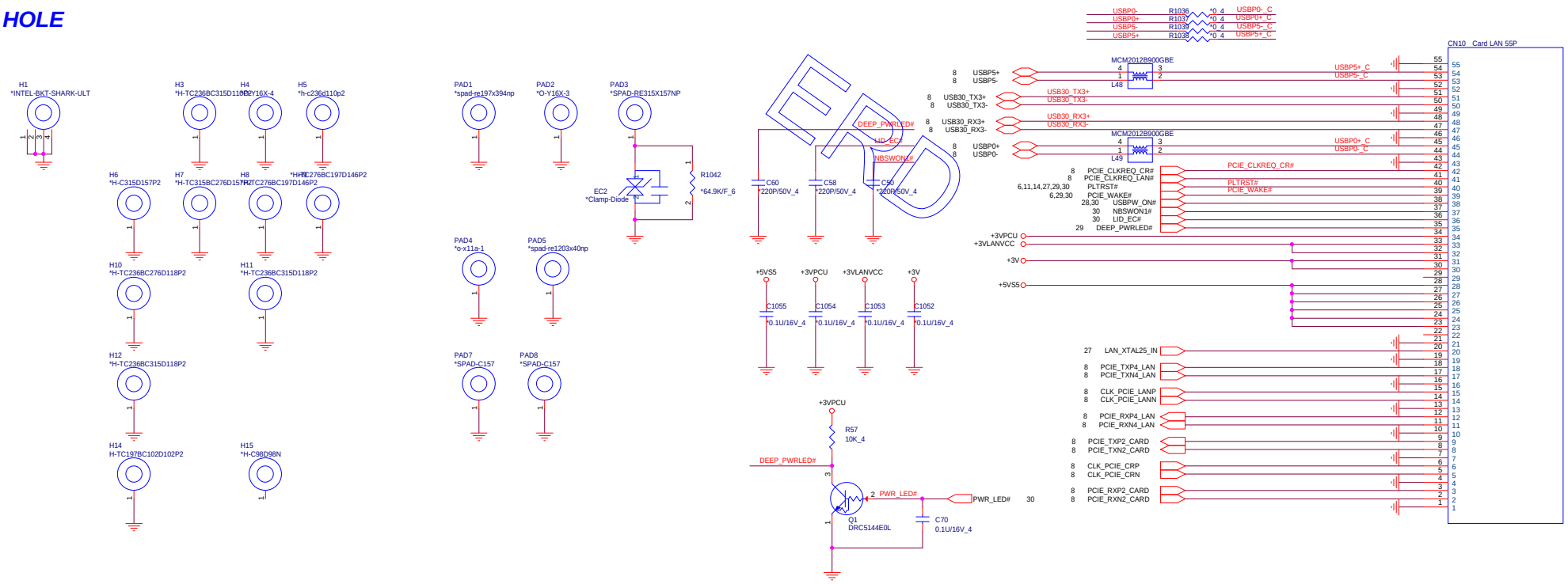
Head Phone out



HOLE



PROJECT : X11			
Quanta Computer Inc.			
Size: C	Document Number: Card Reader		Rev: 1A
Date: Monday, January 05, 2015	Sheet 25 of 40		

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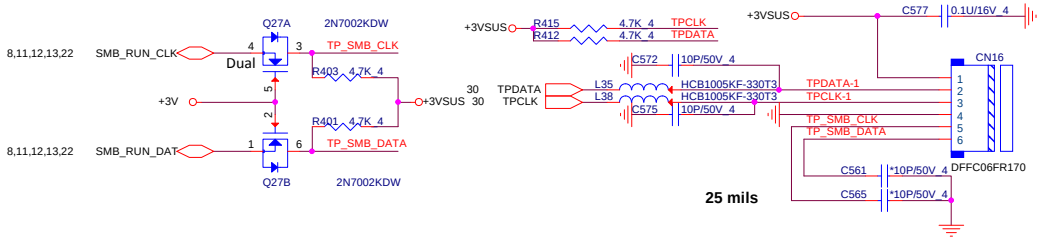
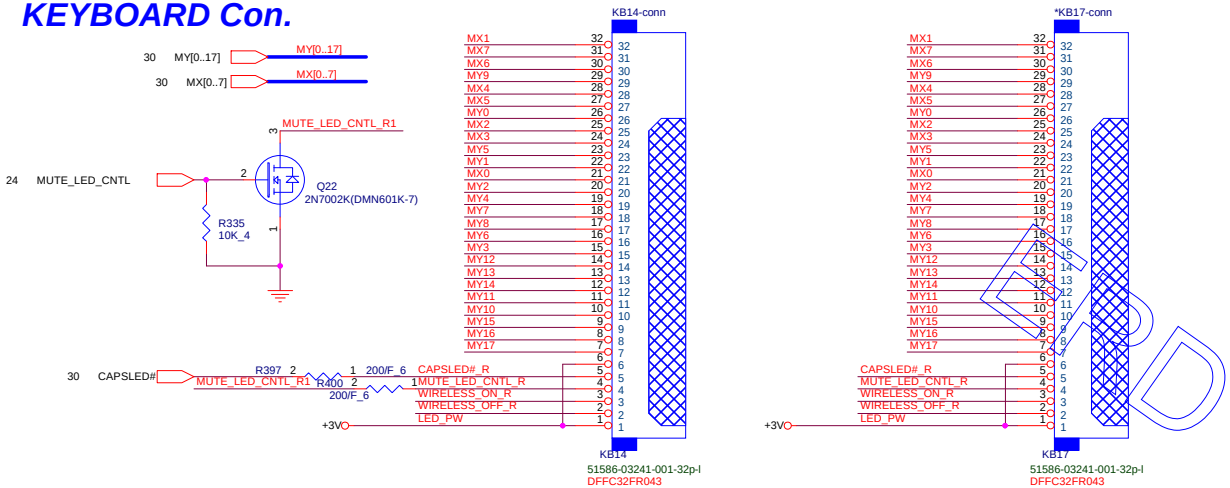
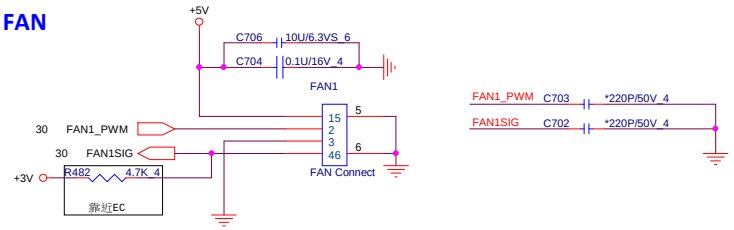
Touch Pad Connector



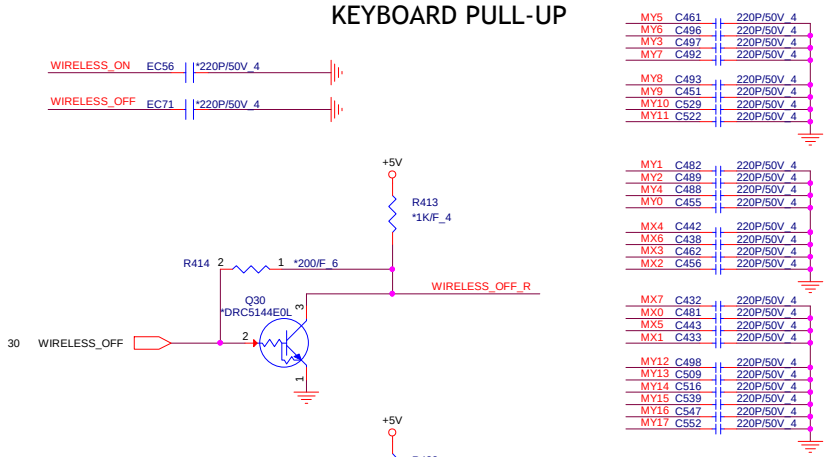
KEYBOARD Con.

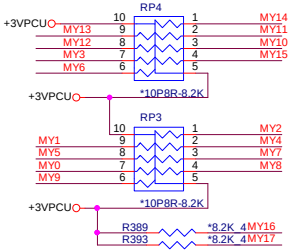


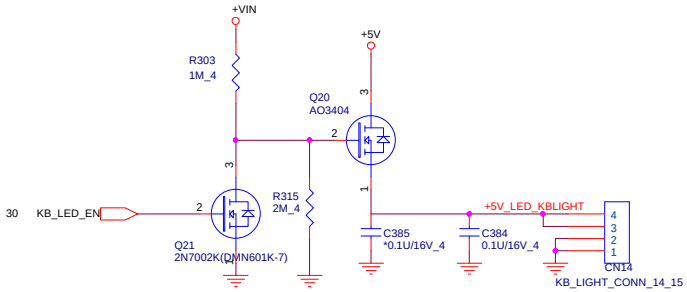
FAN

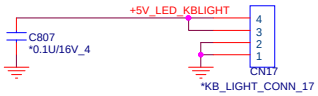


KEYBOARD PULL-UP









PROJECT : X11
Quanta Computer Inc.

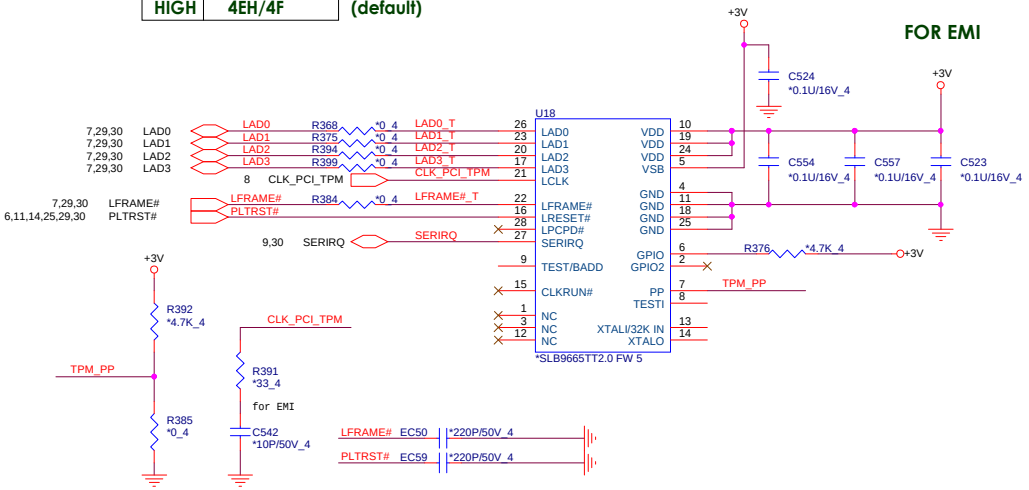
Size	Document Number	Rev
Custom	PB/TP/KB/FAN/EMI Cap	1A
Date: Monday, January 05, 2015	Sheet 26 of 40	

TPM (2.0)

Address

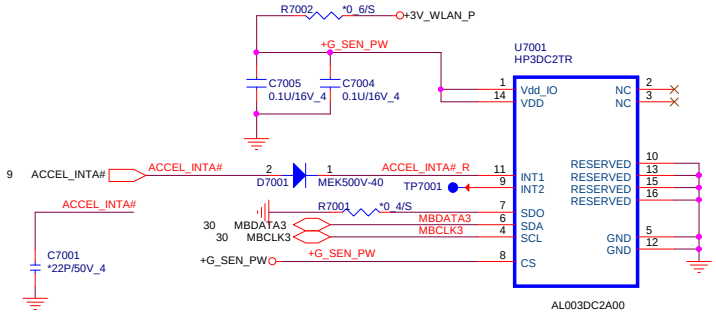
	BADD
HIGH	4EH/4F (default)

FOR EMI

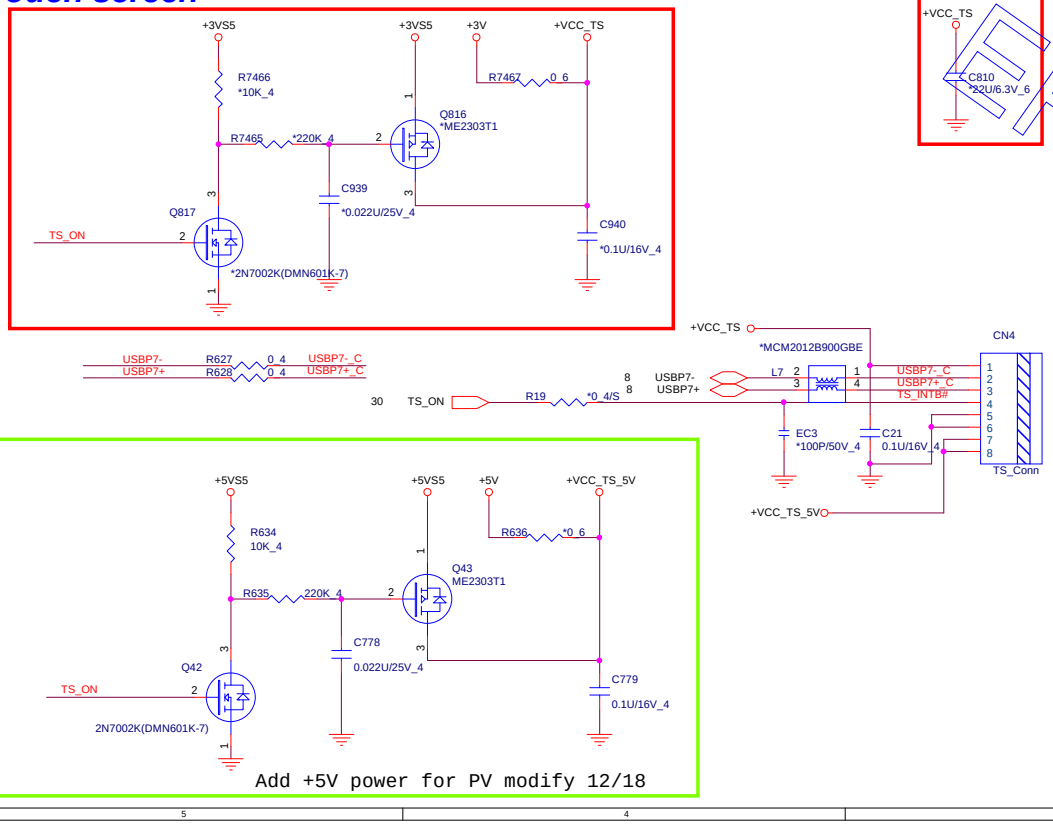


Accelerometer Sensor

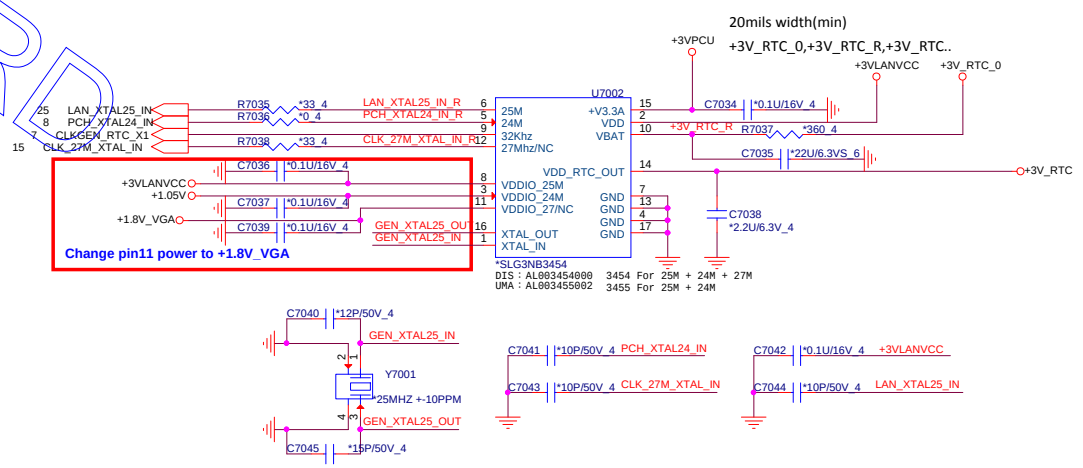
G-Sensor Power need check



Touch screen



Green CLK Circuitry



PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	TPM/G-Sensor/G-CLK/TS/FP	1A

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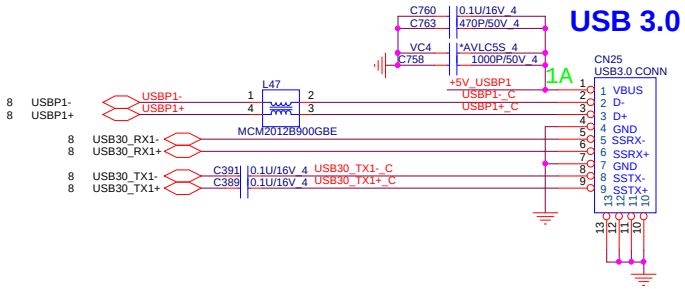
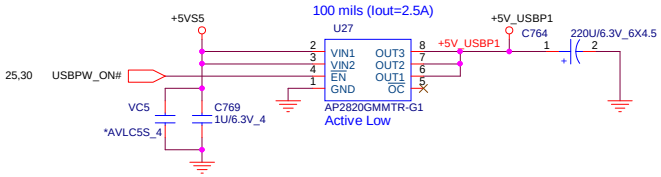
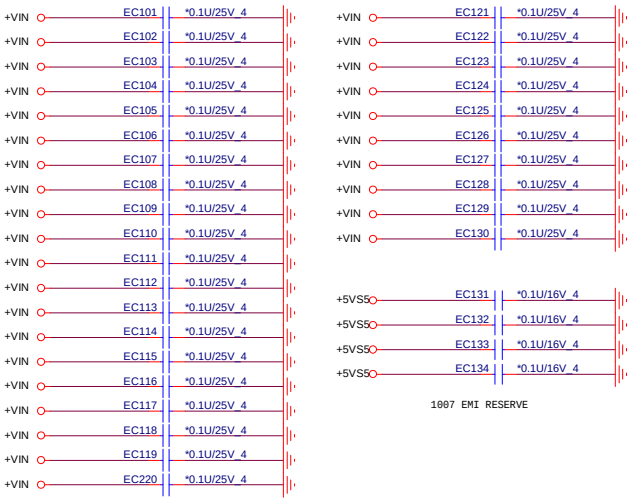
USB 2.0/3.0 Combo





ERD

EMI CAP



PROJECT : X11 Quanta Computer Inc.		
Size: Custom	Document Number: USB 3.0	Rev: 1A
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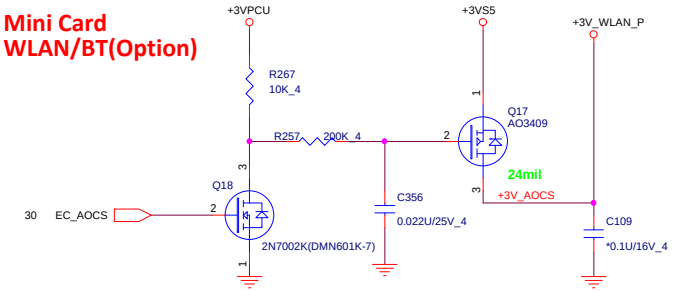
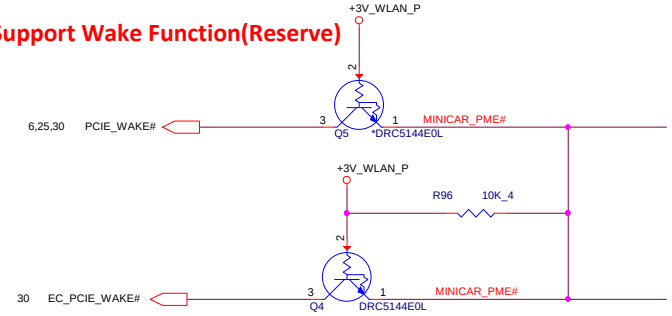
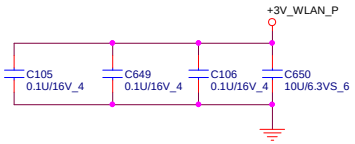
Mini Card WLAN/BT(Option)

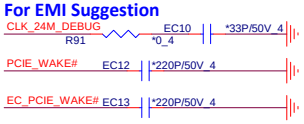


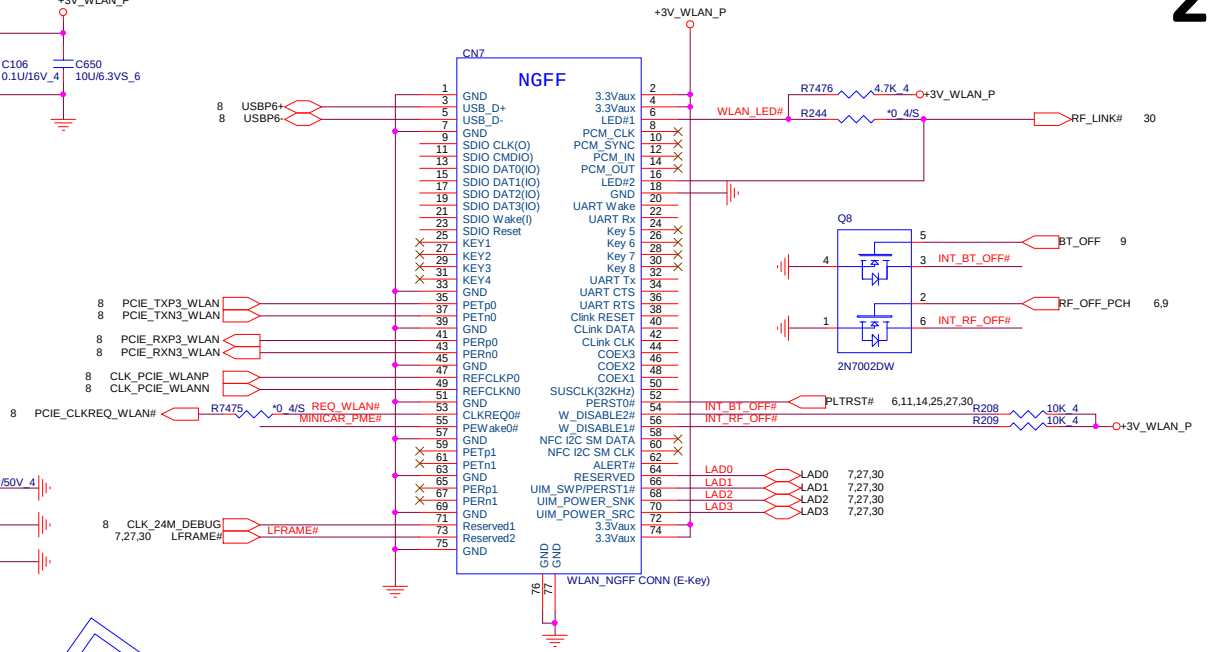
Support Wake Function(Reserve)





For EMI Suggestion

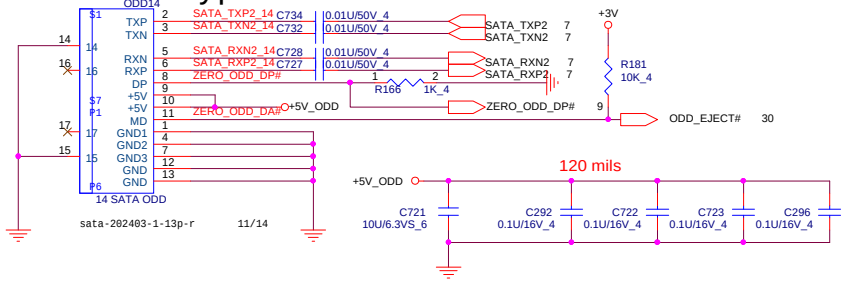




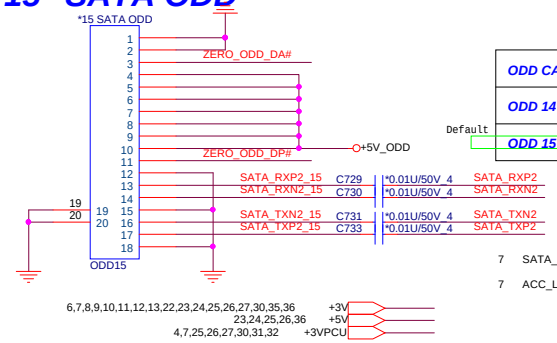
ERD

14" SATA ODD

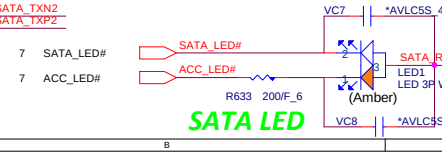
Bypass CAP close conn

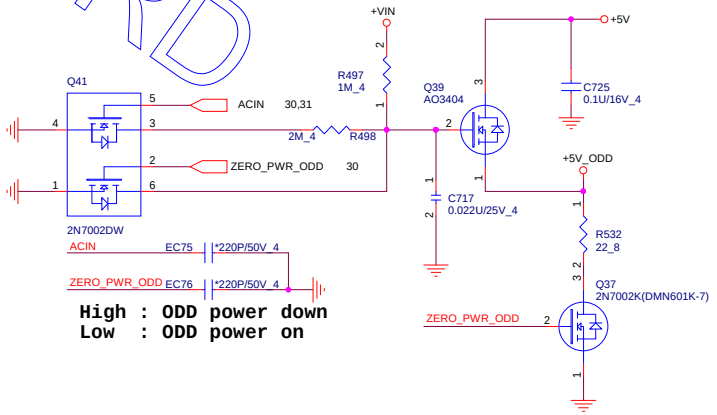


15" SATA ODD

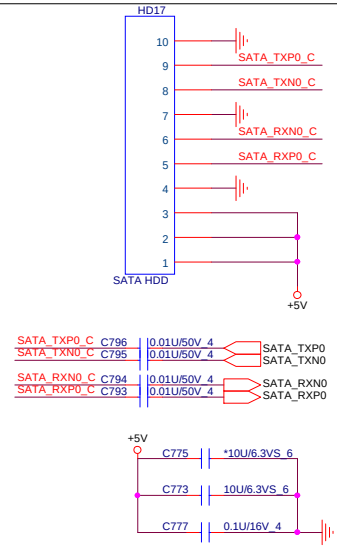


ODD CAP Setting	C727/C728/C732/C734	C729/C730/C731/C733
ODD 14"	O	X
Default ODD 15"/17"	X	O



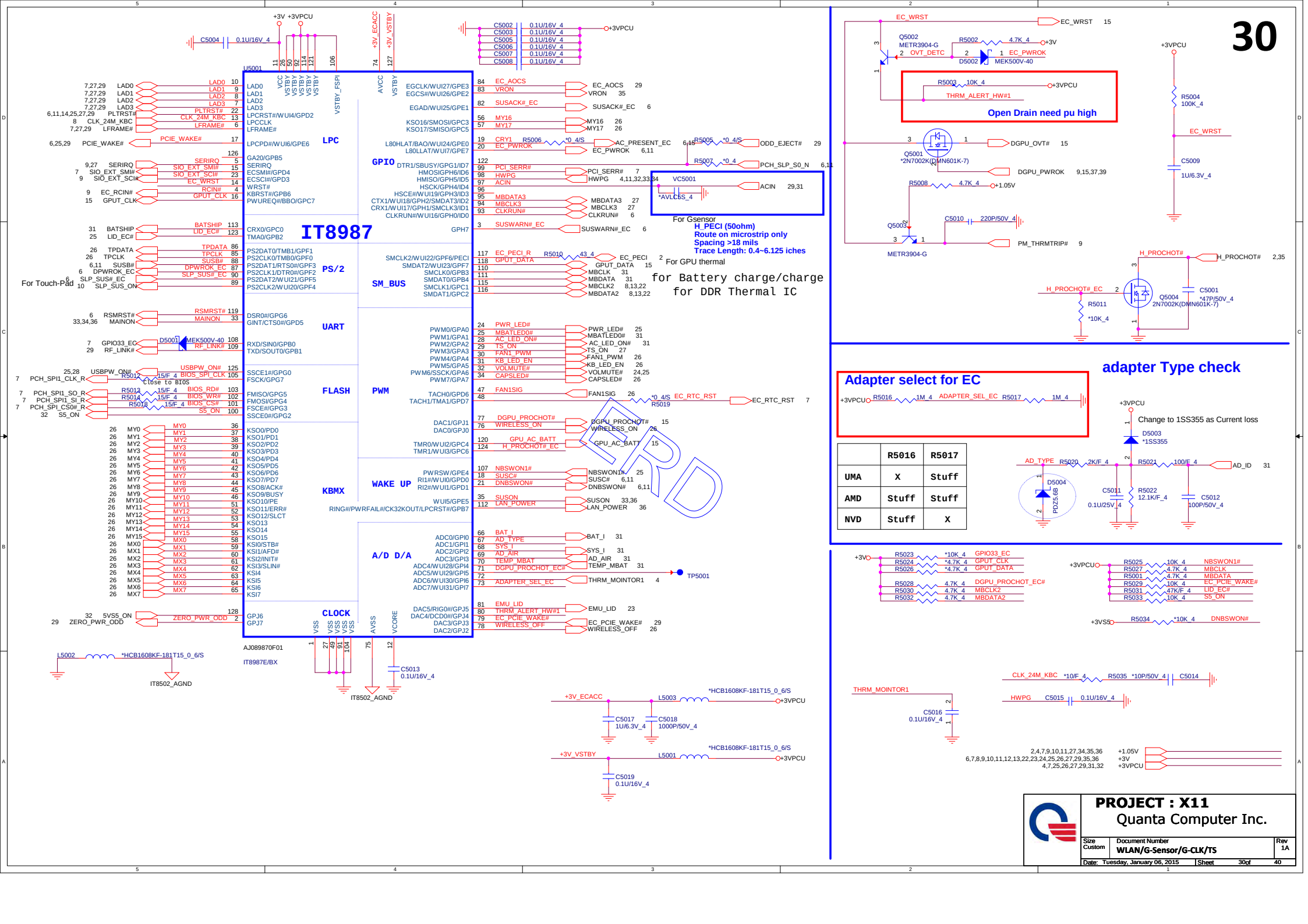


HDD



PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	WLAN/NGFF/MSATA	1A
Date: Monday, January 05, 2015	Sheet 29of 40	


30
IT8987
LPC
GPIO
PS/2
SM_BUS
UART
FLASH
PWM
KBMX
WAKE UP
A/D D/A
CLOCK
H_PECI (50ohm)
Route on microstrip only
Spacing >18 mils
Trace Length: 0.4~6.125 iches
for Battery charge/charge
for DDR Thermal IC
For Gsensor
For GPU thermal
For Touch-Pad
Open Drain need pu high
adapter Type check
Adapter select for EC
Change to 1SS355 as Current loss
PROJECT : X11
Quanta Computer Inc.
WLAN/G-Sensor/G-CLK/TS
Date: Tuesday, January 06, 2015
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90W DC_JACK

AD_ID 30

CN20 DC-IN CONN

EC78 1000P/50V_4

PL6 *0_8/S

PL4 *0_8/S

+VA_AC

PC5 0.1U/25V_4

EC1 0.1U/25V_4

+VA

PQ33 EMB20P03V

IDEA_G

+VAD

PC236 0.1U/25V_4

PD9 P4SMAJ20A

Place this ZVS close to Diode away +VIN

PQ20 AP0203GMT-HF

PC237 2200P/50V_4

BATDIS_G

Do Not add test pad on BATDIS_G signal

PC238 0.1U/50V_6

+PRWSRC

PR211 RC1206-R010

PR228 *0_2/S

PR229 *0_2/S

+VIN

PD10 *P4SMAJ20A

Place this ZVS Far-Far away to +VIN

PQ39 FDMS7698

+BAT_DIS

PR225 4.02K/F_4

BQBATDRV

PC235 0.01U/50V_4

+BATCHG

PL5 *0_8/S

PL7 *0_8/S

BATT+

PC126 0.1U/25V_4

PC127 0.1U/25V_4

14"

2014/9/26 update again

BAT1 BBP28B3-B520A-9H

SMD

SMC

B_TEMP_MBAT

PR226 330_4

PR227 330_4

30 MBDATA

30 MBCLK

PR230 200K/J_4

+3VPCU

PC247 *100P/50V_4

PC248 *100P/50V_4

PD1 PDZ5.6B

PD2 PDZ5.6B

PR231 1K/F_4

TEMP_MBAT 30

PC242 0.01U/50V_4

PC243 0.01U/50V_4

Place this cap close to EC

For EMI

+PRWSRC

EC9 *1U/25V_4

EC6 *1U/25V_4

EC7 *1U/25V_4

EC8 *1U/25V_4

For ISN

+VIN

PC12 4.7U/25V_8

PC244 2200P/50V_4

PC245 1000P/50V_4

PC246 0.1U/25V_4

EC15 10U/25V_8

EC16 10U/25V_8

EC11 10U/25V_8

EC14 10U/25V_8

PQ36 EMB20N03V

+5VPCU

PR235 2.43K/F_6

PC249 1000P/50V_4

PQ41 DRC5144E0L

MBATLED0# 30

+VAD

PQ38 MMDT2907A

PR232 1M_4

PR234 220K_4

PR237 220K_4

PR238 1K_6

+VA

PR241 1M_4

PR242 10F_8

PC251 1U/25V_6

PU1

BQ24780RUYR

CMSRC

ACDRV

VCC

ACDET

BTST

PHASE

LODRV

GND

PAD

SDA

SCL

PROCHOT

BATPRES

TB_STAT

ACIN

ACOK

IADP

IDCHG

ILIM

CMPIN

CMPOUT

PMON

REGN

HIDRV

BQB_2

BQB_1

BQPHASE

BQLODRV

BATSRC

BQSRP

BQSRN

BATDRV

ACP

ACN

REGN6V

PD12 UDZ8V2B-7

PC250 2.2U/10V_6

BQHIDRV

PR19 2.2_6

PC234 0.047U/25V_4

PL8 3.3uH/6A(PCMC063T-3R3MN)

+BAT_DIS

PR137 RC1206-R010

+BATCHG

PC124 10U/25V_8

PC128 10U/25V_8

PC130 0.1U/25V_4

PD8 RB501V-40

PQ37 EMB20N03V

PR14 2.2_6

PC255 2200P/50V_4

PR249 *0_2/S

PR250 *0_2/S

PR255 10/F_6

PR257 10/F_6

PR259 10/F_6

PC256 0.1U/25V_4

PC257 0.1U/25V_4

PC258 0.1U/25V_4

CSOP

CSON

PV change

BQACDRV

BQVCC

BQACDET

BQACMSRC

BQACP_N

BQACN_N

PC239 1U/25V_6

PC240 0.1U/25V_4

PC241 0.1U/25V_4

PR239 *0_4/S

PR240 *0_4/S

ACDET=16.83V

+VA_AIR

PD13 1N4448WS-7-F

PR243 *430K/F_4

PR244 430K/F_4

PR246 75K/F_4

PR247 71.5K/F_4

PC252 *1000P/50_4

PR248 *0_4/S

PR252 0_4/P

PR253 *0_4/S

PR254 *100K/F_4

PR268 *0_4/S

PR256 *100K/F_4

MBDATA

MBCLK

BQDATA

BQCLK

BQPROCHOT

BQBATPRES

BQTB_STAT

PROCHOT#

TP14

+3VPCU

30 AD_AIR

PC254 0.1U/16V_4

PR251 12.4K/F_4

Place this cap close to EC

+5VPCU

PR245 2.43K/F_6

PC253 1000P/50_4

PQ42 DRC5144E0L

AC_LED_ON# 30

REGN6V

PR258 100K/F_4

29,30 ACIN

PR260 100K/F_4

30 SYS_I

PR261 10/F_4

PC259 0.01U/50V_4

PC260 100P/50_4

BQIADP

BQIBAT

Place this cap close to EC

20mV/W (default)

PR263 *0_2/S

PR264 *0_4/S

PC261 100P/50_4

PMON

+3VPCU

PR265 10/F_4

30 BAT_I

PC262 0.01U/50V_4

PC263 100P/50_4

PR266 100K/F_4

PR267 43.2K/F_4

BQLIM

VIDCHG = 8 or 16 × (VSRN – VSRP)

Place this cap close to EC

+BATCHG

PR262 *470_8

30 BATSHIP

PQ43 *DMN601K-7

15"

BAT15 *BBP28B3-B520A-9H

2014/9/26 update again

17"

BAT17 *51483-00801-V01

+3VPCU 4,7,25,26,27,29,30,32

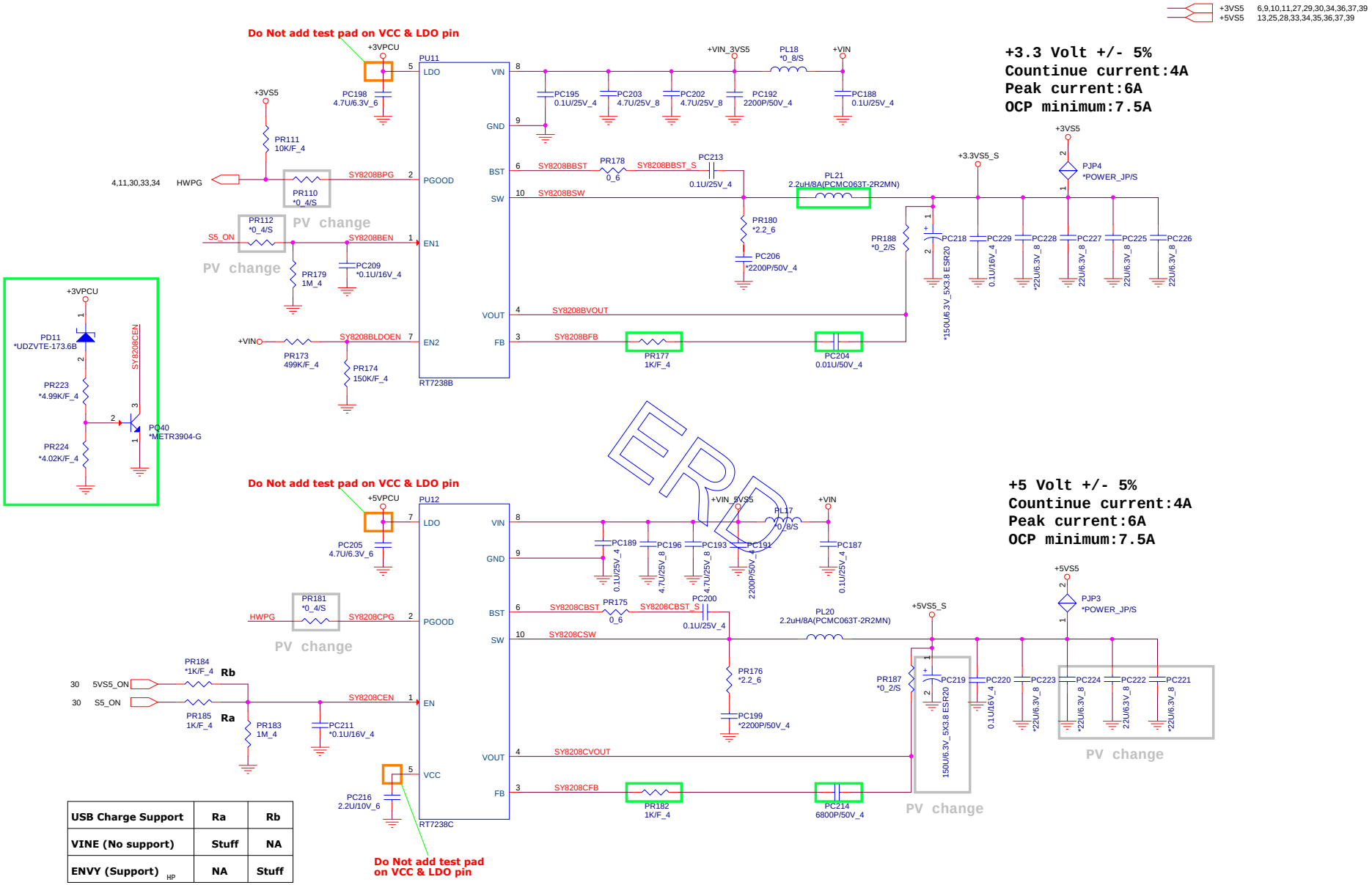
+5VPCU 13,32

PROJECT : X11

Quanta Computer Inc.

Size	Document Number	Rev
Custom	Charger (BQ24780)	1A

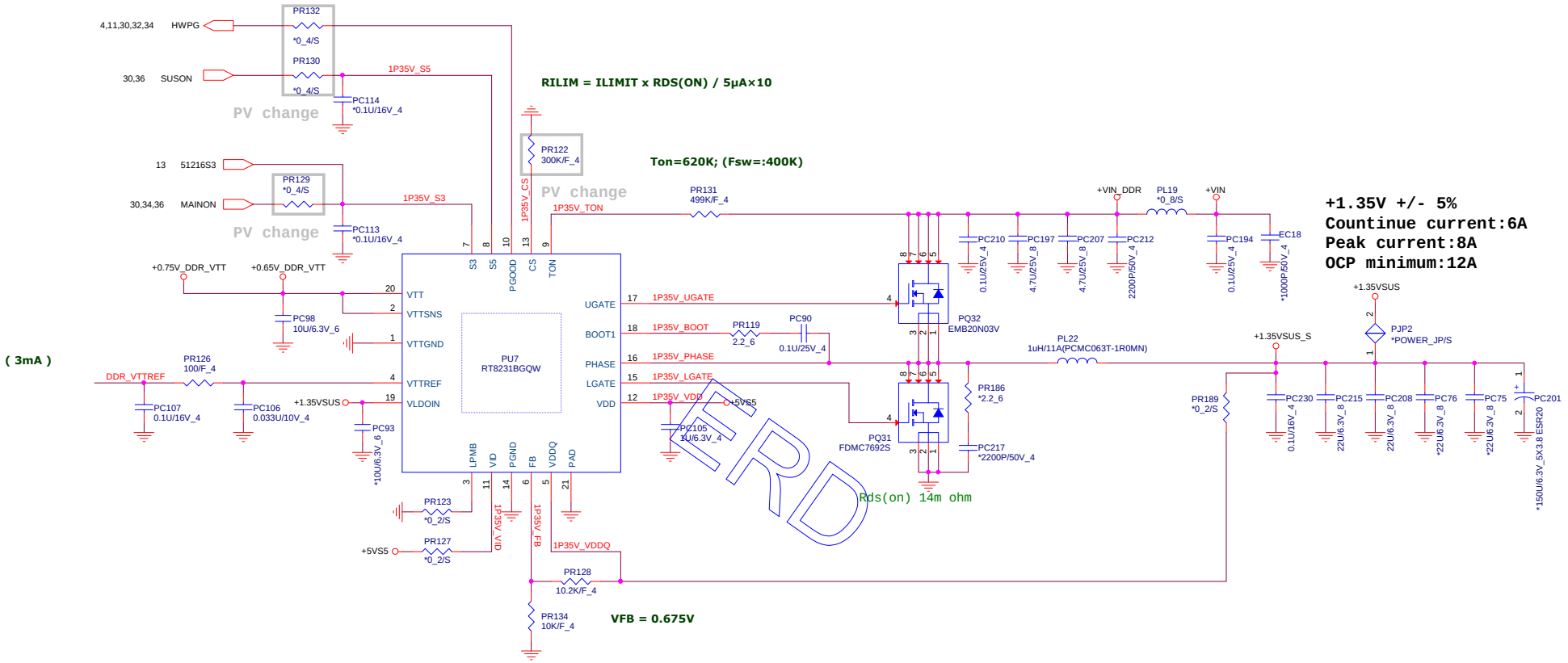
Date: Monday, January 05, 2015 Sheet 31 of 40



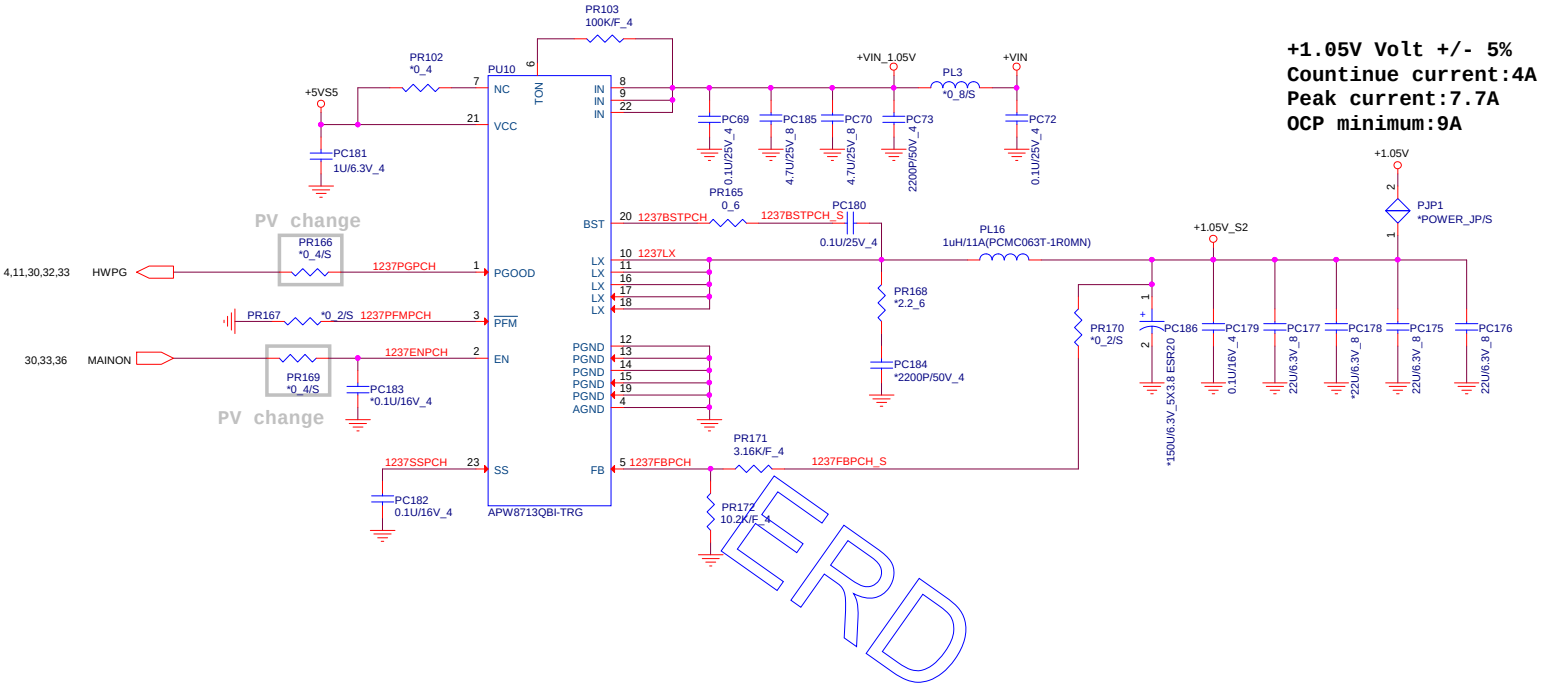
USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support) HP	NA	Stuff

PROJECT : X11
Quanta Computer Inc.

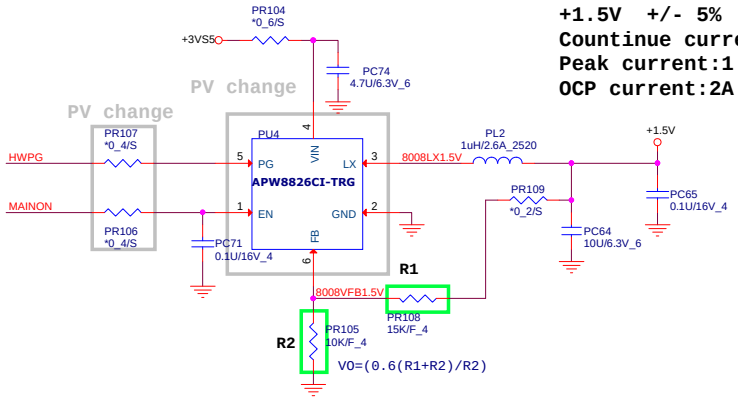
Size	Document Number	Rev
Custom	3/5VPCU(RT8243A)	1A
Date: Monday, January 05, 2015	Sheet 32 of 40	



PROJECT : X11		
Quanta Computer Inc.		
Size: Custom	Document Number: DDR3 (RT8231A)/1.8VS5	Rev: 1A
Date: Monday, January 05, 2015	Sheet 33 of 40	



+1.05V Volt +/- 5%
Countinue current:4A
Peak current:7.7A
OCP minimum:9A



+1.5V +/- 5%
Countinue current:1.3A
Peak current:1.5A
OCP current:2A

+VIN	23,26,28,29,31,32,33,35,36,37,38,39
+3VS5	6,9,10,11,27,29,30,32,36,37,39
+5VS5	13,25,28,32,33,35,36,37,39

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.1VS5 (RT8228)/2.5V	1A
Date: Monday, January 05, 2015	Sheet 34 of 40	

+VIN 23,26,28,29,31,32,33,34,36,37,38,39
+VCC_CORE 4
+3V 6,7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,36
+5VS5 13,25,28,32,33,34,36,37,39
+V1.05S_VCCST 2,4,7,9,10,11,27,30,34,36

POP Rb and no POP Ra for nex version.

Place this NTC close to inductor

Place this NTC close to MOSFET

For Acoustic

Boot Voltage Table	
R_boot	V_boot
30.1K	0V
49.9K	1.65V
69.8K	1.7V
90.9K	1.75V

PU3 NCP81101MNTXG

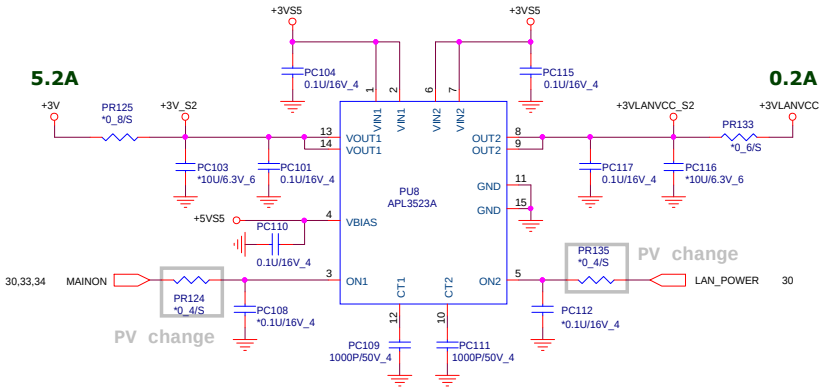
PV change

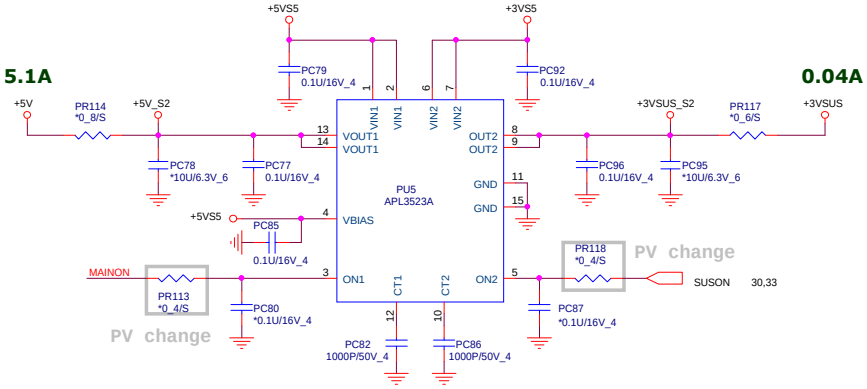
15W
Icc_Max=32A
I_TDC=14A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=7m
AC_LL_VOS=9.4m
VBOOT=1.7V

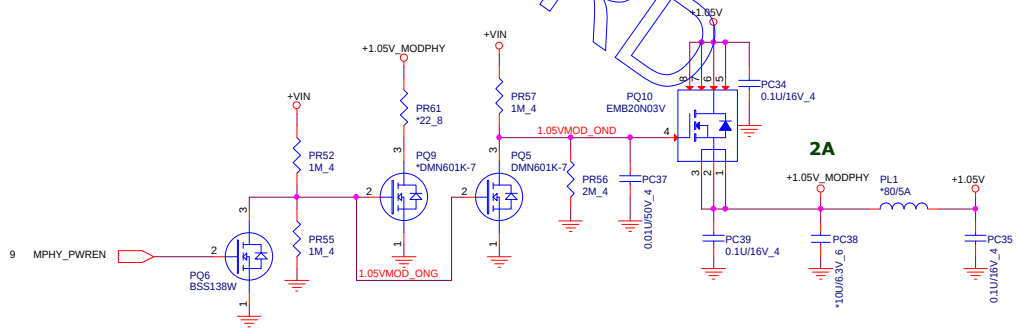
28W
Icc_Max=40A
I_TDC=19A
I_Dynamic=27A
V_Operate=1.6V~1.8V
DC_LL=2m
AC_LL=7m
AC_LL_VOS=9.4m
VBOOT=1.7V

PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	CPU Core (NCP81101)ULT	1A
Date: Monday, January 05, 2015	Sheet 35 of 40	







6,7,8,9,10,11,12,13,22,23,24,25,26,27,29,30,35 +3V
23,24,25,26,29 +5V
23,26,28,29,31,32,33,34,35,37,38,39 +VIN
6,9,10,11,27,29,30,32,34,37,39 +3VS5
13,25,28,32,33,34,35,37,39 +5VS5
25,27 +3VLANVCC

PROJECT : X11 Quanta Computer Inc.		
Size: Custom	Document Number: Dis-charge IC (SLG55448)	Rev: 1A
Date: Monday, January 05, 2015	Sheet 36 of 40	

+MVDDQ Volt +/- 5%
Countinue current:6A
OCP_TDC=12.6A
OCP_SPIKE=18A(1ms)
Vboot=0.9V
LL=0 V/A
external offset=0.45V

DCR=9mohm

PV change

VID Override table (VDD)

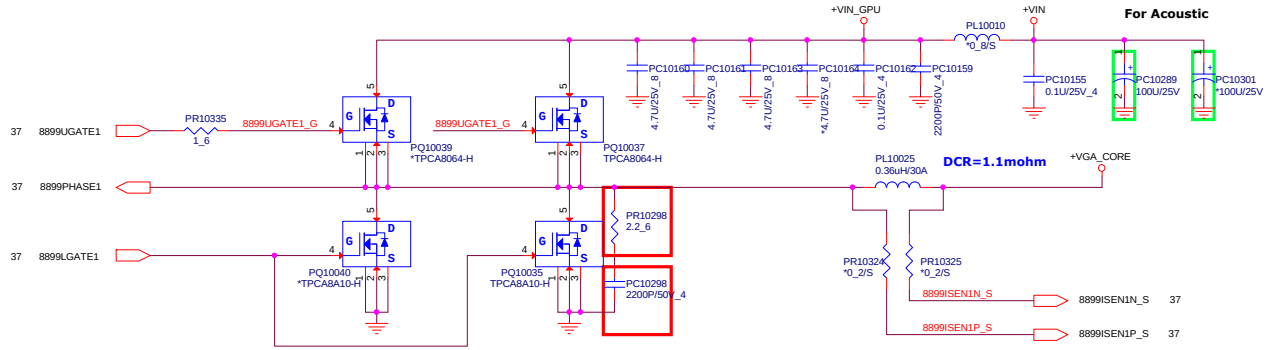
SVC	SVD	Boot Voltage
0	0	1.1V
0	1	1.0V
1	0	0.9V
1	1	0.8V

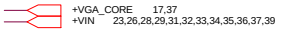
Vset1	109.5mV
Delta Vset1	309.9mV
Vset2	121.8mV
Delta Vset2	18.7mV

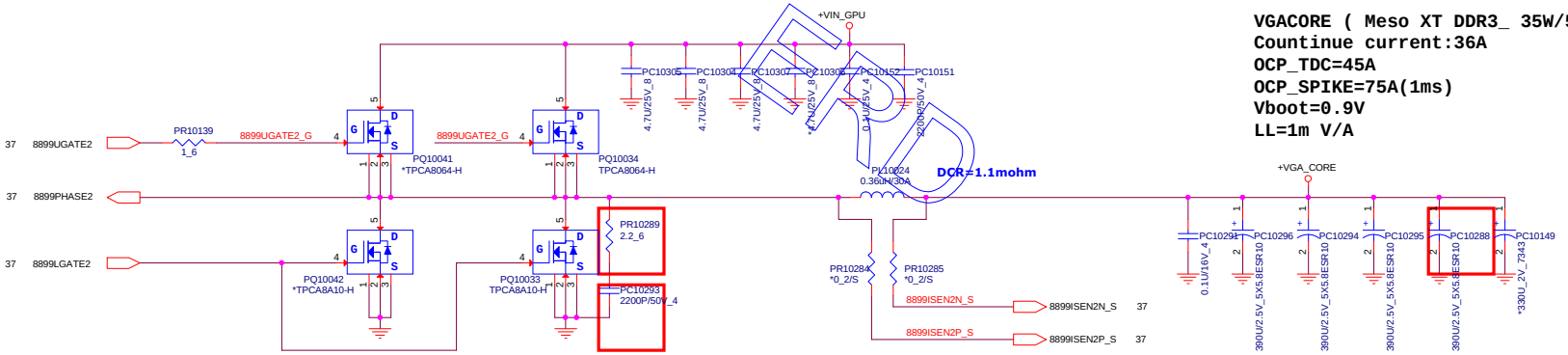
PUT COLSE TO MVDDQ HOT SPOT

PUT COLSE TO VDDC HOT SPOT

PROJECT : X11	
Quanta Computer Inc.	
Size: Custom	Document Number: Vcore(RT8899A)
Rev: 1A	
Date: Monday, January 05, 2015	Sheet 37 of 43

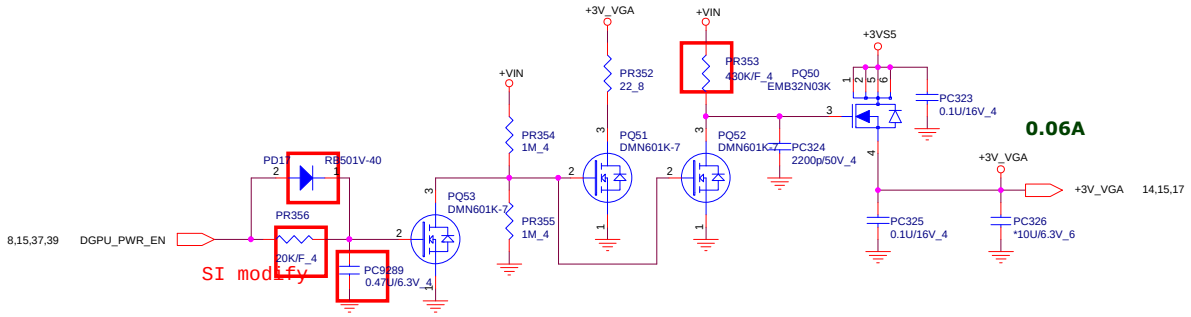




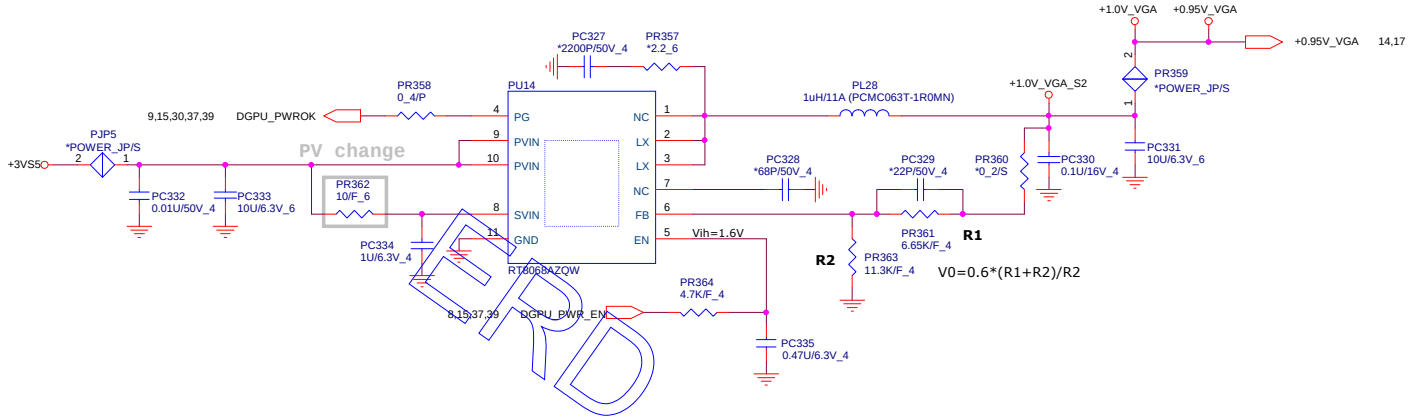


VGACORE (Meso XT DDR3_ 35W/53W(1ms))
Countinue current:36A
OCP_TDC=45A
OCP_SPIKE=75A(1ms)
Vboot=0.9V
LL=1m V/A

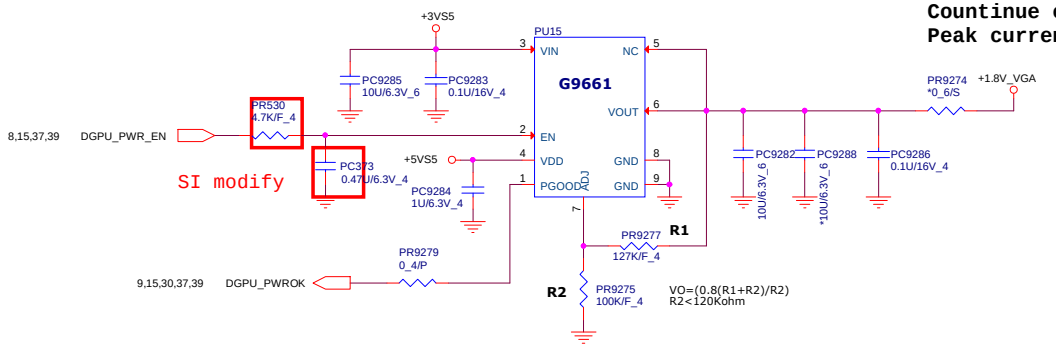
PROJECT : X11 Quanta Computer Inc.		
Size: Custom	Document Number: CPU Core2	Rev: 1A
Date: Monday, January 05, 2015	Sheet 38 of 43	

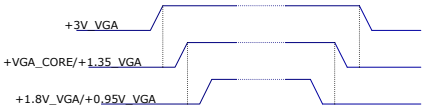


+0.95V +/- 3%
Countinue current:2A
Peak current:3A
OCP minimum:4A[HP]



+1.8V_VGA +/- 5%
Countinue current:0.5A
Peak current:2A





PROJECT : X11
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGA POWER	1A
Date: Monday, January 05, 2015	Sheet 39 of 9	

Battery Connector	Pavillion	ENVY
14"	-	-
15"	-	-
17"	-	-

USB Charge Support	PR185	PR184
Pavillion	Stuff	NA
ENVY (USB charge)	NA	Stuff

UMA	Disable Page 41、42、43 ,but keep below location
Page 41	PC161、PC162
Page 42	PC138、PC144、PC4、PC148
Page 43	PC84、PC102、PC88、PC97、PC40、PC33

Discrete	Location	Part Number
N15S (25W)	PR155	CS29532FB10
	PC151、PC160	NA
	PQ21、PQ23、PQ25、PQ28	NA
N15P (35W)	PR155	CS31242FB13
	PC151、PC160	Stuff
	PQ21、PQ23、PQ25、PQ28	Stuff