POWER PAVILION Trifle INTEL SKL / KABY -H SYSTEM DIAGRAM

01

Charge PG.40

DDR4 PG.42

CPU Core PG.43~45

+1.0V/+1.2VSUS PG.47~48

+3V/+5V S5 PG.41

+VGACORE PG.49

+1.35V_GFX PG.50

Config#3 SODIMM 1DPC

SODIMM1 Max. 8GB STD PG.17 — DDR4 2133MHz — Channel A

SODIMM2 Max. 8GB RSV PG.18 — DDR4 2133MHz — Channel B

INTEL SkyLake - H4+2 / Kaby Lake - H4+2
Processor : Quad Core
Power : 45 (Watt)
Package : BGA1440
Size : 42 x 28 (mm)
Die Size : 13.6 x 9.1 (mm)
PG.2~8

PEG X8 Lane — NVIDIA N17P-G0-A1
Package 29 x 29mm
40W PG.19~23

27MHz PAGE 21

VRAM gDDR5 x 4pcs
128M x32 / 256M x32
2.5GHz PG.14~25

HDMI v2.0 PG.27

eDP (5.4Gb/s) eDP — 15.6" eDP Panel HD/FHD/UHD PG.26

DMI

M.2 2280-S3 SSD PG.33 — SATA0 6GB/s SATA0A / PCIEx4 32GB/s LANE9,10,11,12

HDD PG.32 — SATA0 6GB/s SATA1B

INTEL PCH
Lynx Point
Power : Watt
Package : FCBGA837
Size : 23 x 23 (mm)
cdp PG.9~16

USB 3.0 PORT1 PORT2 PORT3 PORT4
- USB 3.0 Ports PG.30
- USB 3.0 Ports (DB) PG.30
- USB 3.0 Ports (DB) PG.30
- USB3.0 Re-Driving IC PTN36241G PG.31 — 3D Camera Intel F200 3D PG.31

USB 2.0 PORT1 PORT2 PORT3 PORT4 PORT5 PORT8
- HD CAM PG.26
- HD + IR CAM (OPTION) PG.26,34
- Touch Screen Synaptics S7817 PG.26

PCI-E x 1 Gen1
- LANE7 — LAN RTL8107ESH/ 10/100 cdp / RTL8111HSH/ Gbe PG.35
- LANE5 — Card Reader RTS5237S-GR PG.36
- LANE6 — WLAN BT COMBO PG.33 — USB 2.0 PORT7

SPI — G-Sensor HP2DC PG.34 (SMBUS) / ROM PG.12 (LPC)

LPC — KBC ITE IT8987E/BX PG.37
- TPM 2.0 SLB9665TT2.0 (OPTION) PG.34
- KB PG.38
- TP PG.38
- FAN PG.38

Azalia — AUDIO CODEC ALC3258-CG PG.28
- Headphone amplifier HPA0022642RTJR PG.29 — Hp / MIC — Combo Jack (DB) PG.30
- Speaker PG.28
- Dual Digital MIC PG.28 — 3D CAM MIC / INT CAM MIC PG.26

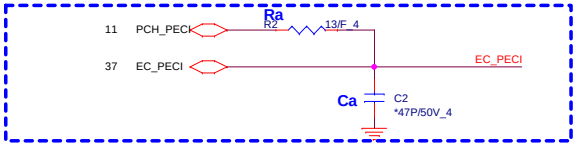
STACKUP
TOP
GND
IN1
IN2
VCC
IN3
GND
BOT

PROJECT : G35
Quanta Computer Inc.
Size: Custom | Document Number: 01 -- Block Diagram | Rev: 1A
Date: Tuesday, June 07, 2016 | Sheet 1 of 52

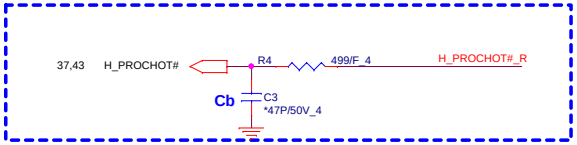
SKYLAKE Processor (CLK,MISC,JTAG)

02

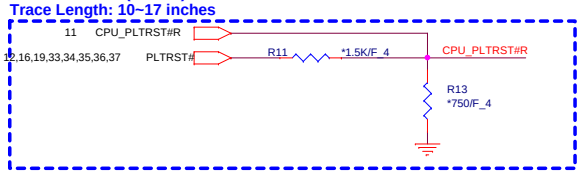
H_PECI (50ohm)
Trace Length: <0.5 iches
Ra,Ca need placement close to PCH.



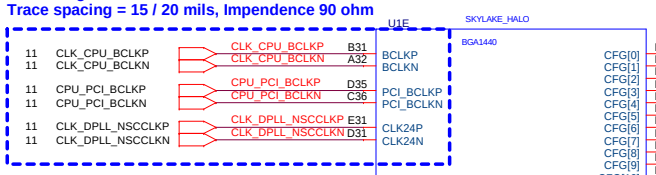
PROCHOT# (50ohm)
Trace Length <11 inches
Cb need placment near VR

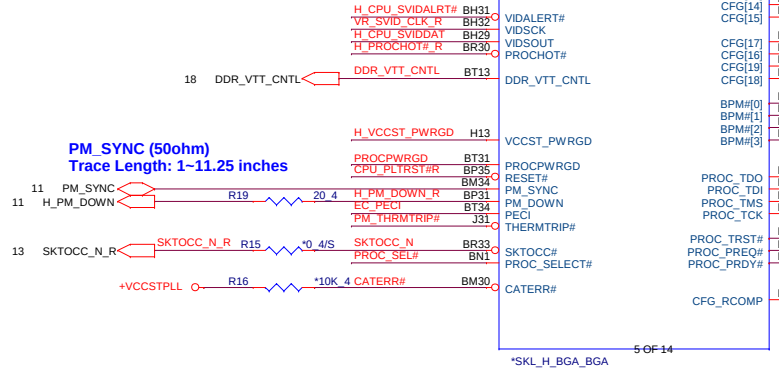


CPU_PLTRST# (50ohm)
Trace Length: 10~17 inches

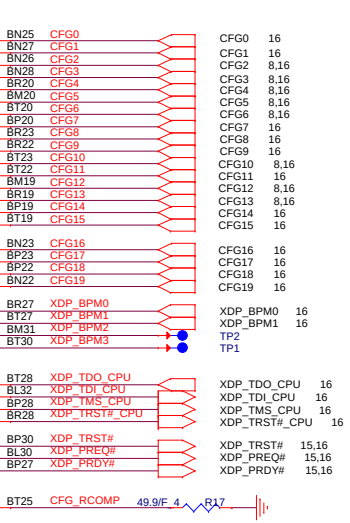


Host CLK:
Trace length < 11000 mils
Trace spacing = 15 / 20 mils, Impendence 90 ohm



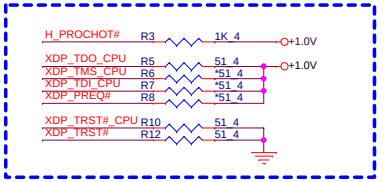


PM_SYNC (50ohm)
Trace Length: 1~11.25 inches



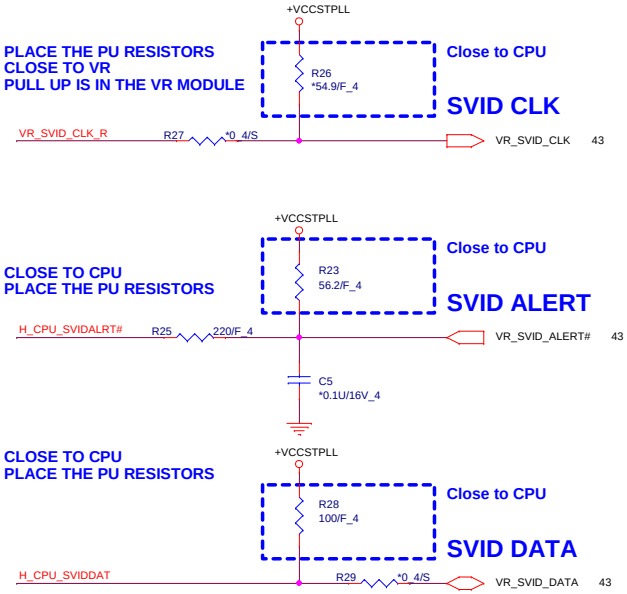
Design Note(CFG_RCOMP):
DEFENSIVE DESIGN 50-OHM FOR R40PR (SV REQ)

Processor pull-up (CPU)

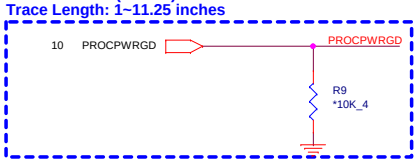


CPU CORE SVID

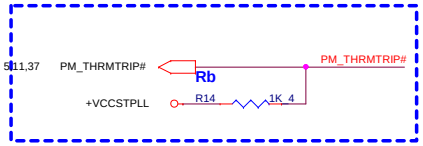
Layout note:
1.Need routing together
2.ALERT need between CLK and DATA.



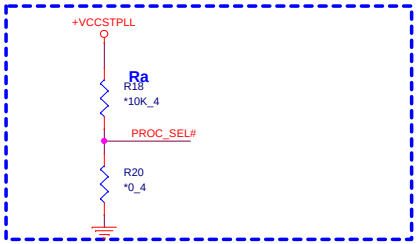
PROCPWRGD (50ohm)
Trace Length: 1~11.25 inches



THERMTRIP# (50ohm)
Trace Length: 1.1~12 inches
Rb need placment near PCH

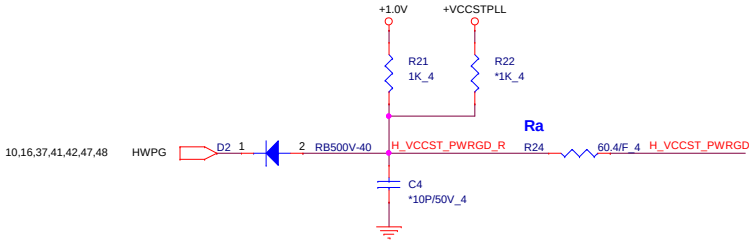


Ra(R10804) Not install in SKL-H



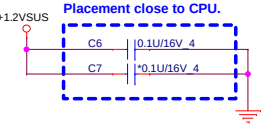
HWPD

Ra close to CPU side
H_VCCST_PWRGD trace 0.3" - 1.5"



CPU VDDQ

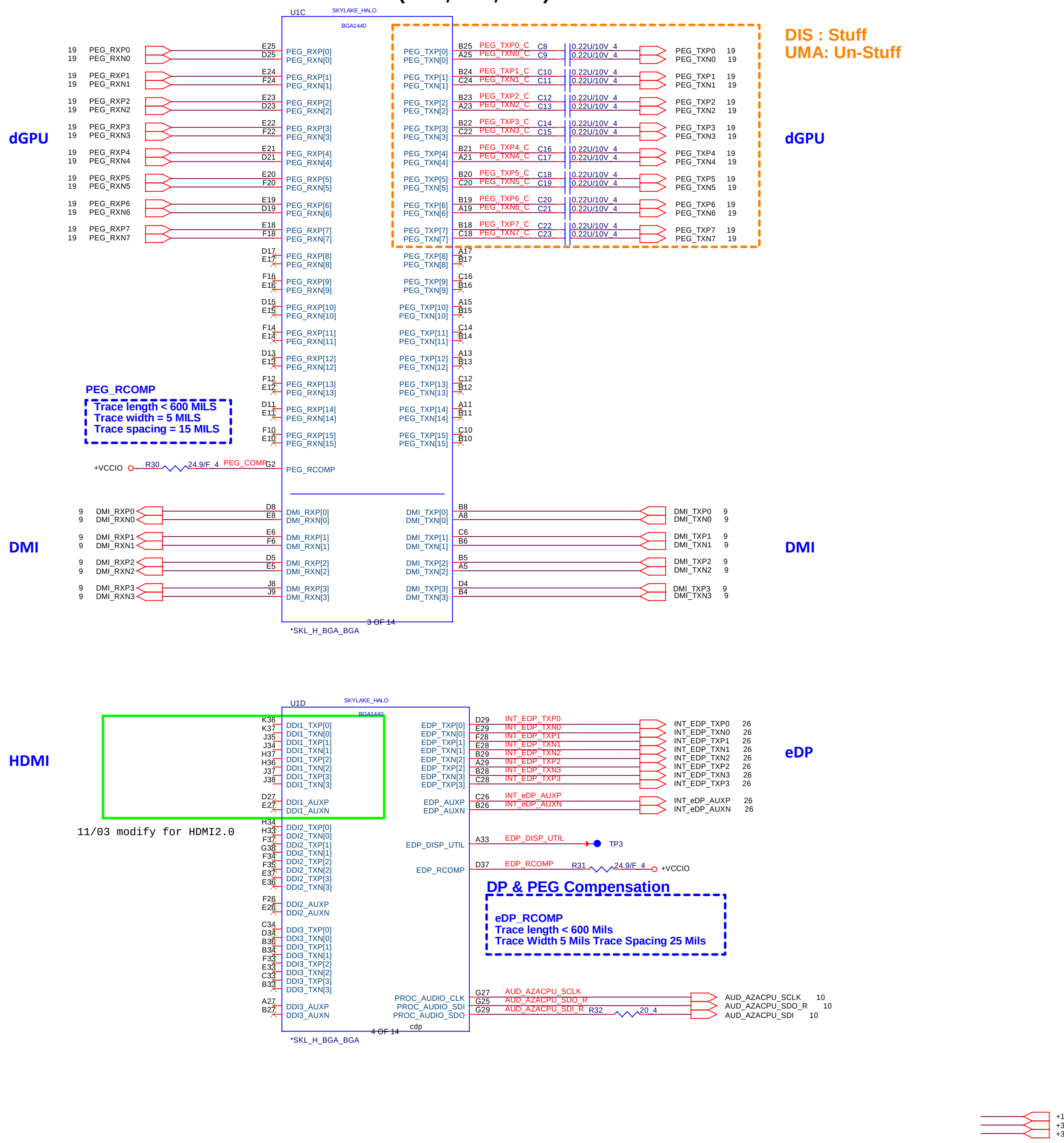
Note: please keep plane is enough for VDDQ 2.8A



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	02 -- SKL 1/7 (JTAG/MISC)	1A
Date: Tuesday, June 07, 2016	Sheet 2 of 52	

SKYLAKE Processor (DMI,PEG,FDI)



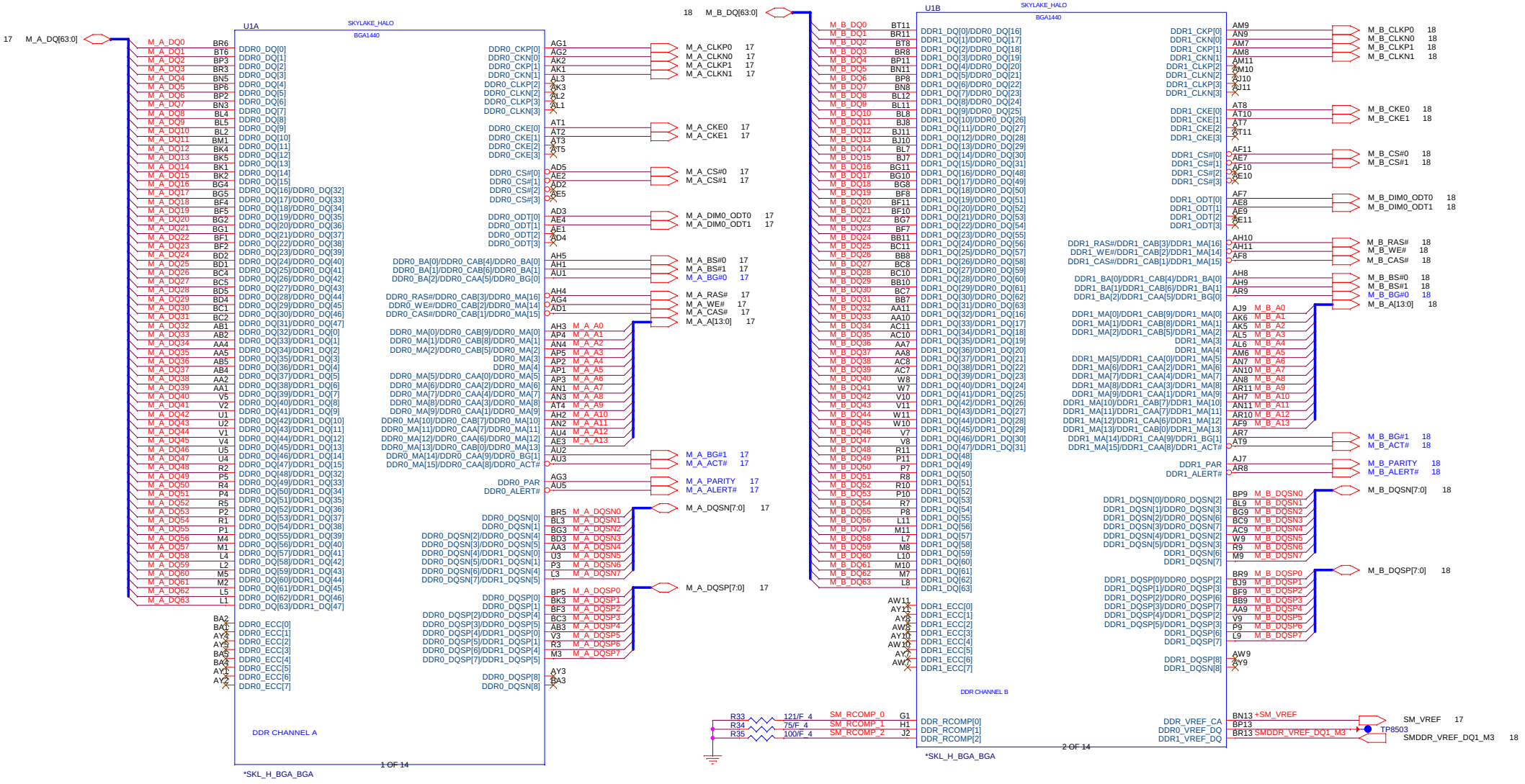
PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	03 -- SKL 2/7 (DMI/EDP/PEG)	1A

Date: Tuesday, June 07, 2016 Sheet 3 of 52

SKYLAKE Processor (DDR4)

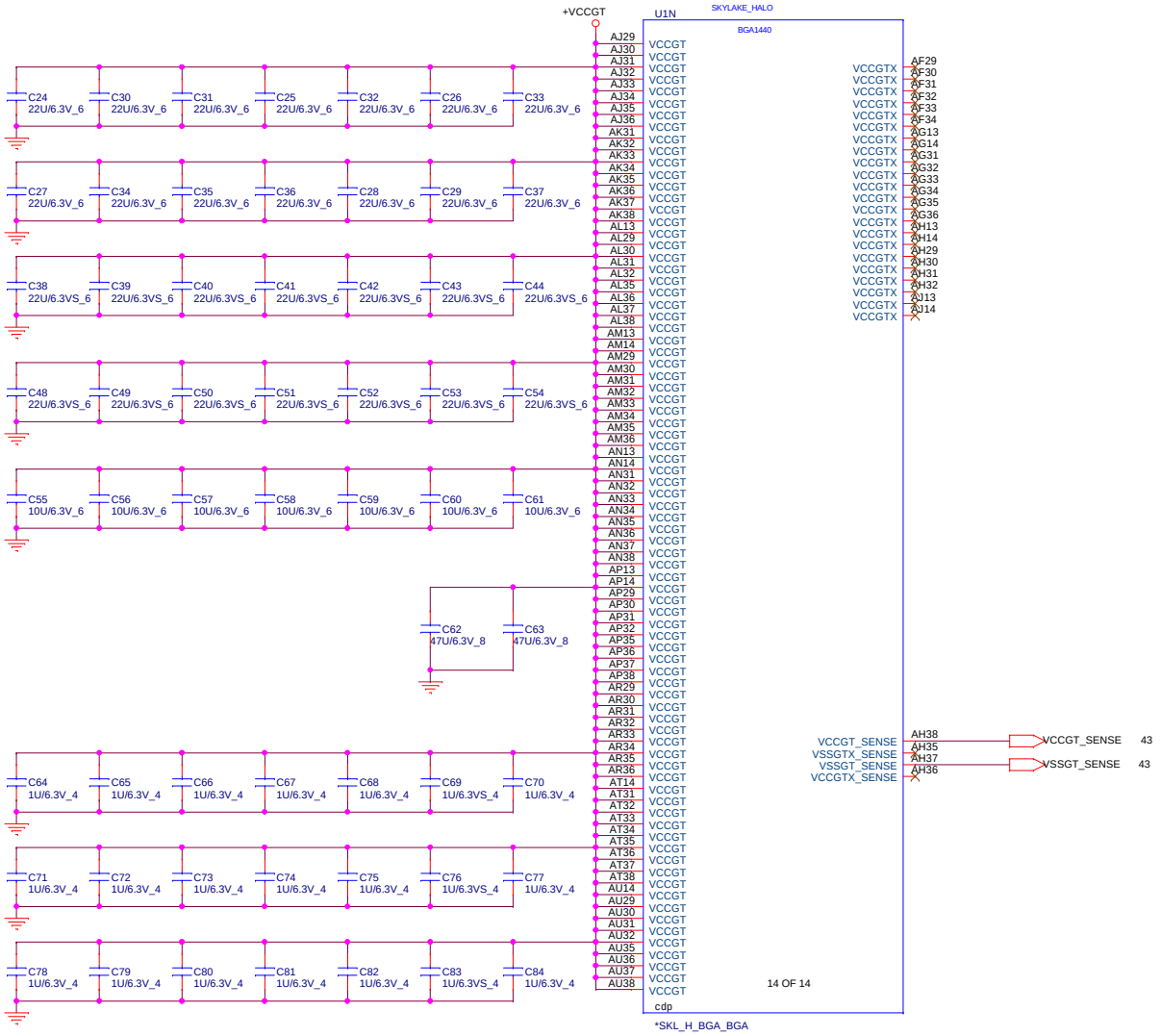


PROJECT : G35		
Quanta Computer Inc.		
Size: Custom	Document Number: 04 -- SKL 3/7 (DDR4 I/F)	Rev: 1A
Date: Tuesday, June 07, 2016	Sheet 4 of 52	

SKYLAKE Processor (POWER)

05

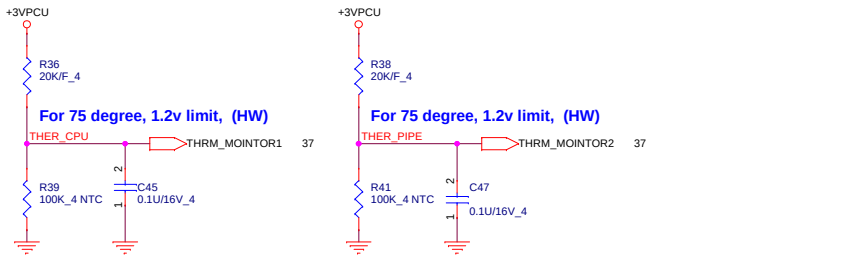
Follow SKL H EDS page 133 to 45W(GT2): +VCCGT=55A



+VCC_CORE 7,43,44
+1.2VSUS 2,6,10,17,18,42,48,51

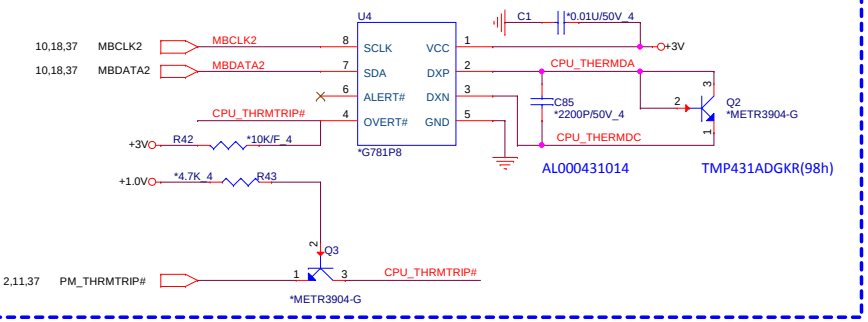
IO Thrm Protect

Location need thermal confirm



CPU Thermal Sensor

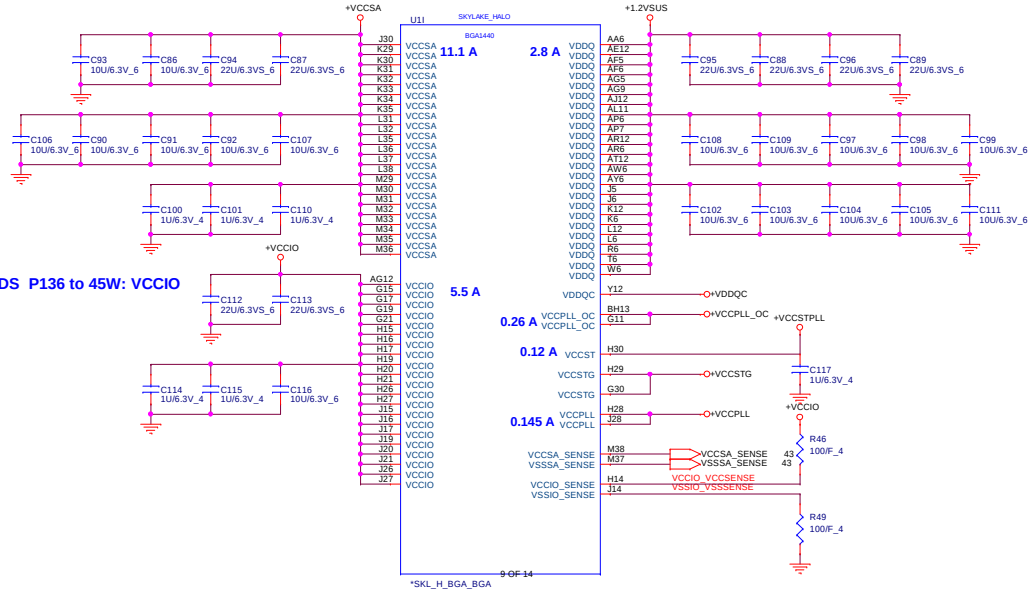
Location need thermal confirm



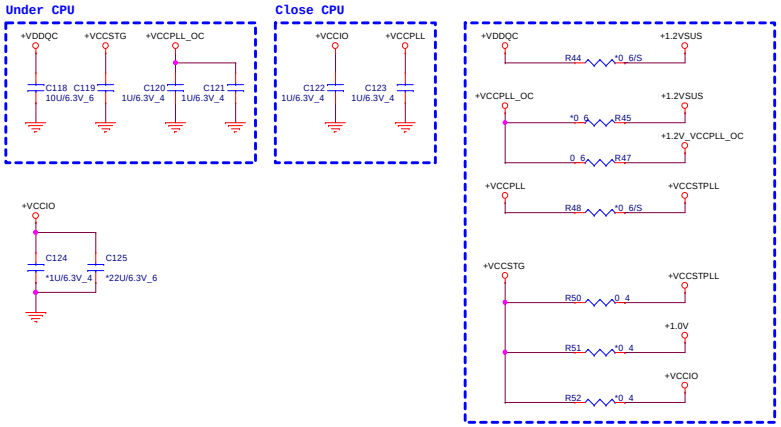
PROJECT : G35			
Quanta Computer Inc.			
Size: Custom	Document Number: 05 -- SKL 4/7 (POWER)		Rev: 1A
Date: Tuesday, June 07, 2016	Sheet 5 of 52		

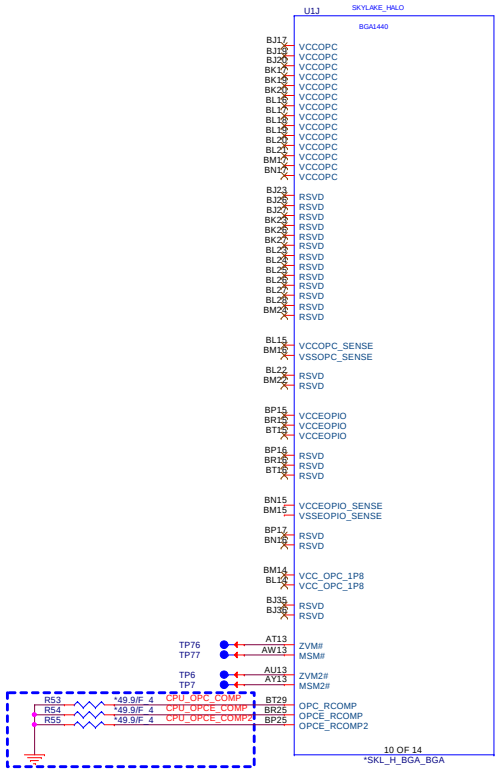
Follow SKL H EDS page 135 to 45W(GT2): VCCSA=11.1A

Follow SKL H EDS page 135 45W: VDDQ=2.8A



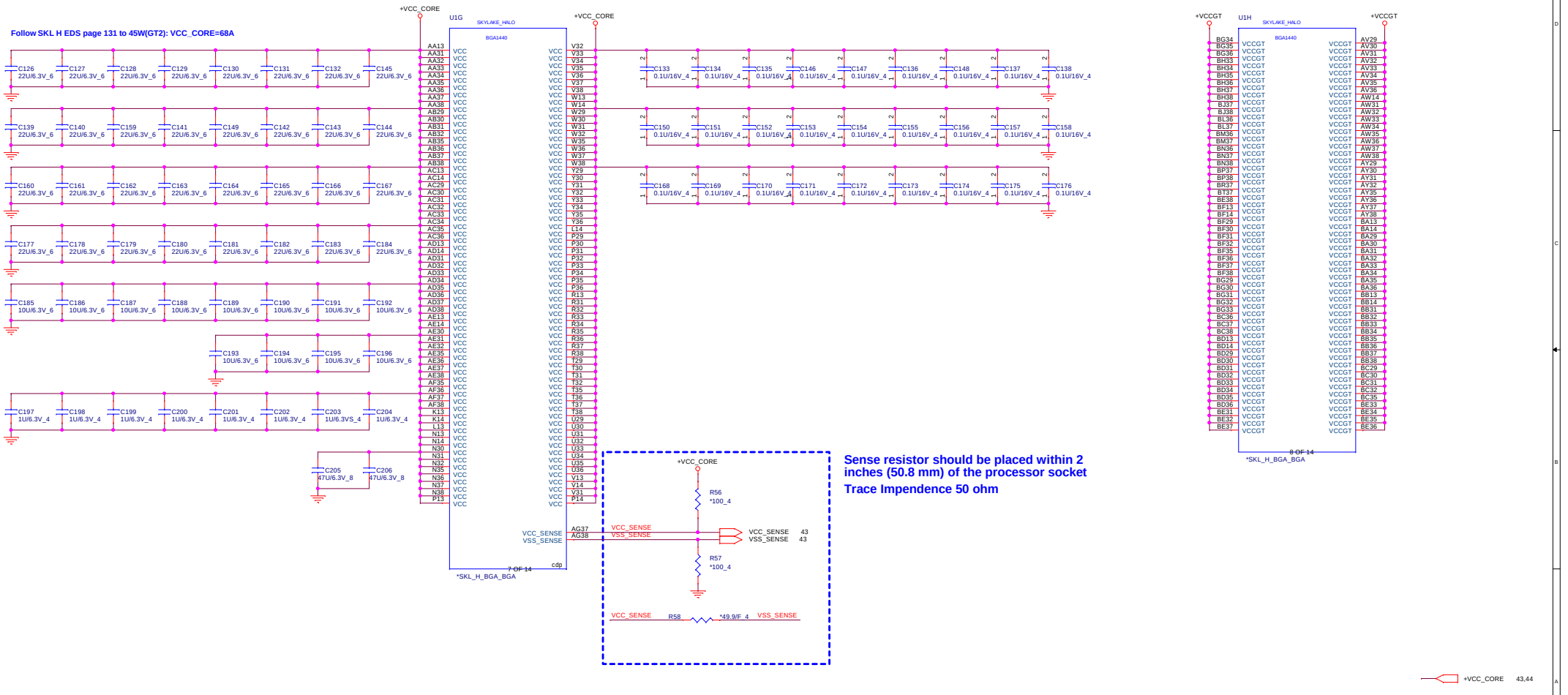
Follow SKL H EDS P136 to 45W: VCCIO
+VCCIO = 0.95V





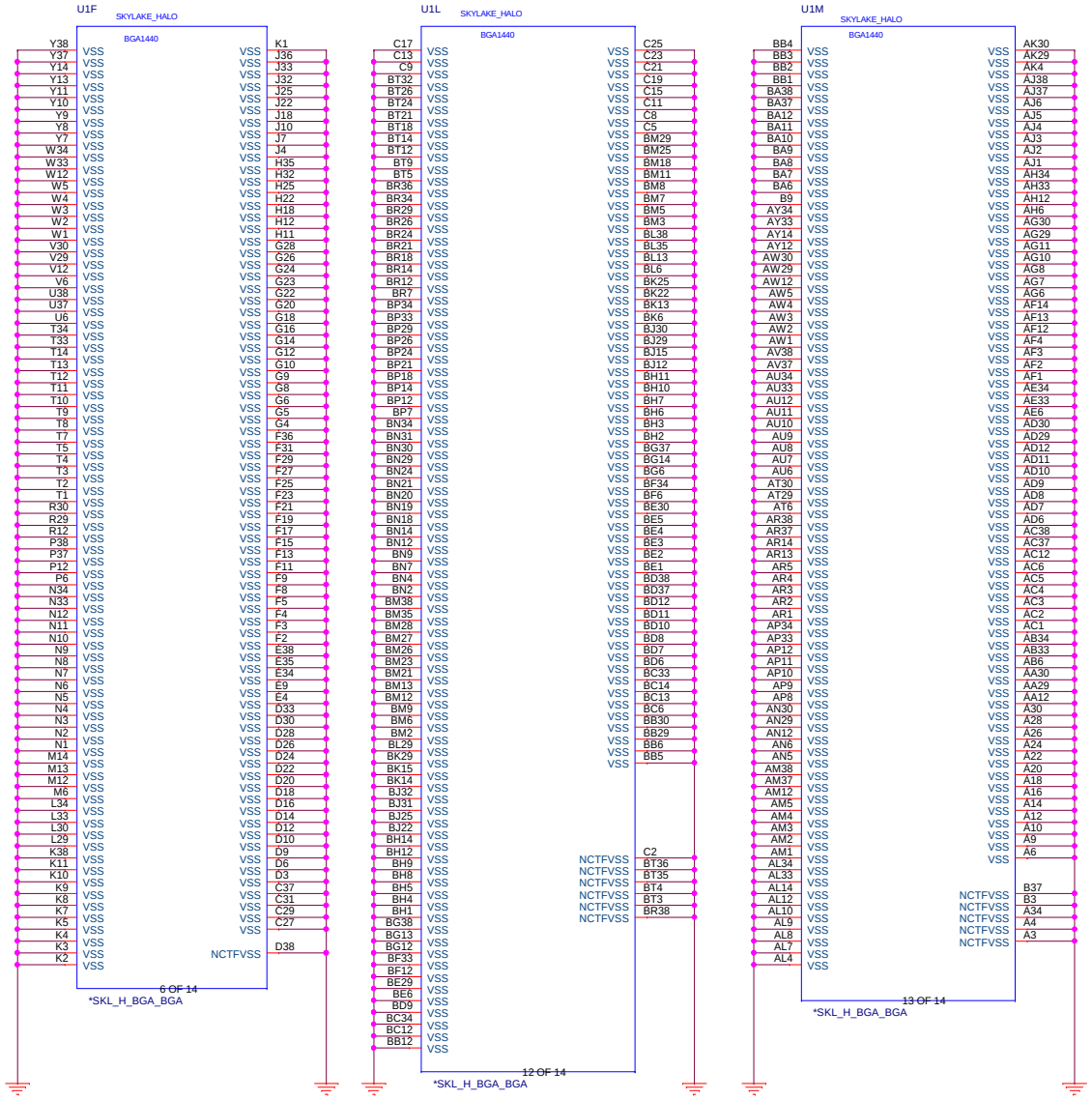
Unconnected for Processors without OPC.

PROJECT : G35 Quanta Computer Inc.			
Size: Custom	Document Number: 06 – SKL 5/7 (POWER&GND)		Rev: 1A
Date: Tuesday, June 07, 2016	Sheet 6 of 52		

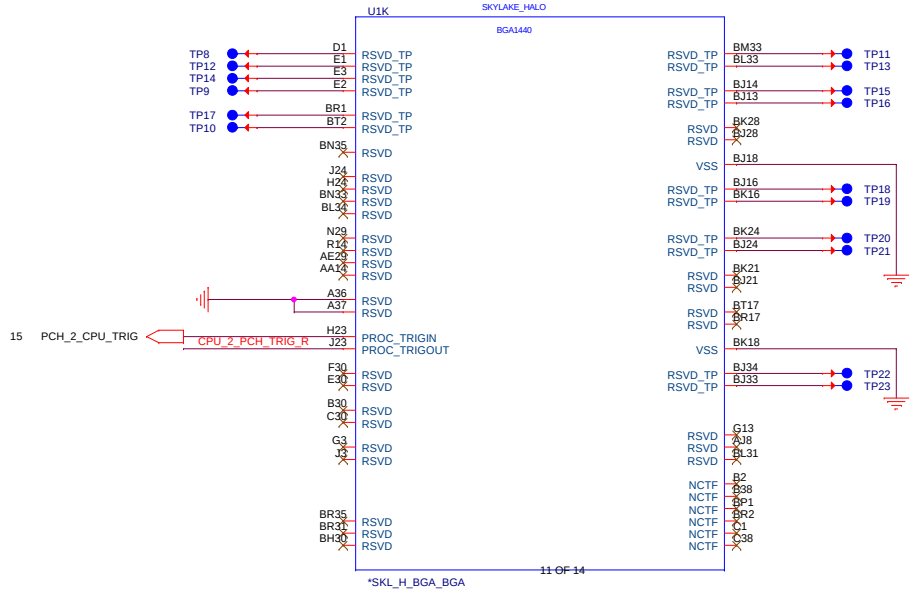


PROJECT : G35 Quanta Computer Inc.			
Size: Custom	Document Number: 07 -- SKL 6/7 (POWER&GND)		Rev: 1A
Date: Tuesday, June 07, 2016	Sheet 7 of 52		

SKL-HProcessor (GND)



SKL-H Processor (RESERVED, CFG)



Processor Strapping

The CFG signals have a default value of '1' if not terminated on the board.

0 Enable; SET DFX ENABLED BIT IN DEBUG

1 , Disable;

2,16 CFG3 — CFG3 R60 *1K_4

2,16 CFG2 — CFG2 R61 *1K_4

2,16 CFG4 — CFG4 R62 1K_4

2,16 CFG5 — CFG5 R63 *1K_4

2,16 CFG6 — CFG6 R64 *1K_4

2,16 CFG10 — CFG10 R65 *1K_4

2,16 CFG12 — CFG12 R66 *1K_4

2,16 CFG13 — CFG13 R67 *1K_4

PROJECT : G35

Quanta Computer Inc.

Size	Document Number	Rev
Custom	08 -- SKL 7/7 (GND)	1A

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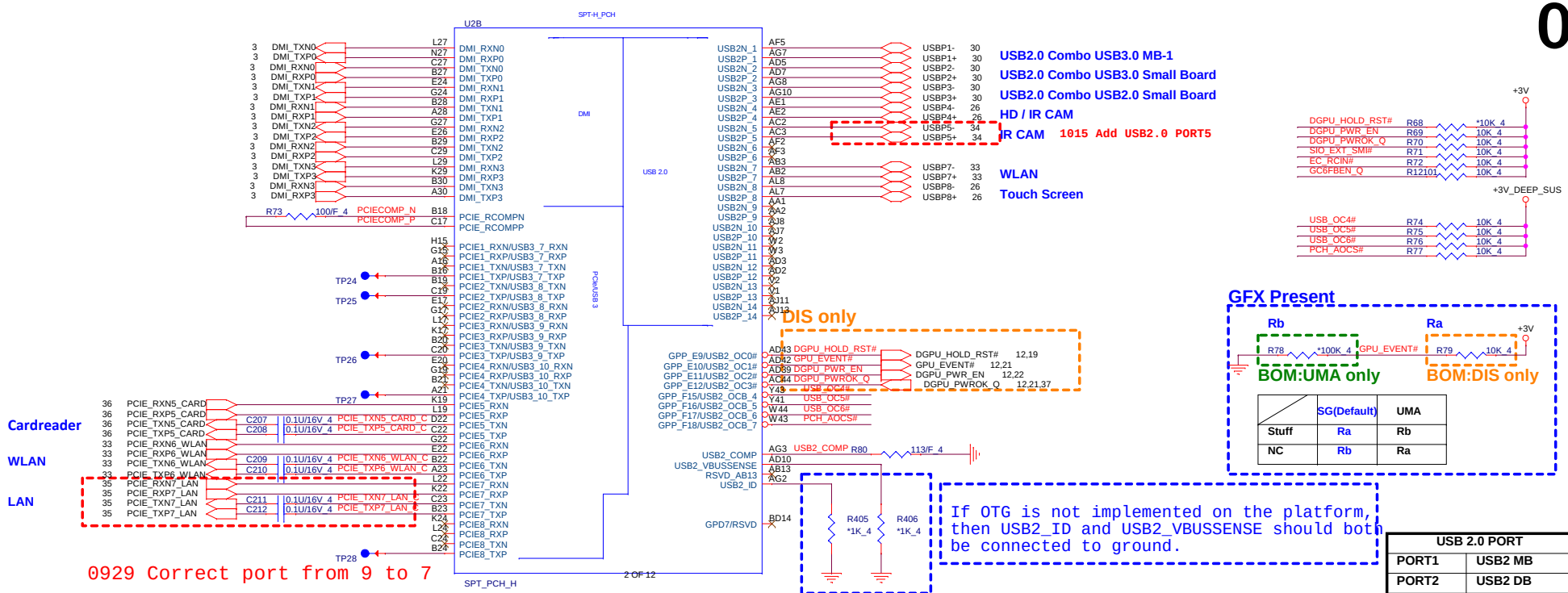
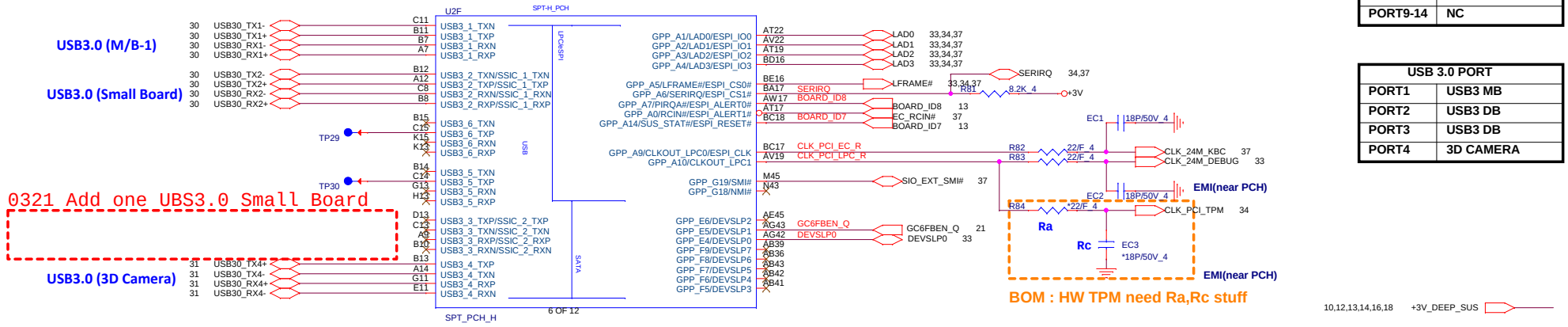


USB 2.0 PORT	
PORT1	USB2 MB
PORT2	USB2 DB
PORT3	USB2 DB
PORT4	HD/IR CAM Option
PORT5	IR CAM Option
PORT6	NC
PORT7	WLAN
PORT8	TOUCH
PORT9-14	NC

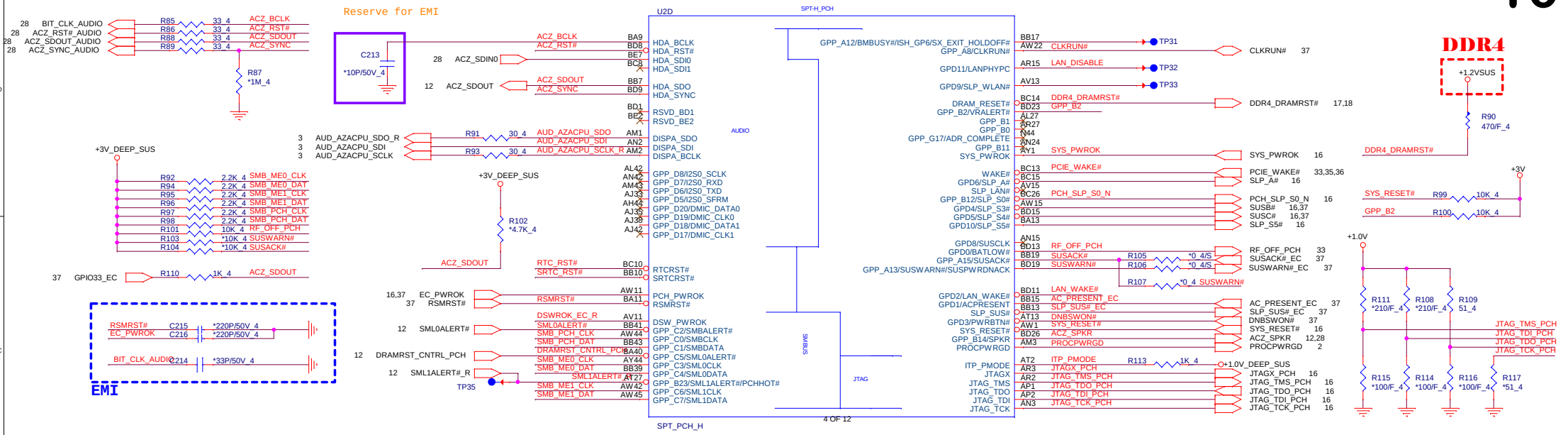
USB 3.0 PORT	
PORT1	USB3 MB
PORT2	USB3 DB
PORT3	USB3 DB
PORT4	3D CAMERA

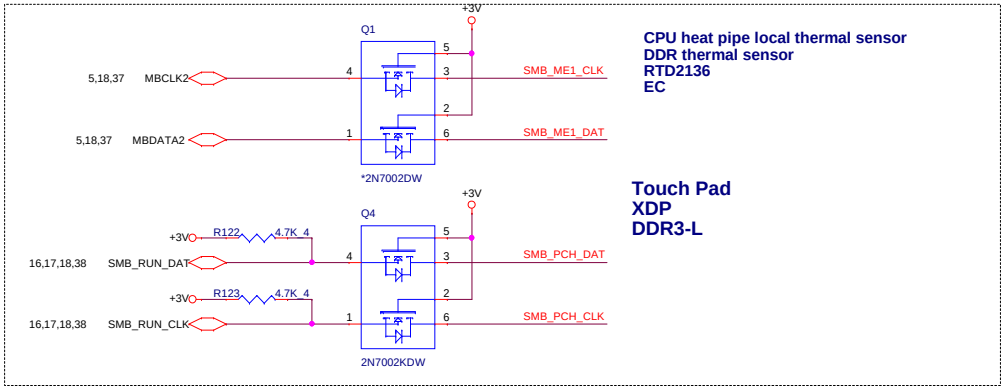


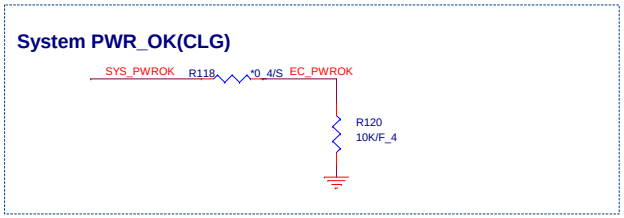
PROJECT : G35
Quanta Computer Inc.

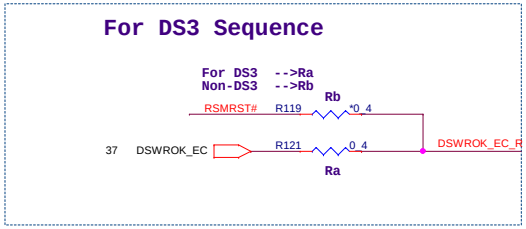
Size	Document Number	Rev
Custom	09 -- PCH 1/7 (DMI/USB/PCIE)	1A
Date: Tuesday, June 07, 2016	Sheet 9 of 52	

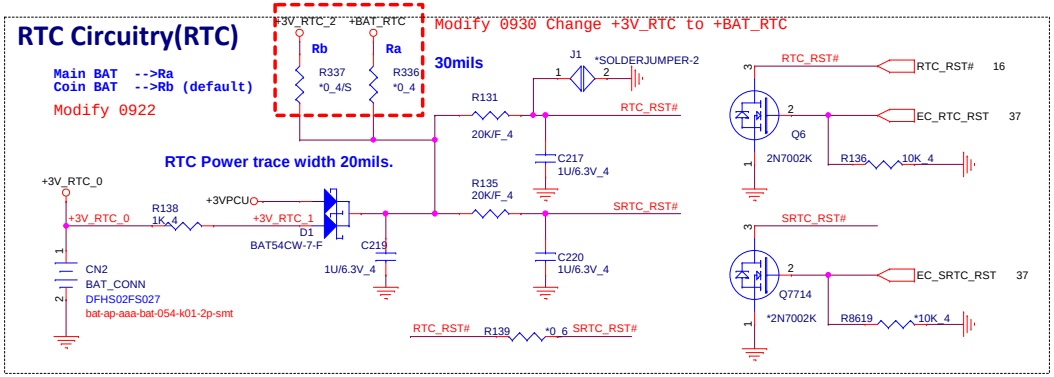
HDA Bus(CLG)

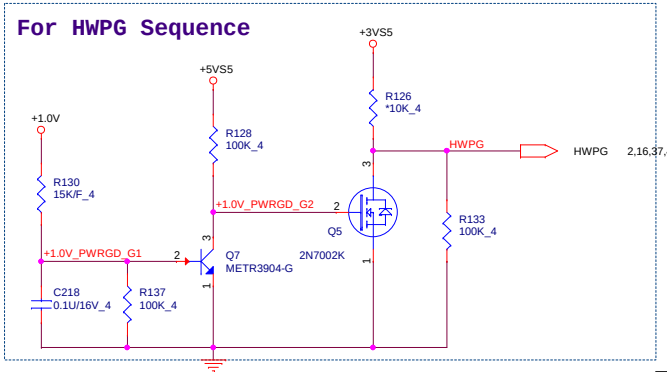


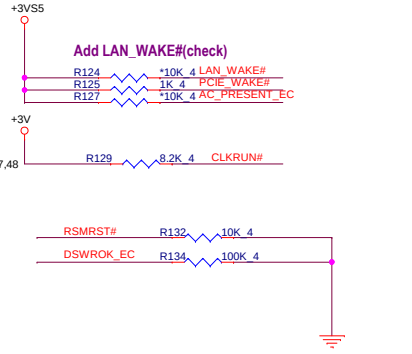












PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	10 -- PCH 2/7 (HDA/SMBUS)	1A
Date: Tuesday, June 07, 2016	Sheet 10 of 52	

HSIO MUX PORT	
PCIE1-4	NC
PCIE5	Cardreader
PCIE6	Wlan
PCIE7	Lan
PCIE8	NC
PCIE9/SATA0A	SSD PCIE * 4
PCIE10	
PCIE11	
PCIE12	
PCIE13	NC
PCIE14	NC
PCIE15	HDD
PCIE16	NC
PCIE17	NC
PCIE18-20	NC

SSD PCIE x4 LANE

SSD PCIE x4 LANE

ODD (SATA2 3.0Gb/s)

HDD2 (SATA3 6Gb/s)

Modify 1005 Change HDD SATA Port2 to port1B

HDD1 (SATA1B 6Gb/s)

SSD PCIE x4 LANE

GPIO35:
SSD SATA IF => High
SSD PCIE IF => Low

For SSD Det (SATA0A)

1002 add

BOM:SSD only

The 24 MHz (50 Ohm ESR) XTAL used for Skylake-H
needs to be replaced by 38.4 MHz (30 Ohm ESR) XTAL for Cannonlake-H.

1123 Change Y1 P/N from 16pF to 20pF

Crystal Components with Surrounding 10 mil Wide GND Shield Trace
Break Out:4-10 mil Wide GND Shield Trace

Card Reader

WLAN

LAN

VGA

SSD

BOM:DIS only

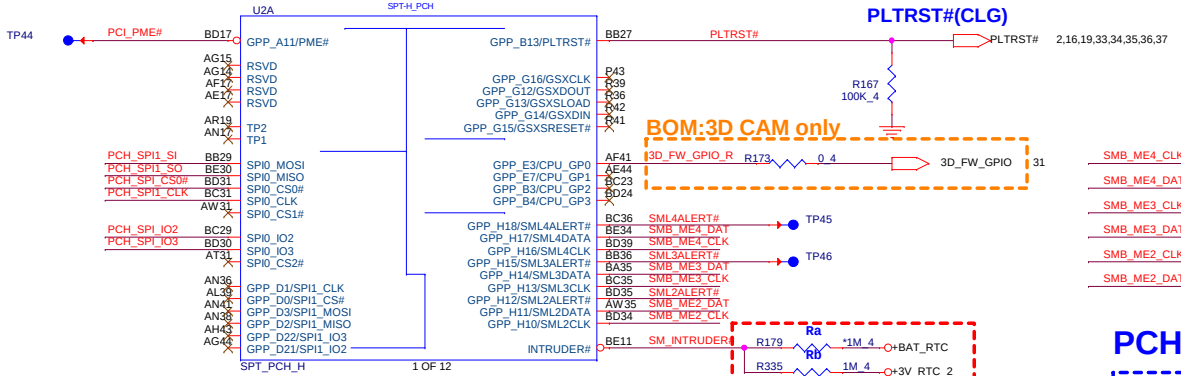
BOM:SSD only

RTC Clock 32.768KHz

32.768KHz
BG332768453 CRYSTAL SMD 32.768KHZ(+-20PPM,12.5PF)
footprint: xtl-3_2X1_5-2_5-0_8h

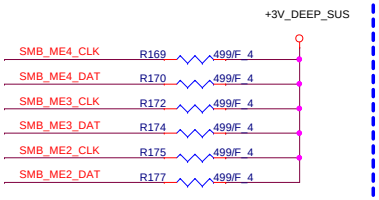
PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	11 – PCH 3/7 (SATA/LPC/CLK)	1A
Date: Tuesday, June 07, 2016	Sheet 11 of 52	



support HW TPM -->Ra
support SW TPM -->Rb (default)

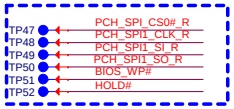
Modify 0930 Change +3V_RTC to +BAT_RTC



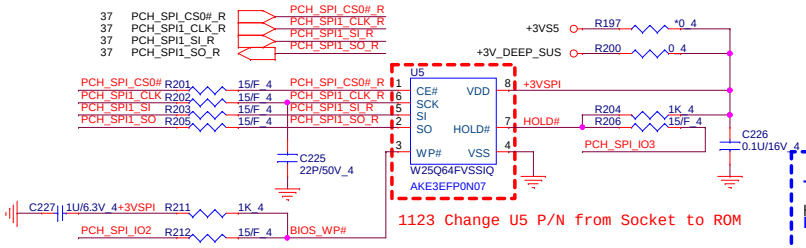
PLTRST#(CLG)

PCH Strap Pin

PCH SPI ROM(CLG)



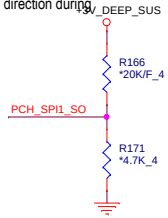
Place to TOP



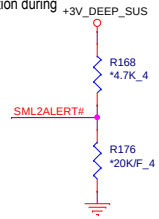
1123 Change U5 P/N from Socket to ROM

Vender	Size	P/N
EON	8MB	AKE3EZN0Q01 (EN25QH64-104HIP)
Winbond	8MB	AKE3EFP0N07 (W25Q64FVSSIQ)
GigaDevice	8MB	AKE3EGN0Q01 (GD25B64BSIGR)
Socket		DFHS08FS023

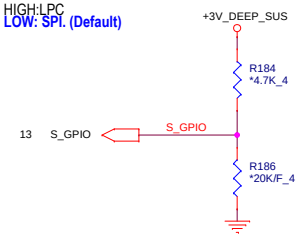
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



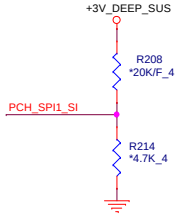
ESPI FLASH SHARING MODE
HIGH:SLAVE ATTACEHD FLASH SHARING
LOW: 0: MASTER ATTACHED FLASH SHARING
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



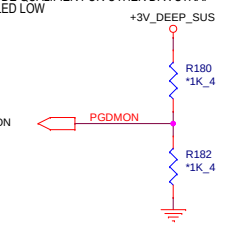
BOOT SELECT STRAP
HIGH:LPC
LOW: SPI. (Default)



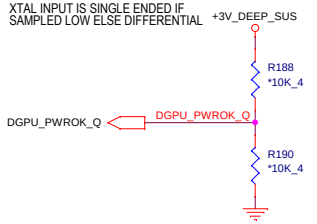
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



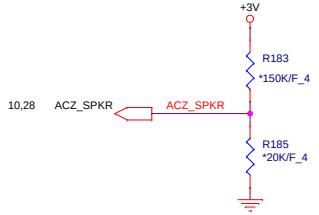
DFX TEST MODE QUALIFIER FOR OTHER DFX STRAP WHEN SAMPLED LOW



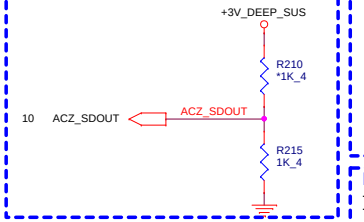
DFX TEST MODE
XTAL INPUT IS SINGLE ENDED IF SAMPLED LOW ELSE DIFFERENTIAL



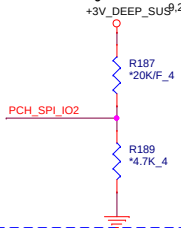
TOP SWAP OVERRIDE STRAP
HIGH:TOP SWAP ENABLED (CRB)
LOW:TOP SWAP DISABLED(DEFAULT)



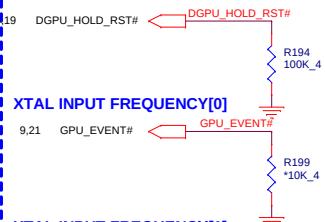
TLS CONFIDENTIALITY ENABLED
HIGH: Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.(CRB)
LOW: security measures defined in the Flash Descriptor. (Default)



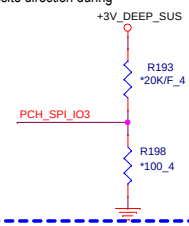
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



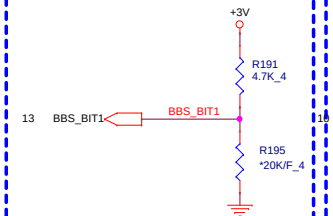
RING OSCILLATOR BYPASS



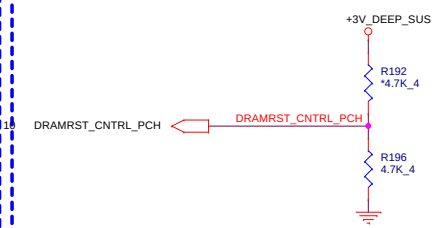
RESERVED
This strap should sample HIGH.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



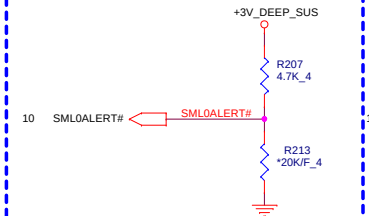
NO REBOOT IF SAMPLED HIGH
HIGH:TOP SWAP ENABLED (CRB)
LOW: Disable "No Reboot" mode. (Default)



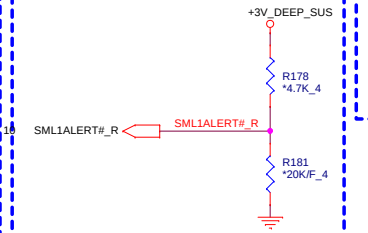
ESPI/LPC SELECT STRAP
HIGH:eSPI Is selected for EC
LOW: LPC Is selected for EC. (Default)



TLS CONFIDENTIALITY ENABLED
HIGH:T Enable Intel ME Crypto Transport Layer Security (TLS) cipher suite (with confidentiality). (CRB)
LOW: Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality). (Default)



RESERVED
This strap should sample LOW.
There should NOT be any on-board device driving it to opposite direction during strap sampling.



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Custom	12 -- PCH 4/7 (GPIO/MISC)	1A
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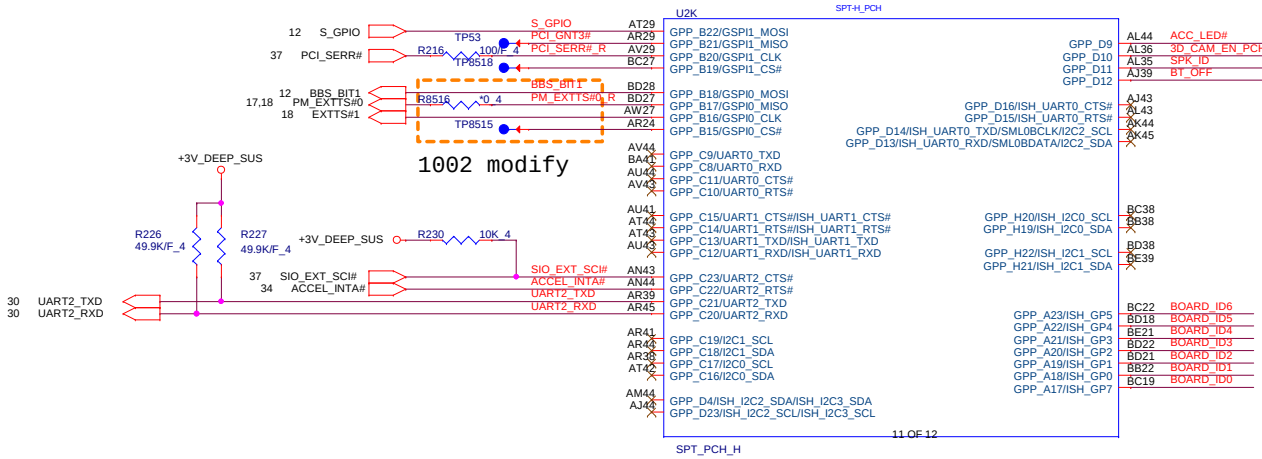
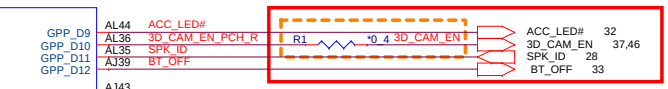
9,10,12,14,16,18 +3V_DEEP_SUS

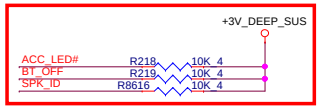
3D CAMERA
BOM: 3D CAM Un-Stuff

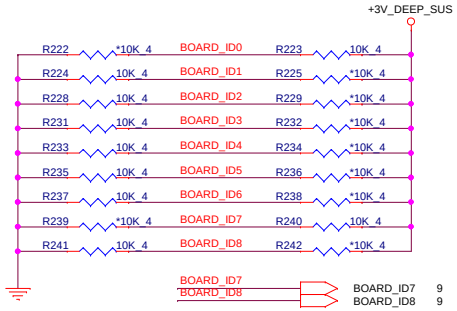
1124 Add SPK_ID for Smart amp feature

1002 modify

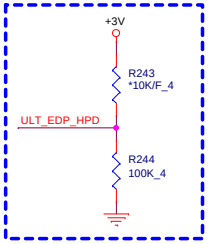






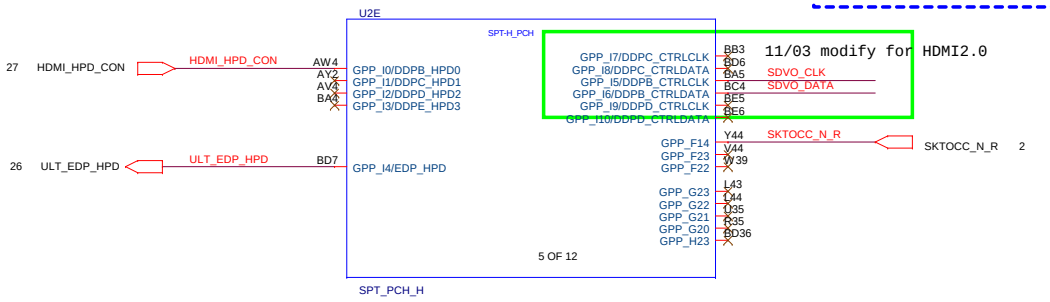


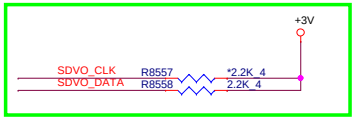
Reserve EDP_HPD opposites circuit!



Model	BOARD_ID[8:7] ID8;ID7	BOARD_ID[6:5] ID6;ID5	Board ID [4:3] ID4;ID3		BOARD_ID[2:1] ID2;ID1	BOARD_ID0 ID0
Definition	01 SKL H 10 KBL H *RSV	00 Reserve	ID4 Reserve	ID3 0 Nvidia 1 AMD	00 15" 01 17" 10 17" SP	0 : UMA 1 : DIS

This signal has a weak internal pull-down.
0 = Port C and D is not detected.
1 = Port C and D is detected.





11/03 modify for HDMI2.0

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	13 -- PCH 5/7 (GPIO)	1A
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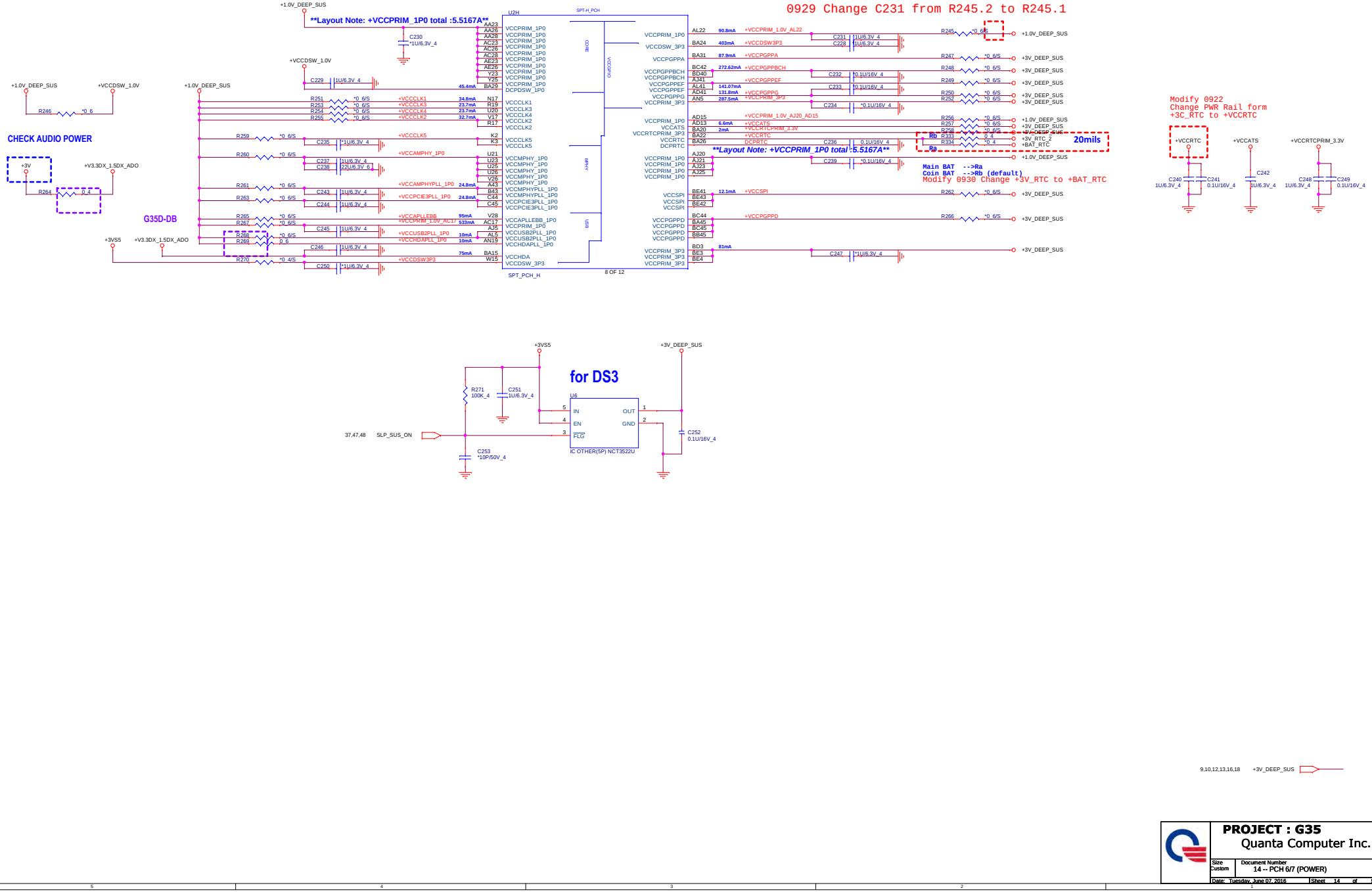

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Size: Custom	Document Number: 14 -- PCH 6/7 (POWER)
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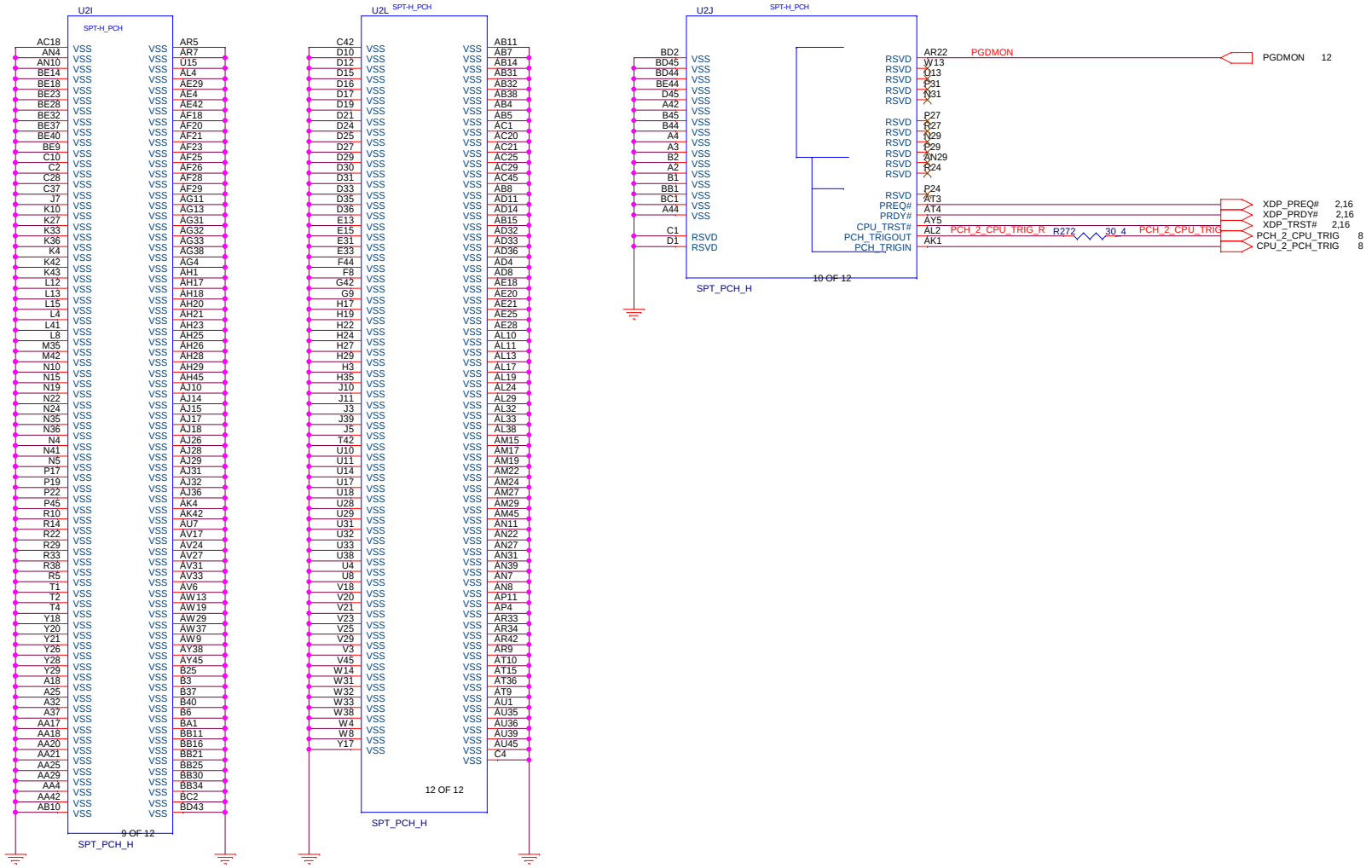
Date: Tuesday, June 07, 2016	Sheet 14 of 52



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Quanta Computer Inc.		
Size: Custom	Document Number: 15 -- PCH 7/7 (GND)	Rev: 1A
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+3VS5 10,12,14,33,37,41,42,46,47,48
+3V_DEEP_SUS 9,10,12,13,14,18
+3V 5,9,10,11,12,13,14,17,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51
+1.0V_DEEP_SUS 10,11,14,47,48
+VCCIO 3,6,48
+1.0V 2,5,6,10,37,48

CPU XDP

CN3 — *Samtec BSH-030-01

2,15	XDP_PREQ#	3	OBSFN_A0	VCC_OBS_CD	44
2,15	XDP_PRDY#	5	OBSFN_A1	VCC_OBS_AB	43
2	CFG0	9	OBSDATA_A0	OBSFN_B0	21
2	CFG1	11	OBSDATA_A1	OBSFN_B1	23
2,8	CFG2	15	OBSDATA_A2	OBSFN_C0	4
2,8	CFG3	17	OBSDATA_A3	OBSFN_C1	6
2,8	CFG4	27	OBSDATA_B0	OBSDATA_C0	10
2,8	CFG5	29	OBSDATA_B1	OBSDATA_C1	12
2,8	CFG6	33	OBSDATA_B2	OBSDATA_C2	16
2	CFG7	35	OBSDATA_B3	OBSDATA_C3	18
16	ON/OFFBTN_KBC#	41	HOOK1	OBSFN_D0	22
		45	HOOK2	OBSFN_D1	24
11	CK_XDP_P	40	ITPCLK/HOOK4	OBSDATA_D0	28
11	CK_XDP_N	42	ITPCLK#/HOOK5	OBSDATA_D1	30
		48	DBR#/HOOK7	OBSDATA_D2	34
10,17,18,38	SMB_RUN_DAT	51	SDA	OBSDATA_D3	36
10,17,18,38	SMB_RUN_CLK	53	SCL	HOOK3	47
		52	TDO	TCK1	55
		54	TRSTN	PWRGOOD/HOOK0	39
		56	TDI	RESET#/HOOK6	46
		58	TMS	GND0	1
		57	TCK0	GND1	2
		60	GND17	GND2	7
		59	GND16	GND3	8
		50	GND15	GND4	13
		49	GND14	GND5	14
		38	GND13	GND6	19
		37	GND12	GND7	20
		32	GND11	GND8	25
		31	GND10	GND9	26

R273 *1K_4 — R274 *1K_4 — CFG0 R275 *1K_4 PWR_DEBUG — R276 *0_4 SMB_RUN_DAT_XDP — R277 *0_4 SMB_RUN_CLK_XDP

XDP_DBRESET_N
XDP_TDO
XDP_TRST#
XDP_TDI
XDP_TMS
XDP_TCK0

TP58 — TP56 — TP57

XDP_BPM0 2
XDP_BPM1 2
CFG17 2
CFG16 2
CFG8 2
CFG9 2
CFG10 2,8
CFG11 2
CFG19 2
CFG18 2
CFG12 2,8
CFG13 2,8
CFG14 2
CFG15 2
EC_PWROK 10,37

XDP_TCK1
SYS_PWROK
XDP_RST — R278 *1K_4

SYS_PWROK 10,16
PLTRST# 2,12,16,19,33,34,35,36,37

+1.0V_DEEP_SUS

XDP_DBRESET_N — R279 *1K_4 — +3V — C254 *0.1U/16V_4

SYS_PWROK — R280 *1K_4 — +3V_DEEP_SUS — C257 *0.1U/16V_4

+1.0V_DEEP_SUS — C255 *0.1U/16V_4 — C256 *0.1U/16V_4

+VCCIO — R281 150/F_4 — PWR_DEBUG — R282 *10K_4

APS

CN1 — *ACES_88511-180N

+3V_DEEP_SUS
+3VS5

1		
2		
3	SUSB#	10,16,37
4		
5	SLP_S5#	10
6	SUSC#	10,37
7	SLP_A#	10
8		
9	RTC_RST#	10
10		
11	ON/OFFBTN_KBC#	16
12		
13	SYS_RESET#	10
14		
15	PCH_SLP_S0_N	10
16		
17		
18	SUSB#	10,16,37

R283 *0_4

+3V — C258 *0.1U/16V_4

U7 — *SN74CBTLV3126RGYR

+1.0V — R284 *51_4 — XDP_TDO

		14	VCC		
		2	1A	1B	3
2,10,37,41,42,47,48	HWPG	1	1OE		
TP59	XDP_TDI	5	2A	2B	6
		4	2OE		
TP60	XDP_TMS	9	3A	3B	8
		10	3OE		
2,15	XDP_TRST#	12	4A	4B	11
	XDP_TRST#	13	4OE		
			DPAD		15
			GND		7

XDP_TDO_CPU 2
XDP_TDI_CPU 2
XDP_TMS_CPU 2
XDP_TRST#_CPU 2

10,16	SYS_PWROK		SYS_PWROK
2,12,16,19,33,34,35,36,37	PLTRST#	R340 *1K_4	XDP_RST
	+1.0V		
		R347 *51_4	
		R345 *0_4	XDP_TDO
10	JTAGX_PCH		XDP_TCK0
10	JTAG_TMS_PCH		XDP_TMS
10	JTAG_TDI_PCH		XDP_TDI
10	JTAG_TDO_PCH		XDP_TDO
		R342 *0_4	XDP_TDI
		R344 *0_4	XDP_TCK0
10	JTAG_TCK_PCH		XDP_TCK1

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	16 -- XDP & APS	1A
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JDIM1A

DDR4 SODIMM 260 PIN (260P)

1002 modify

0104 Update footprint

Place these Caps near So-Dimm0.

0923 Del C286 C287

JDIM1B

2.48A

DDR4 SODIMM 260 PIN (260P)

0104 Update footprint

Place these Caps near So-Dimm0.

1uF/10uF 4pcs on each side of connector

+1.2VSUS 2,6,10,18,42,48,51

+3V 5,9,10,11,12,13,14,16,18,22,26,27,28,29,30,32,33,34,35,36,37,38,43,46,50,51

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Size: Custom	Document Number: 17 -- DDR4 DIMM0-STD(4.0H)
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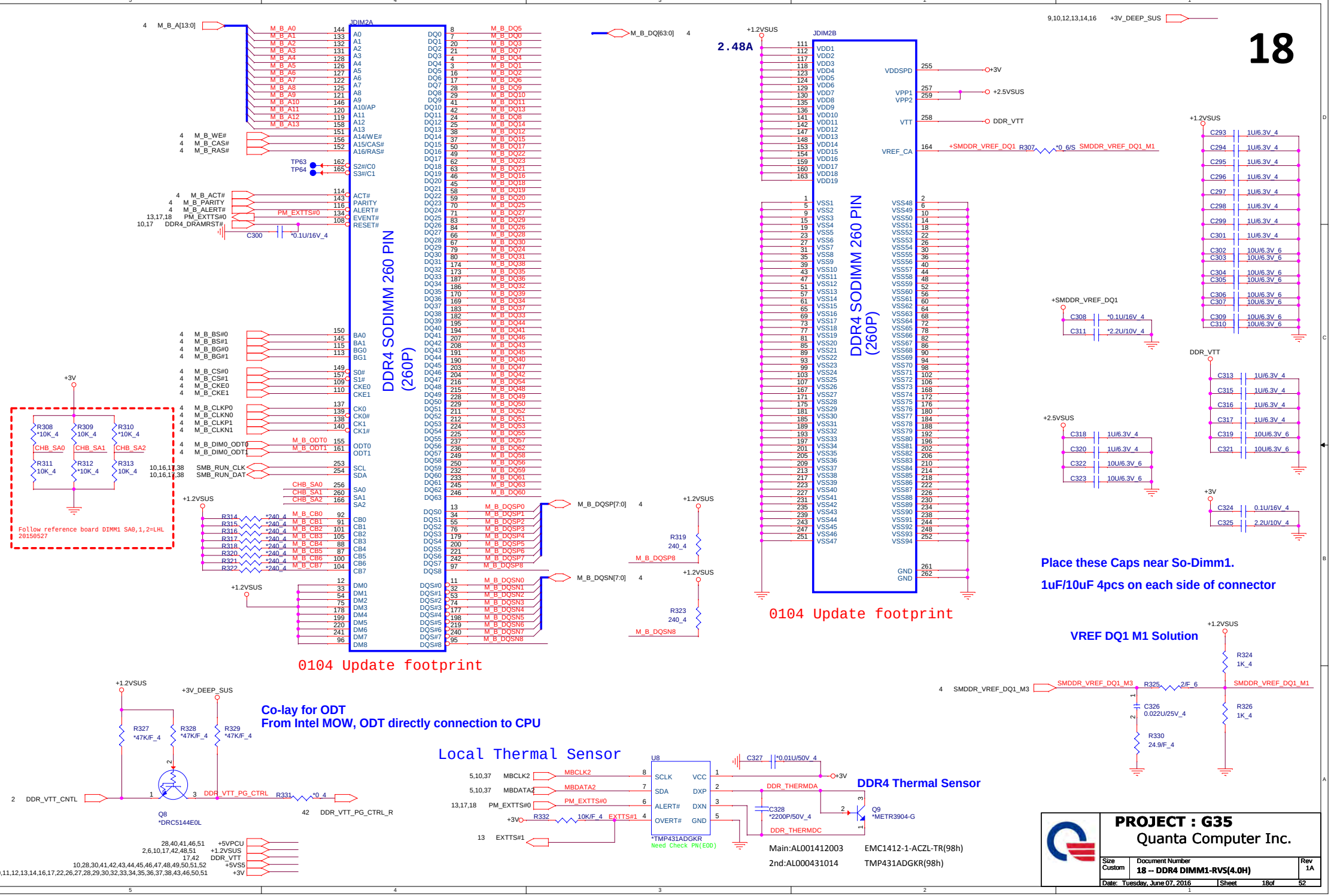
JDIM2A
DDR4 SODIMM 260 PIN (260P)
JDIM2B
DDR4 SODIMM 260 PIN (260P)
2.48A
0104 Update footprint
0104 Update footprint
Follow reference board DIMM1 SA0,1,2=LHL 20150527
Place these Caps near So-Dimm1.
1uF/10uF 4pcs on each side of connector
VREF DQ1 M1 Solution
Co-lay for ODT
From Intel MOW, ODT directly connection to CPU
Local Thermal Sensor
DDR4 Thermal Sensor
*TMP431ADGKR
Need Check PN(EOD)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)
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Quanta Computer Inc.
Size Custom
Document Number 18 -- DDR4 DIMM1-RVS(4.0H)
Rev 1A
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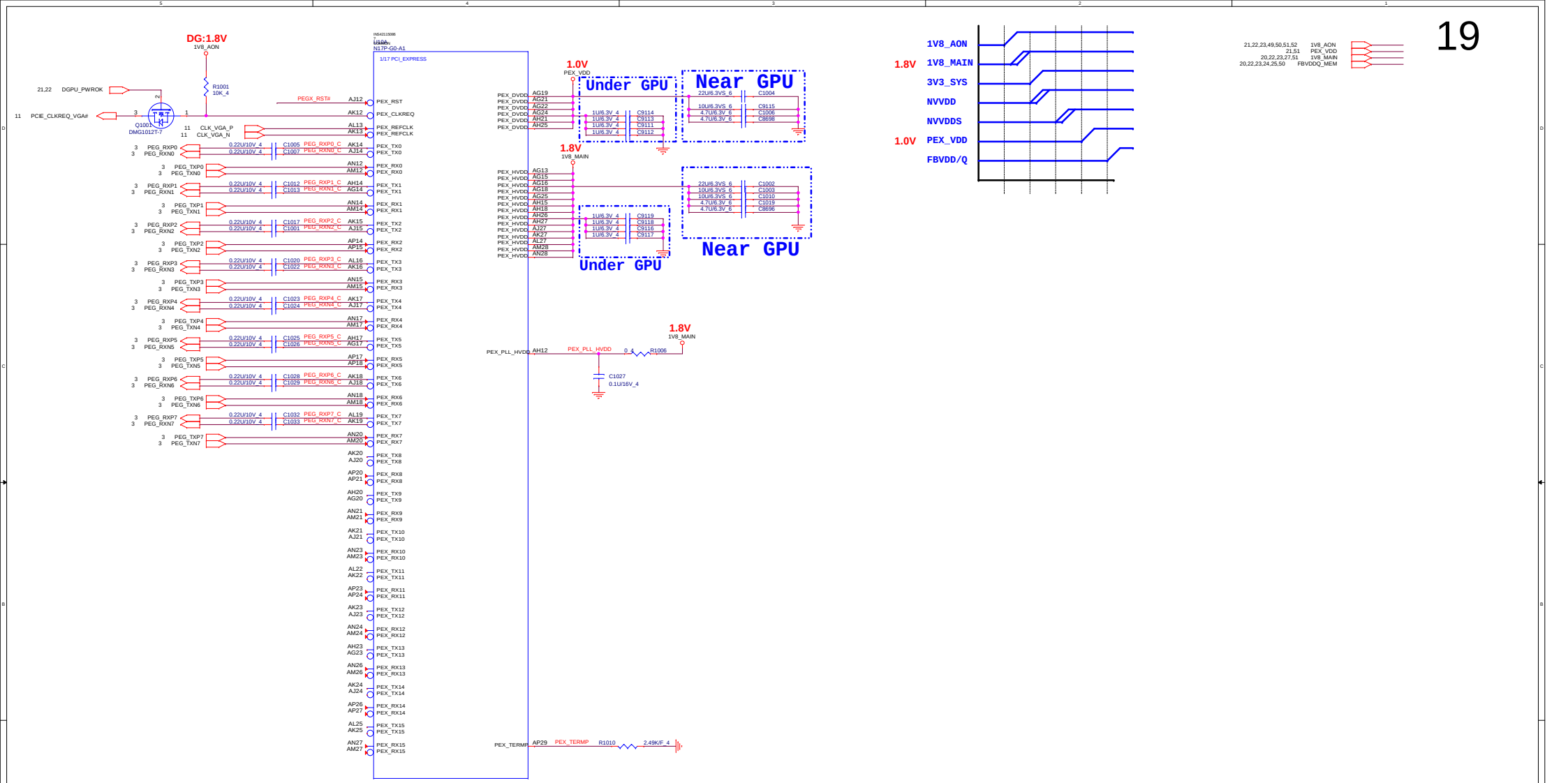

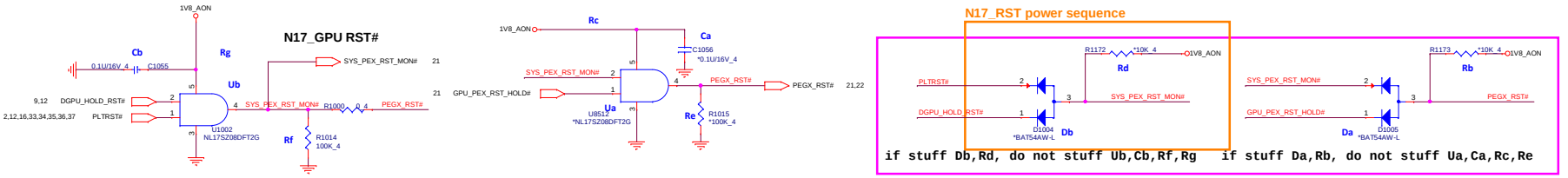

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	N17P-G0-A1-1/9	1A
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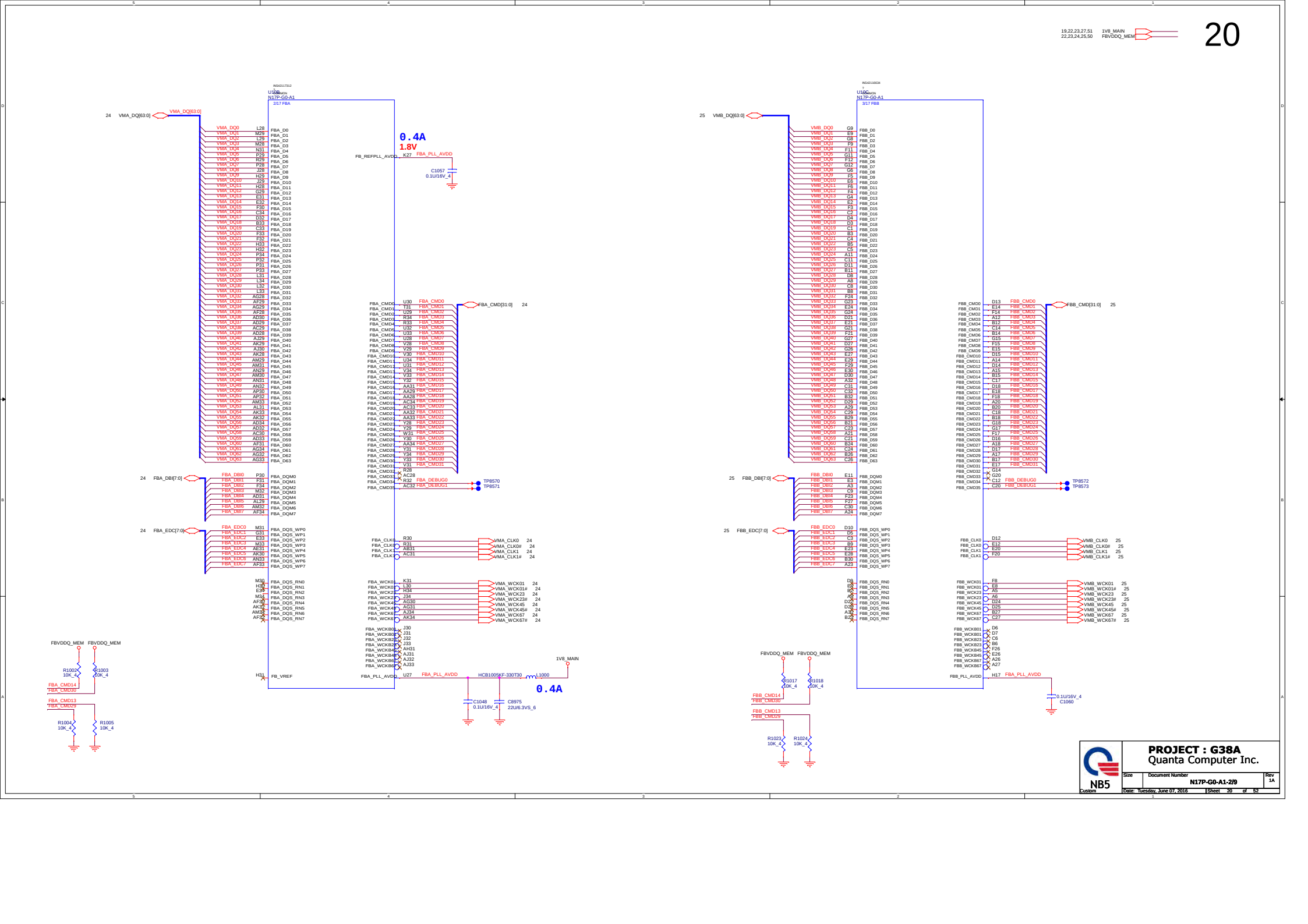

NB5 Custom	PROJECT : G38A Quanta Computer Inc.		
	Size	Document Number	Rev 1A
		N17P-G0-A1-2/9	
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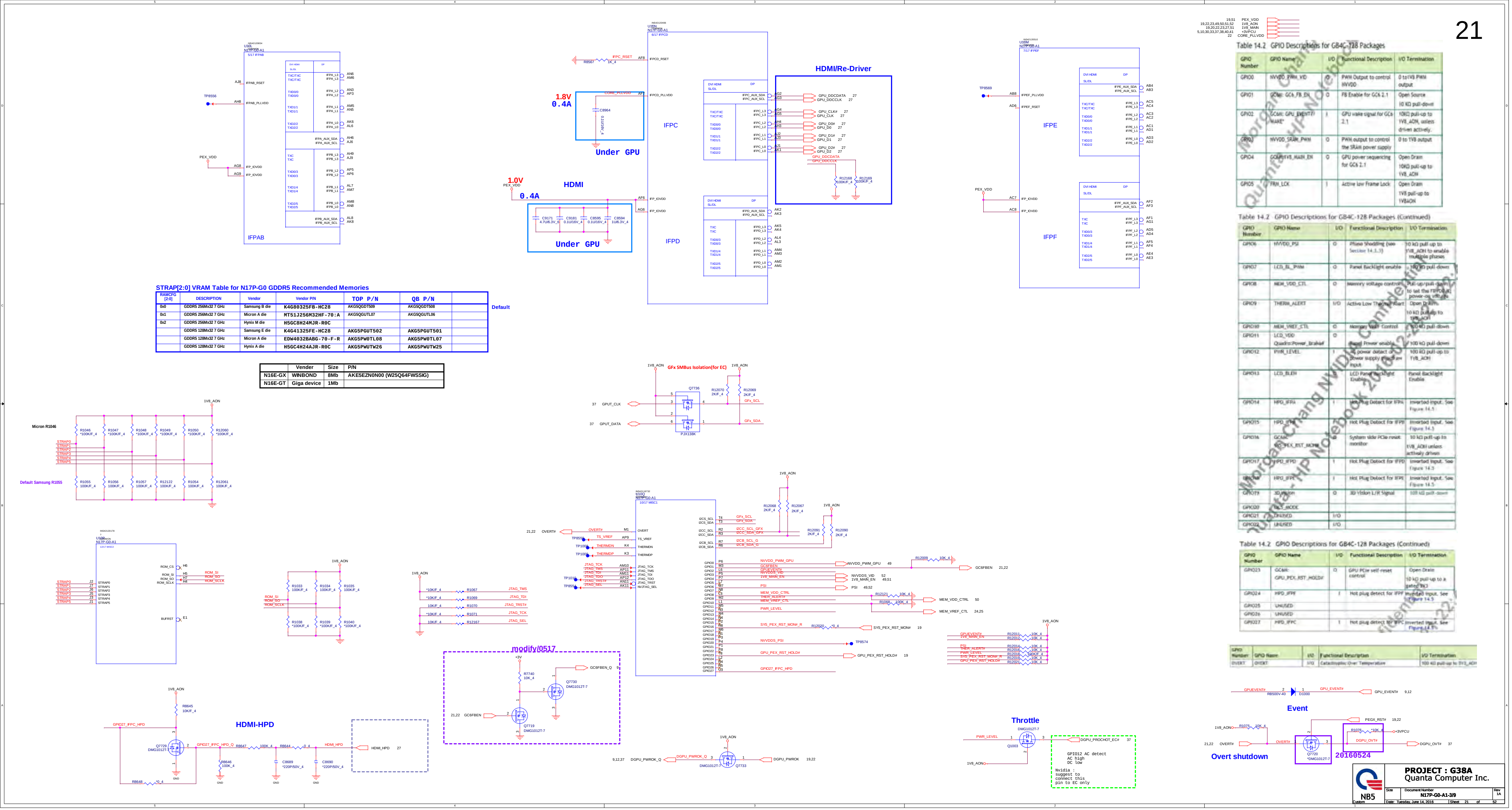

STRAP[2:0] VRAM Table for N17P-G0 GDDR5 Recommended Memories

RAMCFG [2:0]	DESCRIPTION	Vendor	Vendor P/N	TOP P/N	QB P/N	
0x0	GDDR5 256Mx32 7 GHz	Samsung B die	K4G80325FB-HC28	AKG5QGDT509	AKG5QGDT508	
0x1	GDDR5 256Mx32 7 GHz	Micron A die	MT51J256M32HF-70:A	AKG5QGUTL07	AKG5QGUTL06	
0x2	GDDR5 256Mx32 7 GHz	Hynix M die	H5GC8H24MJR-R0C			
	GDDR5 128Mx32 7 GHz	Samsung E die	K4G41325FE-HC28	AKG5PGUT502	AKG5PGUT501	
	GDDR5 128Mx32 7 GHz	Micron A die	EDW4032BABG-70-F-R	AKG5PW0TL08	AKG5PW0TL07	
	GDDR5 128Mx32 7 GHz	Hynix A die	H5GC4H24AJR-R0C	AKG5PWUTW26	AKG5PWUTW25	

Default

	Vender	Size	P/N
N16E-GX	WINBOND	8Mb	AKE5EZN0N00 (W25Q64FWSSIG)
N16E-GT	Giga device	1Mb	

Table 14.2 GPIO Descriptions for GB4C-128 Packages

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO0	NVVDD_PWM_VID	O	PWM Output to control NVVDD	0 to1V8 PWM output
GPIO1	GC6: GC6_FB_EN	O	FB Enable for GC6 2.1	Open Source 10 KΩ pull-down
GPIO2	GC6: GPU_EVENT# / WAKE*	I	GPU wake signal for GC6 2.1	10KΩ pull-up to 1V8_AON, unless driven actively.
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	GC6: 1V8_MAIN_EN	O	GPU power sequencing for GC6 2.1	Open Drain 10KΩ pull-up to 1V8_AON
GPIO5	FRM_LCK	I	Active low Frame Lock	Open Drain 1V8 pull-up to 1V8AON

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO6	NVVDD_PSI	O	Phase Shedding (see Section 14.1.1)	10 kΩ pull-up to 1V8_AON to enable multiple phases
GPIO7	LCD_BL_PWM	O	Panel Backlight enable	100 kΩ pull-down
GPIO8	MEM_VDD_CTL	O	Memory voltage control	Pull-up/pull-down to set the FBVDD(Q) power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	Open Drain 10 kΩ pull-up to 1V8_AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100 kΩ pull-down
GPIO11	LCD_VDD Quadro:Power_Brake#	O	Panel Power enable	100 kΩ pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply [illegible] input	100 kΩ pull-up to 1V8_AON
GPIO13	LCD_BLEN	O	LCD Panel Backlight Enable	Panel Backlight Enable
GPIO14	HPD_IFPA	I	Hot Plug Detect for IFPA	Inverted input. See Figure 14.5
GPIO15	HPD_IFPB	I	Hot Plug Detect for IFPB	Inverted input. See Figure 14.5
GPIO16	GC6: SYS_PEX_RST_MON#	I	System side PCIe reset monitor	10 kΩ pull-up to 1V8_AON unless actively driven
GPIO17	HPD_IFPD	I	Hot Plug Detect for IFPD	Inverted input. See Figure 14.5
GPIO18	HPD_IFPE	I	Hot Plug Detect for IFPE	Inverted input. See Figure 14.5
GPIO19	3D_VISION	O	3D Vision L/R Signal	100 kΩ pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		

Table 14.2 GPIO Descriptions for GB4C-128 Packages (Continued)

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
GPIO23	GC6: GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	Open Drain 10 kΩ pull-up to a gated 3V3
GPIO24	HPD_IFPF	I	Hot plug detect for IFPF	Inverted input. See Figure 14.5
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_IFPC	I	Hot plug detect for IFPC	Inverted input. See Figure 14.5

GPIO Number	GPIO Name	I/O	Functional Description	I/O Termination
OVERT	OVERT	I/O	Catastrophic Over Temperature	100 kΩ pull-up to 3V3_AON

NB5

PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	N17P-G0-A1-3/9	1A

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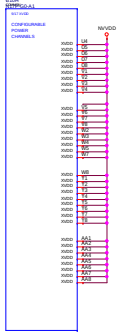
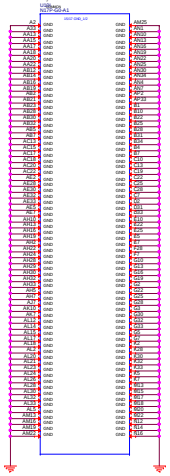
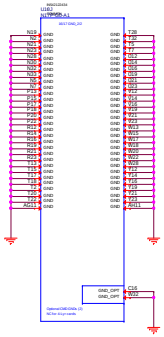
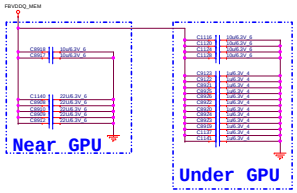
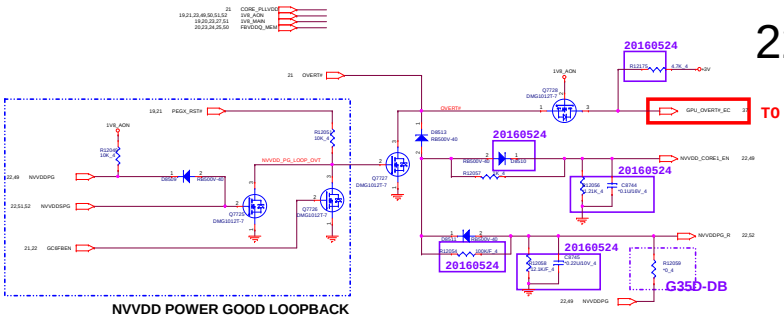






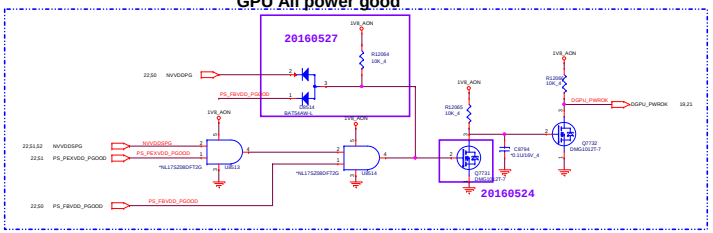


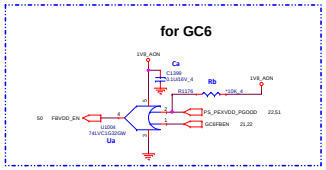


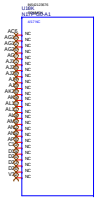
NVVDD POWER GOOD LOOPBACK

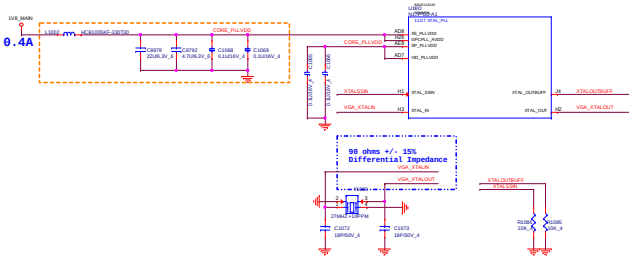
Overt temp ckt for NVVDD and NVVDDS

GPU All power good

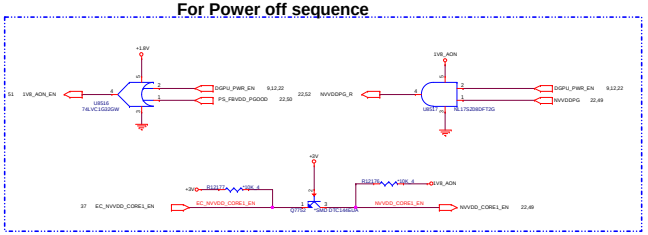


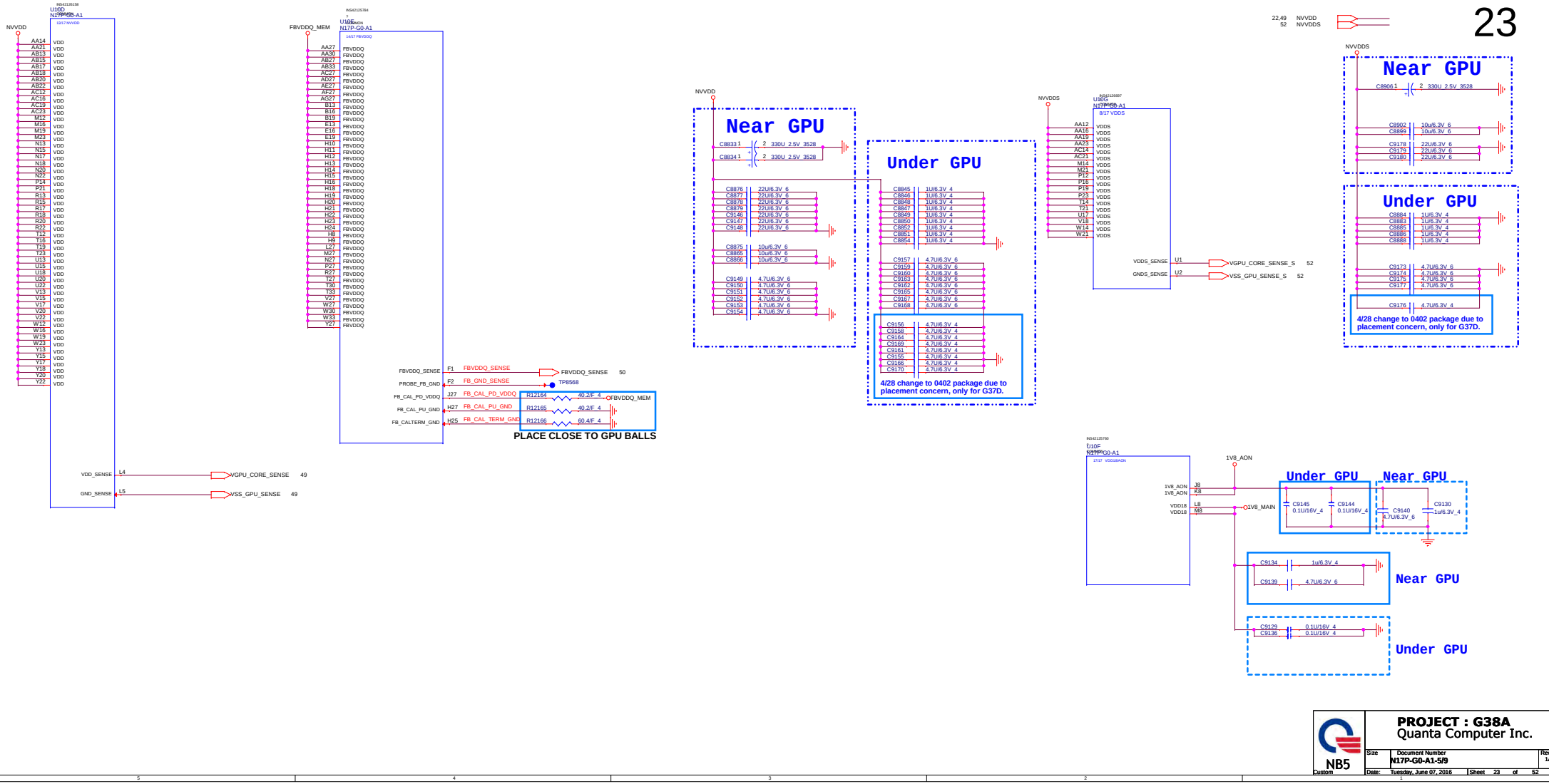






For Power off sequence





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	Size: — Document Number: N17P-G0-A1-5/9	Rev: 1A
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CHANNEL A: 2G/4G GDDR5

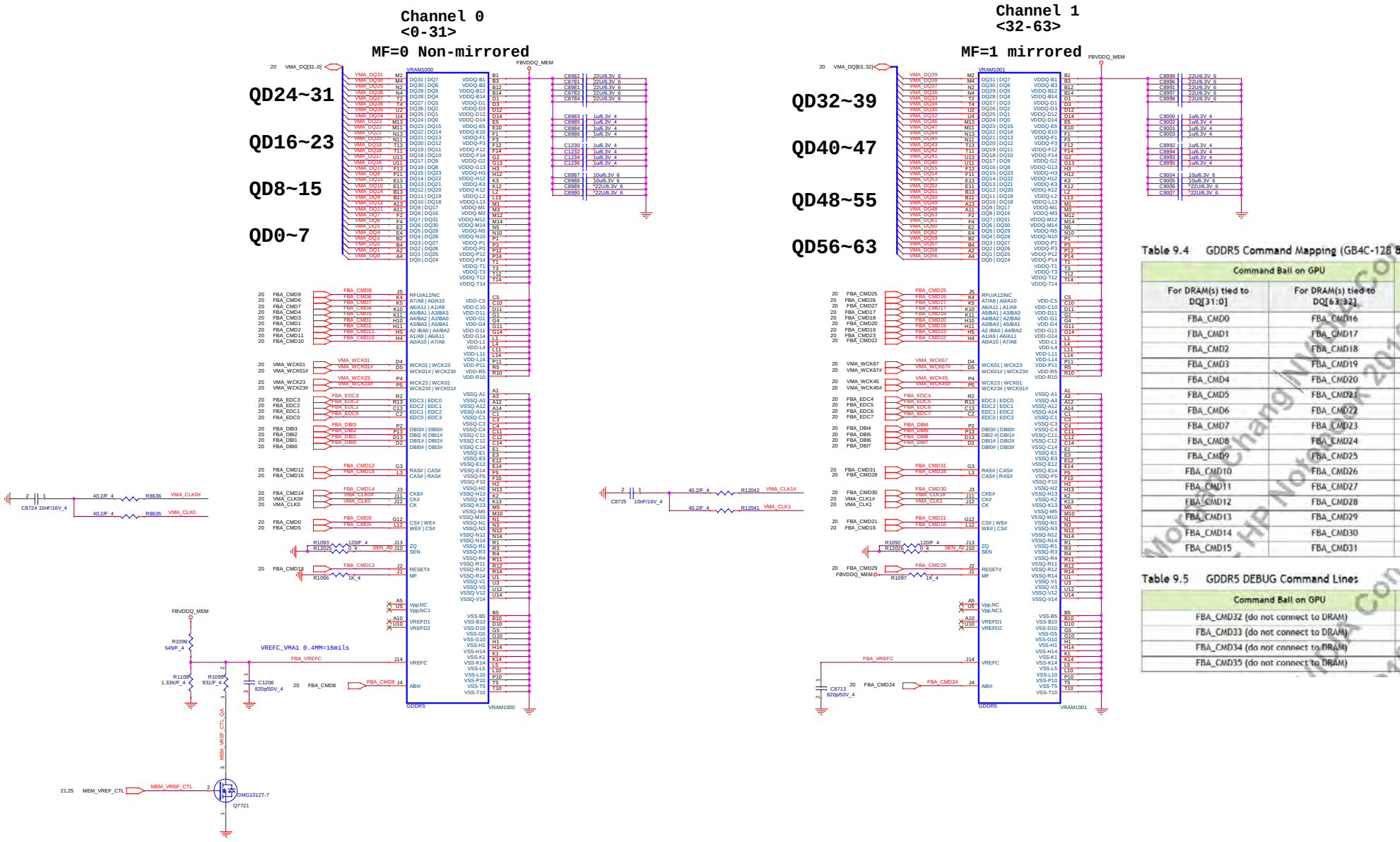

Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

NB5 Custom	PROJECT : G38A Quanta Computer Inc.	
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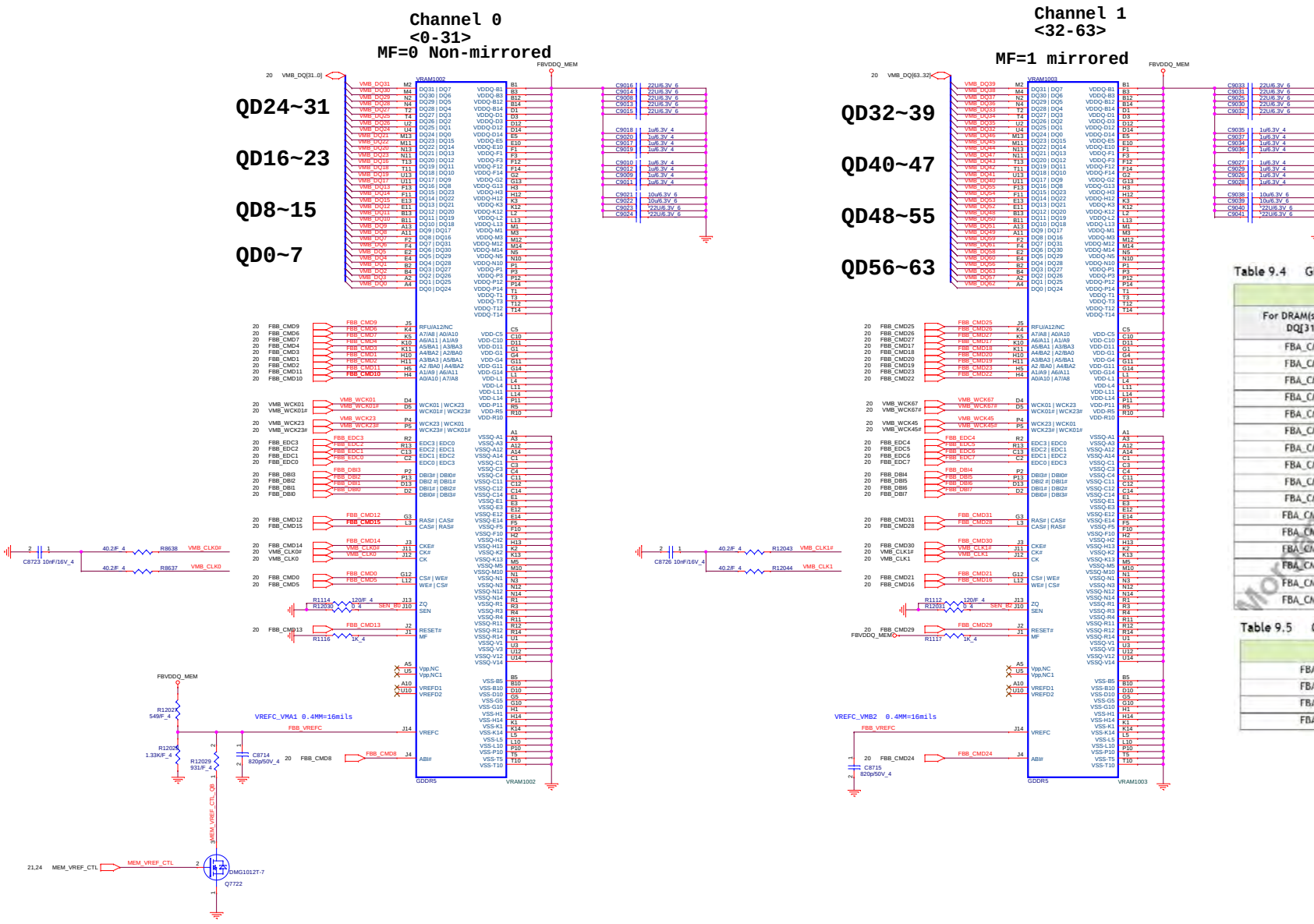


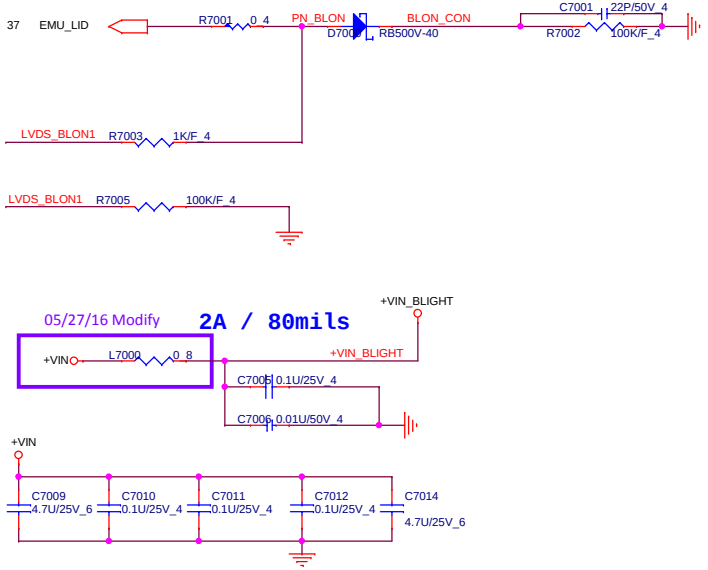
Table 9.4 GDDR5 Command Mapping (GB4C-128 & GB2C-64 packages)

Command Ball on GPU		DRAM Signal Definition
For DRAM(s) tied to DQ[31:0]	For DRAM(s) tied to DQ[63:32]	
FBA_CMD0	FBA_CMD16	CS*
FBA_CMD1	FBA_CMD17	A3_BA3
FBA_CMD2	FBA_CMD18	A2_BA0
FBA_CMD3	FBA_CMD19	A4_BA2
FBA_CMD4	FBA_CMD20	A5_BA1
FBA_CMD5	FBA_CMD21	WE*
FBA_CMD6	FBA_CMD22	A7_A8
FBA_CMD7	FBA_CMD23	A6_A11
FBA_CMD8	FBA_CMD24	ABI*
FBA_CMD9	FBA_CMD25	A12_RFU
FBA_CMD10	FBA_CMD26	A0_A10
FBA_CMD11	FBA_CMD27	A1_A9
FBA_CMD12	FBA_CMD28	RAS*
FBA_CMD13	FBA_CMD29	RST*
FBA_CMD14	FBA_CMD30	CKE*
FBA_CMD15	FBA_CMD31	CAS*

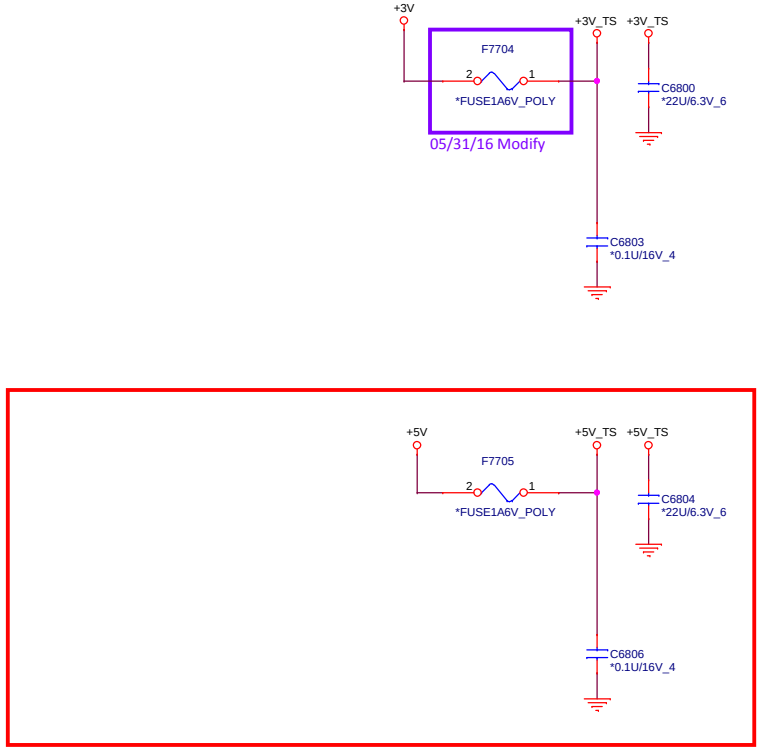
Table 9.5 GDDR5 DEBUG Command Lines

Command Ball on GPU	DRAM Signal Definition
FBA_CMD32 (do not connect to DRAM)	(not used)
FBA_CMD33 (do not connect to DRAM)	(not used)
FBA_CMD34 (do not connect to DRAM)	DEBUG0
FBA_CMD35 (do not connect to DRAM)	DEBUG1

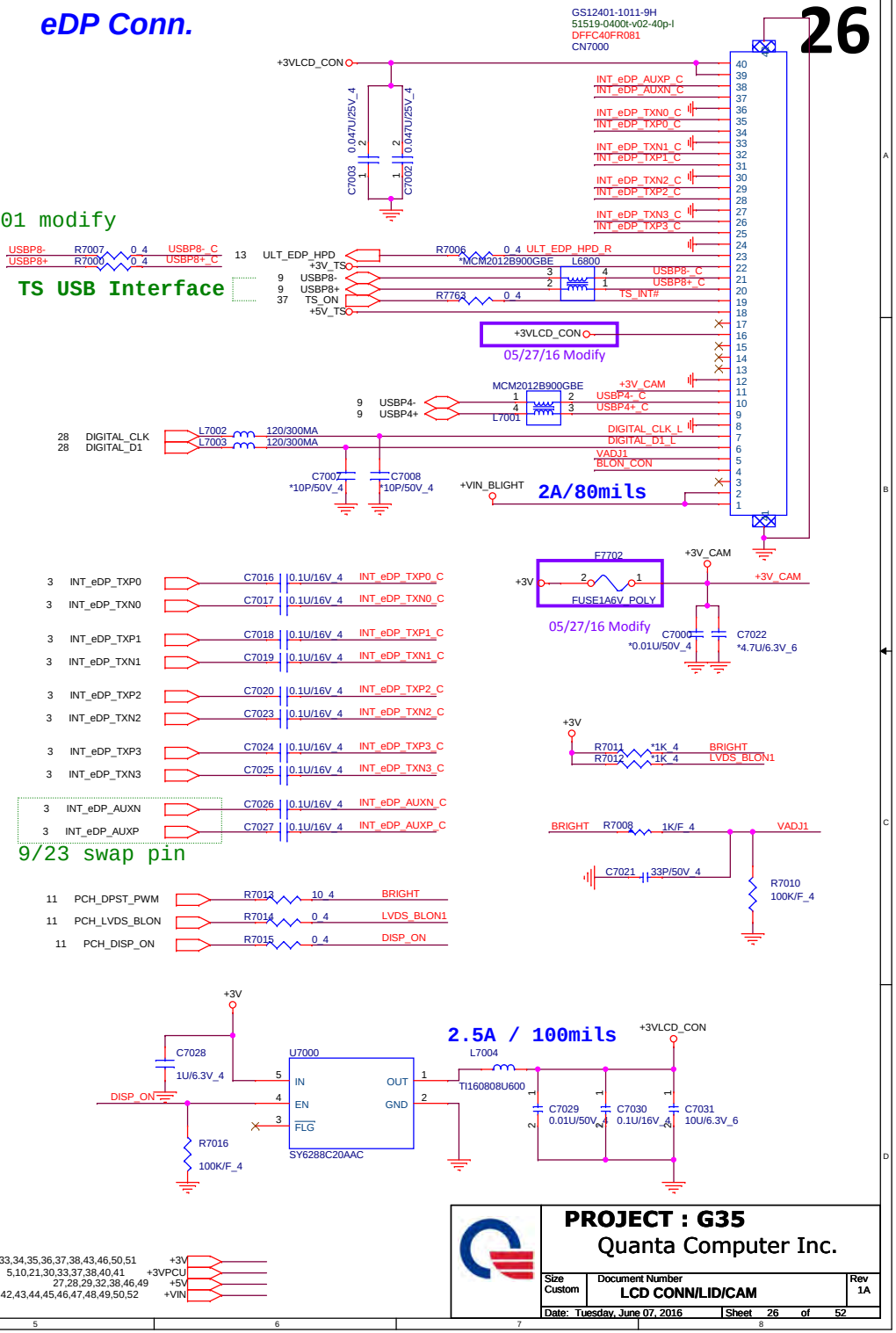
LID Switch



Touch screen



eDP Conn.



26

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	LCD CONN/LID/CAM	1A

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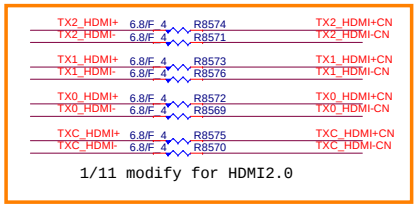
5,9,10,11,12,13,14,16,17,18,22,26,28,29,30,32,33,34,35,36,37,38,43,46,50,51 +3V

26,28,29,32,38,46,49 +5V

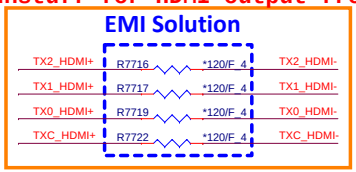
01/11 change to 0 ohm for NV suggest



1/11 modify for HDMI2.0

01/11 unstuff for HDMI output from GPU

EMI Solution



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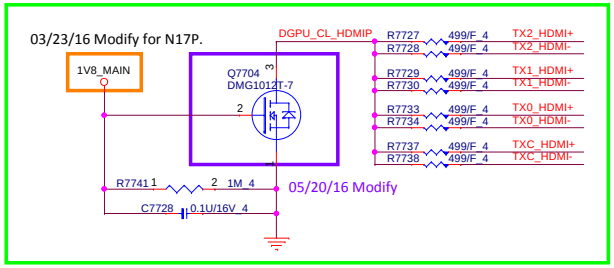
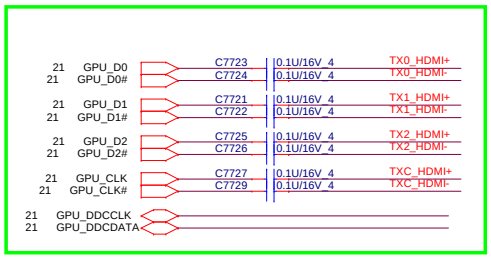
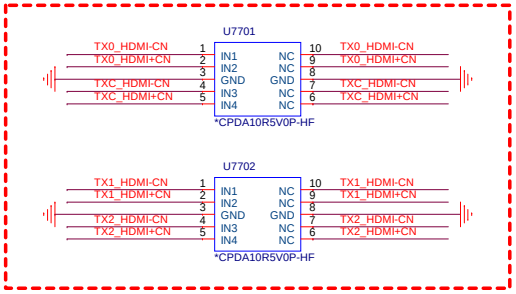


11/03 modify for HDMI2.0



ESD

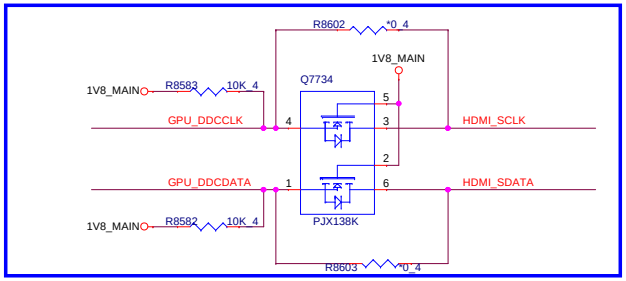


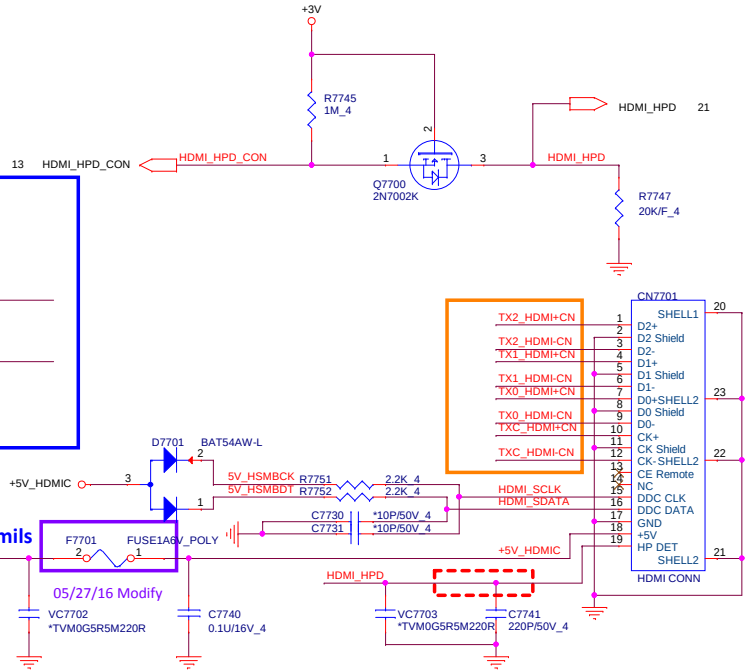
1125 Reserve ESD protection component

1125 SWAP

HDMI SMBus Isolation

Close to HDMI connector





0925 Del Net HDMI_DET_C

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Quanta Computer Inc.

Size	Document Number	Rev
Custom	27 -- HDMI/HDMI REDRIVER	1A
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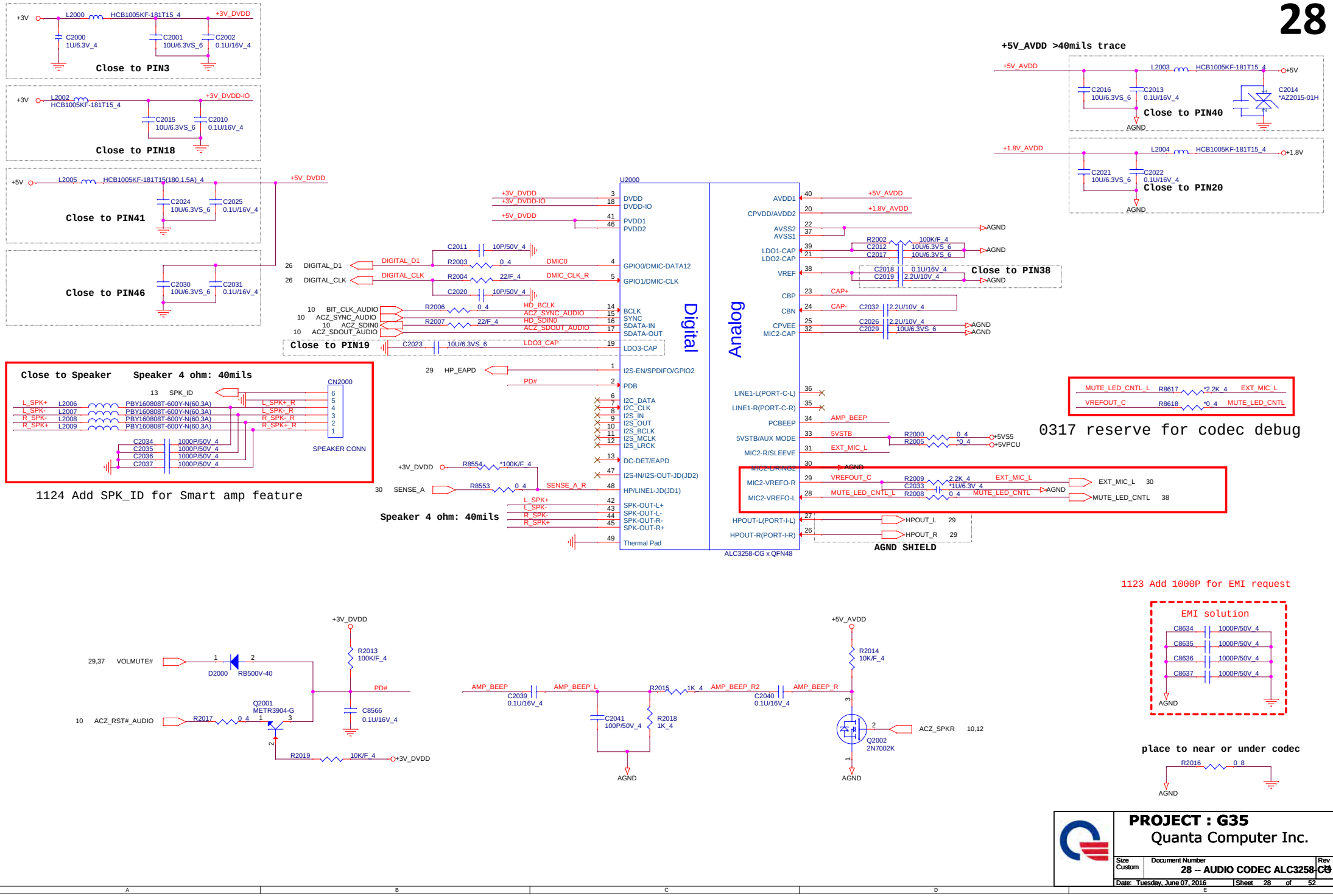
+5V_AVDD >40mils trace
Close to PIN3
Close to PIN18
Close to PIN41
Close to PIN46
Close to PIN19
Close to PIN40
Close to PIN20
Close to PIN38
Close to Speaker
Speaker 4 ohm: 40mils
1124 Add SPK_ID for Smart amp feature
0317 reserve for codec debug
AGND SHIELD
Digital
Analog
ALC3258-CG x QFN48
1123 Add 1000P for EMI request
EMI solution
place to near or under codec
PROJECT : G35
Quanta Computer Inc.
28 -- AUDIO CODEC ALC3258-CG
Date: Tuesday, June 07, 2016
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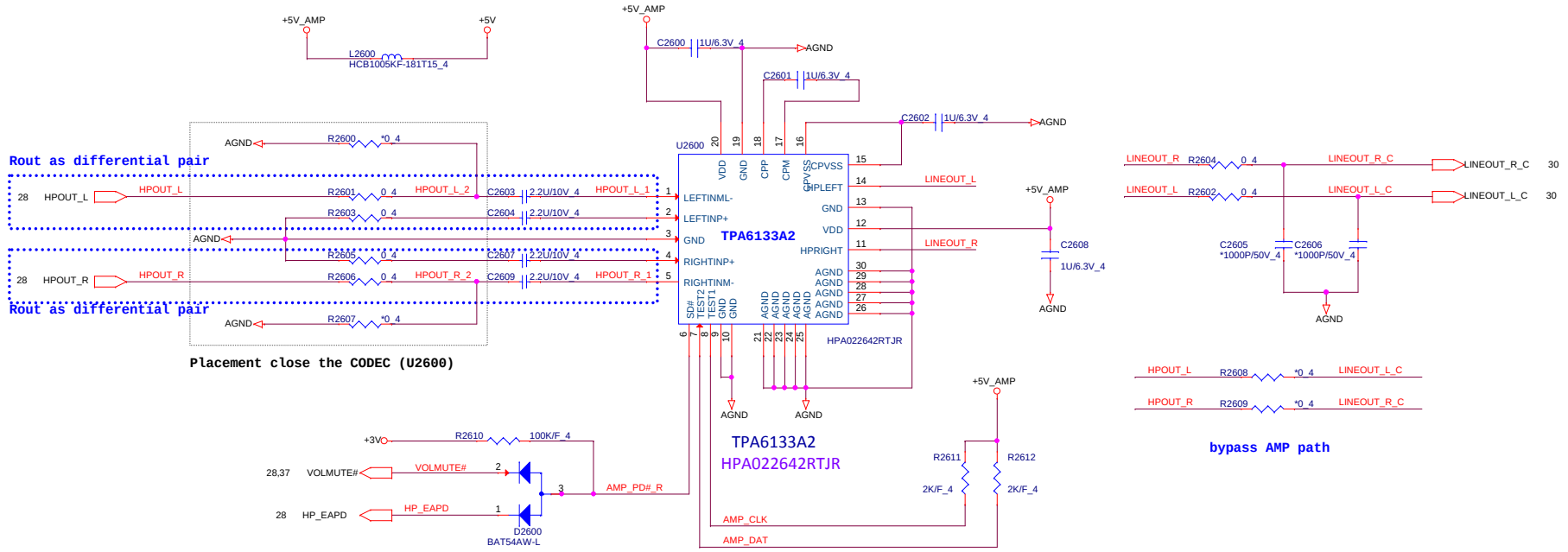
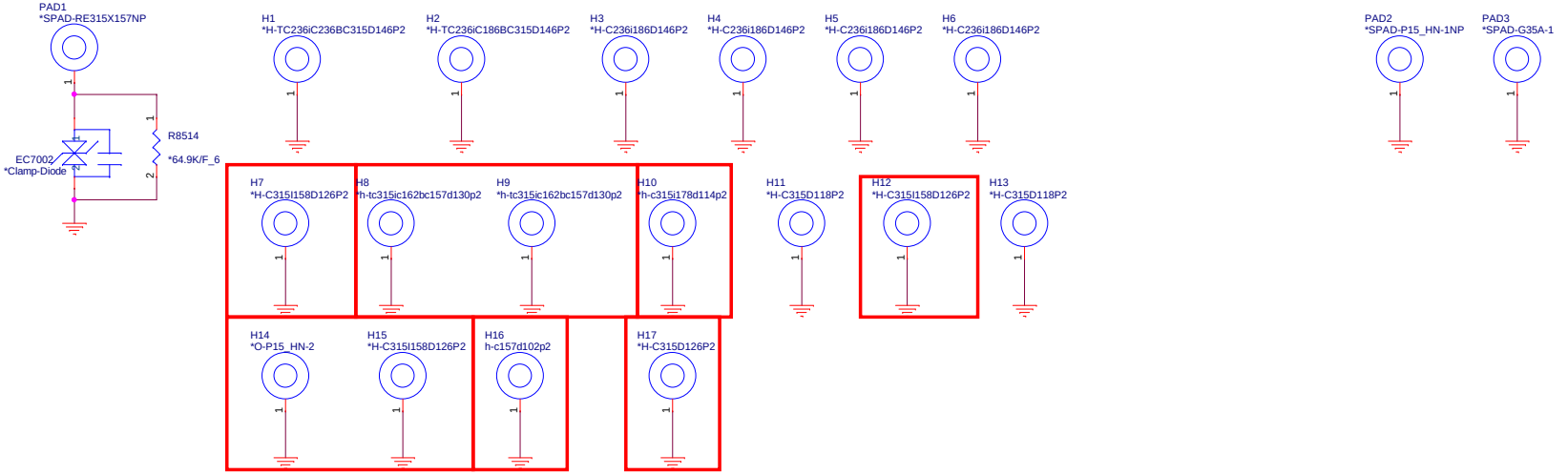
Head Phone out



HOLE



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Quanta Computer Inc.

Size	Document Number	Rev
Custom	29-- HP AMP HPA022642RTJR	1A
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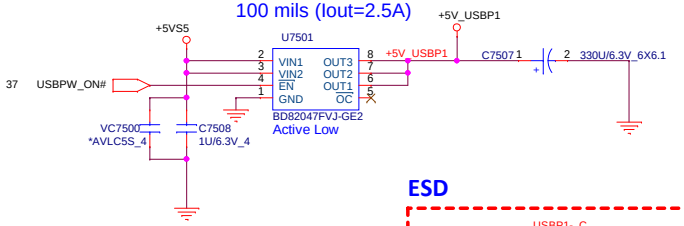
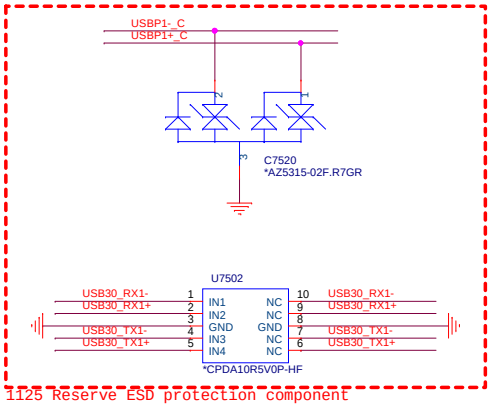
USB 2.0/3.0 Combo

100 mils (Iout=2.5A)

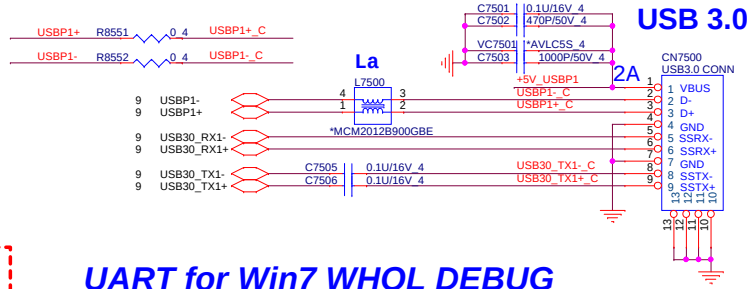


ESD

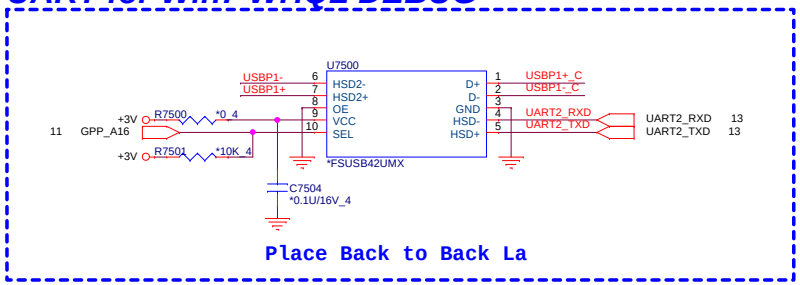


1125 Reserve ESD protection component

USB 3.0



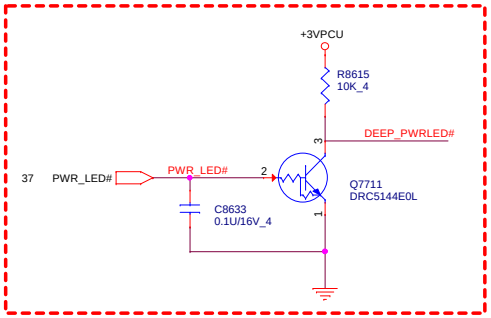
UART for Win7 WHQL DEBUG

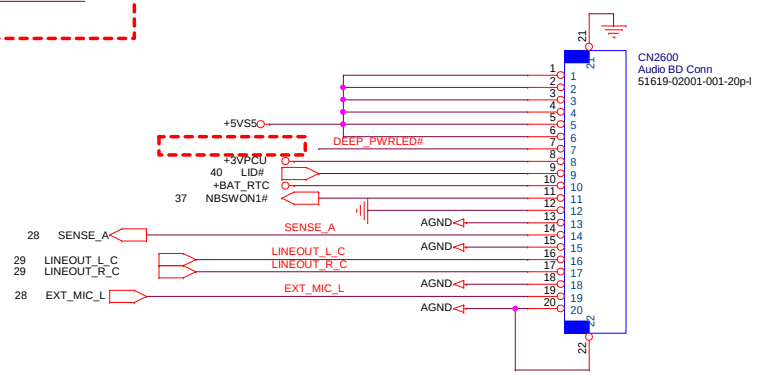


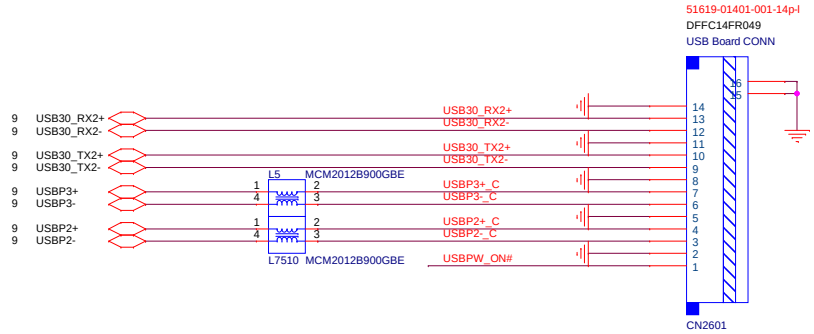
Place Back to Back La

Daughter Board

1123 Add PWR LED MOS Circuit







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Quanta Computer Inc.

Size	Document Number	Rev
Custom	30 – USB3.0/DB	1A
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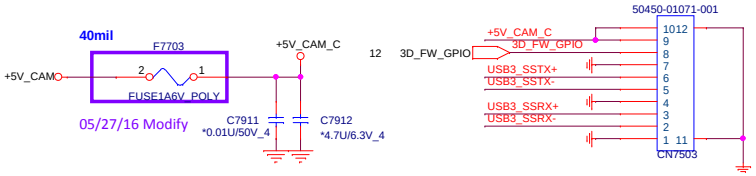
10/08 3D Camera MIC combine in LCD CONN

3D Camera Conn.

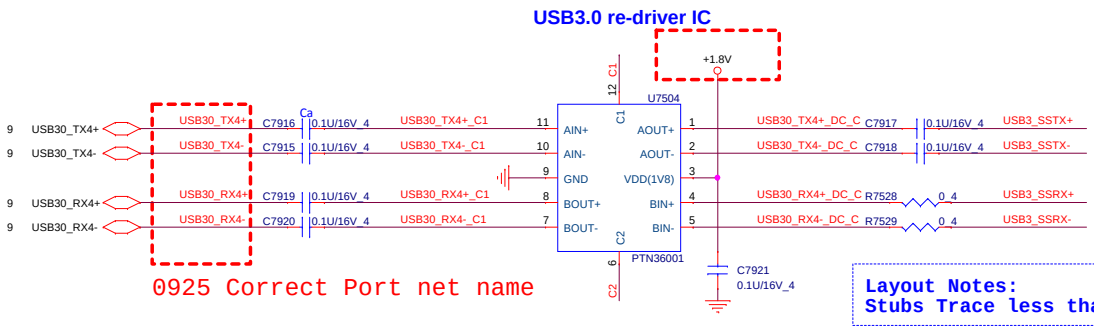


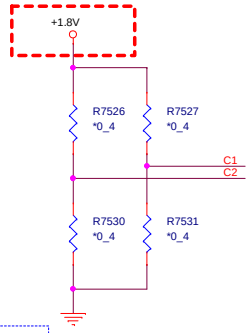
USB3.0

USB3.0 Re-driver IC

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V

1123 Change UB3 re driver power rail
from +1.8V_DEEP_SUS to +1.8V





Layout Notes:
Stubs Trace less than 150mil

Table 4. C1 pin controls long/medium/short traces

State	Channel type	Pin C1 state	Channel B	Channel A	
			EQ[1]	DE[2]	OS[2]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

Table 5. C2 pin controls long/medium/short traces

State	Channel type	Pin C2 state	Channel A	Channel B	
			EQ[1]	DE[2]	OS[2]
H	Long	H	9 dB	–5.3 dB	1.1 V
high-Z	Medium	high-Z	6 dB	–3.1 dB	1.0 V
L	Short	L	3 dB	0 dB	0.9 V

28,40,41,46,51 +5VPCU
5,10,21,30,33,37,38,40,41 +3VPCU
22,28,47,51 +1.8V

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Custom	31 – 3D CAM/REDRIVER	1A
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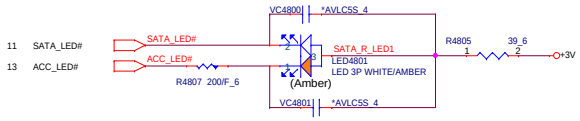
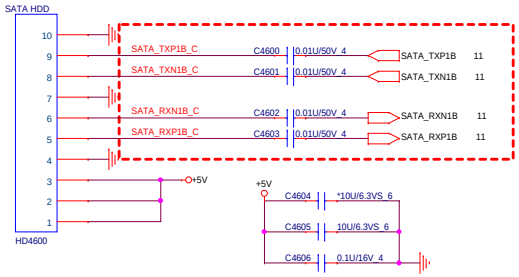
16,49 +3V
+5V
+3VPCU

SATA LED



HDD



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Quanta Computer Inc.

Size	Document Number	Rev
C	32 -- HDD/ODD	1A

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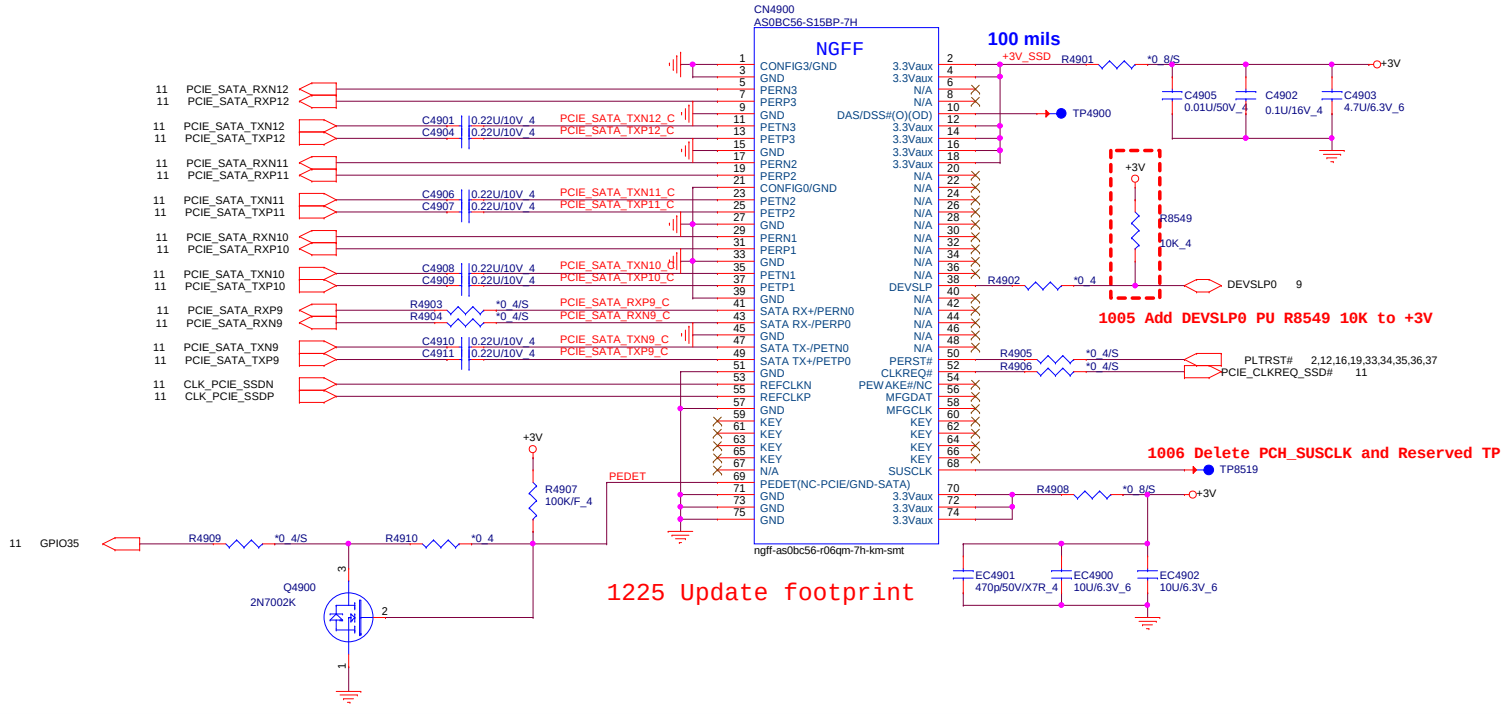
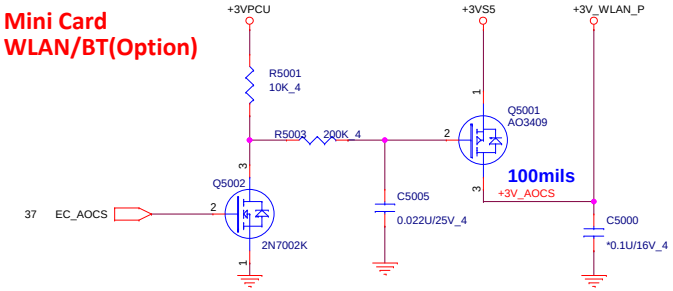
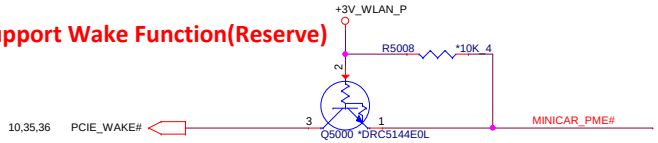
SSD

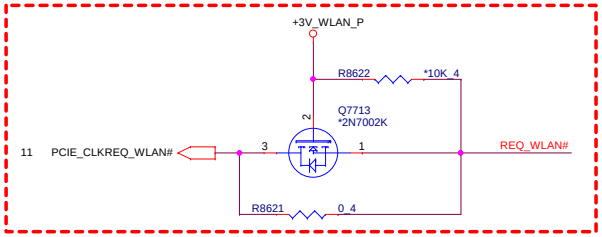


Mini Card WLAN/BT(Option)

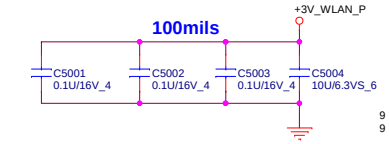


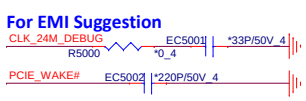
Support Wake Function(Reserve)





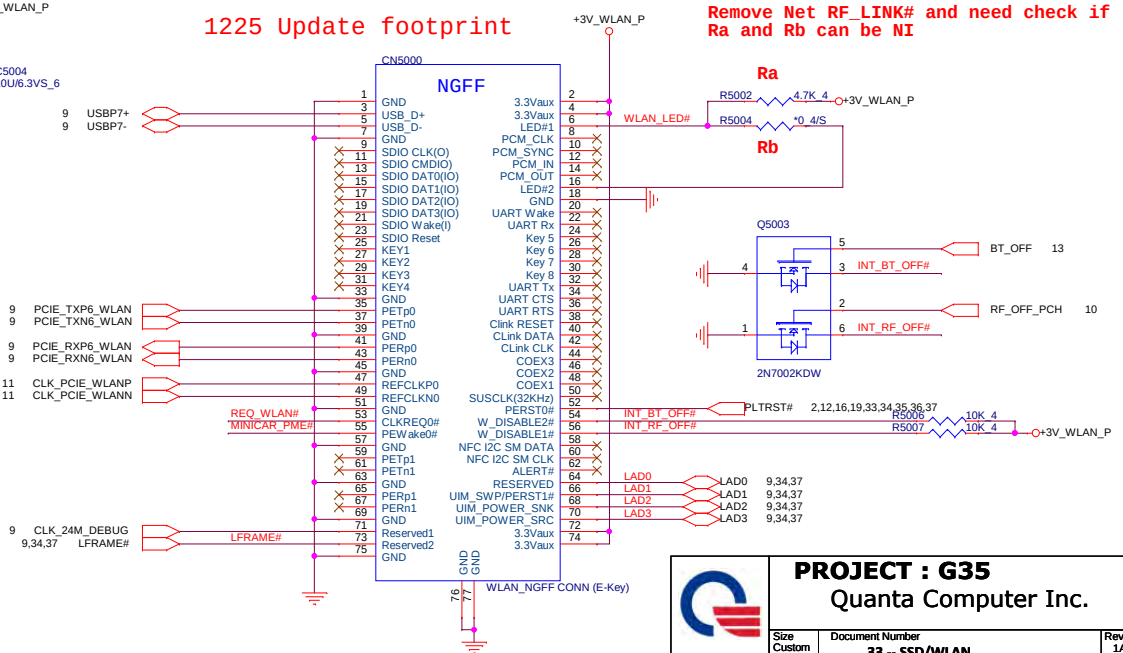
0302 Reserved the MOSFET at CLKREQ# even the current leakage test passed for HP requested





1225 Update footprint

Remove Net RF_LINK# and need check if Ra and Rb can be NI

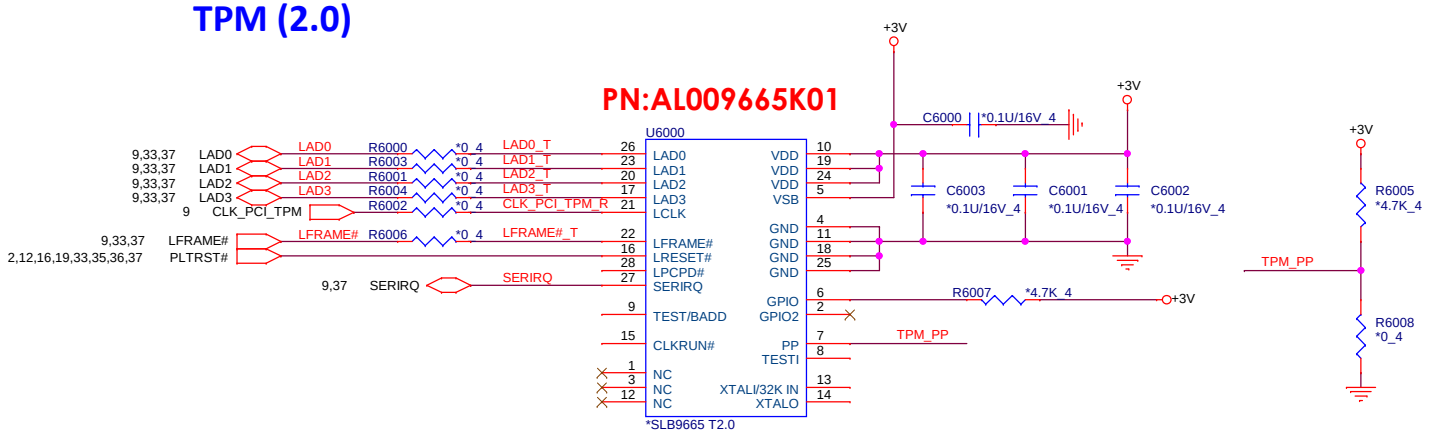


PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	33 -- SSD/WLAN	1A
Date: Tuesday, June 07, 2016	Sheet 33 of 52	

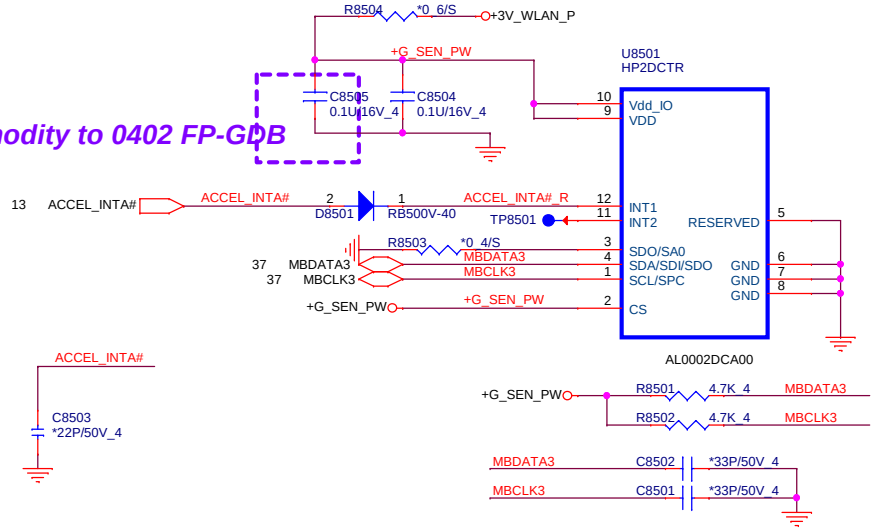
TPM (2.0)

PN:AL009665K01

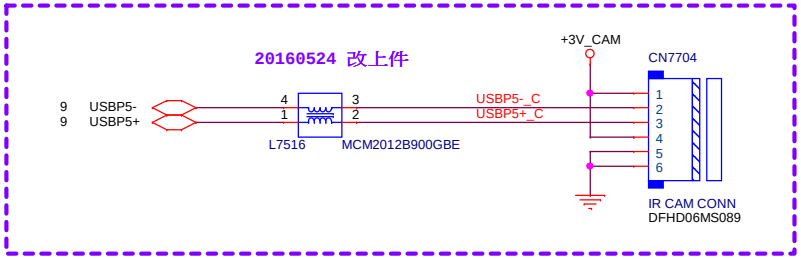


Accelerometer Sensor

modity to 0402 FP-GDB



IR CAM



PROJECT : G35
Quanta Computer Inc.

B 34 -- TPM/Sensor Document Number 1A Rev

Tuesday, June 07, 2016 Date: 34 Sheet 52 of

LAN & RJ45

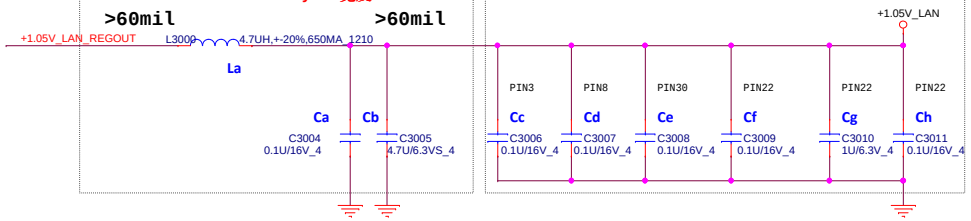
For SWR mode support RTL8111HSH/RTL8107ESH

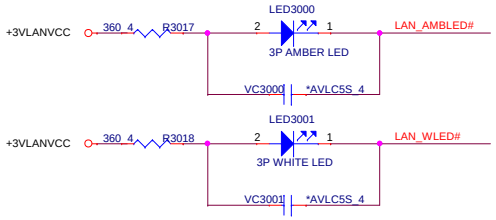
Stuff La, Ca ,Cb

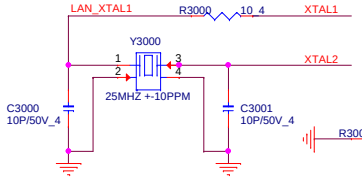
* Place Cc,Cd,Ce,Cf for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 3, 22, 8 , 30

* Place Cg,Ch for RTL8111H(S) & RTL8107E(S) close to each VDD10 pin-- 22(reserved)

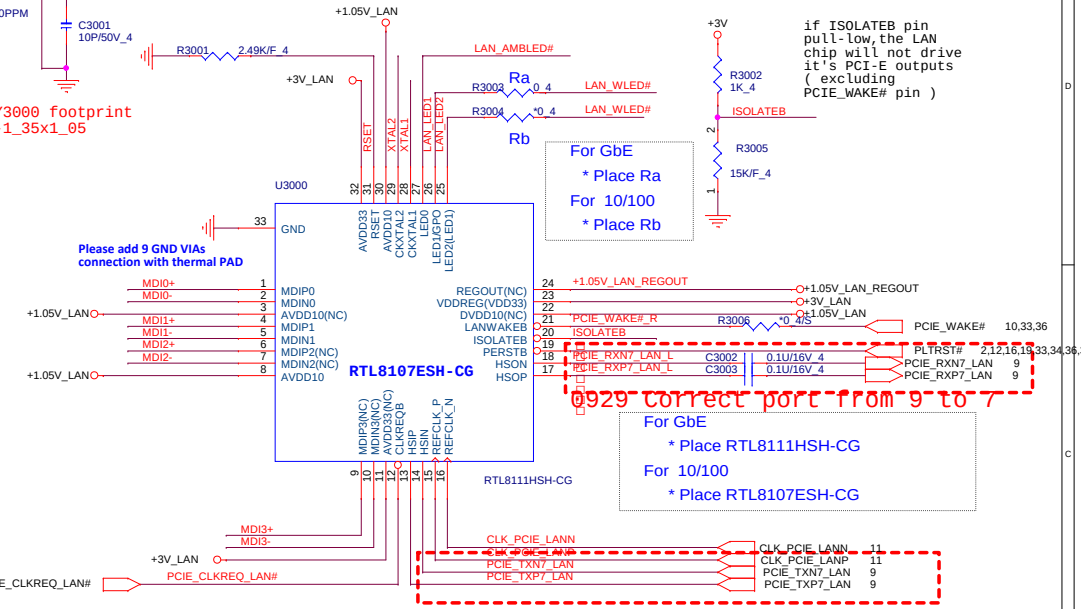
Power trace Layout 寬度> 60mil







1028 Change Y3000 footprint to xtl-2x1_6-1_35x1_05

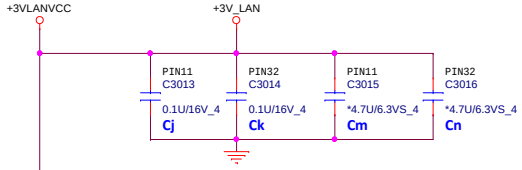


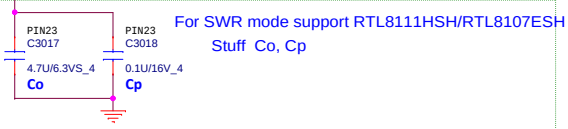
0929 Correct port from 9 to 7

For 10/100 stuff only Close RJ45

* Place Cj and Ck, close to each VDD33 pin-- 11, 32 for RTL8111H(S) & RTL8107E(S)

* For surge improvement, place Cm and Cn, close to each VDD33 pin-- 11, 32(optional)

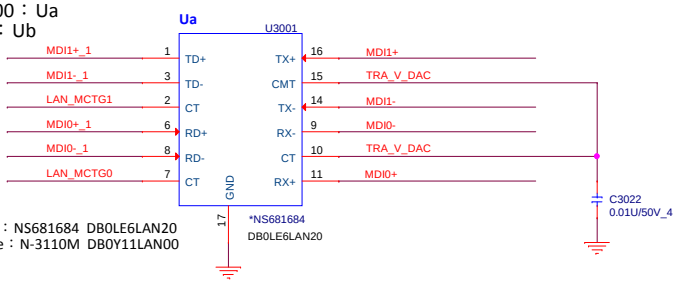




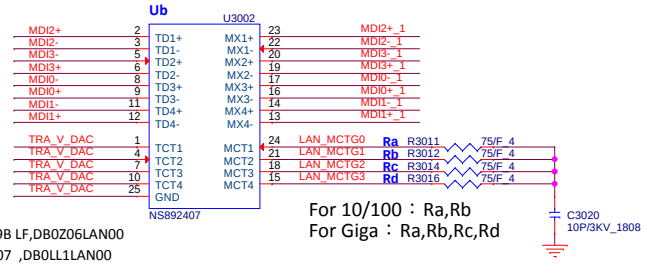
For SWR mode support RTL8111HSH/RTL8107ESH

Stuff Co, Cp

For 10/100：Ua
For Giga：Ub

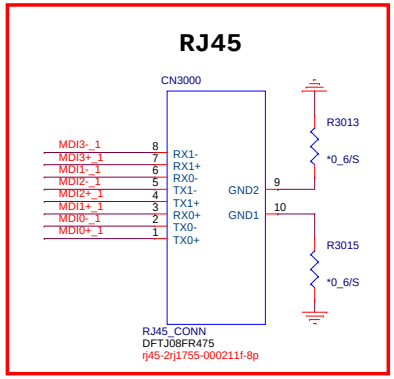


1st source：NS681684 DB0LE6LAN20
2nd source：N-3110M DB0Y11LAN00



For GiGA
BOT:GST5009B LF,DB0Z06LAN00
FCE :NS892407 ,DB0LL1LAN00

For 10/100：Ra,Rb
For Giga：Ra,Rb,Rc,Rd



0104 Update footprint

5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,36,37,38,43,46,50,51

46 +3V +3VLANVCC

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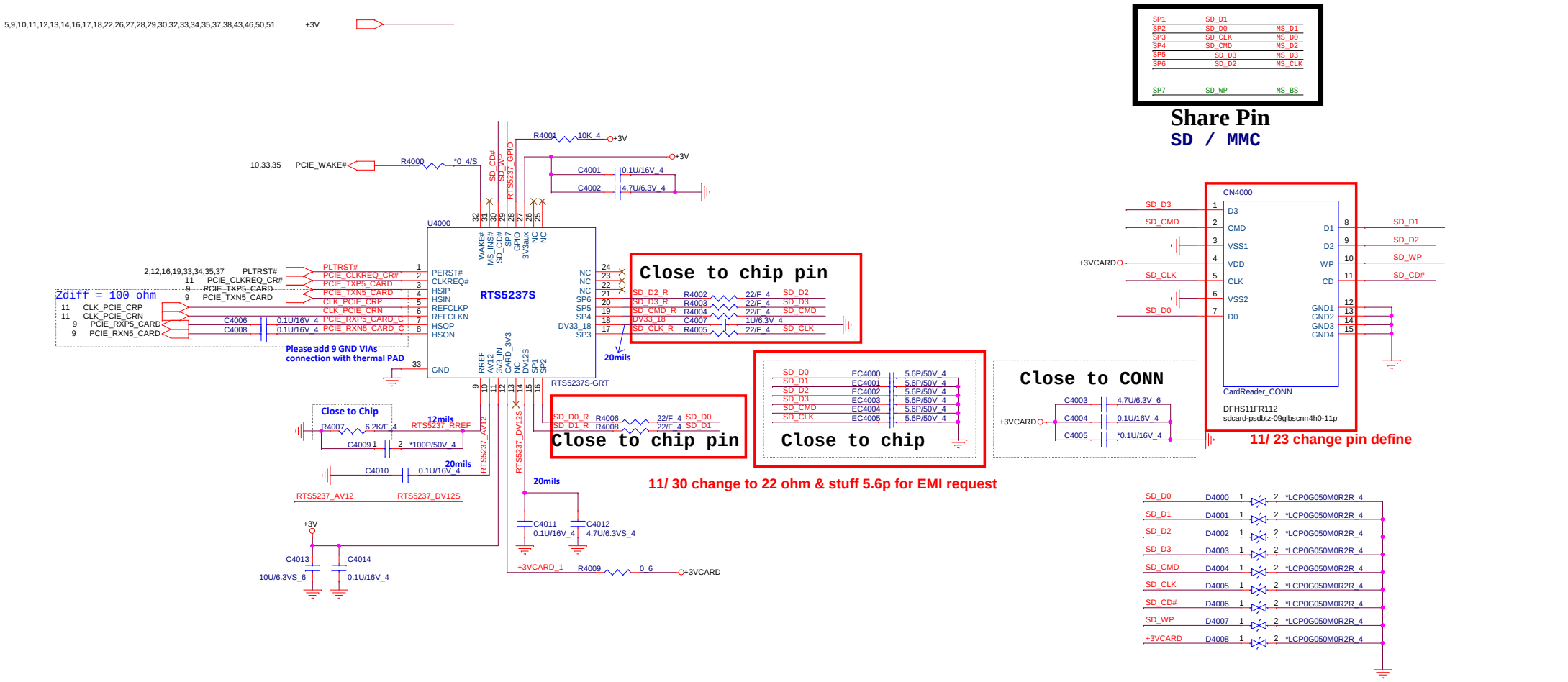
Quanta Computer Inc.

Size	Document Number	Rev
Custom	35 – LAN RTL8107ESH-CG/RJ45	1A
Date: Tuesday, June 07, 2016	Sheet 35 of 52	

RTS5237S PCIE CARD READER Controller



PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	36 – CR RTS5237S/CR SOCKET	1A

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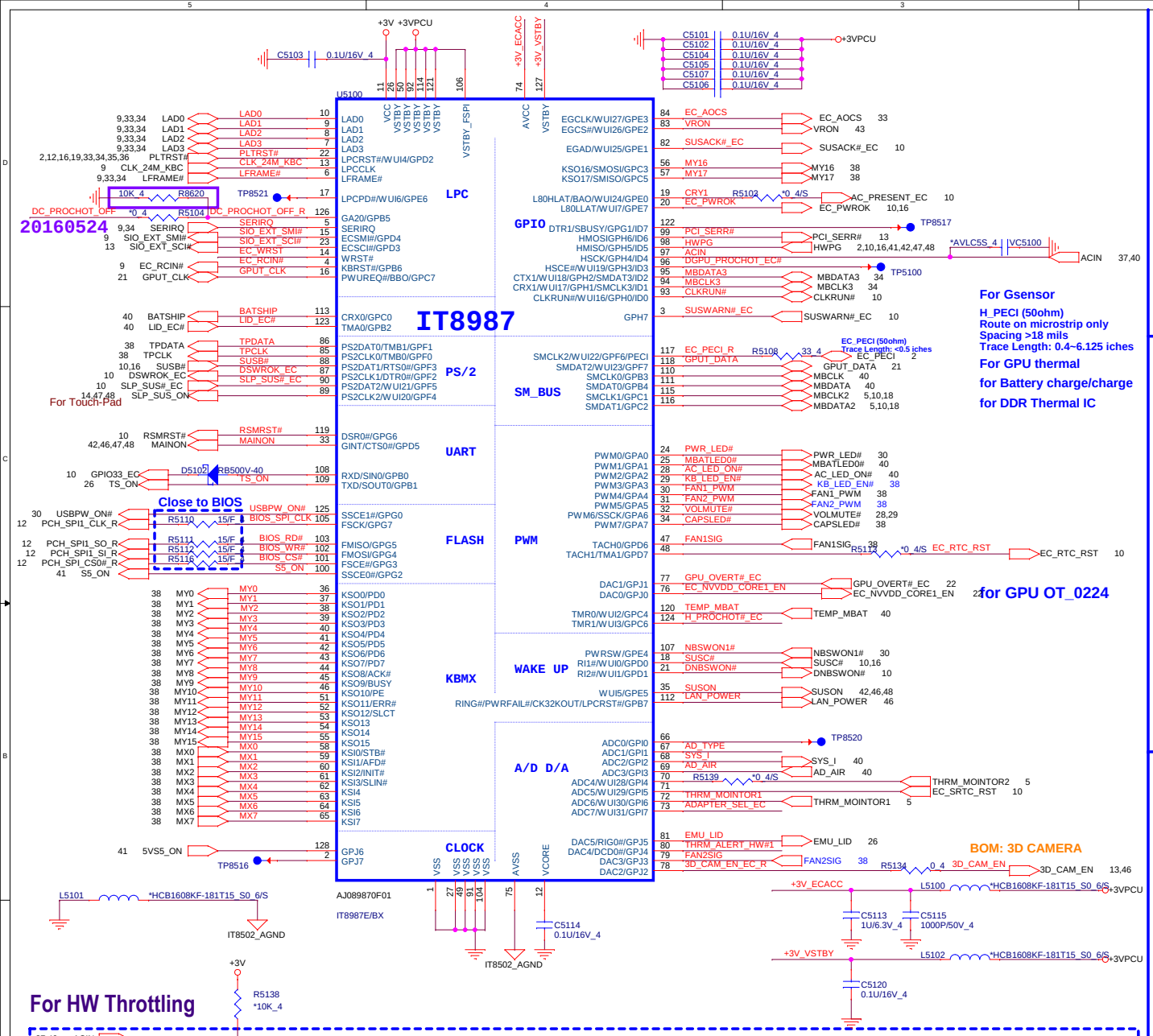
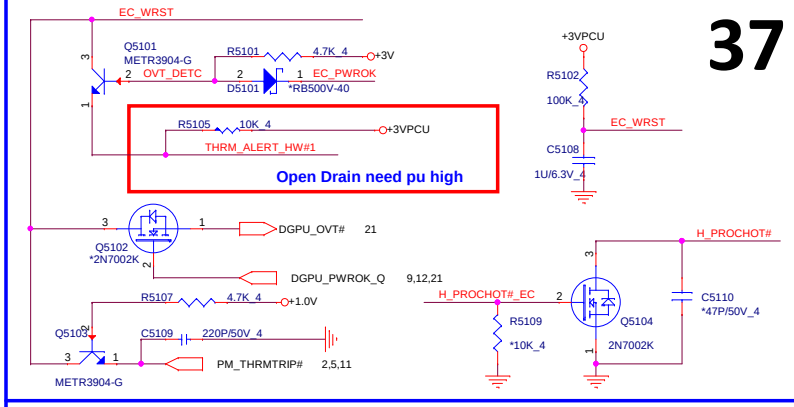
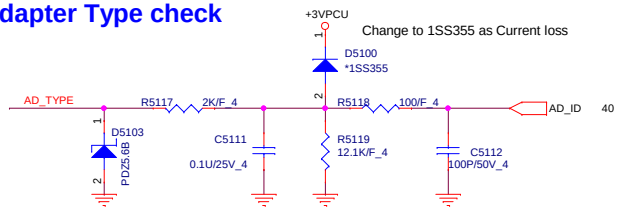


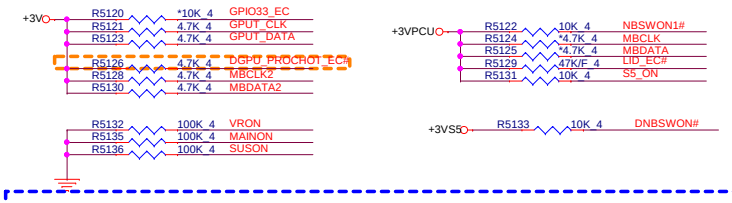


Adapter select for EC

	Ra	Rb	ADAPTER_SEL_EC	BOM
200W	10K(CS31002FB26)	100K (CS41002FB28)	3V	
150W	10K(CS31002FB26)	27.4K(CS32742FB14)	2.42V	
120W	10K(CS31002FB26)	12.1K(CS31212FB28)	1.8V	DIS
90W	10K(CS31002FB26)	6.2K(CS26202FB17)	1.26V	UMA
65W	10K(CS31002FB26)	2.2K(CS22202FB08)	0.59V	
45W	NC	10K(CS31002FB26)	0V	

Adapter Type check





CLOSE to EC Pin

5,9,10,11,12,13,14,16,17,18,22,26,27,28,29,30,32,33,34,35,36,38,43,46,50,51 +3V
10,12,14,16,33,41,42,46,47,48 +3VS5
5,10,21,30,33,38,40,41 +3VPCU

	AC_PRESENT_EC	H_PROCHOT#_EC	H_PROCHOT#
AC IN: AC mode Operation	H	L	H
AC remove: AC mode to DC mode	L	L	L
DC mode recover from PROCHOT	L	H	H

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	37 -- EC (IT8987)	1A
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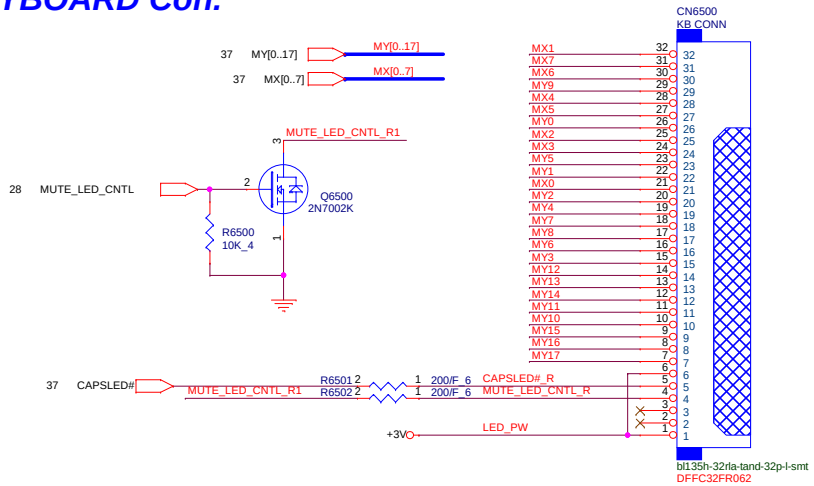
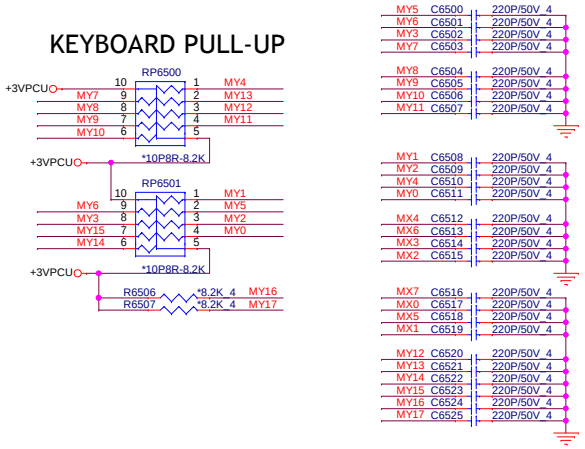
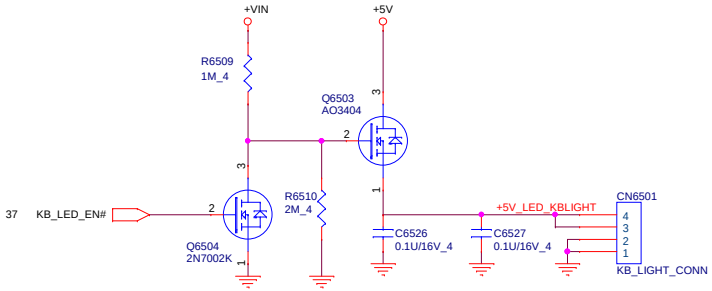
KEYBOARD Con.



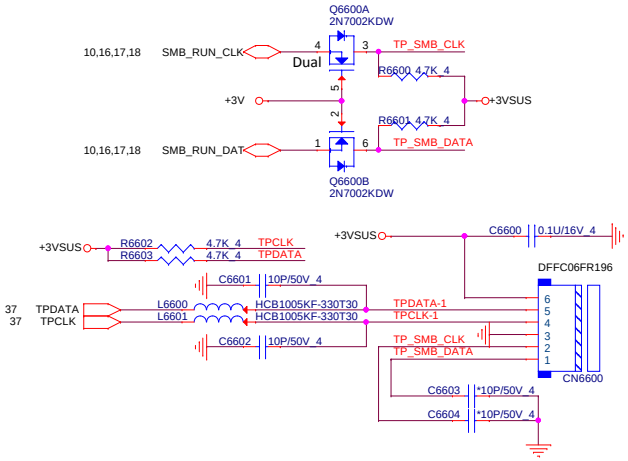
KEYBOARD PULL-UP



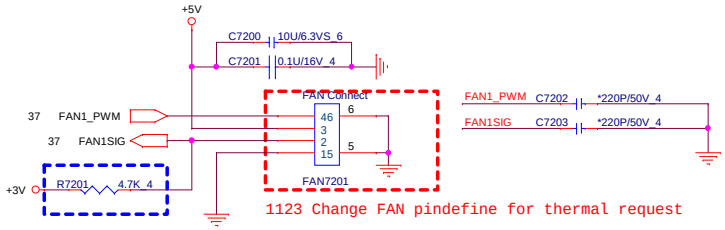
KB LIGHT CONN

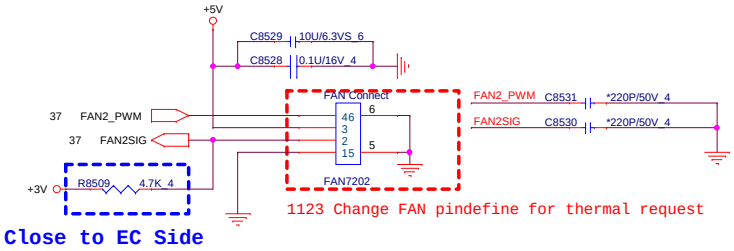


Touch Pad Connector



FAN

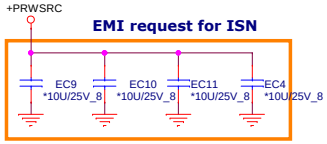


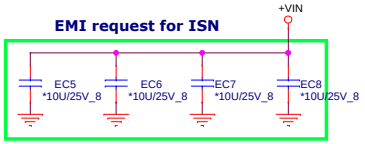


38

PROJECT : G35
Quanta Computer Inc.

Size	Document Number	Rev
Custom	38 -- KB/TP/FAN/HOLE	1A
Date: Tuesday, June 07, 2016	Sheet 38 of 52	





NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	**RF Solution**	1A

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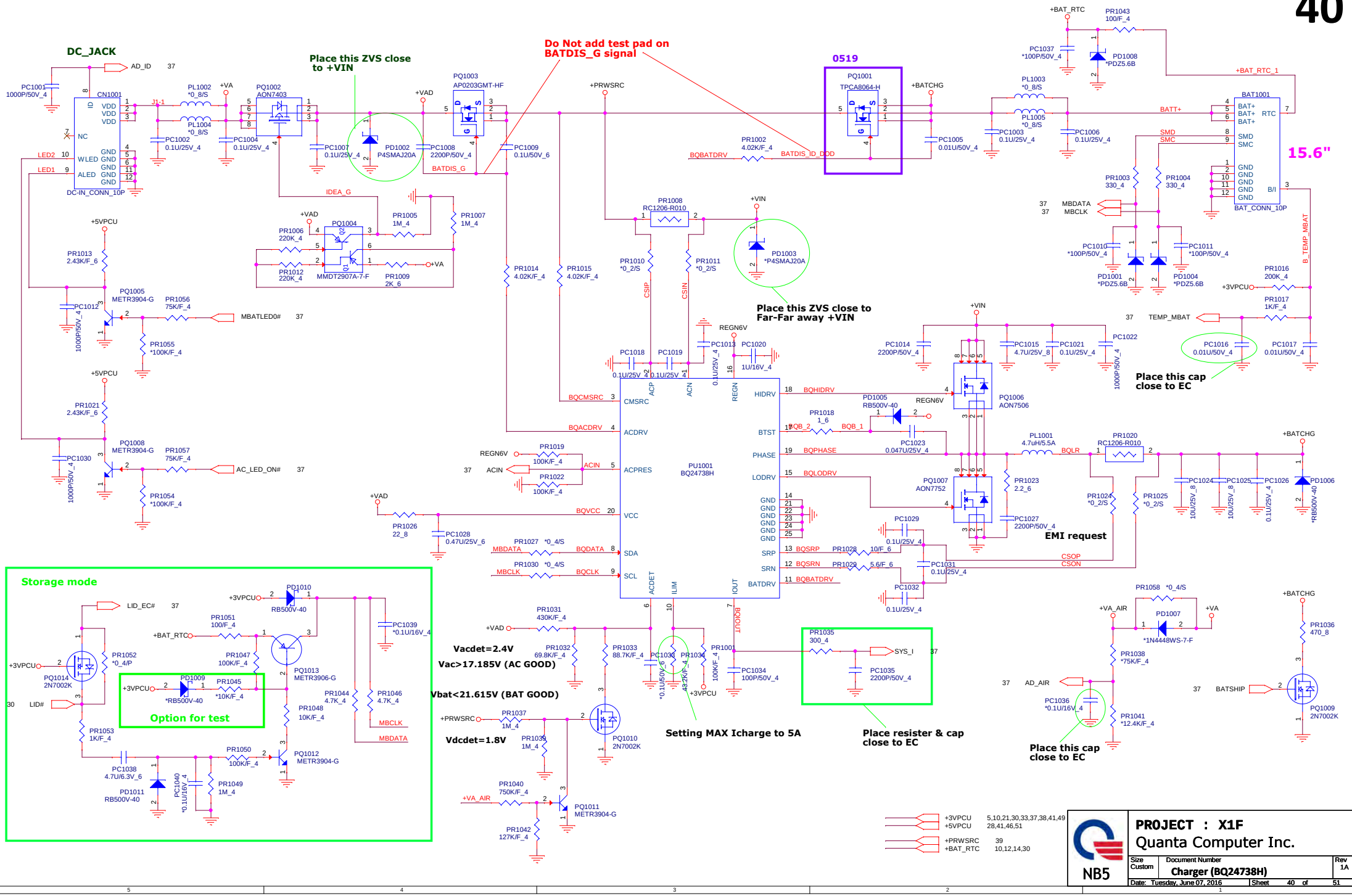
DC_JACK
Place this ZVS close to +VIN
Do Not add test pad on BATDIS_G signal
0519
15.6"
Place this ZVS close to Far-Far away +VIN
Place this cap close to EC
EMI request
Storage mode
Option for test
Vacdet=2.4V
Vac>17.185V (AC GOOD)
Vbat<21.615V (BAT GOOD)
Vdcdet=1.8V
Setting MAX Icharge to 5A
Place resister & cap close to EC
Place this cap close to EC
PU1001 BQ24738H
PROJECT : X1F
Quanta Computer Inc.
NB5
Charger (BQ24738H)
Date: Tuesday, June 07, 2016
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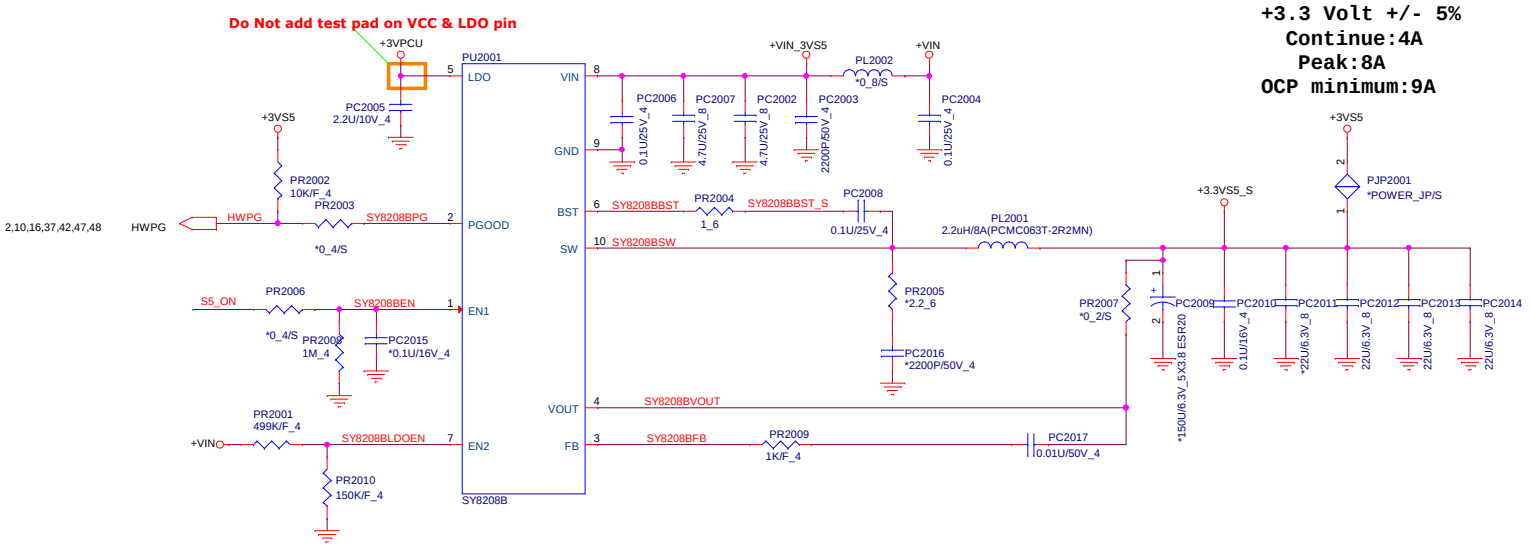

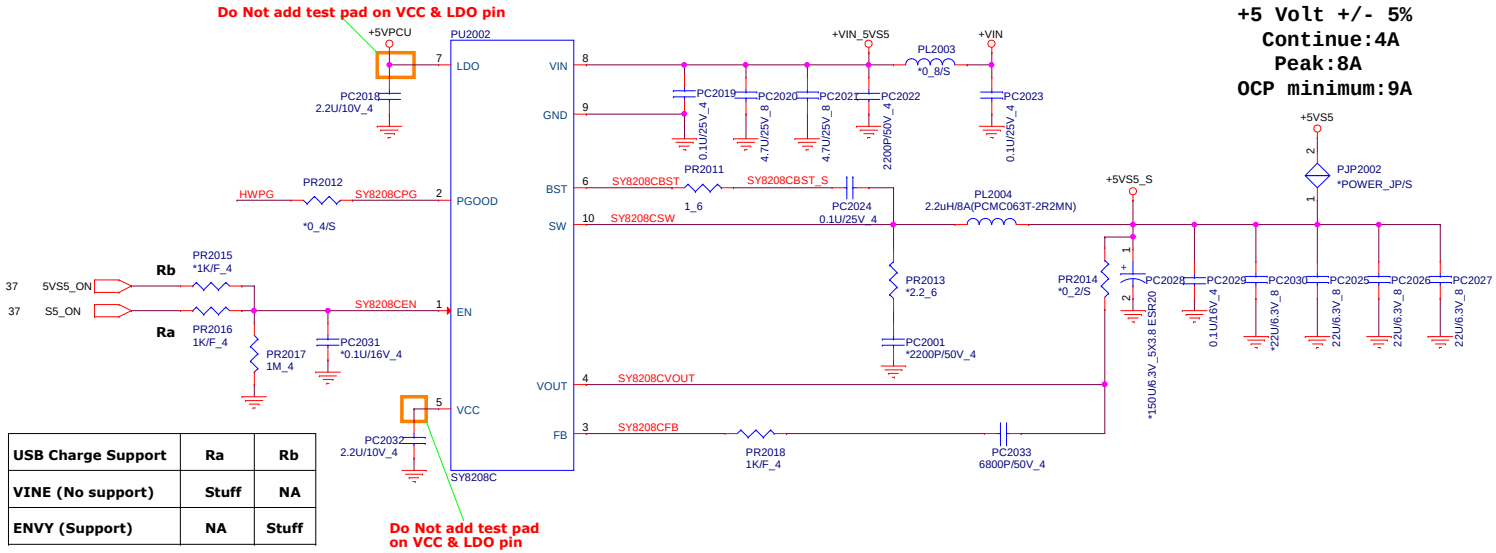

USB Charge Support	Ra	Rb
VINE (No support)	Stuff	NA
ENVY (Support)	NA	Stuff

Do Not add test pad on VCC & LDO pin

+VIN	26,38,39,40,42,43,44,45,46,47,48,49,53,54
+3VS5	10,12,14,16,33,37,42,46,47,48
+5VS5	10,28,30,42,43,44,45,46,47,48,49,51,53,54
+3VPCU	5,10,21,30,33,37,38,40,49
+5VPCU	28,40,46,51

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	3/5VS5 (SY8208B/SY8208C)	1A
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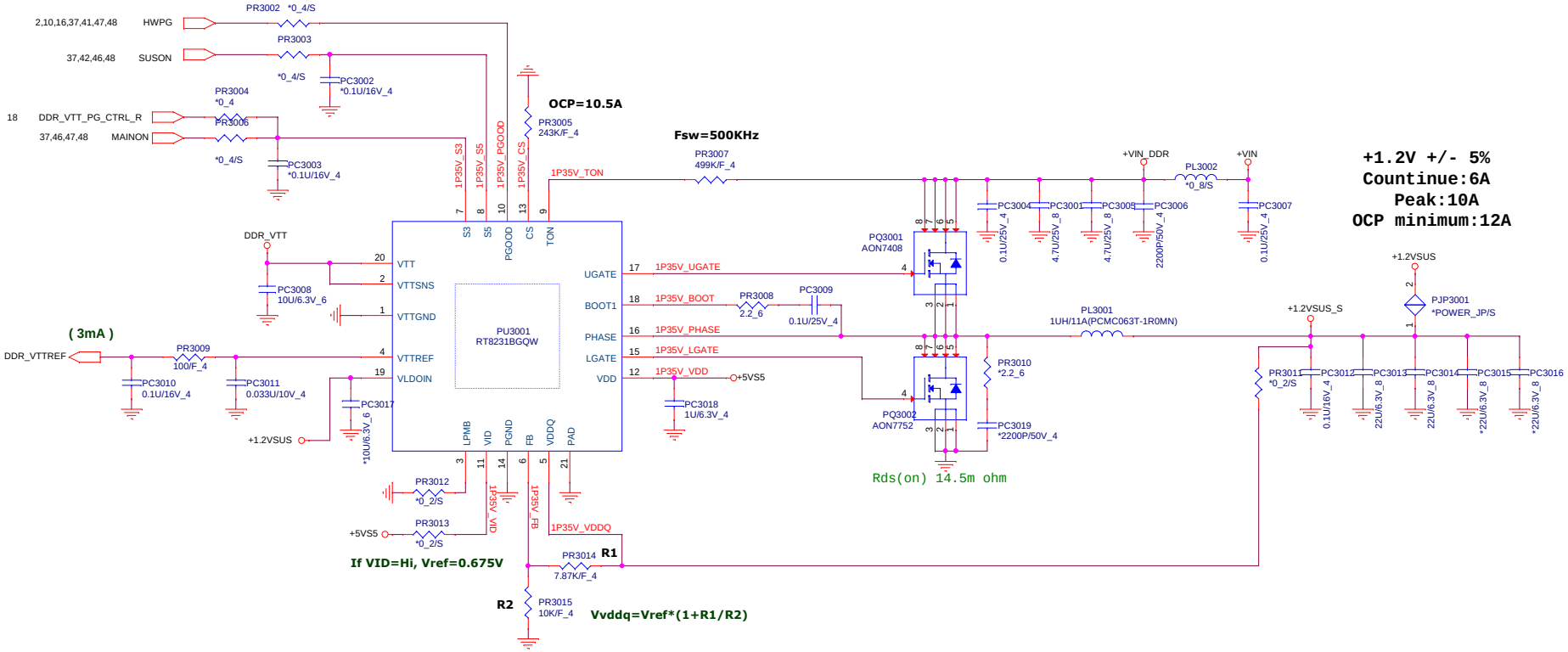

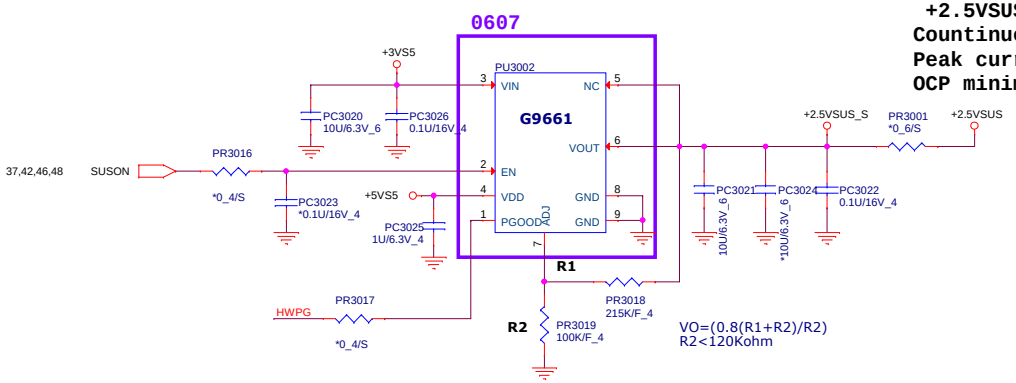

+VIN 26,38,39,40,41,43,44,45,46,47,48,49,53,54
+5VS5 10,28,30,41,43,44,45,46,47,48,49,51,53,54
+1.2VSUS 2,6,10,17,18,48,51
DDR_VTT 17,18
+2.5VSUS 17,18

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
	DDR3 (RT8231B)	1A

NB5

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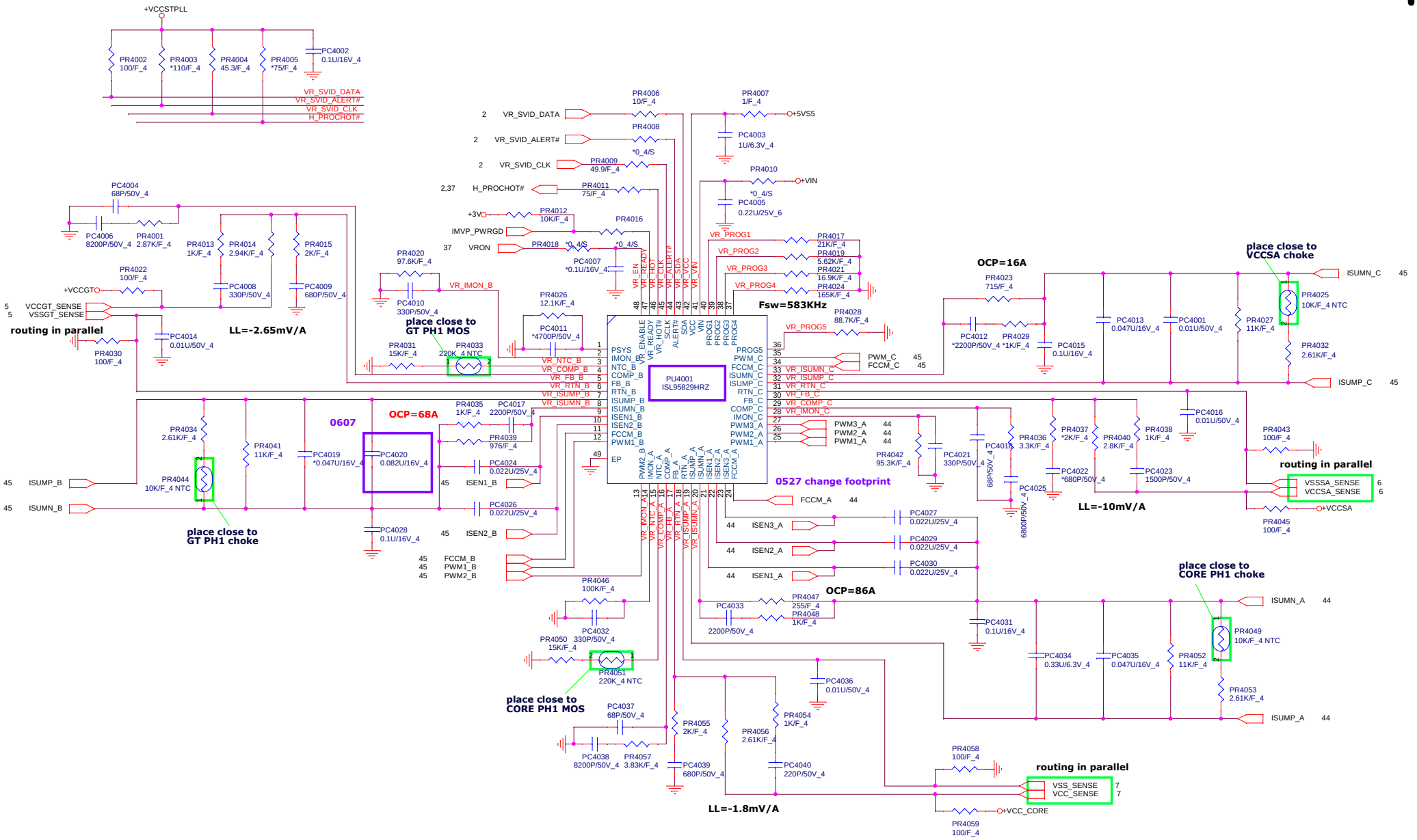

PROJECT : X1F	
Quanta Computer Inc.	
NB5	Size: Custom; Document Number: CPU VR IC (ISL95829HRZ); Rev: 1A
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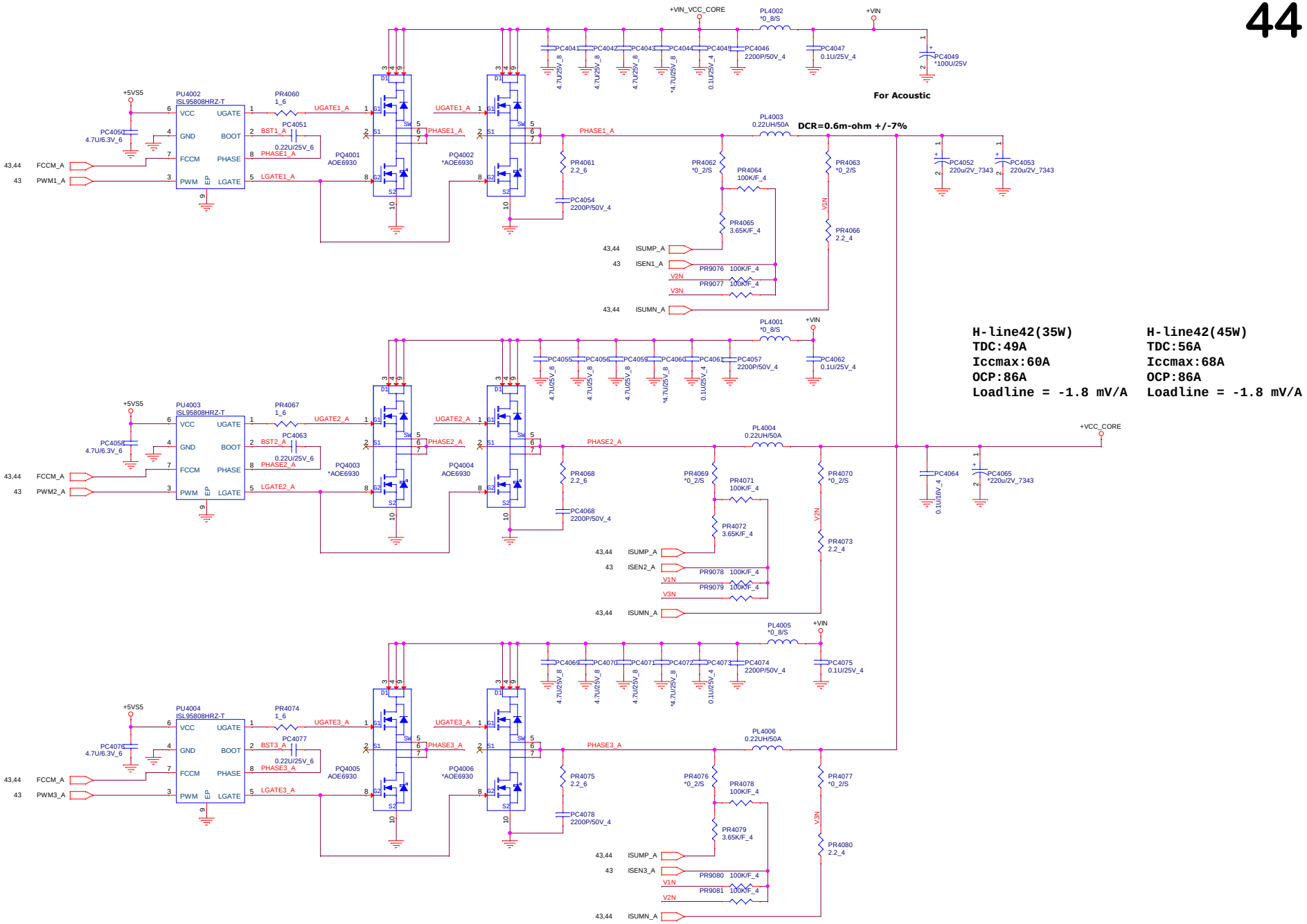

H-line42(35W)
TDC:49A
Iccmax:60A
OCP:86A
Loadline = -1.8 mV/A

H-line42(45W)
TDC:56A
Iccmax:68A
OCP:86A
Loadline = -1.8 mV/A

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCC_CORE (ISL95808HRZ-T)	1A

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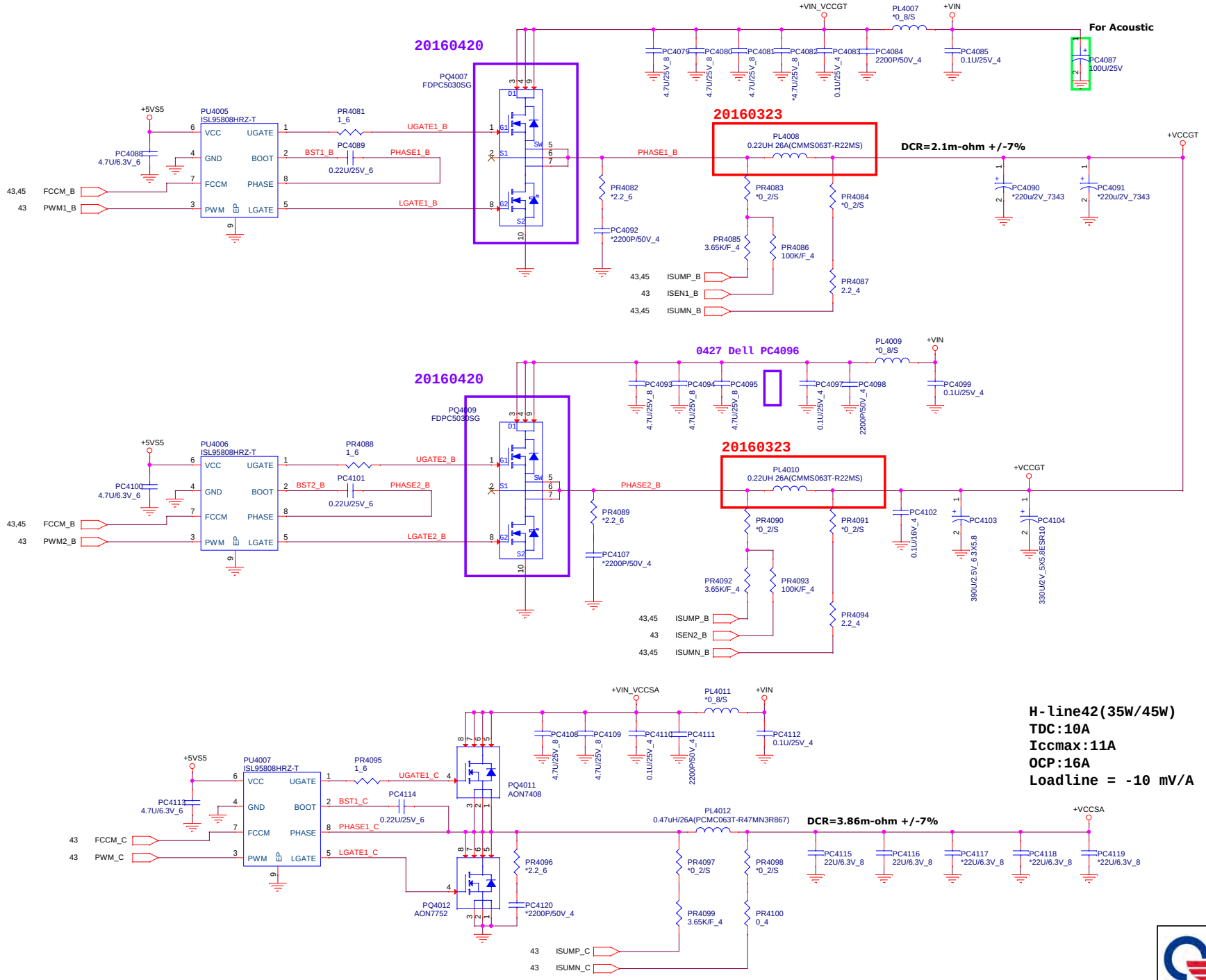

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VCCGT/SA (ISL95808HRZ-T)	1A

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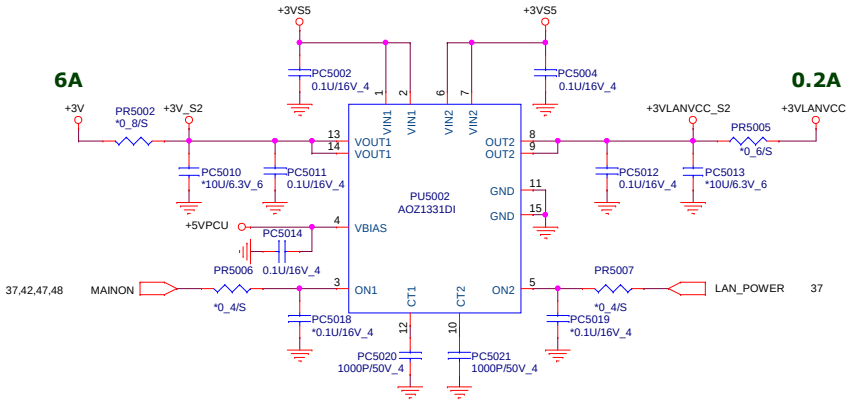

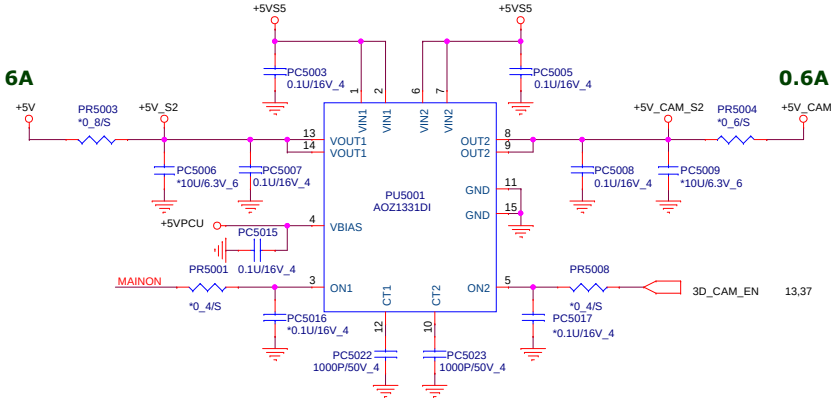

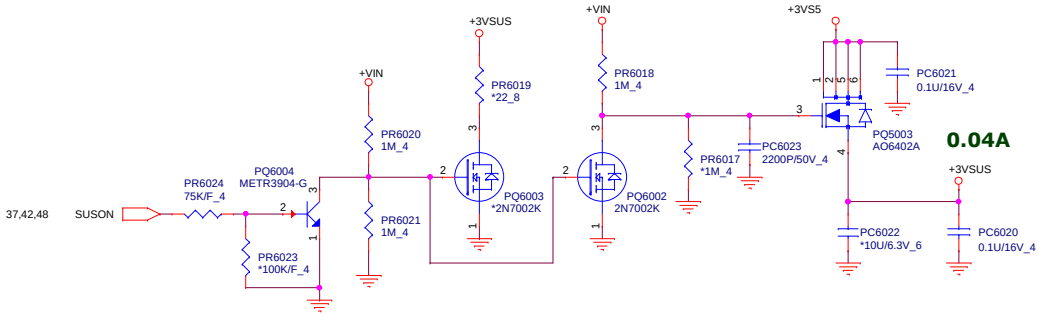

+3V	5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,54
+5V	26,27,28,29,31,32,38,49
+3VS5	10,12,14,16,33,37,41,42,47,48
+5VS5	10,28,30,41,42,43,44,45,47,48,49,51,53,54
+3VSUS	38
+3VLANVCC	35
+5V_CAM	31
+3V_DEEP_SUS	9,10,12,13,14,16,18

NB5

PROJECT : X1F

Quanta Computer Inc.

Size	Document Number	Rev
Custom	**Load switch IC (AOZ1331D)**	1A

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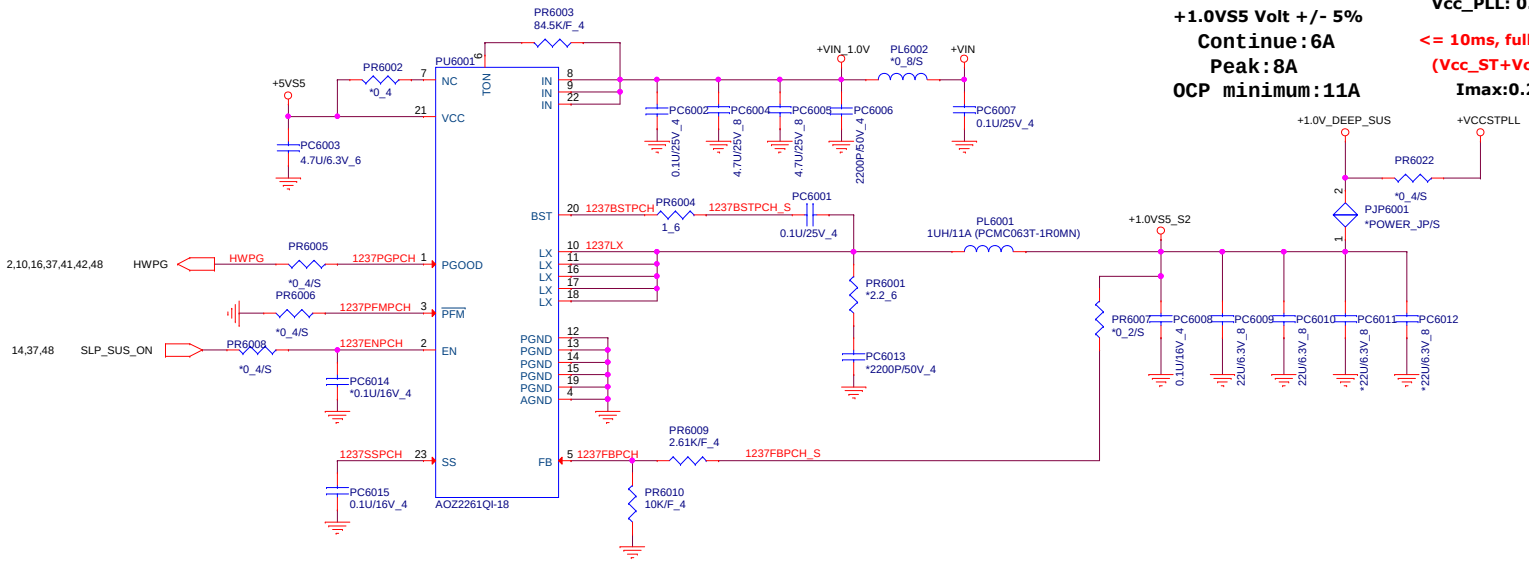
Volume Segment
Vcc_ST: 0.12A
Vcc_PLL: 0.12A

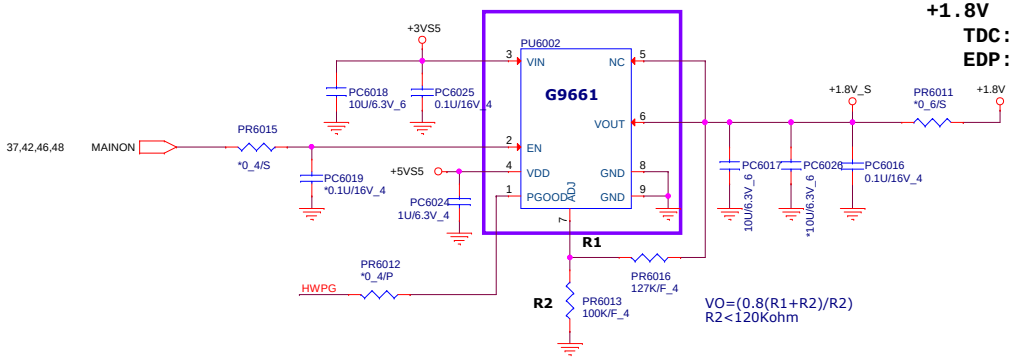
<= 10ms, full load ready
(Vcc_ST+Vcc_PLL)
Imax:0.24A

(V1.00A+V1.00_MODPHY+VccPRIM_CORE)
+1.0VS5 Volt +/- 5%
Continue:6A
Peak:8A
OCP minimum:11A



0607

+1.8V +/- 5%
TDC:1A
EDP:2A



+VIN 26,38,39,40,41,42,43,44,45,46,48,49,53,54
+3VS5 10,12,14,16,33,37,41,42,46,48
+5VS5 10,28,30,41,42,43,44,45,46,48,49,51,53,54
+1.0V_DEEP_SUS 10,11,14,16,48

+1.8V 22,28,31,51
+VCCSTPLL 2,6,43

NB5

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0_DEEP_SUS	1A
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Volume Segment
Vcc_STG: 0.04A
Vcc_IO: 5.5A

<= 10ms full load ready
Imax:5.5A

Imax:0.04A

<= 240us, full load ready
TDC:0.26A

Reserve for separating +1.0V and VCCIO

+0.95 +/- 5%
Continue:4A
Peak:5.5A
OCP minimum:8A

+1.0V 2,5,6,10,16,37
+3VS5 10,12,14,16,33,37,41,42,46,47
+5VS5 10,28,30,41,42,43,44,45,46,47,49,51,53,54
+VCCIO 3,6,16
+1.0V_DEEP_SUS 10,11,14,16,47
+1.2V_VCCPLL_OC 6
+1.2VSUS 2,6,10,17,18,42,51

PROJECT : X1F
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.0V/+VCCSTPLL/+VCCIO	1A

NB5

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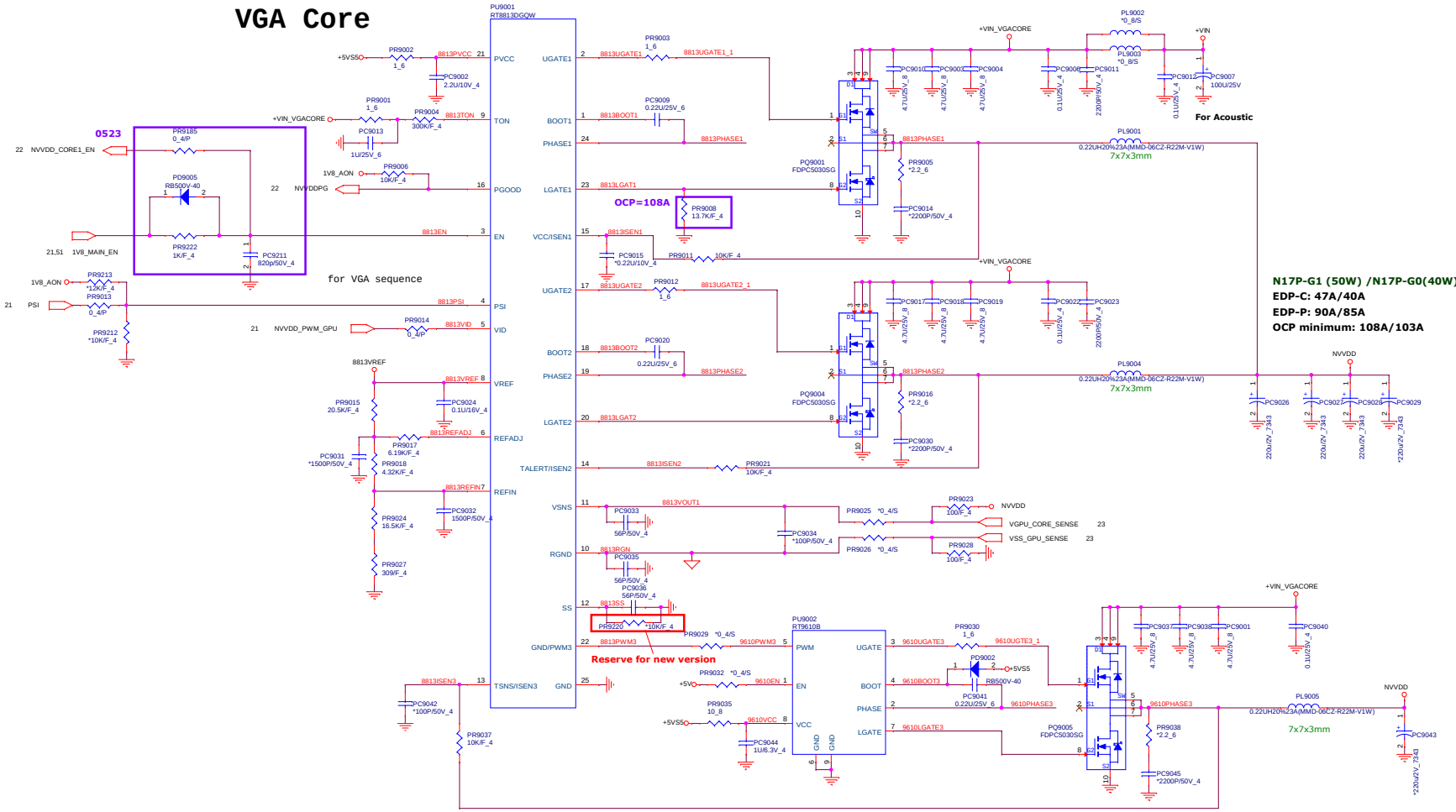
VGA Core



N17P-G1 (50W) /N17P-G0(40W)
EDP-C: 47A/40A
EDP-P: 90A/85A
OCP minimum: 108A/103A

NVDDS

1. Ripple Current:
Irip=7.79A

2. Ripple Voltage:
ESR/1=9mohm
Vrip=70.11mV

3.MOSFET Spec:
L-side MOSFET: FDPC5030
Rds(ON)=3mohm (Vgs=4.5 V)
I cont = 25A (T =25 ℃)
I pulse=503A

4. Frequency:
F=500KHz (PR9224=300k ohm)

5. OCP:
Set = PR9008 to 13.7K
Vtrip= PR9008*10uA-40mV=97V
Iocp=(Vtrip/Rdson) + Iripple/2
= 36.23A (1 phase)

Total OCP=36.23*3=108.6A (3 phase)

+3V 5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,46,54
+VIN 26,38,39,40,41,42,43,44,45,46,47,48,53,54
+5VS5 10,28,30,41,42,43,44,45,46,47,48,51,53,54

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A
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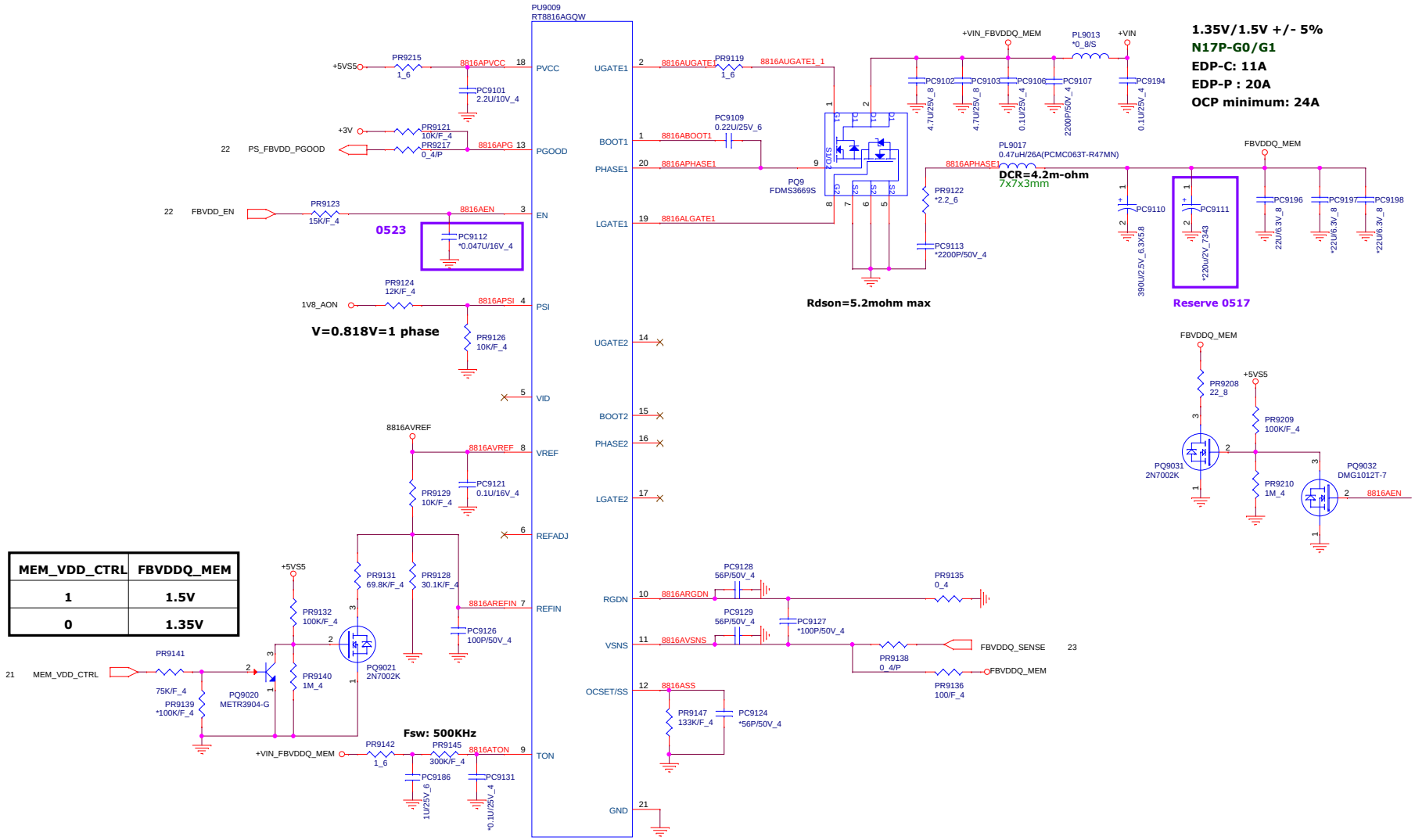

MEM_VDD_CTRL	FBVDDQ_MEM
1	1.5V
0	1.35V

FBVDDQ

1. Ripple Current:

Irip=5.34A Vo=1.35V
Irip=5.88A Vo=1.5V

2. Ripple Voltage:

ESR/1=9mohm
Vrip=48.06mV Vo=1.35
Vrip=53mV Vo=1.5

3.MOSFET Spec:

L-side MOSFET: FDMS3669S
Rds(ON)=5.2mohm (Vgs=4.5 V)
I cont = 18A (T =25 ℃)
I pulse=60A

4. Frequency:

F=500KHz (PR9145=300k ohm)

5. OCP:

Set = PR9147 to 133K Vo=1.35
Vtrip= PR9147*10uA/12=110.83mV
Iocp=(Vtrip/Rdson) + Iripple/2 = 24A

+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,53
+5VS5 10,28,30,41,42,43,44,45,46,47,48,49,51,53
FBVDDQ_MEM 20,22,23,24,25

NB5

PROJECT : G38A
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+1.35V_GFX (AOZ2263QI-18)	1A

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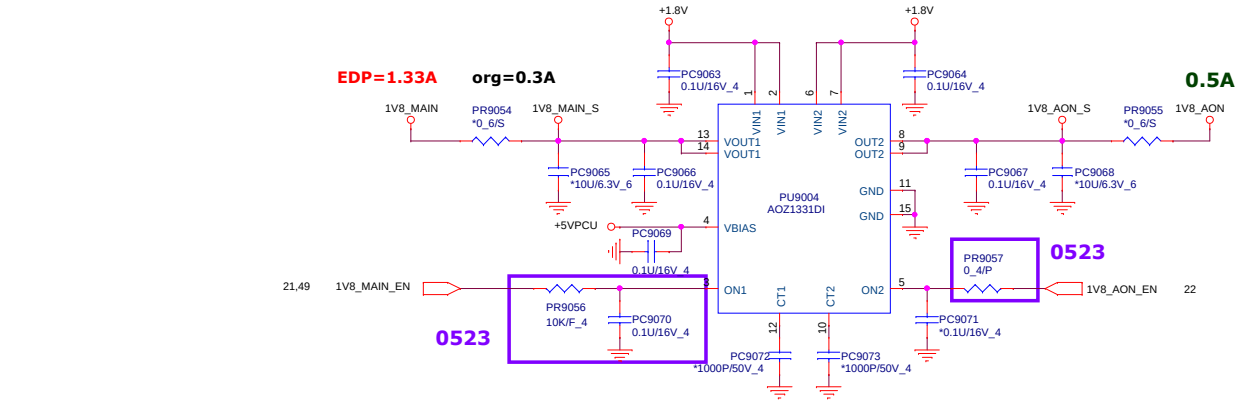
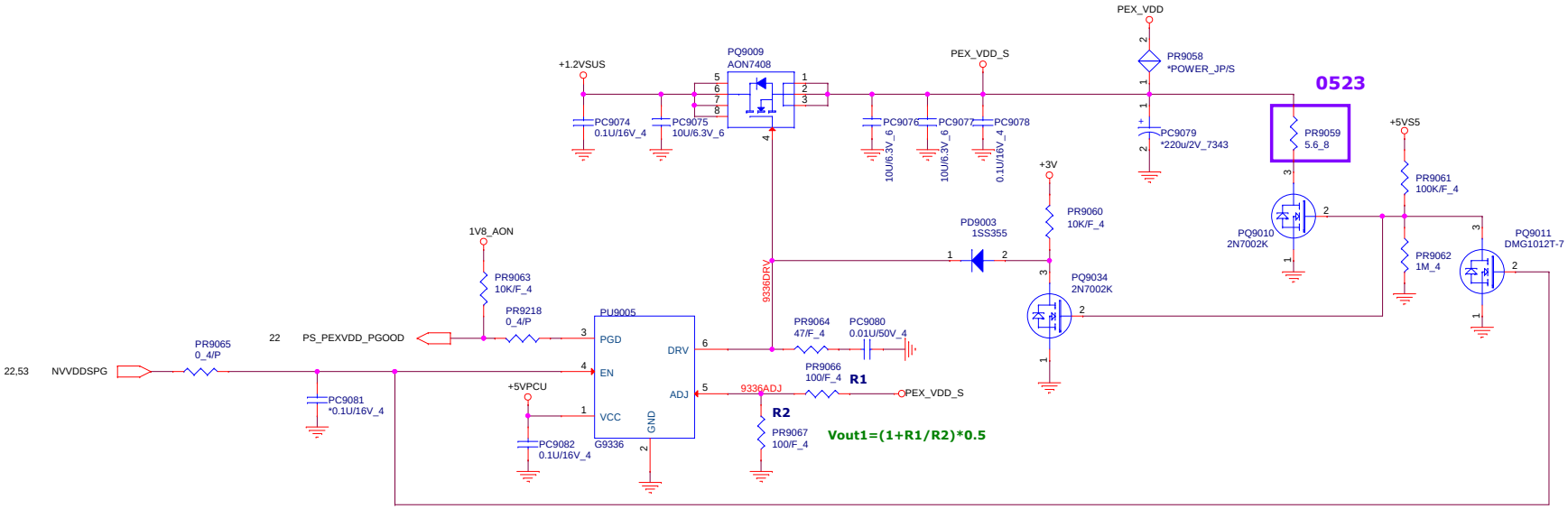


+1.05V_GFX Volt +/- 5%

EDP=3.31A

EDP_peak = TBD



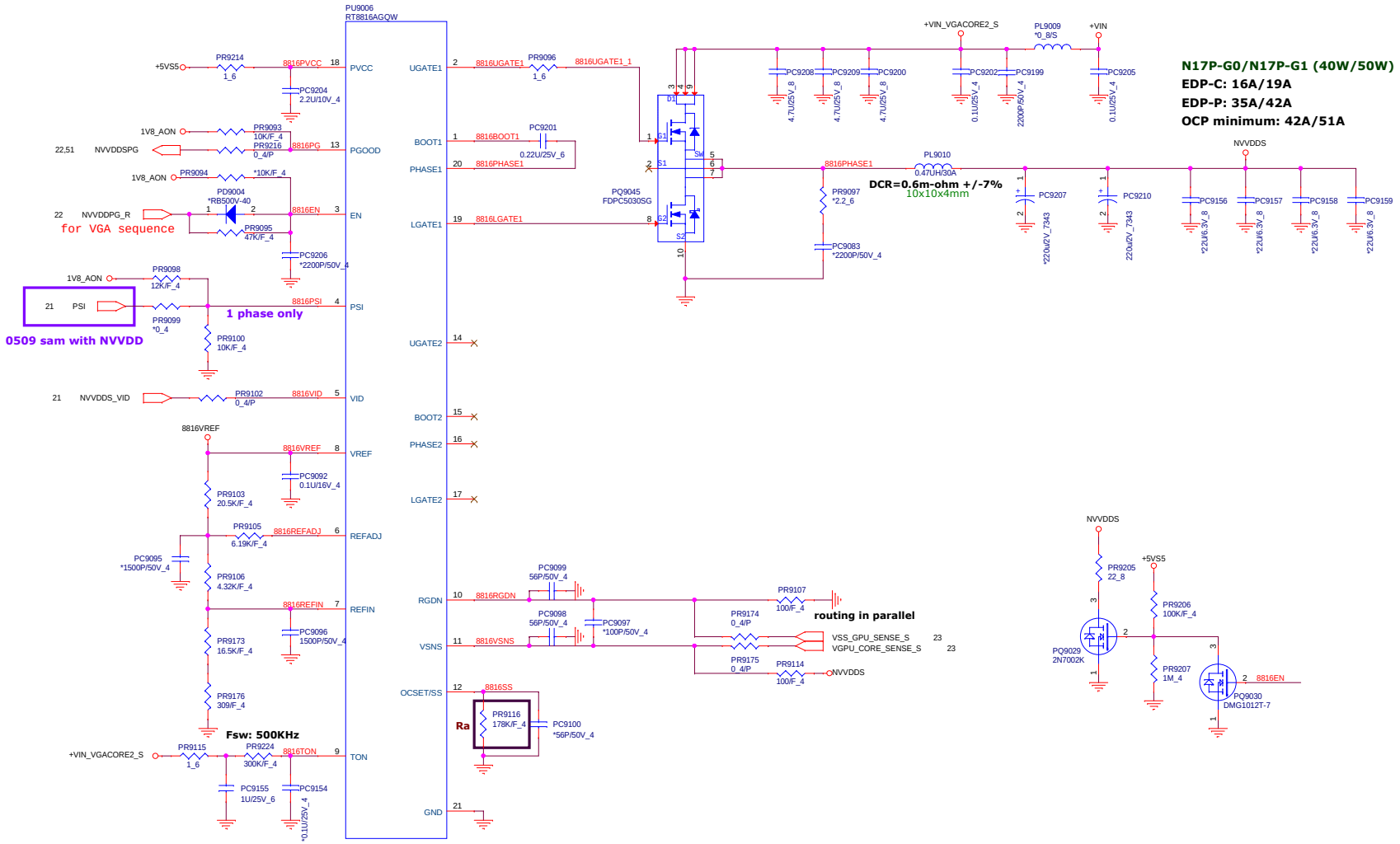
+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,53,54
+3VS5 10,12,14,16,33,37,41,42,46,47,48
+5VS5 10,28,30,41,42,43,44,45,46,47,48,49,53,54

+1.2VSUS 2,6,10,17,18,42,48

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+3V/+1.05V_GFX(AOZ1331DI)	1A
Date: Tuesday, June 07, 2016	Sheet 51 of 51	



NVDDS

1. Ripple Current:
   Irip=3.65A
2. Ripple Voltage:
   ESR/1=9mohm
   Vrip=32.85mV
3. Inductor Spec:
   Isat=40A
   Idc=30A
   DCR=1.68mohm
4. MOSFET Spec:
   H-side MOSFET: FDPC5030
   Rds(ON)=6.5mohm (Vgs=4.5 V)
   I cont = 17A (T =25 ℃)
   L-side MOSFET: FDPC5030
   Rds(ON)=3mohm (Vgs=4.5 V)
   I cont = 25A (T =25 ℃)
   I pulse=503A
5. Frequency:
   F=500KHz (PR9224=300k ohm)
6. OCP:
   Set = PR9116 to 178K
   Vtrip= PR9116*10uA/12=148.3mV
   Iocp=(Vtrip/Rdson) + Iripple/2 = 51.2A

+3V 5,9,10,11,12,13,14,16,17,18,26,27,28,29,30,32,33,34,35,36,37,38,43,46,54
+VIN 26,38,39,40,41,42,43,44,45,46,47,48,49,54
+5VS5 10,28,30,41,42,43,44,45,46,47,48,49,51,54
NVVDDS 23
1V8_AON 19,21,22,23,49,51,54

NB5

PROJECT : X1Q
Quanta Computer Inc.

Size	Document Number	Rev
Custom	+VGACORE (RT8813C)	1A

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