IMG5 20" REV G
11/16/05

H 437411 PRODUCTION RELEASED 04/28/06 ?

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41	58	KODIAC NBMEM PWR & CAPS		Q63	08/26/2005
42	59	Kodiak Memory Dq/Ctl		FINO-M23	08/26/2005
43	61	Parallel Term		FINO-M23	08/26/2005
44	62	Main Memory Clock Buffer		FINO-M23	08/26/2005
45	63	MEMORY ADDR BRANCHING		FINO-M23	08/26/2005
46	67	Memory Dimm A		FINO-M23	08/26/2005
47	68	MLB Mem Series Term		FINO-M23	08/26/2005
48	69	On-Board DDR SDRAM		FINO-M23	08/26/2005
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50	82	KODIAK PCI-E X16		Q63	08/26/2005
51	84	GPU PCIe		FINO-M23	08/18/2005
52	85	Graphics Vregs		M33-DD	06/20/2005
53	86	GPU Core Power		FINO-M23	10/07/2005
54	87	GPU Frame Buffer		FINO-M23	10/07/2005
55	88	FB Series Termination		FINO-M23	08/26/2005
56	89	GPU GDDR SDRAM A		FINO-M23	10/07/2005
57	90	GPU GDDR SDRAM B		FINO-M23	10/07/2005
58	91	FB Parallel Termination		M33-DD	06/20/2005
59	92	GPU Straps		FINO-M23	08/26/2005
60	93	GPU DVI & DACs		FINO-M23	10/07/2005
61	96	TMDS / ExtVGA		M33-DD	06/20/2005
62	97	KODIAK PCI-E CONST		FINO-M23	08/26/2005
63	98	KODIAK HT16		Q63	08/26/2005
64	101	HT ALIASES		FINO-M23	08/26/2005
65	103	Shasta HyperTransport		Q63	08/26/2005
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69	122	USB 2.0 PCI Interface		Q63	08/26/2005
70	125	BootROM		Q63	08/26/2005
71	127	Shasta Disk		M33-DC	06/20/2005
72	129	Disk Connectors		M33-DC	06/20/2005
73	130	ENET SERIES TERM		FINO-M23	08/26/2005
74	131	Shasta Ethernet		Q63	08/26/2005
75	132	Vesta Ethernet PHY		Q63	08/26/2005
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78	139	Vesta FireWire PHY		Q63	08/26/2005
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84	147	AUDIO: CODEC		FINO-SO	10/07/2005
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86	150	AUDIO: LINE OUT AMP		FINO-SO	10/07/2005
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89	154	AUDIO: POWER SUPPLIES		FINO-SO	10/07/2005

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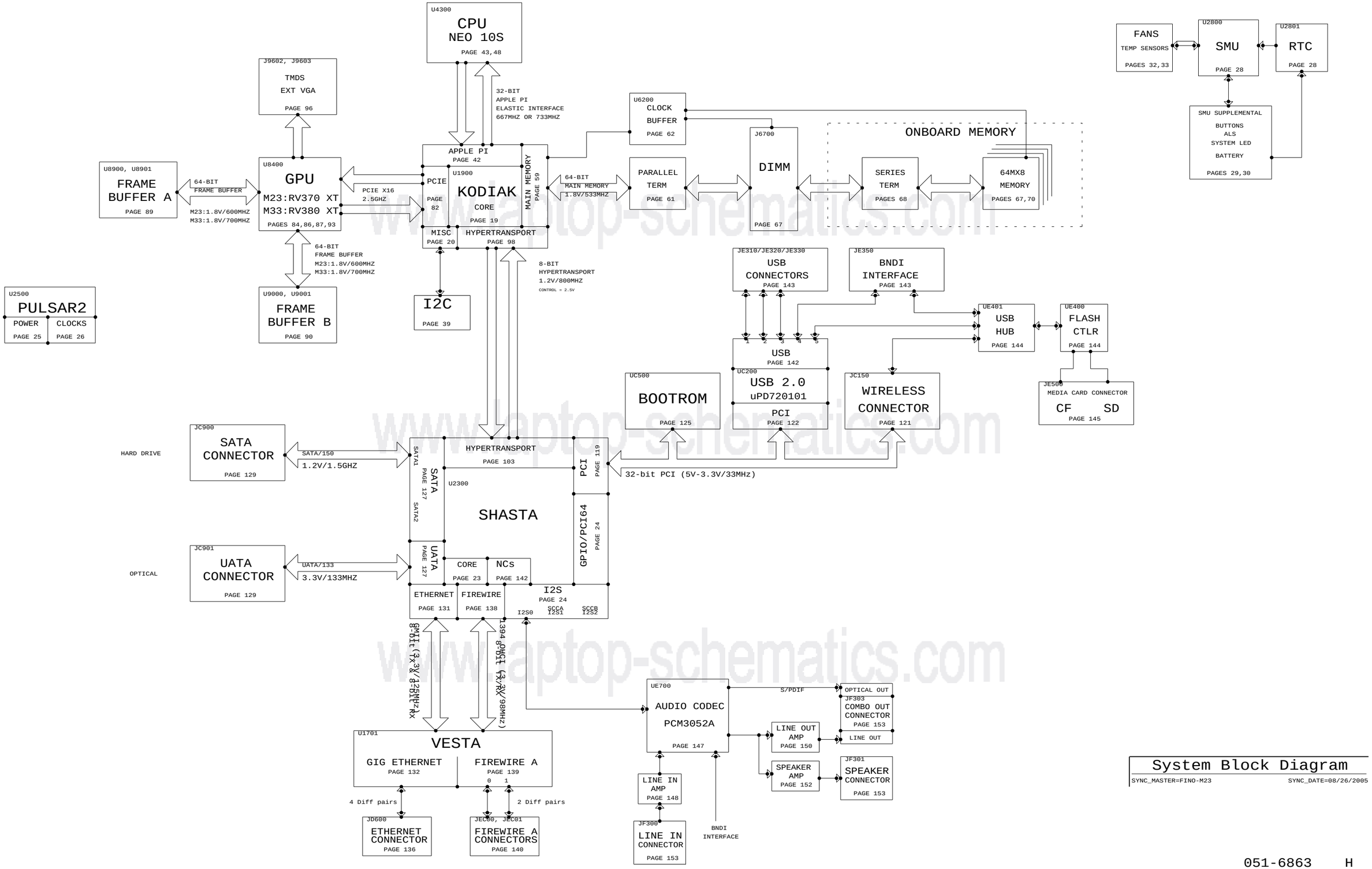

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System Block Diagram

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POWER CONNECTOR

J700
PAGE 7

PP12V_ALL — FW CONN
PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER
PP5V_RUN — OPTICAL
PP5V_ALL
PP3V3_ALL — PCI BUS, AUDIO CODEC
PP3V3_RUN
SYS_POWERUP_L

SMU
SYS_POWERUP_L
POWER SEQUENCE PIN
NC_SMU_PWRSEQ_P1_0
NC_SMU_PWRSEQ_P1_4
SMU_PWRSEQ_P1_0
SMU_PWRSEQ_P1_4
TURN_ON_PP1V2_L
SMU_PWRSEQ_P1_1
PWR_GOOD_PP1V5
SMU_PWRSEQ_P9_5
PWR_GOOD_PP1V8
SMU_PWRSEQ_P9_6
TURN_ON_PP3V3_PWRON_L
SMU_PWRSEQ_P1_2
SMU_PWRSEQ_P1_3

PP1V5_PWRON SWITCHER — PAGE 12 — PULSAR, KODIAK CORE
PP1V5_RUN FET SWITCH — PAGE 12 — EI
CPU CORE SWITCHER — PAGE 50
PP4V5_RUN_AUDIO LINEAR — PAGE 154 — AUDIO CODEC
PP5V_PWRON FET SWITCH — PAGE 16 — USB CONN
PP3V3_PWRON FET SWITCH — PAGE 16 — MODEM & BT, USB2 HOST
PP2V5_RUN_CPU_AVDD LINEAR — PAGE 54
PP2V5_GPU_A2VDD LINEAR — PAGE 85
PP1V2_ALL SWITCHER — PAGE 13 — VESTA CORE
GPU CORE SWITCHER — PAGE 85
PP1V8_PWRON SWITCHER — PAGE 11 — MAIN MEMORY
PP1V8_RUN POWER SW — PAGE 11 — GPU MEMORY
PP0V9_GPU_VTT LINEAR — PAGE 91
PP2V5_ALL LINEAR — PAGE 15 — VESTA
PP1V8_TPVDD LINEAR — PAGE 85
PP1V5_VDDC_CT LINEAR — PAGE 85
PP1V2_TPVDD LINEAR — PAGE 85
PP1V8_GPU LINEAR — PAGE 85
PP1V2_PWRON FET SWITCH — PAGE 13 — SHASTA CORE
PP1V2_RUN FET SWITCH — PAGE 13 — HT BUS
PP2V5_PWRON FET SWITCH — PAGE 15
PP2V5_RUN FET SWITCH — PAGE 15

PP2V5_ALL PVDD
R431 10K RES 5% 1/16W MF-LF 402
PP1V5_PWRON PVDD
R430 100K RES 5% 1/16W MF-LF 402
PS_1V_REF
COMPARE_PP1V5
C430 CAP 0.01UF 20% 16V X7R CERM 402
GND
U400 COMPARATOR_LM339A
SOI-LF
R440 100K RES 5% 1/16W MF-LF 402
COMPARE_PP1V8
C440 CAP 0.01UF 20% 16V X7R CERM 402
R442 150K RES 5% 1/16W MF-LF 402
R443 100K RES 5% 1/16W MF-LF 402
PP5V_ALL PVDD
R441 10K RES 5% 1/16W MF-LF 402
C441 CAP 0.1UF 20% 10V X5R CERM 402
U400P2

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Power Block Diagram

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NO TEST XW NETS

I947	NO_TEST=YES	GND_U1100	11
I948	NO_TEST=YES	GND_U1200	12
I949	NO_TEST=YES	GND_U1300	13
I950	NO_TEST=YES	PP_2V5PWRONNBMISC	20
I951	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
I952	NO_TEST=YES	PP_3V3PWRONSBPCI64	23
I953	NO_TEST=YES	PP_2V5PWRONSB	23
I954	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
I955	NO_TEST=YES	PP_OVDD_PULSAR1	25
I956	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
I957	NO_TEST=YES	PP_1V5PULSAR2	25
I958	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
I959	NO_TEST=YES	GND_SMU_AVSS	28 55
I960	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
I961	NO_TEST=YES	PP_3V3ALLSMU	28
I962	NO_TEST=YES	PP_VEINB	41
I963	NO_TEST=YES	GND_CPU_AVDD	48
I964	NO_TEST=YES	VC_AGND	50
I965	NO_TEST=YES	VC_OUTSEN_R	50
I966	NO_TEST=YES	KPVDD2_FMAX	55
I967	NO_TEST=YES	GND_GPU_PVSS	86
I968	NO_TEST=YES	GND_GPU_MPVSS	87
I969	NO_TEST=YES	GND_AUDIO_MIC	153 154

I970	NO_TEST=YES	GND_GPU_TPVSS	93
I971	NO_TEST=YES	GND_GPU_TXVSSR	93
I972	NO_TEST=YES	GND_GPU_VSSDI	93
I973	NO_TEST=YES	GND_GPU_AVSSN	93
I974	NO_TEST=YES	GND_GPU_AVSSQ	93
I975	NO_TEST=YES	GND_GPU_A2VSSN	93
I976	NO_TEST=YES	GND_GPU_A2VSSQ	93
I977	NO_TEST=YES	KOD_L15_GND	98 101
I978	NO_TEST=YES	PP_3V3SBPCI_B9	
I979	NO_TEST=YES	PP_2V5PWRONSB_B9	119
I980	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
I981	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
I982	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
I983	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
I984	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
I985	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
I986	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
I987	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
I988	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
I989	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
I990	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
I991	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
I992	NO_TEST=YES	GND_AUD_LOAMP	150 154

I993	NO_TEST=YES	GND_NEC_AVSS_R	142
I994	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
I995	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
I996	NO_TEST=YES	KPGND2_FMAX	55
I997	NO_TEST=YES	TDIODE_POS_FMAX	55
I998	NO_TEST=YES	TDIODE_NEG_FMAX	55
I999	NO_TEST=YES	DAGND	55
I1000	NO_TEST=YES	INA138_OUT	55
I1001	NO_TEST=YES	RAMCLK_AVSS	62
I1002	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
I1003	NO_TEST=YES	GND_AUDIO	7 154
I1004	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
I1005	NO_TEST=YES	KOD_H05_GND	82 97
I1006	NO_TEST=YES	KOD_K07_GND	82 97
I1007	NO_TEST=YES	KOD_G10_GND	82 97
I1008	NO_TEST=YES	KOD_J13_GND	82 97
I1009	NO_TEST=YES	KOD_L13_GND	82 97
I1010	NO_TEST=YES	KOD_H08_GND	82 97
I1011	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
I1012	NO_TEST=YES	U8500_GND	85
I1013	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

I955	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
I956	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
I958	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
I959	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
I960	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
I961	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
I962	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
I963	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
I964	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
I966	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56
I969	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
I972	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
I972	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
I973	NO_TEST=YES	NC_CPU_A1_QACK_L	56
I975	NO_TEST=YES	NC_CPU_B0_QACK_L	56
I974	NO_TEST=YES	NC_CPU_B1_QACK_L	56
I976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
I978	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
I977	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
I982	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
I104	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
I104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
I105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
I105	NO_TEST=YES	NC_A_AVREG_0	82
I105	NO_TEST=YES	NC_A_AVREG_1	82
I105	NO_TEST=YES	NC_A_AVREG_2	82
I105	NO_TEST=YES	NC_CPU_B_APSYNC	27
I105	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
I106	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
I105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
I105	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
I106	NO_TEST=YES	NC_J2904_11	29
I106	NO_TEST=YES	NC_J2904_12	29
I106	NO_TEST=YES	NC_NCV1009_1	55
I106	NO_TEST=YES	NC_NCV1009_2	55
I106	NO_TEST=YES	NC_NCV1009_3	55
I106	NO_TEST=YES	NC_NCV1009_4	55
I106	NO_TEST=YES	NC_NCV1009_5	55
I106	NO_TEST=YES	NC_NCV1009_ADJ	55
I106	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
I106	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
I107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
I107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4
I116	NO_TEST=YES	RFBD<38>	88 89
I116	NO_TEST=YES	RFBD<37>	88 89
I116	NO_TEST=YES	RFBD<36>	88 89
I116	NO_TEST=YES	RFBD<34>	88 89
I116	NO_TEST=YES	RFBD<33>	88 89
I116	NO_TEST=YES	RFBD<32>	88 89
I116	NO_TEST=YES	RFBD<31>	88 89
I116	NO_TEST=YES	RFBD<30>	88 89
I117	NO_TEST=YES	RFBD<28>	88 89
I117	NO_TEST=YES	RFBD<27>	88 89
I117	NO_TEST=YES	RFBD<26>	88 89
I117	NO_TEST=YES	RFBD<25>	88 89
I117	NO_TEST=YES	RFBD<23>	88 89
I117	NO_TEST=YES	RFBD<22>	88 89
I117	NO_TEST=YES	RFBD<21>	88 89

I109	NO_TEST=YES	KPVDD2	48 50 55
I109	NO_TEST=YES	KPGND2	48 50 55
I109	NO_TEST=YES	CPU_DIODE_POS	48 55
I109	NO_TEST=YES	CPU_DIODE_NEG	48 55
I110	NO_TEST=YES	FMAXT_P	55
I110	NO_TEST=YES	FMAXT_M	55
I110	NO_TEST=YES	CORE_ISNS_P	55
I110	NO_TEST=YES	CORE_ISNS_M	55
I110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
I110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
I110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
I110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
I110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
I110	NO_TEST=YES	NC_I2S2_MCLK	154
I111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
I111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
I111	NO_TEST=YES	NC_SATA_TXD_N2	129
I111	NO_TEST=YES	NC_SATA_TXD_P2	129
I111	NO_TEST=YES	TP_SB<29>	142
I111	NO_TEST=YES	TP_SB<28>	142
I111	NO_TEST=YES	TP_SB<27>	142
I111	NO_TEST=YES	TP_SB<26>	142
I111	NO_TEST=YES	TP_SB<25>	142
I112	NO_TEST=YES	TP_SB<24>	142
I112	NO_TEST=YES	TP_SB<23>	142
I112	NO_TEST=YES	TP_SB<22>	142
I112	NO_TEST=YES	TP_SB<21>	142
I112	NO_TEST=YES	TP_SB<20>	142
I112	NO_TEST=YES	TP_SB<19>	142
I112	NO_TEST=YES	TP_SB<18>	142
I112	NO_TEST=YES	TP_SB<17>	142
I112	NO_TEST=YES	TP_SB<16>	142
I112	NO_TEST=YES	TP_SB<15>	142
I113	NO_TEST=YES	TP_SB<14>	142
I113	NO_TEST=YES	TP_SB<13>	142
I113	NO_TEST=YES	TP_SB<12>	142
I113	NO_TEST=YES	TP_SB<11>	142
I113	NO_TEST=YES	TP_SB<10>	142
I113	NO_TEST=YES	TP_SB<9>	142
I113	NO_TEST=YES	TP_SB<8>	142
I113	NO_TEST=YES	TP_SB<7>	142
I113	NO_TEST=YES	TP_SB<6>	142
I113	NO_TEST=YES	TP_SB<5>	142
I114	NO_TEST=YES	TP_SB<4>	142
I114	NO_TEST=YES	TP_SB<3>	142
I114	NO_TEST=YES	TP_SB<2>	142
I114	NO_TEST=YES	TP_SB<1>	142
I114	NO_TEST=YES	TP_SB<0>	142
I115	NO_TEST=YES	RFBD<61>	88 89
I115	NO_TEST=YES	RFBD<60>	88 89
I115	NO_TEST=YES	RFBD<59>	88 89
I117	NO_TEST=YES	RFBD<57>	88 89
I118	NO_TEST=YES	RFBD<56>	88 89
I118	NO_TEST=YES	RFBD<54>	88 89
I118	NO_TEST=YES	RFBD<53>	88 89
I118	NO_TEST=YES	RFBD<52>	88 89
I118	NO_TEST=YES	RFBD<50>	88 89
I118	NO_TEST=YES	RFBD<49>	88 89
I118	NO_TEST=YES	RFBD<48>	88 89
I118	NO_TEST=YES	RFBD<47>	88 89
I119	NO_TEST=YES	RFBD<45>	88 89
I119	NO_TEST=YES	RFBD<44>	88 89
I119	NO_TEST=YES	RFBD<42>	88 89
I119	NO_TEST=YES	RFBD<41>	88 89
I119	NO_TEST=YES	RFBD<40>	88 89

I110	NO_TEST=YES	RFBD<126>	88 90
I120	NO_TEST=YES	RFBD<125>	88 90
I110	NO_TEST=YES	RFBD<124>	88 90
I120	NO_TEST=YES	RFBD<122>	88 90
I120	NO_TEST=YES	RFBD<121>	88 90
I120	NO_TEST=YES	RFBD<120>	88 90
I120	NO_TEST=YES	RFBD<118>	88 90
I120	NO_TEST=YES	RFBD<117>	88 90
I120	NO_TEST=YES	RFBD<116>	88 90
I121	NO_TEST=YES	RFBD<114>	88 90
I121	NO_TEST=YES	RFBD<113>	88 90
I121	NO_TEST=YES	RFBD<112>	88 90
I121	NO_TEST=YES	RFBD<110>	88 90
I121	NO_TEST=YES	RFBD<109>	88 90
I121	NO_TEST=YES	RFBD<108>	88 90
I121	NO_TEST=YES	RFBD<106>	88 90
I122	NO_TEST=YES	RFBD<105>	88 90
I121	NO_TEST=YES	RFBD<104>	88 90
I122	NO_TEST=YES	RFBD<102>	88 90
I122	NO_TEST=YES	RFBD<101>	88 90
I122	NO_TEST=YES	RFBD<100>	88 90
I122	NO_TEST=YES	RFBD<98>	88 90
I122	NO_TEST=YES	RFBD<97>	88 90
I122	NO_TEST=YES	RFBD<96>	88 90
I122	NO_TEST=YES	RFBD<95>	88 90
I120	NO_TEST=YES	RFBD<94>	88 90
I120	NO_TEST=YES	RFBD<92>	88 90
I120	NO_TEST=YES	RFBD<91>	88 90
I120	NO_TEST=YES	RFBD<90>	88 90
I120	NO_TEST=YES	RFBD<88>	88 90
I120	NO_TEST=YES	RFBD<87>	88 90
I120	NO_TEST=YES	RFBD<86>	88 90
I120	NO_TEST=YES	RFBD<85>	88 90
I120	NO_TEST=YES	RFBD<83>	88 90
I120	NO_TEST=YES	RFBD<82>	88 90
I120	NO_TEST=YES	RFBD<81>	88 90
I120	NO_TEST=YES	RFBD<79>	88 90
I120	NO_TEST=YES	RFBD<78>	88 90
I120	NO_TEST=YES	RFBD<76>	88 90
I120	NO_TEST=YES	RFBD<75>	88 90
I120	NO_TEST=YES	RFBD<74>	88 90
I120	NO_TEST=YES	RFBD<72>	88 90
I120	NO_TEST=YES	RFBD<71>	88 90
I120	NO_TEST=YES	RFBD<70>	88 90
I120	NO_TEST=YES	RFBD<69>	88 90
I120	NO_TEST=YES	RFBD<67>	88 90
I120	NO_TEST=YES	RFBD<66>	88 90
I120	NO_TEST=YES	RFBD<65>	88 90
I120	NO_TEST=YES	RFBD<62>	88 89

I820	NO_TEST=YES	TP_FBBCS1_L	87
I826	NO_TEST=YES	AUD_4V5_FB	154
I837	NO_TEST=YES	ITS_RUNNING	7
I838	NO_TEST=YES	LED801_1	8
I839	NO_TEST=YES	LED802_1	8
I844	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
I845	NO_TEST=YES	Q800_D	8
I846	NO_TEST=YES	Q800_G	8
I847	NO_TEST=YES	Q801_B	8
I848	NO_TEST=YES	Q802_B	8
I849	NO_TEST=YES	Q802_E	8
I850	NO_TEST=YES	Q803_B	8
I851	NO_TEST=YES	TP_USB2_PWREN<0>	143
I852	NO_TEST=YES	TP_USB2_PWREN<1>	143
I853	NO_TEST=YES	TP_SB_FSTEST	24
I857	NO_TEST=YES	TP_SB_PLLTEST	24
I854	NO_TEST=YES	TP_USB2_PWREN<2>	143
I855	NO_TEST=YES	TP_USB2_PWREN<3>	143
I856	NO_TEST=YES	TP_USB2_PWREN<4>	143
I857	NO_TEST=YES	TP_NEC_NTEST1	122
I858	NO_TEST=YES	TP_NEC_SMC	122
I859	NO_TEST=YES	TP_NEC_SMI_L	122
I860	NO_TEST=YES	TP_NEC_SRCLK	122
I861	NO_TEST=YES	TP_NEC_SRMOD	122
I862	NO_TEST=YES	TP_NEC_TEST	122
I863	NO_TEST=YES	UATA_DASP_L_DS	129
I126	NO_TEST=YES	RFBD<19>	88 89
I126	NO_TEST=YES	RFBD<18>	88 89
I126	NO_TEST=YES	RFBD<16>	88 89
I126	NO_TEST=YES	RFBD<15>	88 89
I126	NO_TEST=YES	RFBD<14>	88 89
I126	NO_TEST=YES	RFBD<13>	88 89
I127	NO_TEST=YES	RFBD<11>	88 89
I127	NO_TEST=YES	RFBD<10>	88 89
I127	NO_TEST=YES	RFBD<8>	88 89
I127	NO_TEST=YES	RFBD<7>	88 89
I127	NO_TEST=YES	RFBD<6>	88 89
I127	NO_TEST=YES	RFBD<5>	88 89
I127	NO_TEST=YES	RFBD<3>	88 89
I128	NO_TEST=YES	RFBD<2>	88 89
I128	NO_TEST=YES	RFBD<1>	88 89
I128	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
I129	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<37>	61 68 70
I130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
I131	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
I131	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
I131	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
I131	NO_TEST=YES	RAM_DQ_R<31>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
I132	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
I133	NO_TEST=YES	RAM_DQ_R<11>	61 68 69

FUNC TEST NETS

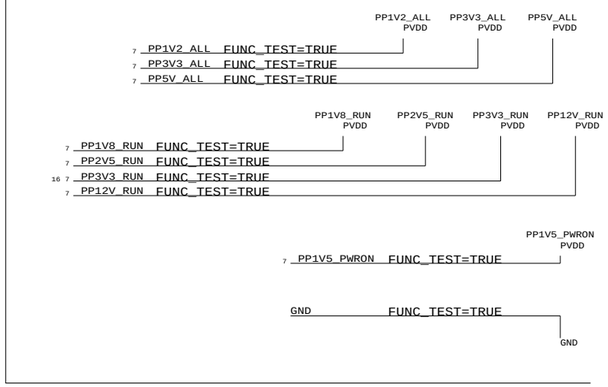
NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

I100	FUNC_TEST=TRUE	PPVCORE_CPU	50
I101	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
I102	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
I103	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
I104	FUNC_TEST=TRUE	POWER_BUTTON_L	29
I105	FUNC_TEST=TRUE	RESET_BUTTON_L	29
I106	FUNC_TEST=TRUE	SMU_RESET_L	28 29
I107	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

I133	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
I133	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
I133	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
I133	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
I133	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
I133	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
I105	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29



I134	NO_TEST=YES	RAM_DQ_R<9>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
I135	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST 1 OF 2

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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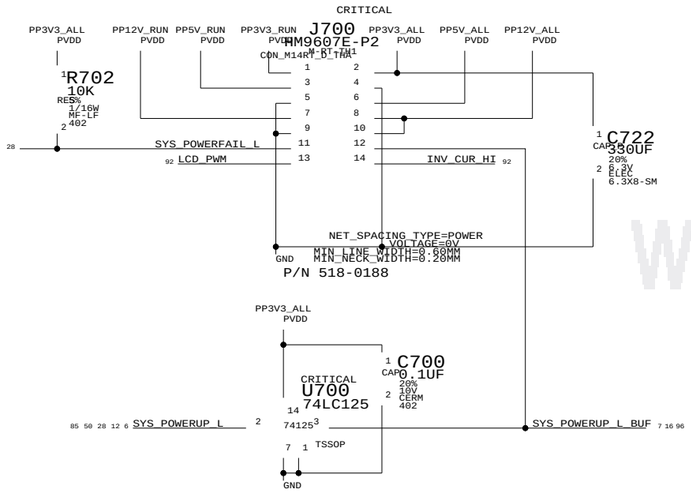
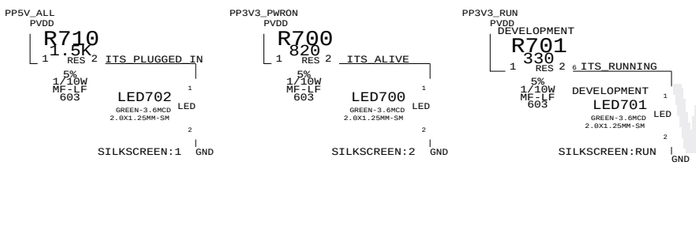
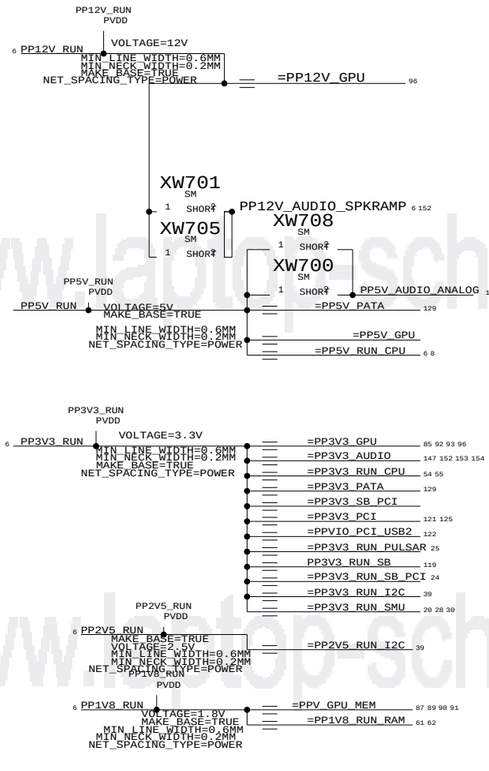
RUN RAILS

ONLY ON IN RUN

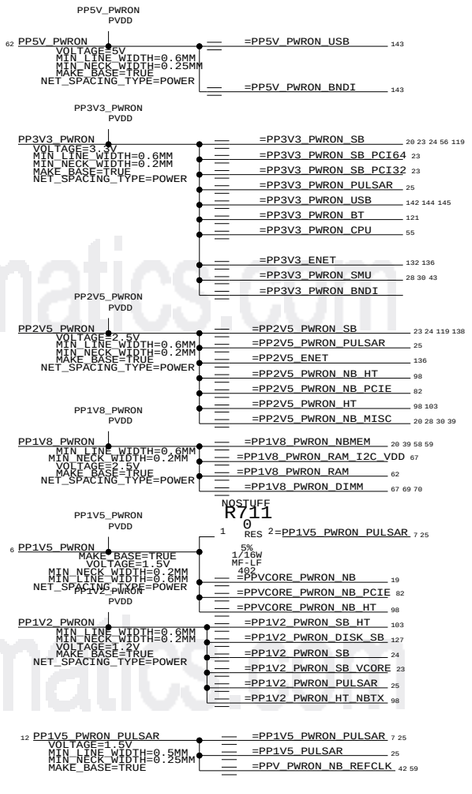






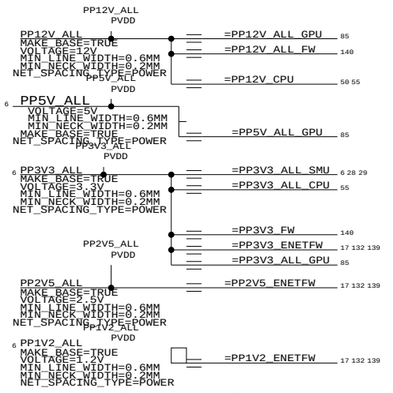
PWRON RAILS

ON IN RUN AND SLEEP

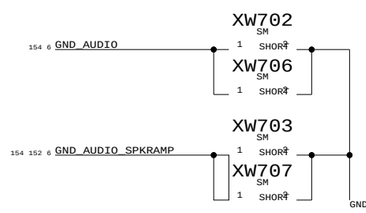


ALL RAILS

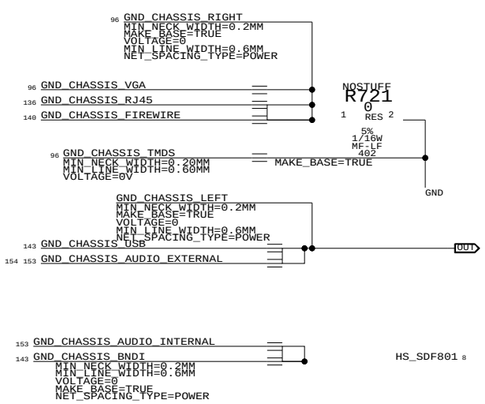
ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

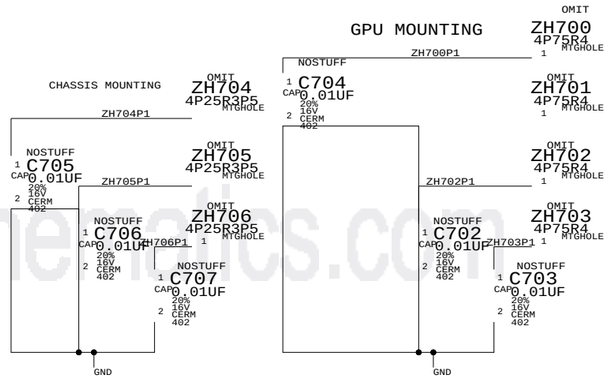


GND RAILS



CHASSIS GND





POWER CONN / ALIAS

SYNC_MASTER=M33-PC SYNC_DATE=06/20/2005

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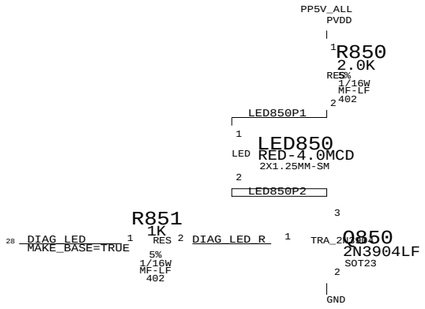
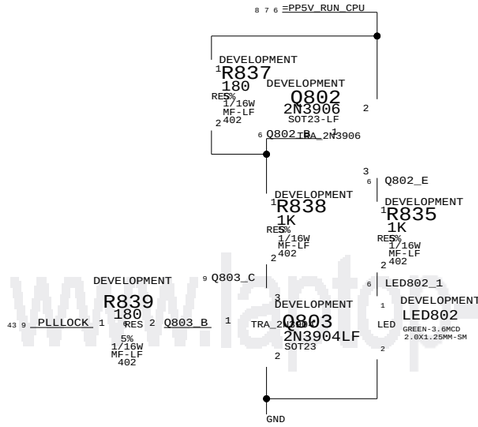
DIAG LED

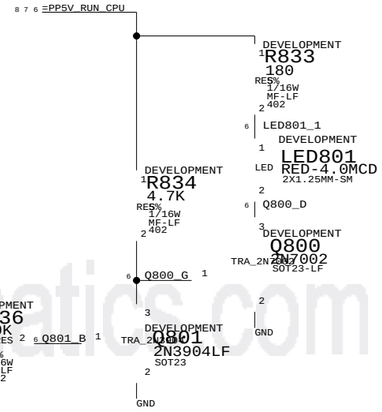
(OVERTEMP LED)



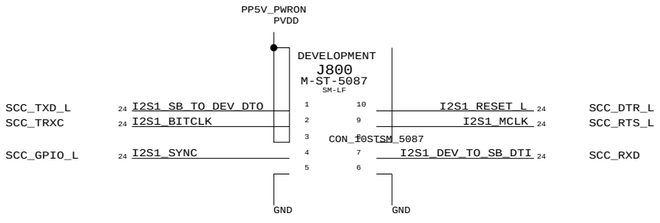
PLL LOCK LED



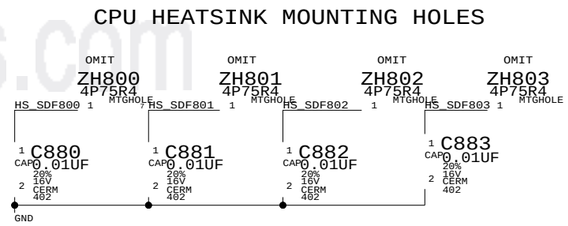
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005

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I1	NO_TEST=YES	ENET_TXD_R<7>	130 131
I2	NO_TEST=YES	ENET_TXD_R<6>	130 131
I3	NO_TEST=YES	ENET_TXD_R<5>	130 131
I4	NO_TEST=YES	ENET_TXD_R<4>	130 131
I5	NO_TEST=YES	ENET_TXD_R<3>	130 131
I6	NO_TEST=YES	ENET_TXD_R<2>	130 131
I7	NO_TEST=YES	ENET_TXD_R<1>	130 131
I8	NO_TEST=YES	ENET_TXD_R<0>	130 131
I9	NO_TEST=YES	ENET_TXD<7>	130 131 132
I10	NO_TEST=YES	ENET_TXD<6>	130 131 132
I12	NO_TEST=YES	ENET_TXD<5>	130 131 132
I11	NO_TEST=YES	ENET_TXD<4>	130 131 132
I13	NO_TEST=YES	ENET_TXD<3>	130 131 132
I14	NO_TEST=YES	ENET_TXD<2>	130 131 132
I15	NO_TEST=YES	ENET_TXD<1>	130 131 132
I16	NO_TEST=YES	ENET_TXD<0>	130 131 132
I18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
I17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
I19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
I20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
I21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
I22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
I24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
I23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
I25	NO_TEST=YES	ENET_RXD<7>	130 131
I26	NO_TEST=YES	ENET_RXD<6>	130 131
I27	NO_TEST=YES	ENET_RXD<5>	130 131
I28	NO_TEST=YES	ENET_RXD<4>	130 131
I30	NO_TEST=YES	ENET_RXD<3>	130 131
I29	NO_TEST=YES	ENET_RXD<2>	130 131
I31	NO_TEST=YES	ENET_RXD<1>	130 131
I32	NO_TEST=YES	ENET_RXD<0>	130 131
I33	NO_TEST=YES	ENET_TX_EN_R	130 131
I34	NO_TEST=YES	ENET_TX_ER_R	130 131
I36	NO_TEST=YES	ENET_TX_EN	130 131 132
I35	NO_TEST=YES	ENET_TX_ER	130 131 132
I37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
I38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
I39	NO_TEST=YES	NC_CPU_AFN	56
I40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
I42	NO_TEST=YES	NC_PSRO	56
I41	NO_TEST=YES	NC_PSRO_ENABLE	56
I43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
I44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
I45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
I46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
I48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
I47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
I49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
I50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
I51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
I52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
I54	NO_TEST=YES	NC_SMU_SER_SEL	31
I53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
I55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
I56	NO_TEST=YES	TP_VESTA_AN_EN	132
I57	NO_TEST=YES	TP_VESTA_DNC_C9	17
I58	NO_TEST=YES	TP_VESTA_DNC_E9	17
I60	NO_TEST=YES	TP_VESTA_EN_10B	132
I59	NO_TEST=YES	TP_VESTA_ER	132
I61	NO_TEST=YES	TP_VESTA_F1000	132
I62	NO_TEST=YES	TP_VESTA_FDX	132
I63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
I64	NO_TEST=YES	TP_VESTA_HUB	132
I66	NO_TEST=YES	TP_VESTA_LINK1_L	132
I65	NO_TEST=YES	TP_VESTA_LINK2_L	132
I67	NO_TEST=YES	TP_VESTA_MANMS	132
I68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
I69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
I70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
I72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
I71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
I73	NO_TEST=YES	TP_VESTA_RBC0	132
I74	NO_TEST=YES	TP_VESTA_RBC1	132
I75	NO_TEST=YES	TP_VESTA_REGCTL1	17
I76	NO_TEST=YES	TP_VESTA_REGCTL2	17
I78	NO_TEST=YES	TP_VESTA_REGSEN1	17
I77	NO_TEST=YES	TP_VESTA_REGSEN2	17
I79	NO_TEST=YES	TP_VESTA_REGSUP1	17
I80	NO_TEST=YES	TP_VESTA_REGSUP2	17
I81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
I82	NO_TEST=YES	TP_VESTA_SPD0	132
I84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
I83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
I85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
I86	NO_TEST=YES	TP_VESTA_TEST<0>	132
I87	NO_TEST=YES	TP_VESTA_TEST<1>	132
I88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
I90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
I89	NO_TEST=YES	TP_VESTA_TVCO	132
I222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
I223	NO_TEST=YES	TP_VESTA_FAVDDL	139
I224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
I225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

I91	NO_TEST=YES	TP_VESTA_TVCO_24	139
I92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
I93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
I94	NO_TEST=YES	TP_NB_APSYNC	44
I95	NO_TEST=YES	TP_SB_WATCHDOG	24
I96	NO_TEST=YES	NC_CPU_TBEN_CLK	
I97	NO_TEST=YES	NC_J3108_10	31
I98	NO_TEST=YES	NC_J3108_11	31
I99	NO_TEST=YES	NC_J3108_12	31
I100	NO_TEST=YES	NC_J3108_8	31
I101	NO_TEST=YES	NC_J3108_9	31
I102	NO_TEST=YES	NC_JTAGMUX_3	30
I103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

I105	NO_TEST=YES	Q803_C	8
I106	NO_TEST=YES	PLLLOCK	8 43
I111	NO_TEST=YES	LED_PP1V8_RUN_P	11
I112	NO_TEST=YES	LED_PP1V8_RUN_N	11
I113	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
I114	NO_TEST=YES	LED_PP1V5_RUN_N	12
I115	NO_TEST=YES	LED_PP1V5_RUN_P	12
I116	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
I120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
I121	NO_TEST=YES	LED_PP1V2_RUN_N	13
I122	NO_TEST=YES	LED_PP1V2_RUN_P	13
I123	NO_TEST=YES	KP_V<1>	55
I124	NO_TEST=YES	KP_V<2>	55
I125	NO_TEST=YES	CPU_SENSE_KP_V	55
I126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
I127	NO_TEST=YES	NB_PLL_OUT_TRG	59
I128	NO_TEST=YES	PP5V_T555	
I131	NO_TEST=YES	T555_DISC	
I132	NO_TEST=YES	T555_THRES	
I129	NO_TEST=YES	T555_OUT	
I130	NO_TEST=YES	T555_PWM	
I133	NO_TEST=YES	PP3V3_GPU_TSENSE	93
I134	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
I135	NO_TEST=YES	TSENSE_GPU_ADD0	93
I136	NO_TEST=YES	TSENSE_GPU_ADD1	93
I137	NO_TEST=YES	GPU_DIODE_PLUS	93
I138	NO_TEST=YES	GPU_DIODE_MINUS	93
I139	NO_TEST=YES	LED8700_P	136
I140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

I141	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
I142	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
I143	NO_TEST=YES	CPU_A_APSYNC_R	26
I144	NO_TEST=YES	CPU_B_APSYNC_R	26
I145	NO_TEST=YES	NB_APSYNC_R	26
I146	NO_TEST=YES	HT_SB_REFCLK_R	26
I147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
I148	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
I149	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
I150	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
I151	NO_TEST=YES	NB_PMR_CLK_P_R	26
I152	NO_TEST=YES	NB_PMR_CLK_N_R	26
I153	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
I154	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
I155	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
I156	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
I157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
I158	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
I159	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
I160	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
I161	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
I162	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
I163	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
I164	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
I165	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
I166	NO_TEST=YES	QUA0_REF_25MHZ_R	26
I167	NO_TEST=YES	SB_CLK25M_SATA_R	26
I168	NO_TEST=YES	QUA1_REF_25MHZ_R	26
I169	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
I170	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
I171	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
I172	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

I173	NO_TEST=YES	100M_N<0>	82 97
I175	NO_TEST=YES	100M_P<0>	82 97
I176	NO_TEST=YES	CKA_N<0>	84 97
I178	NO_TEST=YES	CKA_P<0>	84 97
I174	NO_TEST=YES	HT_NB_N<0>	98 101
I177	NO_TEST=YES	HT_NB_P<0>	98 101
I179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
I180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
I181	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
I182	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
I183	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
I184	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
I185	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
I186	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
I187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
I189	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
I188	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
I191	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97
I192	NO_TEST=YES	UATA_DA<0>	127 129
I193	NO_TEST=YES	UATA_DD<1>	127 129
I194	NO_TEST=YES	UATA_DD<14>	127 129
I195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	9 82 84 97
I196	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	9 82 84 97
I197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	9 82 97
I198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	9 82 97
I199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	9 82 84 97
I200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	9 82 84 97
I201	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	9 82 97
I202	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	9 82 97
I203	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	9 82 97
I204	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	9 82 97
I205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	9 82 97
I206	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
I208	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
I207	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
I210	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
I209	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
I211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
I213	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
I212	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
I214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
I216	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
I215	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
I218	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
I217	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
I219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
I221	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
I220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56
I257	NO_TEST=YES	PLLTESTOUT	43 47
I258	NO_TEST=YES	UATA_DD<13>	127 129
I259	NO_TEST=YES	CPU_SPARE2	43 47
I260	NO_TEST=YES	RFBD<51>	88 89
I261	NO_TEST=YES	TP_CPU_TRIGGER_OUT	56
I262	NO_TEST=YES	UATA_DD<12>	127 129
I263	NO_TEST=YES	EI_CPU_SYSCLK_P	43 56
I264	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
I265	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
I266	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
I267	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

I229	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
I227	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
I228	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
I226	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
I230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24
I232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
I234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
I233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
I236	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
I235	FUNC_TEST=TRUE	JTAG_NB_TRST_L	20
I238	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	17
I240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	17
I239	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	17
I242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	17
I241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	17
I244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
I246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
I245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
I248	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
I247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

ADDING NO_TEST TO ALL PCIE NETS
TO AVOID STUBS
WILL GET COVERAGE IN FCT WITH A DIAG
THAT CHECKS THAT THE BUS IS 16 LANES WIDE

I249	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<0..15>	9 82 97
I250	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<0..15>	9 82 97
I251	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0..15>	9 82 84 97
I252	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 84 97
I253	NO_TEST=YES	PCIE_SLOTA_TO_NB_NF<0..15>	84 97
I254	NO_TEST=YES	PCIE_SLOTA_TO_NB_PF<0..15>	84 97
I255	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
I256	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97

FUNC TEST 2 OF 2

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

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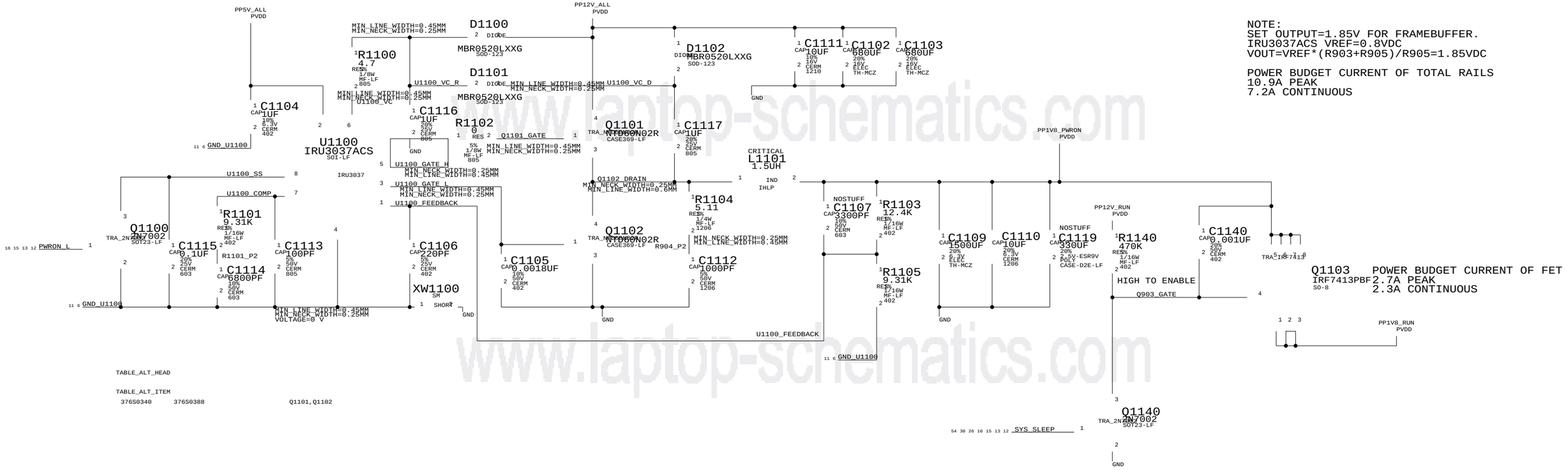
1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

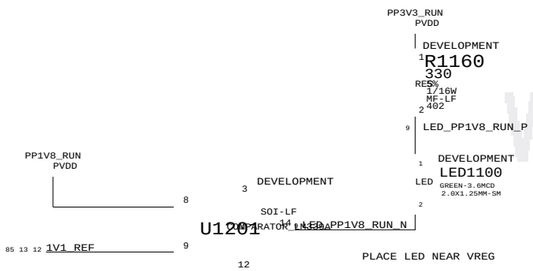
POWER BUDGET CURRENT OF TOTAL RAILS
10.9A PEAK
7.2A CONTINUOUS

Q1103 POWER BUDGET CURRENT OF FET
IRF7413PBF 2.7A PEAK
SO-8 2.3A CONTINUOUS

TABLE_ALT_HEAD

TABLE_ALT_ITEM

376S0340 376S0388 Q1101,Q1102



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1.8V VREG

SYNC_MASTER=M33-PC SYNC_DATE=06/20/2005

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KODIAK CORE VOLTAGE REGULATOR

NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.25VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

1.35V R1205=2.87K
1.30V R1205=3.24K
1.25V R1205=3.65K

TABLE_ALT_HEAD

TABLE_ALT_ITEM
376S0340 376S0388 Q1201,Q1202

PP5V_ALL PVDD
PP12V_ALL PVDD
PP1V5_PWRON PVDD

D1200 DIODE MBR0520LXXG SOD-123
D1202 DIODE MBR0520LXXG SOD-123
D1201 DIODE MBR0520LXXG SOD-123
MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM

R1200 10 RES 5% 1/8W MF-LF 805
C1204 CAP 1UF 10% 6.3V CERM 402
C1216 CAP 1UF 10% 25V X5R 603
C1201 CAP 10UF 10% 16V CERM 1210
C1210 CAP 10UF 10% 16V CERM 1210
C1202 CAP 680UF 20% 16V ELEC TH-MCZ
C1217 CAP 1UF 20% 25V CERM 805
R1202 0 RES 5% 1/8W MF-LF 805

U1200 IRU3037ACS SOI-LF CRITICAL
IRU3037
U1200_VC MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM
U1200_VC_R
U1200_VC_D
GND_U1200
U1200_SS
U1200_COMP
U1200_GATE_H MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM
U1200_GATE_L MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM
U1200_FEEDBACK
Q1201_GATE MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM
Q1202_DRAIN MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM

Q1201 NTTD6N02R CASE369-LF CRITICAL
Q1202 NTTD6N02R CASE369-LF CRITICAL
L1201 1.53UH IND_3P SM CRITICAL

R1201 15.8K RES 1% 1/16W MF-LF 402
R1201_P2
C1213 CAP 56PF 5% 50V CERM 402
C1214 CAP 0.1UF 20% 16V CERM 603
C1215 CAP 6800PF 10% 50V CERM 603
C1206 CAP 220PF 5% 25V CERM 402
C1205 CAP 0.0018UF 10% 50V CERM 402
R1204 5.11 RES 1% 1/4W MF-LF 1206
R2204_P2
C1212 CAP 1000PF 5% 50V CERM 1206
XW1200 SM SHORT
MIN_LINE_WIDTH=0.45MM MIN_NECK_WIDTH=0.25MM VOLTAGE=0 V

NOSTUFF
R1206 0 RES 5% 1/16W MF-LF 402
PWRON_L
TURN_ON_PP1V5_L
R1207 0 RES 5% 1/16W MF-LF 402
TURN_ON_PP1V2_L

Q1200 2N7002 TRA_2N7002 SOT23-LF
R1203 2.05K RES 1% 1/16W MF-LF 402
R1205 2.87K RES 1% 1/16W MF-LF 402
NOSTUFF C1207 CAP 1UF 20% 10V CERM 603
C1208 CAP 1500UF 20% 6.3V ELEC TH-MCZ CRITICAL
C1209 CAP 1500UF 20% 6.3V ELEC TH-MCZ CRITICAL
C1218 CAP 10UF 10% 6.3V X5R 805

TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW

PP1V5_PWRON PVDD
PP5V_PWRON PVDD
PP1V5_RUN PVDD
PP3V3_RUN PVDD

C1250 CAP 0.1UF 20% 10V CERM 402
R1250 100K RES 5% 1/16W MF-LF 402
Q1250 SI3446DV TSOP-LF CRITICAL
Q1250G
TRA_SI3446DV
RDSON=0.012 OHM @ VGS=3.5 V

Q1251 2N7002 SOT23-LF
TRA_2N7002
SYS_SLEEP
1V1_REF

R1261 0 RES 5% 1/16W MF-LF 402 DEVELOPMENT
PP1V5_RUN_FOR_LED

U1201 SOI-LF REGULATOR DEVELOPMENT
LED_PP1V5_RUN_N

R1260 330 RES 5% 1/16W MF-LF 402 DEVELOPMENT
LED_PP1V5_RUN_P
LED1200 LED GREEN-3.6MCD 2.0X1.25MM-SM DEVELOPMENT

PLACE LED NEAR VREG

PP1V5_PWRON_PULSAR

PP3V3_PWRON PVDD
PP12V_RUN PVDD

U1270 MM1571FN SOT-23A CRITICAL
VREG_MM1571FN
C1270 CAP 1UF 20% 10V CERM 805
R1270 10K RES 1% 1/16W MF-LF 402
U1270_CONT
U1270_NOISE
C1271 CAP 0.01UF 20% 10V CERM 402
C1272 CAP 10UF 10% 6.3V X5R 805
C1275 CAP 0.01UF 20% 16V CERM 402 DEVELOPMENT

R1273 10K RES 1% 1/16W MF-LF 402 DEVELOPMENT
PULSAR_1V5_RUN_SWITCH
R1274 10K RES 1% 1/16W MF-LF 402 DEVELOPMENT
Q1270 2N7002 TRA_2N7002 SOT23-LF DEVELOPMENT
SYS_POWERUP_L

Q1271 IRLM2402PBF TRA_IRLM2402 SOT23 DEVELOPMENT
PP1V5_RUN_PULSAR VOLTAGE=1.5V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM
NC_PP1V5_PULSAR MAKE_BASE=TRUE

1.5V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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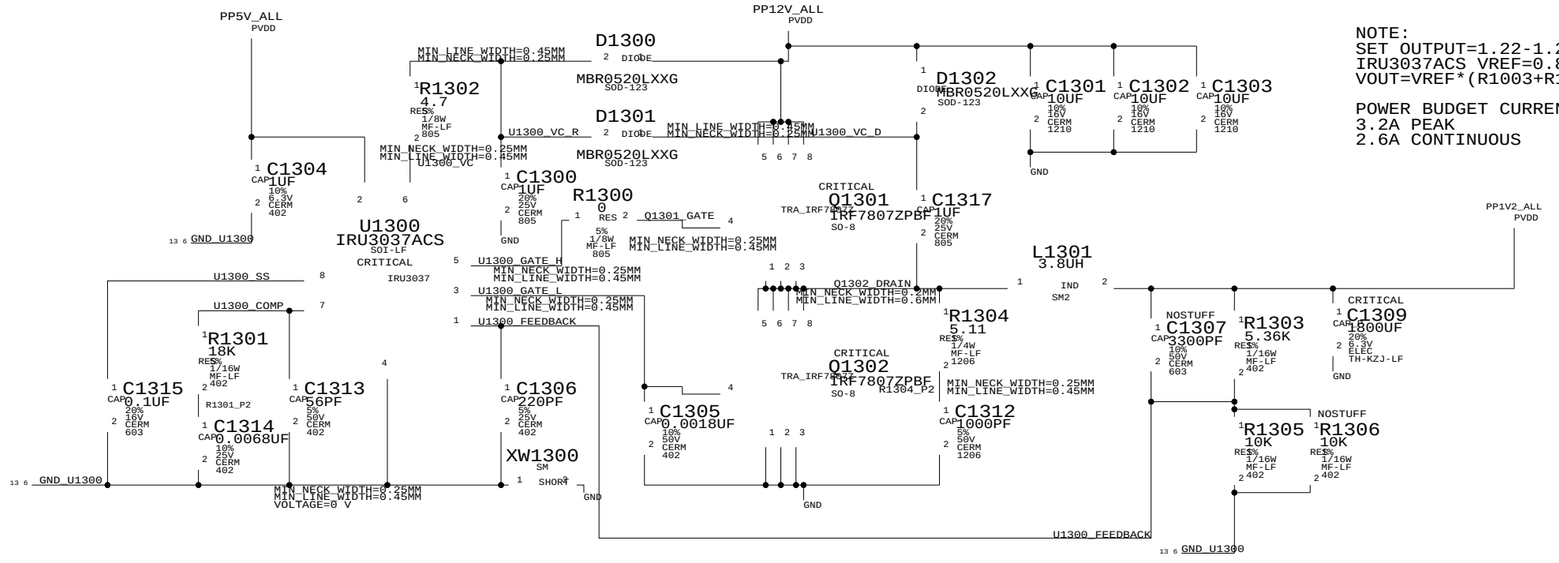
PP1V2_ALL VOLTAGE REGULATOR

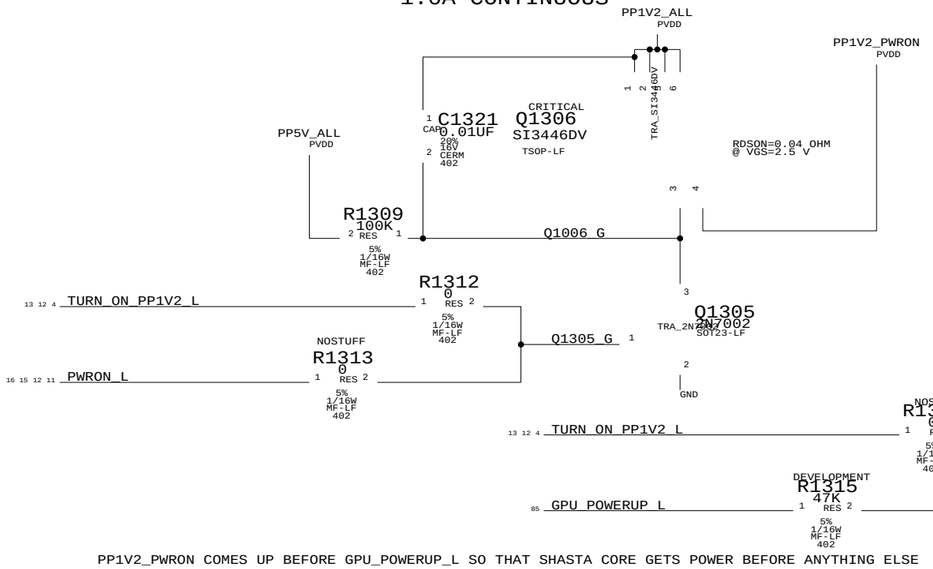


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

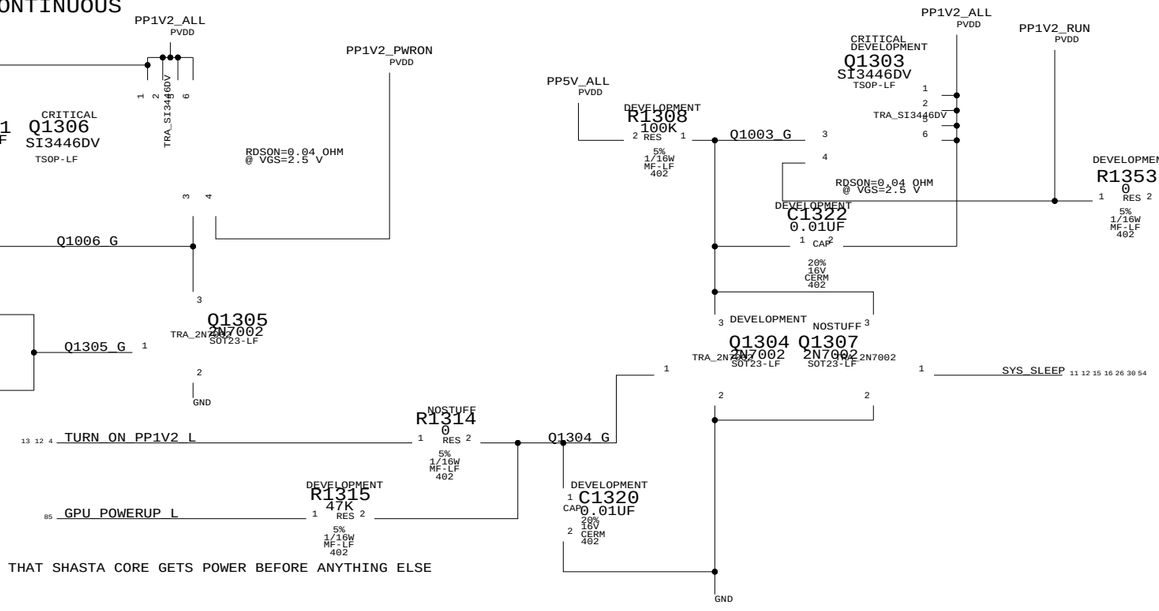
PEAK CURRENT 1.3A
1.0A CONTINUOUS

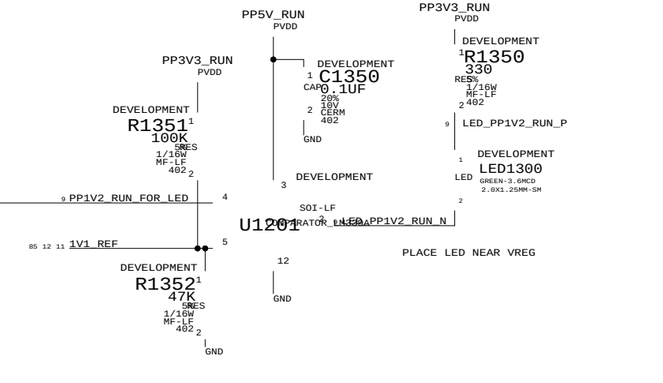


PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



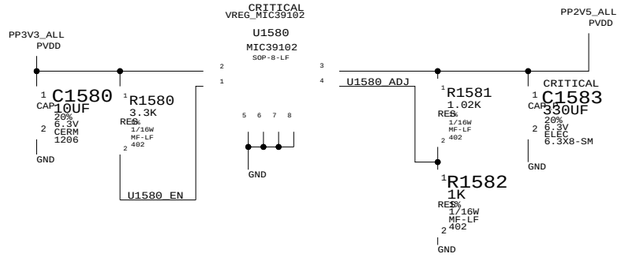


1.2V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

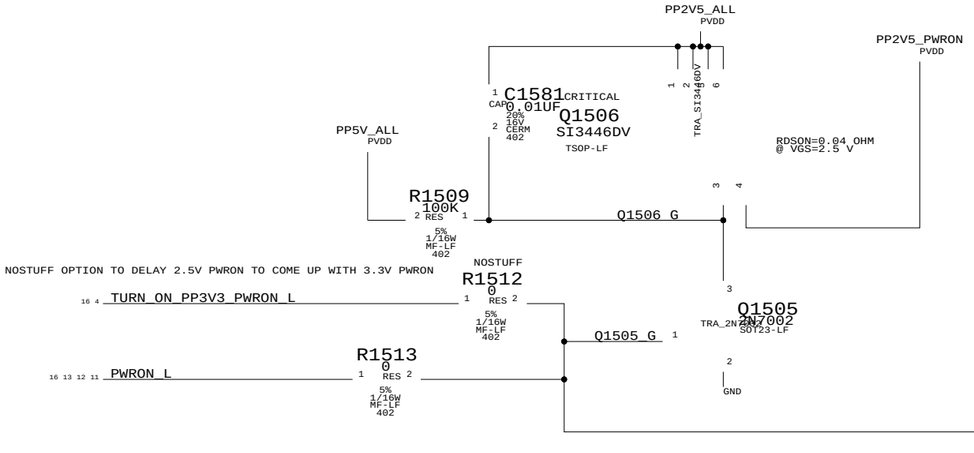
PP2V5_ALL VOLTAGE REGULATOR



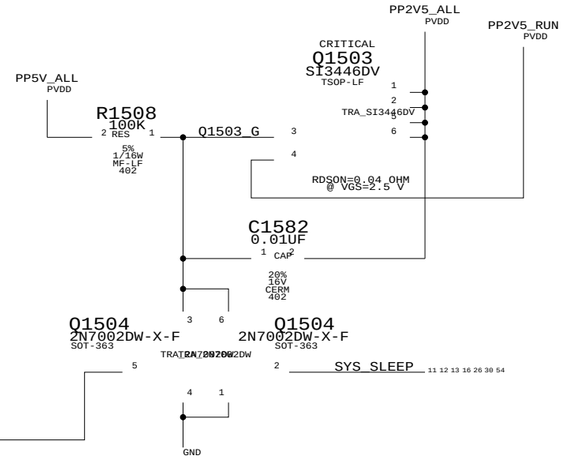
NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

PP2V5_PWRON FET SWITCH
PEAK CURRENT 0.1A



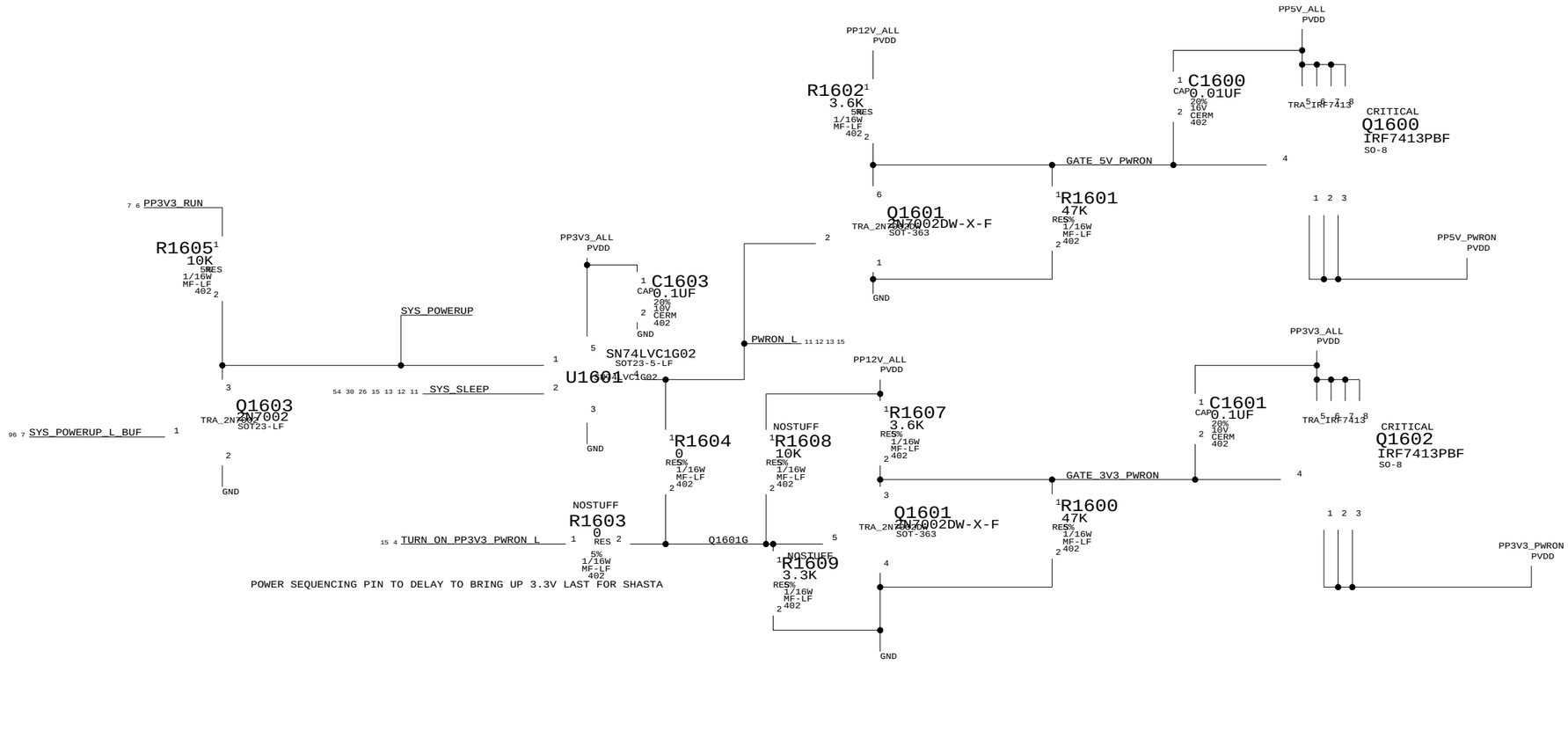
PP2V5_RUN FET SWITCH
PEAK CURRENT 0.1A



2.5V Vreg

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE



POWER SEQUENCING PIN TO DELAY TO BRING UP 3.3V LAST FOR SHASTA

5V & 3.3V Fets

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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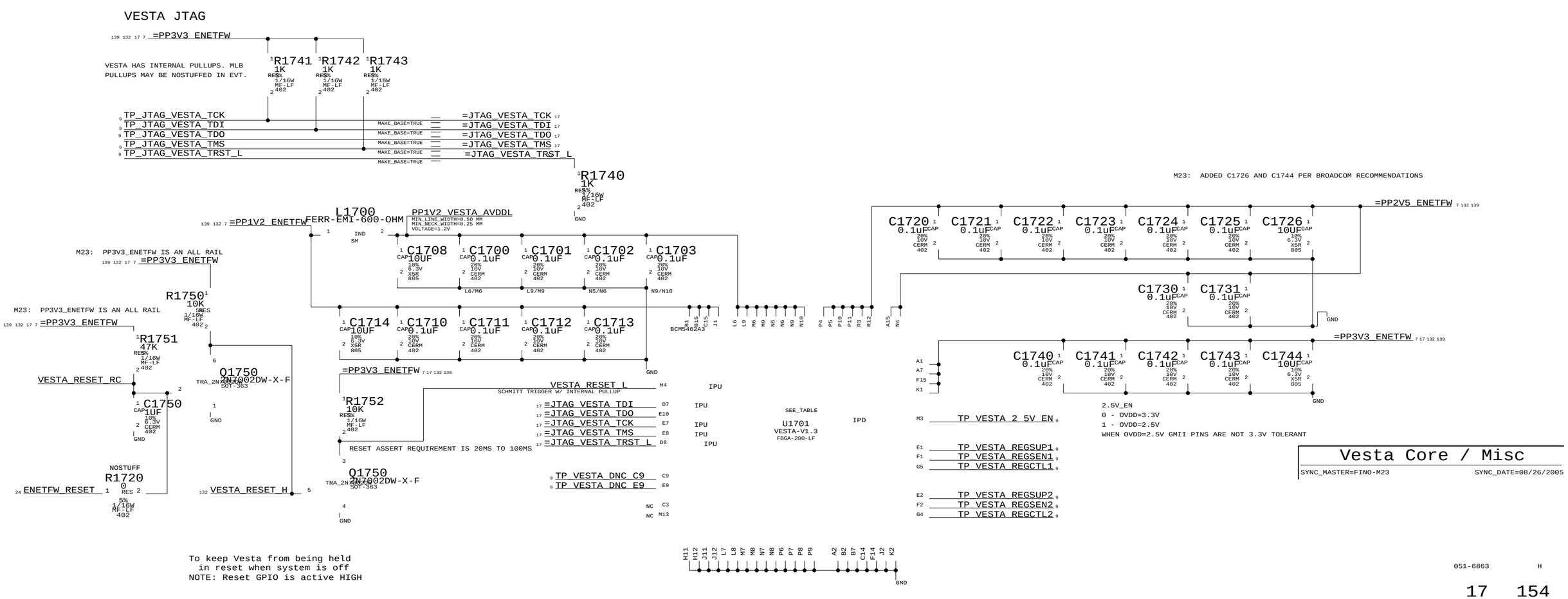
APPLE_DSIZEPAGE

Page Notes

Power aliases required by this page:

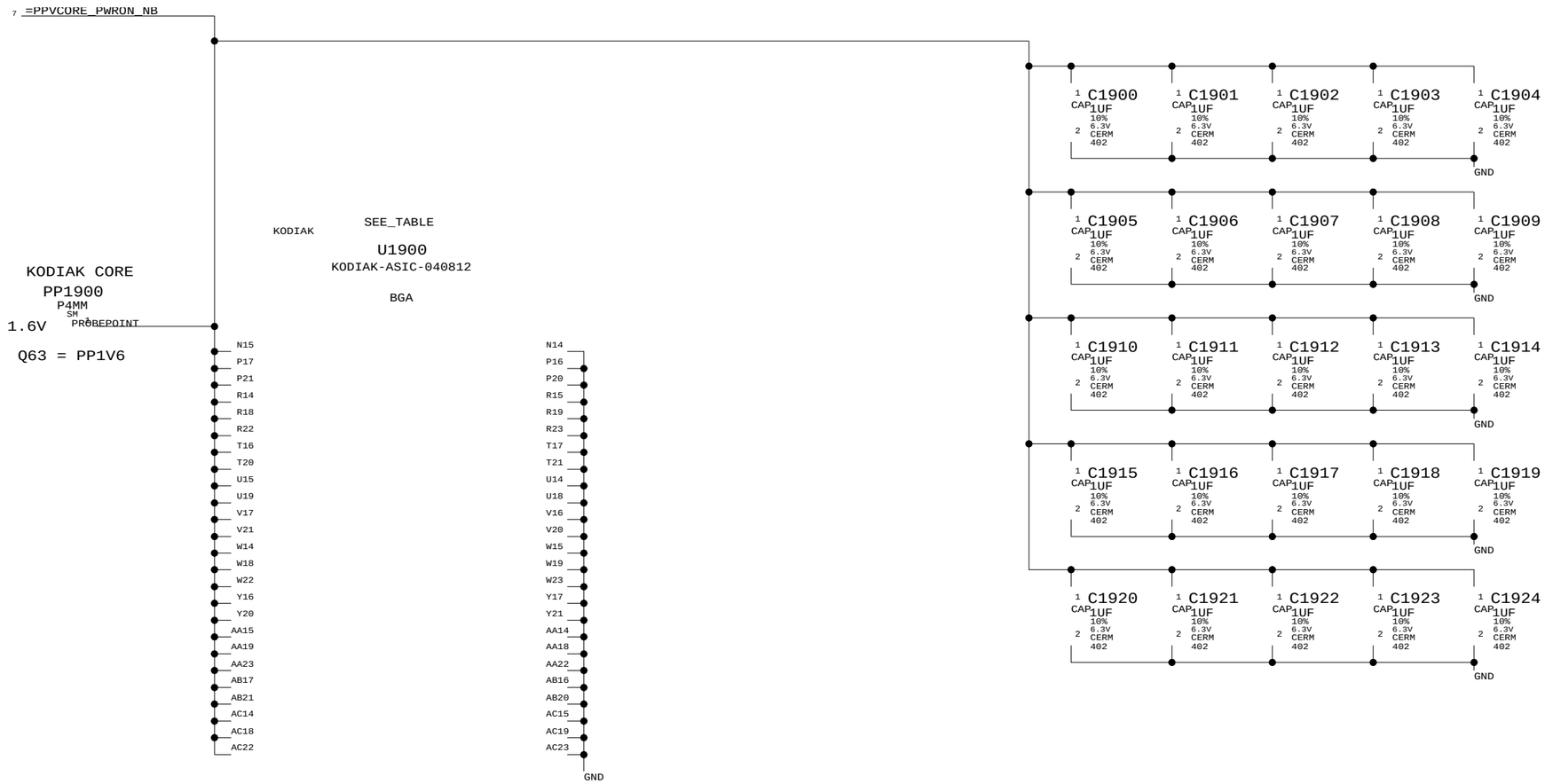
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.



To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

APPLE_DSIZEPAGE



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:22:40 2006

SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

119 92 PCI_RESET_L — MAKE_BASE=TRUE
=PCI_AIRPORT_RESET_L 121
=PCI_ROM_RESET_L 125
=PCI_USB2_RESET_L 122

24 NB_SLOT_RESET_L — MAKE_BASE=TRUE
=GPU_RESET_L 84

SHASTA JTAG

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

9 TP_JTAG_SB_TCK — MAKE_BASE=TRUE — JTAG_SB_TCK 24
9 TP_JTAG_SB_TDI — MAKE_BASE=TRUE — JTAG_SB_TDI 24
9 TP_JTAG_SB_TDO — MAKE_BASE=TRUE — JTAG_SB_TDO 24
9 TP_JTAG_SB_TMS — MAKE_BASE=TRUE — JTAG_SB_TMS 24

24 9 JTAG_SB_TRST_L
R2053 4.7K RES 5% 1/16W MF-LF 402
GND

SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

119 56 24 23 7 =PP3V3_PWRON_SB

24 RAI_EXP_INTR_L<3> — R2061 10K RES 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<2> — R2062 10K RES 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<1> — R2063 10K RES 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<0> — R2064 10K RES 5% 1/16W MF-LF 402

NB_OVERTEMP

30 28 7 =PP3V3_RUN_SMU
R2082 2.2 RES 5% 1/16W MF-LF 402
C2080 1UF CAP 10% 6.3V CERM 402
GND
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.38mm
TSENSE_NB_VCC
CRITICAL
MAX6690
U2080
MAX6690MEE
QSOP
TSENSE_NB_OVERTEMP_L
NOSTUFF R2087 0 RES 5% 1/16W MF-LF 402
SYS_OVERTEMP_L 24 28 93
NOSTUFF R2083 1K RES 5% 1/16W MF-LF 402
NOSTUFF R2084 1K RES 5% 1/16W MF-LF 402
NEED TO CHECK ALL I2C ADDRESSES
39 I2C_NB_TEMP_SDA
39 I2C_NB_TEMP_SCL
TSENSE_NB_ADD0
TSENSE_NB_ADD1
NOSTUFF R2086 1K RES 5% 1/16W MF-LF 402
NOSTUFF R2085 1K RES 5% 1/16W MF-LF 402

A0	A1	ADDR
0	0	30/31
0	hiZ	32/33
0	1	34/35
hiZ	0	52/53
hiZ	hiZ	54/55
hiZ	1	56/57
1	0	98/99
1	hiZ	9A/9B
1	1	9C/9D

20 NB_THERM_A
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_PHYSICAL_TYPE=10MIL_WIDTH
NET_SPACING_TYPE=TSENSE_DIFPAIR
PLACE BY IC
C2081 0.0022UF CAP 10% 50V CERM 402
20 NB_THERM_K
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH
GND

KODIAK ALIASES

6 NC_PMR_CLK_DIS_L — MAKE_BASE=TRUE — PMR_CLK_DIS_L 20

=PP2V5_PWRON_NB_MISC 7 20 28 30 39
R2073 4.7K RES 5% 1/16W MF-LF 402
NOSTUFF
R2074 0 RES 5% 1/16W MF-LF 402
20 9 JTAG_NB_TRST_L — NB_PU_RST_L 20 30
NOSTUFF
R2054 4.7K RES 5% 1/16W MF-LF 402
GND

KODIAK JTAG_TRST PULLED HIGH
TO ALLOW SMU DEBUG ACCESS

=PP1V8_PWRON_NBMEM 7 39 58 59
C2055 1UF CAP 10% 6.3V CERM 402
GND

C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

KODIAK
U1900
KODIAK-ASIC-040812
BGA

30 9 JTAG_NB_TCK — AJ04
30 9 JTAG_NB_TDI — AG07
30 9 JTAG_NB_TDO — AG05
30 9 JTAG_NB_TMS — AL02
20 9 JTAG_NB_TRST_L — AK06
CE0TEST — AG08
20 NB_THERM_A — F15
20 NB_THERM_K — G15
39 30 28 20 7 =PP2V5_PWRON_NB_MISC — AF02, AF05, AH01
C2050 1UF CAP 10% 6.3V CERM 402
C2051 1UF CAP 10% 6.3V CERM 402
C2052 1UF CAP 10% 6.3V CERM 402
R2000 0 RES 5% 1/16W MF-LF 402
GND

P4MM SM PROBEPOINT
TP2000
XW2000 SHORT SM
PP2V5PWRONNBMISC
R2013 10K RES 5% 1/16W MF-LF 402
NOSTUFF R2012 0 RES 5% 1/16W MF-LF 402
20 PMR_CLK_DIS_L
NB_PMR_CLK_STOP_L
NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

39 30 28 20 7 =PP2V5_PWRON_NB_MISC
P4MM SM PROBEPOINT
TP2002
R2003 1K RES 1% 1/16W MF-LF 402

AL01 NB_PU_RST_L — 20 30
AG01 NB_HRST_L
AJ03 NB_SUSPEND_ACK_L — 30 62
AJ01 NB_SUSPEND_REQ_L — 30
AG04 I2C_NB_B_SDA — 39
AK03 I2C_NB_B_SCL — 39
AH06 I2C_NB_C_SDA — 39
AJ05 I2C_NB_C_SCL — 39
AG03 I2C_NB_A_SDA — 39
AH03 I2C_NB_A_SCL — 39
AE09 NB_PMR_CLK_P — 26 27
AE10 NB_PMR_CLK_N — 26 27
AG02

NOSTUFF R2001 60.4 RES 1% 1/16W MF-LF 402
NOSTUFF R2002 60.4 RES 1% 1/16W MF-LF 402
TERM_RC
NOSTUFF C2053 1.5PF CAP +/-0.25PF 50V CERM 402
GND

PLACE TERM R/C CLOSE TO KODIAK

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

Page Notes

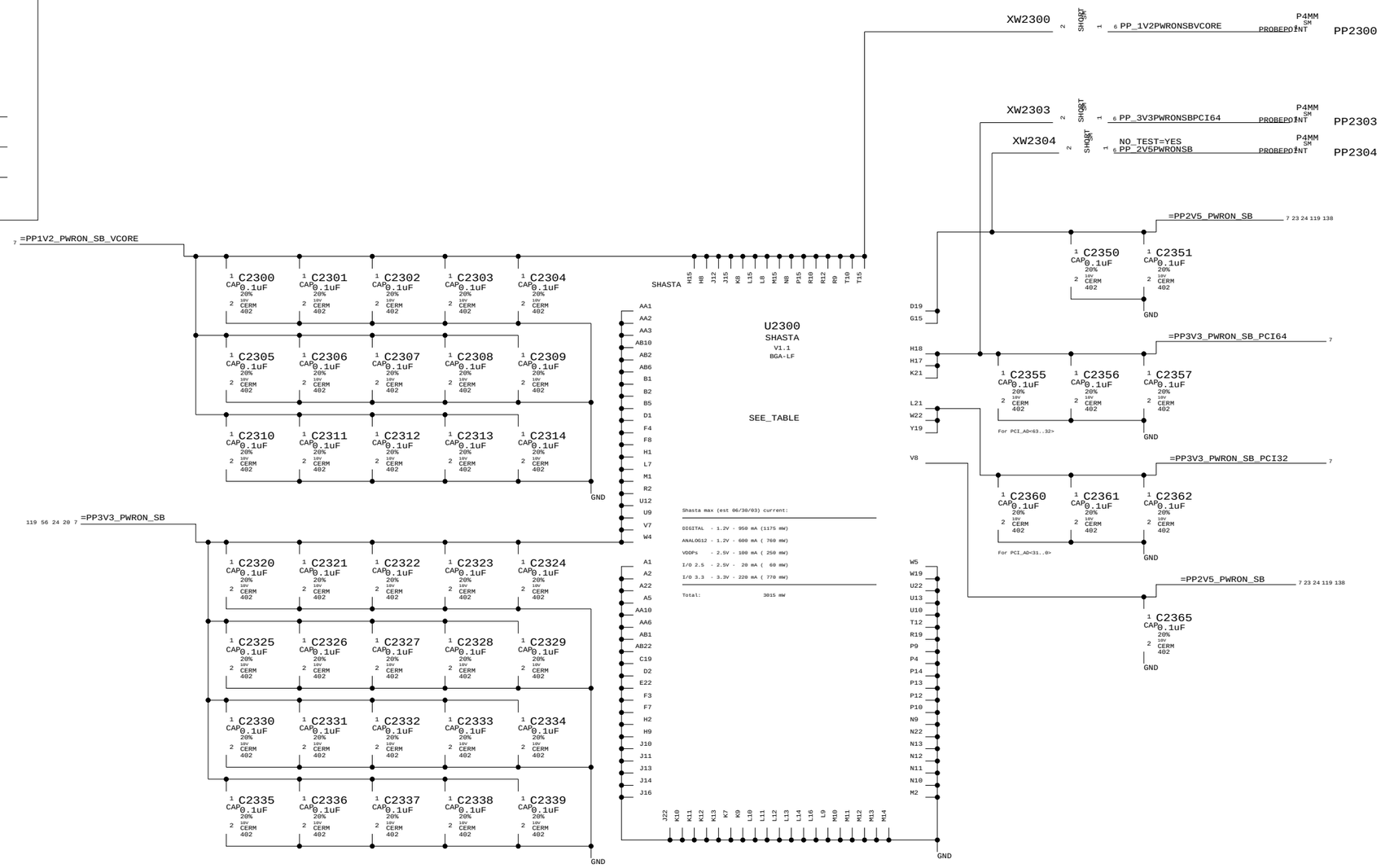
Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.



Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI	24 147
I2S0_SB_TO_DEV_DTO	24 147
I2S0_MCLK	24 154
I2S0_BITCLK	24 147
I2S0_SYNC	24 147
I2S1_DEV_TO_SB_DTI	8 24
I2S1_SB_TO_DEV_DTO	8 24
I2S1_MCLK	8 24
I2S1_BITCLK	8 24
I2S1_SYNC	8 24
I2S2_DEV_TO_SB_DTI	24 154
I2S2_SB_TO_DEV_DTO	24 154
I2S2_MCLK	24 154
I2S2_BITCLK	24 154
I2S2_SYNC	24 154
SB_CLK18M_XTALI	24
SB_CLK18M_XTALO	24
SB_CLK18M_XTALO_R	24
SB_CLK25M_SATA	24 26
NB_TO_SB_INT	24
SB_CPU_A0_INT_L	24
SB_CPU_A1_INT_L	24
SB_CPU_B0_INT_L	24
SB_CPU_B1_INT_L	24
PCI_AIRPORT_INT_L	24 121
PCI_USB2_INT_L	24 122
I2S0_RESET_L	24 147
I2S1_RESET_L	8 24
I2S2_RESET_L	24 154
MB_SLOT_RESET_L	24
NB_SLOT_RESET_L	20 24
SB_CPU_A0_SRESET_L	24 56
SB_CPU_A1_SRESET_L	24 56
SB_CPU_B0_SRESET_L	24 56
SB_CPU_B1_SRESET_L	24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP2V5_PWRON_SB
- _PP3V3_PWRON_SB
- _PP2V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

=PP3V3_RUN_SB_PCI 7 24

R2476 10K 5% 1/16W MF-LF 402 — To SouthBridge -> NB_TO_SB_INT 24

MPIC_SB
42 NB_CPU_A0_INT_L ARROW — FROM NORTHBRIDGE — R2475 10K 5% 1/16W MF-LF 402 — ARROW NB_INT_L_R 1
R2479 MPIC_NB 0 5% 1/16W MF-LF 402 2
56 CPU_A0_INT_R_L ARROW — TO CPU — R2478 0 5% 1/16W MF-LF 402 — ARROW SB_CPU_A0_INT_L 24 — FROM SOUTHBRIDGE

MPIC_SB TRA_2N3904LF Q2476 2N3904LF SOT23 3 2 GND

NorthBridge / SouthBridge MPIC Routing

=PP2V5_PWRON_SB 7 23 119 138

R2405 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTAL18VDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2400 CAP 10UF 10% 6.3V X5R 805 — C2401 CAP 1UF 10% 6.3V CERM 402 — GND

R2410 3.3 5% 1/8W MF-LF 805 — PP2V5_PWRON_SB_XTALVDD (VOLTAGE=2.5V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm) — C2410 CAP 10UF 10% 6.3V X5R 805 — C2411 CAP 1UF 10% 6.3V CERM 402 — GND — U14 SHASTA Y13

Re-pin within each RPAK as necessary DO NOT swap between RPAKs

I2S0_DEV_TO_SB_DTI		(I2S0_DEV_TO_SB_DTI)			W7
I2S0_SB_TO_DEV_DTO	RP2410 3	RPAK4P 33	I2S0_SB_TO_DEV_DTO_R		Y5
I2S0_MCLK	RP2410 4	RPAK4P 33	I2S0_MCLK_R		U8
I2S0_BITCLK	RP2420 1	RPAK4P 33	I2S0_BITCLK_R		AA4
I2S0_SYNC	RP2410 2	RPAK4P 33	I2S0_SYNC_R		Y6
I2S1_DEV_TO_SB_DTI		(I2S1_DEV_TO_SB_DTI)			V10
I2S1_SB_TO_DEV_DTO	RP2420 3	RPAK4P 33	I2S1_SB_TO_DEV_DTO_R		AB5
I2S1_MCLK	RP2430 2	RPAK4P 33	I2S1_MCLK_R		V9
I2S1_BITCLK	RP2430 3	RPAK4P 33	I2S1_BITCLK_R		AA8
I2S1_SYNC	RP2410 1	RPAK4P 33	I2S1_SYNC_R		AA7
I2S1_RESET_L		(I2S1_RESET_L)			V5
I2S2_DEV_TO_SB_DTI		(I2S2_DEV_TO_SB_DTI)			AA5
I2S2_SB_TO_DEV_DTO	RP2430 4	RPAK4P 33	I2S2_SB_TO_DEV_DTO_R		Y8
I2S2_MCLK	RP2420 4	RPAK4P 33	I2S2_MCLK_R		Y7
I2S2_BITCLK	RP2420 2	RPAK4P 33	I2S2_BITCLK_R		AB4
I2S2_SYNC	RP2430 1	RPAK4P 33	I2S2_SYNC_R		W9
I2S2_RESET_L		(I2S2_RESET_L)			Y2

AUDIO GPIO - see note on right

I2S0: Audio DAC
I2S1: Soft Modem
I2S2: S/P-DIF

119 56 24 23 20 7 =PP3V3_PWRON_SB

R2400 10K RES 1/16W MF-LF 402 — SB_PCI_SEL32BIT

R2402 0 RES 5% 1/16W MF-LF 402 — 122 119 30 28 SYS_IO_RESET_L

I2S0_RESET_L			AB3
SB_GPIO_H_3			W8
			W6
I2C_SB_SCL			Y9
I2C_SB_SDA			AB7
SHASTA_SYS_IO_RESET_L		ARROW	R9
SB_STOPXTALS_L		ARROW	AA9
SMU_SUSPENDREQ_L		ARROW	W10
SB_SUSPENDACK_L		ARROW	W11
SYS_PME_L		ARROW	W18
TP_SB_WATCHDOG			V12
JTAG_SB_TDI		ARROW	AA11
JTAG_SB_TDO		ARROW	W11
JTAG_SB_TCK			AB11
JTAG_SB_TMS			Y11
JTAG_SB_TRST_L			W12
SB_TEST_MODE_PD			A3
TP_SB_PLLTEST			U14
TP_SB_FSTEST			V14
SB_CLK18M_XTALI			W13
SB_CLK18M_XTALO_R			V13
SB_CLK25M_SATA			U15
		NC	V15

PLACE R2402 CLOSE TO SHASTA

119 56 24 23 20 7 =PP3V3_PWRON_SB

SB_CPU_A0_INT_L	R2408 10K	MPIC_NB
SB_CPU_A1_INT_L	R2409	MPIC_NB
SB_CPU_B0_INT_L	R2412	MPIC_NB
SB_CPU_B1_INT_L	R2418	MPIC_NB

5% 1/16W MF-LF 402

R2480 4.7K 5% 1/16W MF-LF 402 — GND

R2490 200 1% 1/16W MF-LF 402 — PP2406 — P4MM SM PROBEPOINT

CRITICAL Y2490 18.432M CRYSTAL SM — SB_CLK18M_XTALO 24

C2490 22PF CAP 5% 50V CERM 402 — GND
C2491 22PF CAP 5% 50V CERM 402 — GND

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

24 7 =PP3V3_RUN_SB_PCI

R2456 10K 5% 1/16W MF-LF 402 — PCI_AIRPORT_INT_L 24 121
R2459 10K 5% 1/16W MF-LF 402 — PCI_USB2_INT_L 24 122
SAT_RUN
R2416 1K 1% 1/16W MF-LF 402 — SYS_OVERTEMP_L 20 24 28 93
NOSTUFF R2417 10K 5% 1/16W MF-LF 402 — MAKE_TBEN_SYNC_L 24

LAST_MODIFIED=Fri Apr 28 20:22:45 2006
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AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

XW2400 2 SHORT 6 1 PP_1V2PWRONSBPLL45VDD P4MM SM PROBEPOINT — PP2400

PP1V2_PWRON_SB_PLL45VDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
R2420 3.3 5% 1/8W MF-LF 805 — =PP1V2_PWRON_SB 7
C2421 CAP 1UF 10% 6.3V CERM 402 — C2420 CAP 10UF 10% 6.3V X5R 805 — GND

VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm, PP1V2_PWRON_SB_PLL49VDD
R2430 3.3 5% 1/8W MF-LF 805
C2431 CAP 1UF 10% 6.3V CERM 402 — C2430 CAP 10UF 10% 6.3V X5R 805 — GND

=PP3V3_PWRON_SB 7 20 23 24 56 119
C2440 CAP 0.1UF 20% 10V CERM 402 — GND

NET_SPACING_TYPE=P3MM SPACING — P4MM SM PROBEPOINT — PP2405

U2300 SHASTA V1.1 BGA-LF

U17	NB_CHP_FLT_N_B			24
AA19	SB_SFC_RESET_L	ARROW		24
AB21	SB_CPU_VDNAP1			24 28
AA20	SB_CPU_VDNAP2			24 28
U16	SB_TO_SMU_INT_L	ARROW		24 28
Y20	LOGIC_BRD_GOOD	ARROW		24
D18	SB_VDNAP0	ARROW		24 31
A20	SYS_OVERTEMP_L	ARROW		20 24 28 93
F18	SB_GPIO14			24 143
F17	MB_SLOT_RESET_L			24
G16	NB_SLOT_RESET_L_R			24 143
F16	PCI_AIRPORT_INT_L			24 121
A21	PCIX_INT_L			24
B21	RAI_EXP_INTR_L<3>			20
C20	RAI_EXP_INTR_L<2>			20
G17	RAI_EXP_INTR_L<1>			20
G18	RAI_EXP_INTR_L<0>			20
E19	GIGE_P1_INTA_L			24
F19	GIGE_P2_INTB_L			24
D20	RAI_ALERT_L			24
E20	RAI_FATAL_L			24
C21	PCI_USB2_INT_L			24 122
F20	FW_LOWPWR_R			24
G19	ENETFW_RESET			17 24
C22	MAKE_TBEN_SYNC_L	ARROW		24
D21	ENET_ENERGYDET			24 132
G20	AUDIO_LO_DET_L			153
D22	AUDIO_LO_OPTICAL_PLUG_L			153
K18	AUDIO_LI_DET_L			153
H19	AUDIO_LI_OPTICAL_PLUG_L			154
J17	AUDIO_HP_DET_L			154
F21	AUDIO_MIC_ID			154
G21	AUDIO_LO_MUTE_L			150
H20	AUDIO_HP_MUTE_L			154
J19	AUDIO_SPKR_MUTE_L			152
F22	AUDIO_EXT_MCLK_SEL			154
G22	AUDIO_SPDIFIN_INT_L			154
H21	AUDIO_SPKR_ID			153
J20	SB_CPU_A0_INT_L	ARROW		24
H22	SB_CPU_A1_INT_L	ARROW		24
K22	SB_CPU_B0_INT_L	ARROW		24
K20	SB_CPU_B1_INT_L	ARROW		24
K17	SYS_SLEWING_L			24 26 28 50
L17	SB_CPU_A0_SRESET_L	ARROW		24 56
E18	SB_CPU_A1_SRESET_L	ARROW		24 56
Y4	SB_CPU_B0_SRESET_L	ARROW		24 56
U7	SB_CPU_B1_SRESET_L	ARROW		24 56
T9	NB_TO_SB_INT	ARROW		24
W2	SMU_TO_SB_INT_L	ARROW		24

(SECA1) (SECA2) (SECA3)

R2432 0 5% 1/16W MF-LF 402 — 1 — NB_SLOT_RESET_L 20 24

PLACE R2432 CLOSE TO SHASTA

AUDIO GPIOS

NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

AB12 AB13 AA12 GND

119 56 24 23 20 7 =PP3V3_PWRON_SB

I2S1_RESET_L	R2464 10K RES 5% 1/16W MF-LF 402		
SB_GPIO_H_3	R2463 10K RES 5% 1/16W MF-LF 402		
NB_CHP_FLT_N_B	R2450 10K RES 5% 1/16W MF-LF 402		
SB_SFC_RESET_L	R2451 10K RES 5% 1/16W MF-LF 402		
SB_CPU_VDNAP1	R2452 10K RES 5% 1/16W MF-LF 402		
SB_CPU_VDNAP2	R2453 10K RES 5% 1/16W MF-LF 402		
SB_TO_SMU_INT_L	R2454 10K RES 5% 1/16W MF-LF 402		
LOGIC_BRD_GOOD	R2455 10K RES 5% 1/16W MF-LF 402		
SB_VDNAP0	R2404 10K RES 5% 1/16W MF-LF 402		
SYS_OVERTEMP_L	SAT_PWRON R2460 1K RES 1% 1/16W MF-LF 402	93 28 24 29	
SB_GPIO14	R2422 10K RES 5% 1/16W MF-LF 402		
MB_SLOT_RESET_L	R2461 4.7K RES 5% 1/16W MF-LF 402		
SB_SLOT_RESET_L	NOSTUFF R2406 4.7K RES 5% 1/16W MF-LF 402		
PCIX_INT_L	R2419 10K RES 5% 1/16W MF-LF 402		
GIGE_P1_INTA_L	R2457 10K RES 5% 1/16W MF-LF 402		
GIGE_P2_INTB_L	R2413 10K RES 5% 1/16W MF-LF 402		
RAI_ALERT_L	R2414 10K RES 5% 1/16W MF-LF 402		
RAI_FATAL_L	R2465 10K RES 5% 1/16W MF-LF 402		
SYS_SLEWING_L	NOSTUFF R2462 1K RES 1% 1/16W MF-LF 402	50 28 26 24	
SMU_TO_SB_INT_L	R2421 10K RES 5% 1/16W MF-LF 402		
MAKE_TBEN_SYNC_L	R2415 10K RES 5% 1/16W MF-LF 402		

R2407 0 5% 1/10W MF-LF 402 — NO STUFF — 1 — FW_LOWPWR 139

FW_LOWPWR_R	R2466 10K RES 5% 1/16W MF-LF 402	
ENETFW_RESET	R2467 10K RES 5% 1/16W MF-LF 402	24 17
ENET_ENERGYDET	R2468 10K RES 5% 1/16W MF-LF 402	132 24

GND

Shasta Serial / Misc

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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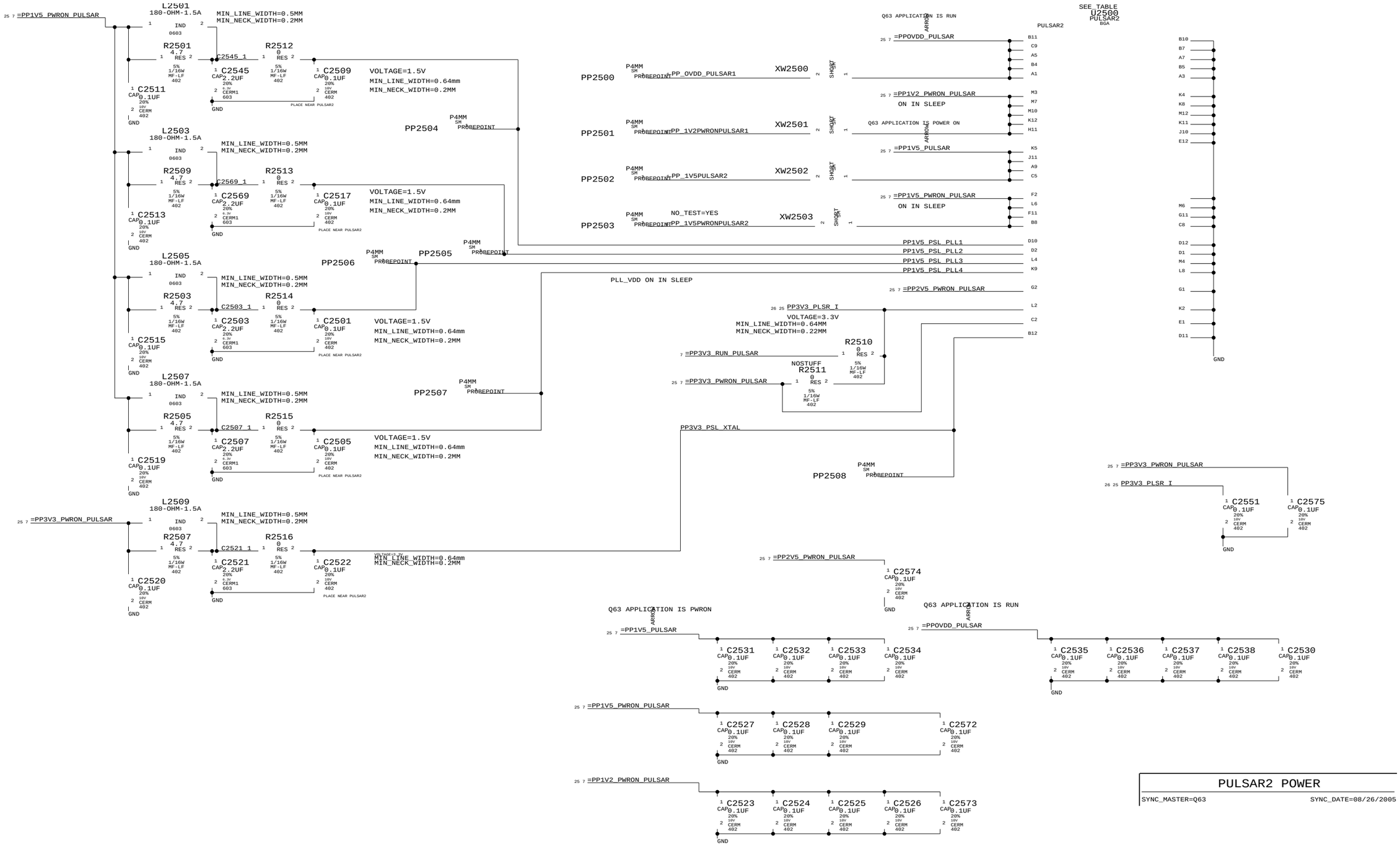

PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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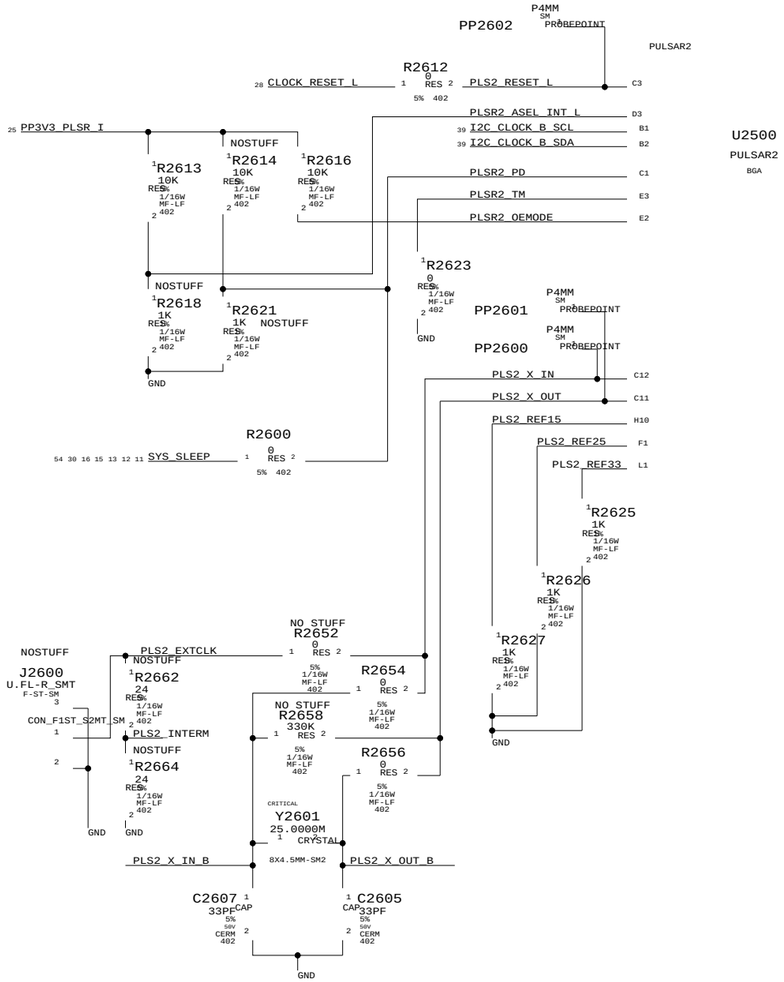
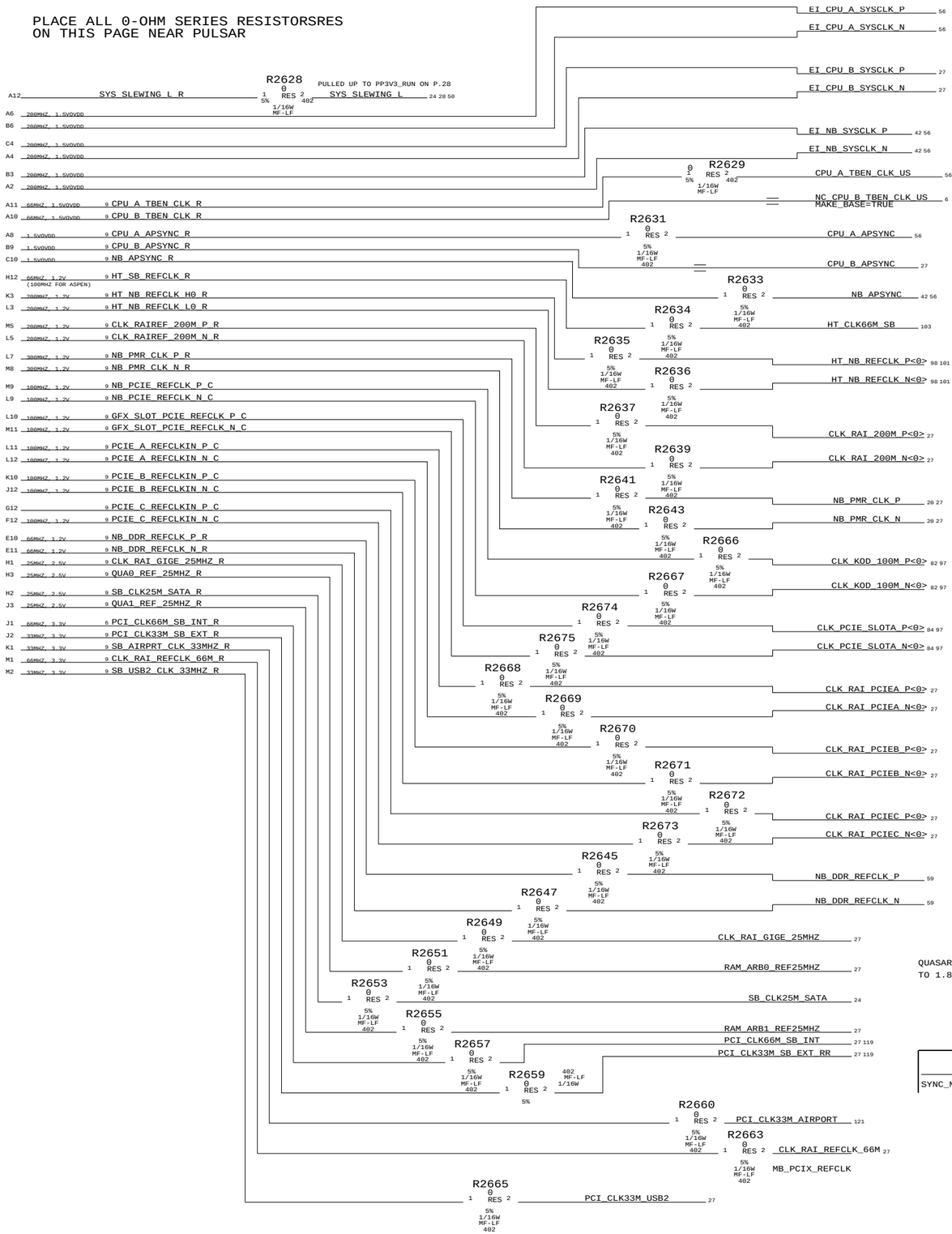
APPLE_DSIZEPAGE

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR





QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M ═══ CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ ═══ CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> ═══ CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> ═══ CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> ═══ CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> ═══ CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> ═══ CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> ═══ CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> ═══ CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> ═══ CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

6 NC_EI_CPU_B_SYSCLK_P ═══ EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N ═══ EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC ═══ CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ ═══ RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ ═══ RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 26 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	T67
26 26 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	T68
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	T69
119 26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP	T70

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 ═══ =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN 28
	0.38MM SPACING		SMU_CLK10M_XOUT 28
	0.38MM SPACING		SMU_CLK10M_XOUT_R 28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1 28
	0.38MM SPACING		RTC_CLK32K_X2 28
	P3MM SPACING		SMU_IO_RESET_L 28 30
	0.25MM SPACING		SYS_NORTH_RESET_L 28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L 28 30
SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L 24 30 119 122
	P3MM SPACING		CLOCK_RESET_L 26 28
	P3MM SPACING		SYS_RESET_BUTTON_L 28 29

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

PP2800 P4MM SM PROBEPOINT PP3V3ALLSMU — XW2802 SHORT

29 28 7 6 =PP3V3_ALL_SMU

C2800 10UF CAP 10% 6.3V X5R 805 — C2801 0.1UF CAP 20% 10V CERM 402 — C2802 0.1UF CAP 20% 10V CERM 402 — GND

R2815 4.7 RES 5% 1/16W MF-LF 402

PP3V3_ALL_SMU_AVCC VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

C2803 1UF CAP 10% 6.3V CERM 402 — GND_SMU_AVSS 6 28 55

XW2801 SHORT — 6 PP_3V3ALLSMUAVCC — P4MM SM PROBEPOINT — PP2801

M30280F8 13 — SEE_TABLE — 78

Y = Primary function
N = Alternate function (see aliases below)
S = Spare

		Portable	Consumer	Entry Desktop	Desktop	Server
55	CPU_SENSE_I	Y	Y	Y	S	S
55	CPU_SENSE_V	Y	Y	Y	S	S
55	CPU_TEMP	Y	Y	Y	S	S
29	CPU_BYPASS	Y	Y	Y	S	S
31	SMU_FAN_RPM3	N	S	Y	Y	Y
31	SMU_FAN_RPM4	N	S	Y	Y	Y
31	SMU_FAN_RPM5	N	S	Y	Y	Y
31	SMU_SER_SEL	Y	Y	Y	Y	Y
4	SMU_PWRSEQ_P1_0	Y	Y	Y	Y	Y
4	SMU_PWRSEQ_P1_1	Y	Y	Y	Y	Y
4	SMU_PWRSEQ_P1_2	Y	Y	Y	Y	Y
4	SMU_PWRSEQ_P1_3	Y	Y	Y	Y	Y
4	SMU_PWRSEQ_P1_4	Y	Y	Y	Y	Y
7	SYS_POWERFAIL_L	N	Y	Y	Y	Y
31	SMU_FAN_TACH9	N	S	S	S	Y
31	SYS_DOOR_AJAR_L	N	S	Y	Y	Y
31	SMU_FAN_TACH6	Y	Y	Y	Y	Y
31	SMU_FAN_TACH7	Y	Y	Y	Y	Y
32	SMU_FAN_TACH0	Y	Y	Y	Y	Y
32	SMU_FAN_TACH1	Y	Y	Y	Y	Y
33	SMU_FAN_TACH2	Y	Y	Y	Y	Y
31	SMU_FAN_TACH3	S	N	Y	Y	Y
31	SMU_FAN_TACH4	S	N	Y	Y	Y
31	SMU_FAN_TACH5	S	N	Y	Y	Y
31 28	I2C_SMU_A_SDA_IN	Y	Y	Y	Y	Y
31 28	I2C_SMU_A_SDA_OUT_L	Y	Y	Y	Y	Y
31 28	I2C_SMU_A_SCL_IN	Y	Y	Y	Y	Y
31 28	I2C_SMU_A_SCL_OUT_L	Y	Y	Y	Y	Y
39	I2C_SMU_E_SDA	Y	Y	Y	Y	Y
39	I2C_SMU_E_SCL	Y	Y	Y	Y	Y
8	DIAG_LED	Y	S	S	S	S
93 24 26	SYS_OVERTEMP_L	Y	S	S	S	S

P1[0] NOT USED --->

U2800 M30280F8-LF QFP-80

AN00	RTS0*/CTS0*		
AN01	CLK0		
AN02	RXD0		
AN03	TXD0		
AN04	RTS1*(BUSY)		
AN05	CLK1		
AN06	RXD1		
AN07	TXD1		
AN20	SDA		
AN21	SCL		
AN22	TA1out		
AN23	TA1in		
	TA2out		
INT3*	TA2in		
INT4*	TA3out		
INT5*	TA3in		
SDAmm	TA4out		
SCLmm	TA4in		
IOC2	INT0*		
IOC3	INT1*		
IOC4	INT2*		
IOC5	NMI*		
IOC6	CE*		
IOC7			
CLK3	TB0in		
Sin3	TB1in		
Sout3	TB2in		
	AN24		
	AN25		
	AN26		
	AN27		
	AN0		
	AN1		
	AN2		
	AN3		
KI0*			
KI1*			
KI2*			
KI3*			

		Portable	Consumer	Entry Desktop	Desktop	Server
43	SMU_BOOT_BUSY (MAKE_BASE=TRUE)	Y	Y	Y	N	N
42	SMU_BOOT_SCLK	Y	Y	Y	N	N
41	SMU_BOOT_CE	Y	Y	Y	N	N
40	CPU_VID<0>	Y	Y	Y	S	S
31	CPU_VID<1>	Y	Y	Y	S	S
30	CPU_VID<2>	Y	Y	Y	S	S
29	CPU_VID<3>	Y	Y	Y	Y	Y
28	CPU_VID<4>	Y	Y	Y	Y	Y
27	CPU_VID<5>	Y	Y	Y	Y	Y
26	SMU_BOOT_RXD	Y	Y	Y	Y	Y
25	SMU_BOOT_TXD	Y	Y	Y	Y	Y
24	I2C_SMU_B_SDA	Y	Y	Y	Y	Y
23	I2C_SMU_B_SCL	Y	Y	Y	Y	Y
22	I2C_SMU_CPU_SDA_IN	Y	Y	Y	N	N
21	SMU_FAN_RPM0	Y	Y	Y	Y	Y
20	I2C_SMU_CPU_SCL_IN	Y	Y	Y	N	N
19	SMU_FAN_RPM1	Y	Y	Y	Y	Y
18	SB_CPU_VDNAP2	N	S	S	Y	Y
17	SMU_FAN_RPM2	Y	Y	Y	Y	Y
16	SYS_LED	Y	Y	Y	Y	Y
15	SYS_NORTH_RESET_L	Y	Y	Y	Y	Y
14	SYS_PME_L	Y	Y	Y	Y	Y
8	SB_CPU_VDNAP0 OR QREQ OR SPDIF	S	S	S	S	S
7	SYS_POWERUP_L (MAKE_BASE=TRUE)	Y	Y	Y	Y	Y
5	SMU_SLEEP	Y	Y	Y	Y	Y
4	CLOCK_RESET_L	Y	Y	Y	S	S
3	SMU_FAN_TACH8	Y	Y	Y	Y	Y
2	SB_TO_SMU_INT_L	Y	Y	Y	Y	Y
1	SB_STOPXTALS_L	Y	Y	Y	Y	Y
80	SMU_PWRSEQ_P9_5	Y	Y	Y	Y	Y
79	SMU_PWRSEQ_P9_6	S	S	Y	Y	S
76	SYS_SLOT_PWR	S	S	S	S	S
74	SB_CPU_VDNAP1	Y	Y	Y	Y	Y
73	SMU_IO_RESET_L	Y	Y	Y	Y	Y
72	NB_SUSPENDACK_L	Y	Y	Y	Y	Y
71	SB_SUSPENDACK_L	Y	Y	Y	Y	Y
70	SMU_SUSPENDREQ_L	Y	Y	Y	Y	Y
69	SYS_POWER_BUTTON_L	Y	Y	Y	Y	Y
68	SYS_RESET_BUTTON_L	Y	Y	Y	S	S
	I2C_SMU_CPU_SCL_OUT_L					

P4MM SM PROBEPOINT PP2804 — 29 6 SMU_BOOT_CNVSS — 6
P4MM SM PROBEPOINT PP2805 — 29 6 SMU_RESET_L — 9
P4MM SM PROBEPOINT PP2806 — 28 SMU_CLK10M_XOUT_R — 10
P4MM SM — 28 SMU_CLK10M_XIN — 12
55 =PPVREF_SMU — 77

R2816 10M RES 5% 1/16W MF-LF 402
R2825 10K RES 1% 1/16W MF-LF 402 — C2825 1uF CAP 10% 6.3V CERM 402 — GND
R2817 470 RES 1% 1/16W MF-LF 402
Y2800 10.0000M CRYSTAL CRITICAL 8X4.5MM-SM
28 SMU_CLK10M_XOUT
C2804 18PF CAP 5% 50V CERM 402 — GND
C2805 18PF CAP 5% 50V CERM 402 — GND

Keep crystal subcircuit close to SMU.
Y2800'S LOAD CAPACITANCE IS 12PF

11 — XW2800 SM SHORT — 75

R2827 10K RES 1% 1/16W MF-LF 402 — GND

GND_SMU_AVSS VOLTAGE=0V 6 28 55
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

Real Time Clock

29 =PP3V3_ALL_RTC
29 28 7 6 =PP3V3_ALL_SMU

C2808 0.1UF CAP 20% 10V CERM 402 — GND

U2801 DS1338U-33 MSOP (DS1338 8 CRITICAL)
39 I2C_RTC_SDA — 5
39 I2C_RTC_SCL — 6
NC — 7
1 — RTC_CLK32K_X1 28
2
3 — RTC_CLK32K_X2 28
4 — GND

CRYSTAL-4PIN
Y2801 32.768K SM-LF CRITICAL

C2809 0.1UF CAP 20% 10V CERM 402 — GND

SMU Pull-ups / pull-down

29 28 7 6 =PP3V3_ALL_SMU

R2800 10K RES 5% 1/16W MF-LF 402 — SYS_POWERUP_L 6 7 12 28 50 85
R2801 10K RES 5% 1/16W MF-LF 402 — SYS_RESET_BUTTON_L 28 29
R2802 10K RES 5% 1/16W MF-LF 402 — SYS_POWER_BUTTON_L 6 28 29

43 30 7 =PP3V3_PWRON_SMU
R2804 10K RES 5% 1/16W MF-LF 402 — SYS_PME_L 24 28 122

30 20 7 =PP3V3_RUN_SMU
R2812 2.0K RES 1% 1/16W MF-LF 402 — SYS_SLEWING_L 24 26 28 50

NOSTUFF
39 30 20 7 =PP2V5_PWRON_NB_MISC
DRIVEN PUSH/PULL — ARROW
R2811 2.0K RES 1% 1/16W MF-LF 402 — SMU_SUSPENDREQ_L 24 28 30 43

NOSTUFF
PULLUP AT LEVEL SHIFTER P.30 — ARROW
R2813 10K RES 5% 1/16W MF-LF 402 — SYS_NORTH_RESET_L 28 30

R2810 100K RES 1% 1/16W MF-LF 402 — SMU_SLEEP 28 30
GND

System Management Unit

Alternate Functions

Tower & Server

		Port		
31 28	CPU_VID<0>	6.0		SAT_MRESET_L
31 28	CPU_VID<1>	6.1		CPU_A_INSERTED_L
31 28	CPU_VID<2>	6.2		CPU_B_INSERTED_L
31 28	I2C_SMU_CPU_SDA_IN	7.2		SMU_FAN_PWM8
31 28	I2C_SMU_CPU_SCL_IN	7.4		SMU_FAN_PWM9
31 28	I2C_SMU_A_SDA_IN	3.0		I2C_SMU_A_SDA 31 39
31 28	I2C_SMU_A_SDA_OUT_L	3.1		I2C_SMU_A_SCL 31 39

		Port		
31 28	CPU_VID<3>	6.3		SMU_FAN_RPM6
31 28	CPU_VID<4>	6.4		SMU_FAN_RPM7
31 28	I2C_SMU_A_SCL_IN	3.2		NB_TDI
31 28	I2C_SMU_A_SCL_OUT_L	3.3		NB_TCK
31 28	I2C_SMU_CPU_SDA_OUT_L	8.5		NB_TMS
31 28	I2C_SMU_CPU_SCL_OUT_L	10.7		NB_TDO_SMU

System Management Unit
SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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LAST_MODIFIED=Fri Apr 28 20:22:48 2006
DRAWING

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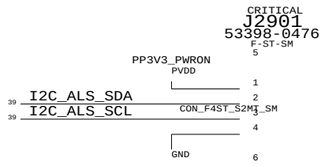
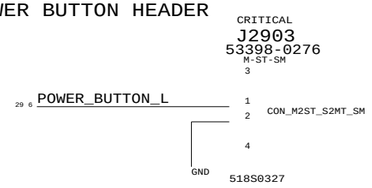
AMBIENT LIGHT SENSOR CONNECTOR



I2C ADDR:72(1001000)

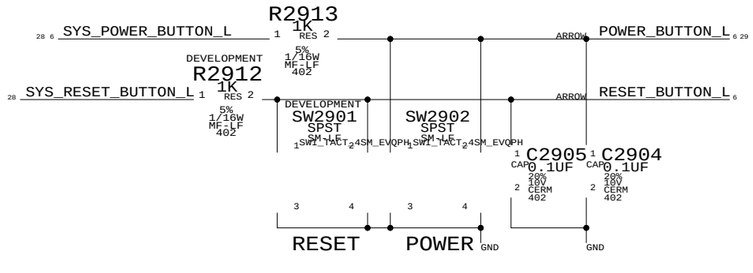
518S0328

POWER BUTTON HEADER



518S0327

SYS POWER AND RESET BUTTON



RTC BATTERY

SYS LED’S

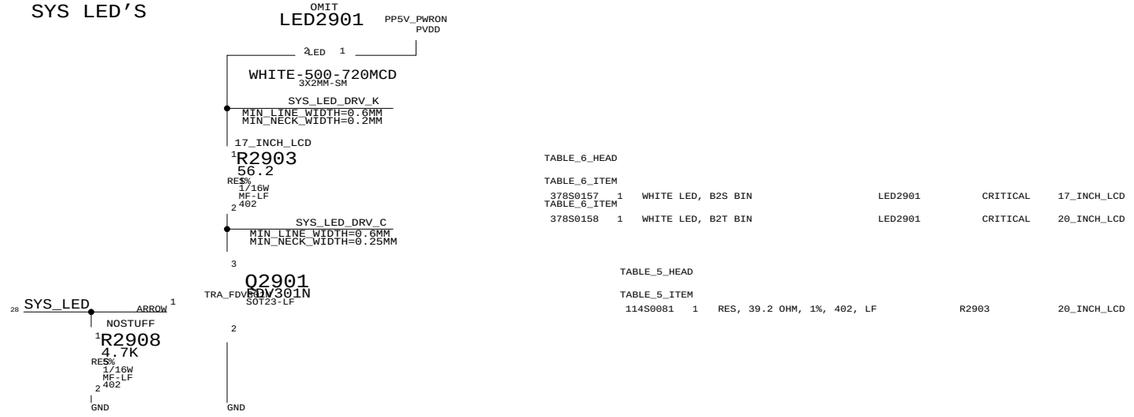


TABLE_6_HEAD

TABLE_6_ITEM

378S0157	1	WHITE LED, B2S BIN	LED2901	CRITICAL	17_INCH_LCD

TABLE_6_ITEM

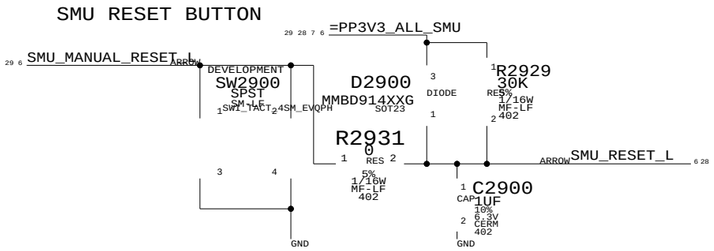
378S0158	1	WHITE LED, B2T BIN	LED2901	CRITICAL	20_INCH_LCD

TABLE_5_HEAD

TABLE_5_ITEM

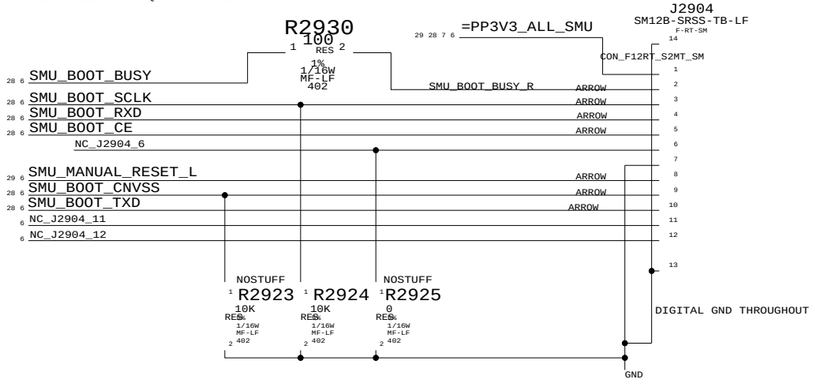
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903		20_INCH_LCD

SMU RESET BUTTON



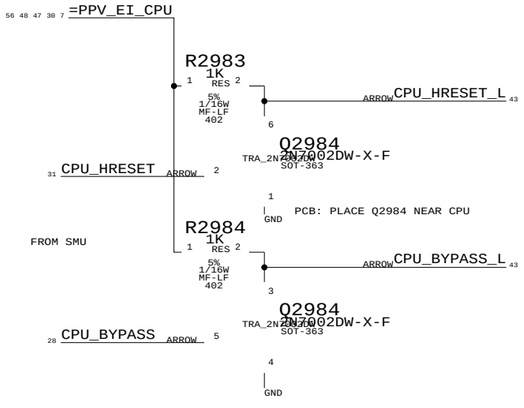
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT



R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVLOPMENT BOM POST-RAMP

DRIVE STRONG HRESET AND BYPASS TO CPU



SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-M23 SYNC_DATE=11/15/2005

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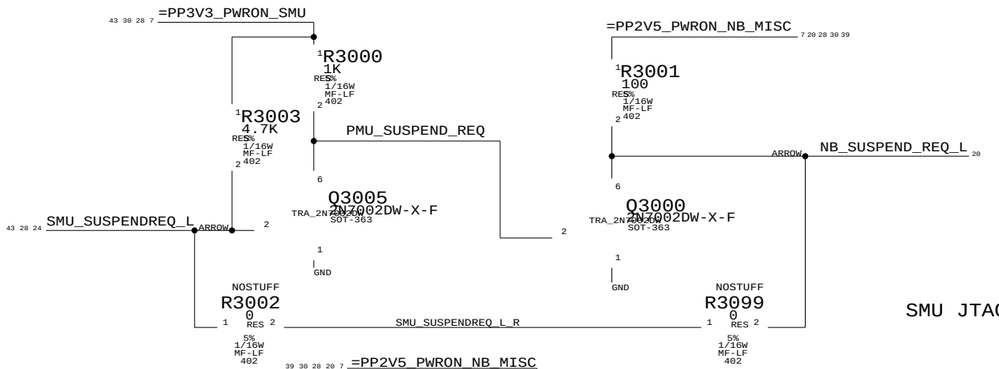
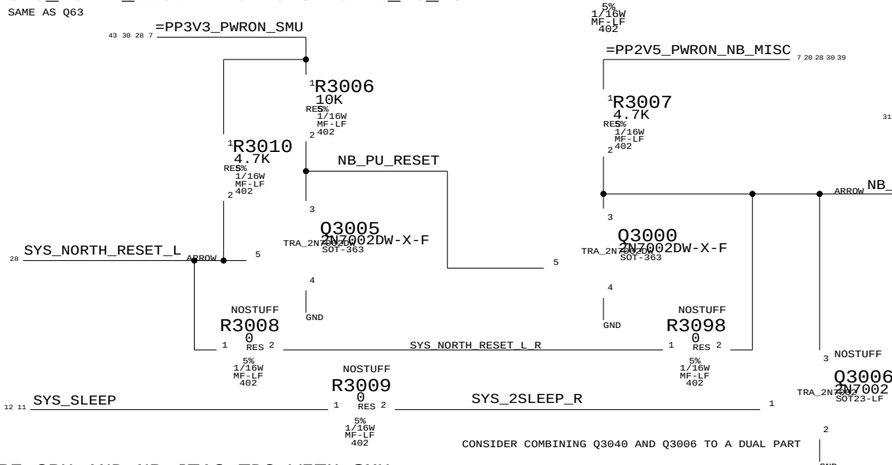
SMU TO NB SUSPEND_REQ

SAME AS Q63



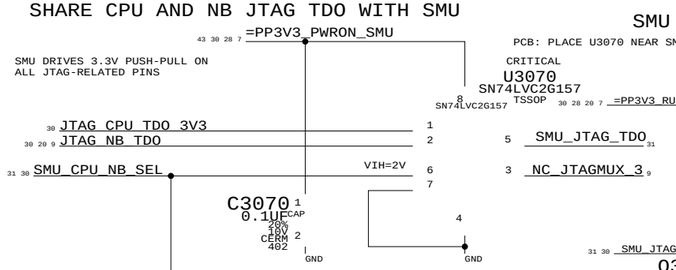
SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

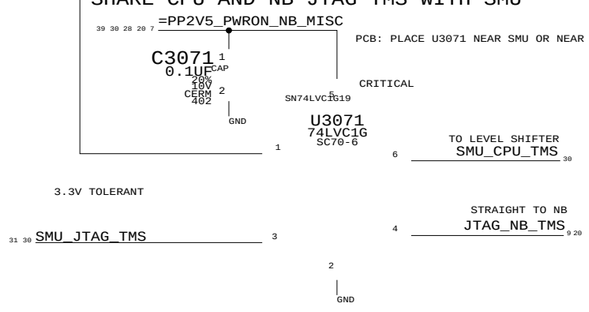


SYS_SLEEP

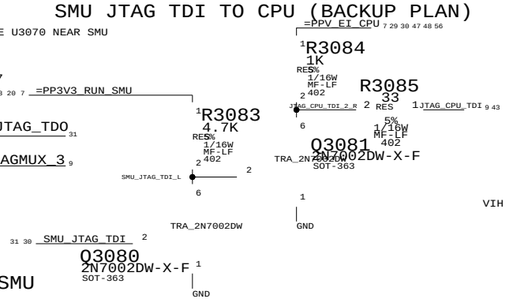
SHARE CPU AND NB JTAG TDO WITH SMU



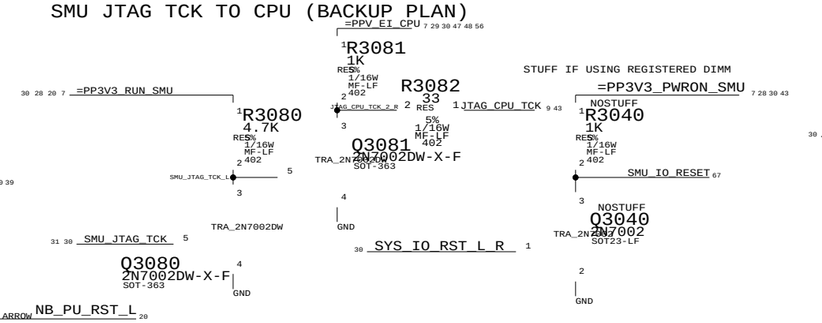
SHARE CPU AND NB JTAG TMS WITH SMU



SMU JTAG TDI TO CPU (BACKUP PLAN)

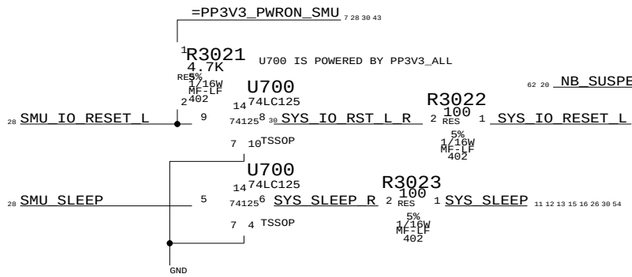


SMU JTAG TCK TO CPU (BACKUP PLAN)



MISC. SMU BUFFERS

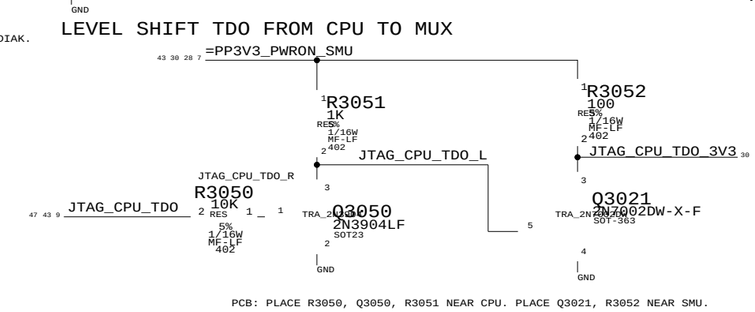
SAME AS (Q63).



STUFF IF USING REGISTERED DIMM

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED TO AVOID STUBS

LEVEL SHIFT TDO FROM CPU TO MUX

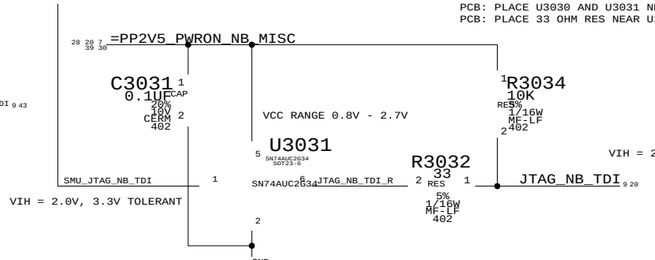


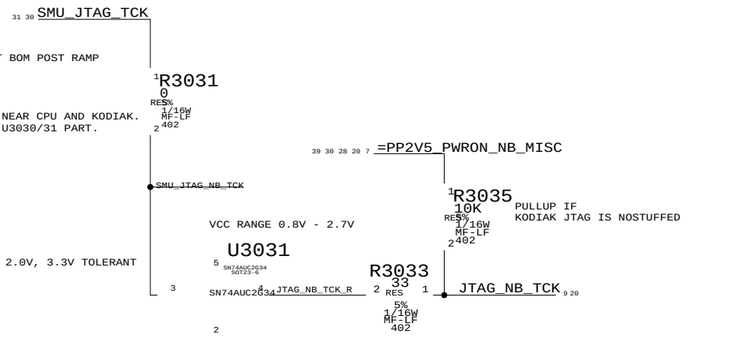
PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

NB JTAG IS A DEVELOPMENT ONLY FEATURE

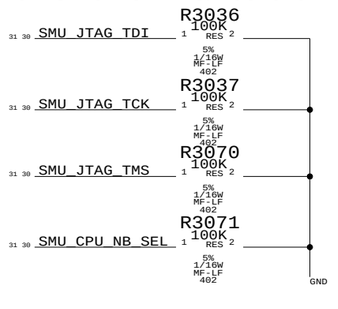
PLACE 0-OHM R3030 AND R3031 TO AVOID STUBS

R3030,R3031,C3031,U3031,R3032,R3033 SHOULD MOVE TO DEVELOPMENT BOM POST RAMP

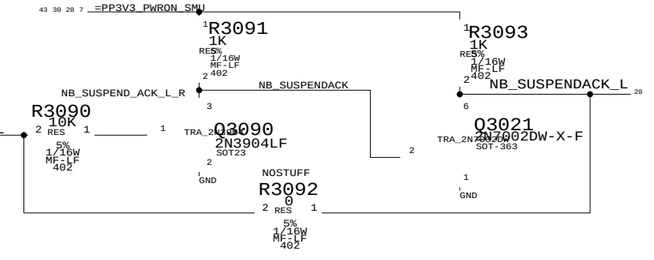




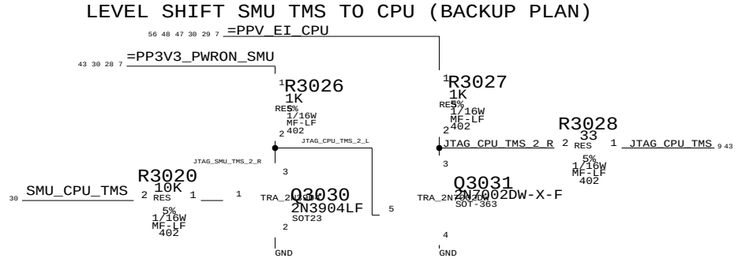
PULLDOWNS TO BUFFERS/LOGIC GATES



NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER



LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)



LEFTOVER FROM UNUSED PRIMARY PLAN - NOT STUFFED

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

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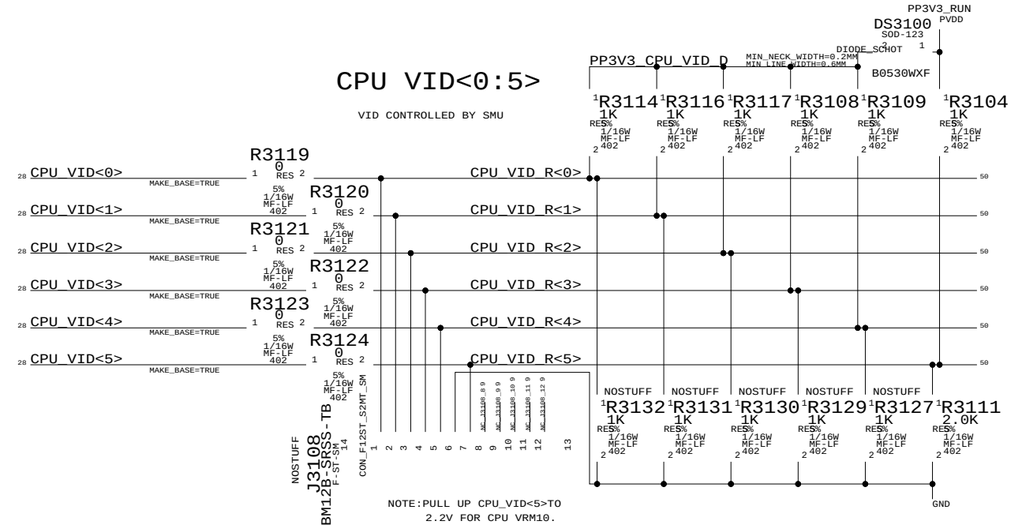
APPLE_DSIZEPAGE

SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
Q63 NC'S THESE AS IT USES A SAT.		CPU_TEMP0	P0.2	
		CPU_BYPASS	P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	30 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN	SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	30 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
		PS9_5	P9.5	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	30 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28

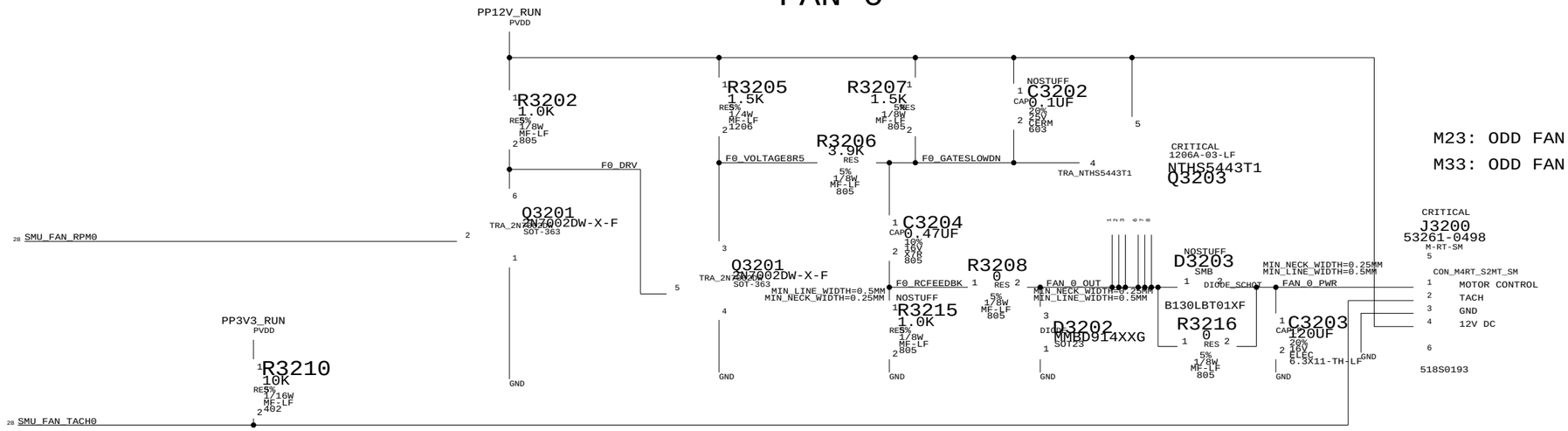


SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

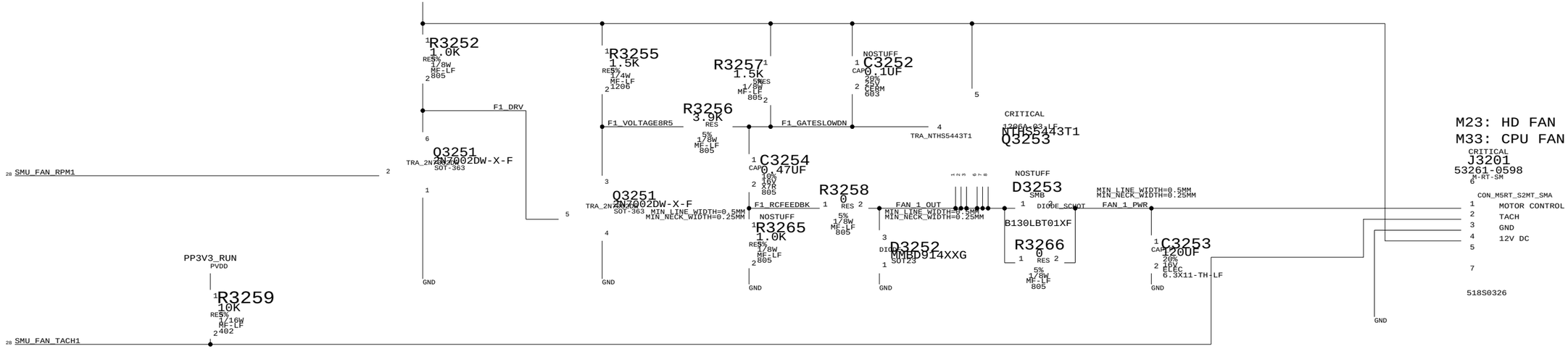
APPLE_DSIZEPAGE

FAN 0



M23: ODD FAN
M33: ODD FAN

FAN 1



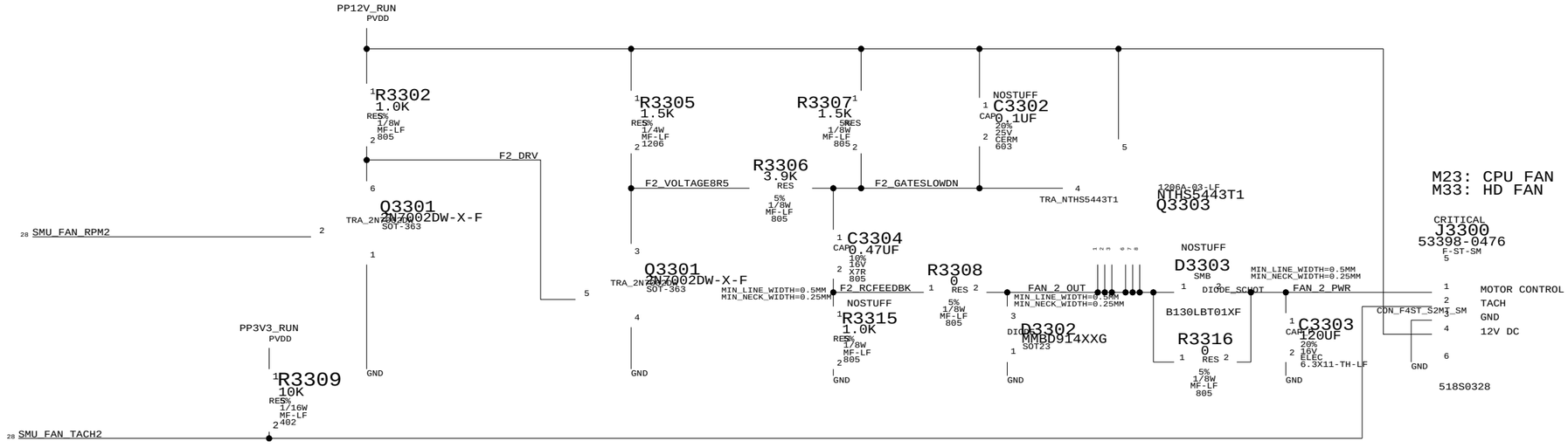
M23: HD FAN
M33: CPU FAN

Fan 0, 1 & System Temp

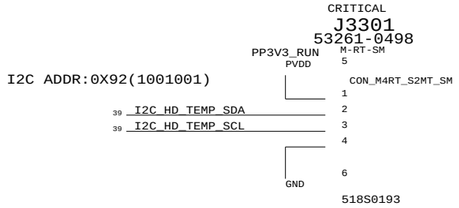
SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

FAN 2

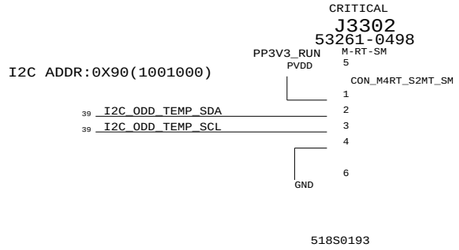


HD TEMP SENSOR



NOTE: BROKE SYNC ON THIS PAGE
TO ALLOW EMC CAPS ON M23 ONLY

ODD TEMP SENSOR



Fan 2 & HD Temp

SYNC_MASTER=M33-HS SYNC_DATE=08/04/2005

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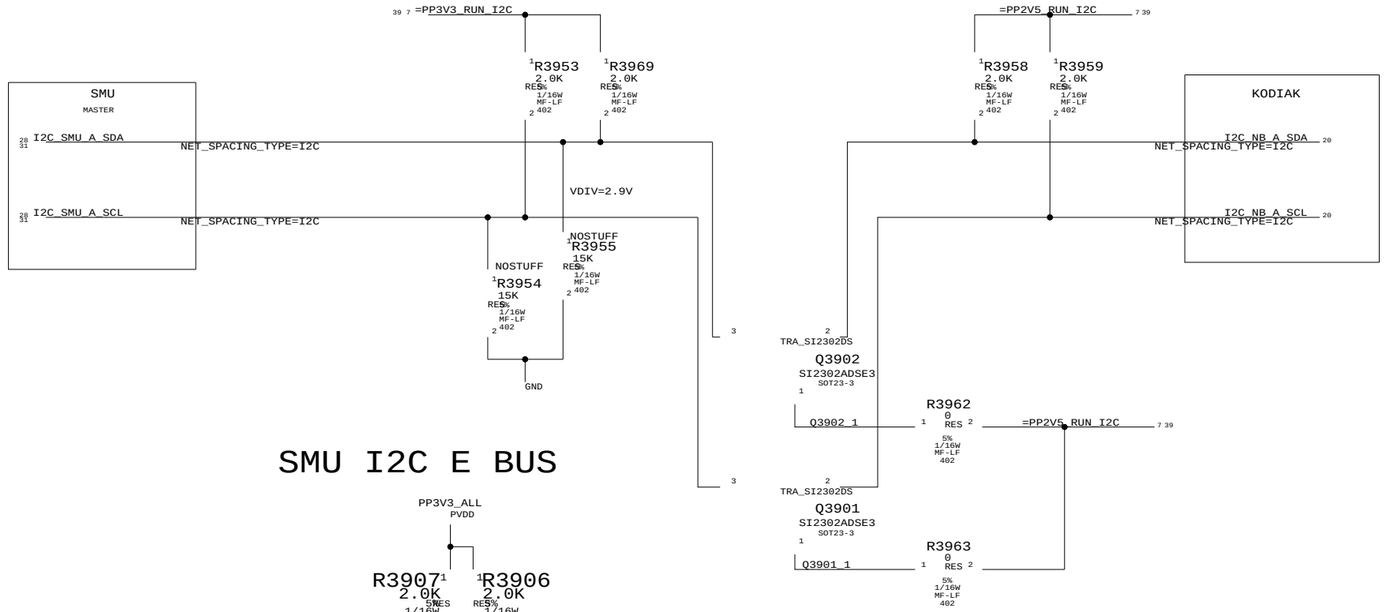
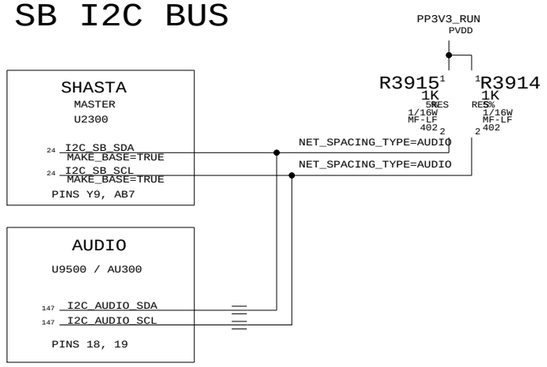
APPLE_DSIZEPAGE

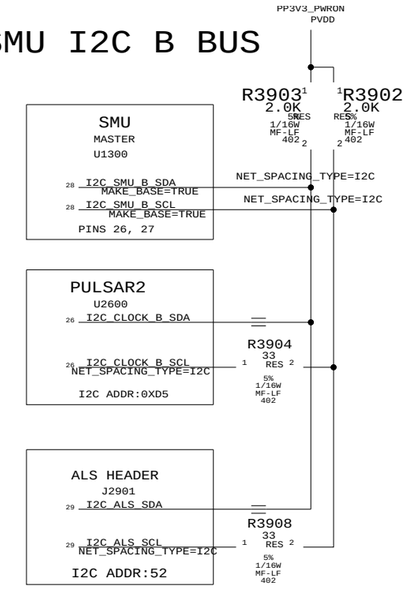
SMU AND NB I2C A BUS



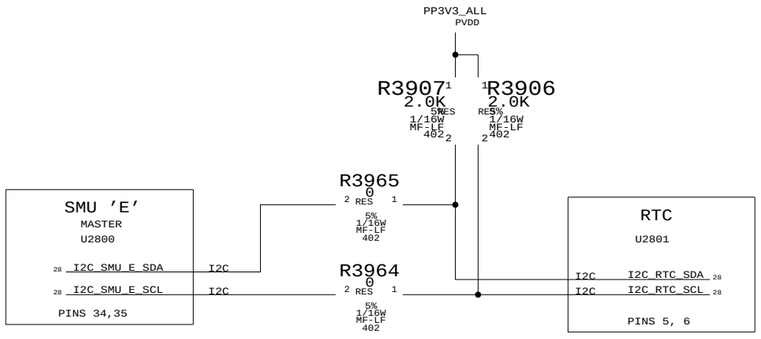
SB I2C BUS



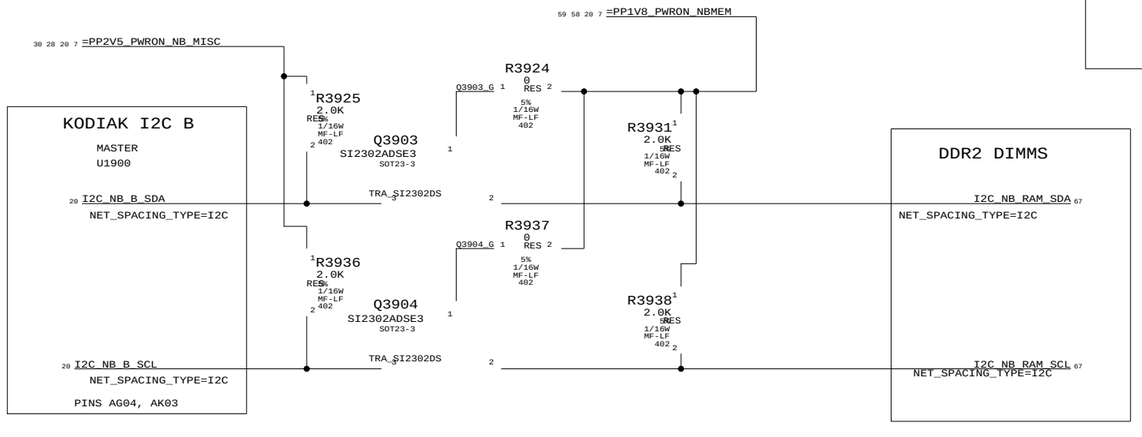
SMU I2C B BUS



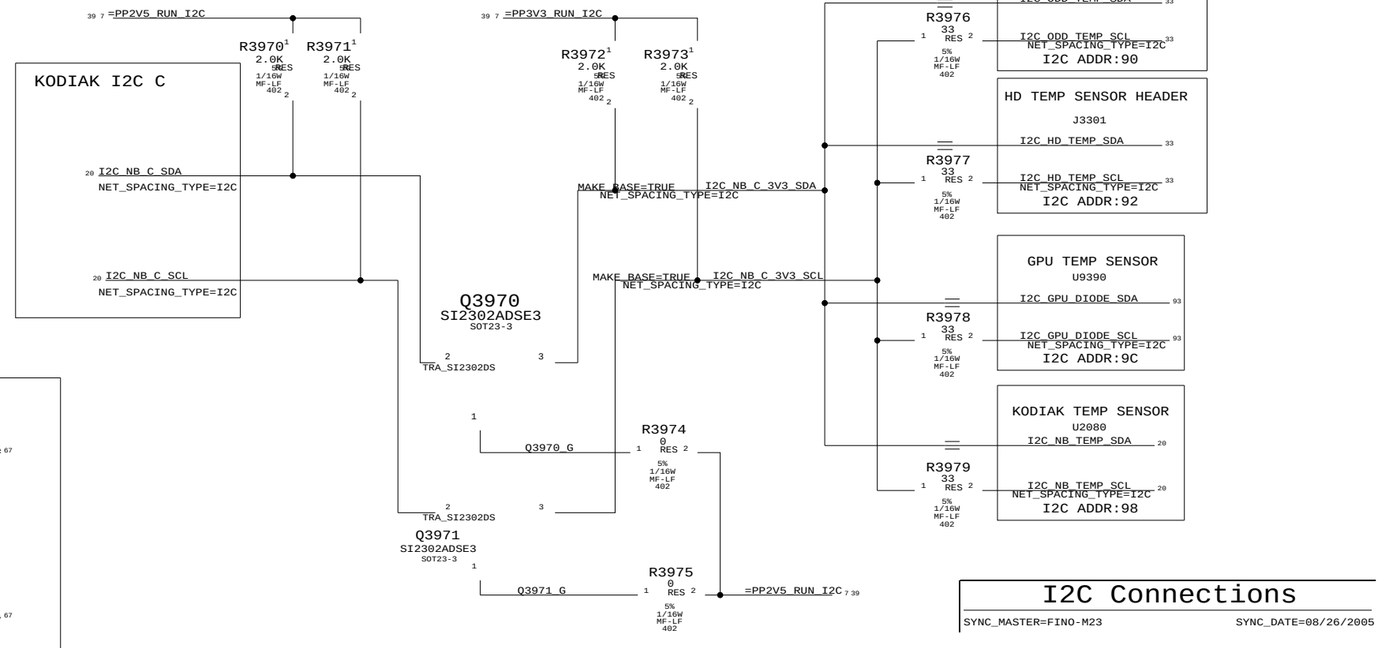
SMU I2C E BUS



NB I2C B BUS



NB I2C C BUS



I2C Connections

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

Q63 APPLICATION IS PP1V5 PWRON

ARRON

=PPV_EI_NB 7 41 42 56

KODIAK

XW4100 2 SHORT SM 1

NO_TEST=YES

6 PP_VEINB

P4MM SM PROBEPOINT

PP4100

U1900
BGA

KODIAK-ASIC-040812

AB01	AB02	AN04	AN05
AB04	AB05	AN07	AN09
AB07	AB08	AN11	AN13
AB10	AB11	AN15	AN17
AB12	AB13	AN19	AN21
AD02	AD01	AP01	AP02
AD05	AD04	AR05	AR07
AD08	AD07	AR09	AR11
AD11	AD10	AR13	AR15
AD13	AD12	AR17	AR19
AD17	AD16	AR21	AT05
AD21	AD20	AT03	AT09
AE15	AE14	AT07	AT13
AE19	AE18	AT11	AT17
AF07	AF08	AT15	AT21
AF10	AF11	AT19	K02
AF13	AF15	K01	K05
AF17	AF19	K04	K08
AG11	AG13	M02	M01
AG15	AG17	M05	M04
AG19	AG21	M08	M07
AH02	AH04	P01	M10
AH05	AH07	P04	P02
AH08	AH09	P07	P05
AJ13	AJ11	P10	P08
AJ17	AJ15	P12	P11
AJ21	AJ19	T02	P13
AK01	AK02	T05	T01
AK04	AK05	T08	T04
AK07	AK09	T11	T07
AK11	AK13	T13	T10
AK15	AK17	V01	T12
AK19	AK21	V04	V02
AM02	AM01	V07	V05
AM05	AM04	V10	V08
AM09	AM07	V12	V11
AM13	AM11	Y02	V13
AM17	AM15	Y05	Y01
AM21	AM19	Y08	Y04
AN04	AN05	Y11	Y07
AN07	AN09	Y13	Y10
AN11	AN13	AF01	Y12
AN15	AN17	AF04	
AN19	AN21	AF21	
AP01	AP02	AJ08	
AR05	AR07	AJ09	
AR09	AR11		
AR13	AR15		
AR17	AR19		
AR21	AT05		
AT03	AT09		
AT07	AT13		
AT11	AT17		
AT15	AT21		
AT19	K02		
K01	K05		
K04	K08		
M02	M01		
M05	M04		
M08	M07		
P01	M10		
P04	P02		
P07	P05		
P10	P08		
P12	P11		
T02	P13		
T05	T01		
T08	T04		
T11	T07		
T13	T10		
V01	T12		
V04	V02		
V07	V05		
V10	V08		
V12	V11		
Y02	V13		
Y05	Y01		
Y08	Y04		
Y11	Y07		
Y13	Y10		
AF01	Y12		
AF04			
AF21			
AJ08			
AJ09			

GND

Q63 APPLICATION IS PP1V5 PWRON

ARRON

56 42 41 7 =PPV_EI_NB

C4168	C4146	C4143	C4139	C4137	C4113	C4112	C4106	C4122	C4100
C4169	C4147	C4145	C4140	C4138	C4114	C4110	C4107	C4133	C4111
C4170	C4149	C4148	C4142	C4141	C4115	C4109	C4108	C4155	C4144
C4171	C4161	C4159	C4152	C4150	C4125	C4118	C4116	C4181	C4166
C4172	C4162	C4160	C4153	C4151	C4126	C4124	C4117	C4101	C4177
C4174	C4165	C4163	C4157	C4154	C4127	C4123		C4104	C4102
C4173	C4167	C4164	C4158	C4156	C4128	C4121	C4120	C4105	C4103
C4180	C4179	C4178	C4176	C4175	C4136	C4135	C4134	C4130	C4129
								C4132	C4131

All: CAP 0.22UF 20% 6.3V XSR 402

GND

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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LAST_MODIFIED=Fri Apr 28 20:22:57 2006

DRAWING

APPLE_DSIZEPAGE

56 26 EI_NB_SYSCLK_P — PROBEPOINT P4MM SM PP4216
56 26 EI_NB_SYSCLK_N — PROBEPOINT P4MM SM PP4201

AJ06, AJ07 KODIAK

PROBEPOINT P4MM SM PP4202
PROBEPOINT P4MM SM PP4203

EI OUTPUT TO CPU A

56	EI_NB_TO_CPU_A_CLK_P	L04
56	EI_NB_TO_CPU_A_CLK_N	L05
56	EI_NB_TO_CPU_A_AD<0>	R01
56	EI_NB_TO_CPU_A_AD<1>	R02
56	EI_NB_TO_CPU_A_AD<2>	T06
56	EI_NB_TO_CPU_A_AD<3>	T03
56	EI_NB_TO_CPU_A_AD<4>	U08
56	EI_NB_TO_CPU_A_AD<5>	U07
56	EI_NB_TO_CPU_A_AD<6>	R03
56	EI_NB_TO_CPU_A_AD<7>	R04
56	EI_NB_TO_CPU_A_AD<8>	R05
56	EI_NB_TO_CPU_A_AD<9>	T09
56	EI_NB_TO_CPU_A_AD<10>	R09
56	EI_NB_TO_CPU_A_AD<11>	R10
56	EI_NB_TO_CPU_A_AD<12>	P09
56	EI_NB_TO_CPU_A_AD<13>	U10
56	EI_NB_TO_CPU_A_AD<14>	P06
56	EI_NB_TO_CPU_A_AD<15>	P03
56	EI_NB_TO_CPU_A_AD<16>	N01
56	EI_NB_TO_CPU_A_AD<17>	N02
56	EI_NB_TO_CPU_A_AD<18>	N03
56	EI_NB_TO_CPU_A_AD<19>	N04
56	EI_NB_TO_CPU_A_AD<20>	R08
56	EI_NB_TO_CPU_A_AD<21>	V06
56	EI_NB_TO_CPU_A_AD<22>	M03
56	EI_NB_TO_CPU_A_AD<23>	M06
56	EI_NB_TO_CPU_A_AD<24>	N08
56	EI_NB_TO_CPU_A_AD<25>	N07
56	EI_NB_TO_CPU_A_AD<26>	N06
56	EI_NB_TO_CPU_A_AD<27>	N05
56	EI_NB_TO_CPU_A_AD<28>	L01
56	EI_NB_TO_CPU_A_AD<29>	L02
56	EI_NB_TO_CPU_A_AD<30>	L03
56	EI_NB_TO_CPU_A_AD<31>	L09
56	EI_NB_TO_CPU_A_AD<32>	K06
56	EI_NB_TO_CPU_A_AD<33>	K09
56	EI_NB_TO_CPU_A_AD<34>	L10
56	EI_NB_TO_CPU_A_AD<35>	L08
56	EI_NB_TO_CPU_A_AD<36>	R07
56	EI_NB_TO_CPU_A_AD<37>	R06
56	EI_NB_TO_CPU_A_AD<38>	L06
56	EI_NB_TO_CPU_A_AD<39>	M09
56	EI_NB_TO_CPU_A_AD<40>	N10
56	EI_NB_TO_CPU_A_AD<41>	N09
56	EI_NB_TO_CPU_A_AD<42>	L07
56	EI_NB_TO_CPU_A_AD<43>	K03
56	EI_NB_TO_CPU_A_SR_P<0>	V09
56	EI_NB_TO_CPU_A_SR_N<0>	W10
56	EI_NB_TO_CPU_A_SR_P<1>	W09
56	EI_NB_TO_CPU_A_SR_N<1>	U09
56	CPU_A0_QACK_L	AH10
56	CPU_A1_QACK_L	AF12

56 26 NB_APSYNC — AC10
42 24 NB_CPU_A0_INT_L — W11
56 42 NB_CPU_A1_INT_L — R11
56 NB_A_TRIGGER_OUT — AL07

PROBEPOINT P4MM SM PP4212
PROBEPOINT P4MM SM PP4213
PROBEPOINT P4MM SM PP4214
PROBEPOINT P4MM SM PP4215

NET_SPACING_TYPE

42	NB_CPU_A0_INT_L	P3MM_SPACING	24 42
42	NB_CPU_A1_INT_L	P3MM_SPACING	42 56

U1900

BGA

KODIAK-ASIC-040812

AG10 — GND

EI INPUT FROM CPU A

AA06	EI_CPU_A_TO_NB_CLK_P	56
AA07	EI_CPU_A_TO_NB_CLK_N	56
AE03	EI_CPU_A_TO_NB_AD<0>	56
AE04	EI_CPU_A_TO_NB_AD<1>	56
AE02	EI_CPU_A_TO_NB_AD<2>	56
AE01	EI_CPU_A_TO_NB_AD<3>	56
AD06	EI_CPU_A_TO_NB_AD<4>	56
AD03	EI_CPU_A_TO_NB_AD<5>	56
AE05	EI_CPU_A_TO_NB_AD<6>	56
AC04	EI_CPU_A_TO_NB_AD<7>	56
AC03	EI_CPU_A_TO_NB_AD<8>	56
AC05	EI_CPU_A_TO_NB_AD<9>	56
AC06	EI_CPU_A_TO_NB_AD<10>	56
AC07	EI_CPU_A_TO_NB_AD<11>	56
AC08	EI_CPU_A_TO_NB_AD<12>	56
AC02	EI_CPU_A_TO_NB_AD<13>	56
AA04	EI_CPU_A_TO_NB_AD<14>	56
AA05	EI_CPU_A_TO_NB_AD<15>	56
AB06	EI_CPU_A_TO_NB_AD<16>	56
AA03	EI_CPU_A_TO_NB_AD<17>	56
AA02	EI_CPU_A_TO_NB_AD<18>	56
AA01	EI_CPU_A_TO_NB_AD<19>	56
AA08	EI_CPU_A_TO_NB_AD<20>	56
AE06	EI_CPU_A_TO_NB_AD<21>	56
W06	EI_CPU_A_TO_NB_AD<22>	56
W05	EI_CPU_A_TO_NB_AD<23>	56
W07	EI_CPU_A_TO_NB_AD<24>	56
W08	EI_CPU_A_TO_NB_AD<25>	56
Y03	EI_CPU_A_TO_NB_AD<26>	56
Y06	EI_CPU_A_TO_NB_AD<27>	56
W04	EI_CPU_A_TO_NB_AD<28>	56
W03	EI_CPU_A_TO_NB_AD<29>	56
W02	EI_CPU_A_TO_NB_AD<30>	56
AB09	EI_CPU_A_TO_NB_AD<31>	56
AC09	EI_CPU_A_TO_NB_AD<32>	56
AA10	EI_CPU_A_TO_NB_AD<33>	56
AA09	EI_CPU_A_TO_NB_AD<34>	56
Y09	EI_CPU_A_TO_NB_AD<35>	56
U02	EI_CPU_A_TO_NB_AD<36>	56
U01	EI_CPU_A_TO_NB_AD<37>	56
U03	EI_CPU_A_TO_NB_AD<38>	56
U04	EI_CPU_A_TO_NB_AD<39>	56
U05	EI_CPU_A_TO_NB_AD<40>	56
V03	EI_CPU_A_TO_NB_AD<41>	56
W01	EI_CPU_A_TO_NB_AD<42>	56
U06	EI_CPU_A_TO_NB_AD<43>	56
AC01	EI_CPU_A_TO_NB_SR_P<0>	56
AB03	EI_CPU_A_TO_NB_SR_N<0>	56
AE08	EI_CPU_A_TO_NB_SR_P<1>	56
AE07	EI_CPU_A_TO_NB_SR_N<1>	56
AA11	CPU_A0_TO_NB_QREQ_L	42 56
AF18	CPU_A1_TO_NB_QREQ_L	42

PROBEPOINT P4MM SM PP4206
PROBEPOINT P4MM SM PP4207
PROBEPOINT P4MM SM PP4208
PROBEPOINT P4MM SM PP4209
PROBEPOINT P4MM SM PP4210
PROBEPOINT P4MM SM PP4211

PROBEPOINT P4MM SM PP4204

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

Q63 APPLICATION IS PP1V5 PWRON

ARROW =PPV_EI_NB 7 41 56

R4205 4.7K RES 5% 1/16W MF-LF 402 — 1 — 2 — NB_CHKSTOP_L 56

CPU_CHKSTOP_L IS SHARED BY BOTH CPUS

AD09

MIN_LINE_WIDTH=0.2MM
AG09 EI_REFCLK_AVDD

C4200 CAP 0.01UF 10% 16V CERM 402 — GND
C4201 CAP 2.2UF 20% 6.3V CERM1 603

R4200 4.99 RES 1% 1/8W MF-LF 805 — =PPV_PWRON_NB_REFCLK 7 59

Q63 CONNECTS THIS TO KODIAK CORE

PULL DOWN QREQS TO NB

56 42	CPU_A0_TO_NB_QREQ_L	R4207	10K RES 5% 1/16W MF-LF 402	
42	CPU_A1_TO_NB_QREQ_L	R4206	10K RES 5% 1/16W MF-LF 402	GND

KODIAK EI A

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

051-6863 H

42 154

APPLE_DSIZEPAGE

LAST_MODIFIED=Fri Apr 28 20:22:58 2006

DRAWING

56 9 EI_CPU_SYSCLK_P ARROW

PCB: PLACE R4303 AND R4301 AT PROCESSOR PINS

56 EI_CPU_SYSCLK_N ARROW

THIS RESISTOR IS HERE TO FIX A KODIAK BUG IN TERM_OFF MODE

R4311 110 RES 1% 1/16W MF-LF 402

REMOVED BACKUP TERMINATION OPTIONS TO OPTIMIZE ROUTING.

CRITICAL

OMIT

U4300

2.1GHZ-1.10V-45W-85C

GPUL10S-DD3.1-CBGA

GPUL

56 9	EI_NB_TO_CPU_CLK_P	ARROW	E24
56 9	EI_NB_TO_CPU_CLK_N	ARROW	D24
56	EI_NB_TO_CPU_AD<0>	ARROW	H21
56	EI_NB_TO_CPU_AD<1>	ARROW	J21
56	EI_NB_TO_CPU_AD<2>	ARROW	H22
56	EI_NB_TO_CPU_AD<3>	ARROW	J22
56	EI_NB_TO_CPU_AD<4>	ARROW	C13
56	EI_NB_TO_CPU_AD<5>	ARROW	A13
56	EI_NB_TO_CPU_AD<6>	ARROW	K22
56	EI_NB_TO_CPU_AD<7>	ARROW	H23
56	EI_NB_TO_CPU_AD<8>	ARROW	J24
56	EI_NB_TO_CPU_AD<9>	ARROW	G20
56	EI_NB_TO_CPU_AD<10>	ARROW	F23
56	EI_NB_TO_CPU_AD<11>	ARROW	G21
56	EI_NB_TO_CPU_AD<12>	ARROW	G22
56	EI_NB_TO_CPU_AD<13>	ARROW	G24
56	EI_NB_TO_CPU_AD<14>	ARROW	G19
56	EI_NB_TO_CPU_AD<15>	ARROW	B15
56	EI_NB_TO_CPU_AD<16>	ARROW	A14
56	EI_NB_TO_CPU_AD<17>	ARROW	C15
56	EI_NB_TO_CPU_AD<18>	ARROW	D15
56	EI_NB_TO_CPU_AD<19>	ARROW	A16
56	EI_NB_TO_CPU_AD<20>	ARROW	C22
56	EI_NB_TO_CPU_AD<21>	ARROW	E20
56	EI_NB_TO_CPU_AD<22>	ARROW	E21
56	EI_NB_TO_CPU_AD<23>	ARROW	B23
56	EI_NB_TO_CPU_AD<24>	ARROW	B24
56	EI_NB_TO_CPU_AD<25>	ARROW	F21
56	EI_NB_TO_CPU_AD<26>	ARROW	B17
56	EI_NB_TO_CPU_AD<27>	ARROW	B19
56	EI_NB_TO_CPU_AD<28>	ARROW	C14
56	EI_NB_TO_CPU_AD<29>	ARROW	C17
56	EI_NB_TO_CPU_AD<30>	ARROW	D18
56	EI_NB_TO_CPU_AD<31>	ARROW	B21
56	EI_NB_TO_CPU_AD<32>	ARROW	D20
56	EI_NB_TO_CPU_AD<33>	ARROW	A22
56	EI_NB_TO_CPU_AD<34>	ARROW	C19
56	EI_NB_TO_CPU_AD<35>	ARROW	C18
56	EI_NB_TO_CPU_AD<36>	ARROW	A21
56	EI_NB_TO_CPU_AD<37>	ARROW	A23
56	EI_NB_TO_CPU_AD<38>	ARROW	A20
56	EI_NB_TO_CPU_AD<39>	ARROW	A18
56	EI_NB_TO_CPU_AD<40>	ARROW	A15
56	EI_NB_TO_CPU_AD<41>	ARROW	A17
56	EI_NB_TO_CPU_AD<42>	ARROW	C16
56	EI_NB_TO_CPU_AD<43>	ARROW	A19
56 9	EI_NB_TO_CPU_SR_P<0>	ARROW	L24
56 9	EI_NB_TO_CPU_SR_N<0>	ARROW	K24
56	EI_NB_TO_CPU_SR_P<1>	ARROW	L21
56	EI_NB_TO_CPU_SR_N<1>	ARROW	L22
56	CPU_QACK_L	ARROW	V21
56 8	CPU_CHKSTOP_L	ARROW	R20
56	EI_CPU_TBEN_CLK	ARROW	A017
56	CPU_APSYNCOUT	ARROW	A014
29	CPU_HRESET_L	ARROW	V20
56	CPU_SRESET_L	ARROW	AB4
47	PROC_THERM_INT_L	ARROW	V22
47	PROCID0	ARROW	L19
47	PROCID1	ARROW	R19
47	PROCID2	ARROW	R18
56 47	CPU_TRIGGER_IN	ARROW	N21
56	CPU_TRIGGER_OUT	ARROW	N19
56	CPU_AFN	ARROW	AA12
47	AVPRESET_L	ARROW	W23
47	BIMODE_L	ARROW	AC24
47	C1UNDGLOBAL	ARROW	AC16
47	C2UNDGLOBAL	ARROW	AC15
47	DI2_L	ARROW	U24
47	LSSDMODE	ARROW	AB5
47	LSSDSCANENABLE	ARROW	U19
47	LSSDSTOPC2ENABLE	ARROW	AD8
47	LSSDSTOPC2STARENABLE	ARROW	AD7
47	LSSDSTOPENABLE	ARROW	AD11
56	CPU_MCP_L	ARROW	AD18
56	CPU_PSRO	ARROW	V23
56	CPU_PSRO_ENABLE	ARROW	Y5
47	PULSESEL0	ARROW	AC9
47	PULSESEL1	ARROW	AB11
47	PULSESEL2	ARROW	AC10
47	RAMSTOPENABLE	ARROW	AB6
47	RI_L	ARROW	AA5
47	SYNCENABLE	ARROW	AB24

PSRO_ENABLE

SPARE2

D3	ARROW	EI_CPU_TO_NB_CLK_P	9 56
E3	ARROW	EI_CPU_TO_NB_CLK_N	9 56
N3	ARROW	EI_CPU_TO_NB_AD<0>	56
M2	ARROW	EI_CPU_TO_NB_AD<1>	56
K3	ARROW	EI_CPU_TO_NB_AD<2>	56
L1	ARROW	EI_CPU_TO_NB_AD<3>	56
M3	ARROW	EI_CPU_TO_NB_AD<4>	56
K4	ARROW	EI_CPU_TO_NB_AD<5>	56
K2	ARROW	EI_CPU_TO_NB_AD<6>	56
M3	ARROW	EI_CPU_TO_NB_AD<7>	56
M1	ARROW	EI_CPU_TO_NB_AD<8>	56
G4	ARROW	EI_CPU_TO_NB_AD<9>	56
F2	ARROW	EI_CPU_TO_NB_AD<10>	56
F4	ARROW	EI_CPU_TO_NB_AD<11>	56
E2	ARROW	EI_CPU_TO_NB_AD<12>	56
G3	ARROW	EI_CPU_TO_NB_AD<13>	56
B8	ARROW	EI_CPU_TO_NB_AD<14>	56
D11	ARROW	EI_CPU_TO_NB_AD<15>	56
E12	ARROW	EI_CPU_TO_NB_AD<16>	56
A11	ARROW	EI_CPU_TO_NB_AD<17>	56
B10	ARROW	EI_CPU_TO_NB_AD<18>	56
C11	ARROW	EI_CPU_TO_NB_AD<19>	56
C1	ARROW	EI_CPU_TO_NB_AD<20>	56
C5	ARROW	EI_CPU_TO_NB_AD<21>	56
B2	ARROW	EI_CPU_TO_NB_AD<22>	56
D6	ARROW	EI_CPU_TO_NB_AD<23>	56
A5	ARROW	EI_CPU_TO_NB_AD<24>	56
A2	ARROW	EI_CPU_TO_NB_AD<25>	56
D2	ARROW	EI_CPU_TO_NB_AD<26>	56
D8	ARROW	EI_CPU_TO_NB_AD<27>	56
C12	ARROW	EI_CPU_TO_NB_AD<28>	56
A12	ARROW	EI_CPU_TO_NB_AD<29>	56
B6	ARROW	EI_CPU_TO_NB_AD<30>	56
B4	ARROW	EI_CPU_TO_NB_AD<31>	56
C4	ARROW	EI_CPU_TO_NB_AD<32>	56
C7	ARROW	EI_CPU_TO_NB_AD<33>	56
A7	ARROW	EI_CPU_TO_NB_AD<34>	56
C8	ARROW	EI_CPU_TO_NB_AD<35>	56
C6	ARROW	EI_CPU_TO_NB_AD<36>	56
A4	ARROW	EI_CPU_TO_NB_AD<37>	56
A9	ARROW	EI_CPU_TO_NB_AD<38>	56
C9	ARROW	EI_CPU_TO_NB_AD<39>	56
A10	ARROW	EI_CPU_TO_NB_AD<40>	56
C10	ARROW	EI_CPU_TO_NB_AD<41>	56
A8	ARROW	EI_CPU_TO_NB_AD<42>	56
A6	ARROW	EI_CPU_TO_NB_AD<43>	56
L3	ARROW	EI_CPU_TO_NB_SR_P<0>	56
L2	ARROW	EI_CPU_TO_NB_SR_N<0>	56
G1	ARROW	EI_CPU_TO_NB_SR_P<1>	9 56
F1	ARROW	EI_CPU_TO_NB_SR_N<1>	9 56
AB12	ARROW	CPU_QREQ_L	43
AB19	ARROW	CPU_INT_L	56
AA10	ARROW	EI_CPU_APSYNC	56
AA20	ARROW	I2C_CPU_SCL	47
Y21	ARROW	I2C_CPU_SDA	47
N22	ARROW	I2CG0	47
AA14	ARROW	CKTERMDIS_L	47
P20	ARROW	EI_DISABLE	47
AA19	ARROW	BUSCFG0	47
AC19	ARROW	BUSCFG1	47
AB16	ARROW	BUSCFG2	47
AD12	ARROW	CPU_ATTENTION	56
AA22	ARROW	GPUL_DBG	47
W4	UNDEFINED	CPU_SPARE2	9 47
AD21	ARROW	JTAG_CPU_TCK	9 30
AB21	ARROW	JTAG_CPU_TDI	9 30
AD13	ARROW	JTAG_CPU_TDO	9 30 47
AD22	ARROW	JTAG_CPU_TMS	9 30
W20	ARROW	JTAG_CPU_TRST_L	9 47
V24	ARROW	CPU_BYPASS_L	29
T20	ARROW	PLLLOCK	8 9
AA8	ARROW	PLLMULT	47
AB7	ARROW	PLLRANGE0	47
AA9	ARROW	PLLRANGE1	47
W22	ARROW	PLLTEST	47
T19	ARROW	PLLTESTOUT	9 47
AA13	ARROW	CPU_SPARE	47

PCB: MATCH APSYNC LENGTH TO SYSCLK

PG 49 & 52 HAVE MORE CAPS

56 55 52 50 49 48 =PPVCORE_CPU

C4353 C4347 C4345 C4339 C4337 C4328 C4324 C4320 C4314 C4312
C4354 C4348 C4346 C4340 C4338 C4329 C4325 C4321 C4315 C4313
C4355 C4351 C4349 C4343 C4341 C4330 C4326 C4322 C4318 C4316
C4356 C4352 C4350 C4344 C4342 C4331 C4327 C4323 C4319 C4317
C4300 C4360 C4359 C4358 C4357 C4336 C4335 C4334 C4333 C4332
C4311 C4310 C4309 C4308 C4307 C4306 C4305 C4304 C4303 C4302

1 CAP 1UF 10% 6.3V 2 CERM 402

GND

QREQ_L AND SUSPENDREQ_L AND HACK

SAME AS Q45

30 28 7 =PP3V3_PWRON_SMU

C4372 0.1UF 1 CAP 20% 10V 2 CERM 402

GND

CRITICAL

U4310 74LVC1G66DBVG4 SOT23-5 TI

74LVC1G66

43 CPU_QREQ_L — 1 — 2 — CPU_TO_NB_QREQ_L 56

30 28 24 SMU_SUSPENDREQ_L — 4

3 GND

NOSTUFF R4310 0 RES 1 2 5% 1/16W MF-LF 402

CPU EI AND IO

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

051-6863 H

43 154

APPLE_DSIZEPAGE

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

KODIAK

U1900
BGA

KODIAK-ASIC-040812

56	EI_NB_TO_CPU_B_CLK_P	AT08
56	EI_NB_TO_CPU_B_CLK_N	AR08
56	EI_NB_TO_CPU_B_AD<0>	AM12
56	EI_NB_TO_CPU_B_AD<1>	AN12
56	EI_NB_TO_CPU_B_AD<2>	AL12
56	EI_NB_TO_CPU_B_AD<3>	AK12
56	EI_NB_TO_CPU_B_AD<4>	AP11
56	EI_NB_TO_CPU_B_AD<5>	AL11
56	EI_NB_TO_CPU_B_AD<6>	AP12
56	EI_NB_TO_CPU_B_AD<7>	AR12
56	EI_NB_TO_CPU_B_AD<8>	AT12
56	EI_NB_TO_CPU_B_AD<9>	AH12
56	EI_NB_TO_CPU_B_AD<10>	AG12
56	EI_NB_TO_CPU_B_AD<11>	AH13
56	EI_NB_TO_CPU_B_AD<12>	AJ12
56	EI_NB_TO_CPU_B_AD<13>	AG14
56	EI_NB_TO_CPU_B_AD<14>	AM10
56	EI_NB_TO_CPU_B_AD<15>	AL10
56	EI_NB_TO_CPU_B_AD<16>	AN10
56	EI_NB_TO_CPU_B_AD<17>	AP10
56	EI_NB_TO_CPU_B_AD<18>	AR10
56	EI_NB_TO_CPU_B_AD<19>	AT10
56	EI_NB_TO_CPU_B_AD<20>	AK10
56	EI_NB_TO_CPU_B_AD<21>	AJ10
56	EI_NB_TO_CPU_B_AD<22>	AM08
56	EI_NB_TO_CPU_B_AD<23>	AN08
56	EI_NB_TO_CPU_B_AD<24>	AL08
56	EI_NB_TO_CPU_B_AD<25>	AP07
56	EI_NB_TO_CPU_B_AD<26>	AT06
56	EI_NB_TO_CPU_B_AD<27>	AR06
56	EI_NB_TO_CPU_B_AD<28>	AP08
56	EI_NB_TO_CPU_B_AD<29>	AT04
56	EI_NB_TO_CPU_B_AD<30>	AR04
56	EI_NB_TO_CPU_B_AD<31>	AP05
56	EI_NB_TO_CPU_B_AD<32>	AM06
56	EI_NB_TO_CPU_B_AD<33>	AN06
56	EI_NB_TO_CPU_B_AD<34>	AP06
56	EI_NB_TO_CPU_B_AD<35>	AP04
56	EI_NB_TO_CPU_B_AD<36>	AM03
56	EI_NB_TO_CPU_B_AD<37>	AN01
56	EI_NB_TO_CPU_B_AD<38>	AL06
56	EI_NB_TO_CPU_B_AD<39>	AL05
56	EI_NB_TO_CPU_B_AD<40>	AL04
56	EI_NB_TO_CPU_B_AD<41>	AL03
56	EI_NB_TO_CPU_B_AD<42>	AN02
56	EI_NB_TO_CPU_B_AD<43>	AN03
56	EI_NB_TO_CPU_B_SR_P<0>	AP09
56	EI_NB_TO_CPU_B_SR_N<0>	AL09
56	EI_NB_TO_CPU_B_SR_P<1>	AR02
56	EI_NB_TO_CPU_B_SR_N<1>	AP03
56	CPU_B0_QACK_L	AF14
56	CPU_B1_QACK_L	AC11
56 44	NB_CPU_B0_INT_L	N11
56 44	NB_CPU_B1_INT_L	U11
9	TP_NB_APSYNC	AH11
56	NB_B_TRIGGER_OUT	AK08

WIRE TP_NB_APSYNC TO A TEST POINT

P4MM SM PROBEPOINT PP4406
P4MM SM PROBEPOINT PP4407
P4MM SM PROBEPOINT PP4408

NET_SPACING_TYPE

NB_CPU_B0_INT_L	P3MM_SPACING	44 56
NB_CPU_B1_INT_L	P3MM_SPACING	44 56

EI INPUT FROM CPU B

AT16	EI_CPU_B_TO_NB_CLK_P	56
AR16	EI_CPU_B_TO_NB_CLK_N	56
AP20	EI_CPU_B_TO_NB_AD<0>	56
AN20	EI_CPU_B_TO_NB_AD<1>	56
AR20	EI_CPU_B_TO_NB_AD<2>	56
AT20	EI_CPU_B_TO_NB_AD<3>	56
AL19	EI_CPU_B_TO_NB_AD<4>	56
AP19	EI_CPU_B_TO_NB_AD<5>	56
AM20	EI_CPU_B_TO_NB_AD<6>	56
AM18	EI_CPU_B_TO_NB_AD<7>	56
AL18	EI_CPU_B_TO_NB_AD<8>	56
AN18	EI_CPU_B_TO_NB_AD<9>	56
AP18	EI_CPU_B_TO_NB_AD<10>	56
AR18	EI_CPU_B_TO_NB_AD<11>	56
AT18	EI_CPU_B_TO_NB_AD<12>	56
AK18	EI_CPU_B_TO_NB_AD<13>	56
AP17	EI_CPU_B_TO_NB_AD<14>	56
AL17	EI_CPU_B_TO_NB_AD<15>	56
AH20	EI_CPU_B_TO_NB_AD<16>	56
AJ20	EI_CPU_B_TO_NB_AD<17>	56
AK20	EI_CPU_B_TO_NB_AD<18>	56
AH19	EI_CPU_B_TO_NB_AD<19>	56
AG20	EI_CPU_B_TO_NB_AD<20>	56
AL20	EI_CPU_B_TO_NB_AD<21>	56
AM16	EI_CPU_B_TO_NB_AD<22>	56
AN16	EI_CPU_B_TO_NB_AD<23>	56
AL16	EI_CPU_B_TO_NB_AD<24>	56
AK16	EI_CPU_B_TO_NB_AD<25>	56
AP15	EI_CPU_B_TO_NB_AD<26>	56
AL15	EI_CPU_B_TO_NB_AD<27>	56
AP16	EI_CPU_B_TO_NB_AD<28>	56
AM14	EI_CPU_B_TO_NB_AD<29>	56
AL14	EI_CPU_B_TO_NB_AD<30>	56
AN14	EI_CPU_B_TO_NB_AD<31>	56
AP14	EI_CPU_B_TO_NB_AD<32>	56
AR14	EI_CPU_B_TO_NB_AD<33>	56
AT14	EI_CPU_B_TO_NB_AD<34>	56
AK14	EI_CPU_B_TO_NB_AD<35>	56
AP13	EI_CPU_B_TO_NB_AD<36>	56
AL13	EI_CPU_B_TO_NB_AD<37>	56
AG16	EI_CPU_B_TO_NB_AD<38>	56
AH15	EI_CPU_B_TO_NB_AD<39>	56
AJ14	EI_CPU_B_TO_NB_AD<40>	56
AH14	EI_CPU_B_TO_NB_AD<41>	56
AH16	EI_CPU_B_TO_NB_AD<42>	56
AH17	EI_CPU_B_TO_NB_AD<43>	56
AG18	EI_CPU_B_TO_NB_SR_P<0>	56
AJ16	EI_CPU_B_TO_NB_SR_N<0>	56
AJ18	EI_CPU_B_TO_NB_SR_P<1>	56
AH18	EI_CPU_B_TO_NB_SR_N<1>	56
AF16	CPU_B0_TO_NB_QREQ_L	44
AF20	CPU_B1_TO_NB_QREQ_L	44

P4MM SM PROBEPOINT PP4410
P4MM SM PROBEPOINT PP4411
P4MM SM PROBEPOINT PP4413
P4MM SM PROBEPOINT PP4400
P4MM SM PROBEPOINT PP4401
P4MM SM PROBEPOINT PP4402
P4MM SM PROBEPOINT PP4403
P4MM SM PROBEPOINT PP4404
P4MM SM PROBEPOINT PP4405

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT
ELECTRICAL_CONSTRAINT_SET
FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

PULL DOWN QREQS TO NB

44 CPU_B0_TO_NB_QREQ_L — R4407 10K RES 1 2 5% 1/16W MF-LF 402
44 CPU_B1_TO_NB_QREQ_L — R4406 10K RES 1 2 5% 1/16W MF-LF 402
R4406 and R4407 → GND

KODIAK EI B

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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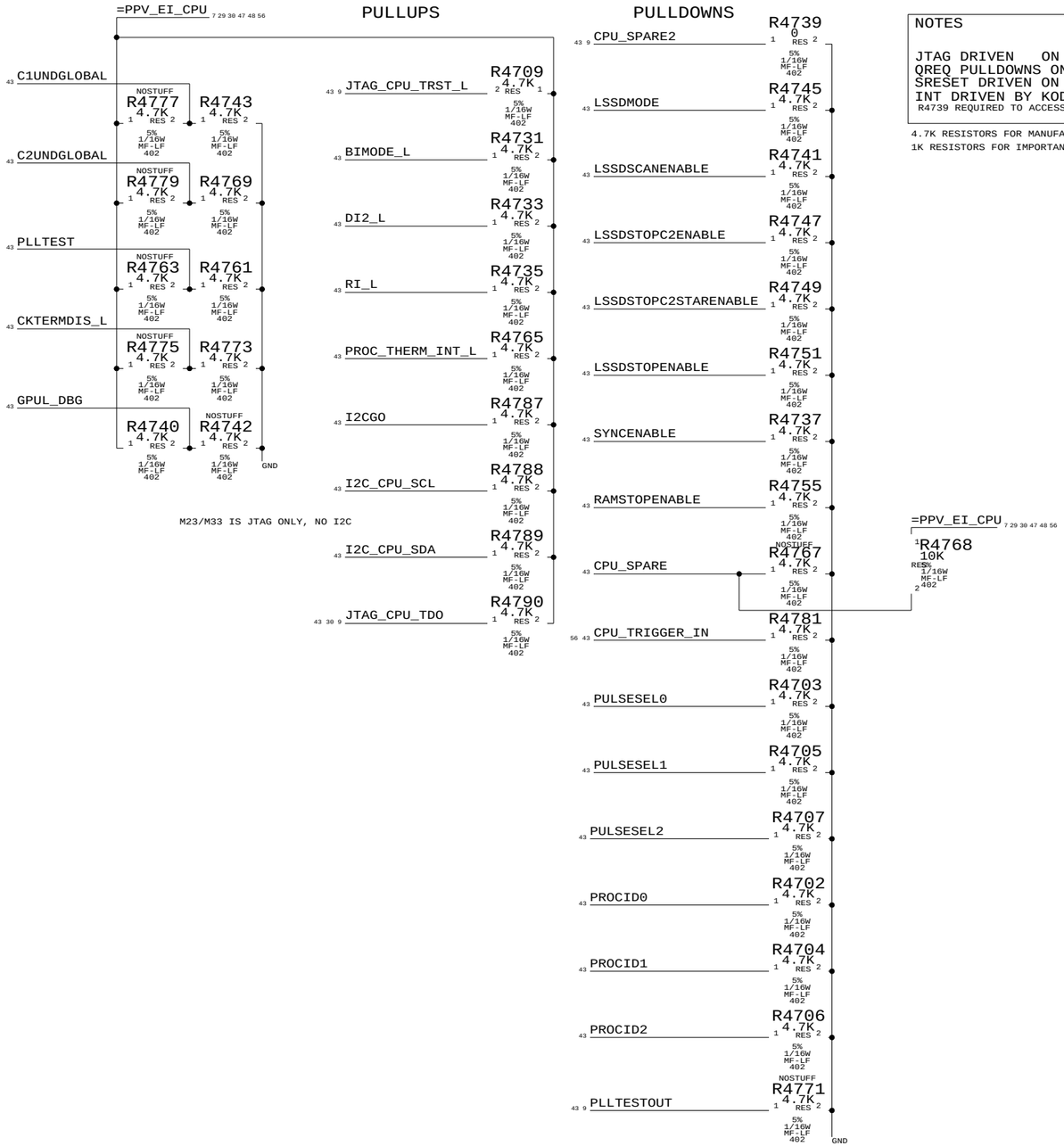
LAST_MODIFIED=Fri Apr 28 20:23:00 2006
DRAWING

APPLE_DSIZEPAGE



NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK
R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

TABLE_5_HEAD					
TABLE_5_ITEM					
*	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
TABLE_5_ITEM					
	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

TABLE_5_HEAD					
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
TABLE_5_ITEM					
	116S0066 3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

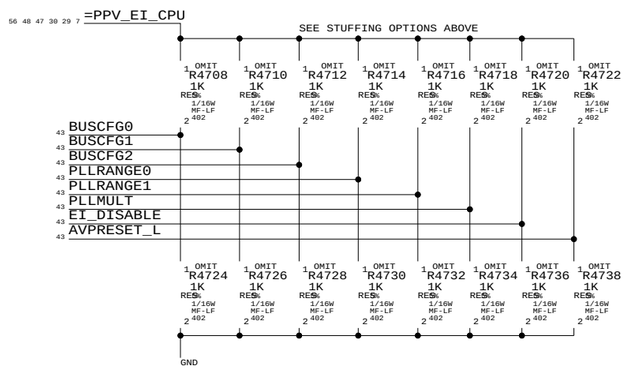
TABLE_5_HEAD					
TABLE_5_ITEM					
*	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4736		
TABLE_5_ITEM					
	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

SELECT PLL FREQUENCY RANGE.

TABLE_5_HEAD					
TABLE_5_ITEM					
>= 1.8 GHZ *	116S0066 2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	
TABLE_5_ITEM					
	116S0066 2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
TABLE_5_ITEM					
	116S0066 2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
TABLE_5_ITEM					
	116S0066 2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED
TABLE_5_HEAD					
TABLE_5_ITEM					
	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
	116S0066 1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



CPU STRAPS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

54 PPV_RUN_AVDD_CPU

R4832 2.2 RES 5% 1/10W MF-LF 603

PPV_RUN_CPU_AVDD_R
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM

L4801 60-OHM-EMI IND SM 0805

6 PPV_RUN_CPU_AVDD_R_L
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.60MM
MIN_NECK_WIDTH=0.20MM

C4802 CAP 10UF 10% 6.3V X5R 805

C4800 CAP 0.1UF 10% 16V X5R 402

56 55 52 50 49 43 =PPVCORE_CPU
VOLTAGE=1.3V
MIN_LINE_WIDTH=0.50MM
MIN_NECK_WIDTH=0.20MM

=PPV_EI_CPU 7 29 30 47 56

NET_PHYSICAL_TYPE=PROC_DIFF
NET_SPACING_TYPE=PROC_DIFF
DIFFERENTIAL_PAIR=P_TDO
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM

CPU_DIODE_POS 6 55

P24 Y1 R2

DIODEPOS

OMIT CRITICAL
U4300
2.1GHZ-1.10V-45W-85C
GPUL10S-DD3.1-CBGA

GPUL

SPARE_GND

GND

DIODENEG

R24 AA1 T2

6 GND_CPU_AVDD

2 OMIT
XW4800
SHORT
1
GND

55 6 CPU_DIODE_NEG
DIFFERENTIAL_PAIR=P_TDD
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

NOSTUFF
R4810 100K RES 5% 1/10W MF-LF 603

PROCESSOR KELVIN POINT PROBE POINT

KPVDD2 6 50 55
DIFFERENTIAL_PAIR=P_KP2
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

REMEMBER TO CHANGE KPVDD TO NO_TEST ON PG 6.
PCB:PUT R4810 AS CLOSE TO RESPECTIVE PINS AS POSSIBLE.

KPGND2 6 50 55
DIFFERENTIAL_PAIR=P_KP2
MIN_LINE_WIDTH=0.25MM
MIN_NECK_WIDTH=0.20MM
NET_SPACING_TYPE=PROC_DIFF
NET_PHYSICAL_TYPE=PROC_DIFF

CRITICAL
OMIT
U4300
2.1GHZ-1.10V-45W-85C
GPUL10S-DD3.1-CBGA

Z_OUT
Z_SENSE

GPUL

GND

C4817 CAP 10UF 10% 6.3V X5R 805
C4816 CAP 10UF 10% 6.3V X5R 805
C4815 CAP 10UF 10% 6.3V X5R 805
C4814 CAP 10UF 10% 6.3V X5R 805

C4811 CAP 0.1UF 20% 10V CERM 402
C4806 CAP 0.1UF 20% 10V CERM 402
C4805 CAP 0.1UF 20% 10V CERM 402
C4803 CAP 0.1UF 20% 10V CERM 402
C4812 CAP 0.1UF 20% 10V CERM 402
C4809 CAP 0.1UF 20% 10V CERM 402
C4807 CAP 0.1UF 20% 10V CERM 402
C4804 CAP 0.1UF 20% 10V CERM 402
C4813 CAP 0.1UF 20% 10V CERM 402
C4810 CAP 0.1UF 20% 10V CERM 402
C4808 CAP 0.1UF 20% 10V CERM 402
C4826 CAP 0.1UF 20% 10V CERM 402
C4820 CAP 0.1UF 20% 10V CERM 402
C4818 CAP 0.1UF 20% 10V CERM 402
C4827 CAP 0.1UF 20% 10V CERM 402
C4821 CAP 0.1UF 20% 10V CERM 402
C4819 CAP 0.1UF 20% 10V CERM 402
C4828 CAP 0.1UF 20% 10V CERM 402
C4824 CAP 0.1UF 20% 10V CERM 402
C4822 CAP 0.1UF 20% 10V CERM 402
C4829 CAP 0.1UF 20% 10V CERM 402
C4825 CAP 0.1UF 20% 10V CERM 402
C4823 CAP 0.1UF 20% 10V CERM 402
C4836 CAP 0.1UF 20% 10V CERM 402
C4831 CAP 0.1UF 20% 10V CERM 402
C4830 CAP 0.1UF 20% 10V CERM 402
C4837 CAP 0.1UF 20% 10V CERM 402
C4834 CAP 0.1UF 20% 10V CERM 402
C4832 CAP 0.1UF 20% 10V CERM 402
C4838 CAP 0.1UF 20% 10V CERM 402
C4835 CAP 0.1UF 20% 10V CERM 402
C4833 CAP 0.1UF 20% 10V CERM 402
C4845 CAP 0.1UF 20% 10V CERM 402
C4841 CAP 0.1UF 20% 10V CERM 402
C4839 CAP 0.1UF 20% 10V CERM 402
C4846 CAP 0.1UF 20% 10V CERM 402
C4842 CAP 0.1UF 20% 10V CERM 402
C4840 CAP 0.1UF 20% 10V CERM 402
C4847 CAP 0.1UF 20% 10V CERM 402
C4844 CAP 0.1UF 20% 10V CERM 402
C4843 CAP 0.1UF 20% 10V CERM 402

GND

CPU POWER AND BYPASS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

56 55 52 50 48 43 =PPVCORE_CPU

C4922	C4921	C4920	C4919	C4918	C4917	C4916	C4915	C4912	C4900
C4993	C4968	C4961	C4959	C4935	C4932	C4926	C4924	C4945	C4923
C4994	C4969	C4964	C4960	C4936	C4933	C4927	C4925	C4956	C4934
C4995	C4971	C4965	C4962	C4939	C4937	C4930	C4928	C4989	C4967
C4996	C4970	C4966	C4963	C4940	C4938	C4931	C4929	C4901	C4978
C4997	C4982	C4976	C4972	C4952	C4950	C4943	C4941	C4906	C4904
C4998	C4981	C4977	C4973	C4953	C4951	C4944	C4942	C4907	C4905
C4999	C4984	C4979	C4974	C4957	C4954	C4948	C4946	C4910	C4908
C4902	C4983	C4980	C4975	C4958	C4955	C4949	C4947	C4911	C4909
C4903	C4992	C4991	C4990	C4988	C4987	C4986	C4985	C4914	C4913

Each: 1 CAP 1UF 10% 6.3V CERM 402 2

GND

PROC DECOUPLING

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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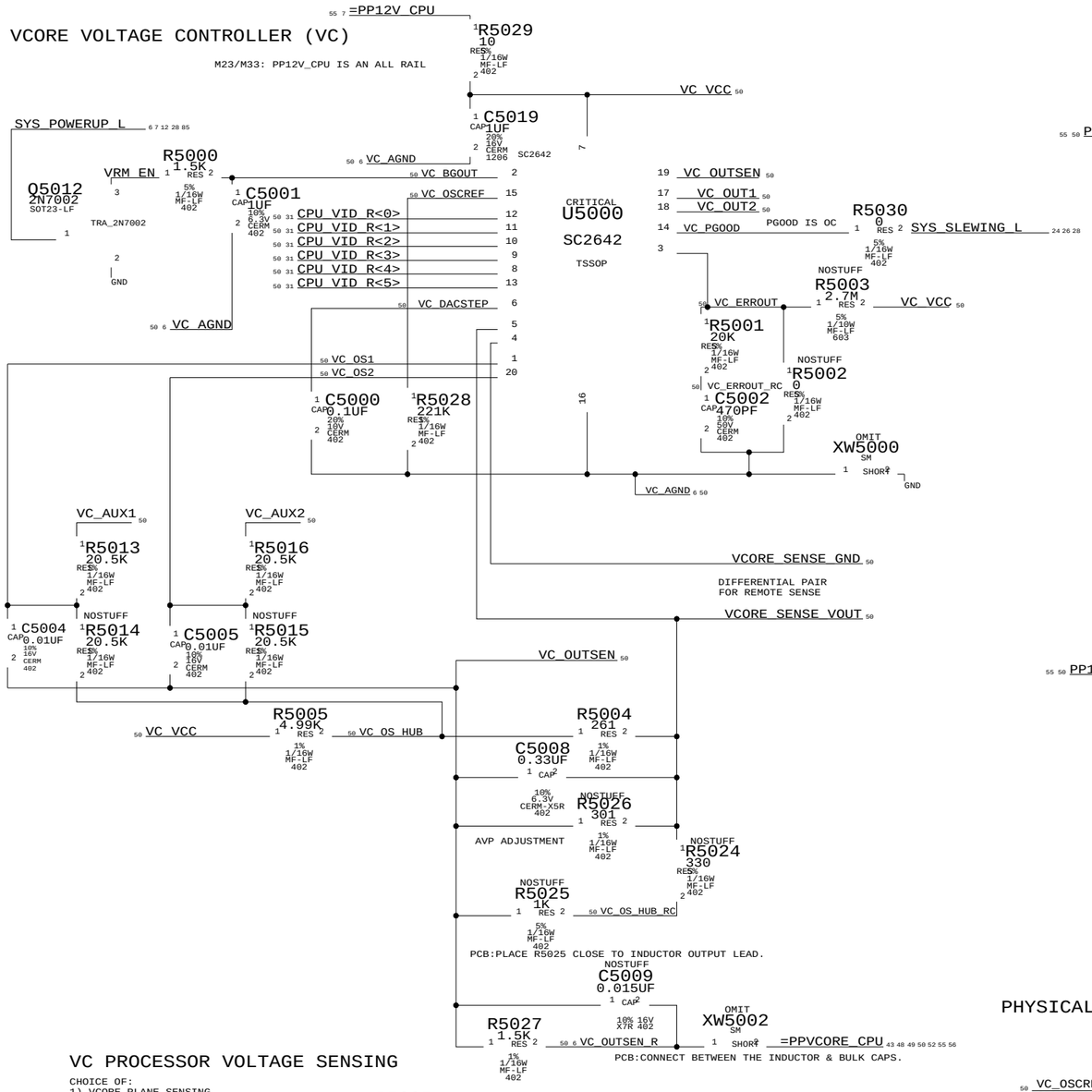
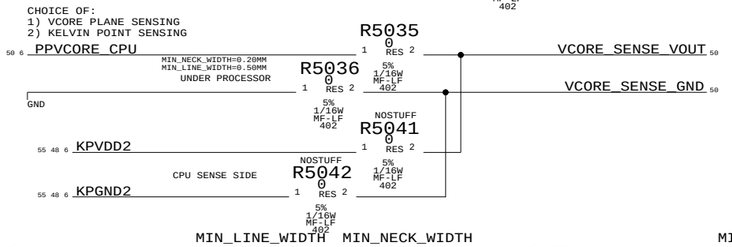
APPLE_DSIZEPAGE

VCORE VOLTAGE CONTROLLER (VC)

M23/M33: PP12V_CPU IS AN ALL RAIL



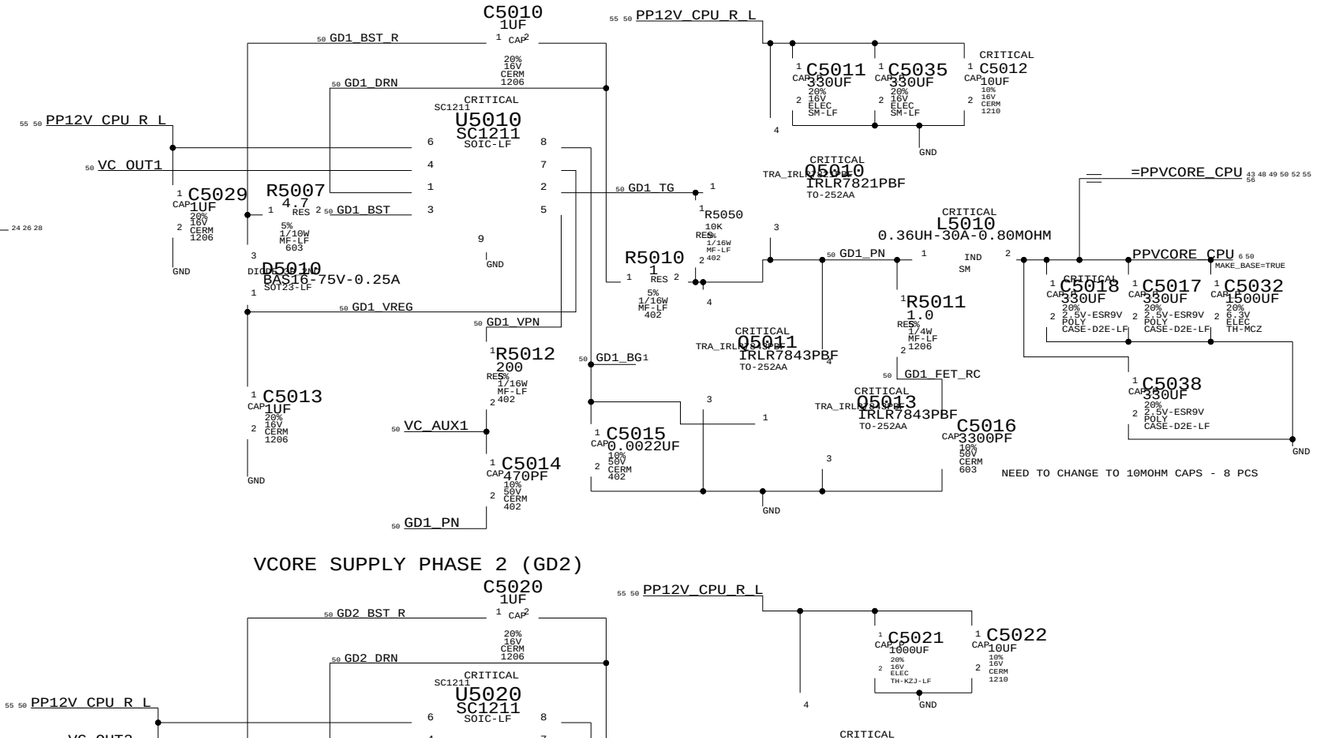
VC PROCESSOR VOLTAGE SENSING



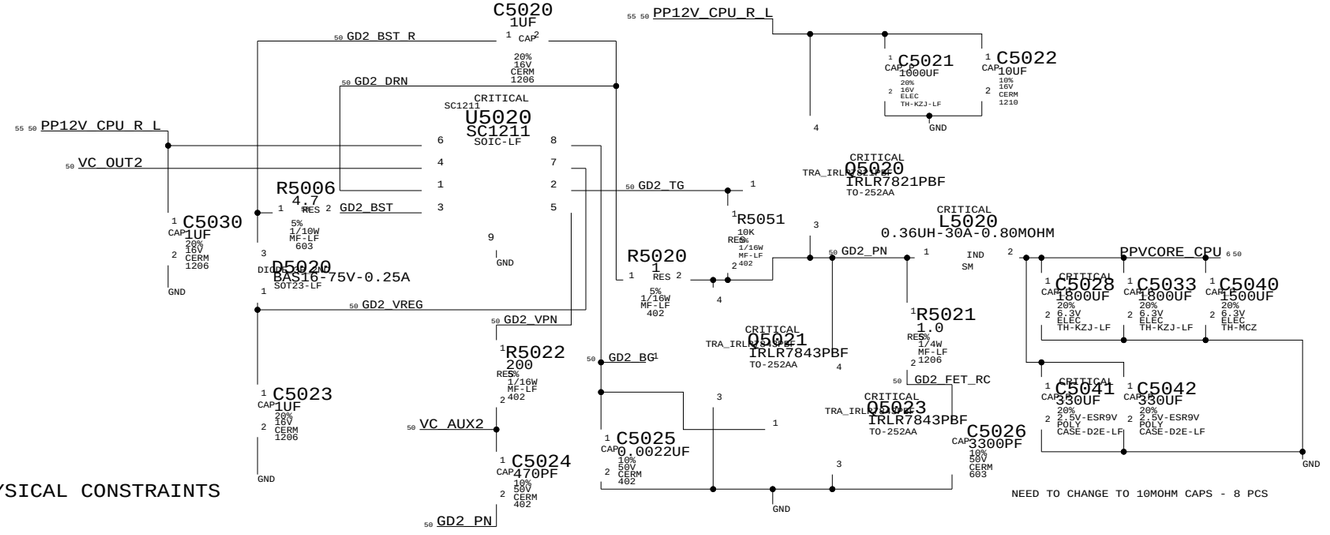
	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD1_DRN	0.25 MM	0.25 MM	4482
GD1_BST	0.25 MM	0.25 MM	4483
GD1_VREG	0.25 MM	0.25 MM	4484
GD1_VPN	0.25 MM	0.25 MM	4434
GD1_TG	0.25 MM	0.25 MM	4435
GD1_BG	0.25 MM	0.25 MM	4438
GD1_FET_RC	0.25 MM	0.25 MM	4437
GD1_PN	0.60 MM	0.25 MM	4439
GD1_BST_R	0.25 MM	0.25 MM	4440

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD2_DRN	0.25 MM	0.25 MM	4490
GD2_BST	0.25 MM	0.25 MM	4491
GD2_VREG	0.25 MM	0.25 MM	4492
GD2_VPN	0.25 MM	0.25 MM	4494
GD2_TG	0.25 MM	0.25 MM	4493
GD2_BG	0.25 MM	0.25 MM	4496
GD2_FET_RC	0.25 MM	0.25 MM	4495
GD2_PN	0.60 MM	0.25 MM	4497
GD2_BST_R	0.25 MM	0.25 MM	4498

VCORE SUPPLY PHASE 1 (GD1)



VCORE SUPPLY PHASE 2 (GD2)



PHYSICAL CONSTRAINTS

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	4470
CPU_VID_R<0..5>	0.25 MM	0.20 MM	4471
VC_DACSTEP	0.25 MM	0.20 MM	4476
VC_AGND	0.50 MM	0.20 MM	4478
VC_BGOUT	0.25 MM	0.20 MM	4480
VC_OS1	0.25 MM	0.20 MM	4475
VC_OS2	0.25 MM	0.20 MM	4482
VC_VCC	0.25 MM	0.25 MM	4481
VC_OS_HUB	0.25 MM	0.20 MM	4488
VC_OUTSEN	0.25 MM	0.20 MM	4484
VC_OUTSEN_R	0.25 MM	0.20 MM	4486
VCORE_SENSE_GND	0.25 MM	0.20 MM	4486
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	4487
VC_AUX1	0.25 MM	0.25 MM	4488
VC_AUX2	0.25 MM	0.25 MM	4489
VC_OUT1	0.45 MM	0.25 MM	4491
VC_OUT2	0.45 MM	0.25 MM	4490
VC_EROUT	0.25 MM	0.20 MM	4496
VC_EROUT_RC	0.25 MM	0.20 MM	4499
VC_OS_HUB_RC	0.25 MM	0.20 MM	4497

CPU VCORE VREG

SYNC_MASTER=M33-HS SYNC_DATE=06/20/2005

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56 55 50 49 48 43 =PPVCORE_CPU

CRITICAL

C5200	C5212	C5223	C5234	C5245	C5201	C5289	C5278	C5267	C5256
C5213	C5211	C5210	C5209	C5208	C5207	C5206	C5205	C5204	C5203
C5224	C5222	C5221	C5220	C5219	C5218	C5217	C5216	C5215	C5214
C5235	C5233	C5232	C5231	C5230	C5229	C5228	C5227	C5226	C5225
C5246	C5244	C5243	C5242	C5241	C5240	C5239	C5238	C5237	C5236
C5257	C5255	C5254	C5253	C5252	C5251	C5250	C5249	C5248	C5247
C5268	C5266	C5265	C5264	C5263	C5262	C5261	C5260	C5259	C5258
C5279	C5277	C5276	C5275	C5274	C5273	C5272	C5271	C5270	C5269
C5290	C5288	C5287	C5286	C5285	C5284	C5283	C5282	C5281	C5280
C5202	C5299	C5298	C5297	C5296	C5295	C5294	C5293	C5292	C5291

Each: 1 CAP 10UF 10% 6.3V 2 X5R 805

GND

CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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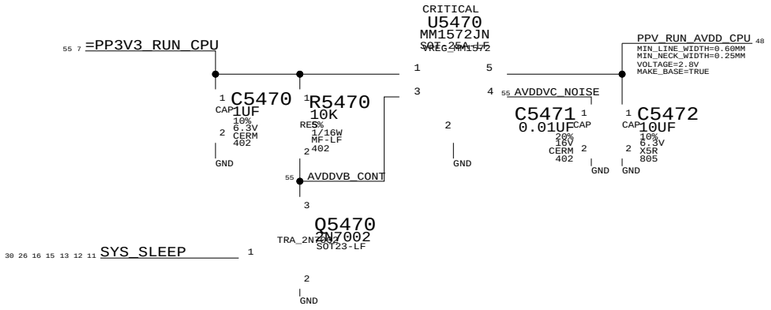
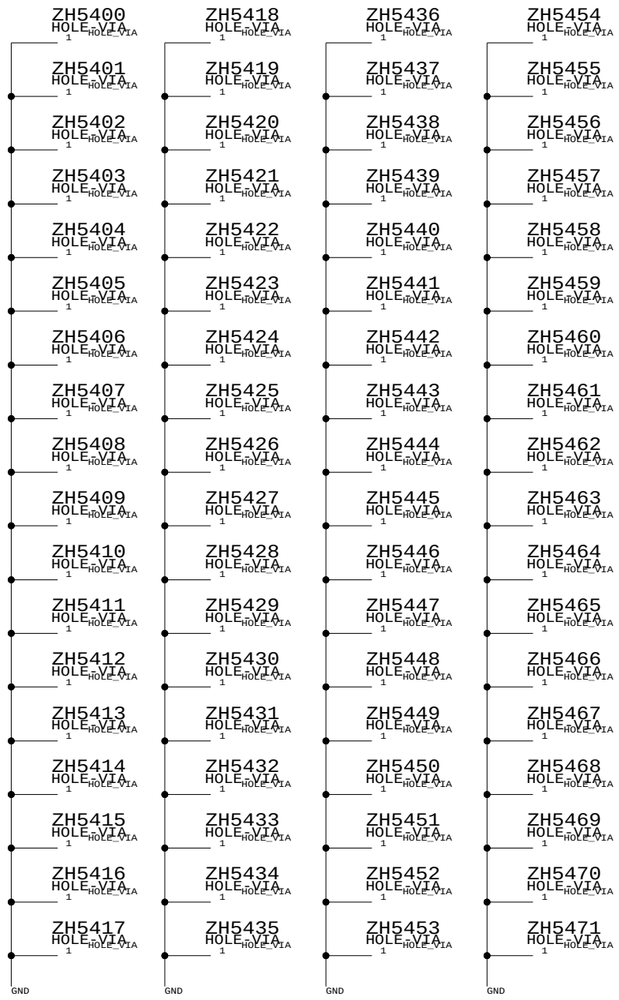
APPLE_DSIZEPAGE

PROCESSOR AVDD VREG





CPU AVDD VREG

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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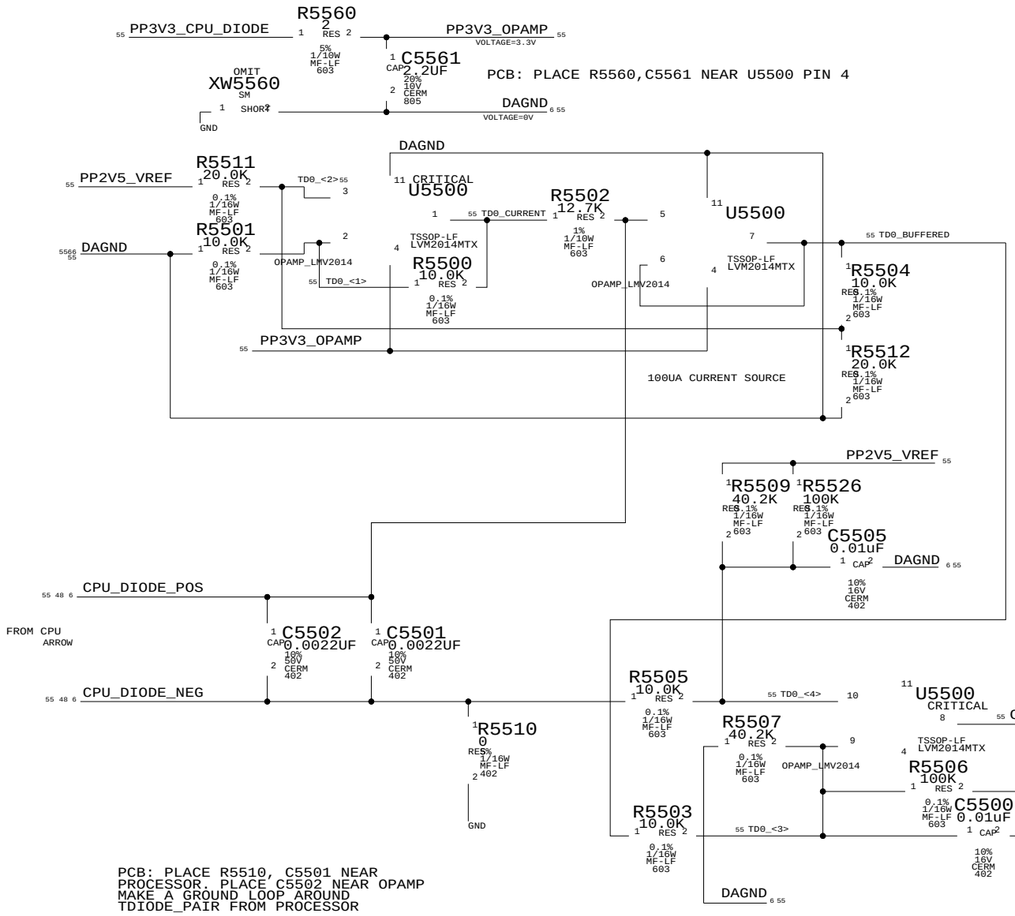
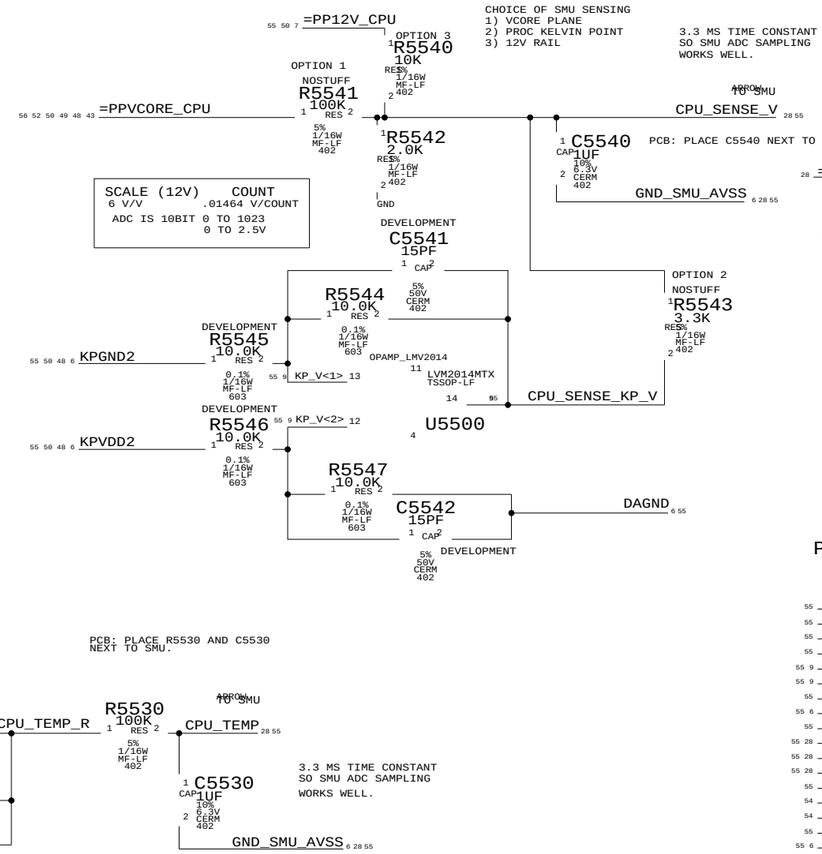
APPLE_DSIZEPAGE

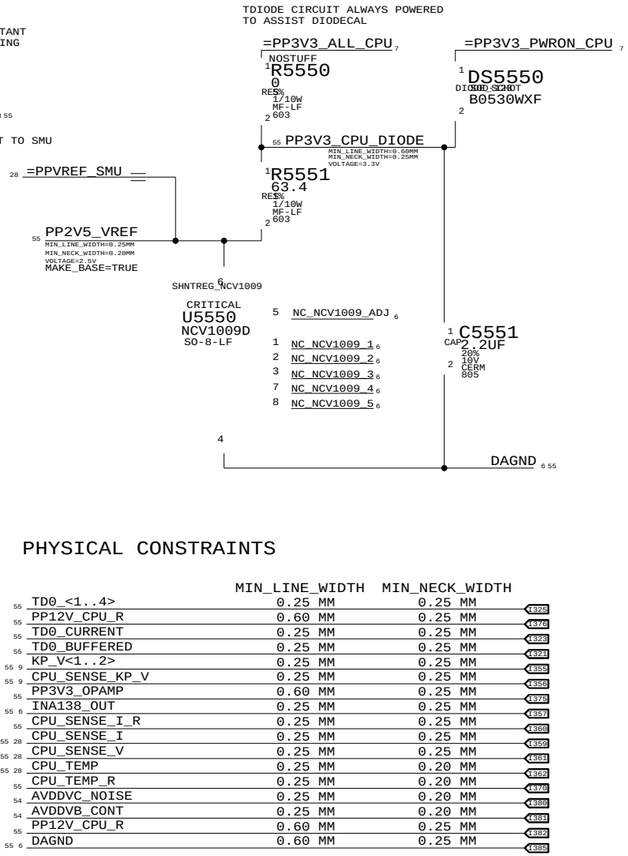
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



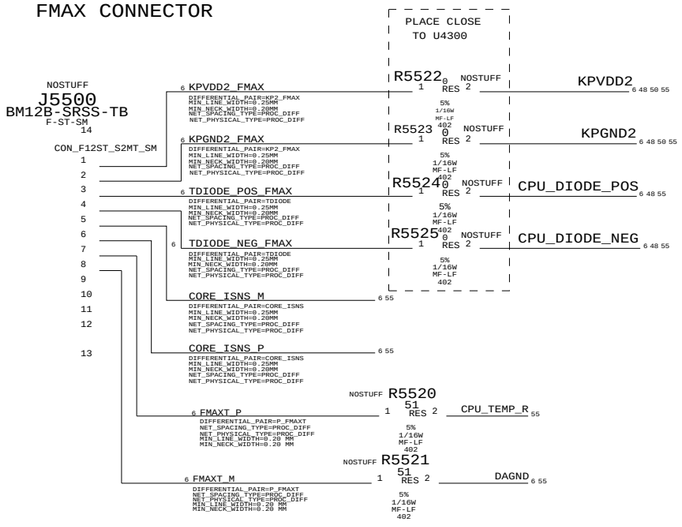
2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

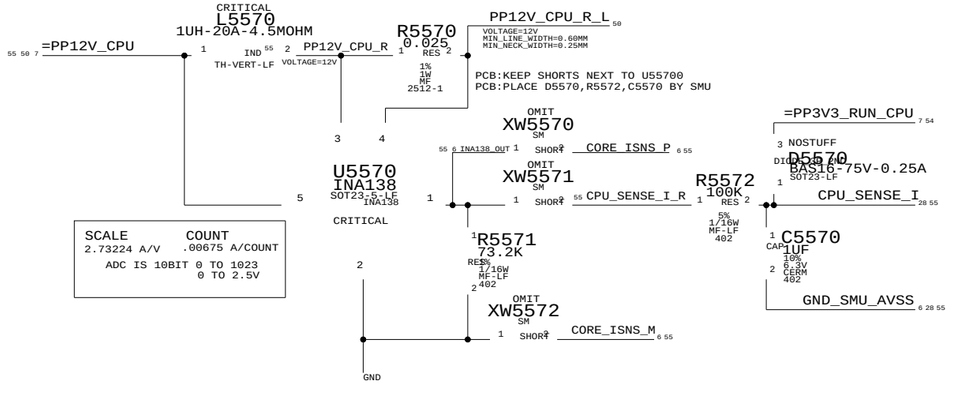
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.25 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/29/2005

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APPLE_DSIZEPAGE

CONNECT PULSAR CLKS TO CPU/NB

56 43 9	EI_CPU_SYSCLK_P	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_P	26
56 43	EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N	26
56 43	EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC	26
43	EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US	26
56	EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC	26 42

CONNECT KODIAK EI A TO/FROM CPU

56 43 9	EI_NB_TO_CPU_CLK_P	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_P	42
56 43 9	EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N	42
56 43	EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43>	42
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1>	42
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1>	42
		MAKE_BASE=TRUE		
56 43 9	EI_CPU_TO_NB_CLK_P	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_P	42
56 43 9	EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N	42
56 43	EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43>	42
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1>	42
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1>	42
		MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L	MAKE_BASE=TRUE	CPU_A0_TO_NB_QREQ_L	42

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L		CPU_A0_QACK_L	42
6	NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L	42
6	NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L	44
6	NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L	44
		MAKE_BASE=TRUE		

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L		CPU_A0_INT_R_L	24 56
6	NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L	42
6	NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L	44
6	NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L	44
		MAKE_BASE=TRUE		

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

	CPU_SRESET_L_R		SB_CPU_A0_SRESET_L	24 56
	NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L	24 56
	NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L	24 56
	NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L	24 56
		MAKE_BASE=TRUE		

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

9	TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT	44
9	TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT	42
	TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT	43
	TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN	43 47
9	TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT	43
9	NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO	43
9	NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE	43
	TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION	43
9	NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN	43
		MAKE_BASE=TRUE		

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

CPU CHKSTOP OR MCP TO NB

56 48 47 30 29 7 =PPV_EI_CPU

R5600 1K 1 RES 2 5% 1/16W MF-LF 402

NB_STOP_IS_CHKSTOP

R5601 0 1 RES 2 5% 1/16W MF-LF 402

TO/FROM CPU ARROW ARROW 43 8 CPU_CHKSTOP_L

R5602 4.7K 1 RES 2 5% 1/16W MF-LF 402

NB_STOP_IS_MCP

R5603 0 1 RES 2 5% 1/16W MF-LF 402

TO CPU ARROW 43 CPU_MCP_L

ARROW ARROW TO/FROM NB

NB_CHKSTOP_L 42

EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9 EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	126
56 43 9 EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43 EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43 9 EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43 9 EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43 9 EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43 9 EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
56 43 EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43 9 EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		136
56 43 9 EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
56 EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		133
56 43 EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43 9 EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	140
56 43 EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
42 26 EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	139
42 26 EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
56 43 EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1195
56 43 EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1196

NC KODIAK EI B OUTPUT PORT

6	NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P	44
6	NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N	44
6	NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43>	44
6	NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1>	44
6	NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1>	44
		MAKE_BASE=TRUE		

NC KODIAK EI B INPUT PORT

6	NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P	44
6	NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N	44
6	NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43>	44
6	NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1>	44
6	NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1>	44
		MAKE_BASE=TRUE		

PULLUPS FOR SRESET'S FROM SHASTA

119 24 23 20 7 =PP3V3_PWRON_SB

ALL SHASTA GPIOS MUST HAVE A PULL-UP WHEN SHASTA IS STARTING UP.

NOSTUFF

R5608 10K 2 RES 1 SB_CPU_A0_SRESET_L 24 56

R5609 10K 2 RES 1 SB_CPU_A1_SRESET_L 24 56

R5610 10K 2 RES 1 SB_CPU_B0_SRESET_L 24 56

R5611 10K 2 RES 1 SB_CPU_B1_SRESET_L 24 56

5% 1/16W MF-LF 402

56 48 47 30 29 7 =PPV_EI_CPU

IF SHASTA SHOULD DRIVE OD WITH EI LEVEL PULLUP, STUFF R5612, NOSTUFF R5608, STUFF R5646

R5612 1K 2 RES 1 SRCOM_SRESET 56

5% 1/16W MF-LF 402

42 41 7 =PPV_EI_NB

NOTE, NB UNUSED INTS DO NOT REQUIRE PULLUPS, ONLY SHASTA (SINCE ITS OUTPUTS ARE TEMPORARILY INPUTS ON BOOTUP).

INT PULLUP IS SO INT PIN IS NOT FLOATING TO PROCESSOR BUT WEAK TO ALLOW KODIAK TO DRIVE PUSH-PULL STRONGLY

R5604 10K 2 RES 1 CPU_A0_INT_R_L 24 56

5% 1/16W MF-LF 402

SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.

R5640 IS OPTIONAL

55 52 50 49 48 43 =PPVCORE_CPU

R5640 100 2 RES 1 SRCOM_VCORE_R 10

MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.20 MM

5% 1/16W MF-LF 402

SRCOM_0V8_REF 11

R5642 10K 2 RES 1 NOSTUFF

MIN_LINE_WIDTH=0.20 MM MIN_NECK_WIDTH=0.20 MM

5% 1/16W MF-LF 402

GND

PP2V5_ALL PVDD

R5641 22.1K 2 RES 1 NOSTUFF

5% 1/16W MF-LF 402

56 48 47 30 29 7 =PPV_EI_CPU

R5646 0 2 RES 1 5% 1/16W MF-LF 402

VCC CAN BE 0.8V TO 2.7V 3.3V INPUT TOLERANT

DAMPEN OUTPUT

R5644 100 2 RES 1 CPU_SRESET_L 43

5% 1/16W MF-LF 402

CRITICAL

PULL-UP PROVIDED

NOSTUFF 24 56 SB_CPU_A0_SRESET_L

R5643 4.7K 2 RES 1 NOSTUFF

5% 1/16W MF-LF 402

C5640 0.1UF 20% 10V CERM 2 CAP NOSTUFF 402

U5640 SN74AUC2G125 VSSOP 8 SRCOM_SRESET

SOI-LF COMPARATOR_LM339

U400 13 12 NOSTUFF

R5645 470K 2 RES 1 5% 1/16W MF-LF 402

SRCOM_SRESET_EN_L

TURN-ON VCORE > 0.80 V

TURN-OFF VCORE < 0.77 V

GND

CPU ALIASES & MISC

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

KODIAK

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A30 A34 AA26 AA29 AA32 AA35 AB24 AC27 AC30 AC33 AC36 AD25 AE23 AE26 AE29 AE32 AE35 AF25 AG23 AG27 AG30 AG33 AG36 AJ25 AJ29 AJ32 AJ35 AK23 AK27 AL31 AL33 AL36 AM25 AM29 AN23 AN27 AN31 AN35 AR25 AR29 AR33 AR35 AT23 AT27 AT31 B28 B32 C36 D30 D33 E28 E32 E35 G30 G33 G36 H28 H29 J29 J32 J35 K26 L27 L30 L33 L36 M25 N22 N26 N29 N32 N35 P24 R27 R30 R33 R36 T25 U22 U26 U29 U32 U35 V24 W27 W30 W33 W36 Y25

GND

A28 A32 AA27 AA30 AA33 AA36 AB25 AC26 AC29 AC32 AC35 AD24 AE22 AE27 AE30 AE33 AE36 AF23 AF26 AG25 AG29 AG32 AG35 AJ23 AJ27 AJ30 AJ33 AJ36 AK25 AK29 AL32 AL35 AM23 AM27 AM31 AN25 AN29 AN33 AN36 AP34 AR23 AR27 AR31 AT25 AT29 AT33 B30 B34 C35 D28 D32 E30 E33 E36 G28 G32 G35 J28 J30 J33 J36 L26 L29 L32 L35 M24 N23 N27 N30 N33 N36 P25 R26 R29 R32 R35 T24 U23 U27 U30 U33 U36 V25 W26 W29 W32 W35 Y24

=PP1V8_PWRON_NBMEM 7 20 39 58 59

59 58 39 20 7 =PP1V8_PWRON_NBMEM

C5836 C5835 C5834 C5832 C5831 C5830 C5829 C5822 C5811 C5800
C5864 C5859 C5857 C5842 C5840 C5837 C5828 C5801 C5855 C5833
C5863 C5860 C5858 C5843 C5841 C5838 C5827 C5802 C5866 C5844
C5865 C5862 C5861 C5846 C5845 C5839 C5826 C5803 C5887 C5877
C5874 C5869 C5867 C5852 C5850 C5847 C5825 C5810 C5806 C5804
C5873 C5870 C5868 C5853 C5851 C5848 C5824 C5812 C5807 C5805
C5875 C5872 C5871 C5856 C5854 C5849 C5823 C5813 C5809 C5808
C5886 C5885 C5883 C5881 C5879 C5876 C5821 C5818 C5816 C5814
C5884 C5882 C5880 C5878 C5820 C5819 C5817 C5815

CAP 1UF 10% 6.3V CERM 402

GND

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

051-6863 H

58 154

APPLE_DSIZEPAGE

LAST_MODIFIED=Fri Apr 28 20:23:12 2006

DRAWING

KODIAK

U1900

BGA

KODIAK-ASIC-040812

RAM_DQ<64>	P32	RAM_DQ<0>	AP31
RAM_DQ<65>	T36	RAM_DQ<1>	AP32
RAM_DQ<66>	U31	RAM_DQ<2>	AN32
RAM_DQ<67>	P31	RAM_DQ<3>	AM30
RAM_DQ<68>	T30	RAM_DQ<4>	AN30
RAM_DQ<69>	T29	RAM_DQ<5>	AP30
RAM_DQ<70>	T28	RAM_DQ<6>	AR30
RAM_DQ<71>	W28	RAM_DQ<7>	AM32
RAM_DQ<72>	P34	RAM_DQ<8>	AM36
RAM_DQ<73>	T34	RAM_DQ<9>	AK31
RAM_DQ<74>	P33	RAM_DQ<10>	AL34
RAM_DQ<75>	T35	RAM_DQ<11>	AT34
RAM_DQ<76>	P35	RAM_DQ<12>	AR34
RAM_DQ<77>	P36	RAM_DQ<13>	AN34
RAM_DQ<78>	R31	RAM_DQ<14>	AM33
RAM_DQ<79>	T31	RAM_DQ<15>	AM34
RAM_DQ<80>	K36	RAM_DQ<16>	AH31
RAM_DQ<81>	M34	RAM_DQ<17>	AK34
RAM_DQ<82>	K35	RAM_DQ<18>	AH32
RAM_DQ<83>	N31	RAM_DQ<19>	AK33
RAM_DQ<84>	L31	RAM_DQ<20>	AH30
RAM_DQ<85>	L34	RAM_DQ<21>	AH29
RAM_DQ<86>	M31	RAM_DQ<22>	AJ34
RAM_DQ<87>	M33	RAM_DQ<23>	AK32
RAM_DQ<88>	M27	RAM_DQ<24>	AE31
RAM_DQ<89>	R28	RAM_DQ<25>	AG34
RAM_DQ<90>	U28	RAM_DQ<26>	AE34
RAM_DQ<91>	T27	RAM_DQ<27>	AH36
RAM_DQ<92>	N28	RAM_DQ<28>	AF36
RAM_DQ<93>	P29	RAM_DQ<29>	AF35
RAM_DQ<94>	P30	RAM_DQ<30>	AF34
RAM_DQ<95>	N34	RAM_DQ<31>	AG31
RAM_DQ<96>	G34	RAM_DQ<32>	AF29
RAM_DQ<97>	J31	RAM_DQ<33>	AF30
RAM_DQ<98>	G31	RAM_DQ<34>	AD31
RAM_DQ<99>	J34	RAM_DQ<35>	AG28
RAM_DQ<100>	H30	RAM_DQ<36>	AD34
RAM_DQ<101>	H36	RAM_DQ<37>	AD35
RAM_DQ<102>	H31	RAM_DQ<38>	AH35
RAM_DQ<103>	H34	RAM_DQ<39>	AH34
RAM_DQ<104>	B35	RAM_DQ<40>	AB36
RAM_DQ<105>	F31	RAM_DQ<41>	AC34
RAM_DQ<106>	C33	RAM_DQ<42>	AA31
RAM_DQ<107>	F34	RAM_DQ<43>	AD36
RAM_DQ<108>	C34	RAM_DQ<44>	AB35
RAM_DQ<109>	D34	RAM_DQ<45>	AB34
RAM_DQ<110>	D35	RAM_DQ<46>	AB33
RAM_DQ<111>	E34	RAM_DQ<47>	AC31
RAM_DQ<112>	D31	RAM_DQ<48>	V32
RAM_DQ<113>	E31	RAM_DQ<49>	Y32
RAM_DQ<114>	C31	RAM_DQ<50>	V31
RAM_DQ<115>	F30	RAM_DQ<51>	Y33
RAM_DQ<116>	A33	RAM_DQ<52>	V33
RAM_DQ<117>	B33	RAM_DQ<53>	V34
RAM_DQ<118>	C32	RAM_DQ<54>	V35
RAM_DQ<119>	C30	RAM_DQ<55>	Y29
RAM_DQ<120>	D27	RAM_DQ<56>	V30
RAM_DQ<121>	F29	RAM_DQ<57>	Y34
RAM_DQ<122>	E29	RAM_DQ<58>	Y35
RAM_DQ<123>	D29	RAM_DQ<59>	U34
RAM_DQ<124>	C29	RAM_DQ<60>	AB28
RAM_DQ<125>	B29	RAM_DQ<61>	AB27
RAM_DQ<126>	A29	RAM_DQ<62>	W34
RAM_DQ<127>	C28	RAM_DQ<63>	AA28
	F36		AB29
	K31		AC28
	K34		AF27
	F35		AE28
	M30		AD29
	L28		AD30
	K29		Y36
	K30		AA34

DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

RAM_CLKA_P	AR28		
RAM_CLKA_N	AT28		
	AL26	OUT	
	AK26	OUT	
RAM_CAS_L	AM24		
RAM_RAS_L	AL24		
RAM_WE_L	AP23		
RAM_BA<0>	AL22		
RAM_BA<1>	AP28		
RAM_BA<2>	AN28		
RAM_A<0>	AN26		
RAM_A<1>	AP26		
RAM_A<2>	AR26		
RAM_A<3>	AT26		
RAM_A<4>	AM26		
RAM_A<5>	AL25		
RAM_A<6>	AP25		
RAM_A<7>	AH28		
RAM_A<8>	AL30		
RAM_A<9>	AR22		
RAM_A<10>	AJ28		
RAM_A<11>	AH27		
RAM_A<12>	AH26		
RAM_A<13>	AH25		
RAM_A<14>	AJ26		
RAM_A<15>	AK24		
	AF22		
RAM_DQS_P<0>	AR32		
RAM_DQS_N<0>	AT32		
RAM_DQS_P<1>	AP35		
RAM_DQS_N<1>	AP36		
RAM_DQS_P<2>	AK35		
RAM_DQS_N<2>	AK36		
RAM_DQS_P<3>	AF33		
RAM_DQS_N<3>	AF32		
RAM_DQS_P<4>	AD33		
RAM_DQS_N<4>	AD32		
RAM_DQS_P<5>	AB30		
RAM_DQS_N<5>	AB31		
RAM_DQS_P<6>	Y31		
RAM_DQS_N<6>	Y30		
RAM_DQS_P<7>	Y27		
RAM_DQS_N<7>	Y28		
RAM_DQS_P<8>	V28		
RAM_DQS_N<8>	V27		
RAM_DQS_P<9>	T33		
RAM_DQS_N<9>	T32		
RAM_DQS_P<10>	M36		
RAM_DQS_N<10>	M35		
RAM_DQS_P<11>	P27		
RAM_DQS_N<11>	P28		
RAM_DQS_P<12>	H33		
RAM_DQS_N<12>	H32		
RAM_DQS_P<13>	F33		
RAM_DQS_N<13>	F32		
RAM_DQS_P<14>	A31		
RAM_DQS_N<14>	B31		
RAM_DQS_P<15>	B27		
RAM_DQS_N<15>	A27		
	AD27		
	AD28		
	K32		
	K33		

KODIAK

U1900

BGA

KODIAK-ASIC-040812

RAM_CS_L<0>	AL27		
	AP33	OUT	
	AJ31	OUT	
	AF31	OUT	
RAM_CS_L<4>	AH33		
RAM_CS_L<5>	AB32		
	V36	OUT	
	W31	OUT	
RAM_CS_L<8>	V29		
RAM_CS_L<9>	R34		
	M32	OUT	
	M28	OUT	
	H35	OUT	
	D36	OUT	
	G29	OUT	
	E27	OUT	
RAM_CKE<0>	AJ24		
RAM_CKE<1>	AH24		
	AL21	OUT	
	AP21	OUT	
RAM_CKE<4>	AT22		
RAM_CKE<5>	AP22		
	AN22	OUT	
	AM22	OUT	
	AP27	OUT	
	AM28	OUT	
	AL28	OUT	
	AK28	OUT	
	AK30	OUT	
	AT30	OUT	
	AL29	OUT	
	AP29	OUT	
RAM_ODT<0>	AL23		
	AT24	OUT	
RAM_ODT<2>	AR24		
	AN24	OUT	
RAM_ODT<4>	AP24		
	AK22	OUT	
	AF28	OUT	
	M29	OUT	

Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM_RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	8	0	4	J6700 rank 1	64:127
B3	9	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	2	5	*unused*	64:127
D7	11	3	-	*unused*	64:127
E8	4	4	2	*unused*	0:63
E9	5	5	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM_RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127

PLACE NEAR KODIAK

NOSTUFF R5928 RES 49.9
NOSTUFF R5929 RES 49.9
NOSTUFF R5912 RES 49.9

NB_DDR_REFCLK_P	AF24	DIFFERENTIAL PAIR=RAM_NB_DDR_REFCLK_DP	NET_PHYSICAL_TYPE=RAM_NB_DDR_80 NET_SPACING_TYPE=RAM_NB_DDR_80
NB_DDR_REFCLK_N	AG24	DIFFERENTIAL PAIR=RAM_NB_DDR_REFCLK_DP	NET_PHYSICAL_TYPE=RAM_NB_DDR_80 NET_SPACING_TYPE=RAM_NB_DDR_80
NB_CHP_FLT_N	AH22		
NB_DDR_STOP_OUT	AJ22		
NB_PLL_OUT_TRG	AG22		
	AG26		
	AD26		
	AB26		
	Y26		
	V26		
	T26		
	P26		
	M26		
	F28		

R5913 1K RES → GND

=PP1V8_PWRON_NBMEM

R5910 56.2 RES 1/16W MF-LF 402 — CHECK VREF CONNECTION

DDR_VREF1_9 (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.25MM)

R5911 56.2 RES 1/16W MF-LF 402

C5904 CAP 1UF 10% 6.3V CERM 402

C5905 C5906 C5907 C5908 C5909 C5910 C5911 C5912 C5913 CAP 1UF 10% 6.3V CERM 402 → GND

PLACE CLOSE TO KODIAK PIN
WITHIN 20MIL FROM VIA FOR EACH VREF

ARROW =PPV_PWRON_NB_REFCLK → R5914 4.7 5% 1/16W MF-LF 402 → PPV_PWRON_NB_REFCLK_PU_R (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.2MM) → R5927 2.2 5% 1/16W MF-LF 402 → AH23

C5900 CAP 1UF 10% 6.3V CERM 402 → GND

C5901 CAP 0.22UF 20% 6.3V X5R 402 → GND

U1900_RFCK_AVDD (MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.5MM) → AH21

Q63 APPLICATION IS PP1V6

CHECK CAP SIZE (0603 OR 0402)

Kodiak Memory Dq/Ctl

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

KODIAK MEMORY INTERFACE

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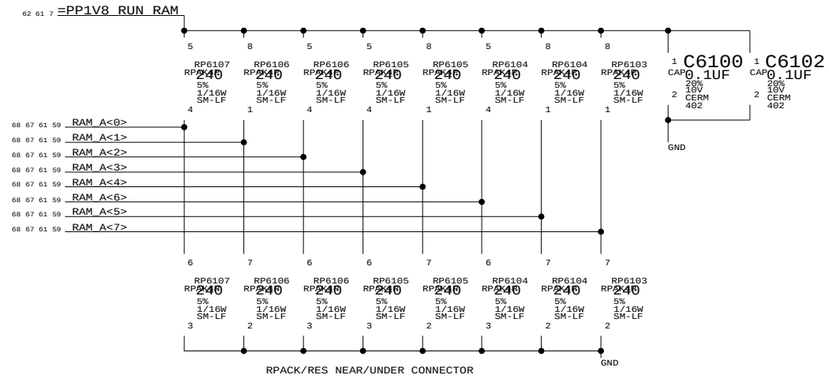
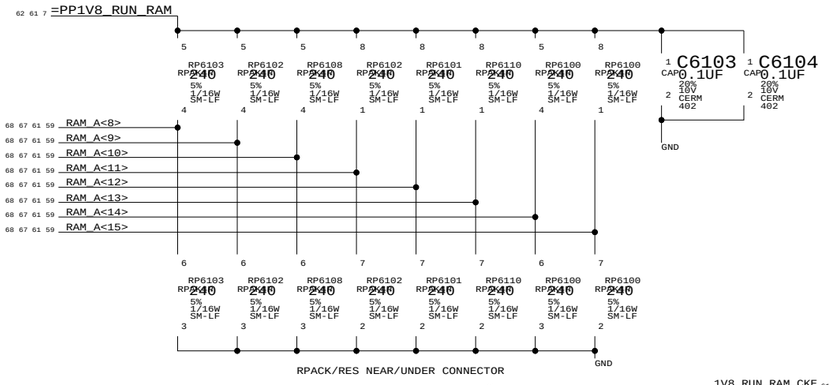
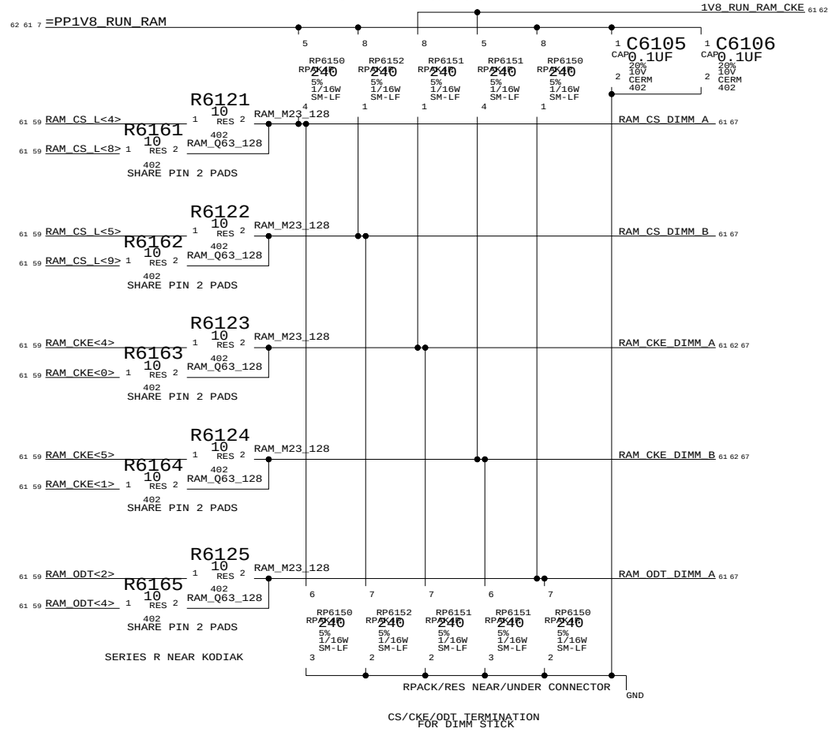
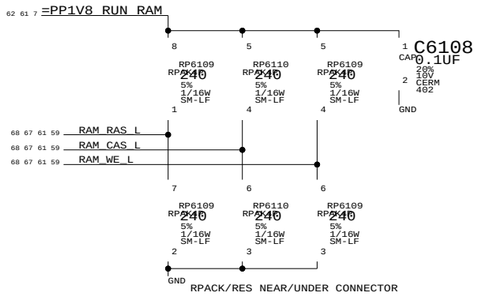
APPLE_DSIZEPAGE

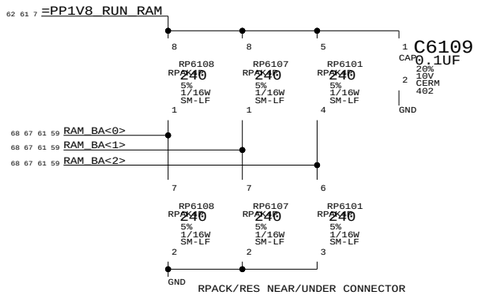
ALL R PACKS ARE 1/16W 5%

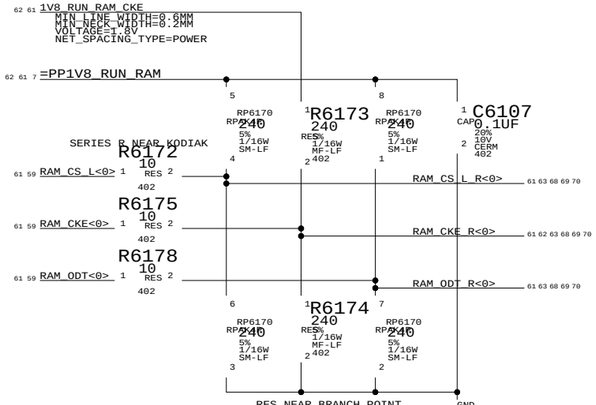












61 59 RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		4243
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61 59 RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4242
61 59 RAM_CS_L<8>		RAM_CSCKEODT	RAM_CSCKEODT		4245
61 59 RAM_CS_L<9>		RAM_CSCKEODT	RAM_CSCKEODT		4244
70 69 68 63 61 RAM_CS_L_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		4238
67 61 RAM_CS_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		4241
67 61 RAM_CS_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		4575
61 59 RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		4234
61 59 RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4236
61 59 RAM_CKE<4>		RAM_CSCKEODT	RAM_CSCKEODT		4235
61 59 RAM_CKE<5>		RAM_CSCKEODT	RAM_CSCKEODT		4237
70 69 68 63 62 61 RAM_CKE_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		4230
67 62 61 RAM_CKE_DIMM_B		RAM_CSCKEODT	RAM_CSCKEODT		4692
67 62 61 RAM_CKE_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		4232
61 59 RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT	RAM_CSCKEODT		4574
61 59 RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT	RAM_CSCKEODT		4576
61 59 RAM_ODT<4>		RAM_CSCKEODT	RAM_CSCKEODT		4577
70 69 68 63 61 RAM_ODT_R<0>		RAM_CSCKEODT	RAM_CSCKEODT		4693
67 61 RAM_ODT_DIMM_A		RAM_CSCKEODT	RAM_CSCKEODT		4594

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
62 59 RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	206
62 59 RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP	207
67 62 RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	210
67 62 RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP	211
67 62 RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	212
67 62 RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP	213
67 62 RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	214
67 62 RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP	215
69 62 RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	216
69 62 RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP	217
69 62 RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	218
69 62 RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP	219
70 62 RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	220
70 62 RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP	221
70 62 RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	222
70 62 RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP	223
62 RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	224
62 RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP	225
62 RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	226
62 RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP	227
68 59 RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD		248
68 59 RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	246
68 59 RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP	1478
68 59 RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD		252
68 59 RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	251
68 59 RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP	1471
68 59 RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD		254
68 59 RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	253
68 59 RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP	1472
68 59 RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD		256
68 59 RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	255
68 59 RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP	1473
68 59 RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD		258
68 59 RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	257
68 59 RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP	1474
68 59 RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD		260
68 59 RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	259
68 59 RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP	1475
68 59 RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD		262
68 59 RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	261
68 59 RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP	1476
68 59 RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD		264
68 59 RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	263
68 59 RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP	1477
67 59 RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD		267
67 59 RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	266
67 59 RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP	1478
67 59 RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD		268
67 59 RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	269
67 59 RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP	1479
67 59 RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD		265
67 59 RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	270
67 59 RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP	1480
67 59 RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD		271
67 59 RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	272
67 59 RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP	1481
67 59 RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD		274
67 59 RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	273
67 59 RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP	1482
67 59 RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD		277
67 59 RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	276
67 59 RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP	1483
67 59 RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD		278
67 59 RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	279
67 59 RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP	1484
67 59 RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD		275
67 59 RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	280
67 59 RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP	1485
70 69 68 6 RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD		1294
70 69 68 RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS		1305
70 69 68 RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS		1486
68 67 61 59 RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1572
68 67 61 59 RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1295
68 67 61 59 RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1296
68 67 61 59 RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD		1573
68 67 61 59 RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1297
68 67 61 59 RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1298
68 67 61 59 RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD		1299
70 69 68 63 RAM_A_R<15..0>		RAM_CAD	RAM_CAD		1306
70 69 68 63 RAM_BA_R<2..0>		RAM_CAD	RAM_CAD		1304
70 69 68 63 RAM_RAS_L_R		RAM_CAD	RAM_CAD		1303
70 69 68 63 RAM_CAS_L_R		RAM_CAD	RAM_CAD		1302
70 69 68 63 RAM_WE_L_R		RAM_CAD	RAM_CAD		1301

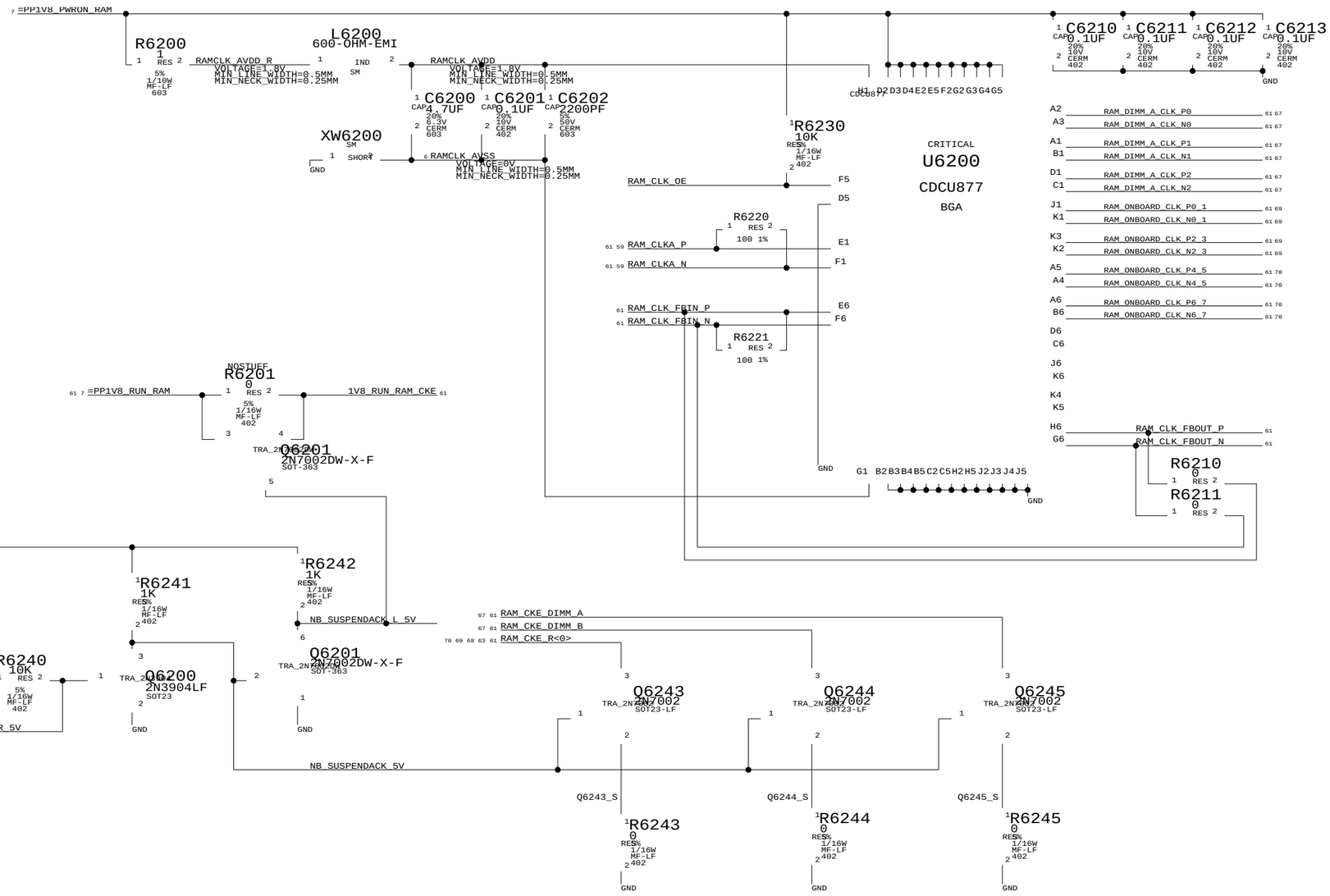
RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE



Main Memory Clock Buffer

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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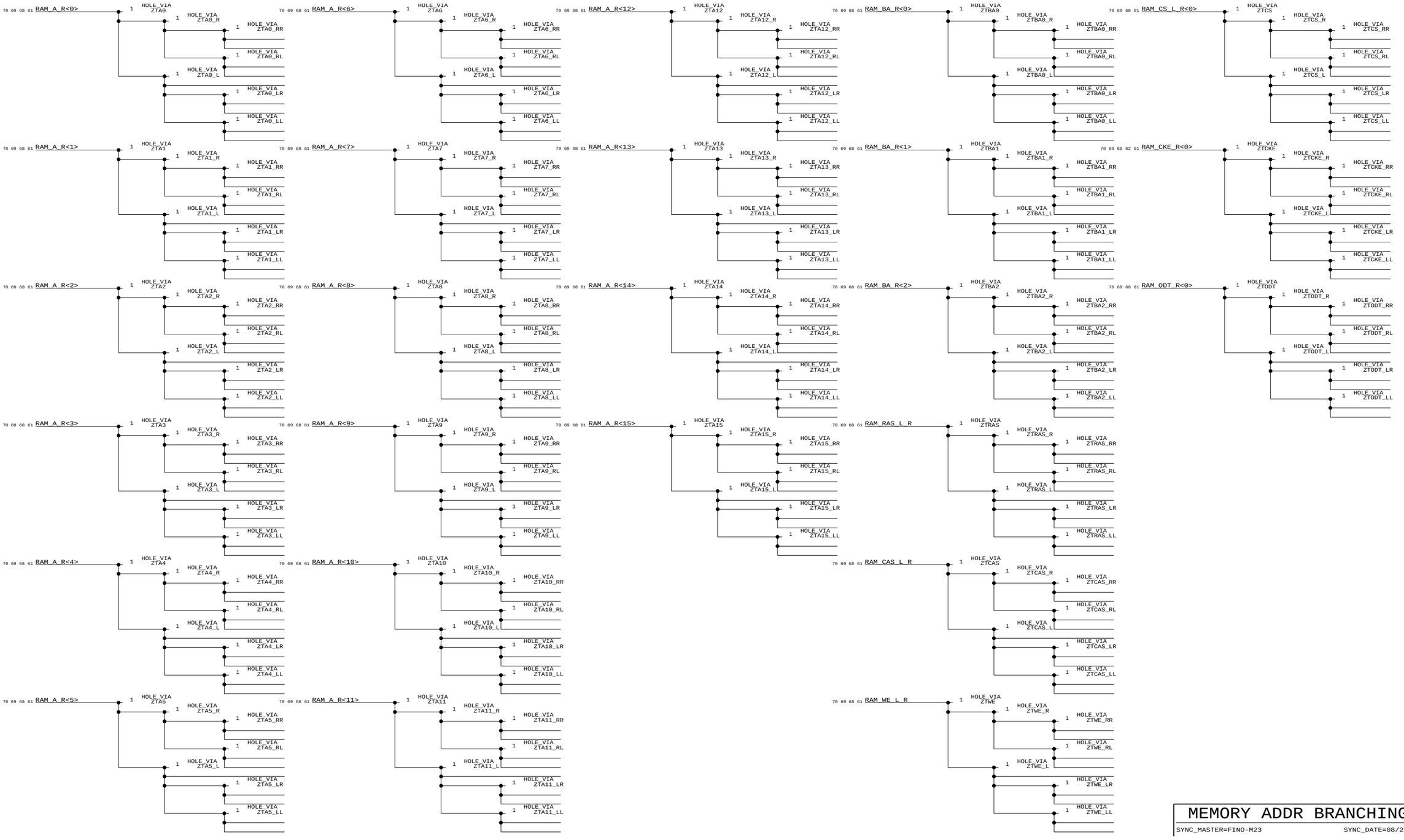
APPLE_DSIZEPAGE



MEMORY ADDR BRANCHING

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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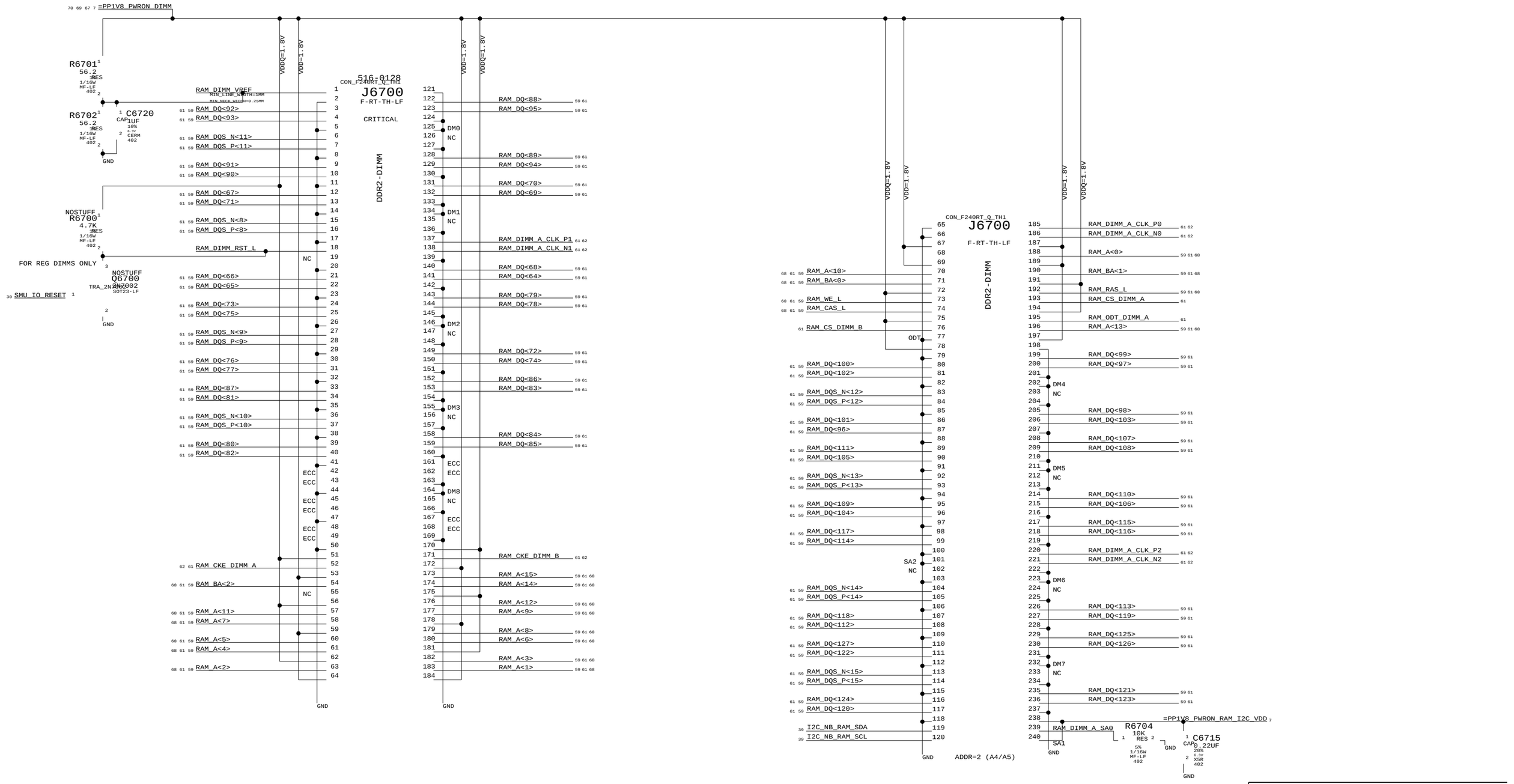
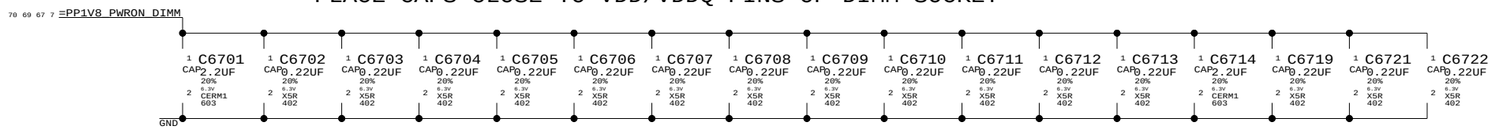


Memory Dimm A

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



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APPLE_DSIZEPAGE

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

RAM_DQ<0>	22	4	RPAR4P	RP6800	RAM_DQ_R<0>	6 61 69
RAM_DQ<1>	22	3	RPAR4P	RP6800	RAM_DQ_R<1>	6 61 69
RAM_DQ<2>	22	1	RPAR4P	RP6801	RAM_DQ_R<2>	6 61 69
RAM_DQ<3>	22	3	RPAR4P	RP6801	RAM_DQ_R<3>	6 61 69
RAM_DQ<4>	22	4	RPAR4P	RP6801	RAM_DQ_R<4>	61 69
RAM_DQ<5>	22	2	RPAR4P	RP6800	RAM_DQ_R<5>	6 61 69
RAM_DQ<6>	22	2	RPAR4P	RP6801	RAM_DQ_R<6>	6 61 69
RAM_DQ<7>	22	1	RPAR4P	RP6800	RAM_DQ_R<7>	6 61 69
RAM_DQ<8>	22	3	RPAR4P	RP6802	RAM_DQ_R<8>	6 61 69
RAM_DQ<9>	22	4	RPAR4P	RP6803	RAM_DQ_R<9>	6 61 69
RAM_DQ<10>	22	1	RPAR4P	RP6803	RAM_DQ_R<10>	61 69
RAM_DQ<11>	22	4	RPAR4P	RP6802	RAM_DQ_R<11>	6 61 69
RAM_DQ<12>	22	3	RPAR4P	RP6803	RAM_DQ_R<12>	6 61 69
RAM_DQ<13>	22	2	RPAR4P	RP6802	RAM_DQ_R<13>	6 61 69
RAM_DQ<14>	22	2	RPAR4P	RP6803	RAM_DQ_R<14>	6 61 69
RAM_DQ<15>	22	1	RPAR4P	RP6802	RAM_DQ_R<15>	61 69
RAM_DQ<16>	22	3	RPAR4P	RP6805	RAM_DQ_R<16>	6 61 69
RAM_DQ<17>	22	4	RPAR4P	RP6805	RAM_DQ_R<17>	6 61 69
RAM_DQ<18>	22	1	RPAR4P	RP6804	RAM_DQ_R<18>	61 69
RAM_DQ<19>	22	2	RPAR4P	RP6805	RAM_DQ_R<19>	6 61 69
RAM_DQ<20>	22	2	RPAR4P	RP6804	RAM_DQ_R<20>	6 61 69
RAM_DQ<21>	22	4	RPAR4P	RP6804	RAM_DQ_R<21>	6 61 69
RAM_DQ<22>	22	3	RPAR4P	RP6804	RAM_DQ_R<22>	6 61 69
RAM_DQ<23>	22	1	RPAR4P	RP6805	RAM_DQ_R<23>	61 69
RAM_DQ<24>	22	4	RPAR4P	RP6807	RAM_DQ_R<24>	6 61 69
RAM_DQ<25>	22	2	RPAR4P	RP6806	RAM_DQ_R<25>	6 61 69
RAM_DQ<26>	22	4	RPAR4P	RP6806	RAM_DQ_R<26>	61 69
RAM_DQ<27>	22	1	RPAR4P	RP6807	RAM_DQ_R<27>	61 69
RAM_DQ<28>	22	3	RPAR4P	RP6807	RAM_DQ_R<28>	6 61 69
RAM_DQ<29>	22	3	RPAR4P	RP6806	RAM_DQ_R<29>	6 61 69
RAM_DQ<30>	22	2	RPAR4P	RP6807	RAM_DQ_R<30>	6 61 69
RAM_DQ<31>	22	1	RPAR4P	RP6806	RAM_DQ_R<31>	6 61 69
RAM_DQ<32>	22	4	RPAR4P	RP6809	RAM_DQ_R<32>	6 61 70
RAM_DQ<33>	22	2	RPAR4P	RP6808	RAM_DQ_R<33>	6 61 70
RAM_DQ<34>	22	3	RPAR4P	RP6808	RAM_DQ_R<34>	6 61 70
RAM_DQ<35>	22	1	RPAR4P	RP6809	RAM_DQ_R<35>	61 70
RAM_DQ<36>	22	2	RPAR4P	RP6809	RAM_DQ_R<36>	6 61 70
RAM_DQ<37>	22	1	RPAR4P	RP6808	RAM_DQ_R<37>	6 61 70
RAM_DQ<38>	22	3	RPAR4P	RP6809	RAM_DQ_R<38>	6 61 70
RAM_DQ<39>	22	4	RPAR4P	RP6808	RAM_DQ_R<39>	61 70
RAM_DQ<40>	22	4	RPAR4P	RP6810	RAM_DQ_R<40>	6 61 70
RAM_DQ<41>	22	3	RPAR4P	RP6811	RAM_DQ_R<41>	6 61 70
RAM_DQ<42>	22	1	RPAR4P	RP6811	RAM_DQ_R<42>	61 70
RAM_DQ<43>	22	2	RPAR4P	RP6810	RAM_DQ_R<43>	6 61 70
RAM_DQ<44>	22	4	RPAR4P	RP6811	RAM_DQ_R<44>	6 61 70
RAM_DQ<45>	22	3	RPAR4P	RP6810	RAM_DQ_R<45>	6 61 70
RAM_DQ<46>	22	2	RPAR4P	RP6811	RAM_DQ_R<46>	6 61 70
RAM_DQ<47>	22	1	RPAR4P	RP6810	RAM_DQ_R<47>	61 70
RAM_DQ<48>	22	3	RPAR4P	RP6812	RAM_DQ_R<48>	6 61 70
RAM_DQ<49>	22	4	RPAR4P	RP6812	RAM_DQ_R<49>	6 61 70
RAM_DQ<50>	22	2	RPAR4P	RP6813	RAM_DQ_R<50>	6 61 70
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RAM_DQ<52>	22	3	RPAR4P	RP6813	RAM_DQ_R<52>	6 61 70
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RAM_DQ<56>	22	3	RPAR4P	RP6814	RAM_DQ_R<56>	6 61 70
RAM_DQ<57>	22	4	RPAR4P	RP6815	RAM_DQ_R<57>	6 61 70
RAM_DQ<58>	22	2	RPAR4P	RP6815	RAM_DQ_R<58>	6 61 70
RAM_DQ<59>	22	3	RPAR4P	RP6815	RAM_DQ_R<59>	6 61 70
RAM_DQ<60>	22	2	RPAR4P	RP6814	RAM_DQ_R<60>	6 61 70
RAM_DQ<61>	22	1	RPAR4P	RP6814	RAM_DQ_R<61>	61 70
RAM_DQ<62>	22	1	RPAR4P	RP6815	RAM_DQ_R<62>	61 70
RAM_DQ<63>	22	4	RPAR4P	RP6814	RAM_DQ_R<63>	6 61 70

RAM_DQS_P<0>	22	1	RES 2	R6800	DIFFERENTIAL_DATA_DQS_P_R<0>	6 61 69
RAM_DQS_N<0>	22	1	RES 2	R6810	DIFFERENTIAL_DATA_DQS_N_R<0>	6 61 69
RAM_DQS_P<1>	22	1	RES 2	R6801	DIFFERENTIAL_DATA_DQS_P_R<1>	6 61 69
RAM_DQS_N<1>	22	1	RES 2	R6811	DIFFERENTIAL_DATA_DQS_N_R<1>	6 61 69
RAM_DQS_P<2>	22	1	RES 2	R6802	DIFFERENTIAL_DATA_DQS_P_R<2>	6 61 69
RAM_DQS_N<2>	22	1	RES 2	R6812	DIFFERENTIAL_DATA_DQS_N_R<2>	6 61 69
RAM_DQS_P<3>	22	1	RES 2	R6803	DIFFERENTIAL_DATA_DQS_P_R<3>	6 61 69
RAM_DQS_N<3>	22	1	RES 2	R6813	DIFFERENTIAL_DATA_DQS_N_R<3>	6 61 69
RAM_DQS_P<4>	22	1	RES 2	R6804	DIFFERENTIAL_DATA_DQS_P_R<4>	6 61 70
RAM_DQS_N<4>	22	1	RES 2	R6814	DIFFERENTIAL_DATA_DQS_N_R<4>	6 61 70
RAM_DQS_P<5>	22	1	RES 2	R6805	DIFFERENTIAL_DATA_DQS_P_R<5>	6 61 70
RAM_DQS_N<5>	22	1	RES 2	R6815	DIFFERENTIAL_DATA_DQS_N_R<5>	6 61 70
RAM_DQS_P<6>	22	1	RES 2	R6806	DIFFERENTIAL_DATA_DQS_P_R<6>	6 61 70
RAM_DQS_N<6>	22	1	RES 2	R6816	DIFFERENTIAL_DATA_DQS_N_R<6>	6 61 70
RAM_DQS_P<7>	22	1	RES 2	R6807	DIFFERENTIAL_DATA_DQS_P_R<7>	6 61 70
RAM_DQS_N<7>	22	1	RES 2	R6817	DIFFERENTIAL_DATA_DQS_N_R<7>	6 61 70

RAM_A<0>	5.1	1	RPAR4P	RP6824	RAM_A_R<0>	61 63 69 70	1	HOLE_VIA ZT6800
RAM_A<1>	5.1	1	RPAR4P	RP6823	RAM_A_R<1>	61 63 69 70	1	HOLE_VIA ZT6801
RAM_A<2>	5.1	2	RPAR4P	RP6823	RAM_A_R<2>	61 63 69 70	1	HOLE_VIA ZT6802
RAM_A<3>	5.1	4	RPAR4P	RP6822	RAM_A_R<3>	61 63 69 70	1	HOLE_VIA ZT6803
RAM_A<4>	5.1	3	RPAR4P	RP6822	RAM_A_R<4>	61 63 69 70	1	HOLE_VIA ZT6804
RAM_A<5>	5.1	2	RPAR4P	RP6822	RAM_A_R<5>	61 63 69 70	1	HOLE_VIA ZT6805
RAM_A<6>	5.1	1	RPAR4P	RP6822	RAM_A_R<6>	61 63 69 70	1	HOLE_VIA ZT6806
RAM_A<7>	5.1	3	RPAR4P	RP6821	RAM_A_R<7>	61 63 69 70	1	HOLE_VIA ZT6807
RAM_A<8>	5.1	4	RPAR4P	RP6821	RAM_A_R<8>	61 63 69 70	1	HOLE_VIA ZT6808
RAM_A<9>	5.1	1	RPAR4P	RP6821	RAM_A_R<9>	61 63 69 70	1	HOLE_VIA ZT6809
RAM_A<10>	5.1	3	RPAR4P	RP6824	RAM_A_R<10>	61 63 69 70	1	HOLE_VIA ZT6810
RAM_A<11>	5.1	2	RPAR4P	RP6821	RAM_A_R<11>	61 63 69 70	1	HOLE_VIA ZT6811
RAM_A<12>	5.1	4	RPAR4P	RP6820	RAM_A_R<12>	61 63 69 70	1	HOLE_VIA ZT6812
RAM_A<13>	5.1	4	RPAR4P	RP6825	RAM_A_R<13>	61 63 69 70	1	HOLE_VIA ZT6813
RAM_A<14>	5.1	2	RPAR4P	RP6820	RAM_A_R<14>	61 63 69 70	1	HOLE_VIA ZT6814
RAM_A<15>	5.1	1	RPAR4P	RP6820	RAM_A_R<15>	61 63 69 70	1	HOLE_VIA ZT6815

VIAS FOR ECC STUB

RAM_BA<0>	5.1	4	RPAR4P	RP6824	RAM_BA_R<0>	61 63 69 70	1	HOLE_VIA ZT6820
RAM_BA<1>	5.1	2	RPAR4P	RP6824	RAM_BA_R<1>	61 63 69 70	1	HOLE_VIA ZT6821
RAM_BA<2>	5.1	3	RPAR4P	RP6820	RAM_BA_R<2>	61 63 69 70	1	HOLE_VIA ZT6822
RAM_RAS_L	5.1	1	RPAR4P	RP6825	RAM_RAS_L_R	61 63 69 70	1	HOLE_VIA ZT6825
RAM_CAS_L	5.1	3	RPAR4P	RP6825	RAM_CAS_L_R	61 63 69 70	1	HOLE_VIA ZT6826
RAM_WE_L	5.1	2	RPAR4P	RP6825	RAM_WE_L_R	61 63 69 70	1	HOLE_VIA ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

RAM_CS_L_R<0> 61 63 69 70

C6870 24PF 1 CAP 2 GND 5% 50V C0G 402

C6871 2PF 1 CAP 2 GND +/-0.25PF 50V C0G 402-1

RAM_CKE_R<0> 61 62 63 69 70

C6880 24PF 1 CAP 2 GND 5% 50V C0G 402

C6881 2PF 1 CAP 2 GND +/-0.25PF 50V C0G 402-1

RAM_ODT_R<0> 61 63 69 70

C6890 24PF 1 CAP 2 GND 5% 50V C0G 402

C6891 2PF 1 CAP 2 GND +/-0.25PF 50V C0G 402-1

MLB Mem Series Term

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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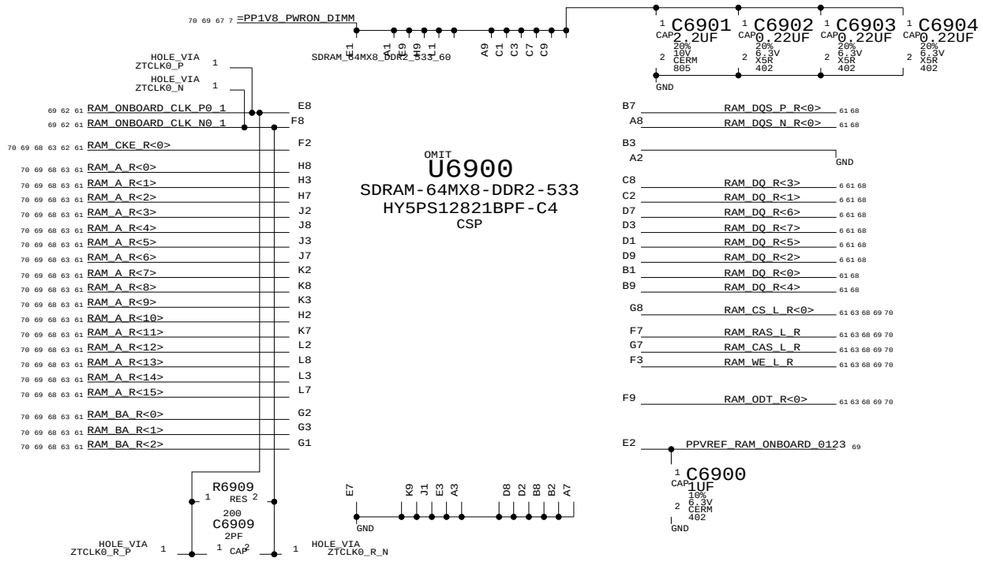
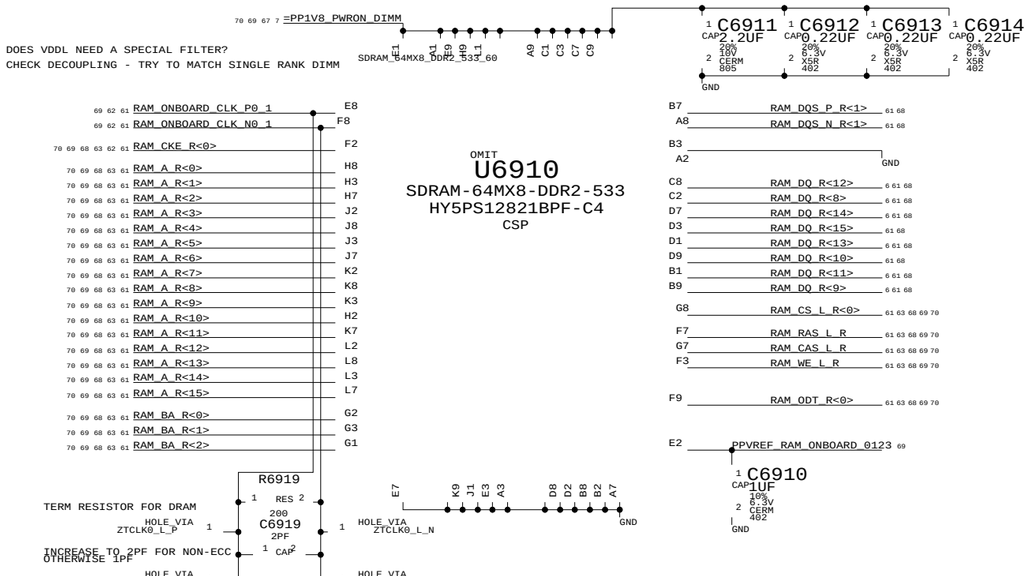
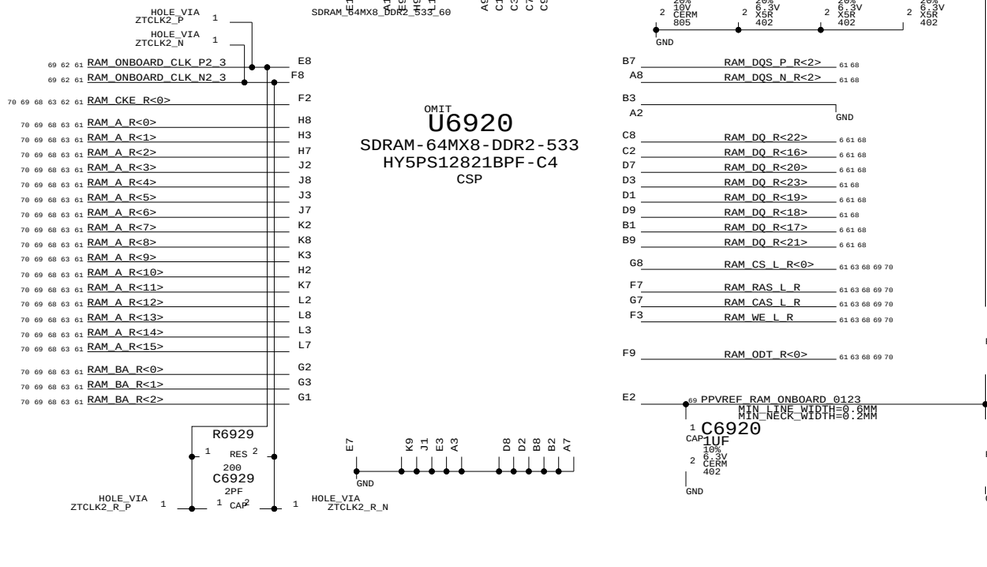
APPLE_DSIZEPAGE







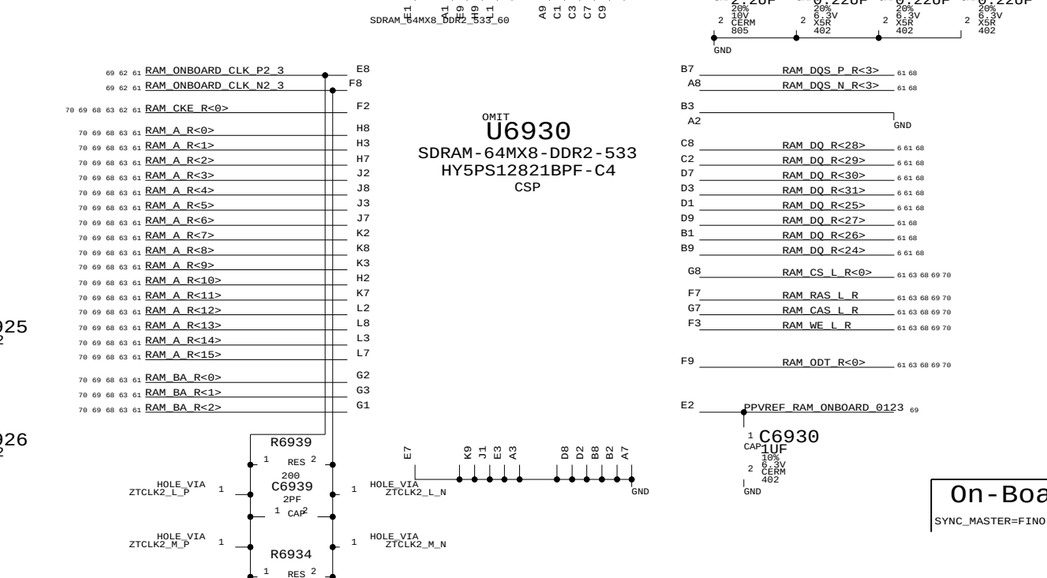


TABLE_6_HEAD

TABLE_6_ITEM

333T0032 4 IC,SDRAM,DDR2,512MBIT,X8 U6900,U6910,U6920,U6930 CRITICAL

TABLE_6_ITEM

333T0032 4 IC,SDRAM,DDR2,512MBIT,X8 U7040,U7050,U7060,U7070 CRITICAL

On-Board DDR SDRAM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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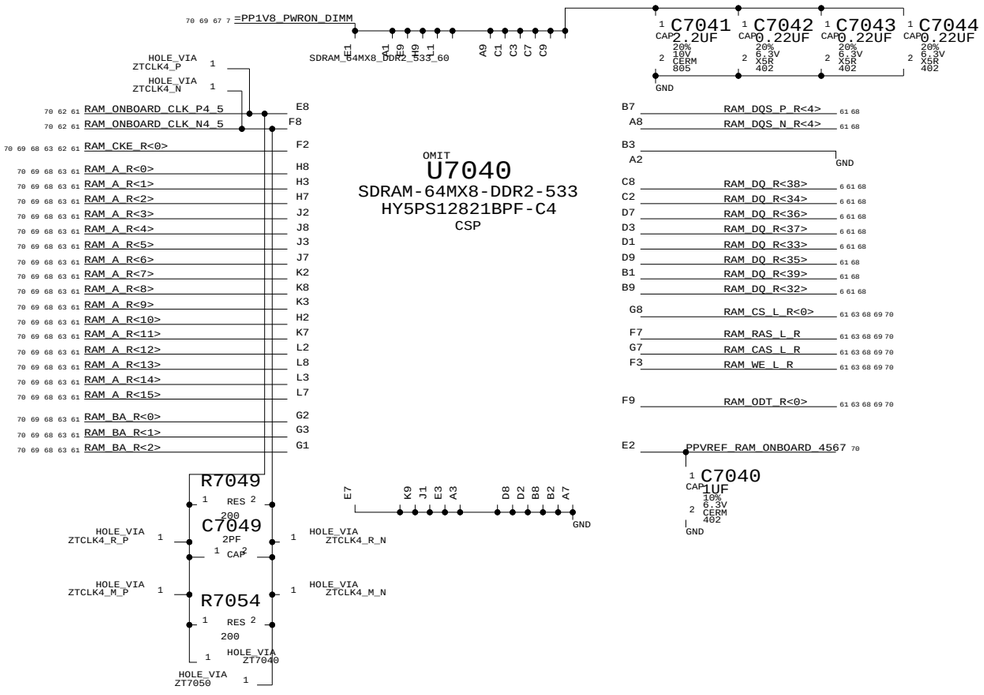

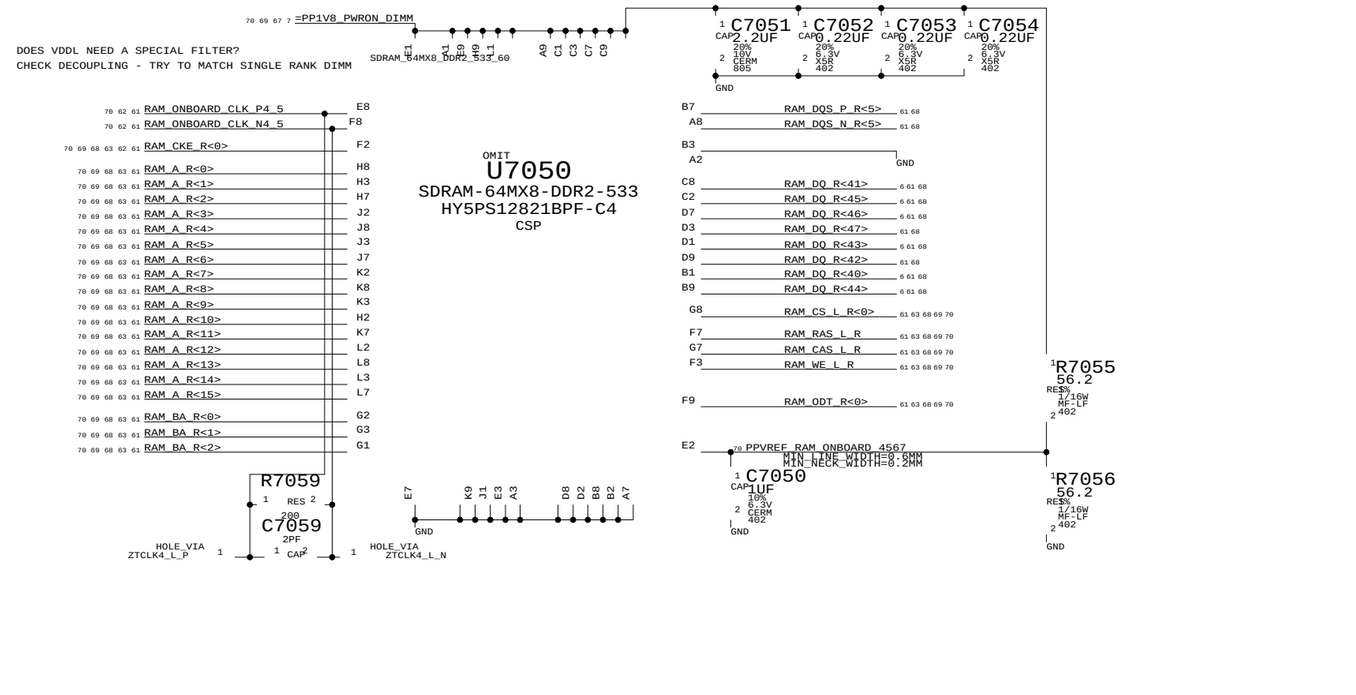

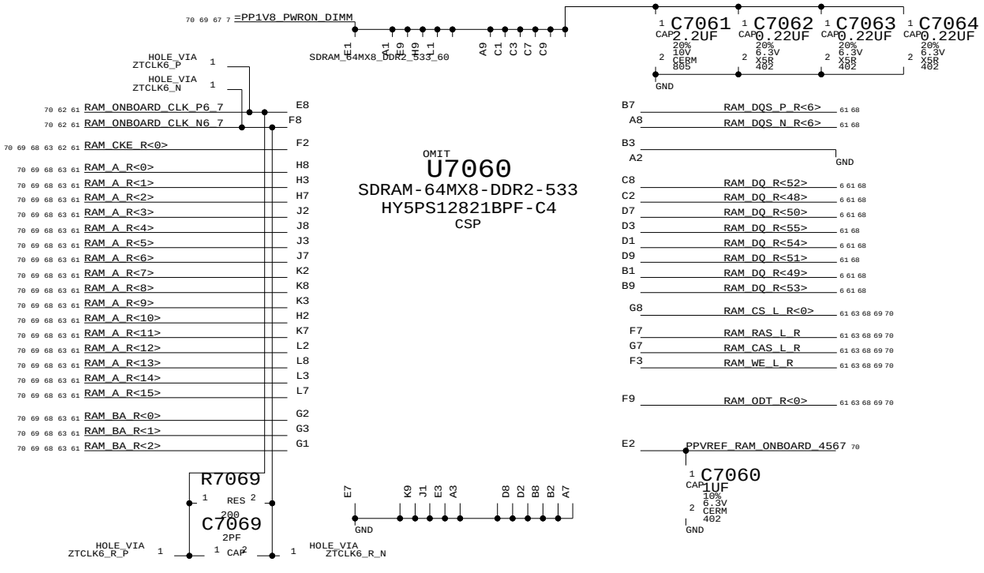

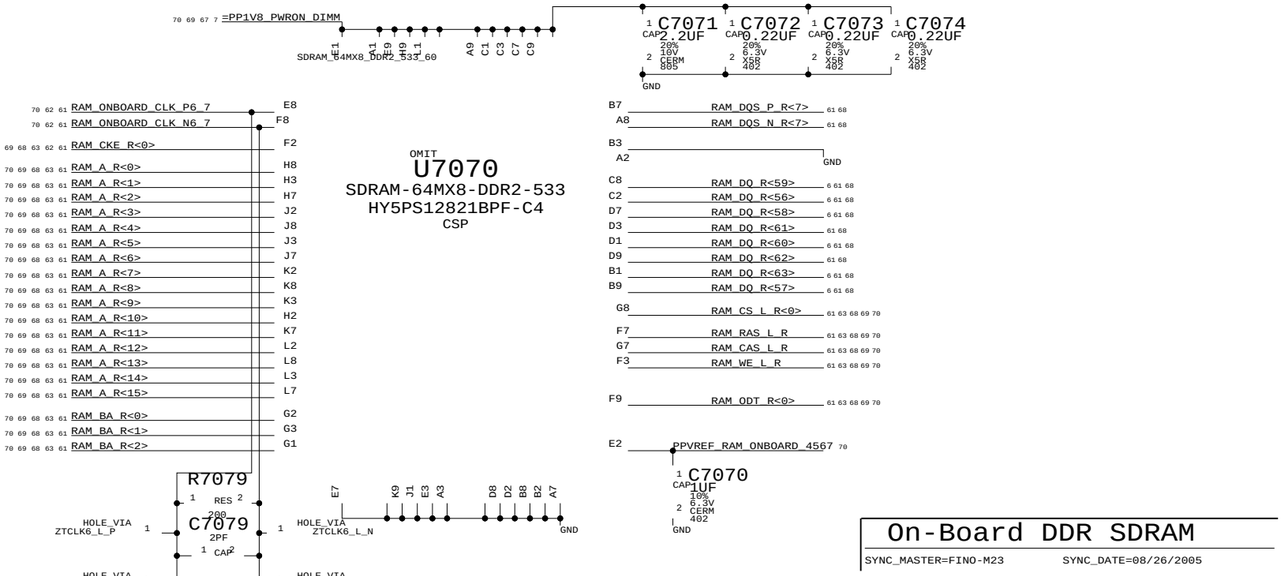

On-Board DDR SDRAM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)

82 7 =PP2V5_PWRON_NB_PCIE
L8200 0.22UH IND 0805-1
PWR_PCIE_A_AVDD_2 82 97
C8200 1 0.01UF CAP 10% 16V CERM 402 2
C8201 1 10UF CAP 10% 6.3V X5R 805 2
C8202 1 1UF CAP 10% 6.3V CERM 402 2
GND
97 82 6 KOD_G10_GND
(THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8201 0.22UH IND 0805-1
PWR_PCIE_A_AVDD_1 82 97
C8203 1 0.01UF CAP 10% 16V CERM 402 2
C8204 1 10UF CAP 10% 6.3V X5R 805 2
C8205 1 1UF CAP 10% 6.3V CERM 402 2
GND
97 82 6 KOD_K07_GND
(THIS PAGE)

82 7 =PP2V5_PWRON_NB_PCIE
L8202 0.22UH IND 0805-1
PWR_PCIE_A_AVDD_0 82 97
C8206 1 0.01UF CAP 10% 16V CERM 402 2
C8207 1 10UF CAP 10% 6.3V X5R 805 2
C8208 1 1UF CAP 10% 6.3V CERM 402 2
GND
97 82 6 KOD_H05_GND
(THIS PAGE)

97 82 PWR_PCIE_A_AVDD_2
97 82 PWR_PCIE_A_AVDD_1
97 82 PWR_PCIE_A_AVDD_0
KODIAK J06 J07 H11 J12 K13 J09

97 PWR_PCIE_A_AVDD_A
97 PWR_PCIE_A_AVDD_B
97 PWR_PCIE_A_AVDD_C
97 PWR_PCIE_A_AVDD
L8203 0.22UH IND 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
C8222 1 CAP 1UF 10% 6.3V CERM 402 2
C8225 1 CAP 1UF 10% 6.3V CERM 402 2
C8223 1 CAP 10UF 10% 6.3V X5R 805 2
C8224 1 CAP 0.01UF 10% 16V CERM 402 2
KOD_L13_GND 6 82 97
(THIS PAGE)
KOD_J13_GND 6 82 97
(THIS PAGE)
L8205 0.22UH IND 0805-1
=PP2V5_PWRON_NB_PCIE 7 82
C8228 1 CAP 1UF 10% 6.3V CERM 402 2
C8229 1 CAP 10UF 10% 6.3V X5R 805 2
C8230 1 CAP 0.01UF 10% 16V CERM 402 2
KOD_H08_GND 6 82 97
(THIS PAGE)

U1900
KODIAK-ASIC-040812
BGA
SEE_TABLE

A04 A08 A12 B06 B10 C03 D01 D04 D08 D12 E06 E10 E14
82 7 =PPVCORE_PWRON_NB_PCIE

F02 F05 G08 G12 H01 H04 H07 H10 H14 K12 L11 L14 M12
=PPVCORE_PWRON_NB_PCIE 7 82

KODIAK PCI-E 100MHZ REFCLK
PP8201 P4MM SM
100+ PROBEPOINT 97 9 CLK_KOD_100M_PF<0> ARROW J11
100- PROBEPOINT 97 9 CLK_KOD_100M_NF<0> ARROW J10
PP8200 P4MM SM
(100MHZ)

97 26 CLK_KOD_100M_P<0> R8202 20.5 1% 1/16W MF-LF 402 RES 97 9 100M_P<0>
C8245 0.01UF CAP 10% 16V CERM 402
NOSTUFF C8244 0.01UF CAP GND 10% 16V CERM 402 100M_G
R8203 29.4 1% 1/16W MF-LF 402 RES
R8204 29.4 1% 1/16W MF-LF 402 RES
97 26 CLK_KOD_100M_N<0> R8205 20.5 1% 1/16W MF-LF 402 RES 97 9 100M_N<0>
C8246 0.01UF CAP 10% 16V CERM 402

97 84 9 PCIE_SLOTA_TO_NB_N<0> ARROW G05
97 84 9 PCIE_SLOTA_TO_NB_P<0> ARROW G04
97 84 9 PCIE_SLOTA_TO_NB_N<1> ARROW G01
97 84 9 PCIE_SLOTA_TO_NB_P<1> ARROW G02
97 84 9 PCIE_SLOTA_TO_NB_N<2> ARROW C04
97 84 9 PCIE_SLOTA_TO_NB_P<2> ARROW C05
97 84 9 PCIE_SLOTA_TO_NB_N<3> ARROW C07
97 84 9 PCIE_SLOTA_TO_NB_P<3> ARROW C06
97 84 9 PCIE_SLOTA_TO_NB_N<4> ARROW E01
97 84 9 PCIE_SLOTA_TO_NB_P<4> ARROW E02
97 84 9 PCIE_SLOTA_TO_NB_N<5> ARROW J05
97 84 9 PCIE_SLOTA_TO_NB_P<5> ARROW J04
97 84 9 PCIE_SLOTA_TO_NB_N<6> ARROW H06
97 84 9 PCIE_SLOTA_TO_NB_P<6> ARROW G06
97 84 9 PCIE_SLOTA_TO_NB_N<7> ARROW E05
97 84 9 PCIE_SLOTA_TO_NB_P<7> ARROW D05
97 84 9 PCIE_SLOTA_TO_NB_N<8> ARROW D11
97 84 9 PCIE_SLOTA_TO_NB_P<8> ARROW E11
97 84 9 PCIE_SLOTA_TO_NB_N<9> ARROW F12
97 84 9 PCIE_SLOTA_TO_NB_P<9> ARROW F13
97 84 9 PCIE_SLOTA_TO_NB_N<10> ARROW H09
97 84 9 PCIE_SLOTA_TO_NB_P<10> ARROW G09
97 84 9 PCIE_SLOTA_TO_NB_N<11> ARROW F09
97 84 9 PCIE_SLOTA_TO_NB_P<11> ARROW F08
97 84 9 PCIE_SLOTA_TO_NB_N<12> ARROW G13
97 84 9 PCIE_SLOTA_TO_NB_P<12> ARROW H13
97 84 9 PCIE_SLOTA_TO_NB_N<13> ARROW C13
97 84 9 PCIE_SLOTA_TO_NB_P<13> ARROW C12
97 84 9 PCIE_SLOTA_TO_NB_N<14> ARROW D07
97 84 9 PCIE_SLOTA_TO_NB_P<14> ARROW E07
97 84 9 PCIE_SLOTA_TO_NB_N<15> ARROW G07
97 84 9 PCIE_SLOTA_TO_NB_P<15> ARROW F07

KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

82 7 =PP2V5_PWRON_NB_PCIE
R8200 8.2K 1% 1/16W MF-LF 402 RES
84 6 PCIE_SLOTA_PRSNT_L ARROW AJ02
PCIE_VCAL_RES0 F14
PCIE_VCAL_RES1 J14
R8201 200 1% 1/16W MF-LF 402 RES

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

=PPVCORE_PWRON_NB_PCIE 7 82
C8209 C8210 C8211 C8212 C8213 C8214 C8215 C8216 C8217 C8218 C8219 C8220 C8221
1 CAP 1UF 10% 6.3V CERM 402 2
GND

A06 A10 B02 B04 B08 B12 D02 D06 D10 D14 E08 E12 F01
GND

97 82 6 KOD_H05_GND
97 82 6 KOD_K07_GND
97 82 6 KOD_G10_GND
(THIS PAGE, X3)
H05 K07 G10
XW8200 XW8201 XW8202 SHORT SM
GND

J13 L13 H08
KOD_H08_GND 6 82 97
KOD_L13_GND 6 82 97
KOD_J13_GND 6 82 97
(THIS PAGE, X3)
XW8203 XW8204 XW8205 SHORT SM
GND

KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)

D03	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<0>	0.1UF	C8247	PCIE_NB_TO_SLOTA_N<0> 9 84 97
E03	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<0>	0.1UF	C8248	PCIE_NB_TO_SLOTA_P<0> 9 84 97
J01	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<1>	0.1UF	C8249	PCIE_NB_TO_SLOTA_N<1> 9 84 97
J02	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<1>	0.1UF	C8250	PCIE_NB_TO_SLOTA_P<1> 9 84 97
C01	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<2>	0.1UF	C8251	PCIE_NB_TO_SLOTA_N<2> 9 84 97
C02	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<2>	0.1UF	C8252	PCIE_NB_TO_SLOTA_P<2> 9 84 97
A07	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<3>	0.1UF	C8253	PCIE_NB_TO_SLOTA_N<3> 9 84 97
B07	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<3>	0.1UF	C8254	PCIE_NB_TO_SLOTA_P<3> 9 84 97
F03	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<4>	0.1UF	C8255	PCIE_NB_TO_SLOTA_N<4> 9 84 97
G03	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<4>	0.1UF	C8256	PCIE_NB_TO_SLOTA_P<4> 9 84 97
H03	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<5>	0.1UF	C8257	PCIE_NB_TO_SLOTA_N<5> 9 84 97
J03	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<5>	0.1UF	C8258	PCIE_NB_TO_SLOTA_P<5> 9 84 97
A03	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<6>	0.1UF	C8259	PCIE_NB_TO_SLOTA_N<6> 9 84 97
B03	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<6>	0.1UF	C8260	PCIE_NB_TO_SLOTA_P<6> 9 84 97
A05	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<7>	0.1UF	C8261	PCIE_NB_TO_SLOTA_N<7> 9 84 97
B05	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<7>	0.1UF	C8262	PCIE_NB_TO_SLOTA_P<7> 9 84 97
C11	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<8>	0.1UF	C8263	PCIE_NB_TO_SLOTA_N<8> 9 84 97
C10	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<8>	0.1UF	C8264	PCIE_NB_TO_SLOTA_P<8> 9 84 97
B11	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<9>	0.1UF	C8265	PCIE_NB_TO_SLOTA_N<9> 9 84 97
A11	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<9>	0.1UF	C8266	PCIE_NB_TO_SLOTA_P<9> 9 84 97
F11	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<10>	0.1UF	C8267	PCIE_NB_TO_SLOTA_N<10> 9 84 97
F10	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<10>	0.1UF	C8268	PCIE_NB_TO_SLOTA_P<10> 9 84 97
B09	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<11>	0.1UF	C8269	PCIE_NB_TO_SLOTA_N<11> 9 84 97
A09	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<11>	0.1UF	C8270	PCIE_NB_TO_SLOTA_P<11> 9 84 97
D13	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<12>	0.1UF	C8271	PCIE_NB_TO_SLOTA_N<12> 9 84 97
E13	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<12>	0.1UF	C8272	PCIE_NB_TO_SLOTA_P<12> 9 84 97
B13	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<13>	0.1UF	C8273	PCIE_NB_TO_SLOTA_N<13> 9 84 97
A13	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<13>	0.1UF	C8274	PCIE_NB_TO_SLOTA_P<13> 9 84 97
D09	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<14>	0.1UF	C8275	PCIE_NB_TO_SLOTA_N<14> 9 84 97
E09	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<14>	0.1UF	C8276	PCIE_NB_TO_SLOTA_P<14> 9 84 97
C08	ARROW 97 9 PCIE_NB_TO_SLOTA_NF<15>	0.1UF	C8277	PCIE_NB_TO_SLOTA_N<15> 9 84 97
C09	ARROW 97 9 PCIE_NB_TO_SLOTA_PF<15>	0.1UF	C8278	PCIE_NB_TO_SLOTA_P<15> 9 84 97

G11 NC_A_AVREG_2 6
J08 NC_A_AVREG_1 6
E04 NC_A_AVREG_0 6

=PPVCORE_PWRON_NB_PCIE 7 82
C8231 C8232 C8233 C8234 C8235 C8236 C8241 C8242 C8243 C8237 C8238 C8239 C8240
1 CAP 1UF 10% 6.3V CERM 402 2
GND

F04 F06 G14 H02 H12 K10 K14 L12 M11 M13
GND

KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)

KODIAK PCI-E X16

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:23:38 2006

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APPLE_DSIZEPAGE DRAWING

TABLE_5_HEAD

TABLE_5_ITEM

338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT	CRITICAL

TABLE_5_ITEM

338S0265	1	IC,RV380 XT A23, GRAPHICS CTLR	U8400	RV380XT	CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

=PP1V2_GPU_PCIE
THIS IS ALIASED TO
PPVCORE_GPU ON PAGE 7

R8460 BRINGS VDDR FROM CORE (1.35) TO 1.2

R8460 0.300 RES 5% 1/8W MF 805 — PP1V2_GPU_PCIE_VDDR (84) VOLTAGE=1.2V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

R8461 0.300 RES 5% 1/8W MF 805

C8460 1UF CAP 10% 6.3V CERM 402
C8461 1UF CAP 10% 6.3V CERM 402
C8462 1UF CAP 10% 6.3V CERM 402
C8463 0.1UF CAP 20% 10V CERM 402
C8464 0.1UF CAP 20% 10V CERM 402
C8465 0.1UF CAP 20% 10V CERM 402
C8466 0.1UF CAP 20% 10V CERM 402

GND

GROUND VIAS FOR LAYER TRANSITIONS

ZH8400 HOLE_VIA
ZH8401 HOLE_VIA
ZH8402 HOLE_VIA
ZH8403 HOLE_VIA
ZH8404 HOLE_VIA
ZH8405 HOLE_VIA
ZH8406 HOLE_VIA
ZH8407 HOLE_VIA
ZH8408 HOLE_VIA
ZH8409 HOLE_VIA
ZH8410 HOLE_VIA
ZH8411 HOLE_VIA
ZH8412 HOLE_VIA
ZH8413 HOLE_VIA
ZH8414 HOLE_VIA
ZH8415 HOLE_VIA
ZH8416 HOLE_VIA
ZH8417 HOLE_VIA
ZH8418 HOLE_VIA
ZH8419 HOLE_VIA

GND

PP1V2_GPU_PCIE_PVDD (84 85)

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

C8450 1UF CAP 10% 6.3V CERM 402
C8451 1UF CAP 10% 6.3V CERM 402
C8452 0.1UF CAP 20% 10V CERM 402
C8453 0.1UF CAP 20% 10V CERM 402
C8454 0.1UF CAP 20% 10V CERM 402
C8455 0.1UF CAP 20% 10V CERM 402

GND

=PP1V8_GPU (93 87 86 85)

L8440 FERR-220-OHM IND 0805

PP1V8_GPU_PCIE_PVDD VOLTAGE=1.8V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM

C8440 1UF CAP 10% 6.3V CERM 402
C8441 1UF CAP 10% 6.3V CERM 402
C8442 0.1UF CAP 20% 10V CERM 402
C8443 0.1UF CAP 20% 10V CERM 402
C8444 0.1UF CAP 20% 10V CERM 402
C8445 0.1UF CAP 20% 10V CERM 402

GND

ATI_RV370XT: T23 U23 V23 W23 N23 N24 P23 AG26 AG27 AG28 AJ30 AK25

PLACE R8470 CLOSE TO U9670

U9670 74LC125 TSSOP (14 74125 11 7 13)

=GPU_RESET_L (20) — 12

R8469 8.2K RES 5% 1/16W MF-LF 402 — GND

ATI_RESET_L — R8470 33 RES 5% 1/16W MF-LF 402

AD25 ATI_RESET_L_R

PP1V2_GPU_PCIE_PVDD (84 85)

R8471 301 RES 1% 1/16W MF-LF 402

R8472 21 RES 1% 1/16W MF-LF 402 — CKA_P<0>

R8473 21 RES 1% 1/16W MF-LF 402

R8474 60.4 RES 1% 1/16W MF-LF 402

C8472 5PF CAP +/-0.25PF 50V CERM 402 — GND

R8476 60.4 RES 1% 1/16W MF-LF 402

C8473 5PF CAP +/-0.25PF 50V CERM 402

R8475 21 RES 1% 1/16W MF-LF 402 — CKA_N<0>

R8477 21 RES 1% 1/16W MF-LF 402

R8478 301 RES 1% 1/16W MF-LF 402

PP1V2_GPU_PCIE_PVDD (84 85)

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

CLK_PCIE_SLOTA_P<0> (97 26)
CLK_PCIE_SLOTA_N<0> (97 26)

CLK_PCIE_SLOTA_PF<0> (97) AF27
CLK_PCIE_SLOTA_NF<0> (97) AE27

U8400
RV370XT
BGA

OMIT

PCIE_NB_TO_SLOTA_P<0>	(97 82 9)	AH30
PCIE_NB_TO_SLOTA_N<0>	(97 82 9)	AG30
PCIE_NB_TO_SLOTA_P<1>	(97 82 9)	AG29
PCIE_NB_TO_SLOTA_N<1>	(97 82 9)	AF29
PCIE_NB_TO_SLOTA_P<2>	(97 82 9)	AE29
PCIE_NB_TO_SLOTA_N<2>	(97 82 9)	AE30
PCIE_NB_TO_SLOTA_P<3>	(97 82 9)	AD30
PCIE_NB_TO_SLOTA_N<3>	(97 82 9)	AD29
PCIE_NB_TO_SLOTA_P<4>	(97 82 9)	AC29
PCIE_NB_TO_SLOTA_N<4>	(97 82 9)	AB29
PCIE_NB_TO_SLOTA_P<5>	(97 82 9)	AB30
PCIE_NB_TO_SLOTA_N<5>	(97 82 9)	AA30
PCIE_NB_TO_SLOTA_P<6>	(97 82 9)	AA29
PCIE_NB_TO_SLOTA_N<6>	(97 82 9)	Y29
PCIE_NB_TO_SLOTA_P<7>	(97 82 9)	W29
PCIE_NB_TO_SLOTA_N<7>	(97 82 9)	W30
PCIE_NB_TO_SLOTA_P<8>	(97 82 9)	V30
PCIE_NB_TO_SLOTA_N<8>	(97 82 9)	V29
PCIE_NB_TO_SLOTA_P<9>	(97 82 9)	U29
PCIE_NB_TO_SLOTA_N<9>	(97 82 9)	T29
PCIE_NB_TO_SLOTA_P<10>	(97 82 9)	T30
PCIE_NB_TO_SLOTA_N<10>	(97 82 9)	R30
PCIE_NB_TO_SLOTA_P<11>	(97 82 9)	R29
PCIE_NB_TO_SLOTA_N<11>	(97 82 9)	P29
PCIE_NB_TO_SLOTA_P<12>	(97 82 9)	N29
PCIE_NB_TO_SLOTA_N<12>	(97 82 9)	N30
PCIE_NB_TO_SLOTA_P<13>	(97 82 9)	M30
PCIE_NB_TO_SLOTA_N<13>	(97 82 9)	M29
PCIE_NB_TO_SLOTA_P<14>	(97 82 9)	L29
PCIE_NB_TO_SLOTA_N<14>	(97 82 9)	K29
PCIE_NB_TO_SLOTA_P<15>	(97 82 9)	K30
PCIE_NB_TO_SLOTA_N<15>	(97 82 9)	J30

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

AF26 (97 9)	PCIE_SLOTA_TO_NB_PF<0>	0.1UF	C8400	PCIE_SLOTA_TO_NB_P<0>	(9 82 97)
AE26 (97 9)	PCIE_SLOTA_TO_NB_NF<0>	0.1UF	C8401	PCIE_SLOTA_TO_NB_N<0>	(9 82 97)
AC25 (97 9)	PCIE_SLOTA_TO_NB_PF<1>	0.1UF	C8402	PCIE_SLOTA_TO_NB_P<1>	(9 82 97)
AB25 (97 9)	PCIE_SLOTA_TO_NB_NF<1>	0.1UF	C8403	PCIE_SLOTA_TO_NB_N<1>	(9 82 97)
AC27 (97 9)	PCIE_SLOTA_TO_NB_PF<2>	0.1UF	C8404	PCIE_SLOTA_TO_NB_P<2>	(9 82 97)
AB27 (97 9)	PCIE_SLOTA_TO_NB_NF<2>	0.1UF	C8405	PCIE_SLOTA_TO_NB_N<2>	(9 82 97)
AC26 (97 9)	PCIE_SLOTA_TO_NB_PF<3>	0.1UF	C8406	PCIE_SLOTA_TO_NB_P<3>	(9 82 97)
AB26 (97 9)	PCIE_SLOTA_TO_NB_NF<3>	0.1UF	C8407	PCIE_SLOTA_TO_NB_N<3>	(9 82 97)
Y25 (97 9)	PCIE_SLOTA_TO_NB_PF<4>	0.1UF	C8408	PCIE_SLOTA_TO_NB_P<4>	(9 82 97)
W25 (97 9)	PCIE_SLOTA_TO_NB_NF<4>	0.1UF	C8409	PCIE_SLOTA_TO_NB_N<4>	(9 82 97)
Y27 (97 9)	PCIE_SLOTA_TO_NB_PF<5>	0.1UF	C8410	PCIE_SLOTA_TO_NB_P<5>	(9 82 97)
W27 (97 9)	PCIE_SLOTA_TO_NB_NF<5>	0.1UF	C8411	PCIE_SLOTA_TO_NB_N<5>	(9 82 97)
Y26 (97 9)	PCIE_SLOTA_TO_NB_PF<6>	0.1UF	C8412	PCIE_SLOTA_TO_NB_P<6>	(9 82 97)
W26 (97 9)	PCIE_SLOTA_TO_NB_NF<6>	0.1UF	C8413	PCIE_SLOTA_TO_NB_N<6>	(9 82 97)
U25 (97 9)	PCIE_SLOTA_TO_NB_PF<7>	0.1UF	C8414	PCIE_SLOTA_TO_NB_P<7>	(9 82 97)
T25 (97 9)	PCIE_SLOTA_TO_NB_NF<7>	0.1UF	C8415	PCIE_SLOTA_TO_NB_N<7>	(9 82 97)
U27 (97 9)	PCIE_SLOTA_TO_NB_PF<8>	0.1UF	C8416	PCIE_SLOTA_TO_NB_P<8>	(9 82 97)
T27 (97 9)	PCIE_SLOTA_TO_NB_NF<8>	0.1UF	C8417	PCIE_SLOTA_TO_NB_N<8>	(9 82 97)
U26 (97 9)	PCIE_SLOTA_TO_NB_PF<9>	0.1UF	C8418	PCIE_SLOTA_TO_NB_P<9>	(9 82 97)
T26 (97 9)	PCIE_SLOTA_TO_NB_NF<9>	0.1UF	C8419	PCIE_SLOTA_TO_NB_N<9>	(9 82 97)
P25 (97 9)	PCIE_SLOTA_TO_NB_PF<10>	0.1UF	C8420	PCIE_SLOTA_TO_NB_P<10>	(9 82 97)
N25 (97 9)	PCIE_SLOTA_TO_NB_NF<10>	0.1UF	C8421	PCIE_SLOTA_TO_NB_N<10>	(9 82 97)
P27 (97 9)	PCIE_SLOTA_TO_NB_PF<11>	0.1UF	C8422	PCIE_SLOTA_TO_NB_P<11>	(9 82 97)
N27 (97 9)	PCIE_SLOTA_TO_NB_NF<11>	0.1UF	C8423	PCIE_SLOTA_TO_NB_N<11>	(9 82 97)
P26 (97 9)	PCIE_SLOTA_TO_NB_PF<12>	0.1UF	C8424	PCIE_SLOTA_TO_NB_P<12>	(9 82 97)
N26 (97 9)	PCIE_SLOTA_TO_NB_NF<12>	0.1UF	C8425	PCIE_SLOTA_TO_NB_N<12>	(9 82 97)
L25 (97 9)	PCIE_SLOTA_TO_NB_PF<13>	0.1UF	C8426	PCIE_SLOTA_TO_NB_P<13>	(9 82 97)
K25 (97 9)	PCIE_SLOTA_TO_NB_NF<13>	0.1UF	C8427	PCIE_SLOTA_TO_NB_N<13>	(9 82 97)
L27 (97 9)	PCIE_SLOTA_TO_NB_PF<14>	0.1UF	C8428	PCIE_SLOTA_TO_NB_P<14>	(9 82 97)
K27 (97 9)	PCIE_SLOTA_TO_NB_NF<14>	0.1UF	C8429	PCIE_SLOTA_TO_NB_N<14>	(9 82 97)
L26 (97 9)	PCIE_SLOTA_TO_NB_PF<15>	0.1UF	C8430	PCIE_SLOTA_TO_NB_P<15>	(9 82 97)
K26 (97 9)	PCIE_SLOTA_TO_NB_NF<15>	0.1UF	C8431	PCIE_SLOTA_TO_NB_N<15>	(9 82 97)

PP1V2_GPU_PCIE_VDDR (84) — R8400 100 RES 1% 1/16W MF-LF 402

GPU_PCIE_CALRN AB24
GPU_PCIE_CALRP AC23

R8401 150 RES 1% 1/16W MF-LF 402 — GND

K28 L28 M24 M25 M26 M27 M28 N28 P28 R23

R24 R25 R26 R27 R28 T24 T28 U28 V24 V25 V26 V27 V28 W24 W28 Y28 AA23 AA24 AA25 AA26 AA27

GND

AB23 GPU_PCIE_CALI
AE25 GPU_PCIE_TEST

AH29 AF28 AE28 AD28 AD27 AD26 AD24 AC28 AB28 AA28

R8402 10K RES 1% 1/16W MF-LF 402 — GND

R8403 10K RES 1% 1/16W MF-LF 402

XW8405 SM — PCIE_SLOTA_PRSNT_L (82 6) — SHORT — GND

GPU PCIe

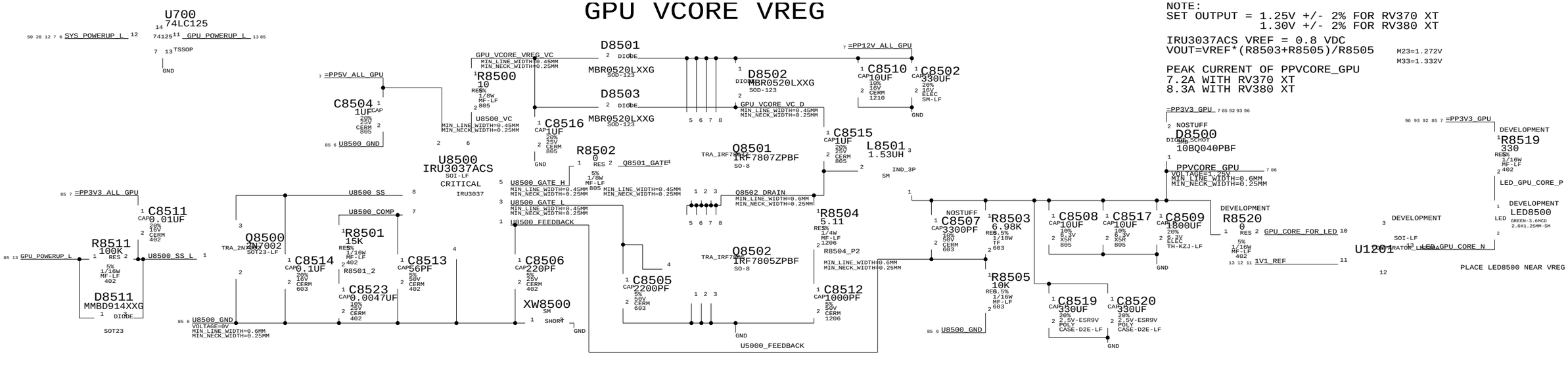
SYNC_MASTER=FINO-M23 SYNC_DATE=08/18/2005

051-6863 H

84 154

APPLE_DSIZEPAGE

GPU VCORE VREG



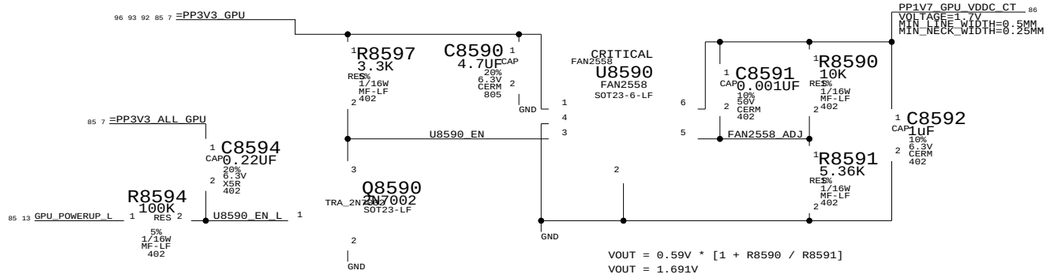
NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505

M23=1.272V
M33=1.332V

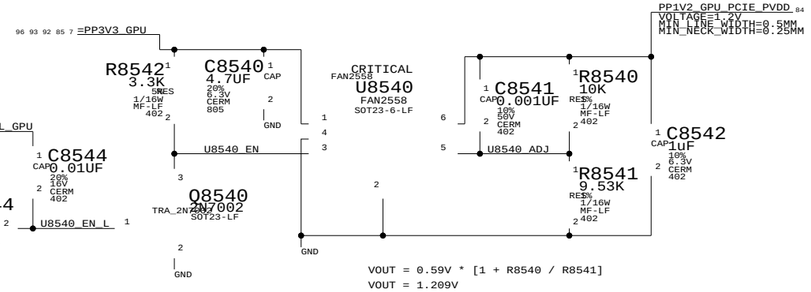
PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

GPU 1.7V VDDC_CT



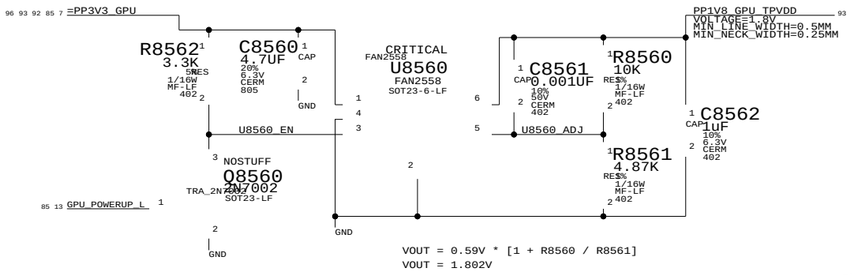
VOUT = 0.59V * [1 + R8590 / R8591]
VOUT = 1.691V

GPU 1.20V PCIE PVDD



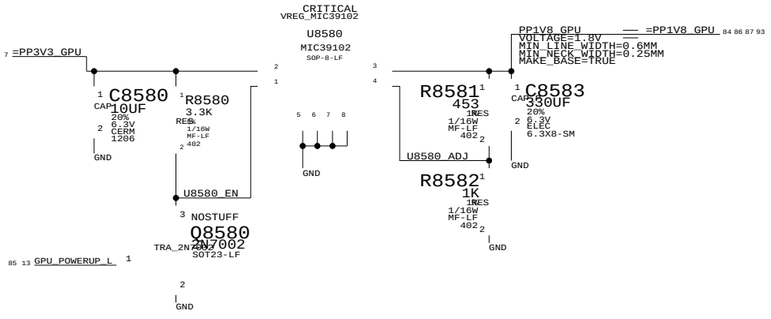
VOUT = 0.59V * [1 + R8540 / R8541]
VOUT = 1.209V

GPU 1.80V TPVDD

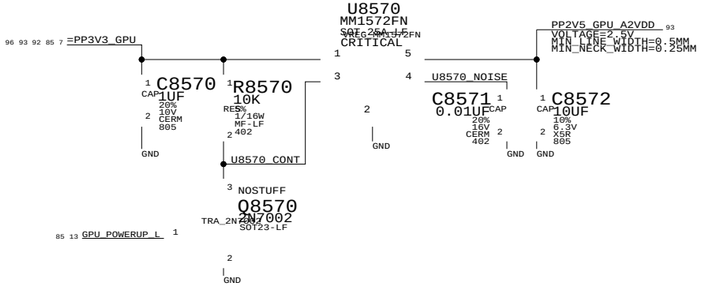


VOUT = 0.59V * [1 + R8560 / R8561]
VOUT = 1.802V

GPU 1.8V VREG



GPU 2.5V A2VDD

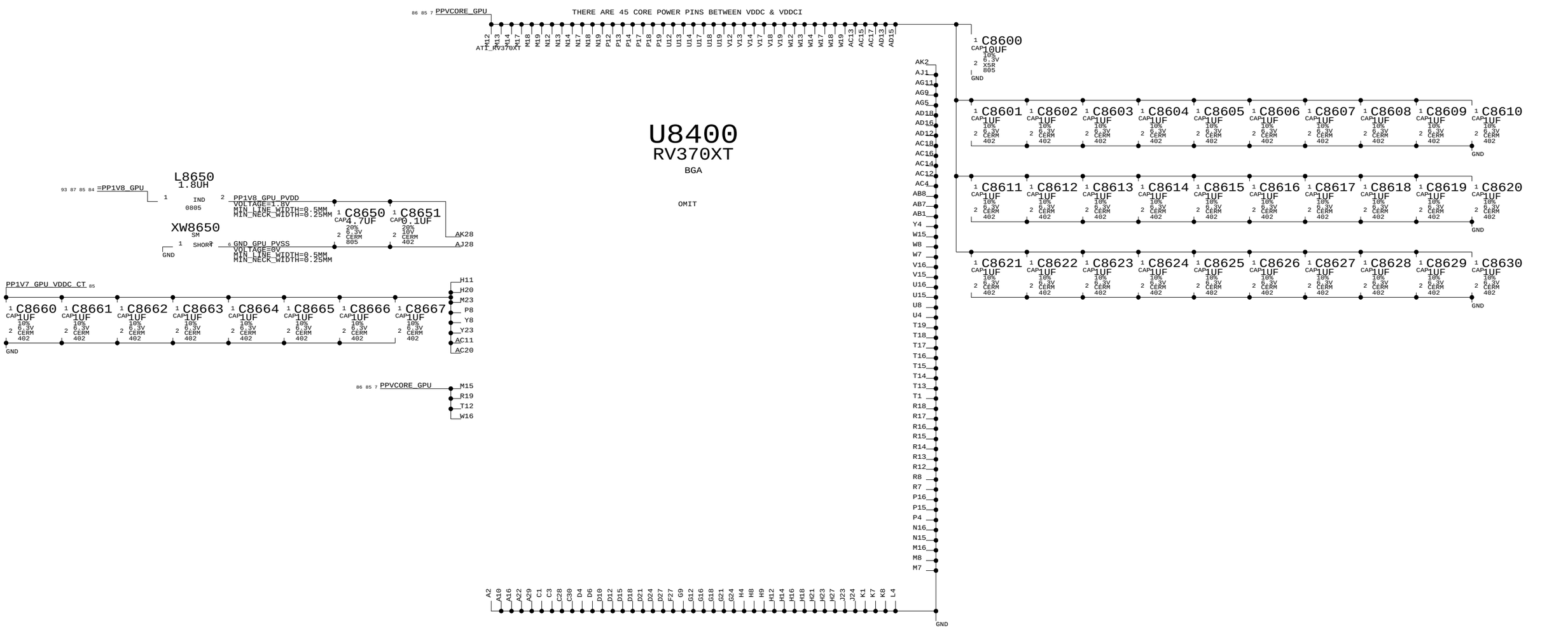


Graphics Vregs

SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER



GPU Core Power

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

051-6863 H

APPLE_DSIZEPAGE

91 90 89 87 7 =PPV_GPU_MEM

C8700 CAP 10UF 10% 6.3V X5R 805
C8701 CAP 10UF 10% 6.3V X5R 805
C8702 CAP 0.1UF 20% 10V CERM 402
C8703 CAP 0.1UF 20% 10V CERM 402
C8704 CAP 0.1UF 20% 10V CERM 402
C8705 CAP 0.1UF 20% 10V CERM 402
C8706 CAP 0.1UF 20% 10V CERM 402
C8707 CAP 0.1UF 20% 10V CERM 402
C8708 CAP 0.1UF 20% 10V CERM 402
C8709 CAP 0.1UF 20% 10V CERM 402
C8710 CAP 0.1UF 20% 10V CERM 402
C8711 CAP 0.1UF 20% 10V CERM 402
C8712 CAP 0.1UF 20% 10V CERM 402
C8713 CAP 0.1UF 20% 10V CERM 402
C8714 CAP 0.1UF 20% 10V CERM 402
C8715 CAP 0.1UF 20% 10V CERM 402
C8716 CAP 0.1UF 20% 10V CERM 402
C8717 CAP 0.1UF 20% 10V CERM 402
C8718 CAP 0.1UF 20% 10V CERM 402
C8719 CAP 0.1UF 20% 10V CERM 402

GND

ATI_RV370XT

F18 N6 A3 A9 A15 A21 A28 B1 B30 D5 D8 D11 D14 D17 D20 D23 D26 E27 F4 G7 G10 G13 G15 G19 G22 G27 H10 H13 H15 H17

93 86 85 84 =PP1V8_GPU

L8730 1.8UH 0805

PP1V8_GPU_MPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

XW8730 SM SHORT

GND

GND_GPU_MPVSS
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

C8730 CAP 4.7UF 20% 6.3V CERM 805
C8731 CAP 0.1UF 20% 10V CERM 402

ATI_RV370XT

H19 H22 J1 J4 J7 J8 K23 K24 L8 L23 M4 N4 N7 N8 R1 R4 T7 T8 V4 V7 V8 AA1 AA4 AA7 AA8 AD4

OMIT

U8400
RV370XT
BGA

91 88	FBD<47>	H28
91 88	FBD<46>	H29
91 88	FBD<44>	J28
91 88	FBD<45>	J29
91 88	FBD<43>	J26
91 88	FBD<41>	H25
91 88	FBD<42>	H26
91 88	FBD<40>	G26
91 88	FBD<34>	G30
91 88	FBD<38>	D29
91 88	FBD<39>	D28
91 88	FBD<37>	E28
91 88	FBD<36>	E29
91 88	FBD<32>	G29
91 88	FBD<33>	G28
91 88	FBD<35>	F28
91 88	FBD<62>	G25
91 88	FBD<63>	F26
91 88	FBD<61>	E26
91 88	FBD<60>	F25
91 88	FBD<56>	E24
91 88	FBD<59>	F23
91 88	FBD<57>	E23
91 88	FBD<58>	D22
91 88	FBD<48>	B29
91 88	FBD<50>	C29
91 88	FBD<55>	C25
91 88	FBD<51>	C27
91 88	FBD<49>	B28
91 88	FBD<54>	B25
91 88	FBD<52>	C26
91 88	FBD<53>	B26
91 88	FBD<5>	F17
91 88	FBD<4>	E17
91 88	FBD<7>	D16
91 88	FBD<6>	F16
91 88	FBD<2>	E15
91 88	FBD<1>	F14
91 88	FBD<3>	E14
91 88	FBD<0>	F13
91 88	FBD<13>	C17
91 88	FBD<15>	B18
91 88	FBD<14>	B17
91 88	FBD<9>	B15
91 88	FBD<11>	C13
91 88	FBD<8>	B14
91 88	FBD<10>	C14
91 88	FBD<12>	C16
91 88	FBD<24>	A13
91 88	FBD<26>	A12
91 88	FBD<25>	C12
91 88	FBD<27>	B12
91 88	FBD<28>	C10
91 88	FBD<31>	C9
91 88	FBD<30>	B9
91 88	FBD<29>	B10
91 88	FBD<23>	E13
91 88	FBD<22>	E12
91 88	FBD<17>	E10
91 88	FBD<21>	F12
91 88	FBD<20>	F11
91 88	FBD<16>	E9
91 88	FBD<18>	F9
91 88	FBD<19>	F8

F19 M6 GND

E22	FBA<0>	88 89 91
B22	FBA<1>	88 89 91
B23	FBA<2>	88 89 91
B24	FBA<3>	88 89 91
C23	FBA<4>	88 89 91
C22	FBA<5>	88 89 91
F22	FBA<6>	88 89 91
F21	FBA<7>	88 89 91
C21	FBA<8>	88 89 91
A24	FBA<9>	88 89 91
C24	FBA<10>	88 89 91
A25	FBA<11>	88 89 91
E21	FBA<12>	88 89 91
B20	FBA<13>	88 89 91
C19	TP_FBA<14>	
J25	FBDQM<5>	88 91
F29	FBDQM<4>	88 91
E25	FBDQM<7>	88 91
A27	FBDQM<6>	88 91
F15	FBDQM<0>	88 91
C15	FBDQM<1>	88 91
C11	FBDQM<3>	88 91
E11	FBDQM<2>	88 91
J27	FBDQS<5>	88 91
F30	FBDQS<4>	88 91
F24	FBDQS<7>	88 91
B27	FBDQS<6>	88 91
E16	FBDQS<0>	88 91
B16	FBDQS<1>	88 91
B11	FBDQS<3>	88 91
F10	FBDQS<2>	88 91
A19	FBARAS_L	88 89 91
E18	FBACAS_L	88 89 91
E19	FBAWE_L	88 89 91
E20	FBACS0_L	88 89 91
F20	TP_FBACS1_L	
B19	FBACKE	88 89 91
B21	FBACLK1	88 89
C20	FBACLK1_L	88 89
C18	FBACLK0	88 89
A18	FBACLK0_L	88 89

R8700 10K RES 5% 1/16W MF-LF 402

GND

B7 GPU_MVREFD
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

B8 GPU_MVREFS
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM

D30 TP_GPU_DIMA_0
B13 TP_GPU_DIMA_1

=PPV_GPU_MEM 7 87 89 90 91

R8720 100 RES 1% 1/16W MF-LF 402

C8721 CAP 0.1UF 20% 10V CERM 402

R8721 100 RES 1% 1/16W MF-LF 402

GND

=PPV_GPU_MEM 7 87 89 90 91

R8722 100 RES 1% 1/16W MF-LF 402

C8723 CAP 0.1UF 20% 10V CERM 402

R8723 100 RES 1% 1/16W MF-LF 402

GND

91 88	FBD<124>	D7
91 88	FBD<127>	F7
91 88	FBD<125>	E7
91 88	FBD<121>	G6
91 88	FBD<120>	G5
91 88	FBD<123>	F5
91 88	FBD<122>	E5
91 88	FBD<126>	C4
91 88	FBD<113>	B5
91 88	FBD<112>	C5
91 88	FBD<114>	A4
91 88	FBD<115>	B4
91 88	FBD<117>	C2
91 88	FBD<119>	D3
91 88	FBD<116>	D1
91 88	FBD<118>	D2
91 88	FBD<111>	G4
91 88	FBD<110>	H6
91 88	FBD<109>	H5
91 88	FBD<108>	J6
91 88	FBD<104>	K5
91 88	FBD<105>	K4
91 88	FBD<107>	L6
91 88	FBD<106>	L5
91 88	FBD<103>	G2
91 88	FBD<99>	F3
91 88	FBD<102>	H2
91 88	FBD<97>	E2
91 88	FBD<98>	F2
91 88	FBD<100>	J3
91 88	FBD<96>	F1
91 88	FBD<101>	H3
91 88	FBD<86>	U6
91 88	FBD<84>	U5
91 88	FBD<85>	U3
91 88	FBD<87>	V6
91 88	FBD<82>	W5
91 88	FBD<83>	W4
91 88	FBD<80>	Y6
91 88	FBD<81>	Y5
91 88	FBD<88>	U2
91 88	FBD<91>	V2
91 88	FBD<90>	V1
91 88	FBD<89>	V3
91 88	FBD<92>	W3
91 88	FBD<93>	Y2
91 88	FBD<94>	Y3
91 88	FBD<95>	AA2
91 88	FBD<71>	AA6
91 88	FBD<69>	AA5
91 88	FBD<68>	AB6
91 88	FBD<70>	AB5
91 88	FBD<66>	AD6
91 88	FBD<64>	AD5
91 88	FBD<65>	AE5
91 88	FBD<67>	AE4
91 88	FBD<72>	AB2
91 88	FBD<73>	AB3
91 88	FBD<75>	AC2
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91 88	FBD<77>	AE3

OMIT

U8400
RV370XT
BGA

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M3	FBBA<2>	88 90 91
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L2	FBBA<4>	88 90 91
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P5	FBBA<12>	88 90 91
P3	FBBA<13>	88 90 91
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B2	FBDQM<14>	88 91
J5	FBDQM<13>	88 91
G3	FBDQM<12>	88 91
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W2	FBDQM<11>	88 91
AC6	FBDQM<8>	88 91
AD2	FBDQM<9>	88 91
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K6	FBDQS<13>	88 91
G1	FBDQS<12>	88 91
V5	FBDQS<10>	88 91
W1	FBDQS<11>	88 91
AC5	FBDQS<8>	88 91
AD1	FBDQS<9>	88 91
R2	FBBRAS_L	88 90 91
T5	FBBCAS_L	88 90 91
T6	FBBWE_L	88 90 91
R5	FBBCS0_L	88 90 91
R6	TP_FBBCS1_L	6
R3	FBBCKE	88 90 91
N1	FBBCLK1	88 90
N2	FBBCLK1_L	88 90
T2	FBBCLK0	88 90
T3	FBBCLK0_L	88 90

R8701 10K RES 5% 1/16W MF-LF 402

GND

MEMVMODE	
* 1.8V	01
2.5V	10
2.8V	11

91 90 89 87 7 =PPV_GPU_MEM

C6 GPU_MEMVMODE0
C7 GPU_MEMVMODE1
C8 GPU_MEMTEST
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
E3 TP_GPU_DIMB_0
AA3 TP_GPU_DIMB_1

NOSTUFF R8724 4.7K RES 5% 1/16W MF-LF 402
R8726 4.7K RES 5% 1/16W MF-LF 402
R8728 47 RES 1% 1/16W MF-LF 402
R8725 4.7K RES 5% 1/16W MF-LF 402
NOSTUFF R8727 4.7K RES 5% 1/16W MF-LF 402

GND

GPU Frame Buffer

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FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

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FBDQS<4>	22	1	RES 2	R8804	RFBDQS<4> 89
FBDQS<5>	22	1	RES 2	R8805	RFBDQS<5> 89
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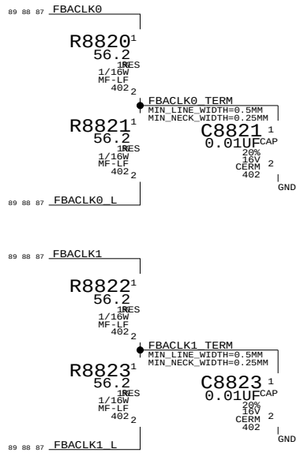
PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION



FRAME BUFFER B TERMINATION

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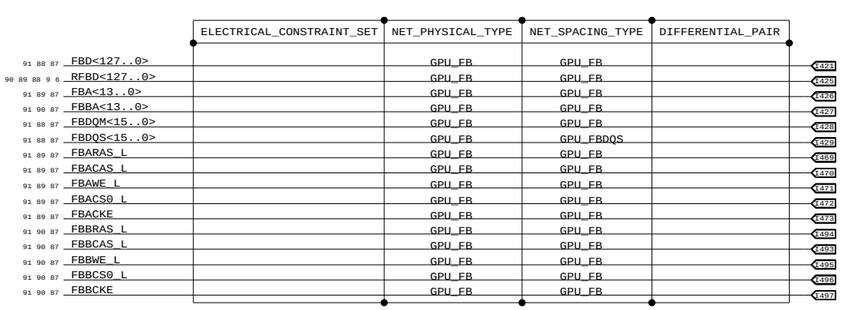

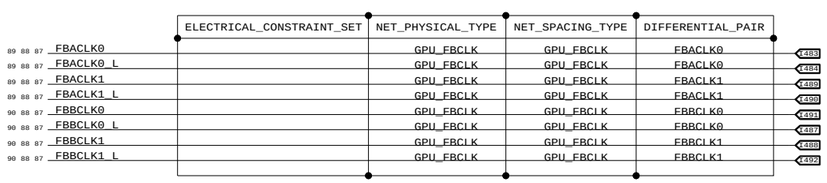

FB Series Termination

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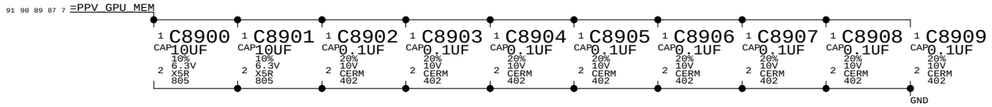

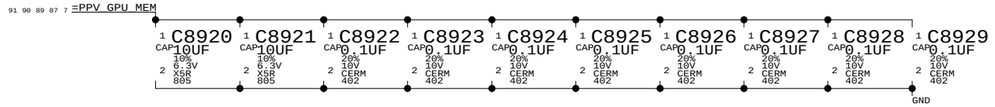

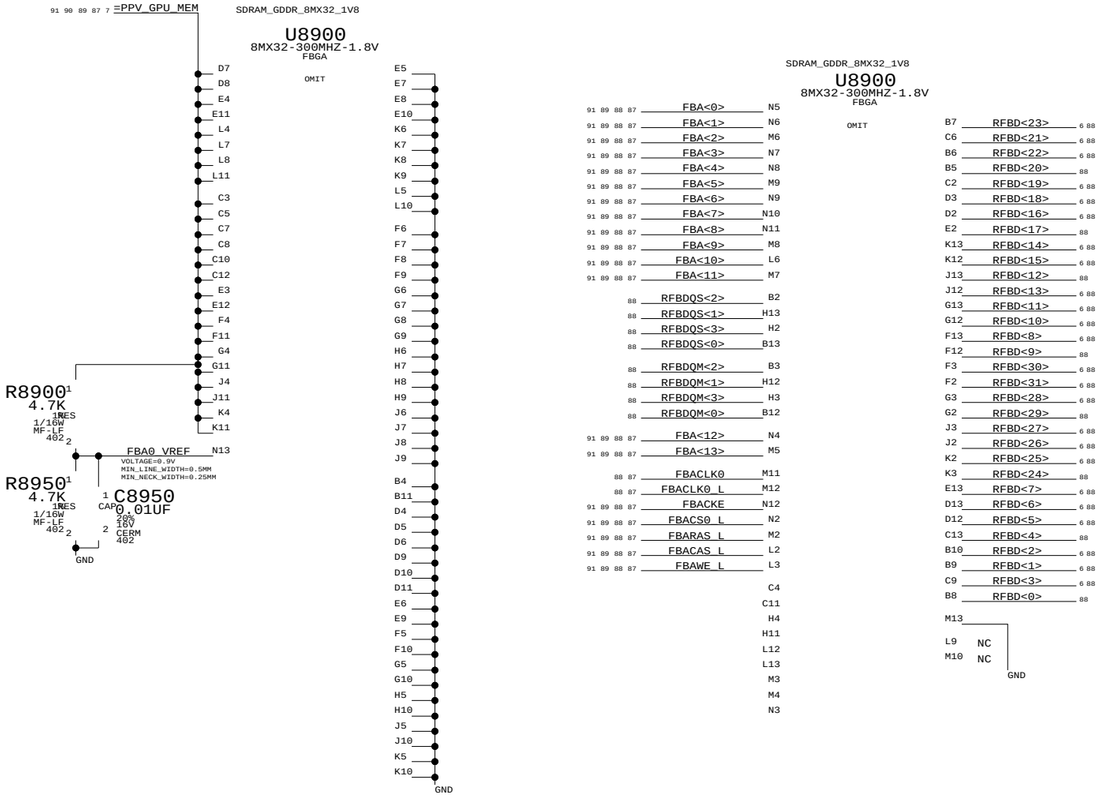

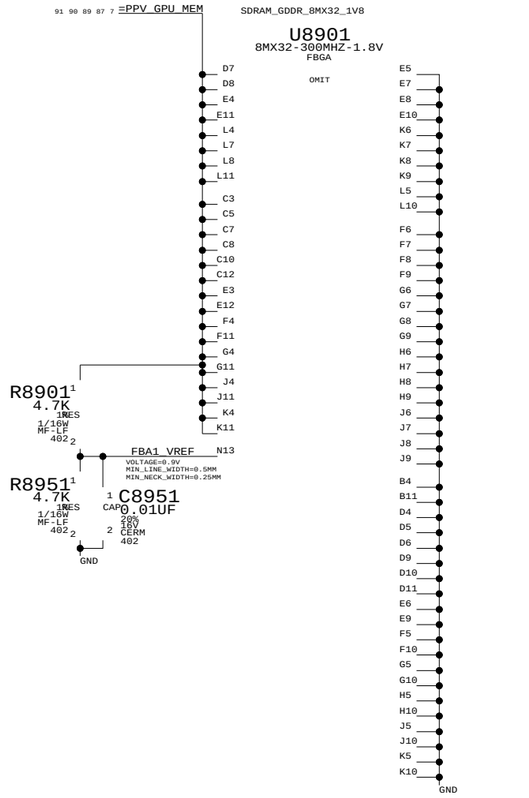

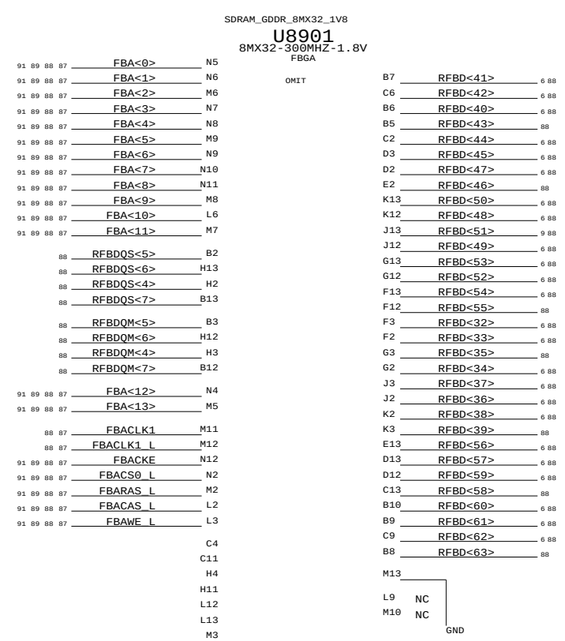

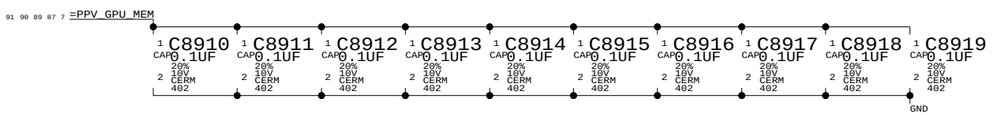

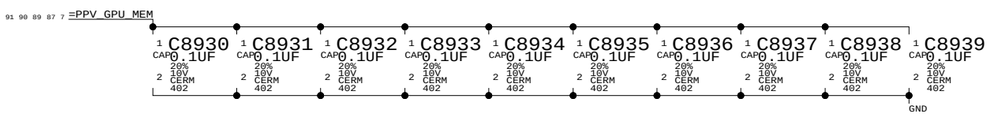

GROUND VIAS FOR SIGNAL LAYER TRANSITIONS

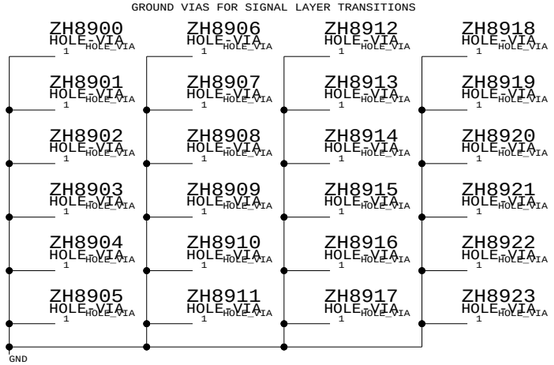

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TABLE_6_ITEM 333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
TABLE_6_ITEM 333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
TABLE_6_ITEM 333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
TABLE_6_ITEM 333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
TABLE_6_ITEM 333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
TABLE_6_ITEM 333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM A

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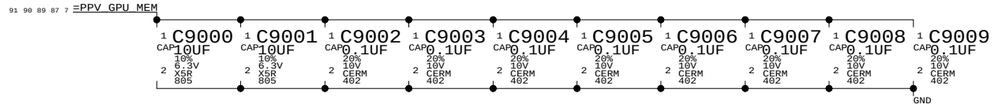

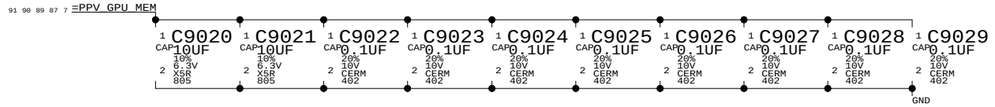

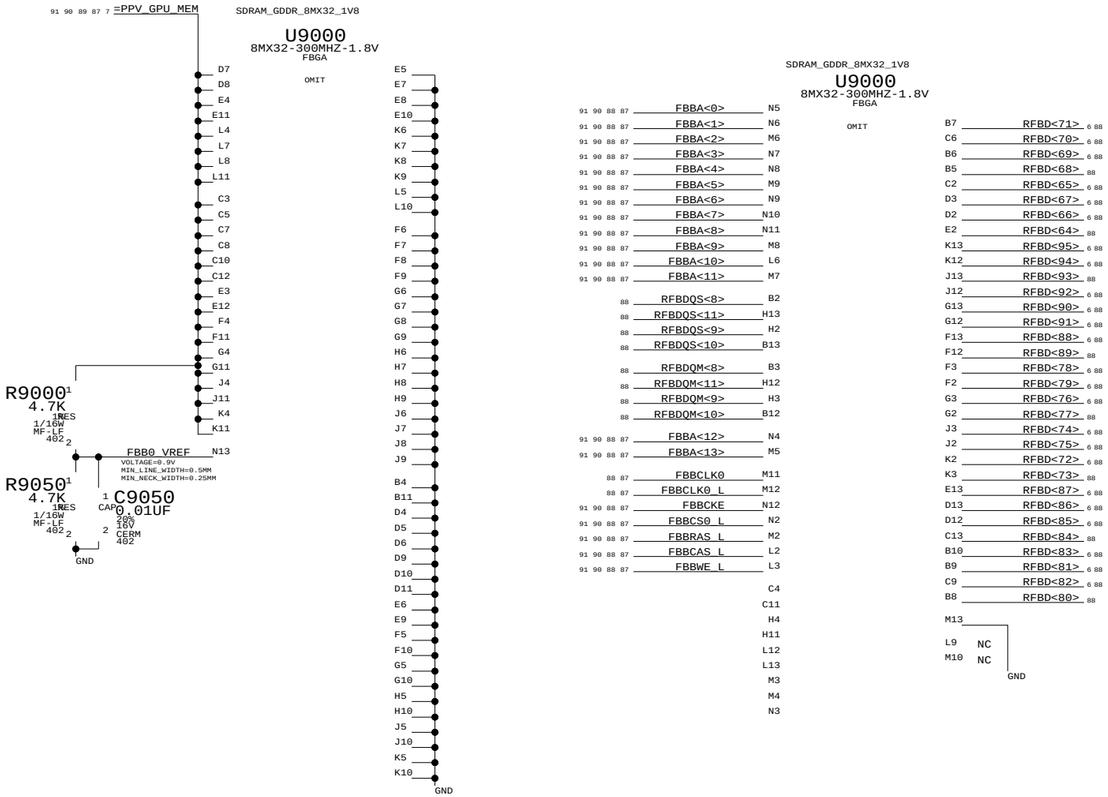

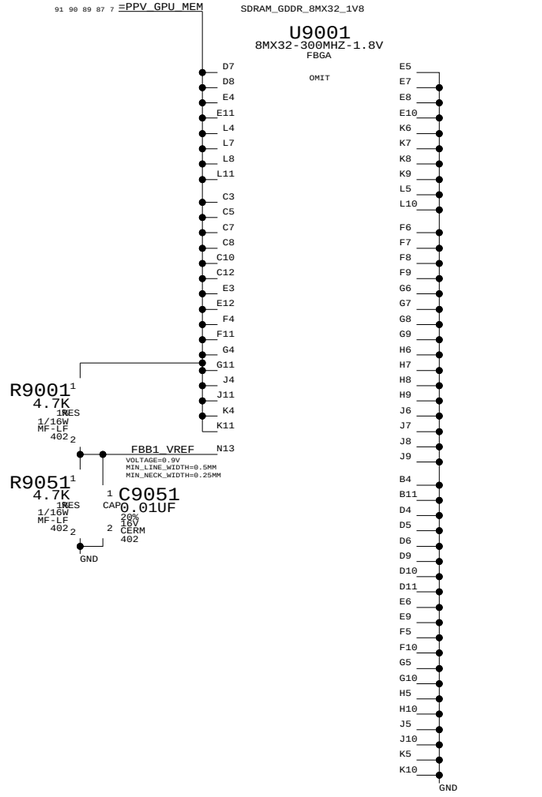

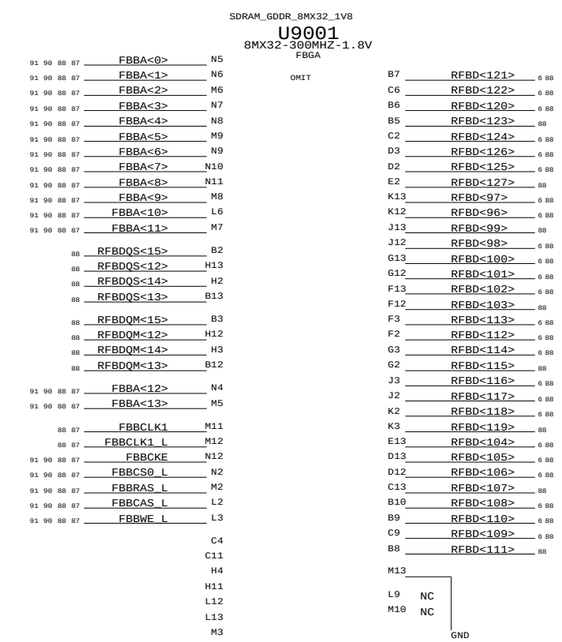

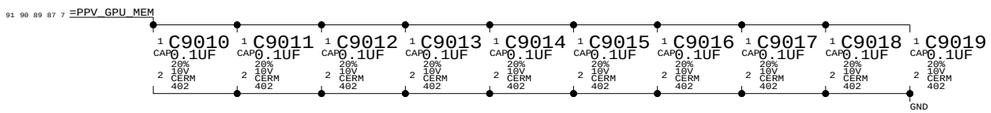

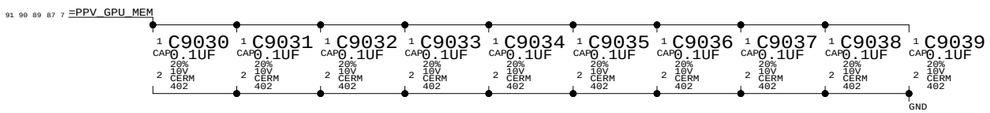

GROUND VIAS FOR SIGNAL LAYER TRANSITIONS

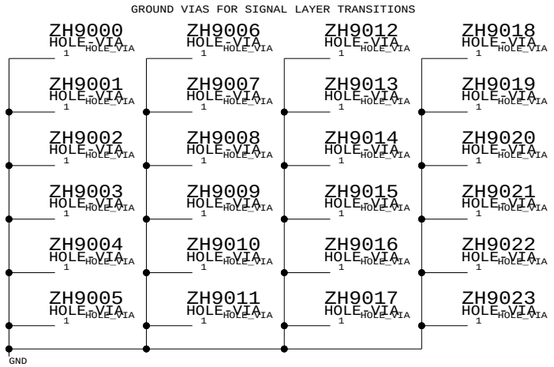

TABLE_6_HEAD

TABLE_6_ITEM 333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
TABLE_6_ITEM 333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
TABLE_6_ITEM 333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
TABLE_6_ITEM 333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
TABLE_6_ITEM 333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
TABLE_6_ITEM 333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

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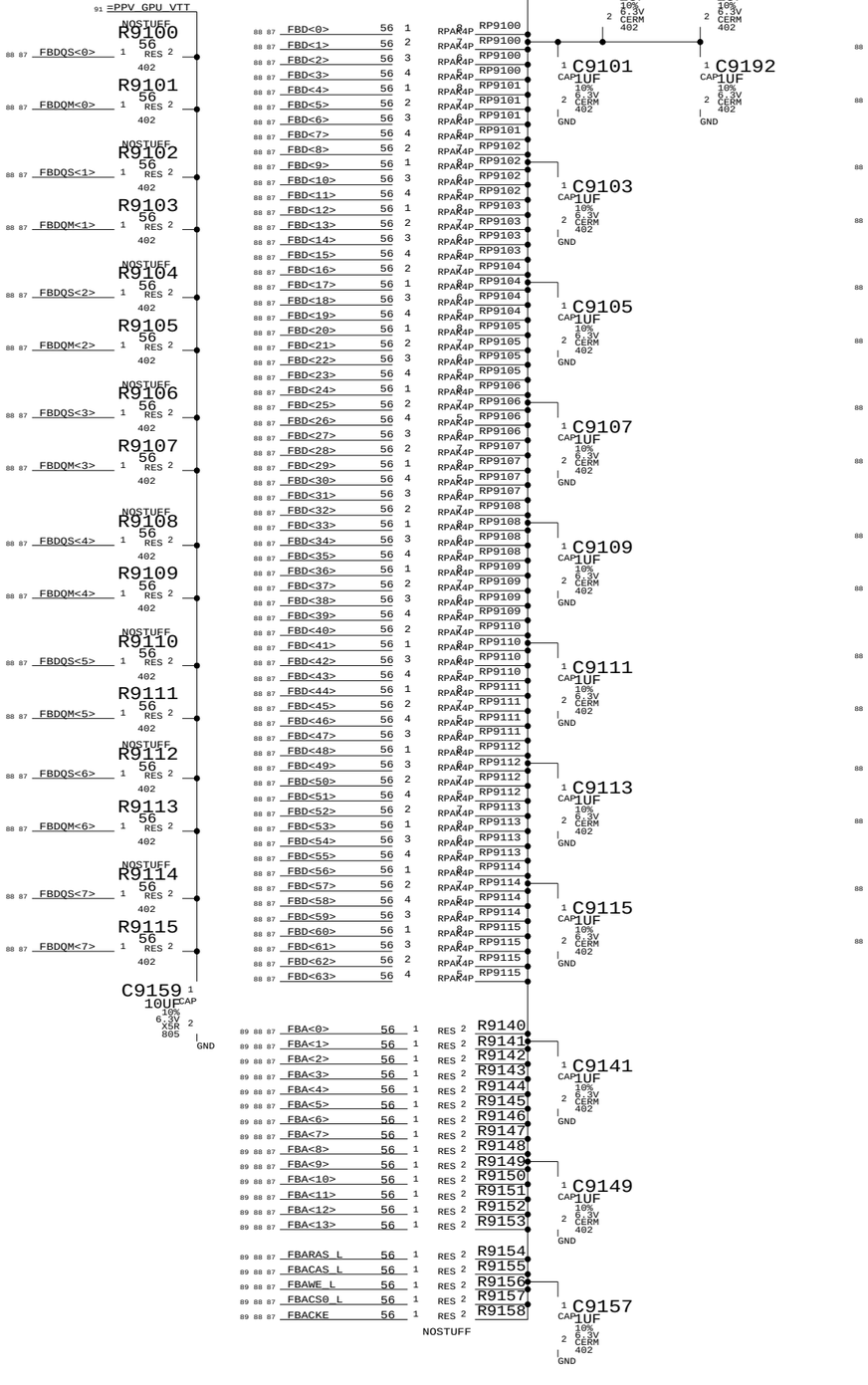
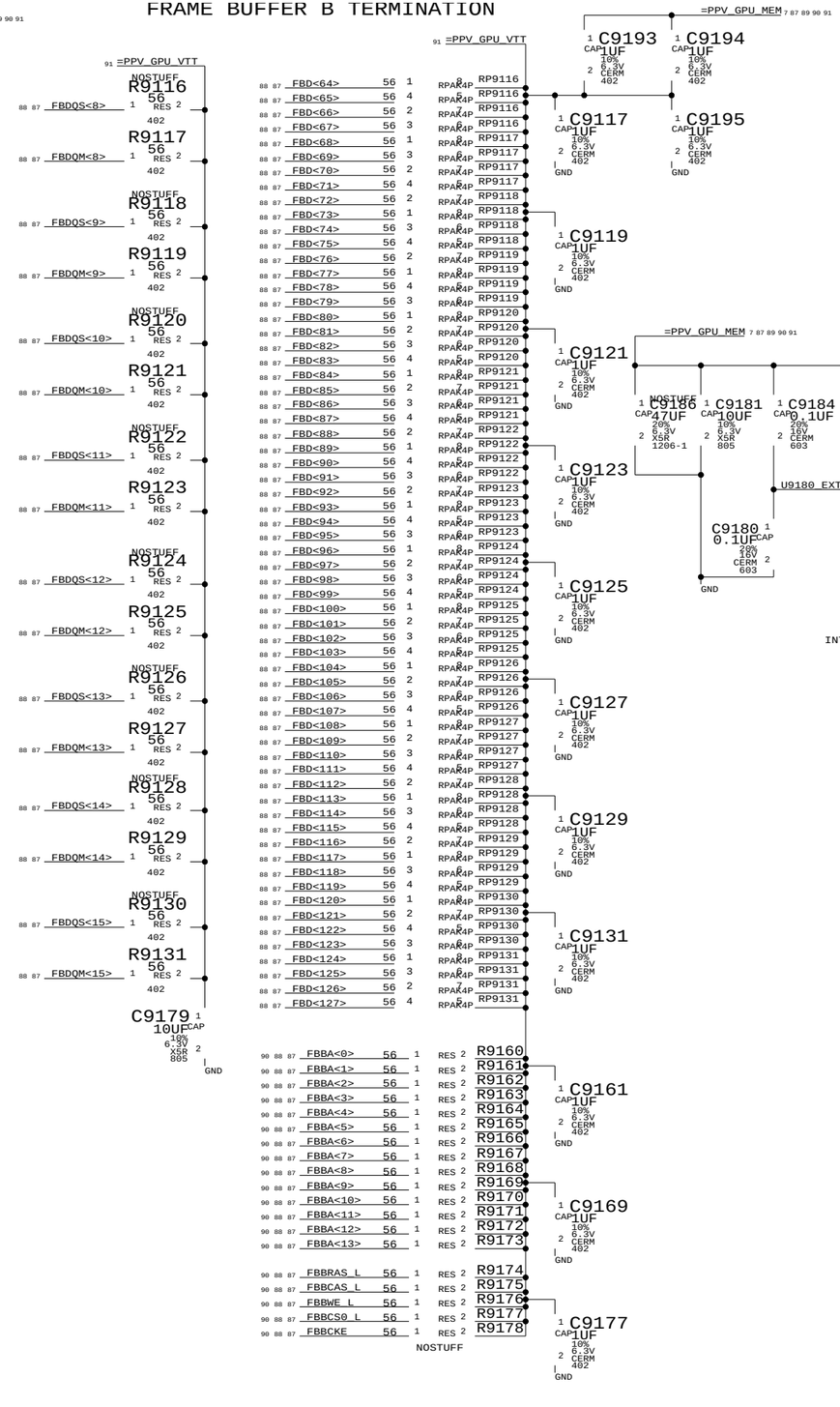
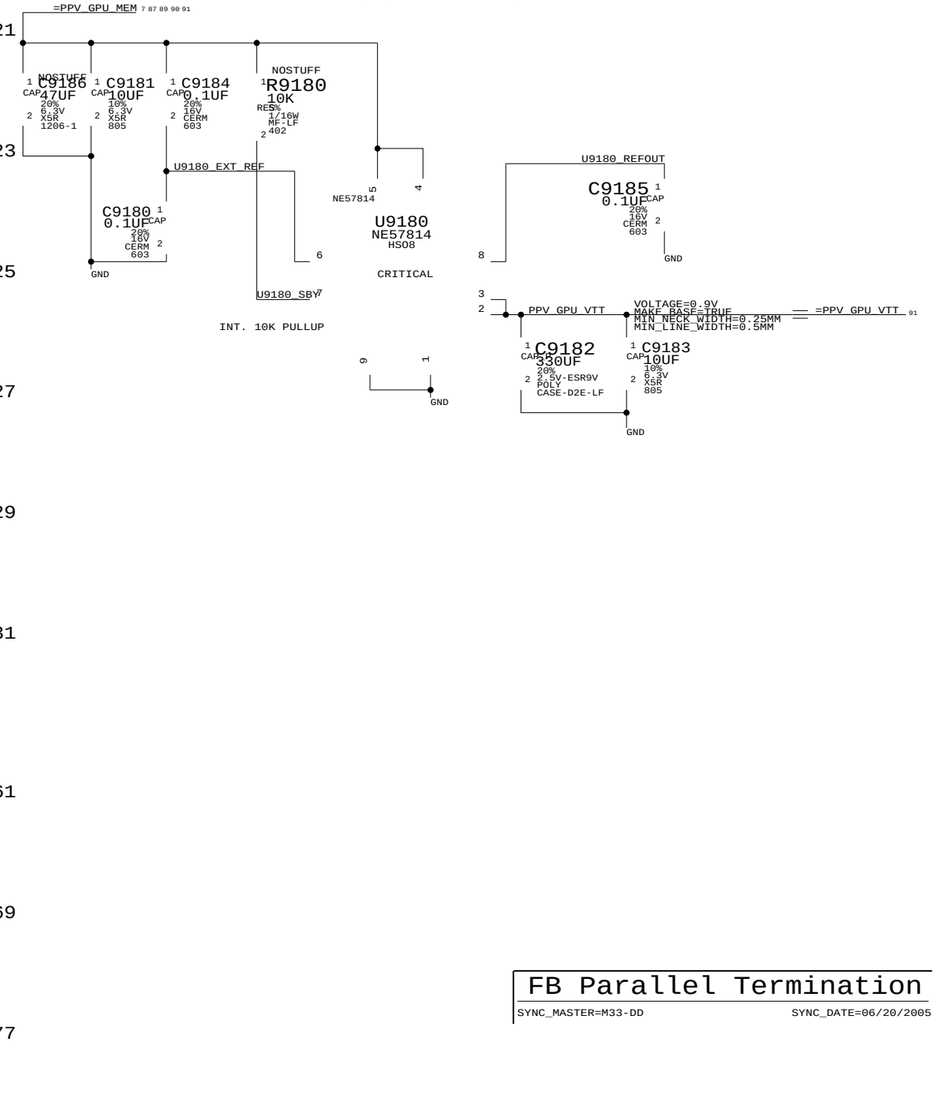
FRAME BUFFER A TERMINATION



FRAME BUFFER B TERMINATION



GPU VTT VREG



FB Parallel Termination

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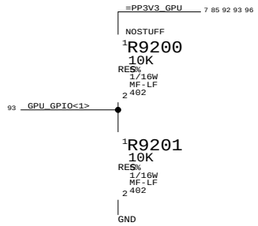
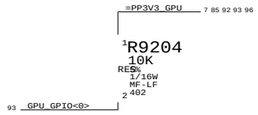
ATI STRAPS

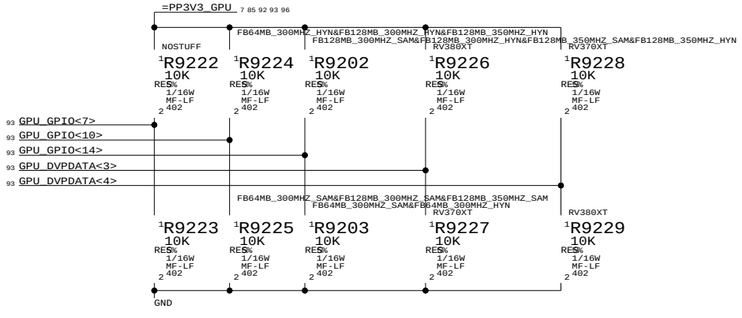


GPIO<1> TRANSMITTER DE-EMPHASIS (ACTIVE LOW)



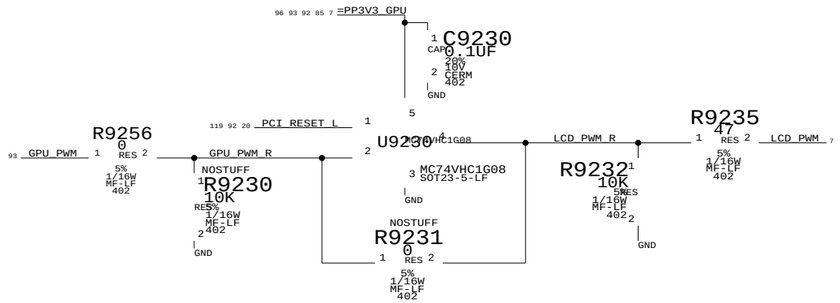
GPIO<0> TRANSMITTER POWER SAVINGS
(FEATURE DOES NOT WORK - PULLED HIGH TO DISABLE)

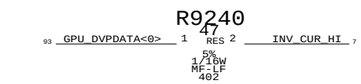
MEMORY STRAPS

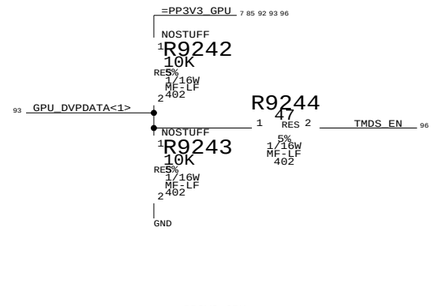


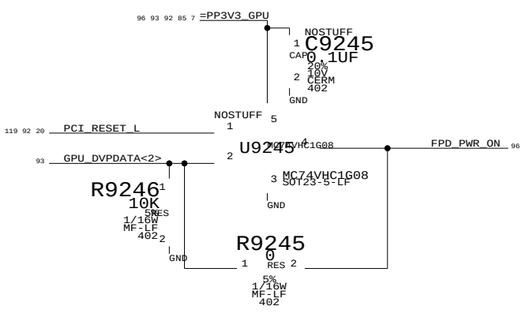
GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS









GPU Straps

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

L9380 FERR-EMI-100-OHM

L9370 FERR-EMI-100-OHM

(PLACE R9371 AND R9372 CLOSE TO OSCILLATOR PIN 8)

L9335 FERR-220-OHM

L9330 1.8UH

L9340 FERR-220-OHM

L9345 FERR-220-OHM

L9365 FERR-220-OHM

U9380 CY25811 SOI-LF

G9370 27.0000M OSC SM-1 OMIT

U8400 RV370XT BGA

OMIT

ATI_RV370XT

PLACE R9373 CLOSE TO ATI PIN AH28

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
TMDS_CKP	GPU_TMDS	GPU_TMDS	TMDS_CK	1572
TMDS_CKM	GPU_TMDS	GPU_TMDS	TMDS_CK	1573
TMDS_D0P	GPU_TMDS	GPU_TMDS	TMDS_D0	1574
TMDS_D0M	GPU_TMDS	GPU_TMDS	TMDS_D0	1575
TMDS_D1P	GPU_TMDS	GPU_TMDS	TMDS_D1	1576
TMDS_D1M	GPU_TMDS	GPU_TMDS	TMDS_D1	1577
TMDS_D2P	GPU_TMDS	GPU_TMDS	TMDS_D2	1578
TMDS_D2M	GPU_TMDS	GPU_TMDS	TMDS_D2	1579
ANALOG_GRN	GPU_VGA	GPU_VGA		1689
ANALOG_RED	GPU_VGA	GPU_VGA		1690
ANALOG_BLU	GPU_VGA	GPU_VGA		1691
ANALOG_HSYNC	GPU_VGA	GPU_VGA		1658
ANALOG_VSYNC	GPU_VGA	GPU_VGA		1661
I2C_GPU_TMDS_SCL		I2C		1680
I2C_GPU_TMDS_SDA		I2C		1681
I2C_GPU_MON_SCL		I2C		1682
I2C_GPU_MON_SDA		I2C		1683

GPU THERMAL SENSOR

U9390 MAX6690MEE QSOP

GPU DVI & DACs

SYNC_MASTER=FINO-M23 SYNC_DATE=10/07/2005

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INTERNAL LCD

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
TCKP	GPU_TMDS	GPU_TMDS	TCK	1885
TCKM	GPU_TMDS	GPU_TMDS	TCK	1887
TD0P	GPU_TMDS	GPU_TMDS	TD0	1886
TD0M	GPU_TMDS	GPU_TMDS	TD0	1888
TD1P	GPU_TMDS	GPU_TMDS	TD1	1890
TD1M	GPU_TMDS	GPU_TMDS	TD1	1900
TD2P	GPU_TMDS	GPU_TMDS	TD2	1892
TD2M	GPU_TMDS	GPU_TMDS	TD2	1891

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M — R9626 0 NOSTUFF — L9602 90-OHM-SM — R9604 130 1% 1/16W MF-LF 402 — FILTER_4P — TD2M, TD2P

TMDS_D2P — R9627 0 NOSTUFF

TMDS_D1M — R9628 0 NOSTUFF — L9608 90-OHM-SM — R9603 130 1% 1/16W MF-LF 402 — FILTER_4P — TD1M, TD1P

TMDS_D1P — R9629 0 NOSTUFF

TMDS_D0M — R9630 0 NOSTUFF — L9609 90-OHM-SM — R9602 130 1% 1/16W MF-LF 402 — FILTER_4P — TD0M, TD0P

TMDS_D0P — R9631 0 NOSTUFF

TMDS_CKM — R9632 0 NOSTUFF — L9610 90-OHM-SM — R9601 165 1% 1/16W MF-LF 402 — FILTER_4P — TCKM, TCKP

TMDS_CK_TERM — C9600 22PF 5% 50V CERM 402 — R9600 165 1% 1/16W MF-LF 402 — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM

TMDS_CKP — R9633 0 NOSTUFF

=PP3V3_GPU — R9605 2.0K 5% 1/16W MF-LF 402 RES — R9607 2.0K 5% 1/16W MF-LF 402 RES — R9682 0 5% 1/8W MF-LF 805 RES — PP3V3_DDC — C9601 0.01UF 10% 16V CERM 402 CAP — GND

I2C_GPU_TMDS_SCL — R9608 33 5% 1/16W MF-LF 402 RES — I2C_TMDS_SCL

I2C_GPU_TMDS_SDA — R9606 33 5% 1/16W MF-LF 402 RES — I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600
STDOFF-3MMOD4.6MMH-1.35-TH
PCB_STANDOFF

(516S0241) CRITICAL
J9602
53307-3072
CONN_FI30ST_D_SM

PPVCC_TMDS
PP3V3_DDC — VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.25MM
TD0M, TD0P, TD2M, TD2P, I2C_TMDS_SDA
TCKM, TCKP, TD1M, TD1P, I2C_TMDS_SCL
GND
C9616 10UF 10% 16V CERM 1210 CAP
C9615 0.01UF 10% 16V CERM 402 CAP
GND_CHASSIS_TMDS

SDF9601
STDOFF-3MMOD4.6MMH-1.35-TH
PCB_STANDOFF

PANEL POWER SEQUENCING

=PP12V_GPU — Q9600 IRF7416BF SO1 NOSTUFF — TRA_IRF7416

=PP12V_GPU — R9634 0 5% 1/4W MF-LF 1206

C9619 0.01UF 20% 16V CERM 402 CAP NOSTUFF

R9625 100K 5% 1/16W MF-LF 402 RES NOSTUFF

376S0385

C9618 0.022UF 20% 16V CERM 402 CAP NOSTUFF

FPD_PWR_SW_G

R9613 100K 5% 1/16W MF-LF 402 RES NOSTUFF

FPD_PWR_ON_D

Q9601 2N7002 SOT23-LF NOSTUFF — TRA_2N7002

FPD_PWR_ON

TMDS_EN_R — R9614 10K 5% 1/16W MF-LF 402 RES

TMDS_EN

DZ9600 MMBZ5227B SOT23 ZENER

D9614 MMBD914XXG SOT23 DIODE

C9617 10UF 10% 16V CERM 1210 CAP

PPVCC_TMDS — VOLTAGE=12V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

R9660 10K 5% 1/16W MF-LF 402 RES NOSTUFF

U9670 74LC125 TSSOP

FPD_PWR_ON — LED5900_PWR

R9612 820 5% 1/10W MF-LF 603 RES — LED5900_P1

LED9600 GREEN-3.6MCD 2.0X1.25MM-SM LED

SILKSCREEN: 3

=PP12V_GPU — R9690 300 5% 1/8W MF-LF 805 RES — R9691 300 5% 1/8W MF-LF 805 RES

Q9690_D — Q9690 2N7002 SOT23-LF — TRA_2N7002

SYS_POWERUP_L_BUF

FOR PANEL VCC FALL TIME SPEC

EXTERNAL VGA CONNECTOR

	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
FILT_ANALOG_GRN	GPU_VGA	GPU_VGA	1955
ANALOG_GRN_LC	GPU_VGA	GPU_VGA	1835
ANALOG_GRN_LCL	GPU_VGA	GPU_VGA	1836
FILT_ANALOG_RED	GPU_VGA	GPU_VGA	1956
ANALOG_RED_LC	GPU_VGA	GPU_VGA	1837
ANALOG_RED_LCL	GPU_VGA	GPU_VGA	1838
FILT_ANALOG_BLU	GPU_VGA	GPU_VGA	1957
ANALOG_BLU_LC	GPU_VGA	GPU_VGA	1839
ANALOG_BLU_LCL	GPU_VGA	GPU_VGA	1840
VGA_VSYNC	GPU_VGA	GPU_VGA	1958
VGA_VSYNC_R	GPU_VGA	GPU_VGA	1959
VGA_HSYNC	GPU_VGA	GPU_VGA	1961
VGA_HSYNC_R	GPU_VGA	GPU_VGA	1960

PP5V_USB2 — R9680 0 5% 1/8W MF-LF 805 RES — PP5V_VGA, VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM

C9602 0.01UF 10% 16V CERM 402 CAP

GND_CHASSIS_VGA

TABLE_5_HEAD

TABLE_5_ITEM
152S0316 3 INDUCTOR, 47NH, 0.20 OHM FL9600,FL9601,FL9602

=PP3V3_GPU

ANALOG_VSYNC — U9670 74LC125 TSSOP — VGA_VSYNC — R9671 33 5% 1/16W MF-LF 402 RES — VGA_VSYNC_R

C9670 0.1UF 20% 10V CERM 402 CAP

ANALOG_HSYNC — U9670 74LC125 TSSOP — VGA_HSYNC — R9672 33 5% 1/16W MF-LF 402 RES — VGA_HSYNC_R

C9607 22PF 5% 50V CERM 402 CAP NOSTUFF

C9608 22PF 5% 50V CERM 402 CAP NOSTUFF

GND_CHASSIS_VGA

=PP3V3_GPU — R9673 10K 5% 1/16W MF-LF 402 RES — R9674 10K 5% 1/16W MF-LF 402 RES

I2C_GPU_MON_SCL — Q9675 2N7002DW-X-F SOT363 — I2C_MON_SCL — R9675 100 5% 1/16W MF-LF 402 RES — I2C_MON_SCL_R

I2C_GPU_MON_SDA — Q9675 2N7002DW-X-F SOT363 — I2C_MON_SDA — R9676 100 5% 1/16W MF-LF 402 RES — I2C_MON_SDA_R

PP5V_VGA — R9677 4.7K 5% 1/16W MF-LF 402 RES — R9678 4.7K 5% 1/16W MF-LF 402 RES

C9677 47PF 5% 50V CERM 402 CAP

C9678 47PF 5% 50V CERM 402 CAP

GND_CHASSIS_VGA

INDUCTORS SHOULD BE 47 NH
ANY ~8PF CAP SHOULD DO

OMIT FL9600

ANALOG_RED — R9640 0 5% 1/8W MF-LF 805 RES — ANALOG_RED_LC — C9640 75 1% 1/16W MF-LF 402 RES — GND

L9641 47NH-0.20-OHM IND 0805 — FILTER_LC — R9640 0 NOSTUFF — ANALOG_RED_LCL

R9643 8.2PF +/-0.25PF 50V CERM 402 CAP

OMIT FL9601

ANALOG_GRN — R9642 0 5% 1/8W MF-LF 805 RES — ANALOG_GRN_LC — C9643 75 1% 1/16W MF-LF 402 RES — GND

L9643 47NH-0.20-OHM IND 0805 — FILTER_LC — R9641 0 NOSTUFF — ANALOG_GRN_LCL

R9644 8.2PF +/-0.25PF 50V CERM 402 CAP

OMIT FL9602

ANALOG_BLU — R9644 0 5% 1/8W MF-LF 805 RES — ANALOG_BLU_LC — C9644 75 1% 1/16W MF-LF 402 RES — GND

L9645 47NH-0.20-OHM IND 0805 — FILTER_LC — R9642 0 NOSTUFF — ANALOG_BLU_LCL

R9645 0.2PF +/-0.25PF 50V CERM 402 CAP

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M33: 514S0097

CRITICAL
J9603
DV01793-M33-4F
F-ST-SM
CON_F14ST_D2MT_SM1

GND_CHASSIS_RIGHT

VGA_HSYNC_R
FILT_ANALOG_RED
FILT_ANALOG_GRN
FILT_ANALOG_BLU
I2C_MON_SCL_R
MON_DETECT

VGA_VSYNC_R
(RED_RTN)
(GRN_RTN)
PP5V_VGA
I2C_MON_SDA_R
(BLU_RTN)

C9605 0.01UF 10% 16V CERM 402 CAP
C9604 0.01UF 10% 16V CERM 402 CAP
C9603 0.01UF 10% 16V CERM 402 CAP

GND_CHASSIS_VGA

TMDS / ExtVGA

SYNC_MASTER=M33-DD SYNC_DATE=06/20/2005

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KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E CONST

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

051-6863 H

97 154 8

APPLE_DSIZEPAGE

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)

=PPVCORE_PWRON_NB_HT 7 98

C9806 CAP 1UF 10% 6.3V CERM 402
C9807 CAP 1UF 10% 6.3V CERM 402
C9808 CAP 1UF 10% 6.3V CERM 402
C9809 CAP 1UF 10% 6.3V CERM 402
C9810 CAP 1UF 10% 6.3V CERM 402
C9811 CAP 1UF 10% 6.3V CERM 402
C9812 CAP 1UF 10% 6.3V CERM 402
C9813 CAP 1UF 10% 6.3V CERM 402
C9814 CAP 1UF 10% 6.3V CERM 402
C9815 CAP 1UF 10% 6.3V CERM 402

GND

PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT

98 7 =PPVCORE_PWRON_NB_HT — C9834 0.1UF CAP 20% 10V CERM 402 — =PP1V2_PWRON_HT_NBTX 7 98

98 7 =PP2V5_PWRON_NB_HT — L9800 0.22UH IND 0805-1 — PWR_HT_AVDD

C9800 0.01UF CAP 10% 10V CERM 402
C9801 10UF CAP 10% 6.3V X5R 805
C9802 1UF CAP 10% 6.3V CERM 402

GND

101 98 6 KOD_L15_GND (THIS PAGE)

98 7 =PPVCORE_PWRON_NB_HT

PP9808 P4MM SM PROBEPOINT — HTM2NC0- — KODIAK — K15
PP9809 P4MM SM PROBEPOINT — HTM2NC0+

98 7 =PP1V2_PWRON_HT_NBTX

101 HT_MB_TO_NB_CLK_N<0> ARROW E25
101 HT_MB_TO_NB_CLK_P<0> ARROW D25
101 HT_MB_TO_NB_CTL_N<0> ARROW J27
101 HT_MB_TO_NB_CTL_P<0> ARROW K27

PP9800 P4MM SM PROBEPOINT — MHT0-
PP9801 P4MM SM PROBEPOINT — MHT0+

101 HT_MB_TO_NB_CAD_N<0> ARROW F26
101 HT_MB_TO_NB_CAD_P<0> ARROW F27
101 HT_MB_TO_NB_CAD_N<1> ARROW F25
101 HT_MB_TO_NB_CAD_P<1> ARROW F24
101 HT_MB_TO_NB_CAD_N<2> ARROW A25
101 HT_MB_TO_NB_CAD_P<2> ARROW B25
101 HT_MB_TO_NB_CAD_N<3> ARROW G25
101 HT_MB_TO_NB_CAD_P<3> ARROW H25
101 HT_MB_TO_NB_CAD_N<4> ARROW L25
101 HT_MB_TO_NB_CAD_P<4> ARROW K25
101 HT_MB_TO_NB_CAD_N<5> ARROW G27
101 HT_MB_TO_NB_CAD_P<5> ARROW H27
101 HT_MB_TO_NB_CAD_N<6> ARROW J25
101 HT_MB_TO_NB_CAD_P<6> ARROW J26
101 HT_MB_TO_NB_CAD_N<7> ARROW C26
101 HT_MB_TO_NB_CAD_P<7> ARROW C27

KODIAK HT RECEIVE CLOCKS

PP9802 P4MM SM PROBEPOINT — MHT1-
PP9803 P4MM SM PROBEPOINT — MHT1+

R9806 8.2K RES 1/16W MF-LF 402

101 HT_MB_TO_NB_CLK_N<1> ARROW F22
101 HT_MB_TO_NB_CLK_P<1> ARROW F23

9 HT_MB_TO_NB_CTL_N<1> ARROW E21
9 HT_MB_TO_NB_CTL_P<1> ARROW D21

R9807 8.2K RES 1/16W MF-LF 402 — GND

101 HT_MB_TO_NB_CAD_N<8> ARROW E23
101 HT_MB_TO_NB_CAD_P<8> ARROW D23
101 HT_MB_TO_NB_CAD_N<9> ARROW A23
101 HT_MB_TO_NB_CAD_P<9> ARROW B23
101 HT_MB_TO_NB_CAD_N<10> ARROW H23
101 HT_MB_TO_NB_CAD_P<10> ARROW G23
101 HT_MB_TO_NB_CAD_N<11> ARROW C22
101 HT_MB_TO_NB_CAD_P<11> ARROW C23
101 HT_MB_TO_NB_CAD_N<12> ARROW K23
101 HT_MB_TO_NB_CAD_P<12> ARROW L23
101 HT_MB_TO_NB_CAD_N<13> ARROW J23
101 HT_MB_TO_NB_CAD_P<13> ARROW J24
101 HT_MB_TO_NB_CAD_N<14> ARROW A21
101 HT_MB_TO_NB_CAD_P<14> ARROW B21
101 HT_MB_TO_NB_CAD_N<15> ARROW C24
101 HT_MB_TO_NB_CAD_P<15> ARROW C25

KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)

101 26 HT_NB_REFCLK_P<0>

R9802 20.5 RES 1/16W MF-LF 402 — HT_NB_REFCLK_P<0>
R9803 29.4 RES 1/16W MF-LF 402 — HT_NB_REFCLK_N<0>
R9804 29.4 RES 1/16W MF-LF 402 — HT_NB_G
R9805 20.5 RES 1/16W MF-LF 402

C9837 0.01UF CAP 10% 16V CERM 402
C9838 0.01UF CAP 10% 16V CERM 402
NOSTUFF C9836 0.01UF CAP 10% 16V CERM 402 — GND

R9800 100 RES 1/16W MF-LF 402 — HT_KOD_PVTREF0 K19
R9801 200 RES 1/16W MF-LF 402 — HT_KOD_PVTREF1 L19
HT_KOD_PVTREF2_ALT L17
HT_KOD_PVTREF3_ALT K17

ARROW J16
ARROW J15

101 9 HT_NB_REFCLK_PF<0>
101 9 HT_NB_REFCLK_NF<0>

PP9804 P4MM SM PROBEPOINT — HREF0-
PP9805 P4MM SM PROBEPOINT — HREF0+

KODIAK HT REFCLK

(200MHZ)

L15
101 98 6 KOD_L15_GND (THIS PAGE)
XW9800 SHORT SM
GND

101 26 HT_NB_REFCLK_N<0>

KODIAK CORES

PP9806 P4MM SM PROBEPOINT — 1.6V — Q63 = PP1V6
PP9807 P4MM SM PROBEPOINT — 1.2V — Q63 = PP1V2

=PP1V2_PWRON_HT_NBTX 7 98

A24 B22 B26 D24 E22 E26 G24 H26 K24 L22
A16 A20 B14 B18 D16 D20 E18 G16 G20 H18 H22 K16 K20 L18 M17 M21 N19

U1900
KODIAK-ASIC-040812
BGA
SEE_TABLE

A14 A18 B16 B20 D18 E16 E20 G18 G22 H16 H20 K18 L16 L20 M16 M20 N18
A22 A26 B24 D22 D26 E24 G26 H24 K22 L24
GND GND

98 7 =PP1V2_PWRON_HT_NBTX

C9817 C9818 C9819 C9820 C9821
C9822 C9823 C9824 C9825 C9826
CAP 1UF 10% 6.3V CERM 402
GND

L9801 0.22UH IND 0805-1 — =PP2V5_PWRON_NB_HT 7 98

101 PWR_HT_AVDD2

C9803 CAP 1UF 10% 6.3V CERM 402
C9804 CAP 10UF 10% 5.3V X5R 805
C9805 CAP 0.01UF 10% 16V CERM 402
GND

KOD_L15_GND 6 98 101 (THIS PAGE)

H15

J19 ARROW HT_NB_TO_MB_CLK_N<0> 101
J20 ARROW HT_NB_TO_MB_CLK_P<0> 101
J22 ARROW HT_NB_TO_MB_CTL_N<0> 101
J21 ARROW HT_NB_TO_MB_CTL_P<0> 101
F16 ARROW HT_NB_TO_MB_CAD_N<0> 101
F17 ARROW HT_NB_TO_MB_CAD_P<0> 101
G17 ARROW HT_NB_TO_MB_CAD_N<1> 101
H17 ARROW HT_NB_TO_MB_CAD_P<1> 101
J18 ARROW HT_NB_TO_MB_CAD_N<2> 101
J17 ARROW HT_NB_TO_MB_CAD_P<2> 101
F18 ARROW HT_NB_TO_MB_CAD_N<3> 101
F19 ARROW HT_NB_TO_MB_CAD_P<3> 101
G19 ARROW HT_NB_TO_MB_CAD_N<4> 101
H19 ARROW HT_NB_TO_MB_CAD_P<4> 101
G21 ARROW HT_NB_TO_MB_CAD_N<5> 101
H21 ARROW HT_NB_TO_MB_CAD_P<5> 101
F21 ARROW HT_NB_TO_MB_CAD_N<6> 101
F20 ARROW HT_NB_TO_MB_CAD_P<6> 101
K21 ARROW HT_NB_TO_MB_CAD_N<7> 101
L21 ARROW HT_NB_TO_MB_CAD_P<7> 101
C16 ARROW HT_NB_TO_MB_CLK_N<1> 101
C17 ARROW HT_NB_TO_MB_CLK_P<1> 101
E15 ARROW 9 HT_NB_TO_MB_CTL_P<1>
D15 ARROW 9 HT_NB_TO_MB_CTL_N<1>
D19 ARROW HT_NB_TO_MB_CAD_N<8> 101
E19 ARROW HT_NB_TO_MB_CAD_P<8> 101
D17 ARROW HT_NB_TO_MB_CAD_N<9> 101
E17 ARROW HT_NB_TO_MB_CAD_P<9> 101
C19 ARROW HT_NB_TO_MB_CAD_N<10> 101
C18 ARROW HT_NB_TO_MB_CAD_P<10> 101
A15 ARROW HT_NB_TO_MB_CAD_N<11> 101
B15 ARROW HT_NB_TO_MB_CAD_P<11> 101
A17 ARROW HT_NB_TO_MB_CAD_N<12> 101
B17 ARROW HT_NB_TO_MB_CAD_P<12> 101
B19 ARROW HT_NB_TO_MB_CAD_N<13> 101
A19 ARROW HT_NB_TO_MB_CAD_P<13> 101
C15 ARROW HT_NB_TO_MB_CAD_N<14> 101
C14 ARROW HT_NB_TO_MB_CAD_P<14> 101
C20 ARROW HT_NB_TO_MB_CAD_N<15> 101
C21 ARROW HT_NB_TO_MB_CAD_P<15> 101

=PP1V2_PWRON_HT_NBTX 7 98
NOSTUFF R9808 8.2K RES 1/16W MF-LF 402
NOSTUFF R9809 8.2K RES 1/16W MF-LF 402
GND

=PP2V5_PWRON_HT 7 103
R9810 1K RES 1/16W MF-LF 402
R9811 1K RES 1/16W MF-LF 402
R9812 1K RES 5% 1/16W MF-LF 402
R9813 1K RES 1/16W MF-LF 402

AF06 ARROW HT_LDTSTOP_L 103
AF09 ARROW HT_LDTREQ_L 103
AF03 ARROW HT_PWROK 103
AE11 ARROW HT_LDTRESET_L 103

KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)

98 7 =PP1V2_PWRON_HT_NBTX

C9827 C9828 C9829 C9830 C9831
C9832 C9833 C9839 C9840 C9841
C9842 C9843 C9844 C9845 C9846
C9847 CAP 1UF 10% 6.3V CERM 402
CAP 1UF 10% 6.3V CERM 402
GND

KODIAK HT16

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:24:02 2006

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APPLE_DSIZEPAGE DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	
HT_NB_TO_SB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_N<0>
HT_NB_TO_SB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK	HT_MB_TO_SB_CLK_P<0>
HT_NB_TO_SB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<0>
HT_NB_TO_SB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<0>
HT_NB_TO_SB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<1>
HT_NB_TO_SB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<1>
HT_NB_TO_SB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<2>
HT_NB_TO_SB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<2>
HT_NB_TO_SB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<3>
HT_NB_TO_SB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<3>
HT_NB_TO_SB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<4>
HT_NB_TO_SB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<4>
HT_NB_TO_SB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<5>
HT_NB_TO_SB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<5>
HT_NB_TO_SB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<6>
HT_NB_TO_SB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<6>
HT_NB_TO_SB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_N<7>
HT_NB_TO_SB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CAD_P<7>
HT_NB_TO_SB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_N<0>
HT_NB_TO_SB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD	HT_MB_TO_SB_CTL_P<0>
HT_SB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_N<0>
HT_SB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK	HT_SB_TO_MB_CLK_P<0>
HT_SB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<0>
HT_SB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<0>
HT_SB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<1>
HT_SB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<1>
HT_SB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<2>
HT_SB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<2>
HT_SB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<3>
HT_SB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<3>
HT_SB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<4>
HT_SB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<4>
HT_SB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<5>
HT_SB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<5>
HT_SB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<6>
HT_SB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<6>
HT_SB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_N<7>
HT_SB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CAD_P<7>
HT_SB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_N<0>
HT_SB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD	HT_SB_TO_MB_CTL_P<0>
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE					HT_MB_TO_NB_CAD_P<8..15>
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE					HT_MB_TO_NB_CAD_N<8..15>
TP_HT_MB_TO_NB_CLK_N<1>	TRUE					HT_MB_TO_NB_CLK_N<1>
TP_HT_MB_TO_NB_CLK_P<1>	TRUE					HT_MB_TO_NB_CLK_P<1>
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE					HT_NB_TO_MB_CAD_P<8..15>
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE					HT_NB_TO_MB_CAD_N<8..15>
NC_HT_NB_TO_MB_CLK_N<1>	TRUE					HT_NB_TO_MB_CLK_N<1>
NC_HT_NB_TO_MB_CLK_P<1>	TRUE					HT_NB_TO_MB_CLK_P<1>
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK	IN
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK	IN
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK	IN
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK	IN
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK	IN

I97

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE	
PWR_HT_AVDD	0.4MM	0.2MM	2.5	IN
PWR_HT_AVDD2	0.4MM	0.2MM	2.5	IN
KOD_L15_GND	0.4MM	0.2MM	0	IN
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0	IN

HT ALIASES

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APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	HT_CLK66M_SB_C
HT_CLK66M_SB	0.38mm SPACING	HT_CLK66M_SB
	P3MM SPACING	HT_LDTRESET_L

Page Notes

Power aliases required by this page:

=PP2V5_PWRON_HT

=PP1V2_PWRON_HT

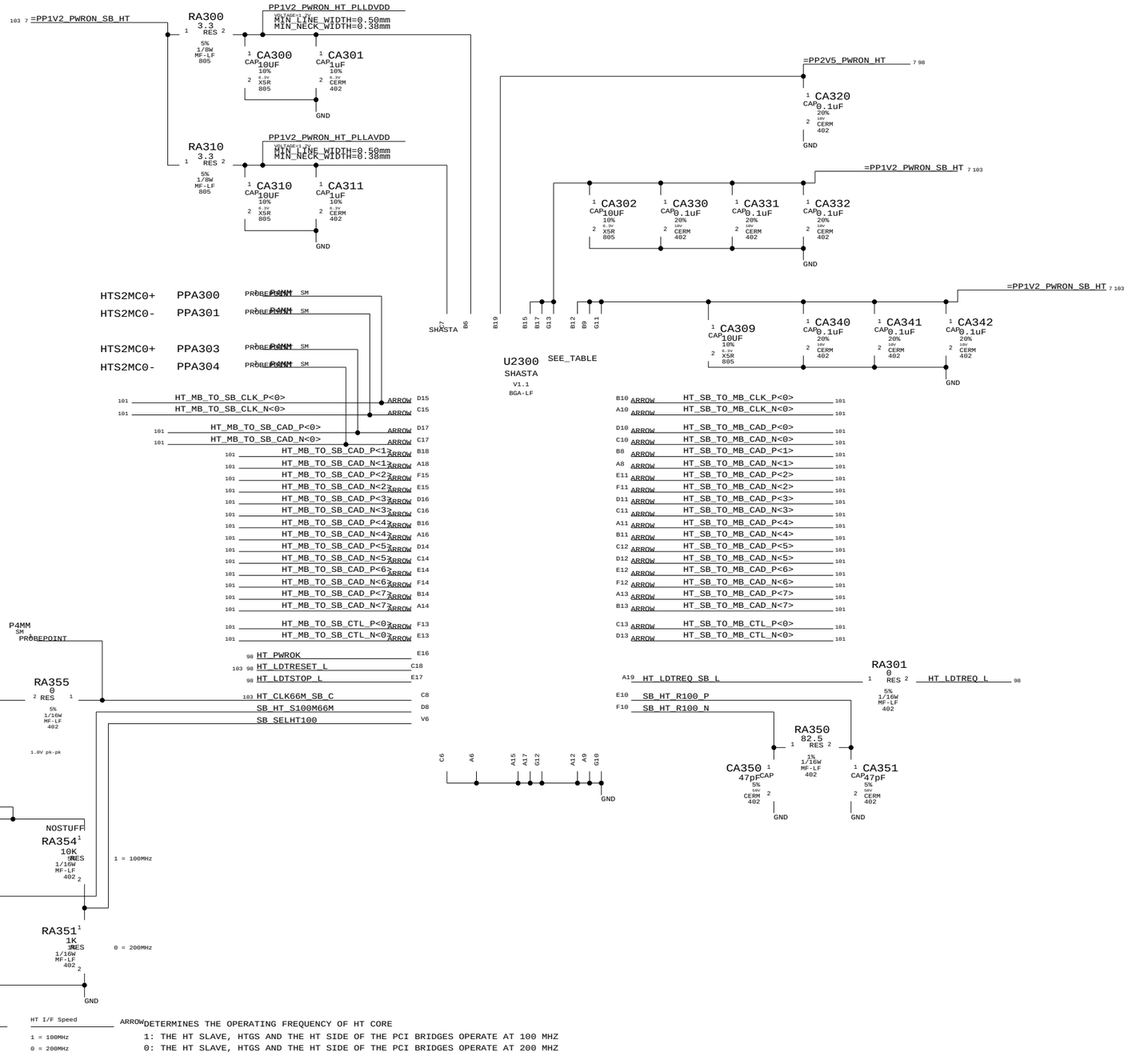
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

- SB_HT_200M

  Stuffs resistor to select 200MHz HT I/F.



Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:22:05 2006

DRAWING

APPLE_DSIZEPAGE

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	RPAR4P 47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	RPAR4P 47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	RPAR4P 47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	RPAR4P 47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	RPAR4P 47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	RPAR4P 47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	RPAR4P 47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	RPAR4P 47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	RPAR4P 47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	RPAR4P 47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	RPAR4P 47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	RPAR4P 47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	RPAR4P 47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	RPAR4P 47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	RPAR4P 47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	RPAR4P 47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	RPAR4P 47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>	1	47 RES 5% 1/16W MF-LF 402	2	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	RPAR4P 47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	RPAR4P 47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	RPAR4P 47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	RPAR4P 47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	RPAR4P 47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	RPAR4P 47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	RPAR4P 47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	RPAR4P 47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	RPAR4P 47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>	1	47 RES 5% 1/16W MF-LF 402	2	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	RPAR4P 47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	RPAR4P 47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	RPAR4P 47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	RPAR4P 47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	RPAR4P 47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	RPAR4P 47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	RPAR4P 47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	RPAR4P 47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	RPAR4P 47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	RPAR4P 47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	RPAR4P 47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	RPAR4P 47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	RPAR4P 47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	RPAR4P 47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	PCI_CLK33M_AIRPORT

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

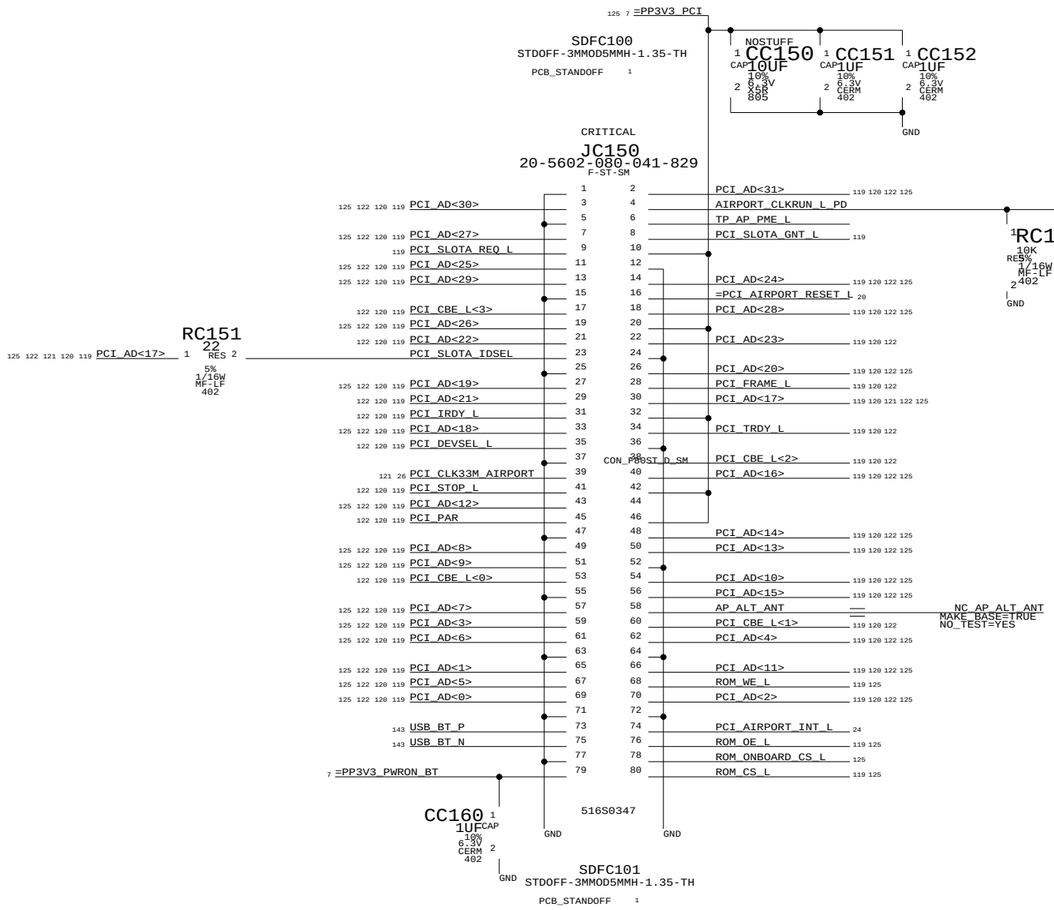
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 — 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122 7 =PPVIO_PCI_USB2

CC201 0.1uF CAP 10V 20% CERM 402 (1, 2)
CC202 0.1uF CAP 10V 20% CERM 402 (1, 2)
CC203 0.1uF CAP 10V 20% CERM 402 (1, 2)
GND

XWC200 SHORT SM (2, 1)
6 PP_VIOPCIUSB2_C2
P4MM SM PROBEPOINT PPC203

UPD720101_FBGA_SPLIT

125 121 120 119 PCI_AD<0>	M5	
125 121 120 119 PCI_AD<1>	P5	
125 121 120 119 PCI_AD<2>	N5	
125 121 120 119 PCI_AD<3>	P4	
125 121 120 119 PCI_AD<4>	N4	
125 121 120 119 PCI_AD<5>	M3	
125 121 120 119 PCI_AD<6>	N3	
125 121 120 119 PCI_AD<7>	M1	
125 121 120 119 PCI_AD<8>	L2	
125 121 120 119 PCI_AD<9>	L1	
125 121 120 119 PCI_AD<10>	K2	
125 121 120 119 PCI_AD<11>	L3	
125 121 120 119 PCI_AD<12>	K1	
125 121 120 119 PCI_AD<13>	K3	
125 121 120 119 PCI_AD<14>	J2	
125 121 120 119 PCI_AD<15>	J1	
125 121 120 119 PCI_AD<16>	F2	
125 121 120 119 PCI_AD<17>	E3	
125 121 120 119 PCI_AD<18>	E1	
125 121 120 119 PCI_AD<19>	D3	
125 121 120 119 PCI_AD<20>	D1	
121 120 119 PCI_AD<21>	D2	
121 120 119 PCI_AD<22>	C2	
121 120 119 PCI_AD<23>	C1	
125 121 120 119 PCI_AD<24>	B4	
125 121 120 119 PCI_AD<25>	A4	
125 121 120 119 PCI_AD<26>	B5	
125 121 120 119 PCI_AD<27>	C4	(PCI_AD<27>)
125 121 120 119 PCI_AD<28>	A5	
125 121 120 119 PCI_AD<29>	C5	
125 121 120 119 PCI_AD<30>	B6	
125 121 120 119 PCI_AD<31>	A6	
121 120 119 PCI_CBE_L<0>	M2	
121 120 119 PCI_CBE_L<1>	J3	
121 120 119 PCI_CBE_L<2>	F1	
121 120 119 PCI_CBE_L<3>	C3	
121 120 119 PCI_PAR	J4	
121 120 119 PCI_FRAME_L	F3	
121 120 119 PCI_IRDY_L	F4	
121 120 119 PCI_TRDY_L	G1	
121 120 119 PCI_STOP_L	G3	
PCI_SLOTG_IDSEL	B3	
121 120 119 PCI_DEVSEL_L	G2	
119 PCI_SLOTG_REQ_L	C6	
119 PCI_SLOTG_GNT_L	D6	
NEC_PERR_L_PU	H2	
NEC_SERR_L_PU	H1	
NEC_INTA_L	C7	OD
NEC_INTB_L	B7	OD
NEC_INTC_L	A7	OD
122 27 =PCI_CLK33M_USB2	A8	
NEC_VBBRST_L	B8	(CHIP RESET)
NEC_CRUN_L_PD	N6	
NEC_PME_L	D9	OD
6 TP_NEC_SMI_L	L6	(PCI RESET) OD
NEC_LEGC_PD	L7	

CRITICAL
UC200
NEC_UPD720101_USB2
FBGA-LF

RC214 22 RES 1/16W MF-LF 402 (1, 2)
RC216 10K RES 1/16W MF-LF 402 (1, 2)
RC213 10K RES 1/16W MF-LF 402 (1, 2)
RC215 4.7K RES 1/16W MF-LF 402 (1, 2)

RPC203 47 RPAR4P 5% 1/16W SM-LF (4, 5)
RPC203 47 RPAR4P 5% 1/16W SM-LF (2, 6)
RPC203 47 RPAR4P 5% 1/16W SM-LF (3, 7)
RPC203 47 RPAR4P 5% 1/16W SM-LF (8, 1)

24 PCI_USB2_INT_L
119 30 28 24 SYS_IO_RESET_L
RC250 47 RES 5% 1/16W MF-LF 402 (1, 2)
28 24 SYS_PME_L
RC251 47 RES 5% 1/16W MF-LF 402 (1, 2)
20 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

GND
P4MM SM PROBEPOINT PPC200
P4MM SM PROBEPOINT PPC201

IPD	M8	TP_NEC_NTEST1 6
IPD	M7	TP_NEC_SMC 6
IPD	N7	TP_NEC_TEB
IPD	P7	TP_NEC_AMC
IPD	L8	TP_NEC_TEST 6
	M10	TP_NEC_NANDTEST
	M9	TP_NEC_SRCLK 6
	N9	TP_NEC_SRDATA
IPD	P9	TP_NEC_SRMOD 6

ALL NETS TO FUNCTIONAL TEST PAGE

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

LAST_MODIFIED=Fri Apr 28 20:22:14 2006
DRAWING

Page Notes

Power aliases required by this page:

- =PP3V3_PCI

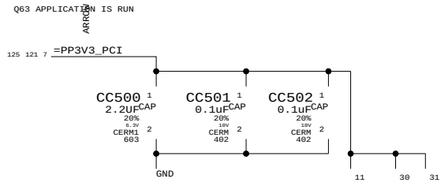
Signal aliases required by this page:

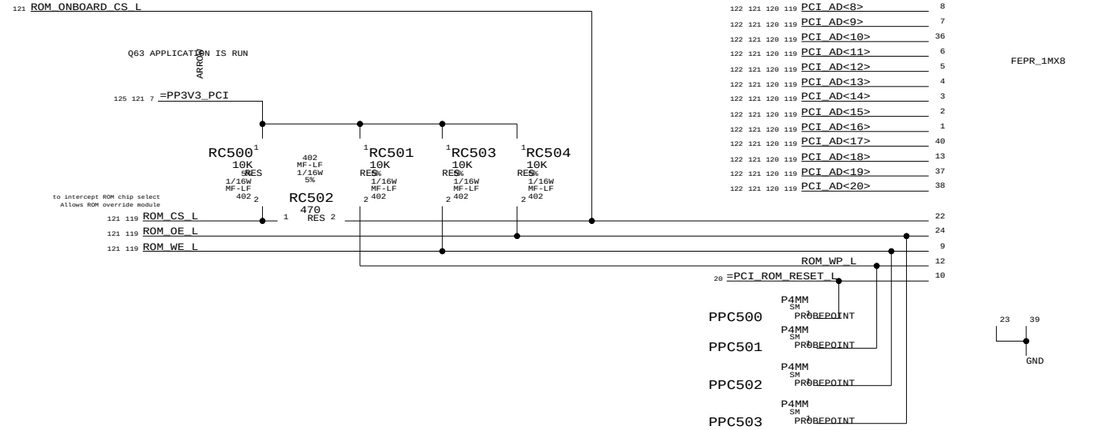
(NONE)

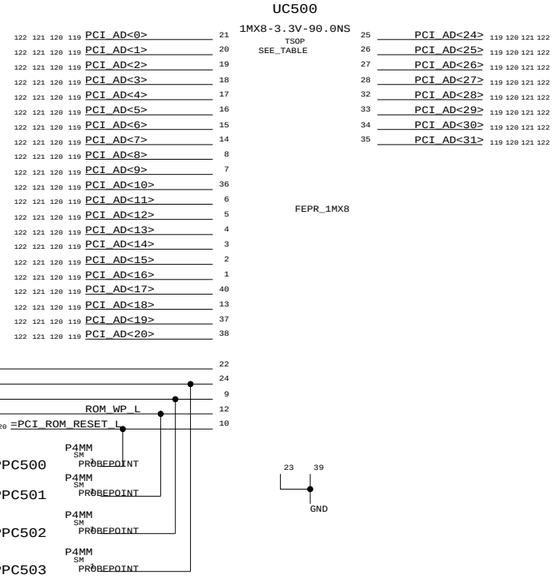
BOM options provided by this page:

(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_X_ITEM symbol to declare U7500 part number.







BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:22:16 2006

DRAWING

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APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
				UATA_DD_R<15..8>
				UATA_DD_R<7>
				UATA_DD_R<6..0>
				UATA_DA_R<2..0>
				UATA_CS0_L_R
				UATA_CS1_L_R
				UATA_DMACK_L_R
				UATA_HSTROBE_R
				UATA_STOP_R
				UATA_RESET_L_R

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

4-29-05

AS OF TODAY THIS PAGE FOR M33 IS NOT SYNC WITH Q63.
RPAK PINS WERE REMAPPED FOR BETTER ROUTING AROUND UATA CONNECTOR.

LAST_MODIFIED=Fri Apr 28 20:22:17 2006

DRAWING

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A FILTER_2P 0805

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
PP1V2_SATA_VDD

CC705 CAP 2.2UF 20% 6.3V CERM1 603
CC700 CAP 0.1uF 20% 10V CERM 402
CC701 CAP 0.1uF 20% 10V CERM 402
CC702 CAP 0.1uF 20% 10V CERM 402
CC703 CAP 0.1uF 20% 10V CERM 402
CC704 CAP 0.1uF 20% 10V CERM 402

GND

XWCC00 → SHASTA AB14, AB17, T14, W15, Y18

SHORT SM → PP_1V2PWRONDISKSB_CC NO_TEST=YES → P4MM SM PROBEPOINT PPCC00

SATA_VDD x 5

U2300 SHASTA V1.1 BGA-LF SEE_TABLE

DSTROBE aka: IORDY/HDMARDY*
HSTROBE aka: DIOR*
STOP aka: DIOW*

UATA_DSTROBE	F9	
UATA_DMARQ	D7	
UATA_INTRQ	C5	
SATA_RXD_P1_C	Y17	
SATA_RXD_N1_C	Y16	
SATA_RXD_P2_C	AB15	
SATA_RXD_N2_C	AA15	

J6	UATA_DD_R<0>	
H7	UATA_DD_R<1>	
H6	UATA_DD_R<2>	
E2	UATA_DD_R<3>	
C1	UATA_DD_R<4>	
C2	UATA_DD_R<5>	
E3	UATA_DD_R<6>	
G6	UATA_DD_R<7>	
G5	UATA_DD_R<8>	
D4	UATA_DD_R<9>	
G7	UATA_DD_R<10>	
F6	UATA_DD_R<11>	
C3	UATA_DD_R<12>	
F5	UATA_DD_R<13>	
E5	UATA_DD_R<14>	
D5	UATA_DD_R<15>	
E6	UATA_DA_R<0>	
C4	UATA_DA_R<1>	
D6	UATA_DA_R<2>	
B3	UATA_CS0_L_R	
B4	UATA_CS1_L_R	
E8	UATA_DMACK_L_R	
E4	UATA_HSTROBE_R	
D3	UATA_STOP_R	
E7	UATA_RESET_L_R	
AA16	SATA_TXD_P1	
AB16	SATA_TXD_N1	
Y15	SATA_TXD_P2	
Y14	SATA_TXD_N2	

AA14, AA17, T13, W16 → GND

P4MM SM PROBEPOINT PPCC01

PLACE UATA TERMINATION RESISTORS NEAR JC901 CONNECTOR

DIOR- :HDMARDY- :HSTROBE >
DIOW- :STOP >

RC706 33 ARROW RES 5% 1/16W MF-LF 402
UATA_RESET_L_R → UATA_RESET_L

RC704 22 ARROW RES 5% 1/16W MF-LF 402
UATA_DMACK_L_R → UATA_DMACK_L

RC702 22 ARROW RES 5% 1/16W MF-LF 402
UATA_HSTROBE_R → UATA_HSTROBE

RC703 22 ARROW RES 5% 1/16W MF-LF 402
UATA_STOP_R → UATA_STOP

RC700 33 ARROW RES 5% 1/16W MF-LF 402
UATA_CS0_L_R → UATA_CS0_L

RC701 33 ARROW RES 5% 1/16W MF-LF 402
UATA_CS1_L_R → UATA_CS1_L

SPARE
RPC704 33 RPAR4P 5% 1/16W SM-LF

RPC704 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DA_R<0> → UATA_DA<0>

RPC704 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DA_R<1> → UATA_DA<1>

RPC704 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DA_R<2> → UATA_DA<2>

RPC700 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<0> → UATA_DD<0>

RPC700 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<1> → UATA_DD<1>

RPC700 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<2> → UATA_DD<2>

RPC700 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<3> → UATA_DD<3>

RPC701 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<4> → UATA_DD<4>

RPC701 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<5> → UATA_DD<5>

RPC701 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<6> → UATA_DD<6>

RPC701 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<7> → UATA_DD<7>

RPC702 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<8> → UATA_DD<8>

RPC702 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<9> → UATA_DD<9>

RPC702 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<10> → UATA_DD<10>

RPC702 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<11> → UATA_DD<11>

RPC703 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<12> → UATA_DD<12>

RPC703 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<13> → UATA_DD<13>

RPC703 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<14> → UATA_DD<14>

RPC703 33 ARROW RPAR4P 5% 1/16W SM-LF
UATA_DD_R<15> → UATA_DD<15>

RC705 10K RES 1/16W MF-LF 402 → GND

Shasta Disk

SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

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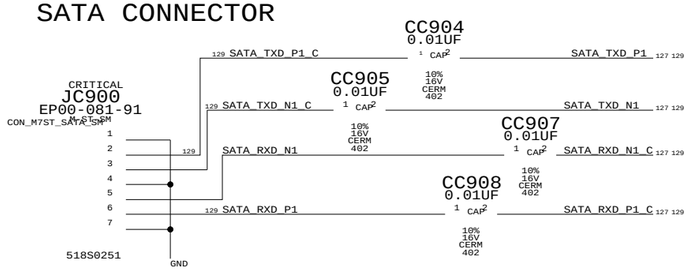
APPLE_DSIZEPAGE

SATA CONNECTOR

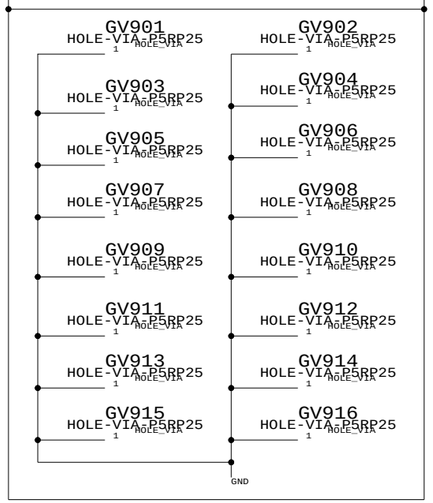


SATA PORT1 IS NOT USED IN M23/M33:NO TEST

SATA_TXD_P2	NC_SATA_TXD_P2	MAKE_BASE=TRUE
SATA_TXD_N2	NC_SATA_TXD_N2	MAKE_BASE=TRUE
SATA_RXD_N2_C	NC_SATA_RXD_N2_C	MAKE_BASE=TRUE
SATA_RXD_P2_C	NC_SATA_RXD_P2_C	MAKE_BASE=TRUE

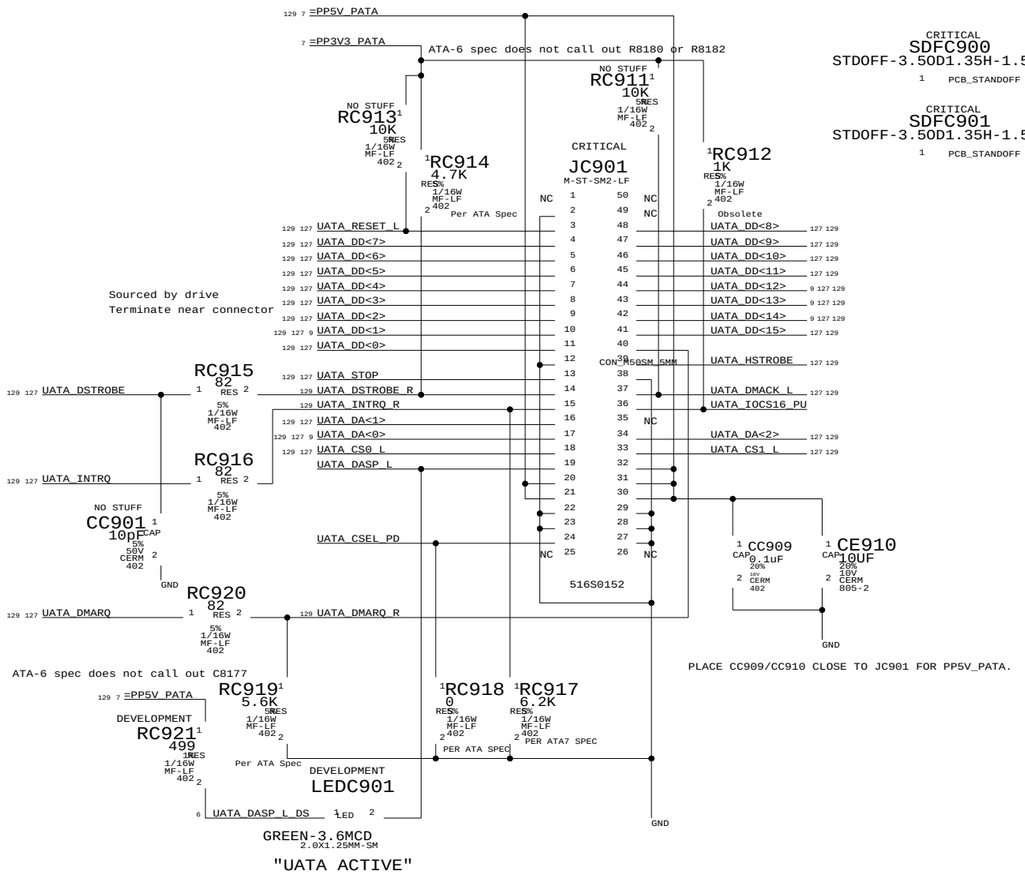
SATA & USB DIFF PAIR GND VIAS

ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA APPROXIMATELY 0.152MM AWAY FROM SIGNAL VIA.



M33 PATA CONNECTOR

4-12-05



	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM RPAKS TO JC901

UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		1392
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		1393
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		1394
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		1395
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		1396
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		1397
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		1398
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		1399
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		1400
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		1401
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		1402
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		1403
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		1404

UATA FROM SHASTA U2300 TO RPAKS

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05

NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.

UPDATED AC COUPLING CAPS FOR SATA JC900.

ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M33-DC SYNC_DATE=06/20/2005

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APPLE_DSIZEPAGE

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I58	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

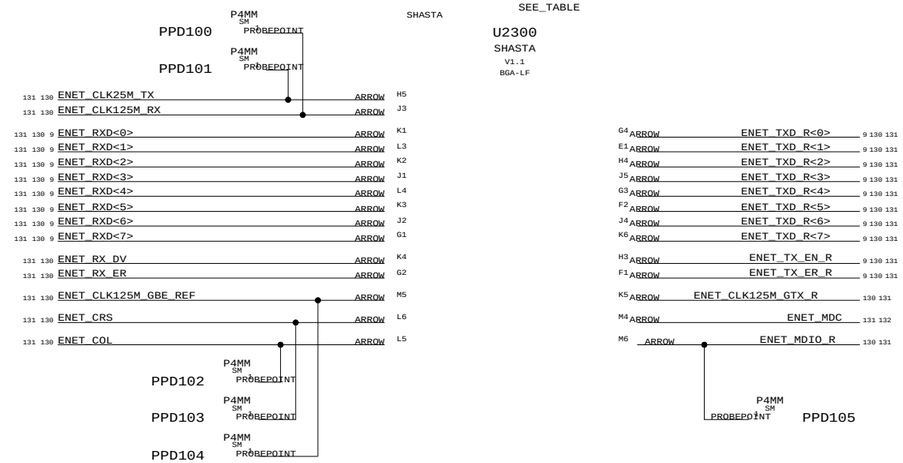
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
1x1	0.38mm SPACING	ENET_CLK25M_TX
1x2	0.38mm SPACING	ENET_CLK125M_RX
1x3	0.38mm SPACING	ENET_CLK125M_GBE_REF
1x4	0.38mm SPACING	ENET_CLK125M_GTX
1x5	0.38mm SPACING	ENET_CLK125M_GTX_R
2x1	ENET_FW_2X	ENET_RXD_R<7..0>
2x2	ENET_FW_3X	ENET_RX_DV_R
2x3	ENET_FW_3X	ENET_RX_ER_R
3x1	ENET_FW_2X	ENET_RXD<7..0>
3x2	ENET_FW_3X	ENET_RX_DV
3x3	ENET_FW_3X	ENET_RX_ER
4x1	ENET_FW_2X	ENET_TXD_R<7..0>
4x2	ENET_FW_3X	ENET_TX_EN_R
4x3	ENET_FW_3X	ENET_TX_ER_R
5x1	ENET_FW_2X	ENET_TXD<7..0>
5x2	ENET_FW_3X	ENET_TX_EN
5x3	ENET_FW_3X	ENET_TX_ER
6x2	ENET_FW_3X	ENET_CRS_R
6x3	ENET_FW_3X	ENET_COL_R
7x1	ENET_FW_3X	ENET_CRS
7x2	ENET_FW_3X	ENET_COL
8x1	ENET_FW_3X	ENET_MDC
8x2	ENET_FW_3X	ENET_MDIO
8x3	ENET_FW_3X	ENET_MDIO_R
8x4	ENET_FW_3X	R8405_1
8x5	ENET_FW_3X	R8405_2
8x6	ENET_FW_3X	R8407_2

Page Notes

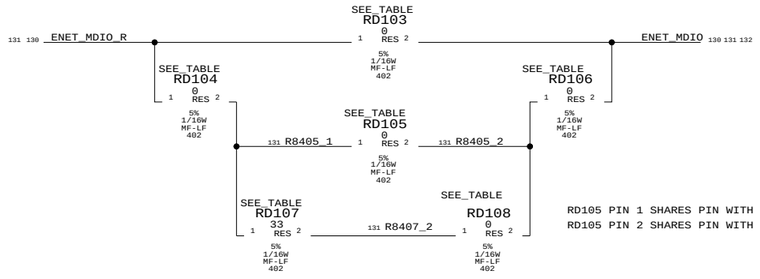
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

TABLE_6_HEAD

TABLE_6_ITEM
116S0004 1 RES,0-OHM,402,5% RD103 ENET_MDIO_DELAY_0 *

TABLE_6_ITEM
116S0004 3 RES,0-OHM,402,5% RD104,RD105,RD106 ENET_MDIO_DELAY_2NS

TABLE_6_ITEM
116S0004 3 RES,0-OHM,402,5% RD104,RD108,RD106 ENET_MDIO_DELAY_4NS

TABLE_6_ITEM
116S0030 1 RES,33-OHM,402,5% RD107 ENET_MDIO_DELAY_4NS

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Tue Nov 15 18:31:13 2005
DRAWING

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APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
A14	0.38mm SPACING	
A15	0.38mm SPACING	
A16	0.38mm SPACING	
A17	ENET	ENET_MDI0
A18	ENET	ENET_MDI0
A19	ENET	ENET_MDI1
A20	ENET	ENET_MDI1
A21	ENET	ENET_MDI2
A22	ENET	ENET_MDI2
A23	ENET	ENET_MDI3
A24	ENET	ENET_MDI3
B25	0.38mm SPACING	
B26	0.38mm SPACING	
B27	0.38mm SPACING	

ENET_CLK125M_GBE_REF_R 130 132
ENET_CLK125M_RX_R 130 132
ENET_CLK25M_TX_R 130 132
ENET_MDI_P<0> 132 136
ENET_MDI_N<0> 132 136
ENET_MDI_P<1> 132 136
ENET_MDI_N<1> 132 136
ENET_MDI_P<2> 132 136
ENET_MDI_N<2> 132 136
ENET_MDI_P<3> 132 136
ENET_MDI_N<3> 132 136
VESTA_CLK25M_XTALI 132
VESTA_CLK25M_XTALO 132
VESTA_CLK25M_XTALO_R 132

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL ARROW

139 17 7 =PP3V3_ENETFW

RD204 2 1K 1% RES 1/10W MF-LF 402 1

3 QD200 2N7002DW-X-F SOT-363 TRA_2N7002DW

136 132 7 =PP3V3_ENET 5

4 GND

1 CD206 CAP 1UF 10% 6.3V CERM 402 2 GND

6 QD200 2N7002DW-X-F SOT-363 TRA_2N7002DW

1 GND

17 VESTA_RESET_H 2

Q63 APPLICATION IS ALL ARROW

139 17 7 =PP2V5_ENETFW

LD200 FERR-EMI-600-OHM IND SM 1 2

PP2V5_VESTA_BIASVDD1 6
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm

CD201 CAP 0.1uF 20% 10V CERM 402 1 2 GND

PP2V5_VESTA_XTALVDD1 6
VOLTAGE=2.5V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm

LD201 FERR-EMI-600-OHM IND SM 1 2

CD202 CAP 10UF 10% 6.3V X5R 805 1 2 GND

CD203 CAP 0.001uF 20% 50V CERM 402 1 2 GND

XWD200 SHORT 2 1 OMIT SM TP_VESTA_BIASVDD1 PROBEPOINT P4MM SM PPD239

XWD201 SHORT 2 1 OMIT SM TP_VESTA_XTALVDD1 PROBEPOINT P4MM SM PPD201

XWD202 SHORT 2 1 OMIT SM TP_VESTA_PLLVDD1 PROBEPOINT P4MM SM PPD238

BCM5462A3 M1 P1 M1

6 PP1V2_VESTA_PLLVDD1
VOLTAGE=1.2V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm

CD204 1 0.001uF CAP 20% 50V CERM 402 2

CD205 1 10UF CAP 10% 6.3V X5R 805 2 GND

Q63 APPLICATION IS ALL ARROW

LD202 FERR-EMI-600-OHM IND SM 1 2

7 17 139 =PP1V2_ENETFW

VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms

P4MM SM PROBEPOINT PPD200

131 130 ENET_CLK125M_GTX ARROW A4 IPD

SEE_TABLE

U1701
VESTA-V1.3
FBGA-200-LF

131 130 9	ENET_TXD<0>	ARROW	B6	IPD
131 130 9	ENET_TXD<1>	ARROW	C6	IPD
131 130 9	ENET_TXD<2>	ARROW	C7	IPD
131 130 9	ENET_TXD<3>	ARROW	D6	IPD
131 130 9	ENET_TXD<4>	ARROW	E6	IPD
131 130 9	ENET_TXD<5>	ARROW	C5	IPD
131 130 9	ENET_TXD<6>	ARROW	B5	IPD
131 130 9	ENET_TXD<7>	ARROW	A5	IPD
131 130 9	ENET_TX_EN	ARROW	B4	IPD
131 130 9	ENET_TX_ER	ARROW	C4	IPD
131	ENET_MDC	ARROW	G1	IPD
131 130	ENET_MDIO	ARROW	G2	IPU
	VESTA_ENET_LOWPWR		H5	IPD

IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

D1	ARROW	ENET_CLK125M_GBE_REF_R	130 132	
A6	ARROW	ENET_CLK25M_TX_R	130 132	
C1	ARROW	ENET_CLK125M_RX_R	130 132	
F4	ARROW	ENET_RXD_R<0>	9 130 131	
F5	ARROW	ENET_RXD_R<1>	9 130 131	
E5	ARROW	ENET_RXD_R<2>	9 130 131	
E4	ARROW	ENET_RXD_R<3>	9 130 131	
E3	ARROW	ENET_RXD_R<4>	9 130 131	
D5	ARROW	ENET_RXD_R<5>	9 130 131	
D4	ARROW	ENET_RXD_R<6>	9 130 131	
D3	ARROW	ENET_RXD_R<7>	9 130 131	
D2	ARROW	ENET_RX_DV_R	130 131	
C2	ARROW	ENET_RX_ER_R	130 131	
F3	ARROW	ENET_COL_R	130 131	
G3	ARROW	ENET_CRS_R	130 131	
A3	ARROW	TP_VESTA_RBC0	9	
B3	ARROW	TP_VESTA_RBC1	9	
R4	ARROW	ENET_MDI_P<0>	132 136	
R5	ARROW	ENET_MDI_N<0>	132 136	
R7	ARROW	ENET_MDI_P<1>	132 136	
R6	ARROW	ENET_MDI_N<1>	132 136	
R8	ARROW	ENET_MDI_P<2>	132 136	
R9	ARROW	ENET_MDI_N<2>	132 136	
R11	ARROW	ENET_MDI_P<3>	132 136	
R10	ARROW	ENET_MDI_N<3>	132 136	
D10	ENET_ENERGYDET		24	
C10	TP_VESTA_AN_EN		9	
A8	TP_VESTA_TXC_RXC_DELAY		9	
A10	TP_VESTA_LINK1_L		9	
B11	TP_VESTA_LINK2_L		9	
B10	TP_VESTA_FDXLED_L		9	
B12	TP_VESTA_XMTLED_L		136	
A11	TP_VESTA_ACTLED_L		136	

TERMINATION OFF PAGE

9	TP_VESTA_PHYA<0>		L5	IPD
9	TP_VESTA_PHYA<1>		L4	IPD
9	TP_VESTA_PHYA<2>		L3	IPD
9	TP_VESTA_PHYA<3>		L2	IPD
9	TP_VESTA_PHYA<4>		L1	IPD
9	TP_VESTA_EN_10B		K3	IPD
9	TP_VESTA_RGMIIEN		B8	IPU
9	TP_VESTA_FDX		C8	IPU
9	TP_VESTA_F1000		K4	IPD
9	TP_VESTA_SPD0		K5	IPD
9	TP_VESTA_MANMS		D9	IPD
9	TP_VESTA_HUB		A9	IPU
9	TP_VESTA_ER		H3	IPD
9	TP_VESTA_TEST<0>		M4	IPD
9	TP_VESTA_TEST<1>		M5	IPD
9	TP_VESTA_TVCO		N3	IPD
132	VESTA_CLK25M_XTALI		N2	
132	VESTA_CLK25M_XTALO_R		P2	

Put crystal circuit close to PHY

RD209 0 5% RES 1/16W MF-LF 402 2 1

CRITICAL YD200 25.0000M CRYSTAL 8X4.5MM-SM2 1 2

VESTA_CLK25M_XTALO 132

CD218 1 33pF CAP 5% 50V CERM 402 2 GND

CD219 1 33pF CAP 5% 50V CERM 402 2 GND

CRYSTAL LOAD CAPACITANCE IS 20PF

P3 R2 M2

RD213 1 1.24K 1% RES 1/16W MF-LF 402 2 GND

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:22:22 2006
DRAWING

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APPLE_DSIZEPAGE

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

P25	ENET	ENET_MDI_P<0>	132 136
P24	ENET	ENET_MDI_N<0>	132 136
P27	ENET	ENET_MDI_P<1>	132 136
P26	ENET	ENET_MDI_N<1>	132 136
P29	ENET	ENET_MDI_P<2>	132 136
P28	ENET	ENET_MDI_N<2>	132 136
P31	ENET	ENET_MDI_P<3>	132 136
P30	ENET	ENET_MDI_N<3>	132 136

TABLE_6_HEAD

TABLE_6_ITEM

514-0253 1 CON,RJ-45 7 DEGRESS JD600 CRITICAL 17_INCH_LCD

TABLE_6_ITEM

514-0254 1 CON,RJ-45 7 DEGRESS JD600 CRITICAL 20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>

RD604 49.9 RES 5% 1/16W MF-LF 402 2
RD605 49.9 RES 5% 1/16W MF-LF 402 2

ENET_MDI0

136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>

CD606 CAP 0.01UF 20% 16V CERM 402 2 GND

RD606 49.9 RES 5% 1/16W MF-LF 402 2
RD607 49.9 RES 5% 1/16W MF-LF 402 2

ENET_MDI1

136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>

RD608 49.9 RES 5% 1/16W MF-LF 402 2
RD609 49.9 RES 5% 1/16W MF-LF 402 2

ENET_MDI2

CD607 CAP 0.01UF 20% 16V CERM 402 2 GND

136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>

CD608 CAP 0.01UF 20% 16V CERM 402 2 GND

RD610 49.9 RES 5% 1/16W MF-LF 402 2
RD611 49.9 RES 5% 1/16W MF-LF 402 2

ENET_MDI3

CD609 CAP 0.01UF 20% 16V CERM 402 2 GND

LD600
FERR-EMI-600-OHM

7 =PP2V5_ENET — 1 IND 2 — PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.38mm
VOLTAGE=2.5V

CD600 CAP 0.1UF 20% 10V CERM 402 2 GND
CD601 CAP 0.1UF 20% 10V CERM 402 2 GND

7 GND_CHASSIS_RJ45

CD604 CAP 0.001UF 10% 50V CERM 402 1 2 GND

CON_RJ45_10ANG_S3MT_TH1
5
6
13
11
1
2
3
4
7
8
9
10
12

CD605 CAP 0.001UF 10% 50V CERM 402 2 GND

(514-0253)

OMIT

JD600
JFM38V10-0112-4F
F-ANG-TH

136 132 7 =PP3V3_ENET

DEVELOPMENT
RD601 330 RES 5% 1/10W MF-LF 603 2

LED8700_P 9

DEVELOPMENT
LEDD600 GREEN-3.6MCD 2.0X1.25MM-SM LED 1 2

132 TP_VESTA_XMTLED_L — VESTA_XMTLED_L
MAKE_BASE=TRUE

136 132 7 =PP3V3_ENET

DEVELOPMENT
RD603 330 RES 5% 1/10W MF-LF 603 2

LED8701_P 9

DEVELOPMENT
LEDD601 GREEN-3.6MCD 2.0X1.25MM-SM LED 1 2

132 TP_VESTA_ACTLED_L — VESTA_ACTLED_L
MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE_VIA 1 HOLE_VIA
ZHD691 HOLE_VIA 1 HOLE_VIA
ZHD692 HOLE_VIA 1 HOLE_VIA
ZHD693 HOLE_VIA 1 HOLE_VIA
GND

ETHERNET CONNECTOR

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

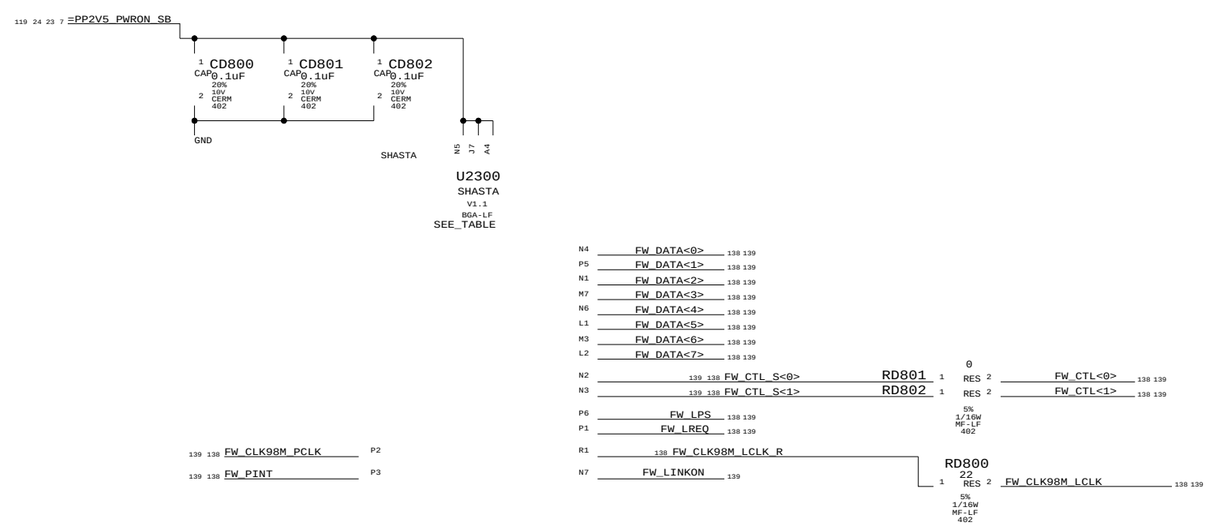
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR		
	ENET_FW_2X		FW_DATA<7..0>	138 139
E91	ENET_FW_3X		FW_CTL_S<1..0>	138 139
	ENET_FW_3X		FW_CTL<1..0>	138 139
E87	ENET_FW_2X		FW_DATA_R<7..0>	139
E88	ENET_FW_3X		FW_CTL_R<1..0>	139
	ENET_FW_3X		FW_LPS	138 139
	ENET_FW_3X		FW_LREQ	138 139
	ENET_FW_3X		FW_PINT	138 139
	0.38mm_SPACING		FW_CLK98M_LCLK	138 139
	0.38mm_SPACING		FW_CLK98M_PCLK	138 139
	0.38mm_SPACING		FW_CLK98M_LCLK_R	138

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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LAST_MODIFIED=Fri Apr 28 20:22:25 2006

DRAWING

APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
		0.38mm SPACING		FW_CLK98M_PCLK_R 139
(PROVIDED BY LINK PAGE)				
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 9	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
1302	FW_CTL			FW_CTL_S<1..0> 138
1400	FW_CTL			FW_CTL<1..0> 138 139
1401	FW_CTL			FW_CTL_R<1..0> 138 139

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

Net Spacing Type: FW

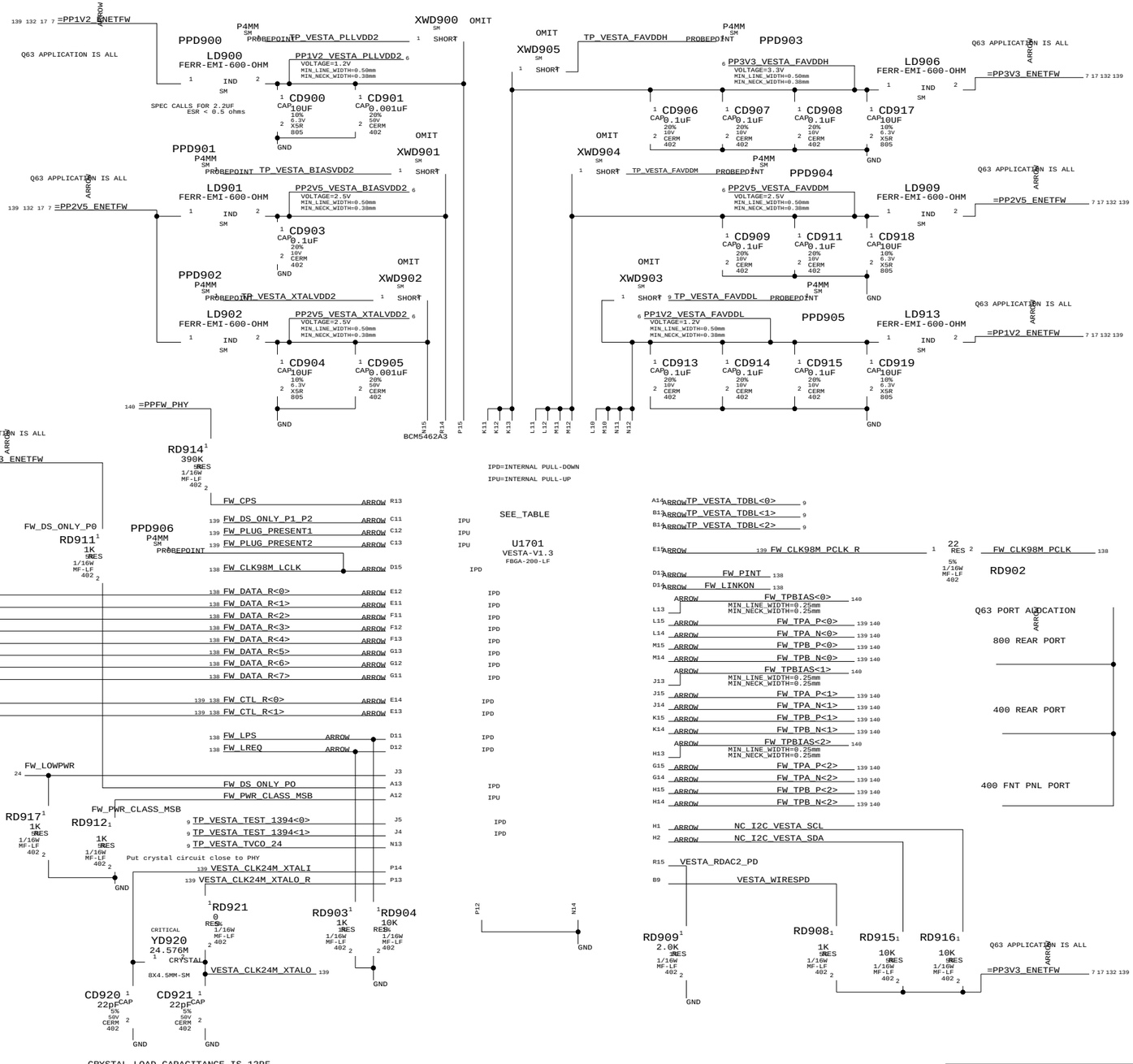
NOTE: Target differential impedance for FW data pairs is 110 ohms.

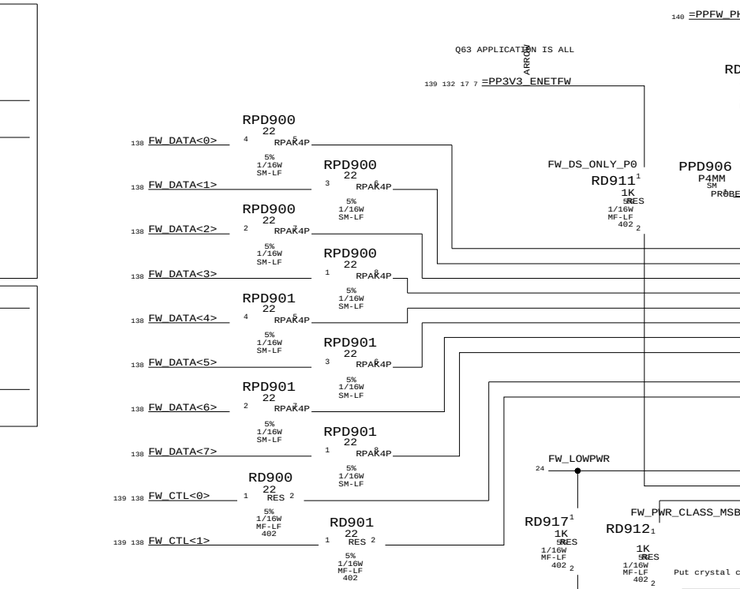
VESTA CONFIG STRAPS:

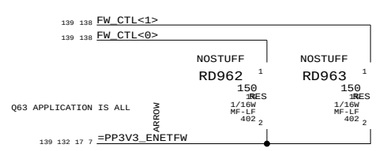
FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

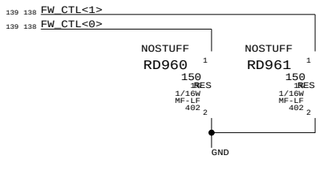
FW_DS_ONLY_P0 - PORT 0 DATA/STROBE
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

LAST_MODIFIED=Fri Apr 28 20:22:26 2006
DRAWING









IPD=INTERNAL PULL-DOWN
IPU=INTERNAL PULL-UP

SEE_TABLE
U1701 VESTA-V1.3 FBGA-200-LF

Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=08/26/2005

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APPLE_DSIZEPAGE

NET_TYPE			
SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
140 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL 140
140 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL 140
140 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL 140
140 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL 140
140 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL 140
140 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL 140
140 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL 140
140 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL 140

8 WATTS MAX
12 VOLTS

7 =PP12V_ALL_FW

RE056 1.3 RES 2512 1% 1W FF
PP12V_FW
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=12V
MAKE_BASE=TRUE

I443 =PPFW_PHY 139

TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XXG DIODE SMC
FW_VP_R
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
MAKE_BASE=TRUE
VOLTAGE=24V

CE009 0.1UF CAP 10% 50V X7R 603-1
GND

CRITICAL
RE002 1.3 RES 2512 1% 1W FF
FW_VP
MIN_LINE_WIDTH=0.8MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=24V

FW_VP MAX IS 24V

FE002 0.75AMP-13.2V FUSE MINISMD-LF
PPFW_PORT0_VP
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=24V

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V FUSE SM-LF
PPFW_PORT1_VP 140
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=24V

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
139 FW_TPBIAS<1>
139 FW_TPBIAS<0>
VOLTAGE=1.86V

CE050 1UF CAP 10% 6.3V CERM 402 GND
CE060 1UF CAP 10% 6.3V CERM 402 GND

RE050 56.2 RES 1% 1/16W MF-LF 402
RE051 56.2 RES 1% 1/16W MF-LF 402
RE060 56.2 RES 1% 1/16W MF-LF 402
RE061 56.2 RES 1% 1/16W MF-LF 402

139 FW_TPA_P<0> — FW_PORT0_TPA_P 140
139 FW_TPA_N<0> — FW_PORT0_TPA_N 140
139 FW_TPB_P<0> — FW_PORT0_TPB_P 140
139 FW_TPB_N<0> — FW_PORT0_TPB_N 140
139 FW_TPA_P<1> — FW_PORT1_TPA_P 140
139 FW_TPA_N<1> — FW_PORT1_TPA_N 140
139 FW_TPB_P<1> — FW_PORT1_TPB_P 140
139 FW_TPB_N<1> — FW_PORT1_TPB_N 140
MAKE_BASE=TRUE

RE052 56.2 RES 1% 1/16W MF-LF 402
RE053 56.2 RES 1% 1/16W MF-LF 402
RE062 56.2 RES 1% 1/16W MF-LF 402
RE063 56.2 RES 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
FW_TPA_C<1> VOLTAGE=0V

CE054 270pF CAP 5% 25V CERM 402
RE054 4.99K RES 1% 1/16W MF-LF 402
CE064 270pF CAP 5% 25V CERM 402
RE064 4.99K RES 1% 1/16W MF-LF 402
GND

3rd TPA/TPB pair unused

139 FW_TPBIAS<2> — NC_FW_TPBIAS2
139 FW_TPA_P<2> — NC_FW_TPA_P2
139 FW_TPA_N<2> — NC_FW_TPA_N2
MAKE_BASE=TRUE
NO_TEST=YES

139 FW_TPB_P<2> —
139 FW_TPB_N<2> — FW_TPB2_PD
MAKE_BASE=TRUE
NO_TEST=YES

RE070 1K RES 5% 1/16W MF-LF 402
GND

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

7 =PP3V3_FW
RE090 215 RES 1% 1/16W MF-LF 402
PP3V3_FW_ESD_F
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

LE090 400-OHM-EMI IND SM-1
PP3V3_FW_ESD 140
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

DE090 SOT23 BZX84C2V7-X-F ZENER
GND

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD
DPE010 BAV99DW-X-F SOT-363
CE010 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
CE011 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
GND

140 FW_PORT0_TPA_P
140 FW_PORT0_TPA_N
FLE010 120-OHM 2012
FLE011 120-OHM 2012
FILTER_4P

140 FW_PORT0_TPB_P
140 FW_PORT0_TPB_N

140 PP3V3_FW_ESD
DPE011 BAV99DW-X-F SOT-363
CE012 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
CE013 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
GND

LE010 IND FERR-160-OHM 1206-LF

PORT 0
1394A
OMIT

JE000 UF01613-M33-4F F-ST-TH CON_F6ST_S4MT_TH1
140 FW_PORT0_TPA_P_FL (TPA+)
140 FW_PORT0_TPA_N_FL (TPA-)
140 FW_PORT0_TPB_P_FL (TPB+)
140 FW_PORT0_TPB_N_FL (TPB-)

PPFW_PORT0_VP_FL
VOLTAGE=24V
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
GND

FW_VP MAX IS 24V
CE015 1UF CAP 10% 50V X7R 603-1
CE016 0.01UF CAP 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD
DPE020 BAV99DW-X-F SOT-363
CE020 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
CE021 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
GND

140 FW_PORT1_TPA_P
140 FW_PORT1_TPA_N
FLE020 120-OHM 2012
FLE021 120-OHM 2012
FILTER_4P

140 FW_PORT1_TPB_P
140 FW_PORT1_TPB_N

140 PP3V3_FW_ESD
DPE021 BAV99DW-X-F SOT-363
CE022 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
CE023 0.001UF CAP 10% 50V CERM 402 DIODE_DUAL_6P
GND

PPFW_PORT1_VP 140

LE020 IND FERR-160-OHM 1206-LF

PORT 1
1394A
OMIT

JE001 UF01613-M33-4F F-ST-TH CON_F6ST_S4MT_TH1
140 FW_PORT1_TPA_P_FL (TPA+)
140 FW_PORT1_TPA_N_FL (TPA-)
140 FW_PORT1_TPB_P_FL (TPB+)
140 FW_PORT1_TPB_N_FL (TPB-)

PPFW_PORT1_VP_FL
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=24V
GND

CE025 0.1UF CAP 10% 50V X7R 603-1
CE026 0.01UF CAP 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

ZHE090 HOLE_VIA
ZHE091 HOLE_VIA
ZHE092 HOLE_VIA
ZHE093 HOLE_VIA
GND

TABLE_6_HEAD					
TABLE_6_ITEM					
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
TABLE_6_ITEM					
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
TABLE_6_ITEM					
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
TABLE_6_ITEM					
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

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APPLE_DSIZEPAGE

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_0
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_1
	USB2	USB2_S	USB2_2
	USB2	USB2_S	USB2_2
	USB2	USB2	USB2_3
	USB2	USB2	USB2_3
	USB2	USB2	USB2_4
	USB2	USB2	USB2_4
	0.38mm SPACING		
	0.38mm SPACING		
	0.38mm SPACING		

USB2_P<0> 142 143
USB2_N<0> 142 143
USB2_P<1> 142 143
USB2_N<1> 142 143
USB2_P<2> 142 143
USB2_N<2> 142 143
USB2_P<3> 142 143
USB2_N<3> 142 143
USB2_P<4> 142 143
USB2_N<4> 142 143
NEC_CLK30M_XT1 142
NEC_CLK30M_XT2 142
NEC_CLK30M_XT2_R 142

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

LE235 FERR-EMI-100-OHM IND SM
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
XWE200 OMIT SM SHORT
TP_NEC_AVDD
P4MM SM PROBEPOINT PPE2000
ARROW
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
RE235 4.7 RES 5% 1/10W MF-LF 603
CE235 10UF CAP 10% 6.3V X5R 805
CE236 0.1UF CAP 20% 10V CERM 402
CE237 0.1UF CAP 20% 10V CERM 402
145 144 142 7 =PP3V3_PWRON_USB
GND_NEC_AVSS_R 6 142
CE220 10UF CAP 10% 6.3V X5R 805
CE221 0.1UF CAP 20% 10V CERM 402
CE222 0.1UF CAP 20% 10V CERM 402
CE223 0.1UF CAP 20% 10V CERM 402
CE224 0.1UF CAP 20% 10V CERM 402
CE225 0.1UF CAP 20% 10V CERM 402
CE226 0.1UF CAP 20% 10V CERM 402
CE227 0.1UF CAP 20% 10V CERM 402
CE228 0.1UF CAP 20% 10V CERM 402
CE229 0.1UF CAP 20% 10V CERM 402
CE230 0.1UF CAP 20% 10V CERM 402
GND
UPD720101_FBGA_SPLIT
CRITICAL
UC200 NEC_UPD720101_USB2 FBGA-LF

RE200 36 RES 1% 1/16W MF-LF 402
M14 143 USB_NEC_N<0>
M13 (USB2_N<0>)
L14 (USB2_P<0>)
K13 143 USB_NEC_P<0>
USB2_N<0> 142 143
USB2_P<0> 142 143
RE201 36 RES 1% 1/16W MF-LF 402

P4MM SM PROBEPOINT PPE2002
RE202 36 RES 1% 1/16W MF-LF 402
K14 143 USB_NEC_N<1>
K12 (USB2_N<1>)
J14 (USB2_P<1>)
J12 143 USB_NEC_P<1>
USB2_N<1> 142 143
USB2_P<1> 142 143
RE203 36 RES 1% 1/16W MF-LF 402
P4MM SM PROBEPOINT PPE2001
RE204 36 RES 1% 1/16W MF-LF 402
H11 143 USB_NEC_N<2>
G11 (USB2_N<2>)
G13 (USB2_P<2>)
G14 143 USB_NEC_P<2>
USB2_N<2> 142 143
USB2_P<2> 142 143
RE205 36 RES 1% 1/16W MF-LF 402
40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION
RE206 36 RES 1% 1/16W MF-LF 402
F12 143 USB_NEC_N<3>
F14 (USB2_N<3>)
E12 (USB2_P<3>)
E14 143 USB_NEC_P<3>
USB2_N<3> 142 143
USB2_P<3> 142 143
RE207 36 RES 1% 1/16W MF-LF 402
RE208 36 RES 1% 1/16W MF-LF 402
E13 143 USB_NEC_N<4>
D14 (USB2_N<4>)
C13 (USB2_P<4>)
C14 143 USB_NEC_P<4>
USB2_N<4> 142 143
USB2_P<4> 142 143
BLUTOOTH CONNECTOR,(PORT #4)
RE209 36 RES 1% 1/16W MF-LF 402

145 144 142 7 =PP3V3_PWRON_USB
RE210 33K RES 1/16W MF-LF 402
RPE210 RPAK4P 10K 5% 1/16W SM-LF
USB2_OC<0> 143 (USB2_OC<0>) B12
USB2_OC<1> 143 (USB2_OC<1>) B11
USB2_OC<2> 143 (USB2_OC<2>) B10
USB2_OC<3> (USB2_OC<3>) A10
USB2_OC<4> (USB2_OC<4>) B9
USB2_PWREN<0> 143 C12
USB2_PWREN<1> 143 A11
USB2_PWREN<2> 143 C11
USB2_PWREN<3> 143 C10
USB2_PWREN<4> 143 A9

SHASTA
U2300 SHASTA V1.1 BGA-LF

P7	TP_SB<0> 6
P8	TP_SB<1> 6
R3	TP_SB<2> 6
R4	TP_SB<3> 6
R5	TP_SB<4> 6
R6	TP_SB<5> 6
R7	TP_SB<6> 6
R8	TP_SB<7> 6
T1	TP_SB<8> 6
T2	TP_SB<9> 6
T3	TP_SB<10> 6
T4	TP_SB<11> 6
T5	TP_SB<12> 6
T6	TP_SB<13> 6
T7	TP_SB<14> 6
T8	TP_SB<15> 6
U1	TP_SB<16> 6
U2	TP_SB<17> 6
U3	TP_SB<18> 6
U4	TP_SB<19> 6
U5	TP_SB<20> 6
U6	TP_SB<21> 6
V1	TP_SB<22> 6
V2	TP_SB<23> 6
V3	TP_SB<24> 6
V4	TP_SB<25> 6
W1	TP_SB<26> 6
W3	TP_SB<27> 6
Y1	TP_SB<28> 6
Y3	TP_SB<29> 6

145 144 142 7 =PP3V3_PWRON_USB
RE240 1.5K RES 1% 1/16W MF-LF 402
RE241 1.5K RES 1% 1/16W MF-LF 402
NEC_NC1_PU P6
NEC_NC2_PU M6

142 NEC_CLK30M_XT1 L9
142 NEC_CLK30M_XT2_R P8
RE245 100 RES 1% 1/16W MF-LF 402
CRITICAL
YE245 30.0000M CRYSTAL
NEC_CLK30M_XT2 142
8X4.5MM-SM1
CE245 22pF CAP 5% 50V CERM 402
CE246 22pF CAP 5% 50V CERM 402
GND
SPEC SHOWS LOAD CAPACITANCE OF 16PF

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8
XWE201 SM SHORT OMIT
P13 M12 N11
Tie to GND at ball N11
GND
P11 NEC_RREF_PD
RE238 9.09K RES 1% 1/16W MF-LF 402
ARROW
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R 6 142
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

USB Host Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

LAST_MODIFIED=Fri Apr 28 20:22:29 2006
DRAWING

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APPLE_DSIZEPAGE

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

External USB Ports

7 =PP5V_PWRON_USB
CRITICAL
SWI_TPS2024
UE300
TPS2024
SOI-LF
GND

142 USB2_OC<0> — USB_OC MAKE_BASE=TRUE
142 USB2_OC<1>
142 USB2_OC<2>

96 PP5V_USB2
LE310
FERR-250-OHM
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
NOSTUFF
CE310
150UF
CAP
20%
6.3V
POLY
SMD2
RE336
0
RES
805
1/8W
MF-LF
5%
GND
PP5V_USB2_PORT1_F
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
GND_USB_PORT1
CE312
CE313
0.01uF
CAP
20%
16V
CERM
402
OMIT
JE310
UB01123M23-4F
F-ST-TH
CON_F4ST_USB_S3MT_TH
VDD
D-
D+
GND
PORT 1
514-0247
GND_CHASSIS_USB
MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
VOLTAGE=0
7 143

LE312
120-OHM
2012
142 USB2_N<0> — USB2_PORT1_N MAKE_BASE=TRUE
142 USB2_P<0> — USB2_PORT1_P MAKE_BASE=TRUE
FILTER_4P
143 USB2_PORT1_N_F
143 USB2_PORT1_P_F
NOSTUFF
RE312
RE313
0
RES
402
RE310
RE311
15K
1/16W
MF-LF
GND

LE320
FERR-250-OHM
PP5V_USB2_PORT2_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
CE320
330UF
RE335
GND_USB_PORT2
CE322
CE323
OMIT
JE320
UB01123M23-4F
PORT 2
514-0247
GND_CHASSIS_USB

LE322
120-OHM
2012
142 USB2_N<1> — USB2_PORT2_N MAKE_BASE=TRUE
142 USB2_P<1> — USB2_PORT2_P MAKE_BASE=TRUE
143 USB2_PORT2_N_F
143 USB2_PORT2_P_F
RE322
RE323
RE320
RE321

LE330
FERR-250-OHM
PP5V_USB2_PORT3_F
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
RE334
GND_USB_PORT3
CE332
CE333
OMIT
JE330
UB01123M23-4F
PORT 3
514-0247
GND_CHASSIS_USB

LE332
120-OHM
2012
142 USB2_N<2> — USB2_PORT3_N MAKE_BASE=TRUE
142 USB2_P<2> — USB2_PORT3_P MAKE_BASE=TRUE
143 USB2_PORT3_N_F
143 USB2_PORT3_P_F
RE332
RE333
RE330
RE331

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F 143
	USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 143
	USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 143
	USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 143
	USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2> 143
	USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2> 143
	USB2	USB2_BNDI_F	USB2	USB2_P_L<3> 143
	USB2	USB2_BNDI_F	USB2	USB2_N_L<3> 143
	USB2	USB2_0_IC	USB2	USB_NEC_P<0> 142
	USB2	USB2_0_IC	USB2	USB_NEC_N<0> 142
	USB2	USB2_1_IC	USB2	USB_NEC_P<1> 142
	USB2	USB2_1_IC	USB2	USB_NEC_N<1> 142
	USB2	USB2_2_IC	USB2	USB_NEC_P<2> 142
	USB2	USB2_2_IC	USB2	USB_NEC_N<2> 142
	USB2	USB2_3_IC	USB2	USB_NEC_P<3> 142
	USB2	USB2_3_IC	USB2	USB_NEC_N<3> 142
	USB2	USB2_4_IC	USB2	USB_NEC_P<4> 142
	USB2	USB2_4_IC	USB2	USB_NEC_N<4> 142

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

TABLE_6_HEAD
TABLE_6_ITEM
514-0294 3 USB RECEPTACLE,4P,UB1123-M23B-4F JE310,JE320,JE330 CRITICAL 17_INCH_LCD
TABLE_6_ITEM
514-0295 3 USB RECEPTACLE,4P,UB1123-M33B-4F JE310,JE320,JE330 CRITICAL 20_INCH_LCD

7 =PP5V_PWRON_BNDI
VOLTAGE=5V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
FE301
0.75AMP-13.2V
MINISMD-LF
740S0509
CRITICAL
PP5V_BNDI_LE340
CE344
CAP
10UF
20%
16V
CERM
805-2
LE340
FERR-250-OHM
IND
SM
PP5V_PWRON_BNDI 143
RE346
0
RES
805
1/8W
MF-LF
5%
GND
VOLTAGE=0V
MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
GND_BNDI 143
CE342
0.01uF
CE343
0.01uF
143 7 GND_CHASSIS_BNDI

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE

NOSTUFF
RE343
0
RES
402
144 USB2_HUB_P<2>
LE342
120-OHM
2012
FILTER_4P
NOSTUFF
RE342
144 USB2_HUB_N<2>
NOSTUFF
RE354
144 USB2_HUB_P<3>
LE352
NOSTUFF
RE355
144 USB2_HUB_N<3>

FHB CONNECTOR
518S0324
JE350
53261-1498
M-RT-SM
CON_M14RT_S2MT_SM
153 AUD_MIC_IN_P_CONN 1
153 GND_AUDIO_MIC_CONN 2
153 AUD_MIC_IN_N_CONN 3
143 7 GND_CHASSIS_BNDI 4
5
143 7 GND_CHASSIS_BNDI 6
143 USB2_HUB_P_L<2> 7
143 USB2_HUB_N_L<2> 8
9
143 GND_BNDI 10
143 USB2_P_L<3> 11
143 USB2_N_L<3> 12
24 SB_GPIO14 13
143 PP5V_PWRON_BNDI 14
15
16

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

SENDS NEC USB PORT 3 TO BLUETOOTH MODULE
121 USB_BT_P — USB2_P<3> 142 MAKE_BASE=TRUE
121 USB_BT_N — USB2_N<3> 142 MAKE_BASE=TRUE
RE350
RE351
15K
1/16W
MF-LF
GND

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT
142 USB2_P<4> — USB2_HUB_P<0> 144 MAKE_BASE=TRUE
142 USB2_N<4> — USB2_HUB_N<0> 144 MAKE_BASE=TRUE
RE352
RE353
15K
1/16W
MF-LF
GND

USB Device Interfaces

SYNC_MASTER=FINO-M23 SYNC_DATE=09/20/2005

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APPLE_DSIZEPAGE

TABLE_6_HEAD

TABLE_6_ITEM

338S0257 1 USX2006-NU-01 CUSTOM MASK UE400 CRITICAL CARD_READER

PP1V8_USB_HUB_VDD_INTERNAL VOLTAGE=1.8V
MIN_LINE_WIDTH=.38 MM
MIN_NECK_WIDTH=.2 MM
CE413 0.1UF 20% 10V CERM 402
CE414 0.1UF 20% 10V CERM 402
CE415 0.1UF 20% 10V CERM 402
CE416 4.7UF 20% 6.3V CERM 805
GND

MIN_LINE_WIDTH=.38 MM
MIN_NECK_WIDTH=.2 MM
PP1V8_USB_HUB_PLL_INTERNAL
VOLTAGE=1.8V
CE418 4.7UF 20% 6.3V CERM 805
GND

145 144 142 7 =PP3V3_PWRON_USB
CE419 0.1UF 20% 10V CERM 402
CE420 0.1UF 20% 10V CERM 402
CE421 0.01UF 20% 16V CERM 402
CE422 4.7UF 20% 6.3V CERM 805
GND

145 144 142 7 =PP3V3_PWRON_USB
CE423 0.1UF 20% 10V CERM 402
CE424 0.1UF 20% 10V CERM 402
GND

USB2503 11 13 23 31 40 45 44 39

=PP3V3_PWRON_USB 7 142 144 145
RE404 10K 5% 1/16W MF-LF 402
RE405 10K 5% 1/16W MF-LF 402
RE406 10K 5% 1/16W MF-LF 402
RE407 10K 5% 1/16W MF-LF 402

TEST PINS SET XNOR
ACTIVE HIGH
GANGED POWER
SELF POWERED
INTERNAL DEFAULTS

TP_USB_HUB_TEST<0> 24
TP_USB_HUB_TEST<1> 36
USB_HUB_PRTPWR_POL 18
USB_HUB_GANG_EN 20
USB_HUB_SELF_PWR 28
USB_HUB_CFG_SEL1 27
USB_HUB_RESET_L 37
USB_HUB_CLKIN_EN 35
144 XTAL_IN_USB_HUB 43
144 XTAL_OUT_USB_HUB 42
144 USB_HUB_ATEST 46
144 USB_HUB_VBUS_DET 29
143 USB2_HUB_P<0> 2
143 USB2_HUB_N<0> 3
INTERNAL DEFAULTS 25
USB_HUB_CFG_SEL0 26
USB_HUB_RBIAS 47

UE401
USB2503
QFN
CRITICAL

=PP3V3_PWRON_USB 7 142 144 145
RE409 100K 5% 1/16W MF-LF 402

CE425 0.1UF 20% 10V CERM 402
GND

RE410 10K 5% 1/16W MF-LF 402

RE411 1M 5% 1/16W MF-LF 402
RE425 0 5% 1/16W MF-LF 402

YE401 24.000M
144 1 CRYSTAL XTAL_OUT_USB_HUB_R 143 USB2_HUB_N<0>
5X3.2X1.2-SM
CRITICAL

CRYSTAL IS 60PP INCLUDING AGING
NEED TO CHECK LOADING
CRYTAL LOADING IS 16PF

CE426 22PF 5% 50V CERM 402
CE427 22PF 5% 50V CERM 402
GND

144 142 7 =PP3V3_PWRON_USB 145
RE414 10K 5% 1/16W MF-LF 402
1.8V INTERNAL REGULATOR ENABLED
USB_HUB_ATEST 144

145 144 142 7 =PP3V3_PWRON_USB
RE415 10K 5% 1/16W MF-LF 402
USB_HUB_VBUS_DET 144

RE412 10K 5% 1/16W MF-LF 402
RE413 12.1K 5% 1/16W MF-LF 402
DATA SHEET SAYS 12.0K 1%
GND

4 10 22 30 38 41 48 49
GND

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
144 IN	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
144 IN	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
144 143 IN	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
144 143 IN	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
143 IN	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
144 143 IN	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
144 IN	0.38MM SPACING			XTAL_IN_CARD_READER
144 IN	0.38MM SPACING			XTAL_OUT_CARD_READER
144 IN	0.38MM SPACING			XTAL_OUT_CARD_READER_R
144 IN	0.38MM SPACING			XTAL_IN_USB_HUB
144 IN	0.38MM SPACING			XTAL_OUT_USB_HUB
144 IN	0.38MM SPACING			XTAL_OUT_USB_HUB_R

=PP3V3_PWRON_USB 7 142 144 145
RE417 10K 5% 1/16W MF-LF 402
RE432 10K 5% 1/16W MF-LF 402

6 USB2_HUB_P<1> 144
5 USB2_HUB_N<1> 144
34
21 USB_HUB_NON_REM0
33
HIGH = PORT 1 NON-REMOVABLE

8 USB2_HUB_P<2> 143 144
9 USB2_HUB_N<2> 143 144
32
19 USB_HUB_NON_REM1
16
HIGH = PORT 2 AND 3 NON-REMOVABLE
LOW = PORT 2 AND 3 REMOVABLE

12 USB2_HUB_P<3> 143 144
11 USB2_HUB_N<3> 143 144
15
17 USB_HUB_PRT_DIS0
14
PORT 3 ENABLED

NOSTUFF
RE418 10K 5% 1/16W MF-LF 402
RE419 10K 5% 1/16W MF-LF 402
GND

=PP3V3_PWRON_USB 7 142 144 145
NOSTUFF
RE426 100K 5% 1/16W MF-LF 402
RE435 100K 5% 1/16W MF-LF 402
RE433 10K 5% 1/16W MF-LF 402

CARD_READER_ACTIVITY 144
CARD_READER_EE_CS 144 113
CARD_READER_VBUS_DETECT 94
CARD_READER_EE_DIO 144 111
SD_DET_R 110
SD_DET_ACTIVE_LOW
AT SMSC 109
CARD_READER_EE_CLK 144 107
CF_PS 145 105
SD_PWR 145 144 44

RE450 0 5% 1/16W MF-LF 402
SD_DET 145
SD_DET_RC
NOSTUFF
CE450 0.1UF 20% 10V CERM 402
GND
RE427 10K 5% 1/16W MF-LF 402
NOSTUFF
QE000 2N7002 SOT23-LF
TRA_2N7002

=PP3V3_PWRON_USB 7 142 144 145
RE401 100K 5% 1/16W MF-LF 402
RE422 10K 5% 1/16W MF-LF 402
RE423 10K 5% 1/16W MF-LF 402
GND

CE430 0.1UF 20% 10V CERM 402
GND

CARD_READER_RESET_L 115
CARD_READER_TEST_N0_L 96
CARD_READER_TEST_N1_L 95

CE410 0.1UF 20% 10V CERM 402
GND

144 XTAL_IN_CARD_READER 102
144 XTAL_OUT_CARD_READER 103

RE424 0 5% 1/16W MF-LF 402

CARD_READER_ACTIVITY 144
DEVELOPMENT
RE434 330 5% 1/16W MF-LF 402
9 CARD_READER_ACTIVITY_R
DEVELOPMENT
LED LEDE400 GREEN-3.6MCD 2.0X1.25MM-SM
GND

CRYSTAL IS 60PPM INCLUDING AGING
CRYSTAL LOADING IS 16PF
NEED TO CHECK LOADING CAPS

RE403 1M 5% 1/16W MF-LF 402
YE400 24.000M
CRITICAL 1 CRYSTAL XTAL_OUT_CARD_READER_R
5X3.2X1.2-SM
CE411 22PF 5% 50V CERM 402
CE412 22PF 5% 50V CERM 402
GND

104 86 15 16 47 84 85 97 112
GND

PP3V3_CARD_READER_VDDA VOLTAGE=3.3V
MIN_LINE_WIDTH=.38 MM
MIN_NECK_WIDTH=.2 MM
CE405 0.1UF 20% 10V CERM 402
CE406 0.1UF 20% 10V CERM 402
CE407 4.7UF 20% 6.3V CERM 805
GND

RE400 0 5% 1/16W MF-LF 402
=PP3V3_PWRON_USB 7 142 144 145

CE402 0.1UF 20% 10V CERM 402
CE403 0.1UF 20% 10V CERM 402
CE404 4.7UF 20% 6.3V CERM 805
GND

MIN_NECK_WIDTH=.2 MM
MIN_LINE_WIDTH=.38 MM
PP1V8_CARD_READER_PLL
VOLTAGE=1.8V
CE409 4.7UF 20% 6.3V CERM 603
GND

VOLTAGE=1.8V PP1V8_CARD_READER_INTERNAL
MIN_LINE_WIDTH=.38 MM
MIN_NECK_WIDTH=.2 MM
CE400 4.7UF 20% 6.3V CERM 603
CE401 0.1UF 20% 10V CERM 402
GND

USB2227 101 89 3 43 80 108 100 49 106

=PP3V3_PWRON_USB 7 142 144 145
RE430 2.2K 1% 1/16W MF-LF 402

144 USB2_HUB_N<1> 87
144 USB2_HUB_P<1> 88
CARD_READER_RBIAS 98
CARD_READER_ATEST 99
RE402 12.1K 1% 1/16W MF-LF 402
DATA SHEET SAYS 12.0K 1%
GND

OMIT
UE400
USB2227
VTQFP

32 CF_D<0> 145
33 CF_D<1> 145
34 CF_D<2> 145
35 CF_D<3> 145
36 CF_D<4> 145
37 CF_D<5> 145
38 CF_D<6> 145
39 CF_D<7> 145
40 CF_D<8> 145
41 CF_D<9> 145
45 CF_D<10> 145
46 CF_D<11> 145
48 CF_D<12> 145
50 CF_D<13> 145
51 CF_D<14> 145
52 CF_D<15> 145

60 CF_CS_L<0> 145
61 CF_CS_L<1> 145

62 CF_SA<0> 145
63 CF_SA<1> 145
64 CF_SA<2> 145

57 CF_IOR_L 145
58 CF_IOW_L 145
55 CF_IRQ 145
59 CF_RESET_L 145
56 CF_IORDY 145
53 CF_CD_L<1> 145
54 CF_CD_L<2> 145

=PP3V3_PWRON_USB 7 142 144 145
NOSTUFF
CE431 0.1UF 20% 10V CERM 402
EEPROM_93LC56A_NOSTUFF
UE402 93LC56A SOI
CRITICAL
144 CARD_READER_EE_CS 1
144 CARD_READER_EE_CLK 2
6
5
GND
3 CARD_READER_EE_DIO 144
4 CR_EE_DO_NOSTUFF
7
RE431 330 5% 1/16W MF-LF 402

145 144 SD_PWR
NOSTUFF
RE421 10K 5% 1/16W MF-LF 402

26 SD_D<0> 145
27 SD_D<1> 145
28 SD_D<2> 145
29 SD_D<3> 145
31 SD_CLK_R
25 SD_WP_L 145
30 SD_CMD 145

RE428 10K 5% 1/16W MF-LF 402
RE429 10K 5% 1/16W MF-LF 402
RE420 33 5% 1/16W MF-LF 402
SD_CLK 145
CE429 10PF 5% 50V CERM 402
GND

Flash Media Ctrl

SYNC_MASTER=FINO-M23 SYNC_DATE=09/27/2005

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APPLE_DSIZEPAGE

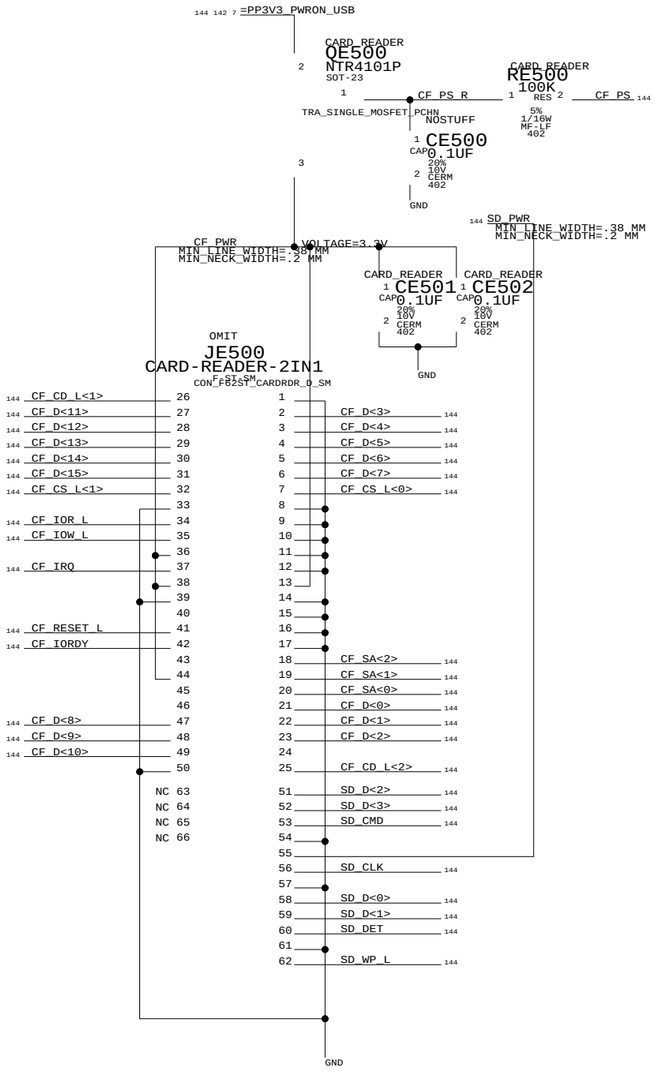
IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

TABLE_6_HEAD

TABLE_6_ITEM

512S0010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER	17_INCH_LCD
512S0012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER	20_INCH_LCD

TABLE_6_ITEM



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC_MASTER=FINO-M23 SYNC_DATE=09/27/2005

APPLE_DSIZEPAGE

AUDIO CODEC
APPLE P/N 353S0933

VOLTAGE=3.3V

LE700
1000-OHM-200MA

MIN_LINE_WIDTH=0.30MM
MIN_NECK_WIDTH=0.20MM
VOLTAGE=3.3V

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=4.5V

154 153 152 7 =PP3V3_AUDIO — 1 — IND 0603 — 2 — PPV_3V3_AUDIO_CODEC

CE700 10UF CAP 10% 6.3V X5R 805 (1 — 2 — GND)

CRITICAL
1 CE701 CAP 1UF 10% 10V CERM 805 2
CRITICAL
1 CE702 CAP 1UF 10% 10V CERM 805 2
CRITICAL
1 CE703 CAP 1UF 10% 10V CERM 805 2

PP4V5_AUDIO_ANALOG 148 154

GND_AUDIO_CODEC 6 147 148 150 154

CRITICAL 16 AUDIO_PCM3052A 23 31

UE700
PCM3052A
VQFN

24 I2S0_BITCLK — NET_SPACING_TYPE=AUDIO — 11
24 I2S0_SYNC — NET_SPACING_TYPE=AUDIO — 10
AUDI2S0OUT — 13
AUDSPDIFOUT — 14
24 I2S0_SB_TO_DEV_DTO — NET_SPACING_TYPE=AUDIO — 12
21 — NC — 20
39 I2C_AUDIO_SCL — NET_SPACING_TYPE=AUDIO — 19
39 I2C_AUDIO_SDA — NET_SPACING_TYPE=AUDIO — 18
24 I2S0_RESET_L — 9
154 AUD_CODEC_MCLK — NET_SPACING_TYPE=AUDIO — 17
NC — 1
24 I2S0_DEV_TO_SB_DTI — NET_SPACING_TYPE=AUDIO

RE700 33 RES 5% 1/16W MF-LF 402 (1 — 2)

RE701 4.7K RES 5% 1/16W MF-LF 402 (1 — 2 — GND)

153 AUD_SPDIF_OUT — NET_SPACING_TYPE=AUDIO

RE702 33 RES 5% 1/16W MF-LF 402 (1 — 2)

15 — GND
8 22 30

2 AUD_CODEC_IN_L 148
6 AUD_CODEC_IN_R 148
25 AUD_CODEC_OUT_L 150 152
24 AUD_CODEC_OUT_R 150 152
26 AUD_PCM_VCOM 152
4 AUD_PCM_REF1
5 AUD_PCM_REF2
3 AUD_CODEC_LI_SHDN_L 148
32 AUD_PSEUDO_VREF 148
27 AUD_PCM_MBIAS 154
28 AUD_MICIN_N 154
29 AUD_MICIN_P 154

CRITICAL
1 CE704 CAP 0.1UF 10% 50V X7R 603-1 2
CRITICAL
1 CE705 CAP 0.1UF 10% 50V X7R 603-1 2
CRITICAL
1 CE706 CAP 10UF 20% 16V ELEC 4X5.5-SM 2
CRITICAL
1 CE707 CAP 0.1UF 10% 50V X7R 603-1 2
CRITICAL
1 CE708 CAP 10UF 20% 16V ELEC 4X5.5-SM 2
CRITICAL
1 CE709 CAP 0.1UF 10% 50V X7R 603-1 2
CRITICAL
1 CE710 CAP 10UF 20% 16V ELEC 4X5.5-SM 2
CRITICAL
1 CE711 CAP 0.1UF 10% 50V X7R 603-1 2
CRITICAL
1 CE712 CAP 10UF 20% 16V ELEC 4X5.5-SM 2

154 150 148 147 6 GND_AUDIO_CODEC

MIN_LINE_WIDTH=0.6MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=0V

AUDIO: CODEC

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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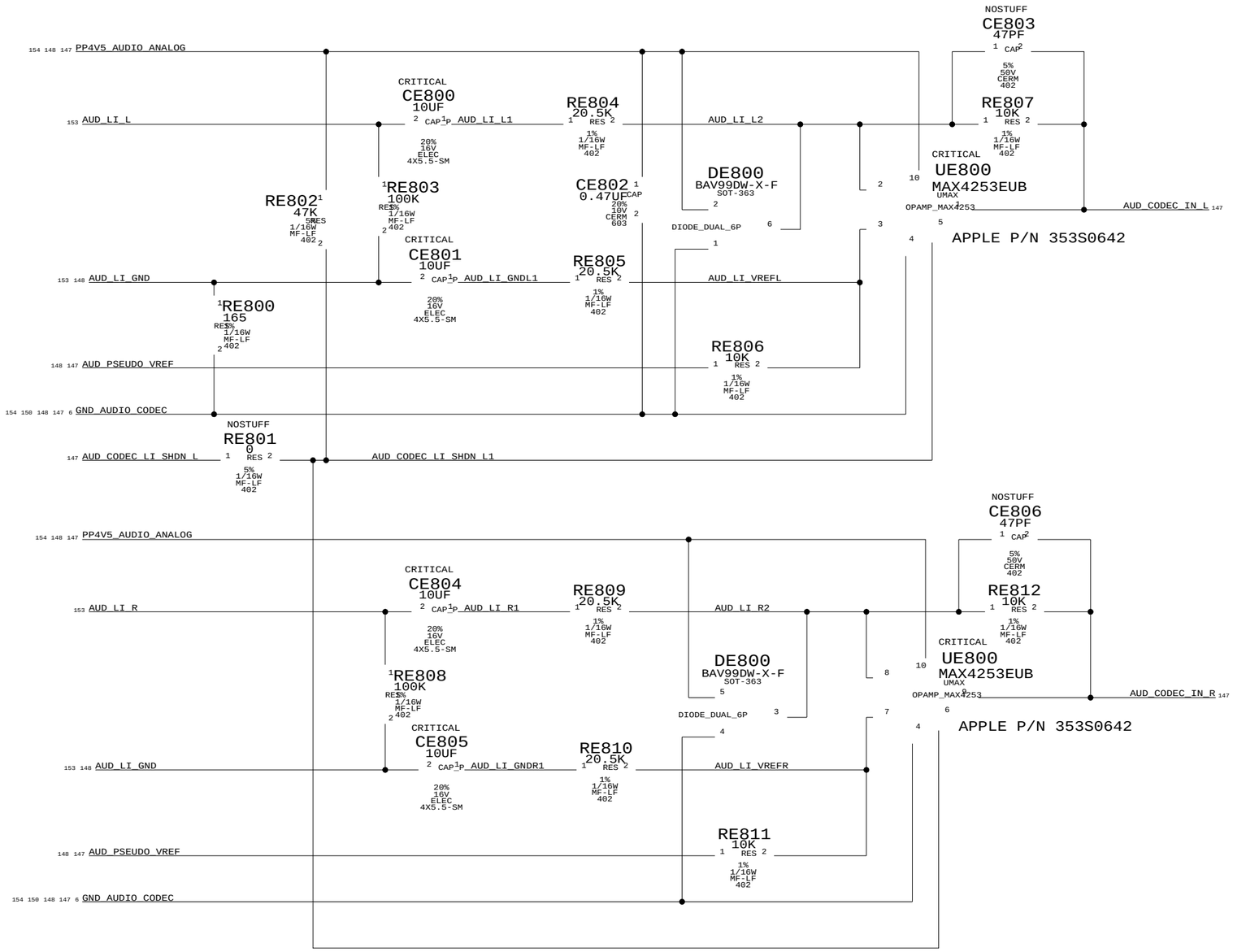
APPLE_DSIZEPAGE

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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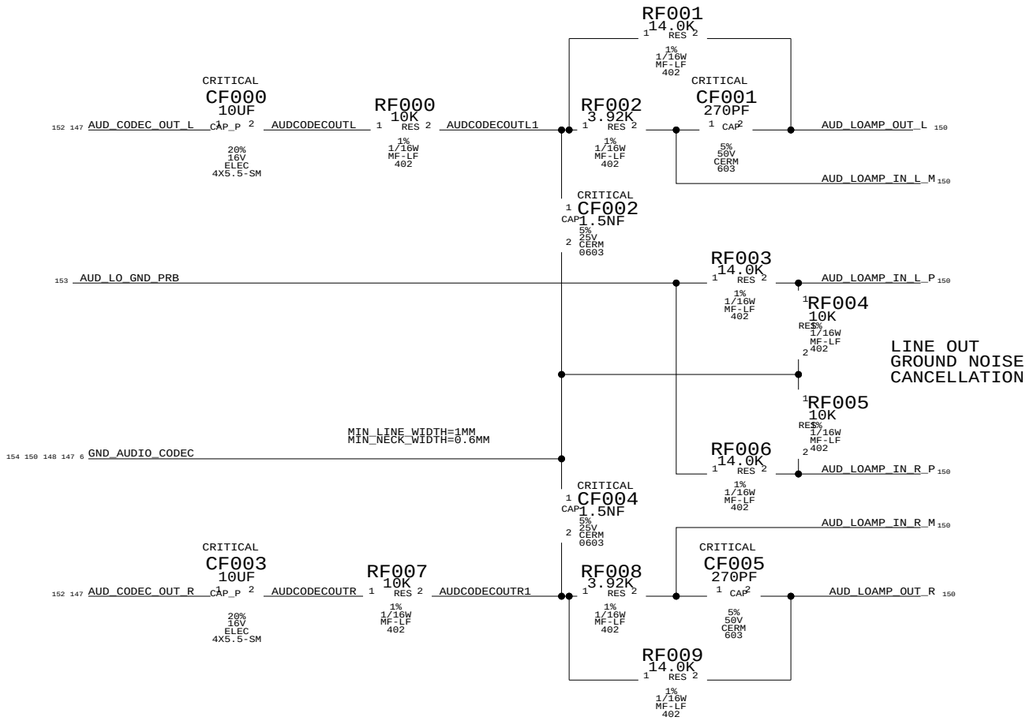
APPLE_DSIZEPAGE

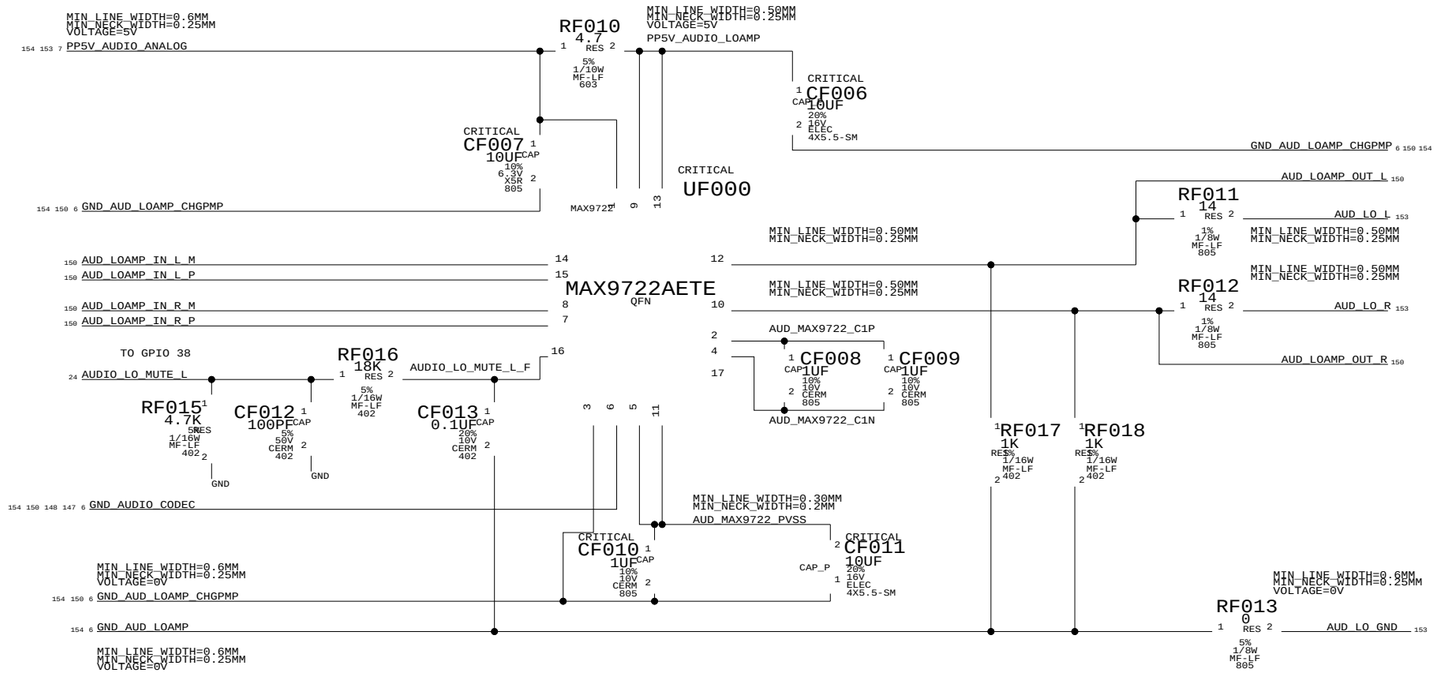
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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APPLE_DSIZEPAGE

SPEAKER AMP

APPLE P/N 353S0680

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUD_SPKRAMP_PWR
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

PP12V_AUDIO_SPKRAMP

LF200
FERR-250-OHM
IND
SM-1

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.30MM
VOLTAGE=12V

PP12V_AUD_SPKRAMP_PLANE

GND_AUDIO_SPKRAMP_PLANE

CRITICAL
CF217 220UF CAP_P 20% 16V ELEC 6.3X8-SM
CF200 220UF CAP_P 20% 16V ELEC 6.3X8-SM
CF201 10UF CAP 10% 16V CERM 1210
CF218 0.1UF CAP 20% 16V CERM 603
CF202 1UF CAP 20% 16V CERM 1206
CF219 0.1UF CAP 20% 16V CERM 603
CF203 10UF CAP 10% 16V CERM 1210
CF223 10UF CAP 10% 16V CERM 1210

AUD_CODEC_OUT_L

LF205 1000-OHM-200MA IND 0603

AUDSAMPINLN

CRITICAL
CF215 100PF CAP 5% 50V CERM 402

CRITICAL
CF204 0.47UF CAP 10% 16V X7R 805

=PP3V3_AUDIO

RF214 10K RES 1% 1/16W MF-LF 402

AUD_PCM_VCOM

LF206 1000-OHM-200MA IND 0603

AUDSAMPINLP

CRITICAL
CF205 0.47UF CAP 10% 16V X7R 805

AUD_SAMP_INL_N
AUD_SAMP_INL_P

LF207 1000-OHM-200MA IND 0603

AUDSAMPINRP

CRITICAL
CF216 100PF CAP 5% 50V CERM 402

CRITICAL
CF206 0.47UF CAP 10% 16V X7R 805

AUD_SAMP_INR_P
AUD_SAMP_INR_N

AUD_CODEC_OUT_R

LF208 1000-OHM-200MA IND 0603

AUDSAMPINRN

CRITICAL
CF207 0.47UF CAP 10% 16V X7R 805

AUD_SAMP_SHDN_L

UF200
MAX9714
QFN-LF

CRITICAL
MAX9714

AUD_SAMP_G1
AUD_SAMP_G2
AUD_SAMP_FS1
AUD_SAMP_FS2

NC

AUD_MAX9714_VREG

MIN_LINE_WIDTH=0.2MM
MIN_NECK_WIDTH=0.15MM

MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.2MM
AUD_MAX9714_CHOLD

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.3MM

AUDSAMPOUTLP
AUDSAMPOUTLN
AUDSAMPCPP
AUDSAMPCPN
AUDSAMPOURTP
AUDSAMPOUTRN
AUDSAMPCSS

CRITICAL
CF208 0.1UF CAP 10% 50V X7R 603-1

CRITICAL
CF209 0.47UF CAP 10% 16V X7R 805

CRITICAL
CF214 0.47UF CAP 10% 16V X7R 805

LF201 180-OHM-1.5A IND 0603
LF202 180-OHM-1.5A IND 0603
LF203 180-OHM-1.5A IND 0603
LF204 180-OHM-1.5A IND 0603

AUD_SPKR_OUTL_P
AUD_SPKR_OUTL_N
AUD_SPKR_OUTR_P
AUD_SPKR_OUTR_N

CRITICAL
CF210 1000PF CAP 5% 25V CERM 603
CF211 1000PF CAP 5% 25V CERM 603
CF212 1000PF CAP 5% 25V CERM 603
CF213 1000PF CAP 5% 25V CERM 603

RF215 10K RES 1% 1/16W MF-LF 402
=PP3V3_AUDIO
AUDIO_SPKR_MUTE_L_INV

TIE TO GPIO 40
AUDIO_SPKR_MUTE_L

RF213 47K RES 5% 1/16W MF-LF 402
AUDIO_SPKR_MUTE_L_F

QF200 2N7002DW-X-F TRA_2N7002DW SOT-363
QF200 2N7002DW-X-F TRA_2N7002DW SOT-363

RF212 4.7K RES 5% 1/16W MF-LF 402
CF220 100PF CAP 5% 50V CERM 402
CF221 100PF CAP 5% 50V CERM 402
GND
GND

XGF200
MOUNTING-HOLE
HOR28

NET_SPACING_TYPE=AUDIO
DIFFERENTIAL_PAIR=AUD_SPKRAMP_PWR
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM

XWF201
SM OMIT
SHORT

NET_SPACING_TYPE=AUDIO
MIN_LINE_WIDTH=1MM
MIN_NECK_WIDTH=0.25MM

GND_AUDIO_SPKRAMP

GND_AUDIO_SPKRAMP_PLANE

GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS

=PP3V3_AUDIO

RPF200
RPAK4P 47K 5% 1/16W SM-LF

AUD_SAMP_FS2
AUD_SAMP_FS1
AUD_SAMP_G2
AUD_SAMP_G1

RF208
0 RES 5% 1/16W MF-LF 402

GND_AUDIO_SPKRAMP_PLANE

AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

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APPLE_DSIZEPAGE

LINE IN JACK

APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)

OMIT
JF300
JA03333-M23-4F
F-ST-TH

CON_F4ST_S4MT_TH1

LF300 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.2MM, MIN_NECK_WIDTH=0.15MM — AUD_LI_L_JACK
LF301 FERR-EMI-100-OHM — AUD_LI_DET_JACK
LF302 FERR-EMI-100-OHM — AUD_LI_R_JACK
LF303 FERR-EMI-100-OHM — AUD_LI_GND_JACK — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.3MM
LF304 FERR-EMI-100-OHM — AUD_LI_L_EMI — AUD_LI_L
LF305 FERR-EMI-100-OHM — AUD_LI_DET_EMI — AUD_LI_DET_H
LF306 FERR-EMI-100-OHM — AUD_LI_R_EMI — AUD_LI_R
LF307 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.3MM — AUD_LI_GND

CF300 CF301 CF302 CF303 100PF 5% 50V CERM 402

DZF300 SUPPR_TRANSIENT 14V-15A 0405

GND_CHASSIS_AUDIO_EXTERNAL

SPEAKER CABLE CONNECTOR

APPLE P/N 518S0249

JF301
53261-0798
M-RT-SM

CON_M7RT_S2MT_SM

LF333 180-OHM-1.5A — AUD_SPKR_OUTR_N_CONN
LF330 180-OHM-1.5A — AUD_SPKR_OUTR_P_CONN
LF332 1000-OHM-200MA — AUDIO_SPKR_ID_CONN
LF331 180-OHM-1.5A — AUD_SPKR_OUTL_N_CONN
LF334 180-OHM-1.5A — AUD_SPKR_OUTL_P_CONN

MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.3MM, NET_SPACING_TYPE=AUDIO

AUD_SPKR_OUTR_N
AUD_SPKR_OUTR_P
=PP3V3_AUDIO
AUDIO_SPKR_ID
AUD_SPKR_OUTL_N
AUD_SPKR_OUTL_P

RF313 47K RES 1/16W MF-LF 402

SPEAKER TYPE DETECT
TO GPIO 43

CF326 CF319 CF325 1000PF 5% 25V CERM 603 — GND

CF327 1000PF 5% 25V CERM 603 — GND

LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED

=PP3V3_AUDIO

RF300 100K RES 1/16W MF-LF 402

RF301 47K RES 1/16W MF-LF 402 — TO GPIO 34 — AUDIO_LI_DET_L

RF302 47K RES 5% 1/16W MF-LF 402 — AUD_LI_DET_H — AUDLINDETH

QF300 2N7002 SOT23-LF TRA_2N7002

CF308 0.1UF 20% 10V CERM 402 — GND

LF308 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO — GND_AUDIO_MIC
LF309 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO, DIFFERENTIAL_PAIR=AUDIO_MIC — AUD_MIC_IN_P
LF310 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO, DIFFERENTIAL_PAIR=AUDIO_MIC — AUD_MIC_IN_N
LF311 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO — GND_AUDIO_MIC_EMI
LF312 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO, DIFFERENTIAL_PAIR=MIC_IN_EMI — AUD_MIC_IN_P_EMI
LF313 FERR-EMI-100-OHM — NET_SPACING_TYPE=AUDIO, DIFFERENTIAL_PAIR=MIC_IN_EMI — AUD_MIC_IN_N_EMI

CF320 CF321 CF322 1000PF 10% 25V X7R 402

GND_CHASSIS_AUDIO_INTERNAL

NET_SPACING_TYPE=AUDIO — GND_AUDIO_MIC_CONN
NET_SPACING_TYPE=AUDIO, DIFFERENTIAL_PAIR=MIC_IN — AUD_MIC_IN_P_CONN
AUD_MIC_IN_N_CONN
NC

DZF302 SUPPR_TRANSIENT 14V-15A 0405
DZF303 SUPPR_TRANSIENT 14V-15A 0405

TABLE_5_HEAD					
CRITICAL	TABLE_5_ITEM				
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	TABLE_5_ITEM				
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	TABLE_5_ITEM				
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE OUT PLUG DETECTS

AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED

=PP3V3_AUDIO

RF303 100K RES 1/16W MF-LF 402

RF304 47K RES 1/16W MF-LF 402 — TO GPIO 32 — AUDIO_LO_DET_L

QF301 2N7002DW-X-F SOT-363 TRA_2N7002DW

RF305 47K RES 5% 1/16W MF-LF 402 — AUD_LO_DET2 — AUD_LO_DET2_1

CF309 0.1UF 20% 10V CERM 402 — GND

=PP3V3_AUDIO
CON_F9ANG_S4MT_TH1

RF306 100K RES 1/16W MF-LF 402

RF307 47K RES 1/16W MF-LF 402 — TO GPIO 33 — AUDIO_LO_OPTICAL_PLUG_L

QF301 2N7002DW-X-F SOT-363 TRA_2N7002DW

RF308 47K RES 5% 1/16W MF-LF 402 — AUD_LO_DET1 — AUD_LO_DET1_1

NOSTUFF
RF309 100K RES 1/16W MF-LF 402 — GND

CF310 0.1UF 20% 10V CERM 402 — GND

LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)

OMIT
JF303
UCNT2052E007-0
F-ANG-TH

10 11 3 6 2 4 1 5 7 8 9 12 13

AUD_LO_DET1_JACK
AUD_LO_L_JACK
AUD_LO_DET2_JACK
AUD_LO_R_JACK
AUD_LO_GND_JACK

MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.4MM, MIN_NECK_WIDTH=0.5MM

MIN_LINE_WIDTH=0.25MM, MIN_NECK_WIDTH=0.2MM — AUD_SPDIF_GND

RF312 0 5% 1/10W MF-LF 402 — GND

PP5V_AUDIO_ANALOG

=PP3V3_AUDIO

RF311 0 1/16W MF-LF 402
RF310 0 NOSTUFF 1/16W MF-LF 402 — AUDIO_SPDIF_PWR

LF314 FERR-EMI-100-OHM — AUD_SPDIF_OUT — AUD_SPDIF_OUT_EMI
LF315 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM — PP5V_AUDIO_SPDIF_EMI
LF316 FERR-EMI-100-OHM — AUD_LO_DET1 — AUD_LO_DET1_EMI
LF318 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM — AUD_LO_L — AUD_LO_L_EMI
LF319 FERR-EMI-100-OHM — AUD_LO_DET2 — AUD_LO_DET2_EMI
LF317 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM — AUD_LO_R — AUD_LO_R_EMI
LF320 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.4MM — AUD_LO_GND — AUD_LO_GND_EMI
LF321 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM — AUD_LO_GND_PRB — AUD_LO_GND_PRB_EMI

LF322 FERR-EMI-100-OHM — AUD_SPDIF_OUT_JACK
LF323 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM — PP5V_AUDIO_SPDIF_JACK
LF324 FERR-EMI-100-OHM
LF326 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM
LF327 FERR-EMI-100-OHM — MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM
LF325 FERR-EMI-100-OHM
LF328 FERR-EMI-100-OHM — MIN_NECK_WIDTH=0.4MM, MIN_LINE_WIDTH=0.5MM
LF329 FERR-EMI-100-OHM

CF317 0.1UF 20% 10V CERM 402
CF318 1UF 10% 10V CERM 805

CF311 CF312 CF315 CF324 100PF 5% 50V CERM 402
CF316 0.01UF 10% 16V CERM 402
CF314 CF313 CF323 100PF 5% 50V CERM 402

DZF301 15V SOT23LF MMBZ15DLT1 — ZENER_MMBZ15VDLT1 — AUD_LI_GND_EMI

GND_CHASSIS_AUDIO_EXTERNAL

AUDIO: CONNECTORS

SYNC_MASTER=FINO-SO
SYNC_DATE=10/07/2005

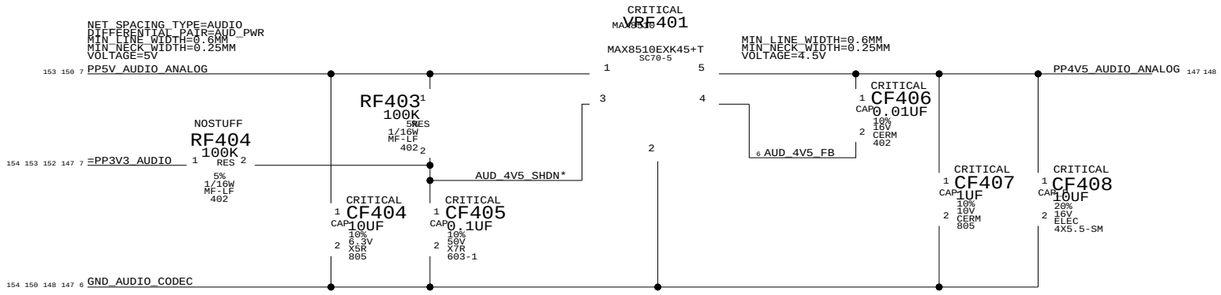
051-6863 H

153 154

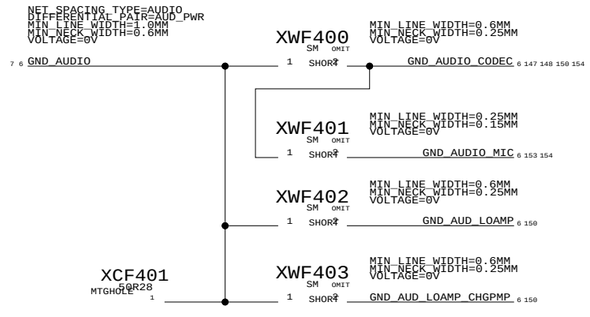
APPLE_DSIZEPAGE

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

APPLE P/N 353S0733



AUDIO GROUND RETURNS



PLACE ACROSS GROUND SPLIT

NOSTUFF RF416 0 5% 1/8W MF-LF 805 RES

152 6 GND_AUDIO_SPKRAMP_PLANE — GND_AUDIO_CODEC 6 147 148 150 154

PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE

NOSTUFF RF417 0 5% 1/8W MF-LF 805 RES

152 7 6 GND_AUDIO_SPKRAMP — GND

PLACE ACROSS GROUND SPLIT AT CODEC UE700

RF405 0 5% 1/8W MF-LF 805 RES

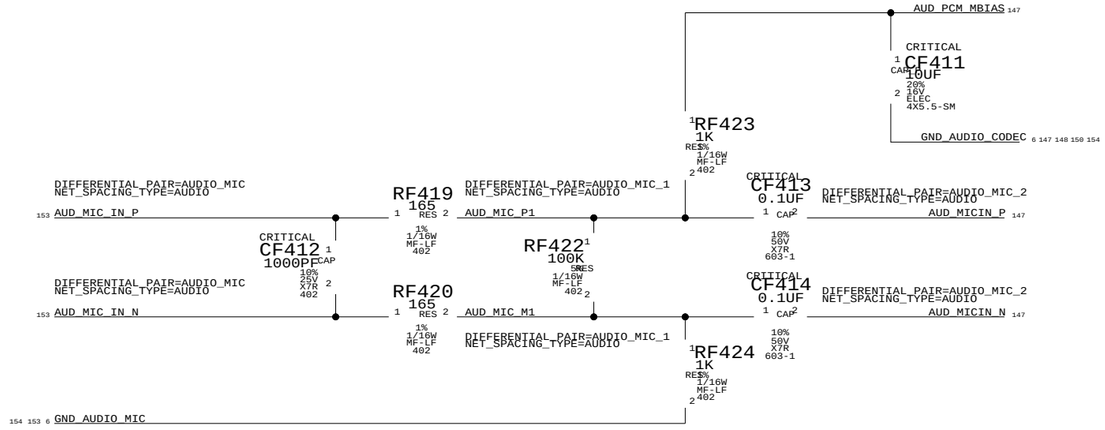
154 150 148 147 6 GND_AUDIO_CODEC — GND

PLACE AT JF303

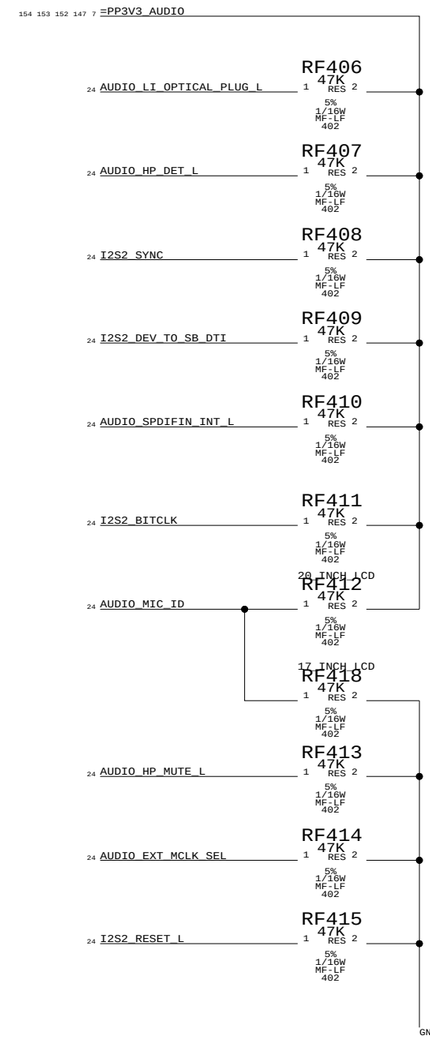
RF429 0 5% 1/8W MF-LF 805 RES

153 7 GND_CHASSIS_AUDIO_EXTERNAL — GND

MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

051-6863 H

154 154

APPLE_DSIZEPAGE