1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

IMG5 17" REV F
11/15/05

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
F		410623	PRODUCTION RELEASED	11/16/05	?

PDF	CSA	CONTENTS	SYNC	MASTER	DATE
2	2	System Block Diagram		FINO-DD	06/20/2005
3	4	Power Block Diagram		FINO-PC	06/20/2005
4	5	Table Items		FINO-M23	08/26/2005
5	6	FUNC TEST 1 OF 2		FINO-ME	06/20/2005
6	7	Power Conn / Alias		M23-PC	06/20/2005
7	8	Signal Alias		FINO-DD	06/20/2005
8	9	FUNC TEST 2 OF 2		FINO-ME	06/20/2005
9	11	1.8V Vreg		M23-PC	06/20/2005
10	12	1.5V Vreg		FINO-PC	06/20/2005
11	13	1.2V Vreg		FINO-PC	06/20/2005
12	15	2.5V Vreg		FINO-PC	06/20/2005
13	16	5V & 3.3V Fets		FINO-PC	06/20/2005
14	17	Vesta Core / Misc		FINO-DC	06/20/2005
15	19	KODIAK CORE & BYPASS		Q63	08/01/2005
16	20	KODIAK & SHASTA MISC		FINO-ME	06/20/2005
17	23	Shasta Core Power		Q63	08/01/2005
18	24	Shasta Serial / Misc		FINO-ME	06/20/2005
19	25	PULSAR2 POWER		Q63	08/01/2005
20	26	PULSAR2 CLOCKS		FINO-ME	06/20/2005
21	27	Pulsar Aliases		FINO-ME	06/20/2005
22	28	System Management Unit		Q63	08/01/2005
23	29	SMU SUPPLEMENTAL (2)		FINO-HS	06/20/2005
24	30	SMU SUPPLEMENTAL (3)		FINO-HS	06/20/2005
25	31	SMU SUPPLEMENTAL (4)		FINO-HS	06/20/2005
26	32	Fan 0, 1 & System Temp		FINO-HS	06/20/2005
27	33	Fan 2 & HD Temp		FINO-HS	06/20/2005
28	39	I2C Connections		FINO-ME	06/20/2005
29	41	KODIAK EI PWR & CAPS		Q63	08/01/2005
30	42	KODIAK EI A		Q63	08/01/2005
31	43	CPU EI AND IO		FINO-HS	06/20/2005
32	44	KODIAK EI B		Q63	08/01/2005
33	47	CPU STRAPS		FINO-HS	06/20/2005
34	48	CPU POWER AND BYPASS		FINO-HS	06/20/2005
35	49	PROC DECOUPLING		FINO-HS	06/20/2005
36	50	CPU VCORE VREG		M23-HS	06/20/2005
37	52	CPU VCORE MORE BYPASS		FINO-HS	06/20/2005
38	54	CPU AVDD VREG		FINO-HS	06/20/2005
39	55	T,V,I SENSORS		FINO-HS	06/20/2005
40	56	CPU ALIASES & MISC		FINO-HS	06/20/2005
41	58	KODIAC NBMEM PWR & CAPS		Q63	08/01/2005
42	59	Kodiak Memory Dq/Ctl		FINO-DS	06/20/2005
43	61	Parallel Term		FINO-DS	06/20/2005
44	62	Main Memory Clock Buffer		FINO-DS	06/20/2005
45	63	MEMORY ADDR BRANCHING		FINO-DS	06/20/2005
46	67	Memory Dimm A		FINO-DS	06/20/2005
47	68	MLB Mem Series Term		FINO-DS	06/20/2005
48	69	On-Board DDR SDRAM		FINO-DS	06/20/2005
49	70	On-Board DDR SDRAM		FINO-DS	06/20/2005
50	82	KODIAK PCI-E X16		Q63	08/01/2005
51	84	GPU PCIe		M23-DD	06/20/2005
52	85	Graphics Vregs		M23-DD	06/20/2005
53	86	GPU Core Power		FINO-DD	06/20/2005
54	87	GPU Frame Buffer		FINO-DD	06/20/2005
55	88	FB Series Termination		FINO-DD	06/20/2005
56	89	GPU GDDR SDRAM A		FINO-DD	06/20/2005
57	90	GPU GDDR SDRAM B		FINO-DD	06/20/2005
58	92	GPU Straps		FINO-DD	06/20/2005
59	93	GPU DVI & DACs		FINO-DD	06/20/2005
60	96	TMDS/Inverter/ExtVGA		M23-DD	06/20/2005
61	97	KODIAK PCI-E CONST		FINO-DD	06/20/2005
62	98	KODIAK HT16		Q63	08/01/2005
63	101	HT ALIASES		FINO-ME	06/20/2005
64	103	Shasta HyperTransport		Q63	08/01/2005
65	119	Shasta PCI Interface		Q63	08/01/2005
66	120	PCI SERIES TERMINATION		FINO-MW	06/20/2005
67	121	AIRPORT & BLUETOOTH		FINO-MW	06/20/2005
68	122	USB 2.0 PCI Interface		Q63	08/01/2005
69	125	BootROM		Q63	08/01/2005
70	127	Shasta Disk		M23-DC	06/20/2005
71	129	Disk Connectors		M23-DC	06/20/2005
72	130	ENET SERIES TERM		FINO-DC	06/20/2005
73	131	Shasta Ethernet		Q63	08/01/2005
74	132	Vesta Ethernet PHY		Q63	08/01/2005
75	136	ETHERNET CONNECTOR		FINO-DC	06/20/2005
76	138	Shasta FireWire		Q63	08/01/2005
77	139	Vesta FireWire PHY		Q63	08/01/2005
78	140	FIREWIRE CONNECTORS		FINO-DC	06/20/2005
79	142	USB Host Interfaces		FINO-PC	07/05/2005
80	143	USB Device Interfaces		FINO-PC	06/20/2005
81	144	Flash Media Ctrl		FINO-PC	06/20/2005
82	145	Flash Connector		FINO-PC	06/20/2005
83	147	AUDIO: CODEC		FINO-SO	10/07/2005
84	148	AUDIO: LINE INPUT AMP		FINO-SO	10/07/2005
85	150	AUDIO: LINE OUT AMP		FINO-SO	10/07/2005
86	152	AUDIO: SPEAKER AMP		FINO-SO	10/07/2005
87	153	AUDIO: CONNECTORS		FINO-SO	10/07/2005
88	154	AUDIO: POWER SUPPLIES		FINO-SO	10/07/2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER | DESIGN CK | ENG APPD | MFG APPD | QA APPD | DESIGNER | RELEASE | SCALE NONE

MATERIAL/FINISH NOTED AS APPLICABLE

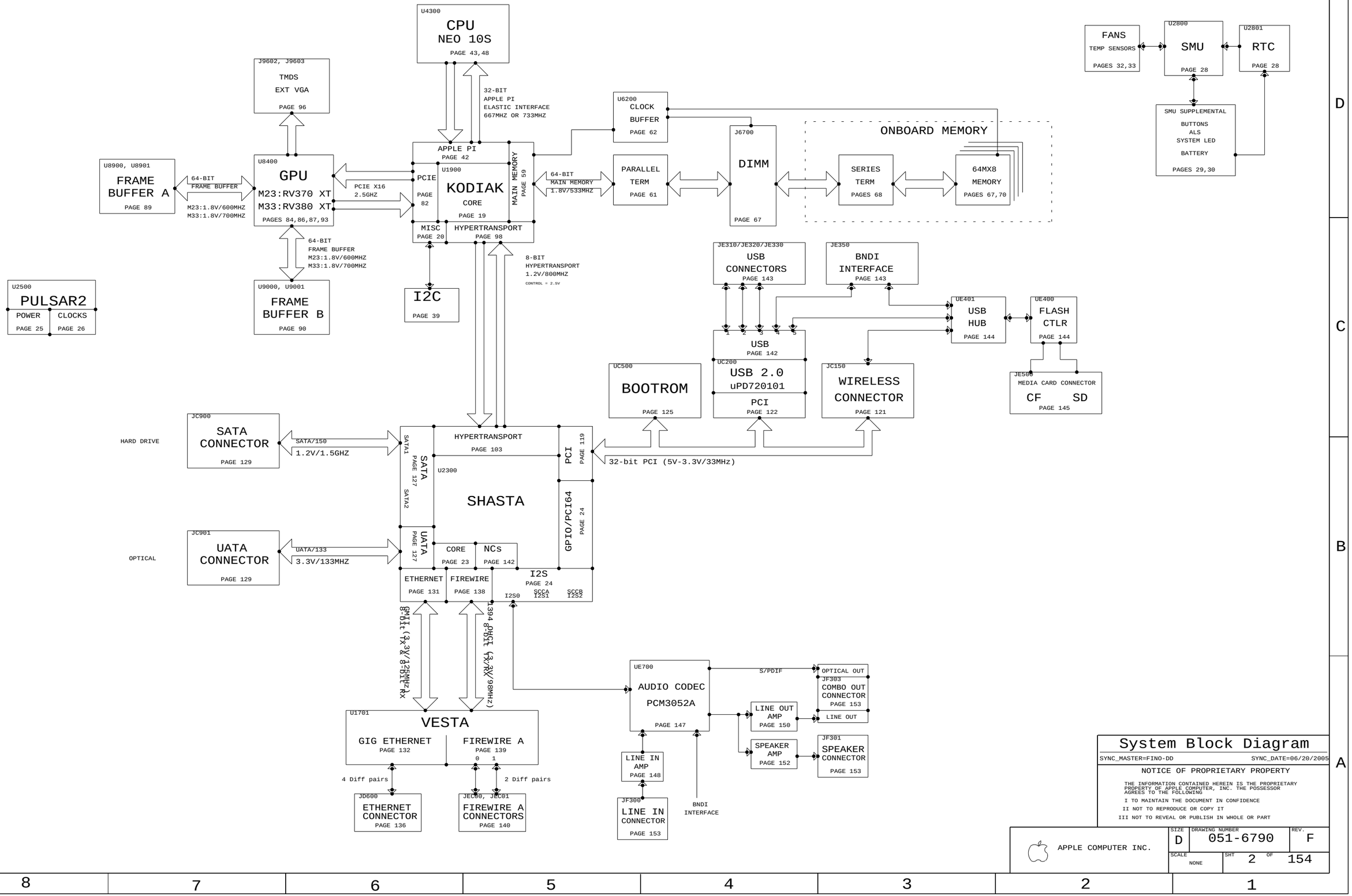
SIZE D

Apple Computer Inc.

TITLE
SCH,MLB,IMG5,17

DRAWING NUMBER 051-6790 REV. F

SHT 1 OF 154


U4300
CPU
NEO 10S
PAGE 43,48
32-BIT
APPLE PI
ELASTIC INTERFACE
667MHZ OR 733MHZ
J9602, J9603
TMDS
EXT VGA
PAGE 96
FANS
TEMP SENSORS
PAGES 32,33
U2800
SMU
PAGE 28
U2801
RTC
PAGE 28
SMU SUPPLEMENTAL
BUTTONS
ALS
SYSTEM LED
BATTERY
PAGES 29,30
U6200
CLOCK
BUFFER
PAGE 62
ONBOARD MEMORY
J6700
DIMM
PAGE 67
SERIES
TERM
PAGES 68
64MX8
MEMORY
PAGES 67,70
U8900, U8901
FRAME
BUFFER A
PAGE 89
64-BIT
FRAME BUFFER
M23:1.8V/600MHZ
M33:1.8V/700MHZ
U8400
GPU
M23:RV370 XT
M33:RV380 XT
PAGES 84,86,87,93
PCIE X16
2.5GHZ
APPLE PI
PAGE 42
PCIE
PAGE
82
U1900
KODIAK
CORE
PAGE 19
MAIN MEMORY
PAGE 59
64-BIT
MAIN MEMORY
1.8V/533MHZ
PARALLEL
TERM
PAGE 61
MISC
PAGE 20
HYPERTRANSPORT
PAGE 98
64-BIT
FRAME BUFFER
M23:1.8V/600MHZ
M33:1.8V/700MHZ
U9000, U9001
FRAME
BUFFER B
PAGE 90
8-BIT
HYPERTRANSPORT
1.2V/800MHZ
CONTROL = 2.5V
U2500
PULSAR2
POWER
PAGE 25
CLOCKS
PAGE 26
I2C
PAGE 39
JE310/JE320/JE330
USB
CONNECTORS
PAGE 143
JE350
BNDI
INTERFACE
PAGE 143
UE401
USB
HUB
PAGE 144
UE400
FLASH
CTLR
PAGE 144
USB
PAGE 142
UC200
USB 2.0
uPD720101
PCI
PAGE 122
UC500
BOOTROM
PAGE 125
JC150
WIRELESS
CONNECTOR
PAGE 121
JE500
MEDIA CARD CONNECTOR
CF
SD
PAGE 145
HARD DRIVE
JC900
SATA
CONNECTOR
PAGE 129
SATA/150
1.2V/1.5GHZ
HYPERTRANSPORT
PAGE 103
U2300
SHASTA
SATA1
SATA2
SATA
PAGE 127
PCI
PAGE 119
32-bit PCI (5V-3.3V/33MHz)
GPIO/PCI64
PAGE 24
OPTICAL
JC901
UATA
CONNECTOR
PAGE 129
UATA/133
3.3V/133MHZ
UATA
PAGE 127
CORE
PAGE 23
NCS
PAGE 142
ETHERNET
PAGE 131
FIREWIRE
PAGE 138
I2S
PAGE 24
SCCA
I2S1
SCCB
I2S2
I2S0
GMII (3.3V/125MHz)
8-bit Tx & 8-bit Rx
1394 PHY (3.3V/98MHz)
U1701
VESTA
GIG ETHERNET
PAGE 132
FIREWIRE A
PAGE 139
0
1
4 Diff pairs
2 Diff pairs
JD600
ETHERNET
CONNECTOR
PAGE 136
JEC00, JEC01
FIREWIRE A
CONNECTORS
PAGE 140
UE700
AUDIO CODEC
PCM3052A
PAGE 147
S/PDIF
OPTICAL OUT
JF303
COMBO OUT
CONNECTOR
PAGE 153
LINE OUT
LINE OUT
AMP
PAGE 150
SPEAKER
AMP
PAGE 152
JF301
SPEAKER
CONNECTOR
PAGE 153
LINE IN
AMP
PAGE 148
JF300
LINE IN
CONNECTOR
PAGE 153
BNDI
INTERFACE
System Block Diagram
SYNC_MASTER=FINO-DD
SYNC_DATE=06/20/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-6790
REV.
F
SCALE
NONE
SHT
2
OF
154

POWER CONNECTOR

J700
PAGE 7

SYS_POWERUP_L

PP12V_ALL — FW CONN
PP12V_RUN — 20" PANEL POWER, 17" LCD INVERTER
PP5V_RUN — OPTICAL
PP5V_ALL
PP3V3_ALL
PP3V3_RUN — PCI BUS, AUDIO CODEC

SMU

POWER SEQUENCE PIN

SYS_POWERUP_L
NC_SMU_PWRSEQ_P1_0 — SMU_PWRSEQ_P1_0
NC_SMU_PWRSEQ_P1_4 — SMU_PWRSEQ_P1_4
TURN_ON_PP1V2_L — SMU_PWRSEQ_P1_1
PWR_GOOD_PP1V5 — SMU_PWRSEQ_P9_5
PWR_GOOD_PP1V8 — SMU_PWRSEQ_P9_6
TURN_ON_PP3V3_PWRON_L — SMU_PWRSEQ_P1_2
SMU_PWRSEQ_P1_3
PP3V3_PWRON

PP1V5_PWRON SWITCHER
PAGE 12
PULSAR, KODIAK CORE

PP1V5_RUN FET SWITCH
PAGE 12
EI

CPU CORE SWITCHER
PAGE 50

GPU CORE SWITCHER
PAGE 85

PP1V8_PWRON SWITCHER
PAGE 11
MAIN MEMORY

PP1V8_RUN
IN
PP1V8_RUN POWER SW
PAGE 11
GPU MEMORY

PP0V9_GPU_VTT LINEAR
PAGE 91

PP4V5_RUN_AUDIO LINEAR
PAGE 154
AUDIO CODEC

PP5V_PWRON FET SWITCH
PAGE 16
USB CONN

PP3V3_PWRON FET SWITCH
PAGE 16
MODEM & BT, USB2 HOST

PP2V5_ALL LINEAR
PAGE 15
VESTA

PP2V5_PWRON FET SWITCH
PAGE 15

PP2V5_RUN FET SWITCH
PAGE 15

PP1V2_ALL SWITCHER
PAGE 13
VESTA CORE

PP2V5_RUN_CPU_AVDD LINEAR
PAGE 54

PP2V5_GPU_A2VDD LINEAR
PAGE 85

PP1V8_TPVDD LINEAR
PAGE 85

PP1V5_VDDC_CT LINEAR
PAGE 85

PP1V2_TPVDD LINEAR
PAGE 85

PP1V8_GPU LINEAR
PAGE 85

PP1V2_PWRON FET SWITCH
PAGE 13
SHASTA CORE

PP1V2_RUN FET SWITCH
PAGE 13
IN
HT BUS

PP2V5_ALL
R431 10K 5% 1/16W MF-LF 402

PP1V5_PWRON
R430 100K 5% 1/10W MF-LF 402
PS_1V_REF
COMPARE_PP1V5
LM339A SOI-LF
U400 V+ GND
C430 0.01UF 20% 16V CERM 402

PP2V5_ALL
R442 150K 5% 1/16W MF-LF 402
PS_1V_REF
PP5V_ALL
LM339A SOI-LF
U400 V+ GND
PP2V5_ALL
R441 10K 5% 1/16W MF-LF 402

R440 100K 5% 1/16W MF-LF 402
COMPARE_PP1V8
C440 0.01UF 20% 16V CERM 402
R443 100K 1% 1/10W MF-LF 402
C441 0.1UF 20% 10V CERM 402

PP2V5_ALL
U400P2
LM339A SOI-LF
U400 V+ GND

Power Block Diagram

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 4 OF 154	

PROCESSORS

NEED TO UPDATED BIN CODES AS NOTES

PART #	QTY	DEVICE	PACKAGE	DESCRIPTION	VALUE	VOLT.	WATT.	TOL.	REFERENCE DESIGNATOR(S)	BOM OPTION	
337S3224	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,1.9G,85C	1.9GHZ	1.10V	45W	50MV	U4300	17_INCH_LCD	CRITICAL
337S3220	1	PROCESSOR	CBGA-576-1MM	IC,GPUL,DD3.1,2.1G,85C	2.1GHZ	1.10V	45W	50MV	U4300	20_INCH_LCD	CRITICAL

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
337S3225	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.15V
337S3226	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.20V
337S3227	337S3224	17_INCH_LCD	U4300	IC,DD3.1,1.9G,1.25V
337S3228	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.15V
337S3229	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.20V
337S3230	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.25V
337S3231	337S3224	17_INCH_LCD	U4300	IC,DD3.0X,1.9G,1.30V
337S3221	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.15V
337S3222	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.20V
337S3223	337S3220	20_INCH_LCD	U4300	IC,DD3.1,2.1G,1.25V

ASICS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
343S0379	1	IC,KODIAK,V1.2,PBGA,200MM	U1900		CRITICAL
343S0377	1	IC,ASIC,SHASTA,V1.1,PBGA,LF	U2300		CRITICAL
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U1701		CRITICAL
343S0319	1	IC,PULSAR2,100P,P8MM,BGA	U2500		CRITICAL

MISC PARTS

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION		
051-6790	1	PCB,SCHEM,MLB,M23	SCH1	17_INCH_LCD		
051-6863	1	PCB,SCHEM,MLB,M33	SCH1	20_INCH_LCD		
820-1783	1	PCB,FAB,MLB,M23	MLB1	17_INCH_LCD	CRITICAL	
820-1766	1	PCB,FAB,MLB,M33	MLB1	20_INCH_LCD	CRITICAL	
062-2082	1	SPEC,VENDOR PACKAGING PROCEDURE	VPP1			
825-6447	1	BARCODE LABEL, MLB	LBL1			
341T1751	1	IC,FLASH,1MX8,3.3V,90NS	UC500		CRITICAL	
341T1752	1	PURCH ASSY, SMU BIG	U2800		CRITICAL	
603-7318	1	M23 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7321	1	M33 CPU HEATSINK	MECH1	OMIT	CRITICAL	
603-7319	1	M23 GPU HEATSINK	MECH2	OMIT	CRITICAL	HEATSINKS ARE NOW ON THE PD BOM
603-7322	1	M33 GPU HEATSINK	MECH2	OMIT	CRITICAL	
603-7320	1	M23 NB HEATSINK	MECH3	OMIT	CRITICAL	
603-7323	1	M33 NB HEATSINK	MECH3	OMIT	CRITICAL	
875-1905	1	CPU GAP FILLER	GAP1			
875-2429	1	LED COVER TAPE	TAPE1	17_INCH_LCD		

ALTERNATES

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
378S0140	378S0141		LED700,LED702	KINGBRIGHT LED
343S0388	343S0356		U1701	VESTA A4
126S0078	126S0086		C722	EL CAP
126S0068	126S0088		CF000	EL CAP
353S1321	353S1105		U400	LM339
138S0558	138S0547			10UF CAP ALL LOC.
124-0338	124-0333			PANASONIC CAPS

Table Items

SYNC_MASTER=FINO-M23 SYNC_DATE=08/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE NONE SHT 5 OF 154

NO TEST XW NETS

F97	NO_TEST=YES	GND_U1100	11
F98	NO_TEST=YES	GND_U1200	12
F99	NO_TEST=YES	GND_U1300	13
F90	NO_TEST=YES	PP_2V5PWRONNBMISC	20
F91	NO_TEST=YES	PP_1V2PWRONSBVCORE	23
F92	NO_TEST=YES	PP_3V3PWRONSBPCIG4	23
F93	NO_TEST=YES	PP_2V5PWRONSB	23
F94	NO_TEST=YES	PP_1V2PWRONSBPLL45VDD	24
F95	NO_TEST=YES	PP_OVDD_PULSAR1	25
F96	NO_TEST=YES	PP_1V2PWRONPULSAR1	25
F86	NO_TEST=YES	PP_1V5PULSAR2	25
F87	NO_TEST=YES	PP_1V5PWRONPULSAR2	25
F88	NO_TEST=YES	GND_SMU_AVSS	28 55
F89	NO_TEST=YES	PP_3V3ALLSMUAVCC	28
F90	NO_TEST=YES	PP_3V3ALLSMU	28
F91	NO_TEST=YES	PP_VEINB	41
F82	NO_TEST=YES	GND_CPU_AVDD	48
F83	NO_TEST=YES	VC_AGND	50
F84	NO_TEST=YES	VC_OUTSEN_R	50
F80	NO_TEST=YES	KPVDD2_FMAX	55
F85	NO_TEST=YES	GND_GPU_PVSS	86
F77	NO_TEST=YES	GND_GPU_MPVSS	87
F106	NO_TEST=YES	GND_AUDIO_MIC	153 154

F79	NO_TEST=YES	GND_GPU_TPVSS	93
F100	NO_TEST=YES	GND_GPU_TXVSSR	93
F92	NO_TEST=YES	GND_GPU_VSSDI	93
F101	NO_TEST=YES	GND_GPU_AVSSN	93
F102	NO_TEST=YES	GND_GPU_AVSSQ	93
F103	NO_TEST=YES	GND_GPU_A2VSSN	93
F104	NO_TEST=YES	GND_GPU_A2VSSQ	93
F105	NO_TEST=YES	KOD_L15_GND	98 101
F106	NO_TEST=YES	PP_3V3SBPCI_B9	
F107	NO_TEST=YES	PP_2V5PWRONSB_B9	119
F108	NO_TEST=YES	PP_VIOPCIUSB2_C2	122
F109	NO_TEST=YES	PP_1V2PWRONDISKSB_CC	127
F100	NO_TEST=YES	PP2V5_VESTA_BIASVDD1	132
F101	NO_TEST=YES	PP2V5_VESTA_XTALVDD1	132
F102	NO_TEST=YES	PP1V2_VESTA_PLLVDD1	132
F103	NO_TEST=YES	PP1V2_VESTA_PLLVDD2	139
F104	NO_TEST=YES	PP2V5_VESTA_BIASVDD2	139
F105	NO_TEST=YES	PP2V5_VESTA_XTALVDD2	139
F106	NO_TEST=YES	PP1V2_VESTA_FAVDDL	139
F107	NO_TEST=YES	PP2V5_VESTA_FAVDDM	139
F108	NO_TEST=YES	PP3V3_VESTA_FAVDDH	139
F109	NO_TEST=YES	PP3V3_PWRON_NEC_AVDD	142
F110	NO_TEST=YES	GND_AUD_LOAMP	150 154

F101	NO_TEST=YES	GND_NEC_AVSS_R	142
F107	NO_TEST=YES	GND_AUDIO_SPKRAMP_PLANE	152 154
F101	NO_TEST=YES	GND_AUDIO_CODEC	147 148 150 154
F101	NO_TEST=YES	KPGND2_FMAX	55
F101	NO_TEST=YES	TDIODE_POS_FMAX	55
F101	NO_TEST=YES	TDIODE_NEG_FMAX	55
F101	NO_TEST=YES	DAGND	55
F101	NO_TEST=YES	INA138_OUT	55
F102	NO_TEST=YES	RAMCLK_AVSS	62
F105	NO_TEST=YES	PP12V_AUDIO_SPKRAMP	7 152
F105	NO_TEST=YES	GND_AUDIO	7 154
F105	NO_TEST=YES	GND_AUDIO_SPKRAMP	7 152 154
F101	NO_TEST=YES	KOD_H05_GND	82 97
F101	NO_TEST=YES	KOD_K07_GND	82 97
F101	NO_TEST=YES	KOD_G10_GND	82 97
F101	NO_TEST=YES	KOD_J13_GND	82 97
F101	NO_TEST=YES	KOD_L13_GND	82 97
F101	NO_TEST=YES	KOD_H08_GND	82 97
F101	NO_TEST=YES	PCIE_SLOTA_PRSNT_L	82 84
F101	NO_TEST=YES	U8500_GND	85
F101	NO_TEST=YES	GND_AUD_LOAMP_CHGPMP	150 154

EE IDENTIFIED NO TEST NETS

F955	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_P	56
F957	NO_TEST=YES	NC_EI_NB_TO_CPU_B_CLK_N	56
F958	NO_TEST=YES	NC_EI_NB_TO_CPU_B_AD<0..43>	56
F959	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_P<0..1>	56
F960	NO_TEST=YES	NC_EI_NB_TO_CPU_B_SR_N<0..1>	56
F961	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_P	56
F962	NO_TEST=YES	NC_EI_CPU_B_TO_NB_CLK_N	56
F963	NO_TEST=YES	NC_EI_CPU_B_TO_NB_AD<0..43>	56
F964	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_P<0..1>	56
F965	NO_TEST=YES	NC_EI_CPU_B_TO_NB_SR_N<0..1>	56
F969	NO_TEST=YES	NC_NB_CPU_A1_INT_L	56
F971	NO_TEST=YES	NC_NB_CPU_B0_INT_L	56
F972	NO_TEST=YES	NC_NB_CPU_B1_INT_L	56
F973	NO_TEST=YES	NC_CPU_A1_QACK_L	56
F976	NO_TEST=YES	NC_CPU_B0_QACK_L	56
F974	NO_TEST=YES	NC_CPU_B1_QACK_L	56
F976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_P<8..15>	101
F976	NO_TEST=YES	NC_HT_MB_TO_NB_CAD_N<8..15>	101
F977	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_P<8..15>	101
F982	NO_TEST=YES	NC_HT_NB_TO_MB_CAD_N<8..15>	101
F102	NO_TEST=YES	NC_CLK_RAI_200M_N<0>	27
F102	NO_TEST=YES	NC_CLK_RAI_200M_P<0>	27
F104	NO_TEST=YES	NC_CLK_RAI_PCIEA_N<0>	27
F104	NO_TEST=YES	NC_CLK_RAI_PCIEA_P<0>	27
F104	NO_TEST=YES	NC_CLK_RAI_PCIEB_N<0>	27
F105	NO_TEST=YES	NC_CLK_RAI_PCIEB_P<0>	27
F105	NO_TEST=YES	NC_CLK_RAI_PCIEC_N<0>	27
F105	NO_TEST=YES	NC_CLK_RAI_PCIEC_P<0>	27
F105	NO_TEST=YES	NC_A_AVREG_0	82
F105	NO_TEST=YES	NC_A_AVREG_1	82
F105	NO_TEST=YES	NC_A_AVREG_2	82
F105	NO_TEST=YES	NC_CPU_B_APSYNC	27
F106	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_N	27
F106	NO_TEST=YES	NC_EI_CPU_B_SYSCLK_P	27
F106	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_N<1>	101
F106	NO_TEST=YES	NC_HT_NB_TO_MB_CLK_P<1>	101
F100	NO_TEST=YES	NC_J2904_11	29
F100	NO_TEST=YES	NC_J2904_12	29
F100	NO_TEST=YES	NC_NCV1009_1	55
F100	NO_TEST=YES	NC_NCV1009_2	55
F100	NO_TEST=YES	NC_NCV1009_3	55
F100	NO_TEST=YES	NC_NCV1009_4	55
F100	NO_TEST=YES	NC_NCV1009_5	55
F100	NO_TEST=YES	NC_NCV1009_ADJ	55
F108	NO_TEST=YES	NC_RAM_ARB0_REF25MHZ	27
F107	NO_TEST=YES	NC_RAM_ARB1_REF25MHZ	27
F107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_0	4
F107	NO_TEST=YES	NC_SMU_PWRSEQ_P1_4	4
F116	NO_TEST=YES	RFBD<38>	88 89
F116	NO_TEST=YES	RFBD<37>	88 89
F116	NO_TEST=YES	RFBD<36>	88 89
F116	NO_TEST=YES	RFBD<34>	88 89
F116	NO_TEST=YES	RFBD<33>	88 89
F116	NO_TEST=YES	RFBD<32>	88 89
F116	NO_TEST=YES	RFBD<31>	88 89
F116	NO_TEST=YES	RFBD<30>	88 89
F117	NO_TEST=YES	RFBD<28>	88 89
F117	NO_TEST=YES	RFBD<27>	88 89
F117	NO_TEST=YES	RFBD<26>	88 89
F117	NO_TEST=YES	RFBD<25>	88 89
F117	NO_TEST=YES	RFBD<23>	88 89
F117	NO_TEST=YES	RFBD<22>	88 89
F117	NO_TEST=YES	RFBD<21>	88 89

F109	NO_TEST=YES	KPVDD2	48 50 55
F109	NO_TEST=YES	KPGND2	48 50 55
F109	NO_TEST=YES	CPU_DIODE_POS	48 55
F109	NO_TEST=YES	CPU_DIODE_NEG	48 55
F110	NO_TEST=YES	FMAXT_P	55
F110	NO_TEST=YES	FMAXT_M	55
F110	NO_TEST=YES	CORE_ISNS_P	55
F110	NO_TEST=YES	CORE_ISNS_M	55
F110	NO_TEST=YES	PPV_RUN_CPU_AVDD_R_L	48
F110	NO_TEST=YES	NC_CLK_RAI_GIGE_25MHZ	27
F110	NO_TEST=YES	NC_CLK_RAI_REFCLK_66M	27
F110	NO_TEST=YES	NC_CPU_B_TBEN_CLK_US	26
F110	NO_TEST=YES	NC_PMR_CLK_DIS_L	20
F110	NO_TEST=YES	NC_I2S2_MCLK	154
F111	NO_TEST=YES	NC_SATA_RXD_N2_C	129
F111	NO_TEST=YES	NC_SATA_RXD_P2_C	129
F111	NO_TEST=YES	NC_SATA_TXD_N2	129
F111	NO_TEST=YES	NC_SATA_TXD_P2	129
F111	NO_TEST=YES	TP_SB<29>	142
F111	NO_TEST=YES	TP_SB<28>	142
F111	NO_TEST=YES	TP_SB<27>	142
F111	NO_TEST=YES	TP_SB<26>	142
F111	NO_TEST=YES	TP_SB<25>	142
F112	NO_TEST=YES	TP_SB<24>	142
F112	NO_TEST=YES	TP_SB<23>	142
F112	NO_TEST=YES	TP_SB<22>	142
F112	NO_TEST=YES	TP_SB<21>	142
F112	NO_TEST=YES	TP_SB<20>	142
F112	NO_TEST=YES	TP_SB<19>	142
F112	NO_TEST=YES	TP_SB<18>	142
F112	NO_TEST=YES	TP_SB<17>	142
F112	NO_TEST=YES	TP_SB<16>	142
F112	NO_TEST=YES	TP_SB<15>	142
F113	NO_TEST=YES	TP_SB<14>	142
F113	NO_TEST=YES	TP_SB<13>	142
F113	NO_TEST=YES	TP_SB<12>	142
F113	NO_TEST=YES	TP_SB<11>	142
F113	NO_TEST=YES	TP_SB<10>	142
F113	NO_TEST=YES	TP_SB<9>	142
F113	NO_TEST=YES	TP_SB<8>	142
F113	NO_TEST=YES	TP_SB<7>	142
F113	NO_TEST=YES	TP_SB<6>	142
F113	NO_TEST=YES	TP_SB<5>	142
F114	NO_TEST=YES	TP_SB<4>	142
F114	NO_TEST=YES	TP_SB<3>	142
F114	NO_TEST=YES	TP_SB<2>	142
F114	NO_TEST=YES	TP_SB<1>	142
F114	NO_TEST=YES	TP_SB<0>	142
F115	NO_TEST=YES	RFBD<61>	88 89
F115	NO_TEST=YES	RFBD<60>	88 89
F115	NO_TEST=YES	RFBD<59>	88 89
F117	NO_TEST=YES	RFBD<57>	88 89
F118	NO_TEST=YES	RFBD<56>	88 89
F118	NO_TEST=YES	RFBD<54>	88 89
F118	NO_TEST=YES	RFBD<53>	88 89
F118	NO_TEST=YES	RFBD<52>	88 89
F118	NO_TEST=YES	RFBD<50>	88 89
F118	NO_TEST=YES	RFBD<49>	88 89
F118	NO_TEST=YES	RFBD<48>	88 89
F118	NO_TEST=YES	RFBD<47>	88 89
F119	NO_TEST=YES	RFBD<45>	88 89
F119	NO_TEST=YES	RFBD<44>	88 89
F119	NO_TEST=YES	RFBD<42>	88 89
F119	NO_TEST=YES	RFBD<41>	88 89
F119	NO_TEST=YES	RFBD<40>	88 89

F119	NO_TEST=YES	RFBD<126>	88 90
F120	NO_TEST=YES	RFBD<125>	88 90
F119	NO_TEST=YES	RFBD<124>	88 90
F120	NO_TEST=YES	RFBD<122>	88 90
F120	NO_TEST=YES	RFBD<121>	88 90
F120	NO_TEST=YES	RFBD<120>	88 90
F120	NO_TEST=YES	RFBD<118>	88 90
F120	NO_TEST=YES	RFBD<117>	88 90
F120	NO_TEST=YES	RFBD<116>	88 90
F121	NO_TEST=YES	RFBD<114>	88 90
F122	NO_TEST=YES	RFBD<113>	88 90
F121	NO_TEST=YES	RFBD<112>	88 90
F121	NO_TEST=YES	RFBD<110>	88 90
F122	NO_TEST=YES	RFBD<109>	88 90
F121	NO_TEST=YES	RFBD<108>	88 90
F122	NO_TEST=YES	RFBD<106>	88 90
F122	NO_TEST=YES	RFBD<105>	88 90
F121	NO_TEST=YES	RFBD<104>	88 90
F122	NO_TEST=YES	RFBD<102>	88 90
F122	NO_TEST=YES	RFBD<101>	88 90
F122	NO_TEST=YES	RFBD<100>	88 90
F122	NO_TEST=YES	RFBD<98>	88 90
F122	NO_TEST=YES	RFBD<97>	88 90
F122	NO_TEST=YES	RFBD<96>	88 90
F122	NO_TEST=YES	RFBD<95>	88 90
F123	NO_TEST=YES	RFBD<94>	88 90
F123	NO_TEST=YES	RFBD<92>	88 90
F123	NO_TEST=YES	RFBD<91>	88 90
F123	NO_TEST=YES	RFBD<90>	88 90
F123	NO_TEST=YES	RFBD<88>	88 90
F123	NO_TEST=YES	RFBD<87>	88 90
F123	NO_TEST=YES	RFBD<86>	88 90
F123	NO_TEST=YES	RFBD<85>	88 90
F124	NO_TEST=YES	RFBD<83>	88 90
F124	NO_TEST=YES	RFBD<82>	88 90
F124	NO_TEST=YES	RFBD<81>	88 90
F124	NO_TEST=YES	RFBD<79>	88 90
F124	NO_TEST=YES	RFBD<78>	88 90
F124	NO_TEST=YES	RFBD<76>	88 90
F124	NO_TEST=YES	RFBD<75>	88 90
F124	NO_TEST=YES	RFBD<74>	88 90
F125	NO_TEST=YES	RFBD<72>	88 90
F125	NO_TEST=YES	RFBD<71>	88 90
F125	NO_TEST=YES	RFBD<70>	88 90
F125	NO_TEST=YES	RFBD<69>	88 90
F125	NO_TEST=YES	RFBD<67>	88 90
F125	NO_TEST=YES	RFBD<66>	88 90
F125	NO_TEST=YES	RFBD<65>	88 90
F126	NO_TEST=YES	RFBD<62>	88 90

F80	NO_TEST=YES	TP_FBBCS1_L	87
F82	NO_TEST=YES	AUD_4V5_FB	154
F83	NO_TEST=YES	ITS_RUNNING	7
F83	NO_TEST=YES	LED801_1	8
F83	NO_TEST=YES	LED802_1	8
F84	NO_TEST=YES	PCI_CLK66M_SB_INT_R	26
F84	NO_TEST=YES	Q800_D	8
F84	NO_TEST=YES	Q800_G	8
F84	NO_TEST=YES	Q801_B	8
F84	NO_TEST=YES	Q802_B	8
F85	NO_TEST=YES	Q802_E	8
F85	NO_TEST=YES	Q803_B	8
F42	NO_TEST=YES	TP_USB2_PWREN<0>	143
F42	NO_TEST=YES	TP_USB2_PWREN<1>	143
F87	NO_TEST=YES	TP_SB_FSTEST	24
F87	NO_TEST=YES	TP_SB_PLLTEST	24
F84	NO_TEST=YES	TP_USB2_PWREN<2>	143
F84	NO_TEST=YES	TP_USB2_PWREN<3>	143
F84	NO_TEST=YES	TP_USB2_PWREN<4>	143
F85	NO_TEST=YES	TP_NEC_NTEST1	122
F85	NO_TEST=YES	TP_NEC_SMC	122
F85	NO_TEST=YES	TP_NEC_SMI_L	122
F86	NO_TEST=YES	TP_NEC_SRCLK	122
F86	NO_TEST=YES	TP_NEC_SRMOD	122
F86	NO_TEST=YES	TP_NEC_TEST	122
F88	NO_TEST=YES	UATA_DASP_L_DS	129
F120	NO_TEST=YES	RFBD<19>	88 89
F120	NO_TEST=YES	RFBD<18>	88 89
F120	NO_TEST=YES	RFBD<16>	88 89
F120	NO_TEST=YES	RFBD<15>	88 89
F120	NO_TEST=YES	RFBD<14>	88 89
F120	NO_TEST=YES	RFBD<13>	88 89
F127	NO_TEST=YES	RFBD<11>	88 89
F127	NO_TEST=YES	RFBD<10>	88 89
F127	NO_TEST=YES	RFBD<8>	88 89
F127	NO_TEST=YES	RFBD<7>	88 89
F127	NO_TEST=YES	RFBD<6>	88 89
F127	NO_TEST=YES	RFBD<5>	88 89
F127	NO_TEST=YES	RFBD<3>	88 89
F128	NO_TEST=YES	RFBD<2>	88 89
F128	NO_TEST=YES	RFBD<1>	88 89
F128	NO_TEST=YES	RAM_DQ_R<63>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<60>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<59>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<58>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<57>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<56>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<54>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<53>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<52>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<50>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<49>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<48>	61 68 70
F128	NO_TEST=YES	RAM_DQ_R<46>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<45>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<44>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<43>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<41>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<40>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<37>	61 68 70
F130	NO_TEST=YES	RAM_DQ_R<38>	61 68 70
F131	NO_TEST=YES	RAM_DQ_R<36>	61 68 70
F131	NO_TEST=YES	RAM_DQ_R<34>	61 68 70
F131	NO_TEST=YES	RAM_DQ_R<33>	61 68 70
F131	NO_TEST=YES	RAM_DQ_R<32>	61 68 70
F133	NO_TEST=YES	RAM_DQ_R<30>	61 68 69
F133	NO_TEST=YES	RAM_DQ_R<29>	61 68 69
F133	NO_TEST=YES	RAM_DQ_R<28>	61 68 69
F133	NO_TEST=YES	RAM_DQ_R<31>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<25>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<24>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<22>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<21>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<20>	61 68 69
F132	NO_TEST=YES	RAM_DQ_R<19>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<17>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<16>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<14>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<13>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<12>	61 68 69
F135	NO_TEST=YES	RAM_DQ_R<11>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<9>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<8>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<7>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<6>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<5>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<3>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<2>	61 68 69
F134	NO_TEST=YES	RAM_DQ_R<1>	61 68 69

FUNC TEST NETS

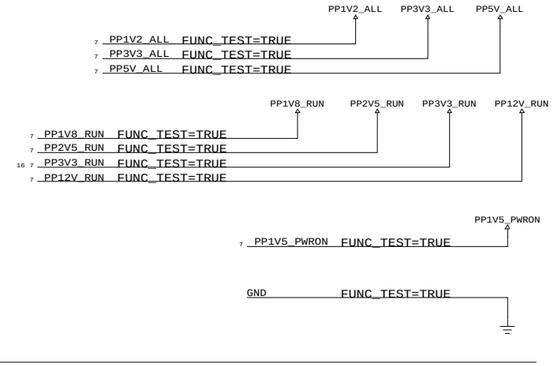
NOTES FROM TOM FUSSELMAN

PLACE TWO TEST POINTS ON TOP SIDE
FOR PP3V3_ALL AND GND
PLACE WITHIN 1 INCH OF EACH OTHER
USE FAT TRACES

F108	FUNC_TEST=TRUE	PPVCORE_CPU	50
F108	FUNC_TEST=TRUE	=PP3V3_ALL_SMU	7 28 29
F108	FUNC_TEST=TRUE	=PP5V_RUN_CPU	7 8
F105	FUNC_TEST=TRUE	SYS_POWER_BUTTON_L	28 29
F105	FUNC_TEST=TRUE	POWER_BUTTON_L	29
F105	FUNC_TEST=TRUE	RESET_BUTTON_L	29
F105	FUNC_TEST=TRUE	SMU_RESET_L	28 29
F105	FUNC_TEST=TRUE	SYS_POWERUP_L	7 12 28 50 85

TOP SIDE ONLY

F138	FUNC_TEST=TRUE	SMU_BOOT_SCLK	28 29
F138	FUNC_TEST=TRUE	SMU_BOOT_RXD	28 29
F138	FUNC_TEST=TRUE	SMU_BOOT_CE	28 29
F138	FUNC_TEST=TRUE	SMU_BOOT_CNVSS	28 29
F138	FUNC_TEST=TRUE	SMU_BOOT_TXD	28 29
F138	FUNC_TEST=TRUE	SMU_BOOT_BUSY	28 29
F105	FUNC_TEST=TRUE	SMU_MANUAL_RESET_L	29

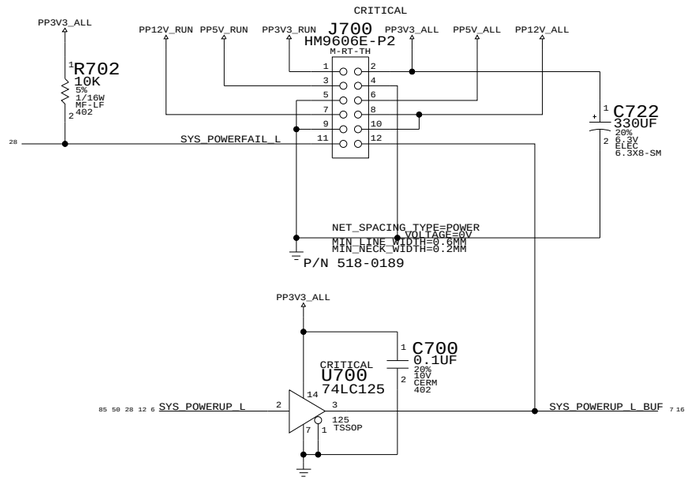


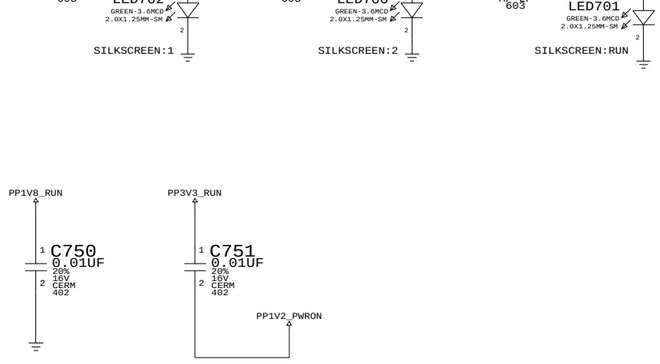
FUNC TEST 1 OF 2

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 6 OF 154	





RUN RAILS

ONLY ON IN RUN

PP12V_RUN
PP12V_RUN VOLTAGE=12V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER =PP12V_GPU

XW701 SM
XW705 SM
XW708 SM
XW700 SM
PP12V_AUDIO_SPKRAMP
PP5V_RUN VOLTAGE=5V MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
PP5V_AUDIO_ANALOG
=PP5V_PATA
=PP5V_RUN_CPU

PP3V3_RUN
PP3V3_RUN VOLTAGE=3.3V MIN_LINE_WIDTH=0.3MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP3V3_GPU
=PP3V3_AUDIO
=PP3V3_RUN_CPU
=PP3V3_PATA
=PP3V3_SB_PCI
=PP3V3_PCI
=PPVIO_PCI_USB2
=PP3V3_RUN_PULSAR
=PP3V3_RUN_SB_PCI
PP3V3_RUN_SB
=PP3V3_RUN_I2C
=PP3V3_RUN_SMU
TO MATCH Q63

PP2V5_RUN
PP2V5_RUN MAKE_BASE=TRUE VOLTAGE=2.5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
NBC
=PP2V5_RUN_I2C

PP1V8_RUN
PP1V8_RUN VOLTAGE=1.8V MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PPV_GPU_MEM
=PP1V8_RUN_RAM

PP1V5_RUN
PP1V5_RUN VOLTAGE=1.5V MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PPV_EI_CPU
=PPV_EI_NB
=PPOVDD_PULSAR

PPVCORE_GPU MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM NET_SPACING_TYPE=POWER
=PP1V2_GPU_PCIE

PP1V2_RUN
PP1V2_RUN VOLTAGE=1.2V MAKE_BASE=TRUE MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER

PP3V3_RUN
R790
33
5%
1/8W
MF-LF
805
Q790D
3V3_RUN LEAKAGE FIX
Q790
2N7002
SOT23-LF
SYS_POWERUP_L_BUF

PWRON RAILS

ON IN RUN AND SLEEP

PP5V_PWRON
PP5V_PWRON VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP5V_PWRON_USB
=PP5V_PWRON_BNDI

PP3V3_PWRON
PP3V3_PWRON VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP3V3_PWRON_SB
=PP3V3_PWRON_SB_PCI64
=PP3V3_PWRON_SB_PCI32
=PP3V3_PWRON_PULSAR
=PP3V3_PWRON_USB
=PP3V3_PWRON_BT
=PP3V3_PWRON_CPU
=PP3V3_ENET
=PP3V3_PWRON_SMU
=PP3V3_PWRON_BNDI

PP2V5_PWRON
PP2V5_PWRON VOLTAGE=2.5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP2V5_PWRON_SB
=PP2V5_PWRON_PULSAR
=PP2V5_ENET
=PP2V5_PWRON_NB_HT
=PP2V5_PWRON_NB_PCIE
=PP2V5_PWRON_HT
=PP2V5_PWRON_NB_MISC

PP1V8_PWRON
PP1V8_PWRON MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=2.5V MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP1V8_PWRON_NBMEM
=PP1V8_PWRON_RAM
=PP1V8_PWRON_DIMM
=PP1V8_PWRON_RAM_I2C_VDD

NOSTUFF
R711
0
5%
1/16W
MF-LF
402
PP1V5_PWRON
PP1V5_PWRON MAKE_BASE=TRUE VOLTAGE=1.5V MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM NET_SPACING_TYPE=POWER
=PPVCORE_PWRON_NB
=PPVCORE_PWRON_NB_PCIE
=PPVCORE_PWRON_NB_HT
PP1V2_PWRON
PP1V2_PWRON MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM VOLTAGE=1.2V MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP1V2_PWRON_SB_HT
=PP1V2_PWRON_DISK_SB
=PP1V2_PWRON_SB
=PP1V2_PWRON_SB_VCORE
=PP1V2_PWRON_PULSAR
=PP1V2_PWRON_HT_NBTX
PP1V5_PWRON_PULSAR VOLTAGE=1.5V MIN_LINE_WIDTH=0.5MM MIN_NECK_WIDTH=0.25MM MAKE_BASE=TRUE
=PP1V5_PWRON_PULSAR
=PP1V5_PULSAR
=PPV_PWRON_NB_REFCLK

ALL RAILS

ALWAYS ON WHEN UNIT HAS AC POWER (TRICKLE)

PP12V_ALL
PP12V_ALL MAKE_BASE=TRUE VOLTAGE=12V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PP12V_ALL_GPU
=PP12V_ALL_FW
PP5V_ALL
=PP12V_CPU

PP5V_ALL
PP5V_ALL VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
=PP5V_ALL_GPU
PP3V3_ALL
PP3V3_ALL MAKE_BASE=TRUE VOLTAGE=3.3V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PP3V3_ALL_SMU
=PP3V3_ALL_CPU
=PP3V3_FW
=PP3V3_ENETFW
=PP3V3_ALL_GPU
PP2V5_ALL
PP2V5_ALL MAKE_BASE=TRUE VOLTAGE=2.5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PP2V5_ENETFW
PP1V2_ALL
PP1V2_ALL MAKE_BASE=TRUE VOLTAGE=1.2V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.2MM NET_SPACING_TYPE=POWER
=PP1V2_VESTA
=PP1V2_ENETFW

GND RAILS

XW702 SM
GND_AUDIO
XW706 SM
XW703 SM
GND_AUDIO_SPKRAMP
XW707 SM

CHASSIS GND

GND_CHASSIS_TO_LEFT MIN_NECK_WIDTH=0.2MM MAKE_BASE=TRUE VOLTAGE=0 MIN_LINE_WIDTH=0.6MM NET_SPACING_TYPE=POWER
GND_CHASSIS_AUDIO_EXTERNAL
NOSTUFF
R721
0
5%
1/16W
MF-LF
402
GND_CHASSIS_USB
GND_CHASSIS_FIREWIRE
GND_CHASSIS_VGA
GND_CHASSIS_RJ45
GND_CHASSIS_TO_RIGHT MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM VOLTAGE=0 MAKE_BASE=TRUE NET_SPACING_TYPE=POWER
GND_CHASSIS_AUDIO_INTERNAL
OMIT
ZH706
160R138
GND_CHASSIS_BNDI MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM VOLTAGE=0 MAKE_BASE=TRUE NET_SPACING_TYPE=POWER

OMIT
ZH704
4P25R3P5
ZH704P1
OMIT
ZH701
4P25R3P5
ZH701P1
NOSTUFF
C704
0.01UF
NOSTUFF
C701
0.01UF
OMIT
ZH702
4P25R3P5
ZH702P1
NOSTUFF
C702
0.01UF
OMIT
ZH703
4P25R3P5
ZH703P1
NOSTUFF
C703
0.01UF

Power Conn / Alias

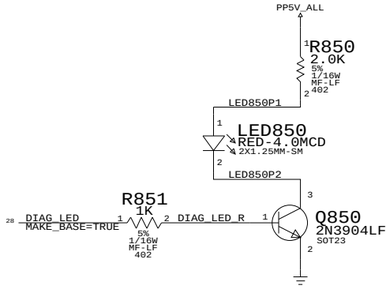
SYNC_MASTER=M23-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

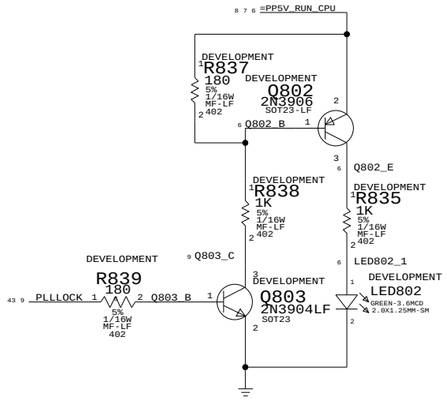
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 7 OF 154	

DIAG LED

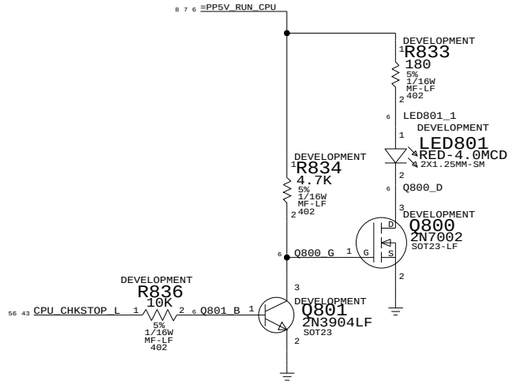
(OVERTEMP LED)



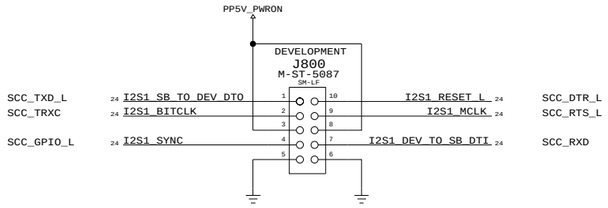
PLL LOCK LED



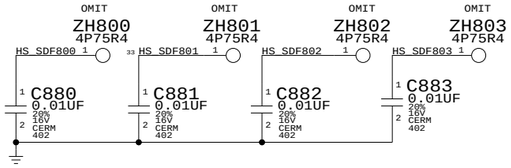
CHKSTOP LED



SERIAL DEBUG



CPU HEATSINK MOUNTING HOLES



Signal Alias

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 8 OF 154	

T1	NO_TEST=YES	ENET_TXD_R<7>	130 131
T2	NO_TEST=YES	ENET_TXD_R<6>	130 131
T3	NO_TEST=YES	ENET_TXD_R<5>	130 131
T4	NO_TEST=YES	ENET_TXD_R<4>	130 131
T5	NO_TEST=YES	ENET_TXD_R<3>	130 131
T6	NO_TEST=YES	ENET_TXD_R<2>	130 131
T7	NO_TEST=YES	ENET_TXD_R<1>	130 131
T8	NO_TEST=YES	ENET_TXD_R<0>	130 131
T9	NO_TEST=YES	ENET_TXD<7>	130 131 132
T10	NO_TEST=YES	ENET_TXD<6>	130 131 132
T12	NO_TEST=YES	ENET_TXD<5>	130 131 132
T11	NO_TEST=YES	ENET_TXD<4>	130 131 132
T13	NO_TEST=YES	ENET_TXD<3>	130 131 132
T14	NO_TEST=YES	ENET_TXD<2>	130 131 132
T15	NO_TEST=YES	ENET_TXD<1>	130 131 132
T16	NO_TEST=YES	ENET_TXD<0>	130 131 132
T18	NO_TEST=YES	ENET_RXD_R<7>	130 131 132
T17	NO_TEST=YES	ENET_RXD_R<6>	130 131 132
T19	NO_TEST=YES	ENET_RXD_R<5>	130 131 132
T20	NO_TEST=YES	ENET_RXD_R<4>	130 131 132
T21	NO_TEST=YES	ENET_RXD_R<3>	130 131 132
T22	NO_TEST=YES	ENET_RXD_R<2>	130 131 132
T24	NO_TEST=YES	ENET_RXD_R<1>	130 131 132
T23	NO_TEST=YES	ENET_RXD_R<0>	130 131 132
T25	NO_TEST=YES	ENET_RXD<7>	130 131
T26	NO_TEST=YES	ENET_RXD<6>	130 131
T27	NO_TEST=YES	ENET_RXD<5>	130 131
T28	NO_TEST=YES	ENET_RXD<4>	130 131
T30	NO_TEST=YES	ENET_RXD<3>	130 131
T29	NO_TEST=YES	ENET_RXD<2>	130 131
T31	NO_TEST=YES	ENET_RXD<1>	130 131
T32	NO_TEST=YES	ENET_RXD<0>	130 131
T33	NO_TEST=YES	ENET_TX_EN_R	130 131
T34	NO_TEST=YES	ENET_TX_ER_R	130 131
T36	NO_TEST=YES	ENET_TX_EN	130 131 132
T35	NO_TEST=YES	ENET_TX_ER	130 131 132
T37	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_N<1>	101
T38	NO_TEST=YES	TP_HT_MB_TO_NB_CLK_P<1>	101
T39	NO_TEST=YES	NC_CPU_AFN	56
T40	NO_TEST=YES	NC_I2C_SMU_CPU_SCL_IN	31
T42	NO_TEST=YES	NC_PSRO	56
T41	NO_TEST=YES	NC_PSRO_ENABLE	56
T43	NO_TEST=YES	NC_SLOT_TOTAL_PWR	31
T44	NO_TEST=YES	NC_SMU_CPU_VID_LE0	31
T45	NO_TEST=YES	NC_SMU_CPU_VID_LE1	31
T46	NO_TEST=YES	NC_SMU_FAN_RPM3	31
T48	NO_TEST=YES	NC_SMU_FAN_RPM4	31
T47	NO_TEST=YES	NC_SMU_FAN_RPM5	31
T49	NO_TEST=YES	NC_SMU_FAN_TACH3	31
T50	NO_TEST=YES	NC_SMU_FAN_TACH4	31
T51	NO_TEST=YES	NC_SMU_FAN_TACH5	31
T52	NO_TEST=YES	NC_SMU_FAN_TACH7	31
T54	NO_TEST=YES	NC_SMU_SER_SEL	31
T53	NO_TEST=YES	NC_SYS_DOOR_AJAR_L	31
T55	NO_TEST=YES	TP_VESTA_2_5V_EN	17
T56	NO_TEST=YES	TP_VESTA_AN_EN	132
T57	NO_TEST=YES	TP_VESTA_DNC_C9	17
T58	NO_TEST=YES	TP_VESTA_DNC_E9	17
T60	NO_TEST=YES	TP_VESTA_EN_10B	132
T59	NO_TEST=YES	TP_VESTA_ER	132
T61	NO_TEST=YES	TP_VESTA_F1000	132
T62	NO_TEST=YES	TP_VESTA_FDX	132
T63	NO_TEST=YES	TP_VESTA_FDXLED_L	132
T64	NO_TEST=YES	TP_VESTA_HUB	132
T66	NO_TEST=YES	TP_VESTA_LINK1_L	132
T65	NO_TEST=YES	TP_VESTA_LINK2_L	132
T67	NO_TEST=YES	TP_VESTA_MANMS	132
T68	NO_TEST=YES	TP_VESTA_PHYA<0>	132
T69	NO_TEST=YES	TP_VESTA_PHYA<1>	132
T70	NO_TEST=YES	TP_VESTA_PHYA<2>	132
T72	NO_TEST=YES	TP_VESTA_PHYA<3>	132
T71	NO_TEST=YES	TP_VESTA_PHYA<4>	132
T73	NO_TEST=YES	TP_VESTA_RBC0	132
T74	NO_TEST=YES	TP_VESTA_RBC1	132
T76	NO_TEST=YES	TP_VESTA_REGCTL1	17
T76	NO_TEST=YES	TP_VESTA_REGCTL2	17
T78	NO_TEST=YES	TP_VESTA_REGSEN1	17
T77	NO_TEST=YES	TP_VESTA_REGSEN2	17
T79	NO_TEST=YES	TP_VESTA_REGSUP1	17
T80	NO_TEST=YES	TP_VESTA_REGSUP2	17
T81	NO_TEST=YES	TP_VESTA_RGMIIEN	132
T82	NO_TEST=YES	TP_VESTA_SPD0	132
T84	NO_TEST=YES	TP_VESTA_TDBL<0>	139
T83	NO_TEST=YES	TP_VESTA_TDBL<1>	139
T85	NO_TEST=YES	TP_VESTA_TDBL<2>	139
T86	NO_TEST=YES	TP_VESTA_TEST<0>	132
T87	NO_TEST=YES	TP_VESTA_TEST<1>	132
T88	NO_TEST=YES	TP_VESTA_TEST_1394<0>	139
T90	NO_TEST=YES	TP_VESTA_TEST_1394<1>	139
T89	NO_TEST=YES	TP_VESTA_TVCO	132
T222	NO_TEST=YES	CARD_READER_ACTIVITY_R	144
T223	NO_TEST=YES	TP_VESTA_FAVDDL	139
T224	NO_TEST=YES	TP_NB_A_TRIGGER_OUT	56
T225	NO_TEST=YES	TP_NB_B_TRIGGER_OUT	56

T91	NO_TEST=YES	TP_VESTA_TVCO_24	139
T92	NO_TEST=YES	TP_VESTA_TXC_RXC_DELAY	132
T93	NO_TEST=YES	TP_I2S2_SB_TO_DEV_DTO	154
T94	NO_TEST=YES	TP_NB_APSYNC	44
T95	NO_TEST=YES	TP_SB_WATCHDOG	24
T96	NO_TEST=YES	NC_CPU_TBEN_CLK	
T97	NO_TEST=YES	NC_J3108_10	31
T98	NO_TEST=YES	NC_J3108_11	31
T99	NO_TEST=YES	NC_J3108_12	31
T100	NO_TEST=YES	NC_J3108_8	31
T101	NO_TEST=YES	NC_J3108_9	31
T102	NO_TEST=YES	NC_JTAGMUX_3	30
T103	NO_TEST=YES	NC_PP1V5_PULSAR	12

THE FOLLOWING NETS ARE USED ONLY
WHEN THE DEVELOPMENT BOM OPTION IS ENABLED

T109	NO_TEST=YES	Q803_C	8
T109	NO_TEST=YES	PLLLOCK	8 43

T111	NO_TEST=YES	LED_PP1V8_RUN_P	11
T112	NO_TEST=YES	LED_PP1V8_RUN_N	11
T113	NO_TEST=YES	PP1V5_RUN_FOR_LED	12
T114	NO_TEST=YES	LED_PP1V5_RUN_N	12
T115	NO_TEST=YES	LED_PP1V5_RUN_P	12
T116	NO_TEST=YES	PULSAR_1V5_RUN_SWITCH	12
T120	NO_TEST=YES	PP1V2_RUN_FOR_LED	13
T121	NO_TEST=YES	LED_PP1V2_RUN_N	13
T122	NO_TEST=YES	LED_PP1V2_RUN_P	13
T123	NO_TEST=YES	KP_V<1>	55
T124	NO_TEST=YES	KP_V<2>	55
T125	NO_TEST=YES	CPU_SENSE_KP_V	55
T126	NO_TEST=YES	NB_PLL_OUT_TRG_R	
T127	NO_TEST=YES	NB_PLL_OUT_TRG	59
T128	NO_TEST=YES	PP5V_T555	
T131	NO_TEST=YES	T555_DISC	
T132	NO_TEST=YES	T555_THRES	
T129	NO_TEST=YES	T555_OUT	
T133	NO_TEST=YES	T555_PWM	
T134	NO_TEST=YES	PP3V3_GPU_TSENSE	93
T135	NO_TEST=YES	TSENSE_GPU_OVERTEMP_L	93
T136	NO_TEST=YES	TSENSE_GPU_ADD0	93
T138	NO_TEST=YES	TSENSE_GPU_ADD1	93
T137	NO_TEST=YES	GPU_DIODE_PLUS	93
T139	NO_TEST=YES	GPU_DIODE_MINUS	93
T140	NO_TEST=YES	LED8700_P	136
T140	NO_TEST=YES	LED8701_P	136

THE FOLLOWING PULSAR NETS WILL BE
TESTED VIA TEST JET

T143	NO_TEST=YES	CPU_A_TBEN_CLK_R	26
T144	NO_TEST=YES	CPU_B_TBEN_CLK_R	26
T145	NO_TEST=YES	CPU_A_APSYNC_R	26
T146	NO_TEST=YES	CPU_B_APSYNC_R	26
T148	NO_TEST=YES	NB_APSYNC_R	26
T149	NO_TEST=YES	HT_SB_REFCLK_R	26
T147	NO_TEST=YES	HT_NB_REFCLK_H0_R	26
T150	NO_TEST=YES	HT_NB_REFCLK_L0_R	26
T151	NO_TEST=YES	CLK_RAIREF_200M_P_R	26
T152	NO_TEST=YES	CLK_RAIREF_200M_N_R	26
T153	NO_TEST=YES	NB_PMR_CLK_P_R	26
T155	NO_TEST=YES	NB_PMR_CLK_N_R	26
T154	NO_TEST=YES	NB_PCIE_REFCLK_P_C	26
T156	NO_TEST=YES	NB_PCIE_REFCLK_N_C	26
T158	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_P_C	26
T159	NO_TEST=YES	GFX_SLOT_PCIE_REFCLK_N_C	26
T157	NO_TEST=YES	PCIE_A_REFCLKIN_P_C	26
T160	NO_TEST=YES	PCIE_A_REFCLKIN_N_C	26
T161	NO_TEST=YES	PCIE_B_REFCLKIN_P_C	26
T162	NO_TEST=YES	PCIE_B_REFCLKIN_N_C	26
T163	NO_TEST=YES	PCIE_C_REFCLKIN_P_C	26
T164	NO_TEST=YES	PCIE_C_REFCLKIN_N_C	26
T165	NO_TEST=YES	NB_DDR_REFCLK_P_R	26
T166	NO_TEST=YES	NB_DDR_REFCLK_N_R	26
T167	NO_TEST=YES	CLK_RAI_GIGE_25MHZ_R	26
T168	NO_TEST=YES	QUA0_REF_25MHZ_R	26
T169	NO_TEST=YES	SB_CLK25M_SATA_R	26
T170	NO_TEST=YES	QUA1_REF_25MHZ_R	26
T171	NO_TEST=YES	PCI_CLK33M_SB_EXT_R	26
T172	NO_TEST=YES	SB_AIRPRT_CLK_33MHZ_R	26
T173	NO_TEST=YES	CLK_RAI_REFCLK_66M_R	26
T174	NO_TEST=YES	SB_USB2_CLK_33MHZ_R	26

THE FOLLOWING NETS DO NOT HAVE
TEST POINT BECAUSE OF ROUTING DENSITY
AND SIGNAL INTEGRITY.
TEST COVERAGE WILL BE BY FCT
NOTE FOR SHARING: DO NOT INCLUDE THIS LIST UNTIL
PCB LAYOUT ADDS TEST POINTS. THIS LIST IS A RESULT OF PCB
LAYOUT HAVING DIFFICULTY PLACING TEST POINTS ON THESE NETS

T177	NO_TEST=YES	100M_N<0>	82 97
T178	NO_TEST=YES	100M_P<0>	82 97
T179	NO_TEST=YES	CKA_N<0>	84 97
T176	NO_TEST=YES	CKA_P<0>	84 97
T177	NO_TEST=YES	HT_NB_N<0>	98 101
T178	NO_TEST=YES	HT_NB_P<0>	98 101
T179	NO_TEST=YES	HT_NB_REFCLK_NF<0>	98 101
T180	NO_TEST=YES	HT_NB_REFCLK_PF<0>	98 101
T185	NO_TEST=YES	HT_NB_TO_SB_CAD_N<0..7>	101
T187	NO_TEST=YES	HT_NB_TO_SB_CAD_P<0..7>	101
T186	NO_TEST=YES	HT_NB_TO_SB_CLK_P<0>	101
T184	NO_TEST=YES	HT_NB_TO_SB_CLK_N<0>	101
T188	NO_TEST=YES	HT_SB_TO_NB_CAD_N<0..7>	101
T189	NO_TEST=YES	HT_SB_TO_NB_CAD_P<0..7>	101
T187	NO_TEST=YES	HT_SB_TO_NB_CLK_P<0>	101
T188	NO_TEST=YES	HT_SB_TO_NB_CLK_N<0>	101
T190	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
T191	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97
T192	NO_TEST=YES	UATA_DA<0>	127 129
T193	NO_TEST=YES	UATA_DD<1>	127 129
T194	NO_TEST=YES	UATA_DD<14>	127 129
T195	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0>	9 82 84 97
T196	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<3>	9 82 84 97
T197	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<13>	9 82 97
T198	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<7>	9 82 97
T199	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<1>	9 82 84 97
T200	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<10>	9 82 84 97
T201	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<13>	9 82 97
T202	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<14>	9 82 97
T203	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<12>	9 82 97
T204	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<10>	9 82 97
T205	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<4>	9 82 97
T206	NO_TEST=YES	HT_MB_TO_NB_CTL_N<1>	98
T208	NO_TEST=YES	HT_MB_TO_NB_CTL_P<1>	98
T207	NO_TEST=YES	HT_NB_TO_MB_CTL_N<1>	98
T209	NO_TEST=YES	HT_NB_TO_MB_CTL_P<1>	98
T210	NO_TEST=YES	HT_NB_TO_SB_CTL_N<0>	101
T211	NO_TEST=YES	HT_SB_TO_NB_CTL_P<0>	101
T213	NO_TEST=YES	CLK_KOD_100M_NF<0>	82 97
T212	NO_TEST=YES	CLK_KOD_100M_PF<0>	82 97
T214	NO_TEST=YES	EI_CPU_TO_NB_CLK_N	43 56
T216	NO_TEST=YES	EI_CPU_TO_NB_CLK_P	43 56
T215	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
T218	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
T217	NO_TEST=YES	EI_NB_TO_CPU_CLK_N	43 56
T219	NO_TEST=YES	EI_NB_TO_CPU_CLK_P	43 56
T221	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
T220	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56
T227	NO_TEST=YES	PLLTESTOUT	43 47
T228	NO_TEST=YES	UATA_DD<13>	127 129
T229	NO_TEST=YES	CPU_SPARE2	43 47
T208	NO_TEST=YES	RFBD<51>	88 89
T209	NO_TEST=YES	TP_CPU_TRIGGER_OUT	56
T207	NO_TEST=YES	UATA_DD<12>	127 129
T210	NO_TEST=YES	EI_CPU_SYSCLK_P	43 56
T204	NO_TEST=YES	EI_CPU_TO_NB_SR_N<1>	9 43 56
T205	NO_TEST=YES	EI_CPU_TO_NB_SR_P<1>	9 43 56
T206	NO_TEST=YES	EI_NB_TO_CPU_SR_N<0>	9 43 56
T203	NO_TEST=YES	EI_NB_TO_CPU_SR_P<0>	9 43 56

JTAG TEST POINTS NEED TO BE ON THE BOTTOM
OF THE BOARD
ADDING FUNC_TEST=TRUE TO THESE NETS

T220	FUNC_TEST=TRUE	TP_JTAG_SB_TCK	20
T222	FUNC_TEST=TRUE	TP_JTAG_SB_TDI	20
T226	FUNC_TEST=TRUE	TP_JTAG_SB_TDO	20
T224	FUNC_TEST=TRUE	TP_JTAG_SB_TMS	20
T230	FUNC_TEST=TRUE	JTAG_SB_TRST_L	20 24

T232	FUNC_TEST=TRUE	JTAG_NB_TCK	20 30
T234	FUNC_TEST=TRUE	JTAG_NB_TDI	20 30
T233	FUNC_TEST=TRUE	JTAG_NB_TDO	20 30
T236	FUNC_TEST=TRUE	JTAG_NB_TMS	20 30
T231	FUNC_TEST=TRUE	JTAG_NB_TRST_L	20

T239	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDI	17
T240	FUNC_TEST=TRUE	TP_JTAG_VESTA_TDO	17
T238	FUNC_TEST=TRUE	TP_JTAG_VESTA_TCK	17
T242	FUNC_TEST=TRUE	TP_JTAG_VESTA_TMS	17
T241	FUNC_TEST=TRUE	TP_JTAG_VESTA_TRST_L	17

T244	FUNC_TEST=TRUE	JTAG_CPU_TCK	30 43
T246	FUNC_TEST=TRUE	JTAG_CPU_TDI	30 43
T245	FUNC_TEST=TRUE	JTAG_CPU_TDO	30 43 47
T248	FUNC_TEST=TRUE	JTAG_CPU_TMS	30 43
T247	FUNC_TEST=TRUE	JTAG_CPU_TRST_L	43 47

ADDING NO_TEST TO ALL PCIE NETS
TO AVOID STUBS
WILL GET COVERAGE IN FCT WITH A DIAG
THAT CHECKS THAT THE BUS IS 16 LANES WIDE

T240	NO_TEST=YES	PCIE_NB_TO_SLOTA_NF<0..15>	9 82 97
T250	NO_TEST=YES	PCIE_NB_TO_SLOTA_PF<0..15>	9 82 97
T251	NO_TEST=YES	PCIE_NB_TO_SLOTA_N<0..15>	9 82 84 97
T252	NO_TEST=YES	PCIE_NB_TO_SLOTA_P<0..15>	9 82 84 97
T253	NO_TEST=YES	PCIE_SLOTA_TO_NB_NF<0..15>	84 97
T254	NO_TEST=YES	PCIE_SLOTA_TO_NB_PF<0..15>	84 97
T255	NO_TEST=YES	PCIE_SLOTA_TO_NB_N<0..15>	9 82 84 97
T256	NO_TEST=YES	PCIE_SLOTA_TO_NB_P<0..15>	9 82 84 97

FUNC TEST 2 OF 2

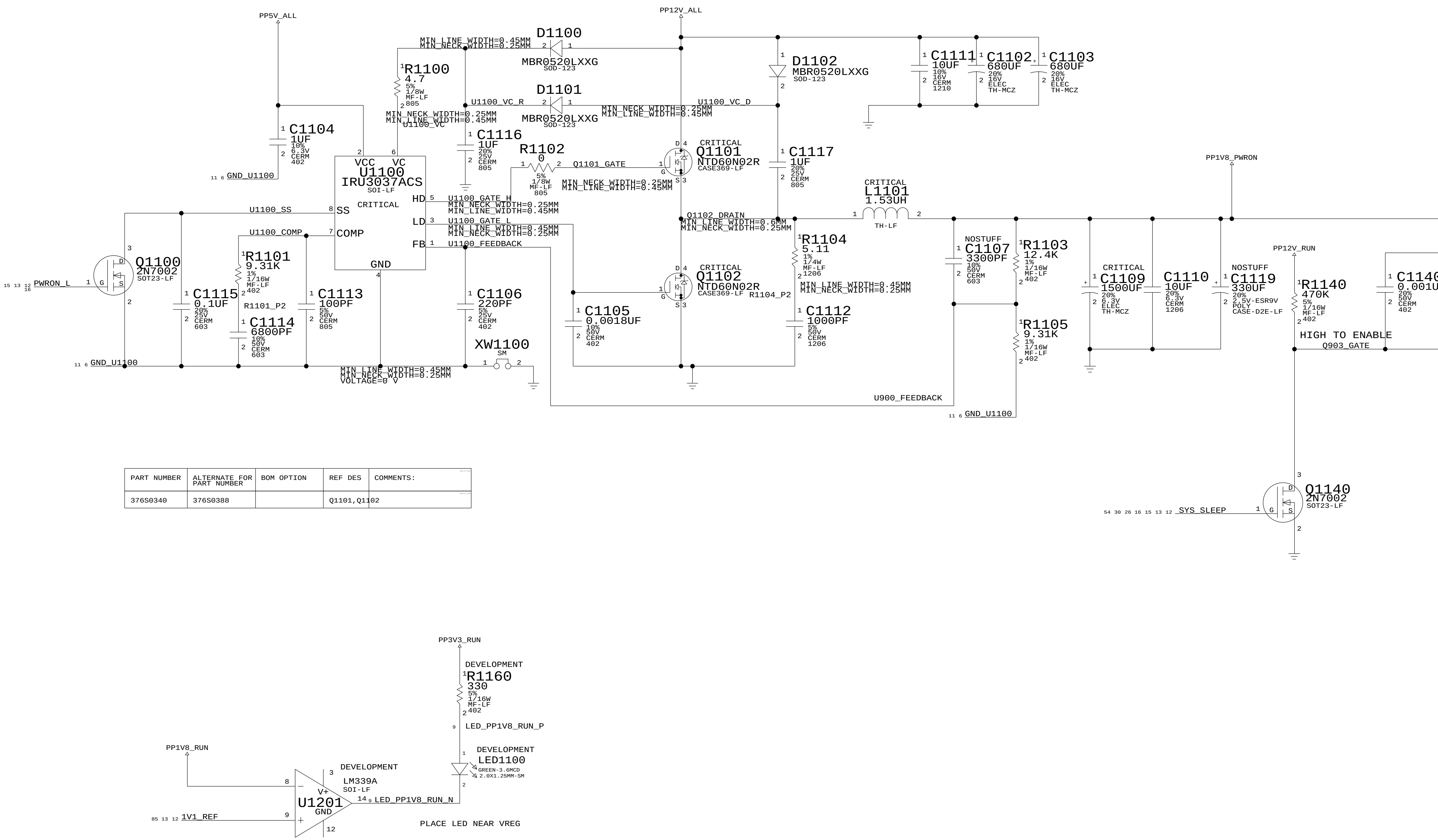
SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE: NONE SHT 9 OF 154

1.8V VOLTAGE REGULATOR



NOTE:
SET OUTPUT=1.85V FOR FRAMEBUFFER.
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R903+R905)/R905=1.85VDC

POWER BUDGET CURRENT OF TOTAL RAILS
9.8A PEAK
6.7A CONTINUOUS

POWER BUDGET CURRENT OF FET
7.4A PEAK
4.5A CONTINUOUS

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1101,Q1102	

1.8V Vreg

SYNC_MASTER=M23-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE NONE	SHT 11 OF 154	

KODIAK CORE VOLTAGE REGULATOR

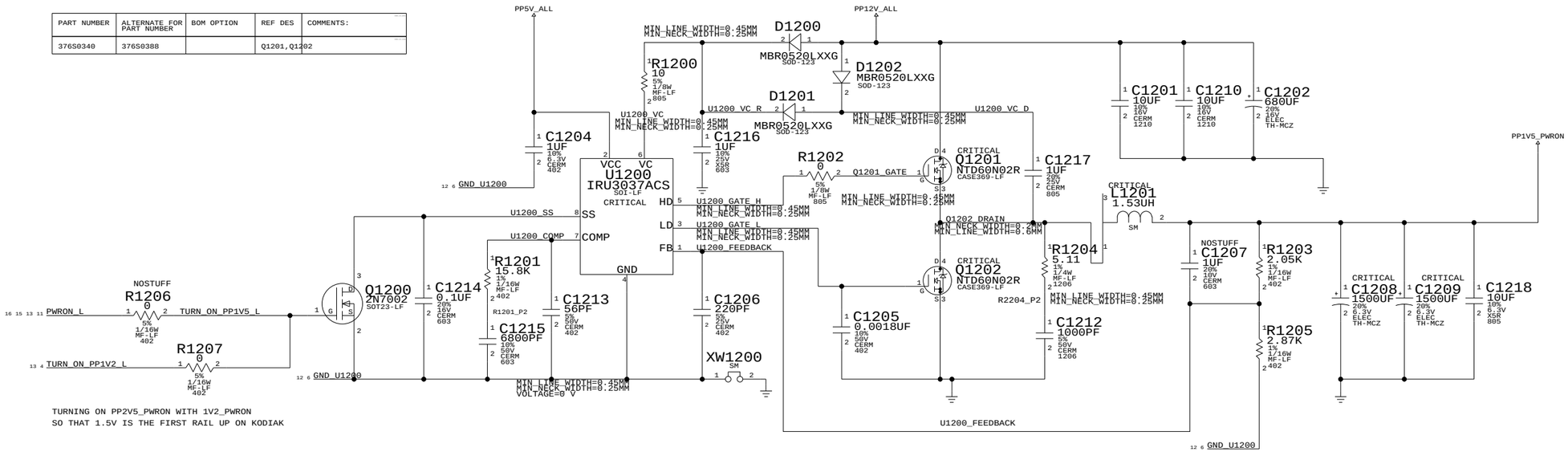
NOTE:

IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1203+R1205)/R1205=1.25VDC

LOAD FROM POWER BUDGET
8.5A PEAK CURRENT DRAW
7.2A CONTINUOUS CURRENT DRAW

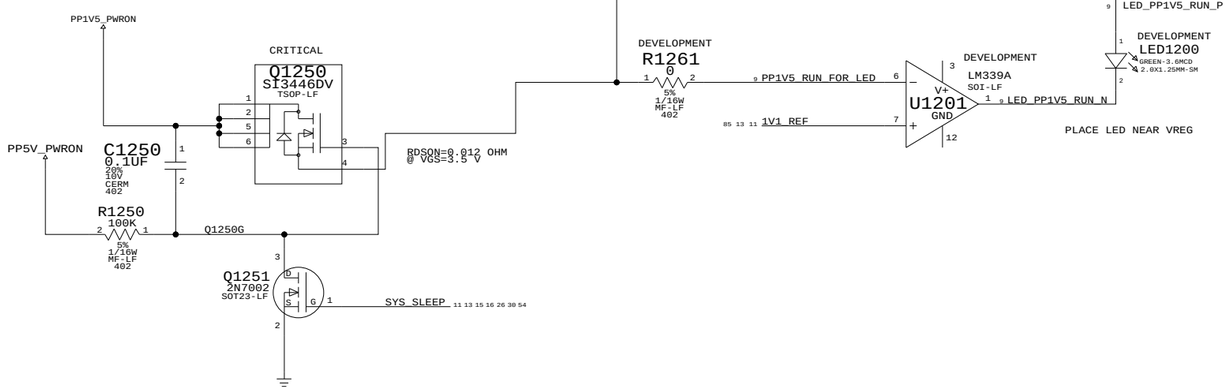
1.35V	R1205=2.87K
1.30V	R1205=3.24K
1.25V	R1205=3.65K

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q1201,Q1202	

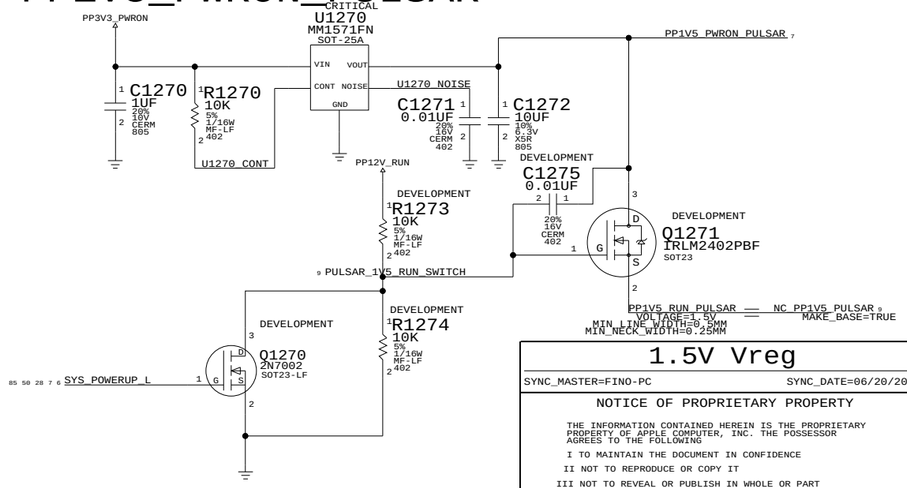


TURNING ON PP2V5_PWRON WITH 1V2_PWRON
SO THAT 1.5V IS THE FIRST RAIL UP ON KODIAK

LOAD FROM POWER BUDGET
1.3A PEAK CURRENT DRAW
1.0A CONTINUOUS CURRENT DRAW



PP1V5_PWRON_PULSAR



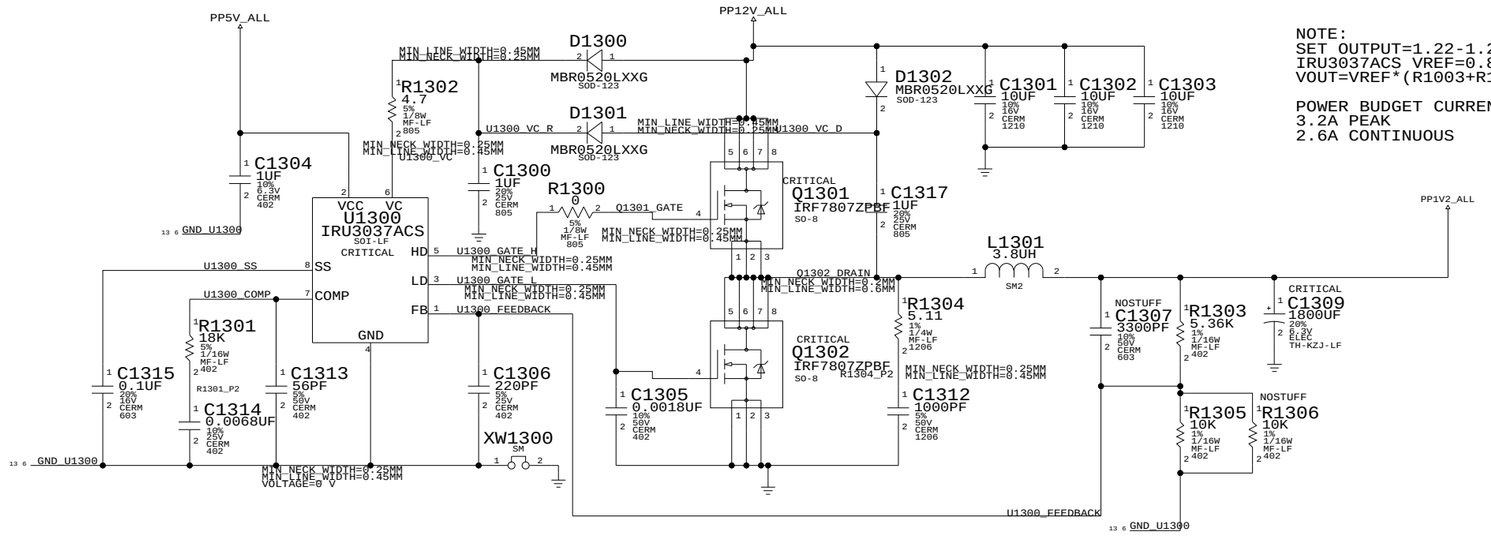
1.5V Vreg

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 12 OF 154	

PP1V2_ALL VOLTAGE REGULATOR

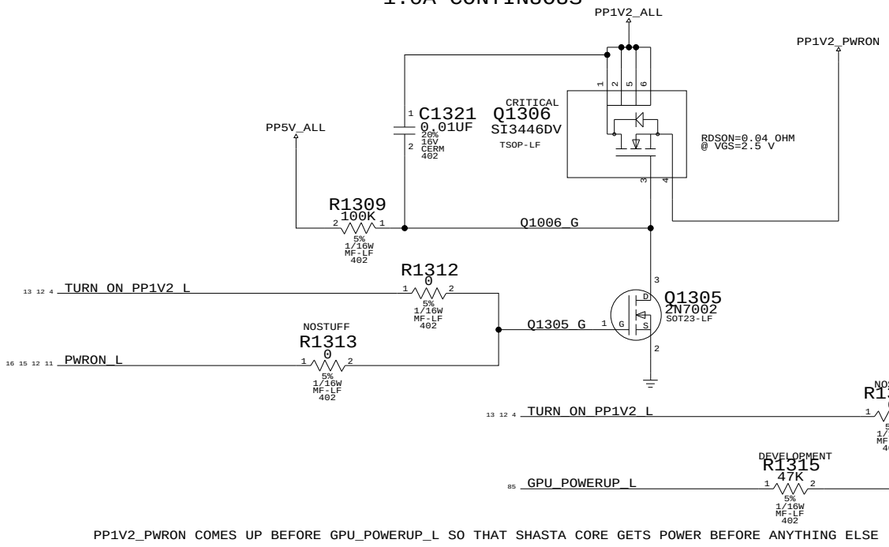


NOTE:
SET OUTPUT=1.22-1.23V
IRU3037ACS VREF=0.8VDC
VOUT=VREF*(R1003+R1005)/R1005=1.22-1.23VDC

POWER BUDGET CURRENT OF TOTAL RAILS
3.2A PEAK
2.6A CONTINUOUS

PP1V2_PWRON FET SWITCH

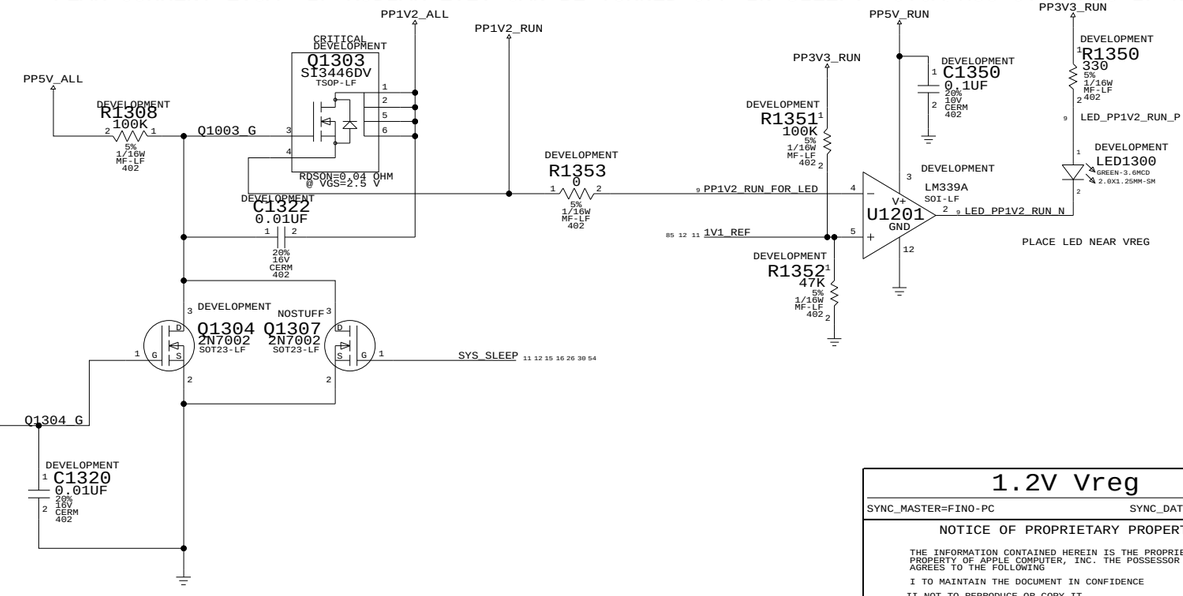
PEAK CURRENT 1.3A
1.0A CONTINUOUS



PP1V2_PWRON COMES UP BEFORE GPU_POWERUP_L SO THAT SHASTA CORE GETS POWER BEFORE ANYTHING ELSE

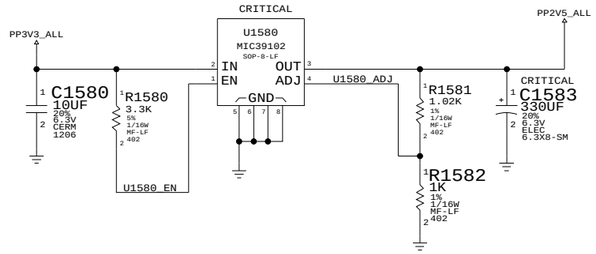
PP1V2_RUN FET SWITCH

PEAK CURRENT 1.3A IF KODIAK 1.2V CAN BE TURNED OFF IN SLEEP. 0.6A/M33 0.0A/M23 IF NOT



1.2V Vreg			
SYNC_MASTER=FINO-PC	SYNC_DATE=06/20/2005		
NOTICE OF PROPRIETARY PROPERTY			
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART			
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6790	REV. F
	SCALE NONE	SHT 13 OF 154	

PP2V5_ALL VOLTAGE REGULATOR

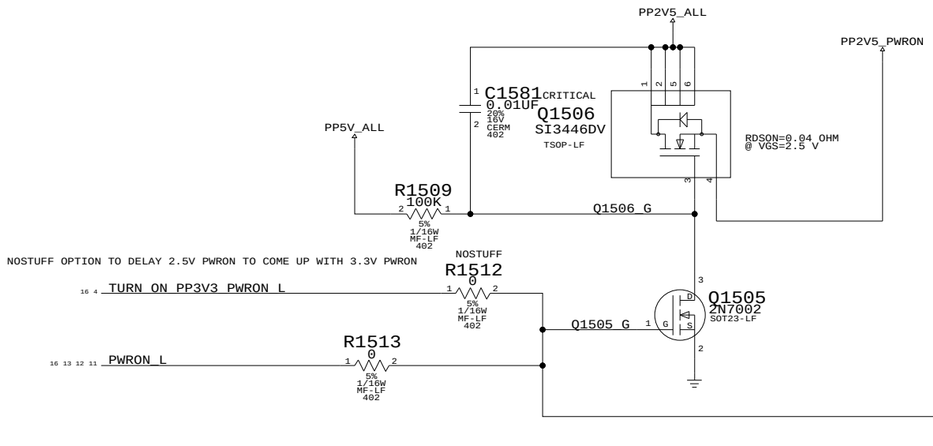


NOTE:
SET OUTPUT=2.5V
IRU3037CS VREF=1.24VDC
VOUT=VREF*(R1581+R1582)+1=5.505VDC

POWER BUDGET CURRENT OF TOTAL RAILS
0.2A PEAK
0.1A CONTINUOUS

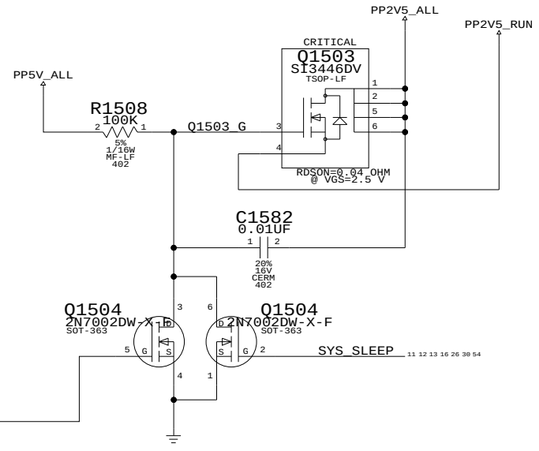
PP2V5_PWRON FET SWITCH

PEAK CURRENT 0.1A



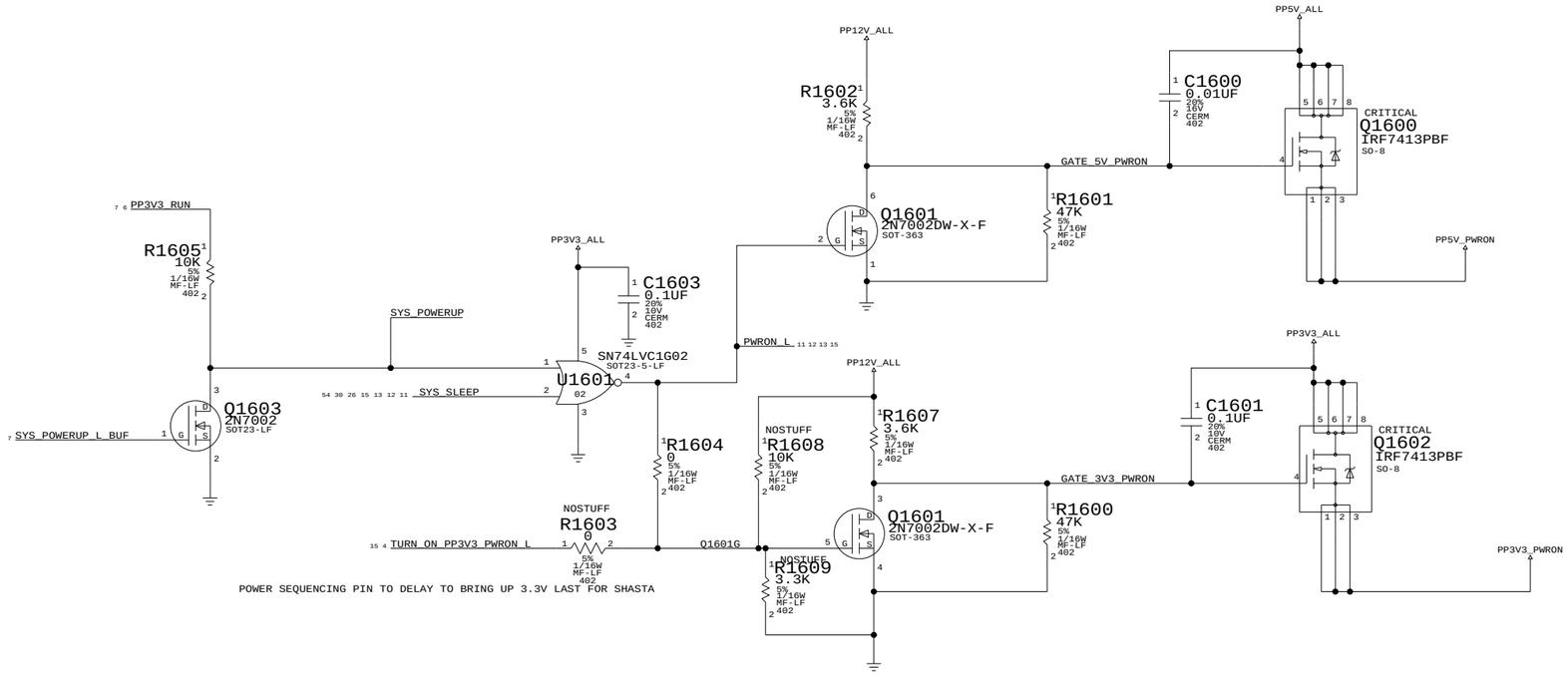
PP2V5_RUN FET SWITCH

PEAK CURRENT 0.1A



2.5V Vreg	
SYNC_MASTER=FINO-PC	SYNC_DATE=06/20/2005

APPLE COMPUTER INC.	SIZE: D	DRAWING NUMBER: 051-6790	REV: F
	SCALE: NONE	SHT: 15 OF 154	



5V & 3.3V Fets

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT
NONE	16 OF 154

Page Notes

Power aliases required by this page:

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

VESTA JTAG

139 132 17 7 =PP3V3_ENETFW

VESTA HAS INTERNAL PULLUPS. MLB PULLUPS MAY BE NOSTUFFED IN EVT.

R1741 1K 5% 1/16W MF-LF 402
R1742 1K 5% 1/16W MF-LF 402
R1743 1K 5% 1/16W MF-LF 402

9 TP_JTAG_VESTA_TCK — MAKE_BASE=TRUE — =JTAG_VESTA_TCK 17
9 TP_JTAG_VESTA_TDI — MAKE_BASE=TRUE — =JTAG_VESTA_TDI 17
9 TP_JTAG_VESTA_TDO — MAKE_BASE=TRUE — =JTAG_VESTA_TDO 17
9 TP_JTAG_VESTA_TMS — MAKE_BASE=TRUE — =JTAG_VESTA_TMS 17
9 TP_JTAG_VESTA_TRST_L — MAKE_BASE=TRUE — =JTAG_VESTA_TRST_L

R1740 1K 5% 1/16W MF-LF 402

139 132 7 =PP1V2_ENETFW

L1700 FERR-EMI-600-OHM SM
PP1V2_VESTA_AVDDL
MIN_LINE_WIDTH=0.50 MM
MIN_NECK_WIDTH=0.25 MM
VOLTAGE=1.2V

C1708 10UF 10% 6.3V X5R 805 — L7/M6
C1700 0.1uF 20% 10V CERM 402 — L9/M9
C1701 0.1uF 20% 10V CERM 402 — N5/N6
C1702 0.1uF 20% 10V CERM 402
C1703 0.1uF 20% 10V CERM 402 — N9/N10

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1750 10K 5% 1/16W MF-LF 402

M23: PP3V3_ENETFW IS AN ALL RAIL
139 132 17 7 =PP3V3_ENETFW

R1751 47K 5% 1/16W MF-LF 402

VESTA_RESET_RC

Q1750 2N7002DW-X-F SOT-363

C1750 1UF 10% 6.3V CERM 402

C1714 10UF 10% 6.3V X5R 805
C1710 0.1uF 20% 10V CERM 402
C1711 0.1uF 20% 10V CERM 402
C1712 0.1uF 20% 10V CERM 402
C1713 0.1uF 20% 10V CERM 402

=PP3V3_ENETFW 7 17 132 139

R1752 10K 5% 1/16W MF-LF 402

VESTA_RESET_L
SCHMITT TRIGGER W/ INTERNAL PULLUP

RESET ASSERT REQUIREMENT IS 20MS TO 100MS

NOSTUFF
R1720 0 5% 1/16W MF-LF 402
24 ENETFW_RESET

Q1750 2N7002DW-X-F SOT-363
132 VESTA_RESET_H

To keep Vesta from being held in reset when system is off
NOTE: Reset GPIO is active HIGH

VESTA MISC

SEE_TABLE
U1701
VESTA-V1.3
FBGA-200-LF
1 OF 3

H4	RESET* IPU	17 =JTAG_VESTA_TRST_L
D7	TDI IPU	17 =JTAG_VESTA_TDI
E10	TDO	17 =JTAG_VESTA_TDO
E7	TCK IPU	17 =JTAG_VESTA_TCK
E8	TMS IPU	17 =JTAG_VESTA_TMS
D8	TRST* IPU	
C9	DNC	9 TP_VESTA_DNC_C9
E9	DNC	9 TP_VESTA_DNC_E9
C3	NC	NC
M13	NC	NC

DVDD B1 B15 C15 J1
AVDDL L6 L9 M6 M9 M5 N6 N9 N10
AVDD P4 P5 P10 P11 R3 R12
PVDD A15 N4
OVDD A1 A7 F15 K1
AGND H11 H12 J11 J12 L7 L8 M7 M8 N7 N8 P6 P7 P8 P9
GND A2 B2 B7 C14 F14 J2 K2

IPD 2.5V_EN M3 — TP_VESTA_2_5V_EN 9

REGSUP1 E1 — TP_VESTA_REGSUP1 9
REGSEN1 F1 — TP_VESTA_REGSEN1 9
REGCTL1 G5 — TP_VESTA_REGCTL1 9

REGSUP2 E2 — TP_VESTA_REGSUP2 9
REGSEN2 F2 — TP_VESTA_REGSEN2 9
REGCTL2 G4 — TP_VESTA_REGCTL2 9

M23: ADDED C1726 AND C1744 PER BROADCOM RECOMMENDATIONS

C1720 0.1uF 20% 10V CERM 402
C1721 0.1uF 20% 10V CERM 402
C1722 0.1uF 20% 10V CERM 402
C1723 0.1uF 20% 10V CERM 402
C1724 0.1uF 20% 10V CERM 402
C1725 0.1uF 20% 10V CERM 402
C1726 10UF 10% 6.3V X5R 805

=PP2V5_ENETFW 7 132 139

C1730 0.1uF 20% 10V CERM 402
C1731 0.1uF 20% 10V CERM 402

C1740 0.1uF 20% 10V CERM 402
C1741 0.1uF 20% 10V CERM 402
C1742 0.1uF 20% 10V CERM 402
C1743 0.1uF 20% 10V CERM 402
C1744 10UF 10% 6.3V X5R 805

=PP3V3_ENETFW 7 17 132 139

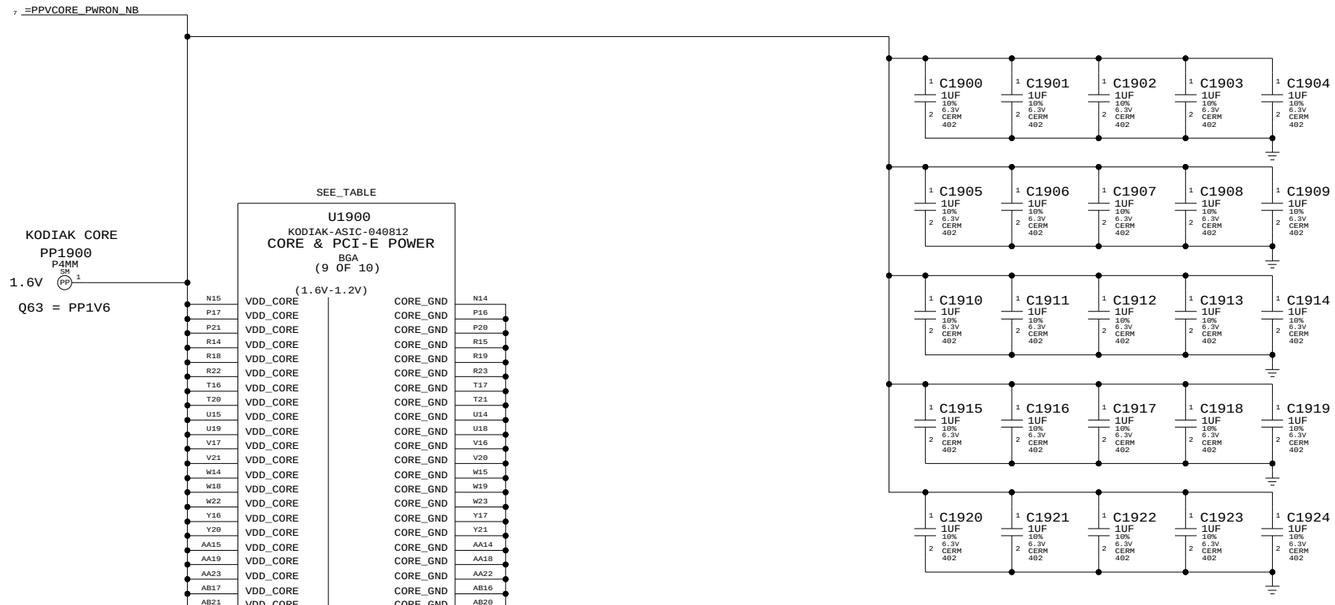
2.5V_EN
0 - OVDD=3.3V
1 - OVDD=2.5V
WHEN OVDD=2.5V GMII PINS ARE NOT 3.3V TOLERANT

Vesta Core / Misc

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 17 OF 154	



KODIAK CORE & BYPASS

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	19	154

DRAWING

SHASTA ALIASES

PCI_RESET_L IS AN 'AND' OF SB_PCI_RESET_L (SB)
AND SYS_IO_RESET_L (SMU)

119 92 PCI_RESET_L (MAKE_BASE=TRUE) — =PCI_AIRPORT_RESET_L 121
=PCI_ROM_RESET_L 125
=PCI_USB2_RESET_L 122

24 NB_SLOT_RESET_L (MAKE_BASE=TRUE) — =GPU_RESET_L 84

SHASTA JTAG

24 9 JTAG_SB_TRST_L — R2053 4.7K 5% 1/16W MF-LF 402

THESE PINS HAVE INTERNAL PULLUPS OR PULLDOWNS

9 TP_JTAG_SB_TCK (MAKE_BASE=TRUE) — JTAG_SB_TCK 24
9 TP_JTAG_SB_TDI (MAKE_BASE=TRUE) — JTAG_SB_TDI 24
9 TP_JTAG_SB_TDO (MAKE_BASE=TRUE) — JTAG_SB_TDO 24
9 TP_JTAG_SB_TMS (MAKE_BASE=TRUE) — JTAG_SB_TMS 24

SHASTA GPIO TERMINATIONS (SOME OF THESE ARE NOSTUFF ON PAGE 24)

119 56 24 23 7 =PP3V3_PWRON_SB

24 RAI_EXP_INTR_L<3> — R2061 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<2> — R2062 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<1> — R2063 10K 5% 1/16W MF-LF 402
24 RAI_EXP_INTR_L<0> — R2064 10K 5% 1/16W MF-LF 402

KODIAK ALIASES

6 NC_PMR_CLK_DIS_L (MAKE_BASE=TRUE) — PMR_CLK_DIS_L 20

KODIAK JTAG_TRST PULLED HIGH TO ALLOW SMU DEBUG ACCESS

=PP2V5_PWRON_NB_MISC 7 20 28 30 39

R2073 4.7K 5% 1/16W MF-LF 402 — NOSTUFF
R2074 0 5% 1/16W MF-LF 402

20 9 JTAG_NB_TRST_L — NB_PU_RST_L 20 30

NOSTUFF R2054 4.7K 5% 1/16W MF-LF 402

=PP1V8_PWRON_NBMEM 7 39 58 59

C2055 1UF 10% 6.3V CERM 402

C2055 ADDED FOR KODIAK RAM DECOUPLING
PAGE 58 IS SHORT ONE CAP

39 30 28 20 7 =PP2V5_PWRON_NB_MISC

P4MM SM TP2002

R2003 1K 1% 1/16W MF-LF 402

U1900
KODIAK-ASIC-040812
BGA
(10 OF 10)

30 9 JTAG_NB_TCK	AJ04	CE1_LT_TCK	NORTH_BRIDGE_RESET_L AL01 — NB_PU_RST_L 20 30
30 9 JTAG_NB_TDI	AG07	CE1_MC_TDI	HRESET_L AG01 — NB_HRST_L
30 9 JTAG_NB_TDO	AG05	CE1_B_TDO	SUSPENDACK_L AJ03 — NB_SUSPEND_ACK_L 30 62
30 9 JTAG_NB_TMS	AL02	CE1_DI1_TMS	SUSPENDREQ_L AJ01 — NB_SUSPEND_REQ_L 30
20 9 JTAG_NB_TRST_L	AK06	CE1_DI2_TRST	SYS_ISCA0 AG04 — I2C_NB_B_SDA 39
			SYS_ISCL0 AK03 — I2C_NB_B_SCL 39
CE0TEST	AG08	CE0_TEST	SYS_ISCA1 AH06 — I2C_NB_C_SDA 39
20 NB_THERM_A	F15	SYS_THDIO_D	SYS_ISCL1 AJ05 — I2C_NB_C_SCL 39
20 NB_THERM_K	G15	SYS_THDIO_G	API_ISCA AG03 — I2C_NB_A_SDA 39
			API_ISCL AH03 — I2C_NB_A_SCL 39
39 30 28 20 7 =PP2V5_PWRON_NB_MISC	AF02	VD5_0	PMR_CLK_P AE09 — NB_PMR_CLK_P 26 27
	AF05	VD5_1	PMR_CLK_N AE10 — NB_PMR_CLK_N 26 27
	AH01	VD5_2	PMR_CLK_STOP_L AG02

POWER/TEST/MISC

C2050 1UF 10% 6.3V CERM 402
C2051 1UF 10% 6.3V CERM 402
C2052 1UF 10% 6.3V CERM 402

R2000 0 5% 1/16W MF-LF 402

NOSTUFF R2001 60.4 1% 1/16W MF-LF 402
NOSTUFF R2002 60.4 1% 1/16W MF-LF 402

TERM_RC

NOSTUFF C2053 1.5PF +/-0.25PF 50V CERM 402

PLACE TERM R/C CLOSE TO KODIAK

P4MM SM TP2000

XW2000

6 PP_2V5PWRONNBMISC

R2013 10K 5% 1/16W MF-LF 402

NOSTUFF R2012 0 5% 1/16W MF-LF 402

20 PMR_CLK_DIS_L — NB_PMR_CLK_STOP_L

NOTE: LOW = DISABLE PMR_CLK

NOTE:
PMR_CLK_STOP CAN BE USED TO STOP ALL CLOCKS IN KODIAK
USED FOR DEBUG
PLACE R2012 IN AN ACCESSIBLE LOCATION

NB_OVERTEMP

30 28 7 =PP3V3_RUN_SMU

R2082 2.2 5% 1/16W MF-LF 402
C2080 1UF 10% 6.3V CERM 402

MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.38MM
TSENSE_NB_VCC

U2080
MAX6690MEE
QSOP (SYM_VER2)

CRITICAL
VCC
STBY
ALERT
SMBDATA
SMBCLK
ADD0
ADD1
DXP
DXN
NC_1
NC_5
NC_9
NC_13
NC_16
GND

39 I2C_NB_TEMP_SDA
39 I2C_NB_TEMP_SCL

TSENSE_NB_ADD0
TSENSE_NB_ADD1

R2083 1K 5% 1/16W MF-LF 402
NOSTUFF R2084 1K 5% 1/16W MF-LF 402
NOSTUFF R2086 1K 5% 1/16W MF-LF 402
R2085 1K 5% 1/16W MF-LF 402

20 NB_THERM_A
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB
NET_PHYSICAL_TYPE=10MIL_WIDTH
NET_SPACING_TYPE=TSENSE_DIFPAIR

C2081 0.0022UF 10% 50V CERM 402
PLACE BY IC

20 NB_THERM_K
MIN_LINE_WIDTH=0.25mm
MIN_NECK_WIDTH=0.25MM
DIFFERENTIAL_PAIR=TSENSE_NB

NET_SPACING_TYPE=TSENSE_DIFPAIR
NET_PHYSICAL_TYPE=10MIL_WIDTH

TSENSE_NB_OVERTEMP_L — NOSTUFF R2087 0 5% 1/16W MF-LF 402 — SYS_OVERTEMP_L 24 28 93

NEED TO CHECK ALL I2C ADDRESSES

A0	A1	ADDR
0	0	30/31
0	hiZ	32/33
0	1	34/35
hiZ	0	52/53
hiZ	hiZ	54/55
hiZ	1	56/57
1	0	98/99
1	hiZ	9A/9B
1	1	9C/9D

KODIAK & SHASTA MISC

SYNC_MASTER=FINO-ME — SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	20	154

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_SB_PCI64 (VIO1) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB_PCI32 (VIO2) (TO 5V OR 3.3V)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB
- =PP1V2_PWRON_SB_VCORE

NOTE: PCI pads use the VIO supply to meet different drive timing characteristics required by the PCI spec for 5V vs. 3.3V operation. CONNECT VIO2 TO appropriate PCI bus voltage and VIO1 TO SAME IF 64-BIT PCI, otherwise 3.3V.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Power Sequencing:
Must power Shasta VCore rail before any other Shasta supplies.

XW2300 SM 2 1 6 PP_1V2PWRONSBVCORE → P4MM SM 1 PP → PP2300
XW2303 SM 2 1 6 PP_3V3PWRONSBPCI64 → P4MM SM 1 PP → PP2303
XW2304 SM 2 1 6 NO_TEST=YES PP_2V5PWRONSB → P4MM SM 1 PP → PP2304

7 =PP1V2_PWRON_SB_VCORE

C2300 C2301 C2302 C2303 C2304
C2305 C2306 C2307 C2308 C2309
C2310 C2311 C2312 C2313 C2314
0.1uF 20% 10V CERM 402

119 56 24 20 7 =PP3V3_PWRON_SB

C2320 C2321 C2322 C2323 C2324
C2325 C2326 C2327 C2328 C2329
C2330 C2331 C2332 C2333 C2334
C2335 C2336 C2337 C2338 C2339
0.1uF 20% 10V CERM 402

U2300
SHASTA
V1.1
BGA-LF
(1 OF 8)

POWER
SEE_TABLE

VDDC: H15 H8 J12 J15 K8 L15 L8 M15 N8 P15 R10 R12 R9 T10 T15
VDDO33: AA1 AA2 AA3 AB10 AB2 AB6 B1 B2 B5 D3 F4 F8 H1 L7 M1 R2 U12 U9 V7 W4
GND: A1 A2 A22 A5 AA10 AA6 AB1 AB22 C19 D2 E22 F3 F7 H2 H9 J10 J11 J13 J14 J16
GND: J22 K10 K11 K12 K13 K7 K9 L10 L11 L12 L13 L14 L16 L9 M10 M11 M12 M13 M14 M6
VDDO25: D19 G15
VIO1: H18 H17 K21
VIO2: L21 W22 Y19
VDDP_KL: V8
GND: W5 W19 U22 U13 U10 T12 R19 P9 P4 P14 P13 P12 P10 N9 N22 N13 N12 N11 N10 M2

Shasta max (est 06/30/03) current:

DIGITAL	1.2V	950 mA (1175 mW)
ANALOG12	1.2V	600 mA (760 mW)
VDDPs	2.5V	100 mA (250 mW)
I/O 2.5	2.5V	20 mA (60 mW)
I/O 3.3	3.3V	220 mA (770 mW)
Total:		3015 mW

=PP2V5_PWRON_SB 7 23 24 119 138
C2350 C2351 0.1uF 20% 10V CERM 402

=PP3V3_PWRON_SB_PCI64 7
C2355 C2356 C2357 0.1uF 20% 10V CERM 402
For PCI_AD<63..32>

=PP3V3_PWRON_SB_PCI32 7
C2360 C2361 C2362 0.1uF 20% 10V CERM 402
For PCI_AD<31..0>

=PP2V5_PWRON_SB 7 23 24 119 138
C2365 0.1uF 20% 10V CERM 402

Shasta Core Power

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE: NONE SHT: 23 OF: 154

LAST_MODIFIED=Wed Nov 16 09:40:51 2005

DRAWING
TITLE=SILICONA
NAME=SHASTA

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I2S0_TO_SB		
I2S0_TO_DEV		
I2S0_TO_DEV	AUDIO	
I2S0_BIDIR		
I2S0_BIDIR		
I2S1_TO_SB		
I2S1_TO_DEV		
I2S1_TO_DEV	0.25mm SPACING	
I2S1_BIDIR		
I2S1_BIDIR		
I2S2_TO_SB		
I2S2_TO_DEV		
I2S2_TO_DEV	0.25mm SPACING	
I2S2_BIDIR		
I2S2_BIDIR		
SB_CLK18M_XTAL	0.38mm SPACING	
	0.38mm SPACING	
	0.38mm SPACING	
SB_CLK25M_ATA	0.38mm SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	
	P3MM SPACING	

I2S0_DEV_TO_SB_DTI 24 147
I2S0_SB_TO_DEV_DTO 24 147
I2S0_MCLK 24 154
I2S0_BITCLK 24 147
I2S0_SYNC 24 147
I2S1_DEV_TO_SB_DTI 8 24
I2S1_SB_TO_DEV_DTO 8 24
I2S1_MCLK 8 24
I2S1_BITCLK 8 24
I2S1_SYNC 8 24
I2S2_DEV_TO_SB_DTI 24 154
I2S2_SB_TO_DEV_DTO 24 154
I2S2_MCLK 24 154
I2S2_BITCLK 24 154
I2S2_SYNC 24 154
SB_CLK18M_XTALI 24
SB_CLK18M_XTALO 24
SB_CLK18M_XTALO_R 24
SB_CLK25M_SATA 24 26
NB_TO_SB_INT 24
SB_CPU_A0_INT_L 24
SB_CPU_A1_INT_L 24
SB_CPU_B0_INT_L 24
SB_CPU_B1_INT_L 24
PCI_AIRPORT_INT_L 24 121
PCI_USB2_INT_L 24 122
I2S0_RESET_L 24 147
I2S1_RESET_L 8 24
I2S2_RESET_L 24 154
MB_SLOT_RESET_L 24
NB_SLOT_RESET_L 20 24
SB_CPU_A0_SRESET_L 24 56
SB_CPU_A1_SRESET_L 24 56
SB_CPU_B0_SRESET_L 24 56
SB_CPU_B1_SRESET_L 24 56

Page Notes

Power aliases required by this page:
- _PP3V3_PCI
- _PP3V3_PWRON_SB
- _PP2V5_PWRON_SB
- _PP1V2_PWRON_SB

Signal aliases required by this page: (NONE)

BOM options provided by this page:
- PCI_64BIT: Configures Shasta for 64-bit PCI
  NOTE: XGC required for Shasta GPIOs
- MPIC_NB/MPIC_SB: Selects whether NorthBridge or SouthBridge MPIC will be used for interrupt controller.

AUDIO PAGES IS RESPONSIBLE FOR TERMINATION OF I2S0 AND I2S2
DO NOT ADD PULLUP/DOWN FOR I2S0 AND IS=2S2 IN THIS PAGE

Re-pin within each RPAK as necessary
DO NOT swap between RPAKs

NorthBridge / SouthBridge MPIC Routing

PLACE R2402 CLOSE TO SHASTA

PLACE R2432 CLOSE TO SHASTA

SPEC SHOWS LOAD CAPACITANCE OF 16PF FOR 197S0004

AUDIO GPIOS
NOTE: It is the responsibility of the audio circuit to provide the necessary pull-ups & pull-downs.

LAST_MODIFIED=Wed Nov 16 09:40:52 2005

Shasta Serial / Misc

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

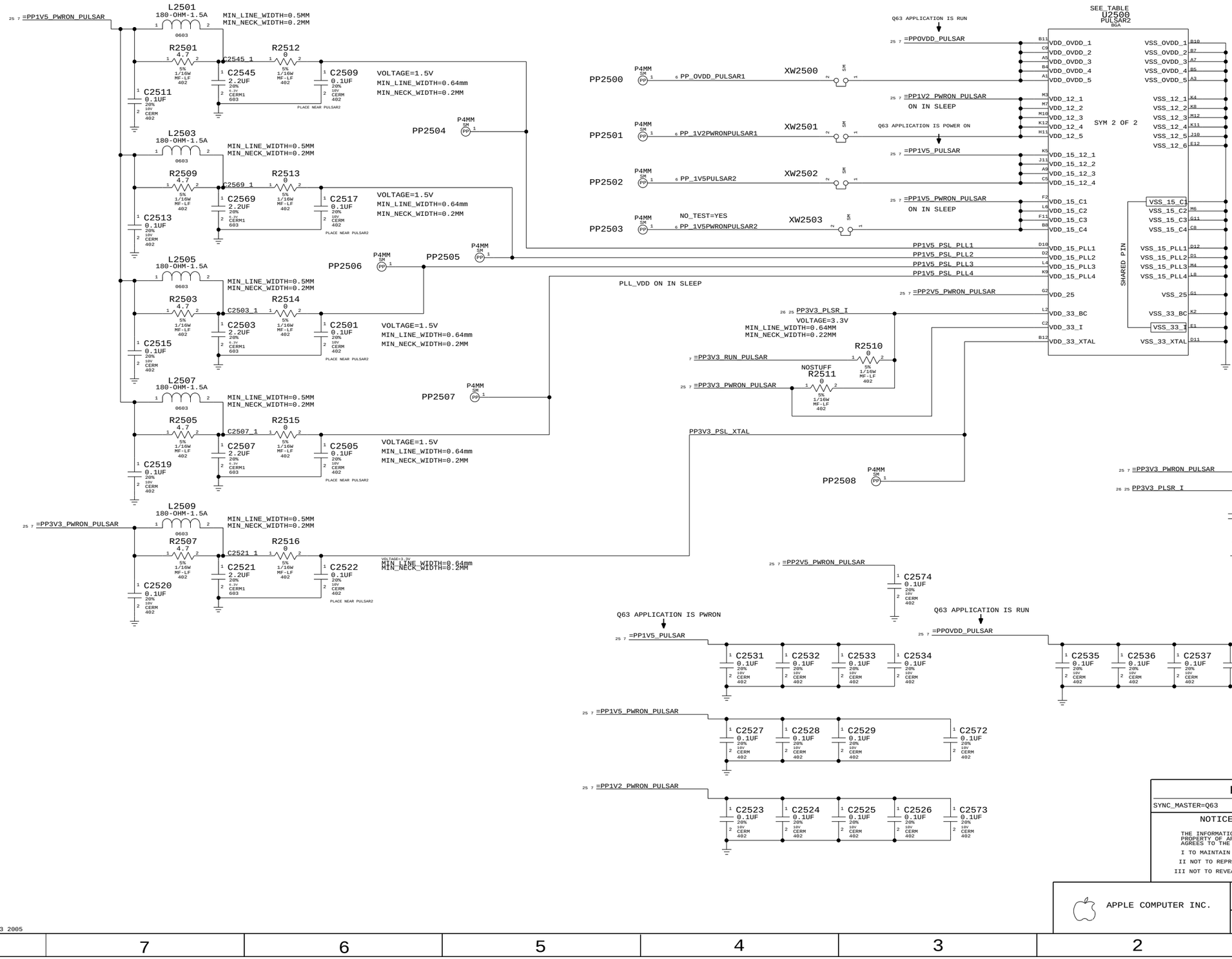
NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 24 OF: 154	

DRAWING
TITLE=SCALEOVRRA
ABBREV=OVRAVING



PULSAR2 POWER

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE	SHT	OF
NONE	25	154

LAST_MODIFIED=Wed Nov 16 09:40:53 2005

DRAWING

PLACE ALL 0-OHM SERIES RESISTORSRES
ON THIS PAGE NEAR PULSAR

REMOVED R2632 AND R2630
FROM UNUSED CLOCKS FOR EMC

QUASAR CLOCKS ARE RESISTOR DIVIDED DOWN
TO 1.8V ON QUASAR PAGES

LAST MODIFIED: APR 26, 04

PULSAR2 CLOCKS

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE: NONE SHT: 26 OF: 154

LAST_MODIFIED=Wed Nov 16 09:40:54 2005

DRAWING
TITLE=K2LOANWA
ABSREV=SHAWING

N/C ALIASES

N/C RAINIER CLOCKS

6 NC_CLK_RAI_REFCLK_66M ═══ CLK_RAI_REFCLK_66M 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_GIGE_25MHZ ═══ CLK_RAI_GIGE_25MHZ 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_P<0> ═══ CLK_RAI_200M_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_200M_N<0> ═══ CLK_RAI_200M_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_P<0> ═══ CLK_RAI_PCIEA_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEA_N<0> ═══ CLK_RAI_PCIEA_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_P<0> ═══ CLK_RAI_PCIEB_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEB_N<0> ═══ CLK_RAI_PCIEB_N<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_P<0> ═══ CLK_RAI_PCIEC_P<0> 26
MAKE_BASE=TRUE

6 NC_CLK_RAI_PCIEC_N<0> ═══ CLK_RAI_PCIEC_N<0> 26
MAKE_BASE=TRUE

N/C CPUB CLOCKS

6 NC_EI_CPU_B_SYSCLK_P ═══ EI_CPU_B_SYSCLK_P 26
MAKE_BASE=TRUE

6 NC_EI_CPU_B_SYSCLK_N ═══ EI_CPU_B_SYSCLK_N 26
MAKE_BASE=TRUE

6 NC_CPU_B_APSYNC ═══ CPU_B_APSYNC 26
MAKE_BASE=TRUE

N/C QUASAR CLOCKS

6 NC_RAM_ARB0_REF25MHZ ═══ RAM_ARB0_REF25MHZ 26
MAKE_BASE=TRUE

6 NC_RAM_ARB1_REF25MHZ ═══ RAM_ARB1_REF25MHZ 26
MAKE_BASE=TRUE

CLOCK CONSTRAINTS

	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	ELECTRICAL_CONSTAINT_SET	
26 20 NB_PMR_CLK_P	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	167
25 20 NB_PMR_CLK_N	NB_PMR_CLK	NB_PMR_CLK	NB_PMR_CLK_SP	NB_PMR_CLK	168
119 26 PCI_CLK66M_SB_INT		PCI_CLK_SB	P3MM SPACING	PCI_CLK_SB	169
119 26 PCI_CLK33M_SB_EXT_RR		PCI_CLK_SB	PCI_CLK_SB	PCI_CLK_SB_CAP	170

NOTE:
ALL OTHER CLOCK CONTRAINTS ON THEIR
RESPECTIVE BUS PAGES

26 PCI_CLK33M_USB2 ═══ =PCI_CLK33M_USB2 122
MAKE_BASE=TRUE

Pulsar Aliases

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE NONE SHT 27 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
SMU_CLK10M_XTAL	0.38MM SPACING		SMU_CLK10M_XIN 28
	0.38MM SPACING		SMU_CLK10M_XOUT 28
	0.38MM SPACING		SMU_CLK10M_XOUT_R 28
RTC_CLK32K_XTAL	0.38MM SPACING		RTC_CLK32K_X1 28
	0.38MM SPACING		RTC_CLK32K_X2 28
A476	P3MM SPACING		SMU_IO_RESET_L 28 30
A475	0.25MM SPACING		SYS_NORTH_RESET_L 28 30

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
A456 SMU_RESET	0.25MM SPACING		SYS_NORTH_RESET_L 28 30
A457 SMU_RESET	0.25MM SPACING		SYS_IO_RESET_L 24 30 119 122
A472	P3MM SPACING		CLOCK_RESET_L 26 28
A475	P3MM SPACING		SYS_RESET_BUTTON_L 28 29

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_SMU
- =PP3V3_ALL_RTC
- =PP3V3_PWRON_SMU
- =PPVREF_SMU (SMU AVCC OR 2.5V REFERENCE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: CPU current/voltage monitoring (CPU_SENSE_I/CPU_SENSE_V) requires 100K/10uF RC filter at SMU pins. Caps should connect to GND_SMU_AVSS. SMU_VREF should be same signal or reference used by monitoring circuit, but be aware that this will affect other analog inputs such as AC adapter ID.

NOTE: All analog inputs to SMU should have a 100pF capacitor to the SMU AVSS signal (GND_SMU_AVSS). None of those capacitors are provided on this page.

NOTE: Some primary and alternate functions reuire pull-ups that are not. provided on this page. Please. review the latest SMU specification to ensure missing pull-ups are provided on another page.

NOTE: Pinout matches SMU pinout v1.51.

PP2800 P4MM SM 1 6 PP_3V3ALLSMU — XW2802 SM 2 1 — 29 28 7 6 =PP3V3_ALL_SMU

C2800 10UF 10% 6.3V XSR 805 (1,2) — C2801 0.1uF 20% 10V CERM 402 (1,2) — C2802 0.1uF 20% 10V CERM 402 (1,2)

R2815 4.7 5% 1/16W MF-LF 402 (1,2)

PP3V3_ALL_SMU_AVCC
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

C2803 1uF 10% 6.3V CERM 402 (1,2)

GND_SMU_AVSS 6 28 55

XW2801 SM 2 1 — 6 PP_3V3ALLSMUAVCC — P4MM SM 1 (PP) PP2801

13 SEE_TABLE 78

VCC 11 — AVCC 75

U2800
M30280F8-LF
QFP-80

Y = Primary function
N = Alternate function (see aliases below)
S = Spare

	Portable	Consumer	Entry Desktop	Desktop	Server
55 CPU_SENSE_I	Y	Y	Y	S	S 67 P0[0] AN00
55 CPU_SENSE_V	Y	Y	Y	S	S 66 P0[1] AN01
55 CPU_TEMP	Y	Y	Y	S	S 65 P0[2] AN02
29 CPU_BYPASS	Y	Y	Y	S	S 64 P0[3] AN03
31 SMU_FAN_RPM3	N	S	Y	Y	Y 63 P0[4] AN04
31 SMU_FAN_RPM4	N	S	Y	Y	Y 62 P0[5] AN05
31 SMU_FAN_RPM5	N	S	Y	Y	Y 61 P0[6] AN06
31 SMU_SER_SEL	Y	Y	Y	Y	Y 60 P0[7] AN07
P1[0] NOT USED --->					
4 SMU_PWRSEQ_P1_0	Y	Y	Y	Y	Y 59 P1[0] AN20
4 SMU_PWRSEQ_P1_1	Y	Y	Y	Y	Y 58 P1[1] AN21
4 SMU_PWRSEQ_P1_2	Y	Y	Y	Y	Y 57 P1[2] AN22
4 SMU_PWRSEQ_P1_3	Y	Y	Y	Y	Y 56 P1[3] AN23
4 SMU_PWRSEQ_P1_4	Y	Y	Y	Y	Y 55 P1[4]
7 SYS_POWERFAIL_L	N	Y	Y	Y	Y 54 P1[5] INT3*
31 SMU_FAN_TACH9	N	S	S	S	Y 53 P1[6] INT4*
31 SYS_DOOR_AJAR_L	N	S	Y	Y	Y 52 P1[7] INT5*
31 SMU_FAN_TACH6	Y	Y	Y	Y	Y 51 P2[0] SDAmm
31 SMU_FAN_TACH7	Y	Y	Y	Y	Y 50 P2[1] SCLmm
32 SMU_FAN_TACH0	Y	Y	Y	Y	Y 49 P2[2] IOC2
32 SMU_FAN_TACH1	Y	Y	Y	Y	Y 48 P2[3] IOC3
33 SMU_FAN_TACH2	Y	Y	Y	Y	Y 47 P2[4] IOC4
31 SMU_FAN_TACH3	S	N	Y	Y	Y 46 P2[5] IOC5
31 SMU_FAN_TACH4	S	N	Y	Y	Y 45 P2[6] IOC6
31 SMU_FAN_TACH5	S	N	Y	Y	Y 44 P2[7] IOC7
31 28 I2C_SMU_A_SDA_IN	Y	Y	Y	Y	Y 39 P3[0] CLK3
31 28 I2C_SMU_A_SDA_OUT_L	Y	Y	Y	Y	Y 38 P3[1] Sin3
31 28 I2C_SMU_A_SCL_IN	Y	Y	Y	Y	Y 37 P3[2] Sout3
31 28 I2C_SMU_A_SCL_OUT_L	Y	Y	Y	Y	Y 36 P3[3]
39 I2C_SMU_E_SDA	Y	Y	Y	Y	Y 35 P3[4]
39 I2C_SMU_E_SCL	Y	Y	Y	Y	Y 34 P3[5]
8 DIAG_LED	Y	S	S	S	S 33 P3[6]
93 24 20 SYS_OVERTEMP_L	Y	S	S	S	S 32 P3[7]

	Portable	Consumer	Entry Desktop	Desktop	Server
SMU_BOOT_BUSY 6 29					MAKE_BASE=TRUE
SMU_BOOT_SCLK 6 29					
SMU_BOOT_CE 6 29					
CPU_VID<0> 28 31	Y	Y	Y	N	N 43 P6[0] RTS0*/CTS0*
CPU_VID<1> 28 31	Y	Y	Y	N	N 42 P6[1] CLK0
CPU_VID<2> 28 31	Y	Y	Y	N	N 41 P6[2] RXD0
CPU_VID<3> 28 31	Y	Y	Y	S	S 40 P6[3] TXD0
CPU_VID<4> 28 31	Y	Y	Y	S	S 31 P6[4] RTS1* (BUSY)
CPU_VID<5> 31	Y	Y	Y	S	S 30 P6[5] CLK1
SMU_BOOT_RXD 6 29	Y	Y	Y	Y	Y 29 P6[6] RXD1
SMU_BOOT_TXD 6 29	Y	Y	Y	Y	Y 28 P6[7] TXD1
I2C_SMU_B_SDA 39	Y	Y	Y	Y	Y 27 P7[0] SDA
I2C_SMU_B_SCL 39	Y	Y	Y	Y	Y 26 P7[1] SCL
I2C_SMU_CPU_SDA_IN 28 31	Y	Y	Y	N	N 25 P7[2] TA1out
SMU_FAN_RPM0 32	Y	Y	Y	Y	Y 24 P7[3] TA1in
I2C_SMU_CPU_SCL_IN 28 31	Y	Y	Y	N	N 23 P7[4] TA2out
SMU_FAN_RPM1 32	Y	Y	Y	Y	Y 22 P7[5] TA2in
SB_CPU_VDNAP2 24	N	S	S	Y	Y 21 P7[6] TA3out
SMU_FAN_RPM2 33	Y	Y	Y	Y	Y 20 P7[7] TA3in
SYS_LED 29	Y	Y	Y	Y	Y 19 P8[0] TA4out
SYS_NORTH_RESET_L 28 30	Y	Y	Y	Y	Y 18 P8[1] TA4in
SYS_PME_L 24 28 122	Y	Y	Y	Y	Y 17 P8[2] INT0*
SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 31	S	S	S	S	S 16 P8[3] INT1*
SYS_SLEWING_L 24 26 28 50	Y	Y	Y	Y	Y 15 P8[4] INT2*
I2C_SMU_CPU_SDA_OUT_L 28 31	Y	Y	Y	S	S 14 P8[5] NMI*
SYS_POWERUP_L 6 7 12 28 50 85	Y	Y	Y	Y	Y 8 P8[6] CE*
MAKE_BASE=TRUE SMU_SLEEP 28 30	Y	Y	Y	Y	Y 7 P8[7]
CLOCK_RESET_L 26 28	Y	Y	Y	Y	Y 5 TB0in P9[0]
SMU_FAN_TACH8 31	Y	Y	Y	S	S 4 TB1in P9[1]
SB_TO_SMU_INT_L 24	Y	Y	Y	Y	Y 3 TB2in P9[2]
SB_STOPXTALS_L 24	Y	Y	Y	Y	Y 2 AN24 P9[3]
SMU_PWRSEQ_P9_5 4	Y	Y	Y	Y	Y 1 AN25 P9[5]
SMU_PWRSEQ_P9_6 4	Y	Y	Y	Y	Y 80 AN26 P9[6]
SYS_SLOT_PWR 31	S	S	Y	Y	S 79 AN27 P9[7]
SB_CPU_VDNAP1 24	S	S	S	S	S 76 AN0 P10[0]
SMU_IO_RESET_L 28 30	Y	Y	Y	Y	Y 74 AN1 P10[1]
NB_SUSPENDACK_L 30	Y	Y	Y	Y	Y 73 AN2 P10[2]
SB_SUSPENDACK_L 24	Y	Y	Y	Y	Y 72 AN3 P10[3]
SMU_SUSPENDREQ_L 24 28 30 43	Y	Y	Y	Y	Y 71 KI0* P10[4]
SYS_POWER_BUTTON_L 6 28 29	Y	Y	Y	Y	Y 70 KI1* P10[5]
SYS_RESET_BUTTON_L 28 29	Y	Y	Y	Y	Y 69 KI2* P10[6]
I2C_SMU_CPU_SCL_OUT_L 28 31	Y	Y	Y	S	S 68 KI3* P10[7]

55 =PPVREF_SMU

29 6 SMU_BOOT_CNVSS — 6 PCNVSS
29 6 SMU_RESET_L — 9 RESET*
28 SMU_CLK10M_XOUT_R — 10 XOUT
28 SMU_CLK10M_XIN — 12 XIN
77 VREF

P4MM SM PP2804 — SMU_RESET_L
P4MM SM PP2805 — SMU_CLK10M_XOUT_R
P4MM SM PP2806 — SMU_CLK10M_XIN

R2816 10M 5% 1/16W MF-LF 402 (1,2)
R2817 470 5% 1/16W MF-LF 402 (1,2)
CRITICAL Y2800 10.0000M 8X4.5MM-SM (1,2)
28 SMU_CLK10M_XOUT
C2804 18PF 5% 50V CERM 402 (1,2)
C2805 18PF 5% 50V CERM 402 (1,2)

Keep crystal subcircuit close to SMU.
Y2800'S LOAD CAPACITANCE IS 12PF

R2825 10K 5% 1/16W MF-LF 402 (1,2)
C2825 1uF 10% 6.3V CERM 402 (1,2)

XW2800 SM (1,2)

R2827 10K 5% 1/16W MF-LF 402 (1,2)

GND_SMU_AVSS 6 28 55
VOLTAGE=0V
MIN_LINE_WIDTH=0.38mm
MIN_NECK_WIDTH=0.2MM

System Management Unit

Real Time Clock

29 =PP3V3_ALL_RTC
29 28 7 6 =PP3V3_ALL_SMU

C2808 0.1uF 20% 10V CERM 402 (1,2)

U2801 DS1338U-33 MSOP
VCC (8 CRITICAL) — SDA (5) — SCL (6) — SQW/OUT (7) — VBAT (3) — GND (4) — X1 (1) — X2 (2)

39 I2C_RTC_SDA
39 I2C_RTC_SCL
NC

CRITICAL Y2801 32.768K SM-LF (1,2,3,4)

RTC_CLK32K_X1 28
RTC_CLK32K_X2 28

C2809 0.1uF 20% 10V CERM 402 (1,2)

SMU Pull-ups / pull-down

29 28 7 6 =PP3V3_ALL_SMU

R2800 10K 5% 1/16W MF-LF 402 (1,2) — SYS_POWERUP_L 6 7 12 28 50 85
R2801 10K 5% 1/16W MF-LF 402 (1,2) — SYS_RESET_BUTTON_L 28 29
R2802 10K 5% 1/16W MF-LF 402 (1,2) — SYS_POWER_BUTTON_L 6 28 29

43 30 7 =PP3V3_PWRON_SMU

R2804 10K 5% 1/16W MF-LF 402 (2,1) — SYS_PME_L 24 28 122

30 20 7 =PP3V3_RUN_SMU

R2812 2.0K 1% 1/16W MF-LF 402 (1,2) — SYS_SLEWING_L 24 26 28 50

NOSTUFF
39 30 20 7 =PP2V5_PWRON_NB_MISC
DRIVEN PUSH/PULL

R2811 2.0K 1% 1/16W MF-LF 402 (1,2) — SMU_SUSPENDREQ_L 24 28 30 43

NOSTUFF
PULLUP AT LEVEL SHIFTER P.30

R2813 10K 5% 1/16W MF-LF 402 (1,2) — SYS_NORTH_RESET_L 28 30

R2810 100K 1% 1/16W MF-LF 402 (1,2) — SMU_SLEEP 28 30

Alternate Functions

Tower & Server

	Port		
31 28 CPU_VID<0>	6.0	—	SAT_MRESET_L
31 28 CPU_VID<1>	6.1	—	CPU_A_INSERTED_L
31 28 CPU_VID<2>	6.2	—	CPU_B_INSERTED_L
31 28 I2C_SMU_CPU_SDA_IN	7.2	—	SMU_FAN_PWM8
31 28 I2C_SMU_CPU_SCL_IN	7.4	—	SMU_FAN_PWM9
31 28 I2C_SMU_A_SDA_IN	3.0	—	I2C_SMU_A_SDA 31 39
31 28 I2C_SMU_A_SDA_OUT_L	3.1	—	I2C_SMU_A_SCL 31 39

	Port		
31 28 CPU_VID<3>	6.3	—	SMU_FAN_RPM6
31 28 CPU_VID<4>	6.4	—	SMU_FAN_RPM7
31 28 I2C_SMU_A_SCL_IN	3.2	—	NB_TDI
31 28 I2C_SMU_A_SCL_OUT_L	3.3	—	NB_TCK
31 28 I2C_SMU_CPU_SDA_OUT_L	8.5	—	NB_TMS
31 28 I2C_SMU_CPU_SCL_OUT_L	10.7	—	NB_TDO_SMU

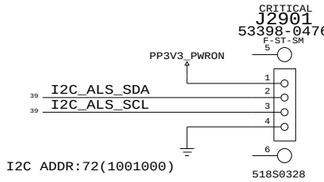
System Management Unit
SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

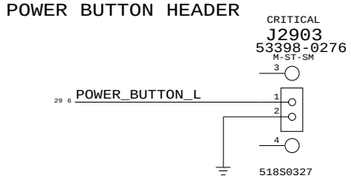
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 28 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:55 2005
DRAWING
TITLE=KILOHANA
ASSEMBLY=DRAWING

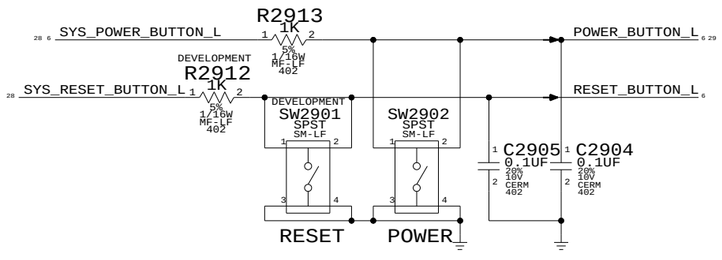
AMBIENT LIGHT SENSOR CONNECTOR



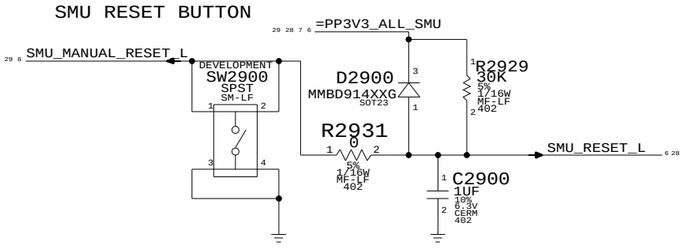
POWER BUTTON HEADER



SYS POWER AND RESET BUTTON

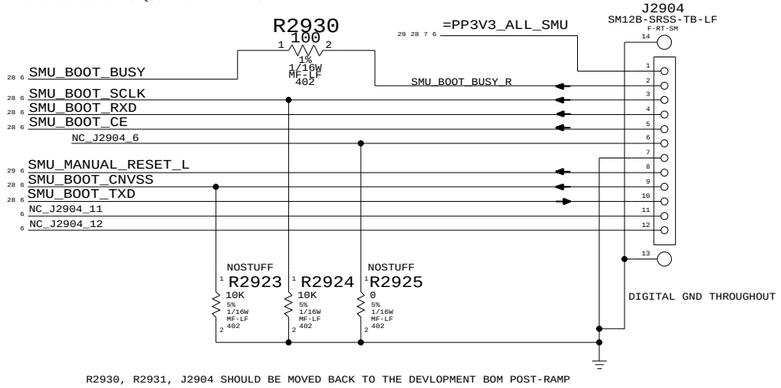


SMU RESET BUTTON



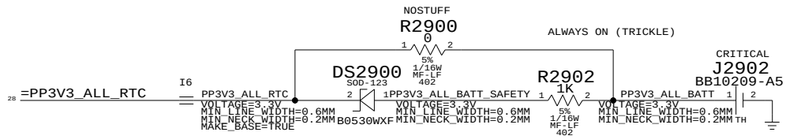
SMU DEBUG/DOWNLOAD CONNECTOR

SAME CONNECTOR AS Q63 CPU CARD FOR SAT

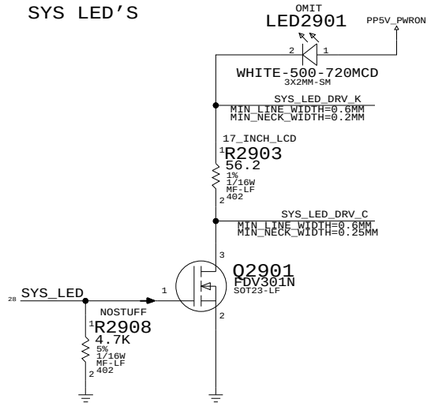


R2930, R2931, J2904 SHOULD BE MOVED BACK TO THE DEVLOPMENT BOM POST-RAMP

RTC BATTERY



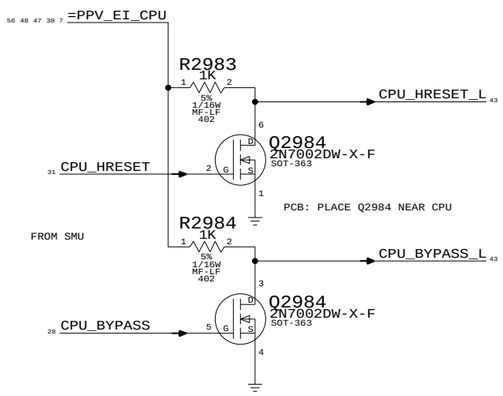
SYS LED'S



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
378S0157	1	WHITE LED, B2S BIN	LED2901	CRITICAL	17_INCH_LCD
378S0158	1	WHITE LED, B2T BIN	LED2901	CRITICAL	20_INCH_LCD

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0081	1	RES, 39.2 OHM, 1%, 402, LF	R2903	20_INCH_LCD

DRIVE STRONG HRESET AND BYPASS TO CPU



SMU SUPPLEMENTAL (2)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	29	154

SMU TO NB SUSPEND_REQ

SAME AS Q63

=PP3V3_PWRON_SMU

R3000 1K 5% 1/16W MF-LF 402

R3003 4.7K 5% 1/16W MF-LF 402

PMU_SUSPEND_REQ

=PP2V5_PWRON_NB_MISC

R3001 100 5% 1/16W MF-LF 402

NB_SUSPEND_REQ_L

SMU_SUSPENDREQ_L

Q03005 2N7002DW-X-F SOT-363

Q03000 2N7002DW-X-F SOT-363

NOSTUFF R3002 0 5% 1/16W MF-LF 402

SMU_SUSPENDREQ_L_R

NOSTUFF R3099 0 5% 1/16W MF-LF 402

MISC. SMU BUFFERS

SAME AS (Q63).

=PP3V3_PWRON_SMU

R3021 4.7K 5% 1/16W MF-LF 402

U700 IS POWERED BY PP3V3_ALL

U700 74LC125 TSSOP

SMU_IO_RESET_L

SYS_IO_RST_L_R

R3022 100 5% 1/16W MF-LF 402

SYS_IO_RESET_L

SMU_SLEEP

SYS_SLEEP_R

R3023 100 5% 1/16W MF-LF 402

SYS_SLEEP

NB SUSPEND_ACK_L LEVEL 2.5V TO 3.3V LEVEL SHIFTER

=PP3V3_PWRON_SMU

R3091 1K 5% 1/16W MF-LF 402

R3093 1K 5% 1/16W MF-LF 402

NB_SUSPEND_ACK_L_R

NB_SUSPENDACK

NB_SUSPENDACK_L

NB_SUSPEND_ACK_L

R3090 10K 5% 1/16W MF-LF 402

Q03090 2N3904LF SOT23

Q03021 2N7002DW-X-F SOT-363

NOSTUFF R3092 0 5% 1/16W MF-LF 402

LEVEL SHIFT SMU TMS TO CPU (BACKUP PLAN)

=PPV_EI_CPU

=PP3V3_PWRON_SMU

R3026 1K 5% 1/16W MF-LF 402

R3027 1K 5% 1/16W MF-LF 402

JTAG_CPU_TMS_2_L

JTAG_SMU_TMS_2_R

JTAG_CPU_TMS_2_R

R3028 33 5% 1/16W MF-LF 402

JTAG_CPU_TMS

SMU_CPU_TMS

R3020 10K 5% 1/16W MF-LF 402

Q03030 2N3904LF SOT23

Q03031 2N7002DW-X-F SOT-363

LEFTOVER FROM UNUSED PRIMARY PLAN - NOT STUFFED

NOSTUFF U5640 SN74AUC2G125 VSSOP

SMU JTAG TCK TO CPU (BACKUP PLAN)

=PPV_EI_CPU

R3081 1K 5% 1/16W MF-LF 402

R3082 33 5% 1/16W MF-LF 402

JTAG_CPU_TCK_2_R

JTAG_CPU_TCK

=PP3V3_RUN_SMU

R3080 4.7K 5% 1/16W MF-LF 402

Q03081 2N7002DW-X-F SOT-363

SMU_JTAG_TCK_L

Q03080 2N7002DW-X-F SOT-363

SMU_JTAG_TCK

STUFF IF USING REGISTERED DIMM

=PP3V3_PWRON_SMU

NOSTUFF R3040 1K 5% 1/16W MF-LF 402

SMU_IO_RESET

NOSTUFF Q03040 2N7002 SOT23-LF

SYS_IO_RST_L_R

SHARE SMU JTAG TCK WITH CPU AND NB (PRIMARY PLAN)
SHARE SMU JTAG TDI WITH CPU AND NB (PRIMARY PLAN)
NOTE: WE WENT WITH BACKUP PLAN, PRIMARY REMOVED TO AVOID STUBS

SYS_NORTH_RESET FROM SMU TO NB_PU_RST

SAME AS Q63

=PP3V3_PWRON_SMU

R3006 10K 5% 1/16W MF-LF 402

R3010 4.7K 5% 1/16W MF-LF 402

NB_PU_RESET

=PP2V5_PWRON_NB_MISC

R3007 4.7K 5% 1/16W MF-LF 402

NB_PU_RST_L

SYS_NORTH_RESET_L

Q03005 2N7002DW-X-F SOT-363

Q03000 2N7002DW-X-F SOT-363

NOSTUFF R3008 0 5% 1/16W MF-LF 402

SYS_NORTH_RESET_L_R

NOSTUFF R3098 0 5% 1/16W MF-LF 402

NOSTUFF Q03006 2N7002 SOT23-LF

SYS_SLEEP

NOSTUFF R3009 0 5% 1/16W MF-LF 402

SYS_2SLEEP_R

CONSIDER COMBINING Q3040 AND Q3006 TO A DUAL PART

SHARE CPU AND NB JTAG TDO WITH SMU

=PP3V3_PWRON_SMU

SMU DRIVES 3.3V PUSH-PULL ON ALL JTAG-RELATED PINS

CRITICAL

U3070 SN74LVC2G157 TSSOP

JTAG_CPU_TDO_3V3

JTAG_NB_TDO

SMU_CPU_NB_SEL

VIH=2V

SMU_JTAG_TDO

NC_JTAGMUX_3

C3070 0.1UF 20% 16V CERM 402

SMU JTAG TDI TO CPU (BACKUP PLAN)

PCB: PLACE U3070 NEAR SMU

=PPV_EI_CPU

R3084 1K 5% 1/16W MF-LF 402

R3085 33 5% 1/16W MF-LF 402

JTAG_CPU_TDI_2_R

JTAG_CPU_TDI

=PP3V3_RUN_SMU

R3083 4.7K 5% 1/16W MF-LF 402

Q03081 2N7002DW-X-F SOT-363

SMU_JTAG_TDI_L

SMU_JTAG_TDI

Q03080 2N7002DW-X-F SOT-363

SHARE CPU AND NB JTAG TMS WITH SMU

=PP2V5_PWRON_NB_MISC

C3071 0.1UF 20% 16V CERM 402

PCB: PLACE U3071 NEAR SMU OR NEAR KODIAK.

CRITICAL

U3071 74LVC1G SC70-6

TO LEVEL SHIFTER

SMU_CPU_TMS

3.3V TOLERANT

STRAIGHT TO NB

JTAG_NB_TMS

SMU_JTAG_TMS

LEVEL SHIFT TDO FROM CPU TO MUX

=PP3V3_PWRON_SMU

R3051 1K 5% 1/16W MF-LF 402

R3052 100 5% 1/16W MF-LF 402

JTAG_CPU_TDO_L

JTAG_CPU_TDO_3V3

JTAG_CPU_TDO_R

R3050 10K 5% 1/16W MF-LF 402

Q03050 2N3904LF SOT23

Q03021 2N7002DW-X-F SOT-363

JTAG_CPU_TDO

PCB: PLACE R3050, Q3050, R3051 NEAR CPU. PLACE Q3021, R3052 NEAR SMU.

NB JTAG IS A DEVELOPMENT ONLY FEATURE

PLACE 0-OHM R3030 AND R3031 TO AVOID STUBS

R3030,R3031,C3031,U3031,R3032,R3033 SHOULD MOVE TO DEVELOPMENT BOM POST RAMP

SMU_JTAG_TDI

R3030 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

C3031 0.1UF 20% 16V CERM 402

PCB: PLACE U3030 AND U3031 NEAR CPU AND KODIAK.
PCB: PLACE 33 OHM RES NEAR U3030/31 PART.

VCC RANGE 0.8V - 2.7V

U3031 SN74AUC2G34 SOT23-6

R3032 33 5% 1/16W MF-LF 402

SMU_JTAG_NB_TDI

JTAG_NB_TDI_R

JTAG_NB_TDI

VIH = 2.0V, 3.3V TOLERANT

SMU_JTAG_TCK

R3031 0 5% 1/16W MF-LF 402

=PP2V5_PWRON_NB_MISC

SMU_JTAG_NB_TCK

VCC RANGE 0.8V - 2.7V

U3031 SN74AUC2G34 SOT23-6

R3033 33 5% 1/16W MF-LF 402

JTAG_NB_TCK_R

JTAG_NB_TCK

R3035 10K 5% 1/16W MF-LF 402

PULLUP IF KODIAK JTAG IS NOSTUFFED

VIH = 2.0V, 3.3V TOLERANT

PULLDOWNS TO BUFFERS/LOGIC GATES

R3036 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TDI

R3037 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TCK

R3070 100K 5% 1/16W MF-LF 402 — SMU_JTAG_TMS

R3071 100K 5% 1/16W MF-LF 402 — SMU_CPU_NB_SEL

SMU SUPPLEMENTAL (3)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 30 OF 154	

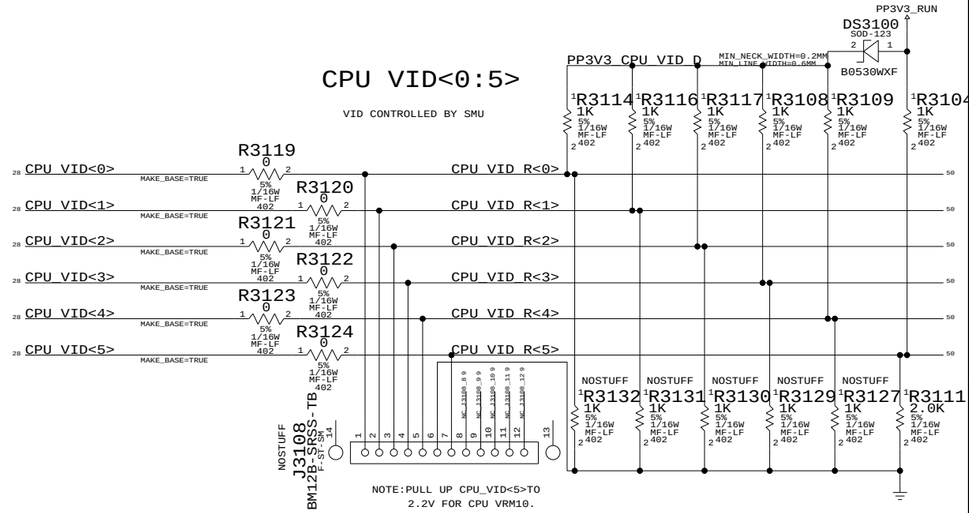
SMU ALIASES

ALIASES ARE ONLY NECESSARY WHERE USE DIFFERS FROM Q63.

COMMENT (ONLY IF USE DIFFERS FROM Q63)	M23 NET NAME	M23 SMU ALLOCATION		Q63 NET NAME (SHARED PAGE)
		CPU_SENSE_I0	P0.0	
		CPU_SENSE_V0	P0.1	
		CPU_TEMP0	P0.2	
Q63 NC'S THESE AS IT USES A SAT.		CPU_BYPASS	P0.3	
	9 NC_SMU_FAN_RPM3	FAN_CNTL0_4	P0.4	SMU_FAN_RPM3 28
M23/M33 DOESN'T HAVE THOSE FANS.	9 NC_SMU_FAN_RPM4	FAN_CNTL0_5	P0.5	SMU_FAN_RPM4 28
	9 NC_SMU_FAN_RPM5	FAN_CNTL0_6	P0.6	SMU_FAN_RPM5 28
Q63 USES SMU_SER_SEL FOR SPDIF-SMU-DEBUG. NOT M23/M33 FEATURE.	9 NC_SMU_SER_SEL	SMU_SCCL_SEL	P0.7	SMU_SER_SEL 28
M23/M33 DOESN'T USE. P1.0 NC ON PG 7.		CPU_SENSE_I1	P1.0	
		CPU_SENSE_V1	P1.1	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		CPU_TEMP1	P1.2	
		PS1_3	P1.3	
M23/M33 DOESN'T USE P1.4. NC ON PG 7.		PS1_4	P1.4	
		POWERFAIL*	P1.5	
CPU_VID_LE0 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE0	CPU_VID_LE0	P1.6	SMU_FAN_TACH9 28
CONSIDER DOOR_AJAR FOR M23/M33 DIMM ACCESS DOOR?	9 NC_SYS_DOOR_AJAR_L	DOOR_AJAR*	P1.7	SYS_DOOR_AJAR_L 28
CPU_VID_LE1 FOR Q82. NOT M23/M33 FEATURE.	9 NC_SMU_CPU_VID_LE1	CPU_VID_LE1	P2.0	SMU_FAN_TACH6 28
M23/M33 DOESN'T HAVE THIS FAN.	9 NC_SMU_FAN_TACH7	FAN_TACH2_1	P2.1	SMU_FAN_TACH7 28
		FAN_TACH2_2	P2.2	
		FAN_TACH2_3	P2.3	
		FAN_TACH2_4	P2.4	
M23/M33 DOESN'T HAVE FAN TACHS P2.5, P2.6, P2.7.	9 NC_SMU_FAN_TACH3	FAN_TACH2_5	P2.5	SMU_FAN_TACH3 28
M23/M33 USES TACH0 (P2.2), TACH1 (P2.3), TACH2 (P2.4) ONLY.	9 NC_SMU_FAN_TACH4	FAN_TACH2_6	P2.6	SMU_FAN_TACH4 28
	9 NC_SMU_FAN_TACH5	FAN_TACH2_7	P2.7	SMU_FAN_TACH5 28
M23/M33 ONLY CONNECTS I2C TO KODIAK NOW; CPU HAS PULLUPS ON ITS PG.	39 28 I2C_SMU_A_SDA	IIC_A_DAT	P3.0	I2C_SMU_A_SDA_IN 28
	39 28 I2C_SMU_A_SCL	IIC_A_CLK	P3.1	I2C_SMU_A_SDA_OUT_L 28
	30 SMU_JTAG_TDI	TDI	P3.2	I2C_SMU_A_SCL_IN 28
	30 SMU_JTAG_TCK	TCK	P3.3	I2C_SMU_A_SCL_OUT_L 28
		IIC_E_DAT	P3.4	
		IIC_E_CLK	P3.5	
		DIAG_LED	P3.6	
		OVERTEMP*	P3.7	
		CPU_VID[0]	P6.0	
		CPU_VID[1]	P6.1	
		CPU_VID[2]	P6.2	
		CPU_VID[3]	P6.3	
		CPU_VID[4]	P6.4	
		CPU_VID[5]	P6.5	
		DEBUG_RXD	P6.6	
		DEBUG_TXD	P6.7	
		IIC_B_DAT	P7.0	
		IIC_B_CLK	P7.1	
Q63 USE OF P7.2 IS PWM FAN — SELECT BETWEEN CPU OR NB TMS AND TDO FROM/TO SMU	30 SMU_CPU_NB_SEL	CPU_TMS	P7.2	I2C_SMU_CPU_SDA_IN 28
		FAN_CNTL7_3	P7.3	
M23/M33 DOESN'T HAVE THIS FAN (P7.4)	9 NC_I2C_SMU_CPU_SCL_IN	FAN_CNTL7_4	P7.4	I2C_SMU_CPU_SCL_IN 28
M23/M33 USES FAN_RPM0 (P7.3), FAN_RPM1 (P7.5), FAN_RPM2 (P7.7) ONLY.		FAN_CNTL7_5	P7.5	
		VDNAP2	P7.6	
		FAN_CNTL7_7	P7.7	
		SYSTEM_LED	P8.0	
		NB_RESET*	P8.1	
		PME*	P8.2	
M23/M33 DOESN'T NEED TO MAKE VDNAP0 DO TRIPLE-DUTY.	24 SB_VDNAP0	VDNAP0	P8.3	SB_CPU_VDNAP0_OR_QREQ_OR_SPDIF 28
		SLEWING*	P8.4	
	30 SMU_JTAG_TMS	NB_TMS	P8.5	I2C_SMU_CPU_SDA_OUT_L 28
		POWERUP*	P8.6	
		SLEEP	P8.7	
		CLK_RESET*	P9.0	
Q63 USE OF P9.1 IS TACH 8.	29 CPU_HRESET	CPU_HRESET	P9.1	SMU_FAN_TACH8 28
		SMU_DOORBELL*	P9.2	
		STOP_XTAL*	P9.3	
SMU USES P1.1, P1.2, P1.3, P9.5, P9.6 FOR PWRSEQ ON PG 7.		PS9_5	P9.5	
		PS9_6	P9.6	
M23/M33 HAS NO SLOTS.	9 NC_SLOT_TOTAL_PWR	SLOT_TOTAL_PWR	P9.7	SYS_SLOT_PWR 28
		VDNAP1	P10.0	
		IO_RESET*	P10.1	
		SUSPEND_ACK*	P10.2	
		SUSPEND_IO_ACK*	P10.3	
		SUSPEND_REQ*	P10.4	
		PWR_BUTTON*	P10.5	
		RST_BUTTON*	P10.6	
	30 SMU_JTAG_TDO	TDO	P10.7	I2C_SMU_CPU_SCL_OUT_L 28

CPU VID<0:5>

VID CONTROLLED BY SMU



NOTE:PULL UP CPU_VID<5>TO 2.2V FOR CPU VRM10.

NOTE: SC2642 VID PINS HAVE LEAKAGE TO GND. SO PULLUPS MUST BE 1K

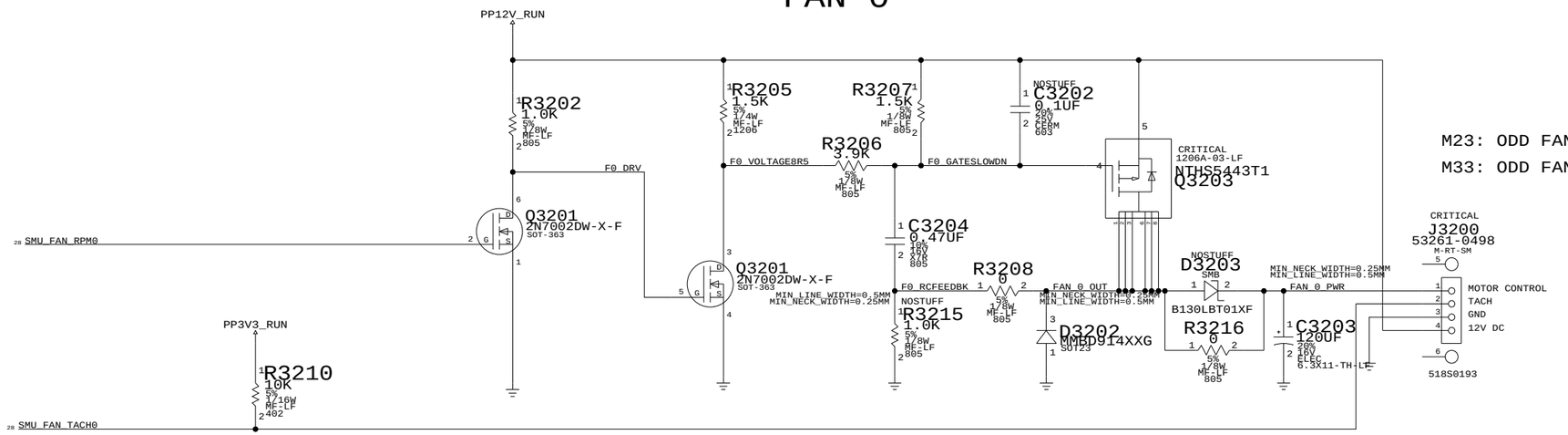
SMU SUPPLEMENTAL (4)

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

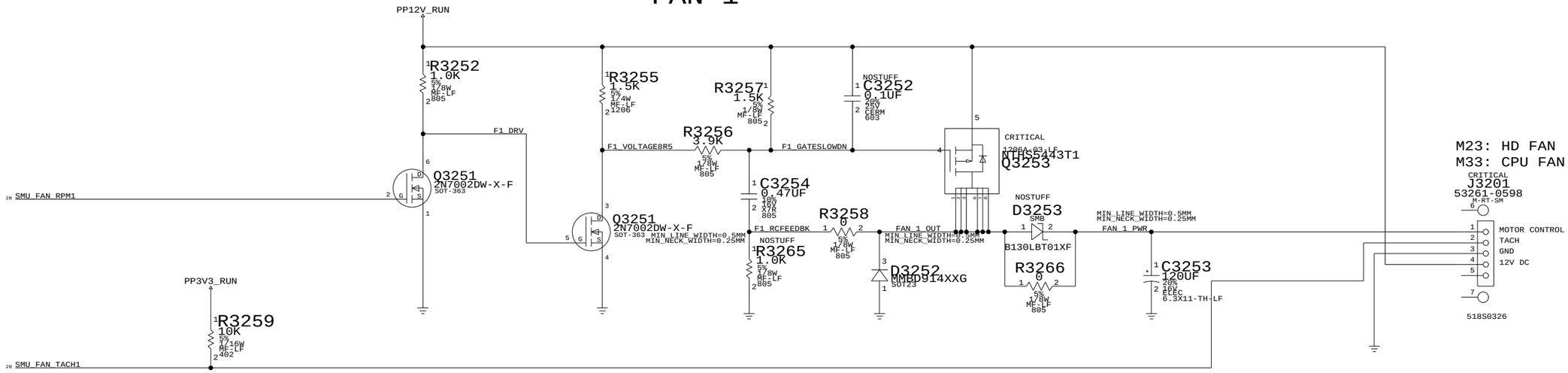
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 31 OF 154	

FAN 0



M23: ODD FAN
M33: ODD FAN

FAN 1



M23: HD FAN
M33: CPU FAN

Fan 0, 1 & System Temp

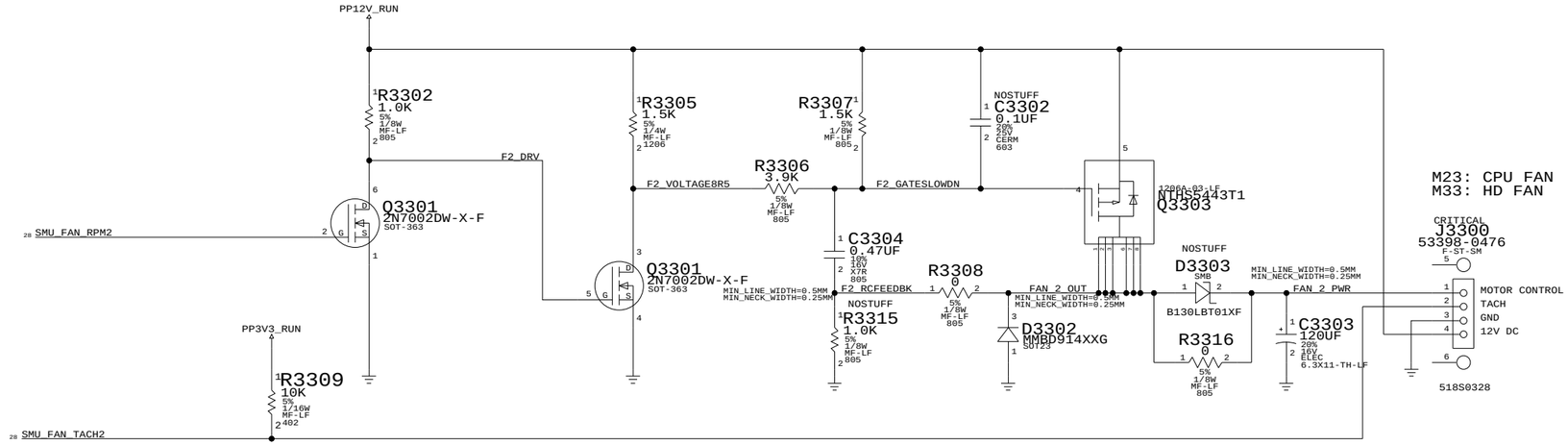
SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

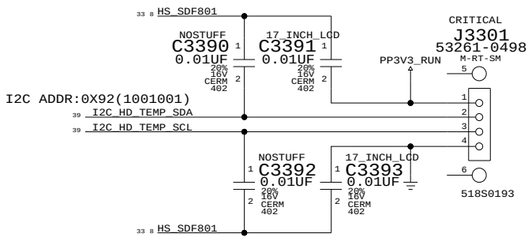
SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT
NONE	32 OF 154

FAN 2

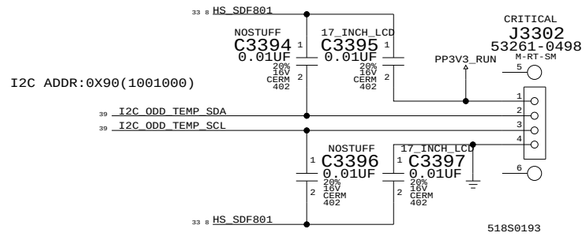


HD TEMP SENSOR



CAPS ARE FOR EMC ON M23 ONLY

ODD TEMP SENSOR



CAPS ARE FOR EMC ON M23 ONLY

Fan 2 & HD Temp

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 33 OF 154	

SMU AND NB I2C A BUS

SMU
MASTER
28 31 I2C_SMU_A_SDA — NET_SPACING_TYPE=I2C
28 31 I2C_SMU_A_SCL — NET_SPACING_TYPE=I2C

39 7 =PP3V3_RUN_I2C
R3953 2.0K 5% 1/16W MF-LF 402
R3969 2.0K 5% 1/16W MF-LF 402
VDIV=2.9V
NOSTUFF R3954 15K 5% 1/16W MF-LF 402
NOSTUFF R3955 15K 5% 1/16W MF-LF 402

=PP2V5_RUN_I2C 7 39
R3958 2.0K 5% 1/16W MF-LF 402
R3959 2.0K 5% 1/16W MF-LF 402

KODIAK
I2C_NB_A_SDA 29 — NET_SPACING_TYPE=I2C
I2C_NB_A_SCL 29 — NET_SPACING_TYPE=I2C

Q3902 SI2302ADSE3 SOT23-3
Q3902_1 — R3962 0 5% 1/16W MF-LF 402 — =PP2V5_RUN_I2C 7 39
Q3901 SI2302ADSE3 SOT23-3
Q3901_1 — R3963 0 5% 1/16W MF-LF 402

SB I2C BUS

SHASTA
MASTER
U2300
24 I2C_SB_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=AUDIO
24 I2C_SB_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=AUDIO
PINS Y9, AB7

PP3V3_RUN
R3915 1K 5% 1/16W MF-LF 402
R3914 1K 5% 1/16W MF-LF 402

AUDIO
U9500 / AU300
147 I2C_AUDIO_SDA
147 I2C_AUDIO_SCL
PINS 18, 19

SMU I2C B BUS

PP3V3_PWRON
R3903 2.0K 5% 1/16W MF-LF 402
R3902 2.0K 5% 1/16W MF-LF 402

SMU
MASTER
U1300
28 I2C_SMU_B_SDA MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
28 I2C_SMU_B_SCL MAKE_BASE=TRUE — NET_SPACING_TYPE=I2C
PINS 26, 27

PULSAR2
U2600
26 I2C_CLOCK_B_SDA — R3904 33 5% 1/16W MF-LF 402
26 I2C_CLOCK_B_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:0XD5

ALS HEADER
J2901
29 I2C_ALS_SDA
R3908 33 5% 1/16W MF-LF 402
29 I2C_ALS_SCL — NET_SPACING_TYPE=I2C
I2C ADDR:52

SMU I2C E BUS

PP3V3_ALL
R3907 2.0K 5% 1/16W MF-LF 402
R3906 2.0K 5% 1/16W MF-LF 402
R3965 0 5% 1/16W MF-LF 402
R3964 0 5% 1/16W MF-LF 402

SMU 'E'
MASTER
U2800
28 I2C_SMU_E_SDA I2C
28 I2C_SMU_E_SCL I2C
PINS 34,35

RTC
U2801
I2C I2C_RTC_SDA 28
I2C I2C_RTC_SCL 28
PINS 5, 6

NB I2C C BUS

39 7 =PP2V5_RUN_I2C
R3970 2.0K 5% 1/16W MF-LF 402
R3971 2.0K 5% 1/16W MF-LF 402

KODIAK I2C C
20 I2C_NB_C_SDA — NET_SPACING_TYPE=I2C
20 I2C_NB_C_SCL — NET_SPACING_TYPE=I2C

39 7 =PP3V3_RUN_I2C
R3972 2.0K 5% 1/16W MF-LF 402
R3973 2.0K 5% 1/16W MF-LF 402

MAKE_BASE=TRUE — I2C_NB_C_3V3_SDA — NET_SPACING_TYPE=I2C
MAKE_BASE=TRUE — I2C_NB_C_3V3_SCL — NET_SPACING_TYPE=I2C

Q3970 SI2302ADSE3 SOT23-3
Q3970_G — R3974 0 5% 1/16W MF-LF 402
Q3971 SI2302ADSE3 SOT23-3
Q3971_G — R3975 0 5% 1/16W MF-LF 402 — =PP2V5_RUN_I2C 7 39

ODD TEMP SENSOR HEADER
J3302
I2C_ODD_TEMP_SDA 33 — R3976 33 5% 1/16W MF-LF 402
I2C_ODD_TEMP_SCL 33 — NET_SPACING_TYPE=I2C
I2C ADDR:90

HD TEMP SENSOR HEADER
J3301
I2C_HD_TEMP_SDA 33 — R3977 33 5% 1/16W MF-LF 402
I2C_HD_TEMP_SCL 33 — NET_SPACING_TYPE=I2C
I2C ADDR:92

GPU TEMP SENSOR
U9390
I2C_GPU_DIODE_SDA 93 — R3978 33 5% 1/16W MF-LF 402
I2C_GPU_DIODE_SCL 93 — NET_SPACING_TYPE=I2C
I2C ADDR:9C

KODIAK TEMP SENSOR
U2080
I2C_NB_TEMP_SDA 20 — R3979 33 5% 1/16W MF-LF 402
I2C_NB_TEMP_SCL 20 — NET_SPACING_TYPE=I2C
I2C ADDR:98

NB I2C B BUS

30 28 20 7 =PP2V5_PWRON_NB_MISC
59 58 20 7 =PP1V8_PWRON_NBMEM

KODIAK I2C B
MASTER
U1900
20 I2C_NB_B_SDA — NET_SPACING_TYPE=I2C
20 I2C_NB_B_SCL — NET_SPACING_TYPE=I2C
PINS AG04, AK03

R3925 2.0K 5% 1/16W MF-LF 402
R3936 2.0K 5% 1/16W MF-LF 402
Q3903 SI2302ADSE3 SOT23-3
Q3903_G — R3924 0 5% 1/16W MF-LF 402
R3931 2.0K 5% 1/16W MF-LF 402
Q3904 SI2302ADSE3 SOT23-3
Q3904_G — R3937 0 5% 1/16W MF-LF 402
R3938 2.0K 5% 1/16W MF-LF 402

DDR2 DIMMS
I2C_NB_RAM_SDA 67 — NET_SPACING_TYPE=I2C
I2C_NB_RAM_SCL 67 — NET_SPACING_TYPE=I2C

I2C Connections

SYNC_MASTER=FINO-ME SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 39 OF 154	

Q63 APPLICATION IS PP1V5 PWRON

=PPV_EI_NB 7 41 42 56

XW4100 NO_TEST=YES

6 PP_VEINB

P4MM SM 1

PP4100

U1900
BGA
(7 OF 10)
PART 0
PWR/GND
KODIAK-ASIC-040812

AB01	GND_0	VD2_0	AB02
AB04	GND_1	VD2_1	AB05
AB07	GND_2	VD2_2	AB08
AB10	GND_3	VD2_3	AB11
AB12	GND_4	VD2_4	AB13
AD02	GND_5	VD2_5	AD01
AD05	GND_6	VD2_6	AD04
AD08	GND_7	VD2_7	AD07
AD11	GND_8	VD2_8	AD10
AD13	GND_9	VD2_9	AD12
AD17	GND_10	VD2_10	AD16
AD21	GND_11	VD2_11	AD20
AE15	GND_12	VD2_12	AE14
AE19	GND_13	VD2_13	AE18
AF07	GND_14	VD2_14	AF08
AF10	GND_15	VD2_15	AF11
AF13	GND_16	VD2_16	AF15
AF17	GND_17	VD2_17	AF19
AG11	GND_18	VD2_18	AG13
AG15	GND_19	VD2_19	AG17
AG19	GND_20	VD2_20	AG21
AH02	GND_21	VD2_21	AH04
AH05	GND_22	VD2_22	AH07
AH08	GND_23	VD2_23	AH09
AJ13	GND_24	VD2_24	AJ11
AJ17	GND_25	VD2_25	AJ15
AJ21	GND_26	VD2_26	AJ19
AK01	GND_27	VD2_27	AK02
AK04	GND_28	VD2_28	AK05
AK07	GND_29	VD2_29	AK09
AK11	GND_30	VD2_30	AK13
AK15	GND_31	VD2_31	AK17
AK19	GND_32	VD2_32	AK21
AM02	GND_33	VD2_33	AM01
AM05	GND_34	VD2_34	AM04
AM09	GND_35	VD2_35	AM07
AM13	GND_36	VD2_36	AM11
AM17	GND_37	VD2_37	AM15
AM21	GND_38	VD2_38	AM19
AN04	GND_39	VD2_39	AN05
AN07	GND_40	VD2_40	AN09
AN11	GND_41	VD2_41	AN13
AN15	GND_42	VD2_42	AN17
AN19	GND_43	VD2_43	AN21
AP01	GND_44	VD2_44	AP02
AR05	GND_45	VD2_45	AR07
AR09	GND_46	VD2_46	AR11
AR13	GND_47	VD2_47	AR15
AR17	GND_48	VD2_48	AR19
AR21	GND_49	VD2_49	AT05
AT03	GND_50	VD2_50	AT09
AT07	GND_51	VD2_51	AT13
AT11	GND_52	VD2_52	AT17
AT15	GND_53	VD2_53	AT21
AT19	GND_54	VD2_54	K02
K01	GND_55	VD2_55	K05
K04	GND_56	VD2_56	K08
M02	GND_57	VD2_57	M01
M05	GND_58	VD2_58	M04
M08	GND_59	VD2_59	M07
P01	GND_60	VD2_60	M10
P04	GND_61	VD2_61	P02
P07	GND_62	VD2_62	P05
P10	GND_63	VD2_63	P08
P12	GND_64	VD2_64	P11
T02	GND_65	VD2_65	P13
T05	GND_66	VD2_66	T01
T08	GND_67	VD2_67	T04
T11	GND_68	VD2_68	T07
T13	GND_69	VD2_69	T10
V01	GND_70	VD2_70	T12
V04	GND_71	VD2_71	V02
V07	GND_72	VD2_72	V05
V10	GND_73	VD2_73	V08
V12	GND_74	VD2_74	V11
Y02	GND_75	VD2_75	V13
Y05	GND_76	VD2_76	Y01
Y08	GND_77	VD2_77	Y04
Y11	GND_78	VD2_78	Y07
Y13	GND_79	VD2_79	Y10
AF01	GND_80	VD2_80	Y12
AF04	GND_81	VD2_81	
AF21	GND_82		
AJ08	GND_83		
AJ09	GND_84		

Q63 APPLICATION IS PP1V5 PWRON

56 42 41 7 =PPV_EI_NB

C4168	C4146	C4143	C4139	C4137	C4113	C4112	C4106	C4122	C4100
C4169	C4147	C4145	C4140	C4138	C4114	C4110	C4107	C4133	C4111
C4170	C4149	C4148	C4142	C4141	C4115	C4109	C4108	C4155	C4144
C4171	C4161	C4159	C4152	C4150	C4125	C4118	C4116	C4181	C4166
C4172	C4162	C4160	C4153	C4151	C4126	C4124	C4117	C4101	C4177
C4174	C4165	C4163	C4157	C4154	C4127	C4123		C4104	C4102
C4173	C4167	C4164	C4158	C4156	C4128	C4121	C4120	C4105	C4103
C4180	C4179	C4178	C4176	C4175	C4136	C4135	C4134	C4130	C4129
								C4132	C4131

All: 0.22UF 20% 6.3V X5R 402

KODIAK EI PWR & CAPS

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

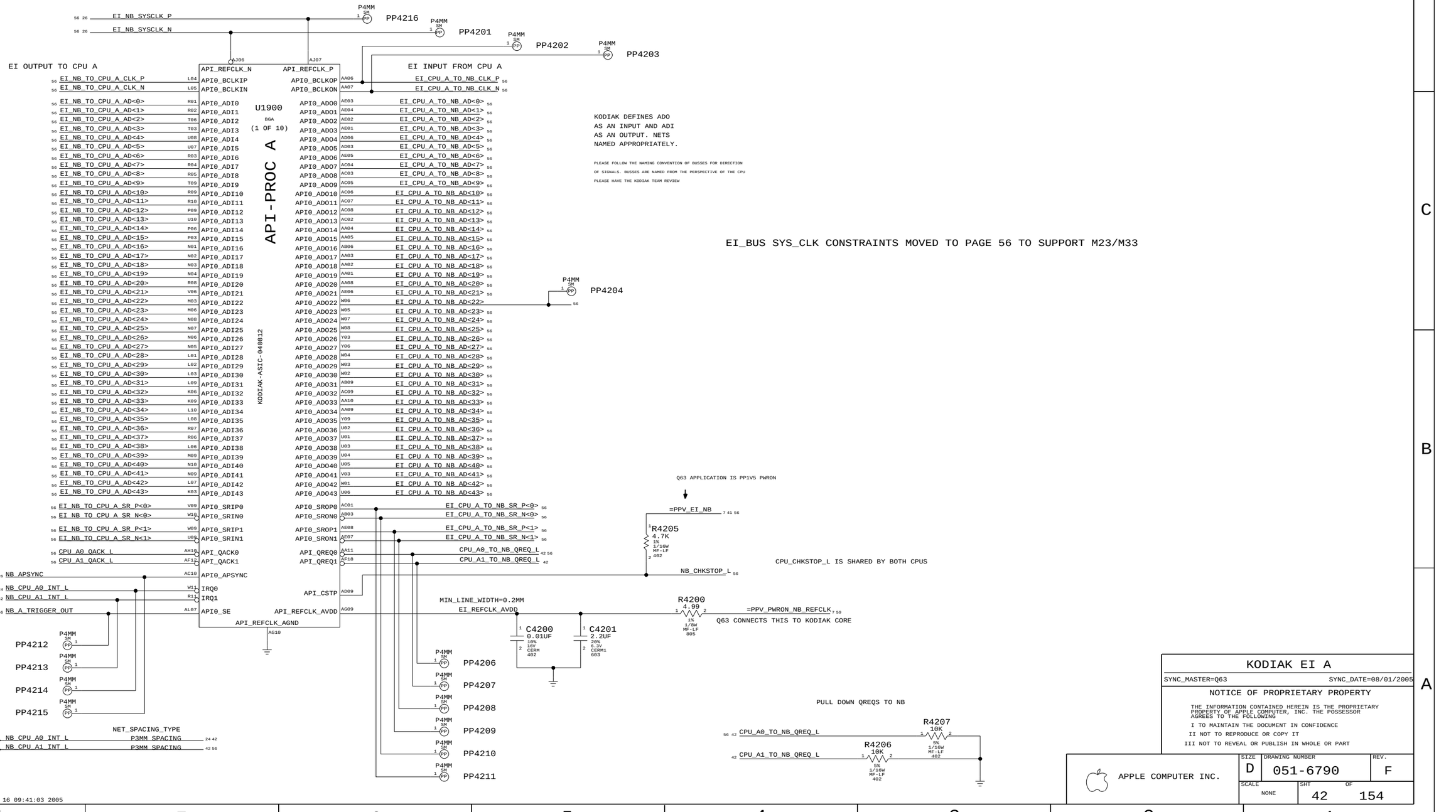
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	41	154

LAST_MODIFIED=Wed Nov 16 09:41:02 2005

DRAWING
TITLE=SCHEMATIC
ABBREV=SCHEMATIC



EI_NB_TO_CPU_A_CLK_P	L04	EI_NB_TO_CPU_A_CLK_N	L05				
EI_NB_TO_CPU_A_AD<0>	R01	EI_NB_TO_CPU_A_AD<1>	R02	EI_NB_TO_CPU_A_AD<2>	T06	EI_NB_TO_CPU_A_AD<3>	T03
EI_NB_TO_CPU_A_AD<4>	U08	EI_NB_TO_CPU_A_AD<5>	U07	EI_NB_TO_CPU_A_AD<6>	R03	EI_NB_TO_CPU_A_AD<7>	R04
EI_NB_TO_CPU_A_AD<8>	R05	EI_NB_TO_CPU_A_AD<9>	T09	EI_NB_TO_CPU_A_AD<10>	R09	EI_NB_TO_CPU_A_AD<11>	R10
EI_NB_TO_CPU_A_AD<12>	P09	EI_NB_TO_CPU_A_AD<13>	U10	EI_NB_TO_CPU_A_AD<14>	P06	EI_NB_TO_CPU_A_AD<15>	P03
EI_NB_TO_CPU_A_AD<16>	N01	EI_NB_TO_CPU_A_AD<17>	N02	EI_NB_TO_CPU_A_AD<18>	N03	EI_NB_TO_CPU_A_AD<19>	N04
EI_NB_TO_CPU_A_AD<20>	R08	EI_NB_TO_CPU_A_AD<21>	V06	EI_NB_TO_CPU_A_AD<22>	M03	EI_NB_TO_CPU_A_AD<23>	M06
EI_NB_TO_CPU_A_AD<24>	N08	EI_NB_TO_CPU_A_AD<25>	N07	EI_NB_TO_CPU_A_AD<26>	N06	EI_NB_TO_CPU_A_AD<27>	N05
EI_NB_TO_CPU_A_AD<28>	L01	EI_NB_TO_CPU_A_AD<29>	L02	EI_NB_TO_CPU_A_AD<30>	L03	EI_NB_TO_CPU_A_AD<31>	L09
EI_NB_TO_CPU_A_AD<32>	K06	EI_NB_TO_CPU_A_AD<33>	K09	EI_NB_TO_CPU_A_AD<34>	L10	EI_NB_TO_CPU_A_AD<35>	L08
EI_NB_TO_CPU_A_AD<36>	R07	EI_NB_TO_CPU_A_AD<37>	R06	EI_NB_TO_CPU_A_AD<38>	L06	EI_NB_TO_CPU_A_AD<39>	M09
EI_NB_TO_CPU_A_AD<40>	N10	EI_NB_TO_CPU_A_AD<41>	N09	EI_NB_TO_CPU_A_AD<42>	L07	EI_NB_TO_CPU_A_AD<43>	K03

EI_NB_TO_CPU_A_SR_P<0>	V09	EI_NB_TO_CPU_A_SR_N<0>	W10
EI_NB_TO_CPU_A_SR_P<1>	W09	EI_NB_TO_CPU_A_SR_N<1>	U09

API0_ADO0	AE03	API0_ADO1	AE04
API0_ADO2	AE02	API0_ADO3	AE01
API0_ADO4	AD06	API0_ADO5	AD03
API0_ADO6	AE05	API0_ADO7	AC04
API0_ADO8	AC03	API0_ADO9	AC05
API0_ADO10	AC06	API0_ADO11	AC07
API0_ADO12	AC08	API0_ADO13	AC02
API0_ADO14	AA04	API0_ADO15	AA05
API0_ADO16	AB06	API0_ADO17	AA03
API0_ADO18	AA02	API0_ADO19	AA01
API0_ADO20	AA08	API0_ADO21	AE06
API0_ADO22	W06	API0_ADO23	W05
API0_ADO24	W07	API0_ADO25	W08
API0_ADO26	Y03	API0_ADO27	Y06
API0_ADO28	W04	API0_ADO29	W03
API0_ADO30	W02	API0_ADO31	AB09
API0_ADO32	AC09	API0_ADO33	AA10
API0_ADO34	AA09	API0_ADO35	Y09
API0_ADO36	U02	API0_ADO37	U01
API0_ADO38	U03	API0_ADO39	U04
API0_ADO40	U05	API0_ADO41	V03
API0_ADO42	W01	API0_ADO43	U06

API0_SROP0	AC01	API0_SRON0	AB03
API0_SROP1	AE08	API0_SRON1	AE07

EI_CPU_A_TO_NB_AD<0>	EI_CPU_A_TO_NB_AD<1>	EI_CPU_A_TO_NB_AD<2>	EI_CPU_A_TO_NB_AD<3>
EI_CPU_A_TO_NB_AD<4>	EI_CPU_A_TO_NB_AD<5>	EI_CPU_A_TO_NB_AD<6>	EI_CPU_A_TO_NB_AD<7>
EI_CPU_A_TO_NB_AD<8>	EI_CPU_A_TO_NB_AD<9>	EI_CPU_A_TO_NB_AD<10>	EI_CPU_A_TO_NB_AD<11>
EI_CPU_A_TO_NB_AD<12>	EI_CPU_A_TO_NB_AD<13>	EI_CPU_A_TO_NB_AD<14>	EI_CPU_A_TO_NB_AD<15>
EI_CPU_A_TO_NB_AD<16>	EI_CPU_A_TO_NB_AD<17>	EI_CPU_A_TO_NB_AD<18>	EI_CPU_A_TO_NB_AD<19>
EI_CPU_A_TO_NB_AD<20>	EI_CPU_A_TO_NB_AD<21>	EI_CPU_A_TO_NB_AD<22>	EI_CPU_A_TO_NB_AD<23>
EI_CPU_A_TO_NB_AD<24>	EI_CPU_A_TO_NB_AD<25>	EI_CPU_A_TO_NB_AD<26>	EI_CPU_A_TO_NB_AD<27>
EI_CPU_A_TO_NB_AD<28>	EI_CPU_A_TO_NB_AD<29>	EI_CPU_A_TO_NB_AD<30>	EI_CPU_A_TO_NB_AD<31>
EI_CPU_A_TO_NB_AD<32>	EI_CPU_A_TO_NB_AD<33>	EI_CPU_A_TO_NB_AD<34>	EI_CPU_A_TO_NB_AD<35>
EI_CPU_A_TO_NB_AD<36>	EI_CPU_A_TO_NB_AD<37>	EI_CPU_A_TO_NB_AD<38>	EI_CPU_A_TO_NB_AD<39>
EI_CPU_A_TO_NB_AD<40>	EI_CPU_A_TO_NB_AD<41>	EI_CPU_A_TO_NB_AD<42>	EI_CPU_A_TO_NB_AD<43>

EI_CPU_A_TO_NB_SR_P<0>	EI_CPU_A_TO_NB_SR_N<0>	EI_CPU_A_TO_NB_SR_P<1>	EI_CPU_A_TO_NB_SR_N<1>

NB_APSYNC	AC10	NB_CPU_A0_INT_L	W11
NB_CPU_A1_INT_L	R11	NB_A_TRIGGER_OUT	AL07

CPU_A0_QACK_L	AH10	CPU_A1_QACK_L	AF12

NB_CHKSTOP_L	AK10		

CPU_A0_TO_NB_QREQ_L	AA11	CPU_A1_TO_NB_QREQ_L	AF18

API0_SRIP0	V09	API0_SRIN0	W10
API0_SRIP1	W09	API0_SRIN1	U09

API_CSTP	AD09	API_REFCLK_AVDD	AG09
API_REFCLK_AGND	AG10		

NB_CPU_A0_INT_L	P3MM_SPACING	NB_CPU_A1_INT_L	P3MM_SPACING

CPU_A0_TO_NB_QREQ_L	CPU_A1_TO_NB_QREQ_L		

KODIAK EI A			
SYNC_MASTER=Q63	SYNC_DATE=08/01/2005		

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

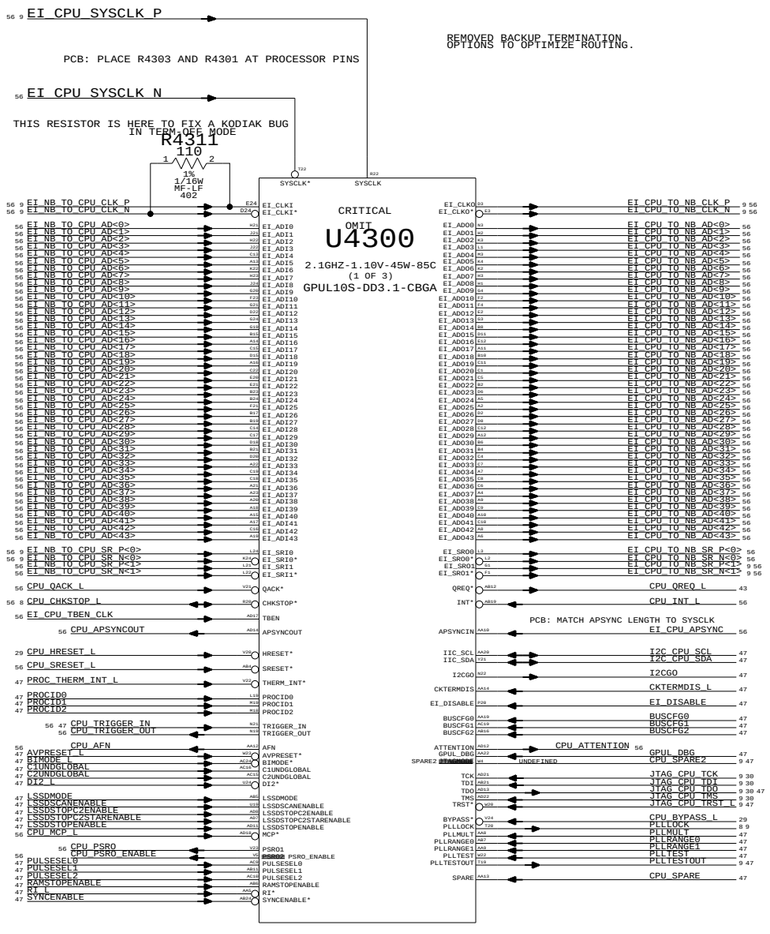
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

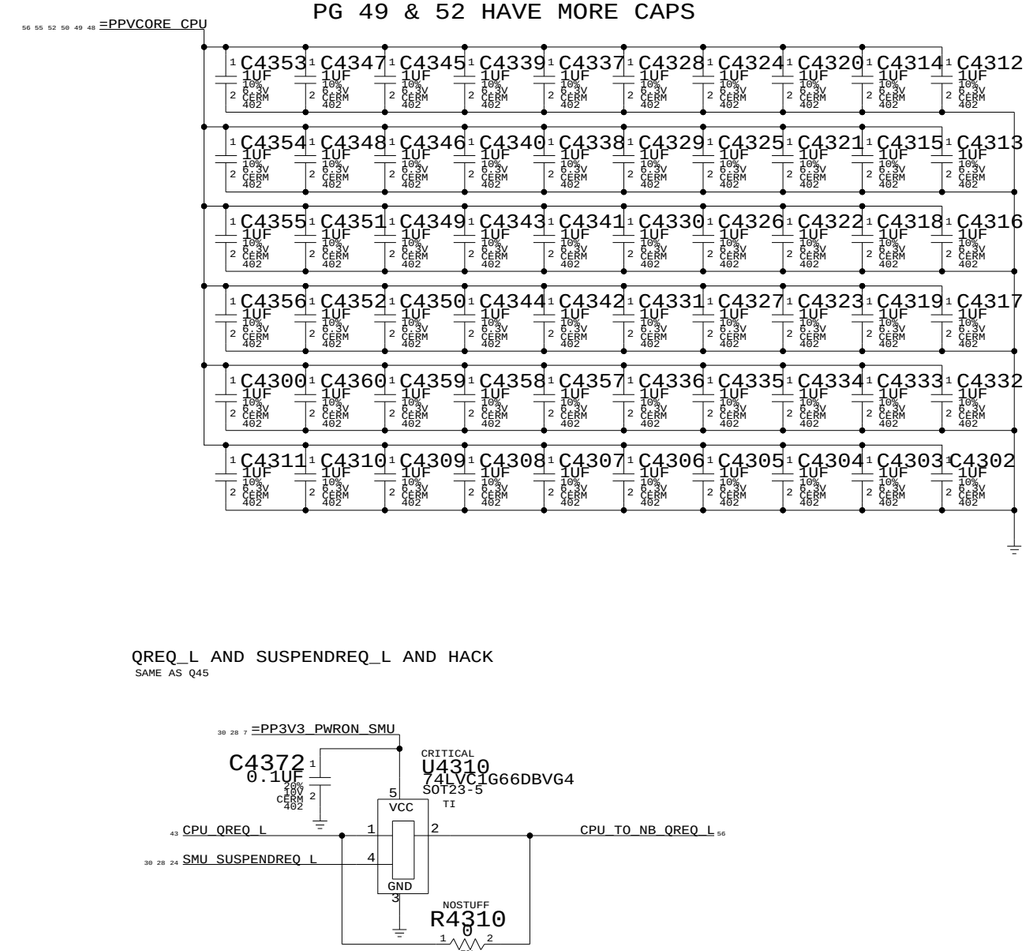
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 42 OF 154	

LAST_MODIFIED=Wed Nov 16 09:41:03 2005

DRAWING





CPU EI AND IO

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 43	OF: 154

PLEASE FOLLOW THE NAMING CONVENTION OF BUSSES FOR DIRECTION
OF SIGNALS. BUSSES ARE NAMED FROM THE PERSPECTIVE OF THE CPU
PLEASE HAVE THE KODIAK TEAM REVIEW

EI OUTPUT TO CPU B

EI INPUT FROM CPU B

U1900
BGA
(2 OF 10)
API-PROC B
KODIAK-ASIC-040812

EI_NB_TO_CPU_B_CLK_P	AT08	API1_BCLKIP	API1_BCLKOP	AT16	EI_CPU_B_TO_NB_CLK_P
EI_NB_TO_CPU_B_CLK_N	AR08	API1_BCLKIN	API1_BCLKON	AR16	EI_CPU_B_TO_NB_CLK_N
EI_NB_TO_CPU_B_AD<0>	AM12	API1_ADI0	API1_AD00	AP20	EI_CPU_B_TO_NB_AD<0>
EI_NB_TO_CPU_B_AD<1>	AN12	API1_ADI1	API1_AD01	AN20	EI_CPU_B_TO_NB_AD<1>
EI_NB_TO_CPU_B_AD<2>	AL12	API1_ADI2	API1_AD02	AR20	EI_CPU_B_TO_NB_AD<2>
EI_NB_TO_CPU_B_AD<3>	AK12	API1_ADI3	API1_AD03	AT20	EI_CPU_B_TO_NB_AD<3>
EI_NB_TO_CPU_B_AD<4>	AP11	API1_ADI4	API1_AD04	AL19	EI_CPU_B_TO_NB_AD<4>
EI_NB_TO_CPU_B_AD<5>	AL11	API1_ADI5	API1_AD05	AP19	EI_CPU_B_TO_NB_AD<5>
EI_NB_TO_CPU_B_AD<6>	AP12	API1_ADI6	API1_AD06	AM20	EI_CPU_B_TO_NB_AD<6>
EI_NB_TO_CPU_B_AD<7>	AR12	API1_ADI7	API1_AD07	AM18	EI_CPU_B_TO_NB_AD<7>
EI_NB_TO_CPU_B_AD<8>	AT12	API1_ADI8	API1_AD08	AL18	EI_CPU_B_TO_NB_AD<8>
EI_NB_TO_CPU_B_AD<9>	AH12	API1_ADI9	API1_AD09	AN18	EI_CPU_B_TO_NB_AD<9>
EI_NB_TO_CPU_B_AD<10>	AG12	API1_ADI10	API1_AD010	AP18	EI_CPU_B_TO_NB_AD<10>
EI_NB_TO_CPU_B_AD<11>	AH13	API1_ADI11	API1_AD011	AR18	EI_CPU_B_TO_NB_AD<11>
EI_NB_TO_CPU_B_AD<12>	AJ12	API1_ADI12	API1_AD012	AT18	EI_CPU_B_TO_NB_AD<12>
EI_NB_TO_CPU_B_AD<13>	AG14	API1_ADI13	API1_AD013	AK18	EI_CPU_B_TO_NB_AD<13>
EI_NB_TO_CPU_B_AD<14>	AM10	API1_ADI14	API1_AD014	AP17	EI_CPU_B_TO_NB_AD<14>
EI_NB_TO_CPU_B_AD<15>	AL10	API1_ADI15	API1_AD015	AL17	EI_CPU_B_TO_NB_AD<15>
EI_NB_TO_CPU_B_AD<16>	AN10	API1_ADI16	API1_AD016	AH20	EI_CPU_B_TO_NB_AD<16>
EI_NB_TO_CPU_B_AD<17>	AP10	API1_ADI17	API1_AD017	AJ20	EI_CPU_B_TO_NB_AD<17>
EI_NB_TO_CPU_B_AD<18>	AR10	API1_ADI18	API1_AD018	AK20	EI_CPU_B_TO_NB_AD<18>
EI_NB_TO_CPU_B_AD<19>	AT10	API1_ADI19	API1_AD019	AH19	EI_CPU_B_TO_NB_AD<19>
EI_NB_TO_CPU_B_AD<20>	AK10	API1_ADI20	API1_AD020	AG20	EI_CPU_B_TO_NB_AD<20>
EI_NB_TO_CPU_B_AD<21>	AJ10	API1_ADI21	API1_AD021	AL20	EI_CPU_B_TO_NB_AD<21>
EI_NB_TO_CPU_B_AD<22>	AM08	API1_ADI22	API1_AD022	AM16	EI_CPU_B_TO_NB_AD<22>
EI_NB_TO_CPU_B_AD<23>	AN08	API1_ADI23	API1_AD023	AN16	EI_CPU_B_TO_NB_AD<23>
EI_NB_TO_CPU_B_AD<24>	AL08	API1_ADI24	API1_AD024	AL16	EI_CPU_B_TO_NB_AD<24>
EI_NB_TO_CPU_B_AD<25>	AP07	API1_ADI25	API1_AD025	AK16	EI_CPU_B_TO_NB_AD<25>
EI_NB_TO_CPU_B_AD<26>	AT06	API1_ADI26	API1_AD026	AP15	EI_CPU_B_TO_NB_AD<26>
EI_NB_TO_CPU_B_AD<27>	AR06	API1_ADI27	API1_AD027	AL15	EI_CPU_B_TO_NB_AD<27>
EI_NB_TO_CPU_B_AD<28>	AP08	API1_ADI28	API1_AD028	AP16	EI_CPU_B_TO_NB_AD<28>
EI_NB_TO_CPU_B_AD<29>	AT04	API1_ADI29	API1_AD029	AM14	EI_CPU_B_TO_NB_AD<29>
EI_NB_TO_CPU_B_AD<30>	AR04	API1_ADI30	API1_AD030	AL14	EI_CPU_B_TO_NB_AD<30>
EI_NB_TO_CPU_B_AD<31>	AP05	API1_ADI31	API1_AD031	AN14	EI_CPU_B_TO_NB_AD<31>
EI_NB_TO_CPU_B_AD<32>	AM06	API1_ADI32	API1_AD032	AP14	EI_CPU_B_TO_NB_AD<32>
EI_NB_TO_CPU_B_AD<33>	AN06	API1_ADI33	API1_AD033	AR14	EI_CPU_B_TO_NB_AD<33>
EI_NB_TO_CPU_B_AD<34>	AP06	API1_ADI34	API1_AD034	AT14	EI_CPU_B_TO_NB_AD<34>
EI_NB_TO_CPU_B_AD<35>	AP04	API1_ADI35	API1_AD035	AK14	EI_CPU_B_TO_NB_AD<35>
EI_NB_TO_CPU_B_AD<36>	AM03	API1_ADI36	API1_AD036	AP13	EI_CPU_B_TO_NB_AD<36>
EI_NB_TO_CPU_B_AD<37>	AN01	API1_ADI37	API1_AD037	AL13	EI_CPU_B_TO_NB_AD<37>
EI_NB_TO_CPU_B_AD<38>	AL06	API1_ADI38	API1_AD038	AG16	EI_CPU_B_TO_NB_AD<38>
EI_NB_TO_CPU_B_AD<39>	AL05	API1_ADI39	API1_AD039	AH15	EI_CPU_B_TO_NB_AD<39>
EI_NB_TO_CPU_B_AD<40>	AL04	API1_ADI40	API1_AD040	AJ14	EI_CPU_B_TO_NB_AD<40>
EI_NB_TO_CPU_B_AD<41>	AL03	API1_ADI41	API1_AD041	AH14	EI_CPU_B_TO_NB_AD<41>
EI_NB_TO_CPU_B_AD<42>	AN02	API1_ADI42	API1_AD042	AH16	EI_CPU_B_TO_NB_AD<42>
EI_NB_TO_CPU_B_AD<43>	AN03	API1_ADI43	API1_AD043	AH17	EI_CPU_B_TO_NB_AD<43>
EI_NB_TO_CPU_B_SR_P<0>	AP09	API1_SRIP0	API1_SROP0	AG18	EI_CPU_B_TO_NB_SR_P<0>
EI_NB_TO_CPU_B_SR_N<0>	AL09	API1_SRIN0	API1_SRON0	AJ16	EI_CPU_B_TO_NB_SR_N<0>
EI_NB_TO_CPU_B_SR_P<1>	AR02	API1_SRIP1	API1_SROP1	AJ18	EI_CPU_B_TO_NB_SR_P<1>
EI_NB_TO_CPU_B_SR_N<1>	AP02	API1_SRIN1	API1_SRON1	AH18	EI_CPU_B_TO_NB_SR_N<1>
CPU_B0_QACK_L	AF12	API_QACK2	API_QREQ2	AF16	CPU_B0_TO_NB_QREQ_L
CPU_B1_QACK_L	AC12	API_QACK3	API_QREQ3	AF20	CPU_B1_TO_NB_QREQ_L
NB_CPU_B0_INT_L	N12	IRQ2			
NB_CPU_B1_INT_L	U12	IRQ3			
TP_NB_APSYNC	AH11	API1_APSYNC			
NB_B_TRIGGER_OUT	AK08	API1_SE			

KODIAK DEFINES ADO
AS AN INPUT AND ADI
AS AN OUTPUT. NETS
NAMED APPROPRIATELY.

WE MAY NEED A DIFFERENT
ELECTRICAL_CONSTRAINT_SET
FOR CPU_A AND CPU_B.

EI_BUS SYS_CLK CONSTRAINTS MOVED TO PAGE 56 TO SUPPORT M23/M33

WIRE TP_NB_APSYNC TO A TEST POINT

P4MM SM
PP4410
PP4411
PP4413
PP4400
PP4401
PP4402
PP4403
PP4404
PP4405
PP4406
PP4407
PP4408

NET_SPACING_TYPE

NB_CPU_B0_INT_L	P3MM_SPACING	44 56
NB_CPU_B1_INT_L	P3MM_SPACING	44 56

PULL DOWN QREQS TO NB

CPU_B0_TO_NB_QREQ_L
CPU_B1_TO_NB_QREQ_L
R4407 10K 5% 1/16W MF-LF 402
R4406 10K 5% 1/16W MF-LF 402

LAST_MODIFIED=Wed Nov 16 09:41:04 2005

SYNC_MASTER=Q63	SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

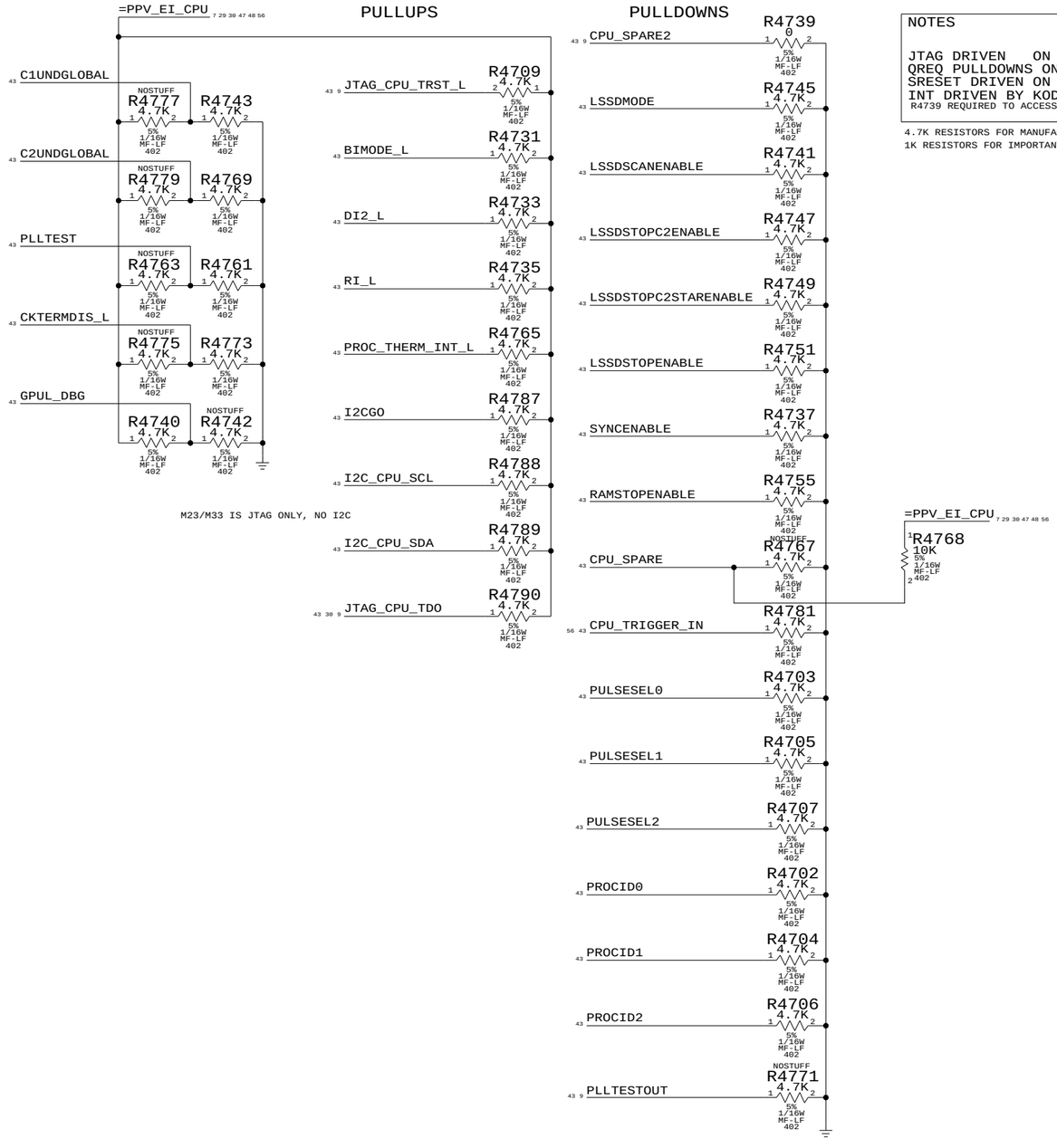
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 44 OF 154	

KODIAK EI B



NOTES

JTAG DRIVEN ON SMU PG 30
QREQ PULLDOWNS ON Q63 SHARED PAGE
SRESET DRIVEN ON PG 56
INT DRIVEN BY KODIAK
R4739 REQUIRED TO ACCESS THE RINGS

4.7K RESISTORS FOR MANUFACTURING-TEST-TYPE PULLUPS OR PULLDOWNS.
1K RESISTORS FOR IMPORTANT USE OR STRAPPING OPTIONS.

SELECT PROCESSOR CLOCK MULTIPLIER. PROCESSOR CLOCK(MHZ)= SYSTCLOCK * PLLMULT.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4734	EI_3TO1	SYSCLK * 12
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4718	EI_2TO1	SYSCLK * 8

SELECT EI BUS DIVIDER. BUS DATA RATE(BPS)= (PROCESSOR CLOCK) / BUSCFG.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4728	EI_2TO1	PROC / 2
*	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4726,R4712	EI_3TO1	PROC / 3
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4728	NOSTUFF	PROC / 4
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4724,R4710,R4712	NOSTUFF	PROC / 6
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4728	NOSTUFF	PROC / 8
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4726,R4712	NOSTUFF	PROC / 12
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4728	NOSTUFF	PROC / 16
	116S0066	3	RES,1K OHM,1/16W,5%,0402	R4708,R4710,R4712	NOSTUFF	

SELECT ELASTIC MODE OR BYPASS.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
*	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4736		
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4720	NOSTUFF	BYPASS MODE

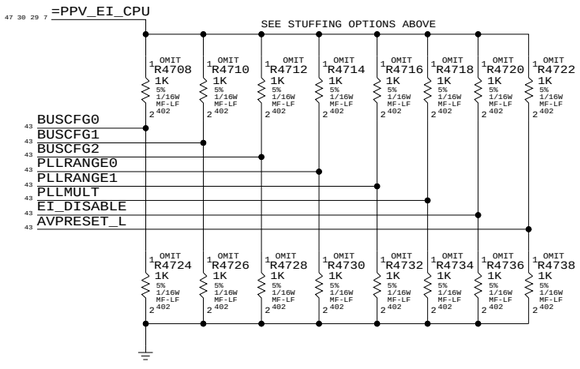
SELECT PLL FREQUENCY RANGE.

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
>= 1.8 GHZ *	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4732	CPU_PLL_LOW	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4730,R4716	CPU_PLL_HIGH	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4732	CPU_PLL_MEDIUM	
	116S0066	2	RES,1K OHM,1/16W,5%,0402	R4714,R4716	NOSTUFF	RESERVED

	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4722		AVPRESET OFF
	116S0066	1	RES,1K OHM,1/16W,5%,0402	R4738	NOSTUFF	AVPRESET ON

* STUFF THESE ON M23.

PROCESSOR BUS CONFIGURATION



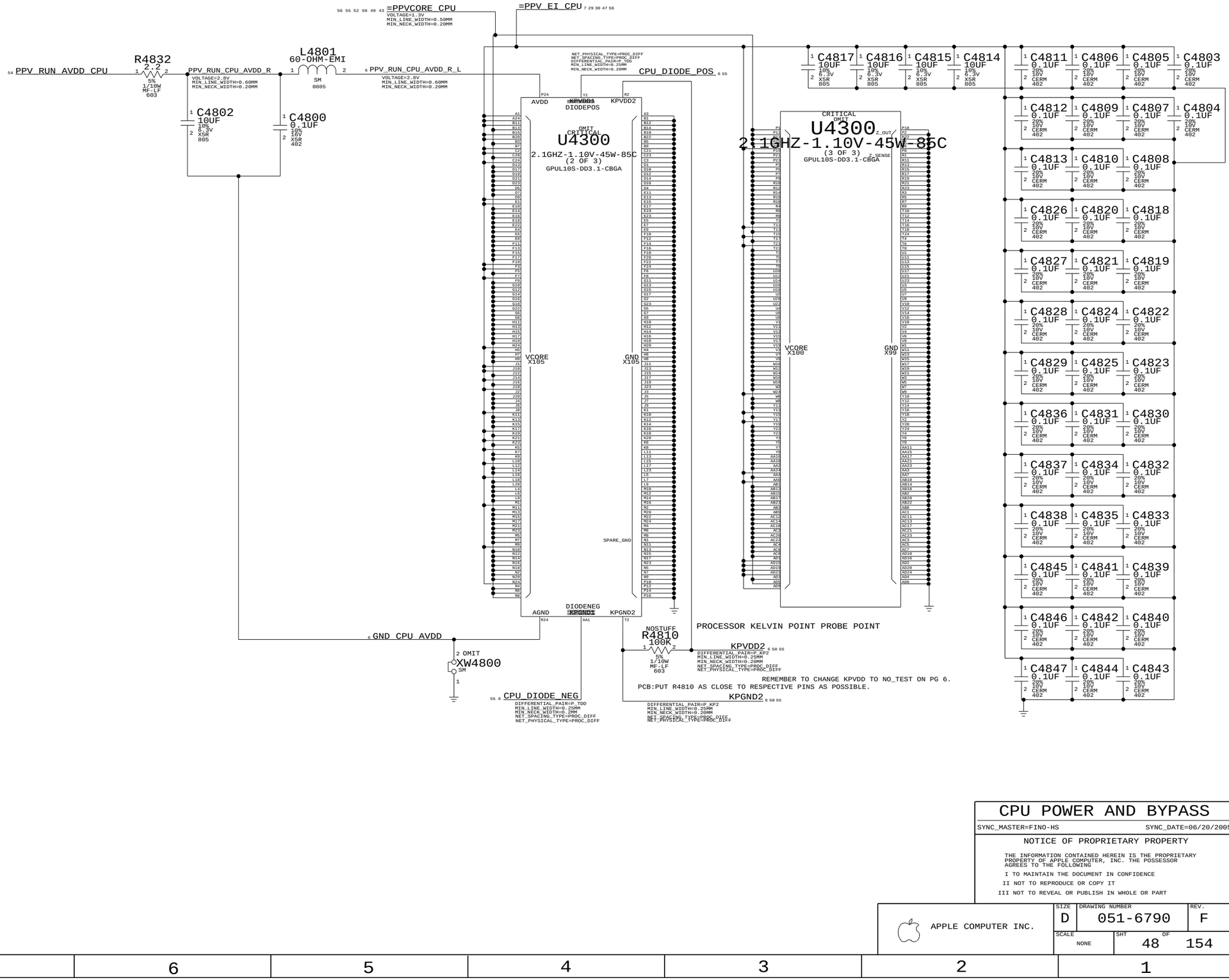
CPU STRAPS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	47	154



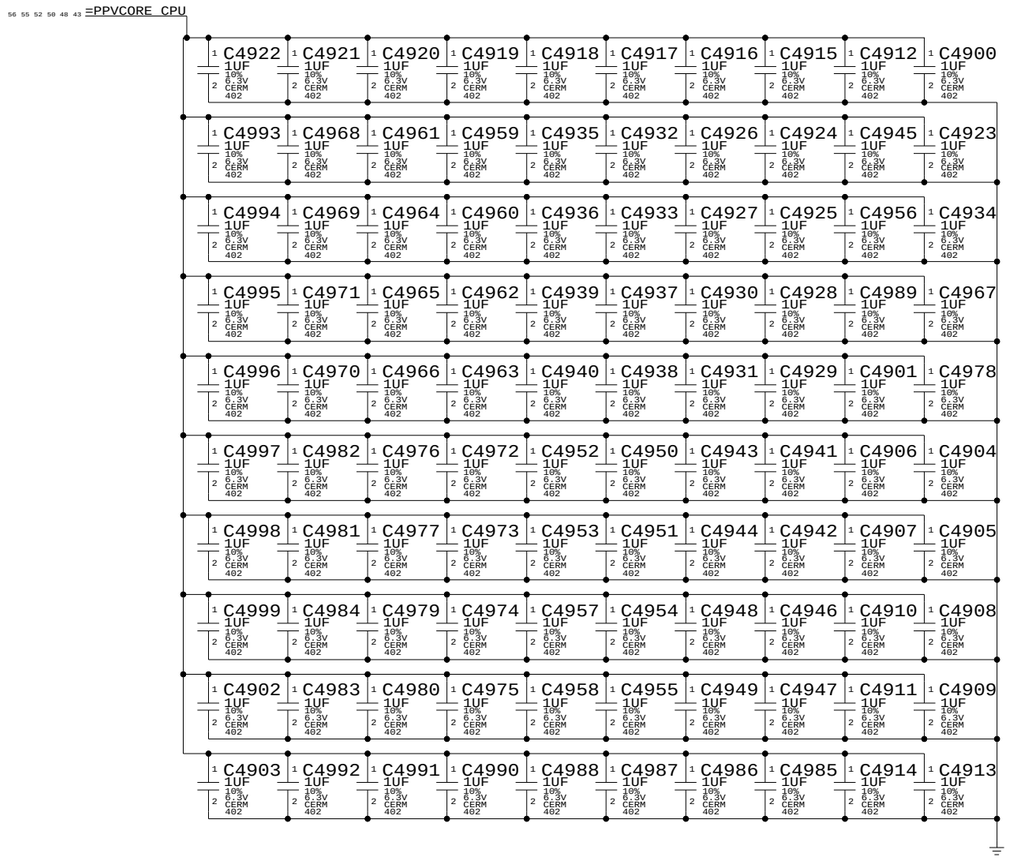
CPU POWER AND BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	48	154

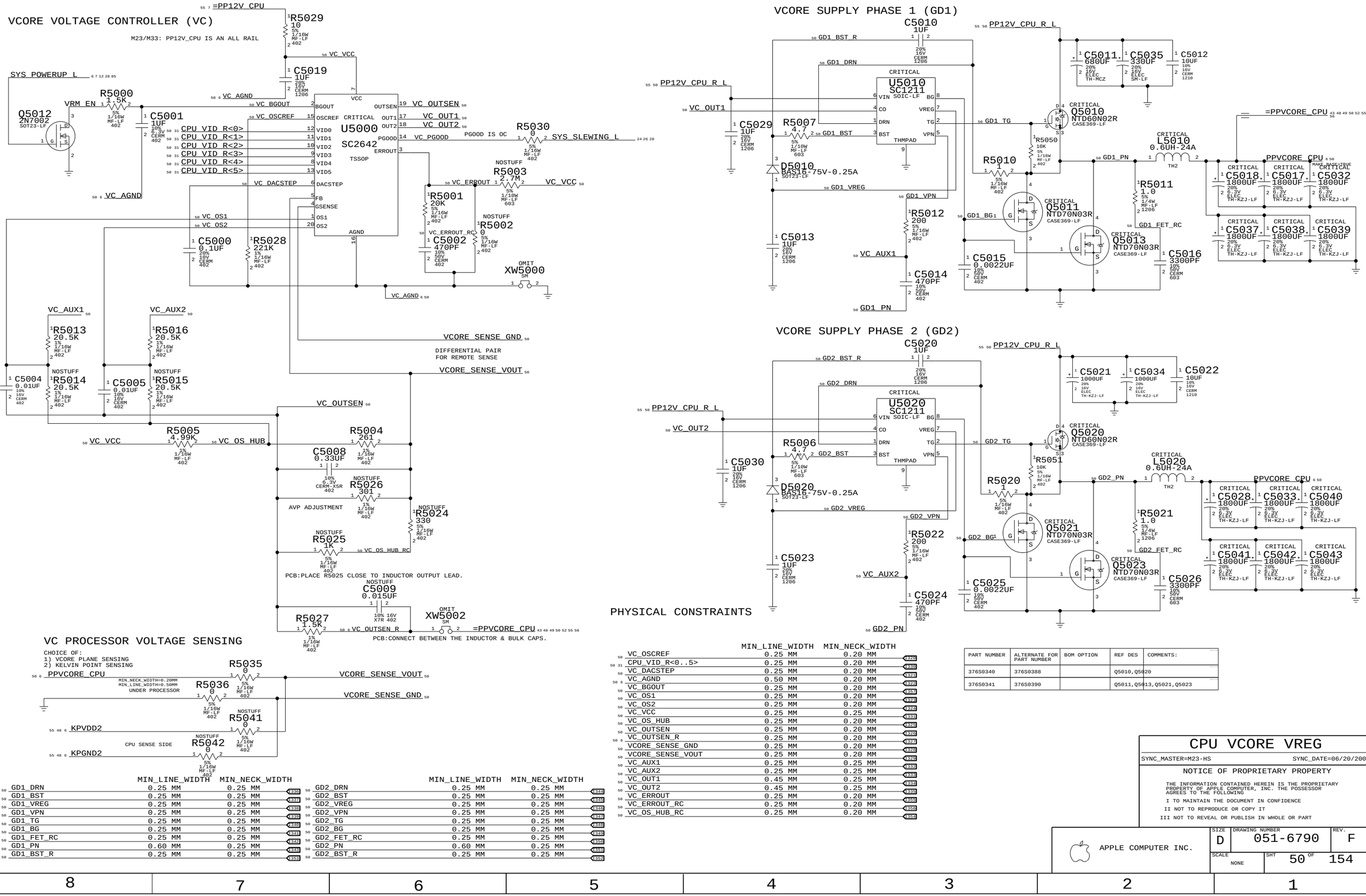


PROC DECOUPLING

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 49 OF 154	



	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD1_DRN	0.25 MM	0.25 MM	R336
GD1_BST	0.25 MM	0.25 MM	R337
GD1_VREG	0.25 MM	0.25 MM	R338
GD1_VPN	0.25 MM	0.25 MM	R339
GD1_TG	0.25 MM	0.25 MM	R340
GD1_BG	0.25 MM	0.25 MM	R341
GD1_FET_RC	0.25 MM	0.25 MM	R342
GD1_PN	0.60 MM	0.25 MM	R343
GD1_BST_R	0.25 MM	0.25 MM	R358

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
GD2_DRN	0.25 MM	0.25 MM	R344
GD2_BST	0.25 MM	0.25 MM	R345
GD2_VREG	0.25 MM	0.25 MM	R346
GD2_VPN	0.25 MM	0.25 MM	R347
GD2_TG	0.25 MM	0.25 MM	R348
GD2_BG	0.25 MM	0.25 MM	R349
GD2_FET_RC	0.25 MM	0.25 MM	R350
GD2_PN	0.60 MM	0.25 MM	R351
GD2_BST_R	0.25 MM	0.25 MM	R352

	MIN_LINE_WIDTH	MIN_NECK_WIDTH	
VC_OSCREF	0.25 MM	0.20 MM	R320
CPU_VID_R<0..5>	0.25 MM	0.20 MM	R330
VC_DACSTEP	0.25 MM	0.20 MM	R321
VC_AGND	0.50 MM	0.20 MM	R322
VC_BGOUT	0.25 MM	0.20 MM	R367
VC_OS1	0.25 MM	0.20 MM	R323
VC_OS2	0.25 MM	0.20 MM	R324
VC_VCC	0.25 MM	0.25 MM	R331
VC_OS_HUB	0.25 MM	0.20 MM	R325
VC_OUTSEN	0.25 MM	0.20 MM	R326
VC_OUTSEN_R	0.25 MM	0.20 MM	R327
VCORE_SENSE_GND	0.25 MM	0.20 MM	R328
VCORE_SENSE_VOUT	0.25 MM	0.20 MM	R329
VC_AUX1	0.25 MM	0.25 MM	R332
VC_AUX2	0.25 MM	0.25 MM	R333
VC_OUT1	0.45 MM	0.25 MM	R334
VC_OUT2	0.45 MM	0.25 MM	R335
VC_ERROUT	0.25 MM	0.20 MM	R355
VC_ERROUT_RC	0.25 MM	0.20 MM	R356
VC_OS_HUB_RC	0.25 MM	0.20 MM	R354

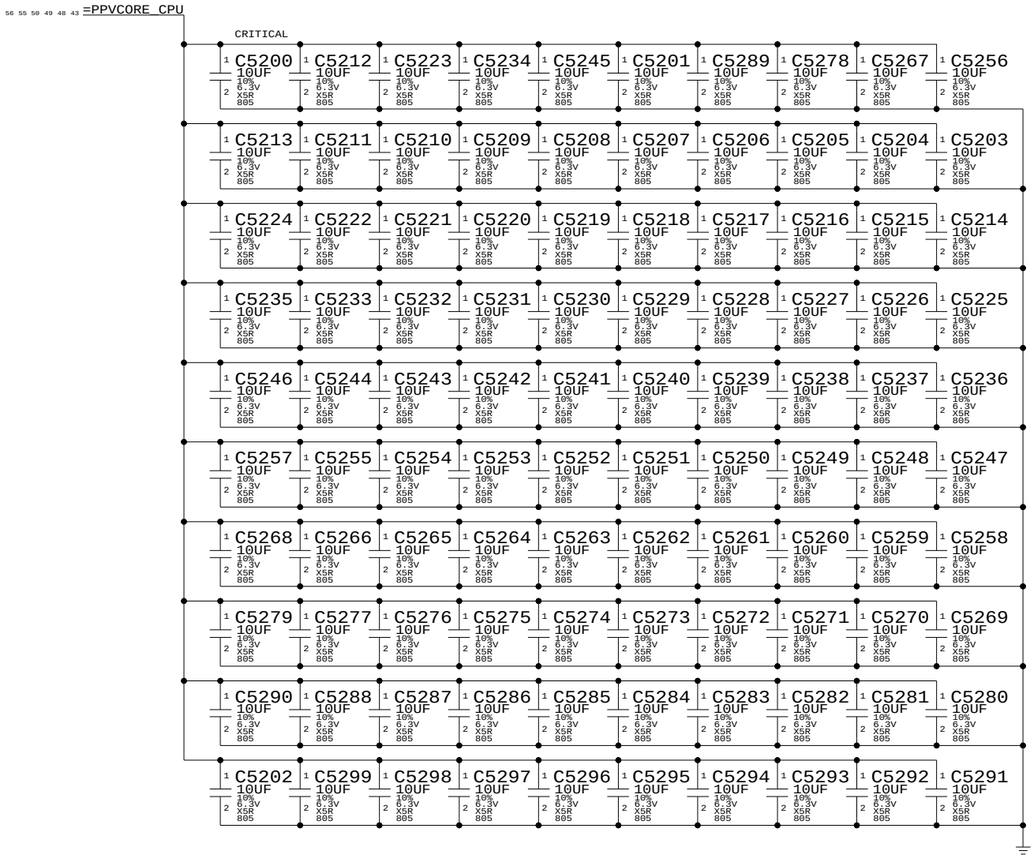
PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
376S0340	376S0388		Q5010,Q5020	
376S0341	376S0390		Q5011,Q5013,Q5021,Q5023	

CPU VCORE VREG

SYNC_MASTER=M23-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 50 OF 154	



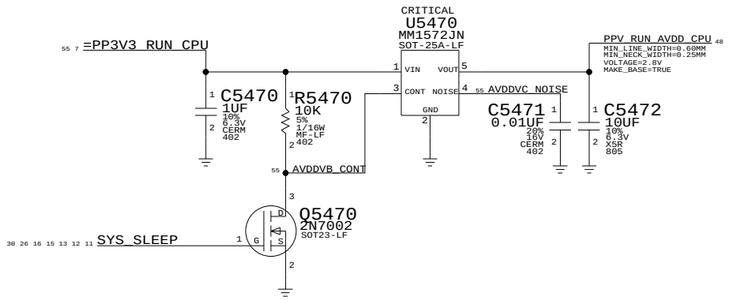
CPU VCORE MORE BYPASS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 52 OF 154	

PROCESSOR AVDD VREG



ZH5400 HOLE-VIA
ZH5401 HOLE-VIA
ZH5402 HOLE-VIA
ZH5403 HOLE-VIA
ZH5404 HOLE-VIA
ZH5405 HOLE-VIA
ZH5406 HOLE-VIA
ZH5407 HOLE-VIA
ZH5408 HOLE-VIA
ZH5409 HOLE-VIA
ZH5410 HOLE-VIA
ZH5411 HOLE-VIA
ZH5412 HOLE-VIA
ZH5413 HOLE-VIA
ZH5414 HOLE-VIA
ZH5415 HOLE-VIA
ZH5416 HOLE-VIA
ZH5417 HOLE-VIA
ZH5418 HOLE-VIA
ZH5419 HOLE-VIA
ZH5420 HOLE-VIA
ZH5421 HOLE-VIA
ZH5422 HOLE-VIA
ZH5423 HOLE-VIA
ZH5424 HOLE-VIA
ZH5425 HOLE-VIA
ZH5426 HOLE-VIA
ZH5427 HOLE-VIA
ZH5428 HOLE-VIA
ZH5429 HOLE-VIA
ZH5430 HOLE-VIA
ZH5431 HOLE-VIA
ZH5432 HOLE-VIA
ZH5433 HOLE-VIA
ZH5434 HOLE-VIA
ZH5435 HOLE-VIA
ZH5436 HOLE-VIA
ZH5437 HOLE-VIA
ZH5438 HOLE-VIA
ZH5439 HOLE-VIA
ZH5440 HOLE-VIA
ZH5441 HOLE-VIA
ZH5442 HOLE-VIA
ZH5443 HOLE-VIA
ZH5444 HOLE-VIA
ZH5445 HOLE-VIA
ZH5446 HOLE-VIA
ZH5447 HOLE-VIA
ZH5448 HOLE-VIA
ZH5449 HOLE-VIA
ZH5450 HOLE-VIA
ZH5451 HOLE-VIA
ZH5452 HOLE-VIA
ZH5453 HOLE-VIA
ZH5454 HOLE-VIA
ZH5455 HOLE-VIA
ZH5456 HOLE-VIA
ZH5457 HOLE-VIA
ZH5458 HOLE-VIA
ZH5459 HOLE-VIA
ZH5460 HOLE-VIA
ZH5461 HOLE-VIA
ZH5462 HOLE-VIA
ZH5463 HOLE-VIA
ZH5464 HOLE-VIA
ZH5465 HOLE-VIA
ZH5466 HOLE-VIA
ZH5467 HOLE-VIA
ZH5468 HOLE-VIA
ZH5469 HOLE-VIA
ZH5470 HOLE-VIA
ZH5471 HOLE-VIA

CPU AVDD VREG

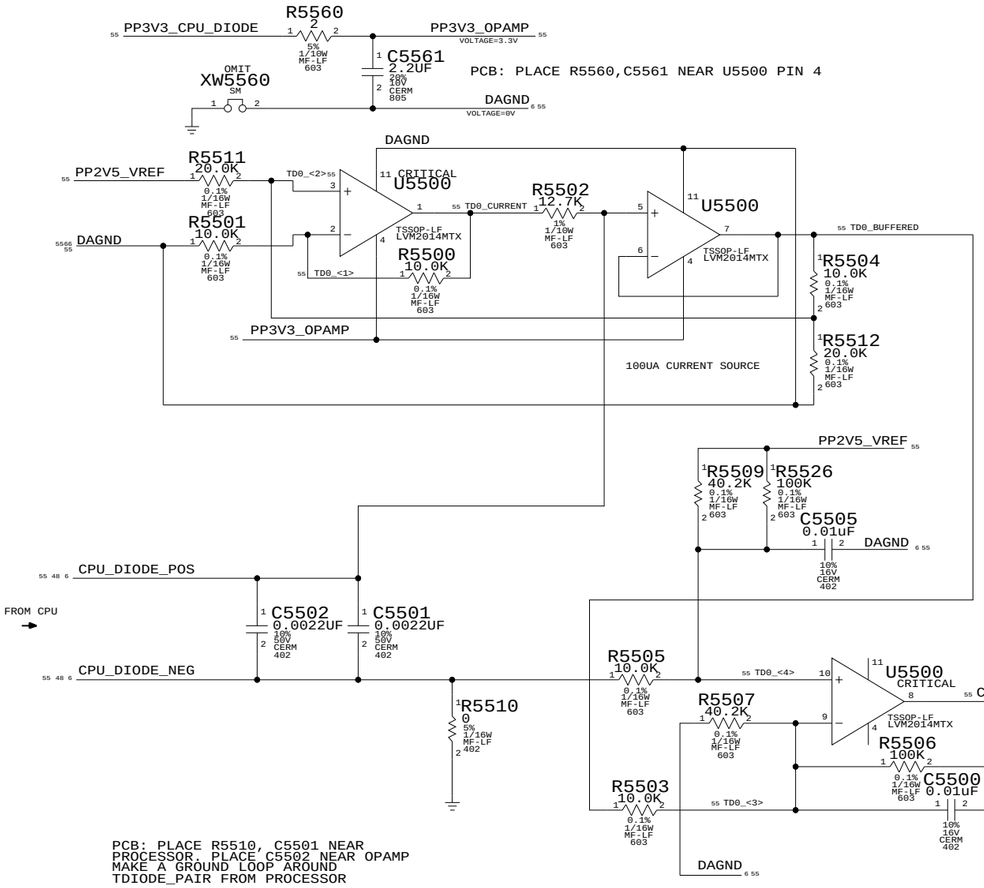
SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

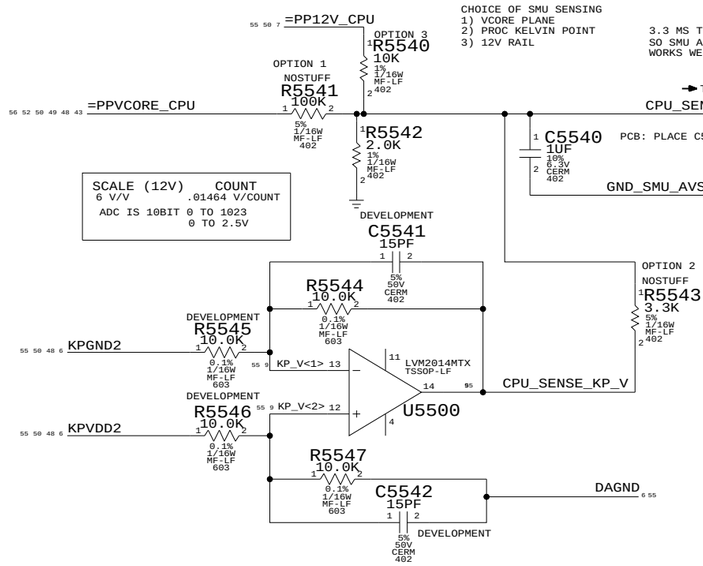
SIZE D | DRAWING NUMBER 051-6790 | REV. F

SCALE NONE | SHT 54 OF 154

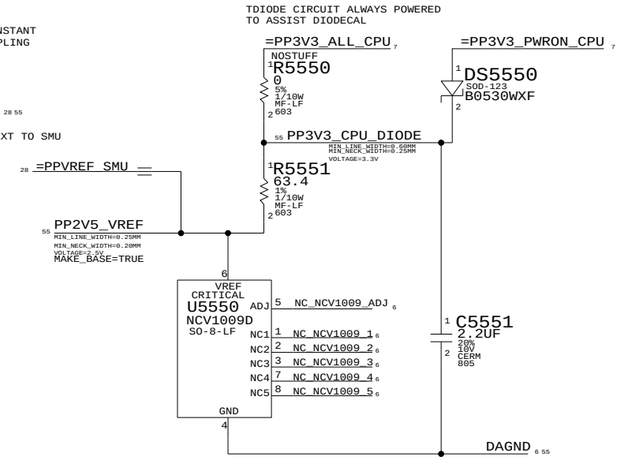
PROCESSOR TEMP SENSE (TDIODE EXCITATION CIRCUIT AND OPAMP)



PROCESSOR VCORE VOLTAGE SENSE



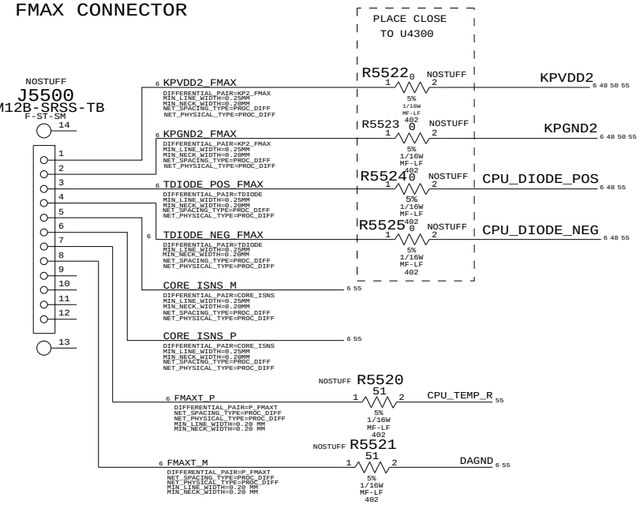
2.5V PRECISION VOLTAGE REFERENCE SOURCE



PHYSICAL CONSTRAINTS

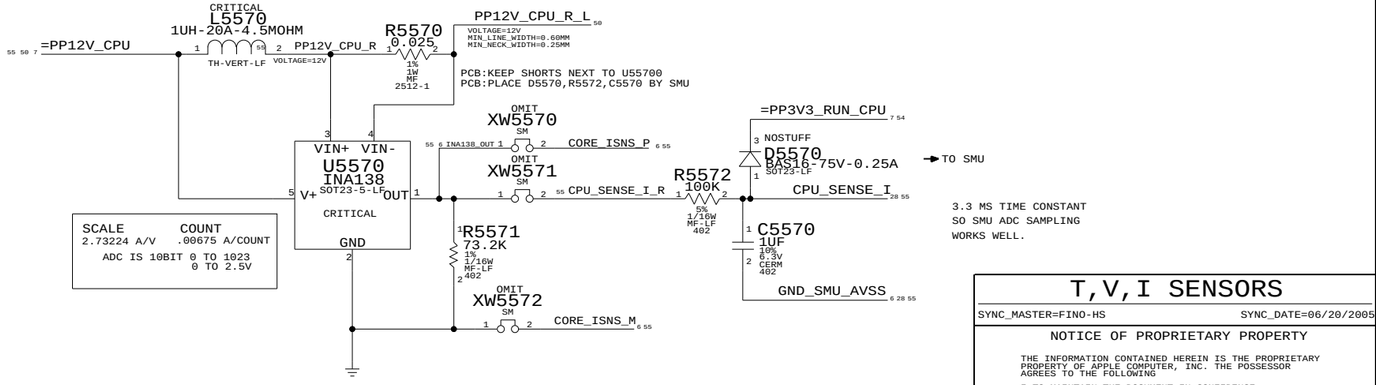
	MIN_LINE_WIDTH	MIN_NECK_WIDTH
TD0_<1..4>	0.25 MM	0.25 MM
PP12V_CPU_R	0.60 MM	0.25 MM
TD0_CURRENT	0.25 MM	0.25 MM
TD0_BUFFERED	0.25 MM	0.25 MM
KP_V<1..2>	0.25 MM	0.25 MM
CPU_SENSE_KP_V	0.25 MM	0.25 MM
PP3V3_OPAMP	0.60 MM	0.20 MM
INA138_OUT	0.25 MM	0.25 MM
CPU_SENSE_I_R	0.25 MM	0.25 MM
CPU_SENSE_I	0.25 MM	0.25 MM
CPU_SENSE_V	0.25 MM	0.25 MM
CPU_TEMP	0.25 MM	0.20 MM
CPU_TEMP_R	0.25 MM	0.20 MM
AVDDVC_NOISE	0.25 MM	0.20 MM
AVDDVB_CONT	0.25 MM	0.20 MM
PP12V_CPU_R	0.60 MM	0.25 MM
DAGND	0.60 MM	0.25 MM

FMAX CONNECTOR



PROCESSOR VCORE CURRENT SENSE

(USING 12V INPUT CURRENT TO DERIVE CPU CURRENT)



T,V,I SENSORS

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 55 OF 154	

CONNECT PULSAR CLKS TO CPU/NB

56 43 9	EI_CPU_SYSCLK_P		EI_CPU_A_SYSCLK_P 26
56 43	EI_CPU_SYSCLK_N	MAKE_BASE=TRUE	EI_CPU_A_SYSCLK_N 26
56 43	EI_CPU_APSYNC	MAKE_BASE=TRUE	CPU_A_APSYNC 26
43	EI_CPU_TBEN_CLK	MAKE_BASE=TRUE	CPU_A_TBEN_CLK_US 26
56	EI_NB_APSYNC	MAKE_BASE=TRUE	NB_APSYNC 26 42
		MAKE_BASE=TRUE	

CONNECT KODIAK EI A TO/FROM CPU

56 43 9	EI_NB_TO_CPU_CLK_P		EI_NB_TO_CPU_A_CLK_P 42
56 43 9	EI_NB_TO_CPU_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_CLK_N 42
56 43	EI_NB_TO_CPU_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_AD<0..43> 42
56 43 9	EI_NB_TO_CPU_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_P<0..1> 42
56 43 9	EI_NB_TO_CPU_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_A_SR_N<0..1> 42
		MAKE_BASE=TRUE	
56 43 9	EI_CPU_TO_NB_CLK_P		EI_CPU_A_TO_NB_CLK_P 42
56 43 9	EI_CPU_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_CLK_N 42
56 43	EI_CPU_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_AD<0..43> 42
56 43 9	EI_CPU_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_P<0..1> 42
56 43 9	EI_CPU_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_A_TO_NB_SR_N<0..1> 42
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK QREQ A0

43	CPU_TO_NB_QREQ_L		CPU_A0_TO_NB_QREQ_L 42
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK QACK A0, NC OTHERWISE

43	CPU_QACK_L		CPU_A0_QACK_L 42
6	NC_CPU_A1_QACK_L	MAKE_BASE=TRUE	CPU_A1_QACK_L 42
6	NC_CPU_B0_QACK_L	MAKE_BASE=TRUE	CPU_B0_QACK_L 44
6	NC_CPU_B1_QACK_L	MAKE_BASE=TRUE	CPU_B1_QACK_L 44
		MAKE_BASE=TRUE	

CONNECT CPU TO KODIAK/SHASTA INT A0, NC OTHERWISE

43	CPU_INT_L		CPU_A0_INT_R_L 24 56
6	NC_NB_CPU_A1_INT_L	MAKE_BASE=TRUE	NB_CPU_A1_INT_L 42
6	NC_NB_CPU_B0_INT_L	MAKE_BASE=TRUE	NB_CPU_B0_INT_L 44
6	NC_NB_CPU_B1_INT_L	MAKE_BASE=TRUE	NB_CPU_B1_INT_L 44
		MAKE_BASE=TRUE	

CONNECT CPU TO SHASTA SRESET A0, NC OTHERWISE

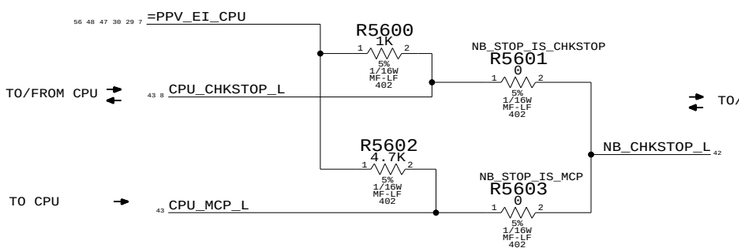
	CPU_SRESET_L_R		SB_CPU_A0_SRESET_L 24 56
	NOTUSED_CPU_A1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_A1_SRESET_L 24 56
	NOTUSED_CPU_B0_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B0_SRESET_L 24 56
	NOTUSED_CPU_B1_SRESET_L	MAKE_BASE=TRUE	SB_CPU_B1_SRESET_L 24 56
		MAKE_BASE=TRUE	

WIRE OUT KODIAK AND CPU SIGNALS FOR TP'S

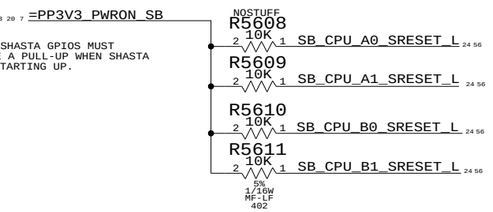
9	TP_NB_B_TRIGGER_OUT		NB_B_TRIGGER_OUT 44
9	TP_NB_A_TRIGGER_OUT	MAKE_BASE=TRUE	NB_A_TRIGGER_OUT 42
	TP_CPU_APSYNCOUT	MAKE_BASE=TRUE	CPU_APSYNCOUT 43
	TP_CPU_TRIGGER_IN	MAKE_BASE=TRUE	CPU_TRIGGER_IN 43 47
	TP_CPU_TRIGGER_OUT	MAKE_BASE=TRUE	CPU_TRIGGER_OUT 43
9	NC_PSRO	MAKE_BASE=TRUE	CPU_PSRO 43
9	NC_PSRO_ENABLE	MAKE_BASE=TRUE	CPU_PSRO_ENABLE 43
9	TP_CPU_ATTENTION	MAKE_BASE=TRUE	CPU_ATTENTION 43
9	NC_CPU_AFN	MAKE_BASE=TRUE	CPU_AFN 43
		MAKE_BASE=TRUE	

REMEMBER TO UPDATE NO_TEST PROPERTIES ON PG 6

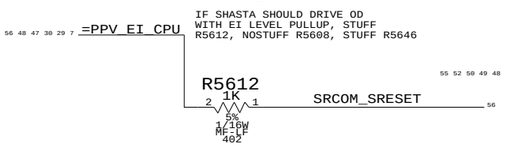
CPU CHKSTOP OR MCP TO NB

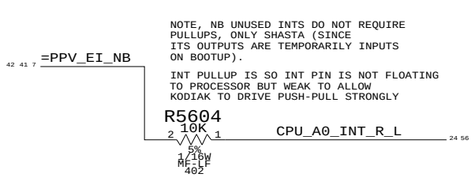


TO/FROM NB



ALL SHASTA GPIOS MUST HAVE A PULL-UP WHEN SHASTA IS STARTING UP.





EI BUS AND SYSCLK CONSTRAINT LABELS

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
56 43 9 EI_CPU_TO_NB_CLK_P	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	128
56 43 9 EI_CPU_TO_NB_CLK_N	EICNCLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	EI_CPU_TO_NB_CLK	127
56 43 EI_CPU_TO_NB_AD<0..21>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		131
56 43 9 EI_CPU_TO_NB_SR_P<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		134
56 43 9 EI_CPU_TO_NB_SR_N<0..1>	EICNCSR	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		132
56 43 9 EI_NB_TO_CPU_CLK_P	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	129
56 43 9 EI_NB_TO_CPU_CLK_N	EINCCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	130
56 43 EI_NB_TO_CPU_AD<0..43>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		135
56 43 9 EI_NB_TO_CPU_SR_P<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		140
56 43 9 EI_NB_TO_CPU_SR_N<0..1>	EINCCAD	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		137
56 EI_NB_APSYNC	EIPNAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		
56 43 EI_CPU_APSYNC	EIPCAPSYNC	EI_NB_TO_CPU_AD	EI_NB_TO_CPU_AD		138
56 43 9 EI_CPU_SYSCLK_P	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	139
56 43 EI_CPU_SYSCLK_N	EIPCSYSCLK	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_CPU_SYSCLK	141
42 26 EI_NB_SYSCLK_P	EIPNSYSCLK_P	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	136
42 26 EI_NB_SYSCLK_N	EIPNSYSCLK_N	EI_NB_TO_CPU_CLK	EI_NB_TO_CPU_CLK	EI_NB_SYSCLK	142
56 43 EI_CPU_TO_NB_AD<22>	EICNCAD_PP	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496
56 43 EI_CPU_TO_NB_AD<23..43>	EICNCAD	EI_CPU_TO_NB_AD	EI_CPU_TO_NB_AD		1496

NC KODIAK EI B OUTPUT PORT

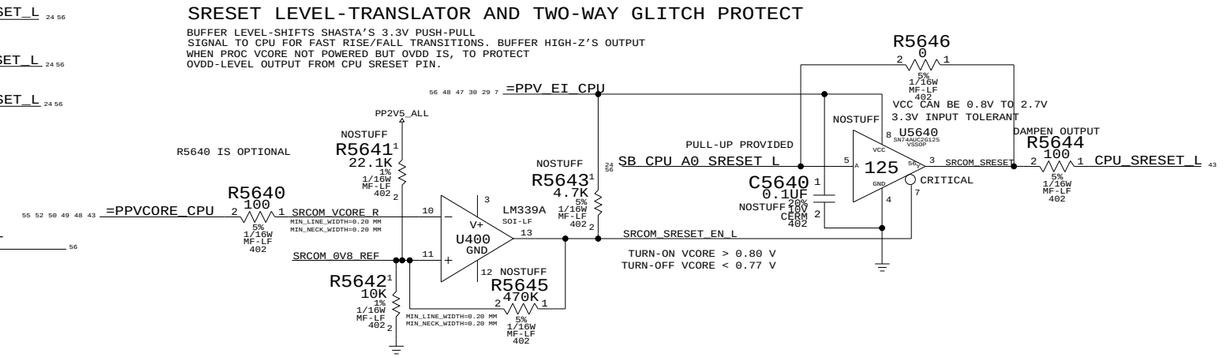
6	NC_EI_NB_TO_CPU_B_CLK_P		EI_NB_TO_CPU_B_CLK_P 44
6	NC_EI_NB_TO_CPU_B_CLK_N	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_CLK_N 44
6	NC_EI_NB_TO_CPU_B_AD<0..43>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_AD<0..43> 44
6	NC_EI_NB_TO_CPU_B_SR_P<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_P<0..1> 44
6	NC_EI_NB_TO_CPU_B_SR_N<0..1>	MAKE_BASE=TRUE	EI_NB_TO_CPU_B_SR_N<0..1> 44
		MAKE_BASE=TRUE	

NC KODIAK EI B INPUT PORT

6	NC_EI_CPU_B_TO_NB_CLK_P		EI_CPU_B_TO_NB_CLK_P 44
6	NC_EI_CPU_B_TO_NB_CLK_N	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_CLK_N 44
6	NC_EI_CPU_B_TO_NB_AD<0..43>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_AD<0..43> 44
6	NC_EI_CPU_B_TO_NB_SR_P<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_P<0..1> 44
6	NC_EI_CPU_B_TO_NB_SR_N<0..1>	MAKE_BASE=TRUE	EI_CPU_B_TO_NB_SR_N<0..1> 44
		MAKE_BASE=TRUE	

SRESET LEVEL-TRANSLATOR AND TWO-WAY GLITCH PROTECT

BUFFER LEVEL-SHIFTS SHASTA'S 3.3V PUSH-PULL SIGNAL TO CPU FOR FAST RISE/FALL TRANSITIONS. BUFFER HIGH-Z'S OUTPUT WHEN PROC VCORE NOT POWERED BUT OVDD IS, TO PROTECT OVDD-LEVEL OUTPUT FROM CPU SRESET PIN.

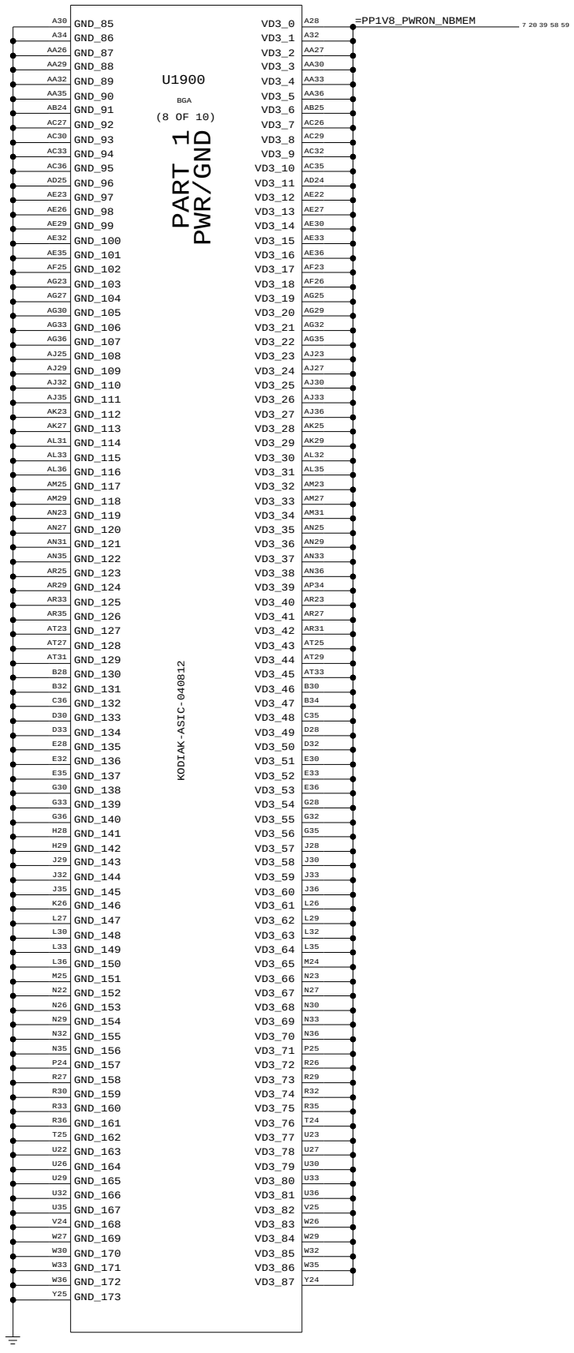


CPU ALIASES & MISC

SYNC_MASTER=FINO-HS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 56 OF 154	



59 58 39 20 7 =PP1V8_PWRON_NBMEM

C5836 C5835 C5834 C5832 C5831 C5830 C5829 C5822 C5811 C5800
C5864 C5859 C5857 C5842 C5840 C5837 C5828 C5801 C5855 C5833
C5863 C5860 C5858 C5843 C5841 C5838 C5827 C5802 C5866 C5844
C5865 C5862 C5861 C5846 C5845 C5839 C5826 C5803 C5887 C5877
C5874 C5869 C5867 C5852 C5850 C5847 C5825 C5810 C5806 C5804
C5873 C5870 C5868 C5853 C5851 C5848 C5824 C5812 C5807 C5805
C5875 C5872 C5871 C5856 C5854 C5849 C5823 C5813 C5809 C5808
C5886 C5885 C5883 C5881 C5879 C5876 C5821 C5818 C5816 C5814
C5884 C5882 C5880 C5878 C5820 C5819 C5817 C5815

1UF 10% 6.3V CERM 402

Q63: SEE P.20 FOR MORE DECOUPLING CAPS FOR THESE PINS.

KODIAC NBMEM PWR & CAPS

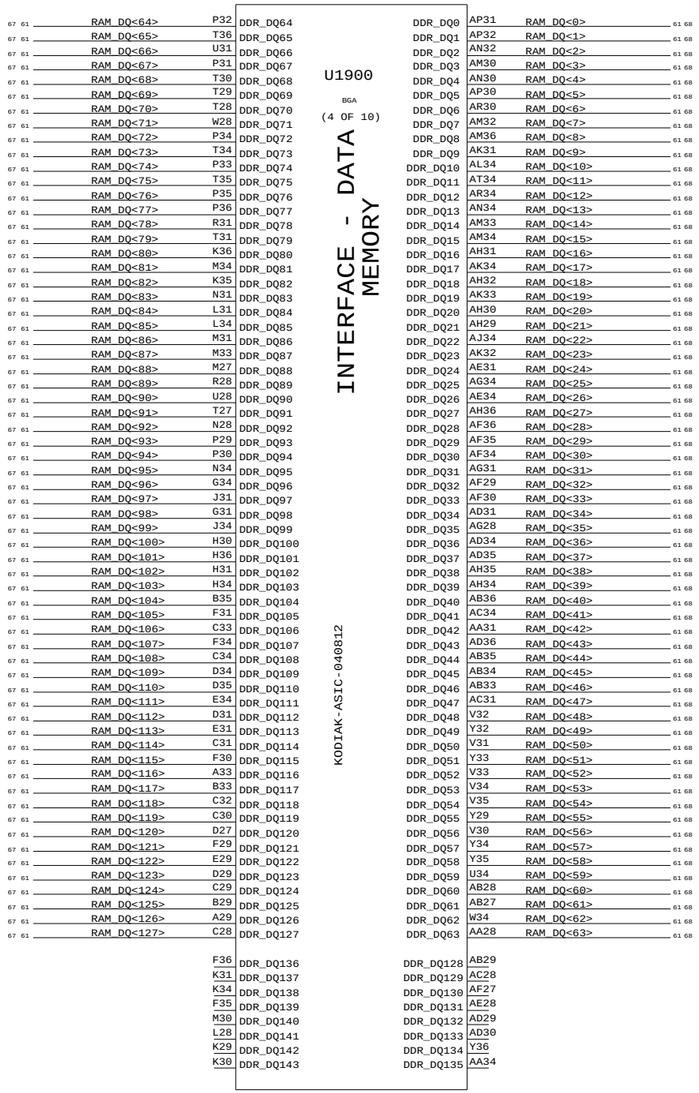
SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

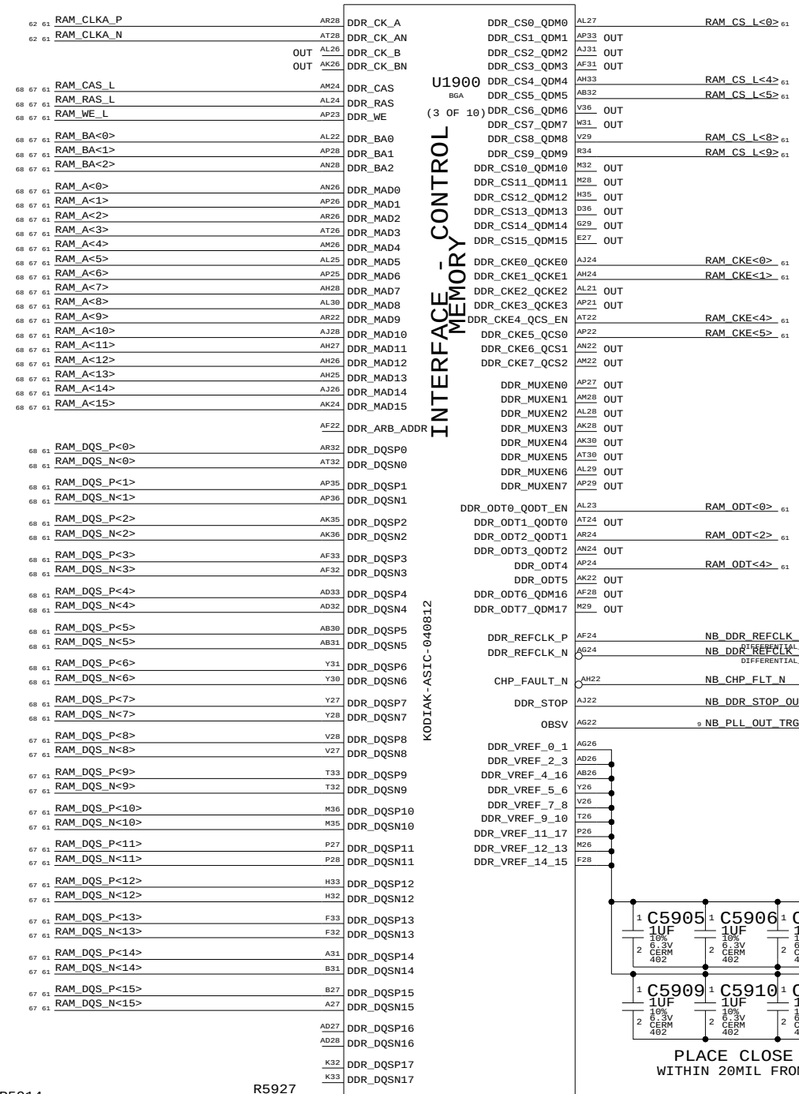
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 58 OF 154	

LAST_MODIFIED=Wed Nov 16 09:41:14 2005

DRAWING



DQ/DQS OKAY TO TIE TO GROUND FOR THERMALS

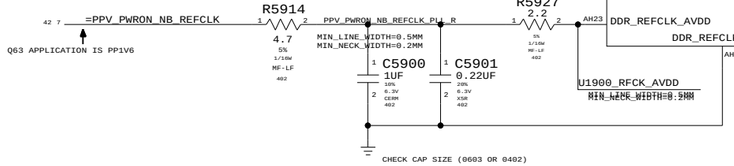


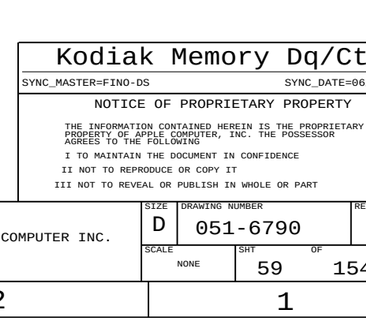
Kodiak 128bit CS/CKE/ODT mapping (Q63 style)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	2	0	4	J6700 rank 1	64:127
B3	3	1	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	10	4	5	*unused*	64:127
D7	11	5	-	*unused*	64:127
E8	4	2	2	*unused*	0:63
E9	5	3	-	*unused*	0:63
F10	12	4	6	*unused*	64:127
F11	13	5	-	*unused*	64:127
G12	6	6	3	*unused*	0:63
G13	7	7	-	*unused*	0:63
H14	14	6	7	*unused*	64:127
H15	15	7	-	*unused*	64:127

Kodiak 128bit CS/CKE/ODT mapping (v1.1 only)

DIMM RANK	CS*	CKE	ODT	M23 Function	D bits
A0	0	0	0	onboard DRAM	0:63
A1	1	1	-	*unused*	0:63
B2	4	4	2	J6700 rank 1	64:127
B3	5	5	-	J6700 rank 2	64:127
C4	2	2	1	*unused*	0:63
C5	3	3	-	*unused*	0:63
D6	6	6	3	*unused*	64:127
D7	7	7	-	*unused*	64:127





KODIAK MEMORY INTERFACE

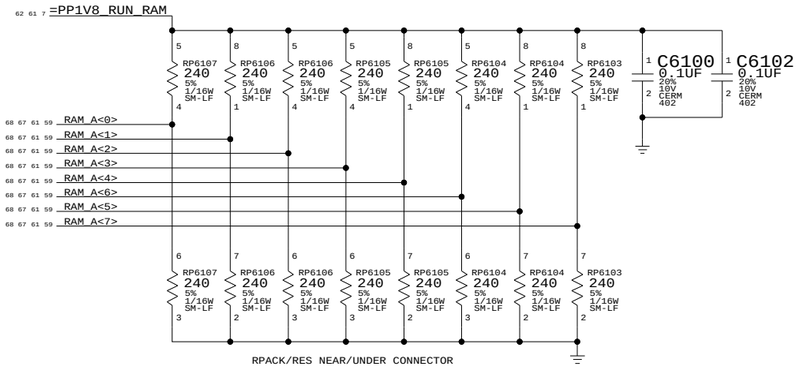
Kodiak Memory Dq/Ctl

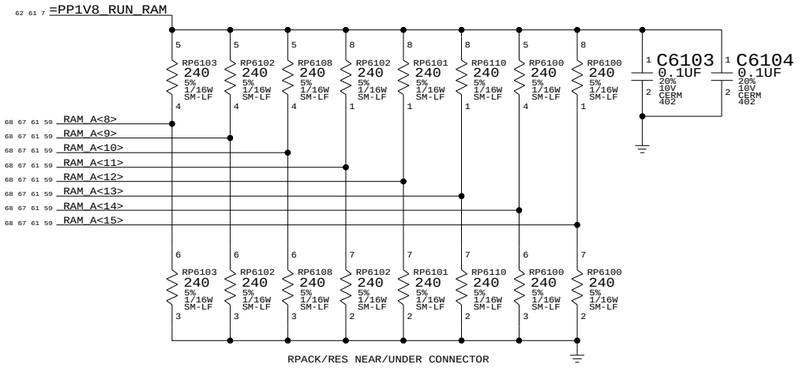
SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

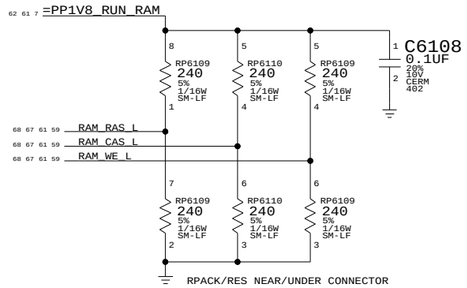
APPLE COMPUTER INC.

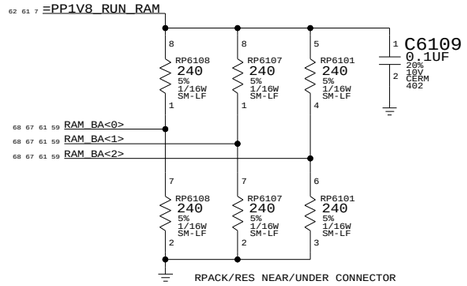
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 59	OF: 154

ALL R PACKS ARE 1/16W 5%









		ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
62 59	RAM_CLKA_P	RAM_KODIAK_CLK_EC	RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP
62 59	RAM_CLKA_N		RAM_CLK	RAM_CLK	RAM_KODIAK_CLK_DP
67 62	RAM_DIMM_A_CLK_P0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP
67 62	RAM_DIMM_A_CLK_N0	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK0_DP
67 62	RAM_DIMM_A_CLK_P1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP
67 62	RAM_DIMM_A_CLK_N1	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK1_DP
67 62	RAM_DIMM_A_CLK_P2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP
67 62	RAM_DIMM_A_CLK_N2	RAM_DIMM_CLK_EC	RAM_CLK	RAM_CLK	RAM_DIMM_CLK2_DP
69 62	RAM_ONBOARD_CLK_P0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP
69 62	RAM_ONBOARD_CLK_N0_1	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK0_DP
69 62	RAM_ONBOARD_CLK_P2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP
69 62	RAM_ONBOARD_CLK_N2_3	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK2_DP
70 62	RAM_ONBOARD_CLK_P4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP
70 62	RAM_ONBOARD_CLK_N4_5	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK4_DP
70 62	RAM_ONBOARD_CLK_P6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP
70 62	RAM_ONBOARD_CLK_N6_7	RAM_ONBOARD_CLK_EC	RAM_CLK	RAM_CLK	RAM_ONBOARD_CLK6_DP
62	RAM_CLK_FBIN_P	RAM_FB_CLK_EC	RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP
62	RAM_CLK_FBIN_N		RAM_CLK	RAM_CLK	RAM_FBIN_CLK_DP
62	RAM_CLK_FBOUT_P		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP
62	RAM_CLK_FBOUT_N		RAM_CLK	RAM_CLK	RAM_FBOUT_CLK_DP
68 59	RAM_DQ<7..0>	RAM_DQS0_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP
68 59	RAM_DQS_N<0>	RAM_DQS0_EC	RAM_DQS	RAM_DQS	RAM_DQS_0_DP
68 59	RAM_DQ<15..8>	RAM_DQS1_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP
68 59	RAM_DQS_N<1>	RAM_DQS1_EC	RAM_DQS	RAM_DQS	RAM_DQS_1_DP
68 59	RAM_DQ<23..16>	RAM_DQS2_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP
68 59	RAM_DQS_N<2>	RAM_DQS2_EC	RAM_DQS	RAM_DQS	RAM_DQS_2_DP
68 59	RAM_DQ<31..24>	RAM_DQS3_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP
68 59	RAM_DQS_N<3>	RAM_DQS3_EC	RAM_DQS	RAM_DQS	RAM_DQS_3_DP
68 59	RAM_DQ<39..32>	RAM_DQS4_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP
68 59	RAM_DQS_N<4>	RAM_DQS4_EC	RAM_DQS	RAM_DQS	RAM_DQS_4_DP
68 59	RAM_DQ<47..40>	RAM_DQS5_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP
68 59	RAM_DQS_N<5>	RAM_DQS5_EC	RAM_DQS	RAM_DQS	RAM_DQS_5_DP
68 59	RAM_DQ<55..48>	RAM_DQS6_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP
68 59	RAM_DQS_N<6>	RAM_DQS6_EC	RAM_DQS	RAM_DQS	RAM_DQS_6_DP
68 59	RAM_DQ<63..56>	RAM_DQS7_EC	RAM_CAD	RAM_CAD	
68 59	RAM_DQS_P<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP
68 59	RAM_DQS_N<7>	RAM_DQS7_EC	RAM_DQS	RAM_DQS	RAM_DQS_7_DP
67 59	RAM_DQ<71..64>	RAM_DQS8_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP
67 59	RAM_DQS_N<8>	RAM_DQS8_EC	RAM_DQS	RAM_DQS	RAM_DQS_8_DP
67 59	RAM_DQ<79..72>	RAM_DQS9_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP
67 59	RAM_DQS_N<9>	RAM_DQS9_EC	RAM_DQS	RAM_DQS	RAM_DQS_9_DP
67 59	RAM_DQ<87..80>	RAM_DQS10_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP
67 59	RAM_DQS_N<10>	RAM_DQS10_EC	RAM_DQS	RAM_DQS	RAM_DQS_10_DP
67 59	RAM_DQ<95..88>	RAM_DQS11_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP
67 59	RAM_DQS_N<11>	RAM_DQS11_EC	RAM_DQS	RAM_DQS	RAM_DQS_11_DP
67 59	RAM_DQ<103..96>	RAM_DQS12_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP
67 59	RAM_DQS_N<12>	RAM_DQS12_EC	RAM_DQS	RAM_DQS	RAM_DQS_12_DP
67 59	RAM_DQ<111..104>	RAM_DQS13_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP
67 59	RAM_DQS_N<13>	RAM_DQS13_EC	RAM_DQS	RAM_DQS	RAM_DQS_13_DP
67 59	RAM_DQ<119..112>	RAM_DQS14_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP
67 59	RAM_DQS_N<14>	RAM_DQS14_EC	RAM_DQS	RAM_DQS	RAM_DQS_14_DP
67 59	RAM_DQ<127..120>	RAM_DQS15_EC	RAM_CAD	RAM_CAD	
67 59	RAM_DQS_P<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP
67 59	RAM_DQS_N<15>	RAM_DQS15_EC	RAM_DQS	RAM_DQS	RAM_DQS_15_DP
70 69 68 6	RAM_DQ_R<127..0>		RAM_CAD	RAM_CAD	
70 69 68	RAM_DQS_P_R<15..0>		RAM_DQS	RAM_DQS	
70 69 68	RAM_DQS_N_R<15..0>		RAM_DQS	RAM_DQS	
68 67 61 59	RAM_A<15..14>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_A<13..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_BA<1..0>	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_BA<2>	RAM_A_CTL_1_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_RAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_CAS_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
68 67 61 59	RAM_WE_L	RAM_A_CTL_EC	RAM_CAD	RAM_CAD	
70 69 68 63	RAM_A_R<15..0>		RAM_CAD	RAM_CAD	
70 69 68 63	RAM_BA_R<2..0>		RAM_CAD	RAM_CAD	
70 69 68 63	RAM_RAS_L_R		RAM_CAD	RAM_CAD	
70 69 68 63	RAM_CAS_L_R		RAM_CAD	RAM_CAD	
70 69 68 63	RAM_WE_L_R		RAM_CAD	RAM_CAD	

61 59	RAM_CS_L<0>	RAM_CS_ONBOARD_EC	RAM_CSCKEODT
61 59	RAM_CS_L<4>	RAM_CS_DIMM_EC	RAM_CSCKEODT
61 59	RAM_CS_L<5>	RAM_CS_DIMM_EC	RAM_CSCKEODT
61 59	RAM_CS_L<8>		RAM_CSCKEODT
61 59	RAM_CS_L<9>		RAM_CSCKEODT
70 69 68 63 61	RAM_CS_L_R<0>		RAM_CSCKEODT
67 61	RAM_CS_DIMM_A		RAM_CSCKEODT
67 61	RAM_CS_DIMM_B		RAM_CSCKEODT
61 59	RAM_CKE<0>	RAM_CKE_DIMM_ONBOARD_EC	RAM_CSCKEODT
61 59	RAM_CKE<1>	RAM_CKE_DIMM_EC	RAM_CSCKEODT
61 59	RAM_CKE<4>		RAM_CSCKEODT
61 59	RAM_CKE<5>		RAM_CSCKEODT
70 69 68 63 62 61	RAM_CKE_R<0>		RAM_CSCKEODT
67 62 61	RAM_CKE_DIMM_B		RAM_CSCKEODT
67 62 61	RAM_CKE_DIMM_A		RAM_CSCKEODT
61 59	RAM_ODT<0>	RAM_ODT_ONBOARD_EC	RAM_CSCKEODT
61 59	RAM_ODT<2>	RAM_ODT_DIMM_EC	RAM_CSCKEODT
61 59	RAM_ODT<4>		RAM_CSCKEODT
70 69 68 63 61	RAM_ODT_R<0>		RAM_CSCKEODT
67 61	RAM_ODT_DIMM_A		RAM_CSCKEODT

RAM_CLK PRIMARY SPACING SET BASED ON DIFF IMPEDANCE
RAM_CLK LINE-LINE SPACING SET TO 15MIL
TOTAL LENGTH TOLERENCE = 20PS = 2.82MM

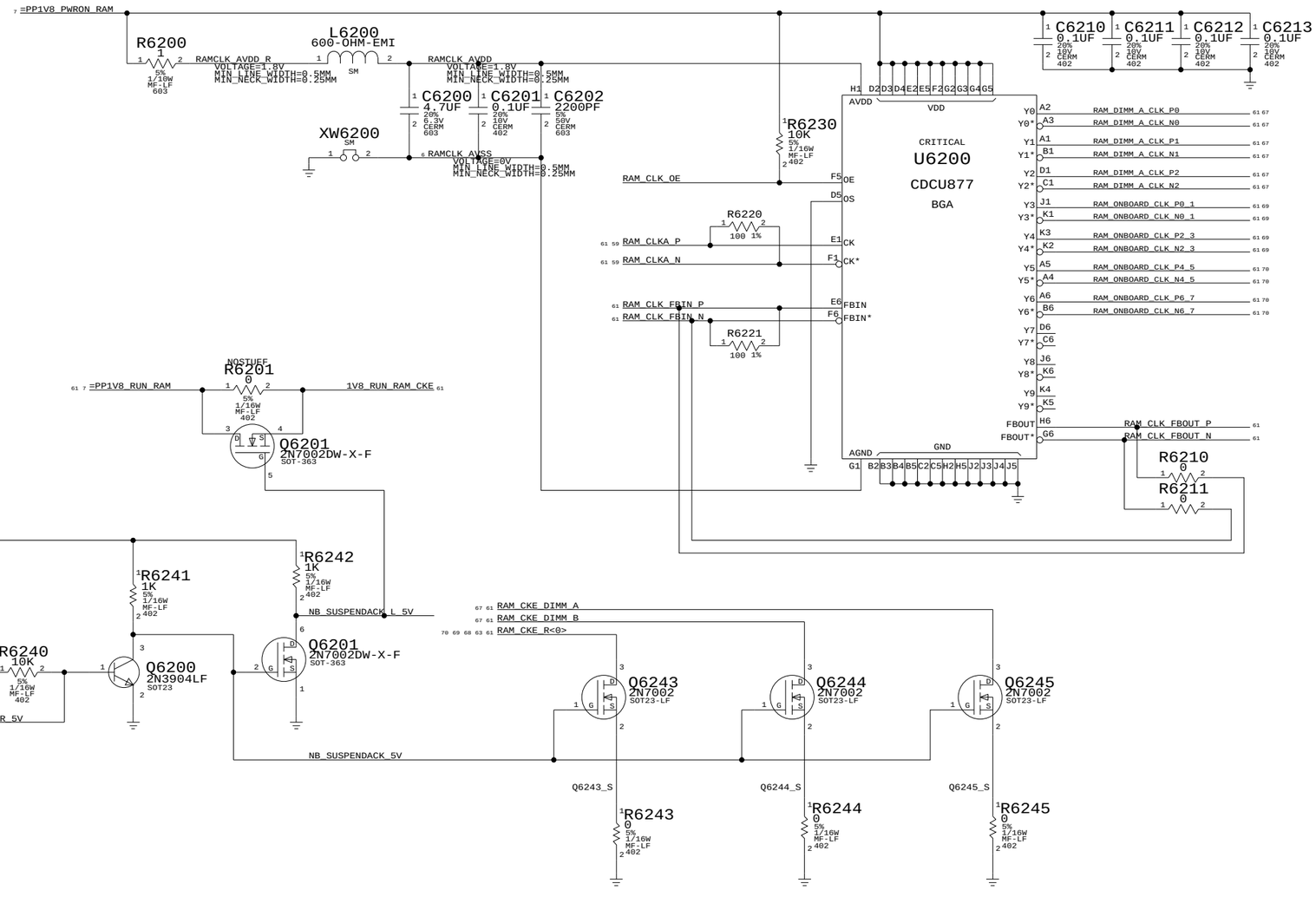
RAM_CAD SPACING IS 10MIL

Parallel Term

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 61 OF 154	

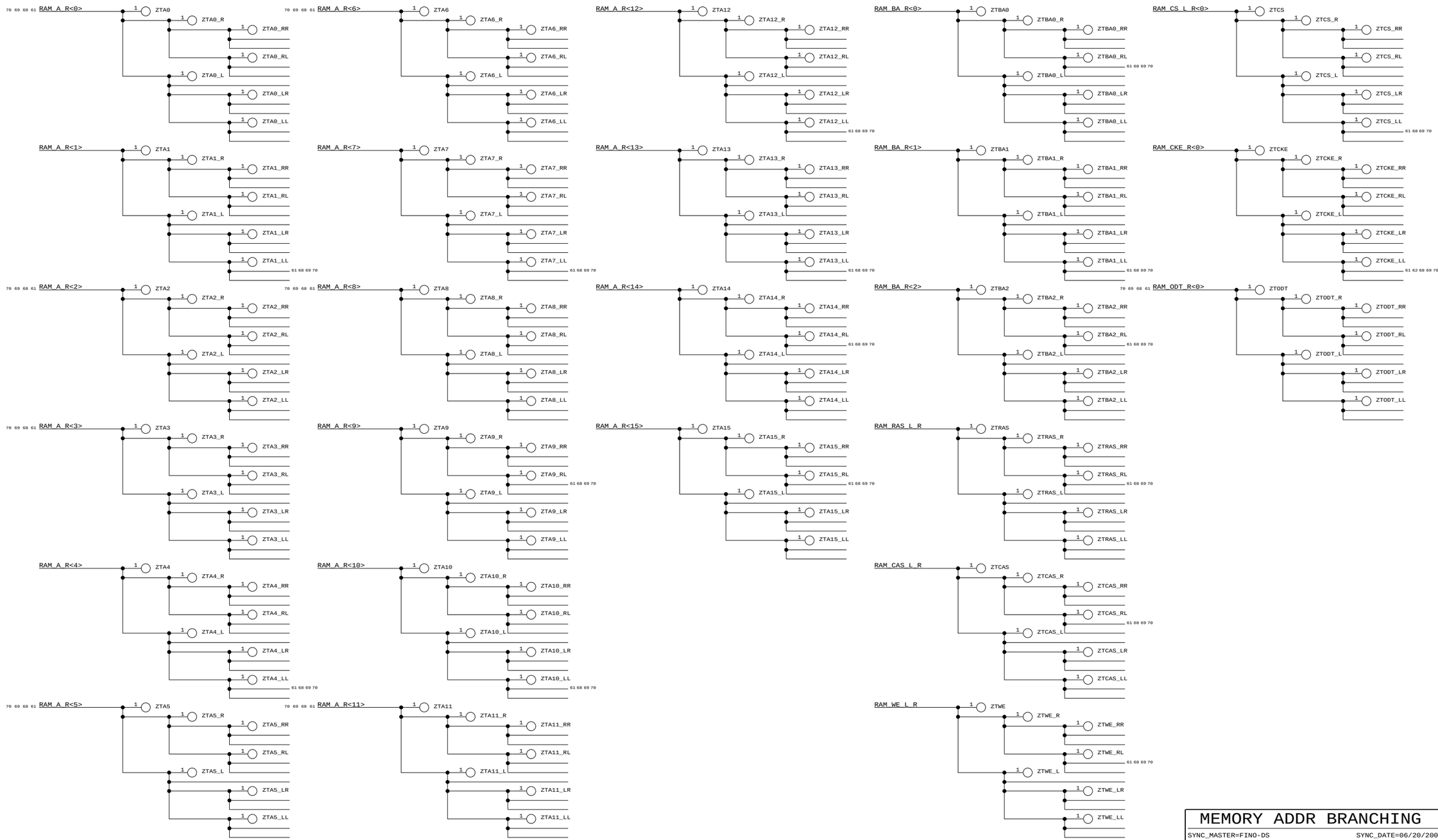


Main Memory Clock Buffer

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 62 OF 154	



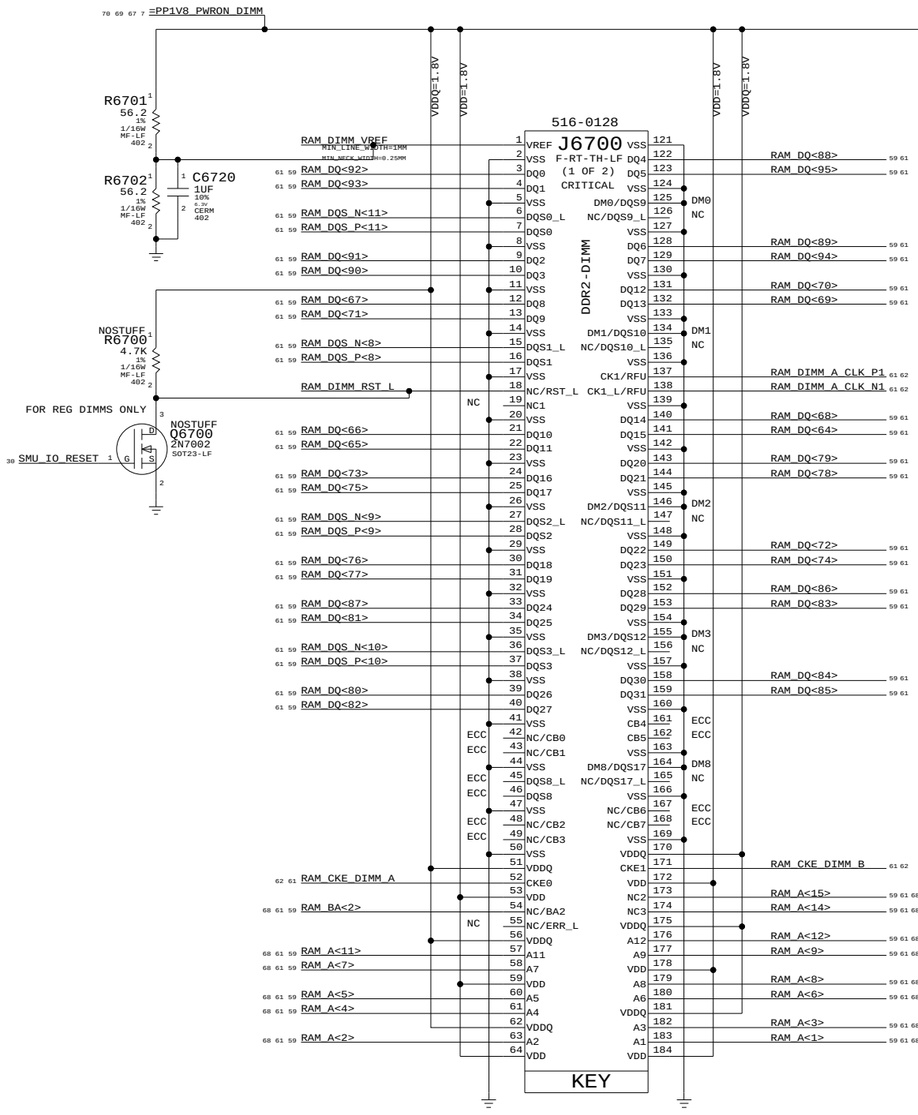
MEMORY ADDR BRANCHING

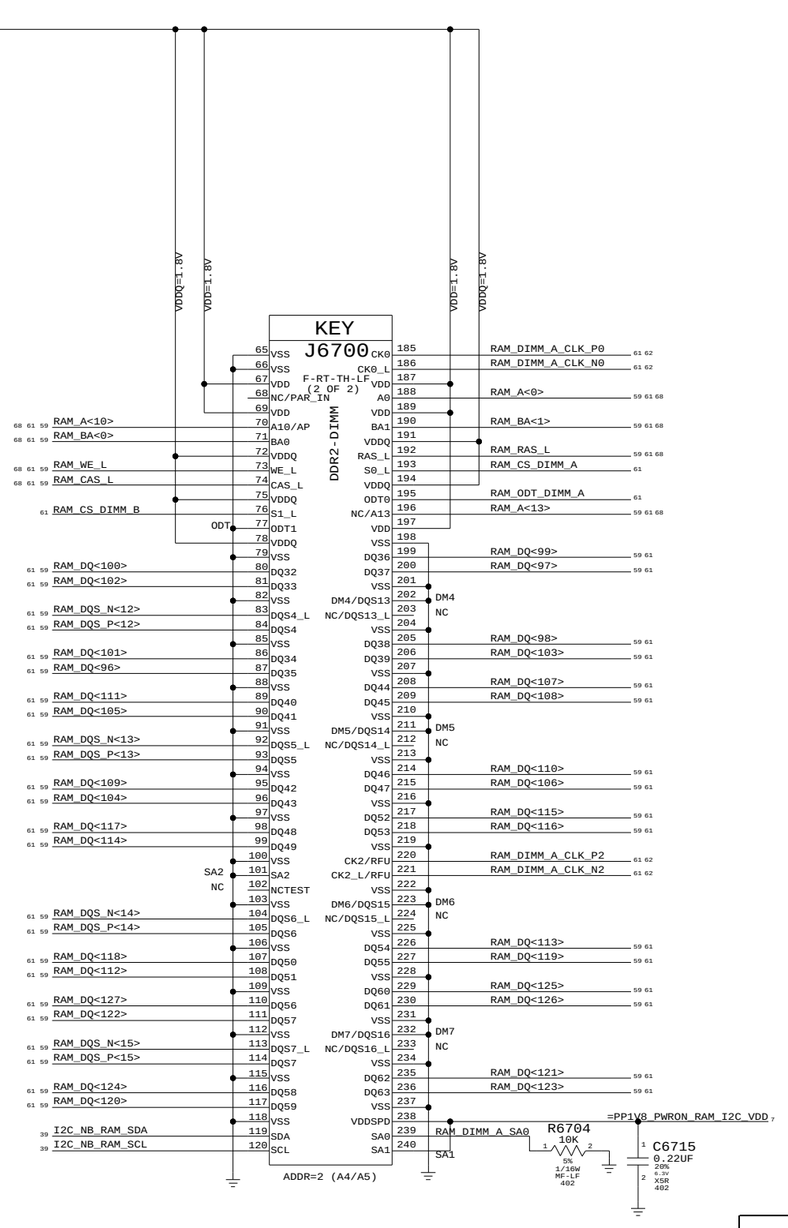
SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

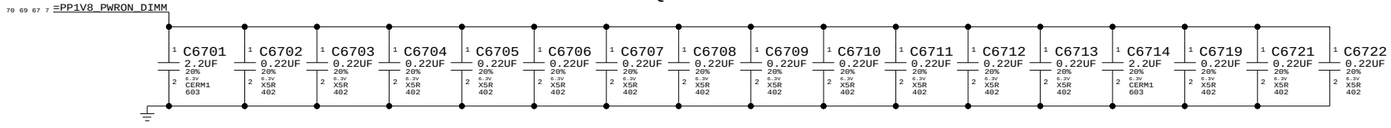
SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE NONE SHT 63 OF 154





PLACE CAPS CLOSE TO VDD/VDDQ PINS OF DIMM SOCKET



Memory Dimm A

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE	SHT	OF
NONE	67	154

ONBOARD MEMORY SHOULD FOLLOW SPEC FOR RAW CARD VERSION A

RAM_DQ<0>	22	4	5	RP6800
RAM_DQ<1>	22	3	6	RP6800
RAM_DQ<2>	22	1	8	RP6801
RAM_DQ<3>	22	3	6	RP6801
RAM_DQ<4>	22	4	5	RP6801
RAM_DQ<5>	22	2	7	RP6800
RAM_DQ<6>	22	2	7	RP6801
RAM_DQ<7>	22	1	8	RP6800
RAM_DQ<8>	22	3	6	RP6802
RAM_DQ<9>	22	4	5	RP6803
RAM_DQ<10>	22	1	8	RP6803
RAM_DQ<11>	22	4	5	RP6802
RAM_DQ<12>	22	3	6	RP6803
RAM_DQ<13>	22	2	7	RP6802
RAM_DQ<14>	22	2	7	RP6803
RAM_DQ<15>	22	1	8	RP6802
RAM_DQ<16>	22	3	6	RP6805
RAM_DQ<17>	22	4	5	RP6805
RAM_DQ<18>	22	1	8	RP6804
RAM_DQ<19>	22	2	7	RP6805
RAM_DQ<20>	22	2	7	RP6804
RAM_DQ<21>	22	4	5	RP6804
RAM_DQ<22>	22	3	6	RP6804
RAM_DQ<23>	22	1	8	RP6805
RAM_DQ<24>	22	4	5	RP6807
RAM_DQ<25>	22	2	7	RP6806
RAM_DQ<26>	22	4	5	RP6806
RAM_DQ<27>	22	1	8	RP6807
RAM_DQ<28>	22	3	6	RP6807
RAM_DQ<29>	22	3	6	RP6806
RAM_DQ<30>	22	2	7	RP6807
RAM_DQ<31>	22	1	8	RP6806
RAM_DQ<32>	22	4	5	RP6809
RAM_DQ<33>	22	2	7	RP6808
RAM_DQ<34>	22	3	6	RP6808
RAM_DQ<35>	22	1	8	RP6809
RAM_DQ<36>	22	2	7	RP6809
RAM_DQ<37>	22	1	8	RP6808
RAM_DQ<38>	22	3	6	RP6809
RAM_DQ<39>	22	4	5	RP6808
RAM_DQ<40>	22	4	5	RP6810
RAM_DQ<41>	22	3	6	RP6811
RAM_DQ<42>	22	1	8	RP6811
RAM_DQ<43>	22	2	7	RP6810
RAM_DQ<44>	22	4	5	RP6811
RAM_DQ<45>	22	3	6	RP6810
RAM_DQ<46>	22	2	7	RP6811
RAM_DQ<47>	22	1	8	RP6810
RAM_DQ<48>	22	3	6	RP6812
RAM_DQ<49>	22	4	5	RP6812
RAM_DQ<50>	22	2	7	RP6813
RAM_DQ<51>	22	1	8	RP6813
RAM_DQ<52>	22	3	6	RP6813
RAM_DQ<53>	22	4	5	RP6813
RAM_DQ<54>	22	2	7	RP6812
RAM_DQ<55>	22	1	8	RP6812
RAM_DQ<56>	22	3	6	RP6814
RAM_DQ<57>	22	4	5	RP6815
RAM_DQ<58>	22	2	7	RP6815
RAM_DQ<59>	22	3	6	RP6815
RAM_DQ<60>	22	2	7	RP6814
RAM_DQ<61>	22	1	8	RP6814
RAM_DQ<62>	22	1	8	RP6815
RAM_DQ<63>	22	4	5	RP6814

RAM_DQS_P<0>	22	1	2	R6800
RAM_DQS_N<0>	22	1	2	R6810
RAM_DQS_P<1>	22	1	2	R6801
RAM_DQS_N<1>	22	1	2	R6811
RAM_DQS_P<2>	22	1	2	R6802
RAM_DQS_N<2>	22	1	2	R6812
RAM_DQS_P<3>	22	1	2	R6803
RAM_DQS_N<3>	22	1	2	R6813
RAM_DQS_P<4>	22	1	2	R6804
RAM_DQS_N<4>	22	1	2	R6814
RAM_DQS_P<5>	22	1	2	R6805
RAM_DQS_N<5>	22	1	2	R6815
RAM_DQS_P<6>	22	1	2	R6806
RAM_DQS_N<6>	22	1	2	R6816
RAM_DQS_P<7>	22	1	2	R6807
RAM_DQS_N<7>	22	1	2	R6817

RAM_A<0>	5.1	1	8	RP6824
RAM_A<1>	5.1	1	8	RP6823
RAM_A<2>	5.1	2	7	RP6823
RAM_A<3>	5.1	4	5	RP6822
RAM_A<4>	5.1	3	6	RP6822
RAM_A<5>	5.1	2	7	RP6822
RAM_A<6>	5.1	1	8	RP6822
RAM_A<7>	5.1	3	6	RP6821
RAM_A<8>	5.1	4	5	RP6821
RAM_A<9>	5.1	1	8	RP6821
RAM_A<10>	5.1	3	6	RP6824
RAM_A<11>	5.1	2	7	RP6821
RAM_A<12>	5.1	4	5	RP6820
RAM_A<13>	5.1	4	5	RP6825
RAM_A<14>	5.1	2	7	RP6820
RAM_A<15>	5.1	1	8	RP6820

RAM_A R<0>	1	ZT6800	1	ZT6801
RAM_A R<1>	1	ZT6802	1	ZT6803
RAM_A R<2>	1	ZT6804	1	ZT6805
RAM_A R<3>	1	ZT6806	1	ZT6807
RAM_A R<4>	1	ZT6808	1	ZT6809
RAM_A R<5>	1	ZT6810	1	ZT6811
RAM_A R<6>	1	ZT6812	1	ZT6813
RAM_A R<7>	1	ZT6814	1	ZT6815

VIAS FOR ECC STUB

RAM_BA<0>	5.1	4	5	RP6824
RAM_BA<1>	5.1	2	7	RP6824
RAM_BA<2>	5.1	3	6	RP6820
RAM_RAS_L	5.1	1	8	RP6825
RAM_CAS_L	5.1	3	6	RP6825
RAM_WE_L	5.1	2	7	RP6825

RAM_BA R<0>	1	ZT6820
RAM_BA R<1>	1	ZT6821
RAM_BA R<2>	1	ZT6822
RAM_RAS_L_R	1	ZT6825
RAM_CAS_L_R	1	ZT6826
RAM_WE_L_R	1	ZT6827

VIAS FOR ECC STUB

PLACE NEAR KODIAK PRIOR TO BRANCH

PLACE AT END POINT TO SIMULATE ECC

C6870 24PF	5% 50V C0G 402	C6871 2PF	+/-0.25PF 50V C0G 402-1
C6880 24PF	5% 50V C0G 402	C6881 2PF	+/-0.25PF 50V C0G 402-1
C6890 24PF	5% 50V C0G 402	C6891 2PF	+/-0.25PF 50V C0G 402-1

RAM_CS_L_R<0>

RAM_CKE_R<0>

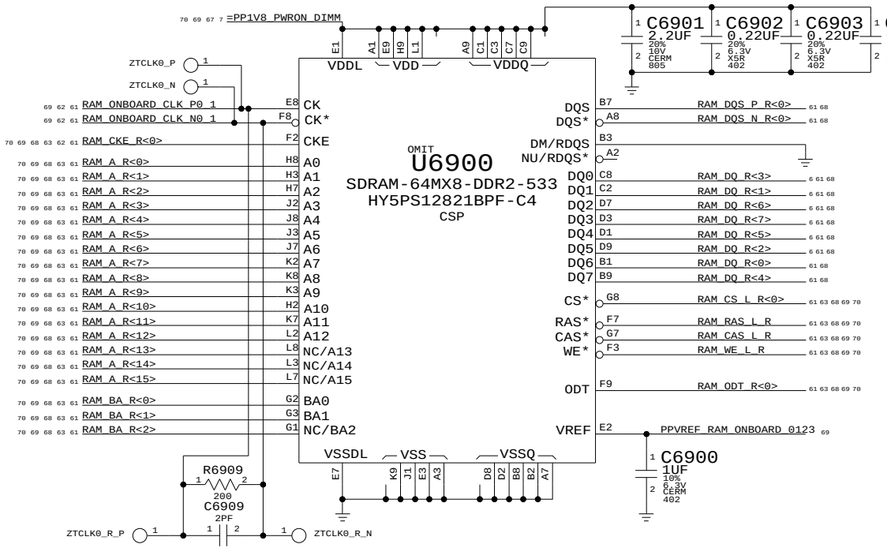
RAM_ODT_R<0>

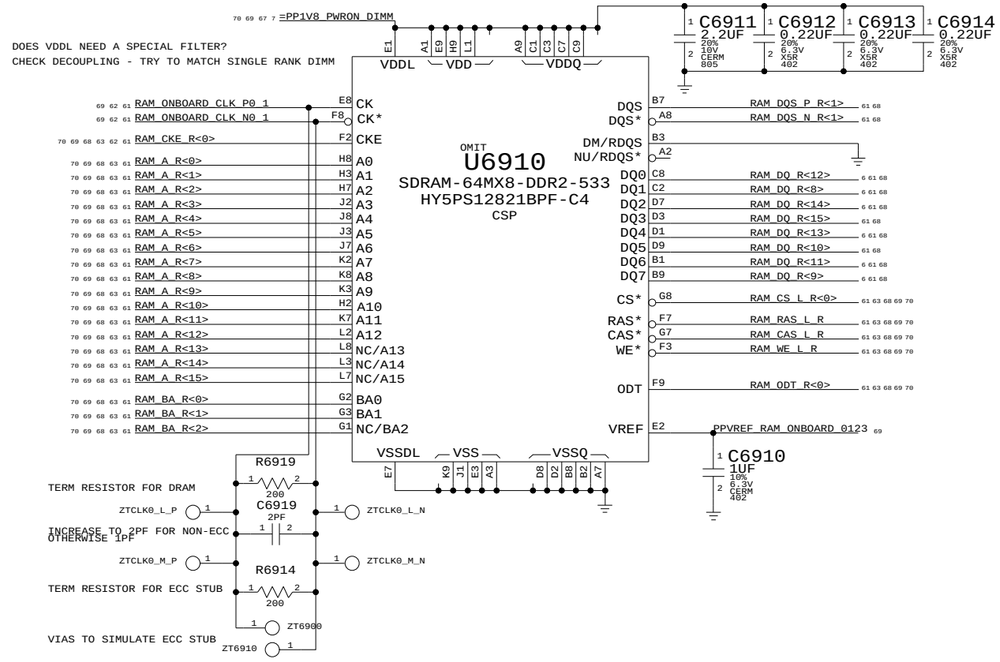
MLB Mem Series Term

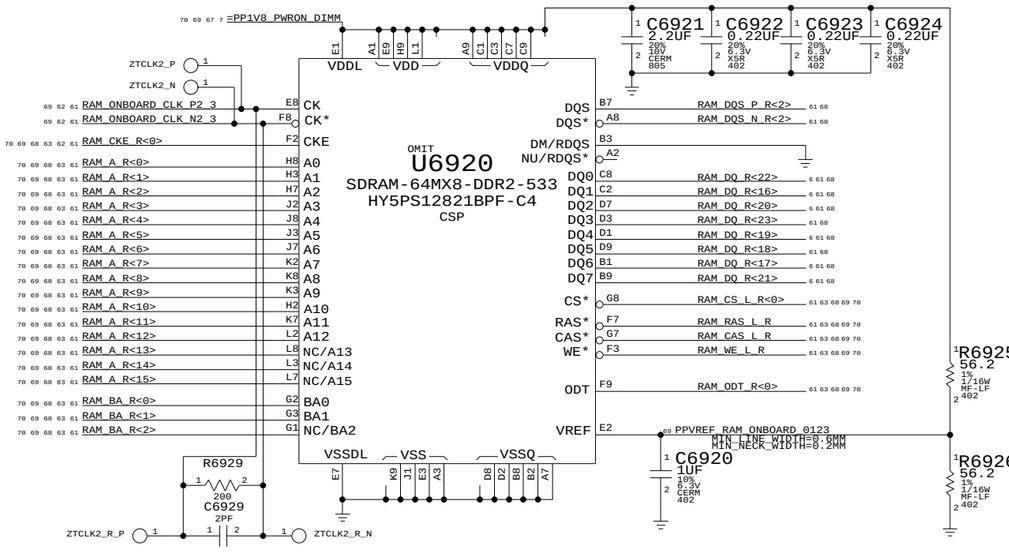
SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

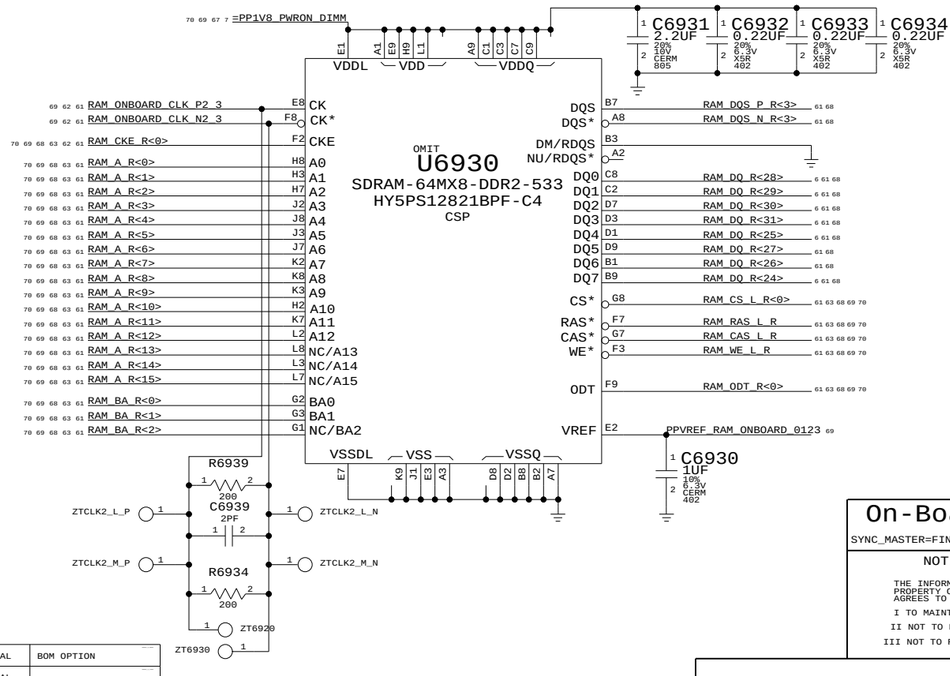
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 68 OF 154	









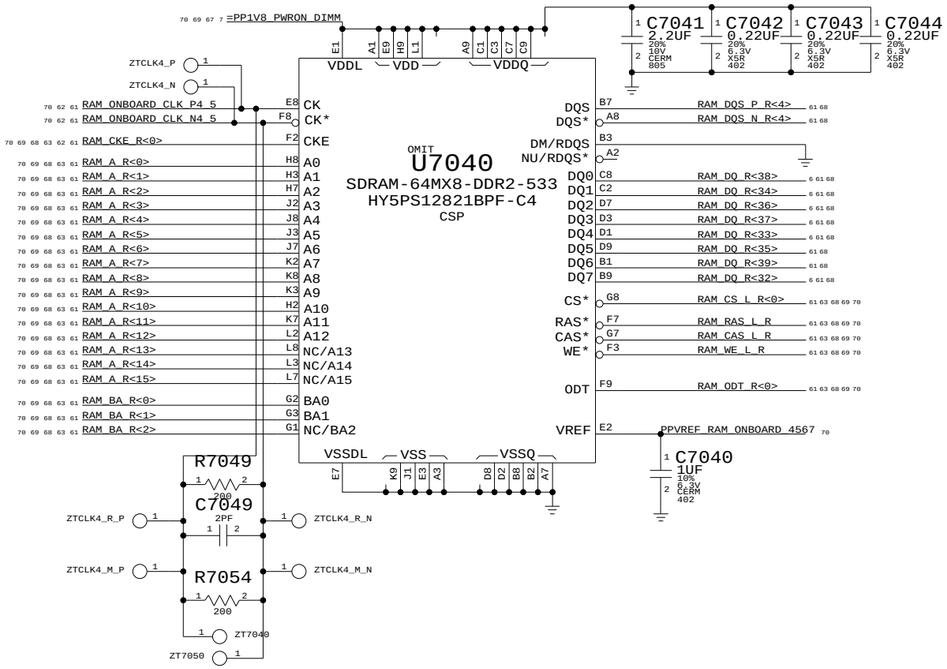
PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U6900,U6910,U6920,U6930	CRITICAL	
333T0032	4	IC,SDRAM,DDR2,512MBIT,X8	U7040,U7050,U7060,U7070	CRITICAL	

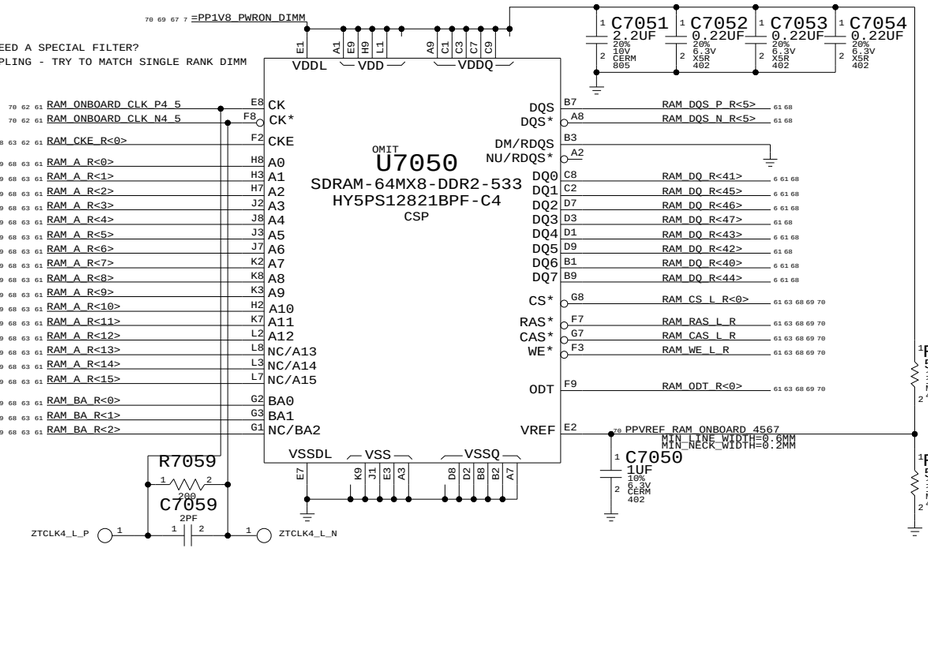
On-Board DDR SDRAM

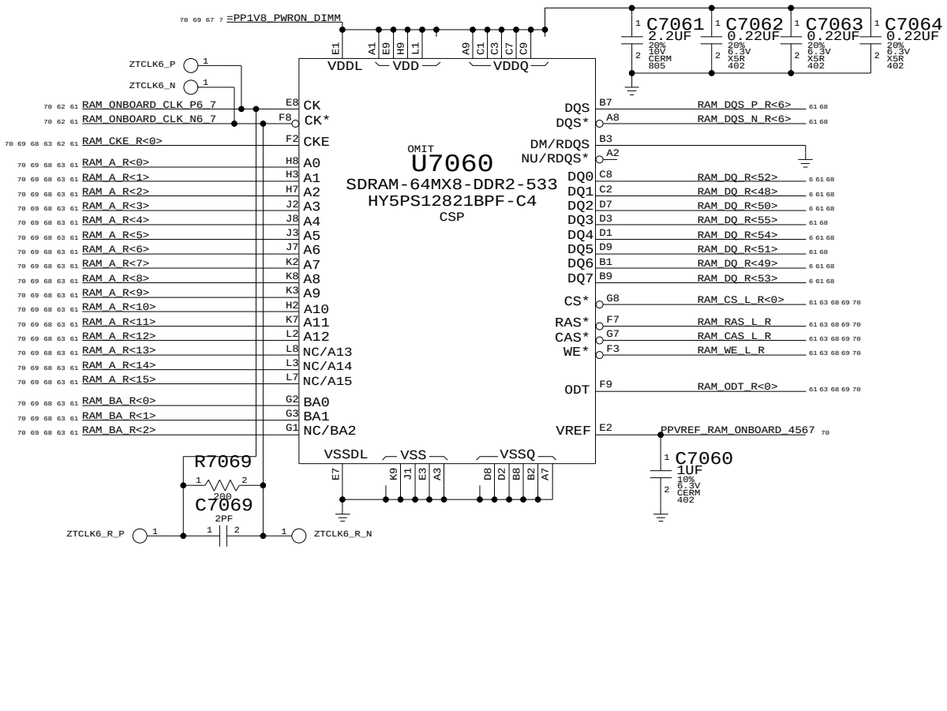
SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

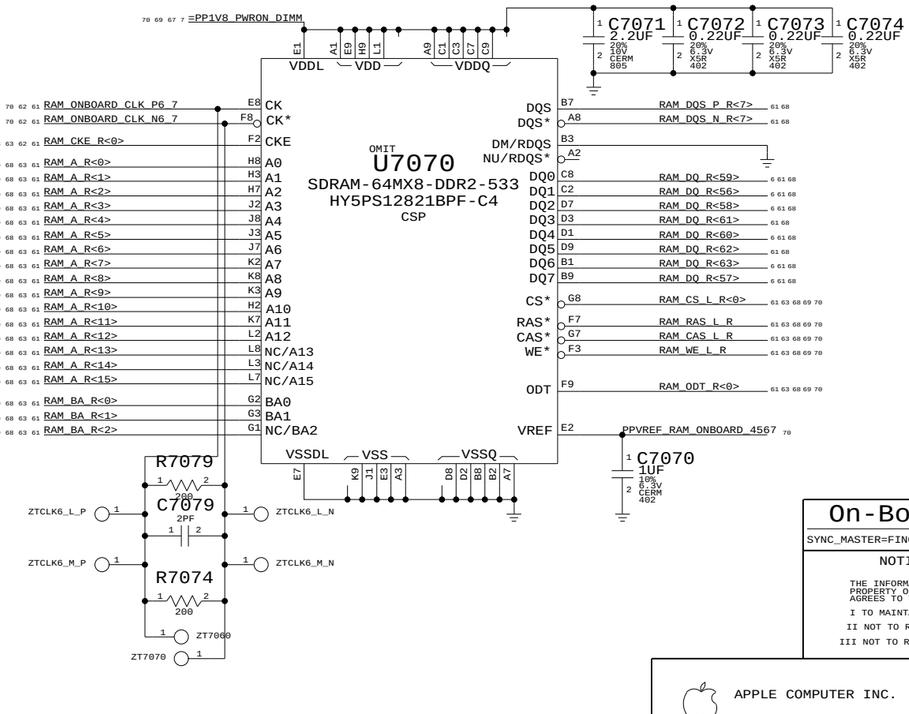
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 69 OF 154	







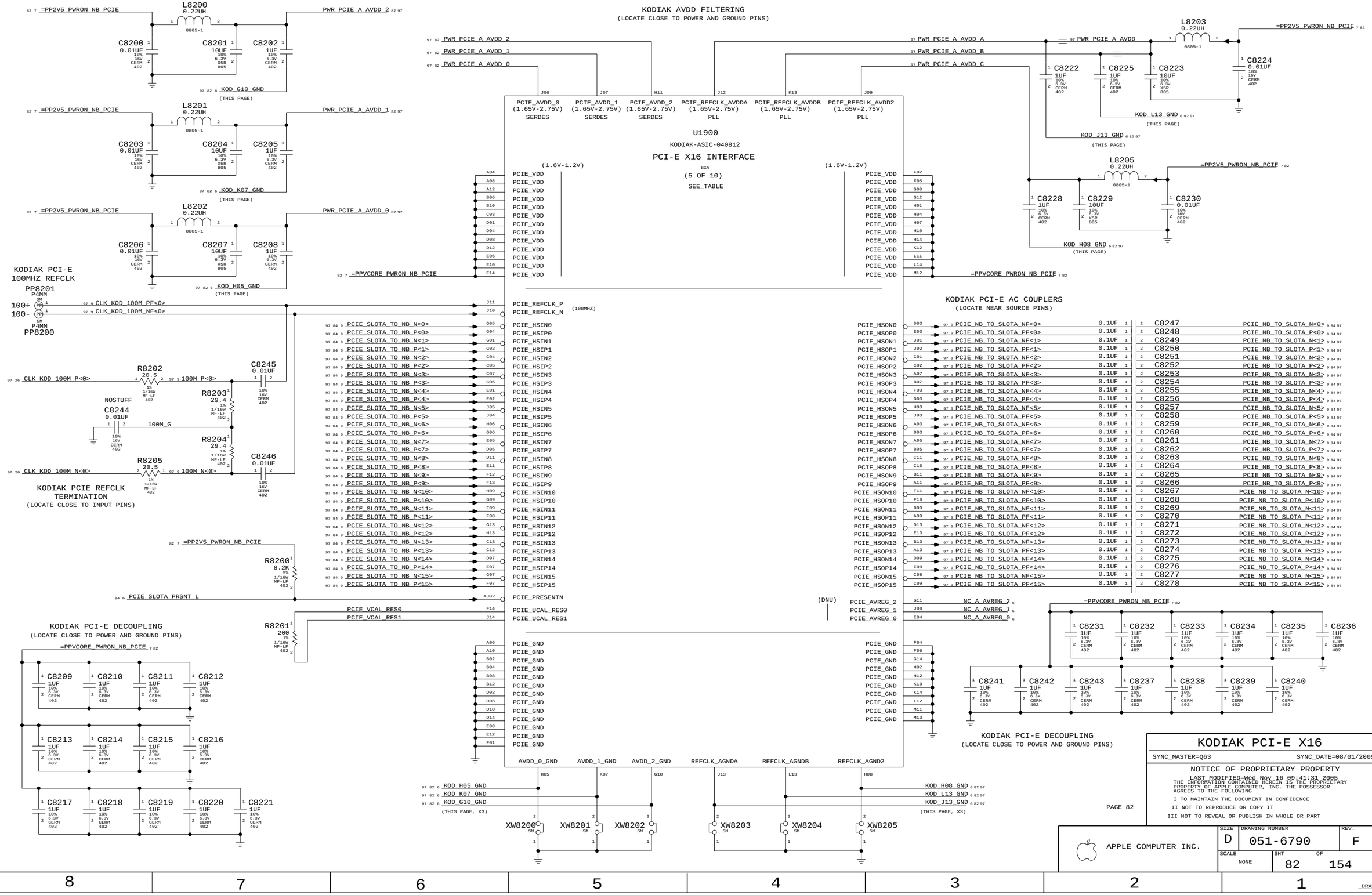


On-Board DDR SDRAM

SYNC_MASTER=FINO-DS SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 70 OF 154	


KODIAK AVDD FILTERING
(LOCATE CLOSE TO POWER AND GROUND PINS)
L8200 0.22UH
L8201 0.22UH
L8202 0.22UH
L8203 0.22UH
L8205 0.22UH
=PP2V5_PWRON_NB_PCIE
PWR_PCIE_A_AVDD_2
PWR_PCIE_A_AVDD_1
PWR_PCIE_A_AVDD_0
KOD_G10_GND
KOD_K07_GND
KOD_H05_GND
KOD_L13_GND
KOD_J13_GND
KOD_H08_GND
(THIS PAGE)
PWR_PCIE_A_AVDD_A
PWR_PCIE_A_AVDD_B
PWR_PCIE_A_AVDD_C
PWR_PCIE_A_AVDD
PCIE_AVDD_0 (1.65V-2.75V) SERDES
PCIE_AVDD_1 (1.65V-2.75V) SERDES
PCIE_AVDD_2 (1.65V-2.75V) SERDES
PCIE_REFCLK_AVDDA (1.65V-2.75V) PLL
PCIE_REFCLK_AVDDB (1.65V-2.75V) PLL
PCIE_REFCLK_AVDD2 (1.65V-2.75V) PLL
U1900
KODIAK-ASIC-040812
PCI-E X16 INTERFACE
BGA
(5 OF 10)
SEE_TABLE
(1.6V-1.2V)
PCIE_VDD
=PPVCORE_PWRON_NB_PCIE
KODIAK PCI-E 100MHZ REFCLK
PP8201
PP8200
P4MM
CLK_KOD_100M_PF<0>
CLK_KOD_100M_NF<0>
KODIAK PCIE REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)
R8202 20.5
R8203 29.4
R8204 29.4
R8205 20.5
C8244 0.01UF
C8245 0.01UF
C8246 0.01UF
NOSTUFF
100M_G
CLK_KOD_100M_P<0>
CLK_KOD_100M_N<0>
PCIE_REFCLK_P
PCIE_REFCLK_N
(100MHZ)
PCIE_HSIN0
PCIE_HSIP0
PCIE_HSIN1
PCIE_HSIP1
PCIE_HSIN2
PCIE_HSIP2
PCIE_HSIN3
PCIE_HSIP3
PCIE_HSIN4
PCIE_HSIP4
PCIE_HSIN5
PCIE_HSIP5
PCIE_HSIN6
PCIE_HSIP6
PCIE_HSIN7
PCIE_HSIP7
PCIE_HSIN8
PCIE_HSIP8
PCIE_HSIN9
PCIE_HSIP9
PCIE_HSIN10
PCIE_HSIP10
PCIE_HSIN11
PCIE_HSIP11
PCIE_HSIN12
PCIE_HSIP12
PCIE_HSIN13
PCIE_HSIP13
PCIE_HSIN14
PCIE_HSIP14
PCIE_HSIN15
PCIE_HSIP15
PCIE_SLOTA_TO_NB_N<0>
PCIE_SLOTA_TO_NB_P<0>
PCIE_SLOTA_TO_NB_N<1>
PCIE_SLOTA_TO_NB_P<1>
PCIE_SLOTA_TO_NB_N<2>
PCIE_SLOTA_TO_NB_P<2>
PCIE_SLOTA_TO_NB_N<3>
PCIE_SLOTA_TO_NB_P<3>
PCIE_SLOTA_TO_NB_N<4>
PCIE_SLOTA_TO_NB_P<4>
PCIE_SLOTA_TO_NB_N<5>
PCIE_SLOTA_TO_NB_P<5>
PCIE_SLOTA_TO_NB_N<6>
PCIE_SLOTA_TO_NB_P<6>
PCIE_SLOTA_TO_NB_N<7>
PCIE_SLOTA_TO_NB_P<7>
PCIE_SLOTA_TO_NB_N<8>
PCIE_SLOTA_TO_NB_P<8>
PCIE_SLOTA_TO_NB_N<9>
PCIE_SLOTA_TO_NB_P<9>
PCIE_SLOTA_TO_NB_N<10>
PCIE_SLOTA_TO_NB_P<10>
PCIE_SLOTA_TO_NB_N<11>
PCIE_SLOTA_TO_NB_P<11>
PCIE_SLOTA_TO_NB_N<12>
PCIE_SLOTA_TO_NB_P<12>
PCIE_SLOTA_TO_NB_N<13>
PCIE_SLOTA_TO_NB_P<13>
PCIE_SLOTA_TO_NB_N<14>
PCIE_SLOTA_TO_NB_P<14>
PCIE_SLOTA_TO_NB_N<15>
PCIE_SLOTA_TO_NB_P<15>
PCIE_SLOTA_PRSNT_L
PCIE_VCAL_RES0
PCIE_VCAL_RES1
R8200 8.2K
R8201 200
PCIE_PRESENTN
PCIE_UCAL_RES0
PCIE_UCAL_RES1
(DNU)
PCIE_AVREG_2
PCIE_AVREG_1
PCIE_AVREG_0
NC_A_AVREG_2
NC_A_AVREG_1
NC_A_AVREG_0
PCIE_GND
KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)
KODIAK PCI-E AC COUPLERS
(LOCATE NEAR SOURCE PINS)
PCIE_HSON0
PCIE_HSOP0
PCIE_HSON1
PCIE_HSOP1
PCIE_HSON2
PCIE_HSOP2
PCIE_HSON3
PCIE_HSOP3
PCIE_HSON4
PCIE_HSOP4
PCIE_HSON5
PCIE_HSOP5
PCIE_HSON6
PCIE_HSOP6
PCIE_HSON7
PCIE_HSOP7
PCIE_HSON8
PCIE_HSOP8
PCIE_HSON9
PCIE_HSOP9
PCIE_HSON10
PCIE_HSOP10
PCIE_HSON11
PCIE_HSOP11
PCIE_HSON12
PCIE_HSOP12
PCIE_HSON13
PCIE_HSOP13
PCIE_HSON14
PCIE_HSOP14
PCIE_HSON15
PCIE_HSOP15
PCIE_NB_TO_SLOTA_NF<0>
PCIE_NB_TO_SLOTA_PF<0>
PCIE_NB_TO_SLOTA_NF<1>
PCIE_NB_TO_SLOTA_PF<1>
PCIE_NB_TO_SLOTA_NF<2>
PCIE_NB_TO_SLOTA_PF<2>
PCIE_NB_TO_SLOTA_NF<3>
PCIE_NB_TO_SLOTA_PF<3>
PCIE_NB_TO_SLOTA_NF<4>
PCIE_NB_TO_SLOTA_PF<4>
PCIE_NB_TO_SLOTA_NF<5>
PCIE_NB_TO_SLOTA_PF<5>
PCIE_NB_TO_SLOTA_NF<6>
PCIE_NB_TO_SLOTA_PF<6>
PCIE_NB_TO_SLOTA_NF<7>
PCIE_NB_TO_SLOTA_PF<7>
PCIE_NB_TO_SLOTA_NF<8>
PCIE_NB_TO_SLOTA_PF<8>
PCIE_NB_TO_SLOTA_NF<9>
PCIE_NB_TO_SLOTA_PF<9>
PCIE_NB_TO_SLOTA_NF<10>
PCIE_NB_TO_SLOTA_PF<10>
PCIE_NB_TO_SLOTA_NF<11>
PCIE_NB_TO_SLOTA_PF<11>
PCIE_NB_TO_SLOTA_NF<12>
PCIE_NB_TO_SLOTA_PF<12>
PCIE_NB_TO_SLOTA_NF<13>
PCIE_NB_TO_SLOTA_PF<13>
PCIE_NB_TO_SLOTA_NF<14>
PCIE_NB_TO_SLOTA_PF<14>
PCIE_NB_TO_SLOTA_NF<15>
PCIE_NB_TO_SLOTA_PF<15>
0.1UF
C8247 PCIE_NB_TO_SLOTA_N<0>
C8248 PCIE_NB_TO_SLOTA_P<0>
C8249 PCIE_NB_TO_SLOTA_N<1>
C8250 PCIE_NB_TO_SLOTA_P<1>
C8251 PCIE_NB_TO_SLOTA_N<2>
C8252 PCIE_NB_TO_SLOTA_P<2>
C8253 PCIE_NB_TO_SLOTA_N<3>
C8254 PCIE_NB_TO_SLOTA_P<3>
C8255 PCIE_NB_TO_SLOTA_N<4>
C8256 PCIE_NB_TO_SLOTA_P<4>
C8257 PCIE_NB_TO_SLOTA_N<5>
C8258 PCIE_NB_TO_SLOTA_P<5>
C8259 PCIE_NB_TO_SLOTA_N<6>
C8260 PCIE_NB_TO_SLOTA_P<6>
C8261 PCIE_NB_TO_SLOTA_N<7>
C8262 PCIE_NB_TO_SLOTA_P<7>
C8263 PCIE_NB_TO_SLOTA_N<8>
C8264 PCIE_NB_TO_SLOTA_P<8>
C8265 PCIE_NB_TO_SLOTA_N<9>
C8266 PCIE_NB_TO_SLOTA_P<9>
C8267 PCIE_NB_TO_SLOTA_N<10>
C8268 PCIE_NB_TO_SLOTA_P<10>
C8269 PCIE_NB_TO_SLOTA_N<11>
C8270 PCIE_NB_TO_SLOTA_P<11>
C8271 PCIE_NB_TO_SLOTA_N<12>
C8272 PCIE_NB_TO_SLOTA_P<12>
C8273 PCIE_NB_TO_SLOTA_N<13>
C8274 PCIE_NB_TO_SLOTA_P<13>
C8275 PCIE_NB_TO_SLOTA_N<14>
C8276 PCIE_NB_TO_SLOTA_P<14>
C8277 PCIE_NB_TO_SLOTA_N<15>
C8278 PCIE_NB_TO_SLOTA_P<15>
KODIAK PCI-E DECOUPLING
(LOCATE CLOSE TO POWER AND GROUND PINS)
AVDD_0_GND
AVDD_1_GND
AVDD_2_GND
REFCLK_AGNDA
REFCLK_AGNDB
REFCLK_AGND2
(THIS PAGE, X3)
XW8200
XW8201
XW8202
XW8203
XW8204
XW8205
KODIAK PCI-E X16
SYNC_MASTER=Q63
SYNC_DATE=08/01/2005
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Nov 16 09:41:31 2005
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
PAGE 82
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6790
REV. F
SCALE NONE
SHT 82 OF 154

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION	
338S0239	1	IC,RV370 XT, GRAPHICS CTLR	U8400	RV370XT	CRITICAL
338S0265	1	IC,RV380 XT A23, GRAPHICS CTLR	U8400	RV380XT	CRITICAL

REMOVED COMPLIANCE TEST POINTS
FINO WILL PLACE COUPLING CAPACITORS ON RECEIVING SIDE
(THIS IS ALLOWED FOR CHIP TO CHIP PCIE)
CAP PAD CAN BE USED FOR COMPLIANCE TEST

THIS IS ALIASED TO
PPVCORE_GPU ON PAGE 7

SYS_POWERUP_L SHOULD CONTROL THE FET ON PP1V2_RUN

PLACE R8470 CLOSE TO U9670

GROUND VIAS FOR LAYER TRANSITIONS

PCI-E SLOTA 100MHZ
REFCLK TERMINATION
(LOCATE CLOSE TO GPU)

GPU PCI-E AC COUPLERS (PLACE NEAR GPU)

XW8405

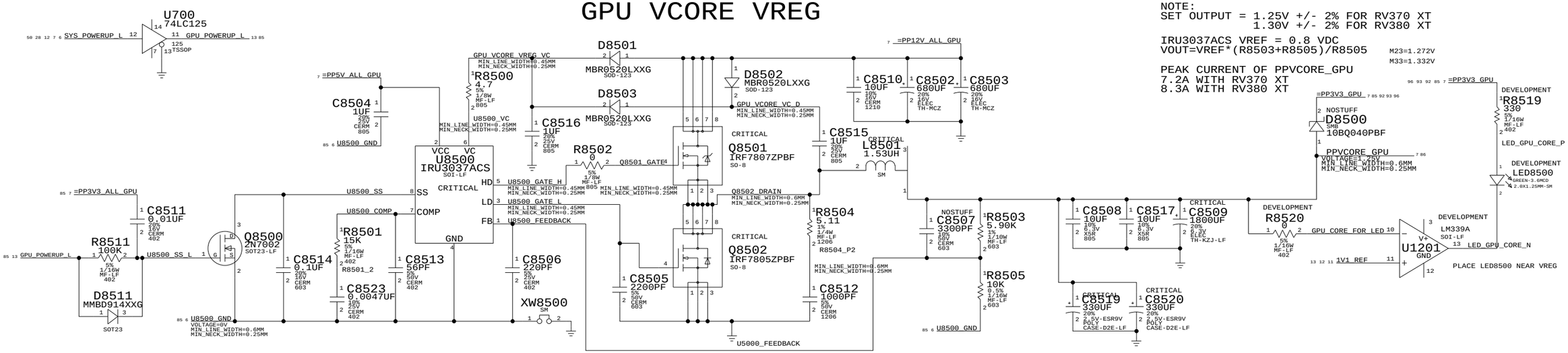
GPU PCIe

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 84	OF: 154

GPU VCORE VREG



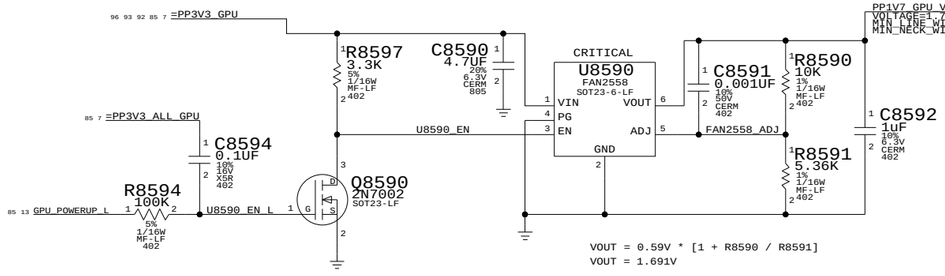
NOTE:
SET OUTPUT = 1.25V +/- 2% FOR RV370 XT
1.30V +/- 2% FOR RV380 XT

IRU3037ACS VREF = 0.8 VDC
VOUT=VREF*(R8503+R8505)/R8505

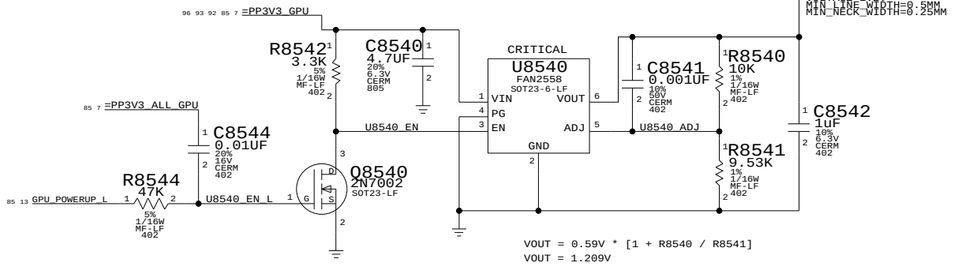
M23=1.272V
M33=1.332V

PEAK CURRENT OF PPVCORE_GPU
7.2A WITH RV370 XT
8.3A WITH RV380 XT

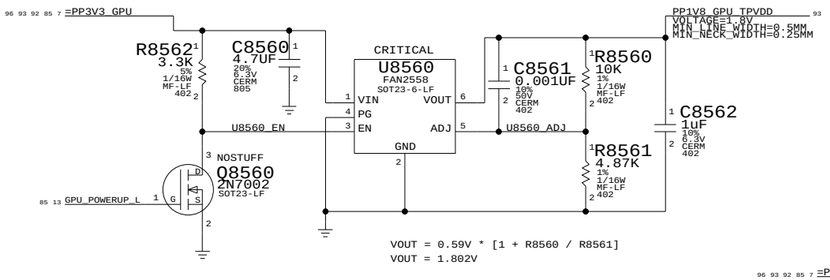
GPU 1.7V VDDC_CT



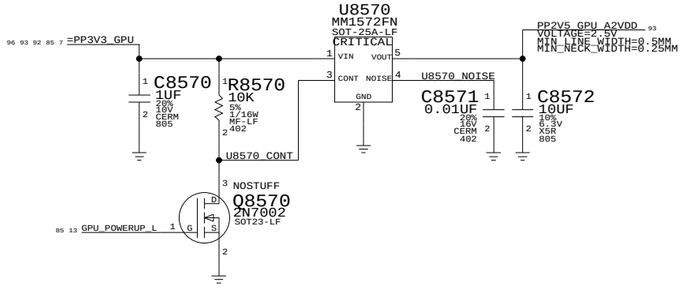
GPU 1.20V PCIE PVDD



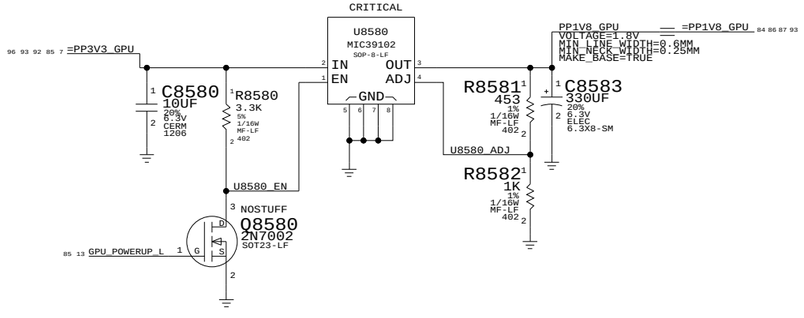
GPU 1.80V TPVDD



GPU 2.5V A2VDD



GPU 1.8V VREG



POWER SEQUENCING FOR RV370/80: =PP3V3_GPU > =PPV_GPU_MEM > VDDC_CT > PPVCORE_GPU
PP2V5_GPU_A2VDD > PP1V8_GPU > PCIE_PVDD

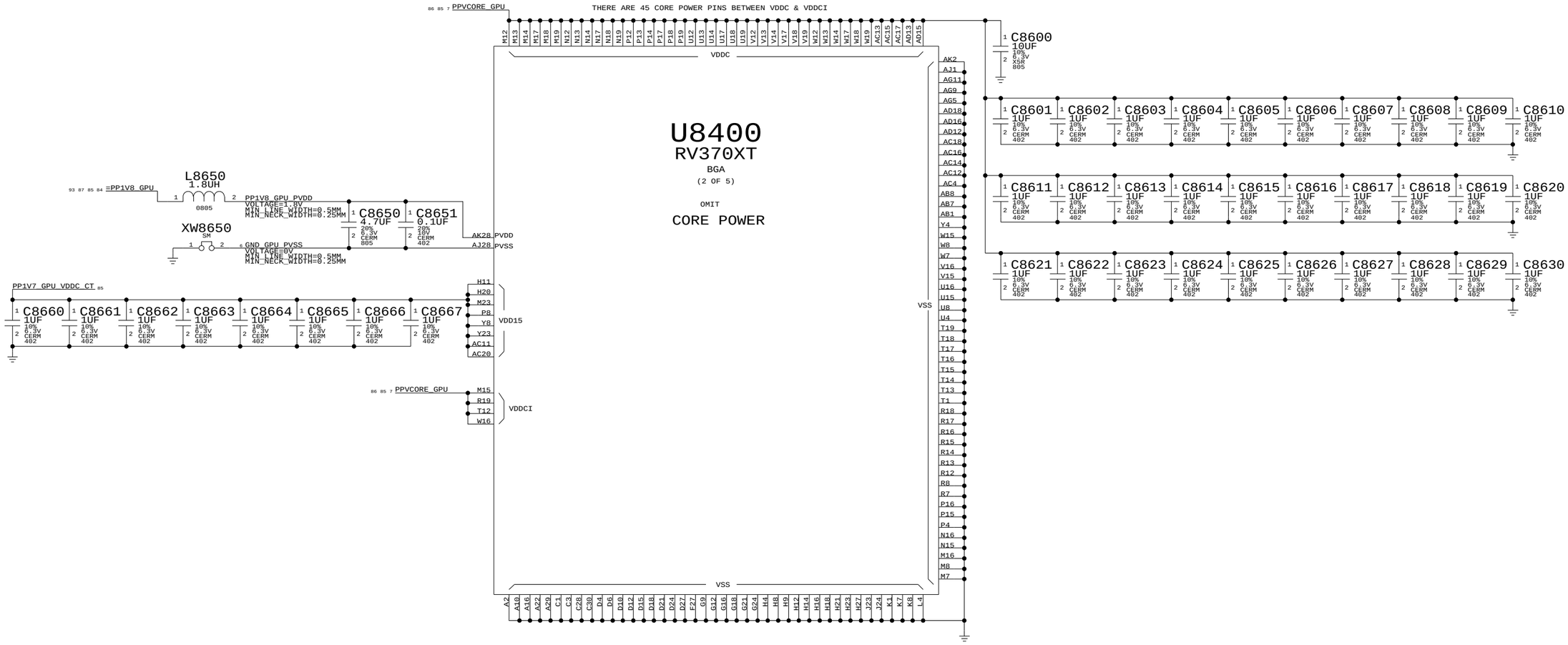
THE ENTIRE SEQUENCE SHOULD TAKE LESS THAN 40 MS (T1+T3 IN DATABOOK)
HOWEVER IDEALLY ALL POWER RAILS SHOULD RAMP TOGETHER
POWER DOWN SEQUENCE SHOULD BE IN REVERSE ORDER

Graphics Vregs

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 85 OF 154	

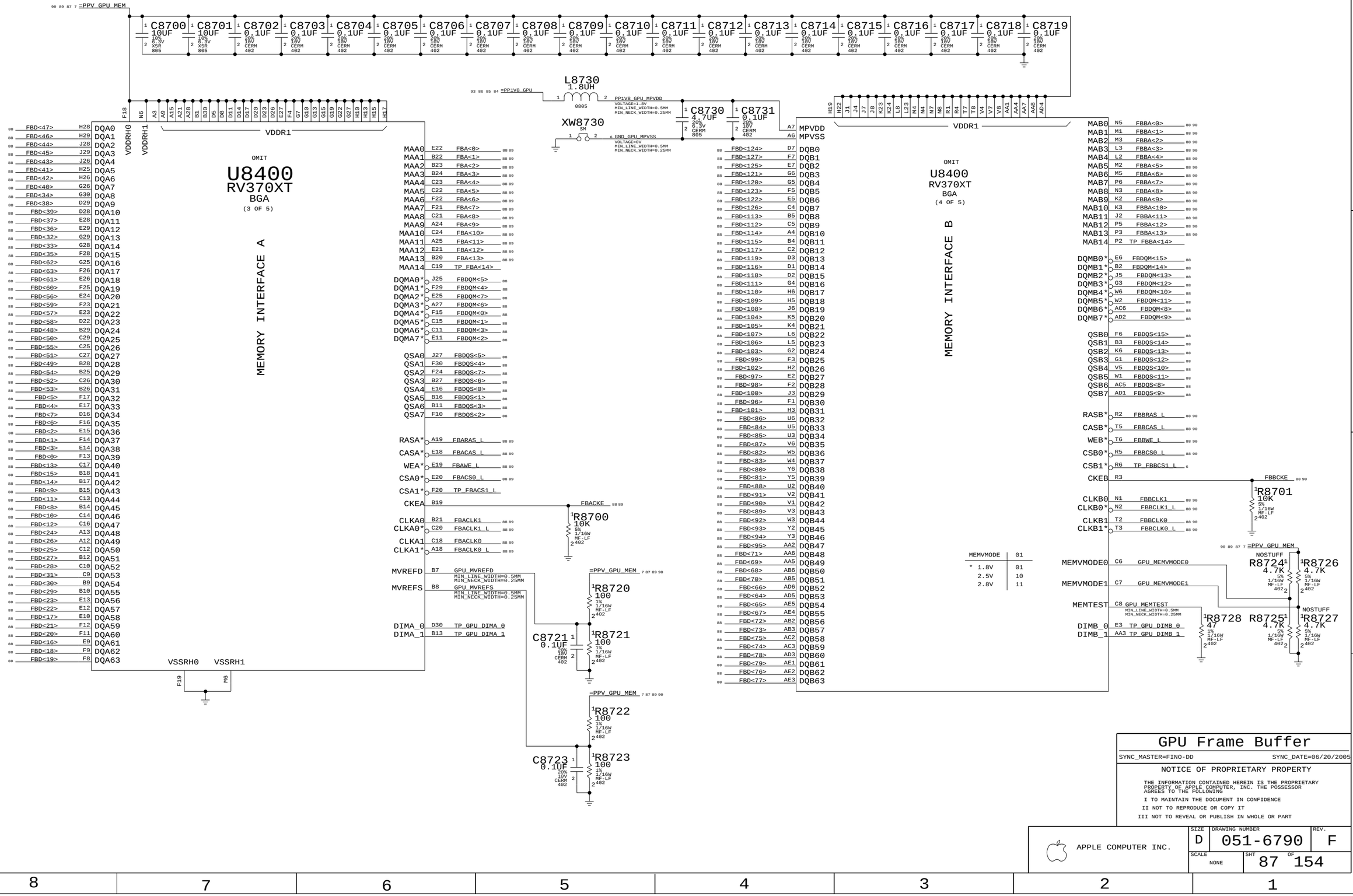


GPU Core Power

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 86 OF 154	


=PPV_GPU_MEM
C8700 10UF 10% 6.3V XSR 805
C8701 10UF 10% 6.3V XSR 805
C8702 0.1UF 20% 10V CERM 402
C8703 0.1UF 20% 10V CERM 402
C8704 0.1UF 20% 10V CERM 402
C8705 0.1UF 20% 10V CERM 402
C8706 0.1UF 20% 10V CERM 402
C8707 0.1UF 20% 10V CERM 402
C8708 0.1UF 20% 10V CERM 402
C8709 0.1UF 20% 10V CERM 402
C8710 0.1UF 20% 10V CERM 402
C8711 0.1UF 20% 10V CERM 402
C8712 0.1UF 20% 10V CERM 402
C8713 0.1UF 20% 10V CERM 402
C8714 0.1UF 20% 10V CERM 402
C8715 0.1UF 20% 10V CERM 402
C8716 0.1UF 20% 10V CERM 402
C8717 0.1UF 20% 10V CERM 402
C8718 0.1UF 20% 10V CERM 402
C8719 0.1UF 20% 10V CERM 402
L8730 1.8UH 0805
=PP1V8_GPU
PP1V8_GPU_MPVDD
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C8730 4.7UF 20% 6.3V CERM 805
C8731 0.1UF 20% 10V CERM 402
XW8730 SM
GND_GPU_MPVSS
VOLTAGE=0V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
VDDR1
OMIT
U8400
RV370XT
BGA
(3 OF 5)
MEMORY INTERFACE A
DQA0 DQA1 DQA2 DQA3 DQA4 DQA5 DQA6 DQA7 DQA8 DQA9 DQA10 DQA11 DQA12 DQA13 DQA14 DQA15 DQA16 DQA17 DQA18 DQA19 DQA20 DQA21 DQA22 DQA23 DQA24 DQA25 DQA26 DQA27 DQA28 DQA29 DQA30 DQA31 DQA32 DQA33 DQA34 DQA35 DQA36 DQA37 DQA38 DQA39 DQA40 DQA41 DQA42 DQA43 DQA44 DQA45 DQA46 DQA47 DQA48 DQA49 DQA50 DQA51 DQA52 DQA53 DQA54 DQA55 DQA56 DQA57 DQA58 DQA59 DQA60 DQA61 DQA62 DQA63
VDDRH0 VDDRH1
VSSRH0 VSSRH1
MAA0 MAA1 MAA2 MAA3 MAA4 MAA5 MAA6 MAA7 MAA8 MAA9 MAA10 MAA11 MAA12 MAA13 MAA14
DQMA0* DQMA1* DQMA2* DQMA3* DQMA4* DQMA5* DQMA6* DQMA7*
QSA0 QSA1 QSA2 QSA3 QSA4 QSA5 QSA6 QSA7
RASA* CASA* WEA* CSA0* CSA1* CKEA
CLKA0 CLKA0* CLKA1 CLKA1*
MVREFD MVREFS
DIMA_0 DIMA_1
R8700 10K 5% 1/16W MF-LF 402
R8720 100 1% 1/16W MF-LF 402
R8721 100 1% 1/16W MF-LF 402
R8722 100 1% 1/16W MF-LF 402
R8723 100 1% 1/16W MF-LF 402
C8721 0.1UF 20% 10V CERM 402
C8723 0.1UF 20% 10V CERM 402
MPVDD MPVSS
DQB0 DQB1 DQB2 DQB3 DQB4 DQB5 DQB6 DQB7 DQB8 DQB9 DQB10 DQB11 DQB12 DQB13 DQB14 DQB15 DQB16 DQB17 DQB18 DQB19 DQB20 DQB21 DQB22 DQB23 DQB24 DQB25 DQB26 DQB27 DQB28 DQB29 DQB30 DQB31 DQB32 DQB33 DQB34 DQB35 DQB36 DQB37 DQB38 DQB39 DQB40 DQB41 DQB42 DQB43 DQB44 DQB45 DQB46 DQB47 DQB48 DQB49 DQB50 DQB51 DQB52 DQB53 DQB54 DQB55 DQB56 DQB57 DQB58 DQB59 DQB60 DQB61 DQB62 DQB63
VDDR1
OMIT
U8400
RV370XT
BGA
(4 OF 5)
MEMORY INTERFACE B
MAB0 MAB1 MAB2 MAB3 MAB4 MAB5 MAB6 MAB7 MAB8 MAB9 MAB10 MAB11 MAB12 MAB13 MAB14
DQMB0* DQMB1* DQMB2* DQMB3* DQMB4* DQMB5* DQMB6* DQMB7*
QSB0 QSB1 QSB2 QSB3 QSB4 QSB5 QSB6 QSB7
RASB* CASB* WEB* CSB0* CSB1* CKEB
CLKB0 CLKB0* CLKB1 CLKB1*
MEMVMODE0 MEMVMODE1 MEMTEST
DIMB_0 DIMB_1
R8701 10K 5% 1/16W MF-LF 402
R8724 4.7K 5% 1/16W MF-LF 402
R8725 4.7K 5% 1/16W MF-LF 402
R8726 4.7K 5% 1/16W MF-LF 402
R8727 4.7K 5% 1/16W MF-LF 402
R8728 47 1% 1/16W MF-LF 402
NOSTUFF
MEMVMODE 01
* 1.8V 01
2.5V 10
2.8V 11
GPU Frame Buffer
SYNC_MASTER=FINO-DD
SYNC_DATE=06/20/2005
NOTICE OF PROPRIETARY PROPERTY
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6790
REV. F
SCALE NONE
SHT 87 OF 154

FRAME BUFFER A TERMINATION

PLACE R'S CLOSE TO MEMORY

FBD<31>	22	3	6	RP8820	RFBD<31>
FBD<30>	22	4	5	RP8820	RFBD<30>
FBD<29>	22	1	8	RP8820	RFBD<29>
FBD<28>	22	2	7	RP8820	RFBD<28>
FBD<27>	22	3	6	RP8821	RFBD<27>
FBD<26>	22	4	5	RP8821	RFBD<26>
FBD<25>	22	2	7	RP8821	RFBD<25>
FBD<24>	22	1	8	RP8821	RFBD<24>
FBD<0>	22	1	8	RP8822	RFBD<0>
FBD<1>	22	2	7	RP8822	RFBD<1>
FBD<2>	22	4	5	RP8822	RFBD<2>
FBD<3>	22	3	6	RP8822	RFBD<3>
FBD<17>	22	1	8	RP8823	RFBD<17>
FBD<16>	22	2	7	RP8823	RFBD<16>
FBD<18>	22	3	6	RP8823	RFBD<18>
FBD<19>	22	4	5	RP8823	RFBD<19>
FBD<15>	22	4	5	RP8824	RFBD<15>
FBD<14>	22	3	6	RP8824	RFBD<14>
FBD<13>	22	2	7	RP8824	RFBD<13>
FBD<12>	22	1	8	RP8824	RFBD<12>
FBD<10>	22	3	6	RP8825	RFBD<10>
FBD<11>	22	4	5	RP8825	RFBD<11>
FBD<9>	22	1	8	RP8825	RFBD<9>
FBD<8>	22	2	7	RP8825	RFBD<8>
FBD<5>	22	2	7	RP8826	RFBD<5>
FBD<6>	22	3	6	RP8826	RFBD<6>
FBD<4>	22	1	8	RP8826	RFBD<4>
FBD<7>	22	4	5	RP8826	RFBD<7>
FBD<20>	22	1	8	RP8827	RFBD<20>
FBD<21>	22	2	7	RP8827	RFBD<21>
FBD<22>	22	3	6	RP8827	RFBD<22>
FBD<23>	22	4	5	RP8827	RFBD<23>

FBD<32>	22	3	6	RP8828	RFBD<32>
FBD<33>	22	4	5	RP8828	RFBD<33>
FBD<34>	22	2	7	RP8828	RFBD<34>
FBD<35>	22	1	8	RP8828	RFBD<35>
FBD<36>	22	4	5	RP8816	RFBD<36>
FBD<37>	22	3	6	RP8816	RFBD<37>
FBD<38>	22	2	7	RP8816	RFBD<38>
FBD<39>	22	1	8	RP8816	RFBD<39>
FBD<40>	22	3	6	RP8829	RFBD<40>
FBD<41>	22	4	5	RP8829	RFBD<41>
FBD<42>	22	2	7	RP8829	RFBD<42>
FBD<43>	22	1	8	RP8829	RFBD<43>
FBD<44>	22	4	5	RP8830	RFBD<44>
FBD<45>	22	3	6	RP8830	RFBD<45>
FBD<46>	22	1	8	RP8830	RFBD<46>
FBD<47>	22	2	7	RP8830	RFBD<47>
FBD<48>	22	4	5	RP8831	RFBD<48>
FBD<49>	22	2	7	RP8831	RFBD<49>
FBD<50>	22	3	6	RP8831	RFBD<50>
FBD<51>	22	1	8	RP8831	RFBD<51>
FBD<52>	22	3	6	RP8800	RFBD<52>
FBD<53>	22	4	5	RP8800	RFBD<53>
FBD<54>	22	2	7	RP8800	RFBD<54>
FBD<55>	22	1	8	RP8800	RFBD<55>
FBD<56>	22	4	5	RP8801	RFBD<56>
FBD<57>	22	3	6	RP8801	RFBD<57>
FBD<58>	22	1	8	RP8801	RFBD<58>
FBD<59>	22	2	7	RP8801	RFBD<59>
FBD<60>	22	4	5	RP8802	RFBD<60>
FBD<61>	22	2	7	RP8802	RFBD<61>
FBD<62>	22	3	6	RP8802	RFBD<62>
FBD<63>	22	1	8	RP8802	RFBD<63>

FBDQS<0>	22	R8800	RFBDQS<0>
FBDQS<1>	22	R8801	RFBDQS<1>
FBDQS<2>	22	R8802	RFBDQS<2>
FBDQS<3>	22	R8803	RFBDQS<3>
FBDQS<4>	22	R8804	RFBDQS<4>
FBDQS<5>	22	R8805	RFBDQS<5>
FBDQS<6>	22	R8806	RFBDQS<6>
FBDQS<7>	22	R8807	RFBDQS<7>

FBDQM<0>	22	R8830	RFBDQM<0>
FBDQM<1>	22	R8831	RFBDQM<1>
FBDQM<2>	22	R8832	RFBDQM<2>
FBDQM<3>	22	R8833	RFBDQM<3>
FBDQM<4>	22	R8834	RFBDQM<4>
FBDQM<5>	22	R8835	RFBDQM<5>
FBDQM<6>	22	R8836	RFBDQM<6>
FBDQM<7>	22	R8837	RFBDQM<7>

PLACE CLOCK TERMINATION AFTER MEMORY
GPU -> MEMORY -> TERMINATION

FBACLK0
R8820 56.2 1% 1/10W MF-LF 402
FBACLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8821 56.2 1% 1/10W MF-LF 402
C8821 0.01UF 20% 16V CERM 402
FBACLK0_L

FBACLK1
R8822 56.2 1% 1/10W MF-LF 402
FBACLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8823 56.2 1% 1/10W MF-LF 402
C8823 0.01UF 20% 16V CERM 402
FBACLK1_L

FRAME BUFFER B TERMINATION

FBD<64>	22	1	8	RP8810	RFBD<64>
FBD<65>	22	4	5	RP8810	RFBD<65>
FBD<66>	22	2	7	RP8810	RFBD<66>
FBD<67>	22	3	6	RP8810	RFBD<67>
FBD<84>	22	1	8	RP8809	RFBD<84>
FBD<85>	22	2	7	RP8809	RFBD<85>
FBD<86>	22	3	6	RP8809	RFBD<86>
FBD<87>	22	4	5	RP8809	RFBD<87>
FBD<72>	22	2	7	RP8819	RFBD<72>
FBD<73>	22	1	8	RP8819	RFBD<73>
FBD<75>	22	4	5	RP8819	RFBD<75>
FBD<74>	22	3	6	RP8819	RFBD<74>
FBD<68>	22	1	8	RP8808	RFBD<68>
FBD<70>	22	2	7	RP8808	RFBD<70>
FBD<69>	22	3	6	RP8808	RFBD<69>
FBD<71>	22	4	5	RP8808	RFBD<71>
FBD<80>	22	1	8	RP8807	RFBD<80>
FBD<81>	22	2	7	RP8807	RFBD<81>
FBD<82>	22	3	6	RP8807	RFBD<82>
FBD<83>	22	4	5	RP8807	RFBD<83>
FBD<76>	22	2	7	RP8817	RFBD<76>
FBD<77>	22	1	8	RP8817	RFBD<77>
FBD<78>	22	4	5	RP8817	RFBD<78>
FBD<79>	22	3	6	RP8817	RFBD<79>
FBD<91>	22	3	6	RP8818	RFBD<91>
FBD<90>	22	4	5	RP8818	RFBD<90>
FBD<89>	22	1	8	RP8818	RFBD<89>
FBD<88>	22	2	7	RP8818	RFBD<88>
FBD<95>	22	3	6	RP8803	RFBD<95>
FBD<94>	22	4	5	RP8803	RFBD<94>
FBD<93>	22	1	8	RP8803	RFBD<93>
FBD<92>	22	2	7	RP8803	RFBD<92>

FBD<96>	22	4	5	RP8815	RFBD<96>
FBD<97>	22	3	6	RP8815	RFBD<97>
FBD<98>	22	2	7	RP8815	RFBD<98>
FBD<99>	22	1	8	RP8815	RFBD<99>
FBD<100>	22	4	5	RP8814	RFBD<100>
FBD<101>	22	3	6	RP8814	RFBD<101>
FBD<102>	22	2	7	RP8814	RFBD<102>
FBD<103>	22	1	8	RP8814	RFBD<103>
FBD<104>	22	4	5	RP8812	RFBD<104>
FBD<105>	22	3	6	RP8812	RFBD<105>
FBD<106>	22	2	7	RP8812	RFBD<106>
FBD<107>	22	1	8	RP8812	RFBD<107>
FBD<108>	22	4	5	RP8813	RFBD<108>
FBD<109>	22	3	6	RP8813	RFBD<109>
FBD<110>	22	2	7	RP8813	RFBD<110>
FBD<111>	22	1	8	RP8813	RFBD<111>
FBD<112>	22	3	6	RP8811	RFBD<112>
FBD<113>	22	4	5	RP8811	RFBD<113>
FBD<114>	22	2	7	RP8811	RFBD<114>
FBD<115>	22	1	8	RP8811	RFBD<115>
FBD<116>	22	3	6	RP8806	RFBD<116>
FBD<117>	22	4	5	RP8806	RFBD<117>
FBD<118>	22	2	7	RP8806	RFBD<118>
FBD<119>	22	1	8	RP8806	RFBD<119>
FBD<120>	22	3	6	RP8804	RFBD<120>
FBD<121>	22	4	5	RP8804	RFBD<121>
FBD<122>	22	2	7	RP8804	RFBD<122>
FBD<123>	22	1	8	RP8804	RFBD<123>
FBD<124>	22	4	5	RP8805	RFBD<124>
FBD<125>	22	2	7	RP8805	RFBD<125>
FBD<126>	22	3	6	RP8805	RFBD<126>
FBD<127>	22	1	8	RP8805	RFBD<127>

FBDQS<8>	22	R8808	RFBDQS<8>
FBDQS<9>	22	R8809	RFBDQS<9>
FBDQS<10>	22	R8810	RFBDQS<10>
FBDQS<11>	22	R8811	RFBDQS<11>
FBDQS<12>	22	R8812	RFBDQS<12>
FBDQS<13>	22	R8813	RFBDQS<13>
FBDQS<14>	22	R8814	RFBDQS<14>
FBDQS<15>	22	R8815	RFBDQS<15>

FBDQM<8>	22	R8838	RFBDQM<8>
FBDQM<9>	22	R8839	RFBDQM<9>
FBDQM<10>	22	R8840	RFBDQM<10>
FBDQM<11>	22	R8841	RFBDQM<11>
FBDQM<12>	22	R8842	RFBDQM<12>
FBDQM<13>	22	R8843	RFBDQM<13>
FBDQM<14>	22	R8844	RFBDQM<14>
FBDQM<15>	22	R8845	RFBDQM<15>

FBBCLK0
R8824 56.2 1% 1/10W MF-LF 402
FBBCLK0_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8825 56.2 1% 1/10W MF-LF 402
C8825 0.01UF 20% 16V CERM 402
FBBCLK0_L

FBBCLK1
R8826 56.2 1% 1/10W MF-LF 402
FBBCLK1_TERM
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
R8827 56.2 1% 1/10W MF-LF 402
C8827 0.01UF 20% 16V CERM 402
FBBCLK1_L

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBD<127..0>		GPU_FB	GPU_FB	
RFBD<127..0>		GPU_FB	GPU_FB	
FBA<13..0>		GPU_FB	GPU_FB	
FBBA<13..0>		GPU_FB	GPU_FB	
FBDQM<15..0>		GPU_FB	GPU_FB	
FBDQS<15..0>		GPU_FB	GPU_FBDQS	
FBARAS_L		GPU_FB	GPU_FB	
FBACAS_L		GPU_FB	GPU_FB	
FBAWE_L		GPU_FB	GPU_FB	
FBACS0_L		GPU_FB	GPU_FB	
FBACKE		GPU_FB	GPU_FB	
FBBRAS_L		GPU_FB	GPU_FB	
FBBCAS_L		GPU_FB	GPU_FB	
FBBWE_L		GPU_FB	GPU_FB	
FBBCS0_L		GPU_FB	GPU_FB	
FBBCKE		GPU_FB	GPU_FB	

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
FBACLK0		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK0_L		GPU_FBCLK	GPU_FBCLK	FBACLK0
FBACLK1		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBACLK1_L		GPU_FBCLK	GPU_FBCLK	FBACLK1
FBBCLK0		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK0_L		GPU_FBCLK	GPU_FBCLK	FBBCLK0
FBBCLK1		GPU_FBCLK	GPU_FBCLK	FBBCLK1
FBBCLK1_L		GPU_FBCLK	GPU_FBCLK	FBBCLK1

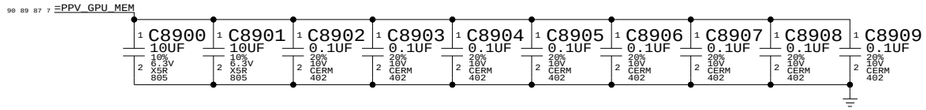
FB Series Termination

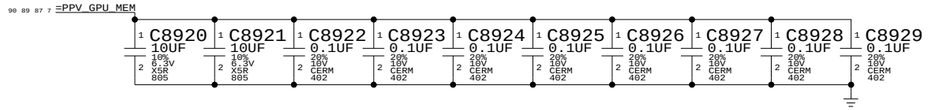
SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

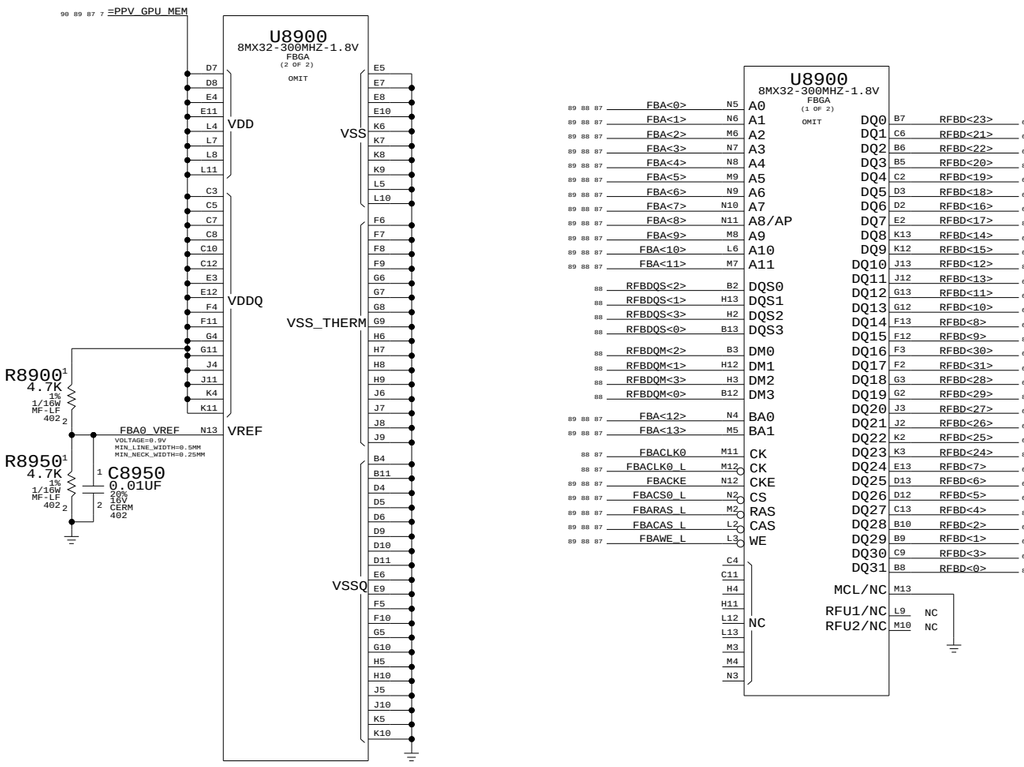
APPLE COMPUTER INC.

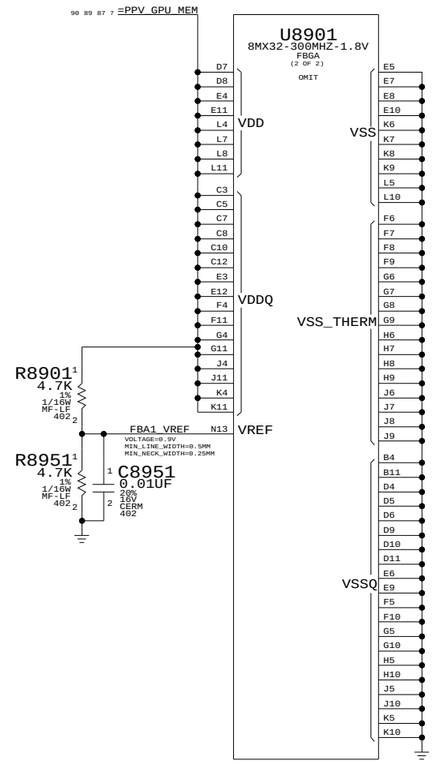
SIZE	DRAWING NUMBER	REV.
D	051-6790	F

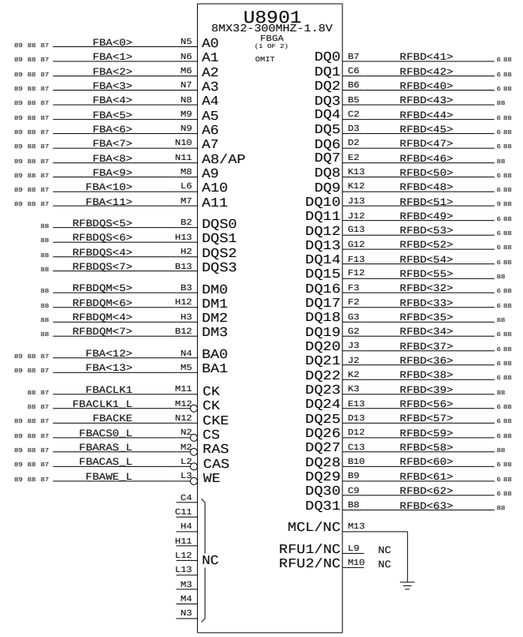
SCALE	SHT	OF
NONE	88	154

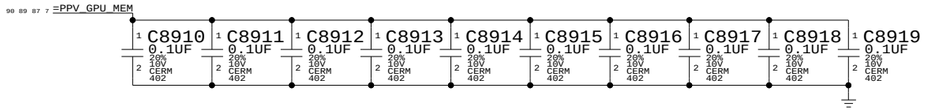


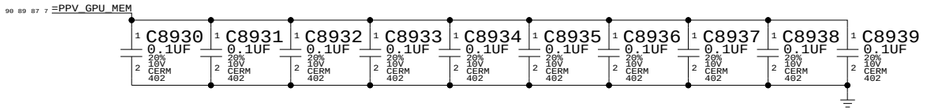




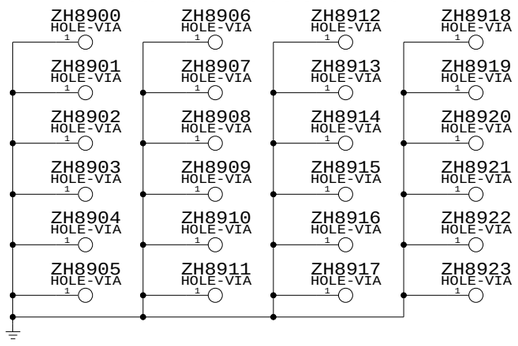








GROUND VIAS FOR SIGNAL LAYER TRANSITIONS



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U8900,U8901	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U8900,U8901	CRITICAL	FB128MB_350MHZ_HYN	

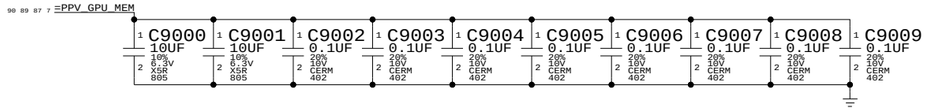
GPU GDDR SDRAM A

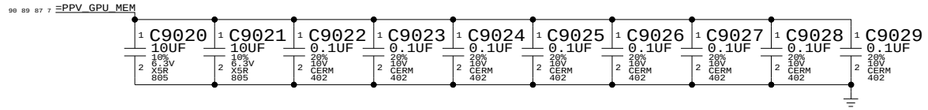
SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

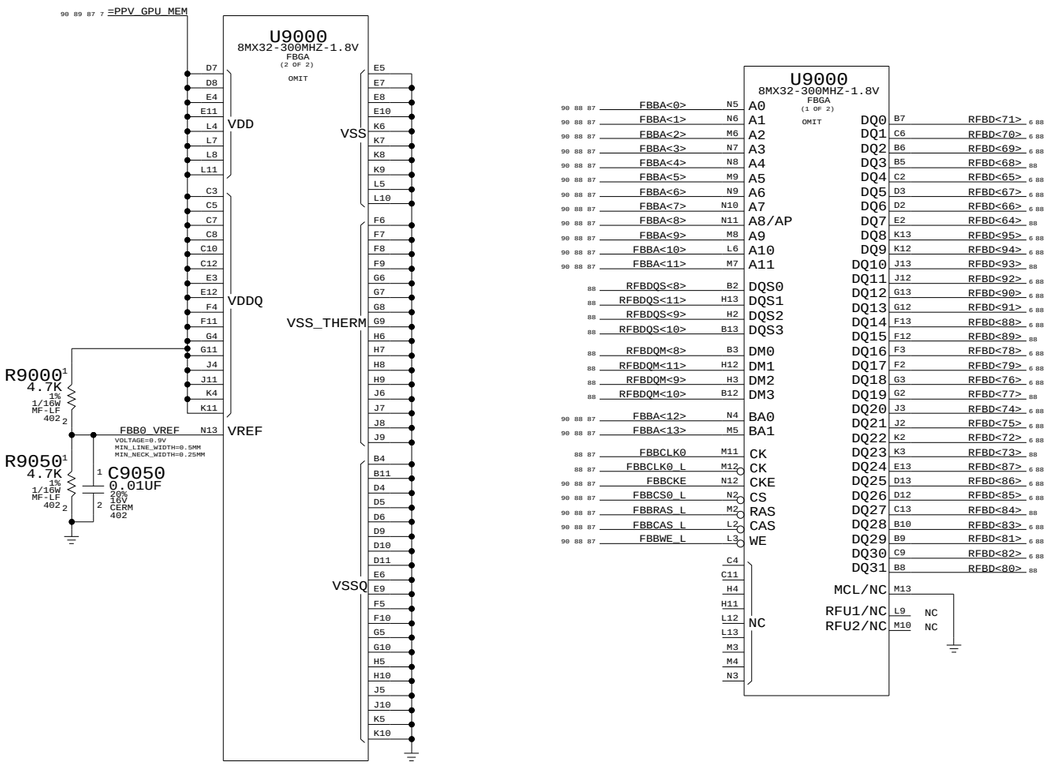
APPLE COMPUTER INC.

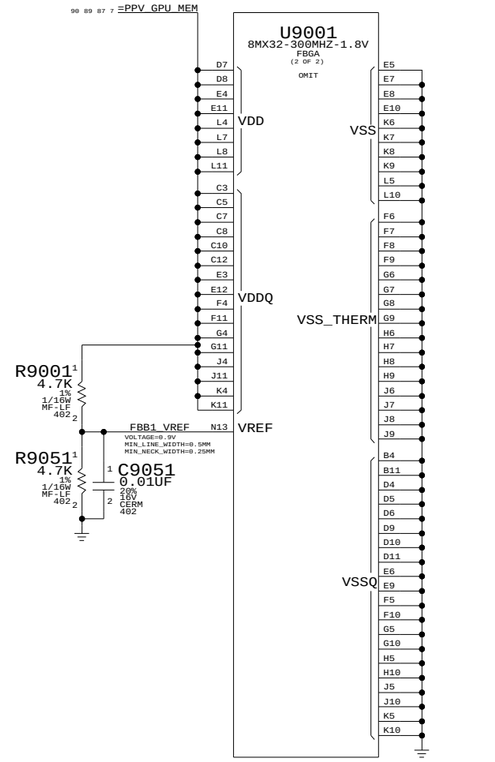
SIZE	DRAWING NUMBER	REV.
D	051-6790	F

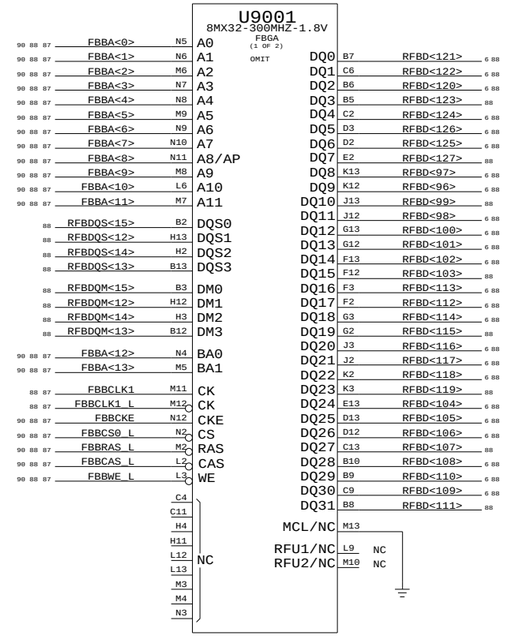
SCALE	SHT	OF
NONE	89	154

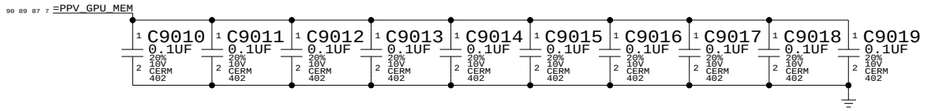


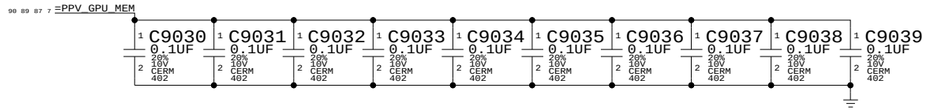


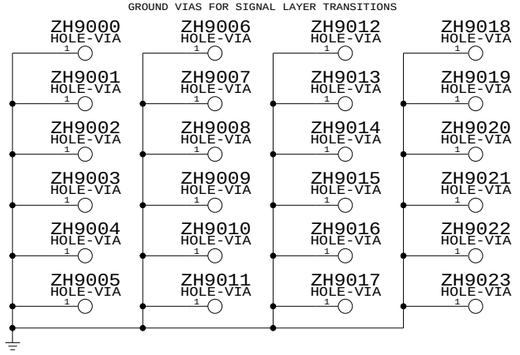












PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
333S0319	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB64MB_300MHZ_SAM	SAMSUNG
333S0311	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_300MHZ_SAM	
333S0312	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,SAM	U9000,U9001	CRITICAL	FB128MB_350MHZ_SAM	
333S0320	2	SDRAM,4MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB64MB_300MHZ_HYN	HYNIX
333S0314	2	SDRAM,8MX32,GDDR,300MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_300MHZ_HYN	
333S0315	2	SDRAM,8MX32,GDDR,350MHZ,1.8V,HYN	U9000,U9001	CRITICAL	FB128MB_350MHZ_HYN	

GPU GDDR SDRAM B

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

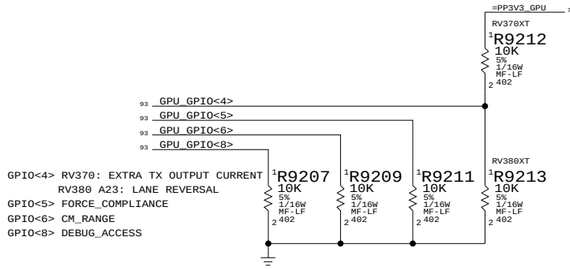
SIZE	DRAWING NUMBER	REV.
D	051-6790	F

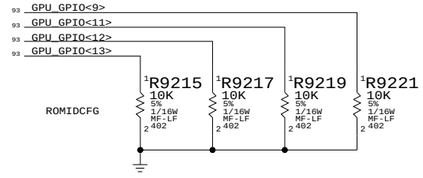
SCALE	SHT	OF
NONE	90	154

ATI STRAPS

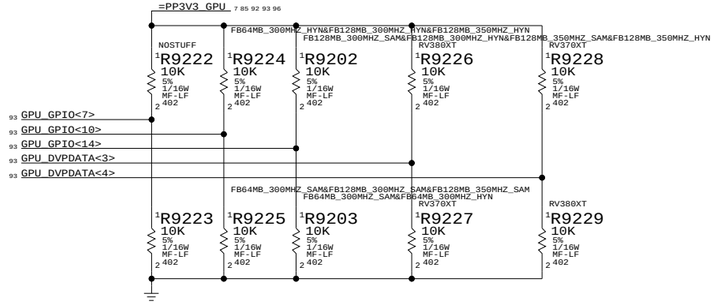
GPIO<1> TRANSMITTER DE-EMPHASIS (ACTIVE LOW)

GPIO<0> TRANSMITTER POWER SAVINGS
(FEATURE DOES NOT WORK - PULLED HIGH TO DISABLE)



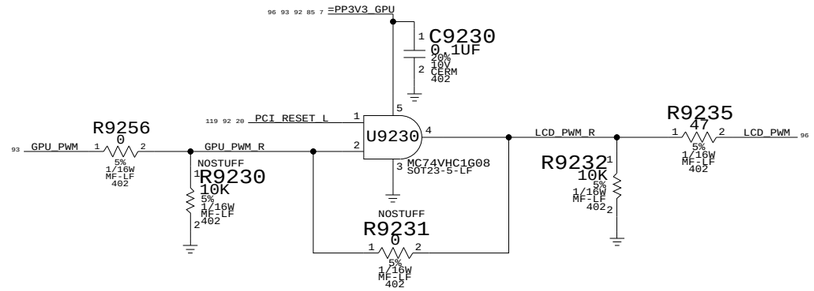


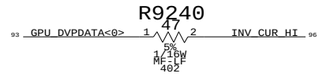
MEMORY STRAPS

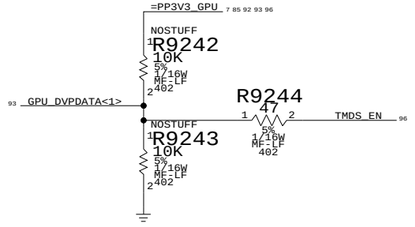


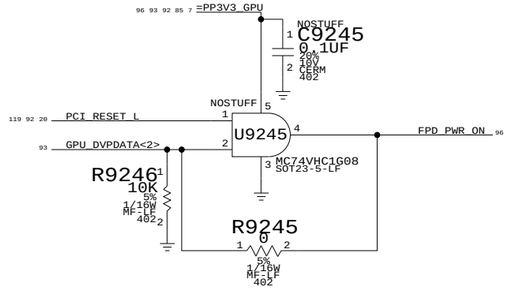
GPIO<7> - MEMORY DIE REVISION
  0 - ORIGINAL DIE REVISION
  1 - NEW (FUTURE) DIE REV
GPIO<10> - MEMORY VENDOR
  0 - SAMSUNG
  1 - HYNIX
GPIO<14> - MEMORY DENSITY
  0 - 4MX32
  1 - 8MX32
DVPDATA<3,4> - SPEED
  00 - 325E / 200M
  01 - 400E / 300M
  10 - 500E / 350M
  11 - RESERVED FOR FUTURE USE

APPLE GPIOS









GPU Straps

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 92 OF 154	

SPREAD SPECTRUM SUPPORT

S0=1;S1=M => -1.5% DOWN-SPREAD

27M OSC

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0176	1	OSC, XTAL, 27 MHZ, 30PPM	G9370	CRITICAL	

DIFFERENTIAL IMPEDANCE SHOULD BE 100 OHM

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TMDS_TCKM	GPU_TMDS	GPU_TMDS	TMDS_CK
	GPU_TMDS	GPU_TMDS	TMDS_CK
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D0
	GPU_TMDS	GPU_TMDS	TMDS_D0
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D1
	GPU_TMDS	GPU_TMDS	TMDS_D1
TMDS0	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_TMDS	GPU_TMDS	TMDS_D2
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
	GPU_VGA	GPU_VGA	
		I2C	
		I2C	
		I2C	
		I2C	

GPU THERMAL SENSOR

PLACE C9392 CLOSE TO TEMP SENSOR

PLACE R9373 CLOSE TO ATI PIN AH28

PLACE R9321-3 & FL9600-2 NEAR MINI-VGA CONNECTOR

ROUTE GND IN BETWEEN RGB SIGNALS WITH A VIA EVERY INCH

GPU DVI & DACs

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	93	154

INTERNAL LCD

NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
TCKP	GPU_TMDS	TCK
TCKM	GPU_TMDS	TCK
TD0P	GPU_TMDS	TD0
TD0M	GPU_TMDS	TD0
TD1P	GPU_TMDS	TD1
TD1M	GPU_TMDS	TD1
TD2P	GPU_TMDS	TD2
TD2M	GPU_TMDS	TD2

PLACE R9600-R9604, C9600 AS CLOSE TO GPU AS POSSIBLE

PLACE FILTER CLOSE TO TMDS CONNECTOR

TMDS_D2M — R9626 0 (NOSTUFF) — L9602 90-OHM — TD2M
TMDS_D2P — R9627 0 (NOSTUFF) — TD2P
R9604 332 1% 1/16W MF-LF 402

TMDS_D1M — R9628 0 (NOSTUFF) — L9608 90-OHM — TD1M
TMDS_D1P — R9629 0 (NOSTUFF) — TD1P
R9603 332 1% 1/16W MF-LF 402

TMDS_D0M — R9630 0 (NOSTUFF) — L9609 90-OHM — TD0M
TMDS_D0P — R9631 0 (NOSTUFF) — TD0P
R9602 332 1% 1/16W MF-LF 402

TMDS_CKM — R9632 0 (NOSTUFF) — L9610 90-OHM — TCKM
TMDS_CKP — R9633 0 (NOSTUFF) — TCKP
R9601 165 1% 1/16W MF-LF 402
C9600 22PF 5% 50V CERM 402
R9600 165 1% 1/16W MF-LF 402
TMDS_CK_TERM: MIN_LINE_WIDTH=0.3MM, MIN_NECK_WIDTH=0.2MM

=PP3V3_GPU — R9605 2.0K 5% 1/16W MF-LF 402 — R9607 2.0K 5% 1/16W MF-LF 402 — R9682 0 5% 1/8W MF-LF 805 — PP3V3_DDC
C9601 0.01UF 10% 16V CERM 402
I2C_GPU_TMDS_SCL — R9608 33 5% 1/16W MF-LF 402 — I2C_TMDS_SCL
I2C_GPU_TMDS_SDA — R9606 33 5% 1/16W MF-LF 402 — I2C_TMDS_SDA

INTERNAL TMDS CONNECTOR

SDF9600 STDOFF-3MMOD4.6MMH-1.35-TH — GND_CHASSIS_TMDS0
(516S0241) CRITICAL — C9620 0.01UF 10% 16V CERM 402
J9602 53307-3072 F-ST-SM
PPVCC_TMDS
PP3V3_DDC — VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5MM, MIN_NECK_WIDTH=0.25MM
TD0M, TD0P, TD2M, TD2P, I2C_TMDS_SDA
TCKM, TCKP, TD1M, TD1P, I2C_TMDS_SCL
C9616 10UF 10% 6.3V X5R 805
C9615 0.01UF 10% 16V CERM 402
SDF9601 STDOFF-3MMOD4.6MMH-1.35-TH — GND_CHASSIS_TMDS1
C9621 0.01UF 10% 16V CERM 402

PANEL POWER SEQUENCING

=PP3V3_GPU — Q9600 IRF7410PBF SO-8 (NOSTUFF) — 376S0337
=PP3V3_GPU — R9634 0 5% 1/4W MF-LF 1206
C9610 0.01UF 20% 16V CERM 402 (NOSTUFF)
R9625 100K 5% 1/16W MF-LF 402 (NOSTUFF)
C9618 0.022UF 20% 16V CERM 402 (NOSTUFF)
FPD_PWR_SW_G
PPVCC_TMDS — VOLTAGE=3.3V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
R9613 10K 5% 1/16W MF-LF 402 (NOSTUFF)
D9614 MMBD914XXG SOT23
C9617 10UF 10% 6.3V X5R 805
R9660 10K 5% 1/16W MF-LF 402 (NOSTUFF)
FPD_PWR_ON_D
FPD_PWR_ON — Q9601 2N7002 SOT23-LF (NOSTUFF)
TMDS_EN_R — R9614 10K 5% 1/16W MF-LF 402 — TMDS_EN

INVERTER INTERFACE

U9670 74LC125 — FPD_PWR_ON — LED5900_PWR — R9612 820 5% 1/10W MF-LF 603 — LED5900_P1 — LED9600 GREEN-3.6MCD 2.0X1.25MM-SM
SILKSCREEN: 3

=PP12V_GPU — C9642 1UF 20% 25V CERM 805 — CRITICAL J9601 87437-0443-BLK M-ST-SM
LCD_PWM
INV_CUR_HI
518S0331

EXTERNAL VGA CONNECTOR

NET_PHYSICAL_TYPE	NET_SPACING_TYPE
FILT_ANALOG_GRN	GPU_VGA
ANALOG_GRN_LC	GPU_VGA
ANALOG_GRN_LCL	GPU_VGA
FILT_ANALOG_RED	GPU_VGA
ANALOG_RED_LC	GPU_VGA
ANALOG_RED_LCL	GPU_VGA
FILT_ANALOG_BLU	GPU_VGA
ANALOG_BLU_LC	GPU_VGA
ANALOG_BLU_LCL	GPU_VGA
VGA_VSYNC	GPU_VGA
VGA_VSYNC_R	GPU_VGA
VGA_HSYNC	GPU_VGA
VGA_HSYNC_R	GPU_VGA

PP5V_USB2 — R9680 0 5% 1/8W MF-LF 805 — PP5V_VGA VOLTAGE=5V, MIN_LINE_WIDTH=0.6MM, MIN_NECK_WIDTH=0.25MM
C9602 0.01UF 10% 16V CERM 402
GND_CHASSIS_VGA

=PP3V3_GPU — C9670 0.1UF 20% 10V CERM 402
U9670 74LC125 CRITICAL 125 TSSOP
ANALOG_VSYNC — R9671 33 5% 1/16W MF-LF 402 — VGA_VSYNC_R
U9670 74LC125 125 TSSOP
ANALOG_HSYNC — R9672 33 5% 1/16W MF-LF 402 — VGA_HSYNC_R
C9607 22PF 5% 50V CERM 402 (NOSTUFF)
C9608 22PF 5% 50V CERM 402 (NOSTUFF)
GND_CHASSIS_VGA

=PP3V3_GPU — R9673 10K 5% 1/16W MF-LF 402 — R9674 10K 5% 1/16W MF-LF 402
Q9675 2N7002DW-X-F SOT-363
I2C_GPU_MON_SCL — R9675 100 5% 1/16W MF-LF 402 — I2C_MON_SCL_R
I2C_GPU_MON_SDA — R9676 100 5% 1/16W MF-LF 402 — I2C_MON_SDA_R
PP5V_VGA — R9677 4.7K 5% 1/16W MF-LF 402 — R9678 4.7K 5% 1/16W MF-LF 402
C9677 47PF 5% 50V CERM 402 — C9678 47PF 5% 50V CERM 402
GND_CHASSIS_VGA

INDUCTORS SHOULD BE 47 NH
ANY ~8PF CAP SHOULD DO

ANALOG_RED — L9640 47NH-0.20-OHM 0805 — ANALOG_RED_LC — C9640 8.2PF +/-0.25PF 50V CERM 402
L9641 47NH-0.20-OHM 0805 — NOSTUFF FL9600 LCFILTER SM-220MHZ-LF — R9640 0 — ANALOG_RED_LCL
R9643 301 1% 1/16W MF-LF 402

ANALOG_GRN — L9642 47NH-0.20-OHM 0805 — ANALOG_GRN_LC — C9643 8.2PF +/-0.25PF 50V CERM 402
L9643 47NH-0.20-OHM 0805 — NOSTUFF FL9601 LCFILTER SM-220MHZ-LF — R9641 0 — ANALOG_GRN_LCL
R9644 301 1% 1/16W MF-LF 402

ANALOG_BLU — L9644 47NH-0.20-OHM 0805 — ANALOG_BLU_LC — C9644 8.2PF +/-0.25PF 50V CERM 402
L9645 47NH-0.20-OHM 0805 — NOSTUFF FL9602 LCFILTER SM-220MHZ-LF — R9642 0 — ANALOG_BLU_LCL
R9645 301 1% 1/16W MF-LF 402

PLACE R9321-3 & FL9600-2 CLOSE TO J9603

M23: 514S0089

CRITICAL J9603 MINI-VGA F-ST-SM
NC — PIN 15 NC REQUESTED BY EMC
VGA_HSYNC_R, FILT_ANALOG_RED, FILT_ANALOG_GRN, FILT_ANALOG_BLU, I2C_MON_SCL_R, MON_DETECT
VGA_VSYNC_R, (RED_RTN), (GRN_RTN), PP5V_VGA, I2C_MON_SDA_R, (BLU_RTN)
C9605 0.01UF 10% 16V CERM 402
C9604 0.01UF 10% 16V CERM 402
C9603 0.01UF 10% 16V CERM 402
GND_CHASSIS_VGA

TMDS/Inverter/ExtVGA

SYNC_MASTER=M23-DD SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 96 OF 154	

KODIAK PCI-E PHYSICAL CONSTRAINT TABLE

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
100M_N<0>		CLK_100M	PCIE_CLK	PCIE_CLK
100M_P<0>		CLK_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_N<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_P<0>		CLK_KODPCIE_100M	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_NF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
CLK_KOD_100M_PF<0>		CLK_KODPCIE_100MF	PCIE_CLK	PCIE_CLK
PCIE_NB_TO_SLOTA_NF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<0>	PCIE_NB2SA0	PCIE_NB_TO_SLOTA_0_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<1>	PCIE_NB2SA1	PCIE_NB_TO_SLOTA_1_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<2>	PCIE_NB2SA2	PCIE_NB_TO_SLOTA_2_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<3>	PCIE_NB2SA3	PCIE_NB_TO_SLOTA_3_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<4>	PCIE_NB2SA4	PCIE_NB_TO_SLOTA_4_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<5>	PCIE_NB2SA5	PCIE_NB_TO_SLOTA_5_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<6>	PCIE_NB2SA6	PCIE_NB_TO_SLOTA_6_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<7>	PCIE_NB2SA7	PCIE_NB_TO_SLOTA_7_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<8>	PCIE_NB2SA8	PCIE_NB_TO_SLOTA_8_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<9>	PCIE_NB2SA9	PCIE_NB_TO_SLOTA_9_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<10>	PCIE_NB2SA10	PCIE_NB_TO_SLOTA_10_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<11>	PCIE_NB2SA11	PCIE_NB_TO_SLOTA_11_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<12>	PCIE_NB2SA12	PCIE_NB_TO_SLOTA_12_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<13>	PCIE_NB2SA13	PCIE_NB_TO_SLOTA_13_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<14>	PCIE_NB2SA14	PCIE_NB_TO_SLOTA_14_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_NF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_PF<15>	PCIE_NB2SA15	PCIE_NB_TO_SLOTA_15_F	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<0>		PCIE_NB_TO_SLOTA_0	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<1>		PCIE_NB_TO_SLOTA_1	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<2>		PCIE_NB_TO_SLOTA_2	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<3>		PCIE_NB_TO_SLOTA_3	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<4>		PCIE_NB_TO_SLOTA_4	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<5>		PCIE_NB_TO_SLOTA_5	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<6>		PCIE_NB_TO_SLOTA_6	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<7>		PCIE_NB_TO_SLOTA_7	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<8>		PCIE_NB_TO_SLOTA_8	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<9>		PCIE_NB_TO_SLOTA_9	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<10>		PCIE_NB_TO_SLOTA_10	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<11>		PCIE_NB_TO_SLOTA_11	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<12>		PCIE_NB_TO_SLOTA_12	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<13>		PCIE_NB_TO_SLOTA_13	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<14>		PCIE_NB_TO_SLOTA_14	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_N<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA
PCIE_NB_TO_SLOTA_P<15>		PCIE_NB_TO_SLOTA_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E POWER PHYSICAL CONSTRAINT TABLE

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
KOD_G10_GND	0.3MM	0.25MM	0
KOD_H05_GND	0.3MM	0.25MM	0
KOD_H08_GND	0.3MM	0.25MM	0
KOD_J13_GND	0.3MM	0.25MM	0
KOD_K07_GND	0.3MM	0.25MM	0
KOD_L13_GND	0.3MM	0.25MM	0
PWR_PCIE_A_AVDD	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_1	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_A	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_B	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_C	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_2	0.3MM	0.25MM	1.2
PWR_PCIE_A_AVDD_0	0.3MM	0.25MM	1.2

SIG_NAME	ELECTRICAL_CONSTRAINT_SET	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
CLK_PCIE_SLOTA_N<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_P<0>		KODPCIE_CLK	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_NF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CLK_PCIE_SLOTA_PF<0>		KODPCIE_CLKF	PCIE_CLK	PCIE_CLK
CKA_P<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
CKA_N<0>		CLK_SLOTA_CKA	PCIE_CLK	PCIE_CLK
PCIE_SLOTA_TO_NB_NF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<0>	PCIE_SA2NB0	PCIE_SLOTA_TO_NB_0_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<1>	PCIE_SA2NB1	PCIE_SLOTA_TO_NB_1_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<2>	PCIE_SA2NB2	PCIE_SLOTA_TO_NB_2_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<3>	PCIE_SA2NB3	PCIE_SLOTA_TO_NB_3_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<4>	PCIE_SA2NB4	PCIE_SLOTA_TO_NB_4_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<5>	PCIE_SA2NB5	PCIE_SLOTA_TO_NB_5_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<6>	PCIE_SA2NB6	PCIE_SLOTA_TO_NB_6_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<7>	PCIE_SA2NB7	PCIE_SLOTA_TO_NB_7_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<8>	PCIE_SA2NB8	PCIE_SLOTA_TO_NB_8_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<9>	PCIE_SA2NB9	PCIE_SLOTA_TO_NB_9_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<10>	PCIE_SA2NB10	PCIE_SLOTA_TO_NB_10_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<11>	PCIE_SA2NB11	PCIE_SLOTA_TO_NB_11_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<12>	PCIE_SA2NB12	PCIE_SLOTA_TO_NB_12_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<13>	PCIE_SA2NB13	PCIE_SLOTA_TO_NB_13_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<14>	PCIE_SA2NB14	PCIE_SLOTA_TO_NB_14_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_NF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_PF<15>	PCIE_SA2NB15	PCIE_SLOTA_TO_NB_15_F	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<0>		PCIE_SLOTA_TO_NB_0	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<1>		PCIE_SLOTA_TO_NB_1	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<2>		PCIE_SLOTA_TO_NB_2	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<3>		PCIE_SLOTA_TO_NB_3	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<4>		PCIE_SLOTA_TO_NB_4	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<5>		PCIE_SLOTA_TO_NB_5	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<6>		PCIE_SLOTA_TO_NB_6	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<7>		PCIE_SLOTA_TO_NB_7	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<8>		PCIE_SLOTA_TO_NB_8	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<9>		PCIE_SLOTA_TO_NB_9	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<10>		PCIE_SLOTA_TO_NB_10	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<11>		PCIE_SLOTA_TO_NB_11	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<12>		PCIE_SLOTA_TO_NB_12	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<13>		PCIE_SLOTA_TO_NB_13	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<14>		PCIE_SLOTA_TO_NB_14	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_N<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA
PCIE_SLOTA_TO_NB_P<15>		PCIE_SLOTA_TO_NB_15	PCIE_DATA	PCIE_DATA

KODIAK PCI-E CONST

SYNC_MASTER=FINO-DD SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

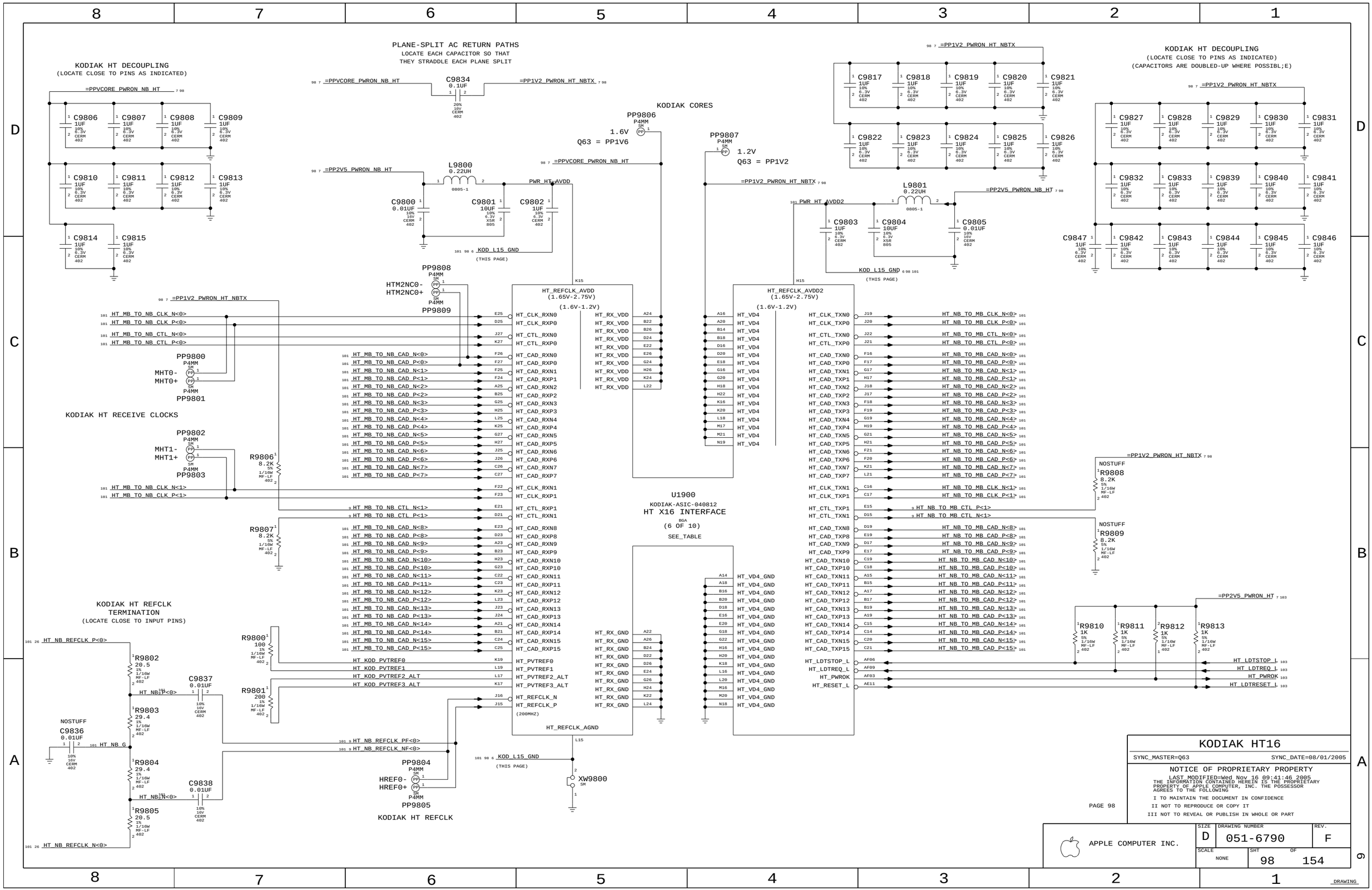
II NOT TO REPRODUCE OR COPY IT

III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	97	154


KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
=PPVCORE_PWRON_NB_HT
C9806 1UF 10% 6.3V CERM 402
C9807 1UF 10% 6.3V CERM 402
C9808 1UF 10% 6.3V CERM 402
C9809 1UF 10% 6.3V CERM 402
C9810 1UF 10% 6.3V CERM 402
C9811 1UF 10% 6.3V CERM 402
C9812 1UF 10% 6.3V CERM 402
C9813 1UF 10% 6.3V CERM 402
C9814 1UF 10% 6.3V CERM 402
C9815 1UF 10% 6.3V CERM 402
PLANE-SPLIT AC RETURN PATHS
LOCATE EACH CAPACITOR SO THAT
THEY STRADDLE EACH PLANE SPLIT
=PPVCORE_PWRON_NB_HT
C9834 0.1UF 20% 16V CERM 402
=PP1V2_PWRON_HT_NBTX
KODIAK CORES
PP9806 P4MM SM
1.6V
Q63 = PP1V6
=PP2V5_PWRON_NB_HT
L9800 0.22UH 0805-1
PWR_HT_AVDD
C9800 0.01UF 10% 16V CERM 402
C9801 10UF 10% 6.3V X5R 805
C9802 1UF 10% 6.3V CERM 402
KOD_L15_GND
(THIS PAGE)
PP9808 P4MM SM
HTM2NC0-
HTM2NC0+
PP9809 P4MM SM
K15
HT_REFCLK_AVDD
(1.65V-2.75V)
(1.6V-1.2V)
HT_CLK_RXN0
HT_CLK_RXP0
HT_CTL_RXN0
HT_CTL_RXP0
HT_CAD_RXN0
HT_CAD_RXP0
HT_CAD_RXN1
HT_CAD_RXP1
HT_CAD_RXN2
HT_CAD_RXP2
HT_CAD_RXN3
HT_CAD_RXP3
HT_CAD_RXN4
HT_CAD_RXP4
HT_CAD_RXN5
HT_CAD_RXP5
HT_CAD_RXN6
HT_CAD_RXP6
HT_CAD_RXN7
HT_CAD_RXP7
HT_CLK_RXN1
HT_CLK_RXP1
HT_CTL_RXP1
HT_CTL_RXN1
HT_CAD_RXN8
HT_CAD_RXP8
HT_CAD_RXN9
HT_CAD_RXP9
HT_CAD_RXN10
HT_CAD_RXP10
HT_CAD_RXN11
HT_CAD_RXP11
HT_CAD_RXN12
HT_CAD_RXP12
HT_CAD_RXN13
HT_CAD_RXP13
HT_CAD_RXN14
HT_CAD_RXP14
HT_CAD_RXN15
HT_CAD_RXP15
HT_PVTREF0
HT_PVTREF1
HT_PVTREF2_ALT
HT_PVTREF3_ALT
HT_REFCLK_N
HT_REFCLK_P
(200MHZ)
HT_RX_VDD
HT_RX_GND
HT_REFCLK_AGND
L15
KOD_L15_GND
(THIS PAGE)
XW9800 SM
PP9804 P4MM SM
HREF0-
HREF0+
PP9805 P4MM SM
KODIAK HT REFCLK
PP9807 P4MM SM
1.2V
Q63 = PP1V2
=PP1V2_PWRON_HT_NBTX
L9801 0.22UH 0805-1
PWR_HT_AVDD2
=PP2V5_PWRON_NB_HT
C9803 1UF 10% 6.3V CERM 402
C9804 10UF 10% 6.3V X5R 805
C9805 0.01UF 10% 16V CERM 402
KOD_L15_GND
(THIS PAGE)
H15
HT_REFCLK_AVDD2
(1.65V-2.75V)
(1.6V-1.2V)
HT_VD4
HT_VD4_GND
U1900
KODIAK-ASIC-040812
HT X16 INTERFACE
BGA
(6 OF 10)
SEE_TABLE
HT_CLK_TXN0
HT_CLK_TXP0
HT_CTL_TXN0
HT_CTL_TXP0
HT_CAD_TXN0
HT_CAD_TXP0
HT_CAD_TXN1
HT_CAD_TXP1
HT_CAD_TXN2
HT_CAD_TXP2
HT_CAD_TXN3
HT_CAD_TXP3
HT_CAD_TXN4
HT_CAD_TXP4
HT_CAD_TXN5
HT_CAD_TXP5
HT_CAD_TXN6
HT_CAD_TXP6
HT_CAD_TXN7
HT_CAD_TXP7
HT_CLK_TXN1
HT_CLK_TXP1
HT_CTL_TXP1
HT_CTL_TXN1
HT_CAD_TXN8
HT_CAD_TXP8
HT_CAD_TXN9
HT_CAD_TXP9
HT_CAD_TXN10
HT_CAD_TXP10
HT_CAD_TXN11
HT_CAD_TXP11
HT_CAD_TXN12
HT_CAD_TXP12
HT_CAD_TXN13
HT_CAD_TXP13
HT_CAD_TXN14
HT_CAD_TXP14
HT_CAD_TXN15
HT_CAD_TXP15
HT_LDTSTOP_L
HT_LDTREQ_L
HT_PWROK
HT_RESET_L
C9817 1UF 10% 6.3V CERM 402
C9818 1UF 10% 6.3V CERM 402
C9819 1UF 10% 6.3V CERM 402
C9820 1UF 10% 6.3V CERM 402
C9821 1UF 10% 6.3V CERM 402
C9822 1UF 10% 6.3V CERM 402
C9823 1UF 10% 6.3V CERM 402
C9824 1UF 10% 6.3V CERM 402
C9825 1UF 10% 6.3V CERM 402
C9826 1UF 10% 6.3V CERM 402
KODIAK HT DECOUPLING
(LOCATE CLOSE TO PINS AS INDICATED)
(CAPACITORS ARE DOUBLED-UP WHERE POSSIBL;E)
=PP1V2_PWRON_HT_NBTX
C9827 1UF 10% 6.3V CERM 402
C9828 1UF 10% 6.3V CERM 402
C9829 1UF 10% 6.3V CERM 402
C9830 1UF 10% 6.3V CERM 402
C9831 1UF 10% 6.3V CERM 402
C9832 1UF 10% 6.3V CERM 402
C9833 1UF 10% 6.3V CERM 402
C9839 1UF 10% 6.3V CERM 402
C9840 1UF 10% 6.3V CERM 402
C9841 1UF 10% 6.3V CERM 402
C9847 1UF 10% 6.3V CERM 402
C9842 1UF 10% 6.3V CERM 402
C9843 1UF 10% 6.3V CERM 402
C9844 1UF 10% 6.3V CERM 402
C9845 1UF 10% 6.3V CERM 402
C9846 1UF 10% 6.3V CERM 402
KODIAK HT RECEIVE CLOCKS
PP9802 P4MM SM
MHT1-
MHT1+
PP9803 P4MM SM
PP9801 P4MM SM
MHT0-
MHT0+
PP9800 P4MM SM
HT_MB_TO_NB_CLK_N<0>
HT_MB_TO_NB_CLK_P<0>
HT_MB_TO_NB_CTL_N<0>
HT_MB_TO_NB_CTL_P<0>
HT_MB_TO_NB_CAD_N<0>
HT_MB_TO_NB_CAD_P<0>
HT_MB_TO_NB_CAD_N<1>
HT_MB_TO_NB_CAD_P<1>
HT_MB_TO_NB_CAD_N<2>
HT_MB_TO_NB_CAD_P<2>
HT_MB_TO_NB_CAD_N<3>
HT_MB_TO_NB_CAD_P<3>
HT_MB_TO_NB_CAD_N<4>
HT_MB_TO_NB_CAD_P<4>
HT_MB_TO_NB_CAD_N<5>
HT_MB_TO_NB_CAD_P<5>
HT_MB_TO_NB_CAD_N<6>
HT_MB_TO_NB_CAD_P<6>
HT_MB_TO_NB_CAD_N<7>
HT_MB_TO_NB_CAD_P<7>
HT_MB_TO_NB_CLK_N<1>
HT_MB_TO_NB_CLK_P<1>
HT_MB_TO_NB_CTL_N<1>
HT_MB_TO_NB_CTL_P<1>
HT_MB_TO_NB_CAD_N<8>
HT_MB_TO_NB_CAD_P<8>
HT_MB_TO_NB_CAD_N<9>
HT_MB_TO_NB_CAD_P<9>
HT_MB_TO_NB_CAD_N<10>
HT_MB_TO_NB_CAD_P<10>
HT_MB_TO_NB_CAD_N<11>
HT_MB_TO_NB_CAD_P<11>
HT_MB_TO_NB_CAD_N<12>
HT_MB_TO_NB_CAD_P<12>
HT_MB_TO_NB_CAD_N<13>
HT_MB_TO_NB_CAD_P<13>
HT_MB_TO_NB_CAD_N<14>
HT_MB_TO_NB_CAD_P<14>
HT_MB_TO_NB_CAD_N<15>
HT_MB_TO_NB_CAD_P<15>
R9806 8.2K 5% 1/16W MF-LF 402
R9807 8.2K 5% 1/16W MF-LF 402
R9800 100 1% 1/16W MF-LF 402
R9801 200 1% 1/16W MF-LF 402
KODIAK HT REFCLK TERMINATION
(LOCATE CLOSE TO INPUT PINS)
HT_NB_REFCLK_P<0>
HT_NB_REFCLK_N<0>
R9802 20.5 1% 1/16W MF-LF 402
R9803 29.4 1% 1/16W MF-LF 402
R9804 29.4 1% 1/16W MF-LF 402
R9805 20.5 1% 1/16W MF-LF 402
C9837 0.01UF 10% 16V CERM 402
C9838 0.01UF 10% 16V CERM 402
NOSTUFF
C9836 0.01UF 10% 16V CERM 402
HT_NB_G
HT_NB_TO_NB_REFCLK_PF<0>
HT_NB_TO_NB_REFCLK_NF<0>
HT_NB_TO_MB_CLK_N<0>
HT_NB_TO_MB_CLK_P<0>
HT_NB_TO_MB_CTL_N<0>
HT_NB_TO_MB_CTL_P<0>
HT_NB_TO_MB_CAD_N<0>
HT_NB_TO_MB_CAD_P<0>
HT_NB_TO_MB_CAD_N<1>
HT_NB_TO_MB_CAD_P<1>
HT_NB_TO_MB_CAD_N<2>
HT_NB_TO_MB_CAD_P<2>
HT_NB_TO_MB_CAD_N<3>
HT_NB_TO_MB_CAD_P<3>
HT_NB_TO_MB_CAD_N<4>
HT_NB_TO_MB_CAD_P<4>
HT_NB_TO_MB_CAD_N<5>
HT_NB_TO_MB_CAD_P<5>
HT_NB_TO_MB_CAD_N<6>
HT_NB_TO_MB_CAD_P<6>
HT_NB_TO_MB_CAD_N<7>
HT_NB_TO_MB_CAD_P<7>
HT_NB_TO_MB_CLK_N<1>
HT_NB_TO_MB_CLK_P<1>
HT_NB_TO_MB_CTL_P<1>
HT_NB_TO_MB_CTL_N<1>
HT_NB_TO_MB_CAD_N<8>
HT_NB_TO_MB_CAD_P<8>
HT_NB_TO_MB_CAD_N<9>
HT_NB_TO_MB_CAD_P<9>
HT_NB_TO_MB_CAD_N<10>
HT_NB_TO_MB_CAD_P<10>
HT_NB_TO_MB_CAD_N<11>
HT_NB_TO_MB_CAD_P<11>
HT_NB_TO_MB_CAD_N<12>
HT_NB_TO_MB_CAD_P<12>
HT_NB_TO_MB_CAD_N<13>
HT_NB_TO_MB_CAD_P<13>
HT_NB_TO_MB_CAD_N<14>
HT_NB_TO_MB_CAD_P<14>
HT_NB_TO_MB_CAD_N<15>
HT_NB_TO_MB_CAD_P<15>
=PP1V2_PWRON_HT_NBTX
R9808 8.2K 5% 1/16W MF-LF 402
NOSTUFF
R9809 8.2K 5% 1/16W MF-LF 402
=PP2V5_PWRON_HT
R9810 1K 5% 1/16W MF-LF 402
R9811 1K 5% 1/16W MF-LF 402
R9812 1K 5% 1/16W MF-LF 402
R9813 1K 5% 1/16W MF-LF 402
HT_LDTSTOP_L
HT_LDTREQ_L
HT_PWROK
HT_LDTRESET_L
KODIAK HT16
SYNC_MASTER=Q63
SYNC_DATE=08/01/2005
NOTICE OF PROPRIETARY PROPERTY
LAST_MODIFIED=Wed Nov 16 09:41:46 2005
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
PAGE 98
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6790
REV. F
SCALE NONE
SHT 98 OF 154
DRAWING

SIG_NAME	MAKE_BASE	DIFFERENTIAL_PAIR	EC_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE
HT_NB_TO_MB_CLK_N<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CLK_P<0>	TRUE	HT_NB_TO_SB_CLK	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CLK
HT_NB_TO_MB_CAD_N<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<0>	TRUE	HT_NB_TO_SB_CAD0	HT_NB_TO_SB_PP	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<1>	TRUE	HT_NB_TO_SB_CAD1	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<2>	TRUE	HT_NB_TO_SB_CAD2	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<3>	TRUE	HT_NB_TO_SB_CAD3	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<4>	TRUE	HT_NB_TO_SB_CAD4	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<5>	TRUE	HT_NB_TO_SB_CAD5	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<6>	TRUE	HT_NB_TO_SB_CAD6	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_N<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CAD_P<7>	TRUE	HT_NB_TO_SB_CAD7	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_N<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_NB_TO_MB_CTL_P<0>	TRUE	HT_NB_TO_SB_CTL0	HT_NB_TO_SB	HT_CAD	HT_NB_TO_SB_CAD
HT_MB_TO_NB_CLK_N<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CLK_P<0>	TRUE	HT_SB_TO_NB_CLK	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CLK
HT_MB_TO_NB_CAD_N<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<0>	TRUE	HT_SB_TO_NB_CAD0	HT_SB_TO_NB_PP	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<1>	TRUE	HT_SB_TO_NB_CAD1	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<2>	TRUE	HT_SB_TO_NB_CAD2	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<3>	TRUE	HT_SB_TO_NB_CAD3	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<4>	TRUE	HT_SB_TO_NB_CAD4	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<5>	TRUE	HT_SB_TO_NB_CAD5	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<6>	TRUE	HT_SB_TO_NB_CAD6	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_N<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CAD_P<7>	TRUE	HT_SB_TO_NB_CAD7	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_N<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
HT_MB_TO_NB_CTL_P<0>	TRUE	HT_SB_TO_NB_CTL0	HT_SB_TO_NB	HT_CAD	HT_SB_TO_NB_CAD
NC_HT_MB_TO_NB_CAD_P<8..15>	TRUE				
NC_HT_MB_TO_NB_CAD_N<8..15>	TRUE				
TP_HT_MB_TO_NB_CLK_N<1>	TRUE				
TP_HT_MB_TO_NB_CLK_P<1>	TRUE				
NC_HT_NB_TO_MB_CAD_P<8..15>	TRUE				
NC_HT_NB_TO_MB_CAD_N<8..15>	TRUE				
NC_HT_NB_TO_MB_CLK_N<1>	TRUE				
NC_HT_NB_TO_MB_CLK_P<1>	TRUE				
HT_NB_REFCLK_P<0>		HT_NB_REFCLK0	HT_NB_REFCLK	HT_CLK	HT_CLK
HT_NB_REFCLK_N<0>		HT_NB_REFCLK0		HT_CLK	HT_CLK
HT_NB_P<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_N<0>		HT_NB0		HT_CLK	HT_CLK
HT_NB_REFCLK_PF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK
HT_NB_REFCLK_NF<0>		HT_NB_REFCLK_F0		HT_CLK	HT_CLK

SIG_NAME	MIN_LINE_WIDTH	MIN_NECK_WIDTH	VOLTAGE
PWR_HT_AVDD	0.4MM	0.2MM	2.5
PWR_HT_AVDD2	0.4MM	0.2MM	2.5
KOD_L15_GND	0.4MM	0.2MM	0
HT_NB_G KEEP DIFF CLOCK FROM BEING A SINGLE XNET			0

HT ALIASES

FINO-ME 06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE: NONE SHT 101 OF 154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	0.38mm SPACING	HT_CLK66M_SB_C
HT_CLK66M_SB	0.38mm SPACING	HT_CLK66M_SB
	P3MM SPACING	HT_LDTRESET_L

Page Notes

Power aliases required by this page:
=PP2V5_PWRON_HT
=PP1V2_PWRON_HT

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- SB_HT_200M
  Stuffs resistor to select 200MHz HT I/F.

RA300 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLDVDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
CA300 10UF 10% 6.3V X5R 805
CA301 1uF 10% 6.3V CERM 402

RA310 3.3 5% 1/8W MF-LF 805 — PP1V2_PWRON_HT_PLLAVDD (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.50mm, MIN_NECK_WIDTH=0.38mm)
CA310 10UF 10% 6.3V X5R 805
CA311 1uF 10% 6.3V CERM 402

=PP2V5_PWRON_HT
CA320 0.1uF 20% 16V CERM 402

=PP1V2_PWRON_SB_HT
CA302 10UF 10% 6.3V X5R 805
CA330 0.1uF 20% 10V CERM 402
CA331 0.1uF 20% 10V CERM 402
CA332 0.1uF 20% 10V CERM 402

=PP1V2_PWRON_SB_HT
CA309 10UF 10% 6.3V X5R 805
CA340 0.1uF 20% 10V CERM 402
CA341 0.1uF 20% 10V CERM 402
CA342 0.1uF 20% 10V CERM 402

HTS2MC0+ PPA300 P4MM SM
HTS2MC0- PPA301 P4MM SM
HTS2MC0+ PPA303 P4MM SM
HTS2MC0- PPA304 P4MM SM

U2300 SHASTA V1.1 BGA-LF (3 OF 8) SEE_TABLE — HYPERTRANSPORT

Pin	HT_PLL / HT_RXVDD / HT_TXVDD	HT_CLKIN / HT_CADIN	HT_CLKOUT / HT_CADOUT
C7	AVDD HT_PLL		
B6	DVDD HT_PLL		
B19	VDDP HT		
B15	HT_RXVDD		
B17	HT_RXVDD		
G13	HT_RXVDD		
B12	HT_TXVDD		
B9	HT_TXVDD		
G11	HT_TXVDD		
D15		HT_CLKIN_P	HT_CLKOUT_P
C15		HT_CLKIN_N	HT_CLKOUT_N
D17		HT_CADIN_0_P	HT_CADOUT_0_P
C17		HT_CADIN_0_N	HT_CADOUT_0_N
B18		HT_CADIN_1_P	HT_CADOUT_1_P
A18		HT_CADIN_1_N	HT_CADOUT_1_N
F15		HT_CADIN_2_P	HT_CADOUT_2_P
E15		HT_CADIN_2_N	HT_CADOUT_2_N
D16		HT_CADIN_3_P	HT_CADOUT_3_P
C16		HT_CADIN_3_N	HT_CADOUT_3_N
B16		HT_CADIN_4_P	HT_CADOUT_4_P
A16		HT_CADIN_4_N	HT_CADOUT_4_N
D14		HT_CADIN_5_P	HT_CADOUT_5_P
C14		HT_CADIN_5_N	HT_CADOUT_5_N
E14		HT_CADIN_6_P	HT_CADOUT_6_P
F14		HT_CADIN_6_N	HT_CADOUT_6_N
B14		HT_CADIN_7_P	HT_CADOUT_7_P
A14		HT_CADIN_7_N	HT_CADOUT_7_N
F13		HT_CTLIN_P	HT_CTLOUT_P
E13		HT_CTLIN_N	HT_CTLOUT_N
E16		HT_PWROK_H	
C18		HT_RESET_L	
E17		HT_LDTSTOP_L	HT_LDTREQ_L
C8		HT_REFCLK	HT_R100P
D8		HT_S100M66M	HT_R100N
V6		SEL_HT00_H	
C6	HT_PLL AGND		
A6	HT_PLL DGND		
A13	HT_RXGND		
A17	HT_RXGND		
G12	HT_RXGND		
A12	HT_TXGND		
A8	HT_TXGND		
G10	HT_TXGND		

HT_MB_TO_SB_CLK_P<0> / HT_MB_TO_SB_CLK_N<0>
HT_MB_TO_SB_CAD_P<0> / HT_MB_TO_SB_CAD_N<0>
HT_MB_TO_SB_CAD_P<1> / HT_MB_TO_SB_CAD_N<1>
HT_MB_TO_SB_CAD_P<2> / HT_MB_TO_SB_CAD_N<2>
HT_MB_TO_SB_CAD_P<3> / HT_MB_TO_SB_CAD_N<3>
HT_MB_TO_SB_CAD_P<4> / HT_MB_TO_SB_CAD_N<4>
HT_MB_TO_SB_CAD_P<5> / HT_MB_TO_SB_CAD_N<5>
HT_MB_TO_SB_CAD_P<6> / HT_MB_TO_SB_CAD_N<6>
HT_MB_TO_SB_CAD_P<7> / HT_MB_TO_SB_CAD_N<7>
HT_MB_TO_SB_CTL_P<0> / HT_MB_TO_SB_CTL_N<0>
HT_PWROK
HT_LDTRESET_L
HT_LDTSTOP_L
HT_CLK66M_SB_C
SB_HT_S100M66M
SB_SELHT100
HT_LDTREQ_SB_L
SB_HT_R100_P
SB_HT_R100_N

HT_SB_TO_MB_CLK_P<0> / HT_SB_TO_MB_CLK_N<0>
HT_SB_TO_MB_CAD_P<0> / HT_SB_TO_MB_CAD_N<0>
HT_SB_TO_MB_CAD_P<1> / HT_SB_TO_MB_CAD_N<1>
HT_SB_TO_MB_CAD_P<2> / HT_SB_TO_MB_CAD_N<2>
HT_SB_TO_MB_CAD_P<3> / HT_SB_TO_MB_CAD_N<3>
HT_SB_TO_MB_CAD_P<4> / HT_SB_TO_MB_CAD_N<4>
HT_SB_TO_MB_CAD_P<5> / HT_SB_TO_MB_CAD_N<5>
HT_SB_TO_MB_CAD_P<6> / HT_SB_TO_MB_CAD_N<6>
HT_SB_TO_MB_CAD_P<7> / HT_SB_TO_MB_CAD_N<7>
HT_SB_TO_MB_CTL_P<0> / HT_SB_TO_MB_CTL_N<0>

PPA302 P4MM SM
RA355 0 5% 1/10W MF-LF 402 — HT_CLK66M_SB — 1.0V pk-pk

=PP1V2_PWRON_SB_HT
RA352 4.7K 1% 1/10W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA354 10K 5% 1/10W MF-LF 402 — NOSTUFF — 1 = 100MHz
RA353 4.7K 1% 1/10W MF-LF 402 — 0 = 66MHz
RA351 1K 1% 1/10W MF-LF 402 — 0 = 200MHz

RA301 0 5% 1/10W MF-LF 402 — HT_LDTREQ_L

RA350 82.5 1% 1/10W MF-LF 402
CA350 47pF 5% 50V CERM 402
CA351 47pF 5% 50V CERM 402

HT Refclk	HT I/F Speed
1 = 100MHz	1 = 100MHz
0 = 66MHz	0 = 200MHz

← DETERMINES THE OPERATING FREQUENCY OF HT CORE
1: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 100 MHZ
0: THE HT SLAVE, HTGS AND THE HT SIDE OF THE PCI BRIDGES OPERATE AT 200 MHZ

Shasta HyperTransport

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	103	154

LAST_MODIFIED=Wed Nov 16 09:40:26 2005

DRAWING
TITLE=K1LOWARA
ASSEMBLY=DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
		PCI_AD<31..28> 120 121 122 125
		PCI_AD<27> 120 121 122 125
		PCI_AD<26..24> 120 121 122 125
		PCI_AD<23> 120 121 122
		PCI_AD<22> 120 121 122
		PCI_AD<21> 120 121 122
		PCI_AD<20> 120 121 122 125
		PCI_AD<19..18> 120 121 122 125
		PCI_AD<17> 120 121 122 125
		PCI_AD<16..0> 120 121 122 125
		PCI_CBE_L<3..0> 120 121 122
		PCI_PAR 120 121 122
		PCI_DEVSEL_L 119 120 121 122
		PCI_FRAME_L 119 120 121 122
		PCI_IRDY_L 119 120 121 122
		PCI_TRDY_L 119 120 121 122
		PCI_STOP_L 119 120 121 122
1161	P3MM_SPACING	PCI_CLK66M_SB_INT 26 27 119

Q63 APPLICATION OF POWER NET "=PP3V3_SB_PCI" IS RUN

Page Notes

Power aliases required by this page:
- =PP3V3_PCI
- =PP3V3_SB_PCI (CAN BE _PP3V3_PCI)
- =PP3V3_PWRON_SB
- =PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD11 - PCI0 (0x106B/0x0053)
AD11 - PCI1 (0x106B/0x0054)
AD11 - PCI2 (0x106B/0x0055)

AD23 - KeyLargo (0x106B/0x004F, PCI1)
AD28 - SATA 150 (0x1166/0x0240, PCI0 or 2)
AD29 - UATA 133 (0x106B/0x0050, PCI0 or 2)
AD30 - FireWire (0x106B/0x0052, PCI0 or 2)
AD31 - Ethernet (0x106B/0x0051, PCI0)

PP3V3_RUN_SB 119 7
PPB905 P4MM SM PP 1 PP_3V3RUNSB_B9
XWB900 SM 2 1
CB910 10UF 10% 6.3V X5R 805
CB900 0.1UF 20% 10V CERM 402
CB901 0.1UF 20% 10V CERM 402
CB902 0.1UF 20% 10V CERM 402
CB903 0.1UF 20% 10V CERM 402
CB904 0.1UF 20% 10V CERM 402
NO STUFF
CB911 10UF 10% 6.3V X5R 805
CB905 0.1UF 20% 10V CERM 402
CB906 0.1UF 20% 10V CERM 402
CB907 0.1UF 20% 10V CERM 402
CB908 0.1UF 20% 10V CERM 402
CB909 0.1UF 20% 10V CERM 402

XWB901 SM 2 1 6 PP_2V5PWRONSB_B9
PPB906 P4MM SM PP 1
=PP2V5_PWRON_SB 7 23 24 138
CB920 0.1UF 20% 10V CERM 402
CB921 0.1UF 20% 10V CERM 402
CB922 0.1UF 20% 10V CERM 402
CB923 0.1UF 20% 10V CERM 402

PPB900 P4MM SM PP 1
P3MM SPACING
PCI_CLK66M_SB_INT 119 27 26
PPB901 P4MM SM PP 1
PCI_CLK33M_SB_EXT_RR 27 26
NOSTUFF
CB912 2PF +/-0.25PF 50V C0G 402-1
STUFF NEAR SHASTA

"Slot A" - AD17
PCI_SLOTA_REQ_L 121 119 → PCIREQ_0_L
PCI_SLOTA_GNT_L 121 119 → PCIGNT_0_L
"Slot G" - AD27
PCI_SLOTG_REQ_L 122 119 → PCIREQ_1_L
PCI_SLOTG_GNT_L 122 119 → PCIGNT_1_L
"Slot D" - AD20
PCI_SLOTD_REQ_L 119 → PCIREQ_2_L
PCI_SLOTD_GNT_L 119 → PCIGNT_2_L
ROM_CS_L 125 121 → ROMCS_L
ROM_OE_L 125 121 → ROMOE_L
ROM_WE_L 125 121 → ROMRW_L

U2300 SHASTA V1.1 BGA-LF (4 OF 8) — SEE_TABLE
VDDOPC: AA22 B22 E21 H16 J21 M16 N21 R20 U21 V19
PCIVDDP: B20 J18 N20 U20
PCIBR_CLK_H AB9
PCI1CLK_H U19
PCI1RST_L U18 SB_PCI_RESET_L
NET_SPACING_TYPE=P3MM SPACING

PCI1AD_0_H	L18	PCI_SB_AD<0>	120
PCI1AD_1_H	K19	PCI_SB_AD<1>	120
PCI1AD_2_H	L22	PCI_SB_AD<2>	120
PCI1AD_3_H	M22	PCI_SB_AD<3>	120
PCI1AD_4_H	M18	PCI_SB_AD<4>	120
PCI1AD_5_H	L20	PCI_SB_AD<5>	120
PCI1AD_6_H	M21	PCI_SB_AD<6>	120
PCI1AD_7_H	N16	PCI_SB_AD<7>	120
PCI1AD_8_H	M20	PCI_SB_AD<8>	120
PCI1AD_9_H	P22	PCI_SB_AD<9>	120
PCI1AD_10_H	M17	PCI_SB_AD<10>	120
PCI1AD_11_H	N18	PCI_SB_AD<11>	120
PCI1AD_12_H	M19	PCI_SB_AD<12>	120
PCI1AD_13_H	N19	PCI_SB_AD<13>	120
PCI1AD_14_H	P21	PCI_SB_AD<14>	120
PCI1AD_15_H	R22	PCI_SB_AD<15>	120
PCI1AD_16_H	P20	PCI_SB_AD<16>	120
PCI1AD_17_H	V21	PCI_SB_AD<17>	120
PCI1AD_18_H	P18	PCI_SB_AD<18>	120
PCI1AD_19_H	T20	PCI_SB_AD<19>	120
PCI1AD_20_H	R16	PCI_SB_AD<20>	120
PCI1AD_21_H	R17	PCI_SB_AD<21>	120
PCI1AD_22_H	W21	PCI_SB_AD<22>	120
PCI1AD_23_H	Y22	PCI_SB_AD<23>	120
PCI1AD_24_H	R18	PCI_SB_AD<24>	120
PCI1AD_25_H	T19	PCI_SB_AD<25>	120
PCI1AD_26_H	T18	PCI_SB_AD<26>	120
PCI1AD_27_H	Y21	PCI_SB_AD<27>	120
PCI1AD_28_H	W20	PCI_SB_AD<28>	120
PCI1AD_29_H	T16	PCI_SB_AD<29>	120
PCI1AD_30_H	AA21	PCI_SB_AD<30>	120
PCI1AD_31_H	T17	PCI_SB_AD<31>	120

PCI

PCI1C_BE_0_L	L19	PCI_SB_CBE_L<0>	120
PCI1C_BE_1_L	P16	PCI_SB_CBE_L<1>	120
PCI1C_BE_2_L	V22	PCI_SB_CBE_L<2>	120
PCI1C_BE_3_L	V20	PCI_SB_CBE_L<3>	120
PCI1DEVSEL_L	T22	PCI_SB_DEVSEL_L	120
PCI1FRAME_L	T21	PCI_SB_FRAME_L	120
PCI1IRDY_L	R21	PCI_SB_IRDY_L	120
PCI1TRDY_L	P19	PCI_SB_TRDY_L	120
PCI1STOP_L	P17	PCI_SB_STOP_L	120
PCI1PAR_H	N17	PCI_SB_PAR	120

=PP3V3_PWRON_SB 7 20 23 24 56
RB955 4.7K 1% 1/16W MF-LF 402
CB950 0.1UF 20% 10V CERM 402
NOSTUFF
RB950 4.7K 1% 1/16W MF-LF 402
UB950 MC74VHC1G08 SOT23-5-LF
PCI_RESET_L 20 92
SYS_IO_RESET_L 122 30 28 24
Shasta drives PCI RESET, but its output may not be valid during power-up, so it is ANDed with a reset from the SMU.
RB900 0 NOSTUFF 5% 1/16W MF-LF 402

PP3V3_RUN_SB 7 119
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_REQ_L 119 121
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTA_GNT_L 119 121
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTG_REQ_L 119 122
RPB900 4.7K 5% 1/16W SM-LF
PCI_SLOTG_GNT_L 119 122
RPB901 4.7K 5% 1/16W SM-LF
PCI_SLOTD_REQ_L 119
RPB901 4.7K 5% 1/16W SM-LF
PCI_SLOTD_GNT_L 119

PP3V3_RUN_SB 119 7
RPB902 4.7K 5% 1/16W SM-LF
PCI_DEVSEL_L 122 121 120 119
RPB902 4.7K 5% 1/16W SM-LF
PCI_FRAME_L 122 121 120 119
RPB902 4.7K 5% 1/16W SM-LF
PCI_IRDY_L 122 121 120 119
RPB902 4.7K 5% 1/16W SM-LF
PCI_TRDY_L 122 121 120 119
RPB901 4.7K 5% 1/16W SM-LF
PCI_STOP_L 122 121 120 119

Shasta PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING
I TO MAINTAIN THE DOCUMENT IN CONFIDENCE
II NOT TO REPRODUCE OR COPY IT
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 119 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:30 2005
DRAWING
TITLE=KILOWARA
ASSEMBLY=DRAWING

ALL RESISTOR PACKS ARE 47 OHM 1/16W 5%

R PAKS ARE PIN SWAPPABLE ACROSS ALL SIGNALS (EXCEPT IDSELS)

119	PCI_SB_AD<0>	RPC003	4	5	47	PCI_AD<0>	119 121 122 125
119	PCI_SB_AD<1>	RPC003	1	8	47	PCI_AD<1>	119 121 122 125
119	PCI_SB_AD<2>	RPC009	1	8	47	PCI_AD<2>	119 121 122 125
119	PCI_SB_AD<3>	RPC001	3	6	47	PCI_AD<3>	119 121 122 125
119	PCI_SB_AD<4>	RPC000	3	6	47	PCI_AD<4>	119 121 122 125
119	PCI_SB_AD<5>	RPC003	2	7	47	PCI_AD<5>	119 121 122 125
119	PCI_SB_AD<6>	RPC001	4	5	47	PCI_AD<6>	119 121 122 125
119	PCI_SB_AD<7>	RPC000	2	7	47	PCI_AD<7>	119 121 122 125
119	PCI_SB_AD<8>	RPC007	4	5	47	PCI_AD<8>	119 121 122 125
119	PCI_SB_AD<9>	RPC002	1	8	47	PCI_AD<9>	119 121 122 125
119	PCI_SB_AD<10>	RPC000	1	8	47	PCI_AD<10>	119 121 122 125
119	PCI_SB_AD<11>	RPC009	3	6	47	PCI_AD<11>	119 121 122 125
119	PCI_SB_AD<12>	RPC000	4	5	47	PCI_AD<12>	119 121 122 125
119	PCI_SB_AD<13>	RPC009	4	5	47	PCI_AD<13>	119 121 122 125
119	PCI_SB_AD<14>	RPC002	2	7	47	PCI_AD<14>	119 121 122 125
119	PCI_SB_AD<15>	RPC002	4	5	47	PCI_AD<15>	119 121 122 125
119	PCI_SB_AD<16>	RPC002	3	6	47	PCI_AD<16>	119 121 122 125

RC000

119	PCI_SB_AD<17>		1		47 5% 1/16W MF-LF 402	2	PCI_AD<17>	119 121 122 125

119	PCI_SB_AD<18>	RPC007	1	8	47	PCI_AD<18>	119 121 122 125
119	PCI_SB_AD<19>	RPC006	2	7	47	PCI_AD<19>	119 121 122 125
119	PCI_SB_AD<20>	RPC007	2	7	47	PCI_AD<20>	119 121 122 125
119	PCI_SB_AD<21>	RPC008	1	8	47	PCI_AD<21>	119 121 122
119	PCI_SB_AD<22>	RPC004	1	8	47	PCI_AD<22>	119 121 122
119	PCI_SB_AD<23>	RPC006	4	5	47	PCI_AD<23>	119 121 122
119	PCI_SB_AD<24>	RPC008	4	5	47	PCI_AD<24>	119 121 122 125
119	PCI_SB_AD<25>	RPC006	3	6	47	PCI_AD<25>	119 121 122 125
119	PCI_SB_AD<26>	RPC008	3	6	47	PCI_AD<26>	119 121 122 125

RC001

119	PCI_SB_AD<27>		1		47 5% 1/16W MF-LF 402	2	PCI_AD<27>	119 121 122 125

119	PCI_SB_AD<28>	RPC004	4	5	47	PCI_AD<28>	119 121 122 125
119	PCI_SB_AD<29>	RPC008	2	7	47	PCI_AD<29>	119 121 122 125
119	PCI_SB_AD<30>	RPC004	2	7	47	PCI_AD<30>	119 121 122 125
119	PCI_SB_AD<31>	RPC007	3	6	47	PCI_AD<31>	119 121 122 125
119	PCI_SB_CBE_L<0>	RPC003	3	6	47	PCI_CBE_L<0>	119 121 122
119	PCI_SB_CBE_L<1>	RPC001	1	8	47	PCI_CBE_L<1>	119 121 122
119	PCI_SB_CBE_L<2>	RPC006	1	8	47	PCI_CBE_L<2>	119 121 122
119	PCI_SB_CBE_L<3>	RPC004	3	6	47	PCI_CBE_L<3>	119 121 122
119	PCI_SB_DEVSEL_L	RPC005	3	6	47	PCI_DEVSEL_L	119 121 122
119	PCI_SB_FRAME_L	RPC005	4	5	47	PCI_FRAME_L	119 121 122
119	PCI_SB_IRDY_L	RPC005	2	7	47	PCI_IRDY_L	119 121 122
119	PCI_SB_TRDY_L	RPC005	1	8	47	PCI_TRDY_L	119 121 122
119	PCI_SB_STOP_L	RPC001	2	7	47	PCI_STOP_L	119 121 122
119	PCI_SB_PAR	RPC009	2	7	47	PCI_PAR	119 121 122

PLACE CLOSE TO SHASTA

AD<17> IS IDSEL FOR AIRPORT
AD<27> IS IDSEL FOR USB

PCI SERIES TERMINATION

SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 120 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
PCI_CLK_AIRPORT	CLOCKS	

PCI_CLK33M_AIRPORT 26 121

Page Notes

Power aliases required by this page:
- _PP3V3_PCI

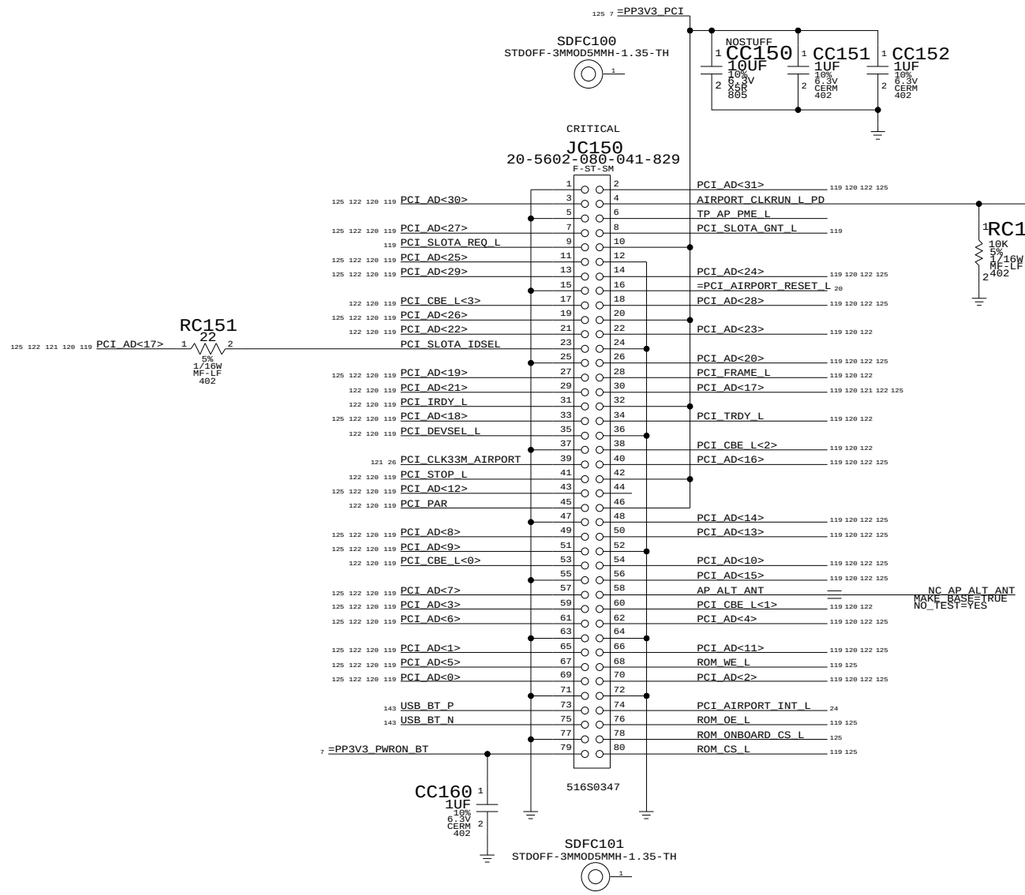
Signal aliases required by this page:
- _PCI_CLK33M_AIRPORT (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

Q85 WIRELESS CONNECTOR



AIRPORT & BLUETOOTH

SYNC_MASTER=FINO-MW SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	121	154

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	CLOCKS	

=PCI_CLK33M_USB2 27 122

Page Notes

Power aliases required by this page:
- _PPVIO_PCI (to 3.3V or 5V)

Signal aliases required by this page:
- _PCI_CLK33M_USB2 (33MHz PCI clock)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports
D3cold.

Q63 APPLICATION OF POWER NET "=PPVIO_PCI_USB2" IS PP3V3_RUN

122 7 =PPVIO_PCI_USB2

CC201 0.1uF 20% 10V CERM 402
CC202 0.1uF 20% 10V CERM 402
CC203 0.1uF 20% 10V CERM 402

XWC200 SM 2 1 6 PP_VIOPCIUSB2_C2 P4MM SM PP PPC203

VDD_PCI (M3, M4, C8)

CRITICAL
UC200
NEC_UPD720101_USB2
FBGA-LF

125 121 120 119 PCI_AD<0>	M5	AD0	
125 121 120 119 PCI_AD<1>	P5	AD1	
125 121 120 119 PCI_AD<2>	N5	AD2	
125 121 120 119 PCI_AD<3>	P4	AD3	
125 121 120 119 PCI_AD<4>	N4	AD4	
125 121 120 119 PCI_AD<5>	M3	AD5	
125 121 120 119 PCI_AD<6>	N3	AD6	
125 121 120 119 PCI_AD<7>	M1	AD7	
125 121 120 119 PCI_AD<8>	L2	AD8	
125 121 120 119 PCI_AD<9>	L1	AD9	
125 121 120 119 PCI_AD<10>	K2	AD10	
125 121 120 119 PCI_AD<11>	L3	AD11	
125 121 120 119 PCI_AD<12>	K1	AD12	
125 121 120 119 PCI_AD<13>	K3	AD13	
125 121 120 119 PCI_AD<14>	J2	AD14	
125 121 120 119 PCI_AD<15>	J1	AD15	
125 121 120 119 PCI_AD<16>	F2	AD16	
125 121 120 119 PCI_AD<17>	E1	AD17	
125 121 120 119 PCI_AD<18>	E2	AD18	
125 121 120 119 PCI_AD<19>	D1	AD19	
125 121 120 119 PCI_AD<20>	D2	AD20	
121 120 119 PCI_AD<21>	D3	AD21	
121 120 119 PCI_AD<22>	C2	AD22	
121 120 119 PCI_AD<23>	C1	AD23	
125 121 120 119 PCI_AD<24>	B2	AD24	
125 121 120 119 PCI_AD<25>	A2	AD25	
125 121 120 119 PCI_AD<26>	B3	AD26	
125 121 120 119 PCI_AD<27> (PCI_AD<27>)	C4	AD27	
125 121 120 119 PCI_AD<28>	A3	AD28	
125 121 120 119 PCI_AD<29>	C5	AD29	
125 121 120 119 PCI_AD<30>	B4	AD30	
125 121 120 119 PCI_AD<31>	A4	AD31	
121 120 119 PCI_CBE_L<0>	M2	CBE0	
121 120 119 PCI_CBE_L<1>	J3	CBE1	
121 120 119 PCI_CBE_L<2>	F3	CBE2	
121 120 119 PCI_CBE_L<3>	C3	CBE3	
121 120 119 PCI_PAR	J4	PAR	
121 120 119 PCI_FRAME_L	F3	FRAME	
121 120 119 PCI_IRDY_L	F4	IRDY	
121 120 119 PCI_TRDY_L	G1	TRDY	
121 120 119 PCI_STOP_L	G3	STOP	
PCI_SLOTG_IDSEL	B1	IDSEL	
121 120 119 PCI_DEVSEL_L	G2	DEVSEL	
119 PCI_SLOTG_REQ_L	C6	REQ	
119 PCI_SLOTG_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR (OD)	
NEC_INTA_L	C7	INTA (OD)	
NEC_INTB_L	B7	INTB (OD)	
NEC_INTC_L	A7	INTC (OD)	
122 27 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST (CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D5	PME (OD)	
	C5	VCCRST (PCI RESET)	
6 TP_NEC_SMI_L	L6	SMI (OD)	
NEC_LEGC_PD	L7	LEGC	

IPD	NTEST1	M8	TP_NEC_NTEST1 6
IPD	SMC	M7	TP_NEC_SMC 6
IPD	TEB	N7	TP_NEC_TEB
IPD	AMC	P7	TP_NEC_AMC
IPD	TEST	L8	TP_NEC_TEST 6
	NANDTEST	M10	TP_NEC_NANDTEST
	SRCLK	M9	TP_NEC_SRCLK 6
	SRDTA	N9	TP_NEC_SRDATA
IPD	SRMOD	P9	TP_NEC_SRMOD 6

ALL NETS TO FUNCTIONAL TEST PAGE

RC214 22 5% 1/16W MF-LF 402

122 7 =PPVIO_PCI_USB2

RC216 10K 5% 1/16W MF-LF 402
RC213 10K 5% 1/16W MF-LF 402

24 PCI_USB2_INT_L

RPC203 47 5% 1/16W SM-LF (4 5)
RPC203 47 5% 1/16W SM-LF (2 7)
RPC203 47 5% 1/16W SM-LF (3 6)

119 30 28 24 SYS_IO_RESET_L

RC250 47 5% 1/16W MF-LF 402

28 24 SYS_PME_L

RC251 47 5% 1/16W MF-LF 402

20 =PCI_USB2_RESET_L

RC250, RC251 & RPC203 REQUIRED TO facilitate NAND-tree testing

RC215 4.7K 1% 1/16W MF-LF 402

RPC203 47 5% 1/16W SM-LF (8 1)

PPC200 P4MM SM PP 1
PPC201 P4MM SM PP 1

USB 2.0 PCI Interface

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 122 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:32 2005

DRAWING

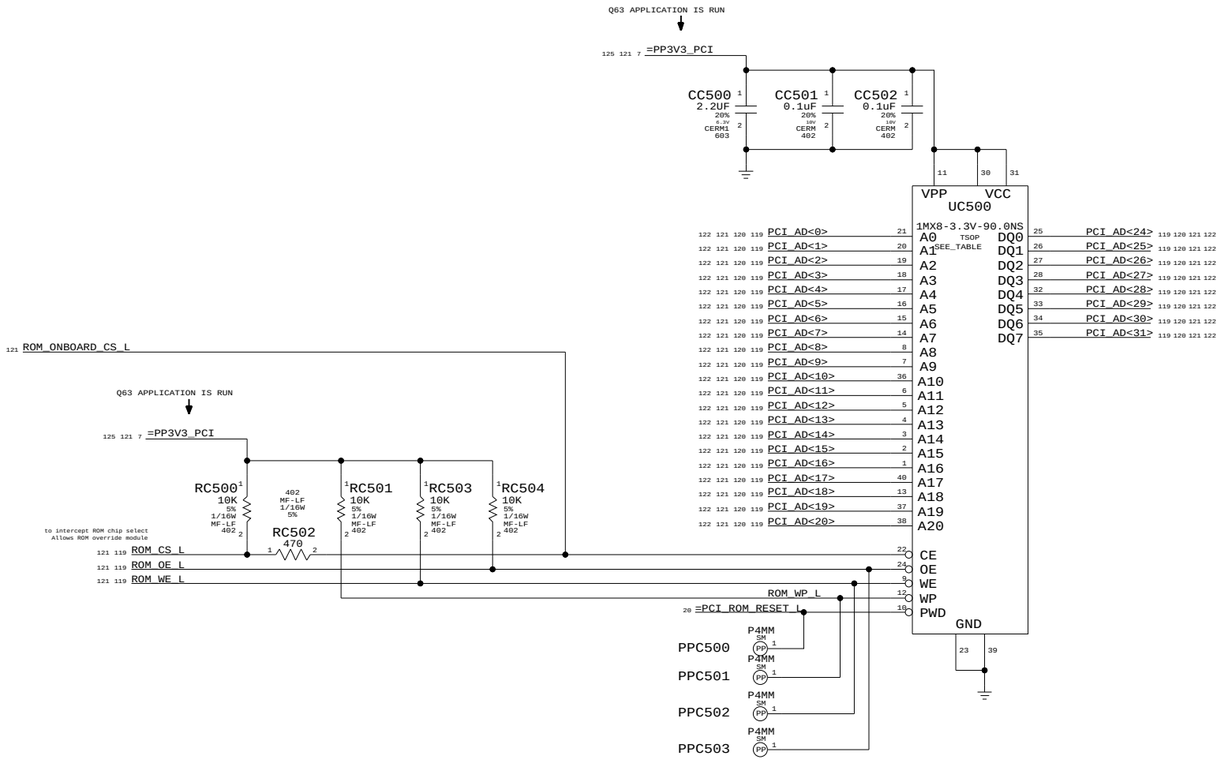
Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a BootROM part number. Must use a TABLE_x_ITEM symbol to declare U7500 part number.



BootROM

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	125	154

LAST_MODIFIED=Wed Nov 16 09:40:33 2005

DRAWING
TITLE=MISLOWARA
ASSEMBLY=DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	SATA	SATA	SATA_RXD1_C	SATA_RXD_P1_C
	SATA	SATA	SATA_RXD1_C	SATA_RXD_N1_C
	SATA	SATA	SATA_TXD1	SATA_TXD_P1
	SATA	SATA	SATA_TXD1	SATA_TXD_N1
	SATA	SATA	SATA_RXD2_C	SATA_RXD_P2_C
	SATA	SATA	SATA_RXD2_C	SATA_RXD_N2_C
	SATA	SATA	SATA_TXD2	SATA_TXD_P2
	SATA	SATA	SATA_TXD2	SATA_TXD_N2
				UATA_DD<15..8>
				UATA_DD<7>
				UATA_DD<6..0>
				UATA_DA<2..0>
				UATA_CS0_L
				UATA_CS1_L
				UATA_HSTROBE
				UATA_STOP
				UATA_DMACK_L
	UATA_NETSPA			UATA_RESET_L
				UATA_DSTROBE
				UATA_DMARQ
				UATA_INTRQ
374				UATA_DD_R<15..8>
375				UATA_DD_R<7>
376				UATA_DD_R<6..0>
374				UATA_DA_R<2..0>
375				UATA_CS0_L_R
376				UATA_CS1_L_R
377				UATA_DMACK_L_R
376				UATA_HSTROBE_R
374				UATA_STOP_R
375				UATA_RESET_L_R

PLACE TERMINATION RESISTORS AT UATA CONNECTOR JC901

RC706 33 — UATA_RESET_L_R → UATA_RESET_L
RC704 22 — UATA_DMACK_L_R → UATA_DMACK_L
RC702 22 — UATA_HSTROBE_R → UATA_HSTROBE
RC703 22 — UATA_STOP_R → UATA_STOP
RC700 33 — UATA_CS0_L_R → UATA_CS0_L
RC701 33 — UATA_CS1_L_R → UATA_CS1_L

5% 1/16W MF-LF 402

DIOR- :HDMARDY- :HSTROBE >

DIOW- :STOP >

SPARE
RPC704 33 5% 1/16W SM-LF

RPC704 33 — UATA_DA_R<0> → UATA_DA<0>
RPC704 33 — UATA_DA_R<1> → UATA_DA<1>
RPC704 33 — UATA_DA_R<2> → UATA_DA<2>

RPC700 33 — UATA_DD_R<0> → UATA_DD<0>
RPC700 33 — UATA_DD_R<1> → UATA_DD<1>
RPC700 33 — UATA_DD_R<2> → UATA_DD<2>
RPC703 33 — UATA_DD_R<3> → UATA_DD<3>
RPC701 33 — UATA_DD_R<4> → UATA_DD<4>
RPC701 33 — UATA_DD_R<5> → UATA_DD<5>
RPC703 33 — UATA_DD_R<6> → UATA_DD<6>
RPC702 33 — UATA_DD_R<7> → UATA_DD<7>
RPC702 33 — UATA_DD_R<8> → UATA_DD<8>
RPC703 33 — UATA_DD_R<9> → UATA_DD<9>
RPC700 33 — UATA_DD_R<10> → UATA_DD<10>
RPC702 33 — UATA_DD_R<11> → UATA_DD<11>
RPC701 33 — UATA_DD_R<12> → UATA_DD<12>
RPC702 33 — UATA_DD_R<13> → UATA_DD<13>
RPC701 33 — UATA_DD_R<14> → UATA_DD<14>
RPC703 33 — UATA_DD_R<15> → UATA_DD<15>

5% 1/16W SM-LF

RC705 10K 5% 1/16W MF-LF 402

=PP1V2_PWRON_DISK_SB → LC700 600-OHM-1.0A 0805

MIN_NECK_WIDTH=0.2MM
MIN_LINE_WIDTH=0.6MM
PP1V2_SATA_VDD

CC705 2.2UF 20% 6.3V CERM1 603
CC700 0.1UF 20% 10V CERM 402
CC701 0.1UF 20% 10V CERM 402
CC702 0.1UF 20% 10V CERM 402
CC703 0.1UF 20% 10V CERM 402
CC704 0.1UF 20% 10V CERM 402

XWCC00 SM → PP_1V2PWRONDISKSB_CC, NO_TEST=YES → P4MM SM PP → PPCC00

SATA_VDD x 5

SATA_VDD (AB14, AB17, T14, W15, Y18)

U2300 SHASTA V1.1 BGA-LF (5 OF 8) SEE_TABLE

UATA

UD_IDEDD_0_H	J6	UATA_DD_R<0>	
UD_IDEDD_1_H	H7	UATA_DD_R<1>	
UD_IDEDD_2_H	H6	UATA_DD_R<2>	
UD_IDEDD_3_H	E2	UATA_DD_R<3>	
UD_IDEDD_4_H	C1	UATA_DD_R<4>	
UD_IDEDD_5_H	C2	UATA_DD_R<5>	
UD_IDEDD_6_H	E3	UATA_DD_R<6>	
UD_IDEDD_7_H	G6	UATA_DD_R<7>	
UD_IDEDD_8_H	G5	UATA_DD_R<8>	
UD_IDEDD_9_H	D4	UATA_DD_R<9>	
UD_IDEDD_10_H	G7	UATA_DD_R<10>	
UD_IDEDD_11_H	F6	UATA_DD_R<11>	
UD_IDEDD_12_H	C3	UATA_DD_R<12>	
UD_IDEDD_13_H	F5	UATA_DD_R<13>	
UD_IDEDD_14_H	E5	UATA_DD_R<14>	
UD_IDEDD_15_H	D5	UATA_DD_R<15>	
UD_IDEDA0_H	E6	UATA_DA_R<0>	
UD_IDEDA1_H	C4	UATA_DA_R<1>	
UD_IDEDA2_H	D6	UATA_DA_R<2>	
UD_IDECS1FX_L	B3	UATA_CS0_L_R	
UD_IDECS3FX_L	B4	UATA_CS1_L_R	
UD_IDEDMACK_L	E8	UATA_DMACK_L_R	
UD_IDERD_L	E4	UATA_HSTROBE_R	
UD_IDEWR_L	D3	UATA_STOP_R	
UD_IDERST_L	E7	UATA_RESET_L_R	
UD_IDECHRDY_H	F9	UATA_DSTROBE	
UD_IDEDMARQ_H	D7	UATA_DMARQ	
UD_IDEINTRQ_H	C5	UATA_INTRQ	

DSTROBE aka: IORDY/HDMARDY* / HSTROBE aka: DIOR* / STOP aka: DIOW*

SATA 0

RXDP1	Y17	SATA_RXD_P1_C	
RXDN1	Y16	SATA_RXD_N1_C	
TXDP1	AA16	SATA_TXD_P1	
TXDN1	AB16	SATA_TXD_N1	

SATA 1

RXDP2	AB15	SATA_RXD_P2_C	
RXDN2	AA15	SATA_RXD_N2_C	
TXDP2	Y15	SATA_TXD_P2	
TXDN2	Y14	SATA_TXD_N2	

SATA_GND (AA14, AA17, T13, W16)

AC coupling required for any SATA pair used.
Recommend 0.1uF cap placed close to Shasta.
(Caps provided by device page)

P4MM SM PP → PPCC01

Page Notes

Power aliases required by this page:
- _PP1V2_PWRON_DISK

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: SATA

Line To Line:	0.38mm
Length Tolerance:	1.27mm
Primary Max Sep:	0.25mm outer
Primary Max Sep:	0.23mm inner
Secondary Max Sep:	2.54mm
Secondary Length:	12.70mm

NOTE: Target differential impedance for SATA data pairs is 100 ohms.

Shasta Disk

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

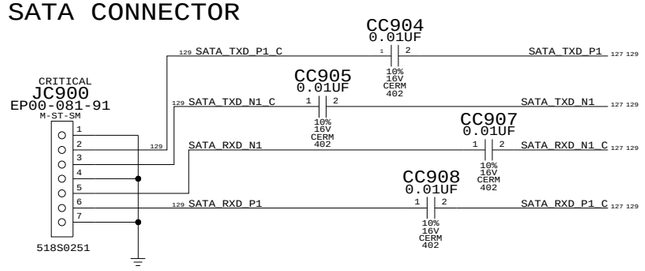
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 127 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:33 2005

DRAWING
TITLE=SCHEMA
ABBREV=SHMAKNG

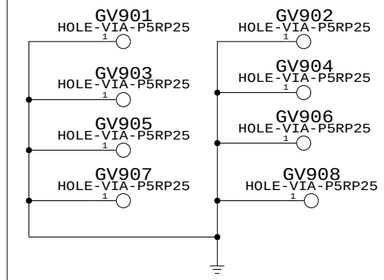
SATA CONNECTOR



SATA PORT1 IS NOT USED IN M23/M33:NO TEST

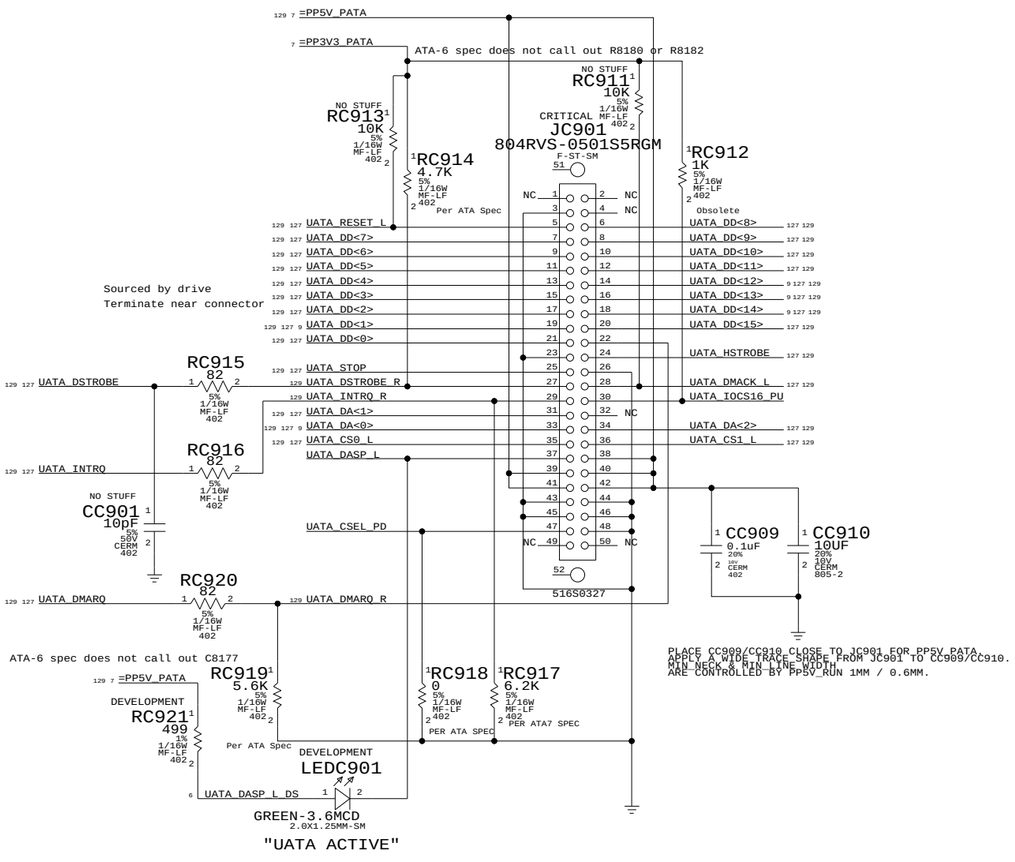
- SATA_TXD_P2 — NC_SATA_TXD_P2 MAKE_BASE=TRUE
- SATA_TXD_N2 — NC_SATA_TXD_N2 MAKE_BASE=TRUE
- SATA_RXD_N2_C — NC_SATA_RXD_N2_C MAKE_BASE=TRUE
- SATA_RXD_P2_C — NC_SATA_RXD_P2_C MAKE_BASE=TRUE

SATA DIFF PAIR GND VIAS



4-12-05
ADD THESE GROUND VIAS NEAR EACH LAYER JUMP FOR THE SATA DIFF PAIRS. ONE GND VIA PER SIGNAL VIA, AND PLACE GND VIA NO CLOSER THAN 0.152MM TO SIGNAL VIA.

PATA CONNECTOR



UATA FROM RPAKS TO JC901

	ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NO_TEST
UATA_DD<15..8>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DD<7>	UATA_DD7	UATA_NETPH	UATA_NETSPA		
UATA_DD<6..0>	UATA_DD	UATA_NETPH	UATA_NETSPA		
UATA_DA<2..0>	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS0_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_CS1_L	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_STOP	UATA_HOST	UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L	UATA_HOST_R	UATA_NETPH	UATA_NETSPA		
UATA_RESET_L	UATA_RESET_L	UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE_R	UATA_DEV_R_C	UATA_NETPH	UATA_NETSPA		
UATA_DMARQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		
UATA_INTRQ_R	UATA_DEV_R	UATA_NETPH	UATA_NETSPA		

UATA FROM SHASTA U2300 TO RPAKS

UATA_DD_R<15..8>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<7>		UATA_NETPH	UATA_NETSPA		
UATA_DD_R<6..0>		UATA_NETPH	UATA_NETSPA		
UATA_DA_R<2..0>		UATA_NETPH	UATA_NETSPA		
UATA_CS0_L_R		UATA_NETPH	UATA_NETSPA		
UATA_CS1_L_R		UATA_NETPH	UATA_NETSPA		
UATA_HSTROBE_R		UATA_NETPH	UATA_NETSPA		
UATA_STOP_R		UATA_NETPH	UATA_NETSPA		
UATA_DMACK_L_R		UATA_NETPH	UATA_NETSPA		
UATA_RESET_L_R		UATA_NETPH	UATA_NETSPA		
UATA_DSTROBE		UATA_NETPH	UATA_NETSPA		
UATA_DMARQ		UATA_NETPH	UATA_NETSPA		
UATA_INTRQ		UATA_NETPH	UATA_NETSPA		

SATA_TXD_P1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_N1	SATA_TXD1	SATA	SATA		TRUE
SATA_TXD_P1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_TXD_N1_C	SATA_TXD1	SATA	SATA	TX1C	TRUE
SATA_RXD_N1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_P1_C	SATA_RXD1	SATA	SATA		TRUE
SATA_RXD_N1	SATA_RXD1	SATA	SATA	RX1C	TRUE
SATA_RXD_P1	SATA_RXD1	SATA	SATA	RX1C	TRUE

4-11-05: BOARD FILE HAS PHYSICAL/SPACING NAME ASSIGMENT ALREADY FOR SATA DIFF PAIRS (CAP TO SHASTA). BUT NOT FOR THE SATA CAP TO CONNECTOR ROUTES, WHICH THE ABOVE ARE ADDED FOR THIS PURPOSE.

UATA TRACE IMPEDANCE ROUTE TO 50 OHMS

4-8-05
NOTES FOR SHARED PAGE 127
FOR M23/M33 CREATE A WIDE SHAPE
FOR PP1V2_SATA_VDD AND THEN NECK DOWN
TO THE DEFAULT VALUE WHEN NECESSARY.
THE WIDTH/NECK PROPERTIES ON PAGE 127
ARE SET BY Q63 FOR SCHEMATIC SHARING.

LC700 CHANGED TO 155S0240 (600 OHM,0.2 OHM DCR,1A)
PREVIOUS ONE WAS 155S0031 (600 OHM,0.6 OHM DCR,0.2A)
PER TOKIN AMERICA PN: N2012Z601.

4-11-05.
PP1V2_ALL REG. IS SET TO BE 1.22V TO 1.23V
AS NOTED ON THE 1.2 REG PAGE 13. THIS WILL
HELP MITIGATE THE LOSS ACROSS THE Q1306 FET
SI3326DV.

4-12-05.
UPDATED AC COUPLING CAPS FOR SATA JC900.
ADDED DECOUPLING CAPS FOR JC901 PP5V_PATA NET.

Disk Connectors

SYNC_MASTER=M23-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 129 OF 154	

PLACE THESE SERIES TERM CLOSE TO DRIVER: SB/SHASTA

SHASTA -> VESTA

131 9	ENET_TXD_R<0>	I59	MAKE_BASE=TRUE	ENET_TXD<0>	9 131 132
131 9	ENET_TXD_R<1>	I60	MAKE_BASE=TRUE	ENET_TXD<1>	9 131 132
131 9	ENET_TXD_R<2>	I61	MAKE_BASE=TRUE	ENET_TXD<2>	9 131 132
131 9	ENET_TXD_R<3>	I62	MAKE_BASE=TRUE	ENET_TXD<3>	9 131 132
131 9	ENET_TXD_R<4>	I63	MAKE_BASE=TRUE	ENET_TXD<4>	9 131 132
131 9	ENET_TXD_R<5>	I64	MAKE_BASE=TRUE	ENET_TXD<5>	9 131 132
131 9	ENET_TXD_R<6>	I65	MAKE_BASE=TRUE	ENET_TXD<6>	9 131 132
131 9	ENET_TXD_R<7>	I66	MAKE_BASE=TRUE	ENET_TXD<7>	9 131 132
131 9	ENET_TX_EN_R	I67	MAKE_BASE=TRUE	ENET_TX_EN	9 131 132
131 9	ENET_TX_ER_R	I68	MAKE_BASE=TRUE	ENET_TX_ER	9 131 132
131	ENET_CLK125M_GTX_R	I69	MAKE_BASE=TRUE	ENET_CLK125M_GTX	131 132
131	ENET_MDIO_R		MAKE_BASE=TRUE	ENET_MDIO	131 132

PLACE THESE SERIES TERM CLOSE TO DRIVER: VESTA

VESTA -> SHASTA

132	ENET_CLK125M_GBE_REF_R	I84	MAKE_BASE=TRUE	ENET_CLK125M_GBE_REF	131
132	ENET_CLK25M_TX_R	I70	MAKE_BASE=TRUE	ENET_CLK25M_TX	131
132	ENET_CLK125M_RX_R	I71	MAKE_BASE=TRUE	ENET_CLK125M_RX	131
132 131 9	ENET_RXD_R<0>	I72	MAKE_BASE=TRUE	ENET_RXD<0>	9 131
132 131 9	ENET_RXD_R<1>	I73	MAKE_BASE=TRUE	ENET_RXD<1>	9 131
132 131 9	ENET_RXD_R<2>	I74	MAKE_BASE=TRUE	ENET_RXD<2>	9 131
132 131 9	ENET_RXD_R<3>	I75	MAKE_BASE=TRUE	ENET_RXD<3>	9 131
132 131 9	ENET_RXD_R<4>	I76	MAKE_BASE=TRUE	ENET_RXD<4>	9 131
132 131 9	ENET_RXD_R<5>	I77	MAKE_BASE=TRUE	ENET_RXD<5>	9 131
132 131 9	ENET_RXD_R<6>	I78	MAKE_BASE=TRUE	ENET_RXD<6>	9 131
132 131 9	ENET_RXD_R<7>	I79	MAKE_BASE=TRUE	ENET_RXD<7>	9 131
132 131	ENET_RX_DV_R	I80	MAKE_BASE=TRUE	ENET_RX_DV	131
132 131	ENET_RX_ER_R	I81	MAKE_BASE=TRUE	ENET_RX_ER	131
132 131	ENET_COL_R	I82	MAKE_BASE=TRUE	ENET_COL	131
132 131	ENET_CRS_R	I83	MAKE_BASE=TRUE	ENET_CRS	131

ENET SERIES TERM

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	130	154

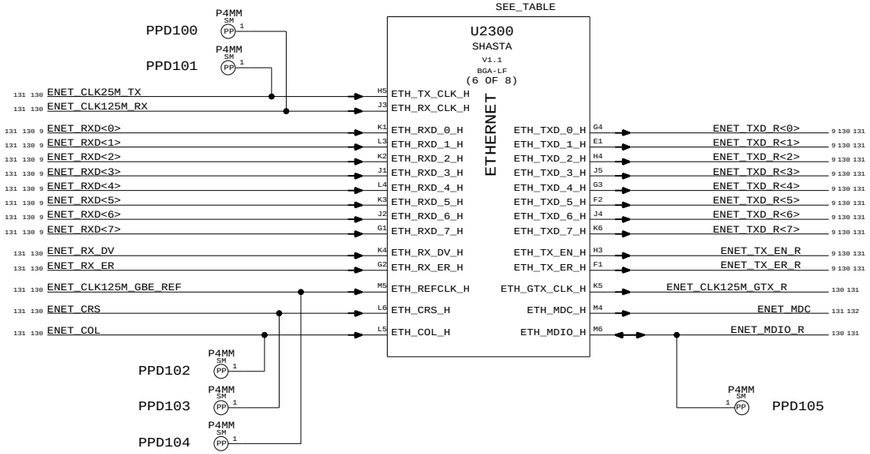
ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
I47	0.38mm SPACING	ENET_CLK25M_TX
I46	0.38mm SPACING	ENET_CLK125M_RX
I48	0.38mm SPACING	ENET_CLK125M_GBE_REF
I22	0.38mm SPACING	ENET_CLK125M_GTX
I50	0.38mm SPACING	ENET_CLK125M_GTX_R
I53	ENET_FW_2X	ENET_RXD_R<7..0>
I52	ENET_FW_3X	ENET_RX_DV_R
I53	ENET_FW_3X	ENET_RX_ER_R
I54	ENET_FW_2X	ENET_RXD<7..0>
I55	ENET_FW_3X	ENET_RX_DV
I56	ENET_FW_3X	ENET_RX_ER
I58	ENET_FW_2X	ENET_TXD_R<7..0>
I57	ENET_FW_3X	ENET_TX_EN_R
I59	ENET_FW_3X	ENET_TX_ER_R
I60	ENET_FW_2X	ENET_TXD<7..0>
I61	ENET_FW_3X	ENET_TX_EN
I62	ENET_FW_3X	ENET_TX_ER
I63	ENET_FW_3X	ENET_CRS_R
I64	ENET_FW_3X	ENET_COL_R
I65	ENET_FW_3X	ENET_CRS
I66	ENET_FW_3X	ENET_COL
I68	ENET_FW_3X	ENET_MDC
I41	ENET_FW_3X	ENET_MDIO
I42	ENET_FW_3X	ENET_MDIO_R
I43	ENET_FW_3X	R8405_1
I45	ENET_FW_3X	R8405_2
I44	ENET_FW_3X	R8407_2

Page Notes

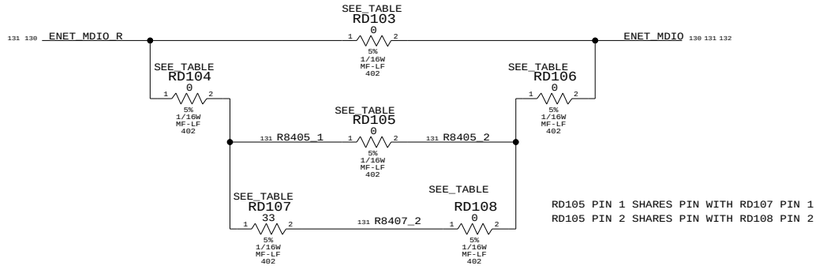
Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



RD103 PIN 1 SHARES PIN WITH RD104 PIN 1
RD103 PIN 2 SHARES PIN WITH RD106 PIN 2



RD105 PIN 1 SHARES PIN WITH RD107 PIN 1
RD105 PIN 2 SHARES PIN WITH RD108 PIN 2

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0-OHM,402,5%	RD103		ENET_MDIO_DELAY_0
116S0004	3	RES,0-OHM,402,5%	RD104,RD105,RD106		ENET_MDIO_DELAY_2NS
116S0004	3	RES,0-OHM,402,5%	RD104,RD108,RD106		ENET_MDIO_DELAY_4NS
116S0030	1	RES,33-OHM,402,5%	RD107		ENET_MDIO_DELAY_4NS

*

Shasta Ethernet

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 131 OF 154	

LAST_MODIFIED=Wed Nov 16 08:55:41 2005

DRAWING

TITLE=X11DAMAA

ABBREV=DRAWING

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
	0.38mm SPACING		ENET_CLK125M_GBE_REF_R
	0.38mm SPACING		ENET_CLK125M_RX_R
	0.38mm SPACING		ENET_CLK25M_TX_R
	ENET	ENET_MDI0	ENET_MDI_P<0>
	ENET	ENET_MDI0	ENET_MDI_N<0>
	ENET	ENET_MDI1	ENET_MDI_P<1>
	ENET	ENET_MDI1	ENET_MDI_N<1>
	ENET	ENET_MDI2	ENET_MDI_P<2>
	ENET	ENET_MDI2	ENET_MDI_N<2>
	ENET	ENET_MDI3	ENET_MDI_P<3>
	ENET	ENET_MDI3	ENET_MDI_N<3>
	0.38mm SPACING		VESTA_CLK25M_XTALI
	0.38mm SPACING		VESTA_CLK25M_XTALO
	0.38mm SPACING		VESTA_CLK25M_XTALO_R

Page Notes

Power aliases required by this page:
- =PP3V3_ENET
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET

Line To Line: 0.38mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.13mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Q63 APPLICATION IS ALL
139 17 7 =PP2V5_ENETFW
LD200 FERR-EMI-600-OHM SM
PP2V5_VESTA_BIASVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD201 0.1uF 20% 10V CERM 402
LD201 FERR-EMI-600-OHM SM
PP2V5_VESTA_XTALVDD1 6 VOLTAGE=2.5V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD202 10UF 10% 6.3V X5R 805
CD203 0.001uF 10% 50V CERM 402
XWD200 SM OMIT TP_VESTA_BIASVDD1 P4MM SM PPD239
XWD201 SM OMIT TP_VESTA_XTALVDD1 P4MM SM PPD201
XWD202 SM OMIT TP_VESTA_PLLVDD1 P4MM SM PPD238
PP1V2_VESTA_PLLVDD1 6 VOLTAGE=1.2V MIN_LINE_WIDTH=0.50mm MIN_NECK_WIDTH=0.38mm
CD204 0.001uF 20% 50V CERM 402
CD205 10UF 10% 6.3V X5R 805
Q63 APPLICATION IS ALL
LD202 FERR-EMI-600-OHM SM
7 17 139 =PP1V2_ENETFW
VESTA SPEC CALLS FOR 2.2UF, LOW ESR CAP
ESR < 0.5 ohms
PPD200 P4MM SM
131 130 ENET_CLK125M_GTX

XTALVDD1 BIASVDD1 PLLVDD1

SEE_TABLE
VESTA ENET
U1701
VESTA-V1.3
FBGA-200-LF
2 OF 3

GTXCLK	IPD	A4			
CLK125		D1	ENET_CLK125M_GBE_REF_R	130	132
TXC		A6	ENET_CLK25M_TX_R	130	132
RXC		C1	ENET_CLK125M_RX_R	130	132
131 130 9 ENET_TXD<0>	IPD	B6			
131 130 9 ENET_TXD<1>	IPD	C6			
131 130 9 ENET_TXD<2>	IPD	C7			
131 130 9 ENET_TXD<3>	IPD	D6			
131 130 9 ENET_TXD<4>	IPD	E6			
131 130 9 ENET_TXD<5>	IPD	C5			
131 130 9 ENET_TXD<6>	IPD	B5			
131 130 9 ENET_TXD<7>	IPD	A5			
TXD[0]			RXD[0]	F4	ENET_RXD_R<0> 9 130 131
TXD[1]			RXD[1]	F5	ENET_RXD_R<1> 9 130 131
TXD[2]			RXD[2]	E5	ENET_RXD_R<2> 9 130 131
TXD[3]			RXD[3]	E4	ENET_RXD_R<3> 9 130 131
TXD[4]			RXD[4]	E3	ENET_RXD_R<4> 9 130 131
TXD[5]			RXD[5]	D5	ENET_RXD_R<5> 9 130 131
TXD[6]			RXD[6]	D4	ENET_RXD_R<6> 9 130 131
TXD[7]			RXD[7]	D3	ENET_RXD_R<7> 9 130 131
131 130 9 ENET_TX_EN	IPD	B4			
131 130 9 ENET_TX_ER	IPD	C4			
TX_EN	IPD		RX_DV	D2	ENET_RX_DV_R 130 131
TX_ER	IPD		RX_ER	C2	ENET_RX_ER_R 130 131
131 ENET_MDC		G1			
131 130 ENET_MDIO		G2			
MDC	IPD		COL	F3	ENET_COL_R 130 131
MDIO	IPU		CRS	G3	ENET_CRS_R 130 131
VESTA_ENET_LOWPWR		H5			
LOWPWR	IPD		RBC0	A3	TP_VESTA_RBC0 9
IPD=INTERNAL PULL-DOWN			RBC1	B3	TP_VESTA_RBC1 9
IPU=INTERNAL PULL-UP					
9 TP_VESTA_PHYA<0>		L5			
9 TP_VESTA_PHYA<1>		L4			
9 TP_VESTA_PHYA<2>		L3			
9 TP_VESTA_PHYA<3>		L2			
9 TP_VESTA_PHYA<4>		L1			
PHYA[0]	IPD		TRD+[0]	R4	ENET_MDI_P<0> 132 136
PHYA[1]	IPD		TRD-[0]	R5	ENET_MDI_N<0> 132 136
PHYA[2]	IPD		TRD+[1]	R7	ENET_MDI_P<1> 132 136
PHYA[3]	IPD		TRD-[1]	R6	ENET_MDI_N<1> 132 136
PHYA[4]	IPD		TRD+[2]	R8	ENET_MDI_P<2> 132 136
			TRD-[2]	R9	ENET_MDI_N<2> 132 136
9 TP_VESTA_EN_10B		K3			
9 TP_VESTA_RGMIIEN		B8			
9 TP_VESTA_FDX		C8			
9 TP_VESTA_F1000		K4			
9 TP_VESTA_SPD0		K5			
9 TP_VESTA_MANMS		D9			
9 TP_VESTA_HUB		A9			
9 TP_VESTA_ER		H3			
EN_10B	IPD		TRD+[3]	R11	ENET_MDI_P<3> 132 136
RGMIIEN	IPD		TRD-[3]	R10	ENET_MDI_N<3> 132 136
FDX	IPU				
F1000	IPU				
SPD0	IPD				
MANMS	IPD				
HUB	IPD				
ER	IPD				
INTR*/ENERGYDET		D10	ENET_ENERGYDET 24		
IPU SLAVE*/AN_EN		C10	TP_VESTA_AN_EN 9		
IPD QUALITY*/TXC_RXC_DELAY		A8	TP_VESTA_TXC_RXC_DELAY 9		
9 TP_VESTA_TEST<0>		M4			
9 TP_VESTA_TEST<1>		M5			
9 TP_VESTA_TVCO		N3			
TEST[0]			IPD LINK1*	A10	TP_VESTA_LINK1_L 9
TEST[1]			IPD LINK2*	B11	TP_VESTA_LINK2_L 9
TVCO			IPD FDXLED*	B10	TP_VESTA_FDXLED_L 9
			IPU XMTLED*	B12	TP_VESTA_XMTLED_L 136
			IPU ACTLED*	C11	TP_VESTA_ACTLED_L 136
Put crystal circuit close to PHY					
132 VESTA_CLK25M_XTALI		N2			
132 VESTA_CLK25M_XTALO_R		P2			
XTALI					
XTALO			RDAC1	R1	VESTA_RDAC1_PD
XTALGND BIASGND PLLGND1		P3 R2 N2			

RD213 1.24K 1% 1/16W MF-LF 402
RD209 0 5% 1/16W MF-LF 402
CRITICAL YD200 25.0000M 8X4.5MM-SM2
VESTA_CLK25M_XTALO 132
CD218 33pF 5% 50V CERM 402
CD219 33pF 5% 50V CERM 402
CRYSTAL LOAD CAPACITANCE IS 20PF

TERMINATION OFF PAGE

Q63 APPLICATION IS ALL
139 17 7 =PP3V3_ENETFW
RD204 1K 1% 1/16W MF-LF 402
136 132 7 =PP3V3_ENET
RD250 1.5K 5% 1/16W MF-LF 402
QD200 2N7002DW-X-F SOT-363
CD206 1UF 10% 6.3V CERM 402
VESTA_ENET_LOWPWR
17 VESTA_RESET_H

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

LAST_MODIFIED=Wed Nov 16 09:40:36 2005

DRAWING
TITLE=SCHEMATIC
ASSEMBLY=SCHEMATIC

Vesta Ethernet PHY

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 132 OF 154	

EXTRA CONSTRAINTS TO SUPPLEMENT THE THE MISSING NET PHYSICAL FROM EARLIER PAGE

NET_PHYSICAL_TYPE

U295	ENET	ENET_MDI_P<0>	132 136
U296	ENET	ENET_MDI_N<0>	132 136
U297	ENET	ENET_MDI_P<1>	132 136
U298	ENET	ENET_MDI_N<1>	132 136
U299	ENET	ENET_MDI_P<2>	132 136
U300	ENET	ENET_MDI_N<2>	132 136
U301	ENET	ENET_MDI_P<3>	132 136
U302	ENET	ENET_MDI_N<3>	132 136

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0253	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	17_INCH_LCD
514-0254	1	CON,RJ-45 7 DEGRESS	JD600	CRITICAL	20_INCH_LCD

PUT DEVELOPMENT LEDS ON TOP SIDE OF BOARD

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD601 330 5% 1/10W MF-LF 603
LED8700_P 9
DEVELOPMENT
LEDD600
GREEN-3.6MCD 2.0X1.25MM-SM

132 TP_VESTA_XMTLED_L = VESTA_XMTLED_L
MAKE_BASE=TRUE

LD600
FERR-EMI-600-OHM
SM
7 =PP2V5_ENET
PP2V5_ENET_CTAP
MIN_LINE_WIDTH=0.150mm
MIN_NECK_WIDTH=0.138mm
VOLTAGE=2.5V
CD600 0.1UF 20% 10V CERM 402
CD601 0.1UF 20% 10V CERM 402

7 GND_CHASSIS_RJ45
CD604 0.001UF 10% 50V CERM 402

ENET TERMINATION

PLACE THESE PARTS NEAR VESTA

136 132 ENET_MDI_P<0>
136 132 ENET_MDI_N<0>
RD604 49.9 1% 1/16W MF-LF 402
RD605 49.9 1% 1/16W MF-LF 402
ENET_MDI0

136 132 ENET_MDI_P<1>
136 132 ENET_MDI_N<1>
CD606 0.01UF 20% 16V CERM 402
RD606 49.9 1% 1/16W MF-LF 402
RD607 49.9 1% 1/16W MF-LF 402
ENET_MDI1

136 132 ENET_MDI_P<2>
136 132 ENET_MDI_N<2>
RD608 49.9 1% 1/16W MF-LF 402
RD609 49.9 1% 1/16W MF-LF 402
CD607 0.01UF 20% 16V CERM 402
ENET_MDI2

136 132 ENET_MDI_P<3>
136 132 ENET_MDI_N<3>
CD608 0.01UF 20% 16V CERM 402
RD610 49.9 1% 1/16W MF-LF 402
RD611 49.9 1% 1/16W MF-LF 402
ENET_MDI3
CD609 0.01UF 20% 16V CERM 402

(514-0253)
OMIT
JD600
JFM38V10-0112-4F
F-ANG-TH

PRIMARY
13
11
5 ENET_CTAP
6 ENET_CTAP
1 MDI_0+
2 MDI_0-
3 MDI_1+
4 MDI_1-
7 MDI_2+
8 MDI_2-
9 MDI_3+
10 MDI_3-
12
RJ45 CHIP SIDE

1CT:1CT
75 OHM
SECONDARY
J1
J2
J3
J4
J5
J6
J7
J8
RJ45 CABLE SIDE

SHIELD 1000PF, 2000V

CD605 0.001UF 10% 50V CERM 402

136 132 7 =PP3V3_ENET
DEVELOPMENT
RD603 330 5% 1/10W MF-LF 603
LED8701_P 9
DEVELOPMENT
LEDD601
GREEN-3.6MCD 2.0X1.25MM-SM

132 TP_VESTA_ACTLED_L = VESTA_ACTLED_L
MAKE_BASE=TRUE

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

ZHD690 HOLE-VIA
ZHD691 HOLE-VIA
ZHD692 HOLE-VIA
ZHD693 HOLE-VIA

ETHERNET CONNECTOR

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 136 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR
	FNET_FW_2X	
	FNET_FW_3X	
	FNET_FW_3X	
	FNET_FW_2X	
	FNET_FW_3X	
	FNET_FW_3X	
	FNET_FW_3X	
	FNET_FW_3X	
	0.38mm_SPACING	
	0.38mm_SPACING	
	0.38mm_SPACING	

FW_DATA<7..0> 138 139
FW_CTL_S<1..0> 138 139
FW_CTL<1..0> 138 139
FW_DATA_R<7..0> 139
FW_CTL_R<1..0> 139
FW_LPS 138 139
FW_LREQ 138 139
FW_PINT 138 139
FW_CLK98M_LCLK 138 139
FW_CLK98M_PCLK 138 139
FW_CLK98M_LCLK_R 138

Page Notes

Power aliases required by this page:
- _PP2V5_PWRON_SB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

119 24 23 7 =PP2V5_PWRON_SB

CD800 0.1uF 20% 10V CERM 402
CD801 0.1uF 20% 10V CERM 402
CD802 0.1uF 20% 10V CERM 402

FWVDDP

U2300
SHASTA
V1.1
BGA-LF
SEE TABLE (7 OF 8)

FIREWIRE

PHY_DATA_0_H	N4	FW_DATA<0>	138 139
PHY_DATA_1_H	P5	FW_DATA<1>	138 139
PHY_DATA_2_H	N1	FW_DATA<2>	138 139
PHY_DATA_3_H	M7	FW_DATA<3>	138 139
PHY_DATA_4_H	N6	FW_DATA<4>	138 139
PHY_DATA_5_H	L1	FW_DATA<5>	138 139
PHY_DATA_6_H	M3	FW_DATA<6>	138 139
PHY_DATA_7_H	L2	FW_DATA<7>	138 139
PHY_CTL_0_H	N2	139 138 FW_CTL_S<0>	RD801 0 5% 1/16W MF-LF 402 FW_CTL<0> 138 139
PHY_CTL_1_H	N3	139 138 FW_CTL_S<1>	RD802 0 5% 1/16W MF-LF 402 FW_CTL<1> 138 139
PHY_LPS_H	P6	FW_LPS	138 139
PHY_LREQ_H	P1	FW_LREQ	138 139
PHY_SCLK_H	P2	139 138 FW_CLK98M_PCLK	
PHY_PINT_L	P3	139 138 FW_PINT	
PHY_LCLK_H	R1	138 FW_CLK98M_LCLK_R	RD800 22 5% 1/16W MF-LF 402 FW_CLK98M_LCLK 138 139
PHY_LINKON_L	N7	FW_LINKON	139

Shasta FireWire

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 138 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:38 2005

DRAWING

TITLE=SCHEMA

ABBREV=SHAWING

ELECTRICAL_CONSTRAINT_SET	NET_PHYSICAL_TYPE	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)		0.38mm SPACING		FW_CLK98M_PCLK_R 139
	FW	FW	FW_TPA0	FW_TPA_P<0> 139 140
	FW	FW	FW_TPA0	FW_TPA_N<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_P<0> 139 140
	FW	FW	FW_TPB0	FW_TPB_N<0> 139 140
	FW	FW	FW_TPA1	FW_TPA_P<1> 139 140
	FW	FW	FW_TPA1	FW_TPA_N<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_P<1> 139 140
	FW	FW	FW_TPB1	FW_TPB_N<1> 139 140
ETHERNET SPACING TO ROUTE ON LAYER 6	FW	FW	FW_TPA2	FW_TPA_P<2> 139 140
	FW	FW	FW_TPA2	FW_TPA_N<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_P<2> 139 140
	FW	FW	FW_TPB2	FW_TPB_N<2> 139 140
		0.38mm SPACING		VESTA_CLK24M_XTALI 139
		0.38mm SPACING		VESTA_CLK24M_XTALO 139
		0.38mm SPACING		VESTA_CLK24M_XTALO_R 139
	FW_CTL			FW_CTL_S<1..0> 138
100R	FW_CTL			FW_CTL<1..0> 138 139
140R	FW_CTL			FW_CTL_R<1..0> 138 139
441R				

Page Notes

Power aliases required by this page:
- =PPFW_PHY
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta.
  See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta.
  See straps table for more information.

Net Spacing Type: FW

NOTE: Target differential impedance for FW data pairs is 110 ohms.

VESTA CONFIG STRAPS:

FW_PWR_CLASS_MSB - FIREWIRE POWER CLASS
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)

FW_DS_ONLY_P0 - PORT 0 DATA/STROBE mode only
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)

ESDET[0]
1=PORTS 1 AND 2 DS ONLY
0=PARTS 1 AND 2 BI-LINGUAL
ESDET[1]
1=PORT 1 PRESENT
0=PORT 1 NOT PRESENT
ESDET[2]
1=PORT 2 PRESENT
0=PORT 2 NOT PRESENT

CRYSTAL LOAD CAPACITANCE IS 12PF

DRAWING	
LAST_MODIFIED	Wed Nov 16 09:40:39 2005

Vesta FireWire PHY

SYNC_MASTER=Q63 SYNC_DATE=08/01/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 139 OF 154	

NET_TYPE SPACING	PHYSICAL	DIFFERENTIAL_PAIR		
T401 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_P_FL	140
T400 FW	FW	FW_TPA0_FL	FW_PORT0_TPA_N_FL	140
T402 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_P_FL	140
T404 FW	FW	FW_TPB0_FL	FW_PORT0_TPB_N_FL	140
T403 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_P_FL	140
T405 FW	FW	FW_TPA1_FL	FW_PORT1_TPA_N_FL	140
T407 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_P_FL	140
T406 FW	FW	FW_TPB1_FL	FW_PORT1_TPB_N_FL	140

7 =PP12V_ALL_FW

8 WATTS MAX
12 VOLTS

RE056 1.3 1 2 20% 1W FF 2512
PP12V_FW MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=12V MAKE_BASE=TRUE

I443 = =PPFW_PHY 139
TO FW CDS PIN (CABLE POWER DETECT)

DE000 MURS320XXG SMC
FW_VP_R MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM MAKE_BASE=TRUE VOLTAGE=24V

CE009 0.1UF 10% 50V X7R 603-1
FW_VP MAX IS 24V

CRITICAL
RE002 1.3 1 2 20% 1W FF 2512
FW_VP MIN_LINE_WIDTH=0.8MM MIN_NECK_WIDTH=0.25MM VOLTAGE=24V

FE002 0.75AMP-13.2V MINISMD-LF
PPFW_PORT0_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

DESIGNED WITH INTENTION TO RESIZE FUSE LIMITS EQUAL FW SPEC 1.5A LIMIT

FE000 1.5AMP-33V SM-LF
PPFW_PORT1_VP MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V

POSSIBLE CURRENT SHARING SCENARIO
KCL = CABLE POWER + SYSTEM POWER = > 1.5 AMPS

Termination

Place close to FireWire PHY

VOLTAGE=1.86V
139 FW_TPBIAS<1> VOLTAGE=1.86V
139 FW_TPBIAS<0> VOLTAGE=1.86V

CE050 1UF 10% 6.3V CERM 402
CE060 1UF 10% 6.3V CERM 402

RE050 56.2 1% 1/10W MF-LF 402
RE051 56.2 1% 1/16W MF-LF 402
RE060 56.2 1% 1/16W MF-LF 402
RE061 56.2 1% 1/16W MF-LF 402

139 FW_TPA_P<0> MAKE_BASE=TRUE FW_PORT0_TPA_P 140
139 FW_TPA_N<0> MAKE_BASE=TRUE FW_PORT0_TPA_N 140
139 FW_TPB_P<0> MAKE_BASE=TRUE FW_PORT0_TPB_P 140
139 FW_TPB_N<0> MAKE_BASE=TRUE FW_PORT0_TPB_N 140
139 FW_TPA_P<1> MAKE_BASE=TRUE FW_PORT1_TPA_P 140
139 FW_TPA_N<1> MAKE_BASE=TRUE FW_PORT1_TPA_N 140
139 FW_TPB_P<1> MAKE_BASE=TRUE FW_PORT1_TPB_P 140
139 FW_TPB_N<1> MAKE_BASE=TRUE FW_PORT1_TPB_N 140

RE052 56.2 1% 1/10W MF-LF 402
RE053 56.2 1% 1/16W MF-LF 402
RE062 56.2 1% 1/16W MF-LF 402
RE063 56.2 1% 1/16W MF-LF 402

FW_TPA_C<0> VOLTAGE=0V
RE054 4.99K 1% 1/16W MF-LF 402
CE054 270pF 5% 25V CERM 402

FW_TPA_C<1> VOLTAGE=0V
RE064 4.99K 1% 1/16W MF-LF 402
CE064 270pF 5% 25V CERM 402

3rd TPA/TPB pair unused

139 FW_TPBIAS<2> — NC_FW_TPBIAS2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPA_P<2> — NC_FW_TPA_P2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPA_N<2> — NC_FW_TPA_N2 MAKE_BASE=TRUE NO_TEST=YES
139 FW_TPB_P<2>
139 FW_TPB_N<2> — FW_TPB2_PD MAKE_BASE=TRUE NO_TEST=YES

RE070 1K 5% 1/10W MF-LF 402

ESD Rail

CALCULATION = 220 OHMS, THERE'S ALREADY A 215 IN THE DESIGN, SO I'M USING 215 INSTEAD

7 =PP3V3_FW — RE090 215 1% 1/10W MF-LF 402 — PP3V3_FW_ESD_F VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm — LE090 400-OHM-EMI SM-1 — PP3V3_FW_ESD 140 VOLTAGE=3.3V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

DE090 SOT23 BZX84C2V7-X-F

[LATE VG NOTES]
CURRENT THROUGH THE BIAS RESISTOR SHOULD BE 5MA FOR A VOLTAGE DROP TO 2.2V
IT IS 2.2V INSTEAD OF 2.7V BECAUSE THE SNAPBACK ESD DIODES HAVE A .5V DROP

ZHE090 HOLE-VIA
ZHE091 HOLE-VIA
ZHE092 HOLE-VIA
ZHE093 HOLE-VIA

SPARE GND VIAS FOR LAYER TRAVERSALS DURING ROUTING

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD

DPE010 BAV99DW-X-F SOT-363
CE010 0.001UF 10% 50V CERM 402
CE011 0.001UF 10% 50V CERM 402

140 FW_PORT0_TPA_P
140 FW_PORT0_TPA_N
140 FW_PORT0_TPB_P
140 FW_PORT0_TPB_N

FLE010 120-OHM 2012 SYM_VER-1
FLE011 120-OHM 2012 SYM_VER-1

140 PP3V3_FW_ESD

DPE011 BAV99DW-X-F SOT-363
CE012 0.001UF 10% 50V CERM 402
CE013 0.001UF 10% 50V CERM 402

LE010 FERR-160-OHM 1206-LF
PORT 0 1394A OMIT

JE000 UF01613-M33-4F F-ST-TH

140 FW_PORT0_TPA_P_FL — TPO (TPA+)
140 FW_PORT0_TPA_N_FL — TPO# (TPA-)
140 FW_PORT0_TPB_P_FL — TPI (TPB+)
140 FW_PORT0_TPB_N_FL — TPI# (TPB-)
PPFW_PORT0_VP_FL — VP
VGND
7 8 9 10

FW_VP MAX IS 24V
CE015 0.1UF 10% 50V X7R 603-1
CE016 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

"Snapback" & "Late VG" Protection

140 PP3V3_FW_ESD

DPE020 BAV99DW-X-F SOT-363
CE020 0.001UF 10% 50V CERM 402
CE021 0.001UF 10% 50V CERM 402

140 FW_PORT1_TPA_P
140 FW_PORT1_TPA_N
140 FW_PORT1_TPB_P
140 FW_PORT1_TPB_N

FLE020 120-OHM 2012 SYM_VER-1
FLE021 120-OHM 2012 SYM_VER-1

140 PP3V3_FW_ESD

DPE021 BAV99DW-X-F SOT-363
CE022 0.001UF 10% 50V CERM 402
CE023 0.001UF 10% 50V CERM 402

PPFW_PORT1_VP 140
LE020 FERR-160-OHM 1206-LF
PORT 1 1394A OMIT

JE001 UF01613-M33-4F F-ST-TH

140 FW_PORT1_TPA_P_FL — TPO (TPA+)
140 FW_PORT1_TPA_N_FL — TPO# (TPA-)
140 FW_PORT1_TPB_P_FL — TPI (TPB+)
140 FW_PORT1_TPB_N_FL — TPI# (TPB-)
PPFW_PORT1_VP_FL — VP
MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=24V
VGND
7 8 9 10

CE025 0.1UF 10% 50V X7R 603-1
CE026 0.01UF 20% 16V CERM 402

514-0251 20_INCH_VERSION SHOWN
GND_CHASSIS_FIREWIRE 7 140

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0248	1	CON,1394A 7 DEGREES	JE000	CRITICAL	17_INCH_LCD
514-0248	1	CON,1394A 7 DEGREES	JE001	CRITICAL	17_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE000	CRITICAL	20_INCH_LCD
514-0251	1	CON,1394A 7 DEGREES	JE001	CRITICAL	20_INCH_LCD

FIREWIRE CONNECTORS

SYNC_MASTER=FINO-DC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 140 OF 154	

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
	USB2	USB2_S	USB2_0	USB2_P<0> 142 143
	USB2	USB2_S	USB2_0	USB2_N<0> 142 143
	USB2	USB2_S	USB2_1	USB2_P<1> 142 143
	USB2	USB2_S	USB2_1	USB2_N<1> 142 143
	USB2	USB2_S	USB2_2	USB2_P<2> 142 143
	USB2	USB2_S	USB2_2	USB2_N<2> 142 143
	USB2	USB2	USB2_3	USB2_P<3> 142 143
	USB2	USB2	USB2_3	USB2_N<3> 142 143
	USB2	USB2	USB2_4	USB2_P<4> 142 143
	USB2	USB2	USB2_4	USB2_N<4> 142 143
	0.38mm SPACING			NEC_CLK30M_XT1 142
	0.38mm SPACING			NEC_CLK30M_XT2 142
	0.38mm SPACING			NEC_CLK30M_XT2_R 142

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 0.50mm
Length Tolerance: 1.27mm
Primary Max Sep: 0.19mm
Secondary Max Sep: 2.54mm
Secondary Length: 12.70mm

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

Q63 USB PORT ALLOCATION
REAR USB (PORT #0)
FRONT PANEL USB (PORT #1)
REAR USB (PORT #2)
REAR USB (PORT #3)

U2300 SHASTA V1.1 BGA-LF (8 OF 8)

NC0 P7 TP_SB<0> 6
NC1 P8 TP_SB<1> 6
NC2 R3 TP_SB<2> 6
NC3 R4 TP_SB<3> 6
NC4 R5 TP_SB<4> 6
NC5 R6 TP_SB<5> 6
NC6 R7 TP_SB<6> 6
NC7 R8 TP_SB<7> 6
NC8 T1 TP_SB<8> 6
NC9 T2 TP_SB<9> 6
NC10 T3 TP_SB<10> 6
NC11 T4 TP_SB<11> 6
NC12 T5 TP_SB<12> 6
NC13 T6 TP_SB<13> 6
NC14 T7 TP_SB<14> 6
NC15 T8 TP_SB<15> 6
NC16 U1 TP_SB<16> 6
NC17 U2 TP_SB<17> 6
NC18 U3 TP_SB<18> 6
NC19 U4 TP_SB<19> 6
NC20 U5 TP_SB<20> 6
NC21 U6 TP_SB<21> 6
NC22 V1 TP_SB<22> 6
NC23 V2 TP_SB<23> 6
NC24 V3 TP_SB<24> 6
NC25 V4 TP_SB<25> 6
NC26 W1 TP_SB<26> 6
NC27 W3 TP_SB<27> 6
NC28 Y1 TP_SB<28> 6
NC29 Y3 TP_SB<29> 6

LE235 FERR-EMI-100-OHM SM
RE235 4.7 5% 1/10W MF-LF 603
PP3V3_PWRON_NEC_AVDD VOLTAGE=3.3V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM
CE235 10UF 10% X5R 805
CE236 0.1uF 20% CERM 402
CE237 0.1uF 20% CERM 402
XWE200 SM OMIT
TP_NEC_AVDD
P4MM PPE2000
MINIMIZE TRACE LENGTH OF CAPS FROM AVDD TO AVSS PINS
GND_NEC_AVSS_R 6 142
145 144 142 7 =PP3V3_PWRON_USB

CE220 10UF 10% X5R 805
CE221 CE222 CE223 CE224 CE225 CE226 CE227 CE228 CE229 CE230 0.1uF 20% CERM 402

P2 P3 P12 A13 A12 A3 E2 N8 L13 J13 H13 F13 D13 G12 H4 D7 — VDD
N10 N12 — AVDD

CRITICAL
UC200 NEC_UPD720101_USB2 FBGA-LF

RE200 RE201 RE202 RE203 RE204 RE205 RE206 RE207 RE208 RE209 36 1% 1/16W MF-LF 402

RSDM1 M14 143 USB_NEC_N<0>
DM1 M13 (USB2_Nc0s) USB2_N<0> 142 143
DP1 L14 (USB2_Pc0s) USB2_P<0> 142 143
RSDP1 K13 143 USB_NEC_P<0>

P4MM PPE2002
RSDM2 K14 143 USB_NEC_N<1>
DM2 K12 (USB2_Nc1s) USB2_N<1> 142 143
DP2 J14 (USB2_Pc1s) USB2_P<1> 142 143
RSDP2 J12 143 USB_NEC_P<1>

P4MM PPE2001
RSDM3 H11 143 USB_NEC_N<2>
DM3 G11 (USB2_Nc2s) USB2_N<2> 142 143
DP3 G13 (USB2_Pc2s) USB2_P<2> 142 143
RSDP3 G14 143 USB_NEC_P<2>

40.2 OHM RESISTORS ON PORT 2 FOR EVALUATION

RSDM4 F12 143 USB_NEC_N<3>
DM4 F14 (USB2_Nc3s) USB2_N<3> 142 143
DP4 E12 (USB2_Pc3s) USB2_P<3> 142 143
RSDP4 E14 143 USB_NEC_P<3>

RSDM5 E13 143 USB_NEC_N<4>
DM5 D14 (USB2_Nc4s) USB2_N<4> 142 143
DP5 C13 (USB2_Pc4s) USB2_P<4> 142 143
RSDP5 C14 143 USB_NEC_P<4>

BLUTOOTH CONNECTOR,(PORT #4)

145 144 142 7 =PP3V3_PWRON_USB
RE210 33K 5% 1/16W MF-LF 402
RPE210 10K 5% 1/16W SM-LF

143 USB2_OC<0> (USB2_OC<0>) B12 OCI1
143 USB2_OC<1> (USB2_OC<1>) B11 OCI2
143 USB2_OC<2> (USB2_OC<2>) B10 OCI3
USB2_OC<3> (USB2_OC<3>) A10 OCI4
USB2_OC<4> (USB2_OC<4>) B9 OCI5

143 USB2_PWREN<0> C12 PPON1
143 USB2_PWREN<1> A11 PPON2
143 USB2_PWREN<2> C11 PPON3
143 USB2_PWREN<3> C10 PPON4
143 USB2_PWREN<4> A9 PPON5

145 144 142 7 =PP3V3_PWRON_USB
RE240 1.5K 5% 1/16W MF-LF 402
RE241 1.5K 5% 1/16W MF-LF 402
NEC_NC1_PU P6 NC1
NEC_NC2_PU M6 NC2

142 NEC_CLK30M_XT1 L9 XT1/SCLK
142 NEC_CLK30M_XT2_R P8 XT2
RE245 100 1% 1/16W MF-LF 402
CRITICAL
YE245 30.0000M 8X4.5MM-SM1
NEC_CLK30M_XT2 142
CE245 22pF 5% 50V CERM 402
CE246 22pF 5% 50V CERM 402
SPEC SHOWS LOAD CAPACITANCE OF 16PF

B1 N1 P10 N14 H14 B14 A2 B2 N2 N13 B13 M11 L12 H12 D12 G4 J11 F11 D8 — VSS
XWE201 SM OMIT
P13 M12 N11 — AVSS
AVSS(R)
Tie to GND at ball N11

RREF P11 NEC_RREF_PD
RE238 9.09K 1% 1/16W MF-LF 402
MINIMIZE TRACE LENGTH TO PINS
GND_NEC_AVSS_R 6 142
VOLTAGE=0V
MIN_LINE_WIDTH=0.50mm
MIN_NECK_WIDTH=0.2MM

USB Host Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=07/05/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 142 OF 154	

LAST_MODIFIED=Wed Nov 16 09:40:41 2005
DRAWING
TITLE=KILOHANA
ABBREV=SRAWING

Page Notes

Power aliases required by this page:
- _PP5V_PWRON_USB
- _PP5V_PWRON_UDASH
- _PP3V3_PWRON_UDASH
- _PP3V3_PWRON_BT

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the USB pairs to their appropriate destinations and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

NOTE: USB pairs are NOT constrained on this page. It is assumed that the USB Host Controller page will provide the appropriate constraints to apply to entire USB D+/D- XNets.

neoBorg Implementation

NOTE: This design does not provide power control on USB ports 2-4. Rename USB controller outputs to indicate single-pin connections.

142 USB2_PWREN<0> — TP_USB2_PWREN<0> 6 MAKE_BASE=TRUE
142 USB2_PWREN<1> — TP_USB2_PWREN<1> 6 MAKE_BASE=TRUE
142 USB2_PWREN<2> — TP_USB2_PWREN<2> 6 MAKE_BASE=TRUE
142 USB2_PWREN<3> — TP_USB2_PWREN<3> 6 MAKE_BASE=TRUE
142 USB2_PWREN<4> — TP_USB2_PWREN<4> 6 MAKE_BASE=TRUE

External USB Ports

7 =PP5V_PWRON_USB

CRITICAL
UE300
TPS2024
SOI-LF
IN_0 OUT_0
IN_1 OUT_1
OUT_2
EN* OC*
GND

142 USB2_OC<0> — USB_OC MAKE_BASE=TRUE
142 USB2_OC<1>
142 USB2_OC<2>

96 PP5V_USB2
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

LE310 FERR-250-OHM SM
NOSTUFF CE310 150UF 20% 6.3V POLY SMD2
RE336 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_USB_PORT1
CE312 0.01UF 20% 16V CERM 402
CE313 0.01UF 20% 16V CERM 402

PP5V_USB2_PORT1_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

OMIT JE310 UB01123M23-4F F-ST-TH
PORT 1
514-0247
GND_CHASSIS_USB
MIN_NECK_WIDTH=0.2MM MIN_LINE_WIDTH=0.6MM VOLTAGE=0 7 143

LE312 120-OHM 2012 SYM_VER-1
142 USB2_N<0> — USB2_PORT1_N MAKE_BASE=TRUE
142 USB2_P<0> — USB2_PORT1_P MAKE_BASE=TRUE
143 USB2_PORT1_N_F
143 USB2_PORT1_P_F
NOSTUFF RE312 0 402
NOSTUFF RE313 0 402
RE310 15K 5% 1/16W MF-LF 402
RE311 15K 5% 1/16W MF-LF 402

LE320 FERR-250-OHM SM
NOSTUFF CE320 330UF 20% 6.3V POLY SMD
RE335 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_USB_PORT2
CE322 0.01UF 20% 16V CERM 402
CE323 0.01UF 20% 16V CERM 402

PP5V_USB2_PORT2_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

OMIT JE320 UB01123M23-4F F-ST-TH
PORT 2
514-0247
GND_CHASSIS_USB 7 143

LE322 120-OHM 2012 SYM_VER-1
142 USB2_N<1> — USB2_PORT2_N MAKE_BASE=TRUE
142 USB2_P<1> — USB2_PORT2_P MAKE_BASE=TRUE
143 USB2_PORT2_N_F
143 USB2_PORT2_P_F
NOSTUFF RE322 0 402
NOSTUFF RE323 0 402
RE320 15K 5% 1/16W MF-LF 402
RE321 15K 5% 1/16W MF-LF 402

LE330 FERR-250-OHM SM
PP5V_USB2_PORT3_F
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM

RE334 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_NECK_WIDTH=0.25MM MIN_LINE_WIDTH=0.6MM
GND_USB_PORT3
CE332 0.01UF 20% 16V CERM 402
CE333 0.01UF 20% 16V CERM 402

OMIT JE330 UB01123M23-4F F-ST-TH
PORT 3
514-0247
GND_CHASSIS_USB 7 143

LE332 120-OHM 2012 SYM_VER-1
142 USB2_N<2> — USB2_PORT3_N MAKE_BASE=TRUE
142 USB2_P<2> — USB2_PORT3_P MAKE_BASE=TRUE
143 USB2_PORT3_N_F
143 USB2_PORT3_P_F
NOSTUFF RE332 0 402
NOSTUFF RE333 0 402
RE330 15K 5% 1/16W MF-LF 402
RE331 15K 5% 1/16W MF-LF 402

FE301 0.75AMP-13.2V MINISMD-LF 740S0509 CRITICAL
LE340 FERR-250-OHM SM
7 =PP5V_PWRON_BNDI
VOLTAGE=5V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
PP5V_PWRON_BNDI 143
PP5V_BNDI LE340
CE344 10UF 20% 10V CERM 805-2
RE346 0 805 1/8W MF-LF 5%
VOLTAGE=0V MIN_LINE_WIDTH=0.6MM MIN_NECK_WIDTH=0.25MM
GND_BNDI 143
CE342 0.01UF 20% 16V CERM 402
CE343 0.01UF 20% 16V CERM 402
143 7 GND_CHASSIS_BNDI

USB_HUB IMPLIMENTS 15K PULLDOWNS INTERNAL SO THEY ARE NOT NEEDED HERE

NOSTUFF RE343 0 402
144 USB2_HUB_P<2> — LE342 120-OHM 2012
NOSTUFF RE342 0 402
144 USB2_HUB_N<2>
NOSTUFF RE354 0 402
144 USB2_HUB_P<3> — LE352 120-OHM 2012
NOSTUFF RE355 0 402
144 USB2_HUB_N<3>

FHB CONNECTOR
518S0324
JE350 53261-1498 M-RT-SM
153 AUD_MIC_IN_P_CONN 1
153 GND_AUDIO_MIC_CONN 2
153 AUD_MIC_IN_N_CONN 3
143 7 GND_CHASSIS_BNDI 4
5
143 7 GND_CHASSIS_BNDI 6
143 USB2_HUB_P_L<2> 7
143 USB2_HUB_N_L<2> 8
9
143 GND_BNDI 10
143 USB2_P_L<3> 11
143 USB2_N_L<3> 12
24 SB_GPIO14 13
143 PP5V_PWRON_BNDI 14
15
16

4-14-05
PLACE CE343, CE344 & LE340 NEAR JE350 PIN 14 IN THE ORDER LISTED, AND NOT ON BOTH SIDES OF THE PIN.

SENDS NEC USB PORT 3 TO BLUETOOTH MODULE
121 USB_BT_P — MAKE_BASE=TRUE — USB2_P<3> 142
121 USB_BT_N — MAKE_BASE=TRUE — USB2_N<3> 142
RE350 15K 5% 1/16W MF-LF 402
RE351 15K 5% 1/16W MF-LF 402

SENDS NEC CONTROLLER PORT 4 TO USB HUB UPSTREAM PORT
142 USB2_P<4> — MAKE_BASE=TRUE — USB2_HUB_P<0> 144
142 USB2_N<4> — MAKE_BASE=TRUE — USB2_HUB_N<0> 144
RE352 15K 5% 1/16W MF-LF 402
RE353 15K 5% 1/16W MF-LF 402

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
514-0294	3	USB RECEPTACLE,4P,UB1123-M23B-4F	JE310,JE320,JE330	CRITICAL	17_INCH_LCD
514-0295	3	USB RECEPTACLE,4P,UB1123-M33B-4F	JE310,JE320,JE330	CRITICAL	20_INCH_LCD

	ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	DIFFERENTIAL_PAIR	NET_PHYSICAL_TYPE	
I602	PROVIDED BY USB CONTROLLER	USB2	USB2_PORT1_F	USB2	USB2_PORT1_P_F 143
I603		USB2	USB2_PORT1_F	USB2	USB2_PORT1_N_F 143
I604		USB2	USB2_PORT2_F	USB2	USB2_PORT2_P_F 143
I605		USB2	USB2_PORT2_F	USB2	USB2_PORT2_N_F 143
I606		USB2	USB2_PORT3_F	USB2	USB2_PORT3_P_F 143
I607		USB2	USB2_PORT3_F	USB2	USB2_PORT3_N_F 143
I608		USB2	USB2_HUB_F	USB2	USB2_HUB_P_L<2> 143
I609		USB2	USB2_HUB_F	USB2	USB2_HUB_N_L<2> 143
I610		USB2	USB2_BNDI_F	USB2	USB2_P_L<3> 143
I611		USB2	USB2_BNDI_F	USB2	USB2_N_L<3> 143
I614		USB2	USB2_0_IC	USB2	USB_NEC_P<0> 142
I615		USB2	USB2_0_IC	USB2	USB_NEC_N<0> 142
I616		USB2	USB2_1_IC	USB2	USB_NEC_P<1> 142
I617		USB2	USB2_1_IC	USB2	USB_NEC_N<1> 142
I620		USB2	USB2_2_IC	USB2	USB_NEC_P<2> 142
I621		USB2	USB2_2_IC	USB2	USB_NEC_N<2> 142
I622		USB2	USB2_3_IC	USB2	USB_NEC_P<3> 142
I623		USB2	USB2_3_IC	USB2	USB_NEC_N<3> 142
I624		USB2	USB2_4_IC	USB2	USB_NEC_P<4> 142
I625		USB2	USB2_4_IC	USB2	USB_NEC_N<4> 142

DUE TO THESE NETS ARE ON A Q63 SHARED PAGE 124, THESE PROPERTIES FOR M23/M33 WERE PLACED ON THIS PAGE.

USB Device Interfaces

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 143 OF 154	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0257	1	USX2006-NU-01 CUSTOM MASK	UE400	CRITICAL	CARD_READER

ELECTRICAL_CONSTRAINT_SET	NET_SPACING_TYPE	NET_PHYSICAL_TYPE	DIFFERENTIAL_PAIR	
IN	USB2	USB2	USB2_HUB_1	USB2_HUB_P<1>
IN	USB2	USB2	USB2_HUB_1	USB2_HUB_N<1>
IN	USB2	USB2	USB2_HUB_2	USB2_HUB_P<2>
IN	USB2	USB2	USB2_HUB_2	USB2_HUB_N<2>
IN	USB2	USB2	USB2_HUB_3	USB2_HUB_P<3>
IN	USB2	USB2	USB2_HUB_3	USB2_HUB_N<3>
IN	0.38MM SPACING			XTAL_IN_CARD_READER
IN	0.38MM SPACING			XTAL_OUT_CARD_READER
IN	0.38MM SPACING			XTAL_OUT_CARD_READER_R
IN	0.38MM SPACING			XTAL_IN_USB_HUB
IN	0.38MM SPACING			XTAL_OUT_USB_HUB
IN	0.38MM SPACING			XTAL_OUT_USB_HUB_R

Flash Media Ctrl

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

NOTICE OF PROPRIETARY PROPERTY

THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING

I TO MAINTAIN THE DOCUMENT IN CONFIDENCE

II NOT TO REPRODUCE OR COPY IT

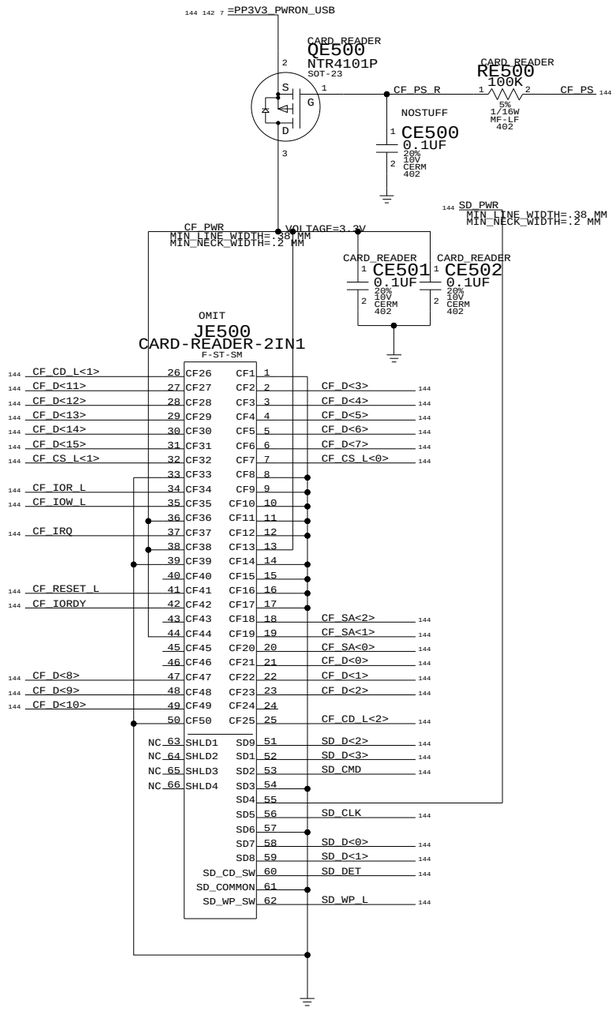
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 144 OF 154	

IF USING THE CARD READER, MUST CHANGE THESE BOM OPTIONS TO:

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION	
512S0010	1	CONN, MEDIA CARD M23	JE500	CRITICAL	CARD_READER	17_INCH_LCD
512S0012	1	CONN, MEDIA CARD M33	JE500	CRITICAL	CARD_READER	20_INCH_LCD



WRITE PROTECT AND CARD DETECT SWITCHES

CARD STATUS	WRITE PROTECT	WRITE ENABLE	CARD DETECT
NOT INSERTED	OPEN	OPEN	OPEN
FULLY INSERTED	OPEN	CLOSE	CLOSE

Flash Connector

SYNC_MASTER=FINO-PC SYNC_DATE=06/20/2005

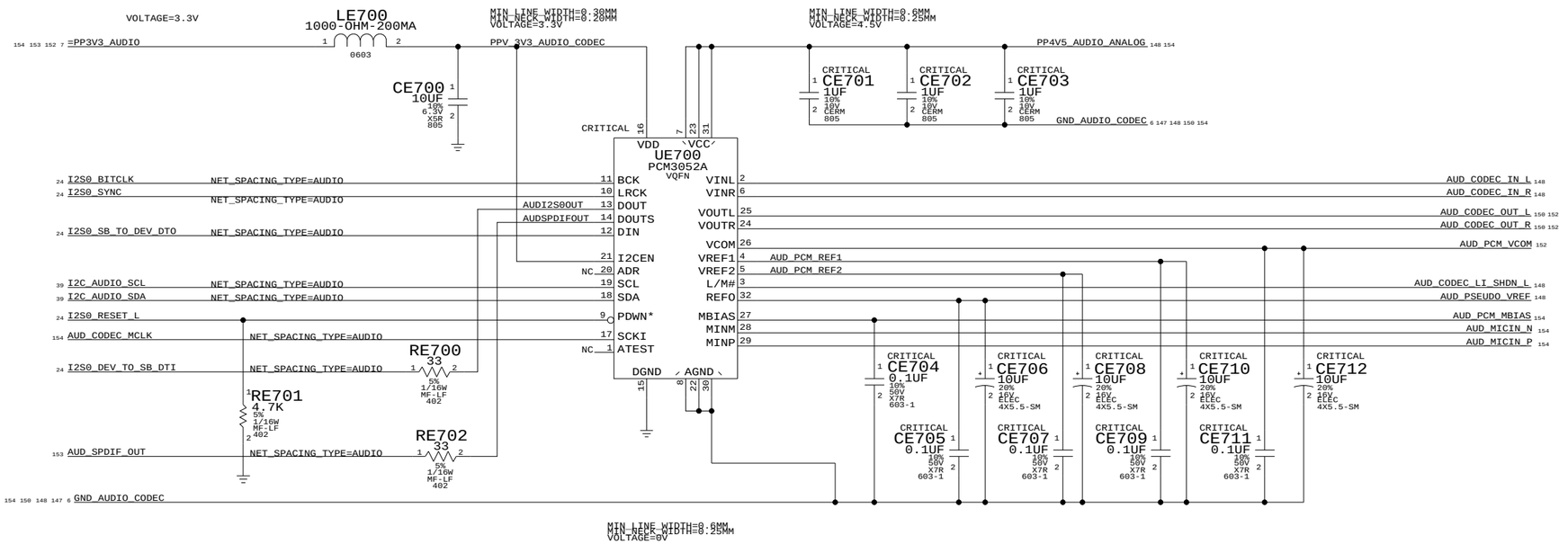
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE: NONE

SHT 145 OF 154

AUDIO CODEC
APPLE P/N 353S0933



AUDIO: CODEC

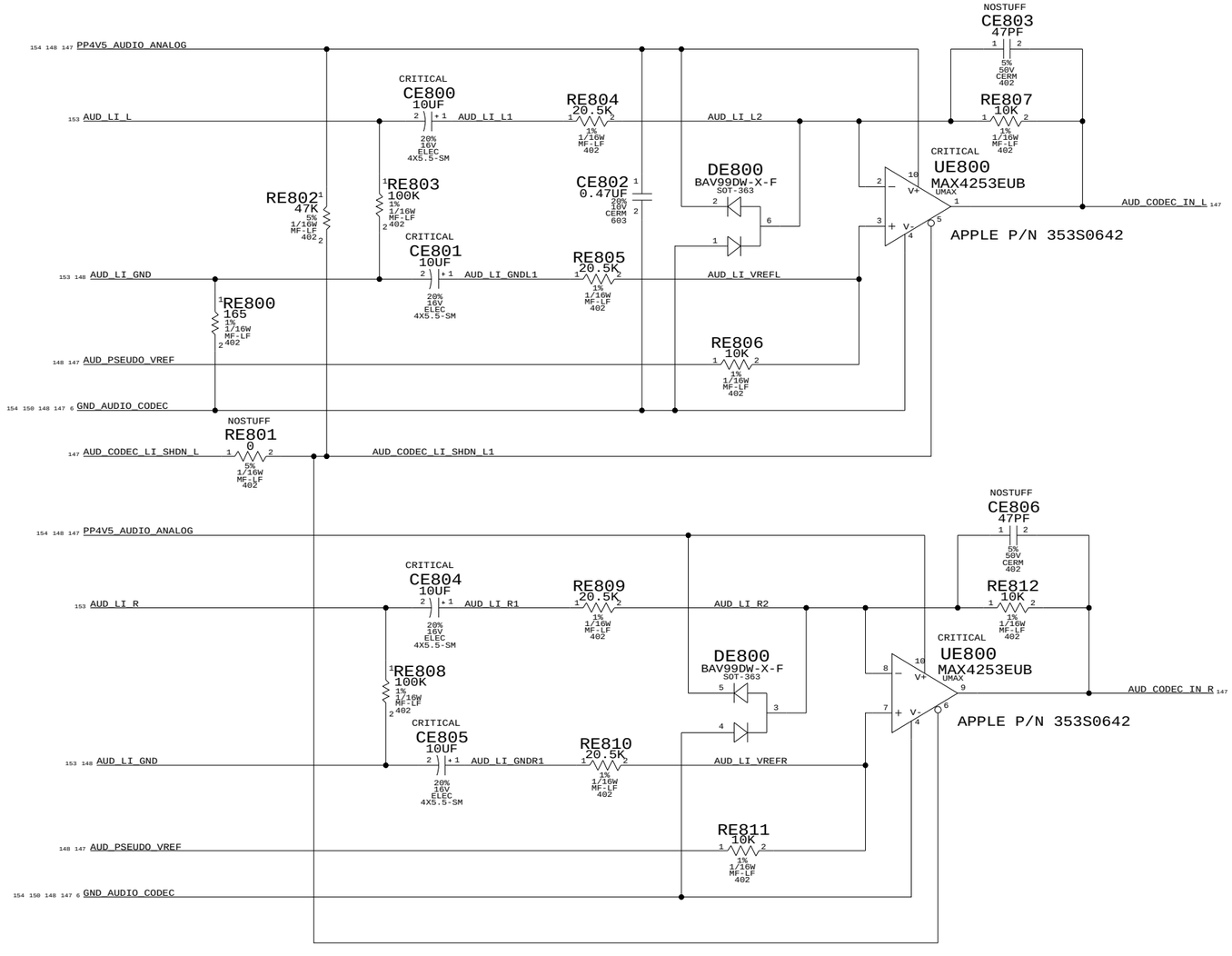
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 147 OF 154	

LINE IN PSEUDO-DIFFERENTIAL AMP

AV= 0.49



AUDIO: LINE INPUT AMP

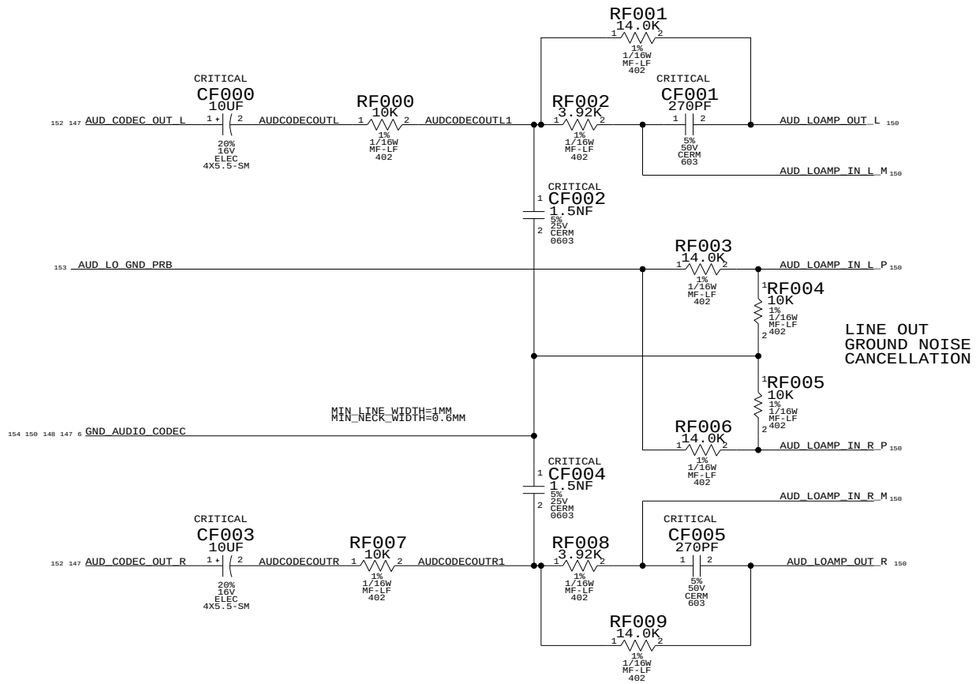
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 148 OF 154	

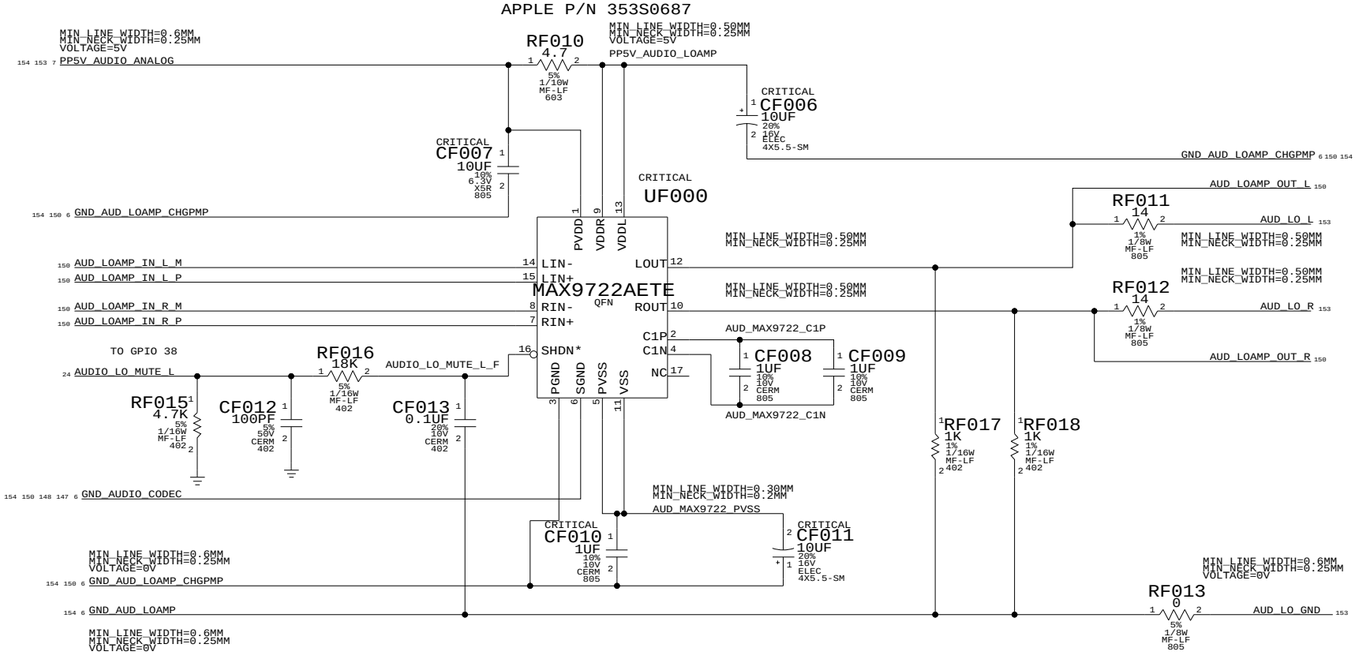
LINE OUT LOW-PASS FILTER

FC = 37 KHZ, HO = -1.4



LINE OUT AMP

APPLE P/N 353S0687



AUDIO: LINE OUT AMP

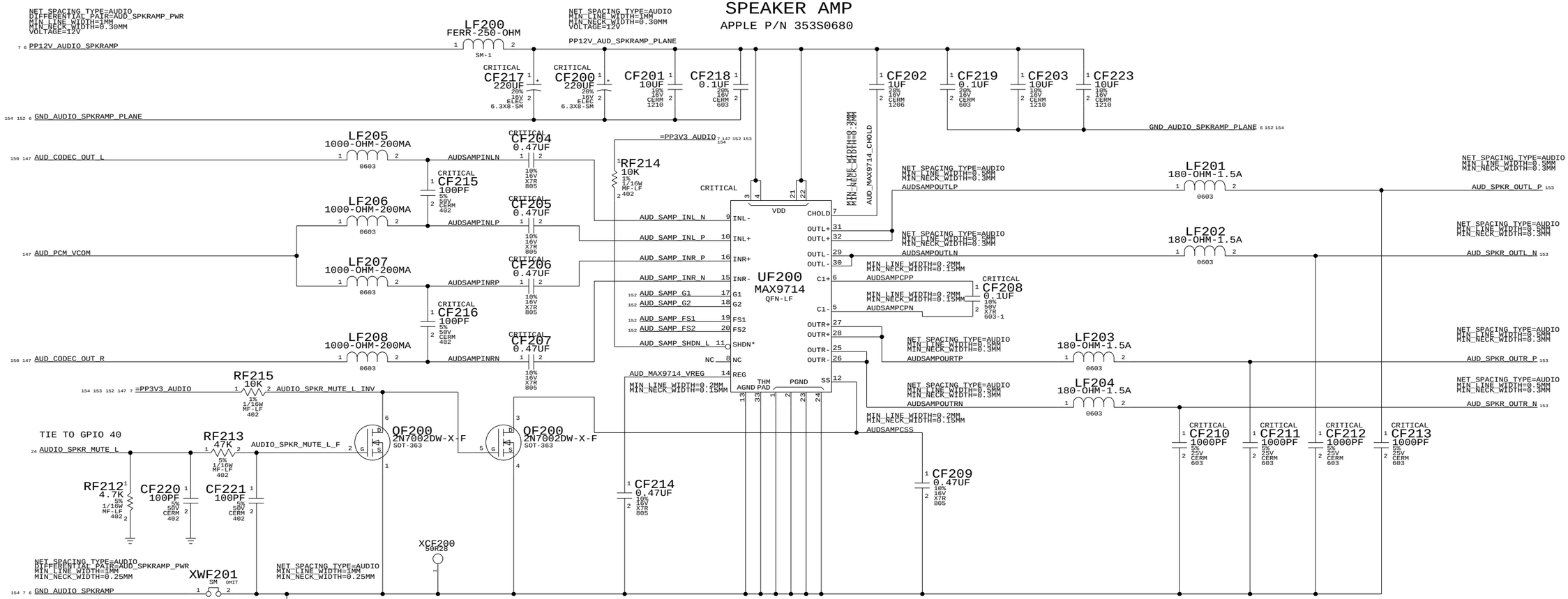
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT 150 OF 154	

SPEAKER AMP

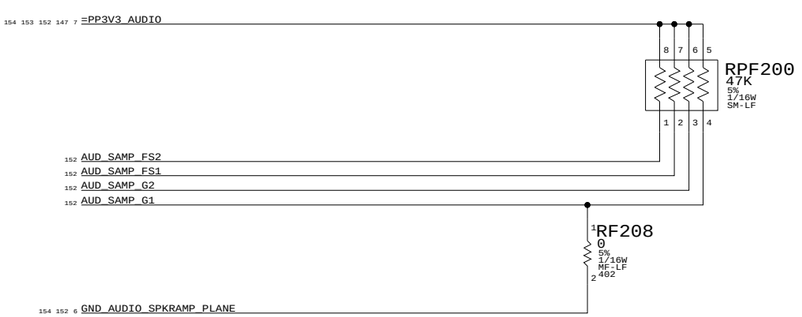
APPLE P/N 353S0680



GAIN SETTINGS: +19DB

MODULATION SETTING: LOW EMI

GAIN AND SWITCHING FREQUENCY STUFF OPTIONS



AUDIO: SPEAKER AMP

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

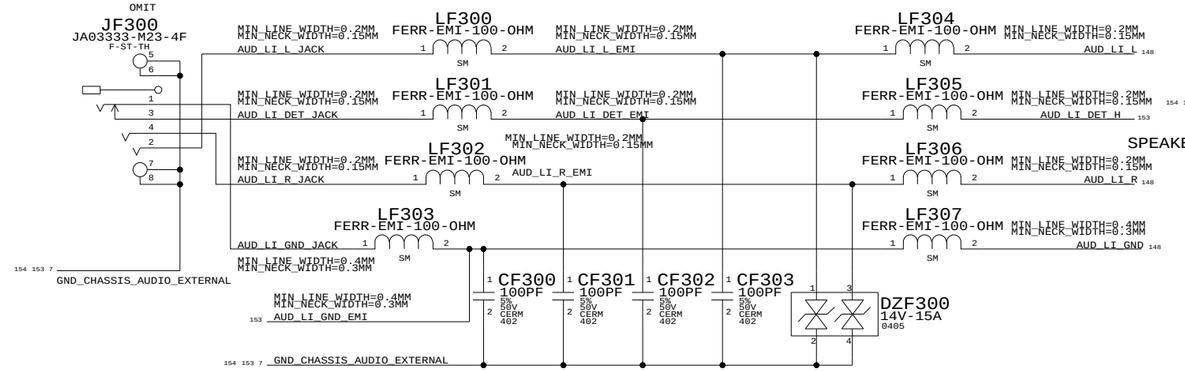
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	152	154

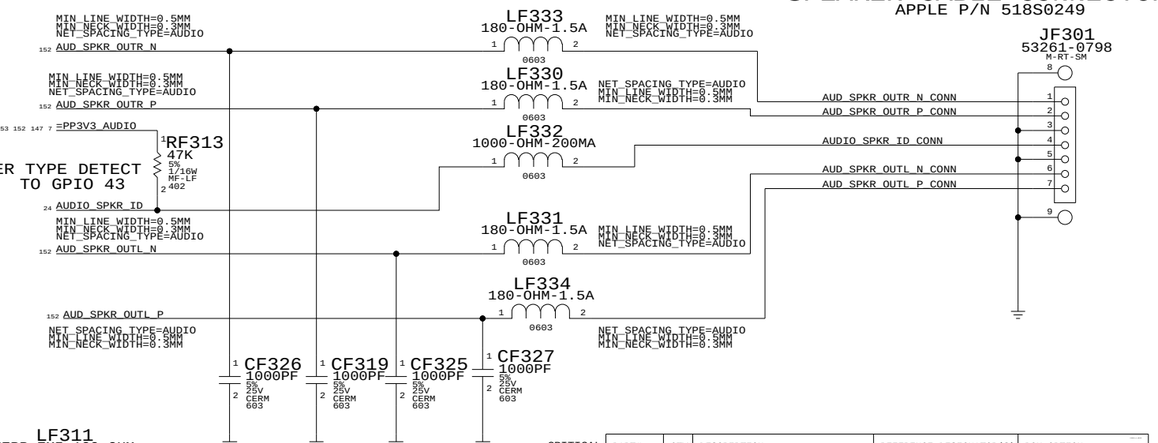
LINE IN JACK

APPLE P/N 514-0246 (M23) APPLE P/N 514-0249 (M33)



SPEAKER CABLE CONNECTOR

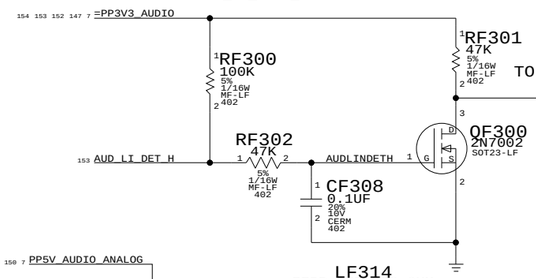
APPLE P/N 518S0249

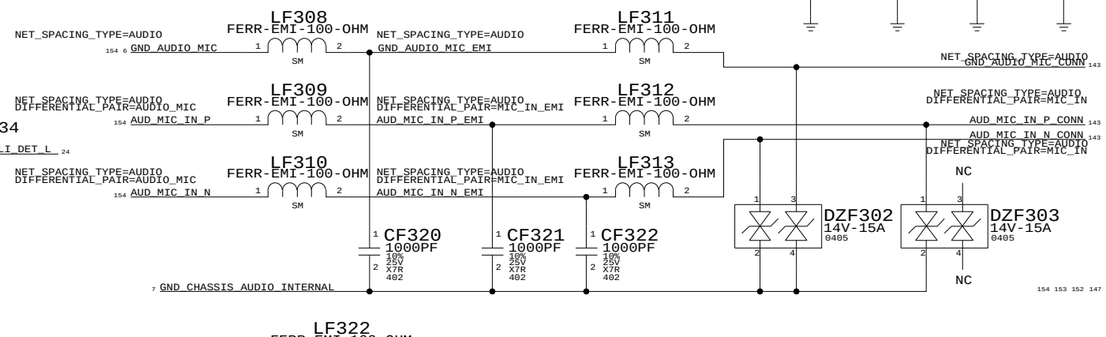


CRITICAL	PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
CRITICAL	514-0246	1	LINE IN CONNECTOR, 5.5 DEG	JF300	17_INCH_LCD
CRITICAL	514-0260	1	COMBO OUT CONN, 4.5 DEG	JF303	17_INCH_LCD
CRITICAL	514-0249	1	LINE IN CONNECTOR, 5.5 DEG	JF300	20_INCH_LCD
CRITICAL	514-0261	1	COMBO OUT CONN, 4.5 DEG	JF303	20_INCH_LCD

LINE IN PLUG DETECT

AUDIO_IN_DET0_L = LOW: PLUG INSERTED
AUDIO_IN_DET0_L = HIGH: PLUG NOT INSERTED

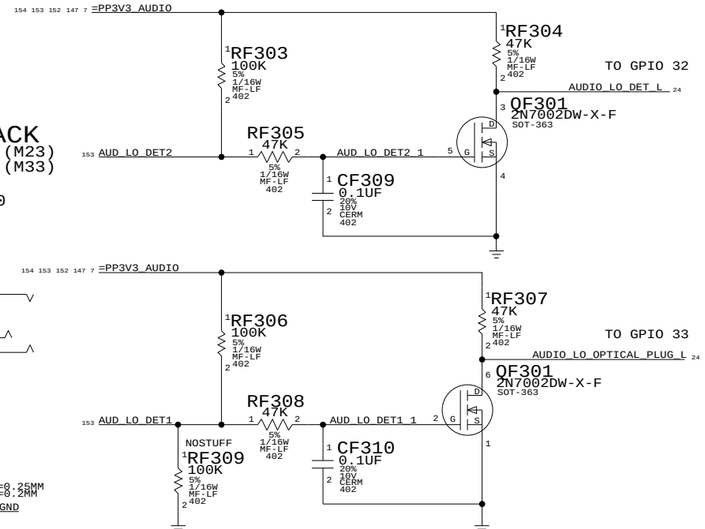




LINE OUT PLUG DETECTS

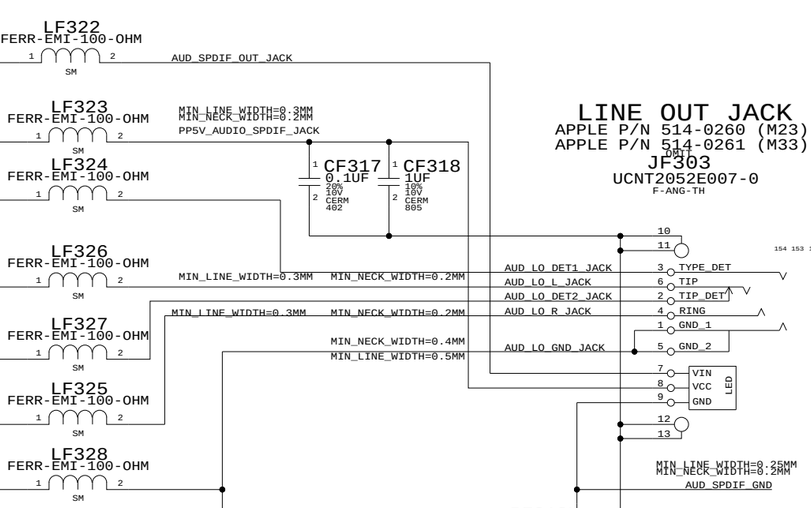
AUDIO_LO_DET_L = LOW: PLUG INSERTED
AUDIO_LO_DET_L = HIGH: PLUG NOT INSERTED

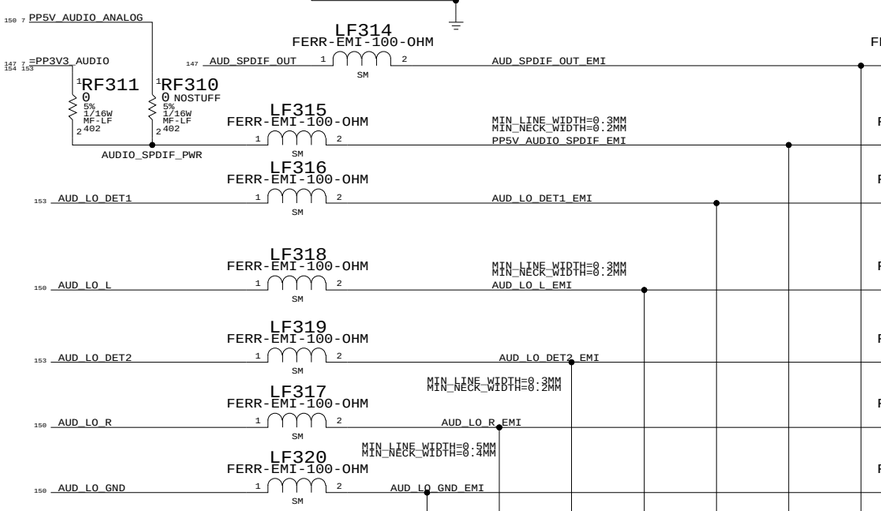
AUDIO_LO_OPTICAL_PLUG_L = LOW: OPTICAL DIGITAL AUDIO PLUG INSERTED
AUDIO_LO_OPTICAL_PLUG_L = HIGH: ANALOG AUDIO PLUG INSERTED



LINE OUT JACK

APPLE P/N 514-0260 (M23)
APPLE P/N 514-0261 (M33)





AUDIO: CONNECTORS

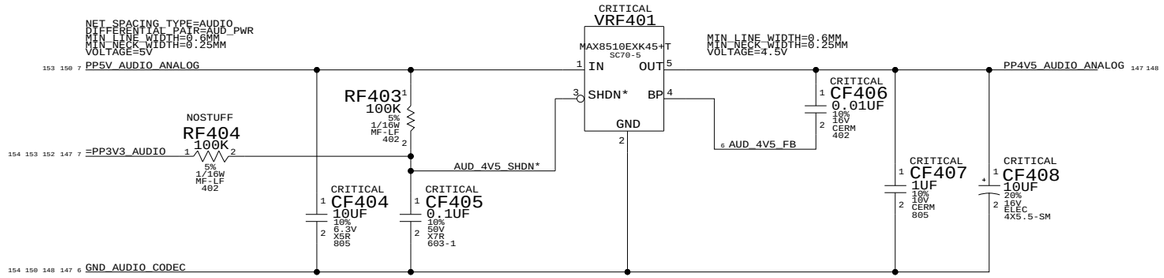
SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

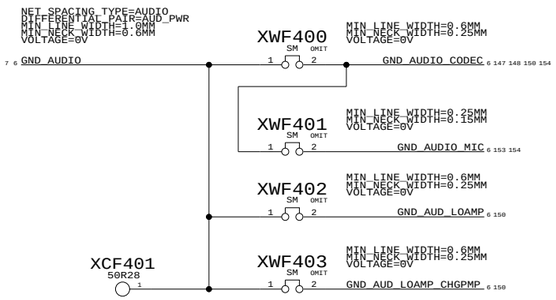
SIZE	DRAWING NUMBER	REV.
D	051-6790	F
SCALE: NONE	SHT: 153 OF 154	

4.5V POWER SUPPLY FOR CODEC AND LINE IN AMP

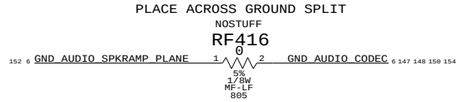
APPLE P/N 353S0733



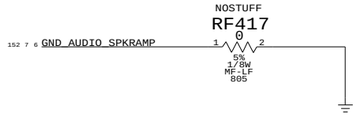
AUDIO GROUND RETURNS



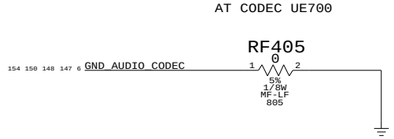
PLACE ACROSS GROUND SPLIT



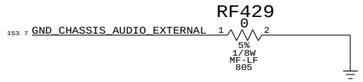
PLACE NEAR ENTRY TO SPEAKER AMP GROUND PLANE



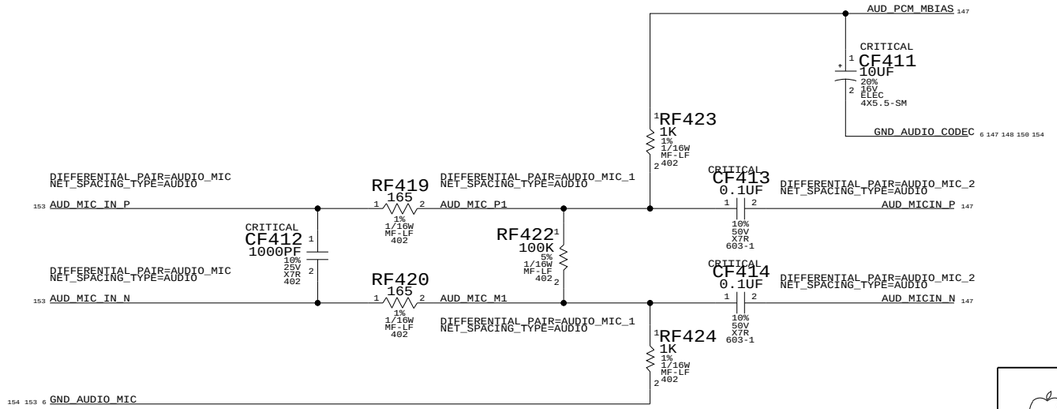
PLACE ACROSS GROUND SPLIT AT CODEC UE700



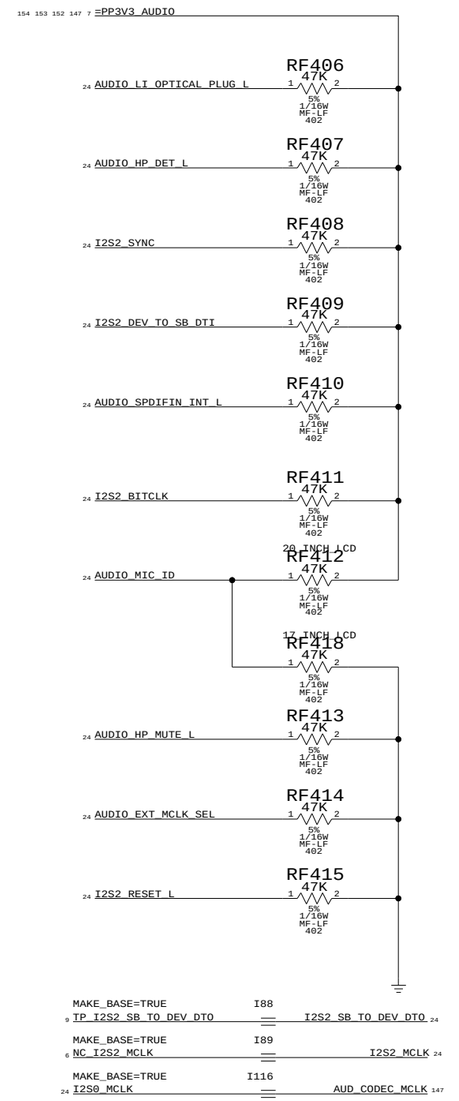
PLACE AT JF303



MICROPHONE IMPEDANCE MATCHING CIRCUIT



UNUSED GPIO TERMINATIONS



AUDIO: POWER SUPPLIES

SYNC_MASTER=FINO-SO SYNC_DATE=10/07/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6790	F

SCALE	SHT	OF
NONE	154	154