1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
03		384363	ENGINEERING RELEASED	06/03/05	?

STD MARIAS EVT

PDF	CSA	CONTENTS	SYNC MASTER	DATE
1	1	Table Of Contents	N/A	N/A
2	2	Board Information	N/A	N/A
3	3	System Block Diagram	N/A	N/A
4	4	Power Block Diagram	N/A	N/A
5	5	Revision History	N/A	N/A
6	6	Q16C Pin Swaps	N/A	N/A
7	7	Functional Test Points	N/A	N/A
8	8	I2C Connections	N/A	N/A
9	9	JTAG Connections	N/A	N/A
10	10	Power Synonyms	N/A	N/A
11	11	Signal Synonyms	N/A	N/A
12	12	Power Inputs	N/A	N/A
13	13	Battery Charger	N/A	N/A
14	14	12.8V PBUS/PMU Supplies	N/A	N/A
15	15	5V/3.3V Supplies	N/A	N/A
16	16	1.8V/1.5V Supplies	N/A	N/A
17	17	2.5V Supply	N/A	N/A
18	19	Vesta Power & Misc	N/A	N/A
19	21	I2 Power	N/A	N/A
20	22	I2 Power Supplies	N/A	N/A
21	23	I2 Supplemental	N/A	N/A
22	24	I2 Miscellaneous	N/A	N/A
23	25	PCI Clock Buffer	N/A	N/A
24	26	LEDs/Reset/Debug	N/A	N/A
25	27	Power Management Unit (PMU05)	N/A	N/A
26	29	Power Sequencing	N/A	N/A
27	30	Fan Controller	N/A	N/A
28	31	ALS Support	N/A	N/A
29	32	Sudden Motion Sensor	N/A	N/A
30	33	Q16C Internal I/O I	N/A	N/A
31	34	Q16C Internal I/O II	N/A	N/A
32	35	I2 Processor Interface	N/A	N/A
33	36	A8 MaxBus (CPU0)	MULLET	05/25/2005
34	37	A8 Configuration Straps	MULLET	05/25/2005
35	38	A8 Power (CPU0)	MULLET	05/25/2005
36	39	CPU VCore Supply	N/A	N/A
37	46	CPU AVDD Supply	N/A	N/A
38	47	I2 Memory Interface	N/A	N/A
39	48	Memory Series Termination	N/A	N/A
40	50	DDR2 SO-DIMM Slot A	N/A	N/A
41	52	DDR2 SO-DIMM Slot B	N/A	N/A
42	55	M11 Frame Buffer Constraints	N/A	N/A
43	56	I2 AGP Interface	N/A	N/A
44	57	GPU (M11) AGP Interface	N/A	N/A
45	58	GPU VCore Supply	N/A	N/A
46	59	GPU (M11) Core Power	N/A	N/A
47	60	GPU (M11) I/O Power	N/A	N/A
48	61	GPU (M11) Frame Buffer I/F	N/A	N/A
49	62	GPU Frame Buffer A	N/A	N/A
50	63	GPU Frame Buffer B	N/A	N/A
51	64	GPU (M11) GPIOs/Straps	N/A	N/A
52	65	GPU (M11) Clocks/Misc	N/A	N/A
53	66	GPU (M11) DVI/DAC Outputs	N/A	N/A
54	67	Lower TMDS Transmitter	N/A	N/A
55	68	Upper TMDS Transmitter	N/A	N/A
56	69	Internal Display Conns	N/A	N/A
57	70	External Display Conns	N/A	N/A
58	71	BootROM	N/A	N/A
59	72	I2 PCI Interface	N/A	N/A
60	73	Q85 Airport/BT Connector	N/A	N/A
61	74	Cardbus	N/A	N/A
62	75	NEC USB2	N/A	N/A
63	81	I2 UATA Interface	N/A	N/A
64	82	HDD/ODD Connectors	N/A	N/A
65	84	I2 Ethernet Interface	N/A	N/A
66	85	Vesta Ethernet PHY	N/A	N/A
67	86	Ethernet Connector	N/A	N/A
68	88	I2 FireWire Interface	N/A	N/A
69	89	Vesta FireWire PHY	N/A	N/A
70	90	FireWire Ports	N/A	N/A
71	91	FireWire Series Term	N/A	N/A
72	92	I2 USB Interface	N/A	N/A
73	93	NEC USB2 Interface	N/A	N/A
74	100	Audio Board Connector	N/A	N/A
75	110	Spacing & Physical Constraints	N/A	N/A
76	111	Spacing & Physical Constraints 2	N/A	N/A
77	112	Cross Reference Page		
78	113	Cross Reference Page		
79	114	Cross Reference Page		
80	115	Cross Reference Page		

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
051-6929	1	SCHEM,MARIAS-STD,Q16C	SCH1	
820-1875	1	PCBF,MARIAS,12L-STD,Q16C	PCB1	
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYT]	Q16C_BTR_VRAM_S
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:SYU]	Q16C_BST_VRAM_S
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TMJ]	Q16C_BTR_VRAM_H
826-4393	1	LBL,P/N LABEL,PCB,28MM x 6MM	[EEE:TMK]	Q16C_BST_VRAM_H

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING
THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE
SIZE D

Apple Computer Inc.

TITLE
SCHEM,MARIAS-STD,Q16C

DRAWING NUMBER 051-6929 REV. 03

Design-Specific Rules

TABLE_SPACING_RULE

TABLE_SPACING_RULE

STANDARD	=DEFAULT	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
BGA_P1MM	10	*	0.10 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
BGA_P2MM	20	*	0.20 MM	1.25 MM	0.1 MM	12.5 MM	15.0 MM
DEFAULT		*	0.1 MM	2.5 MM	0.15 MM	10.0 MM	15.0 MM

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT

*	*	1MM	BGA_P1MM
AGP_STB	*	1MM	BGA_P2MM
CLOCK	*	1MM	BGA_P2MM
RAM_DIFF	*	1MM	BGA_P2MM

"1MM" area defined around BGAs to reduce DRCs caused by fan-out.

"BGA_P2MM" rule ensures these critical signals do not fan-out routed next to any other signals.

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

STANDARD	*	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT
DEFAULT	*	Y	0.100 MM	0.100 mm	1.25 MM

Layer-specific rules for 90-ohm differential impedance

TABLE_SPACING_RULE

TABLE_SPACING_RULE

90_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.200 MM	2.5 MM	1.0 MM
90_OHM_DIFF	*		2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

90_OHM_DIFF	TOP,BOTTOM	Y	0.118 MM	0.1 MM	5 MM
90_OHM_DIFF	*	Y	0.125 MM	0.1 MM	5 MM

Layer-specific rules for 100-ohm differential impedance

TABLE_SPACING_RULE

TABLE_SPACING_RULE

100_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.200 MM	2.5 MM	1.0 MM
100_OHM_DIFF	*		2.5 MM	0.200 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

100_OHM_DIFF	TOP,BOTTOM	Y	0.092 MM	0.1 MM	5 MM
100_OHM_DIFF	*	Y	0.100 MM	0.1 MM	5 MM

Layer-specific rules for 110-ohm differential impedance

TABLE_SPACING_RULE

TABLE_SPACING_RULE

110_OHM_DIFF	TOP,BOTTOM		2.5 MM	0.330 MM	2.5 MM	1.0 MM
110_OHM_DIFF	*		2.5 MM	0.300 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

110_OHM_DIFF	TOP,BOTTOM	Y	0.080 MM	0.1 MM	5 MM
110_OHM_DIFF	*	Y	0.085 MM	0.1 MM	5 MM

Portable-specific Override Rules

TABLE_SPACING_RULE

TABLE_SPACING_RULE

AGP	201	*	0.2 MM

TABLE_SPACING_RULE

AGP_STB	251	*	0.25 MM

TABLE_SPACING_RULE

VGA	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

TABLE_SPACING_RULE

TV	151	*	0.15 MM	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

TABLE_PHYSICAL_RULE

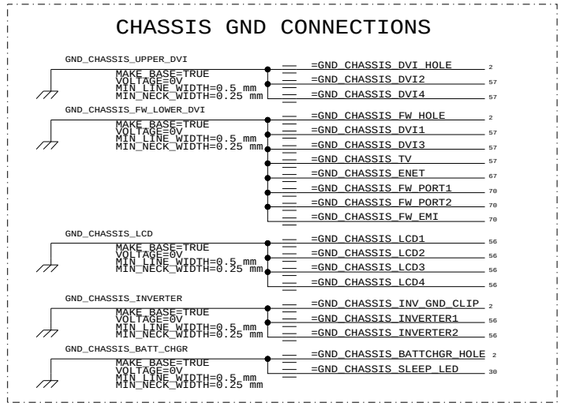
TABLE_PHYSICAL_RULE

VGA	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

TABLE_PHYSICAL_RULE

TV	*	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

CHASSIS GND CONNECTIONS



Layer-specific rules for 60-ohm single-ended impedance

TABLE_SPACING_RULE

TABLE_PHYSICAL_RULE

60_OHM_SE	*	Y	0.076 MM	=50_OHM_SE	=50_OHM_SE	

Layer-specific rules for 50-ohm single-ended impedance

TABLE_SPACING_RULE

TABLE_SPACING_RULE

50_OHM_SE	*	2.5 MM	0.125 MM	2.5 MM	1.0 MM

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

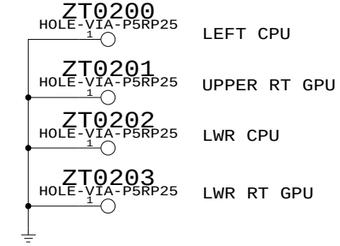
50_OHM_SE	*	Y	0.100 MM	0.100 MM	1.25 MM

NO_TEST Properties

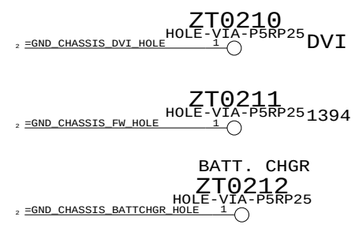
I2C6	1778_ITH_RC	45	NO_TEST=TRUE	I2C6	TP_VESTA_DNC_E9	18	NO_TEST=TRUE
I2C7	1778_VRNG	45	NO_TEST=TRUE	I2C7	TP_VESTA_F1000	66	NO_TEST=TRUE
I2C8	GPU_DVOD_R<18>	6 53	NO_TEST=TRUE	I2C8	TP_VESTA_PHYA<0>	66	NO_TEST=TRUE
I2C9	LTC3412_RUNSS	17	NO_TEST=TRUE	I2C9	TP_VESTA_REGSEN2	18	NO_TEST=TRUE
I2C10	TMDS_CONN_CLKP	57	NO_TEST=TRUE	I2C10	TP_VESTA_SPD0	66	NO_TEST=TRUE
I2C11	TP_NEC_SMC	62	NO_TEST=TRUE	I2C11	USB_NEC_BT_N	6 11	NO_TEST=TRUE
I2C12	TP_NEC_SMI_L	62	NO_TEST=TRUE	I2C12	USB_NEC_N<1>	73	NO_TEST=TRUE
I2C13	TP_NEC_SRCLK	62	NO_TEST=TRUE	I2C13	USB_NEC_N<2>	73	NO_TEST=TRUE
I2C14	TP_USB2_PWREN<0>	73	NO_TEST=TRUE	I2C14	USB_NEC_N<3>	73	NO_TEST=TRUE
I2C15	TP_USB2_PWREN<2>	73	NO_TEST=TRUE	I2C15	USB_NEC_P<0>	73	NO_TEST=TRUE
I2C16	TP_USB2_PWREN<3>	73	NO_TEST=TRUE	I2C16	USB_NEC_P<1>	73	NO_TEST=TRUE
				I2C17	SI_TMDS_DN<5>	55	NO_TEST=TRUE
I2C45	UATA_DD_R<0>	6 63	NO_TEST=TRUE	I2C25	SI_TMDS_DN<4>	55	NO_TEST=TRUE
I2C46	UATA_DD_R<8>	6 63	NO_TEST=TRUE	I2C26	SI_TMDS_DP<3>	55	NO_TEST=TRUE
I2C48	UATA_DD_R<10>	6 63	NO_TEST=TRUE	I2C27	SI_TMDS_DN<2>	54	NO_TEST=TRUE
I2C47	UATA_DA_R<0>	6 63	NO_TEST=TRUE	I2C28	SI_TMDS_DN<1>	54	NO_TEST=TRUE
I2C48	UATA_DA_R<1>	6 63	NO_TEST=TRUE	I2C29	SI_TMDS_DN<0>	54	NO_TEST=TRUE
				I2C30	SI_TMDS_CLKP	54	NO_TEST=TRUE

BOARD HOLES

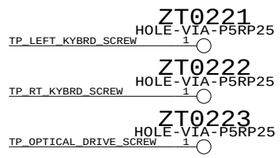
HEATSINK MOUNTS



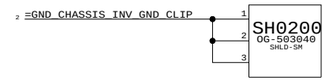
CHASSIS MOUNTS



MECH. HOLES

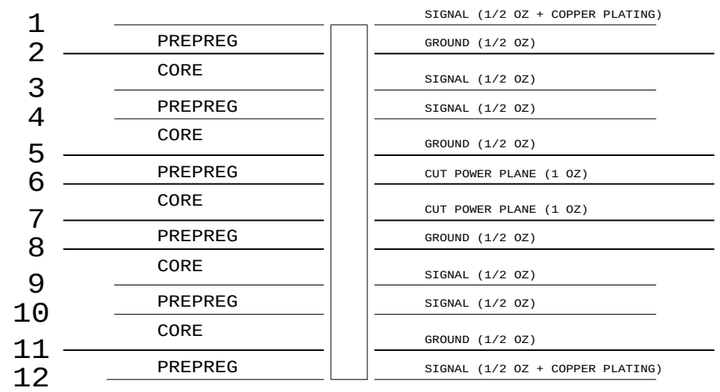


INVERTER



BOARD STACK-UP AND CONSTRUCTION

SEE BOARD FILE FOR DETAILED INFORMATION
CONVENTIONAL CONSTRUCTION WITH Pxx TH VIA



TABLE_BOARD_INFO

TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM NO_TYPE,1MM MM

BOM OPTIONS

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7015	PCBA,MLB,BETTERMHZ,MARIAS,VRAM_S,Q16C	COMMON,ALTERNATE,gQ16C,gQ16C_BTR,Q16C_BTR_VRAM_S,VRAM_SAMSUNG,gCommon
630-7016	PCBA,MLB,BESTMHZ,MARIAS,VRAM_S,Q16C	COMMON,ALTERNATE,gQ16C,gQ16C_BST,Q16C_BST_VRAM_S,VRAM_SAMSUNG,gCommon
630-7184	PCBA,MLB,BETTERMHZ,MARIAS,VRAM_H,Q16C	COMMON,ALTERNATE,gQ16C,gQ16C_BTR,Q16C_BTR_VRAM_H,VRAM_HYNIX,gCommon
630-7185	PCBA,MLB,BESTMHZ,MARIAS,VRAM_H,Q16C	COMMON,ALTERNATE,gQ16C,gQ16C_BST,Q16C_BST_VRAM_H,VRAM_HYNIX,gCommon

BOM GROUP	BOM OPTIONS
gCommon	5V_HD_LOGIC,BACKUP_BATT,CPU_A7PM,I2_FW_BETA,I2_MAXBUS_50OHM,MAXBUS_1V8,gCommon1
gCommon1	MMM_ACCEL_KIONIX,GPU_PWRPLAY,GPU_SS,GPU_LVDDR_2V8,GPU_MEMIO_1V8,gCommon2
gCommon2	I2_REV1_NOT,I2_MAXBUS_FBCLK_MATCHED,I2_AGP_FBCLK_MATCHED,I2_PCI_FBCLK_MATCHED,gCommon3
gCommon3	CPU_VCORE_3STATES,I2_MAXBUS_166MHZ,I2VCORE_1V5,I2VCORE_BURST,gCommon4
gCommon4	VESTA_PORT2_DISABLE,DVO_1V8,TMDS_DUAL,VCORE_OFFSET,VCORE_OFFSET_SW,gUSB
gUSB	USB2_NEC,USB1P1_I2
gQ16C	Q16C_PARTS,BOOTROM_PROG,PMU_PROG,DEVELOPMENT,MAXBUS_TBEN_SYNC
gQ16C_BTR	A7PM_1P5_LGA,CPU0_BUSRATIO_9.0X
gQ16C_BST	A7PM_1P67_LGA,CPU0_BUSRATIO_10.0X

Module Components

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
343S0325	1	IC,ASIC,I2,REV1.1,NB/SB,974 BGA	U2100	CRITICAL	
337S3135	1	IC,PMU05,BLANK,QFP	U2700	CRITICAL	PMU_BLANK
341S1772	1	IC,PMU05,V1,QFP	U2700	CRITICAL	PMU_PROG
337S3162	1	IC,A7PM,R1.5,1.67GHZ,LGA,1.28V,23W,85C	U3600	CRITICAL	A7PM_1P67_LGA
337S3163	1	IC,A7PM,R1.5,1.5GHZ,LGA,1.28V,23W,85C	U3600	CRITICAL	A7PM_1P5_LGA
337S3077	1	IC,A8,xxxGHZ	U3600	CRITICAL	CPU_A8
338S0252	1	IC,GPU,M11P	U5700	CRITICAL	
335S0088	1	BOOTROM,BLANK	U7100	CRITICAL	BOOTROM_BLANK
341S1736	1	IC,BOOTROM,B,Q16C	U7100	CRITICAL	BOOTROM_PROG
343S0356	1	IC,ASIC,VESTA,V1.3,LF	U8500	CRITICAL	
333S0317	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_SAMSUNG
333S0314	4	IC,GDDR SDRAM,2MX32X4,300MHZ, LF FBGA144	U6200,U6250,U6300,U6350	CRITICAL	VRAM_HYNIX

Board Information

SYNC_MASTER=N/A SYNC_DATE=N/A

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 2 OF 115	

U51 INTREPID

J23 Ethernet Connector P.28
4 DATA PAIRS
U43 Ethernet PHY P.28
G/MII
3.3V
10/100/1000
8BIT TX
8BIT RX
125MHZ

J24 FW - A Connector P.30
2 DATA PAIRS @ 200MHZ
J20 FW - B Connector P.30
2 DATA PAIRS @ 400MHZ
U36 FireWire PHY P.29
1394 OHCI
3.3V
8BIT TX/RX
50MHZ

J13 ODD Connector P.26
EIDE
J12 HDD Connector P.26
UIDE

J15 SW MODEM Connector P.27
J3 LIO/Audio Connector P.27
I2S
I2C
I2C
U53/J1/J18 Fan Circuit P.27

J2 RUX Board Connector P.24
J19 ALS BOARD Connector P.24
J16 BACKUP BATTERY CONNECTOR P.33
C692 SUPERCAP P.33
J26 Battery Connector P.32
Power Supply & Charger P.32-36
J27 DC-In Connector P.32
J8 SLEEP LED P.24
SMBUS
3.3V

U15/U20/U58 MMM P.25
U41 BATTERY CURRENT SENSOR P.25

NOT USED

ETHERNET 10/100/1000 P.13	FIREWIRE 400 MB/S P.13	UATA 100 P.13	EIDE P.13	CARDSLOT P.13	I2S P.14	I2C P.13 P.14

NOT USED USB PORT A P.14
NOT USED USB PORT B P.14
NOT USED USB PORT C P.14
NOT USED USB PORT D P.14
USB PORT E P.14
USB PORT F P.14
MAXBUS P.8

SCCA P.14
VIA/PMU P.14
BOOTROM P.12
PCI 64BITS 33MHZ P.12
4X AGP P.12

J28 Serial Debug Connector P.27
U28 PMU P.31
SERIAL
5V
J5 CARDBUS Connector P.18
33MHZ
16/32 BITS
3.3V/5V
U8 TI PCI1510 CardBus Controller P.18
U11 BOOT ROM 1M X 8 P.9
J6 AIRPORT Connector P.26
PCI BUS
32BITS
33MHZ
3.3V

J3 BlueTooth (LIO) P.27
J10 SPIDEY P.24

MAXBUS
1.8V
167MHZ
32BIT ADDRESS
64BIT DATA

DDR MEMORY P.9
MEMORY BUS
2.5V
167MHZ
64BITS
U16/U18/U28/U27 2:1 DDR MUXES P.10
J25 DDR SDRAM DIMM 0
DDR SDRAM DIMM 1 SO-DIMM Connector P.11

AGP BUS
1.5V/3.3V
32BITS
66MHZ
U47 ATI M11 64MB P.19-22
MEMORY CH. A (INTERNAL MEM)
MEMORY CH. C (INTERNAL MEM)
MEMORY CH. B (INTERNAL MEM)
MEMORY CH. D (INTERNAL MEM)

U17 NEC USB2.0 EHCI HC P.17
J3 LEFT USB (VIA LIO) P.27
J17 RIGHT USB (VIA STATLER) P.27

U56 APOLLO CPU (MPC7447) P.5-6
CPU PLL Config P.7
PMU

J4 Inverter Connector P.23

LVDS
EDID (I2C)
S-VIDEO
COMPOSITE
TMDS (VIA SIL1162)
RGB
DDC

J14 LCD Panel Connector P.23
J21 S-Video Connector P.23
J22 DVI-I Connector P.23

System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE NONE	SHT 3 OF 115	

POWER SYSTEM ARCHITECTURE

AC ADAPTER IN PG 32

INRUSH LIMITER PG 32

+24V_PBUS

1V20_REF - PG 33
>~13.44V TURNS-ON
<~13.44V SHUTS-OFF

RUN/SS

BUCK VCC REGULATOR (LTC1625) PG 33

AC: 12.8V
NO AC: BATTERY VOLTAGE
1625 NOT RUNNING

SHUTDOWN: RUNNING
SLEEP: RUNNING
RUN: RUNNING

+PBUS

RC AT 1M*0.047UF @ 24V
STARTS 2.0MSEC AFTER DCDC_EN_L BECOMES LOW

14V_PBUS

+3V_PMU LDO PG 33

+5V_MAIN
+3V_PMU
+4_6V_BU

+BATT

RUN/SS - 5V
TURNS ON AT >1V
<100UA ALLOWED
INTERNAL ZENER CLAMP TO 6V

MAIN 3V/5V DC/DC (LTC3707) PG 34

VCC STBYMD PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

INTERNAL ZENER CLAMP TO 6V
<100UA ALLOWED
TURNS ON AT >1V
RUN/SS - 3V

+5V_MAIN
3V_5V_OK

HOLDS BOTH RUN/SS AT GND WHEN IT'S CONNECTED TO GND

TURNS CONTROL TO RUN/SS WHEN IT'S OPEN

+3.3V_MAIN

RC AT 1M*0.1UF @ 24V
STARTS ~4.25MSEC AFTER DCDC_EN_L BECOMES LOW

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

+24V_PBUS

BACKUP BATTERY

14V_PBUS

14V CHARGES BACKUP BATTERY

24V IS OUTPUT ONLY FROM BACKUP BATTERY

CHARGER INPUT & BOOST OUTPUT PG 33

BACKUP BATTERY CIRCUIT CHARGES OFF +PBUS AND PREVENTS +PBUS AND +24V_PBUS FROM DROPPING BELOW 6V (UNTIL DRAINED)

BATTERY CHARGER (MAX1772) PG 32

DC/DC (LTC3411)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 36

+1.8V_MAIN

MAXBUS

+BATT

3S 2P 18650 CELLS

NO INRUSH PROTECTION
WHEN ONLY BATTERY IS CONNECTED

BATTERY VOLTAGE FEED-IN PATH PG 32

+PBUS

BACKLIGHT INVERTER

+5V_MAIN

VCC MAIN 2.5V/1.5V DC/DC (MAX1715) PG 36

PGOOD

SHUTDOWN: STOPPED
SLEEP: RUNNING
RUN: RUNNING

TURNS ON OUTPUT @ 2.4V ON1/ON2

MAP31 DDR CORE
MAP31 DDR I/O
DDR POWER

+2.5V_MAIN

1_5V_2_5V_OK

+1.5V_MAIN

INTREPID CORE
AGP I/O

+5V_MAIN

DCDC_EN_L

AFTER PMU IS UP AND RUNNING DCDC_EN_L WILL PULL ON1/ON2 LOW IN SHUTDOWN

+PBUS

+5V_MAIN

EXT_VCC

VCC DC/DC (LTC1778)

SHUTDOWN: STOPPED
SLEEP: D3COLD
RUN: RUNNING

TURNS ON AS LOW AS 0.8V/TYP 1.5V
INTERNAL 1.2UA CURRENT SOURCE

RUN/SS PG 20

GPU_VCORE +1.2V

DCDC_EN
SLEEP

D3_COLD

GPU_VCORE SEQUENCING

1M & 0.1UF @14V, IT TAKES ~5.88MS TO START SWITCHER

1_5V_2_5V_OK

D3_HOT

DCDC_EN_L
D3_HOT

1_5V_2_5V_OK WILL NOT PULL LOW UNTIL +5V_MAIN TURNS ON

HOWEVER, 5V SHOULD TURN ON ~2.23MS AFTER DCDC_EN_L OR PMU_POWERUP_L BECOMES '1'; MUCH LESS THAN THE RC CHARGING AT INT_VCC (5V)

+PBUS

DCDC_EN
SLEEP

MAXBUS SEQUENCING

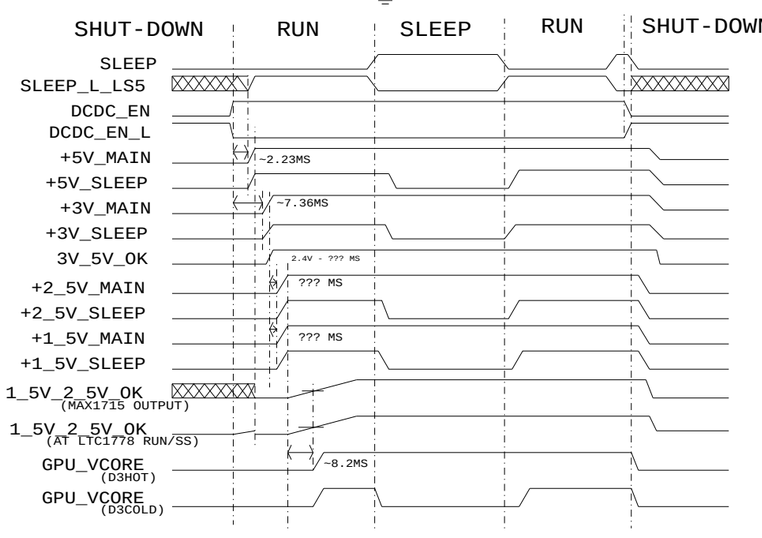
+5V_MAIN

VCC SHDN DC/DC (MAX1717)

SHUTDOWN: STOPPED
SLEEP: STOPPED
RUN: RUNNING

PG 35

CPU_VCORE (+1.385V)



Power Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE NONE | SHT 4 OF 115

REVISION HISTORY

PRE-EVT

04/04/2005 - Beginning revision history
- Made DDR2 and FB pin swaps as requested by CM
04/06/2005 - Modem connector moved to non-shared page
- Chassis grounds partitioned as in previous products
- CPU0 Vcore A/B select line hooked to I2 GPIO1
04/06/2005 - Made additional FB pin swaps
- Changed DDR2 CS/CKE RPAKs to RPAK2P (added RP4871, RP4876)
04/11/2005 - Implemented more DDR2 pin swaps
- Implemented Firewire pin swaps
- Added remaining spacing and physical rule tables
- Added upper LVDS channel to functional test page
- Changed battery sense resistor to 0.006 ohm (R1250)
- Stuffed R2903 to disable FW port power when off on AC
- Changed audio caps to XSR (CA633, CA650, CA651)
04/12/2005 - Corrected MIN_LINE_WIDTH properties on PP3V3_PWRON
- Corrected TMDS_DIFFERENTIAL_PAIR properties at DVI connector
- Reduced MIN_NECK_WIDTH property on GND to 0.2 mm for TMDS parts
- Corrected line and neck width properties
- Added RAM_DQS_N pulldowns
- Added high/low swing BOMOPTIONs for DVO on SI TMDS parts
- Added 3.3V DVO option to GPU
04/13/2005 - Removed 3 caps & isolating VG from digital ground on FW ports (per design guide)
04/14/2005 - Changed CPU to A11
04/15/2005 - Moved FB series R's to page 61
- Updated strobes, vREF inputs and decoupling on GPU
04/18/2005 - Corrected synonym problems on PMU port usage
- Added CPU0_Vcore_VID_MUX
04/19/2005 - Added NO_TEST properties to buses between JTAG enabled devices
04/20/2005 - Corrected ENET power rail to EMRUN from RUN (for Wake-on-LAN)
- Fixed ENET_PWRDWNR and VESTA_RESET circuits per Vesta design guide
- Changed R5880 to 6.34K to take CPU Vcore to 1.3V/1.05V
- Added page 6 and modified pages 11,35,81 for design specific pin swaps
04/21/2005 - Corrected STOP_ACC_L net name (hooked to I2 now) and removed redundant pullup
04/22/2005 - Added external pullups to replace missing internal I2 pullups
- Added ADC caps at PMU
- Corrected load capacitance for Vesta firewire crystal (to 18pF)
- Disconnected FW_POWERDOWN from Vesta LPWR_1394 pin
- Corrected pulldown resistor value for 0.006 ohm battery current sense
05/03/2005 - Changed 220UF CPU Vcore caps to 330 uF LF caps
- Changed GPU FB MVREFS into separate dividers
- Pinswapped UATA I/F, DVO I/F, USB pulldowns
- Added extra cap at input to 12 QSEAVDD
05/04/2005 - Added pulldowns to unused serial debug signals (DTR/RTS)
05/05/2005 - Added pulldown to Vesta LPWR_1394
- Added POZAC signal between HDD and ODD connectors
05/10/2005 - Various Pb-free component replacements
05/13/2005 - Various Pb-free component replacements
- Pinswaps for I2 RPAKs to match up with Q41C style layout
05/16/2005 - Various Pb-free component replacements
- Added Hynix VRAM option and PCBAs
05/19/2005 - Various Pb-free component replacements
- Added TBEN sync circuit
05/20/2005 - Various Pb-free component replacements
- Added PASP signal between HDD and ODD connectors
05/21/2005 - Corrected OCA_INT connection between I2 and GPU
- Corrected VGA_sync connections at GPU
05/23/2005 - Released as USBX 01 for Pre-EVT/EVT
05/24/2005 - Added Ge6 USBX controller
05/25/2005 - Added ZDB clock buffer for PCI clocks
- Various Pb-free component replacements
05/26/2005 - Removed SMS PIC microcontroller
05/31/2005 - Added 2 0.1uF caps to GPU Vcore regulator output
- Corrected USB2 diff pair and spacing/physical rules on port connections
06/01/2005 - Corrected Firewire VP caps to 50V
- Various Pb-free component replacements

03

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	5	115

I2S Series Rs

MAKE_BASE=TRUE	22	I2S0_SB_TO_DEV_DTO_R	=RP1150P1	11	11	=RP1150P8	I2S0_SB_TO_DEV_DTO	7 74	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S0_BITCLK_R	=RP1150P2	11	11	=RP1150P7	I2S0_BITCLK	7 74	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S0_MCLK_R	=RP1150P3	11	11	=RP1150P6	I2S0_MCLK	7 74	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S0_SYNC_R	=RP1150P4	11	11	=RP1150P5	I2S0_SYNC	7 74	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S1_SB_TO_DEV_DTO_R	=RP1151P1	11	11	=RP1151P8	I2S1_SB_TO_DEV_DTO	30	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S1_SYNC_R	=RP1151P2	11	11	=RP1151P7	I2S1_SYNC	30	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S1_MCLK_R	=RP1151P3	11	11	=RP1151P6	I2S1_MCLK	30	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	22	I2S1_BITCLK_R	=RP1151P4	11	11	=RP1151P5	I2S1_BITCLK	30	MAKE_BASE=TRUE		

UATA Series Rs

MAKE_BASE=TRUE	63	UATA_DD_R<12>	=RP8150P1	63	63	=RP8150P8	UATA_DD<12>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_CS0_L_R	=RP8150P2	63	63	=RP8150P7	UATA_CS0_L	7 63 64	MAKE_BASE=TRUE	(IDE_CS1FX_L)	
MAKE_BASE=TRUE	63	UATA_DD_R<14>	=RP8150P3	63	63	=RP8150P6	UATA_DD<14>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<11>	=RP8150P4	63	63	=RP8150P5	UATA_DD<11>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<7>	=RP8151P1	63	63	=RP8151P8	UATA_DD<7>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<2>	=RP8151P2	63	63	=RP8151P7	UATA_DD<2>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<3>	=RP8151P3	63	63	=RP8151P6	UATA_DD<3>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<15>	=RP8151P4	63	63	=RP8151P5	UATA_DD<15>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<9>	=RP8152P1	63	63	=RP8152P8	UATA_DD<9>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<4>	=RP8152P2	63	63	=RP8152P7	UATA_DD<4>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<6>	=RP8152P3	63	63	=RP8152P6	UATA_DD<6>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<5>	=RP8152P4	63	63	=RP8152P5	UATA_DD<5>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DA_R<2>	=RP8153P1	63	63	=RP8153P8	UATA_DA<2>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63 2	UATA_DD_R<8>	=RP8153P2	63	63	=RP8153P7	UATA_DD<8>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63 2	UATA_DD_R<10>	=RP8153P3	63	63	=RP8153P6	UATA_DD<10>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63 2	UATA_DA_R<0>	=RP8153P4	63	63	=RP8153P5	UATA_DA<0>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<13>	=RP8154P1	63	63	=RP8154P8	UATA_DD<13>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63 2	UATA_DD_R<0>	=RP8154P2	63	63	=RP8154P7	UATA_DD<0>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63	UATA_DD_R<1>	=RP8154P3	63	63	=RP8154P6	UATA_DD<1>	7 63 64	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	63 2	UATA_DA_R<1>	=RP8154P4	63	63	=RP8154P5	UATA_DA<1>	7 63 64	MAKE_BASE=TRUE		

MAXBUS Pullups

MAKE_BASE=TRUE	33 32	MAXBUS_TS_L	=RP3510P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BG_L	=RP3510P2	32							
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DBG_L	=RP3510P3	32							
MAKE_BASE=TRUE	32	MAXBUS_TBEN_I2	=RP3510P4	32							
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BG_L	=RP3511P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_HIT_L	=RP3511P2	32							
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_HIT_L	=RP3511P3	32							
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_BR_L	=RP3511P4	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_BR_L	=RP3512P1	32							
MAKE_BASE=TRUE	33 32	MAXBUS_TA_L	=RP3512P2	32							
MAKE_BASE=TRUE	34 32	MAXBUS_CPU0_INT_L	=RP3512P3	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_INT_L	=RP3512P4	32							
MAKE_BASE=TRUE	33 32	MAXBUS_CPU0_DRDY_L	=RP3513P2	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DRDY_L	=RP3513P3	32							
MAKE_BASE=TRUE	33 32	MAXBUS_AACK_L	=RP3513P4	32							
MAKE_BASE=TRUE	33 32	MAXBUS_ARTRY_L	=RP3514P1	32							
MAKE_BASE=TRUE	32	MAXBUS_CPU1_DBG_L	=RP3514P2	32							
MAKE_BASE=TRUE	33 32	MAXBUS_TEA_L	=RP3514P3	32							

AGP Pullups

MAKE_BASE=TRUE	44 43	AGP_TRDY_L	=RP5610P1	43							
MAKE_BASE=TRUE	44 43	AGP_IRDY_L	=RP5610P2	43							
MAKE_BASE=TRUE	44 43	AGP_REQ_L	=RP5610P3	43							
MAKE_BASE=TRUE	44 43	AGP_RBF_L	=RP5610P4	43							
MAKE_BASE=TRUE	44 43	AGP_FRAME_L	=RP5611P1	43							
MAKE_BASE=TRUE	44 43	AGP_DEVSEL_L	=RP5611P2	43							
MAKE_BASE=TRUE	44 43	AGP_STOP_L	=RP5611P3	43							
MAKE_BASE=TRUE	44 43	AGP_GNT_L	=RP5611P4	43							

PCI Pullups

MAKE_BASE=TRUE	11	PCI_AIRPORT_GNT_L	=RP7250P1	59							
MAKE_BASE=TRUE	60 59 62 61	PCI_TRDY_L	=RP7250P2	59							
MAKE_BASE=TRUE	60 59 62 61	PCI_IRDY_L	=RP7250P3	59							
MAKE_BASE=TRUE	60 59 62 61	PCI_STOP_L	=RP7250P4	59							
MAKE_BASE=TRUE	11	PCI_CBUS_REQ_L	=RP7251P1	59							
MAKE_BASE=TRUE	11	PCI_AIRPORT_REQ_L	=RP7251P2	59							
MAKE_BASE=TRUE	11	PCI_CBUS_GNT_L	=RP7251P3	59							
MAKE_BASE=TRUE	60 59 62 61	PCI_FRAME_L	=RP7251P4	59							

FW Series Rs

MAKE_BASE=TRUE	68 9	FW_D_R<7>	=RP9100P1	71	71	=RP9100P8	FW_D<7>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<3>	=RP9100P2	71	71	=RP9100P7	FW_D<3>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<4>	=RP9100P3	71	71	=RP9100P6	FW_D<4>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<2>	=RP9100P4	71	71	=RP9100P5	FW_D<2>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<0>	=RP9101P1	71	71	=RP9101P8	FW_D<0>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<6>	=RP9101P2	71	71	=RP9101P7	FW_D<6>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<1>	=RP9101P3	71	71	=RP9101P6	FW_D<1>	9 69	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	68 9	FW_D_R<5>	=RP9101P4	71	71	=RP9101P5	FW_D<5>	9 69	MAKE_BASE=TRUE		

Lower DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVOD_R<16>	=RP6720P1	54	54	=RP6720P8	GPU_DVOD<16>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<4>	=RP6720P2	54	54	=RP6720P7	GPU_DVOD<4>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<7>	=RP6720P3	54	54	=RP6720P6	GPU_DVOD<7>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<6>	=RP6720P4	54	54	=RP6720P5	GPU_DVOD<6>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<11>	=RP6721P1	54	54	=RP6721P8	GPU_DVOD<11>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<9>	=RP6721P2	54	54	=RP6721P7	GPU_DVOD<9>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<10>	=RP6721P3	54	54	=RP6721P6	GPU_DVOD<10>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVO_HSYNC_R	=RP6721P4	54	54	=RP6721P5	GPU_DVO_HSYNC	54 55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<3>	=RP6722P1	54	54	=RP6722P8	GPU_DVOD<3>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<5>	=RP6722P2	54	54	=RP6722P7	GPU_DVOD<5>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<13>	=RP6722P3	54	54	=RP6722P6	GPU_DVOD<13>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<12>	=RP6722P4	54	54	=RP6722P5	GPU_DVOD<12>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<2>	=RP6723P1	54	54	=RP6723P8	GPU_DVOD<2>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<1>	=RP6723P2	54	54	=RP6723P7	GPU_DVOD<1>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<0>	=RP6723P3	54	54	=RP6723P6	GPU_DVOD<0>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<14>	=RP6723P4	54	54	=RP6723P5	GPU_DVOD<14>	55	MAKE_BASE=TRUE		

Upper DVO Series Rs

MAKE_BASE=TRUE	53	GPU_DVO_DE_R	=RP6821P1	55	55	=RP6821P8	GPU_DVO_DE	54 55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVO_VSYNC_R	=RP6821P2	55	55	=RP6821P7	GPU_DVO_VSYNC	54 55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVO_CLKP_R	=RP6821P3	55	55	=RP6821P6	GPU_DVO_CLKP	54 55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<8>	=RP6821P4	55	55	=RP6821P5	GPU_DVOD<8>	54	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<21>	=RP6822P1	55	55	=RP6822P8	GPU_DVOD<21>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<19>	=RP6822P2	55	55	=RP6822P7	GPU_DVOD<19>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<17>	=RP6822P3	55	55	=RP6822P6	GPU_DVOD<17>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<15>	=RP6822P4	55	55	=RP6822P5	GPU_DVOD<15>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<20>	=RP6823P1	55	55	=RP6823P8	GPU_DVOD<20>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<22>	=RP6823P2	55	55	=RP6823P7	GPU_DVOD<22>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53	GPU_DVOD_R<23>	=RP6823P3	55	55	=RP6823P6	GPU_DVOD<23>	55	MAKE_BASE=TRUE		
MAKE_BASE=TRUE	53 2	GPU_DVOD_R<18>	=RP6823P4	55	55	=RP6823P5	GPU_DVOD<18>	55	MAKE_BASE=TRUE		

USB Pulldowns

72			=RP9210P8			USB_I2_BT_P		11	MAKE_BASE=TRUE		
72			=RP9210P7			USB_I2_BT_N		11	MAKE_BASE=TRUE		
72			=RP9210P6			USB2_I2_RIGHT_PORT_N		11	MAKE_BASE=TRUE		
72			=RP9210P5			USB2_I2_RIGHT_PORT_P		11	MAKE_BASE=TRUE		
72			=RP9211P8			USB2_I2_P<1>		72	MAKE_BASE=TRUE		
72			=RP9211P7			USB2_I2_N<1>		72	MAKE_BASE=TRUE		
72			=RP9211P6			USB2_I2_N<3>		72	MAKE_BASE=TRUE		
72			=RP9211P5			USB2_I2_P<3>		72	MAKE_BASE=TRUE		
72			=RP9212P8			USB_I2_TPAD_N		11	MAKE_BASE=TRUE		
72			=RP9212P7			USB_I2_TPAD_P		11	MAKE_BASE=TRUE		
72			=RP9212P6			USB2_I2_LEFT_PORT_P		11	MAKE_BASE=TRUE		
72			=RP9212P5			USB2_I2_LEFT_PORT_N		11	MAKE_BASE=TRUE		
73			=RP9300P8			USB2_NEC_LEFT_PORT_P		11	MAKE_BASE=TRUE		
73			=RP9300P7			USB2_NEC_LEFT_PORT_N		11	MAKE_BASE=TRUE		
73			=RP9300P6			USB2_NEC_RIGHT_PORT_N		11	MAKE_BASE=TRUE		
73			=RP9300P5			USB2_NEC_RIGHT_PORT_P		11	MAKE_BASE=TRUE		
73			=RP9301P8			USB_NEC_BT_P		11	MAKE_BASE=TRUE		
73			=RP9301P7			USB_NEC_BT_N		2 11	MAKE_BASE=TRUE		
73			=RP9301P6			USB_NEC_TPAD_N		11	MAKE_BASE=TRUE		
73			=RP9301P5			USB_NEC_TPAD_P		11	MAKE_BASE=TRUE		

Q16C Pin Swaps

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	6	115

Enhanced MAC-1 Test Coverage

Functional test points use a P6 pad placed on bottom side.

POWER

E122	PP24V_ADAPTER	10	FUNC_TEST=YES	Place 2 TPs @ connector
E1	PP24V_ALL_PBUSA	10	FUNC_TEST=YES	
E2	PP12V8_ALL_PBUSB	10	FUNC_TEST=YES	
E4	PPVCORE_RUN_GPU	10	FUNC_TEST=YES	
E3	PPVCORE_RUN_CPU	10	FUNC_TEST=YES	
E6	PP1V8_PWRON	10	FUNC_TEST=YES	Place within 50 mm
E5	PP2V5_PWRON	10	FUNC_TEST=YES	of power supply.
E7	PP5V_PWRON	10	FUNC_TEST=YES	
E8	PP3V3_PWRON	10	FUNC_TEST=YES	
E9	PP5V_RUN	10	FUNC_TEST=YES	
E10	PP3V3_ALL	10	FUNC_TEST=YES	
E102	=FTP_GND	7 10	FUNC_TEST=YES	Place 5-10 GND TPs.

LVDS

E79	LVDS_U0_P	53 56	FUNC_TEST=YES	
E80	LVDS_U0_N	53 56	FUNC_TEST=YES	
E81	LVDS_U1_P	53 56	FUNC_TEST=YES	
E82	LVDS_U1_N	53 56	FUNC_TEST=YES	
E83	LVDS_U2_P	53 56	FUNC_TEST=YES	
E84	LVDS_U2_N	53 56	FUNC_TEST=YES	
E85	CLKLVDS_U_P	53 56	FUNC_TEST=YES	
E86	CLKLVDS_U_N	53 56	FUNC_TEST=YES	
E11	LVDS_L0_P	53 56	FUNC_TEST=YES	
E12	LVDS_L0_N	53 56	FUNC_TEST=YES	Place within 25 mm
E13	LVDS_L1_P	53 56	FUNC_TEST=YES	of LVDS connector.
E14	LVDS_L1_N	53 56	FUNC_TEST=YES	
E16	LVDS_L2_P	53 56	FUNC_TEST=YES	
E15	LVDS_L2_N	53 56	FUNC_TEST=YES	
E17	CLKLVDS_L_P	53 56	FUNC_TEST=YES	
E18	CLKLVDS_L_N	53 56	FUNC_TEST=YES	
E19	LVDS_DDC_CLK	51 56	FUNC_TEST=YES	
E20	LVDS_DDC_DATA	51 56	FUNC_TEST=YES	
E21	=PP3V3_DDC_LCD	10 56	FUNC_TEST=YES	
E63	PP3V3_LCD_CONN	56	FUNC_TEST=YES	

INVERTER

E22	PPBUS_INVERTER	56	FUNC_TEST=YES	
E23	PP5V_INV_SW	56	FUNC_TEST=YES	Place within 25 mm
E24	BRIGHT_PWM	56	FUNC_TEST=YES	of inverter connector.
E24	GND_INVERTER	56	FUNC_TEST=YES	

UATA

E106	=PP5V_RUN_ODD	10 64	FUNC_TEST=YES	
E117	=PP5V_RUN_HDD	10 64	FUNC_TEST=YES	
E110	PP3V3R5V_RUN_HDD_LOGIC	64	FUNC_TEST=YES	
E32	UATA_DD<15..0>	6 63 64	FUNC_TEST=YES	
E33	UATA_DMARQ	63 64	FUNC_TEST=YES	
E35	UATA_DSTROBE	63 64	FUNC_TEST=YES	
E34	UATA_DMACK_L	63 64	FUNC_TEST=YES	Place within 50 mm
E36	UATA_DA<2..0>	6 63 64	FUNC_TEST=YES	of ODD/HDD connector.
E38	UATA_CS0_L	6 63 64	FUNC_TEST=YES	
E37	UATA_CS1_L	63 64	FUNC_TEST=YES	
E40	UATA_RESET_L	63 64	FUNC_TEST=YES	
E39	UATA_HSTROBE	63 64	FUNC_TEST=YES	
E41	UATA_STOP	63 64	FUNC_TEST=YES	
E42	UATA_INTRQ	63 64	FUNC_TEST=YES	

AUDIO

E76	PP5V_PWRON_AUDIO_PVDD	74	FUNC_TEST=YES	
E60	PP5V_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
E59	PP3V3_PWRON_AUDIO_AVDD	74	FUNC_TEST=YES	
E61	=PP3V3_RUN_AUDIO	10 74	FUNC_TEST=YES	
E44	=I2C_AUDIO_SCL	8 74	FUNC_TEST=YES	
E46	=I2C_AUDIO_SDA	8 74	FUNC_TEST=YES	
E48	I2S0_MCLK	6 74	FUNC_TEST=YES	
E47	I2S0_BITCLK	6 74	FUNC_TEST=YES	
E50	I2S0_SYNC	6 74	FUNC_TEST=YES	
E49	I2S0_SB_TO_DEV_DTO	6 74	FUNC_TEST=YES	
E51	I2S0_DEV_TO_SB_DTI	22 74	FUNC_TEST=YES	
E53	AUDIO_LO_MUTE_L	22 74	FUNC_TEST=YES	Place within 25 mm
E52	AUDIO_SPKR_MUTE_L	22 74	FUNC_TEST=YES	of audio connector.
E56	AUDIO_CODEC_RESET_L	22 74	FUNC_TEST=YES	
E55	AUDIO_SPDIFRX_RESET_L	22 74	FUNC_TEST=YES	
E57	AUDIO_LO_DET_L	22 74	FUNC_TEST=YES	
E58	AUDIO_LI_DET_L	22 74	FUNC_TEST=YES	
E107	AUDIO_LO_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
E108	AUDIO_LI_OPTICAL_PLUG_L	22 74	FUNC_TEST=YES	
E109	AUDIO_I2S_DTIB_SEL	22 74	FUNC_TEST=YES	
E111	AUDIO_EXT_MCLK_SEL	22 74	FUNC_TEST=YES	
E113	AUDIO_GPIO_11	22 74	FUNC_TEST=YES	
E114	GND_AUDIO_AGND	74	FUNC_TEST=YES	
E115	GND_AUDIO_PGND	74	FUNC_TEST=YES	

SYSTEM

E76	PP5V_TPAD_F	30	FUNC_TEST=YES	
E77	USB_TPAD_P	11 30	FUNC_TEST=YES	
E78	USB_TPAD_N	11 30	FUNC_TEST=YES	
E88	PP3V3_PWRON_DS1775_R	30	FUNC_TEST=YES	
E89	SYS_OVERTEMP_L	11 25 30	FUNC_TEST=YES	
E43	PP3V3_ALL_HALL_EFFECT_R	30	FUNC_TEST=YES	
E45	SYS_LID_OPEN_F	30	FUNC_TEST=YES	
E30	SYS_POWER_BUTTON_L_F	30	FUNC_TEST=YES	Place within 25 mm
E29	=FTP_SLEEP_LED	30	FUNC_TEST=YES	of TPAD connector.
E31	SYS_CHARGE_LED_L	24 74	FUNC_TEST=YES	
E87	SYS_ADAPTER_ANALOG_AC_DET	12 74	FUNC_TEST=YES	
E90	KBDLED_ANODE	28 30	FUNC_TEST=YES	
E91	KBDLED_RETURN	28 30	FUNC_TEST=YES	
E105	=I2C_DS1775_SDA	8 30	FUNC_TEST=YES	
E104	=I2C_DS1775_SCL	8 30	FUNC_TEST=YES	

CPU FAN

E100	=PP5V_FAN1_PWR	10 31	FUNC_TEST=YES	
E98	FAN1_TACH	27 31	FUNC_TEST=YES	Place within 25 mm
E97	FAN1_PWM	27 31	FUNC_TEST=YES	of fan connector.
E119	=FTP_GND	7 10	FUNC_TEST=YES	

GPU FAN

E102	=PP5V_FAN2_PWR	10 31	FUNC_TEST=YES	
E103	FAN2_TACH	27 31	FUNC_TEST=YES	Place within 25 mm
E104	FAN2_PWM	27 31	FUNC_TEST=YES	of fan connector.
E120	=FTP_GND	7 10	FUNC_TEST=YES	

ALS

E70	=PP3V3_PWRON_LEFT_ALS	10 31	FUNC_TEST=YES	
E68	ALS_0_OUT	25 31	FUNC_TEST=YES	Place within 25 mm
E69	ALS_GAIN_BOOST	25 28 31	FUNC_TEST=YES	of ALS connector.

SCCA

E72	SCCA_RXD	22 24	FUNC_TEST=YES	Place within 25 mm
E71	SCCA_TXD_L	22 24	FUNC_TEST=YES	of debug connector.

BACKUP BATT

E73	=PPVIO_BU_BATT	10 31	FUNC_TEST=YES	Place within 25 mm
E74	=PPVOUT_BU_BATT	10 31	FUNC_TEST=YES	of battery connector.

RT USB

E64	=PP5V_PWRON_RIGHT_USB	10 31	FUNC_TEST=YES	
E65	USB2_RIGHT_PORT_P	11 31	FUNC_TEST=YES	Place within 25 mm
E66	USB2_RIGHT_PORT_N	11 31	FUNC_TEST=YES	of right USB connector.

LT USB

E314	=PP5V_PWRON_LEFT_USB	10 74	FUNC_TEST=YES	
E316	USB2_LEFT_PORT_P	11 74	FUNC_TEST=YES	Place within 25 mm
E315	USB2_LEFT_PORT_N	11 74	FUNC_TEST=YES	of left USB connector.

Functional Test Points

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE SHT 7 OF 115

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
	I2C	I2C		I2C_PMU_SMB_SCL
	I2C	I2C		I2C_PMU_SMB_SDA
	I2C	I2C		I2C_PMU_SCL
	I2C	I2C		I2C_PMU_SDA
I2C_NB	I2C	I2C		I2C_I2_NB_SCL
I2C_NB	I2C	I2C		I2C_I2_NB_SDA
	I2C	I2C		I2C_I2_SB_SCL
	I2C	I2C		I2C_I2_SB_SDA
	I2C	I2C		I2C_GPU_TMDS_SCL
	I2C	I2C		I2C_GPU_TMDS_SDA

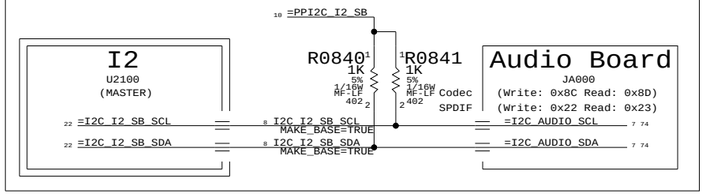
Page Notes

Power aliases required by this page:
(NONE)

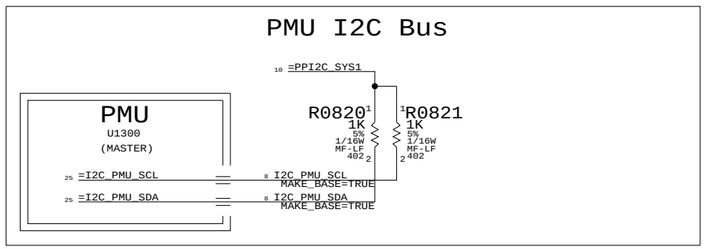
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GOV_I2C / GOV_I2C_BYPASS
  Allows bypassing Governator I2C bus.
  Most devices are connected directly to PMU unstead. One ADT7467 connects to NB I2C bus 1 to resolve address conflict.
- MMM_PWR_ALL / MMM_PWR_PWRON
  Selects whether MMM MCU is powered all the time or only when the system is on. ALL moves the MCU to the PMU I2C bus so it can be monitored by in shutdown.
  NOTE: Neither option is necessary when MMM_MCU_PMU BOM option is selected.

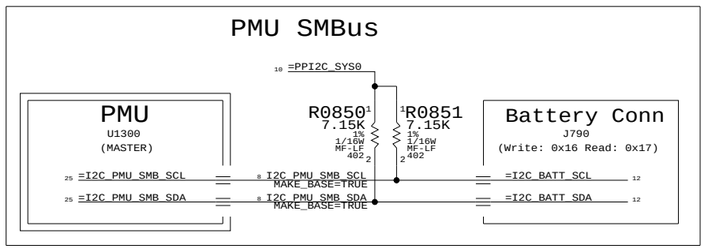
SouthBridge I2C Bus



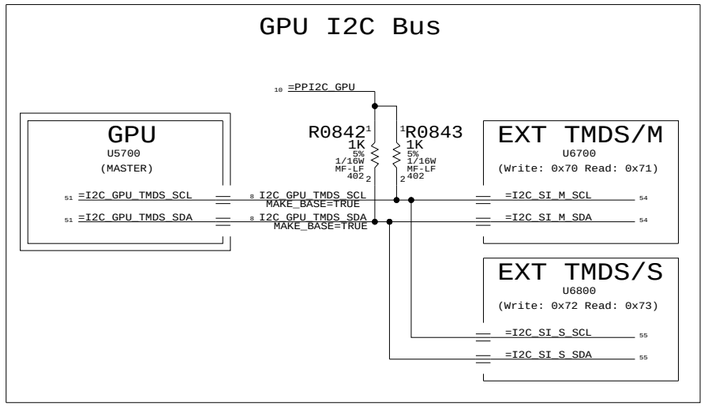
PMU I2C Bus



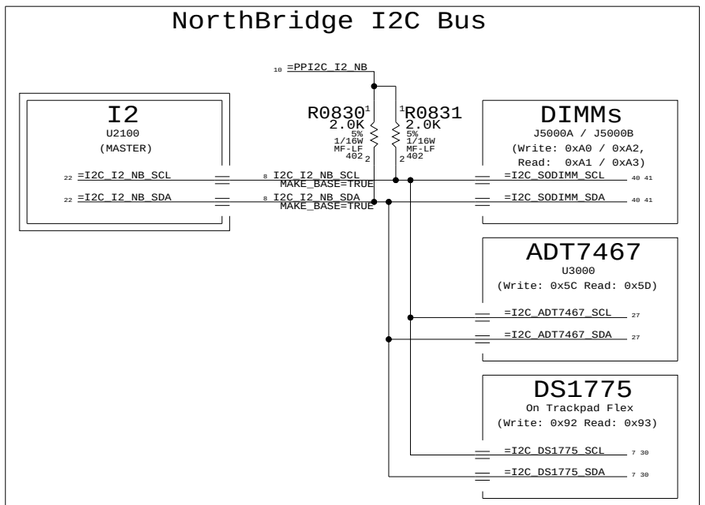
PMU SMBus



GPU I2C Bus



NorthBridge I2C Bus

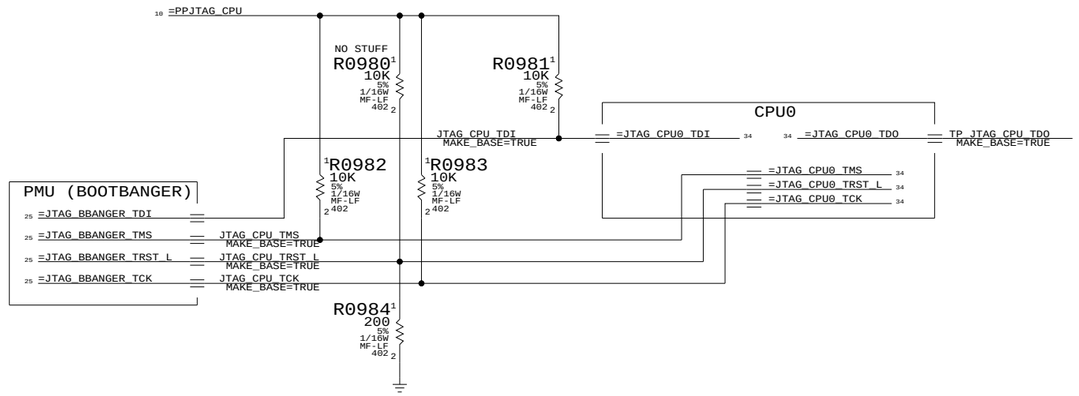


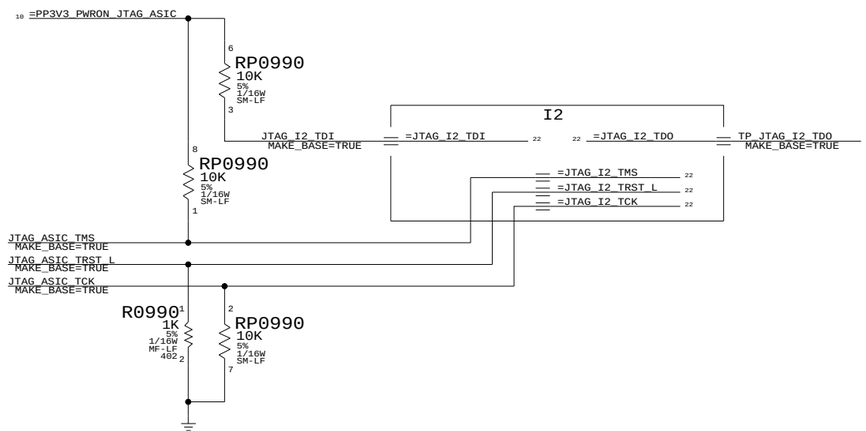
I2C Connections

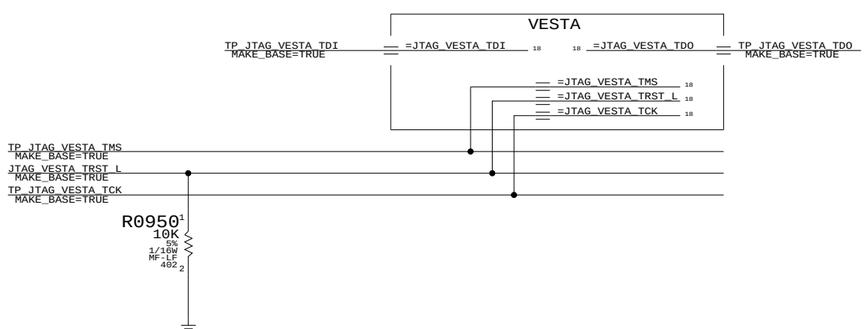
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	8	115







Nets not requiring TPs due to JTAG

MAXBUS

MA6	MAXBUS_DATA<63..0>	21 32 33	NO_TEST=YES
MA7	MAXBUS_ADDR<31..0>	32 33	NO_TEST=YES
MA8	MAXBUS_CI_L	32 33	NO_TEST=YES
MA9	MAXBUS_GBL_L	32 33	NO_TEST=YES
MA10	MAXBUS_TBST_L	32 33	NO_TEST=YES
MA11	MAXBUS_TSIZ<2..0>	32 33	NO_TEST=YES
MA12	MAXBUS_TT<4..0>	32 33	NO_TEST=YES
MA13	MAXBUS_WT_L	32 33	NO_TEST=YES
MA14	MAXBUS_DTI<2..0>	32 33	NO_TEST=YES

ENET

NE6	ENET_MDC	11 65	NO_TEST=YES
NE7	ENET_MDIO	11 65	NO_TEST=YES
NE8	ENET_TXD<7..0>	11	NO_TEST=YES
NE9	ENET_TX_EN	11	NO_TEST=YES
NE10	ENET_TX_ER	11	NO_TEST=YES
NE02	ENET_RXD<7..0>	11 65	NO_TEST=YES
NE01	ENET_RX_DV	11 65	NO_TEST=YES
NE03	ENET_RX_ER	11 65	NO_TEST=YES
NE04	ENET_COL	11 65	NO_TEST=YES
NE05	ENET_CRS	11 65	NO_TEST=YES

FIREWIRE

FW6	FW_D_R<7..0>	6 68	NO_TEST=YES
FW7	FW_D<7..0>	6 69	NO_TEST=YES
FW8	FW_CTL_R<1..0>	68 71	NO_TEST=YES
FW9	FW_CTL<1..0>	69 71	NO_TEST=YES
FW00	FW_LPS_R	68 71	NO_TEST=YES
FW03	FW_LPS	69 71	NO_TEST=YES
FW03	FW_LREQ_R	68 71	NO_TEST=YES
FW02	FW_LREQ	69 71	NO_TEST=YES

JTAG Connections

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE

SHT 9 OF 115

Power Synonyms

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 10 OF 115	

I2S0 Series Rs

RP1150
33
5%
1/16W
SM-LF

6 =RP1150P1 — 1 — 8 — =RP1150P8 6
6 =RP1150P2 — 2 — 7 — =RP1150P7 6
6 =RP1150P3 — 3 — 6 — =RP1150P6 6
6 =RP1150P4 — 4 — 5 — =RP1150P5 6

One resistor for each of:
- I2S0_SB_TO_DEV_DTO(_R)
- I2S0_MCLK(_R)
- I2S0_BITCLK(_R)
- I2S0_SYNC(_R)

I2S1 Series Rs

RP1151
33
5%
1/16W
SM-LF

6 =RP1151P1 — 1 — 8 — =RP1151P8 6
6 =RP1151P2 — 2 — 7 — =RP1151P7 6
6 =RP1151P3 — 3 — 6 — =RP1151P6 6
6 =RP1151P4 — 4 — 5 — =RP1151P5 6

One resistor for each of:
- I2S1_SB_TO_DEV_DTO(_R)
- I2S1_MCLK(_R)
- I2S1_BITCLK(_R)
- I2S1_SYNC(_R)

GPU

R1140
22
5%
1/16W
MF-LF
402

43 AGP_CLK66M_GPU_R — 1 — 2 — AGP_CLK66M_GPU 44

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =AGP_GPU_RESET_L 44

AGP_VREF — MAKE_BASE=TRUE — VOLTAGE=0.75V — MIN_LINE_WIDTH=0.25 mm — MIN_NECK_WIDTH=0.15 mm
- =I2_AGP_VREF 43
- =AGP_VREF 44
- =GPU_AGP_VREF 44

51 TP_EXTTMDS_RESET_L — SI_TMDS_RESET_L — MAKE_BASE=TRUE — =SI_TMDS_RESET_L 54 55

CPU Clocks

R1110
10
5%
1/16W
MF-LF
402

32 MAXBUS_CLK_CPU0_R — 1 — 2 — MAXBUS_CLK_CPU0 — MAKE_BASE=TRUE — =MAXBUS_CPU0_CLK 33

MAXBUS_TBEN_SYNC

R1111
10
5%
1/16W
MF-LF
402

32 TP_MAXBUS_CLK_CPU1_R — MAXBUS_CLK_CPU1_R — MAKE_BASE=TRUE — 1 — 2 — MAXBUS_CLK_TBEN_SYNC — MAKE_BASE=TRUE — =SYSCLK_TBEN_SYNC 21

USB Controller Mux

R1160 0 — USB2_NEC — USB2_NEC_LEFT_PORT_P
R1161 0 — USB2_I2 — USB2_I2_LEFT_PORT_P
74 7 USB2_LEFT_PORT_P — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB2_LT_PORT — 6 11

R1162 0 — USB2_NEC — USB2_NEC_LEFT_PORT_N
R1163 0 — USB2_I2 — USB2_I2_LEFT_PORT_N
74 7 USB2_LEFT_PORT_N — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB2_LT_PORT — 6 11

R1164 0 — USB2_NEC — USB2_NEC_RIGHT_PORT_P
R1165 0 — USB2_I2 — USB2_I2_RIGHT_PORT_P
31 7 USB2_RIGHT_PORT_P — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB2_RT_PORT — 6 11

R1166 0 — USB2_NEC — USB2_NEC_RIGHT_PORT_N
R1167 0 — USB2_I2 — USB2_I2_RIGHT_PORT_N
31 7 USB2_RIGHT_PORT_N — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB2_RT_PORT — 6 11

R1170 0 — USB1P1_NEC — USB_NEC_BT_P
R1171 0 — USB1P1_I2 — USB_I2_BT_P
60 USB_BT_P — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB_BT — 6 11

R1172 0 — USB1P1_NEC — USB_NEC_BT_N
R1173 0 — USB1P1_I2 — USB_I2_BT_N
60 USB_BT_N — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB_BT — 2 6 11

R1174 0 — USB1P1_NEC — USB_NEC_TPAD_P
R1175 0 — USB1P1_I2 — USB_I2_TPAD_P
30 7 USB_TPAD_P — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB_TPAD — 6 11

R1176 0 — USB1P1_NEC — USB_NEC_TPAD_N
R1177 0 — USB1P1_I2 — USB_I2_TPAD_N
30 7 USB_TPAD_N — NET_SPACING_TYPE=USB2 — NET_PHYSICAL_TYPE=USB2 — DIFFERENTIAL_PAIR=USB_TPAD — 6 11

PCI

R1120 22 — 59 TP_PCI_CLK33M_SLOTA_R — PCI_CLK33M_ZDB_R — MAKE_BASE=TRUE — PCI_CLK33M_ZDB — MAKE_BASE=TRUE — =PCI_CLK33M_ZDB_IN 23

MAXBUS_TBEN_SYNC

R1130 22 — 59 TP_PCI_CLK33M_SLOTD_R — PCI_CLK33M_TBEN_SYNC_R — MAKE_BASE=TRUE — PCI_CLK33M_TBEN_SYNC — MAKE_BASE=TRUE — =CLK33M_TBEN_SYNC 21

R1135 0 — 23 =PCI_CLK33M_ZDBOUT_R<0> — PCI_CLK33M_AIRPORT_R — MAKE_BASE=TRUE — PCI_CLK33M_AIRPORT — MAKE_BASE=TRUE — =PCI_CLK33M_AIRPORT 60

- 59 PCI_SLOTA_REQ_L — 6 — PCI_AIRPORT_REQ_L — MAKE_BASE=TRUE — =PCI_AIRPORT_REQ_L 60
- 59 PCI_SLOTA_GNT_L — 6 — PCI_AIRPORT_GNT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_GNT_L 60
- 59 22 PCI_SLOTA_INT_L — PCI_AIRPORT_INT_L — MAKE_BASE=TRUE — =PCI_AIRPORT_INT_L 60
- 62 61 60 59 58 PCI_AD<17> — MAKE_BASE=TRUE — =PCI_AIRPORT_IDSEL 60
- 25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_AIRPORT_RESET_L 60

R1136 0 — 23 =PCI_CLK33M_ZDBOUT_R<1> — PCI_CLK33M_CBUS_R — MAKE_BASE=TRUE — PCI_CLK33M_CBUS — MAKE_BASE=TRUE — =PCI_CLK33M_CBUS 61

- 59 PCI_SLOTD_REQ_L — 6 — PCI_CBUS_REQ_L — MAKE_BASE=TRUE — =PCI_CBUS_REQ_L 61
- 59 PCI_SLOTD_GNT_L — 6 — PCI_CBUS_GNT_L — MAKE_BASE=TRUE — =PCI_CBUS_GNT_L 61
- 59 22 PCI_SLOTD_INT_L — PCI_CBUS_INT_L — MAKE_BASE=TRUE — =PCI_CBUS_INT_L 61
- 62 61 60 59 58 PCI_AD<20> — MAKE_BASE=TRUE — =PCI_CBUS_IDSEL 61
- 25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_CBUS_RESET_L 61

R1137 0 — 23 =PCI_CLK33M_ZDBOUT_R<2> — PCI_CLK33M_USB2_R — MAKE_BASE=TRUE — PCI_CLK33M_USB2 — MAKE_BASE=TRUE — =PCI_CLK33M_USB2 62

- 22 PCI_SLOTE_REQ_L — PCI_USB2_REQ_L — MAKE_BASE=TRUE — =PCI_USB2_REQ_L 62
- 22 PCI_SLOTE_GNT_L — PCI_USB2_GNT_L — MAKE_BASE=TRUE — =PCI_USB2_GNT_L 62
- 22 PCI_SLOTE_INT_L — PCI_USB2_INT_L — MAKE_BASE=TRUE — =PCI_USB2_INT_L 62
- 62 61 60 59 PCI_AD<21> — MAKE_BASE=TRUE — =PCI_USB2_IDSEL 62
- 25 11 PCI_RESET_L — MAKE_BASE=TRUE — =PCI_USB2_RESET_L 62

23 =PCI_CLK33M_ZDBOUT_R<3> — TP_PCI_CLK33M_ZDBOUT3 — MAKE_BASE=TRUE

USB Port Assignments

11 6 USB2_I2_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<0> 72
11 6 USB2_I2_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<0> 72
11 6 USB2_I2_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_I2_P<2> 72
11 6 USB2_I2_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_I2_N<2> 72
11 6 USB_I2_BT_P — MAKE_BASE=TRUE — USB2_I2_P<4> 72
11 6 USB_I2_BT_N — MAKE_BASE=TRUE — USB2_I2_N<4> 72
11 6 USB_I2_TPAD_P — MAKE_BASE=TRUE — USB2_I2_P<5> 72
11 6 USB_I2_TPAD_N — MAKE_BASE=TRUE — USB2_I2_N<5> 72

11 6 USB2_NEC_LEFT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<0> 73
11 6 USB2_NEC_LEFT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<0> 73
11 6 USB2_NEC_RIGHT_PORT_P — MAKE_BASE=TRUE — USB2_NEC_P<1> 73
11 6 USB2_NEC_RIGHT_PORT_N — MAKE_BASE=TRUE — USB2_NEC_N<1> 73
11 6 USB_NEC_BT_P — MAKE_BASE=TRUE — USB2_NEC_P<2> 73
11 6 2 USB_NEC_BT_N — MAKE_BASE=TRUE — USB2_NEC_N<2> 73
11 6 USB_NEC_TPAD_P — MAKE_BASE=TRUE — USB2_NEC_P<3> 73
11 6 USB_NEC_TPAD_N — MAKE_BASE=TRUE — USB2_NEC_N<3> 73

PMU Connections

30 25 7 SYS_OVERTEMP_L — MAKE_BASE=TRUE — =ADT7467_THERM_L 27
13 PMU_CHARGE_V — MAKE_BASE=TRUE — TP_PMU_P7_5 25
25 PMU_CPU_HRESET_L — MAKE_BASE=TRUE — =CPU_HRESET_L 34
12 SYS_PMU_ANALOG_AC_DET — MAKE_BASE=TRUE — TP_PMU_AN_P10_6 25
25 GOV_RESET_L — TP_GOV_RESET_L — MAKE_BASE=TRUE
25 PMU_CPU_CLK_EN — MAKE_BASE=TRUE — =I2_STOPCPU_L 22
25 PMU_SYS_CLK_EN — MAKE_BASE=TRUE — =I2_STOPXTAL_L 22

26 SYS_PWRSEQ_1 — MAKE_BASE=TRUE — TP_PMU_AN_P0_1 25
26 SYS_PWRSEQ_2 — MAKE_BASE=TRUE — TP_PMU_AN_P0_2 25
26 SYS_PWRSEQ_3_L — MAKE_BASE=TRUE — TP_PMU_AN_P0_3 25
26 SYS_PWRSEQ_4 — MAKE_BASE=TRUE — TP_PMU_AN_P0_4 25
26 SYS_PWRSEQ_5 — MAKE_BASE=TRUE — TP_PMU_AN_P0_5 25
26 SYS_PWRSEQ_6_L — MAKE_BASE=TRUE — TP_PMU_P7_4 25
26 SYS_PWRSEQ_FINAL — MAKE_BASE=TRUE — TP_PMU_AN_P10_5 25

I40C TP_PMU_P3_0 — MAKE_BASE=TRUE — 25
I40C TP_PMU_P3_1 — MAKE_BASE=TRUE — 25
I40C TP_PMU_P3_2 — MAKE_BASE=TRUE — 25
I40C TP_PMU_P3_3 — MAKE_BASE=TRUE — 25

Vesta Ethernet

65 ENET_TX_EN_R — 9 — ENET_TX_EN — MAKE_BASE=TRUE — =ENET_TX_EN 66
65 ENET_TX_ER_R — 9 — ENET_TX_ER — MAKE_BASE=TRUE — =ENET_TX_ER 66
65 ENET_TXD_R<7..0> — 9 — ENET_TXD<7..0> — MAKE_BASE=TRUE — =ENET_TXD<7..0> 66
65 ENET_RESET_L
R1185 1 — 100K — 5% — 1/16W — MF-LF — 402 — 2
65 9 ENET_RXD<7..0> — MAKE_BASE=TRUE — =ENET_RXD_R<7..0> 66
65 9 ENET_RX_DV — MAKE_BASE=TRUE — =ENET_RX_DV_R 66
65 9 ENET_RX_ER — MAKE_BASE=TRUE — =ENET_RX_ER_R 66
65 9 ENET_COL — MAKE_BASE=TRUE — =ENET_COL_R 66
65 9 ENET_CRS — MAKE_BASE=TRUE — =ENET_CRS_R 66
65 ENET_CLK125M_GBE_REF — MAKE_BASE=TRUE — =VESTA_CLK125M_GBE_REF 66
65 ENET_CLK125M_RX — MAKE_BASE=TRUE — =VESTA_CLK125M_RX 66
65 ENET_CLK25M_TX — MAKE_BASE=TRUE — =VESTA_CLK25M_TX 66
65 9 ENET_MDC — MAKE_BASE=TRUE — =VESTA_MDC 66
65 9 ENET_MDIO — MAKE_BASE=TRUE — =VESTA_MDIO 66
TP_ENET_ENERGYDET — MAKE_BASE=TRUE — =VESTA_ENERGYDET 66

MISC

25 11 PCI_RESET_L — MAKE_BASE=TRUE — =ROM_PWD_L 58
32 TP_MAXBUS_CPU1_QACK_L — NC_MAXBUS_CPU1_QACK_L — MAKE_BASE=TRUE — NO_TEST=YES
22 I2_GPIO_11 — TP_I2_GPIO_11 — MAKE_BASE=TRUE
22 I2_GPIO_EXT_02 — CPU0_VID_AB_SEL — MAKE_BASE=TRUE — =CPU0_VID_AB_SEL 36
22 =SPI_I2_REQ — CPU0_MAX1717_AB_SEL — MAKE_BASE=TRUE — =CPU0_MAX1717_AB_SEL 36
24 =SLEEP_LED_IOUT — SLEEP_LED_IOUT — MAKE_BASE=TRUE — MIN_LINE_WIDTH=0.25 mm — MIN_NECK_WIDTH=0.25 mm — =SLEEP_LED_CONN 30

Signal Synonyms

SYNC_MASTER=N/A — SYNC_DATE=N/A

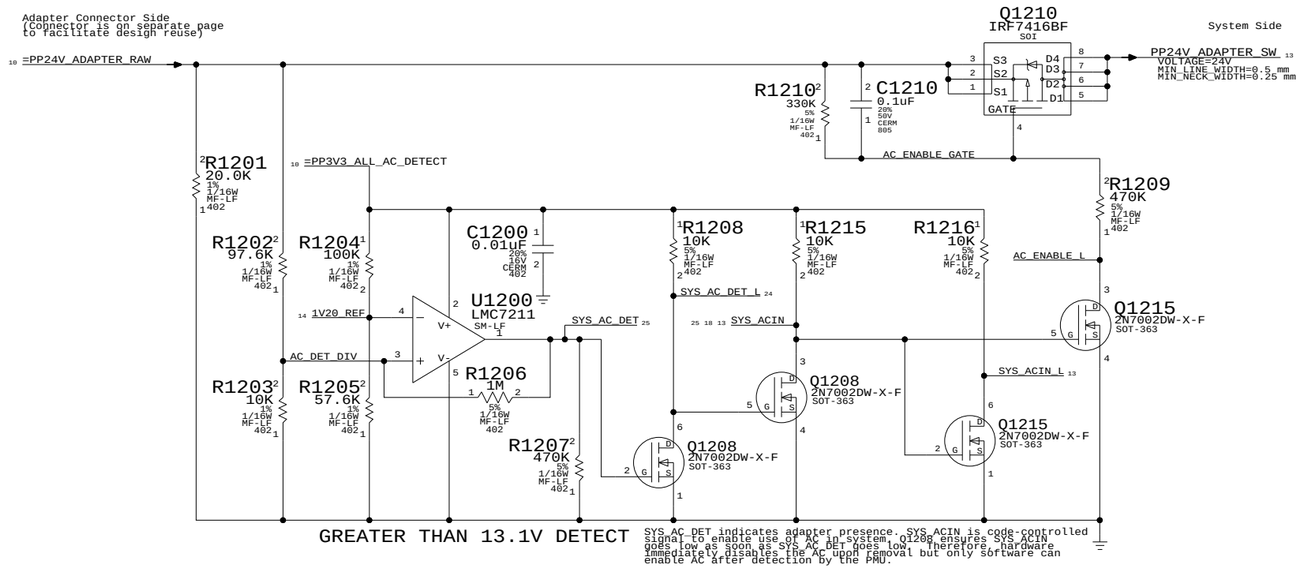
APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 11 OF 115

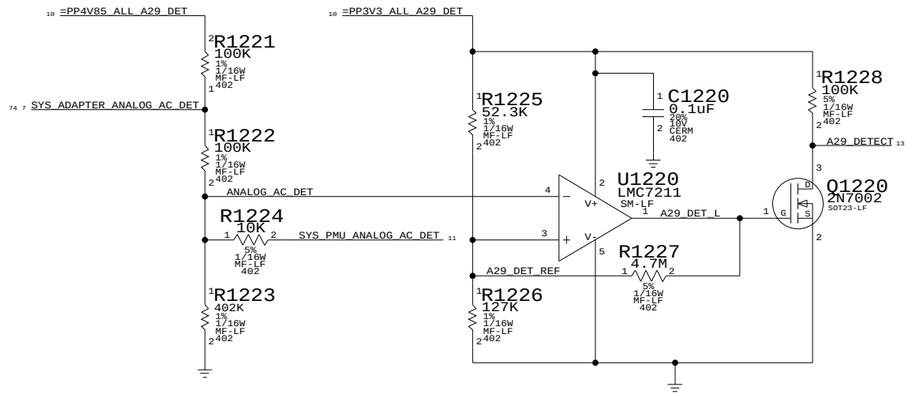
NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
P31V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINP
P30V	THERM	THERM	BATTERY_ISNS	PPVBATT_ISNS_VINN

ADAPTER INPUT/INRUSH LIMITER



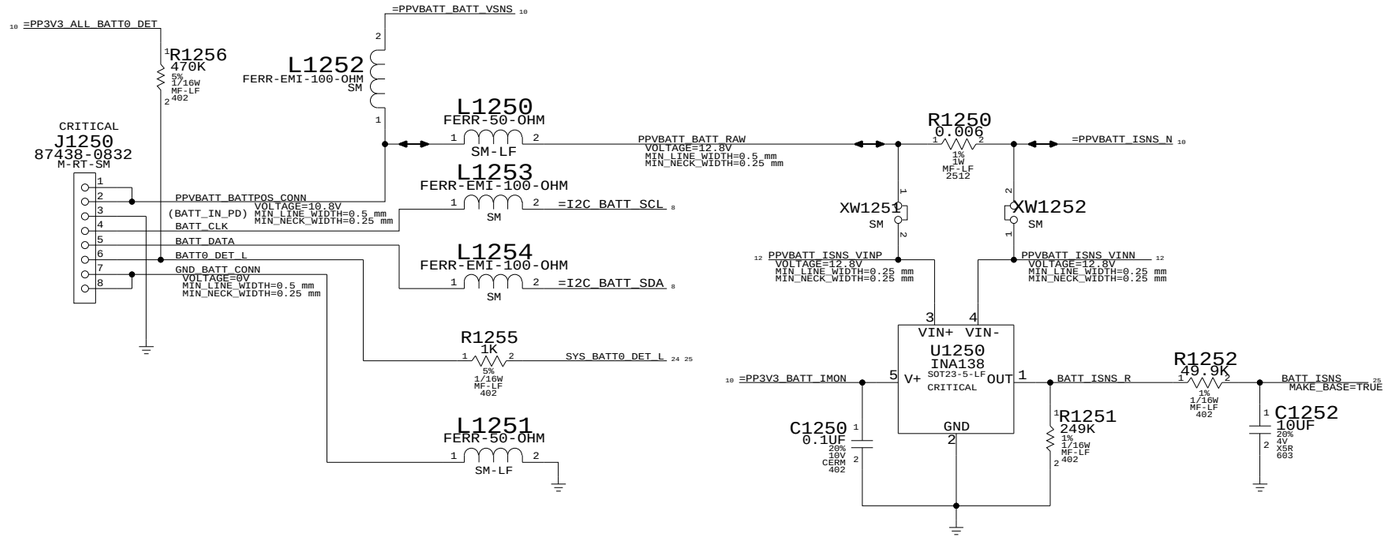
SYS_AC_DET indicates adapter presence. SYS_ACIN is code-controlled signal to enable use of AC by system. Q1208 ensures SYS_ACIN goes low as soon as SYS_AC_DET goes low. Therefore, hardware immediately disables the AC upon removal but only software can enable AC after detection by the PMU.

A29 ADAPTER DETECTION



ADAPTER IDs		
ADAPTER	ID RANGE	PIN VOLTAGE
Q11 (65W)	1.65-2.31V	2.007-2.066V
A29 (45W)	2.31-2.97V	2.558-2.661V
AIRLINE	0.33-0.99V	0.589-0.663V

BATTERY INPUT/CURRENT SENSE



Power Inputs

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 12 OF 115	

BACKFEED PROTECTION

PP24V_ADAPTER_SW

Q1360 IRF7416BF SOI — D1 D2 D3 D4 S1 S2 S3 GATE

PP24V_ADAPTER_ILIM_P — VOLTAGE=24V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

R1360 47K 5% 1/16W MF-LF 402

BKFD_PROT_GATE

R1361 68K 5% 1/16W MF-LF 402

C1361 0.01UF 20% 50V CERM 603

BKFD_PROT_EN_L

Q1392 2N7002DW-X-F SOT-363 — SYS_ACIN

PLACE U1370 NEXT TO R1300

C1370 0.01uF 20% 50V CERM 603

U1370 MAX4172 TSSOP-LF — CRITICAL — V+ RS+ RS- NC1 NC2 PG GND OUT NC NC

=PP14VR24V_ALL_PBUS_A

Place close to RS-

C1371 0.1UF 10% 50V X7R 603-1

CRITICAL R1370 2.21k 0.1% 1/16W MF-LF 603

MAX4172_OUT

+PBUS CURRENT LIMIT

R1386 1K 1% 1/16W MF-LF 402 — IAC_RC_COMP

C1386 0.1uF 20% 10V CERM 402

=PP3V3_ALL_PBUS_ILIM

C1380 0.1uF 20% 10V CERM 402

CRITICAL R1380 42.2K 0.1% 1/16W MF-LF 603 — IAC_FB

R1385 10K 1% 1/16W MF-LF 402

U1380 LMC7111BIM5 SOT23-5 LF — DP1390 BAS16TW-X-F SOT-363

LTC1625_ITH

R1387 150 1% 1/16W MF-LF 402 — 1625_COMP

ADAPTER_I_REG

PLACE R383 CLOSE TO LTC1625
ROUTE LTC1625_ITH CAREFULLY

CURRENT_THRESHOLD

CRITICAL R1381 42.2K 0.1% 1/16W MF-LF 603

CRITICAL R1382 82.5K 0.1% 1/16W MF-LF 603

CRITICAL R1383 51.1K 0.1% 1/16W MF-LF 603

A29_CURRENT_ADJ

R1384 100K 5% 1/16W MF-LF 402 — =PP3V3_ALL_PBUS_ILIM

Q1330 2N7002DW-X-F SOT-363 — A29_DETECT

Q1384 2N7002DW-X-F SOT-363 — AC_GTR_18V

OVER_18V_ADJ

Q1384 2N7002DW-X-F SOT-363 — 1772_ACOK_L

C1384 1uF 20% 10V CERM 603

BATTERY SWITCH-OVER CIRCUIT

=PPVBATT_BATT

F1390 5AMP-125V SM-LF

F1395 5AMP-125V SM-LF

=PPVBATT_BATT_PBUSA

=PPVBATT_BATT_PBUSB

PPVBATT_BATT_PBUSA_FUSE — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

PPVBATT_BATT_PBUSB_FUSE — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

CRITICAL Q1390 IRF7416BF SOI — D1 D2 D3 D4 S1 S2 S3 GATE

CRITICAL Q1395 SUD45P03 TO-252-LF — D G S

R1390 47K 5% 1/16W MF-LF 402

R1395 47K 5% 1/16W MF-LF 402

BATT_24V_GATE

BATT_14V_GATE

R1391 10K 5% 1/16W MF-LF 402

R1396 10K 5% 1/16W MF-LF 402

DP1390 BAS16TW-X-F SOT-363

SYS_ACIN_L

DP1390 BAS16TW-X-F SOT-363

R1392 158K 1% 1/16W MF-LF 402

BATT_24PBUS_EN

BATT_14PBUS_EN

Q1392 2N7002DW-X-F SOT-363

SYS_ACIN_L_RC

C1392 10uF 20% 25V X5R 603

WHEN AC IS IN, P-CHANNEL FETS ARE QUICKLY (DIODE) TURNED OFF
WHEN AC IS NOT PLUGGED, P-CHANNEL FETS ARE ON
RC TIME IS 480K*10UF @ +3V_PMU

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
114S0343	1	RES,20K,1%,1/16W,MF-LF,402	R1345	Q16C_PARTS
114S0382	1	RES,48.7K,1%,1/16W,MF-LF,402	R1345	Q41C_PARTS

SWITCHER VOLTAGE CONTROL

PMU SELECTS BETWEEN TWO VOLTAGES

=PP3V3_ALL_BATT_CHGR

R1341 27.4K 1% 1/16W MF-LF 402

R1344 10K 1% 1/16W MF-LF 402

R1346 10K 1% 1/16W MF-LF 402

OD OUTPUT LOW - WHEN AC GREATER THAN 18V

R1342 4.12K 1% 1/16W MF-LF 402

R1345 20.0K 1% 1/16W MF-LF 402 — OMIT

BATTV_HIGH

R1340 100K 5% 1/16W MF-LF 402

Q1340 2N7002DW-X-F SOT-363

R1343 5.23K 1% 1/16W MF-LF 402

BATTV_LOW

Q1340 2N7002DW-X-F SOT-363 — PMU_CHARGE_V

=PP3V3_ALL_BATT_CHGR

R1347 100K 5% 1/16W MF-LF 402

Q1347 2N7002DW-X-F SOT-363 — CHARGE_DISABLE

Q1347 2N7002DW-X-F SOT-363 — PMU_BATT0_CHARGE

$V_{BATT} = CELLS \times (4.096 + (0.4096 * V_{VCTL} / V_{REFIN}))$

For 4.15V cells, VCTL = 0.123 REFIN

For 4.20V cells, VCTL = 0.245 REFIN

$I_{CHG} = (0.2048/R_{\_62}) * (V_{ICTL} / V_{REFIN})$

SWITCHER CURRENT CONTROL

CHARGE DISABLED BY PMU OR INPUT VOLTAGE <18V

CHARGE THROTTLED BY LOW BATTERY VOLTAGE

R1348 1K 1% 1/16W MF-LF 402

R1323 1K 1% 1/16W MF-LF 402

BATT_LOW_L

Q1348 2N7002DW-X-F SOT-363

Q1348 2N7002DW-X-F SOT-363

R1325 1K 1% 1/16W MF-LF 402

C1325 0.01uF 20% 16V CERM 402

C1326 0.01uF 20% 16V CERM 402

1772_CCV_RC

1772_REF

R1324 1K 1% 1/16W MF-LF 402

C1324 0.1uF 20% 10V CERM 402

C1327 1uF 20% 10V CERM 603

R1328 10K 1% 1/16W MF-LF 402

R1329 4.12K 1% 1/16W MF-LF 402

1772_CLS

VOLTAGE=0V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

=PP3V3_ALL_BATT_CHGR

1772_GND

C1350 0.1uF 20% 16V CERM 402

U1350 LMC7211 SM-LF

R1353 100K 1% 1/16W MF-LF 402

R1354 100K 1% 1/16W MF-LF 402

R1351 499K 1% 1/16W MF-LF 402

R1352 100K 1% 1/16W MF-LF 402

C1352 0.047uF 10% 16V CERM 402

BATT_LOW

BATT_DIV

1V65_REF

R1330 6.34K 1% 1/16W MF-LF 402

A29_CLS_ADJ

Q1330 2N7002DW-X-F SOT-363 — A29_DETECT

PP24V_ADAPTER_SW

R1300 0.025 1% 1W MF 2512-1 — CRITICAL

R1301 4.7 5% 1/16W MF-LF 402

R1302 4.7 5% 1/16W MF-LF 402

1772_CSSP

1772_CSSN

D1303 MMBD914XXG SOT23

R1321 100K 1% 1/16W MF-LF 402

R1322 12.7K 1% 1/16W MF-LF 402

C1301 0.47UF 10% 50V CERM 1210

C1303 1UF 20% 50V CERM 1210

C1302 0.47UF 10% 50V CERM 1206

C1304 0.47UF 10% 50V CERM 1206

U1300 MAX1772 QSOP-LF — CRITICAL — CSSP CSSN DCIN ACIN ACOK RFIN VCTL ICTL ICHG IINP CCV CCI CCS CELLS LDO DLOV BST DHI LX DLO PGND CSIP CSIN BATT GND

1772_DCIN
1772_ACIN
1772_ACOK_L
(+3V_PMU)
1772_VCTL
1772_ICTL
1772_ICHG
1772_IINP
1772_CCV
1772_CCI
1772_CCS
1772_CELLS
1772_DLOV
1772_BST
1772_DHI
1772_LX
1772_DLO
(GND)
1772_CSIP
1772_CSIN

R1319 33 5% 1/4W MF-LF 1206

D1319 MMBD914XXG SOT23

1772_LDO

1772_BST_ESR

R1317 100K 5% 1/16W MF-LF 402

C1319 0.1uF 20% 25V CERM 603

R1320 4.7 5% 1/10W MF-LF 603

C1320 0.1uF 20% 50V CERM 805

C1317 0.1uF 20% 25V CERM 603

C1322 0.1uF 20% 25V CERM 603

C1323 0.1uF 20% 25V CERM 603

R1318 100K 1% 1/16W MF-LF 402

XW1300 SM

NO STUFF
C1321 0.0022UF 10% 50V CERM 402

=PPVIN_ALL_BATT_CHGR

C1312 2.2UF 10% 50V X7R 1206

C1313 2.2UF 10% 50V X7R 1206

C1314 2.2UF 10% 50V X7R 1206

C1315 2.2UF 10% 50V X7R 1206

C1316 2.2UF 10% 50V X7R 1206

CRITICAL Q1300 RLA130N03 SO8

CRITICAL L1300 10uH SM1-LF

R1303 0.05 1% 1W MF 2512

PPVBATT_BATT_PBUSA_FUSE — MAKE_BASE=TRUE

=PPVOUT_BATT_CHRG

PPVOUT_BATT_CHRG_R — VOLTAGE=14V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm

CRITICAL D1300 SMB MBRS140XXG

CRITICAL Q1301 IRF7811W SO-8-LF

R1304 1 5% 1/10W MF-LF 603

R1305 1 5% 1/10W MF-LF 603

C1305 4.7uF 20% 25V CERM 1206

C1306 4.7uF 20% 25V CERM 1206

C1307 4.7uF 20% 25V CERM 1206

C1308 4.7uF 20% 25V CERM 1206

C1309 4.7uF 20% 25V CERM 1206

C1310 4.7uF 20% 25V CERM 1206

C1311 33uF 20% 20V ELEC SM1

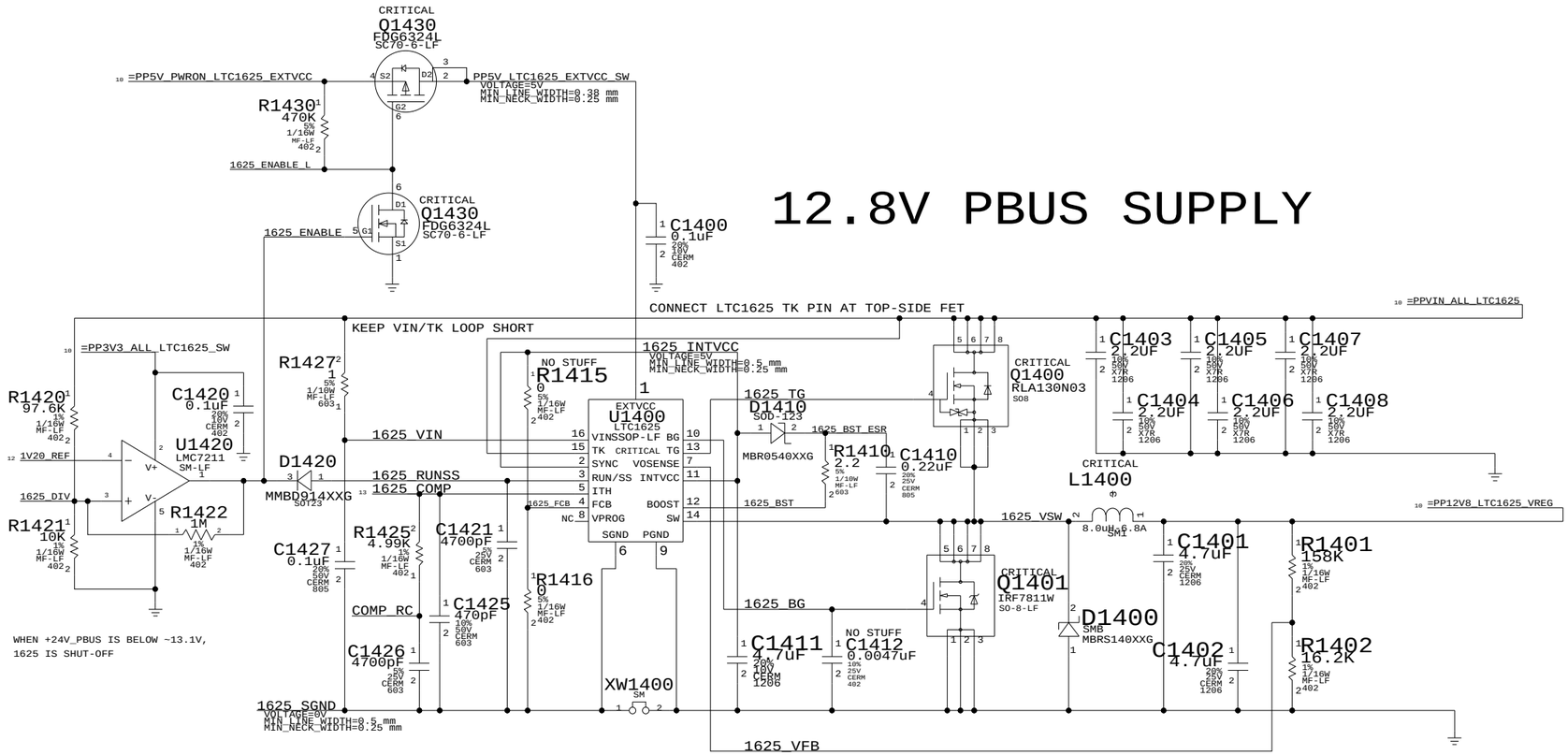
Battery Charger

SYNC_MASTER=N/A — SYNC_DATE=N/A

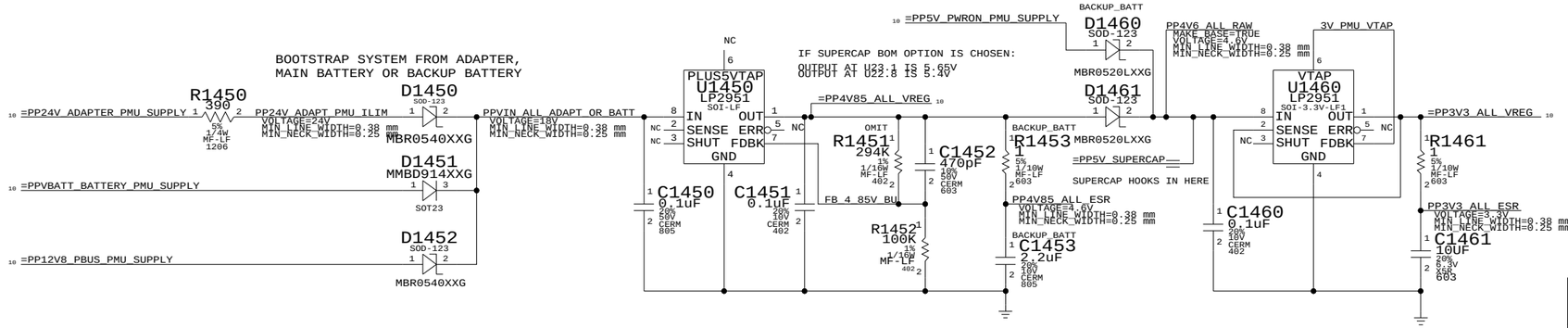
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 13 OF 115	

12.8V PBUS SUPPLY



PMU SUPPLY



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
114S2945	1	RES,MF,1/16W,394K OHM,1%,0402,SMD	R1451	?	BACKUP_BATT
114S3575	1	RES,MF,1/16W,357K OHM,1%,0402,SMD	R1451	?	SUPERCAP

12.8V PBUS/PMU Supplies

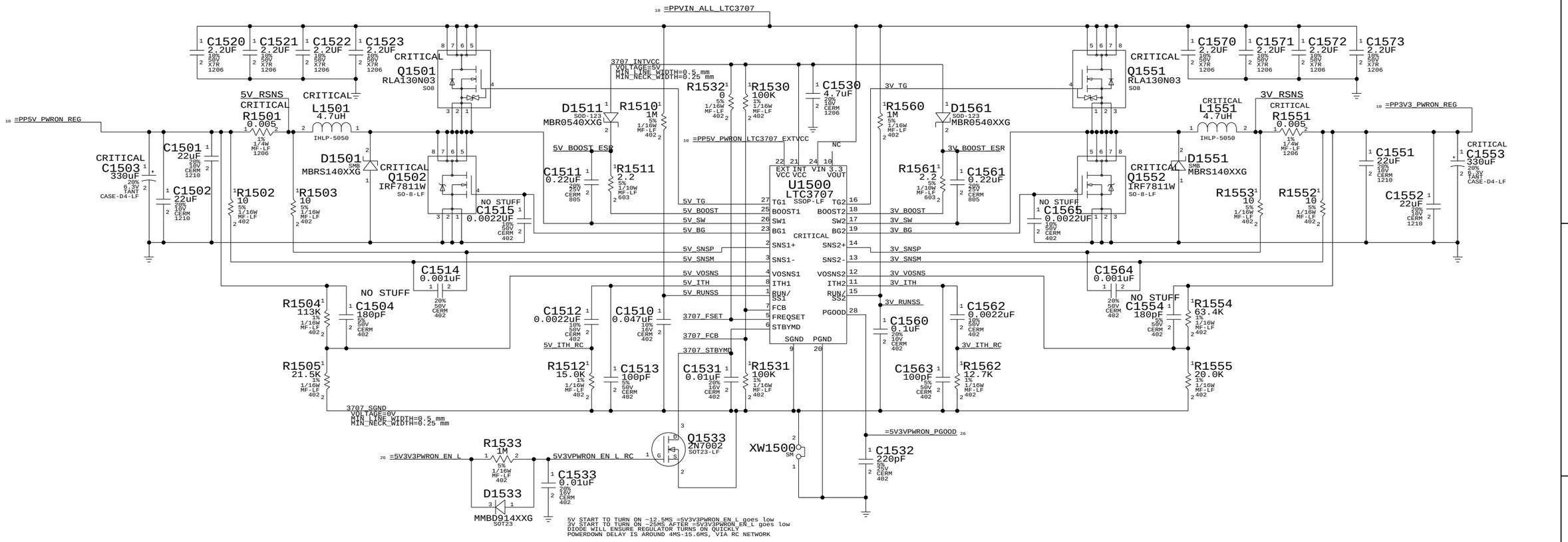
SYNC_MASTER=N/A SYNC_DATE=N/A

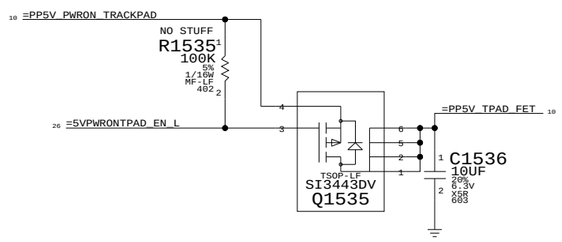
APPLE COMPUTER INC.

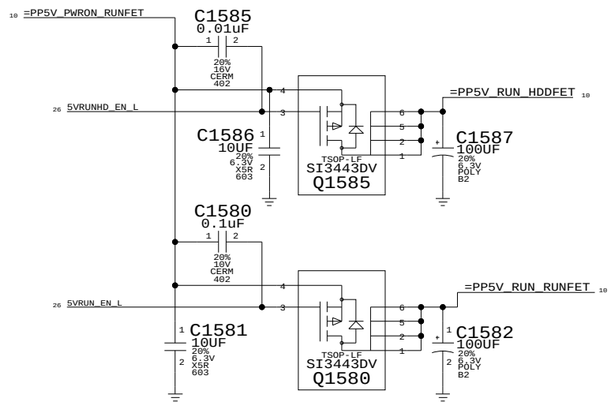
SIZE	DRAWING NUMBER	REV.
D	051-6929	03

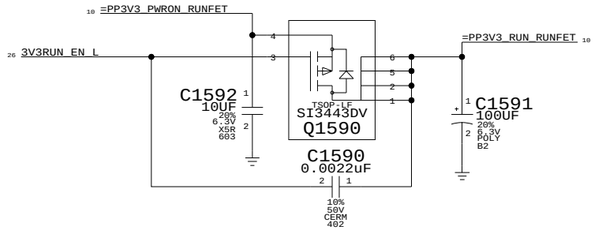
SCALE	SHT	OF
NONE	14	115

3.3V/5V SWITCHER









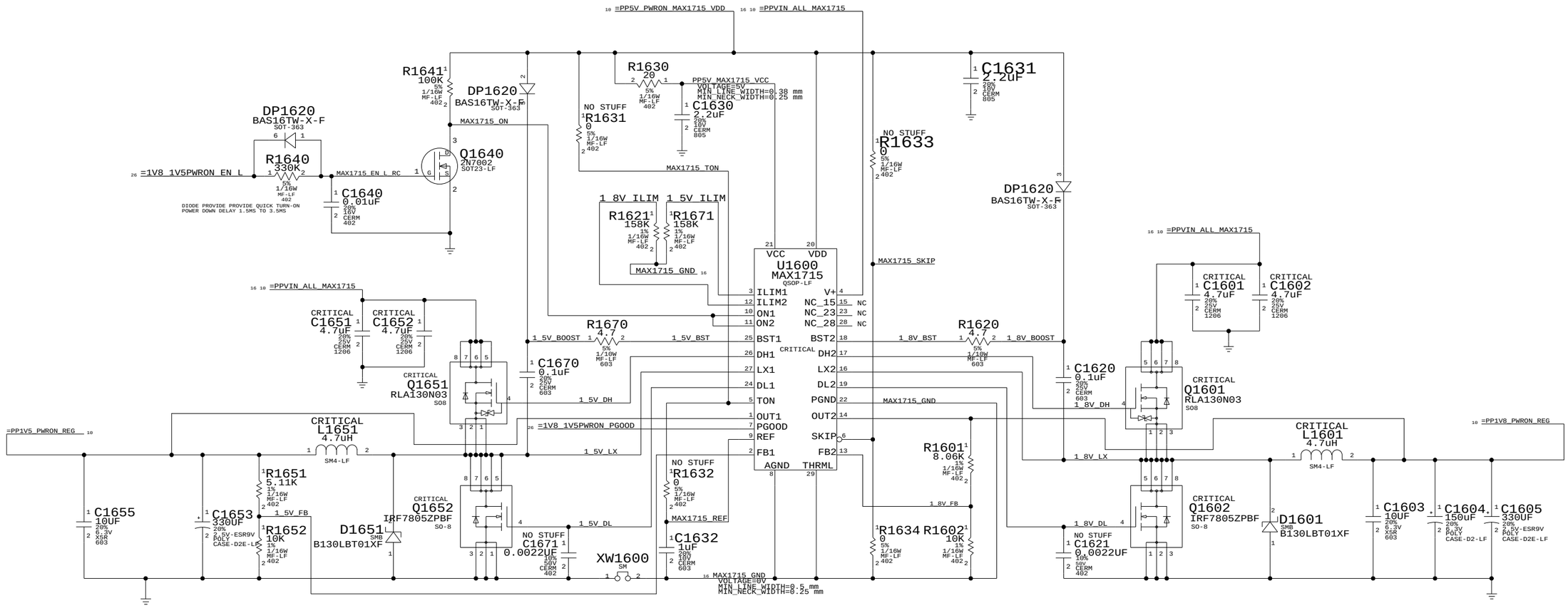
5V/3.3V Supplies

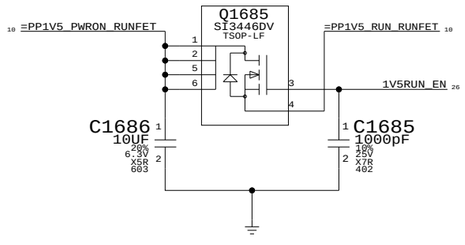
SYNC_MASTER=N/A SYNC_DATE=N/A

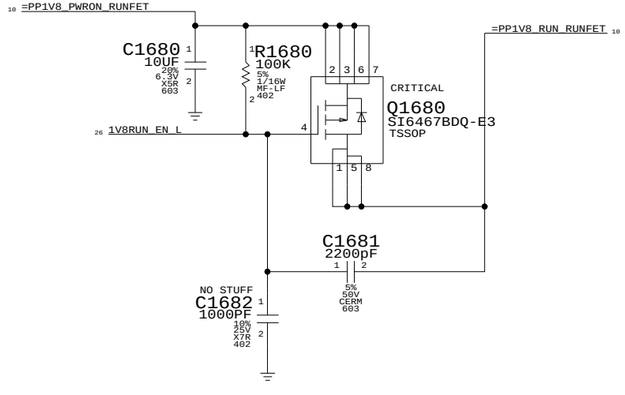
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 15 OF 115	

1.5V/1.8V SWITCHER







1.8V/1.5V Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

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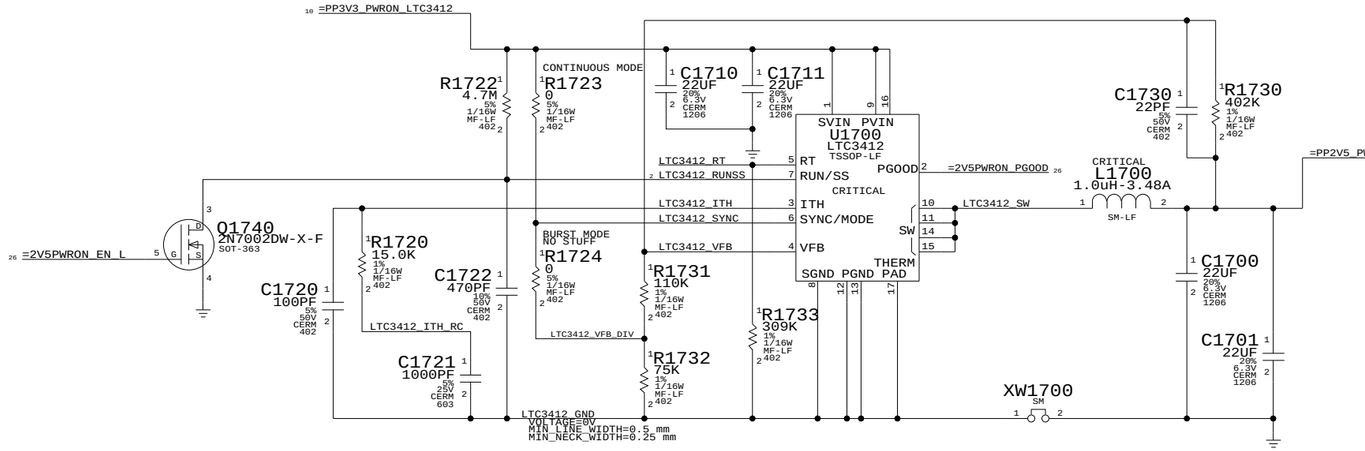
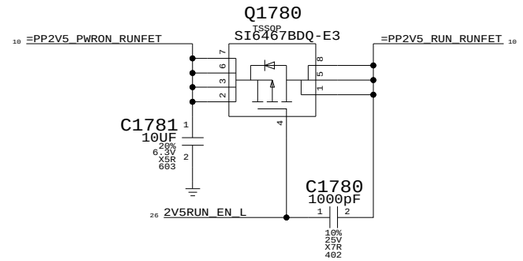
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	16	115

2.5V SWITCHER





2.5V Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	17	115

Page Notes

Power aliases required by this page:
- =PPBUS_FW (system supply for bus power)
- =PPBU_RUN_FW (backup PHY power)
- =PP3V3_RUN_FWPORTPWRSW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- VESTA1V2_BURST / VESTA1V2_PULSE
  Controls operating mode of Vesta 1.2V regulator. If both options are off the regulator will be in continuous mode.

3.3V Regulator

=PPFW_P3V3VESTA, =PPBU_RUN_FW → D1975 SC-59 → SMD20E40C-X-F → PPVIN_VESTA3V3 (VOLTAGE=33V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL U1970 LM2594 SM-LF: VIN, FB, VOUT, GND, ON/OFF

CRITICAL L1970 100uH-0.8A PLC

VESTA3V3_SW (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

D1970 SMD MMBRM140XXG

C1970 10uF N20P20% 50V CERM 2320

CRITICAL C1971 100UF 20% 6.3V POLY B2

=PP3V3_VESTA_REG, Vout = 3.3V @ 500mA

2.5V LDO

=PP3V3_VESTA_2V5REG → CRITICAL U1980 MM1572FN SOT-25A (VIN, VOUT, CONT, NOISE, GND)

C1980 1uF 10% 6.3V CERM 402

VESTA2V5_NOISE (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)

C1981 0.01uF 20% 16V CERM 402

C1982 10UF 20% 6.3V X5R 603

=PP2V5_VESTA_LDO, Vout = 2.5V @ 150 mA

Port Power Switch

=PPBUS_FWPWRSW → F1965 1.5A-24V MINISMDC → PPBUS_FWPWRSW_F (VOLTAGE=25V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL Q1965 NDS9407 SOI-LF

PPBUS_FW_FET_D (VOLTAGE=25V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

CRITICAL D1965 SMB B340XF → =PPBUS_FW_FET

R1965 470K 5% 1/16W MF-LF 402

C1965 0.01uF 20% 16V CERM 402

FWPWR_EN_L_DIV (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)

R1966 330K 5% 1/16W MF-LF 402

=PP3V3_RUN_FWPORTPWRSW → R1960 100K 5% 1/16W MF-LF 402

FWPWR_EN_L (MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm)

Q1960 2N7002 SOT23-LF

FWPWR_RUN, FWPWR_EN

DP1960 BAS16TW-X-F SOT-363

=FWPWR_PWRON

SYS_ACIN → R1961 10K 5% 1/16W MF-LF 402 → FWPWR_ACIN

R1963 470K 5% 1/16W MF-LF 402

If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

1.2V Regulator

=PP3V3_VESTA_1V2REG

R1990 10 5% 1/16W MF-LF 402 → PPVOUT_VESTA1V2 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

C1990 10UF 20% 6.3V XSR 603

Burst Mode VESTA1V2_BURST: R1992 10K 5% 1/16W MF-LF 402; R1991 1M 5% 1/16W MF-LF 402

Pulse Mode VESTA1V2_PULSE: R1993 10K 5% 1/16W MF-LF 402

Continuous Mode: R1994 1M 5% 1/16W MF-LF 402; R1995 324K 1% 1/16W MF-LF 402

C1991 1uF 10% 6.3V CERM 402

SVIN PVIN U1990 LTC3411 MSOP-LF: SHDN/RT, SYNC/MODE, PGOOD, PGND, SGND, SW, VFB, ITH

VESTA1V2_RT, VESTA1V2_MODE

CRITICAL L1990 2.2uH SM1-LF (MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

VESTA1V2_SW, VESTA1V2_VFB, VESTA1V2_ITH

R1996 4.99K 1% 1/16W MF-LF 402

C1992 22pF 5% 50V CERM 402

<R2> R1997 4.99K 1% 1/16W MF-LF 402

C1993 100pF 5% 50V CERM 402

<R1> R1998 10K 1% 1/16W MF-LF 402

VESTA1V2_ITH_RC

C1994 0.0033uF 10% 50V CERM 402

XW1990 SM

VESTA1V2_SGND (VOLTAGE=0V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)

=PP1V2_VESTA_REG

Vout = 0.8V * (1 + (R2 / R1))

Vout = 1.199V @ 1.2 A

C1995 22uF 20% 6.3V X5R 805

L1900 FERR-EMI-600-OHM SM

=PP1V2_VESTA → PP1V2_VESTA_AVDDL (VOLTAGE=1.2V, MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm)

C1908 10UF 20% 6.3V X5R 603

C1900 0.1uF 20% 10V CERM 402 — L6/M6

C1901 0.1uF 20% 10V CERM 402 — L9/M9

C1902 0.1uF 20% 10V CERM 402 — N5/N6

C1903 0.1uF 20% 10V CERM 402 — N9/N10

C1910 0.1uF 20% 10V CERM 402

C1911 0.1uF 20% 10V CERM 402

C1912 0.1uF 20% 10V CERM 402

C1913 0.1uF 20% 10V CERM 402

DVDD, AVDDL, AVDD, PVDD

C1920 0.1uF 20% 10V CERM 402

C1921 0.1uF 20% 10V CERM 402

C1922 0.1uF 20% 10V CERM 402

C1923 0.1uF 20% 10V CERM 402

C1924 0.1uF 20% 10V CERM 402

C1925 0.1uF 20% 10V CERM 402

=PP2V5_VESTA

C1930 0.1uF 20% 10V CERM 402

C1931 0.1uF 20% 10V CERM 402

=PP3V3_VESTA

C1940 0.1uF 20% 10V CERM 402

C1941 0.1uF 20% 10V CERM 402

C1942 0.1uF 20% 10V CERM 402

C1943 0.1uF 20% 10V CERM 402

OVDD

Reset circuit per Vesta design guide

=PP3V3_VESTA → R1950 20K 5% 1/16W MF-LF 402; R1951 10K 5% 1/16W MF-LF 402

VESTA_RESET_L_RC → C1950 1uF 10% 6.3V CERM 402

VESTA_RESET → Q01950 2N7002DW-X-F SOT-363

VESTA_RESET_L

Schmitt trigger

VESTA MISC

OMIT

U8500 BCM5462 FBGA-200 1 OF 3

(Int PU) RESET*

=JTAG_VESTA_TDI → TDI

=JTAG_VESTA_TDO → TDO

=JTAG_VESTA_TCK → TCK

=JTAG_VESTA_TMS → TMS

=JTAG_VESTA_TRST_L → TRST*

R1952 10K 5% 1/16W MF-LF 402 → R1952 to enable wirespeed feature

TP_VESTA_DNC_B9 → DNC

TP_VESTA_DNC_C9 → DNC

TP_VESTA_DNC_E9 → DNC

NC, NC

2.5V_EN → TP_VESTA_2_5V_EN

REGSUP1, REGSEN1, REGCTL1 → TP_VESTA_REGSUP1, TP_VESTA_REGSEN1, NC? TP_VESTA_REGCTL1

REGSUP2, REGSEN2, REGCTL2 → TP_VESTA_REGSUP2, TP_VESTA_REGSEN2, NC? TP_VESTA_REGCTL2

AGND, GND

Vesta Power & Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 19 OF 115	

Page Notes

Power aliases required by this page:
- =PPVCORE_PWRON_I2
- =PP1V5_PWRON_I2_PLL
- =PP3V3_PWRON_I2_IO1
- =PP3V3_PWRON_I2_IO2
- =PP3V3_PWRON_I2_AGPPCI
- =PP3V3_PWRON_I2_MAXBUS

NOTE: The four 3.3V rails are meant to be aliased together. They are called out separately for test purposes.

NOTE: When these four rails are not aliased together, make sure there is at least one 10uF cap per rail.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

VCore Bypassing

(25 Balls on I2)

4 X 10uF (0603)
25 X 1uF (0402)

=PPVCORE_PWRON_I2

C2146 10UF 20% 6.3V X5R 603
C2147 10UF 20% 6.3V X5R 603
C2148 10UF 20% 6.3V X5R 603
C2149 10UF 20% 6.3V X5R 603
C2120 C2121 C2122 C2123 C2124 C2125 C2126 C2127 C2128 C2129 C2130 C2131 C2132
C2133 C2134 C2135 C2136 C2137 C2138 C2139 C2140 C2141 C2142 C2143 C2144
1uF 10% 6.3V CERM 402

VDD15_0 AA22
VDD15_1 AB21
VDD15_2 AC16
VDD15_3 AC19
VDD15_4 AN7
VDD15_5 P16
VDD15_6 P20
VDD15_7 R16
VDD15_8 R18
VDD15_9 R21
VDD15_10 T15
VDD15_11 T19
VDD15_12 T22
VDD15_13 U15
VDD15_14 U18
VDD15_15 U20
VDD15_16 U22
VDD15_17 V17
VDD15_18 V19
VDD15_19 V21
VDD15_20 W18
VDD15_21 W20
VDD15_22 W22
VDD15_23 Y15
VDD15_24 Y17

3.3V I/O DECOUPLING

(48 Balls on I2)

1 X 10uF (0603)
48 X 1uF (0402)

=PP3V3_PWRON_I2_IO1
=PP3V3_PWRON_I2_IO2
=PP3V3_PWRON_I2_MAXBUS
=PP3V3_PWRON_I2_AGPPCI

C2150 C2151 C2152 C2153 C2154 C2155
C2156 C2157 C2158 C2159 C2160 C2161
C2162 C2163
C2164 C2165 C2166 C2167 C2168 C2169
C2170 C2171 C2172 C2173 C2174 C2175
C2176 C2177 C2178 C2179
C2180 C2181 C2182 C2183 C2184 C2185
C2186 C2187 C2188 C2189 C2190 C2191
C2192 C2193 C2194 C2195 C2196 C2197
1uF 10% 6.3V CERM 402

C2199 10UF 20% 6.3V X5R 603

OMIT
U2100
I2
BGA
3.3V I/O POWER
(2 of 14)

VDD33_AGP
VDD33_0 AH17
VDD33_1 E3
VDD33_2 F5
VDD33_3 H3
VDD33_4 H6
VDD33_5 J8
VDD33_6 L10
VDD33_7 L3
VDD33_8 L6
VDD33_9 N13
VDD33_10 P12
VDD33_11 P3
VDD33_12 P6
VDD33_13 R14
VDD33_14 T13

For USB, Firewire, I2S and some GPIOs
VDD33_IO_1 (14)

VDD33_15 AB13
VDD33_16 AC15
VDD33_17 AC3
VDD33_18 AC6
VDD33_19 AF11
VDD33_20 AF3
VDD33_21 AF6
VDD33_22 AF9
VDD33_23 AJ3
VDD33_24 AJ6
VDD33_25 AM3
VDD33_26 Y13

For GPIOs, Pwr Mgt
VDD33_IO_2 (12)

VDD33_MAXBUS
VDD33_27 M16
VDD33_28 M18
VDD33_29 M22

VDD33_30 AC21
VDD33_31 AD20
VDD33_32 AD22
VDD33_33 AH20
VDD33_34 AH23
VDD33_35 AH24
VDD33_36 AH26
VDD33_37 AH27
VDD33_38 AL23
VDD33_39 AL24
VDD33_40 AL26
VDD33_41 AL27
VDD33_42 AL29
VDD33_43 AL30
VDD33_44 AP23
VDD33_45 AP26
VDD33_46 AP29
VDD33_47 AP32

VDD33_PCI (10)

=PP1V5_PWRON_I2_PLL

R2101 R2102 R2103 R2104 R2105 R2106 R2107 R2109
4.7 5% 1/16W MF-LF 402

C2101 C2102 C2103 C2104 C2105 C2106 C2107 C2109
1uF 10% 6.3V CERM 402

PP1V5_PWRON_I2_PLL1AVDD
PP1V5_PWRON_I2_PLL2AVDD
PP1V5_PWRON_I2_PLL3AVDD
PP1V5_PWRON_I2_PLL4AVDD
PP1V5_PWRON_I2_PLL5AVDD
PP1V5_PWRON_I2_PLL6AVDD
PP1V5_PWRON_I2_PLL7AVDD
PP1V5_PWRON_I2_PLL9AVDD
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.2 mm

OMIT
U2100
I2
BGA
PLL POWER
(3 of 14)

AA20 PLL1_AVDD
PLL1
32/48 MHZ
Y20 PLL1_VSSA

AA19 PLL2_AVDD
PLL2
45.16 MHZ
Y19 PLL2_VSSA

AK19 PLL3_AVDD
PLL3
49.15 MHZ
AJ19 PLL3_VSSA

H9 PLL4_AVDD
PLL4
SYSCLK
PCI(SS)
AGP(SS)
H10 PLL4_VSSA

AD9 PLL5_AVDD
PLL5
INT REF
PCI
AGP
ATA
AE9 PLL5_VSSA

M24 PLL6_AVDD
PLL6
SYS TRACK
N24 PLL6_VSSA

AH22 PLL7_AVDD
PLL7
PCI TRACK
AH21 PLL7_VSSA

AK10 PLL9_AVDD
PLL9
AGP TRACK
AL10 PLL9_VSSA

OMIT
U2100
I2
BGA
CORE POWER & GND
(1 of 14)

VSS_0 AA13
VSS_1 AA15
VSS_2 AA17
VSS_3 AA21
VSS_4 AA25
VSS_5 AA29
VSS_6 AB12
VSS_7 AB15
VSS_8 AB16
VSS_9 AB22
VSS_10 AB24
VSS_11 AC2
VSS_12 AC20
VSS_13 AC25
VSS_14 AC26
VSS_15 AC29
VSS_16 AC32
VSS_17 AC35
VSS_18 AC5
VSS_19 AD16
VSS_20 AD21
VSS_21 AD29
VSS_22 AE14
VSS_23 AE15
VSS_24 AE17
VSS_25 AE19
VSS_26 AE20
VSS_27 AE25
VSS_28 AF10
VSS_29 AF18
VSS_30 AF2
VSS_31 AF27
VSS_32 AF29
VSS_33 AF32
VSS_34 AF35
VSS_35 AF5
VSS_36 AF8
VSS_37 AG11
VSS_38 AG14
VSS_39 AG29
VSS_40 AH14
VSS_41 AJ11
VSS_42 AJ14
VSS_43 AJ17
VSS_44 AJ2
VSS_45 AJ20
VSS_46 AJ23
VSS_47 AJ24
VSS_48 AJ26
VSS_49 AJ27

VSS_50 AJ29
VSS_51 AJ32
VSS_52 AJ35
VSS_53 AJ5
VSS_54 AJ8
VSS_55 AM11
VSS_56 AM14
VSS_57 AM17
VSS_58 AM2
VSS_59 AM20
VSS_60 AM23
VSS_61 AM26
VSS_62 AM29
VSS_63 AM32
VSS_64 AM35
VSS_65 AM5
VSS_66 AM7
VSS_67 AM8
VSS_68 AR11
VSS_69 AR14
VSS_70 AR17
VSS_71 AR2
VSS_72 AR20
VSS_73 AR23
VSS_74 AR26
VSS_75 AR29
VSS_76 AR32
VSS_77 AR35
VSS_78 AR5
VSS_79 AR8
VSS_80 B11
VSS_81 B14
VSS_82 B17
VSS_83 B2
VSS_84 B20
VSS_85 B23
VSS_86 B26
VSS_87 B29
VSS_88 B32
VSS_89 B35
VSS_90 B5
VSS_91 B8
VSS_92 E11
VSS_93 E14
VSS_94 E17
VSS_95 E2
VSS_96 E20
VSS_97 E23
VSS_98 E26
VSS_99 E29

E32 VSS_100
E35 VSS_101
E5 VSS_102
E8 VSS_103
H11 VSS_104
H12 VSS_105
H14 VSS_106
H15 VSS_107
H17 VSS_108
H18 VSS_109
H2 VSS_110
H20 VSS_111
H23 VSS_112
H24 VSS_113
H26 VSS_114
H27 VSS_115
H29 VSS_116
H32 VSS_117
H35 VSS_118
H5 VSS_119
H8 VSS_120
K10 VSS_121
K11 VSS_122
K14 VSS_123
K17 VSS_124
K20 VSS_125
K23 VSS_126
K25 VSS_127
K26 VSS_128
K29 VSS_129
L2 VSS_130
L20 VSS_131
L27 VSS_132
L29 VSS_133
L32 VSS_134
L35 VSS_135
L5 VSS_136
L8 VSS_137
M13 VSS_138
M15 VSS_139
M17 VSS_140
M19 VSS_141
M21 VSS_142
M23 VSS_143
M26 VSS_144
N14 VSS_145
N16 VSS_146
N18 VSS_147
N23 VSS_148
N25 VSS_149

VSS_150 P17
VSS_151 P2
VSS_152 P21
VSS_153 P24
VSS_154 P27
VSS_155 P29
VSS_156 P32
VSS_157 P35
VSS_158 P5
VSS_159 P8
VSS_160 R13
VSS_161 R15
VSS_162 R17
VSS_163 R19
VSS_164 R20
VSS_165 R22
VSS_166 R25
VSS_167 R29
VSS_168 T16
VSS_169 T18
VSS_170 T20
VSS_171 U13
VSS_172 U16
VSS_173 U2
VSS_174 U21
VSS_175 U25
VSS_176 U28
VSS_177 U32
VSS_178 U35
VSS_179 U5
VSS_180 U8
VSS_181 V12
VSS_182 V16
VSS_183 V20
VSS_184 V28
VSS_185 W15
VSS_186 W19
VSS_187 W21
VSS_188 W25
VSS_189 W26
VSS_190 Y11
VSS_191 Y16
VSS_192 Y18
VSS_193 Y2
VSS_194 Y22
VSS_195 Y29
VSS_196 Y32
VSS_197 Y35
VSS_198 Y5
VSS_199 Y8

I2 Power

SYNC_MASTER=N/A
SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 21 OF 115

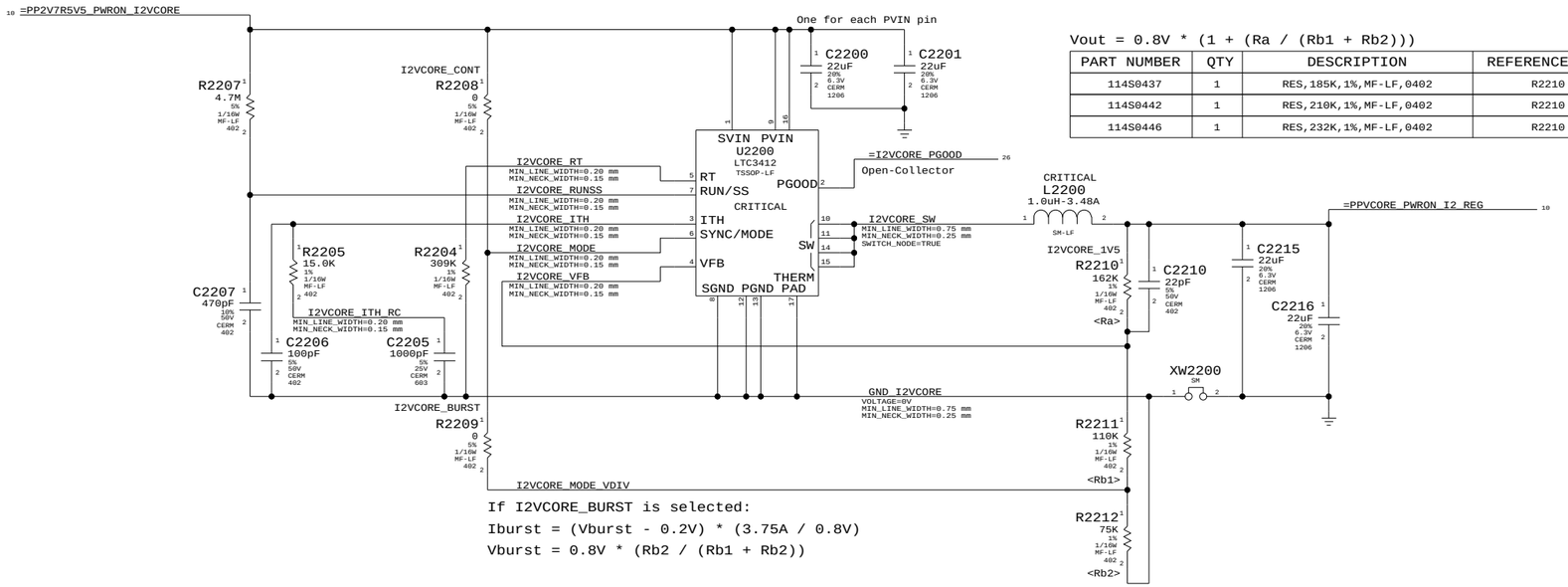
Page Notes

Power aliases required by this page:
- =PP2V7R5V5_PWRON_I2VCORE
- =PPVCORE_PWRON_I2_REG
- =PPVIN_PWRON_I2PLLVDD
- =PP1V5_PWRON_I2PLLVDD_LDO

Signal aliases required by this page:
- =I2VCORE_PGOOD

BOM options provided by this page:
- I2VCORE_CONT / I2VCORE_BURST
  Selects between forced continuous and burst mode for LTC3412 regulator.
- I2VCORE_xVx
  Selects appropriate resistor for the indicated LTC3412 output voltage.

I2 VCore Regulator

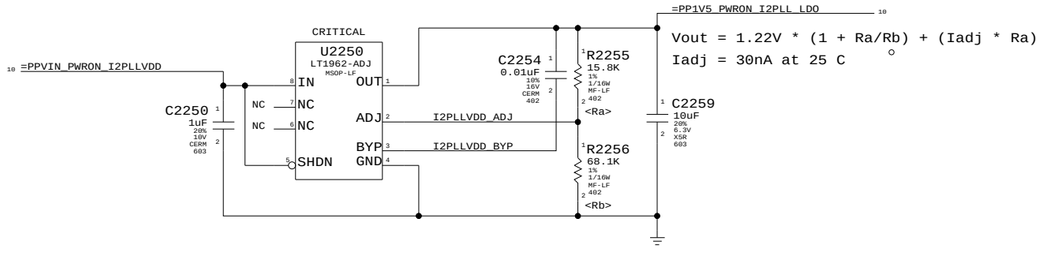


Vout = 0.8V * (1 + (Ra / (Rb1 + Rb2)))

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
114S0437	1	RES,185K,1%,MF-LF,0402	R2210		I2VCORE_1V6
114S0442	1	RES,210K,1%,MF-LF,0402	R2210		I2VCORE_1V7
114S0446	1	RES,232K,1%,MF-LF,0402	R2210		I2VCORE_1V8

If I2VCORE_BURST is selected:
Iburst = (Vburst - 0.2V) * (3.75A / 0.8V)
Vburst = 0.8V * (Rb2 / (Rb1 + Rb2))

I2 PLL LDO



Vout = 1.22V * (1 + Ra/Rb) + (Iadj * Ra)
Iadj = 30nA at 25 C

I2 Power Supplies

SYNC_MASTER=N/A SYNC_DATE=N/A

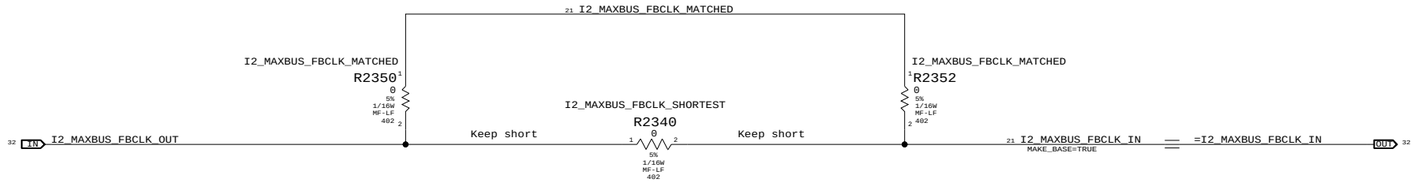
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

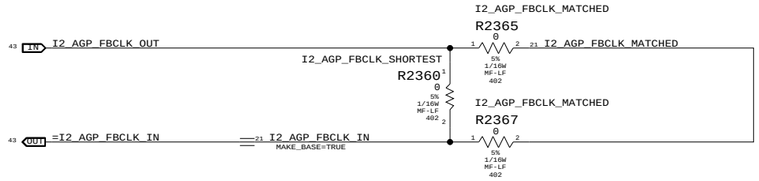
SCALE	SHT	OF
NONE	22	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	I2_FBCLK	I2_FBCLK	I2_MAXBUS_FBCLK_IN
	I2_FBCLK	I2_FBCLK	I2_MAXBUS_FBCLK_MATCHED
	I2_FBCLK	I2_FBCLK	I2_AGP_FBCLK_IN
	I2_FBCLK	I2_FBCLK	I2_AGP_FBCLK_MATCHED
100	I2_FBCLK	I2_FBCLK	I2_PCI_FBCLK_IN
100	I2_FBCLK	I2_FBCLK	I2_PCI_FBCLK_MATCHED
100	CLOCK	CLOCK	=CLK33M_TBEN_SYNC
120	CLOCK	CLOCK	=SYSCLK_TBEN_SYNC

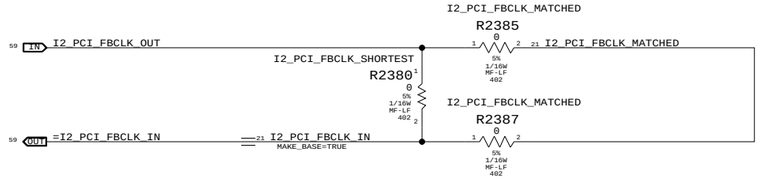
MaxBus Feedback Clock Network



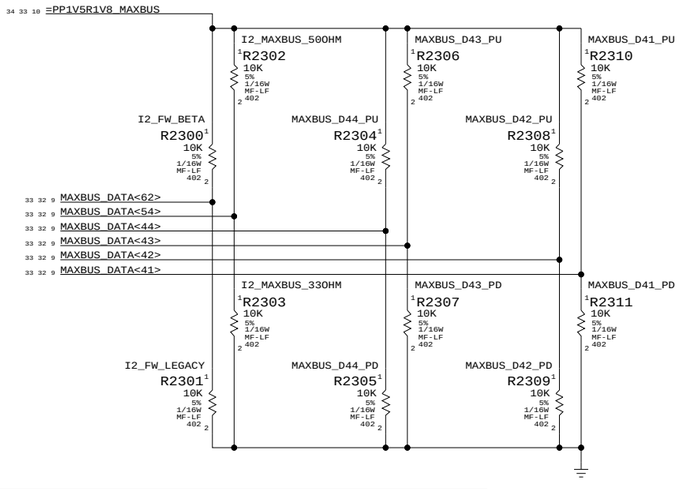
AGP Feedback Clock Ladder



PCI Feedback Clock Ladder

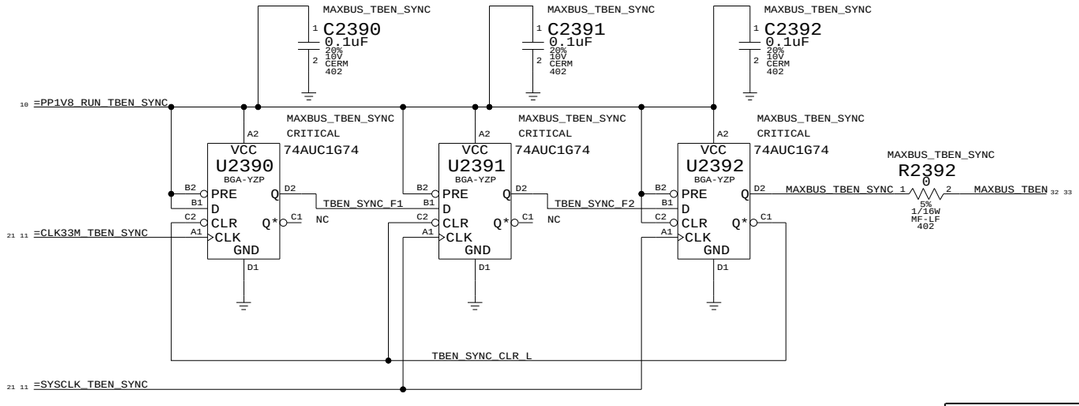


I2 Configuration Straps



Signal	Tied	Description
MAXBUS_DATA<62>	HIGH	1394b Support (Beta Mode)
	LOW	1394a Support (Legacy Mode)
MAXBUS_DATA<54>	HIGH	50-Ohm MaxBus Drivers
	LOW	33-Ohm MaxBus Drivers
MAXBUS_DATA<44:41>	See Table Below	

BOM GROUP	Tied	Description	BOM OPTIONS
I2_MAXBUS_133MHZ	0000	133.12MHz CPU / 266.24MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_150MHZ	1000	149.76MHz CPU / 299.52MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_166MHZ	0100	166.40MHz CPU / 332.80MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_172MHZ	1100	171.95MHz CPU / 342.90MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PD,MAXBUS_D41_PD
I2_MAXBUS_177MHZ	0010	177.49MHz CPU / 354.98MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_183MHZ	1010	183.04MHz CPU / 366.08MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PD,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_189MHZ	0110	188.59MHz CPU / 377.18MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_194MHZ	1110	194.13MHz CPU / 388.26MHz DDR	MAXBUS_D44_PU,MAXBUS_D43_PU,MAXBUS_D42_PU,MAXBUS_D41_PD
I2_MAXBUS_200MHZ	0001	199.68MHz CPU / 399.36MHz DDR	MAXBUS_D44_PD,MAXBUS_D43_PD,MAXBUS_D42_PD,MAXBUS_D41_PD



I2 Supplemental

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 23 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR
I2S0_DTI	I2S	I2S	
I2S0_DTO	I2S	I2S	
I2S0_MCLK	I2S	I2S	
I2S0_BITCLK	I2S	I2S	
I2S0_SYNC	I2S	I2S	
I2S1_DTI	I2S	I2S	
I2S1_DTO	I2S	I2S	
I2S1_MCLK	I2S	I2S	
I2S1_BITCLK	I2S	I2S	
I2S1_SYNC	I2S	I2S	
I2_XTAL	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	
(I2_XTAL)	XTAL	XTAL	

I2S0_DEV_TO_SB_DTI (7 22 74)
I2S0_SB_TO_DEV_DTO_R (6 22)
I2S0_MCLK_R (6 22)
I2S0_BITCLK_R (6 22)
I2S0_SYNC_R (6 22)
I2S1_DEV_TO_SB_DTI (22 30)
I2S1_SB_TO_DEV_DTO_R (6 22)
I2S1_MCLK_R (6 22)
I2S1_BITCLK_R (6 22)
I2S1_SYNC_R (6 22)
I2_CLK18M_XOUT_R (22)
I2_CLK18M_XOUT (22)
I2_CLK18M_XIN (22)

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0

GPIO Pull-ups / Pull-downs

=PP3V3_PWRON_I2_MISC (10 22)
=PP3V3_I2_PCISLOTEGPIOS (10)

EXT_00 Internal pull-up to 3.3V PWRON
EXT_01 Internal pull-up to 3.3V PWRON
EXT_02 10K Pull-up to 3.3V on I2 AGP page.
EXT_03 Pull-up/down to be provided by audio page.
EXT_04 Pull-up/down to be provided by audio page.
EXT_05 10K Pull-up to Enet OVdd on I2 Enet page.
EXT_06 10K Pull-up to 3.3V on I2 PCI page.
EXT_07 10K Pull-up to 3.3V on I2 PCI page.
I2_REV1_NOT
EXT_08 R2455 10K 5% 1/16W MF-LF 402 (I2_EXT_08) PCI_SLOTE_INT_L (11 22)
(*) - Rev 1.0: Internal pull-up to 3.3V PWRON
EXT_09 Internal pull-up to 3.3V PWRON
EXT_10 Pull-up/down to be provided by audio page.
EXT_11 R2452 10K 5% 1/16W MF-LF 402 (I2_REV1) MMM_FFIRQ_L (22 25)
EXT_12 Internal pull-up to 3.3V PWRON (*) - Rev 1.0: Missing internal pull-up to 3.3V PWRON
EXT_13 RP2450 10K 5% 1/16W SM-LF (I2_EXT_13) PCI_SLOTE_GNT_L (11 22)
EXT_14 RP2450 10K 5% 1/16W SM-LF (I2_EXT_14) PCI_SLOTE_REQ_L (11 22)
EXT_15 Pull-up/down to be provided by audio page.
EXT_16 Pull-up/down to be provided by audio page. (*) - See above
GPIO_EXT_00 Pull-up/down to be provided by audio page.
GPIO_EXT_01 RP2450 10K 5% 1/16W SM-LF =SPI_I2_REQ (11 22)
GPIO_EXT_02 R2451 10K 5% 1/16W MF-LF 402 (I2_REV1) I2_GPIO_EXT_02 (11 22)
(*) - Rev 1.0: Missing internal pull-up to 3.3V PWRON
GPIO_EXT_03 Internal pull-up to 3.3V PWRON
GPIO_04 RP2450 10K 5% 1/16W SM-LF FW_POWERDOWN (22)
GPIO_05 Pull-up/down to be provided by audio page.
GPIO_06 Pull-up/down to be provided by audio page.
GPIO_09 Pull-up/down to be provided by audio page.
GPIO_11 Internal pull-up to 3.3V PWRON
GPIO_12 Pull-up/down to be provided by audio page. (*) - See above
GPIO_15 Pull-up/down to be provided by audio page.
GPIO_16 Pull-up/down to be provided by design.

Signal Direction / Pin Direction

U2100 I2 BGA — MISCELLANEOUS (4 OF 14) — GPIO INTERFACE (OMIT)

	Signal Direction	Pin Direction			Pin	Address	MPIC Int	Int PU?	Alt Func
MODEM_RING2SYS_L (30 25)			AH1	EXT_00_H (Int PU)	EXT_00	0x0_0058	46 (0x2E)	Yes	PCI_REQ_2_L (When PCI1_Slot2En = 10)
PMU_INT_L (25)			AK4	EXT_01_H (Int PU)	EXT_01	0x0_0059	47 (0x2F)	Yes	
AGP_INT_L (44 43)			AT19	EXT_02_H	EXT_02	0x0_005A	48 (0x30)	No	
AUDIO_LI_OPTICAL_PLUG_L (74 7)			AH2	EXT_03_H	EXT_03	0x0_005B	49 (0x31)	No	
AUDIO_LI_DET_L (74 7)			J2	EXT_04_H	EXT_04	0x0_005C	50 (0x32)	No	
				EXT_05_H - See Ethernet Sym	EXT_05	0x0_005D	51 (0x33)	No	
PCI_SLOTA_INT_L (59 11)			AR33	EXT_06_H	EXT_06	0x0_005E	52 (0x34)	No	
PCI_SLOTD_INT_L (59 11)			AN33	EXT_07_H	EXT_07	0x0_005F	53 (0x35)	No	
I2_EXT_08			AG4	EXT_08_H (Int PU - rev 1)	EXT_08	0x0_0060	54 (0x36)	Yes	
PMU_SB_NMI_L (25)			AK1	EXT_09_H (Int PU)	EXT_09	0x0_0061	55 (0x37)	Yes	
AUDIO_LO_OPTICAL_PLUG_L (74 7)			AG1	EXT_10_H	EXT_10	0x0_0062	56 (0x38)	No	
MMM_FFIRQ_L (25 22)			AG3	EXT_11_H (Int PU)	EXT_11	0x0_0063	57 (0x39)	Yes	
MMM_SIRQ_L (25)			AG2	EXT_12_H (Int PU)	EXT_12	0x0_0064	58 (0x3A)	Yes	
I2_EXT_13			AF1	EXT_13_H	EXT_13	0x0_0065	59 (0x3B)	No	PCI_GNT_2_L (When PCI1_Slot2En = 11)
I2_EXT_14			AE4	EXT_14_H	EXT_14	0x0_0066	60 (0x3C)	No	PCI_REQ_2_L (When PCI1_Slot2En = 11)
AUDIO_LO_DET_L (74 7)			H1	EXT_15_H	EXT_15	0x0_0067	61 (0x3D)	No	
AUDIO_GPIO_11 (74 7)			G4	EXT_16_H (Int PU - rev 1)	EXT_16	0x0_0068	62 (0x3F)	Yes	
AUDIO_CODEC_RESET_L (74 7)			AK2	GPIO_EXT_00_H	GPIO_00	0x0_006A	14 (0x0E)	No	
=SPI_I2_REQ (22 11)			AJ1	GPIO_EXT_01_H	GPIO_01	0x0_006B	15 (0x0F)	No	SPIREQ (When SPISReqEn = 1)
I2_GPIO_EXT_02 (22 11)			AH4	GPIO_EXT_02_H (Int PU)	GPIO_02	0x0_006C	16 (0x10)	Yes	PCI_GNT_2_L (When PCI1_Slot2En = 10)
MODEM_RESET_L (30)			AH3	GPIO_EXT_03_H (Int PU)	GPIO_03	0x0_006D	17 (0x11)	Yes	
FW_POWERDOWN (22)			M1	GPIO_04_H	GPIO_04	0x0_006E	N/A	No	
AUDIO_LO_MUTE_L (74 7)			G3	GPIO_05_H	GPIO_05	0x0_006F	N/A	No	
AUDIO_SPKR_MUTE_L (74 7)			G1	GPIO_06_H	GPIO_06	0x0_0070	N/A	No	
AUDIO_I2S_DTIB_SEL (74 7)			AG8	GPIO_09_H	GPIO_09	0x0_0073	N/A	No	
I2_GPIO_11 (11)			G2	GPIO_11_H (Int PU)	GPIO_11	0x0_0075	N/A	Yes	
AUDIO_SPDIFRX_RESET_L (74 7)			AG7	GPIO_12_H (Int PU - rev 1)	GPIO_12	0x0_0076	N/A	Yes	
AUDIO_EXT_MCLK_SEL (74 7)			AG6	GPIO_15_H	GPIO_15	0x0_0079	N/A	No	
				GPIO_16_H - See Ethernet Sym	GPIO_16	0x0_007A	N/A	No	

Alternate GPIO Functions
Use MAKE_BASE to force net name

PCI_SLOTE_INT_L (22 11)
PCI_SLOTE_GNT_L (22 11)
PCI_SLOTE_REQ_L (22 11)

I2C

IIC_CLK_0_H	J1	=I2C_I2_NB_SCL (8)	
IIC_D_0_H	J3	=I2C_I2_NB_SDA (8)	
IIC_CLK_2_H	F4	=I2C_I2_SB_SCL (8)	
IIC_D_2_H	F1	=I2C_I2_SB_SDA (8)	

I2S 0 (Master) (Slave)

I2S0_DEV_TO_SB_DTI (74 22 7)	E1 AUD_DTI_A_H	AUD_DTO_A_H	C1 I2S0_SB_TO_DEV_DTO_R (6 22)
		AUD_CLKOUT_A_H	F2 I2S0_MCLK_R (6 22)
		AUD_BITCLK_A_H	F3 I2S0_BITCLK_R (6 22)
		AUD_SYNC_A_H	D2 I2S0_SYNC_R (6 22)

I2S 1 (Master) (Slave)

I2S1_DEV_TO_SB_DTI (30 22)	J5 MOD_DTI_B_H	MOD_DTO_B_H	G5 I2S1_SB_TO_DEV_DTO_R (6 22)
		MOD_CLKOUT_B_H	J6 I2S1_MCLK_R (6 22)
		MOD_BITCLK_B_H	J7 I2S1_BITCLK_R (6 22)
		MOD_SYNC_B_H	G6 I2S1_SYNC_R (6 22)

SCCA

=PP3V3_PWRON_I2_MISC (22 10) → R2490 10K 5% 1/16W MF-LF 402			
SCCA_RXD (24 7)	AG5 SCC_RXDA_H	SCC_TXDA_L	AE5 SCCA_TXD_L (7 24)

SCCB/VIA

VIA_PMU_TO_SB (25)	AL3 SCC_RXDB_H	SCC_TXDB_L	AL2 VIA_SB_TO_PMU (25)
VIA_ACK_L (25)	AM1 SCC_GPIOB_L	SCC_RTSB_L	AL4 VIA_REQ_L (25)
VIA_CLK (25)	AL1 SCC_TRXCB_H		

TEST/JTAG

I2_TST_TEI	AL6 TST_TEI_H		
I2_TST_PLLEN	AL5 TST_PLLEN_H		
=SPI_I2_MOSI			
=JTAG_I2_TDI (9)	AN6 JTG_TDI_H	JTG_TDO_H	AN4 =SPI_I2_MISO / =JTAG_I2_TDO (9)
=JTAG_I2_TMS (9)	AN2 JTG_TMS_H		
=JTAG_I2_TCK (9)	AN3 JTG_TCK_H		
=JTAG_I2_TRST_L (9)	AP1 JTG_TRSTN_L		
=SPI_I2_CLK			

R2400 10K 5% 1/16W MF-LF 402 — R2401 10K 5% 1/16W MF-LF 402

POWER MGMT/CLOCK

SYS_WARM_RESET_L (62 25)	AK3 REF_PURESET_L	PWR_PCI_PME_L	AK7 SYS_PME_L (25 62)
=I2_STOPXTAL_L (11)	AH7 PWR_STPXTL_L		
=I2_STOPCPU_L (11)	AH6 PWR_STPCPU_L	PWR_INTRWD_H	AL7 SYS_WATCHDOG (25)
NB_SUSPENDREQ_L (25)	AH5 PWR_SPDREQ_L	PWR_SPDACK_L	AK5 NB_SUSPENDACK_L (25)
Put crystal circuit close to I2			
I2_CLK18M_XOUT_R (22)	AC12 REF_CLK_OUT	PWR_PENDINT_H	AK6 TP_I2_PENDINT
I2_CLK18M_XIN (22)	AC13 REF_CLK_IN		

NO STUFF
R2410 10M 5% 1/16W MF-LF 402
R2411 0 5% 1/16W MF-LF 402
CRITICAL
Y2410 18.432M 8X4.5MM-SM1
I2_CLK18M_XOUT (22)
C2411 22pF 5% 50V CERM 402
C2410 22pF 5% 50V CERM 402
Crystal load capacitance is 16pF

I2 Miscellaneous

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.
SIZE D | DRAWING NUMBER 051-6929 | REV. 03
SCALE NONE | SHT 24 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
T72	CLOCK	CLOCK	
T73 PCI_ZDBOUT0	CLOCK	CLOCK	
T74 PCI_ZDBOUT1	CLOCK	CLOCK	
T75 PCI_ZDBOUT2	CLOCK	CLOCK	
T76 PCI_ZDBOUT3	CLOCK	CLOCK	

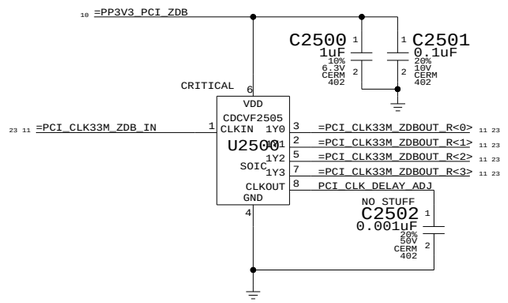
=PCI_CLK33M_ZDB_IN 11 23
=PCI_CLK33M_ZDBOUT_R<0> 11 23
=PCI_CLK33M_ZDBOUT_R<1> 11 23
=PCI_CLK33M_ZDBOUT_R<2> 11 23
=PCI_CLK33M_ZDBOUT_R<3> 11 23

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_I2_GPIO
- =PP3V3_I2_PCISLOTEGPIOS (PWRON or PCI)
  Should be same as =PP3V3_PCI if slot E
  is used, or else =PP3V3_PWRON_I2_GPIO.

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- I2_REV1_NOT
  Use for I2 revisions > 1.0



PCI Clock Buffer

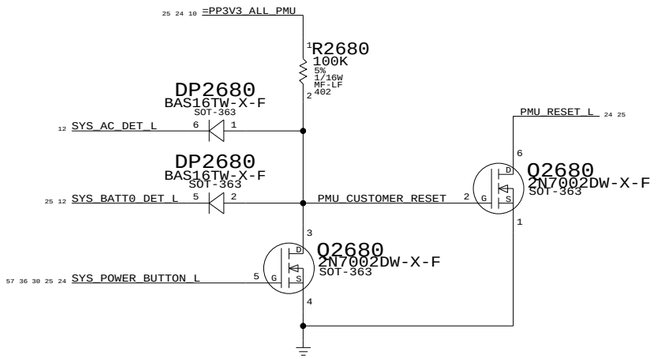
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

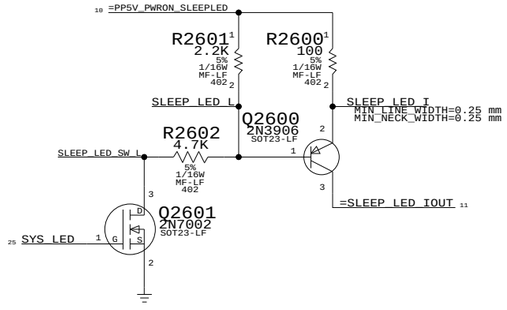
SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	25	115

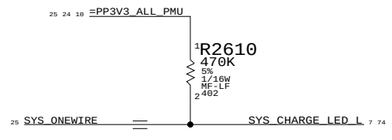
PMU RESET CIRCUIT



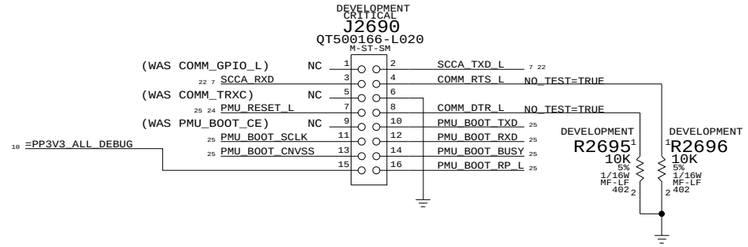
SLEEP LED



CHARGE LED

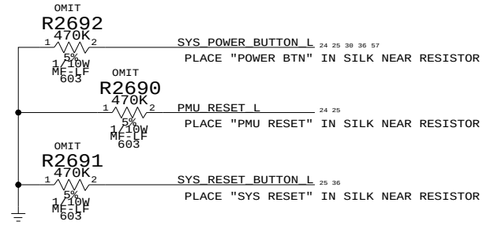


SERIAL DEBUG INTERFACE



DEBUGGING AIDS

PLACE ON TOP SIDE NEAR FRONT EDGE OF BOARD



LEDs/Reset/Debug

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 26 OF 115	

Power Management Unit

Page Notes

Power aliases required by this page:
- =PP3V3_ALL_PMU
- =PP3V3_PWRON_PMU
- =PPVREF_PMU (PMU AVCC or 2.5V reference)

Signal aliases required by this page:
- =I2C_PMU_SCL
- =I2C_PMU_SDA
- =I2C_PMU_SMB_SCL
- =I2C_PMU_SMB_SDA
- =JTAG_BBANGER_TCK
- =JTAG_BBANGER_TDI
- =JTAG_BBANGER_TMS
- =JTAG_BBANGER_TRST_L

NOTE: Boot-banger pins can be aliased to TP_ or NC_ if not implemented.

BOM options provided by this page:
(NONE)

NOTE: TP_PMU_Px_x signals are general-purpose spares. Some pins are reserved for alternate functions. TP_PMU_AN_Px_x signals are general-purpose spares that can also be used as analog inputs.

NOTE: All analog inputs to PMU should have a 100pF capacitor to the PMU AVSS signal (GND_PMU_AVSS). None of those capacitors are provided on this page.

NET_TYPE | ELECTRICAL_CONSTRAINT_SET | SPACING | PHYSICAL | DIFFERENTIAL_PAIR

PMU_CLK10M_XTAL	XTAL	XTAL		PMU_CLK10M_XIN 25
	XTAL	XTAL		PMU_CLK10M_XOUT 25
	XTAL	XTAL		PMU_CLK10M_XOUT_R 25
PMU_CLK32K_XTAL	XTAL	XTAL		PMU_CLK32K_XIN 25
	XTAL	XTAL		PMU_CLK32K_XOUT 25
	XTAL	XTAL		PMU_CLK32K_XOUT_R 25

PMU Pull-ups / pull-downs

=PP3V3_ALL_PMU 10 24 25
- R2760 10K 5% 1/16W MF-LF 402 — PMU_POWER_UP_L 25 26
- R2761 10K 5% 1/16W MF-LF 402 — SYS_POWER_BUTTON_L 24 25 30 36 54

=PP3V3_PWRON_PMU 10
- R2765 10K 5% 1/16W MF-LF 402 — SYS_PME_L 22 25 62
- R2766 100K 5% 1/16W MF-LF 402 — SYS_RESET_BUTTON_L 24 25 36
- R2767 10K 5% 1/16W MF-LF 402 — SYS_OVERTEMP_L 7 11 25 30
- R2770 100K 5% 1/16W MF-LF 402 — SYS_COLD_RESET_L 25
- R2771 100K 5% 1/16W MF-LF 402 — SYS_WARM_RESET_L 22 25 62
- R2772 100K 5% 1/16W MF-LF 402 — PCI_RESET_L 11 25
- R2773 100K 5% 1/16W MF-LF 402 — NB_SUSPENDREQ_L 22 25
- R2774 100K 5% 1/16W MF-LF 402 — SYS_SLEEP 25

Power Management Unit

25 24 10 =PP3V3_ALL_PMU
- C2702 10UF 20% 6.3V X5R 603
- C2701 0.1uF 20% 10V CERM 402
- C2700 0.1uF 20% 10V CERM 402
- R2705 4.7 5% 1/10W MF-LF 402 — PP3V3_ALL_PMU_AVCC 10 (VOLTAGE=3.3V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
- C2705 1uF 10% 6.3V CERM 402 — GND_PMU_AVSS 25 28 29 31

U2700 M30280F8-LF QFP-80

VCC 13 AVCC 78

Spares (Analog capable)

TP_PMU_AN_P0_0	67	P0[0]	AN00	OMIT	P6[0]	43 GOV_RESET_L 11
11 TP_PMU_AN_P0_1	66	P0[1]	AN01	CLK0	P6[1]	42 PCI_RESET_L 11 25
11 TP_PMU_AN_P0_2	65	P0[2]	AN02	RxD0	P6[2]	41 SYS_WARM_RESET_L 22 25 62
11 TP_PMU_AN_P0_3	64	P0[3]	AN03	TxD0	P6[3]	40 SYS_COLD_RESET_L 25
11 TP_PMU_AN_P0_4	63	P0[4]	AN04	RTS1*/BUSY	P6[4]	31 PMU_BOOT_BUSY 24
11 TP_PMU_AN_P0_5	62	P0[5]	AN05	CLK1	P6[5]	30 PMU_BOOT_SCLK 24
25 TP_PMU_AN_P0_6	61	P0[6]	AN06	RxD1	P6[6]	29 PMU_BOOT_RXD 24
25 TP_PMU_AN_P0_7	60	P0[7]	AN07	TxD1	P6[7]	28 PMU_BOOT_TXD 24
						PMU_BOOT_RP_L 24
25 22 NB_SUSPENDREQ_L	59	P1[0]	AN20	SDA/TxD2/TA0out	P7[0]	27 TP_PMU_P7_0 25
22 NB_SUSPENDACK_L	58	P1[1]	AN21	SCL/RxD2/TA0in	P7[1]	26 TP_PMU_P7_1 25
11 PMU_CPU_CLK_EN	57	P1[2]	AN22	CLK2/TA1out	P7[2]	25 TP_PMU_P7_2 25
11 PMU_SYS_CLK_EN	56	P1[3]	AN23	TA1in	P7[3]	24 SYS_ACIN 12 13 18
36 25 24 SYS_RESET_BUTTON_L	55	P1[4]		TA2out	P7[4]	23 TP_PMU_P7_4 11 25
57 36 30 25 24 SYS_POWER_BUTTON_L	54	P1[5]	INT3*/ADtrig	TA2in	P7[5]	22 TP_PMU_P7_5 11 25
30 SYS_LID_OPEN	53	P1[6]	INT4*	TA3out	P7[6]	21 SYS_KBDLED 28
30 22 MODEM_RING2SYS_L	52	P1[7]	INT5*	TA3in	P7[7]	20 SYS_OVERTEMP_L 7 11 25 30
8 =I2C_PMU_SMB_SDA	51	P2[0]	IC0C0/SDAmm	TA4out	P8[0]	19 SYS_LED 24
8 =I2C_PMU_SMB_SCL	50	P2[1]	IC0C1/SCLmm	TA4in	P8[1]	18 PMU_BATT0_CHARGE 13
8 =I2C_PMU_SDA	49	P2[2]	IC0C2	INT0*	P8[2]	17 SYS_BATT0_DET_L 12 24
8 =I2C_PMU_SCL	48	P2[3]	IC0C3	INT1*	P8[3]	16 SYS_PME_L 22 25 62
9 =JTAG_BBANGER_TRST_L	47	P2[4]	IC0C4	INT2*	P8[4]	15 SYS_AC_DET 12
9 =JTAG_BBANGER_TMS	46	P2[5]	IC0C5	RP/NMI*	P8[5]	14 SYS_ONEWIRE 24
9 =JTAG_BBANGER_TDI	45	P2[6]	IC0C6	CE*/Xcout	P8[6]	8 25 PMU_CLK32K_XOUT_R
9 =JTAG_BBANGER_TCK	44	P2[7]	IC0C7	Xcin	P8[7]	7 25 PMU_CLK32K_XIN
25 11 TP_PMU_P3_0	39	P3[0]	CLK3	TB0in	P9[0]	5 VIA_ACK_L 22
25 11 TP_PMU_P3_1	38	P3[1]	Sin3	TB1in	P9[1]	4 VIA_REQ_L 22
25 11 TP_PMU_P3_2	37	P3[2]	Sout3	TB2in	P9[2]	3 PMU_INT_L 22
25 11 TP_PMU_P3_3	36	P3[3]		AN24	P9[3]	2 PMU_SB_NMI_L 22
22 SYS_WATCHDOG	35	P3[4]		CLK4/AN25	P9[5]	1 VIA_CLK 22
11 PMU_CPU_HRESET_L	34	P3[5]		Sout4/AN26	P9[6]	80 VIA_PMU_TO_SB 22
26 25 PMU_POWER_UP_L	33	P3[6]		Sin4//AN27	P9[7]	79 VIA_SB_TO_PMU 22
25 SYS_SLEEP	32	P3[7]				

Spares (Analog capable)

				AN0	P10[0]	76 TP_PMU_AN_P10_0 25
				AN1	P10[1]	74 TP_PMU_AN_P10_1 25
				AN2	P10[2]	73 TP_PMU_AN_P10_2 25
				AN3	P10[3]	72 TP_PMU_AN_P10_3 25
				KI0*/AN4	P10[4]	71 TP_PMU_AN_P10_4 25
				KI1*/AN5	P10[5]	70 TP_PMU_AN_P10_5 11 25
				KI2*/AN6	P10[6]	69 TP_PMU_AN_P10_6 11 25
				KI3*/AN7	P10[7]	68 TP_PMU_AN_P10_7 25

10 =PPVREF_PMU
- 24 PMU_BOOT_CNVSS → 6 PCNVSS
- 24 PMU_RESET_L → 9 RESET*
- 25 PMU_CLK10M_XOUT_R → 10 XOUT
- 25 PMU_CLK10M_XIN → 12 XIN
- 77 VREF

VSS 11 AVSS 75

25 24 10 =PP3V3_ALL_PMU
- D2710 MMBD914XXG SOT23
- R2710 150K 5% 1/16W MF-LF 402
- C2710 0.22uF 10% 6.3V CERM-X5R 402
- R2715 4.7K 5% 1/16W MF-LF 402
- C2720 1uF 10% 6.3V CERM 402
- XW2700 SM — GND_PMU_AVSS 25 28 29 31 (VOLTAGE=0V, MIN_LINE_WIDTH=0.38 mm, MIN_NECK_WIDTH=0.25 mm)
- R2730 4.7K 5% 1/16W MF-LF 402
- NO STUFF R2740 10M 5% 1/16W MF-LF 402
- R2741 0 5% 1/16W MF-LF 402
- CRITICAL Y2740 10.0000M 8X4.5MM-SM1
- 25 PMU_CLK10M_XOUT
- C2741 18pF 5% 50V CERM 402
- C2740 18pF 5% 50V CERM 402

Keep crystal subcircuit close to PMU.
Y2740's load capacitance is 12pF

- NO STUFF R2750 10M 5% 1/16W MF-LF 402
- R2751 0 5% 1/16W MF-LF 402
- CRITICAL Y2750 32.768K SM1
- C2750 12pF 5% 50V CERM 402
- C2751 12pF 5% 50V CERM 402
- PMU_CLK32K_XOUT 25

Additional PMU05 "Modules"

MMM

25 TP_PMU_AN_P10_0	MMM_X_AXIS	29
25 TP_PMU_AN_P10_1	MMM_Y_AXIS	29
25 TP_PMU_AN_P10_2	MMM_Z_AXIS	29
25 TP_PMU_P7_0	MMM_FFIRQ_L	22
25 TP_PMU_P7_1	MMM_SIRQ_L	22
25 TP_PMU_AN_P0_7	MMM_ACC_SELFTEST	29
25 TP_PMU_AN_P0_6	MMM_ACC_PWRDOWN	29

ALS

25 TP_PMU_AN_P10_3	ALS_0_OUT	7 31
25 TP_PMU_AN_P10_4	ALS_1_OUT	28
25 TP_PMU_P7_2	ALS_GAIN_BOOST	7 28 31

CPU T-Diodes

25 11 TP_PMU_AN_P10_5	CPU0_TEMP	
25 11 TP_PMU_AN_P10_6	CPU1_TEMP	

SPI Dual Battery Charger

25 11 TP_PMU_P3_0	SPI_PMU_CHGR_CLK
25 11 TP_PMU_P3_1	SPI_CHGR_TO_PMU_MISO
25 11 TP_PMU_P3_2	SPI_PMU_TO_CHGR_MOSI
25 11 TP_PMU_P3_3	SPI_PMU_CHGR_CS
25 11 TP_PMU_P7_4	PMU_BATT1_DET_L
25 11 TP_PMU_P7_5	PMU_BATT1_CHARGE

Battery Current Mon

25 TP_PMU_AN_P10_7	BATT_ISNS	12

Power Management Unit (PMU05)

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE SHT 27 OF 115

POWER-UP
SLEEP
WAKE
SHUT-DOWN

ACTIVE-LOW, OUTPUT, OPEN-COLLECTOR
PMU_POWER_UP_L
100K pull-up to 3.3V_ALL on pg 13

R2900 0 5% 1/16W MF-LF 402
SYS_POWER_UP_L

R2902 0 5% 1/16W MF-LF 402
5V3V3PWRON_EN_L
MAKE_BASE=TRUE
=5V3V3PWRON_EN_L

=PP3V3_ALL_PWRSEQ
R2901 100K 5% 1/16W MF-LF 402
SYS_POWERUP

R2903 0 5% 1/16W MF-LF 402
FWPWR_PWRON
MAKE_BASE=TRUE
=FWPWR_PWRON

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SYS_PWRSEQ_1

R2913 100K 5% 1/16W MF-LF 402

=PP5V_PWRON_PWRSEQ
R2929 100K 5% 1/16W MF-LF 402
SYS_PWRSEQ_2_L

Q2900 2N7002DW-X-F SOT-363

R2910 100K 5% 1/16W MF-LF 402

R2911 0 5% 1/16W MF-LF 402
1V8_1V5PWRON_EN_L
MAKE_BASE=TRUE
=1V8_1V5PWRON_EN_L

R2912 0 5% 1/16W MF-LF 402
SYS_PWRSEQ_1_L
2V5PWRON_EN_L
MAKE_BASE=TRUE
=2V5PWRON_EN_L

R2920 100K 5% 1/16W MF-LF 402
5VRUN_EN_L

R2921 100K 5% 1/16W MF-LF 402
5VRUNHD_EN_L

R2922 100K 5% 1/16W MF-LF 402
3V3RUN_EN_L

ACTIVE-HIGH, OUTPUT, PUSH-PULL
SYS_PWRSEQ_2

Q2910 2N7002DW-X-F SOT-363

Q2900 2N7002DW-X-F SOT-363

ACTIVE-LOW, OUTPUT, PUSH-PULL
SYS_PWRSEQ_3_L

R2930 0 5% 1/16W MF-LF 402
2V5RUN_EN_L

=PP5V_RUN_PWRSEQ
R2935 100K 5% 1/16W MF-LF 402
SYS_PWRSEQ_3_LS5

R2936 100K 5% 1/16W MF-LF 402
1V5RUN_EN

Q2910 2N7002DW-X-F SOT-363

=PP5V_PWRON_PWRSEQ
R2941 100K 5% 1/16W MF-LF 402
R2942 100K 5% 1/16W MF-LF 402
PWRON_REGS_PGOOD_L

=PP3V3_RUN_PWRSEQ
R2948 100K 5% 1/16W MF-LF 402
RUN_REGS_PGOOD

R2940 0 5% 1/16W MF-LF 402
VCORE_CPU0_SHDN_L

1V8RUN_EN_L

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SYS_PWRSEQ_4

R2949 0 5% 1/16W MF-LF 402

Q2941 2N7002DW-X-F SOT-363

Q2940 2N7002DW-X-F SOT-363

Q2941 2N7002DW-X-F SOT-363

=PP3V3_RUN_PWRSEQ
=5V3VPWRON_PGOOD
=1V8_1V5PWRON_PGOOD
=2V5PWRON_PGOOD
=I2VCORE_PGOOD
PWRON_REGS_PGOOD
MAKE_BASE=TRUE

R2958 100K 5% 1/16W MF-LF 402

R2943 0 5% 1/16W MF-LF 402
5VTPAD_EN_L
MAKE_BASE=TRUE
=5VPWRONTPAD_EN_L

ACTIVE-HIGH, OUTPUT/INPUT, OPEN-COLLECTOR
SYS_PWRSEQ_5

R2950 0 5% 1/16W MF-LF 402
GPUVCORE_SHDN_L

R2951 0 5% 1/16W MF-LF 402
CPU_AVDD_EN

=VCORE_PGOOD
TP_VCORE_PGOOD
MAKE_BASE=TRUE

ACTIVE-LOW, OUTPUT, PUSH-PULL
SYS_PWRSEQ_6_L

=PP5V_RUN_PWRSEQ
R2965 100K 5% 1/16W MF-LF 402

R2969 0 5% 1/16W MF-LF 402
=GPUVCORE_PGOOD
GPUVCORE_PGOOD
MAKE_BASE=TRUE
SYS_PWRSEQ_6_LS5
MAKE_BASE=TRUE

R2966 100K 5% 1/16W MF-LF 402
GPUVDD15_EN

R2967 0 5% 1/16W MF-LF 402
GPUPVDD_EN

Q2940 2N7002DW-X-F SOT-363

ANALOG INPUT, SENSE > 1.7V
SYS_PWRSEQ_FINAL

XW2970 SM
PP1V8_GPU_PVDD
Used to see if last rail is up

Power Sequencing

SYNC_MASTER=N/A
SYNC_DATE=N/A

APPLE COMPUTER INC.

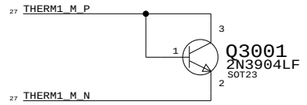
SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	29	115

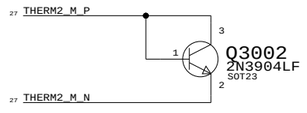
FAN CONTROLLER

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
1528	THERM	THERM	THERM1_M	THERM1_M_P
1529	THERM	THERM	THERM1_M	THERM1_M_N
1530	THERM	THERM	THERM2_M	THERM2_M_P
1531	THERM	THERM	THERM2_M	THERM2_M_N
1532	THERM	THERM	THERM1_A	THERM1_A_P
1533	THERM	THERM	THERM1_A	THERM1_A_N
1534	THERM	THERM	THERM2_A	THERM2_A_P
1535	THERM	THERM	THERM2_A	THERM2_A_N
1536	THERM	THERM	THERM_D1	THERM_D1_P
1537	THERM	THERM	THERM_D1	THERM_D1_N
1538	THERM	THERM	THERM_D2	THERM_D2_P
1539	THERM	THERM	THERM_D2	THERM_D2_N

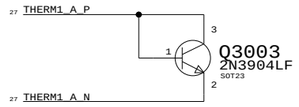
PLACE CLOSE TO CPU
MAIN1



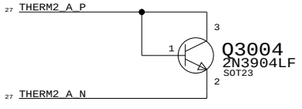
PLACE IN BETWEEN 3/5/1.5/2.5V PWR SUPPLY
MAIN2

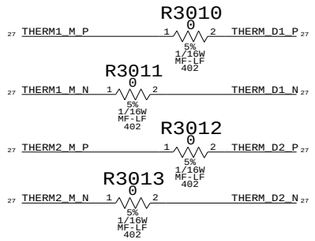


PLACE UNDERNEATH UPPER RAM
ALTERNATE1

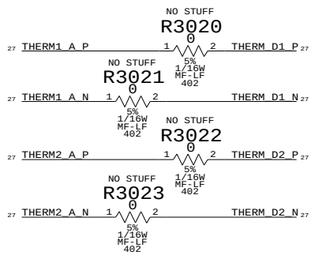


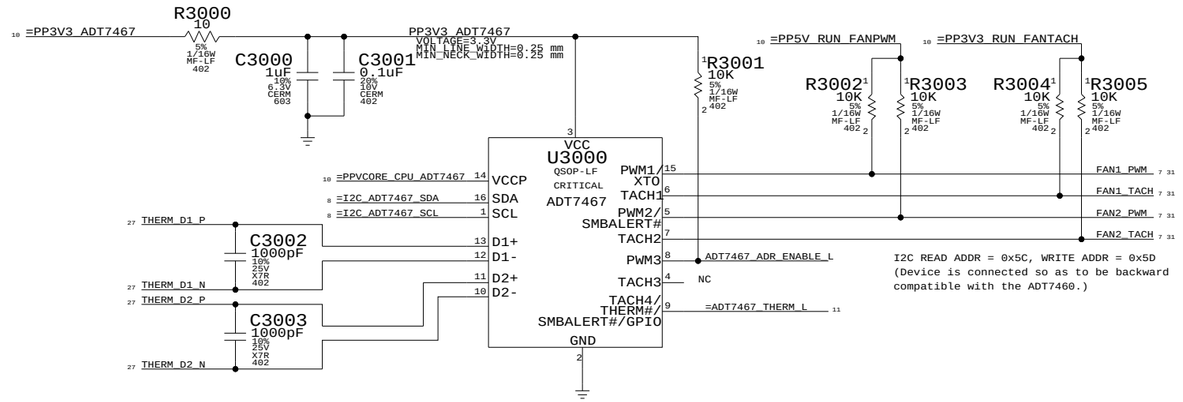
PLACE CLOSE TO BATTERY CHARGER/VCORE
ALTERNATE2





KEEP STUFFING RESISTORS CLOSE TO ADT7467 CONTROLLER

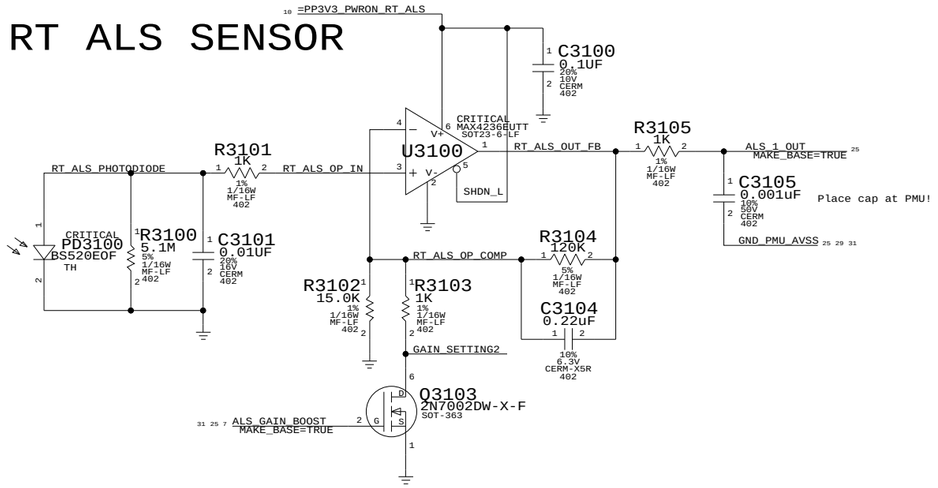




Fan Controller			
SYNC_MASTER=N/A		SYNC_DATE=N/A	

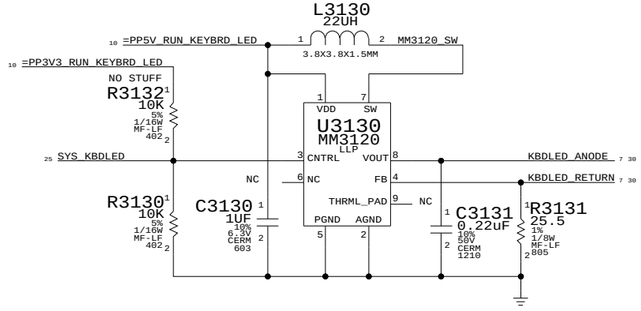
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6929	03
	SCALE: NONE	SHT 30 OF 115	

RT ALS SENSOR



PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0856	353S0504	?	U3100	

Keyboard LED Driver



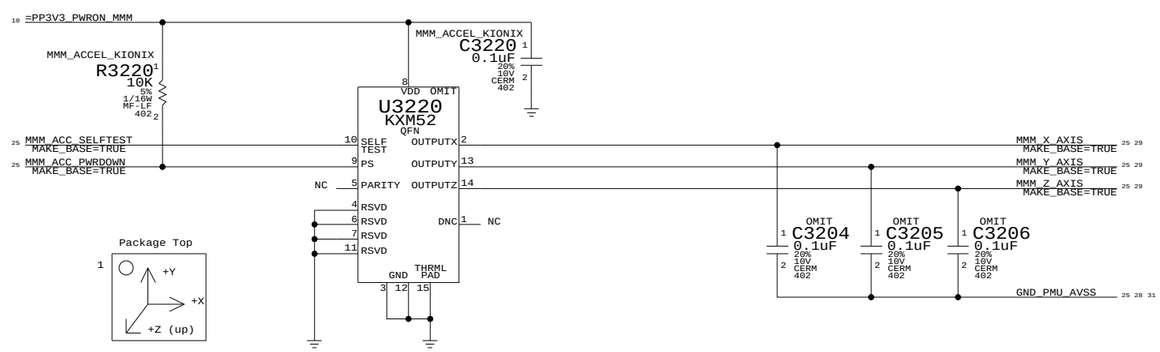
ALS Support

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 31 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
I57	THERM	THERM	MMM_X_AXIS
I58	THERM	THERM	MMM_Y_AXIS
I59	THERM	THERM	MMM_Z_AXIS



PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0222	1	IC,KIONIX,KXM52-2050,3AXIS ACCELEROMETER,SMD	U3220	CRITICAL	MMM_ACCEL_KIONIX

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	BOM OPTION
132S4733	3	CAP,CER .0047UF,10%,25V,X7R,0402,SMD	C3204,C3205,C3206	MMM_ACCEL_KIONIX

Sudden Motion Sensor

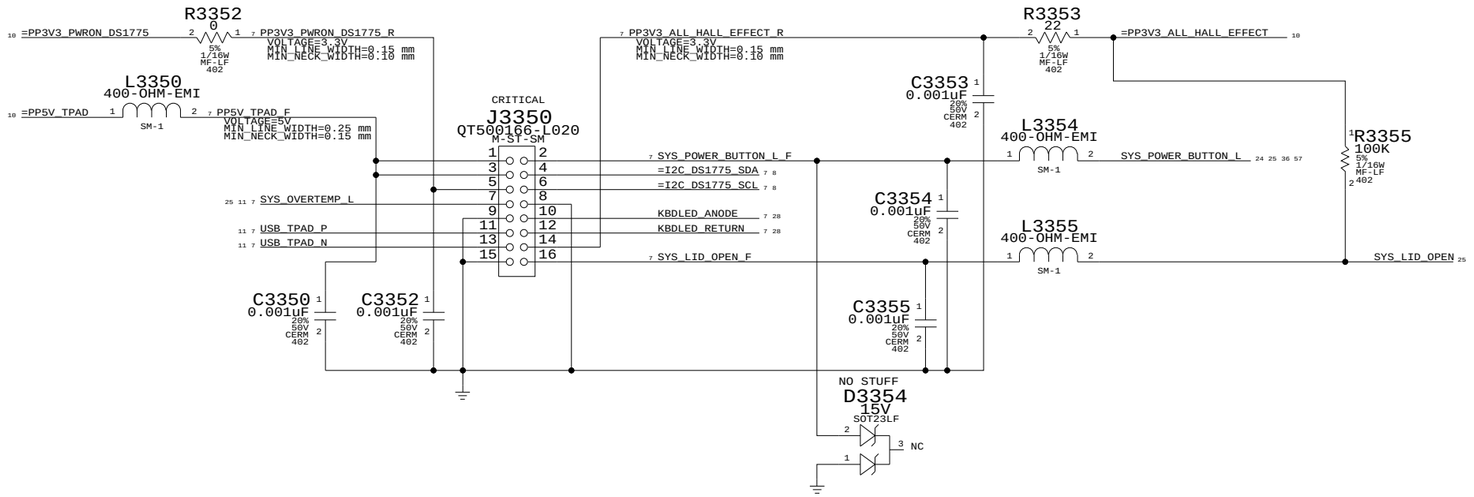
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

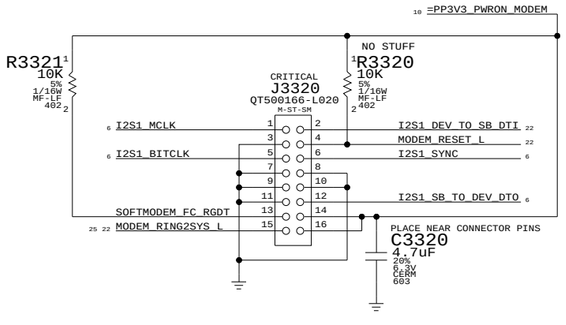
SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE NONE SHT 32 OF 115

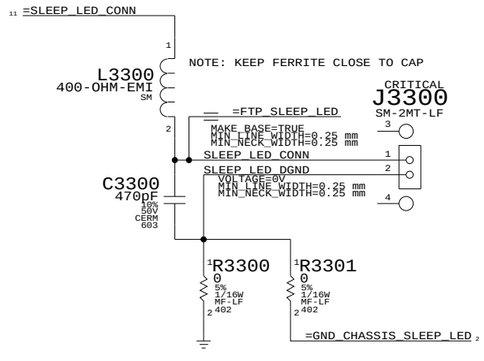
USB Trackpad Connector



SOFT MODEM CONN



SLEEP LED CONNECTOR



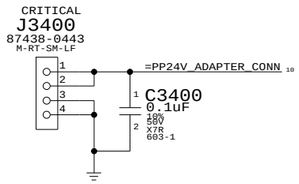
Q16C Internal I/O I

SYNC_MASTER=N/A SYNC_DATE=N/A

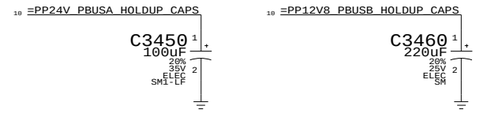
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 33 OF 115	

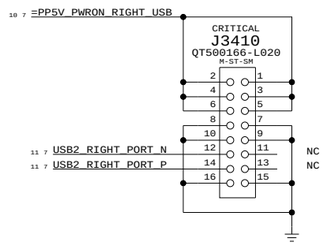
ADAPTER CONNECTOR



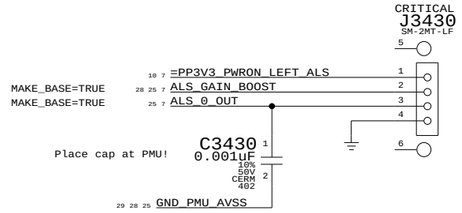
PBUS HOLD-UP CAPS



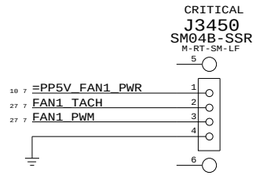
RIGHT USB BOARD



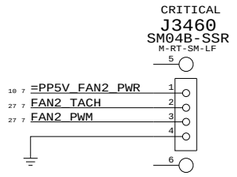
LEFT ALS CONNECTOR



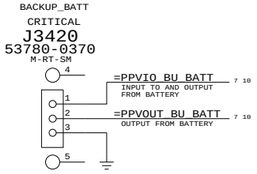
CPU FAN



GPU FAN



BACKUP BATTERY CONNECTOR



Q16C Internal I/O II

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	34	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: SPACING	NET_TYPE: PHYSICAL	DIFFERENTIAL_PAIR
MAXBUS_CLK_CPU0	CLOCK	CLOCK	
MAXBUS_CLK_CPU1	CLOCK	CLOCK	
I2_MAXBUS_FBCLK	I2_FBCLK	I2_FBCLK	
	I2_FBCLK	I2_FBCLK	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA41	MAXBUS	MAXBUS	
MAXBUS_DATA42	MAXBUS	MAXBUS	
MAXBUS_DATA43	MAXBUS	MAXBUS	
MAXBUS_DATA44	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA54	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_DATA62	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NBTO	MAXBUS	MAXBUS	
MAXBUS_DTI	MAXBUS	MAXBUS	
MAXBUS_GBL_L	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NBTO	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NBTO	MAXBUS	MAXBUS	
MAXBUS_CPU0_BIDIR	MAXBUS	MAXBUS	
MAXBUS_WT_L	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU0_R	MAXBUS	MAXBUS	
MAXBUS_CPU0_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU0_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	
MAXBUS_NB_TO_CPU1_R	MAXBUS	MAXBUS	
MAXBUS_CPU1_DRDY_L	MAXBUS	MAXBUS	
MAXBUS_CPU1_TO_NB_R	MAXBUS	MAXBUS	

MAXBUS_CLK_CPU0_R	11 32
TP_MAXBUS_CLK_CPU1_R	11 32
I2_MAXBUS_FBCLK_OUT_R	32
I2_MAXBUS_FBCLK_OUT	21 32
MAXBUS_ADDR<0..31>	9 32 33
MAXBUS_DATA<0..40>	9 32 33
MAXBUS_DATA<41>	9 21 32 33
MAXBUS_DATA<42>	9 21 32 33
MAXBUS_DATA<43>	9 21 32 33
MAXBUS_DATA<44>	9 21 32 33
MAXBUS_DATA<45..53>	9 32 33
MAXBUS_DATA<54>	9 21 32 33
MAXBUS_DATA<55..61>	9 32 33
MAXBUS_DATA<62>	9 21 32 33
MAXBUS_DATA<63>	9 32 33
MAXBUS_TS_L	6 32 33
MAXBUS_TA_L	6 32 33
MAXBUS_TEA_L	6 32 33
MAXBUS_AACK_L	6 32 33
MAXBUS_ARTRY_L	6 32 33
MAXBUS_CI_L	9 32 33
MAXBUS_DTI<0..2>	9 32 33
MAXBUS_GBL_L	9 32 33
MAXBUS_TBST_L	9 32 33
MAXBUS_TSIZ<0..2>	9 32 33
MAXBUS_TT<0..4>	9 32 33
MAXBUS_WT_L	9 32 33
MAXBUS_CPU0_BG_L	6 32 33
MAXBUS_CPU0_BR_L	6 32 33
MAXBUS_CPU0_DBG_L	6 32 33
MAXBUS_CPU0_DRDY_L	6 32 33
MAXBUS_CPU0_HIT_L	6 32 33
MAXBUS_CPU1_BG_L	6 32
MAXBUS_CPU1_BR_L	6 32
MAXBUS_CPU1_DBG_L	6 32
MAXBUS_CPU1_DRDY_L	6 32
MAXBUS_CPU1_HIT_L	6 32

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_I2_MAXBUS

BOM options provided by this page:
- MAXBUS_1V8 - Provides required voltage divider for FBCLK if MaxBus OVdd=1.8V.

Signal aliases required by this page:
- =I2_MAXBUS_FBCLK_IN - MaxBus feedback clock input. Length should match that of clock(s) from I2 to CPU(s).

MaxBus I/O DECOUPLING

(41 Balls on I2)

OMIT
U2100
I2
BGA
MAXBUS POWER
(6 of 14)

32 10 =PP1V5R1V8_I2_MAXBUS

1 X 10uF (0603)
41 X 1uF (0402)

VDD18_0 C11	C3550 1uF 10% 6.3V CERM 402	C3551 1uF 10% 6.3V CERM 402	C3552 1uF 10% 6.3V CERM 402	C3553 1uF 10% 6.3V CERM 402	C3554 1uF 10% 6.3V CERM 402	C3555 1uF 10% 6.3V CERM 402
VDD18_1 C14						
VDD18_2 C17						
VDD18_3 C20						
VDD18_4 C23	C3556 1uF 10% 6.3V CERM 402	C3557 1uF 10% 6.3V CERM 402	C3558 1uF 10% 6.3V CERM 402	C3559 1uF 10% 6.3V CERM 402	C3560 1uF 10% 6.3V CERM 402	C3561 1uF 10% 6.3V CERM 402
VDD18_5 C26						
VDD18_6 C29						
VDD18_7 C3						
VDD18_8 C32	C3562 1uF 10% 6.3V CERM 402	C3563 1uF 10% 6.3V CERM 402	C3564 1uF 10% 6.3V CERM 402	C3565 1uF 10% 6.3V CERM 402	C3566 1uF 10% 6.3V CERM 402	C3567 1uF 10% 6.3V CERM 402
VDD18_9 C8						
VDD18_10 F11						
VDD18_11 F14						
VDD18_12 F17	C3568 1uF 10% 6.3V CERM 402	C3569 1uF 10% 6.3V CERM 402	C3570 1uF 10% 6.3V CERM 402	C3571 1uF 10% 6.3V CERM 402	C3572 1uF 10% 6.3V CERM 402	C3573 1uF 10% 6.3V CERM 402
VDD18_13 F20						
VDD18_14 F23						
VDD18_15 F26						
VDD18_16 F29	C3574 1uF 10% 6.3V CERM 402	C3575 1uF 10% 6.3V CERM 402	C3576 1uF 10% 6.3V CERM 402	C3577 1uF 10% 6.3V CERM 402	C3578 1uF 10% 6.3V CERM 402	C3579 1uF 10% 6.3V CERM 402
VDD18_17 F8						
VDD18_18 J11						
VDD18_19 J12						
VDD18_20 J14						
VDD18_21 J15						
VDD18_22 J17						
VDD18_23 J18						
VDD18_24 J20						
VDD18_25 J23						
VDD18_26 J24						
VDD18_27 J26						
VDD18_28 J27						
VDD18_29 L14						
VDD18_30 L17	C3580 1uF 10% 6.3V CERM 402	C3581 1uF 10% 6.3V CERM 402	C3582 1uF 10% 6.3V CERM 402	C3583 1uF 10% 6.3V CERM 402	C3584 1uF 10% 6.3V CERM 402	C3585 1uF 10% 6.3V CERM 402
VDD18_31 L23						
VDD18_32 M20						
VDD18_33 N15						
VDD18_34 N19						
VDD18_35 N21						
VDD18_36 N22						
VDD18_37 P14	C3586 1uF 10% 6.3V CERM 402	C3587 1uF 10% 6.3V CERM 402	C3588 1uF 10% 6.3V CERM 402	C3589 1uF 10% 6.3V CERM 402	C3590 1uF 10% 6.3V CERM 402	
VDD18_38 P15						
VDD18_39 P18						
VDD18_40 P22						

C3599 10uF 20% 6.3V X5R 603

OMIT
U2100
I2
BGA
PROCESSOR INTERFACE
(5 of 14)

PROCESSOR 0

33 32 MAXBUS_CPU0_QREQ_L	E25	MAX_QREQ_0_L	MAX_QACK_0_L	F18	MAXBUS_CPU0_QACK_L 33
33 32 6 MAXBUS_CPU0_BR_L	F21	MAX_BR_0_L	MAX_BG_0_L	E22	MAXBUS_CPU0_BG_L 6 32 33
33 32 6 MAXBUS_CPU0_DRDY_L	G25	MAX_DRDY_0_L	MAX_DBG_0_L	F24	MAXBUS_CPU0_DBG_L 6 32 33
33 32 6 MAXBUS_CPU0_HIT_L	E21	MAX_HIT_0_L	CPU_INT_0_L	J19	MAXBUS_CPU0_INT_L 6 34
			MAX_CLK_0_H	H21	MAXBUS_CLK_CPU0_R 11 32

PROCESSOR 1

32 MAXBUS_CPU1_QREQ_L	E27	MAX_QREQ_1_L	MAX_QACK_1_L	G18	TP_MAXBUS_CPU1_QACK_L 11
32 6 MAXBUS_CPU1_BR_L	G21	MAX_BR_1_L	MAX_BG_1_L	E24	MAXBUS_CPU1_BG_L 6 32
32 6 MAXBUS_CPU1_DRDY_L	F25	MAX_DRDY_1_L	MAX_DBG_1_L	G24	MAXBUS_CPU1_DBG_L 6 32
32 6 MAXBUS_CPU1_HIT_L	C21	MAX_HIT_1_L	CPU_INT_1_L	H19	MAXBUS_CPU1_INT_L 6
			MAX_CLK_1_H	J21	TP_MAXBUS_CLK_CPU1_R 11 32

MAXBUS INTERFACE

33 32 6 MAXBUS_TS_L	B27	MAX_TS_L	MAX_AACK_L	A31	MAXBUS_AACK_L 6 32 33
33 32 6 MAXBUS_ARTRY_L	C30	MAX_ARTRY_L			
33 32 9 MAXBUS_ADDR<0>	D18	MAX_A_00_H	MAX_D_00_H	D16	MAXBUS_DATA<0> 9 32 33
33 32 9 MAXBUS_ADDR<1>	A28	MAX_A_01_H	MAX_D_01_H	A10	MAXBUS_DATA<1> 9 32 33
33 32 9 MAXBUS_ADDR<2>	A19	MAX_A_02_H	MAX_D_02_H	A9	MAXBUS_DATA<2> 9 32 33
33 32 9 MAXBUS_ADDR<3>	A23	MAX_A_03_H	MAX_D_03_H	D12	MAXBUS_DATA<3> 9 32 33
33 32 9 MAXBUS_ADDR<4>	D21	MAX_A_04_H	MAX_D_04_H	A11	MAXBUS_DATA<4> 9 32 33
33 32 9 MAXBUS_ADDR<5>	A25	MAX_A_05_H	MAX_D_05_H	B10	MAXBUS_DATA<5> 9 32 33
33 32 9 MAXBUS_ADDR<6>	A18	MAX_A_06_H	MAX_D_06_H	C10	MAXBUS_DATA<6> 9 32 33
33 32 9 MAXBUS_ADDR<7>	C28	MAX_A_07_H	MAX_D_07_H	G16	MAXBUS_DATA<7> 9 32 33
33 32 9 MAXBUS_ADDR<8>	D25	MAX_A_08_H	MAX_D_08_H	D9	MAXBUS_DATA<8> 9 32 33
33 32 9 MAXBUS_ADDR<9>	B31	MAX_A_09_H	MAX_D_09_H	C9	MAXBUS_DATA<9> 9 32 33
33 32 9 MAXBUS_ADDR<10>	B24	MAX_A_10_H	MAX_D_10_H	F15	MAXBUS_DATA<10> 9 32 33
33 32 9 MAXBUS_ADDR<11>	G28	MAX_A_11_H	MAX_D_11_H	G15	MAXBUS_DATA<11> 9 32 33
33 32 9 MAXBUS_ADDR<12>	C25	MAX_A_12_H	MAX_D_12_H	B9	MAXBUS_DATA<12> 9 32 33
33 32 9 MAXBUS_ADDR<13>	D31	MAX_A_13_H	MAX_D_13_H	D10	MAXBUS_DATA<13> 9 32 33
33 32 9 MAXBUS_ADDR<14>	F19	MAX_A_14_H	MAX_D_14_H	E15	MAXBUS_DATA<14> 9 32 33
33 32 9 MAXBUS_ADDR<15>	E30	MAX_A_15_H	MAX_D_15_H	C7	MAXBUS_DATA<15> 9 32 33
33 32 9 MAXBUS_ADDR<16>	D27	MAX_A_16_H	MAX_D_16_H	B7	MAXBUS_DATA<16> 9 32 33
33 32 9 MAXBUS_ADDR<17>	A27	MAX_A_17_H	MAX_D_17_H	A8	MAXBUS_DATA<17> 9 32 33
33 32 9 MAXBUS_ADDR<18>	B28	MAX_A_18_H	MAX_D_18_H	F16	MAXBUS_DATA<18> 9 32 33
33 32 9 MAXBUS_ADDR<19>	B25	MAX_A_19_H	MAX_D_19_H	G13	MAXBUS_DATA<19> 9 32 33
33 32 9 MAXBUS_ADDR<20>	E19	MAX_A_20_H	MAX_D_20_H	E13	MAXBUS_DATA<20> 9 32 33
33 32 9 MAXBUS_ADDR<21>	G27	MAX_A_21_H	MAX_D_21_H	E12	MAXBUS_DATA<21> 9 32 33
33 32 9 MAXBUS_ADDR<22>	D30	MAX_A_22_H	MAX_D_22_H	D7	MAXBUS_DATA<22> 9 32 33
33 32 9 MAXBUS_ADDR<23>	C31	MAX_A_23_H	MAX_D_23_H	A7	MAXBUS_DATA<23> 9 32 33
33 32 9 MAXBUS_ADDR<24>	F28	MAX_A_24_H	MAX_D_24_H	G12	MAXBUS_DATA<24> 9 32 33
33 32 9 MAXBUS_ADDR<25>	F27	MAX_A_25_H	MAX_D_25_H	F12	MAXBUS_DATA<25> 9 32 33
33 32 9 MAXBUS_ADDR<26>	B30	MAX_A_26_H	MAX_D_26_H	F13	MAXBUS_DATA<26> 9 32 33
33 32 9 MAXBUS_ADDR<27>	E28	MAX_A_27_H	MAX_D_27_H	A6	MAXBUS_DATA<27> 9 32 33
33 32 9 MAXBUS_ADDR<28>	B18	MAX_A_28_H	MAX_D_28_H	E10	MAXBUS_DATA<28> 9 32 33
33 32 9 MAXBUS_ADDR<29>	C22	MAX_A_29_H	MAX_D_29_H	B6	MAXBUS_DATA<29> 9 32 33
33 32 9 MAXBUS_ADDR<30>	A17	MAX_A_30_H	MAX_D_30_H	C6	MAXBUS_DATA<30> 9 32 33
33 32 9 MAXBUS_ADDR<31>	B19	MAX_A_31_H	MAX_D_31_H	D6	MAXBUS_DATA<31> 9 32 33
			MAX_D_32_H	G7	MAXBUS_DATA<32> 9 32 33
			MAX_D_33_H	A3	MAXBUS_DATA<33> 9 32 33
			MAX_D_34_H	E6	MAXBUS_DATA<34> 9 32 33
			MAX_D_35_H	F7	MAXBUS_DATA<35> 9 32 33
			MAX_D_36_H	C4	MAXBUS_DATA<36> 9 32 33
			MAX_D_37_H	D3	MAXBUS_DATA<37> 9 32 33
			MAX_D_38_H	G9	MAXBUS_DATA<38> 9 32 33
			MAX_D_39_H	D4	MAXBUS_DATA<39> 9 32 33
			MAX_D_40_H	B16	MAXBUS_DATA<40> 9 32 33
			MAX_D_41_H	C16	MAXBUS_DATA<41> 9 21 32 33
			MAX_D_42_H	A13	MAXBUS_DATA<42> 9 21 32 33
			MAX_D_43_H	A16	MAXBUS_DATA<43> 9 21 32 33
			MAX_D_44_H	C13	MAXBUS_DATA<44> 9 21 32 33
			MAX_D_45_H	B15	MAXBUS_DATA<45> 9 32 33
			MAX_D_46_H	D15	MAXBUS_DATA<46> 9 32 33
			MAX_D_47_H	B12	MAXBUS_DATA<47> 9 32 33
			MAX_D_48_H	A14	MAXBUS_DATA<48> 9 32 33
			MAX_D_49_H	A12	MAXBUS_DATA<49> 9 32 33
			MAX_D_50_H	D13	MAXBUS_DATA<50> 9 32 33
			MAX_D_51_H	B13	MAXBUS_DATA<51> 9 32 33
			MAX_D_52_H	A15	MAXBUS_DATA<52> 9 32 33
			MAX_D_53_H	C15	MAXBUS_DATA<53> 9 32 33
			MAX_D_54_H	C5	MAXBUS_DATA<54> 9 21 32 33
			MAX_D_55_H	C12	MAXBUS_DATA<55> 9 32 33
			MAX_D_56_H	F6	MAXBUS_DATA<56> 9 32 33
			MAX_D_57_H	A5	MAXBUS_DATA<57> 9 32 33
			MAX_D_58_H	F9	MAXBUS_DATA<58> 9 32 33
			MAX_D_59_H	E9	MAXBUS_DATA<59> 9 32 33
			MAX_D_60_H	E7	MAXBUS_DATA<60> 9 32 33
			MAX_D_61_H	G10	MAXBUS_DATA<61> 9 32 33
			MAX_D_62_H	B4	MAXBUS_DATA<62> 9 21 32 33
			MAX_D_63_H	F10	MAXBUS_DATA<63> 9 32 33
33 32 9 MAXBUS_CI_L	A26	MAX_CI_L	MAX_DTI_0_H	C27	MAXBUS_DTI<0> 9 32 33
33 32 9 MAXBUS_GBL_L	A24	MAX_GBL_L	MAX_DTI_1_H	A30	MAXBUS_DTI<1> 9 32 33
33 32 9 MAXBUS_TBST_L	E16	MAX_TBST_L	MAX_DTI_2_H	A29	MAXBUS_DTI<2> 9 32 33
33 32 9 MAXBUS_TSIZ<0>	D19	MAX_TSIZ_0_H			
33 32 9 MAXBUS_TSIZ<1>	C18	MAX_TSIZ_1_H	MAX_TA_L	G19	MAXBUS_TA_L 6 32 33
33 32 9 MAXBUS_TSIZ<2>	B21	MAX_TSIZ_2_H	MAX_TEA_L	D28	MAXBUS_TEA_L 6 32 33
33 32 9 MAXBUS_TT<0>	B22	MAX_TT_0_H			
33 32 9 MAXBUS_TT<1>	D22	MAX_TT_1_H	MAX_TBEN_H	C24	6 MAXBUS_TBEN_I2
33 32 9 MAXBUS_TT<2>	E18	MAX_TT_2_H			
33 32 9 MAXBUS_TT<3>	A21	MAX_TT_3_H			
33 32 9 MAXBUS_TT<4>	A22	MAX_TT_4_H			
33 32 9 MAXBUS_WT_L	D24	MAX_WT_L	MAX_FBCLK_OUT_H	J22	32 I2_MAXBUS_FBCLK_OUT_R

I2_ACS_REF — R3500 1K 1% 1/16W MF-LF 402 — K9 ACS_REF_H

21 =I2_MAXBUS_FBCLK_IN — MAXBUS_1V8 — R3506 360 5% 1/16W MF-LF 402 — H22 MAX_CLK_FB_IN_H (1.5V IN)

1.5V-1.8V OUT (Matches MaxBus OVdd)
Output impedance is 50 Ohms

MAXBUS_TBEN_I2 — R3507 0 5% 1/16W MF-LF 402 — MAXBUS_TBEN 21 33

R3505 10 5% 1/16W MF-LF 402 — I2_MAXBUS_FBCLK_OUT 21 32

MaxBus Pull-ups / Pull-downs

32 10 =PP1V5R1V8_I2_MAXBUS

One resistor for each of:
- MAXBUS_TS_L
- MAXBUS_TA_L
- MAXBUS_TEA_L
- MAXBUS_ARTRY_L
- MAXBUS_AACK_L
- MAXBUS_TBEN

6 =RP3510P1	RP3510 10K 5% 1/16W SM-LF	1 8
6 =RP3510P2	RP3510 10K 5% 1/16W SM-LF	2 7
6 =RP3510P3	RP3510 10K 5% 1/16W SM-LF	3 6
6 =RP3510P4	RP3510 10K 5% 1/16W SM-LF	4 5
6 =RP3511P1	RP3511 10K 5% 1/16W SM-LF	1 8
6 =RP3511P2	RP3511 10K 5% 1/16W SM-LF	2 7

I2 CPU0 Support

One resistor for each of:
- MAXBUS_CPU0_BR_L
- MAXBUS_CPU0_BG_L
- MAXBUS_CPU0_DBG_L
- MAXBUS_CPU0_DRDY_L
- MAXBUS_CPU0_HIT_L
- MAXBUS_CPU0_INT_L

6 =RP3511P3	RP3511 10K 5% 1/16W SM-LF	3 6
6 =RP3511P4	RP3511 10K 5% 1/16W SM-LF	4 5
6 =RP3512P1	RP3512 10K 5% 1/16W SM-LF	1 8
6 =RP3512P2	RP3512 10K 5% 1/16W SM-LF	2 7
6 =RP3512P3	RP3512 10K 5% 1/16W SM-LF	3 6
6 =RP3512P4	RP3512 10K 5% 1/16W SM-LF	4 5
33 32 MAXBUS_CPU0_QREQ_L	R3513 10K 5% 1/16W MF-LF 402	1 2

I2 CPU1 Support

One resistor for each of:
- MAXBUS_CPU1_BR_L
- MAXBUS_CPU1_BG_L
- MAXBUS_CPU1_DBG_L
- MAXBUS_CPU1_DRDY_L
- MAXBUS_CPU1_HIT_L
- MAXBUS_CPU1_INT_L

6 =RP3513P2	RP3513 10K 5% 1/16W SM-LF	2 7
6 =RP3513P3	RP3513 10K 5% 1/16W SM-LF	3 6
6 =RP3513P4	RP3513 10K 5% 1/16W SM-LF	4 5
6 =RP3514P1	RP3514 10K 5% 1/16W SM-LF	1 8
6 =RP3514P2	RP3514 10K 5% 1/16W SM-LF	2 7
6 =RP3514P3	RP3514 10K 5% 1/16W SM-LF	3 6
32 MAXBUS_CPU1_QREQ_L	R3514 10K 5% 1/16W MF-LF 402	1 2

I2 Processor Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 35 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
100R	CLOCK	CLOCK	

=MAXBUS_CPU0_CLK 11 33

Page Notes

Power aliases required by this page:

- =PP1V5R1V8_MAXBUS

Signal aliases required by this page:

- =MAXBUS_CPU0_CLK

BOM options provided by this page:

(NONE)

34 33 21 10 =PP1V5R1V8_MAXBUS

U3600
BGA
(5 OF 6)
XXGHZ-XXV
A8-X.X

OVDD: B4, C2, C12, D5, F2, H3, J5, K2, L5, M3, N6, P2, P8

OVDD: P11, R4, R13, R16, T6, T9, U2, U12, U16, V4, V7, V10, V14

OMIT
CRITICAL

TP_CPU0_OVDDSENSE1 E18 OVDDSENSE1
TP_CPU0_OVDDSENSE2 G18 OVDDSENSE2
(Kelvin sense points)

U3600
BGA
(2 OF 6)
XXGHZ-XXV
A8-X.X

OMIT
CRITICAL

32 9 MAXBUS_DATA<0>	R15	D0	
32 9 MAXBUS_DATA<1>	W15	D1	
32 9 MAXBUS_DATA<2>	T14	D2	
32 9 MAXBUS_DATA<3>	V16	D3	
32 9 MAXBUS_DATA<4>	W16	D4	
32 9 MAXBUS_DATA<5>	T15	D5	
32 9 MAXBUS_DATA<6>	U15	D6	
32 9 MAXBUS_DATA<7>	P14	D7	
32 9 MAXBUS_DATA<8>	V13	D8	
32 9 MAXBUS_DATA<9>	W13	D9	
32 9 MAXBUS_DATA<10>	T13	D10	
32 9 MAXBUS_DATA<11>	P13	D11	
32 9 MAXBUS_DATA<12>	U14	D12	
32 9 MAXBUS_DATA<13>	W14	D13	
32 9 MAXBUS_DATA<14>	R12	D14	
32 9 MAXBUS_DATA<15>	T12	D15	
32 9 MAXBUS_DATA<16>	W12	D16	
32 9 MAXBUS_DATA<17>	V12	D17	
32 9 MAXBUS_DATA<18>	N11	D18	
32 9 MAXBUS_DATA<19>	N10	D19	
32 9 MAXBUS_DATA<20>	R11	D20	
32 9 MAXBUS_DATA<21>	U11	D21	
32 9 MAXBUS_DATA<22>	W11	D22	
32 9 MAXBUS_DATA<23>	T11	D23	
32 9 MAXBUS_DATA<24>	R10	D24	
32 9 MAXBUS_DATA<25>	N9	D25	
32 9 MAXBUS_DATA<26>	P10	D26	
32 9 MAXBUS_DATA<27>	U10	D27	
32 9 MAXBUS_DATA<28>	R9	D28	
32 9 MAXBUS_DATA<29>	W10	D29	
32 9 MAXBUS_DATA<30>	U9	D30	
32 9 MAXBUS_DATA<31>	V9	D31	
32 9 MAXBUS_DATA<32>	W5	D32	
32 9 MAXBUS_DATA<33>	U6	D33	
32 9 MAXBUS_DATA<34>	T5	D34	
32 9 MAXBUS_DATA<35>	U5	D35	
32 9 MAXBUS_DATA<36>	W7	D36	
32 9 MAXBUS_DATA<37>	R6	D37	
32 9 MAXBUS_DATA<38>	P7	D38	
32 9 MAXBUS_DATA<39>	V6	D39	
32 9 MAXBUS_DATA<40>	P17	D40	
32 21 9 MAXBUS_DATA<41>	R19	D41	
32 21 9 MAXBUS_DATA<42>	V18	D42	
32 21 9 MAXBUS_DATA<43>	R18	D43	
32 21 9 MAXBUS_DATA<44>	V19	D44	
32 9 MAXBUS_DATA<45>	T19	D45	
32 9 MAXBUS_DATA<46>	U19	D46	
32 9 MAXBUS_DATA<47>	W19	D47	
32 9 MAXBUS_DATA<48>	U18	D48	
32 9 MAXBUS_DATA<49>	W17	D49	
32 9 MAXBUS_DATA<50>	W18	D50	
32 9 MAXBUS_DATA<51>	T16	D51	
32 9 MAXBUS_DATA<52>	T18	D52	
32 9 MAXBUS_DATA<53>	T17	D53	
32 21 9 MAXBUS_DATA<54>	W3	D54	
32 9 MAXBUS_DATA<55>	V17	D55	
32 9 MAXBUS_DATA<56>	U4	D56	
32 9 MAXBUS_DATA<57>	U8	D57	
32 9 MAXBUS_DATA<58>	U7	D58	
32 9 MAXBUS_DATA<59>	R7	D59	
32 9 MAXBUS_DATA<60>	P6	D60	
32 9 MAXBUS_DATA<61>	R8	D61	
32 21 9 MAXBUS_DATA<62>	W8	D62	
32 9 MAXBUS_DATA<63>	T8	D63	

DP0	T3	NC
DP1	W4	NC
DP2	T4	NC
DP3	W9	NC
DP4	M6	NC
DP5	V3	NC
DP6	N8	NC
DP7	W6	NC
DBG*	M2	MAXBUS_CPU0_DBG_L 6 32
DRDY*	R3	MAXBUS_CPU0_DRDY_L_R
DTI0	G1	MAXBUS_EDTI 33
DTI1	K1	MAXBUS_DTI<0> 9 32
DTI2	P1	MAXBUS_DTI<1> 9 32
DTI3	N1	MAXBUS_DTI<2> 9 32
TA*	K6	MAXBUS_TA_L 6 32
TEA*	L1	MAXBUS_TEA_L 6 32
HIT*	B2	MAXBUS_CPU0_HIT_L 6 32

OMIT
CRITICAL

R3600
0
5%
1/10W
MF-LF
402
PLACE RC GLITCH FILTER CLOSE TO CPU PIN

C3600
10PF
5%
50V
CERM
402

U3600
BGA
(1 OF 6)
XXGHZ-XXV
A8-X.X

32 6 MAXBUS_CPU0_BR_L	D2	BR*	
32 6 MAXBUS_CPU0_BG_L	M1	BG*	
32 6 MAXBUS_TS_L	L4	TS*	
CPU0_PULLDOWN	E11	A0	
	H1	A1	
	C11	A2	
	G3	A3	
32 9 MAXBUS_ADDR<0>	F10	A4	
32 9 MAXBUS_ADDR<1>	L2	A5	
32 9 MAXBUS_ADDR<2>	D11	A6	
32 9 MAXBUS_ADDR<3>	D1	A7	
32 9 MAXBUS_ADDR<4>	C10	A8	
32 9 MAXBUS_ADDR<5>	G2	A9	
32 9 MAXBUS_ADDR<6>	D12	A10	
32 9 MAXBUS_ADDR<7>	L3	A11	
32 9 MAXBUS_ADDR<8>	G4	A12	
32 9 MAXBUS_ADDR<9>	T2	A13	
32 9 MAXBUS_ADDR<10>	F4	A14	
32 9 MAXBUS_ADDR<11>	V1	A15	
32 9 MAXBUS_ADDR<12>	J4	A16	
32 9 MAXBUS_ADDR<13>	R2	A17	
32 9 MAXBUS_ADDR<14>	K5	A18	
32 9 MAXBUS_ADDR<15>	W2	A19	
32 9 MAXBUS_ADDR<16>	J2	A20	
32 9 MAXBUS_ADDR<17>	K4	A21	
32 9 MAXBUS_ADDR<18>	N4	A22	
32 9 MAXBUS_ADDR<19>	J3	A23	
32 9 MAXBUS_ADDR<20>	M5	A24	
32 9 MAXBUS_ADDR<21>	P5	A25	
32 9 MAXBUS_ADDR<22>	N3	A26	
32 9 MAXBUS_ADDR<23>	T1	A27	
32 9 MAXBUS_ADDR<24>	V2	A28	
32 9 MAXBUS_ADDR<25>	U1	A29	
32 9 MAXBUS_ADDR<26>	N5	A30	
32 9 MAXBUS_ADDR<27>	W1	A31	
32 9 MAXBUS_ADDR<28>	B12	A32	
32 9 MAXBUS_ADDR<29>	C4	A33	
32 9 MAXBUS_ADDR<30>	G10	A34	
32 9 MAXBUS_ADDR<31>	B11	A35	

R3601
470
5%
1/10W
MF-LF
402

OMIT
CRITICAL

AP0	C1	NC	
AP1	E3	NC	
AP2	H6	NC	
AP3	F5	NC	
AP4	G7	NC	
TT0	E5	MAXBUS_TT<0>	9 32
TT1	E6	MAXBUS_TT<1>	9 32
TT2	F6	MAXBUS_TT<2>	9 32
TT3	E9	MAXBUS_TT<3>	9 32
TT4	C5	MAXBUS_TT<4>	9 32
TBST*	F11	MAXBUS_TBST_L	9 32
TSIZ0	G6	MAXBUS_TSIZ<0>	9 32
TSIZ1	F7	MAXBUS_TSIZ<1>	9 32
TSIZ2	E7	MAXBUS_TSIZ<2>	9 32
GBL*	E2	MAXBUS_GBL_L	9 32
WT*	D3	MAXBUS_WT_L	9 32
CI*	J1	MAXBUS_CI_L	9 32
AACK*	R1	MAXBUS_AACK_L	6 32
ARTRY*	N2	MAXBUS_ARTRY_L	6 32
SHD0*	E4	MAXBUS_SHD0_L	33
SHD1*	H5	MAXBUS_SHD1_L	33
SYSCLK	A10	=MAXBUS_CPU0_CLK	11 33
CLK_OUT	H2	TP_CPU0_CLKOUT	ADD GND TP NEAR CLKOUT TP
TBEN	E1	MAXBUS_TBEN	21 32
QREQ*	P4	MAXBUS_CPU0_QREQ_L	32
QACK*	G5	MAXBUS_CPU0_QACK_L	32
CKSTP_IN*	A3		
CKSTP_OUT*	B1	CPU_CHKSTP_OUT_L	34

=PP1V5R1V8_MAXBUS 10 21 33 34

VIO DECOUPLING (28 PINS)

26 X 1UF (0402)
2 X 10UF (0603)

C3670 C3671 C3672 C3673 C3674 C3675 C3676 C3677 C3678 C3679
C3680 C3681 C3682 C3683 C3684 C3685 C3686 C3687 C3688 C3689
C3690 C3691 C3692 C3693 C3694 C3695
C3698 C3699

1uF 10% 6.3V CERM 402
10uF 20% 4V X5R 603

MAXBUS Straps

34 33 21 10 =PP1V5R1V8_MAXBUS

33 MAXBUS_SHD0_L — R3610 10K 5% 1/16W MF-LF 402
33 MAXBUS_SHD1_L — R3611 10K 1% 1/16W MF-LF 402
33 MAXBUS_EDTI — R3620 1K 1% 1/16W MF-LF 402

A8 MaxBus (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 36 OF 115	

Page Notes

Power aliases required by this page:
- =PP1V5R1V8_MAXBUS
- =PP3V3_PWRON_PLLSEL

Signal aliases required by this page:
- =CPU0_JTAG_TDI
- =CPU0_JTAG_TDO
- =CPU0_JTAG_TMS
- =CPU0_JTAG_TCK
- =CPU0_JTAG_TRST_L
- =CPU_HRESET_L (Reset given to all processors)

BOM options provided by this page:
- CPU0_PLL0_0/1
- CPU0_PLL1_0/1
- CPU0_PLL2_0/1
- CPU0_PLL3_0/1
- CPU0_PLL4_0/1
- CPU0_PLL5_0/1

These must be selected to set the CPU core to Maxbus frequency ratio to attain the desired spec
- MAXBUS_1V5 - MAXBUS_1V8
  One of these must be selected to set the Maxbus voltage
  * the MAXBUS_1V5 option does not exist for A7PM
- CPU_A7PM - CPU_A8
  One of these must be selected to ensure the the above strap is interpreted correctly

U3600

A7PM BGA (3 OF 6) XXGHZ-XXV A8-X.XX

34	CPU_BVSEL<0>	B7	BVSEL0	INT*	D4
34	CPU0_PLL_CFG<0>	B8	PLL_CFG0	SMI*	F9
34	CPU0_PLL_CFG<1>	C8	PLL_CFG1	MCP*	C9
34	CPU0_PLL_CFG<2>	C7	PLL_CFG2	SRESET*	A2
34	CPU0_PLL_CFG<3>	D7	PLL_CFG3	HRESET*	D8
34	CPU0_PLL_CFG<4>	A7	PLL_CFG4 CFGEXT A7PM	PMON_IN*	D9
9	=JTAG_CPU0_TDI	B9	TDI	PMON_OUT*	A9
9	=JTAG_CPU0_TDO	A4	TDO	BMODE0*	G9
9	=JTAG_CPU0_TMS	F1	TMS	BMODE1*	F8
9	=JTAG_CPU0_TCK	C6	TCK	EXT_QUAL	A11
9	=JTAG_CPU0_TRST_L	A5	TRST* OMIT		
34	CPU_LSSD_MODE_L	E8	LSSD_MODE* CRITICAL		
34	CPU0_L1TSTCLK	G8	L1_TSTCLK	DFS2*	A12
34	CPU0_L2TSTCLK	B3	L2_TSTCLK	LVRAM*	B10
			A7PM TEST0	BVSEL1	E10
			TEST2	DFS4*	B6
			TEST3	PLL_CFG5	D10
			TEST1	TEMP_ANODE	N18
			TEST4	TEMP_CATHODE	N19
				HPR_N	A6

6 32	MAXBUS_CPU0_INT_L		
34	CPU0_SMI_L		
34	CPU_MCP_L		
34	CPU0_SRESET_L		
11 34	=CPU_HRESET_L		
34	CPU_PMON_IN_L		
34	TP_CPU0_PMON_OUT_L		
34	CPU0_BMODE0_L		
34	CPU0_BMODE1_L		
34	TP_CPU0_EXT_QUAL		
34	CPU0_DFS2_L		
34	CPU0_LVRAM_L		
34	CPU0_BVSEL<1>		
34	CPU0_DFS4_L		
34	CPU0_PLL_CFG<5>		
34	TP_CPU0_TEMP_ANODE		
34	TP_CPU0_TEMP_CATHODE		
34	TP_CPU0_HPR_N		

CPU0 PLL CONFIG CIRCUITRY

34 33 21 10 =PP1V5R1V8_MAXBUS

CPU0_PLL0_1	R3720	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<0> 34
CPU0_PLL1_1	R3722	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<1> 34
CPU0_PLL2_1	R3724	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<2> 34
CPU0_PLL3_1	R3726	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<3> 34
CPU0_PLL4_1	R3728	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<4> 34
CPU0_PLL5_1	R3730	10K	5% 1/16W MF-LF 402	2	1	CPU0_PLL_CFG<5> 34
CPU0_PLL0_0	R3721	10K	5% 1/16W MF-LF 402	2	1	
CPU0_PLL1_0	R3723	10K	5% 1/16W MF-LF 402	2	1	
CPU0_PLL2_0	R3725	10K	5% 1/16W MF-LF 402	2	1	
CPU0_PLL3_0	R3727	10K	5% 1/16W MF-LF 402	2	1	
CPU0_PLL4_0	R3729	10K	5% 1/16W MF-LF 402	2	1	
CPU0_PLL5_0	R3731	10K	5% 1/16W MF-LF 402	2	1	

BUS TYPE SELECT

SIGNAL	TIED	MODE
CPU0_BMODE0_L (PROCESSOR)	HIGH	60X BUS MODE
	CPU_HRESET_L	MAX BUS MODE

34 CPU0_BMODE0_L — R3704 22 5% 1/16W MF-LF 402 — =CPU_HRESET_L 11 34

A7PM

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
2.5V INTERFACE	CPU_HRESET_L	OVDD
RESERVED(1.5V)	CPU_HRESET_INV	OVDD

A8

OVDD	BVSEL0	BVSEL1
1.8V INTERFACE	GND	GND
1.5V INTERFACE	OVDD	GND
RESERVED	CPU_HRESET_L	GND
RESERVED	CPU_HRESET_INV	GND
2.5V INTERFACE	GND	OVDD
2.5V INTERFACE	OVDD	OVDD
RESERVED	CPU_HRESET_L	OVDD
RESERVED	CPU_HRESET_INV	OVDD

MAXBUS VSEL

34 CPU_BVSEL<0> — MAXBUS_1V5 — R3703 10 5% 1/16W MF-LF 402 — =PP1V5R1V8_MAXBUS 10 21 33 34

MAXBUS_1V8 — R3702[1] 10 5% 1/16W MF-LF 402 2

(SPEC request this pull down resistor should less than 250 ohm)

34 CPU_BVSEL<1> — CPU_A7PM — R3705 10K 5% 1/16W MF-LF 402 — =PP1V5R1V8_MAXBUS 10 21 33 34

CPU_A8 — R3706[1] 1K 5% 1/16W MF-LF 402 2

CPU0 FREQUENCY CONFIGURATION

() Indicates DFS setting supported by A8 only

BOM GROUP	DFS SUPPORT F/2	DFS SUPPORT F/4	PLL BITS 012345	BOM OPTIONS
CPU0_BUSRATIO_1.0X	-	-	001100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_2.0X	-	-	010000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_3.0X	-	-	100000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_4.0X	2.0X	-	101000	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.0X	2.5X	-	101100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_5.5X	(2.75X)	-	100100	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.0X	3.0X	-	110100	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_6.5X	(3.25X)	-	010100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.0X	3.5X	-	001000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_7.5X	(3.75X)	-	000100	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.0X	4.0X	2.0X	110000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_8.5X	(4.25X)	-	011000	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_9.0X	4.5X	(2.25X)	011110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_9.5X	(4.75X)	-	011100	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_10.0X	5.0X	2.5X	101010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_10.5X	(5.25X)	-	100010	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.0X	5.5X	(2.75X)	100110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_11.5X	(5.75X)	-	000000	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_12.0X	6.0X	3.0X	101110	CPU0_PLL0_1,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_12.5X	(6.25X)	-	111110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.0X	6.5X	(3.25X)	010110	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_13.5X	(6.75X)	-	111000	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_0,CPU0_PLL5_0
CPU0_BUSRATIO_14.0X	7.0X	3.5X	110010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_15.0X	7.5X	(3.75X)	000110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_16.0X	8.0X	4.0X	110110	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_17.0X	8.5X	(4.25X)	000010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_18.0X	9.0X	4.5X	001010	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_20.0X	10.0X	5.0X	001110	CPU0_PLL0_0,CPU0_PLL1_0,CPU0_PLL2_1,CPU0_PLL3_1,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_21.0X	10.5X	(5.25X)	010010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_0,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_24.0X	12.0X	6.0X	011010	CPU0_PLL0_0,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0
CPU0_BUSRATIO_28.0X	14.0X	7.0X	111010	CPU0_PLL0_1,CPU0_PLL1_1,CPU0_PLL2_1,CPU0_PLL3_0,CPU0_PLL4_1,CPU0_PLL5_0

CPU PULLUPS

34 33 21 10 =PP1V5R1V8_MAXBUS

33 CPU_CHKSTP_OUT_L	R3752	10K	5% 1/16W MF-LF 402	
34 CPU_LSSD_MODE_L	R3753	10K	5% 1/16W MF-LF 402	
34 CPU_MCP_L	R3756	10K	5% 1/16W MF-LF 402	
34 CPU0_DFS2_L	R3765	10K	5% 1/16W MF-LF 402	
34 CPU0_LVRAM_L	R3766	10K	5% 1/16W MF-LF 402	
34 CPU0_DFS4_L	R3767	10K	5% 1/16W MF-LF 402	
34 CPU0_L2TSTCLK	R3759	10K	5% 1/16W MF-LF 402	
34 CPU_PMON_IN_L	R3758	10K	5% 1/16W MF-LF 402	
34 CPU0_BMODE1_L	R3707	1K	5% 1/16W MF-LF 402	
PID<0> SELECT				
34 11 =CPU_HRESET_L	R3757	10K	5% 1/16W MF-LF 402	

INTERRUPT PULL-UPS

34 33 21 10 =PP1V5R1V8_MAXBUS

34 CPU0_SMI_L	R3769	10K	5% 1/16W MF-LF 402	
34 CPU0_SRESET_L	R3771	10K	5% 1/16W MF-LF 402	

CPU PULLDOWNS

34 CPU0_L1TSTCLK — R3761 1K 5% 1/16W MF-LF 402

A8 Configuration Straps

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 37 OF 115

Page Notes

Power aliases required by this page:

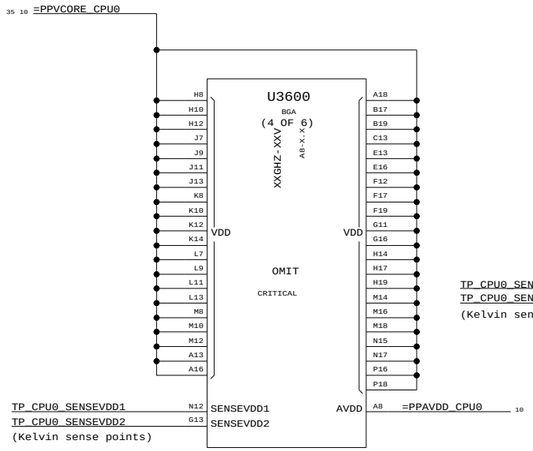
- =PPVCORE_CPU0

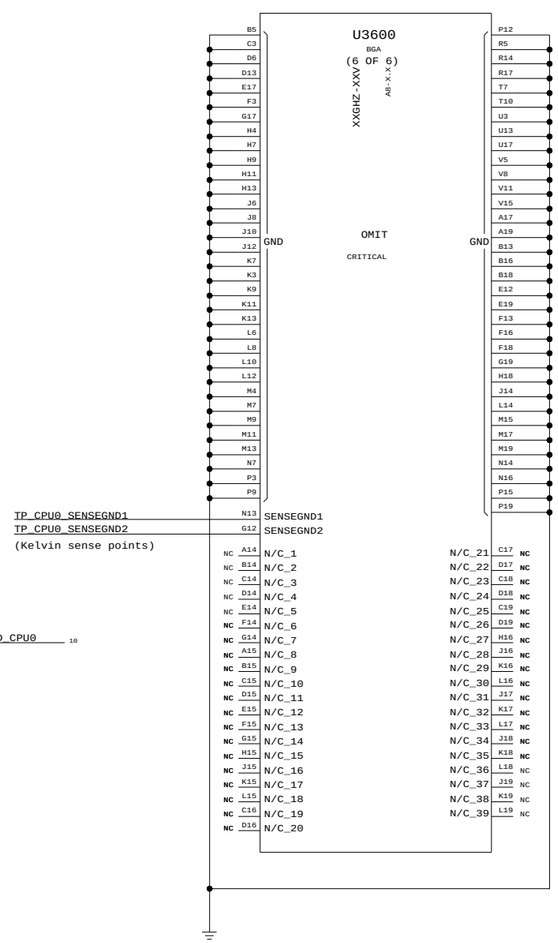
Signal aliases required by this page:

(NONE)

BOM options provided by this page:

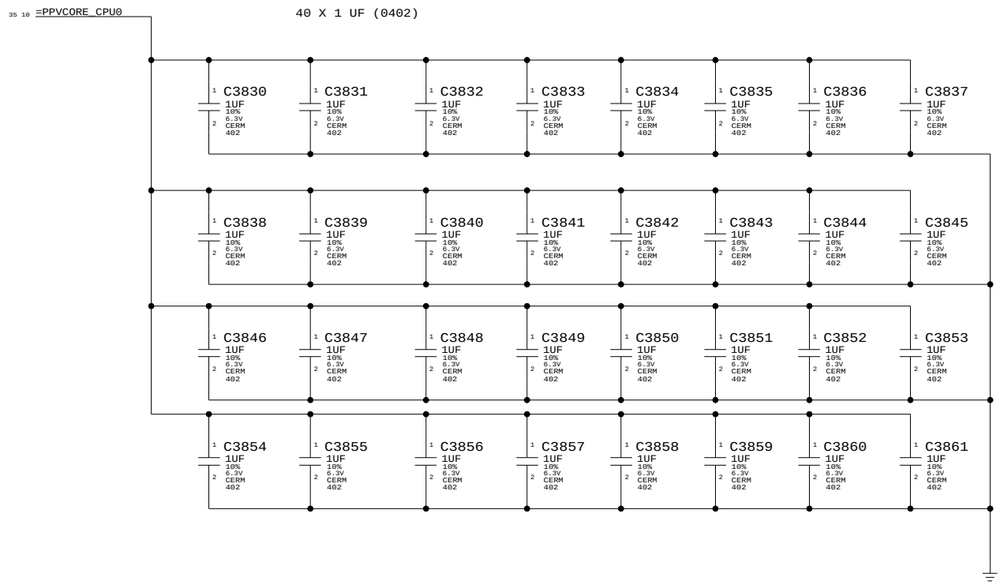
(NONE)



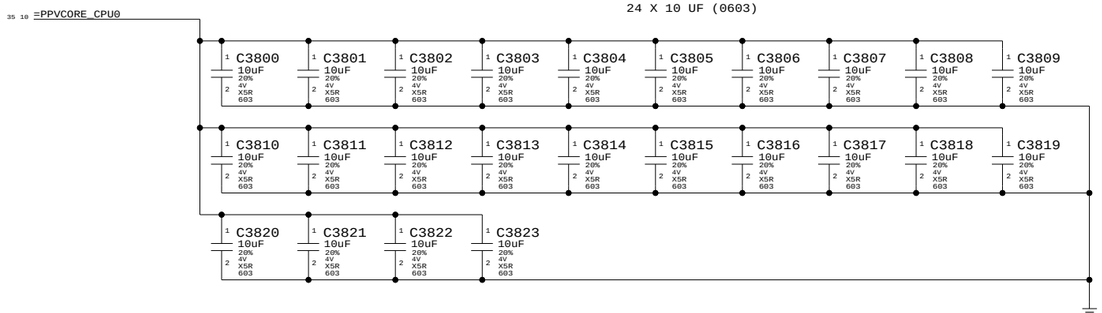


VCORE BULK CAPS

40 X 1 UF (0402)



24 X 10 UF (0603)



A8 Power (CPU0)

SYNC_MASTER=MULLET SYNC_DATE=05/25/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	38	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
14mil	THERM	THERM	
14mil	THERM	THERM	

VCORE_SNS 36
VCORE_GNDSNS 36

"Low" and "Mid" States

"High" State

36 10 =PP3V3_PWRON_CPUVCORE_VID

NO STUFF R3980 470K 5% 1/16W MF-LF 402 <D4>
R3982 470K 5% 1/16W MF-LF 402 <D3>
R3984 470K 5% 1/16W MF-LF 402 <D2>
R3986 0 5% 1/16W MF-LF 402 <D1>

VCORE_VID_A<1> 36
VCORE_VID_A<2> 36
VCORE_VID_A<3> 36
VCORE_VID_A<4> 36

NO STUFF R3981 470K 5% 1/16W MF-LF 402 <D4>
NO STUFF R3983 470K 5% 1/16W MF-LF 402 <D3>
NO STUFF R3985 470K 5% 1/16W MF-LF 402 <D2>
NO STUFF R3987 470K 5% 1/16W MF-LF 402 <D1>

NO STUFF R3970 470K 5% 1/16W MF-LF 402 <D4>
R3972 470K 5% 1/16W MF-LF 402 <D3>
R3974 470K 5% 1/16W MF-LF 402 <D2>
R3976 0 5% 1/16W MF-LF 402 <D1>

VCORE_VID_B<1> 36
VCORE_VID_B<2> 36
VCORE_VID_B<3> 36
VCORE_VID_B<4> 36

NO STUFF R3971 470K 5% 1/16W MF-LF 402 <D4>
NO STUFF R3973 470K 5% 1/16W MF-LF 402 <D3>
NO STUFF R3975 470K 5% 1/16W MF-LF 402 <D2>
NO STUFF R3977 470K 5% 1/16W MF-LF 402 <D1>

CPU_VCORE_3STATES
C3990 0.1UF 20% 10V CERM 402

CPU_VCORE_3STATES CRITICAL
U3990 PI3B3257 QSOP SYM_VER-2

36 VCORE_VID_A<1>	2	A1	Y1 4
36 VCORE_VID_B<1>	3	B1	
36 VCORE_VID_A<2>	5	A2	Y2 7
36 VCORE_VID_B<2>	6	B2	
36 VCORE_VID_A<3>	11	A3	Y3 9
36 VCORE_VID_B<3>	10	B3	
36 VCORE_VID_A<4>	14	A4	Y4 12
36 VCORE_VID_B<4>	13	B4	
11 =CPU0_VID_AB_SEL	1	SEL	
VID_MUX_OE_L	15	OE	
		GND	8
		VCC	16

VCORE_VID<1> 36
VCORE_VID<2> 36
VCORE_VID<3> 36
VCORE_VID<4> 36

CPU_VCORE_3STATES
R3990 1K 5% 1/16W MF-LF 402

Pullup on =CPU0_VID_AB_SEL will set default mux state to VID_B.

CPU_VCORE_2STATES
RP3990 0 5% 1/16W SM-LF

36 VCORE_VID_A<1>
36 VCORE_VID_A<2>
36 VCORE_VID_A<3>
36 VCORE_VID_A<4>

Keep trace fat (1.00-2.54 mm) and short!!

10 =PPVIN_CPUVCORE_MAX1717

CRITICAL C3940 8.2UF 20% 16V TANT CASE-D
CRITICAL C3941 8.2UF 20% 16V TANT CASE-D
CRITICAL C3942 8.2UF 20% 16V TANT CASE-D
CRITICAL C3943 8.2UF 20% 16V TANT CASE-D
CRITICAL C3944 8.2UF 20% 16V TANT CASE-D
CRITICAL C3945 8.2UF 20% 16V TANT CASE-D
CRITICAL C3946 8.2UF 20% 16V TANT CASE-D
CRITICAL C3947 8.2UF 20% 16V TANT CASE-D

10 =PP5V_PWRON_CPUVCORE_VDD

PLACE CLOSE TO TO PINS 15 & 13
D3901 SOD-123 B0530WXF
C3900 1UF 20% 10V CERM 603
VCORE_BOOST

10 =PP5V_PWRON_CPUVCORE_PWRSEQ
R3965 100K 1% 1/16W MF-LF 402
26 VCORE_CPU0_SHDN_L

R3960 0 5% 1/16W MF-LF 402
VCORE_VCC VOLTAGE=12.6V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
R3961 0 5% 1/16W MF-LF 402
C3960 1UF 20% 10V CERM 603

R3962 27.4K 1% 1/16W MF-LF 402
VCORE_ILIM

U3900 MAX1717 QSOP-LF

		VCC	15
		VDD	7
	2	SKP/SDN	
V+	1	FBS	5 (VCORE_SNS)
BST	22	ILIM	10 VCORE_BST2
DH	24	GNDS	11 (VCORE_GNDSNS)
		A/B	16
		REF	9
		TON	8
LX	23	CC	6
DL	14	D0	21
GND	13	D1	20
FB	4	D2	19
TIME	3	D3	18
VGATE	12	D4	17

CRITICAL

(VCORE_VPLUS) R3951 2.2 5% 1/16W MF-LF 603
VCORE_DH
C3951 0.1UF 20% 25V CERM 603
VCORE_LX
VCORE_DL
VCORE_GND VOLTAGE=0V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm
VCORE_FB
VCORE_TIME
=VCORE_PGOOD 26

NO STUFF C3902 0.0047uF 10% 25V CERM 402
CRITICAL Q3900 HAT2168H LFPAK
CRITICAL Q3902 HAT2160H LFPAK
CRITICAL Q3903 HAT2160H LFPAK
C3903 0.0022UF 10% 50V CERM 402

XW3910 SM
R3910 100 5% 1/16W MF-LF 402
XW3911 SM

R3950 390K 5% 1/16W MF-LF 402
C3950 0.001UF 20% 50V CERM 402

VCORE_GNDA VOLTAGE=0V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

Connect MAX1717 GND pin 13 to GND at bottom-side FET

XW3900 SM
CPUVCORE_VSENSE_R
Keep trace fat and short!!
Keep trace fat and short!!
CRITICAL R3900 0.001 1% 1W MF-LF 2512
=PPVCORE_CPU_REG 10

CRITICAL L3900 1.0UH-20.5 SM1
CRITICAL D3900 SWMINI SNM540XF
CPU_VCORE_SNUB
NO STUFF R3901 2.2 5% 1/4W MF-LF 1206
NO STUFF C3901 0.0022UF 10% 50V CERM 603

CRITICAL C3910 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3912 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3914 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3916 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3918 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3911 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3913 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3915 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF
CRITICAL C3917 330uF 20% 2.5V-ESR9V POLY CASE-D2E-LF

36 11 =CPU0_MAX1717_AB_SEL
36 10 =PP3V3_PWRON_CPUVCORE_VID
NO STUFF R3988 470K 5% 1/16W MF-LF 402 <D0>

MAX1717 VID CAN TAKE 3.3V TO 5.5V INPUTS

36 VCORE_VID<0>
36 VCORE_VID<1>
36 VCORE_VID<2>
36 VCORE_VID<3>
36 VCORE_VID<4>

MIN_LINE_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm
MIN_LINE_WIDTH=0.25 mm

R3989 0 5% 1/16W MF-LF 402
C3964 0.01UF 10% 16V CERM 402
R3964 66.5K 1% 1/16W MF-LF 402
R3963 12.7K 1% 1/16W MF-LF 402
C3962 1UF 20% 10V CERM 603
C3963 220PF 5% 25V CERM 402

VCORE_OFFSET_SW
R3943 100K 5% 1/16W MF-LF 402
10 =PP3V3_PWRON_CPUVCORE_OFFSET
VCORE_SEL_OFF_PU

NO STUFF R3940 0 5% 1/16W MF-LF 402
VCORE_SEL_ON
VCORE_OFFSET_SW
Q3940 2N7002DW-X-F SOT-363
VCORE_OFFSET_SW
R3941 0 5% 1/16W MF-LF 402
AB_SEL_LOW
VCORE_OFFSET_SW
Q3940 2N7002DW-X-F SOT-363
NO STUFF R3942 100K 5% 1/16W MF-LF 402

VCORE_OFFSET
R3944 6.04K 1% 1/16W MF-LF 402
R3945 162K 1% 1/16W MF-LF 603 R2
R3946 2.0K 1% 1/16W MF-LF 402 R1
VCORE_GNDDIV 36

GROUND SENSE VOLTAGE DIVIDER

This allows for an offset to the ground sense to adjust the output voltage.
VREF = 2.0V WITH A 0.85 SCALE FACTOR, HENCE VOFFSET = 1.7V * (R1/(R1+R2)) AND VCORE = VDAC + VOFFSET.

NOTE: R310 (R2) NO STUFFED FOR NO OFFSET CASE

ROUTE AS DIFFERENTIAL PAIR

1.67GHZ
(WITH VCORE OFFSET)
1.320V -> 0.990V
(CPU SPEC: 1.280V -> 0.980V)

OMIT R3998 2.05K 1% 1/16W MF-LF 402
36 VCORE_GNDDIV
OMIT R3999 100 1% 1/16W MF-LF 402
36 VCORE_GNDSNS

FMAX CONNECTOR

CRITICAL
OMIT J3999 M-ST-SM-52465-1217

VCORE_GNDDIV_TEST	1	12	VCORE_VID<0>
VCORE_GNDSNS_TEST	2	11	VCORE_VID<1> 36
SYS_RESET_BUTTON_L 25 24	3	10	VCORE_VID<2> 36
SYS_POWER_BUTTON_L 30 25 24	4	9	VCORE_VID<3> 36
NC (RFU)	5	8	VCORE_VID<4> 36
	6	7	

VCORE_GNDSNS VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.15 mm
VCORE_SNS VOLTAGE=1.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.15 mm

PLACE THIS SHORT AT PIN OF 1008UF CAP CLOSEST TO CPU
XW3901 SM

Keep trace fat and short!!

OUTPUT VOLTAGE

VDAC D4=0	VDAC D4=1	D3	D2	D1	D0 36 21 =CPU0_MAX1717_AB_SEL
2.00	1.275	0	0	0	0
1.95	1.250	0	0	0	1
1.90	1.225	0	0	1	0
1.85	1.200	0	0	1	1
1.80	1.175	0	1	0	0
1.75	1.150	0	1	0	1
1.70	1.125	0	1	1	0
1.65	1.100	0	1	1	1
1.60	1.075	1	0	0	0
1.55	1.050	1	0	0	1
1.50	1.025	1	0	1	0
1.45	1.000	1	0	1	1
1.40	0.975	1	1	0	0
1.35	0.950	1	1	0	1
1.30	0.925	1	1	1	0
NO CPU	NO CPU	1	1	1	1

FOR V-STEP:

D<4..0>	A/B_ = Hi/Fast	A/B_ = Lo/Slow
<= 1K PU	1	0
>= 100K PU	1	1
>= 100K PD	0	1
<= 1K PD	0	0

When A/B_ is high (fast): D4-D0 read as-is
When A/B_ is low (slow): <=1K-ohm -> 0
>=100K-ohm -> 1

If all pull-ups are >=100K and all pull-downs are <=1K, $V_A = V_B$.

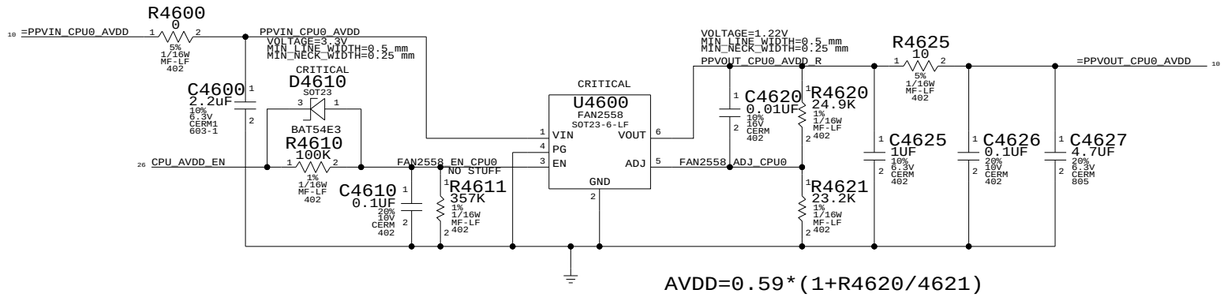
CPU VCore Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 39 OF 115	

CPU PLL POWER SUPPLY



AVDD=0.59*(1+R4620/4621)

CPU AVDD Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	46	115

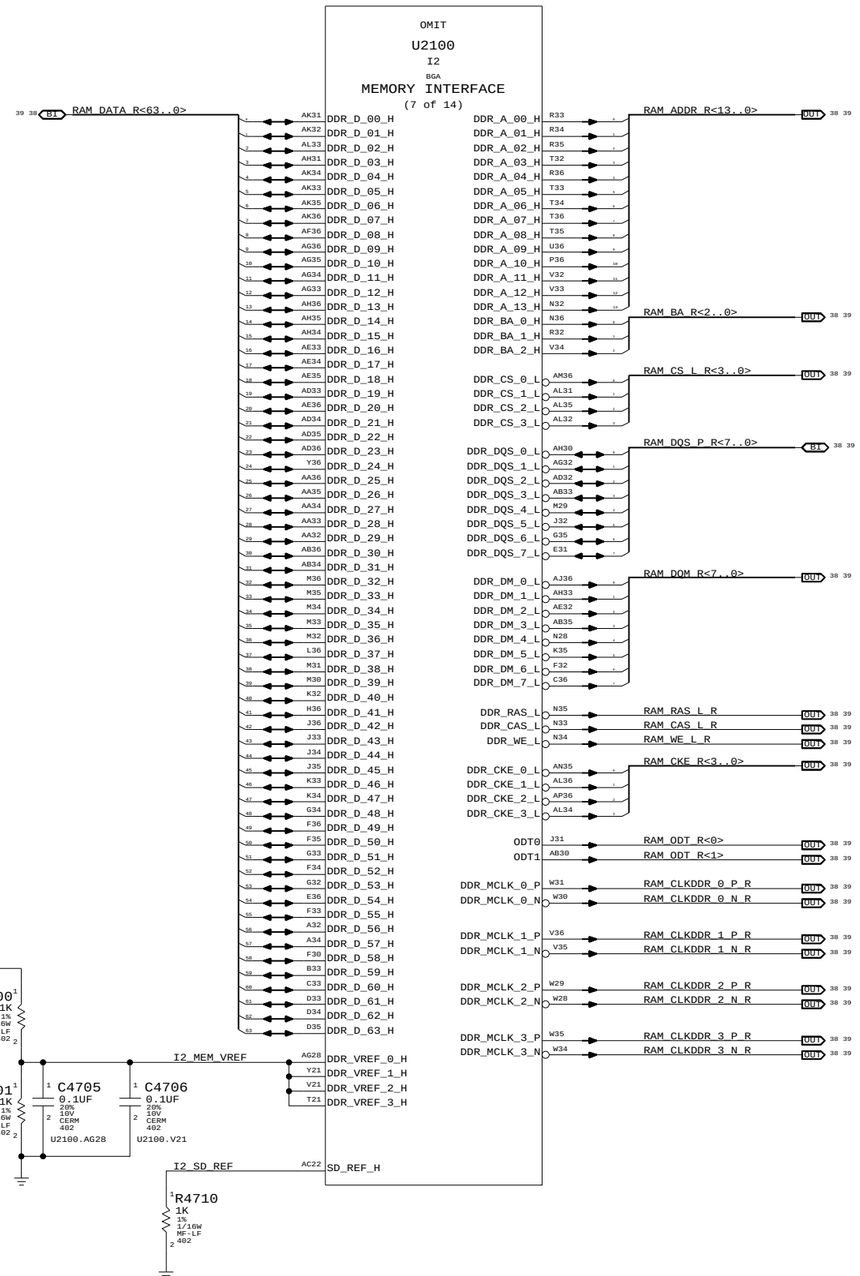
NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_P_R 38 39
RAM_CLK_0	RAM_DIFF	RAM_DIFF	RAM_CLK_0_R	RAM_CLKDDR_0_N_R 38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_P_R 38 39
RAM_CLK_1	RAM_DIFF	RAM_DIFF	RAM_CLK_1_R	RAM_CLKDDR_1_N_R 38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_P_R 38 39
RAM_CLK_2	RAM_DIFF	RAM_DIFF	RAM_CLK_2_R	RAM_CLKDDR_2_N_R 38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_P_R 38 39
RAM_CLK_3	RAM_DIFF	RAM_DIFF	RAM_CLK_3_R	RAM_CLKDDR_3_N_R 38 39
RAM_CKE_0	RAM	RAM		RAM_CKE_R<1..0> 38 39
RAM_CKE_1	RAM	RAM		RAM_CKE_R<3..2> 38 39
RAM_CS_0	RAM	RAM		RAM_CS_L_R<1..0> 38 39
RAM_CS_1	RAM	RAM		RAM_CS_L_R<3..2> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_ADDR_R<13..0> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_BA_R<2..0> 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_RAS_L_R 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_CAS_L_R 38 39
RAM_ADDR_CTL	RAM	RAM		RAM_WE_L_R 38 39
RAM_ODT0	RAM	RAM		RAM_ODT_R<0> 38 39
RAM_ODT1	RAM	RAM		RAM_ODT_R<1> 38 39
RAM_DQS0	RAM	RAM		RAM_DQS_P_R<0> 38 39
RAM_DQS1	RAM	RAM		RAM_DQS_P_R<1> 38 39
RAM_DQS2	RAM	RAM		RAM_DQS_P_R<2> 38 39
RAM_DQS3	RAM	RAM		RAM_DQS_P_R<3> 38 39
RAM_DQS4	RAM	RAM		RAM_DQS_P_R<4> 38 39
RAM_DQS5	RAM	RAM		RAM_DQS_P_R<5> 38 39
RAM_DQS6	RAM	RAM		RAM_DQS_P_R<6> 38 39
RAM_DQS7	RAM	RAM		RAM_DQS_P_R<7> 38 39
RAM_DQM0	RAM	RAM		RAM_DQM_R<0> 38 39
RAM_DQM1	RAM	RAM		RAM_DQM_R<1> 38 39
RAM_DQM2	RAM	RAM		RAM_DQM_R<2> 38 39
RAM_DQM3	RAM	RAM		RAM_DQM_R<3> 38 39
RAM_DQM4	RAM	RAM		RAM_DQM_R<4> 38 39
RAM_DQM5	RAM	RAM		RAM_DQM_R<5> 38 39
RAM_DQM6	RAM	RAM		RAM_DQM_R<6> 38 39
RAM_DQM7	RAM	RAM		RAM_DQM_R<7> 38 39
RAM_DATA_0	RAM	RAM		RAM_DATA_R<7..0> 38 39
RAM_DATA_1	RAM	RAM		RAM_DATA_R<15..8> 38 39
RAM_DATA_2	RAM	RAM		RAM_DATA_R<23..16> 38 39
RAM_DATA_3	RAM	RAM		RAM_DATA_R<31..24> 38 39
RAM_DATA_4	RAM	RAM		RAM_DATA_R<39..32> 38 39
RAM_DATA_5	RAM	RAM		RAM_DATA_R<47..40> 38 39
RAM_DATA_6	RAM	RAM		RAM_DATA_R<55..48> 38 39
RAM_DATA_7	RAM	RAM		RAM_DATA_R<63..56> 38 39

Page Notes

Power aliases required by this page:
- =PP1V8_PWRON_I2_RAM
- =PP1V8_RAM_I2_VREF

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 Memory Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 47 OF 115	

Main Memory Series Termination

SERIES RESISTORS FOR CONTROL SIGNALS

PINS ARE SWAPPABLE FOR RPAKS RP4800-RP4804

RAM_ADDR_R<0> — RP4800 pin 3 — 22 — 5% 1/16W SM-LF — pin 6 — RAM_ADDR<0>
RAM_ADDR_R<1> — RP4803 pin 2 — 22 — 5% 1/16W SM-LF — pin 7 — RAM_ADDR<1>
RAM_ADDR_R<2> — RP4803 pin 4 — 22 — 5% 1/16W SM-LF — pin 5 — RAM_ADDR<2>
RAM_ADDR_R<3> — RP4803 pin 1 — 22 — 5% 1/16W SM-LF — pin 8 — RAM_ADDR<3>
RAM_ADDR_R<4> — RP4803 pin 3 — 22 — 5% 1/16W SM-LF — pin 6 — RAM_ADDR<4>
RAM_ADDR_R<5> — RP4801 pin 4 — 22 — 5% 1/16W SM-LF — pin 5 — RAM_ADDR<5>
RAM_ADDR_R<6> — RP4802 pin 1 — 22 — 5% 1/16W SM-LF — pin 8 — RAM_ADDR<6>
RAM_ADDR_R<7> — RP4802 pin 4 — 22 — 5% 1/16W SM-LF — pin 5 — RAM_ADDR<7>
RAM_ADDR_R<8> — RP4802 pin 3 — 22 — 5% 1/16W SM-LF — pin 6 — RAM_ADDR<8>
RAM_ADDR_R<9> — RP4802 pin 2 — 22 — 5% 1/16W SM-LF — pin 7 — RAM_ADDR<9>
RAM_ADDR_R<10> — RP4800 pin 2 — 22 — 5% 1/16W SM-LF — pin 7 — RAM_ADDR<10>
RAM_ADDR_R<11> — RP4801 pin 3 — 22 — 5% 1/16W SM-LF — pin 6 — RAM_ADDR<11>
RAM_ADDR_R<12> — RP4801 pin 2 — 22 — 5% 1/16W SM-LF — pin 7 — RAM_ADDR<12>
RAM_ADDR_R<13> — RP4804 pin 4 — 22 — 5% 1/16W SM-LF — pin 5 — RAM_ADDR<13>

RAM_BA_R<0> — RP4800 pin 1 — 22 — 5% 1/16W SM-LF — pin 8 — RAM_BA<0>
RAM_BA_R<1> — RP4800 pin 4 — 22 — 5% 1/16W SM-LF — pin 5 — RAM_BA<1>
RAM_BA_R<2> — RP4801 pin 1 — 22 — 5% 1/16W SM-LF — pin 8 — RAM_BA<2>

RAM_RAS_L_R — RP4804 pin 1 — 22 — 5% 1/16W SM-LF — pin 8 — RAM_RAS_L
RAM_CAS_L_R — RP4804 pin 3 — 22 — 5% 1/16W SM-LF — pin 6 — RAM_CAS_L
RAM_WE_L_R — RP4804 pin 2 — 22 — 5% 1/16W SM-LF — pin 7 — RAM_WE_L

RAM_ODT_R<0> — R4810 — 0 — 5% 1/16W MF-LF 402 — RAM_ODT<0>
RAM_ODT_R<1> — R4811 — 0 — 5% 1/16W MF-LF 402 — RAM_ODT<1>

SERIES RESISTORS FOR CLOCKS

RAM_CLKDDR_0_P_R — R4850 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_0_P
RAM_CLKDDR_0_N_R — R4851 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_0_N
RAM_CLKDDR_1_P_R — R4855 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_1_P
RAM_CLKDDR_1_N_R — R4856 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_1_N
RAM_CLKDDR_2_P_R — R4860 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_2_P
RAM_CLKDDR_2_N_R — R4861 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_2_N
RAM_CLKDDR_3_P_R — R4865 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_3_P
RAM_CLKDDR_3_N_R — R4866 — 22 — 5% 1/10W MF-LF 402 — RAM_CLKDDR_3_N

SERIES RESISTORS FOR CS / CKE
Do not swap with other RPAKs

RAM_CS_L_R<0> — RP4870 pin 1 — 22 — 5% 1/16W SM-LF — pin 4 — RAM_CS_L<0>
RAM_CS_L_R<2> — RP4870 pin 2 — 22 — 5% 1/16W SM-LF — pin 3 — RAM_CS_L<2>
RAM_CS_L_R<1> — RP4871 pin 1 — 22 — 5% 1/16W SM-LF — pin 4 — RAM_CS_L<1>
RAM_CS_L_R<3> — RP4871 pin 2 — 22 — 5% 1/16W SM-LF — pin 3 — RAM_CS_L<3>
RAM_CKE_R<0> — RP4875 pin 1 — 22 — 5% 1/16W SM-LF — pin 4 — RAM_CKE<0>
RAM_CKE_R<2> — RP4875 pin 2 — 22 — 5% 1/16W SM-LF — pin 3 — RAM_CKE<2>
RAM_CKE_R<1> — RP4876 pin 1 — 22 — 5% 1/16W SM-LF — pin 4 — RAM_CKE<1>
RAM_CKE_R<3> — RP4876 pin 2 — 22 — 5% 1/16W SM-LF — pin 3 — RAM_CKE<3>

RAM_DATA_R<63..0> — RAM_DATA<63..0> MAKE_BASE=TRUE — RAM_DATA_A<63..0> / RAM_DATA_B<63..0>
RAM_DQM_R<7..0> — RAM_DQM<7..0> MAKE_BASE=TRUE — RAM_DQM_A<7..0> / RAM_DQM_B<7..0>
RAM_DQS_P_R<7..0> — RAM_DQS<7..0> MAKE_BASE=TRUE — RAM_DQS_A_P<7..0> / RAM_DQS_B_P<7..0>

RP4872 (10K 5% 1/16W SM-LF):
RAM_DQS_A_N<3> — RAM_DQS_B_N<3> — RAM_DQS_A_N<2> — RAM_DQS_B_N<2>

RP4873 (10K 5% 1/16W SM-LF):
RAM_DQS_B_N<5> — RAM_DQS_A_N<5> — RAM_DQS_B_N<4> — RAM_DQS_A_N<4>

RP4877 (10K 5% 1/16W SM-LF):
RAM_DQS_B_N<1> — RAM_DQS_A_N<1> — RAM_DQS_A_N<0> — RAM_DQS_B_N<0>

RP4878 (10K 5% 1/16W SM-LF):
RAM_DQS_B_N<7> — RAM_DQS_A_N<7> — RAM_DQS_B_N<6> — RAM_DQS_A_N<6>

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
T199	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_P
T194	RAM_DIFF	RAM_DIFF	RAM_CLK_0	RAM_CLKDDR_0_N
T195	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_P
T193	RAM_DIFF	RAM_DIFF	RAM_CLK_1	RAM_CLKDDR_1_N
T197	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_P
T196	RAM_DIFF	RAM_DIFF	RAM_CLK_2	RAM_CLKDDR_2_N
T198	RAM_DIFF	RAM_DIFF	RAM_CLK_3	RAM_CLKDDR_3_P
T200	RAM_DIFF	RAM_DIFF	RAM_CLK_4	RAM_CLKDDR_3_N
T205	RAM	RAM		RAM_CKE<3..0>
T204	RAM	RAM		RAM_CS_L<3..0>
T203	RAM	RAM		RAM_ADDR<13..0>
T202	RAM	RAM		RAM_BA<2..0>
T201	RAM	RAM		RAM_RAS_L
T208	RAM	RAM		RAM_CAS_L
T207	RAM	RAM		RAM_WE_L
T259	RAM	RAM		RAM_ODT<1..0>
T209	RAM	RAM		RAM_DQS<7..0>
T206	RAM	RAM		RAM_DQM<7..0>
T210	RAM	RAM		RAM_DATA<63..0>

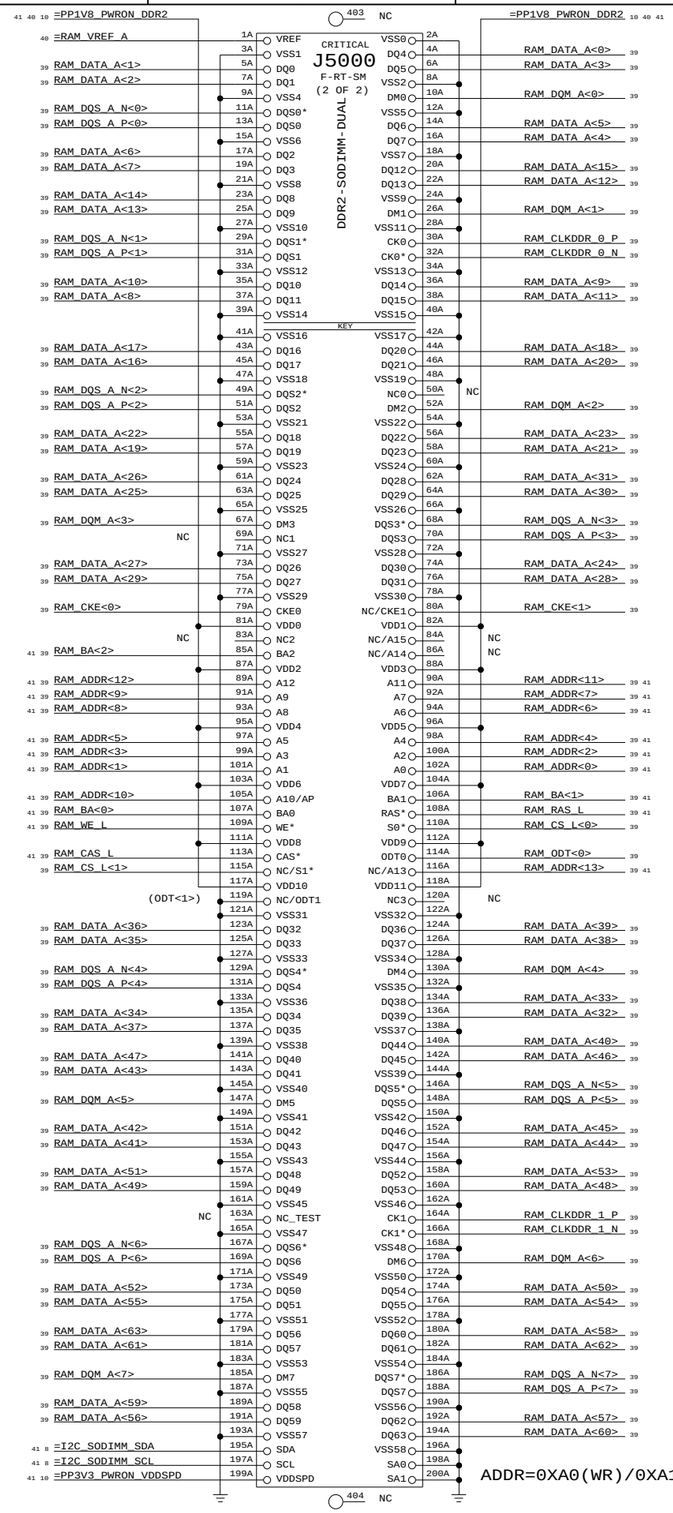
ECSETs provided by memory controller.

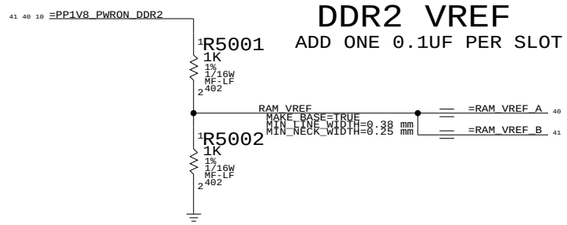
Memory Series Termination		
SYNC_MASTER=N/A	SYNC_DATE=N/A	

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 48 OF 115	

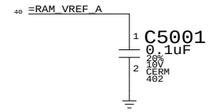
SLOT "A"
LOWER SLOT
FACTORY SLOT



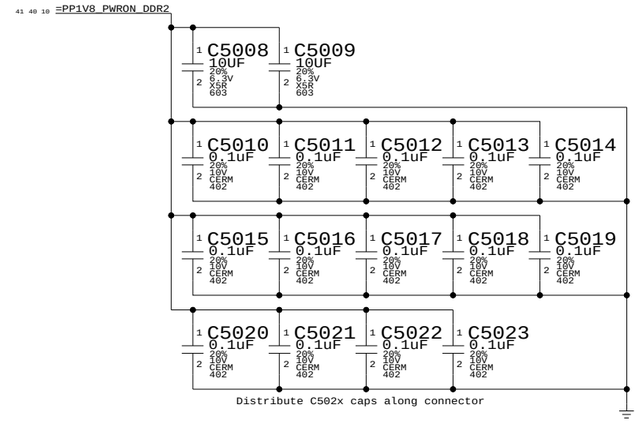


DDR2 VREF
ADD ONE 0.1UF PER SLOT

DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "A"



Distribute C502x caps along connector

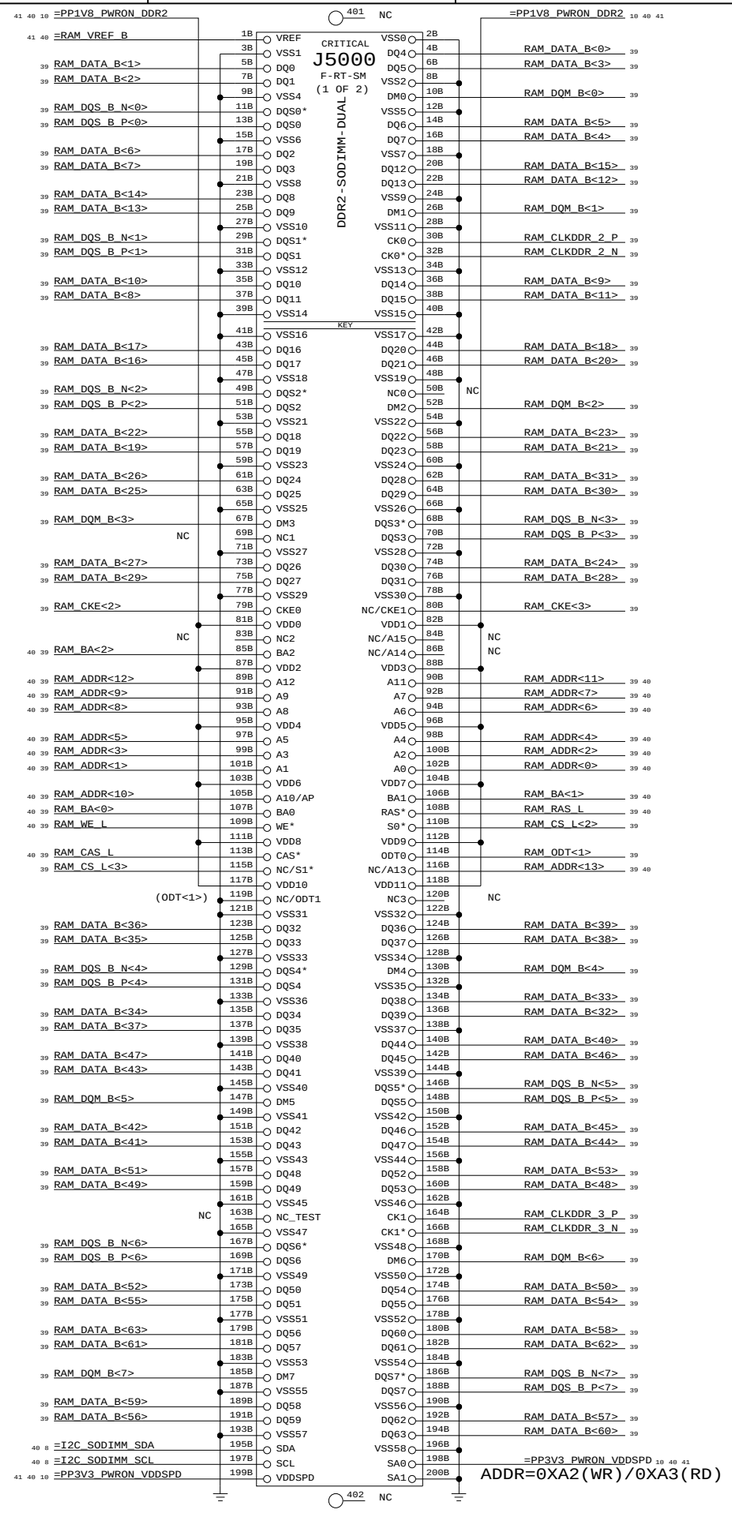
DDR2 SO-DIMM Slot A

SYNC_MASTER=N/A SYNC_DATE=N/A

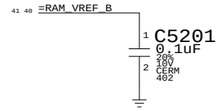
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 50 OF 115	

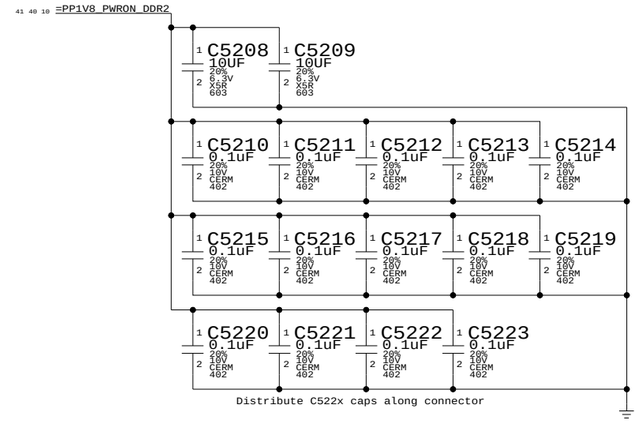
SLOT "B"
UPPER SLOT
CUSTOMER SLOT



DDR2 VREF
ONE 0.1UF PER SLOT



DDR2 BYPASS
SLOT "B"



Distribute C522x caps along connector

DDR2 SO-DIMM Slot B

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 52 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_A_CLK_0	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_0_R	FB_A_CLKDDR_0_N_R 48
FB_A_CLK_1	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_A_CLK_1_R	FB_A_CLKDDR_1_N_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CKE_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_ADDR_R<12..0> 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_BA_R<2..0> 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_RAS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_CAS_L_R 48
FB_A_ADDR_CTL	RAM	RAM		FB_A_WE_L_R 48
FB_A_DQS0	RAM	RAM		FB_A_DQS_R<0> 48
FB_A_DQS1	RAM	RAM		FB_A_DQS_R<1> 48
FB_A_DQS2	RAM	RAM		FB_A_DQS_R<2> 48
FB_A_DQS3	RAM	RAM		FB_A_DQS_R<3> 48
FB_A_DQS4	RAM	RAM		FB_A_DQS_R<4> 48
FB_A_DQS5	RAM	RAM		FB_A_DQS_R<5> 48
FB_A_DQS6	RAM	RAM		FB_A_DQS_R<6> 48
FB_A_DQS7	RAM	RAM		FB_A_DQS_R<7> 48
FB_A_DQM0	RAM	RAM		FB_A_DQM_R<0> 48
FB_A_DQM1	RAM	RAM		FB_A_DQM_R<1> 48
FB_A_DQM2	RAM	RAM		FB_A_DQM_R<2> 48
FB_A_DQM3	RAM	RAM		FB_A_DQM_R<3> 48
FB_A_DQM4	RAM	RAM		FB_A_DQM_R<4> 48
FB_A_DQM5	RAM	RAM		FB_A_DQM_R<5> 48
FB_A_DQM6	RAM	RAM		FB_A_DQM_R<6> 48
FB_A_DQM7	RAM	RAM		FB_A_DQM_R<7> 48
FB_A_DQ0	RAM	RAM		FB_A_DQ_R<7..0> 48
FB_A_DQ1	RAM	RAM		FB_A_DQ_R<15..8> 48
FB_A_DQ2	RAM	RAM		FB_A_DQ_R<23..16> 48
FB_A_DQ3	RAM	RAM		FB_A_DQ_R<31..24> 48
FB_A_DQ4	RAM	RAM		FB_A_DQ_R<39..32> 48
FB_A_DQ5	RAM	RAM		FB_A_DQ_R<47..40> 48
FB_A_DQ6	RAM	RAM		FB_A_DQ_R<55..48> 48
FB_A_DQ7	RAM	RAM		FB_A_DQ_R<63..56> 48

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
FB_B_CLK_0	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_0_R	FB_B_CLKDDR_0_N_R 48
FB_B_CLK_1	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_P_R 48
(provided above)	RAM_DIFF	RAM_DIFF	FB_B_CLK_1_R	FB_B_CLKDDR_1_N_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CKE_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_ADDR_R<12..0> 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_BA_R<2..0> 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_RAS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_CAS_L_R 48
FB_B_ADDR_CTL	RAM	RAM		FB_B_WE_L_R 48
FB_B_DQS0	RAM	RAM		FB_B_DQS_R<0> 48
FB_B_DQS1	RAM	RAM		FB_B_DQS_R<1> 48
FB_B_DQS2	RAM	RAM		FB_B_DQS_R<2> 48
FB_B_DQS3	RAM	RAM		FB_B_DQS_R<3> 48
FB_B_DQS4	RAM	RAM		FB_B_DQS_R<4> 48
FB_B_DQS5	RAM	RAM		FB_B_DQS_R<5> 48
FB_B_DQS6	RAM	RAM		FB_B_DQS_R<6> 48
FB_B_DQS7	RAM	RAM		FB_B_DQS_R<7> 48
FB_B_DQM0	RAM	RAM		FB_B_DQM_R<0> 48
FB_B_DQM1	RAM	RAM		FB_B_DQM_R<1> 48
FB_B_DQM2	RAM	RAM		FB_B_DQM_R<2> 48
FB_B_DQM3	RAM	RAM		FB_B_DQM_R<3> 48
FB_B_DQM4	RAM	RAM		FB_B_DQM_R<4> 48
FB_B_DQM5	RAM	RAM		FB_B_DQM_R<5> 48
FB_B_DQM6	RAM	RAM		FB_B_DQM_R<6> 48
FB_B_DQM7	RAM	RAM		FB_B_DQM_R<7> 48
FB_B_DQ0	RAM	RAM		FB_B_DQ_R<7..0> 48
FB_B_DQ1	RAM	RAM		FB_B_DQ_R<15..8> 48
FB_B_DQ2	RAM	RAM		FB_B_DQ_R<23..16> 48
FB_B_DQ3	RAM	RAM		FB_B_DQ_R<31..24> 48
FB_B_DQ4	RAM	RAM		FB_B_DQ_R<39..32> 48
FB_B_DQ5	RAM	RAM		FB_B_DQ_R<47..40> 48
FB_B_DQ6	RAM	RAM		FB_B_DQ_R<55..48> 48
FB_B_DQ7	RAM	RAM		FB_B_DQ_R<63..56> 48

M11 Frame Buffer Constraints

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE NONE SHT 55 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
AGP_CLK	CLOCK	CLOCK	
I2_AGP_FBCLK	I2_FBCLK	I2_FBCLK	
I2_FBCLK	I2_FBCLK	I2_FBCLK	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_0	AGP	AGP	
AGP_AD_1	AGP	AGP	
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0
AGP_AD_STB_0	AGP_STB	AGP_STB	AGP_AD_STB0
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1
AGP_AD_STB_1	AGP_STB	AGP_STB	AGP_AD_STB1
AGP_SBA	AGP	AGP	
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB
AGP_SB_STB	AGP_STB	AGP_STB	AGP_SB_STB
AGP_ST	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_CTL	AGP	AGP	
AGP_PAR	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
AGP_DEV_CTL	AGP	AGP	
	AGP	AGP	
	AGP	AGP	

AGP_CLK66M_GPU_R 11 43
I2_AGP_FBCLK_OUT_R 43
I2_AGP_FBCLK_OUT 21 43
AGP_AD<15..0> 43 44
AGP_AD<31..16> 43 44
AGP_CBE_L<1..0> 43 44
AGP_CBE_L<3..2> 43 44
AGP_AD_STB0_P 43 44
AGP_AD_STB0_N 43 44
AGP_AD_STB1_P 43 44
AGP_AD_STB1_N 43 44
AGP_SBA<7..0> 43 44
AGP_SB_STB_P 43 44
AGP_SB_STB_N 43 44
AGP_ST<3..0> 43 44
AGP_FRAME_L 6 43 44
AGP_DEVSEL_L 6 43 44
AGP_IRDY_L 6 43 44
AGP_TRDY_L 6 43 44
AGP_STOP_L 6 43 44
AGP_PAR 43 44
AGP_PIPE_L 43
AGP_WBF_L 43 44
AGP_RBF_L 6 43 44
AGP_REQ_L 6 43 44
AGP_GNT_L 6 43 44

Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP
- =PP1V5_I2_AGP

Signal aliases required by this page:
- =I2_AGP_VREF - VRef from graphics card or on-board graphics controller
- =I2_AGP_FBCLK_IN - AGP feedback clock input. Length should match that of clock from I2 to AGP device.

BOM options provided by this page:
(NONE)

NOTE: I2 implements an AGP 4x bridge. AGP 8x signals are not provided by this page.

AGP I/O DECOUPLING

(25 Balls on I2)

10 =PP1V5_I2_AGP

C5649 10UF 20% 6.3V XSR 603

C5650 C5651 C5652 C5653 C5654 C5655 C5656
C5657 C5658 C5659 C5660 C5661 C5662 C5663
C5664 C5665 C5666 C5667 C5668 C5669 C5670
C5671 C5672 C5673 C5674

1uF 10% 6.3V CERM 402

1 X 10uF (0603)
25 X 1uF (0402)

OMIT
U2100
I2
BGA
AGP INTERFACE
(9 of 14)

(3.3V SIGNALS)

(VDDAGP SIGNALS)

44 43 AGP_BUSY_L	AP19	AGP_BUSY_L	AGP_CLK_H	AH19	AGP_CLK66M_GPU_R 11 43
44 43 6 AGP_REQ_L	AR19	AGP_REQ_L	AGP_STP_L	AT21	STOP_AGP_L 43 44
44 43 AGP_PAR	AT15	AGP_PAR_H	AGP_GNT_L	AL16	AGP_GNT_L 6 43 44
44 43 6 AGP_FRAME_L	AK16	AGP_FRAME_L	AGP_AD_00_H	AP6	AGP_AD<0> 43 44
44 43 6 AGP_TRDY_L	AM16	AGP_TRDY_L	AGP_AD_01_H	AP4	AGP_AD<1> 43 44
44 43 6 AGP_IRDY_L	AR15	AGP_IRDY_L	AGP_AD_02_H	AR4	AGP_AD<2> 43 44
44 43 6 AGP_STOP_L	AT14	AGP_STOP_L	AGP_AD_03_H	AT5	AGP_AD<3> 43 44
44 43 6 AGP_DEVSEL_L	AP15	AGP_DEVSEL_L	AGP_AD_04_H	AN7	AGP_AD<4> 43 44
43 AGP_PIPE_L	AN19	AGP_PIPE_L	AGP_AD_05_H	AL13	AGP_AD<5> 43 44
44 43 AGP_WBF_L	AT18	AGP_WBF_L	AGP_AD_06_H	AR6	AGP_AD<6> 43 44
44 43 6 AGP_RBF_L	AM19	AGP_RBF_L	AGP_AD_07_H	AT6	AGP_AD<7> 43 44
			AGP_CBE_0_L	AT3	AGP_CBE_L<0> 43 44
44 43 AGP_SBA<0>	AL18	AGP_SBA_0_H	AGP_AD_08_H	AN9	AGP_AD<8> 43 44
44 43 AGP_SBA<1>	AR18	AGP_SBA_1_H	AGP_AD_09_H	AP7	AGP_AD<9> 43 44
44 43 AGP_SBA<2>	AP18	AGP_SBA_2_H	AGP_AD_10_H	AR7	AGP_AD<10> 43 44
44 43 AGP_SBA<3>	AN18	AGP_SBA_3_H	AGP_AD_11_H	AT7	AGP_AD<11> 43 44
44 43 AGP_SBA<4>	AM18	AGP_SBA_4_H	AGP_AD_12_H	AN10	AGP_AD<12> 43 44
44 43 AGP_SBA<5>	AK18	AGP_SBA_5_H	AGP_AD_13_H	AR9	AGP_AD<13> 43 44
44 43 AGP_SBA<6>	AT16	AGP_SBA_6_H	AGP_AD_14_H	AT8	AGP_AD<14> 43 44
44 43 AGP_SBA<7>	AT17	AGP_SBA_7_H	AGP_AD_15_H	AT9	AGP_AD<15> 43 44
			AGP_CBE_1_L	AP9	AGP_CBE_L<1> 43 44
44 43 AGP_SB_STB_P	AH16	AGP_SB_STB_P	AGP_AD_STB0_P	AH9	AGP_AD_STB0_P 43 44
44 43 AGP_SB_STB_N	AJ16	AGP_SB_STB_N	AGP_AD_STB0_N	AJ9	AGP_AD_STB0_N 43 44
	AD15	VDDAGP_0	AGP_AD_16_H	AM12	AGP_AD<16> 43 44
	AD17	VDDAGP_1	AGP_AD_17_H	AP10	AGP_AD<17> 43 44
	AD19	VDDAGP_2	AGP_AD_18_H	AN12	AGP_AD<18> 43 44
	AE13	VDDAGP_3	AGP_AD_19_H	AT10	AGP_AD<19> 43 44
	AE16	VDDAGP_4	AGP_AD_20_H	AK15	AGP_AD<20> 43 44
	AE18	VDDAGP_5	AGP_AD_21_H	AM13	AGP_AD<21> 43 44
	AF14	VDDAGP_6	AGP_AD_22_H	AP12	AGP_AD<22> 43 44
	AG13	VDDAGP_7	AGP_AD_23_H	AT11	AGP_AD<23> 43 44
	AG16	VDDAGP_8	AGP_CBE_2_L	AR10	AGP_CBE_L<2> 43 44
	AH11	VDDAGP_9			
	AH13	VDDAGP_10	AGP_AD_24_H	AL15	AGP_AD<24> 43 44
	AL11	VDDAGP_11	AGP_AD_25_H	AN13	AGP_AD<25> 43 44
	AL12	VDDAGP_12	AGP_AD_26_H	AR12	AGP_AD<26> 43 44
	AL14	VDDAGP_13	AGP_AD_27_H	AT12	AGP_AD<27> 43 44
	AL17	VDDAGP_14	AGP_AD_28_H	AR13	AGP_AD<28> 43 44
	AL20	VDDAGP_15	AGP_AD_29_H	AT13	AGP_AD<29> 43 44
	AL8	VDDAGP_16	AGP_AD_30_H	AM15	AGP_AD<30> 43 44
	AL9	VDDAGP_17	AGP_AD_31_H	AN15	AGP_AD<31> 43 44
	AP11	VDDAGP_18	AGP_CBE_3_L	AP13	AGP_CBE_L<3> 43 44
	AP14	VDDAGP_19			
	AP17	VDDAGP_20	AGP_AD_STB1_P	AK13	AGP_AD_STB1_P 43 44
	AP20	VDDAGP_21	AGP_AD_STB1_N	AJ13	AGP_AD_STB1_N 43 44
	AP3	VDDAGP_22			
	AP5	VDDAGP_23	AGP_ST_0_H	AR16	AGP_ST<0> 43 44
	AP8	VDDAGP_24	AGP_ST_1_H	AN16	AGP_ST<1> 43 44
			AGP_ST_2_H	AP16	AGP_ST<2> 43 44

11 =I2_AGP_VREF — AD18 AGP_VREF_0_H

47 44 43 10 =PP1V5_AGP — R5600 60.4 1% 1/16W MF-LF 402 — I2_AGP_PVTREF — AJ18 AGP_PVTREF_H

21 =I2_AGP_FBCLK_IN — AM10 AGP_FB_CLK_IN_H

AGP_FBCLK_OUT_H AM9 — 43 I2_AGP_FBCLK_OUT_R — R5605 22 5% 1/16W MF-LF 402 — I2_AGP_FBCLK_OUT 21 43

1.5V IN

1.5V OUT

One resistor for each of:
- AGP_RBF_L
- AGP_GNT_L
- AGP_FRAME_L
- AGP_REQ_L
- AGP_STOP_L
- AGP_DEVSEL_L
- AGP_IRDY_L
- AGP_TRDY_L

AGP PULL-UPS/PULL DOWNS

44 10 =PP3V3_AGP

44 43 AGP_BUSY_L	R5610 10K 5% 1/16W MF-LF 402	
44 43 STOP_AGP_L	R5611 10K 5% 1/16W MF-LF 402	
44 22 AGP_INT_L	R5620 10K 5% 1/16W MF-LF 402	

47 44 43 10 =PP1V5_AGP

6 =RP5610P4	RP5610 10K 5% 1/16W SM-LF	
6 =RP5610P2	RP5610 10K 5% 1/16W SM-LF	
6 =RP5610P3	RP5610 10K 5% 1/16W SM-LF	
6 =RP5611P2	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P3	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P4	RP5611 10K 5% 1/16W SM-LF	
6 =RP5611P1	RP5611 10K 5% 1/16W SM-LF	
6 =RP5610P1	RP5610 10K 5% 1/16W SM-LF	
44 43 AGP_WBF_L	R5612 10K 5% 1/16W MF-LF 402	
43 AGP_PIPE_L	R5613 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB0_P	R5614 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB1_P	R5615 10K 5% 1/16W MF-LF 402	
44 43 AGP_SB_STB_P	R5616 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB0_N	R5617 10K 5% 1/16W MF-LF 402	
44 43 AGP_AD_STB1_N	R5618 10K 5% 1/16W MF-LF 402	
44 43 AGP_SB_STB_N	R5619 10K 5% 1/16W MF-LF 402	

I2 AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 56 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

AGP_CLK66M_GPU 11 44

Page Notes

Power aliases required by this page:
- =PP3V3_AGP
- =PP1V5_AGP

Signal aliases required by this page:
- =AGP_VREF - VRef divider output for both GPU and NB
- =AGP_GPU_RESET_L - Active low reset for GPU

BOM options provided by this page:
(NONE)

NOTE: AGP 8x signals are not provided by this page.

OMIT
CRITICAL

U5700
BGA
M11P
(1 OF 8)

43 AGP_AD<0>	H29	AD_0	
43 AGP_AD<1>	H28	AD_1	
43 AGP_AD<2>	J29	AD_2	
43 AGP_AD<3>	J28	AD_3	
43 AGP_AD<4>	K29	AD_4	
43 AGP_AD<5>	K28	AD_5	
43 AGP_AD<6>	L29	AD_6	
43 AGP_AD<7>	L28	AD_7	
43 AGP_AD<8>	N28	AD_8	
43 AGP_AD<9>	P29	AD_9	
43 AGP_AD<10>	P28	AD_10	
43 AGP_AD<11>	R29	AD_11	
43 AGP_AD<12>	R28	AD_12	
43 AGP_AD<13>	T29	AD_13	
43 AGP_AD<14>	T28	AD_14	
43 AGP_AD<15>	U29	AD_15	
43 AGP_AD<16>	N25	AD_16	
43 AGP_AD<17>	R26	AD_17	
43 AGP_AD<18>	P25	AD_18	
43 AGP_AD<19>	R27	AD_19	
43 AGP_AD<20>	R25	AD_20	
43 AGP_AD<21>	T25	AD_21	
43 AGP_AD<22>	T26	AD_22	
43 AGP_AD<23>	U25	AD_23	
43 AGP_AD<24>	V27	AD_24	
43 AGP_AD<25>	W26	AD_25	
43 AGP_AD<26>	W25	AD_26	
43 AGP_AD<27>	Y26	AD_27	
43 AGP_AD<28>	Y25	AD_28	
43 AGP_AD<29>	AA26	AD_29	
43 AGP_AD<30>	AA25	AD_30	
43 AGP_AD<31>	AA27	AD_31	

AGP/PCI INTERFACE

PCICLK	AG30	AGP_CLK66M_GPU	11 44
RST*	AG28	AGP_ATI_RESET_L	
INTA*	AE26	AGP_INT_L	22 43
GNT*	AD26	AGP_GNT_L	6 43
REQ*	AF28	AGP_REQ_L	6 43
FRAME*	W28	AGP_FRAME_L	6 43
TRDY*	V28	AGP_TRDY_L	6 43
IRDY*	W29	AGP_IRDY_L	6 43
DEVSEL*	V29	AGP_DEVSEL_L	6 43
STOP*	N26	AGP_STOP_L	6 43
PAR	M25	AGP_PAR	43
C_BE_0*	N29	AGP_CBE_L<0>	43
C_BE_1*	U28	AGP_CBE_L<1>	43
C_BE_2*	P26	AGP_CBE_L<2>	43
C_BE_3*	U26	AGP_CBE_L<3>	43

AGP ONLY

RBF*	AE29	AGP_RBF_L	6 43
WBF*	AC26	AGP_WBF_L	43
ST_0	AF29	AGP_ST<0>	43
ST_1	AD27	AGP_ST<1>	43
ST_2	AE28	AGP_ST<2>	43
SB_STBF	AB29	AGP_SB_STB_P	43
SB_STBS	AB28	AGP_SB_STB_N	43
AD_STBF_0	M28	AGP_AD_STB0_P	43
AD_STBS_0	M29	AGP_AD_STB0_N	43
AD_STBF_1	V25	AGP_AD_STB1_P	43
AD_STBS_1	V26	AGP_AD_STB1_N	43
AGPREF	M26	=GPU_AGP_VREF	11
STP_AGP*	AH30	STOP_AGP_L	43
AGP_BUSY*	AH29	AGP_BUSY_L	43
SUS_STAT*	AG26	AGP_SUS_STAT_L_PU	

AGP 8X

ATI_DBI_HI_PU	AB25	DBI_HI	
ATI_DBI_LO_PU	AB26	DBI_LO	
AGP8X_DET_PU	AC25	AGP8X_DET*	

43 AGP_SBA<0>	AD28	SBA_0	
43 AGP_SBA<1>	AD29	SBA_1	
43 AGP_SBA<2>	AC28	SBA_2	
43 AGP_SBA<3>	AC29	SBA_3	
43 AGP_SBA<4>	AA28	SBA_4	
43 AGP_SBA<5>	AA29	SBA_5	
43 AGP_SBA<6>	Y28	SBA_6	
43 AGP_SBA<7>	Y29	SBA_7	
GPU_AGPTEST	M27	AGPTEST	

R5700 47 5% 1/16W MF-LF 402
11 =AGP_GPU_RESET_L

44 43 10 =PP3V3_AGP
R5722 20K 5% 1/16W MF-LF 402

47 44 43 10 =PP1V5_AGP
R5720 10K 5% 1/16W MF-LF 402
R5725 47K 5% 1/16W MF-LF 402
R5726 47K 5% 1/16W MF-LF 402
R5721 47 1% 1/16W MF-LF 402

47 44 43 10 =PP1V5_AGP
R5730 1K 1% 1/16W MF-LF 402
CONNECT TO GPU AGP REF
CAN ALSO CONNECT TO NB IF CHIPS ARE CO-LOCATED
11 =AGP_VREF
C5732 0.1uF 10% 16V X5R 402
C5731 0.1uF 10% 16V X5R 402
R5731 1K 1% 1/16W MF-LF 402

PLACE C5731 AT GPU
PLACE C5732 AT NB
PLACE RESISTORS MIDWAY BETWEEN

GPU (M11) AGP Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 57 OF 115	

Page Notes

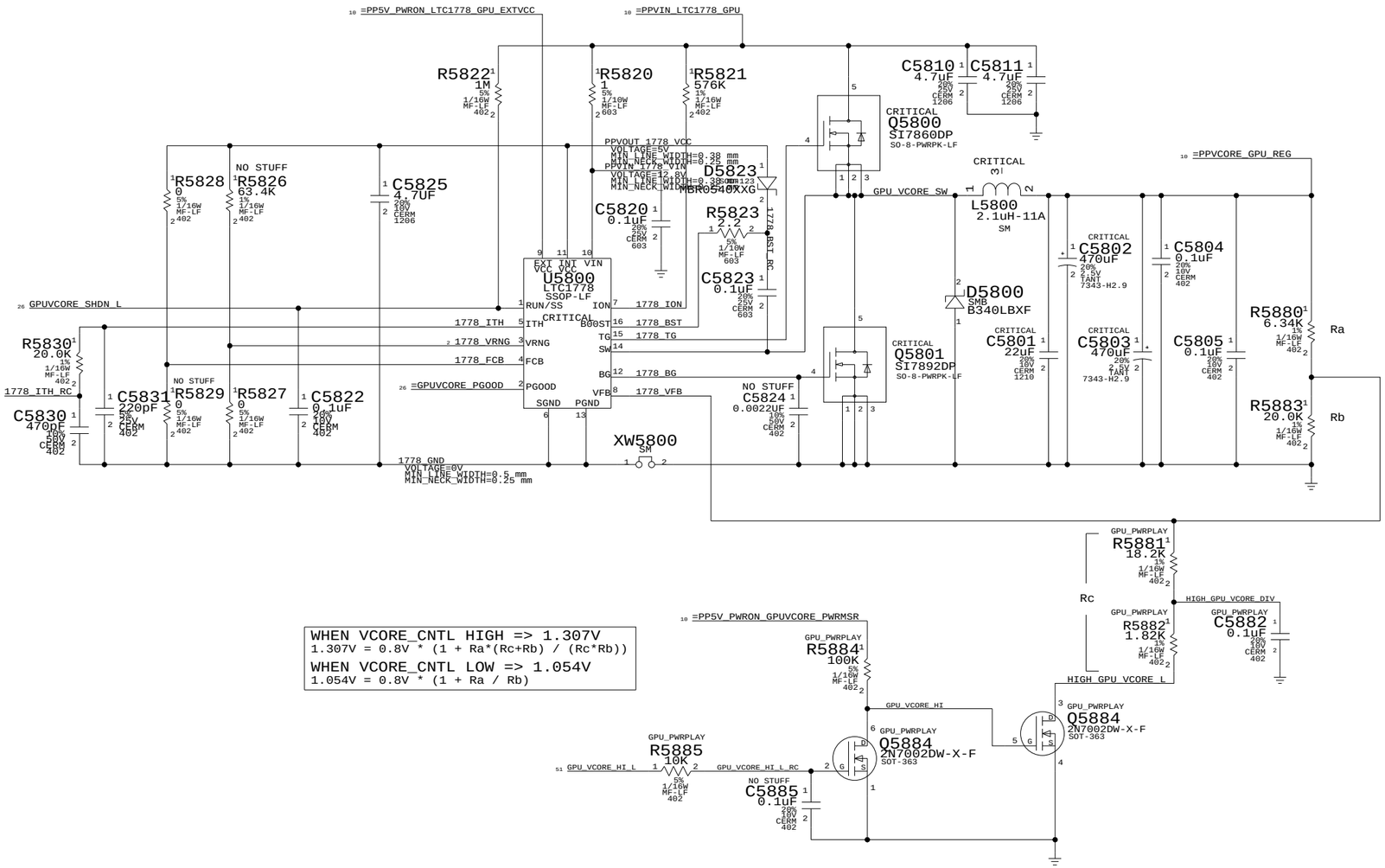
Power aliases required by this page:
- =PPVIN_LTC1778_GPU
- =PP5V_PWRON_LTC1778_GPU_EXTVCC
- =PPVCORE_GPU_REG

Signal aliases required by this page:
- =GPUVCORE_PGOOD - Active high Power Good signal for power sequencing

BOM options provided by this page:
- GPU_PWRPLAY

NOTE: Implements "Power Miser" feature for ATI GPUs

GPU VCORE SUPPLY



WHEN VCORE_CNTL HIGH => 1.307V
1.307V = 0.8V * (1 + Ra*(Rc+Rb) / (Rc*Rb))
WHEN VCORE_CNTL LOW => 1.054V
1.054V = 0.8V * (1 + Ra / Rb)

GPU VCore Supply

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 58 OF 115	

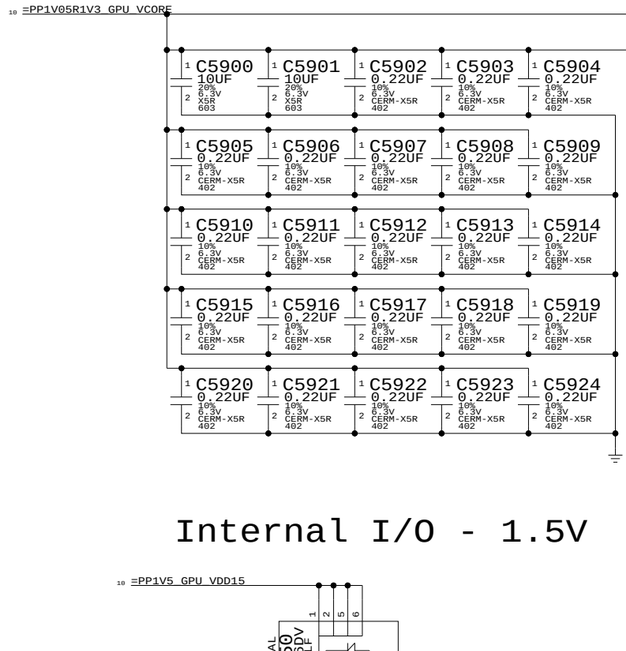
Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

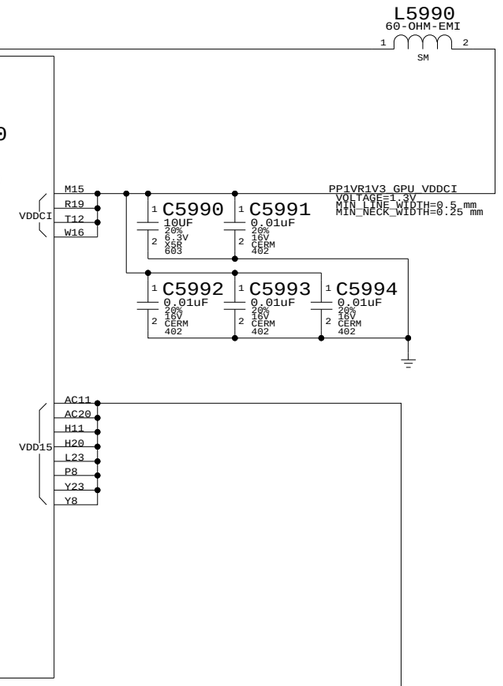
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

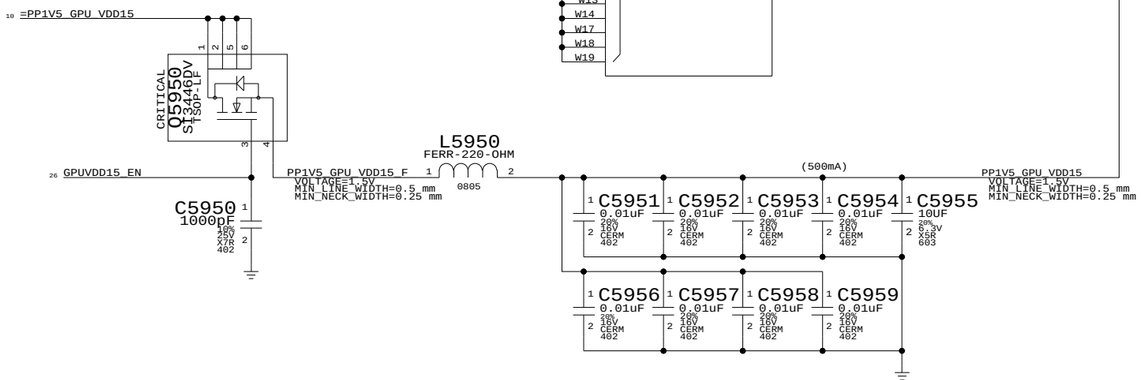
GPU VCORE - 1.3V/1.05V

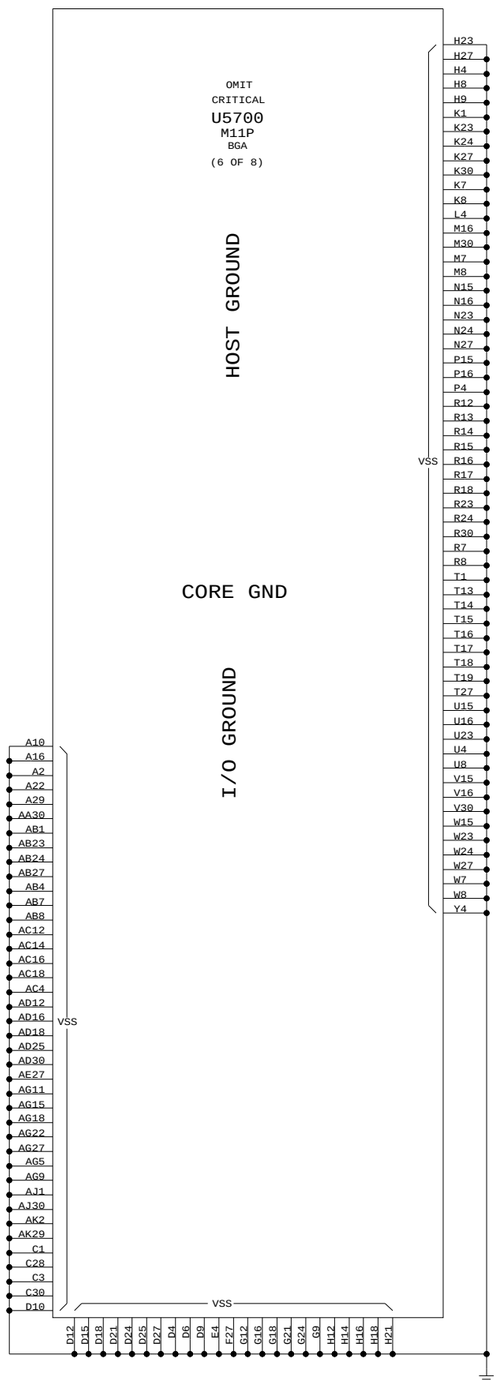


Internal I/O - 1.3V/1.05V



Internal I/O - 1.5V





GPU (M11) Core Power

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE

SHT 59 OF 115

Page Notes

Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP3V3_GPU_VDDR3
- =PP1V5_GPU_DVO
- =PP1V8_GPU_DVO
- =PP1V5R3V3_DVO_VREF
- =PP1V8_GPU_PANEL_IO
- =PP1V8_GPU_LVDS_PLL
- =PP2V5_GPU_LVDS_IO
- =PP2V5_GPU_LVDS_IO
- =PP1V5_AGP

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- DVO_1V8
- GPU_LVDDR_2V5
- GPU_LVDDR_2V8

NOTE: Implements a low-swing DVO bus only

OMIT
CRITICAL
U5700
M11P
BGA
(7 OF 8)

MEMORY I/O - 1.8V/2.5V

L6050
FERR-220-OHM
0805
(1200mA)
48 10 =PP1V8R2V5_GPU_FB_VIO
PP1V8R2V5_GPU_FB_VIO
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

C6050 10UF 20% 6.3V X5R 603
C6051 10UF 20% 6.3V X5R 603
C6052 0.1uF 20% 10V CERM 402
C6053 0.1uF 20% 10V CERM 402
C6054 0.1uF 20% 10V CERM 402
C6055 0.1uF 20% 10V CERM 402
C6056 0.1uF 20% 10V CERM 402
C6057 0.1uF 20% 10V CERM 402
C6058 0.1uF 20% 10V CERM 402
C6059 0.1uF 20% 10V CERM 402
C6060 0.1uF 20% 10V CERM 402
C6061 0.1uF 20% 10V CERM 402
C6062 0.01uF 20% 16V CERM 402
C6063 0.01uF 20% 16V CERM 402
C6064 0.01uF 20% 16V CERM 402
C6065 10UF 20% 6.3V X5R 603
C6066 10UF 20% 6.3V X5R 603
C6067 0.1uF 20% 10V CERM 402
C6068 0.1uF 20% 10V CERM 402
C6069 0.1uF 20% 10V CERM 402
C6070 0.1uF 20% 10V CERM 402
C6071 0.1uF 20% 10V CERM 402
C6072 0.1uF 20% 10V CERM 402
C6073 0.1uF 20% 10V CERM 402
C6074 0.1uF 20% 10V CERM 402
C6075 0.1uF 20% 10V CERM 402
C6076 0.1uF 20% 10V CERM 402
C6077 0.01uF 20% 16V CERM 402
C6078 0.01uF 20% 16V CERM 402
C6079 0.01uF 20% 16V CERM 402
C6080 10UF 20% 6.3V X5R 603
C6081 10UF 20% 6.3V X5R 603
C6082 0.1uF 20% 10V CERM 402
C6083 0.1uF 20% 10V CERM 402
C6084 0.1uF 20% 10V CERM 402
C6085 0.1uF 20% 10V CERM 402
C6086 0.1uF 20% 10V CERM 402
C6087 0.1uF 20% 10V CERM 402
C6088 0.1uF 20% 10V CERM 402
C6089 0.1uF 20% 10V CERM 402
C6090 0.1uF 20% 10V CERM 402
C6091 0.1uF 20% 10V CERM 402
C6092 0.01uF 20% 16V CERM 402
C6093 0.01uF 20% 16V CERM 402
C6094 0.01uF 20% 16V CERM 402

VDDR1
A15 A21 A28 A3 A9 AA1 AA4 AA7 AA8 AD4 B1 B30 D11 D13 D14 D17 D19 D20 D23 D26 D5 D8 E27 F4 G10 G13 G15 G19 G22 G27 G7 H10 H13 H15 H17 H19 H22 J1 J23 J24 J4 J7 J8 L27 L8 M4 N4 N7 N8 R1 R4 T4 T7 T8 V4 V7 V8

GPIO - 3.3V

10 =PP3V3_GPU_VDDR3
L6000
FERR-10-OHM-500MA
51 PP3V3_GPU_VDDR3
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
SM

VDDR3 AC19 AC21 AC22 AC8 AD19 AD21 AD22 AD7
C6000 10UF 20% 6.3V X5R 603
C6001 0.1uF 20% 10V CERM 402
C6002 0.1uF 20% 10V CERM 402
C6003 0.1uF 20% 10V CERM 402
C6004 0.1uF 20% 10V CERM 402
C6005 0.1uF 20% 10V CERM 402
C6006 0.1uF 20% 10V CERM 402

DVO I/O (EXT.TMDS) - 1.5V/1.8V

VDDR4 AC10 AC9 AD10 AD9 AG7
C6010 10UF 20% 6.3V X5R 603
C6011 0.1uF 20% 10V CERM 402
C6012 0.1uF 20% 10V CERM 402
C6013 0.1uF 20% 10V CERM 402
C6014 0.1uF 20% 10V CERM 402
C6015 0.1uF 20% 10V CERM 402

53 PP1V5R3V3_GPU_VDDR4
MAKE_BASE=TRUE
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

10 =PP1V8_GPU_DVO
DVO_1V8
L6010
FERR-10-OHM-500MA
SM

10 =PP1V5_GPU_DVO
DVO_1V5
L6011
FERR-10-OHM-500MA
SM
=PP1V5R3V3_DVO_VREF 54

44 43 10 =PP1V5_AGP
L6020
FERR-10-OHM-500MA
SM

AGP 4X I/O - 1.5V

(20mA)
PP1V5_GPU_AGP
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm

VDDP AA23 AA24 AB30 AC23 AC27 AE30 AF27 J30 M23 M24 N30 P23 P27 T23 T24 T30 U27 V23 V24 W30 Y27
C6020 0.1uF 20% 10V CERM 402
C6021 0.1uF 20% 10V CERM 402
C6022 0.1uF 20% 10V CERM 402
C6023 0.1uF 20% 10V CERM 402
C6024 10UF 20% 6.3V X5R 603
C6025 0.01uF 20% 16V CERM 402
C6026 0.01uF 20% 16V CERM 402
C6027 0.01uF 20% 16V CERM 402
C6028 0.01uF 20% 16V CERM 402
C6029 0.01uF 20% 16V CERM 402
C6030 0.1uF 20% 10V CERM 402
C6031 0.1uF 20% 10V CERM 402
C6032 0.1uF 20% 10V CERM 402
C6033 0.1uF 20% 10V CERM 402

LVDS PLL - 1.8V

51 =PP1V8_GPU_LVDS_PLL
(40mA)
L6048
FERR-220-OHM
0402
PP1V8_GPU_LVDS_PLL
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

C6048 10UF 20% 6.3V X5R 603
C6049 0.01uF 20% 16V CERM 402

L6043
FERR-220-OHM
0402
10 =PP1V8_GPU_PANEL_IO
PP1V8_GPU_PANEL_IO 53
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
ALSO TXVDDR

LVDS I/O - 1.8V

(180mA)
LPVDD AJ20
LVDDR_18_0 AE15
LVDDR_18_1 AF21
LVDDR_25_0 AE17
LVDDR_25_1 AE20

C6043 10UF 20% 6.3V X5R 603
C6044 0.1uF 20% 10V CERM 402
C6045 0.1uF 20% 10V CERM 402
C6046 0.1uF 20% 10V CERM 402
C6047 0.01uF 20% 16V CERM 402

10 =PP2V5_GPU_LVDS_IO
GPU_LVDDR_2V5
L6040
FERR-10-OHM-500MA
SM

(350mA)
PP2V5R2V8_GPU_LVDS_IO
VOLTAGE=2.8V
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
10 =PP2V8_GPU_LVDS_IO
GPU_LVDDR_2V8
L6041
FERR-10-OHM-500MA
SM

C6040 10UF 20% 6.3V X5R 603
C6041 0.01uF 20% 16V CERM 402
C6042 0.01uF 20% 16V CERM 402

LVDS I/O - 2.5V/2.8V

VDDRH1 N6
VDDRH0 F18
VSSRH0 F19
VSSRH1 M6
C6095 10UF 20% 6.3V X5R 603
C6096 0.01uF 20% 16V CERM 402
C6097 0.01uF 20% 16V CERM 402

L6095
FERR-220-OHM
0402
PP1V8_GPU_VDD_MEM_CLK
VOLTAGE=1.8V
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm

GPU (M11) I/O Power

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE	SHT	OF
NONE	60	115

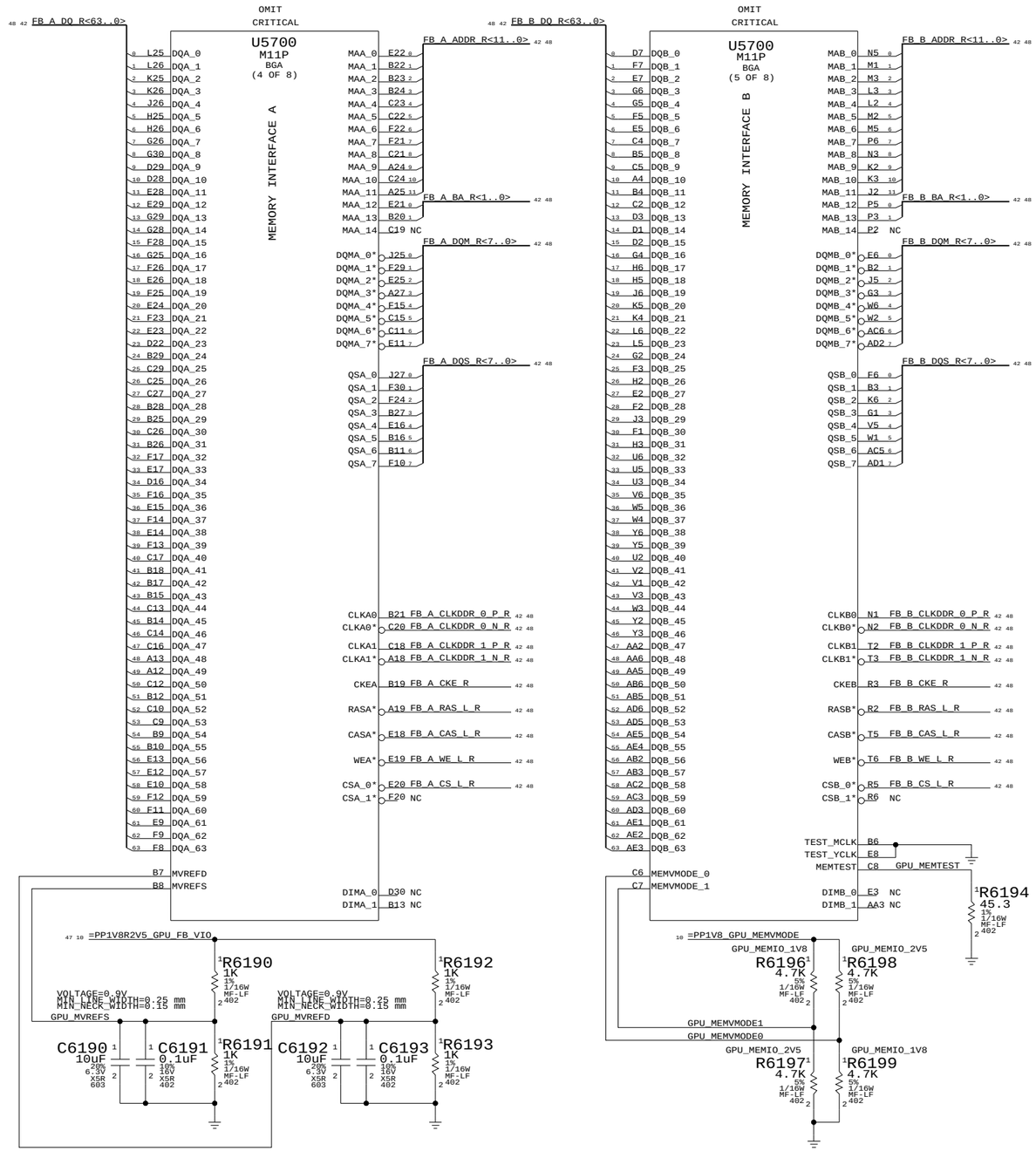
Page Notes

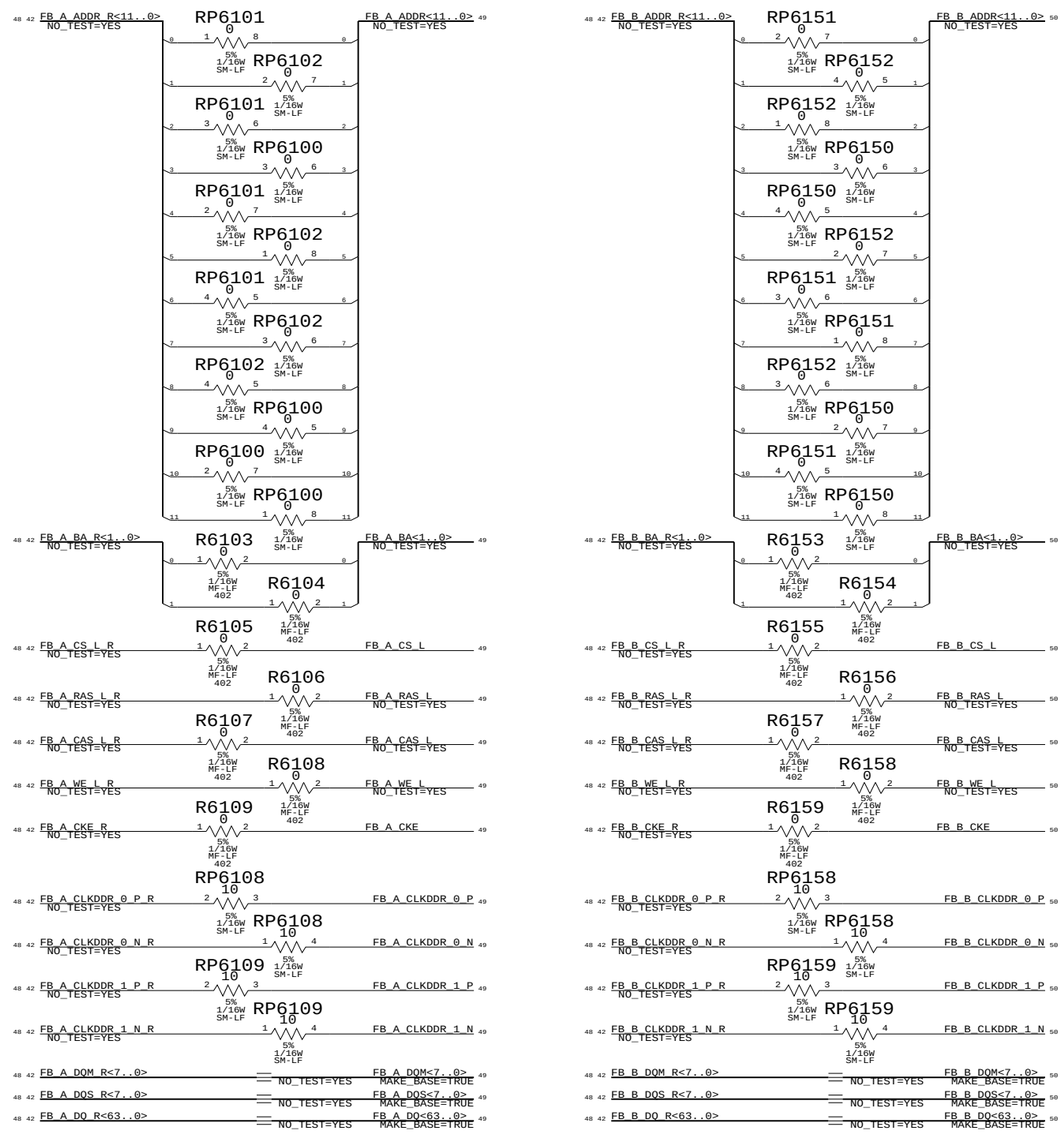
Power aliases required by this page:
- =PP1V8R2V5_GPU_FB_VIO
- =PP1V8_GPU_MEMVMODE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_MEMIO_1V8
- GPU_MEMIO_2V5

GPU Frame Buffer Series Term





GPU (M11) Frame Buffer I/F

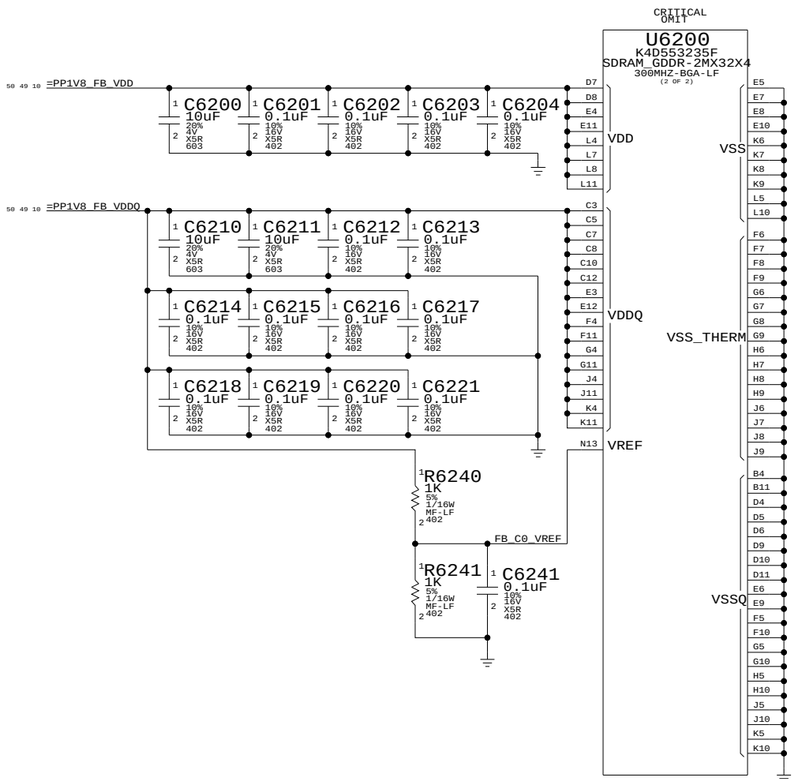
SYNC_MASTER=N/A SYNC_DATE=N/A

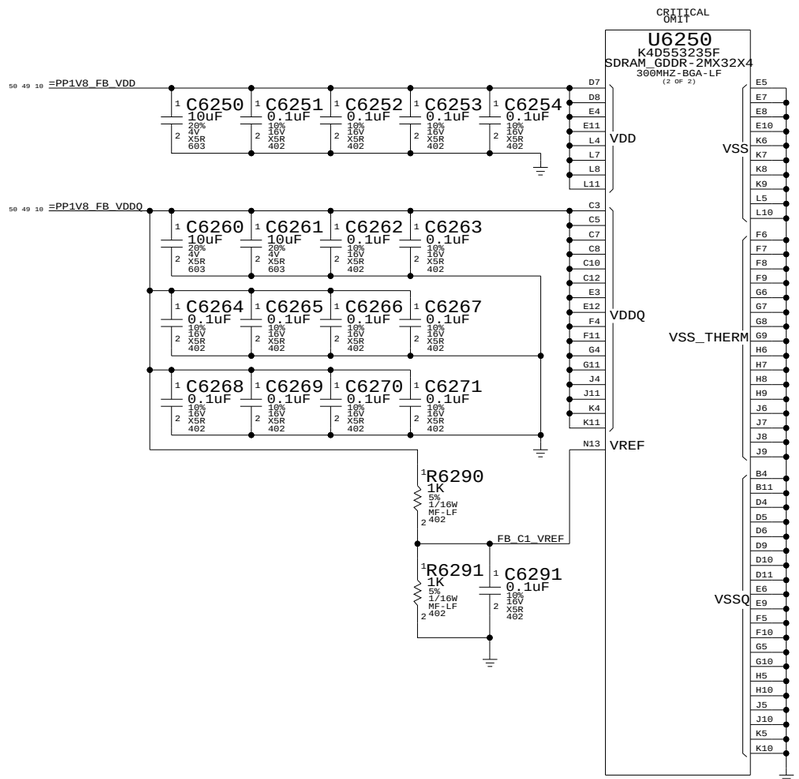
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE

SHT 61 OF 115





Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NET_TYPE

ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
ECSETs provided by GPU				
I244	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_P 48 49
I245	RAM_DIFF	RAM_DIFF	FB_A_CLK_0	FB_A_CLKDDR_0_N 48 49
I246	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_P 48 49
I247	RAM_DIFF	RAM_DIFF	FB_A_CLK_1	FB_A_CLKDDR_1_N 48 49
I248	RAM	RAM		FB_A_CKE 48 49
I249	RAM	RAM		FB_A_CS_L 48 49
I250	RAM	RAM		FB_A_ADDR<11..0> 48 49
I251	RAM	RAM		FB_A_BA<1..0> 48 49
I253	RAM	RAM		FB_A_RAS_L 48 49
I252	RAM	RAM		FB_A_CAS_L 48 49
I254	RAM	RAM		FB_A_WE_L 48 49
I255	RAM	RAM		FB_A_DQS<7..0> 48 49
I256	RAM	RAM		FB_A_DQM<7..0> 48 49
I257	RAM	RAM		FB_A_DQ<63..0> 48 49

GPU Frame Buffer A

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 62 OF 115	

Page Notes

Power aliases required by this page:
- =PP1V8_FB_VDD
- =PP1V8_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

ECSETs provided by GPU

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
I243	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_P
I244	RAM_DIFF	RAM_DIFF	FB_B_CLK_0	FB_B_CLKDDR_0_N
I245	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_P
I247	RAM_DIFF	RAM_DIFF	FB_B_CLK_1	FB_B_CLKDDR_1_N
I246	RAM	RAM		FB_B_CKE
I248	RAM	RAM		FB_B_CS_L
I252	RAM	RAM		FB_B_ADDR<11..0>
I251	RAM	RAM		FB_B_BA<1..0>
I249	RAM	RAM		FB_B_RAS_L
I250	RAM	RAM		FB_B_CAS_L
I253	RAM	RAM		FB_B_WE_L
I254	RAM	RAM		FB_B_DQS<7..0>
I255	RAM	RAM		FB_B_DQM<7..0>
I256	RAM	RAM		FB_B_DQ<63..0>

C6367 removed due to MCO violation

TITLE	GPU Frame Buffer B
SYNC_MASTER	N/A
SYNC_DATE	N/A

APPLE COMPUTER INC.

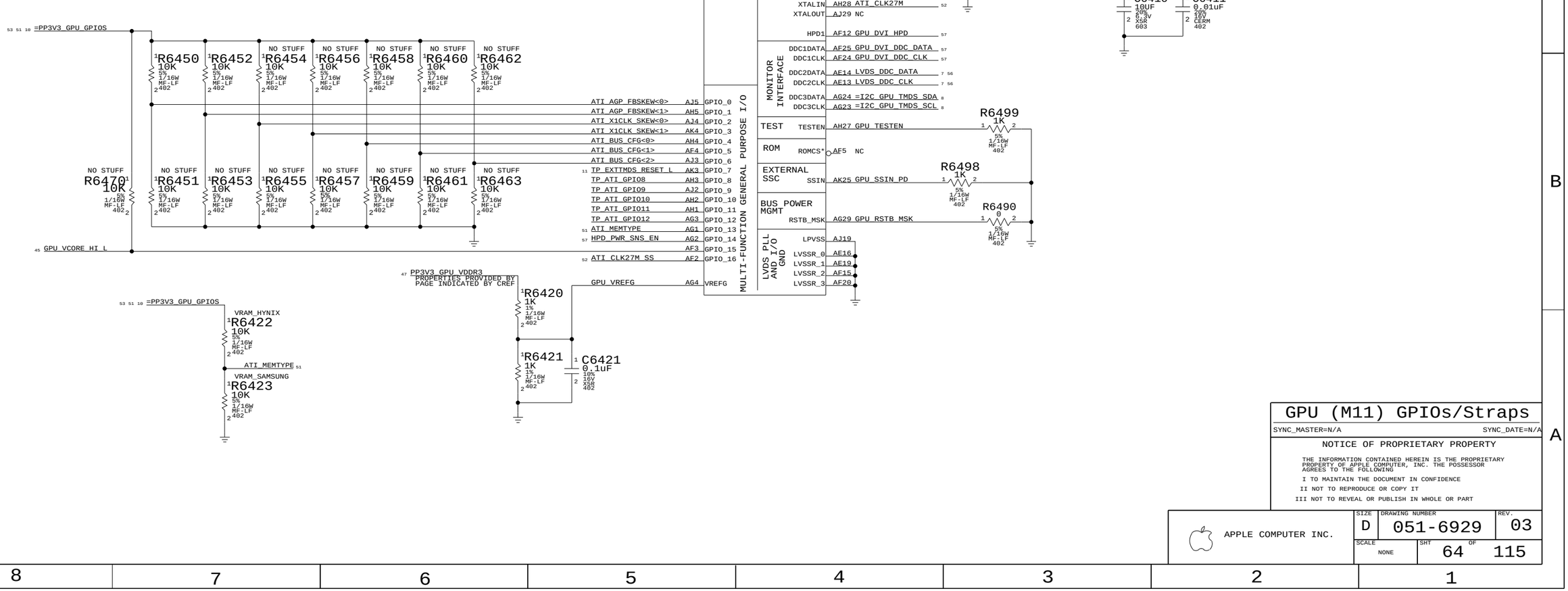
SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 63 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



GPU (M11) GPIOs/Straps

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 64 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_CLOCKS
- =PPVIN_GPU_LVDDR_LDO
- =PP2V5_GPU_LVDDR_LDO
- =PP3V3_GPU_PWRSEQ
- =PP2V5_GPU_PWRSEQ
- =PP1V8_GPU_PWRSEQ
- =PP1V5_GPU_PWRSEQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- GPU_SS
- GPU_LVDDR_2V8

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
160 ATI_CLK27M	CLOCK	CLOCK	
164	CLOCK	CLOCK	
165	CLOCK	CLOCK	
161 ATI_CLK27M_SS	CLOCK	CLOCK	
162	CLOCK	CLOCK	

ATI_CLK27M_R 52
ATI_CLK27M 51 52
ATI_CLK27M_SSIN 52
ATI_CLK27M_SS_R 52
ATI_CLK27M_SS 51 52

27M OSC

52 10 =PP3V3_GPU_CLOCKS
L6500 FERR-EMI-100-OHM SM
VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
PP3V3_GPU_OSC
C6500 0.1uF 20% 10V CERM 402
C6501 4.7uF 20% 6.3V CERM 805
NO STUFF R6503 100K 5% 1/16W MF-LF 402
CRITICAL 14 VCC G6500 27MHZ OSC SM
ATI_OSC_OE 1 OE
OUT 8 52 ATI_CLK27M_R
GND 7
GPU_SS (PLACE R6500 CLOSE TO OSC)
R6500 0 5% 1/16W MF-LF 402
ATI_CLK27M_SSIN 52
R6501 287 1% 1/16W MF-LF 402
(PLACE THE OSCILLATOR AND R6501/R6502 CLOSE TO M18 IC)
ATI_CLK27M 51 52
R6502 162 1% 1/16W MF-LF 402

SPREAD SPECTRUM SUPPORT
S0=1;S1=M => -1.5% DOWN-SPREAD

52 10 =PP3V3_GPU_CLOCKS
GPU_SS L6510 FERR-EMI-100-OHM SM
VOLTAGE=3.3V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm
PP3V3_GPU_SS
GPU_SS C6510 10UF 20% 6.3V X5R 603
GPU_SS C6511 0.1UF 20% 10V CERM 402
GPU_SS CRITICAL
VDD U6510 CY25811 SOI
52 ATI_CLK27M_SSIN XIN/CLKIN
NC XOUT
NC FRSEL
CY25811_S1 S1
CY25811_S0 S0
VSS
SSCLK 52 ATI_CLK27M_SS_R
GPU_SS R6510 33 5% 1/16W MF-LF 402
ATI_CLK27M_SS 51 52
NO STUFF R6511 0 5% 1/16W MF-LF 402
GPU_SS R6513 0 5% 1/16W MF-LF 402
NO STUFF R6512 0 5% 1/16W MF-LF 402
NO STUFF R6514 0 5% 1/16W MF-LF 402

M11 Power Shutdown Sequencing

10 =PP2V5_GPU_PWRSEQ
XW6590 SM
PP2V5_GPU_PSNECK VOLTAGE=2.5V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363

10 =PP1V8_GPU_PWRSEQ
XW6591 SM
PP1V8_GPU_PSNECK VOLTAGE=1.8V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363

10 =PP1V5_GPU_PWRSEQ
XW6592 SM
PP1V5_GPU_PSNECK VOLTAGE=1.5V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm
DP6590 BAS16TW-X-F SOT-363

10 =PP3V3_GPU_PWRSEQ
XW6593 SM
PP3V3_GPU_PSNECK VOLTAGE=3.3V MIN_LINE_WIDTH=0.2 mm MIN_NECK_WIDTH=0.2 mm

LVDDR 2.8V LDO

GPU_LVDDR_2V8 CRITICAL
U6530 MAX8860EUA27+T UMAX10
10 =PPVIN_GPU_LVDDR_LDO
IN
SHDN*
SET
OUT1
OUT2
FAULT*
CC
GND
MAX8860_FAULT_L
MAX8860_CC
GPU_LVDDR_2V8 C6530 2.2uF 20% 6.3V CERM1 603
GPU_LVDDR_2V8 C6531 0.033uF 20% 10V X7R 402
GPU_LVDDR_2V8 R6530 100K 5% 1/16W MF-LF 402
=PP2V8_GPU_LVDDR_LDO 10
GPU_LVDDR_2V8 C6532 2.2uF 20% 6.3V CERM1 603

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
353S0647	353S1140	GPU_LVDDR_2V8	U6530	2.82V instead of 2.77V

GPU (M11) Clocks/Misc

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 65 OF 115

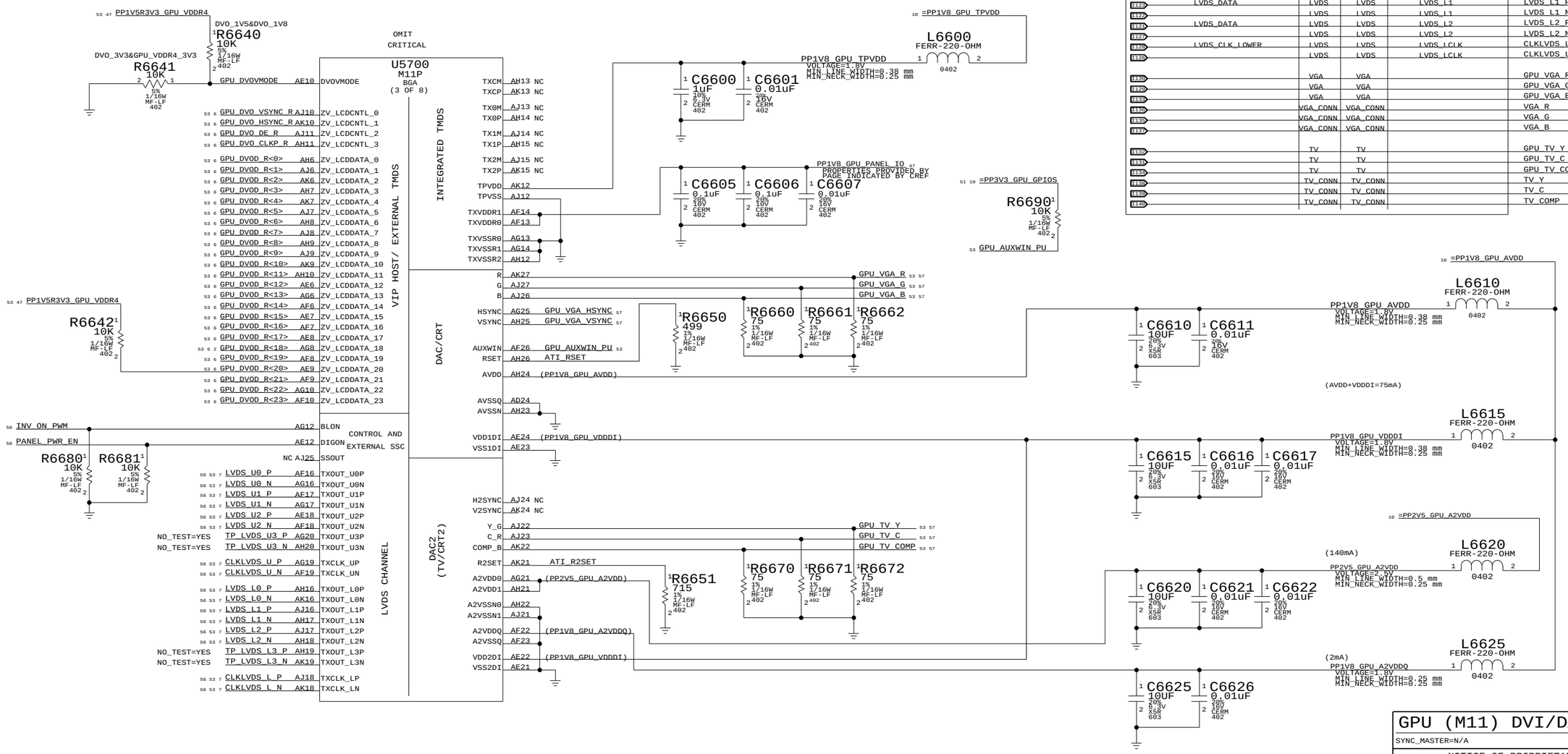
Page Notes

Power aliases required by this page:
- =PP2V5_GPU_A2VDD
- =PP1V8_GPU_AVDD
- =PP1V8_GPU_TPVDD
- =PP3V3_GPU_GPIOS

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
- DVO_1V5
- GPU_VDDR4_3V3
- DVO_1V8
- DVO_3V3

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
	DVO	DVO		GPU_DVOD_R<23..0> 2 6 53
	DVO	DVO		GPU_DVO_HSYNC_R 6 53
ECSETs provided by SI TMDS	DVO	DVO		GPU_DVO_VSYNC_R 6 53
	DVO	DVO		GPU_DVO_DE_R 6 53
	DVO	DVO		GPU_DVO_CLKP_R 6 53
LVDS_DATA	LVDS	LVDS	LVDS_U0	LVDS_U0_P 7 53 56
	LVDS	LVDS	LVDS_U0	LVDS_U0_N 7 53 56
LVDS_DATA	LVDS	LVDS	LVDS_U1	LVDS_U1_P 7 53 56
	LVDS	LVDS	LVDS_U1	LVDS_U1_N 7 53 56
LVDS_DATA	LVDS	LVDS	LVDS_U2	LVDS_U2_P 7 53 56
	LVDS	LVDS	LVDS_U2	LVDS_U2_N 7 53 56
LVDS_CLK_UPPER	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_P 7 53 56
	LVDS	LVDS	LVDS_UCLK	CLKLVDS_U_N 7 53 56
LVDS_DATA	LVDS	LVDS	LVDS_L0	LVDS_L0_P 7 53 56
	LVDS	LVDS	LVDS_L0	LVDS_L0_N 7 53 56
LVDS_DATA	LVDS	LVDS	LVDS_L1	LVDS_L1_P 7 53 56
	LVDS	LVDS	LVDS_L1	LVDS_L1_N 7 53 56
LVDS_DATA	LVDS	LVDS	LVDS_L2	LVDS_L2_P 7 53 56
	LVDS	LVDS	LVDS_L2	LVDS_L2_N 7 53 56
LVDS_CLK_LOWER	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_P 7 53 56
	LVDS	LVDS	LVDS_LCLK	CLKLVDS_L_N 7 53 56
	VGA	VGA		GPU_VGA_R 53 57
	VGA	VGA		GPU_VGA_G 53 57
	VGA	VGA		GPU_VGA_B 53 57
	VGA_CONN	VGA_CONN		VGA_R 57
	VGA_CONN	VGA_CONN		VGA_G 57
	VGA_CONN	VGA_CONN		VGA_B 57
	TV	TV		GPU_TV_Y 53 57
	TV	TV		GPU_TV_C 53 57
	TV	TV		GPU_TV_COMP 53 57
	TV_CONN	TV_CONN		TV_Y 57
	TV_CONN	TV_CONN		TV_C 57
	TV_CONN	TV_CONN		TV_COMP 57



GPU (M11) DVI/DAC Outputs

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 66 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI - =PP1V5R3V3_DVO_VREF

Signal aliases required by this page:
- =SI_TMDS_RESET_L - =RP67xxPy (pinswappable series R)
- =SI_I2C_CLK
- =SI_I2C_DATA

BOM options provided by this page:
- TMDS_EXT - DVO_1V5 - DVO_3V3
- TMDS_DUAL - DVO_1V8

Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
GPU_DVO_LOWER	DVO	DVO		GPU_DVOD<0..11> 6 54
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_HSYNC 6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_VSYNC 6 54 55
GPU_DVO_BOTH	DVO	DVO		GPU_DVO_DE 6 54 55
GPU_DVO_CLKP	DVO	DVO		GPU_DVO_CLKP 6 54 55
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKP 2 54
TMDS_CLK	TMDS	TMDS	SI_TMDS_CLK	SI_TMDS_CLKN 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DP<0> 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D0	SI_TMDS_DN<0> 2 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DP<1> 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D1	SI_TMDS_DN<1> 2 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DP<2> 54
TMDS_DATA	TMDS	TMDS	SI_TMDS_D2	SI_TMDS_DN<2> 2 54

Lower DVO Termination

Place close to GPU

One each for: GPU_DVOD<0..11>, GPU_DVO_HSYNC, GPU_DVO_VSYNC, GPU_DVO_DE, GPU_DVO_CLKP

TMDS_EXT&TMDS_DUAL RP6720 10 5% 1/16W SM-LF
- 6 =RP6720P1 — 1 — 8 =RP6720P8 6
- 6 =RP6720P2 — 2 — 7 =RP6720P7 6
- 6 =RP6720P3 — 3 — 6 =RP6720P6 6
- 6 =RP6720P4 — 4 — 5 =RP6720P5 6

TMDS_EXT&TMDS_DUAL RP6721 10 5% 1/16W SM-LF
- 6 =RP6721P1 — 1 — 8 =RP6721P8 6
- 6 =RP6721P2 — 2 — 7 =RP6721P7 6
- 6 =RP6721P3 — 3 — 6 =RP6721P6 6
- 6 =RP6721P4 — 4 — 5 =RP6721P5 6

TMDS_EXT&TMDS_DUAL RP6722 10 5% 1/16W SM-LF
- 6 =RP6722P1 — 1 — 8 =RP6722P8 6
- 6 =RP6722P2 — 2 — 7 =RP6722P7 6
- 6 =RP6722P3 — 3 — 6 =RP6722P6 6
- 6 =RP6722P4 — 4 — 5 =RP6722P5 6

TMDS_EXT&TMDS_DUAL RP6723 10 5% 1/16W SM-LF
- 6 =RP6723P1 — 1 — 8 =RP6723P8 6
- 6 =RP6723P2 — 2 — 7 =RP6723P7 6
- 6 =RP6723P3 — 3 — 6 =RP6723P6 6
- 6 =RP6723P4 — 4 — 5 =RP6723P5 6

SILICON IMAGE TMDS

TMDS_EXT&TMDS_DUAL RP6707 10 5% 1/16W SM-LF: 54 SI_TMDS_CLKN — 1 — 4 — TMDS_CLKN 54 57

TMDS_EXT&TMDS_DUAL RP6707 10 5% 1/16W SM-LF: 54 2 SI_TMDS_CLKP — 2 — 3 — TMDS_CLKP 54 57

TMDS_EXT&TMDS_DUAL RP6708 10 5% 1/16W SM-LF: 54 2 SI_TMDS_DN<0> — 1 — 4 — TMDS_DN<0> 54 57

TMDS_EXT&TMDS_DUAL RP6708 10 5% 1/16W SM-LF: 54 SI_TMDS_DP<0> — 2 — 3 — TMDS_DP<0> 54 57

TMDS_EXT&TMDS_DUAL RP6709 10 5% 1/16W SM-LF: 54 2 SI_TMDS_DN<1> — 2 — 3 — TMDS_DN<1> 54 57

TMDS_EXT&TMDS_DUAL RP6709 10 5% 1/16W SM-LF: 54 SI_TMDS_DP<1> — 1 — 4 — TMDS_DP<1> 54 57

TMDS_EXT&TMDS_DUAL RP6710 10 5% 1/16W SM-LF: 54 2 SI_TMDS_DN<2> — 1 — 4 — TMDS_DN<2> 54 57

TMDS_EXT&TMDS_DUAL RP6710 10 5% 1/16W SM-LF: 54 SI_TMDS_DP<2> — 2 — 3 — TMDS_DP<2> 54 57

EXTERNAL TMDS TERMINATION

TERMINATION NETWORK SHOULD BE CONNECTED AS SHOWN

EXT_TMDS_CLK_CMF
- TMDS_EXT&TMDS_DUAL R6760 49.9 1% 1/16W MF-LF 402: 57 54 TMDS_CLKP — 1 — 2
- TMDS_EXT&TMDS_DUAL R6761 49.9 1% 1/16W MF-LF 402: 1 — 2 TMDS_CLKN 54 57
- TMDS_EXT&TMDS_DUAL C6760 0.001uF 10% 50V CERM 402: 1 — 2

EXT_TMDS_D0_CMF
- TMDS_EXT&TMDS_DUAL R6762 49.9 1% 1/16W MF-LF 402: 57 54 TMDS_DP<0> — 1 — 2
- TMDS_EXT&TMDS_DUAL R6763 49.9 1% 1/16W MF-LF 402: 1 — 2 TMDS_DN<0> 54 57
- TMDS_EXT&TMDS_DUAL C6762 0.001uF 10% 50V CERM 402: 1 — 2

EXT_TMDS_D1_CMF
- TMDS_EXT&TMDS_DUAL R6764 49.9 1% 1/16W MF-LF 402: 57 54 TMDS_DP<1> — 1 — 2
- TMDS_EXT&TMDS_DUAL R6765 49.9 1% 1/16W MF-LF 402: 1 — 2 TMDS_DN<1> 54 57
- TMDS_EXT&TMDS_DUAL C6764 0.001uF 10% 50V CERM 402: 1 — 2

EXT_TMDS_D2_CMF
- TMDS_EXT&TMDS_DUAL R6766 49.9 1% 1/16W MF-LF 402: 57 54 TMDS_DP<2> — 1 — 2
- TMDS_EXT&TMDS_DUAL R6767 49.9 1% 1/16W MF-LF 402: 1 — 2 TMDS_DN<2> 54 57
- TMDS_EXT&TMDS_DUAL C6766 0.001uF 10% 50V CERM 402: 1 — 2

TMDS_EXT&TMDS_DUAL L6720 400-OHM-EMI SM-1: 1 — 2 =PP3V3_RUN_SI 10 54 55
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.38 mm
- VOLTAGE=3.3V
- PP3V3_SI_M_VCC
- TMDS_EXT&TMDS_DUAL C6720 10UF 10% 6.3V X5R 805: 1 — 2
- TMDS_EXT&TMDS_DUAL C6721 100pF 5% 50V CERM 402: 1 — 2
- TMDS_EXT&TMDS_DUAL C6722 100pF 5% 50V CERM 402: 1 — 2
- TMDS_EXT&TMDS_DUAL

TMDS_EXT&TMDS_DUAL L6723 400-OHM-EMI SM-1: 1 — 2 =PP3V3_RUN_SI 10 54 55
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.38 mm
- VOLTAGE=3.3V
- PP3V3_SI_M_AVCC
- TMDS_EXT&TMDS_DUAL C6723 10UF 10% 6.3V X5R 805: 1 — 2
- TMDS_EXT&TMDS_DUAL C6724 100pF 5% 50V CERM 402: 1 — 2
- TMDS_EXT&TMDS_DUAL C6725 100pF 5% 50V CERM 402: 1 — 2

TMDS_EXT&TMDS_DUAL L6726 400-OHM-EMI SM-1: 1 — 2 =PP3V3_RUN_SI 10 54 55
- MIN_NECK_WIDTH=0.2 mm
- MIN_LINE_WIDTH=0.38 mm
- VOLTAGE=3.3V
- PP3V3_SI_M_PVCC
- TMDS_EXT&TMDS_DUAL C6726 10UF 10% 6.3V X5R 805: 1 — 2
- TMDS_EXT&TMDS_DUAL C6727 100pF 5% 50V CERM 402: 1 — 2
- TMDS_EXT&TMDS_DUAL C6728 10UF 10% 6.3V X5R 805: 1 — 2
- TMDS_EXT&TMDS_DUAL C6729 100pF 5% 50V CERM 402: 1 — 2

Place C6726/C6727 at pin 28

Place C6728/C6729 at pin 46

TMDS_EXT&TMDS_DUAL R6734 10K 5% 1/16W MF-LF 402: 1 — 2

TMDS_EXT&TMDS_DUAL R6752 330 5% 1/16W MF-LF 402: 1 — 2

NO STUFF R6754 4.99K 1% 1/16W MF-LF 402: 1 — 2

CRITICAL U6700 SIL1178CS48 TSSOP

8 =I2C_SI_M_SCL	27	SCL	
8 =I2C_SI_M_SDA	26	SDA	
SI_M_A1	24	CTL3/A1	
55 11 =SI_TMDS_RESET_L	25	RST*	
		TMDS_EXT&TMDS_DUAL SYNCO/SYNCI	
55 SI_SYNC	47		
55 SI_HTPLG	44	EHTPLG	
54 6 GPU_DVOD<0>	18	D0	
54 6 GPU_DVOD<1>	17	D1	
54 6 GPU_DVOD<2>	16	D2	
54 6 GPU_DVOD<3>	15	D3	
54 6 GPU_DVOD<4>	14	D4	
54 6 GPU_DVOD<5>	13	D5	
54 6 GPU_DVOD<6>	10	D6	
54 6 GPU_DVOD<7>	9	D7	
54 6 GPU_DVOD<8>	8	D8	
54 6 GPU_DVOD<9>	7	D9	
54 6 GPU_DVOD<10>	6	D10	
54 6 GPU_DVOD<11>	5	D11	
55 54 6 GPU_DVO_DE	19	DE	
55 54 6 GPU_DVO_HSYNC	20	HSYNC	
55 54 6 GPU_DVO_VSYNC	21	VSYNC	
55 54 6 GPU_DVO_CLKP	12	IDCK+	
55 54 SI_IDCK_N	11	IDCK-	
		TXC+	33 — SI_TMDS_CLKP 2 54
		TXC-	32 — SI_TMDS_CLKN 54
		TX0+	36 — SI_TMDS_DP<0> 54
		TX0-	35 — SI_TMDS_DN<0> 2 54
		TX1+	39 — SI_TMDS_DP<1> 54
		TX1-	38 — SI_TMDS_DN<1> 2 54
		TX2+	42 — SI_TMDS_DP<2> 54
		TX2-	41 — SI_TMDS_DN<2> 2 54
		MSEN	48 — SI_M_MSEN
		EXT_SWING	30 — SI_M_EXTSWING
		VREF	2 — SI_VREF 54 55
	28	PVCC1	
	46	PVCC2	
	40	AVCC	
	34	AVCC	
	22	VCC	
	35	VCC	
	29	PGND	
	45	PGND	
	31	AGND	
	43	AGND	
	37	AGND	
	1	GND	
	23	GND	
	4	GND	
	49	THRML PAD	

DVO_3V3 R6733 1K 5% 1/16W MF-LF 402: 1 — 2

TMDS_EXT&TMDS_DUAL R6730 10K 5% 1/16W MF-LF 402: 1 — 2

NO STUFF R6732 100K 5% 1/16W MF-LF 402: 1 — 2

TMDS_EXT&TMDS_DUAL R6731 10K 5% 1/16W MF-LF 402: 1 — 2

DVO_1V5&DVO_1V8 R6742 0 5% 1/16W MF-LF 402: 55 54 SI_VREF — 2 — 1 — SI_IDCK_N 55 54

MIN_LINE_WIDTH=0.2 mm
MIN_NECK_WIDTH=0.2 mm

TMDS_EXT&TMDS_DUAL C6740 0.1uF 20% 10V CERM 402: 1 — 2

The DVO bus can be run with 3.3V or 1.5V/1.8V signaling. The power rail for the reference should be connected to the GPU DVO rail.

=PP1V5R3V3_DVO_VREF 47

DVO_1V5&DVO_1V8 R6740 1K 1% 1/16W MF-LF 402: 1 — 2

DVO_1V5&DVO_1V8 R6741 1K 1% 1/16W MF-LF 402: 1 — 2

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
TMDS_CLK	TMDS	TMDS	TMDS_CLK	TMDS_CLKP 54 57
TMDS_CLK	TMDS	TMDS	TMDS_CLK	TMDS_CLKN 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D0	TMDS_DP<0> 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D0	TMDS_DN<0> 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D1	TMDS_DP<1> 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D1	TMDS_DN<1> 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D2	TMDS_DP<2> 54 57
TMDS_DATA	TMDS	TMDS	TMDS_D2	TMDS_DN<2> 54 57

Lower TMDS Transmitter

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 67 OF 115	

Page Notes

Power aliases required by this page:
- =PP3V3_RUN_SI

Signal aliases required by this page:
- =SI_I2C_CLK
- =SI_I2C_DATA
- =SI_TMDS_RESET_L
- =RP68xxPy (pinswappable series R)

BOM options provided by this page:
- TMDS_DUAL

Net Spacing Type: TMDS

Net Physical Type: TMDS

NOTE: Target differential impedance for TMDS data pairs is 100 ohms.

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
154	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<12..19>	6 55
155	GPU_DVOD20	DVO	DVO		GPU_DVOD<20>	6 55
156	GPU_DVO_UPPER	DVO	DVO		GPU_DVOD<21..23>	6 55
157		PROVIDED BY LOWER TXMR			GPU_DVO_VSYNC	6 54 55
158		PROVIDED BY LOWER TXMR			GPU_DVO_DE	6 54 55
159		PROVIDED BY LOWER TXMR			GPU_DVO_CLKP	6 54 55
174	TMDS_DATA	TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DP<3>	2 55
175		TMDS	TMDS	SI_TMDS_D3	SI_TMDS_DN<3>	55
176	TMDS_DATA	TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DP<4>	55
177		TMDS	TMDS	SI_TMDS_D4	SI_TMDS_DN<4>	2 55
178	TMDS_DATA	TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DP<5>	55
179		TMDS	TMDS	SI_TMDS_D5	SI_TMDS_DN<5>	2 55
180		TMDS	TMDS	TMDS_D3	TMDS_DP<3>	55 57
181		TMDS	TMDS	TMDS_D3	TMDS_DN<3>	55 57
182		TMDS	TMDS	TMDS_D4	TMDS_DP<4>	55 57
183		TMDS	TMDS	TMDS_D4	TMDS_DN<4>	55 57
184		TMDS	TMDS	TMDS_D5	TMDS_DP<5>	55 57
185		TMDS	TMDS	TMDS_D5	TMDS_DN<5>	55 57

Upper DVO series termination

Place close to GPU

One for each of: GPU_DVOD<12..23>

TMDS_DUAL RP6821 10 — =RP6821P1 (1) — (8) =RP6821P8
TMDS_DUAL RP6821 10 — =RP6821P2 (2) — (7) =RP6821P7
TMDS_DUAL RP6821 10 — =RP6821P3 (3) — (6) =RP6821P6
TMDS_DUAL RP6821 10 — =RP6821P4 (4) — (5) =RP6821P5
TMDS_DUAL RP6822 10 — =RP6822P1 (1) — (8) =RP6822P8
TMDS_DUAL RP6822 10 — =RP6822P2 (2) — (7) =RP6822P7
TMDS_DUAL RP6822 10 — =RP6822P3 (3) — (6) =RP6822P6
TMDS_DUAL RP6822 10 — =RP6822P4 (4) — (5) =RP6822P5
TMDS_DUAL RP6823 10 — =RP6823P1 (1) — (8) =RP6823P8
TMDS_DUAL RP6823 10 — =RP6823P2 (2) — (7) =RP6823P7
TMDS_DUAL RP6823 10 — =RP6823P3 (3) — (6) =RP6823P6
TMDS_DUAL RP6823 10 — =RP6823P4 (4) — (5) =RP6823P5

All: 5% 1/16W SM-LF

VOLTAGE=3.3V
MIN_NECK_WIDTH=0.2 mm
MIN_LINE_WIDTH=0.38 mm
PP3V3_SI_S_PVCC

TMDS_DUAL L6836 400-OHM-EMI SM-1 — =PP3V3_RUN_SI (10 54 55)

TMDS_DUAL C6836 10UF 10% 6.3V X5R 805
TMDS_DUAL C6837 100pF 5% 50V CERM 402
TMDS_DUAL C6838 10UF 10% 6.3V X5R 805
TMDS_DUAL C6839 100pF 5% 50V CERM 402

Place C6836/C6837 at pin 28.

Place C6838/C6839 at pin 46.

TMDS_DUAL L6833 400-OHM-EMI SM-1 — =PP3V3_RUN_SI (10 54 55)

PP3V3_SI_S_AVCC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

TMDS_DUAL C6833 10UF 10% 6.3V X5R 805
TMDS_DUAL C6834 100pF 5% 50V CERM 402
TMDS_DUAL C6835 100pF 5% 50V CERM 402

TMDS_DUAL L6830 400-OHM-EMI SM-1 — =PP3V3_RUN_SI (10 54 55)

PP3V3_SI_S_VCC
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.2 mm
VOLTAGE=3.3V

TMDS_DUAL C6830 10UF 10% 6.3V X5R 805
TMDS_DUAL C6831 100pF 5% 50V CERM 402
TMDS_DUAL C6832 100pF 5% 50V CERM 402

TMDS_DUAL R6880 10K 5% 1/16W MF-LF 402
TMDS_DUAL R6881 330 5% 1/16W MF-LF 402
NO STUFF R6882 4.99K 1% 1/16W MF-LF 402

PVCC1 (28), PVCC2 (46), AVCC (40), AVCC (34), VCC (22), VCC (5)

8	=I2C_SI_S_SCL	27	SCL		
8	=I2C_SI_S_SDA	26	SDA		
	SI_S_A1	24	CTL3/A1		
54 11	=SI_TMDS_RESET_L	25	RST*		
	SI_SYNC	47	SYNCO/SYNCI		
54	SI_HTPLG	44	EHTPLG		
55 6	GPU_DVOD<12>	18	D0	TXC+ (33)	NC
55 6	GPU_DVOD<13>	17	D1	TXC- (32)	NC
55 6	GPU_DVOD<14>	16	D2	TX0+ (36)	SI_TMDS_DP<3> (2 55)
55 6	GPU_DVOD<15>	15	D3	TX0- (35)	SI_TMDS_DN<3> (55)
55 6	GPU_DVOD<16>	14	D4	TX1+ (39)	SI_TMDS_DP<4> (55)
55 6	GPU_DVOD<17>	13	D5	TX1- (38)	SI_TMDS_DN<4> (2 55)
55 6	GPU_DVOD<18>	10	D6	TX2+ (42)	SI_TMDS_DP<5> (55)
55 6	GPU_DVOD<19>	9	D7	TX2- (41)	SI_TMDS_DN<5> (2 55)
55 6	GPU_DVOD<20>	8	D8		
55 6	GPU_DVOD<21>	7	D9		
55 6	GPU_DVOD<22>	6	D10		
55 6	GPU_DVOD<23>	5	D11		
55 54 6	GPU_DVO_DE	19	DE		
54 6	GPU_DVO_HSYNC	20	HSYNC		
55 54 6	GPU_DVO_VSYNC	21	VSYNC		
55 54 6	GPU_DVO_CLKP	12	IDCK+		
54	SI_IDCK_N	11	IDCK-		

MSEN (48) — SI_S_MSEN
EXT_SWING (30) — SI_S_EXTSWING
VREF (2) — SI_VREF (54)

TMDS_DUAL CRITICAL U6800 SIL1178CS48 TSSOP

PGND (29), PGND (45), AGND (31), AGND (43), AGND (37), GND (1), GND (23), GND (4), THRMPAD (49)

Upper Channel Series Termination

TMDS_DUAL RP6811 10 — SI_TMDS_DN<3> — TMDS_DN<3> (55 57)
TMDS_DUAL RP6811 10 — SI_TMDS_DP<3> (55 2) — TMDS_DP<3> (55 57)
TMDS_DUAL RP6812 10 — SI_TMDS_DN<4> (55 2) — TMDS_DN<4> (55 57)
TMDS_DUAL RP6812 10 — SI_TMDS_DP<4> (55) — TMDS_DP<4> (55 57)
TMDS_DUAL RP6813 10 — SI_TMDS_DN<5> (55 2) — TMDS_DN<5> (55 57)
TMDS_DUAL RP6813 10 — SI_TMDS_DP<5> (55) — TMDS_DP<5> (55 57)

All: 5% 1/16W SM-LF

Upper Channel Common-mode Termination

TMDS_D3_CMF
TMDS_DUAL R6804 49.9 — TMDS_DP<3> (57 55) — TMDS_DUAL R6805 49.9 — TMDS_DN<3> (55 57)
TMDS_DUAL C6804 0.001uF 10% 50V CERM 402

TMDS_D4_CMF
TMDS_DUAL R6802 49.9 — TMDS_DP<4> (57 55) — TMDS_DUAL R6803 49.9 — TMDS_DN<4> (55 57)
TMDS_DUAL C6802 0.001uF 10% 50V CERM 402

TMDS_D5_CMF
TMDS_DUAL R6800 49.9 — TMDS_DP<5> (57 55) — TMDS_DUAL R6801 49.9 — TMDS_DN<5> (55 57)
TMDS_DUAL C6800 0.001uF 10% 50V CERM 402

All: 1% 1/16W MF-LF 402

Upper TMDS Transmitter

SYNC_MASTER=N/A SYNC_DATE=N/A

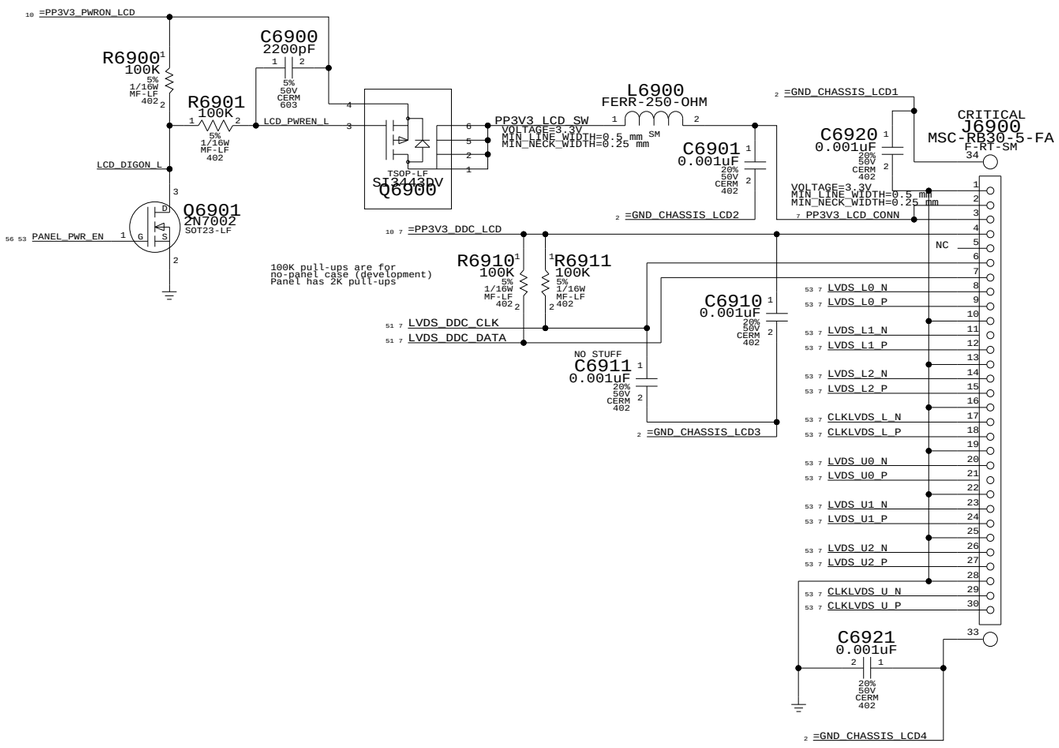
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

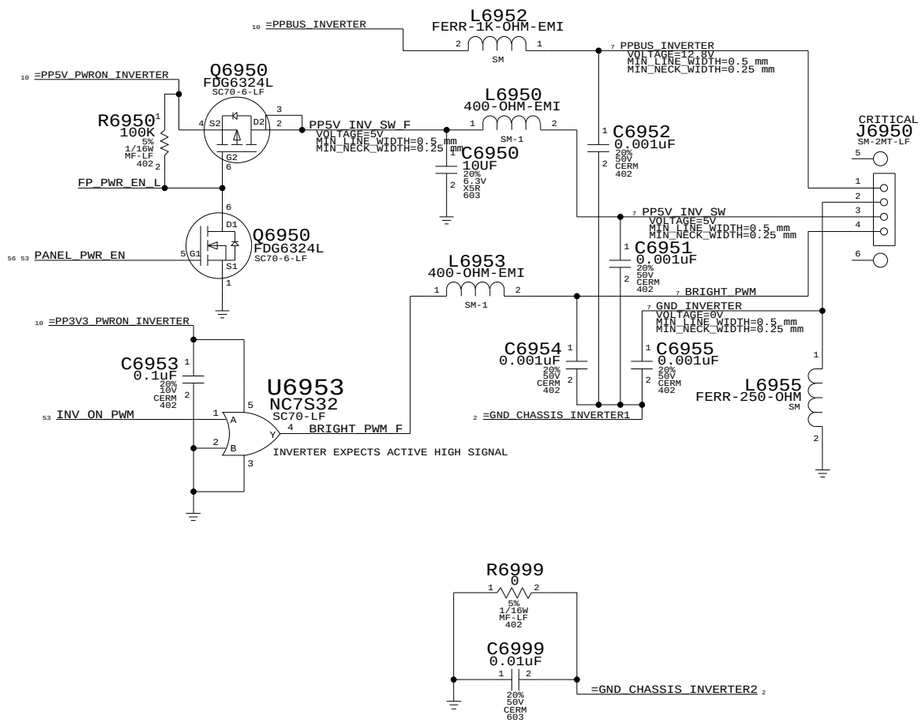
SCALE: NONE

SHT 68 OF 115

LCD (LVDS) INTERFACE



INVERTER INTERFACE



Internal Display Conns

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 69 OF 115	

DVI INTERFACE

DIFFERENTIAL_PAIR

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR	
16410	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKP 2 57
16410	TMDS_CONN	TMDS_CONN	TMDS_CONN_CLK	TMDS_CONN_CLKN 57
16406	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DP<0> 57
16403	TMDS_CONN	TMDS_CONN	TMDS_CONN_D0	TMDS_CONN_DN<0> 57
16402	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DP<1> 57
16399	TMDS_CONN	TMDS_CONN	TMDS_CONN_D1	TMDS_CONN_DN<1> 57
16398	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DP<2> 57
16395	TMDS_CONN	TMDS_CONN	TMDS_CONN_D2	TMDS_CONN_DN<2> 57
16390	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DP<3> 57
16388	TMDS_CONN	TMDS_CONN	TMDS_CONN_D3	TMDS_CONN_DN<3> 57
16386	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DP<4> 57
16384	TMDS_CONN	TMDS_CONN	TMDS_CONN_D4	TMDS_CONN_DN<4> 57
16382	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DP<5> 57
16380	TMDS_CONN	TMDS_CONN	TMDS_CONN_D5	TMDS_CONN_DN<5> 57

TMDS FILTERING
PLACE CLOSE TO CONNECTOR

CRITICAL L7000 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<0> 1 — 4 TMDS_CONN_DN<0> 57
54 TMDS_DP<0> 2 — 3 TMDS_CONN_DP<0> 57

CRITICAL L7001 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<1> 1 — 4 TMDS_CONN_DN<1> 57
54 TMDS_DP<1> 2 — 3 TMDS_CONN_DP<1> 57

CRITICAL L7002 90-OHM-300mA 2012H SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_DN<2> 1 — 4 TMDS_CONN_DN<2> 57
54 TMDS_DP<2> 2 — 3 TMDS_CONN_DP<2> 57

CRITICAL L7006 370-OHM SM SYM_VER-1 — TMDS_EXT&TMDS_DUAL
54 TMDS_CLKP 1 — 4 TMDS_CONN_CLKP 2 57
54 TMDS_CLKN 2 — 3 TMDS_CONN_CLKN 57

CRITICAL L7003 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<3> 1 — 4 TMDS_CONN_DN<3> 57
55 TMDS_DP<3> 2 — 3 TMDS_CONN_DP<3> 57

CRITICAL L7004 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<4> 1 — 4 TMDS_CONN_DN<4> 57
55 TMDS_DP<4> 2 — 3 TMDS_CONN_DP<4> 57

CRITICAL L7005 90-OHM-300mA 2012H SYM_VER-1 — TMDS_DUAL
55 TMDS_DN<5> 1 — 4 TMDS_CONN_DN<5> 57
55 TMDS_DP<5> 2 — 3 TMDS_CONN_DP<5> 57

DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)

CRITICAL F7010 0.5AMP-13.2V SM-LF
10 =PP5V_RUN_DVI_DDC 1 — 2 PP5V_RUN_DDC_FUSE VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

L7010 400-OHM-EMI SM-1
1 — 2 PP5V_RUN_DDC 57 VOLTAGE=5V MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm

Isolation required for DVI power switch

D7010 SOD-123
B0530WXF
R7010[1] 4.7K 5% 1/16W MF-LF 402 2

PP5V_RUN_DDC_PULLUPS VOLTAGE=5V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

[1]R7012 4.7K 5% 1/16W MF-LF 402 2

3V LEVEL SHIFTERS

Q7011 2N7002DW-X-F SOT-363
R7011 100 5% 1/16W MF-LF 402 — 1 — 2 DVI_DDC_CLK — D — S 4 — GPU_DVI_DDC_CLK 51
[1]R7020 10K 5% 1/16W MF-LF 402 2
57 10 =PP3V3_DDC_DVI

[1]C7011 100pF 5% 50V CERM 402 2

Q7011 2N7002DW-X-F SOT-363
R7013 100 5% 1/16W MF-LF 402 — 1 — 2 DVI_DDC_DATA — D — S 1 — GPU_DVI_DDC_DATA 51
[1]R7021 10K 5% 1/16W MF-LF 402 2

[1]C7013 100pF 5% 50V CERM 402 2

Q7014 2N7002DW-X-F SOT-363
R7014 100 5% 1/16W MF-LF 402 — 1 — 2 DVI_HPD — D — S 4 — GPU_DVI_HPD 51
[1]R7022 100K 5% 1/16W MF-LF 402 2

NOTE: Pulldown for DVI_HPD provided by DVI power switch interface

CRITICAL J7000 QH81127-CK1 F-RT-TH-LF 36

33 — 31 =GND_CHASSIS_DVI1 2

57 TMDS_CONN_DN<0>	17	1	TMDS_CONN_DN<2> 57
		9	TMDS_CONN_DN<1>
57 TMDS_CONN_DP<0>	18	2	TMDS_CONN_DP<2> 57
		10	TMDS_CONN_DP<1> 57
	19	3	
57 TMDS_CONN_DN<5>	20	4	TMDS_CONN_DN<4> 57
		12	TMDS_CONN_DN<3> 57
57 TMDS_CONN_DP<5>	21	5	TMDS_CONN_DP<4> 57
		13	TMDS_CONN_DP<3> 57
	22	6	57 DVI_DDC_CLK_UF
		14	(PP5V_RUN_DDC)
57 2 TMDS_CONN_CLKP	23	7	DVI_DDC_DATA_UF
		15	
57 TMDS_CONN_CLKN	24	8	VGA_VSYNC 57
		16	57 DVI_HPD_UF
57 53 VGA_B	C3	C1	VGA_R 53 57
	C5B	C5A	
57 VGA_HSYNC	C4	C2	VGA_G 53 57

34 — 32 — 35 =GND_CHASSIS_DVI2 2

C7010 0.01uF 20% 50V CERM 603 — PLACE NEAR C5A & C5B
R7030 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI3 2
R7031 0 5% 1/16W MF-LF 402 — =GND_CHASSIS_DVI4 2
PLACE NEAR 3, 11 & 19

C7014 100pF 5% 50V CERM 402 2

VGA SYNC BUFFERS

C7050 0.1uF 20% 10V CERM 402
57 10 =PP3V3_PWRON_VGASYNC

U7050 74AHC1G32 SM-LF
53 GPU_VGA_VSYNC 1 — 2 — 32 — 3 — 4 GPU_VSYNC_BUF
R7050 33 5% 1/16W MF-LF 402 — VGA_VSYNC 57

PLACE R7050 & R7051 CLOSE TO DVI CONNECTOR

C7051 0.1uF 20% 10V CERM 402
57 10 =PP3V3_PWRON_VGASYNC

U7051 74AHC1G32 SM-LF
53 GPU_VGA_HSYNC 1 — 2 — 32 — 3 — 4 GPU_HSYNC_BUF
R7051 33 5% 1/16W MF-LF 402 — VGA_HSYNC 57

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

FL7040 LCFILTER CRITICAL SM-220MHZ-LF
53 GPU_VGA_B 1 — 2 — 3 4 — VGA_B 53 57
C7040 3.3pF 0.25% 50V CERM 402
[1]R7040 75 1% 1/16W MF-LF 402 2 NO STUFF

FL7041 LCFILTER CRITICAL SM-220MHZ-LF
53 GPU_VGA_G 1 — 2 — 3 4 — VGA_G 53 57
C7041 3.3pF 0.25% 50V CERM 402
[1]R7041 75 1% 1/16W MF-LF 402 2 NO STUFF

FL7042 LCFILTER CRITICAL SM-220MHZ-LF
53 GPU_VGA_R 1 — 2 — 3 4 — VGA_R 53 57
C7042 3.3pF 0.25% 50V CERM 402
[1]R7042 75 1% 1/16W MF-LF 402 2 NO STUFF

S-VIDEO/COMP OUT INTERFACE

Place GND shorts at graphics controller

XW7060 SM
L7060 FERR-10-OHM-500MA SM
GND_GPU_TV1 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7060 0.01uF 20% 50V CERM 603

L7062 3.3uH 0603
53 GPU_TV_Y — TV_Y 53
C7062 560pF 10% 50V CERM 402
C7063 560pF 10% 50V CERM 402

L7064 3.3uH 0603
53 GPU_TV_C — TV_C 53
C7064 560pF 10% 50V CERM 402
C7065 560pF 10% 50V CERM 402

L7066 3.3uH 0603
53 GPU_TV_COMP — TV_COMP 53
C7066 560pF 10% 50V CERM 402
C7067 560pF 10% 50V CERM 402

CRITICAL J7060 MINIDIN RT-TH-LF MH11773-MR8A-7F
4 3 2 1 5 8 10 9 11

Q16C/514-0265/MH11773-MR8A-7F
Q41C/514-0256/MH11773-MR8N-7F

XW7061 SM
L7061 FERR-10-OHM-500MA SM
GND_GPU_TV2 VOLTAGE=0V MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm

C7061 0.01uF 20% 50V CERM 603

Place GND shorts at graphics controller

2 =GND_CHASSIS_TV

DVI POWER SWITCH

Power key detect path when system is shutdown or asleep.. DDC_CLK is isolated from GPU during shutdown. When power key on remote device is pressed, 5V will be driven into DDC_CLK. Since host rails will be low, TP0610 will turn on, driving SYS_POWER_BUTTON_L low. As host rails rise, TP0610 will turn off, as will remote device path into DDC_CLK. Isolation will be disabled as well.

57 PP5V_RUN_DDC
Q7081 TP0610 SOT23-3
57 DVI_DDC_CLK_UF 2 — S D 3 — DVI_TURN_ON
R7081 680 5% 1/16W MF-LF 402 — DVI_TURN_ON_ILIM
R7083 10K 5% 1/16W MF-LF 402 — DVI_TURN_ON_BASE
Q7080 MMDT3904XF SOT-363-LF
SYS_POWER_BUTTON_L 24 25 30 36
R7082[1] 330 5% 1/16W MF-LF 402 2
Pulldown prevents 3904 from turning on when DVI monitor has active, self-powered DDC clock pullup.

57 10 =PP3V3_DDC_DVI
C7070 0.1uF 20% 10V CERM 402
R7072[1] 68.1K 1% 1/16W MF-LF 402 2

Power key detect path when system is running. HPD normally driven to 3.3V. When power key on remote device pressed, HPD will be driven to 5V. Comparator output enabled by GPU.

HPD_4V_REF
U7070 LMC7211 SM-LF
57 DVI_HPD_UF 1 — DVI_HPD_DIV 3
HPD_PWR_SW 1 — 3
R7070 10K 1% 1/16W MF-LF 402
R7071[1] 10K 1% 1/16W MF-LF 402 2
R7073[1] 100K 1% 1/16W MF-LF 402 2
10 =PPBUS_DVI_PWRSW

Q7076 2N7002DW-X-F SOT-363
HPD_ON — HPD_ON_RC — HPD_BASE
R7078 330 5% 1/16W MF-LF 402
R7080 20K 5% 1/16W MF-LF 402
Q7080 MMDT3904XF SOT-363-LF
C7079 47UF 20% 6.3V CERM 1210
[1]R7079 68K 5% 1/16W MF-LF 402 2

Q7075 TP0610 SOT23-3
S D G
COMP_ENABLE
R7075[1] 100K 5% 1/16W MF-LF 402 2
R7077[1] 100K 5% 1/16W MF-LF 402 2
COMP_DISABLE

NEED PULL-DOWN BECAUSE THIS SIGNAL IS TRISTATED INITIALLY
Q7076 2N7002DW-X-F SOT-363
51 HPD_PWR_SNS_EN 2
R7076[1] 100K 5% 1/16W MF-LF 402 2

External Display Conns

SYNC_MASTER=N/A — SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 70 OF 115

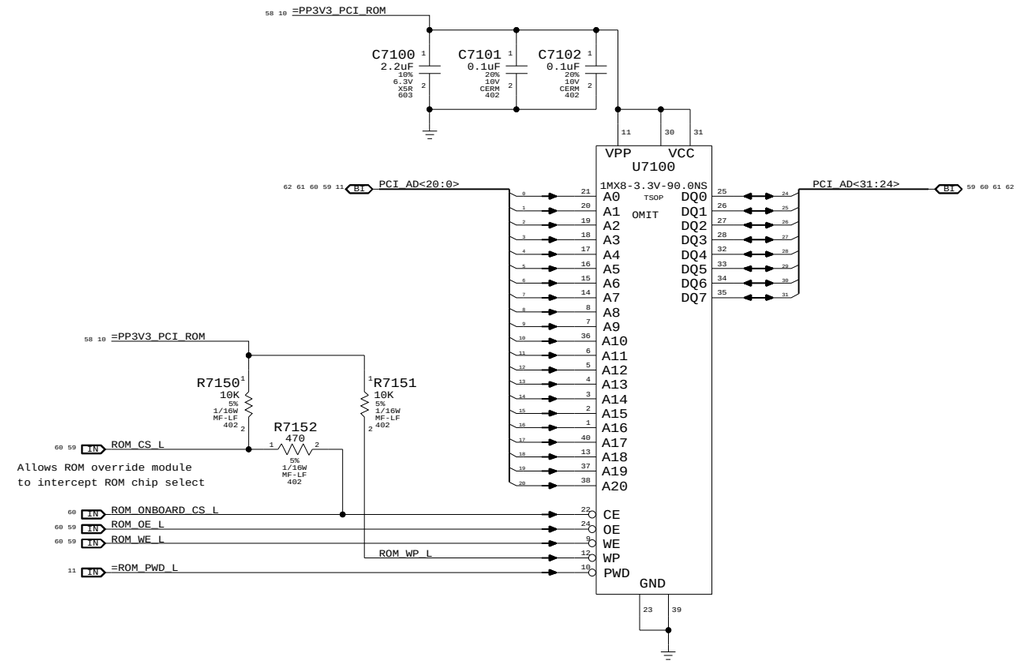
Page Notes

Power aliases required by this page:
- =PP3V3_PCI_ROM

Signal aliases required by this page:
- =ROM_PWD_L

BOM options provided by this page:
(NONE)

NOTE: This page does not specify a
BootROM part number. Must use a
TABLE_x_ITEM symbol to declare
U7100 part number.



BootROM

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE: NONE

SHT 71 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PCI_CLK_SLOTA	CLOCK	CLOCK	
PCI_CLK_SLOTD	CLOCK	CLOCK	
I2_PCI_FBCLK	I2_FBCLK	I2_FBCLK	
	I2_FBCLK	I2_FBCLK	
PCI_AD16_0	PCI	PCI	
PCI_AD17	PCI	PCI	
PCI_AD19_18	PCI	PCI	
PCI_AD20	PCI	PCI	
PCI_AD21	PCI	PCI	
PCI_AD23_22	PCI	PCI	
PCI_AD31_24	PCI	PCI	
PCI_CBE	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_CTL	PCI	PCI	
PCI_PAR	PCI	PCI	
	PCI	PCI	
	PCI	PCI	
	PCI	PCI	
	PCI	PCI	

TP_PCI_CLK33M_SLOTA_R 11 59
TP_PCI_CLK33M_SLOTD_R 11 59
I2_PCI_FBCLK_OUT_R 59
I2_PCI_FBCLK_OUT 21 59
PCI_AD<16..0> 58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<17> 11 58 59 60 61 (BOOTROM ADDR/SLOT A IDSEL)
PCI_AD<19..18> 58 59 60 61 62 (BOOTROM ADDR)
PCI_AD<20> 11 58 59 60 61 62 (SLOT D IDSEL)
PCI_AD<21> 11 59 60 61 62 (SLOT E IDSEL)
PCI_AD<23..22> 59 60 61 62 (PCI ONLY)
PCI_AD<31..24> 58 59 60 61 62 (BOOTROM DATA)
PCI_CBE_L<3..0> 59 60 61 62
PCI_FRAME_L 6 59 60 61 62
PCI_DEVSEL_L 59 60 61 62
PCI_IRDY_L 6 59 60 61 62
PCI_TRDY_L 6 59 60 61 62
PCI_STOP_L 6 59 60 61 62
PCI_PAR 59 60 61 62
PCI_SLOTA_REQ_L 11 59
PCI_SLOTA_GNT_L 11 59
PCI_SLOTD_REQ_L 11 59
PCI_SLOTD_GNT_L 11 59

Page Notes

Power aliases required by this page:
- =PP3V3_PCI

Signal aliases required by this page:
- =I2_PCI_FBCLK_IN - PCI feedback clock input. Length should match that of longest clock from I2 to PCI device.

BOM options provided by this page:
(NONE)

OMIT
U2100
I2
BGA
PCI/ROM INTERFACE
(10 of 14)

ROM INTERFACE
ROM_CS_L AP33 → ROM_CS_L 58 60
ROM_OE_L AM31 → ROM_OE_L 58 60
ROM_WE_L AN34 → ROM_WE_L 58 60

PCI DEVICE 0
PCI_CLK_0_H AL25 → TP_PCI_CLK33M_SLOTA_R 11 59
59 11 PCI_SLOTA_REQ_L → AR21 PCI_REQ_0_L
"Slot A" - AD17
PCI_GNT_0_L AL19 → PCI_SLOTA_GNT_L 11 59

PCI DEVICE 1
PCI_CLK_1_H AR27 → TP_PCI_CLK33M_SLOTD_R 11 59
59 11 PCI_SLOTD_REQ_L → AT20 PCI_REQ_1_L
"Slot D" - AD20
PCI_GNT_1_L AN21 → PCI_SLOTD_GNT_L 11 59

PCI INTERFACE
62 61 60 59 PCI_PAR → AP28 PCI_PAR_H
62 61 60 59 6 PCI_FRAME_L → AT24 PCI_FRAME_L
62 61 60 59 6 PCI_TRDY_L → AN24 PCI_TRDY_L
62 61 60 59 6 PCI_IRDY_L → AR25 PCI_IRDY_L
62 61 60 59 6 PCI_STOP_L → AP27 PCI_STOP_L
62 61 60 59 PCI_DEVSEL_L → AM25 PCI_DEVSEL_L

PCI_AD_00_H AP31 → PCI_AD<0> 58 59 60 61 62
PCI_AD_01_H AT32 → PCI_AD<1> 58 59 60 61 62
PCI_AD_02_H AT31 → PCI_AD<2> 58 59 60 61 62
PCI_AD_03_H AP30 → PCI_AD<3> 58 59 60 61 62
PCI_AD_04_H AN28 → PCI_AD<4> 58 59 60 61 62
PCI_AD_05_H AT34 → PCI_AD<5> 58 59 60 61 62
PCI_AD_06_H AN30 → PCI_AD<6> 58 59 60 61 62
PCI_AD_07_H AR31 → PCI_AD<7> 58 59 60 61 62
PCI_CBE_0_L AR30 → PCI_CBE_L<0> 59 60 61 62
PCI_AD_08_H AM27 → PCI_AD<8> 58 59 60 61 62
PCI_AD_09_H AM30 → PCI_AD<9> 58 59 60 61 62
PCI_AD_10_H AT28 → PCI_AD<10> 58 59 60 61 62
PCI_AD_11_H AT30 → PCI_AD<11> 58 59 60 61 62
PCI_AD_12_H AN27 → PCI_AD<12> 58 59 60 61 62
PCI_AD_13_H AT27 → PCI_AD<13> 58 59 60 61 62
PCI_AD_14_H AN25 → PCI_AD<14> 58 59 60 61 62
PCI_AD_15_H AR28 → PCI_AD<15> 58 59 60 61 62
PCI_CBE_1_L AT29 → PCI_CBE_L<1> 59 60 61 62
PCI_AD_16_H AP25 → PCI_AD<16> 58 59 60 61 62
PCI_AD_17_H AL22 → PCI_AD<17> 11 58 59 60 61 62
PCI_AD_18_H AT26 → PCI_AD<18> 58 59 60 61 62
PCI_AD_19_H AP24 → PCI_AD<19> 58 59 60 61 62
PCI_AD_20_H AR24 → PCI_AD<20> 11 58 59 60 61 62
PCI_AD_21_H AT25 → PCI_AD<21> 11 59 60 61 62
PCI_AD_22_H AK22 → PCI_AD<22> 59 60 61 62
PCI_AD_23_H AT23 → PCI_AD<23> 59 60 61 62
PCI_CBE_2_L AM24 → PCI_CBE_L<2> 59 60 61 62
PCI_AD_24_H AM21 → PCI_AD<24> 58 59 60 61 62
PCI_AD_25_H AP22 → PCI_AD<25> 58 59 60 61 62
PCI_AD_26_H AN22 → PCI_AD<26> 58 59 60 61 62
PCI_AD_27_H AR22 → PCI_AD<27> 58 59 60 61 62
PCI_AD_28_H AK21 → PCI_AD<28> 58 59 60 61 62
PCI_AD_29_H AL21 → PCI_AD<29> 58 59 60 61 62
PCI_AD_30_H AT22 → PCI_AD<30> 58 59 60 61 62
PCI_AD_31_H AP21 → PCI_AD<31> 58 59 60 61 62
PCI_CBE_3_L AM22 → PCI_AD<3> 59 60 61 62

21 =I2_PCI_FBCLK_IN → AM28 PCI_FB_CLK_IN_H
3.3V IN
PCI_FBCLK_OUT_H AE23 → R7205 33 5% 1/16W MF-LF 402Ω → 59 I2_PCI_FBCLK_OUT_R
3.3V OUT
Output Impedance is about 20 Ohms
1 I2_PCI_FBCLK_OUT 21 59

PCI PULL-UPS

10 =PP3V3_PCI

RP7250 10K 5% 1/16W SM-LF
6 =RP7250P1 1 8
6 =RP7250P2 2 7
6 =RP7250P3 3 6
6 =RP7250P4 4 5

One resistor for each of:
- PCI_FRAME_L
- PCI_TRDY_L
- PCI_IRDY_L
- PCI_STOP_L

R7252 10K 5% 1/16W MF-LF 402
62 61 60 59 PCI_DEVSEL_L 1 2

R7253 10K 5% 1/16W MF-LF 402
22 11 PCI_SLOTA_INT_L 1 2

R7254 10K 5% 1/16W MF-LF 402
22 11 PCI_SLOTD_INT_L 1 2

RP7251 10K 5% 1/16W SM-LF
6 =RP7251P1 1 8
6 =RP7251P2 2 7
6 =RP7251P3 3 6
6 =RP7251P4 4 5

One resistor for each of:
- PCI_SLOTA_GNT_L
- PCI_SLOTA_REQ_L
- PCI_SLOTD_GNT_L
- PCI_SLOTD_REQ_L

SLOT E REQ/GNT pull-ups
not provided by this page.

I2 PCI Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 72 OF 115	

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
R315	CLOCK	CLOCK	

=PCI_CLK33M_AIRPORT 11 60

Page Notes

Power aliases required by this page:
- =PP3V3_PCI (802.11g Power)
- =PP3V3_PWRON_BT (Bluetooth Power)

Signal aliases required by this page:
- =PCI_CLK33M_AIRPORT (33MHz PCI clock)
- =PCI_AIRPORT_RESET_L (PCI Reset)
- =USB_BT_P (Bluetooth USB D+)
- =USB_BT_N (Bluetooth USB D-)

BOM options provided by this page:
(NONE)

PCI Devices implemented on this page:
AD17 (Slot "A") - AirPort (0x????/0x????)

NOTE: This AirPort implementation does not support PME#.

CRITICAL
J7300
QT510806-L111-7F
F-ST-SM

10 =PP3V3_PWRON_BT

62 61 59 58 PCI_AD<30>
62 61 59 58 PCI_AD<27>
11 =PCI_AIRPORT_REQ_L
62 61 59 58 PCI_AD<25>
62 61 59 58 PCI_AD<29>
62 61 59 PCI_CBE_L<3>
62 61 59 58 PCI_AD<26>
62 61 59 PCI_AD<22>
PCI_AIRPORT_IDSEL
62 61 59 58 PCI_AD<19>
62 61 59 11 PCI_AD<21>
62 61 59 6 PCI_IRDY_L
62 61 59 58 PCI_AD<18>
62 61 59 PCI_DEVSEL_L
62 61 59 58 PCI_AD<16>
62 61 59 6 PCI_STOP_L
62 61 59 58 PCI_AD<12>
62 61 59 PCI_PAR
62 61 59 58 PCI_AD<8>
62 61 59 58 PCI_AD<9>
62 61 59 PCI_CBE_L<0>
62 61 59 58 PCI_AD<7>
62 61 59 58 PCI_AD<3>
62 61 59 58 PCI_AD<6>
62 61 59 58 PCI_AD<1>
62 61 59 58 PCI_AD<5>
62 61 59 58 PCI_AD<0>
58 ROM_ONBOARD_CS_L
59 58 ROM_CS_L

84 81 83 82

=PP3V3_PCI_AIRPORT 10

PCI_AD<31> 58 59 61 62
AIRPORT_CLKRUN_L_PD
TP_AIRPORT_PME_L
=PCI_AIRPORT_GNT_L 11
PCI_AD<24> 58 59 61 62
=PCI_AIRPORT_RESET_L 11
PCI_AD<28> 58 59 61 62
PCI_AD<23> 59 61 62
PCI_AD<20> 11 58 59 61 62
PCI_FRAME_L 6 59 61 62
PCI_AD<17> 11 58 59 61 62
PCI_TRDY_L 6 59 61 62
PCI_CBE_L<2> 59 61 62
=PCI_CLK33M_AIRPORT 11 60
NC
PCI_AD<14> 58 59 61 62
PCI_AD<13> 58 59 61 62
PCI_AD<10> 58 59 61 62
PCI_AD<15> 58 59 61 62
TP_AIRPORT_ALT_ANTENNA
PCI_CBE_L<1> 59 61 62
PCI_AD<4> 58 59 61 62
PCI_AD<11> 58 59 61 62
ROM_WE_L 58 59
PCI_AD<2> 58 59 61 62
=PCI_AIRPORT_INT_L 11
ROM_OE_L 58 59
USB_BT_P 11
USB_BT_N 11

R7300
22
5%
1/16W
MF-LF
402
11 =PCI_AIRPORT_IDSEL

R7305
10K
5%
1/16W
MF-LF
402

Q85 Connector
Q16C/516S0361/F-ST-SM
Q41C/516S0352/M-ST-SM-LF

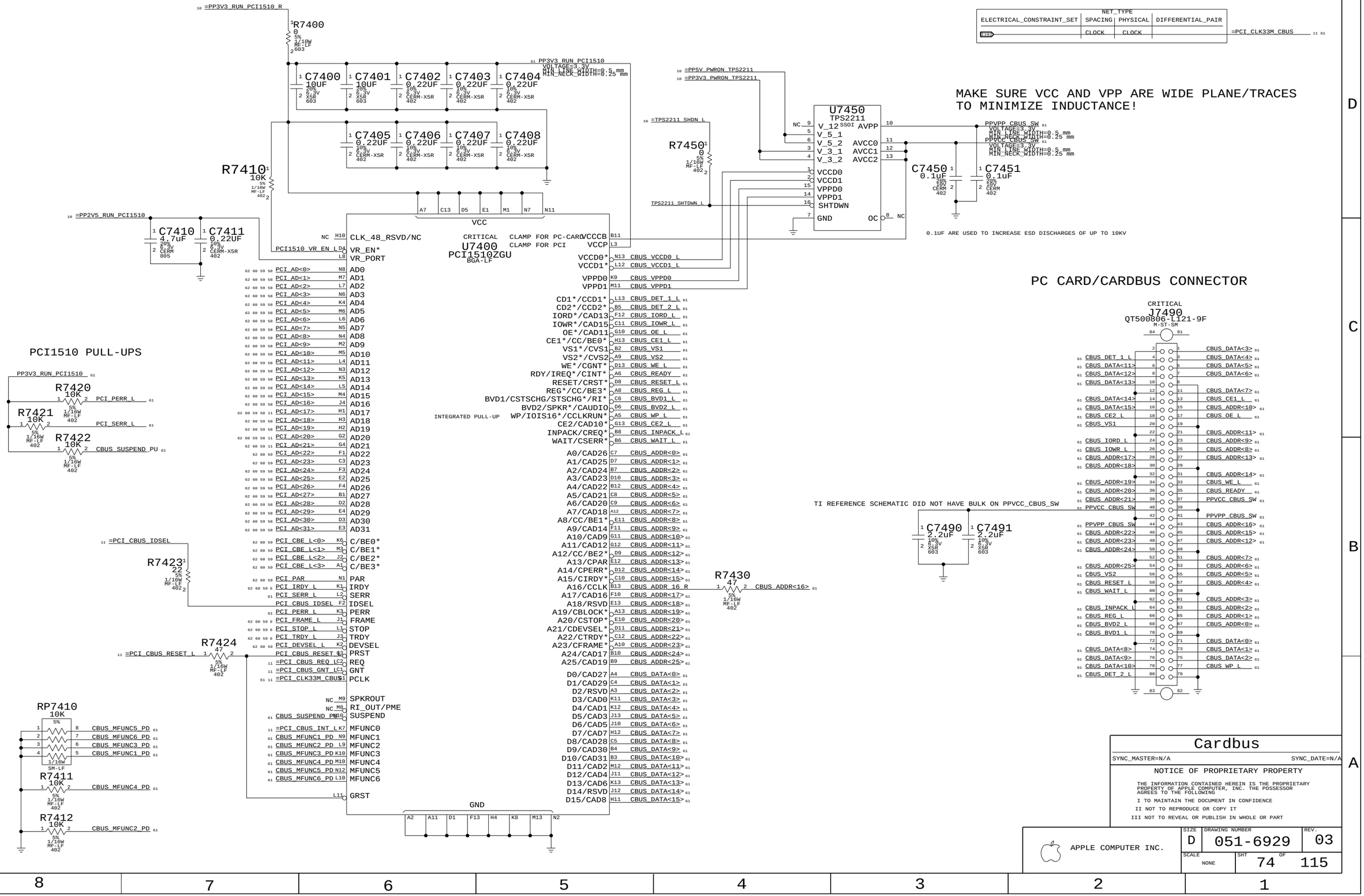
Q85 Airport/BT Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	73	115


NET_TYPE
ELECTRICAL_CONSTRAINT_SET | SPACING | PHYSICAL | DIFFERENTIAL_PAIR
CLOCK | CLOCK
=PCI_CLK33M_CBUS
MAKE SURE VCC AND VPP ARE WIDE PLANE/TRACES TO MINIMIZE INDUCTANCE!
0.1UF ARE USED TO INCREASE ESD DISCHARGES OF UP TO 10KV
TI REFERENCE SCHEMATIC DID NOT HAVE BULK ON PPVCC_CBUS_SW
PCI1510 PULL-UPS
PC CARD/CARDBUS CONNECTOR
U7450 TPS2211
U7400 PCI1510ZGBGA-LF
J7490 QT500806-LI21-9F M-ST-SM
INTEGRATED PULL-UP
R7400 0
R7410 10K
R7423 22
R7424 47
R7430 47
R7450 0
C7400 10UF
C7401 10UF
C7402 0.22UF
C7403 0.22UF
C7404 0.22UF
C7405 0.22UF
C7406 0.22UF
C7407 0.22UF
C7408 0.22UF
C7410 4.7uF
C7411 0.22UF
C7450 0.1uF
C7451 0.1uF
C7490 2.2uF
C7491 2.2uF
RP7410 10K
R7420 10K
R7421 10K
R7422 10K
R7411 10K
R7412 10K
PP3V3_RUN_PCI1510
PP2V5_RUN_PCI1510
=PPSV_PWRON_TPS2211
=PP3V3_PWRON_TPS2211
=TPS2211_SHDN_L
TPS2211_SHTDWN_L
PCI1510_VR_EN_L
=PCI_CBUS_IDSEL
=PCI_CBUS_RESET_L
=PCI_CBUS_REQ_L
=PCI_CBUS_GNT_L
=PCI_CLK33M_CBUS
=PCI_CBUS_INT_L
CBUS_SUSPEND_PU
CBUS_MFUNC1_PD
CBUS_MFUNC2_PD
CBUS_MFUNC3_PD
CBUS_MFUNC4_PD
CBUS_MFUNC5_PD
CBUS_MFUNC6_PD
PPVPP_CBUS_SW
PPVCC_CBUS_SW
VCC
GND
CLK_48_RSVD/NC
VR_EN*
VR_PORT
VCCB
VCCP
VCCD0*
VCCD1*
VPPD0
VPPD1
AD0 AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31
C/BE0* C/BE1* C/BE2* C/BE3*
PAR IRDY SERR IDSEL PERR FRAME STOP TRDY DEVSEL PRST REQ GNT PCLK
SPKROUT RI_OUT/PME SUSPEND
MFUNC0 MFUNC1 MFUNC2 MFUNC3 MFUNC4 MFUNC5 MFUNC6
GRST
CD1*/CCD1* CD2*/CCD2* IORD*/CAD13 IOWR*/CAD15 OE*/CAD11 CE1*/CC/BE0* VS1*/CVS1 VS2*/CVS2 WE*/CGNT* RDY/IREQ*/CINT* RESET/CRST* REG*/CC/BE3* BVD1/CSTSCHG/STSCHG*/RI* BVD2/SPKR*/CAUDIO WP/IOIS16*/CCLKRUN* CE2/CAD10* INPACK/CREQ* WAIT/CSERR*
A0/CAD26 A1/CAD25 A2/CAD24 A3/CAD23 A4/CAD22 A5/CAD21 A6/CAD20 A7/CAD18 A8/CC/BE1* A9/CAD14 A10/CAD9 A11/CAD12 A12/CC/BE2* A13/CPAR A14/CPERR* A15/CIRDY* A16/CCLK A17/CAD16 A18/RSVD A19/CBLOCK* A20/CSTOP* A21/CDEVSEL* A22/CTRDY* A23/CFRAME* A24/CAD17 A25/CAD19
D0/CAD27 D1/CAD29 D2/RSVD D3/CAD0 D4/CAD1 D5/CAD3 D6/CAD5 D7/CAD7 D8/CAD28 D9/CAD30 D10/CAD31 D11/CAD2 D12/CAD4 D13/CAD6 D14/RSVD D15/CAD8
CBUS_DATA<0> CBUS_DATA<1> CBUS_DATA<2> CBUS_DATA<3> CBUS_DATA<4> CBUS_DATA<5> CBUS_DATA<6> CBUS_DATA<7> CBUS_DATA<8> CBUS_DATA<9> CBUS_DATA<10> CBUS_DATA<11> CBUS_DATA<12> CBUS_DATA<13> CBUS_DATA<14> CBUS_DATA<15>
CBUS_ADDR<0> CBUS_ADDR<1> CBUS_ADDR<2> CBUS_ADDR<3> CBUS_ADDR<4> CBUS_ADDR<5> CBUS_ADDR<6> CBUS_ADDR<7> CBUS_ADDR<8> CBUS_ADDR<9> CBUS_ADDR<10> CBUS_ADDR<11> CBUS_ADDR<12> CBUS_ADDR<13> CBUS_ADDR<14> CBUS_ADDR<15> CBUS_ADDR<16>
CBUS_VCCD0_L CBUS_VCCD1_L CBUS_VPPD0 CBUS_VPPD1
CBUS_DET_1_L CBUS_DET_2_L CBUS_IORD_L CBUS_IOWR_L CBUS_OE_L CBUS_CE1_L CBUS_VS1 CBUS_VS2 CBUS_WE_L CBUS_READY CBUS_READY CBUS_REG_L CBUS_BVD1_L CBUS_BVD2_L CBUS_WP_L CBUS_CE2_L CBUS_INPACK_L CBUS_WAIT_L
CBUS_ADDR_16_R
CRITICAL
CLAMP FOR PC-CARD
CLAMP FOR PCI
Cardbus
SYNC_MASTER=N/A
SYNC_DATE=N/A
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6929
REV. 03
SCALE NONE
SHT 74 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
	CLOCK	CLOCK	

=PCI_CLK33M_USB2 11 62

Page Notes

Power aliases required by this page:
- =PPVIO_PCI (to 3.3V or 5V)
- =PP3V3_PCI_USB2 (D3cold rail)

Signal aliases required by this page:
- =PCI_CLK33M_USB2
- =PCI_USB2_REQ_L - =PCI_USB2_IDSEL
- =PCI_USB2_GNT_L - =PCI_USB2_RESET_L
- =PCI_USB2_INT_L

BOM options provided by this page:
- USB2_NEC

PCI Devices implemented on this page:
AD27 (Slot "G") - USB2 (0x1033/0x0035)

NOTE: This USB2 implementation supports D3cold.

10 =PPVIO_PCI_USB2

USB2_NEC C7500 0.1uF 20% 10V CERM 402

VDD_PCI

USB2_NEC CRITICAL U7500 NEC_uPD720101_USB2 FBGA-LF

61 60 59 58 PCI_AD<0>	M5	AD0	
61 60 59 58 PCI_AD<1>	P5	AD1	
61 60 59 58 PCI_AD<2>	N5	AD2	
61 60 59 58 PCI_AD<3>	P4	AD3	
61 60 59 58 PCI_AD<4>	N4	AD4	
61 60 59 58 PCI_AD<5>	M3	AD5	
61 60 59 58 PCI_AD<6>	N3	AD6	
61 60 59 58 PCI_AD<7>	M1	AD7	
61 60 59 58 PCI_AD<8>	L2	AD8	
61 60 59 58 PCI_AD<9>	L1	AD9	
61 60 59 58 PCI_AD<10>	K2	AD10	
61 60 59 58 PCI_AD<11>	L3	AD11	
61 60 59 58 PCI_AD<12>	K1	AD12	
61 60 59 58 PCI_AD<13>	K3	AD13	
61 60 59 58 PCI_AD<14>	J2	AD14	
61 60 59 58 PCI_AD<15>	J1	AD15	
61 60 59 58 PCI_AD<16>	F2	AD16	
61 60 59 58 11 PCI_AD<17>	E3	AD17	
61 60 59 58 PCI_AD<18>	E1	AD18	
61 60 59 58 PCI_AD<19>	D3	AD19	
61 60 59 58 11 PCI_AD<20>	D1	AD20	
61 60 59 11 PCI_AD<21>	D2	AD21	
61 60 59 PCI_AD<22>	C2	AD22	
61 60 59 PCI_AD<23>	C1	AD23	
61 60 59 58 PCI_AD<24>	B4	AD24	
61 60 59 58 PCI_AD<25>	A4	AD25	
61 60 59 58 PCI_AD<26>	B5	AD26	
61 60 59 58 PCI_AD<27>	C4	AD27	
61 60 59 58 PCI_AD<28>	A5	AD28	
61 60 59 58 PCI_AD<29>	C5	AD29	
61 60 59 58 PCI_AD<30>	B6	AD30	
61 60 59 58 PCI_AD<31>	A6	AD31	
61 60 59 PCI_CBE_L<0>	M2	CBE0	
61 60 59 PCI_CBE_L<1>	J3	CBE1	
61 60 59 PCI_CBE_L<2>	F1	CBE2	
61 60 59 PCI_CBE_L<3>	C3	CBE3	
61 60 59 PCI_PAR	J4	PAR	
61 60 59 6 PCI_FRAME_L	F3	FRAME	
61 60 59 6 PCI_IRDY_L	F4	IRDY	
61 60 59 6 PCI_TRDY_L	G1	TRDY	
61 60 59 6 PCI_STOP_L	G3	STOP	
PCI_USB2_IDSEL	B3	IDSEL	
61 60 59 PCI_DEVSEL_L	G2	DEVSEL	
11 =PCI_USB2_REQ_L	C6	REQ	
11 =PCI_USB2_GNT_L	D6	GNT	
NEC_PERR_L_PU	H2	PERR	
NEC_SERR_L_PU	H1	SERR OD	
NEC_INTA_L	C7	INTA OD	
NEC_INTB_L	B7	INTB OD	
NEC_INTC_L	A7	INTC OD	
62 11 =PCI_CLK33M_USB2	A8	PCLK	
NEC_VBBRST_L	B8	VBBRST(CHIP RESET)	
NEC_CRUN_L_PD	N6	CRUN	
NEC_PME_L	D9	PME OD	
NEC_VCCRST_L	C9	VCCRST(PCI RESET)	
2 TP_NEC_SMI_L	L6	SMI OD	
NEC_LEGC_PD	L7	LEGC	

IPD NTEST1	M8	TP_NEC_NTEST1	
IPD SMC	M7	TP_NEC_SMC	2
IPD TEB	N7	TP_NEC_TEB	
IPD AMC	P7	TP_NEC_AMC	
IPD TEST	L8	TP_NEC_TEST	
NANDTEST	M10	TP_NEC_NANDTEST	
SRCLK	M9	TP_NEC_SRCLK	2
SRDTA	N9	TP_NEC_SRDATA	
IPD SRMOD	P9	TP_NEC_SRMOD	

11 =PCI_USB2_IDSEL

USB2_NEC R7500 22 5% 1/16W MF-LF 402

10 =PP3V3_PCI_USB2

USB2_NEC R7501 10K 5% 1/16W MF-LF 402

USB2_NEC R7502 10K 5% 1/16W MF-LF 402

11 =PCI_USB2_INT_L

USB2_NEC RP7510 47 5% 1/16W SM-LF

USB2_NEC RP7510 47 5% 1/16W SM-LF

USB2_NEC RP7510 47 5% 1/16W SM-LF

25 22 SYS_WARM_RESET_L

USB2_NEC R7510 47 5% 1/16W MF-LF 402

25 22 SYS_PME_L

USB2_NEC R7511 47 5% 1/16W MF-LF 402

11 =PCI_USB2_RESET_L

USB2_NEC R7512 47 5% 1/16W MF-LF 402

RP7510 & R7510-12 required to facilitate NAND-tree testing

USB2_NEC R7503 4.7K 5% 1/16W MF-LF 402

USB2_NEC R7504 47 5% 1/16W MF-LF 402

NEC USB2

SYNC_MASTER=N/A SYNC_DATE=N/A

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SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 75 OF 115	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
UATA_DD	UATA	UATA		UATA_DD_R<15..8>	2 6 63
UATA_DD7	UATA	UATA		UATA_DD_R<7>	6 63
UATA_DD	UATA	UATA		UATA_DD_R<6..0>	2 6 63
UATA_HOST	UATA	UATA		UATA_DA_R<2..0>	2 6 63
UATA_HOST	UATA	UATA		UATA_CS0_L_R	6 63
UATA_HOST	UATA	UATA		UATA_CS1_L_R	63
UATA_HSTROBE	UATA	UATA		UATA_HSTROBE_R	63
UATA_HOST	UATA	UATA		UATA_STOP_R	63
UATA_HOST_R	UATA	UATA		UATA_DMACK_L_R	63
UATA_HOST_R	UATA	UATA		UATA_RESET_L_R	63
UATA_DSTROBE	UATA	UATA		UATA_DSTROBE_R	63
UATA_DEV_R	UATA	UATA		UATA_DMARQ_R	63
UATA_DEV_R	UATA	UATA		UATA_INTRQ_R	63
	UATA	UATA		UATA_DD<15..0>	6 7 64
	UATA	UATA		UATA_DA<2..0>	6 7 64
	UATA	UATA		UATA_CS0_L	6 7 64
	UATA	UATA		UATA_CS1_L	7 63 64
	UATA	UATA		UATA_HSTROBE	7 63 64
	UATA	UATA		UATA_STOP	7 63 64
	UATA	UATA		UATA_DMACK_L	7 63 64
	UATA	UATA		UATA_RESET_L	7 63 64
	UATA	UATA		UATA_DSTROBE	7 63 64
	UATA	UATA		UATA_DMARQ	7 63 64
	UATA	UATA		UATA_INTRQ	7 63 64

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

OMIT
U2100
I2
BGA
UATA INTERFACE
(11 of 14)

ATA_D_00_H AB6
ATA_D_01_H AB5
ATA_D_02_H AD6
ATA_D_03_H AD5
ATA_D_04_H AD7
ATA_D_05_H AE7
ATA_D_06_H AE8
ATA_D_07_H AD8
ATA_D_08_H AB4
ATA_D_09_H AE1
ATA_D_10_H AD2
ATA_D_11_H AE2
ATA_D_12_H AD4
ATA_D_13_H AA6
ATA_D_14_H AD1
ATA_D_15_H AB7
UATA_DD_R<15..0> 2 6 63

R8151 10K 5% 1/16W MF-LF 402

I2_UATA_VREF
R8100 1K 1% 1/16W MF-LF 402
AA9 ATA_VREF_H

ATA_A_0_H AC1
ATA_A_1_H AB3
ATA_A_2_H AB2
UATA_DA_R<2..0> 2 6 63

63 UATA_DSTROBE_R AA5 ATA_CHRDY_H
63 UATA_INTRQ_R AB1 ATA_INTRQ_H
63 UATA_DMARQ_R Y9 ATA_DMARQ_H

ATA_RST_L AE6 UATA_RESET_L_R 63
ATA_WR_L ABB8 UATA_STOP_R 63
ATA_RD_L AA8 UATA_HSTROBE_R 63
ATA_CS0_L AE3 UATA_CS0_L_R 6 63
ATA_CS1_L AA4 UATA_CS1_L_R 63
ATA_DMACK_L AA7 UATA_DMACK_L_R 63

UATA100 SERIES TERMINATION

PLACE CLOSE TO I2

One resistor for each of:
- UATA_DD<15..0>(_R)
- UATA_DA<2..0>(_R)
- UATA_CS0_L(_R)
- UATA_CS1_L(_R)
(IDE_CS1FX_L)

RP8150 33 5% 1/16W SM-LF
6 =RP8150P1 1 8 =RP8150P8 BI 6
RP8150 33 5% 1/16W SM-LF
6 =RP8150P2 2 7 =RP8150P7 BI 6
RP8150 33 5% 1/16W SM-LF
6 =RP8150P3 3 6 =RP8150P6 BI 6
RP8150 33 5% 1/16W SM-LF
6 =RP8150P4 4 5 =RP8150P5 BI 6
RP8151 33 5% 1/16W SM-LF
6 =RP8151P1 1 8 =RP8151P8 BI 6
RP8151 33 5% 1/16W SM-LF
6 =RP8151P2 2 7 =RP8151P7 BI 6
RP8151 33 5% 1/16W SM-LF
6 =RP8151P3 3 6 =RP8151P6 BI 6
RP8151 33 5% 1/16W SM-LF
6 =RP8151P4 4 5 =RP8151P5 BI 6
RP8152 33 5% 1/16W SM-LF
6 =RP8152P1 1 8 =RP8152P8 BI 6
RP8152 33 5% 1/16W SM-LF
6 =RP8152P2 2 7 =RP8152P7 BI 6
RP8152 33 5% 1/16W SM-LF
6 =RP8152P3 3 6 =RP8152P6 BI 6
RP8152 33 5% 1/16W SM-LF
6 =RP8152P4 4 5 =RP8152P5 BI 6
RP8153 33 5% 1/16W SM-LF
6 =RP8153P1 1 8 =RP8153P8 BI 6
RP8153 33 5% 1/16W SM-LF
6 =RP8153P2 2 7 =RP8153P7 BI 6
RP8153 33 5% 1/16W SM-LF
6 =RP8153P3 3 6 =RP8153P6 BI 6
RP8153 33 5% 1/16W SM-LF
6 =RP8153P4 4 5 =RP8153P5 BI 6
RP8154 33 5% 1/16W SM-LF
6 =RP8154P1 1 8 =RP8154P8 OUT 6
RP8154 33 5% 1/16W SM-LF
6 =RP8154P2 2 7 =RP8154P7 OUT 6
RP8154 33 5% 1/16W SM-LF
6 =RP8154P3 3 6 =RP8154P6 OUT 6
RP8154 33 5% 1/16W SM-LF
6 =RP8154P4 4 5 =RP8154P5 OUT 6

R8160 33 5% 1/16W MF-LF 402 (IDE_CS3FX_L)
63 UATA_CS1_L_R 2 1 UATA_CS1_L OUT 7 63 64
R8161 33 5% 1/16W MF-LF 402
63 UATA_RESET_L_R 1 2 UATA_RESET_L OUT 7 63 64
R8162 22 5% 1/16W MF-LF 402
63 UATA_DMACK_L_R 1 2 UATA_DMACK_L OUT 7 63 64
R8163 22 5% 1/16W MF-LF 402 (IDE_DIOR_L)
63 UATA_HSTROBE_R 1 2 UATA_HSTROBE OUT 7 63 64
R8164 22 5% 1/16W MF-LF 402 (IDE_DIOW_L)
63 UATA_STOP_R 1 2 UATA_STOP OUT 7 63 64
R8165 82 5% 1/16W MF-LF 402
63 UATA_DMARQ_R 1 2 UATA_DMARQ IN 7 63 64
R8166 82 5% 1/16W MF-LF 402 (IDE_IORDY)
63 UATA_DSTROBE_R 1 2 UATA_DSTROBE IN 7 63 64
C8166 10pF 5% 50V CERM 402
R8167 82 5% 1/16W MF-LF 402
63 UATA_INTRQ_R 1 2 UATA_INTRQ IN 7 63 64

I2 UATA Interface

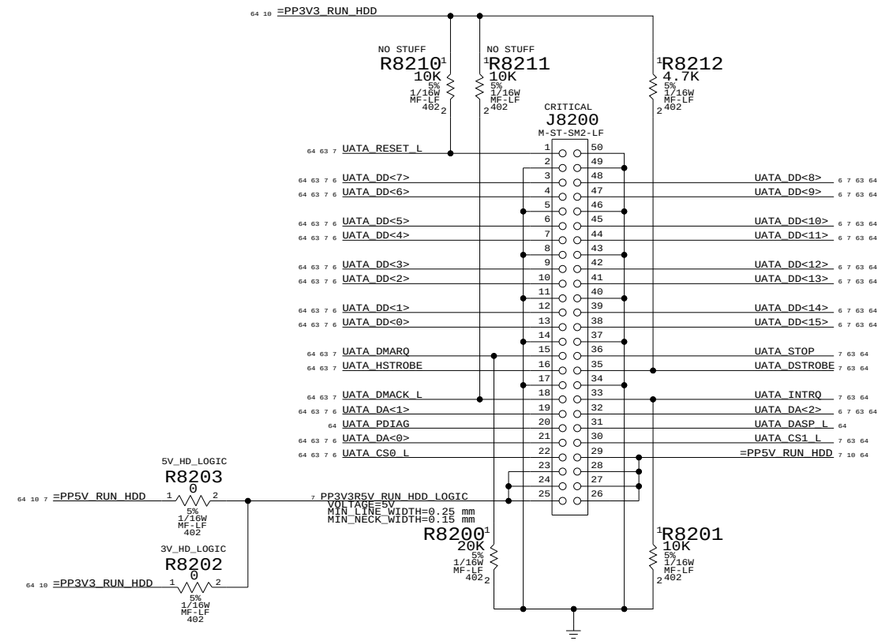
SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

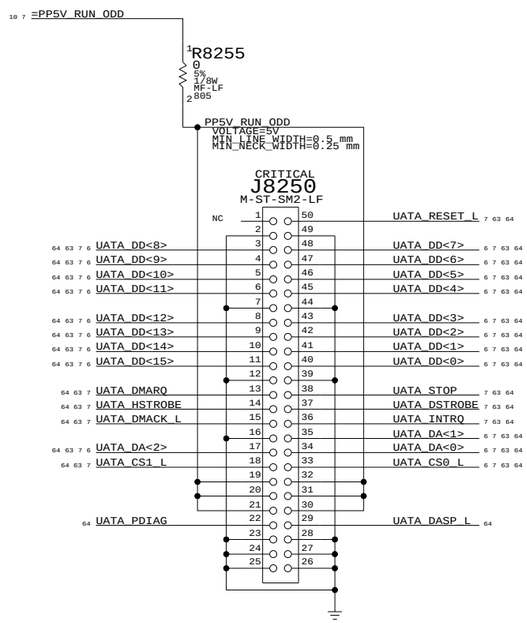
SIZE D | DRAWING NUMBER 051-6929 | REV. 03

SCALE NONE | SHT 81 OF 115

HDD CONNECTOR



ODD CONNECTOR



ATA Connectors

Q16C/516S0357/M-ST-SM2-LF
Q41C/516S0335/M-ST-SM1-LF

HDD/ODD Connectors

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	82	115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
ENET_RX_CLK25M	CLOCK	CLOCK	
ENET_RX_CLK125M	CLOCK	CLOCK	
ENET_GBE_REF	CLOCK	CLOCK	
ENET_TX_CLK	CLOCK	CLOCK	
ENET_RXD3_0	ENET	ENET	
ENET_RXD7_4	ENET	ENET	
ENET_RX_DV	ENET	ENET	
ENET_RX_CTL	ENET	ENET	
ENET_TXD3_0	ENET	ENET	
ENET_TXD7_4	ENET	ENET	
ENET_TX_EN	ENET	ENET	
ENET_TX_ER	ENET	ENET	
ENET_COL	ENET	ENET	
ENET_RX_CTL	ENET	ENET	
ENET_MDC	ENET	ENET	
ENET_MDIO	ENET	ENET	

ENET_CLK25M_TX	11 65
ENET_CLK125M_RX	11 65
ENET_CLK125M_GBE_REF	11 65
ENET_CLK125M_GTX_R	65 66
ENET_RXD<3..0>	9 11 65
ENET_RXD<7..4>	9 11 65
ENET_RX_DV	9 11 65
ENET_RX_ER	9 11 65
ENET_TXD_R<3..0>	11 65
ENET_TXD_R<7..4>	11 65
ENET_TX_EN_R	11 65
ENET_TX_ER_R	11 65
ENET_COL	9 11 65
ENET_CRS	9 11 65
ENET_MDC	9 11 65
ENET_MDIO	9 11 65

Page Notes

Power aliases required by this page:
- =PP2V5R3V3_PWRON_I2_ENET

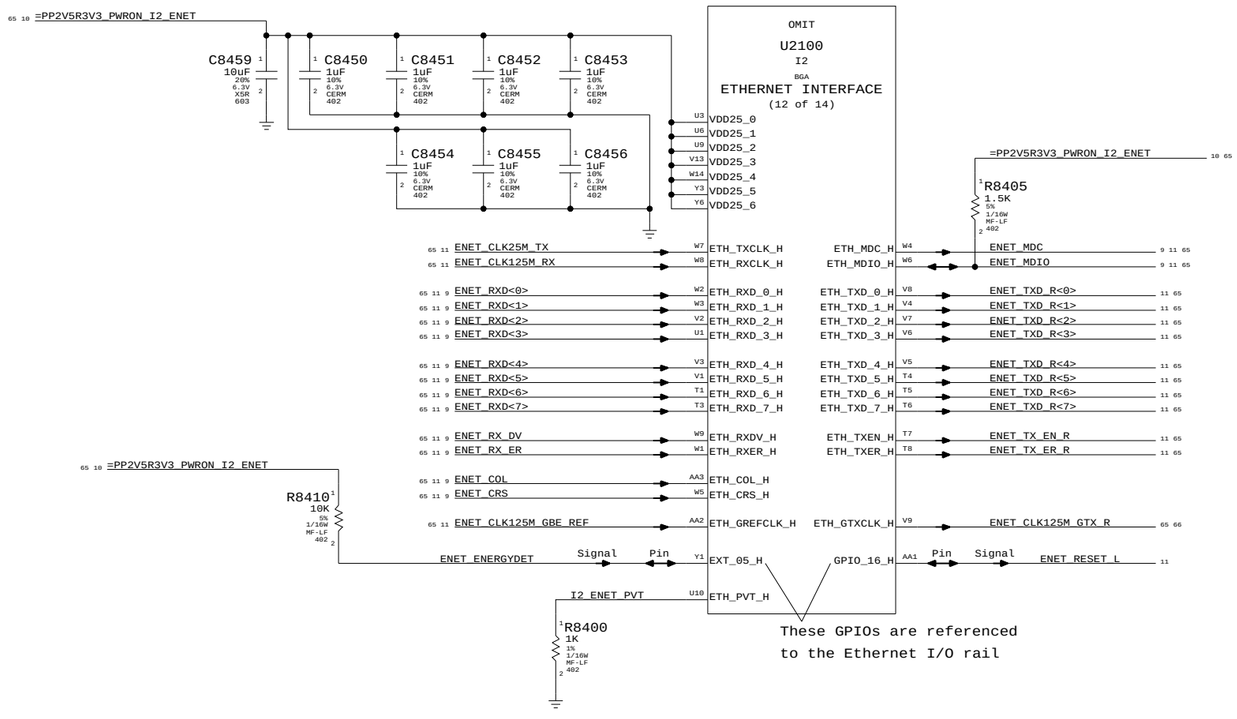
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

NOTE: This page does not provide any series termination. Any termination, including clock signals, should be provided by the PHY page or a non-shared schematic page.

NOTE: All I2 GPIOs should have a pull-up or pull-down resistor. This page does not provide a resistor for GPIO 16. It must be provided by the PHY page or a non-shared schematic page.

NOTE: ENET_RX_DV has a hold spec violation on I2. May want to lengthen net by ~250ps. Net has a unique ECSet name to allow this.



I2 Ethernet Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 84 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_GBE_REF_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK125M_RX_R 66
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		ENET_CLK25M_TX_R 66
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_0	ENETCONN_0_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_1	ENETCONN_1_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_2	ENETCONN_2_N 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_P 66 67
ENETCONN	ENETCONN	ENETCONN	ENETCONN_3	ENETCONN_3_N 66 67
VESTA_CLK25M_XTAL	XTAL	XTAL		VESTA_CLK25M_XTALI 66
	XTAL	XTAL		VESTA_CLK25M_XTALO 66
	XTAL	XTAL		VESTA_CLK25M_XTALO_R 66

Page Notes

Power aliases required by this page:
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Net Spacing Type: ENET_MDI

Line To Line:	0.38 mms
Length Tolerance:	50 mils
Primary Max Sep:	5 mils
Secondary Max Sep:	100 mils
Secondary Length:	500 mils

NOTE: Target differential impedance for ENET data pairs is 100 ohms.

Vesta Ethernet LowPwr

Disables Vesta Ethernet Circuit

=PP3V3_VESTA

R8580 1K 5% 1/16W MF-LF 402

RC time constant not critical. R < 3.9K to counter internal pulldown.

=PP3V3_ENET

Q8580 2N7002DW-X-F SOT-363

Q8580 2N7002DW-X-F SOT-363

C8580 0.1uF 20% 10V CERM 402

VESTA_RESET

Circuit ensures Vesta LOWPWR signal is low when Vesta RESET* is asserted, and allows LOWPWR to assert when ethernet link is unpowered.

Vesta Config Straps:

PHYA<4..0> - PHY Address Select
(Internal Pull-downs)

EN_10B - TBI Interface Select
1 - TBI/RTBI Mode
0 - GMII/RGMII Mode
(Internal Pull-down)

RGMIIEN - RGMII Enable
1 - RGMII/RTBI Mode
0 - GMII/TBI Mode
(Internal Pull-down)

FDX - Full-Duplex Select
Sets manual duplex mode bit
(Internal Pull-up)

F1000 - Speed Select
See table below
(Internal Pull-up)

SPD0 - Speed Select
See table below
(Internal Pull-down)

AN_EN	F1000	SPD0	Description
0	0	0	Force 10BASE-T
0	0	1	Force 100BASE-TX
0	1	X	Force 1000BASE-T (test use only)
1	0	0	Auto-negotiate advertise 10BASE-T
1	0	1	Auto-negotiate advertise 10/100BASE-TX
1	1	0	Auto-negotiate advertise 10/100/1000BASE-T
1	1	1	Auto-negotiate advertise 1000BASE-T

MANMS - Manual Master/Slave Configuration Select
Sets manual master/slave configuration enable bit
(Internal Pull-down)

HUB - Repeater Select
Sets Hub/DTE bit and master/slave configuration value bit
(Internal Pull-down)

ER - Edge Rate Select
1 - Rise time approx. 5 ns
0 - Rise time approx. 4 ns
(Internal Pull-down)

AN_EN - Auto-Negotiation Select
1 - Auto-negotiation enabled
0 - Auto-negotiation disabled
(Internal Pull-up)

TXC_RXC_DELAY
1 - If RGMII Mode enabled, RXC clock and GTXCLK are delayed by 1.9 ns
0 - No clock delay
(Internal Pull-down)

Place close to link

R8569 0 5% 1/16W MF-LF 402

ENET_CLK125M_GTX_R → ENET_CLK125M_GTX → GTXCLK

XTALVDD1 BIASVDD1 PLLVDD1

L8520 FERR-EMI-600-OHM SM =PP2V5_ENETFW

PP2V5_VESTA_XTALVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8520 0.001uF 20% 50V CERM 402

C8521 10UF 20% 6.3V X5R 603

L8510 FERR-EMI-600-OHM SM

PP2V5_VESTA_BIASVDD1 VOLTAGE=2.5V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8510 0.1uF 20% 10V CERM 402

L8530 FERR-EMI-600-OHM SM =PP1V2_ENETFW

PP1V2_VESTA_PLLVDD1 VOLTAGE=1.2V MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm

C8530 0.001uF 20% 50V CERM 402

C8531 10UF 20% 6.3V CERM 1206-1 ESR < 0.5 ohms

OMIT

VESTA ENET U8500 BCM5462 FBGA-200 2 OF 3

=ENET_TXD<0>	B6	TXD[0]
=ENET_TXD<1>	C6	TXD[1]
=ENET_TXD<2>	C7	TXD[2]
=ENET_TXD<3>	D6	TXD[3]
=ENET_TXD<4>	E6	TXD[4]
=ENET_TXD<5>	C5	TXD[5]
=ENET_TXD<6>	B5	TXD[6]
=ENET_TXD<7>	A5	TXD[7]
=ENET_TX_EN	B4	TX_EN
=ENET_TX_ER	C4	TX_ER
=VESTA_MDC	G1	MDC
=VESTA_MDIO	G2	MDIO
VESTA_ENET_LOWPWR	H5	LOWPWR
TP_VESTA_PHYA<0>	L5	PHYA[0]
TP_VESTA_PHYA<1>	L4	PHYA[1]
TP_VESTA_PHYA<2>	L3	PHYA[2]
TP_VESTA_PHYA<3>	L2	PHYA[3]
TP_VESTA_PHYA<4>	L1	PHYA[4]
TP_VESTA_EN_10B	K3	EN_10B
TP_VESTA_RGMIIEN	B8	RGMIIEN
TP_VESTA_FDX	C8	FDX
TP_VESTA_F1000	K4	F1000
TP_VESTA_SPD0	K5	SPD0
TP_VESTA_MANMS	D9	MANMS
TP_VESTA_HUB	A9	HUB
TP_VESTA_ER	H3	ER
TP_VESTA_TEST<0>	M4	TEST[0]
TP_VESTA_TEST<1>	M5	TEST[1]
TP_VESTA_TVCO	N3	TVCO
VESTA_CLK25M_XTALI	N2	XTALI
VESTA_CLK25M_XTALO_R	P2	XTALO

Put crystal circuit close to PHY

R8501 0 5% 1/16W MF-LF 402

CRITICAL Y8500 25.0000M 8X4.5MM-SM2

VESTA_CLK25M_XTALO

C8500 33pF 5% 50V CERM 402

C8501 33pF 5% 50V CERM 402

CRYSTAL LOAD CAPACITANCE IS 20PF

XTALGND BIASGND PLLGND1

CLK125	D1	ENET_CLK125M_GBE_REF_R
TXC	A6	ENET_CLK25M_TX_R
RXC	C1	ENET_CLK125M_RX_R
RXD[0]	F4	=ENET_RXD_R<0>
RXD[1]	F5	=ENET_RXD_R<1>
RXD[2]	E5	=ENET_RXD_R<2>
RXD[3]	E4	=ENET_RXD_R<3>
RXD[4]	E3	=ENET_RXD_R<4>
RXD[5]	D5	=ENET_RXD_R<5>
RXD[6]	D4	=ENET_RXD_R<6>
RXD[7]	D3	=ENET_RXD_R<7>
RX_DV	D2	=ENET_RX_DV_R
RX_ER	C2	=ENET_RX_ER_R
COL	F3	=ENET_COL_R
CRS	G3	=ENET_CRS_R
RBC0	A3	NC? TP_VESTA_RBC0
RBC1	B3	NC? TP_VESTA_RBC1
TRD+[0]	R4	ENETCONN_0_P
TRD-[0]	R5	ENETCONN_0_N
TRD+[1]	R7	ENETCONN_1_P
TRD-[1]	R6	ENETCONN_1_N
TRD+[2]	R8	ENETCONN_2_P
TRD-[2]	R9	ENETCONN_2_N
TRD+[3]	R11	ENETCONN_3_P
TRD-[3]	R10	ENETCONN_3_N
INTR*/ENERGYDET	D10	=VESTA_ENERGYDET
SLAVE*/AN_EN	C10	TP_VESTA_AN_EN
QUALITY*/TXC_RXC_DELAY	A8	TP_VESTA_TXC_RXC_DELAY
LINK1*	A10	TP_VESTA_LINKSPD1_L
LINK2*	B11	TP_VESTA_LINKSPD2_L
FDXLED*	B10	TP_VESTA_FDXLED_L
XMTLED*	B12	TP_VESTA_XMTLED_L
ACTLED*	A11	TP_VESTA_ACTLED_L
RDAC1	R1	VESTA_RDAC1_PD

R8509 1.24K 1% 1/16W MF-LF 402

Place close to PHY

R8560 0 5% 1/16W MF-LF 402 =VESTA_CLK125M_GBE_REF

R8561 0 5% 1/16W MF-LF 402 =VESTA_CLK25M_TX

R8562 0 5% 1/16W MF-LF 402 =VESTA_CLK125M_RX

I2BORG SPECIFIC

Not convention-compliant, '=VESTA_' should be replaced with 'ENET_' (6 nets)

R8590 49.9 1% 1/16W MF-LF 402 — ENET_MDI0

R8591 49.9 1% 1/16W MF-LF 402

R8592 49.9 1% 1/16W MF-LF 402 — ENET_MDI1

R8593 49.9 1% 1/16W MF-LF 402

R8594 49.9 1% 1/16W MF-LF 402 — ENET_MDI2

R8595 49.9 1% 1/16W MF-LF 402

R8596 49.9 1% 1/16W MF-LF 402 — ENET_MDI3

R8597 49.9 1% 1/16W MF-LF 402

C8590 0.01UF 20% 16V CERM 402

C8592 0.01UF 20% 16V CERM 402

C8594 0.01UF 20% 16V CERM 402

C8596 0.01UF 20% 16V CERM 402

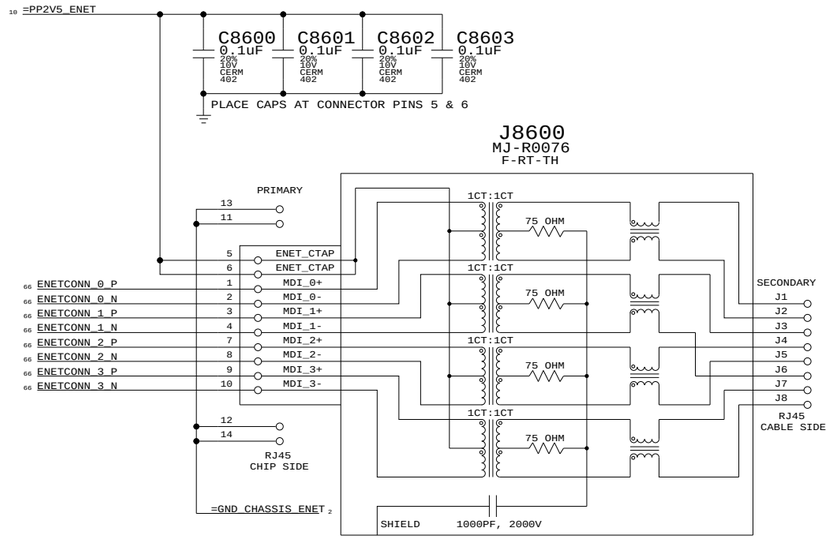
PLACE RESISTORS CLOSE TO PHY

Vesta Ethernet PHY

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 85 OF 115	



Ethernet Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	86	115

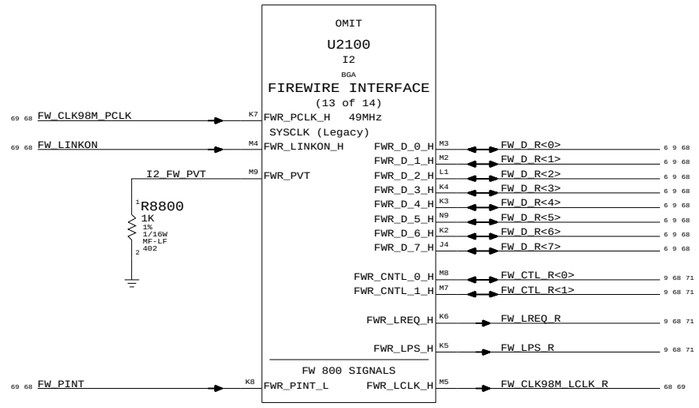
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	DIFFERENTIAL_PAIR		
FW_D_CTL	FW	FW		FW_D_R<7..0>	6 9 68
FW_D_CTL	FW	FW		FW_CTL_R<1..0>	9 68 71
FW_LREQ	FW	FW		FW_LREQ_R	9 68 71
	FW	FW		FW_LPS_R	9 68 71
	FW	FW		FW_LINKON	68 69
FW_PCLK	CLOCK	CLOCK		FW_CLK98M_PCLK	68 69
FW_LCLK	CLOCK	CLOCK		FW_CLK98M_LCLK_R	68 69
FW_PINT	FW	FW		FW_PINT	68 69

Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



I2 FireWire Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	88	115

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
(PROVIDED BY LINK PAGE)	CLOCK	CLOCK		FW_CLK98M_PCLK_R 69
	CLOCK	CLOCK		FW_CLK98M_LCLK 69
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_P 69 70
FW_TPA0	FW_TP	FW_TP	FW_TPA0	FW_TPA0_N 69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_P 69 70
FW_TPB0	FW_TP	FW_TP	FW_TPB0	FW_TPB0_N 69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_P 69 70
FW_TPA1	FW_TP	FW_TP	FW_TPA1	FW_TPA1_N 69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_P 69 70
FW_TPB1	FW_TP	FW_TP	FW_TPB1	FW_TPB1_N 69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_P 69 70
FW_TPA2	FW_TP	FW_TP	FW_TPA2	FW_TPA2_N 69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_P 69 70
FW_TPB2	FW_TP	FW_TP	FW_TPB2	FW_TPB2_N 69 70
VESTA_CLK24M_XTAL	XTAL	XTAL		VESTA_CLK24M_XTALI 69
	XTAL	XTAL		VESTA_CLK24M_XTALO 69
	XTAL	XTAL		VESTA_CLK24M_XTALO_R 69

Page Notes

Power aliases required by this page:
- =PPFW_PHY_CPS
- =PP3V3_FW
- =PP3V3_ENETFW
- =PP2V5_ENETFW
- =PP1V2_ENETFW

Signal aliases required by this page:
- NONE

BOM options provided by this page:
- VESTA_BILINGUAL_EN12
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_DS_ONLY_EN0
  If stuffed, adds external pull-up to counter internal pull-down in Vesta. See straps table for more information.
- VESTA_PORT1_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PORT2_DISABLE
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.
- VESTA_PWR_CLASS_0
  If stuffed, adds external pull-down to counter internal pull-up in Vesta. See straps table for more information.

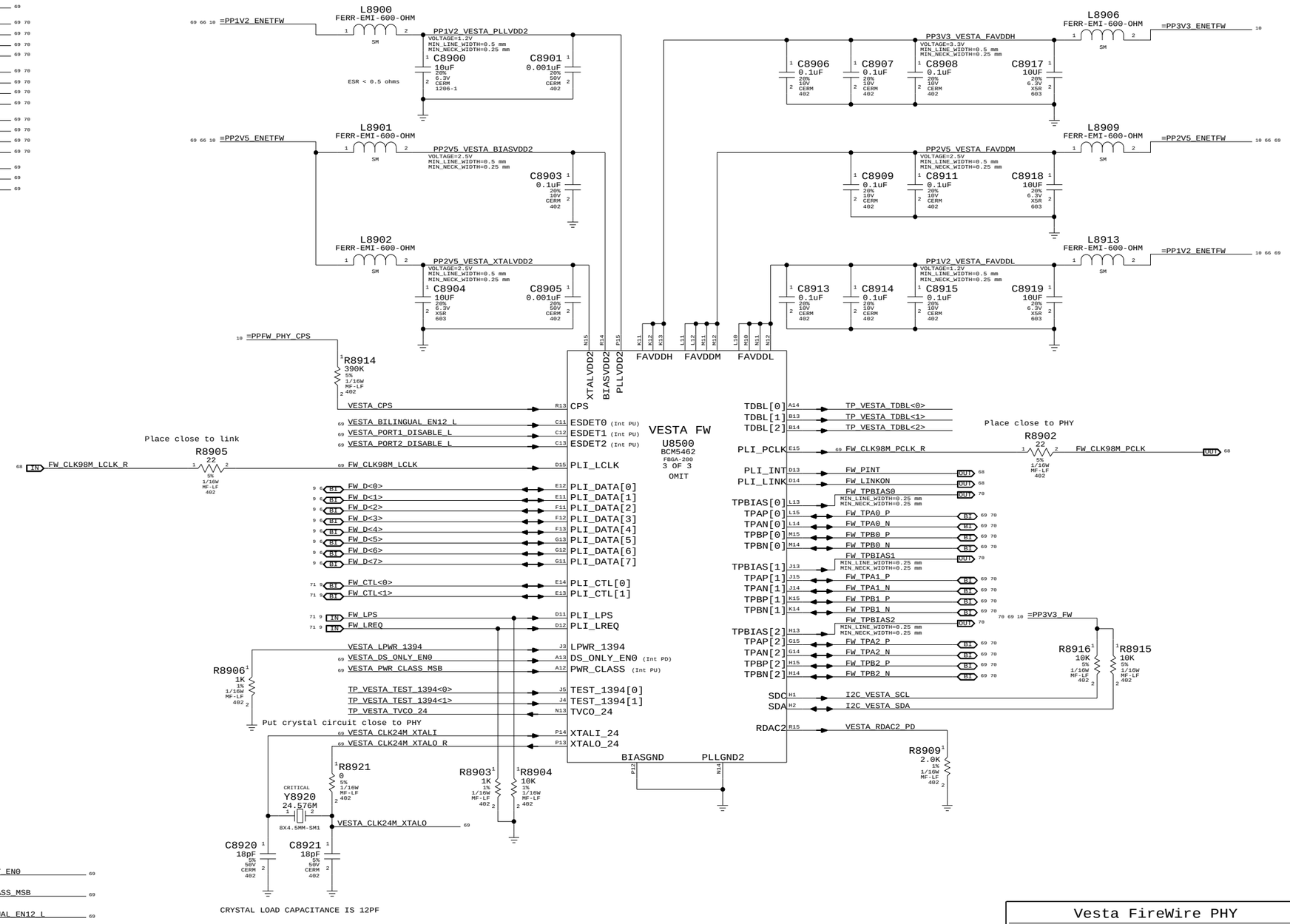
Net Spacing Type: FW_TP

Line To Line: 0.38 mms
Length Tolerance: 100 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for FW data pairs is 110 ohms.

Vesta Config Straps:

DS_ONLY_EN12 - Port 1&2 Data/Strobe
1 - Port 1&2 Data/Strobe mode only
0 - Port 1&2 Bilingual mode
(Internal Pull-up)
DS_ONLY_EN0 - Port 0 Data/Strobe
1 - Port 0 Data/Strobe mode only
0 - Port 0 Bilingual mode
(Internal Pull-down)
PORT1_ENABLE - Port 1 Enable
1 - Port 1 Enabled
0 - Port 1 Disabled (saves power)
(Internal Pull-up)
PORT2_ENABLE - Port 2 Enable
1 - Port 2 Enabled
0 - Port 2 Disabled (saves power)
(Internal Pull-up)
PWR_CLASS - FireWire Power Class
1 - Sets Power Class to 0x4
0 - Sets Power Class to 0x0
(Internal Pull-up)



Vesta FireWire PHY		
SYNC_MASTER=N/A	SYNC_DATE=N/A	
NOTICE OF PROPRIETARY PROPERTY		
THE INFORMATION CONTAINED HEREIN IS THE PROPRIETARY PROPERTY OF APPLE COMPUTER, INC. THE POSSESSOR AGREES TO THE FOLLOWING I TO MAINTAIN THE DOCUMENT IN CONFIDENCE II NOT TO REPRODUCE OR COPY IT III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART		
APPLE COMPUTER INC.	SIZE D / DRAWING NUMBER 051-6929 / REV. 03	SCALE NONE / SHT 89 OF 115

NET_TYPE			
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR
PROVIDED BY PHY PAGE	FW	FW	FW_PORT1_TPA_FL
	FW	FW	FW_PORT1_TPA_FL
	FW	FW	FW_PORT1_TPB_FL
	FW	FW	FW_PORT1_TPB_FL
	FW	FW	FW_PORT2_TPA_FL
	FW	FW	FW_PORT2_TPA_FL
	FW	FW	FW_PORT2_TPB_FL
	FW	FW	FW_PORT2_TPB_FL

FW_PORT1_TPA_P_FL
FW_PORT1_TPA_N_FL
FW_PORT1_TPB_P_FL
FW_PORT1_TPB_N_FL
FW_PORT2_TPA_P_FL
FW_PORT2_TPA_N_FL
FW_PORT2_TPB_P_FL
FW_PORT2_TPB_N_FL

Page Notes

Power aliases required by this page:
- _PPFW_PORT1
- _PPFW_PORT2
- _PPFW_PORT3
- _PP3V3_FW
- _GND_CHASSIS_FW_PORT1
- _GND_CHASSIS_FW_PORT2
- _GND_CHASSIS_FW_PORT3

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

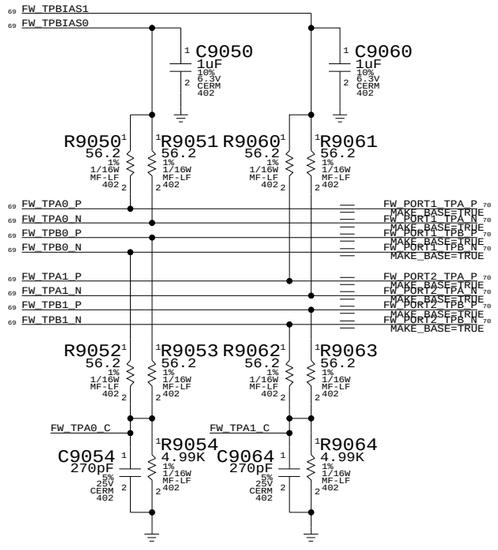
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

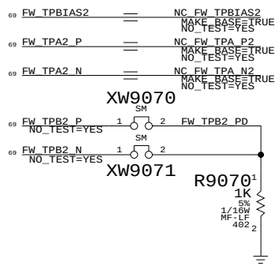
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

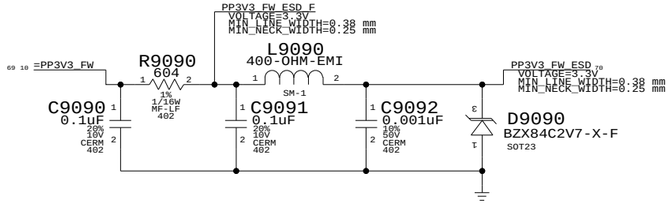
Place close to FireWire PHY



3rd TPA/TPB pair unused

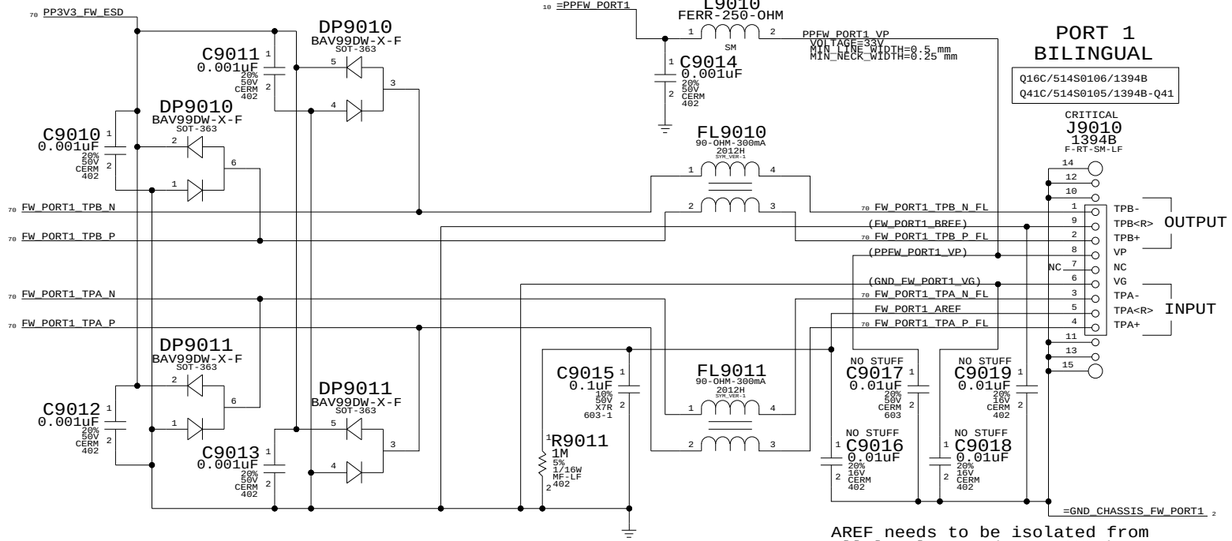


ESD Rail



Cable Power

"Snapback" & "Late VG" Protection

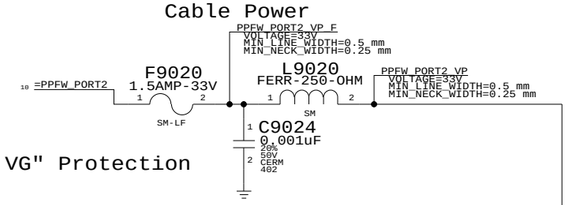


AREF needs to be isolated from all local grounds per 1394b spec

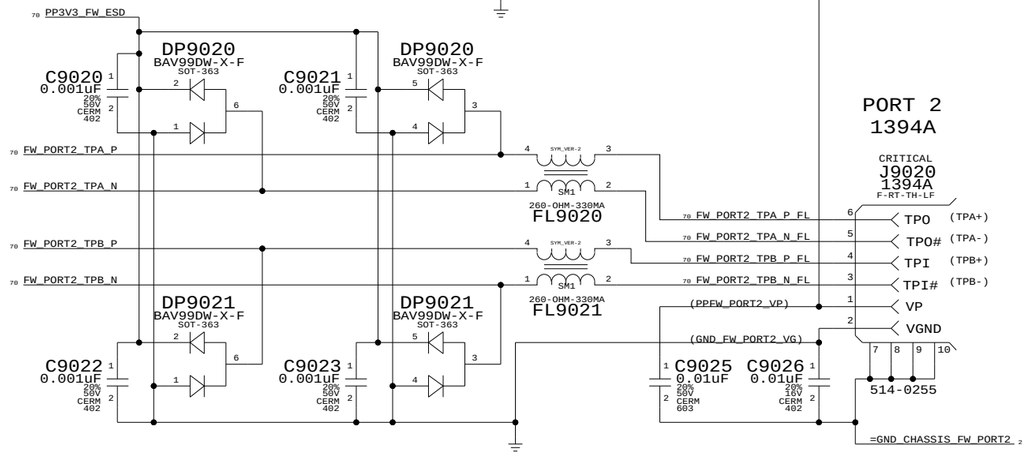
When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection detection currents per 1394b V1.33

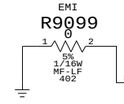
Cable Power



"Snapback" & "Late VG" Protection



EMI



FireWire Ports

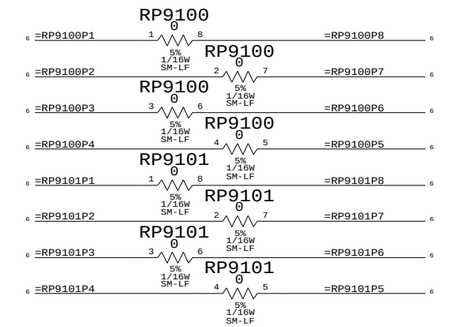
SYNC_MASTER=N/A SYNC_DATE=N/A

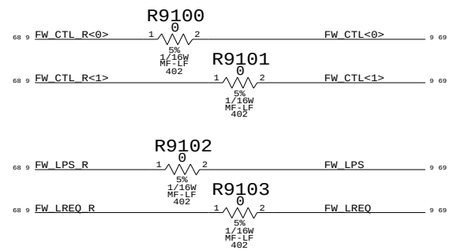
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 90 OF 115	

DRAWING
TITLE=PLASMA
ABBREV=DRAWING
LAST_MODIFIED=Fri Jun 3 15:29:50 2005

Place series terminators approximately halfway between Vesta and NB.
(They should probably be slightly closer to Vesta than the NB.).





FireWire Series Term

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	91	115

ELECTRICAL_CONSTRAINT_SET	NET_TYPE: SPACING	NET_TYPE: PHYSICAL	DIFFERENTIAL_PAIR
USB2_0	USB2	USB2	USB2_I2_0
USB2_0	USB2	USB2	USB2_I2_0
USB2_1	USB2	USB2	USB2_I2_1
USB2_1	USB2	USB2	USB2_I2_1
USB2_2	USB2	USB2	USB2_I2_2
USB2_2	USB2	USB2	USB2_I2_2
USB2_3	USB2	USB2	USB2_I2_3
USB2_3	USB2	USB2	USB2_I2_3
USB2_4	USB2	USB2	USB2_I2_4
USB2_4	USB2	USB2	USB2_I2_4
USB2_5	USB2	USB2	USB2_I2_5
USB2_5	USB2	USB2	USB2_I2_5
USB2_I2_XTAL	XTAL	XTAL	
(USB2_I2_XTAL)	XTAL	XTAL	
(USB2_I2_XTAL)	XTAL	XTAL	

USB2_I2_P<0> 11 72
USB2_I2_N<0> 11 72
USB2_I2_P<1> 6 72
USB2_I2_N<1> 6 72
USB2_I2_P<2> 11 72
USB2_I2_N<2> 11 72
USB2_I2_P<3> 6 72
USB2_I2_N<3> 6 72
USB2_I2_P<4> 11 72
USB2_I2_N<4> 11 72
USB2_I2_P<5> 11 72
USB2_I2_N<5> 11 72
I2_CLK30M_USB2_XOUT_R 72
I2_CLK30M_USB2_XOUT
I2_CLK30M_USB2_XIN 72

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB

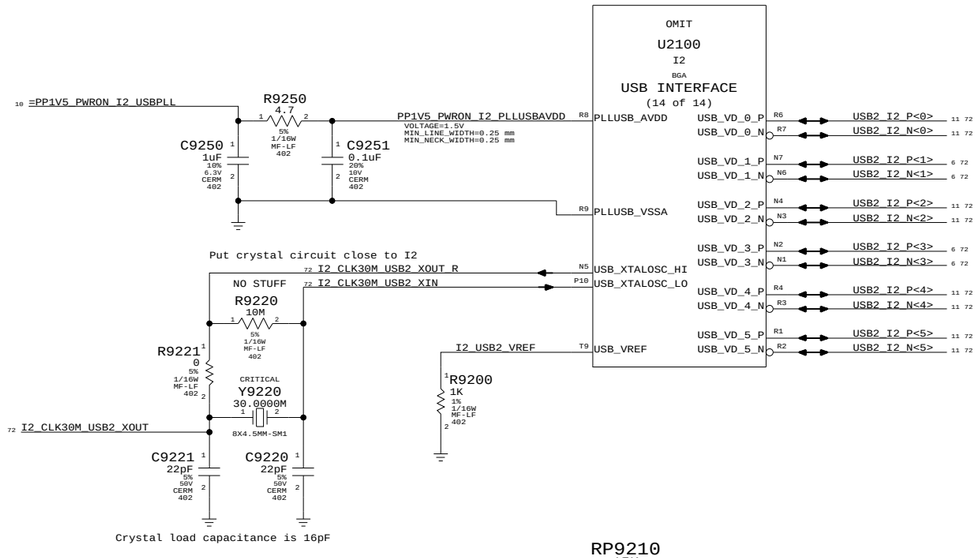
Signal aliases required by this page:
- =RP92xxPy (pinswappable USB pulldowns)

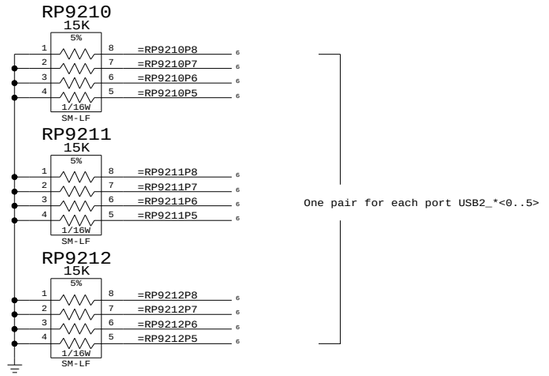
BOM options provided by this page:
(NONE)

Net Spacing Type: USB2

Line To Line: 19.5 mils
Length Tolerance: 50 mils
Primary Max Sep: 7.5 mils
Secondary Max Sep: 100 mils
Secondary Length: 500 mils

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.





I2 USB Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 92 OF 115	

NET_TYPE				
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL	DIFFERENTIAL_PAIR	
J30	USB2	USB2	USB2_NEC_0	USB2_NEC_P<0> 11 73
J31	USB2	USB2	USB2_NEC_0	USB2_NEC_N<0> 11 73
J34	USB2	USB2	USB2_NEC_1	USB2_NEC_P<1> 11 73
J32	USB2	USB2	USB2_NEC_1	USB2_NEC_N<1> 11 73
J33	USB2	USB2	USB2_NEC_2	USB2_NEC_P<2> 11 73
J35	USB2	USB2	USB2_NEC_2	USB2_NEC_N<2> 11 73
J36	USB2	USB2	USB2_NEC_3	USB2_NEC_P<3> 11 73
J37	USB2	USB2	USB2_NEC_3	USB2_NEC_N<3> 11 73
J40	XTAL	XTAL		NEC_CLK30M_XT1 73
J41	XTAL	XTAL		NEC_CLK30M_XT2 73
J42	XTAL	XTAL		NEC_CLK30M_XT2_R 73

ELECTRICAL_CONSTRAINT_SET PROVIDED BY I2 PAGES

Page Notes

Power aliases required by this page:
- =PP3V3_PWRON_USB2

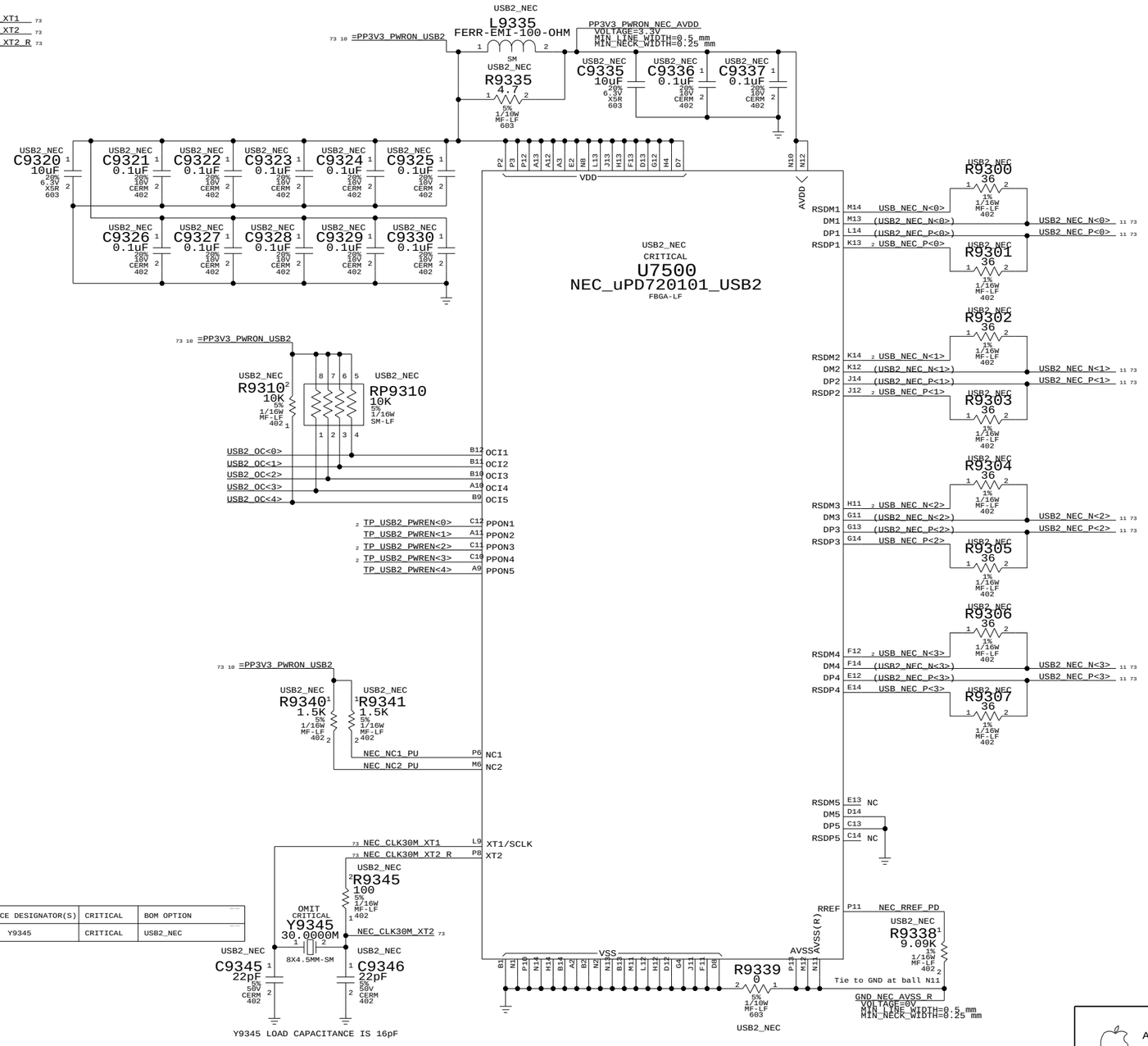
Signal aliases required by this page:
(NONE)

BOM options provided by this page:
USB2_NEC

Net Spacing Type: USB2

NOTE: Target differential impedance for USB2 data pairs is 90 ohms.

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
197S0087	1	XTAL,CER,30.0000MHZ,LW PROF,8X4.5MM,SMD	Y9345	CRITICAL	USB2_NEC



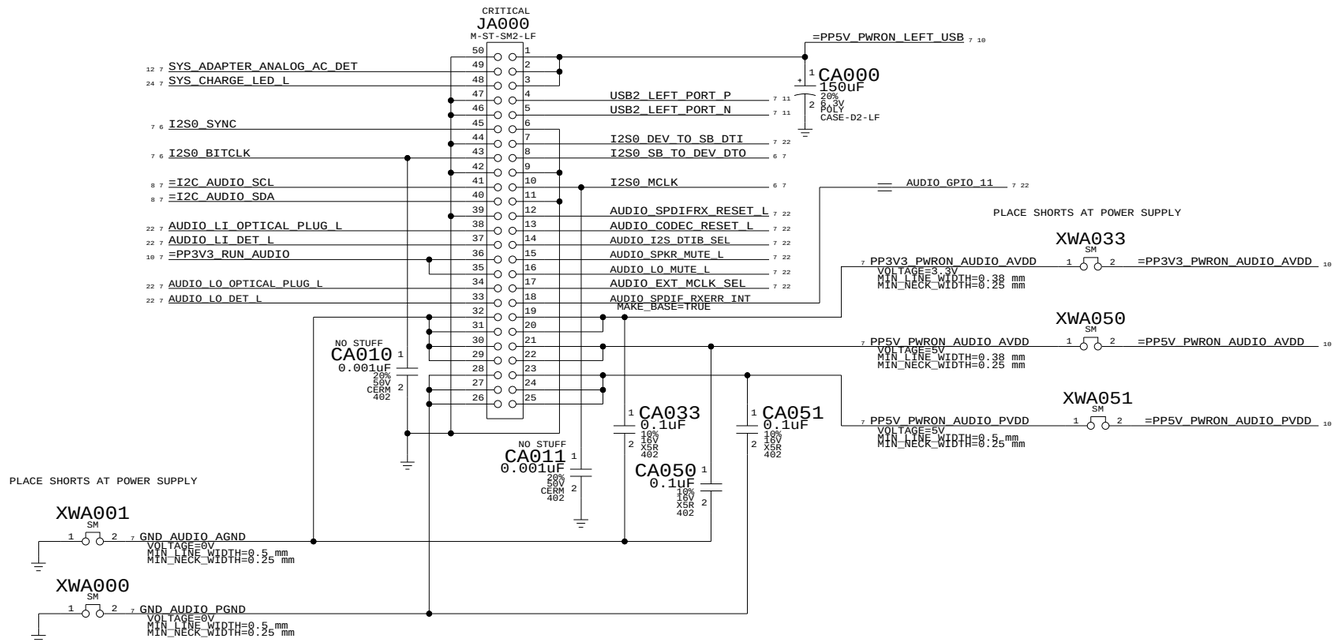
NEC USB2 Interface

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03
SCALE: NONE	SHT 93 OF 115	

AUDIO BOARD & LEFT I/O



Audio Board Connector

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	100	115

AGP

TABLE_SPACING_RULE

TABLE_SPACING_RULE

AGP	401	*	0.4 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_SPACING_RULE

AGP_STB	601	*	0.6 MM	2.5 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

AGP	*	=STANDARD	=60_OHM_SE	=60_OHM_SE	=60_OHM_SE

TABLE_PHYSICAL_RULE

AGP_STB	*	=STANDARD	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

CLOCK

TABLE_SPACING_RULE

TABLE_SPACING_RULE

CLOCK	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

CLOCK	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

ENET (Ethernet Digital)

TABLE_SPACING_RULE

TABLE_SPACING_RULE

ENET_SELF	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	ENET	ENET	*	ENET_SELF

TABLE_SPACING_RULE

ENET	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

ENET	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT

FW (FireWire Digital)

TABLE_SPACING_RULE

TABLE_SPACING_RULE

FW_SELF	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD	FW	FW	*	FW_SELF

TABLE_SPACING_RULE

FW	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

FW	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

I2C

TABLE_SPACING_RULE

TABLE_SPACING_RULE

I2C	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

I2C	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

MaxBus

TABLE_SPACING_RULE

TABLE_SPACING_RULE

MAXBUS	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

MAXBUS	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

PCI

TABLE_SPACING_RULE

TABLE_SPACING_RULE

PCI	=STANDARD	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

PCI	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

RAM

TABLE_SPACING_RULE

TABLE_SPACING_RULE

RAM	201	*	0.2 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_SPACING_RULE

RAM_DIFF	251	*	0.25 MM	2.5 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

RAM	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_PHYSICAL_RULE

RAM_DIFF	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

UATA

TABLE_SPACING_RULE

TABLE_SPACING_RULE

UATA	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

UATA	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

USB2

TABLE_SPACING_RULE

TABLE_SPACING_RULE

USB2	501	*	0.50 MM	3.81 MM	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

USB2	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

AUDIO

TABLE_SPACING_RULE

TABLE_SPACING_RULE

AUDIO	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

AUDIO	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

I2S

TABLE_SPACING_RULE

TABLE_SPACING_RULE

I2S	251	*	0.25 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

I2S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

ENETCONN

TABLE_SPACING_RULE

TABLE_SPACING_RULE

ENETCONN	501	*	0.50 MM	3.81 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

ENETCONN	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

FW_TP

TABLE_SPACING_RULE

TABLE_SPACING_RULE

FW_TP	501	*	0.50 MM	3.81 MM	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

FW_TP	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

I2_FBCLK / XTAL

TABLE_SPACING_ASSIGNMENT

TABLE_SPACING_ASSIGNMENT

I2_FBCLK	*	*	CLOCK

TABLE_SPACING_ASSIGNMENT

XTAL	*	*	CLOCK

TABLE_PHYSICAL_ASSIGNMENT

TABLE_PHYSICAL_ASSIGNMENT

I2_FBCLK	*	CLOCK

TABLE_PHYSICAL_ASSIGNMENT

XTAL	*	CLOCK

Spacing & Physical Constraints

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE	SHT	OF
NONE	110	115

TABLE_SPACING_RULE

TABLE_SPACING_RULE

DVO	151	*	0.15 MM	=STANDARD	=STANDARD	=STANDARD	=STANDARD

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

DVO

DVO	*	=STANDARD	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE

TABLE_SPACING_RULE

TABLE_SPACING_RULE

TV	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_SPACING_RULE

TV_CONN	151	*	=TV	=TV	=TV	=TV	=TV

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

S-VIDEO

TV	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_PHYSICAL_RULE

TV_CONN	*	=TV	=TV	=TV	=TV

TABLE_SPACING_RULE

TABLE_SPACING_RULE

VGA	151	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_SPACING_RULE

VGA_CONN	151	*	=VGA	=VGA	=VGA	=VGA	=VGA

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

VGA

VGA	*	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE

TABLE_PHYSICAL_RULE

VGA_CONN	*	=VGA	=VGA	=VGA	=VGA

TABLE_SPACING_RULE

TABLE_SPACING_RULE

LVDS	151	*		=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

LVDS

LVDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_SPACING_RULE

TABLE_SPACING_RULE

TMDS	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_SPACING_RULE

TMDS_CONN	=TMDS	*	=TMDS	=TMDS	=TMDS	=TMDS	=TMDS

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

TMDS

TMDS	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TMDS_CONN	*	=TMDS	=TMDS	=TMDS	=TMDS

TABLE_SPACING_RULE

TABLE_SPACING_RULE

THERM	251	*	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

TABLE_PHYSICAL_RULE

TABLE_PHYSICAL_RULE

THERM

THERM	*	Y	0.25 MM	=100_OHM_DIFF	=100_OHM_DIFF

Spacing & Physical Constraints 2

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6929	03

SCALE NONE SHT 111 OF 115

8	7	6	5	4	3	2	1

*** Signal Cross-Reference for the entire design ***

```
1V5RUN_EN          16A6< 26B6<
1V5RUN_EN_L        16A4<> 26B4<
1V8_1V5PWRON_EN_L  26D4<
1V20_REF           12C7< 14C8<
1V65_REF           13A5<
1_5V_BOOST         16C6<>
1_5V_BST           16C5<>
1_5V_DH            16C6<>
1_5V_DL            16B6<>
1_5V_FB            16B7<
1_5V_ILIM          16C5<>
1_5V_LX            16B5<>
1_8V_BOOST         16C4<>
1_8V_BST           16C5<>
1_8V_DH            16C3<>
1_8V_DL            16B3<>
1_8V_FB            16B4<
1_8V_ILIM          16C5<>
1_8V_LX            16B3<>
1_8V_PVDD_STD      51C1<
2V5PWRON_EN_L      26D4<
2V5RUN_EN_L        17A5<> 26C6<
3V3RUN_EN_L        15B3<> 26C5<
3V_BG              15C4<>
3V_BOOST           15C5<>
3V_BOOST_ESR       15D3<>
3V_ITH             15C4<>
3V_ITH_RC          15C3<>
3V_PMU_VTAP        14B3<
3V_RSNS            15D2<
3V_RUNSS           15C4<
3V_SNSM            15C4<
3V_SNSP            15C4<
3V_SW              15C4<>
3V_TG              15D4<>
3V_VOSNS           15C4<>
5V3V3PWRON_EN_L    26D6<
5V3VPWRON_EN_L_RC  15B6<
5VRUNHD_EN_L       15B5<> 26D5<
5VRUN_EN_L         15A5<> 26D5<
5VTPAD_EN_L        26B5<
5V_BG              15C5<>
5V_BOOST           15C5<>
5V_BOOST_ESR       15D6<>
5V_ITH             15C5<>
5V_ITH_RC          15C6<>
5V_RSNS            15D7<
5V_RUNSS           15C5<
5V_SNSM            15C5<
5V_SNSP            15C5<
5V_SW              15C5<>
5V_TG              15C5<>
5V_VOSNS           15C5<>
1625_BG            14C5<>
1625_BST           14C5<
1625_BST_ESR       14C5<>
1625_COMP          13D2< 14C6<
1625_DIV           14C8<
1625_ENABLE        14D7<>
1625_ENABLE_L      14D7<>
1625_FCB           14C6<
1625_INTVCC        14C5<>
1625_RUNSS         14C6<>
1625_SGND          14B7<>
1625_TG            14C5<>
1625_VFB           14B5<>
1625_VIN           14C5<>
1625_VSW           14C4<>
1772_ACIN          13B5<
1772_ACOK_L        13B5<> 13C4<>
1772_BST           13B4<>
1772_BST_ESR       13C3<
1772_CC1           13B5<>
1772_CCS           13B5<>
1772_CCV           13B5<>
1772_CCV_RC        13B5<
1772_CELLS         13B4<
1772_CLS           13A4<>
1772_CSIN          13B4<>
1772_CSIP          13B4<>
1772_CSSN          13C5<
1772_CSSP          13C5<
1772_DCIN          13B5<
1772_DHI           13B4<>
1772_DLO           13B4<>
1772_DLOV          13B4<>
1772_GND           13A5<>
1772_ICHG          13B5<>
1772_ICTL          13B5<>
1772_IINP          13B5<
1772_LDO           13C4<>
1772_LX            13B4<>
1772_REF           13B5<>
1772_VCTL          13B5<
1778_BG            45C5<>
1778_BST           45C5<>
1778_BST_RC        45C4<>
1778_FCB           45C6<
1778_GND           45B6<>
1778_ION           45C5<
1778_ITH           45C6<>
1778_ITH_RC        2B5< 45C7<
1778_TG            45C5<>
1778_VFB           45C5<
1778_VRNG          2B5< 45C6<
3707_FCB           15C5<
3707_FSET          15C5<
3707_INTVCC        15D5<>
3707_SGND          15C7<>
3707_STBYMD        15C5<>
=1V8_1V5PWRON_EN_L  16C8<> 26D3>
=1V8_1V5PWRON_PGOOD 16C6> 26B8<
=2V5PWRON_EN_L      17C7<> 26D3>
=2V5PWRON_PGOOD     17C4> 26B8<
=5V3V3PWRON_EN_L    15B6< 26D5>
=5V3VPWRON_PGOOD    15C4<> 26B8<
=5VPWRONTPAD_EN_L   15A8<> 26D3>
=ADT7467_THERM_L    11B3> 27C2<
=AGP_GPU_RESET_L    11C7> 44D4<
=AGP_VREF           11C7> 44B2<
=CLK33M_TBEN_SYNC   11D1> 21A5< 21D6<
=CPU0_MAX1717_AB_SEL 11A3> 36A7< 36C7<
=CPU0_VID_AB_SEL    11A3> 36D3<
=CPU_HRESET_L       11B3> 34A8< 34C6< 34D4<
=ENET_COL_R         11A6> 66B3>
=ENET_CRS_R         11A6> 66B3>
=ENET_RXD_R<0>      66C3>
=ENET_RXD_R<7..0>   11A6<
=ENET_RXD_R<1>      66C3>
=ENET_RXD_R<2>      66C3>
=ENET_RXD_R<3>      66C3>
=ENET_RXD_R<4>      66C3>
=ENET_RXD_R<5>      66C3>
=ENET_RXD_R<6>      66C3>
=ENET_RXD_R<7>      66C3>
=ENET_RX_DV_R       11A6> 66C3>
=ENET_RX_ER_R       11A6> 66B3>
=ENET_TXD<0>        66C6<
=ENET_TXD<7..0>     11A6>
=ENET_TXD<1>        66C6<
=ENET_TXD<2>        66C6<
=ENET_TXD<3>        66C6<
=ENET_TXD<4>        66C6<
=ENET_TXD<5>        66C6<
=ENET_TXD<6>        66C6<
=ENET_TXD<7>        66C6<
=ENET_TX_EN         11A6> 66C6<
=ENET_TX_ER         11A6> 66B6<
=FTP_GND            7C5> 7C5< 7C7> 10D2>
=FTP_SLEEP_LED      7C5> 30B3>
=FWPWR_PWRON        16C8<> 26D3>
=GND_CHASSIS_BATTCHGR_HOLE 2C2<> 2C4>
=GND_CHASSIS_DVI1   2D4> 57D3<>
=GND_CHASSIS_DVI2   2D4> 57C3<>
=GND_CHASSIS_DVI3   2D4> 57C2<
=GND_CHASSIS_DVI4   2D4> 57B2<
=GND_CHASSIS_DVI_HOLE 2D2<> 2D4>
=GND_CHASSIS_ENET   2D4> 67B5<>
=GND_CHASSIS_FW_EMI 2D4> 70A1<
=GND_CHASSIS_FW_HOLE 2D2<> 2D4>
=GND_CHASSIS_FW_PORT1 2D4> 70C1<>
=GND_CHASSIS_FW_PORT2 2D4> 70A2<>
=GND_CHASSIS_INVERTER1 2D4> 56D3<
=GND_CHASSIS_INVERTER2 2C4> 56A2<
=GND_CHASSIS_INV_GND_CLIP 2C2<> 2D4>
=GND_CHASSIS_LCD1   2D4> 56C5<>
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=GND_CHASSIS_LCD2   2D4> 56C6<
=GND_CHASSIS_LCD3   2D4> 56B6<
=GND_CHASSIS_LCD4   2D4> 56A5<>
=GND_CHASSIS_SLEEP_LED 2C4> 30A3<
=GND_CHASSIS_TV     2D4> 57A7<
=GPUVCORE_PGOOD     26A8< 45C6>
=GPU_AGP_VREF       11C7> 44B4<
=I2C_ADT7467_SCL    8B1> 27C4<
=I2C_ADT7467_SDA    8B1> 27C4<>
=I2C_AUDIO_SCL      7A7> 8D1> 74C6<>
=I2C_AUDIO_SDA      7A7> 8D1> 74C6<>
=I2C_BATT_SCL       8B4> 12A5<
=I2C_BATT_SDA       8B4> 12A5<>
=I2C_DS1775_SCL     7C5> 8B1> 30C5<>
=I2C_DS1775_SDA     7C5> 8B1> 30C5<>
=I2C_GPU_TMDS_SCL   8A5< 51B3<>
=I2C_GPU_TMDS_SDA   8A5< 51B3<>
=I2C_I2_NB_SCL      8C3< 22C2<
=I2C_I2_NB_SDA      8C3< 22C2<
=I2C_I2_SB_SCL      8D3> 22C2<
=I2C_I2_SB_SDA      8D3> 22B2<
=I2C_PMU_SCL        8C5< 25C5<>
=I2C_PMU_SDA        8C5< 25C5<>
=I2C_PMU_SMB_SCL    8B5< 25C5<>
=I2C_PMU_SMB_SDA    8B5< 25C5<>
=I2C_SI_M_SCL       8A4> 54B6<
=I2C_SI_M_SDA       8A4> 54B6<
=I2C_SI_S_SCL       8A4> 55B6<
=I2C_SI_S_SDA       8A4> 55B6<
=I2C_SODIMM_SCL     8C1> 40A6<> 41A6<>
=I2C_SODIMM_SDA     8C1> 40A6<> 41A6<>
=I2VCORE_PGOOD      26C4> 26B8<
=I2_AGP_FBCLK_IN    21C5> 43A5<
=I2_AGP_VREF        11C7> 43B5<
=I2_MAXBUS_FBCLK_IN 21D1> 32A6<
=I2_PCI_FBCLK_IN    21B5> 59A5<
=I2_STOPCPU_L       11B3> 22A5<
=I2_STOPXTAL_L      11B3> 22A5<
=JTAG_BBANGER_TCK   9D8< 25B5<>
=JTAG_BBANGER_TDI   9D8< 25B5<>
=JTAG_BBANGER_TMS   9D8< 25B5<>
=JTAG_BBANGER_TRST_L 9D8< 25C5<>
=JTAG_CPU0_TCK      9D5> 34D6<
=JTAG_CPU0_TDI      9D6> 34D6<
=JTAG_CPU0_TDO      9D6> 34D6<
=JTAG_CPU0_TMS      9D5> 34D6<
=JTAG_CPU0_TRST_L   9D5> 34D6<
=JTAG_I2_TCK        9B6> 22B5<
=JTAG_I2_TDI        9C6> 22B5<
=JTAG_I2_TDO        9C6> 22B2<
=JTAG_I2_TMS        9B6> 22B5<
=JTAG_I2_TRST_L     9B6> 22A5<
=JTAG_VESTA_TCK     9A6> 18A6<
=JTAG_VESTA_TDI     9A6> 18A6<
=JTAG_VESTA_TDO     9A6> 18A6<
=JTAG_VESTA_TMS     9A6> 18A6<
=JTAG_VESTA_TRST_L  9A6> 18A6<
=MAXBUS_CPU0_CLK    11D4> 33C1< 33D6<
=PCI_AIRPORT_GNT_L  11D1> 60C3<>
=PCI_AIRPORT_IDSEL  11C1> 60C7<
=PCI_AIRPORT_INT_L  11C1> 60B3<>
=PCI_AIRPORT_REQ_L  11D1> 60C5<>
=PCI_AIRPORT_RESET_L 11C1> 60C3<>
=PCI_CBUS_GNT_L     11C1> 61A7<
=PCI_CBUS_IDSEL     11C1> 61B8<
=PCI_CBUS_INT_L     11C1> 61A7<>
=PCI_CBUS_REQ_L     11C1> 61A7<
=PCI_CBUS_RESET_L   11C1> 61A7<
=PCI_CLK33M_AIRPORT 11D1> 60B3<> 60D6>
=PCI_CLK33M_CBUS    11C1> 61A7< 61D1>
=PCI_CLK33M_USB2    11C1> 62B5< 62D6>
=PCI_CLK33M_ZOBOUT_R<0> 11D4< 23B4> 23D6>
=PCI_CLK33M_ZOBOUT_R<1> 11C4< 23B4> 23D6>
=PCI_CLK33M_ZOBOUT_R<2> 11C4< 23B4> 23D6>
=PCI_CLK33M_ZOBOUT_R<3> 11B4< 23B4> 23D6>
=PCI_CLK33M_ZOB_IN  11D1> 23B5< 23D6>
=PCI_USB2_GNT_L     11C1> 62B5<
=PCI_USB2_IDSEL     11B1> 62B6<
=PCI_USB2_INT_L     11B1> 62B7<
=PCI_USB2_REQ_L     11C1> 62B5<
=PCI_USB2_RESET_L   11B1> 62A7<
=PP1V2_ENETFW       10D4> 66D2< 69C1< 69D5<
=PP1V2_VESTA        10D4> 18B7<
=PP1V2_VESTA_REG    10D6< 18C1<
=PP1V05R1V3_GPU_VCORE 10A6> 46D6<
=PP1V5R1V8_I2_MAXBUS 10A1> 32B6< 32D1<
=PP1V5R1V8_MAXBUS   10A1> 21C8< 33A5< 33B8< 33C8<
        34B5< 34D7< 34C4< 34C4< 34D4<
=PP1V5R3V3_DVO_VREF 47C1> 54A2<
=PP1V5_AGP          10A6> 43A5< 43C1< 44B2< 44B7<
        44C6< 47C2<
=PP1V5_GPU          10A1> 10A8<
=PP1V5_GPU_DVO      10A6> 47C2<
=PP1V5_GPU_PWRSEQ   10A6> 52C4<>
=PP1V5_GPU_VDD15    10A6> 46B5<
=PP1V5_I2_AGP       10A4> 43C7<
=PP1V5_PWRON_I2PLL_LDO 10D3< 20B3<>
=PP1V5_PWRON_I2_PLL 10D1> 19C5<
=PP1V5_PWRON_I2_USBPLL 10D1> 72C7<
=PP1V5_PWRON_REG    10A6<> 16B0<
=PP1V5_RUN_RUNFET   10A3< 16A6<>
=PP1V8R2V5_GPU_FB_VIO 10A6> 47C8< 48A8<
=PP1V8_FB_VDD       10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_FB_VDDQ      10A6> 49D5< 49D8< 50D5< 50D8<
=PP1V8_GPU          10A1> 10A8<
=PP1V8_GPU_AVDD     10A6> 53C2<
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=PP3V3_PWRON_I2_MISC 10B5< 22B6< 22C7<
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=PP3V3_PWRON_JTAG_ASIC 9C8< 10B5<
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=PP3V3_PWRON_VDDSPD 10B5< 40A6<> 41A4<> 41A6<>
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AC_DET_DIV          12C7<
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AC_ENABLE_L         12C5<>
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FB_A_DQ_R<39..32>   42C6>
FB_A_DQ_R<47..40>   42C6>
FB_A_DQ_R<55..48>   42C6>
FB_A_DQ_R<63..56>   42C6>
FB_A_RAS_L          48B3> 49A4< 49A7< 49D1>
FB_A_RAS_L_R        42D6> 48B4< 48B6<
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FB_A_WE_L_R         42D6> 48B4< 48B6<
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FB_B_ADDR<11..0>    48D3> 50D1>
FB_B_ADDR<1>        50B4< 50D7
FB_B_ADDR<2>        50B4< 50D7
FB_B_ADDR<3>        50B4< 50D7
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FB_B_ADDR<5>        50B4< 50D7
FB_B_ADDR<6>        50B4< 50D7
FB_B_ADDR<7>        50B4< 50D7
FB_B_ADDR<8>        50B4< 50D7
FB_B_ADDR<9>        50B4< 50D7
FB_B_ADDR<10>       50B4< 50D7
FB_B_ADDR<11>       50B4< 50D7
FB_B_ADDR_R<11..0>  48D4< 48D5<
FB_B_ADDR_R<12..0>  42D6>
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FB_B_BA<1..0>       48C3> 50D1>
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FB_B_BA_R<1..0>     48C4< 48C5>
FB_B_BA_R<2..0>     42B6>
FB_B_CAS_L          48B1< 50A4< 50A7< 50C1>
FB_B_CKE            48B1< 50A4< 50A7< 50D1>
FB_B_CKE_R          42B6> 48B4< 48B5>
FB_B_CLKDDR_0_N     48B1< 50A7< 50D1>
FB_B_CLKDDR_0_N_R   42C6> 48B2< 48B5>
FB_B_CLKDDR_0_P     48B1< 50A7< 50D1>
FB_B_CLKDDR_0_P_R   42C6> 48B2< 48B5>
FB_B_CLKDDR_1_N     48A1< 50A4< 50D1>
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FB_B_CLKDDR_1_P     48B1< 50A4< 50D1>
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FB_B_CS_L_R         42B6> 48B2< 48B5>
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FB_B_DQ<1>          50B5<
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FB_B_DQ_R<63..56>   42A6>
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FB_B_RAS_L_R        42B6> 48B2< 48B5>
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FW_PORT1_TPB_P_FL   70D2<> 70D6<
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FW_PORT2_TPA_N_FL   70A3<> 70D6<
FW_PORT2_TPA_P      70B5<> 70C5<
FW_PORT2_TPA_P_FL   70A3<> 70D6<
FW_PORT2_TPB_N      70A5<> 70C5<
FW_PORT2_TPB_N_FL   70A3<> 70D6<
FW_PORT2_TPB_P      70A5<> 70C5<
FW_PORT2_TPB_P_FL   70A3<> 70D6<
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FW_TPA0_N           69B2< 69D6< 70C7<
FW_TPA0_P           69B2< 69D6< 70C7<
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FW_TPA2_P           69B2< 69D6< 70B7<
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FW_TPB0_P           69B2< 69D6< 70C7<
FW_TPB1_N           69B2< 69D6< 70C7<
FW_TPB1_P           69B2< 69D6< 70C7<
FW_TPB2_N           69B2< 69D6< 70B7<>
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FW_TPBIAS1          69B2> 70D7<
FW_TPBIAS2          69B2> 70B7<
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GND_AUDIO_PGND      7A7> 74B6<>
GND_BATT_CONN       12A7<>
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GND_GPU_TV2         57A8<>
GND_I2VCORE         20C4<>
GND_INVERTER        7B7> 56B2<>
GND_NEC_AVSS_R      73A3<
GND_PMU_AVSS        25A3<> 25D3< 28D3< 29B3< 31B3<
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GND_TV2             57A7<>
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GPU_MEMVMODE1       48A6<
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GPU_MVREFS          48A8<
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GPU_TV_COMP         53B4< 53C1> 57A8<
GPU_TV_Y            53B4< 53C1> 57A8<
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I2C_I2_SB_SDA       8D2< 8D6<
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I2C_PMU_SDA         8C5< 8D6<
I2C_PMU_SMB_SCL     8B5< 8D6<
I2C_PMU_SMB_SDA     8B5< 8D6<
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I2PLLVDD_BYP        20A4<>
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I2S0_BITCLK_R       6D8< 22B2< 22D6<
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I2S0_MCLK_R         6D8< 22B2< 22D6<
I2S0_SB_TO_DEV_DTO  6D6> 7A7< 74C4<>
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112

8	7	6	5	4	3	2	1

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I2_CLK30M_USB2_XOUT  72B7< 72D6>
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I2_MAXBUS_FBCLK_OUT_R  32A4< 32D6>
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JTAG_VESTA_TRST_L  9A8<
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LTC3412_RT       17C5<
LTC3412_RUNSS    2B5> 17C5<>
LTC3412_SW       17C4<>
LTC3412_SYNC     17C5<>
LTC3412_VFB      17C5<>
LTC3412_VFB_DIV  17C5<
LVDS_DDC_CLK     7B7> 51B3<> 56C7<>
LVDS_DDC_DATA    7B7> 51B3<> 56C7<>
LVDS_L0_N        7C7> 53A7> 53D1> 56C5<>
LVDS_L0_P        7C7> 53A7> 53D1> 56C5<>
LVDS_L1_N        7C7> 53A7> 53D1> 56C5<>
LVDS_L1_P        7C7> 53A7> 53D1> 56C5<>
LVDS_L2_N        7C7> 53A7> 53D1> 56B5<>
LVDS_L2_P        7C7> 53A7> 53D1> 56B5<>
LVDS_U0_N        7C7> 53B7> 53D1> 56B5<>
LVDS_U0_P        7C7> 53B7> 53D1> 56B5<>
LVDS_U1_N        7C7> 53B7> 53D1> 56B5<>
LVDS_U1_P        7C7> 53B7> 53D1> 56B5<>
LVDS_U2_N        7C7> 53B7> 53D1> 56B5<>
LVDS_U2_P        7C7> 53B7> 53D1> 56B5<>
MAX1715_EN_L_RC  16C7<>
MAX1715_GND      16B5<> 16C5<
MAX1715_ON       16D6<
MAX1715_REF      16B5<>
MAX1715_SKIP     16C4<
MAX1715_TON      16C5<
MAX4172_OUT      13D5<>
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MAX8860_FAULT_L  52B3<>
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MAXBUS_CLK_TBEN_SYNC  11D5<
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MAXBUS_WT_L      9C3> 32B5< 32C6> 33C1>
MM3120_SW        28B4<>
MMM_ACC_PWRDOWN  25A7> 29C6<>
MMM_ACC_SELFTEST  25A7> 29C6<>
MMM_FFIRQ_L      22B6> 22C5< 25A7>
MMM_SIRQ_L       22C5< 25A7>
MMM_X_AXIS       25A7> 29C3<> 29D6>
MMM_Y_AXIS       25A7> 29C3<> 29D6>
MMM_Z_AXIS       25A7> 29B3<> 29D6>
MODEM_RESET_L    22C5< 30B5<>
MODEM_RING2SYS_L  22D5< 25C5<> 30A7<
NB_SUSPENDACK_L  22A2< 25C5<>
NB_SUSPENDREQ_L  22A5< 25A7< 25C5<>
NC_FW_TPA_N2     70B6>
NC_FW_TPA_P2     70B6>
NC_FW_TPBIAS2    70B6>
NC_MAXBUS_CPU1_QACK_L  11A4>
NEC_CLK30M_XT1   73A5< 73D7>
NEC_CLK30M_XT2   73A5< 73D7>
NEC_CLK30M_XT2_R  73A5<> 73D7>
NEC_CRUN_L_PD    62A5<>
NEC_INTA_L       62B5<>
NEC_INTB_L       62B5<>
NEC_INTC_L       62B5<>
NEC_LEGC_PD      62A5<
NEC_NC1_PU       73A5<>
NEC_NC2_PU       73A5<>
NEC_PERR_L_PU    62B5<>
NEC_PME_L        62A5<>
NEC_RREF_PD      73A3<>
NEC_SERR_L_PU    62B5<>
NEC_VBBRST_L     62A5<
NEC_VCCRST_L     62A5<
OVER_18V_ADJ     13C3<>
PANEL_PWR_EN     53B8<> 56B4<> 56C8<
PCI1510_VR_EN_L  61C7<
PCI_AD<0>        59C3< 60B5<> 61C7<> 62D5<>
PCI_AD<16..0>    59D6>
PCI_AD<20..0>    58C5<>
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PCI_AD<16>       59B3< 60B5<> 61C7<> 62C5<>
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PCI_AD<19>       59B3< 60C5<> 61B7<> 62C5<>
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PCI_AD<23..22>   59D6>
PCI_AD<23>       59B3< 60C3<> 61B7<> 62C5<>
PCI_AD<24>       59B3< 60C3<> 61B7<> 62C5<>
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PCI_AD<25>       59B3< 60C5<> 61B7<> 62C5<>
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PCI_AD<27>       59A3< 60C5<> 61B7<> 62B5<>
PCI_AD<28>       59A3< 60C3<> 61B7<> 62B5<>
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PCI_AD<31>       59A3< 60C3<> 61B7<> 62B5<>
PCI_AIRPORT_GNT_L  6B6< 11D2
PCI_AIRPORT_IDSEL  60C5<>
PCI_AIRPORT_INT_L  11C2
PCI_AIRPORT_REQ_L  6A6< 11D2
PCI_CBE_L<0>     59B3< 60B5<> 61B7<> 62B5<>
PCI_CBE_L<3..0>  59D6>
PCI_CBE_L<1>     59B3< 60B3<> 61B7<> 62B5<>
PCI_CBE_L<2>     59B3< 60B3<> 61B7<> 62B5<>
PCI_CBE_L<3>     59A3< 60C5<> 61B7<> 62B5<>
PCI_CBUS_GNT_L   6A6< 11C2
PCI_CBUS_IDSEL   61B7<
PCI_CBUS_INT_L   11C2
PCI_CBUS_REQ_L   6B6< 11C2
PCI_CBUS_RESET_L  61A7<
PCI_CLK33M_AIRPORT  11D2<
PCI_CLK33M_AIRPORT_R  11D3<
PCI_CLK33M_CBUS  11C2<
PCI_CLK33M_CBUS_R  11C3<
PCI_CLK33M_TBEN_SYNC  11D2<
PCI_CLK33M_TBEN_SYNC_R  11D3<
PCI_CLK33M_USB2  11C2<
PCI_CLK33M_USB2_R  11C3<
PCI_CLK33M_ZDB   11D2<
PCI_CLK33M_ZDB_R  11D3<
PCI_CLK_DELAY_ADJ  23B5<>
PCI_DEVSEL_L     59C5< 59D2< 59D6> 60B5<> 61A7<>
            62B5<>
PCI_FRAME_L      6A6< 59C5< 59D6> 60C3<> 61B7<>
            62B5<>
PCI_IRDY_L       6B6< 59C5< 59D6> 60C5<> 61B7<>
            62B5<>
PCI_PAR          59C5< 59D6> 60B5<> 61B7<> 62B5<>
PCI_PERR_L       61B7<> 61C7<
PCI_RESET_L      11A5< 11B2< 11C2< 11C2< 11C8<
            25A7< 25C2<>
PCI_SERR_L       61B7< 61B7>
PCI_SLOTA_GNT_L  11D3< 59C3< 59C6>
PCI_SLOTA_INT_L  11C3< 22D5< 59C2<
PCI_SLOTA_REQ_L  11D3< 59C5< 59C6>
PCI_SLOTD_GNT_L  11C3< 59C3< 59C6>
PCI_SLOTD_INT_L  11C3< 22D5< 59C2<
PCI_SLOTD_REQ_L  11C3< 59C5< 59C6>
PCI_SLOTE_GNT_L  11C3< 22B7< 22C5<
PCI_SLOTE_INT_L  11B3< 22B7< 22C5<
PCI_SLOTE_REQ_L  11C3< 22A7< 22C5<
PCI_STOP_L       6B6< 59C5< 59D6> 60B5<> 61B7<>
            62B5<>
PCI_TRDY_L       6B6< 59C5< 59D6> 60B3<> 61A7<>
            62B5<>
PCI_USB2_GNT_L   11C2
PCI_USB2_IDSEL   62B5<
PCI_USB2_INT_L   11B2
PCI_USB2_REQ_L   11C2
PMU_BATT0_CHARGE  13A8<> 25C2<>
PMU_BATT1_CHARGE  25A4>
PMU_BATT1_DET_L  25A4>
PMU_BOOT_BUSY    24C1<> 25C2<>
PMU_BOOT_CNVSS   24C2<> 25B5<
PMU_BOOT_RP_L    24C1<> 25C2>
PMU_BOOT_RXD     24C1<> 25C2<>
PMU_BOOT_SCLK    24C2<> 25C2<>
PMU_BOOT_TXD     24C1<> 25C2<>
PMU_CHARGE_V     11B4< 13B8<>
PMU_CLK10M_XIN   25B5< 25D6>
PMU_CLK10M_XOUT  25A6< 25D6>
PMU_CLK10M_XOUT_R  25B5<> 25D6>
PMU_CLK32K_XIN   25B3< 25D6>
PMU_CLK32K_XOUT  25B1< 25D6>
PMU_CLK32K_XOUT_R  25B3<> 25D6>
PMU_CPU_CLK_EN   11B4< 25C5<>
PMU_CPU_HRESET_L  11B4< 25B5<>
PMU_CUSTOMER_RESET  24C7<>
PMU_INT_L        22D5< 25B2<>
PMU_POWER_UP_L   25B5<> 25B7< 26D8<
PMU_RESET_L      24B2< 24C2<> 24D6<> 25B5<
PMU_SB_NMI_L     22D5< 25B2<>
PMU_SYS_CLK_EN   11B4< 25C5<>
PP1V2_VESTA      10D5
PP1V2_VESTA_AVDDL  18B6<
PP1V2_VESTA_FAVDDL  69C2<
PP1V2_VESTA_PLLVDD1  66D4<
PP1V2_VESTA_PLLVDD2  69D4<
PP1V5R3V3_GPU_VDDR4  47C3< 53C8< 53D8<
PP1V5_GPU        10A7<
PP1V5_GPU_AGP    47C3<
PP1V5_GPU_PSNECK  52C3<>
PP1V5_GPU_VDD15  46B2<
PP1V5_GPU_VDD15_F  46B4<>
PP1V5_PWRON      10A5<>
PP1V5_PWRON_I2PLL  10D2
PP1V5_PWRON_I2_PLL1AVDD  19C4<
PP1V5_PWRON_I2_PLL2AVDD  19C4<
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PP1V5_PWRON_I2_PLL5AVDD  19B4<
PP1V5_PWRON_I2_PLL6AVDD  19B4<
PP1V5_PWRON_I2_PLL7AVDD  19A4<
PP1V5_PWRON_I2_PLL9AVDD  19A4<
PP1V5_PWRON_I2_PLLUSBAVDD  72C5<
PP1V5_PWRON_REG  10A6<
PP1V5_RUN        10A2
PP1V8R2V5_GPU_FB_VIO  47C6<
PP1V8_GPU        10A7<
PP1V8_GPU_A2VDDQ  53A2<
PP1V8_GPU_AVDD   53C2<
PP1V8_GPU_LVDS_PLL  47B2<
PP1V8_GPU_MEMPLL  51C3<
PP1V8_GPU_PANEL_IO  47B1< 53C4<
PP1V8_GPU_PLL    51C3<
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PP1V8_GPU_VDDDI  53B2<
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PP1V8_PWRON_REG  10A6<
PP1V8_RUN        10A2
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PP2V5R2V8_GPU_LVDS_IO  47B2<
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PP2V5_PWRON_REG  10A6<
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PP2V5_VESTA_BIASVDD2  69D4<
PP2V5_VESTA_FAVDDM  69D2<
PP2V5_VESTA_XTALVDD1  66D4<
PP2V5_VESTA_XTALVDD2  69C4<
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PP3V3R5V_RUN_HDD_LOGIC  7B7> 64B7<>
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PP3V3_ALL_HALL_EFFECT_R  7C5> 30D5<>
PP3V3_ALL_PMU_AVCC  10B7<> 25D3<
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PP3V3_GPU_PSNECK  52D2<>
PP3V3_GPU_SS     52B6<
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PP3V3_PWRON_DS1775_R  7D5> 30D6<>
PP3V3_PWRON_NEC_AVDD  73D4<
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PP3V3_RUN_PCI1510  61C8< 61D5<
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PP3V3_SI_M_PVCC  54C4<
PP3V3_SI_M_VCC   54C5<
PP3V3_SI_S_AVCC  55C5<
PP3V3_SI_S_PVCC  55D5<
PP3V3_SI_S_VCC   55C5<
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PP3V3_VESTA_FAVDDH  69D2<
PP4V6_ALL_RAW    14B3<>
PP4V85_ALL       10C7
PP4V85_ALL_ESR   14A4<
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*** Part Cross-Reference for the entire design ***

C1200 CAP 12
C1210 CAP 12
C1220 CAP 12
C1250 CAP 12
C1252 CAP 12
C1301 CAP 13
C1302 CAP 13
C1303 CAP 13
C1305 CAP 13
C1306 CAP 13
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CA000 CAP_P 74
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D1300 DIODE_SCHOT 13
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D1452 DIODE_SCHOT 14
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D1601 DIODE_SCHOT 16
D1651 DIODE_SCHOT 16
D1965 DIODE_SCHOT 18
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D1975 DIODE_SCHOT_3P2 18
D2710 DIODE 25
D3354 ZENER_MMBZ15VDLT1 30
D3900 DIODE_3P_C 36
D3901 DIODE_SCHOT 36
D4610 DIODE_SCHOT 37
D5800 DIODE_SCHOT 45
D5823 DIODE_SCHOT 45
D7010 DIODE_SCHOT 57
D9090 ZENER 70
DP1390 DPAK3P 13
DP1620 DPAK3P 16
DP1960 DPAK3P 18
DP2680 DPAK3P 24
DP6590 DPAK3P 52
DP9010 DIODE_DUAL_6P 70
DP9011 DIODE_DUAL_6P 70
DP9020 DIODE_DUAL_6P 70
DP9021 DIODE_DUAL_6P 70
F1390 FUSE 13
F1395 FUSE 13
F1965 FUSE 18
F7010 FUSE 57
F9020 FUSE 70
FL7040 FILTER_LC 57
FL7041 FILTER_LC 57
FL7042 FILTER_LC 57
FL9010 FILTER_4P 70
FL9011 FILTER_4P 70
FL9020 FILTER_4P 70
FL9021 FILTER_4P 70
G6500 OSC 52
J1250 CON_MBRT_S_SM 12
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J3320 CON_M16ST_D_SMA 30
J3350 CON_M16ST_D_SMA 30
J3400 CON_M4RT_S_SM 31
J3410 CON_M16ST_D_SMA 31
J3420 CON_M3RT_S2MT_SM 31
J3430 CON_4RT_WRIB 31
J3450 CON_M4RT_S2MT_SM 31
J3460 CON_M4RT_S2MT_SM 31
J3999 CON_12 36
J5000 CON_F400RT_DDR2DIMM_SM1 40 41
J6900 CON_F30RT_S2MT_SM 56
J6950 CON_4RT_WRIB 56
J7000 CON_F30RT_T6MT_TH1 57
J7060 CON_F5RT_MINIDIN_TH 57
J7300 CON_F80ST_D4MT_SM 60
J7450 CON_M80ST_D4MT_SM 61
J8200 CON_MS05M_SMM 64
J8250 CON_MS05M_SMM 64
J8600 CON_RJ45_10RT_S4MT_TH1 67
J9010 CON_F5RT_13940_S6MT_SMA 70
J9020 CON_F6RT_S4MT_TH1 70
JA000 CON_MS05M_SMM 74
L1250 IND 12
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L9335 IND 73
P03100 PHOTODIODE_2P 28
Q1208 TRA_2N7002DW 12
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Q1215 TRA_2N7002DW 12
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Q1301 TRA_IRF7811W 13
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