1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

Mullet

M1 MLB
09/26/2005

REV	ZONE	ECN	DESCRIPTION OF CHANGE	CK APPD / DATE	ENG APPD / DATE
?		?	?	?	?

Page (.csa)	Contents	Sync	Date
1 1	Table of Contents	N/A	N/A
2 2	System Block Diagram	N/A	N/A
3 3	Power Block Diagram	N/A	N/A
4 4	BOM Configuration	N/A	N/A
5 5	Functional / ICT Test	N/A	N/A
6 6	Signal Aliases	N/A	N/A
7 7	CPU 1 OF 2-FSB	M42	09/08/2005
8 8	CPU 2 OF 2-PWR/GND	M42	09/08/2005
9 9	CPU Decoupling & VID	(MASTER)	(MASTER)
10 10	CPU MISC1-TEMP SENSOR	M42	09/08/2005
11 11	CPU ITP700FLEX DEBUG	M42	09/08/2005
12 12	NB CPU Interface	(MASTER)	(MASTER)
13 13	NB PEG / Video Interfaces	(MASTER)	(MASTER)
14 14	NB Misc Interfaces	(MASTER)	(MASTER)
15 15	NB DDR2 Interfaces	(MASTER)	(MASTER)
16 16	NB Power 1	(MASTER)	(MASTER)
17 17	NB Power 2	(MASTER)	(MASTER)
18 18	NB Grounds	(MASTER)	(MASTER)
19 19	NB (GM) Decoupling	(MASTER)	(MASTER)
20 20	NB Config Straps	(MASTER)	(MASTER)
21 21		M38	09/08/2005
22 22		M38	09/08/2005
23 23		M38	09/08/2005
24 24		M38	09/08/2005
25 25		M42	09/08/2005
26 26	SB Misc	(MASTER)	(MASTER)
27 27	M1 SMBus Connections	(MASTER)	(MASTER)
28 28	DDR2 SO-DIMM Connector A	(MASTER)	(MASTER)
29 29	DDR2 SO-DIMM Connector B	(MASTER)	(MASTER)
30 30	Memory Active Termination	(MASTER)	(MASTER)
31 31	Memory Vtt Supply	(MASTER)	(MASTER)
32 32	DDR2 VRef	(MASTER)	(MASTER)
33 33	CLOCKS	M42	09/08/2005
34 34	Clock Termination	(MASTER)	(MASTER)
35 37	Mobile Clocking	(MASTER)	(MASTER)
36 38	PATA Connector	(MASTER)	(MASTER)
37 41	ETHERNET CONTROLLER	M42	09/08/2005
38 42	Ethernet Connector	(MASTER)	(MASTER)
39 44	FIREWIRE CONTROLLER	M42	08/29/2005
40 45	FireWire Port Power	(MASTER)	(MASTER)
41 46	FireWire Ports	(MASTER)	(MASTER)
42 49	Internal USB Connections	(MASTER)	(MASTER)
43 52	External USB Connector	(MASTER)	(MASTER)
44 55	Left I/O Board Connector	(MASTER)	(MASTER)
45 57	PCI-E Connections	(MASTER)	(MASTER)
46 58		M38	09/08/2005
47 59	SMC Support	(MASTER)	(MASTER)
48 60	LPC+ Debug Connector	M42	07/20/2005
49 61	Thermal Sensors	(MASTER)	(MASTER)
50 62	Current & Voltage Sensing	(MASTER)	(MASTER)
51 63	SPI BOOTROM	(M42)	07/26/2005
52 64	ALS Support	(MASTER)	(MASTER)
53 65	Fan Connectors	(MASTER)	(MASTER)
54 66	SMS	(M42)	07/26/2005
55 67		M38	09/08/2005
56 75	IMVP6 CPU VCore Regulator	(MASTER)	(MASTER)
57 76	5V / 1.5V Power Supply	(MASTER)	(MASTER)
58 77	2.5V & 1.2V Regulators	(MASTER)	(MASTER)
59 78	1.8V Supply	(MASTER)	(MASTER)
60 79	3.3V / 1.05V Power Supplies	(MASTER)	(MASTER)
61 80	3.3V G3Hot Supply	(MASTER)	(MASTER)
62 81	Power Aliases	(MASTER)	(MASTER)
63 82	PBus-In & Battery Connectors	(MASTER)	(MASTER)
64 83	S3/S0 FETs & Power Control	(MASTER)	(MASTER)
65 84	ATI M56 PCI-E	(MASTER)	(MASTER)
66 85	GPU (M56) Core Supplies	(MASTER)	(MASTER)
67 86	ATI M56 Core Power	(MASTER)	(MASTER)
68 87	ATI M56 Frame Buffer I/F	(MASTER)	(MASTER)
69 88	GPU Straps	(MASTER)	(MASTER)
70 89	GDDR3 Frame Buffer A	(MASTER)	(MASTER)
71 90	GDDR3 Frame Buffer B	(MASTER)	(MASTER)
72 91	ATI M56 GPIO/DVO/Misc	(MASTER)	(MASTER)
73 93	ATI M56 Video Interfaces	(MASTER)	(MASTER)
74 94	Internal Display Connectors	(MASTER)	(MASTER)
75 97	External Display Connector	(MASTER)	(MASTER)
76 99	Physical Security	(MASTER)	(MASTER)
77 100	Revision History	N/A	N/A
78 101	Napa Platform Constraints	(MASTER)	(MASTER)
79 102	More System Constraints	(MASTER)	(MASTER)
80 103	M1 Spacing & Physical Constraints	(MASTER)	(MASTER)
81 104	M1 Net Properties	(MASTER)	(MASTER)

Schematic / PCB #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-6941	1	SCHEM,MULLET,M1	SCH		
820-1881	1	PCBF,MULLET,M1	PCB		
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TSQ]	CRITICAL	VRAM_128
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEE:TYY]	CRITICAL	VRAM_256

DRAWING
TITLE=MULLET
ABBREV=DRAWING
LAST_MODIFIED=Mon Sep 26 13:38:08 2005

DIMENSIONS ARE IN MILLIMETERS
XX ±
X.XX ±
X.XXX ±
ANGLES ±
DO NOT SCALE DRAWING

THIRD ANGLE PROJECTION

METRIC

DRAFTER		DESIGN CK	
ENG APPD		MFG APPD	
QA APPD		DESIGNER	
RELEASE		SCALE	NONE

MATERIAL/FINISH NOTED AS APPLICABLE

SIZE D

Apple Computer Inc.

TITLE
SCHEM,MULLET,M1

DRAWING NUMBER 051-6941 REV. 07001

SHT 1 OF 81

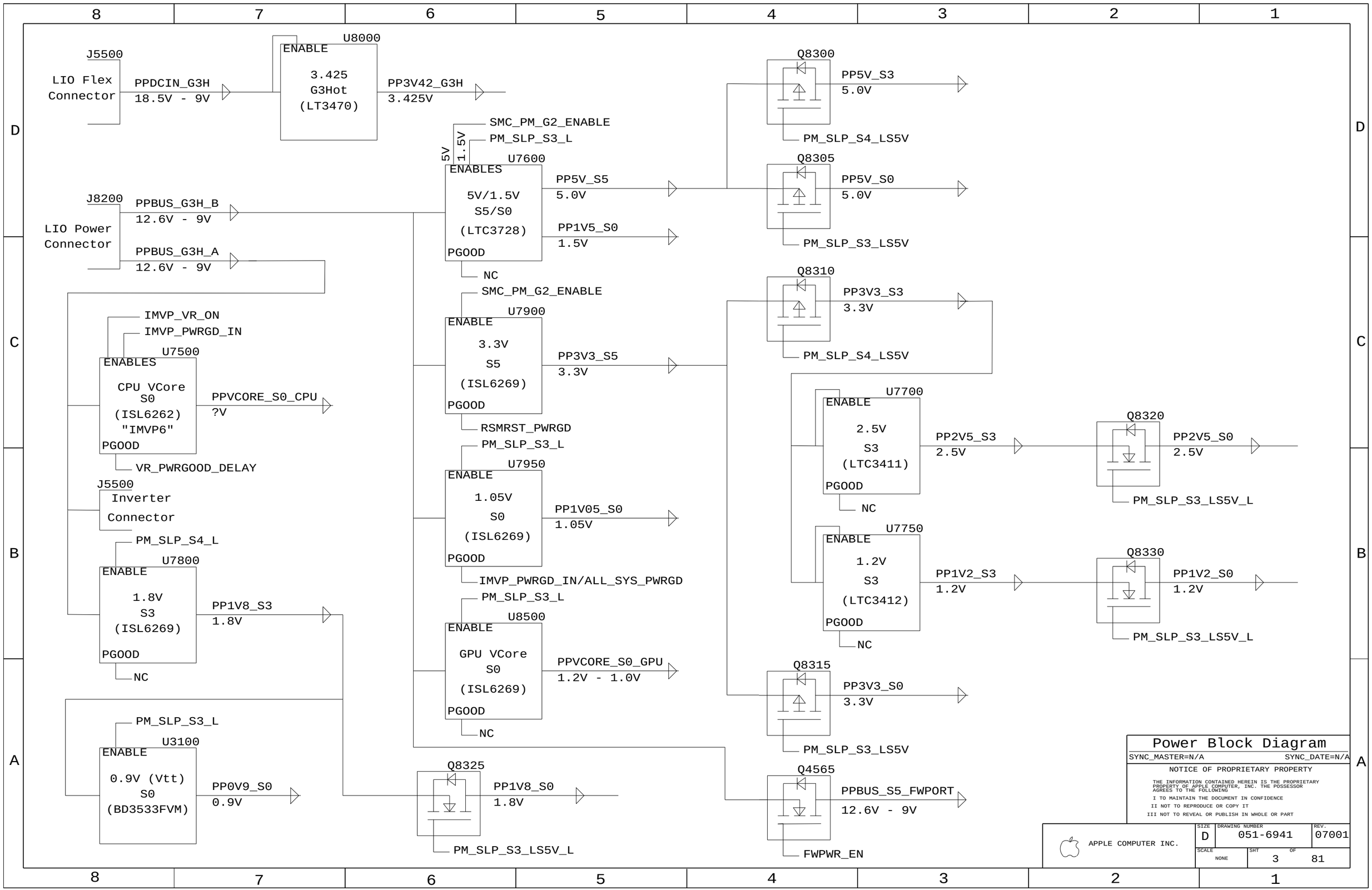
System Block Diagram

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	2	81


J5500
LIO Flex Connector
PPDCIN_G3H
18.5V - 9V
U8000
ENABLE
3.425 G3Hot (LT3470)
PP3V42_G3H
3.425V
J8200
LIO Power Connector
PPBUS_G3H_B
12.6V - 9V
PPBUS_G3H_A
12.6V - 9V
U7600
ENABLES
5V/1.5V S5/S0 (LTC3728)
PGOOD
SMC_PM_G2_ENABLE
PM_SLP_S3_L
5V
1.5V
PP5V_S5
5.0V
PP1V5_S0
1.5V
NC
Q8300
PP5V_S3
5.0V
PM_SLP_S4_LS5V
Q8305
PP5V_S0
5.0V
PM_SLP_S3_LS5V
IMVP_VR_ON
IMVP_PWRGD_IN
U7500
ENABLES
CPU VCore S0 (ISL6262) "IMVP6"
PGOOD
PPVCORE_S0_CPU
?V
VR_PWRGOOD_DELAY
J5500
Inverter Connector
PM_SLP_S4_L
U7800
ENABLE
1.8V S3 (ISL6269)
PGOOD
PP1V8_S3
1.8V
NC
U7900
ENABLE
3.3V S5 (ISL6269)
PGOOD
SMC_PM_G2_ENABLE
PP3V3_S5
3.3V
RSMRST_PWRGD
PM_SLP_S3_L
U7950
ENABLE
1.05V S0 (ISL6269)
PGOOD
PP1V05_S0
1.05V
IMVP_PWRGD_IN/ALL_SYS_PWRGD
U8500
ENABLE
GPU VCore S0 (ISL6269)
PGOOD
PPVCORE_S0_GPU
1.2V - 1.0V
NC
Q8310
PP3V3_S3
3.3V
PM_SLP_S4_LS5V
U7700
ENABLE
2.5V S3 (LTC3411)
PGOOD
PP2V5_S3
2.5V
NC
Q8320
PP2V5_S0
2.5V
PM_SLP_S3_LS5V_L
U7750
ENABLE
1.2V S3 (LTC3412)
PGOOD
PP1V2_S3
1.2V
NC
Q8330
PP1V2_S0
1.2V
PM_SLP_S3_LS5V_L
Q8315
PP3V3_S0
3.3V
PM_SLP_S3_LS5V
U3100
ENABLE
0.9V (Vtt) S0 (BD3533FVM)
PM_SLP_S3_L
PP0V9_S0
0.9V
Q8325
PP1V8_S0
1.8V
PM_SLP_S3_LS5V_L
Q4565
PPBUS_S5_FWPORT
12.6V - 9V
FWPWR_EN
Power Block Diagram
SYNC_MASTER=N/A
SYNC_DATE=N/A
NOTICE OF PROPRIETARY PROPERTY
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APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 07001
SCALE NONE
SHT 3 OF 81

BOM NUMBER	BOM NAME	BOM OPTIONS
630-7207	PCBA,MULLET_128,M1	075-0137,075-0139,075-0140
630-7254	PCBA,MULLET_256,M1	075-0138,075-0139,075-0140
075-0137	128,MULLET,M1	VRAM_128
075-0138	256,MULLET,M1	VRAM_256,GPU_MEM_256M
075-0139	PROJ_PTS,MULLET,M1	COMMON,M1_COMMON1,M1_COMMON2,M1_DEBUG
075-0140	LEMENU_PTS,MULLET,M1	LEMENU_STAGE2,LEMENU_STAGE3

BOM GROUP	BOM OPTIONS
M1_COMMON1	GPU_BB_CTL,GPUTHM_A_GPU,HSTHMSNS_HAS,INVERTER_BUF,KBDLED_HAS,LEMENU_STAGE1
M1_COMMON2	MEMVREF_S3,MEMVTT_EN_PU,PLTRST_GATE_STUFF,USB_C_OC_PU,USB_D_OC_PU,USB_E_OC_PU
M1_DEBUG	DEVELOPMENT,ITP,LPCPLUS

Phantom BOM #’s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
075-0137	1	128,MULLET,M1	BOM1		075-0137
075-0138	1	256,MULLET,M1	BOM2		075-0138
075-0139	1	PROJ PTS,MULLET,M1	BOM3		075-0139
075-0140	1	LeMENU PTS,MULLET,M1	BOM4		075-0140

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
333S0354	4	IC,SGRAM,GDDR3,8MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_128
333S0350	4	IC,SGRAM,GDDR3,16MX32,700MHZ,136 FBGA	U8900,U8950,U9000,U9050	CRITICAL	VRAM_256

"LeMenu Stage #1" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION	
338S0266	1	IC,ATI,M56P,GRPHSCTRL,880BGA,LF	U8400	CRITICAL	LEMENU_STAGE1	
338S0268	1	IC,FW32306,1394A LINK,BGA,129P	U4400	CRITICAL	LEMENU_STAGE1	
338S0270	1	IC,88E8053,GIGABIT ENET XCVR,64P QFN, NO	U4101	CRITICAL	LEMENU_STAGE1	
338S0274	1	IC,SMC,HS8/2116	U5800	CRITICAL	LEMENU_STAGE1	
341S1797	1	IC,EEPROM,SERIAL IIC,8KBIT,SO8	U4102	CRITICAL	LEMENU_STAGE1	
341S1812	1	IC,EFI,BOOTROM DEVELOPMENT,M1	U6301	CRITICAL	LEMENU_STAGE1	341S1813 is production BootROM
353S1235	1	IC,CPU VOLTAGE REGULATOR,IMVP,TWO PHASE	U7530	CRITICAL	LEMENU_STAGE1	
359S0101	1	IC,CY28445-5,CLOCK GEN,68PIN QFN	U3301	CRITICAL	LEMENU_STAGE1	

"LeMenu Stage #2" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
341S1789	1	IC, TPM, 28-PIN TSSOP	U6700	CRITICAL	LEMENU_STAGE2

"LeMenu Stage #3" Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3208	1	IC,YONAH CPU,479 BGA	U0700	CRITICAL	LEMENU_STAGE3
338S0269	1	IC,945GM,SOUTHBRIDGE	U1200	CRITICAL	LEMENU_STAGE3
343S0385	1	IC,SB,652BGA	U2100	CRITICAL	LEMENU_STAGE3

BOM Configuration

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 07001

SCALE NONE | SHT 4 OF 81

Functional Test Points

Power Supply NO_TESTs

NO_TEST

TRUE	IMVP6_RBIAS	56
TRUE	IMVP6_COMP	56
TRUE	P5VS5_RUNSS	57 64
TRUE	P1V5S0_RUNSS	57 64
TRUE	P2V5S3_MODE	58
TRUE	P2V5S3_SHDNRT	58 64
TRUE	P1V2S3_RT	58
TRUE	P1V2S3_RUNSS	58 64
TRUE	P1V8S3_COMP	59
TRUE	P1V8S3_FSET	59
TRUE	P3V3S5_COMP	60
TRUE	P3V3S5_FSET	60
TRUE	P1V05S0_COMP	60
TRUE	P1V05S0_FSET	60
TRUE	P3V42G3H_FB	61
TRUE	GPUVCORE_COMP	66
TRUE	GPUVCORE_FSET	66
TRUE	GPUBBP_ADJ	66

CPU FSB NO_TESTs

NO_TEST

TRUE	FSB_A_L<31..3>	7 12 81
TRUE	FSB_ADS_L	7 12 81
TRUE	FSB_ADSTB_L<1..0>	7 12 81
TRUE	FSB_BNR_L	7 12 81
TRUE	FSB_BREQ0_L	7 12 81
TRUE	FSB_D_L<63..0>	7 12 81
TRUE	FSB_DBSY_L	7 12 81
TRUE	FSB_DINV_L<3..0>	7 12 81
TRUE	FSB_DRDY_L	7 12 81
TRUE	FSB_DSTBN_L<3..0>	7 12 81
TRUE	FSB_DSTBP_L<3..0>	7 12 81
TRUE	FSB_HIT_L	7 12 81
TRUE	FSB_HITM_L	7 12 81
TRUE	FSB_LOCK_L	7 12 81
TRUE	FSB_REQ_L<4..0>	7 12 81

FUNC_TEST property removed since these test points are not on the proper side for Functional Test points.

Fan Connectors

FUNC_TEST

	=PP5V_S0_FAN_LT	53 62
	FAN_LT_PWM	53
	FAN_LT_TACH	53
	FAN_RT_PWM	53
	FAN_RT_TACH	53

LPC+ Debug Connector

FUNC_TEST

TRUE	=PP3V3_S5_LPCPLUS	48 62
TRUE	=PP5V_S0_LPCPLUS	48 62
TRUE	LPC_AD<0>	21 46 48 55
TRUE	LPC_AD<1>	21 46 48 55
TRUE	LPC_FRAME_L	21 46 48 55
TRUE	PM_CLKRUN_L	23 39 46 48 55
TRUE	BOOT_LPC_SPI_L	22 46 48 76
TRUE	SMC_TMS	46 47 48
TRUE	DEBUG_RST_L	26 48
TRUE	SMC_TRST_L	46 48
TRUE	SMC_TDO	46 47 48
TRUE	SMC_MD1	46 48
TRUE	SMC_TX_L	46 47 48
TRUE	FWH_INIT_L	21 47 48
TRUE	PCI_CLK_PORT80_LPC	34 48
TRUE	LPC_AD<2>	21 46 48 55
TRUE	LPC_AD<3>	21 46 48 55
TRUE	INT_SERIRQ	23 46 48 55
TRUE	PM_SUS_STAT_L	23 46 48 55
TRUE	SMC_TDI	46 47 48
TRUE	SMC_TCK	46 47 48
TRUE	SMC_RST_L	46 47 48
TRUE	SMC_NMI	46 48
TRUE	SMC_RX_L	46 47 48
TRUE	SV_SET_UP	23 48

Other Func Test Points

FUNC_TEST

TRUE	=PP1V05_S0_REG	50 60 62

Battery Digital Connector

FUNC_TEST

TRUE	SMC_BS_ALRT_L	46 47 63
TRUE	=SMBUS_BATT_SCL	27 63
TRUE	=SMBUS_BATT_SDA	27 63
TRUE	GND_BATT	63

Left I/O Data Connector

FUNC_TEST

TRUE	=PP1V5_S0_LIO	44 62
TRUE	=PPDCIN_G3H_LIO	44 62
TRUE	=PP5V_S5_LIO	44 62
TRUE	=PP3V42_G3H_LIO	44 62
TRUE	PP5V_S0_AUDIO_PWR	44
TRUE	PP5V_S0_AUDIO	44
TRUE	GND_AUDIO_PWR	44
TRUE	GND_AUDIO	44
TRUE	ACZ_SDATAIN<0>	21 44 81
TRUE	ACZ_SDATAOUT	21 44 81
TRUE	ACZ_BITCLK	21 44 81
TRUE	ACZ_RST_L	21 44 81
TRUE	EXCARD_OC_L	6 44 47
TRUE	LTUSB_OC_L	6 44
TRUE	LIO_BATT_ISENSE	44 50
TRUE	SMC_SYS_ISET	44 46
TRUE	SMC_BATT_ISET	44 46
TRUE	SMC_BATT_CHG_EN	44 46 47
TRUE	SMC_BC_ACOK	44 46 47
TRUE	SMC_ADAPTER_EN	40 44 46 47
TRUE	LIO_P3V3S0_EN_L	44 64
TRUE	LIO_DCIN_ISENSE	44 50
TRUE	LIO_P3V3S3_EN	44 64
TRUE	SMC_BATT_TRICKLE_EN_L	44 46 47
TRUE	SYS_ONEWIRE	44 46 47
TRUE	MINI_CLKREQ_L	34 44
TRUE	SMC_EXCARD_CP	44 46 47
TRUE	EXCARD_CLKREQ_L	34 44
TRUE	SMC_EXCARD_PWR_EN	44 46
TRUE	LIO_PLT_RESET_L	26 44
TRUE	ACZ_SYNC	21 44 81
TRUE	=USB2_LT_N	6 44
TRUE	=USB2_LT_P	6 44
TRUE	=USB2_EXCARD_N	6 44
TRUE	=USB2_EXCARD_P	6 44
TRUE	=PCIE_EXCARD_R2D_N	44 45
TRUE	=PCIE_EXCARD_R2D_P	44 45
TRUE	=PCIE_EXCARD_D2R_N	44 45
TRUE	=PCIE_EXCARD_D2R_P	44 45
TRUE	PCIE_CLK100M_EXCARD_P	34 44
TRUE	PCIE_CLK100M_EXCARD_N	34 44
TRUE	=USB2_MINI_N	6 44
TRUE	=USB2_MINI_P	6 44
TRUE	=PCIE_MINI_R2D_N	44 45
TRUE	=PCIE_MINI_R2D_P	44 45
TRUE	=PCIE_MINI_D2R_N	44 45
TRUE	=PCIE_MINI_D2R_P	44 45
TRUE	PCIE_CLK100M_MINI_P	34 44
TRUE	PCIE_CLK100M_MINI_N	34 44
TRUE	=SMBUS_LIO_SMC_SCL	27 44
TRUE	=SMBUS_LIO_SMC_SDA	27 44
TRUE	=SMBUS_LIO_SB_SCL	27 44
TRUE	=SMBUS_LIO_SB_SDA	27 44
TRUE	PCIE_WAKE_L	23 37 44

Left I/O Power Connector

FUNC_TEST

TRUE	=PPBUS_G3H_LIO_CONN	62 63
TRUE	GND	

Request for at least 10 GND test points

Functional / ICT Test

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	5	81

NC_CPU_A32_L — TP_CPU_A32_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A33_L — TP_CPU_A33_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A34_L — TP_CPU_A34_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A35_L — TP_CPU_A35_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A36_L — TP_CPU_A36_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A37_L — TP_CPU_A37_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A38_L — TP_CPU_A38_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_A39_L — TP_CPU_A39_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM0_L — TP_CPU_APM0_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_APM1_L — TP_CPU_APM1_L (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_EXTBREF — TP_CPU_EXTBREF (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_HFPLL — TP_CPU_HFPLL (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE0 — TP_CPU_SPARE0 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE1 — TP_CPU_SPARE1 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE2 — TP_CPU_SPARE2 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_CPU_SPARE4 — TP_CPU_SPARE4 (7)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_A_A<15..14> — MEM_A_A<15..14> (28)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_MEM_B_A<15..14> — MEM_B_A<15..14> (29)
MAKE_BASE=TRUE, NO_TEST=TRUE

TP_NB_CFG<4..3> — NB_CFG<4..3> (14)
MAKE_BASE=TRUE

TP_NB_CFG<6> — NB_CFG<6> (14)
MAKE_BASE=TRUE

TP_NB_CFG<8> — NB_CFG<8> (14)
MAKE_BASE=TRUE

TP_NB_CFG<11..10> — NB_CFG<11..10> (14)
MAKE_BASE=TRUE

TP_NB_CFG<15..14> — NB_CFG<15..14> (14)
MAKE_BASE=TRUE

TP_NB_CFG<17> — NB_CFG<17> (14)
MAKE_BASE=TRUE

NOTE: NB_CFG<13..12> require test access

TP_NB_CFG<13..12> — NB_CFG<13..12> (14)
MAKE_BASE=TRUE

TP_SB_SUS_CLK — SUS_CLK_SB (23)
MAKE_BASE=TRUE

NC_ENET_CTRL12 — ENET_CTRL12 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_ENET_CTRL25 — ENET_CTRL25 (37)
MAKE_BASE=TRUE, NO_TEST=TRUE

NC_FWPWR_PWRON — =FWPWR_PWRON (40)
MAKE_BASE=TRUE, NO_TEST=TRUE

USB Port "A" (Debug Port) = Right USB 2.0 Port

=USB2_RT_P — USB2_RT_P (MAKE_BASE=TRUE) — USB_A_P (22) (43)
=USB2_RT_N — USB2_RT_N (MAKE_BASE=TRUE) — USB_A_N (22) (43)
=RTUSB_OC_L — RTUSB_OC_L (MAKE_BASE=TRUE) — USB_A_OC_L (22) (43)

USB Port "B" = PCI-E Mini Card

=USB2_MINI_P — USB2_MINI_P (MAKE_BASE=TRUE) — USB_B_P (22) (44 5)
=USB2_MINI_N — USB2_MINI_N (MAKE_BASE=TRUE) — USB_B_N (22) (44 5)
UNUSED_USB_B_OC_L (MAKE_BASE=TRUE) — USB_B_OC_L (22)

USB Port "C" = Left USB 2.0 Port

=USB2_LT_P — USB2_LT_P (MAKE_BASE=TRUE) — USB_C_P (22) (44 5)
=USB2_LT_N — USB2_LT_N (MAKE_BASE=TRUE) — USB_C_N (22) (44 5)
LTUSB_OC_L (MAKE_BASE=TRUE) — USB_C_OC_L (22) (44 5)

USB Port "D" = Camera

=USB2_CAMERA_P — USB2_CAMERA_P (MAKE_BASE=TRUE) — USB_D_P (22) (42)
=USB2_CAMERA_N — USB2_CAMERA_N (MAKE_BASE=TRUE) — USB_D_N (22) (42)
UNUSED_USB_D_OC_L (MAKE_BASE=TRUE) — USB_D_OC_L (22)

USB Port "E" = ExpressCard

=USB2_EXCARD_P — USB2_EXCARD_P (MAKE_BASE=TRUE) — USB_E_P (22) (44 5)
=USB2_EXCARD_N — USB2_EXCARD_N (MAKE_BASE=TRUE) — USB_E_N (22) (44 5)
EXCARD_OC_L (MAKE_BASE=TRUE) — USB_E_OC_L (22) (47 44 5)

USB Port "F" = IR Receiver

=USB_IR_P — TP_USB_IRP (MAKE_BASE=TRUE) — USB_F_P (22)
=USB_IR_N — TP_USB_IRN (MAKE_BASE=TRUE) — USB_F_N (22)

USB Port "G" = Bluetooth (M13P)

=USB_BT_P — USB_BT_P (MAKE_BASE=TRUE) — USB_G_P (22) (42)
=USB_BT_N — USB_BT_N (MAKE_BASE=TRUE) — USB_G_N (22) (42)

USB Port "H" = Trackpad (Geyser)

=USB_TRACKPAD_P — USB_TRACKPAD_P (MAKE_BASE=TRUE) — USB_H_P (22) (42)
=USB_TRACKPAD_N — USB_TRACKPAD_N (MAKE_BASE=TRUE) — USB_H_N (22) (42)

Chassis connection to be made at the mounting hole northwest of the DVI connector

ZT0600
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_TOP
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI2 (75)
GND_CHASSIS_DVI_TOP — =GND_CHASSIS_DVI4 (75)

Chassis connection to be made at the mounting hole southwest of the USB connector

ZT0601
HOLE-VIA-P5RP25
1 — GND_CHASSIS_DVI_BOT
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI1 (75)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_DVI3 (75)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_ENET (38)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_FW_EMI (41)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_FW_PORT1 (41)
GND_CHASSIS_DVI_BOT — =GND_CHASSIS_RTUSB (43)

Chassis connection to be made at the mounting hole east of the LVDS connector

ZT0602
HOLE-VIA-P5RP25
1 — GND_CHASSIS_LVDS
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD1 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD2 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD3 (74)
GND_CHASSIS_LVDS — =GND_CHASSIS_LCD4 (74)

SH0600
OG-503040
SHLD-SM-LF
1, 2, 3 — GND_CHASSIS_INVERTER
MIN_LINE_WIDTH=0.5 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V, MAKE_BASE=TRUE
GND_CHASSIS_INVERTER — =GND_CHASSIS_INVERTER (74)

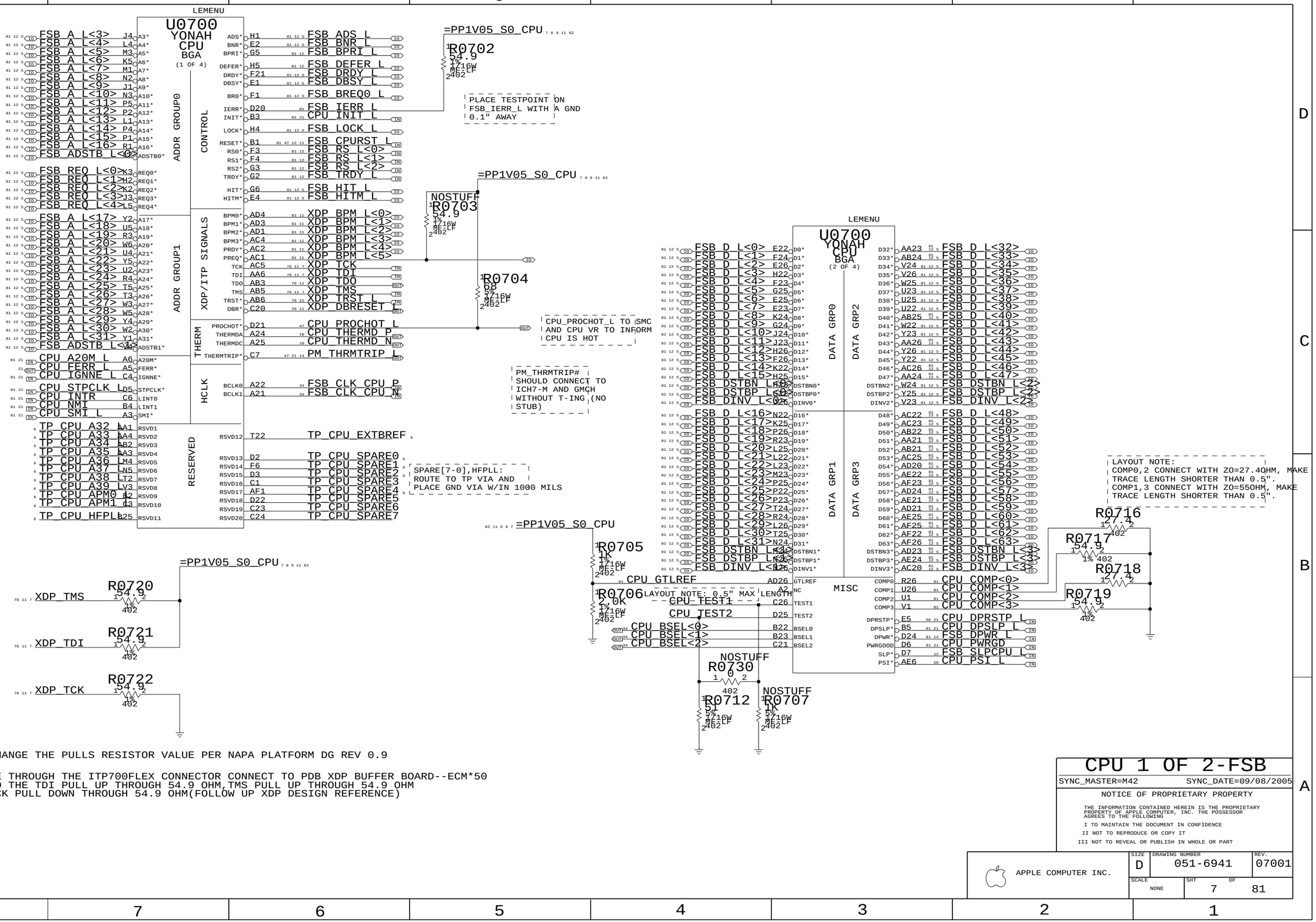
Signal Aliases

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	6	81


LEMENU
U0700
YONAH
CPU
BGA
(1 OF 4)
ADDR GROUP0
CONTROL
XDP/ITP SIGNALS
ADDR GROUP1
THERM
HCLK
RESERVED
FSB_A_L<3>
FSB_A_L<4>
FSB_A_L<5>
FSB_A_L<6>
FSB_A_L<7>
FSB_A_L<8>
FSB_A_L<9>
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FSB_A_L<11>
FSB_A_L<12>
FSB_A_L<13>
FSB_A_L<14>
FSB_A_L<15>
FSB_A_L<16>
FSB_ADSTB_L<0>
FSB_REQ_L<0>
FSB_REQ_L<1>
FSB_REQ_L<2>
FSB_REQ_L<3>
FSB_REQ_L<4>
FSB_A_L<17>
FSB_A_L<18>
FSB_A_L<19>
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FSB_A_L<25>
FSB_A_L<26>
FSB_A_L<27>
FSB_A_L<28>
FSB_A_L<29>
FSB_A_L<30>
FSB_A_L<31>
FSB_ADSTB_L<1>
CPU_A20M_L
CPU_FERR_L
CPU_IGNNE_L
CPU_STPCLK_L
CPU_INTR
CPU_NMI
CPU_SMI_L
TP_CPU_A32_L
TP_CPU_A33_L
TP_CPU_A34_L
TP_CPU_A35_L
TP_CPU_A36_L
TP_CPU_A37_L
TP_CPU_A38_L
TP_CPU_A39_L
TP_CPU_APM0_L
TP_CPU_APM1_L
TP_CPU_HFPLL
FSB_ADS_L
FSB_BNR_L
FSB_BPRI_L
FSB_DEFER_L
FSB_DRDY_L
FSB_DBSY_L
FSB_BREQ0_L
FSB_IERR_L
CPU_INIT_L
FSB_LOCK_L
FSB_CPURST_L
FSB_RS_L<0>
FSB_RS_L<1>
FSB_RS_L<2>
FSB_TRDY_L
FSB_HIT_L
FSB_HITM_L
XDP_BPM_L<0>
XDP_BPM_L<1>
XDP_BPM_L<2>
XDP_BPM_L<3>
XDP_BPM_L<4>
XDP_BPM_L<5>
XDP_TCK
XDP_TDI
XDP_TDO
XDP_TMS
XDP_TRST_L
XDP_DBRESET_L
CPU_PROCHOT_L
CPU_THERMD_P
CPU_THERMD_N
PM_THRMTRIP_L
FSB_CLK_CPU_P
FSB_CLK_CPU_N
TP_CPU_EXTBREF
TP_CPU_SPARE0
TP_CPU_SPARE1
TP_CPU_SPARE2
TP_CPU_SPARE3
TP_CPU_SPARE4
TP_CPU_SPARE5
TP_CPU_SPARE6
TP_CPU_SPARE7
=PP1V05_S0_CPU
R0702
54.9
1% 1/16W MF-LF
402
PLACE TESTPOINT ON FSB_IERR_L WITH A GND 0.1" AWAY
NOSTUFF
R0703
54.9
R0704
68
SPARE[7-0],HFPLL: ROUTE TO TP VIA AND PLACE GND VIA W/IN 1000 MILS
CPU_PROCHOT_L TO SMC AND CPU VR TO INFORM CPU IS HOT
PM_THRMTRIP# SHOULD CONNECT TO ICH7-M AND GMCH WITHOUT T-ING (NO STUB)
R0705
1K
R0706
2.0K
LAYOUT NOTE: 0.5" MAX LENGTH
CPU_GTLREF
CPU_TEST1
CPU_TEST2
CPU_BSEL<0>
CPU_BSEL<1>
CPU_BSEL<2>
R0730
0
R0712
5K
R0707
1K
R0720
R0721
R0722
XDP_TMS
XDP_TDI
XDP_TCK
LEMENU
U0700
YONAH
CPU
BGA
(2 OF 4)
DATA GRP0
DATA GRP2
DATA GRP1
DATA GRP3
MISC
FSB_D_L<0>
FSB_D_L<1>
FSB_D_L<2>
FSB_D_L<3>
FSB_D_L<4>
FSB_D_L<5>
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FSB_D_L<11>
FSB_D_L<12>
FSB_D_L<13>
FSB_D_L<14>
FSB_D_L<15>
FSB_DSTBN_L<0>
FSB_DSTBP_L<0>
FSB_DINV_L<0>
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FSB_D_L<45>
FSB_D_L<46>
FSB_D_L<47>
FSB_DSTBN_L<1>
FSB_DSTBP_L<1>
FSB_DINV_L<1>
FSB_D_L<48>
FSB_D_L<49>
FSB_D_L<50>
FSB_D_L<51>
FSB_D_L<52>
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FSB_D_L<55>
FSB_D_L<56>
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FSB_D_L<58>
FSB_D_L<59>
FSB_D_L<60>
FSB_D_L<61>
FSB_D_L<62>
FSB_D_L<63>
FSB_DSTBN_L<2>
FSB_DSTBP_L<2>
FSB_DINV_L<2>
CPU_COMP<0>
CPU_COMP<1>
CPU_COMP<2>
CPU_COMP<3>
CPU_DPRSTP_L
CPU_DPSLP_L
FSB_DPWR_L
CPU_PWRGD
FSB_SLPCPU_L
CPU_PSI_L
LAYOUT NOTE: COMP0,2 CONNECT WITH ZO=27.4OHM, MAKE TRACE LENGTH SHORTER THAN 0.5". COMP1,3 CONNECT WITH ZO=55OHM, MAKE TRACE LENGTH SHORTER THAN 0.5".
R0716
27.4
R0717
54.9
R0718
27.4
R0719
54.9
CHANGE THE PULLS RESISTOR VALUE PER NAPA PLATFORM DG REV 0.9
WE THROUGH THE ITP700FLEX CONNECTOR CONNECT TO PDB XDP BUFFER BOARD--ECM*50
SO THE TDI PULL UP THROUGH 54.9 OHM,TMS PULL UP THROUGH 54.9 OHM
TCK PULL DOWN THROUGH 54.9 OHM(FOLLOW UP XDP DESIGN REFERENCE)
CPU 1 OF 2-FSB
SYNC_MASTER=M42
SYNC_DATE=09/08/2005
NOTICE OF PROPRIETARY PROPERTY
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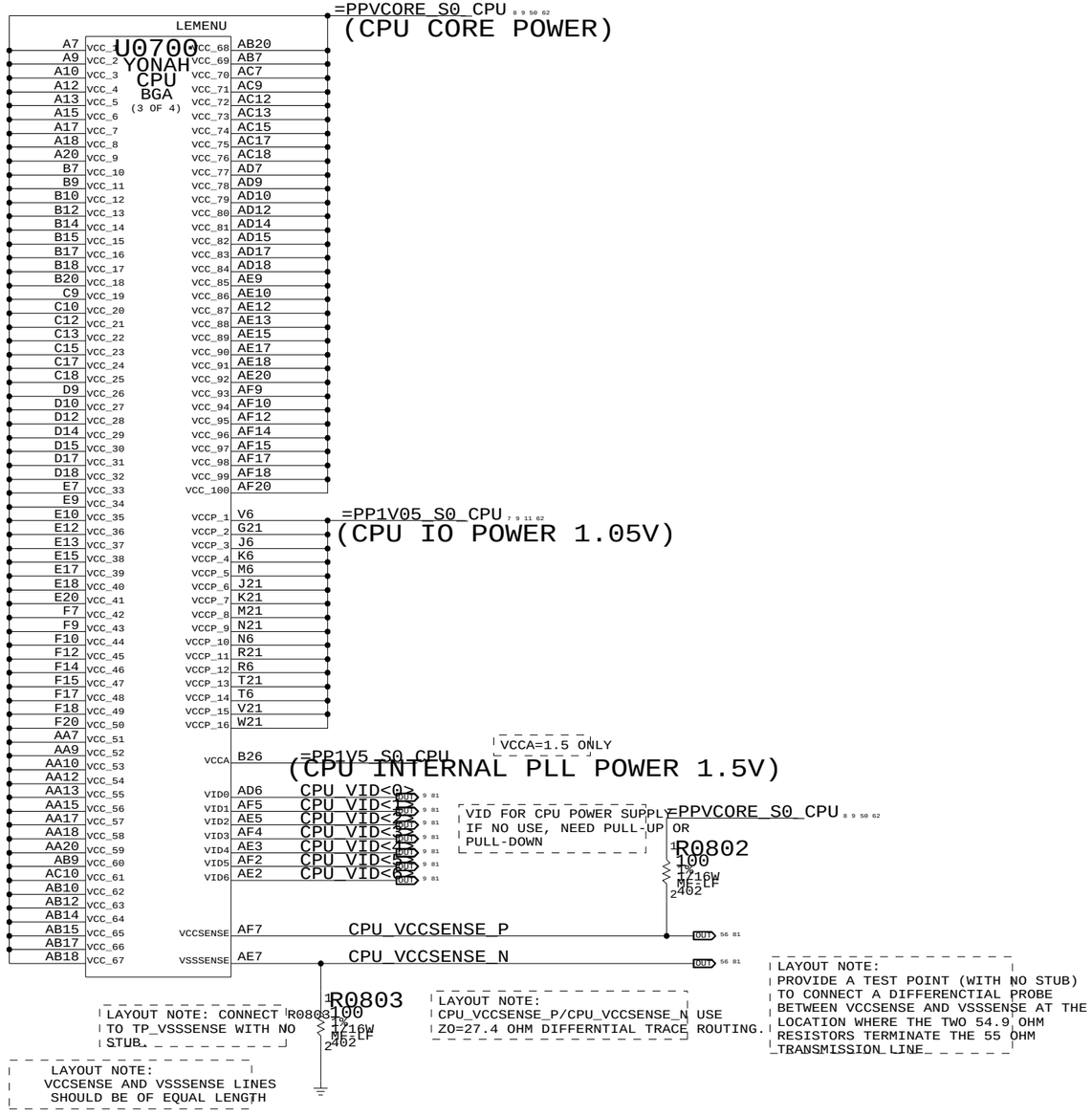
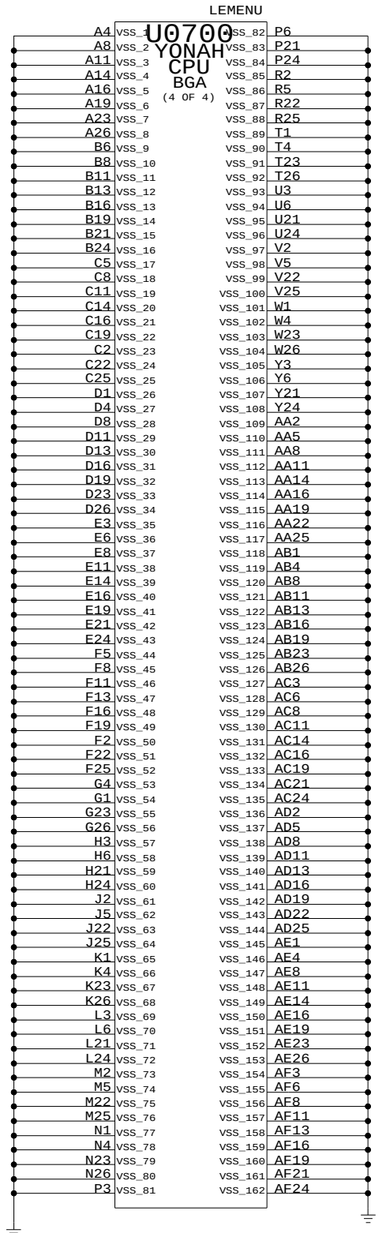
APPLE COMPUTER INC.
SIZE D
DRAWING NUMBER 051-6941
REV. 07001
SCALE NONE
SHT 7 OF 81





CPU 2 OF 2-PWR/GND

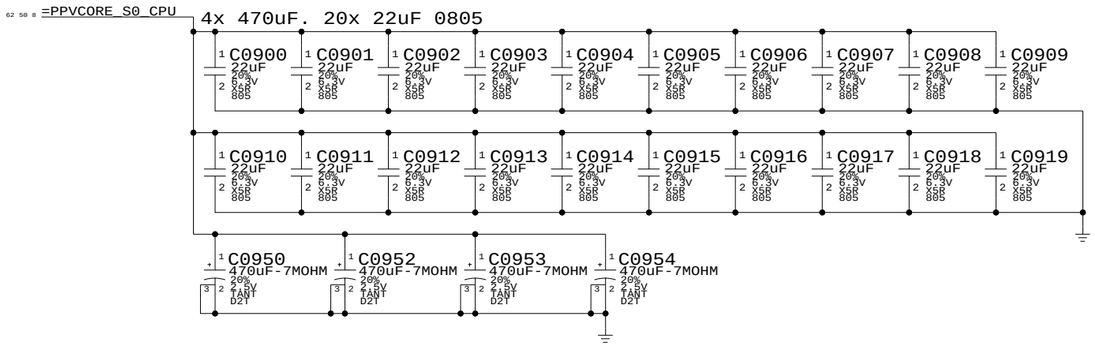
SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

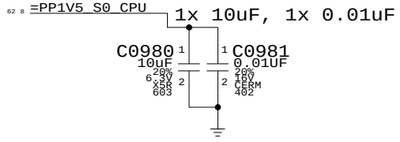
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	8	81

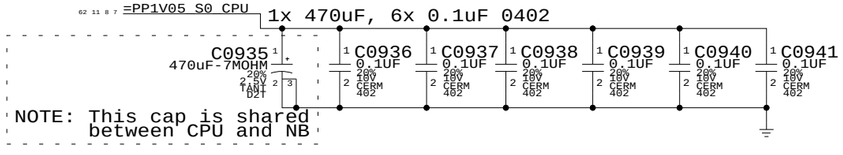
CPU VCORE HF AND BULK DECOUPLING



VCCA (CPU AVdd) Decoupling

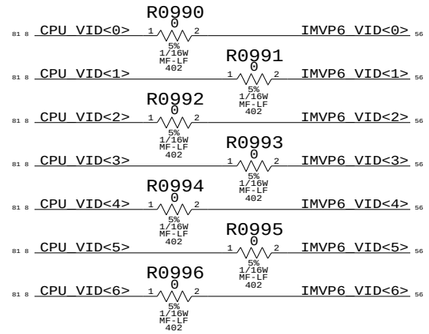


VCCP (CPU I/O) Decoupling



CPU VCORE VID Connections

Resistors to allow for override of CPU VID
Will probably be removed before production



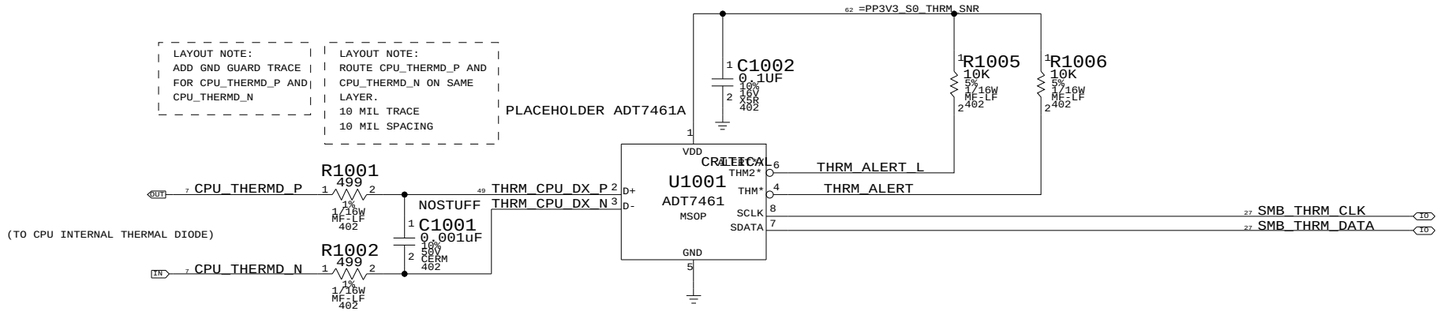
CPU Decoupling & VID

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT: 9 OF: 81	

CPU ZONE THERMAL SENSOR



PLACE U1001 NEAR THE U1200

CPU MISC1-TEMP SENSOR

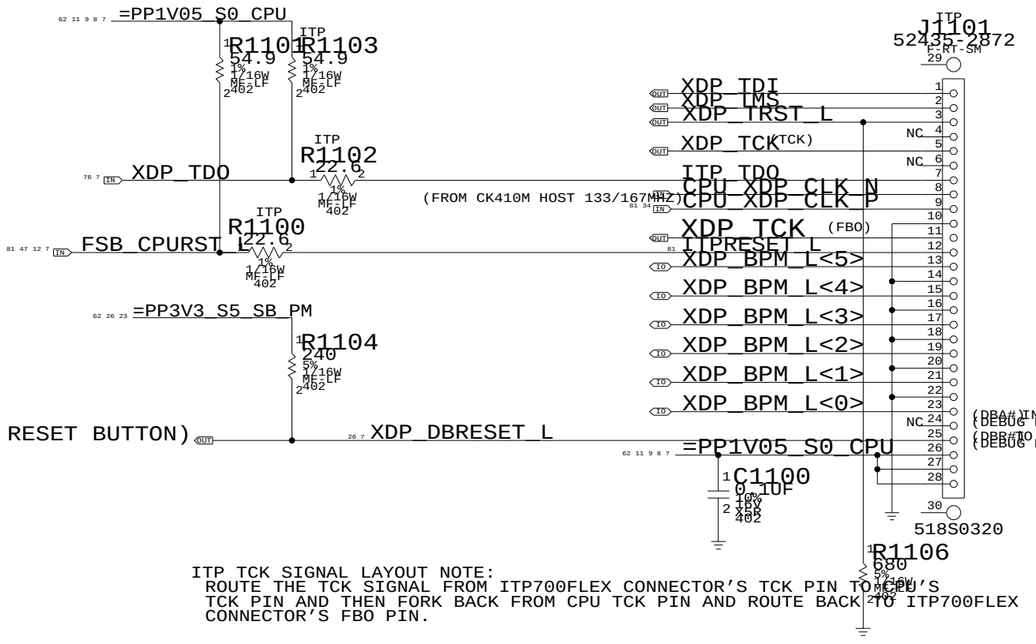
SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	10	81

CPU ITP700FLEX DEBUG SUPPORT

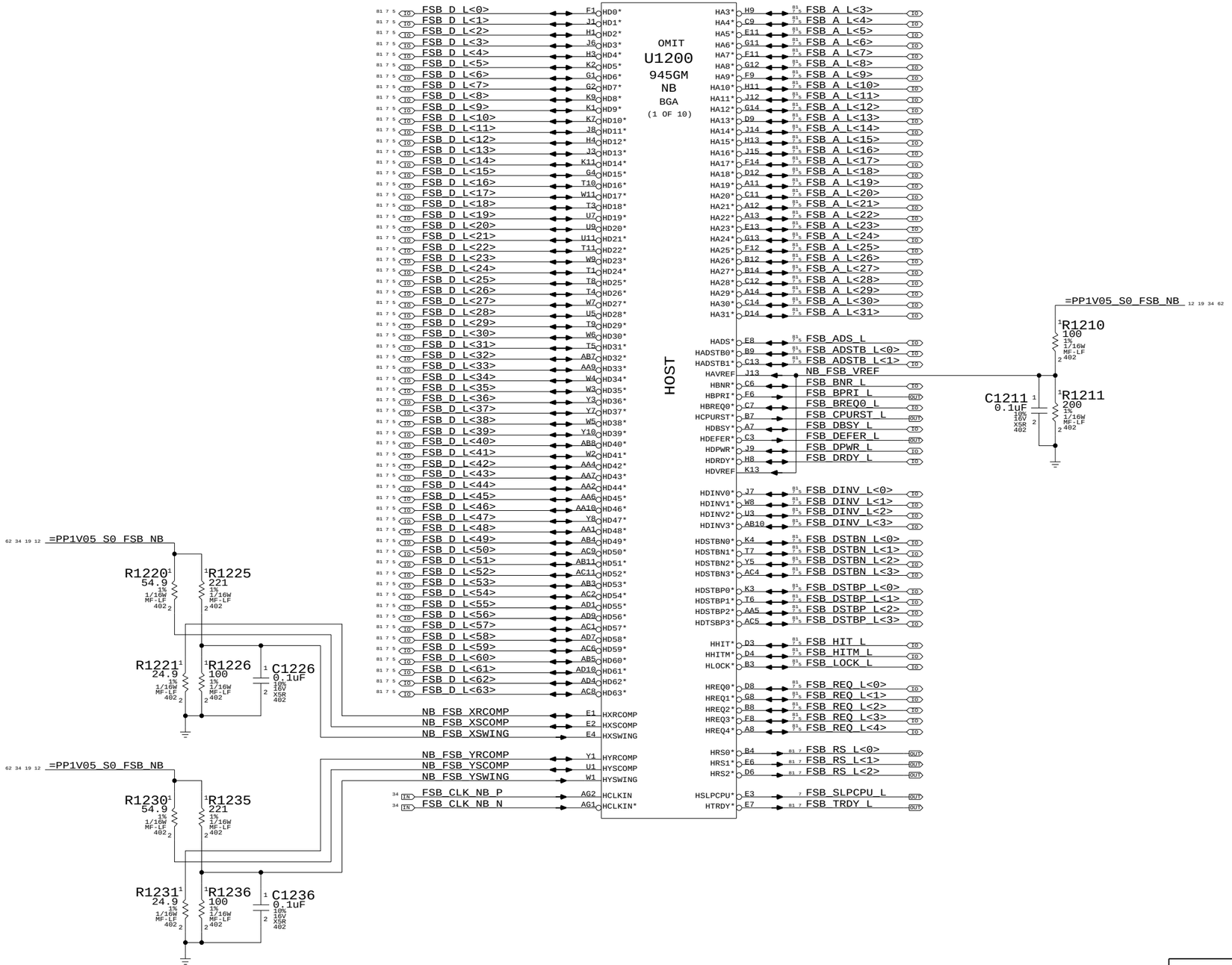


ITP TCK SIGNAL LAYOUT NOTE:
ROUTE THE TCK SIGNAL FROM ITP700FLEX CONNECTOR'S TCK PIN TO CPU'S TCK PIN AND THEN FORK BACK FROM CPU TCK PIN AND ROUTE BACK TO ITP700FLEX CONNECTOR'S FBO PIN.

CPU ITP700FLEX DEBUG

SYNC_MASTER=MSX SYNC_DATE=09/08/2005

APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE	SHT OF	
	NONE	11 81	



NB CPU Interface

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	12	81

LVDS Disable

Can leave all signals NC if LVDS is not implemented
Tie VCC_TXLVDS and VCCA_LVDS to GND. If SDVO is used
VCCD_LVDS must remain powered with proper decoupling.
Otherwise, tie VCCD_LVDS to GND also.

TV-Out Signal Usage:

Composite: DACA only
S-Video: DACB & DACC only
Component: DACA, DACB & DACC

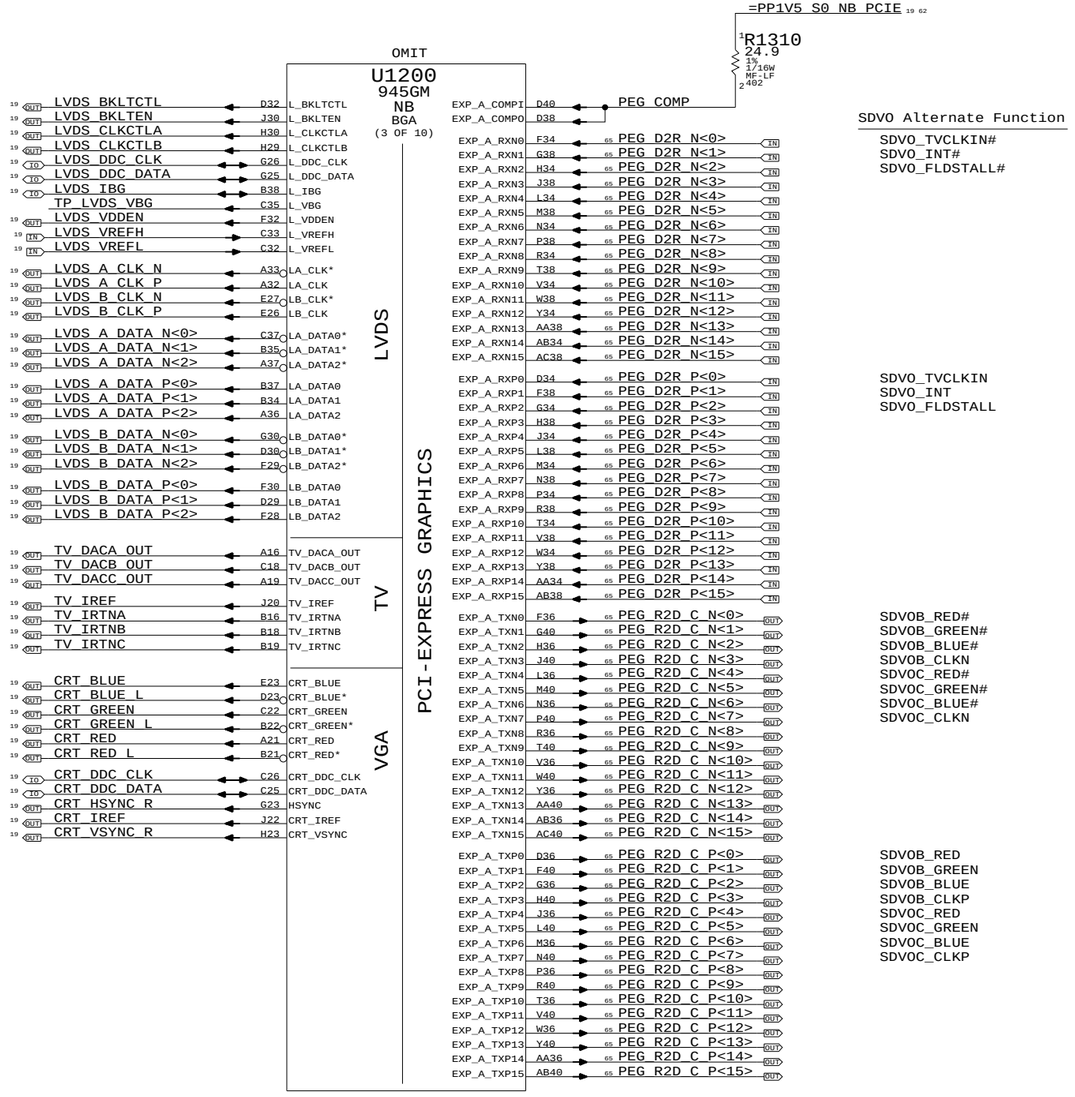
Unused DAC outputs must remain powered, but can omit filtering components. Unused DAC outputs should connect to GND through 75-ohm resistors.

TV-Out Disable

Tie DACx_OUT, IRTNx, and IREF to 1.5V power rail. Tie VCCD_TVDAC, VCCD_QTVDAC, VCCA_TVDACx, and VCCA_TVBG to 1.5V power rail. Tie VSSA_TVBG to GND.

CRT Disable

Tie R/R#/G/G#/B/B# and IREF to VCC Core rail, tie HSYNC and VSYNC to GND. Tie VCCA_CRTDAC to VCC Core rail, and tie VSSA_CRTDAC and VCC_SYNC to GND.



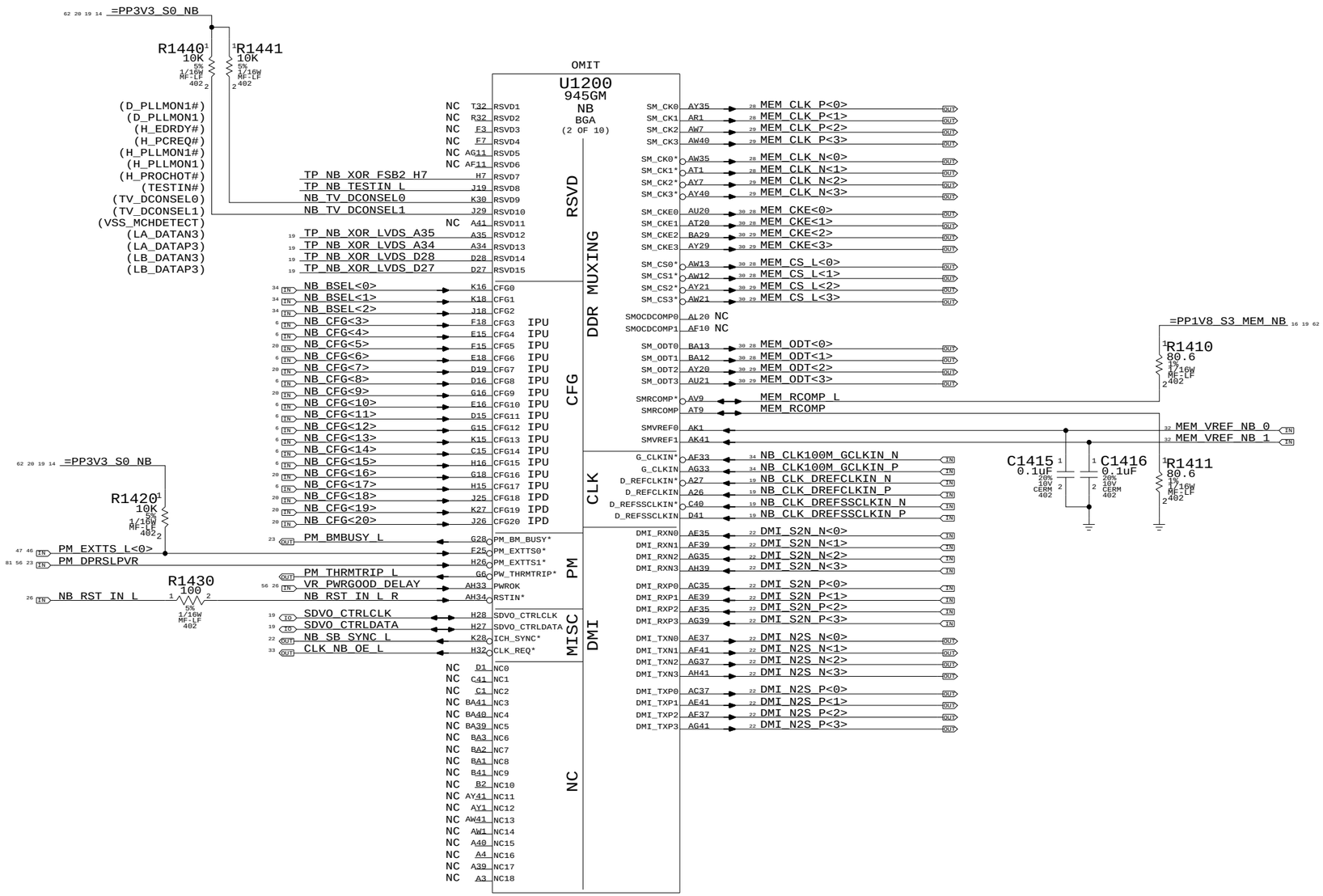
NB PEG / Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	13	81



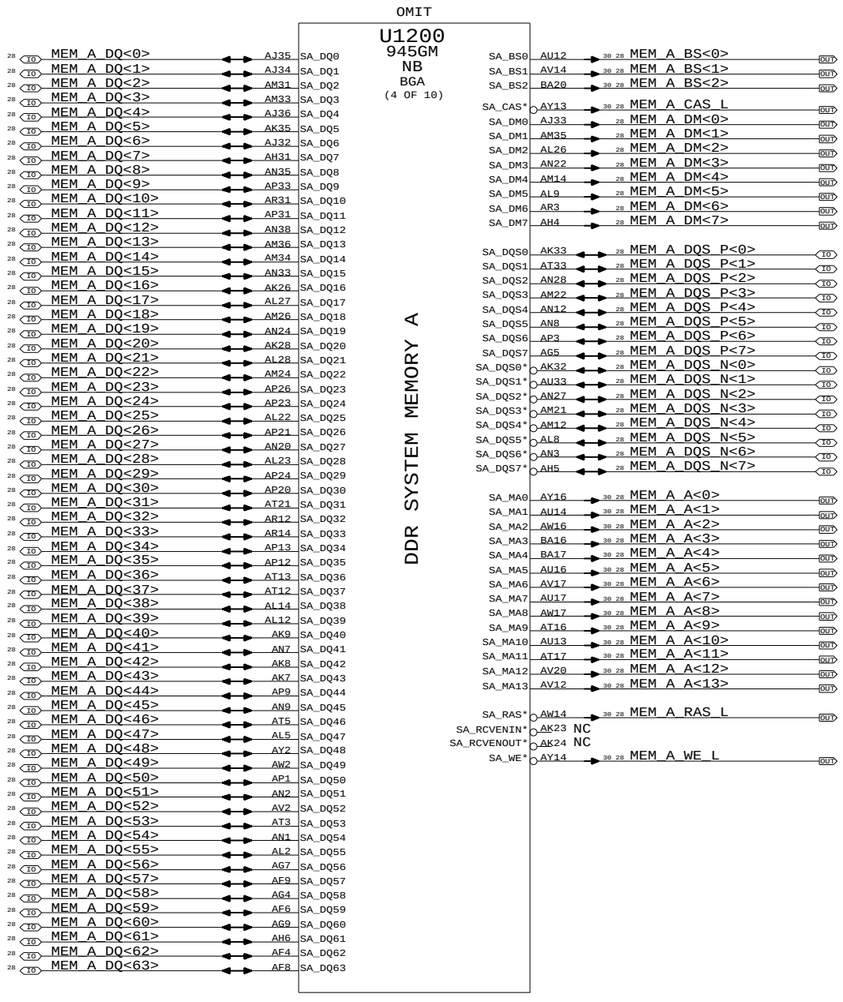
NB Misc Interfaces

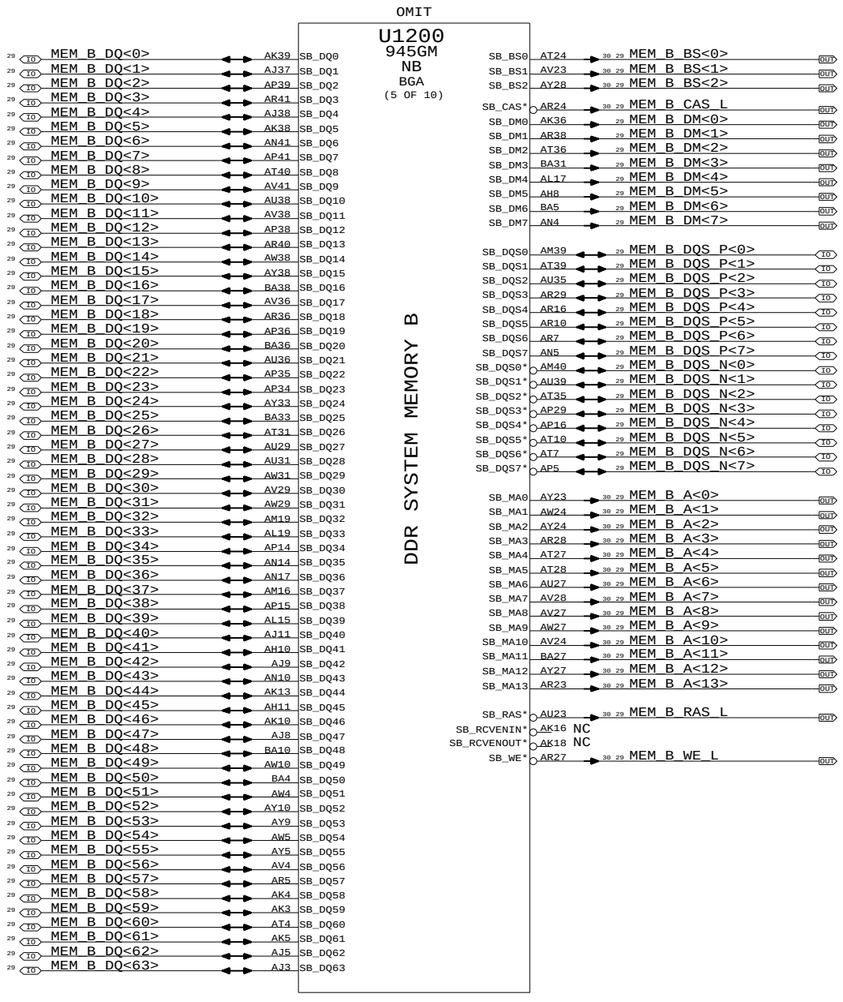
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	14	81





NB DDR2 Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 15 OF 81	

=PPVCORE_S0_NB 16 19 62
1.05V or 1.5V

1.05V, Internal Graphics: 3500mA Max
1.05V, External Graphics: 1500mA Max
1.5V, Internal Graphics: 5500mA Max

U1200
945GM
NB
BGA
(6 OF 10)
OMIT
VCC

1.8V Max Current

Speed	1 Channel	2 Channel
400MTs	1300mA	2400mA
533MTs	1500mA	2800mA
667MTs	1700mA	3200mA

NB_VCCSM_LF4
NB_VCCSM_LF5

C1614 0.47uF 20% 6.3V CERM-X5R 402
C1613 0.47uF 20% 6.3V CERM-X5R 402

C1615 0.47uF 20% 6.3V CERM-X5R 402
62 19 14 =PP1V8_S3_MEM_NB
Layout Note: Place near pin BA23

C1620 10uF 20% 6.3V X5R 603
C1621 10uF 20% 6.3V X5R 603
Layout Note: Place in cavity

C1610 0.47uF 20% 6.3V CERM-X5R 402
Layout Note: Place near pin BA15

NB_VCCSM_LF2
NB_VCCSM_LF1

C1612 0.47uF 20% 6.3V CERM-X5R 402
C1611 0.47uF 20% 6.3V CERM-X5R 402

NCTF balls are Not Critical To Function

These connections can break without impacting part performance.

62 19 16 =PPVCORE_S0_NB

OMIT

U1200
945GM
NB
BGA
(7 OF 10)
NCTF

=PP1V5_S0_NB_VCCAUX 17 19 62

AD27	VCC_NCTF0	VSS_NCTF0	AE27
AC27	VCC_NCTF1	VSS_NCTF1	AE26
AB27	VCC_NCTF2	VSS_NCTF2	AE25
AA27	VCC_NCTF3	VSS_NCTF3	AE24
Y27	VCC_NCTF4	VSS_NCTF4	AE23
W27	VCC_NCTF5	VSS_NCTF5	AE22
V27	VCC_NCTF6	VSS_NCTF6	AE21
U27	VCC_NCTF7	VSS_NCTF7	AE20
T27	VCC_NCTF8	VSS_NCTF8	AE19
R27	VCC_NCTF9	VSS_NCTF9	AE18
AD26	VCC_NCTF10	VSS_NCTF10	AC17
AC26	VCC_NCTF11	VSS_NCTF11	Y17
AB26	VCC_NCTF12	VSS_NCTF12	U17
AA26	VCC_NCTF13		
Y26	VCC_NCTF14		
W26	VCC_NCTF15		
V26	VCC_NCTF16		
U26	VCC_NCTF17		
T26	VCC_NCTF18		
R26	VCC_NCTF19		
AD25	VCC_NCTF20		
AC25	VCC_NCTF21		
AB25	VCC_NCTF22		
AA25	VCC_NCTF23		
Y25	VCC_NCTF24		
W25	VCC_NCTF25		
V25	VCC_NCTF26		
U25	VCC_NCTF27		
T25	VCC_NCTF28		
R25	VCC_NCTF29		
AD24	VCC_NCTF30		
AC24	VCC_NCTF31		
AB24	VCC_NCTF32		
AA24	VCC_NCTF33		
Y24	VCC_NCTF34		
W24	VCC_NCTF35		
V24	VCC_NCTF36		
U24	VCC_NCTF37		
T24	VCC_NCTF38		
R24	VCC_NCTF39		
AD23	VCC_NCTF40		
V23	VCC_NCTF41		
U23	VCC_NCTF42		
T23	VCC_NCTF43		
R23	VCC_NCTF44		
AD22	VCC_NCTF45		
V22	VCC_NCTF46		
U22	VCC_NCTF47		
T22	VCC_NCTF48		
R22	VCC_NCTF49		
AD21	VCC_NCTF50		
V21	VCC_NCTF51		
U21	VCC_NCTF52		
T21	VCC_NCTF53		
R21	VCC_NCTF54		
AD20	VCC_NCTF55		
V20	VCC_NCTF56		
U20	VCC_NCTF57		
T20	VCC_NCTF58		
R20	VCC_NCTF59		
AD19	VCC_NCTF60		
V19	VCC_NCTF61		
U19	VCC_NCTF62		
T19	VCC_NCTF63		
AD18	VCC_NCTF64		
AC18	VCC_NCTF65		
AB18	VCC_NCTF66		
AA18	VCC_NCTF67		
Y18	VCC_NCTF68		
W18	VCC_NCTF69		
V18	VCC_NCTF70		
U18	VCC_NCTF71		
T18	VCC_NCTF72		
		VCCAUX_NCTF0	AG27
		VCCAUX_NCTF1	AF27
		VCCAUX_NCTF2	AG26
		VCCAUX_NCTF3	AF26
		VCCAUX_NCTF4	AG25
		VCCAUX_NCTF5	AF25
		VCCAUX_NCTF6	AG24
		VCCAUX_NCTF7	AF24
		VCCAUX_NCTF8	AG23
		VCCAUX_NCTF9	AF23
		VCCAUX_NCTF10	AG22
		VCCAUX_NCTF11	AF22
		VCCAUX_NCTF12	AG21
		VCCAUX_NCTF13	AF21
		VCCAUX_NCTF14	AG20
		VCCAUX_NCTF15	AF20
		VCCAUX_NCTF16	AG19
		VCCAUX_NCTF17	AF19
		VCCAUX_NCTF18	R19
		VCCAUX_NCTF19	AG18
		VCCAUX_NCTF20	AF18
		VCCAUX_NCTF21	R18
		VCCAUX_NCTF22	AG17
		VCCAUX_NCTF23	AF17
		VCCAUX_NCTF24	AE17
		VCCAUX_NCTF25	AD17
		VCCAUX_NCTF26	AB17
		VCCAUX_NCTF27	AA17
		VCCAUX_NCTF28	W17
		VCCAUX_NCTF29	V17
		VCCAUX_NCTF30	T17
		VCCAUX_NCTF31	R17
		VCCAUX_NCTF32	AG16
		VCCAUX_NCTF33	AF16
		VCCAUX_NCTF34	AE16
		VCCAUX_NCTF35	AD16
		VCCAUX_NCTF36	AC16
		VCCAUX_NCTF37	AB16
		VCCAUX_NCTF38	AA16
		VCCAUX_NCTF39	Y16
		VCCAUX_NCTF40	W16
		VCCAUX_NCTF41	V16
		VCCAUX_NCTF42	U16
		VCCAUX_NCTF43	T16
		VCCAUX_NCTF44	R16
		VCCAUX_NCTF45	AG15
		VCCAUX_NCTF46	AF15
		VCCAUX_NCTF47	AE15
		VCCAUX_NCTF48	AD15
		VCCAUX_NCTF49	AC15
		VCCAUX_NCTF50	AB15
		VCCAUX_NCTF51	AA15
		VCCAUX_NCTF52	Y15
		VCCAUX_NCTF53	W15
		VCCAUX_NCTF54	V15
		VCCAUX_NCTF55	U15
		VCCAUX_NCTF56	T15
		VCCAUX_NCTF57	R15

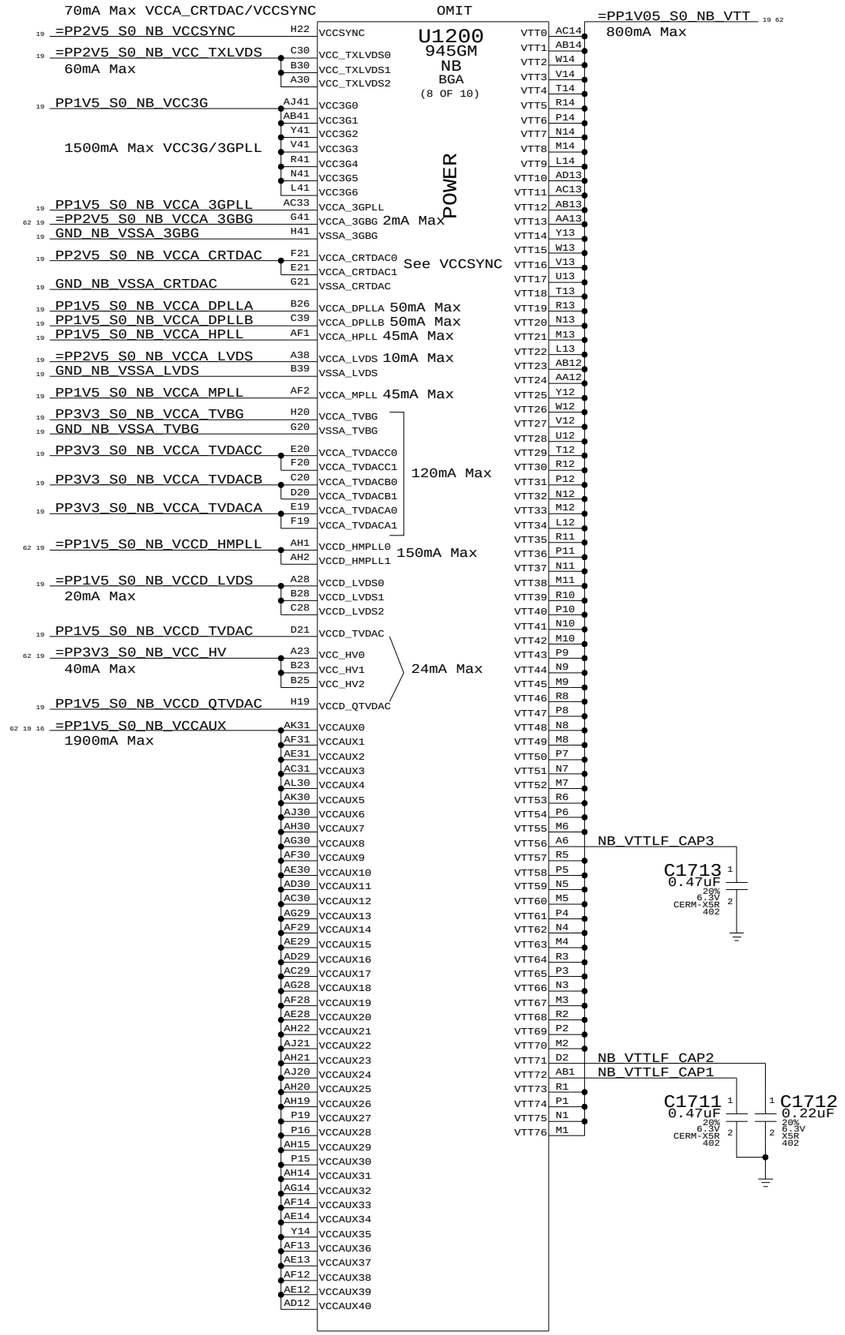
NB Power 1

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	16	81



NB Power 2

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 17 OF 81	

OMIT

U1200
945GM
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VSS

AC41	VSS_0	VSS_97	AK34
AA41	VSS_1	VSS_98	AG34
W41	VSS_2	VSS_99	AF34
T41	VSS_3	VSS_100	AE34
P41	VSS_4	VSS_101	AC34
M41	VSS_5	VSS_102	C34
J41	VSS_6	VSS_103	AW33
F41	VSS_7	VSS_104	AV33
AV40	VSS_8	VSS_105	AR33
AP40	VSS_9	VSS_106	AE33
AN40	VSS_10	VSS_107	AB33
AK40	VSS_11	VSS_108	Y33
AJ40	VSS_12	VSS_109	V33
AH40	VSS_13	VSS_110	T33
AG40	VSS_14	VSS_111	R33
AF40	VSS_15	VSS_112	M33
AE40	VSS_16	VSS_113	H33
B40	VSS_17	VSS_114	G33
AY39	VSS_18	VSS_115	F33
AW39	VSS_19	VSS_116	D33
AV39	VSS_20	VSS_117	B33
AR39	VSS_21	VSS_118	AH32
AN39	VSS_22	VSS_119	AG32
AJ39	VSS_23	VSS_120	AF32
AC39	VSS_24	VSS_121	AE32
AB39	VSS_25	VSS_122	AC32
AA39	VSS_26	VSS_123	AB32
Y39	VSS_27	VSS_124	G32
W39	VSS_28	VSS_125	B32
V39	VSS_29	VSS_126	AY31
T39	VSS_30	VSS_127	AV31
R39	VSS_31	VSS_128	AN31
P39	VSS_32	VSS_129	AJ31
N39	VSS_33	VSS_130	AG31
M39	VSS_34	VSS_131	AB31
L39	VSS_35	VSS_132	Y31
J39	VSS_36	VSS_133	AB30
H39	VSS_37	VSS_134	E30
G39	VSS_38	VSS_135	AT29
F39	VSS_39	VSS_136	AN29
D39	VSS_40	VSS_137	AB29
AT38	VSS_41	VSS_138	T29
AM38	VSS_42	VSS_139	N29
AH38	VSS_43	VSS_140	K29
AG38	VSS_44	VSS_141	G29
AF38	VSS_45	VSS_142	E29
AE38	VSS_46	VSS_143	C29
C38	VSS_47	VSS_144	B29
AK37	VSS_48	VSS_145	A29
AH37	VSS_49	VSS_146	BA28
AB37	VSS_50	VSS_147	AW28
AA37	VSS_51	VSS_148	AU28
Y37	VSS_52	VSS_149	AP28
W37	VSS_53	VSS_150	AM28
V37	VSS_54	VSS_151	AD28
T37	VSS_55	VSS_152	AC28
R37	VSS_56	VSS_153	W28
P37	VSS_57	VSS_154	J28
N37	VSS_58	VSS_155	E28
M37	VSS_59	VSS_156	AP27
L37	VSS_60	VSS_157	AM27
J37	VSS_61	VSS_158	AK27
H37	VSS_62	VSS_159	J27
G37	VSS_63	VSS_160	G27
F37	VSS_64	VSS_161	F27
D37	VSS_65	VSS_162	C27
AY36	VSS_66	VSS_163	B27
AW36	VSS_67	VSS_164	AN26
AN36	VSS_68	VSS_165	M26
AH36	VSS_69	VSS_166	K26
AG36	VSS_70	VSS_167	F26
AF36	VSS_71	VSS_168	D26
AE36	VSS_72	VSS_169	AK25
AC36	VSS_73	VSS_170	P25
C36	VSS_74	VSS_171	K25
B36	VSS_75	VSS_172	H25
BA35	VSS_76	VSS_173	E25
AV35	VSS_77	VSS_174	D25
AR35	VSS_78	VSS_175	A25
AH35	VSS_79	VSS_176	BA24
AB35	VSS_80	VSS_177	AU24
AA35	VSS_81	VSS_178	AL24
Y35	VSS_82	VSS_179	AW23
W35	VSS_83		
V35	VSS_84		
T35	VSS_85		
R35	VSS_86		
P35	VSS_87		
N35	VSS_88		
M35	VSS_89		
L35	VSS_90		
J35	VSS_91		
H35	VSS_92		
G35	VSS_93		
F35	VSS_94		
D35	VSS_95		
AN34	VSS_96		

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VSS

AT23	VSS_180	VSS_273	J11
AN23	VSS_181	VSS_274	D11
AM23	VSS_182	VSS_275	B11
AH23	VSS_183	VSS_276	AV10
AC23	VSS_184	VSS_277	AP10
W23	VSS_185	VSS_278	AL10
K23	VSS_186	VSS_279	AJ10
J23	VSS_187	VSS_280	AG10
F23	VSS_188	VSS_281	AC10
C23	VSS_189	VSS_282	W10
AA22	VSS_190	VSS_283	U10
K22	VSS_191	VSS_284	BA9
G22	VSS_192	VSS_285	AW9
F22	VSS_193	VSS_286	AR9
E22	VSS_194	VSS_287	AH9
D22	VSS_195	VSS_288	AB9
A22	VSS_196	VSS_289	Y9
BA21	VSS_197	VSS_290	R9
AV21	VSS_198	VSS_291	G9
AR21	VSS_199	VSS_292	E9
AN21	VSS_200	VSS_293	A9
AL21	VSS_201	VSS_294	AG8
AB21	VSS_202	VSS_295	AD8
Y21	VSS_203	VSS_296	AA8
P21	VSS_204	VSS_297	U8
K21	VSS_205	VSS_298	K8
J21	VSS_206	VSS_299	C8
H21	VSS_207	VSS_300	BA7
C21	VSS_208	VSS_301	AV7
AW20	VSS_209	VSS_302	AP7
AR20	VSS_210	VSS_303	AL7
AM20	VSS_211	VSS_304	AJ7
AA20	VSS_212	VSS_305	AH7
K20	VSS_213	VSS_306	AF7
B20	VSS_214	VSS_307	AC7
A20	VSS_215	VSS_308	R7
AN19	VSS_216	VSS_309	G7
AC19	VSS_217	VSS_310	D7
W19	VSS_218	VSS_311	AG6
K19	VSS_219	VSS_312	AD6
G19	VSS_220	VSS_313	AB6
C19	VSS_221	VSS_314	Y6
AH18	VSS_222	VSS_315	U6
P18	VSS_223	VSS_316	N6
H18	VSS_224	VSS_317	K6
D18	VSS_225	VSS_318	H6
A18	VSS_226	VSS_319	B6
AY17	VSS_227	VSS_320	AV5
AR17	VSS_228	VSS_321	AF5
AP17	VSS_229	VSS_322	AD5
AM17	VSS_230	VSS_323	AY4
AK17	VSS_231	VSS_324	AR4
AV16	VSS_232	VSS_325	AP4
AN16	VSS_233	VSS_326	AL4
AL16	VSS_234	VSS_327	AJ4
J16	VSS_235	VSS_328	Y4
F16	VSS_236	VSS_329	U4
C16	VSS_237	VSS_330	R4
AN15	VSS_238	VSS_331	J4
AM15	VSS_239	VSS_332	F4
AK15	VSS_240	VSS_333	C4
N15	VSS_241	VSS_334	AY3
M15	VSS_242	VSS_335	AW3
L15	VSS_243	VSS_336	AV3
B15	VSS_244	VSS_337	AL3
A15	VSS_245	VSS_338	AH3
BA14	VSS_246	VSS_339	AG3
AT14	VSS_247	VSS_340	AF3
AK14	VSS_248	VSS_341	AD3
AD14	VSS_249	VSS_342	AC3
AA14	VSS_250	VSS_343	AA3
U14	VSS_251	VSS_344	G3
K14	VSS_252	VSS_345	AT2
H14	VSS_253	VSS_346	AR2
E14	VSS_254	VSS_347	AP2
AV13	VSS_255	VSS_348	AK2
AR13	VSS_256	VSS_349	AJ2
AN13	VSS_257	VSS_350	AD2
AM13	VSS_258	VSS_351	AB2
AL13	VSS_259	VSS_352	Y2
AG13	VSS_260	VSS_353	U2
P13	VSS_261	VSS_354	T2
F13	VSS_262	VSS_355	N2
D13	VSS_263	VSS_356	J2
B13	VSS_264	VSS_357	H2
AY12	VSS_265	VSS_358	F2
AC12	VSS_266	VSS_359	C2
K12	VSS_267	VSS_360	AL1
H12	VSS_268		
E12	VSS_269		
AD11	VSS_270		
AA11	VSS_271		
Y11	VSS_272		

NB Grounds

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	18	81

Power Interface

These are the power signals that leave the NB "block"

Rail Totals:

2310mA Max?	=PPVCORE_S0_NB	16 19 62	1500mA Max
	=PP1V05_S0_FSB_NB	12 34 62	10mA Max?
	=PP1V05_S0_NB_VTT	17 19 62	800mA Max
	=PP1V05_S0_NB_CRT	19 62	?mA Max
3674mA Max	=PP1V5_S0_NB	62	?mA Max
	=PP1V5_S0_NB_3G	19 62	1500mA Max
	=PP1V5_S0_NB_3GPLL	19 62	
	=PP1V5_S0_NB_PCIE	13 62	?mA Max
	=PP1V5_S0_NB_PLL	19 62	100mA Max
	=PP1V5_S0_NB_TVDAC	19 62	24mA Max
	=PP1V5_S0_NB_VCCD_HMPLL	17 62	150mA Max
	=PP1V5_S0_NB_VCCAUX	16 17 19 62	1900mA Max
3200mA Max	=PP1V8_S3_MEM_NB	14 16 62	3200mA Max
	=PP2V5_S0_NB_VCCSYNC	17 19	70mA Max
132mA Max	=PP2V5_S0_NB_VCC_TXLVDS	17 19	60mA Max
	=PP2V5_S0_NB_VCCA_3GBG	17 19 62	2mA Max
	=PP3V3_S0_NB	14 20 62	?mA Max
40mA Max?	=PP3V3_S0_NB_VCC_HV	17 19 62	40mA Max

62 19 =PP1V05_S0_NB_CRT
- CRT_RED — 13
- CRT_GREEN — 13
- CRT_BLUE — 13
- CRT_RED_L — 13
- CRT_GREEN_L — 13
- CRT_BLUE_L — 13
- CRT_IREF — 13
- CRT_HSYNC_R — 13
- CRT_VSYNC_R — 13

TP_CRT_DDC_CLK (MAKE_BASE=TRUE) — CRT_DDC_CLK — 13
TP_CRT_DDC_DATA (MAKE_BASE=TRUE) — CRT_DDC_DATA — 13

62 19 =PP1V5_S0_NB_TVDAC
- TV_DACA_OUT — 13
- TV_DACB_OUT — 13
- TV_DACC_OUT — 13
- TV_IREF — 13
- TV_IRTNA — 13
- TV_IRTNB — 13
- TV_IRTNC — 13

TP_LVDS_BKLTCTL (MAKE_BASE=TRUE) — LVDS_BKLTCTL — 13
TP_LVDS_BKLTEN (MAKE_BASE=TRUE) — LVDS_BKLTEN — 13
TP_LVDS_CLKCTLA (MAKE_BASE=TRUE) — LVDS_CLKCTLA — 13
TP_LVDS_CLKCTLB (MAKE_BASE=TRUE) — LVDS_CLKCTLB — 13
TP_LVDS_DDC_CLK (MAKE_BASE=TRUE) — LVDS_DDC_CLK — 13
TP_LVDS_DDC_DATA (MAKE_BASE=TRUE) — LVDS_DDC_DATA — 13
NC_LVDS_IBG (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_IBG — 13
TP_LVDS_VDDEN (MAKE_BASE=TRUE) — LVDS_VDDEN — 13
NC_LVDS_VREFH (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_VREFH — 13
TP_LVDS_VREFL (MAKE_BASE=TRUE) — LVDS_VREFL — 13
NC_LVDS_A_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_P — 13
NC_LVDS_A_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_CLK_N — 13
NC_LVDS_A_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_P<2..0> — 13
NC_LVDS_A_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_A_DATA_N<2..0> — 13
NC_LVDS_B_CLKP (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_P — 13
NC_LVDS_B_CLKN (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_CLK_N — 13
NC_LVDS_B_DATAP<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_P<2..0> — 13
NC_LVDS_B_DATAN<2..0> (MAKE_BASE=TRUE NO_TEST=TRUE) — LVDS_B_DATA_N<2..0> — 13
NC_NB_XOR_LVDS_A34 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A34 — 14
NC_NB_XOR_LVDS_A35 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_A35 — 14
NC_NB_XOR_LVDS_D27 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D27 — 14
NC_NB_XOR_LVDS_D28 (MAKE_BASE=TRUE NO_TEST=TRUE) — TP_NB_XOR_LVDS_D28 — 14
TP_SDVO_CTRLCLK (MAKE_BASE=TRUE) — SDVO_CTRLCLK — 14
TP_SDVO_CTRLDATA (MAKE_BASE=TRUE) — SDVO_CTRLDATA — 14

(MCH LVDS DATA/CLK TX 2.5V PWR) =PP2V5_S0_NB_VCC_TXLVDS — 17 19
(MCH LVDS DIGITAL 1.5V PWR) =PP1V5_S0_NB_VCCD_LVDS — 17
(MCH LVDS ANALOG 2.5V PWR) =PP2V5_S0_NB_VCCA_LVDS — 17

NC_GND_NB_VSSA_LVDS (MAKE_BASE=TRUE NO_TEST=TRUE) — GND_NB_VSSA_LVDS — 17

62 19 16 =PPVCORE_S0_NB
- (MCH CRTDAC ANALOG 2.5V PWR) PP2V5_S0_NB_VCCA_CRTDAC — 17
- GND_NB_VSSA_CRTDAC — 17
- (MCH H/V SYNC 2.5V PWR) =PP2V5_S0_NB_VCCSYNC — 17 19

62 19 =PP1V5_S0_NB_TVDAC
- (MCH TV OUT CHANNEL A 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACA — 17
- (MCH TV OUT CHANNEL B 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACB — 17
- (MCH TV OUT CHANNEL C 3.3V PWR) PP3V3_S0_NB_VCCA_TVDACC — 17
- (MCH TV DAC BAND GAP 3.3V PWR) PP3V3_S0_NB_VCCA_TVBG — 17
- GND_NB_VSSA_TVBG — 17

(MCH DISPLAY A PLL 1.5V PWR)
TP_NB_VCCA_DPLLA (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLA — 17
(MCH DISPLAY B PLL 1.5V PWR)
TP_NB_VCCA_DPLLB (MAKE_BASE=TRUE) — PP1V5_S0_NB_VCCA_DPLLB — 17

- NB_CLK_DREFCLKIN_P — 14
- NB_CLK_DREFCLKIN_N — 14
- NB_CLK_DREFSSCLKIN_P — 14
- NB_CLK_DREFSSCLKIN_N — 14

62 19 16 =PPVCORE_S0_NB 1500mA Max — GMCH CORE PWR 1.05V BYPASS
- C1900 470uF-7MOHM 20% 2.5V TANT D2T
- C1902 10uF 20% 6.3V X5R 603
- C1903 10uF 20% 6.3V X5R 603
- C1904 1uF 10% 6.3V CERM 402
- C1905 0.22uF 10% 6.3V X5R 402
- C1906 0.22uF 10% 6.3V X5R 402
- C1907 0.22uF 10% 6.3V X5R 402

62 19 17 =PP1V05_S0_NB_VTT 800mA Max — MCH VTT BYPASS (MCH FSB 1.05V PWR) (SHARE C0940 470UF)
- C1965 4.7uF 20% 6.3V CERM 603 — Layout Note: Place in cavity
- C1966 2.2uF 20% 6.3V CERM1 603
- C1967 0.22uF 20% 6.3V X5R 402 — Layout Note: Place on the edge

62 19 17 =PP3V3_S0_NB_VCC_HV 40mA Max — MCH VCC_HV BYPASS (MCH HV BUFFER 3.3V PWR)
- C1914 10uF 20% 6.3V X5R 603
- C1915 0.1uF 20% 10V CERM 402

62 19 17 =PP2V5_S0_NB_VCCA_3GBG 2mA Max — MCH VCCA_3GBG BYPASS (MCH PCIE/DMI BAND GAP 2.5V PWR)
- C1916 0.1uF 20% 10V CERM 402

62 19 17 16 =PP1V5_S0_NB_VCCAUX 1900mA Max — GMCH VCCAUX FILTER (MCH DDR DLL&IO, FSB HSIO&IO PWR 1.5V)
- C1918 0.1uF 20% 10V CERM 402

62 19 =PP1V5_S0_NB_TVDAC 24mA Max — GMCH VCCD_TVDAC FILTER (MCH TVDAC DEDICATED PWR 1.5V)
- C1921 22000pF-1000mA 10V NPM18
- PP1V5_S0_NB_VCCD_TVDAC — 17 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V — 24mA Max TVDAC/QTVDAC
- C1920 0.1uF 20% 10V CERM 402 — Layout Note: These 4 caps should be within 6.35 mm of NB edge

GMCH VCCD_QTVDAC FILTER (MCH TVDAC DIGITAL QUIET 1.5V PWR)
- C1923 22000pF-1000mA 10V NPM18
- PP1V5_S0_NB_VCCD_QTVDAC — 17 — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
- L1922 180-OHM-1.5A 0603 — PP1V5_S0_NB_QTVDAC — MIN_LINE_WIDTH=0.25 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
- C1922 0.1uF 20% 10V CERM 402

1500mA Max — GMCH VCC3G FILTER (PCI-E/DMI ANALOG 1.5V PWR)

62 19 =PP1V5_S0_NB_3G — L1970 91nH 1210 — Layout Note: Place L and C close to MCH
- C1970 220UF 20% 2.5V POLY SMB2
- C1971 10uF 20% 6.3V X5R 603
- C1972 10uF 20% 6.3V X5R 603 — Layout Note: 10uF caps should be close to MCH on opposite side.
- PP1V5_S0_NB_VCC3G — 17 — MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V

62 19 =PP1V5_S0_NB_3GPLL — L1975 1.0UH-220MA-0.12-OHM 0805 — PP1V5_S0_NB_3GPLL_F — MIN_LINE_WIDTH=0.6 mm MIN_NECK_WIDTH=0.4 mm VOLTAGE=1.5V
- R1975 0.51 1% 1/10W MF-LF 402
- C1975 10uF 20% 6.3V X5R 603
- C1976 0.1uF 20% 10V CERM 402
- GMCH VCCA_3GPLL FILTER (3GIO PLL 1.5V PWR)
- PP1V5_S0_NB_VCCA_3GPLL — 17 — MIN_LINE_WIDTH=0.5 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V
- GND_NB_VSSA_3GBG — 17
- Layout Note: 3GPLL 10uF cap should be placed in cavity
- Layout Note: Route to caps, then GND

1500mA Max

62 19 =PP1V5_S0_NB_PLL 100mA Max — GMCH VCCA_HPLL FILTER (HOST PLL 1.5V PWR)
- L1934 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_HPLL — 17 — MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V — 45mA Max
- C1934 22uF 20% 6.3V X5R 805
- C1935 0.1uF 20% 10V CERM 402

GMCH VCCA_MPLL FILTER (MCH MEMORY PLL 1.5V PWR)
- L1936 FERR-120-OHM-0.2A 0603 — PP1V5_S0_NB_VCCA_MPLL — 17 — MIN_LINE_WIDTH=0.38 mm MIN_NECK_WIDTH=0.25 mm VOLTAGE=1.5V — 45mA Max
- C1936 22uF 20% 6.3V X5R 805
- C1937 0.1uF 20% 10V CERM 402

NB (GM) Decoupling

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE D | DRAWING NUMBER 051-6941 | REV. 07001

SCALE NONE | SHT 19 OF 81

NB_CFG<3>	RESERVED

NB_CFG<4>	RESERVED

14 NB_CFG<5>
Internal pull-up

NB_CFG<5> DMI x2 Select	High = DMIx4 Low = DMIx2

NBCFG_DMI_X2
1 R2075
2.2K
5%
1/16W
MF-LF
2 402

PROBABLY NOT NEEDED

NB_CFG<6>	RESERVED

14 NB_CFG<7>
Internal pull-up

NB_CFG<7> CPU Strap	High = Mobile CPU Low = RESERVED

NO STUFF
1 R2077
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<8>	RESERVED

14 NB_CFG<9>
Internal pull-up

NB_CFG<9> PCIE Graphics Lane Reversal	High = Normal Low = Reversed

NBCFG_PEG_REVERSE
1 R2079
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<10>	RESERVED

NB_CFG<11>	RESERVED

Internal pull-ups

NB_CFG<13:12>	00 = Partial Clock Gating Disable 01 = XOR Mode Enabled 10 = All-Z Mode Enabled 11 = Normal Operation

NB_CFG<14>	RESERVED

NB_CFG<15>	RESERVED

14 NB_CFG<16>
Internal pull-up

NB_CFG<16> FSB Dynamic ODT	High = Enabled Low = Disabled

NBCFG_DYN_ODT_DISABLE
1 R2085
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<17>	RESERVED

=PP3V3_S0_NB 14 19 20 62
NBCFG_VCC_1V5
1 R2058
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<18> VCC Select	High = 1.5V Low = 1.05V

14 NB_CFG<18>
Internal pull-down

=PP3V3_S0_NB 14 19 20 62
NBCFG_DMI_REVERSE
1 R2059
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<19> DMI Lane Reversal	High = Reversed Low = Normal

14 NB_CFG<19>
Internal pull-down

945 External Design Spec says reserved

=PP3V3_S0_NB 14 19 20 62
NBCFG_SDVO_AND_PCIE
1 R2060
2.2K
5%
1/16W
MF-LF
2 402

NB_CFG<20> PCIe Backward Interop. Mode	High = Both active Low = Only SDVO or PCIe x1

14 NB_CFG<20>
Internal pull-down

PROBABLY NOT NEEDED

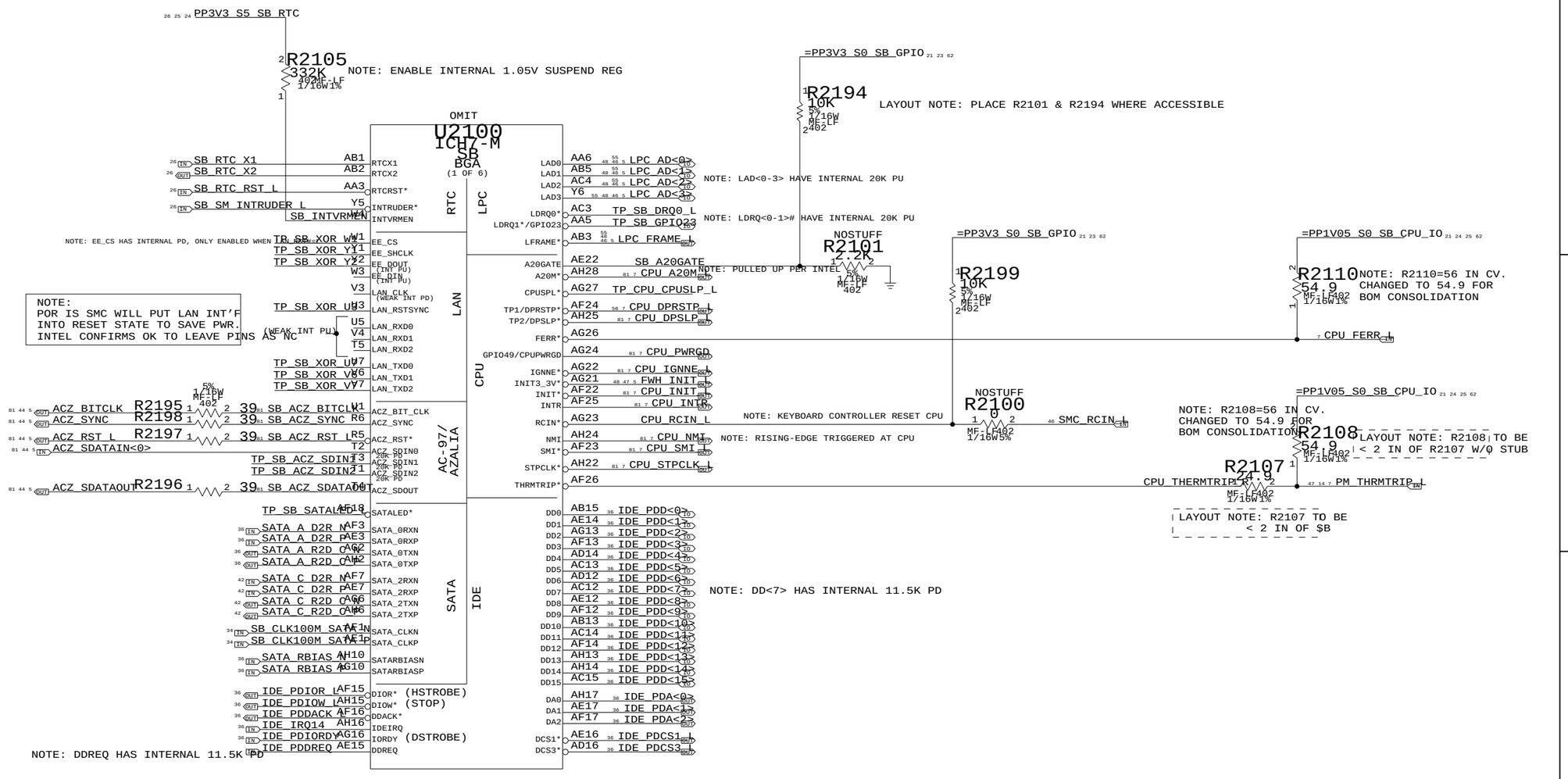
NB Config Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	20	81



	AC '07	INTEL HIGH DEFINITION AUDIO
ACZ_BIT_CLK	INTERNAL 20K PD ENABLED WHEN	INTERNAL 20K PD ONLY ENABLED IN S3COLD
ACZ_RST#	- LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	NONE
ACZ_SDIN[0-2]	INTERNAL 20K PD	INTERNAL 20K PD
ACZ_SDOUT	INTERNAL 20K PD ENABLED DURING RESET AND WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED	INTERNAL 20K PD ENABLED WHEN - LSO BIT IN AC'97 GLOBAL CONTROL REG = 1; OR - BOTH FUNCTION 2 & 3 OF DEVICE 30 ARE DISABLED
ACZ_SYNC		INTERNAL 20K PD

SB: 1 OF 4

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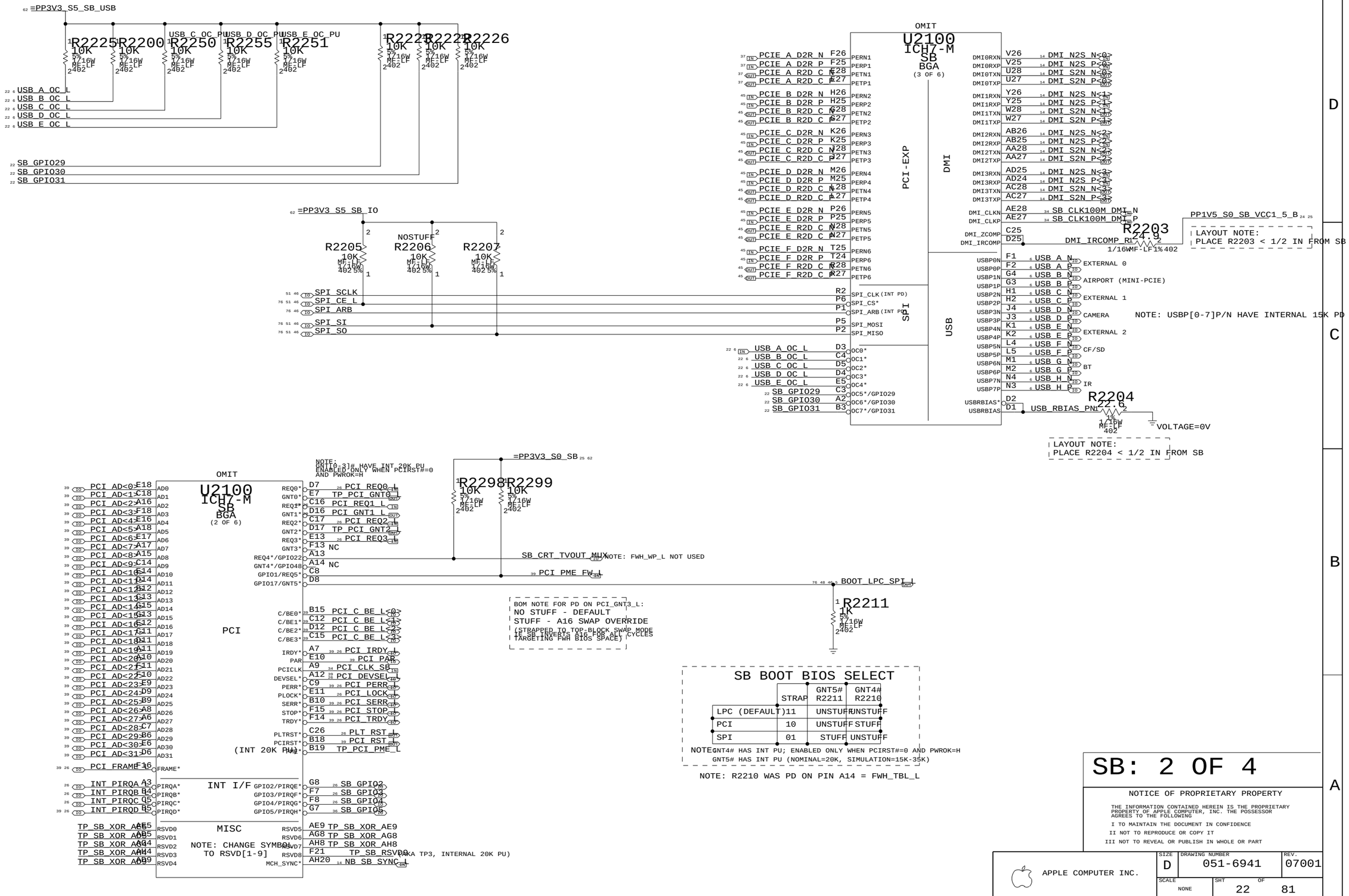
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT: 21	OF: 81


=PP3V3_S5_SB_USB
R2225 10K 5% 1/16W MF-LF 402
R2200 10K 5% 1/16W MF-LF 402
R2250 10K 5% 1/16W MF-LF 402
R2255 10K 5% 1/16W MF-LF 402
R2251 10K 5% 1/16W MF-LF 402
R2227 10K 5% 1/16W MF-LF 402
R2228 10K 5% 1/16W MF-LF 402
R2226 10K 5% 1/16W MF-LF 402
USB_C_OC_PU
USB_D_OC_PU
USB_E_OC_PU
USB_A_OC_L
USB_B_OC_L
USB_C_OC_L
USB_D_OC_L
USB_E_OC_L
SB_GPIO29
SB_GPIO30
SB_GPIO31
=PP3V3_S5_SB_IO
R2205 10K 5% 1/16W 402
NOSTUFF
R2206 10K 5% 1/16W 402
R2207 10K 5% 1/16W 402
SPI_SCLK
SPI_CE_L
SPI_ARB
SPI_SI
SPI_SO
OMIT
U2100
ICH7-M
SB
BGA
(3 OF 6)
PCIE_A_D2R_N F26
PCIE_A_D2R_P F25
PCIE_A_R2D_C_N G28
PCIE_A_R2D_C_P G27
PCIE_B_D2R_N H26
PCIE_B_D2R_P H25
PCIE_B_R2D_C_N G28
PCIE_B_R2D_C_P G27
PCIE_C_D2R_N K26
PCIE_C_D2R_P K25
PCIE_C_R2D_C_N J28
PCIE_C_R2D_C_P J27
PCIE_D_D2R_N M26
PCIE_D_D2R_P M25
PCIE_D_R2D_C_N L28
PCIE_D_R2D_C_P L27
PCIE_E_D2R_N P26
PCIE_E_D2R_P P25
PCIE_E_R2D_C_N N28
PCIE_E_R2D_C_P N27
PCIE_F_D2R_N T25
PCIE_F_D2R_P T24
PCIE_F_R2D_C_N R28
PCIE_F_R2D_C_P R27
PCI-EXP
SPI_CLK (INT PD) R2
SPI_CS* P6
SPI_ARB (INT PU) P1
SPI_MOSI P5
SPI_MISO P2
SPI
USB_A_OC_L D3
USB_B_OC_L C4
USB_C_OC_L D5
USB_D_OC_L D4
USB_E_OC_L E5
SB_GPIO29 C3
SB_GPIO30 A2
SB_GPIO31 B3
OC0*
OC1*
OC2*
OC3*
OC4*
OC5*/GPIO29
OC6*/GPIO30
OC7*/GPIO31
DMI
DMI0RXN V26
DMI0RXP V25
DMI0TXN U28
DMI0TXP U27
DMI1RXN Y26
DMI1RXP Y25
DMI1TXN W28
DMI1TXP W27
DMI2RXN AB26
DMI2RXP AB25
DMI2TXN AA28
DMI2TXP AA27
DMI3RXN AD25
DMI3RXP AD24
DMI3TXN AC28
DMI3TXP AC27
DMI_CLKN AE28
DMI_CLKP AE27
DMI_ZCOMP C25
DMI_IRCOMP D25
DMI_N2S_N<0>
DMI_N2S_P<0>
DMI_S2N_N<0>
DMI_S2N_P<0>
DMI_N2S_N<1>
DMI_N2S_P<1>
DMI_S2N_N<1>
DMI_S2N_P<1>
DMI_N2S_N<2>
DMI_N2S_P<2>
DMI_S2N_N<2>
DMI_S2N_P<2>
DMI_N2S_N<3>
DMI_N2S_P<3>
DMI_S2N_N<3>
DMI_S2N_P<3>
SB_CLK100M_DMI_N
SB_CLK100M_DMI_P
R2203 24.9 1/16W MF-LF 1% 402
PP1V5_S0_SB_VCC1_5_B
LAYOUT NOTE:
PLACE R2203 < 1/2 IN FROM SB
USB
USBP0N F1
USBP0P F2
USBP1N G4
USBP1P G3
USBP2N H1
USBP2P H2
USBP3N J4
USBP3P J3
USBP4N K1
USBP4P K2
USBP5N L4
USBP5P L5
USBP6N M1
USBP6P M2
USBP7N N4
USBP7P N3
USB_A_N
USB_A_P
USB_B_N
USB_B_P
USB_C_N
USB_C_P
USB_D_N
USB_D_P
USB_E_N
USB_E_P
USB_F_N
USB_F_P
USB_G_N
USB_G_P
USB_H_N
USB_H_P
EXTERNAL 0
AIRPORT (MINI-PCIE)
EXTERNAL 1
CAMERA
EXTERNAL 2
CF/SD
BT
IR
NOTE: USBP[0-7]P/N HAVE INTERNAL 15K PD
USBRBIAS* D2
USBRBIAS D1
R2204 22.6 1/16W MF-LF 1% 402
USB_RBIAS_PN
VOLTAGE=0V
LAYOUT NOTE:
PLACE R2204 < 1/2 IN FROM SB
NOTE: GNT0,3]# HAVE INT 20K PU
ENABLED ONLY WHEN PCIRST#=0
AND PWROK=H
=PP3V3_S0_SB
R2298 10K 5% 1/16W MF-LF 402
R2299 10K 5% 1/16W MF-LF 402
SB_CRT_TVOUT_MUX
NOTE: FWH_WP_L NOT USED
PCI_PME_FW_L
BOOT_LPC_SPI_L
R2211 1K 5% 1/16W MF-LF 402
BOM NOTE FOR PD ON PCI_GNT3_L:
NO STUFF - DEFAULT
STUFF - A16 SWAP OVERRIDE
(STRAPPED TO TOP-BLOCK SWAP MODE
IF SB INVERTS A16 FOR ALL CYCLES
TARGETING FWH BIOS SPACE)
PCI
PCI_AD<0> E18
PCI_AD<1> C18
PCI_AD<2> A16
PCI_AD<3> F18
PCI_AD<4> E16
PCI_AD<5> A18
PCI_AD<6> E17
PCI_AD<7> A17
PCI_AD<8> A15
PCI_AD<9> C14
PCI_AD<10> E14
PCI_AD<11> D14
PCI_AD<12> B12
PCI_AD<13> C13
PCI_AD<14> A13
PCI_AD<15> C12
PCI_AD<16> E12
PCI_AD<17> C11
PCI_AD<18> D11
PCI_AD<19> A11
PCI_AD<20> A10
PCI_AD<21> F11
PCI_AD<22> F10
PCI_AD<23> E9
PCI_AD<24> D9
PCI_AD<25> B9
PCI_AD<26> A8
PCI_AD<27> A6
PCI_AD<28> C7
PCI_AD<29> B6
PCI_AD<30> E6
PCI_AD<31> D6
PCI_FRAME# F16
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
FRAME*
C/BE0* B15 PCI_C_BE_L<0>
C/BE1* C12 PCI_C_BE_L<1>
C/BE2* D12 PCI_C_BE_L<2>
C/BE3* C15 PCI_C_BE_L<3>
IRDY* A7 PCI_IRDY
PAR E10 PCI_PAR
PCICLK A9 PCI_CLK_SB
DEVSEL* A12 PCI_DEVSEL_L
PERR* C9 PCI_PERR
PLOCK* E11 PCI_LOCK
SERR* B10 PCI_SERR
STOP* F15 PCI_STOP
TRDY* F14 PCI_TRDY
PLTRST* C26 PLT_RST
PCIRST* B18 PCI_RST
(INT 20K PU) B19 TP_PCI_PME_L
INT I/F
INT_PIRQA A3
INT_PIRQB B4
INT_PIRQC C5
INT_PIRQD B5
PIRQA*
PIRQB*
PIRQC*
PIRQD*
GPIO2/PIRQE* G8 SB_GPIO2
GPIO3/PIRQF* F7 SB_GPIO3
GPIO4/PIRQG* F8 SB_GPIO4
GPIO5/PIRQH* G7 SB_GPIO5
MISC
NOTE: CHANGE SYMBOL TO RSVD[1-9]
TP_SB_XOR_AE5
TP_SB_XOR_AD5
TP_SB_XOR_AG4
TP_SB_XOR_AH4
TP_SB_XOR_AD9
RSVD0
RSVD1
RSVD2
RSVD3
RSVD4
REQ0* D7 PCI_REQ0_L
GNT0* E7 TP_PCI_GNT0_L
REQ1* C16 PCI_REQ1_L
GNT1* D16 PCI_GNT1_L
REQ2* C17 PCI_REQ2_L
GNT2* D17 TP_PCI_GNT2_L
REQ3* E13 PCI_REQ3_L
GNT3* F13 NC
REQ4*/GPIO22 A13
GNT4*/GPIO48 A14 NC
GPIO1/REQ5* C8
GPIO17/GNT5* D8
AE9 TP_SB_XOR_AE9
AG8 TP_SB_XOR_AG8
AH8 TP_SB_XOR_AH8
F21 TP_SB_RSVD21 (AKA TP3, INTERNAL 20K PU)
AH20 NB_SB_SYNC_L
RSVD5
RSVD6
RSVD7
RSVD8
MCH_SYNC*
SB BOOT BIOS SELECT
STRAP GNT5# R2211 GNT4# R2210
LPC (DEFAULT) 11 UNSTUFF UNSTUFF
PCI 10 UNSTUFF STUFF
SPI 01 STUFF UNSTUFF
NOTE: GNT4# HAS INT PU; ENABLED ONLY WHEN PCIRST#=0 AND PWROK=H
GNT5# HAS INT PU (NOMINAL=20K, SIMULATION=15K-35K)
NOTE: R2210 WAS PD ON PIN A14 = FWH_TBL_L
SB: 2 OF 4
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REV. 07001
SCALE NONE
SHT 22 OF 81

NOTE FOR R2323 (DEF=NOSTUFF)
STRAPPING @ PWROK RISING:
SB WILL DISABLE TCO TIMER
SYSTEM REBOOT FEATURE

=PP3V3_S0_SB_GPIO 21 23 62

=PP3V3_S5_SB 23 25 62

NO_REBOOT_MODE

R2318 10K 1/16W 402 2MF-LF 5%
R2395 8.2K 1/16W 402 2MF-LF 5%
R2396 10K 1/16W 402 2MF-LF 5%
R2397 8.2K 1/16W 402 2MF-LF 5%
R2327 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2326 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2323 1K 1/16W 402 2MF-LF 5%

RP2300 10K 5% 1/16W 5M-LF

=PP3V3_S5_SB 62 25 23

R2398 1K 1/16W 402 2MF-LF 5%
R2320 10K 1/16W 402 2MF-LF 5%
R2317 10K 1/16W 402 2MF-LF 5%
R2316 10K 1/16W 402 2MF-LF 5%

OMIT
U2100
ICH7-M SB
BGA
(4 OF 6)

SMB_CLK 27 IO — C22 SMBCLK
SMB_DATA 27 IO — B22 SMBDATA
SMB_LINK_ALERT_L — A16 SMLINKALERT*
SMLINK<0> — B25 SMLINK0
SMLINK<1> — A25 SMLINK1
NOT USED
PM_RI_L — A28 RI*
SB_SPKR — A19 SPKR (INT WEAK PD)
PM_SUS_STAT_L 55 48 46 5 OUT — A27 SUS_STAT*
PM_SYSRST_L 46 26 IN — A22 SYS_RST*
PM_BMBUSY_L 14 IN — AB18 GPIO0/BM_BUSY*
SMB_ALERT_L — B23 GPIO11/SMBALERT*
NOTE: RESERVED FOR FUTURE
PM_STPPCI_L 33 OUT — AC20 GPIO18/STPPCI*
PM_STPCPU_L 33 OUT — AF21 GPIO20/STPCPU*
SB_GPIO26 — A21 GPIO26
BIOS_REC 23 — B21 GPIO27
FWH_MFG_MODE 23 — E23 GPIO28
PM_CLKRUN_L 55 48 46 39 5 IO — AG18 GPIO32/CLKRUN*
TP_AZ_DOCK_EN — AG19 GPIO33/AZ_DOCK_EN*
RESERVED FOR MOBILE AZALIA DOCKING INTF
TP_AZ_DOCK_RST — U2 GPIO34/AZ_DOCK_RST*
PCIE_WAKE_L 44 37 5 IN — F20 WAKE*
INT_SERIRQ 55 48 46 5 IO — AH21 SERIRQ
PM_THRM_L 46 IN — AF20 THRM*
VR_PWRGD_CK410 26 IN — AD22 VRMPWRGD
TP_SB_GPIO6 IO — AG21 GPIO6
SB_RUNTIME_SCI_L — AC18 GPIO7
E21 GPIO8

SMB

CLKS
CLK14 — AC1
CLK48 — B2
SUSCLK — C20 (OUT)

PWR MNGT
SLP_S3* — B24
SLP_S4* — D23
SLP_S5* — F22
PWROK — AA4
RSMRST* — Y4
LAN_RST* — C19
PWRBTN* — C23
(INT 20K PU)
TP0/BATLOW* — C21
DPRSLPVR — AC22

SYS GPIO

GPIO

SATA GPIO
GPIO21/SATA0GP — AF19
GPIO19/SATA1GP — AH18
GPIO36/SATA2GP — AH19
GPIO37/SATA3GP — AE19

R2302 100 1/16W 402 2MF-LF 5%
R2303 100 1/16W 402 2MF-LF 5%
R2305 100 1/16W 402 2MF-LF 5%

SATA_C_DET_L 36 IN

CLK14 — 34 SB_CLK14P3M_TIMER IN
CLK48 — 34 SB_CLK48M_USBCTLR IN
SUSCLK — 8 SUS_CLK_SB OUT
SLP_S3* — 64 46 PM_SLP_S3_L OUT
SLP_S4* — 64 46 PM_SLP_S4_L OUT
SLP_S5* — 46 PM_SLP_S5_L OUT
PWROK — 26 PM_SB_PWROK IN
DPRSLPVR — 81 56 14 PM_DPRSLPVR OUT
NOTE: DPRSLPVR HAS INT 20K PD, ENABLED AT BOOT/RESET FOR STRAPPING FCN
PWRBTN* — 46 PM_PWRBTN_L IN
LAN_RST* — 46 PM_LAN_ENABLE IN
NOTE: SMC WILL DRIVE 0-1-0 TO KEEP LAN INT'F IN RESET STATE TO SAVE PWR
RSMRST* — Y4

GPIO9 — E20 — 47 46 SMS_INT_L IN
GPIO10 — A20 — 46 SMC_SB_NMI IN
DEF=GPI GPIO12 — F19 — 23 PATA_PWR_EN_L OUT
GPIO13 — E19
DEF=GPI GPIO14 — R4 — 36 IDE_RESET_L OUT
GPIO15 — E22 — SV_SET_UP 5 23 48
GPIO24 — R3 — CRB_SV_DET 23
GPIO25 — D20 — TP_SB_GPIO25_DO_NOT_USE
OD GPIO35 — AD21 — 33 SB_CLK100M_SATA_OE_L OUT
GPIO38 — AD20 — TP_SB_GPIO38 IO
DEF=GPI GPIO39 — AE20 — 23 SATA_C_PWR_EN_L OUT

=PP3V3_S5_SB_PM 11 26 62

R2319 10K 1/16W 402 2MF-LF 5%
R2343 8.2K 1/16W 402 2MF-LF 5%

PM_BATLOW_L 46 IN
PM_RSMRST_L 46 IN
SMC_WAKE_SCI_L 46 IN

R2399 100K 1/16W 402 2MF-LF 5%

NOSTUFF
R2300 0

SMC_RUNTIME_SCI_L 46 IN
SMC_EXTSMI_L 46 IN

NOTE FOR GPIO25:
- HAS INTERNAL 20K PU, ENABLED DURING RSMRST# AND DISABLED WITHIN 100MS AFTER RSMRST# DEASSERTS
- CAN NOT BE LOW FOR 35US AFTER RSMRST# ON BOOT (DMI AC COUPLING MODE STRAP)

=PP3V3_S5_SB 62 25 23

R2306 NOSTUFF 10K 1/16W 402 2MF-LF 5%
R2308 10K 1/16W 402 2MF-LF 5%

SV_SET_UP 5 23 48
CRB_SV_DET 23

NOTE:
SV_SET_UP IS LINDACARD DETECT
HI = PRESENT
LO = NOT PRESENT

LAYOUT NOTE:
PLACE R2306-14 WHERE PHYSICALLY ACCESSIBLE

R2307 10K 1/16W 402 2MF-LF 5%
R2309 NOSTUFF 0 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 62 25 23

R2313 10K 1/16W 402 2MF-LF 5%
R2310 10K 1/16W 402 2MF-LF 5%

FWH_MFG_MODE 23
BIOS_REC 23

R2314 NOSTUFF 0 1/16W 402 2MF-LF 5%
R2311 NOSTUFF 10K 1/16W 402 2MF-LF 5%

=PP3V3_S5_SB 23 25 62

R2390 10K 5% 1/16W 2MF-LF 402

PATA_PWR_EN_L 23

=PP3V3_S0_SB_GPIO 21 23 62

R2388 10K 5% 1/16W 2MF-LF 402

SATA_C_PWR_EN_L 23

SB: 3 OF 4

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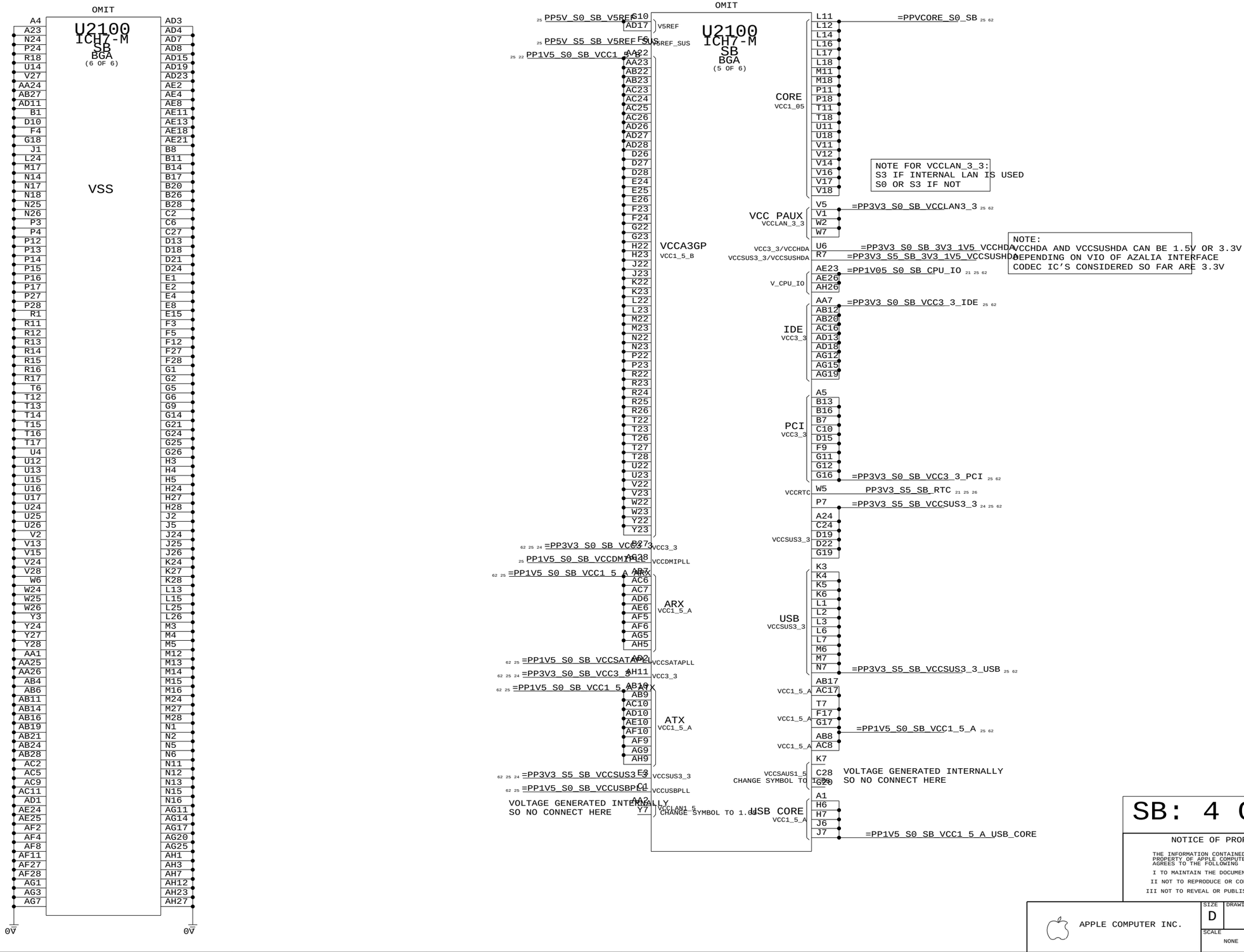
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	23	81



SB: 4 OF 4

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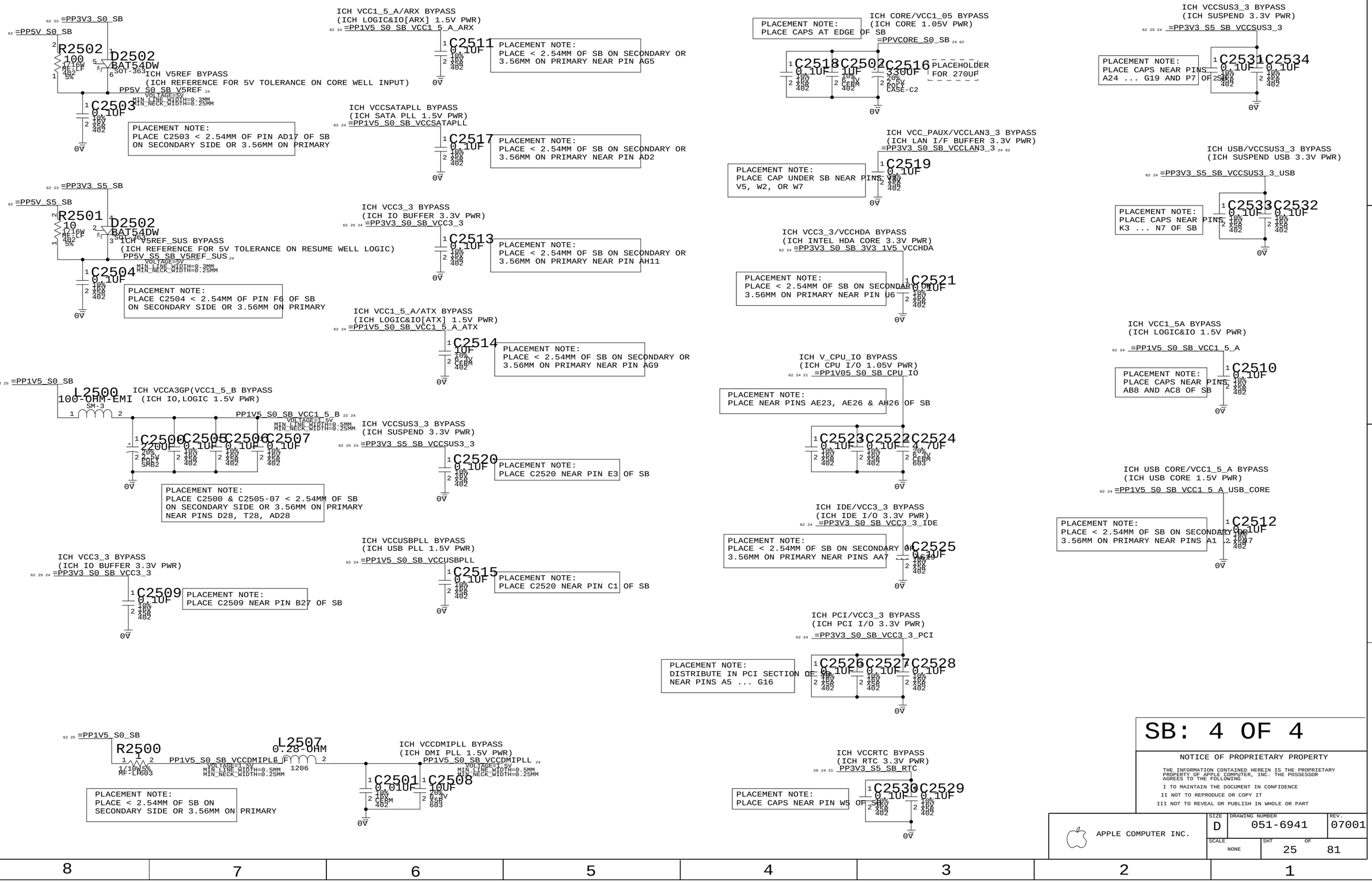
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	24	81


=PP3V3_S0_SB
=PP5V_S0_SB
R2502
100
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
ICH V5REF BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON CORE WELL INPUT)
PP5V_S0_SB_V5REF
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2503
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2503 < 2.54MM OF PIN AD17 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC1_5_A/ARX BYPASS
(ICH LOGIC&IO[ARX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ARX
C2511
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG5
ICH VCCSATAPLL BYPASS
(ICH SATA PLL 1.5V PWR)
=PP1V5_S0_SB_VCCSATAPLL
C2517
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AD2
=PP3V3_S5_SB
=PP5V_S5_SB
R2501
10
1/16W
MF-LF
402
5%
D2502
BAT54DW
SOT-363
ICH V5REF_SUS BYPASS
(ICH REFERENCE FOR 5V TOLERANCE ON RESUME WELL LOGIC)
PP5V_S5_SB_V5REF_SUS
VOLTAGE=5V
MIN_LINE_WIDTH=0.3MM
MIN_NECK_WIDTH=0.25MM
C2504
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2504 < 2.54MM OF PIN F6 OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2513
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AH11
ICH VCC1_5_A/ATX BYPASS
(ICH LOGIC&IO[ATX] 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_ATX
C2514
1UF
10%
6.3V
X5R
603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN AG9
=PP1V5_S0_SB
L2500
100-OHM-EMI
SM-3
ICH VCCA3GP(VCC1_5_B BYPASS
(ICH IO,LOGIC 1.5V PWR)
PP1V5_S0_SB_VCC1_5_B
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
C2500
270UF
20%
2.5V
POLY
SMB2
C2505
0.1UF
10%
16V
X5R
402
C2506
0.1UF
10%
16V
X5R
402
C2507
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2500 & C2505-07 < 2.54MM OF SB
ON SECONDARY SIDE OR 3.56MM ON PRIMARY
NEAR PINS D28, T28, AD28
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
C2520
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN E3 OF SB
ICH VCCUSBPLL BYPASS
(ICH USB PLL 1.5V PWR)
=PP1V5_S0_SB_VCCUSBPLL
C2515
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2520 NEAR PIN C1 OF SB
ICH VCC3_3 BYPASS
(ICH IO BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCC3_3
C2509
0.1UF
10%
16V
X5R
402
PLACEMENT NOTE:
PLACE C2509 NEAR PIN B27 OF SB
=PP1V5_S0_SB
R2500
1/10W5%
MF-LF003
L2507
0.28-OHM
1206
PP1V5_S0_SB_VCCDMIPLL
VOLTAGE=1.5V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.25MM
ICH VCCDMIPLL BYPASS
(ICH DMI PLL 1.5V PWR)
PP1V5_S0_SB_VCCDMIPLL
C2501
0.01UF
10%
16V
CERM
402
C2508
10UF
20%
6.3V
X5R
603
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON
SECONDARY SIDE OR 3.56MM ON PRIMARY
PLACEMENT NOTE:
PLACE CAPS AT EDGE OF SB
ICH CORE/VCC1_05 BYPASS
(ICH CORE 1.05V PWR)
=PPVCORE_S0_SB
C2518
0.1UF
10%
16V
X5R
402
C2502
1UF
10%
6.3V
CERM
402
C2516
330UF
20%
2.5V
POLY
CASE-C2
PLACEHOLDER
FOR 270UF
ICH VCC_PAUX/VCCLAN3_3 BYPASS
(ICH LAN I/F BUFFER 3.3V PWR)
=PP3V3_S0_SB_VCCLAN3_3
PLACEMENT NOTE:
PLACE CAP UNDER SB NEAR PINS V4,
V5, W2, OR W7
C2519
0.1UF
10%
16V
X5R
402
ICH VCC3_3/VCCHDA BYPASS
(ICH INTEL HDA CORE 3.3V PWR)
=PP3V3_S0_SB_3V3_1V5_VCCHDA
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PIN U6
C2521
0.1UF
10%
16V
X5R
402
ICH V_CPU_IO BYPASS
(ICH CPU I/O 1.05V PWR)
=PP1V05_S0_SB_CPU_IO
PLACEMENT NOTE:
PLACE NEAR PINS AE23, AE26 & AH26 OF SB
C2523
0.1UF
10%
16V
X5R
402
C2522
0.1UF
10%
16V
X5R
402
C2524
4.7UF
20%
6.3V
CERM
603
ICH IDE/VCC3_3 BYPASS
(ICH IDE I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_IDE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS AA7
C2525
0.1UF
10%
16V
X5R
402
ICH PCI/VCC3_3 BYPASS
(ICH PCI I/O 3.3V PWR)
=PP3V3_S0_SB_VCC3_3_PCI
PLACEMENT NOTE:
DISTRIBUTE IN PCI SECTION OF SB
NEAR PINS A5 ... G16
C2526
0.1UF
10%
16V
X5R
402
C2527
0.1UF
10%
16V
X5R
402
C2528
0.1UF
10%
16V
X5R
402
ICH VCCRTC BYPASS
(ICH RTC 3.3V PWR)
PP3V3_S5_SB_RTC
PLACEMENT NOTE:
PLACE CAPS NEAR PIN W5 OF SB
C2530
0.1UF
10%
16V
X5R
402
C2529
0.1UF
10%
16V
X5R
402
ICH VCCSUS3_3 BYPASS
(ICH SUSPEND 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
A24 ... G19 AND P7 OF SB
C2531
0.1UF
10%
16V
X5R
402
C2534
0.1UF
10%
16V
X5R
402
ICH USB/VCCSUS3_3 BYPASS
(ICH SUSPEND USB 3.3V PWR)
=PP3V3_S5_SB_VCCSUS3_3_USB
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
K3 ... N7 OF SB
C2533
0.1UF
10%
16V
X5R
402
C2532
0.1UF
10%
16V
X5R
402
ICH VCC1_5A BYPASS
(ICH LOGIC&IO 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A
PLACEMENT NOTE:
PLACE CAPS NEAR PINS
AB8 AND AC8 OF SB
C2510
0.1UF
10%
16V
X5R
402
ICH USB CORE/VCC1_5_A BYPASS
(ICH USB CORE 1.5V PWR)
=PP1V5_S0_SB_VCC1_5_A_USB_CORE
PLACEMENT NOTE:
PLACE < 2.54MM OF SB ON SECONDARY OR
3.56MM ON PRIMARY NEAR PINS A1 ... A7
C2512
0.1UF
10%
16V
X5R
402
SB: 4 OF 4
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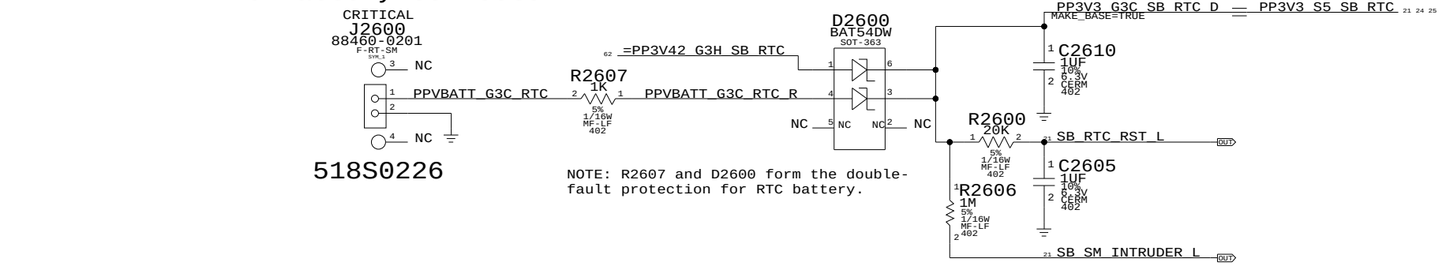
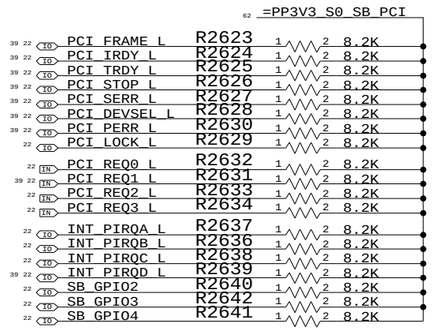
III NOT TO REVEAL OR PUBLISH IN WHOLE OR PART
APPLE COMPUTER INC.
SIZE
D
DRAWING NUMBER
051-6941
REV.
07001
SCALE
NONE
SHT
25
OF
81

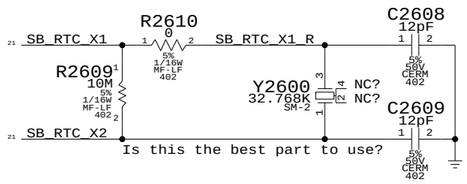
RTC Battery Connector



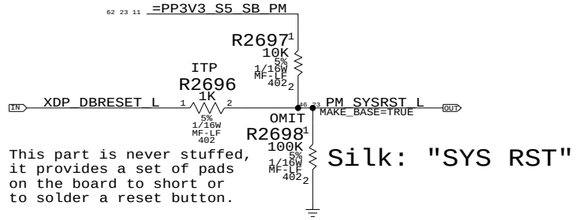
NOTE: R2607 and D2600 form the double-fault protection for RTC battery.



SB RTC Crystal Circuit



Is this the best part to use?

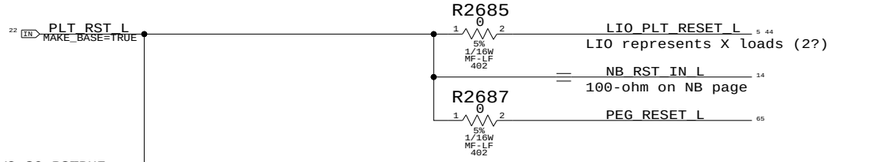


This part is never stuffed, it provides a set of pads on the board to short or to solder a reset button.

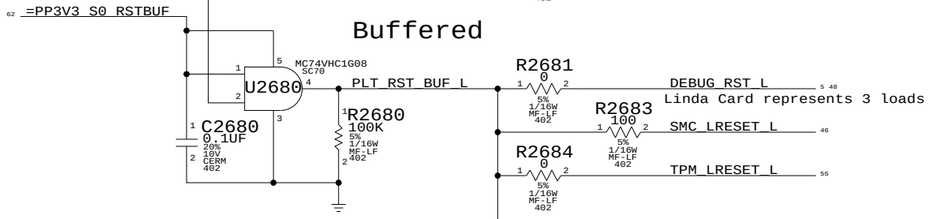
Silk: "SYS RST"

Platform Reset Connections

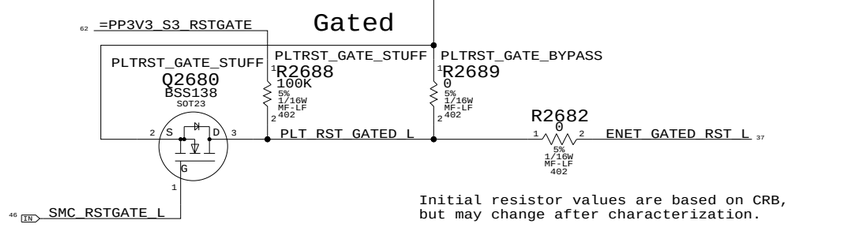
Unbuffered



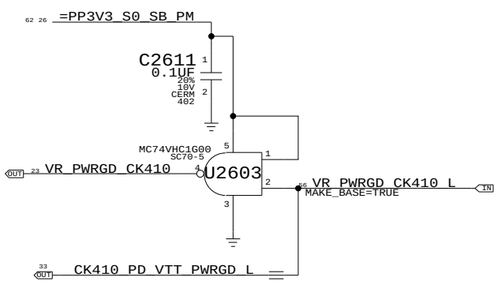
Buffered



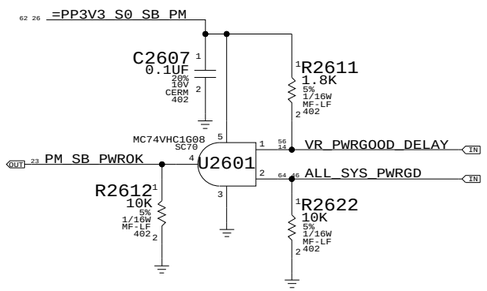
Gated



Initial resistor values are based on CRB, but may change after characterization.



1G00 used as small & cheap inverter



SB Misc

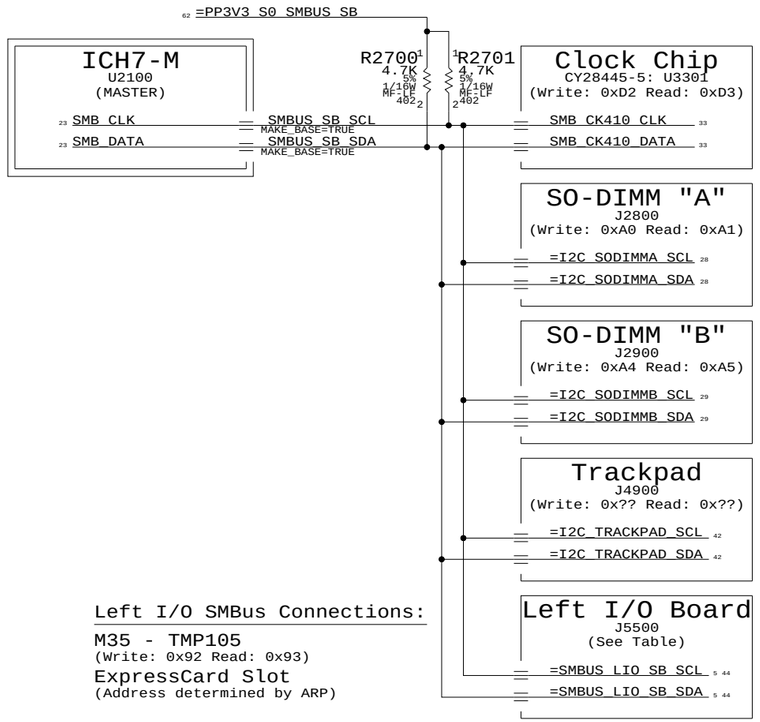
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	26	81

ICH7-M SMBus Connections

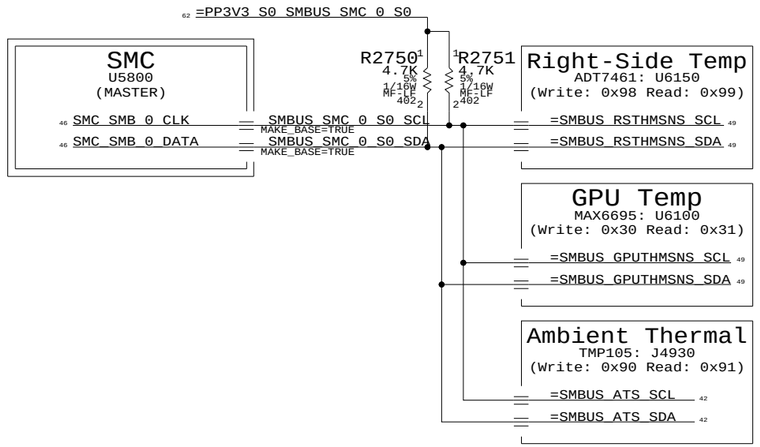


Left I/O SMBus Connections:

M35 - TMP105
(Write: 0x92 Read: 0x93)

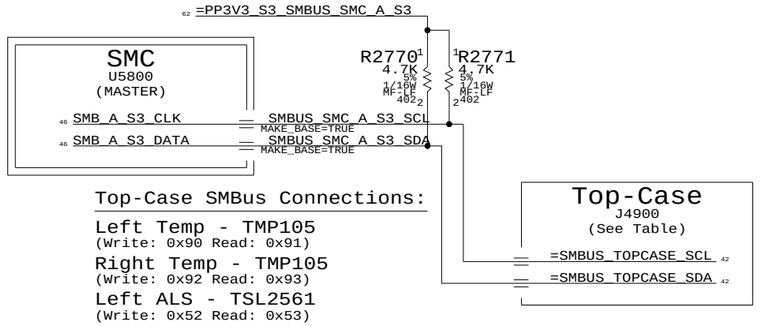
ExpressCard Slot
(Address determined by ARP)

SMC "0" SMBus Connections



SMC "A" SMBus Connections

NOTE: SMC RMT bus remains powered and may be active in S3 state



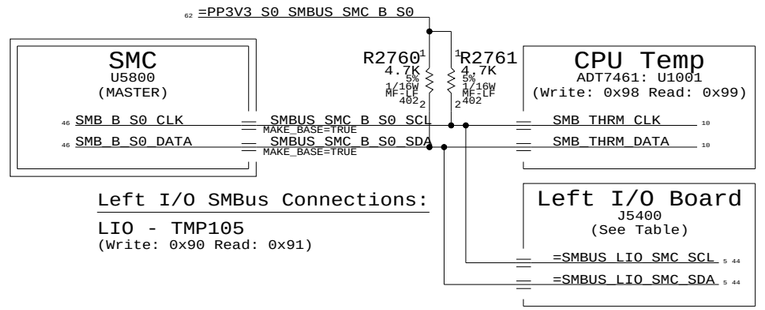
Top-Case SMBus Connections:

Left Temp - TMP105
(Write: 0x90 Read: 0x91)

Right Temp - TMP105
(Write: 0x92 Read: 0x93)

Left ALS - TSL2561
(Write: 0x52 Read: 0x53)

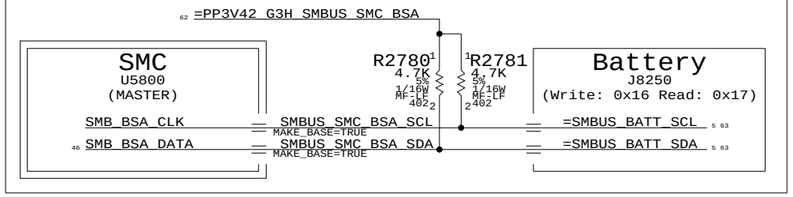
SMC "B" SMBus Connections



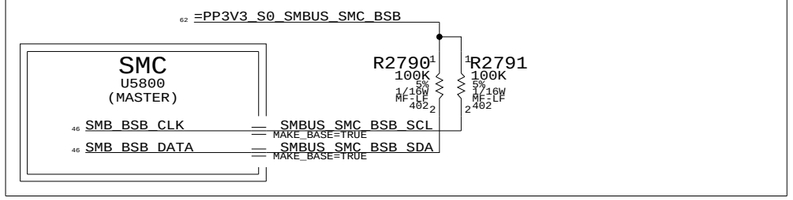
Left I/O SMBus Connections:

LIO - TMP105
(Write: 0x90 Read: 0x91)

SMC "Battery A" SMBus Connections



SMC "Battery B" SMBus Connections



M1 SMBus Connections

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	27	81

Page Notes

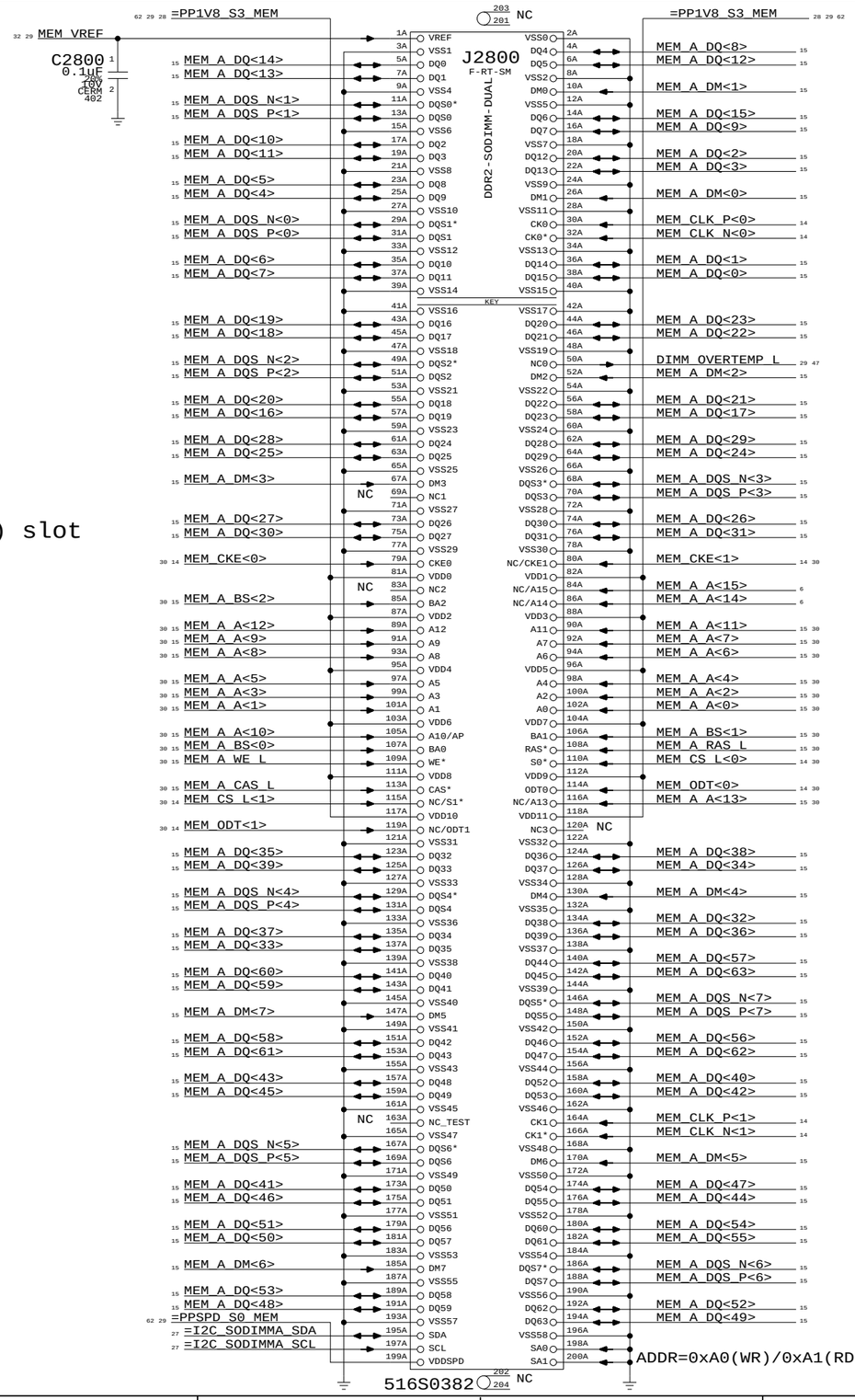
Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Upper" (surface-mount) slot



DDR2 Bypass Caps

(For return current)

DDR2 SO-DIMM Connector A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	28	81

Page Notes

Power aliases required by this page:
- =PP1V8_S3_MEM
- =PPSPD_S0_MEM (2.5V - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)

NOTE: This page does not supply VREF. The reference voltage must be provided by another page.

"Lower" (thru-hole) slot

62 29 28 =PP1V8_S3_MEM

32 28 MEM_VREF

C2900 0.1uF 20% 10V CERM 402

J2900 F-RT-TH DDR2-SODIMM-DUAL

		1B	VREF	VSS0	2B		
		3B	VSS1	DQ4	4B	MEM_B_DQ<9>	15
15	MEM_B_DQ<15>	5B	DQ0	DQ5	6B	MEM_B_DQ<11>	15
15	MEM_B_DQ<14>	7B	DQ1	VSS2	8B		
		9B	VSS4	DM0	10B	MEM_B_DM<1>	15
15	MEM_B_DQS_N<1>	11B	DQS0*	VSS5	12B		
15	MEM_B_DQS_P<1>	13B	DQS0	DQ6	14B	MEM_B_DQ<12>	15
		15B	VSS6	DQ7	16B	MEM_B_DQ<8>	15
15	MEM_B_DQ<10>	17B	DQ2	VSS7	18B		
15	MEM_B_DQ<13>	19B	DQ3	DQ12	20B	MEM_B_DQ<3>	15
		21B	VSS8	DQ13	22B	MEM_B_DQ<6>	15
15	MEM_B_DQ<7>	23B	DQ8	VSS9	24B		
15	MEM_B_DQ<2>	25B	DQ9	DM1	26B	MEM_B_DM<0>	15
		27B	VSS10	VSS11	28B		
15	MEM_B_DQS_N<0>	29B	DQS1*	CK0	30B	MEM_CLK_P<3>	14
15	MEM_B_DQS_P<0>	31B	DQS1	CK0*	32B	MEM_CLK_N<3>	14
		33B	VSS12	VSS13	34B		
15	MEM_B_DQ<1>	35B	DQ10	DQ14	36B	MEM_B_DQ<0>	15
15	MEM_B_DQ<4>	37B	DQ11	DQ15	38B	MEM_B_DQ<5>	15
		39B	VSS14	VSS15	40B		
			KEY				
		41B	VSS16	VSS17	42B		
15	MEM_B_DQ<21>	43B	DQ16	DQ20	44B	MEM_B_DQ<22>	15
15	MEM_B_DQ<19>	45B	DQ17	DQ21	46B	MEM_B_DQ<18>	15
		47B	VSS18	VSS19	48B		
15	MEM_B_DQS_N<2>	49B	DQS2*	NC0	50B	DIMM_OVERTEMP_L	28 47
15	MEM_B_DQS_P<2>	51B	DQS2	DM2	52B	MEM_B_DM<2>	15
		53B	VSS21	VSS22	54B		
15	MEM_B_DQ<20>	55B	DQ18	DQ22	56B	MEM_B_DQ<17>	15
15	MEM_B_DQ<23>	57B	DQ19	DQ23	58B	MEM_B_DQ<16>	15
		59B	VSS23	VSS24	60B		
15	MEM_B_DQ<29>	61B	DQ24	DQ28	62B	MEM_B_DQ<26>	15
15	MEM_B_DQ<24>	63B	DQ25	DQ29	64B	MEM_B_DQ<28>	15
		65B	VSS25	VSS26	66B		
15	MEM_B_DM<3>	67B	DM3	DQS3*	68B	MEM_B_DQS_N<3>	15
	NC	69B	NC1	DQS3	70B	MEM_B_DQS_P<3>	15
		71B	VSS27	VSS28	72B		
15	MEM_B_DQ<27>	73B	DQ26	DQ30	74B	MEM_B_DQ<31>	15
15	MEM_B_DQ<25>	75B	DQ27	DQ31	76B	MEM_B_DQ<30>	15
		77B	VSS29	VSS30	78B		
30 14	MEM_CKE<2>	79B	CKE0	NC/CKE1	80B	MEM_CKE<3>	14 30
		81B	VDD0	VDD1	82B		
	NC	83B	NC2	NC/A15	84B	MEM_B_A<15>	6
30 15	MEM_B_BS<2>	85B	BA2	NC/A14	86B	MEM_B_A<14>	6
		87B	VDD2	VDD3	88B		
30 15	MEM_B_A<12>	89B	A12	A11	90B	MEM_B_A<11>	15 30
30 15	MEM_B_A<9>	91B	A9	A7	92B	MEM_B_A<7>	15 30
30 15	MEM_B_A<8>	93B	A8	A6	94B	MEM_B_A<6>	15 30
		95B	VDD4	VDD5	96B		
30 15	MEM_B_A<5>	97B	A5	A4	98B	MEM_B_A<4>	15 30
30 15	MEM_B_A<3>	99B	A3	A2	100B	MEM_B_A<2>	15 30
30 15	MEM_B_A<1>	101B	A1	A0	102B	MEM_B_A<0>	15 30
		103B	VDD6	VDD7	104B		
30 15	MEM_B_A<10>	105B	A10/AP	BA1	106B	MEM_B_BS<1>	15 30
30 15	MEM_B_BS<0>	107B	BA0	RAS*	108B	MEM_B_RAS_L	15 30
30 15	MEM_B_WE_L	109B	WE*	S0*	110B	MEM_CS_L<2>	14 30
		111B	VDD8	VDD9	112B		
30 15	MEM_B_CAS_L	113B	CAS*	ODT0	114B	MEM_ODT<2>	14 30
30 14	MEM_CS_L<3>	115B	NC/S1*	NC/A13	116B	MEM_B_A<13>	15 30
		117B	VDD10	VDD11	118B		
30 14	MEM_ODT<3>	119B	NC/ODT1	NC3	120B	NC	
		121B	VSS31	VSS32	122B		
15	MEM_B_DQ<36>	123B	DQ32	DQ36	124B	MEM_B_DQ<32>	15
15	MEM_B_DQ<33>	125B	DQ33	DQ37	126B	MEM_B_DQ<37>	15
		127B	VSS33	VSS34	128B		
15	MEM_B_DQS_N<4>	129B	DQS4*	DM4	130B	MEM_B_DM<4>	15
15	MEM_B_DQS_P<4>	131B	DQS4	VSS35	132B		
		133B	VSS36	DQ38	134B	MEM_B_DQ<38>	15
15	MEM_B_DQ<34>	135B	DQ34	DQ39	136B	MEM_B_DQ<39>	15
15	MEM_B_DQ<35>	137B	DQ35	VSS37	138B		
		139B	VSS38	DQ44	140B	MEM_B_DQ<44>	15
15	MEM_B_DQ<40>	141B	DQ40	DQ45	142B	MEM_B_DQ<45>	15
15	MEM_B_DQ<41>	143B	DQ41	VSS39	144B		
		145B	VSS40	DQS5*	146B	MEM_B_DQS_N<5>	15
15	MEM_B_DM<5>	147B	DM5	DQS5	148B	MEM_B_DQS_P<5>	15
		149B	VSS41	VSS42	150B		
15	MEM_B_DQ<42>	151B	DQ42	DQ46	152B	MEM_B_DQ<46>	15
15	MEM_B_DQ<43>	153B	DQ43	DQ47	154B	MEM_B_DQ<47>	15
		155B	VSS43	VSS44	156B		
15	MEM_B_DQ<62>	157B	DQ48	DQ52	158B	MEM_B_DQ<58>	15
15	MEM_B_DQ<59>	159B	DQ49	DQ53	160B	MEM_B_DQ<63>	15
		161B	VSS45	VSS46	162B		
	NC	163B	NC_TEST	CK1	164B	MEM_CLK_P<2>	14
		165B	VSS47	CK1*	166B	MEM_CLK_N<2>	14
15	MEM_B_DQS_N<7>	167B	DQS6*	VSS48	168B		
15	MEM_B_DQS_P<7>	169B	DQS6	DM6	170B	MEM_B_DM<7>	15
		171B	VSS49	VSS50	172B		
15	MEM_B_DQ<60>	173B	DQ50	DQ54	174B	MEM_B_DQ<56>	15
15	MEM_B_DQ<61>	175B	DQ51	DQ55	176B	MEM_B_DQ<57>	15
		177B	VSS51	VSS52	178B		
15	MEM_B_DQ<54>	179B	DQ56	DQ60	180B	MEM_B_DQ<55>	15
15	MEM_B_DQ<51>	181B	DQ57	DQ61	182B	MEM_B_DQ<50>	15
		183B	VSS53	VSS54	184B		
15	MEM_B_DM<6>	185B	DM7	DQS7*	186B	MEM_B_DQS_N<6>	15
		187B	VSS55	DQS7	188B	MEM_B_DQS_P<6>	15
15	MEM_B_DQ<52>	189B	DQ58	VSS56	190B		
15	MEM_B_DQ<49>	191B	DQ59	DQ62	192B	MEM_B_DQ<53>	15
62 29 28	=PPSPD_S0_MEM	193B	VSS57	DQ63	194B	MEM_B_DQ<48>	15
27	=I2C_SODIMMB_SDA	195B	SDA	VSS58	196B		
27	=I2C_SODIMMB_SCL	197B	SCL	SA0	198B		
		199B	VDDSPD	SA1	200B		

516-0130

20 NC — 202 NC

=PP1V8_S3_MEM 28 29 62

=PPSPD_S0_MEM 28 29 62

R2900 10K 5% 1/10W MF-LF 402

Resistor prevents pwr-gnd short

SODIMM_A_SA1

ADDR=0xA4(WR)/0xA5(RD)

DDR2 Bypass Caps

(For return current)

62 29 28 =PP1V8_S3_MEM

C2908 10UF 20% 6.3V X5R 603	C2909 10UF 20% 6.3V X5R 603		
C2910 0.1uF 20% 10V CERM 402	C2911 0.1uF 20% 10V CERM 402	C2912 0.1uF 20% 10V CERM 402	C2913 0.1uF 20% 10V CERM 402
C2914 0.1uF 20% 10V CERM 402	C2915 0.1uF 20% 10V CERM 402	C2916 0.1uF 20% 10V CERM 402	C2917 0.1uF 20% 10V CERM 402
C2918 0.1uF 20% 10V CERM 402	C2919 0.1uF 20% 10V CERM 402	C2920 0.1uF 20% 10V CERM 402	C2921 0.1uF 20% 10V CERM 402

DDR2 SO-DIMM Connector B

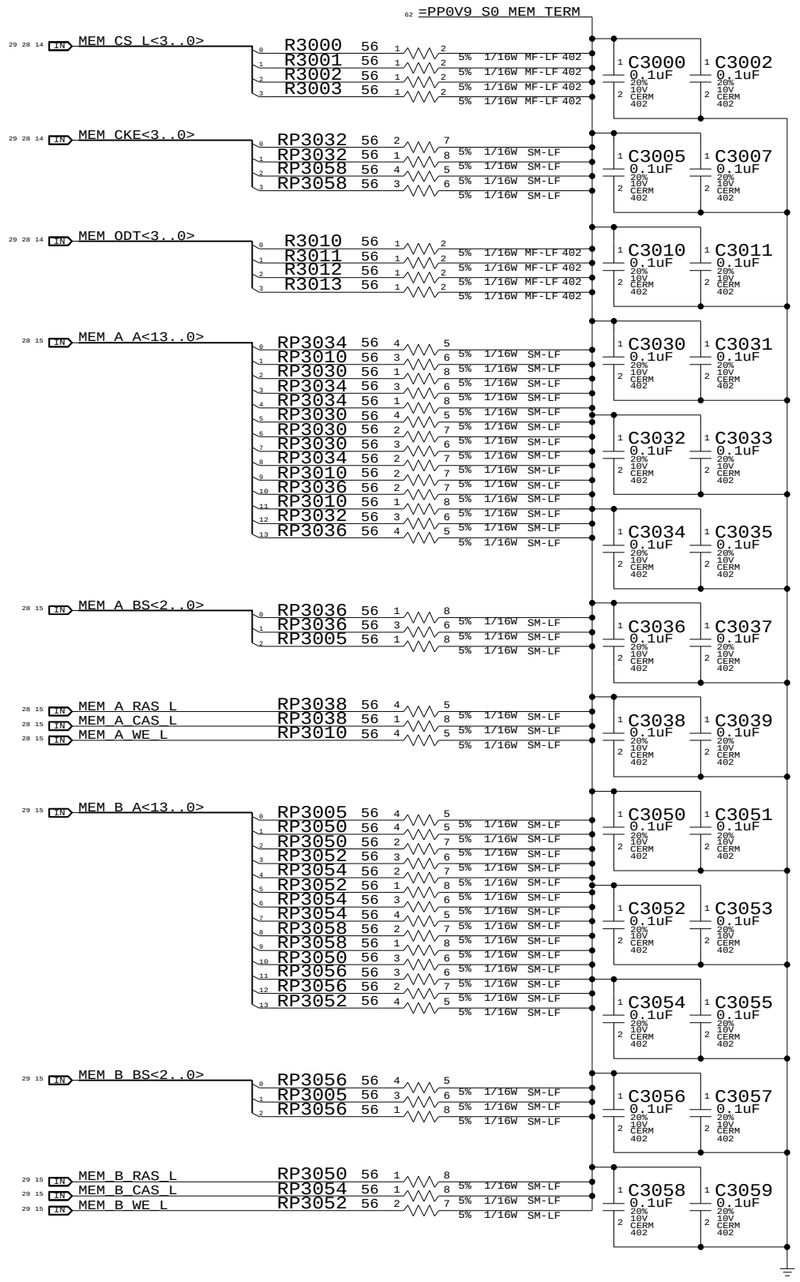
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 29	OF 81

One cap for each side of every RPAK, one cap for every two discrete resistors

Ensure CS_L and ODT resistors are close to SO-DIMM connector



Memory Active Termination

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	30	81

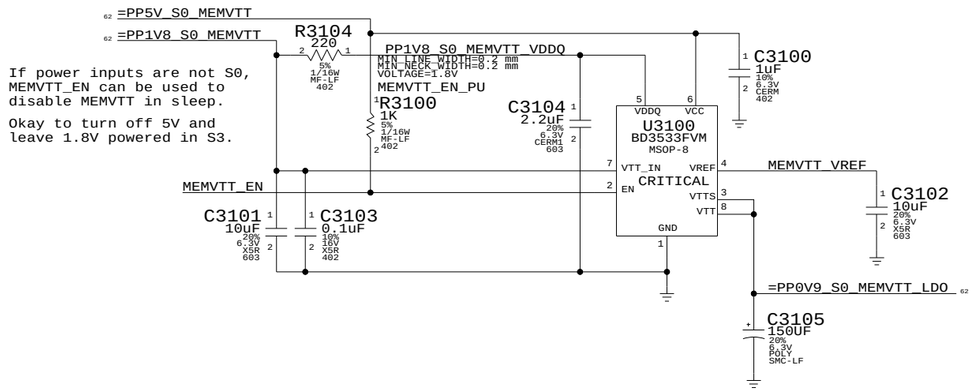
Page Notes

Power aliases required by this page:
- =PP5V_S0_MEMVTT
- =PP1V8_S0_MEMVTT
- =PP0V9_S0_MEMVTT_LDO

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

DDR2 Vtt Regulator



If power inputs are not S0, MEMVTT_EN can be used to disable MEMVTT in sleep.

Okay to turn off 5V and leave 1.8V powered in S3.

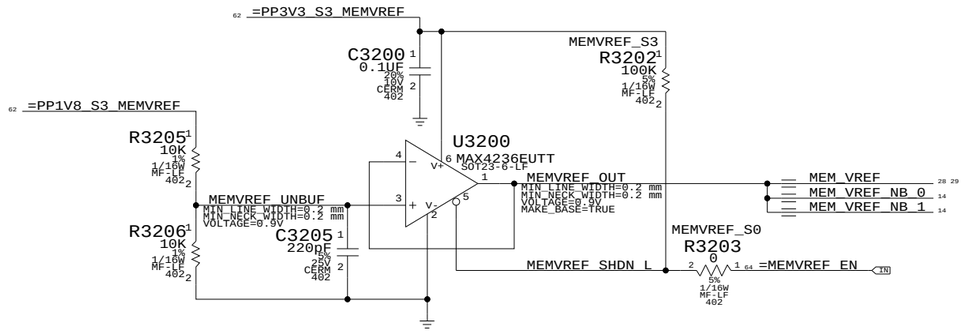
Memory Vtt Supply

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	31	81



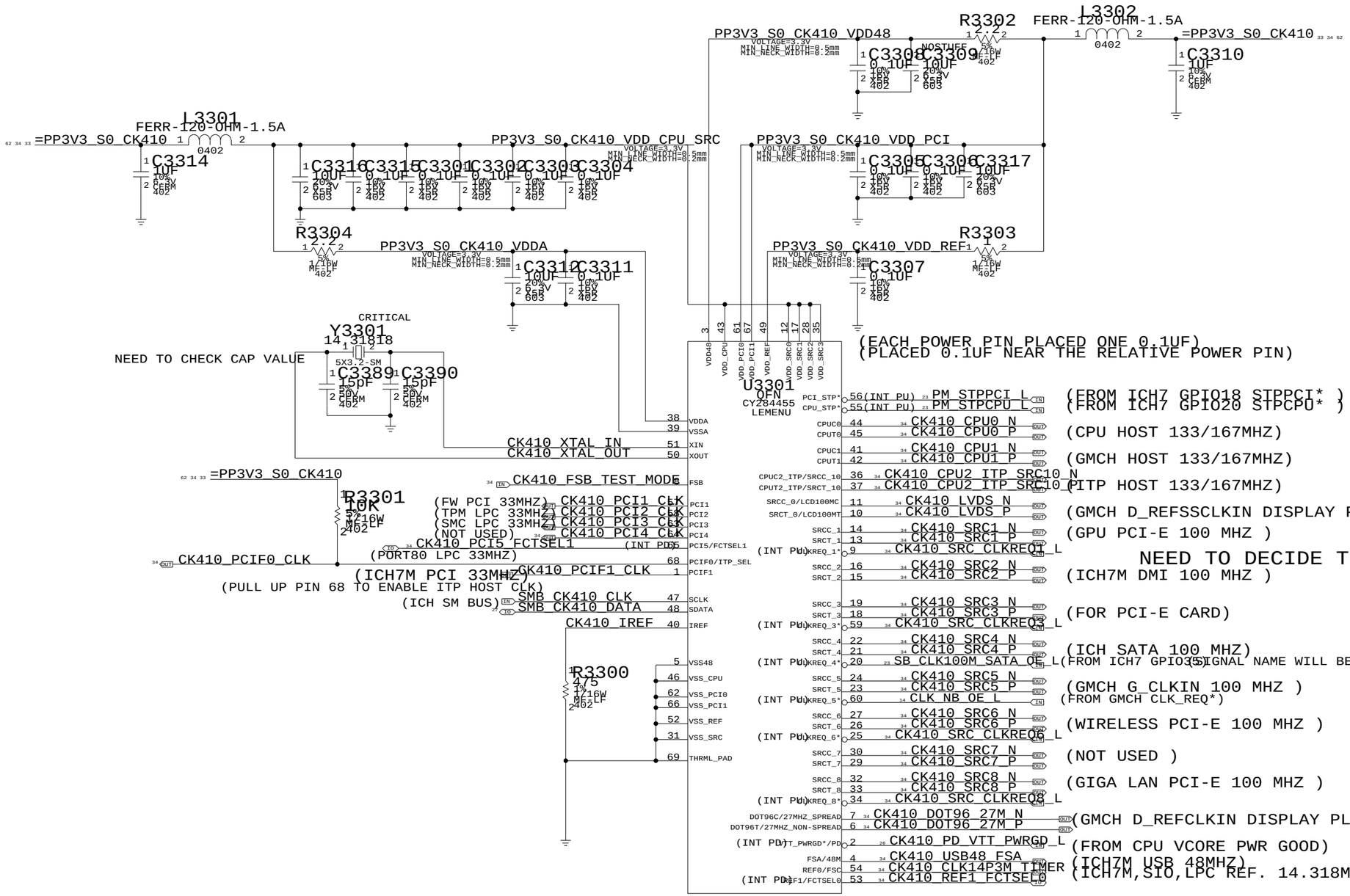
DDR2 VRef

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	32	81



FCTSEL1	FCTSEL0	PIN 6	PIN 7	PIN 10	PIN 11	
0	0	DOT96T	DOT96C	100MT_SST	100MC_SST	* FOR INT. GRAPHIC SYSTEM
0	1	DOT96T	DOT96C	SRCT0	SRCC0	
1	0	27M_NON-SPREAD	27M_SPREAD	SRCT0	SRCC0	* FOR EXT. GRAPHIC SYSTEM
1	1	OFF	LOW	BD	SRCT0	SRCC0

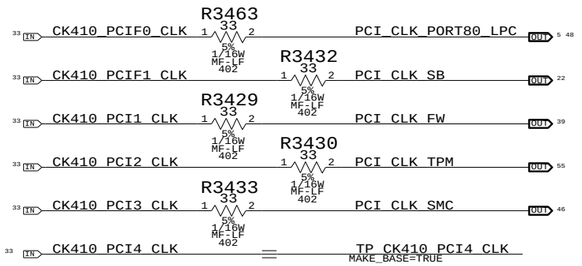
CLOCKS

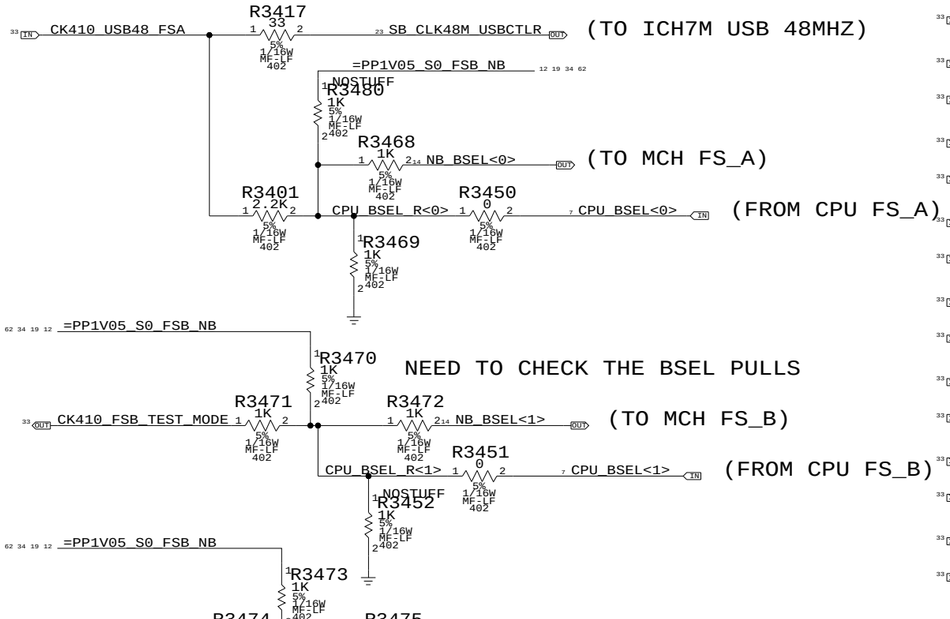
SYNC_MASTER=MBZ SYNC_DATE=09/08/2005

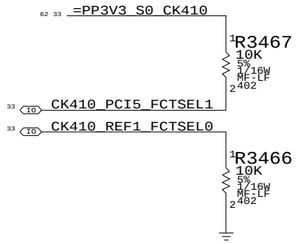
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	33	81



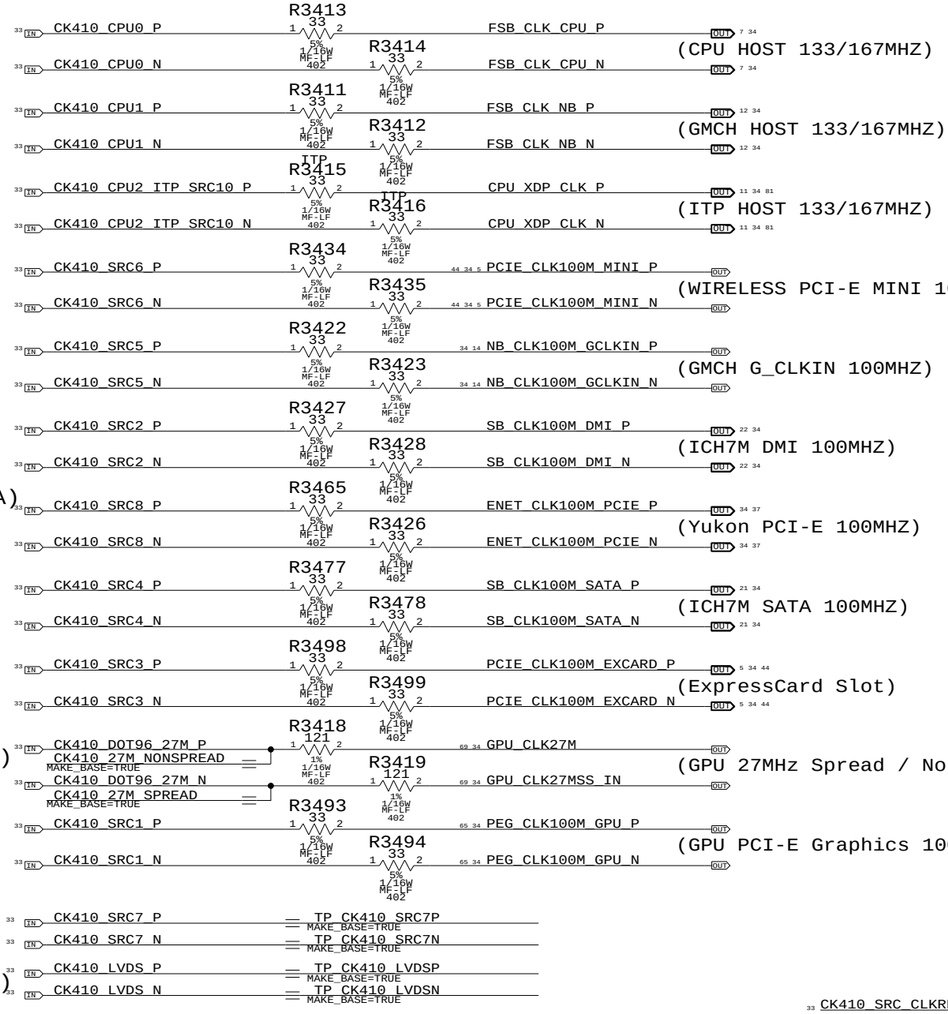


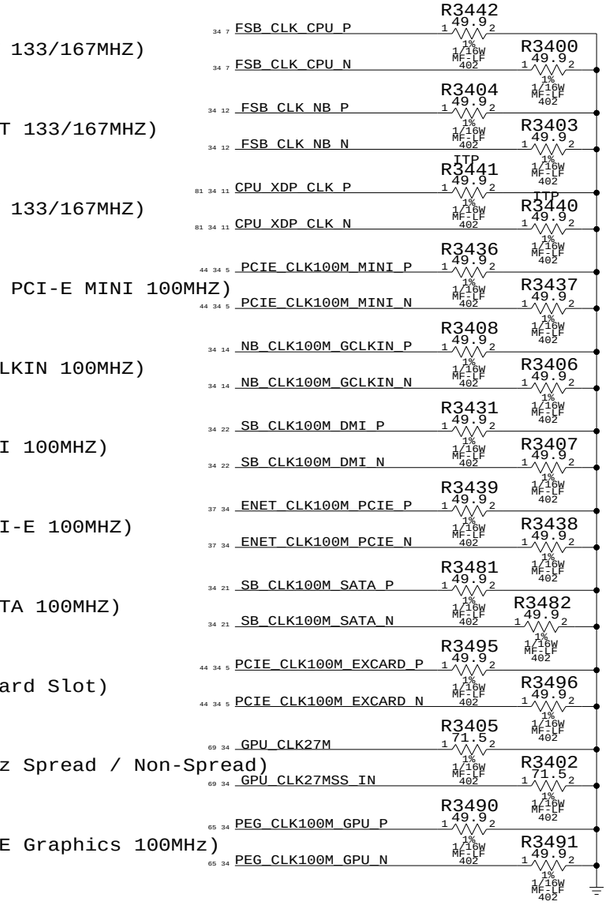


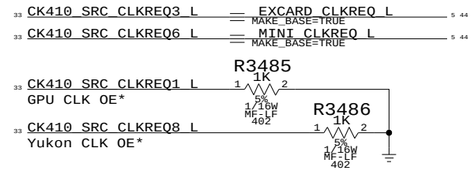
NOSTUFF R3450,R3451,R3453 FOR MANUAL CPU FREQUENCY

	FS_C	FS_B	FS_A	CPU
	0	0	0	266M
#	0	0	1	133M
#	0	1	0	166M
	0	1	1	200M
	1	0	0	100M
	1	0	1	333M
	1	1	0	400M
	1	1	1	RESERVED

NAPA PLATFORM ONLY SUPPORT 133M/166M CPU SPEED







Clock Termination

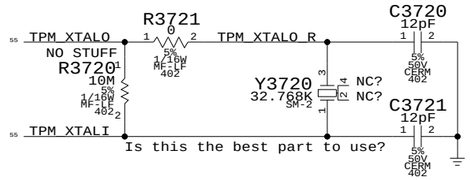
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

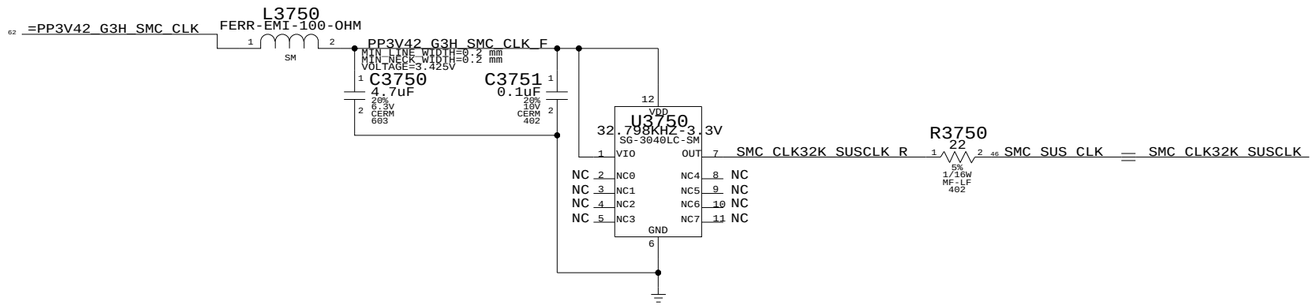
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	34	81

TPM Crystal Circuit



SMC G3Hot Oscillator



Mobile Clocking

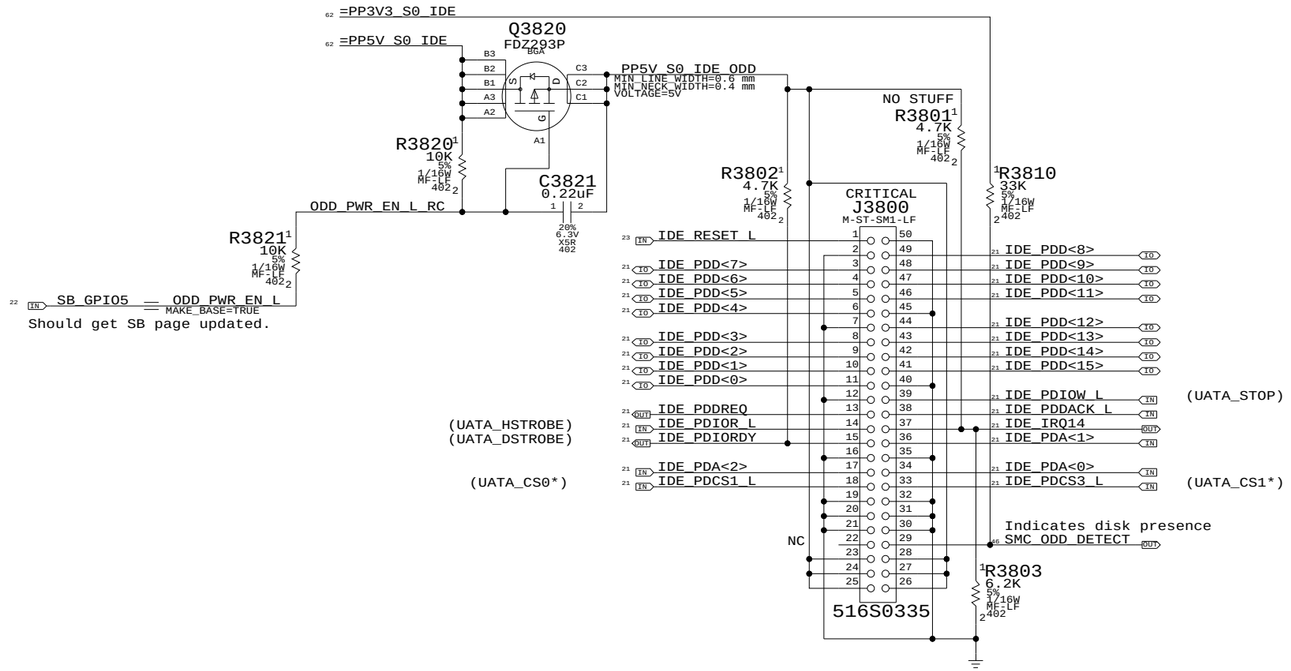
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

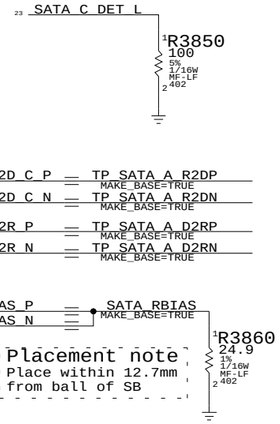
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	35	81

IDE (ODD) Connector





PATA Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	36	81

PLACE C4100-C4106 NEAR PINS AVDLL0-AVDLL6.
SCHEME MATCHES DOC MVL100258-01

MIN_LINE_WIDTH=0.4MM
MIN_NECK_WIDTH=0.25MM
VOLTAGE=2.5V

PP2V5_S3_ENET_AVDD

C4100 1UF 10% 6.3V CERM 402
C4101 0.1UF 10% 16V X5R 402
C4102 0.1UF 10% 16V X5R 402
C4103 0.1UF 10% 16V X5R 402
C4104 0.1UF 10% 16V X5R 402
C4105 0.001UF 10% 50V CERM 402
C4106 0.001UF 10% 50V CERM 402
C4107 0.1UF 10% 16V X5R 402

L4100 FERR-120-OHM-1.5A 0402 =PP2V5_S3_ENET 38 62

PLACE C4107 NEAR U4101 AVDD

62 37 =PP3V3_S3_ENET
=PP1V2_S3_ENET 37 62
=PP3V3_S3_ENET 37 62

R4101 4.7K 5% 1/16W MF-LF 402

PLACE C4110 AND C4111 WITHIN
12 MIL OF U4101 PIN 49 AND 50

C4110 0.1UF 10% 16V X5R 402
C4111 0.1UF 10% 16V X5R 402
C4112 0.1UF 10% 16V X5R 402
C4113 0.1UF 10% 16V X5R 402

PLACE C4113 AND C4112 WITHIN
12 MIL OF U2100 E27 AND E28

PCIE_A_D2R_C_P 1 2 22 PCIE_A_D2R_P OUT
PCIE_A_D2R_C_N 1 2 22 PCIE_A_D2R_N OUT
PCIE_A_R2D_P 1 2 22 PCIE_A_R2D_C_P IN
PCIE_A_R2D_N 1 2 22 PCIE_A_R2D_C_N IN

LEMENU
U4101
88E8053
QFN

VDD7 58
VDD6 48
VDD5 44
VDD4 39
VDD3 33
VDD2 13
VDD1 7
VDD0 2
VDDO_TTL4 61
VDDO_TTL3 45
VDDO_TTL2 40
VDDO_TTL1 8
VDDO_TTL0 1
AVDD 23
AVDDL6 57
AVDDL5 52
AVDDL4 51
AVDDL3 32
AVDDL2 28
AVDDL1 22
AVDDL0 19
VDD25 64

ENET_LOM_DIS_L 10 LOM_DISABLE*
12 VAUX_AVLBL
47 VMAIN_AVLBL
NC 11 SWITCH_VCC
NC 9 SWITCH_VAUX
NC 24 HSDACP
NC 25 HSDACN

ANALOG

OPTIONAL EXTERNAL LDO

OUT 6 ENET_CTRL25 4 CTRL25
OUT 6 ENET_CTRL12 3 CTRL12
ENET_RSET 16 RSET

R4102 4.87K 1% 1/16W MF-LF 402

NO PULL-UP NEEDED

NC 59 LED_ACT*
NC 60 LED_LINK10/100*
NC 62 LED_LINK1000*
NC 63 LINK*

LED

29 TSTPT
46 TESTMODE

TEST

PCI EXPRESS

TX_P 49
TX_N 50
RX_P 54
RX_N 53
REFCLKP 55 34 ENET_CLK100M_PCIE_P IN
REFCLKN 56 34 ENET_CLK100M_PCIE_N IN
WAKE* 6 44 23 5 PCIE_WAKE_L OUT
PERST* 5 26 ENET_GATED_RST_L IN

MEDIA

MDIP0 17 38 ENET_MDI_P<0> IO
MDIN0 18 38 ENET_MDI_N<0> IO
MDIP1 20 38 ENET_MDI_P<1> IO
MDIN1 21 38 ENET_MDI_N<1> IO
MDIP2 26 38 ENET_MDI_P<2> IO
MDIN2 27 38 ENET_MDI_N<2> IO
MDIP3 30 38 ENET_MDI_P<3> IO
MDIN3 31 38 ENET_MDI_N<3> IO

TWSI

VPD_CLK 38 ENET_VPD_CLK 37
VPD_DATA 41 ENET_VPD_DATA 37

TEST

PU_VDDO_TTL0 42 ENET_PU_VDD_TTL0 37
PU_VDDO_TTL1 43 ENET_PU_VDD_TTL1 37

ASF IS UNAVAILABLE ON 8053

SPI

SPI_DI 35 NC
SPI_DO 34 NC
SPI_CLK 37 NC
SPI_CS 36 NC

INTERNAL PULL-UP

MAIN CLK

XTALI 15 ENET_XTALI
XTALO 14 ENET_XTALO

CRITICAL

Y4101 25.0000M SM-3
C4150 22pF 5% 50V CERM 402
C4151 22pF 5% 50V CERM 402

1. KEEP ENET_XTALI AND ENET_XTALO TRACE LENGTH <12MIL
2. DO NOT ROUTE UNDER CRYSTAL

THRML_PAD 67

R4106 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4105 49.9 1% 1/16W MF-LF 402 ENET_MDI0
R4104 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4103 49.9 1% 1/16W MF-LF 402 ENET_MDI1
R4120 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4119 49.9 1% 1/16W MF-LF 402 ENET_MDI2
R4118 49.9 1% 1/16W MF-LF 402 ENET_MDI3
R4117 49.9 1% 1/16W MF-LF 402 ENET_MDI3

C4116 0.001UF 10% 50V CERM 402
C4115 0.001UF 10% 50V CERM 402
C4117 0.001UF 10% 50V CERM 402
C4118 0.001UF 10% 50V CERM 402

PLACE RESISTORS CLOSE TO U4101

=PP3V3_S3_ENET 37 62
R4130 4.7K 5% 1/16W MF-LF 402
R4131 4.7K 5% 1/16W MF-LF 402
37 ENET_PU_VDD_TTL0
37 ENET_PU_VDD_TTL1

62 37 =PP3V3_S3_ENET
PLACE C4140 NEAR U4102 VCC
C4140 0.1UF 10% 16V X5R 402

R4122 4.7K 5% 1/16W MF-LF 402
R4123 4.7K 5% 1/16W MF-LF 402

LEMENU
U4102 M24C08 SO8
E2 3
NC1 2
NC0 1
WC* 7
VCC 8
SDA 5
SCL 6
VSS 4

ENET_VPD_DATA 37
ENET_VPD_CLK 37

PLACE C4127-C4134 NEAR PINS VDD0-VDD7 ON U4101
SCHEME MATCHES DOC MVL100258-01

62 37 =PP1V2_S3_ENET

C4126 0.1UF 10% 16V X5R 402
C4127 0.1UF 10% 16V X5R 402
C4128 0.1UF 10% 16V X5R 402
C4129 0.1UF 10% 16V X5R 402
C4130 0.1UF 10% 16V X5R 402
C4131 0.001UF 10% 50V CERM 402
C4132 0.001UF 10% 50V CERM 402
C4133 0.001UF 10% 50V CERM 402
C4134 0.001UF 10% 50V CERM 402

PLACE C4135-C4139 NEAR VDDO_TTL0-VDD_TTL4 ON U4101
SCHEME MATCHES DOC MVL100258-01

62 37 =PP3V3_S3_ENET

C4135 0.1UF 10% 16V X5R 402
C4136 0.1UF 10% 16V X5R 402
C4137 0.1UF 10% 16V X5R 402
C4138 0.001UF 10% 50V CERM 402
C4139 0.001UF 10% 50V CERM 402

ETHERNET CONTROLLER

SYNC_MASTER=M42 SYNC_DATE=09/08/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	37	81

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY ETHERNET PHY	ENETCONN	ENET_100D	ENETCONN_P<0>
	ENETCONN	ENET_100D	ENETCONN_N<0>
	ENETCONN	ENET_100D	ENETCONN_P<1>
	ENETCONN	ENET_100D	ENETCONN_N<1>
	ENETCONN	ENET_100D	ENETCONN_P<2>
	ENETCONN	ENET_100D	ENETCONN_N<2>
	ENETCONN	ENET_100D	ENETCONN_P<3>
	ENETCONN	ENET_100D	ENETCONN_N<3>

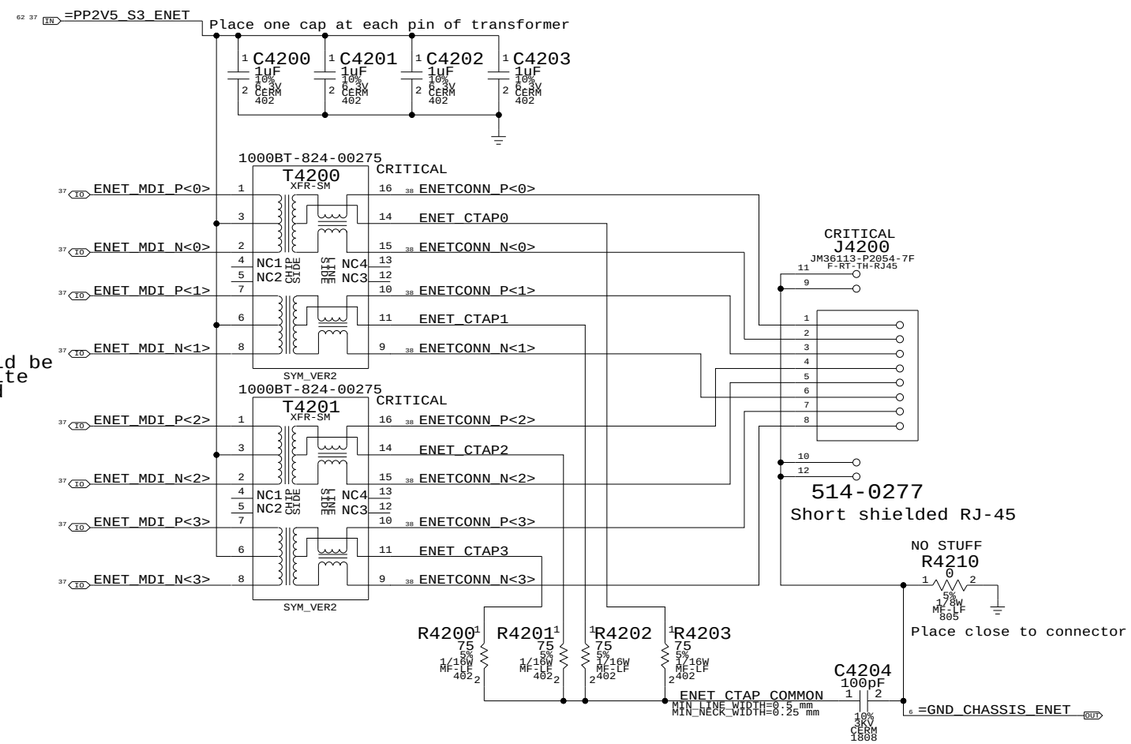
Page Notes

Power aliases required by this page:
- =PP2V5_ENET
- =GND_CHASSIS_ENET

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

Transformers should be mirrored on opposite sides of the board



Ethernet Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	38	81

PAGE NOTES

INPUT

=PP3V3_S0_FW - 3.3V POWER FOR FIREWIRE (MOBILE: OFF DURING SLEEP)
=PP3V3_S0_PCI - 3.3V POWER FOR PCI FIREWIRE (MOBILE: OFF DURING SLEEP)
PCI_GNT3_L - PCI GRANT FROM SB
PCI_CLK_FW - NEED TO REFERENCE TO ALIAS PAGE
PCI_RST_L - PCI RESET FROM SB
FW_PC0 - FIREWIRE POWER CLASS IDENTIFIER

INPUT/OUTPUT

PCI_AD<0..31>,PCI_C_BE_L<0..3>,PCI_FRAME_L,PCI_IRDY_L,PCI_TRDY_L,
PCI_DEVSEL_L, PCI_STOP_L, PCI_PAR, PCI_PERR_L, PCI_SERR_L
FW_A_TPA_P/N, FW_A_TPB_P/N, FW_A_TPBIAS - PORT 0 FIREWIRE DIFF PAIRS
FW_B_TPA_P/N, FW_B_TPB_P/N, FW_B_TPBIAS - PORT 1 FIREWIRE DIFF PAIRS
FW_C_TPA_P/N, FW_C_TPB_P/N, FW_C_TPBIAS - PORT 2 FIREWIRE DIFF PAIRS

OUTPUT

PCI_REQ3_L - PCI REQUEST TO SB
PM_CLKRUN_L - CLOCK-RUN PCI PROTOCOL
INT_PIRQD_L - INTERRUPT TO SB
PCI_PME_FW_L - DEDICATED PME FOR FIREWIRE (SB GPIO1)

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
6/20/2005 - BGA VERSION OF FW23256 ADDED
6/21/2005 - CHANGED INT*_TO_INT_PIRQD_L PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED PCI_IO TO ADD5 PER ARCHITECTURAL DEFINITION)
6/21/2005 - CHANGED REQ/GNT_TO_REQ3/GNT3 PER ARCHITECTURAL DEFINITION)
6/22/2005 - ADDED 510K PULL-DOWN ON RST* AND REMOVED CONNECTION TO PLT_RST_L
6/22/2005 - CHANGED CLK_FW DIFF_PAIR_NAMES TO BE RE-USE COMPLIANT
6/22/2005 - REMOVED CONSTRAINT SETS AS THEY WILL BE MANAGED ON BOARD SIDE
6/22/2005 - REMOVED C4421 - REDUNDANT
6/22/2005 - BRING OUT PC0 CONNECTION TO BE CONNECTED ON PORT PAGE
7/26/2005 - CONNECTED PIN E10 TO GND

MOBILE TURNS OFF CONTROLLER POWER DURING SLEEP
0.001A DURING SLEEP

62 =PP3V3_S3_FW

PLACE ONE CAP PER TWO PINS STARTING WITH C4424 ON VDD0

C4424 10UF 20% 6.3V X5R 603
C4418 0.1UF 10% 16V X5R 402
C4422 0.1UF 10% 16V CERM 402
C4426 0.1UF 10% 16V CERM 402
C4428 0.1UF 10% 16V CERM 402
C4430 0.1UF 10% 16V CERM 402
C4432 0.1UF 10% 16V CERM 402

L4400
600-OHM-300MA
0402

PLACE ONE CAP PER TWO PINS STARTING WITH C4416 ON VDDA0

PP3V3_S3_FW_AVDD
VOLTAGE=3.3V
MIN_LINE_WIDTH=0.5MM
MIN_NECK_WIDTH=0.2MM

C4416 10UF 20% 6.3V X5R 603
C4417 0.1UF 10% 16V X5R 402
C4429 0.1UF 10% 16V X5R 402
C4425 0.1UF 10% 16V X5R 402

62 =PP3V3_S3_PCI

CONNECT TO VDD FOR 3.3V OPERATION

U4400
FW32306
BGA
LEMENU

G4	VDD0		
M1	VDD1		
M2	VDD2		
K5	VDD3		
K6	VDD4		
K7	VDD5		
L13	VDD6		
H13	VDD7		
A2	VDD9		
D10	VDDA0		
A13	VDDA1		
B13	VDDA2		
A7	VDDA3		
A8	VDDA4		
D6	VDDA5		
A11	PCI_VIOS		
F10	PCI_AD0	PCI_AD<0>	
G10	PCI_AD1	PCI_AD<1>	
H10	PCI_AD2	PCI_AD<2>	
H12	PCI_AD3	PCI_AD<3>	
J13	PCI_AD4	PCI_AD<4>	
J12	PCI_AD5	PCI_AD<5>	
K13	PCI_AD6	PCI_AD<6>	
K10	PCI_AD7	PCI_AD<7>	
L12	PCI_AD8	PCI_AD<8>	
M13	PCI_AD9	PCI_AD<9>	
L11	PCI_AD10	PCI_AD<10>	
M12	PCI_AD11	PCI_AD<11>	
M11	PCI_AD12	PCI_AD<12>	
N12	PCI_AD13	PCI_AD<13>	
M10	PCI_AD14	PCI_AD<14>	
N11	PCI_AD15	PCI_AD<15>	
M4	PCI_AD16	PCI_AD<16>	
N5	PCI_AD17	PCI_AD<17>	
N4	PCI_AD18	PCI_AD<18>	
M3	PCI_AD19	PCI_AD<19>	
M2	PCI_AD20	PCI_AD<20>	
N3	PCI_AD21	PCI_AD<21>	
K4	PCI_AD22	PCI_AD<22>	
M1	PCI_AD23	PCI_AD<23>	
K2	PCI_AD24	PCI_AD<24>	
J4	PCI_AD25	PCI_AD<25>	
K1	PCI_AD26	PCI_AD<26>	
J2	PCI_AD27	PCI_AD<27>	
J1	PCI_AD28	PCI_AD<28>	
H2	PCI_AD29	PCI_AD<29>	
H4	PCI_AD30	PCI_AD<30>	
H1	PCI_AD31	PCI_AD<31>	
K12	PCI_CBE0*	PCI_C_BE_L<0>	
M9	PCI_CBE1*	PCI_C_BE_L<1>	
L3	PCI_CBE2*	PCI_C_BE_L<2>	
L1	PCI_CBE3*	PCI_C_BE_L<3>	
N10	PCI_PAR	PCI_PAR	
N6	PCI_FRAME*	PCI_FRAME_L	
M6	PCI_IRDY*	PCI_IRDY_L	
N7	PCI_TRDY*	PCI_TRDY_L	
N8	PCI_DEVSEL*	PCI_DEVSEL_L	
M7	PCI_STOP*	PCI_STOP_L	
L2	PCI_IDSEL	FW_PCI_IDSEL	
E2	PCI_REQ*	PCI_REQ1_L	
E1	PCI_GNT*	PCI_GNT1_L	
M8	PCI_PERR*	PCI_PERR_L	
N9	PCI_SERR*	PCI_SERR_L	
G2	PCI_CLK	PCI_CLK_FW	
D1	CLKRUN*	PM_CLKRUN_L	
F1	PCI_RST*	FW_PCI_RST_L	
D2	PCI_INTA*	INT_PIRQD_L	
F2	PCI_PME*	PCI_PME_FW_L	

R4431 22 5% 1/16W MF-LF 402

R4432 100 5% 1/16W MF-LF 402
THIS IS FROM ICH-7M

197S0030-3.2MMX2.5MM CRITICAL
Y4403 SM-2 24.576MHZ
R4400 390 5% 1/16W MF-LF 402
C4411 15PF 5% 50V CERM 402
C4412 15PF 5% 50V CERM 402
NEED TO CHECK CRYSTAL LOAD CAPACITANCE

XI	A5	FW_XI	
XO	B5	FW_XO	
RESET*	B4	FW_PWRON_RST_L	
R1	A6	FW_R1	R4452 2.49K 1% 1/16W MF-LF 402
R0	B7	FW_R0	
TPBIAS0	B8	FW_A_TPBIAS	
TPA0_P	A9	FW_A_TPA_P	
TPA0_N	B9	FW_A_TPA_N	
TPB0_P	B10	FW_A_TPB_P	
TPB0_N	A10	FW_A_TPB_N	
TPBIAS1	D8	FW_B_TPBIAS	
TPA1_P	A11	FW_B_TPA_P	
TPA1_N	B11	FW_B_TPA_N	
TPB1_P	B12	FW_B_TPB_P	
TPB1_N	A12	FW_B_TPB_N	
TPBIAS2	C13	FW_C_TPBIAS	
TPA2_P	C11	FW_C_TPA_P	
TPA2_N	C12	FW_C_TPA_N	
TPB2_P	D13	FW_C_TPB_P	
TPB2_N	D12	FW_C_TPB_N	

SPEC RECOMMENDS 2.49K

C4420 0.1UF 10% 16V X5R 402
R4420 510K 5% 1/16W MF-LF 402

MODE_420	M5	MODE FOR EXTERNAL LINK	
MODE_A	B6		
PC0	E12	FW_PC0	DUAL PORT DEVICES ARE POWER CLASS 4 (‘100’) SINGLE PORT DEVICES ARE POWER CLASS 0 (‘000’)
PC1	F13		
PC2	F12		
CONTENDER	G12	LOW = NOT BUS MANAGER	
CARDBUSN	B1	LOW = PCI OPERATION	
MPCI_ACTN_323	E10		

MANUFACTURING TEST PINS

TEST0	C2	
TEST1	C1	
TEST	A4	
SE	A3	
SM	B3	

VSS0	A1		
VSS1	B2		
VSS2	C3		
VSS3	D4		
VSS4	E4		
VSS5	E5		
VSS6	F4		
VSS7	F6		
VSS8	F7		
VSS9	F8		
VSS10	G1		
VSS11	G6		
VSS12	G7		
VSS13	G8		
VSS14	H6		
VSS15	H7		
VSS16	H8		
VSS17	J5		
VSS18	J9		
VSS19	J10		
VSS20	K8		
VSS21	K9		
VSS22	N13		
VSSA0	E13		
VSSA1	E9		
VSSA2	D9		
VSSA3	D7		
VSSA4	D5		

FIREWIRE CONTROLLER

SYNC_MASTER=MSX SYNC_DATE=08/29/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 39 OF 81	

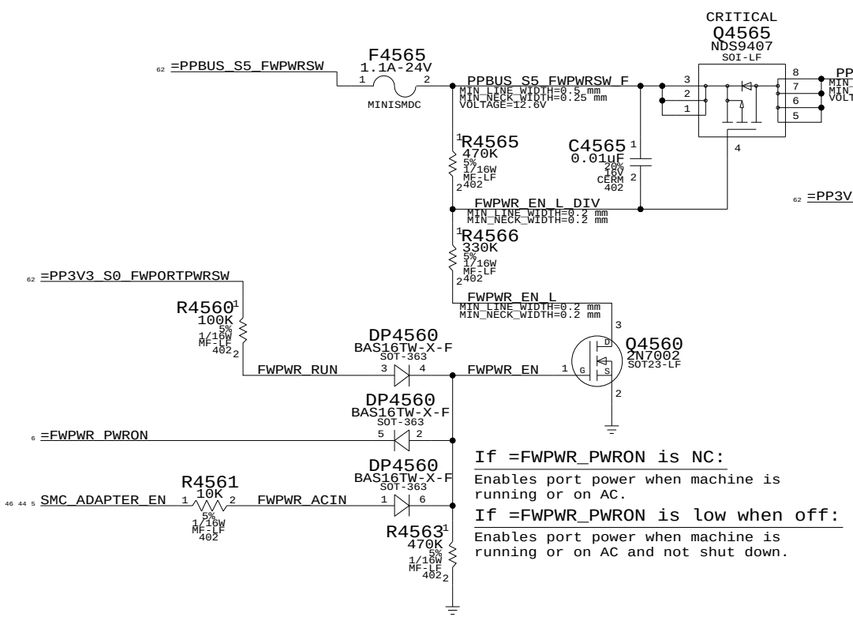
Page Notes

Power aliases required by this page:
- =PPBUS_S0_FWPWRSW (system supply for bus power)
- =PP3V3_S0_FWPORTPWRSW

Signal aliases required by this page:
- =FWPWR_PWRON (see related text note below)

BOM options provided by this page:
(NONE)

Port Power Switch



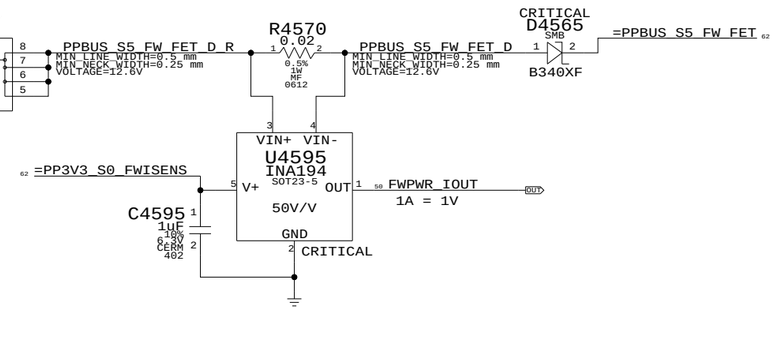
If =FWPWR_PWRON is NC:

Enables port power when machine is running or on AC.

If =FWPWR_PWRON is low when off:

Enables port power when machine is running or on AC and not shut down.

FireWire Port Current Sense



FireWire Port Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 40 OF 81	

ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	NET_TYPE PHYSICAL	
PROVIDED BY PHY PAGE	FW	FW_110D	FW_PORT1_TPA_FL_P 41
	FW	FW_110D	FW_PORT1_TPA_FL_N 41
	FW	FW_110D	FW_PORT1_TPB_FL_P 41
	FW	FW_110D	FW_PORT1_TPB_FL_N 41

Page Notes

Power aliases required by this page:
- =PPFW_PORT1
- =PP3V3_S5_FWLATEVG
- =GND_CHASSIS_FW_PORT1

Signal aliases required by this page:
(NONE)

NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

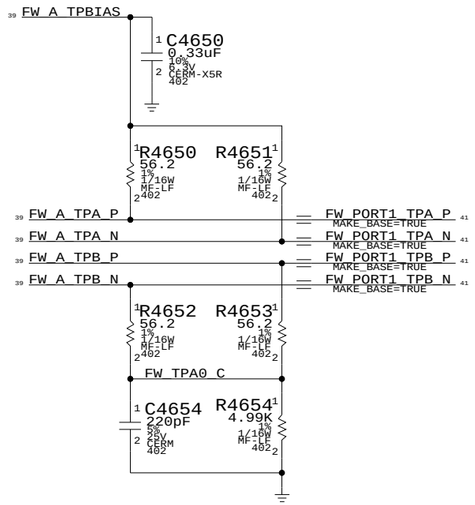
BOM options provided by this page:
(NONE)

NOTE: FireWire TPA/TPB pairs are NOT constrained on this page. It is assumed that FireWire PHY page will provide the appropriate constraints to apply to entire TPA/TPB XNets.

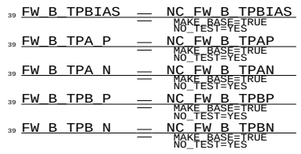
1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

Termination

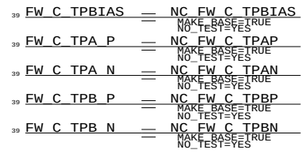
Place close to FireWire PHY



2nd TPA/TPB pair unused

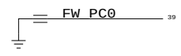


3rd TPA/TPB pair unused

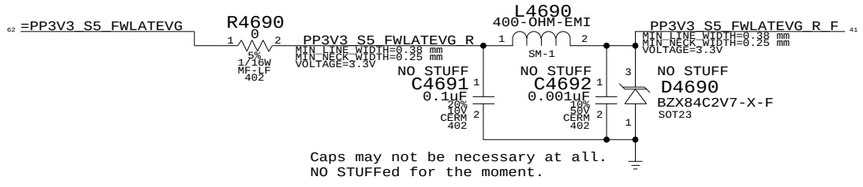


FW Power Class Strap

Single-port system sets PC=0

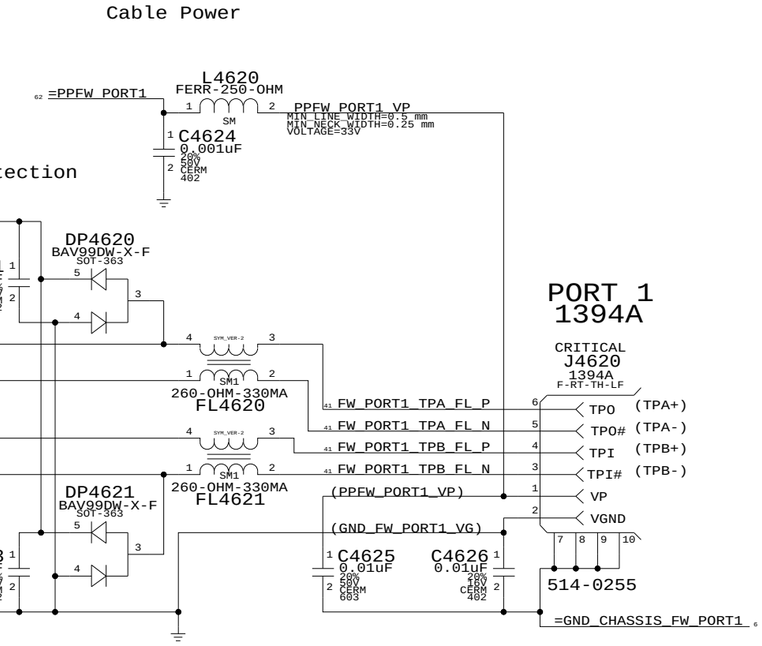


Late-VG Protection Power



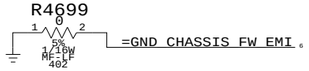
Caps may not be necessary at all.
NO STUFFed for the moment.

Cable Power



"Snapback" & "Late VG" Protection

PORT 1 1394A

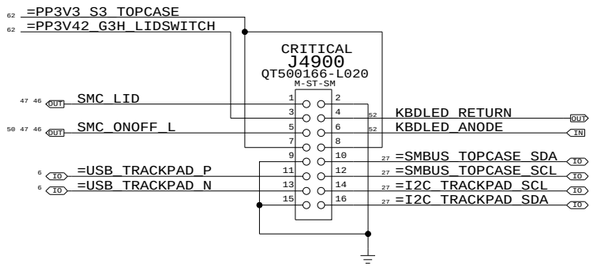


FireWire Ports

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

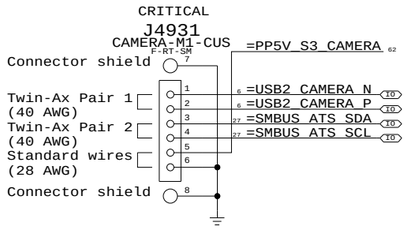
APPLE COMPUTER INC.	SIZE	DRAWING NUMBER	REV.
	D	051-6941	07001
	SCALE NONE	SHT 41 OF 81	

Top-Case Connector



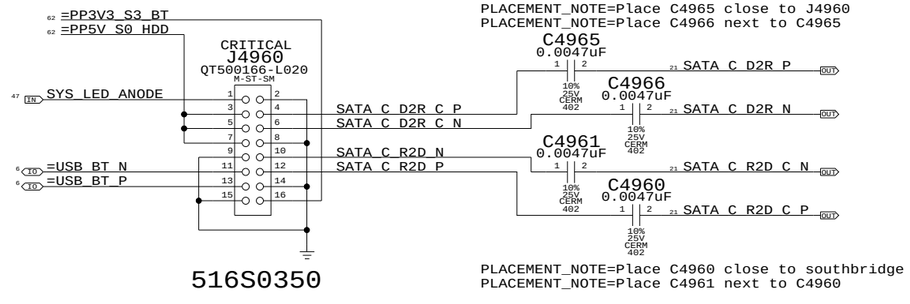
516S0350

Camera Connector



518S0371

Bluetooth (M13P) & SATA HDD Flex Connector



516S0350

Internal USB Connections

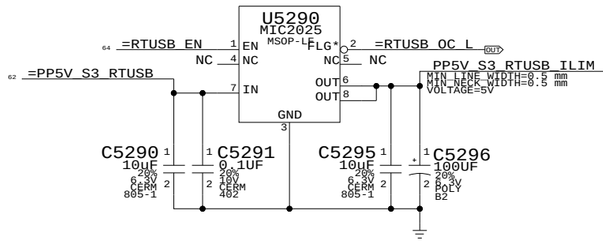
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

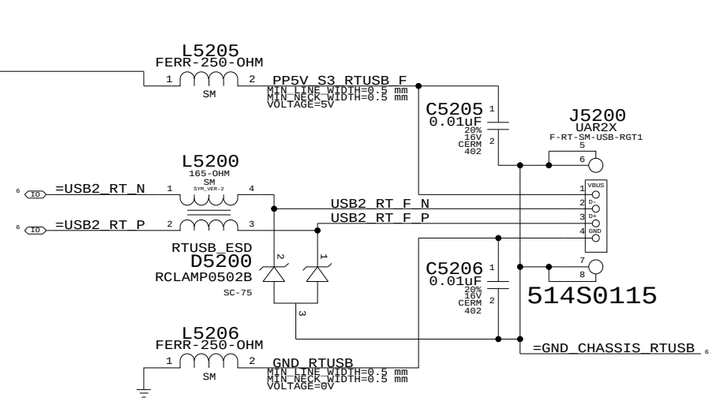
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	42	81

Port Power Switch



Right USB Port



Place L5200, L5205 and L5206 across moat

External USB Connector

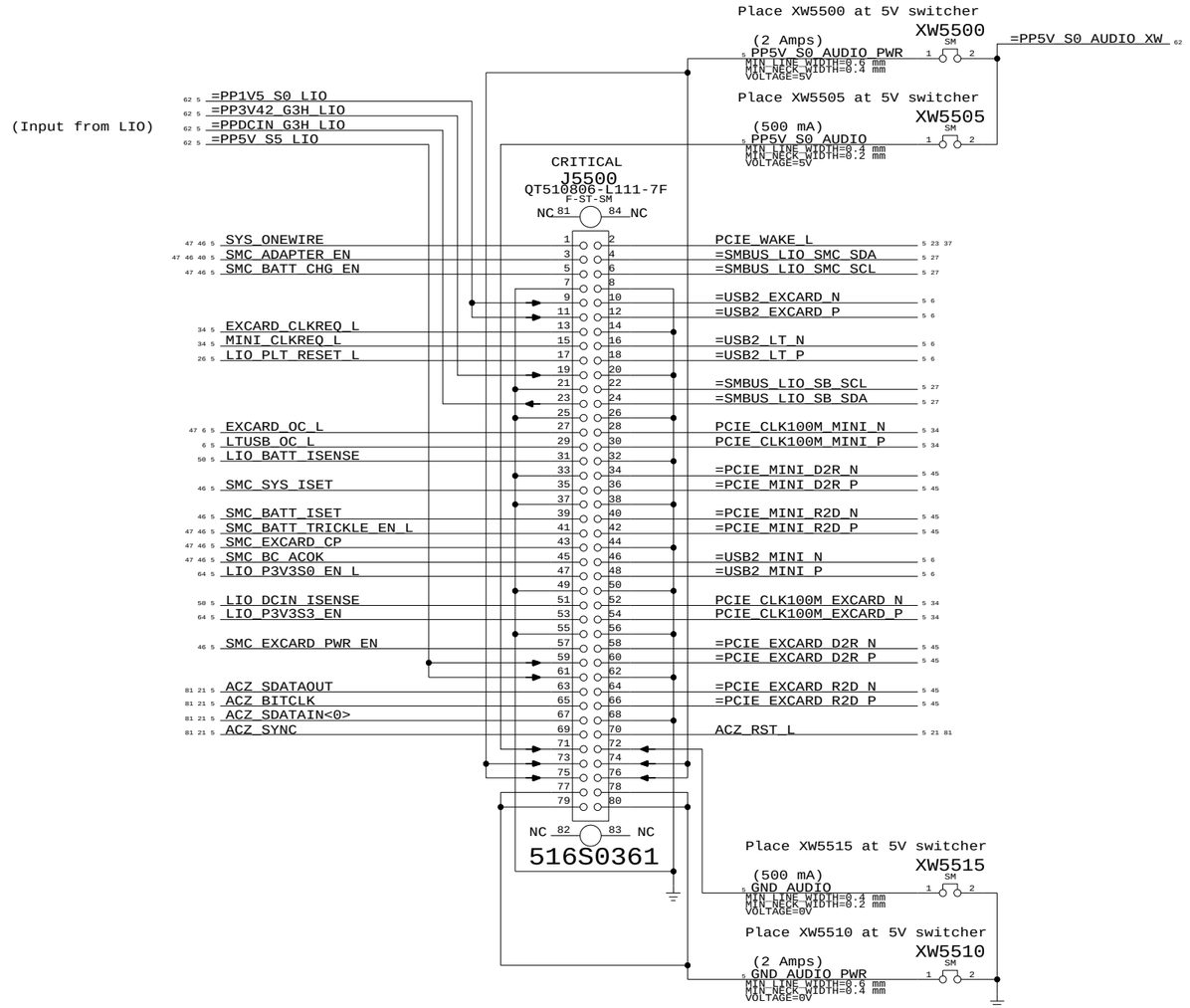
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	43	81

Left I/O Board Connector



Left I/O Board Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	44	81

PCI-E x1 Port "A" = Ethernet (Yukon)

PCI-E x1 Port "B" = PCI-E Mini Card

C5710 0.1uF 10% 16V X5R 402

C5711 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_MINI_R2D_P	MAKE_BASE=TRUE	PCIE_MINI_R2D_C_P	PCIE_B_R2D_C_P	22
=PCIE_MINI_R2D_N	MAKE_BASE=TRUE	PCIE_MINI_R2D_C_N	PCIE_B_R2D_C_N	22
=PCIE_MINI_D2R_P	MAKE_BASE=TRUE	PCIE_MINI_D2R_P	PCIE_B_D2R_P	22
=PCIE_MINI_D2R_N	MAKE_BASE=TRUE	PCIE_MINI_D2R_N	PCIE_B_D2R_N	22

PCI-E x1 Port "C" = ExpressCard

C5720 0.1uF 10% 16V X5R 402

C5721 0.1uF 10% 16V X5R 402 Place caps close to SB

=PCIE_EXCARD_R2D_P	MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_P	PCIE_C_R2D_C_P	22
=PCIE_EXCARD_R2D_N	MAKE_BASE=TRUE	PCIE_EXCARD_R2D_C_N	PCIE_C_R2D_C_N	22
=PCIE_EXCARD_D2R_P	MAKE_BASE=TRUE	PCIE_EXCARD_D2R_P	PCIE_C_D2R_P	22
=PCIE_EXCARD_D2R_N	MAKE_BASE=TRUE	PCIE_EXCARD_D2R_N	PCIE_C_D2R_N	22

PCI-E x1 Port "D" = Unused

TP_PCIE_D_R2DP	MAKE_BASE=TRUE	PCIE_D_R2D_C_P	22
TP_PCIE_D_R2DN	MAKE_BASE=TRUE	PCIE_D_R2D_C_N	22
TP_PCIE_D_D2RP	MAKE_BASE=TRUE	PCIE_D_D2R_P	22
TP_PCIE_D_D2RN	MAKE_BASE=TRUE	PCIE_D_D2R_N	22

PCI-E x1 Port "E" = Unused

TP_PCIE_E_R2DP	MAKE_BASE=TRUE	PCIE_E_R2D_C_P	22
TP_PCIE_E_R2DN	MAKE_BASE=TRUE	PCIE_E_R2D_C_N	22
TP_PCIE_E_D2RP	MAKE_BASE=TRUE	PCIE_E_D2R_P	22
TP_PCIE_E_D2RN	MAKE_BASE=TRUE	PCIE_E_D2R_N	22

PCI-E x1 Port "F" = Unused

TP_PCIE_F_R2DP	MAKE_BASE=TRUE	PCIE_F_R2D_C_P	22
TP_PCIE_F_R2DN	MAKE_BASE=TRUE	PCIE_F_R2D_C_N	22
TP_PCIE_F_D2RP	MAKE_BASE=TRUE	PCIE_F_D2R_P	22
TP_PCIE_F_D2RN	MAKE_BASE=TRUE	PCIE_F_D2R_N	22

PCI-E Connections

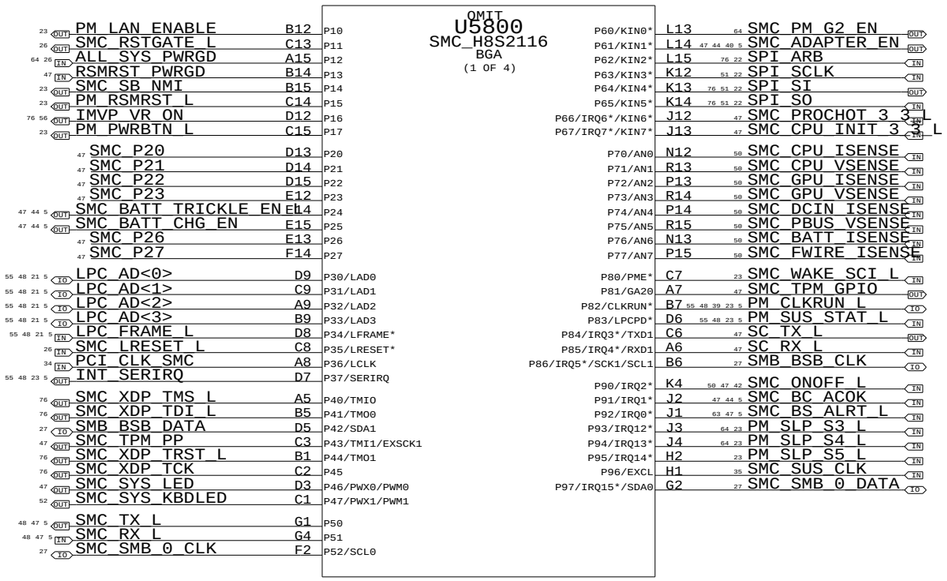
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

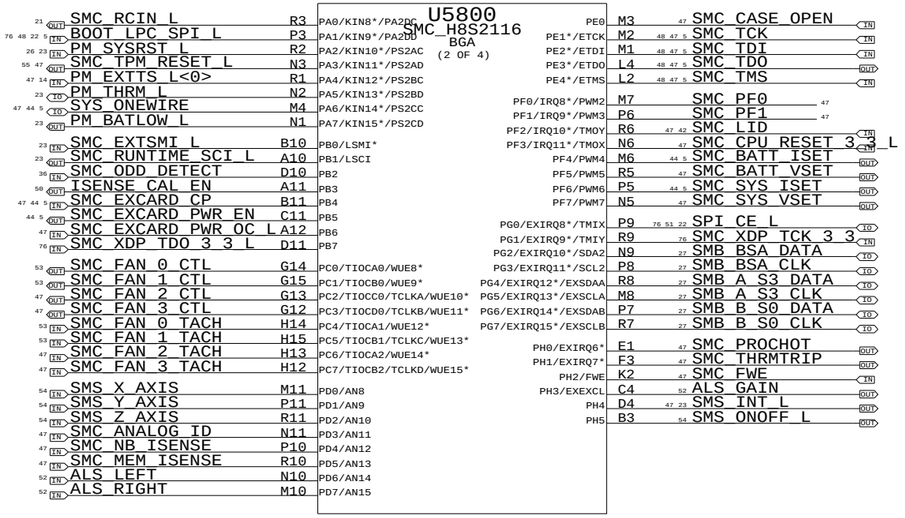
APPLE COMPUTER INC.

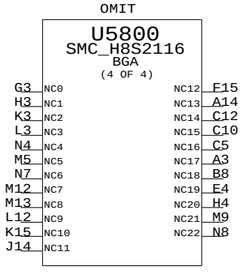
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

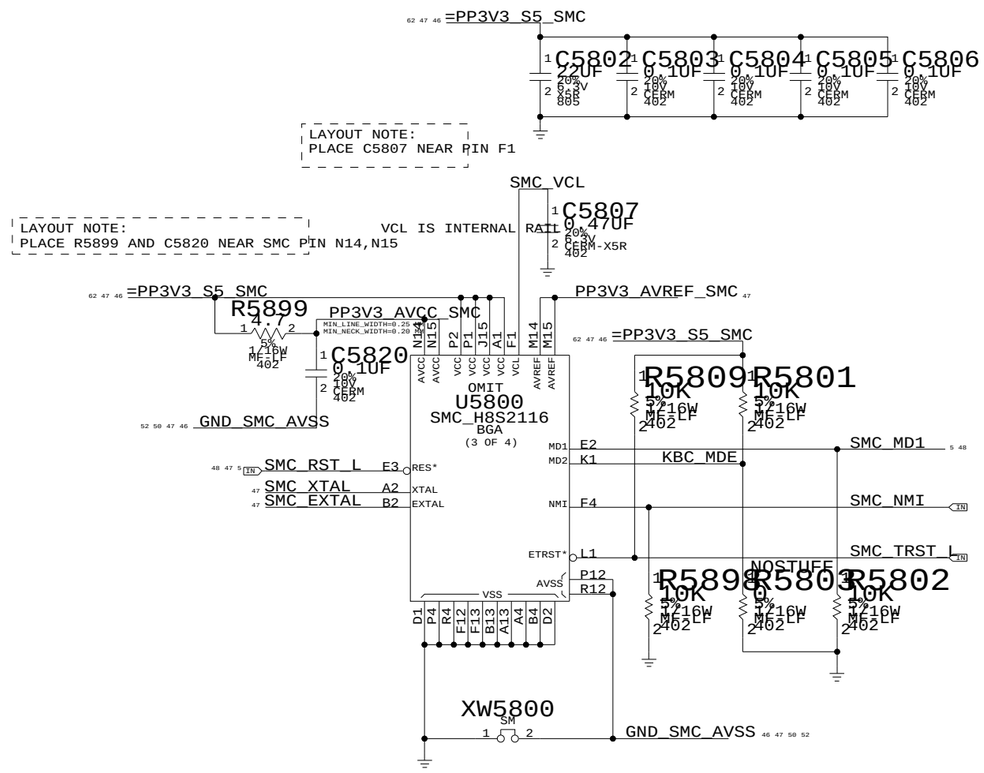
SCALE	SHT	OF
NONE	45	81

UNUSED PINS HAVE THE FORMAT
SMC_XXX_WHERE XXX IS THE PORT NUMBER.
THEY ARE SETS BY SOFTWARE TO BE
DRIVEN OUTPUTS ALWAYS SO THEY
CAN BE LEFT NO-CONNECTED.









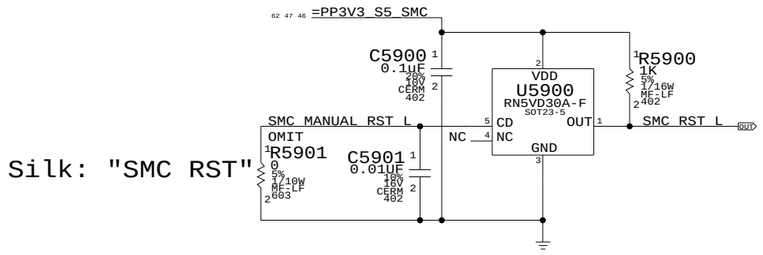
SMC

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

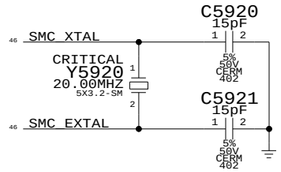
SCALE	SHT	OF
NONE	46	81

SMC Reset Button / Brownout Detect

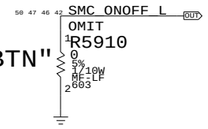


Silk: "SMC RST"

SMC Crystal Circuit

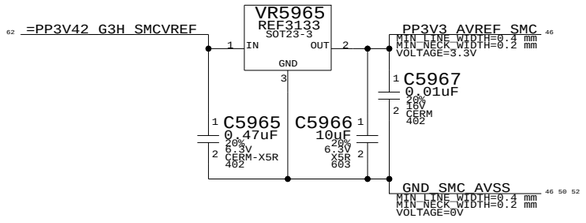


Debug Power Button

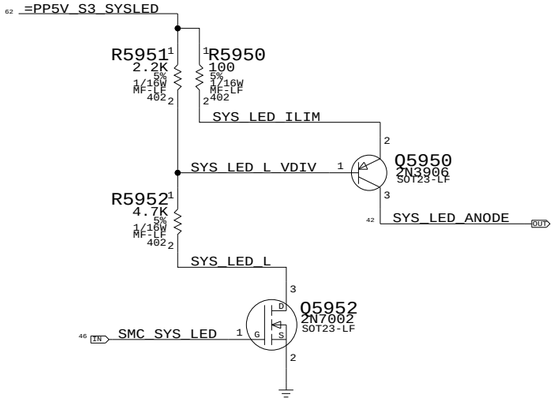


Silk: "PWR BTN"

SMC AVREF Supply

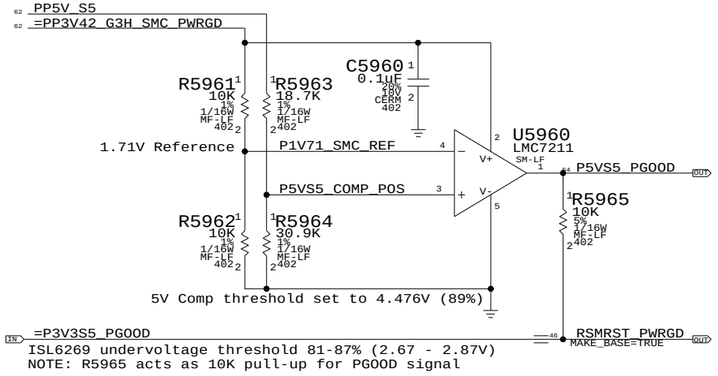


System (Sleep) LED Circuit



SMC PWRGD Circuit

Reports when 5V S5 and 3.3V S5 are in regulation



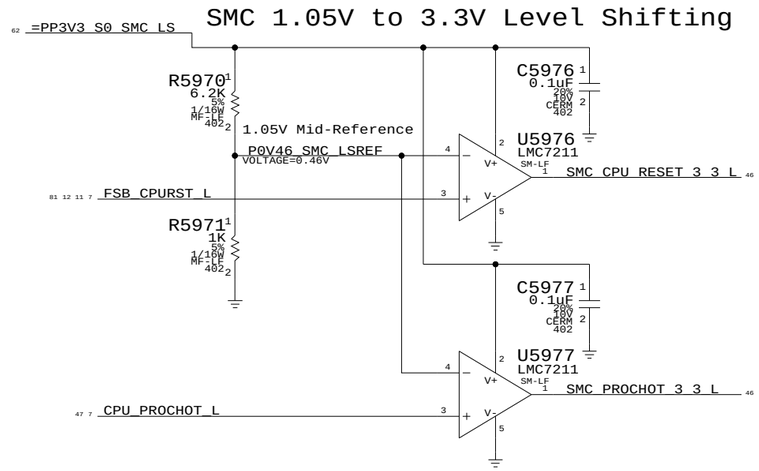
ISL6269 undervoltage threshold 81-87% (2.67 - 2.87V)
NOTE: R5965 acts as 10K pull-up for PGOOD signal

46 SMC_CPU_INIT_3_3_L — FWH_INIT_L 5 21 48 (MAKE_BASE=TRUE)
46 SMC_NB_ISENSE — SMC_P1V05S0_ISENSE 50 (MAKE_BASE=TRUE)
46 SMC_MEM_ISENSE — SMC_P1V8S3_ISENSE 50 (MAKE_BASE=TRUE)
46 14 PM_EXITS_L<0> — DIMM_OVERTEMP_L 28 29 (MAKE_BASE=TRUE)

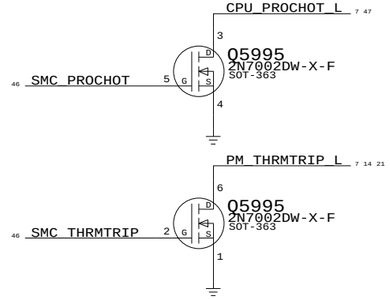
46 SMC_ANALOG_ID — TP_SMC_ANALOG_ID (MAKE_BASE=TRUE)
46 SMC_BATT_VSET — TP_SMC_BATT_VSET (MAKE_BASE=TRUE)
46 SMC_SYS_VSET — TP_SMC_SYS_VSET (MAKE_BASE=TRUE)
46 SMC_FAN_2_CTL — TP_SMC_FAN_2_CTL (MAKE_BASE=TRUE)
46 SMC_FAN_2_TACH — TP_SMC_FAN_2_TACH (MAKE_BASE=TRUE)
46 SMC_FAN_3_CTL — TP_SMC_FAN_3_CTL (MAKE_BASE=TRUE)
46 SMC_FAN_3_TACH — TP_SMC_FAN_3_TACH (MAKE_BASE=TRUE)
46 SMC_P20 — TP_SMC_P20 (MAKE_BASE=TRUE)
SMC_P21 — TP_SMC_P21 (MAKE_BASE=TRUE)
46 SMC_P22 — TP_SMC_P22 (MAKE_BASE=TRUE)
46 SMC_P23 — TP_SMC_P23 (MAKE_BASE=TRUE)
46 SMC_P26 — TP_SMC_P26 (MAKE_BASE=TRUE)
46 SMC_P27 — TP_SMC_P27 (MAKE_BASE=TRUE)
46 SMC_PF0 — TP_SMC_PF0 (MAKE_BASE=TRUE)
46 SMC_PF1 — TP_SMC_PF1 (MAKE_BASE=TRUE)

SMC_TPM_GPIO1
46 SMC_TPM_GPIO — R5990 0 5% 1/16W MF-LF 402 — TPM_GPIO1 55
SMC_TPM_GPIO2
R5991 0 5% 1/16W MF-LF 402 — TPM_GPIO2 55
SMC_TPM_PP
46 SMC_TPM_PP — R5995 0 5% 1/16W MF-LF 402 — TPM_PP 55
DEVELOPMENT
R5992 0 5% 1/16W MF-LF 402
46 SC_RX_L — SMC_RX_L 5 46 47 48
DEVELOPMENT
R5993 0 5% 1/16W MF-LF 402
46 SC_TX_L — SMC_TX_L 5 46 47 48
R5994 0 5% 1/16W MF-LF 402
46 SMC_EXCARD_PWR_OC_L — EXCARD_OC_L 5 6 44

SMC 1.05V to 3.3V Level Shifting



SMC 3.3V to 1.05V Level Shifting



62 47 46 =PP3V3_S5_SMC
62 55 =PP3V3_S3_TPM
62 54 =PP3V3_S3_SMS

46 23 SMS_INT_L	R5829	10K	5% 1/16W MF-LF 402	
55 46 SMC_TPM_RESET_L	R5827	10K	5% 1/16W MF-LF 402	
50 47 46 42 SMC_ONOFF_L	R5808	10K	5% 1/16W MF-LF 402	
46 42 SMC_LID	R5814	100K	5% 1/16W MF-LF 402	
46 SMC_FWE	R5815	10K	5% 1/16W MF-LF 402	
48 47 46 5 SMC_TX_L	R5817	10K	5% 1/16W MF-LF 402	
48 47 46 5 SMC_RX_L	R5818	100K	5% 1/16W MF-LF 402	
46 44 5 SYS_ONEWIRE	R5819	2.0K	5% 1/16W MF-LF 402	
63 46 5 SMC_BS_ALRT_L	R5821	100K	5% 1/16W MF-LF 402	
48 46 5 SMC_TMS	R5822	10K	5% 1/16W MF-LF 402	
48 46 5 SMC_TDO	R5823	10K	5% 1/16W MF-LF 402	
48 46 5 SMC_TDI	R5824	10K	5% 1/16W MF-LF 402	
48 46 5 SMC_TCK	R5825	10K	5% 1/16W MF-LF 402	
46 44 5 SMC_BATT_TRICKLE_EN_L	R5810	10K	5% 1/16W MF-LF 402	
46 44 5 SMC_BATT_CHG_EN	R5811	10K	5% 1/16W MF-LF 402	
46 44 40 5 SMC_ADAPTER_EN	R5812	10K	5% 1/16W MF-LF 402	
46 SMC_CASE_OPEN	R5813	10K	5% 1/16W MF-LF 402	
46 44 5 SMC_BC_ACOK	R5826	470K	5% 1/16W MF-LF 402	
46 44 5 SMC_EXCARD_CP	R5828	10K	5% 1/16W MF-LF 402	

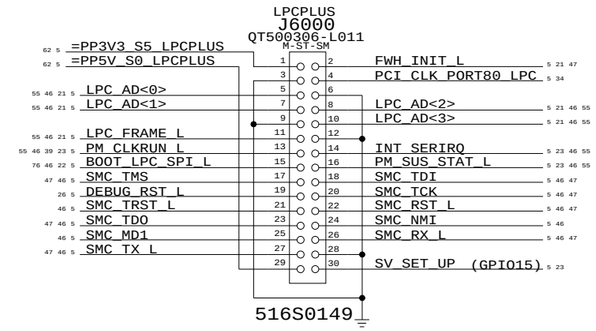
SMC Support

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE D | DRAWING NUMBER 051-6941 | REV. 07001

SCALE NONE | SHT 47 OF 81



LPC+ Debug Connector

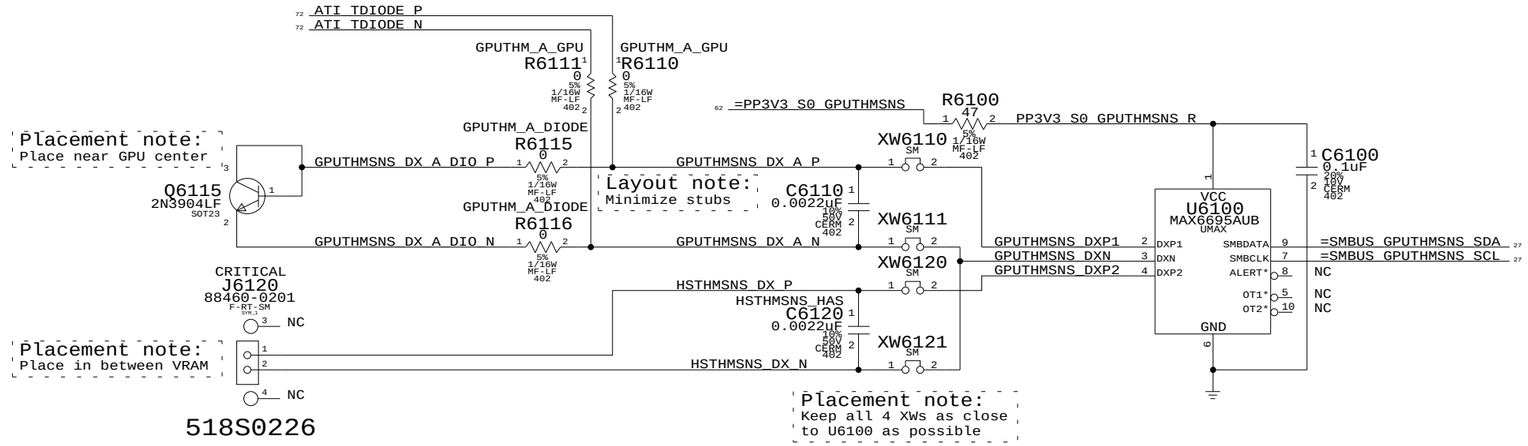
SYNC_MASTER=M42 SYNC_DATE=07/20/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

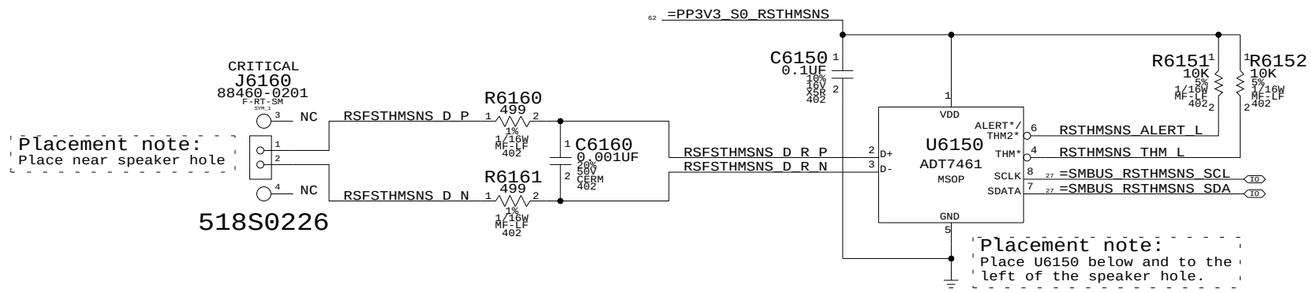
SCALE	SHT	OF
NONE	48	81

GPU / Heat Pipe Thermal Sensor

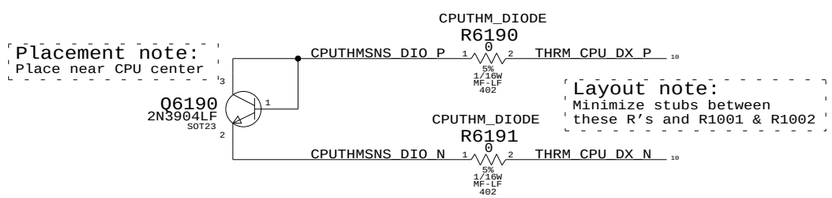


PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	1	RES,0,1/16W,0402	C6120		HSTHMSNS_NOT

Right-Side/Fin Stack Thermal Sensor



CPU Back-Up Thermal Diode



R1001 / R1002 are not currently BOMOPTIONed. Can not programatically unstuff those parts to stuff these.

Thermal Sensors

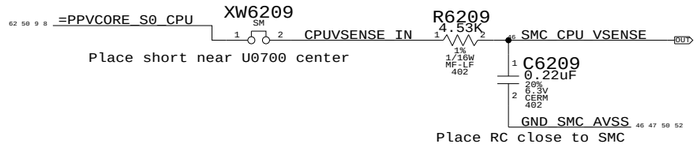
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

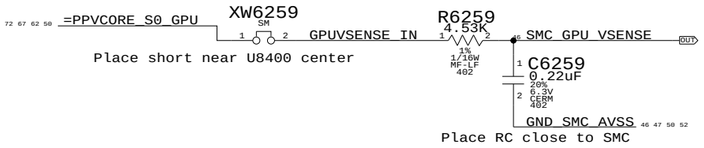
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	49	81

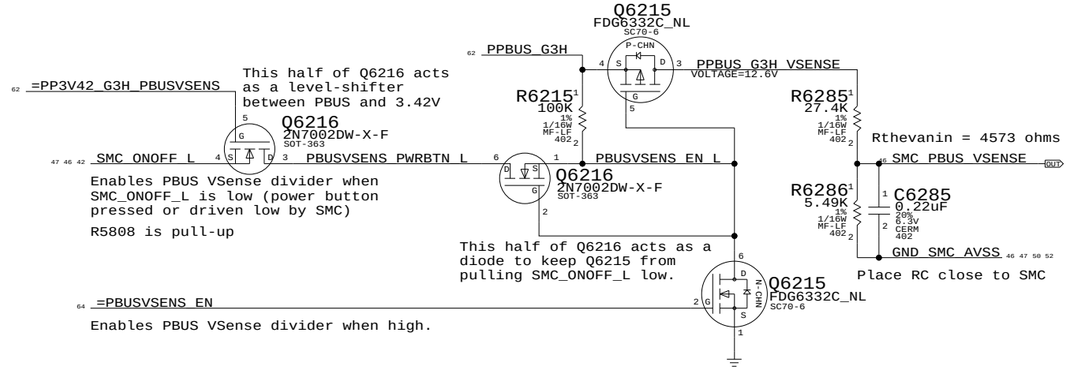
CPU Voltage Sense / Filter



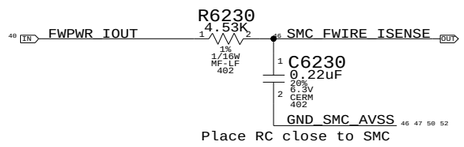
GPU Voltage Sense / Filter



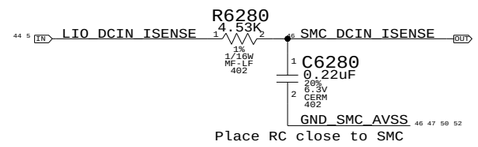
PBUS Voltage Sense Enable & Filter



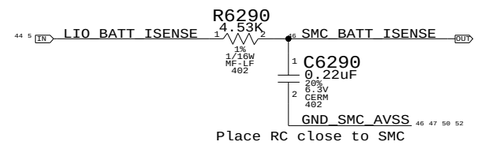
FireWire Current Sense Filter



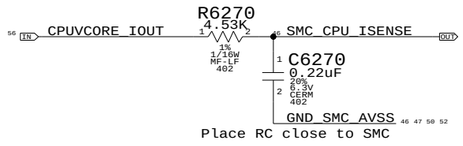
DCIN Current Sense Filter



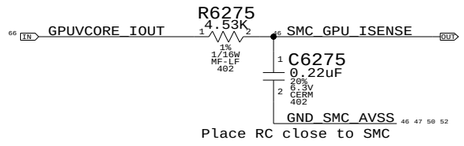
Battery Current Sense Filter



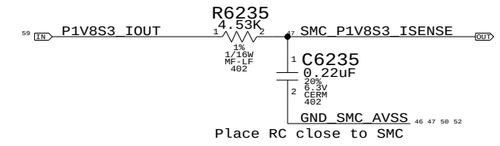
CPU Current Sense Filter



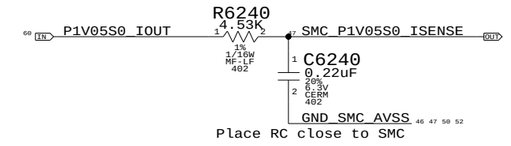
GPU Current Sense Filter



1.8V S3 (Memory) Current Sense Filter

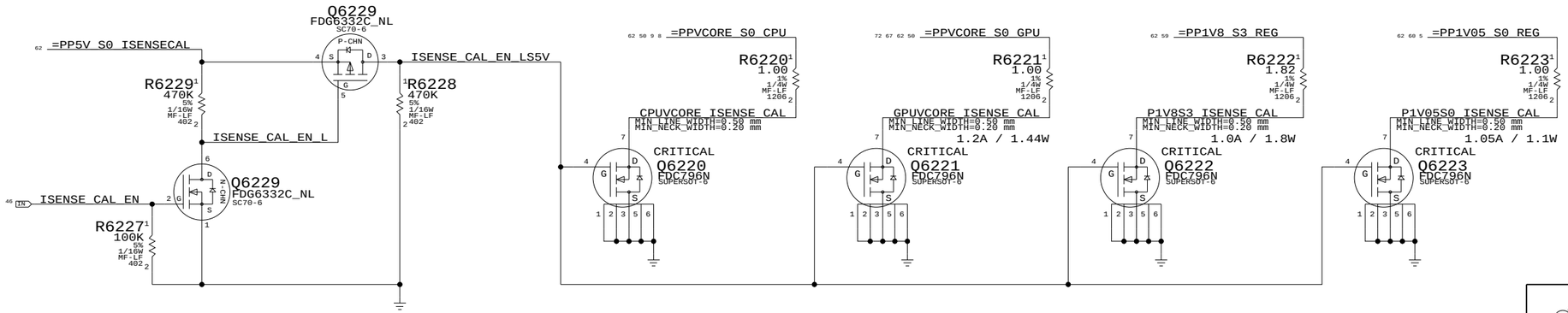


1.05V S0 (NB) Current Sense Filter



Current Sense Calibration Circuit

Switches in fixed load on power supplies to calibrate current sense circuits



Current & Voltage Sensing			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
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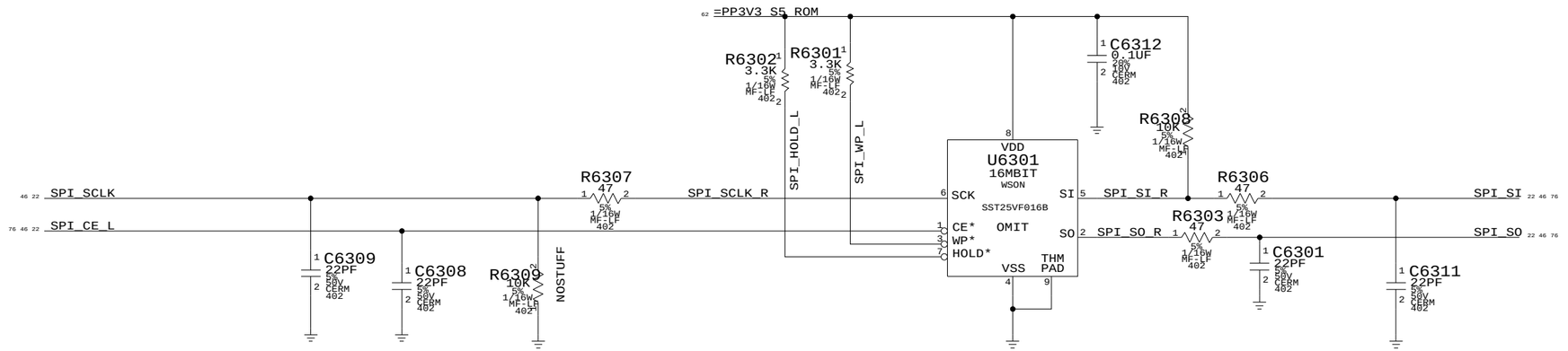
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 07001
	SCALE NONE	SHT 50 OF 81	



R6309 IS NOT NEEDED WHEN SHARING SPI FLASH WITH ICH7M AND TEKOA(LAN CHIP)

R6307 AND R6306 SHOULD BE PLACED LESS THAN 100 MILS FORM ICH7M

R6303 SHOULD BE PLACED LESS THAN 100 MILS FORM FLASH ROM

SPI BOOTROM

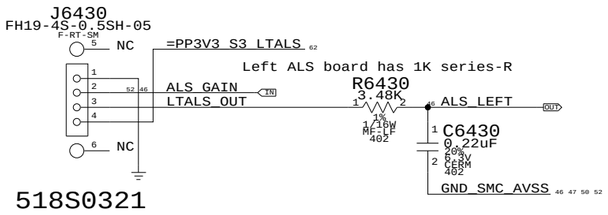
SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

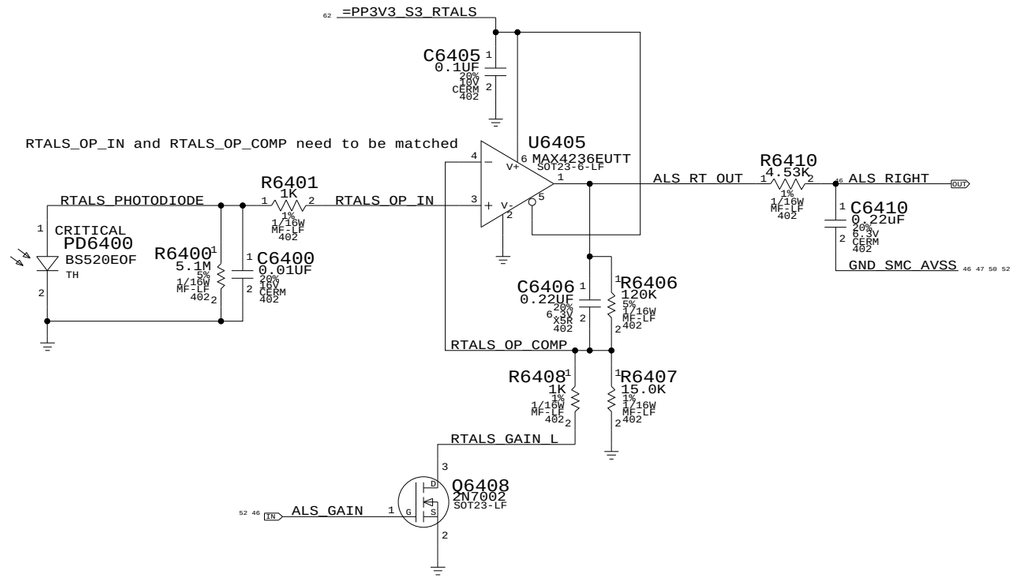
SCALE	SHT	OF
NONE	51	81

Left ALS "Connector"

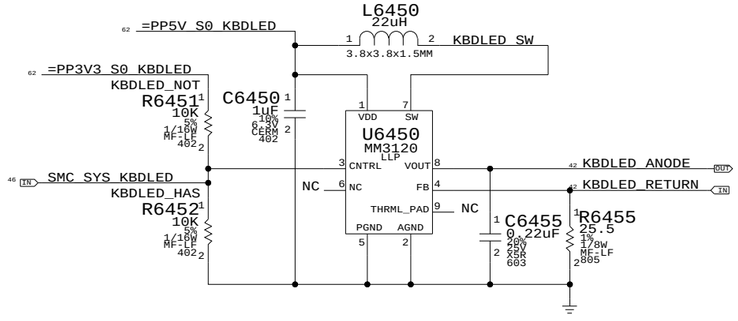


518S0321

Right ALS Circuit



Keyboard LED Driver



ALS Support			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
NOTICE OF PROPRIETARY PROPERTY			
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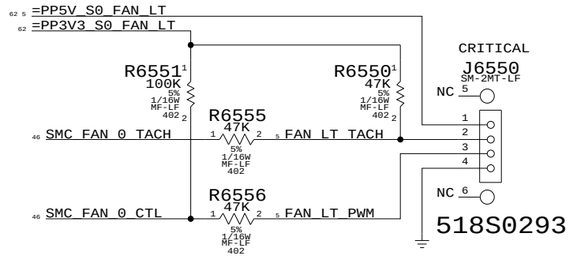
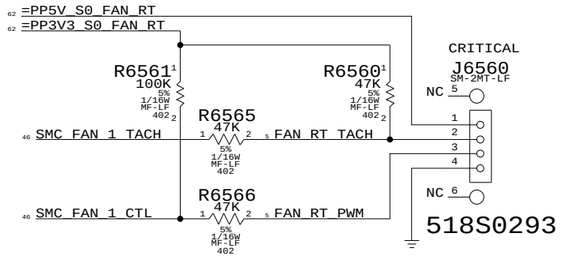
APPLE COMPUTER INC.	SIZE D	DRAWING NUMBER 051-6941	REV. 07001
	SCALE NONE	SHT 52 OF 81	

Left Fan



Right Fan



Fan Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	53	81

PAGE NOTES

INPUT

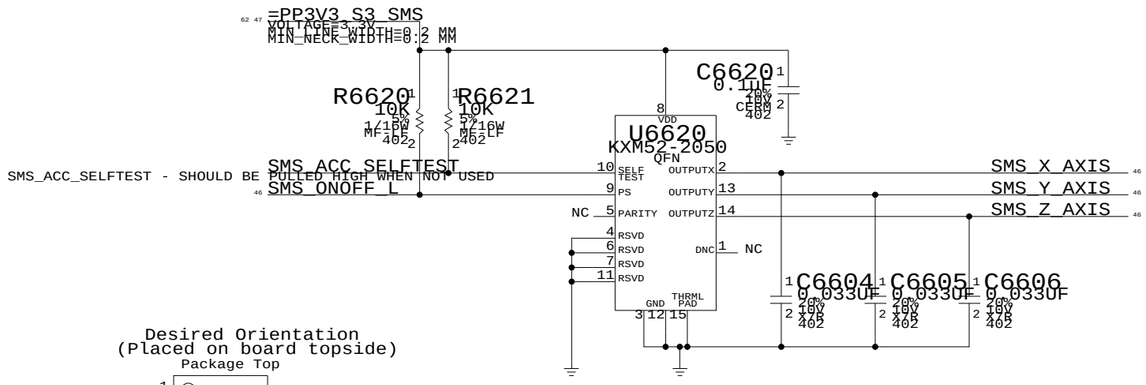
=PP3V3_S3_SMS - 3.3V POWER FOR SMS (STAYS ALIVE IN SLEEP)
SMS_ONOFF_L - CONNECT TO SMC TO BE ABLE TO PUT SMS INTO LOW-POWER MODE

OUTPUT

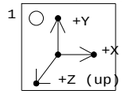
SMS_ACC_*_AXIS - ACCELEROMETER OUTPUT TO SCU

PAGE HISTORY

5/19/2005 - FIRST REVISION OF PAGE
7/26/2005 - REMOVED BOM TABLE AND UPDATED SYMBOL TO KXM52-2050
7/26/2005 - CONNECTED PD PIN TO SMC'S SMS_ONOFF_L
7/26/2005 -



Desired Orientation
(Placed on board topside)



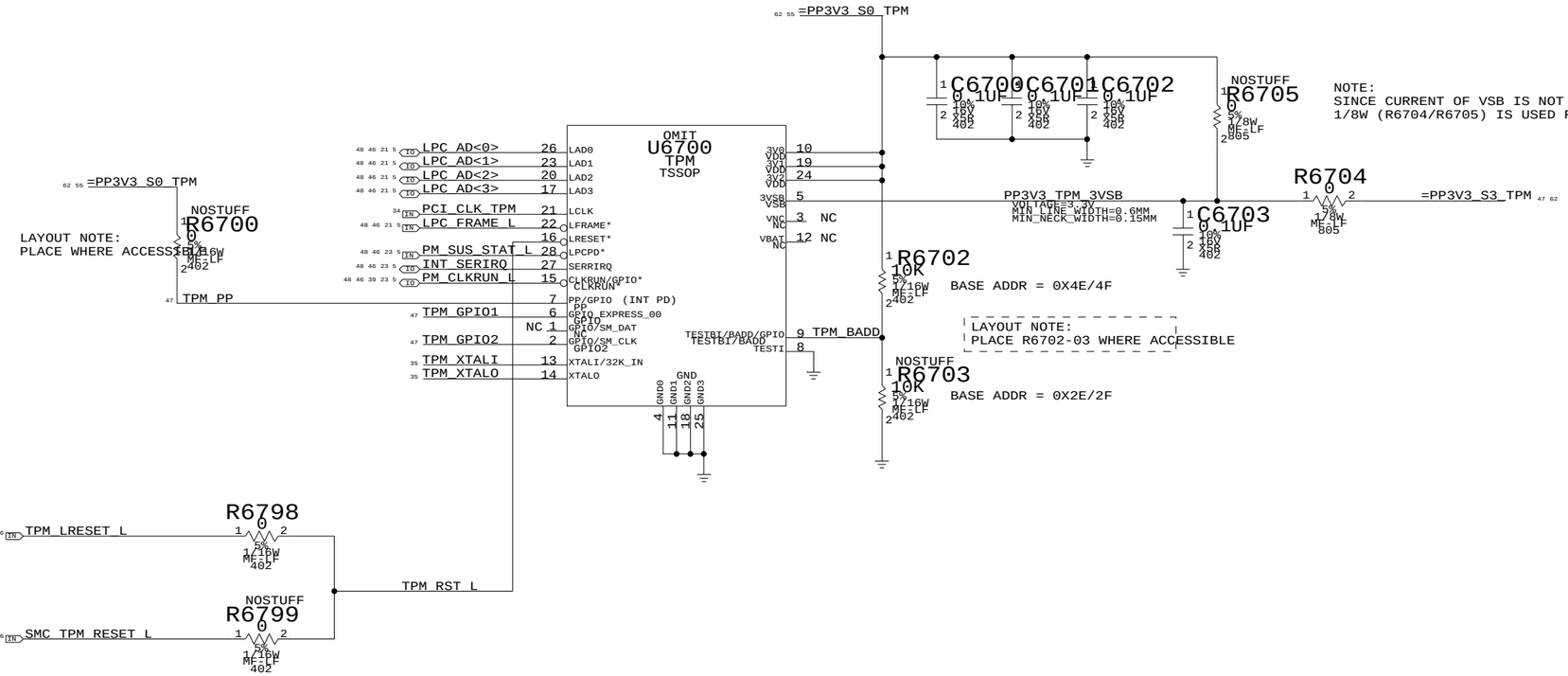
SMS

SYNC_MASTER=(M42) SYNC_DATE=07/26/2005

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	54	81



TPM

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	55	81

DPRSLPVR	DPRSTP*	PSI*	Operation	Mode
0	1	1	2-Phase	CCM
0	1	0	1-Phase	CCM
1	0	1	1-Phase	DCM
1	1	0	1-Phase	DCM

=PPVOUT_S0_IMVP6_REG
Vout = Variable
36A max output
(Inductors limit)

CPU VCore Current Sense

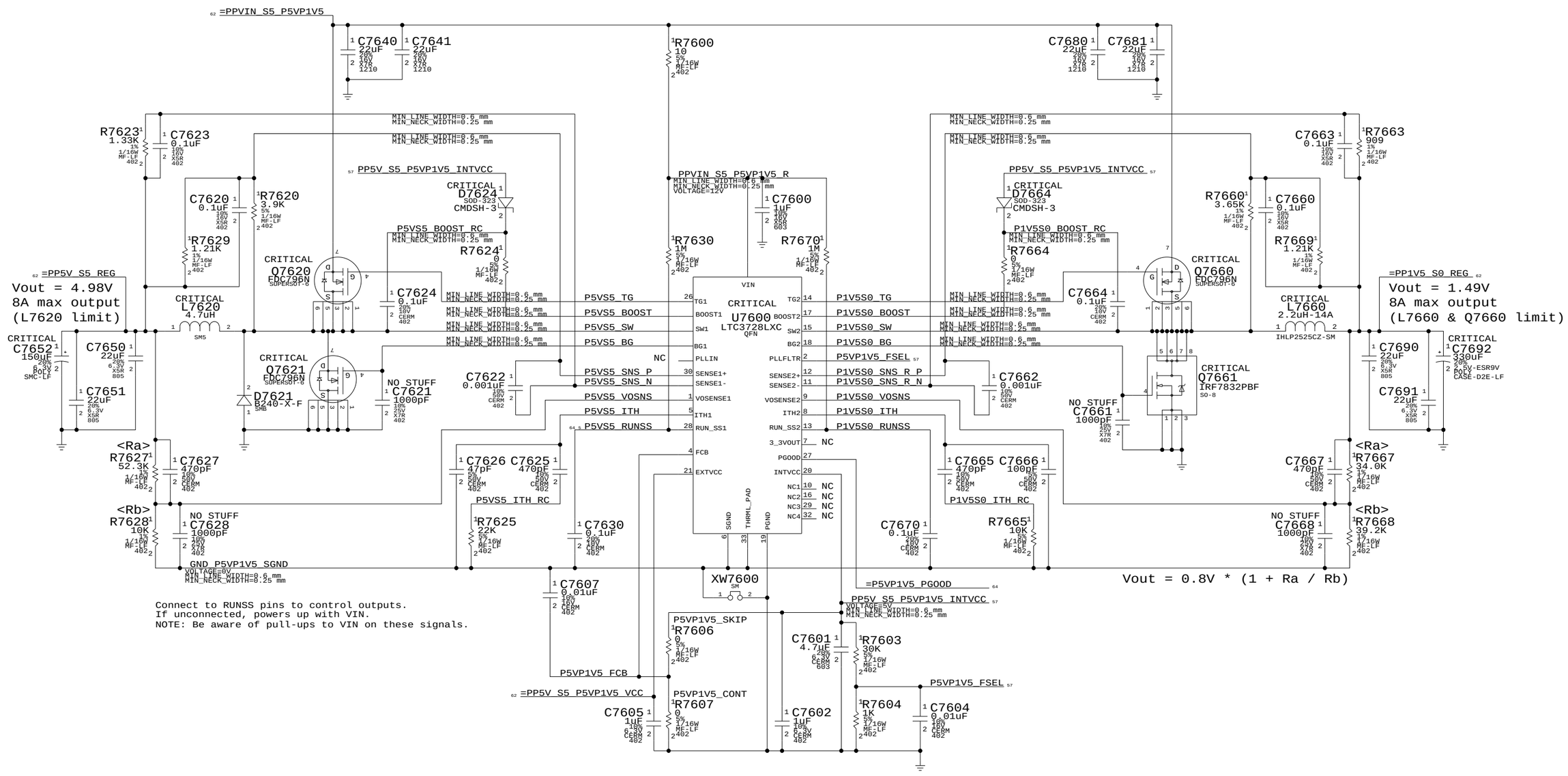
Vout = Gain * ((2.1 mV/A * Iload) + Voffset)
Voffset = (Vdrp_offset * Kdroop) + Vamp_offset
Gain = Rc / (Ra + Rb)
Voffset worst-case ~2.3mV (+/- ~1A offset)
Vout @ 36A = 2.44V-2.60V

IMVP6 CPU VCore Regulator

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 56 OF 81	



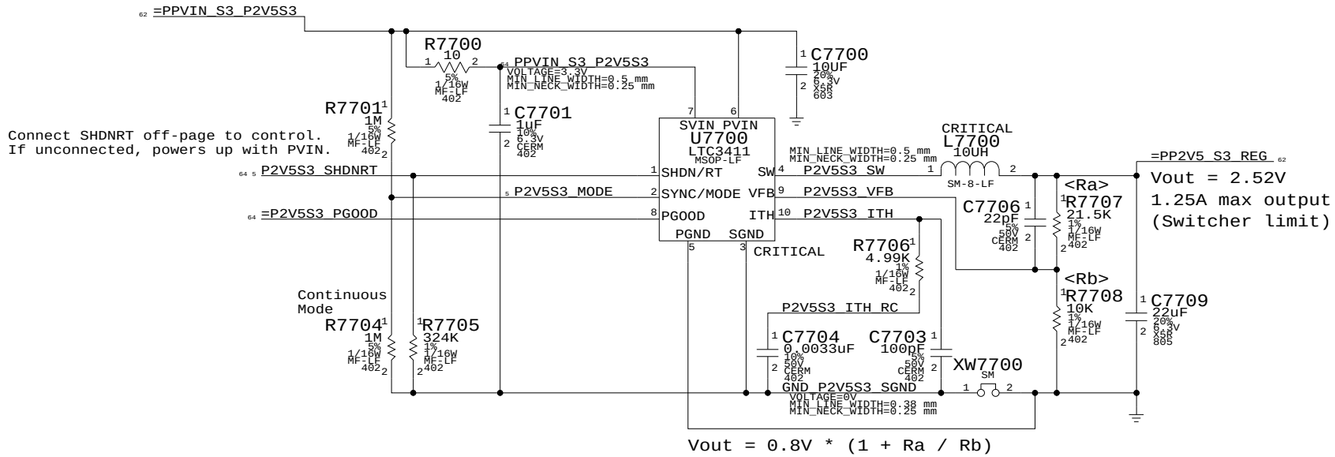
TITLE	5V / 1.5V Power Supply
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

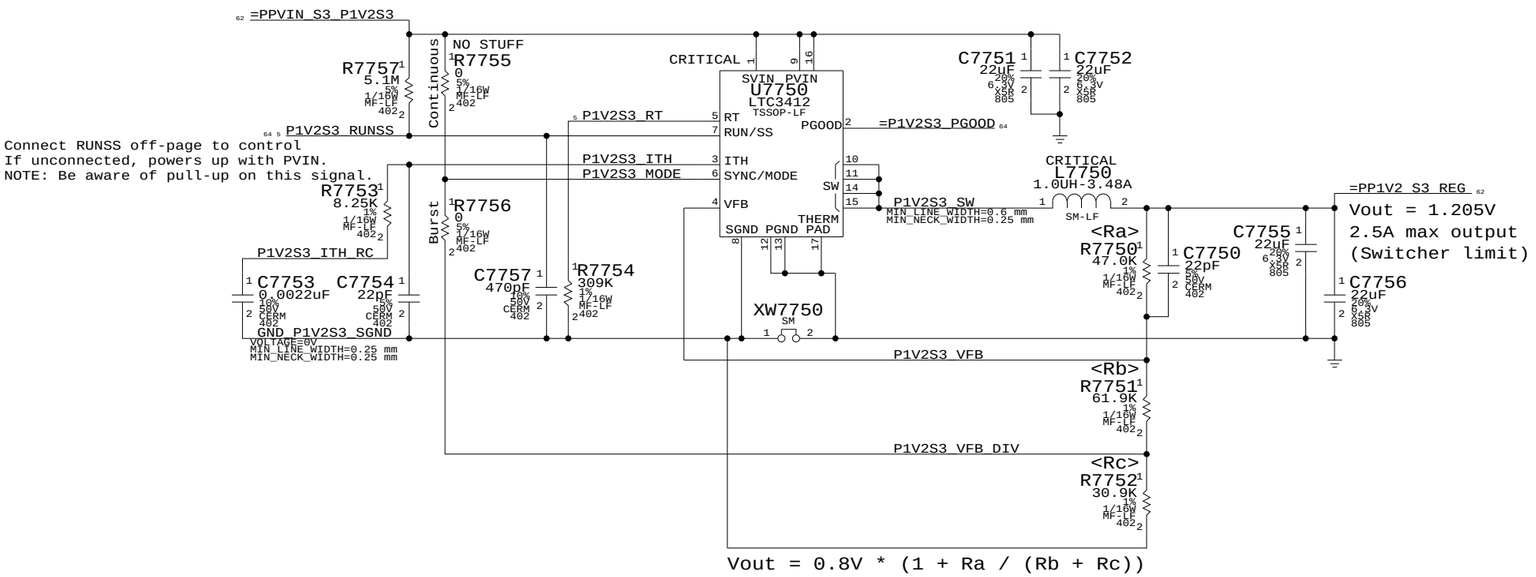
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	57	81

2.5V S3 Regulator



1.2V S3 Regulator



2.5V & 1.2V Regulators

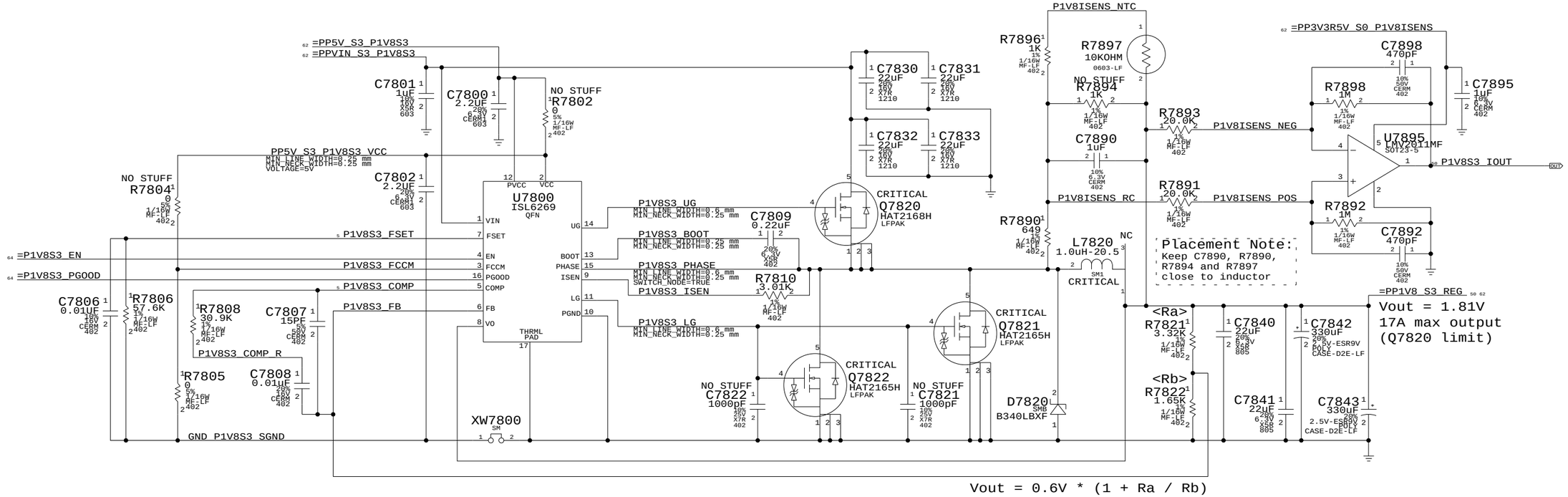
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	58	81

1.8V S3 Current Sense



Vout = 0.6V * (1 + Ra / Rb)

1.8V Supply

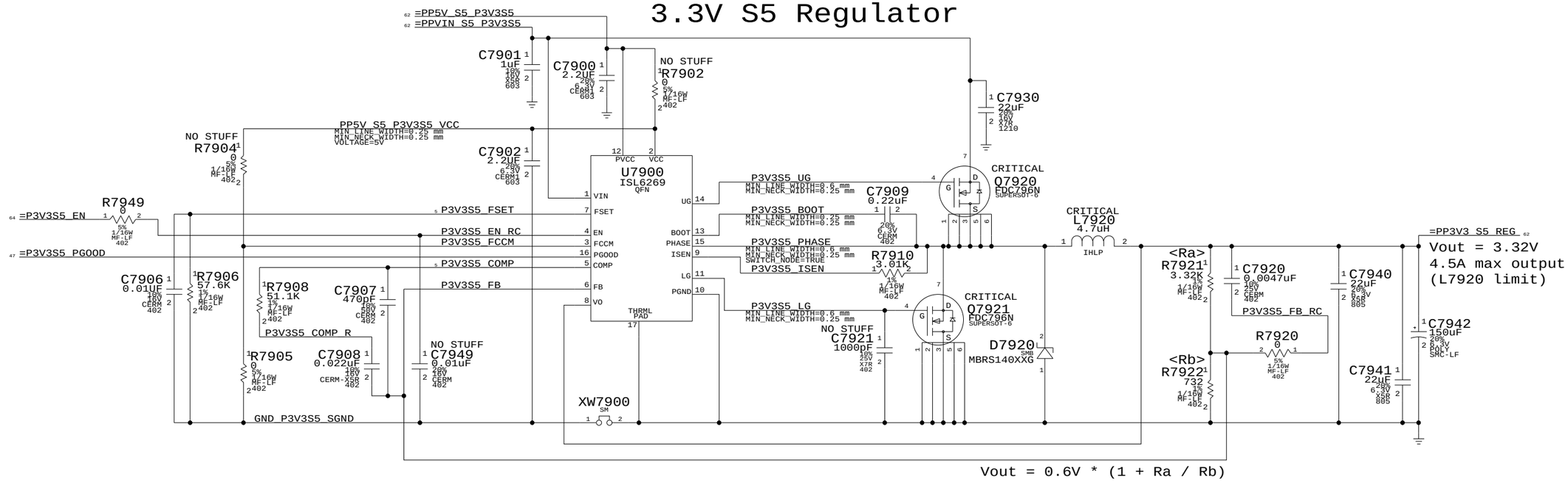
SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

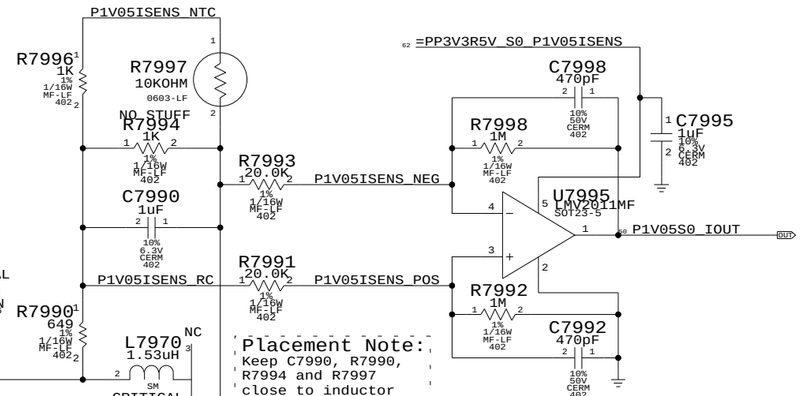
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	59	81

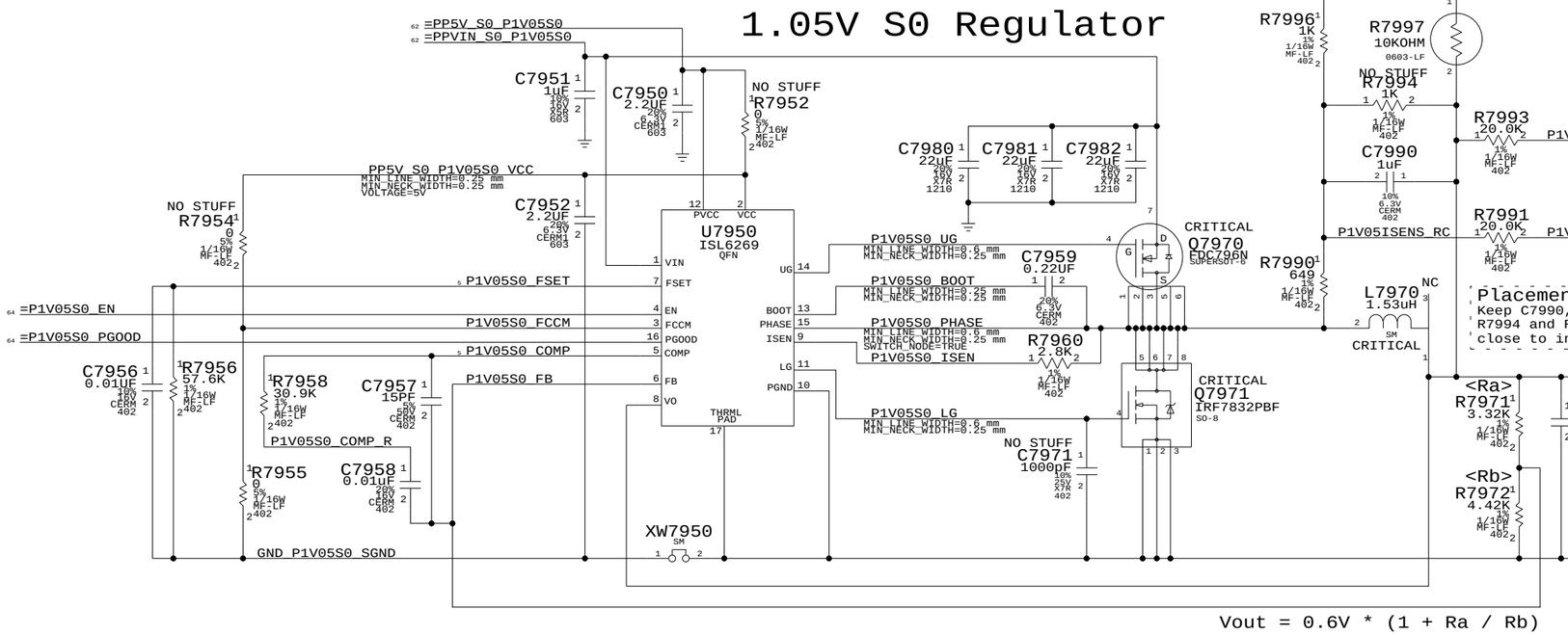
3.3V S5 Regulator



1.05V Current Sense



1.05V S0 Regulator



3.3V / 1.05V Power Supplies	
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)

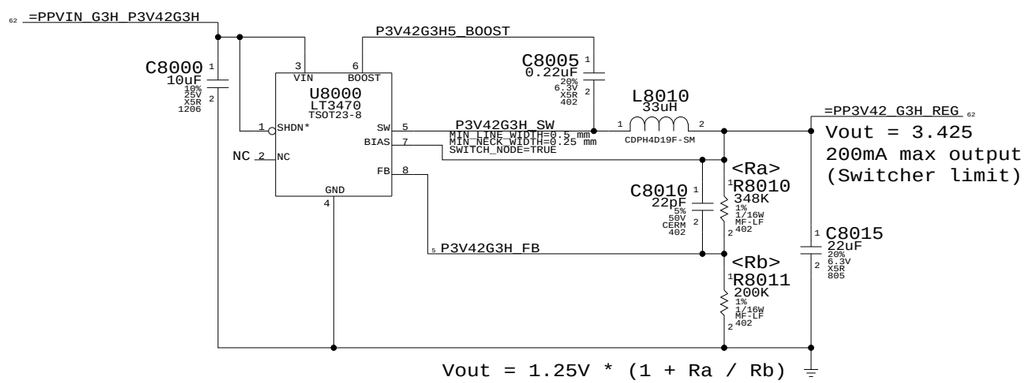
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	60	81

3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



3.3V G3Hot Supply			
SYNC_MASTER=(MASTER)	SYNC_DATE=(MASTER)		
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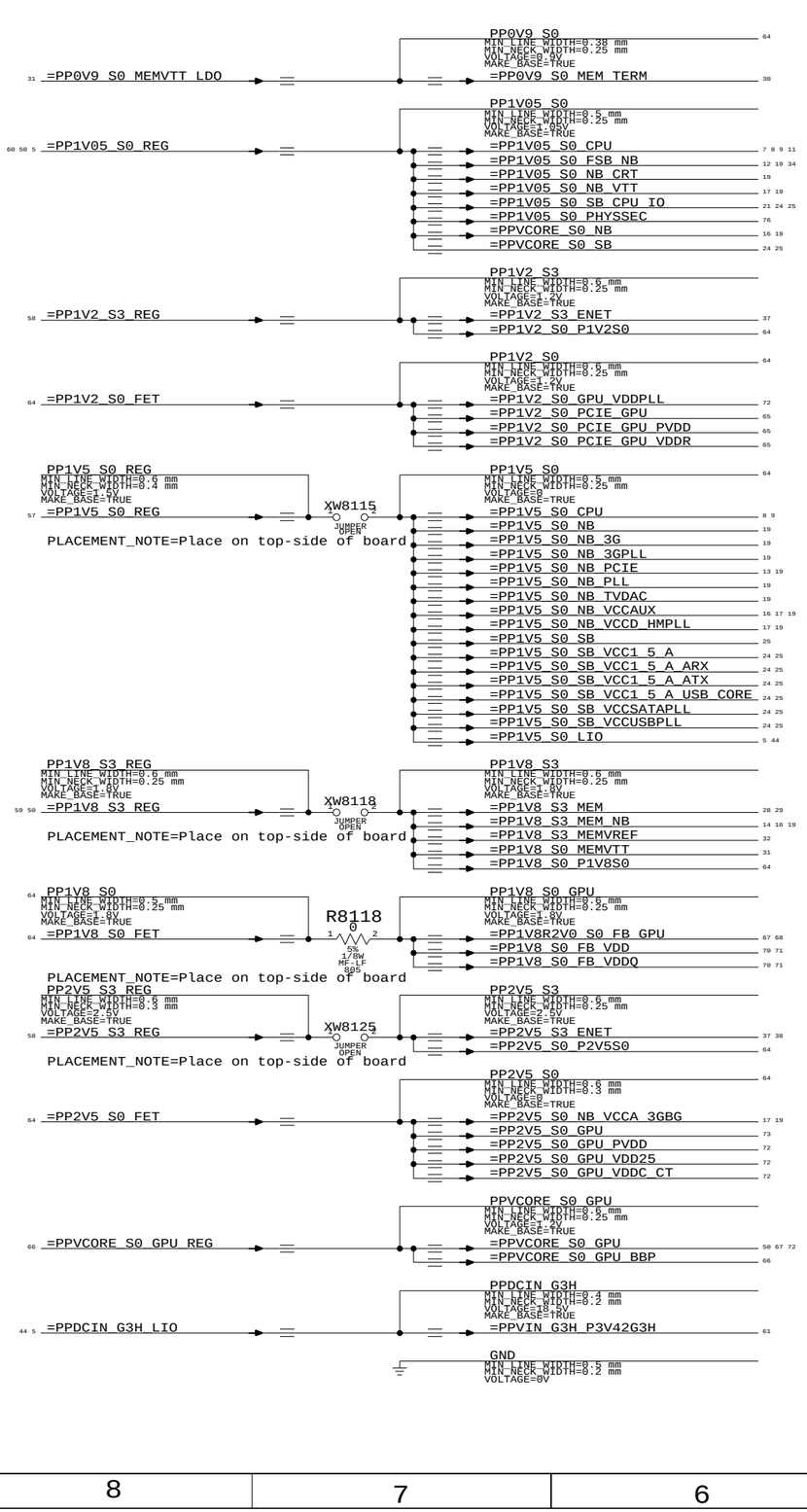
	SCALE NONE	SHT 61 OF 81	



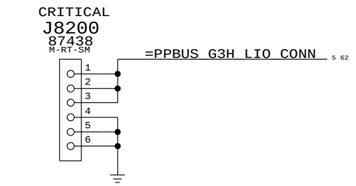
Power Aliases

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

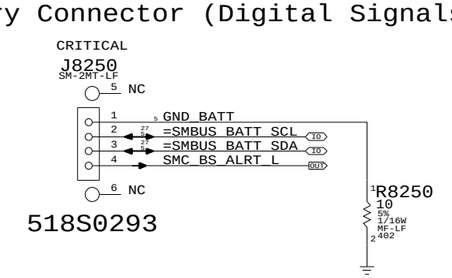
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 62 OF 81	

Left I/O Power Connector



518S0368

Battery Connector (Digital Signals)



518S0293

PBus-In & Battery Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

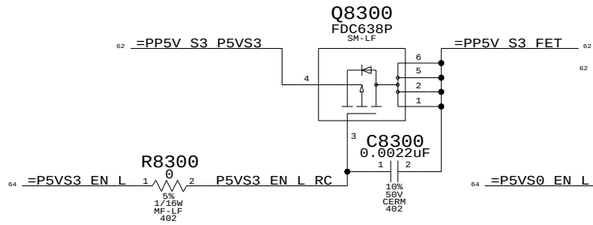
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE NONE

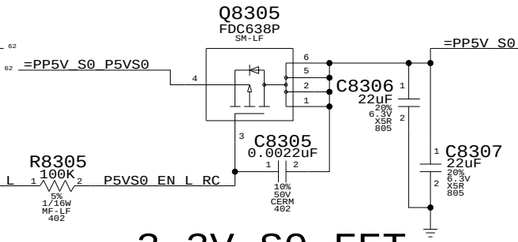
SHT 63 OF 81

State	SMC_PM_G2_ENABLE	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1
Sleep (S3)	1	1	0
Soft-Off (S5)	1	0	0
Battery Off (G3Hot)	0	0	0

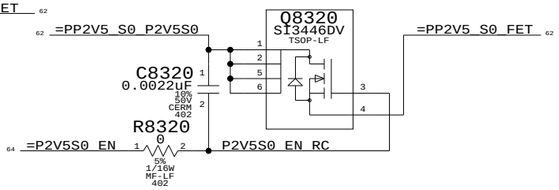
5V S3 FET



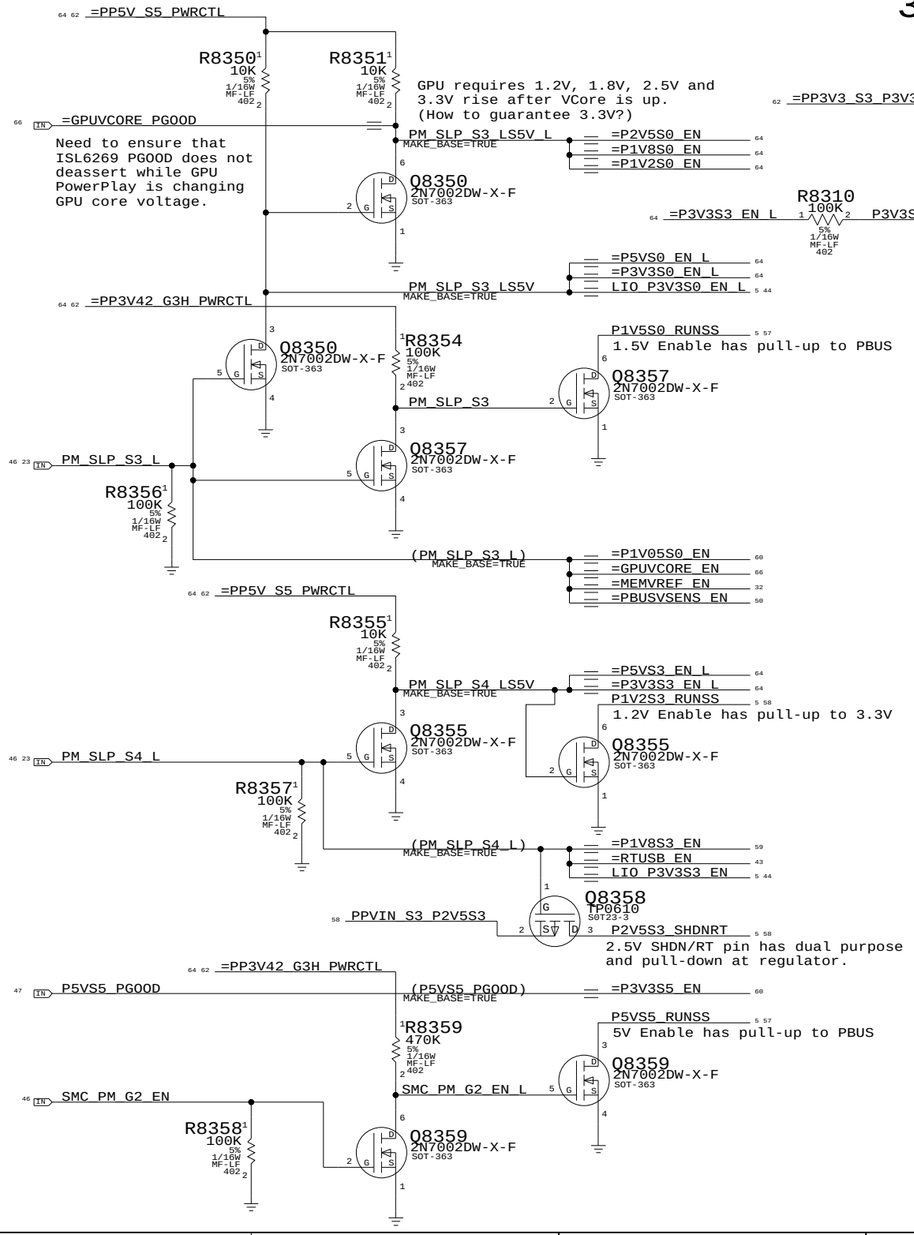
5V S0 FET



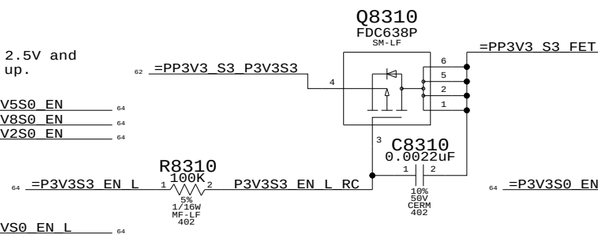
2.5V S0 FET



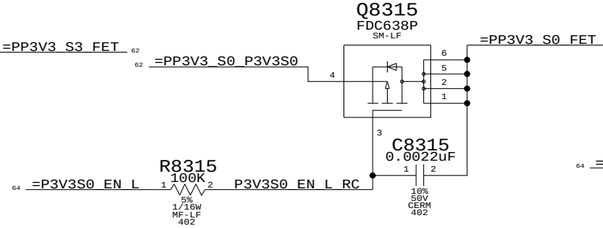
Power Control Signals



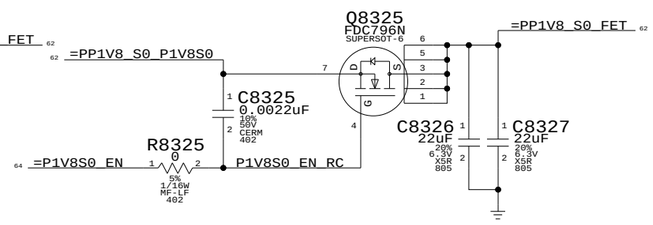
3.3V S3 FET



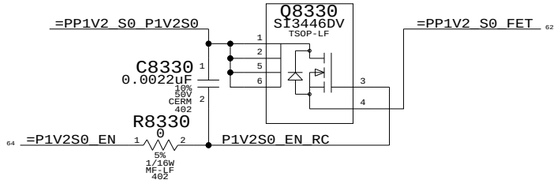
3.3V S0 FET



1.8V S0 FET

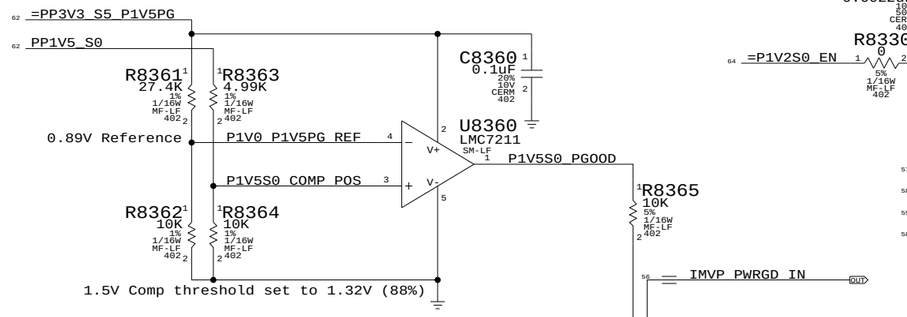


1.2V S0 FET



1.5V / 1.05V PWRGD Circuit

Reports when 1.5V S0 and 1.05V S0 are in regulation



Unused PGOOD Signals

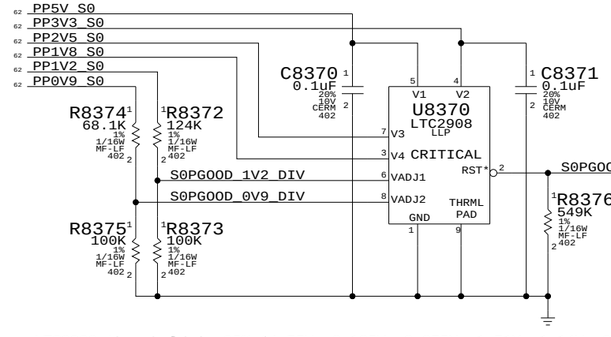
=P5VP1V5_PGOOD	TP_P5V_P1V5_PGOOD
=P2V5S3_PGOOD	TP_P2V5S3_PGOOD
=P1V8S3_PGOOD	TP_P1V8S3_PGOOD
=P1V2S3_PGOOD	TP_P1V2S3_PGOOD

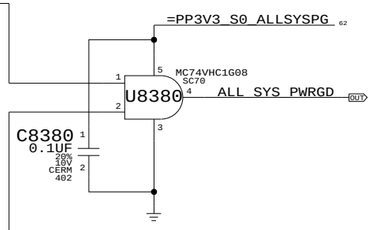
MAKE_BASE=TRUE

These rails are monitored by LTC2908

Other S0 Rails PWRGD Circuit

Reports when 5V S0, 3.3V S0, 2.5V S0, 1.8V S0, 1.2V S0 and 0.9V S0 are in regulation



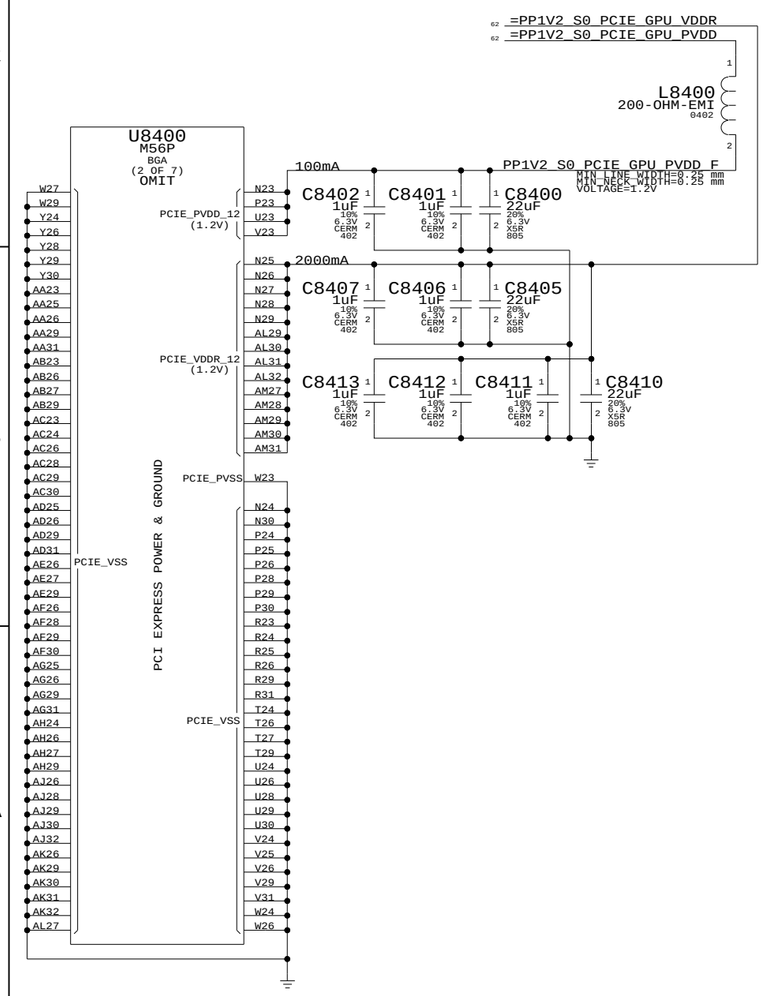


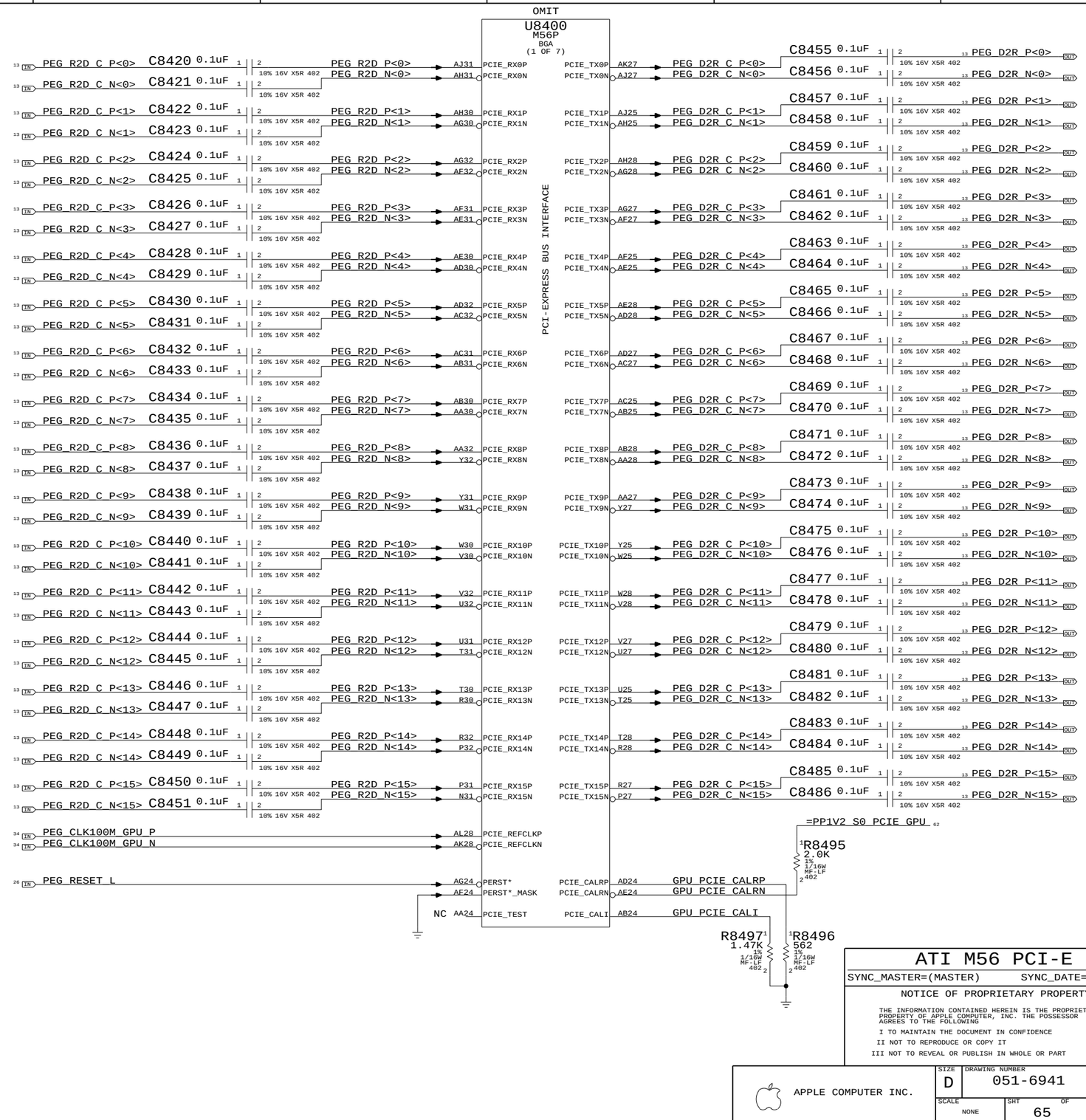
S3/S0 FETs & Power Control

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 64 OF 81	





ATI M56 PCI-E

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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APPLE COMPUTER INC.

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D	051-6941	07001

SCALE	SHT	OF
NONE	65	81

GPU VCore Supply

=PP5V_S0_GPUVCORE
=PPVIN_S0_GPUVCORE
C8501 1uF 10% 16V X5R 603
C8500 2.2UF 20% 6.3V CERM1 603
NO STUFF R8502 0 5% 1/16W MF-LF 402
PP5V_S0_GPUVCORE_VCC
MIN_LINE_WIDTH=0.25 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C8502 2.2UF 20% 6.3V CERM1 603
NO STUFF R8504 0 5% 1/16W MF-LF 402
U8500 ISL6269 QFN
PVCC VCC VIN FSET EN FCCM PGOOD COMP FB VO UG BOOT PHASE ISEN LG PGND THRML PAD
=GPUVCORE_EN
=GPUVCORE_PGOOD
GPUVCORE_FSET
GPUVCORE_FCCM
GPUVCORE_COMP
GPUVCORE_FB
GPUVCORE_UG
GPUVCORE_BOOT
GPUVCORE_PHASE
GPUVCORE_ISEN
GPUVCORE_LG
MIN_LINE_WIDTH=0.6 mm
MIN_NECK_WIDTH=0.25 mm
SWITCH_NODE=TRUE
C8509 0.22UF 20% 6.3V CERM 402
R8510 3.01K 1% 1/16W MF-LF 402
C8530 22uF 20% 16V X7R 1210
C8531 22uF 20% 16V X7R 1210
C8532 22uF 20% 16V X7R 1210
CRITICAL Q8520 HAT2168H LFPAK
CRITICAL L8520 1.0uH-20.5 SM1
R8596 1K 1% 1/10W MF-LF 402
R8597 10KOHM 0603-LF
NO STUFF R8594 1K 1% 1/10W MF-LF 402
C8590 1uF 10% 6.3V CERM 402
R8590 649 1% 1/10W MF-LF 402
GPUISENS_NTC
GPUISENS_RC
GPUISENS_NEG
GPUISENS_POS
=PP3V3R5V_S0_GPUISENS
R8593 20.0K 1% 1/10W MF-LF 402
R8591 20.0K 1% 1/10W MF-LF 402
C8598 470pF 10% 50V CERM 402
R8598 1M 1% 1/16W MF-LF 402
C8595 1uF 10% 6.3V CERM 402
U8595 LMV2011MF SOT23-5
R8592 1M 1% 1/16W MF-LF 402
C8592 470pF 10% 50V CERM 402
GPUVCORE_IOUT
Placement Note:
Keep C8590, R8590, R8594 and R8597 close to inductor
=PPVCORE_S0_GPU_REG
Vout = 1.08V / 1.00V
17A max output
(Q8520 limit)
<Ra> R8521 10K 1% 1/16W MF-LF 402
<Rb> R8522 15.0K 1% 1/16W MF-LF 402
<Rc> R8523 75K 1% 1/16W MF-LF 402
C8520 0.0047uF 10% 25V CERM 402
C8540 22uF 20% 6.3V X5R 805
C8541 22uF 20% 6.3V X5R 805
C8542 330uF 20% 2.5V-ESR9V CASE-D2E-LF
C8543 330uF 20% 2.5V-ESR9V CASE-D2E-LF
GPUVCORE_FB_LOW
R8506 57.6K 1% 1/16W MF-LF 402
C8506 0.01UF 10% 16V CERM 402
R8508 51.1K 1% 1/16W MF-LF 402
C8507 470pF 10% 50V CERM 402
GPUVCORE_COMP_R
R8505 0 5% 1/16W MF-LF 402
C8508 0.022uF 10% 16V CERM-X5R 402
GND_GPUVCORE_SGND
XW8500 SM
CRITICAL Q8521 HAT2165H LFPAK
NO STUFF C8521 1000pF 10% 25V X7R 402
CRITICAL Q8522 HAT2165H LFPAK
NO STUFF C8522 1000pF 10% 25V X7R 402
D8520 B340LBXF

Vout(low) = 0.6V * (1 + Ra / Rb)
Vout(high) = 0.6V * (1 + Ra / Req)
Req = Rb || Rc

=PP3V3_S0_GPU
R8526 100K 5% 1/10W MF-LF 402
R8525 0 5% 1/10W MF-LF 402
GPU_VCORE_HIGH
GPU_VCORE_HIGH_RC
GPU_VCORE_LOW
Q8523 2N7002DW-X-F SOT-363
C8523 0.1uF 10% 16V X5R 402
R8524 10K 5% 1/10W MF-LF 402

Back-Bias Positive Supply

Back-bias positive supply provides VDDC + 0.5V when active.
When inactive, provides VDDC to BBP pins.
NOTE: BBP tracks VDDC based on GPU voltage GPIO.

=PPVCORE_S0_GPU_BBP
Q8575 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
=PPVOUT_S0_GPUBBP_LDO
Vout = 1.58V / 1.50V
180mA max output
(LDO limit)
CRITICAL U8550 FAN2558 SOT23-6-LF VIN PG EN VOUT ADJ GND
=PP3V3_S0_GPUBBP
GPUBB_EN
C8551 2.2uF 20% 6.3V CERM1 603
C8555 0.01UF 10% 16V CERM 402
<Ra> R8555 24.9K 1% 1/16W MF-LF 402
C8556 22uF 20% 6.3V X5R 805
GPUBBP_ADJ
<Rc> R8554 174K 1% 1/16W MF-LF 402
<Rb> R8556 16.2K 1% 1/16W MF-LF 402
C8557 22uF 20% 6.3V X5R 805
GPUBBP_ADJ_LOW
Q8554 2N7002 SOT23-LF
GPU_VCORE_HIGH
Vout(low) = 0.59V * (1 + Ra/Rb)
Vout(high) = 0.59V * (1 + Ra/Req)
Req = Rb || Rc

Pull-up voltage must be high enough to satisfy BBP FET Vgs (where Vs = 1.2V)
=PP5V_S0_GPUBBCTL
FDC796N max Vgs is 3.0V
Vin must be > 4.2V
R8570 100K 5% 1/10W MF-LF 402
Q8570 2N7002 SOT23-LF
GPUBB_EN_L
C8570 0.01uF 10% 16V CERM 402
=PP3V3_S0_GPUBBCTL
GPU_BB_CTL
R8561 0 5% 1/10W MF-LF 402
GPU_GENERICD
GPU_BB_EN
U8560 MC74VHC1G08 SC70
R8560 10K 5% 1/10W MF-LF 402
C8560 1UF 10% 6.3V CERM 402

Back-Bias Negative Supply

Back-bias negative supply provides VSS - 0.5V when active.
When inactive, provides VSS to BBN pins.

=PP3V3_S0_GPUBBN
C8580 10uF 20% 6.3V X5R 603
CRITICAL L8585 15uH SDQ12150-SM
GPUBBN_SW
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
GPUBBN_D
C8585 330pF 10% 50V CERM 402
GPUBBN_D_RC
R8585 10 5% 1/10W MF-LF 603
C8589 22uF 20% 6.3V X5R 805
=PNVOUT_S0_GPUBBN_REG
Vout = -0.50V
150mA max output
(Inductor & IC current limit)
Q8576 FDC796N SUPERSOT-6 CRITICAL
GPUBB_EN_L
Watch FET Vgs, since Vs will be negative
FDC796N min Vgs is 1.0V
U8580 LT3483 TSOT23-6 CRITICAL
SW VIN SHDN* GND FB (GPUBBN_D)
GPUBB_EN
GPUBBN_FB
MIN_LINE_WIDTH=0.38 mm
MIN_NECK_WIDTH=0.25 mm
C8586 220pF 5% 25V CERM 402
<Ra> R8586 49.9K 1% 1/16W MF-LF 402
Vout = -10uA * Ra

GPU (M56) Core Supplies

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

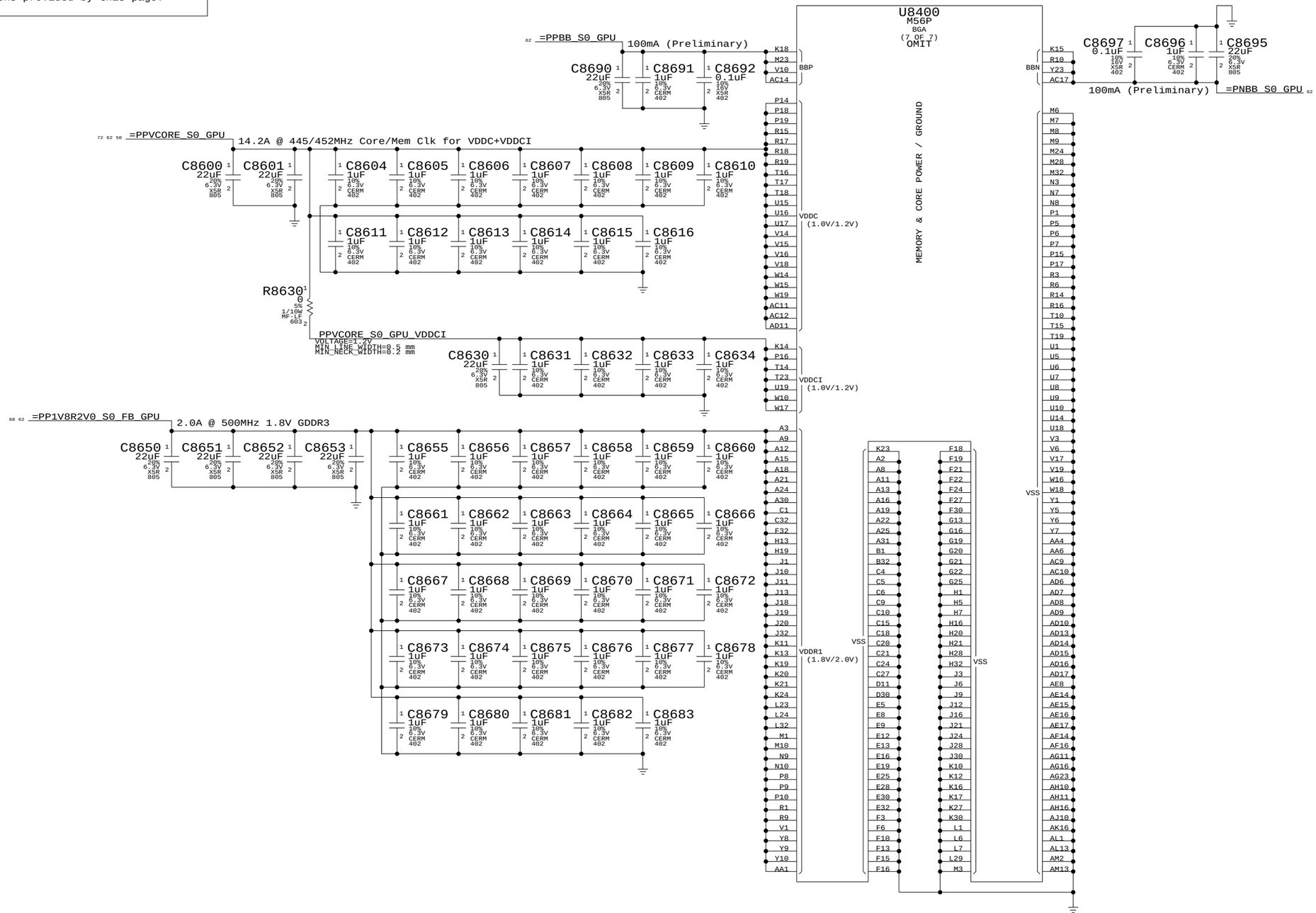
SCALE	SHT	OF
NONE	66	81

Page Notes

Power aliases required by this page:
- =PP1V5_GPU_VDD15
- =PP1VR1V3_GPU_VCORE

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



ATI M56 Core Power

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

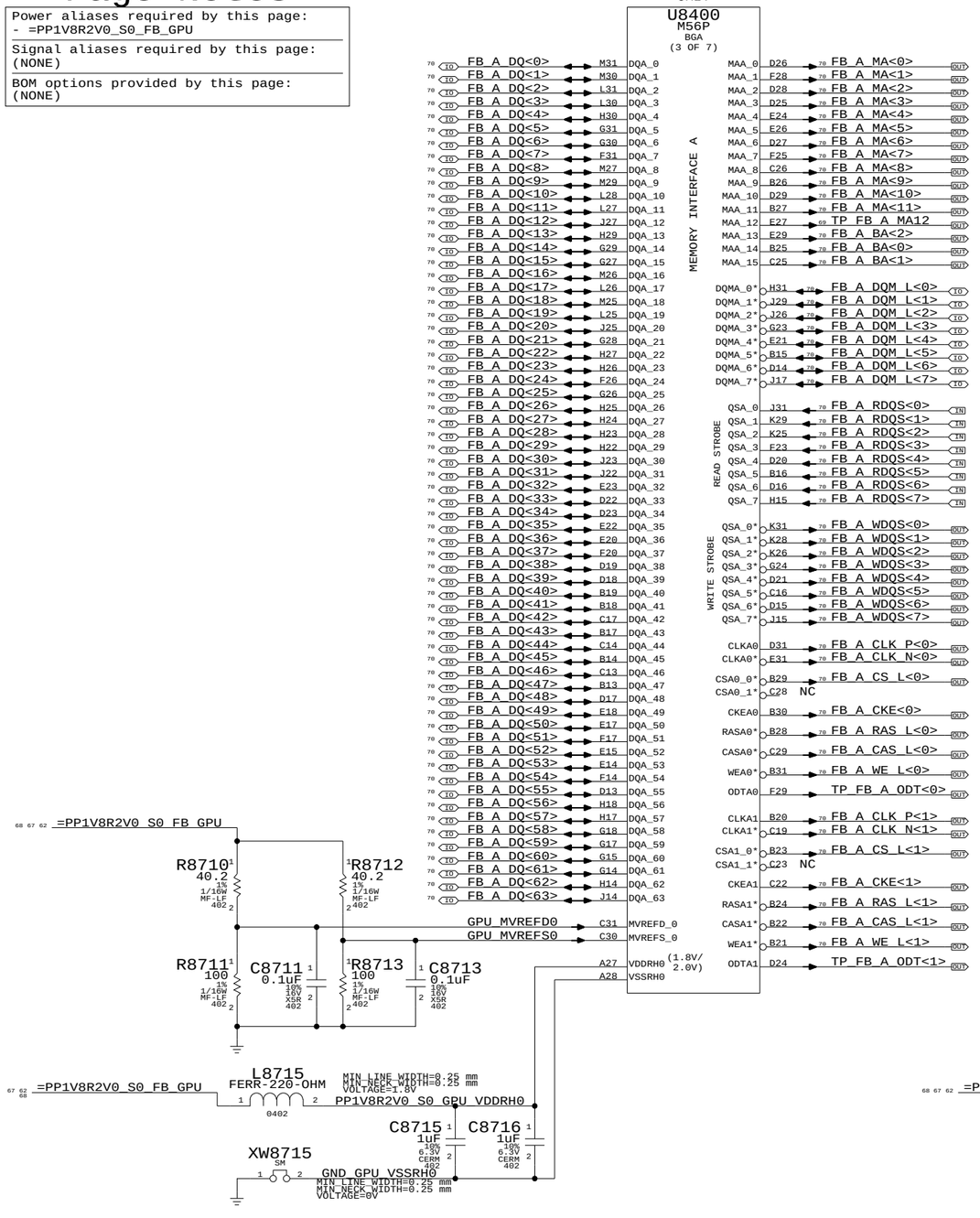
SCALE	SHT	OF
NONE	67	81

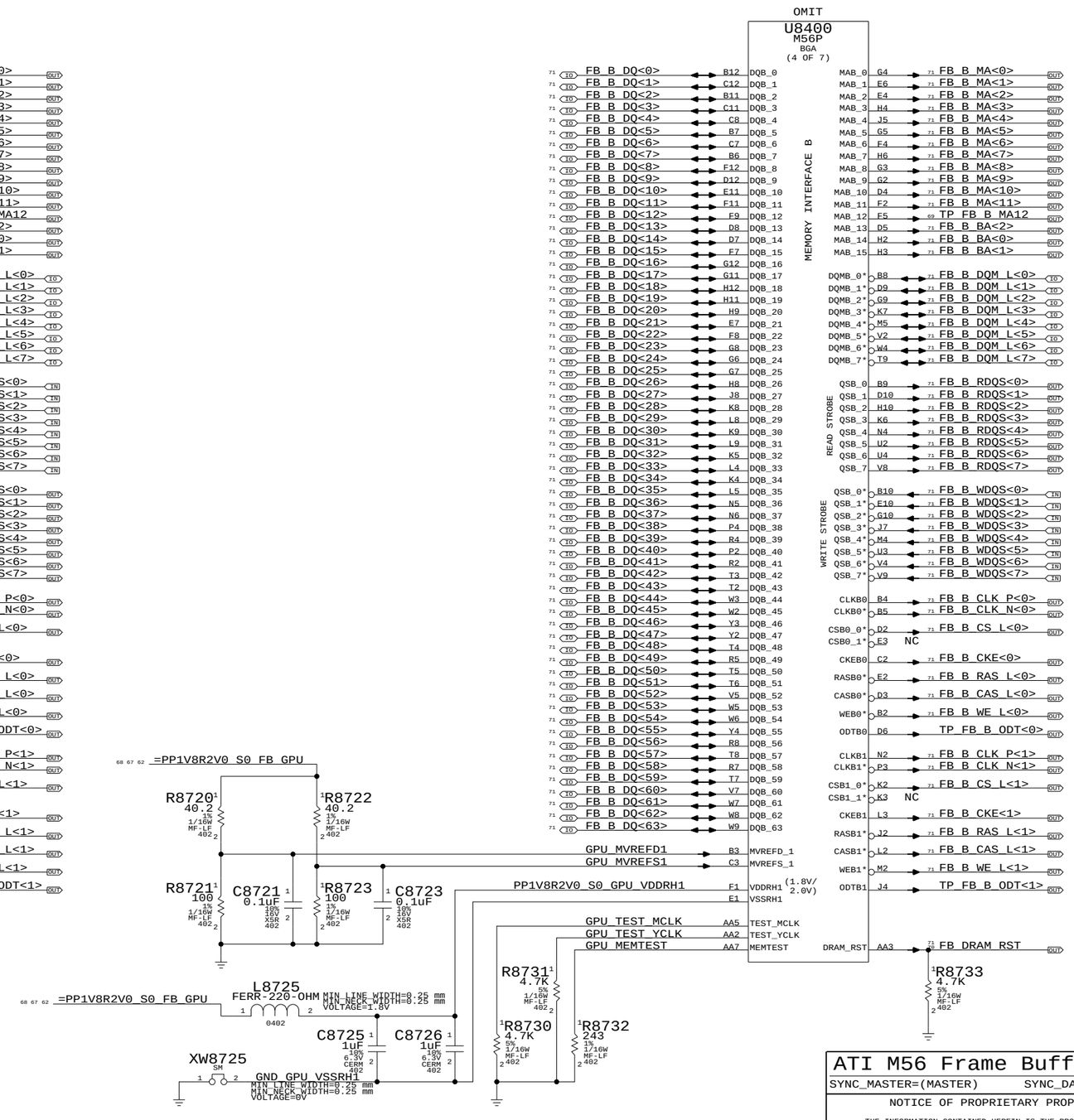
Page Notes

Power aliases required by this page:
- =PP1V8R2V0_S0_FB_GPU

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





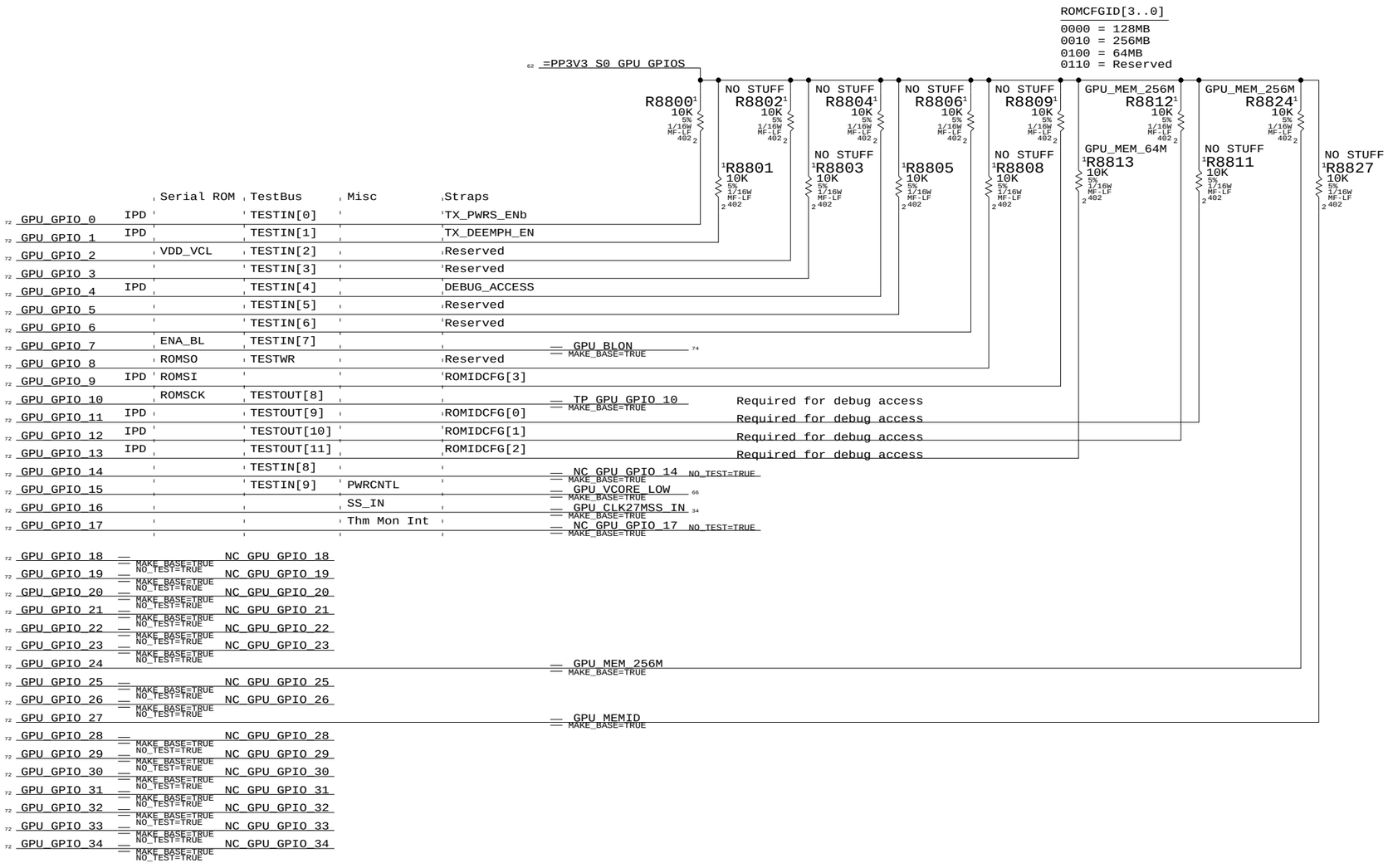
ATI M56 Frame Buffer I/F

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	68	81



GPU Straps

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

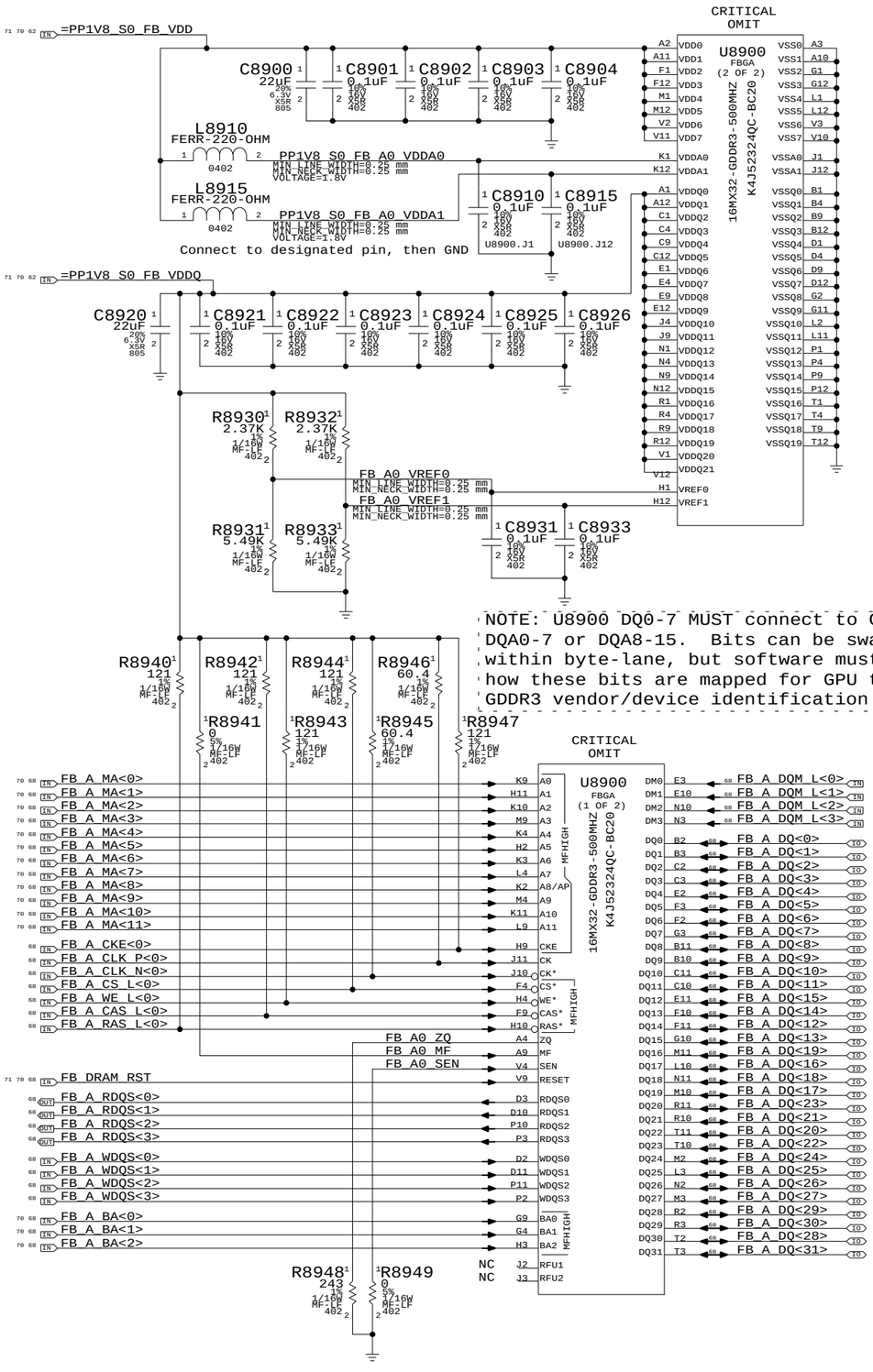
SCALE	SHT	OF
NONE	69	81

Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



GDDR3 Frame Buffer A

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

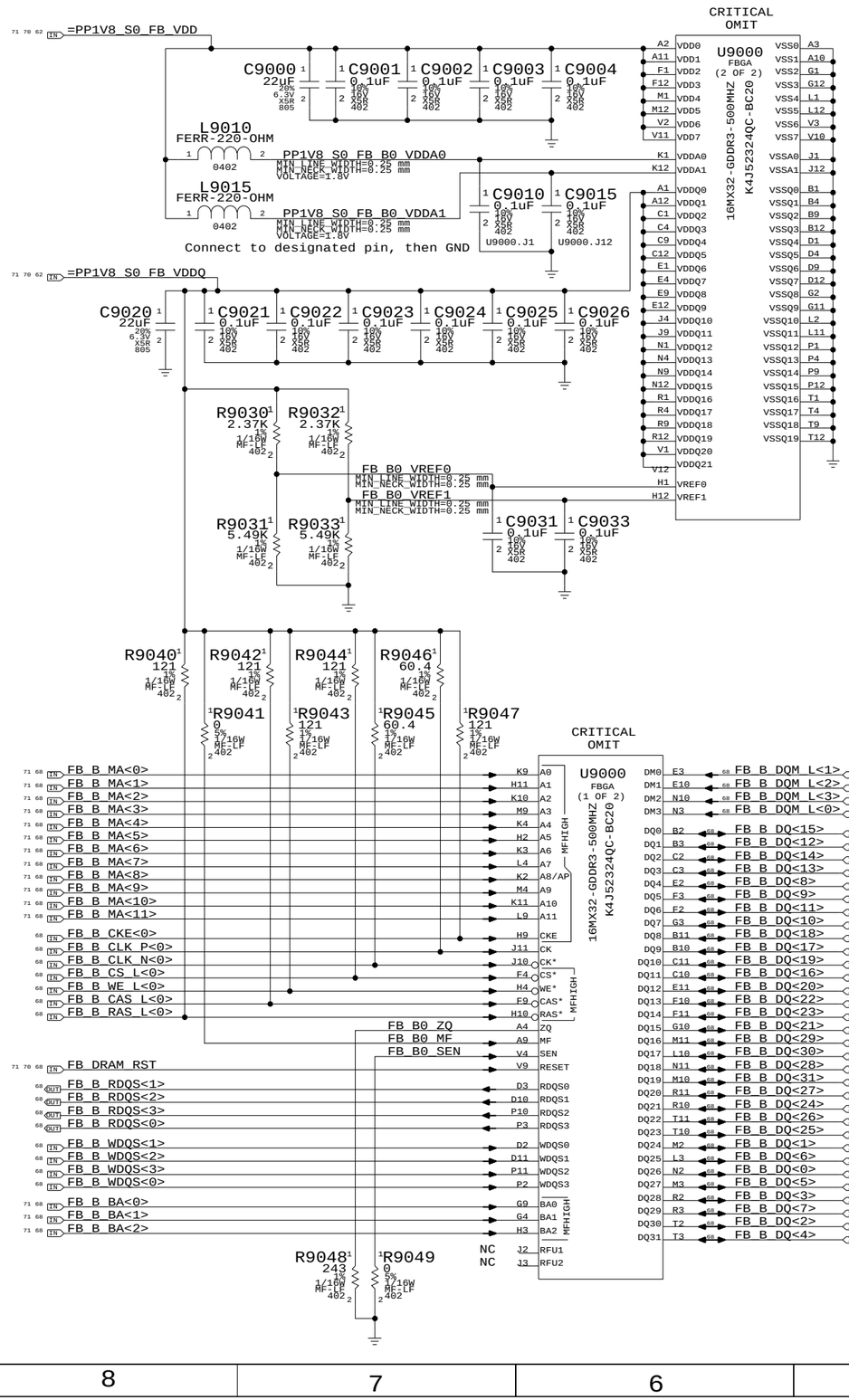
SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 70 OF 81	

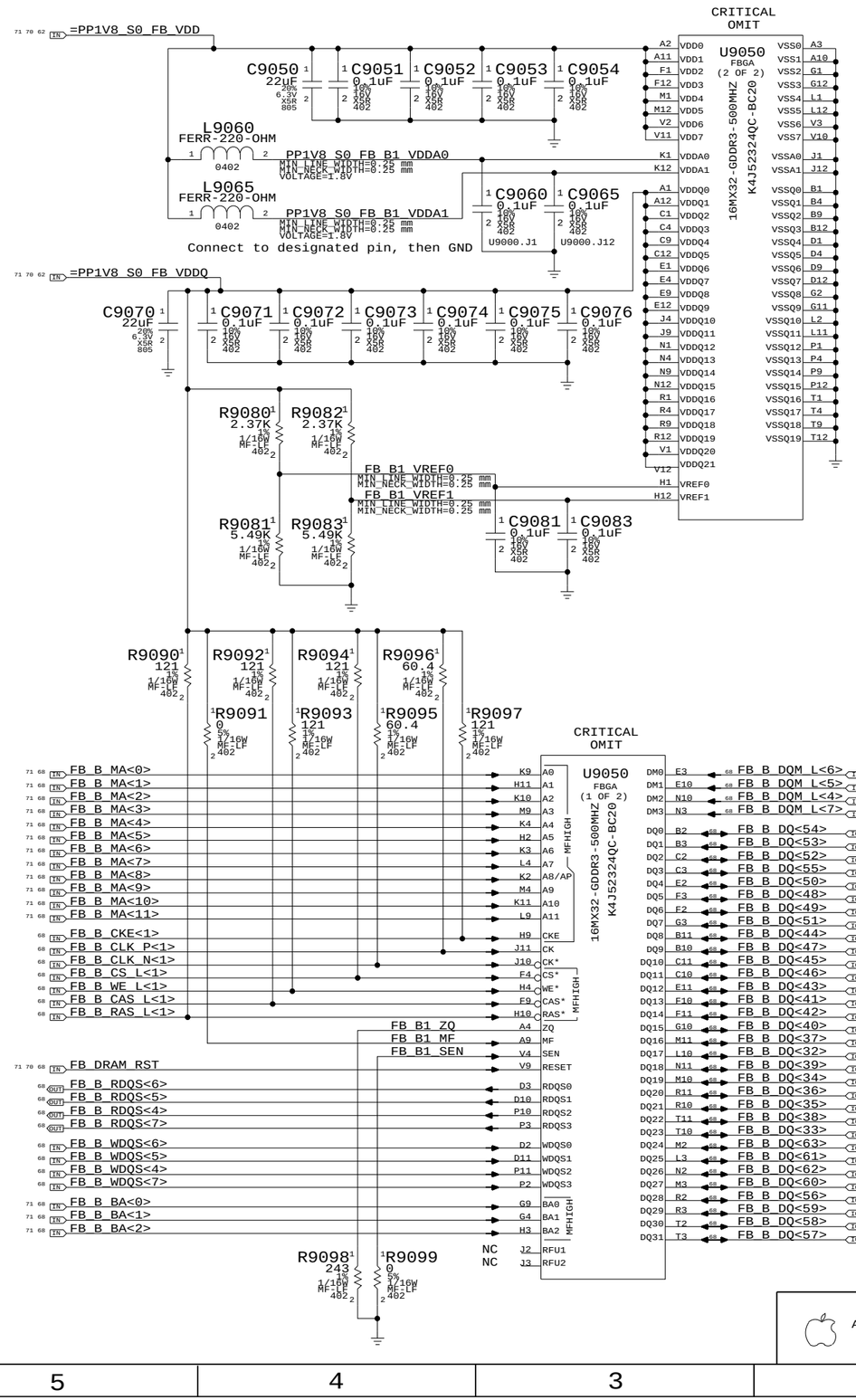
Page Notes

Power aliases required by this page:
- =PP1V8_S0_FB_VDD
- =PP1V8_S0_FB_VDDQ

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)





GDDR3 Frame Buffer B

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

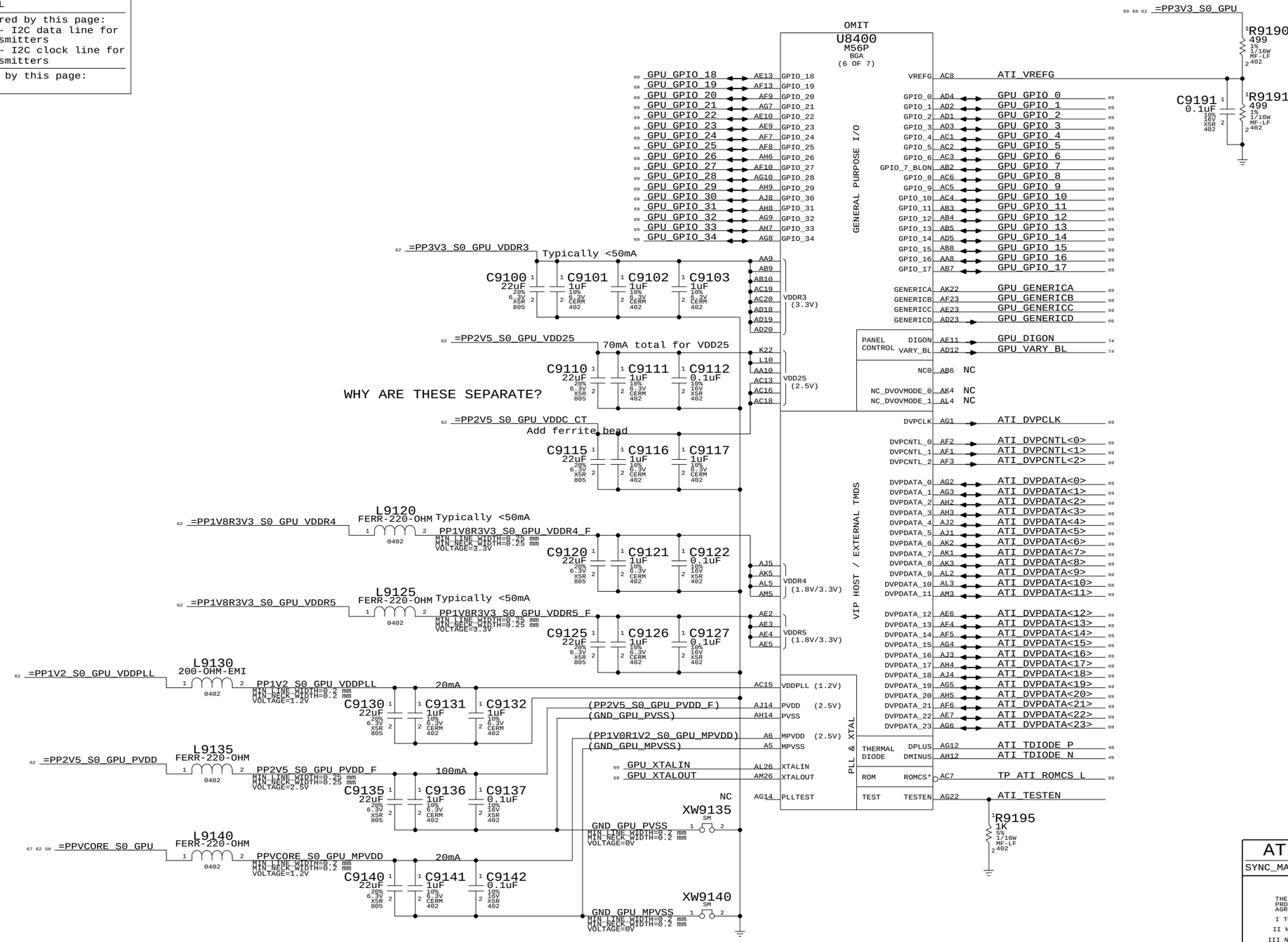
SCALE	SHT	OF
NONE	71	81

Page Notes

Power aliases required by this page:
- =PP3V3_GPU_GPIOS
- =PP2V5_PVDD
- =PP1V8_GPU_LVDS_PLL

Signal aliases required by this page:
- =I2C_GPU_TMDS_SDA - I2C data line for external TMDS transmitters
- =I2C_GPU_TMDS_SCL - I2C clock line for external TMDS transmitters

BOM options provided by this page:
(NONE)



ATI M56 GPIO/DVO/Misc

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001
SCALE: NONE	SHT 72 OF 81	

Page Notes

Power aliases required by this page:
- =PP2V5_S0_GPU
- =PP1V8R2V5_S0_GPU_LVDDR

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)

62 =PP2V5_S0_GPU

Sum of peak currents on this page: 605mA

L9300 FERR-220-OHM 0402 — PP2V5_S0_GPU_TPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9300 SM — GND_GPU_TPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9300 22uF 20% 6.3V X5R 805; C9301 1uF 10% 6.3V CERM 402; C9302 1uF 10% 6.3V CERM 402

L9305 FERR-220-OHM 0402 — PP2V5_S0_GPU_TXVDDR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 150mA peak
XW9305 SM — GND_GPU_TXVSSR — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9305 22uF 20% 6.3V X5R 805; C9306 1uF 10% 6.3V CERM 402; C9307 0.1uF 10% 16V X5R 402

L9310 FERR-220-OHM 0402 — PP2V5_S0_GPU_AVDD — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 65mA peak
XW9310 SM — GND_GPU_AVSSN — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
XW9314 SM — GND_GPU_AVSSQ — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9310 22uF 20% 6.3V X5R 805; C9311 1uF 10% 6.3V CERM 402; C9312 0.1uF 10% 16V X5R 402

L9315 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD1DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
C9315 22uF 20% 6.3V X5R 805; C9316 1uF 10% 6.3V CERM 402; C9317 0.1uF 10% 16V X5R 402

L9320 FERR-220-OHM 0402 — PP2V5_S0_GPU_A2VDD — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 130mA peak
XW9320 SM — GND_GPU_A2VSSN — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9320 22uF 20% 6.3V X5R 805; C9321 1uF 10% 6.3V CERM 402; C9322 0.1uF 10% 16V X5R 402

L9325 FERR-220-OHM 0402 — PP2V5_S0_GPU_VDD2DI — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V
XW9324 SM — GND_GPU_A2VSSQ — MIN_LINE_WIDTH=0.3 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V — 20mA peak
C9325 22uF 20% 6.3V X5R 805; C9326 1uF 10% 6.3V CERM 402; C9327 0.1uF 10% 16V X5R 402

L9330 FERR-220-OHM 0402 — PP2V5_S0_GPU_LPVDD — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=2.5V — 20mA peak
XW9330 SM — GND_GPU_LPVSS — MIN_LINE_WIDTH=0.2 mm, MIN_NECK_WIDTH=0.2 mm, VOLTAGE=0V
C9330 22uF 20% 6.3V X5R 805; C9331 1uF 10% 6.3V CERM 402; C9332 1uF 10% 6.3V CERM 402

L9345 FERR-220-OHM 0402 — PP2V5_S0_GPU_LVDDR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=2.5V — 200mA peak
XW9345 SM — GND_GPU_LVSSR — MIN_LINE_WIDTH=0.25 mm, MIN_NECK_WIDTH=0.25 mm, VOLTAGE=0V
C9340 22uF 20% 6.3V X5R 805; C9345 22uF 20% 6.3V X5R 805; C9341 1uF 10% 6.3V CERM 402; C9342 0.1uF 10% 16V X5R 402; C9346 0.1uF 10% 16V X5R 402; C9347 0.1uF 10% 16V X5R 402

ATI_RSET 73 — R9350 499 1% 1/16W MF-LF 402
ATI_R2SET 73 — R9351 715 1% 1/16W MF-LF 402

OMIT
U8400 M56P BGA (5 OF 7)

INTEGRATED TMDS
- AM8 TPVDD (2.5V)
- AL8 TPVSS
- AJ6, AK6, AL6, AM6 TXVDDR (2.5V)
- AJ7, AK7, AK8, AL7, AM7 TXVSSR

DAC (CRT)
- AL25, AM25 AVDD (2.5V)
- AJ24, AK25 AVSS
- AK23 AVSSQ
- AM23 VDD1DI (2.5V)
- AL23 VSS1DI
- AL22 RSET (73 ATI_RSET)

DAC2 (TV/CRT2)
- AL16, AM16 A2VDD (2.5V)
- AL17, AM17 A2VSS
- NC AL14 NC_A2VDDQ
- AK13 A2VSSQ
- AJ16 VDD2DI (2.5V)
- AJ17 VSS2DI
- AK14 R2SET (73 ATI_R2SET)

LVDS
- AE19 LPVDD (2.5V)
- AE18 LPVSS
- AC21, AC22, AD21, AD22, AE20, AE21, AE22, AF19, AF20 LVDDR (2.5V)
- AF17, AF18, AF21, AF22, AG17, AG19, AH17, AH19, AJ19, AK17 LVSSR

MONITOR IDENTIFICATION
- AF11 HPD1 (75 IN GPU_HPD)

TMDS outputs:
- TXCP AM9 — GPU_TMDS_CLK_P
- TXCM AL9 — GPU_TMDS_CLK_N
- TX0P AL10 — GPU_TMDS_DATA_P<0>
- TX0M AK10 — GPU_TMDS_DATA_N<0>
- TX1P AM11 — GPU_TMDS_DATA_P<1>
- TX1M AL11 — GPU_TMDS_DATA_N<1>
- TX2P AM12 — GPU_TMDS_DATA_P<2>
- TX2M AL12 — GPU_TMDS_DATA_N<2>
- TX3P AJ9 — GPU_TMDS_DATA_P<3>
- TX3M AK9 — GPU_TMDS_DATA_N<3>
- TX4P AJ11 — GPU_TMDS_DATA_P<4>
- TX4M AK11 — GPU_TMDS_DATA_N<4>
- TX5P AJ12 — GPU_TMDS_DATA_P<5>
- TX5M AK12 — GPU_TMDS_DATA_N<5>

DAC (CRT) outputs:
- R AK24 — GPU_VGA_R
- G AM24 — GPU_VGA_G
- B AL24 — GPU_VGA_B
- HSYNC AJ23 — GPU_VGA_HSYNC
- VSYNC AJ22 — GPU_VGA_VSYNC

DAC2 (TV/CRT2) outputs:
- R2 AK15 — GPU_R2
- G2 AM15 — GPU_G2
- B2 AL15 — GPU_B2
- H2SYNC AE15 — GPU_H2SYNC
- V2SYNC AG15 — GPU_V2SYNC
- Y AJ15 — GPU_TV_Y
- C AJ13 — GPU_TV_C
- COMP AH15 — GPU_TV_COMP

LVDS outputs:
- TXCLK_UP AJ21 — GPU_LVDS_U_CLK_P
- TXCLK_UN AK21 — GPU_LVDS_U_CLK_N
- TXOUT_U0P AG18 — GPU_LVDS_U_DATA_P<0>
- TXOUT_U0N AH18 — GPU_LVDS_U_DATA_N<0>
- TXOUT_U1P AK20 — GPU_LVDS_U_DATA_P<1>
- TXOUT_U1N AJ20 — GPU_LVDS_U_DATA_N<1>
- TXOUT_U2P AG20 — GPU_LVDS_U_DATA_P<2>
- TXOUT_U2N AH20 — GPU_LVDS_U_DATA_N<2>
- TXOUT_U3P AH21 — GPU_LVDS_U_DATA_P<3>
- TXOUT_U3N AG21 — GPU_LVDS_U_DATA_N<3>
- TXCLK_LP AM18 — GPU_LVDS_L_CLK_P
- TXCLK_LN AL18 — GPU_LVDS_L_CLK_N
- TXOUT_L0P AL19 — GPU_LVDS_L_DATA_P<0>
- TXOUT_L0N AK19 — GPU_LVDS_L_DATA_N<0>
- TXOUT_L1P AM20 — GPU_LVDS_L_DATA_P<1>
- TXOUT_L1N AL20 — GPU_LVDS_L_DATA_N<1>
- TXOUT_L2P AM21 — GPU_LVDS_L_DATA_P<2>
- TXOUT_L2N AL21 — GPU_LVDS_L_DATA_N<2>
- TXOUT_L3P AJ18 — GPU_LVDS_L_DATA_P<3>
- TXOUT_L3N AK18 — GPU_LVDS_L_DATA_N<3>

MONITOR IDENTIFICATION (TO):
- DDC1CLK AH23 — GPU_DDC_A_CLK
- DDC1DATA AH22 — GPU_DDC_A_DATA
- DDC2CLK AG13 — GPU_DDC_B_CLK
- DDC2DATA AH13 — GPU_DDC_B_DATA
- DDC3CLK AF12 — GPU_DDC_C_CLK
- DDC3DATA AE12 — GPU_DDC_C_DATA

Composite/S-Video	VGA	Component
Y	G	Y
C	R	Pr
Comp	B	Pb

ATI M56 Video Interfaces

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

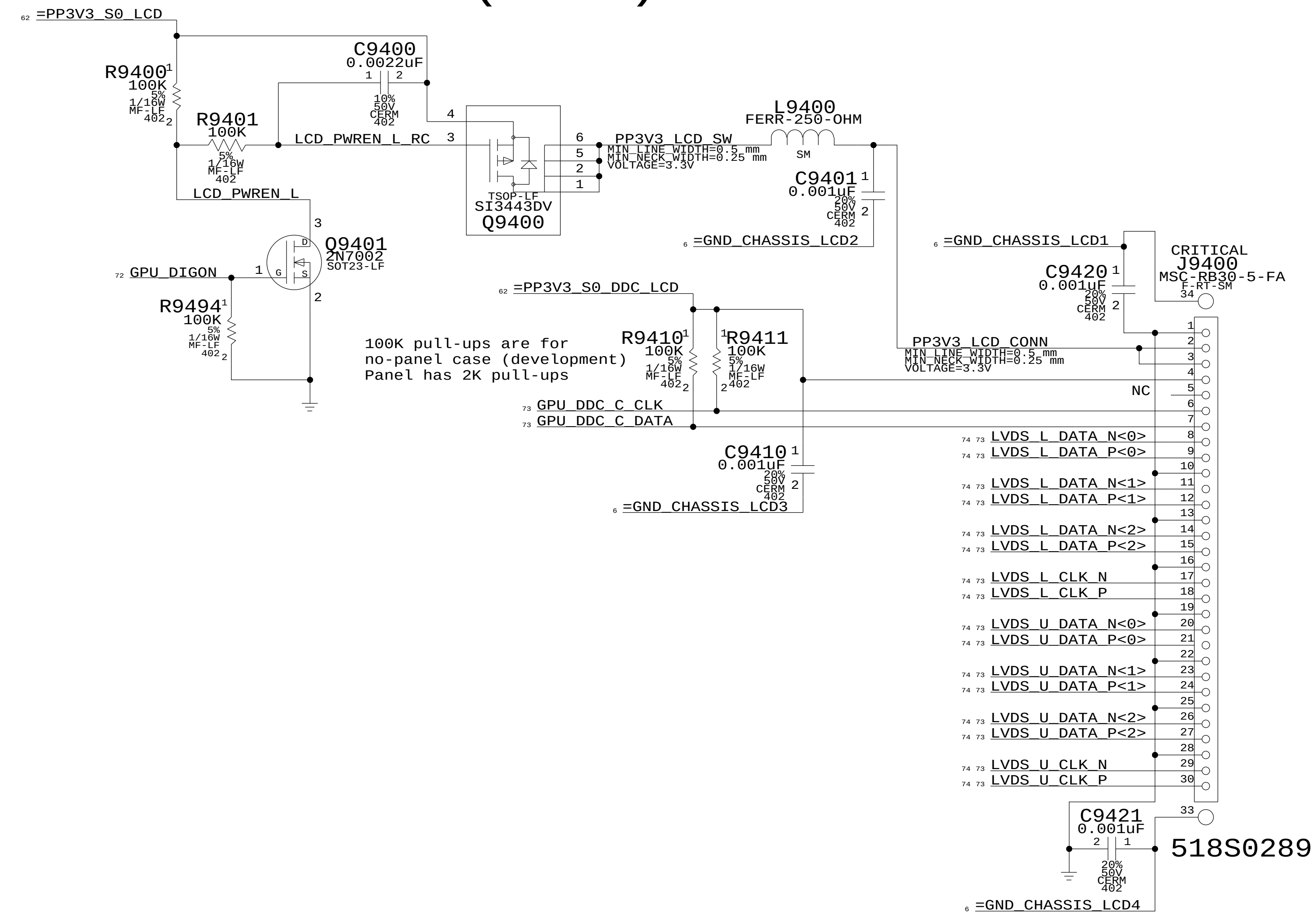
APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE: NONE SHT 73 OF 81

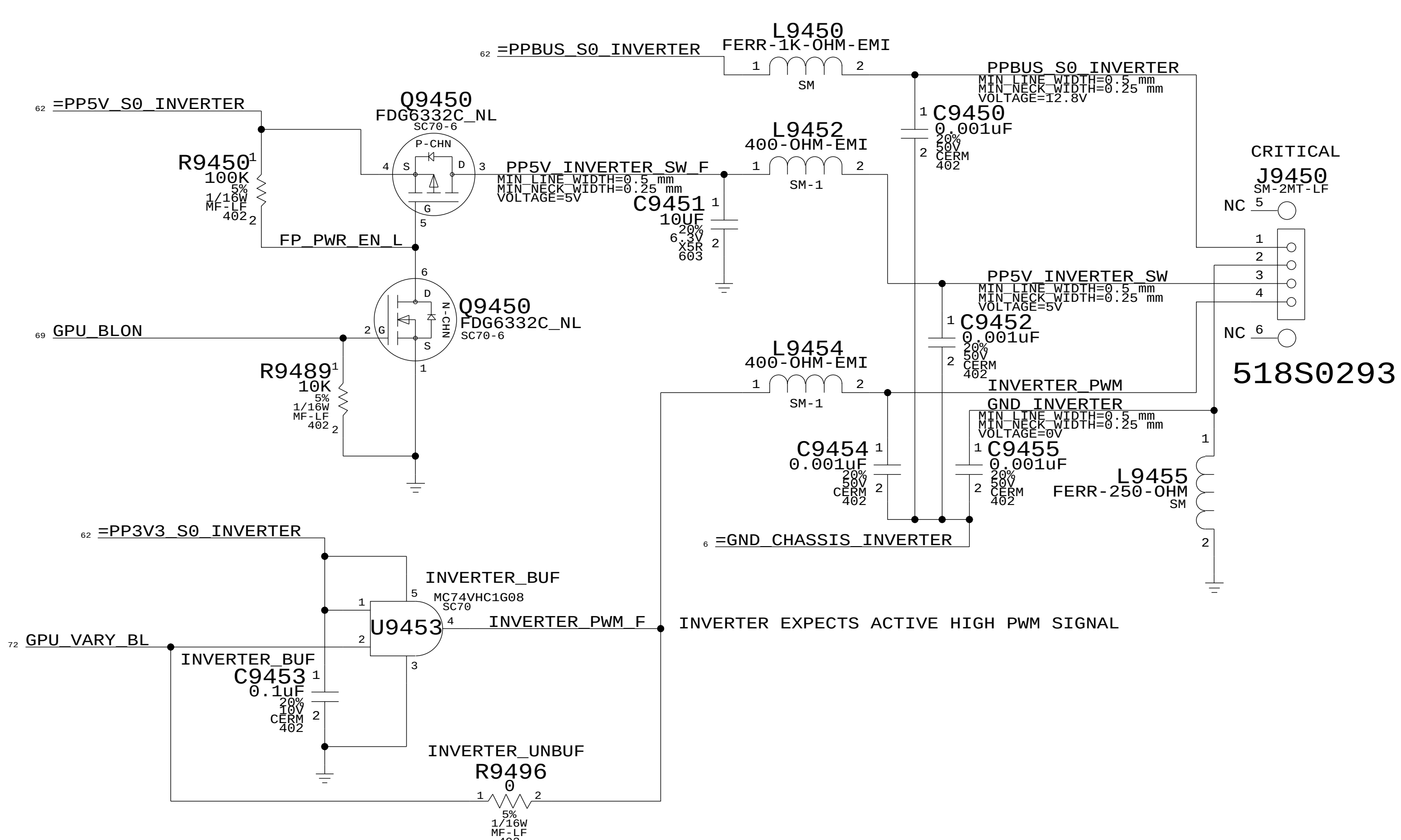
ELECTRICAL_CONSTRAINT_SET	NET_TYPE SPACING	PHYSICAL		
	VGA	VGA	GPU_R2	73 75
	VGA	VGA	GPU_G2	73 75
	VGA	VGA	GPU_B2	73 75
	LVDS	LVDS	LVDS_U_CLK_P	73 74
	LVDS	LVDS	LVDS_U_CLK_N	73 74
	LVDS	LVDS	LVDS_U_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_U_DATA_N<2..0>	73 74
	LVDS	LVDS	LVDS_L_CLK_P	73 74
	LVDS	LVDS	LVDS_L_CLK_N	73 74
	LVDS	LVDS	LVDS_L_DATA_P<2..0>	73 74
	LVDS	LVDS	LVDS_L_DATA_N<2..0>	73 74
	TMDS	TMDS	TMDS_CLK_P	73 75 81
	TMDS	TMDS	TMDS_CLK_N	73 75 81
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 75 81
	TMDS	TMDS	TMDS_DATA_P<2..0>	73 75 81
	TMDS	TMDS	TMDS_DATA_N<2..0>	73 75 81

LCD (LVDS) INTERFACE



=PP3V3_S0_LCD
R9400 100K 5% 1/16W MF-LF 402
C9400 0.0022uF 10% 50V CERM 402
R9401 100K 5% 1/16W MF-LF 402
LCD_PWREN_L_RC
LCD_PWREN_L
TSOP-LF SI3443DV Q9400
PP3V3_LCD_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
L9400 FERR-250-OHM SM
C9401 0.001uF 20% 50V CERM 402
=GND_CHASSIS_LCD2
Q9401 2N7002 SOT23-LF
GPU_DIGON
R9494 100K 5% 1/16W MF-LF 402
=PP3V3_S0_DDC_LCD
100K pull-ups are for
no-panel case (development)
Panel has 2K pull-ups
R9410 100K 5% 1/16W MF-LF 402
R9411 100K 5% 1/16W MF-LF 402
GPU_DDC_C_CLK
GPU_DDC_C_DATA
C9410 0.001uF 20% 50V CERM 402
=GND_CHASSIS_LCD3
=GND_CHASSIS_LCD1
C9420 0.001uF 20% 50V CERM 402
CRITICAL
J9400
MSC-RB30-5-FA
F-RT-SM
PP3V3_LCD_CONN
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=3.3V
NC
LVDS_L_DATA_N<0>
LVDS_L_DATA_P<0>
LVDS_L_DATA_N<1>
LVDS_L_DATA_P<1>
LVDS_L_DATA_N<2>
LVDS_L_DATA_P<2>
LVDS_L_CLK_N
LVDS_L_CLK_P
LVDS_U_DATA_N<0>
LVDS_U_DATA_P<0>
LVDS_U_DATA_N<1>
LVDS_U_DATA_P<1>
LVDS_U_DATA_N<2>
LVDS_U_DATA_P<2>
LVDS_U_CLK_N
LVDS_U_CLK_P
C9421 0.001uF 20% 50V CERM 402
518S0289
=GND_CHASSIS_LCD4

INVERTER INTERFACE



=PPBUS_S0_INVERTER
L9450 FERR-1K-OHM-EMI SM
PPBUS_S0_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=12.8V
C9450 0.001uF 20% 50V CERM 402
=PP5V_S0_INVERTER
Q9450 FDG6332C_NL SC70-6
R9450 100K 5% 1/16W MF-LF 402
PP5V_INVERTER_SW_F
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
L9452 400-OHM-EMI SM-1
C9451 10UF 20% 6.3V X5R 603
FP_PWR_EN_L
GPU_BLON
Q9450 FDG6332C_NL SC70-6
R9489 10K 5% 1/16W MF-LF 402
CRITICAL
J9450
SM-2MT-LF
NC
PP5V_INVERTER_SW
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=5V
C9452 0.001uF 20% 50V CERM 402
518S0293
L9454 400-OHM-EMI SM-1
INVERTER_PWM
GND_INVERTER
MIN_LINE_WIDTH=0.5 mm
MIN_NECK_WIDTH=0.25 mm
VOLTAGE=0V
C9454 0.001uF 20% 50V CERM 402
C9455 0.001uF 20% 50V CERM 402
L9455 FERR-250-OHM SM
=GND_CHASSIS_INVERTER
=PP3V3_S0_INVERTER
INVERTER_BUF
MC74VHC1G08 SC70
U9453
GPU_VARY_BL
INVERTER_PWM_F
INVERTER EXPECTS ACTIVE HIGH PWM SIGNAL
INVERTER_BUF
C9453 0.1uF 20% 10V CERM 402
INVERTER_UNBUF
R9496 0 5% 1/16W MF-LF 402

Internal Display Connectors

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

NOTICE OF PROPRIETARY PROPERTY

APPLE COMPUTER INC.

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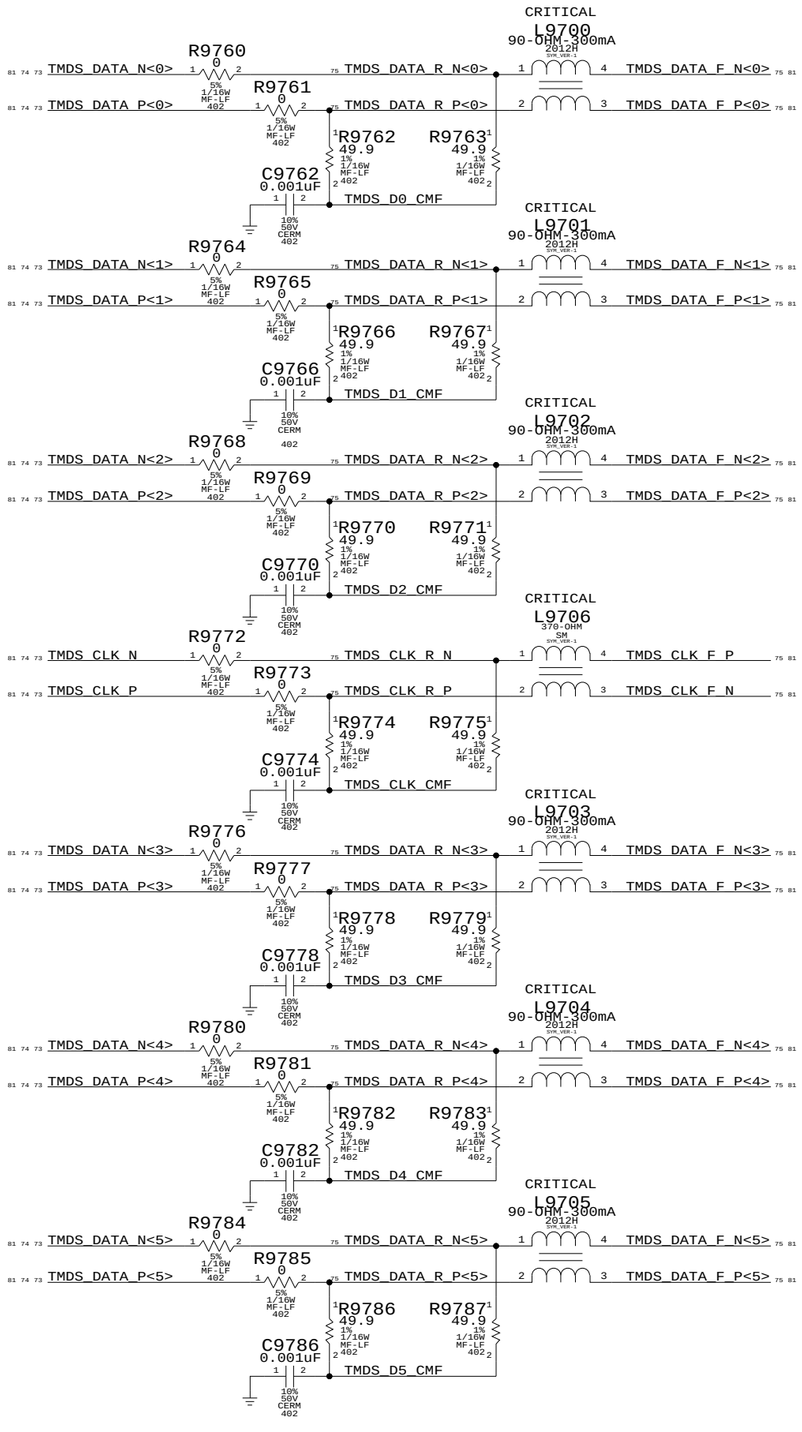
D	051-6941	07001

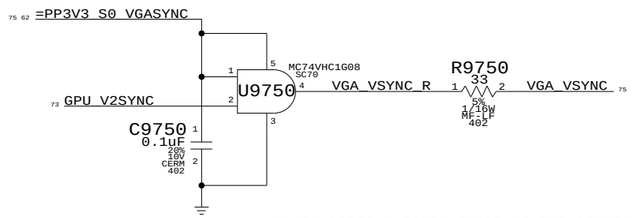
SCALE	SHT	OF
NONE	74	81

TMDS Filtering

Place series R's close to GPU, other parts near connector.

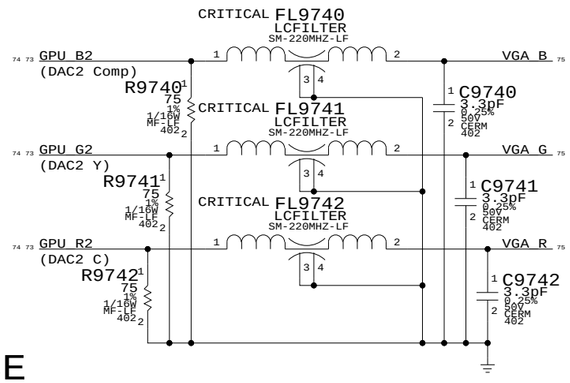


VGA SYNC BUFFERS



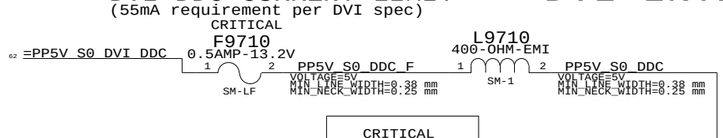
PLACE R9750 & R9751 CLOSE TO DVI CONNECTOR

ANALOG FILTERING
PLACE CLOSE TO CONNECTOR

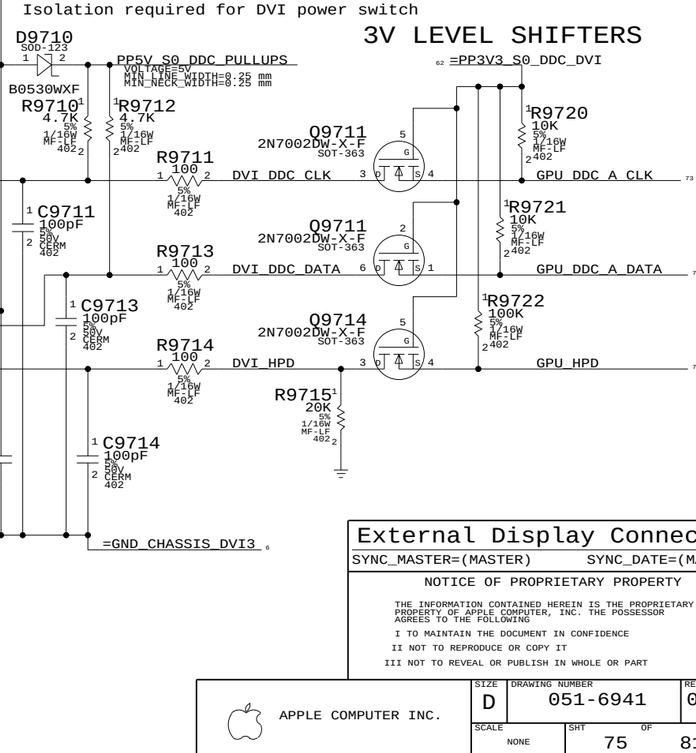


DVI INTERFACE

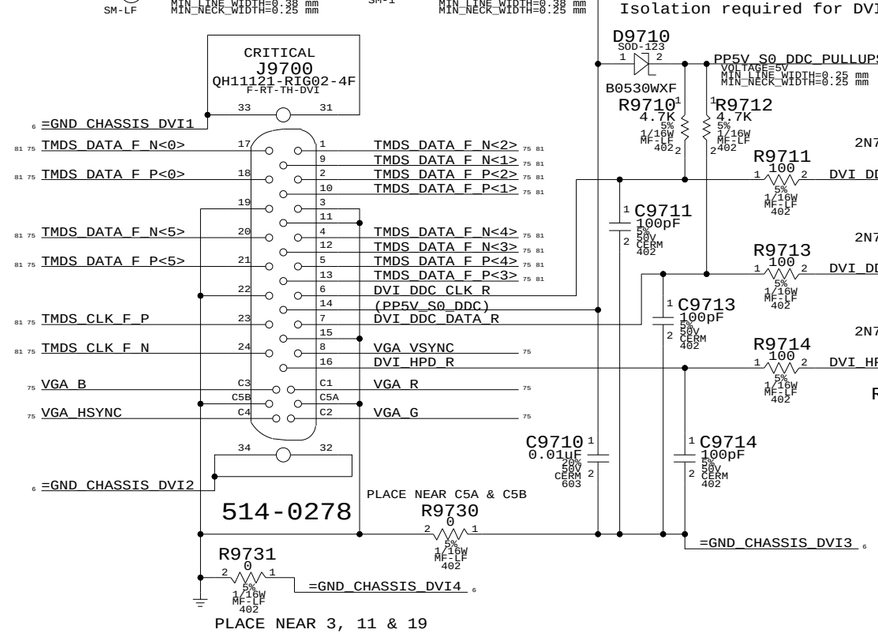
DVI DDC CURRENT LIMIT
(55mA requirement per DVI spec)



Isolation required for DVI power switch



3V LEVEL SHIFTERS



NET_TYPE		
ELECTRICAL_CONSTRAINT_SET	SPACING	PHYSICAL
	TMDS	TMDS_CLK_R_P
	TMDS	TMDS_CLK_R_N
	TMDS	TMDS_DATA_R_P<5..0>
	TMDS	TMDS_DATA_R_N<5..0>
	TMDSCONN	TMDS_CLK_F_P
	TMDSCONN	TMDS_CLK_F_N
	TMDSCONN	TMDS_DATA_F_P<5..0>
	TMDSCONN	TMDS_DATA_F_N<5..0>

External Display Connector

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	75	81

Secure Signal List

Nets must be buried with no exposed vias between parts listed in SECURE_NET property. No test points allowed between the secure devices, test points are allowed past the secure devices except on nets marked as NO_TEST=TRUE, no test points are allowed on those nets.

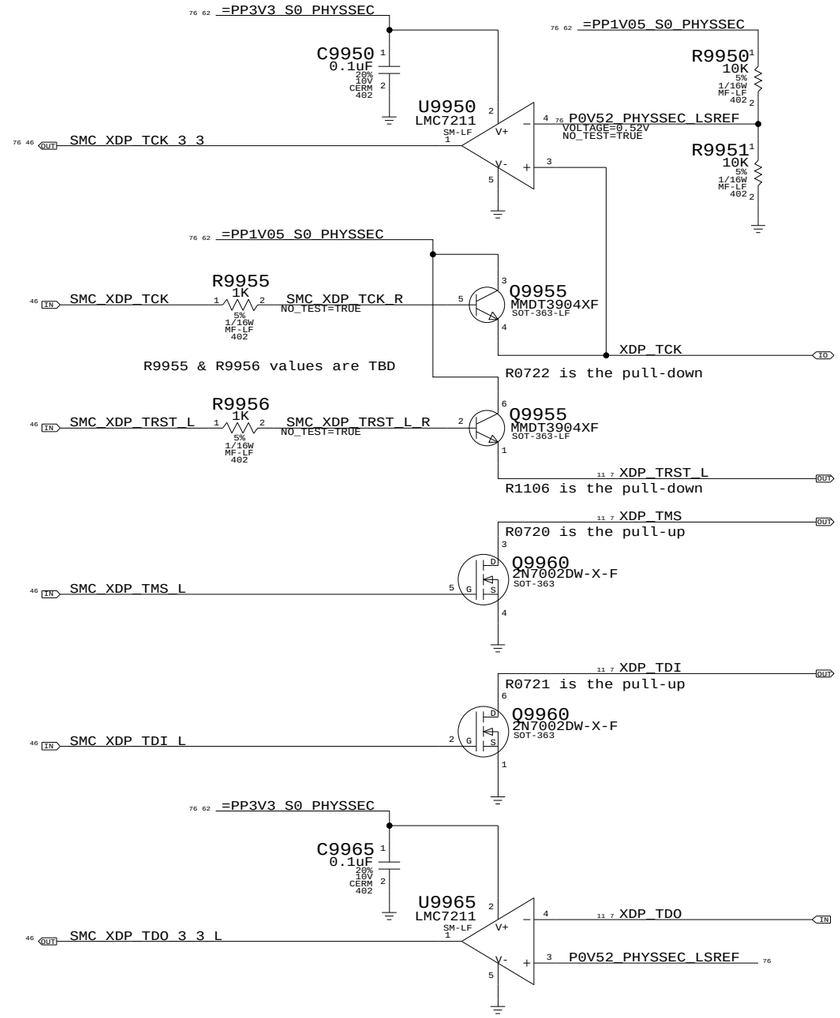
SECURE_NET=U2100:U5800		SPI_CE_L	22 46 51
SECURE_NET=U2100:U5800		SPI_SO	22 46 51
SECURE_NET=U2100:U5800		SPI_SI	22 46 51
SECURE_NET=U2100:U5800	NO_TEST=TRUE	SPI_ARB	22 46
SECURE_NET=U5800:U7530		BOOT_LPC_SPI_L	5 22 46 48
SECURE_NET=U5800:U7530		IMVP_VR_ON	46 56
SECURE_NET=U0700:U9950:Q9955		XDP_TCK	7 11 76
SECURE_NET=U9950:U5800		SMC_XDP_TCK_3_3	46 76
SECURE_NET=U5800:R9955		SMC_XDP_TCK_L	
SECURE_NET=R9955:Q9955		SMC_XDP_TCK_L_R	

NEED TO TURN PCI_GNT3_L INTO A NC NET!

SMC <-> CPU JTAG Level-Shifting

ALL OF THESE PARTS WILL BE COVERED IN EPOXY

Place these parts on one side and as close together as possible, and keep enough room from other parts to leave room for epoxy covering. Nets that are local to this circuit do not need test points as they will not be accessible.



Physical Security

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

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SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	76	81

Date - Radar # - Description

DMS Release #03000 (RFA #394758)

2005/08/11 - 4214109 - Changed J4931 to proper 518S0342 part.
2005/08/12 - 4231030 - Changed pinout of J4960, added placement notes.

Changes from Proto Branch (DMS Release #04000):

2005/08/27 - 4230219 - Changed Y3301 to non-obsoleted part.
2005/08/27 - 4235208 - Changed value of R7707 to fix 2.5V S3 supply.
2005/08/27 - 4235213 - Changed R8305, R8310, R8315 to slow down FET RCs.
2005/08/27 - 4235401 - Moved a few pins at LIO BTB connector.
2005/08/27 - 4227325 - Removed S0 option for camera, now S3-only.
2005/08/27 - 4227369 - Removed SMC options for display/backlight, now GPU-only.
2005/08/27 - 4225433 - Changed PBUS voltage sense circuit.
2005/08/28 - 4217535 - Added Left ALS FFC connector.
2005/08/28 - 4232563 - Changed analog video from Y/C/Comp to G2/R2/B2.
2005/08/28 - 4235203 - Changed BOM settings to stuff R2251.
2005/08/28 - 4217524 - Added LEFT ALS connector (J6430).
2005/08/28 - 4217535 - OMITs and tables to change 4-pin WTB connector parts.
2005/08/28 - 4221973 - Added pull-up for SB GPIO22 (REQ4#).
2005/08/28 - 4225369 - Changed ISL6269 PVCC aliases, added RC for 3.3V S5.
2005/08/28 - 4225433 - Changed PBUS Voltage Sense circuit.
2005/08/28 - 4227322 - Changed FW323 PCI_VIOS pin from 3.3V S0 to 3.3V S3.
2005/08/28 - 4235179 - OMIT and table to change 8-pin DC-In connector to 6-pin.
2005/08/28 - 4235179 - Changed PBUS net names to merge PBUS A & PBUS B.
2005/08/28 - 4232715 - Added FireWire ISense resistor, changed INA193 to INA194.
2005/08/28 - 4235217 - Added RC on Q3820 gate to slow down ODD FET turn-on.
2005/08/28 - 4225369 - OMITs and tables for staged LeMenu BOM approach.
2005/08/28 - 4227323 - Repinned Top-Case Flex connector.

DMS Checkin #04001

2005/08/29 - 4235179 - Changed J8200 to proper 6-pin part.
2005/08/29 - 4232826 - Changed MEM_ODT* from RPAKs to discrete Rs.
2005/08/29 - 4217524 - Changed R6430 from 4.5K to 3.5K.
2005/08/29 - 4237119 - Changed LIO 5V S3 to 5V S5.
2005/08/29 - 4225369 - Changed 3.3V S5 sequence to follow 5V S5 PGOOD.
2005/08/29 - 4227336 - Changed Y5920 to 197S0169.
2005/08/29 - 4227309 - Resolved sync issues with M38 (SB page 21).
2005/08/29 - 4227310 - Resolved sync issues with M38 (SB page 22).
2005/08/29 - 4227312 - Resolved sync issues with M38 (SB page 23).
2005/08/29 - 4227322 - Sync page 44 with M42 to fix FW power net S-states.
2005/08/29 - 4227332 - Resolved sync issues with M38 (SMC page 58).
2005/08/29 - 4227335 - Changed U5900 to resolve ROHS issue.

DMS Checkin #04002

2005/08/30 - 4225433 - Fixed voltage divider values in PBUS VSense circuit.
2005/08/30 - 4217535 - Removed BOM tables and OMITs for new 4-pin WTB connector.
2005/08/31 - 4214109 - Reversed pinout of J4931 to match updated PCB footprint.
2005/08/31 - 4227328 - Added ESD protection diode on right USB port.
2005/08/31 - 4223808 - Various power supply R/C updates, plus some R/C adds.
2005/08/31 - 4227315 - Changed BSA bus pull-ups from 2K to 10K.
2005/08/31 - 4237025 - Added R8824 and R8827 for GPU memory configuration straps.

DMS Checkin #04003

2005/08/31 - 4240157 - Corrected pinout at SATA/BT conn (J4960) to match flex.
2005/08/31 - 4240150 - Swapped PCIE Mini Card R2D/D2R connections at J5500.
2005/08/31 - 4232563 - Corrected net properties on R2/G2/B2 nets.
2005/08/31 - 4227306 - Swapped primary & alt part numbers for CPU VCore caps.
2005/08/31 - 4240300 - Changed C6455 to a smaller part for cost & MCO.
2005/08/31 - 4240486 - Power line width & neck reductions at PCB request.
2005/08/31 - 4240257 - Swapped some top & bottom EMC connections at DVI connector.

DMS Checkin #04004

2005/08/31 - 4227328 - Changed EMI caps from 50V to 16V to fid in ESD protection.

DMS Checkin #04005

2005/09/02 - 4241087 - Fixed pinout of USB D+/D- at camera connector to match FHB.
2005/09/02 - 4243269 - Inverted GPU VCore control, adjusted supply R values.
2005/09/02 - 4244019 - Moved GPU-related power alias from PP3V3_S0 to PP3V3_S0_GPU.
2005/09/02 - 4240486 - Adjusted line/neck widths, changed J4931 to 518S0371.

DMS Checkin #04006

2005/09/03 - 4232534 - Fixed documentation of battery address on I2C page.
2005/09/03 - 4244484 - Changed P1V5S0_RUNSS circuit to work properly in G3Hot.
2005/09/03 - 4244539 - Added GPUVCORE_PGOOD to 1.2V, 1.8V, & 2.5V S0 sequence.
2005/09/03 - 4227315 - Changed SMBus pull-ups to 4.7K.
2005/09/03 - 4232534 - Added notes for power supplies and connectors.

DMS Checkin #04007

2005/09/06 - 4240486 - Removed NO_TEST property from GPU HSYNC and VSYNC.
2005/09/06 - 4246683 - Removed NO STUFF option from R8805 per ATI request.
2005/09/06 - 4232534 - Fixed label BOM tables to call out proper EEE #'s.

DMS Release #05000-07000 (Proto 2 releases)

2005/09/08 - 4247941 - Net property & name changes to support PCB/ICT requests.
2005/09/08 - 4248911 - Sync with M38 & M42
2005/09/08 - 4214493 - Combined RTC coin cell diodes into dual-diode package.
2005/09/08 - 4229560 - First implementation of Physical Security Guidelines.
2005/09/16 - 4256660 - Updated FUNC_TEST property for merged PBUS.
2005/09/16 - 4229560 - Changed FW PCI REQ/GNT pair for Physical Security.
2005/09/20 - 4214847 - Updated L1970 (old part no longer exists in library).
2005/09/26 - 4239505 - Updated J4200 (old part no longer exists in library).
2005/09/26 - 4274915 - Thermal sensor BOM updates from Proto 2 MLB branch.
2005/09/26 - 4274915 - U6301 part number updated to M1 development BootROM.

Revision History

SYNC_MASTER=N/A SYNC_DATE=N/A

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	77	81

FSB (Front-Side Bus) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FSB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR	*	=3:1_SPACING
FSB_ADDR2ADDR	*	=2:1_SPACING
FSB_ADSTB	*	=3:1_SPACING
FSB_ADDR2ADSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA	*	=3:1_SPACING
FSB_DATA2DATA	*	=2:1_SPACING
FSB_DSTB	*	=3:1_SPACING
FSB_DATA2DSTB	*	=3:1_SPACING

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_COMMON	*	=2:1_SPACING

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ADDR	FSB_ADDR	*	FSB_ADDR2ADDR
FSB_ADDR	FSB_ADSTB	*	FSB_ADDR2ADSTB
FSB_DATA	FSB_DATA	*	FSB_DATA2DATA
FSB_DATA	FSB_DSTB	*	FSB_DATA2DSTB

All FSB signals with impedance requirements are 55-ohm single-ended.
Worst-case spacing is 2:1 within Addr bus, with 3:1 spacing to the ADSTBs.
Worst-case spacing is 2:1 within Data bus, with 3:1 spacing to the DSTBs.
DSTB complementary pairs are spaced 3:1, even in constraint areas.

Design Guide recommends each strobe/signal group is routed on the same layer.
Design Guide recommends FSB signals be routed only on internal layers.

NOTE: Design Guide does not indicate FSB spacing to other signals, assumed 3:1.
NOTE: Design Guide allows closer spacing if signal lengths can be shortened.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.2 & 4.3

CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_27P4S	*	Y	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CPU_2TO1	*	=2:1_SPACING
CPU_COMP	*	25 MIL
CPU_GTLREF	*	25 MIL
CPU_ITP	*	=2:1_SPACING
CPU_VCCSENSE	*	25 MIL

DG recommends at least 25 mils, >50 mils preferred

Most CPU signals with impedance requirements are 55-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 4.4, 4.6.2, & 5.8.2.4

DDR2 Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S	*	Y	=45_OHM_SE	=45_OHM_SE	=45_OHM_SE	=STANDARD	=STANDARD
MEM_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
MEM_70D	*	Y	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF	=70_OHM_DIFF
MEM_85D	*	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_CLK2MEM	*	=4:1_SPACING
MEM_CTRL2CTRL	*	=2:1_SPACING
MEM_CTRL2MEM	*	=3:1_SPACING
MEM_CMD2CMD	*	=1.5:1_SPACING
MEM_CMD2MEM	*	=3:1_SPACING
MEM_DATA2DATA	*	=1.5:1_SPACING
MEM_DATA2MEM	*	=3:1_SPACING
MEM_DQS2MEM	*	=3:1_SPACING
MEM_2OTHER	*	25 MIL

Need to support MEM_*-style wildcards!

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 6.2

PCI-Express / DMI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
DMI_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCIE	*	20 MIL
DMI	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 7.2, 9.2 & 10.5.2

Disk Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
IDE_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SATA_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
IDE	*	=1.8:1_SPACING
SATA	*	20 MIL

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Sections 10.6 & 10.7.2

Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
AUDIO_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
AUDIO	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.9.1

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
USB2_90D	*	Y	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
USB2	*	=4:1_SPACING
USB2_2CLK	*	25 MIL

DG says minimum spacing 50 mils to clocks

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.10.1.2

Internal Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
SPI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
SMB	*	=3:1_SPACING
SPI	*	=1.8:1_SPACING

SOURCE: Napa Platform DG, Rev 0.9 (#17978), Section 10.17.1.1

Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_FSB_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_PCIE_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
CLK_MED_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_SLOW_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	*	25 MIL
CLK_PCIE	*	20 MIL
CLK_MED	*	20 MIL
CLK_SLOW	*	10 MIL

Napa Platform Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	78	81

GDDR3 (Frame Buffer) Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FB_35S_TO_55S	*	Y	=35_OHM_SE	=55_OHM_SE	=35_55_OHM_SE	=STANDARD	=STANDARD
FB_40S	*	Y	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
FB_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
FB_75D	*	Y	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF	=75_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FB_ADCTRL	*	=2.5:1_SPACING
FB_CLK	*	=2.5:1_SPACING
FB_DATA	*	=2.5:1_SPACING

ADDR/CTRL lines should route 35-ohms to T, then 55-ohms to each VRAM device.
CTRL lines are 55-ohm single-ended impedence.
DQ/DQM/DQS lines are 40-ohm single-ended impedence.

NOTE: CLK lines are specified in Layout Guide as 40-ohm single-ended. We treat as 75-ohm differential.
NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LVDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
TMDS_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
VGA_75S	*	Y	=75_OHM_SE	=75_OHM_SE	=75_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS	*	=3:1_SPACING
TMDS	*	=3:1_SPACING
VGA	*	15 MIL

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
LVDS_PAIR2PAIR	*	25 MIL
TMDS_PAIR2PAIR	*	25 MIL

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	LVDS	*	LVDS_PAIR2PAIR
TMDS	TMDS	*	TMDS_PAIR2PAIR

LVDS and TMDS signals are 100-ohm +/- 10% differential impedence.
LVDS and TMDS pairs should be kept at least 25 mils apart.
Ground shields can be used around each pair if spacing cannot be met.
VGA should be routed as close to 75-ohms single-ended impedence as possible.
VGA signals should be kept at least 15 mils from other traces.
Ground shields recommended around VGA signals.

NOTE: Layout Guide does not specify LVDS/TMDS spacing to other traces other than "do not run close"

SOURCE: ATI Layout Guide, Rev 0.5 (DSG-216MOBRADEON-05), Sections 7 & 8.1.2.

High-Speed I/O Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	Y	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
FW_110D	*	Y	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
ENET	*	=3:1_SPACING
FW	*	=3:1_SPACING

note

PCI Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCI_55S	*	Y	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
PCI	*	=2:1_SPACING

More System Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	79	81

M1 Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.2

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=55_OHM_SE	=55_OHM_SE	12.7 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.100 MM	0.100 MM			
55_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.124 MM	0.124 MM			
50_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
45_OHM_SE	TOP,BOTTOM	Y	0.150 MM	0.150 MM			
45_OHM_SE	*	Y	0.105 MM	0.105 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.185 MM	0.185 MM			
40_OHM_SE	*	Y	0.131 MM	0.131 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.230 MM			
35_OHM_SE	*	Y	0.165 MM	0.165 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.335 MM	0.335 MM			
27P4_OHM_SE	*	Y	0.240 MM	0.240 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
35_55_OHM_SE	TOP,BOTTOM	Y	0.230 MM	0.100 MM			
35_55_OHM_SE	*	Y	0.165 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

Unsupported rule

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_SE	*	Y	0.076 MM	0.076 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
70_OHM_DIFF	*	Y	0.149 MM	0.149 MM	=STANDARD	0.125 MM	0.125 MM
70_OHM_DIFF	TOP,BOTTOM	Y	0.185 MM	0.185 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
75_OHM_DIFF	*	Y	0.131 MM	0.131 MM	=STANDARD	0.125 MM	0.125 MM
75_OHM_DIFF	TOP,BOTTOM	Y	0.161 MM	0.161 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	Y	0.115 MM	0.111 MM	=STANDARD	0.125 MM	0.125 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	Y	0.101 MM	0.101 MM	=STANDARD	0.125 MM	0.125 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.125 MM		0.125 MM	0.125 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	Y	0.102 MM	0.102 MM	=STANDARD	0.220 MM	0.220 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.130 MM	0.130 MM		0.220 MM	0.220 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	Y	0.080 MM	0.080 MM	=STANDARD	0.200 MM	0.200 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.099 MM	0.099 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	Y	0.076 MM	0.076 MM	=STANDARD	0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.089 MM	0.089 MM		0.330 MM	0.330 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
DEFAULT	*	0.1 MM
STANDARD	*	=DEFAULT
BGA_P1MM	*	=DEFAULT
BGA_P2MM	*	=DEFAULT
BGA_P3MM	*	=DEFAULT

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_FSB	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_MED	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM
FB_CLK	*	BGA	BGA_P2MM
FSB_DSTB	FSB_DSTB	BGA	BGA_P3MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	*	0.15 MM
1.8:1_SPACING	*	0.18 MM
2:1_SPACING	*	0.2 MM
2.5:1_SPACING	*	0.25 MM
3:1_SPACING	*	0.3 MM
4:1_SPACING	*	0.4 MM

Allow 0.1 MM on blind-to-buried via dogbones (layers 2 & 11)

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
1.5:1_SPACING	ISL2,ISL11	0.1 MM
1.8:1_SPACING	ISL2,ISL11	0.1 MM
2:1_SPACING	ISL2,ISL11	0.1 MM
2.5:1_SPACING	ISL2,ISL11	0.1 MM
3:1_SPACING	ISL2,ISL11	0.1 MM
4:1_SPACING	ISL2,ISL11	0.1 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
CLK_FSB	ISL2,ISL11	0.1 MM
CLK_PCIE	ISL2,ISL11	0.1 MM
CLK_MED	ISL2,ISL11	0.1 MM
CLK_SLOW	ISL2,ISL11	0.1 MM
CPU_COMP	ISL2,ISL11	0.1 MM
CPU_GTLREF	ISL2,ISL11	0.1 MM
CPU_VCCSENSE	ISL2,ISL11	0.1 MM
DMI	ISL2,ISL11	0.1 MM
LVDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
MEM_2OTHER	ISL2,ISL11	0.1 MM
PCIE	ISL2,ISL11	0.1 MM
SATA	ISL2,ISL11	0.1 MM
TMDS_PAIR2PAIR	ISL2,ISL11	0.1 MM
VGA	ISL2,ISL11	0.1 MM

Rules for "Topology #3" for FSB signals, Napa DG tables 4-7 & 4-12.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_ADDR OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADDR OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_ADDR2ADSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
FSB_DATA OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DATA OVERRIDE	* OVERRIDE	=STANDARD OVERRIDE
FSB_DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE
FSB_DATA2DSTB OVERRIDE	* OVERRIDE	=2:1_SPACING OVERRIDE

NET_PHYSICAL_TYPE	AREA_TYPE	PHYSICAL_RULE_SET
LVDS	*	LVDS_100D
TMDS	*	TMDS_100D
TMDSCONN	*	TMDS_100D
VGA	*	VGA_75S

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING
MEM_2OTHER OVERRIDE	* OVERRIDE	0.5 MM OVERRIDE

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENETCONN	*	*	ENET
TMDSCONN	*	*	TMDS

"Stale" physical / spacing types

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
FSB_ANALOG	*	*	FSB_COMMON
FSB_P2MM	*	*	FSB_COMMON
I2C	*	*	SMB
GND	*	*	STANDARD
MEM_PP1V8_S3	*	*	STANDARD
FB_PP1V8	*	*	STANDARD

FSB_ANALOG
FSB_P2MM
I2C
GND
MEM_PP1V8_S3
FB_PP1V8
PCI PCI_55S

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_45S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_70D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.100 MM OVERRIDE	OVERRIDE	OVERRIDE	OVERRIDE

M1 Spacing & Physical Constraints

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

SIZE	DRAWING NUMBER	REV.
D	051-6941	07001

SCALE	SHT	OF
NONE	80	81

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	SPACING		
	FSB_55S	FSB_COMMON	FSB_ADS_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BNR_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_BPRI_L	7 12
	FSB_55S	FSB_COMMON	FSB_BREQ0_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DBSY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_DEFER_L	7 12
	FSB_55S	FSB_COMMON	FSB_DPWR_L	7 12
	FSB_55S	FSB_COMMON	FSB_DRDY_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HIT_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_HITM_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_LOCK_L	5 7 12
	FSB_55S	FSB_COMMON	FSB_RS_L<2..0>	7 12
	FSB_55S	FSB_COMMON	FSB_TRDY_L	7 12
	FSB_55S	FSB_COMMON	FSB_CPURST_L	7 11 12 47
	FSB_55S	FSB_DATA	FSB_D_L<63..0>	5 7 12
	FSB_55S	FSB_DATA	FSB_DINV_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBP_L<3..0>	5 7 12
	FSB_55S	FSB_DSTB	FSB_DSTBN_L<3..0>	5 7 12
	FSB_55S	FSB_ADDR	FSB_A_L<31..3>	5 7 12
	FSB_55S	FSB_ADDR	FSB_REQ_L<4..0>	5 7 12
	FSB_55S	FSB_ADSTB	FSB_ADSTB_L<3..0>	5 7 12
	CPU_55S		FSB_IERR_L	7
	CPU_55S		FSB_FERR_L	
	CPU_55S		CPU_PWRGD	7 21
	CPU_55S		CPU_INTR	7 21
	CPU_55S		CPU_NMI	7 21
	CPU_55S		CPU_A20M_L	7 21
	CPU_55S		CPU_DPSLP_L	7 21
	CPU_55S		CPU_IGNNE_L	7 21
	CPU_55S		CPU_INIT_L	7 21
	CPU_55S		CPU_SMI_L	7 21
	CPU_55S		CPU_STPCLK_L	7 21
	CPU_55S	CPU_2TO1	CPU_THERMTRIP_L	
	CPU_55S	CPU_2TO1	PM_DPRSLPVR	14 23 56
	CPU_55S	CPU_2TO1	IMVP_DPRSLPVR	56
	CPU_55S	CPU_GTLREF	CPU_GTLREF	7
	CPU_55S	CPU_COMP	CPU_COMP<3>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<2>	7
	CPU_55S	CPU_COMP	CPU_COMP<1>	7
	CPU_27P4S	CPU_COMP	CPU_COMP<0>	7
	CPU_55S	CPU_ITP	XDP_BPM_L<5..0>	7 11
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_P	11 34
	CLK_FSB_100D	CPU_ITP	CPU_XDP_CLK_N	11 34
	CPU_55S	CPU_ITP	ITPRESET_L	11
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_55S	CPU_2TO1	CPU_VID<6..0>	8 9 81
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	8 56
	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	8 56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_P	56
	CPU_27P4S	CPU_VCCSENSE	IMVP6_VSEN_N	56

MEM_CLK	MEM_70D	
MEM_CTRL	MEM_45S	
MEM_CMD	MEM_55S	
MEM_DATA	MEM_55S	
MEM_DQS	MEM_85D	
FB_CLK	FB_75D	
FB_ADCTRL	FB_35S_TO_55S	
FB_ADCTRL	FB_55S	
FB_DATA	FB_40S	
LVDS	LVDS_100D	
TMDS	TMDS_100D	
VGA	VGA_75S	
PCIE	PCIE_100D	
DMI	DMI_100D	
SATA	SATA_100D	
IDE	IDE_55S	
USB2	USB2_90D	
ENET	ENET_100D	
FW	FW_110D	
SMB	SMB_55S	
SPI	SPI_55S	
CLK_FSB	CLK_FSB_100D	
CLK_PCIE	CLK_PCIE_100D	
CLK_MED	CLK_MED_55S	
CLK_SLOW	CLK_SLOW_55S	

	AUDIO_55S	AUDIO	SB_ACZ_BITCLK	21
	AUDIO_55S	AUDIO	ACZ_BITCLK	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SYNC	21
	AUDIO_55S	AUDIO	ACZ_SYNC	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_RST_L	21
	AUDIO_55S	AUDIO	ACZ_RST_L	5 21 44
	AUDIO_55S	AUDIO	ACZ_SDATAIN<0>	5 21 44
	AUDIO_55S	AUDIO	SB_ACZ_SDATAOUT	21
	AUDIO_55S	AUDIO	ACZ_SDATAOUT	5 21 44

	TMDS	TMDS	TMDS_CLK_P	73 74 75
	TMDS	TMDS	TMDS_CLK_N	73 74 75
	TMDS	TMDS	TMDS_DATA_P<5..3>	73 74 75
	TMDS	TMDS	TMDS_DATA_N<5..3>	73 74 75
LV0	TMDS	TMDS	TMDS_DATA_P<2..0>	73 74 75
LV1	TMDS	TMDS	TMDS_DATA_N<2..0>	73 74 75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_P	75
	TMDSCONN	TMDSCONN	TMDS_CLK_F_N	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<5..3>	75
	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<5..3>	75
LV2	TMDSCONN	TMDSCONN	TMDS_DATA_F_P<2..0>	75
LV3	TMDSCONN	TMDSCONN	TMDS_DATA_F_N<2..0>	75

M1 Net Properties

SYNC_MASTER=(MASTER) SYNC_DATE=(MASTER)

APPLE COMPUTER INC.

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SCALE	SHT	OF
NONE	81	81